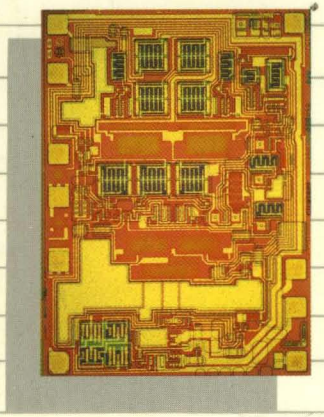

BURR-BROWN

integrated circuits data book

volume 33

BURR-BROWN®

Operational Amplifiers
Instrumentation Amplifiers
Isolation Amplifiers
Analog Circuit Functions
D/S Converters
Analog Circuit Multiplexers
Sample/Hold Amplifiers
A/D Converters
Voltage-to-Frequency Converters
Data Acquisition Components

MODEL INDEX

Individual Product Data Sheets for models not listed here are available from your local Burr-Brown salesperson or representative. See the listing on the inside back cover.

HOW TO USE THIS BOOK

If you know the **MODEL NUMBER,**	Use the Model Index on the **INSIDE FRONT COVER.**
If you know the **PRODUCT TYPE,**	Use the **TABBED TABLE OF CONTENTS** on page *v*. Or, use the **SELECTION GUIDE TABLES** at the front of each tabbed section.
If you know the **MODEL NUMBER FROM ANOTHER MANUFACTURER,**	Use the **CROSS-REFERENCE INFORMATION** in Section 15.
If you want **NEW MODELS,**	Use the Model Index on the **INSIDE FRONT COVER** or the **SELECTION GUIDE TABLES** at the front of each tabbed section. New models are shown in boldface. Contact your local Burr-Brown salesperson or representative for information on new models.
If you want a **PRICE,**	If you are in the U.S.A., see the **U.S.A. PRICE LIST,** Section 16. If you are outside the U.S.A., contact your local Burr-Brown salesperson or representative.
If you want **MILITARY** components,	Contact your local Burr-Brown salesperson or representative. See **INSIDE BACK COVER.**
If you want **DIE,**	Contact your local Burr-Brown salesperson or representative. See **INSIDE BACK COVER.**

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BURR-BROWN INTEGRATED CIRCUITS DATA BOOK

VOLUME 33

BURR-BROWN®

ABOUT BURR-BROWN

Burr-Brown Corporation is a leading designer and manufacturer of precision microcircuits and microelectronic-based systems for use in data acquisition, signal conditioning, measurement, and control.

We make our products for customers who pursue business success much as we do—through worldwide competition based on high performance, high quality, and high value. Our customers include OEMs, sophisticated end-users, systems integrators, and VARs who demand an extra measure of performance for their products and operations.

COMPANY FACTS

- Founded in 1956.
- Corporate headquarters, Tucson, Arizona, U.S.A.
- 1500 employees.
- Manufacturing and technical facilities: Tucson; Livingston, Scotland; Atsugi, Japan.
- Sales and distribution subsidiaries in Austria, Belgium, England, France, Germany, Italy, Japan, the Netherlands, Sweden, and Switzerland; 19 international sales representative organizations worldwide.
- Over 300 sales and service staff worldwide.
- 800+ high-performance products.

BURR-BROWN PRODUCTS

- Precision linear microcircuits, including data converters, operational and instrumentation amplifiers, power amplifiers, and isolation amplifiers. Many military/high reliability models.
- DC/DC converter power supplies in a broad range of input/output ratings.*
- Board-level microcomputer subsystems, including high-speed DSP boards for VME and IBM PC systems; industrial STD boards; and modular PC instrumentation for data acquisition, test, measurement, and control.*
- Data entry terminals, transaction processors, and peripherals for factory data collection, inventory control, labor tracking, and quality assurance. Modems, multiplexers, and network servers for industrial data communications and LANs. See Section 14.

* These items are described in Section 14 and in separate databooks. Also see Section 1.

QUALITY AT BURR-BROWN

BUILT-IN QUALITY AND RELIABILITY GUARANTEE HIGH PERFORMANCE

We have been building quality and reliability into our microcircuits, subsystems, and systems for over 30 years. Today, our manufacturing and quality assurance processes and procedures are backed by millions of units of worldwide experience; we make sure our customers get all the operating performance in their applications that we design into our products.

A SYSTEMS APPROACH TO QUALITY MANUFACTURING

In the manufacture of microcircuits, sophisticated production techniques and test equipment are used to fabricate silicon wafers and fashion them into hybrid and monolithic electronic components. Our engineers have pioneered hundreds of innovations in manufacturing technology, including thin-film deposition processes and wafer-level laser trimming to improve accuracy and stability.

HIGH-PERFORMANCE PEOPLE

Our 1500 worldwide engineers, technicians, managers, and other employees are educated, trained and motivated to continuously improve the products and services demanded by our customers. Employee skills are constantly improved through in-house and community educational programs to meet new operating and competitive challenges. From top to bottom, our people focus on the customer and his needs; everyone is a high-performance partner in your aggregate business success.

GETTING IT RIGHT THE FIRST TIME!

Quality control, like almost everything else at Burr-Brown, begins at the design phase. The completed design is carefully checked prior to production to make sure that it will meet the quality criteria set up for it. Incoming materials from vendors are sampled and carefully inspected to the standard established for each item before going into manufactured product.

During production, our in-line quality control people sample parts from the production line at several stages and inspect partially assembled products against performance criteria. A 100% electrical test performed after production completes the manufacturing cycle.

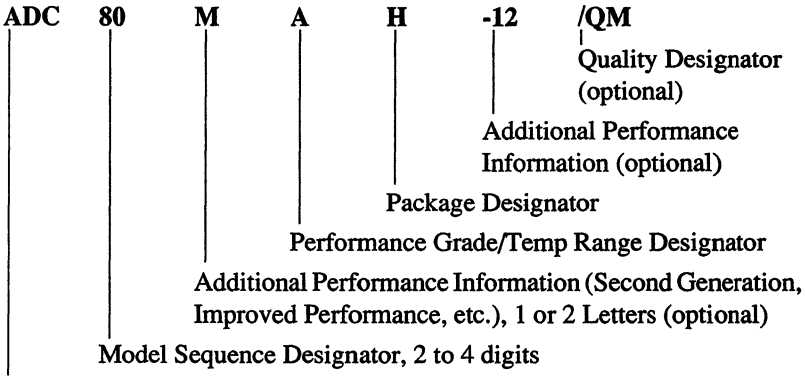
Inspection and testing don't stop when production is completed. Many Burr-Brown products are subjected to "burn-in" at elevated temperatures to catch early or "infant mortality" failures before they reach the customer.

To maintain both quality and on-time delivery, Burr-Brown uses several computerized manufacturing systems. In our AMAPS system, information, such as the location of materials, how they are being used, inventory of parts, and what materials need to be ordered, is collected and analyzed on a regular basis to make sure the work flows smoothly.

We are also now expanding a rigorous Statistical Process Control (SPC) system throughout the company. Our employees are directly involved in all aspects of the manufacturing process, so we "do it right the first time" instead of catching errors later. SPC is a proven technique that represents the future in electronics manufacturing.

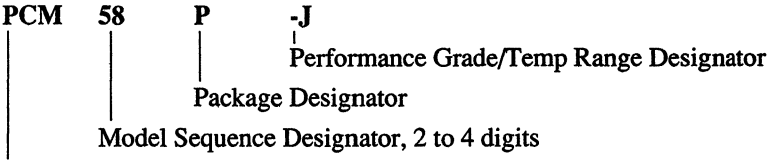
UNDERSTANDING COMPONENT MODEL NUMBERS

Most Burr-Brown component products in this book have model numbers in the following form:



Exceptions: Second-source products are marked as similarly to the original vendor's part number as possible.

Some products designed for digital audio and signal processing applications have model numbers as follows:



PRODUCT TYPE PREFIXES

Product Type	Prefix	Description
Amplifiers	OPA	Operational Amplifier
	INA	Instrumentation Amplifier
	PGA	Programmable Gain Amplifier
	ISO	Isolation Amplifier
Analog Circuit Functions	MFC	Multifunction Converter
	MPY	Multiplier
	DIV	Divider
	LOG	Logarithmic Amplifier
Frequency Products	VFC	Voltage-to-Frequency Converter
	UAF	Universal Active Filter
Conversion Products	ADC	A/D Converter
	ADS	A/D Converter with Sample/Hold
	DAC	D/A Converter
	MPC	Multiplexer
	PCM	A/D and D/A Converters for Audio and Digital Signal Processing
	SDM	System Data Modules
	SHC	Sample/Hold
Miscellaneous	PWS	Power Supply
	PWR	Power Supply
	REF	Reference
	XTR	Transmitter
	RCV	Receiver

PERFORMANCE GRADE AND TEMPERATURE RANGE DESIGNATORS

	Temperature Range		
	0°C to 70°C (Commercial)	–25°C to +85°C [1] (Industrial)	–55°C to +125°C (Military)
Increasing Parametric Performance ↓	H	A	R
	J	B	S
	K	C (best)	T (best)
	L (best)		

NOTE: (1) For some industrial products this may be –40°C to 85°C.

PACKAGE DESIGNATORS

M	Metal (hermetic)
P	Plastic DIP (nonhermetic)
G	Ceramic (hermetic or nonhermetic)
U	SOIC
N	PLCC
L	Ceramic Leadless Chip Carrier
D	Die
H	Ceramic hermetic

QUALITY DESIGNATORS

Q	Burr-Brown's Q program
QM or /QM	Burr-Brown's Q program with Military Visual Criteria
BI or B	Burn-in

WHERE TO GO FROM HERE: BURR-BROWN SALES & SERVICE

GETTING TECHNICAL ASSISTANCE

We have a large and competent field sales force, backed up by an experienced staff of technical applications specialists. They are eager to assist you in selecting the right product for your application. This free service is available from our Tucson-based headquarters and all sales offices.

GETTING PRODUCT DATA SHEETS AND OTHER TECHNICAL LITERATURE

Burr-Brown uses Product Data Sheets (PDSs) to describe its components. This Data Book is a compilation of PDSs for products *recommended for new designs* at the time of publication (1/89). You can receive individual PDSs for older products, new introductions, or revisions of existing products by contacting your local Burr-Brown salesperson or representative. See the listing on the inside back cover.

HOW TO PLACE AN ORDER

You can place orders via telephone, FAX, mail, TWX, or TELEX with any authorized Burr-Brown field sales office, sales representative, or our headquarters in Tucson. A complete list of sales offices is on the inside back cover of this book. When placing an order, please provide complete information, including model number with all option designations, product description or name, quantity desired, and ship-to and bill-to addresses. This will help us serve you most efficiently.

PRICES AND TERMS

Prices listed in this catalog are effective until March 31, 1989 and unless otherwise noted apply only to domestic U.S.A. customers. All other customers should contact their local Burr-Brown sales office for pricing. Prices and specifications are subject to change without notice.

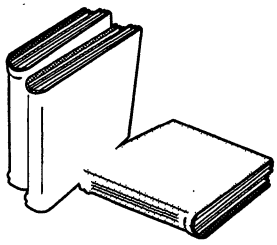
For U.S.A. customers all prices are FOB Tucson, Arizona, U.S.A., in U.S. dollars. Applicable federal, state, and local taxes are extra. Terms are net 30 days.

QUOTATIONS

Price quotations made by Burr-Brown or its authorized field sales representatives are valid for 30 days. Delivery quotations are subject to reconfirmation at the time of order placement.

RETURNS AND WARRANTY SERVICE

When returning products for any reason, it is necessary to contact Burr-Brown prior to shipping for authorization and shipping instructions. In the U.S.A., contact our Tucson headquarters. In other countries, contact your local Burr-Brown sales office or representative. Please ship returned units prepaid and supply the original purchase order number and date, along with an explanation of the malfunction. Upon receipt of the returned unit, Burr-Brown will verify the malfunction and will inform you of the warranty status, cost to repair or replace, credits, and status of replacement units where applicable.



1

BURR-BROWN TECHNICAL LITERATURE

An extensive library of Burr-Brown technical literature is available to design engineers and others interested in using Burr-Brown components. Contact your local Burr-Brown salesperson or representative for the items you need. See the listing on the inside back cover.

PRODUCT DATA SHEETS (PDSs)

Individual PDSs similar to those in this book are available. You may want to request a particular PDS to get the most recent version or to obtain information on products not featured here. This last group includes new products not introduced when this book was created and those listed in Other Products Still Available tables in the introductory material of each section.

MILITARY PRODUCTS DATA BOOK

This publication covers the complete line of Burr-Brown military/high reliability components and die. Burr-Brown's Military Products Division facilities have been certified to both MIL-STD-976 and MIL-STD-1772. All product families are fully specified from –55°C to +125°C with up to three performance grades at the /883B product assurance level. For more information, see page 14-5.

The *Military Products Data Book* will be available in Second Quarter 1989. To obtain a copy, contact your local Burr-Brown salesperson or representative. See the listing on the inside back cover.

POWER SOURCES HANDBOOK

Burr-Brown offers a wide selection of power conversion products, all completely described in this useful book. In addition to containing detailed PDSs, it also has an extensive selection guide, a discussion of advanced reliability programs, a glossary of terms, and application notes for effective

use of these products. For more information, see pages 14-1 to 14-4.

The *Power Sources Handbook* will be available in early 1989. To obtain a copy, contact your local Burr-Brown salesperson or representative.

RELIABILITY REPORTS

Burr-Brown performs extensive reliability evaluations of new products and processes. Copies of these reports are available from your local Burr-Brown salesperson or representative.

APPLICATIONS HANDBOOK

This is a booklength collection of more than 50 Application Notes written by Burr-Brown's engineering staff. It offers practical, detailed information on the most popular components, such as those covered in this book—operational amplifiers, isolation amplifiers, digital-to-analog converters, analog-to-digital converters, and more.

UPDATE

Burr-Brown publishes this full-color supplement several times a year to keep our customers informed about new product developments, supporting literature, and applications.

TECHNICAL BOOKS

Burr-Brown engineers, in cooperation with McGraw-Hill, have authored the world's most extensive and authoritative library dealing with the art of analog signal conditioning, conversion, and computation. These four hard-bound books, described below, are respected and referenced throughout the international engineering community. They are available to you directly from Burr-Brown.

FUNCTION CIRCUITS: Design and Applications

This volume is the first to cover the multifaceted area of analog function circuits. It explores in depth both the design theory and numerous applications for such analog functions as Multipliers, Dividers, Logarithmic Amplifiers, Exponentiators, RMS-to-DC Converters, and Active Filters. It also clearly shows how to specify and test these functions, which are increasingly becoming available in integrated circuit form. (more than 300 pages, 200 illustrations)

OPERATIONAL AMPLIFIERS: Design and Applications

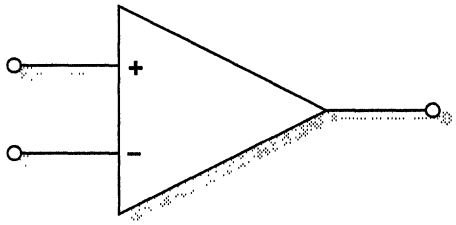
This pioneering work provides practical information you can directly apply to instrumentation design. It covers basic theory, test methods, amplifier design techniques, and applications. Part I discusses the design of operational amplifiers, offering insight into factors determining performance characteristics, and outlines techniques for their control. Part II presents a wide range of practical operational amplifier applications, and provides sufficient descriptions of operation to permit design adaptation from the specific circuits described. (more than 470 pages, 300 illustrations)

APPLICATIONS OF OPERATIONAL AMPLIFIERS: Third Generation Techniques

The second volume of the Operational Amplifier series, this book is much more than just a collection of circuit or theoretical analysis. It also presents numerous applications of operational amplifiers in a variety of electronic equipment—specialized amplifiers, signal controls, processors, waveform generators, and special-purpose circuits. It is a storehouse of detailed, practical information, featuring numerous circuit diagrams, circuit values, pertinent design equations, error sources and test-based comments on the efficiency of the arrangements and devices. (more than 230 pages, 170 illustrations)

DESIGNING WITH OPERATIONAL AMPLIFIERS: Applications Alternatives

The latest volume of the Operational Amplifier series offers a wealth of innovative applications and circuit techniques that have recently been developed. Example applications include complete explanations of circuit operations, allowing you to efficiently develop further circuits. Practical limitations are also discussed, in addition to pertinent design equations that can be adapted to your specific requirements. (more than 270 pages, 200 illustrations)



OPERATIONAL AMPLIFIERS

2

APPLICATION GROUPS

Burr-Brown operational amplifiers are listed in eight applications groups described below. This helps you determine and select the best operational amplifier available for a design. Instrumentation amplifiers and isolation amplifiers are described in Sections 3 and 4 respectively.

LOW DRIFT

Low drift operational amplifiers are best suited for applications where accuracy must be preserved over a substantial temperature range. These amplifiers are optimized to minimize the initial input offset voltage and input offset voltage change with temperature. Input offset drifts from 0.1μV/°C to 5μV/°C are available within this group.

LOW BIAS CURRENT

Low bias current operational amplifiers consist of FET input designs. This group includes amplifiers with input bias currents from 0.01pA to 50pA. Applications with large feedback resistances or large source resistances (long time constants, integrators, current sources, etc.) and buffer applications will benefit by the use of low bias current amplifiers.

LOW NOISE

This group contains low noise bipolar and FET input operational amplifiers. Burr-Brown units offer guaranteed noise spectral density, 100% tested. In applications such as low noise signal conditioning, light measurements, radiation measurements, photodiode circuits or low noise data acquisition, the fully characterized and tested voltage noise performance of these units allows the designer to truly bound noise errors.

WIDEBAND

Wideband operational amplifiers have bandwidths greater than 5MHz. This group also contains fast settling and high slew rate amplifiers. These amplifiers reduce phase errors at high frequencies and accurately reproduce complex waveforms. These amplifiers are well suited for pulse, video, fast settling, and multiplexing applications.

HIGH VOLTAGE

Amplifiers in this group are designed to provide large output voltage swings and to operate on wide ranges of supply voltage. Output voltages from ±10V and ±145V (up to 290V, single supply) are available in this applications group. These amplifiers provide good frequency response and performance in other parameters. Most models have electrically isolated packages and automatic thermal sensing and shutdown. All units have FET inputs to minimize bias current errors when the amplifier is used with the large resistances usually found with high-voltage amplifiers.

HIGH CURRENT

These amplifiers provide output currents from ±1A to ±10A. They are used with small load resistances, coax cable driving, and with power booster applications. Many units have self-contained thermal sensing and shutdown to automatically protect the amplifiers from overheating and damage. All of these units have electrically isolated packages.

UNITY-GAIN BUFFER (POWER BOOSTER)

Unity-gain buffer amplifiers have a wide variety of applications. They are used to boost the output current capability of another amplifier, buffer an impedance that might load a critical circuit or to be an input impedance converter from an input that must not be loaded. These amplifiers may also be used inside the feedback loop of another operational amplifier to form a current-boosted composite amplifier.

SPECIAL PURPOSE

Special purpose op amps provide features or performance that don't fit conventional categories. These include op amps specified for very wide temperature range and devices with switchable inputs.

OPERATIONAL AMPLIFIERS SELECTION GUIDES

The following Selection Guides show parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

LOW DRIFT

Low offset voltage drift vs temperature performance in both FET and bipolar input types is obtained by our sophisticated drift compensation techniques. First, the drift is measured and then special laser trim techniques are used to minimize the drift and the initial offset voltage at 25°C. Finally, "max drift" performance is retested for conformance with specifications.

LOW DRIFT (≤5μV/°C) **Boldface = NEW**

Description	Model	Offset Voltage, max: At 25°C, (±mV)	Offset Voltage, max: Temp Drift, (±μV/°C)	Bias Current (25°C), max (nA)	Open Loop Gain, min (dB)	Frequency Response: Unity Gain (MHz)	Frequency Response: Slew Rate (V/μs)	Rated Output, min: (±V)	Rated Output, min: (±mA)	Temp Range[1]	Pkg	Page
FET	**OPA627M**	**0.1**	**0.8**	**20**	**110**	**16**	**45**	**12**	**30**	**Ind**	**TO-99**	**2-174**
	OPA627P	**0.25**	**2**	**50**	**104**	**16**	**40**	**12**	**30**	**Ind**	**DIP**	**2-174**
	OPA111M	0.25	1	±0.001	120	2	2	11	5	Ind	TO-99	2-55
Wideband	OPA156M	2	5	0.05	94	6	14	10	5	Mil	TO-99	2-80
	OPA356M	2	5	0.05	94	6	14	10	5	Com	TO-99	2-80
	OPA602M	**0.25**	**2**	**±.001**	**92**	**6.5**	**28**	**10**	**15**	**Ind**	**TO-99**	**2-145**
	OPA602P	**0.5**	**5**	**±.002**	**88**	**6.5**	**24**	**10**	**15**	**Ind**	**DIP**	**2-145**
	OPA606M	0.5	5	±0.01	100	13	35	12	5	Com	TO-99	2-158
Dual FET	OPA2111M	0.5	2.8	±0.004	114	2	2	11	5	Ind	TO-99	2-195
	OPA2107P	**0.5**	**5**	**0.006**	**80**	**5**	**15**	**11**	**10**	**Ind**	**DIP**	**2-193**
Bipolar	OPA27J, Z	0.025	0.6	±40	120	8	1.9[3]	12	16.6	Mil	TO-99, DIP	2-27
	OPA37J, Z	0.025	0.6	±40	120	63[2]	11.9[3]	12	16.6	Mil	TO-99, DIP	2-27
	OPA27P	0.100	1.8	±80	117	8	1.9[3]	12	16.6	Com	DIP	2-27
	OPA37P	0.100	1.8	±80	117	63[2]	11.9[3]	12	16.6	Com	DIP	2-27
Low Power	OPA21Z	0.1	1	25	120	0.3	0.2	13	5	Ind	DIP	2-21

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) Gain-bandwidth product for OPA37. A_V = 5 min. (3) Typical.

LOW BIAS CURRENT

Our many years of experience in designing, manufacturing and testing FET amplifiers give us unique abilities in providing low and ultra-low bias current op amps. These amplifiers offer bias currents as low as 75fA (75 x 10^{-15}A) and voltage drift as low as 1μV/°C. With offset voltage laser-trimmed to as low as 250μV, the need for expensive trim pot adjustments is eliminated.

LOW BIAS CURRENT (≤50pA) **Boldface = NEW**

Description	Model	Offset Voltage, max: At 25°C, (±mV)	Offset Voltage, max: Temp Drift, (±μV/°C)	Bias Current (25°C), max (pA)	Open Loop Gain, min (dB)	Frequency Response: Unity Gain (MHz)	Frequency Response: Slew Rate (V/μs)	Rated Output, min: (±V)	Rated Output, min: (±mA)	Temp Range[1]	Pkg	Page
FET	OPA111M	0.25	1	±1	120	2	2	11	5	Ind	TO-99	2-55

(Continued on next page.)

LOW BIAS CURRENT (≤50pA) (Continued) **Boldface = NEW**

Description	Model	Offset Voltage, max: At 25°C, (±mV)	Offset Voltage, max: Temp Drift, (±µV/°C)	Bias Current (25°C), max (pA)	Open Loop Gain, min (dB)	Frequency Response: Unity Gain (MHz)	Frequency Response: Slew Rate (V/µs)	Rated Output, min: (±V)	Rated Output, min: (±mA)	Temp Range[1]	Pkg	Page
FET	**OPA627M**	**0.1**	**0.8**	**20**	**110**	**16**	**45**	**12**	**30**	**Ind**	**TO-99**	**2-174**
	OPA627P	**0.25**	**2**	**50**	**104**	**16**	**40**	**12**	**30**	**Ind**	**DIP**	**2-174**
Low Noise	OPA101M	0.25	5	–10	94	10	6.5	12	12	Ind	TO-99	2-43
	OPA102M	0.25	5	–10	94	40	14	12	12	Ind	TO-99	2-43
Ultra-Low Bias Current	OPA128M	0.5	5	±0.075	110	1	3	10	5	Com	TO-99	2-72
	AD515H	1	25	0.075	88	0.35	1	10	5	Com	TO-99	2-13
Dual FET	OPA2111M	0.5	2.8	±4	114	2	2	11	5	Ind	TO-99	2-195
	OPA2111P	2	15	±15	106	2	2	11	5	Com	DIP	2-195
	OPA2107P	**0.5**	**5**	**6**	**80**	**5**	**15**	**11**	**10**	**Ind**	**DIP**	**2-193**
Quad FET	OPA404G	0.75	3[2]	±4	92	6.4	35	12	5	Ind	DIP	2-94
	OPA404P	2.5	5[2]	±12	88	6.4	35	11.5	5	Com	DIP	2-94
Low Cost	OPA121M	2	10	±5	110	2	2	11	5	Com	TO-99	2-66
	OPA121P	3	10	±10	106	2	2	11	5	Com	DIP	2-66
	OPA602M	**0.25**	**2**	**1**	**92**	**6.5**	**28**	**10**	**15**	**Ind**	**TO-99**	**2-145**
	OPA602P	**0.5**	**5**	**2**	**88**	**6.5**	**24**	**10**	**15**	**Ind**	**TO-99**	**2-145**
Wideband	OPA606M	0.5	5	±10	100	13	35	12	5	Com	TO-99	2-145
	OPA606P	3	10[2]	±25	90	12	30	11	5	Com	DIP	2-145

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) Typical.

LOW NOISE

Now both FET and bipolar input op amps are offered with guaranteed low noise specifications. Until now the designer had to rely on "typical" specs for his demanding low noise designs. These fully characterized parts allow a truly complete error budget calculation.

LOW NOISE (Very Low e_N) **Boldface = NEW**

Descrip.	Model	Noise Voltage at 10kHz, max (nV/√Hz)	Bias Current (25°C), max (pA)	Offset Voltage, max: at 25°C (±mV)	Offset Voltage, max: Temp Drift (±µV/°C)	Open Loop Gain, min (dB)	Frequency Response: Gain BW (MHz)	Frequency Response: Slew Rate, min (V/µs)	Rated Output, min: (±V)	Rated Output, min: (±mA)	Temp Range[1]	Pkg	Page
Bipolar	OPA27J, Z	3.8	±40nA	0.025	0.6	120	8	1.9[2]	12	16.6	Mil	TO-99, DIP	2-27
	OPA37J, Z	3.8	±40nA	0.025	0.6	120	63	11.9[2]	12	16.6	Mil	TO-99, DIP	2-27
Wide Bandwidth	OPA101M	8	–10	0.25	5	94	20	5	12	12	Ind	TO-99	2-43
	OPA102M	8	–10	0.25	5	94	40	10	12	12	Ind	TO-99	2-43
FET	OPA111M	8	±1	0.25	1	120	2	1	11	5	Ind	TO-99	2-55
	OPA602M	**12[2]**	**1**	**0.25**	**2**	**92**	**6.5**	**28**	**10**	**15**	**Ind**	**TO-99**	**2-145**

(Continued on next page.)

LOW NOISE (Very Low e_N) (Continued) **Boldface = NEW**

Descrip.	Model	Noise Voltage at 10kHz, max (nV/√Hz)	Bias Current (25°C), max (pA)	Offset Voltage, max at 25°C (±mV)	Offset Voltage, max Temp Drift (±µV/°C)	Open Loop Gain, min (dB)	Frequency Response Gain BW (MHz)	Frequency Response Slew Rate, min (V/µs)	Rated Output, min (±V)	Rated Output, min (±mA)	Temp Range[1]	Pkg	Page
FET	**OPA627M**	**5.4**	**20**	**0.1**	**0.8**	**110**	**16**	**45**	**12**	**30**	**Ind**	**TO-99**	**2-174**
	OPA627P	**6.2**	**50**	**0.25**	**2**	**104**	**16**	**40**	**12**	**30**	**Ind**	**DIP**	**2-174**
Low Cost	OPA27P	4.5	±80nA	0.100	1.8	117	8	1.9[2]	10	16.6	Com	DIP	2-27
	OPA37P	4.5	±80nA	0.100	1.8	117	63	11.9[2]	10	16.6	Com	DIP	2-27
Dual FET	OPA2111M	8	±4	0.5	2.8	114	2	1	11	5	Ind	TO-99	2-195
	OPA2111P	6[2]	±15	2	15	106	2	1	11	5	Com	DIP	2-195

NOTES: (1) Ind = –25°C to +85°C, Mil = –55°C to +125°C, Com = 0°C to +70°C. (2) Typical.

UNITY-GAIN BUFFER (POWER BOOSTER)

These versatile amplifiers boost the ouput current capability of another amplifier; buffer an impedance that might load a critical circuit; and may be used inside the feedback loop of another op amp to form a current-boosted, composite amplifier. Currents as high as ±200mA are available with speeds of 2000V/µs.

UNITY-GAIN BUFFER **Boldface = NEW**

Description	Model	Rated Output, min (±V)	Rated Output, min (±mA)	Frequency Responses –3dB (MHz)	Frequency Responses Full Power (MHz)	Frequency Responses Slew Rate (V/µs)	Gain (V/V)	Input Impedance (Ω)	Temp Range[1]	Pkg	Page
High Performance	3553AM	10	200	300	32	2000	≈1	10^{11}	Ind	TO-3	2-225
Low Cost	**OPA633H, P**	**11**	**80**	**275**	**65**	**2500**	**≈1**	**1.5×10^6**	**Ind**	**TO-8, DIP**	**2-176**

NOTE: (1) Ind = –25°C to +85°C.

WIDE BANDWIDTH

Design expertise in wideband circuits combines with our fully developed technology to create cost-effective wideband op amps. Burr-Brown high-speed amplifiers also offer outstanding DC performance specifications.

WIDE BANDWIDTH (≥5MHz)

Descrip.	Model	Frequency Response Gain BW (MHz)	Frequency Response Slew Rate min (V/µs)	Frequency Response t_S ±0.1% (ns)	Comp	Rated Output, min (±V)	Rated Output, min (±mA)	Offset Voltage, max At 25°C (±mV)	Offset Voltage, max Temp Drift (±µV/°C)	Open Loop Gain, min (dB)	Temp Range[1]	Pkg	Page
FET	OPA156M	6	10	1.5µs	int	10	5	2	5	94	Mil	TO-99	2-80
	OPA356M	6	10	1.5µs	int	10	5	2	5	94	Com	TO-99	2-80

(Continued on next page.)

Descrip.	Model	Frequency Response: Gain BW (MHz)	Slew Rate min (V/µs)	t_S ±0.1% (ns)	Comp	Rated Output, min (±V)	Rated Output, min (±mA)	Offset Voltage, max: At 25°C (±mV)	Offset Voltage, max: Temp Drift (±µV/°C)	Open Loop Gain, min (dB)	Temp Range[1]	Pkg	Page
FET	**OPA602M**	**6.5**	**28**	**600**	**int**	**10**	**15**	**0.25**	**2**	**92**	**Ind**	**TO-99**	**2-145**
	OPA602P	**6.5**	**24**	**600**	**int**	**10**	**15**	**0.5**	**5**	**88**	**Ind**	**TO-99**	**2-145**
(Dual)	**OPA2107**	**5**	**15**	**1µs**	**int**	**11**	**10**	**0.5**	**5**	**80**	**Ind**	**DIP**	**2-193**
	OPA605C	200, A=1000	300[3]	300	ext	10	30	0.5	5	96[3]	Ind	DIP	2-152
	OPA606M	13	25	1µs	int	12	5	0.5	5[2]	100	Com	TO-99	2-158
	OPA606P	12	20	1µs	int	11	5	3	10[2]	90	Com	TO-99	2-158
	OPA627M	**16**	**45**	**400**	**int**	**12**	**30**	**0.1**	**0.8**	**110**	**Ind**	**TO-99**	**2-174**
	OPA627P	**16**	**40**	**400**	**int**	**12**	**30**	**0.25**	**2**	**104**	**Ind**	**DIP**	**2-174**
	3554M	1700, A=1000	1000	120	ext	10	100	1	15	100	Ind	TO-3	2-229
	3551	50, A=10	250	400	ext	10	10	1	50[2]	88	Com	TO-99	2-221
	3550	20, A=1	100	400	int	10	10	1	50[2]	88	Com	TO-99	2-217
Bipolar	3508	100, A=100	20	—	ext	10	10	5	30[2]	98	Com	TO-99	2-215
	3507	20, A=10	80	200	ext	10	10	10	30[2]	83	Com	TO-99	2-213
Quad FET	OPA404G	6.4	28	600	int	11.5	5	0.75	3[2]	92	Ind	DIP	2-94
	OPA404P	6.4	24	600	int	11.5	5	2.5	5[2]	88	Com	DIP	2-94
Low Noise Bipolar	OPA27	8,A=1	1.9[2]	—	int[3]	12	16.6	0.025	0.6	120	Mil	TO-99, DIP	2-27
	OPA37	63,A=5	11.9[2]	—	int[3]	12	16.6	0.025	0.6	120	Mil	TO-99, DIP	2-27
Low Noise FET	OPA101M	20, A=100	5	2.5µs	int	12	12	0.25	5	94	Ind	TO-99	2-43
	OPA102M	40, A=100	10	1.5µs	int	12	12	0.25	5	94	Ind	TO-99	2-43
Fast Settling	**OPA600M**	**5000, A=1000**	**500**	**80**	**ext**	**9**	**180**	**4**	**40**	**86**	**Ind**	**DIP**	**2-137**
Very Fast Settling Precision	**OPA620**	**170**	**200[2]**	**10**	**int**	**2.7**	**150[2]**	**0.5**	**5[2]**	**55**	**Com, Mil**	**DIP**	**2-166**
	OPA621	**250, A=10**	**1000[2]**	**10**	**ext**	**2.7**	**150[2]**	**0.5**	**5[2]**	**55**	**Com, Mil**	**DIP**	**2-170**
Very Fast Settling	**OPA675G**	**3000, A=16**	**200**	**15**	**ext**	**2.1**	**30**	**1**	**5**	**65**	**Com, Mil**	**DIP**	**2-186**
Switched Input	**OPA676G**	**3000, A=16**	**200**	**15**	**ext**	**2.1**	**30**	**1**	**5**	**65**	**Com, Mil**	**DIP**	**2-186**
Low Cost	OPA27P	8,A=1	1.9[2]	—	int	12	16.6	0.100	1.8	117	Com	DIP	2-27
	OPA37P	63, A=5	11.9[2]	—	int[3]	12	16.6	0.100	1.8	117	Com	DIP	2-27
Wide Temp Range	OPA11HT	12,A=1	4	1.5µs	ext	10	15	5[2]	5	98	–55/+200°C	TO-99	2-17
	OPA27HT	6,A=1	1.9	—	int	12	16.6[2]	0.050	0.25[2]	120	–55/+200°C	TO-99	2-39

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) Typical. (3) G = 5 min. for OPA37.

HIGH VOLTAGE, HIGH CURRENT — **Boldface = NEW**

Description	Model	Rated Output, min (±V)	Rated Output, min (±mA)	Offset Voltage, max At 25°C (±mV)	Offset Voltage, max Temp Drift (±µV/°C)	Bias Current (25°C), max (pA)	Frequency Response Unity Gain (MHz)	Frequency Response Slew Rate (V/µs)	Open Loop Gain (dB)	Temp Range[1]	Pkg	Page
High Power	OPA501M	26	10A	5	40	20nA	1	1.35	98	Ind	TO-3	2-109
	OPA511M	22	5A	10	65	40	1	1	91	Ind	TO-3	2-117
	OPA512BM	35	10A	6	65	30	4	2.5	110	Ind	TO-3	2-122
	OPA512SM	35	15A	3	40	20	4	2.5	110	Mil	TO-3	2-122
	OPA541M	**35**	**5A**	**1**	**30**	**50**	**1.6**	**8**	**90**	**Ind**	**TO-3**	**2-127**
(Dual)	**OPA2541M**	**35**	**5A**	**1**	**30**	**50**	**1.6**	**8**	**90**	**Ind**	**TO-3**	**2-205**
	OPA550	**35**	**2A**	**1**	**30**	**50**	**3**	**15**	**90**	**Ind**	**TO-220**	**2-135**
	3573M	20	2A[4]	10	65	40nA	1	2.6	94	Ind	TO-3	2-243
	3572M	30	2A[4]	2	40	100	0.5	3	94	Ind	TO-3	2-237
	3571M	30	1A[3]	2	40	100	0.5	3	94	Ind	TO-3	2-237
Wideband	3554M	10	100	1	15	50	1700[2]	1200	100	Ind	TO-3	2-229
High Voltage	3584M	145	15	3	25	20	20[2]	150	126	Com	TO-3	2-255
	3583M	140	75	3	25	20	5	30	118	Ind	TO-3	2-251
	3582	145	15	3	25	20	5	20	118	Com	TO-3	2-247
	3581	70	30	3	25	20	5	20	112	Com	TO-3	2-247
	3580	30	60	10	30	50	5	15	106	Com	TO-3	2-247
	OPA445BM	35	15	3	10	50	2	10	100	Ind	TO-99	2-104
Buffer	3553M	10	200	50	300[5]	200	300	2000	NA	Ind	TO-3	2-225
	OPA633	**11**	**80**	**15**	**33[5]**	**35µA**	**275[5]**	**2500**	**NA**	**Ind**	**TO-8, DIP**	**2-176**

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) Gain-bandwidth product. (3) 2A peak. (4) 5A peak. (5) Typical.

SPECIAL PURPOSE

These op amps offer specialized performance or function, including devices with wide temperature range, low quiescent current, and switched inputs.

SPECIAL PURPOSE — **Boldface = NEW**

Description	Model	Offset Voltage, max At 25°C, (±mV)	Offset Voltage, max Temp Drift, (±µV/°C)	Bias Current (25°C), max (nA)	Open Loop Gain, min (dB)	Frequency Response Unity Gain (MHz)	Frequency Response Slew Rate (V/µs)	Rated Output, min (±V)	Rated Output, min (±mA)	Temp Range[1]	Pkg	Page
Low Power	OPA21Z	0.1	1	25	120	0.3	0.2	13.7	1.4	Ind	DIP	2-21
Switchable Input	OPA201G	0.1	1	25	120	0.5	0.1	13.5	5	Com	DIP	2-86
Very Fast Settling	**OPA675G**	**1**	**5**	**35µA**	**65**	**185[3]**	**350**	**2.1**	**30**	**Com, Mil**	**DIP**	**2-186**
	OPA676G	**1**	**5**	**35µA**	**65**	**185[3]**	**350**	**2.1**	**30**	**Com, Mil**	**DIP**	**2-186**
Wide Temp Range	OPA11HT	5	5[2]	±25	94	12	7	10	15	–55°C to +175°C	TO-99	2-17
	OPA27HT	0.05	0.25[2]	1µA	120	6	1.9	12	16[2]	–55°C to +200°C	TO-99	2-39

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C Mil = –55°C to +125°C. (2) Typical. (3) –3dB BW at Gain of +10V/V.

MODELS STILL AVAILABLE BUT NOT FEATURED IN THIS BOOK

Model	Description	Recommended Newer Model	Equivalency[1]
3329/03	Hybrid Power Booster	OPA633	F/E
3500	Low Bias Current Op Amp	OPA27	F/E
3501	Low Bias Current Op Amp	OPA111	P/P
3510	Low Drift Op Amp	OPA27	F/E
3521	Low Drift Op Amp	OPA111	P/P
3522	Low Drift Op Amp	OPA111	P/P
3523	Low Bias Current Op Amp	OPA128	P/P
3527	Low Drift FET Op Amp	OPA111	P/P
3528	Low Bias Current Op Amp	OPA128	P/P
3542	FET Input Op Amp	OPA121[2]	P/P
OPA37HT	Wide Temp Op Amp	OPA11HT	P/P
OPA103	Low Bias Current Op Amp	OPA128	P/P
OPA104	Low Bias Current Op Amp	OPA128	P/P
DEM102	Demo Kit for ISO102		
DEM106	Demo Kit for ISO106		

NOTES: (1) P/P = Pin for Pin. A true second source. F/E = Functional Equivalent. Very similar function, very similar performance, but not pin for pin. C/P = Closest Part. Similar function, similar performance, but significant differences exist. (2) Supply Range for OPA121 is ±5V to ±18V (instead of ±5V to ±20V).

OPERATIONAL AMPLIFIERS GLOSSARY

COMMON-MODE INPUT IMPEDANCE

Effective impedance (resistance in parallel with capacitance) between either input of an amplifier and its common, or ground terminal.

COMMON-MODE REJECTION (CMR)

When both inputs of a differential amplifier experience the same common-mode voltage (CMV), the output should, ideally, be unaffected. CMR is the ratio of the common-mode input voltage change to the differential input voltage (error voltage) which produces the same output change.

$$\text{CMR (in dB)} = 20 \log_{10} \text{CMV/Error Voltage}$$

Thus a CMR of 80dB means that 1V of common-mode voltage will cause an error of 100μV (referred to input).

COMMON-MODE VOLTAGE (CMV)

That portion of an input signal common to both inputs of a differential amplifier. Mathematically it is defined as the average of the signals at the two inputs:

$$\text{CMV} = (e_1 + e_2)/2$$

COMMON-MODE VOLTAGE GAIN

Ratio of the output signal voltage (ideally zero) to the common-mode input signal voltage.

COMMON-MODE VOLTAGE RANGE

Range of input voltage for linear, nonsaturated operation.

DIFFERENTIAL INPUT IMPEDANCE

Apparent impedance, resistance in parallel with capacitance, between the two input terminals.

FULL POWER FREQUENCY RESPONSE

Maximum frequency at which a device can supply its peak-to-peak rated output voltage and current, without introducing significant distortion.

GAIN-BANDWIDTH PRODUCT

Product of small signal, open-loop gain and frequency at that gain.

INPUT BIAS CURRENT

DC input current required at each input of an amplifier to provide zero output voltage when the input signal and input offset voltage are zero. The specified maximum is for each input.

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

Sensitivity of input bias current to power supply voltages.

INPUT BIAS CURRENT vs TEMPERATURE

Sensitivity of input bias current to temperature.

INPUT CURRENT NOISE

Input current that would produce, at the output of a noiseless amplifier, the same output as that produced by the inherent noise generated internally in the amplifier when the source resistances are large.

INPUT OFFSET CURRENT

Difference of the two input bias currents of a differential amplifier.

INPUT OFFSET VOLTAGE

DC input voltage required to provide zero voltage at the output of an amplifier when the input signal and input bias currents are zero.

INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE (PSR)

Sensitivity of input offset voltage to the power supply voltages. Both power supply voltages are changed in the same direction and magnitude over the operating voltage range.

INPUT OFFSET VOLTAGE vs TEMPERATURE (DRIFT)

Rate of change of input offset voltage with temperature. At Burr-Brown, this is the change in input offset voltage from +25°C to the maximum specification temperature, plus the change in input offset voltage from +25°C to the minimum specification temperature, this quantity is divided by the specified temperature range.

INPUT OFFSET VOLTAGE vs TIME

The sensitivity of input offset voltage to time.

INPUT VOLTAGE NOISE

Differential input voltage that would produce, at the output of a noiseless

amplifier, the same output as that produced by the inherent noise generated internally in the amplifier when the source resistances are small.

MAXIMUM SAFE INPUT VOLTAGE

Maximum voltage that may be applied at, or between, the inputs without damage.

OPEN-LOOP GAIN

Ratio of the output signal voltage to the differential input signal voltage.

OPERATING TEMPERATURE RANGE

Temperature range over which the amplifier may be safely operated.

OUTPUT RESISTANCE

Open-loop output source resistance with respect to ground.

POWER SUPPLY RATED VOLTAGE

Normal value of power supply voltage at which the amplifier is designed to operate.

POWER SUPPLY VOLTAGE RANGE

Range of power supply voltage over which the amplifier may be safely operated.

QUIESCENT CURRENT

Current required from the power supply to operate the amplifier with no load and with the output at zero volts.

RATED OUTPUT

Peak output voltage and current that can be continuously, simultaneously supplied.

SETTLING TIME

Time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

SLEW RATE

Maximum rate of change of the output voltage when supplying rated output current.

SPECIFICATION TEMPERATURE RANGE

Temperature range over which "versus temperature" specifications are specified.

STORAGE TEMPERATURE RANGE

Temperature range over which the amplifier may be safely stored, unpowered.

UNITY-GAIN FREQUENCY RESPONSE

Frequency at which the open-loop gain becomes unity.

BURR-BROWN®

AD515

FET-Input Electrometer OPERATIONAL AMPLIFIER

FEATURES

- ULTRA-LOW BIAS CURRENT: 0.075pA max
- LOW POWER: 1.5mA max
- LOW OFFSET: 1mV max
- LOW DRIFT: 15μV/°C max
- LOW COST
- REPLACES ANALOG DEVICES AD515

APPLICATIONS

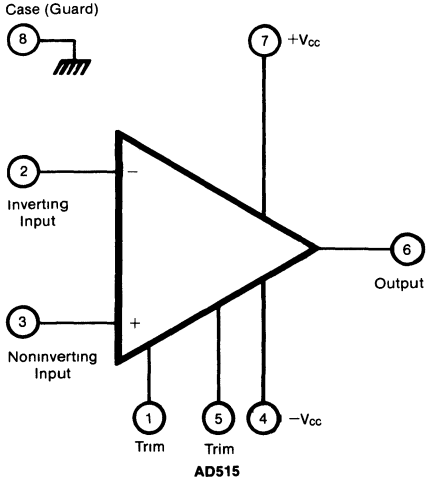
- pH SENSORS
- INTEGRATORS
- TEST EQUIPMENT
- ELECTRO-OPTICS
- CHARGE AMPLIFIERS
- GAS DETECTORS

DESCRIPTION

The Burr-Brown AD515 is a monolithic pin-for-pin replacement for the hybrid Analog Devices AD515 ultra-low bias current operational amplifier.

Laser-trimmed offset voltage and very-low bias current are important features of this popular amplifier. Monolithic construction allows lower cost and higher reliability than hybrid designs.

The AD515 is available in three electrical grades; all are specified over 0°C to +70°C and supplied in a TO-99 hermetic package.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-654A

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted Pin 8 connected to ground

PARAMETER	CONDITIONS	AD515J			AD515K			AD515L			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain[1]	$R_L \geq 2k\Omega$	20k			40k			25k			V/V
	$R_L \geq 10k\Omega$	40k			100k			50k			V/V
	T_{MIN} to T_{MAX}, R_L = 2k	15k			40k			25k			V/V
RATED OUTPUT											
Voltage Output $R_L = 2k\Omega$	T_{MIN} to T_{MAX}	±10	±12		*	*		*	*		V
$R_L = 10k\Omega$	T_{MIN} to T_{MAX}	±12	±13		*	*		*	*		V
Load Capacitance Stability	Gain = +1		1000			*			*		pF
Short Circuit Current		10	25	50	*	*	*	*	*	*	mA
FREQUENCY RESPONSE											
Unity Gain, Small Signal			350			*			*		kHz
Full Power Response	20V p-p, R_L = 2k	5	16		*	*		*	*		kHz
Slew Rate	V_O = ±10V, R_L = 2k, Gain = −1	0 3	1 0		*	*		*	*		V/μs
Overload Recovery	Gain = −1		16	100		*	*		*	*	μs
INPUT											
OFFSET VOLTAGE[2]											
Input Offset Voltage	V_{CM} = 0VDC		0 4	3 0		*	1 0		*	1 0	mV
Average Drift	T_{MIN} to T_{MAX}			50			15			25	μV/°C
Supply Rejection	T_{MIN} to T_{MAX}	68	86		80			74			dB
			50	400			100			200	μV/V
BIAS CURRENT[2]											
Input Bias Current Either Input	V_{CM} = 0VDC			300			150			75	fA
IMPEDANCE											
Differential			$10^{13} \parallel 1\,6$			*			*		Ω ‖ pF
Common-Mode			$10^{15} \parallel 0\,8$			*			*		Ω ‖ pF
VOLTAGE RANGE[3]											
Differential Input Range		±20			*			*			V
Common-Mode Input Range		±10	±11		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±10VDC	66	94		80			70			dB
NOISE											
Voltage 0 1Hz to 10Hz			4 0			*			*		μV p-p
f_O = 10Hz			75			*			*		nV/√Hz
f_O = 100Hz			55			*			*		nV/√Hz
f_O = 1kHz			50			*			*		nV/√Hz
Current 0 1Hz to 10Hz			0 003			*			*		pA p-p
f_O = 10Hz to 10kHz			0 01			*			*		pA rms
POWER SUPPLY											
Rated Voltage			±15			*			*		VDC
Voltage Range, Derated Performance		±5		±18	*		*	*		*	VDC
Current, Quiescent	I_O = 0mADC		0 8	1 5		*	*		*	*	mA
TEMPERATURE RANGE											
Specification Range	Ambient temp	0		+70	*		*	*		*	°C
Storage	Ambient temp	−65		+150	*		*	*		*	°C

* Specification same as AD515J

NOTES (1) With or without nulling of V_{OS} (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up (3) If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0 5mA The input devices can withstand overload currents of 0 3mA indefinitely without damage

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage[2]	±36VDC
Input Voltage Range[2]	±18VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[3]	Continuous
Junction Temperature	+175°C

NOTES (1) Packages must be derated based on θ_{JC} = 150°C/W or θ_{JA} = 200°C/W (2) For supply voltages less than ±18VDC the absolute maximum input voltage is equal to the supply voltage. (3) Short circuit may be to power supply common only Rating applies to +25°C ambient. Observe dissipation limit and T_J

ORDERING INFORMATION

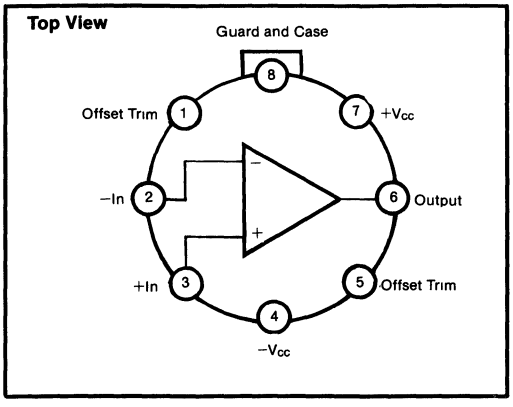
AD515 X H

Basic model number

Performance grade
J, K, L = 0°C to +70°C

Package code
H = TO-99 metal can

CONNECTION DIAGRAM

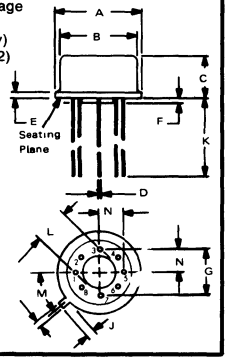


MECHANICAL

"H" PACKAGE TO-99 (Hermetic)

NOTE Leads in true position within .010" (.25mm) R at MMC at seating plane
Pin numbers shown for reference only
Numbers may not be marked on package
Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

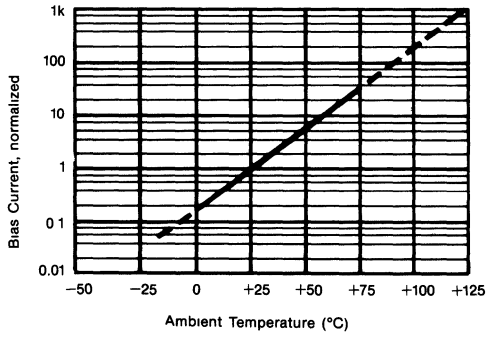
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	---	12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67



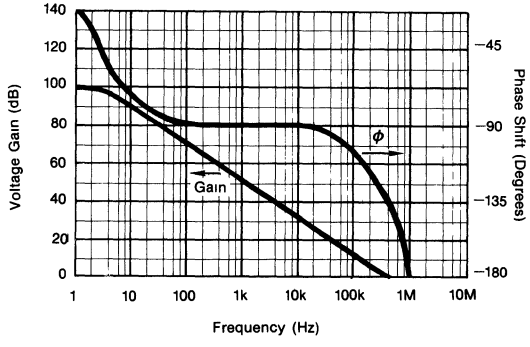
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted

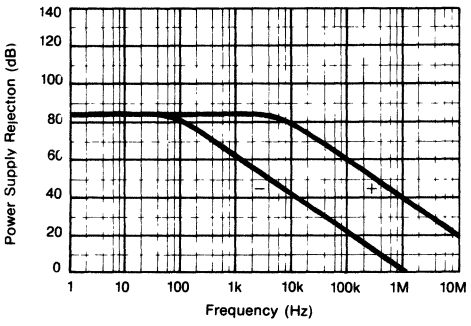
NORMALIZED BIAS CURRENT vs TEMPERATURE



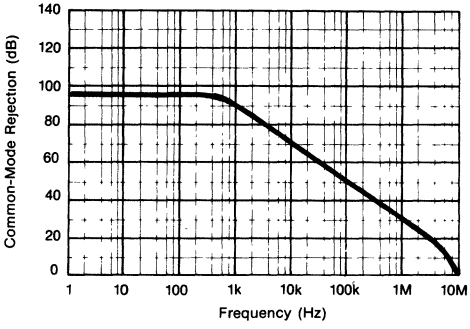
OPEN-LOOP FREQUENCY RESPONSE



POWER SUPPLY REJECTION vs FREQUENCY



COMMON-MODE REJECTION vs FREQUENCY



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

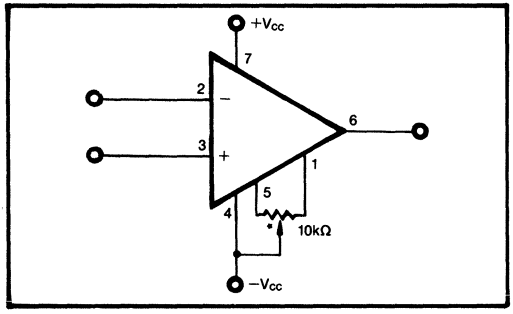


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

The AD515 requires input protection only if the source is not current limited. Limiting input current to 0.5mA with a series resistor is recommended when input voltage exceeds supply voltage.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the AD515. To avoid leakage problems, it is recommended that the signal input lead of the AD515 be wired to a Teflon standoff. If the lead is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout.

A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential. The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 2).

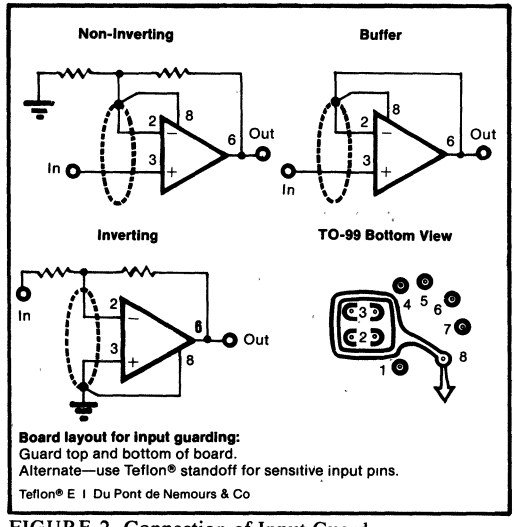


FIGURE 2. Connection of Input Guard.

BURR-BROWN®

OPA11HT

Wide Temperature-Range General Purpose OPERATIONAL AMPLIFIER

FEATURES

- −55°C TO +175°C SPECIFICATIONS
- 30nA MAX, INPUT BIAS CURRENT AT +175°C
- ±6mV, MAX, INPUT OFFSET VOLTAGE AT +175°C
- ±5μV/°C TYP, INPUT OFFSET VOLTAGE COEFFICIENT
- 12MHz BANDWIDTH, TYPICAL
- HERMETIC PACKAGE WITH STANDARD PINOUT (741-TYPE)

DESCRIPTION

These specifications give you a versatile operational amplifier that will work in circuits that are subjected to extremely wide temperature ranges. Typical applications for OPA11HT include general purpose gain blocks, high-speed pulse amplifiers, audio amplifiers, high-frequency active filters, high-speed integrators, and photodiode amplifiers.

You're assured of this product's performance over the -55°C to +175°C range because we conduct 100% screening procedures in accordance with MIL-STD-883, method 5004, class B. Burn-in is performed at 200°C. Our sample and inspection procedures include both destructive and nondestructive bonding wire pull tests in accordance with Method 2011 of MIL-STD-883. The product is assembled in a clean-room environment.

Model OPA11HT is internally compensated for stability at all gains. Pins are available for special tailoring of the bandwidth compensation. Significant advantages in high gain, wide bandwidth, low-bias current, high output current and high common-mode rejection are provided by OPA11HT. Inputs are protected against common-mode voltages up to the value of the power supplies while the output is current limited to offer short circuited protection. TO-99 hermetic package has standard 741-type pinout arrangement.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-476

SPECIFICATIONS

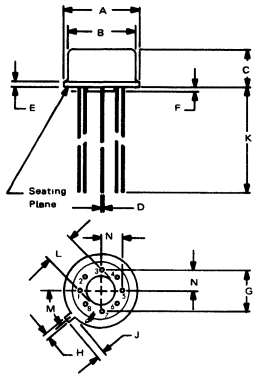
ELECTRICAL

Specifications at ±15VDC and T_A = +175°C unless otherwise noted

MODEL		OPA11HT			
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
OPEN LOOP GAIN, DC, single-ended	A_V				
No load			103		dB
R_L = 2kΩ		94	100		dB
RATED OUTPUT					
Voltage, R_L = 2kΩ	V_{om}	±10	±12		V
Current (T_A = 25°C)	I_{om}	±15	±23		mA
DYNAMIC RESPONSE (T_A = 25°C)					
Small-Signal Bandwidth (0dB)			12		MHz
Full-Power Bandwidth (V_{OUT} = ±10V)	BW_{fp}	50	75		kHz
Slew Rate (R_L = 2kΩ)	SR	4	7		V/µsec
Settling Time (0.1%)			1.5		µsec
Rise Time (10% to 90%, small-signal)			30		nsec
INPUT OFFSET VOLTAGE	V_{IO}				
Initial (without adj at 25°C)			±1	±5	mV
Over Temperature					
T_A = +175°C				±6	mV
T_A = −55°C				±7	mV
Average V_{IO} coefficient			±5		µV/°C
Average V_{IO} coefficient vs supply voltage (T_A = 25°C)			±10	±200	µV/V
INPUT BIAS CURRENT	I_{IB}				
Initial at +25°C			±10	±25	nA
Over Temperature					
T_A = +175°C				±30	nA
T_A = −55°C				±40	nA
Average I_{IB} coefficient			±0.1		nA/°C
INPUT DIFFERENCE CURRENT	I_{IO}				
Initial at +25°C			±10	±25	nA
Over Temperature					
T_A = +175°C				±30	nA
T_A = −55°C				±40	nA
Average I_{IO} coefficient			±0.1		nA/°C
INPUT IMPEDANCE (T_A = 25°C)					
Differential	r_i	100	300		MΩ
	c_i		3		pF
Common Mode	r_i(CM)		1000		MΩ
	c_i(CM)		3		pF
INPUT VOLTAGE RANGE					
Common Mode				±11	V
Differential Mode				±12	V
Common-Mode Rejection	CMR	80	100		dB
Over Temperature (−55°C ≤ T_A ≤ +175°C)			100		dB
POWER SUPPLY (T_A = 25°C)					
Rated Voltage	V_{CC}			±15	V
Voltage Range, derated			±8 to ±22		V
Current, quiescent	I_q		±3	±3.7	mA
Over Temperature (−55°C ≤ T_A ≤ +175°C)			±3		mA
Power Supply Rejection Ratio (T_A = +175°C)	PS_{rr}	80	100		dB
TEMPERATURE RANGE					
Specification		−55°C ≤ T_A ≤ +175°C			
Operating		−55°C ≤ T_A ≤ +200°C			
Storage		−65°C ≤ T_A ≤ +250°C			

MECHANICAL

TO-99 PACKAGE

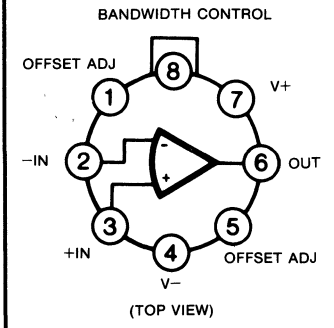


NOTE
Leads in true position within .010" (.25mm) R @ MMC at seating plane

Pin numbers shown for reference only
Numbers may not be marked on package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	335	370	8.51	9.40
B	305	335	7.75	8.51
C	165	185	4.19	4.70
D	016	021	0.41	0.53
E	010	040	0.25	1.02
F	010	040	0.25	1.02
G	200 BASIC		5.08 BASIC	
H	028	034	0.71	0.86
J	029	045	0.74	1.14
K	500	---	12.7	---
L	110	160	2.79	4.06
M	45° BASIC		45° BASIC	
N	095	105	2.41	2.67

CONNECTION DIAGRAM



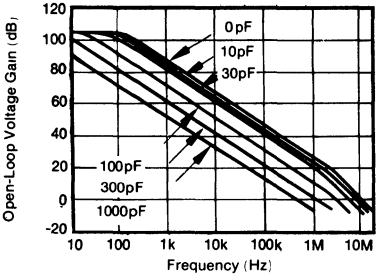
(TOP VIEW)

PIN 4 IS CONNECTED TO CASE

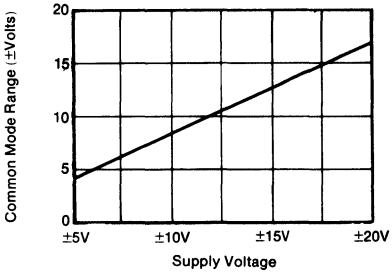
TYPICAL PERFORMANCE CURVES

(at ±15VDC and T_A = +25°C unless otherwise specified)

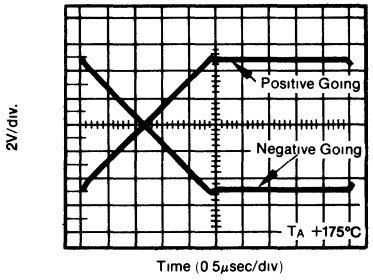
OPEN LOOP FREQUENCY RESPONSE[1]



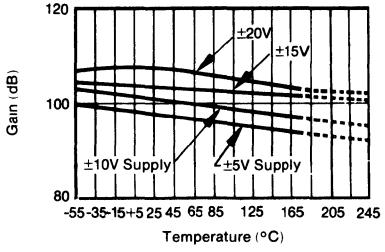
COMMON MODE VOLTAGE RANGE vs SUPPLY VOLTAGE



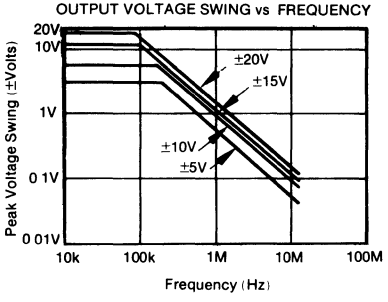
STEP RESPONSE IN FOLLOWER CONFIGURATION[2]



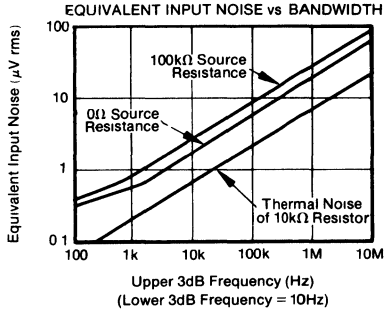
OPEN LOOP VOLTAGE GAIN vs TEMPERATURE



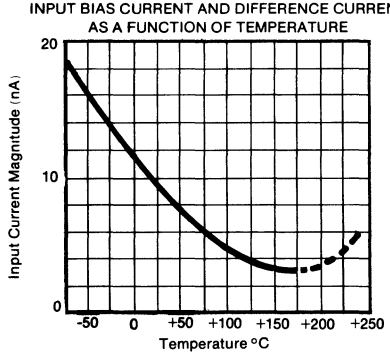
OUTPUT VOLTAGE SWING vs FREQUENCY



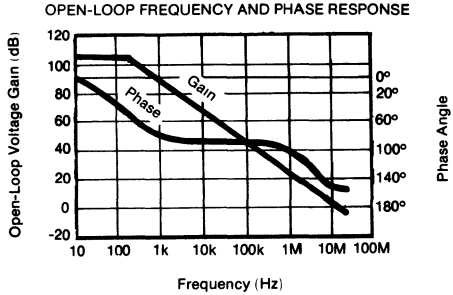
EQUIVALENT INPUT NOISE vs BANDWIDTH



INPUT BIAS CURRENT AND DIFFERENCE CURRENT AS A FUNCTION OF TEMPERATURE



OPEN-LOOP FREQUENCY AND PHASE RESPONSE



1. Capacitance values shown are compensation from pin 8 to common Not required for stability See Figure 1 2 See Figure 3.

APPLICATIONS

BANDWIDTH COMPENSATION

The frequency response of the OPA11HT can be adjusted by use of an external compensation capacitor from pin 8 to common as shown in Figure 1. The open-loop frequency response curves illustrate the effect of various values of capacitance. The OPA11HT is stable at any gain level without the use of compensation, provided that stray wiring capacitance and/or load capacitance are not excessive, and that moderate values of feedback resistance are used ($R_{FB} \leq 10k\Omega$). A load capacitance of ≈50pF is desirable in all feedback configurations.

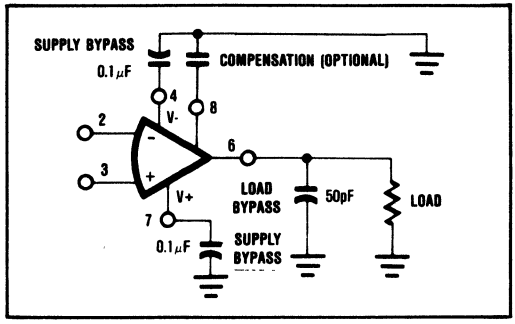


FIGURE 1. Compensated Amplifier with Supply Load Bypassing.

STABILITY

Because the OPA11HT is an extremely-fast amplifier with high gain, stray wiring capacitance and inductance in power supply leads can cause circuit oscillation. This can be prevented by proper circuit layout (all leads or patterns as short as possible) and by properly by passing the power supply lines to common at points close to the amplifier. In addition, it is recommended that the load be bypassed by a 50pF capacitor, see Figure 1.

OFFSET VOLTAGE AND ADJUSTMENT

Although the offset voltage of these amplifiers is only a few millivolts, it may in some cases be desirable to null this offset. This is done by use of a 100kΩ potentiometer as shown in Figure 2.

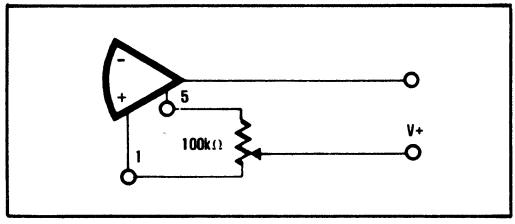


FIGURE 2. External Adjustment of Offset Voltage.

TEST CIRCUIT - DYNAMIC RESPONSE

The test circuit of Figure 3 is used for measurement of slew rate, settling time, rise time and overshoot. Both rise time and overshoot are measured for a small output signal ($V_{OUT} = \pm 100mV$). Slew rate and settling time are measured for a 10V, p-p, square wave.

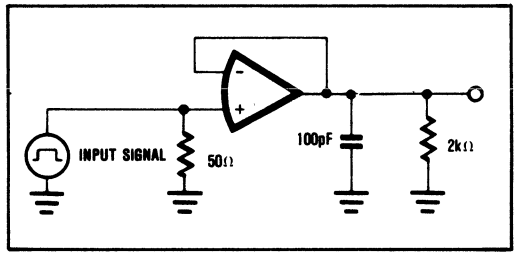


FIGURE 3. Dynamic Response Test Circuit.

VOLTAGE REGULATOR AT 200°C

In many applications, a regulated source of ±15V is needed. A voltage regulator that typically will operate up to +175°C is shown in Figure 4. This regulator accepts +16V to +30V at its input and provides +15V at 20mA at its output. A complementary version may be constructed to provide -15V by using the OPA11HT with a 2N1711 transistor. Short-circuit protection should be added if required.

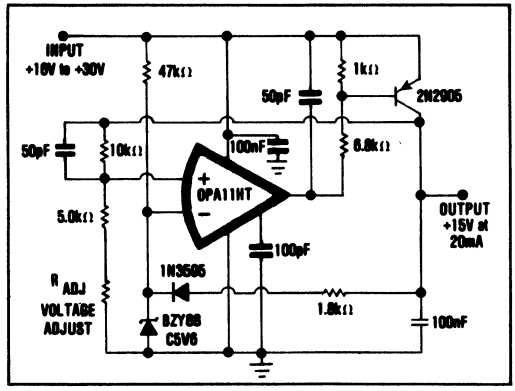
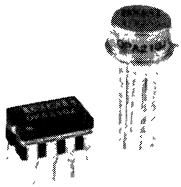


FIGURE 4. A +15V Voltage Regulator that will Operate at +175°C.

BURR-BROWN®



OPA21

AVAILABLE IN DIE FORM

Low-Power Precision OPERATIONAL AMPLIFIER

FEATURES

- LOW SUPPLY CURRENT
  230μA max at $V_{CC} = \pm 15V$
- WIDE SUPPLY RANGE
  ±2.5V to ±18V
- LOW OFFSET VOLTAGE
  100μV max
- LOW OFFSET VOLTAGE DRIFT
  1.0μV/°C max

APPLICATIONS

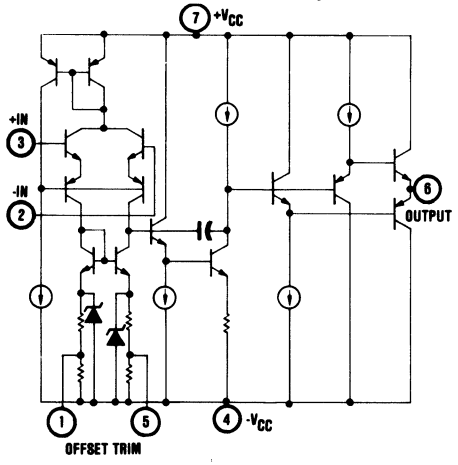
- PORTABLE EQUIPMENT
- BATTERY OPERATION
- IMPROVED REPLACEMENT FOR OP-21

DESCRIPTION

A unique circuit design, state-of-the-art monolithic processing and advanced laser-trimming techniques are used to provide a low power amplifier with outstanding parameters—truly "instrumentation grade" performance over a wide voltage supply range.

The OPA21 consumes only 6.9mW of power at $V_{CC} = \pm 15V$ and 1.1mW at $V_{CC} = \pm 2.5V$ but offers far higher performance than MOS op-amps.

The OPA21 is internally compensated for unity-gain stability.



SIMPLIFIED CIRCUIT

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-482C

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 2.5VDC to 15VDC, unless otherwise noted.

PARAMETERS	CONDITIONS	OPA21E			OPA21G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT OFFSET VOLTAGE								
OFFSET VOLTAGE[1]			40	100		300	500	µV
	−25°C to +85°C		75	200		500	1000	µV
Drift	−25°C to +85°C		0.5	1.0		2 5	5.0	µV/°C
Offset Adjustment Range			±4			*		mV
INPUT OFFSET CURRENT								
Offset Current			0 3	1		1 2	4	nA
	−25°C to +85°C		0 5	2		2	6	nA
INPUT BIAS CURRENT								
Bias Current			7	25		15	50	nA
	−25°C to +85°C		9	40		18	75	nA
INPUT NOISE								
Voltage	0 1Hz to 10Hz		1 0			*		µV p-p
Voltage Density	f_O = 1Hz		60			*		nV/√Hz
	f_O = 10Hz		20			*		nV/√Hz
	f_O = 100Hz		20			*		nV/√Hz
Current Density	f_O = 1Hz		0 7			*		pA/√Hz
	f_O = 10Hz		0 25			*		pA/√Hz
	f_O = 100Hz		0 07			*		pA/√Hz
INPUT RESISTANCE								
Differential			6			4		MΩ
Common-Mode			10^{10}||2			*		Ω||pF
INPUT VOLTAGE RANGE								
Input Voltage Range		−12 5			*			V
		+14 3			*			V
	−25°C to +85°C	−12 0			*			V
		+14.0			*			V
COMMON-MODE REJECTION RATIO								
CMRR	V_{CM} = −12V to +14V, R_L = 100kΩ	100	110		84	100		dB
	−25°C to +85°C	96	105		80	95		dB
POWER SUPPLY REJECTION RATIO								
PSRR	$\pm V_{CC}$ = 2 5V to 18V, R_L = 100kΩ	104	114		90	100		dB
	−25°C to +85°C	100	108		85	95		dB
LARGE SIGNAL VOLTAGE GAIN								
Open-Loop Voltage Gain	R_L = 10kΩ	1000	2000		500	1000		V/mV
		120	126		114	120		dB
	−25°C to +85°C	500	1500		250	1000		V/mV
		114	124		108	120		dB
RATED OUTPUT								
Output Voltage Swing	R_L = 10kΩ	−13 7	−14 2		−13 6	*		V
		+14 0	+14 1		+13 8	*		V
Output Current	R_L = 2kΩ		5			*		mA
	−25°C to +85°C, R_L = 10kΩ	−13 5			*			V
		+13 8			+13 6			V
Output Resistance	Open-Loop		500			*		Ω
DYNAMIC RESPONSE								
Slew Rate	C_L = 100pF, R_L = 25kΩ		0 2			*		V/µsec
Closed-Loop Bandwidth	A_{CL} = +1, R_L = 10kΩ		300			*		kHz
POWER SUPPLY								
Rated Voltage			±15			*		VDC
Voltage Range	Derated	±2 5		±18	*		*	VDC
Current Quiescent	I_O = 0MA							
	$\pm V_{CC}$ = 2 5V		170	210		*	250	µA
	$\pm V_{CC}$ = 15V		200	230		*	325	µA
	$\pm V_{CC}$ = 2 5V, −25°C to +85°C		210	275		*	325	µA
	$\pm V_{CC}$ = 15V, −25°C to +85°C		230	325		*	375	µA
TEMPERATURE RANGE								
Specification	Ambient	−25		+85	*		*	°C
Operating	Ambient	−55		+125	*		*	°C

NOTE (1) Guaranteed fully warmed-up

*Specification same as OPA21E

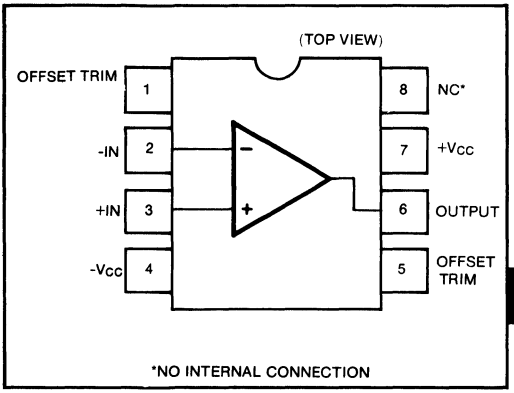
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation[1]	500mW
Input Voltage	Supply Voltage
Differential Input Voltage	±30V
Output Short Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature Range (soldering, 60sec)	+300°C

NOTE (1) Maximum package power dissipation vs ambient temperature

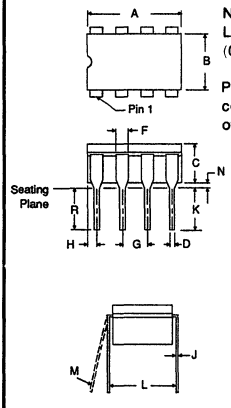
Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
8-Pin Hermetic DIP (Z)	+75°C	6.7mW/°C

PIN CONFIGURATION



MECHANICAL

8-PIN HERMETIC DIP
("Z" SUFFIX)



NOTE
Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.375	.405	9.53	10.28
B	.245	.261	6.22	6.36
C	.140	.170	3.56	4.32
D	.016	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	-	.050	-	2.49
J	.008	.012	0.20	0.30
K	.150	-	3.80	-
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.126	.176	3.18	4.46

ORDERING INFORMATION

OPA21 E Z

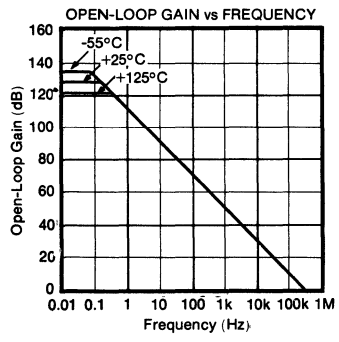
Basic Model Number

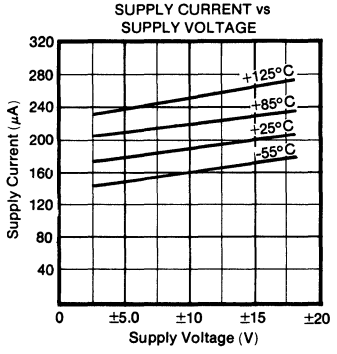
Performance Grade Code
E, G = −25°C to +85°C

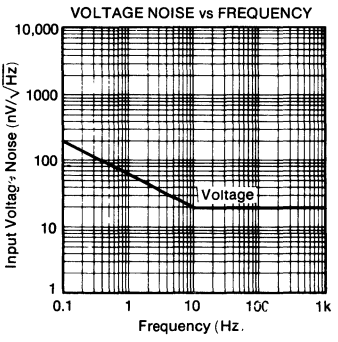
Package Code
Z = 8-Pin Hermetic DIP

TYPICAL PERFORMANCE CURVES

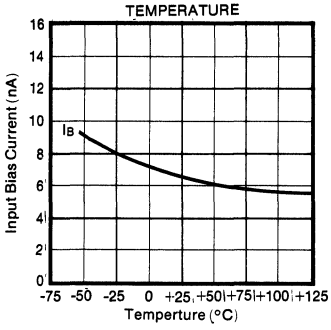
(T_A = +25°C, ±V_{CC} = 15VDC unless otherwise noted)



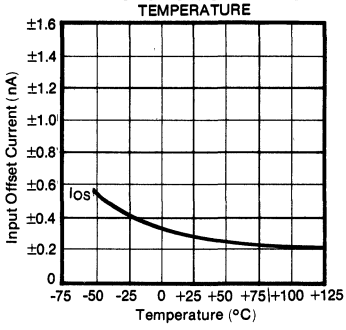




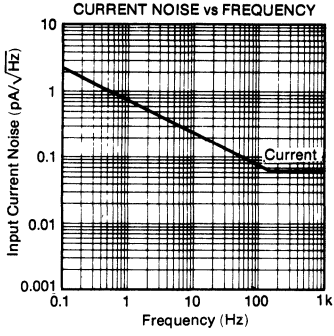
INPUT BIAS CURRENT vs TEMPERATURE



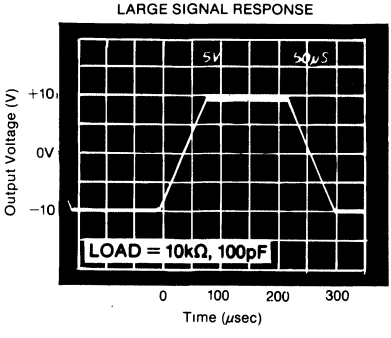
INPUT OFFSET CURRENT vs TEMPERATURE



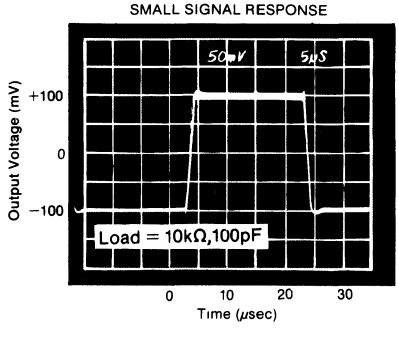
CURRENT NOISE vs FREQUENCY



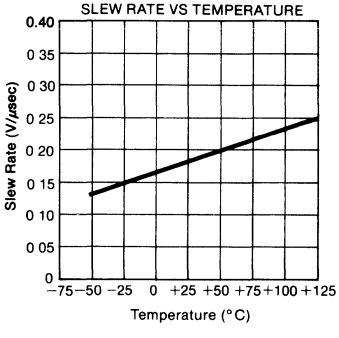
LARGE SIGNAL RESPONSE



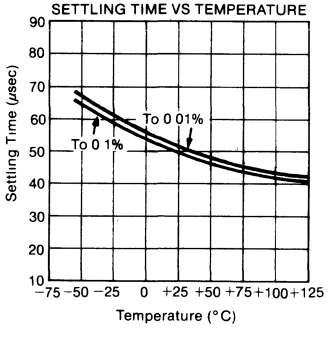
SMALL SIGNAL RESPONSE



SLEW RATE VS TEMPERATURE



SETTLING TIME VS TEMPERATURE



APPLICATIONS

Figures 1 through 6 are typical applications of the OPA21.

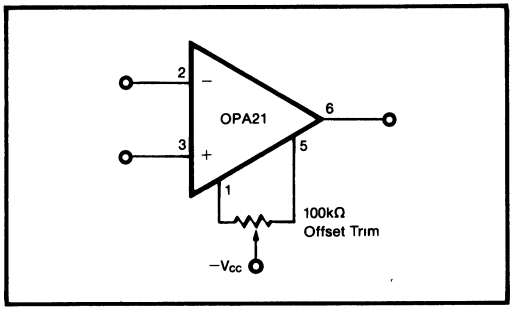


FIGURE 1. Voltage Offset Trim.

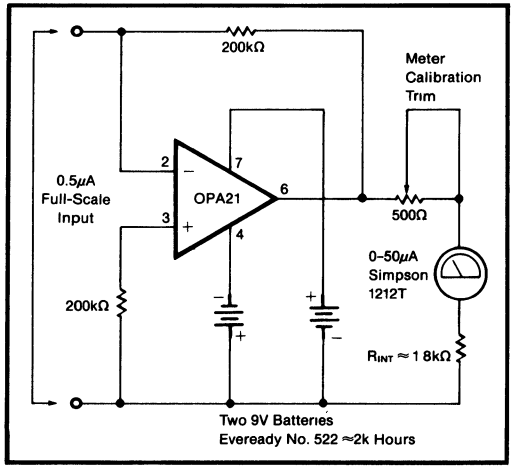


FIGURE 2. Fully-Floating Current Meter.

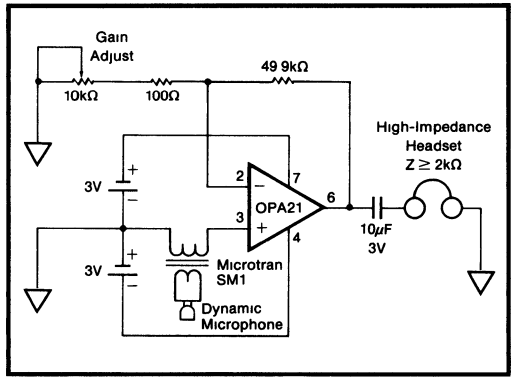


FIGURE 3. Portable Microphone Amplifier.

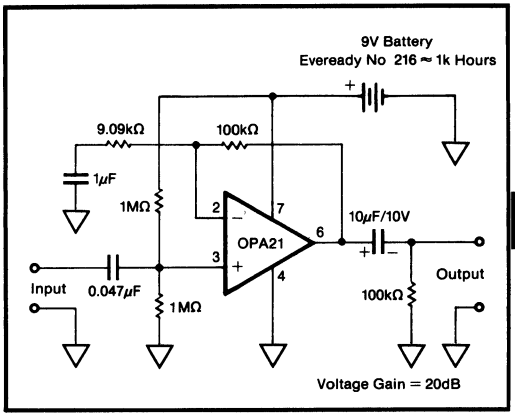


FIGURE 4. AC Amplifier.

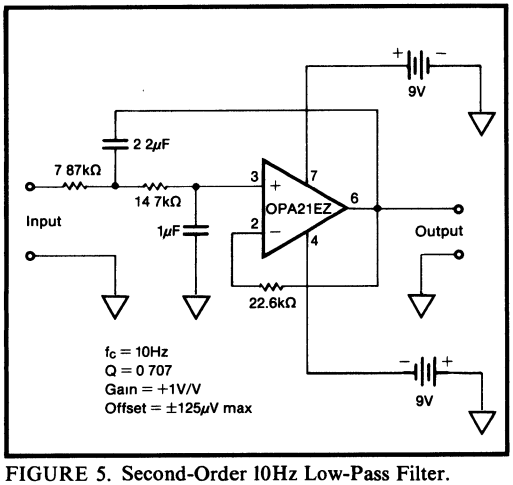


FIGURE 5. Second-Order 10Hz Low-Pass Filter.

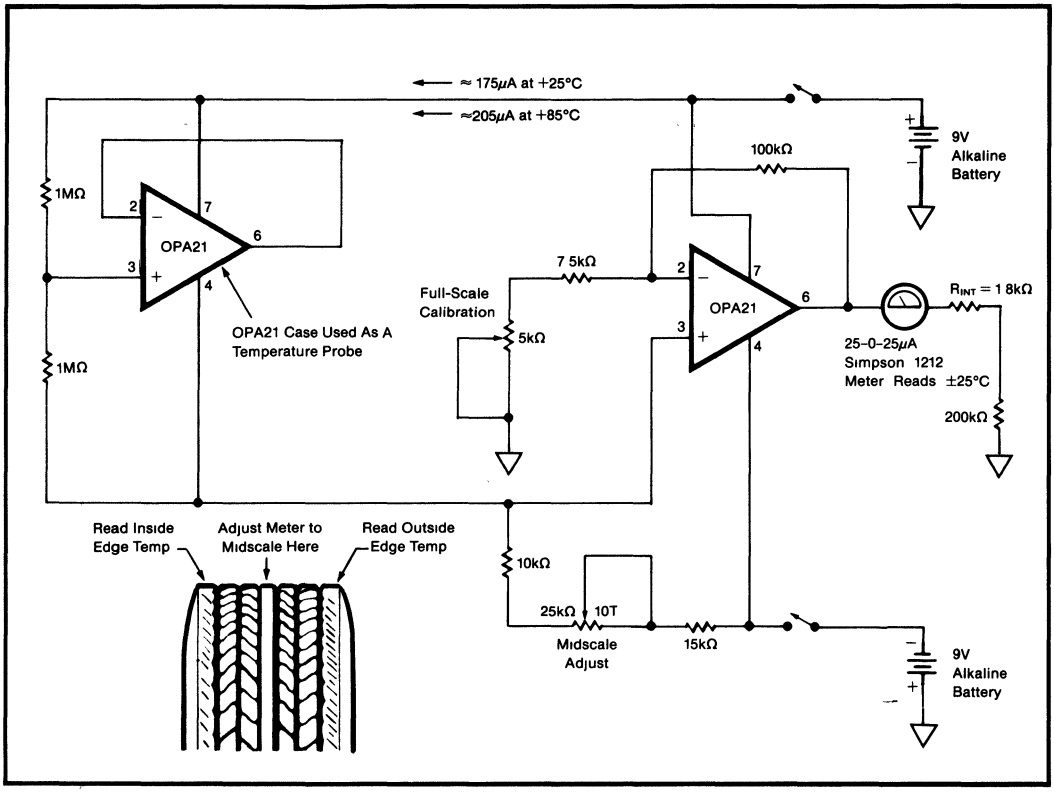
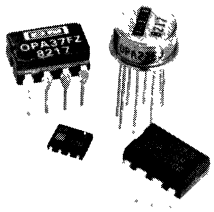


FIGURE 6. Portable Tire Pyrometer.

BURR-BROWN®



OPA27
OPA37

MILITARY & DIE VERSIONS AVAILABLE

Ultra-Low Noise Precision OPERATIONAL AMPLIFIERS

FEATURES

- LOW NOISE: 100% tested, 3.8nV/$\sqrt{Hz}$ max at 1kHz
- LOW OFFSET: 25μV max
- LOW DRIFT: 0.6μV/°C max
- HIGH OPEN-LOOP GAIN: 120dB min
- HIGH COMMON-MODE REJECTION: 114dB min
- HIGH POWER SUPPLY REJECTION: 100dB min
- FITS OP-07, OP-05, AD510, AD517 SOCKETS

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- TRANSDUCER AMPLIFIER
- RADIATION HARD EQUIPMENT

DESCRIPTION

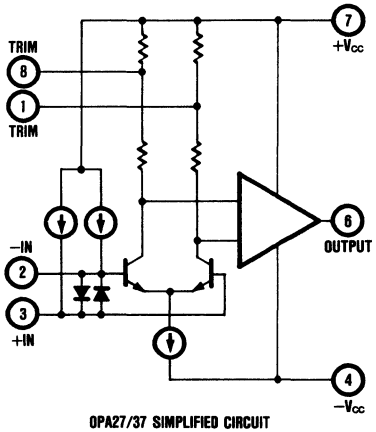
The OPA27/37 is an ultra-low noise, high precision monolithic operational amplifier.

Laser-trimmed thin-film resistors provide excellent long-term voltage offset stability and allow superior voltage offset compared to common zener-zap techniques.

A unique bias current cancellation circuit allows bias and offset current specifications to be met over the full −55°C to +125°C temperature range.

The OPA27 is internally compensated for unity-gain stability. The decompensated OPA37 requires a closed-loop gain ≥ 5.

The Burr-Brown OPA27/37 is an improved replacement for the industry-standard OP-27/OP-37.



OPA27/37 SIMPLIFIED CIRCUIT

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-466H

SPECIFICATIONS

ELECTRICAL

At V_{CC} = P15VDC and T_A = +25°C unless otherwise noted

PARAMETER	CONDITIONS	OPA27/37A, OPA27/37E			OPA27/37B, OPA27/37F			OPA27/37C, OPA27/37G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
NOISE											
Voltage, f_O = 10Hz	100% tested, (A, E)		3.1	5 5		3.5	5 5		3.8	8 0[6]	nV/√Hz
f_O = 30Hz	100% tested, (A, E)		2.9	4.5		3 1	4.5		3 3	5 6[6]	nV/√Hz
f_O = 1kHz	100% tested, (A, E)		2 7	3.8		3.0	3 8		3 2	4 5[6]	nV/√Hz
f_B = 0 1Hz to 10Hz			0 07	0 18		0.08	0.18		0.09	0 25[6]	μV, p-p
Current,[1] f_O = 10Hz	100% tested, (A, E)		1 7	4.0		1.7	4 0		1.7		pA/√Hz
f_O = 30Hz	100% tested, (A, E)		1.0	2.3		1.0	2 3		1 0		pA/√Hz
f_O = 1kHz	100% tested, (A, E)		0 4	0.6		0.4	0.6		0.4	0 6[6]	pA/√Hz
OFFSET VOLTAGE[2]											
Input Offset Voltage			±6	±25		±12	±60		±25	±100	μV
Average Drift[3]	$T_{A\ MIN}$ to $T_{A\ MAX}$		±0.2	±0 6		±0.3	±1 3		±0 4	±1 8[6]	μV/°C
Long Term Stability[4]			0.2	1		0.3	1 5		0 4	2 0	μV/mo
Supply Rejection	±V_{CC} = 4 to 18V	100	134		100	125		94	120		dB
	±V_{CC} = 4 to 18V		±0.2	±10		±0.6	±10		±1	±20	μV/V
BIAS CURRENT											
Input Bias Current			±11	±40		±13	±55		±15	±80	nA
OFFSET CURRENT											
Input Offset Current			6	35		8	50		10	75	nA
IMPEDANCE											
Common-Mode			3			2 5			2		GΩ
VOLTAGE RANGE											
Common-Mode Input Range		±11	±12.3		±11	±12.3		±11	±12 3		V
Common-Mode Rejection	V_{IN} = ±11VDC	114	128		106	125		100	122		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	120	126		120	125		117	124		dB
	$R_L \geq 1k\Omega$	118	125		118	125			124		dB
FREQUENCY RESPONSE											
Gain-Bandwidth Product[5]	OPA27	5	8		5	8		5[6]	8		MHz
	OPA37	45	63		45	63		45[6]	63		MHz
Slew Rate[5]	V_O = ±10V, R_L = 2kΩ										
	OPA27, G = +1	1 7	1 9		1 7	1 9		1 7[6]	1 9		V/μs
	OPA37, G = +5	11	11 9		11	11 9		11[6]	11.9		V/μs
Settling Time, 0 01%	OPA27, G = +1		25			25			25		μs
	OPA37, G = +5		25			25			25		μs
RATED OUTPUT											
Voltage Output	$R_L \geq 2k\Omega$	±12	±13 8		±12	±13.8		±12	±13 8		V
	$R_L \geq 600\Omega$	±10	±12 8		±10	±12.8		±10	±12 8		V
Output Resistance	DC, open loop		70			70			70		Ω
Short Circuit Current	R_L = 0Ω		25	60		25	60		25	60[6]	mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated Performance		±4		±22	±4		±22	±4		±22	VDC
Current, Quiescent	I_O = 0mADC		3	4 7		3	4 7		3.3	5 7	mA
TEMPERATURE RANGE											
Specification											
A, B, C (J, Z)		−55		+125	−55		+125	−55		+125	°C
E, F, G (J, Z)		−25		+85	−25		+85	−25		+85	°C
G (P) (U)								0		+70	°C
Operating J, Z		−55		+125	−55		+125	−55		+125	°C
P, U								−25		+85	°C

NOTES: (1) Measured with industry-standard noise test circuit (Figures 1 and 2). Due to errors introduced by this method, these current noise specifications should be used for comparison purposes only (2) Offset voltage specifications on grades A and E are also guaranteed with units fully warmed up. Grades B, C, F, and G are measured with automatic test equipment after approximately 0 5 second from power turn-on. (3) Unnulled or nulled with 8kΩ to 20kΩ potentiometer (4) Long-term voltage offset vs time trend line does not include warm-up drift (5) Typical specification only on plastic package units Slew rate varies on all units due to differing test methods Minimum specification applies to open-loop test (6) This parameter not guaranteed in SOIC "U" package.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA27/37A, OPA27/37E			OPA27/37B, OPA27/37F			OPA27/37C, OPA27/37G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification Range											
A, B, C (J, Z)		−55		+125	−55		+125	−55		+125	°C
E, F, G (J, Z)		−25		+85	−25		+85	−25		+85	°C
G (P)								0		+70	°C
INPUT											
OFFSET VOLTAGE[1]											
Input Offset Voltage											
A, B, C			±24	±60		±45	±200		±60	±300[3]	µV
E, F, G			±17	±50		±33	±140		±48	±220[3]	µV
Average Drift[2]	$T_{A\ MIN}$ to $T_{A\ MAX}$		±0.2	±0.6		±0.3	±1 3		±0.4	±1 8[3]	µV/°C
Supply Rejection											
A, B, C	$\pm V_{CC}$ = 4.5 to 18V	96	130		94	127		86[3]	122		dB
E, F, G	$\pm V_{CC}$ = 4.5 to 18V	97	130		96	127		90[3]	122		dB
BIAS CURRENT											
Input Bias Current											
A, B, C			±16	±60		±22	±95		±29	±150[3]	nA
E, F, G			±13	±60		±16	±95		±21	±150[3]	nA
OFFSET CURRENT											
Input Offset Current											
A, B, C			23	50		25	85		35	135[3]	nA
E, F, G			12	50		14	85		20	135[3]	nA
VOLTAGE RANGE											
Common-Mode Input Range											
A, B, C		±10.3	±11 5		±10 3	±11.5		±10 3[3]	±11.5		V
E, F, G		±10.5	±11.8		±10 5	±11 8		±10 5[3]	±11.8		V
Common-Mode Rejection	V_{IN} = ±11VDC										
A, B, C		108	124		100	122		94[3]	120		dB
E, F, G		110	126		102	124		96[3]	122		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$										
A, B, C		116	121		114	120		110[3]	118		dB
E, F, G		118	123		117	122		113	120		dB
RATED OUTPUT											
Voltage Output	$R_L = 2k\Omega$										
A, B, C		±11.5	±13.7		±11 0	±13 5		±10 5[3]	±13.3		V
E, F, G		±11.7	±13.8		±11 4	±13 6		±11 0[3]	±13.4		V
Short Circuit Current	V_O = 0VDC		25			25			25		mA

NOTES: (1) Offset voltage specifications on grades A and E are also guaranteed with the units fully warmed up. Grades B, C, F, and G are measured with automatic equipment after approximately 0.5 second (2) Unnulled or nulled with 8kΩ to 20kΩ potentiometer (3) This parameter not guaranteed in SOIC "U" package

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Internal Power Dissipation[1] 500mW
Input Voltage ..... $\pm V_{CC}$
Output Short-Circuit Duration[2] ..... Indefinite
Differential Input Voltage[3] ..... ±0.7V
Differential Input Current[3] ..... ±25mA
Storage Temperature Range:
J, Z ..... −65°C to +150°C
P ..... −55°C to +125°C
Operating Temperature Range:
A, B, C, E, F, G (J, Z) ..... −55°C to +125°C
G (P, U) ..... −25°C to +85°C
Lead Temperature (Soldering, 60s) ..... +300°C
SOIC Package (3s) ..... +260°C

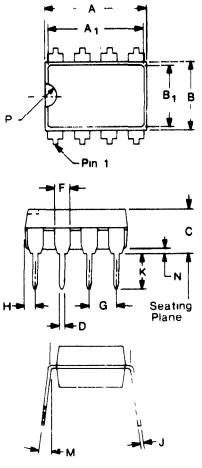
NOTES:
(1) Maximum package power dissipation vs ambient temperature

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7 1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6 7mW/°C
8-Pin Plastic DIP (P)	62°C	5 6mW/°C
8-Pin SOIC (U)	85°C	—

(2) To common with $\pm V_{CC}$ = 15V
(3) The inputs are protected by back-to-back diodes Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0 7V, the input current should be limited to 25mA

MECHANICAL

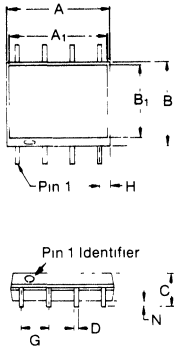
"P" PACKAGE, 8-PIN PLASTIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	355	400	9 03	10 16
A_1	340	385	8 65	9 80
B	230	290	5 85	7 38
B_1	200	250	5 09	6 36
C	120	200	3 05	5 09
D	015	023	0 38	0 59
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	025	050	0 64	1 27
J	008	015	0 20	0 38
K	070	150	1 78	3 82
L	300 BASIC		7 63 BASIC	
M	0°	15°	0°	15°
N	010	030	0 25	0 76
P	025	050	0 64	1 27

NOTE
Leads in true position within 0 01" (0 25mm) R at MMC at seating plane

"U" PACKAGE, 8-PIN SOIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	185	201	4 70	5 11
A_1	178	201	4 52	5 11
B	146	162	3 71	4 11
B_1	130	149	3 30	3 78
C	054	145	1 37	3 69
D	015	019	0 38	0 48
G	050 BASIC		1 27 BASIC	
H	018	026	0 46	0 66
J	008	012	0 20	0 30
L	220	252	5 59	6 40
M	0°	10°	0°	10°
N	000	012	0 00	0 30

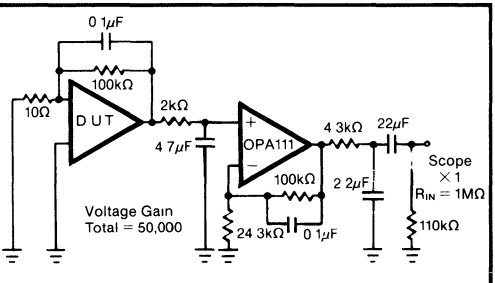


FIGURE 1 0 1Hz to 10Hz Noise Test Circuit

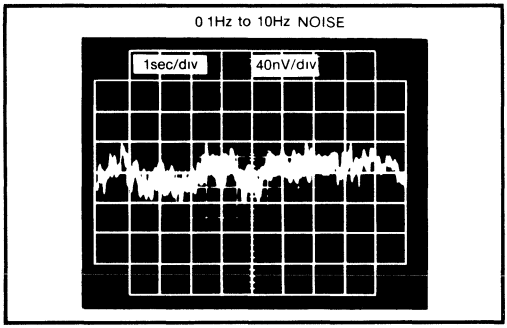


FIGURE 2 Low Frequency Noise

ORDERING INFORMATION

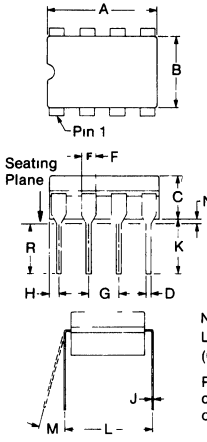
Model[1]	Package	Temperature Range	Offset Voltage max (μV), 25°C
OPA27AJ	TO-99	–55°C to +125°C	±25
OPA27BJ	TO-99	–55°C to +125°C	±60
OPA27CJ	TO-99	–55°C to +125°C	±100
OPA27EJ	TO-99	–25°C to +85°C	±25
OPA27FJ	TO-99	–25°C to +85°C	±60
OPA27GJ	TO-99	–25°C to +85°C	±100
OPA27AZ	Ceramic	–55°C to +125°C	±25
OPA27BZ	Ceramic	–55°C to +125°C	±60
OPA27CZ	Ceramic	–55°C to +125°C	±100
OPA27EZ	Ceramic	–25°C to +85°C	±25
OPA27FZ	Ceramic	–25°C to +85°C	±60
OPA27GZ	Ceramic	–25°C to +85°C	±100
OPA27GP	Plastic	0°C to +70°C	±100
OPA27GU	SOIC	0°C to +70°C	±100

BURN-IN SCREENING OPTION

Model[1]	Package	Temperature Range	Burn-In Temp. (160h)[2]
OPA27AJ-BI	TO-99	–55°C to +125°C	+125°C
OPA27EJ-BI	TO-99	–25°C to +85°C	+125°C
OPA27GJ-BI	TO-99	–25°C to +85°C	+125°C
OPA27AZ-BI	Ceramic	–55°C to +125°C	+125°C
OPA27EZ-BI	Ceramic	–25°C to +85°C	+125°C
OPA27GP-BI	Plastic	0°C to +70°C	+85°C
OPA27GU-BI	SOIC	0°C to +70°C	+85°C

NOTE (1) Packages and prices for OPA37 are the same as for OPA27
(2) Or equivalent combination of time and temperature

"Z" PACKAGE, 8-PIN HERMETIC

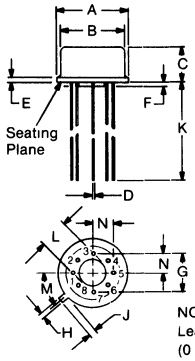


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	375	405	9 53	10 28
B	245	251	6 22	6 38
C	140	170	3 56	4 32
D	015	021	0 38	0 53
F	045	060	1 14	1 52
G	100 BASIC		2 54 BASIC	
H	—	098	—	2 49
J	008	012	0 20	0 30
K	150	—	3 80	—
L	290	320	7 37	8 13
M	0°	15°	0°	15°
N	009	060	0 23	1 52
R	125	175	3 18	4 45

NOTE
Leads in true position within 0 01" (0 25mm) R at MMC at seating plane

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragrah 3 2)

"J" PACKAGE, TO-99



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	335	370	8 51	9 40
B	305	335	7 75	8 51
C	165	185	4 19	4 70
D	016	021	0 41	0 53
E	010	040	0 25	1 02
F	010	040	0 25	1 02
G	200 BASIC		5 08 BASIC	
H	028	034	0 71	0 86
J	029	045	0 74	1 14
K	500	—	12 7	—
L	110	160	2 79	4 06
M	45° BASIC		45° BASIC	
N	095	105	2 41	2 67

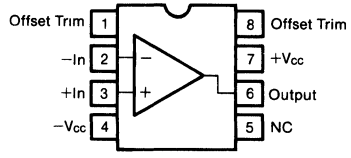
NOTE
Leads in true position within 0 01" (0 25mm) R at MMC at seating plane

Pin numbers shown for reference only
Numbers may not be marked on packag

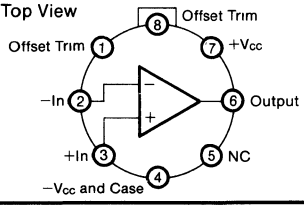
Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragrah 3 2)

CONNECTION DIAGRAMS

P, U, Z Packages—Top View



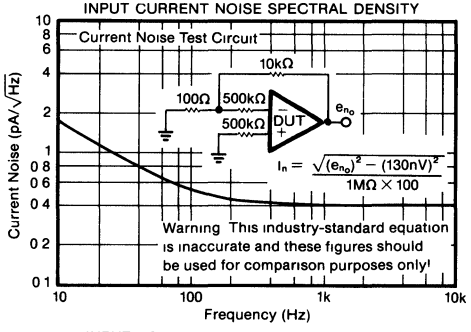
J Package—Top View



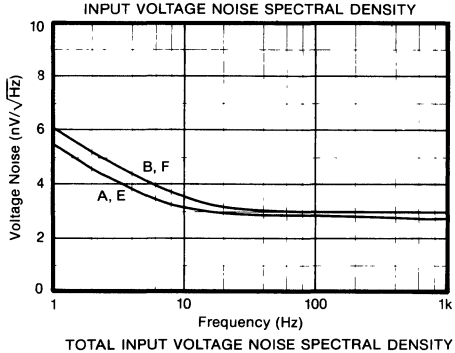
TYPICAL PERFORMANCE CURVES

T_A = +25°C, ±V_{CC} = ±15VDC unless otherwise noted

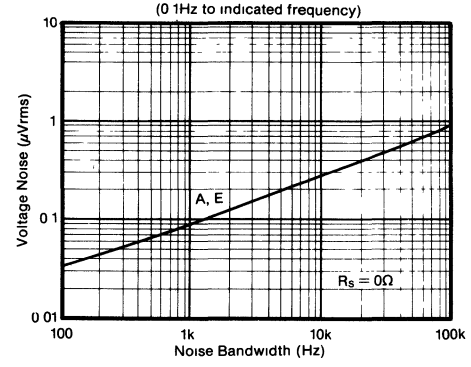
INPUT CURRENT NOISE SPECTRAL DENSITY



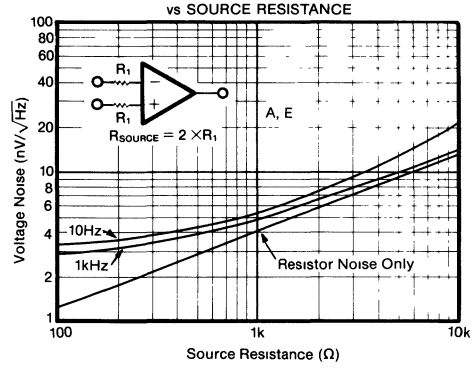
INPUT VOLTAGE NOISE SPECTRAL DENSITY



INPUT VOLTAGE NOISE vs NOISE BANDWIDTH
(0 1Hz to indicated frequency)



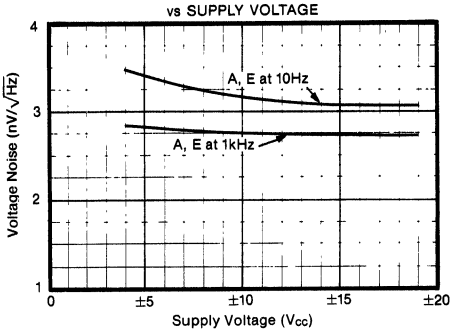
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY
vs SOURCE RESISTANCE



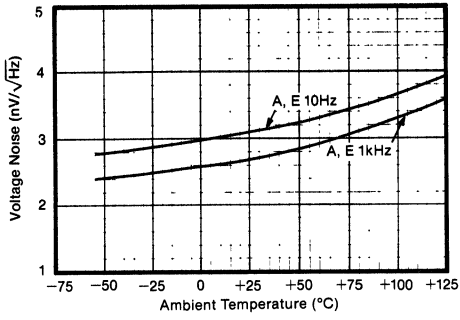
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, $\pm V_{CC}$ = ±15VDC unless otherwise noted.

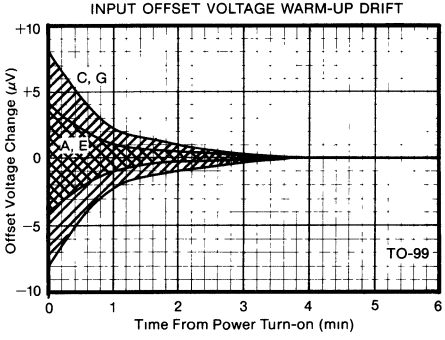
VOLTAGE NOISE SPECTRAL DENSITY vs SUPPLY VOLTAGE



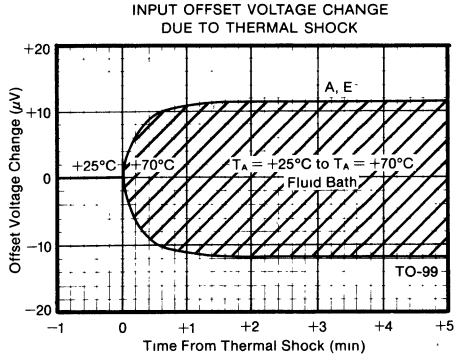
VOLTAGE NOISE SPECTRAL DENSITY vs TEMPERATURE



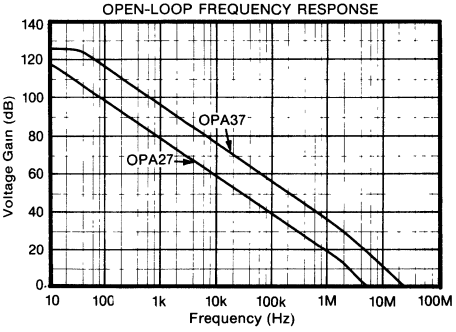
INPUT OFFSET VOLTAGE WARM-UP DRIFT



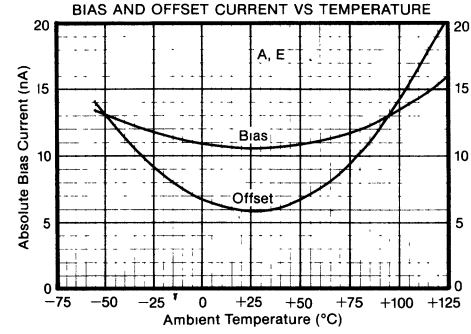
INPUT OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



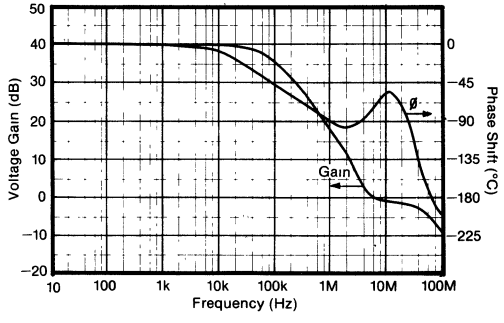
OPEN-LOOP FREQUENCY RESPONSE



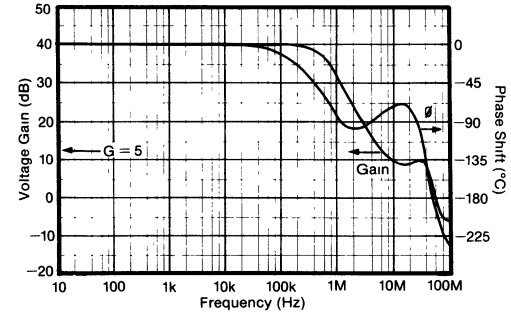
BIAS AND OFFSET CURRENT VS TEMPERATURE



OPA27 CLOSED-LOOP VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY (G = 100)



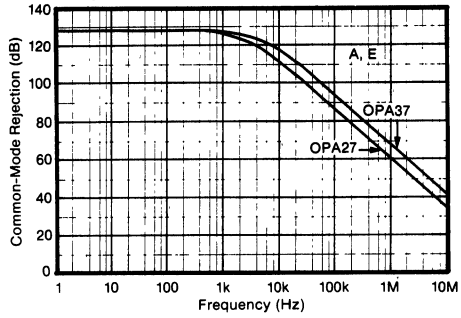
OPA37 CLOSED-LOOP VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY (G = 100)



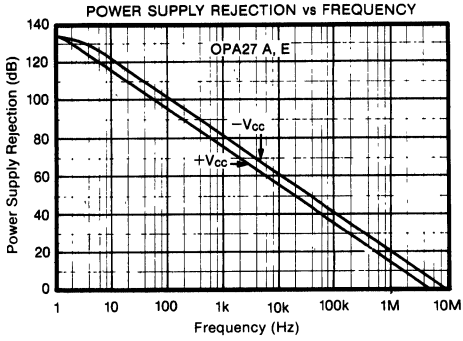
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, $\pm V_{CC}$ = ±15VDC unless otherwise noted.

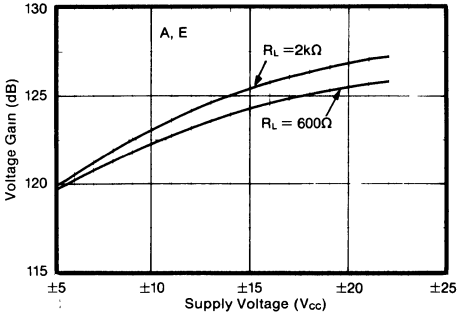
COMMON-MODE REJECTION vs FREQUENCY



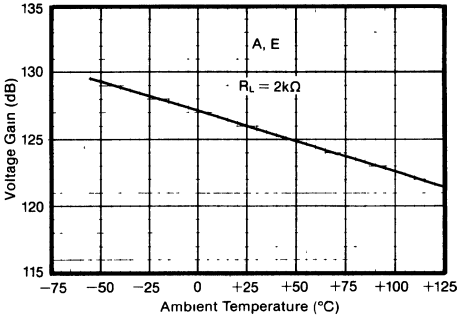
POWER SUPPLY REJECTION vs FREQUENCY



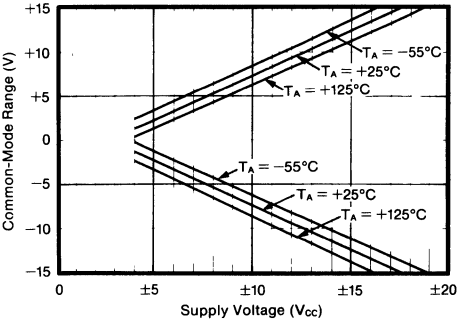
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



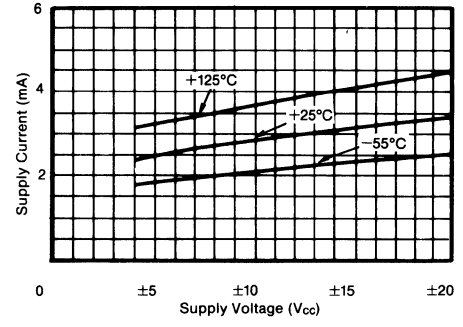
OPEN-LOOP VOLTAGE GAIN vs TEMPERATURE



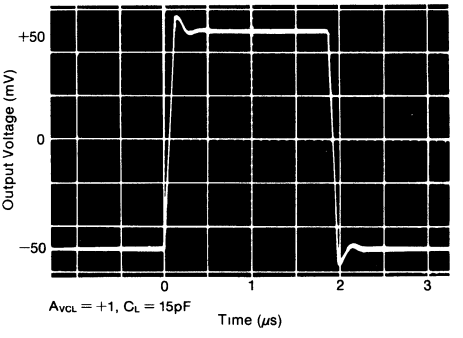
COMMON-MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE



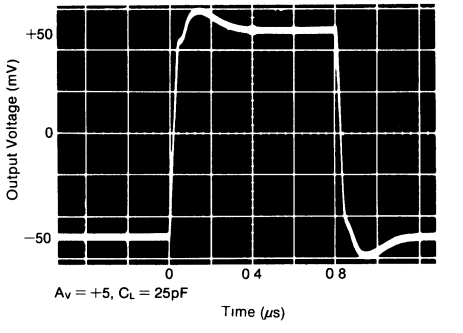
SUPPLY CURRENT vs SUPPLY VOLTAGE



OPA27 SMALL SIGNAL TRANSIENT RESPONSE

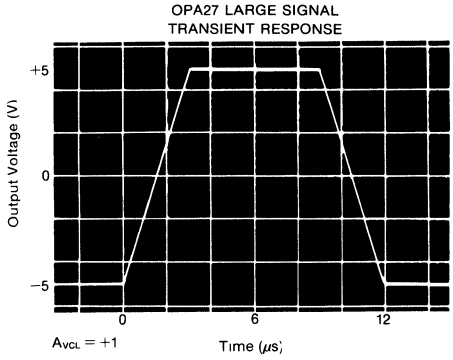


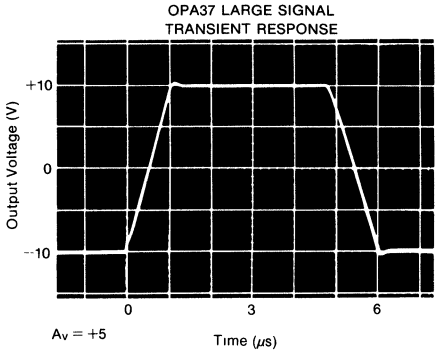
OPA37 SMALL SIGNAL TRANSIENT RESPONSE



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, $\pm V_{CC}$ = ±15VDC unless otherwise noted





APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA27/37 offset voltage is laser-trimmed and will require no further trim for most applications. Offset voltage drift will not be degraded when the input offset is nulled with a 10kΩ trim potentiometer. Other potentiometer values from 1kΩ to 1MΩ can be used but V_{OS} drift will be degraded by an additional 0.1 to 0.2μV/°C. Nulling large system offsets by use of the offset trim adjust will degrade drift performance by approximately 3.3μV/°C per millivolt of offset. Large system offsets can be nulled without drift degradation by input summing.

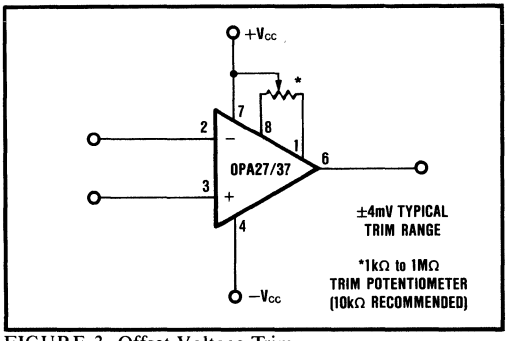


FIGURE 3. Offset Voltage Trim.

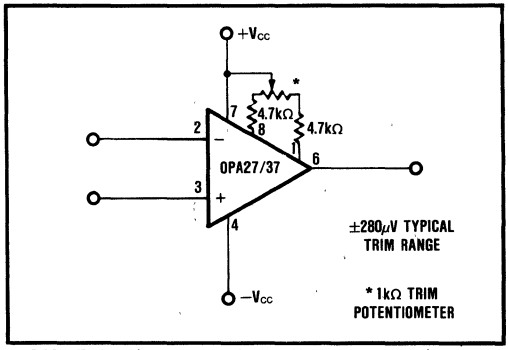


FIGURE 4. High Resolution Offset Voltage Trim.

The conventional offset voltage trim circuit is shown in Figure 3. For trimming very-small offsets, the higher resolution circuit shown in Figure 4 is recommended.

The OPA27/37 can replace 741-type operational amplifiers by removing or modifying the trim circuit.

THERMOELECTRIC POTENTIALS

The OPA27/37 is laser-trimmed to microvolt-level input offset voltage and for very-low input offset voltage drift.

Careful layout and circuit design techniques are necessary to prevent offset and drift errors from external thermoelectric potentials. Dissimilar metal junctions can generate small EMF's if care is not taken to eliminate either their sources (lead-to-PC, wiring, etc.) or their temperature difference. See Figure 11.

Short, direct mounting of the OPA27/37 with close spacing of the input pins is highly recommended. Poor layout can result in circuit drifts and offsets which are an order of magnitude greater than the operational amplifier alone.

NOISE: BIPOLAR VERSUS FET

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ the Burr-Brown OPA111 low-noise FET operational amplifier is recommended for lower total noise than the OPA27 (see Figure 5).

COMPENSATION

Although internally compensated for unity-gain stability, the OPA27 may require a small capacitor in parallel with a feedback resistor (R_f) which is greater than 2kΩ. This capacitor will compensate the pole generated by R_f and C_{IN} and eliminate peaking or oscillation.

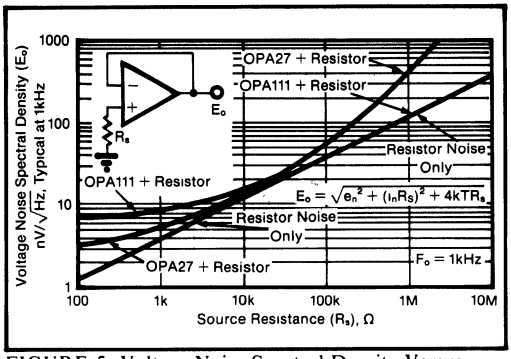


FIGURE 5. Voltage Noise Spectral Density Versus Source Resistance.

INPUT PROTECTION

Back-to-back diodes are used for input protection on the OPA27/37. Exceeding a few hundred millivolts differential input signal will cause current to flow and without external current limiting resistors the input will be destroyed.

Accidental static discharge as well as high current can damage the amplifier's input circuit. Although the unit may still be functional, important parameters such as input offset voltage, drift, and noise may be permanently damaged if any precision operational amplifier is subjected to abuse.

Transient conditions can cause feedthrough due to the amplifier's finite slew-rate. When using the OP-27 as a unity-gain buffer (follower) a feedback resistor of 1kΩ is recommended (see Figure 6).

BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information table. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

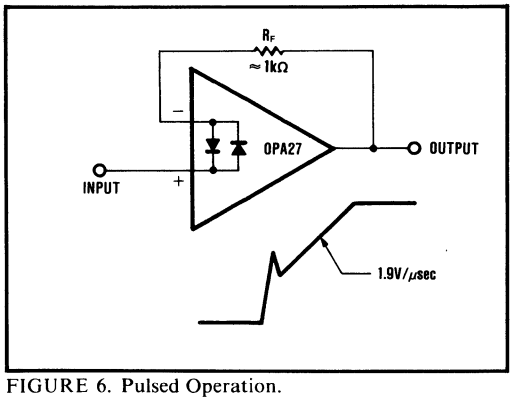


FIGURE 6. Pulsed Operation.

APPLICATIONS CIRCUITS

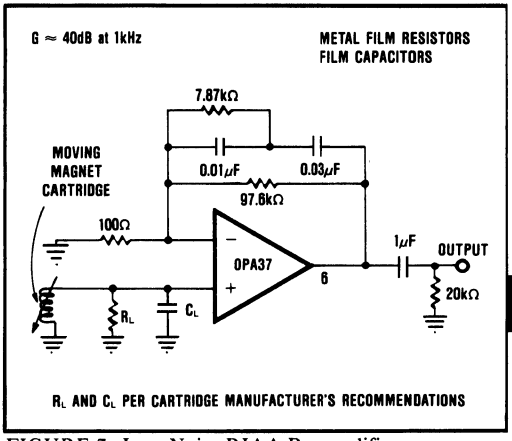


FIGURE 7. Low-Noise RIAA Preamplifier.

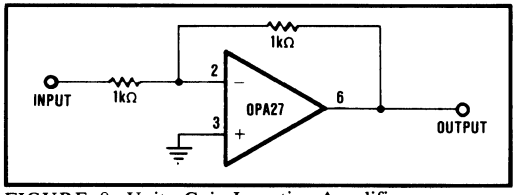


FIGURE 8. Unity-Gain Inverting Amplifier.

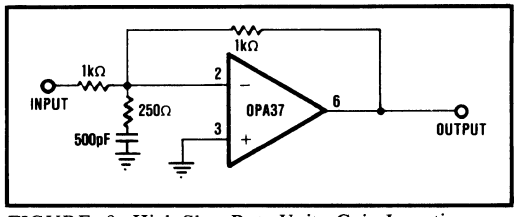


FIGURE 9. High Slew Rate Unity-Gain Inverting Amplifier.

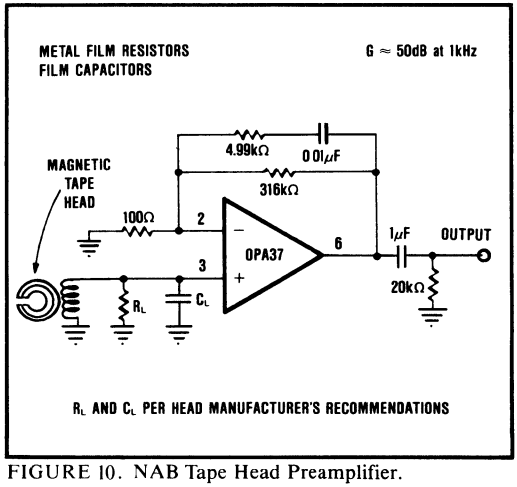


FIGURE 10. NAB Tape Head Preamplifier.

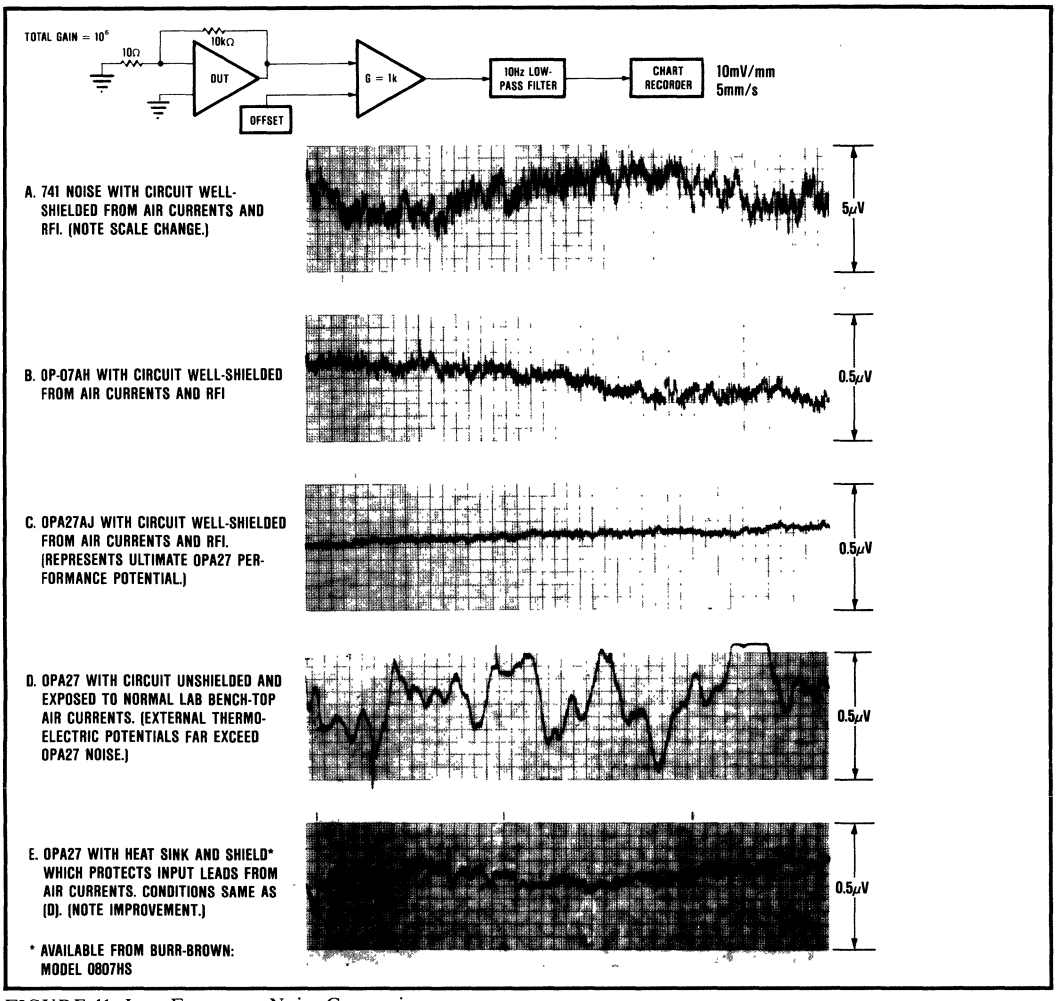


FIGURE 11. Low Frequency Noise Comparison.

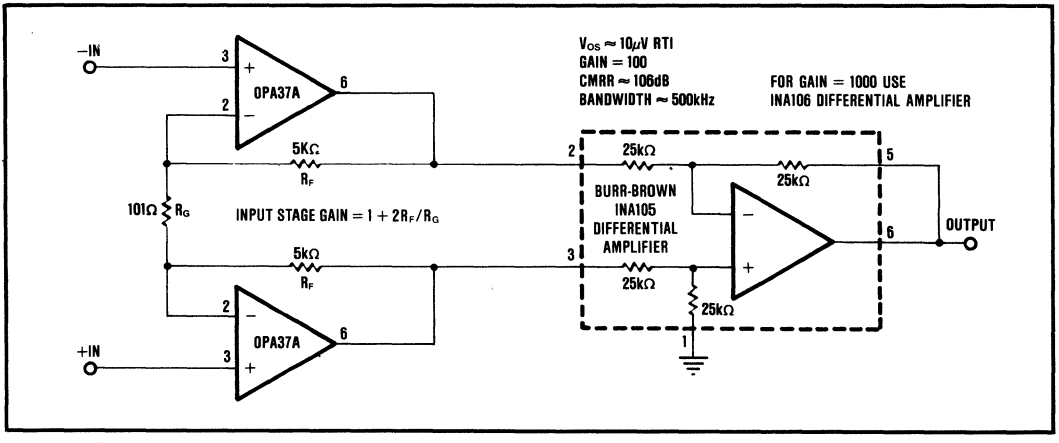


FIGURE 12. Low Noise Instrumentation Amplifier.

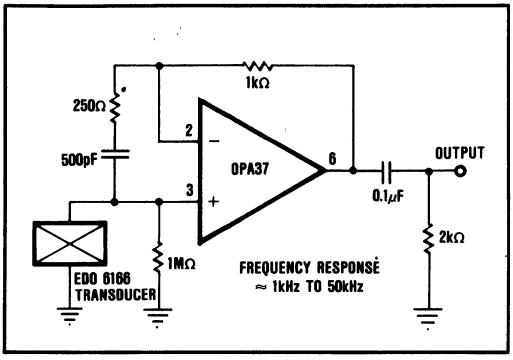


FIGURE 13. Hydrophone Preamplifier.

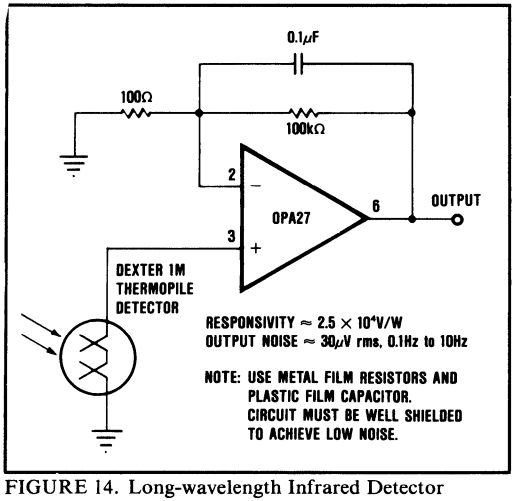


FIGURE 14. Long-wavelength Infrared Detector Amplifier.

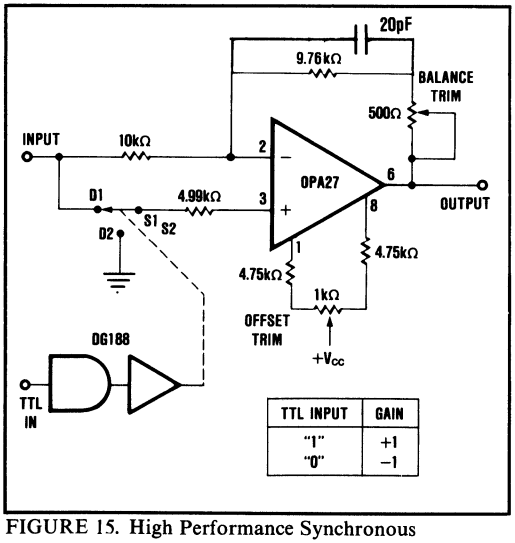


FIGURE 15. High Performance Synchronous Demodulator.

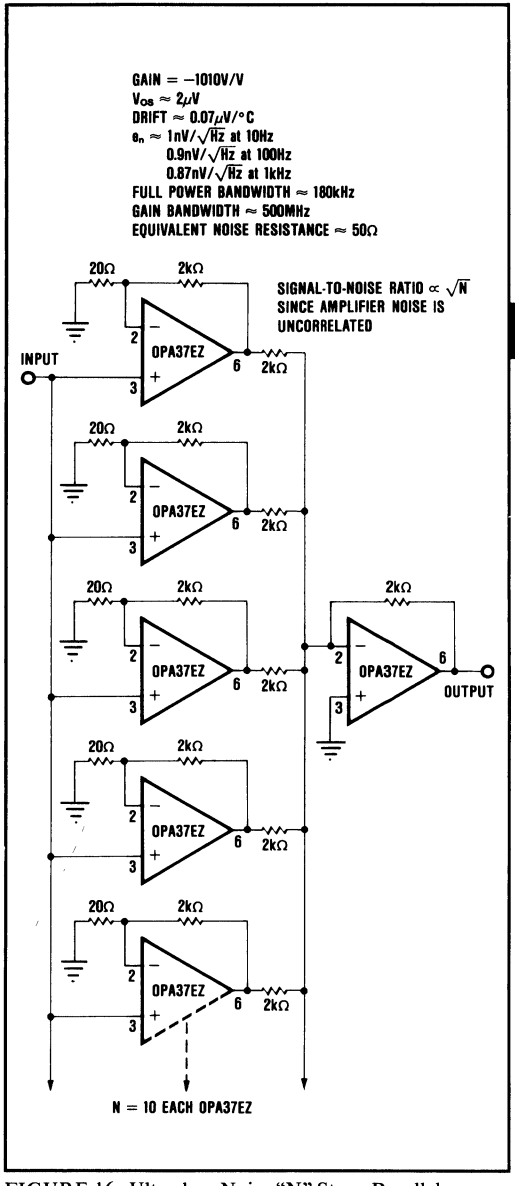


FIGURE 16. Ultra-low Noise "N" Stage Parallel Amplifier.

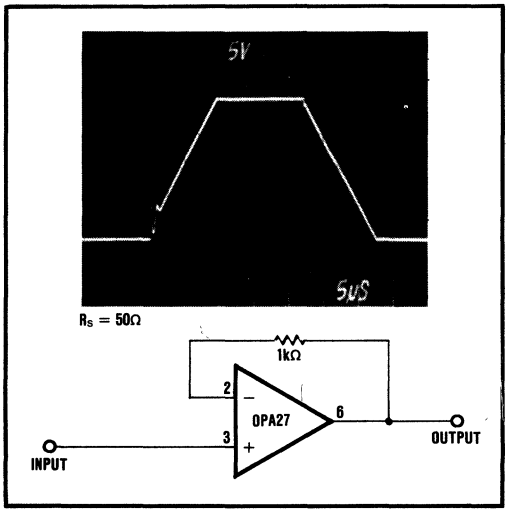


FIGURE 17. Unity-Gain Buffer.

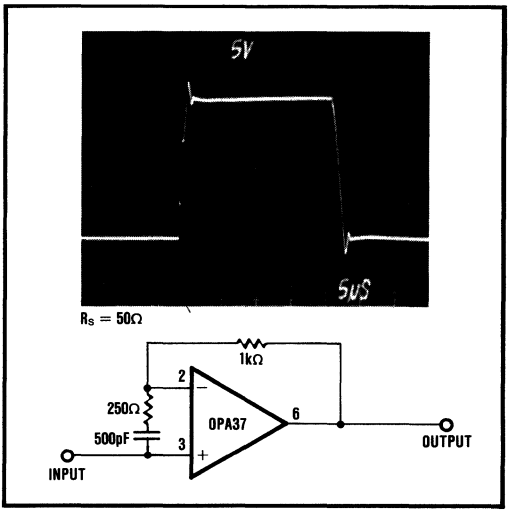


FIGURE 18. High Slew Rate Unity-Gain Buffer.

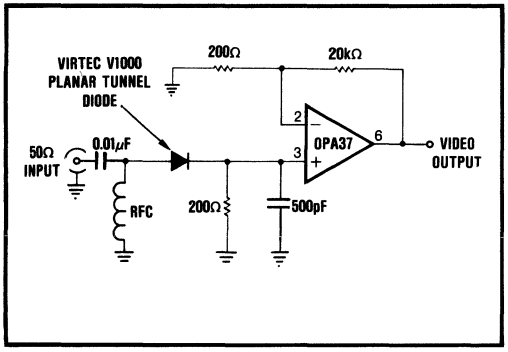


FIGURE 19. RF Detector and Video Amplifier.

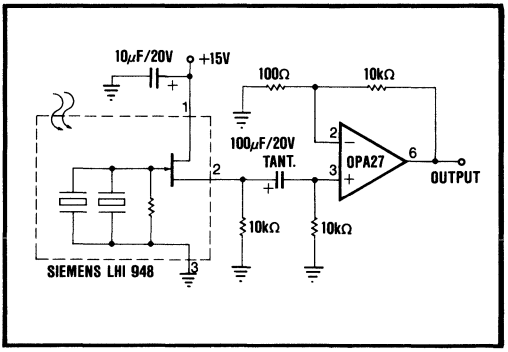


FIGURE 20. Balanced Pyroelectric Infrared Detector.

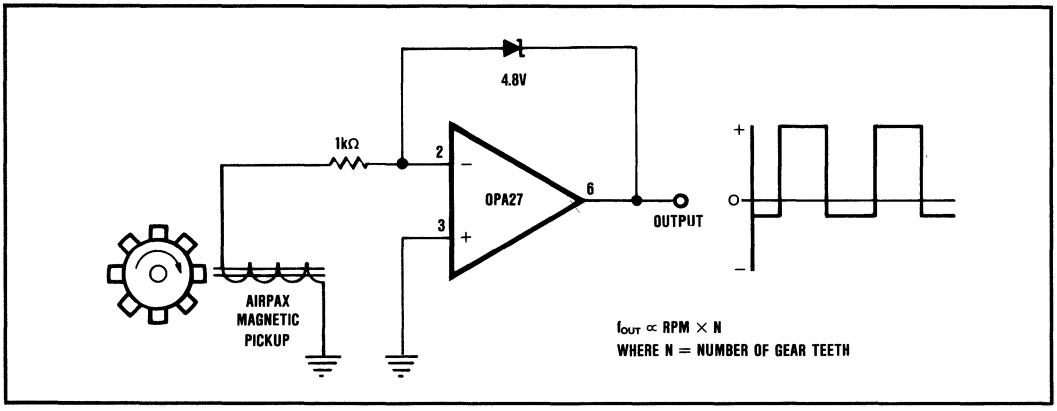
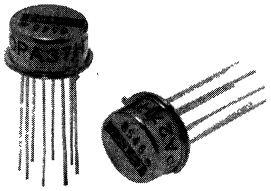


FIGURE 21. Magnetic Tachometer.

BURR-BROWN®



OPA27HT
OPA37HT*

* OPA37HT NOT RECOMMENDED FOR NEW DESIGNS.

Wide Temperature Range Precision OPERATIONAL AMPLIFIERS

FEATURES

- FULLY SPECIFIED OVER −55°C to +200°C
- LOW OFFSET: ±400μV max at +200°C
- LOW DRIFT: ±0.4μV/°C
- ULTRA-LOW NOISE
- MONOLITHIC
- HERMETIC TO-99 PACKAGE
- 100% BURN-IN AT +200°C

APPLICATIONS

- DOWN-HOLE INSTRUMENTATION
- WELL LOGGING
- ENGINE CONTROLS
- EXTREMELY SEVERE ENVIRONMENT
- TRANSDUCER AMPLIFIER
- RADIATION HARD EQUIPMENT

DESCRIPTION

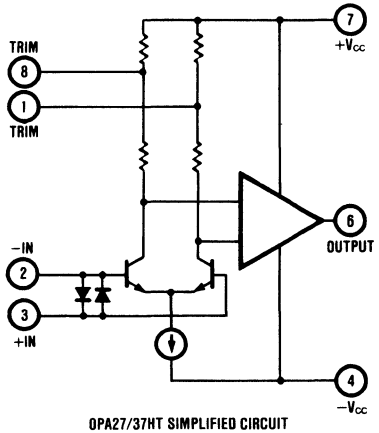
The OPA27/37HT is an ultra-low noise, high precision monolithic operational amplifier.

Laser trimmed thin-film resistors provide excellent long-term voltage offset stability and allow superior voltage offset and drift performance.

The OPA27/37HT are tested and guaranteed over an extremely wide temperature range: −55°C to +200°C. In addition, they have demonstrated an ability to withstand a total dose of 2×10^6 RAD (Si) gamma and a neutron fluence of 1×10^{13}, 1MEV equivalent n/cm^2.

The OPA27HT is internally compensated for unity-gain stability. The decompensated OPA37HT requires a closed-loop gain ≥ 5.

The Burr-Brown OPA27/37HT use an industry-standard OP27/37 pinout and they can replace many existing amplifiers in low-source-impedance applications.



OPA27/37HT SIMPLIFIED CIRCUIT

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable. BBRCORP - Telex: 66-6491

PDS-656A

SPECIFICATIONS

ELECTRICAL

At V_{CC} = 15VDC, T_A = indicated temperature

PARAMETER	CONDITIONS	+25°C			−55°C TO +125°C			+200°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
NOISE											
Voltage, f_O = 10Hz	(1)		3 1			8 5			5.6		nV/√Hz
f_O = 30Hz	(1)		2 9			4.0			4 5		nV/√Hz
f_O = 1kHz	(1)		2.7			3.6			4 0		nV/√Hz
f_B = 0 1Hz to 10Hz			0.07								μV, p-p
Current, f_O = 1kHz			0.4			0.5			0 8		pA/√Hz
OFFSET VOLTAGE[2]											
Input Offset Voltage			±25	±75		±37	±200		±150	±400	μV
Average Drift[3]	$T_{A\ MIN}$ to $T_{A\ MAX}$								±0 4		μV/°C
Long Term Stability[4]	T_A = +125°C		8								μV/kHrs
Supply Rejection[7]	±V_{CC} = 4V to 18V	100	134		94	127		94	127		dB
	±V_{CC} = 4V to 18V		±0.2	±10		±0.45	±20		±0 45	±20	μV/V
BIAS CURRENT											
Input Bias Current			430	1μA		600	2μA		3 4μA	5μA	nA
OFFSET CURRENT											
Input Offset Current			±40	±180		±50	±200		±300	±550	nA
IMPEDANCE											
Common-Mode			3								GΩ
VOLTAGE RANGE											
Common-Mode Input Range		±11	±12.3		±10.3	±11 5		±9 0	±11 0		V
Common-Mode Rejection	V_{IN} = ±10VDC[5]	106	128		100	122		96	119		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	120	126		109	120		104	113		dB
	$R_L \geq 1k\Omega$	116	125								dB
FREQUENCY RESPONSE											
Gain-Bandwidth Product	OPA27HT		6			7			6		MHz
A_V = 1000V/V	OPA37HT		36			38			41		MHz
Slew Rate	V_O = ±10V, R_L = 2kΩ										
	OPA27HT, G = +1		1.9			1.7			3 5		V/μs
	OPA37HT, G = +5		11.9			10			16		V/μs
Settling Time, 0.01%	OPA27HT, G = +1		25								μs
	OPA37HT, G = +5		25								μs
RATED OUTPUT											
Voltage Output	$R_L \geq 2k\Omega$	±12	±13.9		±11	±13 8		±10 5	±13 7		V
Output Resistance	DC, open loop		70								Ω
Short Circuit Current	R_L = 0Ω		35	60		25			15		mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated Performance		±4		±18							VDC
Current, Quiescent	I_O = 0mADC		3.6	4.7		4 3	6		6 1	8	mA
TEMPERATURE RANGE											
Specification[6]	Ambient temp.	−55		+200							°C
Operating (Typical)	Ambient temp	−65		+225							°C
Storage	Ambient temp.	−65		+225							°C
θ Junction-Ambient			125								°C/W

NOTES (1) Noise testing available—inquire (2) Offset voltage specifications on grade HT are also guaranteed with units fully warmed up (3) Unnulled or nulled with 8kΩ to 20kΩ potentiometer (4) Long-term voltage offset vs time trend line does not include warm-up drift (5) Common-mode rejection specified at +200°C with V_{IN} = ±9VDC (6) 100% tested at −55°C, +25°C and +200°C using forced-air environment +125°C specification is guaranteed by design (7) ±V_{CC} = 6V to 18V at +200°C

ABSOLUTE MAXIMUM RATINGS

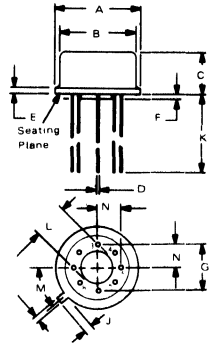
Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage[2]	±0.7VDC
Input Voltage Range[3]	±18VDC
Storage Temperature Range	−65°C to +225°C
Operating Temperature Range	−65°C to +225°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[4]	Continuous
Junction Temperature	+250°C

NOTES (1) Packages must be derated based on θ_{JC} = 45°C/W or θ_{JA} = 175°C/W (2) The inputs are protected by back-to-back diodes Current limiting resistors are not used in order to achieve low noise If differential input voltage exceeds ±0 7V, the input current should be limited to 25mA (3) For supply voltages less than ±18VDC, the absolute maximum input voltage is equal to the supply voltage (4) Short circuit may be to power supply common only Rating applies to +25°C ambient Observe dissipation limit and T_J

MECHANICAL

"M" PACKAGE TO-99 (Hermetic)

NOTE
Leads in true position within .010" (.25mm R) at MMC at seating plane

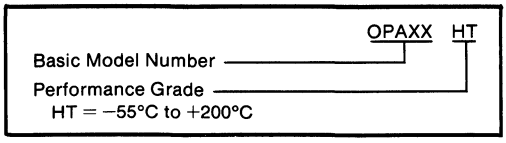


Pin numbers shown for reference only Numbers may not be marked on package

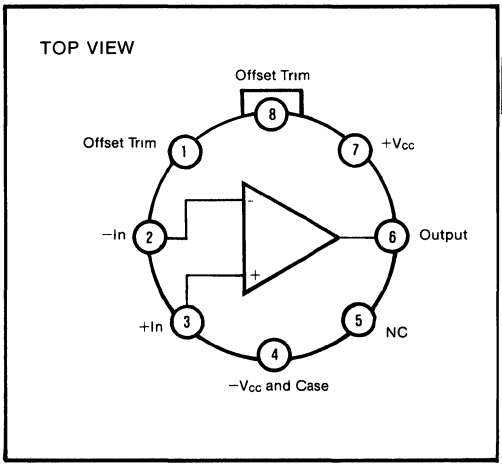
Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3 2)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

ORDERING INFORMATION



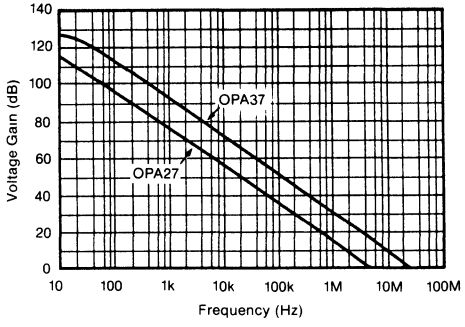
CONNECTION DIAGRAM



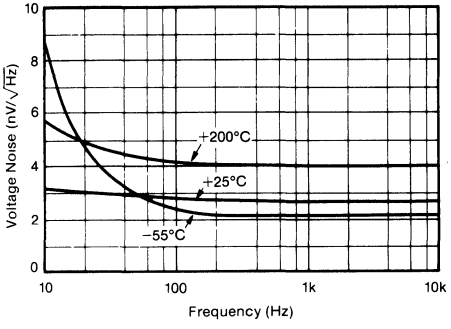
TYPICAL PERFORMANCE CURVES

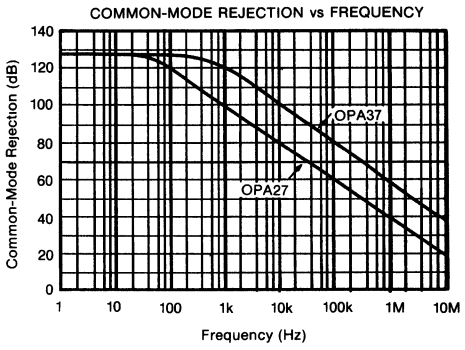
T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted

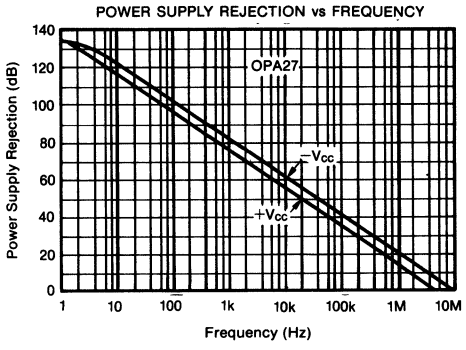
OPEN-LOOP FREQUENCY RESPONSE

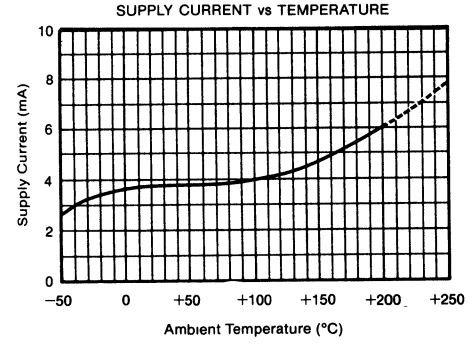


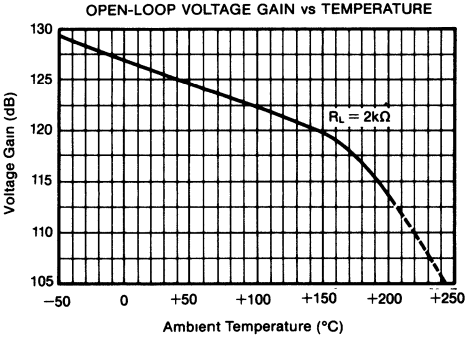
INPUT VOLTAGE NOISE SPECTRAL DENSITY

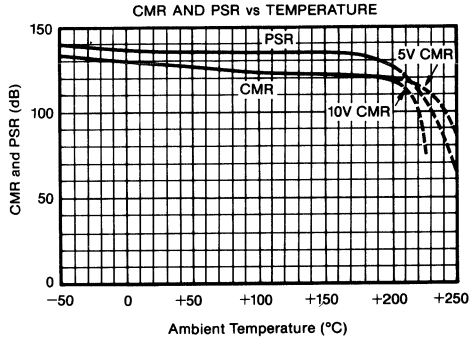


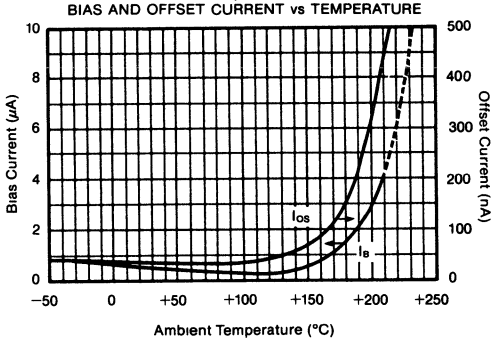










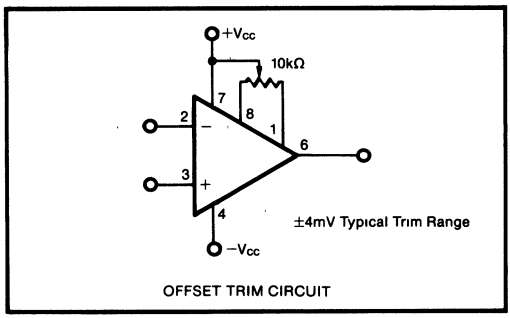


APPLICATIONS INFORMATION

These amplifiers are capable of unusually low voltage offset and drift and to achieve this ultimate capability, attention must be paid to externally generated thermal EMF contributions. Dissimilar metal junctions together with temperature gradients can generate thermocouple voltages that exceed the OPA27/37HT amplifier drift.

The OPA27/37HT are extremely wide-temperature range versions of the standard Burr-Brown OPA27 and OPA37. These high-temperature amplifiers do not employ bias current cancellation but note that their noise current performance has not been degraded.

Eutectic die attach is used exclusively for the OPA27HT and OPA37HT. Hermeticity is assured by 100% fine leak testing. Units are 100% burned-in for 28 hours at +200°C for increased reliability.



BURR-BROWN®

OPA101
OPA102

Low Noise - Wideband
PRECISION JFET INPUT OPERATIONAL AMPLIFIER

FEATURES

- GUARANTEED NOISE SPECTRAL DENSITY - 100% Tested
- LOW VOLTAGE NOISE - 8nV/$\sqrt{Hz}$ max at 10kHz
- LOW VOLTAGE DRIFT - 5μV/°C max (B grade)
- LOW OFFSET VOLTAGE - 250μV max (B grade)
- LOW BIAS CURRENTS - 10pA max at 25°C Ambient (B Grade)
- HIGH SPEED - 10V/μsec min (OPA102)
- GAIN BANDWIDTH PRODUCT - 40MHz (OPA102)

APPLICATIONS

- LOW NOISE SIGNAL CONDITIONING
- LIGHT MEASURMENTS
- RADIATION MEASUREMENTS
- PIN DIODE APPLICATIONS
- DENSITOMETERS
- PHOTODIODE/PHOTOMULTIPLIER CIRCUITS
- LOW NOISE DATA ACQUISITION

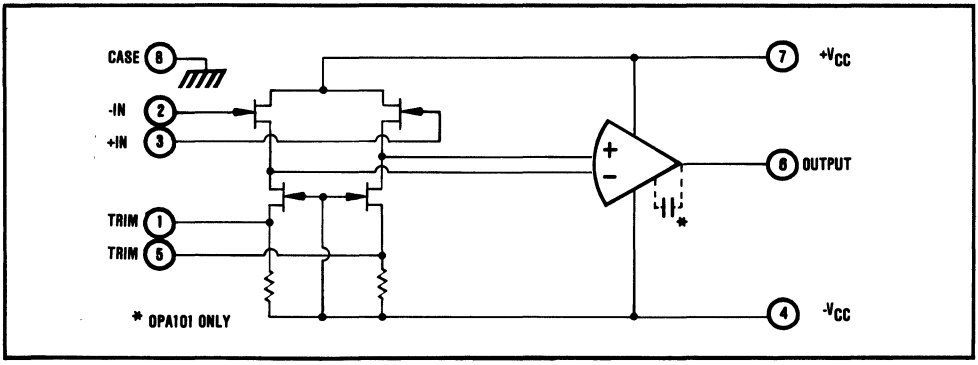
DESCRIPTION

The OPA101 and OPA102 are the first FET operational amplifiers available with noise characteristics (voltage spectral density) guaranteed and 100% tested.

The amplifiers have a complementary set of specifications permitting low errors in signal conditioning applications; low noise, low bias current, high open-loop gain, high common-mode rejection, low offset voltage, low offset voltage drift, etc.

In addition, the amplifiers have moderately high speed. The OPA101 is compensated for unity gain stability and has a slew rate of 5V/μsec, min. The OPA102 is compensated for gains of 3V/V and above and has a slew rate of 10V/μsec, min.

Each unit is laser-trimmed for low offset voltage and low offset voltage drift versus temperature. Bias currents are specified with the units fully warmed up at +25°C ambient temperature.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-434B

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_{CC}$ = ±15VDC unless otherwise noted.

MODEL		OPA101/102AM			OPA101/102BM			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT NOISE								
Voltage Noise Density	f_O = 1Hz(1)		100	200		80	100	nV/√Hz
	f_O = 10Hz		32	60		25	30	nV/√Hz
	f_O = 100Hz		14	30		11	15	nV/√Hz
	f_O = 1kHz		9	15		8	12	nV/√Hz
	f_O = 10kHz		7	8		7	8	nV/√Hz
	f_O = 100kHz		6.5	8		6.5	8	nV/√Hz
f_C, 1/f Corner Frequency			125			100		Hz
Voltage Noise	f_B = 0.1Hz to 10Hz(1)		1.3	2.6		1.0	1.3	μV, p-p
	f_B = 10Hz to 10kHz		1.0	1.2		0.8	1.0	μV, rms
	f_B = 10Hz to 100kHz		2 1	2 6		2.1	2 6	μV, rms
Current Noise Density	f_O = 0.1Hz thru 10kHz		2.0			1 4		fA/√Hz
Current Noise	f_B = 0 1Hz to 10Hz		38			26		fA, p-p
	f_B = 10Hz to 10kHz		200			140		fA, rms
DYNAMIC RESPONSE								
Bandwidth, Unity Gain	Small Signal							
OPA101			10			*		MHz
OPA102			Note 2			*		
Gain-Bandwidth Product	A_{CL} = 100							
OPA101			20			*		MHz
OPA102			40			*		MHz
Full Power Bandwidth	V_O = 20V, p-p, R_L = 1kΩ							
OPA101		80	100		*	*		kHz
OPA102		160	210		*	*		kHz
Slew Rate	V_O = ±10V; R_L = 1kΩ							
OPA101	A_{CL} = -1	5	6 5		*	*		V/μsec
OPA102	A_{CL} = -3	10	14		*	*		V/μsec
Settling Time (OPA101)	V_O = ±5V, A_{CL} = -1, R_L = 1kΩ							
ε = 1%			2			*		μsec
ε = 0.1%			2 5			*		μsec
ε = 0 01%			10			*		μsec
Settling Time (OPA102)	V_O = ±5V; A_{CL} = -3; R_L = 1kΩ							
ε = 1%			1			*		μsec
ε = 0 1%			1.5			*		μsec
ε = 0 01%			8			*		μsec
Small-Signal Overshoot	R_L = 1kΩ, C_L = 100pF							
OPA101	A_{CL} = +1		15			*		%
OPA102	A_{CL} = +3		20			*		%
Rise Time	10% to 90%, Small Signal							
OPA101			40			*		nsec
OPA102			30			*		nsec
Phase Margin	R_L = 1kΩ							
OPA101	A_{CL} = +1		60			*		Degrees
OPA102	A_{CL} = +3		45			*		Degrees
Overload Recovery(3)								
OPA101	A_{CL} = -1, 50% overdrive		1			*		μsec
OPA102	A_{CL} = -3, 50% overdrive		0 8			*		μsec
OPEN-LOOP GAIN, DC								
Full Load	V_O = ±10V, R_L = 1kΩ	94	105		*	*		dB
No Load	V_O = ±10V; R_L ≥ 10kΩ	96	108		*	*		dB
RATED OUTPUT								
Voltage	I_O = ±12mA	±12	±13		*	*		V
Current	V_O = ±12V	±12	±30		*	*		mA
Output Resistance	Open-Loop, f = DC		500			*		Ω
Short-Circuit Current			±45			*		mA
Capacitive Load Range	Phase Margin ≥ 25°							
OPA101	A_{CL} = +1		500			*		pF
OPA102	A_{CL} = +3		300			*		pF
INPUT OFFSET VOLTAGE								
Initial Offset	T_A = +25°C		±100	±500		±50	±250	μV
vs Temperature	-25°C ≤ T_A ≤ +85°C		±6	±10		±3	±5	μV/°C
vs Supply Voltage	±5VDC ≤ | V_{CC} | ≤ ±20VDC		±10	±50		*	*	μV/V
vs Time			±10			*		μV/mo.
Adjustment Range	Circuit in "Connection Diagram"		±1			*		mV
INPUT BIAS CURRENT								
Initial Bias	T_A = +25°C		-12	-15		-6	-10	pA
vs Temperature			Note 4			*		
vs Supply Voltage			Note 5			*		

ELECTRICAL (CONT)

MODEL		OPA101/102AM			OPA101/102BM			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT DIFFERENCE CURRENT								
Initial Difference	T_A = +25°C		±3	±6		±1 5	±4	pA
vs Temperature			Note 4			*		
vs Supply Voltage			Note 5			*		
INPUT IMPEDANCE								
Differential								
Resistance			10^{12}			*		Ω
Capacitance			1			*		pF
Common-mode								
Resistance			10^{13}			*		Ω
Capacitance			3			*		pF
INPUT VOLTAGE RANGE								
Common-mode Voltage Range	Linear Operation		±(| V_{CC} | -3)			*		V
Common-mode Rejection	f_o = DC, V_{CM} = ±10V	80	105		*	*		dB
POWER SUPPLY								
Rated Voltage			±15			*		VDC
Voltage Range	Derated Performance	±5		±20	*		*	VDC
Current, Quiescent			5 8	8		*	*	mA
TEMPERATURE RANGE								
Specification		-25		+85	*		*	°C
Operating	Derated Performance	-55		+125	*		*	°C
Storage		-65		+150	*		*	°C

NOTES *Specifications same as for OPA101/102AM.
1. Parameter is untested and is not guaranteed. This specification is established to a 90% confidence level
2 Minimum stable gain for the OPA102 is 3V/V.
3. Time required for output to return from saturation to linear operation following the removal of an input overdrive signal
4 Doubles approximately every 8 5°C
5 See Typical Performance Curves

ABSOLUTE MAXIMUM RATINGS

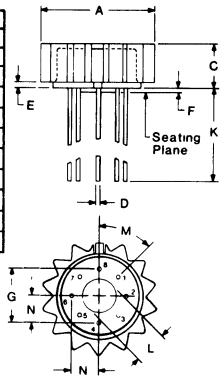
Supply	±20VDC
Internal Power Dissipation(1)	750mW
Differential Input Voltage(2)	±20VDC
Input Voltage, Either Input(2)	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-Circuit Duration(3)	60 seconds
Junction Temperature	+175°C

NOTES

1. Package must be derated according to the details in the Application Information section
2. For supply voltages less than ±20VDC, the absolute maximum input is equal to the supply voltage
3. Short-circuit may be to ground only. See discussion of Thermal Model in the Application Information section

MECHANICAL SPECIFICATIONS

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.489	.522	12.42	13.26
C	.243	.307	6.17	7.80
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67



NOTE

Leads in true position within .010" (.25mm) R at MMC at seating plane

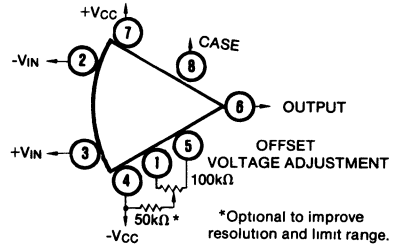
Pin numbers shown for reference only. Numbers may not be marked on package

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

Weight. 2 grams

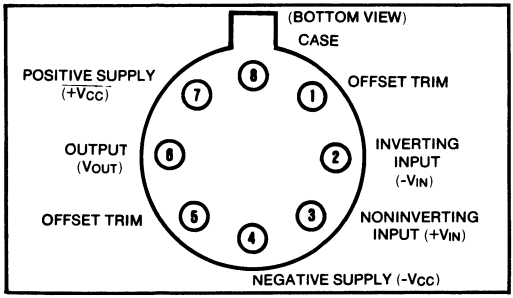
Order Number.
OPA101AM OPA101BM
OPA102AM OPA102BM

CONNECTION DIAGRAM



NOTE: Offset voltage adjustment affects voltage drift vs temperature by approximately ±0.3μV/°C for each 100μV of offset adjusted.

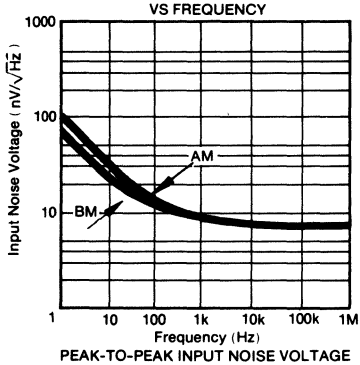
PIN CONFIGURATION



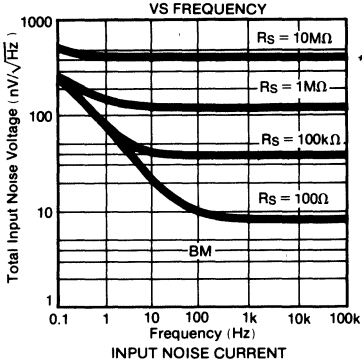
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, ±V_{CC} = ±15VDC, unless otherwise noted. Performance curves apply to both OPA101 and OPA102 unless otherwise noted.)

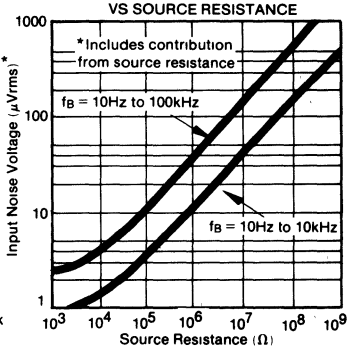
INPUT NOISE VOLTAGE VS FREQUENCY



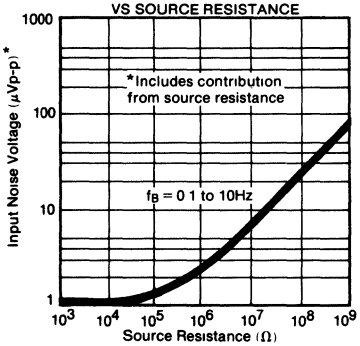
TOTAL INPUT NOISE VOLTAGE VS FREQUENCY



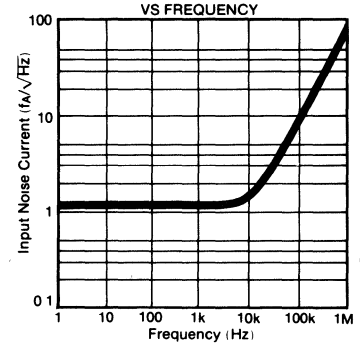
RMS INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



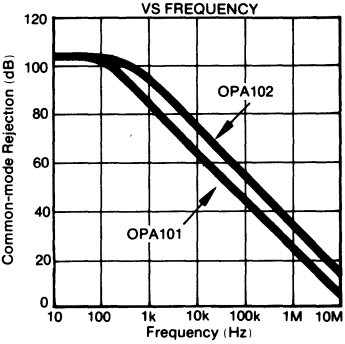
PEAK-TO-PEAK INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



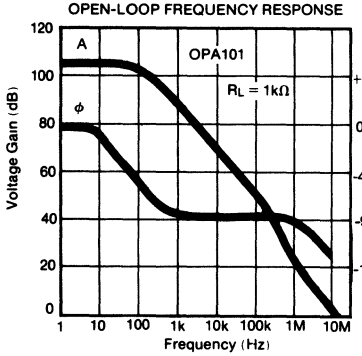
INPUT NOISE CURRENT VS FREQUENCY



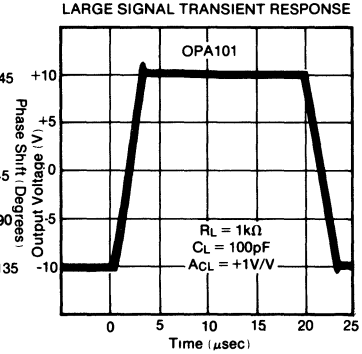
COMMON-MODE REJECTION VS FREQUENCY



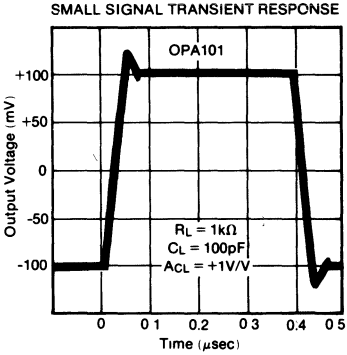
OPEN-LOOP FREQUENCY RESPONSE



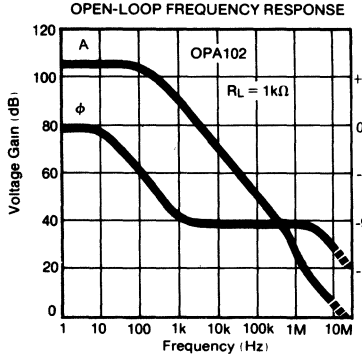
LARGE SIGNAL TRANSIENT RESPONSE



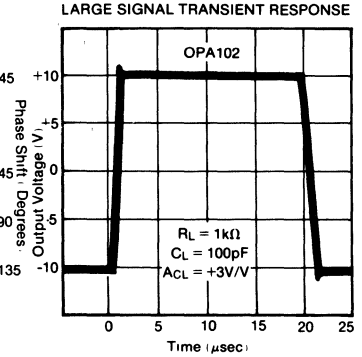
SMALL SIGNAL TRANSIENT RESPONSE



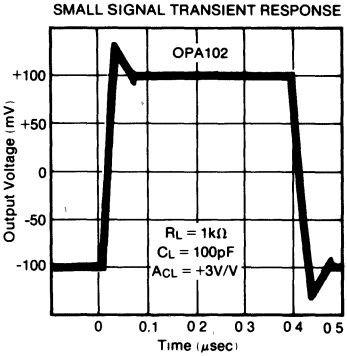
OPEN-LOOP FREQUENCY RESPONSE



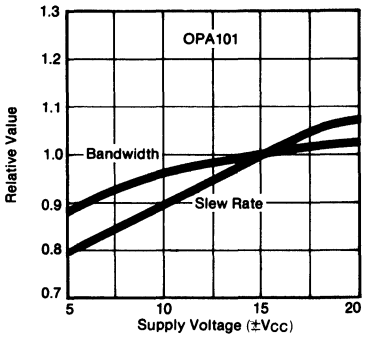
LARGE SIGNAL TRANSIENT RESPONSE



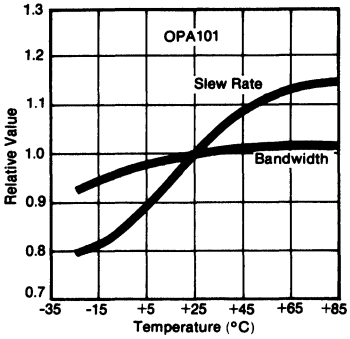
SMALL SIGNAL TRANSIENT RESPONSE



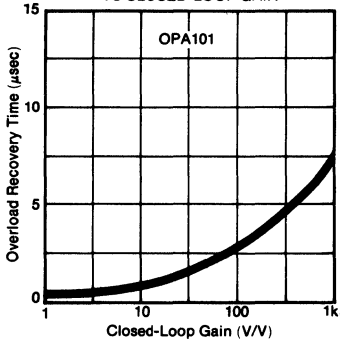
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



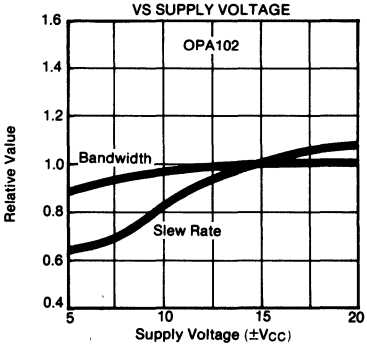
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



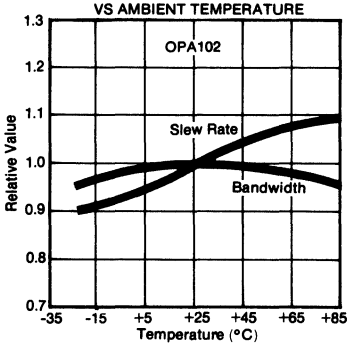
OVERLOAD RECOVERY TIME VS CLOSED-LOOP GAIN



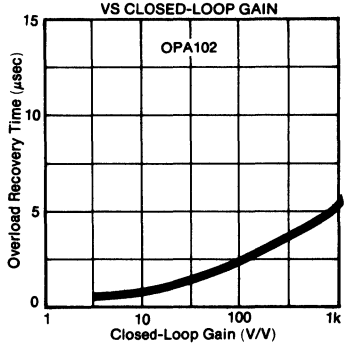
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



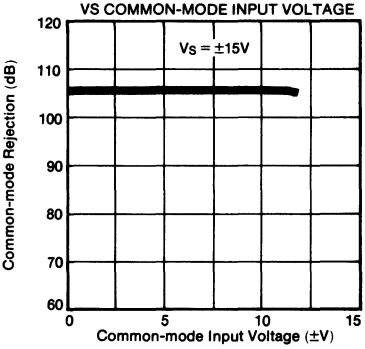
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



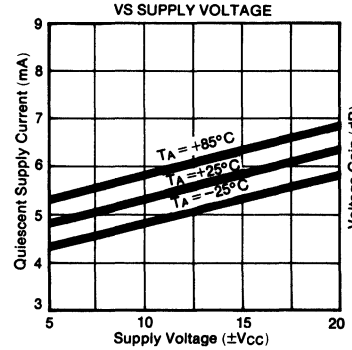
OVERLOAD RECOVERY TIME VS CLOSED-LOOP GAIN



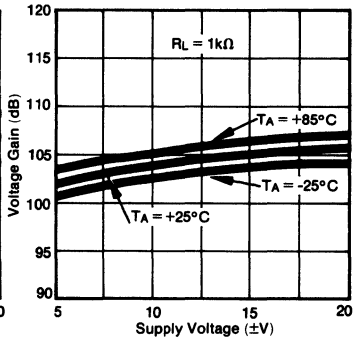
COMMON-MODE REJECTION VS COMMON-MODE INPUT VOLTAGE



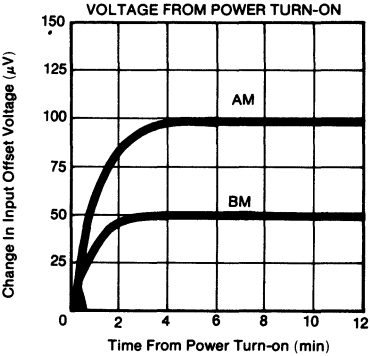
QUIESCENT SUPPLY CURRENT VS SUPPLY VOLTAGE



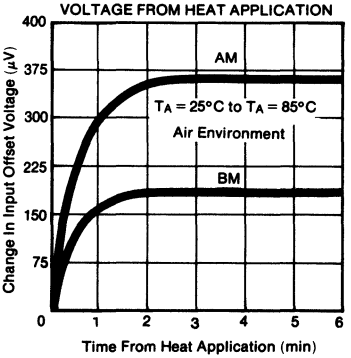
VOLTAGE GAIN VS SUPPLY VOLTAGE



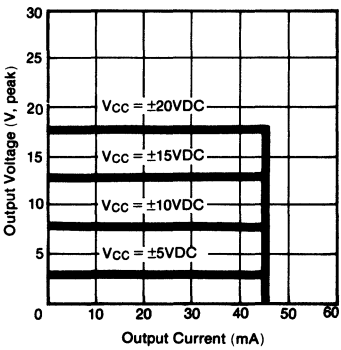
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



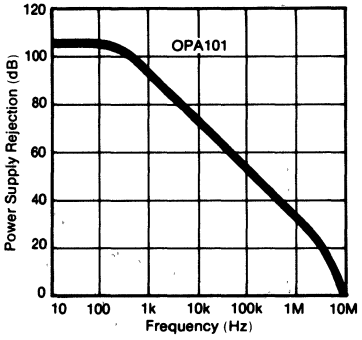
THERMAL RESPONSE TIME OF INPUT OFFSET VOLTAGE FROM HEAT APPLICATION



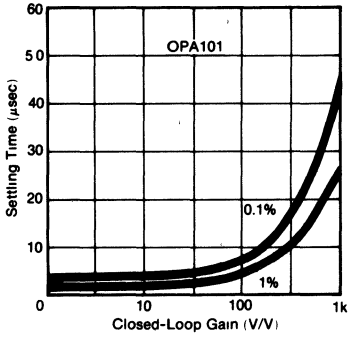
OUTPUT VOLTAGE VS OUTPUT CURRENT



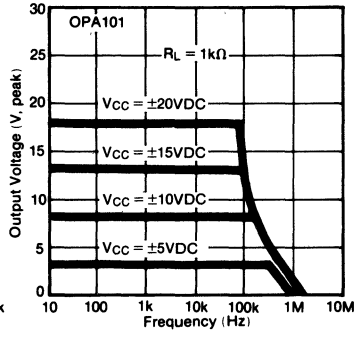
POWER SUPPLY REJECTION VS FREQUENCY



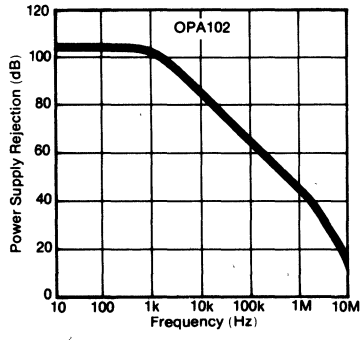
SETTLING TIME VS CLOSED-LOOP GAIN



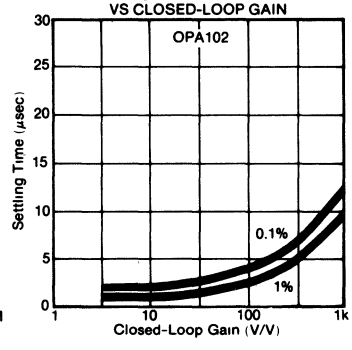
OUTPUT VOLTAGE VS FREQUENCY



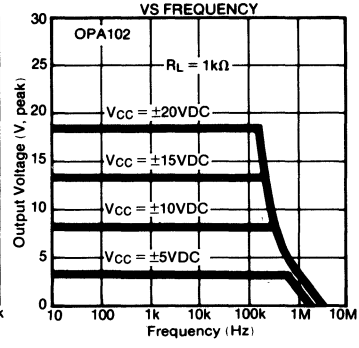
POWER SUPPLY REJECTION VS FREQUENCY



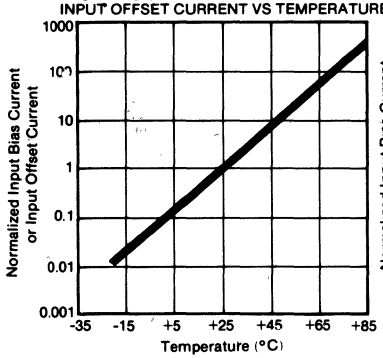
SETTLING TIME VS CLOSED-LOOP GAIN



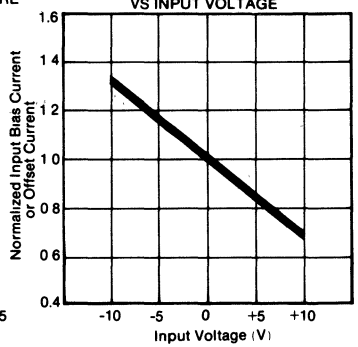
OUTPUT VOLTAGE VS FREQUENCY



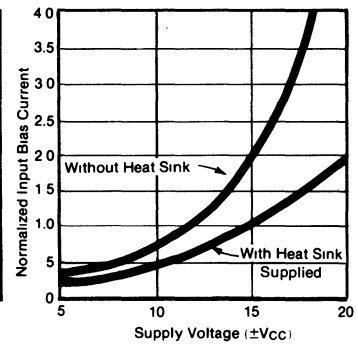
INPUT BIAS CURRENT VS TEMPERATURE AND INPUT OFFSET CURRENT VS TEMPERATURE



INPUT BIAS CURRENT VS INPUT VOLTAGE AND INPUT OFFSET CURRENT VS INPUT VOLTAGE



INPUT BIAS CURRENT VS SUPPLY VOLTAGE



APPLICATION INFORMATION

INTRODUCTION

The availability of detailed noise spectral density characteristics for the OPA101/102 amplifiers allows an accurate noise error analysis in a variety of different circuit configurations. The fact that the spectral characteristics are guaranteed maximums allows absolute noise errors to be truly bounded. Other FET amplifiers normally use simpler specifications of rms noise in a given bandwidth (typically 10Hz to 10kHz) and peak-to-peak noise (typically specified in the band 0.1Hz to 10Hz). These specifications do not contain enough information to allow accurate analysis of noise behavior in any but the simplest of circuit configurations.

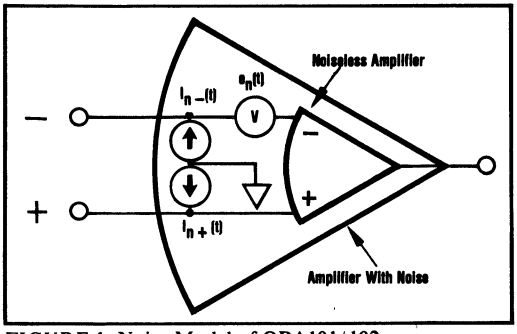


FIGURE 1. Noise Model of OPA101/102.

Noise in the OPA101/102 can be modeled as shown in Figure 1. This model is the same form as the DC model for offset voltage (E_{OS}) and bias currents (I_B). In fact, if the voltage $e_n(t)$ and currents $i_n(t)$ are thought of as general instantaneous error sources, then they could represent either noise or DC offsets. The error equations for the general instantaneous model are shown in Figure 2 below.

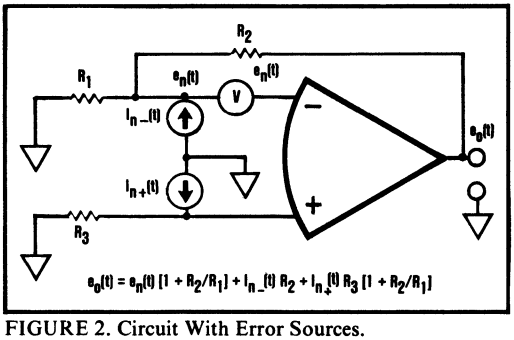


FIGURE 2. Circuit With Error Sources.

If the instantaneous terms represent DC errors (i.e., offset voltage and bias currents) the equation is a useful tool to compute actual errors. It is not, however, useful in the same direct way to compute noise errors. The basic problem is that noise cannot be predicted as a function of time. It is a random variable and must be described in probabilistic terms. It is normally described by some type of average - most commonly the rms value.

$$N_{rms} \triangleq \sqrt{1/T \int_0^T n^2(t)\, dt} \qquad (1)$$

where N_{rms} is the rms value of some random variable n(t). In the case of amplifier noise, n(t) represents either $e_n(t)$ or $i_n(t)$.

The internal noise sources in operational amplifiers are normally uncorrelated. That is, they are randomly related to each other in time and there is no systematic phase relationship. Uncorrelated noise quantities are combined as root-sum-squares. Thus, if $n_1(t)$, $n_2(t)$, and $n_3(t)$ are uncorrelated then their combined value is

$$N_{TOTAL_{rms}} = \sqrt{N_1^2{}_{rms} + N_2^2{}_{rms} + N_3^2{}_{rms}} \qquad (2)$$

The basic approach in noise error calculations then is to identify the noise sources, segment them into conveniently handled groups (in terms of the shape of their noise spectral densities), compute the rms value of each group, and then combine them by root-sum-squares to get the total noise.

TYPICAL APPLICATION

The circuit in Figure 3 is a common application of a low noise FET amplifier. It will be used to demonstrate the above noise calculation method.

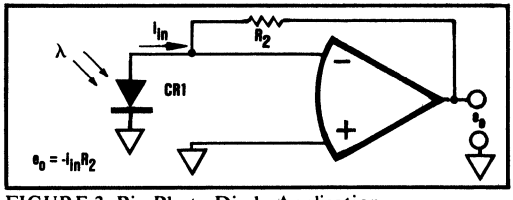


FIGURE 3. Pin Photo Diode Application.

CR1 is a PIN photo diode connected in the photovoltaic mode (no bias voltage) which produces an output current i_{in} when exposed to the light, λ.

A more complete circuit is shown in Figure 4. The values shown for C_1 and R_1 are typical for small geometry PIN diodes with sensitivities in the range of 0.5 A/W. The value of C_2 is what would be expected from stray capacitance with moderately careful layout (0.5pF to 2pF). A larger value of C_2 would normally be used to limit the bandwidth and reduce the voltage noise at higher frequencies.

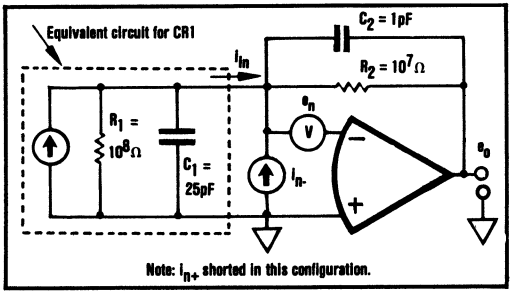


FIGURE 4. Noise Model of Photo Diode Application.

In Figure 4, e_n and i_n represent the amplifier's voltage and current spectral densities, $e_n(\omega)$ and $i_n(\omega)$ respectively. These are shown in Figure 5.

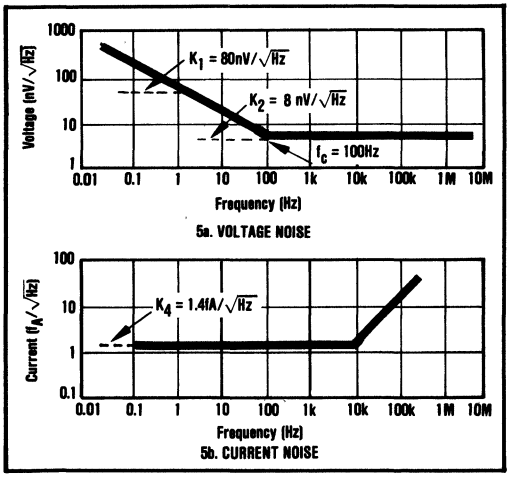


FIGURE 5. Noise Voltage and Current Spectral Density.

Figure 6 shows the desired "gain" of the circuit (transimpedance of $e_o/i_{in} = Z_2(s)$). It has a single-pole rolloff at $f_2 = 1/(2\pi R_2 C_2) = \omega_2/2\pi$. Output noise is minimized if f_2 is made smaller. Normally R_2 is chosen for the desired DC transimpedance based on the full scale input current (i_{in} full scale) and maximum output (e_o max). Then C_2 is chosen to make f_2 as small as possible consistent with the necessary signal frequency response.

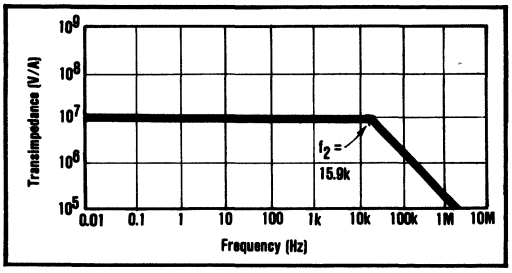


FIGURE 6. Transimpedance.

Voltage Noise

Figure 7 shows the noise voltage gain for the circuit in Figure 4. It is derived from the equation

$$e_o = e_n\left[\frac{A}{1+A\beta}\right] = e_n\,\frac{1}{\beta}\left[\frac{1}{1+\frac{1}{A\beta}}\right] \qquad (3)$$

where:

$A = A(\omega)$ is the open-loop gain

$\beta = \beta(\omega)$ is the feedback factor. It is the amount of output voltage feedback to the input of the op amp.

$A\beta = A(\omega)\,\beta(\omega)$ is the loop gain. It is the amount of the output voltage feedback to the input and then amplified and returned to the output.

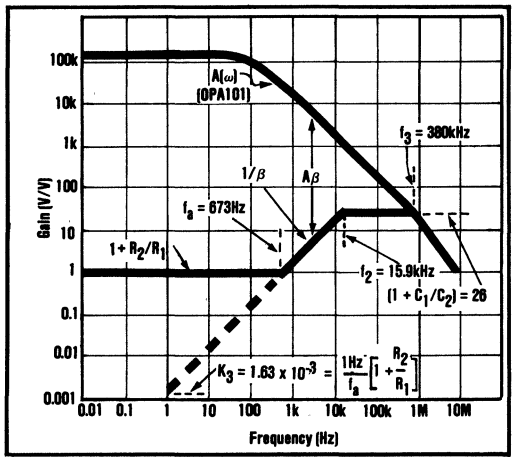


FIGURE 7. Noise Voltage Gain.

Note that for large loop gain ($A\beta >> 1$)

$$e_o \approx e_n\,\frac{1}{\beta}\,. \qquad (4)$$

For the circuit in Figure 4 it can be shown that

$$\frac{1}{\beta} = 1 + \frac{R_2(R_1C_1s+1)}{R_1(R_2C_2s+1)}\,. \qquad (5)$$

This may be rearranged to

$$\frac{1}{\beta} = \frac{R_2+R_1}{R_1}\left[\frac{\tau_a s+1}{\tau_2 s+1}\right] \qquad (5a)$$

where $\tau_a = (R_1 \parallel R_2)(C_1 \parallel C_2)$ (5b)

$$= \left[\frac{R_1R_2}{R_1+R_2}\right](C_1+C_2)$$

and $\tau_2 = R_2C_2$. (5c)

Then, $f_a = \dfrac{1}{2\pi\tau_a}$ and $f_2 = \dfrac{1}{2\pi\tau_2}$. (5d)

For very low frequencies ($f << f_a$), s approaches zero and equation 5 becomes

$$\frac{1}{\beta} = 1 + \frac{R_2}{R_1}\,. \qquad (6)$$

For very high frequencies ($f >> f_2$), s approaches infinity and equation 5 becomes

$$\frac{1}{\beta} = 1 + \frac{C_1}{C_2}\,. \qquad (7)$$

The noise voltage spectral density at the output is obtained by multiplying the amplifier's noise voltage spectral density (Figure 5a) times the circuits noise gain (Figure 7). Since both curves are plotted on log-log scales the multiplication can be performed by the addition of the two curves. The result is shown in Figure 8.

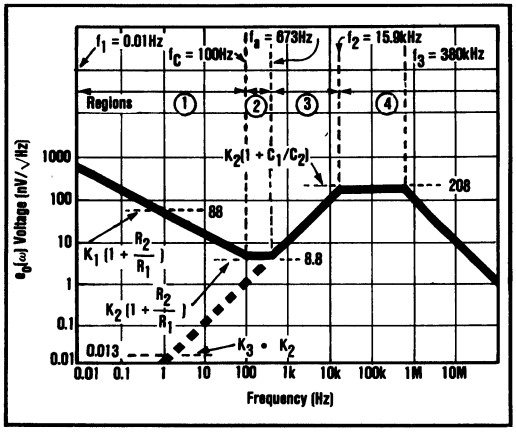


FIGURE 8. Output Noise Voltage Spectral Density.

The total rms noise at the amplifier's output due to the amplifier's internal voltage noise is derived from the $e_o(\omega)$ function in Figure 8 with the following expression:

$$E_{o\ rms} = \sqrt{\int_{-\infty}^{+\infty} e_o^2(\omega)\, d\omega} \qquad (8)$$

It is both convenient and informative to calculate the rms noise using a piecewise approach (region-by-region) for each of the four regions indicated in Figure 8.

Region 1; $f_1 = 0.01Hz$ to $f_c = 100Hz$

$$E_{n1\ rms} = K_1 \left(1 + \frac{R_2}{R_1}\right) \sqrt{\ln(f_c/f_1)} \qquad (9)$$

$$= 80nV/\sqrt{Hz}\ \left(1 + \frac{10^7}{10^8}\right) \sqrt{\ln \frac{100}{0.01}} \qquad (9a)$$

$$= 0.267\mu V$$

This region has the characteristic of 1/f or "pink" noise (slope of -10dB per decade on the log-log plot of $e_n(\omega)$). The selection of 0.01Hz is somewhat arbitrary but it can be shown that for this example there would be only negligible additional contribution by extending f_1 several decades lower. Note that $K_1(1 + R_2/R_1)$ is the value of e_o at f = 1Hz.

Region 2; $f_c = 100Hz$ to $f_a = 673Hz$

$$E_{n2\ rms} = K_2 \left(1 + \frac{R_2}{R_1}\right) \sqrt{f_a - f_c} \qquad (10)$$

$$= 8nV/\sqrt{Hz}\left(1 + \frac{10^7}{10^8}\right) \sqrt{673 - 100} \qquad (10a)$$

$$= 0.21\mu V$$

This is a region of "white" noise which leads to the form of equation (10).

Region 3; $f_a = 673Hz$ to $f_2 = 15.9kHz$

$$E_{n3\ rms} = K_2 \cdot K_3 \sqrt{\frac{f_2^3}{3} - \frac{f_a^3}{3}} \qquad (11)$$

$$= 8nV/\sqrt{Hz}\,(1.63 \times 10^{-3}) \sqrt{\frac{(15.9k)^3}{3} - \frac{(673)^3}{3}} \qquad (11a)$$

$$= 15.1\mu V$$

This is the region of increasing noise gain (slope of +20dB/decade on the log-log plot) caused by the lead network formed by the resistance $R_1 || R_2$ and the capacitance $(C_1 + C_2)$. Note that $K_3 \cdot K_2$ is the value of the $e_o(\omega)$ function for this segment projected back to 1Hz.

Region 4; f > 15.9kHz

$$E_{n4\ rms} = K_2 \left(1 + \frac{C_1}{C_2}\right) \sqrt{\left[\frac{\pi}{2}\right] f_3 - f_2} \qquad (12)$$

$$= 8nV/\sqrt{Hz}\left(1 + \frac{25}{1}\right) \sqrt{\left[\frac{\pi}{2}\right] 380k - 15.9k} \qquad (12a)$$

$$= 158.5\mu V$$

This is a region of white noise with a single order rolloff at $f_3 = 380kHz$ caused by the intersection of the $1/\beta$ curve and the open-loop gain curve. The value of 380kHz is obtained from observing the intersection point of Figure 7. The $\pi/2$ applied to f_3 is to convert from a 3dB corner frequency to an effective noise bandwidth.

Current Noise

The output voltage component due to current noise is equal to:

$$E_{ni} = i_n \times Z_2(s) \qquad (13)$$

where $Z_2(s) = R_2 \ || \ X_{C_2}$ (13a)

This voltage may be obtained by combining the information from figures 5 (b) and 6 together with the open loop gain curve of Figure 7. The result is shown in Figure 9 below.

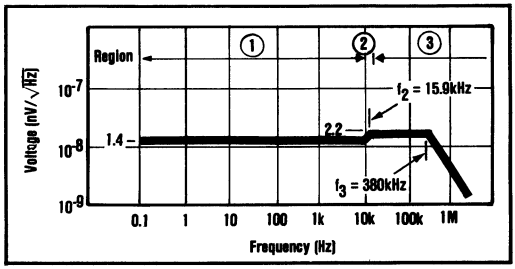


FIGURE 9. Output Voltage Due to Noise Current.

Using the same techniques that were used for the voltage noise:

Region 1; 0.1Hz to 10kHz

$$E_{ni1} = 1.4 \times 10^{-8} \sqrt{10k - 0.1} \quad (14)$$

$$= 1.4\mu V$$

Region 2; 10kHz to 15.9kHz

$$E_{ni2} = 1.4 \times 10^{-12} \sqrt{\frac{(15.9k)^3}{3} - \frac{(10k)^3}{3}} \quad (14a)$$

$$= 1.4\mu V$$

Region 3; f > 15.9kHz

$$E_{ni3} = 2.2 \times 10^{-8} \sqrt{\frac{\pi}{2} 380k - 15.9k} \quad (14b)$$

$$= 16.8\mu V$$

$$E_{ni\ total} = 10^{-6} \sqrt{(1.4)^2 + (1.4)^2 + (16.8)^2} \quad (14c)$$

$$= 16.9\mu V_{rms}$$

Resistor Noise

For a complete noise analysis of the circuit in Figure 4, the noise of the feedback resistor, R_2, must also be included. The thermal noise of the resistor is given by:

$$E_{R\ rms} = \sqrt{4kTRB} \quad (15)$$

K = Boltzmann's constant = 1.38×10^{-23} Joules/°Kelvin
T = Absolute temperature (degrees Kelvin)
R = Resistance (ohms)
B = Effective noise bandwidth (Hz) (ideal filter assumed)

At 25°C this becomes

E_R rms $\approx 0.13 \sqrt{RB}$
E_R rms in μV
R in MΩ
B in Hz

For the circuit in Figure 4

$R_2 = 10^7\Omega = 10M\Omega$

$$B = \frac{\pi}{2}(f_2) = \frac{\pi}{2} 15.9k$$

Then

$$E_R \text{ rms} = (411nV/\sqrt{Hz}) \sqrt{B}$$

$$= (411nV/\sqrt{Hz}) \sqrt{\frac{\pi}{2} 15.9kHz}$$

$$= 64.9\mu V \text{ rms}$$

Total Noise

The total noise may now be computed from

$$E_{n\ total} = \sqrt{E_{n1}^2 + E_{n2}^2 + E_{n3}^2 + E_{n4}^2 + E_{nR}^2 + E_{ni}^2} \quad (16)$$

$$= \sqrt{0.267^2 + 0.21^2 + 15.1^2 + 158.5^2 + 64.9^2 + 16.9^2} \quad (16a)$$

$$= \sqrt{0.07 + 0.04 + 228 + 25122 + 4212 + 286} \quad (16b)$$

$$= 173\mu V \text{ rms}$$

Conclusions

Examination of the results in equation (16b) together with the curves in Figure 8 leads to some interesting conclusions. In this example 84% of the noise comes from E_{n4}. From Figure 8 it is seen that this is the area beyond the pole formed by R_2 and C_2.

The E_{n4} contribution could be reduced several ways. The most common method is to increase C_2. This reduces f_2 and the value of $K2(1 + C1/C2)$ (see Figure 8). It also reduces the signal bandwidth (see Figure 6) and the final value of C_2 is normally a compromise between noise gain and necessary signal bandwidth.

It should be noted that increasing C_2 will also affect f_a since f_a is determined by $(C_1 + C_2)$ (see equation (5b)). Normally C_2 is larger than C_1 and f_2 will change more than for a given change in C_2.

The other means of reducing the noise in region 4 involves changing amplifier parameters. For example, the use of a slower amplifier would move the open-loop gain curve to the left and decrease f_3. Of course, reducing the value of K_2, the noise floor, would also reduce the noise in this region.

The second largest component is the resistor noise E_{nR} (14% of the total noise). A lower resistor value decreases resistor noise as a function of $\sqrt{R}$, but it also lowers the desired signal gain as a direct function of R. Thus, lowering R reduces the signal-to-noise ratio at the output which shows that the feedback resistor should be as large as possible. The noise contribution due to R_2 can be decreased by raising the value of C_2 (lowering f_2) but this reduces signal bandwidth.

It is interesting to note that the current noise of the amplifier accounted for only 1% of the total E_n. This is different than would be expected when comparing the current and voltage spectral densities with the size of the feedback resistor. For example, if we define a characteristic value of resistance as

$$R_{characteristic} = \frac{e_n(\omega)}{i_n(\omega)} \text{ at } f = 10kHz \quad (17)$$

$$= \frac{8nV/\sqrt{Hz}}{1.4fA/\sqrt{Hz}}$$

$$= 5.7M\Omega$$

Thus, in simple transimpedance circuits with feedback resistors greater than the characteristic value, the amplifier's current noise would cause more output noise than the amplifier's voltage noise. Based on this and the 10MΩ feedback resistor in the example, the amplifier noise current would be expected to have a higher contribution than the noise voltage. The reason it does not in the example of Figure 4 is that the noise voltage has high gain at higher frequencies (Figure 7) and the noise current does not (Figure 6).

The fourth largest component of total noise comes from E_{n3} (0.8%). Decreasing C_1 will also lower the term $K_2(1 + C_1/C_2)$. In this case, f_2 will stay fixed and f_a will move to the right (i.e., the +20dB/decade slope segment will move

to the right). This can have a significant reduction on noise without lowering the signal bandwidth. This points out the importance of maintaining low capacitance at the amplifier's input in low noise applications.

Shielding and Guarding

The low noise, low bias current and high input impedance of the OPA101/102 are well suited to a number of precision applications. In order to fully benefit from the outstanding specifications of this unit, careful layout, shielding, and guarding are required. Careless signal wiring or printed circuit board layout can easily degrade circuit performance several orders of magnitude below the capability of the OPA101/102.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry. The metal case of the OPA101/102 is connected to pin 8 and is not connected to any internal amplifier circuitry. Thus it is possible to use the case as a shield to reduce noise pickup.

Unless care is used, leakage currents across printed circuit boards can easily exceed the bias current of the OPA101/102. To avoid leakage problems, it is recommended that a Teflon IC socket be used or that at least the signal input lead of the amplifier be wired to a Teflon standoff. If this is not done and instead the OPA101/102 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 10). The amplifier case, pin 8, should also be connected to the guard. This insures that the entire amplifier circuitry is fully surrounded by the guard potential. This minimizes the voltage placed across any leakage paths and thus reduces leakage currents. In addition, noise pickup is also reduced.

Figures 11, 12, and 13 show typical applications using the guard and case shielding.

Cleanliness is also a prime concern in low bias current circuits. It is recommended that after installation is complete the assembly be washed with a low residue solvent such as TMC Freon followed by rinsing with deionized water. The use of some form of high dielectric conformal coating such as a good two-part urathane should be considered if the assembly will be used in air environment which could deposit contaminants on the low current circuitry.

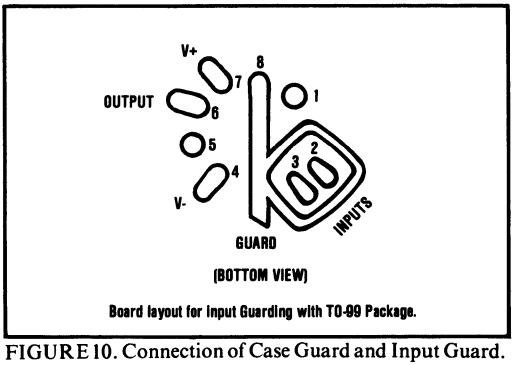


FIGURE 10. Connection of Case Guard and Input Guard.

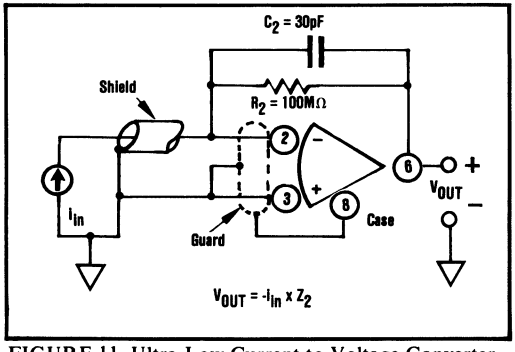


FIGURE 11. Ultra-Low Current to Voltage Converter.

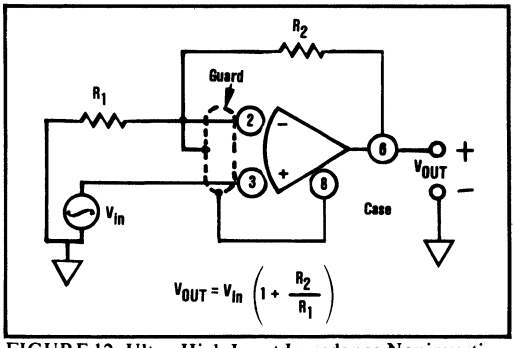


FIGURE 12. Ultra-High Input Impedance Noninverting Circuit.

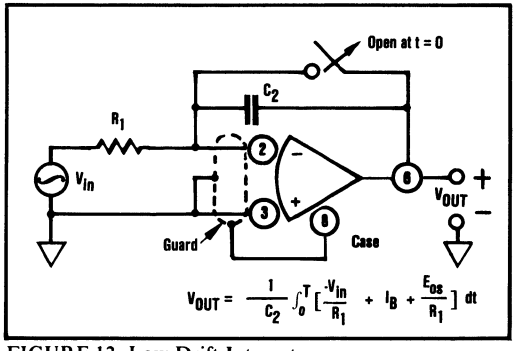


FIGURE 13. Low Drift Integrator.

Thermal Model

Figure 14 is the thermal model for the OPA101/102 where:

T_J = Junction temperature (output load)
T_J* = Junction temperature (no load)
T_C = Case temperature
T_A = Ambient temperature
θ_{CA} = Thermal resistance, case-to-ambient

θ_{HS} = Effective thermal resistance of the heat sink
P_{DQ} = Quiescent power dissipation
$|+V_{CC}| I_{+QUIESCENT} + |-V_{CC}| I_{-QUIESCENT}$
P_{DX} = Power dissipation in the output transistor
$= (V_{OUT} - V_{CC}) I_{OUT}$

(In a complementary output stage only one output transistor is conducting current at a time.)

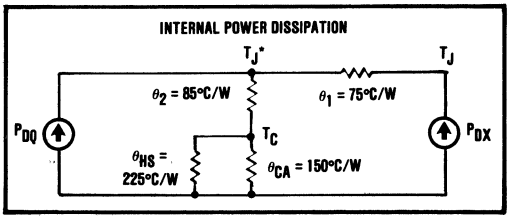


FIGURE 14. OPA101/102 Thermal Model

This model is obviously not the simple one-power source model used with most linear integrated circuits. It is, however, a more accurate model for multichip hybrid integrated circuits where the quiescent power is dissipated in the input stage and the internal power dissipation due to the load is dissipated in a somewhat physically separated output stage.

The model in Figure 14 must be used in conjunction with the OPA101/102's absolute maximum ratings of internal power dissipation and junction temperature to determine the derated power dissipation capability of the package.

As an example of how to use this model, consider this problem: Determine the output transistor junction temperature when the output has its maximum load resistance and is operated at the worst-case output voltage conditions. Assume $V_{CC} = \pm 15$VDC and $T_A = 25°C$.

Maximum P_{DX} occurs where $V_{OUT} = 1/2 V_{CC}$. Then

$$P_{DX\ max} = \frac{(V_{CC})^2}{4R_{load}} \qquad (18)$$

$$T_J = T_A + P_{DQ}[\theta_2 + (\theta_{HS} \parallel \theta_{CA})] + P_{DX}[\theta_1 + \theta_2 + (\theta_{HS} \parallel \theta_{CA})] \qquad (19)$$

where $(\theta_{HS} \parallel \theta_{CA}) = \dfrac{\theta_{HS}\theta_{CA}}{\theta_{HS} + \theta_{CA}} = 90°C/W$

Substituting appropriate values yields

$$T_J = 25° + (30V \times 8mA)[85°C/W + 90°C/W] + \frac{(15V)^2}{4 \times 1k\Omega}[75°C/W + 85°C/W + 90°C/W]$$

$$= 25°C + 42°C + 14°C = T_A + 56°C$$

$$= 81°C$$

The conclusion is that under a worst-case output voltage condition and with a 1kΩ load the junction temperature rise is 56°C above ambient. Thus, under these conditions, the device could be operated in an ambient up to 119°C without exceeding the 175°C junction temperature rating.

A similar analysis for conditions of the output short-circuited to ground where

$$P_{DX\ SS} = V_{CC} I_{(output\ limit)} \qquad (20)$$

shows that the maximum junction temperature rating of 175°C is exceeded. Thus, the output should not be shorted to ground for sustained periods of time.

HEAT SINK

The heat sink used on the OPA101/102 should not be removed. It has the effect of reducing the package thermal resistance from 150°C/W to about 90°C per watt. Removing the heat sink would naturally increase the junction temperature of the amplifier which would in turn raise the input bias current. The change in thermal resistance also affects the noise performance. Removing the heat sink would increase the noise in the 1/f region.

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Low Noise Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 100% tested, 8nV/$\sqrt{Hz}$ max at 10kHz
- LOW BIAS CURRENT: 1pA max
- LOW OFFSET: 250μV max
- LOW DRIFT: 1μV/°C max
- HIGH OPEN-LOOP GAIN: 120dB min
- HIGH COMMON-MODE REJECTION: 100dB min

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- OPTOELECTRONICS
- MEDICAL EQUIPMENT—CAT SCANNER
- RADIATION HARD EQUIPMENT

DESCRIPTION

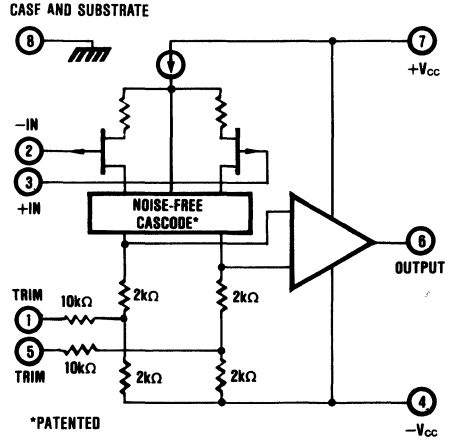
The OPA111 is a precision monolithic dielectrically-isolated FET (*Difet*®) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very-low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very-low offset and drift. Extremely-low noise is achieved with new circuit design techniques (patented). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.



OPA111 SIMPLIFIED CIRCUIT

BIFET®National Semiconductor Corp., *Difet*® Burr-Brown Corp.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-526G

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITIONS	OPA111AM			OPA111BM			OPA111SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
NOISE											
Voltage, f_o = 10Hz	100% tested		40	80		30	60		40	80	nV/√Hz
f_o = 100Hz	100% tested		15	40		11	30		15	40	nV/√Hz
f_o = 1kHz	100% tested		8	15		7	12		8	15	nV/√Hz
f_o = 10kHz	100% tested		6	8		6	8		6	8	nV/√Hz
f_B = 10Hz to 10kHz	100% tested		0.7	1 2		0 6	1.0		0.7	1 2	µV, rms
f_B = 0 1Hz to 10Hz	(1)		1 6	3 3		1 2	2 5		1 6	3.3	µV, p-p
Current, f_B = 0 1Hz to 10Hz	(1)		9 5	15		7 5	12		9 5	15	fA, p-p
f_o = 0 1Hz thru 20kHz	(1)		0 5	0 8		0 4	0 6		0 5	0 8	fA/√Hz
OFFSET VOLTAGE[2]											
Input Offset Voltage	V_{cm} = 0VDC		±100	±500		±50	±250		±100	±500	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±2	±5		±0 5	±1		±2	±5	µV/°C
Supply Rejection	V_{CC} = ±10V to ±18V	90	110		100	110		90	110		dB
			±3	±31		±3	±10		±3	±31	µV/V
BIAS CURRENT[2]											
Input Bias Current	V_{cm} = 0VDC		±0 8	±2		±0 5	±1		±0 8	±2	pA
OFFSET CURRENT[2]											
Input Offset Current	V_{cm} = 0VDC		±0 5	±1 5		±0 25	±0 75		±0.5	±1 5	pA
IMPEDANCE											
Differential			10^{13} ‖ 1			10^{13} ‖ 1			10^{13} ‖ 1		Ω ‖ pF
Common-Mode			10^{14} ‖ 3			10^{14} ‖ 3			10^{14} ‖ 3		Ω ‖ pF
VOLTAGE RANGE											
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	90	110		100	110		90	110		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	114	125		120	125		114	125		dB
FREQUENCY RESPONSE											
Unity Gain, Small Signal			2			2			2		MHz
Full Power Response	20V p-p, R_L = 2k	16	32		16	32		16	32		kHz
Slew Rate	V_o = ±10V, R_L = 2k	1	2		1	2		1	2		V/µsec
Settling Time, 0 1%	Gain = −1, R_L = 2k		6			6			6		µsec
0 01%	10V step		10			10			10		µsec
Overload Recovery, 50% Overdrive[3]	Gain = −1		5			5			5		µsec
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11	±12		±11	±12		±11	±12		V
Current Output	V_o = ±10VDC	±5 5	±10		±5 5	±10		±5 5	±10		mA
Output Resistance	DC, open loop		100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000		pF
Short Circuit Current		10	40		10	40		10	40		mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_o = 0mADC		2 5	3 5		2.5	3 5		2.5	3 5	mA
TEMPERATURE RANGE											
Specification	Ambient temp	−25		+85	−25		+85	−55		+125	°C
Operating	Ambient temp	−55		+125	−55		+125	−55		+125	°C
Storage	Ambient temp	−65		+150	−65		+150	−65		+150	°C
θ Junction-Ambient			200			200			200		°C/W

NOTES. (1) Sample tested—this parameter is guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.

ELECTRICAL [FULL TEMPERATURE RANGE SPECIFICATIONS]

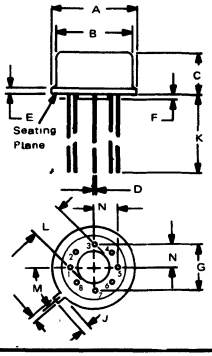
At V_{CC} = ±15VDC and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA111AM			OPA111BM			OPA111SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification Range	Ambient temp	−25		+85	−25		+85	−55		+125	°C
INPUT											
OFFSET VOLTAGE[1]											
Input Offset Voltage	V_{cm} = 0VDC		±220	±1000		±110	±500		±300	±1500	µV
Average Drift			±2	±5		±0.5	±1		±2	±5	µV/°C
Supply Rejection	V_{CC} = ±10V to ±18V	86	100		90	100		86	100		dB
			±10	±50		±10	±32		±10	±50	µV/V
BIAS CURRENT[1]											
Input Bias Current	V_{cm} = 0VDC		±50	±250		±30	±130		±820	±4100	pA
OFFSET CURRENT[1]											
Input Offset Current	V_{cm} = 0VDC		±30	±200		±15	±100		±510	±3100	pA
VOLTAGE RANGE											
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	86	100		90	100		86	100		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 2kΩ	110	120		114	120		110	120		dB
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±10.5	±11		±11	±11.5		±11	±11.5		V
Current Output	V_o = ±10VDC	±5.25	±10		±5.25	±10		±5.25	±10		mA
Short Circuit Current	V_o = 0VDC	10	40		10	40		10	40		mA
POWER SUPPLY											
Current, Quiescent	I_o = 0mADC		2.5	3.5		2.5	3.5		2.5	3.5	mA

NOTES (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

MECHANICAL "M" PACKAGE TO-99 (Hermetic)

NOTE
Leads in true position within .010" (.25mmR) at MMC at seating plane

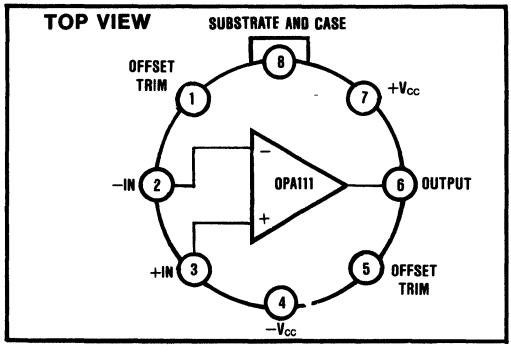


Pin numbers shown for reference only. Numbers may not be marked on package

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	335	370	8.51	9.40
B	305	335	7.75	8.51
C	165	185	4.19	4.70
D	016	021	0.41	0.53
E	010	040	0.25	1.02
F	010	040	0.25	1.02
G	200 BASIC		5.08 BASIC	
H	028	034	0.71	0.86
J	029	045	0.74	1.14
K	500	—	12.7	—
L	110	160	2.79	4.06
M	45° BASIC		45° BASIC	
N	095	105	2.41	2.67

CONNECTION DIAGRAM



ORDERING INFORMATION

Model	Package	Temperature Range	Offset Voltage, max (µV)
OPA111AM	TO-99	−25°C to +85°C	±500
OPA111BM	TO-99	−25°C to +85°C	±250
OPA111SM	TO-99	−55°C to +125°C	±500
BURN-IN SCREENING OPTION			
Model	**Package**	**Temperature Range**	**Burn-In Temp. (160h)**[1]
OPA111AM-BI	TO-99	−25°C to +85°C	+125°C
OPA111BM-BI	TO-99	−25°C to +85°C	+125°C
OPA111SM-BI	TO-99	−25°C to +85°C	+125°C

NOTE: (1) Or equivalent combination of time and temperature.

ABSOLUTE MAXIMUM RATINGS

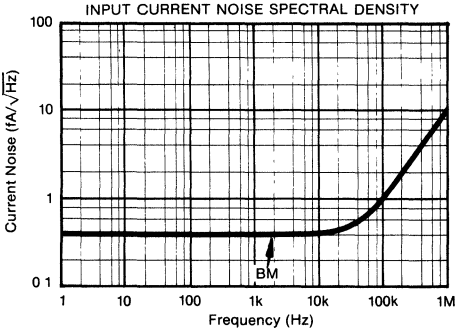
Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage[2]	±36VDC
Input Voltage Range[2]	±18VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[3]	Continuous
Junction Temperature	+175°C

NOTES
(1) Packages must be derated based on $\theta_{JC} = 150°C/W$ or $\theta_{JA} = 300°C/W$
(2) For supply voltages less than ±18VDC the absolute maximum input voltage is equal to $+18V > V_{IN} > -V_{CC} - 6V$. See Figure 2
(3) Short circuit may be to power supply common only Rating applies to +25°C ambient Observe dissipation limit and T_J

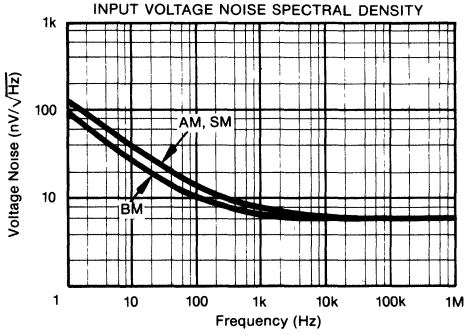
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_{CC} = \pm 15VDC$ unless otherwise noted.

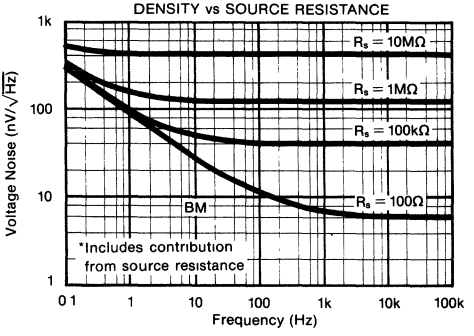
INPUT CURRENT NOISE SPECTRAL DENSITY



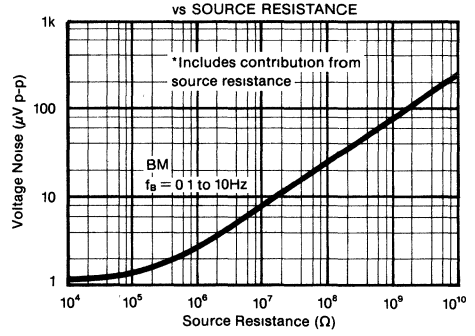
INPUT VOLTAGE NOISE SPECTRAL DENSITY



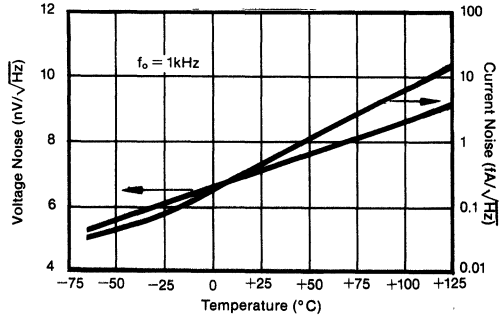
TOTAL* INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



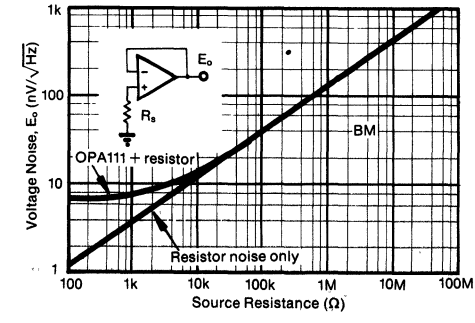
TOTAL* INPUT VOLTAGE NOISE (PEAK-TO-PEAK) vs SOURCE RESISTANCE



VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



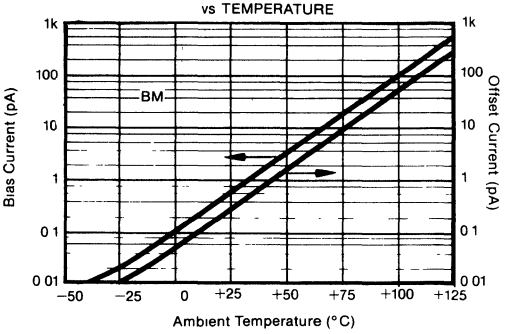
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



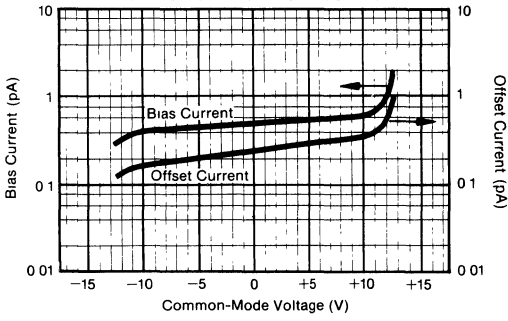
TYPICAL PERFORMANCE CURVES [CONT]

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

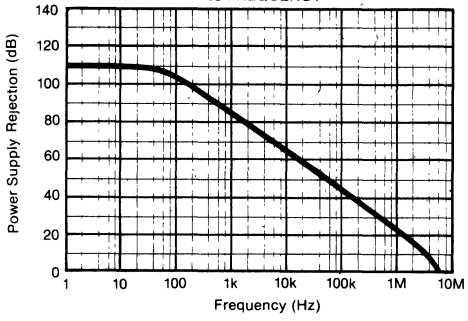
BIAS AND OFFSET CURRENT vs TEMPERATURE



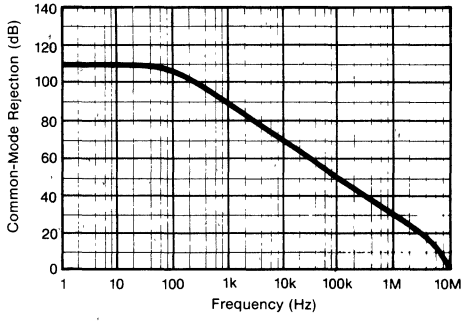
BIAS AND OFFSET CURRENT vs INPUT COMMON MODE VOLTAGE



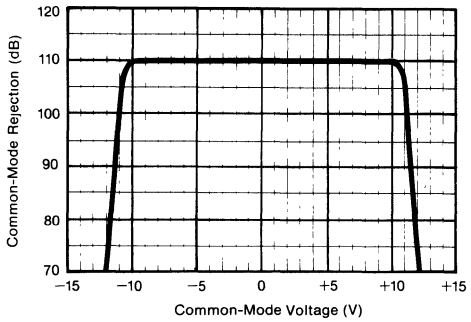
POWER SUPPLY REJECTION vs FREQUENCY



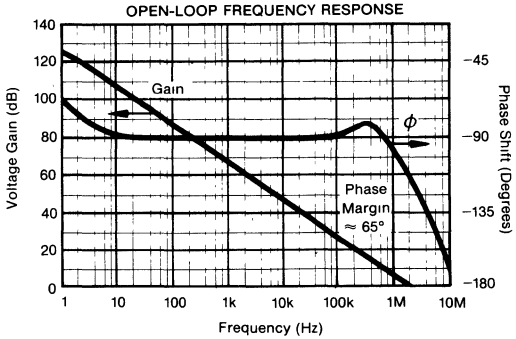
COMMON-MODE REJECTION vs FREQUENCY



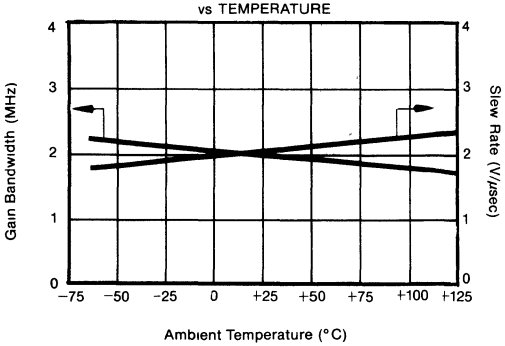
COMMON-MODE REJECTION vs INPUT COMMON MODE VOLTAGE



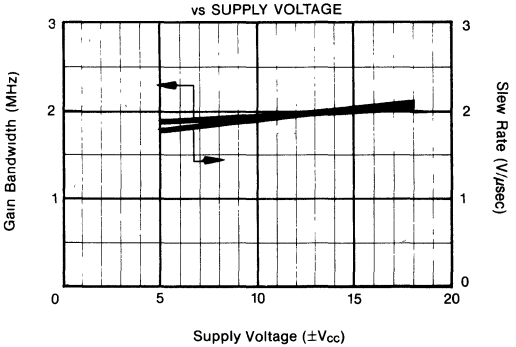
OPEN-LOOP FREQUENCY RESPONSE



GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



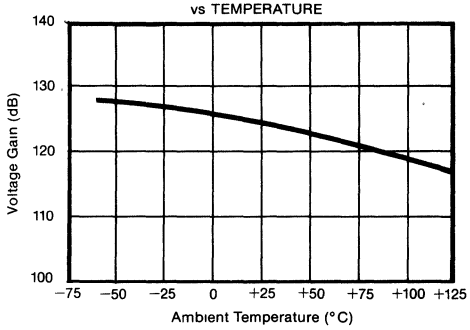
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



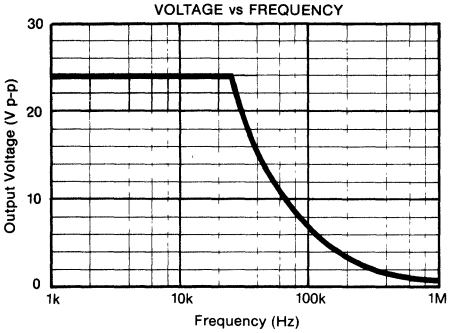
TYPICAL PERFORMANCE CURVES [CONT]

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted

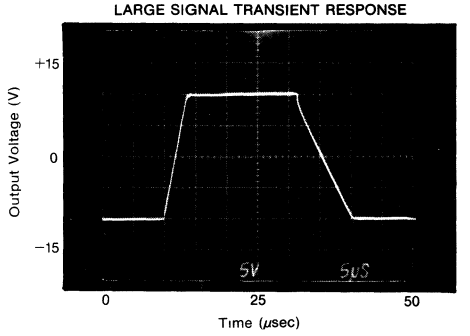
OPEN-LOOP GAIN vs TEMPERATURE



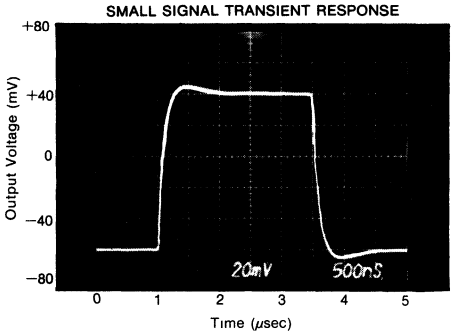
MAXIMUM UNDISTORTED OUTPUT VOLTAGE vs FREQUENCY



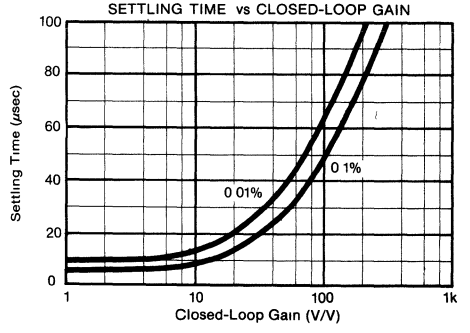
LARGE SIGNAL TRANSIENT RESPONSE



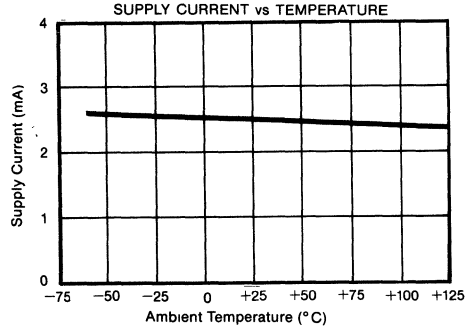
SMALL SIGNAL TRANSIENT RESPONSE



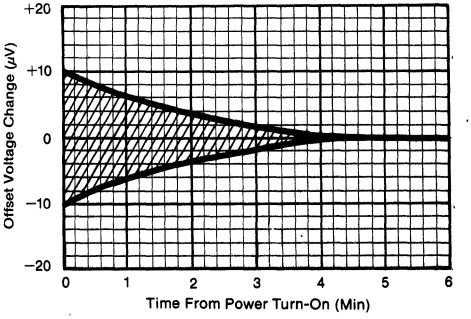
SETTLING TIME vs CLOSED-LOOP GAIN



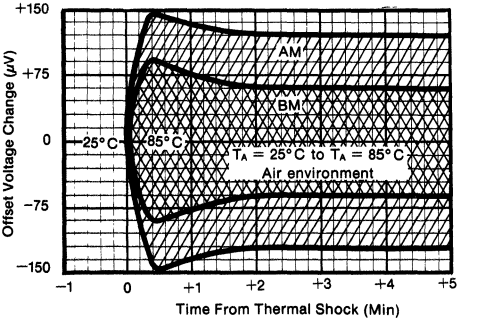
SUPPLY CURRENT vs TEMPERATURE



INPUT OFFSET VOLTAGE WARM-UP DRIFT



INPUT OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA111 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.3μV/°C for each 100μV of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as 741 and AD547. The OPA111 can replace most other amplifiers by leaving the external null circuit unconnected.

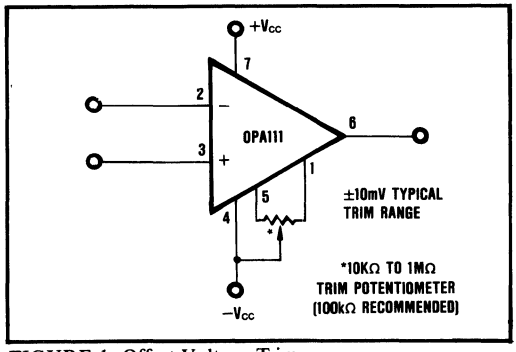


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Unlike BIFET amplifiers, the ***Difet*** OPA111 requires input current limiting resistors only if its input voltage is greater than 6 volts more negative than $=V_{CC}$. A 10kΩ series resistor will limit input current to a safe level with up to ±15V input levels even if both supply voltages are lost.

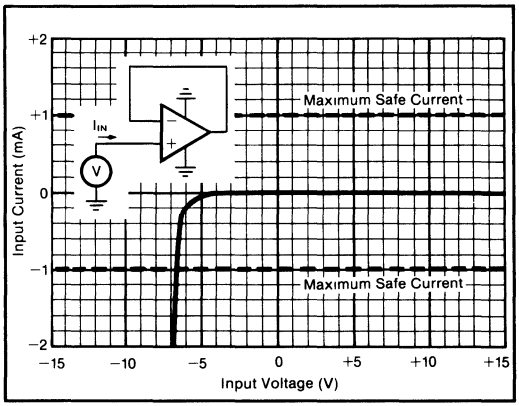


FIGURE 2. Input Current vs Input Voltage with ±V_{CC} Pins Grounded.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is rquired to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias curent of the OPA111. To avoid leakage problems, it is recommended that the signal input lead of the OPA111 be wired to a Teflon standoff. If the OPA111 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 3).

If guarding is not required, pin 8 (case) should be connected to ground.

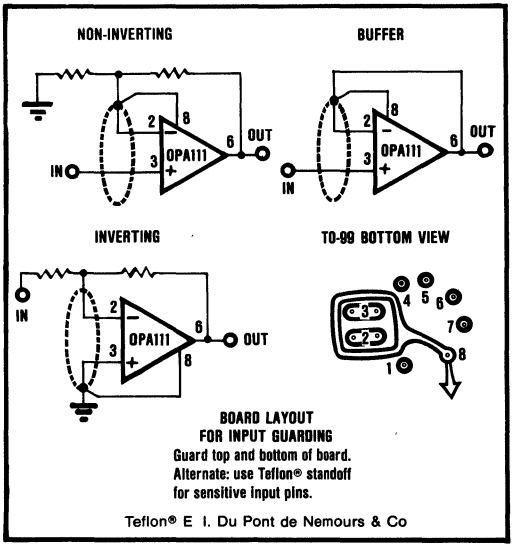


FIGURE 3. Connection of Input Guard.

NOISE: FET VERSUS BIPOLAR

Low noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar

operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ the OPA111 will have lower total noise than an OP-27 (see Figure 4).

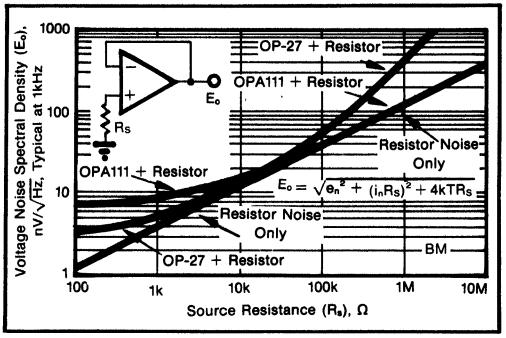


FIGURE 4. Voltage Noise Spectral Density Versus Source Resistance.

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET operational amplifiers are affected by common-mode voltage (Figure 5). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely-low bias current of the OPA111 is not compromised by common-mode voltage.

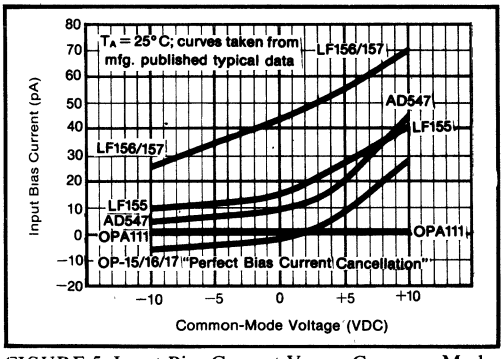


FIGURE 5. Input Bias Current Versus Common-Mode Voltage.

BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information table. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

APPLICATIONS CIRCUITS

Figures 6 through 18 are circuit diagrams of various applications for the OPA111.

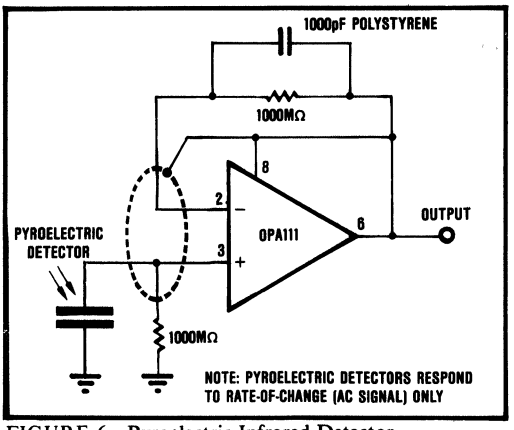


FIGURE 6. Pyroelectric Infrared Detector.

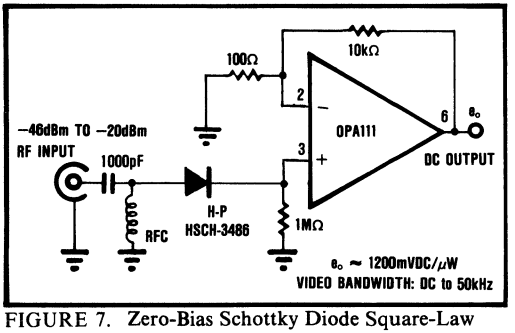


FIGURE 7. Zero-Bias Schottky Diode Square-Law RF Detector.

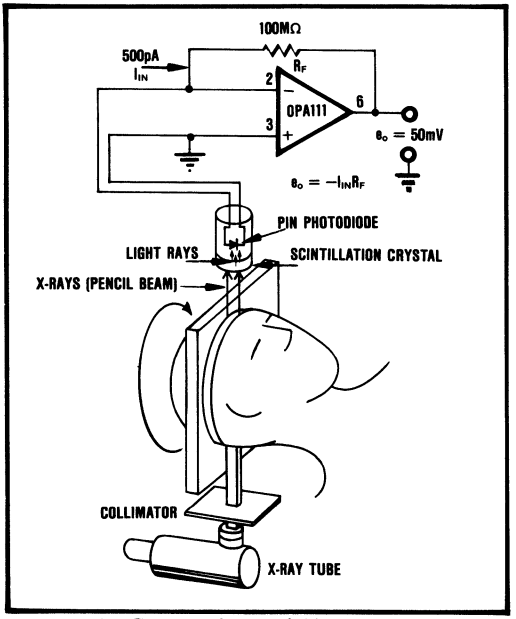


FIGURE 8. Computerized Axial Tomography (CAT) Scanner Channel Amplifier.

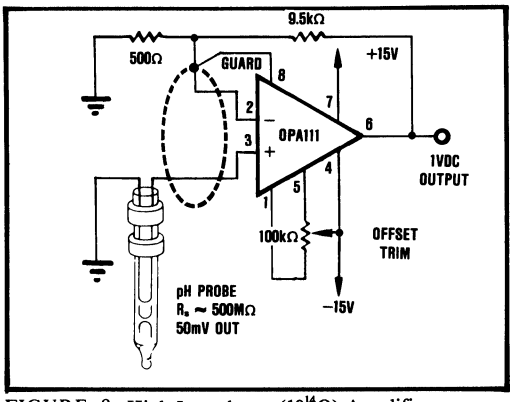


FIGURE 9. High Impedance ($10^{14}\Omega$) Amplifier.

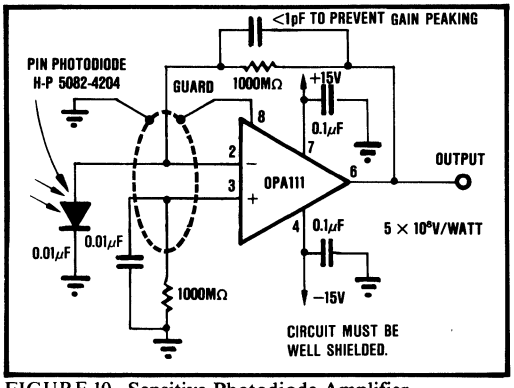


FIGURE 10. Sensitive Photodiode Amplifier.

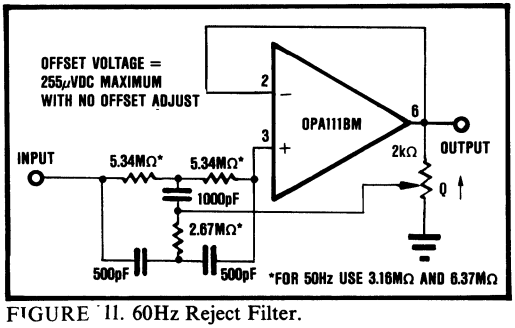


FIGURE 11. 60Hz Reject Filter.

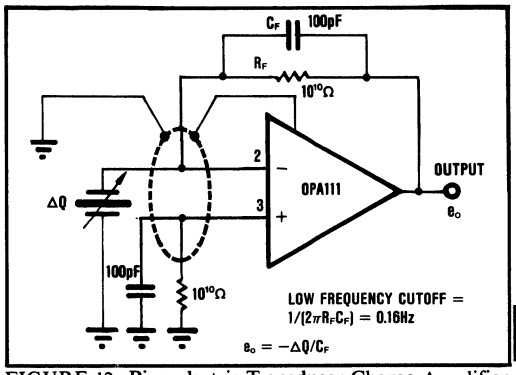


FIGURE 12. Piezoelectric Transducer Charge Amplifier.

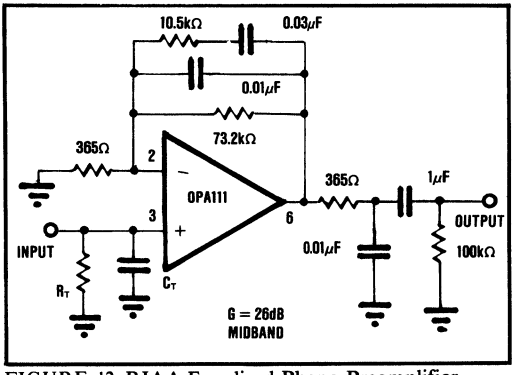


FIGURE 13. RIAA Equalized Phono Preamplifier.

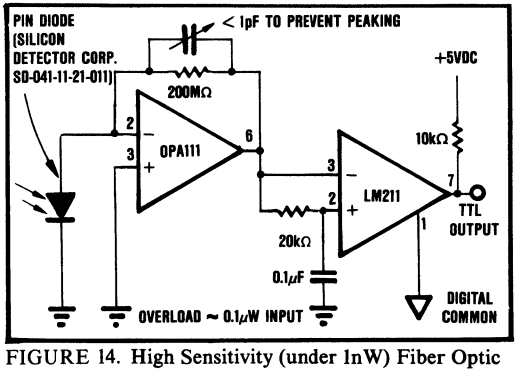


FIGURE 14. High Sensitivity (under 1nW) Fiber Optic Receiver for 9600 Baud Manchester Data.

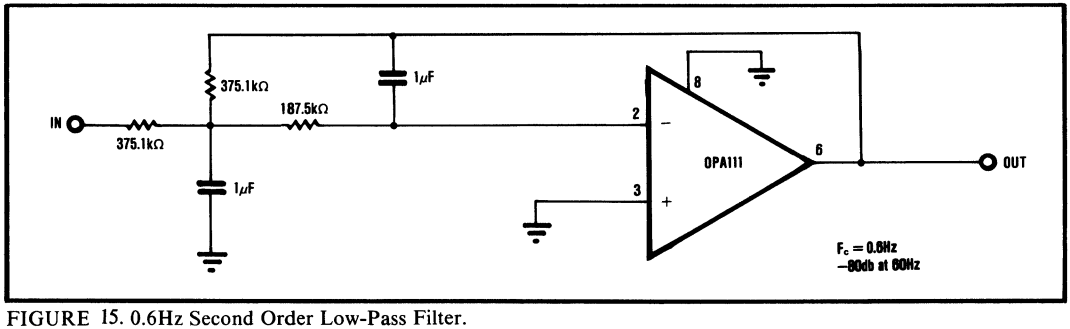


FIGURE 15. 0.6Hz Second Order Low-Pass Filter.

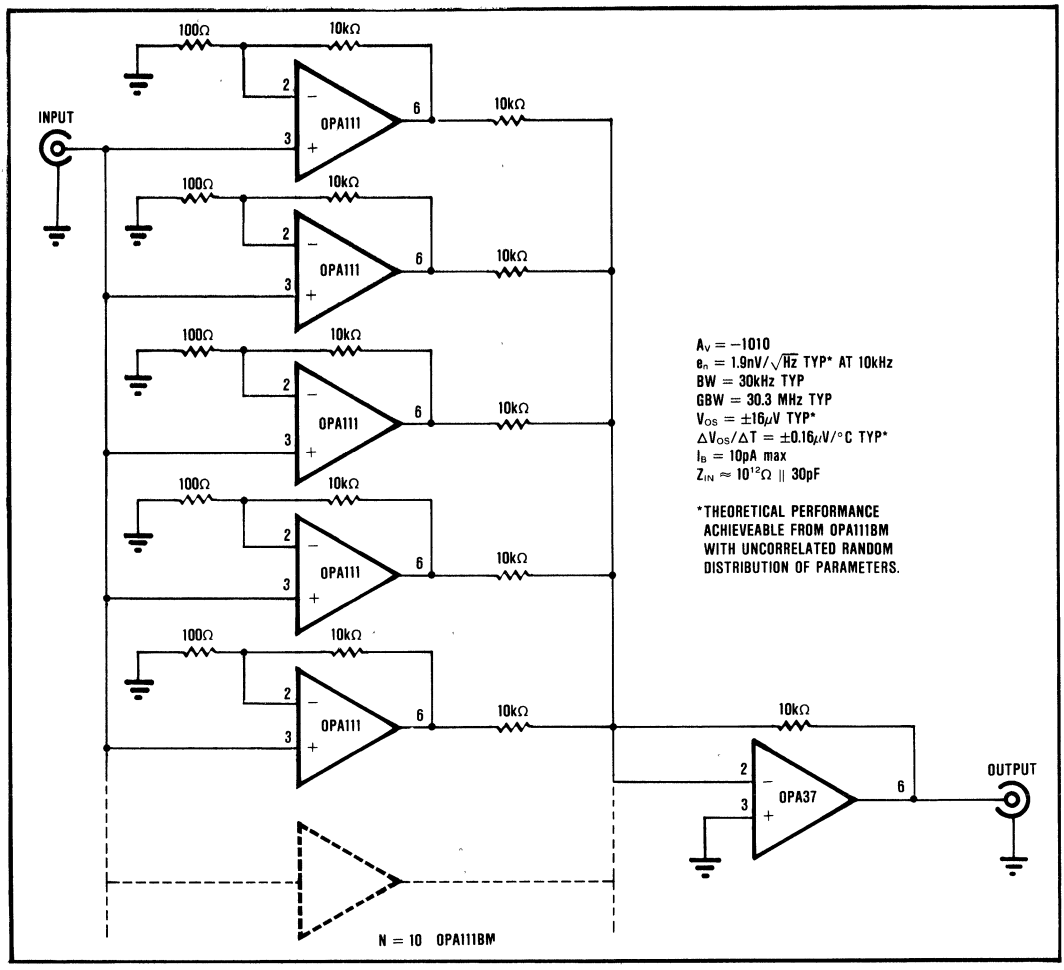


FIGURE 16. 'N' Stage Parallel-Input Amplifier For Reduced Relative Amplifier Noise At The Output.

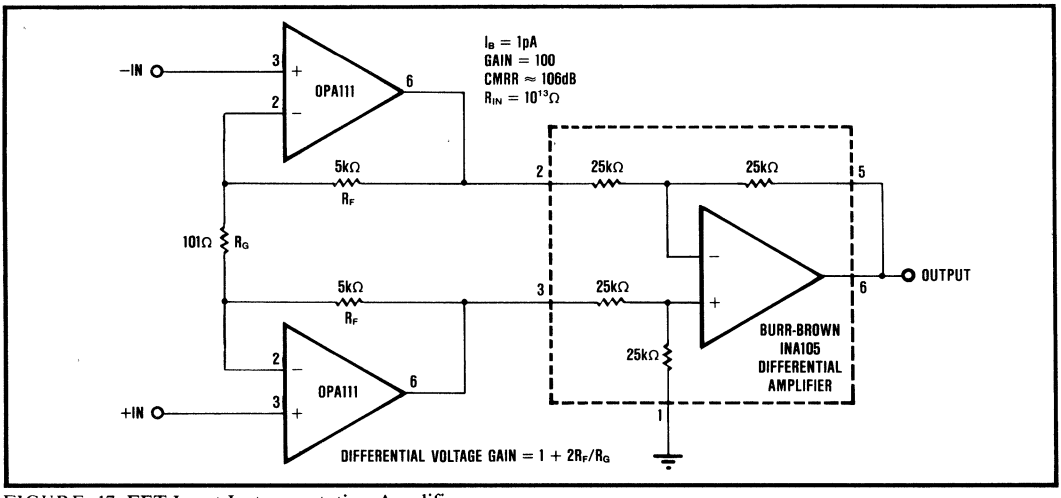


FIGURE 17. FET Input Instrumentation Amplifier.

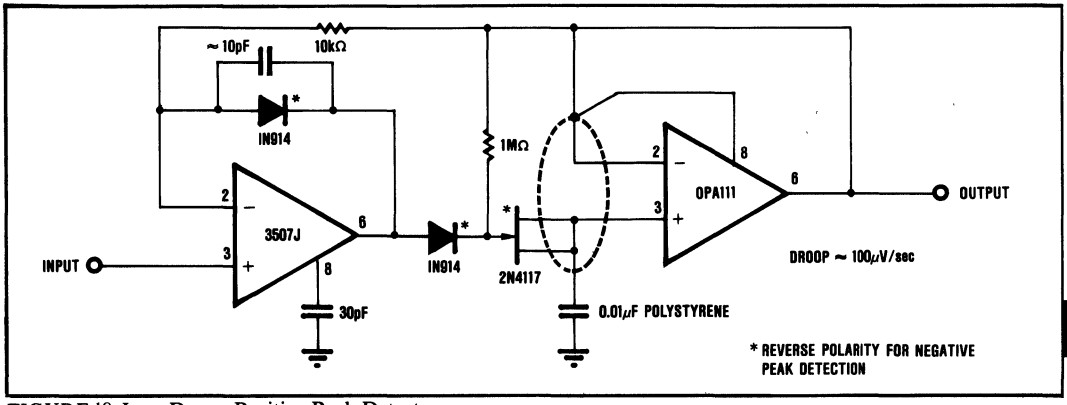
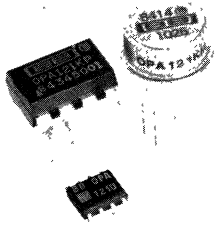


FIGURE 18. Low-Droop Positive Peak Detector.

BURR-BROWN®



OPA121

Low Cost Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 6nV/$\sqrt{Hz}$ typ at 10kHz
- LOW BIAS CURRENT: 5pA max
- LOW OFFSET: 2mV max
- LOW DRIFT: 3μV/°C typ
- HIGH OPEN-LOOP GAIN: 110dB min
- HIGH COMMON-MODE REJECTION: 86dB min

APPLICATIONS

- OPTOELECTRONICS
- DATA ACQUISITION
- TEST EQUIPMENT
- MEDICAL EQUIPMENT
- RADIATION HARD EQUIPMENT

DESCRIPTION

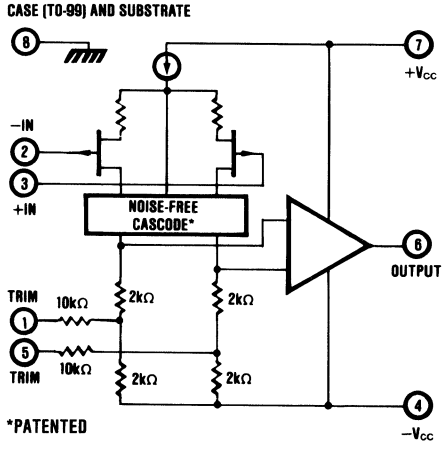
The OPA121 is a precision monolithic dielectrically-isolated FET (*Difet*®) operational amplifier. Outstanding performance characteristics are now available for low-cost applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very low bias current is obtained by dielectric isolation with on-chip guarding.

Laser-trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with new circuit design techniques (patented). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.



OPA121 SIMPLIFIED CIRCUIT

BIFET® National Semiconductor Corp., *Difet*® Burr-Brown Corp.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITIONS	OPA121KM			OPA121KP/KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
NOISE								
Voltage, f_O = 10Hz	[1]		40			50		nV/√Hz
f_O = 100Hz	[1]		15			18		nV/√Hz
f_O = 1kHz	[1]		8			10		nV/√Hz
f_O = 10kHz	[1]		6			7		nV/√Hz
f_B = 10Hz to 10kHz	[1]		0 7			0 8		μVrms
f_B = 0 1Hz to 10Hz	[1]		1.6			2		μVp-p
Current, f_B = 0 1Hz to 10Hz	[1]		15			21		fA, p-p
f_O = 0 1Hz thru 20kHz	[1]		0 8			1 1		fA/√Hz
OFFSET VOLTAGE[2]								
Input Offset Voltage	V_{CM} = 0VDC		±0.5	±2		±0.5	±3	mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3	±10		±3	±10	μV/°C
Supply Rejection		86	104		86	104		dB
			±6	±50		±6	±50	μV/V
BIAS CURRENT[2]								
Input Bias Current	V_{CM} = 0VDC Device Operating		±1	±5		±1	±10	pA
OFFSET CURRENT[2]								
Input Offset Current	V_{CM} = 0VDC Device Operating		±0 7	±4		±0 7	±8	pA
IMPEDANCE								
Differential			10^{13} ‖ 1			10^{13} ‖ 1		Ω ‖ pF
Common-Mode			10^{14} ‖ 3			10^{14} ‖ 3		Ω ‖ pF
VOLTAGE RANGE								
Common-Mode Input Range		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	86	104		82	100		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	110	120		106	114		dB
FREQUENCY RESPONSE								
Unity Gain, Small Signal			2			2		MHz
Full Power Response	20V p-p, R_L = 2kΩ		32			32		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ		2			2		V/μs
Settling Time, 0 1%	Gain = −1, R_L = 2kΩ		6			6		μs
0 01%	10V step		10			10		μs
Overload Recovery, 50% Overdrive[3]	Gain = −1		5			5		μs
RATED OUTPUT								
Voltage Output	R_L = 2kΩ	±11	±12		±11	±12		V
Current Output	V_O = ±10VDC	±5 5	±10		±5 5	±10		mA
Output Resistance	DC, open loop		100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000		pF
Short Circuit Current		10	40		10	40		mA
POWER SUPPLY								
Rated Voltage			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		2.5	4.0		2.5	4.5	mA
TEMPERATURE RANGE								
Specification	Ambient temp	0		+70	0		+70	°C
Operating	Ambient temp.	−40		+85	−25		+85	°C
Storage	Ambient temp.	−65		+150	−55		+125	°C
θ Junction-Ambient			200			150[4]		°C/W

NOTES (1) Sample tested (2) Offset voltage, offset current, and bias current are specified with the units fully warmed up (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive (4) 100°C/W for KU grade

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

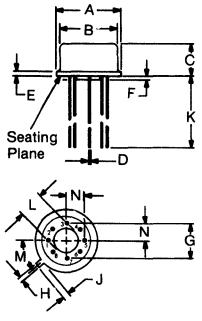
At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted

PARAMETER	CONDITIONS	OPA121KM MIN	OPA121KM TYP	OPA121KM MAX	OPA121KP/KU MIN	OPA121KP/KU TYP	OPA121KP/KU MAX	UNITS
TEMPERATURE RANGE								
Specification Range	Ambient temp	0		+70	0		+70	°C
INPUT								
OFFSET VOLTAGE[1]								
Input Offset Voltage	V_{CM} = 0VDC		±1	±3		±1	±5	mV
Average Drift			±3	±10		±3	±10	µV/°C
Supply Rejection		82	94		82	94		dB
			±20	±80		±20	±80	µV/V
BIAS CURRENT[1]								
Input Bias Current	V_{CM} = 0VDC, Device operating		±23	±115		±23	±250	pA
OFFSET CURRENT[1]								
Input Offset Current	V_{CM} = 0VDC, Device operating		±16	±100		±16	±200	pA
VOLTAGE RANGE								
Common-Mode Input Range		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	82	98		80	96		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	106	116		100	110		dB
RATED OUTPUT								
Voltage Output	R_L = 2kΩ	±10 5	±11		±10 5	±11		V
Current Output	V_O = ±10VDC	±5 25	±10		±5 25	±10		mA
Short Circuit Current	V_O = 0VDC	10	40		10	40		mA
POWER SUPPLY								
Current, Quiescent	I_O = 0mADC		2 5	4 5		2 5	5 0	mA

NOTES (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up

MECHANICAL

"M" PACKAGE TO-99 (Hermetic)



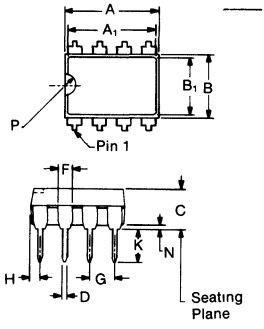
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	335	370	8 51	9 40
B	305	335	7 75	8 51
C	165	185	4 19	4 70
D	016	021	0 41	0 53
E	010	040	0 25	1 02
F	010	040	0 25	1 02
G	200 BASIC		5 08 BASIC	
H	028	034	0 71	0 86
J	029	045	0 74	1 14
K	500	—	12 7	—
L	110	160	2 79	4 06
M	45° BASIC		45° BASIC	
N	095	105	2 41	2 67

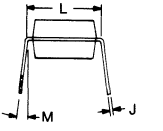
NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

Pin numbers shown for reference only Numbers may not be marked on package

"P" PACKAGE 8-Pin Plastic

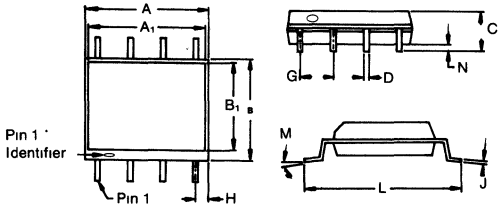




DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	355	400	9 03	10 16
A_1	340	384	8 64	9 78
B	230	290	5.85	7 37
B_1	200	250	5 09	6 36
C	120	200	3 05	5.09
D	015	023	0 38	0 59
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	025	050	0 64	1 27
J	008	015	0 20	0 38
K	070	150	1 78	3 82
L	300 BASIC		7 63 BASIC	
M	0°	15°	0°	15°
N	010	030	0 25	0 76
P	025	050	0 64	1 27

NOTE Leads in true position within 010" (25mm) R at MMC at seating plane

"U" PACKAGE Plastic SOIC

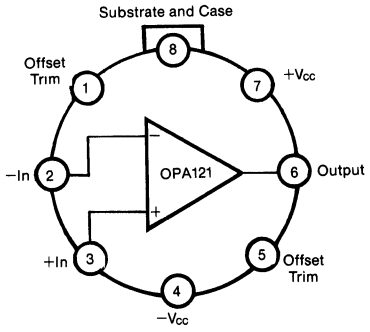


NOTE· Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	185	201	4 70	5 11
A_1	178	201	4 52	5 11
B	146	162	3 71	4 11
B_1	130	149	3 30	3 78
C	054	145	1 37	3 69
D	015	019	0 38	0 48
G	050 BASIC		1 27 BASIC	
H	018	026	0 46	0 66
J	008	012	0 20	0 30
L	220	252	5 59	6 40
M	0°	10°	0°	10°
N	000	012	0 00	0 30

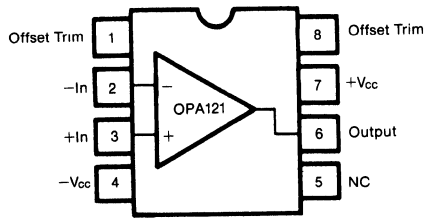
CONNECTION DIAGRAMS

"M" PACKAGE TO-99 (Hermetic)



TOP VIEW

"P" PACKAGE Plastic Mini-DIP
"U" PACKAGE Plastic SOIC



TOP VIEW

ORDERING INFORMATION

Model	Package	Temperature Range	
OPA121KM	TO-99	0°C to +70°C	
OPA121KP	Plastic	0°C to +70°C	
OPA121KU	SOIC	0°C to +70°C	

BURN-IN SCREENING OPTION

Model	Package	Temperature Range	Burn-In Temp. (160h)[1]
OPA121KM-BI	TO-99	0°C to +70°C	+85°C
OPA121KP-BI	Plastic	0°C to +70°C	+85°C
OPA121KU-BI	SOIC	0°C to +70°C	+85°C

NOTE (1) Or equivalent combination of time and temperature.

ABSOLUTE MAXIMUM RATINGS

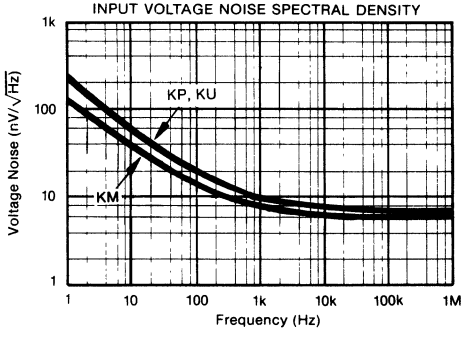
Supply ..... ±18VDC
Internal Power Dissipation[1] 500mW
Differential Input Voltage ..... ±36VDC
Input Voltage Range ..... ±18VDC
Storage Temperature Range
M package ..... −65°C to +150°C
P, U packages ..... −55°C to +125°C
Operating Temperature Range
M package ..... −40°C to +85°C
P, U packages ..... −25°C to +85°C
Lead Temperature
M, P packages (soldering 10 seconds) ..... +300°C
U package (soldering 3 seconds) ..... +260°C
Output Short-Circuit Duration[2] ..... Continuous
Junction Temperature ..... +175°C

NOTES (1) Packages must be derated based on θ_{JA} = 150°C/W (P package), θ_{JA} = 200°C/W (M package), θ_{JA} = 100°C/W (U package) (2) Short circuit may be to power supply common only Rating applies to +25°C ambient Observe dissipation limit and T_J

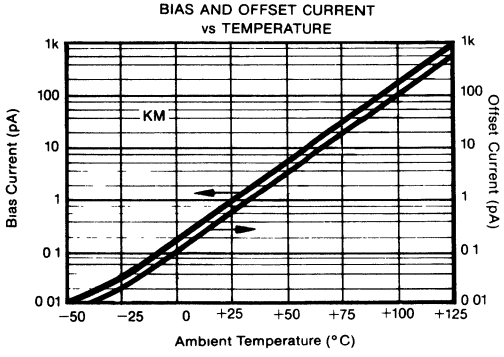
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted

INPUT VOLTAGE NOISE SPECTRAL DENSITY



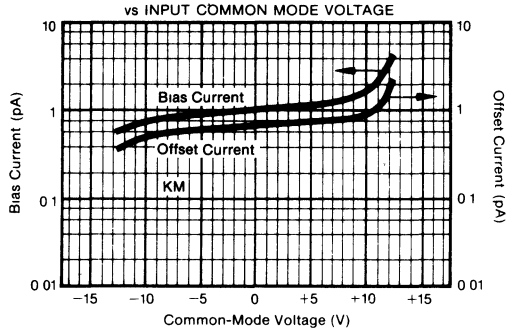
BIAS AND OFFSET CURRENT vs TEMPERATURE



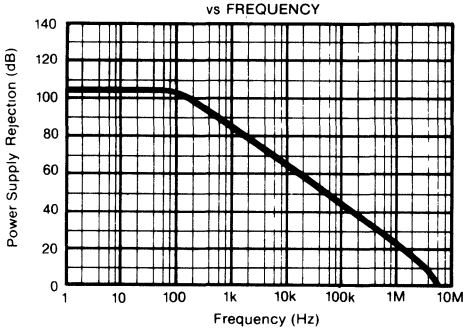
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted

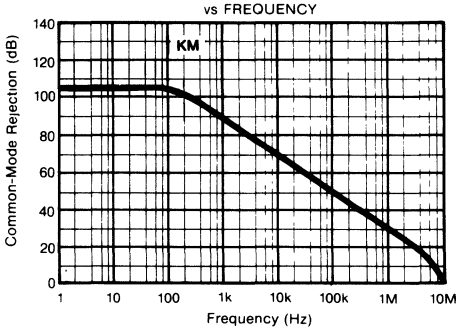
BIAS AND OFFSET CURRENT vs INPUT COMMON MODE VOLTAGE



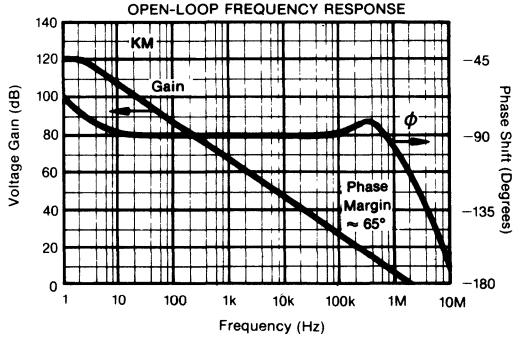
POWER SUPPLY REJECTION vs FREQUENCY



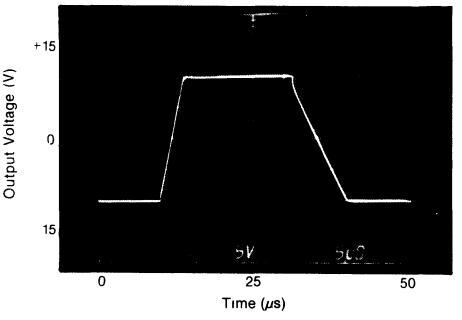
COMMON-MODE REJECTION vs FREQUENCY



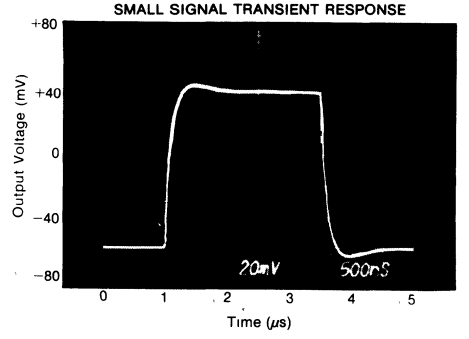
OPEN-LOOP FREQUENCY RESPONSE



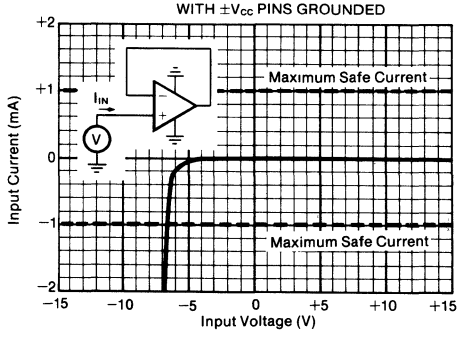
LARGE SIGNAL TRANSIENT RESPONSE



SMALL SIGNAL TRANSIENT RESPONSE



INPUT CURRENT VS INPUT VOLTAGE WITH ±V_{CC} PINS GROUNDED



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA121 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.3μV/°C for each 100μV of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as 741 and AD547. The OPA121 can replace most BIFET amplifiers by leaving the external null circuit unconnected.

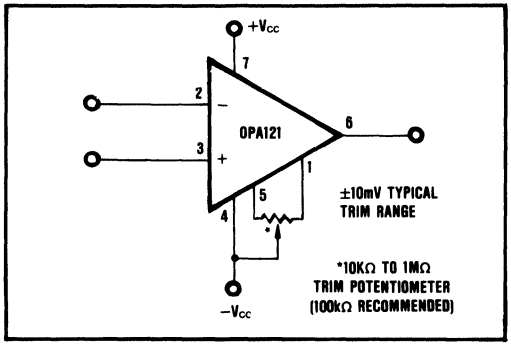


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Unlike BIFET amplifiers, the ***Difet*** OPA121 requires input current limiting resistors only if its input voltage is greater than 6 volts more negative than $-V_{CC}$. A 10kΩ series resistor will limit input current to a safe level with up to ±15V input levels even if both supply voltages are lost.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA121. To avoid leakage problems, it is recommended that the signal input lead of the OPA121 be wired to a Teflon™ standoff. If the OPA121 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high-impedance input leads and should be connected to a low-impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 2).
If guarding is not required, pin 8 (case) should be connected to ground.

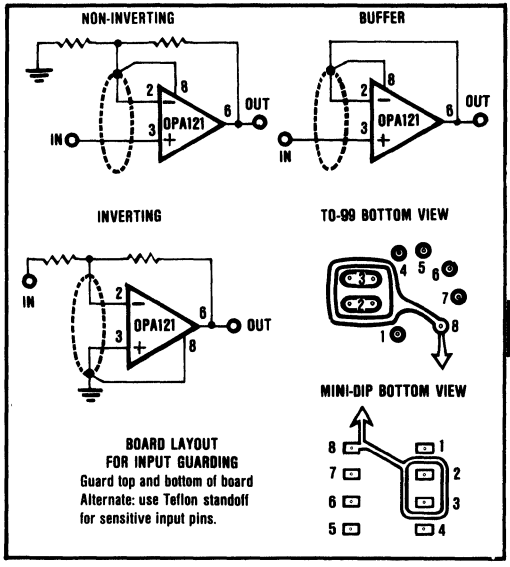


FIGURE 2. Connection of Input Guard.

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET operational amplifiers are affected by common-mode voltage (Figure 3). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely-low bias current of the OPA121 is not compromised by common-mode voltage.

BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information table. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

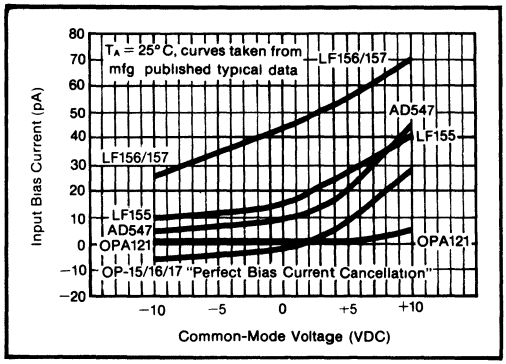
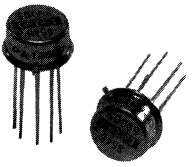


FIGURE 3. Input Bias Current Versus Common-Mode Voltage.

Teflon™ E.I du Pont de Nemours & Co

BURR-BROWN®

OPA128



MILITARY & DIE VERSIONS AVAILABLE

Difet® Electrometer-Grade OPERATIONAL AMPLIFIER

FEATURES

- ULTRA-LOW BIAS CURRENT: 75fA max
- LOW OFFSET: 500μV max
- LOW DRIFT: 5μV/°C max
- HIGH OPEN-LOOP GAIN: 110dB min
- HIGH COMMON-MODE REJECTION: 90dB min
- IMPROVED REPLACEMENT FOR AD515 AND AD549

APPLICATIONS

- ELECTROMETER
- MASS SPECTROMETER
- CHROMATOGRAPH
- ION GAUGE
- PHOTODETECTOR
- RADIATION-HARD EQUIPMENT

DESCRIPTION

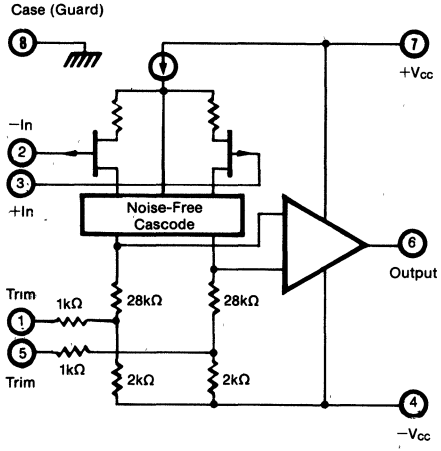
The OPA128 is an ultra-low bias current monolithic operational amplifier. Using advanced geometry dielectrically-isolated FET (*Difet*®) inputs, this monolithic amplifier achieves a performance level exceeding even the best hybrid electrometer amplifiers.

Laser-trimmed thin-film resistors give outstanding voltage offset and drift performance.

A noise-free cascode and low-noise processing give the OPA128 excellent low-level signal handling capabilities. Flicker noise is very low.

The OPA128 is an improved pin-for-pin replacement for the AD515.

Difet® Burr-Brown Corp.



OPA128 Simplified Circuit

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted Pin 8 connected to ground.

PARAMETER	CONDITIONS	OPA128JM			OPA128KM			OPA128LM			OPA128SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT														
BIAS CURRENT[1]														
Input Bias Current	V_{CM} = 0VDC, $R_L \geq 10k\Omega$		±150	±300		±75	±150		±40	±75		±75	±150	fA
OFFSET CURRENT[1]														
Input Offset Current	V_{CM} = 0VDC, $R_L \geq 10k\Omega$		65			30			30			30		fA
OFFSET VOLTAGE[1]														
Input Offset Voltage	V_{CM} = 0VDC		±260	±1000		±140	±500		±140	±500		±140	±500	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}			±20			±10			±5			±10	µV/°C
Supply Rejection		80	120		90	120		90	120		90	120		dB
			±1	±100		±1	±32		±1	±32		±1	±32	µV/V
NOISE[4]														
Voltage, f_O = 10Hz			92			92			92			92		nV/√Hz
f_O = 100Hz			78			78			78			78		nV/√Hz
f_O = 1kHz			27			27			27			27		nV/√Hz
f_O = 10kHz			15			15			15			15		nV/√Hz
f_B = 10Hz to 10kHz			2 4			2 4			2 4			2 4		µV, rms
f_B = 0 1Hz to 10Hz			4			4			4			4		µV, p-p
Current, f_B = 0 1Hz to 10Hz			4 2			3			2 3			3		fA, p-p
f_O = 0 1Hz thru 20kHz			0 22			0 16			0 12			0 16		fA/√Hz
IMPEDANCE														
Differential			$10^{13} \| 1$			$10^{13} \| 1$			$10^{13} \| 1$			$10^{13} \| 1$		Ω | pF
Common-Mode			$10^{15} \| 2$			$10^{15} \| 2$			$10^{15} \| 2$			$10^{15} \| 2$		Ω | pF
VOLTAGE RANGE														
Common-Mode Input Range		±10	±12		±10	±12		±10	±12		±10	±12		V
Common-Mode Rejection	V_{IN} = ±10VDC	80	118		90	118		90	118		90	118		dB
OPEN-LOOP GAIN, DC														
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	94	128		110	128		110	128		110	128		dB
FREQUENCY RESPONSE														
Unity Gain, Small Signal	[2]	0 5	1		0 5	1		0 5	1		0 5	1		MHz
Full Power Response	20V p-p, R_L = 2kΩ		47			47			47			47		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	0 5	3		1	3		1	3		1	3		V/µs
Settling Time, 0 1%	Gain = −1, R_L = 2kΩ		5			5			5			5		µs
0 01%	10V step		10			10			10			10		µs
Overload Recovery, 50% Overdrive[3]	Gain = −1		5			5			5			5		µs
RATED OUTPUT														
Voltage Output	R_L = 2kΩ	±10	±13		±10	±13		±10	±13		±10	±13		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		±5	±10		mA
Output Resistance	DC, open loop		100			100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000			1000		pF
Short Circuit Current		10	29	40	10	29	40	10	29	40	10	29	40	mA
POWER SUPPLY														
Rated Voltage			±15			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		0 9	1 5		0 9	1 5		0 9	1 5		0 9	1 5	mA
TEMPERATURE RANGE														
Specification	Ambient temp.	0		+70	0		+70	0		+70	−55		+125	°C
Operating	Ambient temp	−55		+125	−55		+125	−55		+125	−55		+125	°C
Storage	Ambient temp	−65		+150	−65		+150	−65		+150	−65		+150	°C
θ Junction-Ambient			200			200			200			200		°C/W

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up Bias current doubles approximately every 11°C. (2) Sample tested (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) Noise test available—inquire

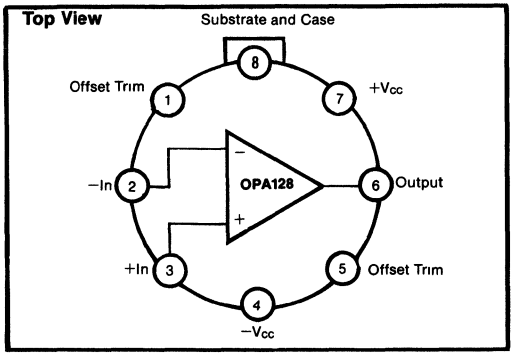
ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA128JM			OPA128KM			OPA128LM			OPA128SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE														
Specification Range	Ambient temp	0		+70	0		+70	0		+70	−55		+125	°C
INPUT														
BIAS CURRENT[1]														
Input Bias Current	V_{CM} = 0VDC		±2 5	±8		±1 3	±4		±0 7	±2		±43	±170	pA
OFFSET CURRENT[1]														
Input Offset Current	V_{CM} = 0VDC		1 1			0 6			0 6			18		pA
OFFSET VOLTAGE[1]														
Input Offset Voltage	V_{CM} = 0VDC			±2 2mV			±1mV			±750			±1 5mV	μV
Average Drift				±20			±10			±5			±10	μV/°C
Supply Rejection		74	114		80	114		80	114		80	106		dB
			±2	±200		±2	±100		±2	±100		±5	±100	μV/V
VOLTAGE RANGE														
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	74	112		80	112		80	112		74	104		dB
OPEN-LOOP GAIN, DC														
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	90	125		104	125		104	125		90	122		dB
RATED OUTPUT														
Voltage Output	R_L = 2kΩ	±10			±10			±10			±10			V
Current Output	V_O = ±10VDC	±5			±5			±5			±5			mA
Short Circuit Current	V_O = 0VDC	10	22		10	22		10	22		10	18		mA
POWER SUPPLY														
Current, Quiescent	I = 0mADC		0 9	1.8		0 9	1 8		0 9	1 8		0.9	2	mA

NOTES (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up

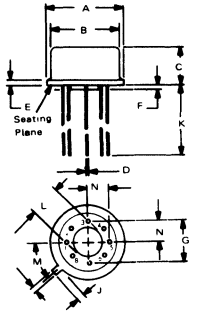
CONNECTION DIAGRAM



MECHANICAL

"M" PACKAGE TO-99 (Hermetic)

NOTE Leads in true position within .010" (.25mm) R at MMC at seating plane
Pin numbers shown for reference only. Numbers may not be marked on package
Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	335	370	8 51	9 40
B	305	335	7 75	8 51
C	165	185	4 19	4 70
D	016	021	0 41	0 53
E	010	040	0 25	1 02
F	010	040	0 25	1 02
G	200 BASIC		5 08 BASIC	
H	028	034	0 71	0 86
J	029	045	0 74	1 14
K	500	–	12 7	
L	110	160	2 79	4 06
M	45° BASIC		45° BASIC	
N	095	105	2 41	2 67

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage	±36VDC
Input Voltage Range	±18VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[2]	Continuous
Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on θ_{CA} = 150°C/W or θ_{JA} = 200°C/W. (2) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

ORDERING INFORMATION

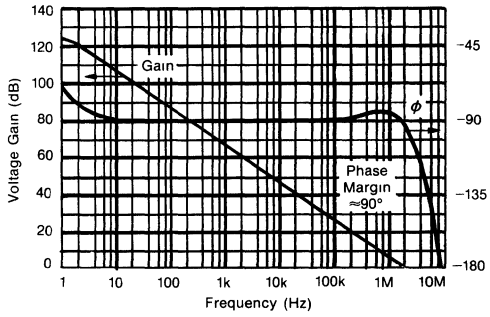
Model	Package	Temperature Range	
OPA128JM	TO-99	0°C to +70°C	
OPA128KM	TO-99	0°C to +70°C	
OPA128LM	TO-99	0°C to +70°C	
OPA128SM	TO-99	−55°C to +125°C	
BURN-IN SCREENING OPTION			
Model	**Package**	**Temperature Range**	**Burn-In Temp. (160h)[1]**
OPA128JM-BI	TO-99	0°C to +70°C	+125°C
OPA128KM-BI	TO-99	0°C to +70°C	+125°C
OPA128LM-BI	TO-99	0°C to +70°C	+125°C
OPA128SM-BI	TO-99	−55°C to +125°C	+125°C

NOTE (1) Or equivalent combination of time and temperature

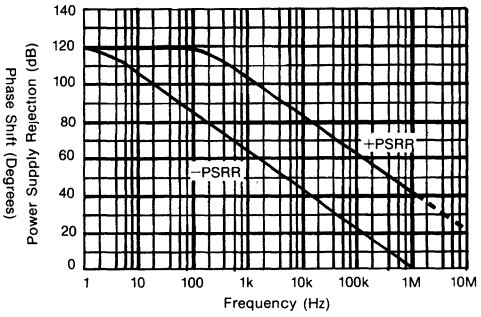
TYPICAL PERFORMANCE CURVES

T_A = +25°C, ±15VDC unless otherwise noted

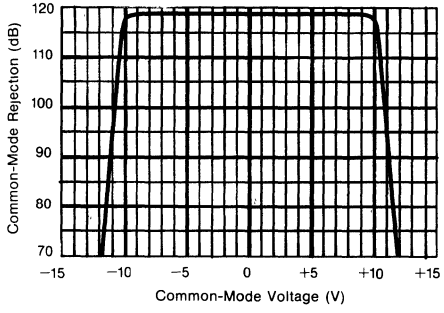
OPEN-LOOP FREQUENCY RESPONSF



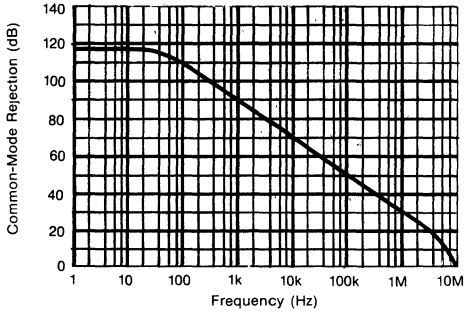
POWER SUPPLY REJECTION vs FREQUENCY



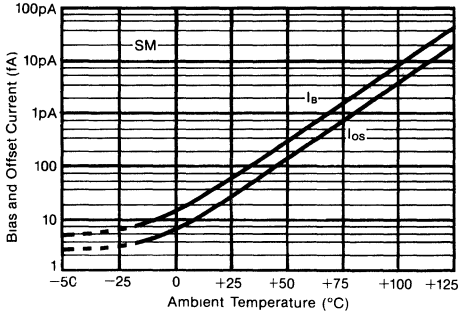
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



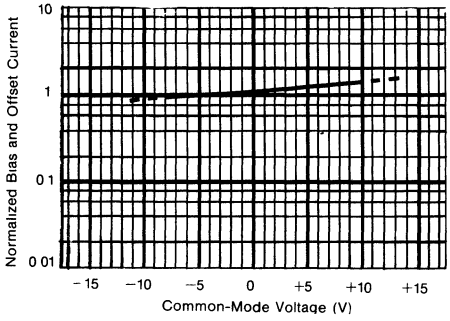
COMMON-MODE REJECTION vs FREQUENCY



BIAS AND OFFSET CURRENT vs TEMPERATURE



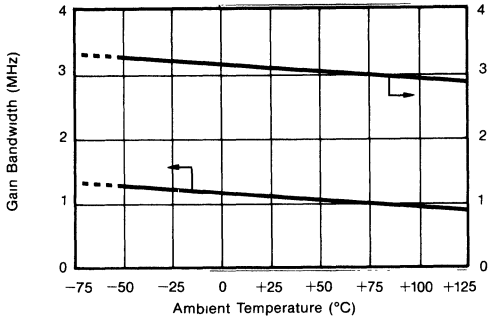
BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



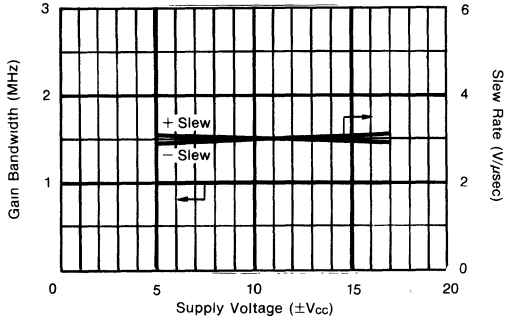
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, ±15VDC unless otherwise noted

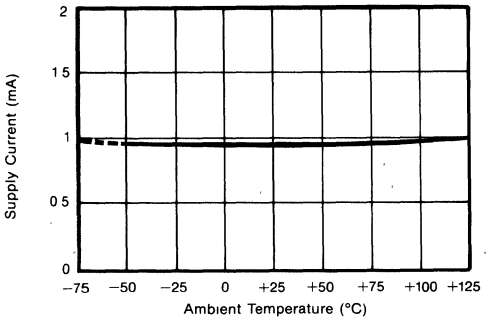
GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



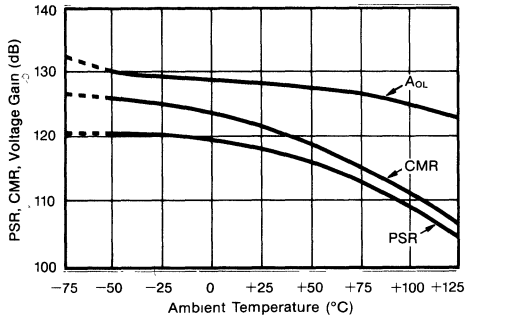
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



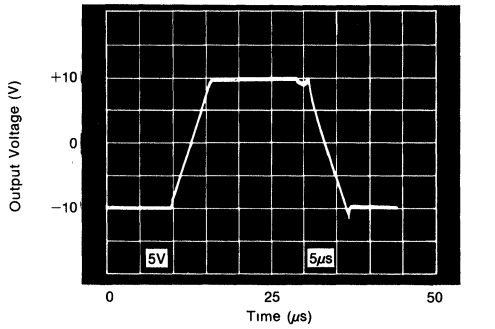
SUPPLY CURRENT vs TEMPERATURE



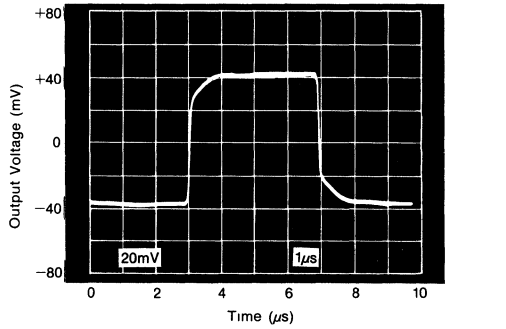
OPEN-LOOP GAIN, PSR, AND CMR vs TEMPERATURE



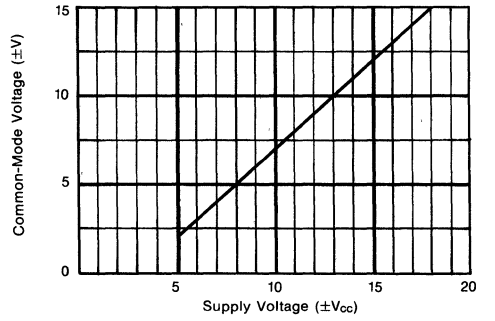
LARGE SIGNAL TRANSIENT RESPONSE



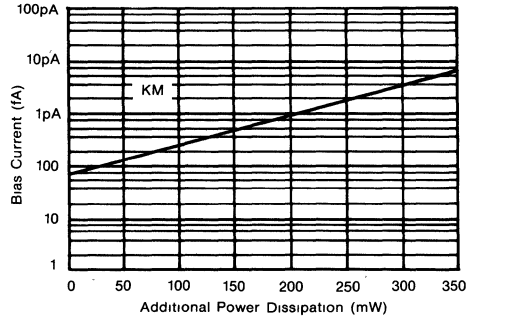
SMALL SIGNAL TRANSIENT RESPONSE



COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE

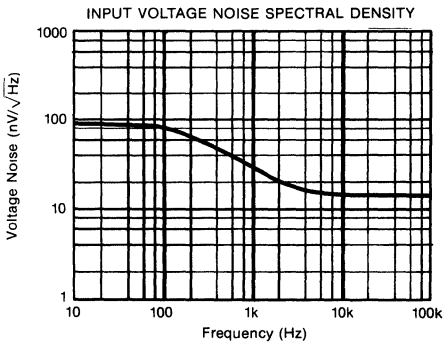


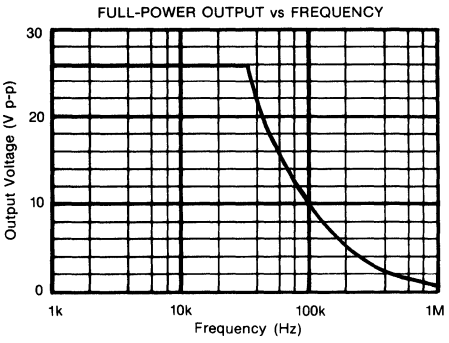
BIAS CURRENT vs ADDITIONAL POWER DISSIPATION



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, ±15VDC unless otherwise noted.





APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA128 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.3μV/°C for each 100μV of adjusted effort. Note that the trim (Figure 1) is similar to operational amplifiers such as HA-5180 and AD515. The OPA128 can replace many other amplifiers by leaving the external null circuit unconnected.

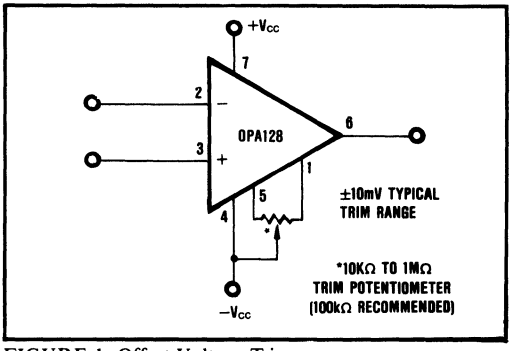


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers' inputs must be protected against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET® amplifiers can be destroyed by the loss of $-V_{CC}$.

Because of its dielectric isolation, no special protection is needed on the OPA128. Of course, the differential and common-mode voltage limits should be observed.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

BIFET® National Semiconductor Corp

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry. Leakage currents across printed circuit boards can easily exceed the bias current of the OPA128. To avoid leakage problems, it is recommended that the signal input lead of the OPA128 be wired to a Teflon standoff. If the input is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 2).

Triboelectric charge (static electricity generated by friction) can be a troublesome noise source from cables connected to the input of an electrometer amplifier. Special low-noise cable will minimize this effect but the optimum solution is to mount the signal source directly at the electrometer input with short, rigid, wiring to preclude microphonic noise generation.

TESTING

Accurately testing the OPA128 is extremely difficult due to its high level of performance. Ordinary test equipment may not be able to resolve the amplifier's extremely low bias current.

Inaccurate bias current measurements can be due to:

1. Test socket leakage
2. Unclean package
3. Humidity or dew point condensation
4. Circuit contamination from fingerprints or anti-static treatment chemicals
5. Test ambient temperature
6. Load power dissipation.

BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information table. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

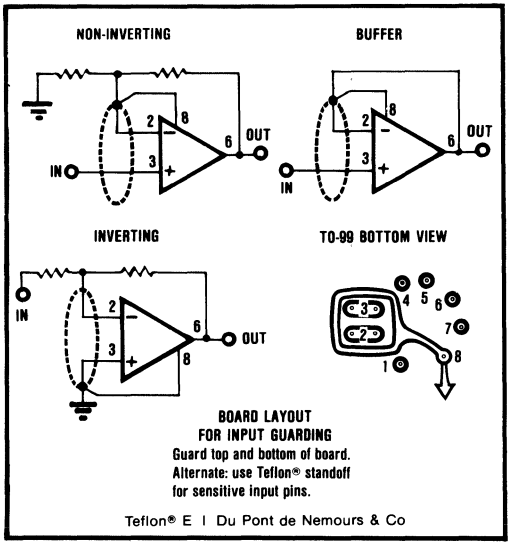


FIGURE 2. Connection of Input Guard.

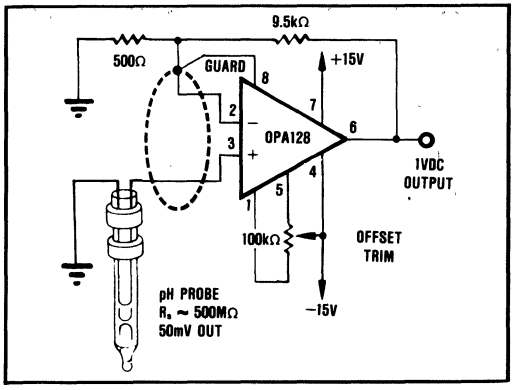


FIGURE 3. High Impedance ($10^{15}\Omega$) Amplifier.

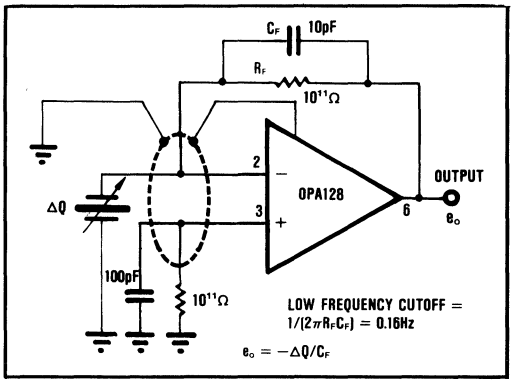


FIGURE 4. Piezoelectric Transducer Charge Amplifier.

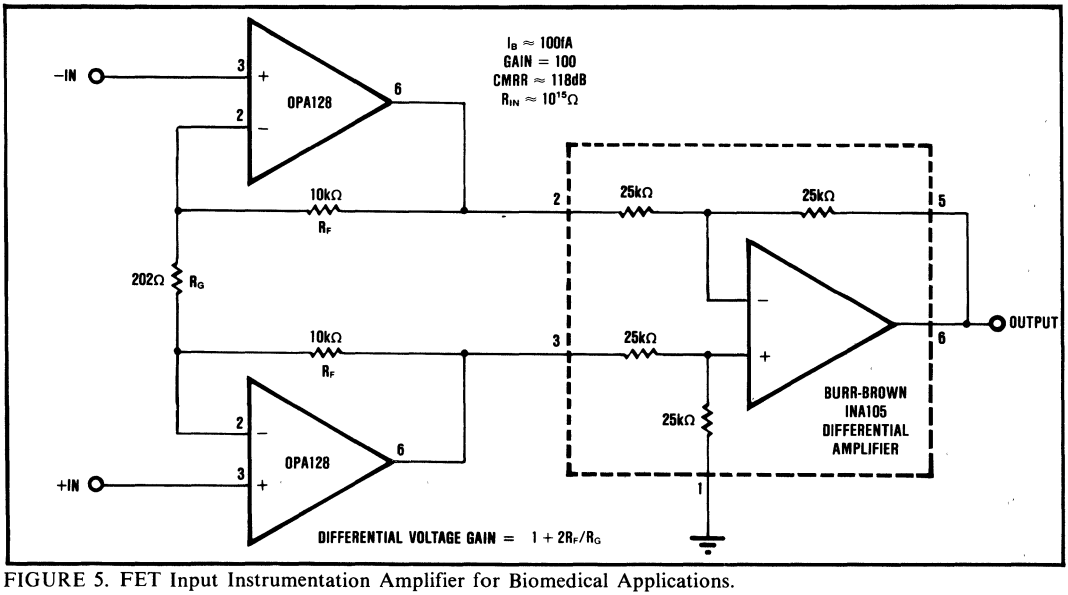


FIGURE 5. FET Input Instrumentation Amplifier for Biomedical Applications.

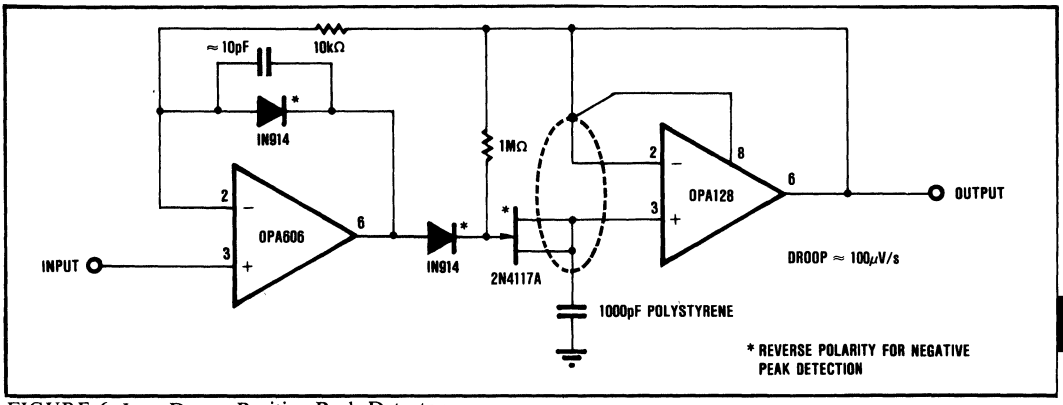
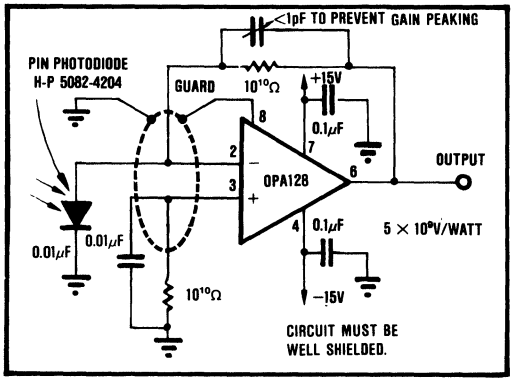


FIGURE 6. Low-Droop Positive Peak Detector.



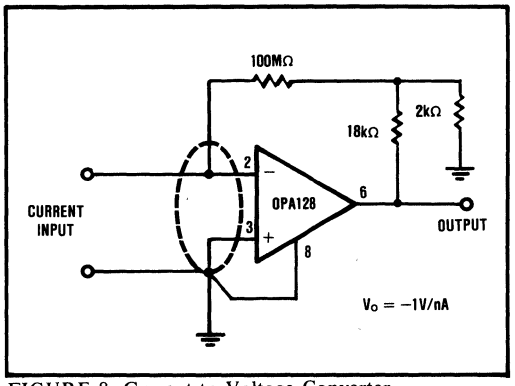


FIGURE 8. Current-to-Voltage Converter.

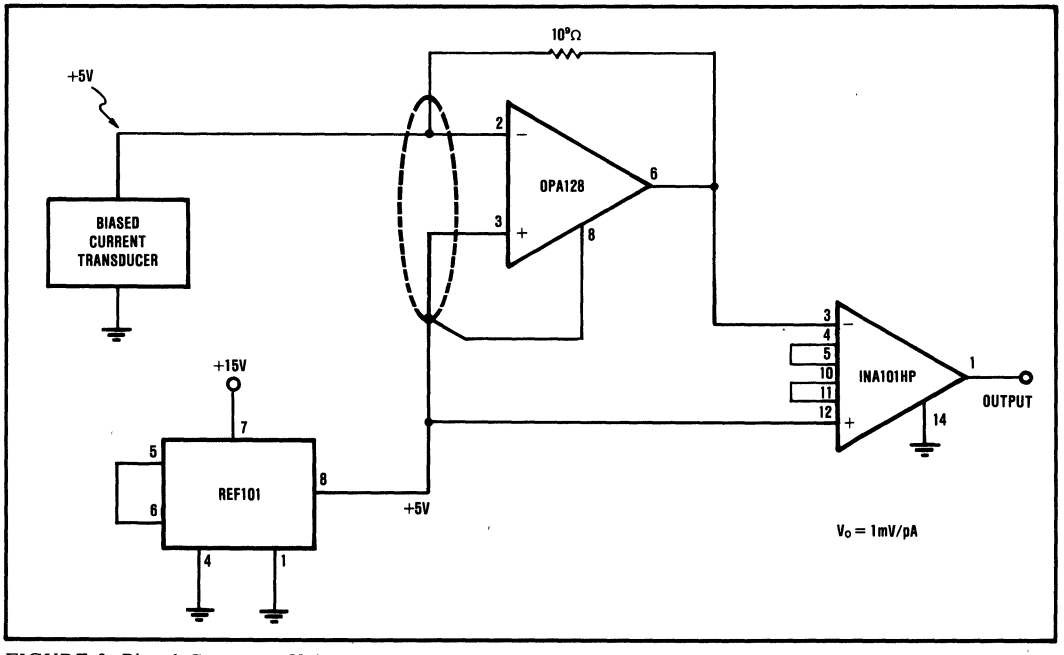
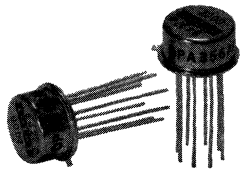


FIGURE 9. Biased Current-to-Voltage Converter.

BURR-BROWN®



OPA156A
OPA356A

MILITARY & DIE VERSIONS AVAILABLE

Wide-Bandwidth *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH, 4MHz min
- HIGH SLEW RATE, 10V/μsec min
- LOW BIAS CURRENT, 50pA max at T_A = +25°C
- LOW OFFSET VOLTAGE, 2mV max
- LOW DRIFT, 5μV/°C max

APPLICATIONS

- OPTOELECTRONICS
- DATA ACQUISITION
- IMPROVED REPLACEMENT FOR INDUSTRY-STANDARD LF156A BIFET® OPERATIONAL AMPLIFIER

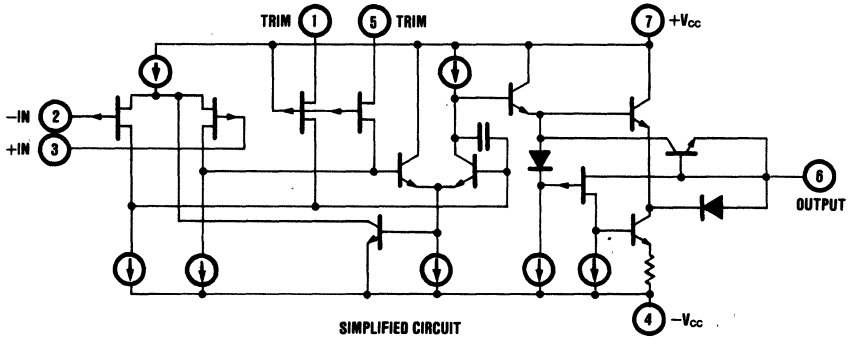
DESCRIPTION

The OPA156A/356A is a wide-bandwidth monolithic dielectrically-isolated FET (*Difet*) operational amplifier. Improved circuit design and dielectric isolation allow lower bias current than BIFET LF156A amplifiers. Bias current is specified under warmed-up and operating conditions, not at a JUNCTION temperature of +25°C.

Laser-trimmed thin-film resistors offer improved offset voltage and noise performance.

The OPA156A is internally compensated for unity-gain stability.

BIFET® National Semiconductor Corp., *Difet*® Burr-Brown Corp.



SIMPLIFIED CIRCUIT

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-548A

SPECIFICATIONS

ELECTRICAL

At $\pm V_{CC}$ = 15VDC and T_A = +25°C unless otherwise specified

PARAMETER	CONDITIONS	OPA156A MIN	OPA156A TYP	OPA156A MAX	OPA356A MIN	OPA356A TYP	OPA356A MAX	UNITS
FREQUENCY RESPONSE								
Slew Rate	V_o = ±10V, R_L = 2kΩ							
	G = +1	10	14		10	14		V/µsec
Settling Time, 0.01%[1]	10V Step, R_L = 2kΩ		4			4		µsec
Gain Bandwidth		4	6		4	6		MHz
INPUT								
NOISE								
Voltage f_o = 100Hz	R_s = 100Ω		25			25		nV/√Hz
f_o = 1kHz	R_s = 100Ω		15			15		nV/√Hz
Current f_o = 100Hz			0.005			0.005		pA/√Hz
f_o = 1kHz			0.005			0.005		pA/√Hz
OFFSET VOLTAGE[2]								
Input Offset Voltage	R_s = 50Ω		±1	±2		±1	±2	mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3	±5		±3	±5	µV/°C
Supply Rejection	$\Delta+V_{CC} = \Delta-V_{CC}$	85	100		85	100		dB
			±10	±57		±10	±57	µV/V
BIAS CURRENT[2]								
Input Bias Current	V_{cm} = 0VDC		30	50		30	50	pA
OFFSET CURRENT[2]								
Input Offset Current	V_{cm} = 0VDC		3	10		3	10	pA
INPUT IMPEDANCE								
Resistance ‖ Capacitance			10^{12} ‖ 3			10^{12} ‖ 3		Ω ‖ pF
VOLTAGE RANGE								
Common-Mode Input Range		±11	±12		±11	±12		V
Common-Mode Rejection	V_{IN} = ±10VDC	85	100		85	100		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	94	106		94	106		dB
		50	200		50	200		V/mV
RATED OUTPUT								
Voltage Output	R_L = 10kΩ	±12	±13		±12	±13		V
	R_L = 2kΩ	±10	±12		±10	±12		V
POWER SUPPLY								
Rated Voltage			±15			±15		VDC
Voltage Range, Derated Performance		±5		±20	±5		±18	VDC
Current, Quiescent	I_o = 0mADC		5	7		5	10	mA
TEMPERATURE RANGE								
Specification	Ambient temp.	−55		+125	0		+70	°C
Storage	Ambient temp	−65		+150	−65		+150	°C
θ Junction-Ambient			150			150		°C/W

NOTES: (1) Sample tested—this parameter is not guaranteed See settling time test circuit (Figure 2) (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $\pm V_{CC}$ = 15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted

PARAMETER	CONDITIONS	OPA156A MIN	OPA156A TYP	OPA156A MAX	OPA356A MIN	OPA356A TYP	OPA356A MAX	UNITS
TEMPERATURE RANGE								
Specification Range	Ambient temp	−55		+125	0		+70	°C
INPUT								
OFFSET VOLTAGE[1]								
Input Offset Voltage	R_s = 50Ω		±1	±2 5		±1	±2 3	mV
Average Drift	R_s = 50Ω		±3	±5		±3	±5	µV/°C
Supply Rejection	$\Delta+V_{CC} = \Delta-V_{CC}$	85	100		85	100		dB
			±10	±57		±10	±57	µV/V
BIAS CURRENT[1]								
Input Bias Current	V_{cm} = 0VDC		15	25		3	5	nA
OFFSET CURRENT[1]								
Input Offset Current	V_{cm} = 0VDC		6	10		0.6	1	nA
VOLTAGE RANGE								
Common-Mode Input Range		±11	±12		±11	±12		V
Common-Mode Rejection	V_{IN} = ±10VDC	85	100		85	100		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	88	92		88	92		dB
		25	40		25	40		V/mV
RATED OUTPUT								
Voltage Output	R_L = 10kΩ	±12	±13		±12	±13		V
	R_L = 2kΩ	±10	±12		±10	±12		V

NOTE (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

ABSOLUTE MAXIMUM RATINGS

Supply. OPA156A	±22VDC
OPA356A	±18VDC
Internal Power Dissipation[1]	670mW
Differential Input Voltage[2]	±40VDC
Input Voltage Range[2]	±20VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[3]	Continuous
Junction Temperature	+150°C

NOTES. (1) Packages must be derated based on θ_{JC} = 45°C/W or θ_{JA} = 150°C/W (2) For supply voltages less than ±18VDC the absolute maximum input voltage is equal to the supply voltage. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient Observe dissipation limit and T_J.

ORDERING INFORMATION

OPA X 56A X

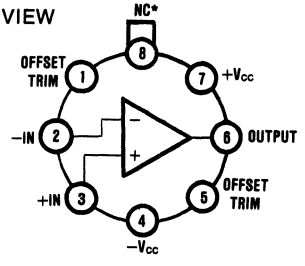
Basic model number

Temperature range
- 1 = −55°C to +125°C
- 3 = 0°C to +70°C

Package code
- M = TO-99

CONNECTION DIAGRAMS

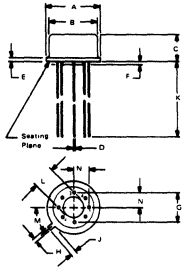
TOP VIEW



* NO INTERNAL CONNECTION
CASE IS INTERNALLY CONNECTED TO V_{CC}

MECHANICAL

"M" PACKAGE: TO-99



NOTE: Leads in true position within 0 01" (0 25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

The TO-99 can and leads are bright acid tin plated.

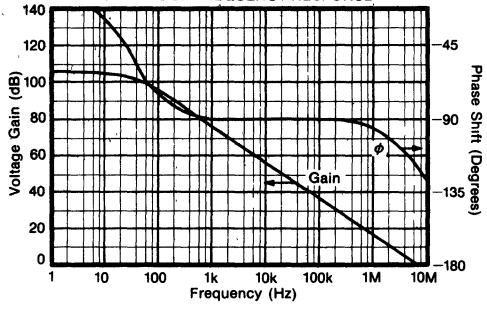
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	335	370	8 51	9 40
B	305	335	7 75	8 51
C	165	185	4 19	4 70
D	016	021	0 41	0 53
E	010	040	0 25	1 02
F	010	040	0 25	1 02
G	200 BASIC		5 08 BASIC	
H	028	034	0 71	0 86
J	029	045	0 74	1 14
K	500		12 7	
L	110	160	2 79	4 06
M	45° BASIC		45° BASIC	
N	095	105	2 41	2 67

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

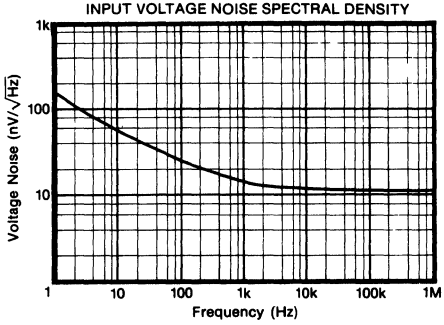
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted

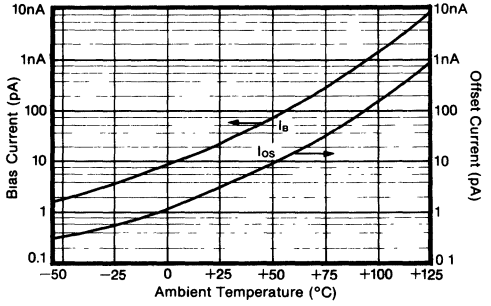
OPEN-LOOP FREQUENCY RESPONSE



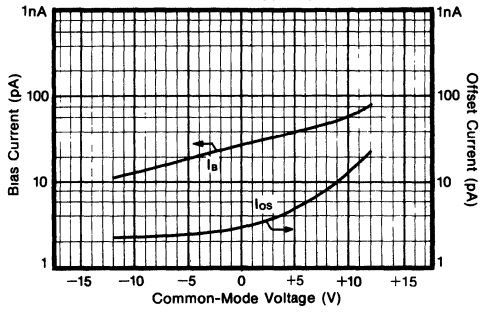
INPUT VOLTAGE NOISE SPECTRAL DENSITY



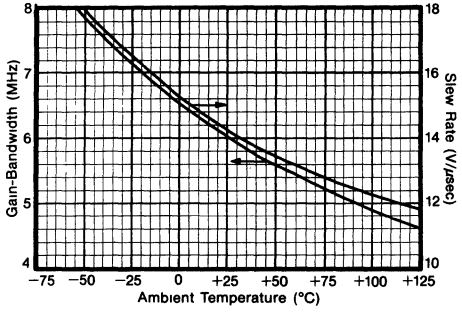
BIAS AND OFFSET CURRENT vs TEMPERATURE



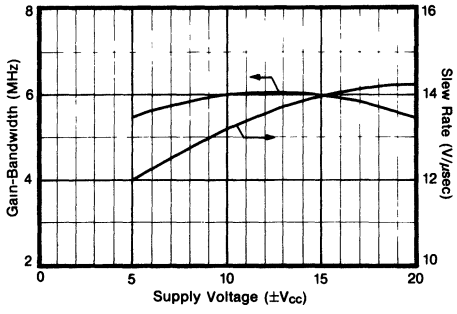
BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



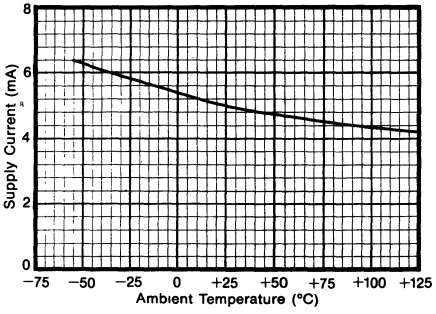
GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



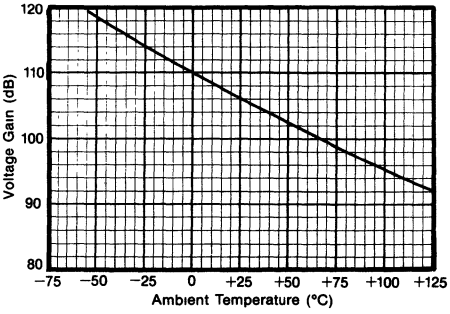
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



SUPPLY CURRENT vs TEMPERATURE



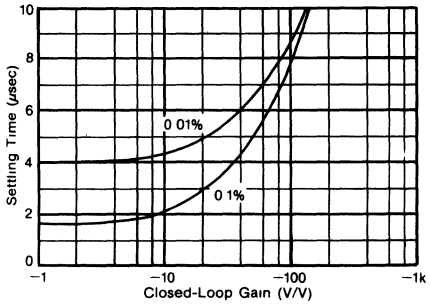
OPEN-LOOP GAIN vs TEMPERATURE



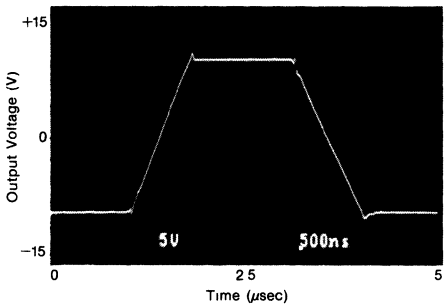
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted

SETTLING TIME vs CLOSED-LOOP GAIN



LARGE SIGNAL TRANSIENT RESPONSE



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA156A offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.5μV/°C for each millivolt of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as LF156 and OP-16. The OPA156A can replace most other amplifiers by leaving the external null circuit unconnected.

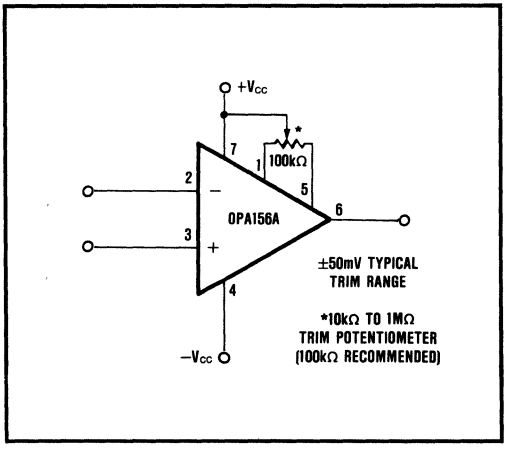


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

If the input voltage exceeds the supply voltage, current must be limited to 1mA to prevent damage.

CIRCUIT LAYOUT

Wideband amplifiers require good circuit layout techniques and adequate power supply bypassing. Short, direct connections and good high frequency bypass capacitors (ceramic or tantalum) will help avoid noise pickup or oscillation.

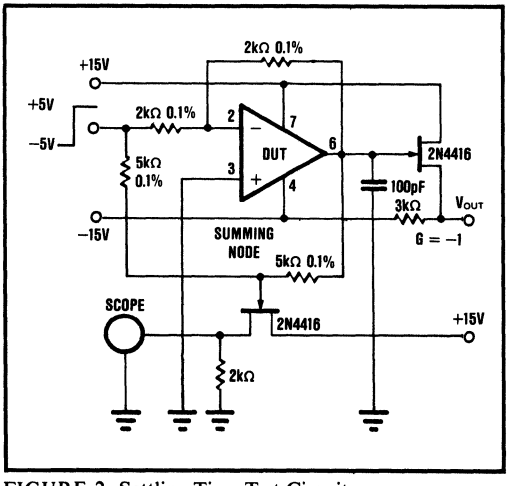


FIGURE 2. Settling Time Test Circuit.

APPLICATIONS CIRCUITS

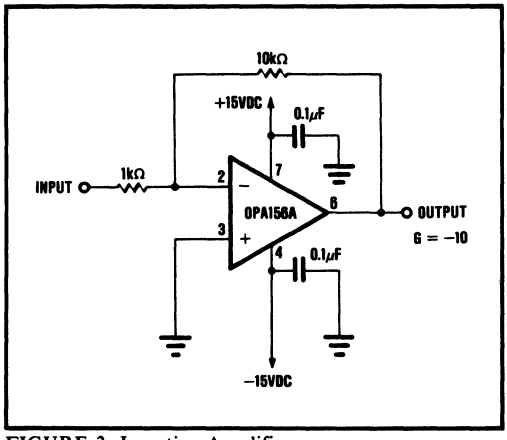


FIGURE 3. Inverting Amplifier.

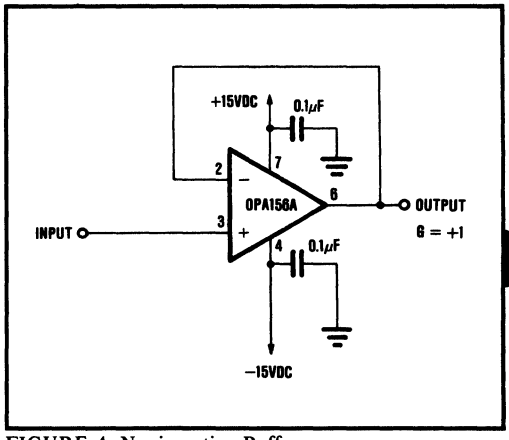


FIGURE 4. Noninverting Buffer.

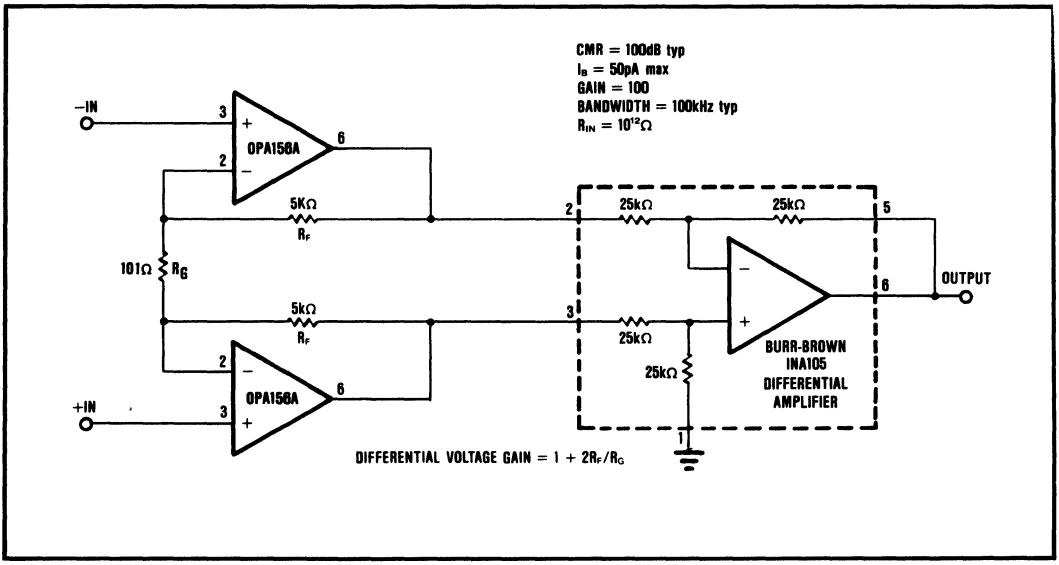


FIGURE 5. Wideband FET Input Instrumentation Amplifier.

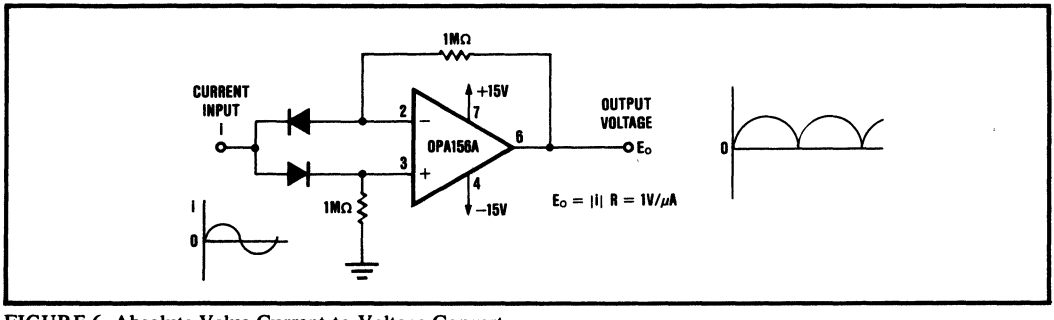
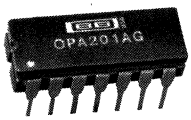


FIGURE 6. Absolute Value Current-to-Voltage Converter.

BURR-BROWN®



OPA201

Switchable-Input Operational Amplifier SWOP AMP®

FEATURES

- TWO PRECISION INPUT STAGES SELECTABLE BY DIGITAL SIGNAL
- EXCELLENT INPUT SPECIFICATIONS
  - V_{OS} 100μV max
  - DRIFT: 0.5μV/°C typ
  - I_B 25nA max
- LOW POWER
  - $\pm V_{CC}$ 2.5V to 18V
  - I_Q 500μA max

APPLICATIONS

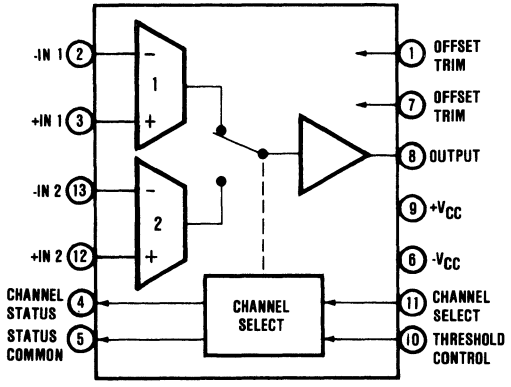
- AUTO-ZERO SYSTEMS
- TWO-CHANNEL MULTIPLEXER WITH GAIN
- SWITCHABLE-GAIN CIRCUITS
- SWITCHABLE-BANDWIDTH CIRCUITS
- SYNCHRONOUS MODULATOR/DEMODULATOR
- BATTERY OPERATED SYSTEMS

DESCRIPTION

The OPA201 is a switchable-input operational amplifier (Swop Amp®). It contains two independent differential input stages and one output stage. Either of the input stages may be connected to the output stage under the control of the Channel Select digital input signal which is TTL-compatible or user-programmable. The OPA201 is easy to use and functions as an operational amplifier that can switch between two sets of inputs.

Each input stage provides excellent input characteristics: low offset voltage (100μV, max), low offset voltage drift versus temperature (1μV/°C, max), and low bias current (25nA, max).

Additionally, the Swop Amp is a low power device. It draws less than 500μA (max) over the supply range $\pm$2.5V to $\pm$18V. It is well suited for portable, remote, and other battery powered applications. Also, its low power consumption and excellent specifications make it well suited for isolation circuit applications. Burr-Brown's state-of-the-art monolithic design and processing, compatible thin-film resistors, and active laser trimming produce a truly unique highly versatile circuit. The unique switchable input stage design allows solutions to very demanding analog circuit design problems.



Swop Amp® Burr-Brown Corp.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-491E

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted Specifications are for both channels unless otherwise noted

PARAMETER	CONDITIONS	OPA201AG/RG MIN	OPA201AG/RG TYP	OPA201AG/RG MAX	OPA201BG/SG MIN	OPA201BG/SG TYP	OPA201BG/SG MAX	OPA201CG MIN	OPA201CG TYP	OPA201CG MAX	UNITS
OPEN-LOOP GAIN, DC	$V_{OUT} = \pm 10V$										
Rated Load	$R_L = 10k\Omega$	114	130		*	*		120	*		dB
RATED OUTPUT											
Voltage	$R_L = 10k\Omega$	±13 5	±14		*	*		*	*		V
Current	$V_{OUT} = \pm 10V$		5			*			*		mA
Output Impedance			0 5			*			*		kΩ
Short Circuit Current			10			*			*		mA
INPUT OFFSET VOLTAGE											
Either Channel											
Voltage Offset[1]			120	500		70	200		35	100	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		1 4			0 9			0 5		µV/°C
PSRR	$\pm V_{CC} = \pm 2$ 5V to ±18V		8	32		5	18		4	10	µV/V
	$T_A = T_{MIN}$ to T_{MAX}		10			6			5		µV/V
Match Between Channels 1 and 2											
Offset Voltage			150	500		65	100		25	50	µV
Over Temperature			150			90			30		µV
INPUT BIAS CURRENT											
Bias Current			15	50		13	40		12	25	nA
INPUT OFFSET CURRENT											
Offset Current			1 4	4		0 75	2		0 7	1	nA
FREQUENCY RESPONSE											
Gain Bandwidth			500			*			*		kHz
Full Power Response			4			*			*		kHz
Slew Rate	$V_{OUT} = \pm 10V$, $R_L = 10k\Omega$	0 1	0 18		*	*		*	*		V/µs
Settling Time 0 1%	10V Step		49			*			*		µs
0 01%	10V Step		52			*			*		µs
INPUT IMPEDANCE											
Differential			6			*			*		MΩ
Common-Mode			$10^{10} \parallel 2$			*			*		Ω ‖ pF
INPUT NOISE											
Voltage	f_B = 0 1 to 10Hz		1			*			*		µV, p-p
Voltage Density	f_o = 10Hz		27			*			*		nV/√Hz
	f_o = 100Hz		27			*			*		nV/√Hz
	f_o = 1kHz		27			*			*		nV/√Hz
Current	f_B = 0 1 to 10Hz		1 5			*			*		pA, p-p
Current Density	f_o = 10Hz		300			*			*		fA/√Hz
	f_o = 100Hz		100			*			*		fA/√Hz
	f_o = 1kHz		100			*			*		fA/√Hz
INPUT VOLTAGE RANGE											
Common-Mode Range		−12 5		+12 5	*		*	*		*	V
	$T_A = T_{MIN}$ to T_{MAX}		±12			*			*		V
Common-Mode Rejection	$V_{IN} = +10V$	85	94		90	98		95	98		dB
	$T_A = T_{MIN}$ to T_{MAX}		92			95			97		dB
POWER SUPPLY											
Rated Voltage	Specification		±15			*			*		VDC
Voltage Range, Derated Performance		±2 5		±18	*		*	*		*	VDC
Current, Quiescent	I_O = 0mA		425	500		*	*		*	*	µA
DIGITAL SIGNALS											
Threshold Control (TC) Voltage Range		$-V_{CC}$		$+V_{CC} - 5$	*		*	*		*	V
Channel Select (CSEL)											
Voltage Range		$-V_{CC}$		$+V_{CC}$	*		*	*		*	V
V_{IH} (selects ch 1)		$V_{TC} + 2$		$+V_{CC}$	*		*	*		*	V
V_{IL} (selects ch 2)		$-V_{CC}$		$V_{TC} + 0$ 8	*		*	*		*	V
I_{IH}	$V_{CSEL} = +V_{CC}$		<1	50		*	*		*	*	µA
I_{IL}	$V_{CSEL} = V_{TC} = 0V$		25	60		*	*		*	*	µA
Status Common (SC) Voltage Range		$-V_{CC}$		[3]	*		[3]	*		[3]	V
Channel Status (CSTA = CSEL)[2]											
V_{OL}	I_{OL} = 1mA, V_{SC} = 0V			0 4			*			*	V
V_{OH}	V_{Pullup} = 15V, V_{SC} = 0V	2 0	15		*	*		*	*		V

ELECTRICAL (CONT)

PARAMETER	CONDITIONS	OPA201AG/RG			OPA201BG/SG			OPA201CG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL SIGNALS											
I_{OH} (OFF)			<1	20		*	*		*	*	μA
Switching Time											
Between Channels	$T_{MIN} \leq T_A \leq T_{MAX}$		5			*			*		μs
CROSSTALK											
DC	V_{IN} to OFF	−100	−130		−120	*		−120	*		dB
60Hz	Channel = ±12V		−108			*			*		dB
TEMPERATURE RANGE	Ambient										
Specification											
A, B, C Grades		−25		+85	*		*	*		*	°C
S Grade					−55		+125				°C
Operating		−55		+125	*		*	*		*	°C

*Specification same as OPA201AG/RG

NOTES

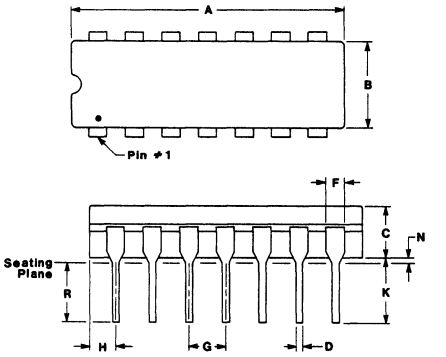
1 Voltage offset is also guaranteed fully warmed-up

2 V_{TC} = Voltage on threshold control, pin 10 V_{IH}, V_{IL}, V_{OH}, V_{OL}, I_{IH}, I_{IL}, I_{OH}, I_{OL}, refer to voltage and current, input and output, high and low logic states.

3 Maximum voltage at Status Common must not be more positive than the Channel Select voltage (pin 11) or Threshold Control voltage (pin 10).

MECHANICAL

"G" Package



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.753	.787	19.13	19.48
B	.245	.251	6.22	6.38
C	.140	.170	3.56	4.32
D	.018	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	–	.085	–	2.16
J	.008	.012	0.20	0.30
K	.150	–	3.80	–
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

NOTES 1 Leads in true position within 0.01" (0.25mm) R at seating plane.

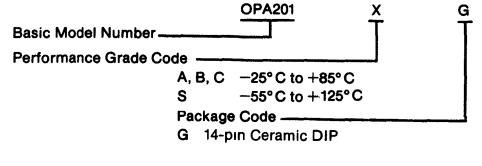
ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage[2]	±36VDC
Input Voltage Range[2]	±18VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[3]	Continuous
Junction Temperature	+175°C

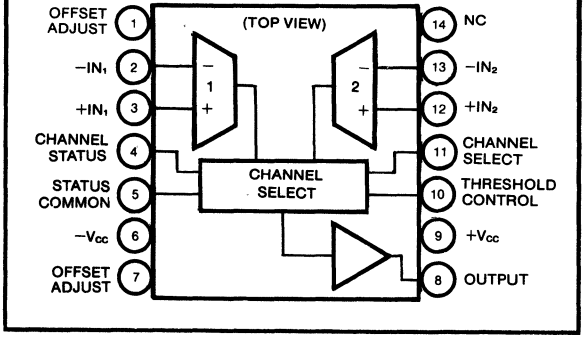
NOTES:

1. θ_{JA} = 100°C/W
2. For supply voltages less than ±18VDC the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to power supply common or ±V_{CC}.

ORDERING INFORMATION



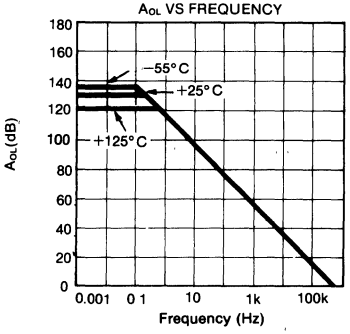
PIN CONFIGURATION



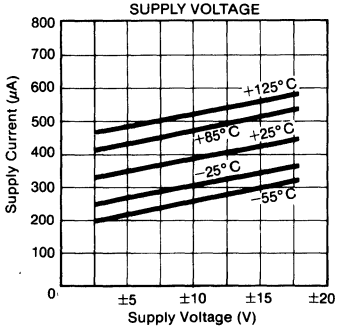
TYPICAL PERFORMANCE CURVES

T_A = +25°C, ±V_{CC} = 15VDC, specifications are for both channels unless otherwise noted

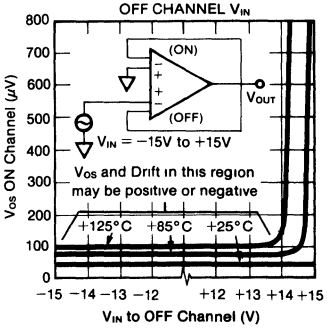
A_{OL} VS FREQUENCY



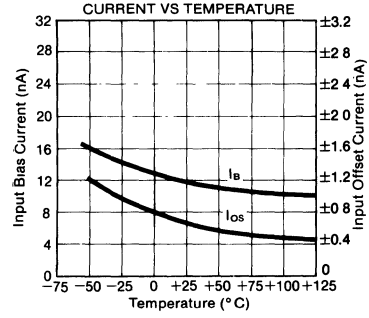
SUPPLY CURRENT VS SUPPLY VOLTAGE



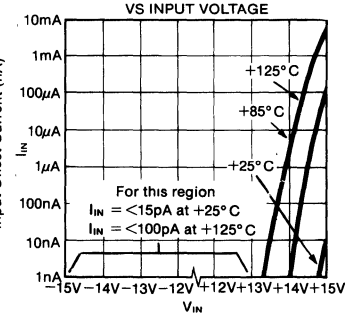
ON CHANNEL V_{OS} VS OFF CHANNEL V_{IN}



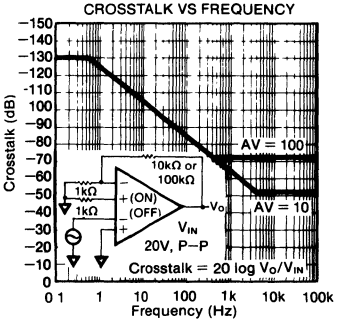
INPUT BIAS AND OFFSET CURRENT VS TEMPERATURE



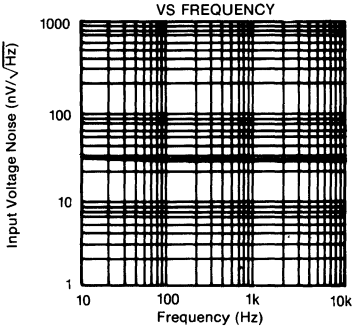
OFF CHANNEL INPUT CURRENT VS INPUT VOLTAGE



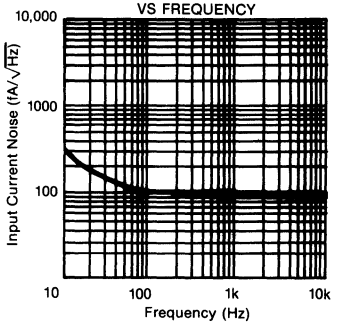
CROSSTALK VS FREQUENCY



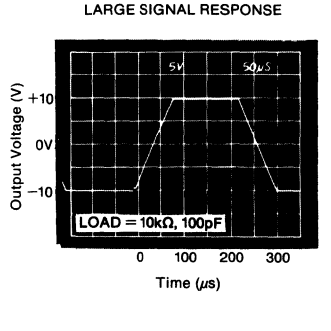
INPUT VOLTAGE NOISE DENSITY VS FREQUENCY



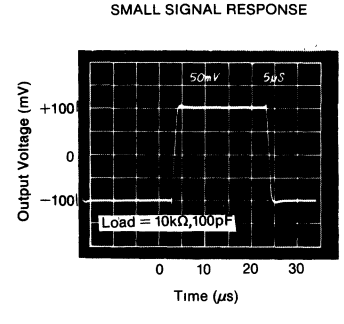
INPUT CURRENT NOISE DENSITY VS FREQUENCY



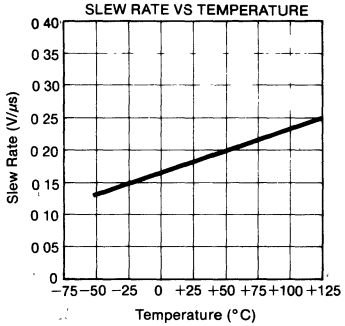
LARGE SIGNAL RESPONSE



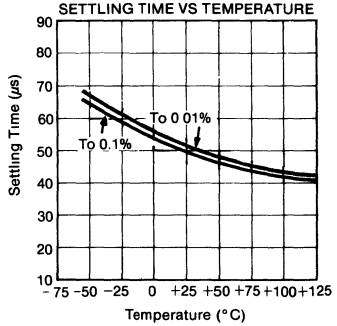
SMALL SIGNAL RESPONSE



SLEW RATE VS TEMPERATURE



SETTLING TIME VS TEMPERATURE



THEORY OF OPERATION

A simplfied schematic of the OPA201 Swop Amp is shown in Figure 1. The circuit has four main parts: (A) input stage 1, (B) input stage 2, (C) active load and output amplifier, and (D) channel select circuit. The two precision differential input stages are identical, with offset and drift laser-trimmed for very-tight matching. The input stages share a balanced, high precision active load and external offset adjust pins, so offset trim affects both channels (see "Using the Swop Amp" section for independent trim techniques). The input stages also share a gain stage and complementary output stage. The biasing circuits for the two input stages are well matched, so the characteristics of the two amplifiers are very nearly identical.

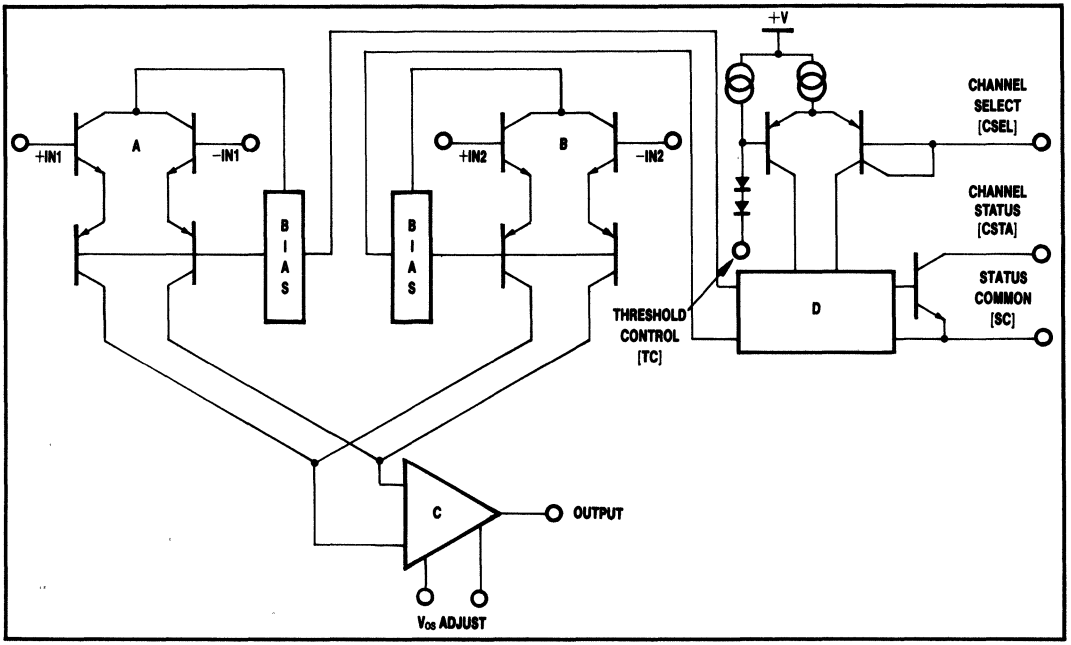


FIGURE 1. OPA 201 Simplified Schematic.

Under control of the channel select circuitry, only one input stage at a time is active. The selected input stage controls the output amplifier, while the unselected input stage is turned off by deactivating its bias circuitry. With no current in the unselected stage, it has negligible input bias current, and the OFF channel cannot send signals to the output amplifier (see Crosstalk specifications and Typical Performance Curves).

The channel select circuitry is simple but versatile, and its use is fully described in the "Using the Swop Amp" section. The trip point for changing channels is set by the threshold control, pin 10. This provides TTL-compatible levels for the channel select voltage on pin 11 when pin 10 is grounded. An open collector output transistor provides the logic inverse of the channel select voltage at the channel status pin. The emitter of this transistor, status common, is also brought out to a pin so the channel status can be referenced to ground or −V.

The complete circuit functions as a high precision operational amplifier which can switch between two sets of inputs under control of a 1-bit logic signal.

USING THE SWOP AMP

Designing with the Swop Amp is basically the same as designing with any precision operational amplifer, with the added versatility of switchable inputs. Feedback is connected from the output to each differential input to configure each channel as an inverting or noninverting amplifier, integrator, or other analog circuit function. The transfer functions for channels 1 and 2 may be identical to the point of sharing feedback elements, or they may be completely independent. Feedback resistors for the off channel are driven by the output as part of the load resistance. Error analysis involving E_{os}, I_B, I_{os}, and V_{cm} is the same as for any operational amplifier.

The OFF channel may be modeled as an open circuit in most applications, with input currents typically under 15pA for input voltages within the specified common-mode range (see Typical Performance Curves). Although crosstalk is specified for OFF channel input voltages equal to the common-mode input range extremes, the same crosstalk characteristics are typically observed for **all input voltages between $-V_{CC}$ and ($+V_{CC}$ −1VDC). Rejection of signals applied to the OFF channel's inputs** is outstanding, as shown by the −120dB Crosstalk specifications and Typical Performance Curves for cross-talk versus frequency.

CHANNEL SELECTION

Four pins are involved in the channel select logic,

providing programmable input logic levels for channel select and an output status indicating which channel has been selected. Programmable logic levels allow the logic to be referenced to ground or virtually any voltage. Referencing the logic to −V is especially useful in applications where the supply voltage is low, for example ±3V. The pin-by-pin description and recommended connections describe the versatile but simple channel select techniques (refer to Figures 2 and 3).

Pin 10 - Threshold Control

Pin 10 sets the threshold voltage for channel switching, such that the switching point is two diode drops (≈1.3V) more positive than the Threshold Control voltage. This results in TTL compatibility when pin 10 is grounded. **Pin 10 must be at least 5V more negative than $+V_{CC}$, and should be tied to $-V_{CC}$ when the minimum supply voltages are used (±2.5V or +5V). This results in TTL compatibility for logic referenced to $-V_{CC}$.**

Pin 11 - Channel Select

The voltage on pin 11 determines which input stage is active. A logic high **selects channel 1,** logic low selects channel 2. Logic voltages are referenced to the Threshold Control, pin 10, and are TTL-, CMOS-, and open collector-compatible.

Pin 4 - Channel Status

Channel Status is an open collector output indicating which channel has been selected. It is the logic inverse of the Channel Select input referenced to Status Common, pin 5. This function is not required in many applications, and pin 4 should be left unconnected if not used. When using Channel Status, a pullup resistor is connected between pin 4 and a potential more positive than pin 5 (usually +V or ground). The logic low (indicating channel 1 selected) will be less than 0.4V more positive than pin 5 if the pullup resistor sets a current of 1mA or less. Logic high will be the voltage connected to the pullup resistor.

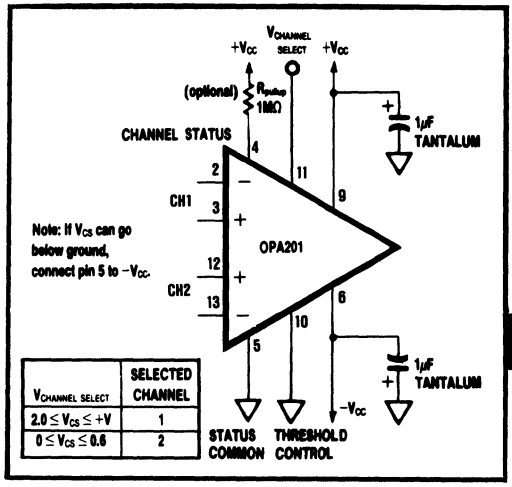
Pin 5 - Status Common

Status Common sets the reference point for Channel Status, and is usually connected to the same potential as the Threshold Control. Pin 5 must be more negative than pins 10 and 11 at all times, and should be connected to $-V_{CC}$ if the Channel Status function is not used. **Status Common must be at least 5V more negative than $+V_{CC}$.**

OFFSET ADJUSTMENT

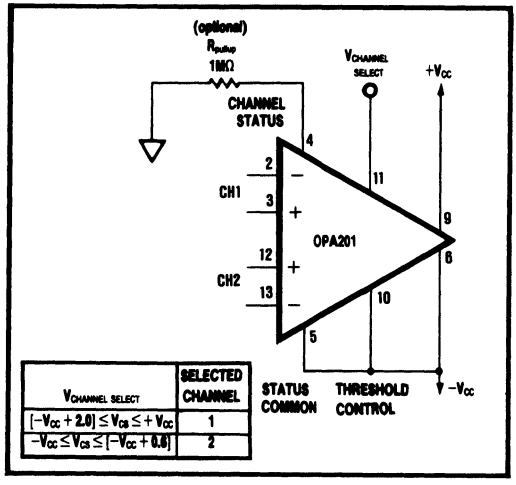
The input offset voltage is laser-trimmed and will not require user-adjustment for most applications. Pins 1 and 7 may be used to adjust the offset of the active **channel to zero (see Figure 4). This will also affect the** offset of the inactive channel (both offsets move in the same direction as the pot is adjusted). This technique may be used to make the offset for each channel equal in magnitude and opposite in polarity, which is desirable in many applications. Besides the complementary nature of the adjusted offsets, their magnitudes will now be less than one-half of the V_{os} match specification.

An inexpensive CMOS IC, CD4007 (dual-Complementary Pair Plus Inverter), may be used to alternately **connect dual-offset adjust potentiometers (see Figure 5)** allowing independent V_{os} adjustment. In this circuit, the channel status output from the Swop Amp is used to drive the CMOS logic, which connects one wiper or the



VCHANNEL SELECT	SELECTED CHANNEL
2.0 ≤ VCS ≤ +V	1
0 ≤ VCS ≤ 0.6	2

FIGURE 2. Channel Selection for Ground-Referenced Channel Select Signals.



VCHANNEL SELECT	SELECTED CHANNEL
[-Vcc + 2.0] ≤ VCS ≤ +Vcc	1
-Vcc ≤ VCS ≤ [-Vcc + 0.8]	2

FIGURE 3. Channel Selection for $-V_{CC}$ Referenced Logic Signals.

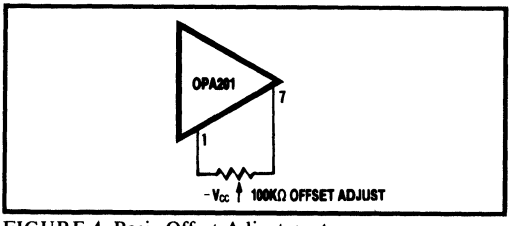


FIGURE 4. Basic Offset Adjustment.

other to $-V_{CC}$. Thus R_1 adjusts the offset of channel 1 while R_2 affects the offset only when channel 2 is selected.

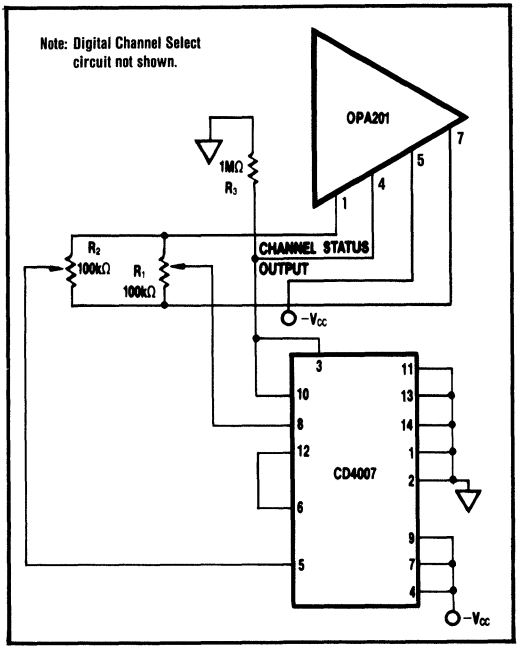


FIGURE 5. Independent Dual-Offset Adjustment.

Note: The CMOS logic requires $-V_{CC}$ (3V minimum) and common. The Status Common (pin 5) must be connected to $-V_{CC}$.

APPLICATIONS

The OPA201 is ideal for a variety of applications where a precision amplifier and switch are needed. Since the two input stages are contained on the same IC and are precision laser-trimmed, their offsets match very closely. Therefore, the OPA201 can be used as an auto-zeroing circuit as well as a dual-channel or switchable-gain amplifier. It can also be extended to become a low power 4-channel Swop Amp or dual-channel instrumentation amplifier under control of TTL level logic. General purpose and unique applications are only limited by the user's imagination.

Software auto-zeroing using the Swop Amp is easy to perform (Figure 6). One channel processes signals and the other channel has the input grounded (both channels have the same gain). The system generating the error signal may be a VFC, Iso Amp, ADC, Modulator, etc. When the zero-input channel is selected,

$$V_{out} = V_{error} + A_V V_{os2}$$

V_{error} = system error voltage
V_{os2} = Channel 2 V_{os}
A_V = Swop Amp voltage gain $= 1 + (R_2/R_1)$

When the signal channel is selected,

$$V_{out} = V_{error} + A_V V_{os1} + A_V V_{IN}$$

Subtracting the "zero" V_o from signal V_o leaves a corrected output voltage

$$V_{0ut} = A_V V_{IN} + A_V (V_{os1} - V_{os2})$$
$$= A_V (V_{IN} + \Delta V_{os})$$

Using this technique, system errors may be reduced to the V_{os} match error ($50\mu V$ untrimmed for CG grade) of the Swop Amp. Obviously the channel used for zeroing could have a voltage reference or AC waveform for gain calibration for an input, instead of ground.

Auto-zeroing may be free-running, with the Swop Amp functioning as a chopper, by connecting an oscillator to the channel select. Figure 6 shows pin 10 grounded, which allows TTL level interfacing. By programming this pin with a voltage level, other logic levels can be accommodated.

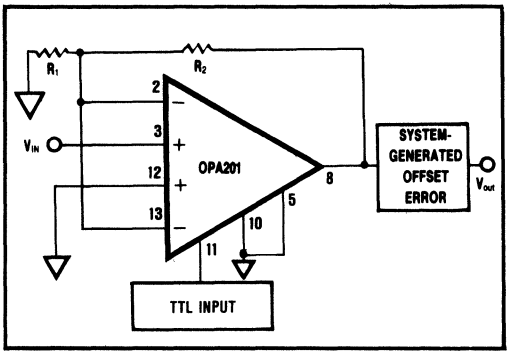


FIGURE 6. Input Amplifier for Auto-Zeroing Systems.

The OPA201 requires only external resistors to make a dual-channel amplifier (2-channel multiplexer with gain). Gain for either channel may be noninverting (Figure 7) or inverting (Figure 8) with the usual operational amplifier gain equations applying in each case. In the noninverting case, feedback is connected from the output to each input, with a common feedback resistor for equal gains. The advantage, in inverting gain circuits, is that the signal does not produce a common-mode voltage which can introduce error or input swing limitations. This is especially important in low supply voltage applications where common-mode range becomes limited. Also one channel can be noninverting and the other inverting, which is particularly useful in absolute value circuits. Note that in order to achieve the specified open-loop gain and maximum output voltage swing, the total output load including both feedback networks should not be less than $10k\Omega$ (see Figures 7 and 8).

Amplifiers with switchable transfer functions are designed much like dual-channel amplifiers, except both inputs are connected in parallel, with each channel configured for a different transfer function. Figure 9 shows a circuit that has a gain of 10 for Channel Select HIGH (channel 1 selected) and a gain of 1000 for Channel Select LOW (channel 2 selected). In this case, the channel select may be thought of as a gain select.

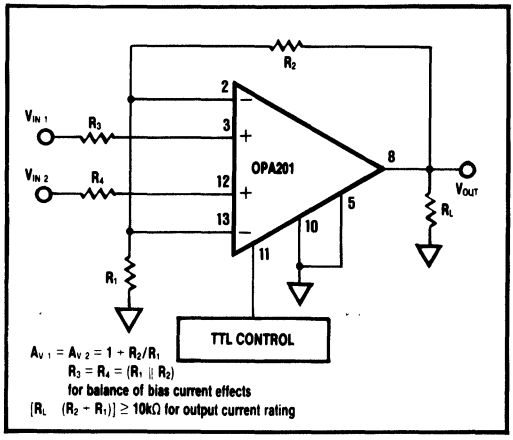


FIGURE 7. Selectable Input Amplifier, Noninverting.

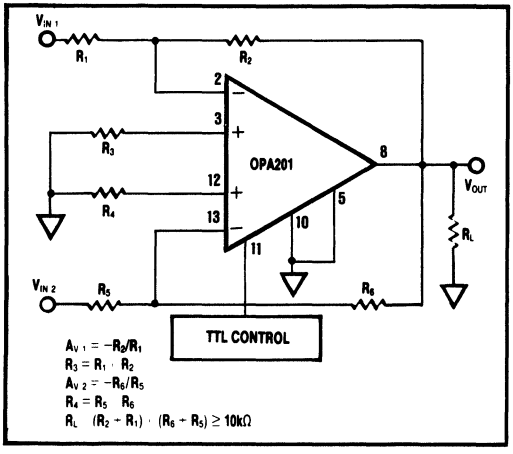


FIGURE 8. Selectable Input Amplifier, Inverting.

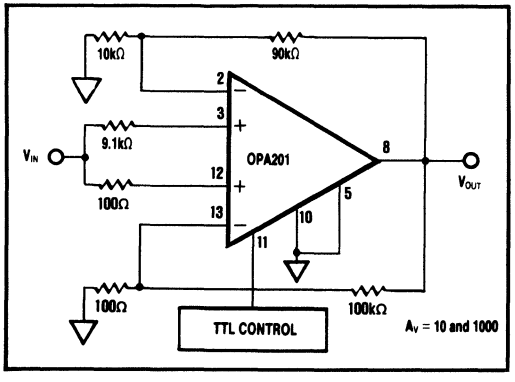


FIGURE 9. Switchable Gain Amplifier.

This concept also applies to switchable bandwidth circuits, where AC coupling (high-pass) or smoothing (low-pass) characteristics need to be switched in under digital control. A wide variety of operational amplifier function circuits may be made selectable or switchable using these techniques.

Figure 10 shows a two-channel differential amplifier. This concept can be expanded to a full high input impedance instrumentation amplifier by adding four input buffer amplifiers or by using two front end Swop Amps followed by an operational amp (Figure 11).

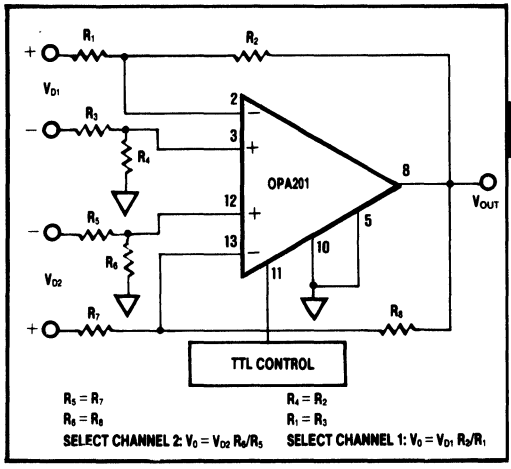


FIGURE 10. Low Power Dual-Channel Differential Amplifier.

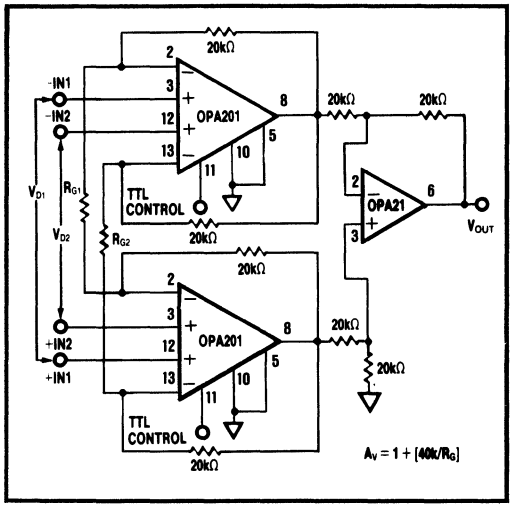
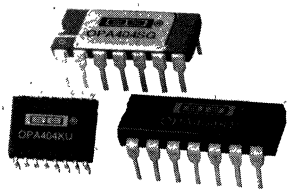


FIGURE 11. Low Power Dual-Channel Instrumentation Amplifier.

BURR-BROWN®



OPA404

MILITARY & DIE VERSIONS AVAILABLE

Quad High-Speed Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 6.4MHz
- HIGH SLEW RATE: 35V/μs
- LOW OFFSET: ±750μV max
- LOW BIAS CURRENT: ±4pA max
- FAST SETTLING: 1.5μs to 0.01%
- STANDARD QUAD PINOUT

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DETECTOR ARRAYS

DESCRIPTION

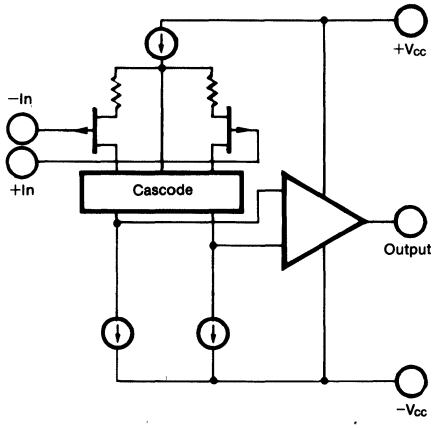
The OPA404 is a high performance monolithic *Difet*® (dielectrically-isolated FET) quad operational amplifier. It offers an unusual combination of very-low bias current together with wide bandwidth and fast slew rate.

Noise, bias current, voltage offset, drift, and speed are superior to BIFET® amplifiers.

Laser trimming of thin-film resistors gives very-low offset and drift—the best available in a quad FET op amp.

The OPA404's input cascode design allows high precision input specifications and uncompromised high-speed performance.

Standard quad op amp pin configuration allows upgrading of existing designs to higher performance levels. The OPA404 is unity-gain stable.



OPA404 Simplified Circuit
(Each Amplifier)

Difet® Burr-Brown Corp., BIFET® National Semiconductor Corp.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-677B

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA404AG, KP, KU			OPA404BG			OPA404SG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
NOISE[1]											
Voltage: f_O = 10Hz			32			*			*		nV/√Hz
f_O = 100Hz			19			*			*		nV/√Hz
f_O = 1kHz			15			*			*		nV/√Hz
f_O = 10kHz			12			*			*		nV/√Hz
f_B = 10Hz to 10kHz			1 4			*			*		μV, rms
f_B = 0 1Hz to 10Hz			0 95			*			*		μV, p-p
Current f_B = 0 1Hz to 10Hz			12			*			*		fA, p-p
f_O = 0 1Hz to 20kHz			0.6			*			*		fA/√Hz
OFFSET VOLTAGE											
Input Offset Voltage	V_{CM} = 0VDC		±260	±1mV		*	±750		*	*	μV
KP, KU			±750	±2.5mV							μV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3			*			*		μV/°C
KP			±5								μV/°C
Supply Rejection	±V_{CC} = 12V to 18V	80	100		86	*		*	*		dB
KP, KU		76	100								dB
Channel Separation	100Hz, R_L = 2kΩ		125			*			*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		±1	±8		*	±4		*	*	pA
KP, KU			±1	±12							pA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.5	8		*	4		*	*	pA
KP, KU			0 5	12							pA
IMPEDANCE											
Differential			10^{13} ‖ 1			*			*		Ω ‖ pF
Common-Mode			10^{14} ‖ 3			*			*		Ω ‖ pF
VOLTAGE RANGE											
Common-Mode Input Range		±10 5	+13, −11		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±10VDC	88	100		92	*		*	*		dB
KP, KU		84	100								dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq$ 2kΩ	88	100		92	*		*	*		dB
FREQUENCY RESPONSE											
Gain Bandwidth	Gain = 100	4	6 4		5	*		*	*		MHz
Full Power Response	20V p-p, R_L = 2kΩ		570			*			*		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	24	35		28	*		*	*		V/μs
Settling Time 0 1%	Gain = −1, R_L = 2kΩ		0 6			*			*		μs
0 01%	C_L = 100pF, 10V step		1.5			*			*		μs
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11 5	+13.2, −13.8		*	*		*	*		V
Current Output	V_O = ±10VDC	±5	±10		*	*		*	*		mA
Output Resistance	1MHz, open loop		80			*			*		Ω
Load Capacitance Stability	Gain = +1		1000			*			*		pF
Short Circuit Current		±10	±18	±20	*	*	*	*	*	*	mA
POWER SUPPLY											
Rated Voltage			±15			*			*		VDC
Voltage Range, Derated Performance		±5		±18	*		*	*		*	VDC
Current, Quiescent	I_O = 0mADC		9	10		*	*		*	*	mA
TEMPERATURE RANGE											
Specification	Ambient temp	−25		+85	*		*	−55		+125	°C
KP, KU		0		+70							°C
Operating	Ambient temp	−55		+125	*		*	*		*	°C
KP, KU		−25		+85							°C
Storage	Ambient temp	−65		+150	*		*	*		*	°C
θ Junction-Ambient			100			*			*		°C/W
KP, KU			120/100								°C/W

*Specification same as OPA404AG

NOTES: (1) Noise testing available—inquire

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA404AG, KP, KU			OPA404BG			OPA404SG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification Range	Ambient temp.	–25		+85	*		*	–55		+125	°C
KP, KU		0		+70							°C
INPUT											
OFFSET VOLTAGE											
Input Offset Voltage	V_{CM} = 0VDC		±450	2mV		*	±1.5mV		±550	±2.5mV	µV
KP, KU			±1	±3.5							mV
Average Drift			±3			*			*		µV/°C
KP, KU			±5								µv/°C
Supply Rejection		75	96		80	*		70	93		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		±32	±200		*	±100		±500	±5nA	pA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		17	100		*	50		260	2 5nA	pA
VOLTAGE RANGE											
Common-Mode Input Range		±10 2	+12 7, –10 6		*	*		±10	+12.6, –10 5		V
Common-Mode Rejection	V_{IN} = ±10VDC	82	99		86	*		80	88		dB
KP, KU		80	99								dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	82	94		86	*		80	88		dB
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11.5	+12 9, –13.8		*	*		±11	+12 7, –13 8		V
Current Output	V_O = ±10VDC	±5	±9		*	*		*	±8		mA
Short Circuit Current	V_O = 0VDC	±5	±12	±30	*	*	*	±8	±10	*	mA
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		9 3	10 5		*	*		9 4	11	mA

*Specification same as OPA404AG.

ORDERING INFORMATION

OPA404 ( ) ( )

- Basic model number
- Performance grade
  - K = 0°C to +70°C
  - A, B = –25°C to +85°C
  - S = –55°C to +125°C
- Package code
  - G = 14-pin ceramic DIP
  - P = 14-pin plastic DIP
  - U = 16-Pin plastic SOIC

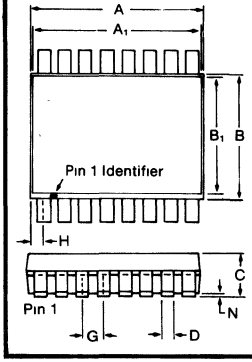
ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	1000mW
Differential Input Voltage[2]	±36VDC
Input Voltage Range[2]	±18VDC
Storage Temperature Range	P, U = –40/+85°C, G = –65/+150°C
Operating Temperature Range	P, U = –25/+85°C, G = –55/+125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[3]	Continuous
Junction Temperature	+175°C

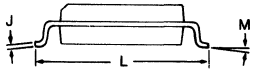
NOTES:
(1) Packages must be derated based on θ_{JC} = 30°C/W or θ_{JA} = 120°C/W
(2) For supply voltages less than ±18VDC the absolute maximum input voltage is equal to. 18V > V_{IN} > $-V_{CC}$ – 8V. See Figure 2.
(3) Short circuit may be to power supply common only Rating applies to +25°C ambient Observe dissipation limit and T_J

MECHANICAL

"U" (SOIC) Package



NOTE. Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

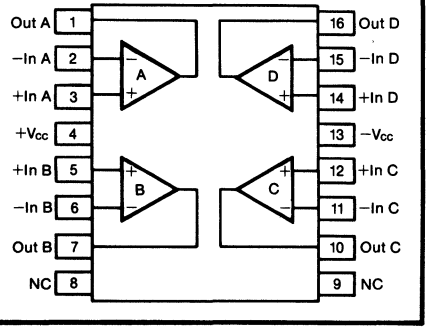


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	400	416	10 16	10 57
A_1	388	412	9 86	10 46
B	286	302	7 26	7 67
B_1	268	286	6 81	7 26
C	093	109	2 36	2.77
D	015	.020	0 38	0 51
G	050 BASIC		1 27 BASIC	
H	022	038	0 56	0 97
J	.008	012	0 20	0.30
L	391	421	9 93	10 69
M	5° TYP		5° TYP	
N	000	012	0 00	0 30

PIN CONFIGURATION

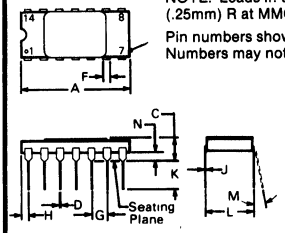
Top View

"U" (SOIC) Package



MECHANICAL

"G" Package



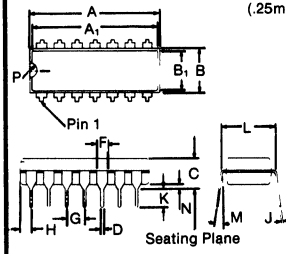
NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	710	17.02	18 03
C	.065	170	1.65	4.32
D	.015	.021	0 38	0.53
F	.045	060	1 14	1 52
G	100 BASIC		2 54 BASIC	
H	025	.070	0.64	1 78
J	.008	.012	0.20	0.30
K	120	240	3.05	6 10
L	.300 BASIC		7 62 BASIC	
M	—	10°	—	10°
N	.009	060	0.23	1 52

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

"P" Package



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane

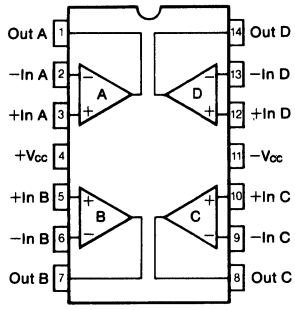
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.700	.800	17.78	20.32
A_1	.685	.785	17.40	19 94
B	.230	.290	5 85	7 38
B_1	.200	.250	5 09	6.36
C	.120	.200	3 05	5 09
D	.015	023	0.38	0.59
F	.030	.070	0.76	1 78
G	.100 BASIC		2.54 BASIC	
H	.050	100	1 27	2 54
J	008	.015	0 20	0.38
K	070	150	1 78	3 82
L	300 BASIC		7 63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0 25	0 76
P	025	050	0 64	1.27

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

CONNECTION DIAGRAM

Top View

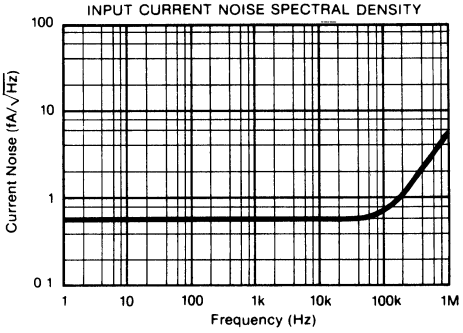
"G" or "P" (DIP) Package



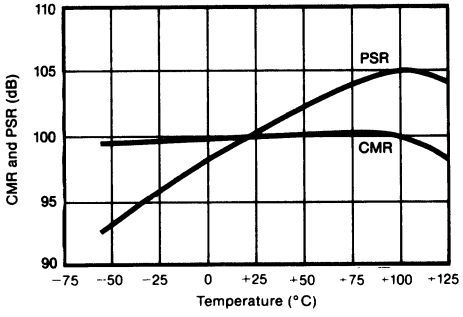
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted

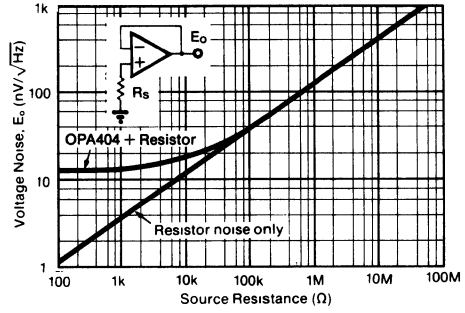
INPUT CURRENT NOISE SPECTRAL DENSITY



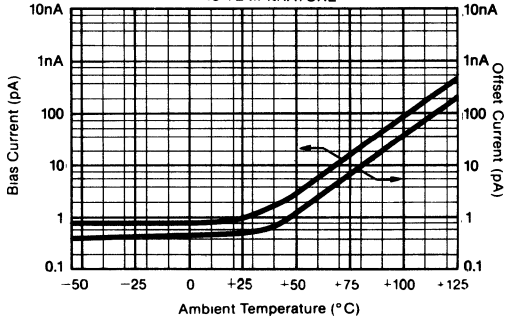
POWER SUPPLY REJECTION AND COMMON-MODE REJECTION vs TEMPERATURE



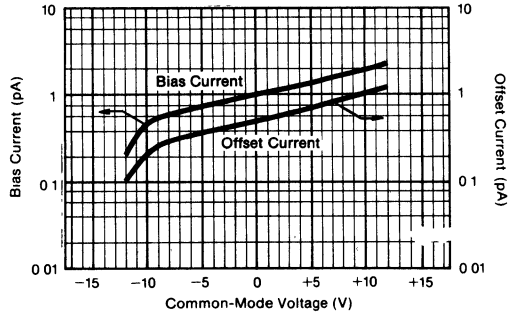
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



BIAS AND OFFSET CURRENT vs TEMPERATURE



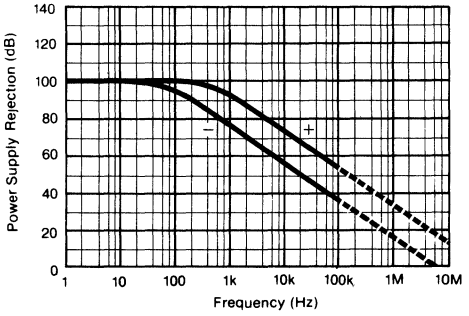
BIAS AND OFFSET CURRENT vs INPUT COMMON MODE VOLTAGE



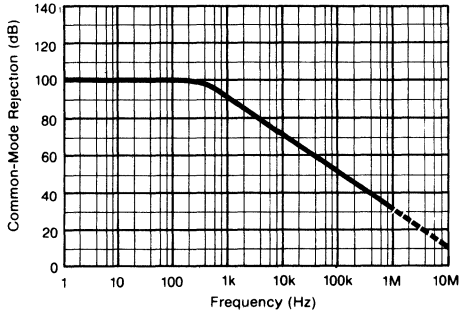
TYPICAL PERFORMANCE CURVES [CONT]

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted

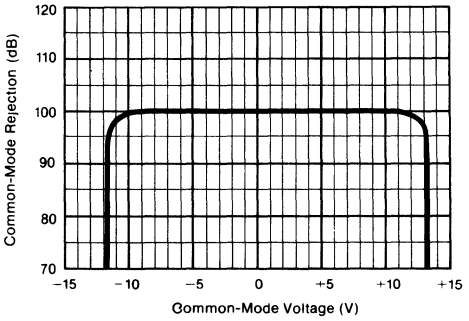
POWER SUPPLY REJECTION vs FREQUENCY



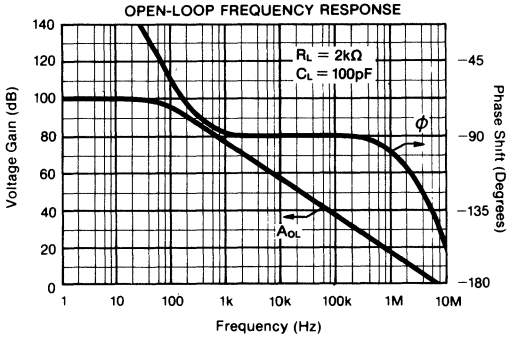
COMMON-MODE REJECTION vs FREQUENCY



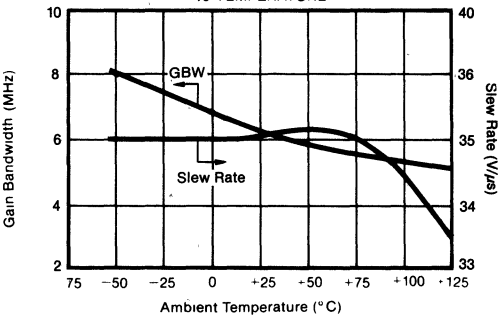
COMMON-MODE REJECTION vs INPUT COMMON MODE VOLTAGE



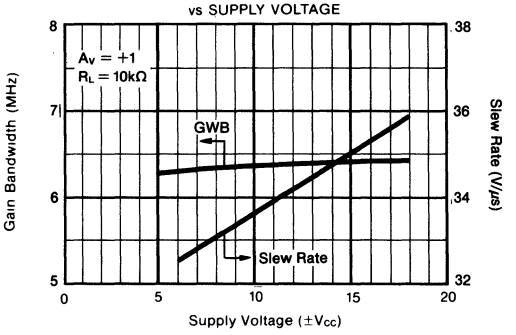
OPEN-LOOP FREQUENCY RESPONSE



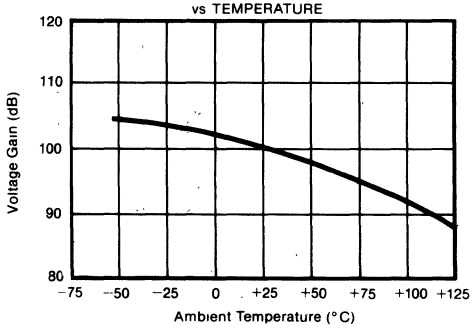
GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



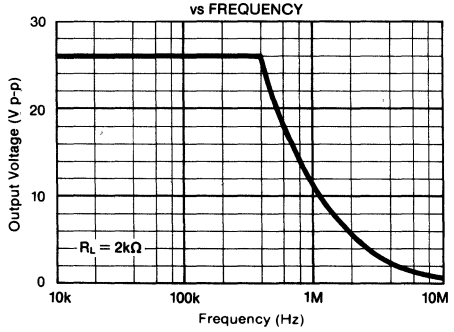
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



OPEN-LOOP GAIN vs TEMPERATURE



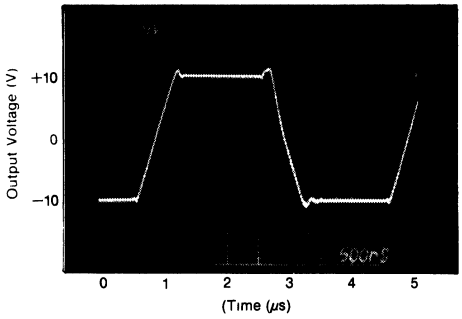
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



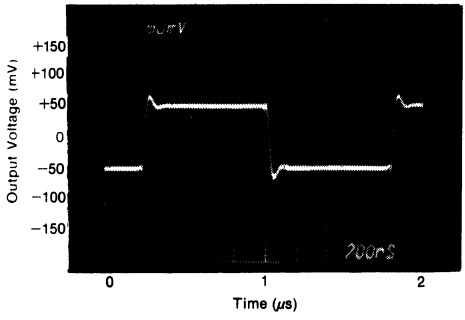
TYPICAL PERFORMANCE CURVES [CONT]

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted

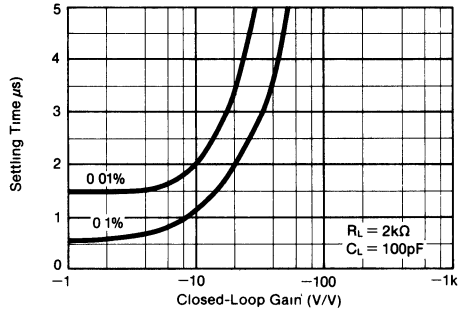
LARGE SIGNAL TRANSIENT RESPONSE



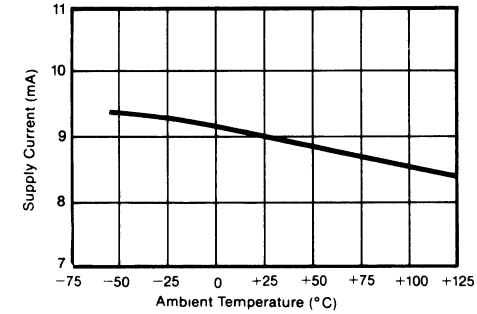
SMALL SIGNAL TRANSIENT RESPONSE



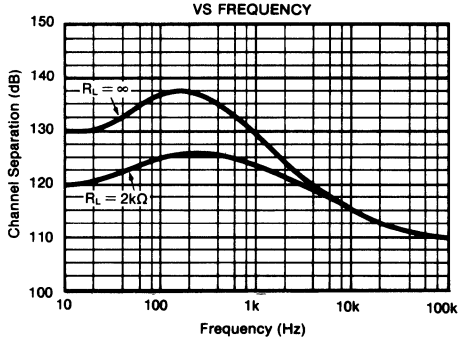
SETTLING TIME vs CLOSED-LOOP GAIN



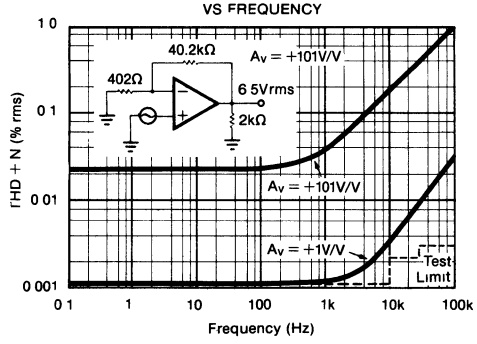
SUPPLY CURRENT vs TEMPERATURE



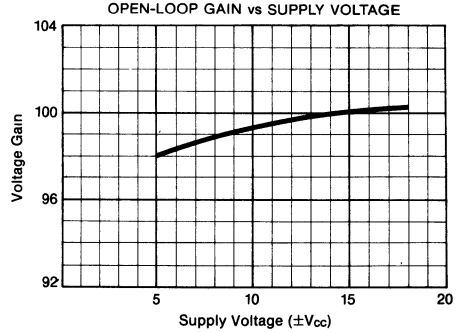
CHANNEL SEPARATION VS FREQUENCY



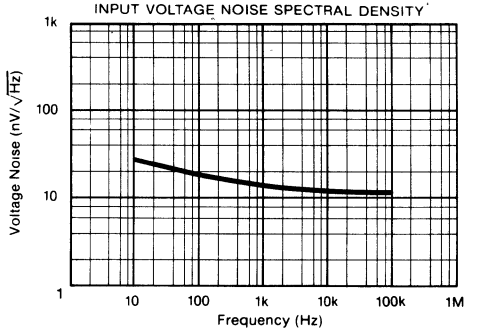
TOTAL HARMONIC DISTORTION VS FREQUENCY



OPEN-LOOP GAIN vs SUPPLY VOLTAGE



INPUT VOLTAGE NOISE SPECTRAL DENSITY



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA404 offset voltage is laser-trimmed and will require no further trim for most applications. If desired, offset voltage can be trimmed by summing (see Figure 1). With this trim method there will be no degradation of input offset drift.

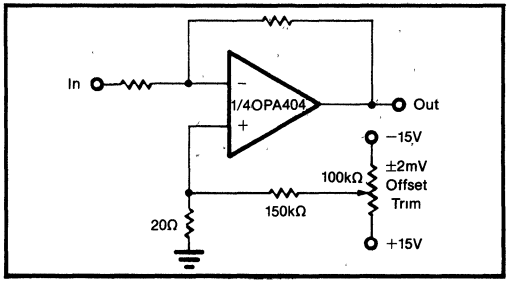


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET® amplifiers can be destroyed by the loss of $-V_{CC}$

Unlike BIFET® amplifiers, the ***Difet***® OPA404 requires input current limiting resistors only if its input voltage can exceed −8V. A 10kΩ series resistor will limit the input current to a safe value with up to ±15V input levels even if both supply voltages are lost. (See Figure 2 and Absolute Maximum Ratings).

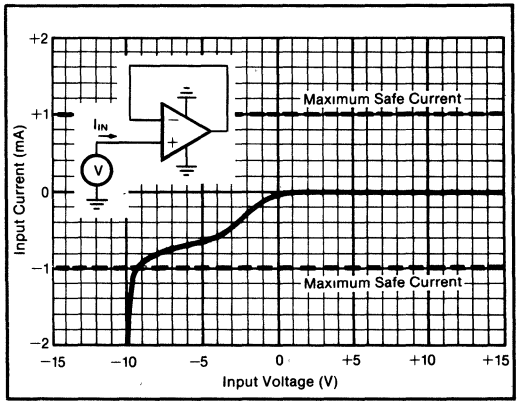


FIGURE 2. Input Current vs Input Voltage with $\pm V_{CC}$ Pins Grounded.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA404. To avoid leakage, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input ptotential (see Figure 3).

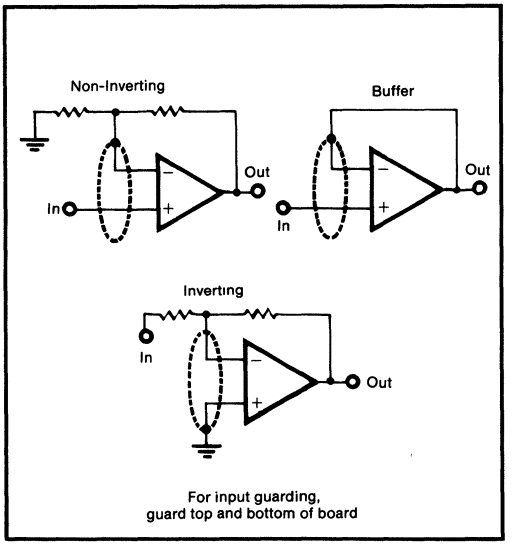


FIGURE 3. Connection of Input Guard.

HANDLING AND TESTING

Measuring the unusually low bias current of the OPA404 is difficult without specialized test equipment; most commercial benchtop testers cannot accurately measure the OPA404 bias current. Low-leakage test sockets and special test fixtures are recommended if incoming inspection of bias current is to be performed.

To prevent surface leakage between pins, the DIP package should not be handled by bare fingers. Oils and salts from fingerprints or careless handling can create leakage currents that exceed the specified OPA404 bias currents.

If necessary, DIP packages and PC board assemblies can be cleaned with Freon TF®, baked for 30 minutes at 85°C, rinsed with de-ionized water, and baked again for 30 minutes at 85°C. Surface contamination can be prevented by the application of a high-quality conformal coating to the cleaned PC board assembly.

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET® operational amplifiers are affected by common-mode voltage (Figure 4). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely-low bias current of the OPA404 is not compromised by common-mode voltage.

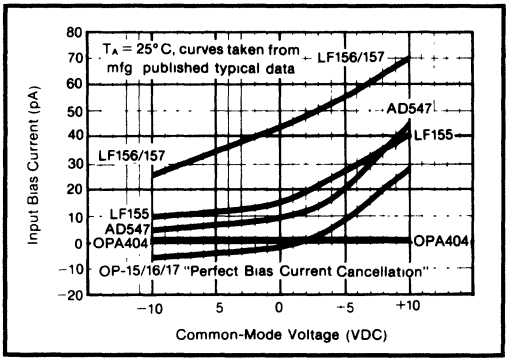


FIGURE 4. Input Bias Current Versus Common-Mode Voltage.

APPLICATIONS CIRCUITS

Figures 5 through 11 are circuit diagrams of various applications for the OPA404.

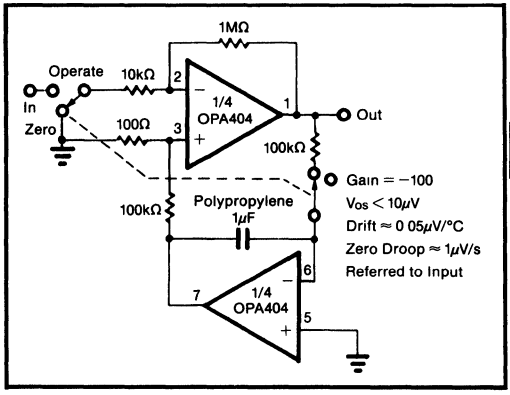


FIGURE 5. Auto-Zero Amplifier.

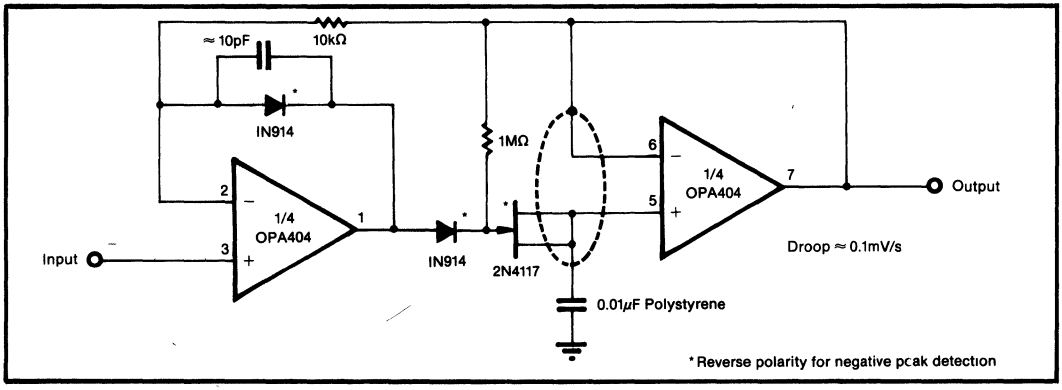


FIGURE 6. Low-Droop Positive Peak Detector.

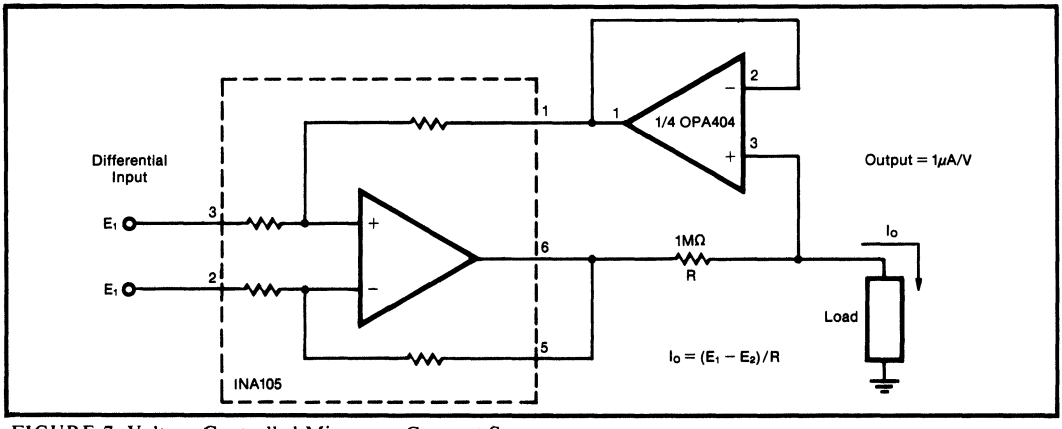


FIGURE 7. Voltage-Controlled Microamp Currrent Source.

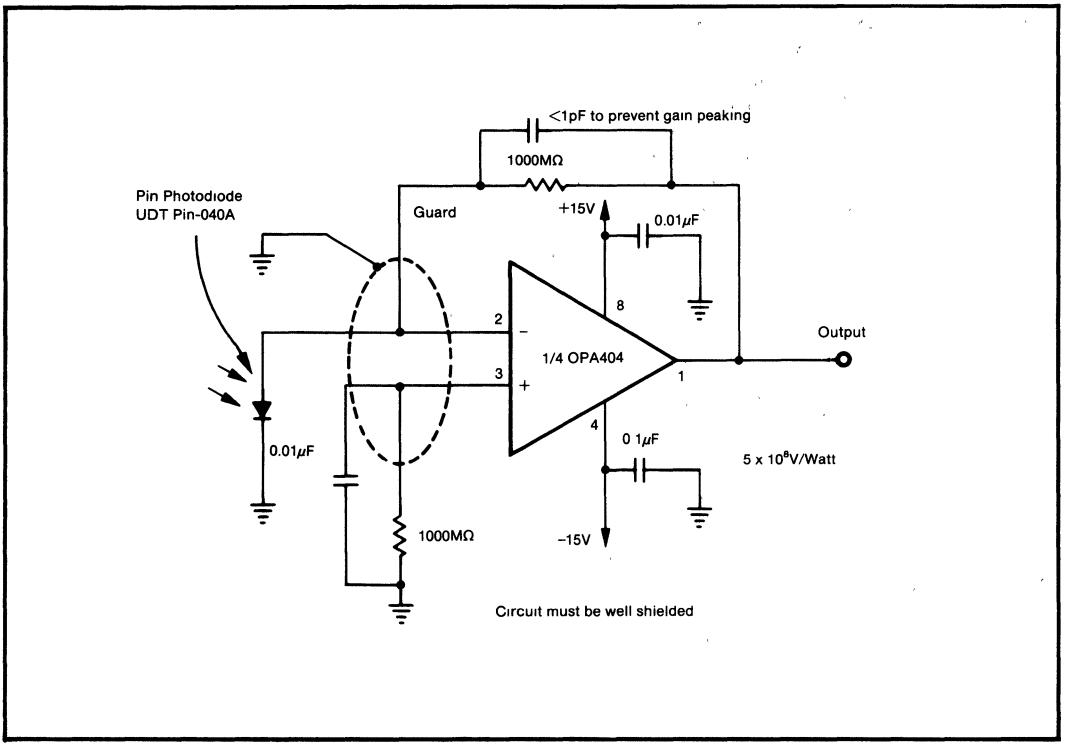


FIGURE 8. Sensitive Photodiode Amplifier.

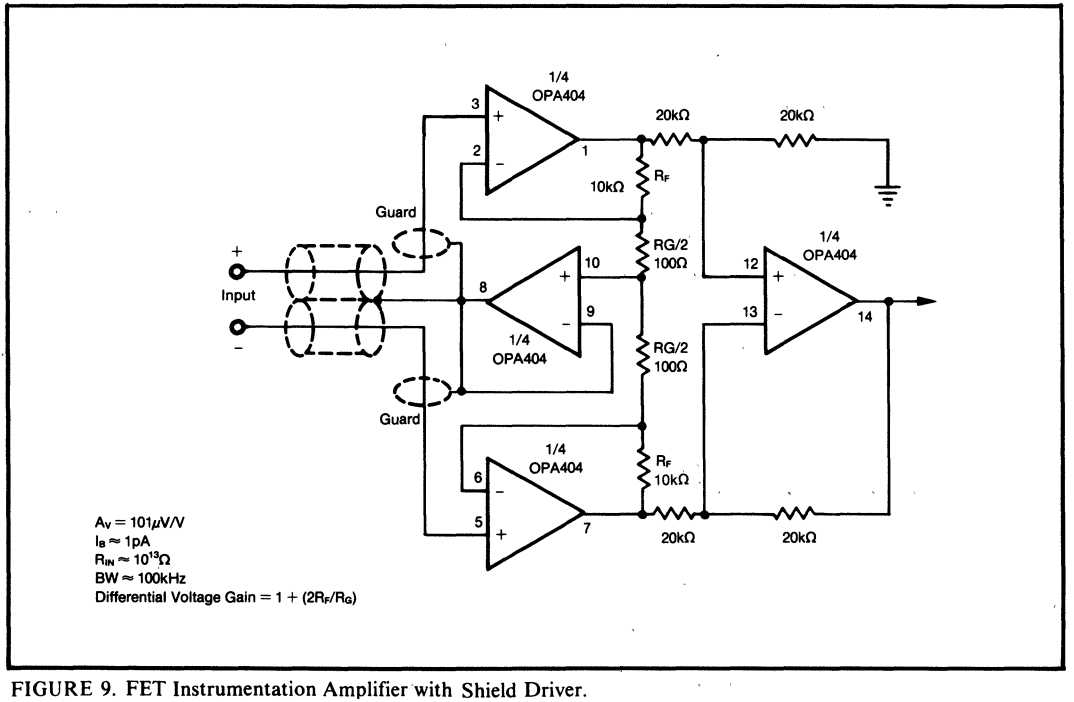


FIGURE 9. FET Instrumentation Amplifier with Shield Driver.

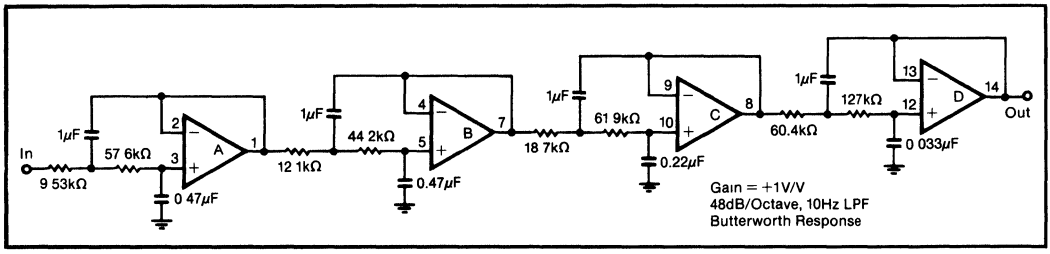


FIGURE 10. 8-Pole 10Hz Low-Pass Filter.

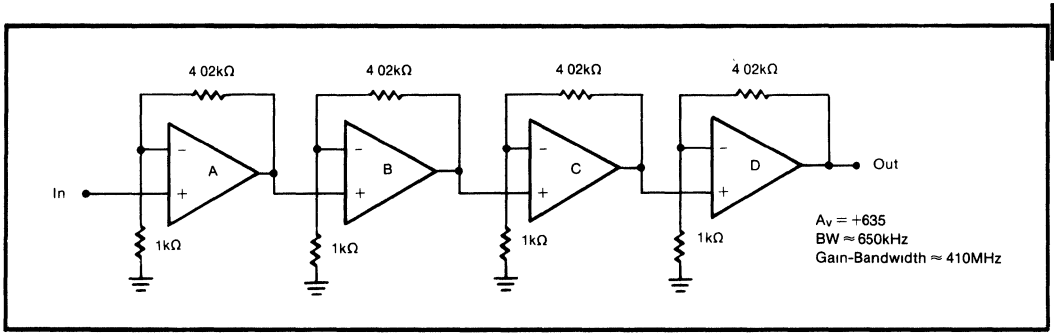
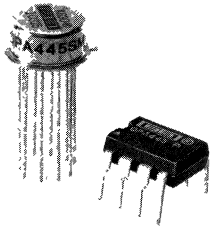


FIGURE 11. Wide-Band Amplifier

BURR-BROWN®



OPA445

MILITARY VERSION AVAILABLE

High Voltage FET-Input OPERATIONAL AMPLIFIER

FEATURES

- WIDE POWER SUPPLY RANGE: ±10V to ±45V
- HIGH SLEW RATE: 10V/μs
- LOW INPUT BIAS CURRENT: 50pA max
- STANDARD-PINOUT TO-99 AND DIP PACKAGES

APPLICATIONS

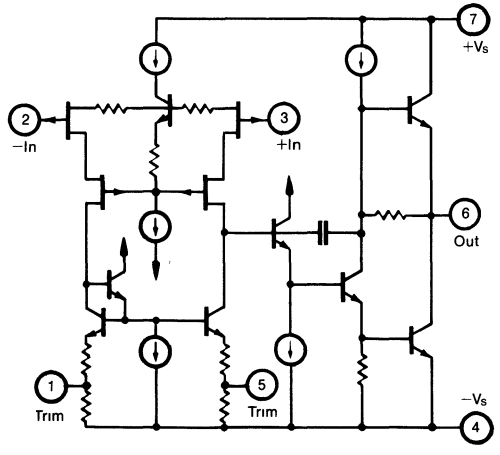
- TEST EQUIPMENT
- HIGH VOLTAGE REGULATORS
- POWER AMPLIFIERS
- DATA ACQUISITION
- SIGNAL CONDITIONING

DESCRIPTION

The OPA445 is a monolithic operational amplifier capable of operation from power supplies up to ±45V and output currents of 15mA. It is useful in a wide variety of applications requiring high output voltage or large common-mode voltage swings.

The OPA445's high slew rate provides wide power-bandwidth response, which is often required for high voltage applications. FET input circuitry allows the use of high impedance feedback networks, thus minimizing their output loading effects. Laser trimming of the input circuitry yields low input offset voltage and drift.

The OPA445 is unity-gain stable and requires no external compensation components. It is available in both industrial (−25°C to +85°C) and military (−55°C to +125°C) temperature ranges.



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PDS-754A

SPECIFICATIONS

ELECTRICAL

At $V_S = \pm 40V$ and $T_A = +25°C$ unless otherwise specified

PARAMETER	CONDITIONS	OPA445SM			OPA445BM			OPA445AP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
OFFSET VOLTAGE											
Input Offset Voltage	$V_{CM} = 0V$		0 5	1 0		1 0	3 0		2 0	5 0	mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		*			10			15		µV/°C
Supply Rejection	$V_S = \pm 10V$ to $\pm 50V$	*	*		80	110		*	*		dB
BIAS CURRENT											
Input Bias Current	$V_{CM} = 0V$		*	*		20	50		50	100	pA
Over Temperature				100			10			20	nA
OFFSET CURRENT											
Input Offset Current	$V_{CM} = 0V$		*	*		4	10		20	40	pA
Over Temperature				50			5			10	nA
IMPEDANCE											
Differential			*			$10^{13} \parallel 1$			*		Ω ‖ pF
Common-Mode			*			$10^{14} \parallel 3$			*		Ω ‖ pF
VOLTAGE RANGE											
Common-Mode Input Range		*			±35			*			V
Common-Mode Rejection	$V_{IN} = \pm 30V$,										
	Over temp	*	*		80	95		*	*		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L = 5k\Omega$	*	*		100	105		*	*		dB
Over Temperature		*			97			*			dB
FREQUENCY RESPONSE											
Gain Bandwidth	Small signal		*			2			*		MHz
Full Power Response	35Vp-p, $R_L = 5k\Omega$	*	*		45	55		*	*		kHz
DYNAMIC RESPONSE											
Slew Rate	$V_O = \pm 35V$,										
	$R_L = 5k\Omega$	*	*		5	10		*	*		V/µs
Rise Time	$V_O = \pm 200mV$		*			100			*		ns
Overshoot	$A_V = +1$										
	$Z_L = 5k\Omega \parallel 50pF$		*			30			*		%
RATED OUTPUT											
Voltage Output, over temp	$R_L = 5k\Omega$	*			±35			*			V
Current Output	$V_O = \pm 28V$	*			±15			*			mA
Output Resistance	DC, open loop		*			220			*		Ω
Short Circuit Current			*			±26			*		mA
POWER SUPPLY											
Rated Voltage, $\pm V_S$			*			±40			*		V
Voltage Range, $\pm V_S$											
Derated Performance	Over temp	*		*	±10		±45	*		*	V
Current, Quiescent	$I_O = 0mA$		*	*		3 8	4 5		*	*	mA
TEMPERATURE RANGE											
Specification		−55		+125	−25		+85	*		*	°C
Operating	Ambient temp	*		*	−55		+125	−25		+85	°C
θ Junction-Ambient			*			200			100		°C/W

*Specification same as OPA445BM

ORDERING INFORMATION

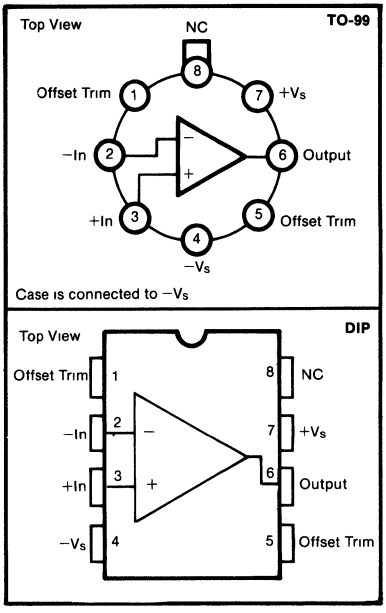
OPA445 ( ) ( )

- Basic model number
- Performance grade (blank indicates A grade)
  - A −25°C to +85°C
  - B −25°C to +85°C
  - S −55°C to +125°C
- Package code
  - M 8-pin TO-99
  - P 8-pin plastic DIP

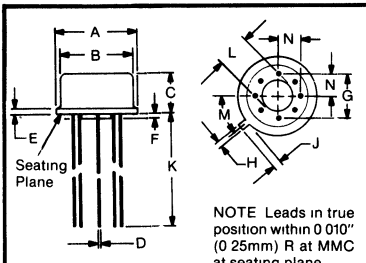
ABSOLUTE MAXIMUM RATINGS

Power Supply	±50V
Internal Power Dissipation	680mW
Differential Input Voltage	±80V
Input Voltage Range	$\lvert\pm V_S\rvert - 3V$
Storage Temperature Range M	−65°C to +150°C
P	−40°C to +85°C
Operating Temperature Range M	−55°C to +125°C
P	−40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short-Circuit to Ground ($T_A = +25°C$)	Continuous
Junction Temperature	+175°C

CONNECTION DIAGRAMS

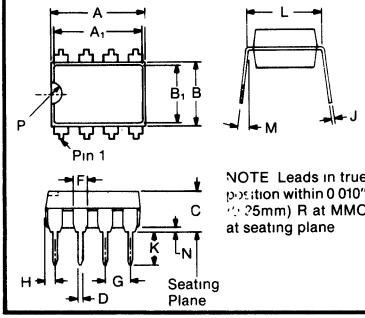


MECHANICALS



NOTE Leads in true position within 0.010" (0.25mm) R at MMC at seating plane

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	335	370	8.51	9.40
B	305	335	7.75	8.51
C	165	185	4.19	4.70
D	016	021	0.41	0.53
E	010	040	0.25	1.02
F	010	040	0.25	1.02
G	200 BASIC		5.08 BASIC	
H	028	034	0.71	0.86
J	029	045	0.74	1.14
K	500	—	12.7	—
L	110	160	2.79	4.06
M	45° BASIC		45° BASIC	
N	095	105	2.41	2.67



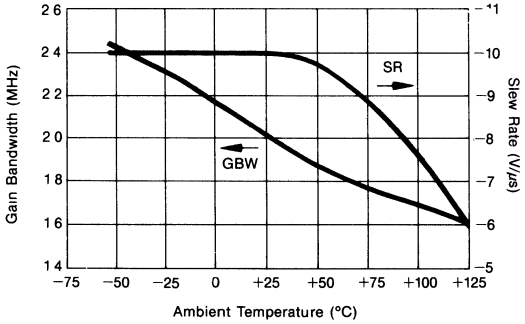
NOTE Leads in true position within 0.010" (0.25mm) R at MMC at seating plane

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	355	400	9.03	10.16
A_1	340	385	8.65	9.80
B	230	290	5.85	7.38
B_1	200	250	5.09	6.36
C	120	200	3.05	5.09
D	015	023	0.38	0.59
F	030	070	0.76	1.78
G	100 BASIC		2.54 BASIC	
H	025	050	0.64	1.27
J	008	015	0.20	0.38
K	070	150	1.78	3.82
L	300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	010	030	0.25	0.76
P	025	050	0.64	1.27

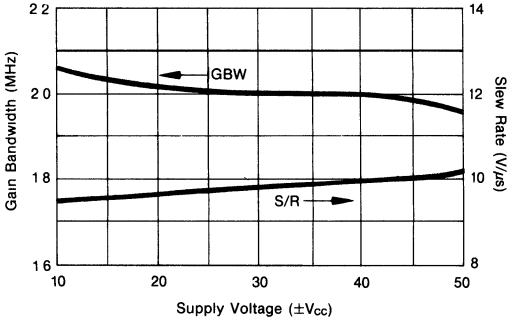
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15VDC unless otherwise noted

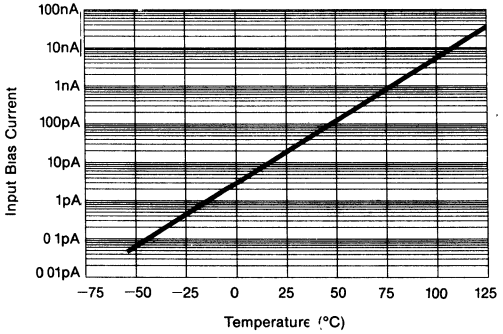
GAIN BANDWIDTH AND SLEW RATE VS TEMPERATURE



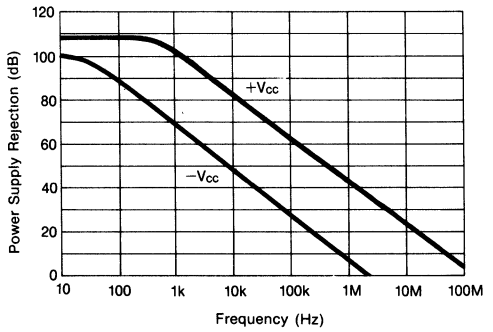
GAIN BANDWIDTH AND SLEW RATE VS SUPPLY VOLTAGE



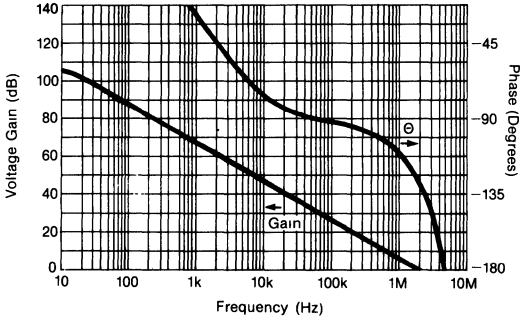
INPUT BIAS CURRENT VS TEMPERATURE



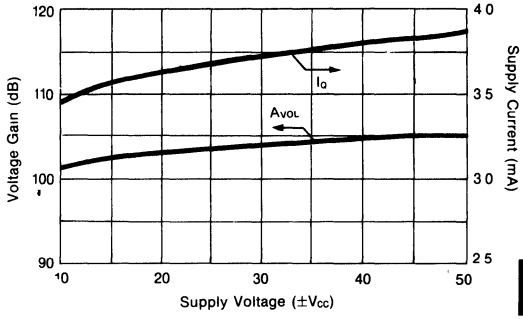
POWER SUPPLY REJECTION VS FREQUENCY



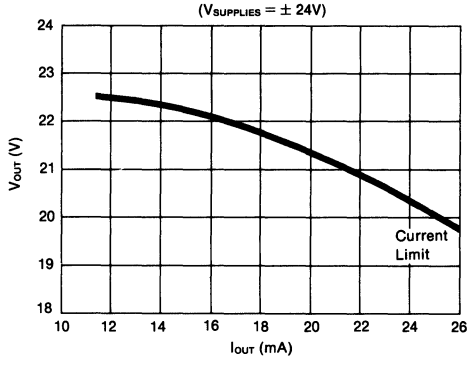
OPEN-LOOP
FREQUENCY RESPONSE



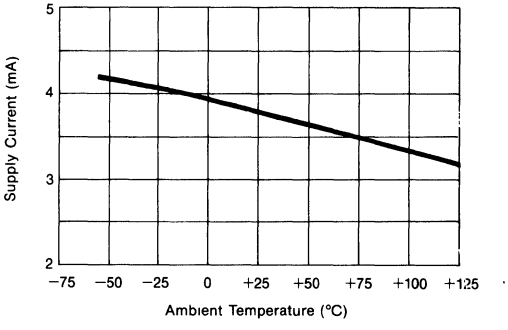
OPEN-LOOP GAIN AND SUPPLY CURRENT
VS SUPPLY VOLTAGE



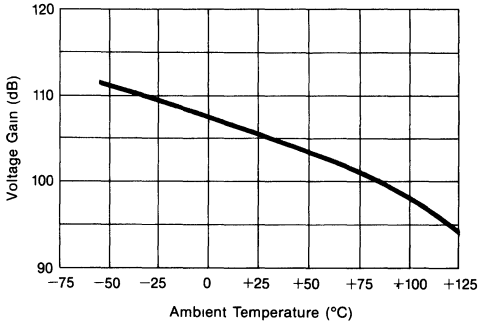
OUTPUT VOLTAGE vs OUTPUT CURRENT
($V_{SUPPLIES}$ = ± 24V)



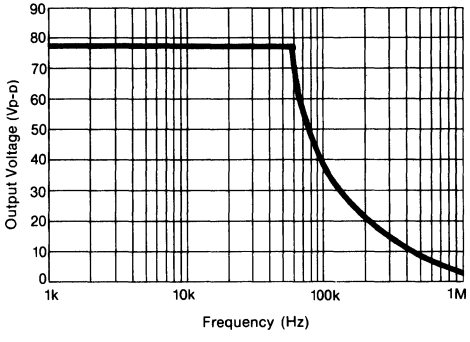
SUPPLY CURRENT VS TEMPERATURE



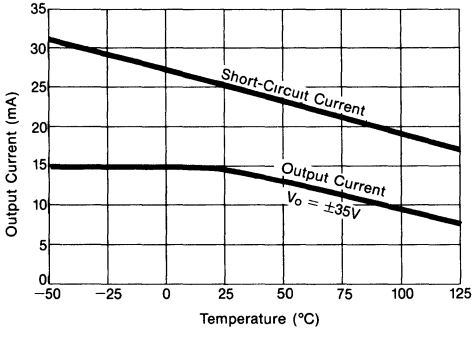
OPEN-LOOP GAIN VS TEMPERATURE



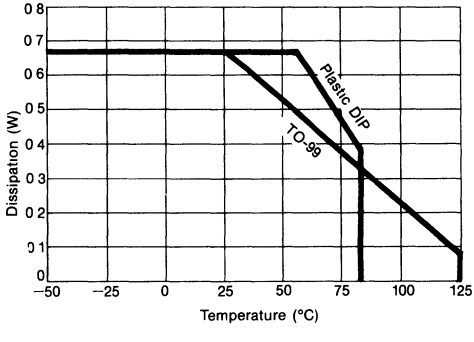
MAXIMUM OUTPUT VOLTAGE SWING
VS FREQUENCY

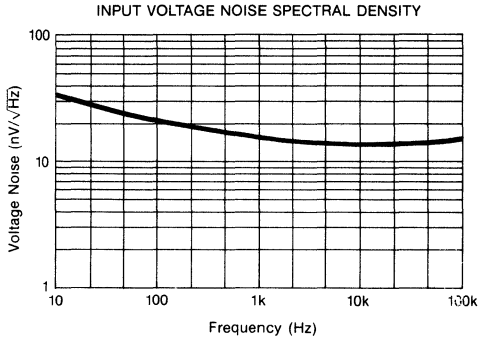


OUTPUT CURRENT VS TEMPERATURE



MAXIMUM POWER DISSIPATION VS TEMPERATURE





INSTALLATION AND OPERATING INSTRUCTIONS

The OPA445 may be operated from power supplies up to ±45V or a total of 90V. Power supplies should be bypassed with 0.022μF capacitors, or greater, near the power supply pins. Be sure that the capacitors are appropriately rated for the supply voltage used.

The OPA445 can supply output currents of 15mA and larger. This would present no problem for a standard op amp operating from ±15V supplies. With high supply voltages, however, internal power dissipation of the op amp can be quite large. Operation from a single power supply (or unbalanced power supplies) can produce even larger power dissipation since a larger voltage is impressed across the conducting output transistor.

Dissipation should be limited to 680mW at 25°C. At temperatures above 25°C, the maximum dissipation should be derated according to the thermal resistance of the package type used.

Package thermal resistance, θ_{JC}, is affected by mounting techniques and environments. The figures provided are typical for common mounting configurations with convection air flow. Poor air circulation and use of sockets can signficantly increase thermal resistance. Best thermal performance is achieved by soldering the op amp into a circuit board with wide printed circuit traces to allow greater conduction through the op amp leads. Simple clip-on heat sinks can reduce the thermal resistance of the TO-99 metal package by as much as 50°C/W.

A short-circuit to ground will produce a typical output current of 25mA. With ±40V power supplies, this creates an internal power dissipation of 1.0W. This exceeds the maximum rating for the device, and is not recommended. Permanent damage is unlikely, however, since the short-circuit output current will diminish as the junction temperature rises.

TYPICAL APPLICATIONS

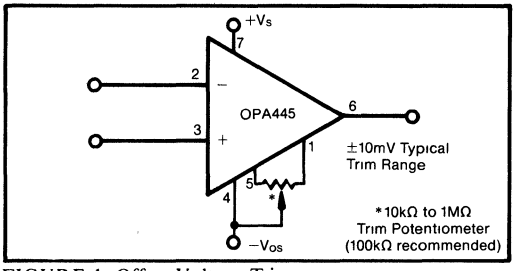


FIGURE 1. Offset Voltage Trim.

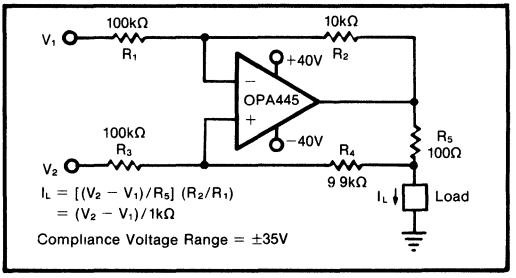


FIGURE 2. Voltage-to-Current Converter.

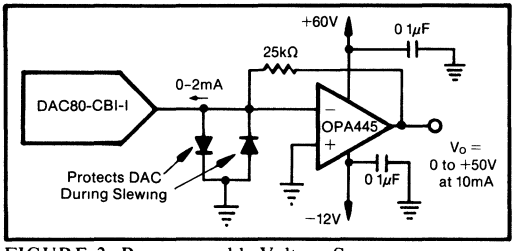


FIGURE 3. Programmable Voltage Source.

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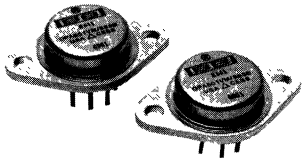


OPA501

MILITARY VERSION AVAILABLE

High Current - High Power OPERATIONAL AMPLIFIER

FEATURES

- WIDE SUPPLY RANGE ±10 to ±40 Volts
- HIGH OUTPUT CURRENT ±10 Amps Peak
- HIGH OUTPUT POWER 260 Watts Peak
- SMALL SIZE: TO-3 PACKAGE

APPLICATIONS

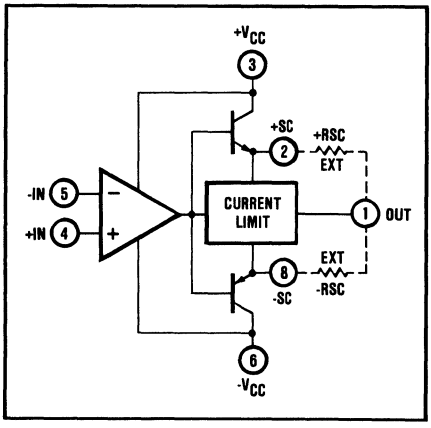
- SERVO AMPLIFIER
- MOTOR DRIVER
- ACTUATOR CONTROL
- AUDIO AMPLIFIER
- SYNCRO DRIVER
- POWER SUPPLY REGULATOR

DESCRIPTION

The OPA501 is a high power operational amplifier. Its high current output stage delivers ±10A yet the amplifier is unity-gain stable and it can be used in any operational amplifier configuration. The 260W peak output capability allows the OPA501 to drive loads (such as motors) with a greater safety margin.

Safe operating area is fully specified and output current limiting is provided to protect both the amplifier and the load from excessive current.

This hybrid IC is housed in an 8-pin hermetic TO-3 package. The electrically-isolated package allows direct mounting to chassis or heat sink without an insulating washer or spacer which would increase thermal resistance.



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PDS-490D

SPECIFICATIONS

ELECTRICAL

At T_C = +25°C and $\pm V_{CC}$ = 28VDC (OPA501RM/AM), $\pm V_{CC}$ = 34VDC (OPA501SM/BM) unless otherwise noted.

PARAMETER	CONDITIONS	OPA501RM/AM			OPA501SM/BM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RATED OUTPUT(1)(2)								
Output Current,	R_L = 2Ω (RM/AM)	±10			*			A
Continuous(3)	R_L = 2.6Ω (SM/BM)	±10			*			A
Output Voltage(3)	I_o = 10A peak	±20	23		±26	±29		V
DYNAMIC RESPONSE								
Bandwidth, Unity Gain	Small Signal		1			*		MHz
Full Power Bandwidth	V_o = 40Vp-p, R_L = 8Ω	10	16		*	*		kHz
Slew Rate	R_L = 5Ω (RM/AM)	1.35			*			V/µs
	R_L = 6.5Ω (SM/BM)	1.35			*			V/µs
INPUT OFFSET VOLTAGE								
Initial Offset			±5	±10		±2	±5	mV
vs Temperature	−25°C < T < +85°C (AM/BM)		±10	±65				µV/°C
	−55°C < T < +125°C (RM/SM)					±10	±40	µV/°C
vs Supply Voltage			±35			*		µV/V
INPUT BIAS CURRENT								
Initial	T_{case} = +25°C		15	40		*	20	nA
vs Temperature			±0.05			*		nA/°C
vs Supply Voltage			±0.02			*		nA/V
INPUT DIFFERENCE CURRENT								
Initial	T_{case} = +25°C		±5	±10		±2	±3	nA
vs Temperature	−25°C < T < +85°C (AM/BM)		±0.01					nA/°C
	−55°C < T < +125°C (RM/SM)					±0.01		nA/°C
OPEN-LOOP GAIN, DC	R_L = 5Ω (RM/AM)	94	115					dB
	R_L = 6.5Ω (SM/BM)				98	115		dB
INPUT IMPEDANCE								
Differential			10			*		MΩ
Common-mode			250			*		MΩ
INPUT NOISE								
Voltage Noise	f_n = 0.3Hz to 10Hz		3			*		µV, p-p
	f_n = 10Hz to 10kHz		5			*		µV, rms
Current Noise	f_n = 0.3Hz to 10Hz		20			*		pA, p-p
	f_n = 10Hz to 10kHz		4.5			*		pA, rms
INPUT VOLTAGE RANGE								
Common-mode Voltage(4)	Linear Operation	±(|V_{CC}|-6)	±(|V_{CC}|-3)		*	*		V
Common-mode Rejection	F = DC, V_{CM} = ±(|V_{CC}|-6)	70	110		80	*		dB
POWER SUPPLY								
Rated Voltage			±28			±34		V
Operating Voltage Range		±10		±36	*		±40	V
Current, quiescent			±2.6	±10		*	*	mA
TEMPERATURE RANGE	case							
Specification, RM/SM		-55		+125	*		*	°C
AM/BM		-25		+85	*		*	°C
Operating, derated performance, AM/BM		-55		+125	*		*	°C
Storage		-65		+150	*		*	°C
THERMAL RESISTANCE	Steady State θ_{JC}		2.0	2.2		*	*	°C/W

*Specification same as for OPA501RM/AM

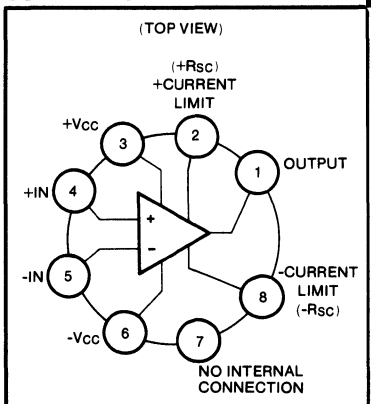
NOTES:
1. Package must be derated based on a junction to case thermal resistance of 2.2° C/W or a junction to ambient thermal resistance of 30° C/W.
2. Safe Operating Area and Power Derating Curves must be observed.
3. With $\pm R_{SC}$ = 0. Peak output current is typically greater than 10A if duty cycle and pulse width limitations are observed. Output current greater than 10A is not guaranteed.
4. The absolute maximum voltage is 3V less than supply voltage.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (V_{CC})	±40VDC
Power Dissipation at +25°C[1][2]	79W
Differential Input Voltage	$\pm V_{CC}$ – 3V
Common-Mode Input Voltage	$\pm V_{CC}$
Operating Temperature Range	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10 seconds)	+300°C
Junction Temperature	+200°C
Output Short-Circuit Duration[3]	Continuous

NOTES
1 At case temperature of +25°C. Derate at 2 2°C/W above case temperature of +25°C
2 Average dissipation
3 Within safe operating area and with appropriate derating.

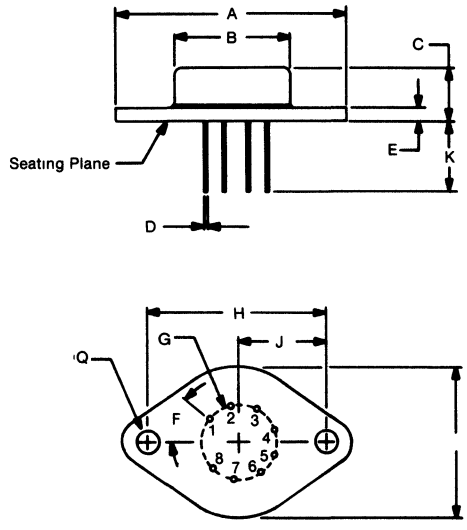
CONNECTION DIAGRAM



ORDERING INFORMATION

	OPA501	X	M	
Basic Model Number				
Performance Grade Code				
A, B = -25° C to +85° C				OPA501AM
R, S = -55° C to +125° C				OPA501BM
				OPA501RM
Package Code				OPA501SM
TO-3	(See Military Data Sheet)			OPA501SM/883

MECHANICAL



NOTE. Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

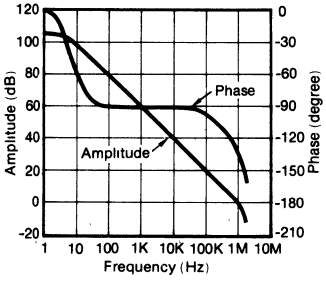
Pin numbers shown for reference only. Numbers may not be marked on package.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.260	.300	6.60	7.62
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

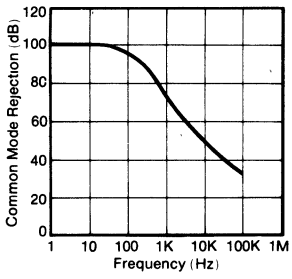
TYPICAL PERFORMANCE CURVES

(Typical at +25° case and ±V_{CC} = 28VDC unless otherwise noted.)

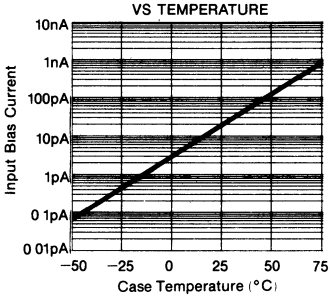
OPEN-LOOP FREQUENCY RESPONSE



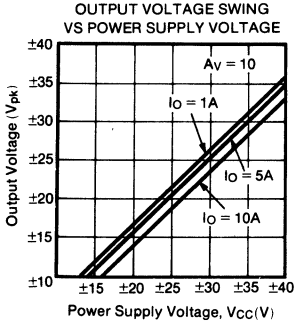
COMMON MODE REJECTION VS FREQUENCY



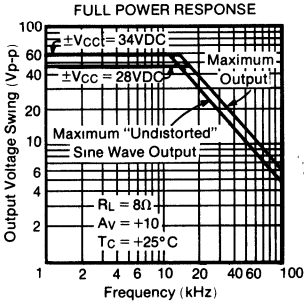
INPUT BIAS CURRENT VS TEMPERATURE



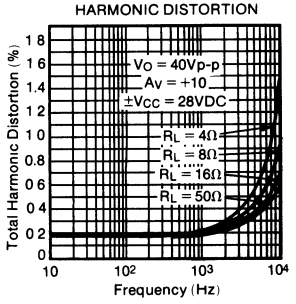
OUTPUT VOLTAGE SWING VS POWER SUPPLY VOLTAGE



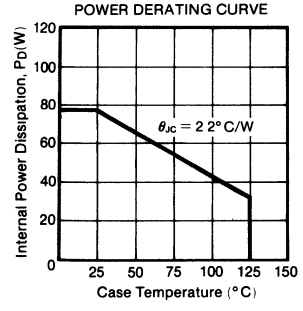
FULL POWER RESPONSE



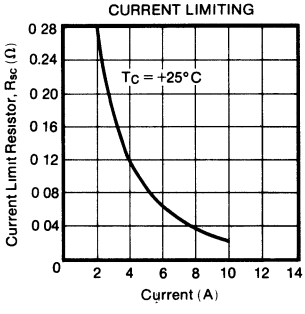
HARMONIC DISTORTION



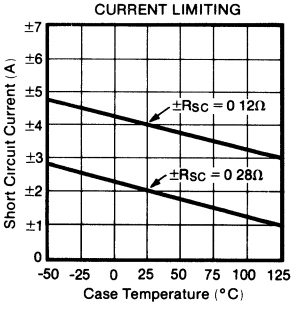
POWER DERATING CURVE



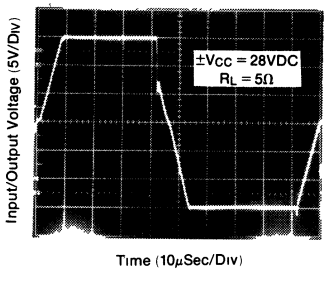
CURRENT LIMITING



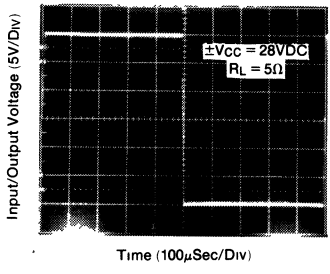
CURRENT LIMITING



PULSE RESPONSE, Av = +1



PULSE RESPONSE, AV = +1



INSTALLATION AND OPERATING INSTRUCTIONS

PROPER GROUNDING AND POWER SUPPLY BYPASSING

Particular attention should be given to proper grounding practices because the large output currents can cause significant ground-loop errors. Figure 1 illustrates proper connections.

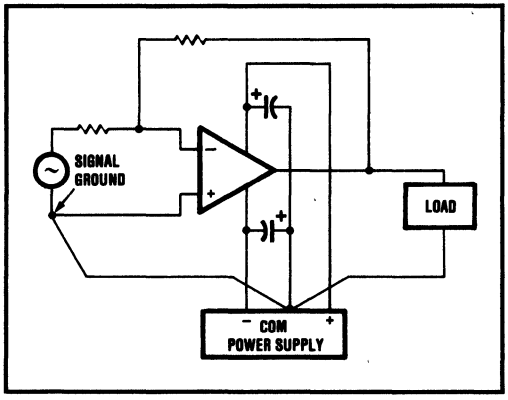


FIGURE 1. Proper Power Supply Connections.

Note that the connections are such that the load curent does not flow through the wire connecting the signal ground point to the power supply common. Also, power supply and load leads should be run physically separated from the amplifier input and signal leads.

The amplifier should be power-supply-bypassed with 10μF tantalum capacitors connected as close to pins 3 and 6 as possible. The capacitors should be connected to the load ground rather than the signal ground.

CURRENT LIMITS

The OPA501 amplifier is designed so that both the positive and negative load current limits can be set independently with external resistors R_{+SC} and R_{-SC} respectively. The approximate value of these resistors is given by the equation:

$$R_{SC} = \left(\frac{0.65}{I_{LIMIT}} - 0.0437\right) \text{ ohms}$$

I_{LIMIT} is the desired maximum current in amperes. The power dissipation of the current limit resistor is:

$$P_{max} = R_{SC} (I_{LIMIT})^2 \text{ watts}$$

R_{SC} is in ohms and I_{LIMIT} is in amperes.

Current limit resistors carry the full amplifier output current so lead lengths should be minimized. Highly inductive resistors can cause loop instability. Variation in I_{LIMIT} with case temperature is shown in the Typical Performance Curves.

The amplifier should be used with as low a current limit as possible for its particular application. This will minimize the chance of damaging the amplifier under abnormal load conditions and will increase reliability by limiting internal power dissipation.

The current limits may be used to generate other functions such as constant current supplies and torque or stall current limits for servomotor applications.

HEAT SINKING

The OPA501 requires a heat sink to limit output transistor junction temperature (T_J) to an absolute maximum of +200°C. The steady-state thermal circuit is illustrated in Figure 2.

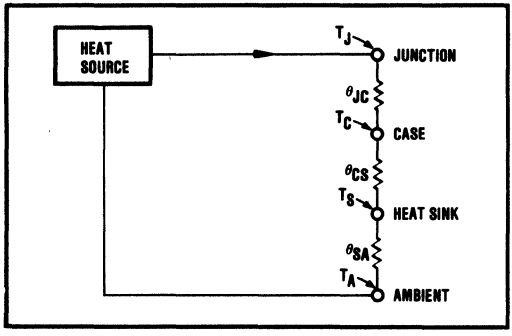


FIGURE 2. Simplified Steady-State Heat Flow Model.

Junction temperature (T_J) is found from the equation:

$$T_J = P_D (\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A$$

Where P_D = average amplifier power dissipation (W)
θ_{JC} = junction to case thermal resistance (°C/W)
θ_{CS} = device mounting thermal resistance (°C/W)
θ_{SA} = heat sink thermal resistance (°C/W)
T_A = ambient temperature (°C)

For most heat sink calculations the quiescent power dissipation is very low (<1 watt) and can be disregarded with only a small error.

The minimum size heat sink can be found from the equation:

$$\theta_{SA} = \frac{T_J - T_A}{P_D} - \theta_{CS} - \theta_{JC}$$

Example: Find the maximum thermal resistance (smallest heat sink) that can be used for an OPA501 with $\pm V_{CC}$ = 28VDC. Output voltage is +10VDC across a 10Ω resistor and ambient temperature is +50°C:

$$P_D = [(+28\text{VDC}) - (+10\text{VDC})] \times \frac{+10\text{VDC}}{10\Omega} = 18\text{W}$$

$$\theta_{SA} = \frac{200°\text{C} - 50°\text{C}}{18\text{W}} - 0.1°\text{C/W} - 2.2°\text{C/W}$$

θ_{SA}= 6.03°C/W maximum

As large a heat sink as possible should be used. θ_{CS} depends on the flatness of the heat sink, the thermal compound used, and the roughness of the mating surfaces. Typical values are between 0.1°C/W and 0.3°C/W for a TO-3 package properly mounted on a heat sink.

The OPA501 mounting flange is electrically-isolated and can be mounted directly to a heat sink without insulating washers or spacers. Screws with Bellville spring washers are recommended to maintain positive clamping pressure on heat sink mounting surfaces. Long periods of thermal cycling can loosen mounting screws and increase θ_{CS}.

The output transistor thermal resistance (θ_{JC}) is a function of output current pulse width, pulse shape, and duty cycle. Long duration pulses allow the junction temperature to approach its steady state value while shorter pulses cause a lower peak junction temperature due to the junction's thermal time constant. Heat is conducted rapidly away from the junction so that as duty cycle decreases, junction temperature decreases.

Steady state θ_{JC} is rated at 2.2°C/W maximum. In applications where the amplifier's output current alternates between output transistors–for example, an AC amplifier–the transistor θ_{JC} will depend on frequency as shown in Figure 3.

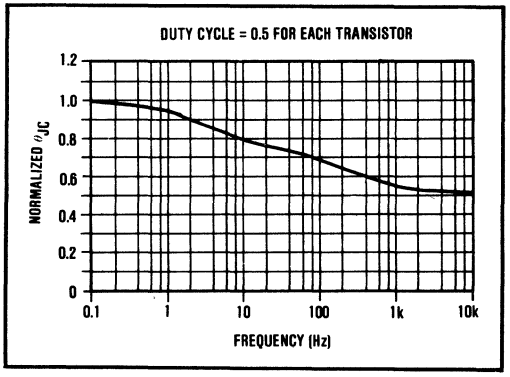


FIGURE 3. Effective θ_{JC} for Applications Where Output Current Alternates Between Output Transistors.

Example: OPA501SM with $\pm V_{CC}$ = 28VDC; heat sink θ_{SA} = 0.4°C/W; output = 11.2VAC, rms 400Hz (sine) at 5A, rms; Power Factor = 1.0; assume a mounting resistance of 0.1°C/W and an ambient temperature of +25°C.

The power dissipated by the OPA501, P_D, is equal to the power delivered by the power supplies, P_S, minus the power delivered to the load, P_L.

Peak output current is $(5A)(\sqrt{2}) = 7.07A$ peak.
$P_S = (V_{CC})(I_{AVG}) = (28V)(2/\pi)(7.07A) = 126W$.

Note that the power delivered by the power supply is equal to its voltage times the *average* current (not rms). Average is equal to $2/\pi$ times peak for a sine wave.

$P_L = (11.2VAC)(5A) = 56W$.

Average power dissipation of the amplifier is 126W − 56W = 70W. From Figure 3, the effective value of θ_{JC} at 400Hz is 0.6 × the rated θ_{JC}, threrfore, θ_{JC} = 1.32°C/W. This accounts for the fact that each output transistor is "resting" during alternate half cycles.

The junction temperature will be:

$$T_J = (70W)(1.32 + 0.1 + 0.4°C/W) + 25°C = 152°C.$$

This is well below the maximum junction temperature limit of 200°C. Best circuit reliability can be achieved, however, by keeping junction temperature to a minimum. In this case, a lower $\pm V_{CC}$ could be used to further reduce amplifier power dissipation.

At frequencies of 50Hz or less the junction temperature will change in response to the instantaneous dissipation—the product of the instantaneous voltage and current across the power transistors. Under approximately 50Hz the junction will heat in response to the peak dissipation condition which occurs at an output of one-half the power supply voltage. In the previous example, the peak dissipation can be found as follows:

Peak dissipation occurs at half of 28V = 14V output.
The load impedance Z_{LOAD} = 11.2V/5A = 2.24Ω.
The load current at peak dissipation = 14V/2.24Ω = 6.25A.
The peak dissipation = (14V)(6.25A) = 87.5W.

Furthermore, the θ_{JC} at this low frequency is equal to its specified value of 2.2°C/W (see Figure 3). In this case, the junction temperature would be:

$$T_J = (87.5W)(2.2 + 0.1 + 0.4°C/W) + 25°C = 261°C.$$

This exceeds the maximum specified junction temperature and is clearly unacceptable. More examples of this type of calculation can be found in Burr-Brown Application Note AN-123.

SAFE OPERATING AREA (SOA)

In addition to the limits imposed by power dissipation, the amplifier's output transistors are also limited by a

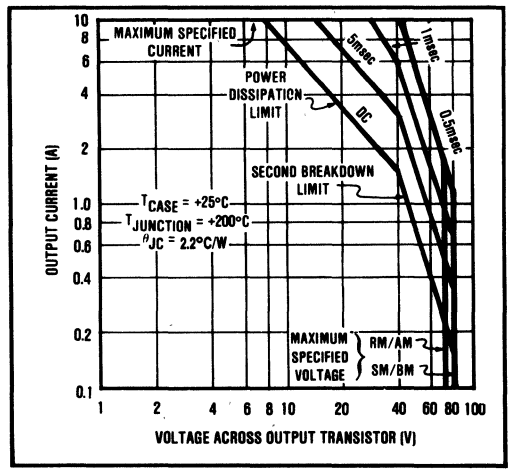


FIGURE 4. Transistor Safe Operating Area at +25°C Case Temperature.

second breakdown region. This occurs because of increased emitter current density due to current crowding at higher operating voltages. Both the dissipation and second breakdown limits depend on time and temperature. Figure 4 shows each output transistor's SOA at a case temperature of +25°C.

Limits for short pulse widths are substantially greater than for steady state (DC). At a case temperature of +125°C the SOA limits are reduced (see Figure 5). The SOA shown in these curves is based on a conservative linear derating of both the power dissipation and the second breakdown region.

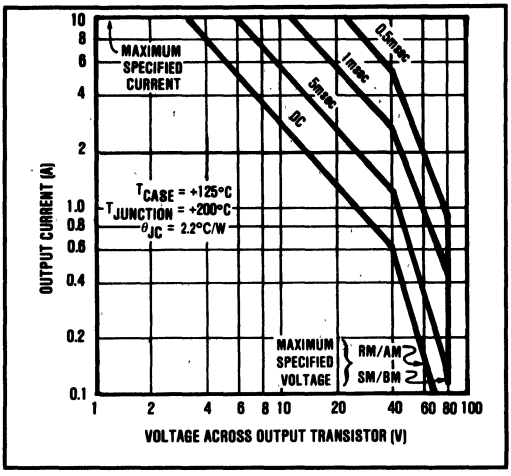


FIGURE 5. Transistor Safe Operating Area at +125°C Case Temperature.

Resistive loads are easy to analyze by simply plotting load lines on the SOA curve. If the curve representing the load line stays within the OPA501 output transistor SOA curve and all other parameters are observed, such as case temperature, etc., the amplifier will be safe. The load line can swing through the larger SOA limits if their time duration constraints are strictly observed.

Reactive loads present a more complex problem since the output voltage and current are not in phase. This results in the reactive load line becoming elliptical (when plotted on linear axes) which requires a larger SOA for safe operation.

Although detailed analysis is beyond the scope of this data sheet, the load line can be viewed on an oscilloscope as shown in Figure 6. The X-Y display is driven by the voltage across the load and by the current into the load.

This set up can also display voltage and current stress across the OPA501 output transistors as shown in Figure 7. This data can then be compared to the SOA limits.

The amplifier is designed to operate with electromotive-force-generating loads such as servomotors, relays, and actuators. Careful attention must be paid to both the load characteristics and the amplifier's SOA to ensure safe operation.

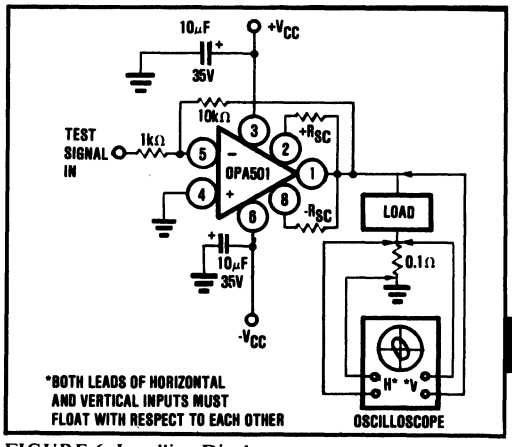


FIGURE 6. Loadline Display.

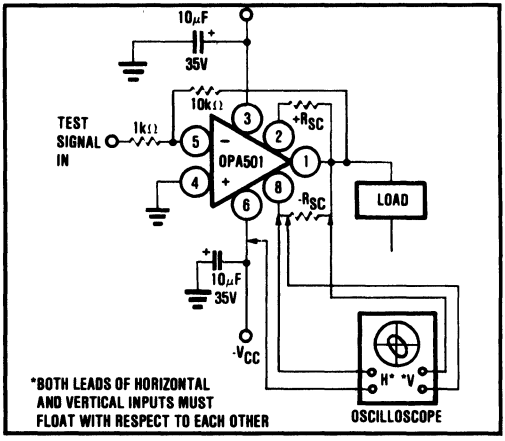


FIGURE 7. Output Transistor Safe Operating Area Stress Display.

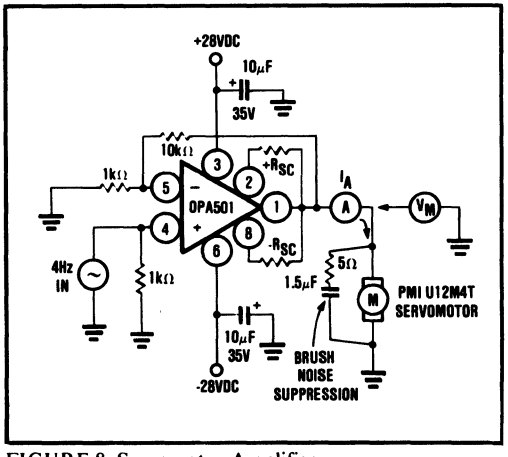


FIGURE 8. Servomotor Amplifier.

Figure 8 shows the OPA501 configured as a DC permanent magnet motor driver. The armature current (I_A) and motor voltage (V_m) are monitored within an oscilloscope in the X-Y mode displaying I_A and V_m respectively. Slewing the motor with a 4Hz sine wave results in the motor power ellipse of Figure 9. The input level has been adjusted to give ±20V, pk, across the motor. An examination of the power ellipse indicates that the instan-

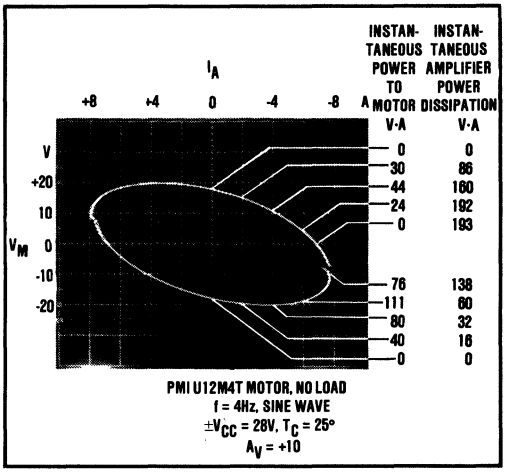


FIGURE 9. D.C. Servomotor Load Line.

taneous power delivered to the motor exceeds the amplifier output transistor's safe operating area at a case temperature of +25°C. The point at which the motor shows 0V at -6.9A is a problem. The voltage across the output transistor is 28V - 0V = 28V. Checking the SOA curve shows that the amplifier can safely withstand this condition for slightly under 5msec. At 4Hz this transient swing outside the DC SOA region is exceeded for much longer than 5msec. Continued operation under these conditions will result in failure. Peak junction temperatures should not exceed +200°C. Perhaps a motor with a higher impedance winding should be considered for this application. Current limiting and lower supply voltage can also reduce dissipation.

Motors used in servo applications often required a surprisingly large current to accelerate quickly. Worst case conditions occur when the motor is operating at full speed and is suddenly slammed into reverse ("plugging"). This condition is illustrated in Figure 10 when a DC servomotor is driven by a bipolar square wave. As the motor reverses direction a large surge current flows, causing very high peak power dissipation in the amplifier. After several time constants (determined by the inertia moment) the current drops to a lower steady-state value. Loading the motor increases the motor average power and amplifier dissipation. SOA curves should be checked for safe operation under these surge conditions.

The OPA501 current limits may be set to clip the high surge currents to a safe level. This is shown in Figure 11. Note that the current limit does limit the servo motor peak acceleration.

Inductive loads should be investigated for high peak transients generated by a collapsing magnetic field. Resistive damping can reduce this problem and although the amplifier has substrate diodes as part of the Darlington output transistor structure, external diodes are recommended for heavy clamping.

Fast diodes such as those normally used as rectifiers in switching power supplies are suitable.

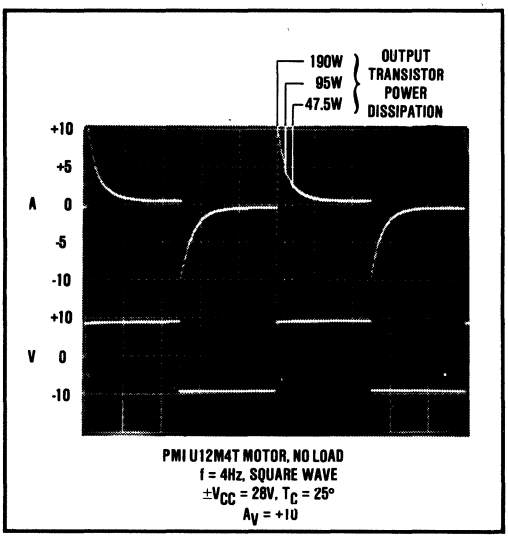


FIGURE 10. Servomotor Drive – "Plugging"

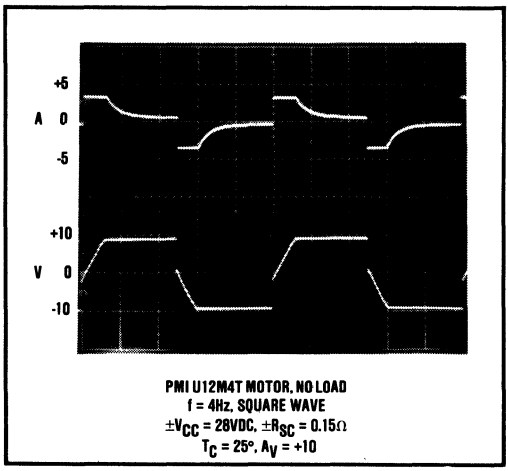


FIGURE 11. Servomotor Drive With Current Limit.

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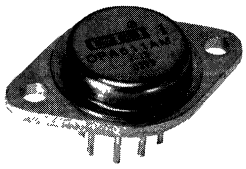


OPA511

High Current—High Power OPERATIONAL AMPLIFIER

FEATURES

- WIDE SUPPLY RANGE: ±10V to ±30V
- HIGH OUTPUT CURRENT: 5A peak
- CLASS A/B OUTPUT STAGE: Low distortion
- SMALL TO-3 PACKAGE

APPLICATIONS

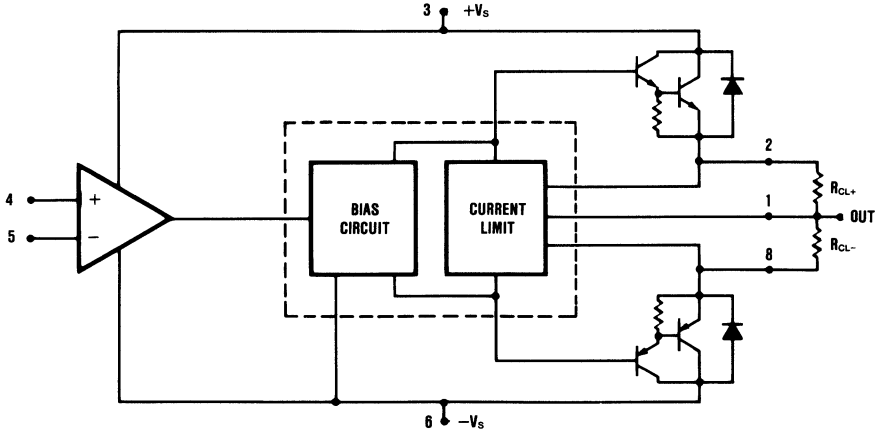
- SERVO AMPLIFIER
- MOTOR DRIVER
- SYNCRO EXCITATION
- AUDIO AMPLIFIER
- TEST PIN DRIVER

DESCRIPTION

The OPA511 is a high voltage, high current operational amplifier designed to drive a wide variety of resistive and reactive loads. Its complementary class A/B output stage provides superior performance in applications requiring freedom from cross-over distortion. User-set current limit circuitry provides protection to the amplifier and load in fault conditions.

The OPA511 employs a laser-trimmed monolithic integrated circuit to bias the output transistors, providing excellent low-level signal fidelity and high output voltage swing. The reduced internal parts count made possible with this bias IC improves performance and reliability.

This hybrid integrated circuit is housed in a hermetically sealed TO-3 package and all circuitry is electrically isolated from the case. This allows direct mounting to a chassis or heat sink without cumbersome insulating hardware and provides optimum heat transfer.



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PDS-599A

SPECIFICATIONS

ELECTRICAL

At T_C = +25°C and V_S = ±28VDC unless otherwise noted

PARAMETER	CONDITIONS	OPA511AM MIN	OPA511AM TYP	OPA511AM MAX	UNITS
INPUT					
OFFSET VOLTAGE					
Initial Offset			±5	±10	mV
vs Temperature	Full temperature range		±10	±65	µV/°C
vs Supply Voltage			±35	±200	µV/V
vs Power			±20		µV/W
BIAS CURRENT					
Initial			±15	±40	nA
vs Temperature	Full temperature range		±0 05	±0 4	nA/°C
vs Supply Voltage			±0 02		nA/V
OFFSET CURRENT					
Initial			±5	±10	nA
vs Temperature	Full temperature range		±0 01		nA/°C
INPUT IMPEDANCE					
Common-Mode			200		MΩ
Differential			10		MΩ
VOLTAGE RANGE[1]					
Common-Mode Voltage	Full temperature range	±(|V_S| − 6)	±(|V_S| − 3)		V
Common-Mode Rejection	V_{CM} = V_S − 6V	70	110		dB
GAIN					
Open-Loop Gain at 10Hz	Full temperature range, full load	91	113		dB
Gain-Bandwidth Product at 1MHz	T_C = +25°C, full load		1		MHz
Power Bandwidth	T_C = +25°C, I_O = 4A, V_O = 40V p-p	15	23		kHz
Phase Margin	Full temperature range		45		Degrees
OUTPUT					
Voltage Swing	I_O = 5A	±(|V_S| − 8)	±(|V_S| − 5)		V
	Full temperature range, I_O = 2A	±(|V_S| − 6)	±(|V_S| − 5)		V
	Full temperature range, I_O = 56mA	±(|V_S| − 5)			V
Current, Peak		±5			A
Settling Time to 0 1%	2V step		2		µs
Slew Rate	R_L = 2 5Ω	±1 0	1 8		V/µs
Capacitive Load Unity Gain	Full temperature range			3 3	nF
Gain > 4	Full temperature range			SOA[2]	
POWER SUPPLY					
Voltage	Full temperature range	±10	±28	±30	V
Current, Quiescent			20	30	mA
THERMAL					
RESISTANCE					
AC Junction to Case[3]	f > 60Hz		1 9	2 1	°C/W
DC Junction to Case	f > 60Hz		2 4	2 6	°C/W
Junction to Air			30		°C/W
TEMPERATURE RANGE, case		−25		+85	°C

NOTES (1) +V_S and −V_S denote the positive and negative supply voltage respectively Total V_S is measured from +V_S to −V_S (2) SOA = Safe Operating Area (3) Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$		68V
Output Current	source	5A
	sink	see SOA
Power Dissipation, internal[1]		67W
Input Voltage	differential	$\pm(\lvert V_S \rvert - 3V)$
	common-mode	$\pm V_S$
Temperature	junction[1]	+200°C
	pin solder, 10sec	+300°C
Temperature Range	storage	−65°C to +150°C
	operating (case)	−25°C to +85°C

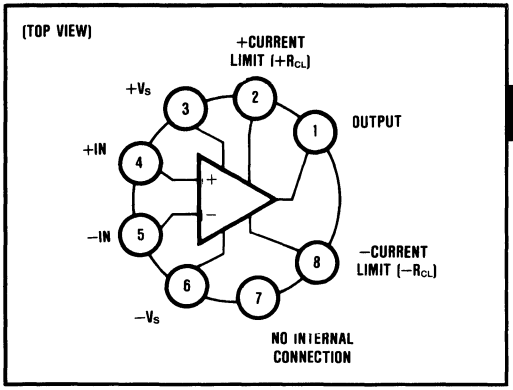
NOTE. (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

ORDERING INFORMATION

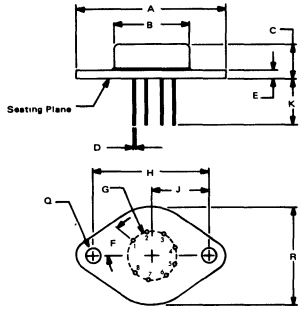
OPA511 A M

Basic Model Number
Grade Code
Package Code (TO-3)

CONNECTION DIAGRAM



MECHANICAL



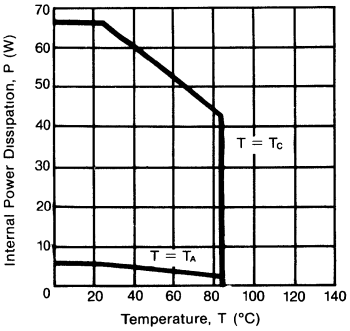
NOTE Leads in true position within .010" (.25mm) R at MMC at seating plane
Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.260	.300	6.60	7.62
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

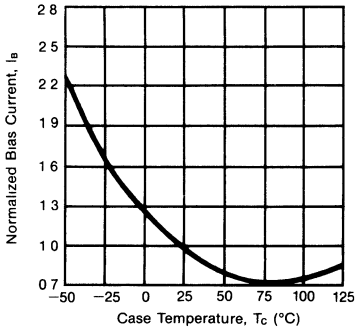
TYPICAL PERFORMANCE CURVES

$T_A = 25°C$ $V_S = \pm 28VDC$ unless otherwise noted

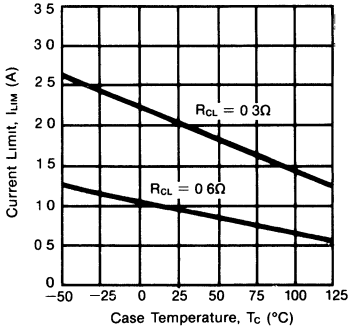
POWER DERATING



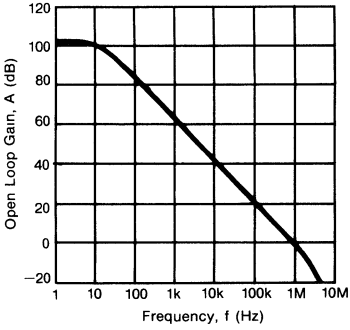
BIAS CURRENT



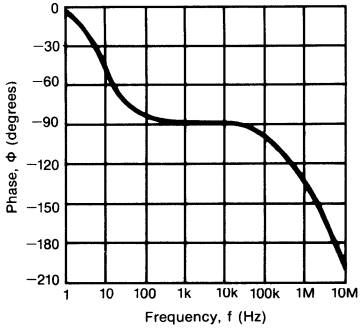
CURRENT LIMIT



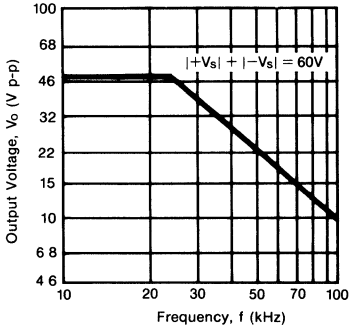
SMALL SIGNAL RESPONSE



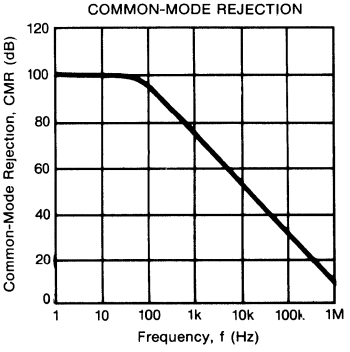
PHASE RESPONSE



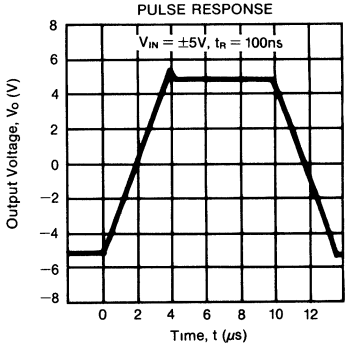
POWER RESPONSE



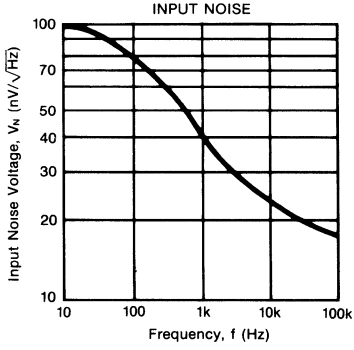
COMMON-MODE REJECTION



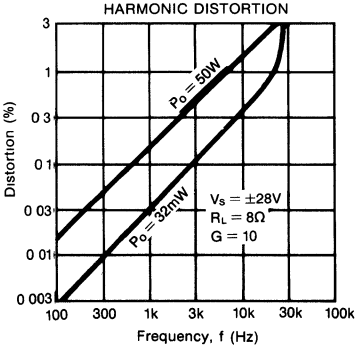
PULSE RESPONSE



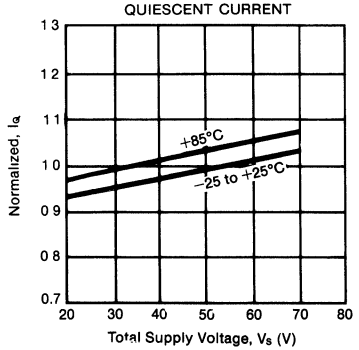
INPUT NOISE



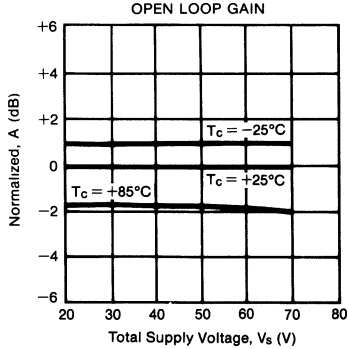
HARMONIC DISTORTION



QUIESCENT CURRENT



OPEN LOOP GAIN



APPLICATIONS INFORMATION

POWER SUPPLIES

Specifications for the OPA511 are based on a nominal operating voltage of ±28V. A single power supply or unbalanced supplies may be used so long as the maximum total operating voltage (total of $+V_S$ and $-V_S$) is not greater than 68V.

CURRENT LIMITS

Current limit resistors must be provided for proper operation. Independent positive and negative current limit values may be selected by choice of R_{CL+} and R_{CL-} respectively. Resistor values are calculated by:

$$R_{CL} = 0.65/I_{LIM} \text{ (amps)} - 0.01$$

This is the nominal current limit value at room temperature. The maximum output current decreases at high temperature as shown in the typical performance curve. Most wire-wound resistors are satisfactory, but some highly inductive types may cause loop stability problems. Be sure to evaluate performance with the actual resistors to be used in production.

HEAT SINKING

Power amplifiers are rated by case temperature (not ambient temperature). The maximum allowable power dissipation is a function of the case temperature as shown in the power derating curve. Load characteristics, signal conditions, and power supply voltage determine the power dissipated by the amplifier. The case temperature will be determined by the heat sinking conditions. Sufficient heat sinking must be provided to keep the case temperature within safe bounds given the power dissipated and ambient temperature. See Applications Note AN-83 for further details.

SAFE OPERATING AREA (SOA)

The safe area plot provides a comprehensive summary of the power handling limitations of a power amplifier, including maximum current, voltage and power as well as the secondary breakdown region (see Figure 1). It shows the allowable output current as a function of the power supply to output voltage differential (voltage across the conducting power device). See Applications Note AN-123 for details on SOA.

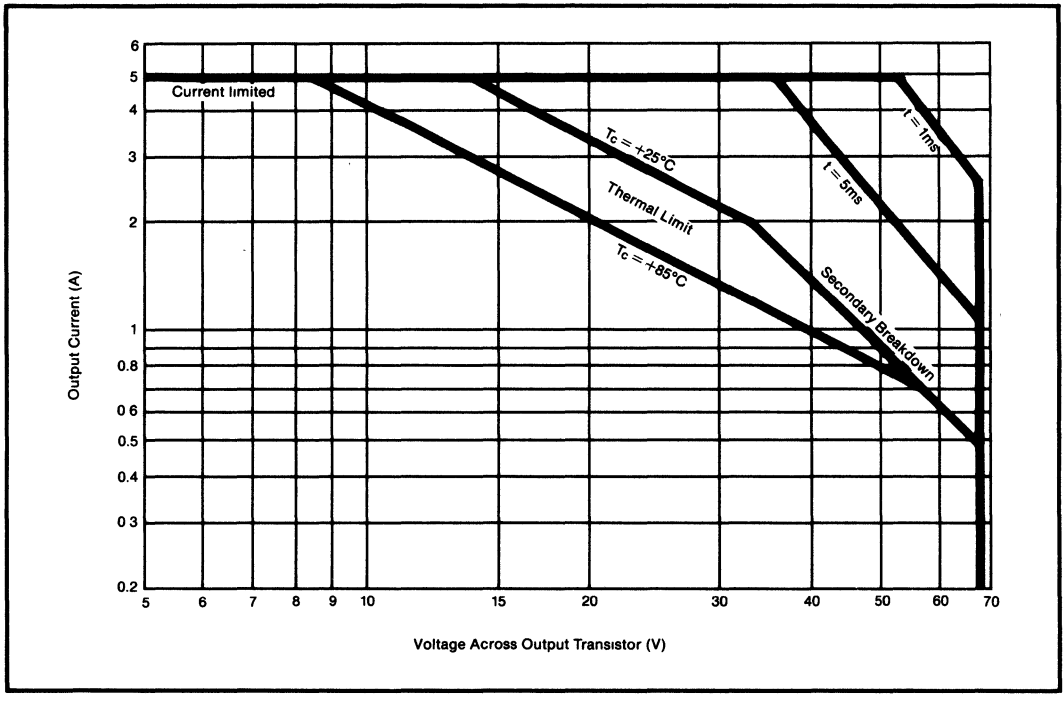


FIGURE 1. Safe Operating Area.

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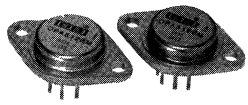


OPA512

MILITARY VERSION AVAILABLE

Very-High Current—High Power OPERATIONAL AMPLIFIER

FEATURES

- WIDE SUPPLY RANGE: ±10V to ±50V
- HIGH OUTPUT CURRENT: 15A peak
- CLASS A/B OUTPUT STAGE: Low distortion
- VOLTAGE-CURRENT LIMIT PROTECTION CIRCUIT
- SMALL TO-3 PACKAGE

APPLICATIONS

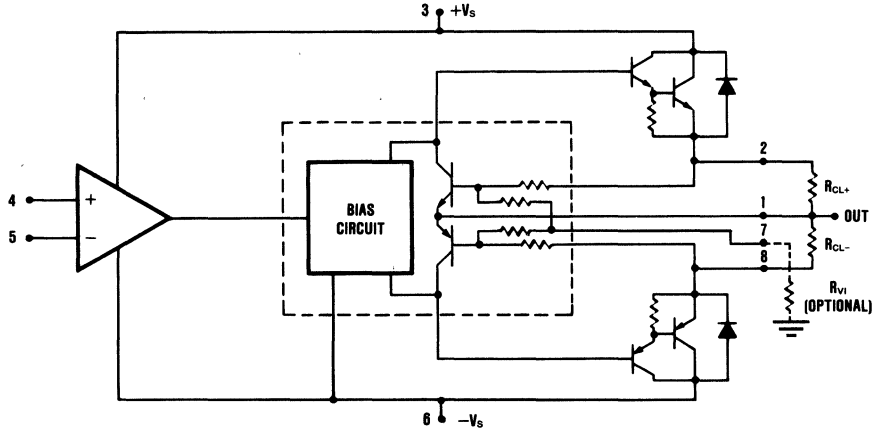
- SERVO AMPLIFIER
- MOTOR DRIVER
- SYNCRO EXCITATION
- AUDIO AMPLIFIER
- TEST PIN DRIVER

DESCRIPTION

The OPA512 is a high voltage, very-high current operational amplifier designed to drive a wide variety of resistive and reactive loads. Its complementary class A/B output stage provides superior performance in applications requiring freedom from cross-over distortion. User-set current limit circuitry provides protection to the amplifier and load in fault conditions. A resistor-programmable voltage-current limiter circuit may be used to further protect the amplifier from damaging conditions.

The OPA512 employs a laser-trimmed monolithic integrated circuit to bias the output transistors, providing excellent low-level signal fidelity and high output voltage swing. The reduced internal parts count made possible with this monolithic IC improves performance and reliability.

This hybrid integrated circuit is housed in a hermetically-sealed TO-3 package and all circuitry is electrically-isolated from the case. This allows direct mounting to a chassis or heat sink without cumbersome insulating hardware and provides optimum heat transfer.



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PDS-600B

SPECIFICATIONS

ELECTRICAL

At T_C = +25°C and V_S = ±40VDC unless otherwise noted.

PARAMETER	CONDITIONS	OPA512BM MIN	OPA512BM TYP	OPA512BM MAX	OPA512SM MIN	OPA512SM TYP	OPA512SM MAX	UNITS
INPUT								
OFFSET VOLTAGE								
Initial Offset			±2	±6		±1	±3	mV
vs Temperature	Specified temp range		±10	±65		*	±40	µV/°C
vs Supply Voltage			±30	±200		*	*	µV/V
vs Power			±20			*		µV/W
BIAS CURRENT								
Initial			12	30		10	20	nA
vs Temperature	Specified temp range		±50	400		*	*	pA/°C
vs Supply Voltage			±10			*		pA/V
OFFSET CURRENT								
Initial			±12	±30		±5	±10	nA
vs Temperature	Specified temp range		±50			*		pA/°C
INPUT IMPEDANCE, DC			200			*		MΩ
INPUT CAPACITANCE			3			*		pF
VOLTAGE RANGE								
Common-Mode Voltage	Specified temp range	±(|V_S| − 5)	±(|V_S| − 3)		*	*		V
Common-Mode Rejection	Specified temp range	74	100		*	*		dB
GAIN								
Open-Loop Gain at 10Hz	1kΩ load		110			*		dB
	Specified temp. range, 8Ω load	96	108		*	*		dB
Gain-Bandwidth Product, 1MHz	8Ω load		4			*		MHz
Power Bandwidth	8Ω load	13	20		*	*		kHz
Phase Margin	Specified temp range, 8Ω load		20			*		Degrees
OUTPUT								
Voltage Swing[1]	BM at 10A, SM at 15A	±(|V_S| − 6)			±(|V_S| − 7)			V
	Specified temp range, I_O = 80mA	±(|V_S| − 5)			*			V
	I_O = 5A	±(|V_S| − 5)			*			V
Current, Peak		10			15			A
Settling Time to 0 1%	2V step		2			*		µs
Slew Rate		2 5	4		*	*		V/µs
Capacitive Load	Specified temp range, G = 1			1 5			*	nF
	Specified temp range, G > 10			SOA[2]			*	
POWER SUPPLY								
Voltage	Specified temp range	±10	±40	±45	*	*	±50	V
Current, Quiescent			25	50		*	35	mA
THERMAL								
RESISTANCE								
AC Junction to Case[3]	T_C = −55°C to +125°C, f > 60Hz		0 8	0 9		*	*	°C/W
DC Junction to Case	T_C = −55°C to +125°C		1 25	1 4		*	*	°C/W
Junction to Air	T_C = −55°C to +125°C		30			*		°C/W
TEMPERATURE RANGE, specified	T_C	−25		+85	−55		+125	°C

*Specification same as OPA512BM.

NOTES: (1) +V_S and −V_S denote the positive and negative supply voltage respectively Total V_S is measured from +V_S to −V_S (2) SOA = Safe Operating Area (3) Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ 100V
Output Current source 15A
sink ..... see SOA
Power Dissipation, internal[1] 125W
Input Voltage differential ..... $\pm(|V_S| - 3V)$
common-mode ..... $\pm V_S$
Temperature, pin solder, 10s ..... +300°C
junction[1] ..... +200°C
Temperature Range storage[2] ..... −65°C to +150°C
operating (case) ..... −55°C to +125°C

NOTE (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. (2) OPA512BM, −55°C to +100°C.

ORDERING INFORMATION

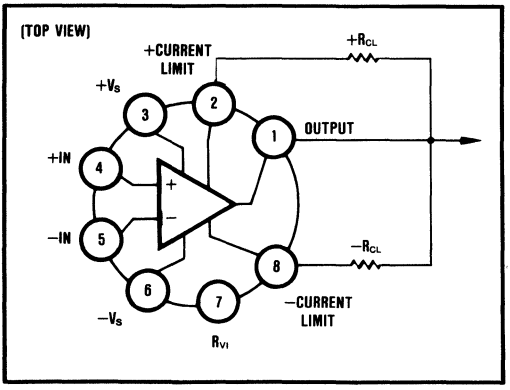
OPA512 X M

Basic Model Number

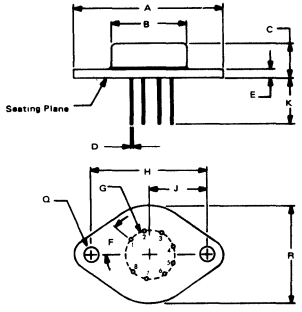
Performance Grade Code
B = −25°C to +85°C
S = −55°C to +125°C

Package Code (TO-3)
M = TO-3

CONNECTION DIAGRAM



MECHANICAL



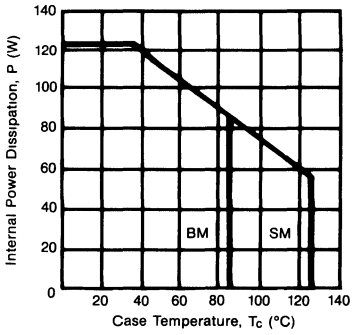
NOTE Leads in true position within .010" (.25mm) R at MMC at seating plane.
Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.240	.290	6.10	7.37
D	.038	.042	.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

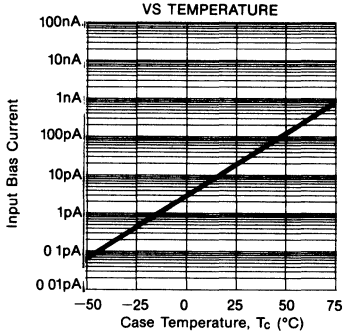
TYPICAL PERFORMANCE CURVES

$T_A = 25°C$, $V_S = \pm 40VDC$ unless otherwise noted.

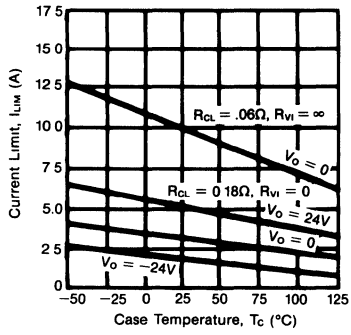
POWER DERATING



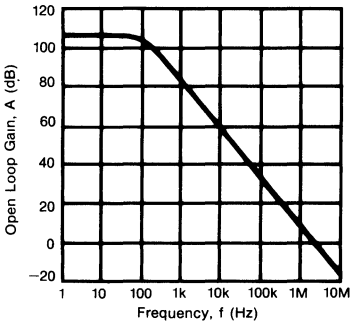
INPUT BIAS CURRENT VS TEMPERATURE



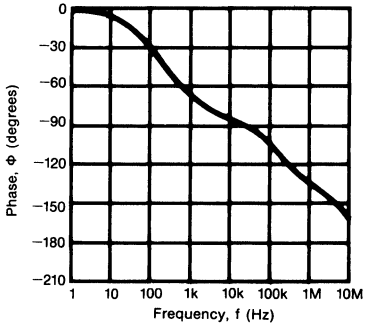
CURRENT LIMIT



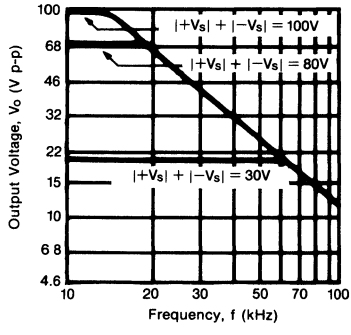
SMALL SIGNAL RESPONSE



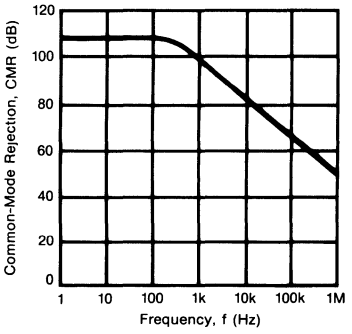
PHASE RESPONSE



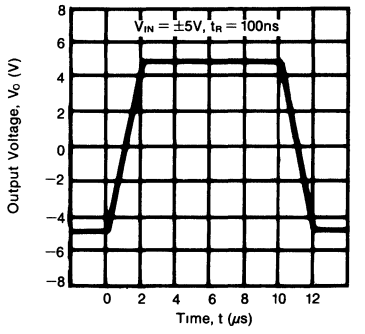
POWER RESPONSE



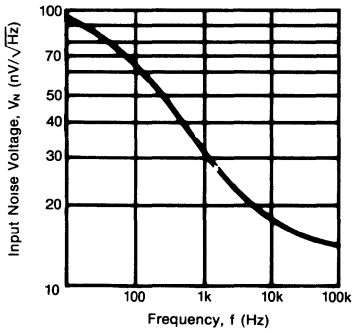
COMMON-MODE REJECTION



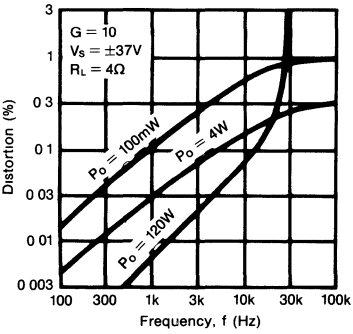
PULSE RESPONSE



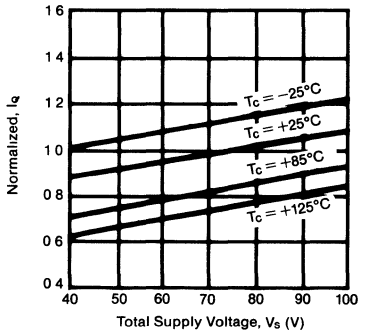
INPUT NOISE



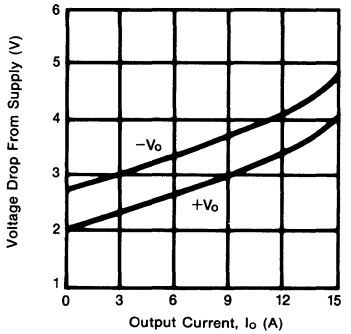
HARMONIC DISTORTION



QUIESCENT CURRENT



OUTPUT VOLTAGE SWING



APPLICATIONS INFORMATION

POWER SUPPLIES

Specifications for the OPA512 are based on a nominal operating voltage of ±40V. A single power supply or unbalanced supplies may be used as long as the maximum total operating voltage (total of $+V_S$ and $-V_S$) is not greater than 90V (100V for "S" grade version).

CURRENT LIMITS

Current limit resistors must be provided for proper operation. Independent positive and negative current limit values may be selected by choice of R_{CL+} and R_{CL-} respectively. Resistor values are calculated by:

$$R_{CL} = 0.65/I_{LIM} \text{ (amps)} - 0.007$$

This is the nominal current limit value at room temperature. The maximum output current decreases at high temperature as shown in the typical performance curve. Most wire-wound resistors are satisfactory, but some highly inductive types may cause loop stability problems. Be sure to evaluate performance with the actual resistors to be used in production.

HEAT SINKING

Power amplifiers are rated by case temperature (not ambient temperature). The maximum allowable power dissipation is a function of the case temperature as shown in the power derating curve. Load characteristics, signal conditions, and power supply voltage determine the power dissipated by the amplifier. The case temperature will be determined by the heat sinking conditions. Sufficient heat sinking must be provided to keep the case temperature within safe bounds given the power dissipated and ambient temperature. See Applications Note AN-83 for further details.

SAFE OPERATING AREA (SOA)

The safe area plot provides a comprehensive summary of the power handling limitations of a power amplifier, including maximum current, voltage and power as well as the secondary breakdown region (see Figure 1). It shows the allowable output current as a function of the power supply to output voltage differential (voltage across the conducting power device). See Applications Note AN-123 for details on SOA.

VOLTAGE-CURRENT LIMITER CIRCUITRY

The voltage-current (V-I) limiter circuit provides a means to protect the amplifier from SOA damage such as a short circuit to ground, yet allows high output currents to flow under normal load conditions. Sensing both the output current and the output voltage, this limiter circuit increases the current limit value as the output voltage approaches the power supply voltage (where power dissipation is low). This type of limiting is achieved by connecting pin 7 through a programming resistor to ground. The V-I limiter circuit is governed by the equation:

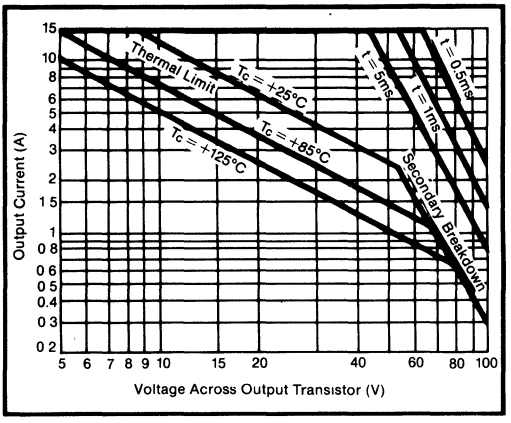


FIGURE 1. Safe Operating Area.

$$I_{LIMIT} = \frac{0.65 + \dfrac{0.28\ V_O}{20 + R_{VI}}}{R_{CL} + 0.007}$$

where:

I_{LIMIT} is the maximum current available at a given output voltage.

R_{VI} is the value (kΩ) of the resistor from pin 7 to ground.

R_{CL} is the current limit resistor in ohms.

V_O is the instantaneous output voltage in volts.

Reactive or EMF generating loads may produce unusual (perhaps undesirable) waveforms with the V-I limit circuit driven into limit. Since current peaks in a reactive load do not align with the output voltage peaks, the output waveform will not appear as a simple voltage-limited waveform. Response of the load to the limiter, in fact, may produce a "backfire" reaction producing unusual output waveforms.

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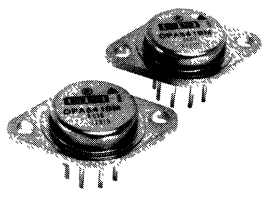


OPA541

MILITARY & DIE VERSIONS AVAILABLE

High Power Monolithic OPERATIONAL AMPLIFIER

FEATURES

- POWER SUPPLIES TO ±40V
- OUTPUT CURRENT TO 10A PEAK
- PROGRAMMABLE CURRENT LIMIT
- INDUSTRY-STANDARD PINOUT
- FET INPUT

APPLICATIONS

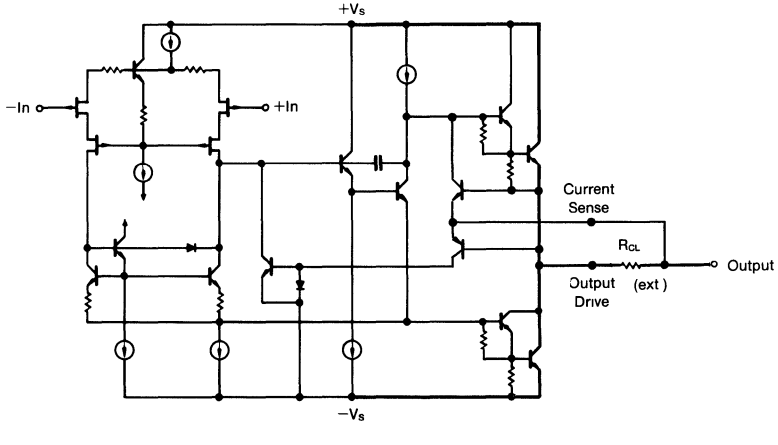
- MOTOR DRIVER
- SERVO AMPLIFIER
- SYNCHRO EXCITATION
- AUDIO AMPLIFIER
- PROGRAMMABLE POWER SUPPLY

DESCRIPTION

The OPA541 is a power operational amplifier capable of operation from power supplies up to ±40V and continuous output currents up to 5A. Internal current limit circuitry can be user-programmed with a single external resistor, protecting the amplifier and load from fault conditions. The OPA541 is fabricated using a proprietary bipolar/FET process.

Pinout is compatible with popular hybrid power amplifiers such as the OPA511, OPA512 and the 3573. The OPA541 uses a single current-limit resistor to set both the positive and negative current limits. Applications currently using hybrid power amplifiers requiring two current-limit resistors need not be modified.

The OPA541 is available in an industry-standard 8-pin TO-3 hermetic package. The case is isolated from all circuitry, thus allowing it to be mounted directly to a heat sink without special insulators which degrade thermal performance.



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PDS-737A

SPECIFICATIONS

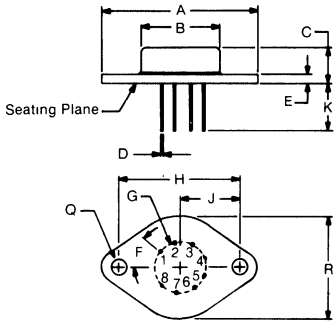
ELECTRICAL

At T_C = +25°C and V_S = ±35VDC unless otherwise noted

PARAMETER	CONDITIONS	OPA541AM			OPA541BM/SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT OFFSET VOLTAGE								
V_{OS}			±2	±10		±0 1	±1	mV
vs Temperature	Specified temperature range		±20	±40		±15	±30	µV/°C
vs Supply Voltage	V_S = ±10V to ±V_{MAX}		±2 5	±10		*	*	µV/V
vs Power			±20	±60		*	*	µV/W
INPUT BIAS CURRENT								
I_B			4	50		*	*	pA
INPUT OFFSET CURRENT								
I_{OS}			±1	±30		*	*	pA
	Specified temperature range			5		*		nA
INPUT CHARACTERISTICS								
Common Mode Voltage Range	Specified temperature range	±(|V_S|−6)	±(|V_S|−3)		*	*		V
Common Mode Rejection	V_{CM} = (|±V_S|−6V)	95	113		*	*		dB
Input Capacitance			5			*		pF
Input Impedance, DC			1			*		TΩ
GAIN CHARACTERISTICS								
Open Loop Gain at 10Hz	R_L = 6Ω	90	97		*	*		dB
Gain Bandwidth Product			1 6			*		MHz
OUTPUT								
Voltage Swing	I_O = 5A, Continuous	±(|V_S|−5 5)	±(|V_S|−4 5)		*	*		V
	I_O = 2A	±(|V_S|−4)	±(|V_S|−3 6)		*	*		V
	I_O = 0 5A	±(|V_S|−4)	±(|V_S|−3 2)		*	*		V
Current, Peak		9	10		*	*		A
AC PERFORMANCE								
Slew Rate		6	10		*	*		V/µs
Power Bandwidth	R_L = 8Ω, V_O = 20Vrms	45	55		*	*		kHz
Settling Time to 0 1%	2V Step		2			*		µs
Capacitive Load	Specified temperature range, G = 1	3 3					*	nF
	Specified temperature range, G > 10			SOA			*	
Phase Margin	Specified temperature range, R_L = 8Ω		40			*		Degrees
POWER SUPPLY								
Power Supply Voltage, ±V_S	Specified temperature range	±10	±30	±35	*	±35	±40	V
Current, Quiescent			20	25		*	*	mA
THERMAL RESISTANCE								
θ_{JC}, (junction to case)	AC output f > 60Hz		1 25	1 5		*	*	°C/W
θ_{JC}	DC output		1 4	1 9		*	*	°C/W
θ_{JA}, (junction to ambient)	No heat sink		30			*		°C/W
TEMPERATURE RANGE								
T_{CASE}	AM, BM	−25		+85	*		*	°C
	SM				−55		+125	°C

*Specification same as OPA541AM

MECHANICAL



NOTE Leads in true position within 0.010" (0.25mm) R at MMC at seating plane

Pin numbers shown for reference only. Numbers may not be marked on package

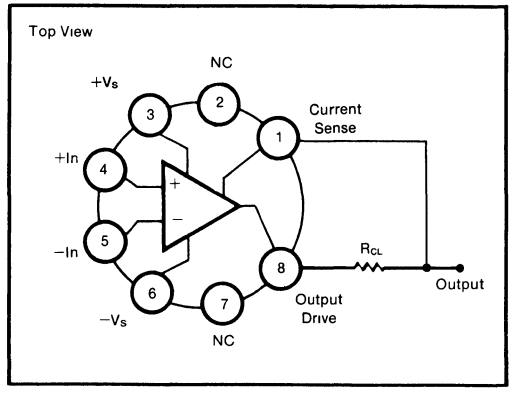
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.260	.300	6.60	7.62
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$	80V
Output Current	see SOA
Power Dissipation, Internal[1]	125W
Input Voltage Differential	$\pm V_S$
Common-mode	$\pm V_S$
Temperature Pin solder, 10s	+300°C
Junction[1]	+150°C
Temperature Range	
Storage	−65°C to +150°C
Operating (case)	−55°C to +125°C

NOTE (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

CONNECTION DIAGRAM



ORDERING INFORMATION

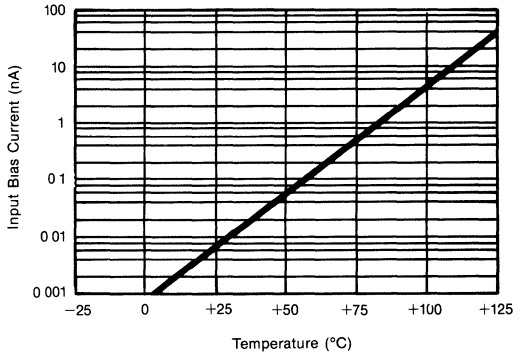
Model	Package	Temperature Range	
OPA541AM	TO-3	−25°C to +85°C	
OPA541BM	TO-3	−25°C to +85°C	
OPA541SM	TO-3	−55°C to +125°C	
BURN-IN SCREENING OPTION			
Model	**Package**	**Temperature Range**	**Burn-In Temp. (160h)[1]**
OPA541AM-BI	TO-3	−25°C to +85°C	+85°C
OPA541BM-BI	TO-3	−25°C to +85°C	+85°C
OPA541SM-BI	TO-3	−55°C to +125°C	+125°C

NOTE. (1) Or equivalent combination of time and temperature (2) Minimum order is 25 pieces

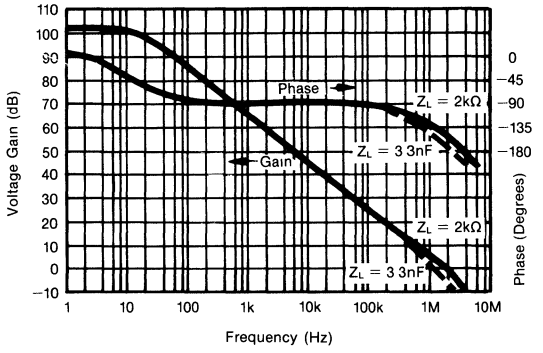
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±35VDC unless otherwise noted

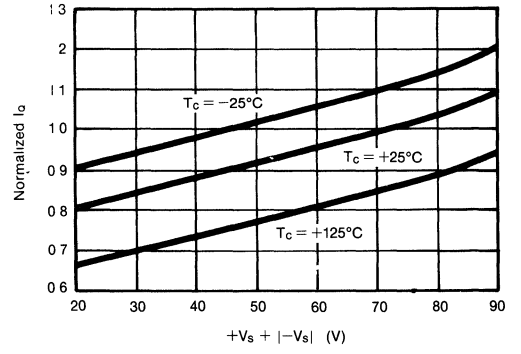
INPUT BIAS CURRENT
VS TEMPERATURE



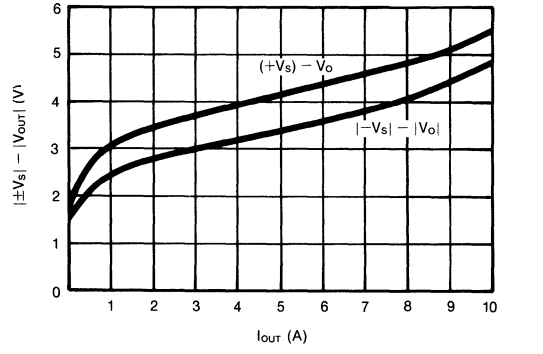
OPEN-LOOP GAIN AND
PHASE VS FREQUENCY



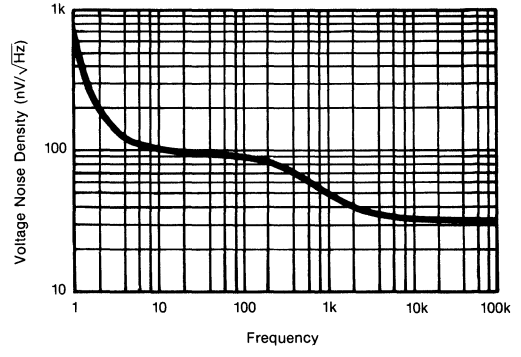
NORMALIZED QUIESCENT CURRENT VS
TOTAL POWER SUPPLY VOLTAGE



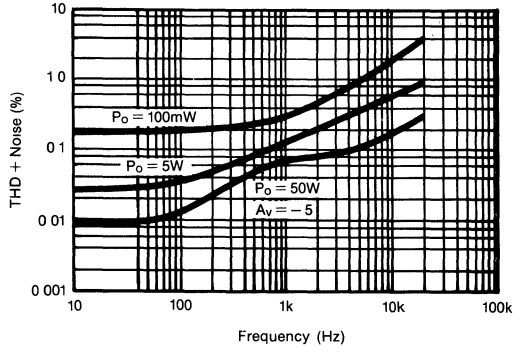
OUTPUT VOLTAGE SWING
VS OUTPUT CURRENT



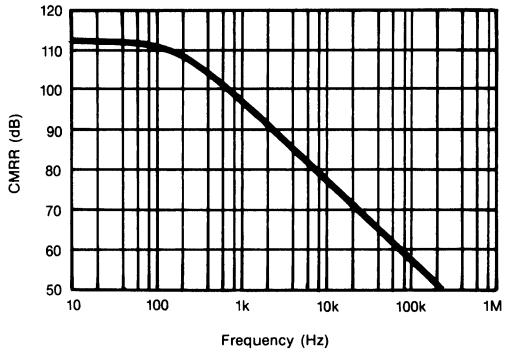
VOLTAGE NOISE DENSITY
VS FREQUENCY



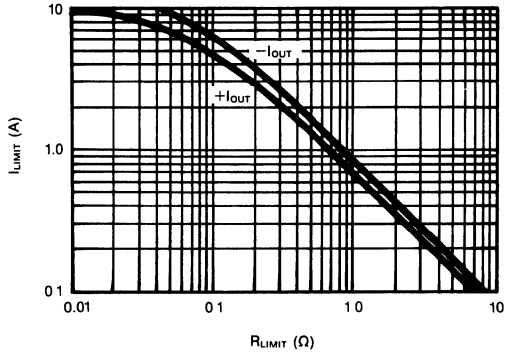
TOTAL HARMONIC DISTORTION
VS FREQUENCY



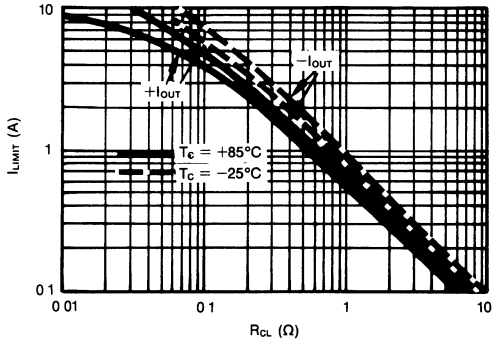
COMMON-MODE REJECTION VS FREQUENCY



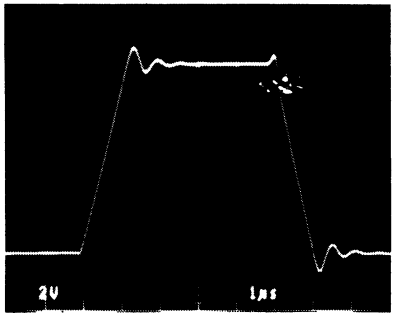
CURRENT LIMIT VS RESISTANCE LIMIT



CURRENT LIMIT VS RESISTANCE LIMIT VS TEMPERATURE



DYNAMIC RESPONSE



G = 1, C_L = 4.7nF

INSTALLATION INSTRUCTIONS

POWER SUPPLIES

The OPA541 is specified for operation from power supplies up to ±40V. It can also be operated from unbalanced or single power supply as long as the total power supply voltage does not exceed 80V. The power supplies should be bypassed with low series impedance capacitors such as ceramic or tantalum. These should be located as near as practical to the amplifier's power supply pins. Good power amplifier circuit layout is, in general, like good high frequency layout. Consider the path of large power supply and output currents. Avoid routing these connections near low-level input circuitry to avoid waveform distortion and oscillations.

CURRENT LIMIT

Internal current limit circuitry is controlled by a single external resistor, R_{CL}. Output load current flows through this external resistor. The current limit is activated when the voltage across this resistor is approximately a base-emitter turn-on voltage. The value of the current limit resistor is approximately:

$$R_{CL} = \frac{0.809}{|I_{LIM}|} - 0.057$$

The current limit value decreases with increasing temperature due to the temperature coefficient of a base-emitter junction voltage. Similarly, the current limit value increases at low temperatures. Current limit versus resistor value and temperature effects are shown in the Typical Performance Curves.

The adjustable current limit can be set to provide protection from short circuits. The safe short-circuit current depends on power supply voltage. See the discussion on Safe Operating Area to determine the proper current limit value.

Since the full load current flows through R_{CL}, it must be selected for sufficient power dissipation. For a 5A current limit, the dissipation of R_{CL} will be 3.25W for 5A continuous currents. Sinusoidal output will create dissipation according to the rms load current. Thus for the same 5A current limit, AC peaks would be limited to 5A, but the rms current would be 3.5A and a resistor with a lower power rating could be used. Some applications

(such as voice amplification) are assured of signals with much lower duty cycles, allowing a current resistor with a lower power rating. Wire-wound resistors may be used for R_{CL}. Some wire-wound resistors, however, have excessive inductance and may cause loop-stability problems. Be sure to evaluate circuit performance with resistor type planned for production to assure proper circuit operation.

HEAT SINKING

Power amplifiers are rated by case temperature, not ambient temperature as with signal op amps. The maximum allowable power dissipation is a function of the case temperature as shown on the power derating curve. All points on the power derating slope produce a maximum internal junction temperature of +150°C. Sufficient heat sinking must be provided to keep the case temperature within safe bounds for the maximum ambient temperature and power dissipation. The thermal resistance of the heat sink required may be calculated by:

$$\theta_{HS} = \frac{T_{CASE} - T_{AMBIENT}}{P_D \text{ (max)}}$$

Commercially available heat sinks often specify their thermal resistance. These ratings are often suspect, however, since they depend greatly on the mounting environment and air flow conditions. Actual thermal performance should be verified by measurement of case temperature under the required load and environmental conditions.

No insulating hardware is required when using the TO-3 package. Since mica and other similar insulators typically add approximately 0.7°C/W thermal resistance, their elimination significantly improves thermal performance. See Burr-Brown Application Note AN-83 for further details on heat sinking.

SAFE OPERATING AREA

The safe operating area (SOA) plot provides comprehensive information on the power handling abilities of the OPA541. It shows the allowable output current as a function of the voltage across the conducting output transistor (see Figure 1). This voltage is equal to the power supply voltage minus the output voltage. For example, as the amplifier output swings near the positive power supply voltage, the voltage across the output transistor decreases and the device can safely provide large output currents demanded by the load.

Short circuit protection requires evaluation of SOA. When the amplifier output is shorted to ground, the full power supply voltage is impressed across the conducting output transistor. The current limit must be set to a value which is safe for the power supply voltage used. For instance, with V_S ±35V, a short to ground would force 35V across the conducting power transistor. A current limit of 1.8A would be safe.

Reactive, or EMF-generating, loads such as DC motors can present difficult SOA requirements. With a purely reactive load, output voltage and load current are 90° out of phase. Thus, peak output current occurs when the output voltage is zero and the voltage across the conducting transistor is equal to the full power supply voltage. See Burr-Brown Application Note AN-123 for further information on evaluating SOA.

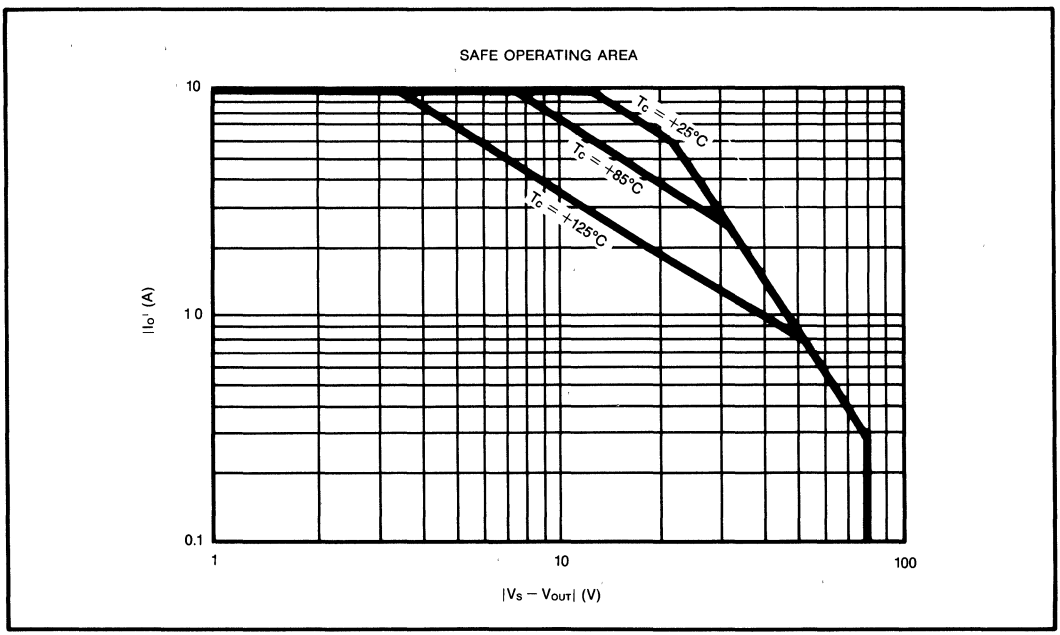


FIGURE 1. Safe Operating Area.

REPLACING HYBRID POWER AMPLIFIERS

The OPA541 can be used in applications currently using various hybrid power amplifiers, including the OPA501, OPA511, OPA512, and 3573. Of course, the application must be evaluated to assure that the output capability and other performance attributes of the OPA541 meet the necessary requirements. These hybrid power amplifiers use two current limit resistors to independently set the positive and negative current limit value. Since the OPA541 uses only one current limit resistor to set both the positive and negative current limit, only one resistor (see Figure 4) need be installed. If installed, the resistor connected to pin 2 is superfluous — it does no harm.

Because one resistor carries the current previously carried by two, the resistor may require a higher power rating. Minor adjustments may be required in the resistor value to achieve the same current limit value. Often, however, the change in current limit value when changing models is small compared to its variation over temperature. Many applications can use the same current limit resistor.

BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information table. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

APPLICATIONS CIRCUITS

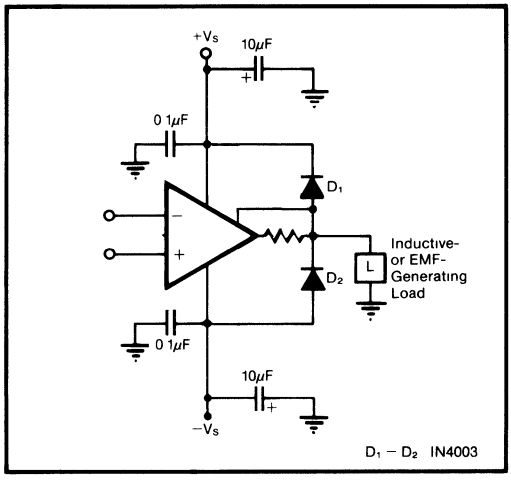


FIGURE 2. Clamping Output for EMF-Generating Loads.

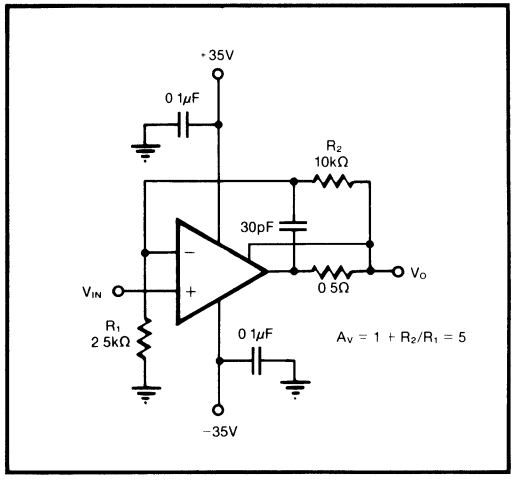


FIGURE 3. Isolating Capacitive Loads.

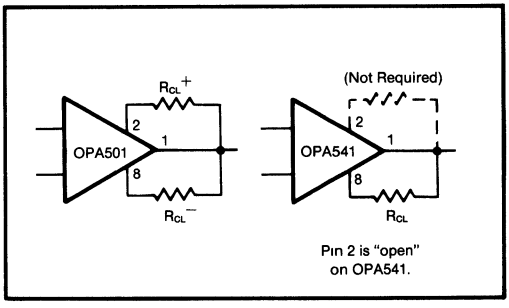


FIGURE 4. Replacing OPA501 with OPA541.

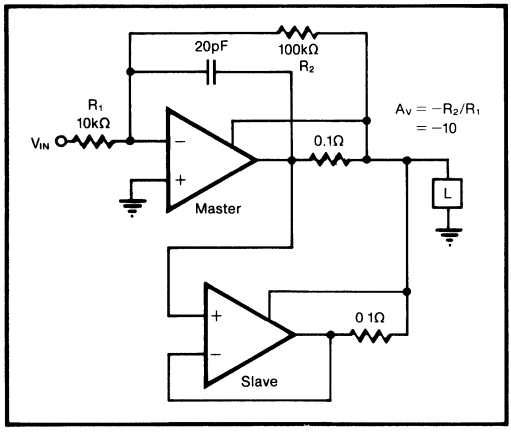


FIGURE 5. Paralleled Operation, Extended SOA.

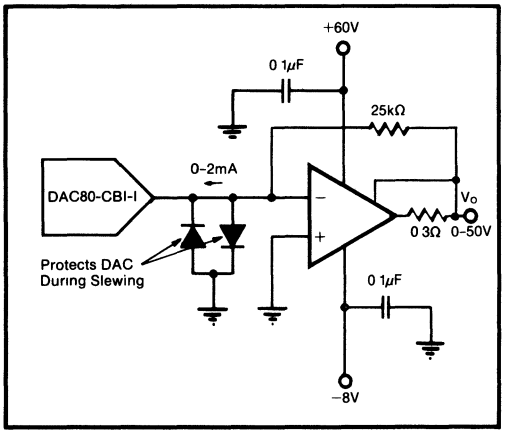


FIGURE 6. Programmable Voltage Source.

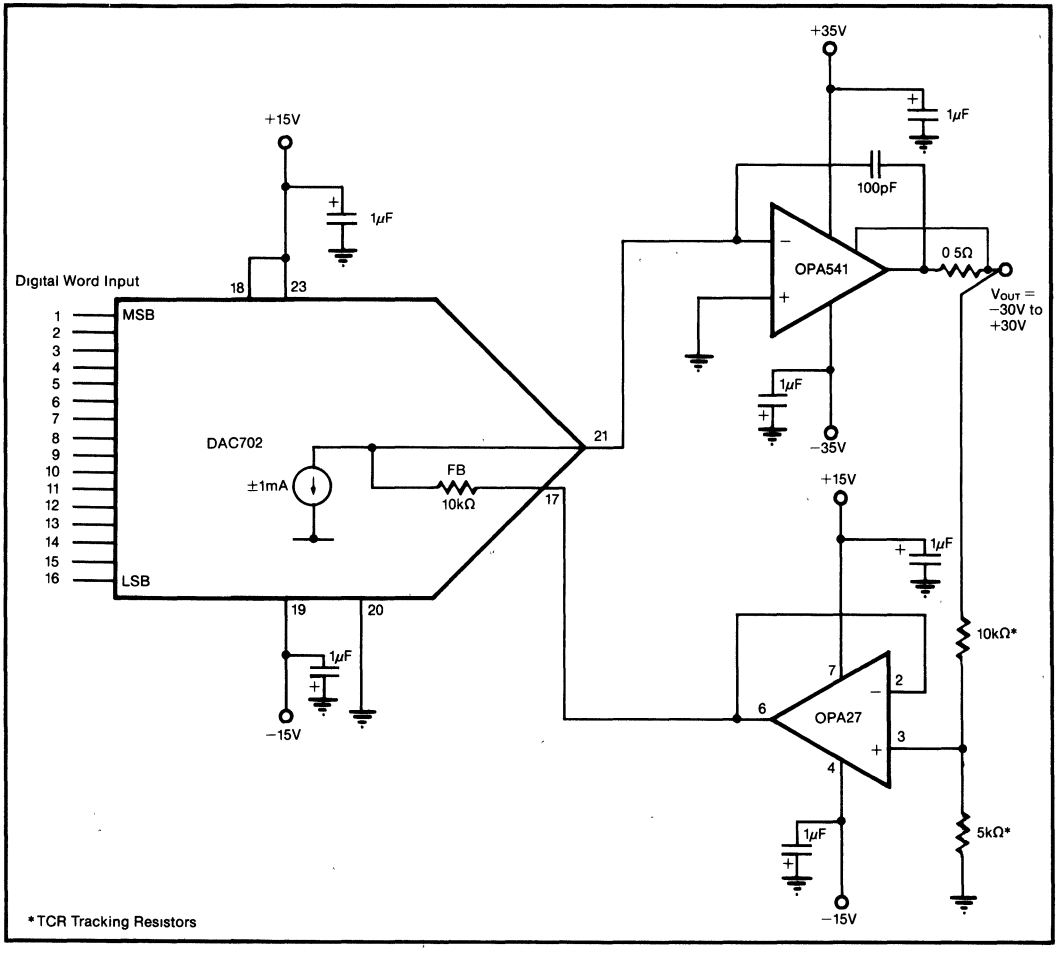


FIGURE 7. 16-Bit Programmable Voltage Source.

BURR-BROWN®

OPA550

ADVANCE INFORMATION
SUBJECT TO CHANGE

High-Power OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT CURRENT: 2A
- SOA PROTECTION CIRCUITRY
- HIGH POWER SUPPLY VOLTAGE: V_S = ±35V
- HIGH SLEW RATE: 15V/µs
- FET INPUT
- PACKAGING OPTIONS:
  Low-Cost Plastic Package
  TO-3 Metal Package

APPLICATIONS

- SERVO-MOTOR DRIVER
- PROGRAMMABLE POWER SUPPLIES
- AUDIO AMPLIFIER
- LINE DRIVER
- ATE PIN DRIVER

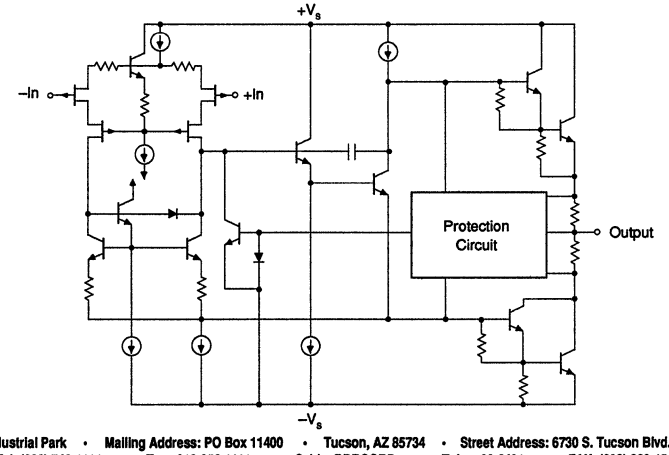
DESCRIPTION

The OPA550 is a low-cost power operational amplifier capable of outputs to ±30V at 2A. It combines the ease-of-use of a simple op amp with high-output capability for demanding loads. Its 15V/µs slew rate provides the wide power bandwidth often required in high-power applications.

Unique protection circuitry senses output and load characteristics to limit output to safe levels. The OPA550 is safe for highly reactive, as well as resistive, loads.

Laser-trimmed FET input circuitry eliminates external trimming and provides low input bias current. The OPA550 idles at low quiescent current, yet is free from troublesome cross-over distortion common with low quiescent current power amplifiers.

The OPA550 is available in a low-cost, 5-pin TO-220 package and in a TO-3 metal package. Industrial and military temperature ranges are available.



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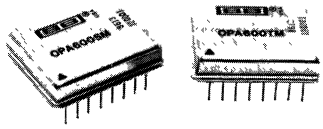
PDS-853

SPECIFICATIONS

T_C = +25°C, V_S = ±35V unless otherwise noted.

		OPA550AP/AM			OPA550SM			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OFFSET VOLTAGE								
Input Offset Voltage			0.5			*		mV
Over Specified Temperature			2.0			5		mV
Average Drift			15			20		µV/°C
Power Supply Rejection	V_S = ±10 to ±35V		90			*		dB
INPUT BIAS CURRENT								
Input Bias Current	V_{CM} = 0V		50			*		pA
Over Specified Temperature	V_{CM} = 0V		5			50		nA
Input Bias Current	V_{CM} = 0V		20			*		pA
Over Specified Temperature	V_{CM} = 0V		2			20		nA
NOISE								
Input Voltage Noise f = 1kHz			20			*		$nV/\sqrt{Hz}$
INPUT IMPEDANCE								
Differential			10			*		GΩ
Common-Mode			10			*		GΩ
INPUT VOLTAGE RANGE								
Common-mode Input Range			V_S–4V			*		V
Common-mode Rejection	V_{CM} = ±10V		90			*		dB
OPEN-LOOP GAIN								
Open-loop Voltage Gain	V_O = ±30V, R_L = 20Ω		90			*		dB
Over Specified Temperature	V_O = ±30V, R_L = 20Ω		86			*		dB
FREQUENCY RESPONSE								
Slew Rate	G = +1		15			*		V/µs
Unity-Gain Bandwidth Product			3			*		MHz
Total Harmonic Distortion	G = +10, f = 1kHz							%
OUTPUT								
Voltage Output	I_O = 2A		±V_S–5			*		V
Over Specified Temperature	I_O = 0.5A		±V_S–3.5			*		V
Current Output		2			*			A
Short Circuit Current			2.5			*		A
Output Resistance, Open-loop	1MHz		8			*		Ω
Load Capacitance			1			*		µF
POWER SUPPLY								
Specified			±35			*		V
Operating		±10		±40	*		*	V
Current, quiescent	I_O = 0		±10			*		mA
TEMPERATURE RANGE								
Specification								
AP, AM		–25		+85	*		*	°C
SM		–55		+125	*		*	°C
Storage								
AP		–40		+125	*		*	°C
AM, SM		–60		+150	*		*	°C

BURR-BROWN®



OPA600

MILITARY VERSION AVAILABLE

Fast-Settling Wideband OPERATIONAL AMPLIFIER

FEATURES

- GAIN BANDWIDTH PRODUCT: 5GHz
- FAST SETTLING: 80ns to ±0.1%
  100ns to ±0.01%
- −25°C to +85°C AND
  −55°C to +125°C TEMPERATURE RANGES
- ±10V OUTPUT: 200mA

APPLICATIONS

- FAST VCO
- HIGH-SPEED D/A CONVERTER OUTPUT AMPLIFIER
- VIDEO AMPLIFIER
- HIGH-SPEED ADC DRIVER
- LOW-DISTORTION AMPLIFIER
- TRANSMISSION LINE BUFFER

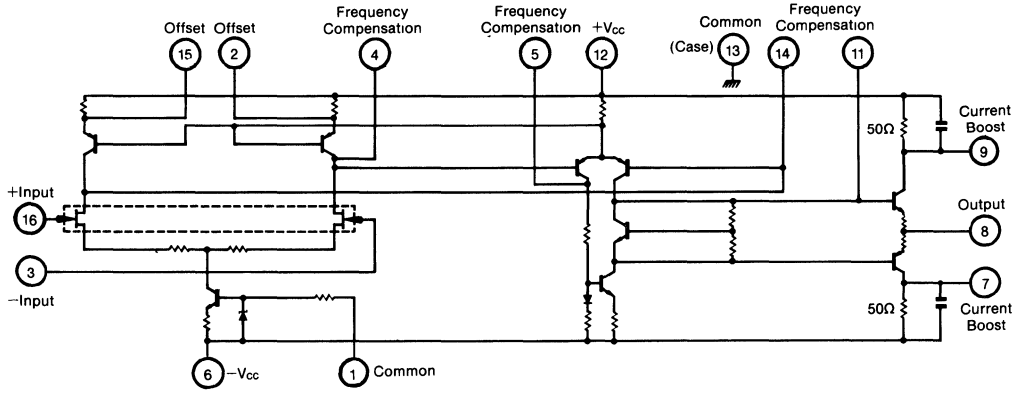
DESCRIPTION

The OPA600 is a wideband operational amplifier specifically designed for fast settling to ±0.01% accuracy. It is stable, easy to use, has good phase margin with minimum overshoot, and it has excellent DC performance. It utilizes an FET input stage to give low input bias current. Its DC stability over temperature is outstanding. The slew rate exceeds 400V/μs. All of this combines to form an outstanding amplifier for large and small signals.

High accuracy with fast settling time is achieved by using a high open-loop gain which provides the accuracy at high frequencies. The thermally balanced design maintains this accuracy without droop or thermal tail. External frequency compensation allows the user to optimize the settling time for various gains and load conditions.

The OPA600 is useful in a broad range of video, high speed test circuits and ECM applications. It is particularly well suited to operate as a voltage controlled oscillator (VCO) driver. It makes an excellent digital-to-analog converter output amplifier. It is a workhorse in test equipment where fast pulses, large signals, and 50Ω drive are important. It is a good choice for sample/holds, integrators, fast waveform generators, and multiplexers.

The OPA600 is specified over the industrial temperature range (OPA600BM, CM) and military temperature range (OPA600SM, TM). The OPA600 is housed in a welded, hermetic metal package.



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PDS-672

SPECIFICATIONS

ELECTRICAL

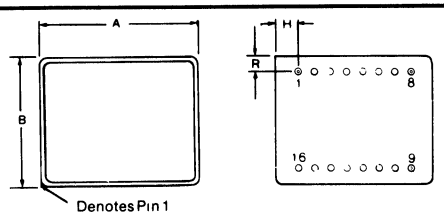
At V_{CC} = ±15VDC and T_A = +25°C unless otherwise specified

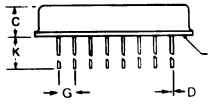
PARAMETER	CONDITIONS	OPA600CM, TM[1] MIN	OPA600CM, TM[1] TYP	OPA600CM, TM[1] MAX	OPA600BM, SM MIN	OPA600BM, SM TYP	OPA600BM, SM MAX	UNITS
OUTPUT								
Voltage	R_L = 2kΩ	±10			*			V
	R_L = 50Ω[2]	±9			*			V
Current	R_L = 50Ω[2]	±180	±200		*	*		mA
Current Pulse	R_L = 50Ω[3]	±180	±200		*	*		mA
Resistance	Open loop DC		75			*		Ω
Short-Circuit Current	To COMMON only, t_{MAX} = 1s[4]		250	300		*	*	mA
DYNAMIC RESPONSE								
Settling Time[5] to ±0.01% (±1mV)	ΔV_{OUT} = 10V		100	125		*	*	ns
to ±0.1% (±10mV)	ΔV_{OUT} = 10V		80	105		*	*	ns
to ±1% (±100mV)	ΔV_{OUT} = 10V		70	95		*	*	ns
Gain-Bandwidth Product (open-loop)	C_C = 0pF, G = 1V/V		150			*		MHz
	C_C = 0pF, G = 10V/V		500			*		MHz
	C_C = 0pF, G = 100V/V		1.5			*		GHz
	C_C = 0pF, G = 1000V/V		5			*		GHz
	C_C = 0pF, G = 10,000V/V		10			*		GHz
Bandwidth (−3dB small signal)[6]	G = +1V/V		125			*		MHz
	G = −1V/V		90			*		MHz
	G = −10V/V		95			*		MHz
	G = −100V/V		20			*		MHz
	G = −1000V/V		6			*		MHz
Full Power Bandwidth	V_{OUT} = ±5V, G = −1V/V, C_C = 3.3pF, R_L = 100Ω		16			*		MHz
Slew Rate	V_{OUT} = ±5V, G = −1000V/V, C_C = 0pF, R_L = 100Ω		500			*		V/μs
	V_{OUT} = ±5V, G = −1V/V[4]	400	440		*	*		V/μs
Phase Margin	G = −1V/V, C_C = 3.3pF		40			*		Degrees
GAIN								
Open-Loop Voltage Gain	f = DC, R_L = 2kΩ, T_A = +25°C	86	94		*	*		dB
INPUT								
Offset Voltage[7]	T_A = +25°C		±1	±4		±2	±5	mV
	T_A = −25°C to +85°C			±5			±10	mV
	T_A = −55°C to +125°C			±6			±15	mV
Offset Voltage Drift	T_A = −25°C to +85°C			±20			±80	μV/°C
	T_A = −55°C to +125°C			±20			±100	μV/°C
Bias Current	T_A = +25°C		−20	−100		*	*	pA
	T_A = −25°C to +125°C		−20	−100		*	*	nA
Offset Current	T_A = +25°C		20			*		pA
	T_A = −55°C to +125°C		20			*		nA
Power Supply Rejection Ratio	V_{CC} = ±15V, ±1V		200	500		*	*	μV/V
Common-Mode Voltage Range		−10		+7	*		*	V
Common-Mode Rejection Ratio	V_{CM} = −5V to +5V	60	80		*	*		dB
Impedance	Differential and Common-Mode		$10^{11}\|\|2$			*		Ω||pF
Voltage Noise	10kHz Bandwidth		20			*		nV/√Hz
POWER SUPPLY								
Rated (V_{CC})			±15			*		VDC
Operating Range		±9		±16	*		*	VDC
Quiescent Current			±30	±38		*	*	mA
TEMPERATURE RANGE (Ambient)[8]								
Operating BM, CM		−25		+85	*		*	°C
SM, TM		−55		+125	*		*	°C
Storage		−65		+150	*		*	°C
θ_{JC}, (junction to case)			30			*		°C/W
θ_{CA}, (case to ambient			35			*		°C/W

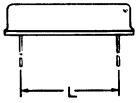
*Specification same as OPA600CM, TM

NOTES (1) BM, CM grades −25°C to +85°C SM, TM grades −55°C to +125°C (2) Pin 9 connected to +V_{CC}, pin 7 connected to −V_{CC} Observe power dissipation ratings (3) Pin 9 and pin 7 open Single pulse t = 100ns Observe power dissipation ratings. (4) Pin 9 and pin 7 open See section on Current Boost (5) G = −1V/V Optimum settling time and slew rate achieved by individually compensating each device Refer to section on Compensation (6) Frequency compensation as discussed in section on Compensation (7) Adjustable to zero. (8) Heat Sink (optional): IERC LBOCI-72CB with 2 each DCV-1B Clamps

MECHANICAL



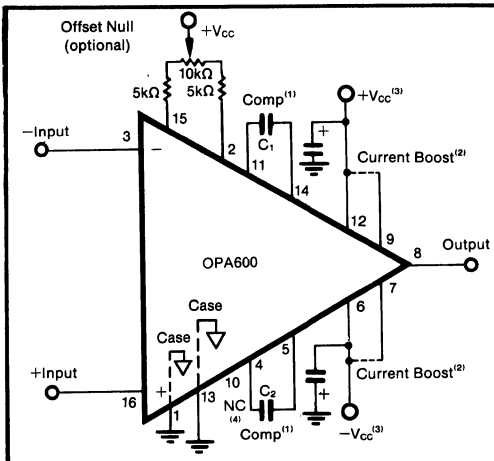




DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	963	980	24 46	24 89
B	760	805	19 30	20 45
C	175	190	4 45	4 83
D	014	022	0 36	0 56
G	100 BASIC		2 54 BASIC	
H	135	155	3 43	3 94
K	230	270	5 84	6 86
L	600 BASIC		15 24 BASIC	
R	095	115	2 41	2 92

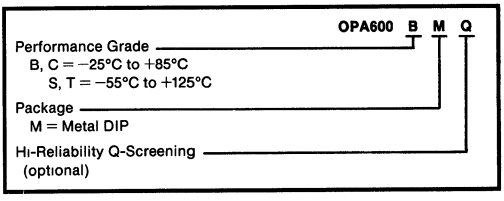
NOTES
1 Leads in true position within 0 010" (0 25mm) R at MMC at seating plane
2 Pin numbers shown for reference only

CONNECTION DIAGRAM



NOTES (1) Refer to Figure 4 for recommended frequency compensation (2) Connect pin 9 to pin 12 and connect pin 7 to pin 6 for maximum output current See Application Information for further information (3) Bypass each power supply lead as close as possible to the amplifier pins A 1μF CS13 tantalum capacitor is recommended (4) There is no internal connection An external connection may be made (5) It is recommended that the amplifier be mounted with the case in contact with a ground plane for good thermal transfer and optimum AC performance

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS(1)

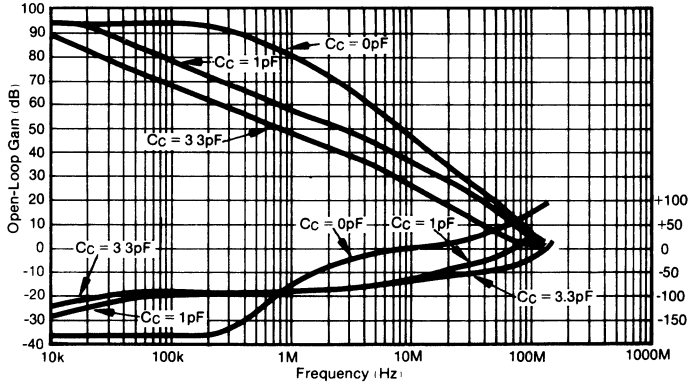
Supply Voltage, +Vcc to −Vcc	±17V
Power Dissipation, At TCASE +125°C(2)	1 6W
Input Voltage Differential	±Vcc
Common-Mode	±Vcc
Output Short Circuit Duration to Common	<5sec
Temperature: Pin (soldering, 20sec)	+300°C
Junction(1), TJ	+175°C
Temperature Range Storage	−65°C to +150°C
Operating (case)	−55°C to +125°C

NOTES (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device Exposure to absolute maximum conditions for extended periods may affect device reliability (2) Long term operation at the maximum junction temperature will result in reduced product life Derate internal power dissipation to achieve high MTTF

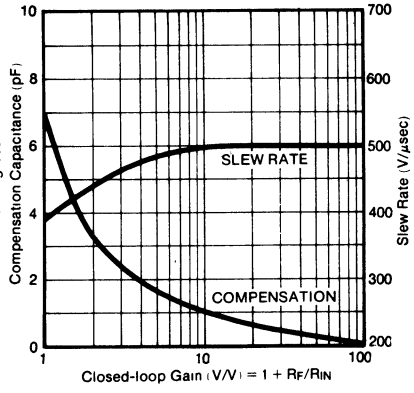
TYPICAL PERFORMANCE CURVES

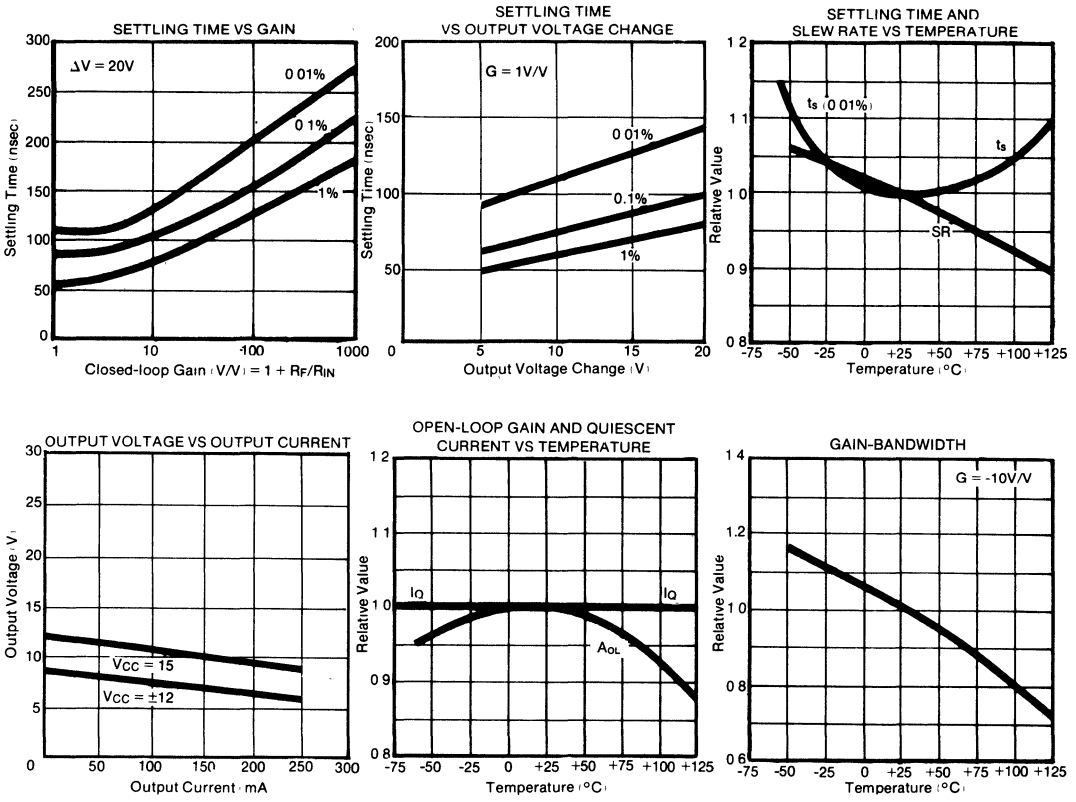
Typical at T_A = +25°C and ±V_{CC} = 15VDC, unless otherwise specified

BODE PLOT



COMPENSATION AND SLEW RATE VS GAIN





INSTALLATION AND OPERATION

WIRING PRECAUTIONS

The OPA600 is a wideband, high frequency operational amplifier with a gain-bandwidth product exceeding 5GHz. This capability can be realized by observing a few wiring precautions and using high frequency layout techniques. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths and should be as short as possible. The entire physical circuit should be as small as is practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the input terminals of the amplifier and compensation pins. Stray signal coupling from the output to the input should be minimized. All circuit element leads should be as short as possible and low values of resistance should be used. This will give the best circuit performance as it will minimize the time constants formed with the circuit capacitances and will eliminate stray, unwanted tuned circuits.

Grounding is the most important application consideration for the OPA600, as it is with all high frequency circuits. Ultra-high frequency transistors are used in the design of the OPA600 and oscillations at frequencies of 500MHz and above can be stimulated if good grounding techniques are not used. A ground plane is highly recommended. It should connect all areas of the pattern side of the printed circuit that are not otherwise used. The ground plane provides a low resistance, low inductance common return path for all signal and power returns. The ground plane also reduces stray signal pickup.

Point-to-point wiring is not recommended. However, if point-to-point wiring is used, a single-point ground should be used. The input signal return, the load signal return and the power supply common should all be connected at the same physical point. This eliminates common current paths or ground loops which can cause unwanted feedback.

Each power supply lead should be bypassed to ground as near as possible to the amplifier pins. A 1μF CS13 tantalum capacitor is recommended. A parallel 0.01μF ceramic may be added if desired. This is especially important when driving high current loads. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

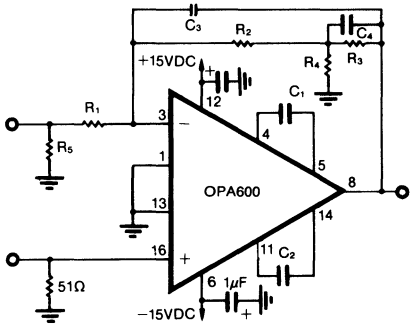
OPA600 circuit common is connected to pins 1 and 13; these pins should be connected to the ground plane. The input signal return, load return, and power supply commmon should also be connected to the ground plane.

The case of the OPA600 is internally connected to circuit common, and as indicated above, pins 1 and 13 should be connected to the ground plane. Ideally, the case should be mechanically connected to the ground plane for good thermal transfer, but because this is difficult in practice, the OPA600 should be fully inserted into the printed circuit board with the case very close to the ground plane to make the best possible thermal connection. If the case and ground plane are physically connected or are in close thermal proximity, the ground plane will provide heat sinking which will reduce the case temperature rise. The minimum OPA600 pin length will minimize lead inductance, thereby maximizing performance.

COMPENSATION

The OPA600 uses external frequency compensation so that the user may optimize the bandwidth or settling time for his particular application. Several performance curves aid in the selection of the correct compensations capacitance value. The Bode plot shows amplitude and phase versus frequency for several values of compensation. A related curve shows the recommended compensation capacitance versus closed-loop gain.

Figure 1 shows a recommended circuit schematic. Component values and compensation for amplifiers with several different closed-loop gains are shown. This circuit will yield the specified settling time. Because each device is unique and slightly different, as is each user's circuit, optimum settling time will be achieved by individually compensating each device in its own circuit, if desired. A 10% to 20% improvement in settling time has been experienced from the values indicated in the Electrical Specifications table.



Closed Loop Gain	R_1	R_2	R_3	R_4	C_1, C_2	C_3	C_4	R_5
+1	open	100	short	open	6.8	0	0	--
−1	620	620	short	open	3.3	4.7	0	56
−10	100	1k	short	open	1	2.2	0	100
−100	100	3.3k	3.3k	3.2k	0	1	0	100
−1000	100	3.3k	3.3k	116	0	0	4.7	100

FIGURE 1. Recommended Amplifier Circuits and Frequency Compensation.

The primary compensation capacitors are C_1 and C_2 (see Figure 1). They are connected between pins 4 and 5 and between pins 11 and 14. Both C_1 and C_2 should be the same value. As Figure 1 and the performance curves show, larger closed-loop configurations require less capacitance and improved gain-bandwidth product can be realized. Note that no compensation capacitor is required for closed-loop gains equal to or above 100V/V. If upon initial application the user's circuit is unstable, and remains so after checking for proper bypassing, grounding, etc., it may be necessary to increase the compensation slightly to eliminate oscillations. Do not over compensate. It should not be necesary to increase C_1 and C_2 beyond 10pF to 15pF. It may also be necessary to individually optimize C_1 and C_2 for improved performance.

The flat high frequency response of the OPA600 is preserved and high frequency peaking is minimized by connecting a small capacitor in parallel with the feedback resistor (see Figure 1). This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier, typically 2pF, and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. It will typically be 2pF for a clean layout using low resistances (1kΩ) and up to 10pF for circuits using larger resitances. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator is recommended to avoid using a large value resistor with its long time constant.

CAPACITIVE LOADS

The OPA600 will drive large capacitive loads (up to 100pF) when properly compensated and settling times of under 150ns are achievable. The effect of a capacitive load is to decrease the phase margin of the amplifier, which may cause high frequency peaking or oscillations. A solution is to increase the compensation capacitance, somewhat slowing the amplifier's ability to respond. The recommended compensation capacitance value as a function of load capacitance is shown in Figure 2. (Use two capcitors, each with the value indicated.) Alternately, without increasing the OPA600's compensation capacitance, the capacitive load may be buffered by connecting a small resistance, usually 5Ω to 50Ω, in series with the Output, pin 8.

For very-large capacitive loads, greater than 100pF, it will be necessary to use doublet compensation. Refer to Figure 3 and discussion on slew rate. This places the dominant pole at the input stage. Settling time will be approximately 50% slower; slew rate should increase. Load capacitance should be minimized for optimum high frequency performance.

Because of its large output capability, the OPA600 is particularly well suited for driving loads via coaxial

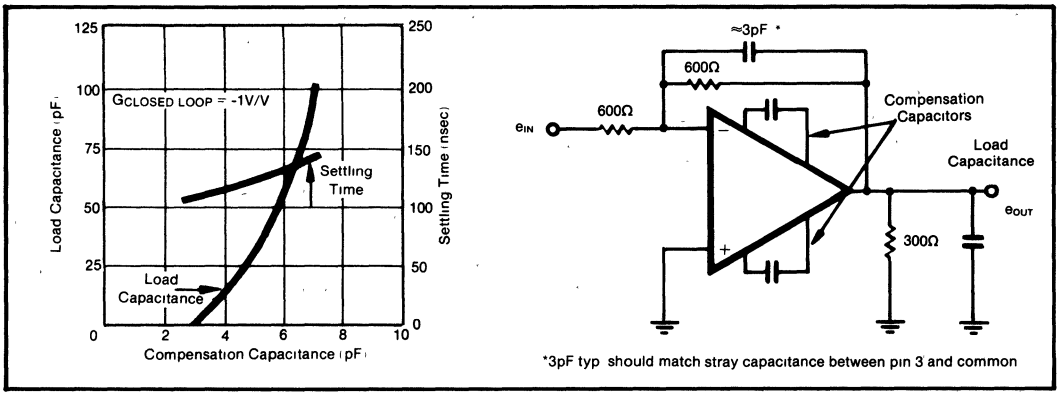


FIGURE 2. Capacitive Load Compensation and Response.

cables. Note that the capacitance of coaxial cable (29pF/foot of length for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the magnitude of the output transition, a 10V step.

Settling time is a complete dynamic measure of the OPA600's total performance. It includes the slew rate time, a large signal dynamic parameter, and the time to accurately reach the final value, a small signal parameter that is a function of bandwidth and open-loop gain. Performance curves show the OPA600 settling time to ±1%, ±0.1%, and ±0.01%. The best settling time is achieved in low closed-loop gain circuits.

Settling time is dependent upon compensation. Under-compensation will result in small phase margin, overshoot or instability. Over-compensation will result in poor settling time.

Figure 1 shows the recommended compensation to yield the specified settling time. Improved or optimum settling time may be achieved by individually compensating each device in the user's circuit since individual devices vary slightly from one to another, as do user's circuits.

SLEW RATE

Slew rate is primarily an output, large signal parameter. It has virtually no dependence upon the closed-loop gain or small signal bandwidth. Slew rate is dependent upon compensation and decreasing the compensation capacitor value will increase the available slew rate as shown in the performance curve.

The OPA600 slew rate may be increased by using an alternate compensation as shown in Figure 3. The slew rate will increase between 700 and 800V/μs typical, with 0.01% settling time increasing to between 175 and 190ns typical, and 0.1% settling time increasing to between 110 and 120ns typical.

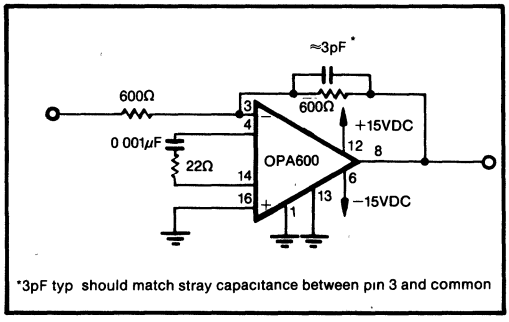


FIGURE 3. Amplifier Circuit for Increased Slew Rate.

For alternate doublet compensation refer to Figure 3. For a closed-loop gain equal to −1, delete C_1 and C_2 and add a series RC circuit (R = 22Ω, C = 0.01μF) between pins 14 and 4. Make no connections to pins 11 and 5. Absolutely minimze the capacitance to these pins. If a connector is used for the OPA600, it is recommended that sockets for pins 11 and 5 be removed. For a PC board mount, it is recommended that the PC board holes be overdrilled for pins 11 and 5 and adjacent ground plane copper be removed. Effectively this compensation places the dominant pole at the input stage, allowing the output stage to have no compensation and to slew as fast as possible. Bandwidth and settling time are impaired only slightly. For closed-loop gains other than −1, different values of R and C may be required.

OFFSET ADJUSTMENT

The offset voltage of the OPA600 may be adjusted to zero by connecting a 5kΩ resistor in series with a 10kΩ linear potentiometer in series with another 5kΩ resistor between pins 2 and 15, as shown in Figure 4. It is important that one end of each of the two resistors be located very close to pins 2 and 15 to isolate and avoid loading these sensitive terminals. The potentiometer should be a small noninductive type with the wiper connected to the positive supply. The leads connecting these components should be short, no longer than 0.5-inch, to avoid stray capacitance and stray signal pick-up. If the potentiometer must be located away from the immediate vicin-

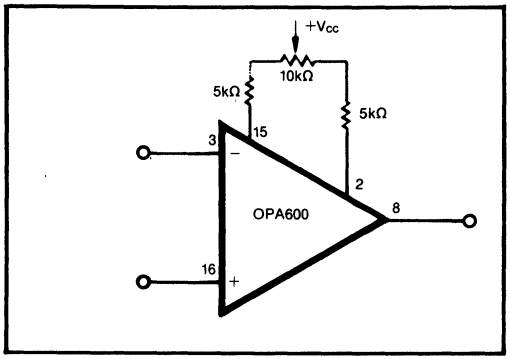


FIGURE 4. Offset Null Circuit.

ity of the OPA600, extreme care must be observed with the sensitive leads. Locate the two 5kΩ resistors very close to pins 2 and 15.

Never connect $+V_{CC}$ directly to pin 2 or 15. Do not attempt to eliminate the 5kΩ resistors because at extreme rotation, the potentiometer will directly connect $+V_{CC}$ to pin 2 or 15 and permanent damage will result.

Offset voltage adjustment is optional. The potentiometer and two resistors are omitted when the offset voltage is considered sufficiently low for the particular application. For each microvolt of offset voltage adjusted, the offset voltage temperature sensitivity will change by $\pm 0.004\mu V/°C$.

CURRENT BOOST

External ability to bypass the internal current limiting resistors has been provided in the OPA600. This is referred to as current boost. Current boost enables the OPA600 to deliver large currents into heavy loads (±200mA at ±10V). To bypass the resistors and activate the current boost, connect pin 7 to $-V_{CC}$ at pin 6 with a short lead to minimize lead inductance and connect pin 9 to $+V_{CC}$ at pin 12 with a short lead.

CAUTION—Activating current boost by bypassing the internal current limiting resistors can permanently damage the OPA600 under fault conditions. See section on short circuit protection.

Not activating current boost is especially useful for initial breadboarding. The 50Ω (±5%) current limiting resistor in the collector circuit of each of the output transistors causes the output transistors to saturate; this limits the power dissipation in the output stage in case of a fault. Operating with the current boost not activated may also be desirable with small-signal outputs (i.e., ±1V) or when the load current is small.

Each resistor is internally capacitively-bypassed (0.01μF, ±20%) to allow the amplifier to deliver large pulses of current, such as to charge diode junctions or circuit capacitance and still respond quickly. The length of time that the OPA600 can deliver these current pulses is limited by the RC time constant.

The internal voltage drops, output voltage available, power dissipation, and maximum output current can be determined for the user's application by knowing the load resistance and computing:

$$V_{OUT} = 14\,[R_{LOAD} \div (50 + R_{LOAD})]$$

This applies for R_{LOAD} less than 100Ω and the current boost not activated. When R_{LOAD} is large, the peak output voltage is typically ±11V, which is determined by other factors within the OPA600.

SHORT-CIRCUIT PROTECTION

The OPA600 is short-circuit-protected for momentary short to common (<5s), typical of those enountered when probing a circuit during experimental breadboarding or troubleshooting. This is true only if pins 7 and 9 are open (current boost not activated). An internal 50Ω resistor is in series with the collector of each of the output transistors, which under fault conditions will cause the output transistors to saturate and limit the power dissipation in the output stage. Extended application of an output short can damage the amplifier due to excessive power dissipation.

The OPA600 is not short-circuit-protected when the current boost is activated. The large output current capability of the OPA600 will cause excessive power dissipation and permanent damage will result even for momentary shorts to ground.

Output shorts to either supply will destroy the OPA600 whether the current boost is activated or not.

HEAT SINKING AND POWER DISSIPATION

The OPA600 is intended as a printed circuit board mounted device, and as such does not require a heat sink. It is specified for ambient temperature operation from −55°C to +125°C. However, the power dissipation must be kept within safe limits. At extreme temperature and under full load conditions, some form of heat sinking will be necessary. The use of a heat sink, or other heat dissipating means such as proximity to the ground plane, will result in cooler operating temperatures, better temperature performance, and improved reliability.

It may be necessary to physically connect the OPA600 to the printed circuit board ground plane, attach fins, tabs, etc., to dissipate the generated heat. Because of the wide variety of possibilities, this task is left to the user. For all applications it is recommended that the OPA600 be fully inserted into the printed circuit board and that the pin length be short. Heat will be dissipated through the ground plane and the AC performance will be its best.

With a maximum case temperature of +125°C and not exceeding the maximum junction of +175°C, a maximum power dissipation of 600mW is allowed in either output transistor.

TESTING

For static and low frequency dynamic measurements, the OPA600 may be tested in conventional operational amplifier test circuits, provided proper ground techniques are observed, excessive lead lengths are avoided, and care is maintained to avoid parasitic oscillations. The circuit in Figure 3 is recommended for low frequency functional testing, incoming inspection, etc. This circuit is less susceptible to stray capacitance, excessive lead length, parasitic tuned circuits, changing capacitive loads, etc. It does not yield optimum settling time. We recommend placing a resistor (approximately 300Ω) in series with each piece of test equipment, such as a DVM, to isolate loading effects on the OPA600.

To realize the full performance capabilities of the OPA600, high frequency techniques must be employed and the test fixture must not limit the amplifier. Settling time is the most critical dynamic test and Figure 5 shows a recommended OPA600 settling time test circuit schematic. Good grounding, truly square drive signals, minimum stray coupling, and small physical size are important.

The input pulse generator must have a flat topped, fast settling pulse to measure the true settling time of the amplifier. A circuit that generates a ±5V flat topped pulse is shown in Figure 6.

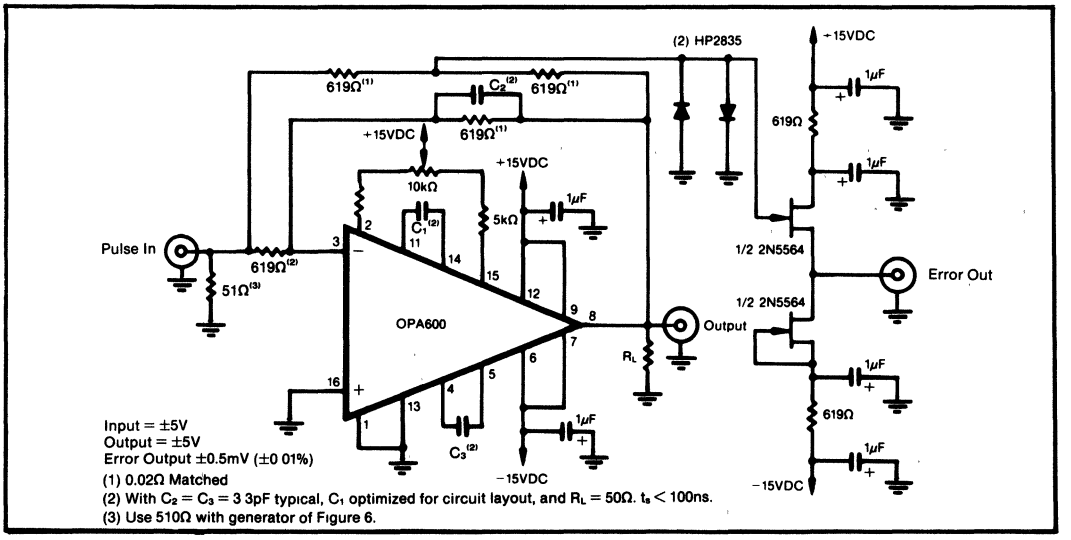


FIGURE 5. Settling Time and Slew Rate Test Circuit.

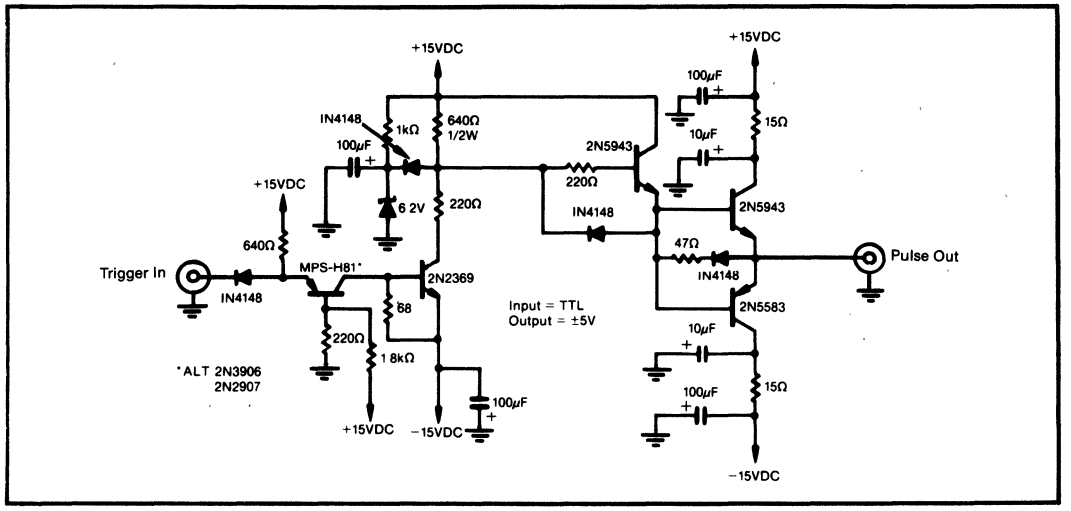
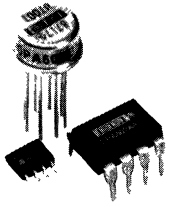


FIGURE 6. Flat Top Pulse Generator.

BURR-BROWN®



OPA602

MILITARY & DIE VERSIONS AVAILABLE

High-Speed Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 6.5MHz
- HIGH SLEW RATE: 35V/μs
- LOW OFFSET: ±250μV max
- LOW BIAS CURRENT: ±1pA max
- FAST SETTLING: 1μs to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DATA CONVERSION

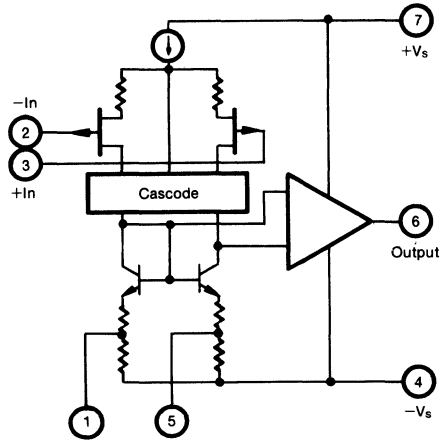
DESCRIPTION

The OPA602 is a precision, wide bandwidth FET operational amplifier. Monolithic *Difet* (dielectrically isolated FET) construction provides an unusual combination of high speed and accuracy.

Its wide-bandwidth design minimizes dynamic errors. High slew rate and fast settling time allow accurate signal processing in pulse and data conversion applications. Wide bandwidth and low distortion minimize AC errors. All specifications are rated with a 1kΩ resistor in parallel with 500pF load. The OPA602 is unity-gain stable and easily drives capacitive loads up to 1500pF.

Laser-trimmed input circuitry provides offset voltage and drift performance normally associated with precision bipolar op amps. *Difet* construction achieves extremely low input bias currents (1pA max) without compromising input voltage noise.

The OPA602's unique input cascode circuitry maintains low input bias current and precise input characteristics over its full input common-mode voltage range.



Difet® Burr-Brown Corp

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-753B

SPECIFICATIONS

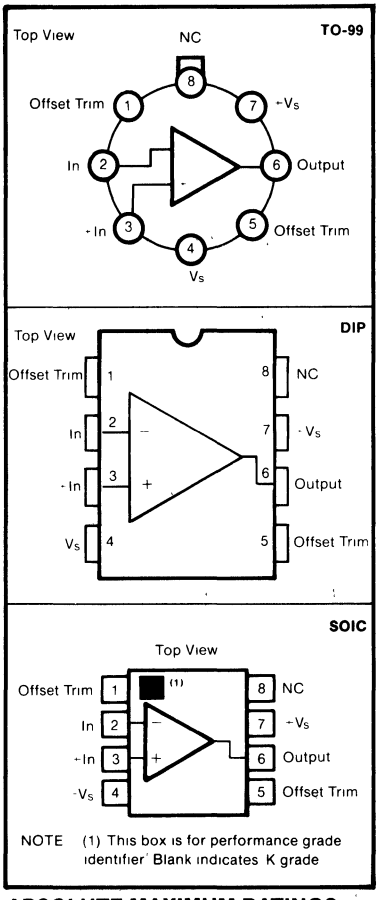
ELECTRICAL

At V_S = ±15VDC and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA602AM/AP/AU			OPA602BM/SM/BP			OPA602CM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE											
Voltage: f_O = 10Hz			*			23			*		nV/√Hz
f_O = 100Hz			*			19			*		nV/√Hz
f_O = 1kHz			*			13			*		nV/√Hz
f_O = 10kHz			*			12			*		nV/√Hz
f_B = 10Hz to 10kHz			*			1.4			*		µVrms
f_B = 0.1Hz to 10Hz			*			0.95			*		µVp-p
Current f_B = 0.1Hz to 10Hz			*			12			*		fAp-p
f_O = 0.1Hz to 20kHz			*			0.6			*		fA/√Hz
OFFSET VOLTAGE											
Input Offset Voltage											
"M" Package	V_{CM} = 0VDC		±300	±1000		±150	±500		±100	±250	µV
"P" Package			1	2		0.5	1				mV
"U" Package			1	3							mV
Over Specified Temp:											
"M" Package			±550			±250	±1000		±200	±500	µV
"P", "U" Packages			±1.5			±0.75	±1.5				mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		*	±15		±3	±5		*	±2	µV/°C
Supply Rejection	$±V_S$ = 12V to 18V	70	*		80	100		86	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		±2	±10		±1	±2		±0.5	±1	pA
Over Specified Temp.			±20	±500		±20	±200		±10	±100	pA
SM Grade						±200	±2000				pA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC	1	10		0 5	2		0.5	1	pA	
Over Specified Temp.			20	500		20	200		10	100	pA
SM Grade						200	1000				pA
INPUT IMPEDANCE											
Differential			*			10^{13}‖1			*		Ω‖pF
Common-Mode			*			10^{14}‖3			*		Ω‖pF
INPUT VOLTAGE RANGE											
Common-Mode Input Range		*	*		±10.2	+13, −11		*	*		V
Common-Mode Rejection	V_{IN} = ±10VDC	75	*		88	100		92	*		dB
OPEN LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 1k\Omega$	75	*		88	100		92	*		dB
FREQUENCY RESPONSE											
Gain Bandwidth	Gain = 100	3 5	*		4	6.5		5	*		MHz
Full Power Response	20Vp-p, R_L = 1kΩ		*			570			*		kHz
Slew Rate	V_O = ±10V, R_L = 1kΩ	20	*		24	35		28	*		V/µs
Settling Time. 0.1%	Gain = −1, R_L = 1kΩ		*			0.6			*		µs
0.01%	C_L = 500pF, 10V step		*			1.0			*		µs
RATED OUTPUT											
Voltage Output	R_L = 1kΩ	±11	*		±11.5	+12.9, −13.8			*	*	V
Current Output	V_O = ±10VDC	*	*		±15	±20		*	*		mA
Output Resistance	1MHz, open loop		*			80			*		Ω
Load Capacitance Stability	Gain = +1		*			1500			*		pF
Short Circuit Current		±25	*		±30	±50		*	*		mA
POWER SUPPLY											
Rated Voltage			*			±15			*		VDC
Voltage Range,											
Derated Performance		*		*	±5		±18	*		*	VDC
Current, Quiescent	I_O = 0mADC		*	*		3	4		*	*	mA
Over Specified Temp.			*	*		3.5	4.5		*	*	mA
TEMPERATURE RANGE											
Specification	Ambient temp.	*		*	−25		+85	*		*	°C
SM Grade					−55		+125				°C
Operating: "M" Package	Ambient temp.	*		*	−55		+125	*		*	°C
"P", "U" Packages		−25		+85	−25		+85				°C
Storage. "M" Package	Ambient temp.	*		*	−65		+150	*		*	°C
"P", "U" Packages		−40		+125	−40		+125				°C
θ Junction-Ambient			*			200			*		°C/W

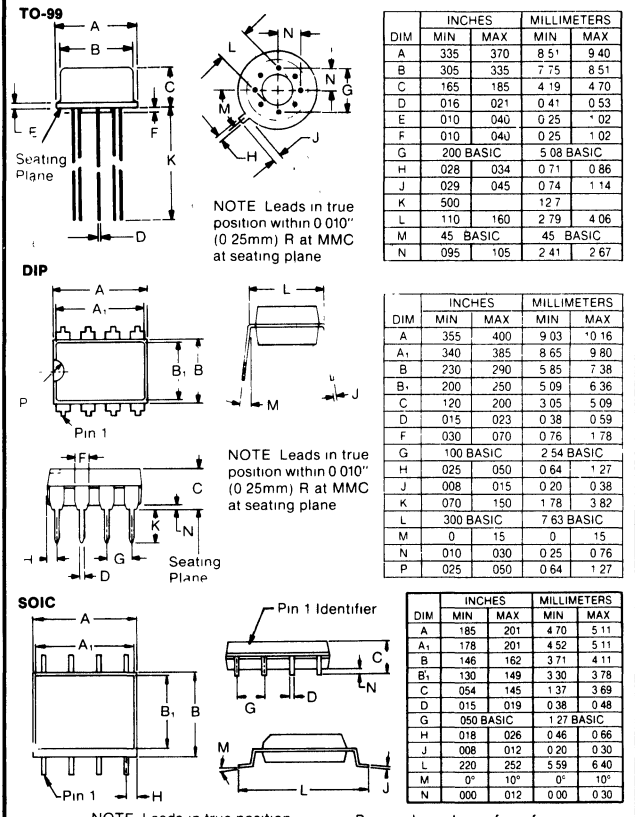
*Specification same as OPA602BM

CONNECTION DIAGRAMS



NOTE (1) This box is for performance grade identifier. Blank indicates K grade.

MECHANICALS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.355	.400	9.03	10.16
A_1	.340	.385	8.65	9.80
B	.230	.290	5.85	7.38
B_1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.025	.050	0.64	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.201	4.70	5.11
A_1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B_1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

ABSOLUTE MAXIMUM RATINGS

Supply	+18VDC
Internal Power Dissipation ($T_J \leq +175°C$)	+1000mW
Differential Input Voltage	Total V_S
Input Voltage Range	$\pm V_S$
Storage Temperature Range	"M" −65°C to +150°C "U", "P" −40°C to +125°C
Operating Temperature Range	"M" −55°C to +125°C "U", "P" −25°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to ground (+25°C)	Continuous
Junction to Temperature	+175°C

ORDERING INFORMATION

Model	Package	Temperature Range	Offset Voltage max (μV)
OPA602AM	TO-99	−25°C to +85°C	±1000
OPA602BM	TO-99	−25°C to +85°C	±500
OPA602CM	TO-99	−25°C to +85°C	±250
OPA602SM	TO-99	−55°C to +125°C	±500
OPA602AP	Plastic DIP	−25°C to +85°C	±1000
OPA602BP	Plastic DIP	−25°C to +85°C	±500
OPA602AU	Plastic SOIC	−25°C to +85°C	±1000

BURN-IN SCREENING OPTION

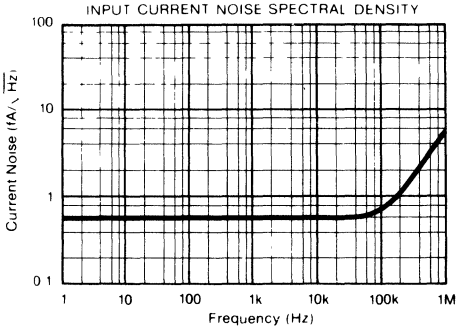
Model	Package	Temperature Range	Burn-In Temp. (160h)(1)
OPA602AM-BI	TO-99	−25°C to +85°C	+125°C
OPA602CM-BI	TO-99	−25°C to +85°C	+125°C
OPA602SM-BI	TO-99	−55°C to +125°C	+125°C
OPA602AP-BI	Plastic	−25°C to +85°C	+85°C
OPA602BP-BI	Plastic	−25°C to +85°C	+85°C
OPA602AU-BI	Plastic SOIC	−25°C to +85°C	+85°C

NOTE (1) Or equivalent combination of time and temperature

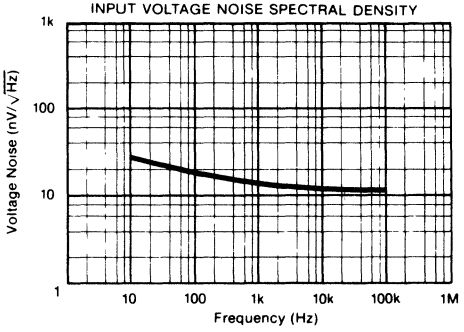
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15VDC unless otherwise noted

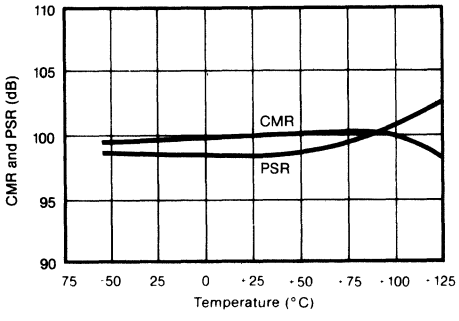
INPUT CURRENT NOISE SPECTRAL DENSITY



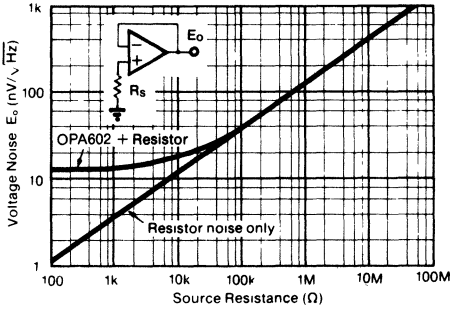
INPUT VOLTAGE NOISE SPECTRAL DENSITY



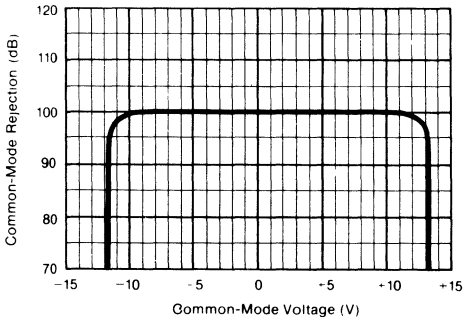
POWER SUPPLY REJECTION AND COMMON-MODE REJECTION vs TEMPERATURE



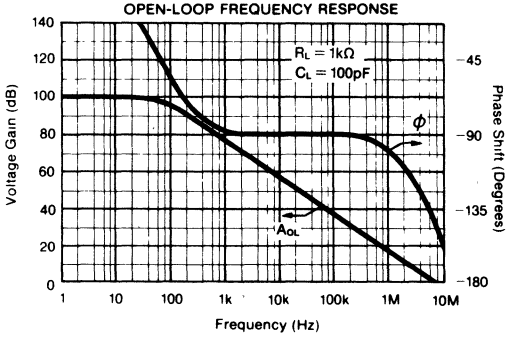
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



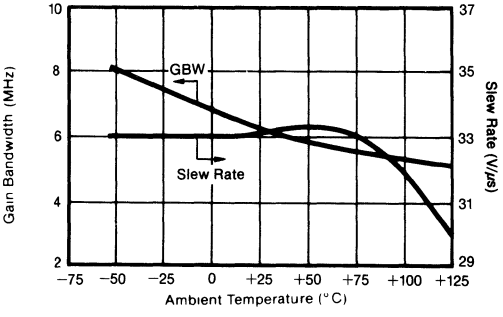
COMMON-MODE REJECTION vs INPUT COMMON MODE VOLTAGE



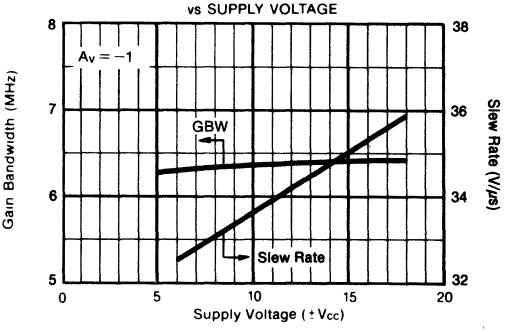
OPEN-LOOP FREQUENCY RESPONSE



GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



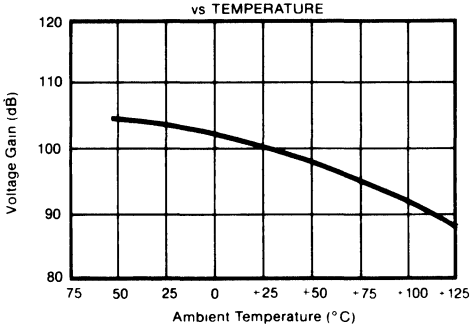
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



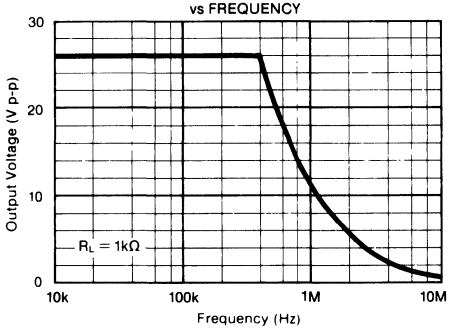
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15VDC unless otherwise noted

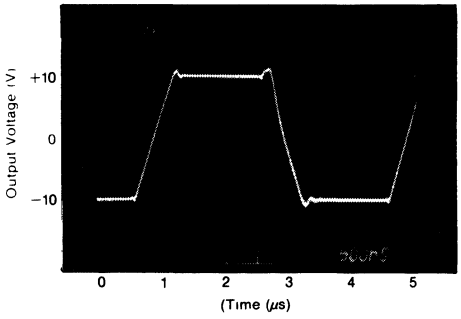
OPEN-LOOP GAIN vs TEMPERATURE



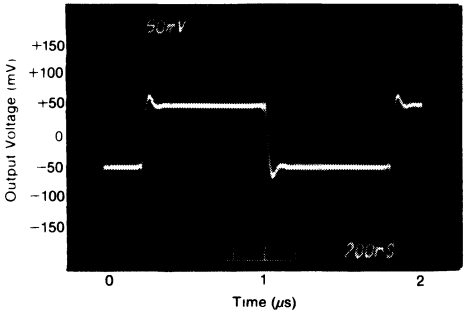
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



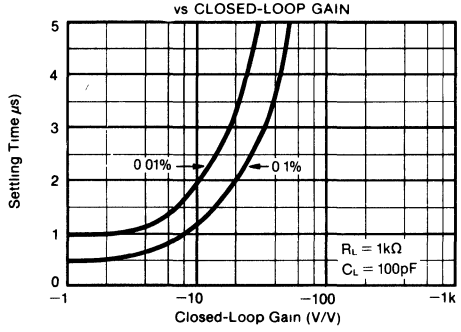
LARGE SIGNAL TRANSIENT RESPONSE



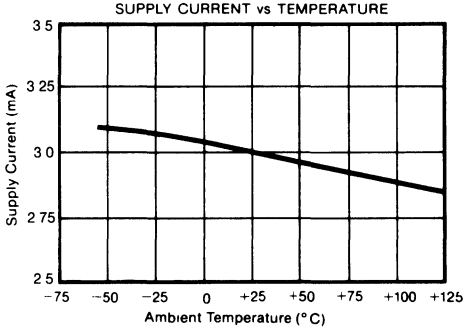
SMALL SIGNAL TRANSIENT RESPONSE



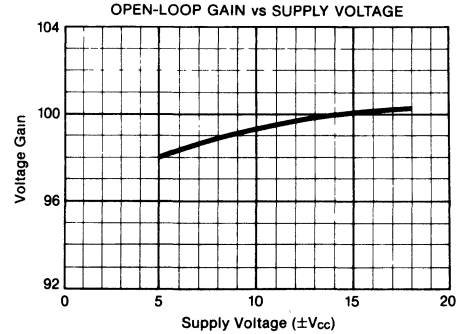
SETTLING TIME vs CLOSED-LOOP GAIN



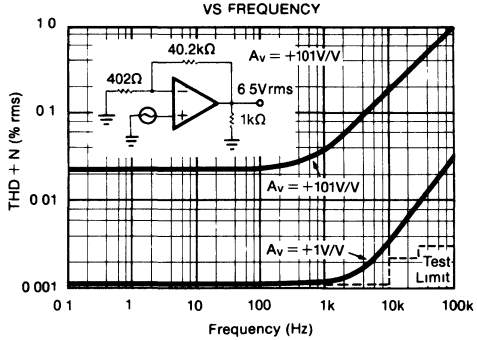
SUPPLY CURRENT vs TEMPERATURE



OPEN-LOOP GAIN vs SUPPLY VOLTAGE

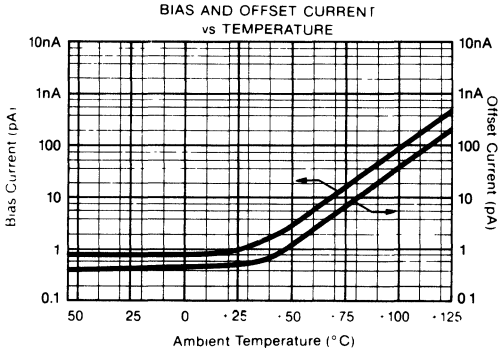


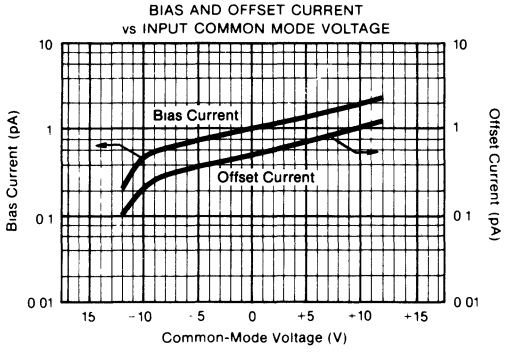
TOTAL HARMONIC DISTORTION VS FREQUENCY

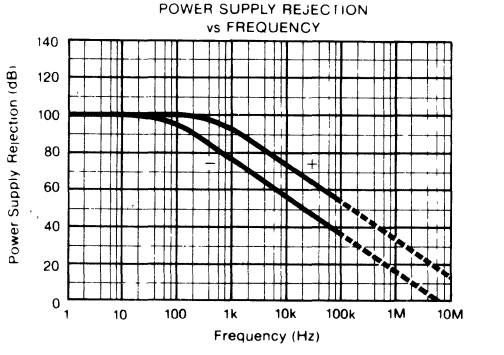


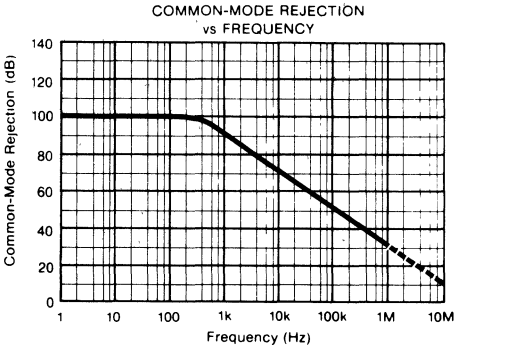
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15VDC unless otherwise noted









APPLICATIONS INFORMATION

Unity-gain stability with good phase margin and excellent output drive characteristics bring freedom from the subtle problems associated with other high speed amplifiers. But with any high speed, wide bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance —especially at the inverting input pin.

Power supplies should be bypassed with good high frequency capacitors positioned close to the op amp pins. In most cases 0.1μF ceramic capacitors are adequate. Applications with heavier loads and fast transient waveforms may benefit from use of 1.0μF tantalum bypass capacitors.

INPUT BIAS CURRENT GUARDING

Leakage currents across printed circuit boards can easily exceed the input bias current of the OPA602. A circuit board "guard" pattern (Figure 1) is an effective solution to difficult leakage problems. By surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential, leakage currents will flow harmlessly to the low impedance node.

Input bias current may also be degraded by improper handling or cleaning. Contamination from handling parts

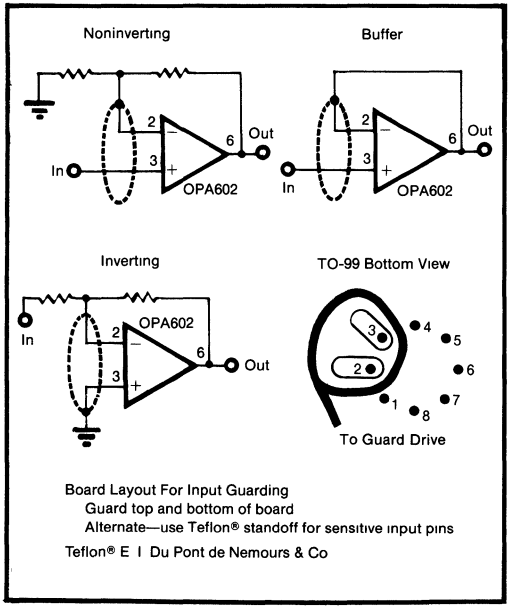


FIGURE 1. Connection of Input Guard.

and circuit boards may be cleaned with appropriate solvents and de-ionized water. Each rinsing operation should be followed by a 30-minute bake at +85°C.

BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information table. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

APPLICATION CIRCUITS

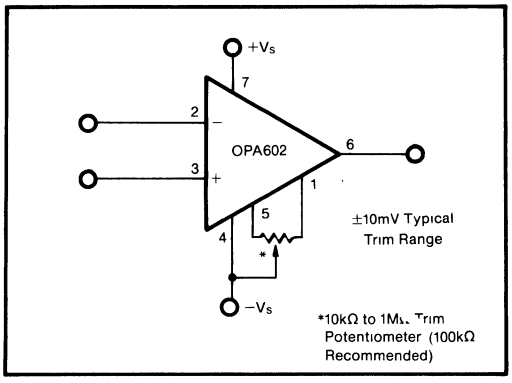


FIGURE 2. Offset Voltage Trim.

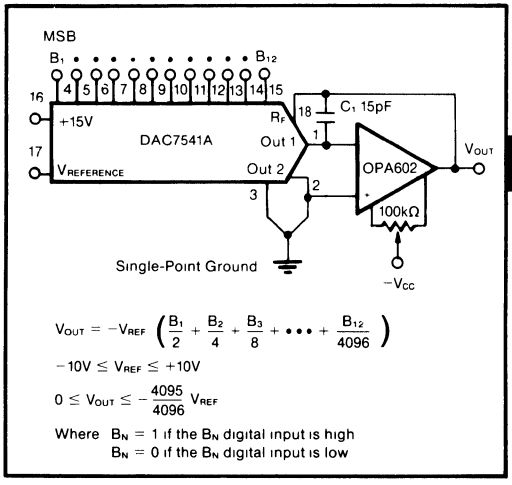


FIGURE 3. Voltage Output D/A Converter.

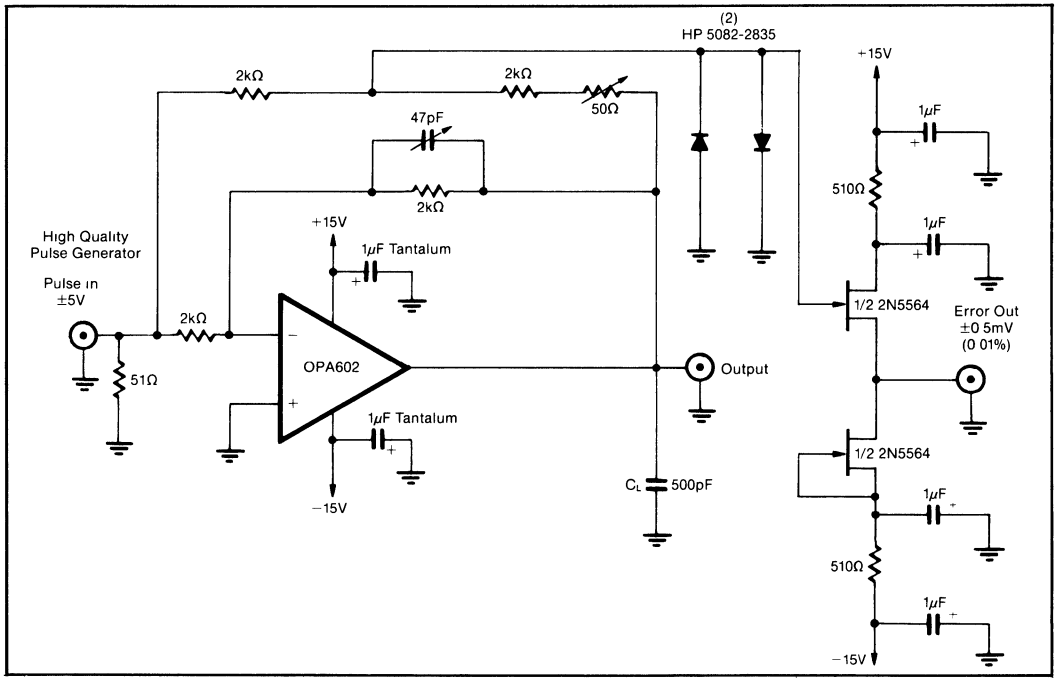
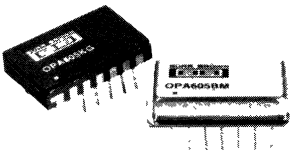


FIGURE 4. Settling Time and Slew Rate Test Circuit.

BURR-BROWN®

OPA605



Wideband Fast-Settling OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING: 230nsec typ to 0.01%
- WIDE BANDWIDTH: 200MHz Gain-Bandwidth Product
- FAST SLEWING: 300V/μsec slew rate, $A_{CL} \geq 50$
- LARGE OUTPUT CURRENT: ±20mA min at ±10V
- LOW VOLTAGE OFFSET AND DRIFT: 500μV max, 5μV/°C max

APPLICATIONS

- PULSE AMPLIFIERS
- FAST D/A CONVERTERS
- LINE DRIVERS
- WAVEFORM GENERATORS
- HIGH SPEED TEST EQUIPMENT
- PHOTODIODE AMPLIFIERS

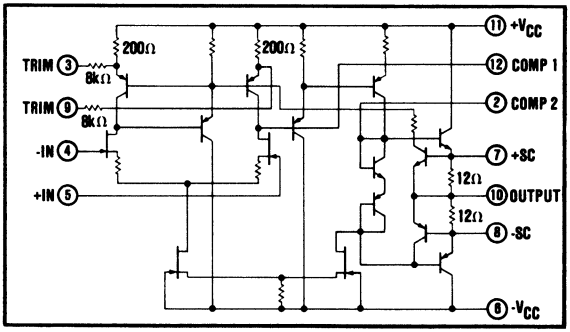
DESCRIPTION

The OPA605 is designed to offer a well balanced set of both AC and DC specifications. Versatility in fast settling, wideband and steady state AC applications is provided by the use of a single external compensation capacitor. This allows the user to optimize speed and stability for any particular application.

The full ±30mA guaranteed minimum output current (at ±10V) allows the user to realize the high speed features of the OPA605. Unlike most integrated circuit wideband amplifiers additional current booster circuitry is not needed for most applications.

The 500nsec max to 0.1% settling time specification is guaranteed with a load of 500Ω and 100pF. Also the open-loop gain is guaranteed at the full ±30mA output.

In addition to the excellent wideband and fast settling characteristics, the OPA605 also offers outstanding DC performance. Offset voltages are as low as 500μV max and offset voltage drift versus temperature of only 5μV/°C max is available.



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PDS-443B

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_{CC}$ = ±15VDC unless otherwise noted.

MODEL		OPA605HG/OPA605AM			OPA605KG/OPA605CM			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OPEN-LOOP GAIN, DC								
Full Load	V_O = ±10V, R_L = 330Ω	80	96		*	*		dB
No Load	V_O = ±10V, $R_L \geq$ 10kΩ		102			*		dB
RATED OUTPUT								
Voltage	I_O = ±30mA	±10	±12		*	*		V
Current	V_O = ±10V	±30	±50		*	*		mA
Output Resistance	Open Loop		200			*		Ω
Short Circuit Current	Internal Limits(1)	±30	±50	±80	*	*	*	mA
Capacitive Load(2)	A_{CL} = -1, C_C = 20pF	500			*			pF
DYNAMIC RESPONSE								
Gain-Bandwidth Product								
A_{CL} = 1000, C_C = 0			200			*		MHz
A_{CL} = -1, C_C = 20pF			20			*		MHz
Slew Rate	R_L = 330Ω, V_O = 0 to +10V,							
$A_{CL} \geq$ 50, C_C = 0	0 to -10V		300			*		V/µsec
A_{CL} = -1, C_C = 20pF		80	94		*	*		V/µsec
Full Power Bandwidth	R_L = 330Ω, V_O = ±10V,	1 3	1 5		*	*		MHz
	A_{CL} = -1, C_C = 20pF							
Settling Time, A_V = -1(3)	C_C = 20pF, R_L = 500Ω,							
	C_L = 100pF, V_O = 0 to +10V,							
	0 to -10V							
ε = 1%			200			*		nsec
ε = 0 1%			230	500		*	*	nsec
ε = 0 01%			350			*		nsec
Small-Signal Overshoot	A_V = -1, C_C = 20pF, R_L = 500Ω		0	20		*	*	%
	C_L = 100pF							
INPUT OFFSET VOLTAGE								
Initial Offset	T_A = +25°C		±0.25	±1 0		*	±0 5	mV
vs Temperature	T_L to T_H, V_{CM} = 0			±25			±5	µV/°C
vs Supply Voltage			±30	±200		*	*	µV/V
Adjustment Range(4)	Circuit in		±9			*		mV
	"Connection Diagram"							
INPUT BIAS CURRENT								
Initial Bias	T_A = +25°C, V_{CM} = 0		-5	-35		*	*	pA
vs Temperature	T_L to T_H		Note 5			*		
vs Supply Voltage			0 2			*		pA/V
vs V_{CM}			Note 6			*		
INPUT DIFFERRENCE CURRENT								
Initial Difference	T_A = +25°C, V_{CM} = 0		±2			*		pA
vs Temperature			Note 5			*		
vs Supply Voltage			0 05			*		pA/V
VOLTAGE NOISE DENSITY	$R_S \leq$ 100Ω							
	f_O = 10Hz		22			*		nV/√Hz
	f_O = 100Hz		11			*		nV/√Hz
	f_O = 1kHz		8			*		nV/√Hz
	f_O = 10kHz		6			*		nV/√Hz
	f_O = 100kHz		6			*		nV√Hz
INPUT IMPEDANCE								
Differential								
Resistance			10^{11}			*		Ω
Capacitance			3			*		pF
Common-Mode								
Resistance			10^{11}			*		Ω
Capacitance			3			*		pF
INPUT VOLTAGE RANGE								
Common-Mode Voltage	Linear Operation							
Range		±10	±12		*	*		V
Common-Mode Rejection		70	90		80	*		dB
POWER SUPPLY								
Rated Voltage			±15			*		VDC
Voltage Range	Derated Performance	±5		±18	*		*	VDC
Current, Quiescent			±7 2	±9		*	*	mA
TEMPERATURE RANGE								
Specification								
HG, KG Grades	T_L to T_H	0		+70	*		*	°C
AM, CM Grades	T_L to T_H	-25		+85	*		*	°C
Operating	Derated Performance	-55		+125	*		*	°C
Storage		-65		+150	*		*	°C

NOTES: *Specifications same as for OPA605HG/AM (1) Current limit may be increased with external resistors. (2) Allowable capacitive load depends on several factors. See Compensation section. (3) Settling Time measured in circuit of Figure 4. (4) Adjustment affects voltage drift vs temperature by approximately ±0.3µV/°C for each 100µV of offset adjusted. (5) Doubles approximately every 8.5°C. (6) See Typical Performance Curves.

ABSOLUTE MAXIMUM RATINGS

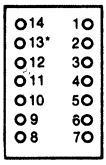
Supply	±20V
Internal Power Dissipation	(1)
Differential Input Voltage[2]	±20VDC
Input Voltage, Either Input[2]	±20VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-Circuit Duration[3]	Continuous
Junction Temperature	+175°C

NOTES: (1) Package must be derated according to details in the Application Information section. (2) For supply voltages less than ±20VDC, the absolute maximum input is equal to the supply voltage. (3) Short circuit to ground only See Short Circuit Protection discussion in the Application Information section.

PIN CONFIGURATION

1 No Internal Connection
2 Optional Frequency Compensation
3 Offset Adjust
4 Inverting Input
5 Noninverting Input
6 -Vcc
7 Optional Short Circuit Adjust
8 Optional Short Circuit Adjust
9 Offset Adjust
10 Output
11 +Vcc
12 Frequency Compensation
13 No Internal Connection *
14 No Internal Connection

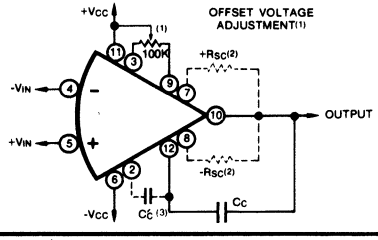
* Case on metal package



Bottom View

Pin numbers shown for reference only
Numbers are not marked on package
Pin 13 is case on metal unit

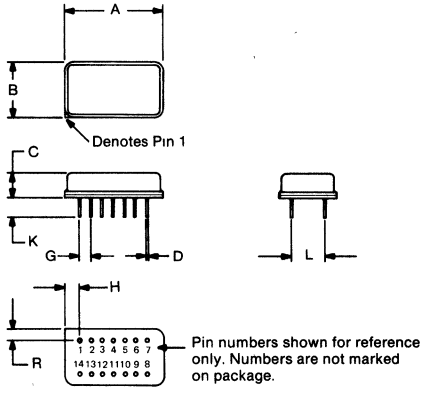
CONNECTION DIAGRAM



NOTES. (1) Offset voltage adjustment affects voltage drift versus temperature by approximately ±0.3μV/°C for each 100μV of offset adjusted (2) Optional resistors to increase current limits See Application Information (3) Optional frequency compensation See Application Information

MECHANICAL

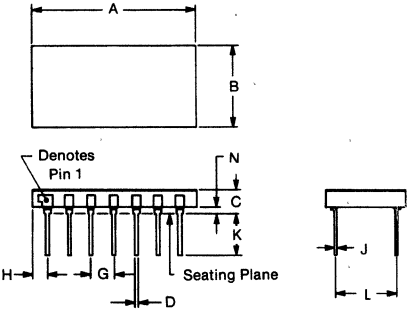
METAL PACKAGE—"M"



NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

CERAMIC PACKAGE—"G"



NOTES.
(1) Leads in true position within 0.010" (0.25mm) R at MMC at seating plane

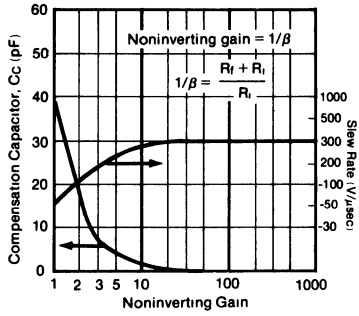
(2) Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.770	.810	19.56	20.57
B	.480	.500	12.19	12.70
C	.155	.215	3.94	5.46
D	.016	.020	0.41	0.51
G	.100 BASIC		2.54 BASIC	
H	.080	.110	2.03	2.79
J	.009	.012	0.23	0.30
K	.150	.210	3.81	5.33
L	.300 BASIC		7.62 BASIC	
N	.015	.035	0.38	0.89

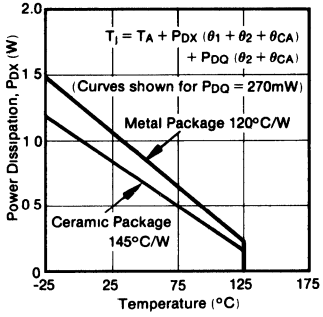
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

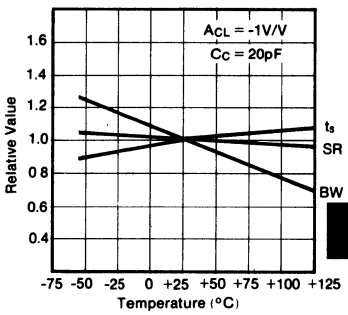
COMPENSATION CAPACITANCE AND SLEW RATE VS NONINVERTING GAIN



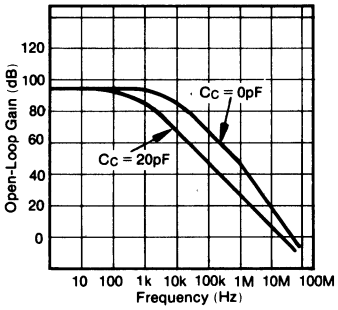
POWER DERATING



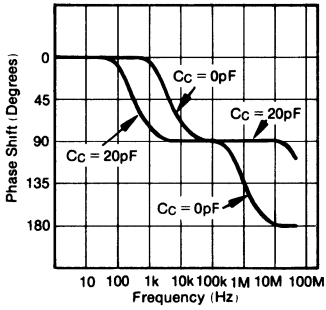
AC PARAMETERS VS TEMPERATURE



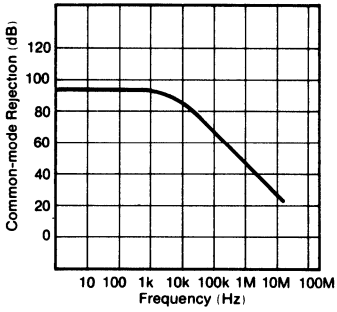
OPEN-LOOP GAIN VS FREQUENCY



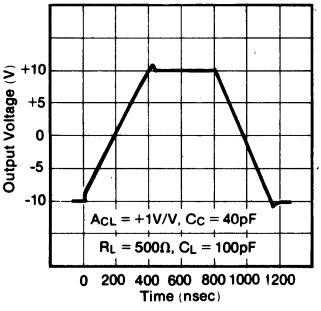
OPEN-LOOP PHASE SHIFT VS FREQUENCY



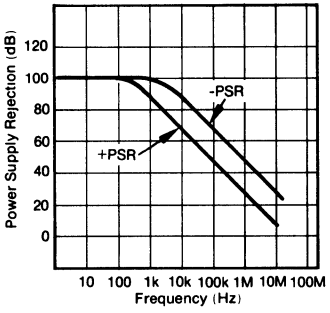
COMMON-MODE REJECTION VS FREQUENCY



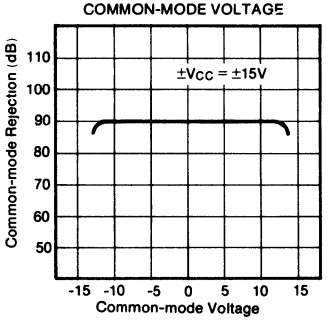
LARGE SIGNAL TRANSIENT RESPONSE



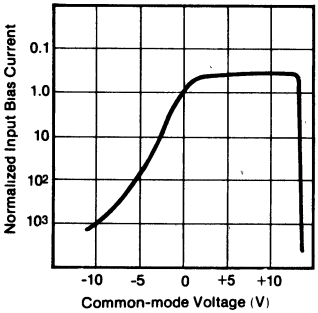
POWER SUPPLY REJECTION VS FREQUENCY



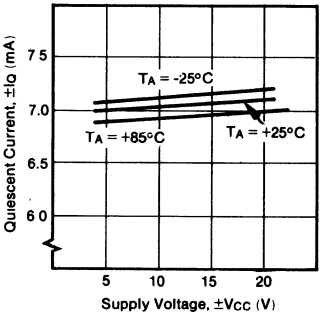
COMMON-MODE REJECTION VS COMMON-MODE VOLTAGE



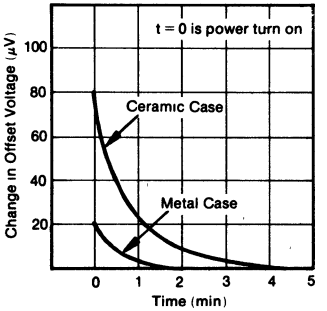
BIAS CURRENT VS COMMON-MODE VOLTAGE



QUIESCENT CURRENT VS SUPPLY VOLTAGE



OFFSET VOLTAGE VS TIME



APPLICATION INFORMATION

SLEW RATE

Slew rate is a large signal output parameter. It is primarily dependent on the compensation capacitor value (C_C) and has almost no dependence on changes in the closed loop gain or bandwidth. Typical values of slew rate versus compensation capacitor value are shown in the Typical Performance Curves. Decreasing the compensation capacitance increases the slew rate but reduces the frequency stability of the closed-loop circuit. Stray circuit capacitances may appear as added compensation to the amplifier. Therefore, stray capacitances should be minimized to avoid limiting slew rate performance.

BANDWIDTH

The closed-loop bandwidth is a small signal parameter. It is dependent on the open-loop frequency response of the op amp (which is determined by the value of the compensation capacitor, C_C) and the external closed-loop circuitry applied to the amplifier. Requirements for increased bandwidth and more frequency stability result in opposing constraints on the circuitry and generally the final selection of circuit values represents a compromise between the two needs.

SETTLING TIME

Settling time is defined as the total time required, measured from the input signal step, for the output to settle to within the specified error band around the final value. The error band is expressed as a percent of the full scale output voltage (10V) and the output transition is from 0V to +10V or 0V to -10V.

Settling time depends on slew rate (discussed above) and the time to reach the final value after the slew portion of the transition is complete. The latter is a function of the closed-loop bandwidth (discussed above) and the closed-loop gain. Thus, settling time is a function of both the open-loop frequency compensation (value of C_C) and the particular closed-loop circuit configuration. The best settling time is generally obtained at low gains.

COMPENSATION

The OPA605 uses external frequency compensation which allows the user to optimize slew rate, bandwidth and settling time for a particular application. As mentioned previously, compensation is normally a compromise between the desired speed and the necessary frequency stability - the higher the speed the lower the value of C_C and the less stable the circuit. Several of the Typical Performance Curves provide information to aid in the selection of the correct value of compensation capacitor. In addition, several typical circuits show recommended compensation in different applications.

The value of compensation capacitor required for stability is a function of the amount of negative feedback used in the particular application. This is characterized as $1/\beta$, where β is the "feedback factor". $1/\beta$ is also equal to the gain in noninverting configurations (see figures 2 and 3).

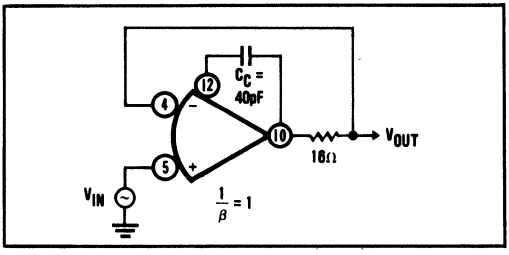


FIGURE 1. Unity Gain Follower.

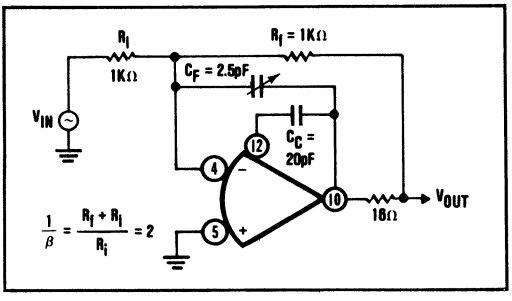


FIGURE 2. Unity Gain Inverting.

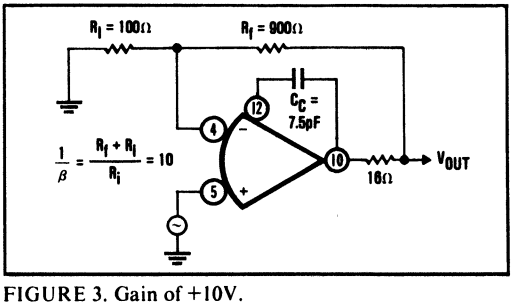


FIGURE 3. Gain of +10V.

The OPA605 may be compensated in either one of two ways. In the primary compensation method, C_C is connected between pins 10 and 12. Alternately the amplifier may be compensated with C_C' between pins 12 and 2 (see Connection Diagram). Normally the use of C_C is recommended. The use of C_C' will give lower output impedance at higher frequencies. This can be an advantage in some applications, but the effects are subtle and must be determined empirically.

Improved stability with larger capacitive loads may be obtained by connecting a small resistor (a value of 16Ω is recommended) in series with the output (see figures 2 through 4).

Flat high frequency closed-loop frequency response may be preserved and any high frequency peaking reduced by connecting a small capacitor (C_f in the examples) in parallel with the feedback resistor. This capacitor will compensate for the high frequency closed-loop transfer function zero formed by the capacitance at the amplifier's input and the input and feedback resistors. C_f may be a trimmer capacitor, a fixed capacitor or a planned printed circuit board capacitance. Typical values range from 0pF to 5pF.

WIRING PRECAUTIONS

Of all the wiring precautions, grounding is the most important. A good ground plane and good grounding practices should be used. The ground plane should connect all areas of the pattern side of the printed circuit board that are not otherwise used. The ground plane provides a low resistance, low inductance common return path for all signal and power returns.

If point-to-point wiring is used (no ground plane), single point grounding should be used. The input signal return, the load signal return and the power supply common should all be connected at the same physical point. This will eliminate any common current paths or ground loops which could cause signal modulation or unwanted feedback.

Each power supply lead should be bypassed to ground as near as possible to the amplifier pins.

All printed circuit board conductors should be wide to provide low resistance, low inductance connections, and should be as short as possible. In general, the entire physical circuit should be as small as practical. Stray capacitance should be minimized especially at high impedance nodes. Pin 4, the inverting input is especially sensitive to capacitance and all connections to that point must be short.

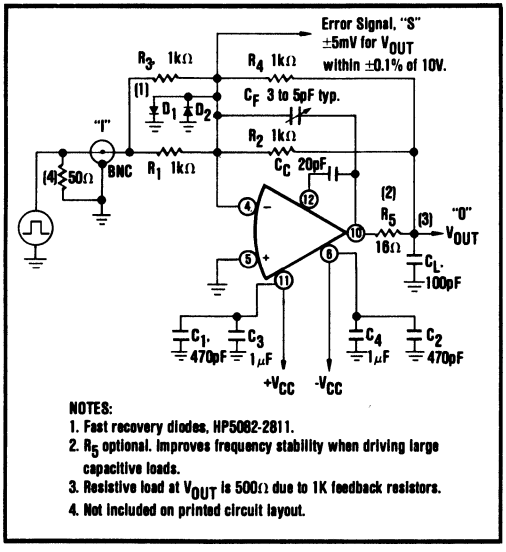


FIGURE 4. Dynamic Test Circuit.

Input and feedback resistors should be kept as small in value as practical; values less than 5.6kΩ are recommended. This will minimize performance limitations caused by the time constants formed by these resistors and circuit capacitances.

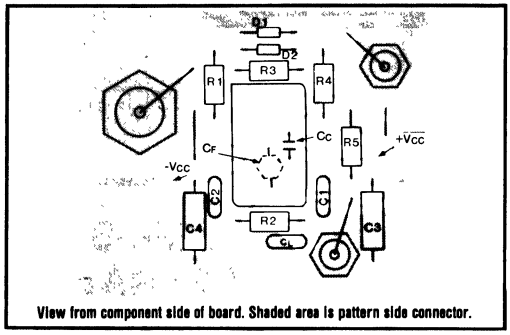


FIGURE 5. Dynamic Test Circuit Layout.

SHORT CIRCUIT PROTECTION

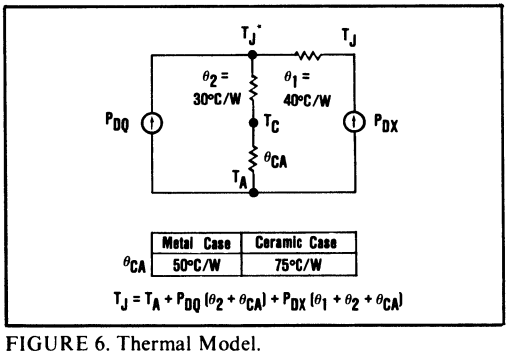
Short circuit protection to common is provided by internal current limiting resistors. (Output shorts to either supply can destroy the device.) The current limits may be increased by paralleling the internal resistors with external resistors, R_{EXT} connected between pins 7 and 10 and pins 8 and 10. The short-circuit current is then $I_{SC} \approx 0.05 + 0.6/R_{EXT}$ (in amps). The power derating constraints must be observed when modifying the current limits. Details are given by the thermal model.

THERMAL MODEL

Figure 6 is the thermal model for the OPA605 where:

T_J = Junction temperature (output load)
T_J* = Junction temperature (no load)
T_C = Case temperature
T_A = Ambient temperature
θ_{CA} = Thermal resistance, case-to-ambient
P_{DQ} = Quiescent power dissipation
$|+V_{CC}|\ I_{+QUIESCENT} + |-V_{CC}|\ I_{-QUIESCENT}$
P_{DX} = Power dissipation in the output transistor
$= (V_{OUT} - V_{CC})\ I_{OUT}$

(In a complementary output stage only one output transistor is conducting current at a time.)



	Metal Case	Ceramic Case
θ_{CA}	50°C/W	75°C/W

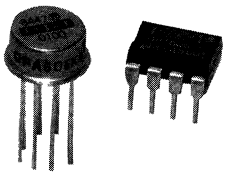
$$T_J = T_A + P_{DQ}(\theta_2 + \theta_{CA}) + P_{DX}(\theta_1 + \theta_2 + \theta_{CA})$$

FIGURE 6. Thermal Model.

This model yields a Power Derating curve which is a function of P_{DQ}. See Typical Performance Curves.

BURR-BROWN®

OPA606



AVAILABLE IN DIE FORM

Wide-Bandwidth *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH, 13MHz typ
- HIGH SLEW RATE, 35V/μsec typ
- LOW BIAS CURRENT, 10pA max at $T_A = +25°C$
- LOW OFFSET VOLTAGE, 500μV max
- LOW DISTORTION, 0.0035% typ at 10kHz

APPLICATIONS

- OPTOELECTRONICS
- DATA ACQUISITION
- TEST EQUIPMENT
- AUDIO AMPLIFIERS

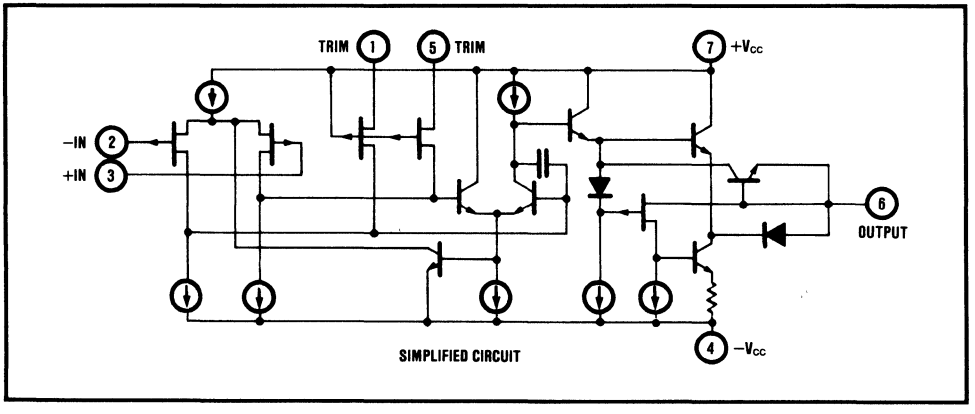
DESCRIPTION

The OPA606 is a wide-bandwidth monolithic dielectrically-isolated FET (*Difet*®) operational amplifier featuring a wider bandwidth and lower bias current than BIFET® LF156A amplifiers. Bias current is specified under warmed-up and operating conditions, not at a JUNCTION temperature of +25°C.

Laser-trimmed thin-film resistors offer improved offset voltage and noise performance.

The OPA606 is internally compensated for unity-gain stability.

Difet® Burr-Brown Corp , Bifet® National Semiconductor Corp.



SIMPLIFIED CIRCUIT

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx. 910-952-1111 - Cable. BBRCORP - Telex: 66-6491

PDS-598A

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = + 25°C unless otherwise specified

PARAMETER	CONDITIONS	OPA606KM/SM MIN	OPA606KM/SM TYP	OPA606KM/SM MAX	OPA606LM MIN	OPA606LM TYP	OPA606LM MAX	OPA606KP MIN	OPA606KP TYP	OPA606KP MAX	UNITS
FREQUENCY RESPONSE											
Gain Bandwidth	Small signal	10	12 5		11	13		9	12		MHz
Full Power Response	20V p-p, R_L = 2kΩ		515			550			470		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	22	33		25	35		20	30		V/µsec
Settling Time[1]: 0 1%	Gain = −1, R_L = 2kΩ		1 0			1 0			1 0		µsec
0.01%	10V step		2 1			2 1			2 1		µsec
Total Harmonic Distortion	G = +1, 20V p-p R_L = 2kΩ, f = 10kHz		0 0035			0 0035			0 0035		%
INPUT											
OFFSET VOLTAGE[2]											
Input Offset Voltage	V_{CM} = 0VDC		±180	±1.5mV		±100	±500		±300	±3mV	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±5			±3	±5		±10		µV/°C
Supply Rejection	V_{CC} = ±10V to ±18V	82	100		90	104		80	90		dB
			±10	±79		±6	±32		±32	±100	µV/V
BIAS CURRENT[2]											
Input Bias Current	V_{CM} = 0VDC		±7	±15		±5	±10		±8	±25	pA
OFFSET CURRENT[2]											
Input Offset Current	V_{CM} = 0VDC		±0 6	±10		±0 4	±5		±1	±15	pA
NOISE											
Voltage, f_O = 10Hz	100% tested (L)		37			30	40		37		nV/√Hz
100Hz	100% tested (L)		21			20	28		21		nV/√Hz
1kHz	100% tested (L)		14			13	16		14		nV/√Hz
10kHz	[3]		12			11	13		12		nV/√Hz
20kHz	[3]		11			10 5	13		11		nV/√Hz
f_B = 10Hz to 10kHz	[3]		1 3			1 2	1 5		1 3		µV rms
Current, f_O = 0 1Hz thru 20kHz	[3]		1 5			1 3	2		1 7		fA/√Hz
IMPEDANCE											
Differential			10^{13} ‖ 1			10^{13} ‖ 1			10^{13} ‖ 1		Ω ‖ pF
Common-Mode			10^{14} ‖ 3			10^{14} ‖ 3			10^{14} ‖ 3		Ω ‖ pF
VOLTAGE RANGE											
Common-Mode Input Range		±10 5	±11 5		±11	±11.6		±10 2	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	80	95		85	96		78	90		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq$ 2kΩ	95	115		100	118		90	110		dB
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11	±12 2		±12	±12 6		±11	±12		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		mA
Output Resistance	DC, open loop		40			40			40		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000		pF
Short Circuit Current		10	20		10	20		10	20		mA
POWER SUPPLY											
Rated Voltage			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		6 5	9 5		6 2	9		6 5	10	mA
TEMPERATURE RANGE											
Specification	Ambient temp										
	KM, KP, LM	0		+70	0		+70	0		+70	°C
	SM	−55		+125							°C
Operating	Ambient Temp	−55		+125	−55		+125	−25		+85	°C
θ Junction-Ambient			200			200			155		°C/W

NOTES (1) See settling time test circuit in Figure 2 (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up (3) Sample tested—this parameter is guaranteed on L grade only

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±15VDC and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA606KM/SM			OPA606LM			OPA606KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification Range	Ambient temp KM	0		+70	0		+70	0		+70	°C
	SM	−55		+125							°C
INPUT											
OFFSET VOLTAGE[1]											
Input Offset Voltage	V_{CM} = 0VDC KM		±400	±2mV		±335	±750		±750	±3 5mV	µV
	SM		±680	±3mV							µV
Average Drift			±5			±3	±5		±10		µV/°C
Supply Rejection	V_{CC} = ±10V to ±18V	80	98		85	100		78	95		dB
			±13	±100		±10	±56		±18	±126	µV/V
BIAS CURRENT[1]											
Input Bias Current	V_{CM} = 0VDC KM		±158	±339		±113	±226		±181	±566	pA
	SM		±7 2	±15 4							nA
OFFSET CURRENT[1]											
Input Offset Current	V_{CM} = 0VDC KM		±14	±226		±9	±113		±23	±339	pA
	SM		±614	±10.2nA							pA
VOLTAGE RANGE											
Common-Mode Input Range		±10 4	±11 4		±10 9	±11.5		±10	±10 9		V
Common-Mode Rejection	V_{IN} = ±10VDC	78	92		82	95		75	88		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	90	106		95	112		88	104		dB
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±10 5	±12		±11 5	±12.4		±10 4	±11 8		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		mA
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		6 6	10		6 4	9 5		6.6	10 5	mA

NOTES (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up

ORDERING INFORMATION

OPA606 X X

Basic model number

Performance grade
- K, L = 0°C to +70°C
- S = −55°C to +125°C

Package code
- M = TO-99 metal can
- P = 8-pin plastic DIP (K grade only)

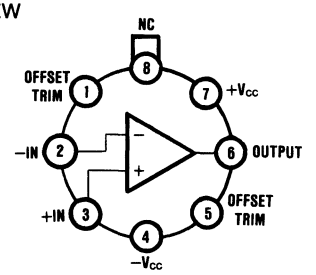
ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage	±36VDC
Input Voltage Range[2]	±18VDC
Storage Temperature Range	M = −65°C to +150°C, P = −40°C to +85°C
Operating Temperature Range	M = −55°C to +125°C, P = −40°C to +85°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[3]	Continuous
Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on θ_{JC} = 15°C/W or θ_{JA}. (2) For supply voltages less than ±18VDC, the absolute maximum input voltage is equal to the negative supply voltage. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

CONNECTION DIAGRAMS

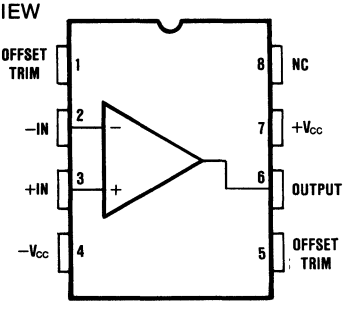
TOP VIEW — TO-99



CASE IS CONNECTED TO V_{CC}

MECHANICAL

TOP VIEW — DIP



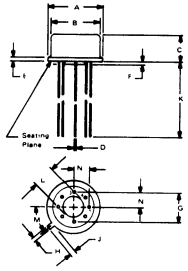
MECHANICAL

"M" PACKAGE — TO-99 (Hermetic)

NOTE Leads in true position within 0 01" (0 25mm) R at MMC at seating plane

Pin numbers shown for reference only. Numbers may not be marked on package

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3 2)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	335	370	8 51	9 40
B	305	335	7 75	8 51
C	165	185	4 19	4 70
D	016	021	0 41	0 53
E	010	040	0 25	1 02
F	010	040	0 25	1 02
G	200 BASIC		5 08 BASIC	
H	028	034	0 71	0 86
J	029	045	0 74	1 14
K	500		12 7	
L	110	160	2 79	4 06
M	45° BASIC		45° BASIC	
N	05	105	2 41	2 67

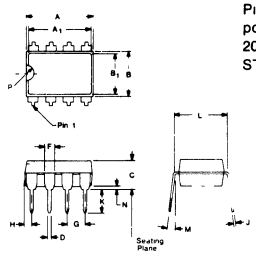
MECHANICAL

"P" PACKAGE — Plastic DIP

NOTE Leads in true position within 0 01" (0.25mm) R at MMC at seating plane

Pin numbers shown for reference only. Numbers may not be marked on package

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3 2)

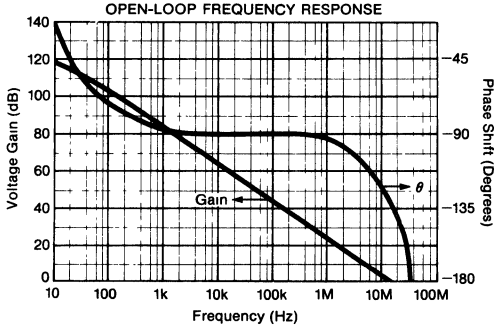


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	355	400	9 03	10 16
A_1	340	385	8 65	9 80
B	230	290	5 85	7 36
B_1	200	260	5 09	6 36
C	120	200	3 05	5 08
D	015	023	0 38	0 59
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	025	050	0 64	1 27
J	008	015	0 20	0 38
K	070	150	1 78	3 82
L	300 BASIC		7 63 BASIC	
M	0°	15°	0°	15°
N	010	030	0 25	0 76
P	025	050	0 64	1 27

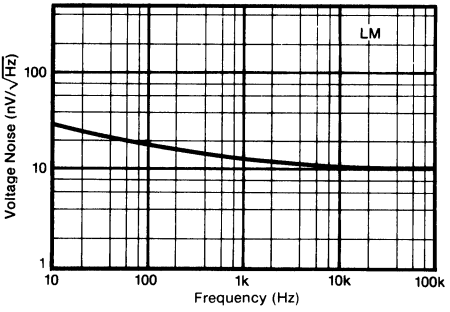
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

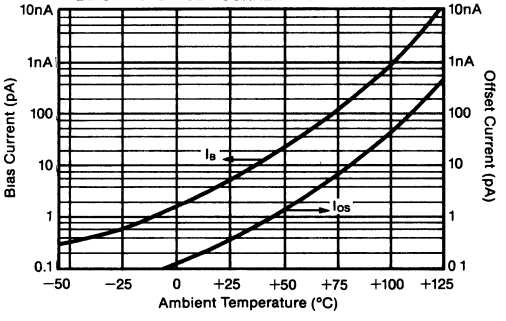
OPEN-LOOP FREQUENCY RESPONSE



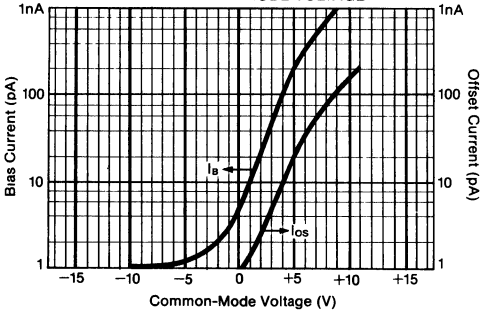
INPUT VOLTAGE NOISE SPECTRAL DENSITY



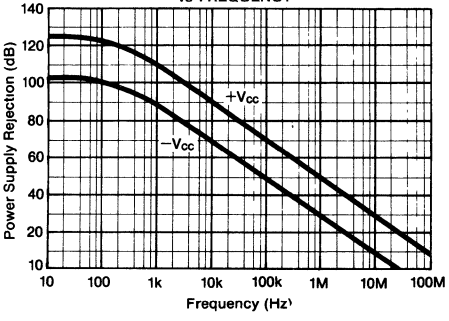
BIAS AND OFFSET CURRENT vs TEMPERATURE



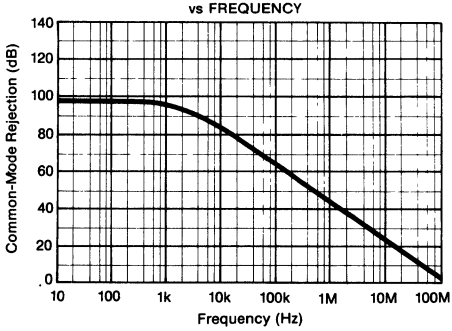
BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



POWER SUPPLY REJECTION vs FREQUENCY



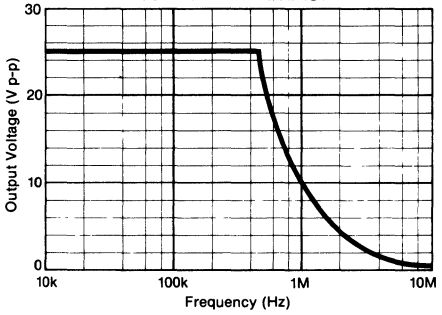
COMMON-MODE REJECTION vs FREQUENCY



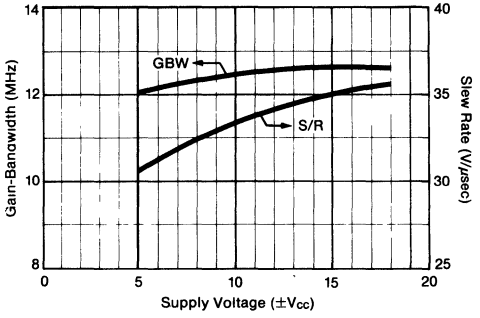
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

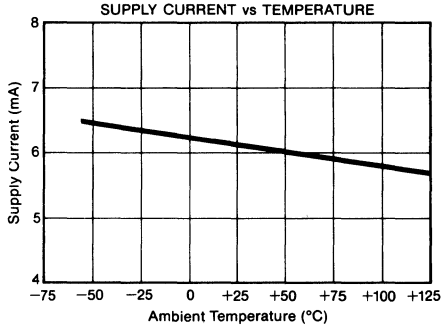
MAXIMUM UNDISTORTED OUTPUT VOLTAGE vs FREQUENCY



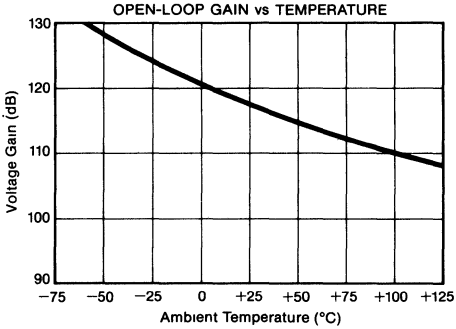
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



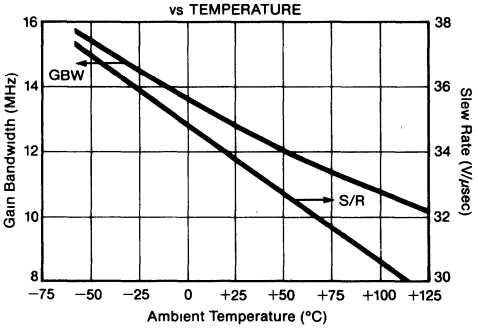
SUPPLY CURRENT vs TEMPERATURE



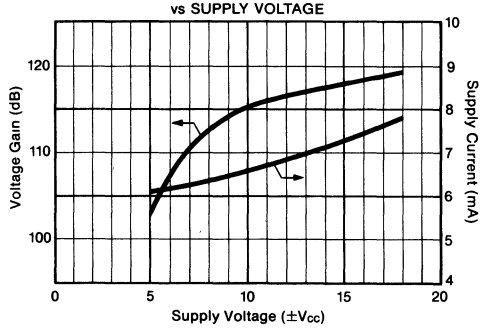
OPEN-LOOP GAIN vs TEMPERATURE



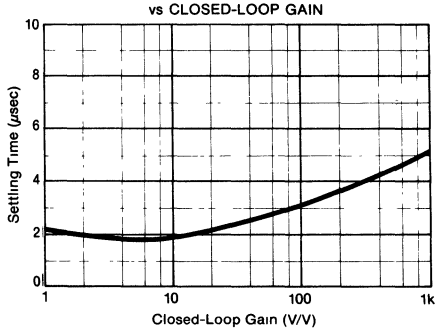
GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



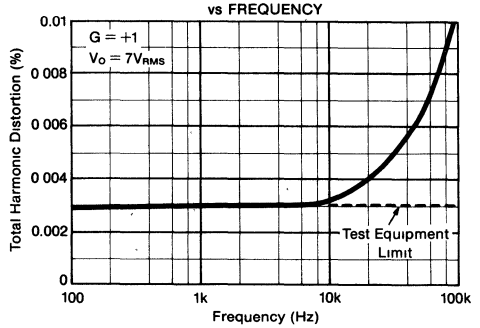
OPEN-LOOP GAIN AND SUPPLY CURRENT vs SUPPLY VOLTAGE



SETTLING TIME vs CLOSED-LOOP GAIN



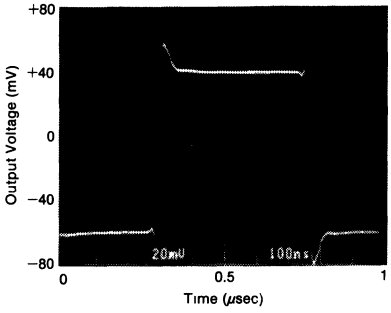
TOTAL HARMONIC DISTORTION vs FREQUENCY



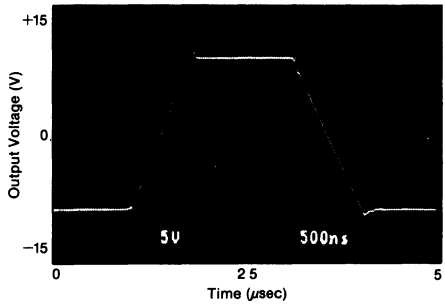
TYPICAL PERFORMANCE CURVES (CONT)

T_a = +25°C, V_{CC} = ±15VDC unless otherwise noted

SMALL SIGNAL TRANSIENT RESPONSE



LARGE SIGNAL TRANSIENT RESPONSE



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA606 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.5μV/°C for each millivolt of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as LF156 and OP-16. The OPA606 can replace most other amplifiers by leaving the external null circuit unconnected.

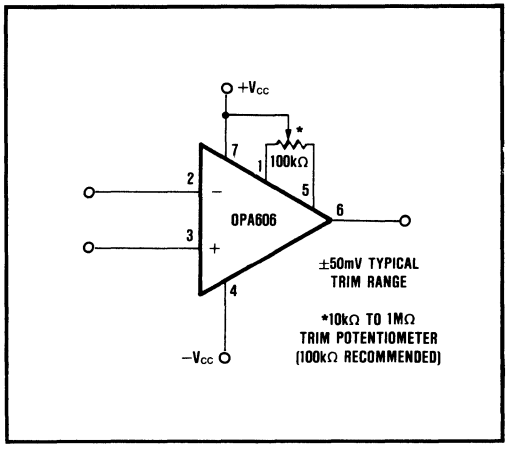


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift. Static protection is recommended when handling any precision IC operational amplifier.

If the input voltage exceeds the amplifier's negative supply voltage, input current limiting must be used to prevent damage.

CIRCUIT LAYOUT

Wideband amplifiers require good circuit layout techniques and adequate power supply bypassing. Short, direct connections and good high frequency bypass capacitors (ceramic or tantalum) will help avoid noise pickup or oscillation.

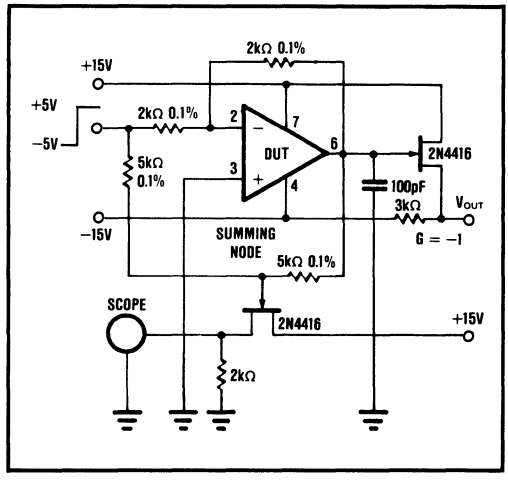


FIGURE 2. Settling Time Test Circuit.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA606. To avoid leakage problems, it is recommended that the signal input lead of the OPA606 be wired to a Teflon® standoff. If the OPA606 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout.

A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 3).

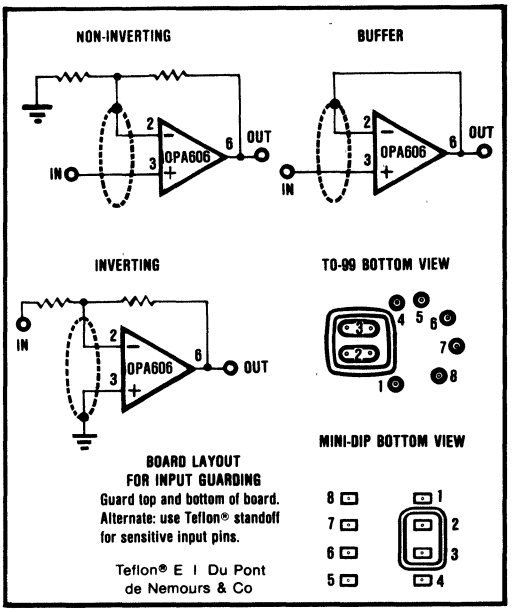


FIGURE 3. Connection of Input Guard.

APPLICATIONS CIRCUITS

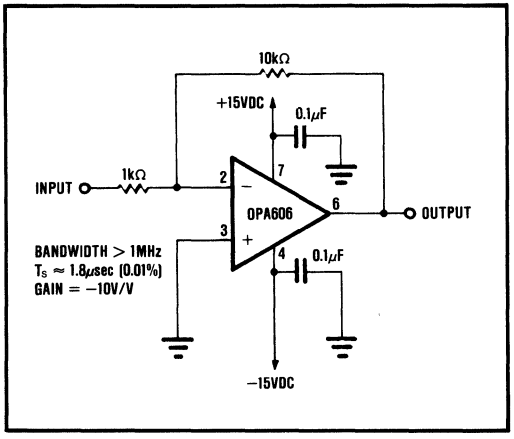


FIGURE 4. Inverting Amplifier.

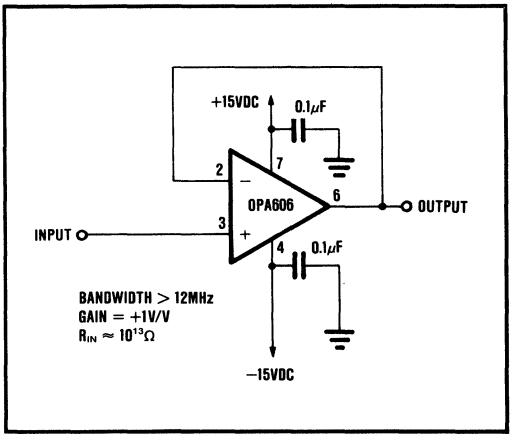


FIGURE 5. Noninverting Buffer.

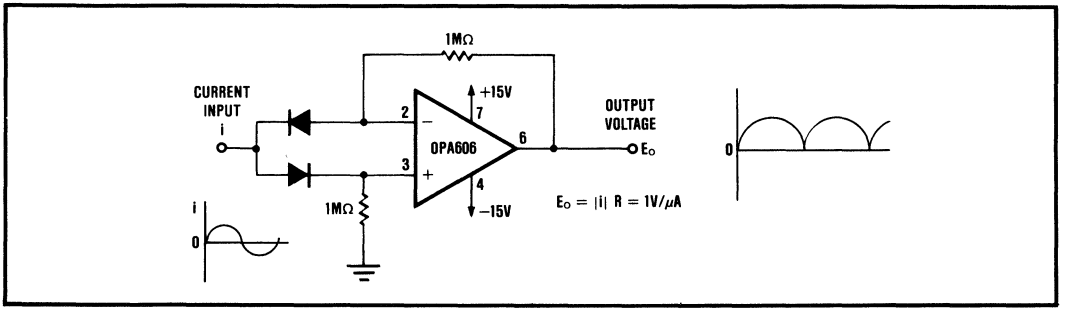


FIGURE 6. Absolute Value Current-to-Voltage Converter.

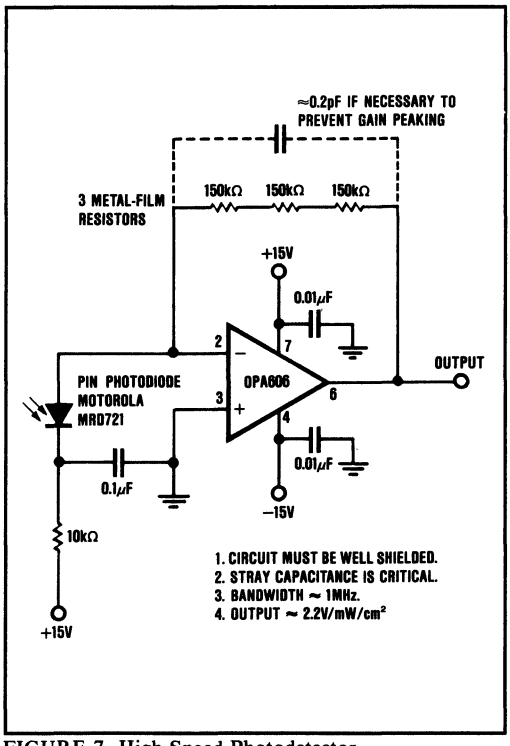


FIGURE 7. High-Speed Photodetector.

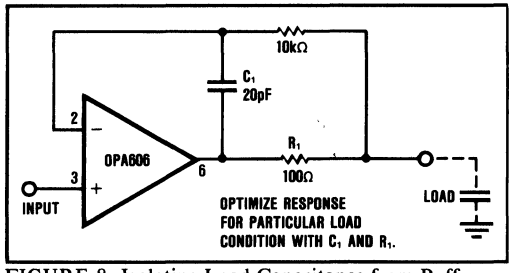


FIGURE 8. Isolating Load Capacitance from Buffer.

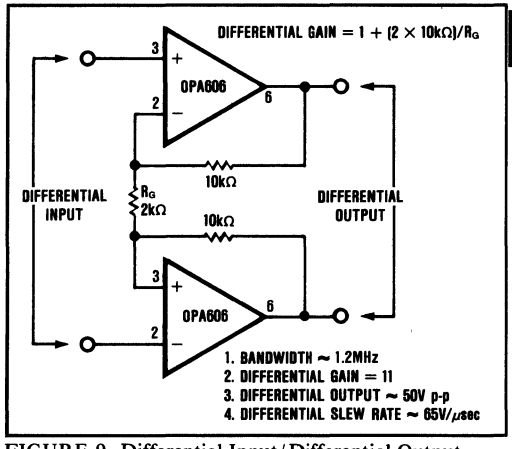


FIGURE 9. Differential Input/Differential Output Amplifier.

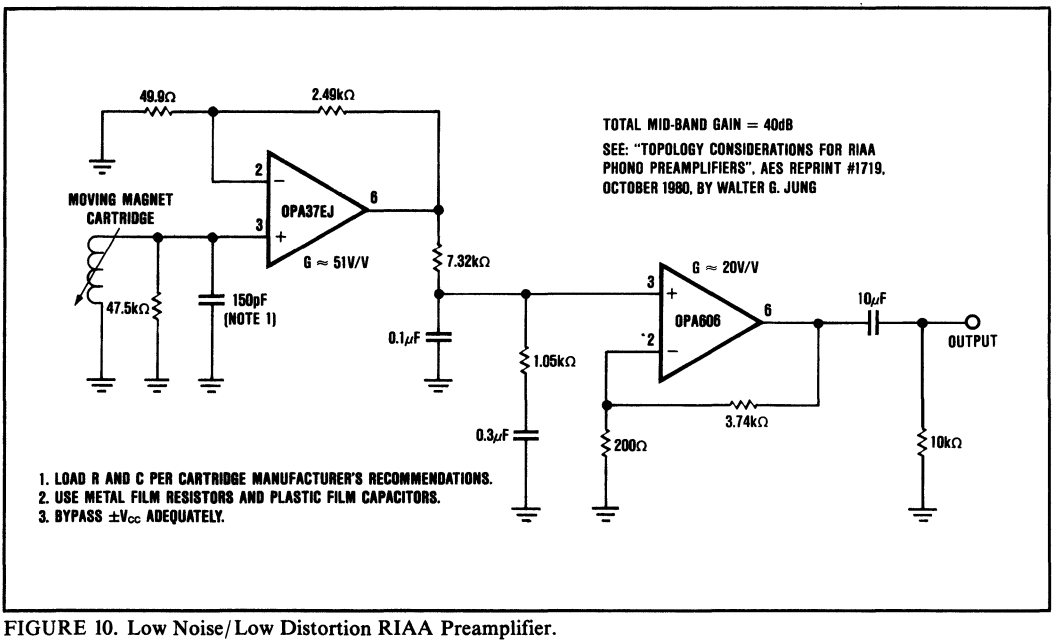
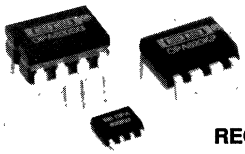


FIGURE 10. Low Noise/Low Distortion RIAA Preamplifier.

BURR-BROWN®



OPA620

ABRIDGED DATA SHEET
REQUEST COMPLETE DATA SHEET
FROM BURR-BROWN SALES OFFICE

Wideband Precision OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING: 13ns (0.1%)
  25ns (0.01%)
- GAIN-BANDWIDTH: 200MHz
- UNITY-GAIN STABLE
- LOW OFFSET VOLTAGE: ±100µV
- SLEW RATE: 250V/µs
- LOW DIFFERENTIAL GAIN/PHASE ERROR
- 8-PIN DIP AND SOIC PACKAGES

APPLICATIONS

- HIGH-SPEED SIGNAL PROCESSING
- ADC/DAC BUFFER
- ULTRASOUND
- PULSE/RF AMPLIFIERS
- HIGH-RESOLUTION VIDEO
- ACTIVE FILTERS

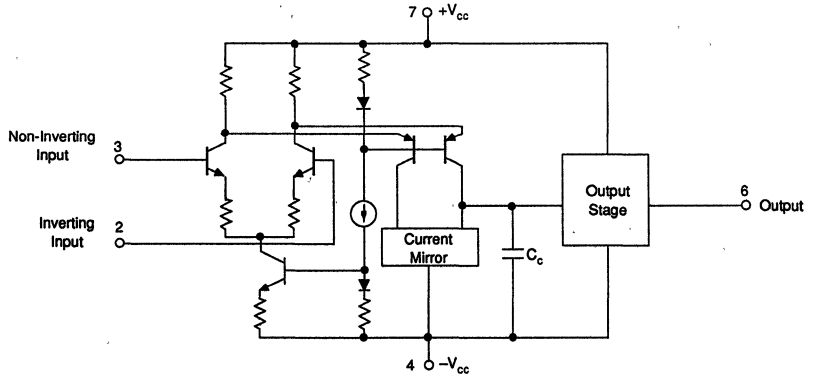
DESCRIPTION

The OPA620 is a precision wideband monolithic operational amplifier featuring very fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA620 is internally compensated for unity-gain stability. This amplifier has a very low offset, fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA620 may be used in all op amp applications requiring high speed and precision.

Low noise and distortion, wide bandwidth, and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

The OPA620 is available in plastic, ceramic, and SOIC packages. Two temperature ranges are offered: 0°C to +70°C and –55°C to +125°C.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491 • FAX: (602) 889-1510

PDS-872

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA620KP/KU MIN	OPA620KP/KU TYP	OPA620KP/KU MAX	OPA620KG/SG MIN	OPA620KG/SG TYP	OPA620KG/SG MAX	OPA620LG MIN	OPA620LG TYP	OPA620LG MAX	UNITS
INPUT NOISE											
Voltage: f_O = 100Hz	R_S = 0Ω		10			*			*		nV/√Hz
f_O = 1kHz			5.5			*			*		nV/√Hz
f_O = 10kHz			3.3			*			*		nV/√Hz
f_O = 100kHz			2.5			*			*		nV/√Hz
f_O = 1MHz to 100MHz			2.3			*			*		nV/√Hz
f_B = 100Hz to 10MHz			8.0			*			*		µV, rms
Current: f_O = 10kHz to 100MHz			2.3			*			*		pA/√Hz
OFFSET VOLTAGE[1]											
Input Offset Voltage	V_{CM} = 0VDC		±200	±1mV		*	*		±100	±500	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±8			*			*		µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	50	60		*	*		55	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		15	30		*	*		*	25	µA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.2	2		*	*		*	*	µA
INPUT IMPEDANCE											
Differential	Open-Loop		15 || 1			*			*		kΩ || pF
Common-Mode			1 || 1			*			*		MΩ || pF
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±3.0	±3.5		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±2.5VDC, V_O = 0VDC	65	75		*	*		70	*		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L = 100Ω	50	60		*	*		55	*		dB
	R_L = 50Ω	48	58		*	*		53	*		dB
FREQUENCY RESPONSE											
Closed-Loop Bandwidth	Gain = +1V/V		300			*			*		MHz
(–3dB)	Gain = +2V/V		100			*			*		MHz
	Gain = +5V/V		40			*			*		MHz
	Gain = +10V/V		20			*			*		MHz
Gain-Bandwidth	Gain = +10V/V		200			*			*		MHz
Differential Gain	3.58MHz, G = +1V/V		0.05			*			*		%
Differential Phase	3.58MHz, G = +1V/V		0.05			*			*		Degrees
Harmonic Distortion	G =+2V/V, R_L=50Ω, V_O=0.5Vp-p										
	f = 10MHz, Second Harmonic		–62			*			*		dBc[2]
	Third Harmonic		–67			*			*		dBc
Full Power Response	V_O = 5Vp-p, Gain = +1V/V		16			*			*		MHz
	V_O = 2Vp-p, Gain = +1V/V		40			*			*		MHz
Slew Rate	2V Step, Gain = –1V/V		250			*			*		V/µs
Overshoot	2V Step, Gain = –1V/V		15			*			*		%
Settling Time: 0.1%	2V Step, Gain = –1V/V		13			*			*		ns
0.01%			25			*			*		ns
Phase Margin	Gain = +1V/V		60			*			*		Degrees
Rise Time	Gain = +1V/V, 10% to 90%								*		
	V_O = 100mVp-p; Small Signal		2			*			*		ns
	V_O = 6Vp-p; Large Signal		22			*			*		ns
RATED OUTPUT											
Voltage Output	R_L = 100Ω	±3.0	±3.5		*	*		*	*		V
	R_L = 50Ω	±2.5	±3.0		*	*		*	*		V
Output Resistance	1MHz, Gain = +1V/V		0.015			*			*		Ω
Load Capacitance Stability	Gain = +1V/V		20			*			*		pF
Short Circuit Current	Continuous		±150			*			*		mA
POWER SUPPLY											
Rated Voltage	$\pm V_{CC}$		5			*			*		VDC
Derated Performance	$\pm V_{CC}$	4.0		6.0	*		*	*		*	VDC
Current, Quiescent	I_O = 0mADC		21	23		*	*		*	*	mA
TEMPERATURE RANGE											
Specification: KP, KU, KG, LG	Ambient Temperature	0		+70	*		*	*		*	°C
SG					–55		+125				°C
Operating: KG, LG, SG	Ambient Temperature				–55		+125	–55		+125	°C
KP, KU		–25		+85							°C
θ_{JA}											
KG, LG, SG						125			125		°C/W
KP			90								°C/W
KU			100								°C/W

* Same Specifications as for KP/KU.

SPECIFICATIONS (cont)

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

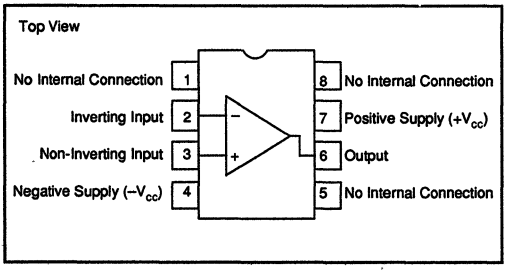
At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA620KP/KU			OPA620KG/SG			OPA620LG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification: KP, KU, KG, LG	Ambient Temperature	0		+70	*		*	*		*	°C
SG					–55		+125				°C
OFFSET VOLTAGE[1]											
Average Drift	T_A = T_{MIN} to T_{MAX}		±8			*			*		µV/°C
Supply Rejection	±V_{CC} = 4.5V to 5.5V	45	60		*	*		50	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		15	40		*	*		*	35	µA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.2	5		*	*		*	*	µA
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±2.5	±3.0		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±2.5VDC, V_O = 0VDC	60	75		*	*		65	*		dB
OPEN LOOP GAIN, DC											
Open-Loop Voltage Gain	RL = 100Ω	46	60		*	*		52	*		dB
	RL = 50Ω	44	58		*	*		50	*		dB
RATED OUTPUT											
Voltage Output	R_L = 100Ω	±3.0	±3.5		*	*		*	*		V
	R_L = 50Ω	±2.5	±3.0		*	*		*	*		V
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		21	25		*	*		*	*	mA

* Same specifications as for KP/KU.

NOTES: (1) Offset Voltage specifications are also guaranteed with units fully warmed up. (2) dBc = dB refered to carrier-input signal.

PIN CONFIGURATION (8-PIN DIP)



ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Internal Power Dissipation[3]	See Applications Information
Differential Input Voltage	Total V_{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range KG, LG, SG:	–65°C to +150°C
KP, KU:	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous to Ground
Junction Temperature (T_J)	+175°C

Notes: (3) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

ORDERING INFORMATION

OPA620 ( )( ) Q

Basic Model Number

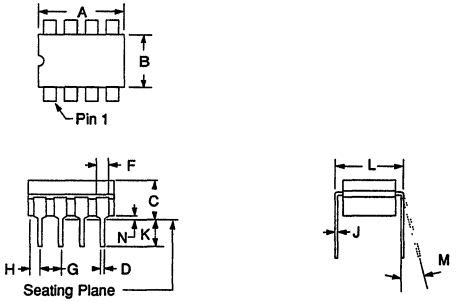
Performance Grade Code
- K, L = 0°C to +70°C
- S = –55°C to +125°C

Package Code
- G = 8-pin Ceramic DIP
- P = 8-pin Plastic DIP
- U = 8-pin Plastic SOIC

Reliability Screening
- Q = Q-Screened

MECHANICAL

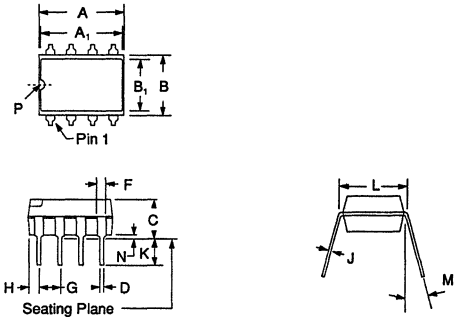
G Package— 8-Pin Ceramic DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.375	.405	9.53	10.28
B	.245	.251	6.22	6.38
C	.140	.170	3.56	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	—	.098	—	2.49
J	.008	.012	0.20	0.30
K	.150	—	3.80	—
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

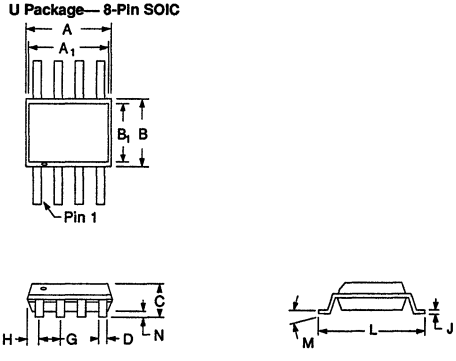
P Package— 8-Pin Plastic DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.355	.400	9.03	10.16
A1	.340	.385	8.65	9.80
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.025	.050	0.64	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

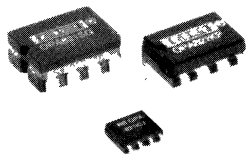
U Package— 8-Pin SOIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.201	4.70	5.11
A1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	.030

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

BURR-BROWN®



OPA621

ADVANCE INFORMATION
SUBJECT TO CHANGE

Wideband Precision OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING: 10ns (0.1%)
  20ns (0.01%)
- GAIN-BANDWIDTH: 600MHz
- EXTERNAL COMPENSATION
- LOW OFFSET VOLTAGE: ±100µV
- SLEW RATE: 1000V/µs
- LOW DIFFERENTIAL GAIN/PHASE ERROR
- 8-PIN DIP AND SOIC PACKAGES

APPLICATIONS

- HIGH-SPEED SIGNAL PROCESSING
- ADC/DAC BUFFER
- ULTRASOUND
- PULSE/RF AMPLIFIERS
- HIGH-RESOLUTION VIDEO
- ACTIVE FILTERS

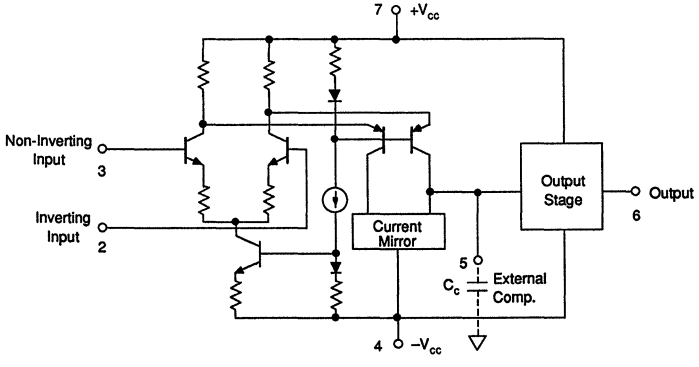
DESCRIPTION

The OPA621 is a precision wideband monolithic operational amplifier featuring very fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA621 is externally compensated. This amplifier has a very low offset, fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA621 may be used in all op-amp applications requiring high speed and precision.

Low distortion, wide bandwidth, and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal output current-limiting circuit.

The OPA621 is available in plastic, ceramic and SOIC packages. Two temperature ranges are offered: 0°C to +70°C and –55°C to +125°C.



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PDS-871

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 100Ω, C_C = 0pF, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA621KP/KU MIN	OPA621KP/KU TYP	OPA621KP/KU MAX	OPA621KG/SG MIN	OPA621KG/SG TYP	OPA621KG/SG MAX	OPA621LG MIN	OPA621LG TYP	OPA621LG MAX	UNITS
INPUT NOISE											
Voltage: f_O= 100 Hz	R_S = 0Ω		10			*			*		nV/√Hz
f_O= 1kHz			5.5			*			*		nV/√Hz
f_O= 10kHz			3.3			*			*		nV/√Hz
f_O= 100kHz			2.5			*			*		nV/√Hz
f_O= 1MHz to 100MHz			2.3			*			*		nV/√Hz
f_B= 100Hz to 10MHz			8.0			*			*		µV, rms
Current: f_O= 10kHz to 100MHz			2.3			*			*		pA/√Hz
OFFSET VOLTAGE[1]											
Input Offset Voltage	V_{CM} = 0VDC		±200	±1mV		*	*		±100	±500	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±8			*			*		µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	50	60		*	*		55	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		15	30		*	*		*	25	µA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.2	2		*	*		*	*	µA
INPUT IMPEDANCE											
Differential	Open-Loop		15||1			*			*		kΩ||pF
Common-Mode			1||1			*			*		MΩ||pF
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±3.0	±3.5		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±2.5VDC, V_O = 0VDC	65	75		*	*		70	*		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L = 100Ω	50	60		*	*		55	*		dB
	R_L = 50Ω	48	58		*	*		53	*		dB
FREQUENCY RESPONSE											
Closed-Loop Bandwidth[2]											
(–3dB)	Gain = +2V/V		300			*			*		MHz
	Gain = +5V/V		120			*			*		MHz
	Gain = +10V/V		60			*			*		MHz
Gain-Bandwidth	Gain = +10V/V		600			*			*		MHz
Differential Gain	3.58MHz, G = +2V/V		0.08			*			*		%
Differential Phase	3.58MHz, G = +2V/V		0.08			*			*		Degrees
Harmonic Distortion	G= +2V/V, R_L=50Ω, V_O=0.5Vp-p										
	f = 10MHz, Second Harmonic		–65			*			*		dBc[3]
	Third Harmonic		–70			*			*		dBc
Full Power Response	V_O = 5Vp-p, Gain = +2V/V		150			*			*		MHz
	V_O = 2Vp-p, Gain = +2V/V		60			*			*		MHz
Slew Rate	2V Step, Gain = –1V/V		1000			*			*		V/µs
Overshoot	2V Step, Gain = –1V/V		20			*			*		%
Settling Time: 0.1%	2V Step, Gain = –1V/V		10			*			*		ns
0.01%			20			*			*		ns
Phase Margin	Gain = +2V/V		50			*			*		Degrees
Rise Time	Gain = +2V/V, 10% to 90%								*		
	V_O = 100mVp-p; Small Signal		1			*			*		ns
	V_O = 6Vp-p; Large Signal		6			*			*		ns
RATED OUTPUT											
Voltage Output	R_L = 100Ω	±3.0	±3.5		*	*		*	*		V
	R_L = 50Ω	±2.5	±3.0		*	*		*	*		V
Output Resistance	1MHz, Open-Loop		0.2			*			*		Ω
Load Capacitance Stability	Gain = +2V/V		10			*			*		pF
Short Circuit Current	Continuous		±150			*			*		mA
POWER SUPPLY											
Rated Voltage	$\pm V_{CC}$		5			*			*		VDC
Derated Performance	$\pm V_{CC}$	4.0		6.0	*		*	*		*	VDC
Current, Quiescent	I_O = 0mADC		25	27		*	*		*	*	mA
TEMPERATURE RANGE											
Specification: KP, KU, KG, LG	Ambient Temperature	0		+70	*		*	*		*	°C
SG					–55		+125				°C
Operating: KG, LG, SG	Ambient Temperature				–55		+125	–55		+125	°C
KP, KU		–25		+85							°C
θ_{JA}											
KG, LG, SG					125			125			°C/W
KP			90								°C/W
KU			100								°C/W

SPECIFICATIONS (cont)

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

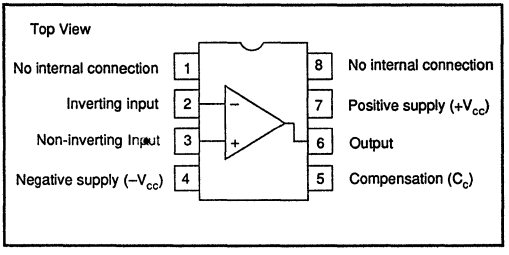
At V_{CC} = ±5VDC, R_L = 100Ω, C_C = 0pF, and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA621KP/KU			OPA621KG/SG			OPA621LG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification:KP, KU, KG, LG	Ambient Temperature	0		+70	*		*	*		*	°C
SG					–55		+125				°C
OFFSET VOLTAGE[1]											
Average Drift	T_A = T_{MIN} to T_{MAX}		±8			*			*		µV/°C
Supply Rejection	±V_{CC} = 4.5V to 5.5V	45	60		*	*		50	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		15	40		*	*		*	35	µA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.2	5		*	*		*	*	µA
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±2.5	±3.0		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±2.5VDC, V_O = 0VDC	60	75		*	*		65	*		dB
OPEN LOOP GAIN, DC											
Open-Loop Voltage Gain	RL = 100Ω	46	60		*	*		52	*		dB
	RL = 50Ω	44	58		*	*		50	*		dB
RATED OUTPUT											
Voltage Output	R_L = 100Ω	±3.0	±3.5		*	*		*	*		V
	R_L = 50Ω	±2.5	±3.0		*	*		*	*		V
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		25	30		*	*		*	*	mA

* Same specifications as for KP/KU

NOTES: (1) Offset Voltage specifications are also guaranteed with units fully warmed up. (2) G = +2V/V, (or G = –1V/V), is minimum stable closed-loop gain without external compensation. (3) dBc = dB refered to carrier-input signal.

PIN CONFIGURATION (8-PIN DIP)



ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Internal Power Dissipation[1]	1W
Differential Input Voltage	Total V_{CC}
Input Voltage Range	±V_{CC}
Storage Temperature Range KG, LG, SG:	–65°C to +150°C
KP, KU:	–40°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
(soldering, SOIC 3 seconds)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous to Ground
Junction Temperature (T_J)	+175°C

NOTES: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

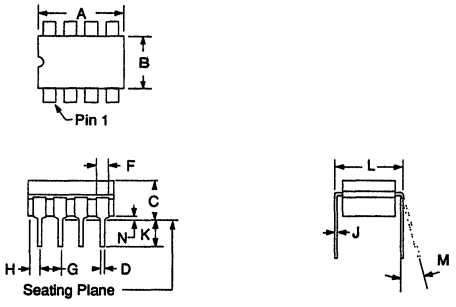
ORDERING INFORMATION

OPA621 ( ) ( ) Q

- Basic Model Number
- Performance Grade Code
  - K, L = 0°C to +70°C
  - S = –55°C to +125°C
- Package Code
  - G = 8-Pin Ceramic DIP
  - P = 8-Pin Plastic DIP
  - U = 8-Pin Plastic SOIC
- Reliability Screening
  - Q = Q-Screened

MECHANICAL

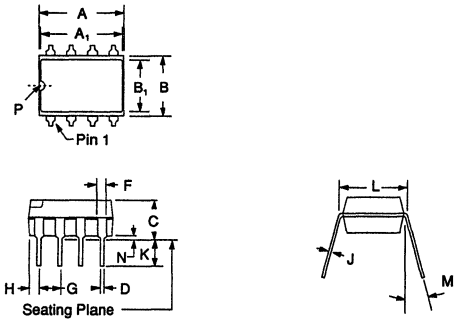
G Package— 8-Pin Ceramic DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.375	.405	9.53	10.28
B	.245	.251	6.22	6.38
C	.140	.170	3.56	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	—	.098	—	2.49
J	.008	.012	0.20	0.30
K	.150	—	3.80	—
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

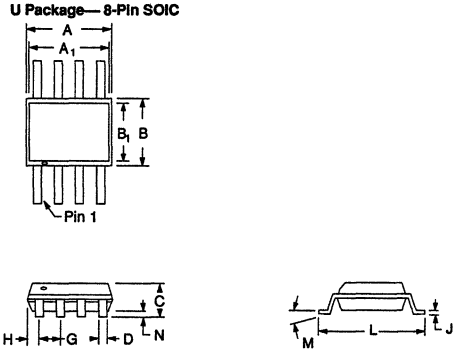
P Package— 8-Pin Plastic DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.355	.400	9.03	10.16
A1	.340	.385	8.65	9.80
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.025	.050	0.64	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

U Package— 8-Pin SOIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.201	4.70	5.11
A1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	.030

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

BURR-BROWN®

OPA627

ADVANCE INFORMATION
SUBJECT TO CHANGE

Precision High-Speed *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- VERY LOW NOISE: 5.4nV/√Hz at 10kHz
- FAST SETTLING TIME: 600ns to 0.01%
- LOW V_{OS}: 100μV max
- LOW DRIFT: 0.8μV/°C max
- LOW I_B: 20pA max
- UNITY-GAIN STABLE

APPLICATIONS

- FAST DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY

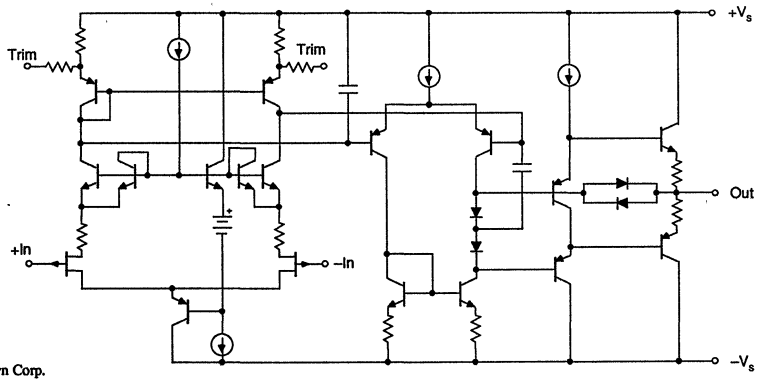
DESCRIPTION

The OPA627 ***Difet*** operational amplifier provides a new level of performance in a precision FET op amp. When compared to the popular OPA111 op amp, the OPA627 has lower noise voltage, offset voltage and drift, and much higher speed. It is useful in a wide range of precision and low noise analog circuitry.

The OPA627 is fabricated on a proprietary high-speed, dielectrically-isolated complementary npn/pnp process. Laser-trimmed input circuitry yields excellent DC performance. High-frequency complementary transistors increase circuit bandwidth, attaining speeds previously not possible with precision FET op amps. The OPA627 is unity-gain stable.

Difet construction achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry.

The OPA627 is available in Plastic DIP and Metal TO-99 packages. Industrial and Military temperature range gradeouts are available.



Difet® Burr-Brown Corp.

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491 • FAX: (602) 889-1510

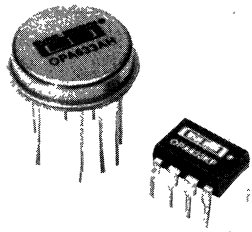
PDS-860

SPECIFICATIONS

T_A = +25°C, V_S = ±15V unless otherwise noted.

		OPA627BM			OPA627AM/AP/SM			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OFFSET VOLTAGE								
Input Offset Voltage			40	100		130	250	µV
Over Specified Temperature			70	180		230	450	µV
Average Drift			0.5	0.8		1.2	2.0	µV/°C
Power Supply Rejection	V_S = ±4.5 to ±18V	106			100			dB
INPUT BIAS CURRENT								
Input Bias Current	V_{CM} = 0V		8	20		20	50	pA
Over Specified Temperature	V_{CM} = 0V			1.6			3.2	nA
SM Grade							50	nA
Input Offset Current	V_{CM} = 0V		8	20		20	50	pA
NOISE								
Input Voltage Noise								
Noise Density, f = 10Hz			30	60		40	80	nV/√Hz
f = 100Hz			11	30		15	40	nV/√Hz
f = 1kHz			5.2	5.8		5.6	6.8	nV/√Hz
f = 10kHz			4.8	5.4		5.2	6.2	nV/√Hz
Voltage Noise, BW = 0.1 to 10Hz			1.2	2.5		1.6	3.3	µVp-p
Input Current Noise								
Noise Density, f = 1kHz			1.6	2.5		2.5	4.0	fA/√Hz
Current Noise, BW = 0.1 to 10Hz			30	60		48	90	fAp-p
INPUT IMPEDANCE								
Differential			10^{13} || 2			*		GΩ || pF
Common-Mode			10^{14} || 6			*		GΩ || pF
INPUT VOLTAGE RANGE								
Common-mode Input Range		±11	±11.5		*	*		V
Over Specified Temperature		±10.5	±11		*	*		V
Common-mode Rejection	V_{CM} = ±10V	106			100			dB
OPEN-LOOP GAIN								
Open-loop Voltage Gain	V_O = ±10V, R_L = 1kΩ	110	115		104	115		dB
Over Specified Temperature	V_O = ±10V, R_L = 1kΩ	104	106		98	106		dB
FREQUENCY RESPONSE								
Slew Rate	G = –1	45	55		40	50		V/µs
Settling Time, 0.01%	G = –1		500	600		600	750	ns
0.1%	G = –1		400			*		ns
Gain-Bandwidth Product	G = 100		16			*		MHz
Total Harmonic Distortion	G = +10, f = 1kHz							%
POWER SUPPLY								
Specified Operating Voltage			±15					V
Operating Voltage Range		±4.5		±18				V
Current			±6.5	±8				mA
OUTPUT								
Voltage Output	R_L = 1kΩ	±12	±13		*	*		V
Over Specified Temperature		±11	±12.5		*	*		V
Current Output			±30			*		mA
Short Circuit Current		±35	±55	±85	*	*	*	mA
Output Resistance, Open-loop	1MHz							Ω
Load Capacitance		300	500		*	*		pF
TEMPERATURE RANGE								
Specification								
AP, AM, BM		–25		+85				°C
SM		–55		+125				°C
Storage								
AP		–40		+125				°C
AM, BM, SM		–60		+150				°C

BURR-BROWN®



OPA633

AVAILABLE IN DIE FORM

High Speed BUFFER AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 275MHz
- HIGH SLEW RATE: 2500V/μs
- HIGH OUTPUT CURRENT: 100mA
- LOW OFFSET VOLTAGE: 1.5mV
- REPLACES HA-5033
- IMPROVED PERFORMANCE/PRICE: LH0033, LTC1010, HOS200

APPLICATIONS

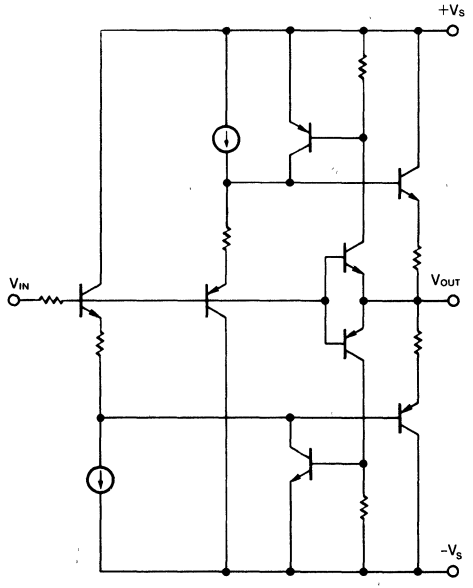
- OP AMP CURRENT BOOSTER
- VIDEO BUFFER
- LINE DRIVER
- A/D CONVERTER INPUT BUFFER

DESCRIPTION

The OPA633 is a monolithic unity-gain buffer amplifier featuring very wide bandwidth and high slew rate. A dielectric isolation process incorporating both NPN and PNP high frequency transistors achieves performance unattainable with conventional integrated circuit technology. Laser trimming provides low input offset voltage.

High output current capability allows the OPA633 to drive 50Ω and 75Ω lines, making it ideal for RF, IF and video applications. Low phase shift allows the OPA633 to be used inside amplifier feedback loops thus bringing high current output and ability to drive capacitive loads to many circuit applications.

The OPA633 is available in the 12-pin TO-8 hermetic metal package with −25°C to +85°C and −55°C to +125°C temperature ranges and a low cost plastic DIP package specified for operation from 0°C to +75°C.



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PDS-699A

SPECIFICATIONS

ELECTRICAL

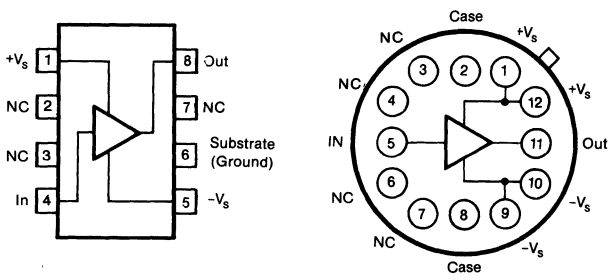
At +25°C, $V_S = \pm 12V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $C_L = 10pF$ unless otherwise noted

PARAMETER	CONDITIONS	OPA633AH MIN	OPA633AH TYP	OPA633AH MAX	OPA633SH MIN	OPA633SH TYP	OPA633SH MAX	OPA633KP MIN	OPA633KP TYP	OPA633KP MAX	UNITS
FREQUENCY RESPONSE											
Small Signal Bandwidth			275			*			260		MHz
Full Power Bandwidth	$V_O = 1Vrms$, $R_L = 1k\Omega$		65			*			40		MHz
Slew Rate	$V_O = 10V$, $V_S = \pm 15V$, $R_L = 1k\Omega$	1000	2500		*	*		*	*		V/μs
Rise Time, 10% to 90%	$V_O = 500mV$		2 5			*			*		ns
Propagation Delay			1			*			*		ns
Overshoot			10			*			*		%
Settling Time, 0 1%			50			*			*		ns
Differential Phase Error[1]			0 1			*			*		Degrees
Differential Gain Error[1]			0 1			*			*		%
Total Harmonic Distortion	$V_O = 1Vrms$, $R_L = 1k\Omega$, f = 100kHz		0 005			*			*		%
	$V_O = 1Vrms$, $R_L = 100\Omega$, f = 100kHz		0 02								%
OUTPUT CHARACTERISTICS											
Voltage	$T_A = T_{MIN}$ to T_{MAX}	±8 0	±10		*	*		*	*		V
	$R_L = 1k\Omega$, $V_S = \pm 15V$	±11	±13		*	*		*	*		V
Current		±80	±100		*	*		*	*		mA
Resistance			5			*			*		Ω
TRANSFER CHARACTERISTICS											
Gain		0 93	0 95		*	*		*	*		V/V
	$R_L = 1k\Omega$		0 99			*			*		V/V
	$T_A = T_{MIN}$ to T_{MAX}	0 92	0 95		*	*		*	*		V/V
INPUT											
Offset Voltage	$T_A = +25°C$		±1 5	±15		*	*		±5	*	mV
	$T_A = T_{MIN}$ to T_{MAX}		±5	±25		*	*		±6	*	mV
vs Temperature			±33			*			*		μV/°C
vs Supply	$T_A = T_{MIN}$ to T_{MAX}	54	72		*	*		*	*		dB
Bias Current	$T_A = +25°C$		±15	±35		*	*		*	*	μA
	$T_A = T_{MIN}$ to T_{MAX}		±20	±50		*	*		*	*	μA
Noise Voltage	10Hz to 1MHz		20			*			*		μVp-p
Resistance			1 5			*			*		MΩ
Capacitance			1 6			*			*		pF
POWER SUPPLY											
Rated Supply Voltage	Specified performance		±12			*			*		V
Operating Supply Voltage	Derated performance	±5		±16	*		*	*		*	V
Current, Quiescent	$I_O = 0$		21	25		*	*		*	*	mA
	$I_O = 0$, $T_A = T_{MIN}$ to T_{MAX}		21	30		*	*		*	*	mA
TEMPERATURE RANGE											
Specification, Ambient		−25		+85	−55		+125	0		+75	°C
Operating, Ambient		−55		+125	*		*	−25		+85	°C
θ Junction, Ambient[2]			99			*			90		°C/W
θ Junction, Case[2]			31			*			27		°C/W

* Specification same as OPA633AH

NOTES (1) Differential phase error in video transmission systems is the change in phase of a color subcarrier resulting from a change in picture signal from blanked to white Differential gain error is the change in amplitude at the color subcarrier frequency resulting from a change in picture signal from blanked to white (2) Recommended heat sinks for the TO-8 package are Thermalloy 2204A with $\theta_{SA} = 27°C/W$ and IERC Up TO-8-48CB, $\theta_{SA} = 10°C/W$

CONNECTION DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Power Supply, $\pm V_S$	±20V
Input Voltage V_{IN}	$+V_S + 2$ to $-V_S - 2$
Output Current (peak)	±200mA
Internal Power Dissipation (25°C) TO-8 (H)	1.75W
DIP (P)	1 95W
Junction Temperature	200°C
Storage Temperature Range TO-8	−65°C to +150°C
DIP	−40°C to +85°C
Lead Temperature (soldering, 60s)	300°C

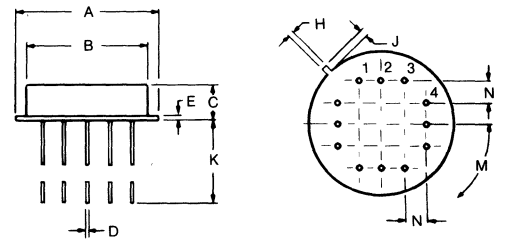
ORDERING INFORMATION

Model	Package	Temperature Range	Full Power Bandwidth (MHz)
OPA633AH	Ceramic	–25°C to +85°C	65
OPA633SH	Ceramic	–55°C to +125°C	65
OPA633KP	Plastic	0°C to +75°C	40
BURN-IN SCREENING OPTION			
Model	**Package**	**Temperature Range**	**Burn-In Temp. (160h)[1]**
OPA633AH-BI	Ceramic	–25°C to +85°C	+125°C
OPA633SH-BI	Ceramic	–55°C to +125°C	+125°C
OPA633KP-BI	Plastic	0°C to +75°C	+85°C

NOTE. (1) Or equivalent combination of time and temperature.

MECHANICAL

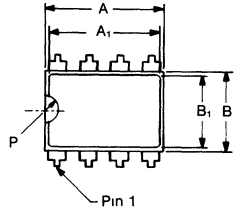
TO-8



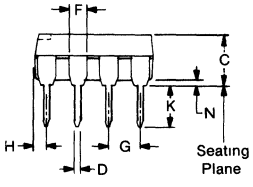
NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

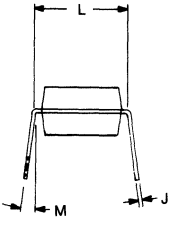
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	593	603	15 06	15 32
B	547	553	13 89	14 05
C	130	150	3 30	3 81
D	016	019	0 41	0 48
E	010	040	0 25	1 02
H	026	036	0 66	0 91
J	026	036	0 66	0 91
K	500	562	12 70	14 27
M	45° BASIC		45° BASIC	
N	100 BASIC		2 54 BASIC	

"P" Package, 8-Pin Plastic



NOTE Leads in true position within 0 01" (0 25mm) R at MMC at seating plane

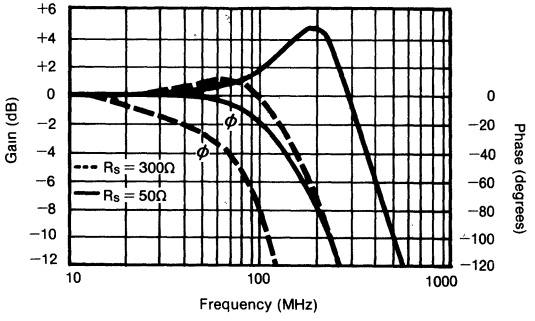




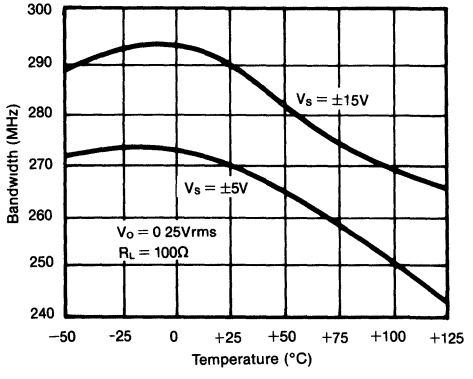
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	355	400	9 03	10 16
A_1	340	385	8 65	9.80
B	230	290	5 85	7 38
B_1	200	250	5 09	6 36
C	120	200	3 05	5 09
D	015	023	0 38	0 59
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	025	050	0 64	1 27
J	008	015	0 20	0 38
K	070	150	1 78	3 82
L	300 BASIC		7 63 BASIC	
M	0°	15°	0°	15°
N	010	030	0 25	0 76
P	025	050	0 64	1 27

TYPICAL PERFORMANCE CURVES

GAIN/PHASE VS FREQUENCY

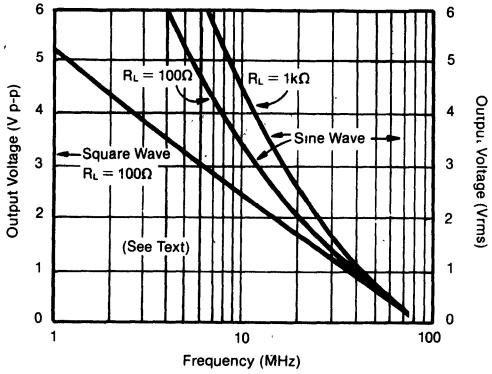


SMALL SIGNAL BANDWIDTH VS TEMPERATURE

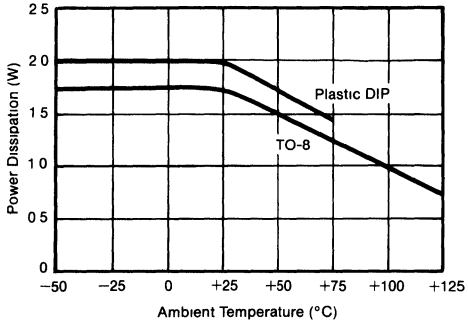


TYPICAL PERFORMANCE CURVES (CONT)

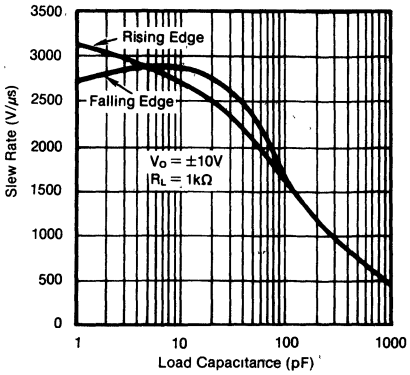
SAFE INPUT VOLTAGE VS FREQUENCY



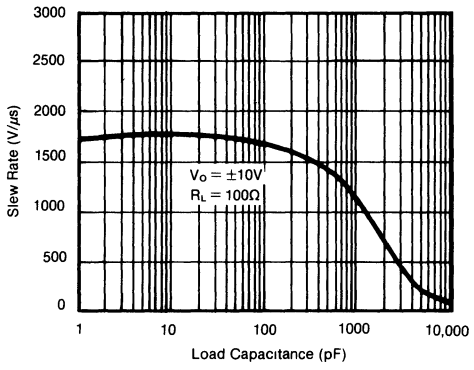
MAXIMUM POWER DISSIPATION VS AMBIENT TEMPERATURE



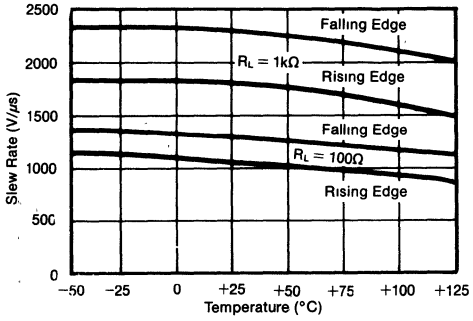
SLEW RATE VS LOAD CAPACITANCE



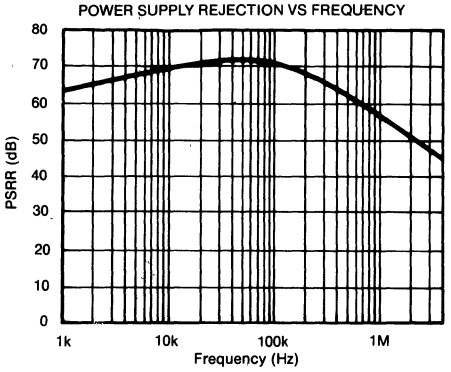
SLEW RATE VS LOAD CAPACITANCE



SLEW RATE VS TEMPERATURE

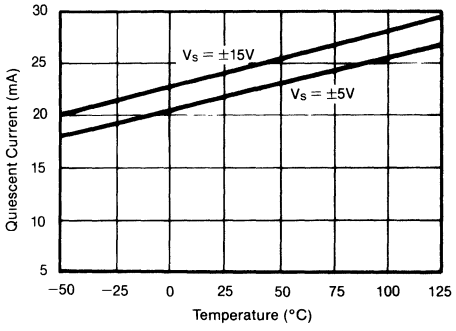


POWER SUPPLY REJECTION VS FREQUENCY

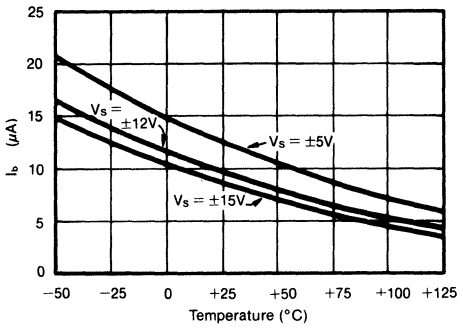


TYPICAL PERFORMANCE CURVES (CONT)

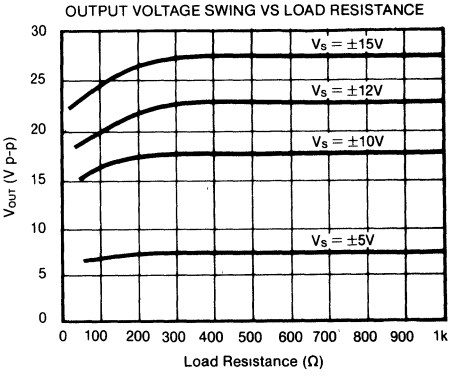
QUIESCENT CURRENT VS TEMPERATURE



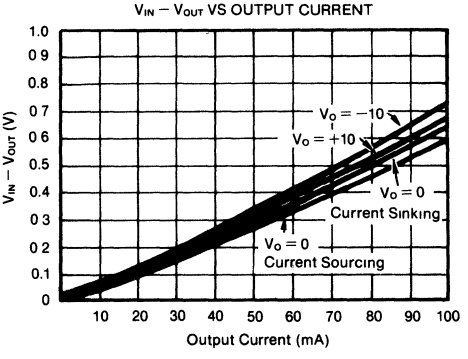
INPUT BIAS CURRENT VS TEMPERATURE



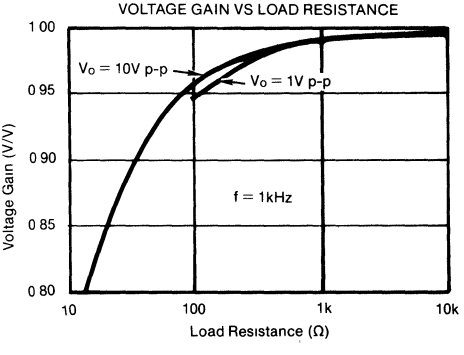
OUTPUT VOLTAGE SWING VS LOAD RESISTANCE



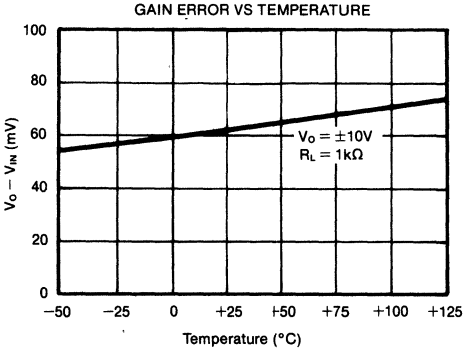
$V_{IN} - V_{OUT}$ VS OUTPUT CURRENT



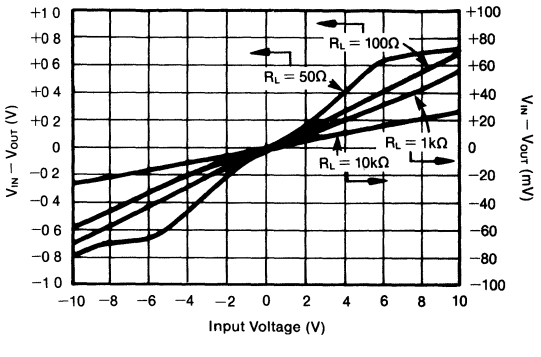
VOLTAGE GAIN VS LOAD RESISTANCE



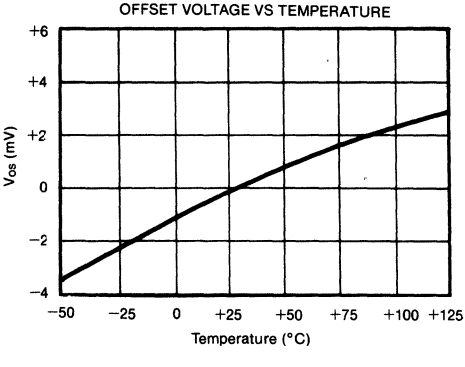
GAIN ERROR VS TEMPERATURE



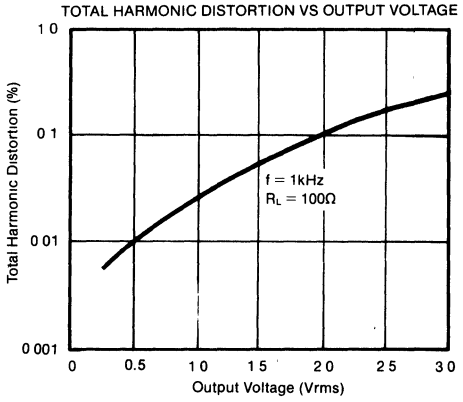
OUTPUT ERROR VS INPUT VOLTAGE

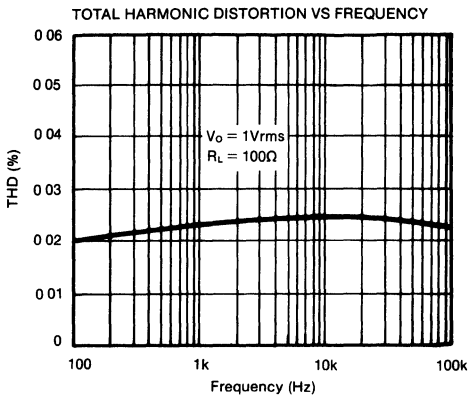


OFFSET VOLTAGE VS TEMPERATURE



TYPICAL PERFORMANCE CURVES (CONT)





INSTALLATION AND OPERATION

CIRCUIT LAYOUT

As with any high frequency circuitry, good circuit layout technique must be used to achieve optimum performance. A circuit-board layout is provided which demonstrates the principles of good layout. Most of the applications circuits shown can be evaluated using this circuit board.

Pinout of the TO-8 package version has been designed for maximum compatibility with other buffer amplifiers. Pins 1 and 12 are internally connected to $+V_S$. Pins 9 and 10 are internally connected to $-V_S$. This allows the OPA633 to be used in applications presently using the LH0033 buffer amplifier. Only one of the power supply connections for $+V_S$ and $-V_S$ must be connected for proper operation.

Power supply connections must be bypassed with high frequency capacitors. Many applications benefit from the use of two capacitors on each power supply—a ceramic capacitor for good high frequency decoupling and a tantalum type for lower frequencies. They should be located as close as possible to the buffer's power supply pins. A large ground plane is used to minimize high frequency ground drops and stray coupling.

The case of the TO-8 package is connected to pin 2, which should be grounded. Pin 6 of the DIP package connects to the substrate of the integrated circuit and should be connected to ground. In principle it could also be connected to $+V_S$ or $-V_S$, but ground is preferable. The additional lead length and capacitance associated with sockets may present problems in applications requiring the highest fidelity of high speed pulses.

Depending on the nature of the input source impedance, a series input resistor may be required for best stability. This behavior is influenced somewhat by the load impedance (including any reactive effects). A value of 50Ω to 200Ω is typical. This resistor should be located close to the OPA633's input pin to avoid stray capacitance at the input which could reduce bandwidth (see Gain and Phase Versus Frequency curve).

OVERLOAD CONDITIONS

The input and output circuitry of the OPA633 are not protected from overload. When the input signal and load characteristics are within the device's capabilities, no protection circuitry is required. Exceeding device limits can result in permanent damage.

The OPA633's small package and high output current capability can lead to overheating. The internal junction temperature should not be allowed to exceed 150°C. Although failure is unlikely to occur until junction temperature exceeds 200°C, reliability of the part will be degraded significantly at such high temperatures. External heat sinks can be used to reduce the temperature rise. Since significant heat transfer takes place through the package leads, wide printed circuit traces to all leads will improve heat sinking. Sockets can reduce heat sinking significantly and thus are not recommended.

Junction temperature rise is proportional to internal power dissipation. This can be reduced by using the minimum supply voltage necessary to produce the required output voltage swing. For instance, 1V video signals can be easily handled with ±5V power supplies thus minimizing the internal power dissipation.

Output overloads or short circuits can result in permanent damage by causing excessive output current. The 50Ω or 75Ω series output resistor used to match line impedance will, in most cases, provide adequate protection. When this resistor is not used, the device can be protected by limiting the power supply current. See "Protection Circuits."

Excessive input levels at high frequency can cause increased internal dissipation and permanent damage. See the safe input voltage versus frequency curves. When used to buffer an op amp's output, the input to the OPA633 is limited, in most cases, by the op amp. When high frequency inputs can exceed safe levels, the device must be protected by limiting the power supply current.

PROTECTION CIRCUITS

The OPA633 can be protected from damage, due to excessive currents, by the simple addition of resistors in series with the power supply pins (Figure 5a). While this limits output current, it also limits voltage swing with low impedance loads. This reduction in voltage swing is minimal for AC or high crest factor signals since only the average current from the power supply causes a voltage drop across the series resistor. Short duration load-current peaks are supplied by the bypass capacitors.

The circuit of Figure 5b overcomes the limitations of the previous circuit with DC loads. It allows nearly full output voltage swing up to its current limit of approximately 140mA. Both circuits require good high frequency capacitors (e.g., tantalum) to bypass the buffer's power supply connections.

CAPACITIVE LOADS

The OPA633 is designed to safely drive capacitive loads up to 0.01μF. It must be understood, however, that rapidly changing voltages demand large output load currents:

$$I_{LOAD} = (C_{LOAD})\, dV/dt$$

Thus a signal slew rate of 1000V/μs and load capacitance of 0.01μF demands a load current of 10A. Clearly maximum slew rates cannot be combined with large capacitive loads. Load current should be kept less than 100mA continuous (200mA peak) by limiting the rate of change of the input signal or reducing the load capacitance.

USE INSIDE A FEEDBACK LOOP

The OPA633 may be used inside the feedback path of an op amp such as the OPA606. Higher output current is achieved without degradation in accuracy. This approach may actually improve performance in precision applications by removing load-dependent dissipation from a precision op amp. All vestiges of load-dependent offset voltage and temperature drift can be eliminated with this technique. Since the buffer is placed within the feedback loop of the op amp, its DC errors will have a negligible effect on overall accuracy. Any DC errors contributed by the buffer are divided by the loop gain of the op amp.

The low phase shift of the OPA633 allows its use inside the feedback loop of a wide variety of op amps. To assure stability, the buffer must not add significant phase shift to the loop at the gain crossing frequency of the circuit—the frequency at which the open loop gain of the op amp is equal to the closed loop gain of the application. The OPA633 has a typical phase shift of less than 10° up to 70MHz, thus making it useful even with wideband op amps.

BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information table. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

APPLICATIONS CIRCUITS

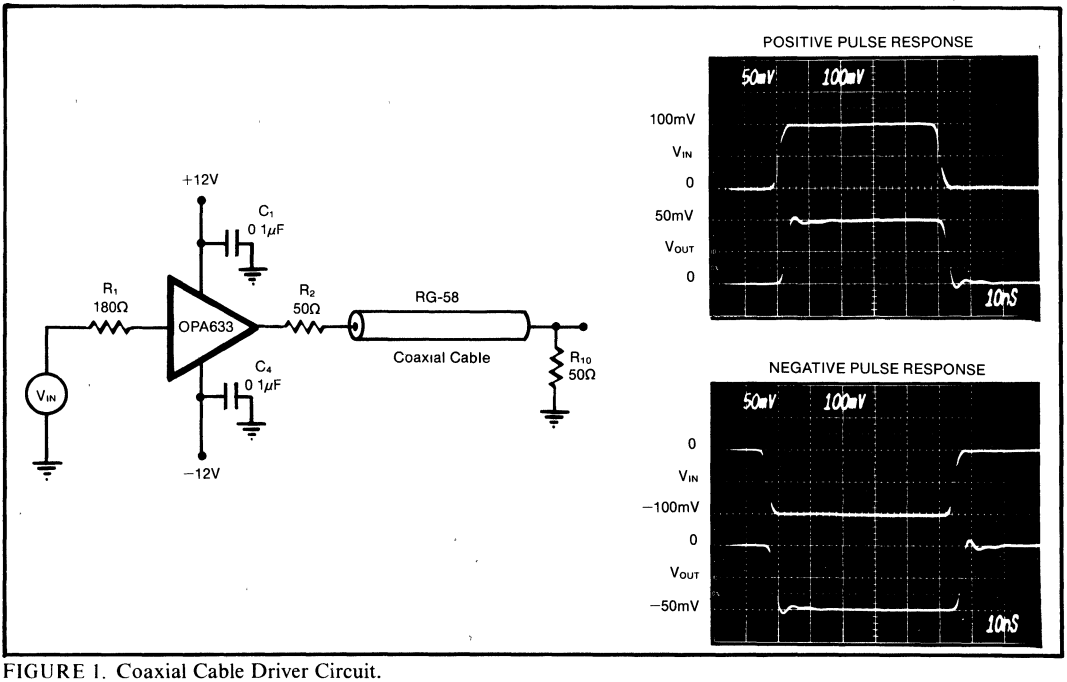


FIGURE 1. Coaxial Cable Driver Circuit.

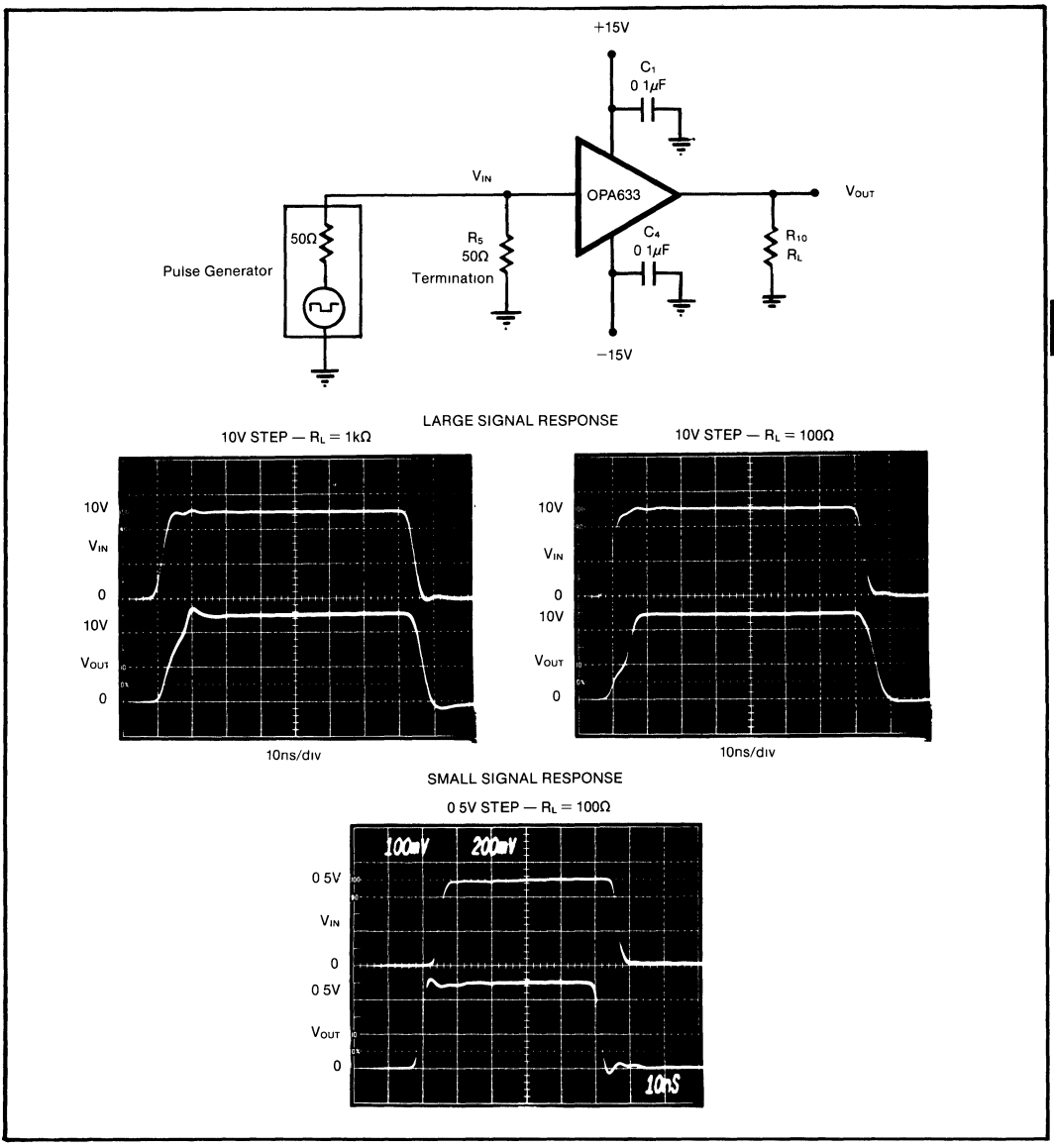


FIGURE 2. Dynamic Response Test Circuit.

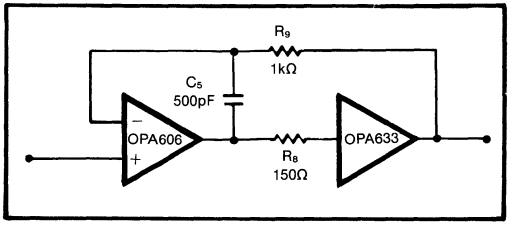


FIGURE 3. Precision High Current Buffer.

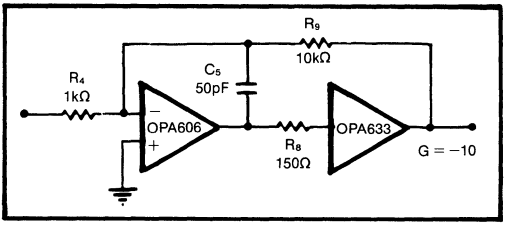


FIGURE 4. Buffered Inverting Amplifier.

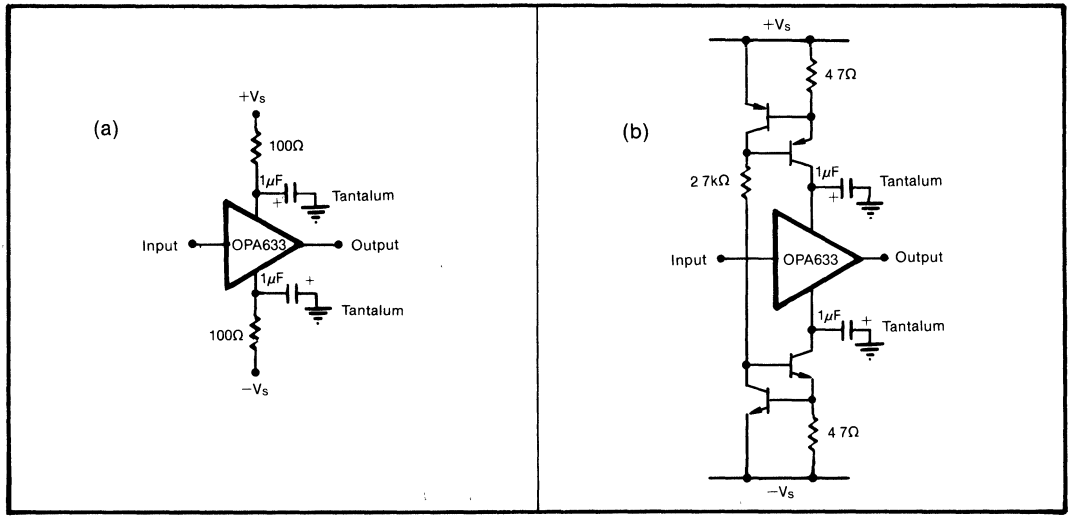
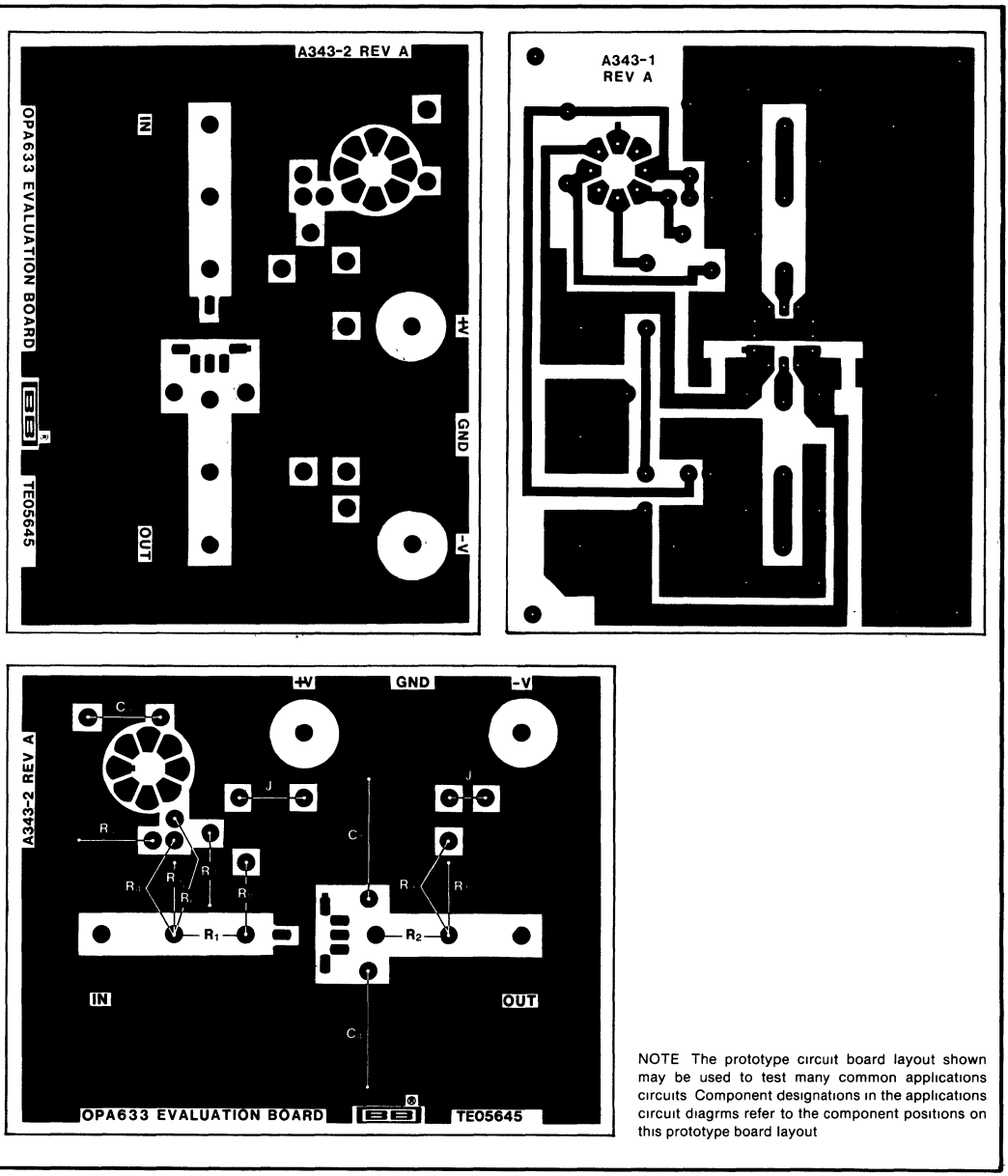


FIGURE 5. Output Protection Circuits.

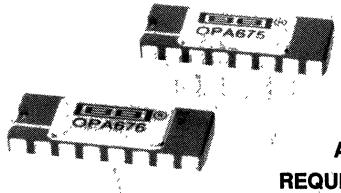


NOTE The prototype circuit board layout shown may be used to test many common applications circuits Component designations in the applications circuit diagrms refer to the component positions on this prototype board layout

FIGURE 6. Prototype Circuit Board Layout.

BURR - BROWN®

MILITARY
VERSION
AVAILABLE



OPA675
OPA676

ABRIDGED DATA SHEET
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Wideband Switched-Input OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING: 9ns (1%)
- WIDE BANDWIDTH: 185MHz (A_V = 10)
- LOW OFFSET VOLTAGE: ±250μV
- TWO LOGIC SELECTABLE INPUTS
- FAST INPUT SWITCHING: 6ns (TTL)
- 16-PIN DIP PACKAGE

APPLICATIONS

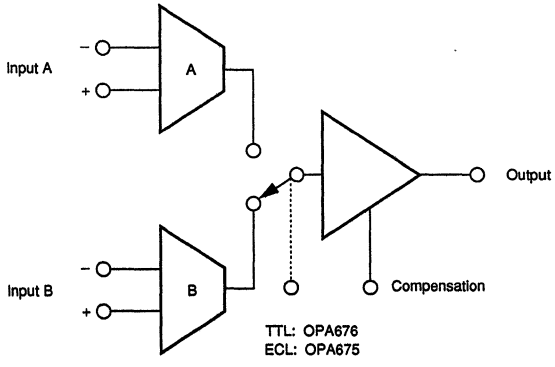
- PROGRAMMABLE-GAIN AMPLIFIER
- FAST 2-INPUT MULTIPLEXER
- SYNCHRONOUS DEMODULATOR
- PULSE/RF AMPLIFIERS
- VIDEO AMPLIFIERS
- ACTIVE FILTERS

DESCRIPTION

The OPA675 and OPA676 are wideband monolithic operational amplifiers with two independent differential inputs. Either input can be selected by an external logic signal. The OPA675 is compatible with differential ECL logic while the OPA676 is TTL compatible. Both amplifiers are externally compensated and feature very fast input selection speed: ECL = 4ns, TTL = 6ns. This amplifier features fully symmetrical differential inputs due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA675/676 may be used in all op-amp applications requiring high speed and precision.

Low distortion and crosstalk make these amplifiers suitable for RF and video applications.

The OPA675 and OPA676 are available in KG (0°C to +70°C) and SG (–55°C to +125°C) grades. All grades are packaged in a 16-pin DIP.



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PDS-864

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	JG MIN	JG TYP	JG MAX	SG MIN	SG TYP	SG MAX	KG MIN	KG TYP	KG MAX	UNITS
INPUT NOISE[1]											
Voltage: f_O = 10Hz	R_S = 0Ω		27			*			*		nV/√Hz
f_O = 100 Hz			10			*			*		nV/√Hz
f_O = 1kHz			3.8			*			*		nV/√Hz
f_O = 10kHz			2.6			*			*		nV/√Hz
f_O = 100kHz			2.4			*			*		nV/√Hz
f_B = 10Hz to 10MHz			7.9			*			*		µVrms
Current: f_O = 10Hz to 1MHz			2.7			*			*		pA/√Hz
OFFSET VOLTAGE[1]											
Input Offset Voltage	V_{CM} = 0VDC		±500	±2mV		*	*		±250	±1mV	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3	±10		*	*		±1	±5	µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	65	86		*	*		70	*		dB
BIAS CURRENT[1]											
Input Bias Current	V_{CM} = 0VDC		23	35		*	*		*	30	µA
OFFSET CURRENT[1]											
Input Offset Current	V_{CM} = 0VDC		0.8	5		*	*		*	*	µA
INPUT IMPEDANCE[1]											
Differential			10^6 || 2			*			*		Ω || pF
Common-Mode			10^8 || 5			*			*		Ω || pF
INPUT VOLTAGE RANGE[1]											
Common-Mode Input Range		±2.1	±2.5		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC	75	100		*	*		85	*		dB
OPEN LOOP GAIN, DC[1]											
Open-Loop Voltage Gain		65	70		*	*		*	*		dB
FREQUENCY RESPONSE											
Closed-Loop Bandwidth	Gain = +2V/V		100			*			*		MHz
	Gain = +5V/V		145			*			*		MHz
	Gain = +10V/V		185			*			*		MHz
	Gain = +50V/V		60			*			*		MHz
Crosstalk	Gain = +10V/V, f = 100kHz		–100			*			*		dBC[2]
	f = 1MHz		–80			*			*		dBC
	f = 10MHz		–68			*			*		dBC
	f = 100MHz		–35			*			*		dBC
Harmonic Distortion: 10MHz	G= +10V/V,R_L=50Ω,V_O=0.5Vp-p										
	second harmonic		–61			*			*		dBC
	third harmonic		–73			*			*		dBC
Full Power Response	V_O = 2.5Vp-p, Gain = +16V/V	25	44		*	*		30	*		MHz
Slew Rate	Gain = +16V/V	200	350		*	*		240	*		V/µs
Settling Time: 1%			9			*			*		ns
0.1%	Gain = +16 V/V		15			*			*		ns
0.01%	0.625V step		25			*			*		ns
INPUT SELECTION[3]											
Transition Time	ECL: OPA675		4			*			*		ns
50% in to 50% Out	TTL: OPA676		6			*			*		ns
DIGITAL INPUT											
TTL Logic Levels: V_{IL}	Logic "LO", I_{IL} = –6.4mA	0		+0.8	*		*	*		*	V
V_{IH}	Logic "HI", I_{IH} = 160µA	+2.0		+5	*		*	*		*	V
I_{IL}	Logic "LO", V_{IL} = +0.8V		–0.05	–0.2		*	*		*	*	mA
I_{IH}	Logic "HI", V_{IH} = +2.8V		1	20		*	*		*	*	µA
ECL Logic Levels: V_{IL}	Logic "LO"	–1.15		–0.88	*		*	*		*	V
V_{IH}	Logic "HI"	–1.81		–1.475	*		*	*		*	V
I_{IL}	Logic "LO", V_{IL} = –1.6V		0.05			*			*		µA
I_{IH}	Logic "HI", V_{IH} = –1.0V		50			*			*		µA
RATED OUTPUT											
Voltage Output	R_L = 150Ω	±2.1	±2.6		*	*		*	*		V
	R_L = 50Ω	+1.25	+1.8		*	*		*	*		V
		–0.95	–1.1		*	*		–1.0	*		V
Current Output			±30			*			*		mA
Output Resistance	1MHz, Open Loop, C_C = 5pF		5			*			*		Ω
Load Capacitance Stability	Gain = +2V/V		50			*			*		pF
Short Circuit Current	Momentary	±30	±50		*	*		±30	*		mA

* Same specifications as for JG.

SPECIFICATIONS (Cont)

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	JG			SG			KG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY											
Rated Voltage	±V_{CC}		5			*			*		VDC
Derated Performance	±V_{CC}	4.5		6.5	*		*	*		*	VDC
Current, Quiescent	I_O = 0mADC		22	30		*	*		*	*	mA
TEMPERATURE RANGE											
Specification	Ambient temp	0		+70	–55		+125	*		*	°C
Operating:	Ambient temp	–55		+125	*		*	*		*	°C
θ_{JA}			125			*			*		°C/W

* Same specifications as for JG.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

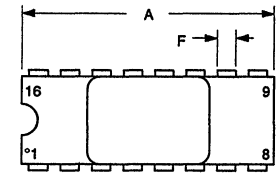
PARAMETER	CONDITIONS	JG			SG			KG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification	Ambient temp	0		+70	–55		+125	*		*	°C
OFFSET VOLTAGE											
Average Drift	T_A = T_{MIN} to T_{MAX}		±3	±10		*	*		±1	±5	µV/°C
Supply Rejection	±V_{CC} = 4.5V to 5.5V	60	85		*	*		65	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		29	50		*	*		*	*	µA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		0.8	10		*	*		*	*	µA
INPUT VOLTAGE RANGE											
Common-Mode Input Range		±2.0	±2.3		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC	60	80		*	*		65	*		dB
OPEN LOOP GAIN, DC											
Open-Loop Voltage Gain		60	68		*	*		63	69		dB
DIGITAL INPUT											
TTL Logic Levels: V_{IL}	Logic "LO", I_{IL} = – 6.4mA	0		+0.8	*		*	*		*	V
V_{IH}	Logic "HI", I_{IH} = 160µA	+2.0		+5	*		*	*		*	V
I_{IL}	Logic "LO", V_{IL} = +0.8V		–0.08	–0.4		*	*		*	*	mA
I_{IH}	Logic "HI", V_{IH} = +2.8V		5	50		*	*		*	*	µA
ECL Logic Levels: V_{IL}	Logic "LO"	–1.15		–0.88	*		*	*		*	V
V_{IH}	Logic "HI"	–1.81		–1.475	*		*	*		*	V
I_{IL}	Logic "LO", V_{IL} = –1.6V		0.05			*			*		µA
I_{IH}	Logic "HI", V_{IH} = –1.0V		50			*			*		µA
RATED OUTPUT											
Voltage Output	R_L = 150Ω	±2.0	±2.5		*	*		*	*		V
	R_L = 50Ω	+1.25	+1.6		*	*		*	*		V
		–0.8	–1.0		*	*		–0.9	*		V
POWER SUPPLY											
Current, Quiescent	I_O = 0mADC		25	35		*	*		*	*	mA

* Same specifications as for JG.

NOTES: (1) Specifications are for both inputs (A and B). (2) dBC = Level referred to carrier-input signal. (3) Switching time from application of digital logic signal to input signal selection.

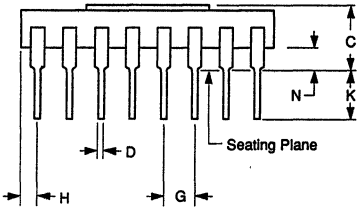
MECHANICAL

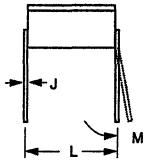
G Package— 16 Pin Ceramic DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.





PIN ASSIGNMENTS: OPA675

1	+In A	16	+In B
2	–In A	15	–In B
3	Offset Trim	14	DNC
4	Offset Trim	13	$\overline{\text{CHA}}$ (ECL)
5	Compensation Capacitor	12	CHA (ECL)
6	NC	11	Common
7	$+V_{cc}$	10	$-V_{cc}$
8	Output	9	NC

PIN ASSIGNMENTS: OPA676

1	+In A	16	+In B
2	–In A	15	–In B
3	Offset Trim	14	DNC
4	Offset Trim	13	$\overline{\text{DNC}}$
5	Compensation Capacitor	12	CHA (TTL)
6	NC	11	Common
7	$+V_{cc}$	10	$-V_{cc}$
8	Output	9	NC

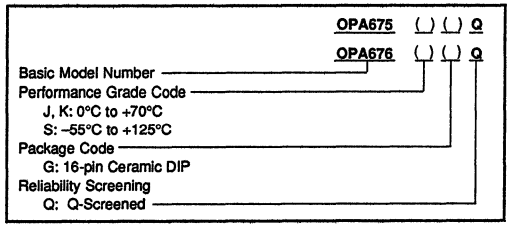
DNC = Do Not Connect

NC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

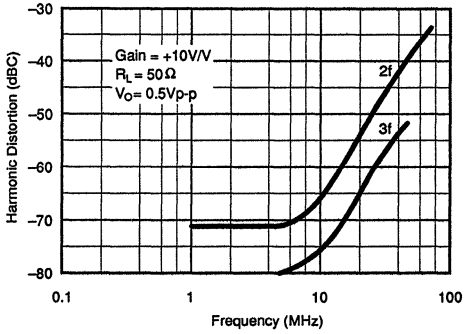
Supply	±7VDC
Internal Power Dissipation	1000mW
Differential Input Voltage	Total V_{cc}
Input Voltage Range	$\pm V_{cc}$
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Ground (+25°C)	Continuous to ground
Junction Temperature	+175°C

ORDERING INFORMATION

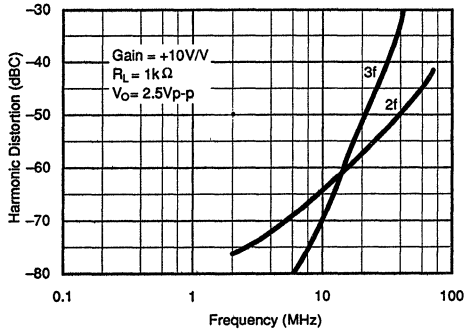


TYPICAL PERFORMANCE CURVES

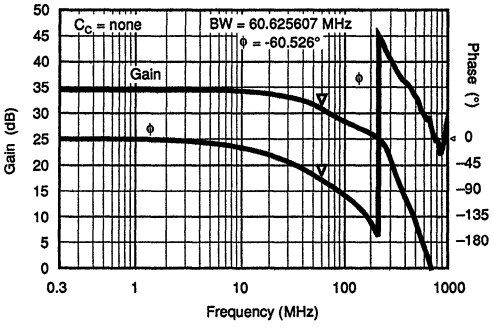
SMALL SIGNAL
HARMONIC DISTORTION vs FREQUENCY



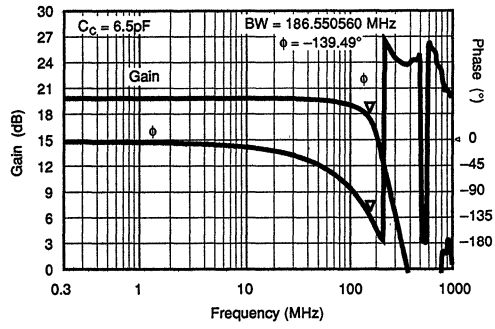
LARGE SIGNAL
HARMONIC DISTORTION vs FREQUENCY



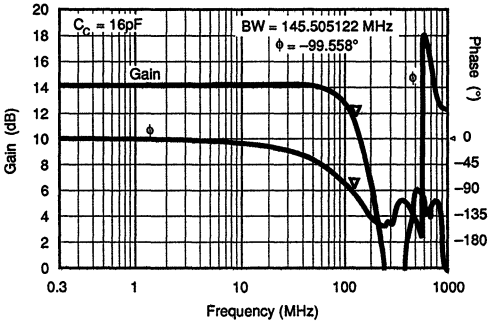
A_V = +50V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



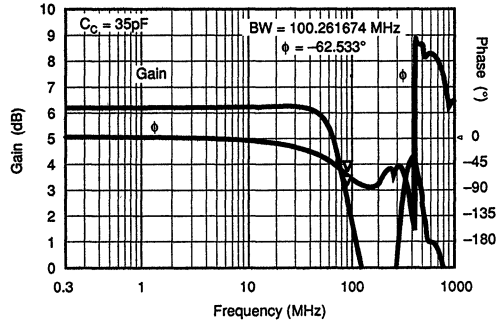
A_V = +10V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH

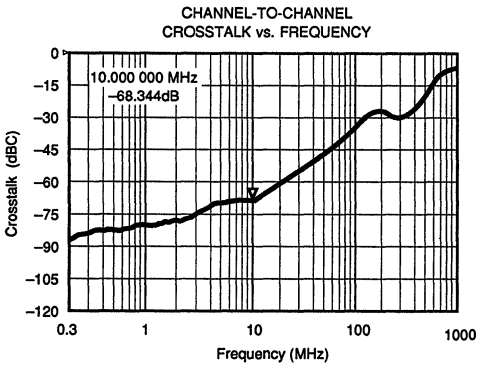


A_V = +5V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH

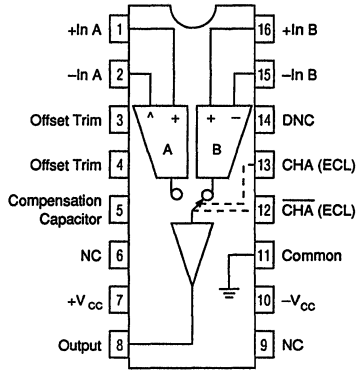


A_V = +2V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH

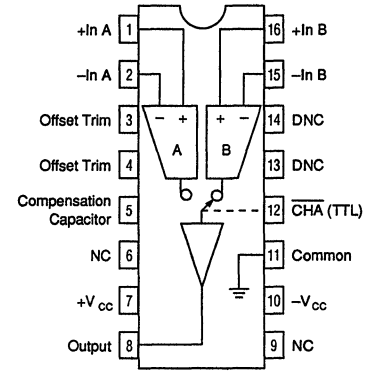


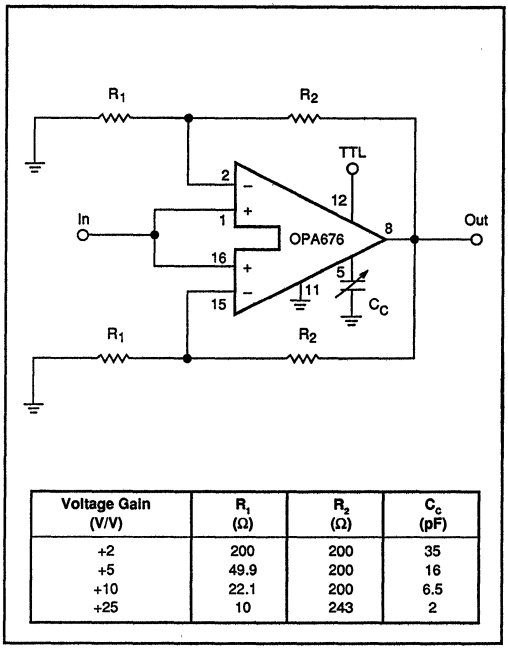


OPA675



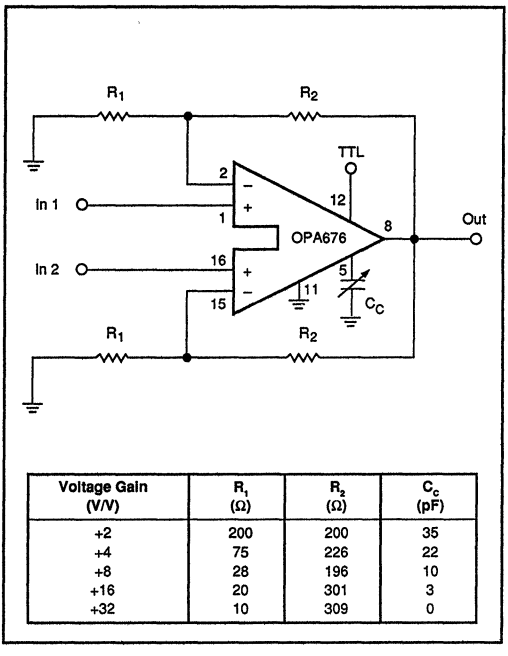
OPA676





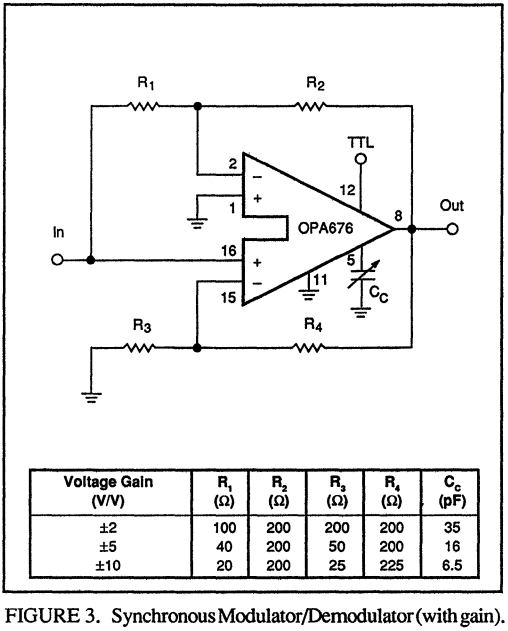
Voltage Gain (V/V)	R_1 (Ω)	R_2 (Ω)	C_c (pF)
+2	200	200	35
+5	49.9	200	16
+10	22.1	200	6.5
+25	10	243	2

FIGURE 1. Programmable-Gain Amplifier.



Voltage Gain (V/V)	R_1 (Ω)	R_2 (Ω)	C_c (pF)
+2	200	200	35
+4	75	226	22
+8	28	196	10
+16	20	301	3
+32	10	309	0

FIGURE 2. Two-Input Multiplexer (with gain).



Voltage Gain (V/V)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)	C_c (pF)
±2	100	200	200	200	35
±5	40	200	50	200	16
±10	20	200	25	225	6.5

FIGURE 3. Synchronous Modulator/Demodulator (with gain).

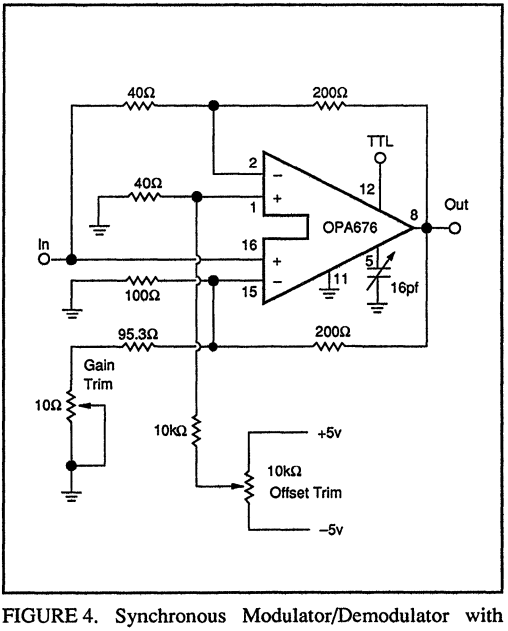


FIGURE 4. Synchronous Modulator/Demodulator with Carrier Balance Trim (gain = ±5V/V).

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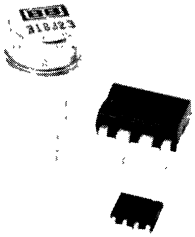


OPA2107

ADVANCE INFORMATION SUBJECT TO CHANGE

Precision Dual *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- VERY LOW NOISE: 8nV/√Hz at 10kHz
- LOW V_{OS}: 500µV max
- LOW DRIFT: 5µV/°C max
- LOW I_B: 6pA max
- FAST SETTLING TIME: 1.5µs to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

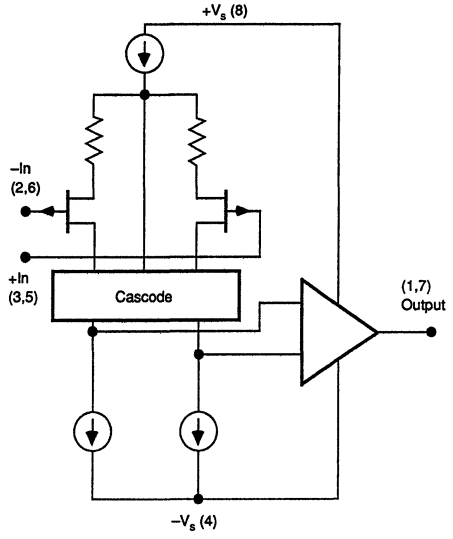
- DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- MEDICAL EQUIPMENT—CT SCANNERS

DESCRIPTION

The OPA2107 Dual operational amplifier provides precision ***Difet*** performance with the cost and space savings of a dual op amp. It is useful in a wide range of precision and low-noise analog circuitry and can be used to upgrade the performance of designs currently using BIFET® type amplifiers.

The OPA2107 is fabricated on a proprietary dielectrically-isolated (***Difet***) process. This holds input bias currents to very low levels without sacrificing other important parameters, such as input offset voltage, drift and noise. Laser-trimmed input circuitry yields excellent DC performance. Superior dynamic performance is achieved, yet quiescent current is held to under 2.5mA per amplifier. The OPA2107 is unity-gain stable.

The OPA2107 is available in Plastic DIP, Metal TO-99, and SOIC packages. Industrial and Military temperature range versions are available.



Difet® Burr-Brown Corp.
BIFET® National Semiconductor

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PDS-863

SPECIFICATIONS

T_A = +25°C, V_S = ±15V unless otherwise noted.

		OPA2107AM, SM, AP, AU			OPA2107BM			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OFFSET VOLTAGE[1]								
Input Offset Voltage	V_{CM} = 0V		100	1mV		50	500	µV
Over Specified Temperature			0.5	2		0.2	1	mV
SM Grade			0.8	2.5				mV
Average Drift: Over Specified Temperature			3	10		2	5	µV/°C
Power Supply Rejection	V_S = ±10 to ±18V	80	96		84	100		dB
INPUT BIAS CURRENT[1]								
Input Bias Current	V_{CM} = 0V		4	10		2	5	pA
Over Specified Temperature			0.25	1.5		0.15	1	nA
SM Grade			4	35				nA
Input Offset Current	V_{CM} = 0V		1	8		0.5	3	pA
Over Specified Temperature				1			0.5	nA
SM Grade			1	28				nA
INPUT NOISE								
Voltage: f = 10Hz	(R_S = 0)		30			*		nV/√Hz
f = 100Hz			12			*		nV/√Hz
f = 1kHz			9			*		nV/√Hz
f = 10kHz			8			*		nV/√Hz
BW = 0.1 to 10Hz			1.2			*		µV, p-p
BW = 10 to 10kHz			0.85			*		µV, rms
Current: f = 0.1Hz thru 20kHz			1.2			0.9		fA/√Hz
BW = 0.1Hz to 10Hz			23			17		fA, p-p
INPUT IMPEDANCE								
Differential			10^{13} || 2			*		Ω || pF
Common-Mode			10^{14}|| 4			*		Ω || pF
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±10.5	±11		*	*		V
Over Specified Temperature		±10.2	±10.5		*	*		V
SM Grade		±10	±10.3					V
Common-mode Rejection	V_{CM} = ±10V	80	94		84	96		dB
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±10V, R_L = 2kΩ	82	96		84	100		dB
Over Specified Temperature		80	94		82	96		dB
SM Grade		80	92					dB
DYNAMIC RESPONSE								
Slew Rate	G = +1	15	20		*	*		V/µs
Settling Time: 0.1%	G = –1, 10V Step		1			*		µs
0.01%			1.5			*		µs
Gain-Bandwidth Product	G = 100		5			*		MHz
THD + Noise	G = +1, f = 10kHz		0.001			0.001		%
Channel Separation	f = 100Hz, R_L = 2kΩ		125			125		dB
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±4.5		±18	*		*	V
Current			±4.5	±5		*	*	mA
OUTPUT								
Voltage Output	R_L = 2kΩ	±11	±12		*	*		V
Over Specified Temperature		±10.5	±11.5		*	*		V
SM Grade		±10.2	±11.3					V
Short Circuit Current		±10	±40		*	*		mA
Output Resistance, Open-Loop	1MHz		70			*		Ω
Capacitive Load Stability	G = +1		1000			*		pF
TEMPERATURE RANGE								
Specification								
AP, AU, AM, BM		–25		+85	*		*	°C
SM		–55		+125				°C
Operating								
AP, AU		–25		+85				°C
AM, BM, SM		–55		+125	*		*	°C
Storage								
AP, AU		–40		+125				°C
AM, BM, SM		–65		+150	*		*	°C
Thermal Resistance								
AP			90					°C/W
AU			100					°C/W
AM, BM, SM			125			*		°C/W

* Specifications same as OPA2107AM.

NOTE: (1) Specified with devices fully warmed up.

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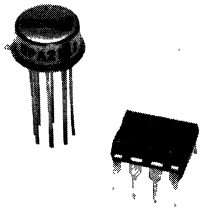


OPA2111

MILITARY & DIE VERSIONS AVAILABLE

Dual Low Noise Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 100% tested: 8nV/$\sqrt{Hz}$ max at 10kHz
- LOW BIAS CURRENT: 4pA max
- LOW OFFSET: 500μV max
- LOW DRIFT: 2.8μV/°C
- HIGH OPEN LOOP GAIN: 114dB min
- HIGH COMMON-MODE REJECTION: 96dB min

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DETECTOR ARRAYS

DESCRIPTION

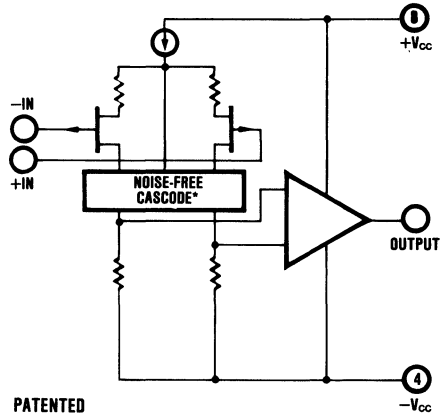
The OPA2111 is a high precision monolithic *Difet* (dielectrically isolated FET) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very-low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very-low offset and drift. Extremely-low noise is achieved with new circuit design techniques (patent pending). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard dual op-amp pin configuration allows upgrading of existing designs to higher performance levels.



OPA2111 SIMPLIFIED CIRCUIT (EACH AMPLIFIER)

BIFET® National Semiconductor Corp , *Difet*® Burr-Brown Corp.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±15VDC and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA2111AM			OPA2111BM			OPA2111SM			OPA2111KM/KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT														
NOISE														
Voltage, f_O = 10Hz	Max: 100% tested		40	80		30	60		40	80		40		nV/√Hz
f_O = 100Hz	Max: 100% tested		15	40		11	30		15	40		15		nV/√Hz
f_O = 1kHz	Max: 100% tested		8	15		7	12		8	15		8		nV/√Hz
f_O = 10kHz	(1)		6	8		6	8		6	8		6		nV/√Hz
f_B = 10Hz to 10kHz	(1)		0.7	1.2		0.6	1.0		0.7	1.2		0 7		µV, rms
f_B = 0.1Hz to 10Hz	(1)		1.6	3.3		1.2	2.5		1.6	3.3		1.6		µV, p-p
Current, f_B = 0 1Hz to 10Hz	(1)		15	24		12	19		15	24		15		fA, p-p
f_O = 0.1Hz to 20kHz	(1)		0.8	1.3		0.6	1.0		0.8	1.0		0.8		fA/√Hz
OFFSET VOLTAGE[2]														
Input Offset Voltage	V_{CM} = 0VDC		±0.1	±0.75		±0.05	±0.5		±0.1	±0.75		±0.3	±2	mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±2	±6		±0.5	±2.8		±2	±6		±8	±15	µV/°C
Match			±1			±0.5			2			2		µV/°C
Supply Rejection		90	110		96	110		90	110		86	110		dB
			±3	±31		±3	±16		±3	±31		±3	±50	µV/V
Channel Separation	100Hz, R_L = 2kΩ		136			136			136			136		dB
BIAS CURRENT[2]														
Initial Bias Current	V_{CM} = 0VDC		±2	±8		±1.2	±4		±2	±8		±3	±15	pA
Match			±1			±0.5			±1			2		pA
OFFSET CURRENT[2]														
Input Offset Current	V_{CM} = 0VDC		±1.2	±6		±0.6	±3		±1.2	±6		±3	±12	pA
IMPEDANCE														
Differential			10^{13} || 1			10^{13} || 1			10^{13} || 1			10^{13} || 1		Ω || pF
Common-Mode			10^{14} || 3			10^{14} || 3			10^{14} || 3			10^{14} || 3		Ω || pF
VOLTAGE RANGE														
Common-Mode Input Range		±10	±11	±10	±11		±10	±11			±10	±11	V	
Common-Mode Rejection	V_{IN} = ±10VDC	90	110		96	110		90	110		82	110		dB
OPEN-LOOP GAIN, DC														
Open-Loop Voltage Gain	$R_L \geq$ 2kΩ	110	125		114	125		110	125		106	125		dB
Match			3			2			3			3		dB
FREQUENCY RESPONSE														
Unity Gain, Small Signal			2			2			2			2		MHz
Full Power Response	20V p-p, R_L = 2kΩ	16	32		16	32		16	32			32		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	1	2		1	2		1	2			2		V/µs
Settling Time, 0.1%	Gain = −1, R_L = 2kΩ		6			6			6			6		µs
0.01%	10V step		10			10			10			10		µs
Overload Recovery, 50% Overdrive[3]	Gain = −1		5			5			5			5		µs
RATED OUTPUT														
Voltage Output	R_L = 2kΩ	±10	±11		±10	±11		±10	±11		±10	±11		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		±5	±10		mA
Output Resistance	DC, open loop		100			100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000			1000		pF
Short Circuit Current		10	40		10	40		10	40		10	40		mA
POWER SUPPLY														
Rated Voltage			±15			±15			±15			±15		VDC
Voltage Range, Derated Performance		±5		±18	±5		±18	±5		±18	±5		±18	VDC
Current, Quiescent	I_O = 0mADC		5	7		5	7		5	7		5	9	mA
TEMPERATURE RANGE														
Specification	Ambient temp.	−25		+85	−25		+85	−55		+125	0		+70	°C
Operating "M" Package	Ambient temp.	−55		+125	−55		+125	−55		+125	−55		+125	°C
"P" Package											−40		+85	°C
Storage "M" Package	Ambient temp.	−65		+150	−65		+150	−65		+150	−65		+150	°C
"P" Package											−40		+85	°C
θ Junction-Ambient			200			200			200			200[4]		°C/W

NOTES: (1) Sample tested—maximum parameters are guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) Typical θ_{J-A} = 150°C/W for plastic DIP.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

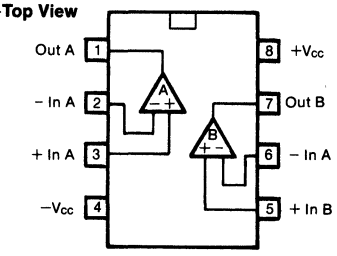
At V_{CC} = ±15VDC and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA2111AM			OPA2111BM			OPA2111SM			OPA2111KM/KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE														
Specification Range	Ambient temp	−25		+85	−25		+85	−55		+125	0		+70	°C
INPUT														
OFFSET VOLTAGE[1]														
Input Offset Voltage	V_{CM} = 0VDC		±0.22	±1.2		±0 08	±0 75		±0.3	±1 5		±0 9	±5	mV
Average Drift			±2	±6		±0 5	±2 8		±2	±6		±8	±15	µV/°C
Match			1			0 5			2			2		µV/°C
Supply Rejection		86	100		90	100		86	100		82	100		dB
			±10	±50		±10	±32		±10	±50		±10	±80	µV/V
BIAS CURRENT[1]														
Initial Bias Current	V_{CM} = 0VDC		±125	±1nA		±75	±500		±2 0nA	±16 3nA		±125	±500	pA
Match			60			30			1nA					pA
OFFSET CURRENT[1]														
Input Offset Current	V_{CM} = 0VDC		±75	±750		±38	±375		±1.3nA	±12nA		±75	±375	pA
VOLTAGE RANGE														
Common-Mode Input Range		±10	±11		±10	±11		±10	±11		±10	±11		V
Common-Mode Rejection	V_{IN} = ±10VDC	86	100		90	100		86	100		80	100		dB
OPEN-LOOP GAIN, DC														
Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	106	120		110	120		106	120		100	120		dB
Match			5			3			5			5		dB
RATED OUTPUT														
Voltage Output	R_L = 2kΩ	±10 5	±11		±10.5	±11		±10 5	±11		±10 5	±11		V
Current Output	V_O = ±10VDC	±5	±10		±5	±10		±5	±10		±5	±10		mA
Short Circuit Current	V_O = 0VDC	10	40		10	40		10	40		10	40		mA
POWER SUPPLY														
Current, Quiescent	I_O = 0mADC		5	8		5	8		5	8		5	10	mA

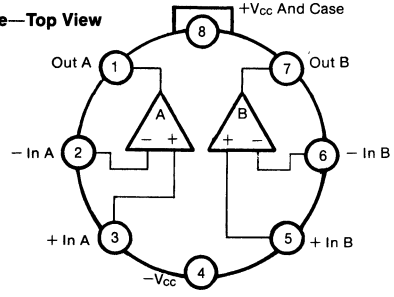
NOTES (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up

CONNECTION DIAGRAMS

'P' Package—Top View



'M' Package—Top View



ORDERING INFORMATION

Model	Package	Temperature Range	Offset Voltage, max (mV)
OPA2111AM	TO-99	−25°C to +85°C	±0.75
OPA2111BM	TO-99	−25°C to +85°C	±0.5
OPA2111KM	TO-99	0°C to +70°C	±2.0
OPA2111SM	TO-99	−55°C to +125°C	±0.75
OPA2111KP	Plastic	0°C to +70°C	±2.0

BURN-IN SCREENING OPTION

Model	Package	Temperature Range	Burn-In Temp. (160h)[1]
OPA2111AM-BI	TO-99	−25°C to +85°C	+125°C
OPA2111BM-BI	TO-99	−25°C to +85°C	+125°C
OPA2111KM-BI	TO-99	0°C to +70°C	+125°C
OPA2111SM-BI	TO-99	−55°C to +125°C	+125°C
OPA2111KP-BI	Plastic	0°C to +70°C	+85°C

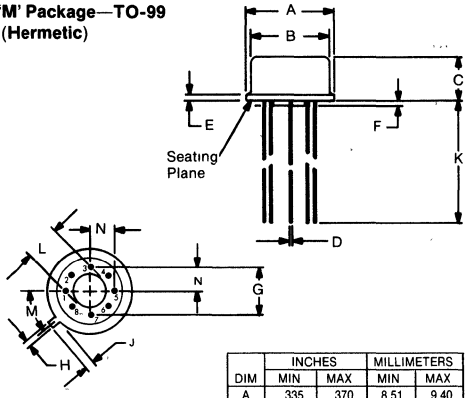
NOTE: (1) Or equivalent combination of time and temperature.

ABSOLUTE MAXIMUM RATINGS

Supply ..... ±18VDC
Internal Power Dissipation ($T_J \leq +175°C$) 500mW
Differential Input Voltage ..... Total V_{CC}
Input Voltage Range ..... $\pm V_{CC}$
Storage Temperature Range: "M" Package..... −65°C to +150°C
"P" Package ..... −40°C to +85°C
Operating Temperature Range: "M" Package ..... −55°C to +125°C
"P" Package ..... −40°C to +85°C
Lead Temperature (soldering, 10s) ..... +300°C
Output Short Circuit to ground (+25°C) ..... Continuous
Junction Temperature ..... +175°C

MECHANICAL

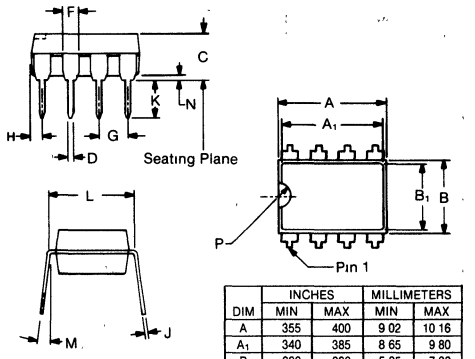
'M' Package—TO-99 (Hermetic)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	335	370	8 51	9 40
B	305	335	7 75	8 51
C	165	185	4 19	4 70
D	016	021	0 41	0 53
E	010	040	0 25	1 02
F	010	040	0 25	1 02
G	200 BASIC		5 08 BASIC	
H	028	034	0 71	0 86
J	029	045	0 74	1 14
K	500	—	12 7	—
L	110	160	2 79	4 06
M	45° BASIC		45° BASIC	
N	095	105	2 41	2 67

NOTE Leads in true position within 0 01" (0 25mm) R at MMC at seating plane Pin numbers shown for reference only Numbers may not be marked on package Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3 2)

'P' Package—Plastic DIP



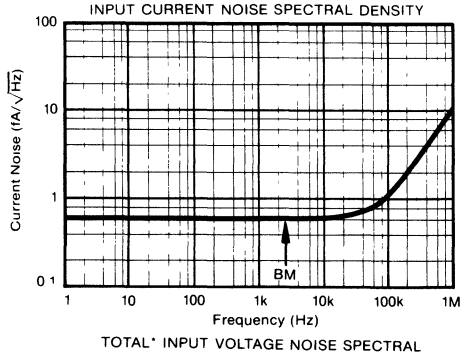
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	355	400	9 02	10 16
A_1	340	385	8 65	9 80
B	230	290	5 85	7 38
B_1	200	250	5 09	6 36
C	120	200	3 05	5 09
D	015	023	0 38	0 59
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	025	050	0 64	1 27
J	008	015	0 20	0 38
K	070	150	1 78	3 82
L	300 BASIC		7 63 BASIC	
M	0°	15°	0°	15°
N	010	030	0 25	0 76
P	025	050	0 64	1 27

NOTE Leads in true position within 0 01" (0 25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package. Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3 2)

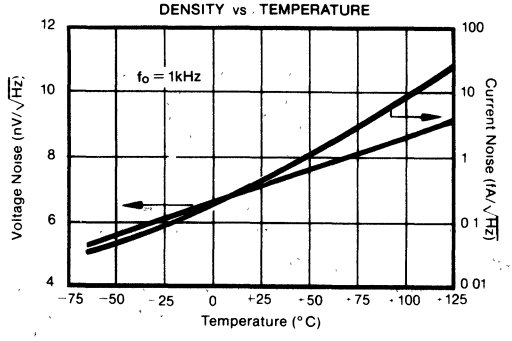
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_{CC} = \pm 15VDC$ unless otherwise noted.

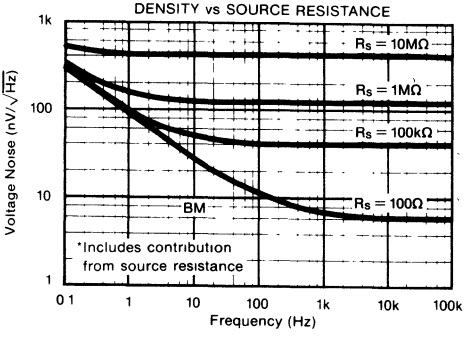
INPUT CURRENT NOISE SPECTRAL DENSITY



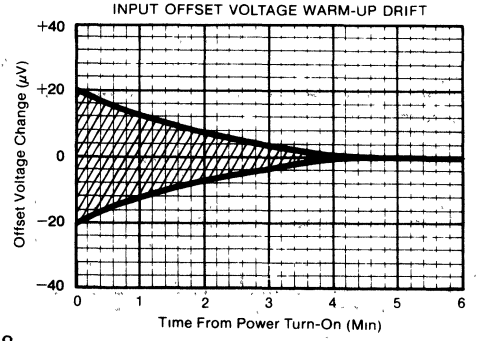
VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



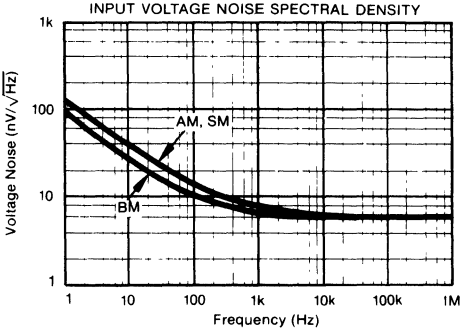
TOTAL* INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



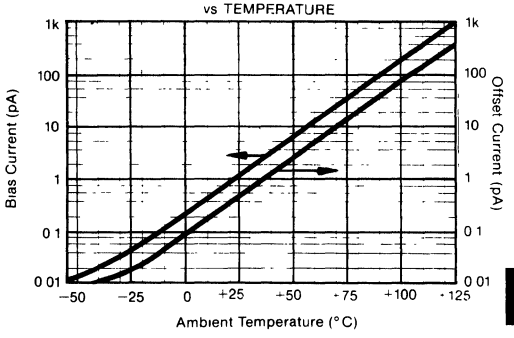
INPUT OFFSET VOLTAGE WARM-UP DRIFT



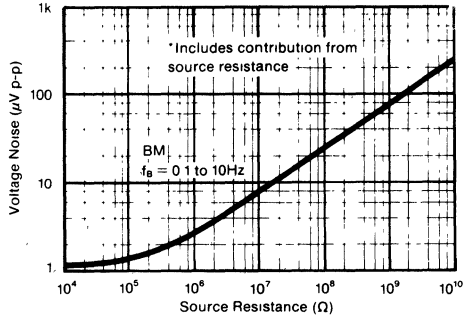
INPUT VOLTAGE NOISE SPECTRAL DENSITY



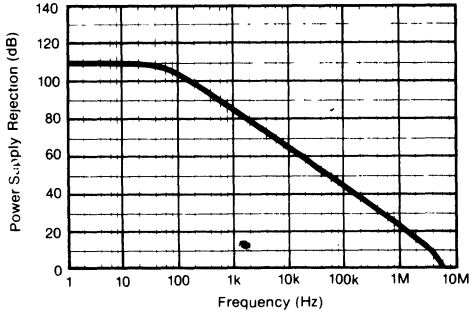
BIAS AND OFFSET CURRENT vs TEMPERATURE



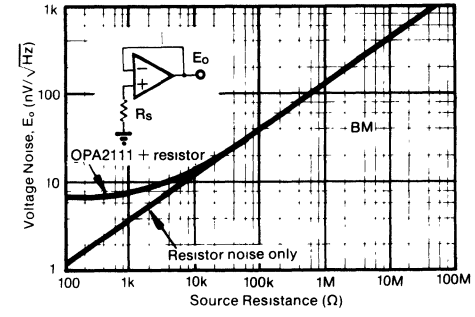
TOTAL* INPUT VOLTAGE NOISE (PEAK-TO-PEAK) vs SOURCE RESISTANCE



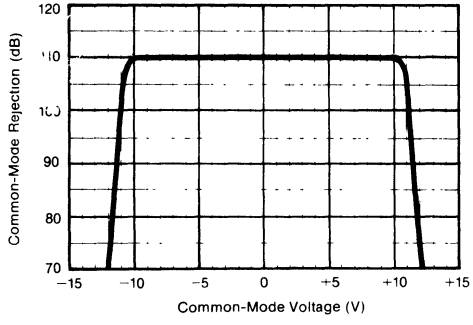
POWER SUPPLY REJECTION vs FREQUENCY



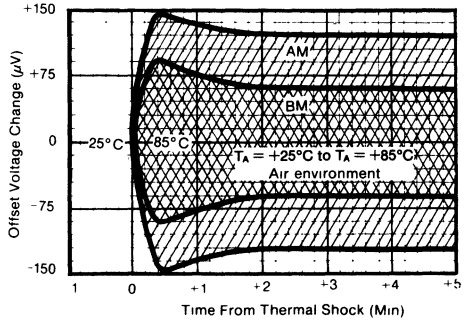
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



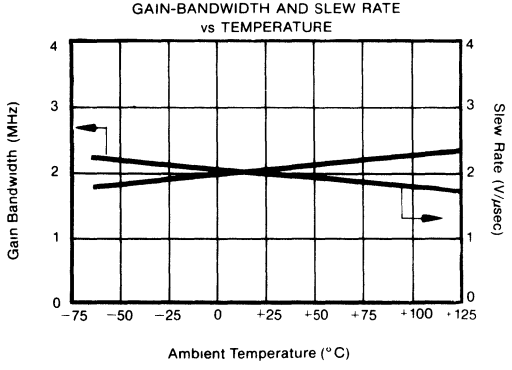
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



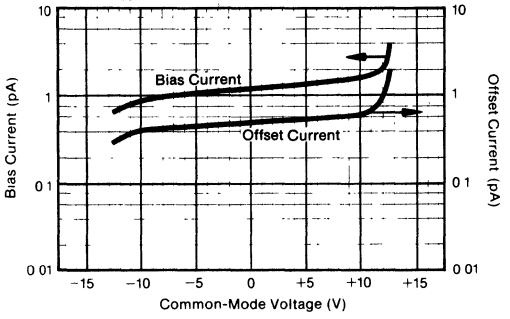
INPUT OFFSET VOLTAGE CHANGE DUE THERMAL SHOCK



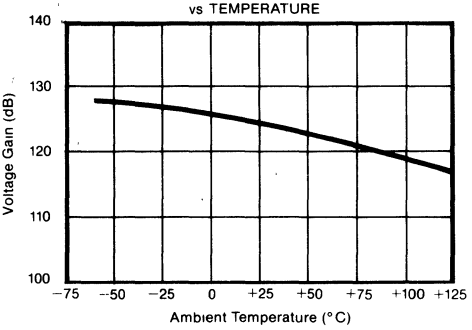
GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



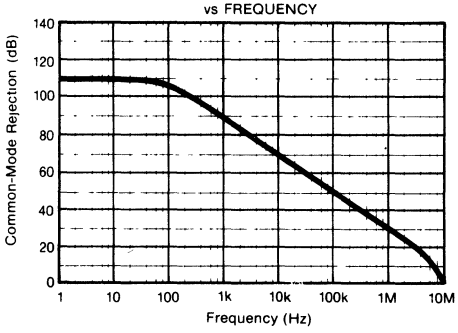
BIAS AND OFFSET CURRENT
vs INPUT COMMON MODE VOLTAGE



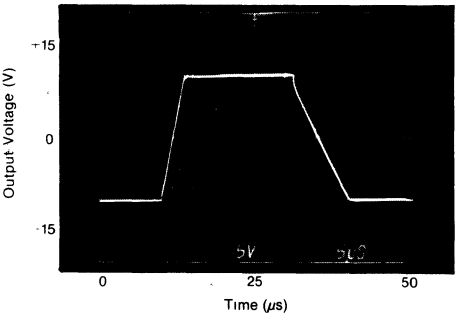
OPEN-LOOP GAIN
vs TEMPERATURE



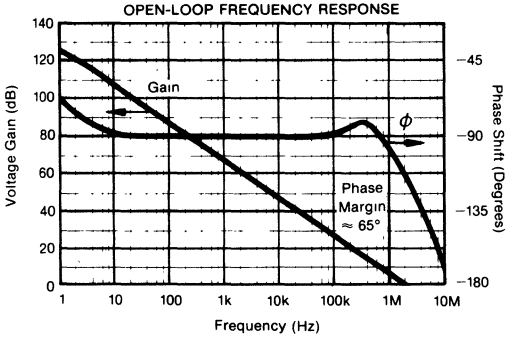
COMMON-MODE REJECTION
vs FREQUENCY



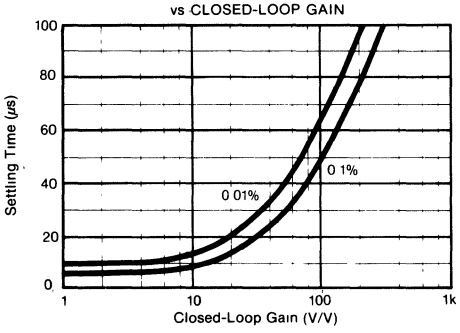
LARGE SIGNAL TRANSIENT RESPONSE



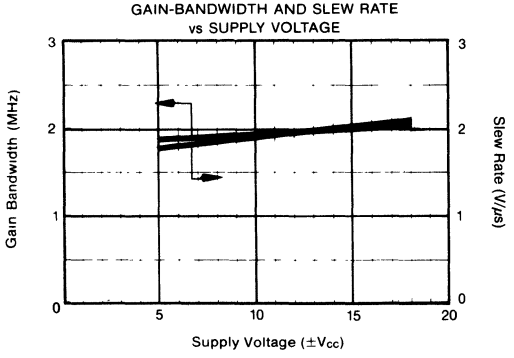
OPEN-LOOP FREQUENCY RESPONSE



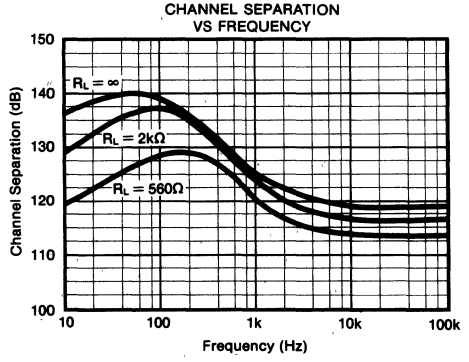
SETTLING TIME
vs CLOSED-LOOP GAIN

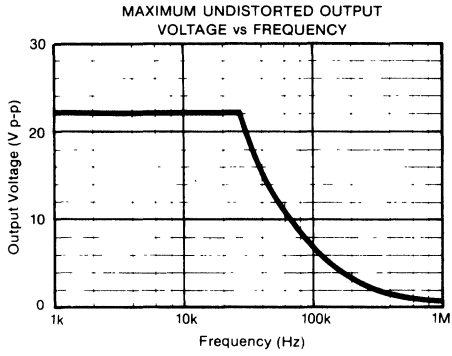


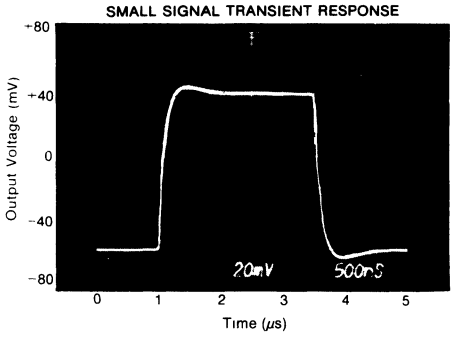
GAIN-BANDWIDTH AND SLEW RATE
vs SUPPLY VOLTAGE

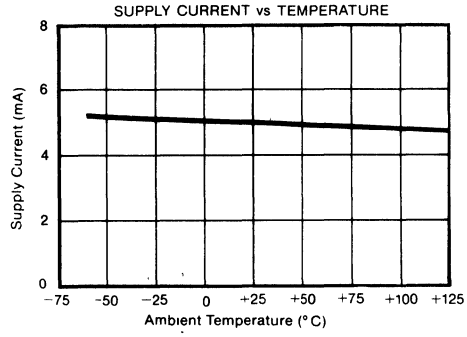


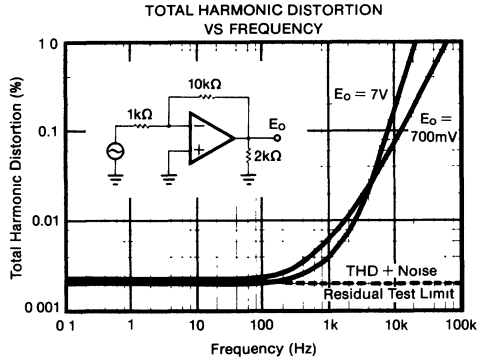
CHANNEL SEPARATION
VS FREQUENCY











APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA2111 offset voltage is laser-trimmed and will require no further trim for most applications.

Offset voltage can be trimmed by summing (see Figure 1). With this trim method there will be no degradation of input offset drift.

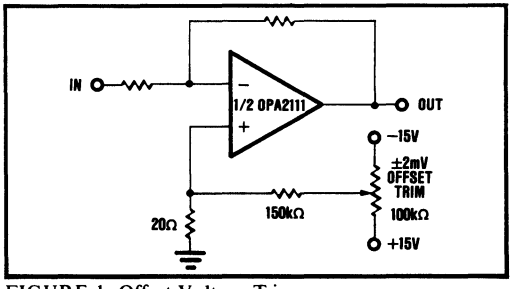


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET® amplifiers can be destroyed by the loss of $-V_{CC}$.

Because of its dielectric isolation, no special protection is needed on the OPA2111. Of course, the differential and common-mode voltage limits should be observed.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA2111. To avoid leakage problems, it is recommended that the signal input lead of the OPA2111 be wired to a Teflon standoff. If the OPA2111 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 2).

NOISE: FET VERSUS BIPOLAR

Low noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the low voltage noise of a bipolar operational amplifier is superior, but at higher impedances

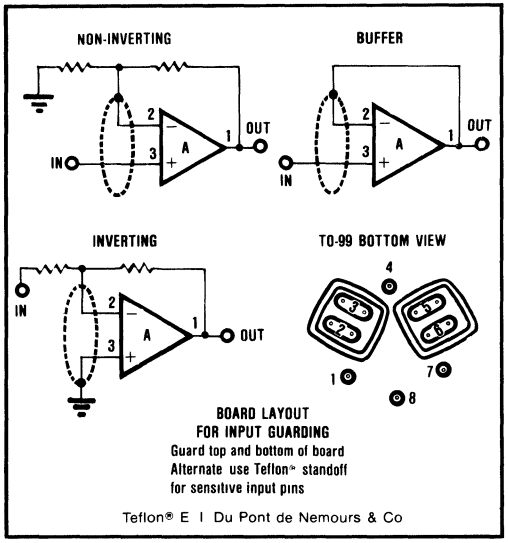


FIGURE 2. Connection of Input Guard.

the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ the OPA2111 will have lower total noise than an OP-27 (see Figure 3).

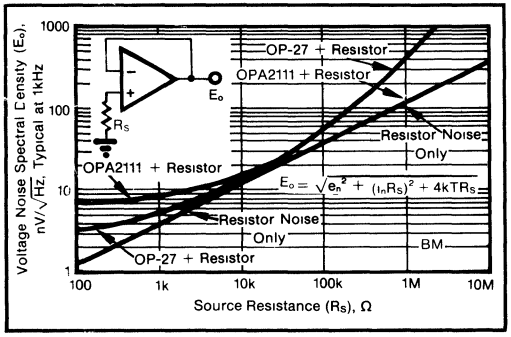


FIGURE 3. Voltage Noise Spectral Density Versus Source Resistance.

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET® operational amplifiers are affected by common-mode voltage (Figure 4). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely-low bias current of the OPA2111 is not compromised by common-mode voltage.

BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information table. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

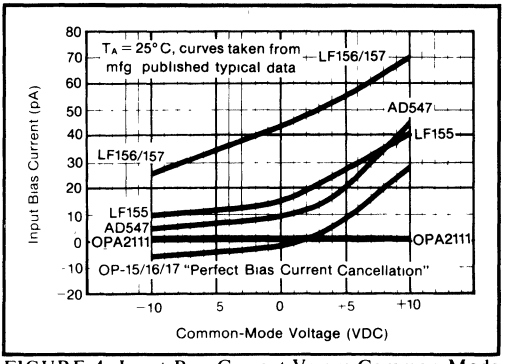


FIGURE 4. Input Bias Current Versus Common-Mode Voltage.

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

APPLICATIONS CIRCUITS

Figures 5 through 13 are circuit diagrams of various applications for the OPA2111.

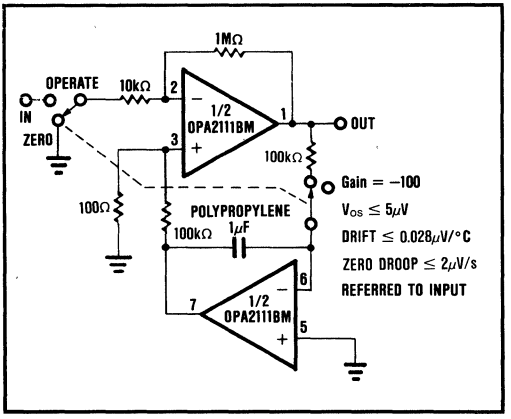


FIGURE 5. Auto-Zero Amplifier.

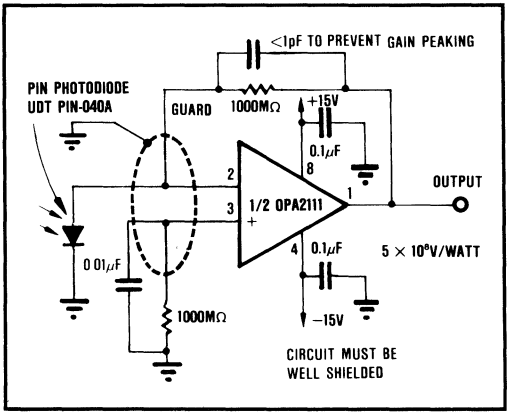


FIGURE 6. Sensitive Photodiode Amplifier.

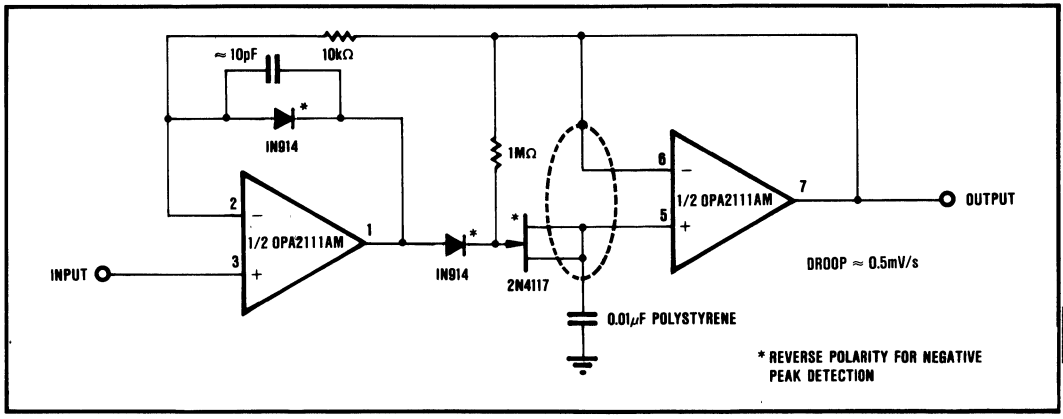


FIGURE 7. Low-Droop Positive Peak Detector.

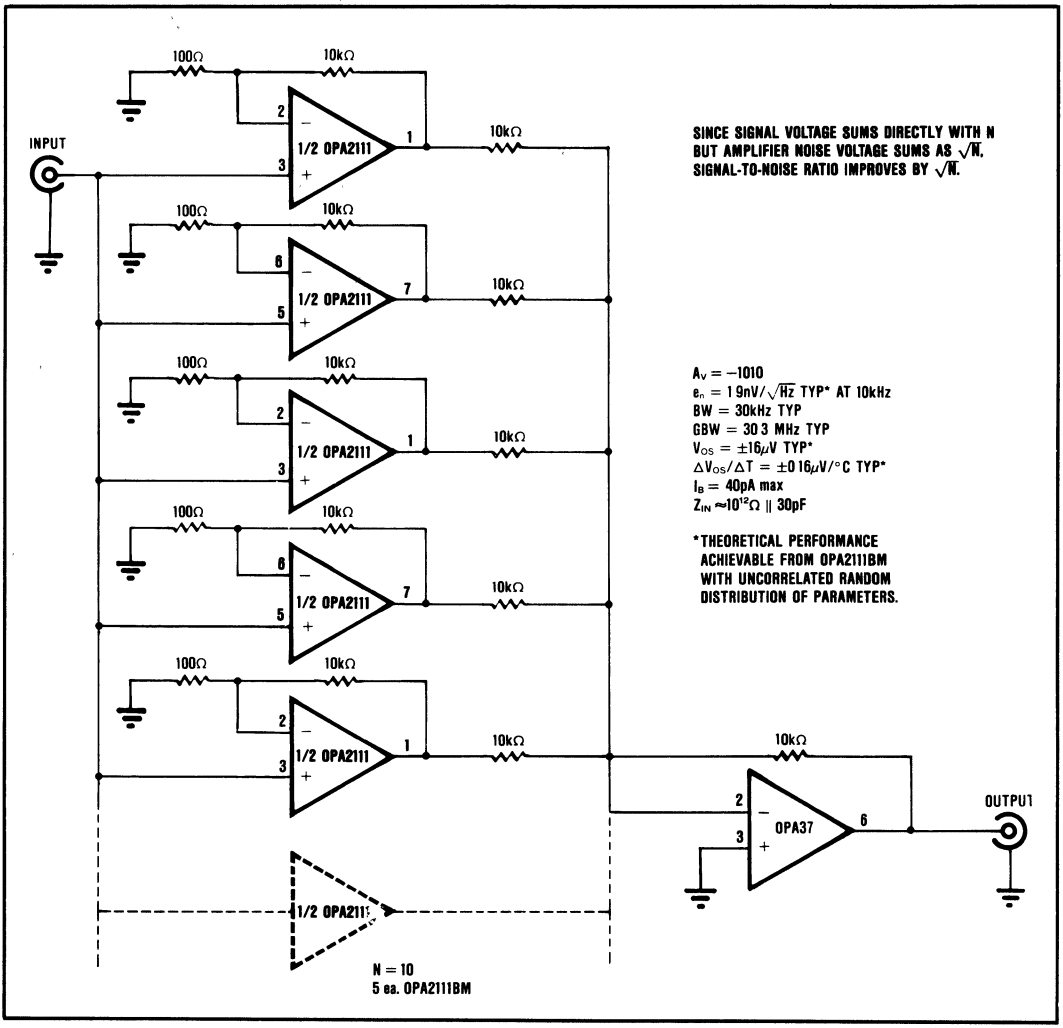


FIGURE 8. 'N' Stage Parallel-Input Amplifier.

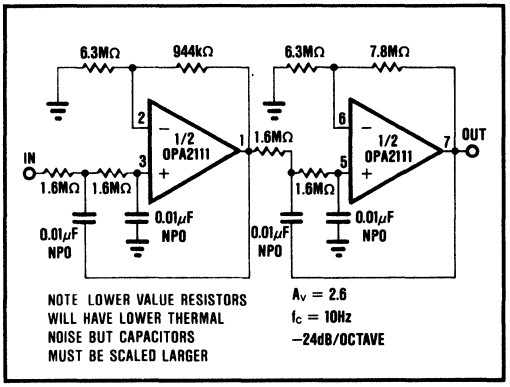


FIGURE 9. 10Hz Fourth-Order Butterworth Low-Pass Filter.

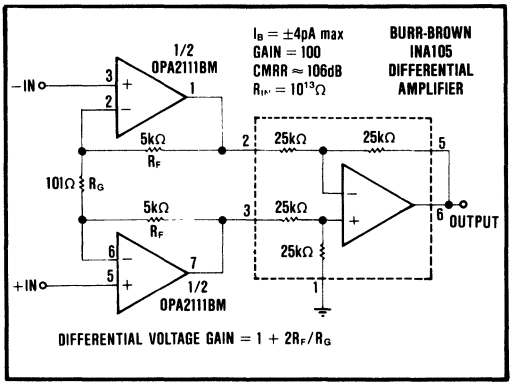


FIGURE 10. FET Input Instrumentation Amplifier.

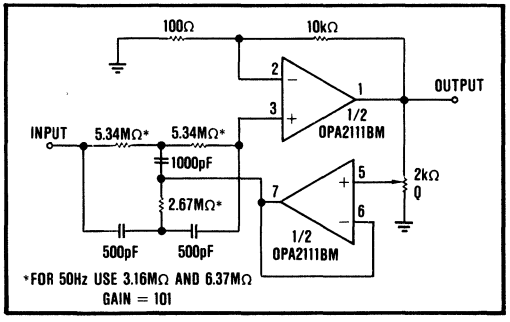


FIGURE 11. High-Impedance 60Hz Reject Filter with Gain.

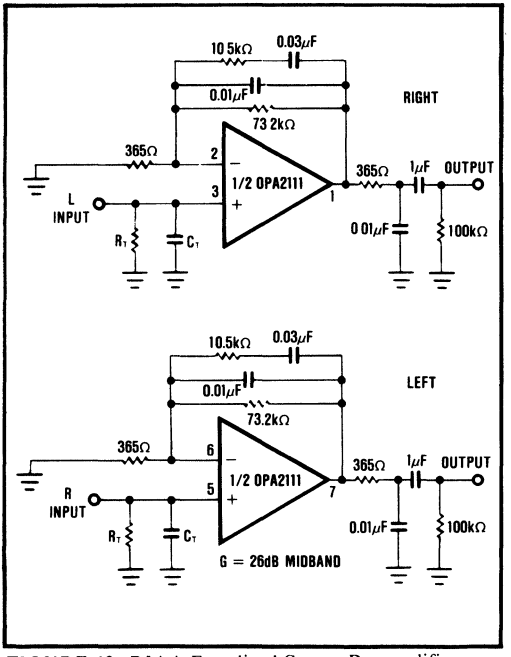
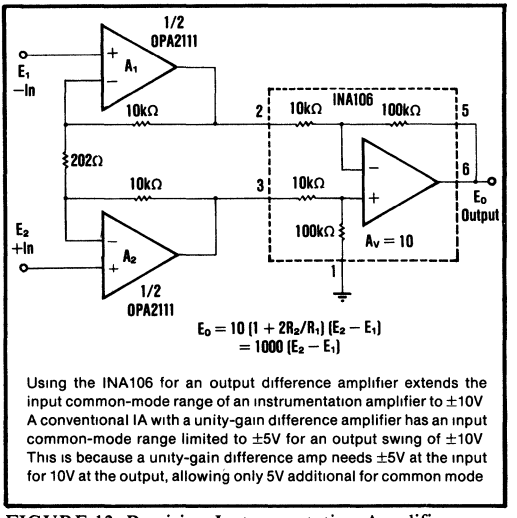


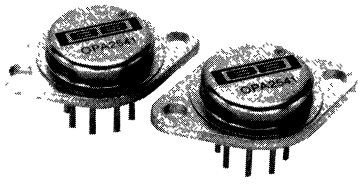
FIGURE 12. RIAA Equalized Stereo Preamplifier.



Using the INA106 for an output difference amplifier extends the input common-mode range of an instrumentation amplifier to ±10V. A conventional IA with a unity-gain difference amplifier has an input common-mode range limited to ±5V for an output swing of ±10V. This is because a unity-gain difference amp needs ±5V at the input for 10V at the output, allowing only 5V additional for common mode.

FIGURE 13. Precision Instrumentation Amplifier.

BURR-BROWN®



OPA2541

MILITARY VERSION AVAILABLE

Dual High Power OPERATIONAL AMPLIFIER

FEATURES

- OUTPUT CURRENTS TO 5A
- POWER SUPPLIES TO ±40V
- FET INPUT
- ELECTRICALLY ISOLATED CASE

APPLICATIONS

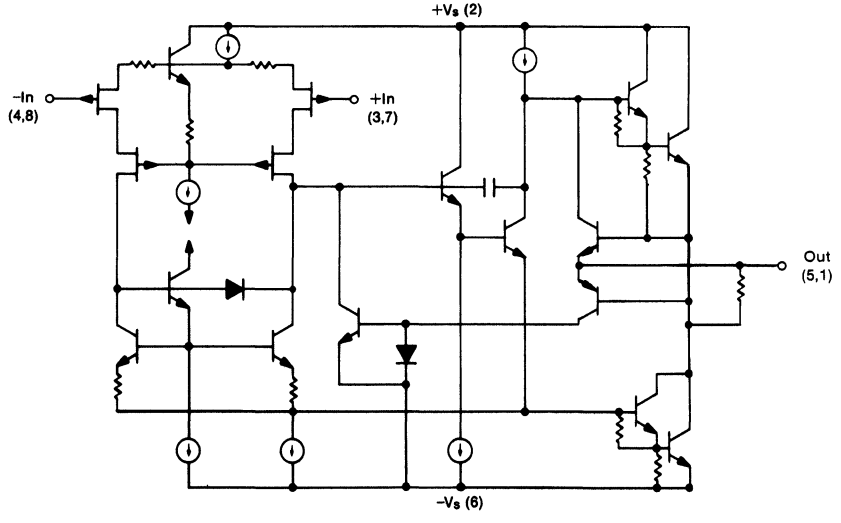
- MOTOR DRIVER
- SERVO AMPLIFIER
- SYNCHRO/RESOLVER EXCITATION
- VOICE COIL DRIVER
- BRIDGE AMPLIFIER
- PROGRAMMABLE POWER SUPPLY
- AUDIO AMPLIFIER

DESCRIPTION

The OPA2541 is a dual power operational amplifier capable of operation from power supplies up to ±40V and output currents of 5A continuous. With two monolithic power amplifiers in a single package it provides unequaled functional density.

The industry-standard 8-pin TO-3 package is isolated from all internal circuitry allowing it to be mounted directly to a heat sink without insulators which degrade thermal performance. Internal circuitry limits output current to approximately 6A.

The OPA2541 is available in both industrial and military temperature range versions. Enhanced reliability screening is also available.



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PDS-768A

SPECIFICATIONS

ELECTRICAL

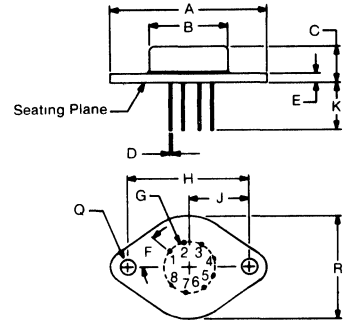
At T_C = +25°C and V_S = ±35VDC unless otherwise noted

PARAMETER	CONDITIONS	OPA2541AM MIN	OPA2541AM TYP	OPA2541AM MAX	OPA2541BM/SM MIN	OPA2541BM/SM TYP	OPA2541BM/SM MAX	UNITS
INPUT OFFSET VOLTAGE								
V_{OS}			±2	±10		±0.25	±1	mV
vs Temperature	Specified temperature range		±20	±40		±15	±30	µV/°C
vs Supply Voltage	V_S = ±10V to ±V_{MAX}		±2 5	±10		*	*	µV/V
vs Power			±20	±60		*	*	µV/W
INPUT BIAS CURRENT								
I_B			15	50		*	*	pA
	Specified temperature range		Note 1			*		
INPUT OFFSET CURRENT								
I_{OS}			±5	±30		*	*	pA
	Specified temperature range		Note 1			*		
INPUT CHARACTERISTICS								
Common-Mode Voltage Range	Specified temperature range	±(|V_S|−6)	±(|V_S|−3)		*	*		V
Common-Mode Rejection	V_{CM} = (|±V_S|−6V)	95	106		*	*		dB
Input Capacitance			5			*		pF
Input Impedance, DC			1			*		$10^{12}\Omega$
GAIN CHARACTERISTICS								
Open Loop Gain at 10Hz	R_L = 6Ω	90	96		*	*		dB
Gain-Bandwidth Product			1 6			*		MHz
OUTPUT								
Voltage Swing	I_O = 5A	±(|V_S|−5 5)	±(|V_S|−4 5)		*	*		V
	I_O = 2A	±(|V_S|−4.5)	±(|V_S|−3 6)		*	*		V
	I_O = 0 5A	±(|V_S|−4)	±(|V_S|−3 2)		*	*		V
Current, Continuous	+25°C	5	7.0		*	*		A
	+85°C	4	5.0		*			A
	+125°C (SM grade only)				3	3.5		A
AC PERFORMANCE								
Slew Rate		6	8		*	*		V/µs
Power Bandwidth	R_L = 8Ω, V_O = 20Vrms	45	55		*	*		kHz
Settling Time to 0 1%	2V Step		2			*		µs
Capacitive Load	Specified temperature range, G = 1			3.3			*	nF
	Specified temperature range, G > 10			SOA			*	
Phase Margin	Specified temperature range, R_L = 8Ω		40			*		Degrees
Channel Separation	1kHz, R_L = 6Ω		80			*		dB
POWER SUPPLY								
Power Supply Voltage, ±V_S	Specified temperature range	±10	±30	±35	*	±35	±40	V
Current, Quiescent	Total—both amplifiers		40	50		*	*	mA
THERMAL RESISTANCE								
θ_{JC}, (junction to case)	Both amplifiers[2], AC output f > 60Hz		0.8	1.0		*	*	°C/W
θ_{JC}	Both amplifiers[2], DC output		0.9	1 2		*	*	°C/W
θ_{JC}	One amplifier, AC output f > 60Hz		1.25	1 5		*	*	°C/W
θ_{JC}	One amplifier, DC output		1 4	1.9		*	*	°C/W
θ_{JA}, (junction to ambient)	No heat sink		30			*		°C/W
TEMPERATURE RANGE								
Case	AM, BM	−25		+85	*		*	°C
	SM				−55		+125	°C

*Specification same as OPA541AM

NOTES. (1) Input bias and offset current approximately doubles for every 10°C increase in temperature. (2) Assumes equal dissipation in both amplifiers

MECHANICAL



NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers may not be marked on package

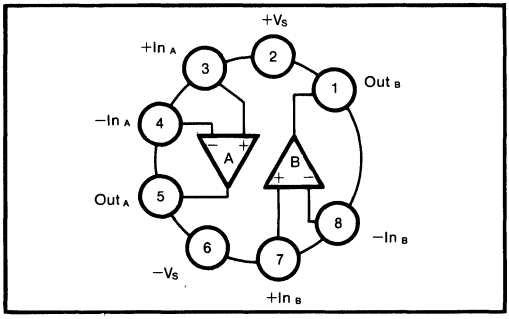
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 510	1 550	38 35	39 37
B	745	770	18 92	19 56
C	260	300	6 60	7 62
D	038	042	0 97	1 07
E	080	105	2 03	2 67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12 7 BASIC	
H	1 186 BASIC		30 12 BASIC	
J	593 BASIC		15 06 BASIC	
K	400	500	10 16	12 70
Q	151	161	3 84	4 09
R	980	1 020	24 89	25 91

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$	80V
Output Current	see SOA
Power Dissipation, Internal[1]	125W
Input Voltage. Differential	$\pm V_S$
Common-mode	$\pm V_S$
Temperature: Pin solder, 10s	+300°C
Junction[1]	+150°C
Temperature Range	
Storage	−65°C to +150°C
Operating (case)	−55°C to +125°C

NOTE (1) Long term operation at the maximum junction temperature will result in reduced product life Derate internal power dissipation to achieve high MTTF

CONNECTION DIAGRAM



ORDERING INFORMATION

Model	Package	Temperature Range	Current Continuous
OPA2541AM	TO-3	-25°C to +85°C	5A at 25°C
OPA2541BM	TO-3	-25°C to +85°C	4A at 25°C
OPA2541SM	TO-3	-55°C to +125°C	3A at 25°C

BURN-IN SCREENING OPTION

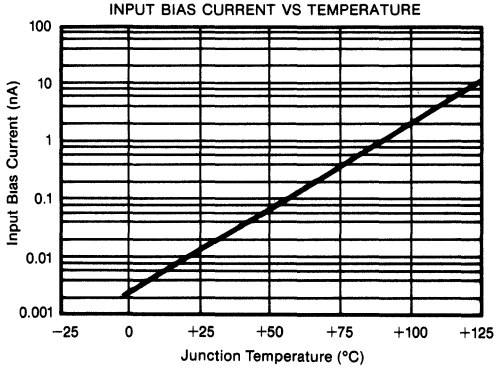
Model	Package	Temperature Range	Burn-In Temp. (160h)[1]
OPA2541AM-BI	TO-3	-25°C to +85°C	+85°C
OPA2541BM-BI	TO-3	-25°C to +85°C	+85°C
OPA2541SM-BI	TO-3	-55°C to +125°C	+125°C

NOTE. (1) Or equivalent combination of time and temperature (2) Minimum order is 25 pieces

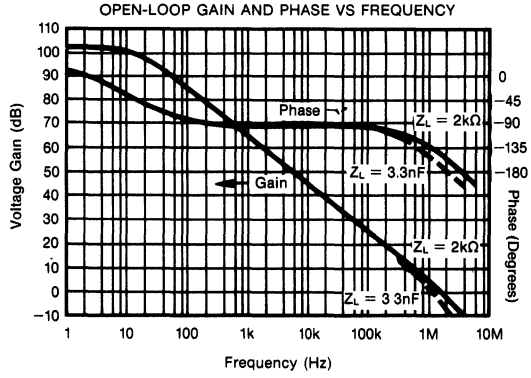
TYPICAL PERFORMANCE CURVES

$T_A = +25°C$, $V_S = \pm 35VDC$ unless otherwise noted

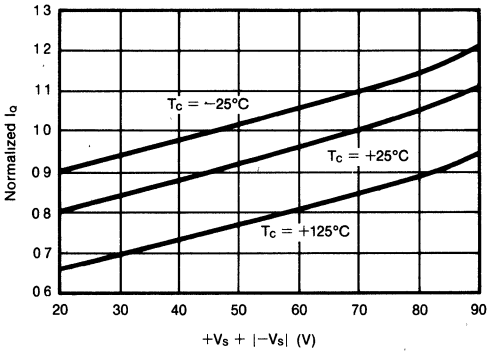
INPUT BIAS CURRENT VS TEMPERATURE



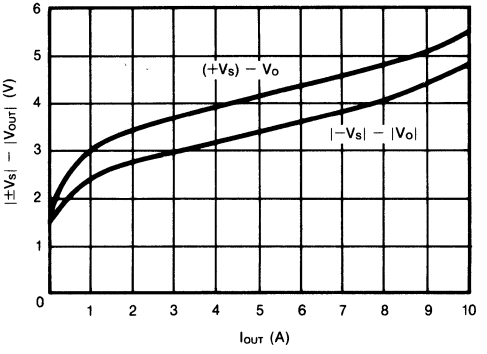
OPEN-LOOP GAIN AND PHASE VS FREQUENCY



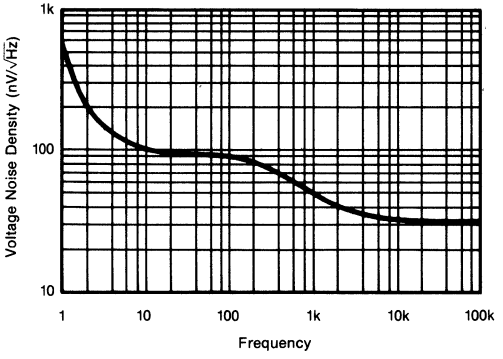
NORMALIZED QUIESCENT CURRENT
VS TOTAL POWER SUPPLY VOLTAGE



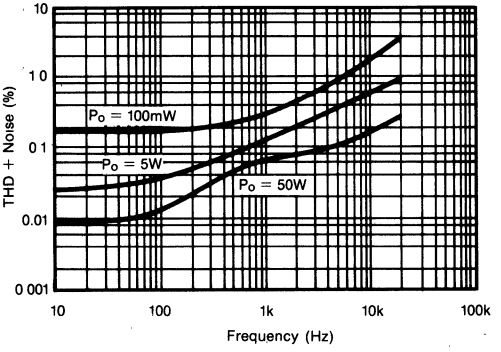
OUTPUT VOLTAGE SWING
VS OUTPUT CURRENT



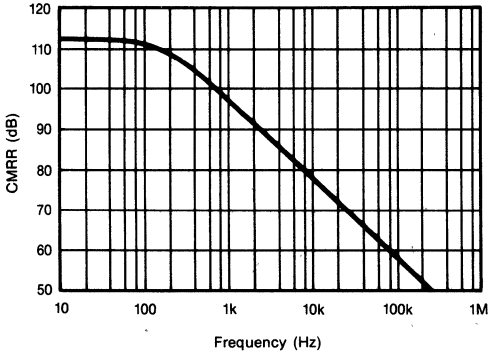
VOLTAGE NOISE DENSITY VS FREQUENCY



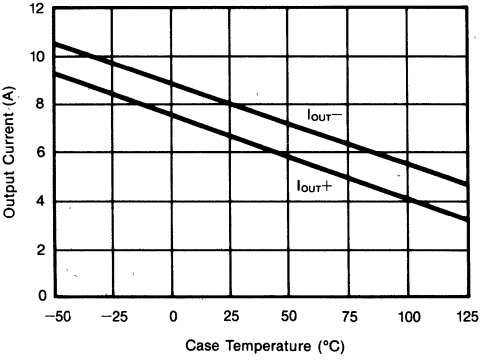
TOTAL HARMONIC DISTORTION VS FREQUENCY



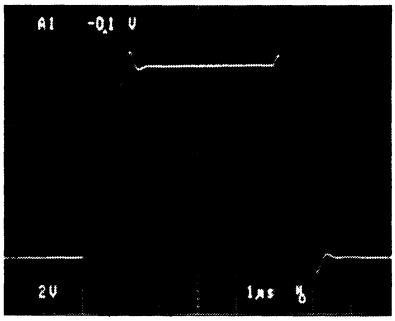
COMMON-MODE REJECTION VS FREQUENCY



OUTPUT CURRENT VS TEMPERATURE

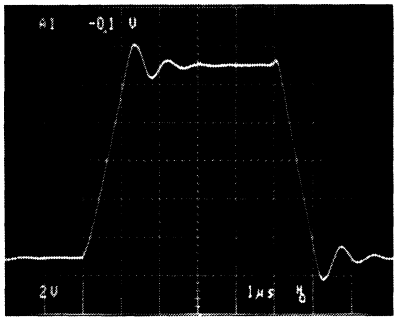


DYNAMIC RESPONSE



$Z_{LOAD} = \infty$, $V_S = \pm 35V$, $A_V = +1$

DYNAMIC RESPONSE



$Z_{LOAD} = 4700pF$, $V_S = \pm 35$, $A_V = +1$

INSTALLATION INSTRUCTIONS

POWER SUPPLIES

The OPA2541 is specified for operation from power supplies up to ±40V. It can also be operated from an unbalanced or a single power supply so long as the total power supply voltage does not exceed 80V (70V for "AM" grade). The power supplies should be bypassed with low series impedance capacitors such as ceramic or tantalum. These should be located as near as practical to the amplifier's power supply pins. Good power amplifier circuit layout is, in general, like good high-frequency layout. Consider the path of large power supply and output currents. Avoid routing these connections near low-level input circuitry to avoid waveform distortion and instability.

Signal dependent load current can modulate the power supply voltage with inadequate power supply bypassing. This can affect both amplifiers' outputs. Since the second amplifier's signal may not be related to the first, this will degrade the inherent channel separation of the OPA2541.

HEAT SINKING

Most applications will require a heat sink to prevent junction temperatures from exceeding the 150°C maximum rating. The type of heat sink required will depend on the output signals, power dissipation of each amplifier, and ambient temperature. The thermal resistance from junction to case, θ_{JC}, depends on how the power dissipation is distributed on the amplifier die.

DC output concentrates the power dissipation in one output transistor. AC output distributes the power dissipation equally between the two output transistors and therefore has lower thermal resistance. Similarly, the power dissipation may be all in one amplifier (worst case) or equally distributed between the two amplifiers (best case). Thermal resistances are provided for each of these possibilities. The case-to-junction temperature rise is the product of the power dissipation (total of both amplifiers) times the appropriate thermal resistance—

$$\Delta T_{JC} = (P_D \text{ total}) (\theta_{JC}).$$

Sufficient heat sinking must be provided to keep the case temperature within safe limits for the maximum ambient temperature and power dissipation. The thermal resistance of the heat sink required may be calculated by:

$$\theta_{HS} = 150°C - \Delta T_{JC} - T_A / P_D \text{ total}$$

Commercially available heat sinks usually specify thermal resistance. These ratings are often suspect, however, since they depend greatly on the mounting environment and air flow conditions. Actual thermal performance should be verified by measurement of case temperature under the required load and environmental conditions.

No insulating hardware is required when using the OPA2541. Since mica and other similar insulators typically add 0.7°C/W thermal resistance, this is a significant advantage. See Burr-Brown Application Note AN-83 for further details on heat sinking.

SAFE OPERATING AREA

The Safe Operating Area (SOA) curve provides comprehensive information on the power handling abilities of the OPA2541. It shows the allowable output current as a function of the voltage across the conducting output transistor (see Figure 1). This voltage is equal to the power supply voltage minus the output voltage. For example, as the amplifier output swings near the positive power supply voltage, the voltage across the output transistor decreases and the device can safely provide large output currents demanded by the load.

The internal current limit will not provide short-circuit protection in most applications. When the amplifier output is shorted to ground, the full power supply voltage is impressed across the conducting output transistor. For instance, with $V_S = \pm 35V$, a short circuit to ground would impress 35V across the conducting power transistor. The maximum safe output current at this voltage is 1.8A, so the internal current limit would not protect the amplifier. The unit-to-unit variation and temperature dependence of the internal current limit suggest that it be used to handle abnormal conditions and not activated in commonly encounted circuit operation.

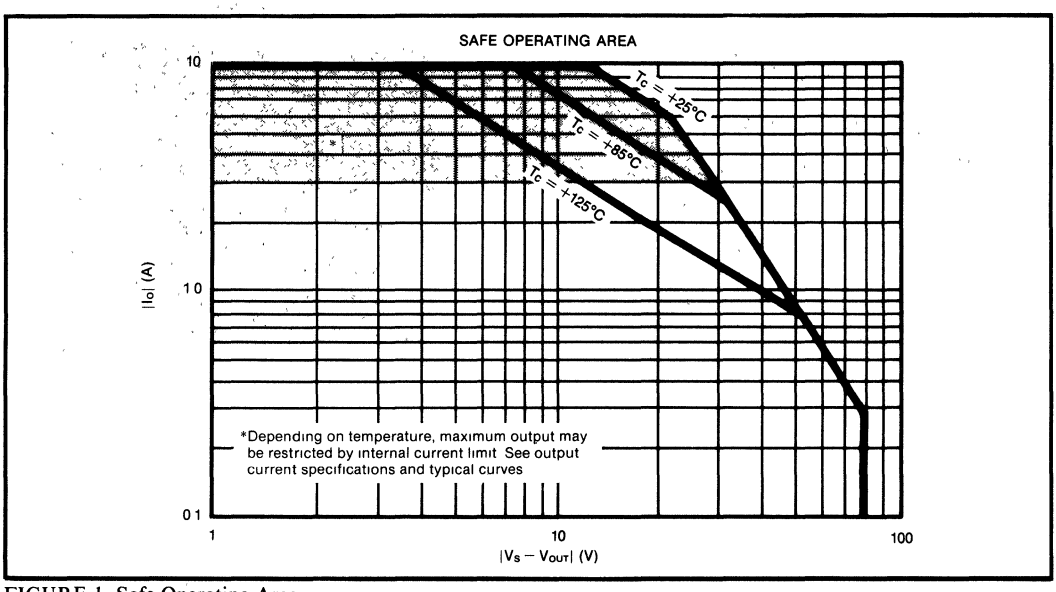


FIGURE 1. Safe Operating Area.

Reactive, or EMF generating loads such as DC motors can present demanding SOA requirements. With a purely reactive load, output voltage current occurs when the output voltage is zero and the voltage across the conducting transistor is equal to the full power supply voltage. See Burr-Brown Application Note AN-123 for further information on evaluating SOA.

Applications with inductive or EMF-generating loads which can produce "kick back" voltage surges to the amplifiers should include clamp diodes from the output terminals to the power supplies. These diodes should be chosen to limit the peak amplifier output voltage surges to less than 2V beyond the power supply rail voltage. Common 1A rated rectifier diodes will suffice in most applications.

BURN-IN SCREENING

Burn-in screening is an option available for the products listed in the Ordering Information table. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

APPLICATIONS CIRCUITS

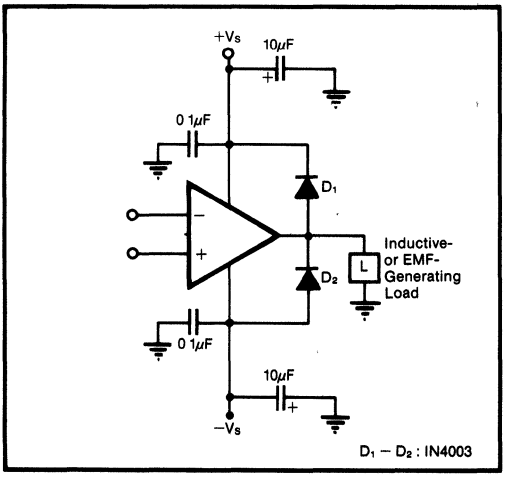


FIGURE 2. Clamping Output for EMF-Generating Loads.

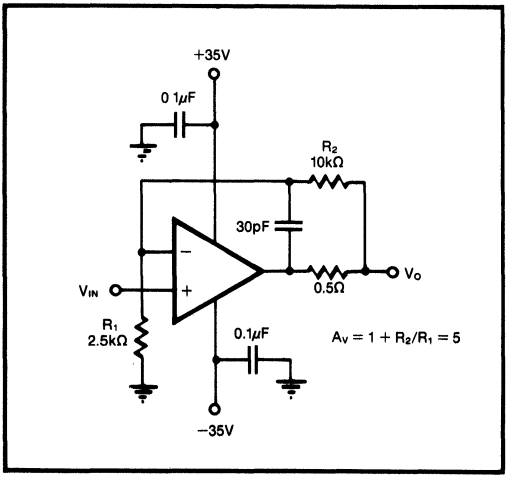


FIGURE 3. Isolating Capacitive Loads.

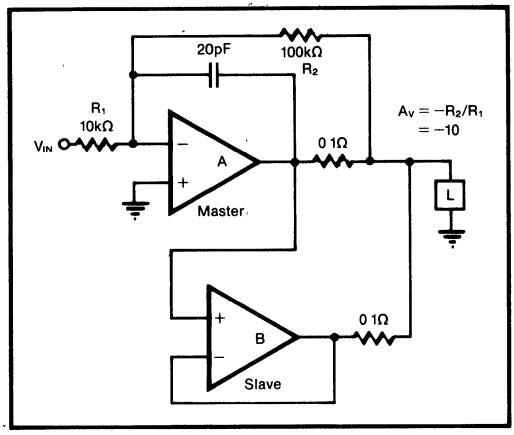


FIGURE 4. Paralleled Operation, Extended SOA.

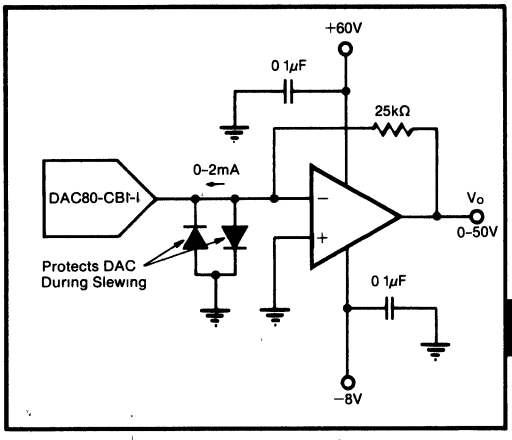


FIGURE 5. Programmable Voltage Source.

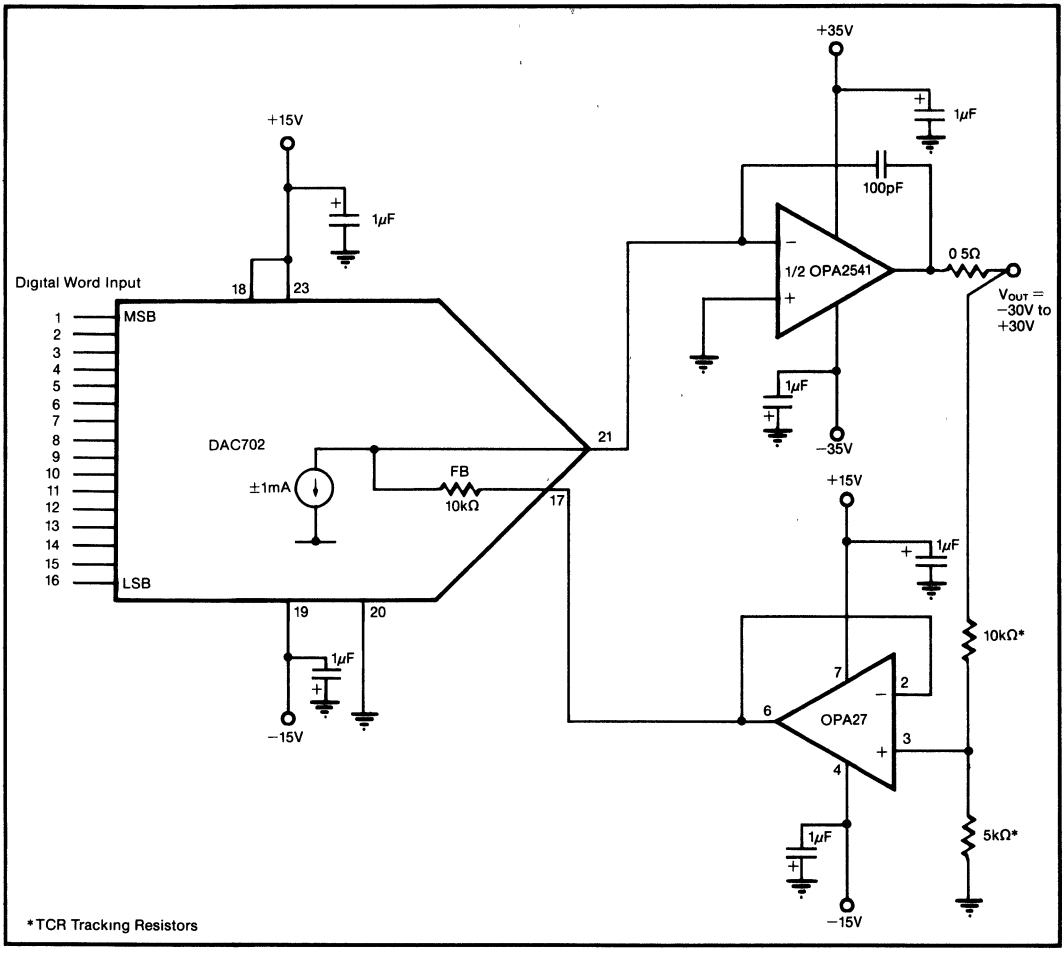


FIGURE 6. 16-Bit Programmable Voltage Source.

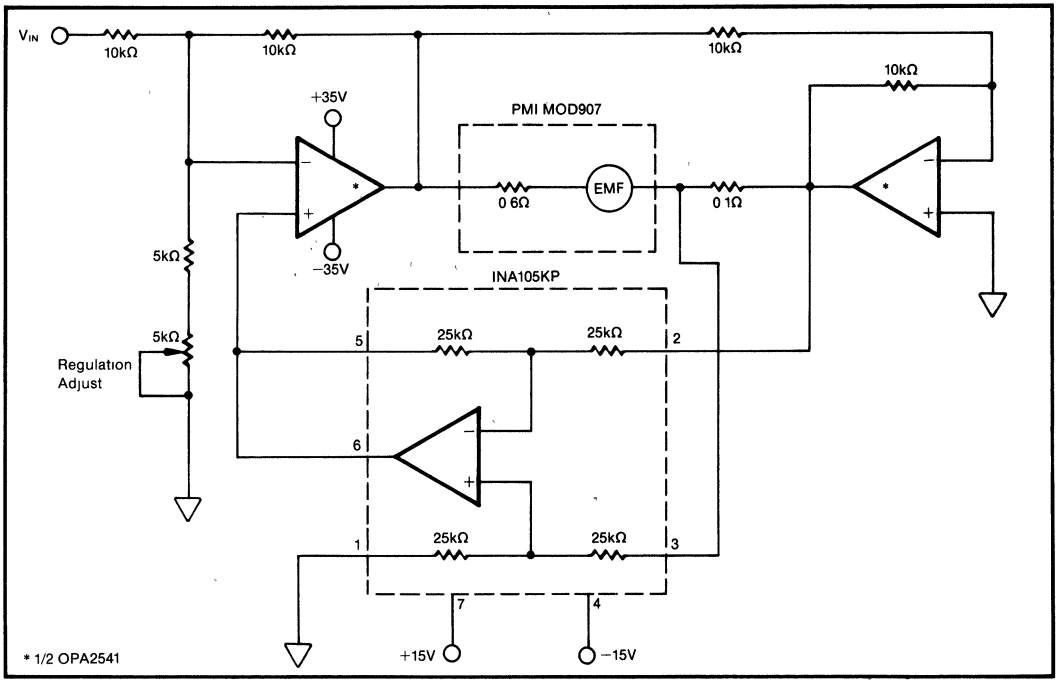


FIGURE 7. Bridge Amplifier Motor-Speed Controller.

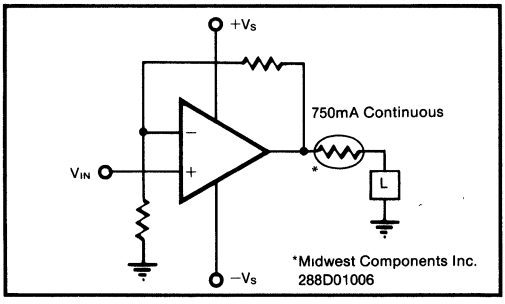


FIGURE 8. Limiting Output Current.

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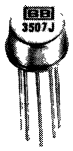


3507J

Fast-Slewing OPERATIONAL AMPLIFIER

FEATURES

- 120V/μsec SLEW RATE
- 20MHz GAIN-BANDWIDTH PRODUCT
- INTERCHANGEABLE WITH 741 TYPES

DESCRIPTION

Burr-Brown model 3507J is intended for use in circuits requiring fast transient response-pulse amplifiers, D/A converters, comparators, fast followers, etc. Key parameters such as slew rate, settling time and bandwidth are orders of magnitude better than for most other IC op amps.

The 3507J is compensated to allow faster slewing and greater bandwidth for gains of 3 or more. For gains greater than 3, the gain rolloff is 6dB/octave. By use of a single external 20pF compensation capacitor the 3507J can be stabilized at all gains including unity. In addition, by use of an alternate compensation technique, it is possible to stabilize the 3507J at unity gain without sacrificing its faster slew rate.

The 3507J is pin-compatible with other standard IC op amps while offering greater speed and higher output current. It also is input- and output-protected to prevent damage if the output is shorted to common, or the input is shorted to supply voltage.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

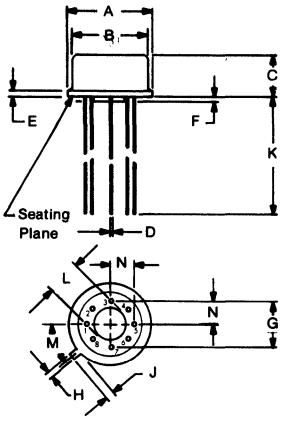
ELECTRICAL

Typical at ±15VDC and +25°C unless otherwise noted.

MODEL	3507J	
	TYPICAL	GUARANTEED
OPEN-LOOP GAIN, DC		
No Load	90dB	
2kΩLoad	83dB	77dB
RATED OUTPUT		
Voltage (1kΩ load)	±12V	±10V
Current	±20mA	±10mA
DYNAMIC RESPONSE		
Small Signal Bandwidth (0dB)	--	
Gain-Bandwidth Product (A_{CL} = 10)	20MHz	
Full Power Bandwidth	1.6MHz	1.2MHz
Slew Rate	120V/μsec	80V/μsec
Settling Time (0.1%)	200nsec	
Rise Time (10-90%, small signal)	25nsec	50nsec
Overshoot	--	--
INPUT OFFSET VOLTAGE		
Initial (without adjust) at +25°C	±5mV	±10mV
Over Temperature		±14mV
(avg. 0°C to +70°C)	±30μV/°C	
vs Supply Voltage	±30μV/V	200μV/V
vs Time	±50μV/mo	
INPUT BIAS CURRENT		
Initial at +25°C	+50nA	+250nA
Over Temperature		+500nA
(avg. 0°C to +70°C)	±0.5nA/°C	
INPUT DIFFERENCE CURRENT		
Initial at +25°C	±20nA	±50nA
Over Temperature		±100nA
(avg. 0°C to +70°C)	±0.1nA/°C	
INPUT IMPEDANCE		
Differential	100MΩ || 3pF	40MΩ
Common-Mode	1000MΩ || 3pF	
INPUT VOLTAGE RANGE		
Common-Mode (linear operation)	±12V	±10V
Differential (between inputs)		±15V
Absolute Max (either input)		±Supply
Common-Mode Rejection	90dB	74dB
POWER SUPPLY		
Rated Voltage		±15VDC
Voltage Range, derated	±8V to ±20V	
Current, quiescent	±4mA	±6mA
TEMPERATURE RANGE		
Specifications		0°C to +70°C
Operating		-25°C to +85°C
Storage		-65°C to +150°C

MECHANICAL

TO-99 PACKAGE

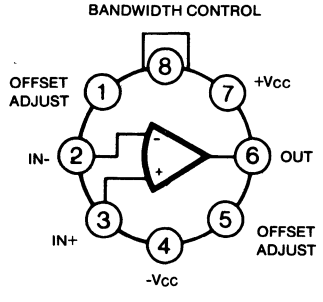


NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	335	370	8 51	9 40
B	305	335	7 75	8 51
C	165	185	4 19	4 70
D	016	021	0 41	0 53
E	.010	040	0 25	1 02
F	010	040	0 25	1 02
G	200 BASIC		5 08 BASIC	
H	028	034	0 71	0 86
J	.029	045	0 74	1 14
K	500	--	12 7	--
L	110	160	2 79	4 06
M	45° BASIC		45° BASIC	
N	095	105	2 41	2 67

CONNECTION DIAGRAM



(TOP VIEW)

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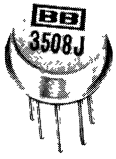

3508J

Wideband OPERATIONAL AMPLIFIER

FEATURES

- 100mHz GAIN BANDWIDTH PRODUCT
- 5nA INPUT BIAS CURENT
- 103dB OPEN-LOOP GAIN

DESCRIPTION

Burr-Brown model 3508J is a wideband operational amplifier intended for use in circuits requiring extended bandwidth and high gain. Typical examples of applications are: RF signal amplifiers, fast recovery voltage references, high speed integrators, high frequency active filters, and photodiode amplifiers.

Model 3508J is internally compensated for stability at gains greater than five and thus has a high gain-bandwidth product and fast slew rate. The 3508J can be externally compensated by use of a single capacitor, and can thus be stabilized at any value of gain. By use of an alternate compensation scheme the 3508J can be stabilized at unity gain without sacrificing slew rate.

In addition to its wide bandwidth and high gain the amplifier has a number of other significant advantages over other IC op amps; low bias current, high output current, and high common-mode rejection. Inputs are protected against voltages up to the value of the power supplies. The output is current-limited to provide short-circuit protection.

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PDS-298B

SPECIFICATIONS

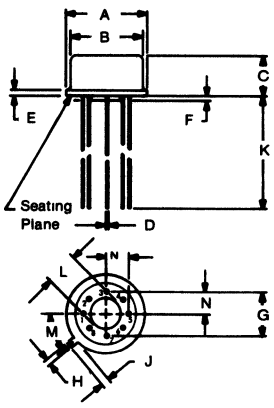
ELECTRICAL

Typical at ±15V and +25°C unless otherwise noted.

MODEL	3508J	
	TYPICAL	GUARANTEED
OPEN-LOOP GAIN, DC		
No Load	106dB	
2kΩ Load	103dB	98dB
RATED OUTPUT		
Voltage	±12V	±10V
Current	±18mA	±10mA
DYNAMIC RESPONSE		
Gain-Bandwidth Product (A_{CL} = 10)	100MHz	
Full Power Bandwidth	600kHz	320kHz
Slew Rate	35V/μsec	20V/μsec
Rise Time (10-90%, small signal)	17nsec	45nsec
INPUT OFFSET VOLTAGE		
Initial (without adjust) at +25°C	±3mV	±5mV
Over Temperature		±7mV
(avg. 0°C to +70°C)	±30μV/°C	
vs Supply Voltage	±30μV/V	±200μV/V
vs Time	±50μV/mo	
INPUT BIAS CURRENT		
Initial at +25°C	±15nA	±25nA
Over Temperature		±40nA
(avg. 0°C to +70°C)	±0.5nA/°C	
INPUT DIFFERENCE CURRENT		
Initial at +25°C	±5nA	±25nA
Over Temperature		±40nA
(avg. 0°C to +70°C)	±0.2nA/°C	
INPUT IMPEDANCE		
Differential	300MΩ ‖ 3pF	40MΩ
Common-Mode	1000MΩ ‖ 3pF	
INPUT VOLTAGE RANGE		
Common-Mode (linear operation)	±13V	±11V
Differential-Mode (between inputs)		±12V
Absolute Max (either input)		± Supply
Common-Mode Rejection	100dB	74dB
POWER SUPPLY		
Rated Voltage		±15VDC
Voltage Range, derated	±8V to ±22V	
Current, quiescent	±3mA	±4mA
TEMPERATURE RANGE		
Specification		0°C to +70°C
Operating		−25°C to +85°C
Storage		−65°C to +150°C

MECHANICAL

TO-99 PACKAGE

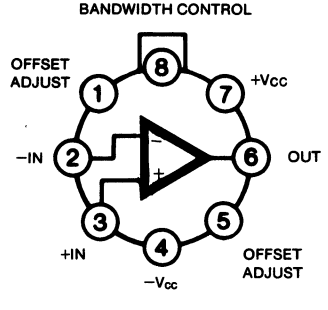


NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

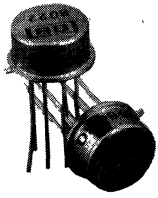
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

CONNECTION DIAGRAM



(TOP VIEW)

BURR-BROWN®

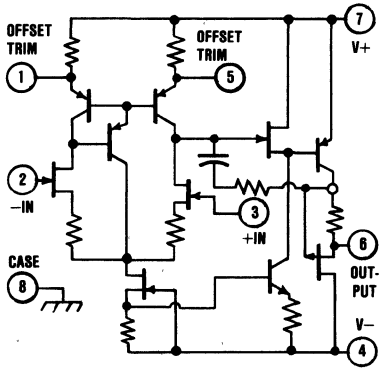


3550 SERIES

Fast-Settling FET OPERATIONAL AMPLIFIERS

FEATURES

- SETTLING TIME (0.01%), 600nsec, max
- TRUE DIFFERENTIAL INPUT
- SLEW RATE, 100V/μsec, min
- FULL POWER, 1.5MHz, min
- INPUT IMPEDANCE, $10^{11}\Omega$
- INTERNALLY COMPENSATED
- STABLE OPERATION, 1000pF, typ



DESCRIPTION

The 3550 is specifically designed for fast transient applications such as D/A and A/D conversion, sample/hold, multiplexer buffering and pulse amplification where the primary amplifier requirements are fast settling, good accuracy, and high input impedance.

Because the 3550 is internally compensated, elaborate compensation schemes requiring external components are not necessary. The smooth 6dB/octave rolloff of open-loop gain and the low output impedance provides the excellent step response and smooth settling without sacrificing frequency stability (no oscillations even with 1000pF of capacitive load)! A 10 to 1 improvement in settling time with large capacitive loads can be obtained with the addition of a single capacitor.

Unlike many wideband and fast settling amplifiers the 3550 has a true differential input. This means it can provide its excellent transient performance in the inverting, non-inverting, current to voltage, and difference configurations.

The 3550J and S have identical specifications except for temperature range: The 3550J is specified for 0°C to +70°C and the 3550S is specified for -55°C to +125°C. The 3550K has improved dynamic specifications and is specified over the 0°C to +70°C temperature range.

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PDS-302B

SPECIFICATIONS

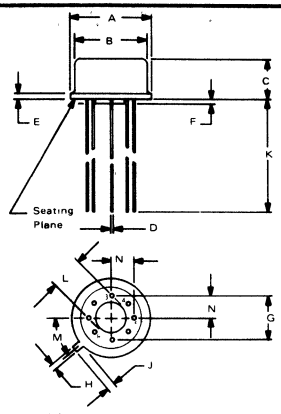
ELECTRICAL

Specifications typical at +25°C and ±15VDC Power Supply unless otherwise noted.

MODELS	3550J	3550K	3550S
OPEN LOOP GAIN, DC			
No load		100dB	
1kΩ, load min		88dB	
RATED OUTPUT			
Voltage, min		±10V	
Current, min		±10mA	
Open-loop Output Resistance		100Ω at 1MHz	
DYNAMIC RESPONSE			
Bandwidth (0dB, small signal)	10MHz	20MHz	10MHz
Full Power Response, min	1.0MHz	1 5MHz	1.0MHz
Slew Rate, min	65V/μsec	100V/μsec	65V/μsec
Settling Time (0 01%), max	1μsec	0.6μsec	1μsec
INPUT OFFSET VOLTAGE			
Initial Offset, +25°C, max		±1mV	
vs Temperature		±50μV/°C	
vs Supply Voltage		±500μV/V	
vs Time		±100μV/mo	
INPUT BIAS CURRENT			
Initial Bias, +25°C, max		−100pA (after full warm-up)	
vs Temperature		doubles every 10°C	
vs Supply Voltage		±1pA/V	
INPUT DIFFERENCE CURRENT			
Initial Difference, +25°C		±40pA	
INPUT IMPEDANCE			
Differential		$10^{11}\Omega$ || 3pF	
Common Mode		$10^{11}\Omega$ || 3pF	
INPUT NOISE			
Voltage, 0.01Hz - 10Hz, p-p		20μV	
10Hz - 10kHz, rms		4μV	
Current, 0.01Hz - 10Hz, p-p		0 2pA	
10Hz - 10kHz, rms		1.5pA	
INPUT VOLTAGE RANGE			
Common-Mode Voltage		±(|V_{cc}| −5)V	
Common-Mode Rejection		70dB at +5V, −10V	
Safe Input Voltage, max		±Supply	
POWER SUPPLY			
Rated Voltage		±15VDC	
Voltage Range, derated		±5VDC to ±20VDC	
Current, quiescent[1]		11mA	
TEMPERATURE RANGE			
Specification	0°C to +70°C		−55°C to +125°C
Operating	−55°C to +125°C		−55°C to +125°C
Storage		−65°C to +150°C	

NOTES:
1 The use of a finned heat sink is recommended.

MECHANICAL



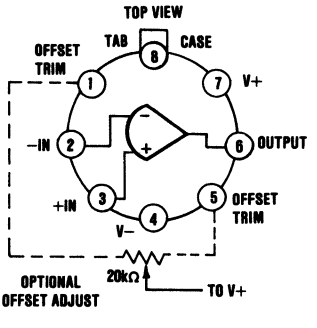
NOTE
Leads in true position within .010" (.25mm) R @ MMC at seating plane
Pin numbers shown for reference only
Numbers may not be marked on package

BOTTOM VIEW
Dimensions in inches are in parentheses.

Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	335	370	8 51	9 40
B	305	335	7 75	8 51
C	165	185	4 19	4 70
D	016	021	0 41	0 53
E	010	040	0 25	1 02
F	010	040	0 25	1 02
G	200 BASIC		5 08 BASIC	
H	028	034	0 71	0 86
J	029	045	0 74	1 14
K	500		12 7	
L	110	160	2 79	4 06
M	45° BASIC		45° BASIC	
N	095	105	2 41	2 67

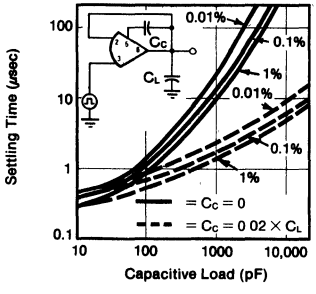
CONNECTION DIAGRAM



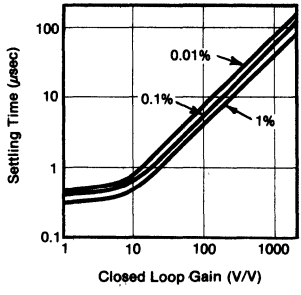
TYPICAL PERFORMANCE CURVES

T_A = +25°C ±V_{CC} = 15VDC unless otherwise indicated.

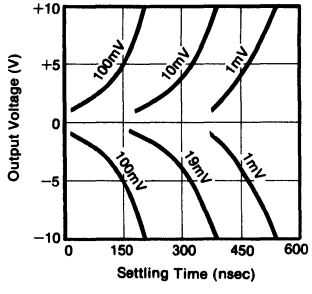
SETTLING TIME VS CAPACITIVE LOAD



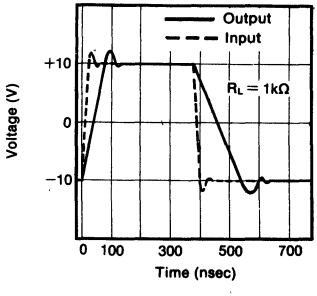
SETTLING TIME VS CLOSED LOOP GAIN



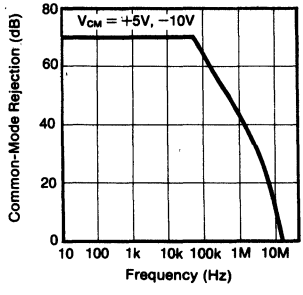
SETTLING TIME VS OUTPUT VOLTAGE CHANGE



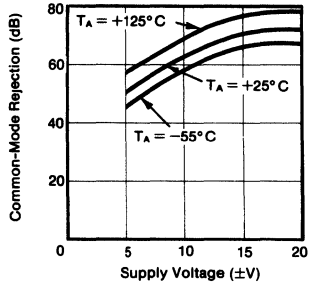
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



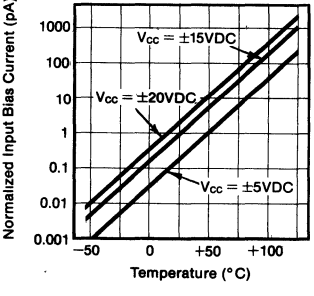
COMMON MODE REJECTION VS FREQUENCY



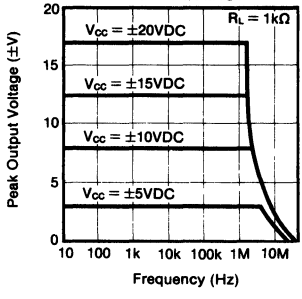
COMMON MODE REJECTION VS SUPPLY VOLTAGE



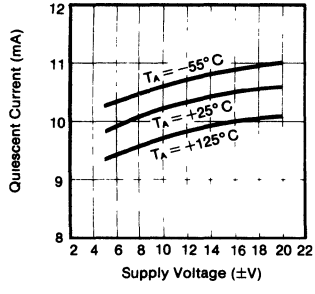
NORMALIZED INPUT BIAS CURRENT VS TEMPERATURE



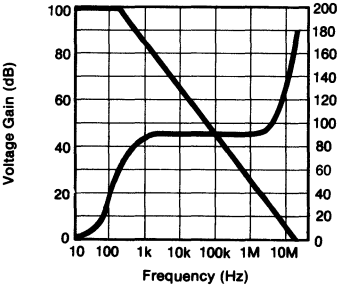
OUTPUT VOLTAGE VS FREQUENCY



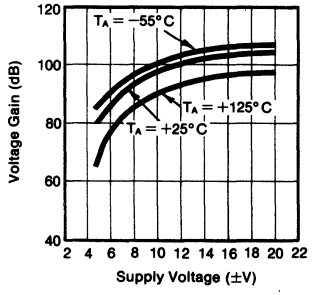
QUIESCENT CURRENT VS SUPPLY VOLTAGE



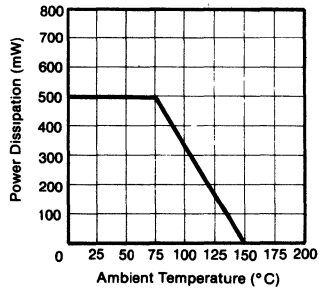
OPEN LOOP RESPONSE



OPEN LOOP GAIN VS SUPPLY VOLTAGE



MAXIMUM POWER DISSIPATION



APPLICATIONS

SETTLING TIME

Settling time of an amplifier is defined (see Figure 1) as the total time required, after an input step signal, for the output to "settle" within a specified error band around the final value. This error band is expressed as a percentage of the magnitude of the step transition. A recommended test circuit for settling time is shown in Figure 2. The output error signal appears, attenuated by a factor of two, at point A and may be observed at this point with the aid of an oscilloscope. The diodes act as limiters to prevent overloading the oscilloscope during the fast leading edge of the input signal. All resistors should be 2kΩ or less to eliminate degradation of performance due to stray capacitance. A typical measurement desired is the settling time to 0.01% for a 10-volt step input. This is the time required for the signal at point A to decrease to 0.5mV or less and remain below this level.

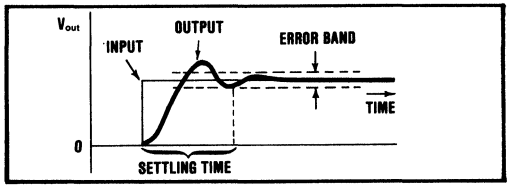


FIGURE 1. Concept of Settling Time.

Settling time for noninverting circuits can also be measured but requires the use of ultra-fast differential amplifier test fixtures. For the 3550 settling time is equal for inverting or noninverting circuits of equal gain.

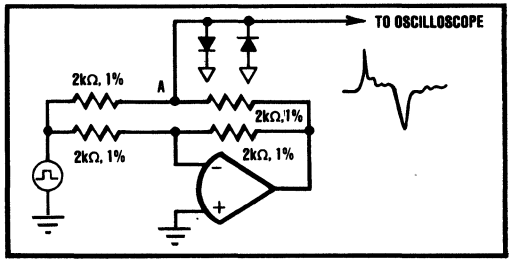


FIGURE 2. Settling Time Test Circuit.

Because settling time is affected by bandwidth which in turn is dependent upon closed-loop gain, the settling time of any operational amplifier will be a function of closed loop gain. Settling Time versus Gain curves illustrate this effect for the 3550 at several levels of settling accuracy.

The 3550 is remarkably tolerant of load capacitance because of its stable, 6dB/octave gain rolloff and low output impedance. Settling Time versus Load Capacitance curves show this characteristic for the unity-gain configuration. For larger values of load capacitance the compensation technique of Figure 3 may be used to optimize the response. The slight negative feedback provided by C_C tends to reduce any ringing at the top of the output voltage waveform without significantly affecting the slew rate. See the Settling Time versus Load Capacitance curves for typcial improvements in settling time.

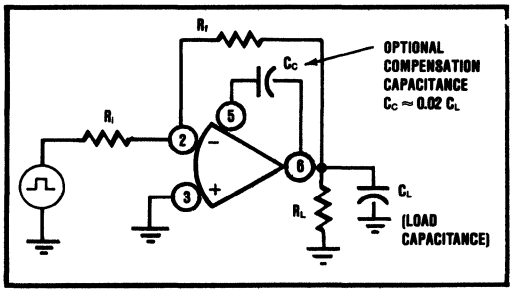


FIGURE 3. Compensation for Load Capacitance.

WIRING RECOMMENDATIONS

In order to fully realize the high frequency performance capabilities of the 3550, proper attention must be given to layout, component selection and grounding. All leads associated with the input and feedback elements should be as short as possible and all connections should be made as close to the amplifier terminals as possible. Input and feedback resistors should be made as small as possible consistent with other circuit constraints. Capacitance from the ouput to noninverting input can cause high frequency oscillations, particularly in high gain circuits operating from large source impedance. Careful layout of wiring or PC board patterns is the only satisfactory way of preventing such problems.

In order to prevent high frequency oscillations due to lead inductance the power supply leads should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 0.001μF ceramic capacitor from pins 7 and 4 to the power supply common.

INPUT AND OUTPUT VOLTAGE RANGE

Although the 3550 is specified for best operation on power supply voltage of ±15VDC, it will operate with minor performance changes over a power supply voltage range of ±5VDC to ±20VDC. Many of the curves show performance of the 3550 when operated from supplies other than ±15VDC.

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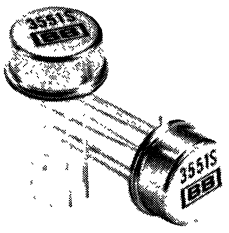
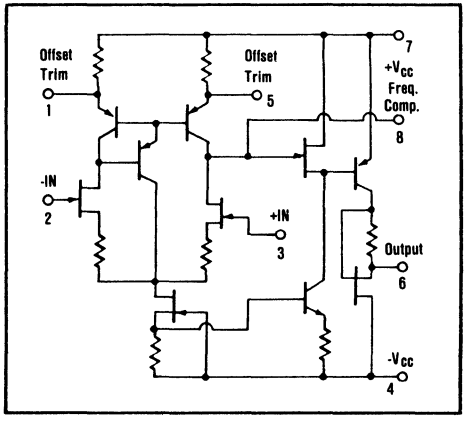


3551 SERIES

Wideband and Fast-Settling FET OPERATIONAL AMPLIFIERS

FEATURES

- REDUCES WIDEBAND ERRORS
  - 50MHz Gain-bandwidth product (ACL ≥10)
  - 250V/μs slew rate (Cf = 0)
- VERSATILE
  - Single compensation capacitor allows optimum response
  - True differential input
- PRESERVES DC ACCURACY
  - Bias current, 100pA, max
  - Laser-trimmed offset voltage



DESCRIPTION

The 3551 is designed to offer the user versatility in wideband steady state and fast transient applications. The use of a single external compensation capacitor allows the user to optimize frequency response for maximum bandwidth for a variety of closed loop gains and capacitive loads. The amplifier is stable at closed loop gains of greater than 10V/V, with no external compensation and may be stabilized at all gains with the single 10pF compensation capacitor.

In addition to the excellent dynamic response characteristics, the 3551 also has good DC properties. The use of a monolithic FET input stage gives the 3551 very low input bias and offset currents. This is in contrast to the high input currents usually associated with fast amplifiers having bipolar input stages. Also, the input offset voltage and offset voltage drift are low as a result of Burr-Brown's laser-trimming techniques.

Unlike many wideband and fast settling amplifiers, the 3551 has a true differential input. This means it can provide its excellent wideband response in the inverting, noninverting, current-to-voltage and difference configurations.

The 3551 is an excellent choice for applications such as fast D/A and A/D converters, high speed comparators and fast sampling circuits, to name just a few.

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PDS-301C

SPECIFICATIONS

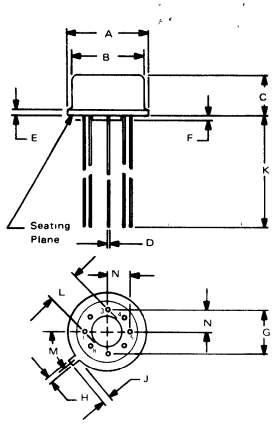
ELECTRICAL

Specifications typical at 25°C and ±15VDC Power Supply unless otherwise noted

MODELS	3551J	3551S
OPEN LOOP GAIN, DC		
No Load	100dB	
1kΩ, Load min	88dB	
RATED OUTPUT		
Voltage, min	±10V	
Current, min	±10mA	
Open Loop Output Resistance	100Ω at 1MHz	
DYNAMIC RESPONSE		
Gain-Bandwidth Product		
Gain = 1000	50MHz	
Gain = 10	50MHz	
Slew Rate (Cf = 0)	250V/μsec	
INPUT OFFSET VOLTAGE		
Initial Offset, 25°C, max	±1mV	
vs Temp(1)	±50μV/°C	
vs Supply Voltage	±500μV/V	
vs Time	±100μV/mo	
INPUT BIAS CURRENT		
Initial Bias, 25°C, max	-400pA (after full warm-up)	
vs Temperature	doubles every 10°C	
vs Supply Voltage	±1pA/V	
INPUT DIFFERENCE CURRENT		
Initial Difference, 25°C	±40pA	
INPUT IMPEDANCE		
Differential	$10^{11}\Omega$ || 3pF	
Common-mode	$10^{11}\Omega$ || 3pF	
INPUT NOISE		
Voltage, 0.01Hz to 10Hz, p-p	20μV	
Voltage, 10Hz to 10kHz, rms	4μV	
Current, 0.01Hz to 10Hz, p-p	0.2pA	
Current, 10Hz to 10kHz, rms	1.5pA	
INPUT VOLTAGE RANGE		
Common-mode Voltage	±(|Vcc|-5)V	
Common-mode Rejection	70dB at +5V, -10V	
Max Safe Input Voltage	±Supply	
POWER SUPPLY		
Rated Voltage	±15VDC	
Voltage Range, derated	±5VDC to ±20VDC	
Current, quiescent(1)	11mA (15mA max)	
TEMPERATURE RANGE		
Specification	0°C to +70°C	-55°C to +125°C
Operating	-55°C to +125°C	-55°C to +125°C
Storage	-65°C to +150°C	

NOTE
1 The use of a finned heat sink is recommended

MECHANICAL TO-99



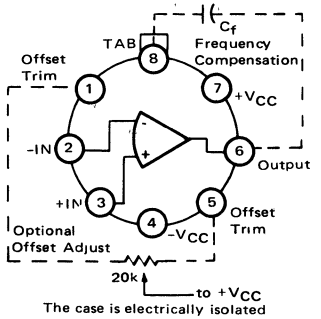
NOTE
Leads in true position within .010 (.25mm) R @ MMC at seating plane

Pin numbers shown for reference only. Numbers may not be marked on package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	–	12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]

CONNECTION DIAGRAM

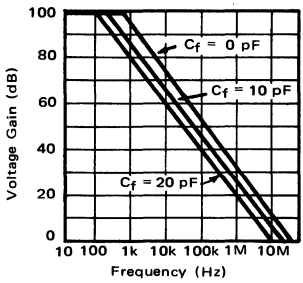


The case is electrically isolated

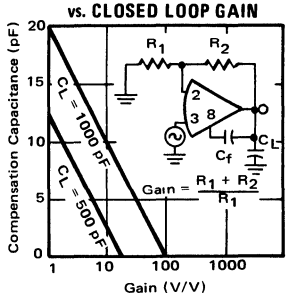
TYPICAL PERFORMANCE CURVES

T_A = 25°C V_S = ±15 VDC unless otherwise indicated.

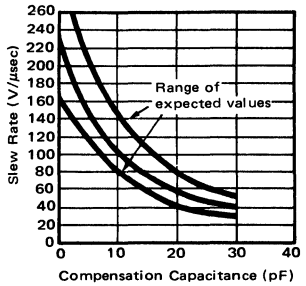
OPEN LOOP RESPONSE



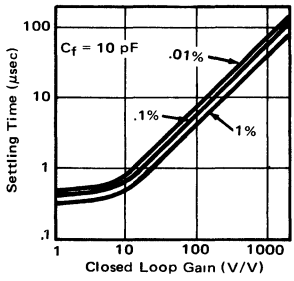
RECOMMENDED VALUES OF FREQUENCY COMPENSATION CAPACITANCE vs. CLOSED LOOP GAIN



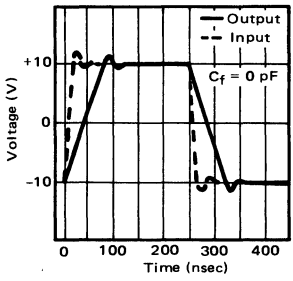
SLEW RATE vs. COMPENSATION CAPACITANCE



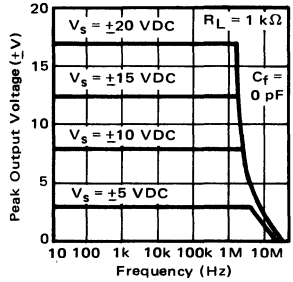
SETTLING TIME vs. CLOSED LOOP GAIN



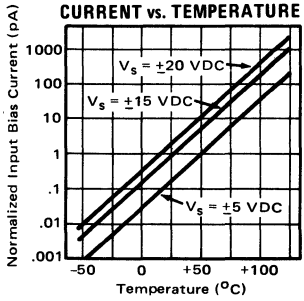
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



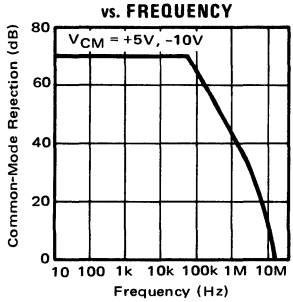
OUTPUT VOLTAGE vs. FREQUENCY



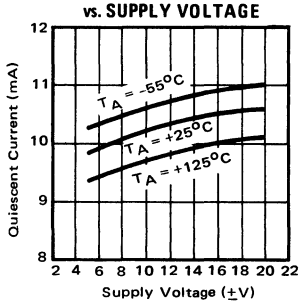
NORMALIZED INPUT BIAS CURRENT vs. TEMPERATURE



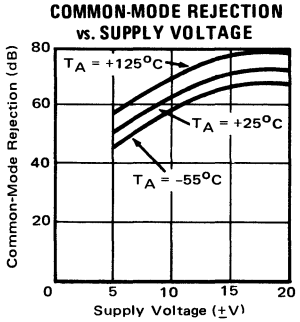
COMMON-MODE REJECTION vs. FREQUENCY



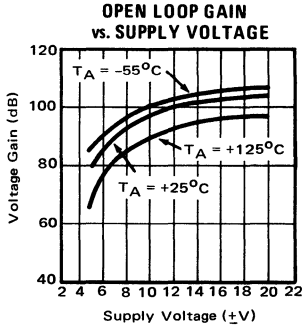
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



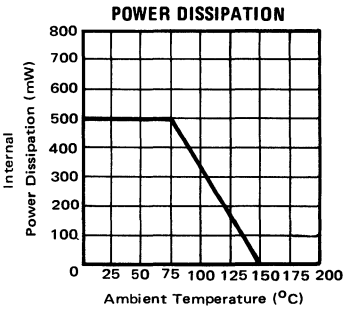
COMMON-MODE REJECTION vs. SUPPLY VOLTAGE



OPEN LOOP GAIN vs. SUPPLY VOLTAGE



MAXIMUM POWER DISSIPATION



APPLICATIONS

WIRING RECOMMENDATIONS

In order to fully realize the high frequency performance capabilities of the 3551, proper attention must be given to layout, component selection and grounding. All leads associated with the input and feedback elements should be as short as possible and all connections should be made as close to the amplifier terminals as possible. Input and feedback resistors should be made as small as possible consistent with other circuit constraints. Capacitance from the output to noninverting input can cause high frequency oscillations, particularly in high gain circuits operating from large source impedances. Careful layout of wiring or PC board patterns is the only satisfactory way of preventing such problems.

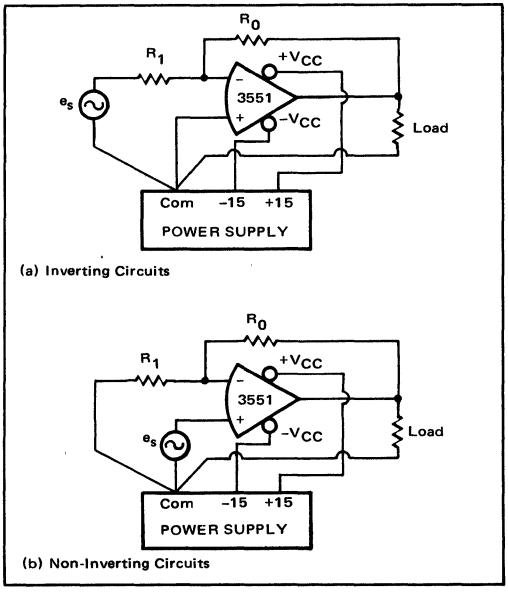


FIGURE 1. Proper Grounding Methods.

Provision for phase compensation should always be made on the PC board even if initial calculations and breadboarding may indicate that none is needed.

In order to prevent high frequency oscillations due to lead inductance the power supply leads should be bypassed. This should be done by connecting a 10 μf tantalum capacitor in parallel with a 0.001 μf ceramic capacitor from pins 7 and 4 to the power supply common.

INPUT AND OUTPUT VOLTAGE RANGE

Although the 3551 is specified for best operation on power supply voltage of ±15 VDC, it will operate with minor performance changes over a power supply voltage range of ±5 VDC to ±20 VDC. Many of the performance curves show performance of the 3551 when operated from supplies other than ±15 VDC.

INPUT/OUTPUT PROTECTION

All of the amplifiers listed in the specification table are designed to withstand input voltages as high as the supply voltage, without damage to the amplifier. Thus, inputs may be subjected to either supply voltage, in any combination, without damage.

Output stages are internally current limited and will withstand short-circuit-to-ground conditions. However, application of nonzero potential to the output pin may cause permanent damage and should be prevented by the proper precautions.

SETTLING TIME

Settling time of an amplifier is defined as the total time required, after an input step signal, for the output to "settle" within a specified error band around the final value. This error band is expressed as a percentage of the magnitude of the step transition.

Because settling time is affected by bandwidth which in turn is dependent upon closed loop gain, the settling time of any operational amplifier will be a function of closed loop gain. Settling time vs. gain curves illustrate this effect for the 3551 at several levels of settling accuracy.

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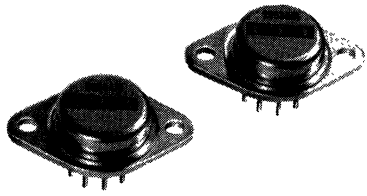

3553

Wideband - Fast-Slewing BUFFER AMPLIFIER

FEATURES

- GAIN = .99V/V
- OUTPUT CURRENT, ±200mA
- BANDWIDTH, 300MHz
- SLEW RATE, 2000V/μsec
- ELECTRICALLY ISOLATED CASE
- EXTENDS OP AMP DRIVING CAPABILITY WHILE PRESERVING BANDWIDTH & SETTLING TIME

DESCRIPTION

The 3553 is a unity-gain amplifier designed to be used either as a signal buffer, or as the power output stage for an operational amplifier. Because of its wideband response (300MHz, -3dB bandwidth) and fast slewing capability (2000V/μsec) the 3553 is capable of following very fast signals. When used inside the feedback loop of an operational amplifier, these high speed characteristics are essential in order to preserve the performance and stability of the feedback amplifier circuit.

With its ±200mA of output current capability, the 3553 is capable of driving a signal of ±10V into a 50Ω load. This power capability, coupled with its extremely high speed and wide bandwidth, makes the 3553 ideally suited for line driving applications where fast pulses or wideband signals are involved.

In addition to its fast/wideband characteristics and high output current, the 3553 has low input offset voltage and drift. This adds to its versatility, particularly in stand-alone buffer amplifier applications.

The 3553 is packaged in a reliable hermetically sealed TO-3 package for environmental ruggedness. The metal case is completely electrically isolated. This simplifies mounting and reduces cost since the need for insulating spacers and bushings is eliminated.

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PDS-329B

SPECIFICATIONS

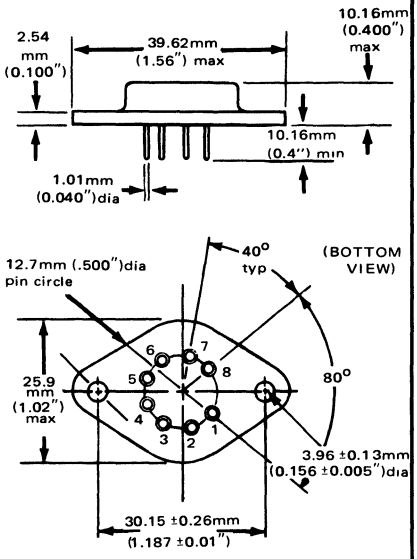
Specifications are typical at +25°C Case Temperature and ± 15 VDC power supply unless otherwise noted.

ELECTRICAL

MODEL	3553AM
GAIN, DC	
No Load	0.98 V/V
50 Ω Load, min	0.92 V/V
RATED OUTPUT	
Voltage, min	±10 V
Current, min	±200 mA
Output Resistance	1 Ω
DYNAMIC RESPONSE	
Slew Rate, min	2000 V/μsec
Full Power Bandwidth, min	32 MHz
Small Signal -3dB Bandwidth	300 MHz
Settling Time to 1%	7.2 nsec
to .01%	14.5 nsec
INPUT PARAMETERS	
Input Voltage, linear range	±10 V
Input Voltage, absolute, max	±Supply Voltage
Input Impedance	$\pm 10^{11}$ Ω
Input Bias Current @ +25°C (doubles/+10°C)	-200 pA
OUTPUT OFFSET VOLTAGE	
Initial Offset @ +25°C, max	±50 mV
vs. Temperature (average) -25°C to +85°C	±300 μV/°C
POWER SUPPLY	
Rated Voltage	±15 VDC
Voltage Range, derated	±5 VDC to ±20 VDC
Current, Quiescent, max	±80 mA
typ	±50 mA
TEMPERATURE RANGE (Case)	
Specification	-25°C to +85°C
Operation (derate above +120°C Case)	-55°C to +125°C
Storage	-65°C to +150°C
θ_{JC} Thermal Resistance, junction to case	6°C/W
θ_{JA} Thermal Resistance, junction to ambient	33°C/W

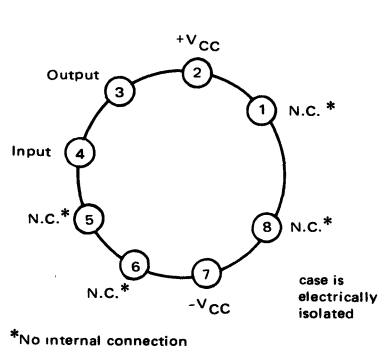
MECHANICAL

M PACKAGE (TO-3)

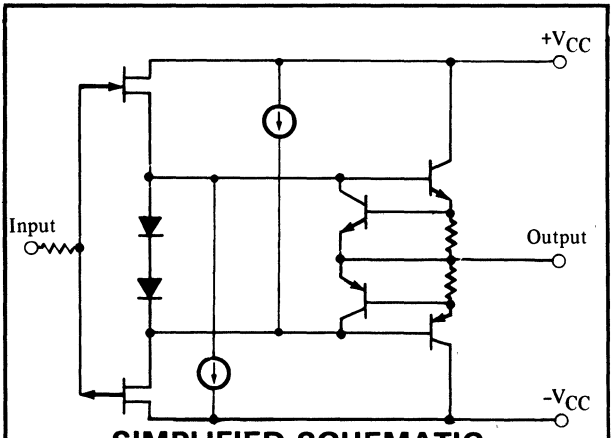


Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]

CONNECTION DIAGRAM



*No internal connection
CONNECTOR: 0803MC
HEATSINKS: 0803HS 12°C/W
0804HS 4.2°C/W
0805HS 3°C/W

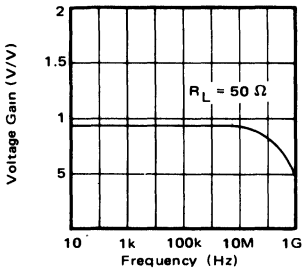


SIMPLIFIED SCHEMATIC

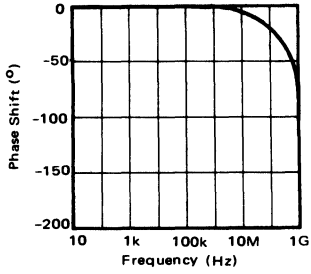
TYPICAL PERFORMANCE CURVES

Typical at 25°C and rated supply voltage unless otherwise noted.

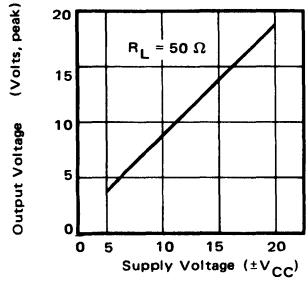
SMALL SIGNAL FREQUENCY RESPONSE



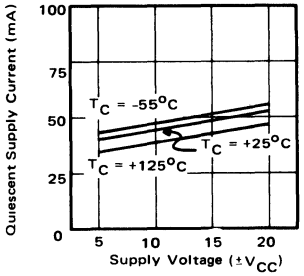
PHASE SHIFT vs FREQUENCY



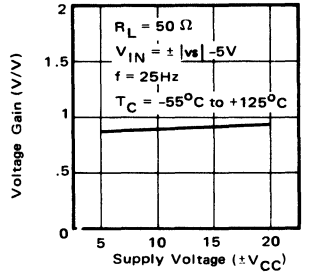
OUTPUT VOLTAGE RANGE vs SUPPLY VOLTAGE



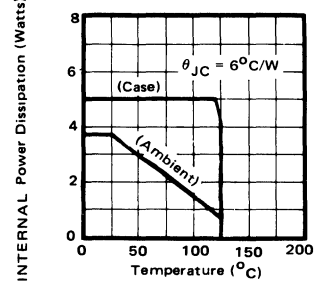
QUIESCENT POWER SUPPLY CURRENT vs SUPPLY VOLTAGE



GAIN vs SUPPLY VOLTAGE



POWER DISSIPATION



APPLICATION INFORMATION

BOOSTER AMPLIFIER

One of the primary applications for the 3553 is that of a current booster for an operational amplifier. The circuit of Figure 1 is typical of such applications. Note that the 3553 is used inside the feedback loop and becomes, effectively, the output stage of the composite amplifier. Because the 3553 has unity voltage gain, wideband response, fast slewing rate, and very little phase delay, the dynamic response of the operational amplifier is virtually unaffected by the addition of the booster.

The already low offset voltage of the 3553 is effectively reduced by a factor equal to the open loop gain of the operational amplifier and becomes a negligible factor in total offset error of the circuit.

Input impedance of the 3553 is extremely high, thus requiring almost no drive current from the operational amplifier. On the other hand, the presence of the 3553 in the circuit increases the output current capability to ±200 mA, drastically lowers the output impedance of the loop, and permits the driving of low impedance loads such as a terminated 50Ω coaxial line.

Capacitive loads, often a source of instability and oscillations in operational amplifier circuits, are buffered by the presence of the 3553. In driving heavily capacitive loads the slew rate of the 3553 will be seen to decrease. This is due simply to the large currents required by fast voltage slewing in a capacitive load,

$$I_c = C_{load} \frac{dV}{dt}.$$

The internal current limit of the 3553 (approximately 600 mA) places a limit on the slewing rate under such conditions.

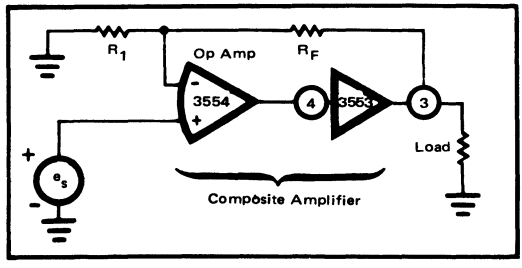


FIGURE 1. Model 3553 as a power booster.

BUFFER AMPLIFIER

The 3553 may also be used, as shown in Figure 2, as a unity gain buffer amplifier. No operational amplifier is required in this mode of operation. Since the 3553 is then operated without feedback, it's offset voltage and drift are translated to the output. While the gain is not precisely unity in this mode, the accuracy is adequate for many applications.

INPUT/OUTPUT PROTECTION

The output stage of the 3553 is current limited at approximately 600mA. This will provide a measure of output short circuit protection for the amplifier for a period of time as determined by the heatsinking used, the amplifier's thermal resistance, the ambient temperature, etc. The amplifier's output stage transistors should not be allowed to exceed 150°C (175°C absolute max).

The input stage is designed to allow the application of either supply voltage without damage to the amplifier.

POWER DISSIPATION

The power dissipation capability of the 3553 varies with ambient temperature and with the type of heat sink used. A heat sink may be used to increase the dissipation capability or to achieve a given dissipation capability at higher temperature. The power derating curve is given in the Typical Performance Curves.

WIRING RECOMMENDATIONS

No special wiring techniques are necessary with the 3553. However, it is recommended, as a good engineering practice, that the power supply lines be bypassed to common at a point near the amplifier. (A 1.0μF electrolytic in parallel with a 1000pF ceramic is recommended.) If the 3553 is used with a wideband operational amplifier, all leads must be kept as short as possible to minimize stray capacitance and unwanted feedback paths.

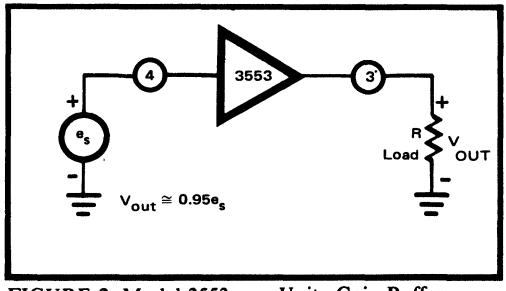


FIGURE 2. Model 3553 as a Unity Gain Buffer.

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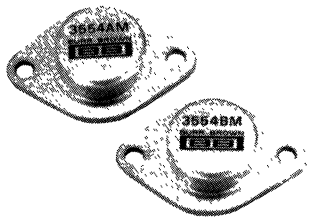


3554

Wideband - Fast-Settling OPERATIONAL AMPLIFIER

FEATURES

- SLEW RATE, 1000V/μsec
- FAST SETTLING, 150nsec, max (to ±.05%)
- GAIN-BANDWIDTH PRODUCT, 1.7GHz
- FULL DIFFERENTIAL INPUT

APPLICATIONS

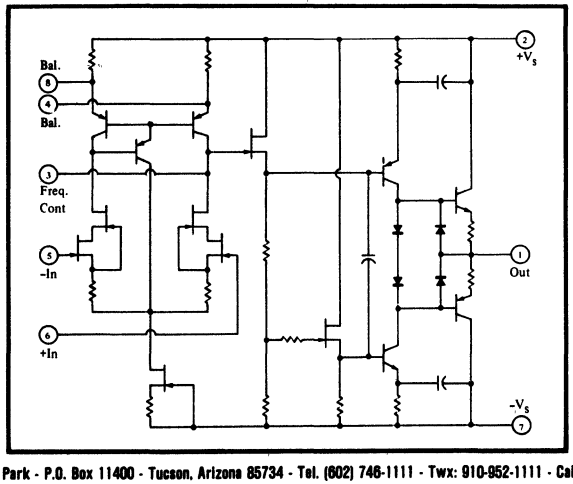
- PULSE AMPLIFIERS
- TEST EQUIPMENT
- WAVEFORM GENERATORS
- FAST D/A CONVERTERS

DESCRIPTION

The 3554 is a full differential input, wideband operational amplifier. It is designed specifically for the amplification or conditioning of wideband data signals and fast pulses. It features an unbeatable combination of gain-bandwidth product, settling time and slew rate. It uses hybrid construction. On the beryllia substrate are matched input FETs, thin-film resistors and high speed silicon dice. Active laser trimming and complete testing provide superior performance at a very moderate price.

The 3554 has a slew rate of 1000V/μsec and will output ±10V and ±100mA. When used as a fast settling amplifier, the 3554 will settle to ±0.05% of the final value within 150nsec. A single external compensation capacitor allows the user to optimize the bandwidth, slew rate or settling time in the particular application.

The 3554 is reliable and rugged and addresses almost any application when speed and bandwidth are serious considerations. It is particularly a good choice for use in fast settling circuits, fast D/A converters, multiplexer buffers, comparators, waveform generators, integrators, and fast current amplifiers. It is available in several grades to allow selection of just the performance required.



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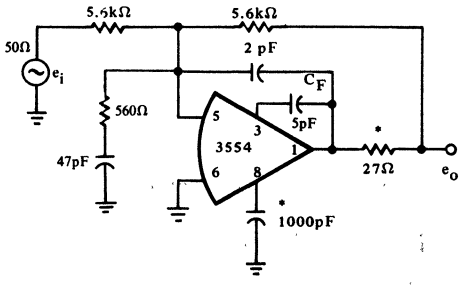
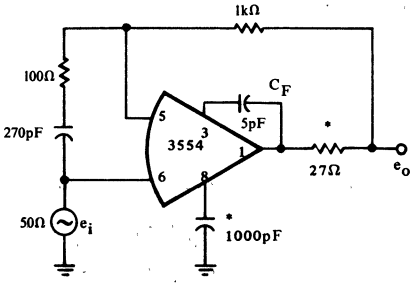
PDS-331B

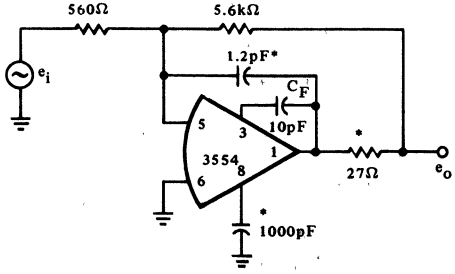
TYPICAL CIRCUITS



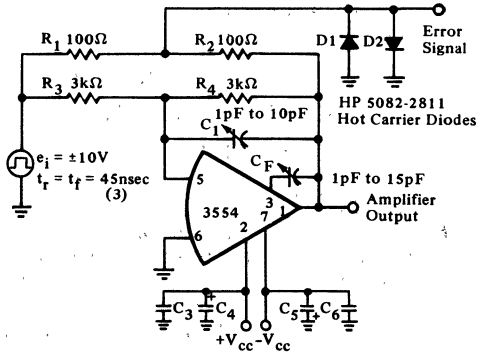
X1 Inverter



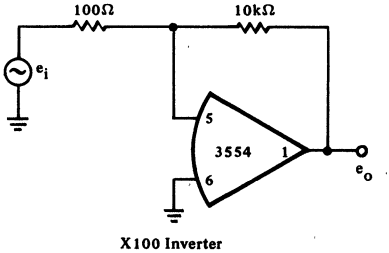
X1 Noninverter



X10 Inverter

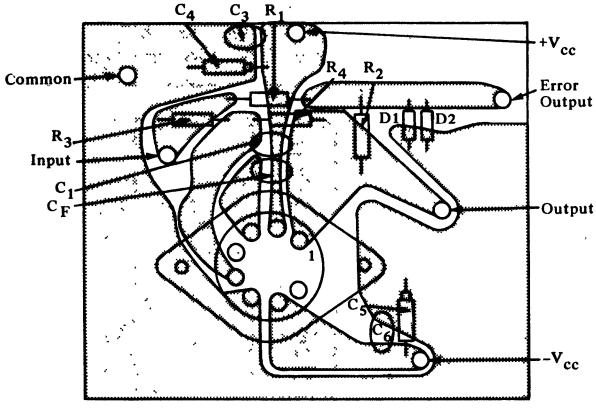


Settling Time Test Circuit Schematic



X100 Inverter

View from Component Side.
Shaded area is the pattern side conductor.



Settling Time Test Circuit Layout

NOTES:
1. These circuits are optimized for driving large capacitive loads (to 470pF).
2. The 3554 is stable at gains of greater than 55 ($C_L \leq 100$pF) without any frequency compensation.
3. 45nsec is optimum. Very fast rise times (10-20nsec) may saturate the input stage causing less than optimum settling time performance.

*Indicates component that may be eliminated when large capacitive loads are not being driven by the device.

ELECTRICAL SPECIFICATIONS

At T_{CASE} = 25°C and ±15VDC, unless otherwise noted

PARAMETERS	CONDITIONS	3554AM			3554BM			3554SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OPEN-LOOP GAIN,DC					*	*	*	*	*	*	
No Load		100	106								dB
Rated Load	R_L = 100Ω	90	96								dB
RATED OUTPUT					*	*	*	*	*	*	
Voltage	I_O = ±100mA	±10	±11								V
Current	V_O = ±10V	±100	±125								mA
Output Resistance, open loop	f = 10MHz		20								•Ω
DYNAMIC RESPONSE					*	*	*	*	*	*	
Bandwidth (0dB, small signal)	C_F = 0	70	90								MHz
Gain-bandwidth Product	C_F = 0, G = 10 V/V	150	225								MHz
	C_F = 0, G = 100 V/V	425	725								MHz
	C_F = 0, G = 1000 V/V	1000	1700								MHz
Full Power Bandwidth	C_F = 0, V_o = 20Vp-p, R_L = 100Ω	16	19								MHz
Slew Rate	C_F = 0, V_o = 20Vp-p, R_L = 100Ω	1000	1200								V µsec
Settling Time to ±1%	A = 1		60								nsec
to ±.1%	A = 1		120								nsec
to ±.05%	A = 1		140	150							nsec
to ±.01%	A = 1		200	250							nsec
INPUT OFFSET VOLTAGE											
Initial offset, T_A = 25°C			±0.5	±2		±0.2	±1		±0.2	±1	mV
vs Temp (T_A = -25°C to +85°C)			±20	±50		±8	±15				µV °C
vs Temp (T_A = -55°C to +125°C)									±12	±25	µV °C
vs Supply Voltage			±80	±300		*	*		*	*	µV V
INPUT BIAS CURRENT					*	*	*	*	*	*	
Initial bias, 25°C		0	-10	-50							pA
vs Temp			**								
vs Supply Voltage			±1								pA V
INPUT DIFFERENCE CURRENT					*	*	*	*	*	*	
Initial difference, 25°C			±2	±10							pA
INPUT IMPEDANCE						*			*		
Differential			10^{11} ‖ 2								Ω ‖ pF
Common-mode			10^{11} ‖ 2								Ω ‖ pF
INPUT NOISE					*	*	*	*	*	*	
Voltage f_o = 1Hz	R_S = 100Ω		125								nV $\sqrt{Hz}$
f_o = 10Hz	R_S = 100Ω		50								nV $\sqrt{Hz}$
f_o = 100Hz	R_S = 100Ω		25								nV $\sqrt{Hz}$
f_o = 1kHz	R_S = 100Ω		15								nV $\sqrt{Hz}$
f_o = 10kHz	R_S = 100Ω		10								nV $\sqrt{Hz}$
f_o = 100kHz	R_S = 100Ω		8								nV $\sqrt{Hz}$
f_o = 1MHz	R_S = 100Ω		7								nV $\sqrt{Hz}$
f_B = .3Hz to 10Hz	R_S = 100Ω		2								µV, p-p
f_B = 10Hz to 1MHz	R_S = 100Ω		8								µV, rms
Current, f_B = .3Hz to 10Hz	R_S = 100Ω		45								fA, p-p
f_B = 10Hz to 1MHz	R_S = 100Ω		2								pA, rms
INPUT VOLTAGE RANGE					*	*	*	*	*	*	
Common-mode Voltage Range	Linear Operation		±(V_{CC}-4)								V
Common-mode Rejection	f = DC, V_{CM} = +7V, -10V	44	78								dB
Max Safe Input Voltage			±Supply								V
POWER SUPPLY					*	*	*	*	*	*	
Rated Voltage			±15								VDC
Voltage Range, derated performance		±5		±18							VDC
Current, quiescent		±17	±35	±45							mA
TEMPERATURE RANGE (ambient)											
Specification		-25		+85	-25		+85	-55		+125	°C
Operating, derated performance		-55		+125	-55		+125	-55		+125	°C
Storage		-65		+150	-65		+150	-65		+150	°C
θ junction-case			15			15			15		°C W
θ junction-ambient			45			45			45		°C W

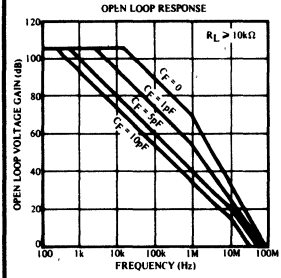
* Specifications same as for 3554AM

** Doubles every +10°C

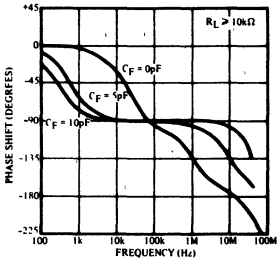
TYPICAL PERFORMANCE CURVES

at T_C = +25°C and ±15VDC unless otherwise noted.

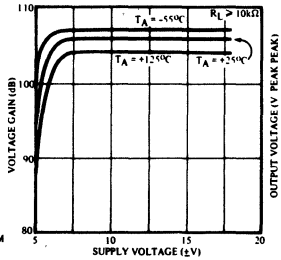
OPEN LOOP RESPONSE



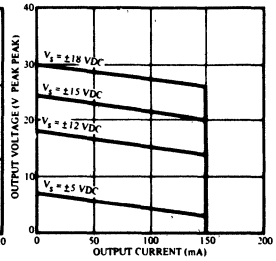
OPEN LOOP RESPONSE



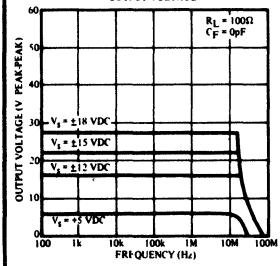
VOLTAGE GAIN



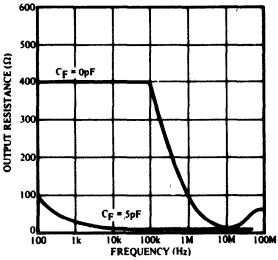
OUTPUT VOLTAGE VS OUTPUT CURRENT



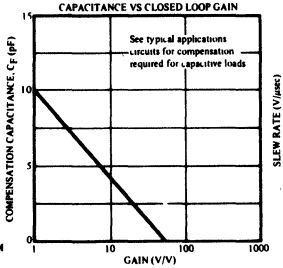
OUTPUT VOLTAGE



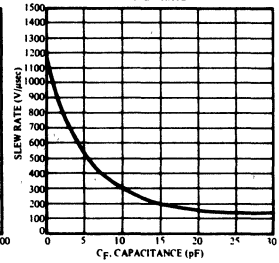
OPEN LOOP OUTPUT RESISTANCE VS FREQUENCY



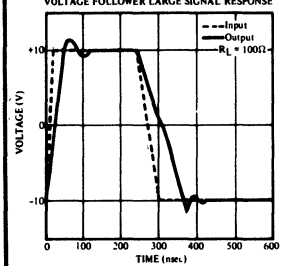
RECOMMENDED VALUES OF COMPENSATION CAPACITANCE VS CLOSED LOOP GAIN



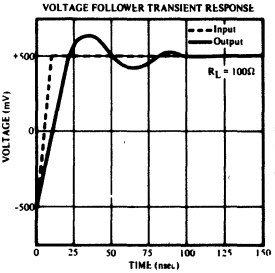
SLEW RATE



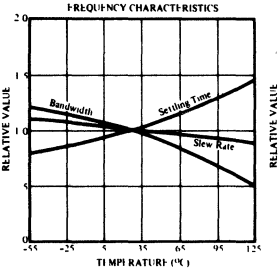
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



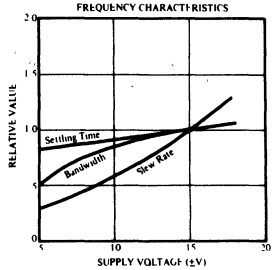
VOLTAGE FOLLOWER TRANSIENT RESPONSE



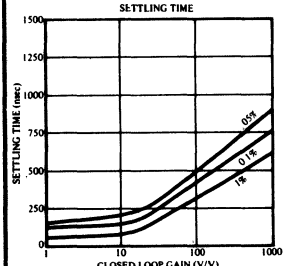
FREQUENCY CHARACTERISTICS



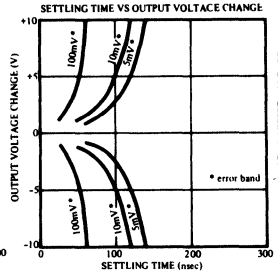
FREQUENCY CHARACTERISTICS



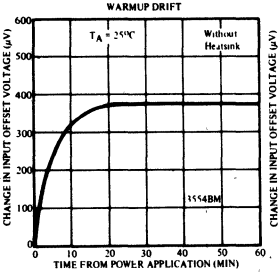
SETTLING TIME



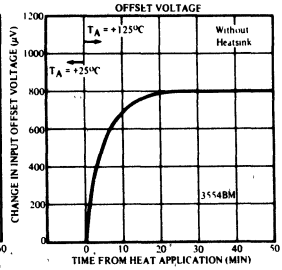
SETTLING TIME VS OUTPUT VOLTACE CHANGE



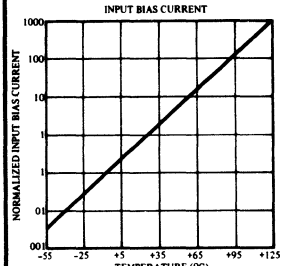
WARMUP DRIFT



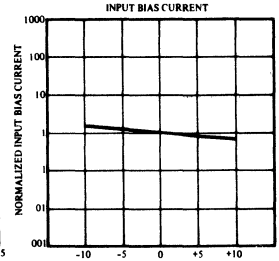
EFFECT OF THERMAL SHOCK ON OFFSET VOLTAGE



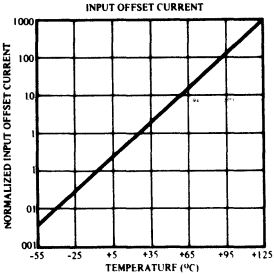
INPUT BIAS CURRENT



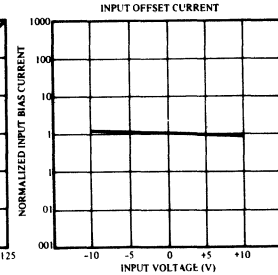
INPUT BIAS CURRENT

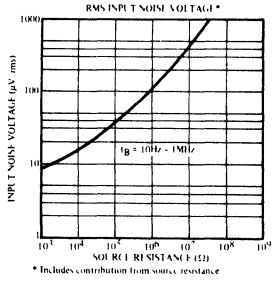


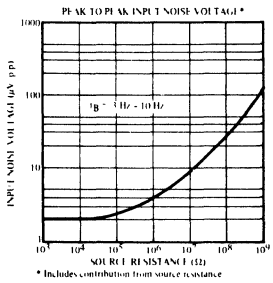
INPUT OFFSET CURRENT

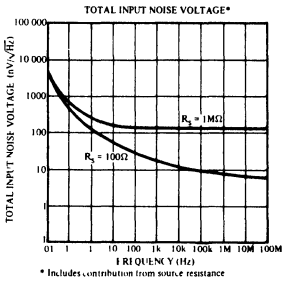


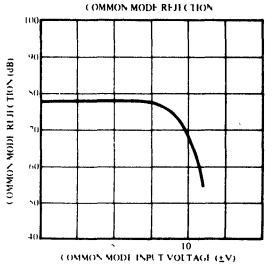
INPUT OFFSET CURRENT

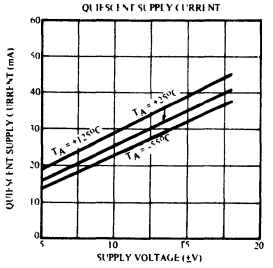


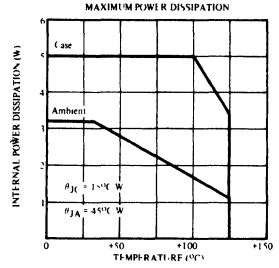




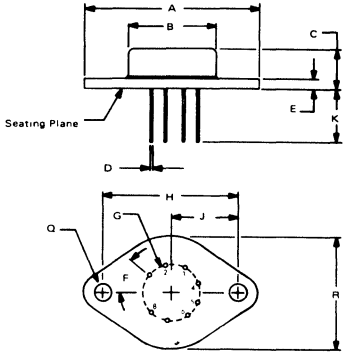








MECHANICAL

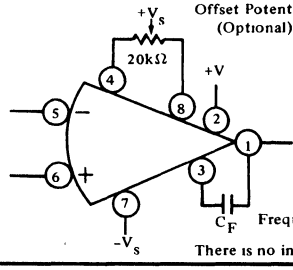


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.300	.400	7.62	10.16
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.583 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

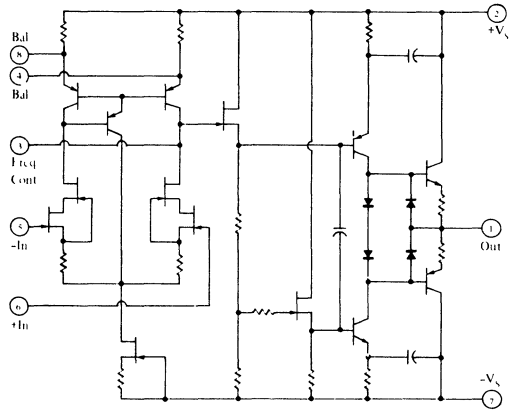
Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

NOTE
Leads in true position within .010 (.25mm) R @ MMC at seating plane
Pin numbers shown for reference only
Numbers may not be marked on package

AMPLIFIER CONNECTIONS



There is no internal case connection.



APPLICATIONS INFORMATION

WIRING PRECAUTIONS

The 3554 is a wideband, high frequency operational amplifier that has a gain-bandwidth product exceeding 1 Gigahertz. The full performance capability of this amplifier will be realized by observing a few wiring precautions and high frequency techniques.

Of all the wiring precautions, grounding is the most important and is described in an individual section. The mechanical circuit layout also is very important. All circuit element leads should be as short as possible. All printed circuit board conductors should be wide to provide low resistance, low inductance connections and should be as short as possible. In general, the entire physical circuit should be as small as practical. Stray capacitances should be minimized especially at high impedance nodes such as the input terminals of the amplifier. Pin 5, the inverting input, is especially sensitive and all associated connections must be short. Stray signal coupling from the output to the input or to pin 8 should be minimized. A recommended printed circuit board layout is shown with the "Typical Circuits." It also may be used for test purposes as described below.

When designing high frequency circuits low resistor values should be used; resistor values less than 5.6kΩ are recommended. This practice will give the best circuit performance as the time constants formed with the circuit capacitances will not limit the performance of the amplifier.

GROUNDING

As with all high frequency circuits a ground plane and good grounding techniques should be used. The ground plane should connect all areas of the pattern side of the printed circuit board that are not otherwise used. The ground plane provides a low resistance, low inductance common return path for all signal and power returns. The ground plane also reduces stray signal pick up. An example of an adequate ground plane and good high frequency techniques is the Settling Time Test Circuit Layout shown with the "Typical Circuits."

Each power supply lead should be bypassed to ground as near as possible to the amplifier pins. A combination of a 1μF tantalum capacitor in parallel with a 470pF ceramic capacitor is a suitable bypass.

In inverting applications it is recommended that pin 6, the noninverting input, be grounded rather than being connected to a bias current compensating resistor. This assures a good signal ground at the noninverting input. A slight offset error will result; however, because the resistor values normally used in high frequency circuits are small and the bias current is small, the offset error will be minimal.

If point-to-point wiring is used or a ground plane is not, single point grounding should be used. The input signal return and the load signal return and the power supply common should all be connected at the same physical point. This will eliminate any common current paths or ground loops which could cause signal modulation or unwanted feedback.

It is recommended that the case of the 3554 not be grounded during use (it may, if desired). A grounded case will add a slight capacitance to each pin. To an already functional circuit, grounding the case will probably require slight compensation readjustment and the compensation capacitor values will be slightly different from those recommended in the typical performance curves. There is no internal connection to the case.

Proper grounding is the single most important aspect of high frequency circuitry.

GUARDING

The input terminals of the 3554 may be surrounded by a guard ring to divert leakage currents from the input terminals. This technique is particularly important in low bias current and high input impedance applications. The guard, a conductive path that completely surrounds the two amplifier inputs, should be connected to a low impedance point which is at the input signal potential. It blocks unwanted printed circuit board leakage currents from reaching the input terminals. The guard also will reduce stray signal coupling to the input.

In high frequency applications guarding may not be desirable as it increases the input capacitance and can degrade performance. The effects of input capacitance, however, can be compensated by a small capacitor placed across the feedback resistor. This is described further in the following section.

COMPENSATION

The 3554 uses external frequency compensation so that the user may optimize the bandwidth or slew rate or settling time for his particular application. Several typical performance curves are provided to aid in the selection of the correct compensation capacitance value. In addition several typical circuits show recommended compensation in different applications.

The primary compensation capacitor, C_F, is connected between pins 1 and 3. As the performance curves show, larger closed-loop gain configurations require less capacitance and an improved gain-bandwidth product will be realized. Note that no compensation capacitor is required for closed-loop gains above 55V/V and when the load capacitance is less than 100pF.

When driving large capacitive loads, 470pF and greater,

an additional capacitor, C_8, is connected between pin 8 and ground. This capacitor is typically 1000pF. It is particularly necessary in low closed loop voltage gain configurations. The value may be varied to optimize performance and will depend upon the load capacitance value. In addition, the performance may be optimized by connecting a small resistance in series with the output and a small capacitor from pin 1 to 5. See the "Typical Circuits" for the X10 Inverter.

The flat high frequency response of the 3554 may be preserved and any high frequency peaking avoided by connecting a small capacitor in parallel with the feedback resistor. This capacitor will compensate for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier, typically 2pF, and the input and feedback resistors. Using small resistor values will keep the break frequency of this zero sufficiently high, avoiding peaking and preserving the phase margin. Resistor values less than 5.6kΩ are recommended. The selected compensation capacitor may be a trimmer, a fixed capacitor or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. It will typically be 2pF for a clean layout using low resistances (1kΩ) and up to 10pF for circuits using larger resistances.

SETTLING TIME

Settling time is truly a complete dynamic measure of the 3554's total performance. It includes the slew rate time, a large signal dynamic parameter, and the time to accurately reach the final value, a small signal parameter that is a function of bandwidth and open loop-gain. The settling time may be optimized for the particular application by selection of the closed-loop gain and the compensation capacitance. The best settling time is observed in low closed-loop gain circuits. A performance curve shows the settling time to three different error bands.

Settling time is defined as the total time required, from the signal input step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the magnitude of the output transition.

SLEW RATE

Slew rate is primarily an output, large signal parameter. It has virtually no dependence upon the closed-loop gain or the bandwidth, per se. It is dependent upon compensation. Decreasing the compensation capacitor value will increase the available slew rate as shown in the performance curve. Stray capacitances may appear to the amplifier as compensation. To avoid limiting the slew rate performance, stray capacitances should be minimized.

CAPACITIVE LOADS

The 3554 will drive large capacitive loads (up to 1000pF) when properly compensated. See the section on "Compensation." The effect of a capacitive load is to decrease the phase margin of the amplifier. With compensation the amplifier will provide stable operation even with large capacitive loads.

The 3554 is particularly well suited for driving 50Ω loads connected via coaxial cables due to its ±100mA output drive capability. The capacitance of the coaxial cable, 29pF/foot of length for RG-58, does not load the amplifier when the coaxial cable or transmission line is terminated in the characteristic impedance of the transmission line.

OFFSET VOLTAGE ADJUSTMENT

The offset voltage of the 3554 may be adjusted to zero by connecting a 20kΩ linear potentiometer between pins 4 and 8 with the wiper connected to the positive supply. A small, noninductive potentiometer is recommended. The leads connecting the potentiometer to pins 4 and 8 should be extremely short to avoid stray capacitance and stray signal pickup. Stray coupling from the output, pin 1, to pin 4 (negative feedback) or to pin 8 (positive feedback) should be avoided or oscillation may occur.

The potentiometer is optional and may be omitted when the guaranteed offset voltage is considered sufficiently low for the particular application.

For each microvolt of offset voltage adjusted, the offset voltage temperature drift will change by ±0.004μV/°C.

HEAT SINKING

The 3554 does not require a heat sink for operation in most environments. The use of a heat sink, however, will reduce the internal thermal rise and will result in cooler operating temperatures. At extreme temperature and under full load conditions a heat sink will be necessary as indicated in the "Maximum Power Dissipation" curve. A heat sink with 8 holes for the 8 amplifier pins should be used. Burr-Brown has heat sinks available in three sizes - 3°C/W, 4.2°C/W and 12°C/W. A separate product data sheet is available upon request.

When heat sinking the 3554, it is recommended that the heat sink be connected to the amplifier case and the combination not connected to the ground plane. For a single-sided printed circuit board, the heat sink may be mounted between the 3554 and the nonconductive side of the PC board, and insulating washers, etc., will not be required. The addition of a heat sink to an already functional circuit will probably require slight compensation readjustment for optimum performance due to the change in stray capacitances. The added stray capacitance from the heat sink to each pin will depend on the thickness and type of heat sink used.

SHORT CIRCUIT PROTECTION

The 3554 is short circuit protected for continuous output shorts to common. Output shorts to either supply will destroy the device, even for momentary connections. Output shorts to other potential sources are not recommended as they may cause permanent damage.

TESTING

The 3554 may be tested in conventional operational amplifier test circuits; however, to realize the full performance capabilities of the 3554, the test fixture must not limit the full dynamic performance capability of the amplifier. High frequency techniques must be employed. The most critical dynamic test is for settling time. The 3554 Settling Time Test Circuit Schematic and a test circuit layout is shown with the "Typical Circuits." The input pulse generator must have a flat topped, fast settling pulse to measure the true settling time of the amplifier. The layout exemplifies the high frequency considerations that must be observed. The layout also may be used as a guide for other test circuits. Good grounding, truly square drive signals, minimum stray coupling and small physical size are important.

Every 3554 is thoroughly tested prior to shipment assuring the user that all parameters equal or exceed their specifications.

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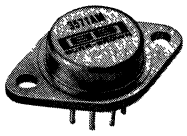
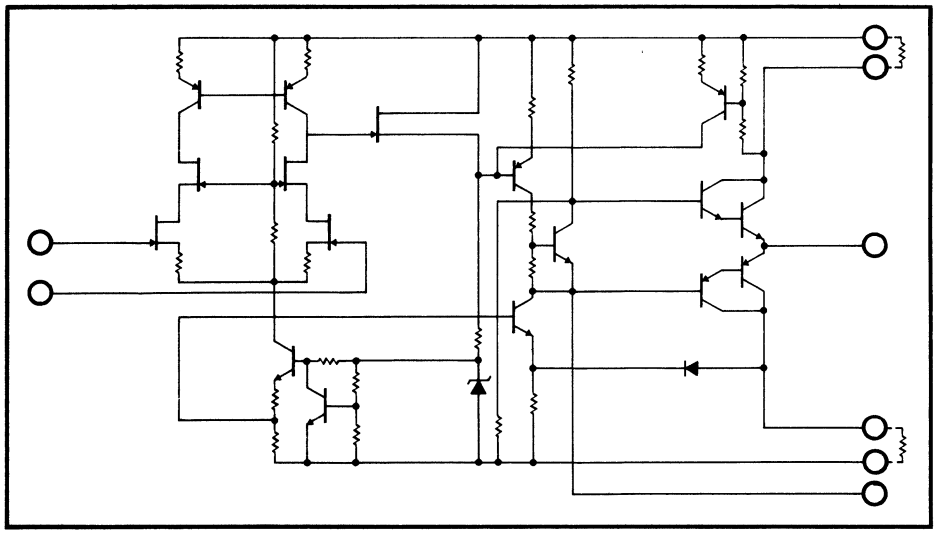


3571
3572

High Current — High Power OPERATIONAL AMPLIFIERS

FEATURES

- HIGH CURRENT
  Up to 5A Peak, 2A Continuous
- EASY TO USE
  Adjustable Current Limits
  Electrically Isolated Case
  Small Size — 8-Pin TO-3 Package
- HIGH VOLTAGE
  Up to 70V p-p Output
- SELF-PROTECTED
  Self-Contained Automatic Thermal Sensing and Shutdown
- HIGH POWER
  Delivers up to 70W to Load



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PDS-334C

DESCRIPTION

The 3571AM and 3572AM are high output current integrated circuit operational amplifiers. Their performance, ease of use and compact size make them ideal to use in a variety of high current applications. They are especially well suited for driving permanent magnet DC servo and torque motors.

The equivalent circuit for the 3571AM and 3572AM is shown in Figure 1. The design uses a monolithic FET input stage for high input impedance, low bias current, and low voltage drift versus temperature. The high input impedance provides negligible source impedance loading errors when the noninverting circuit configuration is used. The low bias currents minimize offset errors when large values of source and feedback resistors are used.

The input offset voltage at 25°C and the input offset voltage drift versus temperature are compensated by state-of-the-art laser trimming techniques. The offset voltage is low enough so that trimming will not be required in most applications. The excellent input characteristics and the high gain available mean that the use of a preamplifier, sometimes required with other servo type amplifiers, will not be necessary with the 3571AM and 3572AM.

The output stage is a class AB design which provides low distortion and minimizes quiescent current drain. The output circuitry provides for external current limiting resistors for both positive and negative output currents. This allows the user to select the current limit value suited to his particular application. This is especially desirable for driving permanent magnet motors where the high current seen during direction reversal (plugging) can demagnetize the motor.

The 3571AM and 3572AM have been designed to operate over a relatively wide supply range (±15VDC to ±40VDC) while still maintaining the high output current capability. This allows the user a wide range for the selection of the proper output voltage and current and makes the amplifiers useful for many different types of loads.

The output circuit has a unique protection feature which is practical only in integrated circuit amplifiers - self-contained automatic thermal-sensing and shut-off circuitry which automatically turns the amplifier off when the internal temperature reaches approximately 150°C. This is accomplished by sensing the substrate temperature and deactivating the amplifiers biasing network when the temperature reaches 150°C. As this happens, the output load current limits at a safe value and the amplifier's quiescent current decreases. The output current may remain at a low value or oscillate between two values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal load condition is removed.

Internal thermal protection removes some of the constraints of power derating for abnormal operating conditions. The amplifier will protect itself for many conditions of excess power dissipation (see Power Derating Curve). This allows the use of a smaller heat sink to protect against abnormal output conditions since the amplifier has its own internal protection for many conditions of excess power dissipation. The output constraints of the Safe Operating Area Curves must still be observed.

The 3571AM and 3572AM have several other features that improve their utility. For instance, the metal case of the units is completely electrically isolated. (This can be contrasted to most power semiconductors where the case is connected to the collector of the device.) This simplifies mounting and reduces cost because the need for insulating spacers and bushings is eliminated. The hermetically sealed package improves reliability and will withstand severe environments better than discrete component amplifiers. The small package size makes mounting more convenient.

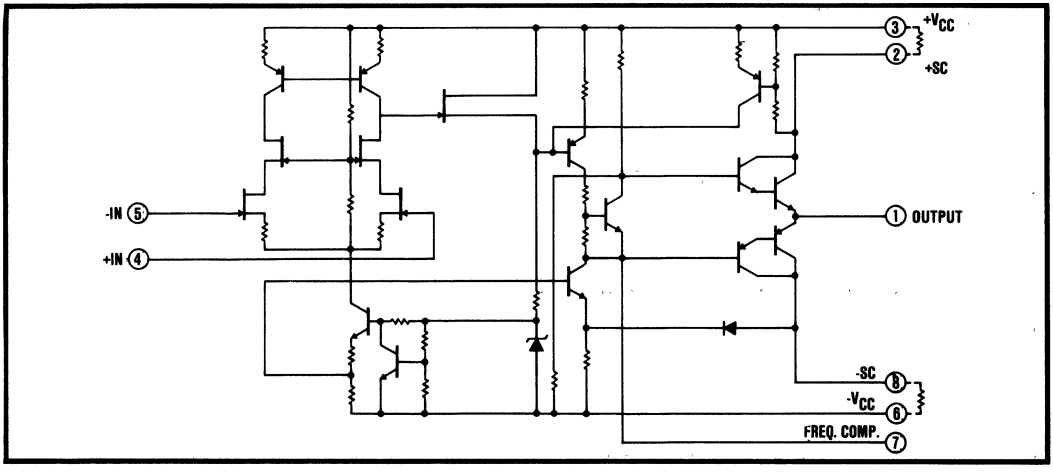


FIGURE 1. Equivalent Circuit

SPECIFICATIONS

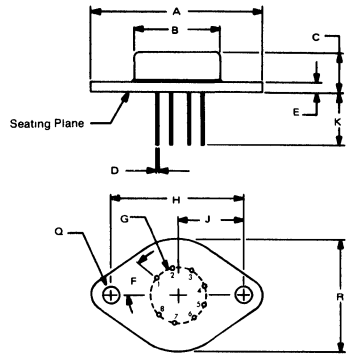
ELECTRICAL

Typical at T_{case} = 25°C and ±V_{CC} = ±35VDC max unless otherwise noted.

MODELS	3571AM	3572AM
RATED OUTPUT (to load)		
Power to Load		
Continuous, min(1)	30W	60W
Peak, min(1)	60W	150W
Output Voltage, ±(|V_{CC}|-5)V		
Continuous, min(1)	±30V at ±1A	±30V at ±2A
Peak, min(1)	±30V at 2A	±30A at 5A
Load Capacitance, min. C_C = 0	3300pF	
C_C = 1000pF	15µF	
DISSIPATION RATING		
At 25°C Case Temperature	33W	50W
Derating Above 25°C	See Typical Performance Curves	
Thermal Resistance, Case to Free Air	30°C/W	
Thermal Time Constant (no heat sink)	2 minutes	
Thermal Resistance, Junction to Case	2.5°C/W	
POWER SUPPLY		
Voltage, ±V_{CC}	±15VDC to ±40VDC	
Quiescent Current, max	±35mA	
OPEN LOOP		
Gain min, at R_{load} = 30Ω (3572AM)	94dB	
R_{load} = 60Ω (3571AM)		
Output Impedance	2.5Ω	
FREQUENCY RESPONSE		
Unity Gain Bandwidth, Small Signal	500kHz	
Full Power Bandwidth	16kHz at Vpk = 30V	
Slew Rate, C_C = 1000pF	3V/µsec	
INPUT OFFSET VOLTAGE		
Initial at 25°C, max	±2mV	
Drift vs Temp., max	±40µV/°C	
Drift vs. Supply Voltage	±100µV/V	
Drift vs Time	50µV/mo	
Drift vs. Power Dissipation (T_C constant)	20µV/W	
INPUT BIAS CURRENT		
Initial at 25°C, max	-100pA	
Drift vs. Temp.	doubles every 10°C	
Drift vs. Supply Voltage	0.5pA/V	
INPUT OFFSET CURRENT		
Initial at 25°C	±50pA	
Drift vs Temp	doubles every 10°C	
Drift vs. Supply Voltage	0.5pA/V	
INPUT IMPEDANCE		
Differential	10^{11}Ω || 10pF	
Common-mode	10^{11}Ω	
INPUT NOISE		
Voltage 0.01Hz to 10Hz, p-p	4µV	
10Hz to 1kHz, rms	3µV	
Current 0.01Hz to 10Hz, p-p	1pA	
10Hz to 1kHz, rms	0.1pA	
INPUT VOLTAGE RANGE		
Max Safe Differential Voltage	(+V_{CC} + | -V_{CC} |)	
Max Safe Common-mode Voltage	+V_{CC} to -V_{CC}	
Common-mode Voltage, Linear Operation	±(|V_{CC}| -10)V	
Common-mode Rejection	80dB min., 90dB, typ	
TEMPERATURE RANGE (Case)		
Specification	-25°C to +85°C	
Operating	-55°C to +125°C	
Storage	-55°C to +125°C	

NOTE:
1. Safe Operating Area and Power Derating limitations must be observed.

MECHANICAL



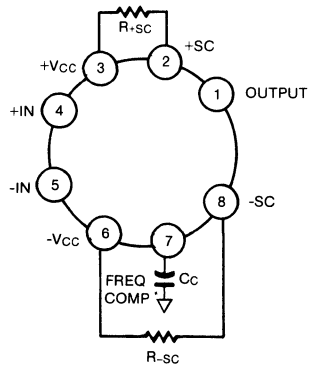
NOTE
Leads in true position within 0.010" 0.25mm · R at MMC at seating plane

Pin numbers shown for reference only
Numbers may not be marked on package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.300	.400	7.62	10.16
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

CONNECTION DIAGRAM

(TOP VIEW)



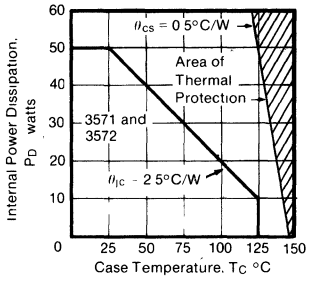
The case is electrically isolated It is recommended that the case be grounded during use

*A 1000pF ±20% ceramic capacitor is recommended for all circuit configurations and at all amplifier gains The capacitor's lead lengths should be short For gains above 10V/V, C_C is not absolutely required but is recommended

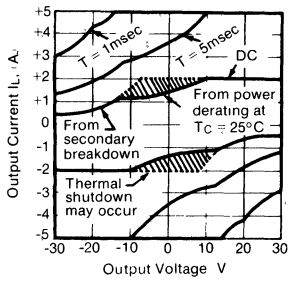
TYPICAL PERFORMANCE CURVES

Typical T_{case} = 25°C and $\pm V_{CC}$ = ±35VDC unless otherwise noted

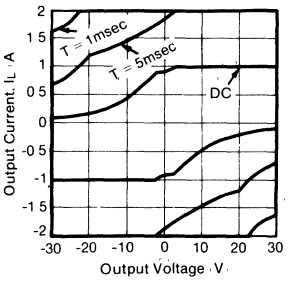
POWER DERATING



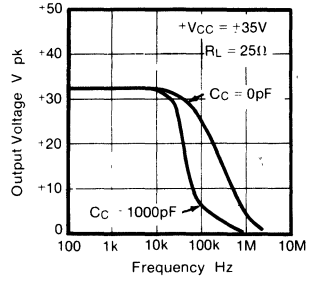
3572 SAFE OPERATING AREA



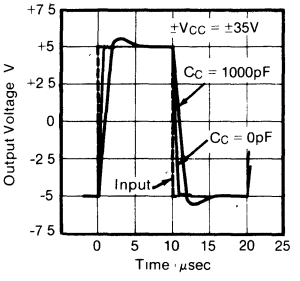
3571 SAFE OPERATING AREA



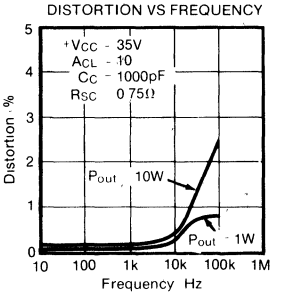
OUTPUT VOLTAGE VS FREQUENCY



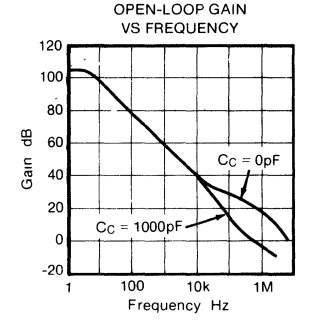
VOLTAGE FOLLOWER PULSE RESPONSE



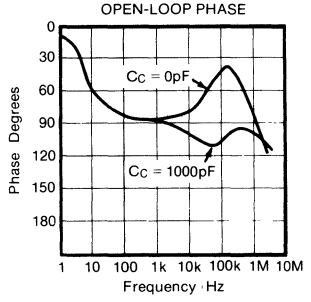
DISTORTION VS FREQUENCY



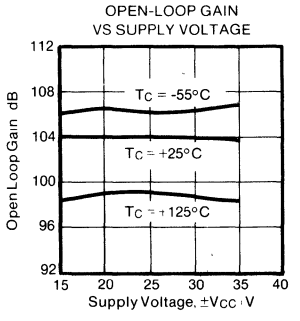
OPEN-LOOP GAIN VS FREQUENCY



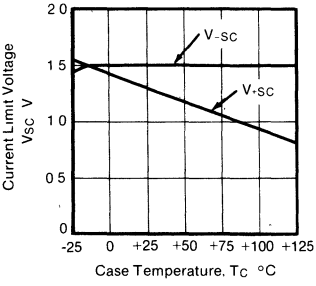
OPEN-LOOP PHASE



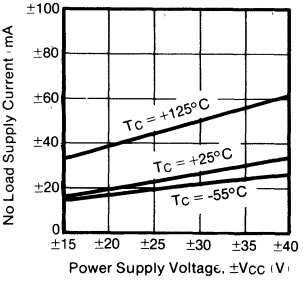
OPEN-LOOP GAIN VS SUPPLY VOLTAGE



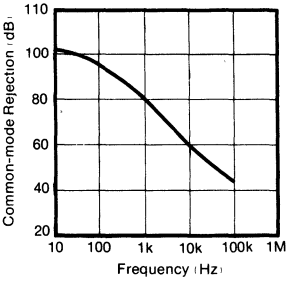
CURRENT LIMIT VOLTAGE VS TEMPERATURE



QUIESCENT CURRENT VS SUPPLY VOLTAGE



COMMON-MODE REJECTION VS FREQUENCY



INSTALLATION AND OPERATING INSTRUCTIONS

GENERAL PRECAUTIONS

Current Limiting

It is recommended that during initial amplifier setup, particularly in breadboarding and when a lack of familiarity with the amplifier exists, that the current limit be set at about 250mA ($R_{sc} \cong 5.6\Omega$). This will allow verification of the circuit and will minimize the possibility of damaging the amplifier. Later, when the circuit configuration and connections have been proven, the current limits can be raised to the desired value.

Minimum Heat Sink

The 3571AM and 3572AM require a minimum heat sink of 16°C W or lower in order to insure thermal stability (mounting on a 3" x 3" x 0.06" piece of 80% copper-clad printed circuit board material will be sufficient). Normally this will not be a consideration since a larger heat sink will be used to provide the proper power dissipation as described in the Thermal Considerations section which follows.

Proper Grounding and Power Supply Bypassing

Particular attention should be given to proper grounding practices because the large output currents can cause significant grounding-loop errors. Proper connections are shown in Figure 2.

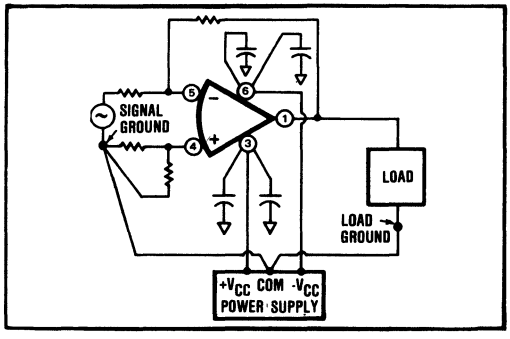


FIGURE 2. Proper Power Supply Connections.

Note that the connections are such that the load current does not flow through the wire connecting the signal ground point to the power supply common. Also, power supply and load leads should be physically separated from the amplifier input and signal leads.

The amplifier power supply should be bypassed with 50μF tantalum capacitors connected in parallel with 0.01μF ceramic capacitors connected as close to pins 3 and 6 as possible. The capacitors should be connected to the load ground rather than the signal ground.

CURRENT LIMITS

The amplifiers are designed so that both the positive and negative load current limits can be adjusted with external resistors, R_{+SC} and R_{-SC} respectively. The value of the resistors are given by the following equations:

$$R_{+SC} = \frac{1.3\ (\text{volts})}{I_{+limit}(\text{amps})},\quad R_{-SC} = \frac{1.5\ (\text{volts})}{I_{-limit}(\text{amps})}$$

I_{limit} is the desired maximum current. The maximum power dissipation of the resistors is $P_{max} = R_{sc}\ (I_{limit})^2$. The current limits determined by the equations above are accurate to about ±10%. The variation of I_{limit} versus temperature is shown in the Typical Performance Curves. Both $+V_{cc}$ and $-V_{cc}$ must be on for the current limits to function.

To avoid introducing unwanted inductance into the current limit circuitry, which may introduce oscillations and permanent damage, both current limit resistors must be noninductive. Do not use wire wound resistors. Carbon composition resistors are preferred and paralleling them can provide a wide current limit range at the wattage needed.

The maximum value of the negative current limit resistor is 15Ω (100mA, min). Exceeding this value, or an open circuit, could permanently damage the internal 75Ω, thin-film resistor which parallel R_{-SC}.

The amplifier should be used with as low a current limit as possible for the particular application. This will minimize the chance of damaging the amplifier under abnormal load conditions and increase reliability by limiting the internal power dissipation of the amplifier.

THERMAL CONSIDERATIONS

The 3571AM and 3572AM are rated for 150°C maximum junction temperature. The thermal resistance from junction to case (θ_{jc}) is 2.5°C W. The corresponding Power Derating Curve is given in the Typical Performance Curves.

The internal power dissipation of the amplifier is given by the equation $P_D = P_{DQ} + P_{DI}$ where P_{DQ} is the quiescent power dissipation and P_{DI} is the power dissipated in the output stage due to the load. (For $\pm V_{cc} = \pm 40V$, $P_{DQ} = 80 \times 0.035 = 2.8W$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{out}$) the maximum value of P_{DI} occurs at $\pm V_{out} = \pm V_{cc}/2$ and is equal to $P_{DI\ max} = (\pm V_{cc})^2/4R_L$. Figure 3 shows P_D as function of the output voltage with the load resistance as a running parameter.

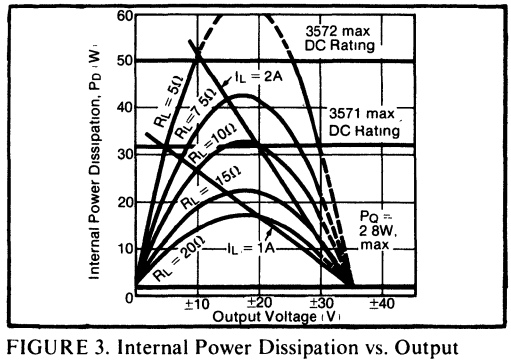


FIGURE 3. Internal Power Dissipation vs. Output Voltage.

P_{DI} for any other value of V_{out} can be computed from

$$P_{DI} = (\pm V_{CC} - \pm V_{out}) \cdot I_L = (\pm V_{CC} - \pm V_{out}) \left(\frac{\pm V_{out}}{R_L} \right)$$

The use of an adequate heat sink is mandatory and thermal resistance of the heat sink (θ_{hs}) can be determined from the equation:

$$\theta_{hs} = (T_J - T_A / P_D) - \theta_{jc}$$

where T_J is the desired amplifier junction temperature (+150°C, max), T_A is the ambient temperature, P_D is the amplifiers dissipation, $P_D = P_{DO} + P_{DI}$, and θ_{jc} is the junction to case thermal resistance of the amplifier. Burr-Brown Application Note AN-83 entitled, "How to Determine What Heat Sink to Use", is available for additional information.

The electrically isolated case of the 3571AM and 3572AM simplifies mounting the amplifiers to the heat sink (and the heat sink to any other assemblies) since there is no need for electrical insulation. Thermal joint compound and lock washers should be used to prevent mechanical relaxation due to thermal stresses.

Safe Operating Area

There are additional constraints on the output voltage and current other than those just due to the maximum internal power dissipation of the amplifiers. These are related to the prevention of secondary breakdown in the output stage transistors. These restrictions are shown in the Safe Operating Area Curves in the Typical Performance Curves.

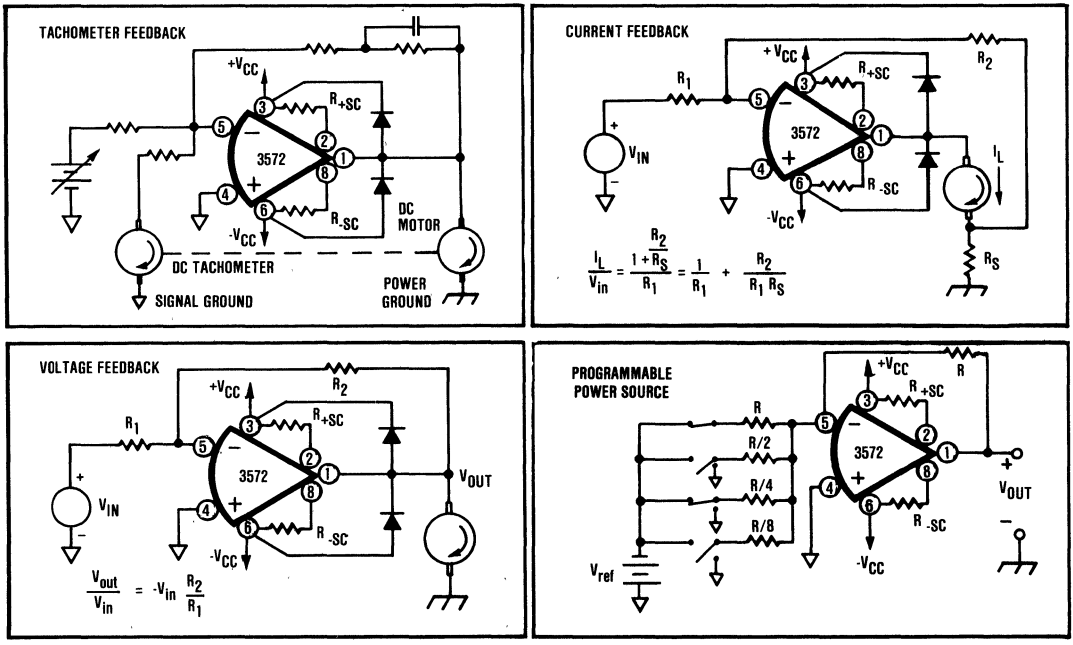
Application Constraint

Because of the possibility of damaging the output stage if frequency instability (oscillations) occurs, applications with an inductive load which will activate the current limit of the amplifier, are limited to a load impedance phase angle of less than 60°C leading, over the frequency band of 10kHz to 100kHz. Increasing the load's series resistance will decrease the angle, if necessary. Larger inductive loads may be applied if current limit is not activated.

Frequency Compensation

The optimum value of the compensation capacitor is 1000pF. A ±20% tolerance ceramic capacitor is recommended. The compensation capacitor should be used with all circuit configurations and at all amplifier gains (see note on Connection Diagram).

TYPICAL APPLICATIONS



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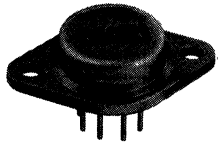
3573



High Current - High Power OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT POWER
  100 Watts Peak
  40 Watts Continuous
- WIDE SUPPLY RANGE
  ±10 to ±34 Volts
- HIGH OUTPUT CURRENT
  ±5 Amps Peak
  ±2 Amps Continuous
- SMALL SIZE: TO-3 PACKAGE
- LOW COST

APPLICATIONS

- DC MOTORS
- AC MOTORS
- ACTUATORS
- ELECTRONIC VALVES
- SYNCROS

DESCRIPTION

If you need to supply 100 watts peak or 40 watts continuous, yet must choose a small, easy to use op amp, you'll find the 3573 a logical solution. This hybrid IC delivers ±5A peak minimum at ±20V minimum to the load when operated from ±28V power supplies. The design of this op amp has been optimized for low cost while preserving moderately good input and distortion characteristics.

Output circuitry provides for external current limiting resistors for both positive and negative currents. This allows current limits to be set to values dictated by the op amp's application. 3573 is internally frequency compensated and is unconditionally stable with capacitive loads to 3300pF.

Housed in a small, rugged, hermetically sealed 8-lead TO-3 package, 3573 will withstand severe environments far better than discrete component amplifiers. The metal case is completely electrically isolated from the amplifier circuitry. Thus, mounting is easier (no isolation washers or spacers) and the hazards of a case connected to the output or supply voltage is eliminated.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex. 66-6491

PDS-393B

ELECTRICAL SPECIFICATIONS

At T_{Case} = 25°C and $\pm V_{CC}$ = ±28VDC unless otherwise noted.

PARAMETER	CONDITIONS	3573AM MIN	3573AM TYP	3573AM MAX	UNITS
OPEN LOOP GAIN, DC	$R_L \geq 30\Omega$	94	115		dB
RATED OUTPUT					
Power to Load[1]					
Continuous		40			W
Peak		100			W
Output Current					
Continuous		±2			A
Peak		±5			A
Output Voltage	$I_{out} = \pm 5A$[4]	±20	±23		V
DYNAMIC RESPONSE					
Bandwidth, Unity Gain	Small Signal		1		MHz
Full Power Bandwidth		15	23		kHz
Slew Rate		1 35	1.5		V μs
INPUT OFFSET VOLTAGE					
Initial Offset			±5	±10	mV
vs Temperature	-25°C ≤ T_{case} ≤ 85°C		±10	±65	μV °C
vs Supply Voltage			±35		μV/V
INPUT BIAS CURRENT					
Initial	T_{case} = 25°C		15	40	nA
vs Temperature			±0.05		nA °C
vs Supply Voltage			±0 02		nA V
INPUT DIFFERENCE CURRENT					
Initial	T_{case} = 25°C		±5	±10	nA
vs Temperature	-25°C ≤ T_{case} ≤ 85°C		±0.01		nA °C
INPUT IMPEDANCE					
Differential			10		MΩ
Common-mode			250		MΩ
INPUT NOISE					
Voltage Noise	f_n = 0 3Hz to 10Hz		3		μV p-p
	f_n = 10Hz to 10kHz		5		μVrms
Current Noise	f_n = 0 3Hz to 10Hz		20		pA p-p
	f_n = 10Hz to 10kHz		4 5		pA rms
INPUT VOLTAGE RANGE					
Common-mode Voltage	Linear Operation	±(|V_{CC}|-6)	±(|V_{CC}|-3)		V
Common-mode Rejection	f = DC, V_{CM} = ±22	70	110		dB
POWER SUPPLY					
Rated Voltage			±28		V
Voltage Range, derated		±10		±34	V
Current, quiescent			±2.6	±5	mA
TEMPERATURE RANGE					
Specification		-25		+85	°C
Operating,derated performance		-25		+85	°C
Storage		-65		+150	°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range	±34VDC
Internal Power Dissipation[1]	45W
Differential Input Voltage[2]	±62VDC
Input Voltage Range[2]	±31VDC
Storage Temperature Range	-65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C
Output Short-Circuit Duration[3]	Continuous
Junction Temperature	150°C

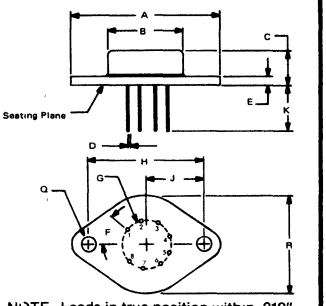
1 Package must be derated based on a junction to case thermal resistance of 2 8°C/W, or a junction to ambient thermal resistance of 30°C/W.

2. For supply voltages less than ±34VDC, the absolute maximum voltage is three volts less than supply voltage

3. Safe Operating Area and Power Derating Curves must be observed

4. With R±SC = 0.

MECHANICAL

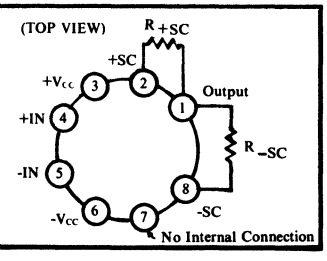


NOTE. Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1 510	1 550	38 35	39 37
B	745	770	18 92	19 56
C	260	300	6 60	7 62
D	038	042	0 97	1 07
E	080	105	2 03	2 67
F	40° BASIC		40° BASIC	
G	500 BASIC		12 7 BASIC	
H	1 186 BASIC		30.12 BASIC	
J	593 BASIC		15 06 BASIC	
K	400	500	10 16	12.70
Q	151	.161	3.84	4 09
R	980	1 020	24 89	25 91

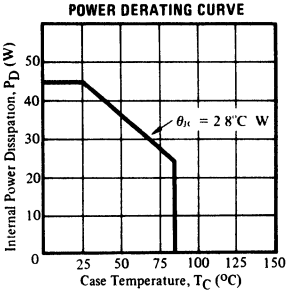
CONNECTION DIAGRAM



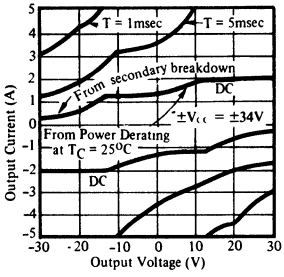
TYPICAL PERFORMANCE CURVES

(Typical at 25°C case and $\pm V_{CC}$ = ±28 VDC unless otherwise noted.)

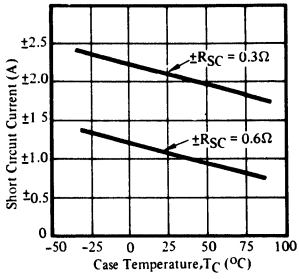
POWER DERATING CURVE



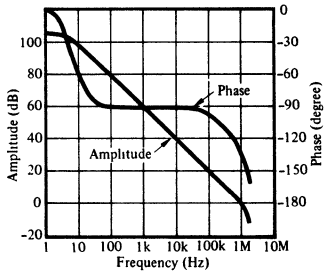
SAFE OPERATING AREA



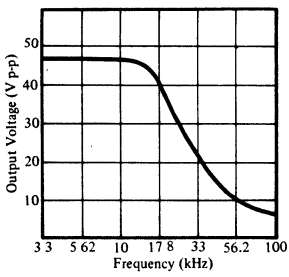
CURRENT LIMITING



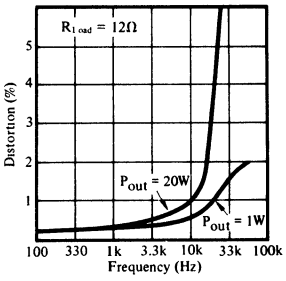
OPEN LOOP FREQUENCY RESPONSE



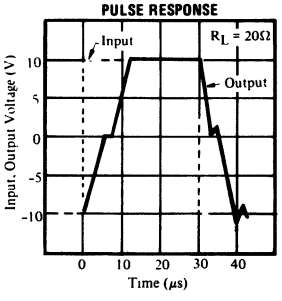
OUTPUT VOLTAGE VS FREQUENCY



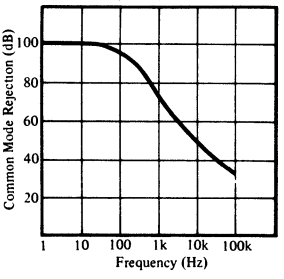
HARMONIC DISTORTION



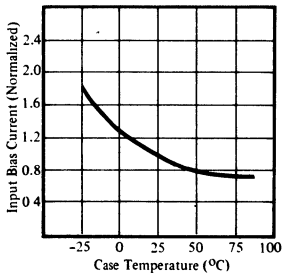
VOLTAGE FOLLOWER PULSE RESPONSE



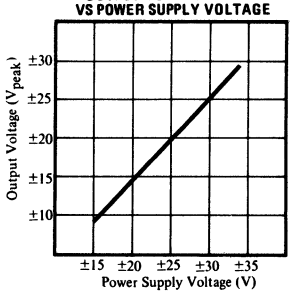
COMMON MODE REJECTION VS FREQUENCY



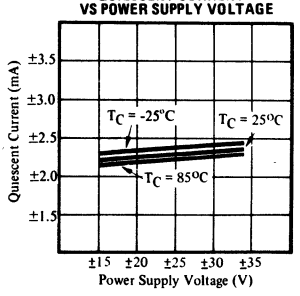
INPUT BIAS CURRENT VS TEMPERATURE



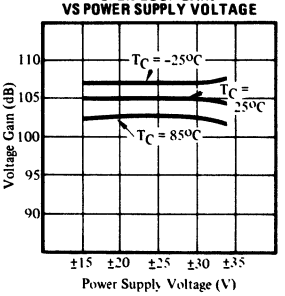
OUTPUT VOLTAGE SWING VS POWER SUPPLY VOLTAGE



QUIESCENT CURRENT VS POWER SUPPLY VOLTAGE



OPEN LOOP GAIN VS POWER SUPPLY VOLTAGE



INSTALLATION AND OPERATING INSTRUCTIONS

GENERAL PRECAUTIONS

CURRENT LIMITING

It is recommended that during initial amplifier setup, particularly in breadboarding and when a lack of familiarity with the amplifier exists, that the current limit be set at about 250mA ($R_{SC} \cong 2.6\Omega$). This will allow verification of the circuit and will minimize the possibility of damaging the amplifier. Later, when the circuit configuration and connections have been proven, the current limits can be raised to the desired value.

PROPER GROUNDING & POWER SUPPLY BYPASSING

Particular attention should be given to proper grounding practices because the large output currents can cause significant ground loop errors. Figure 1 illustrates proper connections.

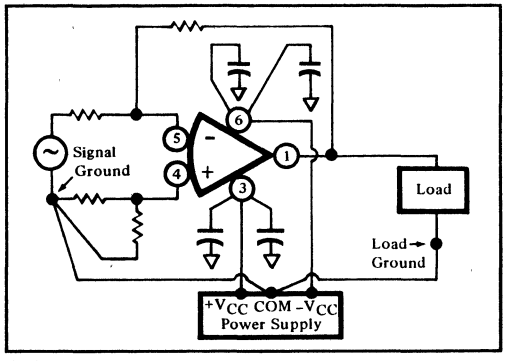


FIGURE 1. Proper Power Supply Connections.

Note that the connections are such that the load current does not flow through the wire connecting the signal ground point to the power supply common. Also, power supply and load leads should be run physically separated from the amplifier input and signal leads.

The amplifier should be power supply bypassed with 50μF tantalum capacitors connected in parallel with 0.01 μF ceramic capacitors connected as close to pins 3 and 6 as possible. The capacitors should be connected to the load ground rather than the signal ground.

CURRENT LIMITS

The amplifier is designed so that both the positive and negtive load current limits can be adjusted with external resistors, R_{+SC} and R_{-SC} respectively. The value of the resistors are given by the following equation:

$$R_{SC} = \frac{0.65 \text{ (volts)}}{I_{limit} \text{ (amps)}}$$

I_{limit} is the desired maximum current. The maximum power dissipation of the resistors is $P_{max} = R_{SC} (I_{limit})^2$. The current limits determined by the equations above are accurate to about ±10%. The variation of I_{limit} vs temperature is shown in the Typical Performance Curves.

The amplifier should be used with as low a current limit as possible for the particular application. This will minimize the chance of damaging the amplifier under abnormal load conditions and increase reliability by limiting the internal power dissipation of the amplifier.

THERMAL CONSIDERATIONS

The 3573AM is rated for 150°C maximum junction temperature. The thermal resistance from junction to case (θ_{jc}) is 2.8°C/W per watt. The corresponding Power Derating Curve is given in the Typical Performance Curves section.

The internal power dissipation of the amplifier is given by the equation $P_D = P_{DQ} + P_{DL}$ where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipated in the output stage due to the load.

The thermal resistance of the required heat sink (θ_{hs}) can be determined from the equation:

$$\theta_{hs} = \frac{T_J - T_A}{P_D} - \theta_{jc}$$

where T_J is the desired amplifier junction temperature (+150°C max), T_A is the ambient temperature, P_D is the amplifier's dissipation, $P_D = P_{DQ} + P_{DL}$, and θ_{jc} is the junction to case thermal resistance of the amplifier.

The electrically isolated case of the 3573AM simplifies mounting the amplifiers to the heat sink (and the heat sink to any other assemblies) since there is no need for electrical insulation. Thermal joint compound and lock washers should be used to prevent mechanical relaxation due to thermal stresses.

SAFE OPERATING AREA

There are additional constraints on the output voltage and current other than those just due to the maximum internal power dissipation of the amplifiers. These are related to the prevention of secondary breakdown in the output stage transistors. These restrictions are shown in the SAFE OPERATING AREA CURVES in the Typical Performance Curves.

BURR-BROWN®

3580
3581
3582

High Voltage OPERATIONAL AMPLIFIERS

FEATURES

- HIGH OUTPUT SWINGS, up to ±145V (3582)
- LARGE LOAD CURRENTS, up to ±60mA (3580)
- DIFFICULT TO DAMAGE, automatic thermal shutoff
- REDUCES SOURCE LOADING, $10^{11}\Omega$ Input Z
- PRESERVES SYSTEM ACCURACY, 110dB CMR 20pA bias current

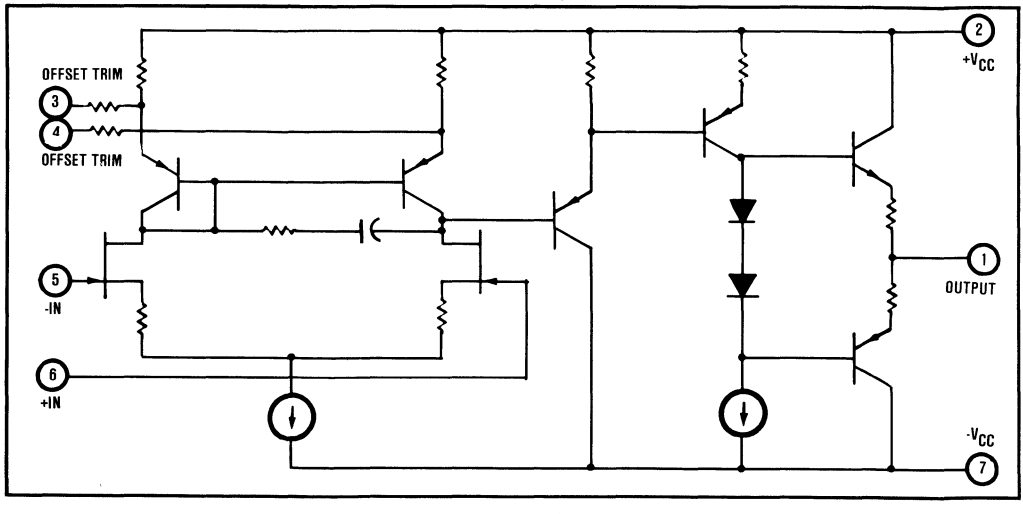
DESCRIPTION

The 3580 series is the first family of Integrated Circuit operational amplifiers which will provide output voltage swings of up to ±145V.

The monolithic FET input stage has low bias currents (20pA) which minimizes the offset voltages caused by the bias current and the large resistance normally associated with high voltage circuits.

The 3580 series is packaged in a TO-3 package which will dissipate over 3W of power without a heat sink and 4.5W with a suitable heat sink.

The input stage is protected against overvoltages and the output stage is protected against short-circuits-to-ground. A special thermal sensing circuit prevents damage to the amplifier by automatically shutting the amplifier down when too much power is being dissipated.



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PDS-313E

THEORY OF OPERATION

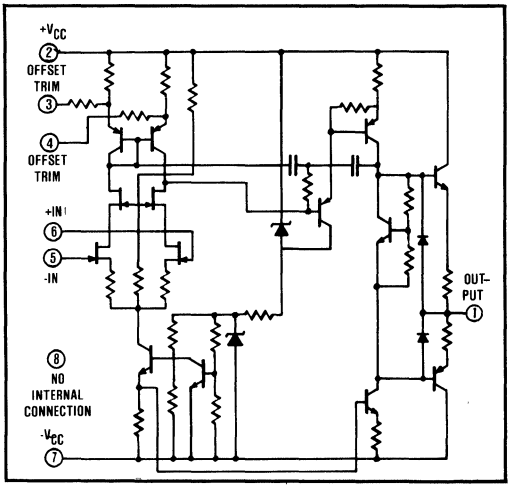


FIGURE 1. Simplifier Schematic of 3580.

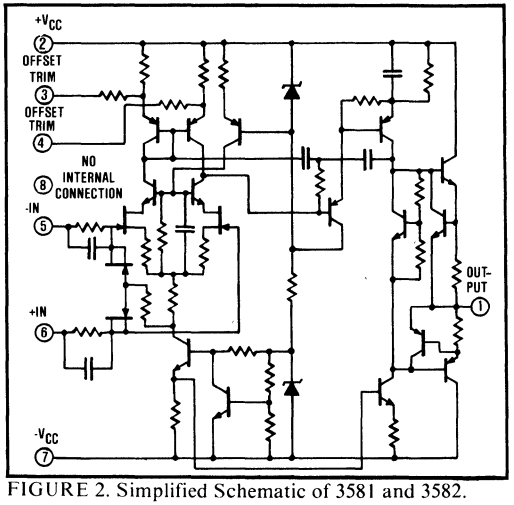


FIGURE 2. Simplified Schematic of 3581 and 3582.

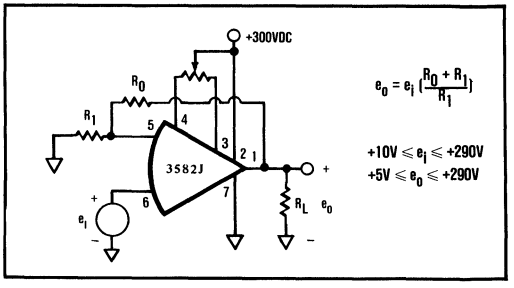


FIGURE 3. Operation from a Single Supply.

The 3580 family of integrated circuit high voltage amplifiers provides performance which previously was only available in bulky modular packages (see Figures 1 and 2). In addition to the smaller size and inherent reliability, the integrated circuit construction offers other advantages not normally available in modular or discrete component units. The amplifiers have thermal sensing and shut-off circuitry which automatically turns the amplifier off when the internal temperature reaches approximately 150°C. This is accomplished by sensing the substrate temperature and deactivating the input stage current source when the temperature reaches a critical level. As this happens, the output load current limits at a safe value and the amplifier's quiescent current decreases.

If the cause of the abnormal power dissipation is continuous (such as a short circuit across the load) the output current may remain at a low value or oscillate between two values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal condition is removed.

The incorporation of thermal sensing and shut-off in the amplifier will allow the use of a smaller heat sink than would otherwise be required. This is due to the fact that the amplifier will protect itself and does not require a massive heat sink for protection under abnormal conditions.

Another unique feature of the 3580 family is the thorough testing of the unit receiver. In addition to the normal tests, all amplifiers are 100% tested for input protection at the full rated differential voltage ($+V_{CC} - (-V_{CC})$). Each unit is also 100% tested for output short circuit to common at maximum supply voltage.

The 3581 and 3582 have a unique feature that is important in many high voltage applications. In these two models the input bias current is virtually independent of the applied common-mode voltage. This is accomplished by the true cascode input stage which keeps the drain-to-source voltage of the input transistors constant as the common-mode voltage changes.

OPERATION FROM A SINGLE SUPPLY

It may be desirable in some applications to operate the amplifiers from a single supply. The circuit in Figure 3 illustrates a typical application.

Note that there are restrictions on the input and output voltages (e_i and e_o) which are necessary in order to keep the amplifier circuits operating in a linear manner.

It should be noted that when the 3581 and 3582 amplifiers are operated from a single supply, the output stage, which is still short-circuit-current limited and thermally protected, is not protected against short circuits to ground (the 3580 will still be short circuit protected under these conditions). When the amplifiers are operated from a single supply, the voltage across one of the output transistors is high enough that secondary breakdown is a consideration. The output current must be limited in order to prevent damage. This can be done by keeping the load resistor larger than 5kΩ for the 3582 and greater than 1kΩ for the 3581.

SPECIFICATIONS

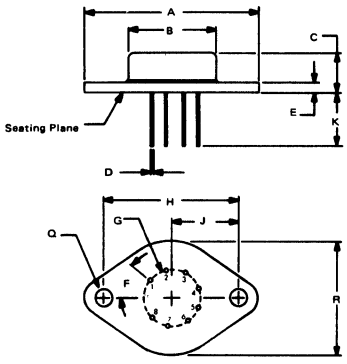
ELECTRICAL

Typical at T_{CASE} = +25°C max unless otherwise noted

MODELS	3580J	3581J	3582J
POWER SUPPLY			
Voltage, $\pm V_{CC}$	±15VDC to ±35VDC	±32VDC to ±75VDC	±70VDC to ±150VDC
Quiescent Current, max	±10mA	±8mA	±6 5mA
RATED OUTPUT			
Voltage, + |V_{CC}| -5 VDC, min	±10VDC to ±30VDC	±27VDC to ±70VDC	±65VDC to +145VDC
Current, min	±60mA	±30mA	+15mA
Current, Short Circuit	±100mA	±50mA	±25mA
Load Capacitance, max		10nF	
OPEN-LOOP GAIN			
No Load, DC	106dB	112dB	118dB
Rated Load, DC, min	86dB	94dB	100dB
FREQUENCY RESPONSE			
Unity Gain Bandwidth, Small Signal		5MHz, min	
Full Power Bandwidth	100kHz	60kHz	30kHz
Slew Rate	15V/μs	20V/μs	20V/μs
Settling Time, 0 1%		12μs	
INPUT OFFSET VOLTAGE			
Initial at T_{CASE} = +25°C, max	±10mV	±3mV	±3mV
Drift vs Temp, max	±30μV/°C	±25μV/°C	±25μV/°C
Drift vs Supply Voltage	100μV/V	20μV/V	20μV/V
Drift vs Time	100μV/mo	50μV/mo	50μV/mo
INPUT BIAS CURRENT			
Initial at T_{CASE} = +25°C max	-50pA	-20pA	-20pA
Drift vs Temp		doubles every 10°C	
Drift vs Supply Voltage	0 5pA/V	0 2pA/V	0 2pA/V
INPUT OFFSET CURRENT			
Initial at T_{CASE} = +25°C, max		±20pA	
Drift vs Temp		doubles every 10°C	
Drift vs Supply Voltage	0 5pA/V	0 2pA/V	0 2pA/V
INPUT IMPEDANCE			
Differential		$10^{11}\Omega$ 10pF	
Common-mode		$10^{11}\Omega$	
INPUT NOISE			
Voltage 0 01Hz to 10Hz, p-p		5μV	
10Hz to 1kHz, rms	1μV	1 7μV	1.7μV
Current 0 01Hz to 10Hz, p-p	1pA	0 3pA	0.3pA
INPUT VOLTAGE RANGE			
Max Safe Differential Voltage(1)		+V_{CC} + |-V_{CC}|	
Max Safe Common-mode Voltage		+V_{CC} to -V_{CC}	
Common-mode Voltage, Linear Operation	+ |V_{CC}| -8 V	± |V_{CC}| -10 V	± |V_{CC}| -10 V
Common-mode Rejection	86dB	110dB	110dB
TEMPERATURE Case			
Specification		0°C to 70°C	
Operating		-55°C to +125°C	
Storage		-55°C to +150°C	

NOTE
1 On Models 3581 and 3582 the inputs may be damaged by pulses at pins 5 or 6 with dV/dt≥1V/ns| Any possible damage can be eliminated by limiting the input current to 150mA with external resistors in series with those pins No external protection is needed for slower voltage

MECHANICAL



NOTE
Leads in true position within .010" (.25mm) R @ MMC at seating plane

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.510	1 550	38.35	39.37
B	.745	.770	18.92	19.56
C	.260	.300	6 60	7.62
D	.038	.042	0.97	1 07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1 186 BASIC		30.12 BASIC	
J	593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	151	.161	3 84	4.09
R	980	1.020	24.89	25.91

Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).

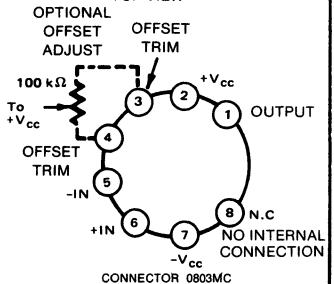
ORDER NUMBER 3580J
3581J
3582J

WEIGHT 15 GRAMS

CASE: METAL

PIN CONFIGURATION

TOP VIEW



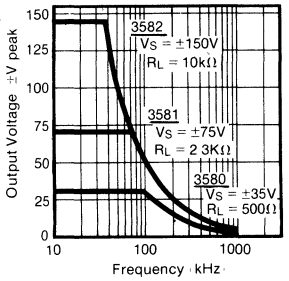
CONNECTOR 0803MC
HEAT SINK 0803HS
0804HS
0805HS

*The case is electrically isolated It is recommended that the case be grounded during use

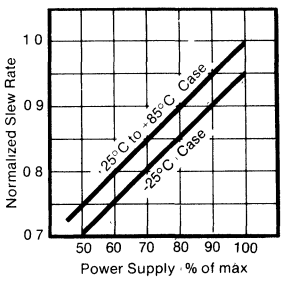
TYPICAL PERFORMANCE CURVES

T_{CASE} = +25°C and $\pm V_{CC}$ max unless otherwise noted

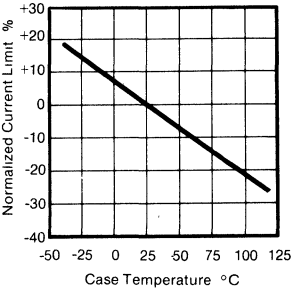
OUTPUT VOLTAGE VS FREQUENCY



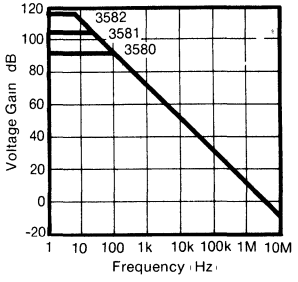
SLEW RATE VS SUPPLY VOLTAGE AT FULL LOAD



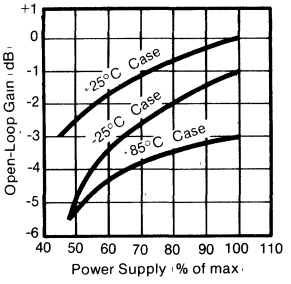
CURRENT LIMIT VS TEMPERATURE



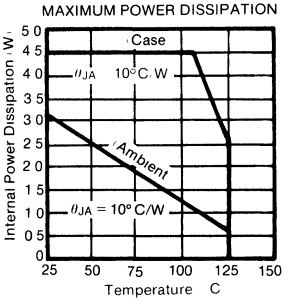
OPEN-LOOP FREQUENCY RESPONSE-FULL LOAD



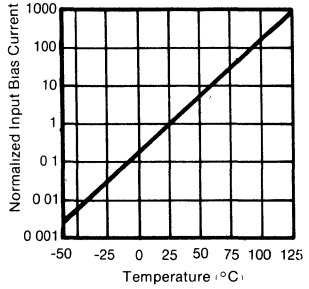
OPEN-LOOP GAIN VS SUPPLY VOLTAGE AT MAX LOAD



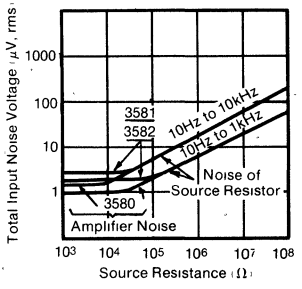
MAXIMUM POWER DISSIPATION



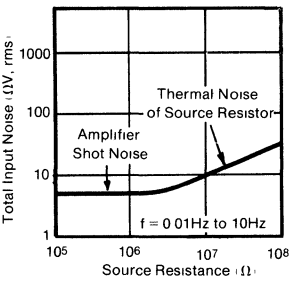
NORMALIZED INPUT BIAS CURRENT VS TEMPERATURE



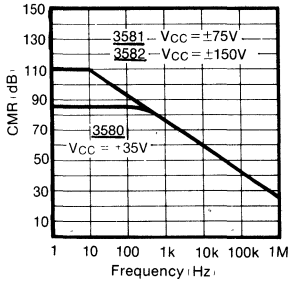
TOTAL INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



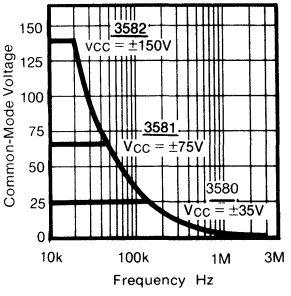
TOTAL LOW FREQUENCY INPUT NOISE VS SOURCE RESISTANCE



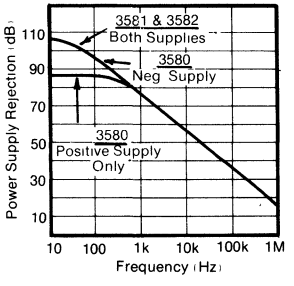
COMMON-MODE REJECTION VS FREQUENCY



MAXIMUM COMMON-MODE VOLTAGE VS FREQUENCY

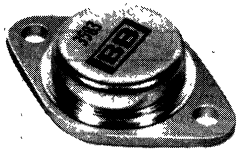


POWER SUPPLY REJECTION VS FREQUENCY



BURR-BROWN®

3583



High Voltage - High Current OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT SWINGS, Up to ±140V
- LARGE LOAD CURRENTS, ±75mA
- PROTECTED OUTPUT STAGE, Automatic Thermal Shutoff
- REDUCES SOURCE LOADING, $10^{11}\Omega$ Input Z
- PRESERVES SYSTEM ACCURACY, 110dB CMR 20pA Bias Current

APPLICATIONS

- PROGRAMMABLE POWER SUPPLY OUTPUT AMPLIFIER
- HIGH VOLTAGE CURRENT SOURCE
- POWER BOOSTER
- HIGH VOLTAGE INTEGRATOR
- DIFFERENTIAL AMPLIFIER FOR HIGH COMMON-MODE VOLTAGE CIRCUITS

DESCRIPTION

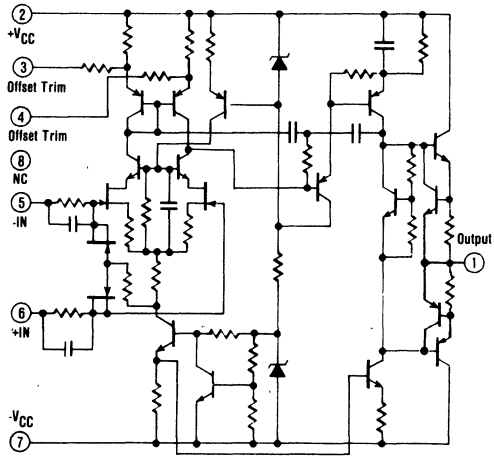
The 3583 is the first integrated circuit operational amplifier to provide output voltage swings of ±140V with currents as high as ±75mA.

The amplifier operates over a wide supply range (±50VDC to ±150VDC) and has excellent input characteristics (110dB CMR, 3mV V_{OS}, 25μV/°C $\Delta V_{OS}/\Delta T$).

The monolithic FET input stage has low bias current (20pA) which minimizes the offset voltages caused by the bias current and the large resistances normally associated with high voltage circuits.

The input stage is protected against overvoltages and the output stage is protected against short-circuits to ground for supply voltages below ±100VDC. A special thermal sensing circuit prevents damage to the amplifier by automatically shutting the amplifier down when too much power is being dissipated.

Two temperature ranges are available: 0°C to +70°C (3583JM) and -25°C to +85°C (3583AM).



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PDS-343D

SPECIFICATIONS

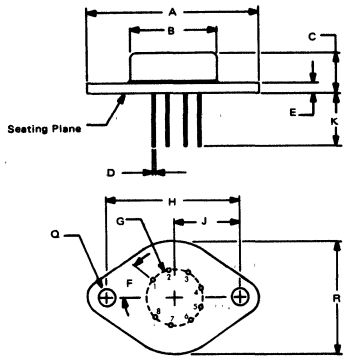
ELECTRICAL

Specifications typical at T_{CASE} = +25°C and $\pm V_{CC}$ = 150VDC unless otherwise noted

MODELS	3583AM	3583JM
POWER SUPPLY		
Voltage, $\pm V_{CC}$	±50VDC to ±150VDC	
Quiescent Current, max	8 5mA	
RATED OUTPUT		
Voltage, $\pm(\lvert V_{CC}\rvert - 10)$VDC, min	±40VDC to ±140VDC	
Current, min	±75mA	
Current, Short Circuit	±100mA	
Load Capacitance, max	10nF	
OPEN-LOOP GAIN		
No Load, DC	118dB	
Rated Load, DC	94dB, min; 105dB, typ	
FREQUENCY RESPONSE		
Unity Gain Bandwidth, Small Signal	5MHz	
Full Power Bandwidth, R_L = 10kΩ	60kHz	
Slew Rate	30V/μsec	
Settling Time, 0 1%	12μsec	
INPUT OFFSET VOLTAGE T_A = +25°C		
Initial at 25°C, max	±3mV	
Drift vs Temp, max	±23μ/°C	
Drift vs Supply Voltage	±20μV/V	
Drift vs Time	±50μV/mo	
INPUT BIAS CURRENT		
Initial at 25°C, max	-20pA	
Drift vs Temp	doubles every 10°C	
Drift vs Supply Voltage	0.2pA/V	
INPUT OFFSET CURRENT		
Initial at 25°C	±20pA	
Drift vs Temp	doubles every 10°C	
Drift vs Supply Voltage	0 2pA/V	
INPUT IMPEDANCE		
Differential	$10^{11}\Omega \parallel 10$pF	
Common-mode	$10^{11}\Omega$	
INPUT NOISE		
Voltage 0 01Hz to 10Hz, p-p	5μV	
10Hz to 1kHz, rms	1 7μV	
Current 0 01Hz to 10Hz, p-p	0 3pA	
INPUT VOLTAGE RANGE		
Max Safe Differential Voltage(1)	$(+V_{CC} + \lvert -V_{CC}\rvert)$	
Max Safe Common-mode Voltage	$+V_{CC}$ to $-V_{CC}$	
Common-mode Voltage, Linear Operation	$\pm(\lvert V_{CC}\rvert - 10)$V	
Common-mode Rejection	110dB	
TEMPERATURE RANGE (Case)		
Specification	-25°C to +85°C	0°C to 70°C
Operating	-55°C to +125°C	
Storage	-55°C to +125°C	

NOTES
1 The inputs may be damaged by pulses at pins 5 or 6 with dV/dt ≥ 1V/nsec. Any possible damage can be eliminated by limiting the input current to 150mA with external resistors in series with those pins No external protection is needed for slower voltage changes

MECHANICAL



NOTE
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only
Numbers may not be marked on package

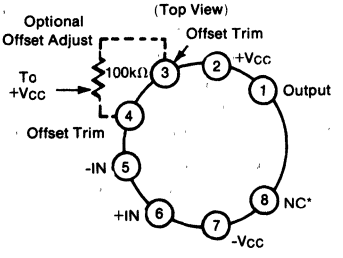
ORDER NUMBER:
3583AM 3583JM

WEIGHT:
15.1 Grams

MATING CONNECTOR:
0803MC

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39 37
B	.745	770	18.92	19 56
C	260	.300	6 60	7.62
D	038	042	0.97	1 07
E	080	105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12 7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15 06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3 84	4 09
R	.980	1 020	24 89	25.91

CONNECTION DIAGRAM

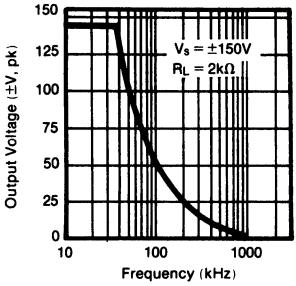


* No internal connection.
The metal case is electrically isolated.
It is recommended that the case be grounded during use.

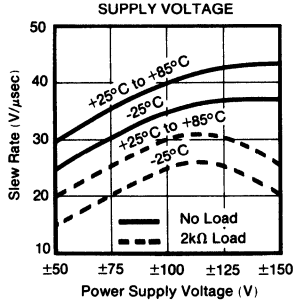
TYPICAL PERFORMANCE CURVES

Typical at T_{CASE} = +25°C and $\pm V_{CC}$ = 150VDC unless otherwise noted

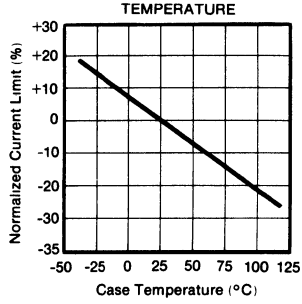
OUTPUT VOLTAGE vs FREQUENCY



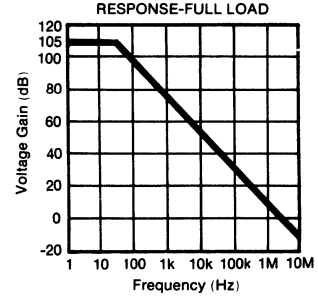
SLEW RATE vs SUPPLY VOLTAGE



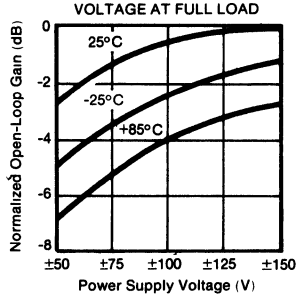
CURRENT LIMIT vs TEMPERATURE



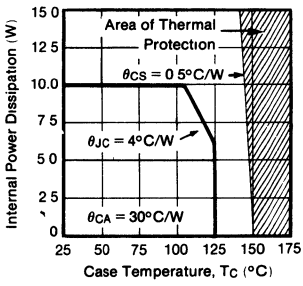
OPEN-LOOP FREQUENCY RESPONSE-FULL LOAD



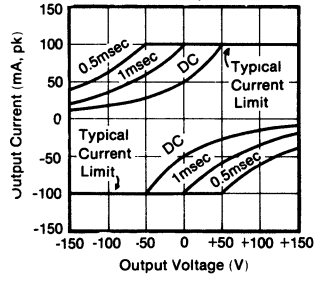
OPEN-LOOP GAIN vs SUPPLY VOLTAGE AT FULL LOAD



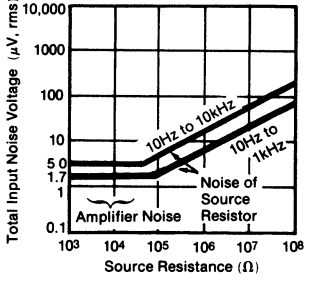
RECOMMENDED POWER DERATING



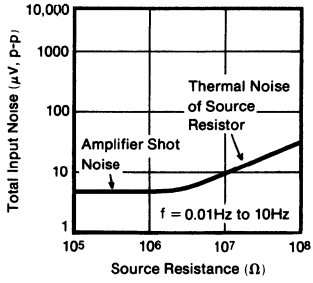
RECOMMENDED SAFE OPERATING AREA (Secondary Breakdown)



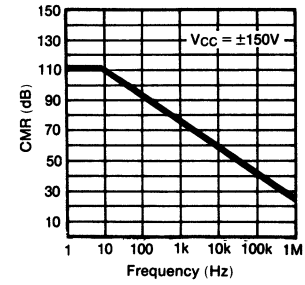
TOTAL INPUT NOISE VOLTAGE vs SOURCE RESISTANCE



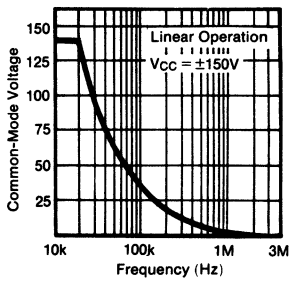
TOTAL LOW FREQUENCY INPUT NOISE vs SOURCE RESISTANCE



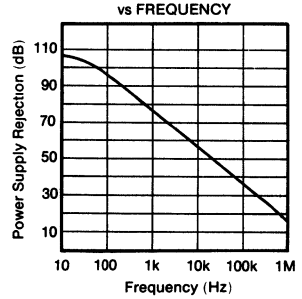
COMMON-MODE REJECTION vs FREQUENCY



COMMON-MODE VOLTAGE vs FREQUENCY



POWER SUPPLY REJECTION vs FREQUENCY



APPLICATIONS INFORMATION

The 3583 is a high voltage, high output current integrated circuit operational amplifier. Its ease of use, compact size, and excellent input and output specifications makes it well suited for a wide variety of high voltage applications.

The equivalent circuit for the 3583 is shown in Figure 1. The design uses a monolithic FET input stage for high input impedance, low bias current, and low voltage drift versus temperature. The offset voltage at 25°C and the drift versus temperature are compensated by state-of-the-art laser-trimming techniques. They are low enough so that user-trimming will not be required in most applications. The high input impedance provides negligible source impedance loading errors when the noninverting circuit configuration is used. The low bias currents minimize offset errors when large values of source and feedback resistors are used.

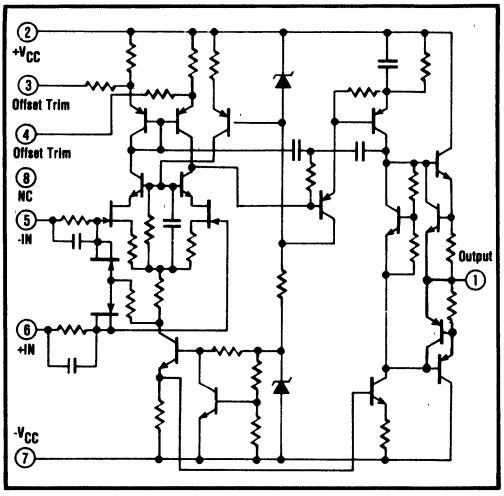


FIGURE 1. 3583 Equivalent Circuit.

A true cascade input stage is used together with considerable protection circuitry. There are voltage limiting transistors to prevent damage due to reverse bias breakdown of the input pair and current limiting resistors to limit the input current to 1mA with the inputs at ±150 volts. The units are conservatively rated (and 100% tested) at full rated differential voltage (+150V and -150V) but typically will withstand a 50% overvoltage without damage.

The unit operates over a wide supply range (±50V to ±150V) with outstanding common-mode rejection (110dB). It also has another feature which is important in many high voltage applications. The input bias current is virtually independent of applied common-mode voltage. The output circuit has a unique protection feature which is only practical in integrated-circuit amplifiers - self-contained automatic thermal sensing and shutoff circuitry which automatically turns the amplifier off when the internal temperature reaches approximately 150°C. This is accomplished by sensing the substrate temperature and deactivating the amplifier's biasing network when the temperature reaches 150°C. As this happens, the output load current limits at a safe value and the amplifier's quiescent current decreases. The output current will remain at a low value or oscillate between two values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal load condition is removed.

The internal thermal protection removes some of the constraints of power derating for abnormal operating conditions. The amplifier will protect itself for many conditions of excess power dissipation (see the Power Derating Curve). This allows the use of a smaller heat sink to protect against abnormal output conditions since the amplifier has its own internal protection for many conditions of excess power dissipation. The output constraints of the Recommended Safe Operating Area curves must still be observed.

The 3583 has several other features that improve its utility. For instance, the metal case of the unit is completely electrically isolated. (This can be contrasted to most power semiconductors where the case is connected to the collector of the device.) This simplifies mounting and reduces cost since the need for insulating spacers and bushings is eliminated. The hermetically sealed package improves reliability and will more easily withstand severe environments than do discrete component amplifiers. The small package size reduces weight and makes mounting more convenient.

Burr-Brown offers three heat sinks as accessories; 0803HS with a thermal resistance of 12°C/watt, 0804HS at 4.2°C/watt, and 0805HS at 3°C/watt. A convenient mating connector, 0803MC is also available.

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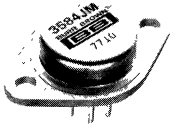
3584



High Voltage OPERATIONAL AMPLIFIER

FEATURES

- TYPICAL GAIN-BANDWIDTH, 50MHz
- OUTPUT, +145V
- PROTECTED OUTPUT, automatic thermal shutoff
- BIAS CURRENT, -20pA
- CMR, 110dB
- SLEW RATE, 150V/μs

APPLICATIONS

- ANALOG SIMULATORS
- DIGITALLY-CONTROLLED POWER SUPPLIES
- CRT DEFLECTION
- ELECTROSTATIC TRANSDUCERS

DESCRIPTION

The 3584 is a high voltage, integrated circuit operational amplifier that will provide up to ±145V output.

The amplifier will provide a gain-bandwidth product of 20MHz minimum, 50MHz typical. The amplifier uses external frequency compensation (one R and one C) so that the user may optimize the bandwidth and slew rate for his particular application.

The amplifier operates over a wide supply range (±70VDC to ±150VDC) and has excellent input characteristics (110dB CMR, 3mV E_{os}, and 25μV/°C E_{os} Drift). The input stage is a FET. The low -20pA bias current minimizes the offset errors caused by the large value resistors normally used in high voltage circuits.

The input stage is protected against overvoltages and the output stage is protected against short circuits to ground. A special thermal sensing circuit helps to prevent damage to the amplifier by automatically shutting the amplifier down when too much power is being dissipated.

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PDS-376A

DISCUSSION

The 3584 is a high voltage, integrated circuit operational amplifier. Its ease of use, compact size, and excellent input and output specifications makes it well suited for a wide variety of high voltage and high speed applications.

The design uses a monolithic FET input stage for high input impedance, low bias current, and low voltage drift versus temperature. The offset voltage and the drift are laser trimmed. They are low enough so that user trimming will not be required in most applications.

To achieve the high common-mode voltage capability and rejection a true cascode input stage is used together with considerable protection circuitry. There are voltage limiting diodes to prevent damage due to reverse bias breakdown of the input pair and current limiting resistors to limit the steady state input current to 1mA with the inputs at ±150 volts. The units are conservatively rated (and 100% tested) at full rated differential voltage (+150 and -150V) but typically will withstand a 50% overvoltage without damage.

It also has another feature which is important in many high voltage applications. The input bias current is virtually independent of applied common-mode voltage. This is a benefit of the true cascode input stage which keeps the drain to source voltage of the input transistors constant as the common-mode voltage changes.

The amplifier contains automatic thermal sensing and shut-off circuitry which automatically turns the amplifier off when the internal (substrate) temperature reaches approximately 150°C. This is accomplished by sensing the substrate temperature and deactivating all current sources when the temperature reaches a critical level. As this happens, the output current gradually decreases to zero. The output current may remain at a low value or oscillate between 2 values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal condition is removed.

The incorporation of thermal sensing and shut-off in the amplifier will require a smaller heat sink than normal. This is due to the fact that the amplifier will protect itself and does not require a massive heat sink for protection under abnormally high power dissipation.

The 3584 has several other features that improve its utility. The metal case of the unit is completely electrically isolated. This simplifies mounting and reduces cost since the need for insulating spacers is eliminated. The hermetically sealed package improves reliability and will withstand severe environments better. And the small package size reduces weight and makes mounting more convenient.

OPERATION FROM A SINGLE SUPPLY

It may be desirable in some applications to operate the amplifiers from a single supply. The circuit in Figure 1 illustrates a typical application. Note that there are restrictions on the input and output voltages (e_i and e_o) which are necessary in order to keep the amplifier circuits operating in a linear manner.

It should be noted that when the amplifier is operated from a single supply, the output stage, which is still short circuit current limited and thermally protected, is not protected for short circuits to ground under all operating conditions. Consult the safe operating area curve.

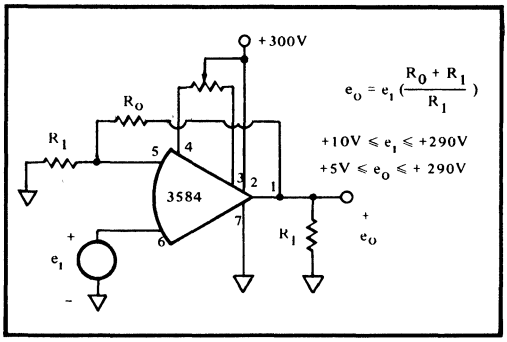


FIGURE 1. Operation from a single supply.

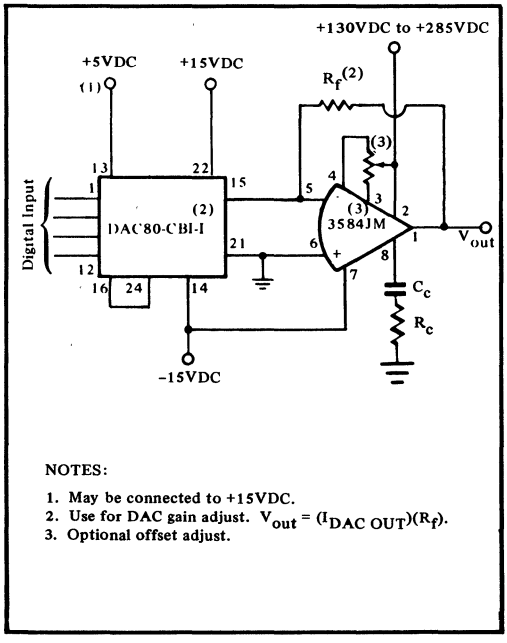


FIGURE 2. High Speed, High Voltage DAC.

SPECIFICATIONS

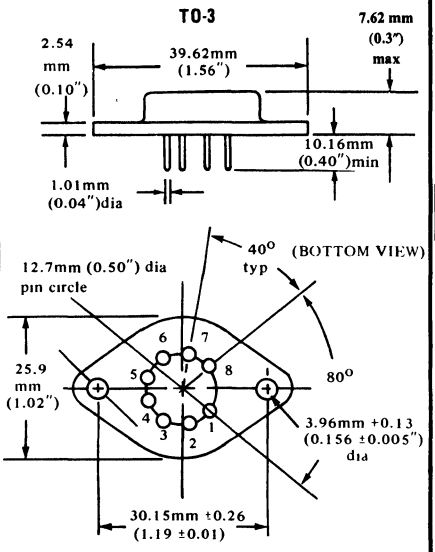
ELECTRICAL

Typical at 25°C and $\pm V_{cc}$ max unless otherwise noted.

MODELS	3584JM
POWER SUPPLY	
Voltage, $\pm V_{cc}$	±70 to ±150 VDC
Quiescent Current, max	±6.5mA
RATED OUTPUT	
Voltage, ± (| V_{cc} | -5)VDC, min	±65 to ±145 VDC
Current, min	±15mA
Current, Short Circuit	±25mA
Load Capacitance, max	10 nF
OPEN LOOP GAIN	
No Load, DC	120 dB
Rated Load, DC, min	100dB
FREQUENCY RESPONSE	
Unity Gain Bandwidth, Small Signal	7 MHz
Gain-bandwidth Product, f = 1 kHz, G = 100	20 MHz, min
Full Power Bandwidth, G = 100	135 kHz
Slew Rate, G = 100	150 V/μs
Settling Time, 0.1%, G = 100	12 μs
INPUT OFFSET VOLTAGE	
Initial @ 25°C, max	3 mV
Drift vs Temp, max	25 μV/°C
Drift vs Supply Voltage	20 μV/V
Drift vs Time	50 μV/mo
INPUT BIAS CURRENT	
Initial @ 25°C, max	-20 pA
Drift vs Temp	doubles every 10°C
Drift vs Supply Voltage	0.2 pA/V
INPUT OFFSET CURRENT	
Initial @ 25°C	±20 pA
Drift vs Temp	doubles every 10°C
Drift vs Supply Voltage	0.2 pA/V
INPUT IMPEDANCE	
Differential	10^{11} Ω || 10 pF
Common Mode	10^{11} Ω
INPUT NOISE	
Voltage 0.01 Hz to 10 Hz p-p	5 μV
10 Hz to 1 kHz rms	1.7 μV
Current 0.01 Hz to 10 Hz p-p	0.3 pA
INPUT VOLTAGE RANGE	
Max Safe Differential Voltage[1]	(+V_{cc} + | -V_{cc} |)
Max Safe Common Mode Voltage	+V_{cc} to -V_{cc}
Common Mode Voltage, Linear Operation	±(| V_{cc} | -10)V
Common Mode Rejection	110dB
TEMPERATURE RANGE (Case)	
Specification	0°C to 70°C
Operating	-55°C to +125°C
Storage	-55°C to +150°C

(1) The inputs may be damaged by pulses at pins 5 or 6 with $dV/dt \geq 1$ V/ns. Any possible damage can be eliminated by limiting the input current to 150mA with external resistors in series with those pins. No external protection is needed for slower voltage changes.

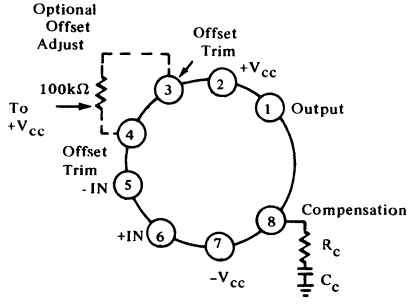
MECHANICAL



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]

CONNECTION DIAGRAM

(TOP VIEW)



Connector: 0803MC
Heatsinks: 0803HS, 0804HS, or 0805HS

Compensation		
Gain	C_c	R_c
1	10 nF	200Ω
10	500 pF	2kΩ
100	50 pF	20kΩ
1000	not required	

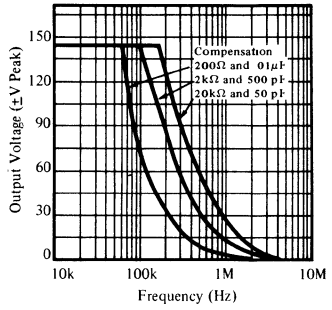
For intermediate values of gain, R and C values may be interpolated.

The case is electrically isolated. It is recommended that the case be grounded during use.

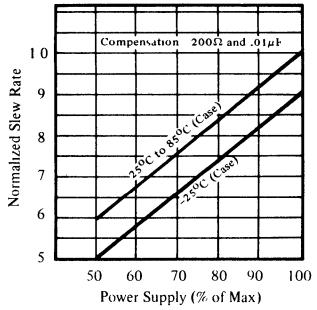
TYPICAL PERFORMANCE CURVES

Typical at 25°C and $\pm V_{cc}$ max unless otherwise noted.

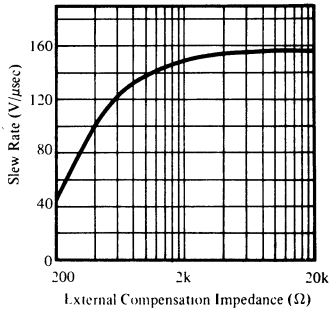
OUTPUT VOLTAGE vs FREQUENCY



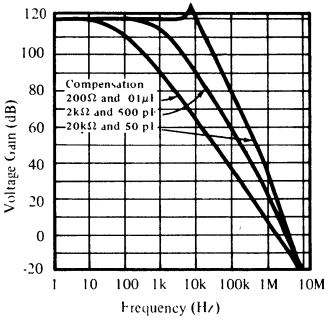
SLEW RATE vs SUPPLY VOLTAGE @ FULL LOAD



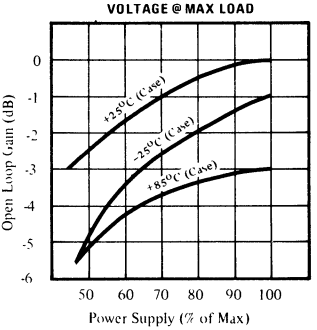
SLEW RATE vs COMPENSATION



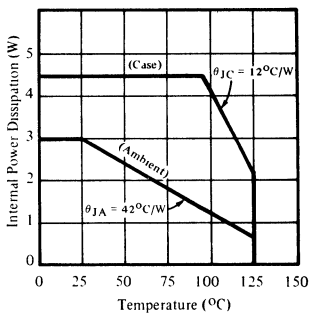
OPEN LOOP FREQUENCY RESPONSE FULL LOAD



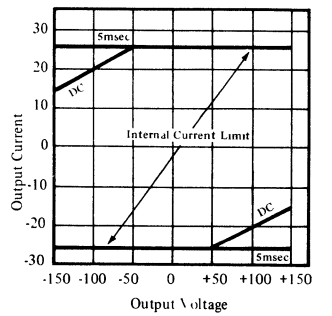
OPEN LOOP GAIN vs SUPPLY VOLTAGE @ MAX LOAD



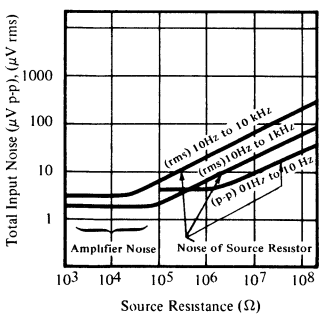
POWER DISSIPATION



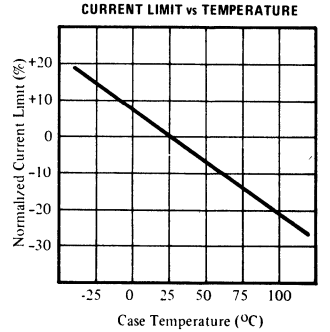
SAFE OPERATING AREA (Secondary Breakdown)



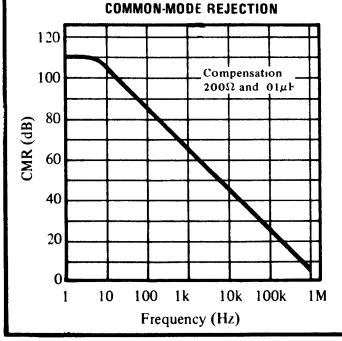
NOISE vs SOURCE RESISTANCE



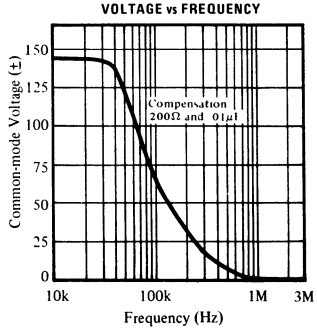
CURRENT LIMIT vs TEMPERATURE



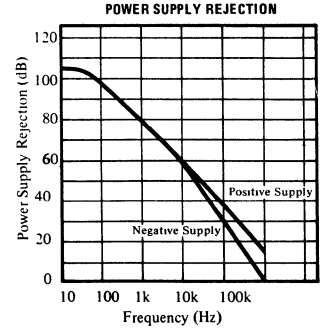
COMMON-MODE REJECTION

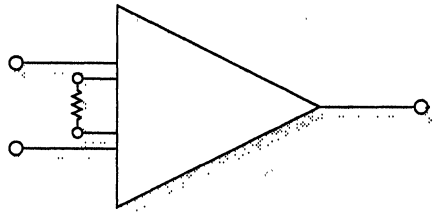


MAXIMUM COMMON-MODE VOLTAGE vs FREQUENCY



POWER SUPPLY REJECTION





INSTRUMENTATION AMPLIFIERS

3

WHAT IS AN INSTRUMENTATION AMPLIFIER?

An instrumentation amplifier is a closed-loop, differential input, gain block. It is a committed circuit with the primary function of accurately amplifying the voltage applied to its inputs.

Ideally, the instrumentation amplifier responds only to the difference between the two input signals and exhibits extremely high impedance between the two input terminals, and from each terminal to ground. The output voltage is developed single-ended with respect to ground and is equal to the product of amplifier gain and the difference of the two input voltages. See Figure 1.

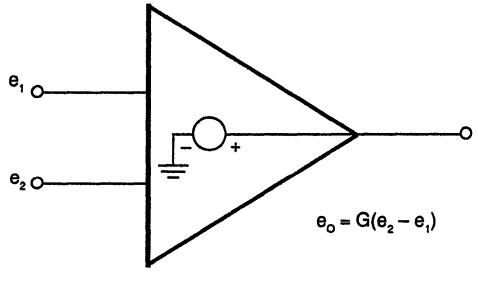


Figure 1. Idealized Model of an Instrumentation Amplifier.

Amplifier gain (G) is normally set by the user with a single external resistor. The properties of this model may be summarized as infinite input impedance, zero output impedance, the output voltage proportional to only the difference voltage ($e_2 - e_1$), a precisely known gain constant (G) (implying no nonlinearity), and unlimited bandwidth. This amplifier would completely

reject signal components common to both inputs (common-mode rejection) and would exhibit no DC offset voltage or drift.

CHARACTERISTICS OF INSTRUMENTATION AMPLIFIERS

It is desirable to achieve, as close as possible, the characteristics of the ideal instrumentation amplifier. The following paragraphs are a discussion of the other-than-ideal characteristics of instrumentation amplifiers.

INPUT IMPEDANCE

A simple model of a realistic instrumentation amplifier is shown in Figure 2. The impedance Z_{ID} represents the differential input impedance. The common-mode input impedance Z_{ICM} is represented as two equal components, $2Z_{ICM}$, from each input to ground. These finite resistances contribute an effective gain error due to loading of the source resistance. The instrumentation amplifier provides a load on the source of $Z_I = Z_{ID} \parallel Z_{ICM}$. If source impedance is $R_S = R_{S1} + R_{S2}$, the gain error caused by this loading is:

$$\text{Gain Error} = 1 - \frac{Z_I}{Z_I + R_S} = \frac{R_S}{Z_I + R_S} \cong \frac{R_S}{Z_I} \quad \text{if } Z_I >> R_S$$

If R_s is 10kΩ and Z_I is 10MΩ,

$$\text{Gain Error} \cong \frac{10 \times 10^3}{10 \times 10^6} = 0.1\%$$

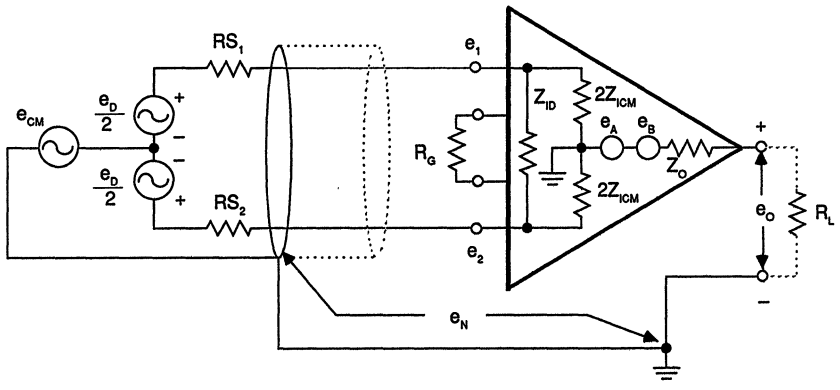


Figure 2. Simple Model of an Instrumentation Amplifier Shown in a Typical Application Configuration.

The DC common-mode input impedance Z_{ICM} will be independent of gain. The DC differential input impedance Z_{ID} may vary as a function of gain. Specifications give the worst-case value. The nonzero output impedance of the amplifier will also create a gain error, the value of which depends on the load resistance.

NONLINEARITY

The linearity of gain is possibly of more importance than the gain accuracy, since the value of the gain can be adjusted to compensate for simple gain errors. The nonlinearity is specified to be the peak deviation from a "best fit" straight line, expressed as a percent of peak-to-peak full scale output.

COMMON-MODE REJECTION

As illustrated in Figure 2, the output voltage has two components. One component is proportional to the differential input voltage $e_D = (e_2 - e_1)$. The second component is proportional to the common-mode input voltage. The common-mode voltage which appears at the amplifier's input terminals is defined as $e_{CM} = e_2 + e_1/2$. This may consist of some common-mode voltage in the source itself, $e_{CM'}$ (such as bridge excitation) plus any noise voltage, e_N, between the source common and the amplifier common. As shown in Figure 2, the constant G represents the differential amplifier gain factor (fixed by the external gain-setting resistor). The constant (G/CMRR) represents the common-mode signal gain of the amplifier. The CMRR (common-mode rejection ratio) is the ratio of differential gain to common-mode gain. Thus CMRR is proportional to the differential gain and CMRR increases as the differential gain (G) increases. Hence, CMRR is usually specified for the maximum and the minimum values of gain of the amplifier. The common-mode rejection may be expressed in dB as CMRR (dB) = $20\log_{10}$ CMRR.

For an ideal instrumentation amplifier the output voltage component due to common-mode voltage should be zero. For a realistic instrumentation amplifier, the CMRR though very high, is still not infinite and so will cause an error voltage of e_{CM}/CMRR x G to appear at the output.

SOURCE IMPEDANCE UNBALANCE

If the source impedances are unbalanced, the source voltages ($e_{CM} + e_N$) are divided unequally upon the common-mode impedance, and a differential signal is developed at the amplifier's input. This error signal cannot be separated from the desired signal. In the circuit in Figure 2 if $R_{S2} = 0$, $R_{S1} = 1k\Omega$, $e_{CM} + e_N = 10V$, and $Z_{CM} = 100M\Omega$, then the effect of unbalance is to generate a voltage:

$$e_2 - e_1 = 10V - 10V\frac{10^8}{10^8 + 10^3} = 10V\frac{10^3}{10^8 + 10^3} \cong \frac{10V}{10^5} = 0.1mV$$

If e_D full scale is 10mV then this error is

$$\text{Error} = \frac{0.1\text{mV}}{10\text{mV}} = 1\% \text{ of full scale}$$

OFFSET VOLTAGE AND DRIFT

Most instrumentation amplifiers are two-stage devices—they have a variable gain input stage and a fixed gain output stage. If V_I and V_O are the offset voltages of the input and output stages respectively, then the amplifiers total offset voltage referred to the input (RTI) = $V_I + V_O/G$, where G is the amplifier's gain. (Note that total E_{OS} (RTI) x G appears at the output.)

The initial offset voltage is usually adjustable to zero. Therefore voltage drift is the more significant term because it cannot be nulled. The offset voltage drift also has two components—one due to the input stage of the amplifier and the other due to the output stage. When the amplifier is operated at high gain, the drift of the input stage dominates. At low values of gain, the drift of the output stage will be the major component of drift. When the total output drift is referred to the input, the effective input voltage drift is largest for low values of gain. Output voltage drift will always be lowest at low gains. If $\Delta V_I/\Delta T = 2\mu V/°C$ and $\Delta V_O/\Delta T = 500\mu V/°C$ and the amplifier in a gain of 1000V/V is nulled at 25°C, then at 65°C the offset voltage will be

$$\begin{aligned} E_{OS}(\text{RTI})\ 65° &= 40°C[2\mu V/°C + (500\mu V/°C/1000V/V)] \\ &= 40°C(2.5\mu V/°C) = 100\mu V = 0.1\text{mV} \end{aligned}$$

If the full scale input is 10mV, then the error due to voltage drift is

$$\text{Error} = \frac{0.1\text{mV}}{10\text{mV}} = 1\% \text{ of full scale}$$

INPUT BIAS AND OFFSET CURRENTS

The input bias currents are the currents that flow out of (or into) either of the two inputs of the amplifier. They are the base currents for bipolar input stages and the leakage currents for JFET input stages. Offset current is the difference of the two bias currents.

The bias currents flowing into the source resistances will generate offset voltages of $E_{OS2} = I_{B2} \times R_{S2}$ and $E_{OS1} = I_{B1} \times R_{S1}$. If $R_{S1} = R_{S2} = R_S/2$, the offset voltage at the input is $E_{OS2} - E_{OS1} = I_{OS} \times R_S/2$. This input-referred offset error may be compared directly with the input voltage to compute percent error. (Note that the source must be returned to power supply common or R_S will be infinite and the amplifier will saturate.)

APPLICATIONS OF INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are generally used in applications where extracting and accurately amplifying low level differential signals riding on high common-mode voltages (±10V) is very important. Such applications require high input impedance, high CMRR, low input noise, and excellent DC level stability (low offset voltage drift).

Instrumentation amplifiers are used as transducer amplifiers for various types of transducers such as strain gauge bridges, load cells, thermistor networks, thermocouples, current shunts, biological probes, weather gauges, and so forth. Other applications include recorder preamplifiers, multiplexer buffers, servo error amplifiers, current sensors, signal conditioners in process control and data acquisition systems, and in general measurements of small differential signals riding on common-mode voltages.

The small size, low cost, and high performance of these amplifiers offer an attractive approach for data acquisition applications, that is, assigning a fixed-gain amplifier to each transducer and locating the amplifier physically near the transducer. This approach largely eliminates common-mode noise pickup problems since a high level signal (rather than a low level transducer signal) is then transmitted to the data gathering station. The result is a higher signal/noise ratio at the output. Using one amplifier per point may well be more economical, as well as offering better performance and flexibility, than the approach of using low level multiplexers.

INSTRUMENTATION AMPLIFIERS SELECTION GUIDES

The following Selection Guides show parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

Description	Model	Gain Range	Gain Accuracy, G=100 25°C, max(%)	Gain Drift, G=100 (ppm/°C)	Non-Linearity G=100 max(%)	Input Parameters CMR[6] min(dB)	Input Parameters Offset Voltage vs Temp max (µV/°C)	Dynamic Response, G=100 ±3dB BW (kHz)	Temp Range[1]	Pkg	Page
Very High Accuracy	INA104P	1-1000[2]	0.15	22	±0.003	96	±(0.25±10/G)	25	Com	DIP	3-34
	INA104M	1-1000[2]	0.15	22[3]	±0.003	96	±(0.25±10/G)	25	Ind	DIP	3-34
	INA101G	1-1000[2]	0.03	22[3]	±0.003	96	±(0.25±10/G)	25	Ind	DIP	3-11
	INA101P	1-1000[2]	0.3	22[3]	±0.007	90	±(2±20/G) typ	25	Com	DIP	3-11
Low Quiescent Power	INA102G	1,10,100, 1000	0.15	15	±0.02	90	±(2±5/G)	3	Ind	DIP	3-23
Fast Settling FET Input	INA110G	1,10,100, 200,500	0.1	20	±0.01	96	±(2±50/G)	470	Ind	DIP	3-65
	INA110P	1,10,100, 200, 500	0.2	6 typ	±0.02	87	±(2±20/G) typ	470	Com	DIP	3-65
Buffer, Unity-Gain Difference	3627M	1V/V,fixed	0.01[3]	5	±0.001[3]	100	20	800[3]	Ind	TO-99	3-158
	INA105M	1V/V,fixed	0.01[3]	5	±0.001[3]	86[5]	10	1000[3]	Ind	TO-99	3-45
	INA105P	1V/V,fixed	0.025[3]	5	±0.001[3]	72[5]	5 typ	1000[3]	Com	DIP	3-45
Gain of 10 Difference	**INA106M**	**10V/V,fixed**	**0.01[4]**	**10**	**±0.001[4]**	**100[5]**	**2**	**500[4]**	**Ind**	**TO-99**	**3-57**
	INA106P	**10V/V,fixed**	**0.025[4]**	**4 typ**	**±0.001[4]**	**86[5]**	**0.2 typ**	**500[4]**	**Com**	**DIP**	**3-57**
High Common Mode Voltage Difference (200VDC CMV)	**INA117G**	**1V/V,fixed**	**0.02[3]**	**10[3]**	**±0.001[3]**	**86[5]**	**20**	**200[3]**	**Ind**	**DIP**	**3-77**
	INA117P	**1V/V,fixed**	**0.05[3]**	**10[3]**	**±0.001[3]**	**74[5]**	**40**	**200[3]**	**Com**	**DIP**	**3-77**
4-20mA Loop Receiver	**RCV420BG**	**.3125V/mA**	**0.025**	**25**	**±0.001**	**86**	**25[7]**	**150**	**Ind**	**DIP**	**3-110**
	RCV420KP	**.3125V/mA**	**0.05**	**50**	**±0.001**	**74**	**50[7]**	**150**	**Com**	**DIP**	**3-110**

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C. (2) Set with external resistor. (3) Unity-gain. (4) Gain = 10. (5) No source imbalance. (6) DC to 60Hz, Gain = 10, 1kΩ unbalanced. (7) RTO.

PROGRAMMABLE GAIN AMPLIFIERS

Description	Model	Gain Range	Gain Accuracy, G=100 25°C, max(%)	Gain Drift, G=100 (ppm/°C)	Non-Linearity G=100 max(%)	Input Parameters CMR[6] min(dB)	Input Parameters Offset Voltage vs Temp max (µV/°C)	Dynamic Response, G=100 ±3dB BW (kHz)	Temp Range[1]	Pkg	Page
Noninverting Multiplexed Input	PGA100G	Gain set with 4-bit word 1, 2, 4, 8...128	0.02	10	±0.005	NA	6 typ	5MHz	Ind	DIP	3-85
	PGA102G	Gain set with 2-bit word 1, 10 100	0.01	20	±0.01		3,G=100	250	Ind	DIP	3-93
	PGA102P		0.02	50	±0.01		3,G=100	250	Com	DIP	3-93
Instrumentation Amplifier Input	PGA200G	Gain set with 2-bit word 1, 10, 100, 1000	0.02	10	±0.003	96	0.4,G=100	30	Ind	DIP	3-103
Differential Input	3606M	Gain set with 3-bit word 1, 2, 4, 8...1024	0.02	10	±0.004	90,G=1	±(1+20/G)	40	Ind	DIP	3-150

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C. (2) Set with external resistor. (3) Unity-gain. (4) Gain = 10 (5) No source imbalance. (6) DC to 60Hz, Gain = 10, 1kΩ unbalanced.

PRECISION TRANSMITTERS

Description	Model	Span: Untrimmed Error, max (%)	Span: Non-linearity, max (%)	Span: Temp Drift[1] (ppm/°C)	Input Parameters: Offset Voltage max	Input Parameters: Offset Voltage vs Temp max (µV/°C)	Input Parameters: CMR, DC, min (dB)	Output Parameters: Current Range (mA)	Output Parameters: Offset Current Error, max (µA)	Output Parameters: FS Output Current Error, max (µA)	Temp Range[2]	Pkg	Page
Two-Wire	XTR100P	–3	0.01	±100	±25µV	±0.5	90	4-20	±4	±20	Ind	DIP	3-114
	XTR101G	–5	0.01	±100	±30µV	±0.75	90	4-20	±6	±30	Ind	DIP	3-126
	XTR101P	–5	0.01	±100	±100µV	±1.5	90	4-20	±19	±60	Ind[3]	DIP	3-126
Three-Wire and Current Source	XTR110G	0.2	0.005	30	—	—	—	4-20, 0-20, 5-25[4]	±16	±32	Ind	DIP	3-139
	XTR110P	0.6	0.025	50	—	—	—	4-20, 0-20, 5-25[4]	±64	±96	Com	DIP	3-139

NOTES: (1) With zero TC span resistor. (2) Com = 0°C to +70°C, Ind = –25°C to +85°C. (3) –40°C to +85°C. (4) Many more ranges with appropriate circuit.

INSTRUMENTATION AMPLIFIERS GLOSSARY

COMMON-MODE INPUT IMPEDANCE

Effective impedance (resistance in parallel with capacitance) between either input of an amplifier and its common, or ground, terminal.

COMMON-MODE REJECTION (CMR)

When both inputs of a differential amplifier experience the same common-mode voltage (CMV), the output should, ideally, be unaffected. CMR is the ratio of the common-mode input voltage change to the differential input voltage (error voltage) producing the same output change:

$$\text{CMR (in dB)} = 20\log_{10} \text{CMV/Error Voltage}$$

Thus a CMR of 80dB means that 1V of common-mode voltage will cause an error of 100μV (referred to input).

COMMON-MODE REJECTION RATIO (CMRR)

Ratio of the differential voltage gain of an amplifier to its common-mode voltage gain.

COMMON-MODE VOLTAGE (CMV)

That portion of an input signal common to both inputs of a differential amplifier. Mathematically it is defined as the average of the signals at the two inputs:

$$\text{CMV} = (e_1 + e_2) / 2$$

FEEDBACK

Return of a portion of the output signal from a device to the input of the device.

FULL POWER FREQUENCY RESPONSE

Maximum sinewave frequency at which a device can supply its peak-to-peak rated output voltage and current, without introducing significant distortion.

GAIN

Ratio of the output signal to the associated input signal of a device.

GAIN ERROR

Difference between the actual gain of an amplifier and the one predicted by the ideal gain expression.

INPUT BIAS CURRENT

DC input current required at each input of an amplifier to provide zero output voltage when the input signal and input offset voltage are zero. The specified maximum is for each input.

INPUT BIAS CURRENT DRIFT

Rate of change of input bias current with temperature or time.

INPUT GUARDING

Use of an input shield that is sometimes driven to follow the voltage level of the input signal and, thereby, remove leakage and loss-inducing voltage differences between the input signal path and surrounding stray conduction paths.

INPUT OFFSET CURRENT

Difference of the two input bias currents in a differential amplifier.

INPUT OFFSET VOLTAGE

DC input voltage required to provide zero voltage at the output of an amplifier when the input signal and input bias currents are zero.

INPUT PROTECTION

Means of protecting an input of a device from damage due to the application of excessive input voltage.

INSTRUMENTATION AMPLIFIER

Closed-loop, differential input, gain block exhibiting high input impedance and high common-mode rejection. Its primary function is to accurately amplify the voltage applied to its inputs.

NONLINEARITY

Peak deviation from a best-fit straight line (curve fitting on input/output graph) expressed as a percent of peak-to-peak full scale output.

OVERLOAD RECOVERY TIME

Time required for the output of an amplifier to return from saturation to linear operation, following the removal of an input overdrive signal.

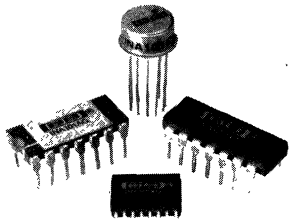
SETTLING TIME

Time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

SLEW RATE

Maximum rate of change of an output voltage when supplying the rated output.

BURR-BROWN®



INA101

MILITARY & DIE VERSIONS AVAILABLE

Very-High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- ULTRA-LOW VOLTAGE DRIFT - 0.25μV/°C
- LOW OFFSET VOLTAGE - 25μV
- LOW NONLINEARITY - 0.002%
- LOW NOISE - 13nV/√Hz at f_0 = 1kHz
- HIGH CMR - 106dB at 60Hz
- HIGH INPUT IMPEDANCE - $10^{10}\Omega$
- LOW COST, TO-100, CERAMIC DIP AND PLASTIC PACKAGE

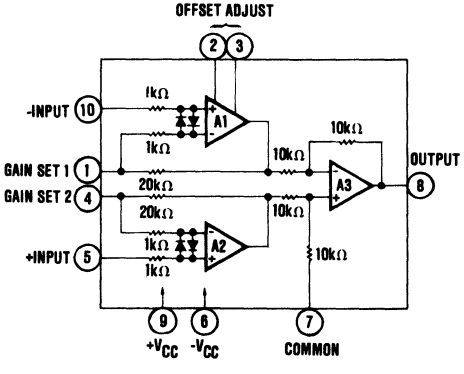
APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gages
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCERS
- LOW LEVEL SIGNALS
- MEDICAL INSTRUMENTATION

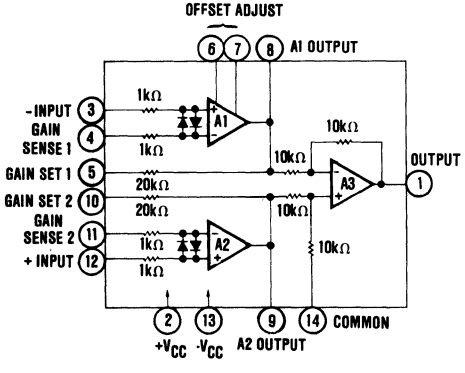
DESCRIPTION

The INA101 is a high accuracy, multistage, integrated-circuit instrumentation amplifier designed for signal conditioning requirements where very-high performance is desired. All circuits, including the interconnected laser-trimmed thin-film resistors, are integrated on a single monolithic substrate.

A multiamplifier design is used to provide the highest performance and maximum versatility with monolithic construction for low cost. The input stage uses Burr-Brown's ultra-low drift, low noise technology to provide exceptional input characteristics.



M Package



G and P Packages

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-454H

SPECIFICATIONS

ELECTRICAL

At +25°C with ±15VDC power supply and in circuit of Figure 2 unless otherwise noted

MODEL	INA101AM/AG			INA101SM/SG			INA101CM/CG			INA101HP/KU			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
GAIN													
Range of Gain	1		1000	*		*	*		*	*		*	V/V
Gain Equation		G=1+(40k/R_G)			*			*			*		V/V
Error From Equation, DC[1]		±(0.04+0.00016G 0.02/G)	±(0.1+0.0003G −0.05/G)		*	*		*	*		±(0.1+ 0.00015G) −0.05/G	±(0.3+ 0.0002G) −0.10/G	%
Gain Temp. Coefficient[3]													
G = 1		2	5		*	*		*	*		*	*	ppm/°C
G = 10		20	100		*	*		10	*		*	*	ppm/°C
G = 100		22	110		*	*		11	*		*	*	ppm/°C
G = 1000		22	110		*	*		11	*		*	*	ppm/°C
Nonlinearity, DC[2]		±(0.002+10^{-5}G)	±(0.005+2×10^{-5}G)		±(0.001 +10^{-5}G)	±(0.002 +10^{-5}G)		±(0.001 +10^{-5}G)	±(0.002 +10^{-5}G)		*	*	% of p-p FS
RATED OUTPUT													
Voltage	±10	±12.5		*	*		*	*		*	*		V
Current	±5	±10		*	*		*	*		*	*		mA
Output Impedance		0.2			*			*			*		Ω
Capacitive Load		1000			*			*			*		pF
INPUT OFFSET VOLTAGE													
Initial Offset at +25°C		±(25+200/G)	±(50+400/G)		±(10+ 100/G)	±(25 +200/G)		±(10+ 100/G)	±(25+ 200/G)		±(125+ 450/G)	±(250+ 900/G)	µV
vs Temperature			±(2+20/G)			±(0.75 +10/G)			±(0.25+ 10/G)		±(2+20/G)		µV/°C
vs Supply		±(1+20/G)			*			*			*		µV/V
vs Time		±(1+20/G)			*			*			*		µV/mo
INPUT BIAS CURRENT													
Initial Bias Current (each input)		±15	±30		±10	*		±5	±20		*	*	nA
vs Temperature		±0.2			*			*			*		nA/°C
vs Supply		±0.1			*			*			*		nA/V
Initial Offset Current		±15	±30		±10	*		±5	±20		*	*	nA
vs Temperature		±0.5			*			*			*		nA/°C
INPUT IMPEDANCE													
Differential		10^{10} 3			*			*			*		Ω pF
Common-mode		10^{10} 3			*			*			*		Ω pF
INPUT VOLTAGE RANGE													
Range, Linear Response	±10	±12		*	*		*	*		*	*		V
CMR with 1kΩ Source Imbal													
DC to 60Hz, G=1	80	90		*	*		*	*		65	85		dB
DC to 60Hz, G=10	96	106		*	*		*	*		90	95		dB
DC to 60Hz, G=100 to 1000	106	110		*	*		*	*		100	105		dB
INPUT NOISE													
Input Voltage Noise													
f_B=0.01Hz to 10Hz		0.8			*			*			*		µV, p-p
Density, G=1000													
f_O=10Hz		18			*			*			*		nV/√Hz
f_O=100Hz		15			*			*			*		nV/√Hz
f_O=1kHz		13			*			*			*		nV/√Hz
Input Current Noise													
f_B=0.01Hz to 10Hz		50			*			*			*		pA, p-p
Density													
f_O=10Hz		0.8			*			*			*		pA/√Hz
f_O=100Hz		0.46			*			*			*		pA/√Hz
f_O=1kHz		0.35			*			*			*		pA/√Hz
DYNAMIC RESPONSE													
Small Signal, ±3dB Flatness													
G = 1		300			*			*			*		kHz
G = 10		140			*			*			*		kHz
G = 100		25			*			*			*		kHz
G = 1000		2.5			*			*			*		kHz
Small Signal, ±1% Flatness													
G = 1		20			*			*			*		kHz
G = 10		10			*			*			*		kHz
G = 100		1			*			*			*		kHz
G = 1000		200			*			*			*		Hz
Full Power, G=1 to 100		6.4			*			*			*		kHz
Slew Rate, G=1 to 100	0.2	0.4		*	*		*	*		*	*		V/µs
Settling Time (0.1%)													
G = 1		30	40		*	*		*	*		*	*	µs
G = 100		40	55		*	*		*	*		*	*	µs
G = 1000		350	470		*	*		*	*		*	*	µs
Settling Time (0.01%)													
G = 1		30	45		*	*		*	*		*	*	µs
G = 100		50	70		*	*		*	*		*	*	µs
G = 1000		500	650		*	*		*	*		*	*	µs
POWER SUPPLY													
Rated Voltage		±15			*			*			*		V
Voltage Range	±5		±20	*		*	*		*	*		*	V
Current, Quiescent[2]		±6.7	±8.5		*	*		*	*		*	*	mA
TEMPERATURE RANGE[5]													
Specification	−25		+85	−55		+125	*		*		0	+70	°C
Operation	−55		+125	*		*	*		*		−25	+85	°C
Storage	−65		+150	*		*	*		*		−40	+85	°C

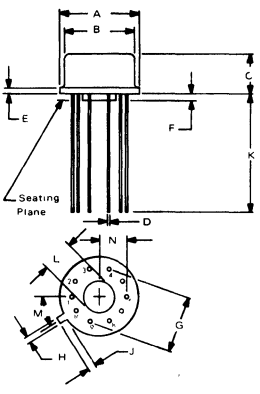
* Specifications same as for INA101AM/AG

NOTES (1) Typically the tolerance of R_G will be the major source of gain error (2) Nonlinearity is the maximum peak deviation from the best straight-line as a percentage of peak-to-peak full scale output. (3) Not including the TCR of R_G (4) Adjustable to zero at any one gain (5) θ_{JC} output stage = 113°C/W, θ_{JC} quiescent circuitry = 19°C/W, θ_{CA} = 83°C/W

MECHANICAL

M Package

TO-100



BOTTOM VIEW

Case = $-V_{CC}$

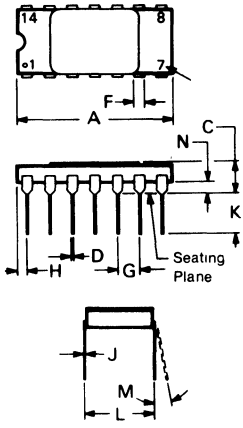
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane

Pin numbers shown for reference only
Numbers may not be marked on package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	–	12.70	
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

G Package

Hermetic DIP

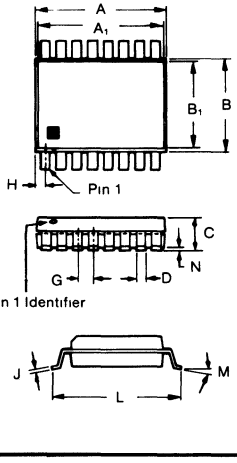


Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	–	10°	–	10°
N	.009	.060	0.23	1.52

U Package

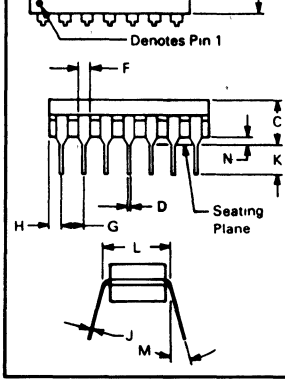


NOTE Leads in true position within .010" (.25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers are not marked on package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.400	.416	10.16	10.57
A_1	.388	.412	9.86	10.46
B	.286	.302	7.26	7.67
B_1	.268	.286	6.81	7.26
C	.093	.109	2.36	2.77
D	.015	.020	0.38	0.51
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.391	.421	9.93	10.69
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

P Package



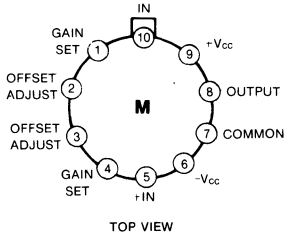
Case = $-V_{CC}$

Leads in true position within 0.10" (0.25mm) R at MMC at seating plane

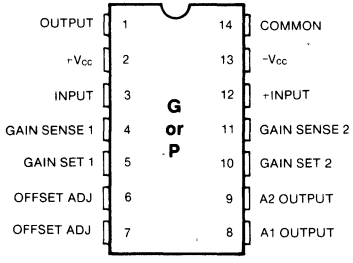
Pin numbers shown for reference only
Numbers may not be marked on package

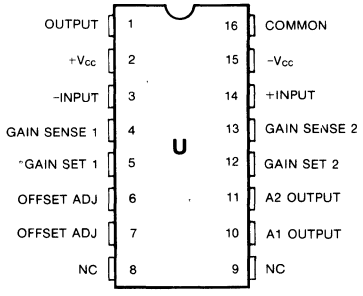
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.660	.785	16.76	19.94
B	.220	.280	5.59	7.11
C	–	.200		5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095		
J	.008	.015	0.20	0.38
K	.100	–	2.54	
L	.300 BASIC		7.62 BASIC	
M	–	15°		15°
N	.020	.050	0.51	1.27

PIN CONFIGURATION



TOP VIEW





ORDERING INFORMATION

Model	Package	Temperature Range
INA101AG	Ceramic DIP	–25°C to +85°C
INA101CG	Ceramic DIP	–25°C to +85°C
INA101AM	Metal TO-100	–25°C to +85°C
INA101CM	Metal TO-100	–25°C to +85°C
INA101HP	Plastic DIP	0°C to +70°C
INA101KU	Plastic SOIC	0°C to +70°C
INA101SG	Ceramic DIP	–55°C to +125°C
INA101SM	Metal TO-100	–55°C to +125°C

BURN-IN SCREENING OPTION
See text for details.

Model	Package	Burn-In Temp. (160h)[1]
INA101AG-BI	Ceramic DIP	125°C
INA101CG-BI	Ceramic DIP	+125°C
INA101AM-BI	Metal TO-100	+125°C
INA101CM-BI	Metal TO-100	+125°C
INA101HP-BI	Plastic DIP	+85°C
INA101KU-BI	Plastic SOIC	+85°C
INA101SG-BI	Ceramic DIP	+125°C
INA101SM-BI	Metal TO-100	+125°C

NOTE: (1) Or equivalent combination. See text.

ABSOLUTE MAXIMUM RATINGS

Supply	±20V
Internal Power Dissipation	600mW
Input Voltage Range	±V_{CC}
Operating Temperature Range M, G	–55°C to +125°C
P, U	–25°C to +85°C
Storage Temperature Range: M, G	–65°C to +150°C
P, U	–40°C to +85°C
Lead Temperature (soldering, 10s) M, G, P	+300°C
Lead Temperature (wave soldering, 3s) U	+260°C
Output Short-Circuit Duration	Continuous to ground

BURN-IN SCREENING

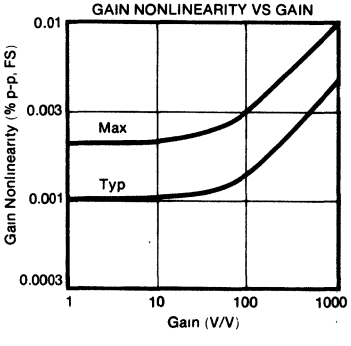
Burn-in screening is an option available for both the plastic- and ceramic-packaged INA101. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

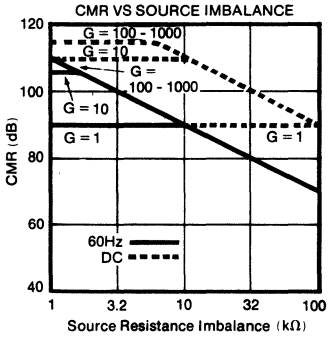
Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

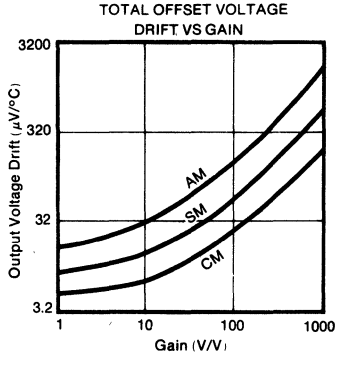
All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

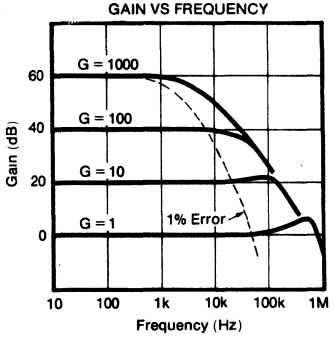
TYPICAL PERFORMANCE CURVES

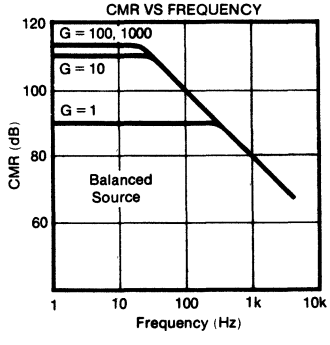
At +25°C and in circuit of Figure 2 unless otherwise noted.

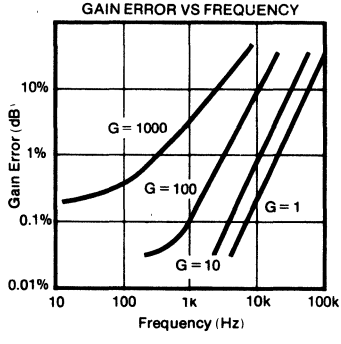


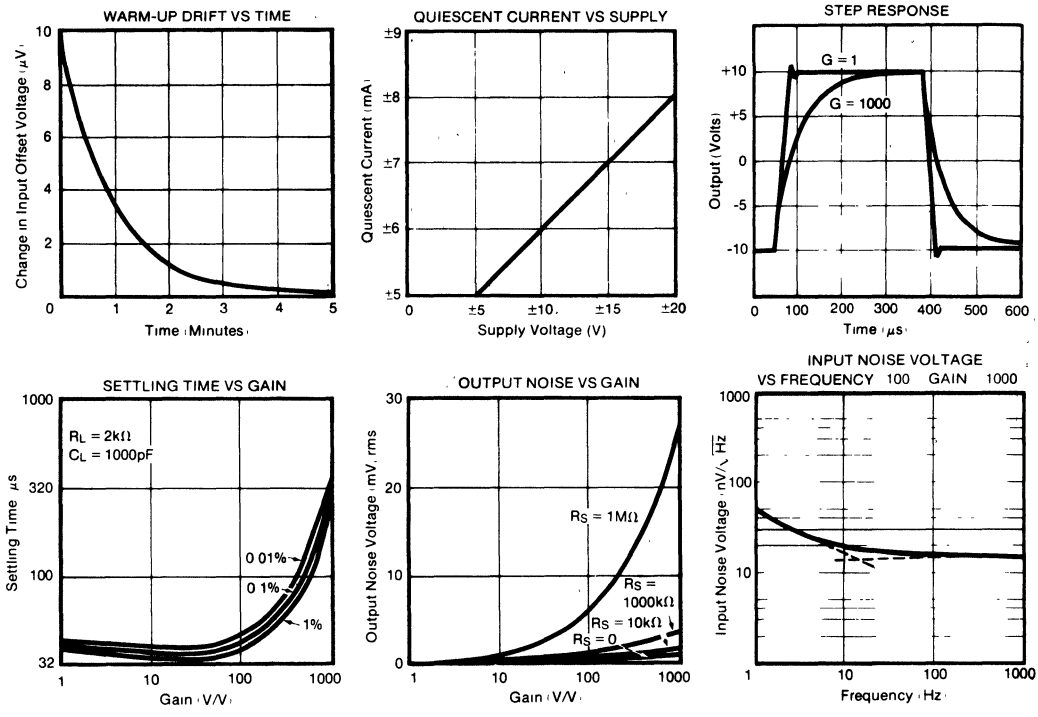












DISCUSSION OF PERFORMANCE

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are differential input closed-loop gain blocks whose committed circuit accurately amplifies the voltage applied to their inputs. They respond only to the difference between the two input signals and exhibit extremely-high input impedance, both differentially and common-mode. Feedback networks are packaged within the amplifier module. Only one external gain setting resistor must be added. An operational amplifier, on the other hand, is an open-loop, uncommitted device that requires external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is very difficult to reach the same level of performance. Using op amps often leads to design trade-offs when it is necessary to amplify low level signals in the presence of common-mode voltages while maintaining high input impedances. Figure 1 shows a simplified model of an instrumentation amplifier that eliminates most of the problems.

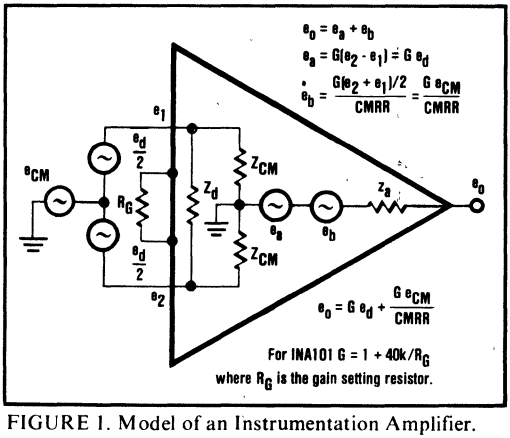


FIGURE 1. Model of an Instrumentation Amplifier.

THE INA101

Simplified schematics of the INA101 are shown on the first page. It is a three-amplifier device which provides all the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found in integrated circuit instrumentation amplifiers.

The input section (A1 and A2) incorporates high performance, low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide the high input impedance ($10^{10}\Omega$) desirable in the instrumentation amplifier function. The offset voltage and offset voltage versus temperature is low due to the monolithic design and improved even further by the state-of-the-art laser-trimming techniques.

The output section (A3) is connected in a unity-gain difference amplifier configuration. A critical part of this stage is the matching of the four 10kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain excellent common-mode rejection. (The 106dB minimum at 60Hz for gains greater than 100V/V is a significant improvement compared to most other integrated circuit instrumentation amplifiers.)

All of the internal resistors are compatible thin-film nichrome formed with the integrated circuit. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. Nichrome ensures long-term stability of trimmed resistors and simultaneous achievement of excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA101 is operated over wide temperature ranges.

USING THE INA101

Figure 2 shows the simplest configuration of the INA101. The gain is set by the external resistor, R_G, with a gain equation of $G = 1 + (40K/R_G)$. The reference and TCR of R_G contribute directly to the gain accuracy and drift.

For gains greater than unity, resistor R_G is connected externally between pins 1 and 4. At high gains where the value of R_G becomes small, additional resistance (i.e., relays, sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect.

The optional offset null capability is shown in Figure 2. The adjustment affects only the input stage component of the offset voltage. Thus, the null condition will be disturbed when the gain is changed. Also, the input drift will be affected by approximately 0.31μV/°C per 100μV of input offset voltage that is trimmed. Therefore, care should be taken when considering use of the control for removal of other sources of offset. Output offsetting can be accomplished in Figure 3 by applying a voltage to Common (pin 7) through a buffer amplifier. This limits the resistance in series with pin 7 to minimize CMR error. Resistance above 0.1Ω will cause the common-mode rejection to fall below 106dB. Be certain to keep this resistance low.

It is important to not exceed the input amplifiers' dynamic range. The amplified differential input signal and its associated common-mode voltage should not cause the output of A_1 or A_2 to exceed approximately ±10V or nonlinear operation will result.

BASIC CIRCUIT CONNECTION

The basic circuit connection for the INA101 is shown in Figure 2. The output voltage is a function of the differential input voltage times the gain.

OPTIONAL OFFSET ADJUSTMENT PROCEDURE

It is frequently desirable to null the input component of offset (Figure 2) and occasionally that of the output (Figure 3). The quality of the potentiometer will affect the results, therefore, choose one with good temperature and mechanical-resistance stability. The procedure is as follows:

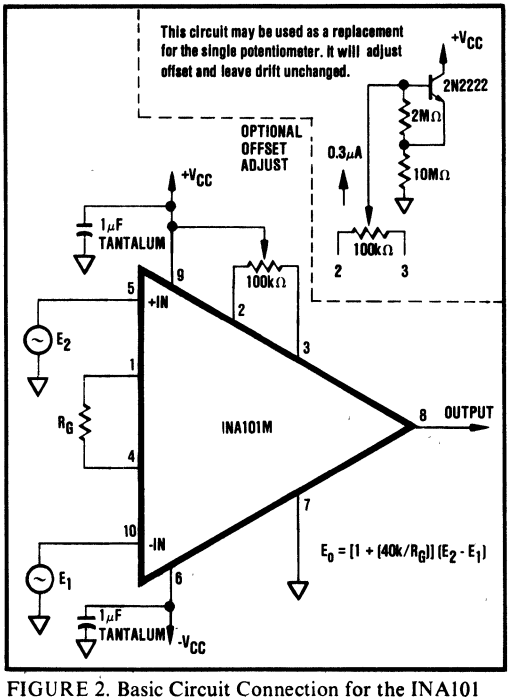


FIGURE 2. Basic Circuit Connection for the INA101 Including Optional Input Offset Null Potentiometer.

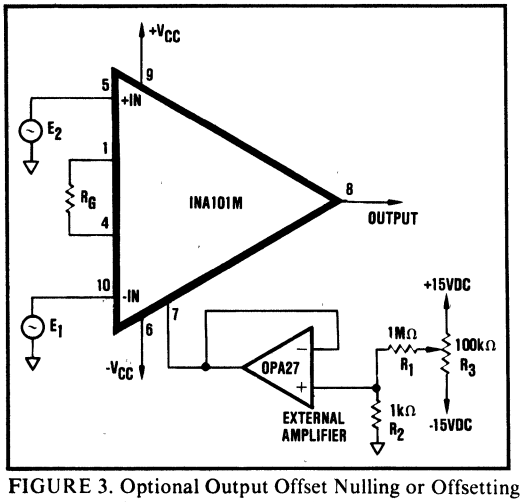


FIGURE 3. Optional Output Offset Nulling or Offsetting Using External Amplifier (Low Impedance to Pin 7).

1. Set $E_1 = E_2 = 0V$ (be sure a good ground return path exists to the input).
2. Set the gain to the desired value by choosing R_G.
3. Adjust to 100kΩ potentiometer in Figure 2 until the output reads 0V ±1mV or desired setting. Note that the offset will change when the gain is changed. If the output component of offset is to be removed or if it is desired to establish an intentional offset, adjust the 100kΩ potentiometer in Figure 3 until the output reads 0V ±1mV or desired setting. Note that the offset will not change with gain, but be sure to use a stable external amplifier with good DC characteristics. The range of adjustment is ±15mV as shown. For larger ranges change the ratio of R_1 to R_2.

THERMAL EFFECTS ON OFFSET

To maintain specified offset performance, especially in high gain, prevent air currents from circulating around the input pins. This can be done by using a skirted heat sink on the INA101M package. Rapid changes in die temperature and thermocouple effects on the pins will then be minimized. Surrounding the package with low power components will also help to reduce air flow across the package and pins.

TYPICAL APPLICATIONS

Many applications of instrumentation amplifiers involve the amplification of low level differential signals from bridges and transducers such as strain gages, thermocouples, and RTD's. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise, see Figure 1), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA101 accomplishes all of these with high precision.

Figures 4 through 16 show some typical applications circuits.

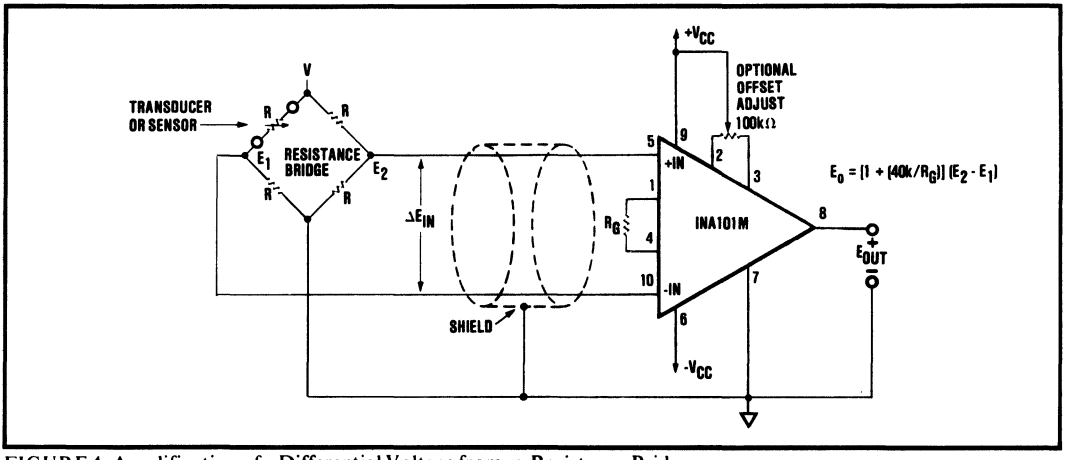


FIGURE 4. Amplification of a Differential Voltage from a Resistance Bridge.

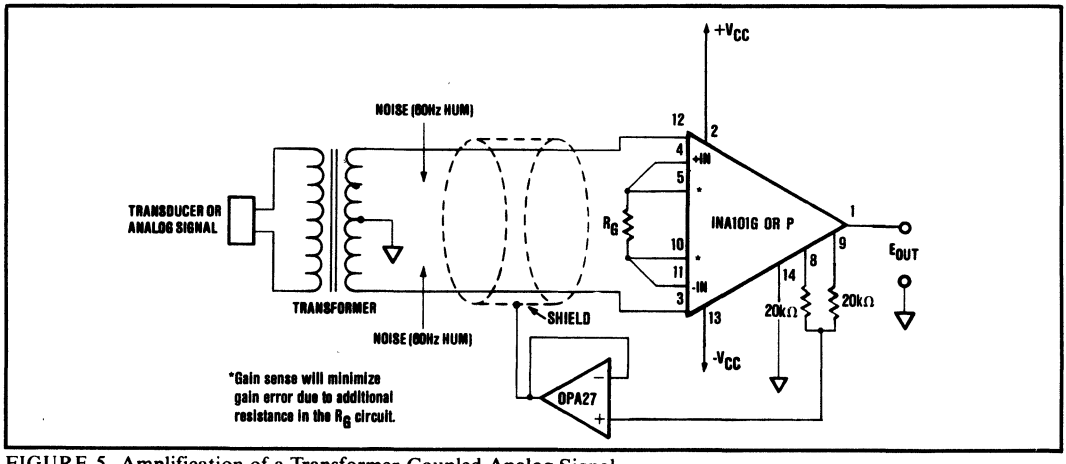


FIGURE 5. Amplification of a Transformer-Coupled Analog Signal.

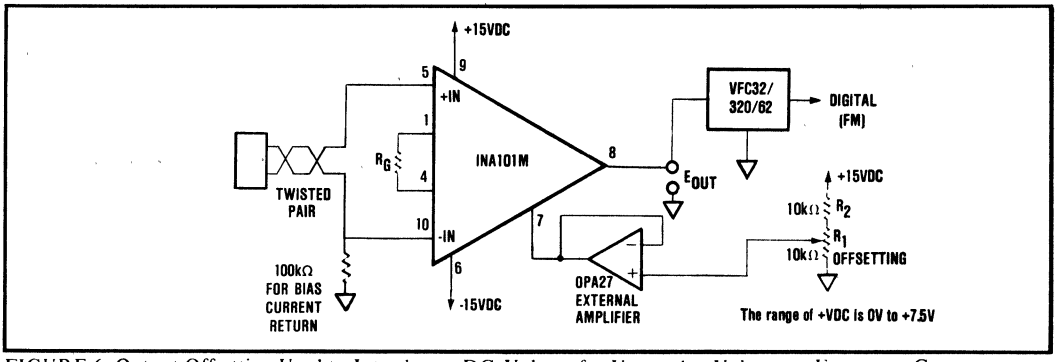


FIGURE 6. Output Offsetting Used to Introduce a DC Voltage for Use with a Voltage-to-Frequency Converter.

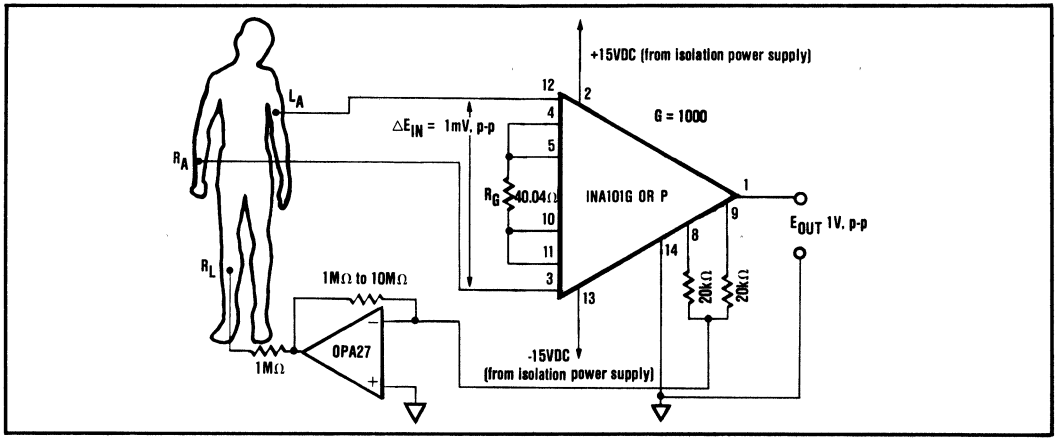


FIGURE 7. ECG Amplifier or Recorder Preamp for Biological Signals.

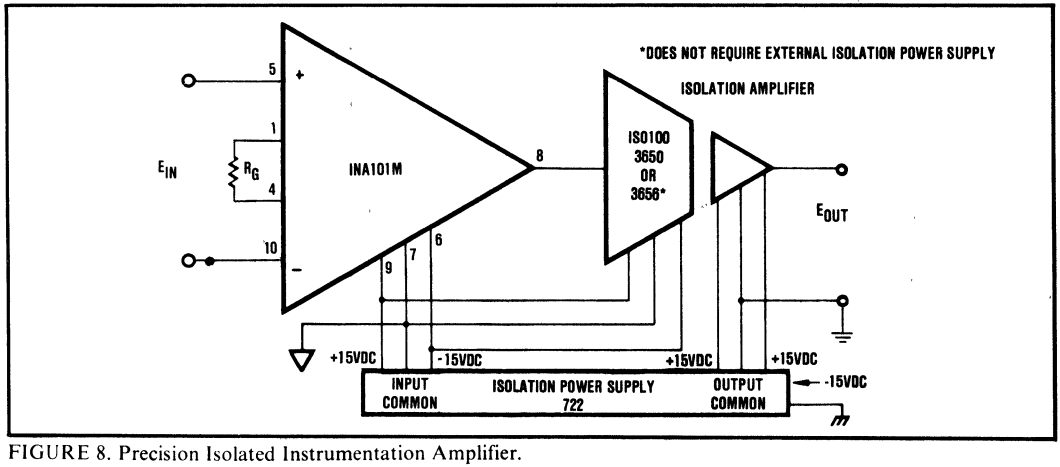


FIGURE 8. Precision Isolated Instrumentation Amplifier.

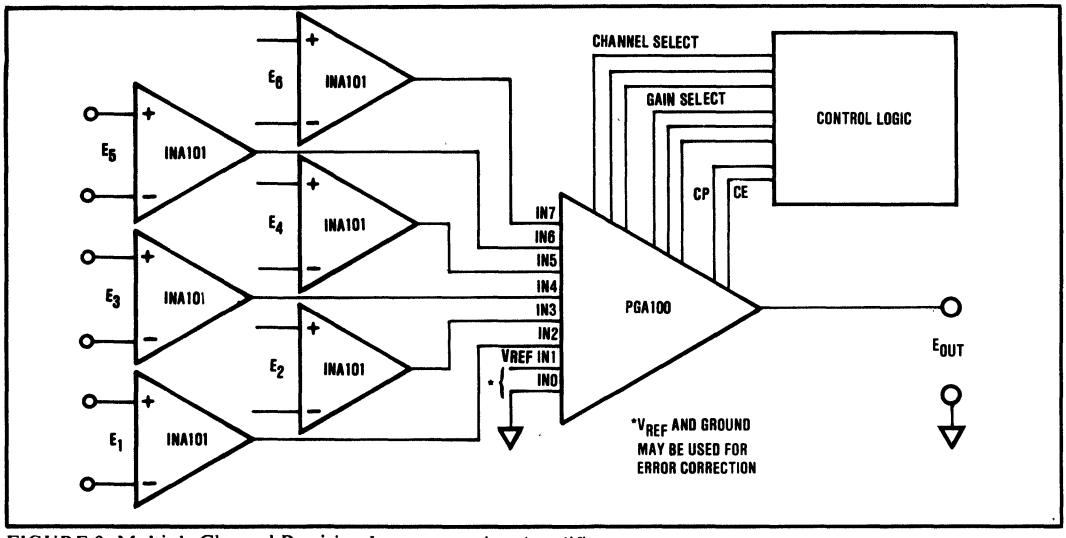


FIGURE 9. Multiple Channel Precision Instrumentation Amplifier.

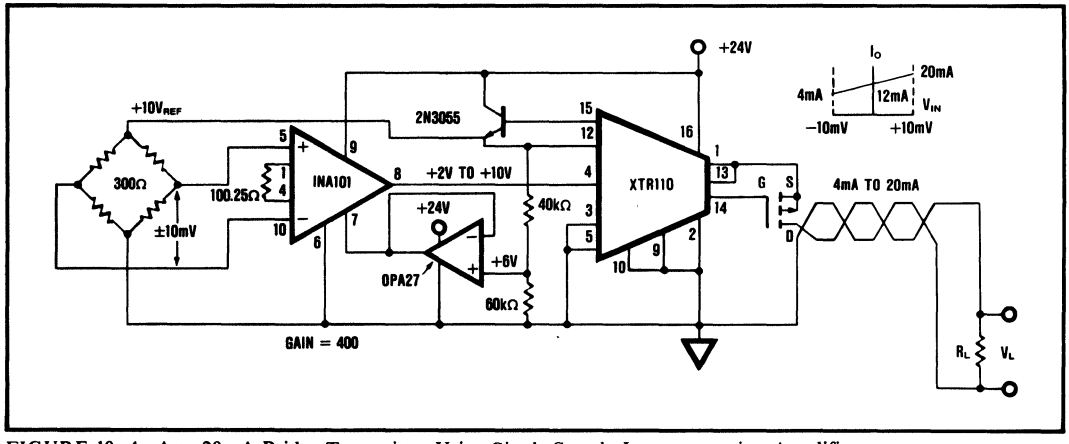


FIGURE 10. 4mA to 20mA Bridge Transmitter Using Single Supply Instrumentation Amplifier.

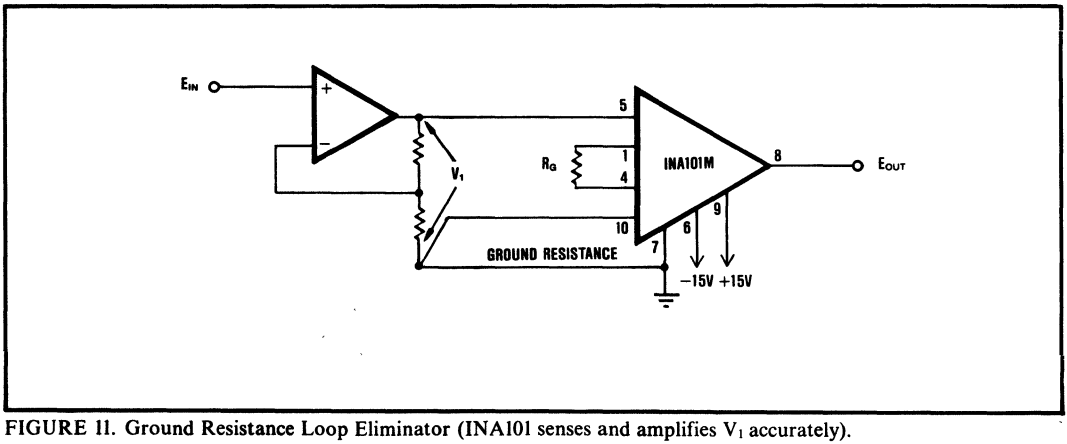


FIGURE 11. Ground Resistance Loop Eliminator (INA101 senses and amplifies V_1 accurately).

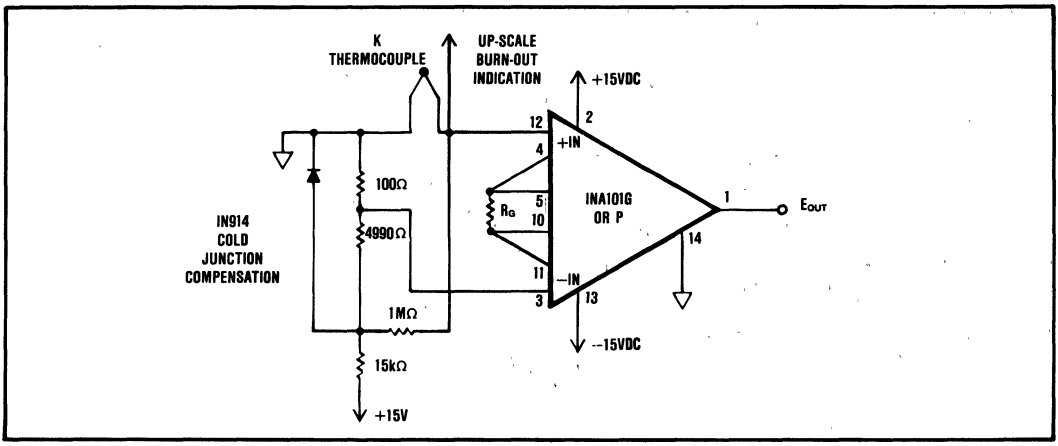


FIGURE 12. Thermocouple Amplifier with Cold Junction Compensation.

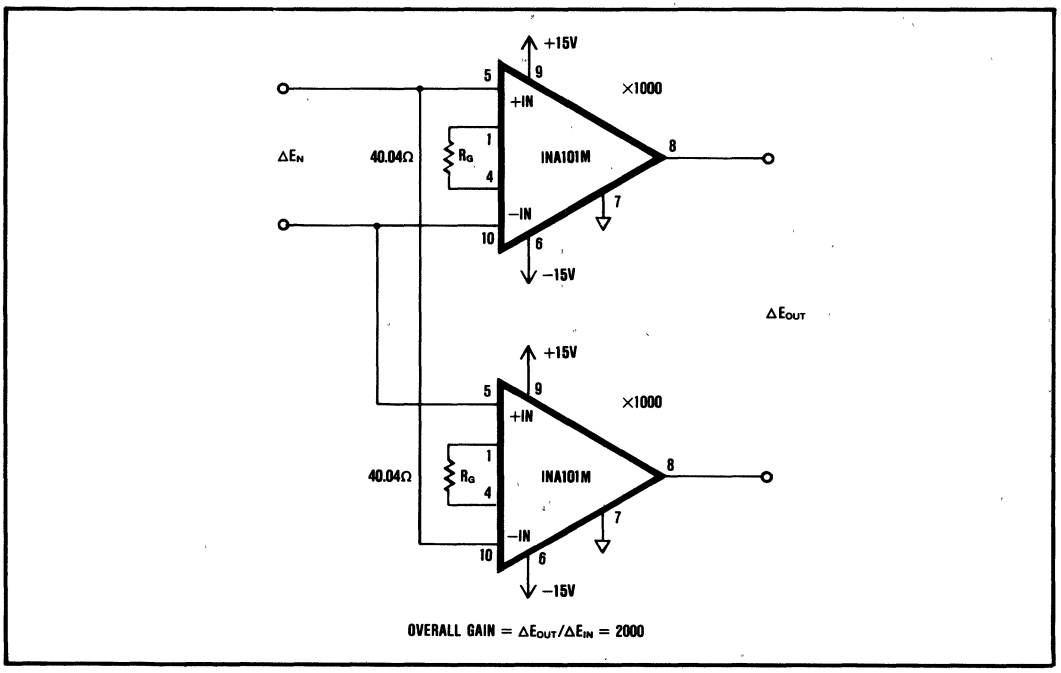
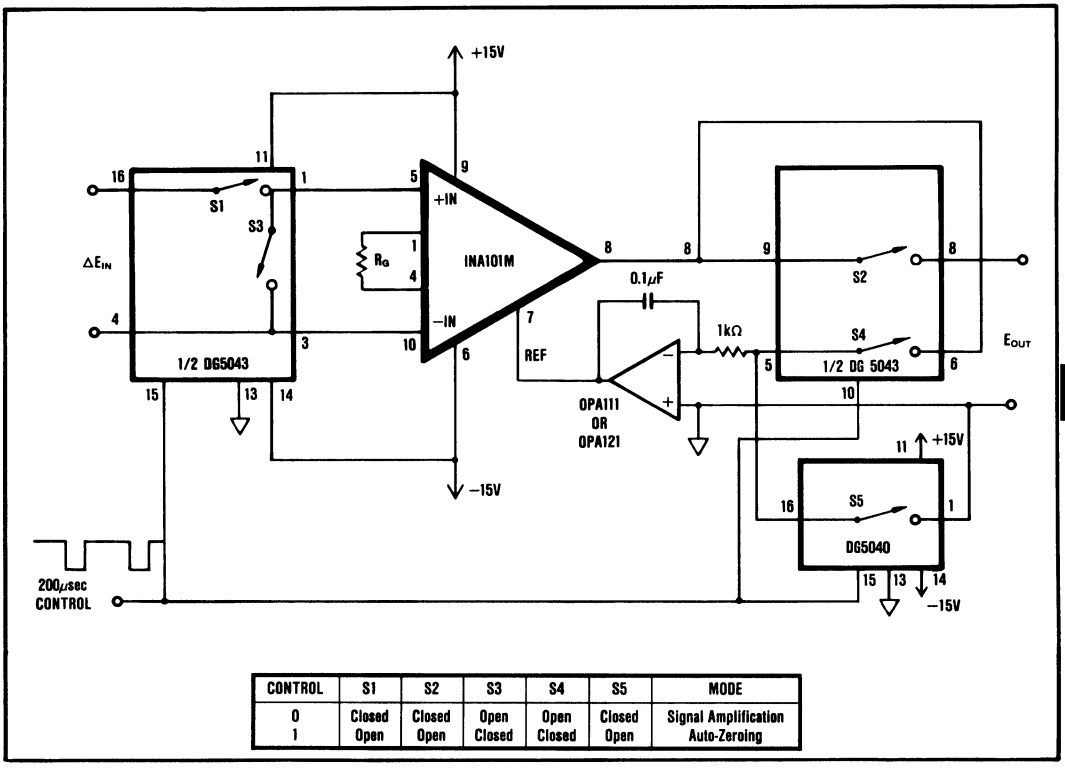
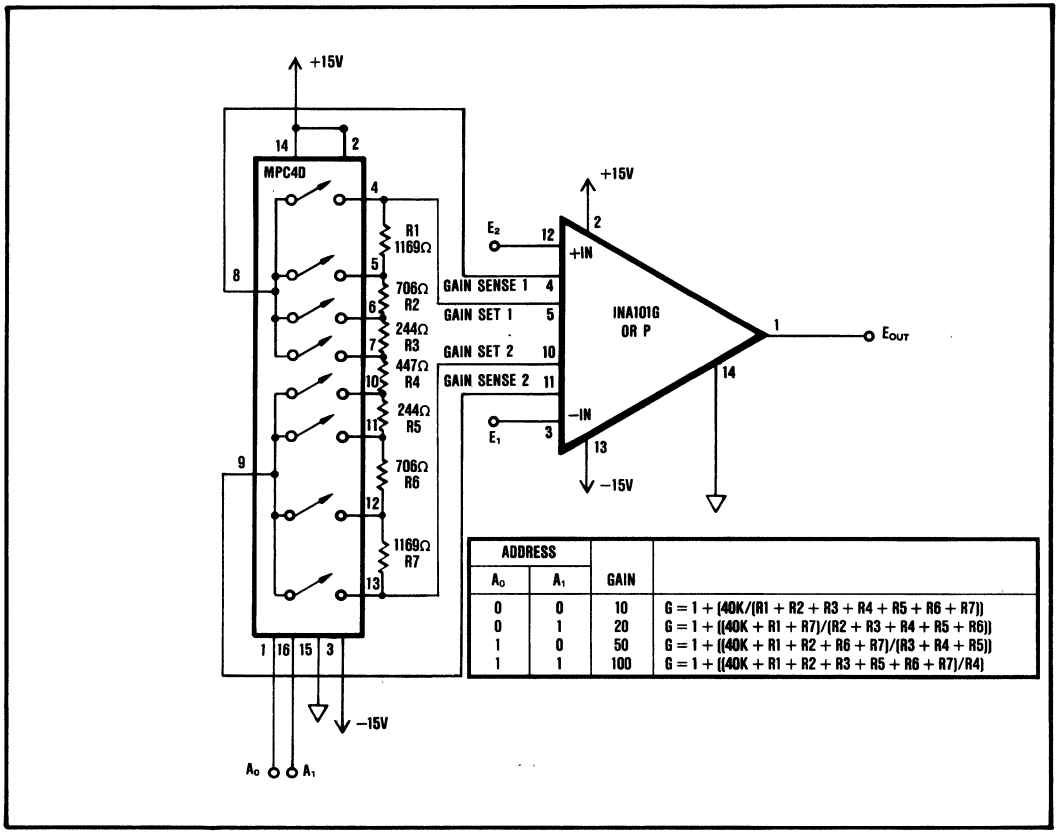


FIGURE 13. Differential Input/Differential Output Amplifier (twice the gain of one INA).



CONTROL	S1	S2	S3	S4	S5	MODE
0	Closed	Closed	Open	Open	Closed	Signal Amplification
1	Open	Open	Closed	Closed	Open	Auto-Zeroing

FIGURE 14. Auto-Zeroing Instrumentation Amplifier Circuit.



ADDRESS			
A_0	A_1	GAIN	
0	0	10	G = 1 + (40K/(R1 + R2 + R3 + R4 + R5 + R6 + R7))
0	1	20	G = 1 + ((40K + R1 + R7)/(R2 + R3 + R4 + R5 + R6))
1	0	50	G = 1 + ((40K + R1 + R2 + R6 + R7)/(R3 + R4 + R5))
1	1	100	G = 1 + ((40K + R1 + R2 + R3 + R5 + R6 + R7)/R4)

FIGURE 15. Programmable Gain Instrumentation Amplifier.

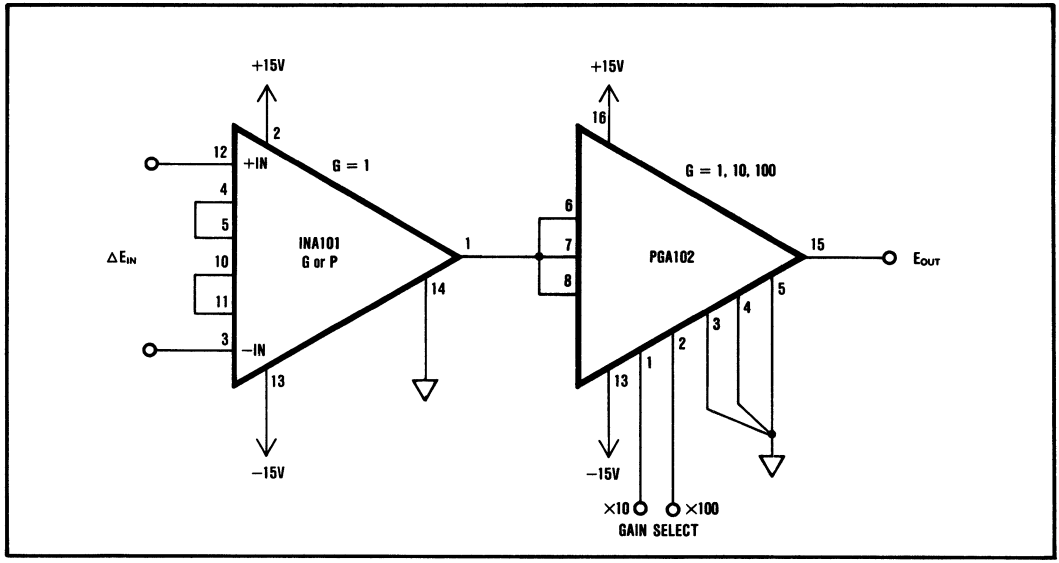


FIGURE 16. Programmable-Gain Instrumentation Amplifier Using the INA101 and PGA102.

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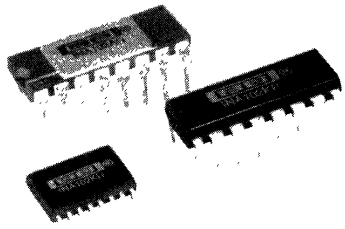


INA102

AVAILABLE IN DIE FORM

Low-Power, High-Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- LOW-QUIESCENT POWER: 750μA, max
- INTERNAL GAINS: 1, 10, 100, 1000
- LOW-GAIN DRIFT: 5ppm/°C, max
- HIGH CMR: 90dB, min
- LOW-OFFSET VOLTAGE DRIFT: 2μV/°C, max
- LOW-OFFSET VOLTAGE: 100μV, max
- LOW NONLINEARITY: 0.01%, max
- HIGH-INPUT IMPEDANCE: $10^{10}\Omega$
- LOW COST

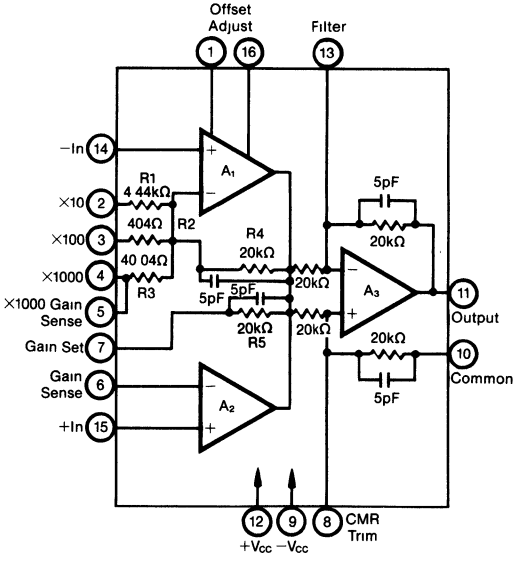
APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gauges
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCER AMPLIFIER
- LOW-LEVEL SIGNAL AMPLIFIER
- MEDICAL INSTRUMENTATION
- MULTICHANNEL SYSTEMS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

The INA102 is a high-accuracy monolithic instrumentation amplifier designed for signal-conditioning applications where low-quiescent power is desired. On-chip thin-film resistors provide excellent temperature and stability performance. State-of-the-art laser-trimming technology insures high-gain accuracy and common-mode rejection while avoiding expensive external components. These features make the INA102 ideally suited for battery powered and high-volume applications.

The INA102 is also convenient to use. A gain of 1, 10, 100 or 1000 may be selected by simply strapping the appropriate pins together. 5ppm/°C gain drift in low gains can then be achieved without external adjustment. When higher than specified CMR is required, CMR can be trimmed using the pins provided. In addition, balanced filtering can be accomplished in the output stage.



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PDS-523D

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C with ±15VDC power supply and in circuit of Figure 2 unless otherwise noted.

KU IS ADVANCE INFORMATION

MODEL	CONDITIONS	INA102AG			INA102CG			INA102KP/KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Range of Gain		1		1000	*		*	*		*	V/V
Gain Equation,			G = 1 +								
External, ±20%			(40k/R_G)[1]			*			*		V/V
Error, DC: G = 1	T_A = +25°C			0.1			0.05			0.15	%
G = 10	T_A = +25°C			0.1			0.05			0.35	%
G = 100	T_A = +25°C			0.25			0.15			0.4	%
G = 1000	T_A = +25°C			0.75			0.5			0.9	%
G = 1	$T_A = T_{MIN}$ to T_{MAX}			0.16			0.08			0.21	%
G = 10	$T_A = T_{MIN}$ to T_{MAX}			0.19			0.11			0.44	%
G = 100	$T_A = T_{MIN}$ to T_{MAX}			0.37			0.21			0.52	%
G = 1000	$T_A = T_{MIN}$ to T_{MAX}			0.93			0.62			1.08	%
Gain Temp. Coefficient											
G = 1				10			5			*	ppm/°C
G = 10				15			10			*	ppm/°C
G = 100				20			15			*	ppm/°C
G = 1000				30			20			*	ppm/°C
Nonlinearity, DC											
G = 1	T_A = +25°C			0.03			0.01			*	% of FS
G = 10	T_A = +25°C			0.03			0.01			*	% of FS
G = 100	T_A = +25°C			0.05			0.02			*	% of FS
G = 1000	T_A = +25°C			0.1			0.05			*	% of FS
G = 1	$T_A = T_{MIN}$ to T_{MAX}			0.045			0.015			*	% of FS
G = 10	$T_A = T_{MIN}$ to T_{MAX}			0.045			0.015			*	% of FS
G = 100	$T_A = T_{MIN}$ to T_{MAX}			0.075			0.03			*	% of FS
G = 1000	$T_A = T_{MIN}$ to T_{MAX}			0.15			0.1			*	% of FS
RATED OUTPUT											
Voltage	R_L = 10kΩ	±(|V_{CC}| −2.5)			*			*			V
Current		±1			*			*			mA
Short-Circuit Current[2]			2			*			*		mA
Output Impedance											
G = 1000			0.1			*			*		Ω
INPUT											
OFFSET VOLTAGE											
Initial Offset[3]	T_A = +25°C			±300			±100			*	μV
				±300/G			±200/G				
vs Temperature				±5			±2			*	μV/°C
				±10/G			±5/G				
vs Supply				±40			±10			*	μV/V
				±50/G			±20/G				
vs Time			±(20								
			+30/G)			*			*		μV/mo
BIAS CURRENT											
Initial Bias Current											
(each input)	$T_A = T_{MIN}$ to T_{MAX}		25	50		6	30		*	*	nA
vs Temperature			±0.1			*			*		nA/°C
vs Supply			±0.1			*			*		nA/V
Initial Offset Current	$T_A = T_{MIN}$ to T_{MAX}		±2.5	±15		±2.5	±10		*	*	nA
vs Temperature			±0.1			*			*		nA/°C
IMPEDANCE											
Differential			10^{10}||2			*			*		Ω||pF
Common-mode			10^{10}||2			*			*		Ω||pF
VOLTAGE RANGE											
Range, Linear Response	$T_A = T_{MIN}$ to T_{MAX}	±(|V_{CC}| −4.5)			*			*			V
CMR with 1kΩ											
Source Imbalance											
G = 1	DC to 60 Hz	80	94		90	*		75	*		dB
G = 10	DC to 60 Hz	80	100		90	*		*	*		dB
G = 10 to 1000	DC to 60 Hz	80	100		90	*		*	*		dB
NOISE											
Input Voltage Noise											
f_B = 0.01Hz to 10Hz			1.0			*			*		μVp-p
Density, G = 1000											
f_O = 10Hz			30			*			*		nV/√Hz
f_O = 100Hz			25			*			*		nV/√Hz
f_O = 1kHz			25			*			*		nV/√Hz
Input Current Noise											
f_B = 0.01Hz to 10Hz			25			*			*		pA p-p
Density: f_O = 10Hz			0.3			*			*		pA/√Hz
f_O = 100Hz			0.2			*			*		pA/√Hz
f_O = 1kHz			0.15			*			*		pA/√Hz

ELECTRICAL (CONT)

KU IS ADVANCE INFORMATION

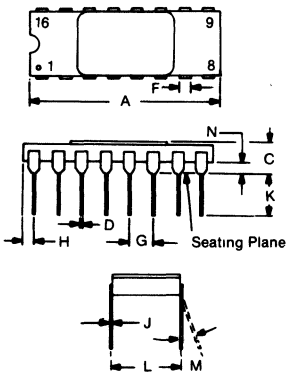
MODEL	CONDITIONS	INA102AG			INA102CG			INA102KP/KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC RESPONSE											
Small Signal											
±3dB Flatness	V_{OUT} = 0 1Vrms										
G = 1			300			*					kHz
G = 10			30			*					kHz
G = 100			3			*					kHz
G = 1000			0.3			*					kHz
Small Signal,											
±1% Flatness	V_{OUT} = 0 1Vrms										
G = 1			30			*					kHz
G = 10			3			*					kHz
G = 100			0 3			*					kHz
G = 1000			0 03			*					kHz
Full Power, G = 1 to 100	V_{OUT}=10V, R_L=10kΩ	1 7	2 5		*	*					kHz
Slew Rate, G = 1 to 100	V_{OUT}=10V, R_L=10kΩ	0 1	0 15		*	*					V/μs
Settling Time	R_L=10kΩ, C_L=100pF										
0 1% G = 1	10V step		50			*					μs
G = 100			360			*					μs
G = 1000			3300			*					μs
0 01% G = 1	10V step		60			*					μs
G = 100			500			*					μs
G = 1000			4500			*					μs
POWER SUPPLY											
Rated Voltage			±15			*					V
Voltage Range		±3 5		±18	*		*	*		*	V
Quiescent Current	V_O = 0V,										
	$T_A = T_{MIN}$ to T_{MAX}		±500	±750		*	*				μA
TEMPERATURE RANGE											
Specification		−25		+85	*		*	0		+70	°C
Operation	$R_L > 50k\Omega$[2]	−25		+85	*		*	−25		+85	°C
Storage		−65		+150	*		*	−55		+125	°C

*Specification same as for INA102AG

NOTES (1) The internal gain set resistors have an absolute tolerance of ±20%, however, their tracking is 50ppm/°C R_G will add to the gain error if gains other than 1, 10, 100 or 1000 are set externally (2) At high temperature, output drive current is limited An external buffer can be used if required (3) Adjustable to zero at any one time

MECHANICAL

Hermetic



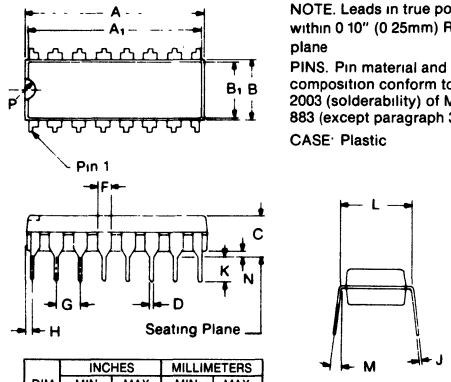
NOTE: Leads in true position within 0 10" (0 25mm) R at seating plane

Pin numbers shown for reference only Numbers are not marked on package

CASE Ceramic

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	790	810	20 07	20 57
C	105	170	2 67	4 32
D	015	021	0 38	0 53
F	048	060	1 22	1 52
G	100 BASIC		2 54 BASIC	
H	030	070	0 76	1 78
J	008	012	0 20	0 30
K	120	240	3 05	6 10
L	300 BASIC		7 62 BASIC	
M	—	10°	—	10°
N	025	060	0 64	1 52

Plastic



NOTE. Leads in true position within 0 10" (0 25mm) R at seating plane

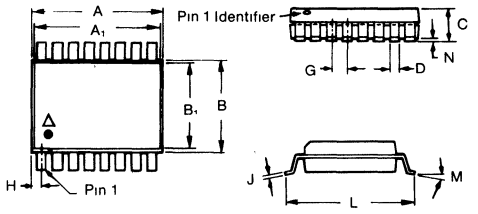
PINS. Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3 2)

CASE· Plastic

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	740	800	18 80	20 32
A_1	725	785	18 42	19 94
B	230	290	5 85	7 38
B_1	200	250	5 09	6 36
C	120	200	3 05	5 09
D	015	023	0 38	0 59
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	0 02	0 05	0 51	1 27
J	008	015	0 20	0 38
K	070	150	1 78	3 82
L	.300 BASIC		7 63 BASIC	
M	0°	15°	0°	15°
N	010	030	0 25	0 76
P	025	050	0 64	1 27

MECHANICAL

SOIC

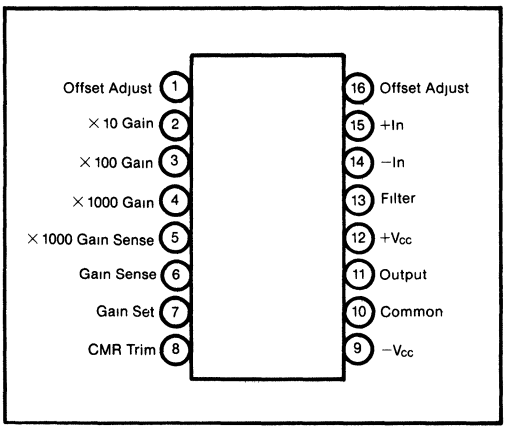


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	400	416	10 16	10 57
A_1	388	412	9 86	10 46
B	286	302	7 26	7 67
B_1	268	286	6 81	7 26
C	093	109	2 36	2 77
D	015	020	0 38	0 51
G	050 BASIC		1 27 BASIC	
H	022	038	0 56	0 97
J	008	012	0 20	0 30
L	391	421	9 93	10 69
M	5° TYP		5° TYP	
N	000	012	0 00	0 30

NOTE Leads in true position within .010" (25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers are not marked on package.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply	±18V
Input Voltage Range	±V_{CC}
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range: Ceramic	−65°C to +150°C
Plastic	−55°C to +125°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-Circuit Duration	Continuous to ground

ORDERING INFORMATION

Model	Package	Temperature Range
INA102AG	Ceramic DIP	−25°C to +85°C
INA102CG	Ceramic DIP	−25°C to +85°C
INA102KP	Plastic DIP	0°C to +70°C
INA102KU	Plastic SOIC	0°C to +70°C
BURN-IN SCREENING OPTION See text for details		
Model	**Package**	**Burn-In Temp. (160h)[1]**
INA102AG-BI	Ceramic DIP	+125°C
INA102CG-BI	Ceramic DIP	+125°C
INA102KP-BI	Plastic DIP	+85°C
INA102KU-BI	Plastic SOIC	+85°C

NOTE (1) Or equivalent combination See text.

BURN-IN SCREENING

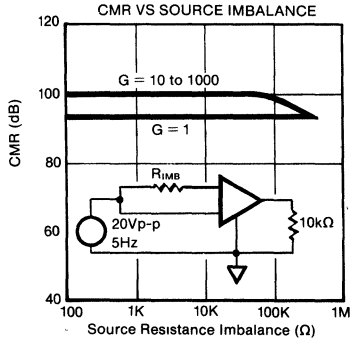
Burn-in screening is an option available for both plastic- and ceramic-packaged INA102s. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

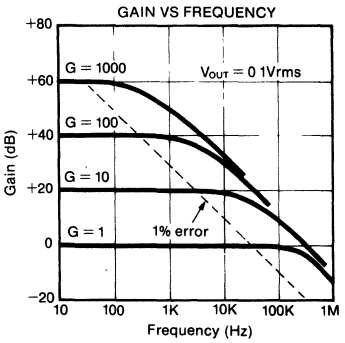
Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

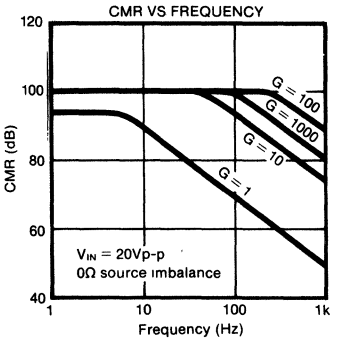
All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

TYPICAL PERFORMANCE CURVES

At +25°C and in circuit of Figure 2 unless otherwise noted

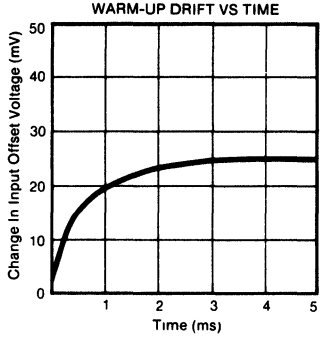


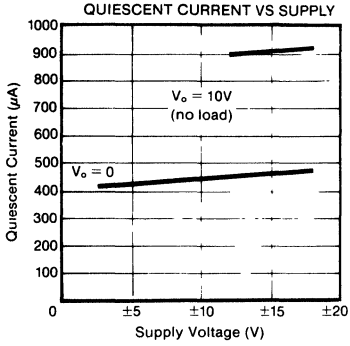


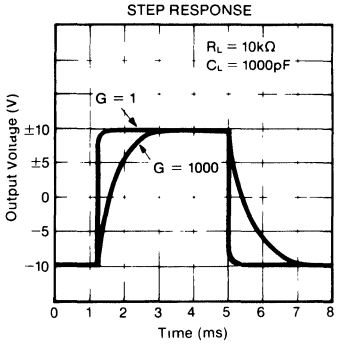


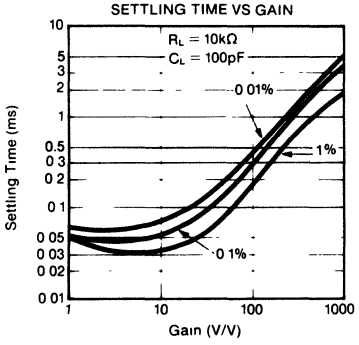
TYPICAL PERFORMANCE CURVES (CONT)

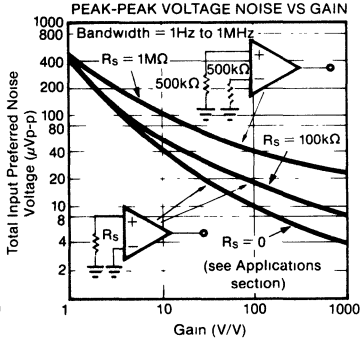
At +25°C and in circuit of Figure 2 unless otherwise noted

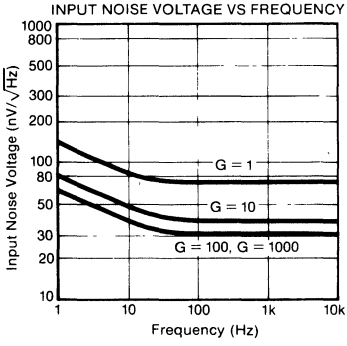


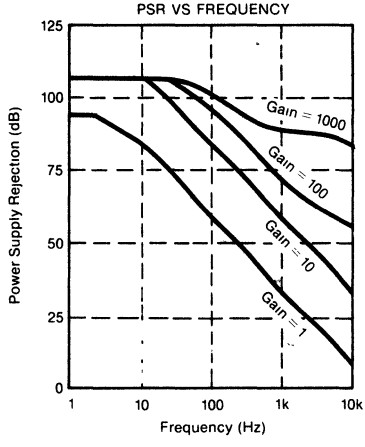












DISCUSSION OF PERFORMANCE

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are differential input closed-loop gain blocks whose committed circuit accurately amplifies the voltage applied to their inputs. They respond mainly to the difference between the two input signals and exhibit extremely high input impedance, both differentially and common-mode. The feedback networks of this instrumentation amplifier is included on the monolithic chip. No external resistors are required for gains of 1, 10, 100, and 1000 in the INA102.

An operational amplifier, on the other hand, is an open-loop, uncommitted device that requires external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is very difficult to reach the same level of performance. Using op amps often leads to design tradeoffs when it is necessary to amplify low-level signals in the presence of common-mode voltages while maintaining high-input impedances. Figure 1 shows a simplified model of an instrumentation amplifier that eliminates most of the problems.

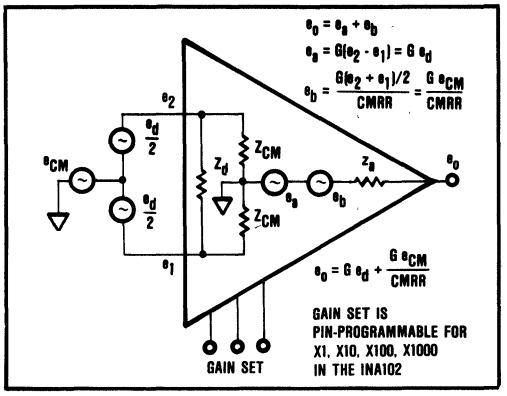


FIGURE 1. Model of an Instrumentation Amplifier.

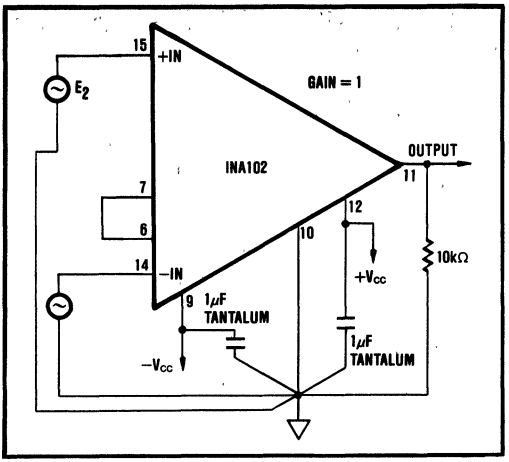


FIGURE 2. Basic Circuit Connection for the INA102.

THE INA102

A simplified schematic of the INA102 is shown on the first page. A three-amplifier configuration is used to provide the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found in integrated circuit instrumentation amplifiers.

The input buffers (A1 and A2) incorporate high performance, low-drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide the high input impedance ($10^{10}\Omega$) desirable in instrumentation amplifier applications. The offset voltage and offset voltage versus temperature are low due to the monolithic design, and improved even further by state-of-the-art laser-trimming techniques.

The output stage (A3) is connected in a unity-gain differential amplifier configuration. A critical part of this stage is the matching of the four 20kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain good common-mode rejection.

All of the internal resistors are made of thin-film nichrome on the integrated circuit. The critical resistors are laser-trimmed to provide the desired high-gain accuracy and common-mode rejection. Nichrome ensures long-term stability and provides excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA102 is operated over wide temperature ranges.

USING THE INA102

Figure 2 shows the simplest configuration of the INA102. The output voltage is a function of the differential input voltage times the gain.

A gain of 1, 10, 100, or 1000 is selected by programming pins 2 through 7 (see Table I). Notice that for the gain of 1000, a special gain sense is provided to preserve accuracy. Although this is not always required, gain errors caused by external resistance in series with the low value 40.04Ω internal gain set resistor are thus eliminated.

Other gains between 1 and 10, 10 and 100, and 100 and 1000 can also be obtained by connecting an external resistor between pin 6 and either pin 2, 3, or 4, respectively (see Figure 6 for application).

$G = 1 + (40/R_G)$ where R_G is the total resistance between the two inverting inputs of the input op amps. At high gains, where the value of R_G becomes small, additional resistance (i.e., relays or sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect.

TABLE I. Pin-Programmable Gain Connections

GAIN	CONNECT PINS
1	6 to 7
10	2 to 6 and 7
100	3 to 6 and 7
1000	4 to 7 and separately 5 to 6

OPTIONAL OFFSET ADJUSTMENT PROCEDURE

It is sometimes desirable to null the input and/or output offset to achieve higher accuracy. The quality of the potentiometer will affect the results; therefore, choose one with good temperature and mechanical-resistance stability.

The optional offset null capabilities are shown in Figure 3. R_4 adjustment affects only the input stage component of the offset voltage. Note that the null condition will be disturbed when the gain is changed. Also, the input drift will be affected by approximately 0.31μV/°C per 100μV of input offset voltage that is trimmed. Therefore, care should be taken when considering use of the control for removal of other sources of offset. Output offset correction can be accomplished with A_1, R_1, R_2, and R_3, by applying a voltage to Common (pin 10) through a buffer amplifier. This buffer limits the resistance in series with pin 10 to minimize CMR error. Resistance above 0.1Ω will cause the common-mode rejection to fall below 100dB. Be certain to keep this resistance low.

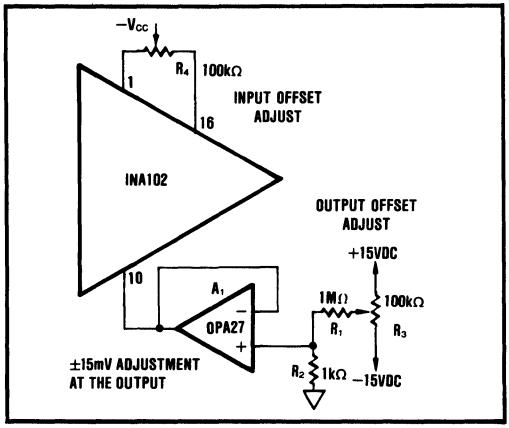


FIGURE 3. Optional Offset Nulling

It is important to not exceed the input amplifiers' dynamic range. The amplified differential input signal and its associated common-mode voltage should not cause the output of A_1 or A_2 to exceed approximately ±12V with ±15V supplies or nonlinear operation will result. To protect against moisture, especially in high gain, sealing compound may be used. Current injected into the offset pins should be minimized.

OPTIONAL FILTERING

The INA102 has provisions for accomplishing filtering with one external capacitor between pins 11 and 13. This single-pole filter can be used to reduce noise outside the signal bandwidth, but with some degradation to AC CMR.

When it is important to preserve CMR versus frequency (especially at 60Hz), two capacitors should be used. The additional capacitor is connected between pins 8 and 10. This will maintain a balance of impedances in the output stage. Either of these capacitors could also be trimmed slightly, to maximize CMR, if desired. Note that their ratio tracking will affect CMR over temperature.

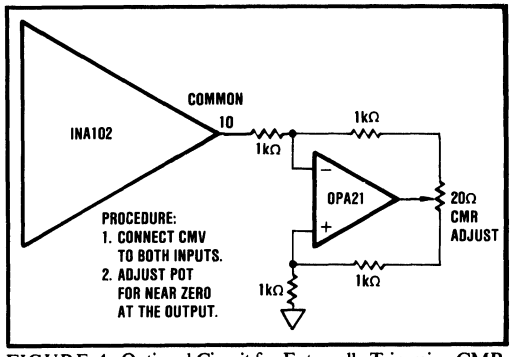


FIGURE 4. Optional Circuit for Externally Trimming CMR.

OPTIONAL COMMON-MODE REJECTION TRIM

The INA102 is laser-adjusted during manufacturing to assure high CMR. However, if desired, a small resistance can be added in series with pin 10 to trim the CMR to an improved level. Depending upon the nature of the internal imbalances, either a positive or negative resistance value could be required. The circuit shown in Figure 4 acts as a bipolar potentiometer and allows easy adjustment of CMR.

TYPICAL APPLICATIONS

Many applications of instrumentation amplifiers involve the amplification of low-level differential signals from bridges and transducers such as strain gauges, thermocouples, and RTDs. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise, see Figure 1), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA102 accomplishes all of these with high precision at surprisingly low-quiescent current. However, in higher gains (>100), the bias current can cause a large offset error at the output. This can saturate the output unless the source impedance is separated, e.g., two 500kΩ paths instead of one 1MΩ unbalanced input.

Figures 5 through 16 show some typical applications circuits.

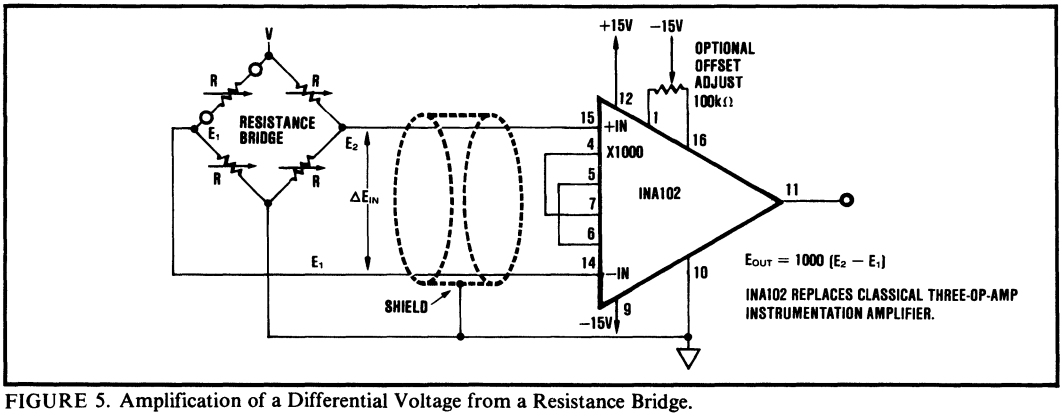


FIGURE 5. Amplification of a Differential Voltage from a Resistance Bridge.

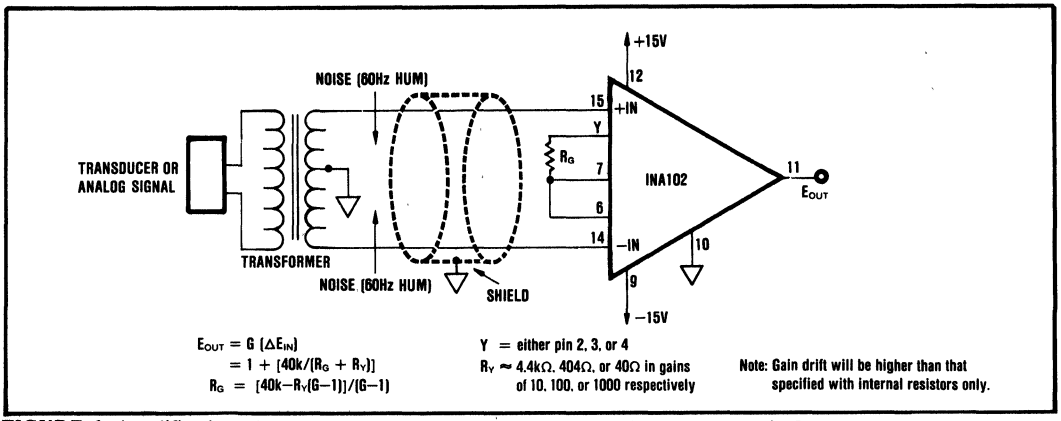


FIGURE 6. Amplification of a Transformer-Coupled Analog Signal Using External Gain Set.

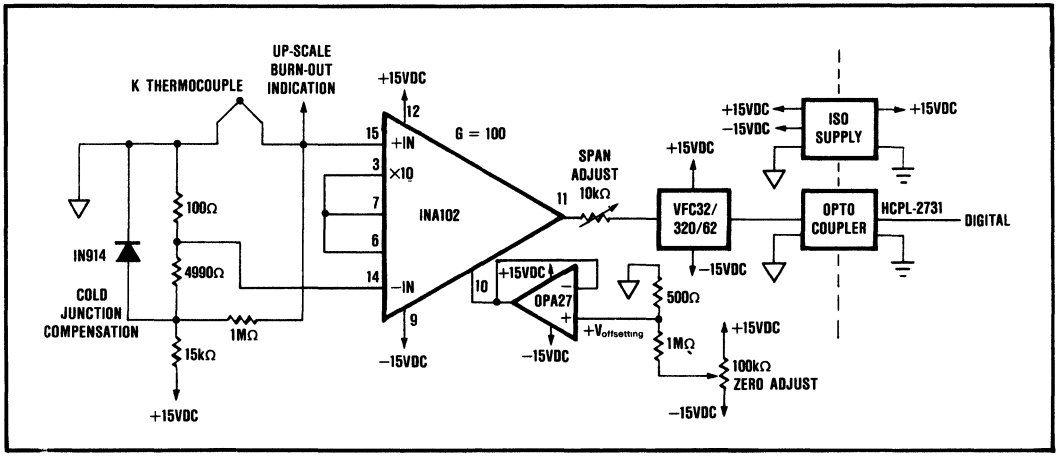


FIGURE 7. Isolated Thermocouple Amplifier with Cold Junction Compensation.

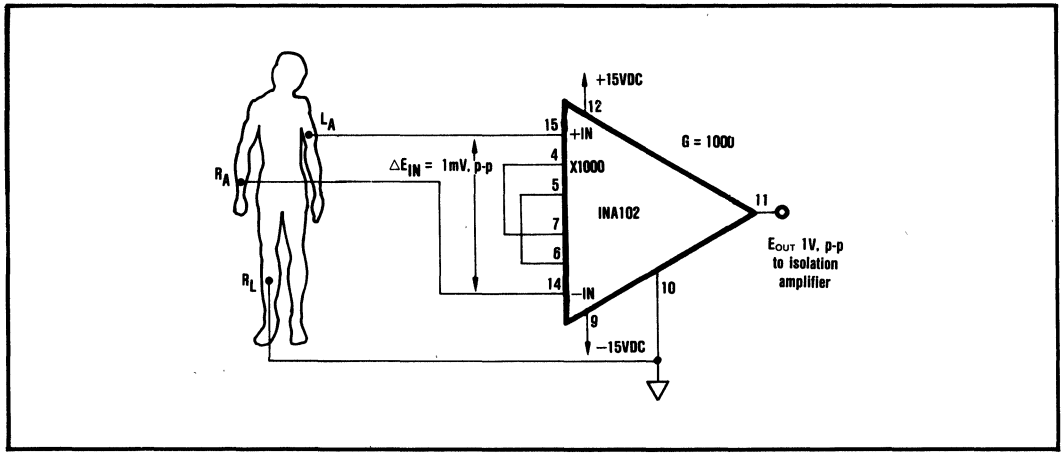


FIGURE 8. ECG Amplifier or Recorder Preamp for Biological Signals.

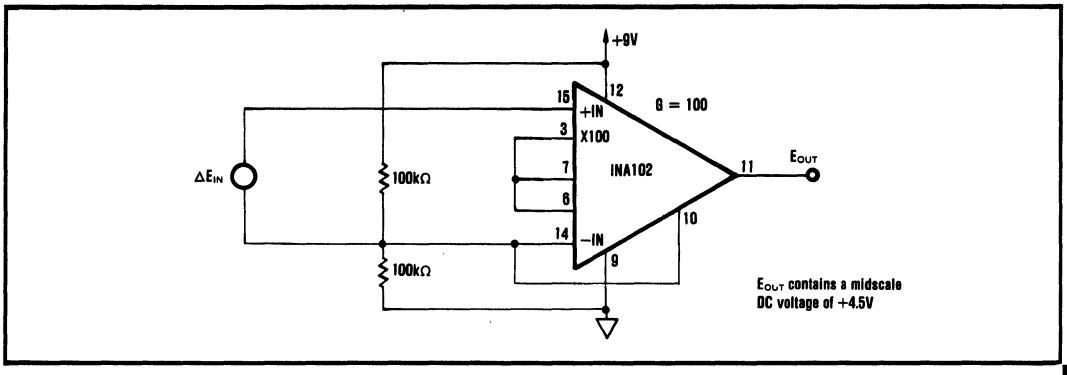


FIGURE 9. Single Supply Low Power Instrumentation Amplifier.

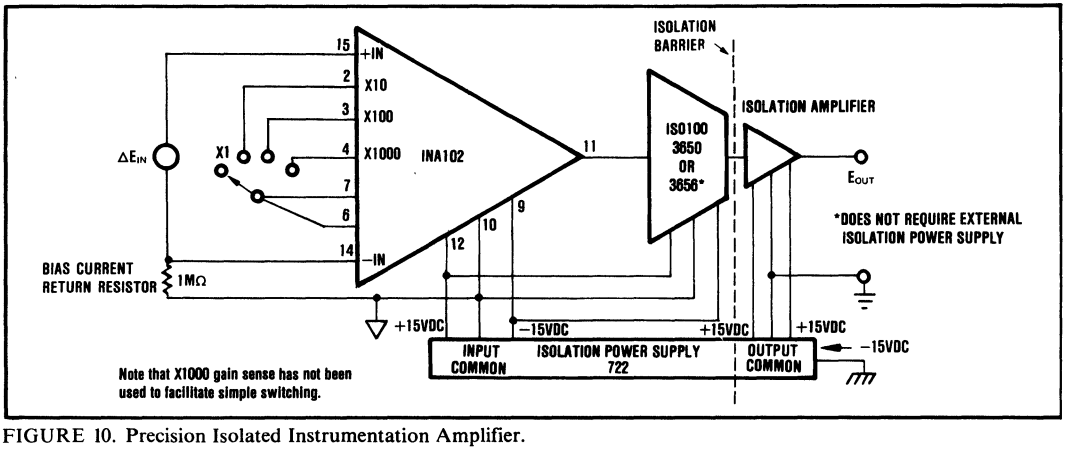


FIGURE 10. Precision Isolated Instrumentation Amplifier.

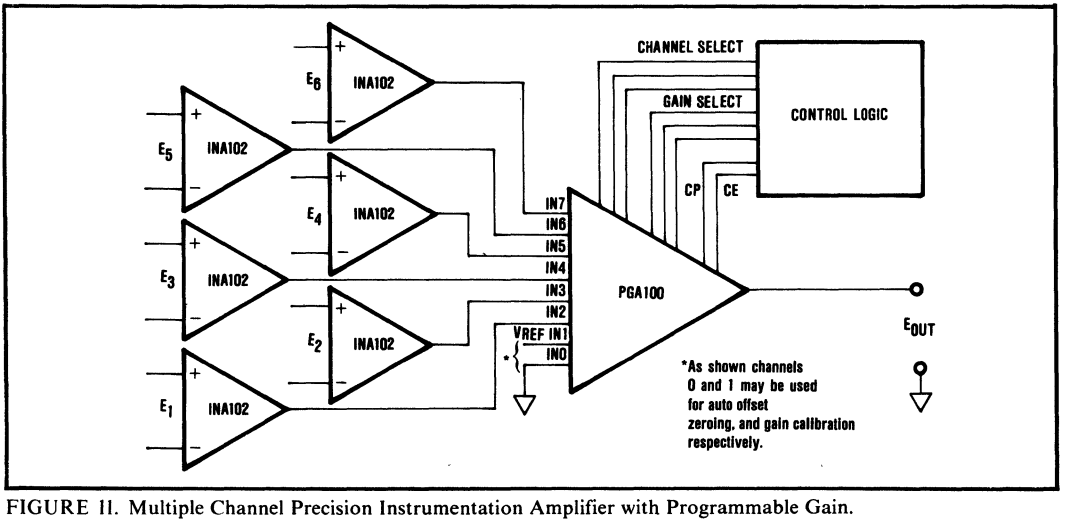


FIGURE 11. Multiple Channel Precision Instrumentation Amplifier with Programmable Gain.

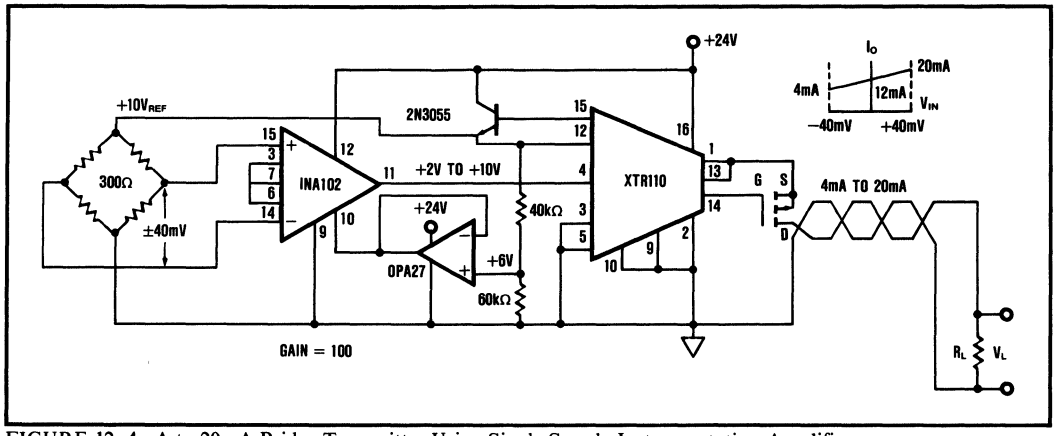


FIGURE 12. 4mA to 20mA Bridge Transmitter Using Single Supply Instrumentation Amplifier.

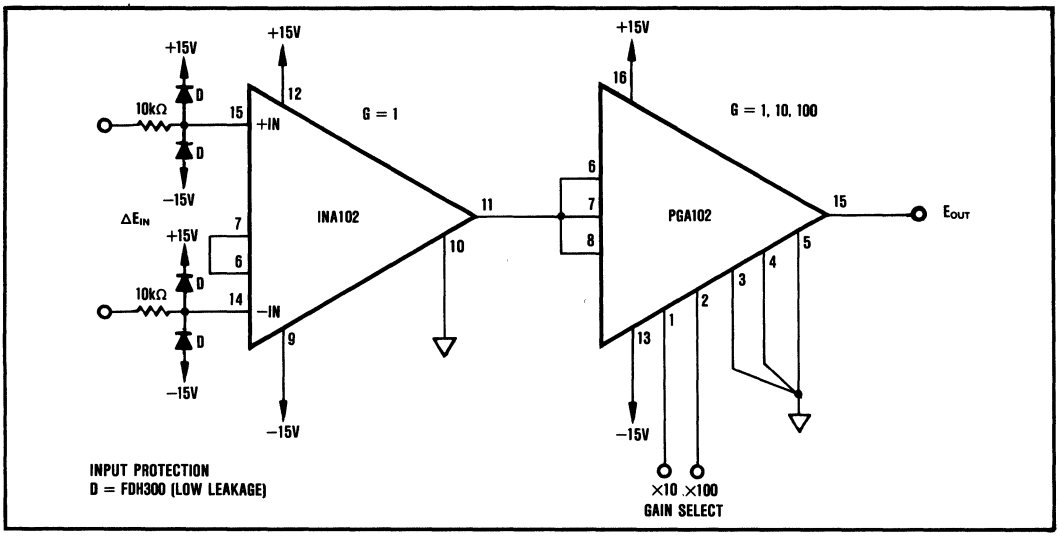


FIGURE 13. Programmable-Gain Instrumentation Amplifier Using the INA102 and PGA102.

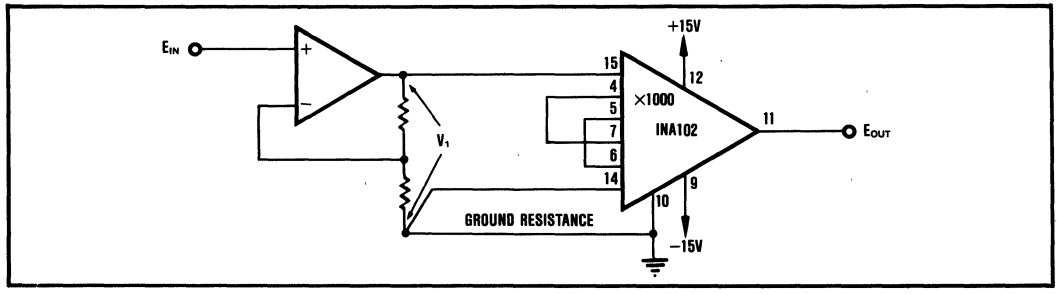


FIGURE 14. Ground Resistance Loop Eliminator (INA102 senses and amplifies V_1 accurately).

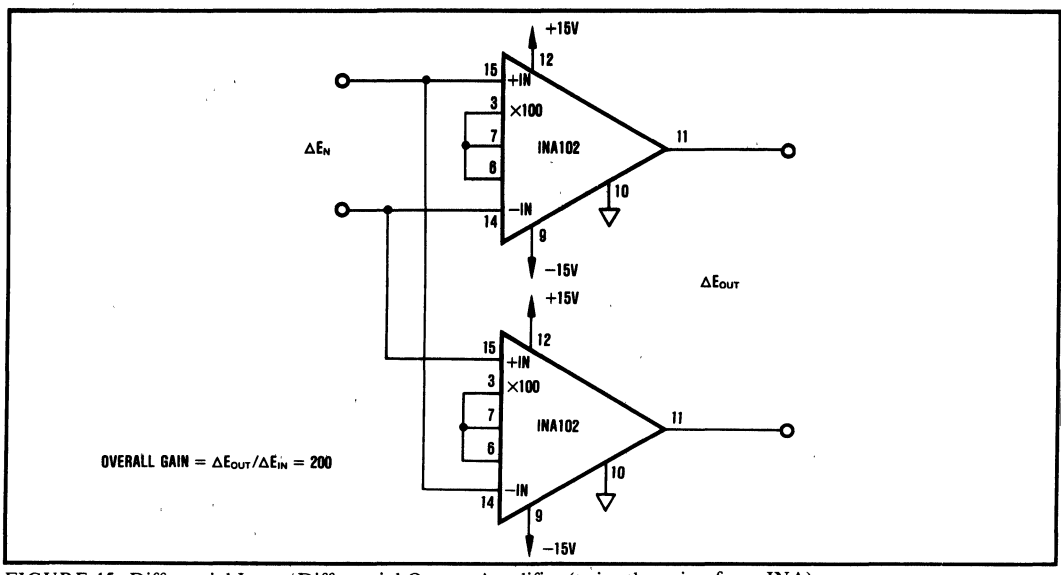
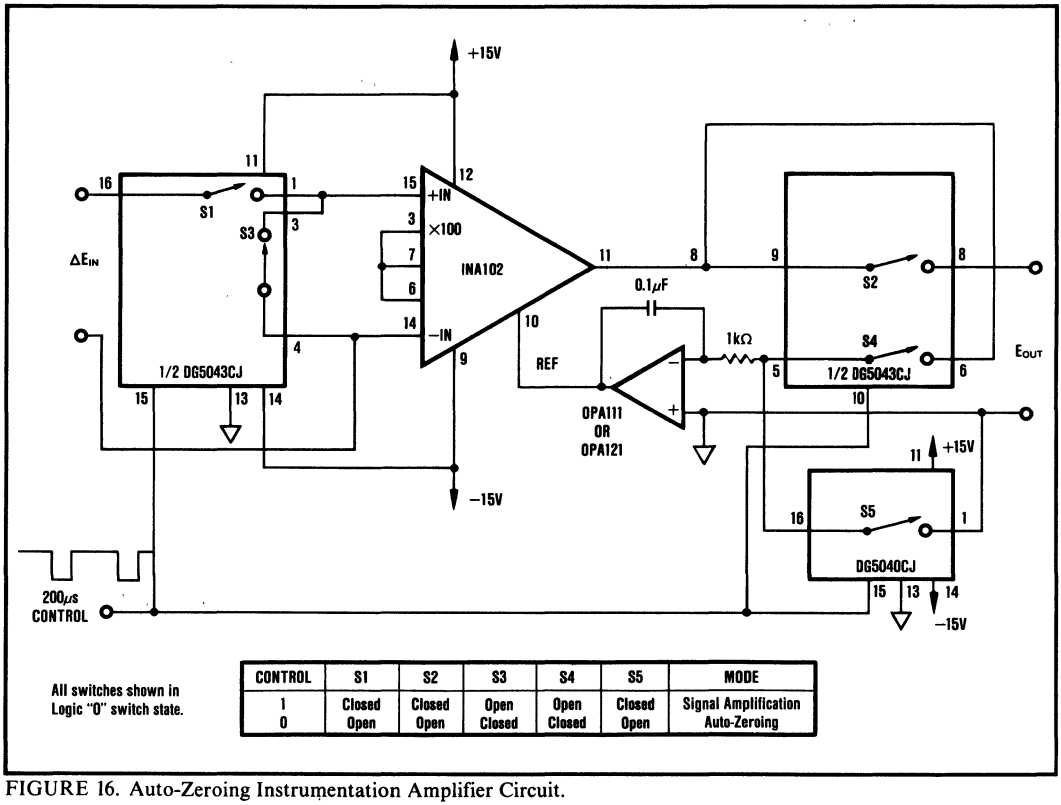


FIGURE 15. Differential Input/Differential Output Amplifier (twice the gain of one INA).

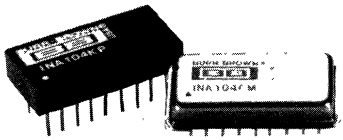


CONTROL	S1	S2	S3	S4	S5	MODE
1	Closed	Closed	Open	Open	Closed	Signal Amplification
0	Open	Open	Closed	Closed	Open	Auto-Zeroing

FIGURE 16. Auto-Zeroing Instrumentation Amplifier Circuit.

BURR-BROWN®

INA104



Very-High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- VERSATILE FOUR-OP AMP DESIGN
- ULTRA-LOW VOLTAGE DRIFT - 0.25μV/°C, max
- LOW OFFSET VOLTAGE - 25μV, max
- LOW NONLINEARITY - 0.002%, max
- LOW NOISE - 13nV/$\sqrt{Hz}$ at f_0 = 1kHz
- HIGH CMR - 106dB at 60Hz, min
- HIGH INPUT IMPEDANCE - $10^{10}\Omega$
- LOW COST

APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gages
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCER AMPLIFIER
- LOW LEVEL SIGNAL CONDITIONER
- MEDICAL INSTRUMENTATION

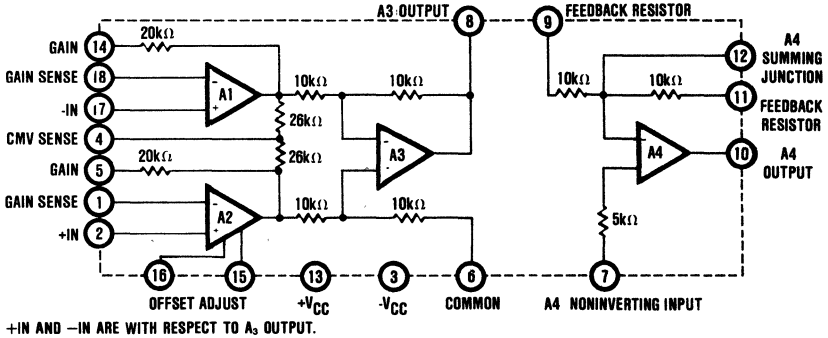
DESCRIPTION

The INA104 is a high accuracy, multistage, integrated-circuit instrumentation amplifier designed for signal conditioning requirements where very-high performance is desired.

A multiamplifier, monolithic design, which uses Burr-Brown's ultra-low drift, low noise technology, provides the highest performance with maximum versatility at the lowest cost and this makes the INA104 ideal for even high volume applications.

Burr-Brown's compatible thin-film resistors and state-of-the-art wafer level laser-trimming techniques are used for minimizing offset voltage and temperature drift. This advanced technique also maximized common-mode rejection and gain accuracy.

The INA104 also contains a fourth operational amplifier, specified separately, which can conveniently be used for some important applications such as single capacitor active low-pass filtering, easy output level shifting, Common-mode voltage active guard drive, and increased gain (x 10,000 and greater).



NOTE: +IN AND −IN ARE WITH RESPECT TO A_3 OUTPUT.
IF A_4 IS USED INVERTING, +IN AND −IN ARE REVERSED.

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PDS-488C

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C with ±15VDC power supply and in circuit of Figure 1 unless otherwise noted

MODEL	INA104AM/HP MIN	INA104AM/HP TYP	INA104AM/HP MAX	INA104BM/SM/JP MIN	INA104BM/SM/JP TYP	INA104BM/SM/JP MAX	INA104CM/KP MIN	INA104CM/KP TYP	INA104CM/KP MAX	UNITS
INSTRUMENTATION AMPLIFIER										
GAIN										
Range of Gain	1		1000	*		*	*		*	V/V
Gain Equation		G = 1 + (40k/R_G)			*			*		V/V
Error From Equation, DC(1)		±(0 08 − 0 05/G)	±(0 15 − 0 1/G)		*	*		*	*	% of FS
Gain Temp Coefficient(2)										
G = 1		2	5		*	*		*	*	ppm/°C
G = 10		20	100		*	*		−10	−50	ppm/°C
G = 100		22	110		*	*		−11	−55	ppm/°C
G = 1000		22	110		*	*		−11	−55	ppm/°C
Nonlinearity, DC		±(0 002 + 10^{-5}G)	±(0 005 + 2 × 10^{-5}G)		±(0 001 + 10^{-5}G)	±(0 002 + 10^{-5}G)		±(0 001 + 10^{-5}G)	±(0 002 + 10^{-5}G)	% of p-p FS
RATED OUTPUT										
Voltage	±10	+11 5, −12 5		*	*		*	*		V
Current	±5	+11 5, −12 5		*	*		*	*		mA
Output Impedance		0 2			*			*		Ω
INPUT OFFSET VOLTAGE										
Initial Offset at +25°C(3)		±25 ±200/G	±50 ±400/G		±10 ±100/G	±25 ±200/G		±10 ±100/G	±25 ±200/G	µV
vs Temperature			±2 ±20/G			±0 75 ±10/G			±0 25 ±10/G	µV/°C
vs Supply		±(1 + 50/G)			*			*		µV/V
vs Time		±(1 + 20/G)			*			*		µV/mo
INPUT BIAS CURRENT										
Initial Bias Current (each input		±15	±30		±10	*		±5	±20	nA
vs Temperature		±0.2			*			*		nA/°C
vs Supply		±0.1			*			*		nA/V
Initial Offset Current		±5	±30		±2	*		±2	±20	nA
vs Temperature		±0 5			*			*		nA/°C
INPUT IMPEDANCE										
Differential		10^{10} || 3			*			*		Ω || pF
Common-mode		10^{10} || 3			*			*		Ω || pF
INPUT VOLTAGE RANGE										
Range, Linear Response	±10			*			*			V
CMR with 1kΩ Source Imbal										
DC to 60Hz, G = 1	80	90		*	*		*	*		dB
DC to 60Hz, G = 10	96	106		*	*		*	*		dB
DC to 60Hz, G = 100 to 1000	106	110		*	*		*	*		dB
INPUT NOISE										
Input Voltage Noise										
f_B = 0 1Hz to 10Hz		0 8			*			*		µV, p-p
Density, G = 1000										
f_O = 10Hz		18			*			*		nV/√Hz
f_O = 100Hz		15			*			*		nV/√Hz
f_O = 1kHz		13			*			*		nV/√Hz
Input Current Noise										
f_B = 0 01Hz to 10Hz		50			*			*		pA, p-p
Density										
f_O = 10Hz		0 8			*			*		pA/√Hz
f_O = 100Hz		0 46			*			*		pA/√Hz
f_O = 1kHz		0 35			*			*		pA/√Hz
DYNAMIC RESPONSE										
Small Signal, ±3dB Flatness										
G = 1		300			*			*		kHz
G = 10		140			*			*		kHz
G = 100		25			*			*		kHz
G = 1000		2 5			*			*		kHz
Small Signal, ±1% Flatness										
G = 1		20			*			*		kHz
G = 10		10			*			*		kHz
G = 100		1			*			*		kHz
G = 1000		200			*			*		Hz
Full Power, G = 1 - 100		6.4			*			*		kHz
Slew Rate, G = 1 - 100	0 2	0 4		*	*		*	*		V/µsec
Settling Time (0.1%)										
G = 1		30	40		*	*		*	*	µsec
G = 100		40	55		*	*		*	*	µsec
G = 1000		350	470		*	*		*	*	µsec
Settling Time (0.01%)										
G = 1		30	45		*	*		*	*	µsec
G = 100		50	70		*	*		*	*	µsec
G = 1000		500	650		*	*		*	*	µsec

ELECTRICAL (CONT)

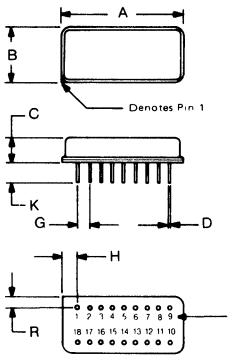
MODEL	INA104AM/HP			INA104BM/SM/JP			INA104CM/KP			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT AMPLIFIER, A_4										
OPEN-LOOP GAIN, $V_O = \pm 100$										
Rated Load $R_L \geq 2k\Omega$	100	115		•	•		•	•		dB
$R_L \geq 10k\Omega$	110	125		•	•		•	•		dB
RATED OUTPUT										
Voltage at $R_L = 2k\Omega$	10	+13, −14 5		•	•		•	•		V
$R_L = 10k\Omega$		+13, −14 5			•			•		V
Current	5	7 5		•	•		•	•		mA
Output Impedance		2			•			•		kΩ
Load Capacitance unity-gain inverting		2000			•			•		pF
Short Circuit Current		10			•			•		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			•			•		MHz
Full Power		9			•			•		kHz
Slew Rate	0 35	0 55		•	•		•	•		V/μsec
Settling Time (unity gain)										
0 1%		37			•			•		μsec
0 01%		40			•			•		μsec
INPUT OFFSET VOLTAGE										
Initial, $T_A = +25°C$		±1	±2		•	•		•	•	mV
vs Temperature		±5			•			•		μV/°C
INPUT BIAS CURRENT		+55	+150		*	*		*	*	nA
INPUT IMPEDANCE										
Differential		500			•			•		kΩ
Common-Mode		100			•			•		MΩ
RESISTORS, 10kΩ										
Accuracy		0 5	5		•			•		%
Drift		30	50		•	•		•	•	ppm/°C
Ratio Match		0 06	0 12		•	•		•	•	%
Drift		5			•			•		ppm/°C
INPUT VOLTAGE NOISE										
F_B = 0 1Hz to 10Hz		1 5			•			•		μV,p-p
Density										
f_O = 10Hz		35			•			•		$nV\sqrt{Hz}$
f_O = 100Hz		33			•			•		$nV\sqrt{Hz}$
f_O = 1kHz		32			•			•		$nV\sqrt{Hz}$
POWER SUPPLY, TOTAL										
Rated Voltage		±15			•			•		V
Voltage Range	±5		±20	•		•	•		•	V
Current, Quiescent		±8.1	±9 6		•	•		•	•	mA
TEMPERATURE RANGE										
Specification										
INA104HP/JP/KP	0		+70							°C
INA104AM/BM/CM	−25		+85							°C
INA104SM	−55		+125							°C
Operation										
INA104HP/JP/KP	−40		+85							°C
INA104AM/BM/CM/SM	−55		+125							°C
Storage										
INA104HP/JP/KP	−40		+85							°C
INA104AM/BM/CM/SM	−65		+150							°C
θ_{J-C}		115			•			•		0°C/W
θ_{J-A}		350			•			•		0°C/W

*Specifications same as for INA104HP

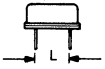
NOTES.
1 Typically the tolerance of R_G will be the major source of gain error 2 Not including the TCR of R_G 3 Adjustable to zero at any one gain

MECHANICAL

METAL HERMETIC DIP



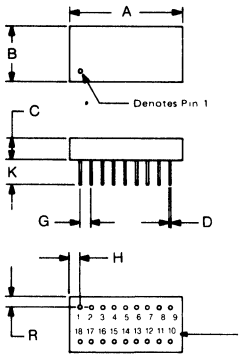
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 060	1 080	26 92	27 43
B	490	510	12 45	12 95
C	170	250	4 32	6 35
D	016	021	0 41	0 53
G	100 BASIC		2 54 BASIC	
H	115	155	2 92	3 94
K	150	300	3 81	7 62
L	300 BASIC		7 62 BASIC	
R	080	120	2 03	3 05



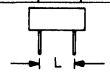
NOTE Leads in true position within 0 01" (25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers are not marked on package

PLASTIC DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	990	1 010	25 15	25 65
B	490	510	12 45	12 95
C	190	210	4 83	5 33
D	018	021	0 46	0 53
G	100 BASIC		2 54 BASIC	
H	080	115	2 03	2 92
K	130	300	3 30	7 62
L	300 BASIC		7 62 BASIC	
R	080	115	2 03	2 92



NOTE Leads in true position within 0 01" (25mm) R at MMC at seating plane

Pin numbers shown fo eference only Numbers are not marked on package

ABSOLUTE MAXIMUM RATINGS

Supply	±20V
Internal Power Dissipation	980mW
Input Voltage Range	±V_{CC}
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−40°C to +85°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-Circuit Duration	Continuous to ground

ORDERING INFORMATION

INA104 X X

Basic Model Number

Performance Grade Code
- H, J, K 0°C to +70°C
- A, B, C −25°C to +85°C
- S −55°C to +125°C

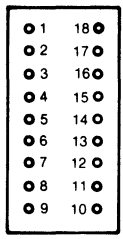
Package Code
- P - Plastic DIP
- M - Metal Hermetic DIP

Plastic DIP (Hybripak)	Metal DIP
INA104HP	INA104AM
INA104JP	INA104BM
INA104KP	INA104CM
	INA104SM

PIN DESIGNATIONS

1 GAIN SENSE
2 +IN
3 NEGATIVE SUPPLY
4 COMMON-MODE VOLTAGE SENSE
5 GAIN
6 COMMON
7 NONINVERTING INPUT TO A_4
8 OUTPUT
9 FEEDBACK RESISTOR
10 OUTPUT OF A_4
11 FEEDBACK RESISTOR
12 SUMMING JUNCTION OF A_4
13 POSITIVE SUPPLY
14 GAIN
15 OFFSET ADJUST
16 OFFSET ADJUST
17 -IN
18 GAIN SENSE

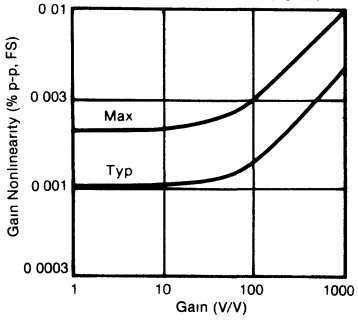
(TOP VIEW)



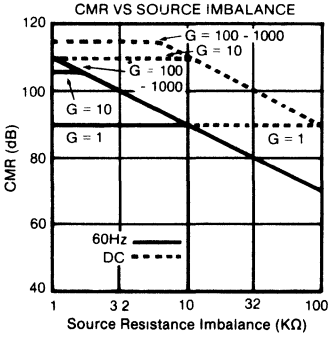
TYPICAL PERFORMANCE CURVES

At +25°C, ±V_{CC} = 15VDC, and in circuit of Figure 1 unless otherwise specified

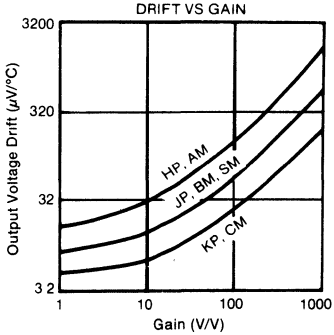
GAIN NONLINEARITY VS GAIN

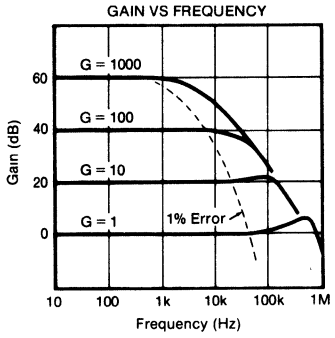


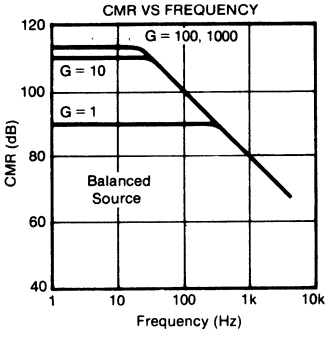
CMR VS SOURCE IMBALANCE

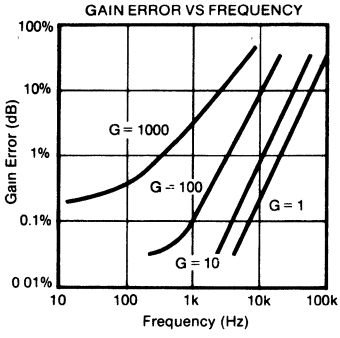


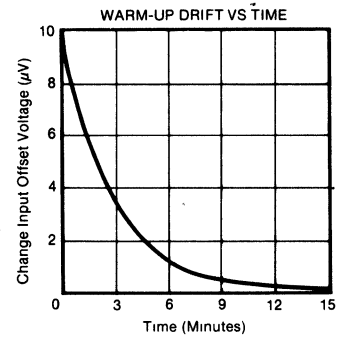
TOTAL OFFSET VOLTAGE DRIFT VS GAIN

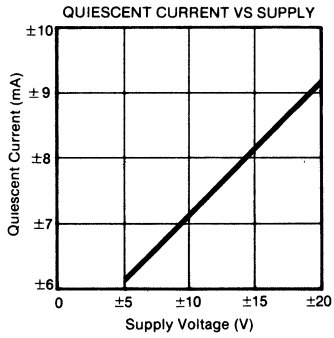


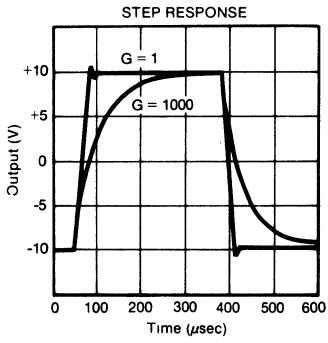


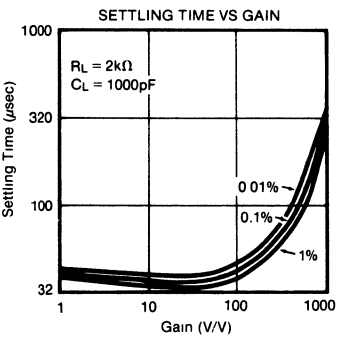


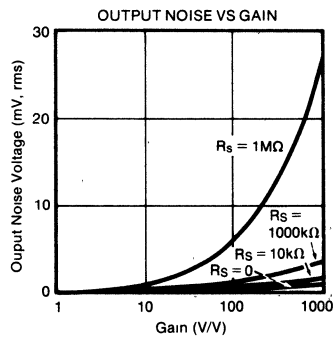


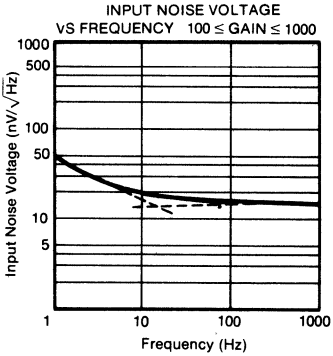












DISCUSSION OF PERFORMANCE

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are closed-loop gain blocks whose committed circuitry accurately amplifies the voltage applied to their inputs. They respond only to the difference between the two input signals and exhibit extremely-high input impedance, both differentially and common-mode. Feedback networks are packaged within the amplifier module. Only one external gain setting resistor must be added. An operational amplifier, on the other hand, is an open-loop, uncommitted device that requires external networks to close the loop. While operational amplifiers can be used to achieve the same basic function as instrumentation amplifiers, it is difficult to reach the same level of performance. Using operational amplifiers often leads to design trade-offs when it is necessary to amplify low level signals in the presence of common-mode voltages while maintaining high input impedances.

THE INA104

A simplified schematic of the INA104 is shown on the first page of this data sheet. It is a three-amplifier device which provides all the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found on integrated circuit instrumentation amplifiers.

The input section (A1 and A2) incorporates high performance, low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide

the high input impedance ($10^{10}\Omega$) desirable in the instrumentation amplifier function. The offset voltage and offset voltage versus temperature is low due to the monolithic design and improved even further by the state-of-the-art laser-trimming techniques.

The output section (A3) is connected in a unity-gain difference amplifier configuration. A critical part of this stage is the matching of the four 10kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain excellent common-mode rejection. (The 106dB minimum at 60Hz for gains greater than 100V/V is a significant improvement compared to most other integrated circuit instrumentation amplifiers.)

All of the internal resistors are compatible thin-film nichrome formed with the integrated circuit. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. Nichrome ensures long-term stability of trimmed resistors and simultaneous achievement of excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA104 is operated over wide temperature ranges.

The fourth op-amp (A4) of the INA104 adds a great deal of versatility and convenience to the amplifier. Its use allows easy implementation of active low-pass filtering, output offsetting, and additional gain generation. The pin connections make the use of this stage optional and the specifications appear separately in the table of Electrical Specifications.

USING THE INA104

Figure 1 shows the simplest configuration of the INA104. The gain is set by the external resistor, R_G, with a gain equation of $G = 1 + (40K/R_G)$. The reference and TCR of R_G contribute directly to the gain accuracy and drift.

For gains greater than unity, resistor R_G is connected externally between pins 5 and 14. At high gains where the value of R_G becomes small, additional resistance (i.e., relays, sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect. However, this error can be virtually eliminated with the INA104 by using the gain sense circuit connection.

Pins 1, 5, 14, and 18 are accessible so that a four-terminal connection can be made to R_G. (Pins 1 and 18 are the voltage sense terminals since no signal current flows into the operational amplifiers' inputs.) This may be useful at high gains where the value of R_G becomes small.

The optional offset adjust capability is shown in Figure 1. The adjustment affects only the input stage component of the offset voltage. Thus, the null condition will be disturbed (if input offset is not adjusted to zero) when the gain is changed. Also, the input drift will be affected by approximately 0.31μV/°C per 100μV of input offset voltage that is trimmed. Therefore, care should be taken when considering use of the control for removal of other sources of offset.

OPTIONAL OFFSET ADJUSTMENT PROCEDURE

It is frequently desirable to null the input component of offset (Figure 1) and occasionally that of the output

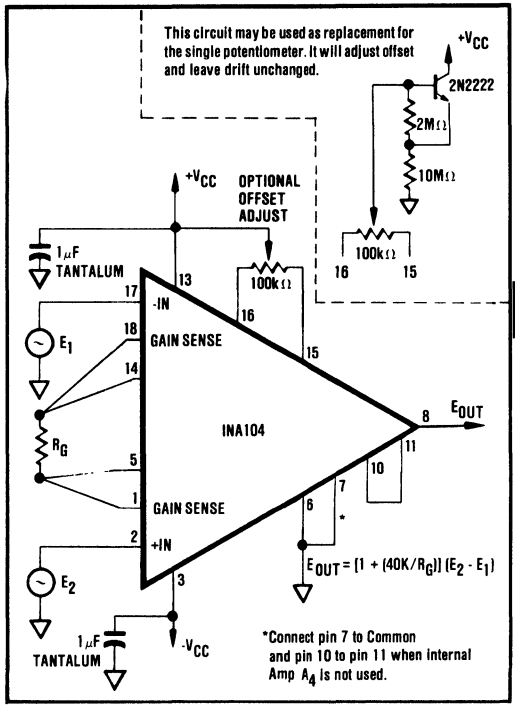


FIGURE 1. Basic Circuit Connection for the INA104 Including Optional Input Offset Null Potentiometer.

(Figure 2). The quality of the potentiometer will affect the results, therefore, choose one with good temperature and mechanical-resistance stability. The procedure is as follows:

1. Set $E_1 = E_2 = 0V$ (be sure a good ground return path exists to the input).
2. Set the gain to the desired value (greater than 1) by choosing R_G.
3. Adjust the 100kΩ potentiometer in Figure 1 until the output reads 0V ±1mV or desired setting. Note that the offset will change when the gain is changed. If the output component of offset is to be removed or if it is desired to establish an intentional offset, adjust the 100kΩ potentiometer in Figure 2 until the output reads 0V ±1mV or desired setting. Note that the offset will not change with gain, but be sure to use a stable amplifier with good DC characteristics. The range of adjustment is ±15mV as shown. For larger ranges change the ratio of R_1 to R_2. The op amp is used to maintain a low resistance (<0.1Ω) from pin 6 to Common to avoid CMR degradation.

BASIC CIRCUIT CONNECTION

The basic circuit connection for the INA104 is shown in Figure 1. The output voltage is a function of the differential input voltage times the gain.

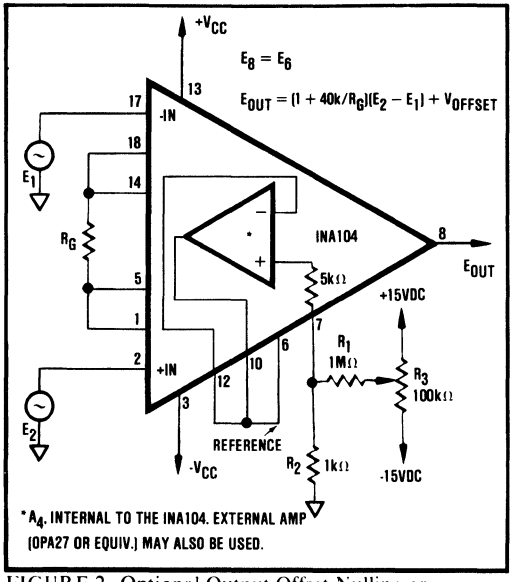


FIGURE 2. Optional Output Offset Nulling or Offsetting Using an Amplifier(Low Impedance to Pin 6).

Figure 1 does not include additional internal op amp A_4. Power supply bypassing with a 1μF tantalum capacitor or equivalent is always recommended.

In applications which do not use the fourth internal amplifier (A_4 - pins 7, 9, 10, 11, and 12), pin 7 should be connected to Common and pins 10 and 11 should be connected together. This will prevent the output of A_4 from saturating ("locking-up") and affecting the offset of the instrumentation amplifier, A_1, A_2, and A_3.

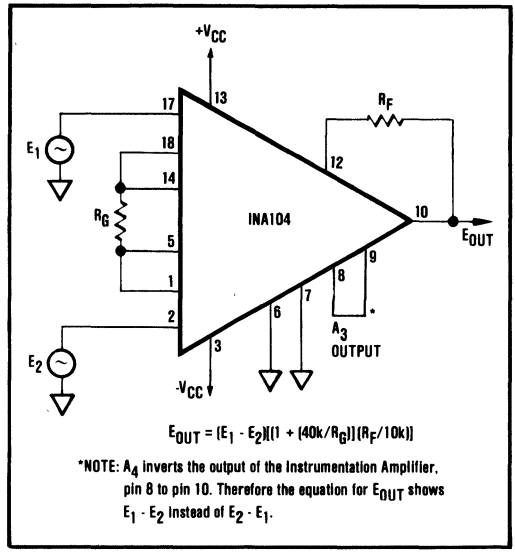


FIGURE 3. Additional Gain From Output Stage.

with most other IC instrumentation amplifiers as shown in Figure 4. The use of the extra internal op amp, A_4, means that CMR of the instrument amp is not disturbed, and that a convenient value of variable resistor can be used. The circuit shown in Figure 2 can also be used to achieve the desired offsetting by scaling the resistors R_1 and R_2. A low impedance path from pin 6 to Common should be provided to achieve the high CMR specified. Resistance above 0.1Ω will cause the CMR to fall below 106dB.

TYPICAL APPLICATIONS

Many applications of instrumentation amplifiers involve the amplification of low-level differential signals from bridges and transducers such as strain gages, thermocouples, and RTD's. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA104 accomplishes all of these with high precision.

Figures 3 through 13 show some typical applications circuits.

Figure 3 shows how the output stage may be used to provide additional gain. If gains greater than 1000V V (10,000 up to 100,000 and greater) are desired it is better to place some gain in the output amplifier rather than the input stage due to the low values of R_G required ($R_G <$ 40Ω for (1 + 40k R_G) > 1000). Note, however, that accuracy can degrade due to very-high amplification of offset, drift, and noise errors.

Output offsetting ("zero suppression" or "zero elevation") may be more easily accomplished with the INA104 than

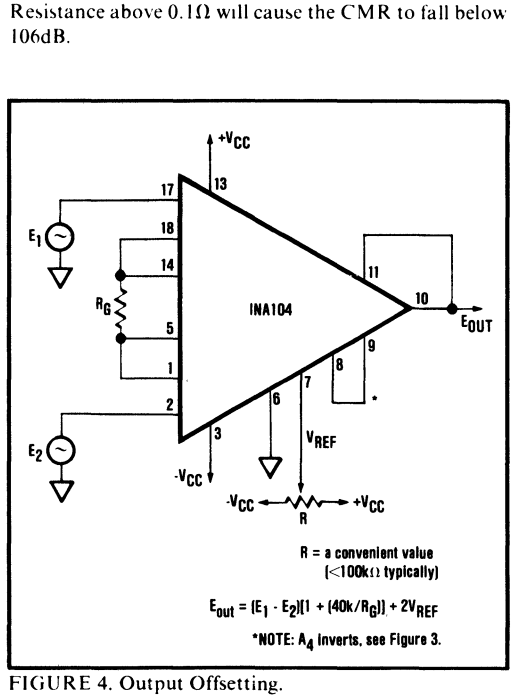


FIGURE 4. Output Offsetting.

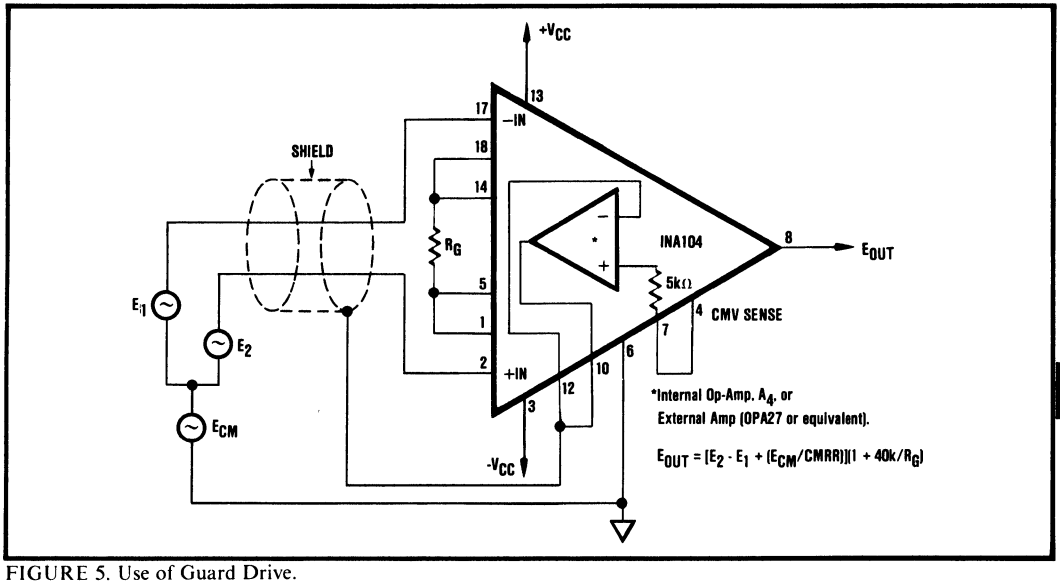


FIGURE 5. Use of Guard Drive.

Amplifier A_4 also allows active low-pass filtering to be implemented conveniently with a single capacitor. Filtering can be used for noise reduction or band-limiting of the output signal as shown in Figure 6.

The common-mode voltage from the 26kΩ resistors in the input section appears at pin 4. Figure 5 shows how this voltage can be used to drive the shield of the input cable. Since the cable is driven at the common-mode voltage, the effects of distributed capacitance is reduced and the AC system common-mode rejection may be improved. Amplifier A_4 buffers the CMV at pin 4 from the input cable.

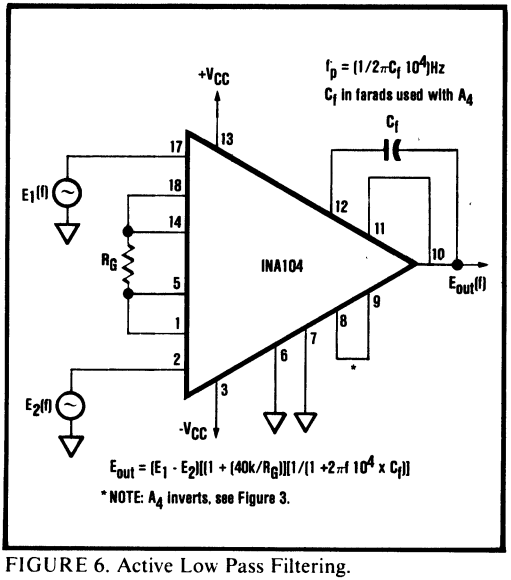


FIGURE 6. Active Low Pass Filtering.

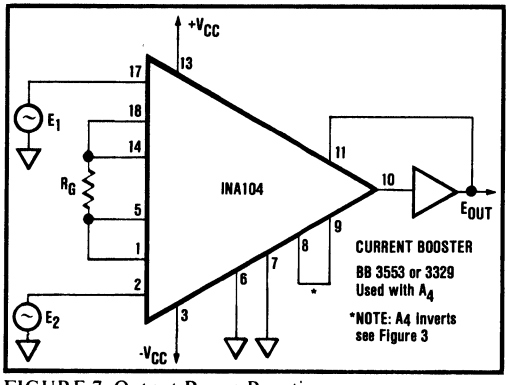


FIGURE 7. Output Power Boosting.

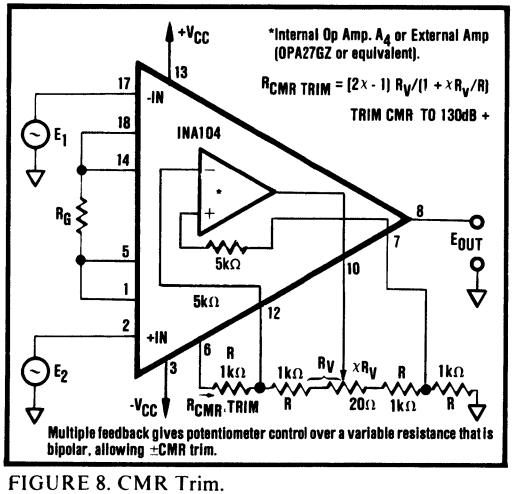


FIGURE 8. CMR Trim.

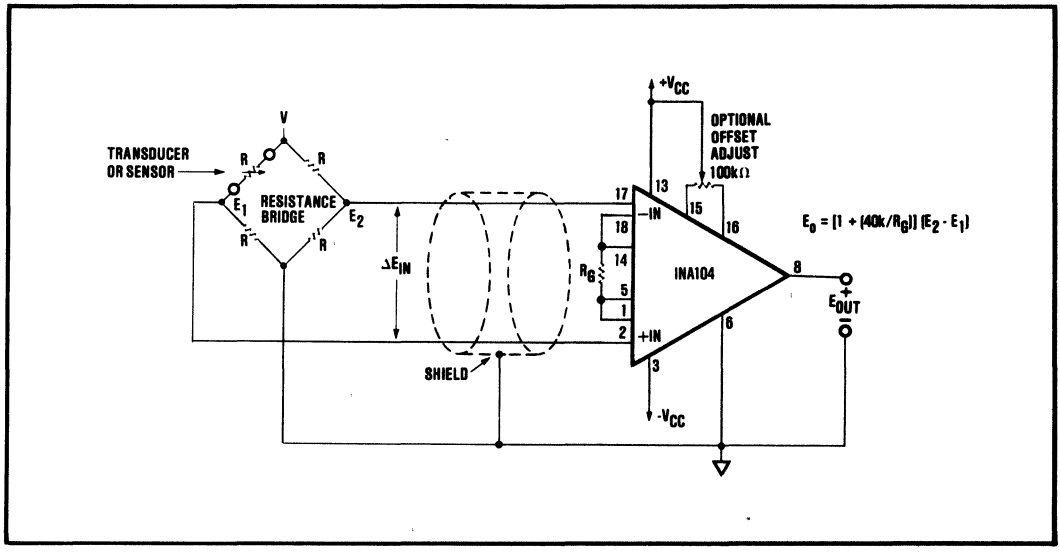


FIGURE 9. Amplification of a Differential Voltage from a Resistance Bridge.

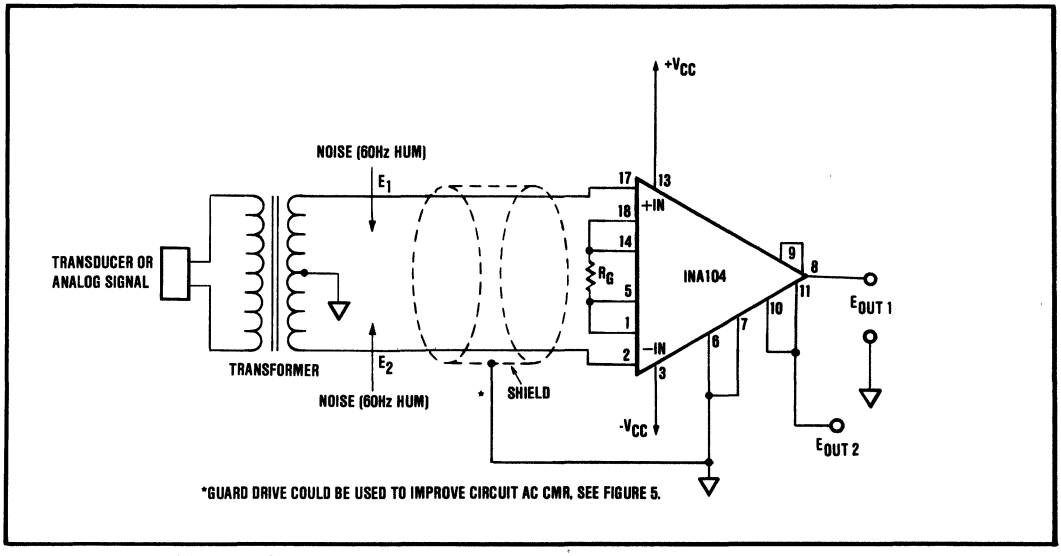


FIGURE 10. Amplification of a Transformer Coupled Analog Signal.

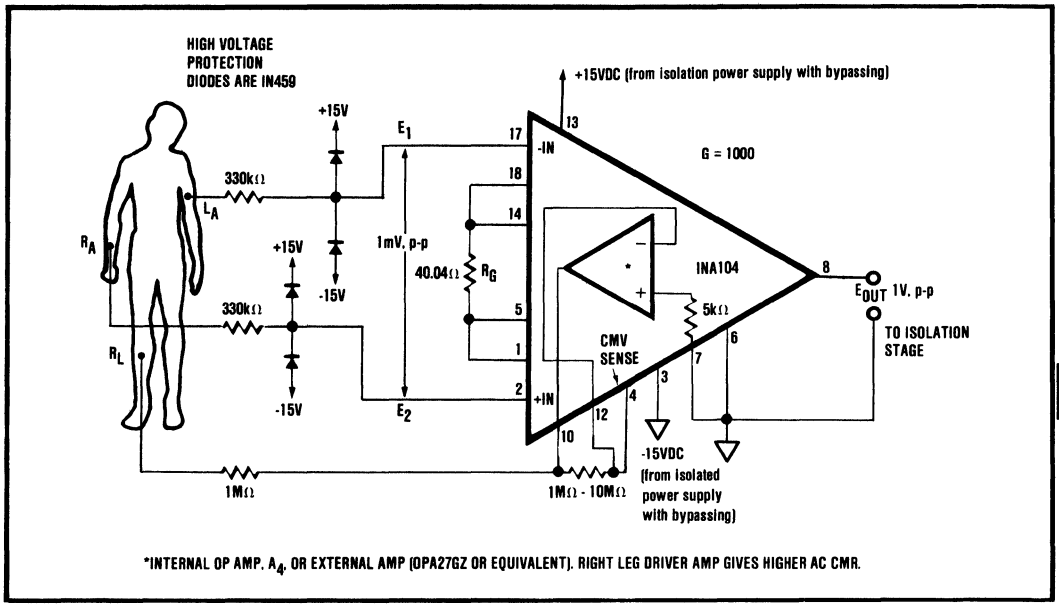


FIGURE 11. ECG Amplifier or Recorder Preamp for Biological Signals.

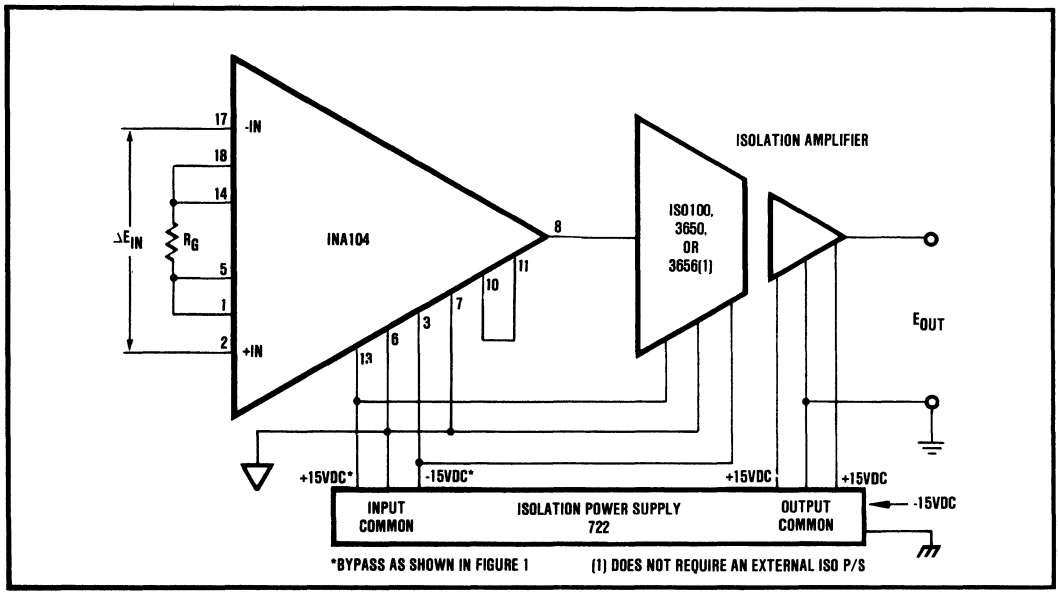


FIGURE 12. Precision Isolated Instrumentation Amplifier.

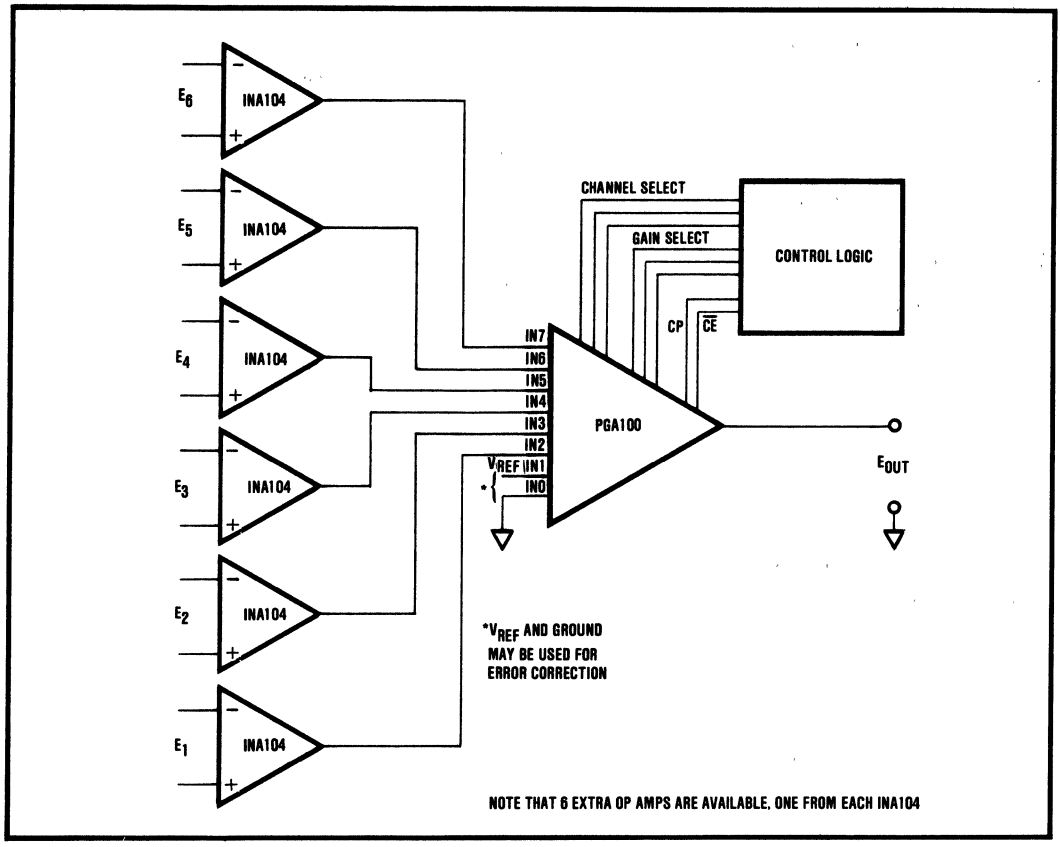


FIGURE 13. Multiple Channel Precision Instrumentation Amplifier.

GENERAL RECOMMENDED HANDLING PROCEDURES FOR INTEGRATED CIRCUITS

All semiconductor devices are vulnerable, in varying degrees, to damage from the discharge of electrostatic energy. Such damaging can cause performance degradation or failure, either immediate or latent. As a general practice we recommend the following handling procedures to reduce the risk of electrostatic damage.

1. Remove static-generating materials, such as untested plastics, from all areas that handle microcircuits.
2. Ground all operators, equipment, and work stations.
3. Transport and ship microcircuits, or products incorporating microcircuits, in static-free, shielded containers.
4. Connect together all leads of each device by means of a conductive material, when the device is not connected into a circuit.
5. Control relative humidity to as high a value as practical (50% is recommended).

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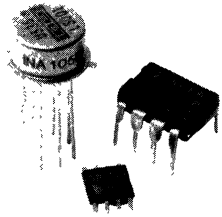


INA105

AVAILABLE IN DIE FORM

Precision Unity Gain DIFFERENTIAL AMPLIFIER

FEATURES

- CMR 86dB min over temp
- GAIN ERROR 0.01% max
- NONLINEARITY 0.001% max
- NO EXTERNAL ADJUSTMENTS REQUIRED
- EASY TO USE
- COMPLETE SOLUTION
- HIGHLY VERSATILE
- LOW COST
- TO-99 HERMETIC METAL, LOW COST PLASTIC DIP, AND SMALL OUTLINE PACKAGES

APPLICATIONS

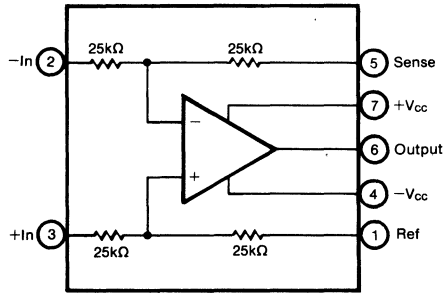
- DIFFERENTIAL AMPLIFIER
- BASIC INSTRUMENTATION AMPLIFIER BUILDING BLOCK
- UNITY-GAIN INVERTING AMPLIFIER
- GAIN-OF-1/2 AMPLIFIER
- NONINVERTING GAIN-OF-2 AMPLIFIER
- AVERAGE VALUE AMPLIFIER
- ABSOLUTE VALUE AMPLIFIER
- SUMMING AMPLIFIER
- SYNCHRONOUS DEMODULATOR
- CURRENT RECEIVER WITH COMPLIANCE TO RAILS
- 4mA to 20mA TRANSMITTER
- VOLTAGE-CONTROLLED CURRENT SOURCE
- ALL-PASS FILTERS

DESCRIPTION

The INA105 is a precision unity-gain differential amplifier. As a monolithic circuit, it offers high reliability at low cost. It consists of a premium grade operational amplifier and an on-chip precision resistor network.

As a special feature, the INA105 can drive 20mA from the positive supply. This simplifies construction of 4mA to 20mA current sources and transmitters.

The INA105 is completely self-contained and offers the user a highly versatile function. No adjustments to gain, offset, and CMR are necessary. This provides three important advantages: (1) lower initial design engineering time, (2) lower manufacturing assembly time and cost, and (3) easy cost-effective field repair of a precision circuit.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-617D

SPECIFICATIONS

ELECTRICAL

At +25°C, V_{CC} = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	INA105AM			INA105BM			INA105KP/KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Initial[1]			1			*			*		V/V
Error			0 005	0.01		*	*		0 01	0 025	%
vs Temperature			1	5		*	*		*		ppm/°C
Nonlinearity[2]			0 0002	0.001		*	*		*	*	%
OUTPUT											
Rated Voltage	I_O = +20mA, −5mA	10	12		*	*		*	*		V
Rated Current	E_O = 10V	+20, −5			*			*			mA
Impedance			0.01			*			*		Ω
Current Limit	To common		+40/−10			*			*		mA
Capacitive Load	Stable operation		1000			*			*		pF
INPUT											
Impedance[3]	Differential		50			*			*		kΩ
	Common-mode		50			*			*		kΩ
Voltage Range[4]	Differential	±10			*			*			V
	Common-mode	±20			*			*			V
Common-mode Rejection[5]	$T_A = T_{MIN}$ to T_{MAX}	80	90		86	100		72	*		dB
OFFSET VOLTAGE	RTO[6][7]										
Initial			50	250		*	*		*	500	µV
vs Temperature			5	20		5	10		*		µV/°C
vs Supply	$\pm V_{CC}$ = 6V to 18V		1	25		*	15		*	*	µV/V
vs Time			20			*			*		µV/mo
OUTPUT NOISE VOLTAGE	RTO[6][8]										
F_B = 0 01Hz to 10Hz			2 4			*			*		µV p-p
F_O = 10kHz			60			*			*		nV/√Hz
DYNAMIC RESPONSE											
Small Signal	−3dB		1			*			*		MHz
Full Power BW	V_O = 20V p-p	30	50		*	*		*	*		kHz
Slew Rate		2	3		*	*		*	*		V/µs
Settling Time. 0.1%	V_O = 10V step		4			*			*		µs
0.01%	V_O = 10V step		5			*			*		µs
0.01%	V_{CM} = 10V step, V_{DIFF} = 0V		1 5			*			*		µs
POWER SUPPLY											
Rated			±15			*			*		V
Voltage Range	Derated performance	±5		±18	*		*	*		*	V
Quiescent Current	V_{OUT} = 0V		±1.5	±2		*	*		*	*	mA
TEMPERATURE RANGE											
Specification		−25		+85	*		*	0		+70	°C
Operation		−55		+125	*		*	−25		+85	°C
Storage		−65		+150	*		*	−40		+85	°C

* Specification same as for INA105AM

NOTES. (1) Connected as difference amplifier (see Figure 4). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output (3) 25kΩ resistors are ratio matched but have ±20% absolute value. (4) Maximum input voltage without protection is 10V more than either ±15V supply (±25V) Limit I_{IN} to 1mA (5) With zero source impedance (see Maintaining CMR section). (6) Referred to output in unity-gain difference configuration. Note that this circuit has a gain of 2 for the operational amplifier's offset voltage and noise voltage. (7) Includes effects of amplifier's input bias and offset currents (8) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

ABSOLUTE MAXIMUM RATINGS

Supply ..... ±18V
Input Voltage Range..... $\pm V_{CC}$
Operating Temperature Range: M ..... −55°C to +125°C
P, U..... −40°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (soldering 10 seconds) M, P..... +300°C
Wave Soldering (3 seconds, max) U ..... +260°C
Output Short Circuit to Common ..... Continuous

ORDERING INFORMATION

Model	Package	Temperature Range
INA105AM	Metal TO-99	-25°C to +85°C
INA105BM	Metal TO-99	-25°C to +85°C
INA105KP	Plastic DIP	0°C to +70°C
INA105KU	Plastic SOIC	0°C to +70°C

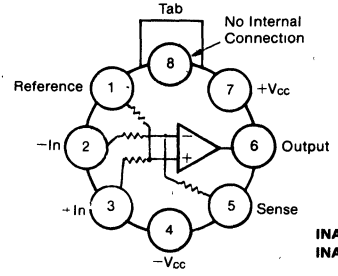
BURN-IN SCREENING OPTION
See text for details.

Model	Package	Burn-In Temp. (160h)[1]
INA105AM-BI	Metal TO-99	+125°C
INA105BM-BI	Metal TO-99	+125°C
INA105KP-BI	Plastic DIP	+85°C
INA105KU-BI	Plastic SOIC	+85°C

NOTE: (1) Or equivalent combination. See text

PIN DESIGNATIONS

TOP VIEW
TO-99

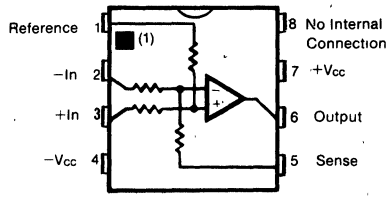


INA105AM
INA105BM

Case connected to $-V_{CC}$ internally Make no connection

TOP VIEW
PLASTIC DIP AND SMALL OUTLINE

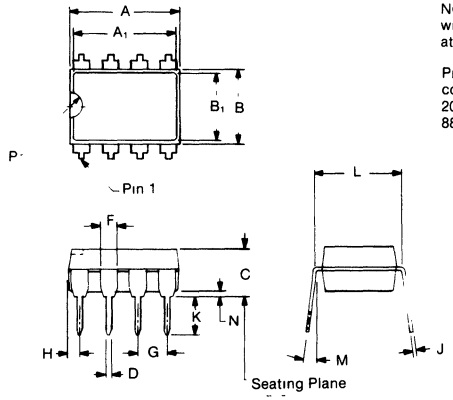
INA105



NOTE: (1) Peformance grade identifier box for small outline surface mount Blank indicates K grade Part is marked INA105U

MECHANICAL

"P" Package—Plastic DIP

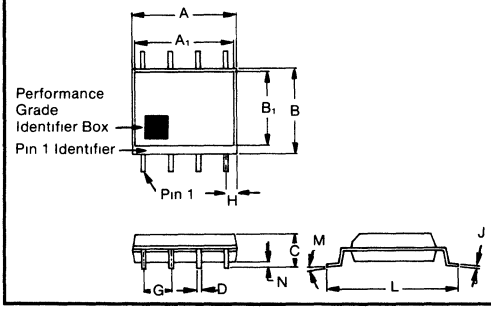


NOTE Leads in true position within 0 01" (0 25mm) R at MMC at seating plane

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3 2)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	355	400	9 03	10 16
A_1	340	385	8 65	9 80
B	230	290	5 85	7 38
B_1	200	250	5 09	6 36
C	120	200	3 05	5 09
D	015	023	0 38	0 59
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	025	050	0 64	1 27
J	008	015	0 20	0.38
K	070	150	1 78	3 82
L	300 BASIC		7 63 BASIC	
M	0°	15°	0°	15°
N	010	030	0 25	0 76
P	025	050	0 64	1 27

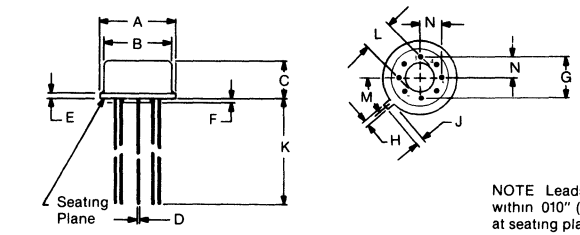
Small Outline Surface Mount



NOTE Leads in true position within 010" (25mm) R at MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	185	201	4.70	5 11
A_1	178	201	4 52	5 11
B	146	162	3 71	4 11
B_1	130	149	3 30	3 78
C	054	145	1 37	3 69
D	015	019	0 38	0 48
G	050 BASIC		1 27 BASIC	
H	018	026	0 46	0 66
J	008	012	0 20	0 30
L	220	252	5 59	6 40
M	0°	10°	0°	10°
N	000	012	0 00	0 30

TO-99 Package



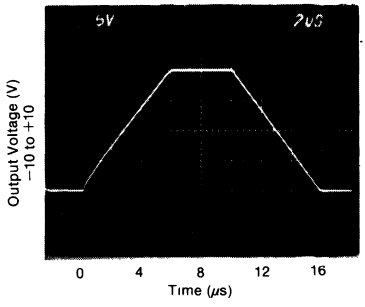
NOTE Leads in true position within 010" (25mm) R at MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	335	370	8 51	9 40
B	305	335	7 75	8 51
C	165	185	4 19	4 70
D	016	021	0 41	0 53
E	010	040	0 25	1 02
F	010	040	0 25	1 02
G	200 BASIC		5 08 BASIC	
H	028	034	0 71	0 86
J	029	045	0 74	1 14
K	500	—	12 7	—
L	110	160	2 79	4 06
M	45° BASIC		45° BASIC	
N	095	105	2 41	2 67

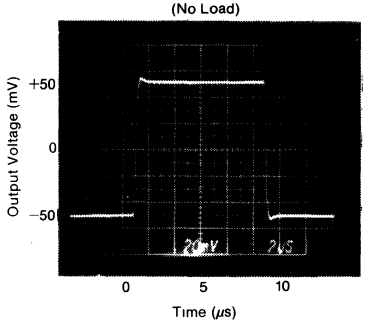
TYPICAL PERFORMANCE CURVES

T_A = 25°C, $\pm V_{CC}$ = 15VDC unless otherwise noted

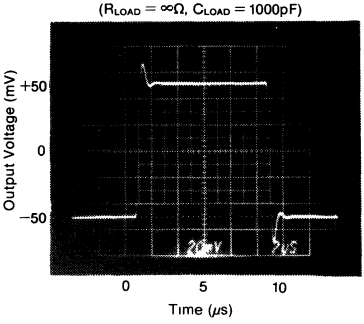
STEP RESPONSE



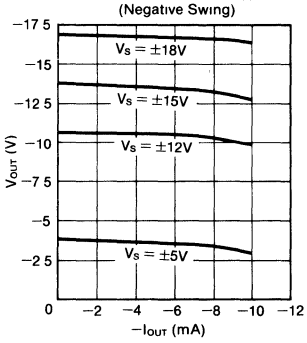
SMALL SIGNAL RESPONSE
(No Load)



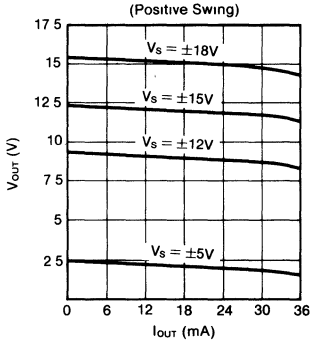
SMALL SIGNAL RESPONSE
(R_{LOAD} = ∞Ω, C_{LOAD} = 1000pF)



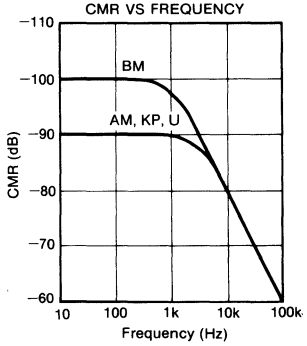
MAXIMUM V_{OUT} VS I_{OUT}
(Negative Swing)



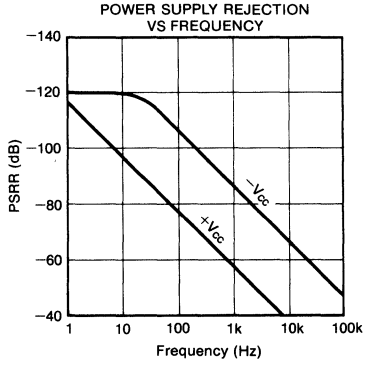
MAXIMUM V_{OUT} VS I_{OUT}
(Positive Swing)



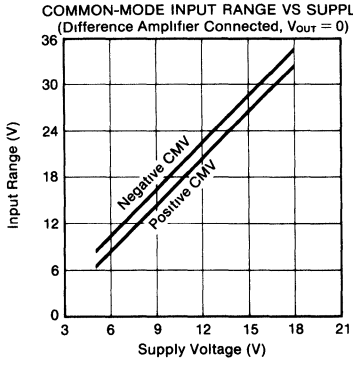
CMR VS FREQUENCY



POWER SUPPLY REJECTION
VS FREQUENCY



COMMON-MODE INPUT RANGE VS SUPPLY
(Difference Amplifier Connected, V_{OUT} = 0)



BURN-IN SCREENING

Burn-in screening is an option available for both the plastic- and ceramic-packaged INA105. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

DISCUSSION OF PERFORMANCE

The INA105 is the new solution to a widely occurring problem—how to realize a very accurate unity-gain differential amplifier at low cost. Burr-Brown's solution is a reliable monolithic circuit including both operational amplifier and thin-film resistors on the chip. State-of-the-art laser-trimming techniques assure total error of less than ±0.015% (gain error, nonlinearity, offsets, and common-mode rejection).

The performance of the unity-gain differential amplifier circuit can mistakenly be taken for granted. The necessary resistor accuracy is difficult to achieve, especially over temperature. Two classical techniques employed for obtaining the necessary accuracy are either manual trimming or the use of available packaged matched and tracking resistor networks. Both are expensive compared to the cost of the complete INA105.

The INA105 provides the total solution. By using a computer-controlled laser-trimming procedure, both accuracy and low cost are guaranteed. This makes external adjustment of gain, CMR, and offset voltage unnecessary. The user can be assured of excellent accuracy over temperature due to the properties inherent in Burr-Brown's thin-film resistors.

Other advantages are also apparent. Design, purchasing, and inventory costs are reduced. Labor time in adjusting independent resistors is eliminated both during manufacturing and field repair. Best of all, expensive potentiometers are not required. This further enhances circuit reliability.

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. Supplies should be decoupled with 1μF tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance.

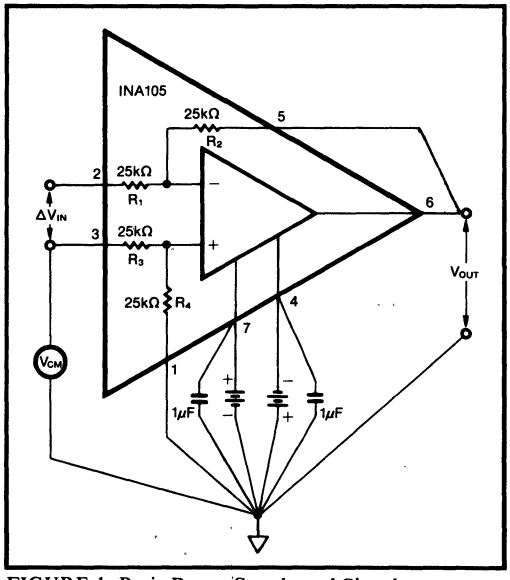


FIGURE 1. Basic Power Supply and Signal Connections.

OFFSET ADJUSTMENT

Figure 2 shows the offset adjustment circuit for the INA105. This circuit will allow ±300μV of adjustment and will not affect the gain accuracy or CMR.

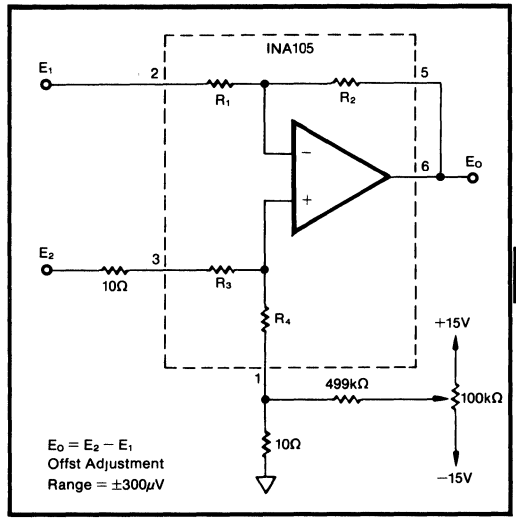


FIGURE 2. Offset Adjustment.

MAINTAINING COMMON-MODE REJECTION

Two factors are important in maintaining high CMR: (1) resistor matching and tracking (the internal INA105 circuitry does this for the user) and (2) source impedance including its imbalance.

Referring to Figure 1, the CMR depends upon the match of the internal R_4/R_3 ratio to the R_1/R_2 ratio. A CMR of 100dB requires resistor matching of 0.002%. To maintain 86dB, minimum CMR to +85°C, the resistor TCR tracking must be better than 2ppm/°C. These accuracies are difficult and expensive to reliably achieve with discrete components.

Any source impedance adds directly to the input resistors, R_1 and R_3, and will degrade DC and AC CMR. Likewise any wiring resistance adds directly to any of the precision difference resistors. A resistance of 0.5Ω (0.002% of 25kΩ) will degrade the 100dB CMR of the INA105; 5Ω will degrade the CMR to 80dB. Don't be tempted to interchange pins 1 and 3 or pins 2 and 5. The resistors in the INA105 are carefully matched to faithfully preserve the proper ratios. If they are switched, CMR and temperature drift performance will be degraded.

When input filters are used preceding an instrumentation amplifier (see Figure 5), care should also be taken to match RCs on the two input lines. For example, mismatched input filters for high frequencies will reduce the CMR at lower frequencies, e.g, 60Hz. Differential filters will not degrade AC CMR.

RESISTOR NOISE IN THE INA105

Figure 3 shows the model for calculating resistor noise in the INA105. Resistors have Johnson noise resulting from thermal agitation. The expression for this noise is:

$$E_{RMS} = \sqrt{4KTRB}$$

Where: K = Boltzman's constant (J/°K)
T = Absolute temperature (°K)
R = Resistance (Ω)
B = Bandwidth (Hz)

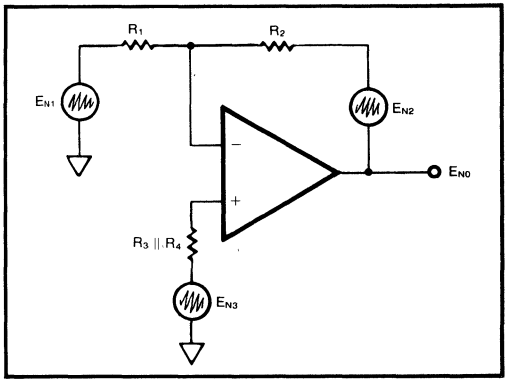


FIGURE 3. Resistor Noise Model.

At room temperature, this noise becomes:

$$E_N = 1.3^{-10}\sqrt{R} \qquad (V/\sqrt{Hz})$$

The three noise sources in Figure 2 are:

$$E_{N1} = 1.3^{-10}(R_2/R_1)\sqrt{R_1}$$

$$E_{N2} = 1.3^{-10}\sqrt{R_2}$$

$$E_{N3} = 1.3^{-10}(1 + R_2/R_1)\sqrt{R_3||R_4}$$

The output noise (given $R_1 = R_2 = R_3 = R_4 = 25k\Omega$) is:

$$E_{NO} = 2.6^{-10}\sqrt{R}$$

$$\boxed{E_{NO} = 41nV_{RMS}/\sqrt{Hz}}$$

For example,

E_{NO} within a 100Hz BW = $410nV_{RMS}$
= $2460nV_{P-P}$ with a crest factor of 6 (statistically includes 99.7% of all noise peak occurrences)

This is the noise due to the resistors alone. It is included in the noise specification of the INA105.

APPLICATIONS CIRCUITS

The INA105 is ideally suited for a wide range of circuit functions. Figures 4 through 29 show many applications circuits ranging from difference amplifiers and single-ended gain blocks to average and absolute value amplifiers. It is ideal as a current-loop receiver. Also, since the positive output current drive has been extended, it serves uniquely as a current transmitter for ranges such as 4mA to 20mA. When using these applications recall that the internal 25kΩ resistors are ratio-matched but ±20% absolute.

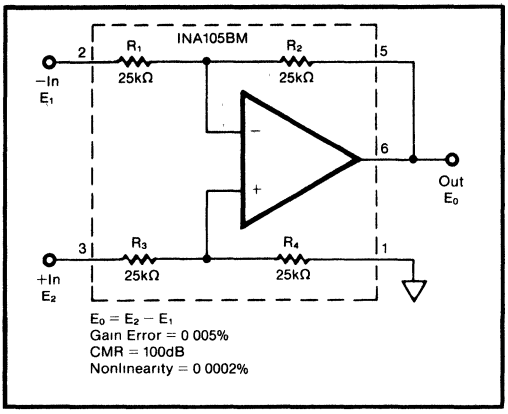
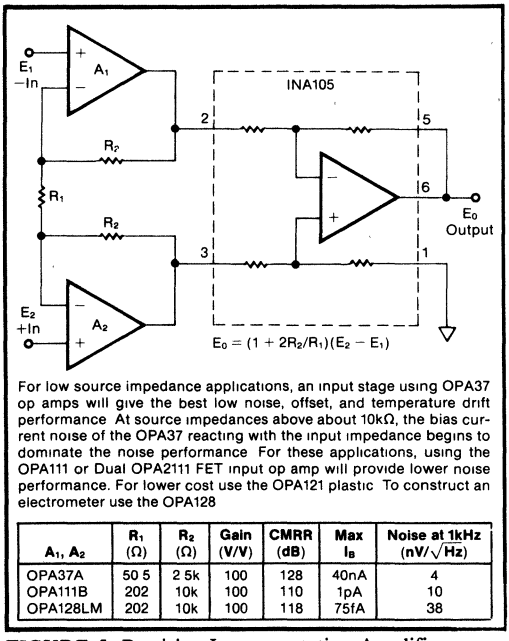


FIGURE 4. Precision Difference Amplifier.



For low source impedance applications, an input stage using OPA37 op amps will give the best low noise, offset, and temperature drift performance At source impedances above about 10kΩ, the bias current noise of the OPA37 reacting with the input impedance begins to dominate the noise performance For these applications, using the OPA111 or Dual OPA2111 FET input op amp will provide lower noise performance. For lower cost use the OPA121 plastic To construct an electrometer use the OPA128

A_1, A_2	R_1 (Ω)	R_2 (Ω)	Gain (V/V)	CMRR (dB)	Max I_B	Noise at 1kHz (nV/√Hz)
OPA37A	50 5	2 5k	100	128	40nA	4
OPA111B	202	10k	100	110	1pA	10
OPA128LM	202	10k	100	118	75fA	38

FIGURE 5. Precision Instrumentation Amplifier.

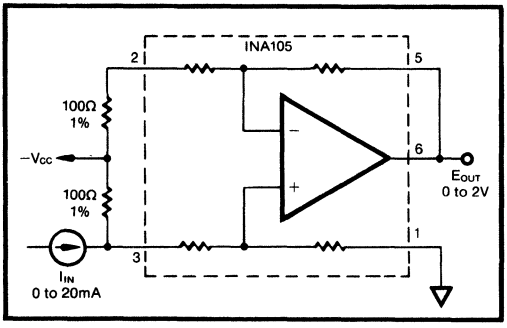


FIGURE 6. Current Receiver with Compliance to Rails.

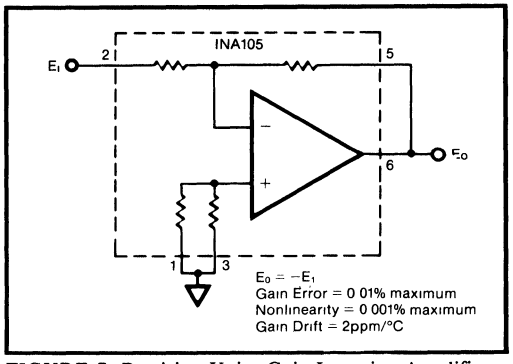


FIGURE 7. Precision Unity-Gain Inverting Amplifier.

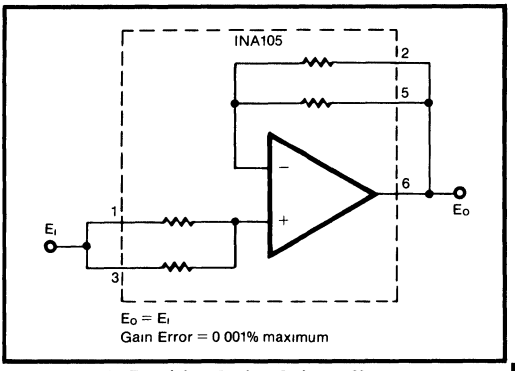


FIGURE 10. Precision Unity-Gain Buffer.

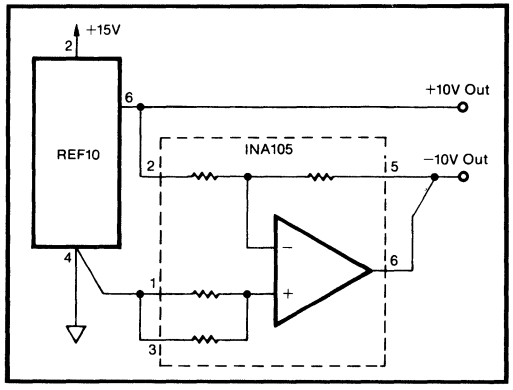


FIGURE 8. ±10V Precision Voltage Reference.

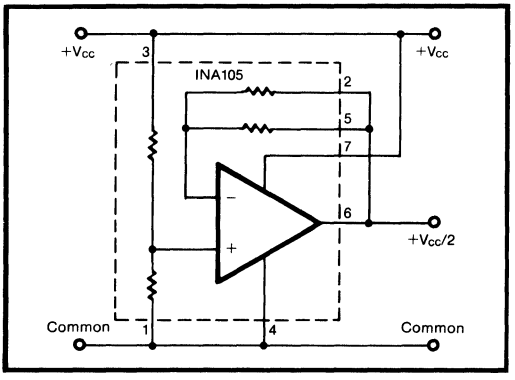


FIGURE 11. Pseudoground Generator.

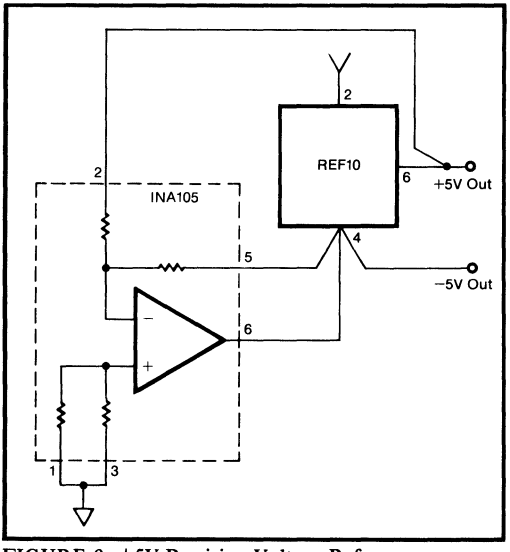


FIGURE 9. ±5V Precision Voltage Reference.

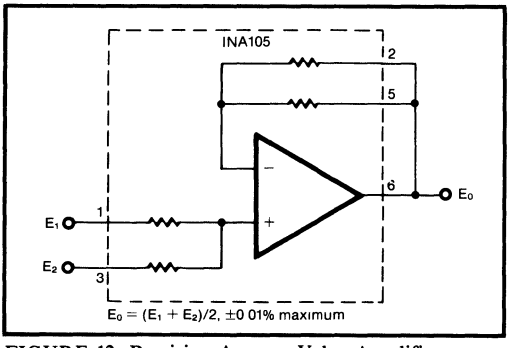


FIGURE 12. Precision Average Value Amplifier.

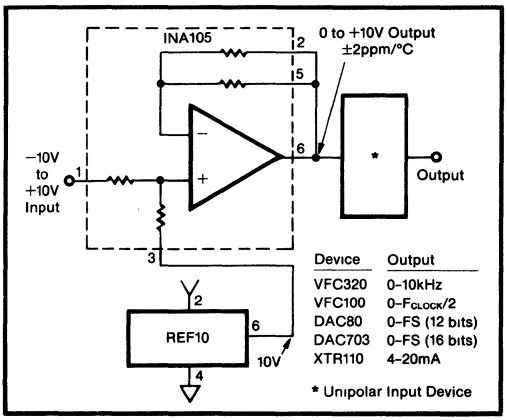


FIGURE 13. Precision Bipolar Offsetting.

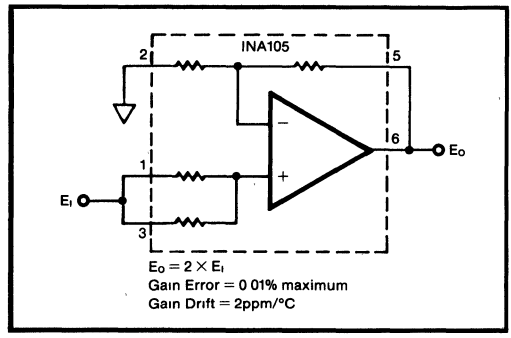


FIGURE 15. Precision (G = 2) Amplifier.

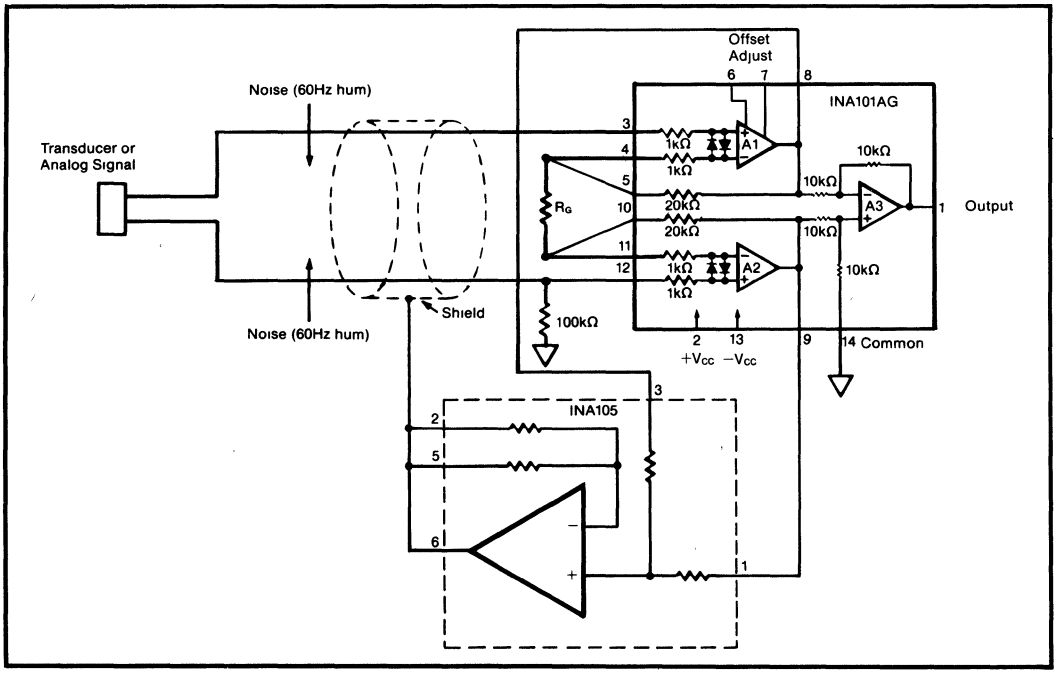


FIGURE 14. Instrumentation Amplifier Guard Drive Generator.

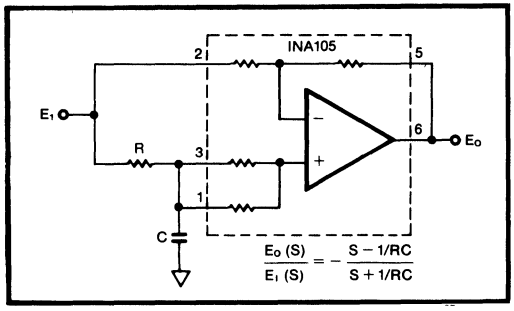


FIGURE 16. All-Pass Filter (provides unity gain and 0° to 180° phase shift output for frequencies of DC to ∞Hz).

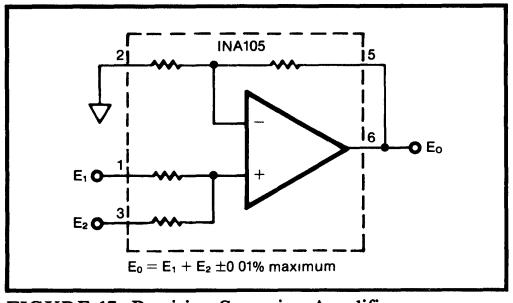


FIGURE 17. Precision Summing Amplifier.

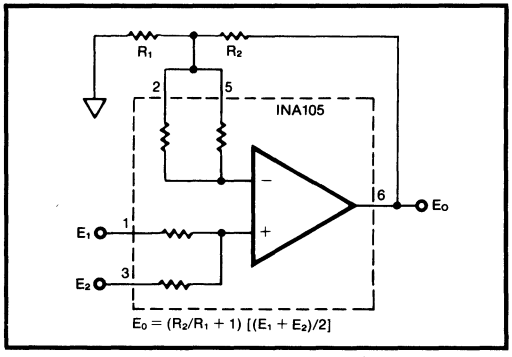


FIGURE 18. Precision Summing Amplifier with Gain.

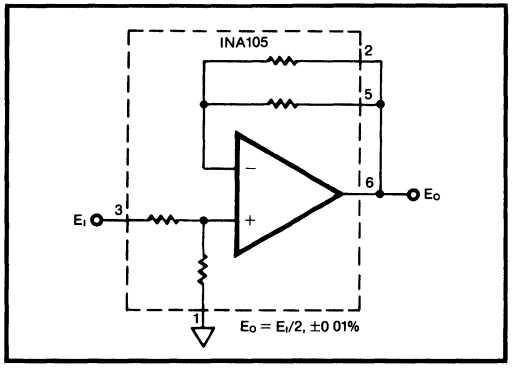


FIGURE 19. Precision (Gain = 1/2) Amplifier. Allows ±20V Input with ±15V Power Supplies.

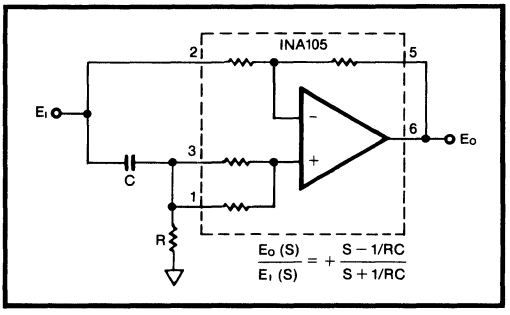


FIGURE 20. All-Pass Filter (provides unity gain and −180° to 0° phase shift output for frequencies of DC to ∞Hz).

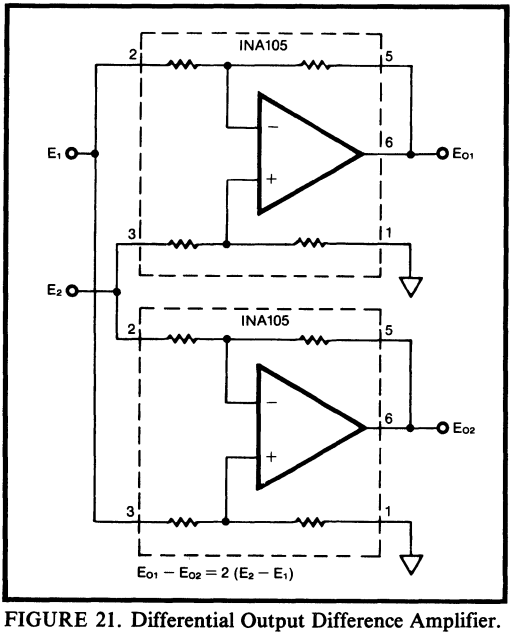


FIGURE 21. Differential Output Difference Amplifier.

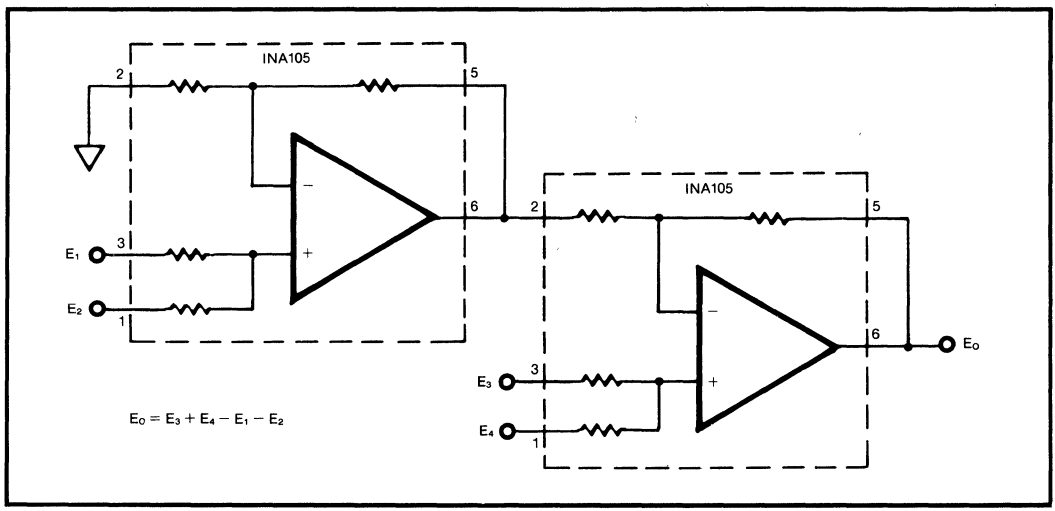


FIGURE 22. Precision Summing Instrumentation Amplifier.

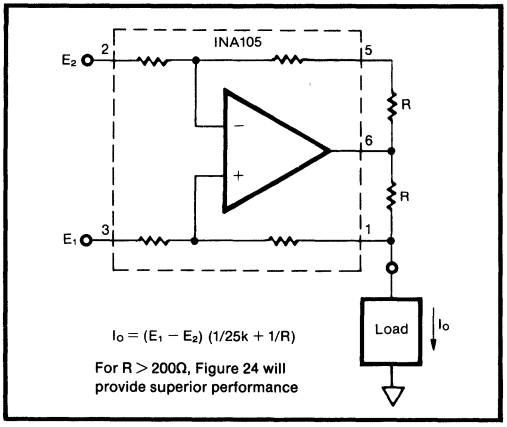


FIGURE 23. Precision Voltage-to-Current Converter with Differential Inputs.

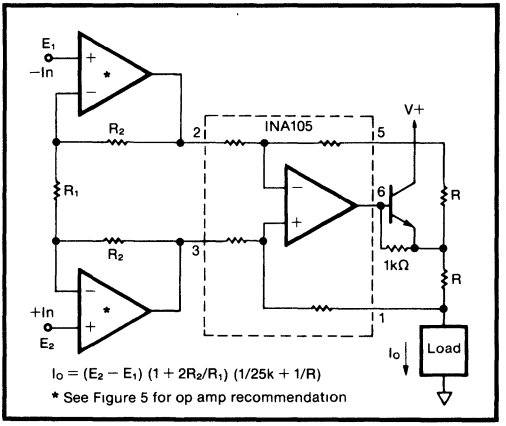


FIGURE 25. Precision Voltage-Controlled Current Source with Buffered Differential Inputs and Gain.

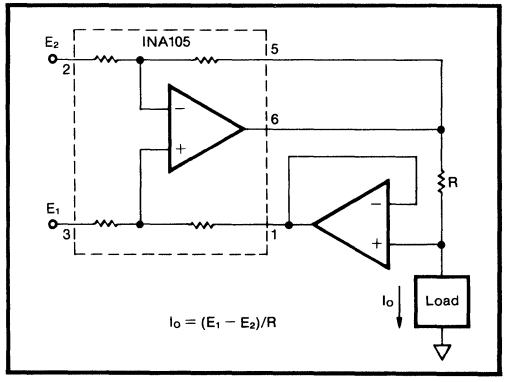


FIGURE 24. Differential Input Voltage-to-Current Converter for Low I_{OUT}.

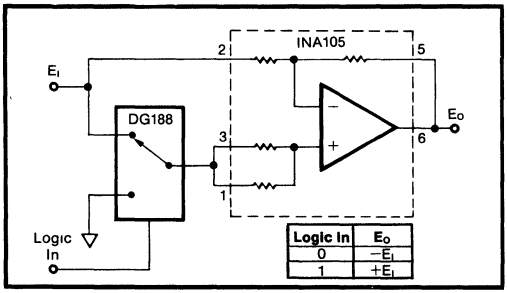


FIGURE 26. Digitally Controlled Gain of ±1 Amplifier.

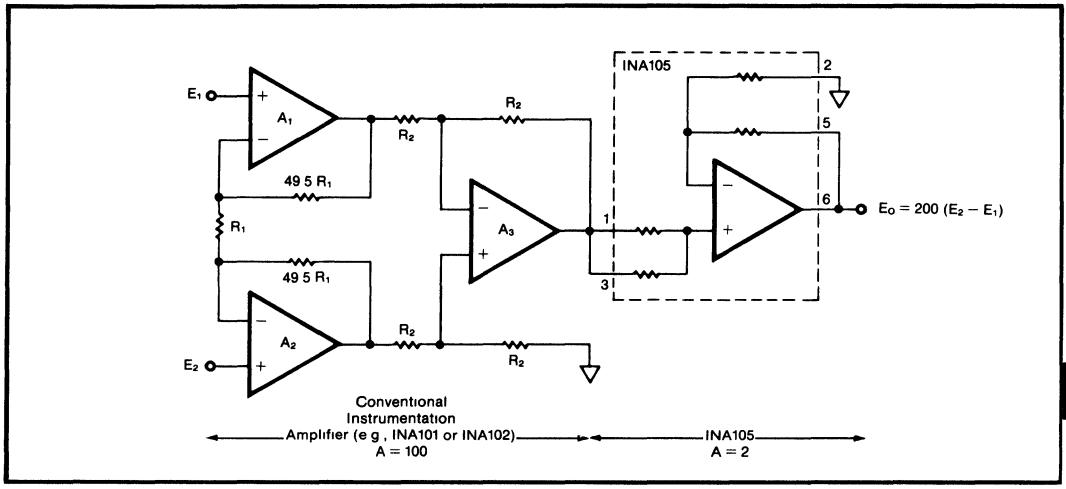


FIGURE 27. Boosting Instrumentation Amplifier Common-Mode Range From ±5V to ±7.5V with 10V Full-Scale Output.

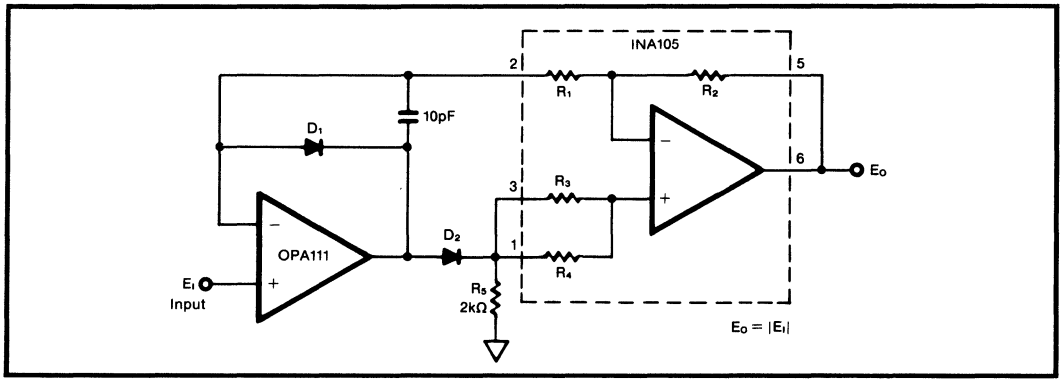


FIGURE 28. Precision Absolute Value Buffer.

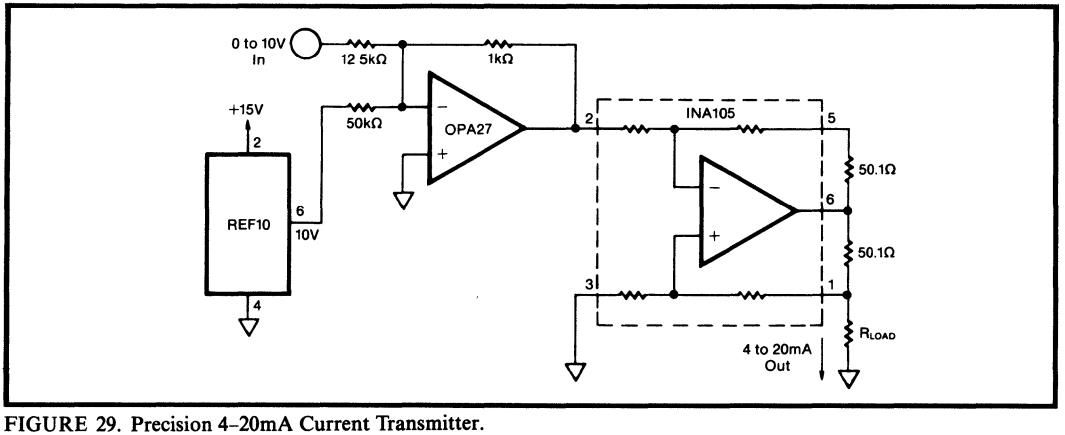


FIGURE 29. Precision 4–20mA Current Transmitter.

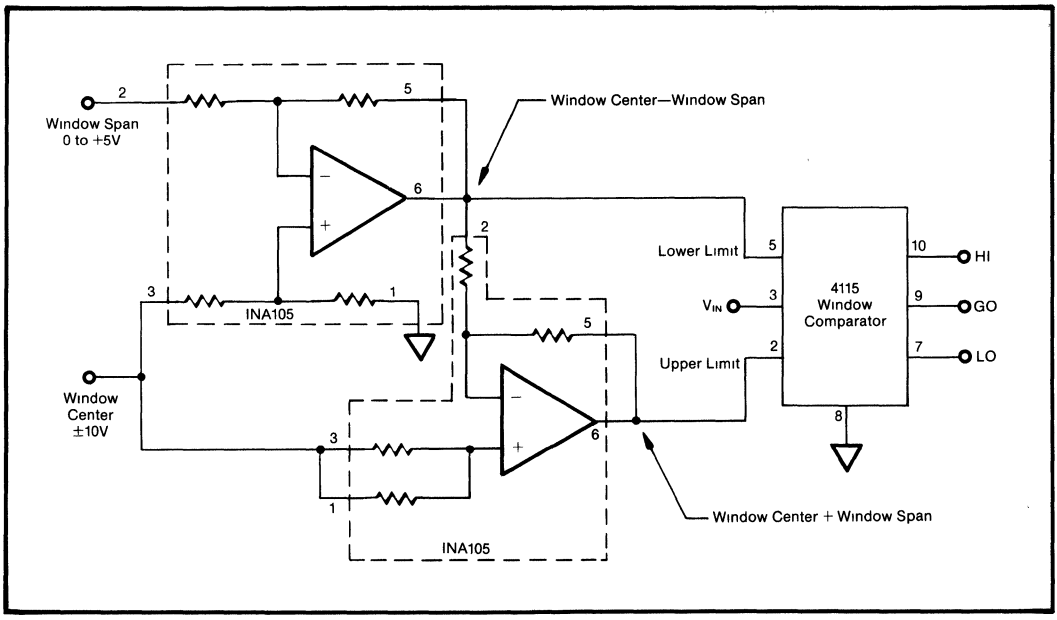


FIGURE 30. Window Comparator with Window Span and Window Center Inputs.

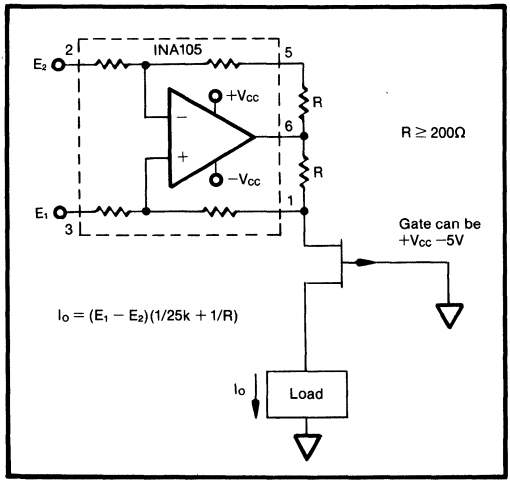


FIGURE 31. Isolating Current Source.

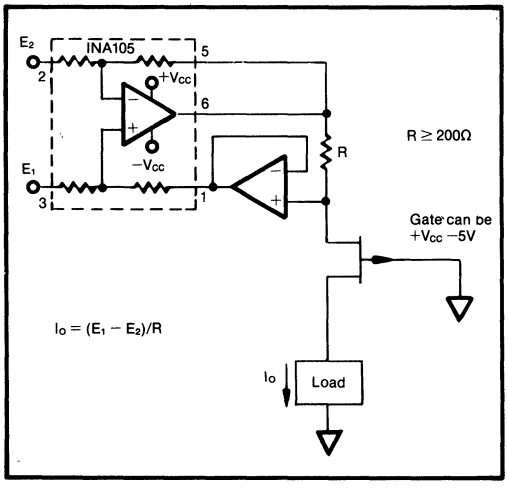
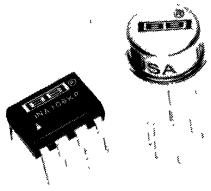


FIGURE 32. Isolating Current Source with Buffering Amplifier for Greater Accuracy.

BURR-BROWN®



INA106

Precision Fixed-Gain DIFFERENTIAL AMPLIFIER

FEATURES

- FIXED GAIN, A = 10
- CMR 100dB min over temp
- NONLINEARITY 0.001% max
- NO EXTERNAL ADJUSTMENTS REQUIRED
- EASY TO USE
- COMPLETE SOLUTION
- HIGHLY VERSATILE
- LOW COST
- TO-99 HERMETIC METAL AND LOW COST PLASTIC PACKAGES

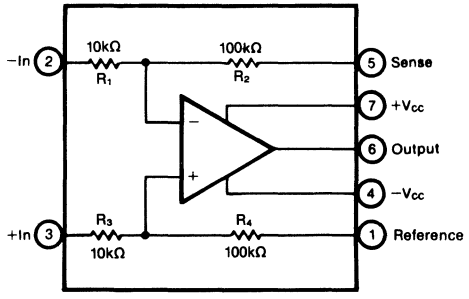
APPLICATIONS

- DIFFERENTIAL AMPLIFIER, A = 10
- BASIC INSTRUMENTATION AMPLIFIER BUILDING BLOCK
- INVERTING AMPLIFIER, A = −10
- NONINVERTING AMPLIFIER, A = 10
- SUMMING AMPLIFIER, WEIGHTED
- ±100V CM RANGE DIFFERENTIAL AMPLIFIER

DESCRIPTION

The INA106 is a precision fixed-gain differential amplifier. As a monolithic circuit, it offers high reliability at low cost. It consists of a premium grade operational amplifier and an on-chip precision resistor network.

The INA106 is completely self-contained and offers the user a highly versatile function. No adjustments to gain, offset, and CMR are necessary. This provides three important advantages: (1) lower initial design engineering time, (2) lower manufacturing assembly time and cost, and (3) easy cost-effective field repair of a precision circuit.



International Airport Industrial Park • P.O. Box 11400 • Tucson, Arizona 85734 • Tel.: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491

PDS-729B

SPECIFICATIONS

ELECTRICAL

At +25°C, V_{CC} = ±15V unless otherwise noted

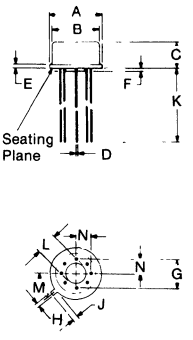
PARAMETER	CONDITIONS	INA106AM MIN	INA106AM TYP	INA106AM MAX	INA106BM MIN	INA106BM TYP	INA106BM MAX	INA106KP MIN	INA106KP TYP	INA106KP MAX	UNITS
GAIN											
Initial[1]			10			*			*		V/V
Error			0.005	0 01		*	*		0.01	0.025	%
vs Temperature			−4	±10		*	*		*		ppm/°C
Nonlinearity[2]			0.0002	0.001		*	*		*	*	%
OUTPUT											
Rated Voltage	I_O = +20mA, −5mA	10	12		*	*		*	*		V
Rated Current	E_O = 10V	+20, −5			*			*			mA
Impedance			0.01			*			*		Ω
Current Limit	To common		+40/−10			*			*		mA
Capacitive Load	Stable operation		1000			*			*		pF
INPUT											
Impedance	Differential		10			*			*		kΩ
	Common-mode		110			*			*		kΩ
Voltage Range	Differential	±1			*			*			V
	Common-mode	±11			*			*			V
Common-mode Rejection[3]	$T_A = T_{MIN}$ to T_{MAX}	94	100		100	106		86	*		dB
OFFSET VOLTAGE	RTI[4]										
Initial			50	100		*	*		*	200	µV
vs Temperature			0 2	5		*	2		*		µV/°C
vs Supply	$\pm V_{CC}$ = 6V to 18V		1	10		*	*		*	*	µV/V
vs Time			10			*			*		µV/mo
OUTPUT NOISE VOLTAGE	RTI[5]										
F_B = 0 01Hz to 10Hz			1			*			*		µV p-p
F_O = 10kHz			30			*			*		nV/√Hz
DYNAMIC RESPONSE											
Gain Bandwidth	−3dB		5			*			*		MHz
Full Power BW	V_O = 20V p-p	30	50		*	*		*	*		kHz
Slew Rate		2	3		*	*		*	*		V/µs
Settling Time. 0 1%	V_O = 10V step		5			*			*		µs
0 01%	V_O = 10V step		10			*			*		µs
0 01%	V_{CM} = 10V step, V_{DIFF} = 0V		5			*			*		µs
POWER SUPPLY											
Rated			±15			*			*		V
Voltage Range	Derated performance	±5		±18	*		*	*		*	V
Quiescent Current	V_{OUT} = 0V		±1.5	±2		*	*		*	*	mA
TEMPERATURE RANGE											
Specification		−25		+85	*		*	0		+70	°C
Operation		−55		+125	*		*	−25		+85	°C
Storage		−65		+150	*		*	−40		+85	°C

* Specification same as for INA106AM

NOTES (1) Connected as difference amplifier (see Figure 4). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output (3) With zero source impedance (see Maintaining CMR section). (4) Includes effects of amplifier's input bias and offset currents. (5) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

MECHANICAL

TO-99 Package

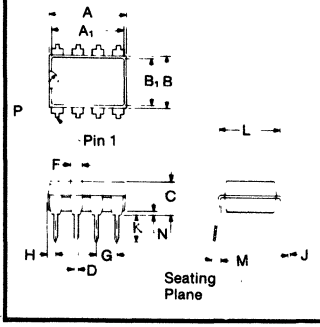


NOTE. Leads in true position within 0 01" (0 25 mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers are not marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	335	370	8.51	9 40
B	305	335	7 75	8 51
C	165	185	4.19	4.70
D	016	021	0 41	0 53
E	010	040	0 25	1 02
F	010	040	0 25	1.02
G	200 BASIC		5 08 BASIC	
H	028	034	0 71	0 86
J	029	045	0 74	1 14
K	500	—	12.7	—
L	110	160	2 79	4 06
M	45° BASIC		45° BASIC	
N	095	105	2 41	2 67

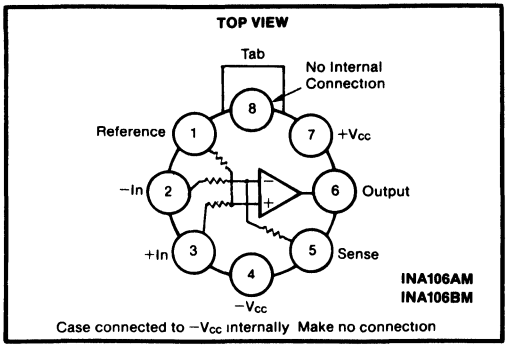
"P" Package—Plastic DIP



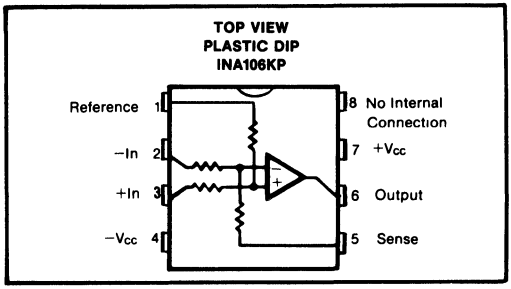
NOTE. Leads in true position within 0 01" (0 25mm) R at MMC at seating plane. Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	355	.400	9 02	10 16
A1	340	.385	8 64	9 78
B	230	290	5 84	7 37
B1	200	.250	5 08	6 35
C	120	200	3 05	5 08
D	015	023	0 38	0 58
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	025	050	0 64	1 27
J	008	015	0 20	0 38
K	070	150	1 78	3 81
L	300 BASIC		7 63 BASIC	
M	0°	15°	0°	15°
N	010	030	0.25	0 76
P	025	050	0 64	1 27

PIN DESIGNATIONS



PIN DESIGNATIONS



ABSOLUTE MAXIMUM RATINGS

Supply	±18V
Input Voltage Range	±Vcc
Operating Temperature Range: M	−55°C to +125°C
P	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short Circuit to Common	Continuous

ORDERING INFORMATION

INA106 X X

Basic Model Number

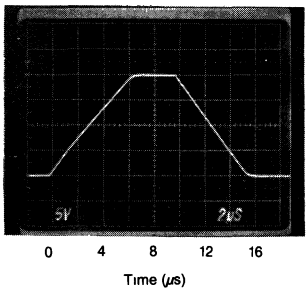
Performance Grade
A, B: −25°C to +85°C
K: 0°C to +70°C

Package Code
M: TO-99 metal can
P: 8-pin mini plastic DIP

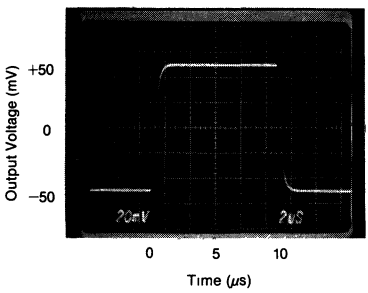
TYPICAL PERFORMANCE CURVES

T_A = 25°C, ±V_{CC} = 15V unless otherwise noted

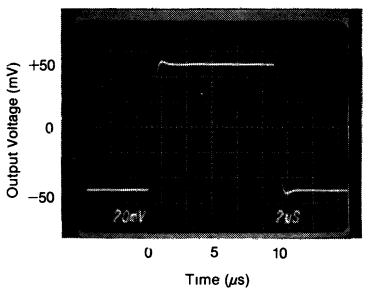
STEP RESPONSE



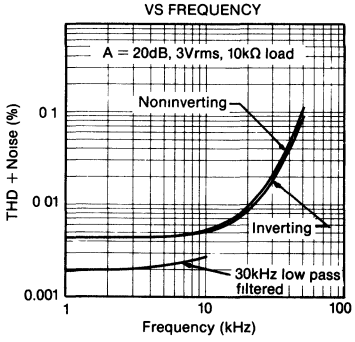
SMALL SIGNAL RESPONSE
(No Load)



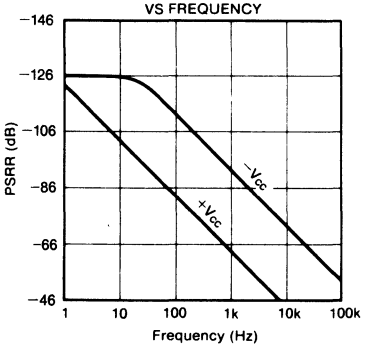
SMALL SIGNAL RESPONSE
(R_{LOAD} = ∞Ω, C_{LOAD} = 1000pF)



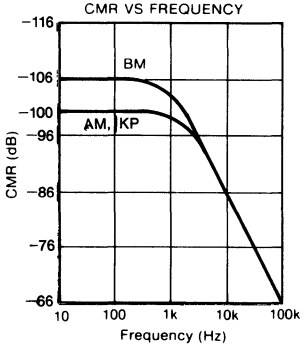
TOTAL HARMONIC DISTORTION AND NOISE
VS FREQUENCY



POWER SUPPLY REJECTION
VS FREQUENCY

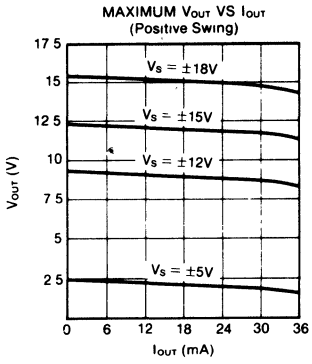


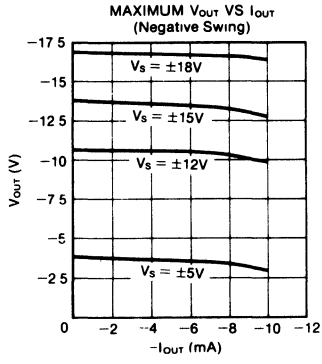
CMR VS FREQUENCY



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.





DISCUSSION OF PERFORMANCE

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. Supplies should be decoupled with 1μF tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance.

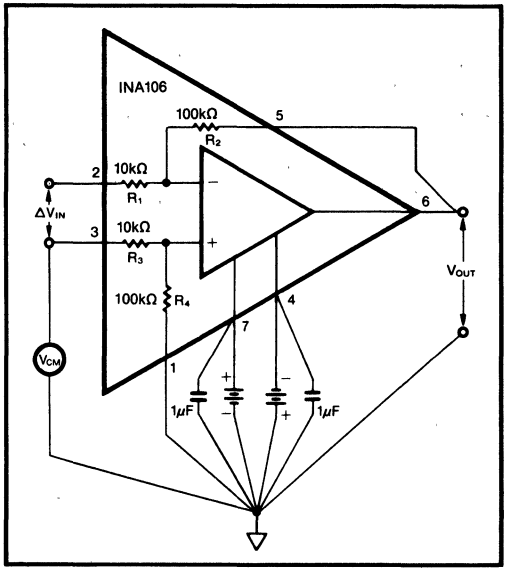


FIGURE 1. Basic Power Supply and Signal Connections.

OFFSET ADJUSTMENT

Figure 2 shows the offset adjustment circuit for the INA106. This circuit will allow ±3mV of adjustment and will not affect the gain accuracy or CMR.

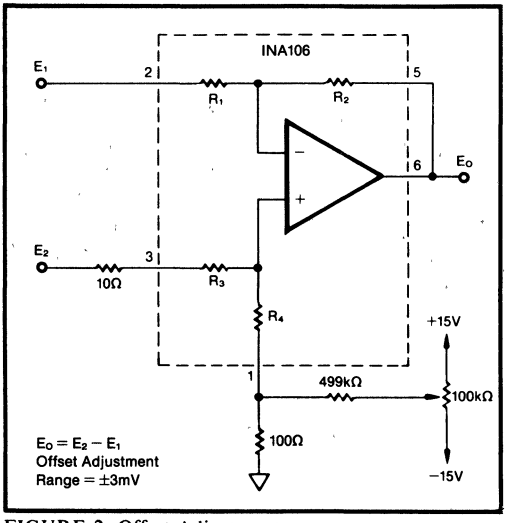


FIGURE 2. Offset Adjustment.

MAINTAINING COMMON-MODE REJECTION

Two factors are important in maintaining high CMR: (1) resistor matching and tracking (the internal INA106 circuitry does this for the user) and (2) source impedance including its imbalance.

Referring to Figure 1, the CMR depends upon the match of the internal R_4/R_3 ratio to the R_1/R_2 ratio. A CMR of 106dB requires resistor matching of 0.005%. To maintain 100dB, minimum CMR to +85°C, the resistor TCR tracking must be better than 2ppm/°C. These accuracies are difficult and expensive to reliably achieve with discrete components.

Any source impedance adds directly to the input resistors, R_1 and R_3, and will degrade DC and AC CMR. Likewise any wiring resistance adds directly to any of the precision difference resistors. A resistance of 0.5Ω (0.005% of 10kΩ) will degrade the 106dB CMR of the INA106; 5Ω will degrade the CMR to 86dB.

When input filters are used preceding an instrumentation amplifier, care should also be taken to match RCs on the two input lines. For example, mismatched input filters for high frequencies will reduce the CMR at lower frequencies, e.g, 60Hz. Differential filters will not degrade AC CMR.

RESISTOR NOISE IN THE INA106

Figure 3 shows the model for calculating resistor noise in the INA106. Resistors have Johnson noise resulting from thermal agitation. The expression for this noise is:

$$E_{RMS} = \sqrt{4KTRB}$$

Where: K = Boltzman's constant (J/°K)
T = Absolute temperature (°K)
R = Resistance (Ω)
B = Bandwidth (Hz)

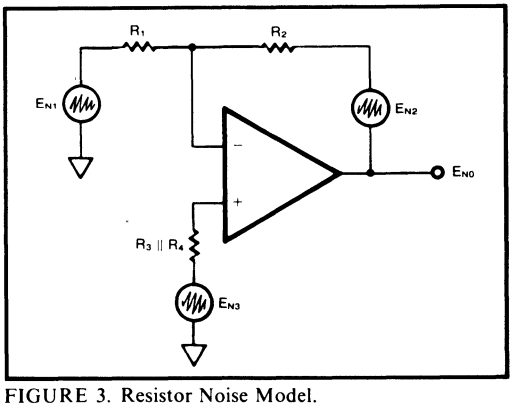


FIGURE 3. Resistor Noise Model.

At room temperature, this noise becomes:

$$E_N = 1.3^{-10}\sqrt{R} \qquad (V/\sqrt{Hz})$$

The three noise sources in Figure 2 are:

$$E_{N1} = 1.3^{-10}\,(R_2/R_1)\,\sqrt{R_1}$$
$$E_{N2} = 1.3^{-10}\,\sqrt{R_2}$$
$$E_{N3} = 1.3^{-10}\,(1 + R_2/R_1)\,\sqrt{R_3 \| R_4}$$

Adding as the root of the sums squared,

$$E_{NO} = 193nV\,\sqrt{Hz}$$

RTI, with A = 10,

$$E_{NI} = 19.3nV/\sqrt{Hz}$$

For example,

E_{NO} within a
600kHz BW = $0.15mV_{RMS}$
= 0.9mVp-p with a crest factor of 6 (statistically includes 99.7% of all noise peak occurrences)

This is the noise due to the resistors alone. It is included in the noise specification of the INA106.

APPLICATIONS CIRCUITS

The INA106 is ideally suited for a wide range of circuit functions. The following figures show many applications circuits.

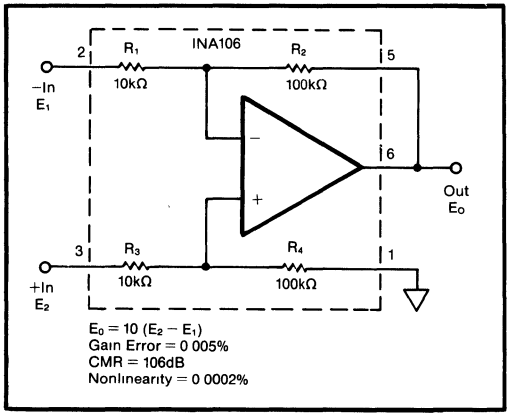


FIGURE 4A. Precision Difference Amplifier.

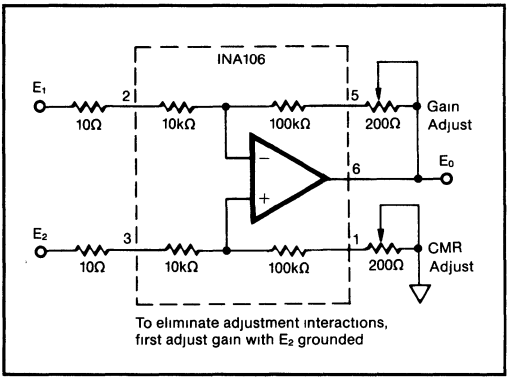
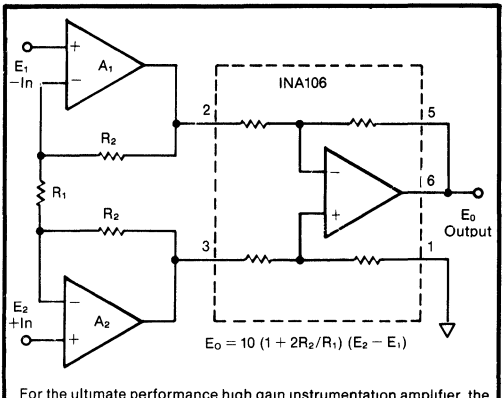


FIGURE 4B. Difference Amplifier With Gain And CMR Adjust.



For the ultimate performance high gain instrumentation amplifier, the INA106 can be combined with state-of-the-art op amps For low source impedance applications, an input stage using OPA37s will give the best low noise, offset, and temperature drift At source impedances above about 10kΩ, the bias current noise of the OPA37 reacting with the input impedance begins to dominate the noise For these applications, using an OPA111 or a dual OPA2111 FET input op amp will provide lower noise For an electrometer grade IA, use the OPA128 (See table below)

Using the INA106 for the difference amplifier also extends the input common-mode range of the instrumentation amplifier to ±10V A conventional IA with a unity-gain difference amplifier has an input common-mode range limited to ±5V for an output swing of ±10V This is because a unity-gain difference amp needs ±5V at the input for 10V at the output, allowing only 5V additional for common mode

A_1, A_2	R_1 (Ω)	R_2 (kΩ)	Gain (V/V)	CMRR (dB)	I_b (pA)	Noise at 1kHz (nV/√Hz)
OPA37A	50 5	2 5	1000	128	40000	4
OPA111B	202	10	1000	110	1	10
OPA128LM	202	10	1000	118	0 075	38

FIGURE 5. Precision Instrumentation Amplifier.

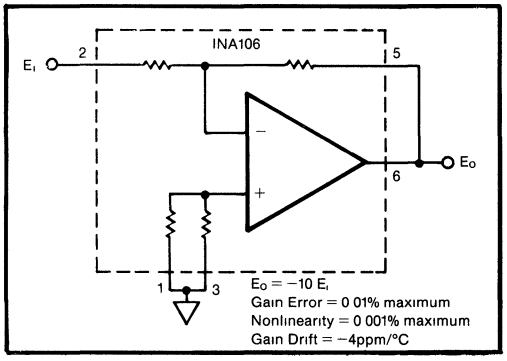


FIGURE 6. Precision Inverting Amplifier with Gain of –10.

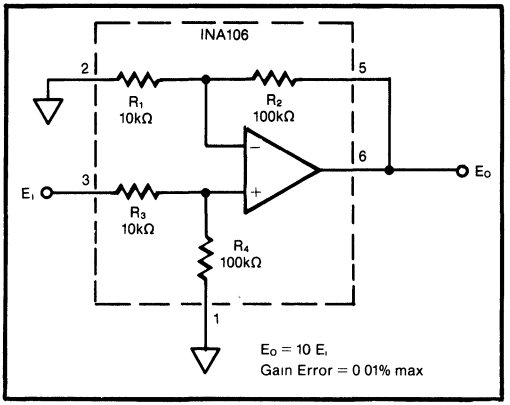


FIGURE 7. Precision Noninverting Amplifier with Gain of 10.

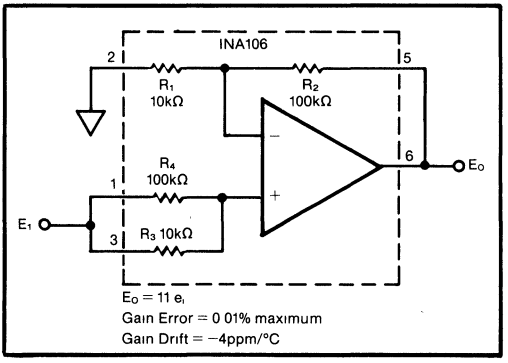


FIGURE 8. Precision Noninverting Amplifier with Gain of 11.

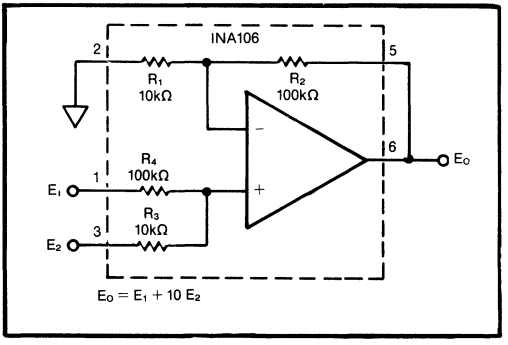
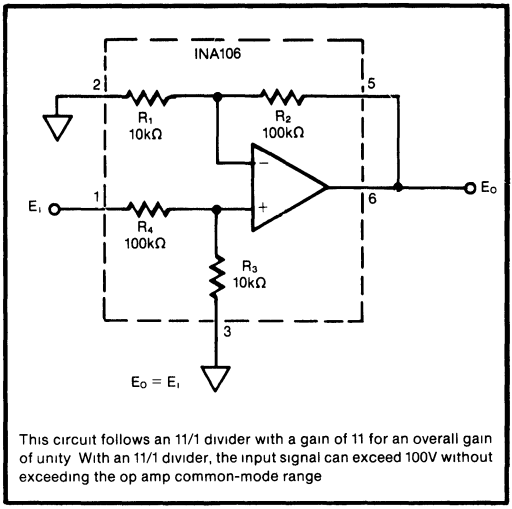


FIGURE 9. Precision Summing Amplifier with Weighted Inputs.



This circuit follows an 11/1 divider with a gain of 11 for an overall gain of unity With an 11/1 divider, the input signal can exceed 100V without exceeding the op amp common-mode range

FIGURE 10. Voltage Follower with Input Protection.

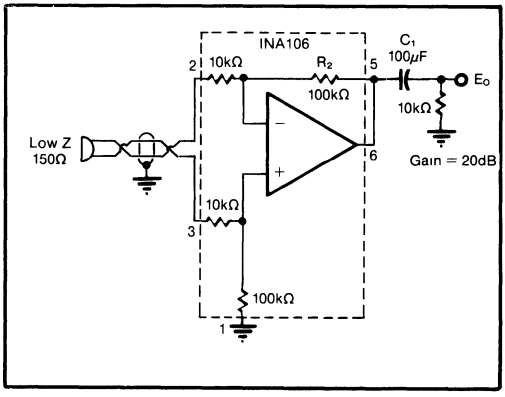
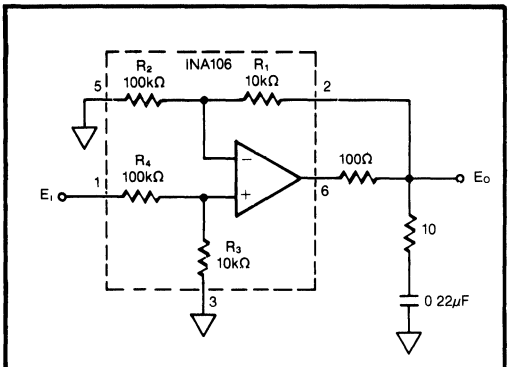


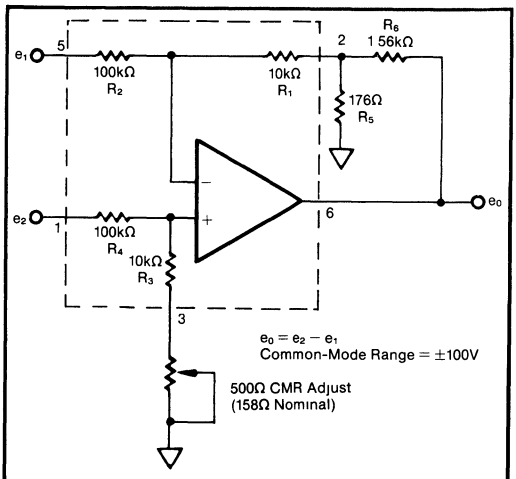
FIGURE 11. Differential-Input, Low-Impedance, Microphone Preamplifier (20dB gain).



Gain = 1/10
Also Gain = −1/10 by grounding R_4 and driving R_2
Gain = 1/10 differential driving both R_2 and R_4

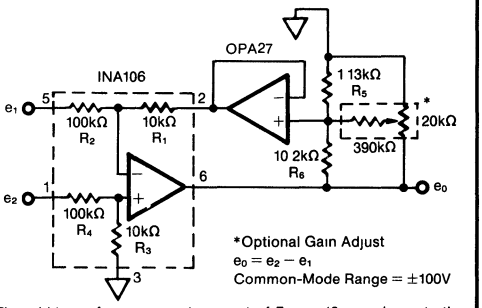
The 100Ω, 10Ω, 0 22μF network on the output assures stability by inserting a 70kHz zero and 700kHz pole to decrease the loop gain by 10 at 700kHz With the output taken at the junction of the 100Ω and 10Ω resistors, gain accuracy is maintained, and noise gain at the output remains at unity For a 10V output swing, the load should be limited to 10kΩ since the 100Ω resistor acts as a voltage divider with the load Also the large signal bandwidth will be limited by the ability of the amplifier to slew into the 0 22μF capacitor Assuming 10mA output current and a 20Vp-p output signal, the full power bandwidth will be 1 0kHz Since the circuit is a 10/1 attenuator, this would assume a 200Vp-p input signal With a 20Vp-p input signal, the bandwidth would be 10kHz

FIGURE 12. Precision Attenuator.



The addition of two external resistors and a pot turns the INA106 into a unity-gain difference amplifier with input common-mode range exceeding ±100V The circuit requires CMR adjustment and has a 2% gain accuracy Better gain accuracy is difficult to obtain, since CMR and gain adjustments interact See Figure 14

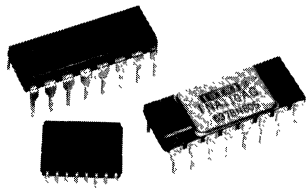
FIGURE 13. ±100V Common-Mode Range Difference Amplifier.



The addition of an op amp to circuit of Figure 13 can eliminate the need for CMR and gain adjustments CMR will be 20dB lower than that of the INA106, which is specified in a gain of 10 Gain accuracy is set strictly by the R_5, R_6 ratio and the initial gain accuracy of the INA106 ($A = 1 + R_6/R_5 \pm 01\%$) CMR can be adjusted by adding a 10Ω resistor in series with R_1 (pin 2) and a 20Ω pot in series with R_3 (pin 2) Gain and CMR adjustments do not interact

FIGURE 14. ±100V Common-Mode Range Difference Amplifier Requiring No Adjustments.

BURR-BROWN®



INA110

AVAILABLE IN DIE FORM

Fast-Settling FET-Input Very High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- LOW BIAS CURRENT: 50pA, max
- FAST SETTLING: 4μs to 0.01%
- HIGH CMR: 106dB, min; 90dB at 10kHz
- CONVENIENT INTERNAL GAINS: 1, 10, 100, 200, 500
- VERY-LOW GAIN DRIFT: 10 to 50ppm/°C
- LOW OFFSET DRIFT: 2μV/°C
- LOW COST
- PINOUT COMPATIBLE WITH AD524 AND AD624, allowing upgrading of many existing applications

APPLICATIONS

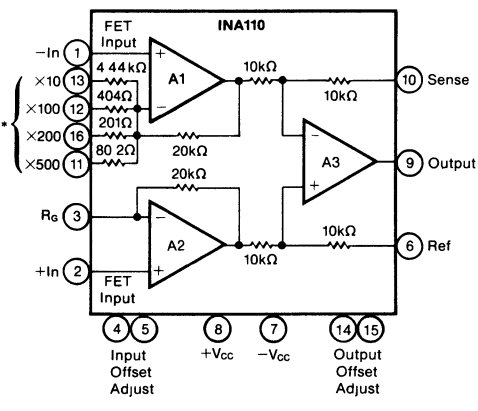
- Fast scanning rate multiplexed input data acquisition system amplifier
- Fast differential pulse amplifier
- High speed, low drift gain block
- Amplification of low level signals from high impedance sources and sensors
- Instrumentation amplifier with input low pass filtering using large series resistors
- Instrumentation amplifier with overvoltage input protection using large series resistors
- Amplification of signals from strain gauges, thermocouples, and RTDs

DESCRIPTION

The INA110 is a monolithic FET input instrumentation amplifier with a maximum bias current of 50pA. The circuit provides fast settling of 4μs to 0.01%. Laser trimming guarantees exceptionally good DC performance. Voltage noise is low, and current noise is virtually zero. Internal gain set resistors guarantee high gain accuracy and low gain drift. Gains of 1, 10, 100, 200, and 500 are provided.

The inputs are inherently protected by P-channel FETs on each input. Differential and common-mode voltages should be limited to $\pm V_{CC}$. When severe overvoltage exists, use diode clamps as shown in the application section.

The INA110 is ideally suited for applications requiring large input resistors for overvoltage protection or filtering. Input signals from high source impedances can easily be handled without degrading DC performance. Fast settling for rapid scanning data acquisition systems is now achievable with one component, the INA110.



* Connect to R_G for desired gain

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx. 910-952-1111 - Cable BBRCORP - Telex. 66-6491

PDS-645B

SPECIFICATIONS

ELECTRICAL

At +25°C, $\pm V_{CC}$ = 15VDC, R_L = 2kΩ unless otherwise noted

PARAMETER	CONDITIONS	INA110AG			INA110BG/SG			INA110KP/KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Range of Gain		1		800	*		*	*		*	V/V
Gain Equation[1]						G = 1 + [40K/(R_G + 50Ω)]					V/V
Gain Error, DC G = 1			0 002	0 04		*	0 02		*	*	%
G = 10			0 01	0 1		0 005	0 05		*	*	%
G = 100			0 02	0 2		0 01	0 1		*	*	%
G = 200			0 04	0 4		0 02	0 2		*	*	%
G = 500			0.1	1 0		0 05	0 5		*	*	%
Gain Temp Coefficient G = 1			±3	±20		*	±10		*		ppm/°C
G = 10			±4	±20		±2	±10		*		ppm/°C
G = 100			±6	±40		±3	±20		*		ppm/°C
G = 200			±10	±60		±5	±30		*		ppm/°C
G = 500			±25	±100		±10	±50		*		ppm/°C
Nonlinearity, DC G = 1			±0 001	±0 01		±0 0005	±0 005		*	*	% of FS
G = 10			±0.002	±0 01		±0 001	±0 005		*	*	% of FS
G = 100			±0 004	±0 02		±0 002	±0 01		*	*	% of FS
G = 200			±0 006	±0 02		±0 003	±0 01		*	*	% of FS
G = 500			±0 01	±0 04		±0 005	±0 02		*	*	% of FS
OUTPUT											
Voltage, R_L = 2kΩ	Over temp	±10	±12 7		*	*		*	*		V
Current	Over temp	±5	±25		*	*		*	*		mA
Short-Circuit Current			±25			*			*		mA
Capacitive Load	Stability		5000			*			*		pF
INPUT											
OFFSET VOLTAGE[2]											
Initial Offset G, P			±(100 + 1000/G)	±(500 + 5000/G)		±(50 + 600/G)	±(250 + 3000/G)		*	*	μV
U									±(200 + 2000/G)	±(1000+ 5000/G)	μV
vs Temperature			±(2 + 20/G)	±(5 + 100/G)		±(1 + 10/G)	±(2 + 50/G)		*		μV/°C
vs Supply	V_{CC} = ±6V to ±18V		±(4 + 60/G)	±(30 + 300/G)		±(2 + 30/G)	±(10 + 180/G)		*	*	μV/V
BIAS CURRENT											
Initial Bias Current	Each input		20	100		10	50		*	*	pA
Initial Offset Current			2	50		1	25		*	*	pA
Impedance Differential			$5\times10^{12}\|\|6$			*			*		Ω||pF
Common-Mode			$2\times10^{12}\|\|1$			*			*		Ω||pF
VOLTAGE RANGE	V_{IN} Diff = 0V[3]										
Range, Linear Response		±10	±12					*	*		V
CMR with 1kΩ Source Imbalance											
G = 1	DC	70	90		80	100		*	*		dB
G = 10	DC	87	104		96	112		*	*		dB
G = 100	DC	100	110		106	116		*	*		dB
G = 200	DC	100	110		106	116		*	*		dB
G = 500	DC	100	110		106	116		*	*		dB
NOISE, Input[4]											
Voltage, f_O = 10kHz			10			*			*		nV/√Hz
f_B = 0 1Hz to 10Hz			1			*			*		μVp-p
Current, f_O = 10kHz			1 8			*			*		fA/√Hz
NOISE, Output[4]											
Voltage, f_O = 10kHz			65			*			*		nV/√Hz
f_B = 0 1Hz to 10Hz			8			*			*		μVp-p
DYNAMIC RESPONSE											
Small Signal G = 1	−3dB		2 5			*			*		MHz
G = 10			2 5			*			*		MHz
G = 100			470			*			*		kHz
G = 200			240			*			*		kHz
G = 500			100			*			*		kHz
Full Power	V_{OUT} = ±10V, R_L = 2kΩ	190	270		*	*			*		kHz
Slew Rate	G = 1 to 100	12	17		*	*			*		V/μs
Settling Time											
0 1%, G = 1	V_O = 20V step		4			*			*		μs
G = 10			2			*			*		μs
G = 100			3			*			*		μs
G = 200			5			*			*		μs
G = 500			11			*			*		μs

* Same as INA110AG

ELECTRICAL (CONT)

PARAMETER	CONDITIONS	INA110AG MIN	INA110AG TYP	INA110AG MAX	INA110BG/SG MIN	INA110BG/SG TYP	INA110BG/SG MAX	INA110KP/KU MIN	INA110KP/KU TYP	INA110KP/KU MAX	UNITS
Settling Time											
0 01%, G = 1	V_O = 20V step		5	12.5		*	*		*		µs
G = 10			3	7 5		*	*		*		µs
G = 100			4	7 5		*	*		*		µs
G = 200			7	12 5		*	*		*		µs
G = 500			16	25		*	*		*		µs
Overload Recovery[5]	50% overdrive		1			*			*		µs
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range		±6		±18	*		*	*		*	V
Quiescent Current	V_O = 0V		±3.0	±4 5		*	*		*	*	mA
TEMPERATURE RANGE											
Specification A, B, K		−25		+85	*		*	0		+70	°C
S					−55		+125				°C
Operation		−55		+125	*		*	−25		+85	°C
Storage		−65		+150	*		*	−40		+85	°C
θ_{JA}			100			*			*		°C/W

* Same as INA110AG

NOTES (1) Gains other than 1, 10, 100, 200, and 500 can be set by adding an external resistor, R_G, between pin 3 and pins 11, 12, and 16 Gain accuracy is a function of R_G and the internal resistors which have a ±20% tolerance with 20ppm/°C drift (2) Adjustable to zero (3) For differential input voltage other than zero, see Typical Performance Curves (4) $V_{NOISE\ RTI} = \sqrt{V_{N\ INPUT}^2 + (V_{N\ OUTPUT}/Gain)^2}$ (5) Time required for output to return from saturation to linear operation following the removal of an input overdrive voltage

ABSOLUTE MAXIMUM RATINGS

Supply ..... ±18V
Input voltage Range ..... $\pm V_{CC}$
Operating Temperature Range: G. ..... −55°C to +125°C
P, U... .. −25°C to +85°C
Storage Temperature Range: G ..... −65°C to +150°C
P, U .... −40°C to +85°C
Lead Temperature (soldering 10s): G, P..... +300°C
(soldering 3s): U.. ..... +260°C
Output Short-Circuit Duration . .... Continuous to Common

BURN-IN SCREENING

Burn-in screening is an option available for both the plastic- and ceramic-packaged INA110. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

PIN CONFIGURATION

−In	1	16	×200
+In	2	15	Output Offset Adjust
RG	3	14	Output Offset Adjust
Input Offset Adjust	4	13	×10
Input Offset Adjust	5	12	×100
Reference	6	11	×500
$-V_{CC}$	7	10	Output Sense
$+V_{CC}$	8	9	Output

ORDERING INFORMATION

Model	Package	Temperature Range
INA110AG	Ceramic DIP	−25°C to +85°C
INA110BG	Ceramic DIP	−25°C to +85°C
INA110SG	Ceramic DIP	−55°C to +125°C
INA110KP	Plastic DIP	0°C to +70°C
INA110KU	Plastic SO	0°C to +70°C

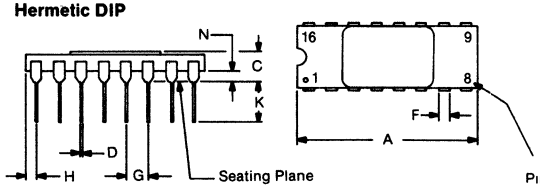
BURN-IN SCREENING OPTION
See text for details

Model	Package	Burn-In Temp. (160h)[1]
INA110AG-BI	Ceramic DIP	+125°C
INA110BG-BI	Ceramic DIP	+125°C
INA110SG-BI	Ceramic DIP	+125°C
INA110KP-BI	Plastic DIP	+85°C
INA110KU-BI	Plastic SO	+85°C

NOTE Or equivalent combination. See text

MECHANICAL

Hermetic DIP

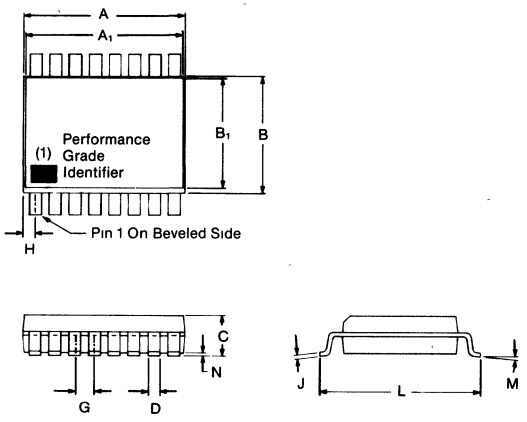


NOTE Leads in true position within .010" (.25mm) R at seating plane

Pin numbers shown for reference only Numbers are not marked on package

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	790	810	20 07	20.57
C	105	170	2 67	4 32
D	015	021	0 38	0 53
F	048	060	1 22	1 52
G	100 BASIC		2 54 BASIC	
H	030	070	0 76	1 78
J	008	012	0 20	0 30
K	120	240	3 05	6 10
L	300 BASIC		7 62 BASIC	
M	—	10°	—	10°
N	025	060	0 64	1 52

Small Outline Surface Mount

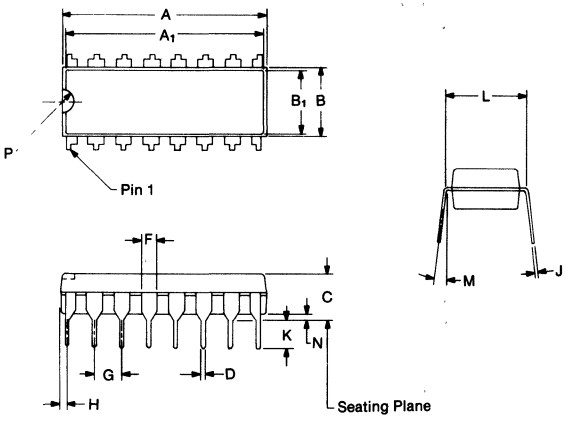


NOTE Leads in true position within 0 010" (25mm) R at MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	400	416	10 16	10 57
A_1	388	412	9 86	10 46
B	286	302	7 26	7 67
B_1	268	286	6 81	7 26
C	093	109	2 36	2 77
D	015	020	0 38	0 51
G	050 BASIC		1 27 BASIC	
H	022	038	0 56	0.97
J	008	012	0 20	0.30
L	391	421	9 93	10.69
M	5° TYP		5° TYP	
N	000	.012	0 00	0 30

(1) Performance grade identifier box for small outline surface mount Blank indicates K grade Part is marked INA110U.

Plastic DIP



NOTE: Leads in true position within 010" (.25mm) R at MMC at seating plane

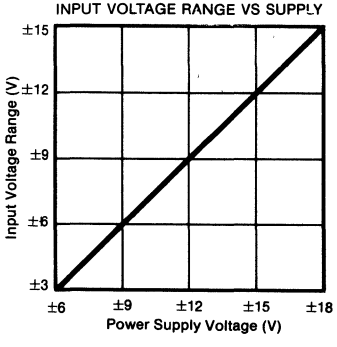
PINS: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

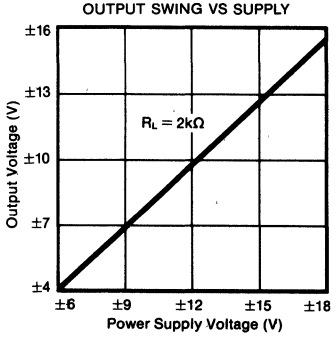
CASE: Plastic

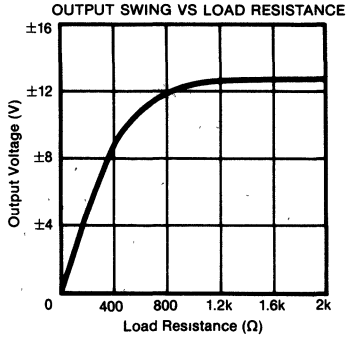
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	740	800	18.80	20.32
A_1	725	785	18 42	19.94
B	.230	.290	5 85	7 38
B_1	.200	250	5.09	6.36
C	120	200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	070	0.76	1 78
G	100 BASIC		2 54 BASIC	
H	0 02	0 05	0.51	1.27
J	.008	015	0 20	0 38
K	070	150	1 78	3 82
L	300 BASIC		7 63 BASIC	
M	0°	15°	0°	15°
N	010	030	0 25	0 76
P	025	050	0.64	1.27

TYPICAL PERFORMANCE CURVES

$T_A = 25°C$, $\pm V_{CC} = 15VDC$ unless otherwise noted



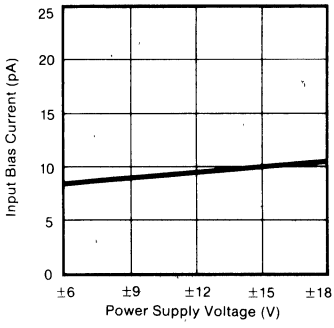




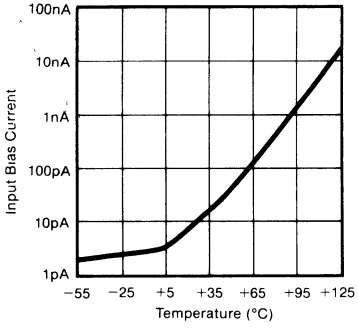
TYPICAL PERFORMANCE CURVES (CONT)

T_A = 25°C, $\pm V_{CC}$ = 15VDC unless otherwise noted

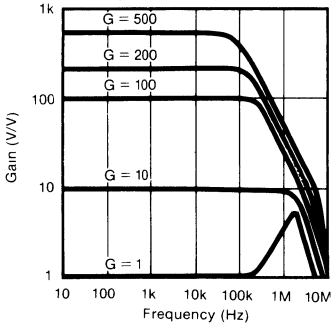
BIAS CURRENT VS SUPPLY



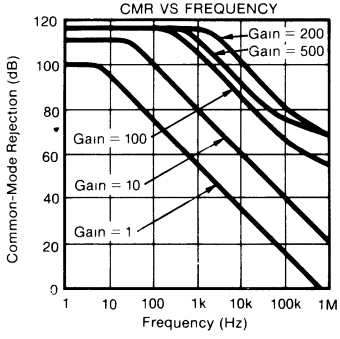
BIAS CURRENT VS TEMPERATURE



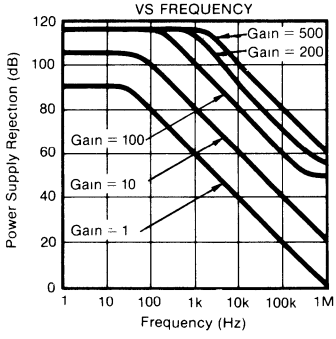
GAIN VS FREQUENCY



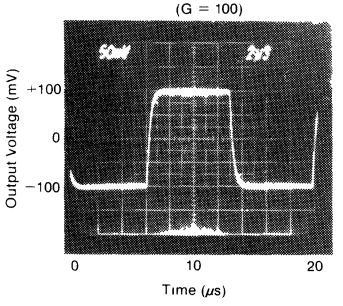
CMR VS FREQUENCY



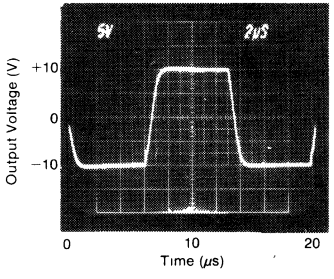
POWER SUPPLY REJECTION VS FREQUENCY



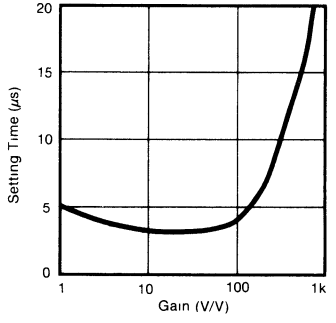
SMALL SIGNAL TRANSIENT RESPONSE (G = 100)



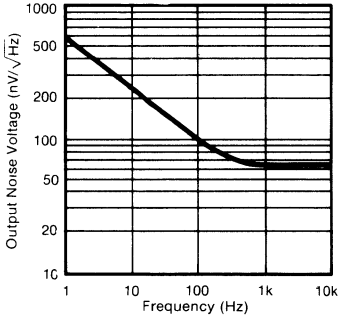
LARGE SIGNAL TRANSIENT RESPONSE (G = 100)



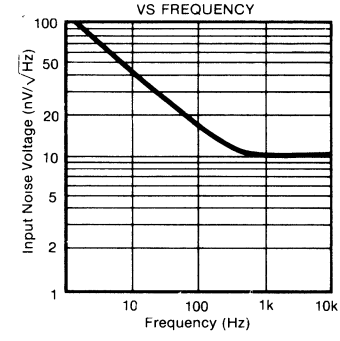
SETTLING TIME VS GAIN (0.01%, 20V STEP)



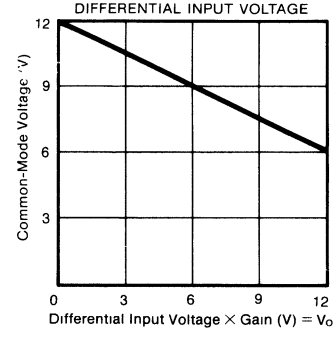
OUTPUT NOISE VOLTAGE VS FREQUENCY



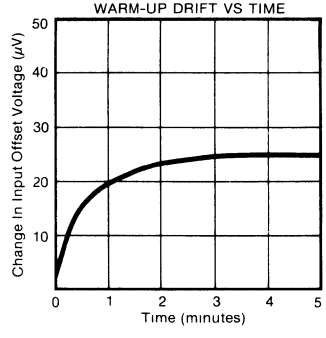
INPUT NOISE VOLTAGE VS FREQUENCY



COMMON-MODE VOLTAGE VS DIFFERENTIAL INPUT VOLTAGE



WARM-UP DRIFT VS TIME



DISCUSSION OF PERFORMANCE

A simplified diagram of the INA110 is shown on the first page. The design consists of the classical three operational amplifier configuration with precision FET buffers on the input. The result is an instrumentation amplifier with premium performance not normally found in integrated circuits.

The input section (A_1 and A_2) incorporates high performance, low bias current, and low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide high input impedance ($10^{12}\Omega$). Laser-trimming is used to achieve low offset voltage. Input cascoding assures low bias current and high CMR. Thin-film resistors on the integrated circuit provide excellent gain accuracy and temperature stability.

The output section (A_3) is connected in a unity-gain difference amplifier configuration. Precision matching of the four 10kΩ resistors, especially over temperature and time, assures high common-mode rejection.

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. Supplies should be decoupled with 1μF tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance. Resistance in series with the reference (pin 6) will degrade CMR. Also to maintain stability, avoid capacitance from the output to the gain set, offset adjust, and input pins. The layout shown in Figure 2 is suggested for best performance.

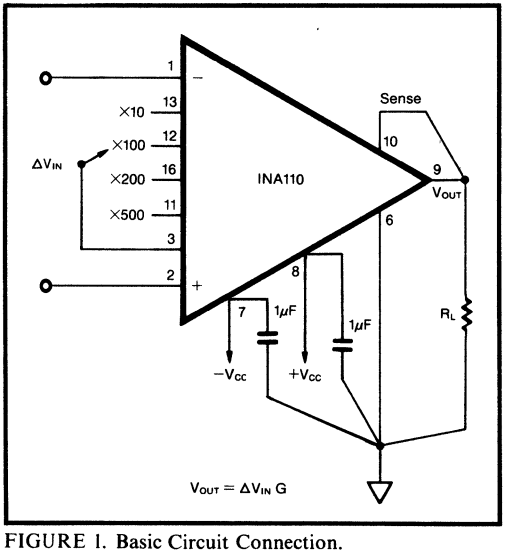


FIGURE 1. Basic Circuit Connection.

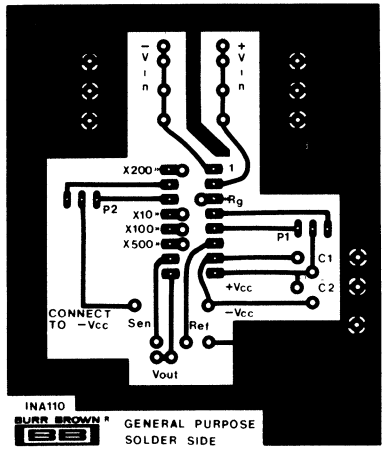


FIGURE 2. Suggested PC Board Layout for INA110.

OFFSET ADJUSTMENT

Figure 3 shows the offset adjustment circuit for the INA110. Both the offset of the input stage and output stage can be adjusted separately. Notice that the offset referred to the INA110's input (RTI) is the offset of the input stage plus the offset of the output stage divided by the gain of the input stage. This allows specification of offset independent of gain.

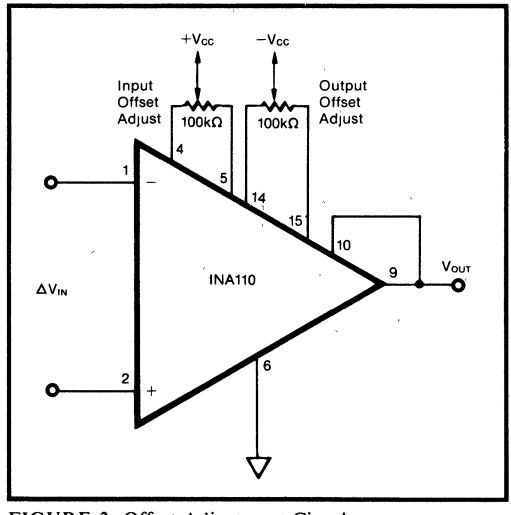


FIGURE 3. Offset Adjustment Circuit.

For systems using computer autozeroing techniques, neither offset nor offset drift are of concern. In many other applications the factory-trimmed offset gives excellent results. When greater accuracy is desired, one adjustment is usually sufficient. In high gains (>100) adjust only the input offset, and in low gains the output

offset. For higher precision in all gains, both can be adjusted by first selecting high gain and adjusting input offset and then low gain and adjusting output offset. The offset adjustment will, however, add to the drift by approximately 0.33μV/°C per 100μV of input offset voltage that is adjusted. Therefore, care should be taken when considering use of adjustment.

Output offsetting can be accomplished as shown in Figure 4 by applying a voltage to the reference (pin 6) through a buffer. This limits the resistance in series with pin 6 to minimize CMR error. Be certain to keep this resistance low. Note that the offset error can be adjusted at this reference point with no appreciable degradation in offset drift.

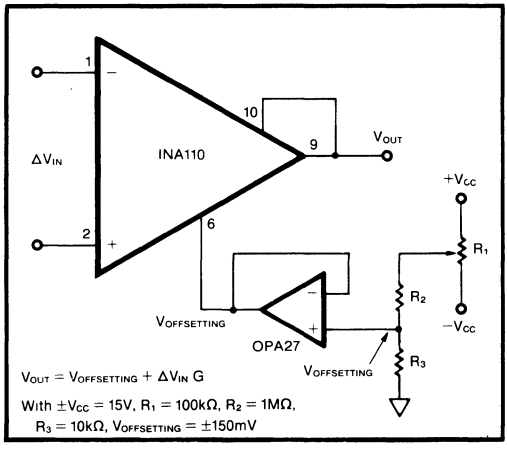


FIGURE 4. Output Offsetting.

GAIN SELECTION

Gain selection is accomplished by strapping the appropriate pins together on the INA110. Table I shows possible gains from the internal resistors. Keep the connections as short as possible to maintain accuracy.

TABLE I. Internal Gain Connections.

Gain	Connect pin 3 to pin —	Gain Accuracy (%)	Gain Drift (ppm/°C)
The following gains have guaranteed accuracy			
1	none	0 02	10
10	13	0 05	10
100	12	0 1	20
200	16	0 2	30
500	11	0 5	50
The following gains have typical accuracy as shown			
300	12 & 16	0 25	10
600	11 & 12	0 25	40
700	11 & 16	2 0	40
800	11, 12, & 16	2 0	80

Gains other than 1, 10, 100, 200, and 500 can be set by adding an external resistor, R_G, between pin 3 and pins 12, 16, and 11. Gain accuracy is a function of R_G and the internal resistors which have a ±20% tolerance with 20ppm/°C drift. The equation for choosing R_G is shown below.

$$R_G = \frac{40k}{G - 1} - 50\Omega$$

Gain can also be changed in the output stage by adding resistance to the feedback loop shown in Figure 5. This is useful for increasing the total gain or reducing the input stage gain to prevent saturation of input amplifiers.

The output gain can be changed as shown in Table II. Matching of R_1 and R_3 is required to maintain high CMR. R_2 sets the gain with no effect on CMR.

TABLE II. Output Stage Gain Control.

Output Stage Gain	R_1 and R_3	R_2
2	1 2kΩ	2 74kΩ
5	1kΩ	511Ω
10	1 5kΩ	340Ω

COMMON-MODE INPUT RANGE

It is important not to exceed the input amplifiers' dynamic range (see Typical Performance Curves). The differential input signal and its associated common-mode voltage should not cause the output of A_1 and A_2 (input amplifiers) to exceed approximately ±10V with ±15V supplies or nonlinear operation will result. Such large common-mode voltages, when the INA110 is in high gain, can cause saturation of the input stage even though the differential input is very small. This can be avoided by reducing the input stage gain and increasing the output stage gain with an H pad attenuator (see Figure 5).

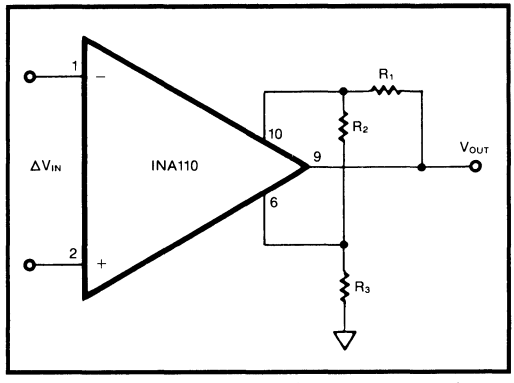


FIGURE 5. Gain Adjustment of Output Stage Using H Pad Attenuator.

OUTPUT SENSE

An output sense has been provided to allow greater accuracy in connecting the load. By attaching this feedback point to the load at the load site, IR drops due to load currents are eliminated since they are inside the feedback loop. Proper connection is shown in Figure 1. When more current is to be supplied, a power booster can be placed within the feedback loop as shown in Figure 6. Buffer errors are minimized by the loop gain of the output amplifier.

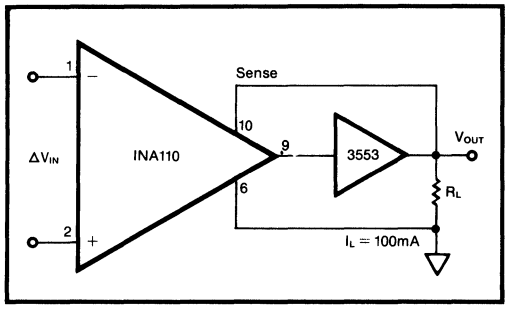


FIGURE 6. Current Boosting the Output.

LOW BIAS CURRENT OF FET INPUT ELIMINATES DC ERRORS

Because the INA110 has FET inputs, bias currents drawn through input source resistors have a negligible effect on DC accuracy. The picoamp levels produce no more than microvolts through megohm sources. Thus, input filtering and input series protection are readily achievable.

A return path for the input bias currents must always be provided to prevent charging of stray capacitance. Otherwise the output can wander and saturate. A 1MΩ to 10MΩ resistor from the input to common will return floating sources such as transformers, thermocouples, and AC-coupled inputs (see Applications section).

DYNAMIC PERFORMANCE

The INA110 is a fast-settling FET input instrumentation amplifier. Therefore, careful attention to minimize stray capacitance is necessary to achieve specified performance. High source resistance will interact with input capacitance to reduce the overall bandwidth. Also, to maintain stability, avoid capacitance from the output to the gain set, offset adjust, and input pins (see Figure 2 for PC board layout).

Applications with balanced-source impedance will provide the best performance. In some applications, mismatched source impedances may be required. If the impedance in the negative input exceeds that in the positive input, stray capacitance from the output will create a net negative feedback and improve the circuit stability. If the impedance in the positive input is greater, the feedback due to stray capacitance will be positive and instability may result. The degree of positive feedback depends upon source impedance imbalance, operating gain, and board layout. The addition of a small bypass capacitor of 5pF to 50pF directly between the inputs of the IA will generally eliminate any positive feedback. CMR errors due to the input impedance mismatch will also be reduced by the capacitor.

The INA110 is designed for fast settling with easy gain selection. It has especially excellent settling in high gain. It can also be used in fast-settling unity-gain applications. As with all such amplifiers, the INA110 does exhibit significant gain peaking when set to a gain of 1. It is, however, unconditionally stable. The gain peaking can be cancelled by band-limiting the negative input to 400kHz with a simple external RC circuit for applications requiring flat response. CMR is not affected by the addition of the 400kHz RC in a gain of 1.

Another distinct advantage of the INA110 is the high frequency CMR response. High frequency noise and sharp common-mode transients will be rejected. To preserve AC CMR, be sure to minimize stray capacitance on the input lines. Matching the RCs in the two inputs will help to maintain high AC CMR.

APPLICATIONS

In addition to general purpose uses, the INA110 is designed to accurately handle two important and demanding applications: (1) inputs with high source impedances such as capacitance/crystal/photodetector sensors and low-pass filters and series-input protection devices, and (2) rapid-scanning data acquisition systems requiring fast settling time. Because the user has access to the output sense, current sources can also be constructed using a minimum of external components. Figures 7 through 24 show application circuits.

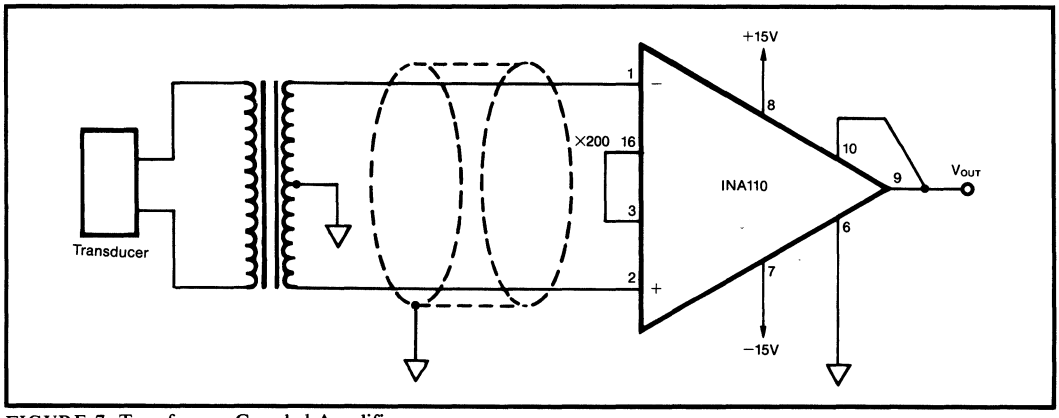


FIGURE 7. Transformer-Coupled Amplifier.

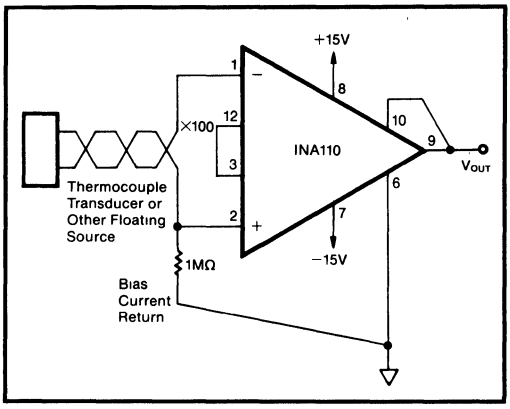


FIGURE 8. Floating Source Instrumentation Amplifier.

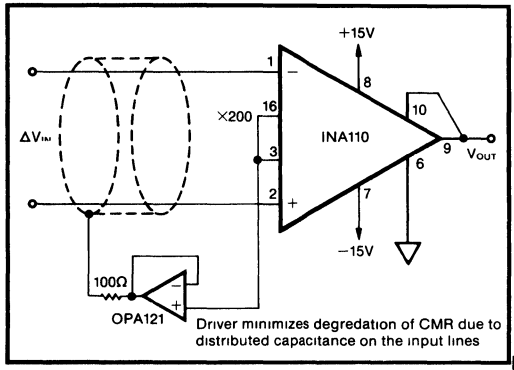


FIGURE 9. Instrumentation Amplifier with Shield Driver.

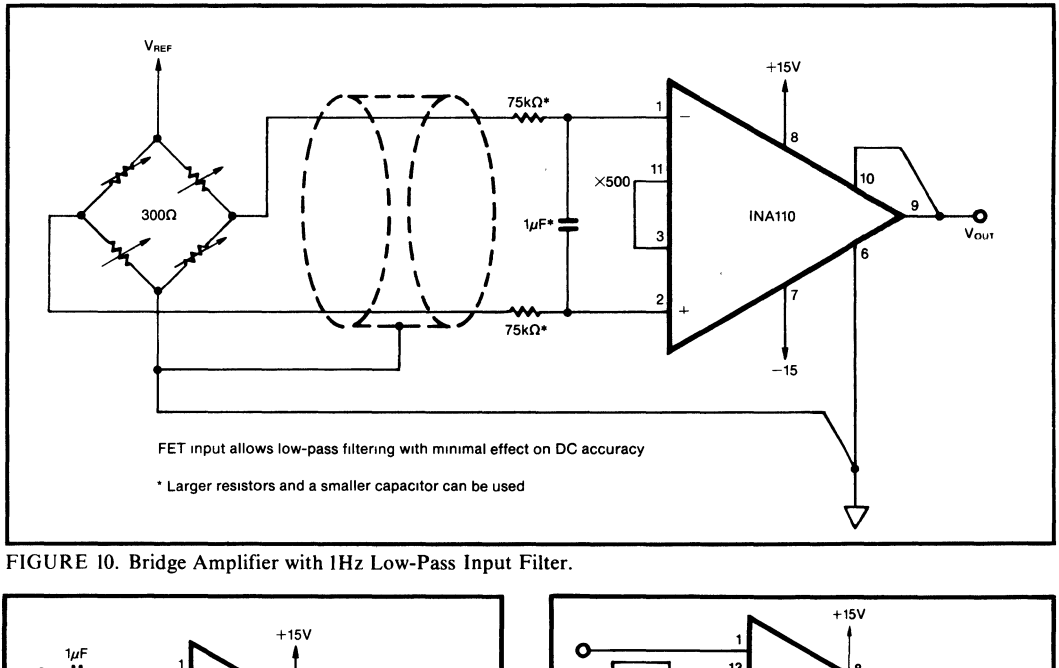


FIGURE 10. Bridge Amplifier with 1Hz Low-Pass Input Filter.

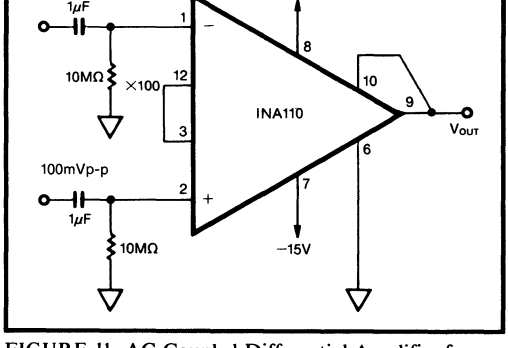


FIGURE 11. AC-Coupled Differential Amplifier for Frequencies Greater Than 0.016Hz.

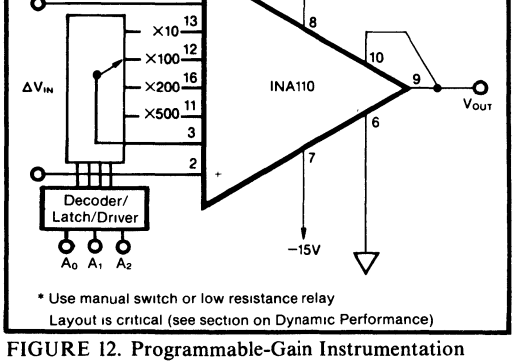


FIGURE 12. Programmable-Gain Instrumentation Amplifier (Precision Noninverting or Inverting Buffer with Gain).

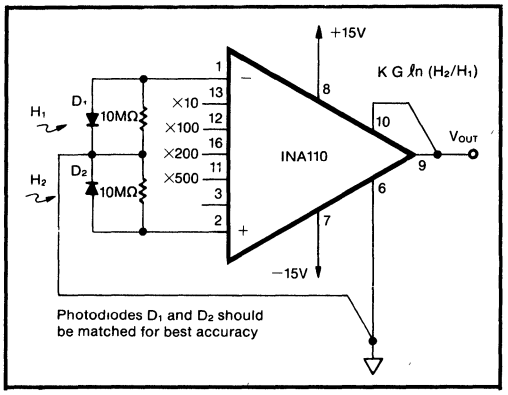


FIGURE 13. Ratiometric Light Amplifier (Absorbance Measurement).

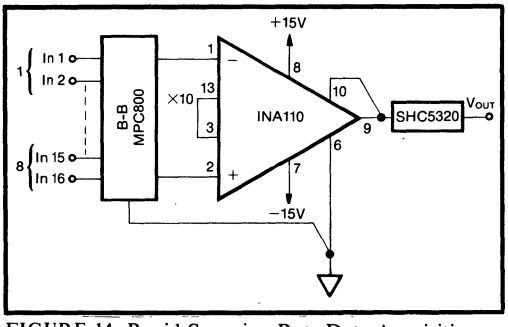


FIGURE 14. Rapid-Scanning-Rate Data Acquisition Channel with 5μs Settling to 0.01%.

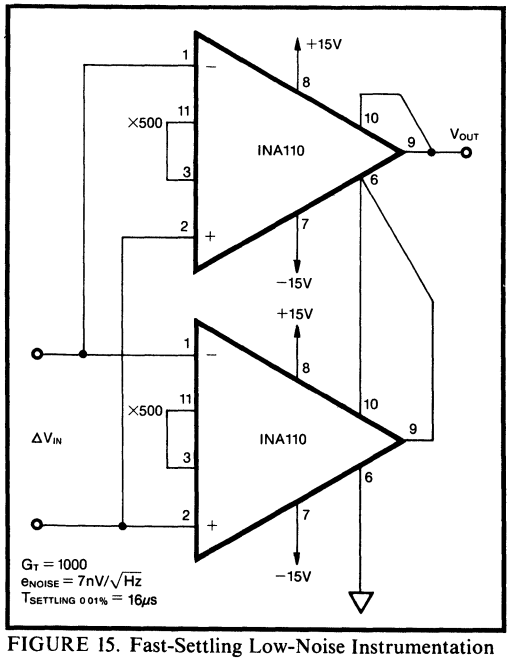


FIGURE 15. Fast-Settling Low-Noise Instrumentation Amplifier with Gain of 1000.

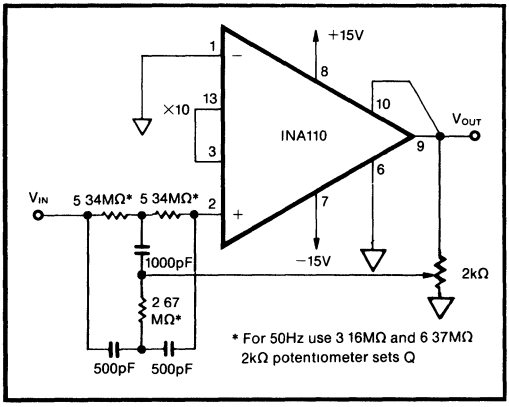


FIGURE 16. Precision Gain-of-10 Amplifier with 60Hz Input Notch Filter.

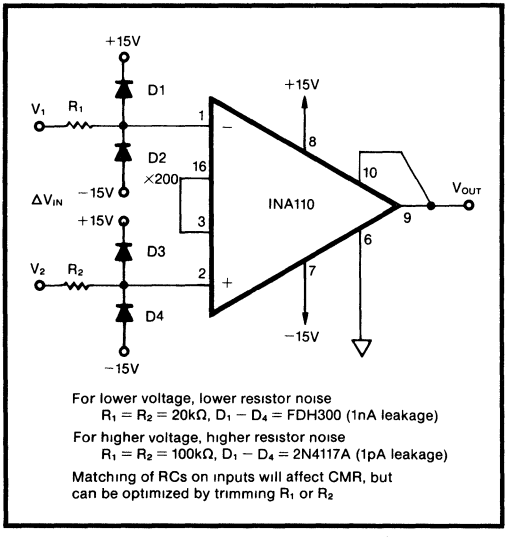


FIGURE 17. Input-Protected Instrumentation Amplifier with Minimal Degradation of DC Accuracy.

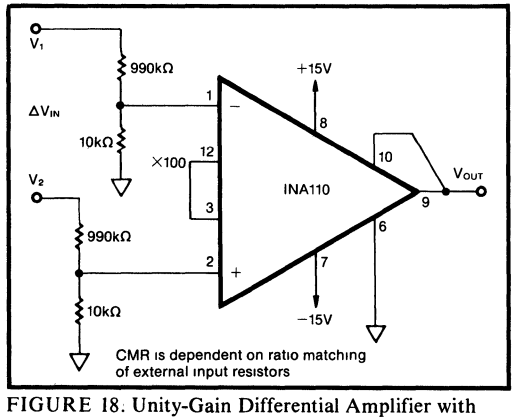


FIGURE 18. Unity-Gain Differential Amplifier with Common-Mode Voltage Range of 1000V.

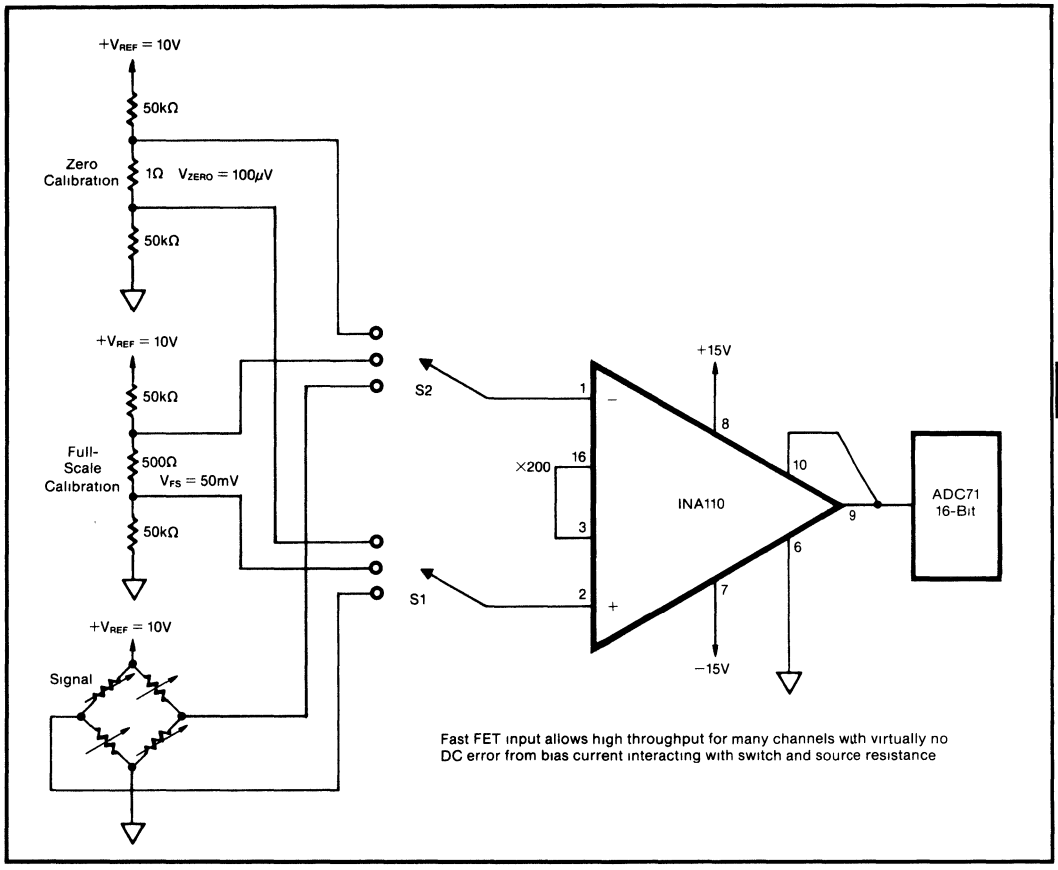


FIGURE 19. Load Cell Weighing Scale Instrumentation Amplifier.

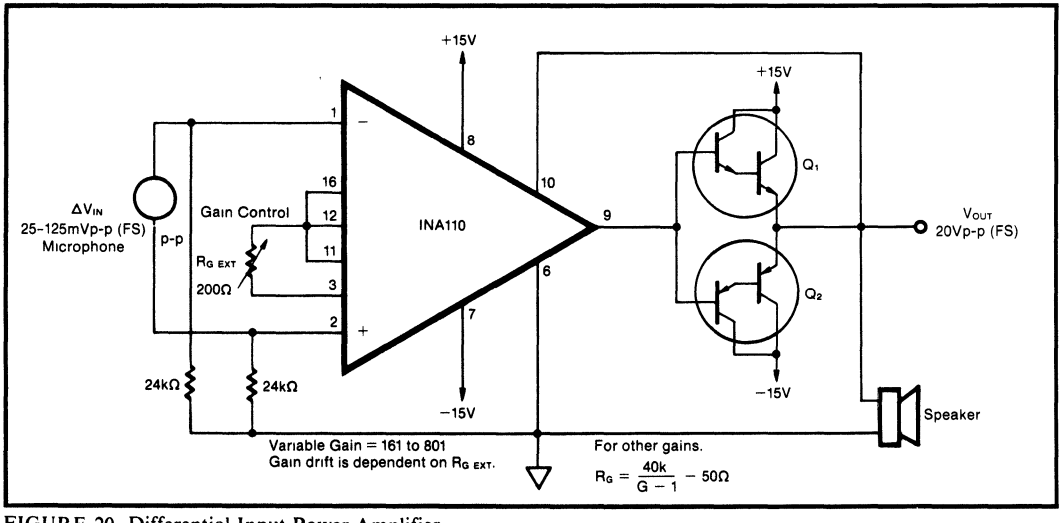


FIGURE 20. Differential Input Power Amplifier.

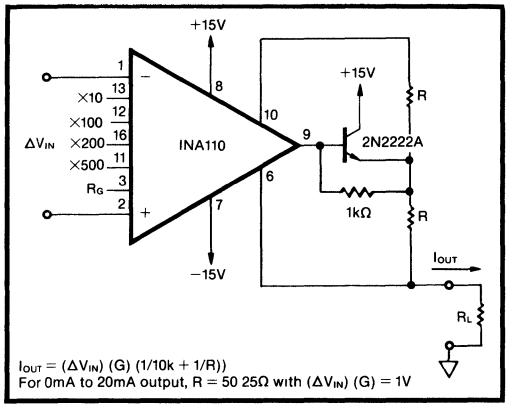


FIGURE 21. Differential Input FET Buffered Current Source.

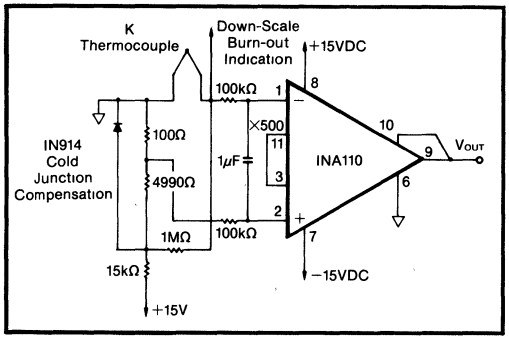


FIGURE 22. Thermocouple Amplifier with Cold Junction Compensation and Input Low-Pass Filtering (< 1Hz).

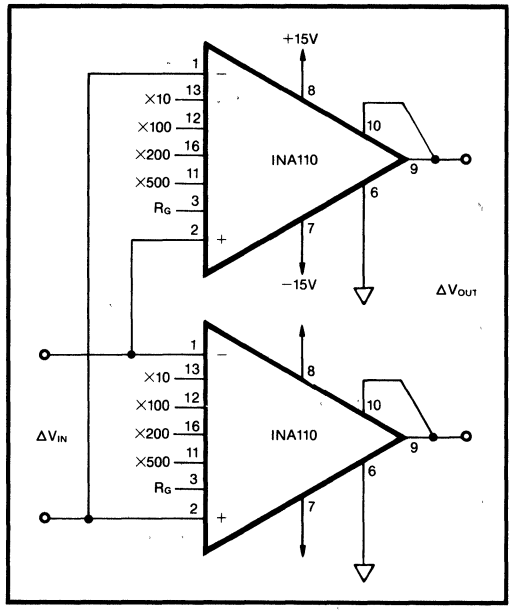


FIGURE 23. Differential Input/Differential Output Amplifier.

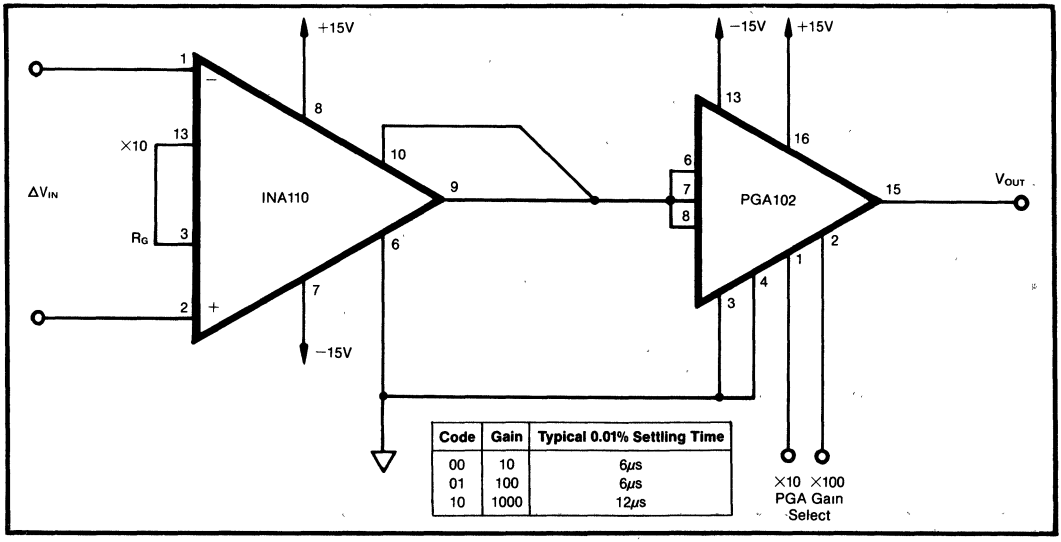
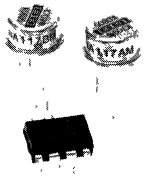


FIGURE 24. Digitally-Controlled Fast-Settling Programmable-Gain Instrumentation Amplifier.

BURR-BROWN®



INA117

AVAILABLE IN DIE FORM

Precision High Common-Mode Voltage Unity-Gain DIFFERENTIAL AMPLIFIER

FEATURES

- HIGH COMMON-MODE RANGE: ±200VDC OR ACpk, continuous
- UNITY GAIN: 0.02% GAIN ERROR, max
- EXCELLENT NONLINEARITY: 0.001% max
- HIGH CMR: 86dB, min
- 8-PIN TO-99 OR PLASTIC DIP
- LOW COST

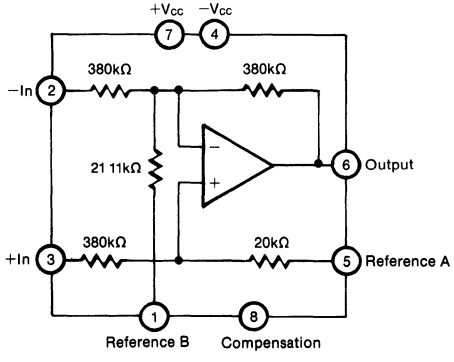
APPLICATIONS

- AC OR DC POWER LINE MONITORING
- TEST EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- GROUND BREAKER
- INDUSTRIAL DATA ACQUISITION SYSTEMS—INPUT BUFFER WITH OVER-VOLTAGE PROTECTION

DESCRIPTION

The INA117 is a precision unity-gain differential amplifier offering an extremely high common-mode input voltage range. As a monolithic circuit, it offers high reliability at low cost. The INA117 consists of a premium operational amplifier with an integrated precision resistor network. In instances where an isolation amplifier is used for its inherent high common-mode capabilities and not for galvanic isolation, the INA117 may be substituted at substantially lower cost. No costly isolation power supply is needed.

The INA117 is completely self-contained and offers the user a highly versatile function. No adjustments to gain, offset or CMR are needed. This provides three important advantages: lower initial design engineering time, lower manufacturing assembly time and cost, and easy, cost-effective field repair of a precision circuit.



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PDS-748B

SPECIFICATIONS

ELECTRICAL

At +25°C, V_{CC} = ±15V unless otherwise noted

PARAMETER	CONDITIONS	INA117AM			INA117BM			INA117P			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Initial[1]			1			*			*		V/V
Error			0 01	0 05		*	0 02		*	*	%
vs Temperature			2	10			*		*		ppm/°C
Nonlinearity[2]			0 0002	0 001		*	*		*	*	%
OUTPUT											
Rated Voltage	I_O = +20mA, −5mA	10 0	12		*	*		*	*		V
Rated Current	E_O = 10V	+20, −5			*			*			mA
Impedance			0 01			*			*		Ω
Current Limit	To common		+49,								
			−13			*			*		mA
Capacitive Load	Stable operation		1000			*			*		pF
INPUT											
Impedance	Differential		800			*			*		kΩ
	Common-mode		400			*			*		kΩ
Voltage Range	Differential	±10				*			*		V
	Common-mode, continuous	±200			*			*			VDC, ACpk
Common-mode Rejection[3]		70	80		86	94		*	*		dB
vs Temperature DC	$T_A = T_{MIN}$ to T_{MAX}	66	75		80	90			*		dB
AC, 60Hz		66	80		*	94			*		dB
OFFSET VOLTAGE	RTO[4]										
Initial			120	1000		*	1000		*	*	μV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		8 5	40		*	20		*		μV/°C
vs Supply	±V_{CC} = 5V to 18V	74	90		80	*		*	*		dB
vs Time			200			*			*		μV/mo
OUTPUT NOISE VOLTAGE	RTO[5]										
F_B = 0 01Hz to 10Hz			25			*			*		μVp-p
F_O = 10kHz			550			*			*		nV/√Hz
DYNAMIC RESPONSE											
Gain Bandwidth	−3dB		200			*			*		kHz
Full Power Bandwidth	V_O = 20Vp-p	30			*			*			kHz
Slew Rate		2	2 6		*	*		*	*		V/μs
Settling Time 0 1%	V_O = 10V step		6 5			*			*		μs
0 01%	V_O = 10V step		10			*			*		μs
0 01%	V_{CM} = 10V step, V_{DIFF} = 0V		4 5			*			*		μs
POWER SUPPLY											
Rated			±15			*			*		V
Voltage Range	Derated performance	±5		±18	*		*	*		*	V
Quiescent Current	V_{OUT} = 0V		1 5	2 0		*	*		*	*	mA
TEMPERATURE RANGE											
Specification		−25		+85	*		*	0		+70	°C
Operation		−55		+125	*		*	−25		+85	°C
Storage		−65		+150	*		*	−40		+85	°C

*Specification same as for INA117AM

NOTES (1) Connected as difference amplifier (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output (3) With zero source impedance (see Offset and CMR section) (4) Includes effects of amplifier's input bias and offset currents (5) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network

ORDERING INFORMATION

Model	Package	Temperature Range
INA117AM	Metal TO-99	-25°C to +85°C
INA117BM	Metal TO-99	-25°C to +85°C
INA117KP	Plastic DIP	0°C to +70°C

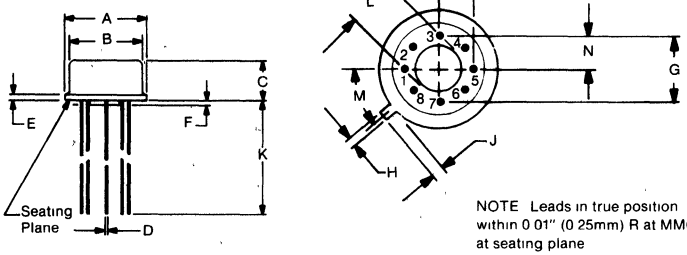
BURN-IN SCREENING OPTION
See text for details

Model	Package	Burn-In Temp. (160h)[1]
INA117AM-BI	Metal TO-99	+125°C
INA117BM-BI	Metal TO-99	+125°C
INA117KP-BI	Plastic DIP	+85°C

NOTE. (1) Or equivalent combination. See text

MECHANICAL

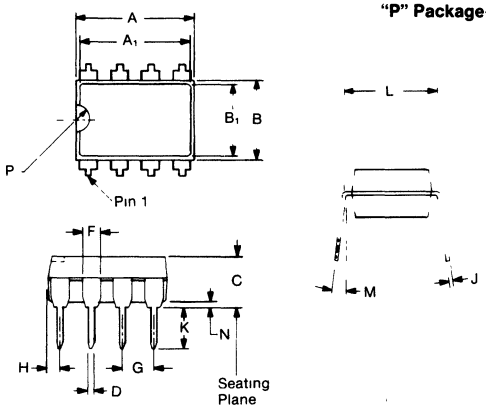
TO-99 Package



NOTE Leads in true position within 0 01" (0 25mm) R at MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	335	370	8 51	9 40
B	305	335	7 75	8 51
C	165	185	4 19	4 70
D	016	021	0 41	0 53
E	010	040	0 25	1.02
F	010	040	0 25	1 02
G	200 BASIC		5.08 BASIC	
H	028	034	0 71	0 86
J	029	045	0 74	1 14
K	500	—	12 7	—
L	110	160	2 79	4 06
M	45° BASIC		45° BASIC	
N	095	105	2 41	2 67

"P" Package—Plastic DIP

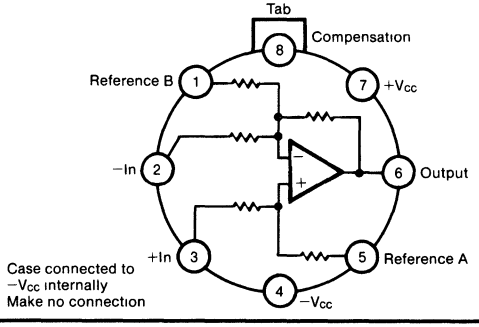


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	355	400	9 02	10 16
A_1	340	385	8 64	9 78
B	230	290	5 84	7 37
B_1	200	250	5 08	6 35
C	120	200	3 05	5 08
D	015	023	0 38	0 58
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	025	050	0 64	1 27
J	008	015	0 20	0 38
K	070	150	1 78	3 81
L	300 BASIC		7 63 BASIC	
M	0°	15°	0°	15°
N	010	030	0 25	0 76
P	025	050	0 64	1 27

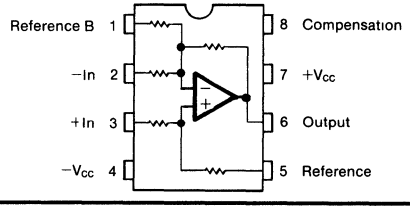
NOTE Leads in true position within 0 01" (0 25mm) R at MMC at seating plane Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3 2)

PIN DESIGNATIONS

Top View **Metal TO-99—INA117AM, BM**



Top View **Plastic DIP—INA117P**



ABSOLUTE MAXIMUM RATINGS

Supply	±22V
Input Voltage Range (Common & Differential)	
Continuous	±200V
Momentary, 10s	±500V
Operating Temperature Range M	−55°C to +125°C
P	−25°C to +85°C
Storage Temperature Range M	−65°C to +125°C
P	−40°C to +85°C
Lead Temperature (soldering 10s)	+300°C
Output Short Circuit to Common	Continuous

BURN-IN SCREENING

Burn-in screening is an option available for both the plastic- and ceramic-packaged INA117. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

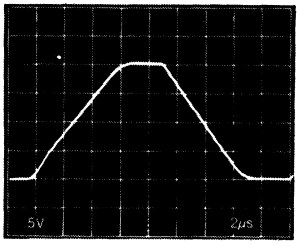
Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

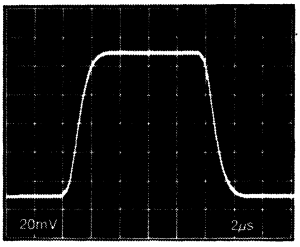
TYPICAL PERFORMANCE CURVES

T_A = +25°C, $\pm V_{CC}$ = 15V unless otherwise noted

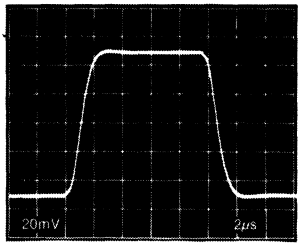
STEP RESPONSE
No Load



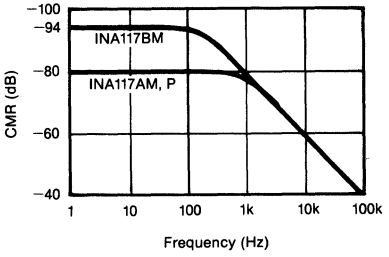
SMALL SIGNAL RESPONSE
No Load



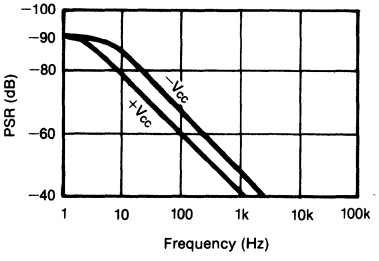
SMALL SIGNAL RESPONSE
$R_L = \infty$, C_L = 1000pF



COMMON-MODE REJECTION
VS FREQUENCY



POWER-SUPPLY REJECTION
VS FREQUENCY



DISCUSSION OF SPECIFICATIONS

Refer to Figure 1. Resistor networks at the amplifier input divide the input voltages down to levels suitable for the operational amplifier's common-mode and differential signal capabilities. Feedback around the operational amplifier then restores overall circuit gain to unity for differential signals, while preserving high common-mode rejection.

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 also shows the proper connections for power supply and signal. Supplies should be decoupled with 1μF tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance.

OFFSET AND COMMON-MODE REJECTION

Two factors are important in maintaining high CMR: resistor matching and tracking (already trimmed in the INA117 for the user) and source impedance.

CMR depends on the accurate matching of several resistor ratios. High accuracies needed to maintain the specified CMR and CMR temperature coefficient are difficult and expensive to reliably achieve with discrete components.

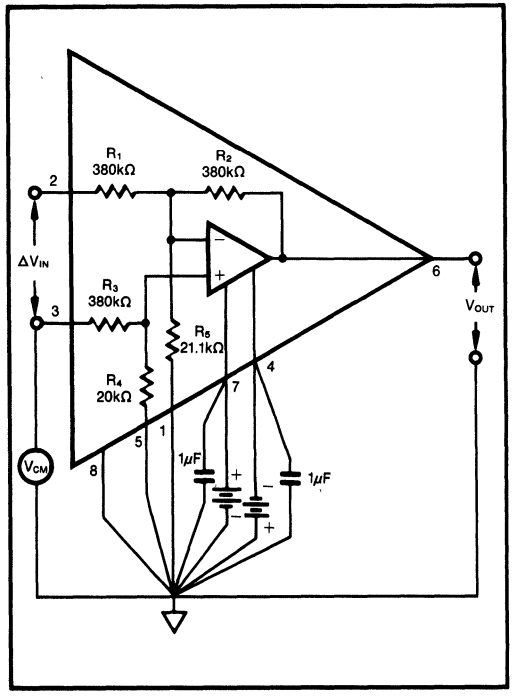


FIGURE 1. Basic Power Supply and Signal Connections.

Any external resistance imbalance adds directly to these resistor ratios. These imbalances can occur either directly in series with R_1 or R_3 or in series with R_4 or R_5. For example, 4Ω added in series with pin 1 or 76Ω in series with pin 2 will degrade CMR from 86dB to 72dB.

When input filters are used preceding an instrumentation amplifier, care should also be taken to match RCs on the two input lines. For example, mismatched input filters for high frequencies will reduce the CMR at lower frequencies, e.g., 60Hz. Differential filters will not degrade AC CMR.

Figures 2a, b, and c show circuitry to allow trim of both CMR and DC offset. Use of these circuits will affect gain accuracy slightly.

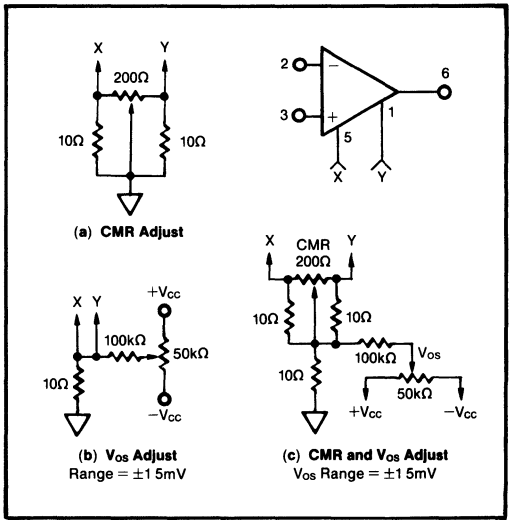


FIGURE 2. CMR and V_{OS} Adjustment.

RESISTOR NOISE IN THE INA117

Figure 3 shows the model for calculating resistor noise in the INA117. Resistors have Johnson noise resulting from thermal agitation. The expression for this noise is:

$$E_{rms} = \sqrt{2\pi KTRB}$$

Where: K = Boltzman's constant (J/°K)
T = Absolute temperature (°K)
R = Resistance (Ω)
B = Bandwidth (Hz)

At room temperature, this noise becomes:

$$E_N = 1.3 \times 10^{-10} \sqrt{R} \quad (V/\sqrt{Hz})$$

The two noise sources in Figure 3 are:

$$E_{N1} = 1.3 \times 10^{-10} \sqrt{R_5} \quad (V/\sqrt{Hz})$$
$$E_{N2} = 1.3 \times 10^{-10} \sqrt{R_4} \quad (V/\sqrt{Hz})$$

Referred to output,

$$E_{NO1} = E_{N1} (R_2/R_5)$$
$$E_{NO2} = E_{N2} [(R_2/R_1 \parallel R_5) + 1]$$

Adding as the root of the sums squared:

$$E_{NO} = \sqrt{E_{NO1}^2 + E_{NO2}^2} \quad (V/\sqrt{Hz})$$

E_{NO} at a 200kHz bandwidth
= 0.27mVrms
= 1.6mVp-p with a crest factor of 6
(statistically includes 99.7% of all noise peak occurrences)

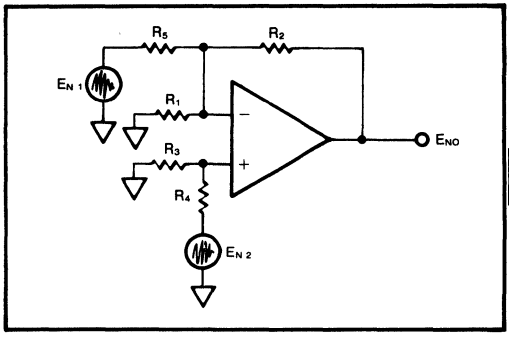


FIGURE 3. Resistor Noise Model.

APPLICATIONS CIRCUITS

The INA117 is ideally suited for a wide range of circuit functions. The following figures show many applications circuits.

BATTERY CELL MONITOR

Batteries are often charged in series. The INA117 is ideal for directly monitoring the condition of each cell. Operating range is up to ±200V, and differential fault conditions in this range will not damage the amplifier. Since the INA117 requires no isolated front-end power, cost per cell is very low.

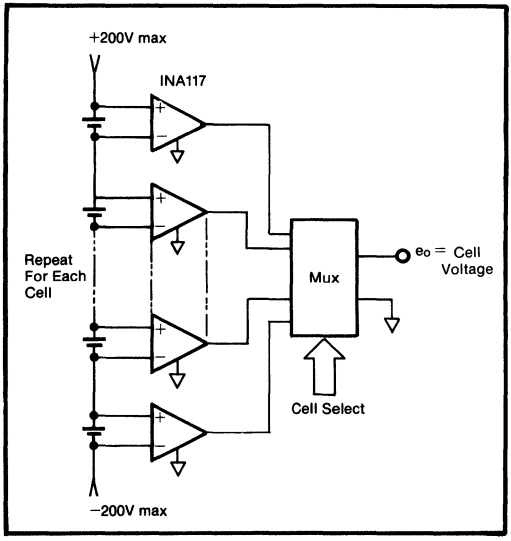


FIGURE 4. Battery Cell Monitor.

BRIDGE AMPLIFIER LOAD CURRENT MONITOR

Bridge amplifiers are popular because they double the voltage swing possible across the load with any given power supply. In this circuit A_1 and A_2 form a bridge amplifier driving a load. A_1 is connected as a follower and A_2 as an inverter.

At low frequencies, a sense resistor could be inserted in series with the load and an instrumentation amplifier used to directly monitor the load current. Under high frequency or transient conditions, CMR errors limit the accuracy of this approach. An alternate approach is to measure the power amplifier supply currents. To understand how it works, notice that since essentially no current flows in the amplifier inputs, $I_{LOAD} = I_1 - I_2$.

A_3 and A_4 are INA117s used to monitor A_1 supply currents I_1 and I_2 across sense resistors R_1 and R_2. Since the INA117 has a ±200V CMV range, the inputs (pins 2 and 3) can be tied to $\pm V_{CC}$ as long as the differential input is less than 10V.

If $R_1 = R_2 = R$
then $e_1 = I_1 \times R$
$e_2 = -I_2 \times R$
and $e_1 + e_2 = I_{LOAD} \times R$

A_5 is an INA105 difference amplifier connected as a noninverting summing amplifier with a gain of 5. The accurate matching of the two 25kΩ input resistors makes a very accurate summing amplifier.

$e_O = 5\,(e_1 + e_2) = 5\,(I_{LOAD} \times R)$
since $R = 0.2\Omega$
$e_O = I_{LOAD}$ (1V/A)

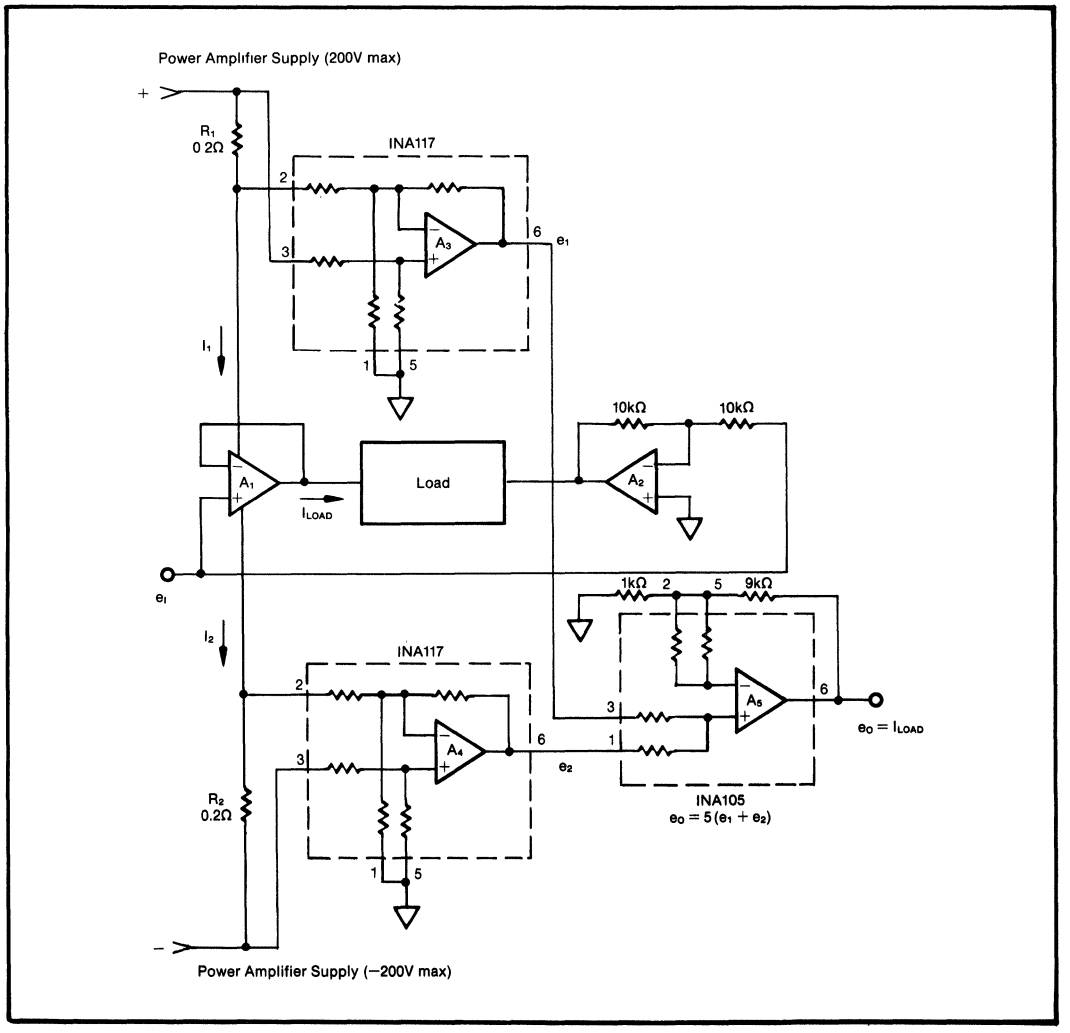


FIGURE 5. Bridge Amplifier Load Current Monitor.

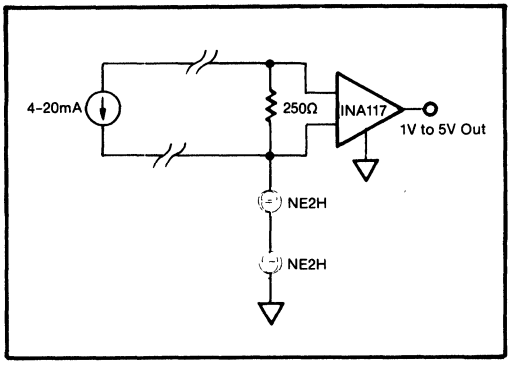


FIGURE 6. 4–20mA Current Receiver.

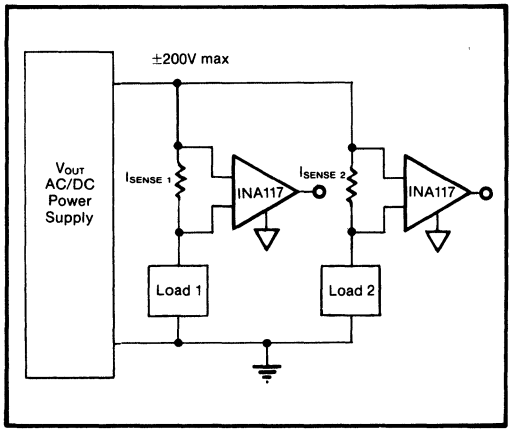


FIGURE 7. Power Supply Current Monitor.

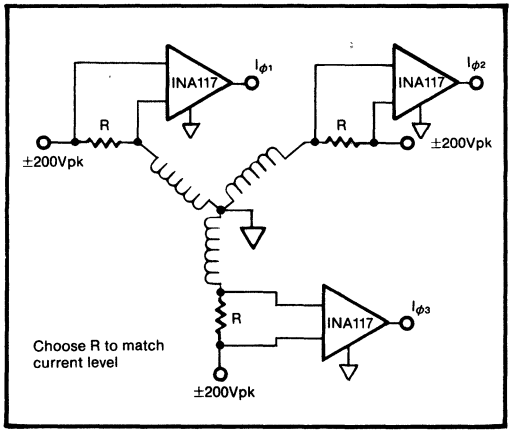


FIGURE 8. Three-Phase Current Monitor.

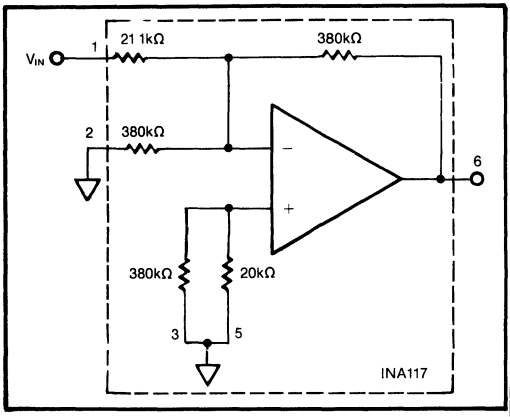


FIGURE 9. Inverting Amplifier, Gain = 18.

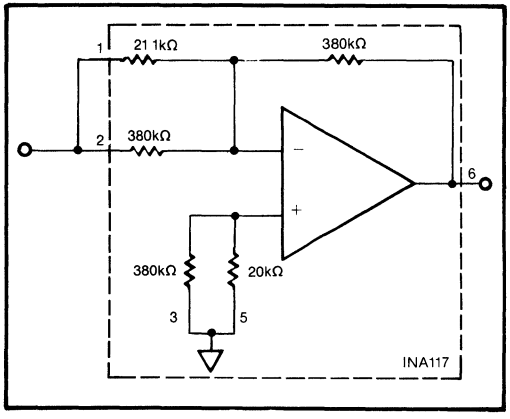


FIGURE 10. Inverting Amplifier, Gain = 19.

LEAKAGE CURRENT TEST MONITOR

When the return path is not independently available, leakage current must be measured in series with the input. When the 400kΩ input impedance of the INA117 is too low, a buffer amplifier may be added to the front end. In this example, an OPA128 electrometer-grade operational amplifier is used. The 1kΩ and 9kΩ feedback resistors set a noninverting gain of 10. Bias current of the amplifier is less than 75fA. The diodes and 100kΩ resistor protect the amplifier from 200V short circuit fault conditions.

Since common-mode rejection is the ratio of common-mode gain to differential gain, CMR is boosted. The 20dB gain of the OPA128 added to the 86dB CMR of the INA117 results in a total CMR of 106dB minimum.

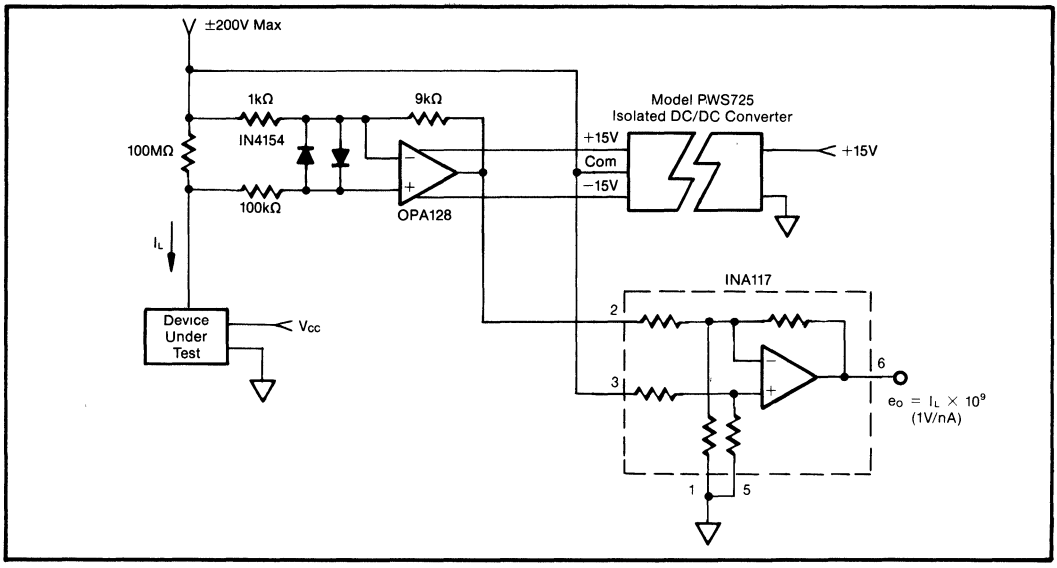


FIGURE 11. Leakage Current Monitor.

MAINTAINING GAIN ACCURACY AND CMR IN I_{SENSE} APPLICATIONS

Figure 12 shows the INA117 used as a transimpedance device, i.e.,

$$V_{OUT} / I_I = 1 \text{ gm}$$

To calculate a value for R_S and R_{COMP}:

$$R_S = R_{COMP} = \frac{(1 \text{ gm})\ 380k}{380k - (1 \text{ gm})}$$

Example:

For 1V out per 4mA of I_I

$$1 \text{ gm} = 1V / 4mA = 250$$

$$R_S = R_{COMP} = 250\ (380k)/380k - 250 = 250.165$$

For $R_S \leq 380\Omega$, Maximum Error = 0.02%.

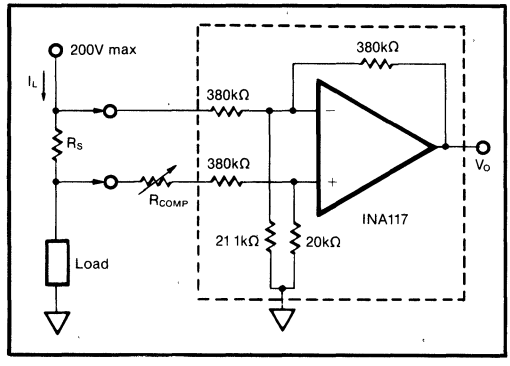
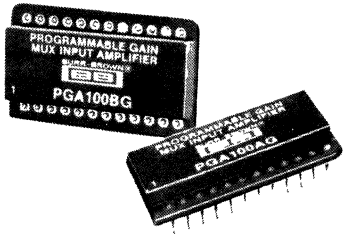


FIGURE 12. Using the INA117 as a Transimpedance Device.

BURR-BROWN®



PGA100

Digitally-Controlled Programmable Gain/Multiplexed Input OPERATIONAL AMPLIFIER

FEATURES

- HIGH GAIN ACCURACY, ±0.02%, max (B grade)
- LOW NONLINEARITY, ±0.005%, max (B grade)
- FAST SETTLING, 5μsec to 0.01%
- LOW CHANNEL-TO-CHANNEL CROSSTALK, ±0.003%
- INPUT PROTECTION, ±20V, max above $\pm V_{CC}$
- 8 ANALOG INPUT CHANNELS WITH HIGH Z_{IN}, $10^{11}\Omega$
- 8 BINARY GAINS 1, 2, 4, 8, 16, 32, 64, 128 (V/V)
- FULLY MICROPROCESSOR-COMPATIBLE

APPLICATIONS

- DATA ACQUISITION SYSTEM AMPLIFIER
- SOFTWARE ERROR CORRECTION
- AUTO-ZEROING CAPABILITY
- DIGITALLY-CONTROLLED AUTORANGING SYSTEM
- TEST EQUIPMENT
- REMOTE INSTRUMENTATION SYSTEM
- SYSTEM DYNAMIC RANGE AND RESOLUTION IMPROVEMENT

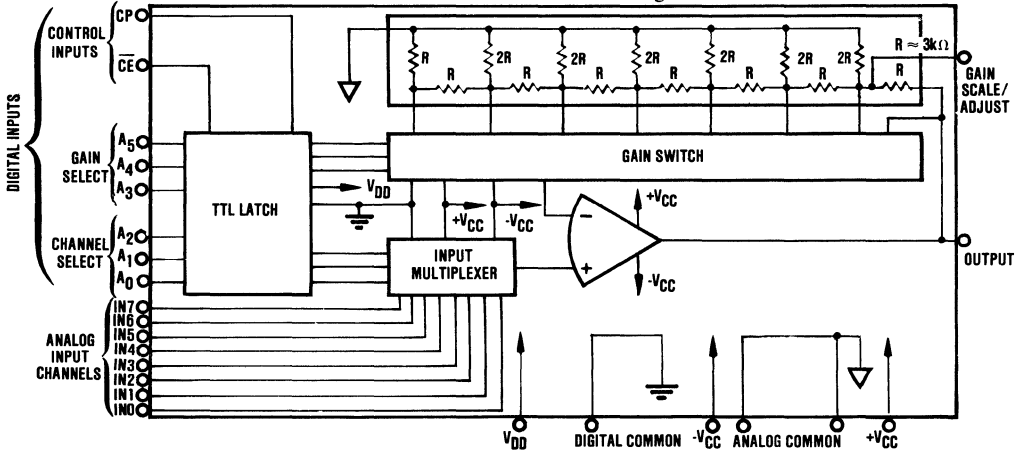
DESCRIPTION

The PGA100 is a precision, digitally-programmable-gain multiplexed-input amplifier. The user can select any one of eight analog input channels simultaneously with any one of eight noninverting binarily weighted gain steps from 1 to 128 (V/V). The digital gain and channel select are latchable for microprocessor interface. Also, the fast 5μsec settling time is ideal for rapid channel scanning in data acquisition systems.

Precision laser-trimming of both offset voltage and gain accuracy, with good temperature tracking of feedback resistor ratios, permits direct use without adjustments. However, hardware or software correction of errors is readily achievable.

In addition, gain scaling to gains other than 1 to 128V/V can easily be accomplished.

Microcircuit construction and the use of laser-trimmed thin-film feedback resistors achieve high accuracy, small size, and low cost not obtained with discrete designs.



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PDS-457B

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C, ±V_{CC} = 15VDC, V_{DD} = +5VDC unless otherwise noted.

PARAMETER	CONDITIONS	PGA100AG			PGA100BG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
GAIN, G								
Inaccuracy(1)	G = 1 to 128, I_O = 1mA		±0.01	±0.05		±0 005	±0 02	%
vs Temperature(2)	-25°C ≤ T_A ≤ +85°C		±5	±10		*	*	ppm/°C
vs Time			±0 001			*		%/1000 hrs
Nonlinearity(3)	G = 1 to 128, I_O = 1mA		±0 004	±0 01		±0 002	±0 005	% of FS
vs Temperature(2)	-25°C ≤ T_A ≤ +85°C		±2	±5		*	*	ppm/°C
vs Time			±0.001			*		%/1000 hrs.
Warm-up Time		1			*			min
RATED OUTPUT								
Voltage	I_O = ±2mA	±10			*			V
Current	V_O = ±10V	±2			*			mA
Output Resistance	G ≤ 128		0.05			*		Ω
Short Circuit Current			±15			*		mA
Capacitive Load Range	Phase Margin ≥ 25°		1000			*		pF
INPUT OFFSET VOLTAGE								
Initial	T_A = +25°C		±0 1	±1		±0 05	±0.5	mV
vs Temperature	-25°C ≤ T_A ≤ +85°C		±6			*		µV/°C
vs Supply Voltage	±8VDC ≤ | V_{CC} | ≤ ±18VDC		±10	±80		*	*	µV/V
vs Time			±15			*		µV/mo.
INPUT BIAS CURRENT								
Initial	T_A = +25°C							
"OFF" Channel			±10			*		pA
"ON" Channel			±0.1			*	±1	nA
vs Temperature			Note 4			*		
INPUT DIFFERENCE CURRENT, BETWEEN CHANNELS								
Initial	T_A = +25°C							
"OFF" Channel			±20			*		pA
"ON" Channel			±0.2			*	±2	nA
vs Temperature			Note 4			*		
ANALOG INPUT CHARACTERISTICS								
Absolute Max Voltage	No damage			±(|Vcc|+20)			*	V
Input Voltage Range	Linear operation	±10			*			V
Input Impedance								
"OFF" Channel			10^{12} ‖ 5			*		Ω ‖ pF
"ON" Channel			10^{11} ‖ 25			*		Ω ‖ pF
INPUT NOISE								
Voltage Noise Density	f_O = 1Hz		200			*		nV/√Hz
	f_O = 10Hz		60			*		nV/√Hz
	f_O = 100Hz		25			*		nV/√Hz
	f_O = 1kHz		18			*		nV/√Hz
	f_O = 10kHz		18			*		nV/√Hz
	f_O = 100kHz		18			*		nV/√Hz
Voltage Noise	f_B = 0.1Hz to 10Hz		2.6			*		µV, p-p
Current Noise Density	f_O = 0.1Hz thru 8kHz		6			*		fA/√Hz
Current Noise	f_B = 0 1Hz to 10Hz		115			*		fA, p-p
DYNAMIC RESPONSE								
Gain Bandwidth Product			5			*		MHz
Full Power Bandwidth	G = .1, V_O = 20V, p-p, R_L = 5kΩ		220		80	*		kHz
Slew Rate	G = 1, V_O = ±10V, R_L = 5kΩ		14		5	*		V/µsec
Settling Time(5)	G = 1, V_O = ±10V, R_L = 5kΩ							
ε = 1%			2 5			*		µsec
ε = 0 1%			3			*		µsec
ε = 0.01%			5			*		µsec
Rise Time	10% to 90%, small signal		70			*		nsec
Phase Margin	G = 1, R_L = 5kΩ		60			*		Degrees
Overload Recovery (6)	G = 1, 50% overdrive		2			*		µsec
Crosstalk, RTI(5)(7)	20V, p-p, 1kHz sine, R_S = 1kΩ on all OFF channels		±0.003			*		%
DIGITAL INPUT(8)								
Input "Low" Threshold, V_{IL}				0 8			*	V
Input "High" Threshold, V_{IH}		2 0			*			V
f_{max}, Maximum Clock Frequency		30			*			MHz
t_{WL}, Clock Pulse Width (Low)	Figure 1	20			*			nsec
t_{s_1}, Setup Time (Data to CP)	Figure 1	20			*			nsec
t_{h_1}, Hold Time (Data to CP)	Figure 1	5			*			nsec
t_{s_2}, Setup Time ($\overline{CE}$ to CP)	Figure 1	25			*			nsec
t_{h_2}, Hold Time ($\overline{CE}$ to CP)	Figure 1	5			*			nsec

ELECTRICAL (CONT)

PARAMETER	CONDITIONS	PGA100AG MIN	PGA100AG TYP	PGA100AG MAX	PGA100BG MIN	PGA100BG TYP	PGA100BG MAX	UNITS
ANALOG SUPPLY								
Rated Voltage			±15			•	•	VDC
Voltage Range	Derated performance	±8		±18	•			V
Positive Quiescent Current			+20	+27		-15	+20	mA
Negative Quiescent Current			-10	-16		-7.5	-12	mA
DIGITAL SUPPLY								
Rated Voltage			+5			•	•	VDC
Voltage Range		+4 75		+5 25	•		•	V
Quiescent Current	V_{DD} = +5 25V		15	27		•	•	mA
TEMPERATURE RANGE								
Specification		-25		+85	•		•	°C
Operating	Derated performance	-55		+125	•		•	°C
Storage		-55		+125	•		•	°C

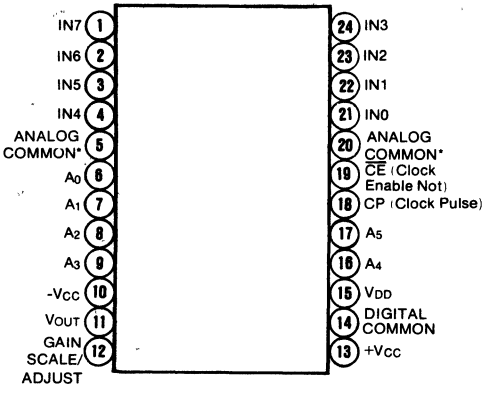
*Specifications same as PGA100AG

NOTES
1 Inaccuracy is the percent error between the actual and ideal gain selected It may be externally adjusted to zero
2 Parameter is untested and is not guaranteed This specification is established to a 90% confidence level
3 Nonlinearity is the maximum peak deviation from a "best straight line" (curve fitting on input-output graph) expressed as a percent of the full scale peak-to-peak output Gain constant, V_{OUT} ranges from -10V to +10V
4 Doubles approximately every 10°C
5 See Typical Performance Curves
6 Time required for the output to return from saturation to linear operation following the removal of an input overdrive signal
7 Crosstalk is the amount of signal feedthrough from all OFF channels that appears at the output of the input multiplexer It is expressed as a percent of the signal applied to all OFF channels
8 All digital inputs are one 74LSTTL load

ABSOLUTE MAXIMUM RATINGS

Analog Supply	±18V
Digital Supply	+7V
Input Voltage Range, Analog	±(|V_{CC}| +20)V
Input Voltage Range, Digital	+7V
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering 10 seconds)	300°C
Output Short-circuit Duration	Continuous to ground
Junction Temperature	175°C

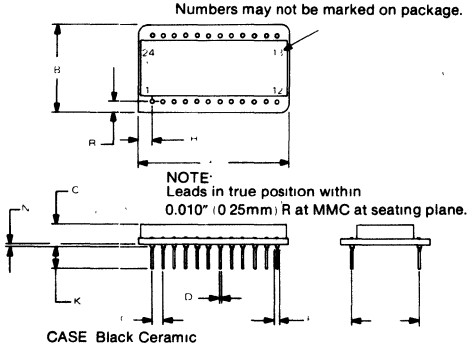
PIN DESIGNATIONS



*Connected internally, Use pin 20 as the primary analog common.

MECHANICAL

Pin numbers shown for reference only
Numbers may not be marked on package.



CASE Black Ceramic
MATING CONNECTOR 245MC
PIN Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3 2)
WEIGHT 6 3 grams (0 225 oz.)
HERMETICITY: Conform to method 1014 Condition C Step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1 310	1 360	33 27	34 54
B	770	810	19 56	20 57
C	150	210	3 81	5 33
D	018	021	0 46	0 53
F	035	050	0 89	1 27
G	100 BASIC		2 54 BASIC	
H	110	130	2 79	3 30
K	150	250	3 81	6 35
L	600 BASIC		15 24 BASIC	
N	002	010	0 05	0 25
R	085	105	2 16	2 67

ORDERING INFORMATION

Model	Package	Temperature Range
PGA100AG	Ceramic	-25°C to +85°C
PGA100BG	Ceramic	-25°C to +85°C

BURN-IN SCREENING OPTION
See text for details

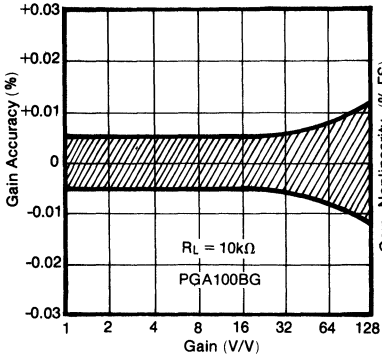
Model	Package	Burn-In Temp. (160h)[1]
PGA100AG-BI	Ceramic	+125°C
PGA100BG-BI	Ceramic	+125°C

NOTE: (1) Or equivalent combination See text

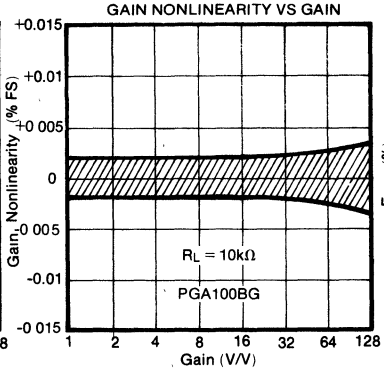
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, ±V_{CC} = 15VDC, V_{DD} = +5VDC, unless otherwise noted.)

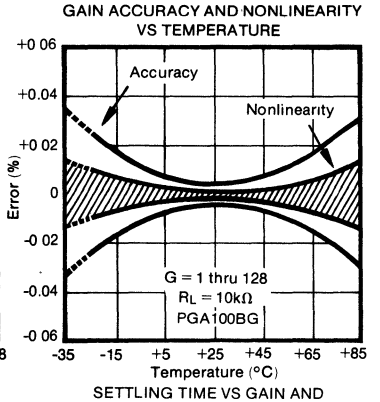
GAIN ACCURACY VS GAIN



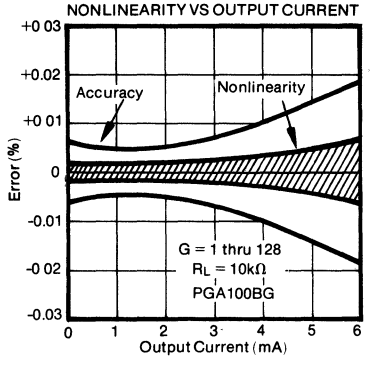
GAIN NONLINEARITY VS GAIN



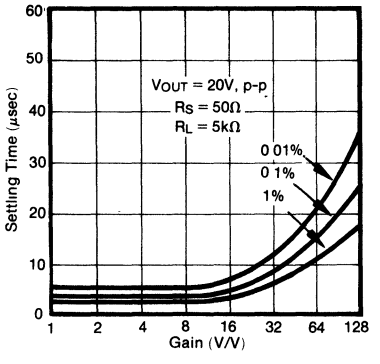
GAIN ACCURACY AND NONLINEARITY VS TEMPERATURE



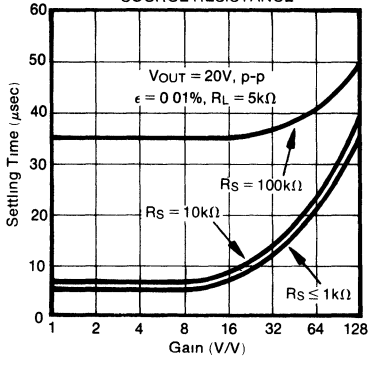
GAIN ACCURACY AND NONLINEARITY VS OUTPUT CURRENT



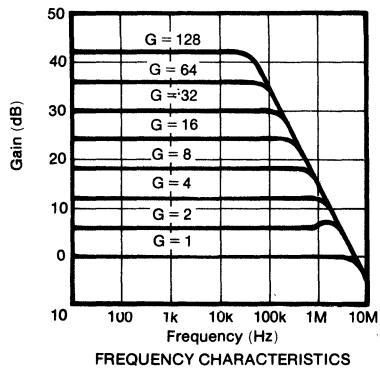
SETTLING TIME VS GAIN



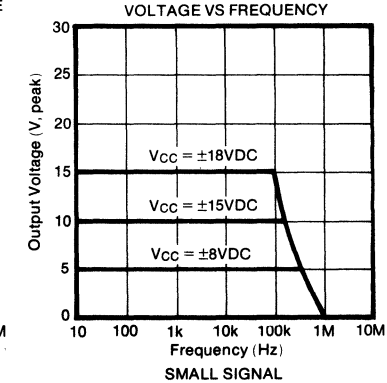
SETTLING TIME VS GAIN AND SOURCE RESISTANCE



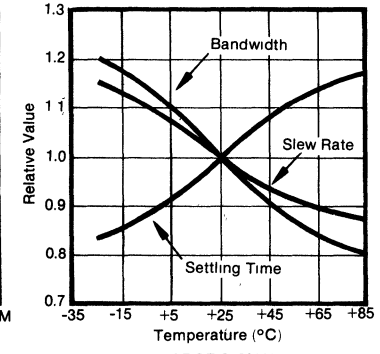
SMALL SIGNAL FREQUENCY RESPONSE



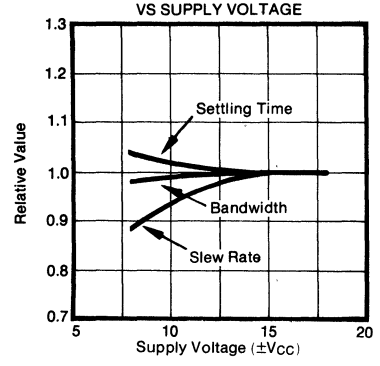
LARGE SIGNAL OUTPUT VOLTAGE VS FREQUENCY



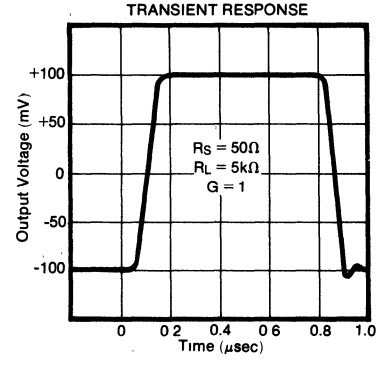
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



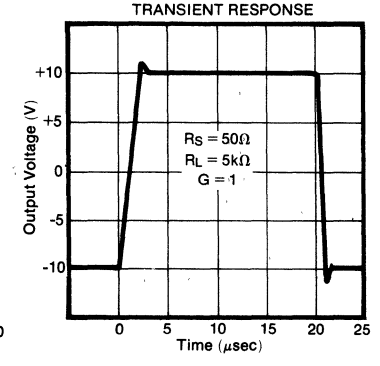
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



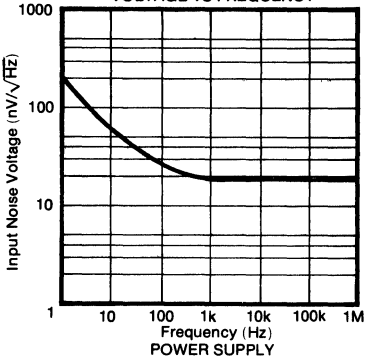
SMALL SIGNAL TRANSIENT RESPONSE



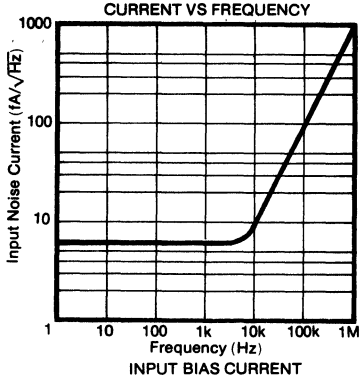
LARGE SIGNAL TRANSIENT RESPONSE



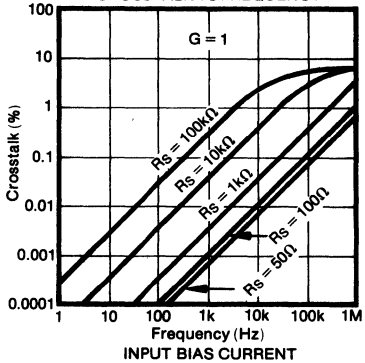
INPUT NOISE VOLTAGE VS FREQUENCY



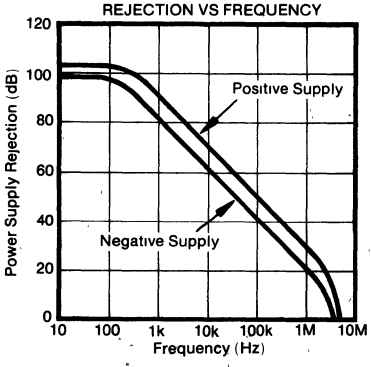
INPUT NOISE CURRENT VS FREQUENCY



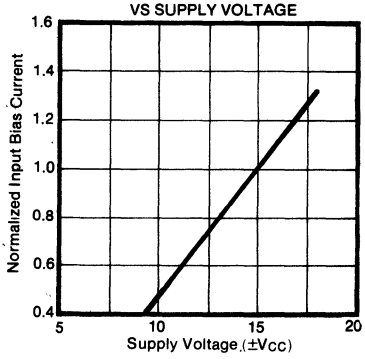
CHANNEL-TO-CHANNEL CROSSTALK VS FREQUENCY



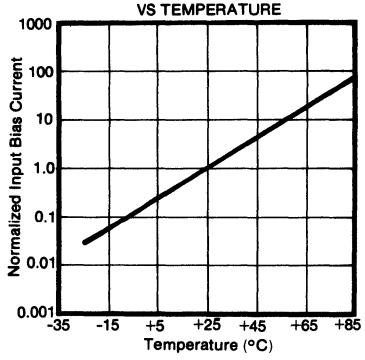
POWER SUPPLY REJECTION VS FREQUENCY



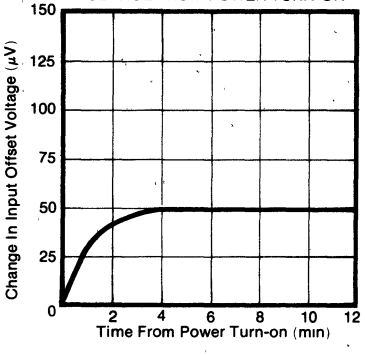
INPUT BIAS CURRENT VS SUPPLY VOLTAGE



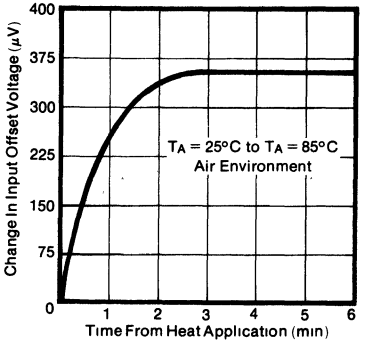
INPUT BIAS CURRENT VS TEMPERATURE



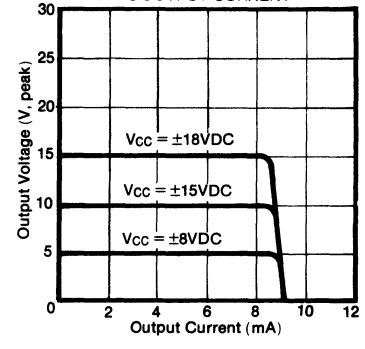
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



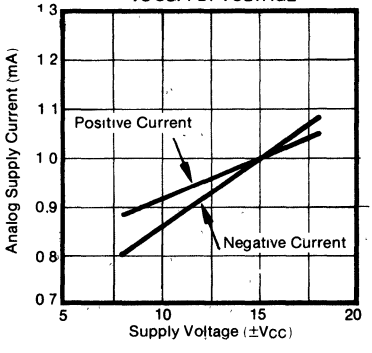
THERMAL RESPONSE TIME OF INPUT OFFSET VOLTAGE FROM HEAT APPLICATION



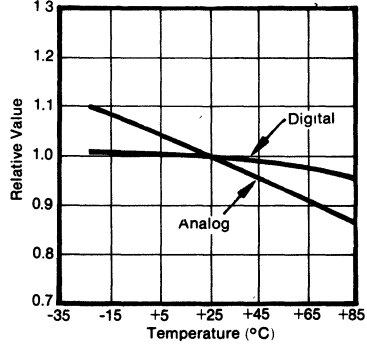
OUTPUT VOLTAGE VS OUTPUT CURRENT



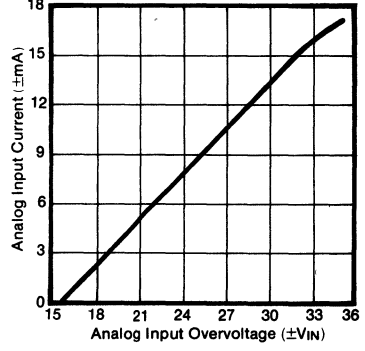
ANALOG SUPPLY CURRENT VS SUPPLY VOLTAGE



QUIESCENT SUPPLY CURRENT VS TEMPERATURE



ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



BURN-IN SCREENING

Burn-in screening is an option available for the PGA100. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

DISCUSSION OF PERFORMANCE

The PGA100 is a self-contained programmable-gain amplifier whose gain can be changed in 8 binarily weighted steps from 1 to 128 or as scaled externally through the gain scale/adjust pin. The gain control is accomplished by the gain switch (break-before-make) whose position is determined by the 3-bit TTL address, A_3, A_4, and A_5. When selected, 1 of 8 positions connects the thin-film resistor network to the feedback loop of the op amp. This establishes the desired gain. (See Installation and Operating Instructions for gain scaling.)

Similarly, the 8 analog input channels are switched by the input multiplexer (break-before-make) whose position is determined by the 3-bit TTL address, A_0, A_1, and A_2. Gain and channel selection appear in Table I. 64-channel gain combinations are possible.

The digital inputs are latched by the positive transition of the clock pulse, pin 18, when the clock enable, pin 19, is low. The relative set up and holding times specified in the Electrical Specifications are shown in Figure 1. The internal latch is similar to the industry standard 74LS378. Figure 2 shows a timing diagram for selected addresses indicating: the enable function, changing channel and gain, changing channel constant gain, and constant channel, changing gain.

TABLE I. Gain and Channel Select Truth Table.

GAIN SELECT			GAIN	CHANNEL SELECT			CHANNEL
A_5	A_4	A_3		A_2	A_1	A_0	
0	0	0	1	0	0	0	IN0
0	0	1	2	0	0	1	IN1
0	1	0	4	0	1	0	IN2
0	1	1	8	0	1	1	IN3
1	0	0	16	1	0	0	IN4
1	0	1	32	1	0	1	IN5
1	1	0	64	1	1	0	IN6
1	1	1	128	1	1	1	IN7

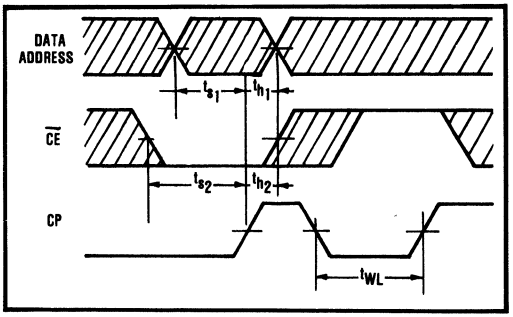


FIGURE 1. Data Address and Clock Enable Setup and Hold Times.

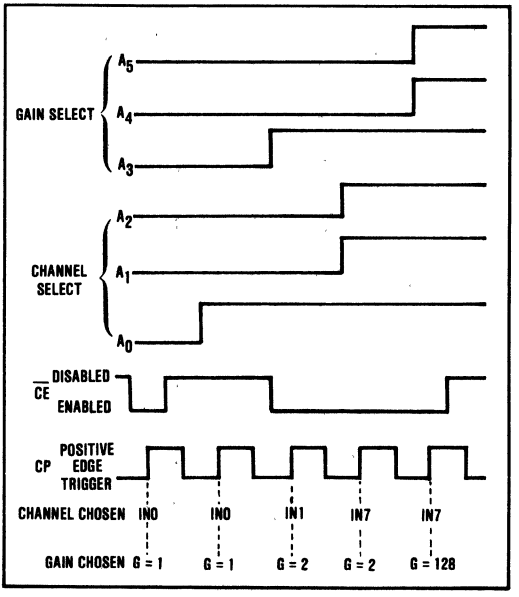


FIGURE 2. Timing Diagram for Selected Addresses.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY AND SIGNAL CONNECTIONS

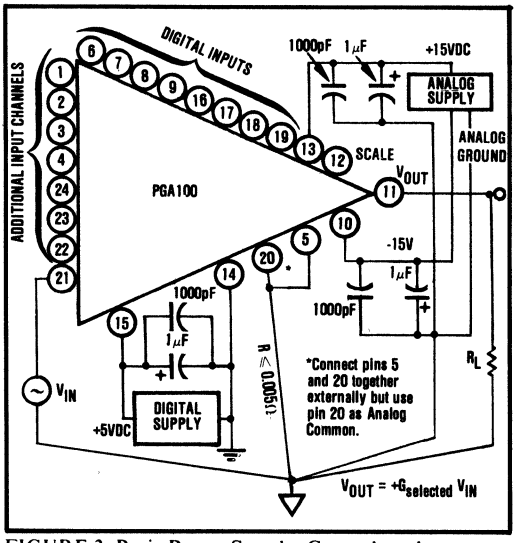


FIGURE 3. Basic Power Supply, Ground, and Signal Connections.

Figure 3 shows the proper analog and digital power supply connections. The supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the amplifier as possible. To avoid gain errors connect grounds as indicated being sure to minimize ground resistance. Note that a resistance of greater than

0.005Ω in series with the analog common will degrade the specified gain accuracy. IMPORTANT: Normally the digital ground is brought in from the digital power supply on a separate line. However, the analog and digital commons must be connected together somewhere in the system.

OPTIONAL GAIN SCALE/ADJUST

The gain scale/adjust pin is shown in Figure 4. When no connection is made, gains appear as in Table I. At least two functions can be performed. First, the gain range can be scaled to gains other than 1 to 128, for example, 1 to 100 or 1 to 1024. Gain steps, however, retain binary weighting. Some examples are: (1, 1, 2, 4, 8, 16, 32, 64 with pins 11 and 12 connected together), (1, 1.5625, 3.125, 6.25, 12.5, 25, 50, 100), (1, 12.5, 25, 50, 100, 200, 400, 800), and (1, 16, 32, 64, 128, 256, 512, 1024). Scaling is accomplished by using a potentiometer, R_1, shown in Figure 4. Be certain to use a potentiometer of good mechanical and thermal stability. Additional gain drift with temperature should be minimal since it depends on the thermal tracking of the resistance ratio, R_A to R_B, set by the potentiometer.

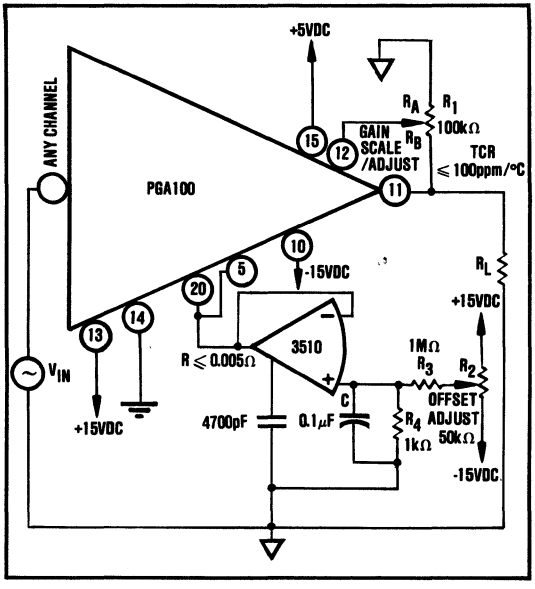


FIGURE 4. External Gain and Offset Adjustment.

Second, the gain inaccuracy, remaining after laser trimming at the factory, can be adjusted to zero at any gain other than unity. To improve resolution and limit adjustment range, a resistor may be added in series with the wiper of the potentiometer and pin 12. This will, however, increase gain drift. Figure 5 shows the effect of gain adjustment. R_1 does not affect gain linearity.

OPTIONAL OFFSET ADJUSTMENT

Figure 4 also illustrates a technique for offset adjustment. This adjustment has no effect at unity gain. R_2 will trim the offset to zero and have neglible effect on the gain accuracy. For best results, trim the offset at the highest

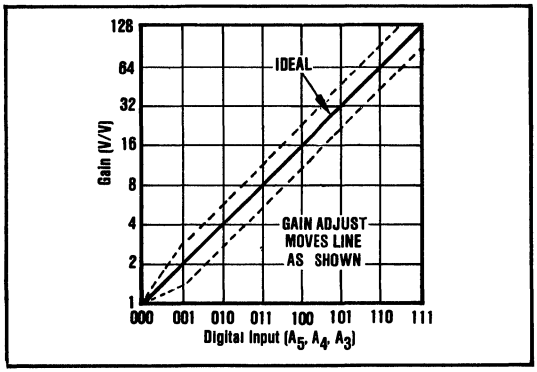


FIGURE 5. Effect of Gain Adjustment.

gain. If R_3 is made smaller, output offsetting can be accomplished. This can be used to introduce an intentional DC voltage at the output. The external amplifier used will add to the input noise, therefore, use one with a noise level of at least three times lower than that specified for the PGA100.

LAYOUT CONSIDERATIONS

Proper attention to layout is necessary to achieve the specified performance of the PGA100. Major goals are to reduce crosstalk, noise pickup, noise coupled from the power supply, and gain errors.

Be certain to separate analog and digital runs to avoid coupling of digital transients. To reduce gain errors, connect analog grounds with a ground plane or a low resistance star configuration as shown in Figure 3. Analog and digital commons must be connected at some point in the system to insure proper operation.

GAIN INACCURACY AND NONLINEARITY

As shown in Figure 3, connect pins 5 and 20 directly together at the unit and use pin 20 as the primary analog common. Ground resistance in series with pin 20 also appears in series with the internal gain-setting resistors and will decrease the magnitude of all gains except unity. The resulting accuracy error varies nonlinearly with the gain selected and therefore cannot be externally adjusted to zero for more than one gain at a time. Gain linearity is not affected by external ground resistance (see Performance Curves.)

CROSSTALK

Crosstalk is the amount of signal feedthrough from all OFF channels that appears at the output of the input multiplexer. It is expressed as a percent of the input signal applied to all OFF channels. For example, the 0.003% specification indicates that 0.6mV, p-p, out of a 20V, p-p, 1kHz sine wave (applied to 7 OFF channels) will appear at the noninverting input of the internal op amp. Note that crosstalk increases with high frequencies due to the capacitive coupling between ON and OFF channels. It also increases with greater source resistance. However, because both the input signal and crosstalk noise are amplified equally, the resulting output signal-to-noise

ratio is independent of gain. Unused input channels should be grounded in order to reduce crosstalk and extraneous noise pickup. (See Performance Curves.)

SETTLING TIME

Settling time is the time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value. It is a very important consideration since this will be the limiting parameter in determining the maximum channel scanning or throughput rate. The PGA100 specification includes the effects of both the multiplexer and amplifier. Note that settling time increases with increasing source resistance and gain. Minimum settling time is achieved by choosing a low source resistance, for example, $R_S \leq 10k\Omega$ and gains ≤ 16. (See Performance Curves.)

INPUT OVERVOLTAGE PROTECTION

The PGA100 provides input overvoltage protection of 20V in excess of either power supply voltage expressed as $\pm(|V_{CC}|+20)$. This is achieved in the dielectrically isolated analog multiplexer which will withstand overvoltage even when the power supplies are off. As a consequence the PGA100 is protected against high input levels and brief transient spikes of up to several hundred volts that can result from signals originating from outside the system. (See Performance Curves.)

TYPICAL APPLICATIONS

The PGA100 is ideal for a variety of applications, especially where low channel-to-channel crosstalk is required. In many applications the PGA100 will not require trimming of offset and gain errors. However, these can be minimized utilizing hardware or software error correction techniques. Figures 6 and 7 show applications of the PGA100 separately and in a data acquisition system.

Figure 7 shows a Data Acquisition System. In this system the PGA100 allows the user to deal with signals of wide dynamic range while maintaining high system resolution. For example: When used with a 12-bit A/D converter in a "floating point" system, the 2^7 gain range of the PGA100 plus the 2^{12} range of the converter produces a total system resolution of 2^{19} (524,000 to 1).

Also the user can modify and reprogram gain values for different analog input channels merely by changing the software computer program. Since different dedicated amplifiers are not required for various input channels, the PGA100 also saves space and overall system costs. Software correction virtually eliminates system offset and gain errors over both time and temperature.

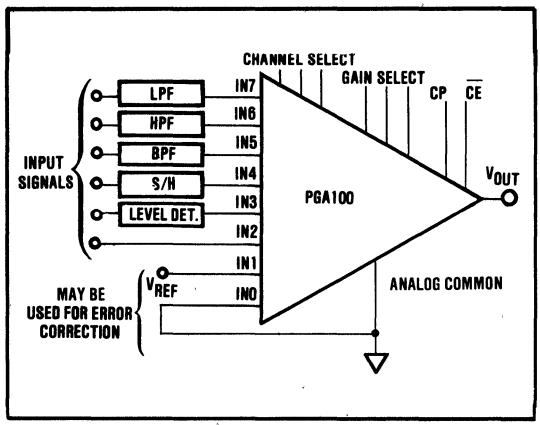


FIGURE 6. Digitally Selectable Function Amplifier.

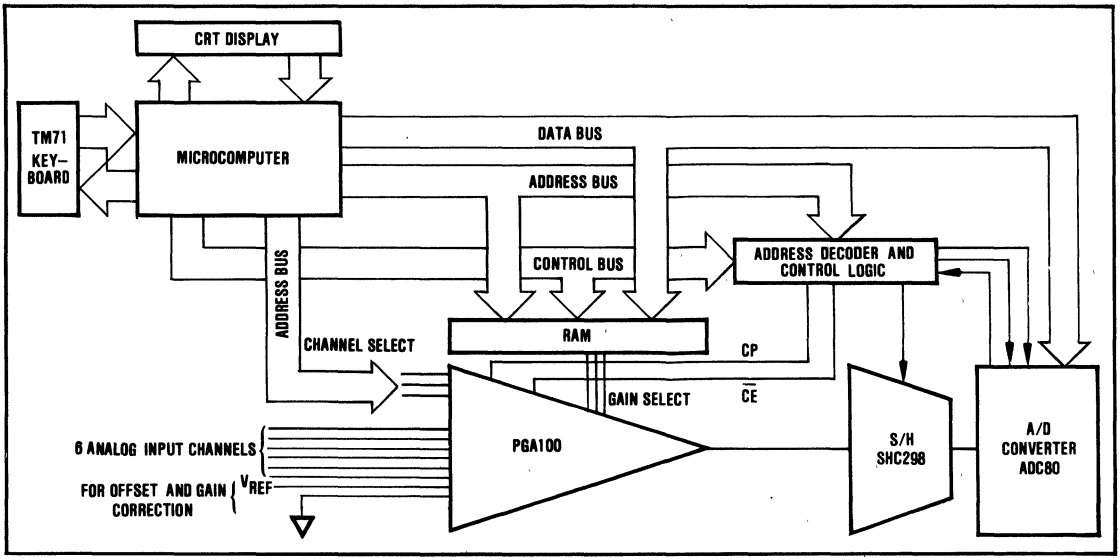
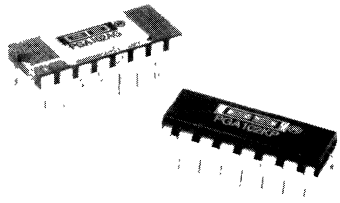


FIGURE 7. Use of PGA100 in a Data Acquisition System with Software Auto-zero and Gain Calibration.

BURR-BROWN®



PGA102

AVAILABLE IN DIE FORM

Digitally-Controlled Programmable-Gain/Fast-Settling OPERATIONAL AMPLIFIER

FEATURES

- DIGITALLY-PROGRAMMABLE GAINS, X1, X10, X100
- LOW GAIN ERROR, 0.01%, max
- LOW GAIN DRIFT, 5ppm/°C, max
- LOW NONLINEARITY, 0.003%, max, 14-BIT
- FAST SETTLING, 2.8μs, 0.01%, typ
- THREE INDEPENDENT INPUT CHANNELS WITH SEPARATE GAIN ADJUSTMENT
- LOW COST
- SMALL 16-PIN DIP PACKAGE, CERAMIC AND PLASTIC

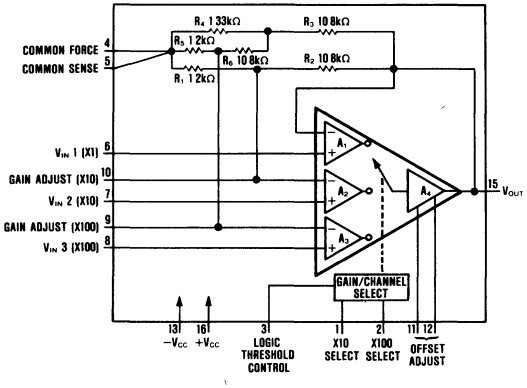
APPLICATIONS

- DATA ACQUISITION AMPLIFIER
- AUTORANGING AMPLIFIER UNDER COMPUTER CONTROL
- SUPER-ACCURACY, LOW COST, FIXED GAIN BLOCK
- TEST EQUIPMENT GAIN CONTROL
- PORTABLE INSTRUMENT GAIN SELECTION
- DATA LOGGING RANGING CONTROL
- 3-CHANNEL MULTIPLEXER

DESCRIPTION

The PGA102 is a precision digitally-programmable gain block. Its monolithic design permits low cost and high reliability. The user can select one of three gains (1, 10, 100), two of which are independently adjustable. The logic section has high input impedance and functions without a separate supply. Precision laser-trimmed offset and gains permit use without external adjustments. High performance thin-film resistors with excellent temperature tracking assure low gain drift and excellent stability.

The fast 2.8μsec settling makes the PGA102 ideal for rapid channel scanning in data acquisition systems. Also the high accuracy is very beneficial in test equipment and instrumentation applications where programmable or fixed gain is required.



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SPECIFICATIONS

ELECTRICAL

At +25°C, ±V_{CC} = 15VDC unless otherwise specified

PARAMETER	CONDITIONS	PGA102AG			PGA102BG/SG			PGA102KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Inaccuracy[1]	R_L = 2kΩ, G = 1		±0.007	±0 02		±0 003	±0 01		*	*	%
	G = 10		±0 015	±0.03		±0 01	±0.02		*	±0 05	%
	G = 100		±0 02	±0 05		±0 015	±0 025		*	±0 06	%
vs Temperature	G = 1		±0 4	±5		*	*		*	*	ppm/°C
	G = 10		±2	±7		*	*		*	*	ppm/°C
	G = 100		±7	±20		*	*		±9	*	ppm/°C
Nonlinearity	R_L = 2kΩ, G = 1		0 001	0 003		*	*		*	*	% of FS
	G = 10		0 002	0 005		*	*		*	*	% of FS
	G = 100		0 003	0 01		*	*		*	*	% of FS
RATED OUTPUT											
Voltage	R_L = 2kΩ	±10	±12 5		*	*		*	*		V
Current	V_{OUT} = 10V	±5	±10		*	*		*	*		mA
Short Circuit Current		±10	±25		*	*		*	*		mA
Output Resistance			0 01			*			*		Ω
Load Capacitance	For stable operation		2000			*			*		pF
INPUT OFFSET VOLTAGE											
Initial[2]	G = 1		±200	±500		±100	±250		*	±1500	μV
	G = 10		±70	±200		±50	±100		*	±600	μV
	G = 100		±70	±200		±50	±100		*	±600	μV
vs Temperature	G = 1		±5	±20		*	*		±7	±50	μV/°C
	G = 10		±1	±7		*	*		±3	±10	μV/°C
	G = 100		±0 5	±3		*	*		±2	±7	μV/°C
vs Supply Voltage	±5 < V_{CC} < ±18V										
	G = 1		±30	±70		*	*		*	*	μV/V
	G = 10		±8	±30		*	*		*	*	μV/V
	G = 100		±8	±30		*	*		*	*	μV/V
INPUT BIAS CURRENT											
Initial	T_A = +25°C		±20	±50		*	*		*	*	nA
Over Temperature	$T_{A\ MIN}$ to $T_{A\ MAX}$		±25	±60		*	*		*	*	nA
ANALOG INPUT CHARACTERISTICS											
Voltage Range	Linear operation	±10	±12		*	*		*	*		V
Resistance			7×10^8			*			*		Ω
Capacitance			4			*			*		pF
INPUT NOISE											
Voltage Noise	f_B = 0 1Hz to 10Hz										
	G = 1		4 5			*			*		μV p-p
	G = 10		1 5			*			*		μV p-p
	G = 100		0 6			*			*		μV p-p
Voltage Noise Density	f_O = 1Hz, G = 1		490			*			*		nV/√Hz
	G = 10		178			*			*		nV/√Hz
	G = 100		83			*			*		nV/√Hz
	f_O = 10Hz, G = 1		155			*			*		nV/√Hz
	G = 10		56			*			*		nV/√Hz
	G = 100		20			*			*		nV/√Hz
	f_O = 100Hz, G = 1		93			*			*		nV/√Hz
	G = 100		31			*			*		nV/√Hz
	G = 100		18			*			*		nV/√Hz
	f_O = 1kHz, G = 1		79			*			*		nV/√Hz
	G = 10		31			*			*		nV/√Hz
	G = 100		18			*			*		nV/√Hz
Current Noise	f_B = 0 1Hz to 10Hz		76			*			*		pA p-p
Current Noise Density	f_O = 1Hz		8 8			*			*		pA/√Hz
	f_O = 10Hz		2 8			*			*		pA/√Hz
	f_O = 100Hz		0 99			*			*		pA/√Hz
	f_O = 1kHz		0 43			*			*		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Power Supply ..... ±18V

Input Voltage Range Analog ..... ±V_{CC}

Digital ..... ($V_{PIN\ 3}$ − 5 6V) to +V_{CC}

Storage Temperature Range G Package ..... −65°C to +150°C

P Package ..... −55°C to +125°C

Lead Temperature (soldering 10 seconds) ..... +300°C

Output Short-Circuit Duration ..... Continuous to Common

Junction Temperature. G Package ..... +175°C

P Package ..... +110°C

ELECTRICAL (CONT)

PARAMETER	CONDITIONS	PGA102AG			PGA102BG/SG			PGA102KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC RESPONSE											
±3dB Bandwidth	Small signal, G = 1		1500			*			*		kHz
	G = 10		750			*			*		kHz
	G = 100		250			*			*		kHz
Full Power Bandwidth	V_{OUT} = ±10V, R_L = 2kΩ		160			*			*		kHz
Slew Rate	V_{OUT} = ±10V step,										
	R_L = 2kΩ	6	9		*	*		*	*		V/μs
Settling Time (0 1%)	V_{OUT} = 10V step, G = 1		1.6			*			*		μs
	G = 10		2 2			*			*		μs
	G = 100		5 2			*			*		μs
Settling Time (0 01%)	V_{OUT} = 10V step, G = 1		2.8			*			*		μs
	G = 10		2 8			*			*		μs
	G = 100		8 2			*			*		μs
Overload Recovery Time, 0 1%	50% overdrive, G = 1 (see Performance Curve)		2 5			*			*		μs
CROSSTALK											
DC	±10V to both Off channels		−155			*			*		dB
60Hz	±10V to both Off channels		−144			*			*		dB
DIGITAL INPUT CHARACTERISTICS											
Input "Low" Threshold	V_{IL}[3] on pin 1 or 2			VLTC+0 8			*			*	V
Input "Low" Current				1			*			*	μA
Input "High" Threshold	V_{IH}[3] on pin 1 or 2	VLTC+2		1	*		*	*		*	V
Input "High" Current			0 1	1		*	*		*	*	μA
Logic Threshold Control	VLTC on pin 3	−V_{CC}		V_{CC} − 4	*		*	*		*	V
Switching Time[4]	Between channels		1			*			*		μs
POWER SUPPLY											
Rated Voltage			±15			*			*		VDC
Voltage Range		±5		±18	*		*	*		*	VDC
Quiescent Current	V_{OUT} = 0V		±2 4	±3.3		*	*		*	*	mA
	No external load, V_{OUT} = ±10V			±5 3			*			*	mA
TEMPERATURE RANGE											
Specification, KP grade	$T_{A\ MIN}$ to $T_{A\ MAX}$							0		+70	°C
AG and BG grades		−25		+85	*		*				°C
SG grade					−55		+125				°C
Operating		−55		+125	*		*	−25		+85	°C
Storage		−65		+150	*		*	−55		+125	°C
Thermal Resistance	θ_{JA}		100			*			*		°C/W

* Specification same as AG grade

NOTES (1) Gain inaccuracy is the percent error between the actual and ideal gain selected It may be externally adjusted to zero for gains of 10 and 100 (2) Offset voltage can be adjusted for any one channel Adjustment affects temperature drift by approximately ±0 3μV/°C for each 100μV of offset adjusted (3) Voltage on the logic threshold control pin, VLTC, adjusts the threshold for "Low" and "High" logic levels (4) Total time to settle equals switching time plus settling time of the newly selected gain

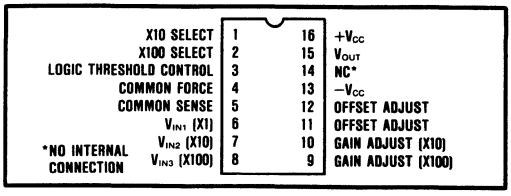
BURN-IN OPTION

Burn-in screening is an option available for the PGA102. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

PIN CONFIGURATION



ORDERING INFORMATION

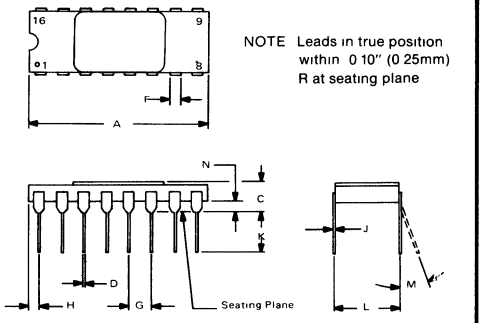
Model	Package	Temperature Range
PGA102AG	Ceramic DIP	-25°C to +85°C
PGA102BG	Ceramic DIP	-25°C to +85°C
PGA102SG	Ceramic DIP	-55°C to +125°C
PGA102KP	Plastic DIP	0°C to +70°C

BURN-IN SCREENING OPTION
See text for details

Model	Package	Burn-In Temp. (160h)[1]
PGA102AG-BI	Ceramic DIP	+125°C
PGA102BG-BI	Ceramic DIP	+125°C
PGA102SG-BI	Ceramic DIP	+125°C
PGA102KP-BI	Plastic DIP	+85°C

NOTE Or equivalent combination See text

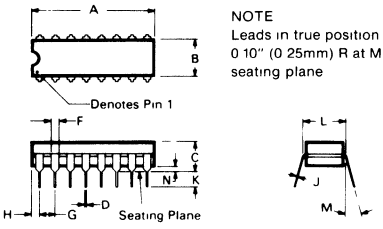
MECHANICAL



NOTE Leads in true position within 0.10" (0.25mm) R at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.025	.060	0.64	1.52

EPOXY DUAL-IN-LINE

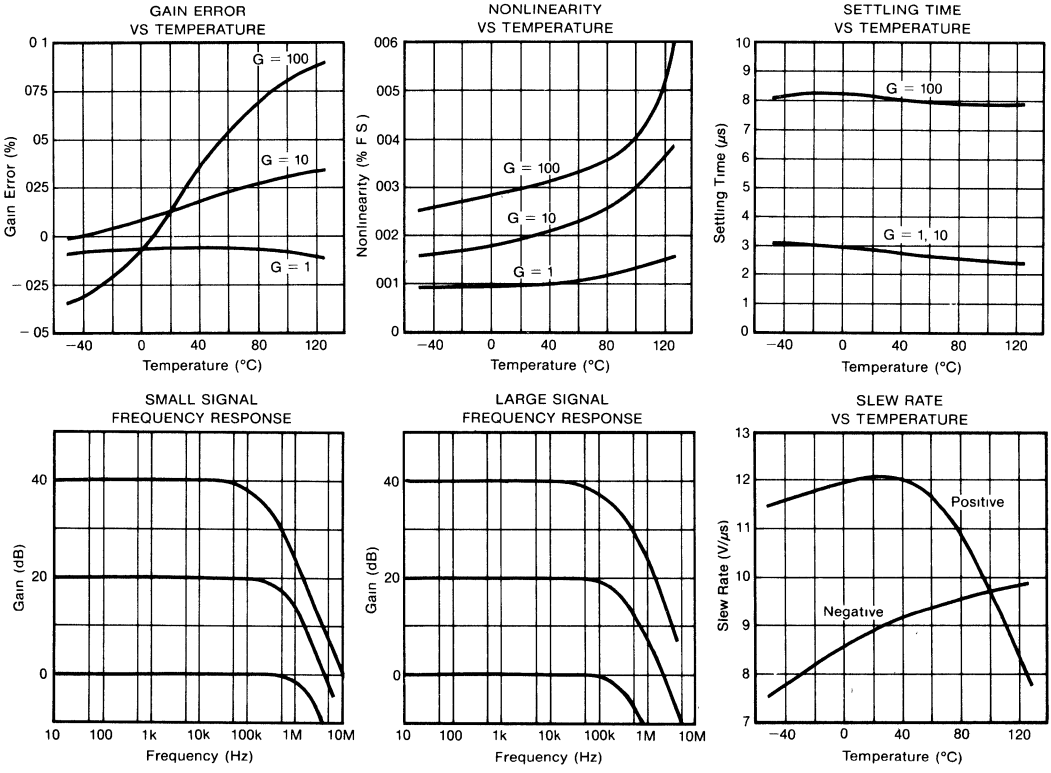


NOTE
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.760	.885	19.30	22.48
B	.220	.280	5.59	7.11
C		.200		5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.008	.015	0.20	0.38
K	.100	--	2.54	--
L	.300 BASIC		7.62 BASIC	
M	--	15°	--	15°
N	.020	.050	0.51	1.27

TYPICAL PERFORMANCE CURVES

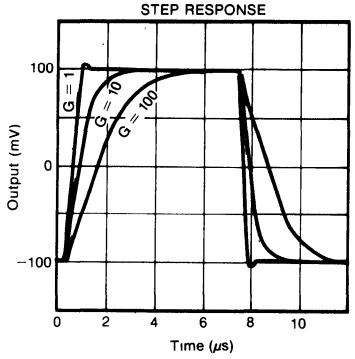
T_A = 25°C, $\pm V_{CC}$ = 15VDC unless otherwise noted



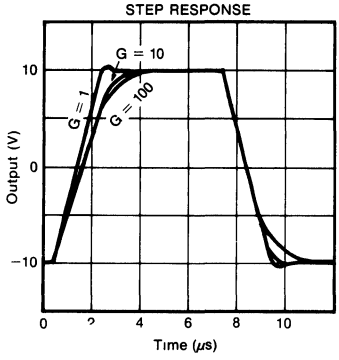
TYPICAL PERFORMANCE CURVES (CONT)

T_A = 25°C, $\pm V_{CC}$ = 15VDC unless otherwise noted.

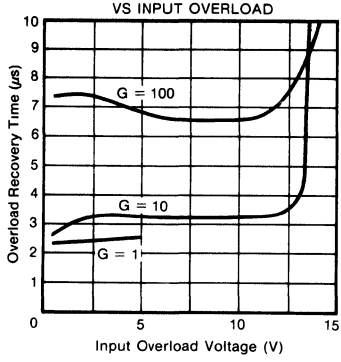
SMALL SIGNAL STEP RESPONSE



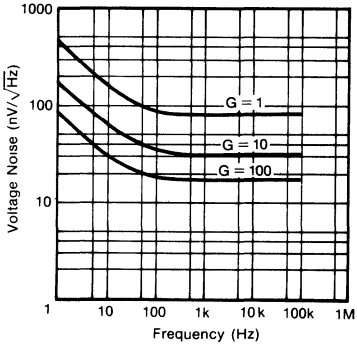
LARGE SIGNAL STEP RESPONSE



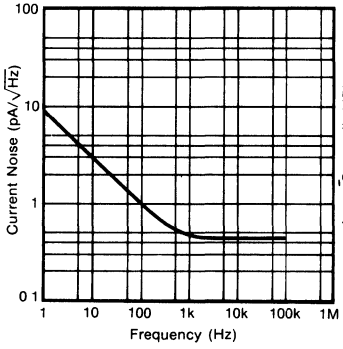
OVERLOAD RECOVERY VS INPUT OVERLOAD



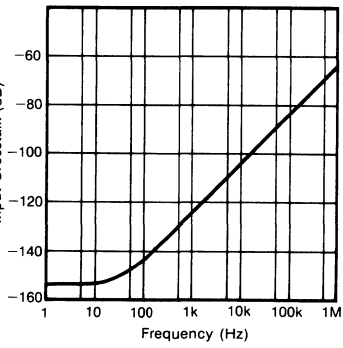
INPUT VOLTAGE NOISE VS FREQUENCY



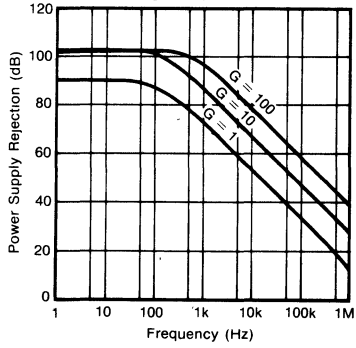
INPUT CURRENT NOISE VS FREQUENCY



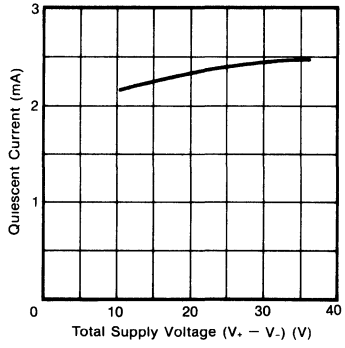
INPUT CROSSTALK VS FREQUENCY



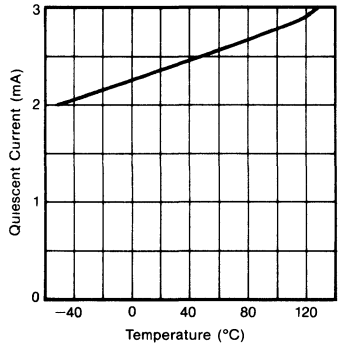
POWER SUPPLY REJECTION VS FREQUENCY



QUIESCENT CURRENT VS SUPPLY VOLTAGE



QUIESCENT CURRENT VS TEMPERATURE



THEORY OF OPERATION

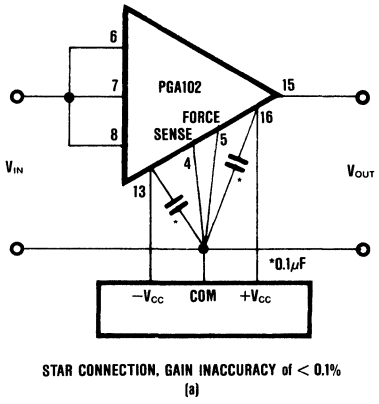
The PGA102 is a self-contained programmable-gain amplifier with digitally selectable gains of 1, 10, and 100.

A block diagram of the PGA102 is shown on the first page of this data sheet. The circuit contains three sections: (1) 3-channel switchable-input operational amplifier, (2) precision thin-film resistor network (R_1–R_6), and (3) gain/channel select digital circuit.

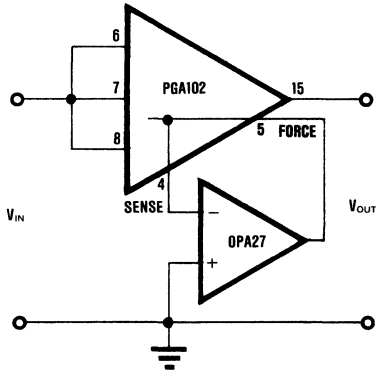
Under control of the channel select circuitry, only one input stage (A_1, A_2, or A_3) is active at any time. The selected input stage steers input signals (V_{IN1}, V_{IN2}, or V_{IN3}) to the output amplifier (A_4). At this time the unselected input stages are turned off by deactivation of their internal bias circuitry. Three different precision gains are produced by closing the feedback loop through the selected input stage. This unique feature of having each channel set to a specific gain allows the user more flexibility in applications. Low gain drift is achieved by the excellent tracking of the thin-film gain set resistors. The "trip point" on select pins 1 and 2 for changing channels, and hence gain, is set by the logic threshold control voltage on pin 3.

INSTALLATION AND OPERATING INSTRUCTIONS

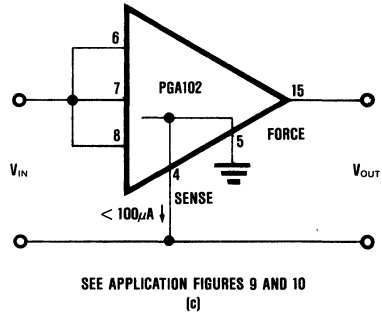
Figure 1 shows proper power supply and signal connections. The supplies should be decoupled with 0.1μF capacitors as close to the package as possible. To avoid gain errors, connect ground as indicated, being sure to minimize ground resistance. The PGA102 has a separate ground force and ground sense which virtually eliminate gain errors due to resistance in the common line. The gain error results from any resistance added in series with the internal junction of R_1, R_4, and R_5. Internally, wire bond resistance of 0.2Ω can cause a 0.02% error for gain of 10 and 0.2% error for gain of 100. By minimizing the current in the sense line, specified performance is achievable.



STAR CONNECTION, GAIN INACCURACY of < 0.1%
(a)



SEE APPLICATION FIGURE 14
(b)



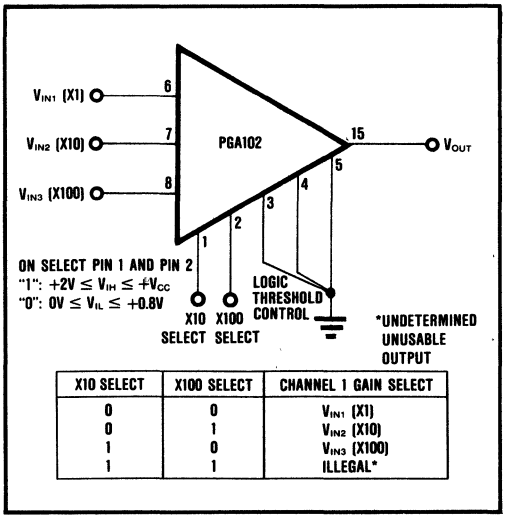
SEE APPLICATION FIGURES 9 AND 10
(c)

(b) AND (c) ELIMINATE GAIN ERRORS DUE TO RESISTANCE OF THE INTERNAL WIRE BOND (INACCURACY < 0.05%).

FIGURE 1. Power Supply and Signal Connections.

GAIN/CHANNEL SELECTION

Gain is chosen by digitally manipulating the voltage level on the X10 and X100 select pins as shown in Figure 2. The table in Figure 2 shows how to select a specific channel which has a gain of 1, 10, or 100. In this circuit, the logic threshold control has been grounded to give compatibility with TTL levels. However, this threshold can be set anywhere between [$-V_{CC}$ + 4V] and [$+V_{CC}$ − 2.6V] for compatibility with other logic such as CMOS.



X10 SELECT	X100 SELECT	CHANNEL 1 GAIN SELECT
0	0	V_{IN1} (X1)
0	1	V_{IN2} (X10)
1	0	V_{IN3} (X100)
1	1	ILLEGAL*

FIGURE 2. Channel Selection for Ground-Referenced Logic Threshold (TTL-compatible).

In general, the logic state is determined by the voltage on pin 1 or pin 2 relative to the threshold control voltage on pin 3. The input high (V_{IH}) and low (V_{IL}) voltages to switch states are shown below:

Logic one, "1": $(V_{LTC} + 2V) < V_{IH} < +V_{CC}$

Logic zero, "0": $(V_{LTC} - 5.6) < V_{IL} < (V_{LTC} + 0.8V)$

An external decoder and latch on the select lines may be added for operation in computer-controlled analog input/output systems.

OPTIONAL OFFSET ADJUSTMENT

The input offset voltage is laser trimmed and will not require user adjustment for most applications. However, pins 11 and 12 may be used to adjust the offset of the

active channel to zero as shown in Figure 3. This also affects the inactive channels (all offsets move as the potentiometer is adjusted). By compromising, the user can adjust for the average offset of all three channels using one potentiometer; or a compromise for just the X10 and X100 channels can be made, considering the unity gain channel's offset is insignificant for high-level inputs.

Figure 4 shows another approach to offset adjustment. An inexpensive CMOS switch (4016) may be used to independently connect the wipers of three potentiometers to $-V_{CC}$. Therefore, R_1, R_2, and R_3 adjust the offset of channels 1, 2, and 3 respectively.

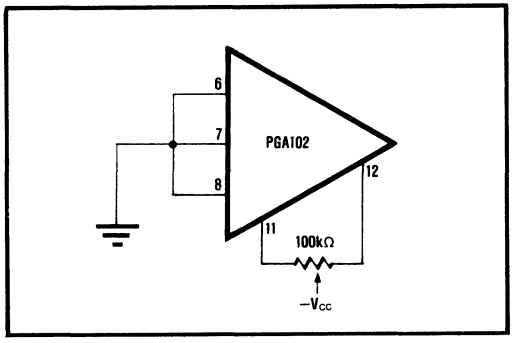


FIGURE 3. Offset Adjustment.

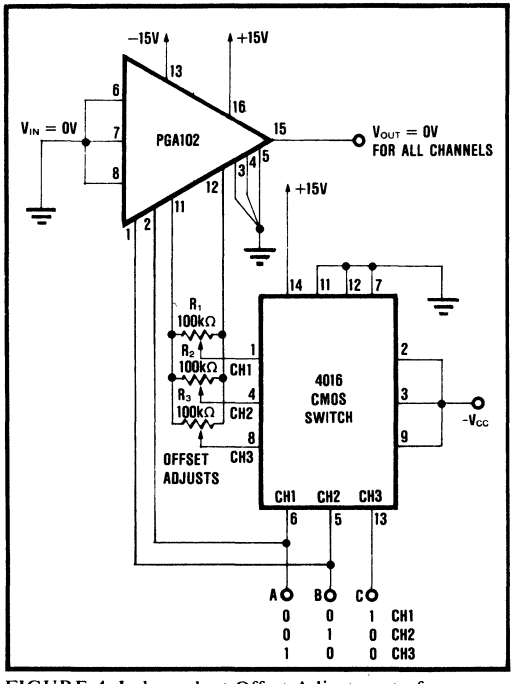


FIGURE 4. Independent Offset Adjustment of Channels 1, 2, and 3.

OPTIONAL GAIN ADJUSTMENT

The initial gain accuracy has been internally laser trimmed to high precision, but can be adjusted. Figure 5 shows independent fine-gain adjustment of channels 2 and 3. This involves either paralleling the internal input resistors for gain up or the internal feedback resistors for gain down. External resistors R_2, R_3, R_5, and R_6 are chosen to trade off range and resolution. Channel 1's gain cannot be adjusted due to the internal zero feedback resistance.

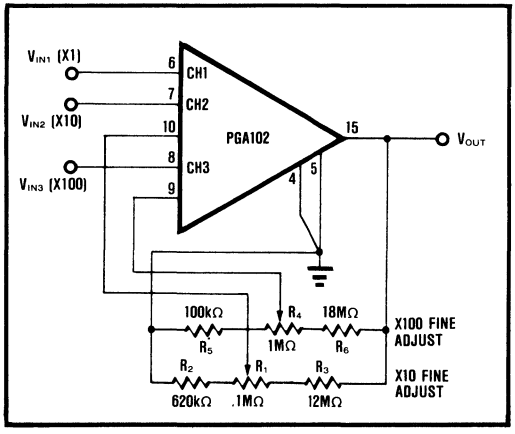


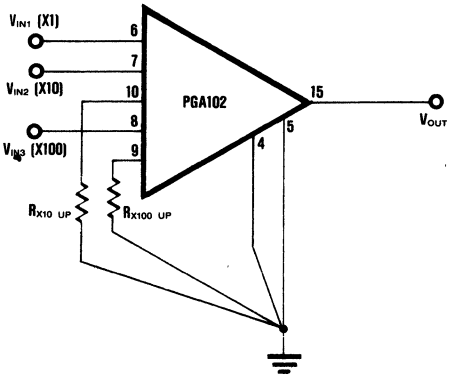
FIGURE 5. Independent Fine Gain Adjustment of Channels 2 and 3.

For applications requiring gains other than 1, 10, or 100, the PGA102 can be gained up (Figure 6) or down (Figure 7). It is important to realize that the temperature drift of the external gain adjustment resistors will affect the total gain drift. This becomes more predominant as the gain is changed further from the factory-set specification. For example, with small adjustments (20% or so), a 30ppm/°C external resistor will add 6ppm/°C to the 10ppm/°C internal resistor ratio tracking. For large adjustment (50% or so), the effect becomes larger. The best that can be achieved is 25ppm/°C (the TCR of one internal resistor) when the external resistor has 0ppm/°C. Also when adjusting the X10 channel, keep the gain above 5 to assure frequency stability.

LAYOUT CONSIDERATIONS

Proper attention to layout is necessary to achieve the specified performance of the PG102. Major goals are to reduce crosstalk, noise pickup, noise coupled from the power supply, and gain errors.

Be certain to separate the runs for analog and digital grounds to avoid coupling of digital transients. To reduce gain errors, connect analog grounds with a ground plane or a low resistance star configuration. Properly using the PGA102 ground force and sense (see Figure 1) assures the best performance, especially in high gains.

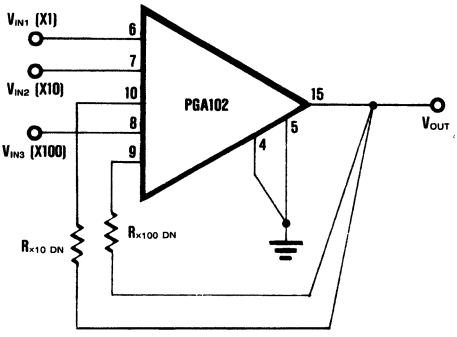


$$R_{X10\ UP} \approx \frac{10.8k\Omega}{G_{X10\ UP} - 10}$$

$$R_{X100\ UP} \approx \frac{108k\Omega}{G_{X100\ UP} - 100}$$

Example:
$R_{X10\ UP} \approx 1.08k\Omega$ and $R_{X100\ UP} \approx 1.08k\Omega$
Gives gains of 1, 20, 200

FIGURE 6. Gain Up Control.



$$R_{X10\ DN} \approx -\left(\frac{97.2k\Omega}{G_{X10\ DN} - 10} + 10.8k\Omega\right)$$

$$R_{X100\ DN} \approx 100\left(\frac{108k\Omega}{100 - G_{X100\ DN}} - 1.09k\Omega\right)$$

Example:
$R_{X10\ DN} \approx 8.64k\Omega$ and $R_{X100\ DN} \approx 107k\Omega$
Gives gains of 1, 5, 50

FIGURE 7. Gain Down Control.

CROSSTALK

Crosstalk expresses the signal feedthrough from an OFF channel that appears at the active input. It is expressed in dB, which translates to a percent of the input signal applied to the OFF channel. Crosstalk increases with increasing frequency (see Typical Performance Curve). Best performance is achieved by keeping input lines short and band limiting if possible.

SETTLING TIME

The PGA102 is designed for applications requiring fast settling. Settling time is the time required, after the onset of a step input signal, for the output voltage to settle and remain within a specified error band around the final value. It is very important because it limits maximum channel scanning or throughput rate in multiplexed systems. Since the error increases with source resistance, keep sources $< 10k\Omega$ for best results.

INPUT OVERLOAD RECOVERY

Another important parameter in data acquisition systems is overload recovery, especially when high gain is selected. The PGA102's fast recovery limits delays in capturing input signals in the presence of large transients. Best results are obtained by clamping input overvoltages to less than 13V (see Typical Performance Curve).

TYPICAL APPLICATIONS

The PGA102 is ideal for auto-gain-ranging systems with many multiplexed input channels that must be scanned quickly. Its high gain accuracy and low temperature drift permit application where computer error correction is not available. In other cases, the PGA102 provides an inexpensive precision fixed gain block requiring no precision external components. An external decoder and latch allow the user flexibility to configure the system as desired. Figures 8 through 15 show application circuits.

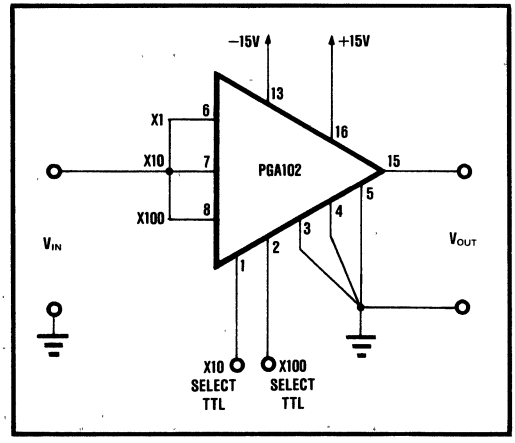


FIGURE 8. Fast Settling Programmable-Gain Amplifier (Gain = 1, 10, 100).

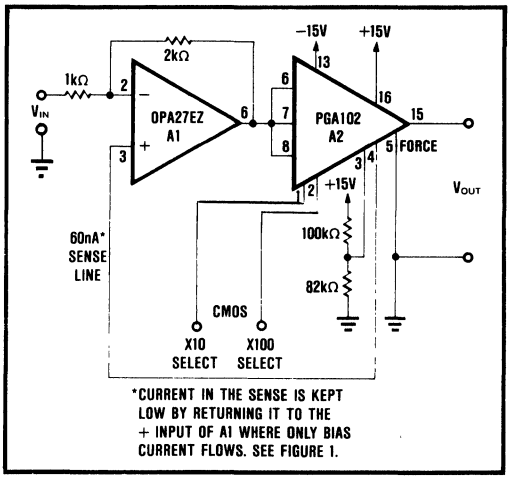


FIGURE 9. Fast-Settling Programmable-Gain Amplifier (Gain = 2, 20, 200).

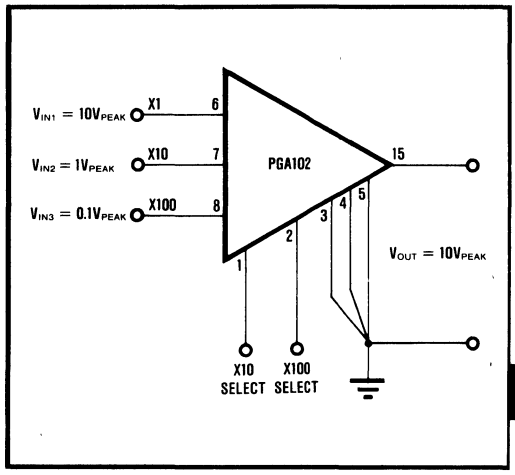


FIGURE 10. Three-Channel Separate Gain Amplifier.

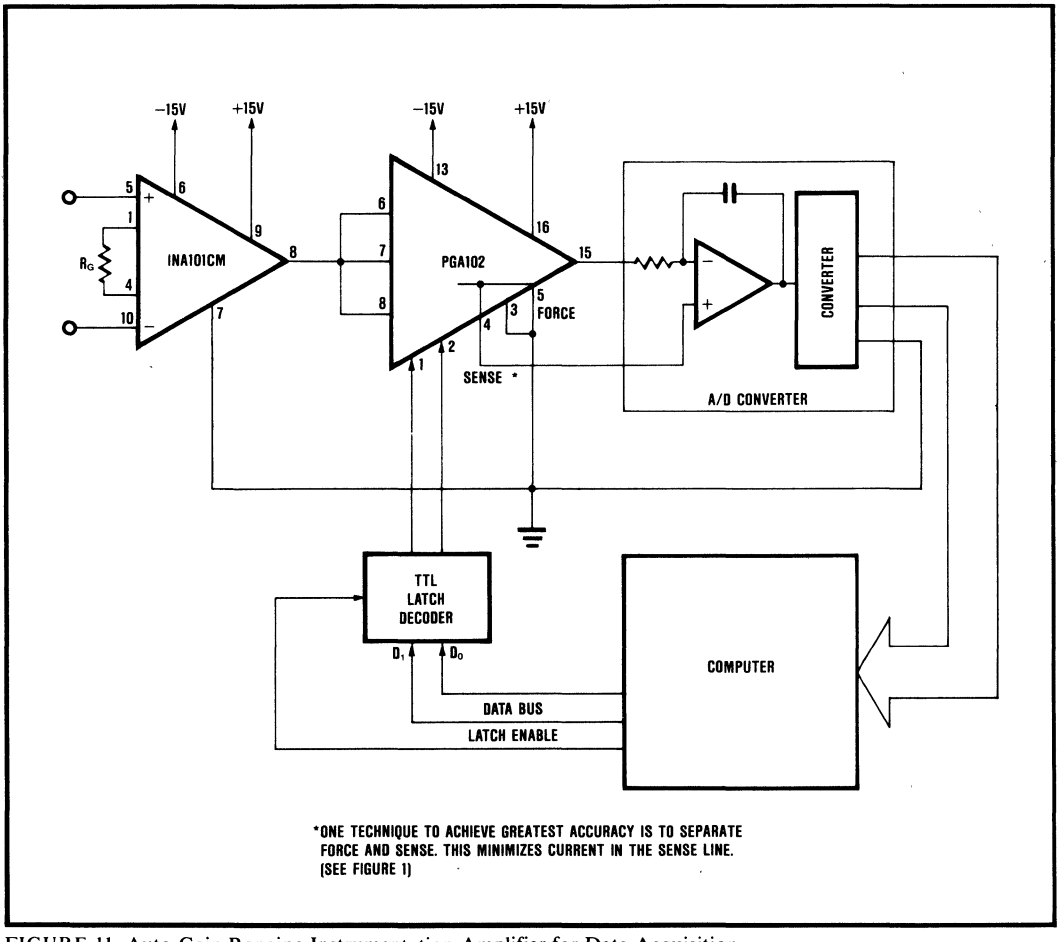


FIGURE 11. Auto-Gain Ranging Instrumentation Amplifier for Data Acquisition.

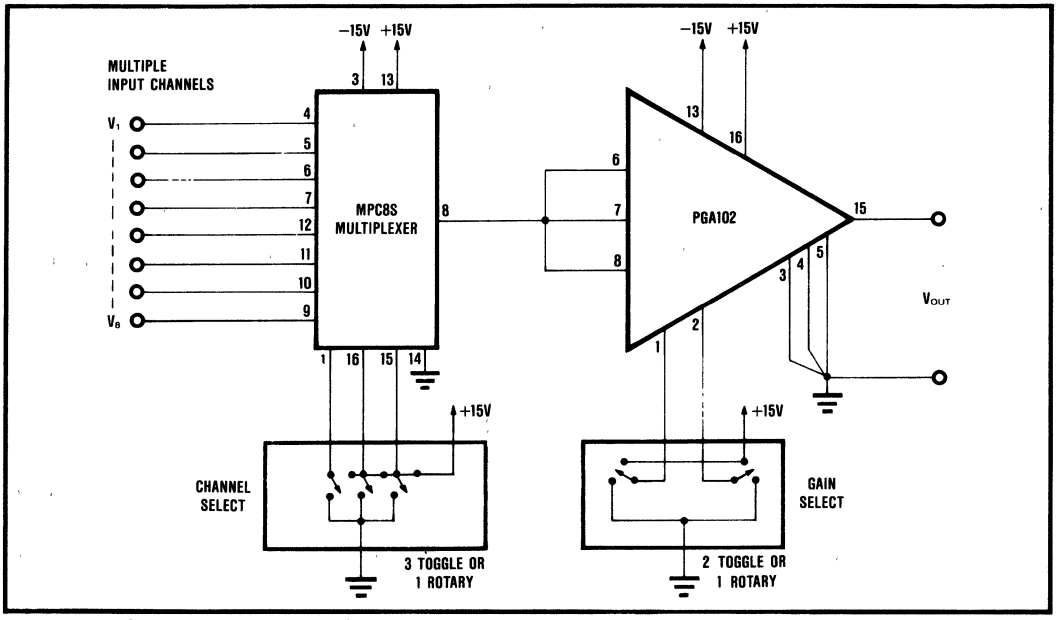


FIGURE 12. Manually Controlled Gain-Ranging Amplifier for Portable Test Equipment.

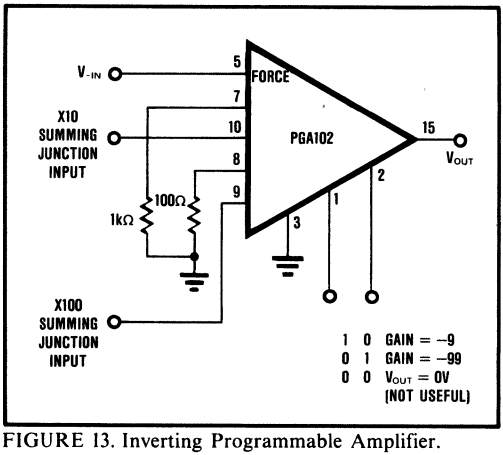


FIGURE 13. Inverting Programmable Amplifier. Summing Junctions Can Be Used for Offsetting.

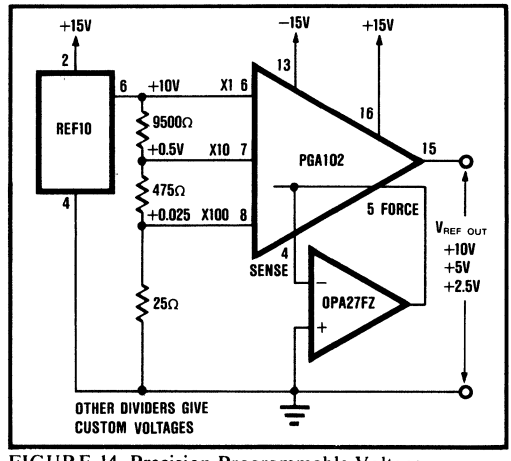


FIGURE 14. Precision Programmable Voltage Reference.

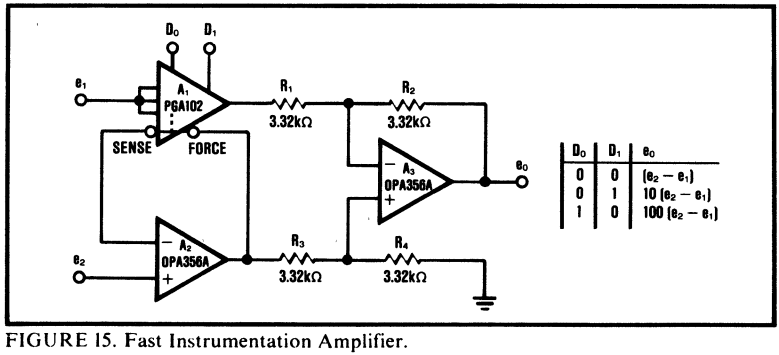
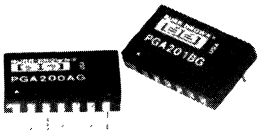


FIGURE 15. Fast Instrumentation Amplifier.

BURR-BROWN®

PGA200/201



Digitally-Controlled Programmable-Gain INSTRUMENTATION AMPLIFIER

FEATURES

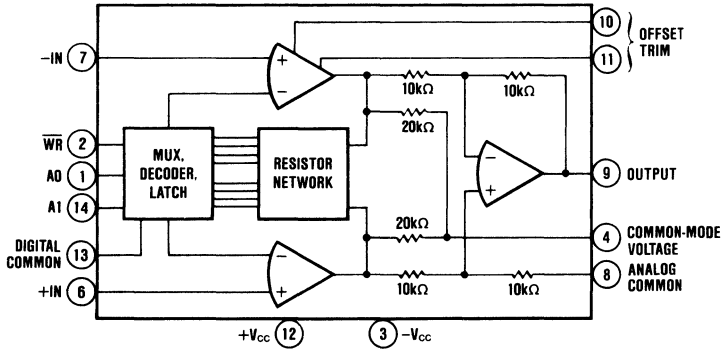
- DIGITALLY-PROGRAMMABLE GAIN
  - Decade Model - PGA200
    Gains of 1, 10, 100, 1000
  - Binary Model - PGA201
    Gains of 1, 8, 64, 512
- EXCELLENT GAIN ACCURACY (0.02%, max)
- LOW GAIN NONLINEARITY (0.012%, max; G = 1000)
- LOW GAIN DRIFT (10ppm/°C, max; G = 1000)
- 2-BIT LATCHED TTL-COMPATIBLE GAIN CONTROL
- LOW OFFSET VOLTAGE (25μV RTI, max; G = 1000)
- LOW OFFSET VOLTAGE DRIFT (0.30μV/°C, max; G = 1000)

APPLICATIONS

- DATA ACQUISITION SYSTEM AMPLIFIER
- DIGITALLY-CONTROLLED AUTORANGING SYSTEM
- SYSTEM DYNAMIC RANGE EXPANSION
- REMOTE INSTRUMENTATION SYSTEM
- TEST EQUIPMENT

DESCRIPTION

The PGA200 is a hybrid IC instrumentation amplifier with digitally-controlled decade gain steps of 1, 10, 100, and 1000. The PGA201 differs only by providing binary steps of 1, 8, 64, and 512. Both have TTL-compatible latched inputs for microprocessor interface. The logic section has high input impedance and functions without a separate logic power supply. Precision laser-trimmed offset and gain permits use without external adjustments. High performance thin-film resistors with excellent tracking assure low gain drift and excellent stability.



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PDS-522B

SPECIFICATIONS

ELECTRICAL

At +25°C with ±15VDC power supply unless otherwise noted

MODEL[1]		PGA200/201AG			PGA200/201BG			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
GAIN								
Inaccuracy[2] G = 1			0 02	0 05		0.01	0 02	%
G = 10			0 02	0.05		0 01	0 02	%
G = 100			0.02	0 05		0 01	0 02	%
G = 1000			0 02	0 05		0 01	0 02	%
Nonlinearity, G = 1			0 002	0 005		0 001	0 002	%
G = 10			0 002	0 005		0 001	0.002	%
G = 100			0 003	0 007		0 002	0 003	%
G = 1000			0 012	0 025		0 011	0 012	%
Drift vs Temperature, G = 1			10	20		5	10	ppm/°C
G = 10			10	20		5	10	ppm/°C
G = 100			10	20		5	10	ppm/°C
G = 1000			10	20		5	10	ppm/°C
Stability vs Time			0.01			*		%/1khr
RATED OUTPUT								
Voltage	I_O = 5mA	10	12.5		*	*		V
Current	V_O = 10V	5	10 0		*	*		mA
Impedance			0 3			*		Ω
Capacitive Load			1000			*		pF
ANALOG INPUT CHARACTERISTICS								
Common-Mode Range		10			*			V
Absolute Maximum Voltage	No Damage			V_{CC}			*	V
Impedance, Differential			10^{10} || 3			*		Ω || pF
Common-Mode			10^{10} || 3			*		Ω || pF
OFFSET VOLTAGE (RTI)								
Initial Offset, max[3], G = 1			225	450		110	225	µV
G = 10			45	90		20	45	µV
G = 100			27	54		11	27	µV
G = 1000			25	50		10	25	µV
vs Temperature, G = 1			10	22		5	10	µV/°C
G = 10			2	4		0.75	1 5	µV/°C
G = 100			1	2		0 20	0 40	µV/°C
G = 1000			1	2		0.15	0 30	µV/°C
vs Time			1 + (20/G)			*		µV/mo
vs Supply	10 < V_{CC} < 18V		1 + (20/G)			*		µV/V
INPUT BIAS CURRENT								
Initial at 25°C	Each input		10	30		5	20	nA
vs Temperature			0 2			*		nA/°C
vs Supply			0 1			*		nA/V
Offset Current			10	30		5	20	nA
vs Temperature			0 5			*		nA/°C
COMMON-MODE REJECTION								
G = 1	DC to 60Hz,	80	95		*	*		dB
G = 10	1kΩ Source	96	110		*	*		dB
G = 100	Imbalance	106	120		*	*		dB
G = 1000		106	120		*	*		dB
INPUT NOISE[4]								
Input Voltage Noise, f_B = 0 1Hz to 10Hz			0 8			*		µV, p - p
Density, f_o = 10Hz			18			*		nV/√Hz
f_o = 100Hz			15			*		nV/√Hz
f_o = 1kHz			13			*		nV/√Hz
Input Current Noise, f_B = 0 1Hz to 10Hz			50			*		pA, p - p
Density, f_o = 10Hz			0.8			*		pA/√Hz
f_o = 100Hz			0 46			*		pA/√Hz
f_o = 1kHz			0.35			*		pA/√Hz
DYNAMIC RESPONSE								
±3dB Flatness	Small signal							
G = 1			500			*		kHz
G = 10			150			*		kHz
G = 100			30			*		kHz
G = 1000			2.4			*		kHz
±1% Flatness	Small signal							
G = 1			50			*		kHz
G = 10			25			*		kHz
G = 100			3			*		kHz
G = 1000			300			*		Hz

ELECTRICAL (CONT)

MODEL[1]		PGA200/201AG			PGA200/201BG			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
DYNAMIC RESPONSE								
±1% Flatness	Small signal							
G = 1			50			*		kHz
G = 10			25			*		kHz
G = 100			53			*		kHz
G = 1000			300			*		Hz
Full Power	G = 1 to 100		6.4			*		kHz
Slew Rate	G = 1 to 100	0.2	0.4			*		V/µsec
Settling Time (0.1%), G = 1			35			*		µsec
G = 10			35			*		µsec
G = 100			50			*		µsec
G = 1000			480			*		µsec
Settling Time (0.01%), G = 1			40			*		µsec
G = 10			40			*		µsec
G = 100			80			*		µsec
G = 1000[5]			670			*		µsec
Overload Recovery Time	50% overdrive							
G = 1 to 100			12			*		µsec
G = 1000			22			*		µsec
DIGITAL INPUT CHARACTERISTICS								
Input Low Threshold				0.8			*	V
Input Low Current				30			*	µA
Input High Threshold		2.4			*			V
Input High Current				30			*	µA
T_{WW}, Write Pulse Width		300			*			nsec
T_S, Data Setup Time		180			*			nsec
T_H, Data Hold Time		30			*			nsec
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range		10		18	*		*	V
Quiescent Current			±10	±12		*	*	mA
TEMPERATURE RANGE								
Specification		−40		+85	*		*	°C
Operating		−55		+125	*		*	°C
Storage		−55		+150	*		*	°C

*Specifications same as for PGA200/201AG.

NOTES (1) All specifications pertain to both PGA200 and PGA201. Values for gains of 10, 100, and 1000 for the PGA200 are the same for gains of 8, 64 and 512 (2) Measured with a 10kΩ load (3) Adjustable to zero This offset is the total offset including both input and output components referred to the input (4) Noise due to the input stage There is also an output component which becomes significant in low gain (see Typical Performance Curves). (5) Settling time of the average value of the output waveform since the noise floor in a gain of 1000 is on the order of 0.01% of full scale.

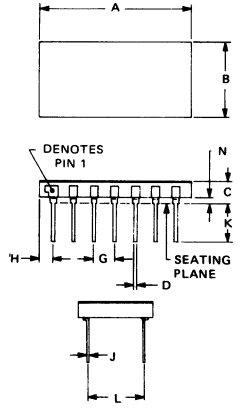
ABSOLUTE MAXIMUM RATINGS

Supply ..... ±18VDC
Internal Power Dissipation 600mW
Analog And Digital Inputs ..... ±V_{CC}
Operating Temperature Range ..... −55°C to +125°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering 10 Seconds) ..... +300°C
Output Short-Circuit Duration ..... Continuous To Ground
Junction Temperature ..... 175°C

PIN DESIGNATIONS

1	AO	8	Analog Common
2.	$\overline{WR}$	9	Output
3	−V_{CC}	10	Offset Trim
4.	Common-Mode Voltage	11.	Offset Trim
5.	NC	12.	+V_{CC}
6.	+IN	13.	Digital Common
7	−IN	14.	A1

MECHANICAL



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	770	810	19 56	20 57
B	480	500	12 19	12 70
C	155	215	3 94	5 46
D	016	020	41	51
G	100 BASIC		2 54 BASIC	
H	080	110	2 03	2 79
J	009	012	23	30
K	150	210	3 81	5 33
L	300 BASIC		7 62 BASIC	
N	015	035	38	89

BURN-IN SCREENING

Burn-in screening is an option available for the PGA200 and PGA201. Burn-in duration is 160 hours at +125°C (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

ORDERING INFORMATION

Model	Package	Temperature Range
PGA200AG	Ceramic DIP	-55°C to +125°C
PGA200BG	Ceramic DIP	-55°C to +125°C
PGA201AG	Ceramic DIP	-55°C to +125°C
PGA201BG	Ceramic DIP	-55°C to +125°C

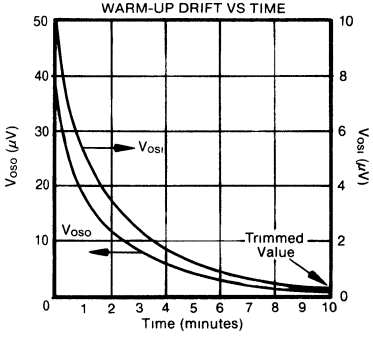
BURN-IN SCREENING OPTION
See text for details.

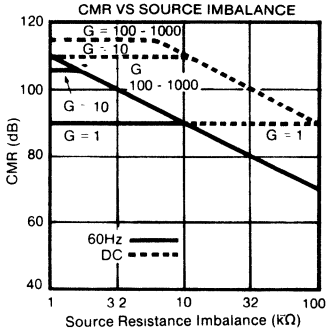
Model	Package	Burn-In Temp. (160h)[1]
PGA200AG-BI	Ceramic DIP	+125°C
PGA200BG-BI	Ceramic DIP	+125°C
PGA201AG-BI	Ceramic DIP	+125°C
PGA201BG-BI	Ceramic DIP	+125°C

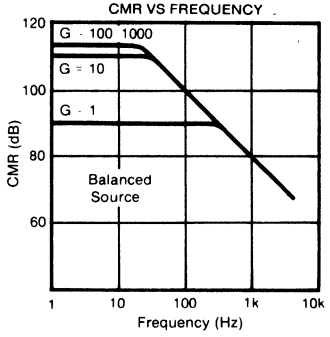
NOTE Or equivalent combination See text

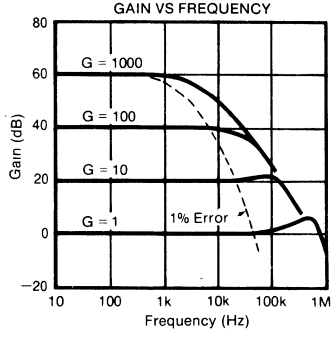
TYPICAL PERFORMANCE CURVES

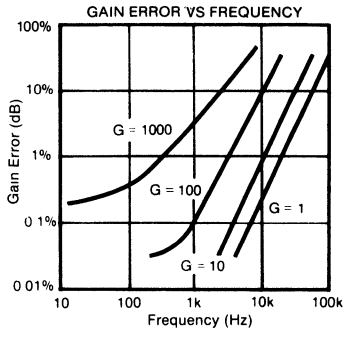
T_A = +25°C, $\pm V_{CC}$ = 15VDC, unless otherwise noted

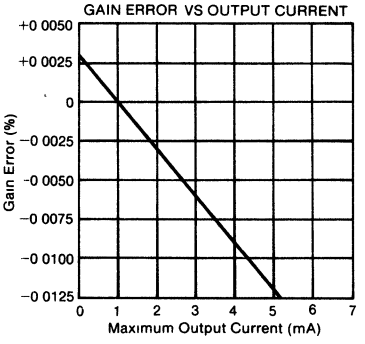


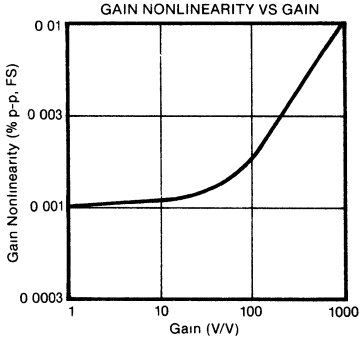


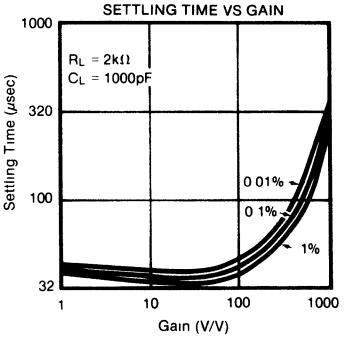


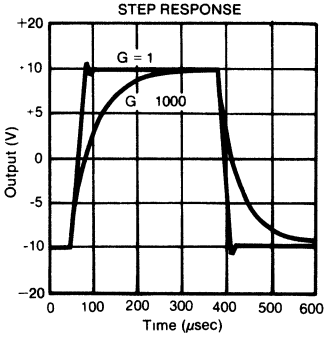


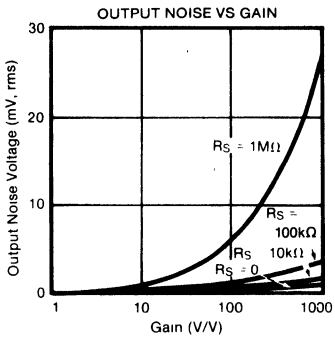


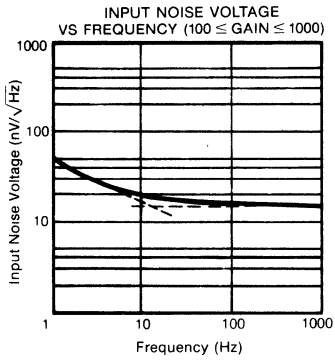


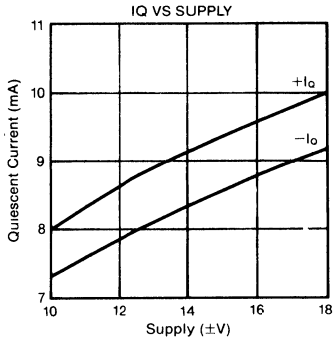












THEORY OF OPERATION

A simplified block diagram of the PGA200/201 appears on the first page. The diagram consists of three distinct parts. Together these parts form a high-perfomance, differential-input, digitally-programmable dedicated gain block. Each of the parts is optimized for a specific function.

The operational amplifiers are arranged on a monolithic substrate in the classical three-op-amp IA configuration. A nitride-passivated compatible thin-film bipolar process is used to achieve excellent offset and common-mode rejection stability over time and temperature. Advanced laser trimming techniques are used to minimize both the initial input offset and the input offset drift which are typically below 10μV and 0.15μ/V°C respectively. Additionally, careful layout techniques assure input stage thermal tracking with varying load conditions.

The gain-setting resistors are arranged on a separate substrate which is thermally isolated from the output stage. This results in minimum thermal interaction and a layout optimized for resistor tracking. All gains are dependent on the ratio of resistors which are composed of combinations of equal valued segments. The segmented approach provides the ultimate in accuracy and stability.

The latch and multiplexer, which set the gain, are implemented in CMOS. This provides high impedance logic inputs, low quiescent current and TTL compatibility without the need for a separate logic power supply. The logic threshold is internally derived from the $+V_{CC}$ power supply and is referenced to digital common. The circuit is arranged so that multiplexer ON resistance is in series with the high input impedance of the input amplifiers and hence contributes negligible gain error.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper analog and digital power supply connections. The analog supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors with connections made as close as possible to the amplifier supply terminals and load common connection.

Because the amplifier is direct-coupled, it must have a ground return path for the bias currents associated with the amplifier inputs at pins 6 and 7. If the ground return path is not inherent in the signal source (floating source), it must be provided externally. The ground return resistance (R_{gr}) should be kept as low as practical. The upper limit is approximately 50MΩ because of the input bias current of the amplifier and its common-mode voltage range.

In order to maintain linear operation of the input amplifiers the common-mode input voltage must be kept within the following limits:

$$-10V + (E_{in} \times G)/2 < E_{cm} < +10V - (E_{in} \times G)/2.$$

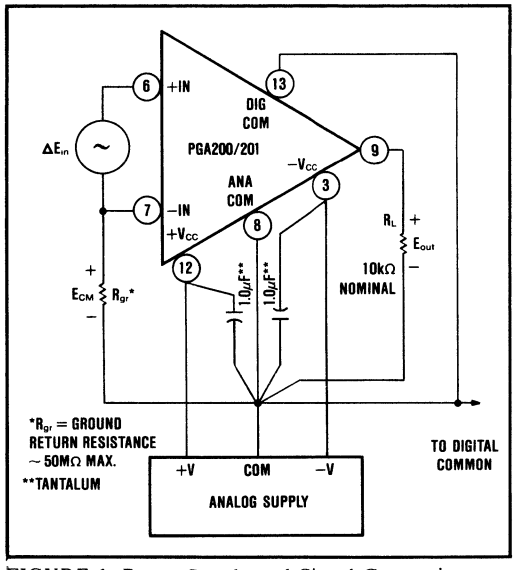


FIGURE 1. Power Supply and Signal Connections.

GAIN SETTING

Gain is determined by a 2-bit digital word applied to the A0 and A1 inputs (see Table I). The $\overline{WR}$ (pin 2) provides a latch function. When $\overline{WR}$ is a logic low, the latch is transparent and the gain directly follows the code on A0 and A1. When $\overline{WR}$ goes to a logic high, the gain is latched according to the previous state of A0 and A1. The timing requirements illustrated in Figure 2 must be observed. The minimum write pulse width is 300nsec while the data setup and hold times are 180nsec and 30nsec respectively. Although the logic inputs are TTL compatible, they are high impedance and the allowable logic high voltage extends to $+V_{CC}$.

Table I shows the gain select truth table. The gains for the PGA201 are shown in parenthesis.

TABLE I. Gain Select Truth Table.

A1	A0	$\overline{WR}$	GAIN PGA200 [PGA201]
X	X	⎍	Maintains previous gain
0	0	0	1 (1)
0	1	0	10 (8)
1	0	0	100 (64)
1	1	0	1000 (512)

Logic "1". $V_{AH} \geq 2.4V$
Logic "0" $V_{AL} \leq 0.8V$

INPUT AND OUTPUT OFFSETTING

Figure 3 illustrates the appropriate connections for offset adjustment. Since the instrumentation amplifier is a two-stage device, the total offset is composed of two parts, an input and an output component. Because both are actively laser trimmed, adjustment is not required in most applications. The input component is due to the mismatch in the offset voltage of the two input amplifiers and changes with gain. The output component is due to the offset of the second stage amplifier and is constant.

R_1 may be used to null the input offset. Its quality will affect the results; therefore, choose a potentiometer with good temperature and mechanical resistance stability. The wiper should be connected to $+V_{CC}$ at a point as close as possible to the $+V_{CC}$ terminal of the instrumentation amplifier. Null the offset as follows:

1. Set $E_1 = E_2 = 0$ (be sure a good ground return path exists to the inputs).
2. Set the gain to 1000 (or 512 for PGA201).
3. Adjust R_1 until the output reaches 0V ±1mV or desired value.

Input offset adjustment will affect the offset drift by approximately 3.1μV/°C/mV of offset that is trimmed. This effect can be greatly reduced by using the alternate offset adjust circuit shown inside the dashed line.

The output offset may be nulled or, alternately, the output can be level shifted with R_4. R_2 and R_3 divide the wiper voltage of R_4 down for increased sensitivity. Their ratio may be changed in order to increase the range of adjustment if desired. The buffer amplifier is required in order to keep the impedance at pin 8 low so that the gain and common-mode rejection will not be disturbed.

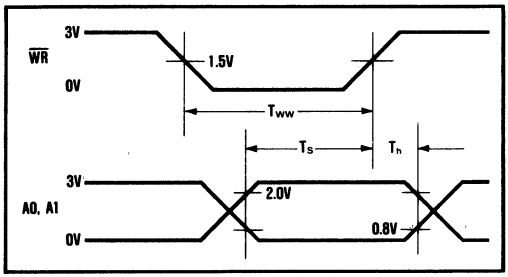


FIGURE 2. Timing Diagrams.

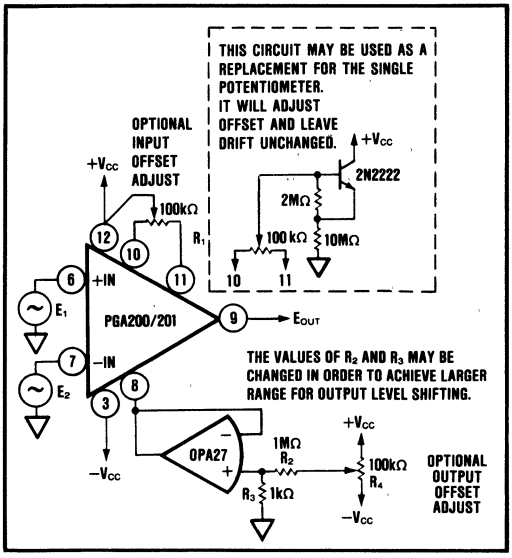


FIGURE 3. Optional Input/Output Offset Adjust.

GUARD DRIVE

Use of the guard drive connection in Figure 4 can improve system common-mode rejection when the

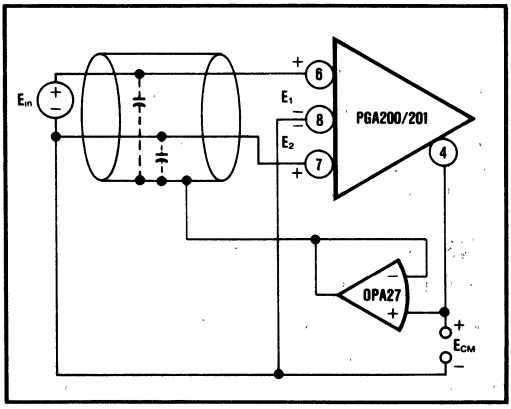


FIGURE 4. Guard Drive.

distributed capacitance of the input lines is significant. The common-mode voltage which appears on pin 4 is resistively derived from the output of the first stage amplifiers and has the value $(E_1 - E_2)/2$. This voltage is used to drive the shield which preferably should extend up to and around the input pins 6 and 7. This configuration improves common-mode rejection by reducing the common-mode current flow. The buffer amplifier is used in order to supply more current than the internal 20kΩ resistors can provide so that the guard can accurately track the actual common-mode voltage.

TYPICAL APPLICATIONS

The PGA200 and PGA201 are ideal for computer-controlled data acquisition systems as shown in Figure 5.

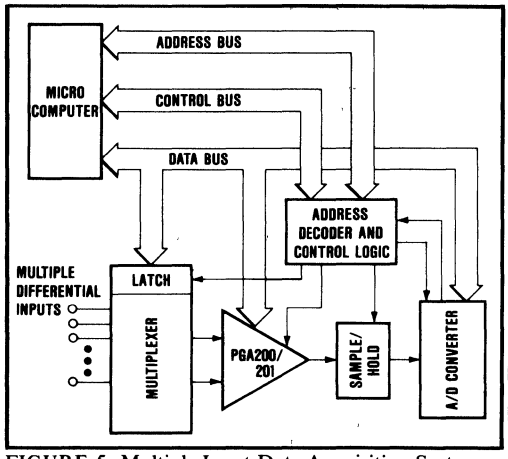


FIGURE 5. Multiple Input Data Acquisition System With Various Input Ranges.

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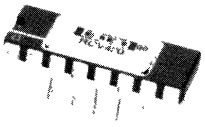


RCV420

ADVANCE INFORMATION
SUBJECT TO CHANGE

Precision 4mA to 20mA CURRENT LOOP RECEIVER

FEATURES

- COMPLETE 4-20mA to 0-5V CONVERSION
- INTEGRAL SENSE RESISTORS
- PRECISION 10V REFERENCE
- BUILT-IN LEVEL-SHIFTING
- ±40V COMMON-MODE INPUT RANGE
- 0.1% OVERALL CONVERSION ACCURACY
- HIGH NOISE IMMUNITY: 86dB CMR

APPLICATIONS

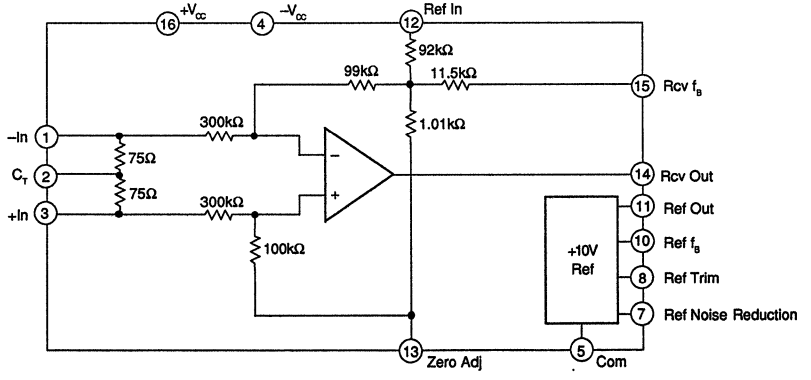
- PROCESS CONTROL
- INDUSTRIAL CONTROL
- FACTORY AUTOMATION
- DATA ACQUISITION
- SCADA
- RTUs
- ESD
- MACHINE MONITORING

DESCRIPTION

The RCV420 is a precision current-loop receiver designed to convert a 4-20mA input signal into a 0-5V output signal. As a monolithic circuit, it offers high reliability at low cost. The circuit consists of a premium grade operational amplifier, an on-chip precision resistor network, and a precision 10V reference. The RCV420 features 0.1% overall conversion accuracy, 86dB CMR, and ±40V common-mode input range.

The circuit introduces only a 1.5V drop at full scale, which is useful in loops containing extra instrument burdens or in intrinsically safe applications where transmitter compliance voltage is at a premium. The 10V reference provides a precise 10.00V output with a typical drift of 10ppm/°C.

The RCV420 is completely self-contained and offers a highly versatile function. No adjustments to gain, offset, and CMR are needed. This provides three important advantages over discrete, board-level designs: 1) lower initial design cost, 2) lower manufacturing cost, and 3) easy, cost-effective field repair of a precision circuit.



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PDS-837

SPECIFICATIONS

ELECTRICAL

T = 25°C and $\pm V_{cc}$ = ±15V unless otherwise noted.

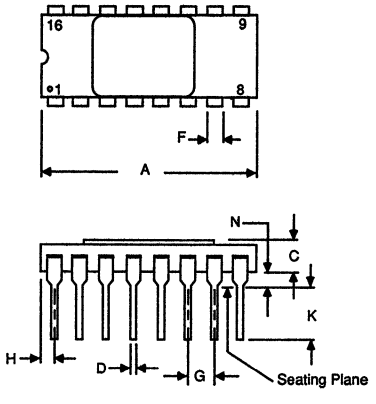
	AG			BG			KP			
CHARACTERISTICS	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
GAIN										
Initial		0.3125			*			*		V/mA
Error		.015	0.05		*	0.025		*	*	%
vs Temp		15	50.0		*	25.0		*		ppm/°C
Nonlinearity[1]		0.0002	0.001		*	*		*	*	%
OUTPUT										
Rated Voltage (I_o = +10, –5mA)	10	12		*	*		*	*		V
Rated Current (E_o = 10V)	+10,–5			*			*			mA
Impedance (Differential)		0.01			*			*		Ω
Current Limit (To Common)		+49,–13			*			*		mA
Capacitive Load (Stable Operation)		1000			*			*		pF
INPUT										
Sense Resistance	74.25	75	75.75	*	*	*	*	*	*	Ω
Input Impedance (Common Mode)		200			*			*		kΩ
Common Mode Voltage			±40			*			*	V
CMR[2]	74	80		86	94		*	*		dB
vs Temp (DC) (T_A = T_{MIN} to T_{MAX})	66	75		80	90			*		dB
AC 60Hz		80			94			*		dB
OFFSET VOLTAGE (RTO)[3]										
Initial			1			*			*	mV
vs Temp		15	50		*	25		*		µV/°C
vs Supply (±11.4V to ±18V)	74	90		80	*		*	*		dB
vs Time		200			*			*		µV/mo
ZERO ERROR[4]										
Initial		0.02	0.05		*	0.025		*	*	%
vs Temp		20	60		*	30		*		ppm/°C
OUTPUT NOISE VOLTAGE										
f_B = 0.1Hz to 10Hz		50			*			*		µVp-p
f_O = 10kHz		800			*			*		nV/√Hz
DYNAMIC RESPONSE										
Gain Bandwidth		150			*			*		kHz
Full Power Bandwidth		30			*			*		kHz
Slew Rate		1.5			*			*		V/µs
Settling Time (.01%)		10			*			*		µs
VOLTAGE REFERENCE										
Output Voltage										
Initial	9.995		10.005	*		*	*		*	V
Trim Range[5]		±5			*			*		%
vs Temp[6]		10	20		*	*		*		ppm/°C
vs Supply (±11.4V to ±18V)		.0005			*			*		%/V
vs Output Current (I_o = 0 to +10mA)		.0005			*			*		%/mA
vs Time		25			*			*		ppm/1kh
Noise (0.10Hz to 10Hz)		10			*			*		µVp-p
Output Current	+10,–2			*			*			mA
POWER SUPPLY										
Rated		±15			*			*		V
Voltage Range[7]	±11.4		±18	*		*	*		*	V
Quiescent Current (V_o = 0V)		3	4		*	*		*	*	mA
TEMPERATURE RANGE										
Specification	–25		+85	*		*	0		+70	°C
Operation	–55		+125	*		*	–25		+85	°C
Storage	–65		+150	*		*	–40		+85	°C

*Specification same as RCV420AG.

NOTES: (1) Nonlinearity is the max peak deviation from best fit straight line. (2) With 0 source impedance on Zero Adj pin. (3) With all inputs grounded including Ref In. (4) With 4mA input signal and Voltage Reference connected (includes V_{os}, Gain Error, and Voltage Reference Errors). (5) External trim slightly affects drift. (6) The "box method" is used to specify output voltage drift vs temperature. (7) I_o Ref = 5mA, I_o Rcv = 2mA.

MECHANICAL

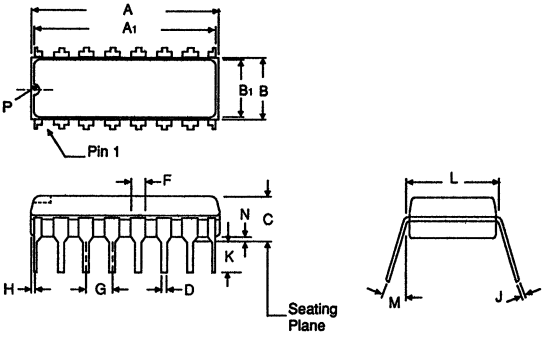
G Package —16-Pin Hermetic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

P Package—16 Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.740	.800	18.80	20.32
A1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.20	0.50	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ORDERING INFORMATION

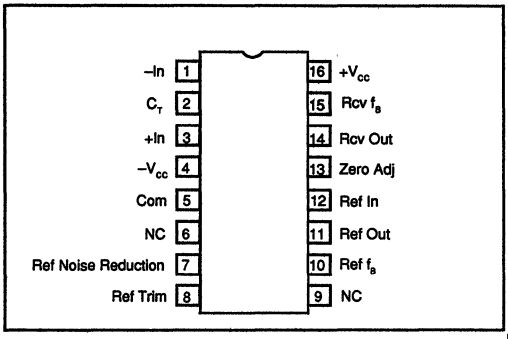
RCV420 X X

- Basic Model Number
- Performance Grade
  - A, B: –25°C to +85°C
  - K: 0°C to +70°C
- Package Code
  - G: 16-pin Hermetic DIP
  - P: 16-pin Plastic DIP

ABSOLUTE MAXIMUM RATINGS

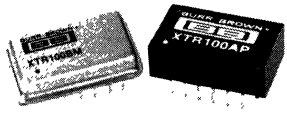
Supply	±22V
Input Current, Continuous	40mA
Input Current Momentary, 0.1s	250mA, 1% Duty Cycle
Common Mode Input Voltage, Continuous	±40V
Common Mode Input Voltage, Momentary, 10s	±100V
Operating Temperature Range:	
G Package:	–55°C to +125°C
P Package:	–25°C to +85°C
Storage Temperature Range:	
G Package:	–65°C to +150°C
P Package:	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Common (Rcv & Ref)	Continuous

PIN CONFIGURATION



BURR-BROWN®

XTR100



Precision, Low Drift 4mA to 20mA TWO-WIRE TRANSMITTER

FEATURES

- INSTRUMENTATION AMPLIFIER INPUT
  - Low Offset Voltage, 25μV max
  - Low Voltage Drift, 0.5μV/°C max
  - Low Nonlinearity, 0.01% max
- TRUE TWO-WIRE OPERATION
  - Power and Signal on One Wire Pair
  - Current Mode Signal Transmission
  - High Noise Immunity
- DUAL MATCHED CURRENT SOURCES
- WIDE SUPPLY RANGE, 11.6V to 40V
- -40°C TO +85°C SPECIFICATION RANGE
- SMALL 14-PIN DIP PACKAGE

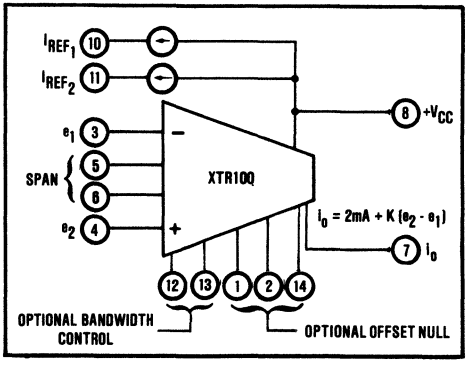
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  - Pressure Transmitters
  - Temperature Transmitters
  - Millivolt Transmitters
- RESISTANCE BRIDGE INPUTS
- THERMOCOUPLE INPUTS
- RTD INPUTS
- CURRENT SHUNT (mV) INPUTS
- AUTOMATED MANUFACTURING
- POWER PLANT/ENERGY SYSTEM MONITORING

DESCRIPTION

The XTR100 is a microcircuit, 4mA to 20mA, two-wire transmitter containing a high accuracy instrumentation amplifier (IA), a voltage controlled output current source, and dual-matched precision current references. This combination is ideally suited for remote signal conditioning of a wide variety of transducers such as thermocouples, RTD's, thermistors, and strain gauge bridges. State-of-the art design and laser-trimming, wide temperature range operation and small size make it very suitable for industrial process control applications.

The two-wire transmitter allows signal and power to be supplied on a single wire-pair by modulating the power supply current with the input signal source. The transmitter is immune to voltage drops from long runs and noise from motors, relays, actuators, switches, transformers, and industrial equipment. It can be used by OEMs producing transmitter modules or by data acquisition system manufacturers. Also, the XTR100 is generally very useful for low noise, current-mode signal transmission.



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PDS-467C

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, +V_{CC} = 24VDC, R_L = 100Ω unless otherwise noted.

PARAMETER	CONDITIONS/DESIGNATION	XTR100AM/AP MIN	XTR100AM/AP TYP	XTR100AM/AP MAX	XTR100BM/BP MIN	XTR100BM/BP TYP	XTR100BM/BP MAX	UNITS
OUTPUT AND LOAD CHARACTERISTICS								
Current	Linear Operating Region	4		20	*		*	mA
Current	Derated Performance	3.8		22	*		*	mA
Current Limit	I_O min		28	38		*	*	mA
Offset Current Error	I_{OS}, I_O = 4mA		±1.5	±4		*	*	µA
Offset Current Error vs Temp	$\Delta I_{OS}/\Delta T$		±5	±10		*	*	ppm, FS/°C
Full Scale Output Current Error	Full Scale = 20mA			±20			*	µA
Power Supply Rejection		110	135		*	*		dB
Power Supply Voltage	V_{CC}, pins 7 & 8, compliance(1)	+11.6		+40	*		*	VDC
Load Resistance	At V_{CC} = +24V, I_O = 20mA			600			*	Ω
	At V_{CC} = +40V, I_O = 20mA			1400			*	Ω
SPAN								
Equation	R_S in Ω, e_1 and e_2 in V	$I_O = 4mA + [0.016\Omega + (40/R_S)](e_2 - e_1)$						
Untrimmed Error(2)	ϵ_{SPAN}	-5	-2.5	0	*	*	*	%
Nonlinearity	$\epsilon_{NONLINEARITY}$			0.01			*	%
Hysteresis			0			*		%
Dead Band			0			*		%
Temperature Effects			30	±100		*	*	ppm %/°C
INPUT CHARACTERISTICS								
Impedance								
Differential			0.4 ‖ 0.047			*		GΩ ‖ µF
Common-Mode			10 ‖ 180			*		GΩ ‖ pF
Voltage Range, Full Scale	$\Delta e = (e_2 - e_1)$(3)	0		1	*		*	V
Offset Voltage	V_{OS}			±50			±25	µV
vs Temperature	$\Delta V_{OS}/\Delta T$		±0.7	±1		±0.25	±0.5	µV/°C
Bias Current	I_B		60	150		*	*	nA
vs Temperature	$\Delta I_B/\Delta T$		0.30	1		*	*	nA/°C
Offset Current	I_{OSI}		10	±30		*	±20	nA
vs Temperature	$\Delta I_{OSI}/\Delta T$		0.1	0.3		*	*	nA/°C
Common-Mode Rejection(4)	DC	90	100		*	*	*	dB
Common-Mode Range	e_1 and e_2 with respect to pin 7	4		6	*		*	V
CURRENT SOURCES								
Magnitude			1			*		mA
Accuracy	V_{CC} = 24V, $V_{PIN\ 8} - V_{PIN\ 10, 11}$ = 19V, R_2 = 5kΩ, Fig 3		±0.03	±0.1		±0.015	±0.05	%
vs Temperature				±30			*	ppm/°C
vs Time			±8			*		ppm/mo.
Ratio Match	Tracking							
Accuracy	1 - I_{REF1}/I_{REF2}		±0.006	±0.02			*	%
vs Temperature				±15			10	ppm/°C
vs Time			±1			*		ppm/mo
Output Impedance		10	20		*			MΩ
TEMPERATURE RANGE								
Specification		-40		+85	*		*	°C
Operating (AM, BM)		-55		+125	*		*	°C
(AP, BP)		-40		+85	*		*	°C
Storage (AM, BM)		-55		+165	*		*	°C
(AP, BP)		-40		+85	*		*	°C

*Same as XTR100AM/AP

NOTES

1 See Typical Performance Curves

2. Span error shown is untrimmed and may be adjusted to zero

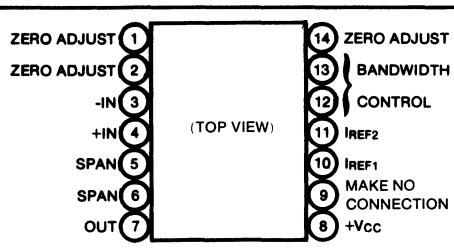
3. e_1 and e_2 are signals on the -IN and +IN terminals with respect to the output, pin 7. While the maximum permissible Δe is 1V, it is primarily intended for much lower input signal levels, e.g., 10mV or 50mV full scale for the XTR100A and XTR100B grades respectively. 2mV FS is also possible with the B grade; but accuracy will degrade due to possible errors in the low value span resistance and very high amplification of offset, drift, and noise.

4. Offset voltage is trimmed with the application of a 5V common-mode voltage. Thus the associated common-mode error is removed See Application Information section.

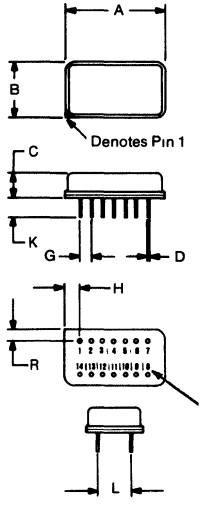
ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC}	40V
Input Voltage, e_1, or e_2	≥ V_{OUT}, ≤ +V_{CC}
Storage Temperature Range, metal	-55°C to +165°C
Storage Temperature Range, plastic	-40°C to +85°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-circuit Duration	Continuous to ground
Junction Temperature	+165°C

PIN DESIGNATIONS



MECHANICAL



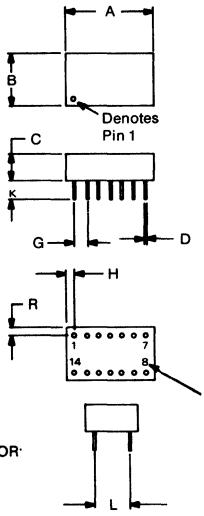
XTR100AM/BM (Metal)

NOTE Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

Pin numbers shown for reference only. Numbers are not marked on package.

MATING CONNECTOR: 0145MC



XTR100AP/BP (Plastic)

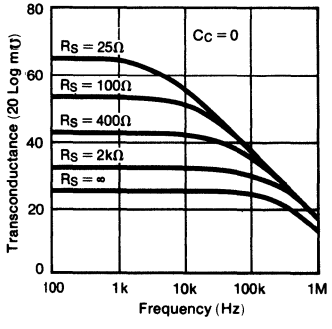
NOTE Leads in true position within 0.10" (0.25mm) R at MMC at seating plane

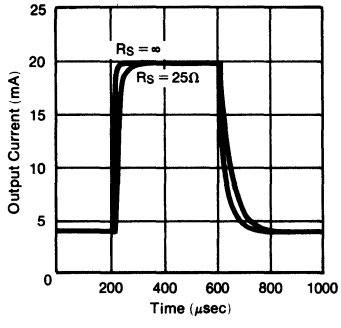
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.210	4.83	5.33
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

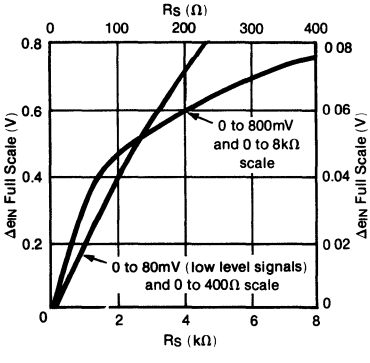
Pin numbers shown for reference only Numbers are not marked on package

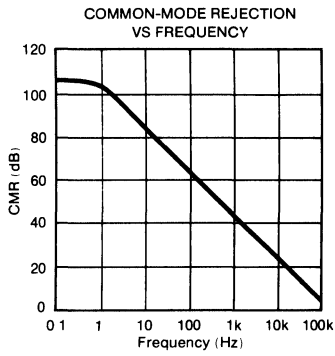
TYPICAL PERFORMANCE CURVES

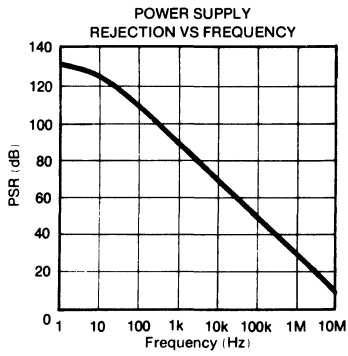
(T_A = +25°C, +V_{CC} = 24VDC unless otherwise noted)

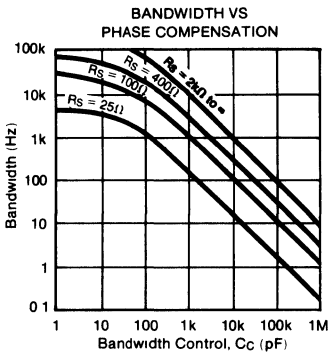


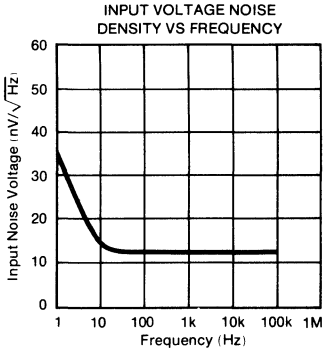


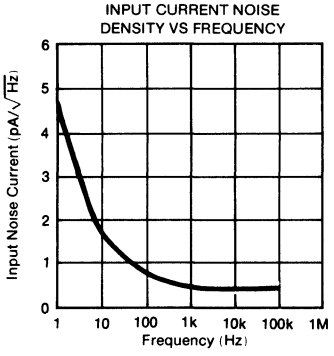


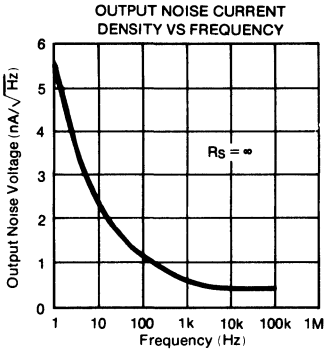












THEORY OF OPERATION

A simplified schematic of the XTR100 is shown in Figure 1. Basically the amplifiers, A_1 and A_2, act as an instrumentation amplifier controlling a current source, A_3 and Q_1. Operation is determined by an internal feedback loop. e_1 applied to pin 3 will also appear at pin 5 and similarly e_2 will appear at pin 6. Therefore the current in R_S, the span setting resistor, will be $I_S = (e_2 - e_1)/R_S = e_{IN}/R_S$. This current combines with the current, I_3, to form I_1. The circuit is configured such that I_2 is 19 times I_1. From this point the derivation of the transfer function is straightforward but lengthy. The result is shown in Figure 1.

Examination of the transfer function shows that I_O has a lower range-limit of 4mA when $e_{IN} = e_2 - e_1 = 0V$. This 4mA is composed of 2mA quiescent current exiting pin 7 plus 2mA from the current sources. The upper range limit of I_O is set to 20mA by the proper selection of R_S based on the upper range limit of e_{IN}. Specifically R_S is chosen for a 16mA output current span for the given full scale input voltage span; i.e., $(0.016\Omega + 40/R_S)(e_{IN}$ full scale$) = 16mA$. Note that since I_O is unipolar e_2 must be kept larger than e_1; i.e., $e_2 \geq e_1$ or $e_{IN} \geq 0$. Also note that in order not to exceed the output upper range limit of 20mA, e_{IN} must be kept less than 1V when $R_S = \infty$ and proportionately less as R_S is reduced.

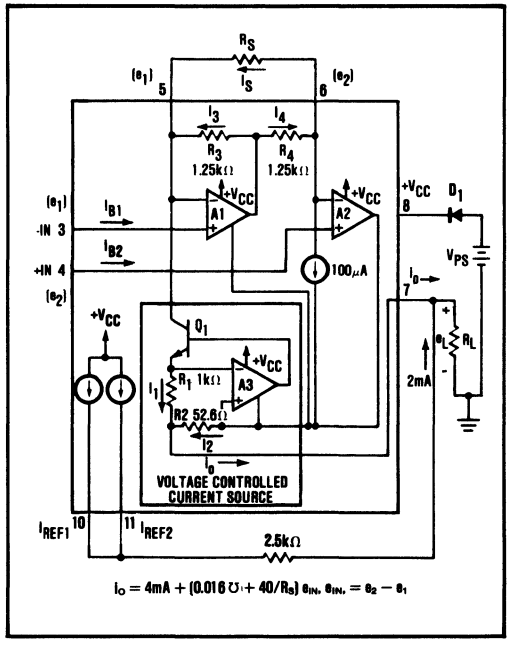


FIGURE 1. Simplified Schematic of the XTR100.

INSTALLATION AND OPERATING INSTRUCTIONS

Major points to consider when designing with the XTR100:

1. The leads to R_S should be kept as short as possible to reduce noise pick-up and parasitic resistance.
2. $+V_{CC}$ should be bypassed with a 0.01μF capacitor as close to the unit at possible (pin 8 to 7).
3. Always keep the input voltages within their range of linear operation
$$+4V \leqslant e_1 \leqslant +6V$$
$$+4V \leqslant e_2 \leqslant +6V$$
(e_1 and e_2 measured with respect to pin 7).
4. The maximum input signal level ($e_{IN_{FS}}$) is 1V with $R_S = \infty$ and proportionally less as R_S decreases.
5. Always return the current references (pins 10 and 11) to the output (pin 7) through an appropriate resistor. If the references are not used for biasing or excitation connect them together and through a 1kΩ resistor to pin 7. Each reference must have between +1V and +(V_{CC} -4V) with respect to pin 7. Filter with one 0.01μF or two 0.0047μF capacitors.
6. Always choose R_L (including line resistance) so that the voltage between pins 7 and 8 ($+V_{CC}$) remains within the 11.6V to 40V range as the output changes between the 4mA to 20mA range (see Figure 2).
7. It is recommended that a reverse polarity protection diode (D_1 in Figure 1) be used. This will prevent damage to the XTR100 caused by momentary (e.g., transient) or long term application of the wrong polarity of voltage between pins 7 and 8.
8. When the XTR100 is in high gain, use a compensation capacitor, pins 12 and 13, and consider PC board layout which minimizes parasitic capacitance.

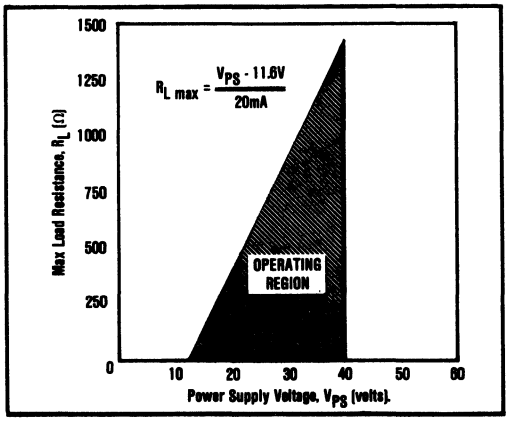


FIGURE 2. Power Supply Operating Range.

SELECTING R_S

R_{SPAN} is chosen so that a given full scale input span $e_{IN_{FS}}$ will result in the desired full scale output span of ΔI_{OFS},

$[(0.016\text{Ω}) + (40/R_S)]\ \Delta e_{IN} = \Delta I_O = 16mA.$

Solving for R_S;

$$R_S = \frac{40}{\Delta I_O/\Delta e - 0.016\text{Ω}} \quad (1)$$

For example, if $\Delta e_{IN_{FS}} = 100mV$ for $\Delta I_{o_{FS}} = 16mA$

$$R_S = \frac{40}{(16mA/100mV)} = \frac{40}{0.16 - 0.016} = \frac{40}{0.144} = 278\Omega$$

See Typical Performance Curves for a plot of R_S vs $\Delta e_{IN_{FS}}$. Note that in order not to exceed the 20mA upper range limit e_{IN} must be less than 1V when $R_S = \infty$ and proportionately smaller as R_S decreases.

BIASING THE INPUTS

The internal circuitry of the XTR100 is such that both e_1 and e_2 must be kept approximately 5V above the voltage at pin 7. This is easily done by using one or both current sources and an external resistor R_2. Figure 3 shows the simplest case - a floating voltage source e'_2. The 2mA from the current sources flows through the 2.5kΩ value of R_2 and both e_1 and e_2 are raised by the required 5V with respect to pin 7. For linear operation the constraint is

$$+4V \leqslant e_1 \leqslant +6V$$
$$+4V \leqslant e_2 \leqslant +6V$$

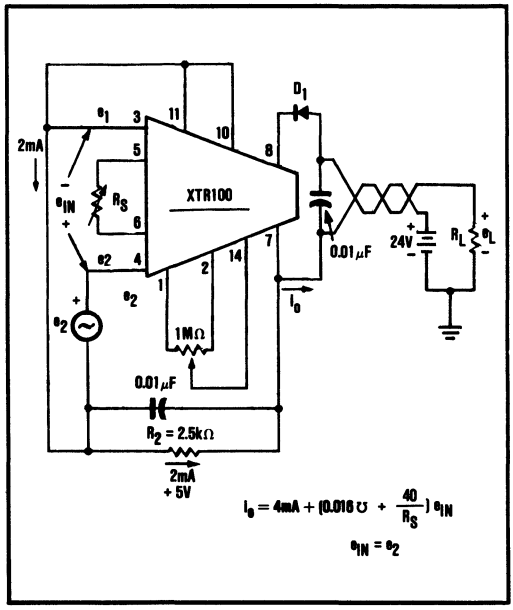


FIGURE 3. Basic Connection for Floating Voltage Source.

Figure 4 shows a similar connection for a resistive transducer. The transducer could be excited either by one (as shown) or both current sources.

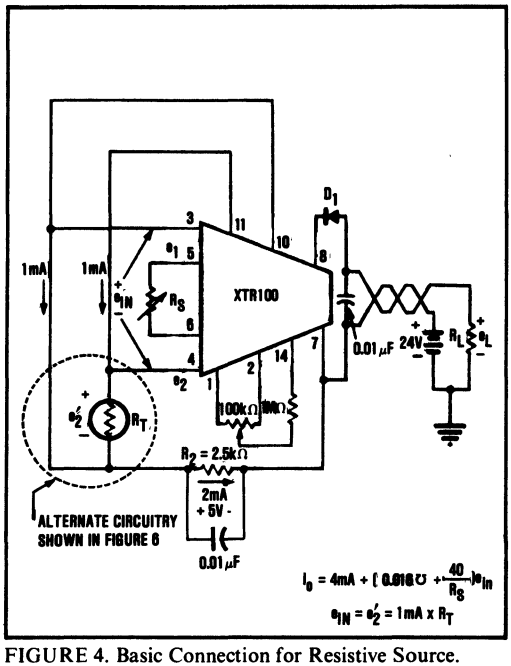


FIGURE 4. Basic Connection for Resistive Source.

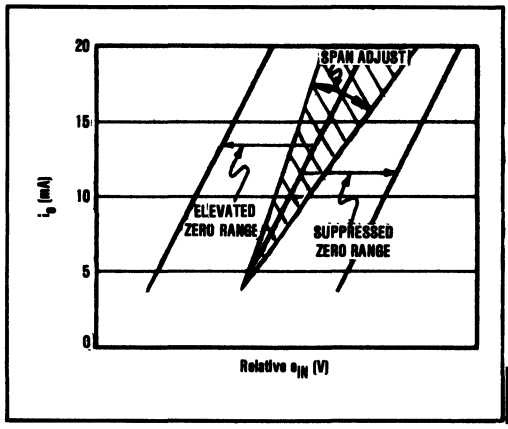


FIGURE 5. Elevation and Suppression Graph.

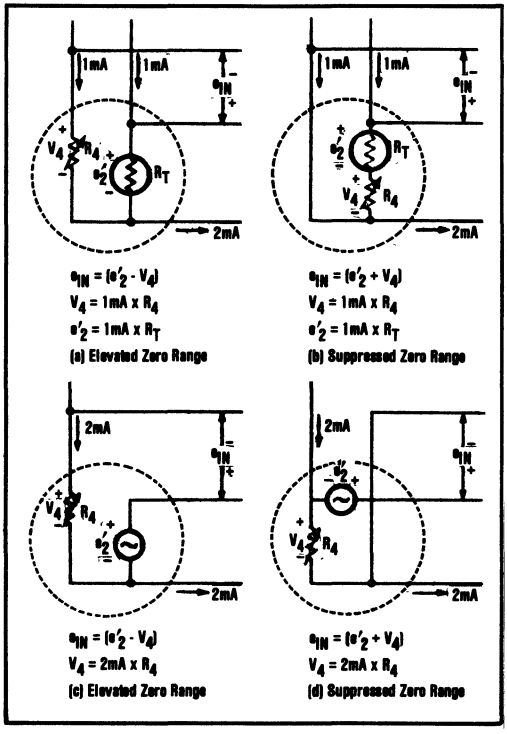


FIGURE 6. Elevation and Suppression Circuits.

CMV AND CMR

Thus the XTR100 is designed to operate with a nominal 5V common-mode voltage at the input and will function properly with either input operating over the range of 4V to 6V with respect to pin 7. The error caused by the 5V CMV is already included in the accuracy specifications. If the inputs are biased at some other CMV then an input offset error term is (CMV - 5)/CMRR; CMR is in dB, CMRR is in V/V.

SIGNAL SUPPRESSION AND ELEVATION

In some applications it is desired to have suppressed zero range (input signal elevation) or elevated zero range (input signal suppression). This is easily accomplished with the XTR100 by using the current sources to create the suppression/elevation voltage. The basic concept is shown in Figures 5 and 6(a). In this example the sensor voltage is derived from R_T (a thermistor, RTD or other variable resistance element) excited by one of the 1mA current sources. The other current source is used to create the elevated zero range voltage. Figures 6(b), (c) and (d) show some of the possible circuit variations. These circuits have the desirable feature of noninteractive span and suppression/elevation adjustments. Note: It is not recommended to use the optional offset voltage null (pins 1, 2, and 14) for elevation/suppression. This trim capability is used only to null the amplifier's input offset voltage. In many applications the already low offset voltage (typically 20μV) will not need to be nulled at all. Adjusting the offset voltage to nonzero values will disturb the voltage drift by ±0.3μV/°C per 100μV of induced offset.

APPLICATION INFORMATION

The small size, low offset voltage and drift, excellent linearity, and internal precision current sources, make the XTR100 ideal for a variety of two-wire transmitter applications. It can be used by OEM's producing different types of transducer transmitter modules and by data acquisition systems manufacturers who gather transducer data. Current mode transmission greatly reduces noise

interference. The two-wire nature of the device allows economical signal conditioning at the transducer. Thus the XTR100 is, in general, very suitable for individualized and special purpose applications.

EXAMPLE 1 - RTD Transducer shown in Figure 7. Given a process with temperature limits of +25°C and +150°C, configure the XTR100 to measure the temperature with a platinum RTD which produces 100Ω at 0°C and 200Ω at +266°C (obtained from standard RTD tables). Transmit 4mA for +25°C and 20mA for +150°C.

Computing R_S.

The sensitivity of the RTD is $\Delta R/\Delta T = 100\Omega/266°C$. When excited with a 1mA current source for a 25°C to 150°C range (i.e., 125°C span) the span of e_{IN} is 1mA x (100Ω/266°C) x 125°C = 47mV = Δe_{IN}.

From equation 1, $$R_S = \frac{40}{\frac{\Delta I_O}{\Delta e_{in}} - 0.016\,\mho}$$

$$R_S = \frac{40}{\frac{16mA}{47mV} - 0.016\,\mho} = \frac{40}{0.3244} = 123.3\Omega$$

Span adjustment (calibration) is accomplished by trimming R_S.

Computing R_4:

At 25°C, $e'_2 = 1mA \times [100\Omega + (\frac{100\Omega}{266°C} \times 25°C)]$

$= 1mA \times 109.4\Omega$

$= 109.4mV$

In order to make the lower range limit of 25°C correspond to the output lower range limit of 4mA the input circuitry shown in Figure 7 is used.

e_{IN} is made 0 at 25°C

or $e'_{2\,25°C} - V_4 = 0$

thus, $V_4 = e'_{2\,25°C} = 109.4mV$

$$R_4 = \frac{V_4}{1mA} = \frac{109.4mV}{1mA} = 109.4\Omega$$

Computing R_2 and checking CMV:

At 25°C, $e'_2 = 109.4mV$

At 150°C, $e'_2 = 1mA \times [100\Omega + (\frac{100\Omega}{266°C} \times 150°C)]$

$= 156.4mV$

Since both e'_2 and V_4 are small relative to the desired 5V common-mode voltage they may be ignored in computing R_2 as long as the CMV is met.

$R_2 = 5V/2mA = 2.5k\Omega$

e_2 min = 5V + 0.1094V
e_2 max = 5V + 0.1564V
e_1 = 5V + 0.1094V

The +4V to +6V CMV requirement is met.

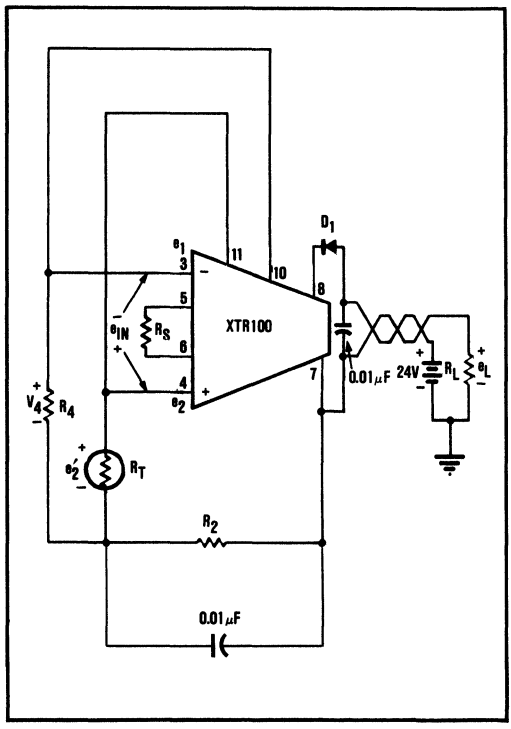


FIGURE 7. Circuit for Example 1.

EXAMPLE 2 - Thermocouple Transducer shown in Figure 8. Given a process with temperature (T_1) limits of 0°C and +1000°C, configure the XTR100 to measure the temperature with a type J thermocouple that produces a 58mV change for 1000°C change. Use a semiconductor diode for a cold junction compensation to make the measurement relative to 0°C. This is accomplished by supplying a compensating voltage, V_{R6}, equal to that normally produced by the thermocouple with its "cold junction" (T_2) at ambient. At a typical ambient of +25°C this is 1.28mV (obtained from standard thermocouple tables with reference junction of 0°C). Transmit 4mA for T_1 = 0°C and 20mA for T_1 = +1000°C. Note: $e_{IN} = e_2 - e_1$ indicates that T_1 is relative to T_2.

Establishing R_S:

The input full scale span is 58mV ($\Delta e_{IN_{FS}} = 58mV$).

R_S is found from equation (1)

$$R_S = \frac{40}{\frac{\Delta I_O}{\Delta e_{IN}} - 0.016\,\mho}$$

$$= \frac{40}{\frac{16mA}{58mV} - 0.016\,\mho} = \frac{40}{0.2599}$$

$R_S = 153.9\Omega$

Selecting R_4:

R_4 is chosen to make the output 4mA at $T_{TC} = 0°C$ (V_{TC} = -1.28mV) and $T_D = 25°C$ ($V_D = 0.6V$). A circuit is shown in Figure 8.

V_{TC} will be -1.28mV when $T_{TC} = 0°C$ and the reference junction is at +25°C. e_1 must be computed for the condition of $T_D = +25°C$ to make $e_{IN} = 0V$.

$V_{D_{25°C}}$ = 600mV.
$e_{1_{25°C}}$ = 600mV x 51/2051 = 14.9mV
$e_{IN} = e_2 - e_1 = + V_{TC} + V_4 - e_1$
with e_{IN} = 0 and V_{TC} = -1.28mV
$V_4 = e'_1 + e_{IN} - V_{TC}$ = 14.9mV + 0V -(-1.28mV)
1mA x R_4 = 16.18mV
R_4 = 16.18Ω

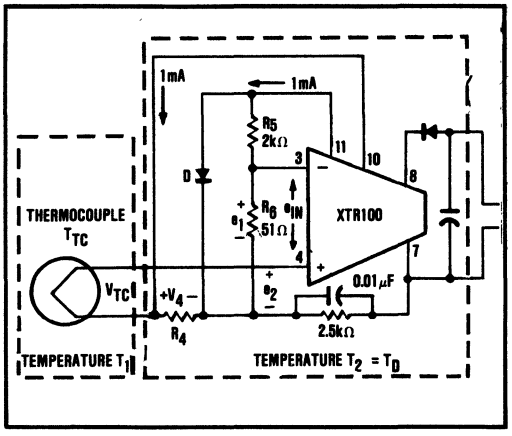


FIGURE 8. Thermocouple Input Circuit with Two Temperature Regions and Diode (D) Cold Junction Compensation.

Cold Junction Compensation:

The temperature reference circuit is shown in Figure 9.

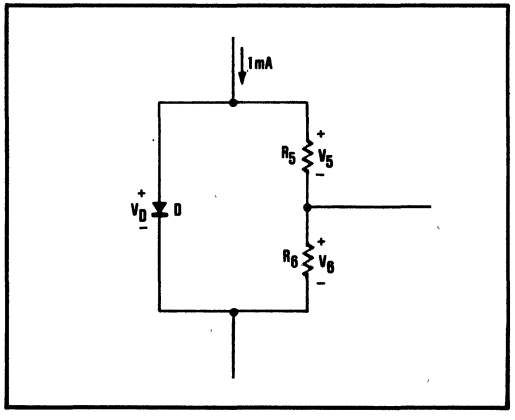


FIGURE 9. Cold Junction Compensation Circuit.

The diode voltage has the form

$$V_D = \frac{KT}{q} \ln \frac{I_{DIODE}}{I_{SAT}}$$

Typically at T_2 = 25°C, V_D = 0.6V and $\Delta V_D/\Delta T$ = -2mV/°C. R_5 and R_6 form a voltage divider for the diode voltage V_D. The divider values are selected so that the gradient $\Delta V_D/\Delta T$ equals the gradient of the thermocouple at the reference temperature. At 25°C this is approximately 52μV/°C (obtained from standard thermocouple table) therefore,

$$\Delta V_{TC}/\Delta T = \Delta V_D/\Delta T \left(\frac{R_6}{R_5 + R_6}\right) \quad (2)$$

$$52\mu V/°C = 2000\mu V/°C \left(\frac{R_6}{R_5 + R_6}\right)$$

R_5 is chosen as 2kΩ to be much larger than the resistance of the diode. Solving for R_6 yields 51Ω.

THERMOCOUPLE BURN-OUT INDICATION

In process control applications it is desirable to detect when a thermocouple has burned out. This is typically done by forcing the two-wire transmitter current to either limit when the thermocouple impedance goes very high. The circuits of Figures 14 and 15 inherently have down scale indication. When the impedance of the thermocouple gets very large (open) the bias current flowing into the +input (large impedance) will cause I_O to go to its lower range limit value (about 3.8mA). If up scale indication is desired the circuit of Figure 16 should be used. When the TC opens the output will go to its upper range limit value (about 25mA or higher).

OPTIONAL INPUT OFFSET VOLTAGE TRIM

The XTR100 has provisions for nulling the input offset voltage associated with the input amplifiers. In many applications the already low offset voltage (25μV max for the B grade, 50μV max for the A grade) will not need to be nulled at all. The null adjustment can be done with a potentiometer at pins 1, 2, and 14 as shown in Figures 3 and 4. Either of these two circuits may be used. NOTE: It is not recommended to use this input offset voltage nulling capability for elevation or suppression. See the Signal Suppression and Elevation section for the proper techniques.

OPTIONAL BANDWIDTH CONTROL

Low-pass filtering is recommmended where possible and can be done by either one of two techniques shown in Figure 10. C_2 connect to pins 3 and 4 will reduce the bandwidth with a cutoff frequency given by,

$$f_{CO} = \frac{1.59 \times 10}{(R_1 + R_2 + R_3 + R_4)(C_2 + 0.047\mu F)}$$

with f_{CO} in Hz, all R_S in Ω and C_2 in μF. This method has the disadvantage of having f_{CO} vary with R_1, R_2, R_3, R_4, and it may require large values of R_3 and R_4. The other method, using C_1 will use smaller values of capacitance and is not a function of the input resistors. It is however, more subject to nonlinear distortion caused by slew rate limiting. This is normally not a problem with the slow signals associated with most process control transducers. The relationship between C_1 and f_{CO} is shown in the Typical Performance Curves.

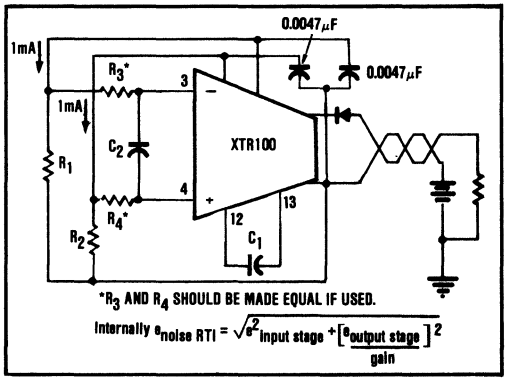


FIGURE 10. Optional Filtering.

APPLICATION CIRCUITS

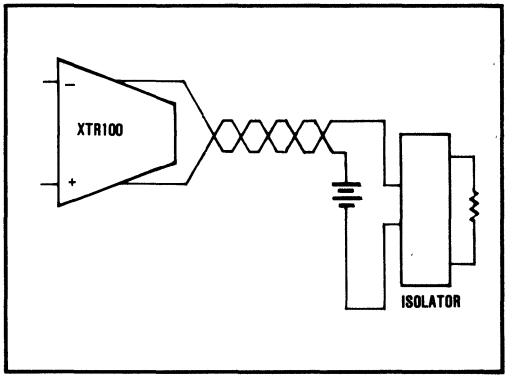


FIGURE 11. XTR100 with Loop-powered Isolation.

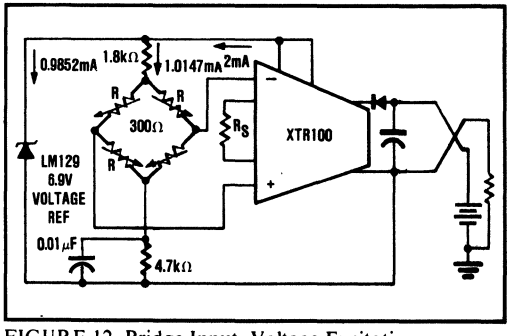


FIGURE 12. Bridge Input, Voltage Excitation.

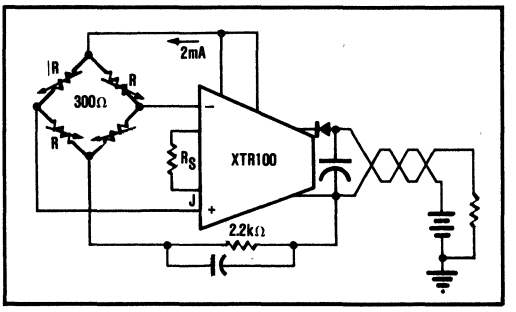


FIGURE 13. Bridge Input, Current Excitation.

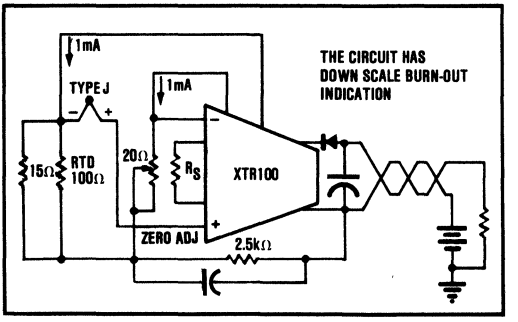


FIGURE 14. Thermocouple Input with RTD Cold Junction Compensation.

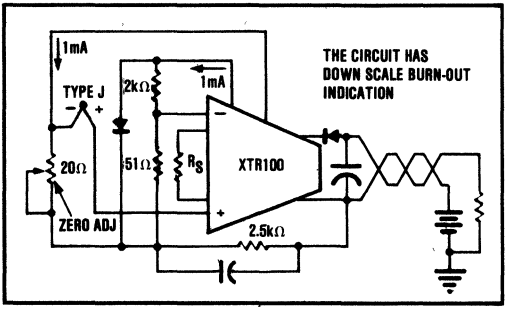


FIGURE 15. Thermocouple Input with Diode Cold Junction Compensation.

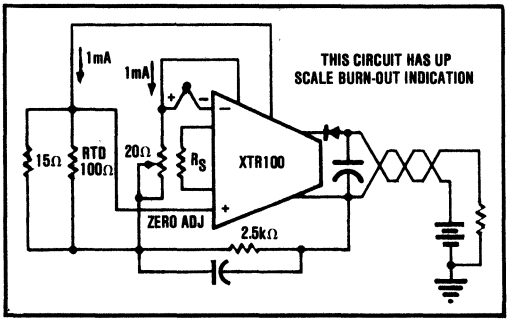


FIGURE 16. Thermocouple Input with RTD Cold Junction Compensation.

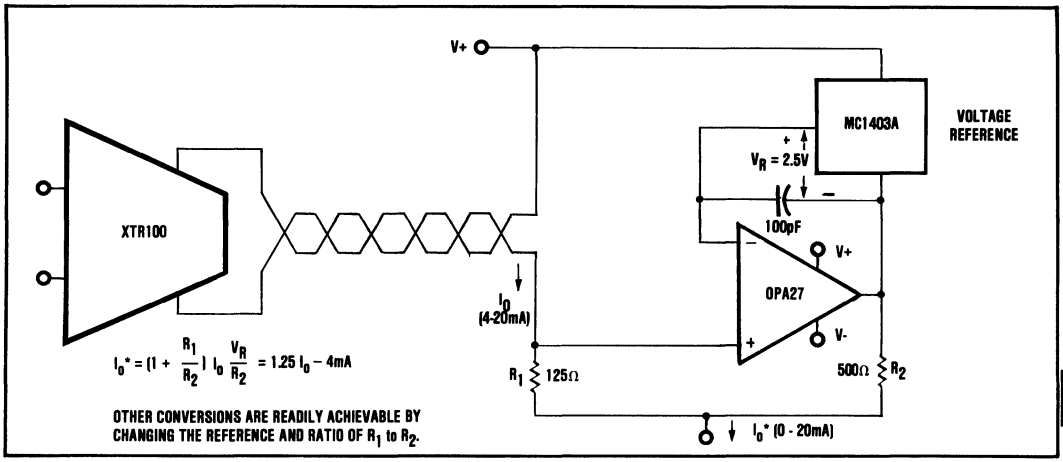


FIGURE 17. 0mA to 20mA Output Converter.

DETAILED ERROR ANALYSIS

The ideal output current is

$$i_{O\ IDEAL} = 4mA + K\ e_{IN} \quad (3)$$

K is the span (gain) term, $(0.016mA/mV) + (40/R_S)$

The nature of the XTR100 circuit is such that there are three major components of error

σ_O = error associated with the output stage.
σ_S = errors associated with span adjustment.
σ_I = errors associated with input stage.

The transfer function including these errors is

$$I_{O\ ACTUAL} = (4mA + \sigma_O) + K\ (1 + \sigma_S)(e_{IN} + \sigma_I) \quad (4)$$

When this expression is expanded, second order terms (σ_S σ_I) dropped, and terms collected, the result is

$$i_{O\ ACTUAL} = (4mA + \sigma_O) + K\ e_{IN} \text{ "} K\sigma_I + K\sigma_S\ e_{IN} \quad (5)$$

The error in the output current is $i_{O\ ACTUAL}$ - $i_{O\ IDEAL}$ and can be found by subtracting equations (5) and (3).

$$i_{O\ ERROR} = \sigma_O + K\sigma_S + K\ \sigma_S\ e_{IN} \quad (6)$$

This is a general error expression. The composition of each component of error depends on the circuitry inside the XTR100 and the particular circuit in which it is applied. The circuit of Figure 7 will be used to illustrate the principles.

$$\sigma_O = Ios_{RTO} \quad (7)$$

Ios_{RTO}* = the output offset error current.

For the circuit of Figure 7,

$$\sigma_I = V_{OSI} + [I_{B1}\ R_T - I_{B2}\ R_4] + \frac{\Delta V_{CC}}{PSRR} + \frac{(e_1 + e_2)/2 - 5V}{CMRR} \quad (8)$$

The term in brackets maybe written in terms of offset current and resistor mismatches as $I_{B1}\ \Delta R + I_{OS}\ R_4$.

V_{OSI}* = input offset voltage
I_{B1},* I_{B2}* = input bias current
I_{OSI}* = input offset current
$\Delta R = R_T - R_4$ = mismatch in resistor
ΔV_{CC} = change supply voltage between pins 7 and 8 away from 24V nomimal
PSRR* = power supply rejection ratio
CMRR* = common-mode rejection ratio

$\sigma_S = \epsilon_{NONLIN} + \epsilon_{SPAN}$
ϵ_{NONLIN}* = span nonlinearity
ϵ_{SPAN}* = span equation error. Untrimmed error = 3% max. May be trimmed to zero.

*Items marked with an asterisk (*) can be found in the Electrical Specifications.

EXAMPLE 3

Given the circuit in Figure 7 with the XTR100B specifications and the following conditions: R_I = 109.4Ω at 25°C, R_T = 156.4Ω at 150°C, I_o = 4mA at 25°C, I_o = 20mA at 150°C, R_S = 123.3Ω, R_4 = 109Ω, R_L = 250Ω, R_{LINE} = 100Ω, V_{D1} = 0.6V, V_{PS} = 24V ±0.5%. Determine the % error at the upper and lower range values.

A. At the lower range value (T = 25°C).

$\sigma_O = Ios_{RTO} = \pm 4\mu A$

$$\sigma_I = V_{OSI} + [I_{B1}\ \Delta R + I_{OSI}\ R_4] + \frac{\Delta V_{CC}}{PSRR} + \frac{(e_1 + e_2)/2 - 5}{CMRR}$$

$\Delta R = R_{T_{25°C}} - R_4 = 109.4 - 109 \approx 0$

$\Delta V_{CC} = 24 \times 0.005 + 4mA\ (250\Omega + 100\Omega) + 0.6V$
$= 120mV + 1400mV + 600mV = 2120mV$

$e_1 = (2mA \times 2.5k\Omega) + (1mA \times 109\Omega) = 5.109V$
$e_2 = (2mA \times 2.5k\Omega) + (1mA \times 109.4\Omega) = 5.1094V$
$(e_1 + e_2)/2 - 5 \approx 0$

$PSRR = 3.16 \times 10^5$ for 110dB
$CMRR = 31.6 \times 10^3$ for 90dB

$$\sigma_I = 25\mu V + (150nA \times 0 + 30nA \times 109\Omega) \quad (9)$$

$$+ \frac{2120mV}{3.16 \times 10^5} + \frac{0}{31.6 \times 10^3}$$

$$= 25\mu V + 3.27\mu V + 6.7\mu V + 0$$
$$= 34.97$$

$$\sigma_S = \epsilon_{NONLIN} + \epsilon_{SPAN}$$
$$= 0.0001 + 0 \text{ (assumes trim of } R_S)$$
$$i_O \text{ error} = \sigma_O + K\,\sigma_I + K\,\sigma_S\,e_{IN}$$

$$K = 0.016 + \frac{40}{R_S} = 0.016 + \frac{40}{123.3\Omega} = 0.341\,U$$

$$e_{IN} = e_2 - V_4 = I_{REF1}\,R_{T_{25°C}} - I_{REF2}\,R_4$$
since $R_{T\ 25°C} = R_4$
$$e_{IN} = (I_{REF1} - I_{REF2})\,R_4 = 0.1\mu A \times 109\Omega = 10.9\mu V$$

Since the maximum mismatch of the current references is 0.01% of 1mA = 0.1μA

$$i_O \text{ error} = 4\mu A + (0.34U \times 34.97) + (0.341 \times 0.0001) \times 10.9\mu V = 4\mu A + 11.89\mu A + 0.0004\mu A = 15.89\mu A$$

$$\%\text{ error} = \frac{15.89}{4mA} \times 100\% = 0.4\% \text{ at lower range value.}$$

B. At the upper range value (T = 150°C)

$$\Delta R = R_{T\ 150°C} - R_4 = 156.4 - 109.4 = 47\Omega$$
$$\Delta V_{CC} = 24 \times 0.005 + 20mA\,(250\Omega + 100\Omega) + 0.6 = 7720mV$$
$$e_1 = 5.109V$$
$$e_2 = (2mA \times 2.5k\Omega) + (1mA \times 156.4\Omega) = 5.156V$$
$$(e_1\ e_2)/2 - 5V \approx 0$$
$$\Delta R = -R_{1\ 150°C} + R_4 = 156.4 - 109 = 47\Omega$$
$$\sigma_O = 4\mu A$$
$$\sigma_I = 25\mu V + (150nA \times 47\Omega + 30nA \times 109\Omega) + \frac{7720mV}{3.16 \times 10^5} + \frac{0}{31.6 \times 10^3}$$
$$= 25\mu V + 10.33\mu V + 24\mu V\ F0 = 59.33\mu V$$
$$\sigma_S = 0.0001$$
$$e_{IN} = e_2' - V_4 = I_{REF1}\,R_{T\ 150°C} - I_{REF2}\,R_4$$
$$= (1mA \times 156.4\Omega) - (1mA - 109\Omega)$$
$$= 47mV.$$

$$i_{O\ ERROR} = \sigma_O + K\,\sigma_I + K\,\sigma_S \times e_{IN} \quad (10)$$
$$= 4\mu A + 0.341U \times 59.33\mu V + 0.341U \times 0.0001 \times 47000\mu V$$
$$= 4 \times 20.23 + 1.6 = 25.83\mu A$$

$$\%\text{ error} = \frac{25.83\mu A}{20mA} \times 100\% = 0.13\% \text{ at upper range value or \% of FS.}$$

CONCLUSIONS

From equation (9) it is observed that the predominant error term is the input offset voltage (25μV for the B grade). This is of little consequence in many applications. $V_{OS\ RTI}$ can, however, be nulled using the pot shown in Figures 3 and 4. From equation (10), the predominant errors are $I_{OS\ RTI}$ (4μA), $V_{OS\ RTI}$ (25μV), and I_B (150nA), max, B grade.

A NOTE FOR HIGH GAIN APPLICATIONS

In applications where e_{in} full scale is small (<50mV) and R_{span} is small (<≈150Ω), caution should be taken to consider errors from the external span circuit plus high amplification of offset drift and noise.

In such applications, be sure to include the effect of the normal thermal feedback within the XTR100 package. Small additional errors occur from a change in input offset voltage and current due to a change in chip temperature resulting from a change in output current (4mA up to 20mA).

The XTR100 has two thermal resistance specifications:

$\theta_{JA} = 115°C$

This is the thermal resistance from output transistor to ambient. It is used for normal power dissipation considerations (see Figure 18).

$\theta_{JI} = 60°C/W$

This is the thermal resistance which describes the effect of output stage power dissipation in input stage temperature rise.

As an example of how θ_{JI} would be applied, we will calculate the limits with $V_{PS} = 40V$ and $R_L = 250\Omega$.

Power Dissipation:

at 20mA output: 20mA [40V−(20mA × 250Ω)] = 700mW
at 4mA output: 4mA [40V−(4mA × 250Ω)] = 156mW

Thermal Resistance: $\theta_{JI} = 60°C/W$

Input Stage Temperature Rise:

at 20mA output: 700mW × 60°C/W = 42°C
at 4mA output: 156mW × 60°C/W = 9.4°C

Thus under these conditions when the output changes from 4mA to 20mA the input stage temperature changes 42°C − 9.4°C = 32.6°C. The maximum input stage offset change will depend on the particular grade specification:

A Grade (1μV/°C max) = 32.6μV
B Grade (0.5μV/°C max) = 16.3μV

The amount of error that this offset voltage represents depends on how large the full scale input voltage is. It is worse, of course, for small input voltages. Table I shows the error as a percentage of full scale and in terms of output current (% FS error × 16mA FS output span).

TABLE I. Maximum Errors Due to Thermal Feedback
$V_{PS} = 40V$, $R_L = 250\Omega$.

	10mV FS	100mV FS	1V FS
A Grade	0.326% (52.2μA)	0.0326% (5.22μA)	0.0033% (0.522μA)
B Grade	0.163% (26 1μA)	0.0163% (2.61μA)	0.0016% (0 261μA)

HOW TO REDUCE ERRORS

Lower V_{PS}

The errors can be reduced by lowering the voltage at the XTR100 line terminals. The errors in the example above represent a fairly demanding condition of maximum voltage ($V_{PS} = 40V$) and minimum resistance ($R_L = 250\Omega$). If the voltage is lowered to 24V, then a 4mA to 20mA output change causes a change in input stage temperature of 17.3°C and the errors in Table I are reduced by a factor of 17.3°C/32.6°C = 0.53. (Note that this is different than the decrease in the voltage itself: 24/40 = 0.6.)

Raise Resistance

If the load or line resistance is raised the output power dissipation will also be reduced. If $R_L = 400\Omega$ (400/250 = 1.6), the change in output temperature is 29.2°C as the output changes from 4mA to 20mA (still with V_{PS} = 40V) and the errors in Table I are reduced by a factor of 29.2°C/32.6°C = 0.9.

Heat Sink

Heat sinking the package will reduce both θ_{JA} and θ_{JI}. The following is information on small-finned heat sinks that are attached with an epoxy heat sink adhesive (AHAM-985). The three models are 0.75″ × 0.4″ × 0.21″.

Model 141
AHAM
27901 Front St.
Rancho, CA 92390
(714) 676-4151

Models 141 and 142
Heat Sink Plus
28715 Via Montezuma
Temecula, CA 92390
(714) 676-3031

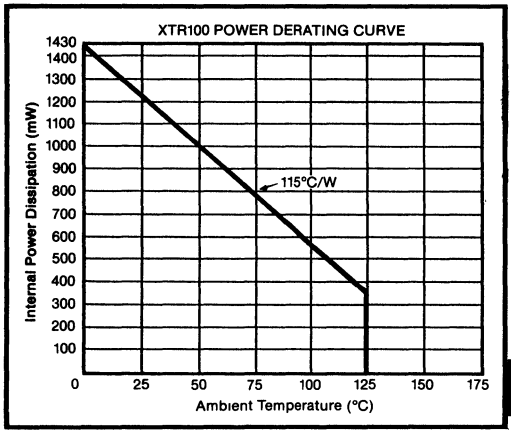


FIGURE 18. Power Derating Curve.

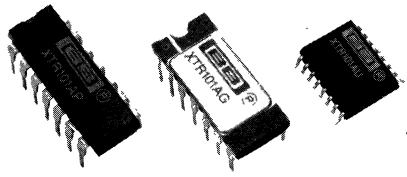
GENERAL RECOMMENDATIONS HANDLING PROCEDURES FOR INTEGRATED CIRCUITS

All semiconductor devices are vulnerable, in varying degrees, to damage from the discharge of electrostatic energy. Such damage can cause performance degradation or failure, either immediate or latent. As a general practice we recommend the following handling procedures to reduce the risk of electrostatic damage.

1. Remove the static-generating materials, such as untreated plastics, from all areas that handle microcircuits.
2. Ground all operators, equipment, and work stations.
3. Transport and ship microcircuits, or products incorporating microcircuits, in static-free, shielded containers.
4. Connect together all leads of each device by means of a conductive material, when the device is not connected into a circuit.
5. Control relative humidity to as high a value as practical (50% is recommended).

BURR-BROWN®

XTR101



AVAILABLE IN DIE FORM

Precision, Low Drift 4mA to 20mA TWO-WIRE TRANSMITTER

FEATURES

- INSTRUMENTATION AMPLIFIER INPUT
  - Low Offset Voltage, 30μV max
  - Low Voltage Drift, 0.75μV/°C max
  - Low Nonlinearity, 0.01% max
- TRUE TWO-WIRE OPERATION
  - Power and Signal on One Wire Pair
  - Current Mode Signal Transmission
  - High Noise Immunity
- DUAL MATCHED CURRENT SOURCES
- WIDE SUPPLY RANGE, 11.6V to 40V
- −40°C to +85°C SPECIFICATION RANGE
- SMALL 14-PIN DIP PACKAGE, CERAMIC AND PLASTIC

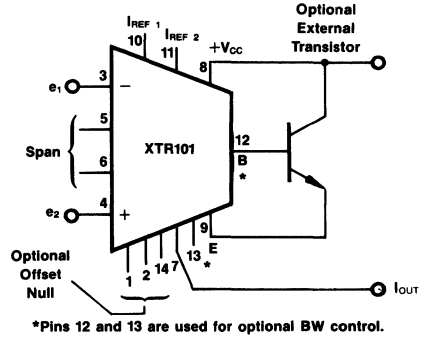
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  - Pressure Transmitters
  - Temperature Transmitters
  - Millivolt Transmitters
- RESISTANCE BRIDGE INPUTS
- THERMOCOUPLE INPUTS
- RTD INPUTS
- CURRENT SHUNT (mV) INPUTS
- PRECISION DUAL CURRENT SOURCES
- AUTOMATED MANUFACTURING
- POWER PLANT/ENERGY SYSTEM MONITORING

DESCRIPTION

The XTR101 is a microcircuit, 4mA to 20mA, two-wire transmitter containing a high accuracy instrumentation amplifier (IA), a voltage-controlled output current source, and dual-matched precision current reference. This combination is ideally suited for remote signal conditioning of a wide variety of transducers such as thermocouples, RTDs, thermistors, and strain gauge bridges. State-of-the-art design and laser-trimming, wide temperature range operation and small size make it very suitable for industrial process control applications. In addition the optional external transistor allows even higher precision.

The two-wire transmitter allows signal and power to be supplied on a single wire-pair by modulating the power supply current with the input signal source. The transmitter is immune to voltage drops from long runs and noise from motors, relays, actuators, switches, transformers, and industrial equipment. It can be used by OEMs producing transmitter modules or by data acquisition system manufacturers. Also, the XTR101 is generally very useful for low-noise, current-mode signal transmission.



*Pins 12 and 13 are used for optional BW control.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-627C

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, +V_{CC} = 24VDC, R_L = 100Ω with external transistor connected unless otherwise noted.

PARAMETER	CONDITIONS/DESIGNATION	XTR101AG MIN	XTR101AG TYP	XTR101AG MAX	XTR101BG MIN	XTR101BG TYP	XTR101BG MAX	XTR101AP MIN	XTR101AP TYP	XTR101AP MAX	XTR101AU MIN	XTR101AU TYP	XTR101AU MAX	UNITS
OUTPUT AND LOAD CHARACTERISTICS														
Current	Linear Operating Region	4		20	*		*	*		*	*		*	mA
	Derated Performance	3.8		22	*		*	*		*	*		*	mA
Current Limit			28	38		*	*		31	*		31	*	mA
Offset Current Error	I_{OS}, I_O = 4mA		±3.9	±10		±2.5	±6		±8.5	±19		±8.5	±19	µA
vs Temperature	$\Delta I_{OS}/\Delta T$		±10 5	±20		±8	±15		±10.5	±20		*		ppm, FS/°C
Full Scale Output Current Error	Full Scale = 20mA		±20	±40		±15	±30		±30	±60		±30	±60	µA
Power Supply Voltage	V_{CC}, pins 7 and 8, compliance[1]	+11.6		+40	*		*	*		*	*		*	VDC
Load Resistance	At V_{CC} = +24V, I_O = 20mA			600			*			600			*	Ω
	At V_{CC} = +40V, I_O = 20mA			1400			*			1400			*	Ω
SPAN														
Output Current Equation	R_S in Ω, e_1 and e_2 in V					$I_O = 4mA + [0.016Ω + (40/R_S)] (e_2 - e_1)$								
Span Equation	R_S in Ω					$S = [0.016Ω + (40/R_S)]$								A/V
vs Temperature	Excluding TCR of R_S		±30	±100		*	*		*	*		*	*	ppm/°C
Untrimmed Error[2]	ε_{SPAN}	−5	−2 5	0	*	*	*	*	*	*	*	*	*	%
Nonlinearity	$\varepsilon_{NONLINEARITY}$			0.01			*			*			*	%
Hysteresis			0			*			*			*		%
Dead Band			0			*			*			*		%
INPUT CHARACTERISTICS														
Impedance Differential			0 4 ‖ 3			*			*			*		GΩ ‖ pF
Common-Mode			10 ‖ 3			*			*			*		GΩ ‖ pF
Voltage Range, Full Scale	$\Delta e = (e_2 - e_1)$ [3]	0		1	*		*	*		*	*		*	V
Offset Voltage	V_{OS}		±30	±60		±20	±30		*	±100		*	±100	µV
vs Temperature	$\Delta V_{OS}/\Delta T$		±0 75	±1.5		±0 35	±0 75		*	*		*	*	µV/°C
Power Supply Rejection	$\Delta V_{CC}/PSRR = V_{OS}$ Error	110	125		*	*		*	122		110	122		dB
Bias Current	I_B		60	150		*	*		*	*		*	*	nA
vs Temperature	$\Delta I_B/\Delta T$		0 30	1		*	*		*	*		*	*	nA/°C
Offset Current	I_{OSI}		10	±30		*	±20		*	*		*	*	nA
vs Temperature	$\Delta I_{OSI}/\Delta T$		0 1	0 3		*	*		*	*		*	*	nA/°C
Common-Mode Rejection[4]	DC	90	100		*	*		*	*		*	*		dB
Common-Mode Range	e_1 and e_2 with respect to pin 7	4		6	*		*	*		*	*		*	V
CURRENT SOURCES														
Magnitude			1			*			*			*		mA
Accuracy	V_{CC} = 24V, $V_{PIN\ 8} - V_{PIN\ 10, 11}$ = 19V, R_2 = 5kΩ, Figure 5		±0 06	±0 17		±0.025	±0.075		±0.2	±0 37		±0.2	±0 37	%
vs Temperature			±50	±80		±30	±50		*	*		*	*	ppm/°C
vs V_{CC}			±3			*			*			*		ppm/V
vs Time			±8			*			*			*		ppm/month
Compliance Voltage	With respect to pin 7	0		V_{CC} − 3.5				*		*	*		*	V
Ratio Match	Tracking													
Accuracy	$(1 - I_{REF\ 1}/I_{REF\ 2}) \times 100\%$		±0 014	±0 06		±0.009	±0.04		±0.031	±0.088		±0 031	±0 088	%
vs Temperature				±15			10			*			*	ppm/°C
vs V_{CC}			±10			*			*			*		ppm/V
vs Time			±1			*			*			*		ppm/month
Output Impedance		10	20		*	*		*	15		*	15		MΩ
TEMPERATURE RANGE														
Specification		−40		+85	*		*	−40		+85	*		*	°C
Operating		−55		+125	*		*	−40		+85	−40		+85	°C
Storage		−55		+165	*		*	−55		+125	−55		+125	°C

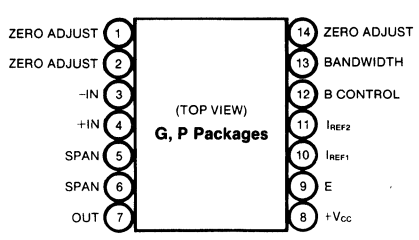
*Same as XTR101AG

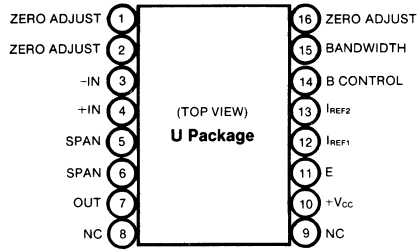
NOTES. (1) See Typical Performance Curves. (2) Span error shown is untrimmed and may be adjusted to zero (3) e_1 and e_2 are signals on the −In and +In terminals with respect to the output, pin 7. While the maximum permissible Δe is 1V, it is primarily intended for much lower input signal levels, e.g., 10mV or 50mV full scale for the XTR101A and XTR101B grades respectively. 2mV FS is also possible with the B grade, but accuracy will degrade due to possible errors in the low value span resistance and very high amplification of offset, drift, and noise. (4) Offset voltage is trimmed with the application of a 5V common-mode voltage. Thus the associated common-mode error is removed See Application Information section.

ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC}	40V
Input Voltage, e_1 or e_2	≥V_{OUT}, ≤+V_{CC}
Storage Temperature Range, Ceramic	−55°C to +165°C
Plastic	−55°C to +125°C
Lead Temperature	
(soldering, 10s) G, P	+300°C
(wave soldering, 3s) U	+260°C
Output Short-Circuit Duration	Continuous +V_{CC} to I_{OUT}
Junction Temperature	+165°C

PIN DESIGNATIONS



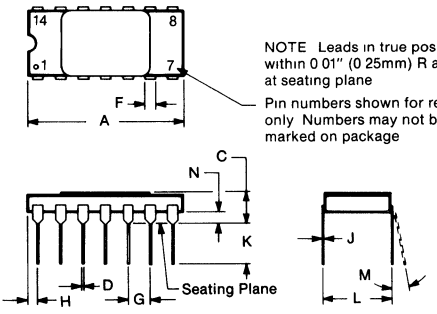


MECHANICAL

G PACKAGE

Hermetic DIP

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	670	710	17 02	18 03
C	065	170	1 65	4 32
D	015	021	0 38	0 53
F	045	060	1 14	1 52
G	100 BASIC		2 54 BASIC	
H	025	070	0 64	1 78
J	008	012	0 20	0 30
K	120	240	3 05	6 10
L	300 BASIC		7 62 BASIC	
M	—	10°	—	10°
N	009	060	0 23	1 52

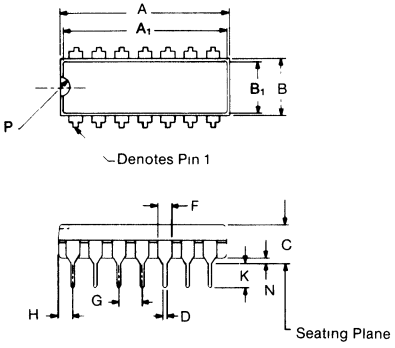


NOTE Leads in true position within 0 01" (0 25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers may not be marked on package

P PACKAGE

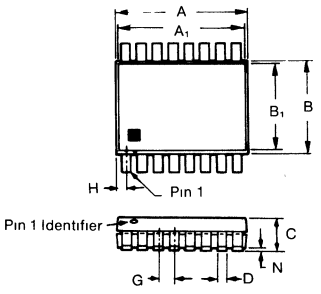
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	700	800	17 78	20 32
A_1	685	785	17 40	19 94
B	230	290	5 85	7 38
B_1	200	250	5 09	6 36
C	120	200	3 05	5 09
D	015	023	0 38	0 59
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	050	100	1 27	2 54
J	008	015	0 20	0 38
K	070	150	1 78	3 82
L	300 BASIC		7 63 BASIC	
M	0°	15°	0°	15°
N	010	030	0 25	0 76
P	025	050	0 64	1 27



NOTE Leads in true position within 010" (25mm) R at MMC at seating plane

U PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	400	416	10 16	10 57
A_1	388	412	9 86	10 46
B	286	302	7 26	7 67
B_1	268	286	6 81	7 26
C	093	109	2 36	2 77
D	015	020	0 38	0 51
G	050 BASIC		1 27 BASIC	
H	022	038	0 56	0 97
J	008	012	0 20	0 30
L	391	421	9 93	10 69
M	5° TYP		5° TYP	
N	000	012	0 00	0 30



NOTE Leads in true position within 010" (25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers are not marked on package Pins 8 and 9 on U package are not used

ORDERING INFORMATION

Model	Package	Temperature Range
XTR101AG	Ceramic DIP	-40°C to +85°C
XTR101BG	Ceramic DIP	-40°C to +85°C
XTR101AP	Plastic DIP	-40°C to +85°C
XTR101AU	Plastic SOIC	-40°C to +85°C

BURN-IN SCREENING OPTION
See text for details.

Model	Package	Burn-In Temp. (160h)[1]
XTR101AG-BI	Ceramic DIP	+125°C
XTR101BG-BI	Ceramic DIP	+125°C
XTR101AP-BI	Plastic DIP	+85°C
XTR101AU-BI	Plastic SOIC	+85°C

NOTE (1) Or equivalent combination See text

BURN-IN SCREENING

Burn-in screening is an option available for both plastic- and ceramic-packaged XTR101s. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

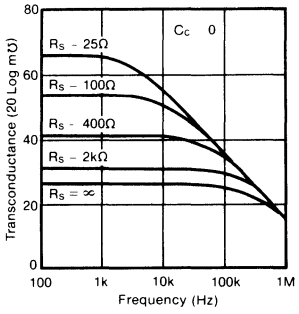
Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

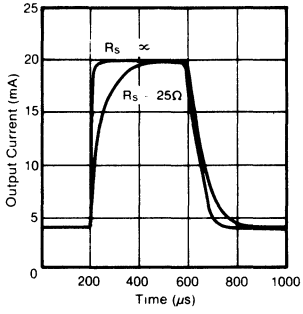
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, $+V_{CC}$ = 24VDC unless otherwise noted)

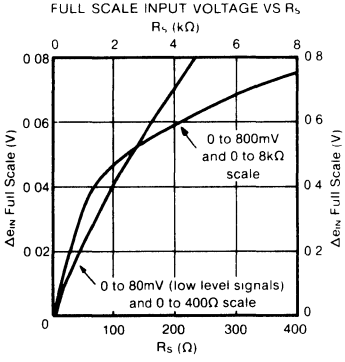
SPAN VS FREQUENCY



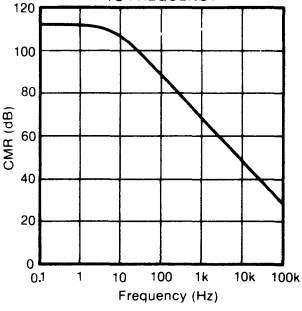
STEP RESPONSE



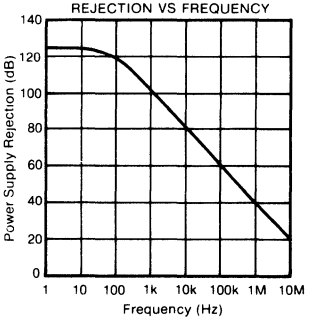
FULL SCALE INPUT VOLTAGE VS R_S



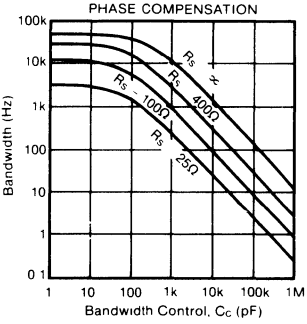
COMMON-MODE REJECTION VS FREQUENCY



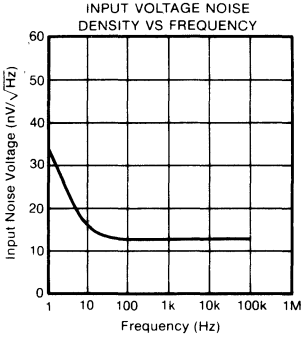
POWER SUPPLY REJECTION VS FREQUENCY



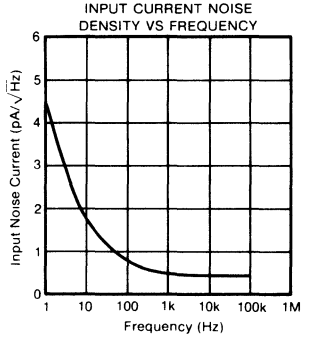
BANDWIDTH VS PHASE COMPENSATION



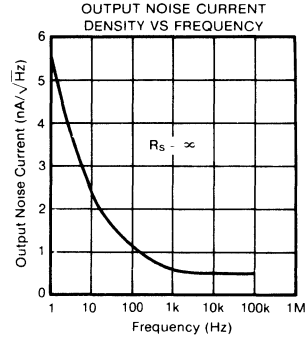
INPUT VOLTAGE NOISE DENSITY VS FREQUENCY



INPUT CURRENT NOISE DENSITY VS FREQUENCY



OUTPUT NOISE CURRENT DENSITY VS FREQUENCY



THEORY OF OPERATION

A simplified schematic of the XTR101 is shown in Figure 1. Basically the amplifiers, A_1 and A_2, act as a single power supply instrumentation amplifier controlling a current source, A_3 and Q_1. Operation is determined by an internal feedback loop. e_1 applied to pin 3 will also appear at pin 5 and similarly e_2 will appear at pin 6. Therefore the current in R_S, the span setting resistor, will be $I_S = (e_2 - e_1)/R_S = e_{IN}/R_S$. This current combines with the current, I_3, to form I_1. The circuit is configured such that I_2 is 19 times I_1. From this point the derivation of the transfer function is straightforward but lengthy. The result is shown in Figure 1.

Examination of the transfer function shows that I_O has a lower range-limit of 4mA when $e_{IN} = e_2 - e_1 = 0V$. This 4mA is composed of 2mA quiescent current exiting pin 7 plus 2mA from the current sources. The upper range limit of I_O is set to 20mA by the proper selection of R_S based on the upper range limit of e_{IN}. Specifically R_S is chosen for a 16mA output current span for the given full scale input voltage span; i.e., $(0.016\Omega + 40/R_S)(e_{IN}$ full scale$) = 16mA$. Note that since I_O is unipolar e_2 must be kept larger than e_1; i.e., $e_2 \geq e_1$ or $e_{IN} \geq 0$. Also note that in order not to exceed the output upper range limit of 20mA, e_{IN} must be kept less than 1V when $R_S = \infty$ and proportionately less as R_S is reduced.

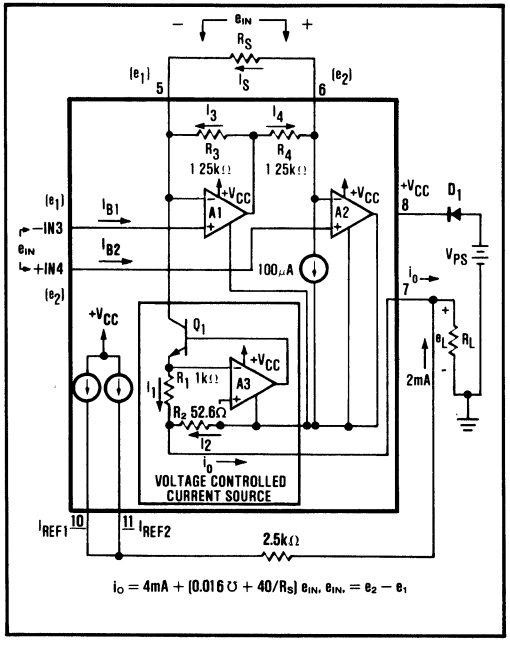


FIGURE 1. Simplified Schematic of the XTR101.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CONNECTION

The basic connection of the XTR101 is shown in Figure 1. A difference voltage applied between input pins 3 and 4 will cause a current of 4mA to 20mA to circulate in the two-wire output loop (through R_L, V_{PS}, and D_1). For applications requiring moderate accuracy, the XTR101 operates very cost-effectively with just its internal drive transistor. For more demanding applications (high accuracy in high gain) an external NPN transistor can be added in parallel with the internal one. This keeps the heat out of the XTR101 package and minimizes thermal feedback to the input stage. Also in such applications where e_{IN} full scale is small (<50mV) and R_{SPAN} is small (<150Ω), caution should be taken to consider errors from the external span circuit plus high amplification of offset drift and noise.

OPTIONAL EXTERNAL TRANSISTOR

The optional external transistor, when used, is connected in parallel with the XTR101's internal transistor. The purpose is to increase accuracy by reducing heat change inside the XTR101 package as the output current spans from 4mA to 20mA. Under normal operating conditions, the internal transistor is never completely turned off as shown in Figure 2. This maintains frequency stability with varying external transistor characteristics and wiring capacitance. The actual "current sharing" between internal and external transistors is dependent on two factors: (1) relative geometry of emitter areas and (2) relative package dissipation (case size and thermal conductivity). For best results, the external device should have a larger base emitter area and smaller package. It will, upon turn on, take about [0.95 (I_O – 3.3mA)]mA. However, it will heat faster and take a greater share after a few seconds.

Although any NPN of suitable power rating will operate with the XTR101, two readily available transistors are recommended for accuracy improvement:

1. 2N2222 in the TO-18 package. For power supply voltages above 24V, a 750Ω, 1/2W resistor should be connected in series with the collector. This will limit the power dissipation to 377mW under the worst-case conditions shown in Figure 2. Thus the 2N2222 will safely operate below its 400mW rating at the upper temperature of +85°C. Heat sinking the 2N2222 will result in greatly reduced accuracy improvement and is not recommended.
2. 2N6121 in the TO-220 package. This transistor will operate over the specified temperature and output voltage range without a series collector resistor. Heat sinking the 2N6121 will result in slightly less accuracy improvement. It can be done, however, when mechanical constraints require it.

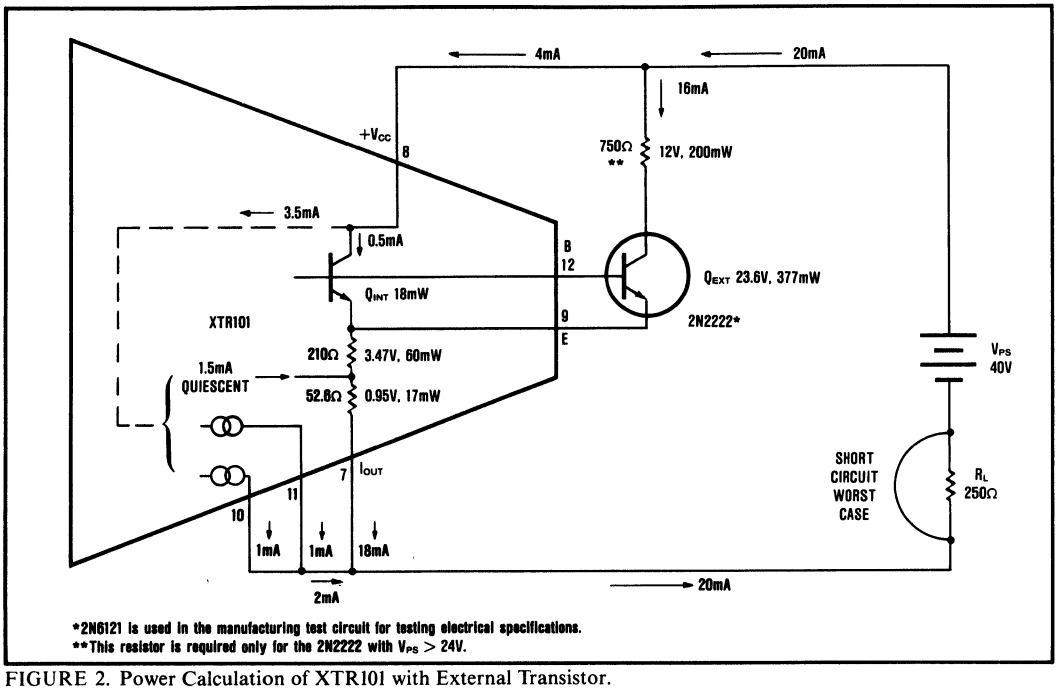


FIGURE 2. Power Calculation of XTR101 with External Transistor.

ACCURACY WITH AND WITHOUT EXTERNAL TRANSISTOR

The XTR101 has been tested in a circuit using a 2N6121 external transistor. The relative difference in accuracy with and without an external transistor is shown in Figure 3. Notice that a dramatic improvement in offset voltage change with supply voltage is evident for any value of load resistor.

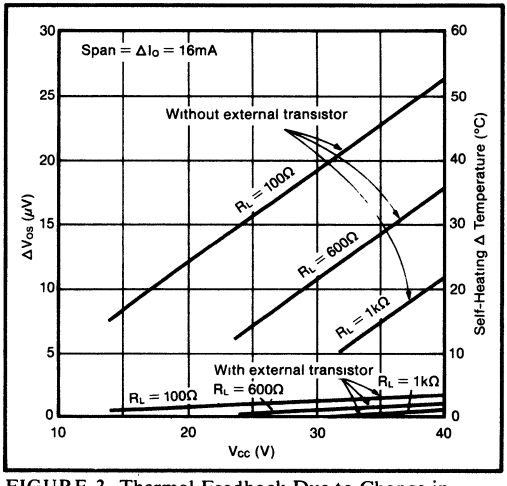


FIGURE 3. Thermal Feedback Due to Change in Output Current.

MAJOR POINTS TO CONSIDER WHEN USING THE XTR101

1. The leads to R_S should be kept as short as possible to reduce noise pick-up and parasitic resistance.
2. $+V_{CC}$ should be bypassed with a 0.01μF capacitor as close to the unit as possible (pin 8 to 7).
3. Always keep the input voltages within their range of linear operation, +4V to +6V (e_1 and e_2 measured with respect to pin 7).
4. The maximum input signal level ($e_{IN_{FS}}$) is 1V with $R_S = \infty$ and proportionally less as R_S decreases.
5. Always return the current references (pins 10 and 11) to the output (pin 7) through an appropriate resistor. If the references are not used for biasing or excitation, connect them together to pin 7. Each reference must have between 0V and $+(V_{CC} - 4V)$ with respect to pin 7.
6. Always choose R_L (including line resistance) so that the voltage between pins 7 and 8 ($+V_{CC}$) remains within the 11.6V to 40V range as the output changes between the 4mA to 20mA range (see Figure 4).
7. It is recommended that a reverse polarity protection diode (D_1 in Figure 1) be used. This will prevent damage to the XTR101 caused by a momentary (e.g., transient) or long term application of the wrong polarity of voltage between pins 7 and 8.
8. Consider PC board layout which minimizes parasitic capacitance, especially in high gain.

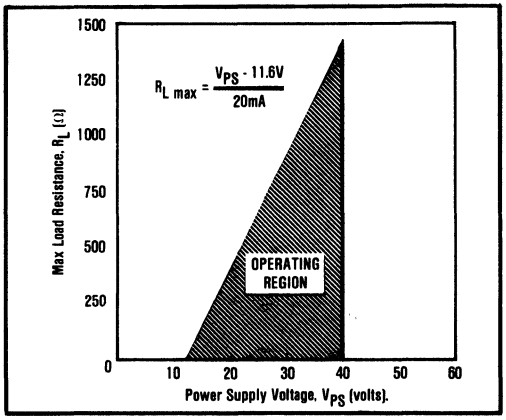


FIGURE 4. Power Supply Operating Range.

SELECTING R_S

R_{SPAN} is chosen so that a given full scale input span $e_{IN_{FS}}$ will result in the desired full scale output span of ΔI_{OFS},

$$[(0.016\text{Ω}) + (40/R_S)]\ \Delta e_{IN} = \Delta I_O = 16mA.$$

Solving for R_S:

$$R_S = \frac{40}{\Delta I_O/\Delta e_{IN} - 0.016\text{Ω}} \qquad (1)$$

For example, if $\Delta e_{IN_{FS}} = 100mV$ for $\Delta I_{O_{FS}} = 16mA$,

$$R_S = \frac{40}{(16mA/100mV) - 0.016} = \frac{40}{0.16 - 0.016} = \frac{40}{0.144}$$
$$= 278\Omega$$

See Typical Performance Curves for a plot of R_S vs $\Delta e_{IN_{FS}}$. Note that in order not to exceed the 20mA upper range limit, e_{IN} must be less than 1V when $R_S = \infty$ and proportionately smaller as R_S decreases.

BIASING THE INPUTS

Because the XTR operates from a single supply both e_1 and e_2 must be biased approximately 5V above the voltage at pin 7 to assure linear response. This is easily done by using one or both current sources and an external resistor R_2. Figure 5 shows the simplest case—a floating voltage source e'_2. The 2mA from the current sources flows through the 2.5kΩ value of R_2 and both e_1 and e_2 are raised by the required 5V with respect to pin 7. For linear operation the constraint is

$$+4V \leq e_1 \leq +6V$$
$$+4V \leq e_2 \leq +6V$$

The offset adjustment is used to remove the offset voltage of the input amplifier. When the input differential voltage (e_{IN}) equals zero, adjust for 4mA output.

Figure 6 shows a similar connection for a resistive transducer. The transducer could be excited either by one (as shown) or both current sources. Also, the offset adjustment has higher resolution compared to Figure 5.

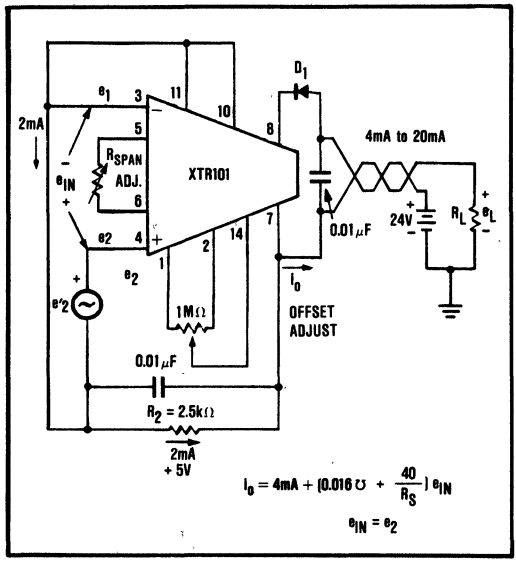


FIGURE 5. Basic Connection for Floating Voltage Source.

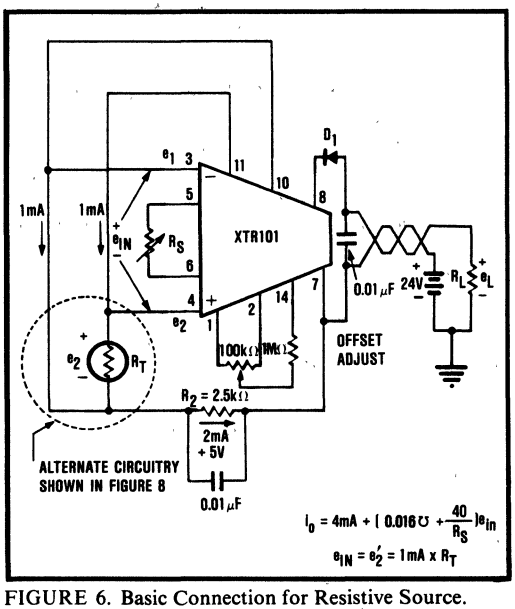


FIGURE 6. Basic Connection for Resistive Source.

CMV AND CMR

The XTR101 is designed to operate with a nominal 5V common-mode voltage at the input and will function properly with either input operating over the range of 4V to 6V with respect to pin 7. The error caused by the 5V CMV is already included in the accuracy specifications.

If the inputs are biased at some other CMV then an input offset error term is (CMV − 5)/CMRR; CMR is in dB, CMRR is in V/V.

SIGNAL SUPPRESSION AND ELEVATION

In some applications it is desired to have suppressed zero range (input signal elevation) or elevated zero range (input signal suppression). This is easily accomplished with the XTR101 by using the current sources to create the suppression/elevation voltage. The basic concept is shown in Figures 7 and 8 (a). In this example the sensor voltage is derived from R_T (a thermistor, RTD or other variable resistance element) excited by one of the 1mA current sources. The other current source is used to create the elevated zero range voltage. Figures 8 (b), (c) and (d) show some of the possible circuit variations. These circuits have the desirable feature of noninteractive span and suppression/elevation adjustments. Note: It is not recommended to use the optional offset voltage null (pins 1, 2, and 14) for elevation/suppression. This trim capability is used only to null the amplifier's input offset voltage. In many applications the already low offset voltage (typically 20μV) will not need to be nulled at all. Adjusting the offset voltage to nonzero values will disturb the voltage drift by ±0.3μV/°C per 100μV of induced offset.

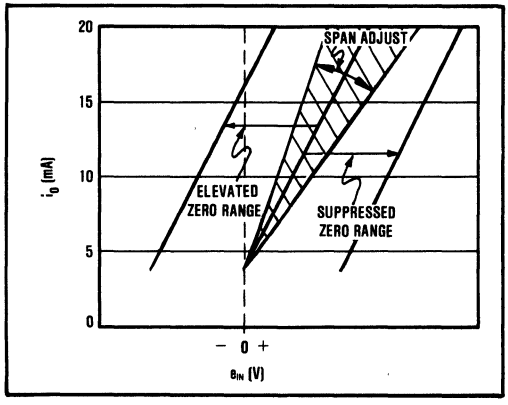


FIGURE 7. Elevation and Suppression Graph.

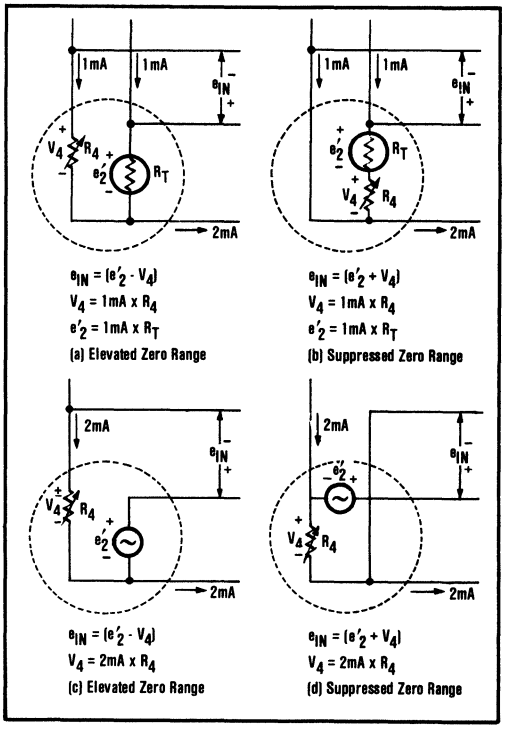


FIGURE 8. Elevation and Suppression Circuits.

APPLICATION INFORMATION

The small size, low offset voltage and drift, excellent linearity, and internal precision current sources, make the XTR101 ideal for a variety of two-wire transmitter applications. It can be used by OEMs producing different types of transducer transmitter modules and by data acquisition systems manufacturers who gather transducer data. Current mode transmission greatly reduces noise interference. The two-wire nature of the device allows economical signal conditioning at the transducer. Thus the XTR101 is, in general, very suitable for individualized and special purpose applications.

EXAMPLE 1

RTD Transducer shown in Figure 9.

Given a process with temperature limits of +25°C and +150°C, configure the XTR101 to measure the tempera-

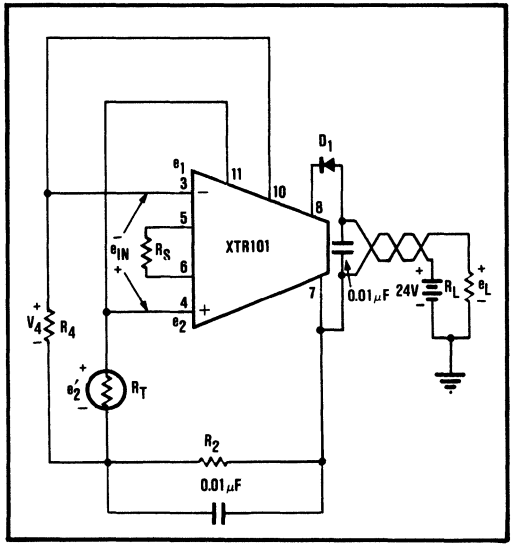


FIGURE 9. Circuit for Example 1.

ture with a platinum RTD which produces 100Ω at 0°C and 200Ω at +266°C (obtained from standard RTD tables). Transmit 4mA for +25°C and 20mA for +150°C.

COMPUTING R_S:

The sensitivity of the RTD is $\Delta R/\Delta T = 100\Omega/266°C$. When excited with a 1mA current source for a 25°C to 150°C range (i.e., 125°C span), the span of e_{IN} is 1mA × (100Ω/266°C) × 125°C = 47mV = Δe_{IN}.

$$\text{From equation 1, } R_S = \frac{40}{\frac{\Delta I_O}{\Delta e_{IN}} - 0.016\Omega}$$

$$R_S = \frac{40}{\frac{16mA}{47mV} - 0.016\mho} = \frac{40}{0.3244} = 123.3\Omega$$

Span adjustment (calibration) is accomplished by trimming R_S.

COMPUTING R_4:

$$\text{At } +25°C,\ e'_2 = 1mA\ (R_T + \Delta R_T)$$
$$= 1mA\ [100\Omega + (\frac{100\Omega}{266°C} \times 25°C)]$$
$$= 1mA\ (109.4\Omega)$$
$$= 109.4mV$$

In order to make the lower range limit of 25°C correspond to the output lower range limit of 4mA, the input circuitry shown in Figure 9 is used.

e_{IN}, the XTR101 differential input, is made 0 at 25°C

$$\text{or } e'_{2\,25°C} - V_4 = 0$$
$$\text{thus, } V_4 = e'_{2\,25°C} = 109.4mV$$
$$R_4 = \frac{V_4}{1mA} = \frac{109.4mV}{1mA} = 109.4\Omega$$

COMPUTING R_2 AND CHECKING CMV:

$$\text{At } +25°C,\ e'_2 = 109.4mV$$
$$\text{At } +150°C,\ e'_2 = 1mA\ (R_T + \Delta R_T)$$
$$= 1mA\ [100\Omega + (\frac{100\Omega}{266°C} \times 150°C)]$$
$$= 156.4mV$$

Since both e'_2 and V_4 are small relative to the desired 5V common-mode voltage, they may be ignored in computing R_2 as long as the CMV is met.

$$R_2 = 5V/2mA = 2.5k\Omega$$
$$e_2\ min = 5V + 0.1094V$$
$$e_2\ max = 5V + 0.1564V$$
$$e_1 = 5V + 0.1094V$$

The +4V to +6V CMV requirement is met.

EXAMPLE 2

Thermocouple Transducer shown in Figure 10.

Given a process with temperature (T_1) limits of 0°C and +1000°C, configure the XTR101 to measure the temperature with a type J thermocouple that produces a 58mV change for 1000°C change. Use a semiconductor diode for a cold junction compensation to make the measurement relative to 0°C. This is accomplished by supplying a compensating voltage, V_{R6}, equal to that normally produced by the thermocouple with its "cold junction" (T_2) at ambient. At a typical ambient of +25°C this is 1.28mV (obtained from standard thermocouple tables with reference junction of 0°C). Transmit 4mA for T_1 = 0°C and 20mA for T_1 = +1000°C. Note: $e_{IN} = e_2 - e_1$ indicates that T_1 is relative to T_2.

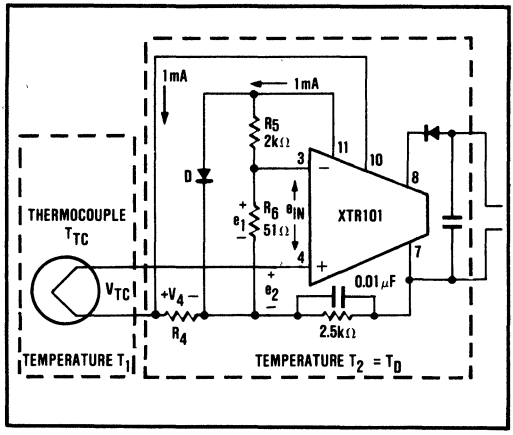


FIGURE 10. Thermocouple Input Circuit with Two Temperature Regions and Diode (D) Cold Junction Compensation.

ESTABLISHING R_S:

The input full scale span is 58mV ($\Delta e_{IN_{FS}}$ = 58mV).

R_S is found from equation (1)

$$R_S = \frac{40}{\frac{\Delta I_O}{\Delta e_{IN}} - 0.016\mho}$$
$$= \frac{40}{\frac{16mA}{58mV} - 0.016\mho} = \frac{40}{0.2599} = 153.9\Omega$$

SELECTING R_4:

R_4 is chosen to make the output 4mA at T_{TC} = 0°C (V_{TC} = −1.28mV) and T_D = +25°C (V_D = 0.6V). A circuit is shown in Figure 10.

V_{TC} will be −1.28mV when T_{TC} = 0°C and the reference junction is at +25°C. e_1 must be computed for the condition of T_D = +25°C to make e_{IN} = 0V.

$$V_{D\,25°C} = 600mV$$
$$e_{1\,25°C} = 600mV\ (51/2051) = 14.9mV$$
$$e_{IN} = e_2 - e_1 = V_{TC} + V_4 - e_1$$

With e_{IN} = 0 and V_{TC} = −1.28mV,

$$V_4 = e_1 + e_{IN} - V_{TC}$$
$$= 14.9mV + 0V - (-1.28mV)$$
$$1mA\ (R_4) = 16.18mV$$
$$R_4 = 16.18\Omega$$

COLD JUNCTION COMPENSATION:

The temperature reference circuit is shown in Figure 11. The diode voltage has the form

$$V_D = \frac{KT}{q} \ln \frac{I_{DIODE}}{I_{SAT}}$$

Typically at $T_2 = +25°C$, $V_D = 0.6V$ and $\Delta V_D/\Delta T = -2mV/°C$. R_5 and R_6 form a voltage divider for the diode voltage V_D. The divider values are selected so that the gradient $\Delta V_D/\Delta T$ equals the gradient of the thermocouple at the reference temperature. At +25°C this is approximately 52μV/°C (obtained from standard thermocouple table); therefore,

$$\Delta V_{TC}/\Delta T = \Delta V_D/\Delta T \left(\frac{R_6}{R_5 + R_6}\right) \quad (2)$$

$$52\mu V/°C = 200\mu V/°C \left(\frac{R_6}{R_5 + R_6}\right)$$

R_5 is chosen as 2kΩ to be much larger than the resistance of the diode. Solving for R_6 yields 51Ω.

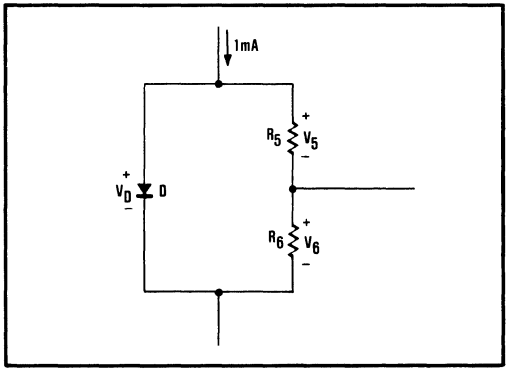


FIGURE 11. Cold Junction Compensation Circuit.

THERMOCOUPLE BURN-OUT INDICATION

In process control applications it is desirable to detect when a thermocouple has burned out. This is typically done by forcing the two-wire transmitter current to either limit when the thermocouple impedance goes very high. The circuits of Figures 16 and 17 inherently have down scale indication. When the impedance of the thermocouple gets very large (open) the bias current flowing into the + input (large impedance) will cause I_O to go to its lower range limit value (about 3.8mA). If up scale indication is desired the circuit of Figure 18 should be used. When the TC opens the output will go to its upper range limit value (about 25mA or higher).

OPTIONAL INPUT OFFSET VOLTAGE TRIM

The XTR101 has provisions for nulling the input offset voltage associated with the input amplifiers. In many applications the already low offset voltages (30μV max for the B grade, 60μV max for the A grade) will not need to be nulled at all. The null adjustment can be done with a potentiometer at pins 1, 2, and 14 as shown in Figures 5 and 6. Either of these two circuits may be used. NOTE: It is not recommended to use this input offset voltage nulling capability for elevation or suppression. See the Signal Suppression and Elevation section for the proper techniques.

OPTIONAL BANDWIDTH CONTROL

Low-pass filtering is recommended where possible and can be done by either one of two techniques shown in Figure 12. C_2 connected to pins 3 and 4 will reduce the bandwidth with a cutoff frequency given by,

$$f_{CO} = \frac{15.9}{(R_1 + R_2 + R_3 + R_4)\ (C_2 + 3pF)}$$

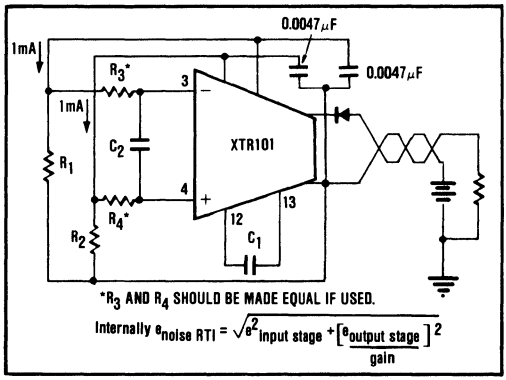


FIGURE 12. Optional Filtering.

This method has the disadvantage of having f_{CO} vary with R_1, R_2, R_3, R_4, and it may require large values of R_3 and R_4. The other method, using C_1, will use smaller values of capacitance and is not a function of the input resistors. It is, however, more subject to nonlinear distortion caused by slew rate limiting. This is normally not a problem with the slow signals associated with most process control transducers. The relationship between C_1 and f_{CO} is shown in the Typical Performance Curves.

APPLICATION CIRCUITS

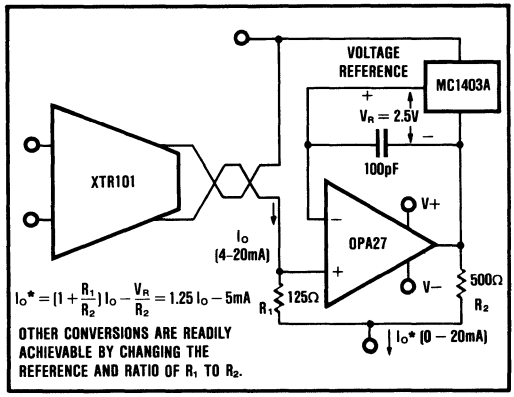


FIGURE 13. 0mA to 20mA Output Converter.

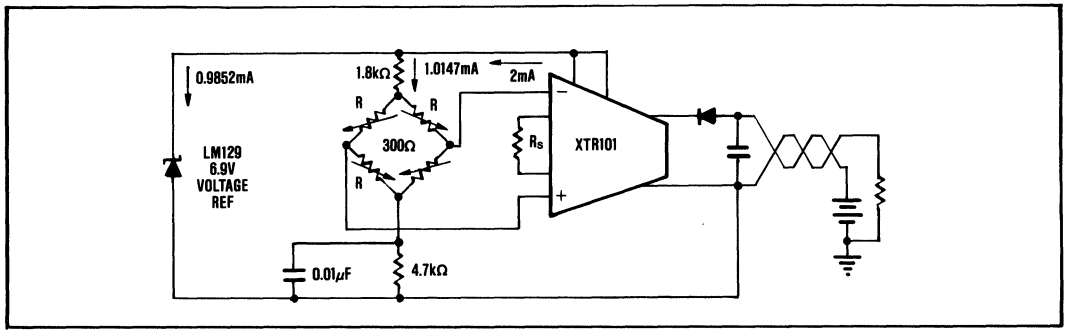


FIGURE 14. Bridge Input, Voltage Excitation.

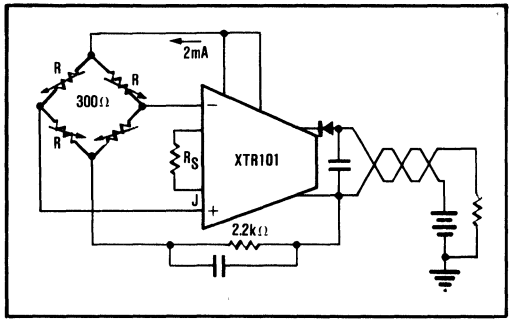


FIGURE 15. Bridge Input, Current Excitation.

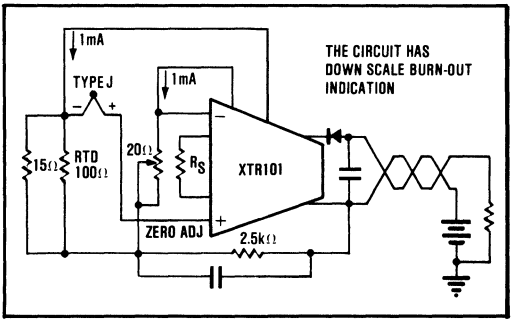


FIGURE 16. Thermocouple Input with RTD Cold Junction Compensation.

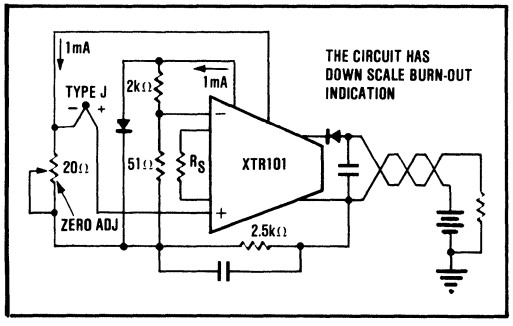


FIGURE 17. Thermocouple Input with Diode Cold Junction Compensation.

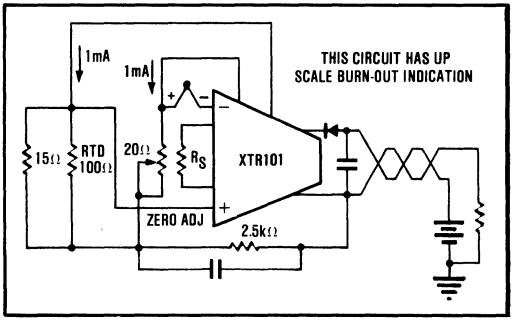


FIGURE 18. Thermocouple Input with RTD Cold Junction Compensation.

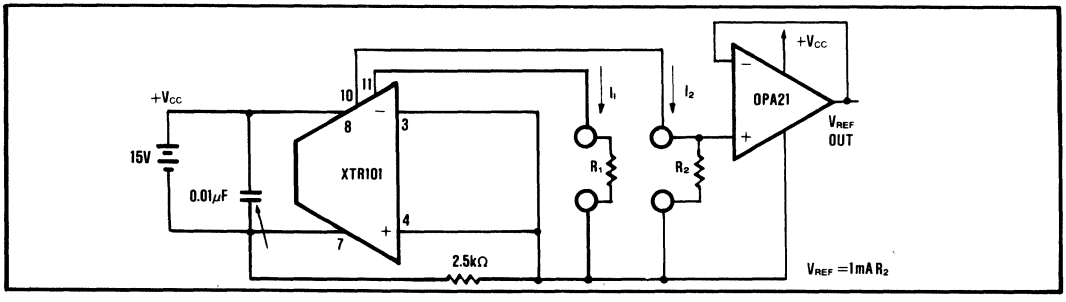


FIGURE 19. Dual Precision Current Sources Operated From One Supply.

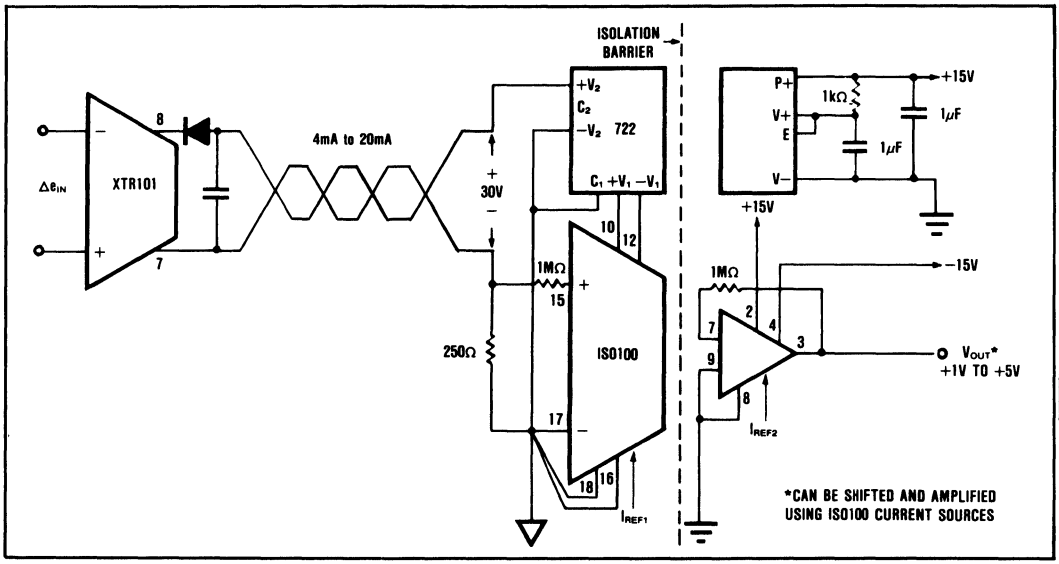


FIGURE 20. Isolated Two-Wire Current Loop.

DETAILED ERROR ANALYSIS

The ideal output current is

$$i_{O\ IDEAL} = 4mA + K\ e_{IN} \quad (3)$$

K is the span (gain) term, $(0.016\Omega + (40/R_S))$

In the XTR101 there are three major components of error:

1. σ_O = errors associated with the **output stage.**
2. σ_S = errors associated with **span adjustment.**
3. σ_I = errors associated with the **input stage.**

The transfer function including these errors is

$$i_{O\ ACTUAL} = (4mA + \sigma_O) + K\ (1 + \sigma_S)(e_{IN} + \sigma_I) \quad (4)$$

When this expression is expanded, second order terms ($\sigma_S\ \sigma_I$) dropped, and terms collected, the result is

$$i_{O\ ACTUAL} = (4mA + \sigma_O) + K\ e_{IN} + K\sigma_I + K\sigma_S\ e_{IN} \quad (5)$$

The error in the output current is $i_{O\ ACTUAL} - i_{O\ IDEAL}$ and can be found by subtracting equations (5) and (3).

$$i_{O\ ERROR} = \sigma_O + K\sigma_I + K\sigma_S\ e_{IN} \quad (6)$$

This is a general error expression. The composition of each component of error depends on the circuitry inside the XTR101 and the particular circuit in which it is applied. The circuit of Figure 9 will be used to illustrate the principles.

1. $\sigma_O = I_{OS\ RTO}$ (7)
2. $\sigma_S = \epsilon_{NONLINEARITY} + \epsilon_{SPAN}$ (8)
3. $\sigma_I = V_{OSI} + (I_{B1}\ R_4 - I_{B2}\ R_T) + \dfrac{\Delta V_{CC}}{PSRR} + \dfrac{(e_1 + e_2)/2 - 5V}{CMRR}$ (9)

The term in parentheses may be written in terms of offset current and resistor mismatches as $I_{B1}\ \Delta R + I_{OS}'\ R_4$.

V_{OSI}* = input offset voltage
I_{B1}*, I_{B2}* = input bias current
I_{OSI}* = input offset current
I_{OSRTO}* = output offset current error
$\Delta R = R_T - R_4$ = mismatch in resistor
ΔV_{CC} = change supply voltage between pins 7 and 8 away from 24V nominal
PSRR* = power supply rejection ratio
CMRR* = common-mode rejection ratio
ϵ_{NONLIN}* = span nonlinearity
ϵ_{SPAN}* = span equation error. Untrimmed error = 5% max. May be trimmed to zero.

Items marked with an asterisk (*) can be found in the Electrical Specifications.

EXAMPLE 3

The circuit in Figure 9 with the XTR101BG specifications and the following conditions: $R_T = 109.4\Omega$ at 25°C, $R_T = 156.4\Omega$ at 150°C, $I_O = 4mA$ at 25°C, $I_O = 20mA$ at 150°C, $R_S = 123.3\Omega$, $R_4 = 109\Omega$, $R_L = 250\Omega$, $R_{LINE} = 100\Omega$, $V_{DI} = 0.6V$, $V_{PS} = 24V \pm 0.5\%$. Determine the % error at the upper and lower range values.

A. AT THE LOWER RANGE VALUE (T = +25°C).

$$\sigma_O = I_{OSRTO} = \pm 6\mu A$$

$$\sigma_I = V_{OSI} + (I_{B1}\ \Delta R + I_{OSI}\ R_4) + \frac{\Delta V_{CC}}{PSRR} + \frac{(e_1 + e_2)/2 - 5V}{CMRR}$$

$$\Delta R = R_{T25°C} - R_4 = 109.4 - 109 \approx 0$$

$$\Delta V_{CC} = (24 \times 0.005) + 4mA\ (250\Omega + 100\Omega) + 0.6V$$
$$= 120mV + 1400mV + 600mV$$
$$= 2120mV$$

$e_1 = (2mA \times 2.5k\Omega) + (1mA \times 109\Omega) = 5.109V$

$e_2 = (2mA \times 2.5k\Omega) + (1mA \times 109.4\Omega)$
$= 5.1094V$

$(e_1 + e_2)/2 - 5 = 0.1092V$

$PSRR = 3.16 \times 10^5$ for 110dB

$CMRR = 31.6 \times 10^3$ for 90dB

$$\sigma_I = 30\mu V + (150nA \times 0 + 20nA \times 109\Omega) + \frac{2120mV}{3.16 \times 10^5} + \frac{0.1092V}{31.6 \times 10^3} \quad (10)$$
$= \mathbf{30\mu V} + 2.18\mu V + 6.7\mu V + 3.46\mu V$
$= 42.34\mu V$

$\sigma_S = \epsilon_{NONLIN} + \epsilon_{SPAN}$
$= 0.0001 + 0$ (assumes trim of R_S)

I_O error $= \sigma_O + \mathbf{K}\ \sigma_I + \mathbf{K}\ \sigma_S\ e_{IN}$

$$K = 0.016 + \frac{40}{R_S} = 0.016 + \frac{40}{123.3\Omega} = 0.340\text{Ʊ}$$

$e_{IN} = e_2 - V_4 = I_{REF1}\ R_{T25°C} - I_{REF2}\ R_4$

since $R_{T25°C} = R_4$,

$e_{IN} = (I_{REF1} - I_{REF2})\ R_4 = 0.4\mu A \times 109\Omega$
$= 43.6\mu V$

Since the maximum mismatch of the current references is 0.04% of 1mA = 0.4μA,

I_O error $= 6\mu A + (0.34\text{Ʊ} \times 42.34\mu V) + (0.34\text{Ʊ} \times 0.0001 \times 43.6\mu V) = 6\mu A + 14.40\mu A + 0.0015\mu A$
$= \mathbf{20.40\mu A}$

$$\%\ \text{error} = \frac{20.40\mu A}{16mA} \times 100\% =$$

0.13% of span at lower range value.

B. AT THE UPPER RANGE VALUE (T = +150°C).

$\Delta R = R_{T150°C} - R_4 = 156.4 - 109.4 = 47\Omega$

$\Delta V_{CC} = (24 \times 0.005) + 20mA\ (250\Omega + 100\Omega) + 0.6V = 7720mV$

$e_1 = 5.109V$

$e_2 = (2mA \times 2.5k\Omega) + (1mA \times 156.4\Omega)$
$= 5.156V$

$(e_1 + e_2)/2 - 5V = 0.1325V$

$\sigma_O = \mathbf{6\mu A}$

$$\sigma_I = \mathbf{30\mu V} + (\mathbf{150nA} \times 47\Omega + 20nA \times 109\Omega) + \frac{7720mV}{3.16 \times 10^5} + \frac{0.1325V}{31.6 \times 10^3}$$
$= 30\mu V + 9.23\mu V + 24\mu V + 4.19\mu V$
$= 67.42\mu V$

$\sigma_S = 0.0001$

$e_{IN} = e_2' - V_4 = I_{REF1}\ R_{T150°C} - I_{REF2}\ R_4 =$
$(1mA \times 156.4\Omega) - (1mA \times 109\Omega) = 47mV$

I_O error $= \sigma_O + \mathbf{K}\ \sigma_I + \mathbf{K}\ \sigma_S\ e_{IN} = 6\mu A +$ (11)
$(0.34\text{Ʊ} \times 67.42\mu V) + (0.34\text{Ʊ} \times 0.0001 \times 47000\mu V) = \mathbf{6\mu A + 22.92\mu A} + 1.60\mu A$
$= \mathbf{30.52\mu A}$

$$\%\ \text{error} = \frac{30.52\mu A}{16mA} \times 100\% =$$

0.19% of span at upper range value.

CONCLUSIONS

Lower Range: From equation (10) it is observed that the predominant error term is the input offset voltage (30μV for the B grade). This is of little consequence in many applications. $V_{OS\ RTI}$ can, however, be nulled using the pot shown in Figures 5 and 6. The result is an error of 0.06% of span instead of 0.13% if span.

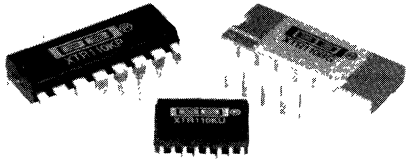
Upper Range: From equation (11), the predominant errors are $I_{OS\ RTO}$ (6μA), $V_{OS\ RTI}$ (30μV), and I_B (150nA), max, B grade. Both I_{OS} and V_{OS} can be trimmed to zero; however, the result is an error of 0.09% of span instead of 0.19% of span.

RECOMMENDED HANDLING PROCEDURES FOR INTEGRATED CIRCUITS

All semiconductor devices are vulnerable, in varying degrees, to damage from the discharge of electrostatic energy. Such damage can cause performance degradation or failure, either immediate or latent. As a general practice, we recommend the following handling procedures to reduce the risk of electrostatic damage.

1. Remove the static-generating materials, such as untreated plastic, from all areas that handle microcircuits.
2. Ground all operators, equipment, and work stations.
3. Transport and ship microcircuits, or products incorporating microcircuits, in static-free, shielded containers.
4. Connect together all leads of each device by means of a conductive material, when the device is not connected into a circuit.
5. Control relative humidity to as high a value as practical (50% recommended).

BURR-BROWN®



XTR110

PRECISION VOLTAGE-TO-CURRENT CONVERTER/TRANSMITTER

FEATURES

- 4mA TO 20mA TRANSMITTER
- SELECTABLE INPUT/OUTPUT RANGES:
  0V to +5V, 0V to +10V Inputs
  0mA to 20mA, 5mA to 25mA Outputs
  Other Ranges
- 0.005% MAX NONLINEARITY, 14 BIT
- PRECISION +10V REFERENCE OUTPUT
- SINGLE SUPPLY OPERATION
- CURRENT SOURCING TO COMMON
- WIDE SUPPLY RANGE, 13.5V TO 40V

APPLICATIONS

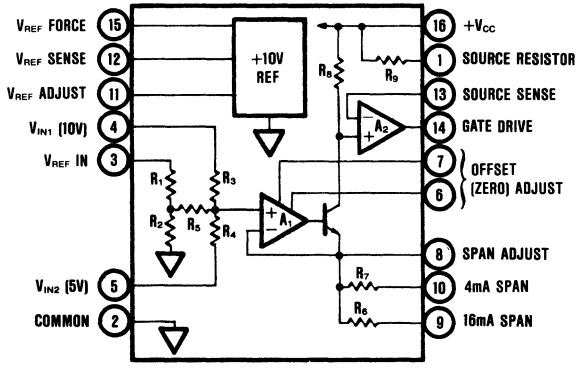
- INDUSTRIAL PROCESS CONTROL
- PRESSURE/TEMPERATURE TRANSMITTERS
- CURRENT-MODE BRIDGE EXCITATION
- GROUNDED TRANSDUCER CIRCUITS
- CURRENT SOURCE REFERENCE FOR DATA ACQUISITION
- PROGRAMMABLE CURRENT SOURCE FOR TEST EQUIPMENT
- AUTOMATED MANUFACTURING
- POWER PLANT/ENERGY SYSTEM MONITORING

DESCRIPTION

The XTR110 is a monolithic precision voltage-to-current converter. It can convert standard 0V to +10V or 0V to +5V inputs into 4mA to 20mA, or 5mA to 25mA outputs. The required external MOS transistor keeps heat outside the XTR110 package to optimize performance under all output conditions.

A precision +10V reference output can drive 10mA. An external transistor can be added for more current, e.g. 33mA for 300Ω bridges.

The XTR110 is a key data acquisition component, designed for high noise immunity current-mode transmission. It is also ideal as a precision programmable current source for transducer circuits and test equipment.



International Airport Industrial Park · P.O. Box 11400 · Tucson, Arizona 85734 · Tel. (602) 746-1111 · Twx 910-952-1111 · Cable BBRCORP · Telex 66-6491

PDS-555C

SPECIFICATIONS

ELECTRICAL

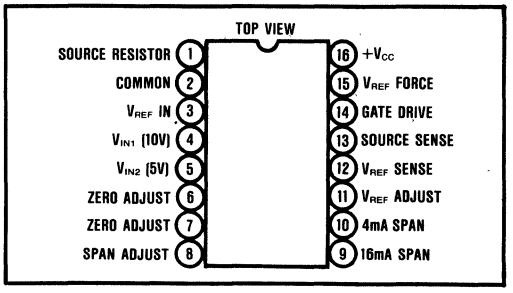
At T_A = +25°C and V_{CC} = +24V and R_L = 250Ω† unless otherwise specified

PARAMETER	CONDITIONS	XTR110AG/KP/KU MIN	XTR110AG/KP/KU TYP	XTR110AG/KP/KU MAX	XTR110BG MIN	XTR110BG TYP	XTR110BG MAX	UNITS
TRANSMITTER								
Transfer Function			$I_O = 10\ [(V_{REF}IN/16) + (V_{IN1}/4) + (V_{IN2}/2)]/R_{SPAN}$					
Input Range: V_{IN1} [5]	Specified performance	0		+10	*		*	V
V_{IN2}	Specified performance	0		+5	*		*	V
Current, I_O	Specified performance [1]	4		20	*		*	mA
	Derated performance [1]	0		40	*		*	mA
Nonlinearity	16mA/20mA span [2]		0 01	0 025		0 002	0 005	% of span
Offset Current, I_{OS}	I_O = 4mA [1]							
Initial	[1]		0 2	0 4		0 02	0 1	% of span
vs Temp	[1]		0 0003	0 005		*	0 003	% of span/°C
vs Supply, V_{CC}	[1]		0 0005	0.005		*	*	% of span/V
Span Error	I_O = 20mA							
Initial	[1]		0 3	0 6		0 05	0 2	% of span
vs Temp	[1]		0 0025	0 005		0 0009	0 003	% of span/°C
vs Supply, V_{CC}	[1]		0 003	0 005		*	*	% of span/V
Output Resistance	From drain of FET (Q_{EXT}) [3]		10×10^{9}			*		Ω
Input Resistance	V_{IN1}		27			*		kΩ
	V_{IN2}		22			*		kΩ
	V_{REF} IN		19			*		kΩ
Dynamic Response								
Settling Time	To 0 1% of span		15			*		µsec
	To 0 01% of span		20			*		µsec
Slew Rate			1 3			*		mA/µsec
VOLTAGE REFERENCE								
Output Voltage		+9 95	+10	+10 05	+9 98	*	+10.02	V
vs Temp			35	50		15	30	ppm/°C
vs Supply, V_{CC}	Line regulation		0 0002	0 005		*	*	%/V
vs Output Current	Load regulation		0 0005	0 01		*	*	%/mA
vs Time			100			*		ppm/1k hrs
Trim Range		−0.100		+0 25	*		*	V
Output Current	Specified performance	10			*			mA
POWER SUPPLY								
Input Voltage, V_{CC}		+13 5		+40	*		*	V
Quiescent Current	Excluding I_O		3	4 5		*	*	mA
TEMPERATURE RANGE								
Specification AG, BG		−40		+85	*		*	°C
KP, KU		0		+70				°C
Operating AG BG		−55		+125	*		*	°C
KP, KU		−25		+85				°C

* Specification same as AG/KP grades † Specifications apply to the range of R_L shown in Typical Performance Curves

NOTES: (1) Including internal reference (2) Span is the change in output current resulting from a full-scale change in input voltage. (3) Within compliance range limited by ($+V_{CC}$ − 2V) $+V_{DS}$ required for linear operation of the FET. (4) For V_{REF} adjustment circuit see Figure 4. (5) For extended I_{REF} drive circuit see Figure 8. (5) Unit may be damaged. See "Input Voltage Range" on next page

PIN CONFIGURATION



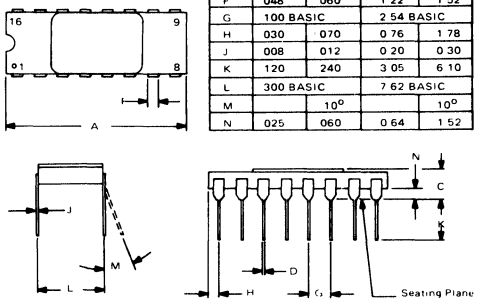
ABSOLUTE MAXIMUM RATINGS

Power Supply, $+V_{CC}$	40V
Input Voltage, $V_{IN\ 1}$, $V_{IN\ 2}$, $V_{REF\ IN}$	$+V_{CC}$
Storage Temperature Range A, B	−55°C to +125°C
K, U	−40°C to +85°C
Lead Temperature	
(soldering, 10s) G, P	300°C
(wave soldering, 3s) U	260°C
Output Short-Circuit Duration, Gate Drive and V_{REF} Force	Continuous to common and $+V_{CC}$
Output Current Using Internal 50Ω Resistor	40mA

MECHANICAL

G Package - 16-pin Hermetic Ceramic DIP

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	790	810	20 07	20 57
C	105	170	2 67	4 32
D	015	021	0 38	0 53
F	048	060	1 22	1 52
G	100 BASIC		2 54 BASIC	
H	030	070	0 76	1 78
J	008	012	0 20	0 30
K	120	240	3 05	6 10
L	300 BASIC		7 62 BASIC	
M		10°		10°
N	025	060	0 64	1 52

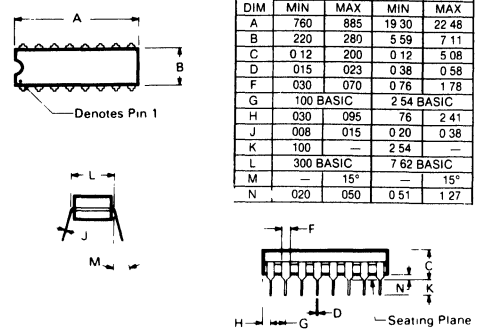


NOTE Leads in true position within .010" (.25mm) R at MMC at seating plane

Pin numbers shown for reference only
Numbers may not be marked on package

P Package - 16-pin Plastic DIP

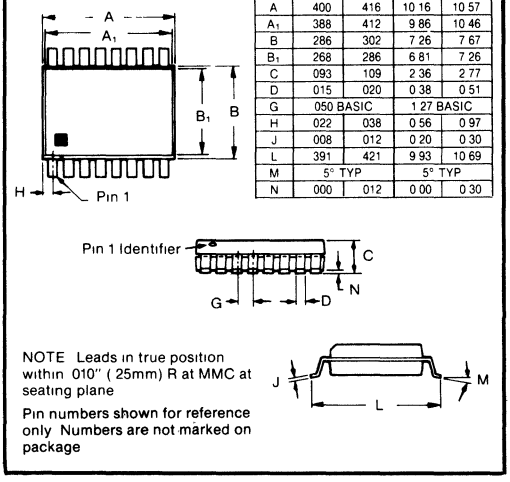
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	760	885	19 30	22 48
B	220	280	5 59	7 11
C	0 12	200	0 12	5 08
D	015	023	0 38	0 58
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	030	095	76	2 41
J	008	015	0 20	0 38
K	100	—	2 54	—
L	300 BASIC		7 62 BASIC	
M	—	15°	—	15°
N	020	050	0 51	1 27



NOTE
Leads in true position within 0 01"
(0 25mm) R at MMC at seating plane

U Package - 16-pin SOIC

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	400	416	10 16	10 57
A_1	388	412	9 86	10 46
B	286	302	7 26	7 67
B_1	268	286	6 81	7 26
C	093	109	2 36	2 77
D	015	020	0 38	0 51
G	050 BASIC		1 27 BASIC	
H	022	038	0 56	0 97
J	008	012	0 20	0 30
L	391	421	9 93	10 69
M	5° TYP		5° TYP	
N	000	012	0 00	0 30



NOTE Leads in true position within .010" (.25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers are not marked on package

ORDERING INFORMATION

Model	Package	Temperature Range
XTR110AG	Ceramic DIP	-40°C to +85°C
XTR110BG	Ceramic DIP	-40°C to +85°C
XTR110KP	Plastic DIP	0°C to +70°C
XTR110KU	Plastic SOIC	0°C to +70°C

BURN-IN SCREENING OPTION
See text for details

Model	Package	Burn-In Temp. (160h)[1]
XTR110AG-BI	Ceramic DIP	+125°C
XTR110BG-BI	Ceramic DIP	+125°C
XTR110KP-BI	Plastic DIP	+85°C
XTR110KU-BI	Plastic SOIC	+85°C

NOTE (1) Or equivalent combination See text

BURN-IN SCREENING

Burn-in screening is an option available for both plastic- and ceramic-packaged XTR110s. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

INPUT VOLTAGE RANGE

The XTR110 can be damaged if the inputs are taken below pin 2 (COMMON). Under carefully controlled conditions, the input can be allowed to go below system ground. To determine the allowable range for the input, use the following equation:

$$(V_{REF}\ IN/16) + (V_{IN1}/4) + (V_{IN2}/2) = 0$$

For example, assume that the standard configuration of Figure 1 is being used. In this case, $V_{REF}IN = 10V$ and $V_{IN2} = 0V$. The equation now becomes:

$$(10/16) + (V_{IN1}/4) + (0/2) = 0$$

Rearranging gives:

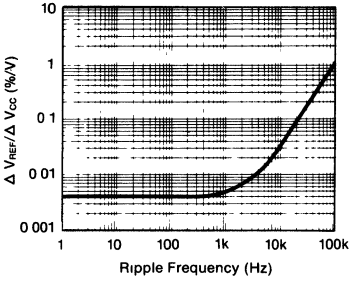
$$V_{IN1} = -2.5V$$

which is the maximum negative voltage that the input can be taken to. Note, however, that this applies only as long as there is 10V at $V_{REF}IN$. If, for example, the supply for the XTR110 is interrupted, the 10V will no longer be generated and any negative input at V_{IN1} could damage the unit.

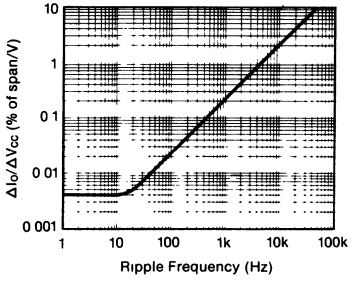
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = 24VDC, R_L = 250Ω unless otherwise noted.

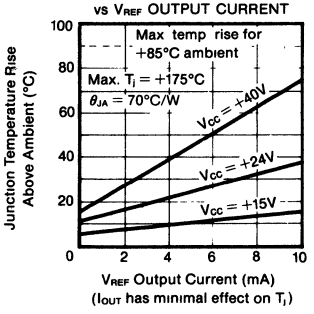
V_{REF} LINE REGULATION vs FREQUENCY



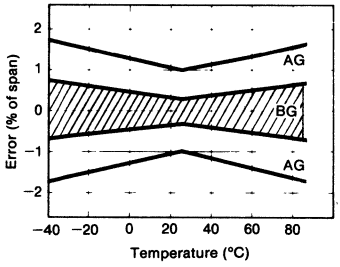
I_O POWER SUPPLY REJECTION vs FREQUENCY



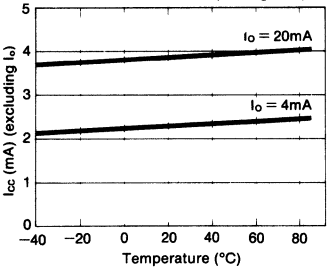
JUNCTION TEMPERATURE RISE vs V_{REF} OUTPUT CURRENT



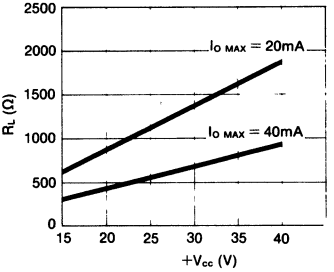
TOTAL OUTPUT ERROR vs TEMPERATURE



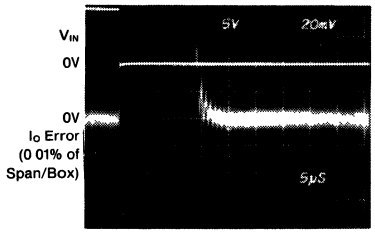
I_{CC} VS TEMPERATURE (see Figure 1)



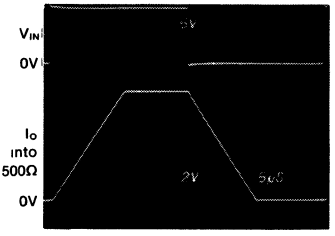
MAXIMUM R_L vs V_{CC}



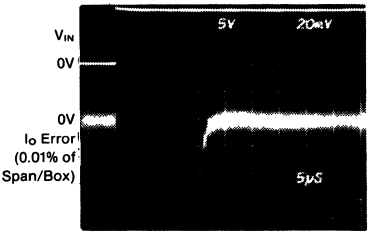
SETTLING TIME WITH NEG V_{IN} STEP



PULSE RESPONSE



SETTLING TIME WITH POS V_{IN} STEP



THEORY OF OPERATION

The XTR110 is designed to convert a high level input voltage into a positive output current.

A block diagram of the XTR110 is shown in Figure 1. The circuit contains four main functional blocks: (1) a precision resistor divider network (R_1–R_5), (2) a voltage-to-current converter (A_1, Q_1, R_6, R_7), (3) a current-to-current converter (A_2, R_8, R_9, Q_{LX1}), and (4) a precision +10V reference.

The precision divider network sums three input voltages to the noninverting input of A_1. These are V_{IN1} (10V full scale), V_{IN2} (5V full scale), and V_{REF} IN (for offsetting).

In the voltage-to-current converter, the op amp, A_1, forces its input voltage across the span setting resistors, R_6 and R_7. Since Q_1 is a high gain Darlington, base current error is negligible and all current flows to the current-to-current converter (into R_8). The transfer function including input divider is as follows:

$$I_{R8} = [(V_{REF}\ IN/16) + (V_{IN1}/4) + (V_{IN2}/2)]/R_{SPAN}$$

where R_{SPAN} is the resistance from Q_1 emitter to common.

The current-to-current converter is the output section of the XTR110 transmitter. The voltage across the 500Ω resistor (R_8) is forced across the 50Ω resistor (R_9) by A_2 and the external MOSFET (Q_{EXT}). Since no current flows in the gate of the MOSFET, all current is delivered to the output. This current (I_{OUT}) is ten times the internal current through R_8. Use of the external transistor keeps power out of the precision IC to maintain accuracy.

The overall transfer function for the XTR110 transmitter is:

$$I_O = 10[(V_{REF}\ IN/16) + (V_{IN1}/4) + (V_{IN2}/2)]/R_{SPAN}.$$

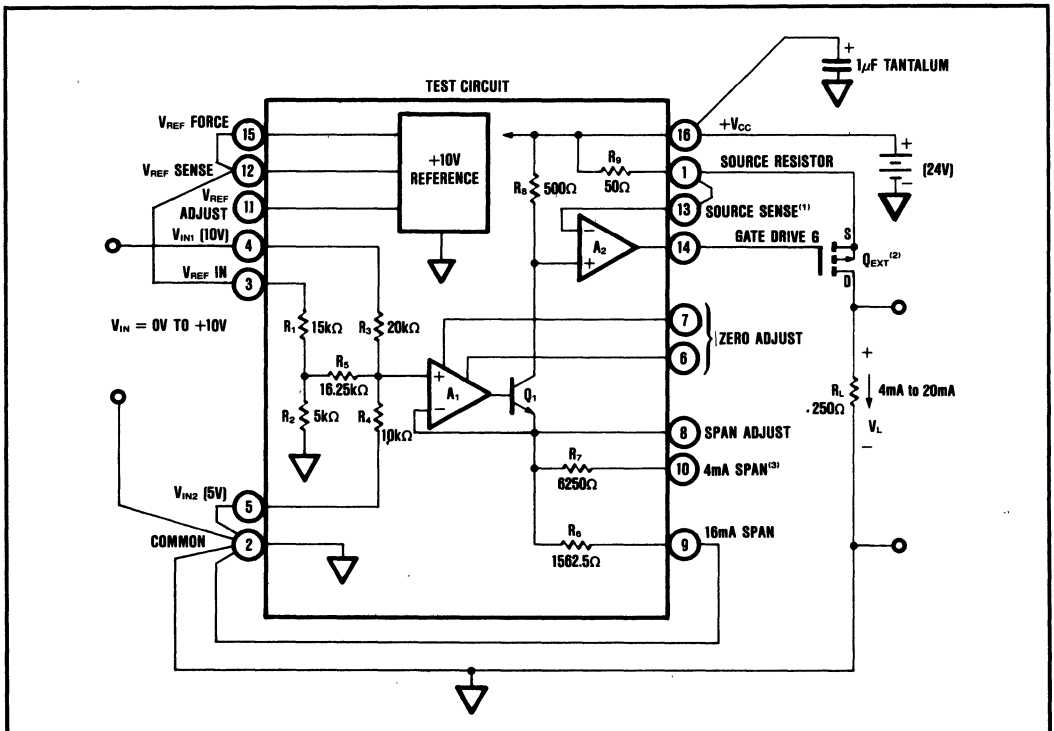
For output currents beyond 40mA an external resistor can be used in place of R_9.

The +10V reference provides input offsetting, e.g. 4mA offset for the 4ma to 20mA output configuration. The reference can deliver 10mA and is protected from shorts to common. Higher current can be provided for other applications by using an external NPN transistor connected to the sense and force pins.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CONNECTION

The basic connection of the XTR110 is the standard 0V to +10V input; 4mA to 20mA output configuration is shown in Figure 1.



NOTES: (1) To maintain accuracy, make a separate direct connection between pins 1 and 13. (2) Q_{EXT} is any P-channel enhancement-mode power MOSFET with appropriate voltage and power rating. PNP bipolar transistors can be used with slight degradation in end-point accuracy and linearity. For recommended devices see section on external transistor. (3) For 20mA span, strap 4mA and 16mA pins together to common.

FIGURE 1. Block Diagram of the XTR110 in Basic Connection: 0V to +10V in, 4mA to 20mA out.

$+V_{CC}$ may originate at the XTR110 site or may be brought in as part of a three-wire twisted line. Be sure to use sufficient bypassing close to the XTR110 on the $+V_{CC}$ line.

EXTERNAL TRANSISTOR

Connections to the MOSFET are gate drive (pin 14) and source resistor (pin 1). To eliminate errors due to resistance in the connection between pin 1 and the source of the external transistor, connect pin 13 directly to pin 1 as shown in Figure 1.

The output of A2, pin 14, is intended to drive a MOSFET or PNP external pass transistor, and for that reason, is atypical of op amp outputs. The output stage can be visualized as a 300μA current source in parallel with an NPN collector. The NPN is the active element that, through feedback, determines where the gate drive should be set. It is capable of sinking over 15mA.

External MOSFET

The XTR110 can operate with a variety of output transistors having appropriate breakdown voltage and power rating which is influenced by package type. Some general observations on package thermal characteristics are listed in Table I.

TABLE I. External Transistor Package Type and Dissipation.

Package Type	Allowable Power Dissipation
TO-92	Lowest Use minimum supply and at +25°C
TO-237	Acceptable Trade-off supply and temperature
TO-39	Good Adequate for majority of designs
TO-220	Excellent For prolonged maximum stress
TO-3	Overkill If nothing else is available

Maximum power dissipation of the external transistor can be derived from the derating curve. It can also be calculated from the thermal characteristics using the equation below:

$$P_A = P_D - (T_A - 25)/\theta_{JA}$$

P_A = Power to be dissipated at T_A
T_A = Maximum ambient temperature
P_D = Maximum continuous power dissipation at +25°C ($I_D V_{DS}$)
θ_{JA} = Junction to ambient thermal resistance

(Refer to the manufacturer's data sheet for required numbers.)

Table II shows suitable MOSFET output transistors.

Summary of points to consider for selecting the transistor are:

1. Power rating—Equal to 1.5 × P_A if possible, or at least equal to P_A.
2. Drain-source breakdown—Greater than maximum expected V_{DS}. This includes any additional voltage that may exist between the transmitter and receiver grounds.
3. Gate-source breakdown—Greater than $+V_{CC}$, because V_{CC} will be applied gate-to-source, under the condition of an open drain line (V_{GATE} then = 0V). Most MOSFETS will tolerate only 20V, but a zener (12V or more) connected gate-to-source will clamp the junction and remain off during normal operation.

TABLE II. Available P-Channel MOSFETs.

Manufacturer	Part No.	BV_{DSS}*	BV_{GS}*	Package
Ferranti	ZVP1304A	−40V	20V	TO-92
	ZVP1304B	−40V	20V	TO-39
	ZVP1306A	−60V	20V	TO-92
	ZVP1306B	−60V	20V	TO-39
International Rectifier	IRF9513	−60V	20V	TO-220
Motorola	MTP8P08	−80V	20V	TO-220
RCA	RFL1P08	−80V	20V	TO-39
	RFT2P08	−80V	20V	TO-220
Siliconix (preferred)	VP0300B	−30V	40V	TO-39
	VP0300L	−30V	40V	TO-92
	VP0300M	−30V	40V	TO-237
	VP0808B	−80V	40V	TO-39
	VP0808L	−80V	40V	TO-92
	VP0808M	−80V	40V	TO-237
Supertex	VP1304N2	−40V	20V	TO-220
	VP1304N3	−40V	20V	TO-92
	VP1306N2	−60V	20V	TO-220
	VP1306N3	−60V	20V	TO-92

*BV_{DSS}—Drain-source breakdown voltage. BV_{GS}—Gate-source breakdown voltage.

External PNP Transistor

A PNP bipolar transistor can also be used for the output but it will result in a slight drop in end-point accuracy and linearity. A TN2905 in a TO-237 package performs adequately. The end point shifts can be calculated if the beta of the PNP is known. The offset shift is I_{OS}/beta and the span shift is I_{SPAN}/beta. For example, if the transistor's beta is 250 and the output range is 4mA to 20mA, the calculations are as follows:

$dI_{OS} = 4mA/250 = 16\mu A$ (0.1% of span)
$dI_{SPAN} = 16mA/250 = 64\mu A$ (0.4% of span)

The offset error can be corrected by using the offset correction circuitry of Figure 5. The span error due to base current loss can be compensated by connecting an external resistor, R_{PAD}, in parallel with the internal resistor as shown in Figure 2. R_{PAD} can be calculated with the following formula:

$$R_{PAD} = 50 \text{ (beta + 1)}$$

Any span error due to the XTR110 itself can be corrected with the span adjust circuitry of Figure 5. Use a nominal beta to calculate the value of R_{PAD} if individual transistor measurements are not made. There should be enough range in the span adjust circuit to compensate for normal tolerances.

Small nonlinearity degradation (0.01% typical at $24V_{CC}$) results from changes in beta caused by changes in power as collector current varies from 4mA to 20mA. A heat sink can be added to minimize the heat dissipation effect.

A Darlington configuration (two separate PNPs) can also be used with no degradation in end-point accuracy and linearity. A 0.047μF capacitor across pins 13 and 14 is required for stability as shown in Figure 3. Single-

packaged Darlingtons with internal bleeder resistors are not recommended since they will severly degrade accuracy.

To select a bipolar transistor, follow the same points as for MOSFETs. Note, however, the base-emitter breakdown is not considered because this junction is forward biased should the collector open.

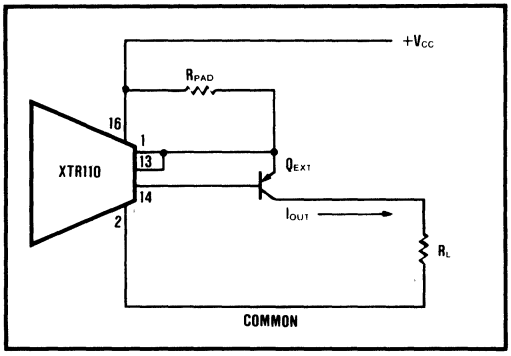


FIGURE 2. PNP Output Transistor (R_{PAD} corrects for span error caused by beta).

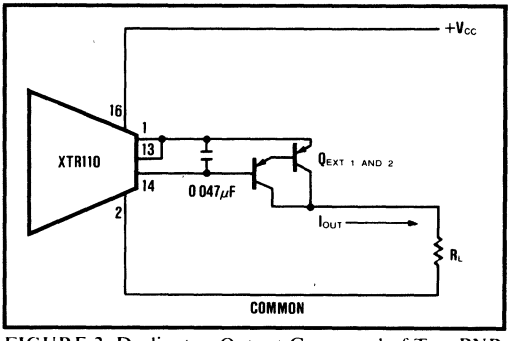


FIGURE 3. Darlington Output Composed of Two PNP Transistors.

COMMONS

Careful attention should be directed toward proper connection of the commons. All commons should be joined at one point as close to pin 2 of the XTR110 as possible. The exception is the I_{OUT} return. It can be returned to any place where it will not modulate the common at pin 2.

VOLTAGE REFERENCE

The reference voltage is accurately regulated at pin 12 (V_{REF} sense). To preserve accuracy, any load including pin 3 should be connected to this point.

The circuit in Figure 4 shows coarse and fine adjustment of the voltage reference.

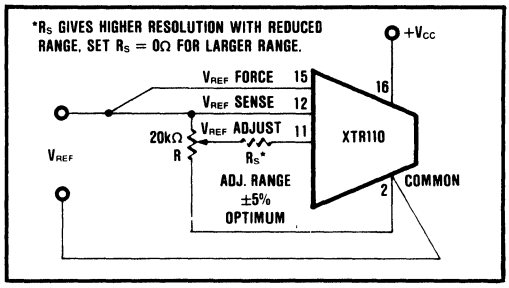


FIGURE 4. Optional Adjustment of Reference Voltage.

OFFSET (ZERO) ADJUSTMENT

The offset current can be adjusted by using the potentiometer, R_1, shown in Figure 5. The procedure is to set the input voltage to zero and then adjust R_1 to give 4mA at the output. For spans starting at 0mA, the following special procedure is recommended: set the input to a small nonzero value and then adjust R_1 to the proper output current. When the input is zero the output will be zero. Figures 6 and 7 show graphically how offset is adjusted.

SPAN ADJUSTMENT

The span is adjusted at the full-scale output current using the potentiometer, R_2, shown in Figure 5. This adjustment is interactive with the offset adjustment, and a few iterations may be necessary. For the circuit shown, set the input voltage to +10V full scale and then adjust R_2 to give 20mA full-scale output. Figures 6 and 7 show graphically how span is adjusted.

The values of R_2, R_3, and R_4 for adjusting the span are determined as follows: choose R_4 in series to slightly decrease the span; then choose R_2 and R_3 to increase the span to be adjustable about the center value.

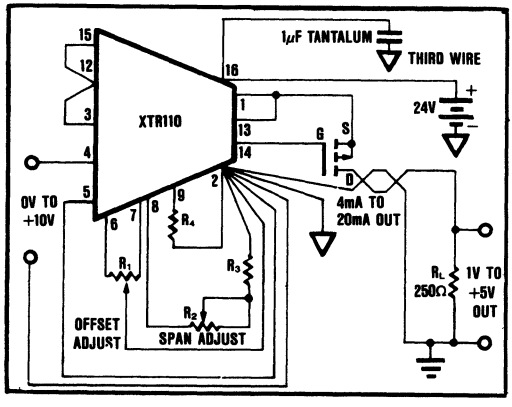


FIGURE 5. Offset and Span Adjustment Circuit for 0V to +10V Input, 4mA to 20mA Output.

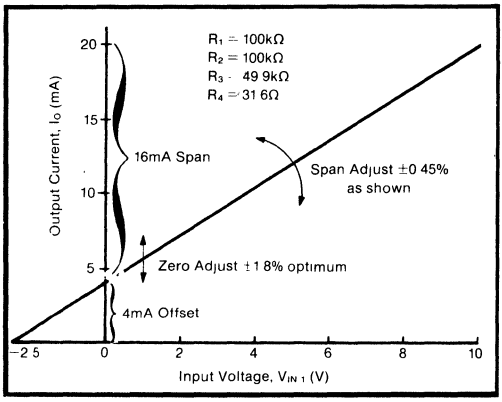


FIGURE 6. Zero and Span of 0V to +10V Input, 4mA to 20mA Output Configuration (see Figure 5).

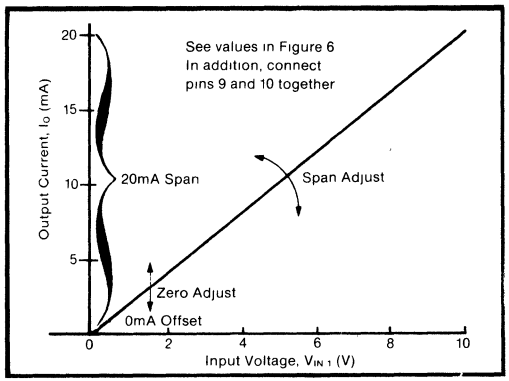


FIGURE 7. Zero and Span of 0V to +10V$_{IN}$, 0mA to 20mA Output Configuration (see Figure 5).

ERROR CALCULATIONS

Errors can be calculated by considering these key parameters:

1. Offset Current (Initial, vs Temperature, vs Supply)
2. Span Error (Initial, vs Temperature, vs Supply)
3. Nonlinearity

Lower errors can readily be obtained by externally adjusting the initial offset and span errors to zero (see Performance Curves).

EXTENDED REFERENCE CURRENT DRIVE

The current drive capability of the XTR110's internal reference is 10mA. This can be extended if desired by adding an external NPN transistor shown in Figure 8.

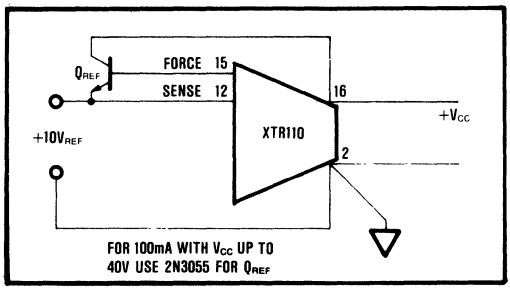


FIGURE 8. Extended Reference Current Drive.

LOW TEMPERATURE COEFFICIENT (TC) OPERATION

Although the precision resistors in the XTR110 track within 1ppm °C, the output current depends upon the absolute temperature coefficient of any one of the resistors, R_6, R_7, R_8, and R_9. Since the absolute TC of the resistors is 20ppm/°C, maximum, the TC of the output current can have 20ppm/°C drift. For low TC operation, zero TC resistors can be substituted for either the span resistors (R_6 or R_7) or for the source resistor (R_9) but not both.

EXTENDED SPAN

For spans beyond 40mA, the internal 50Ω resistor (R_9) may be replaced by an external resistor connected between pins 13 and 16.

Its value can be calculated as follows:

$$R_{EXT} = R_9 \left(Span_{OLD}/Span_{NEW}\right)$$

Since the internal thin-film resistors have a 20% absolute value tolerance, measure R_9 before determining the final value of R_{EXT}. Self-heating of R_{EXT} can cause nonlinearity. Therefore, choose one with a low TC and adequate power rating. See Figure 14 for application.

STANDARD CURRENT RANGES OR SPANS

Table III shows the pin connections for standard XTR110 current ranges.

TABLE III. Pin Connections for Standard Ranges.

Input Range (V)	Output Range (mA)	Pin 3	Pin 4	Pin 5	Pin 9	Pin 10
0 - 10	0 - 20	Com	Input	Com	Com	Com
2 - 10	4 - 20	Com	Input	Com	Com	Com
0 - 10	4 - 20	+10V Ref	Input	Com	Com	Open
0 - 10	5 - 25	+10V Ref	Input	Com	Com	Com
0 - 5	0 - 20	Com	Com	Input	Com	Com
1 - 5	4 - 20	Com	Com	Input	Com	Com
0 - 5	4 - 20	+10V Ref	Com	Input	Com	Open
0 - 5	5 - 25	+10V Ref	Com	Input	Com	Com

TYPICAL APPLICATIONS

The XTR110 is ideal for a variety of applications requiring high noise immunity current-mode signal transmission. The precision +10V reference is convenient and can be exciting for bridges and transducers. Selectable ranges make it very useful as a precision programmable current source. The compact design and low price of the XTR110 allow versatility with a minimum of external components and design engineering expense.

Figures 9 through 16 show typical applications of the XTR110.

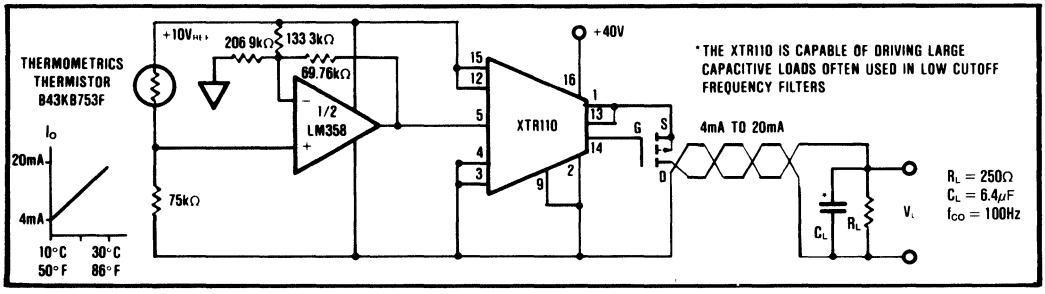


FIGURE 9. 4mA to 20mA Single-Supply Thermistor Transmitter for Energy Management Systems.

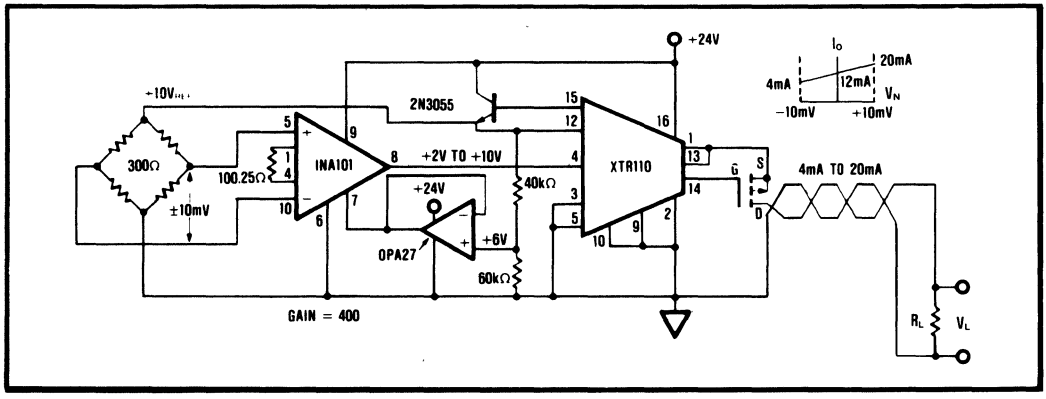


FIGURE 10. 4mA to 20mA Single-Supply Bridge Transmitter.

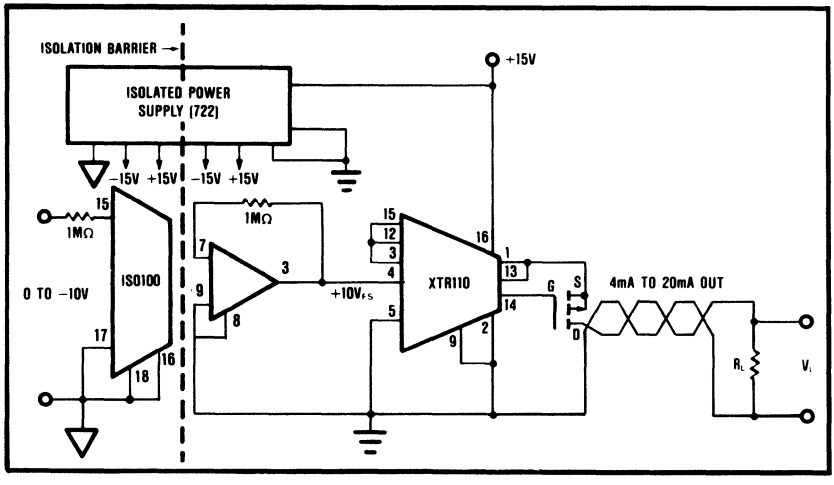


FIGURE 11. Isolated 4mA to 20mA Channel

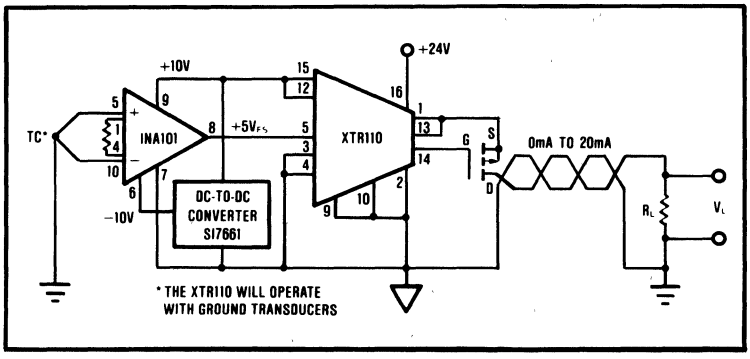


FIGURE 12. 0mA to 20mA Single-Supply Thermocouple Transmitter.

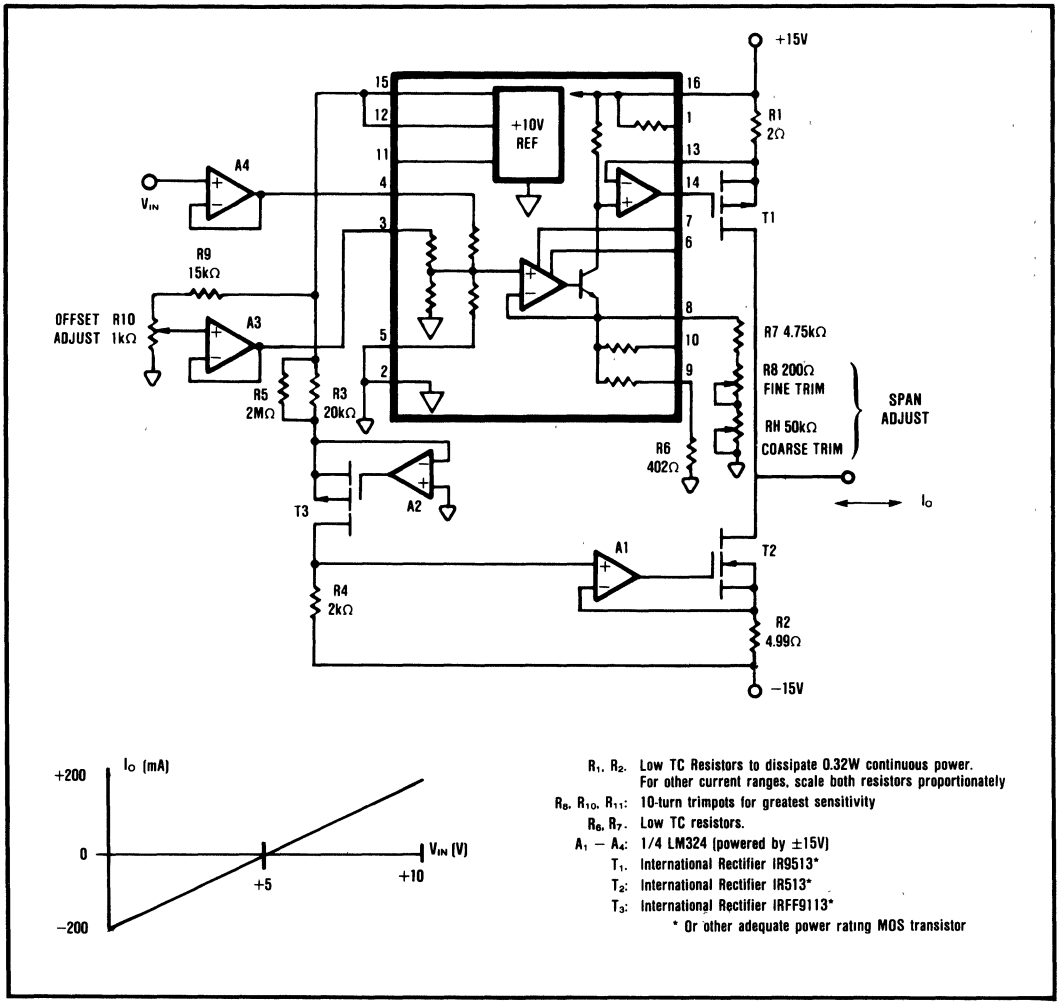


FIGURE 13. ±200mA Current Pump.

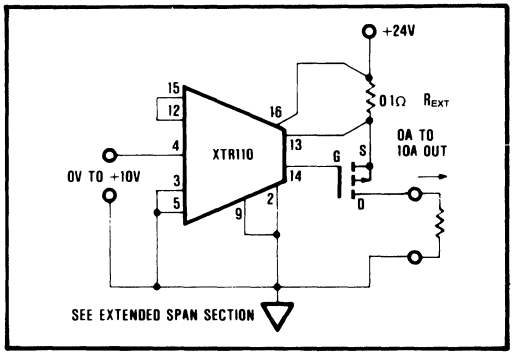


FIGURE 14. 0A to 10A High Current Voltage-to-Current Converter.

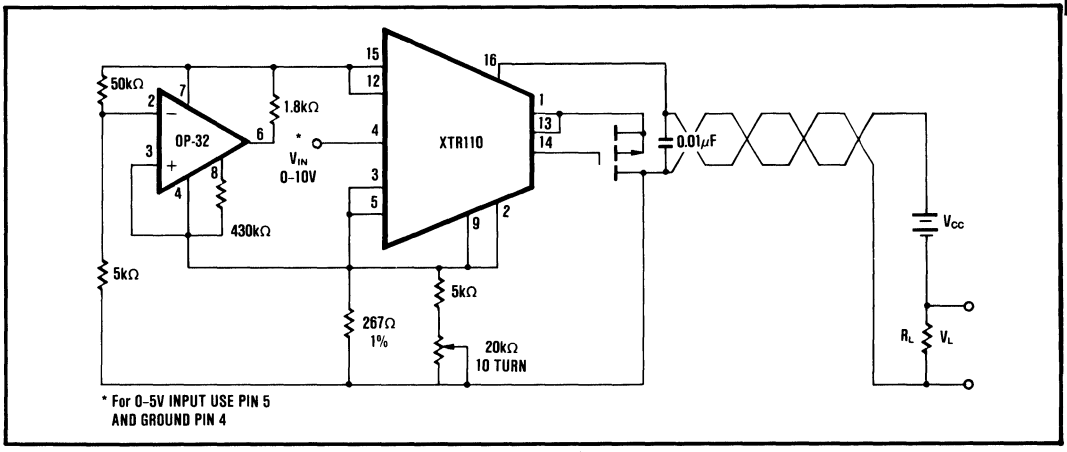


FIGURE 15. High Level Input 4ma to 20mA Two-Wire Transmitter.

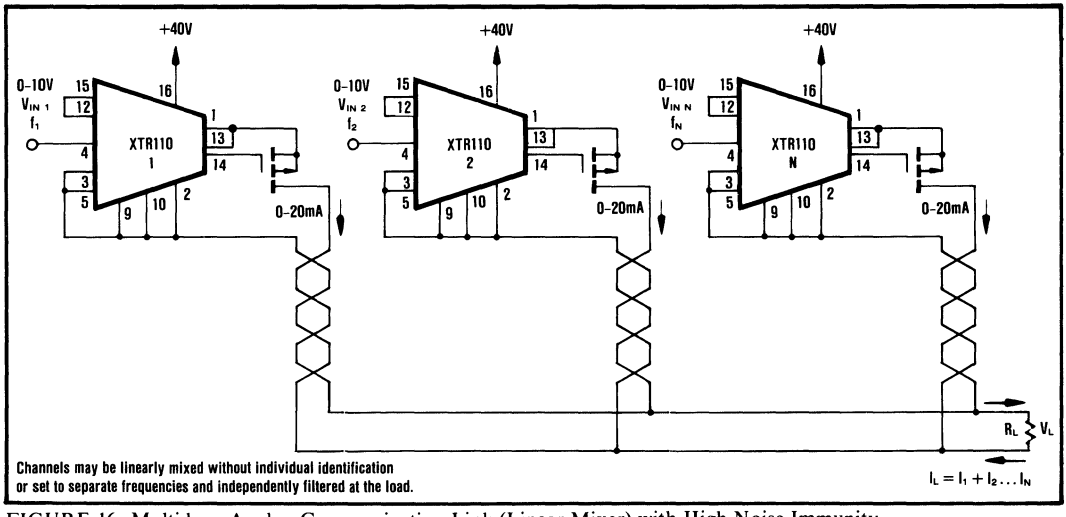
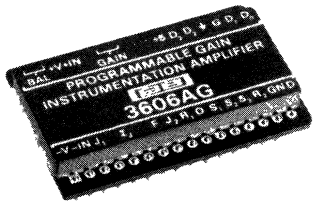


FIGURE 16. Multidrop Analog Communication Link (Linear Mixer) with High Noise Immunity.

BURR-BROWN®

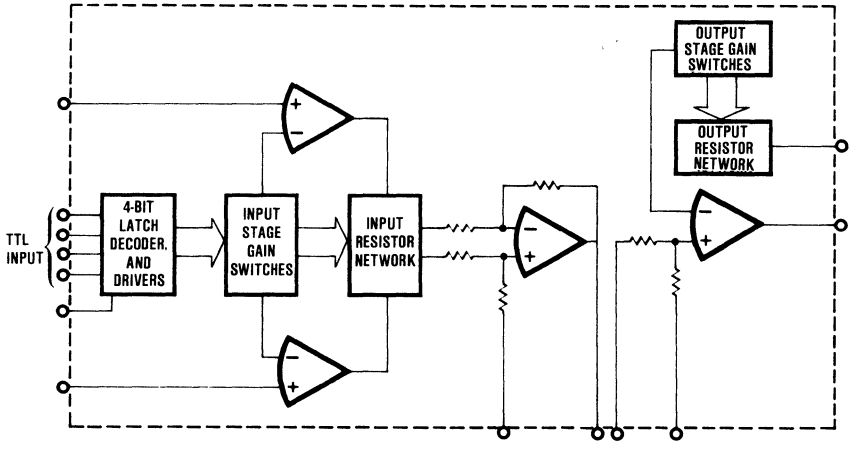
3606



Digitally Controlled Programmable Gain INSTRUMENTATION AMPLIFIER

FEATURES

- 11 BINARY GAINS - 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024V/V
- 4-BIT TTL GAIN CONTROL
- EXCELLENT GAIN NONLINEARITY 0.01% max at G = 1024V/V
- LOW GAIN ERRORS - 0.02% max
- LOW GAIN DRIFT - 10ppm/°C max
- LOW VOLTAGE DRIFT 1μV/°C max RTI, G = 1024V/V
- HIGH CMR - 110dB min, G = 1024V/V
- HIGH INPUT IMPEDANCE - 10 x $10^9\Omega$
- LOW OFFSET VOLTAGE 22μV max RTI, G = 1024V/V 2mV max RTI, G = 1V/V



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PDS-388C

DESCRIPTION

The 3606 is a self-contained, Programmable Gain Instrumentation Amplifier (PGIA) whose gain can be changed in 11 binary weighted steps from 1 to 1024V/V. The gain control is accomplished through a 4-bit TTL input.

The PGIA function allows the user to deal with wide dynamic range signals while maintaining high system resolution. For example: when used with a 10-bit A to D converter in a "floating point" system, the 2^{10} gain range of the 3606, plus the 2^{10} range of the converter produces a total system resolution of 2^{20} (|| 1,000,000:1).

Desirable characteristics of a high performance instrumentation amplifier are offered by the 3606: high input impedance (10GΩ), excellent gain nonlinearity (0.01% max, G = 1024V/V; 0.02% max, G = 1V/V), high common-mode rejection (100dB min, G≥ 4V/V), low gain error (0.02% max with no trimming required), low gain temperature coefficient (10ppm/°C max), and low offset voltage drift vs temperature (1μV/°C max, RTI, G = 1024).

Added to these outstanding instrumentation amplifier characteristics is the ability to change 3606's gain under control of a 4-bit TTL input word. An important characteristic of the 3606 PGIA is its low change in offset plus laser trimming minimized this change to a maximum of ±25mV with no external adjustments. With two simple offset adjustments the change can be limited to less than 2mV (1mV typ) at the output over the entire 1V/V to 1024V/V gain range.

A simplified schematic of the 3606 is shown in Figure 1. The circuit consists of a variable gain high input impedance voltage follower input stage (A1 and A2) followed by a unity gain difference amplifier (A3) with a variable gain output stage (A4).

Common-mode voltage is derived for active guard drive to improve system common-mode rejection. Two-pole, low-pass filtering can easily be implemented on the output stage to reduce noise bandwidth and improve system signal-to-noise operation. A latch function is provided to inhibit gain changes while the digital gain control input is changed.

Burr-Brown's instrumentation grade monolithic operational amplifiers, high stability precision thin-film resistor networks and advanced laser-trimming techniques are used by the 3606 to achieve a performance, size and cost combination never before achieved in a PGIA. It is available in a 32-pin dual-in-line ceramic package.

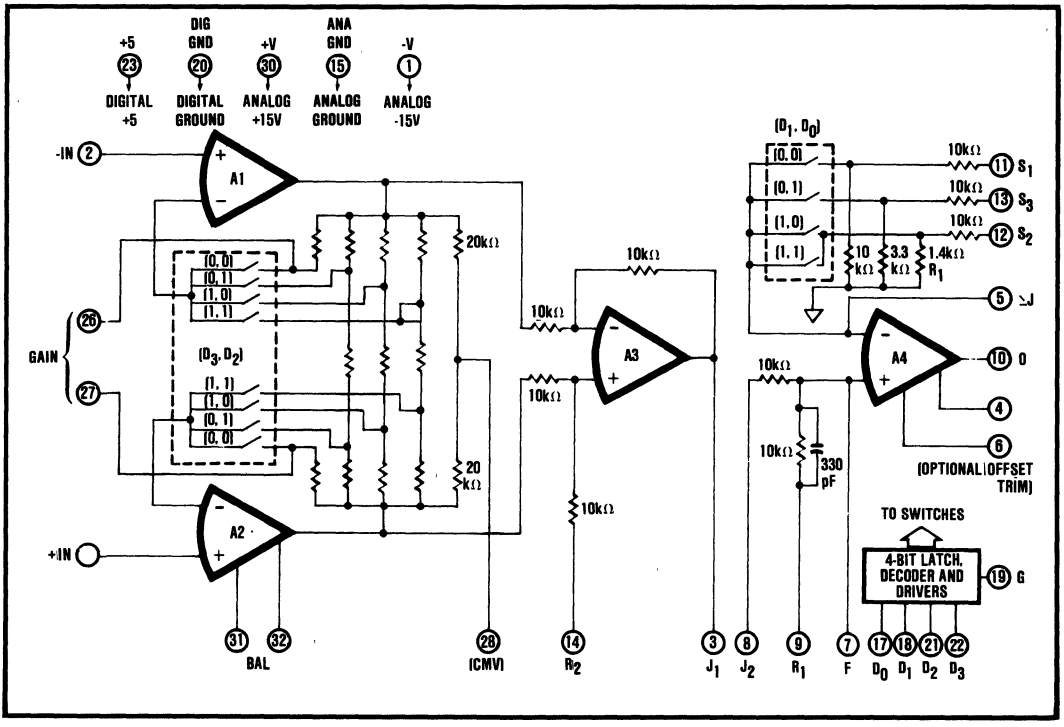


FIGURE 1. Simplified Schematic.

SPECIFICATIONS

ELECTRICAL

Typical at +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	3606A[1] MIN	3606A[1] TYP	3606A[1] MAX	3606B[1] MIN	3606B[1] TYP	3606B[1] MAX	UNITS
GAIN, G[2]								
Inaccuracy	G = 1 to 1024, I_O = 1mA		±0.02	±0.05		±0.01	±0.02	%
Nonlinearity[3]	G = 1 to 16		0.001	0.002		*	*	%(5)
	G = 32 to 128		0.003	0.004		*	*	%
	G = 256 to 1024		0.005	0.01		*	*	%
Drift vs Temperature	G = 1 to 1024		±5	±10		*	*	ppm/°C
vs Time	G = 1 to 1024		±0.01					%/1000 hrs
RATED OUTPUT								
Voltage	I_O = ±5mA	±10	±12		*	*		V
Current	V_O = ±10V	±5	±10		*	*		mA
Impedance			0.05			*		Ω
INPUT CHARACTERISTICS								
Absolute Max Voltage	No damage			±V_{CC}			*	V
Common-Mode Voltage Range	Linear operation	±10	±10.5		*	*		V
Differential Impedance			10 ‖ 3			*		$10^9\Omega$ ‖ pF
Common-Mode Impedance			10 ‖ 3			*		$10^9\Omega$ ‖ pF
OFFSET VOLTAGE, RTO[4]								
Initial at +25°C[5]			±(0.02G +1)	±(0.04G +2)		±(0.01G +1)	±(0.02G +2)	mV
vs Temperature	-25°C to +85°C		(±0.0015G ±0.03G_2)	(±0.003G ±0.05G_2)		(±0.0005G ±0.01G_2)	(±0.001G ±0.02G_2)	mV/°C
vs Time			(±0.001G ±0.01G_2)			*		mV/mo
vs Supply			(±0.002G ±0.04G_2)			*		mV/V
vs Gain[6]	With trimming		±1	±2		*	*	mV
INPUT BIAS CURRENT								
Initial	+25°C		±15	±50		±5	±20	nA
vs Temperature	-25°C to +85°C		±0.3			*		nA/°C
vs Supply Voltage			±0.1			*		nA/V
INPUT DIFFERENCE CURRENT								
Initial	+25°C		±15	±50		±5	±20	nA
vs Temperature	−25°C to +85°C		±0.5			*		nA/°C
vs Supply Voltage			±0.1			*		nA/V
INPUT NOISE								
Voltage	$R_{SOURCE} \leq 5k\Omega$							
0.01Hz to 10Hz	G = 1024		1.4			*		μV, p-p
10Hz to 1kHz			1.0			*		μV, rms
Current								
0.01Hz to 10Hz			70			*		nA, p-p
10Hz to 1kHz			20			*		nA, rms
COMMON-MODE REJECTION								
DC, 1kΩ Source Imbalance								
G = 1, 2		80	90		90	100		dB
G = 4 to 6		90	100		100	110		dB
G = 32 to 1024		100	114		110	114		dB
60Hz, 1kΩ Source Imbalance								
G = 1, 2		80	86		*	*		dB
G = 4 to 16		90	96		*	*		dB
G = 32 to 1024		100	106		*	*		dB
DYNAMIC RESPONSE								
±3dB Response	Small Signal							kHz
G = 1			100			*		kHz
G = 32 to 128			40			*		kHz
G = 256 to 1024			10			*		kHz
±1% Response	Small Signal							
G = 1			40			*		kHz
G = 32 to 128			8			*		kHz
G = 256 to 1024			3			*		kHz
Slew Rate	G = 1	0.2	0.5		*	*		V/μsec
Settling Time	G = 128							
to 1%			75			*		μsec
to 0.1%			100			*		μsec
to 0.01%			200			*		μsec

ELECTRICAL (CONT)

Typical at +25°C, unless otherwise noted

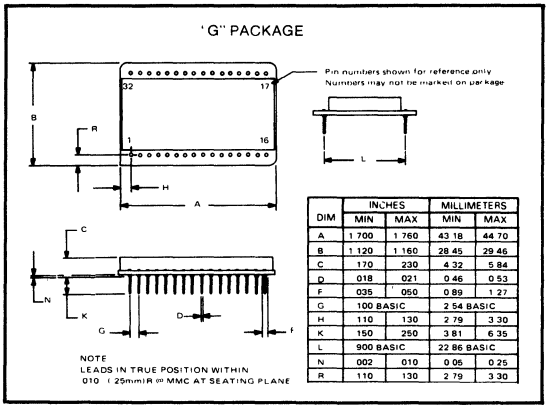
PARAMETER	CONDITIONS	3606A[1] MIN	3606A[1] TYP	3606A[1] MAX	3606B[1] MIN	3606B[1] TYP	3606B[1] MAX	UNITS
LOGIC VOLTAGES								
"0" Level[7]			0	+0 4		*	*	V
"1" Level[7]		+2 4	+5 0		*	*		V
Absolute Max	No damage			+7			*	V
ANALOG SUPPLY								
Rated Voltage			±15			*		VDC
Voltage Range, Derated Performance		±8		±18	*		*	VDC
Current, quiescent			±10	±20		*	*	mA
DIGITAL SUPPLY								
Rated Voltage			+5			*		VDC
Voltage Range		+4 5		+5 5	*		*	VDC
Current quiescent			10			*		mA
TEMPERATURE RANGE								
Specification		-25		+85	*		*	°C
Storage		-40		+100	*		*	°C

*Specifications same as 3606A

NOTES

1 Specify 3606AG or 3606BG for ceramic package
2 $G = G_1 \times G_2$
3 Nonlinearity is the maximum peak deviation from the best straight-line as a percent of full scale peak-to-peak output
4 RTO = Referred To Output. May be referred to input by dividing by gain G
5 May be adjusted to zero
6 Trimmed according to Figure 8
7 All digital inputs are 1 TTL unit load

MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	170	230	4.32	5.84
D	018	021	0.46	0.53
F	035	050	0.89	1.27
G	100 BASIC		2.54 BASIC	
H	110	130	2.79	3.30
K	150	250	3.81	6.35
L	900 BASIC		22.86 BASIC	
N	002	010	0.05	0.25
R	110	130	2.79	3.30

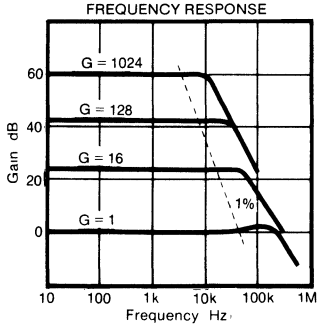
PIN DESIGNATIONS

PIN NO.	DESIG.	FUNCTION	PIN NO.	DESIG.	FUNCTION
1	-V	-15V Analog Supply	17	D_0	Digital Input, LSB
2	-IN	Inverting Input	18	D_1	Digital Input, next LSB
3	J_1	Output of A_3	19	G	Latch
4	(None)	Optional A_4 Offset Trim	20	DIG GND	Digital Ground
5	ΣJ	Summing Junction of A_4	21	D_2	Digital Input, next MSB
6	(None)	Optional A_4 Offset Trim	22	D_3	Digital Input, MSB
7	F	Low-Pass Filter Pin	23	+5	+5 Digital Supply
8	J_2	Input to A_4	24	(None)	No Internal Connection
9	R_1	Output Reference	25	(None)	No Internal Connection
10	O	Output	26	Gain	Optional External Gain
11	S_1	Sense G = 1	27	Gain	Optional External Gain
12	S_2	Sense G = 4	28	(None)	Input CMV
13	S_3	Sense G = 2	29	+IN	Noninverting Input
14	R_2	Output Reference	30	+V	+15V Analog Supply
15	ANA GND	Analog Ground	31	BAL	Optional Input Stage
16	(None)	No Internal Connection	32	BAL	Offset Null

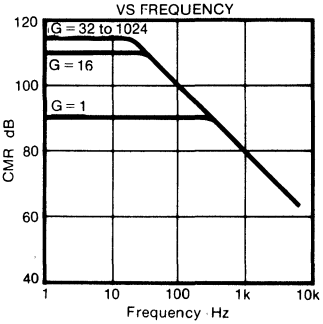
TYPICAL PERFORMANCE CURVES

Typical at +25°C unless otherwise noted

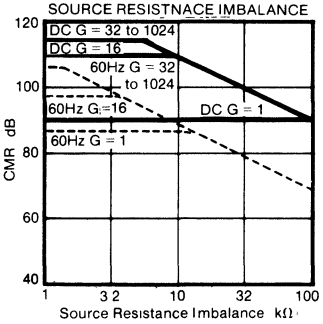
SMALL SIGNAL FREQUENCY RESPONSE



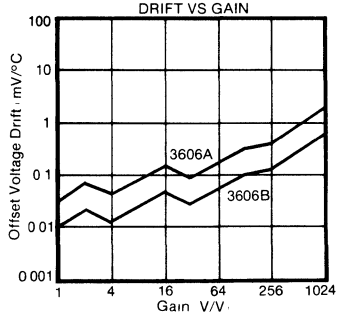
COMMON-MODE REJECTION VS FREQUENCY



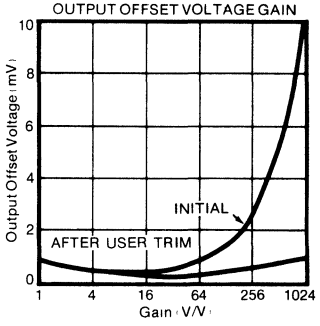
COMMON-MODE REJECTION VS SOURCE RESISTNACE IMBALANCE



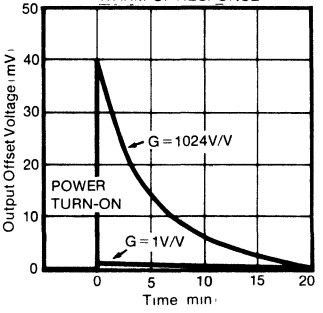
OUTPUT OFFSET VOLTAGE DRIFT VS GAIN



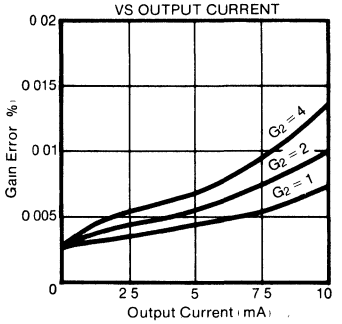
OUTPUT OFFSET VOLTAGE GAIN



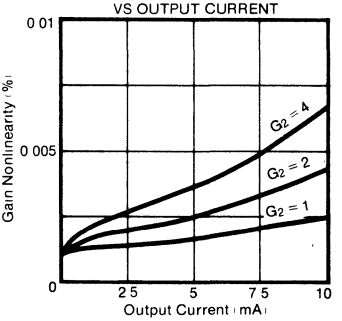
WARM-UP RESPONSE



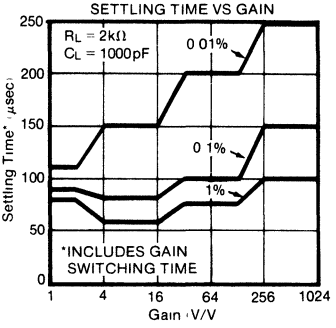
OUTPUT STAGE GAIN ERROR VS OUTPUT CURRENT



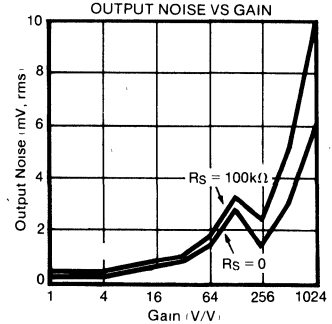
OUTPUT STAGE GAIN NONLINEARITY VS OUTPUT CURRENT



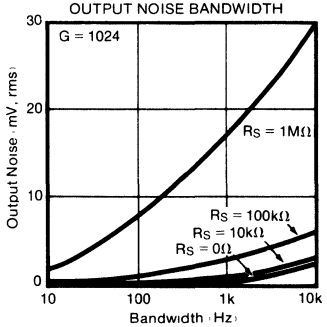
SETTLING TIME VS GAIN



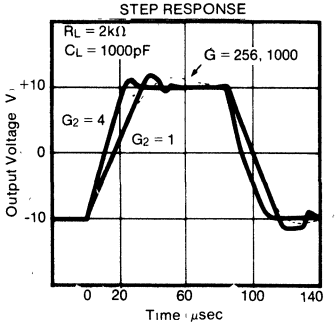
WIDEBAND OUTPUT NOISE VS GAIN



OUTPUT NOISE BANDWIDTH



STEP RESPONSE



INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Figure 2 shows the proper analog and digital power supply connections. The analog supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the amplifier as possible. Because the amplifier is direct-coupled it must have a ground return path for the bias currents associated with the amplifier inputs at pins 2 and 29. If the ground return path is not inherent in the signal source (floating source) it must be provided externally. The ground return resistance (R_{GR}) should be kept as low as practical. An upper limit of approximately 50MΩ is established by the input bias currents of the amplifier and its common-mode voltage.

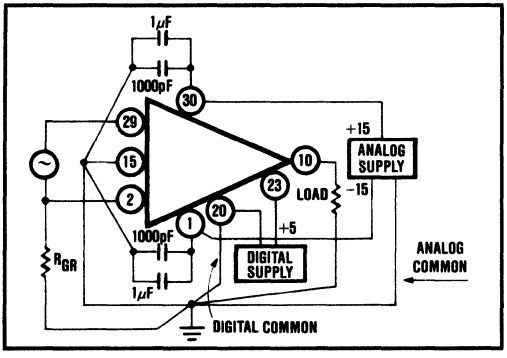


FIGURE 2. Power Supply and Ground Connections.

SIGNAL CONNECTIONS

Basic signal connections are shown in Figure 3. The connection to pin 14 completes the difference amplifier of A_3 (see Figure 1). The 3 to 8 jumper connects the output stage. The pin 9 connection provides a divide-by-two attenuator for the A_4 stage. This is necessary to limit the signal on the output stage switches to maintain signal linearity. The pin 11, 12 and 13 connections to pin 10 close the feedback loop around A_4.

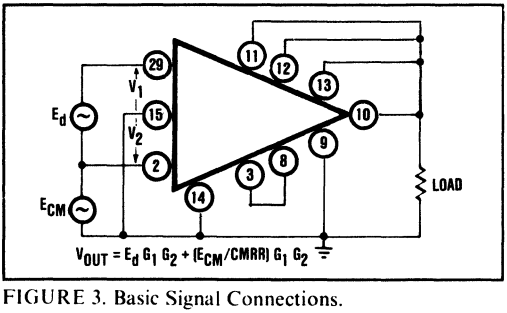


FIGURE 3. Basic Signal Connections.

In the equation shown in Figure 3, G_1 is the input stage gain and G_2 is the output stage gain. CMRR is the common-mode rejection ratio [CMR (in dB) = 20 log CMRR (in V/V)]. Common-mode voltage shown as E_{CM} is actually the average of the two voltages appearing at the two inputs (pins 29 and 2) with respect to pin 15 (V_1 and V_2).

GAIN SETTING

Gain is determined by a 4-bit digital word applied to the input D_0 through D_3 (see Figure 1). Pin 19 provides a latch function for the inputs. When pin 19 is a logic 0, changes on the D_0 through D_3 inputs are inhibited. Pin 19 should be at +5V if the latch is not used.

A gain state truth table is shown in Table I. Gains are determined by the resistor networks shown in Figure 1. For the state D_3, D_2 = 0, 0, the input stage gain is a function of the gain setting resistor R_G connected between pins 26 and 27. If gains of 1, 2 and 4 are desired, no connection should be made to pins 26 and 27 and the resistance across these pins should be kept high with respect to 40kΩ (> 400MΩ).

Gain accuracy is established by laser-trimming the thin-film resistor networks during assembly. No external, user trimming is required.

OUTPUT OFFSET

Output offset may be varied by either of two methods shown in Figure 4. Sources at pin 9 and pin 14 apply voltages to the noninverting inputs of A_4 and A_3 respectively (see Figure 1). Since the output stage gain occurs after these points, the output voltage bias established with V_{R1} and V_{R2} will vary with the output gain, G_2. Sources connected at pins 9 and 14 must have resistances low with respect to 10kΩ in order not to disturb gain accuracy and common-mode rejection.

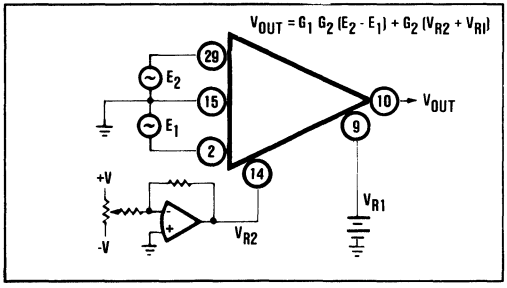


FIGURE 4. Output Offsetting.

LOW-PASS FILTER

For low frequency signals, system performance may be improved by reducing noise bandwidth in the amplifier. This may be accomplished with the addition of one or two external capacitors as shown in Figure 5. C_2 is connected to a 10k/10k attenuator and C_1 is connected as a feedback element across A4 (see Figures 1 and 5). The transfer function is:

$$\frac{V_O}{V_{IN}} = \left[\frac{10 \times 10^3}{100 \times 10^6\, S(C_2 + 330 \times 10^{-12}) + 20 \times 10^3}\right]\left[1 + \frac{10 \times 10}{10 \times 10^3\, R_1 SC_1 + R_1}\right]$$

TABLE I. Gain State Truth Table.

Digital Inputs (G_1) D_3	D_2	(G_2) D_1	D_0	G_1 (A_1 and A_2) (Pins 2 & 29 to 3)	G_2 (A_{IN}) (Pin 8 to Pin 10)	$G_1 \cdot G_2$ (R_G* = ∞)	$G_1 \cdot G_2$ (R_G* ≠ ∞)
0	0	0	0	1 + 40k/R_G	1	1	1(1 + 40k/R_G)
0	0	0	1		2	2	2(1 + 40k/R_G)
0	0	1	0		4	4	4(1 + 40k/R_G)
0	0	1	1		4	4	4(1 + 40k/R_G)
0	1	0	0	4	1	4	4
0	1	0	1		2	8	8
0	1	1	0		4	16	16
0	1	1	1		4	16	16
1	0	0	0	32	1	32	32
1	0	0	1		2	64	64
1	0	1	0		4	128	128
1	0	1	1		4	128	128
1	1	0	0	256	1	256	256
1	1	0	1		2	512	512
1	1	1	0		4	1024	1024
1	1	1	1		4	1024	1024

*R_G connected between pins 26 and 27

The first term is a first order filter. The second term is more complex. R_1 varies with the output stage gain - 1.4k for $G_2 = 4$ (see Figure 1). The "1 + ..." nature of the transfer function prevents a true first order filter rolloff.

For most applications, the first order low-pass filter obtained by C_2 provides sufficient filtering. The value C_2 required for a desired cutoff frequency (f_2 in Hz) is obtained by the equation shown in Figure 5.

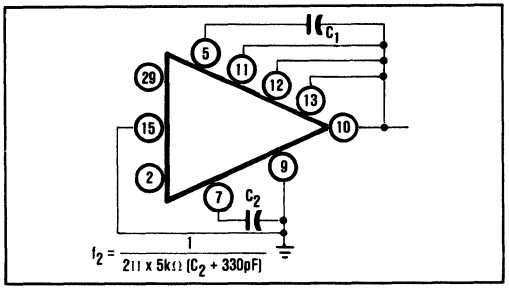


FIGURE 5. Low-Pass Filter Connections.

LARGER OUTPUT CURRENT

The output current rating of the 3606 is a minimum of ±5mA. The linearity of the gain is affected by output current. See Typical Performance Curves. Optimum linearity is achieved with $I_O \leq 1mA$. $I_O \leq 5mA$ is acceptable. Above 5mA it may be desirable to use a power or current booster as shown in Figure 6. Burr-Brown's 3329 will provide ±100mA output while Burr-Brown's 3553 will supply ±200mA. When either booster is placed inside the feedback loop as shown, the booster's offset voltage produces no significant errors since it is divided by the open-loop gain of the output stage.

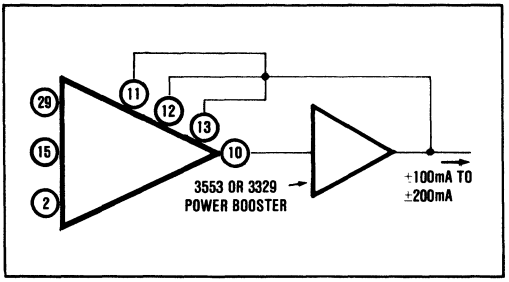


FIGURE 6. Output Current Booster.

GUARD DRIVE CONNECTIONS

Use of the guard drive connection shown in Figure 7 can improve system common-mode rejection when the distributed capacitance of the input lines is significant. The common-mode voltage which appears on the input lines and on pins 29 and 2 is computed by the 3606 [(V_1 + V_2) 2] and appears at pin 28. It is then fed back to the shield so that the voltage across the distributed capacitances is minimized. This reduces the common-mode current and improves common-mode rejection. The operational amplifier in the voltage follower configuration is used to supply more current than can be obtained from the 20k resistors connected internally to pin 28 (see Figure 1).

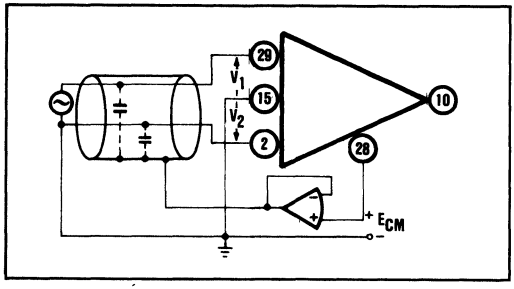


FIGURE 7. Guard Drive Connections.

OFFSET TRIM

Offset voltages of the 3606 are reduced by laser-trimming during assembly. This reduces the initial offset voltage and the offset voltage change with gain change to levels that are acceptable for most applications. For more critical applications the offset voltages can be externally

nulled to zero. The following steps should be followed (see Figure 8).

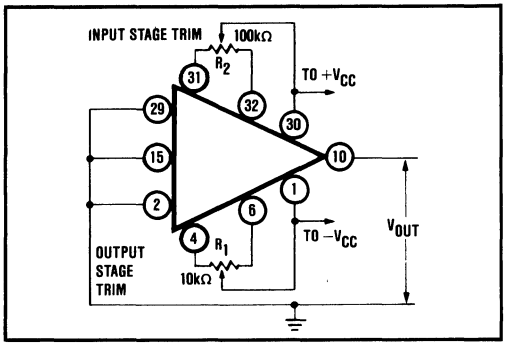


FIGURE 8 Optional Offset Trim.

1. Adjust both R_1 and R_2 to mid-range.
2. Set the gain to minimum (1V V)
3. Adjust R_1 to make V_{OUT} equal zero.
4. Set the gain to maximum (1024V V)
5. Adjust R_2 to make V_{OUT} equal zero.

By using this technique, the change in output offset voltage caused by a gain change of 1V V to 1024V V may be reduced to, typically 1mV instead of 10mV with no external trimming. Trimming may cause the offset voltage drift vs temperature to increase slightly.

APPLICATIONS

A typical application of 3606 in a microcomputer based data acquisition system is shown in the block diagram below.

The purpose of this system is to be able to acquire data from a specific analog input channel, suitably condition it (amplify it and convert it to digital form) and store it or transmit it for further processing.

Initially the Microcomputer loads the RAM (random access memory) with the required coding for various desired gains via Data Bus. The coding associates the gain state truth table for 3606 with corresponding address locations in the computer memory. So when the computer puts out an instruction to multiplex a specific analog input channel through the multiplexer via the Address Bus, the RAM also receives the same address information and puts out corresponding gain code to the PGIA 3606. The 3606 amplifies the multiplexed signal by the programmed gain value, and outputs it to S/H (sample and hold). The S/H holds the output value when it receives the control signal from the computer and the A/D converts it and outputs it to the computer via the Data Bus under computer control.

The PGIA 3606 allows the system user to modify and reprogram gain values for different analog input channels merely by changing the software computer program. Since different dedicated instruments are not required for various input channels, the PGIA also saves space and overall system costs.

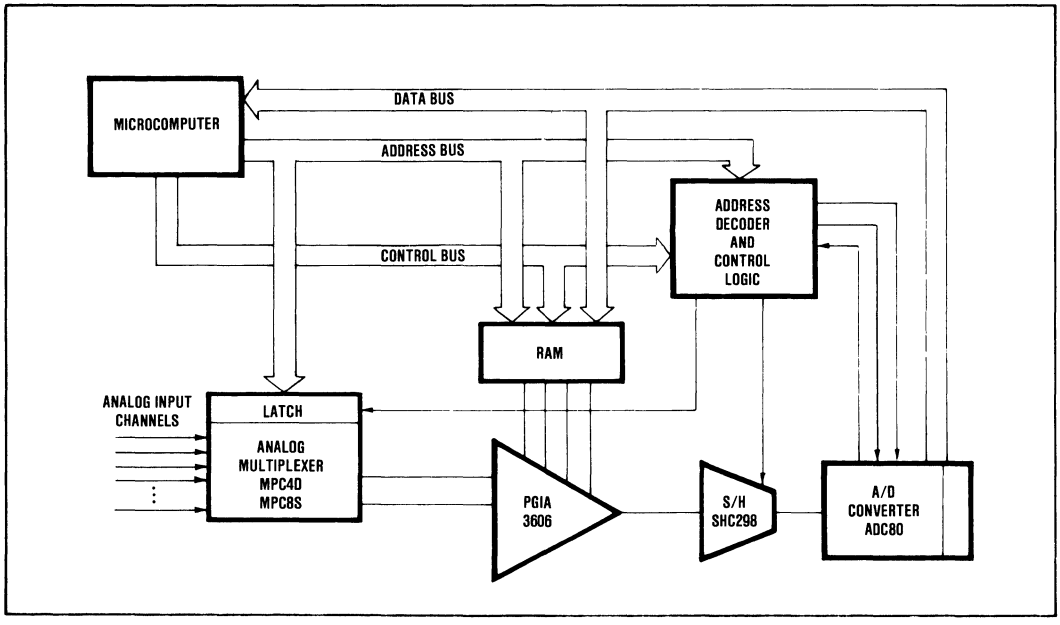


FIGURE 9. Use of 3606 in Data Acquisition System.

BURR-BROWN®

3627

High Accuracy Unity-Gain DIFFERENTIAL AMPLIFIER

FEATURES

- LOW COST
- EASY TO USE
- COMPLETELY SELF-CONTAINED
- HIGH ACCURACY
  - Gain Error, 0.005%
  - Nonlinearity, 0.0005%
  - CMR, 106dB
- NO TRIMMING REQUIRED

DESCRIPTION

The 3627 is a high accuracy committed-gain differential amplifier. It consists of a high quality monolithic operation amplifier, a low drift thin-film resistor network and laser-trimmed offset circuitry - all inside a single integrated circuit package.

The fact that the 3627 is completely self-contained in a TO-99 package has several user benefits:

The total performance is guaranteed as a single component.

No gain adjustments are required.

No offset trimming is required.

The whole circuit, including the gain setting resistors and offset trim circuitry, is protected by the environmentally rugged hermetically sealed package.

The total amplifier function is very small in size (0.108 square inches of area and 0.025 cubic inches of volume).

The 3627 is offered in two grades; the 3627AM and the 3627BM. They differ only in common-mode rejection (94dB typ. vs 106dB typ.) and offset voltage drift (15μV/°C typ. vs 10μV/°C typ.)

The 3627 offers excellent total performance with no fuss and a very-low total installed cost.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-364A

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and ±15VDC power supply unless otherwise noted.

MODELS	3627AM	3627BM
GAIN		
Gain Equation	G = 1V/V(1)	
Gain Error	±0.01%, max (±0.005% typ)	
Gain Nonlinearity(2)	±0.001%, max (±0.0005% typ)	
Gain Temp. Coefficient, max	±0.0005%/°C (5ppm/°C)	
Gain Temp Coefficient, typ	±0.0002%/°C (2ppm/°C)	
OUTPUT		
Rated Output, min	±10V at ±5mA	
Rated Output, typ	±12V at ±10mA	
Output Impedance	0.01Ω	
INPUT		
Input Impedance		
Differential	50kΩ	
Common-mode	50kΩ	
Input Voltage Range		
Differential	±20V	
Common-mode	±20V	
Common-mode Rejection, DC to 60Hz		
CMR, at 25°C	90dB, min (94dB, typ)	100dB, min (106dB, typ)
CMR, -25°C to +85°C	80dB, min (90dB, typ)	86dB, min (94dB, typ)
OFFSET AND NOISE		
Offset Voltage, RTO(4)(5)		
at 25°C	250µV, max (100µV, typ)	
vs Temperature, µV/°C	30, max (15, typ)	20, max (10, typ)
vs Supply	20µV/V	
vs Time	20µV/mo	
Noise Voltage, RTO(4)(6)		
0.01Hz to 10Hz	2µV, p-p	
10Hz to 100Hz	1.5µV, rms	
DYNAMIC RESPONSE		
Small Signal, ±1% Flatness	5kHz min (8kHz, typ)	
Small Signal, ±3dB Flatness	0.8MHz min (1.2MHz, typ)	
Full Power Bandwidth	14kHz min (18kHz, typ)	
Slew Rate	0.6V/µsec min (1V/µsec, typ)	
Settling Time, 0.1% (±10mV)	20µsec	
Settling Time, 0.01% (±1mV)	50µsec	
POWER SUPPLY		
Rated Voltage	±15VDC	
Voltage Range	±5VDC to ±18VDC	
Quiescent Supply Current	±2mA	
TEMPERATURE RANGE		
Specifications, min	-25°C to +85°C	
Operation	-55°C to +125°C	
Storage	-65°C to +150°C	

NOTES.

1 Connected as unity-gain amplifier. Several other configurations are possible. See the figures in Discussion and Typical Applications.
2 Nonlinearity is the maximum peak deviation from the best straightline as a percent of full scale peak-to-peak output.
3 With zero source impedance unbalance.
4 Referred to output in unity-gain difference configuration. Note that this circuit has a gain of 2 for the operational amplifiers offset voltage and noise voltage.
5 Includes effects of amplifiers' input bias currents.
6 Includes effects of amplifiers' input current noise.

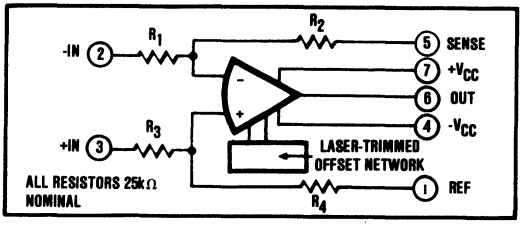
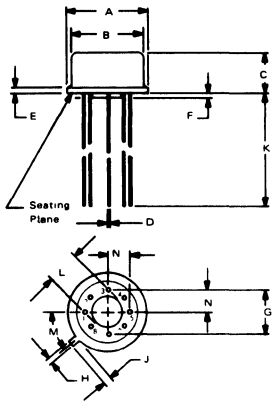


FIGURE 1. Simplified Circuit Diagram.

MECHANICAL
TO-99

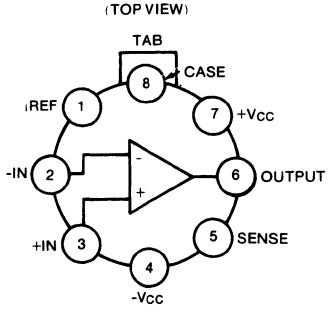


NOTE
Leads in true position within .010 (.25mm) R @ MMC at seating plane

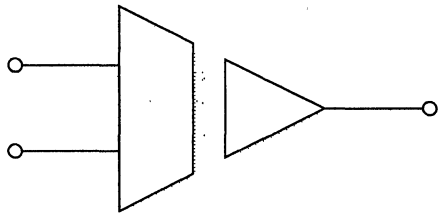
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	-	12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Pin material and plating compostion conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

CONNECTION DIAGRAM



See Figure 1 for circuit diagram



ISOLATION PRODUCTS

4

WHAT IS AN ISOLATION AMPLIFIER?

An isolation amplifier is a device with the primary function of providing ohmic isolation (break the ohmic continuity of electrical signal) between the input signal/circuitry and the output of the amplifier. It usually consists of an input operational amplifier or instrumentation amplifier followed by a unity-gain isolation stage. The sole purpose of the unity-gain isolation stage is to completely isolate the input from the output of the device. Ideally, the ohmic continuity of the input signal is broken (at the isolation barrier) yet accurate signal transfer without any attenuation is achieved across the unity-gain isolation stage. An important feature of an isolation amplifier is that it has a completely floating input which helps eliminate cumbersome connections to source ground.

Figures 1 and 2 show typical isolation amplifier applications. The isolation-mode voltage V_{ISO} is the voltage that exists across the isolation barrier. The contribution of the output referred error caused by V_{ISO} is (V_{ISO}/IMRR) x Gain where IMRR is the Isolation Mode Rejection Ratio. V_{SIG} is the differential input signal and V_{CM} is the common-mode voltage. Leakage Current is the current that flows across the isolation barrier with some specified isolation voltage applied between the input and the output.

CHARACTERISTICS OF ISOLATION AMPLIFIERS

Following is a discussion of some characteristics and terms unique to isolation amplifiers.

COMMON-MODE VOLTAGE AND ISOLATION VOLTAGE

Some manufacturers (other than Burr-Brown) treat common-mode voltage and isolation voltages synonymously in describing the use and /or specifications of isolation amplifiers. It is important to understand the significance of these terms and the difference between them.

When the input common is grounded, the differential input signal V_D (see Figure 1) can be floated by the amount V_{CM} above the input ground. V_{CM} is the common-mode voltage (CMV) and is generally ±10V, limited by the CMV rating of the input stage amplifier. In applications involving higher systems common-mode voltages, input common terminal is not grounded and the common-mode voltages are referenced across the isolation barrier to the output common terminal.

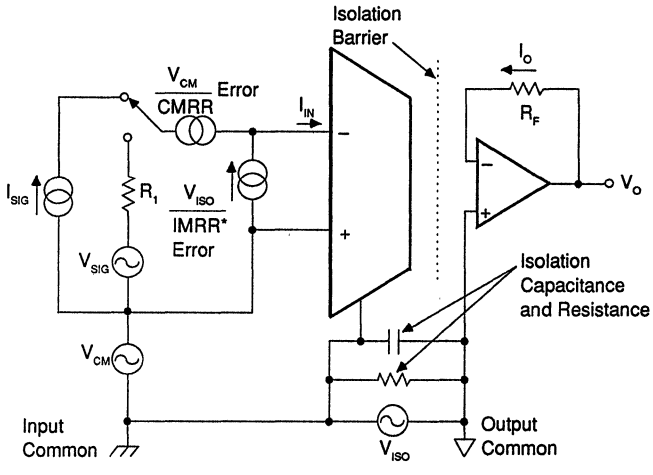


Figure 1. Typical Isolation Amplifier, Current (Input) Mode.

The isolation voltage V_{ISO} shown in Figure 1 is the potential difference between the input common and the output common terminals. The isolation voltage rating describes the amount of voltage that the isolation barrier can withstand without breakdown. This feature of the isolation amplifier allows two distinct ground connections to be made when necessary. It allows the isolation amplifier to be used in applications involving very-high common-mode voltages and in applications of breaking ground loops.

Many applications involve a large "system common-mode voltage." In such applications, the isolation amplifier's input common terminal is not connected to any ground but the output common terminal is connected to the system ground. In such a case, the term V_{CM} shown in Figures 1 and 2 becomes negligible and V_{ISO} determines the safe limit for the system common-mode voltage. In this manner, the isolation amplifier can accommodate common-mode voltages of 2000V or more.

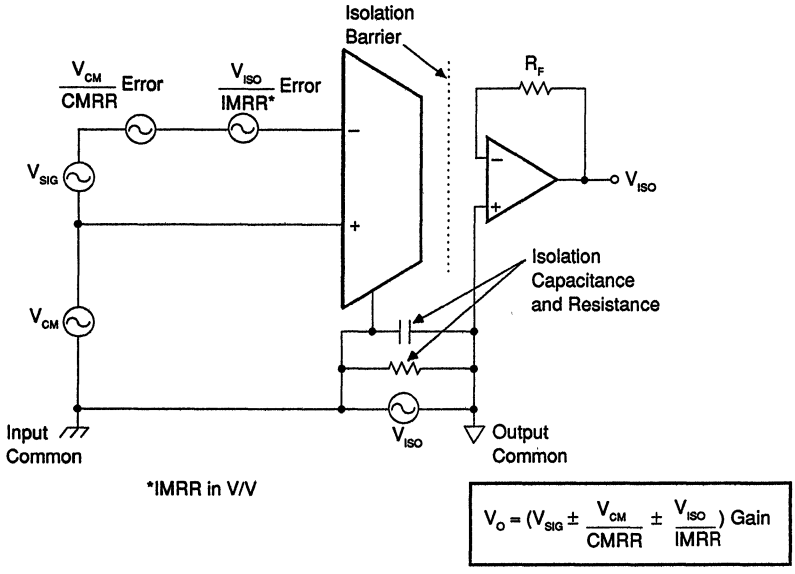


Figure 2. Typical Isolation Amplifier, Voltage (Input) Mode.

COMMON-MODE REJECTION AND ISOLATION REJECTION

Isolation-mode rejection (IMR) is another term that some other manufacturers refer to as common-mode rejection (CMR). The preceding discussion on the common-mode voltage and isolation voltage helps recognize the difference between CMR and the IMR. The CMR is the measure of the input stage amplifier's ability to reject common-mode input signals (common-mode with reference to the output common) while transmitting the differential signal across the isolation barrier. The isolation-mode rejection ratio (IMRR) is defined by the equations shown in Figures 1 and 2. Thus, understanding the IMR capability of isolation amplifiers allows their meaningful use in applications requiring very high common-mode rejection ratios such as 100dB to 140dB.

ISOLATION VOLTAGE RATINGS, TEST VOLTAGE

It is important to understand the significance of the continuous derated isolation voltage specification and its relationship to the actual test voltage applied to the unit. Since a "continuous" test is impractical in a product manufacturing situation (implies infinite test duration) it is generally accepted practice to perform a production test at a higher voltage (higher than the continuous rating) for some shorter length of time.

The important consideration is then "what is the relationship between actual test conditions and the continuous derated minimum specification?" There are several rules of thumb used throughout the industry to establish this relationship. For most isolation amplifiers, Burr-Brown has chosen a very

conservative one: $V_{TEST} = (2 \times V_{CONTINOUS\ RATING}) + 1000V$. This relationship is appropriate for conditions where the system transient voltages are not well defined.* Where the real voltages are well defined or where the isolation voltage is not continuous the user may chose to use a less conservative derating to establish a specification from the test voltage.

Beginning with the introduction of the ISO120 and ISO121, new introductions are being tested for partial discharge. To accommodate poorly defined transients, the part under test is exposed to a voltage 1.6 times the continuous rated voltage and must display a partial discharge level of ≤5pC in a 100% production test. This method is described in detail in the ISO120 data sheet.

APPLICATIONS OF ISOLATION AMPLIFIERS

When one or more of the following conditions/requirements are present in an application, an isolation amplifier would generally be the right choice as a signal conditioning device:

- When ohmic isolation between the signal source and the output is a requirement (isolation impedance between the input and the output is >10MΩ).
- When common-mode noise and voltage rejection requirements are >100dB).
- When is is necessary to process signals in the presence of, or riding on, high common-mode voltages (CMV >> 10V).

In general, most applications can be broadly categorized into the following four types:

- Amplifying and measuring low level signals in the presence of high common-mode voltages.
- Breaking ground loops and/or eliminating source ground connections. The isolation amplifier provides full floating input, eliminating the need for connections to source ground, and thus allows two-wire hook-up to the signal sources.
- Providing an interface between medical patient monitoring equipment and the transducer/devices that may be in physical contact with the patients. Such applications require high isolation voltage levels and very-low leakage currents.
- Providing isolation protection to electronic instruments/equipment. Large common-mode voltages occasionally cause hazardous electronic faults. Low leakage currents and high isolation voltage capability of isolation amplifiers help protect instruments against damage caused by such faults.

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*Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS 1-109 and ICS 1-111.

Isolation amplifier performance requirements vary significantly, depending on the type of requirement. In applications where bandwidth and speed of response are more important than gain accuracy and linearity, the optically or capacitatively coupled amplifiers will be the best choice. For applications where gain accuracy and linearity are key parameters, Burr-Brown's family of transformer or capacitatively coupled amplifiers are the suitable choice.

ISOLATION AMPLIFIERS SELECTION GUIDES

The following Selection Guides show parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

TRANSFORMER-COUPLED AMPLIFIERS

Descrip	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test, Peak	Isolation Mode Rejection, typ DC (dB)	Isolation Mode Rejection, typ 60Hz (dB)	Leakage Current at Test Voltage (μA)	Iso Impedance (Ω)	Iso Impedance (pF)	Gain Nonlinearity max (%)	Gain Nonlinearity typ (%)	Voltage Drift max	Bias Current (±μV/°C) max	±3dB Freq (kHz)	Ext Iso Power Req	Temp[1]	Pg
High Isolation Voltage	3656G	±3500	±8000	160	125	0.5	10^{12}	6	±0.05	±0.03	5+ (1000/G_1)	100nA	30	No	Ind	4-108

NOTES: All packages are DIPs. (1) Ind = –25°C to +85°C.

OPTICALLY COUPLED AMPLIFIERS

Descrip	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test, Peak	Isolation Mode Rejection, typ DC (dB)	Isolation Mode Rejection, typ 60Hz (dB)	Leakage Current at Test Voltage (μA)	Iso Impedance (Ω)	Iso Impedance (pF)	Gain Nonlinearity max (%)	Gain Nonlinearity typ (%)	Voltage Drift (±μV/°C) max	Bias Current max	±3dB Freq (kHz)	Ext Iso Power Req	Temp[1]	Pg
Balanced Current Input	3650G	±2000	±5000	140	120	0.25[2]	10^{12}	1.8	±0.05	±0.02	5	10nA	15	Yes[3]	Ind	4-100
Balanced FET Input	3652G	±2000	±5000	140	120	0.25[2]	10^{12}	1.8	±0.1	±0.05	25	50nA	15	Yes	Ind	4-100
Low Drift Wide BW	ISO100P	750	2500	146[3]	108[3]	0.3	10^{12}	2.5	0.07	0.02	4[3]	10nA	60	Yes	Ind	4-8

NOTES: All packages are DIPs. (1) Ind = –25°C to +85°C. (2) At 240V/60Hz. (3) R_{IN} = 10k, Gain = 100.

CAPACITOR COUPLED, HERMETICALLY SEALED AMPLIFIERS

Boldface = NEW

Descrip	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test, Peak	Isolation Mode Rejection, typ DC (dB)	Isolation Mode Rejection, typ 60Hz (dB)	Leakage Current at Test Voltage (μA)	Iso Impedance (Ω)	Iso Impedance (pF)	Gain Nonlinearity max (%)	Gain Nonlinearity typ (%)	Voltage Drift (±μV/°C) max	Bias Current max	±3dB Freq (kHz)	Ext Isol Power Req	Temp[1]	Pg
1500VAC Isolation	**ISO102B**	±2121	±4000	160	120	1.0	10^{14}	6	±0.025	±0.02	±250	100μA	70	Yes	Ind	4-20
	ISO120B	±2121	±3535[2]	160	115	0.5	10^{14}	2	±0.01	±0.005	±150	50μA	60	Yes	Ind	4-44
	ISO122	±2121	±3394		140	0.5	10^{14}	2	±0.01	±0.005	±200	50μA	50	Yes	Com	4-57
3500VAC Isolation	**ISO106B**	±4950	±8000	160	130	1.0	10^{14}	6	±0.012	±0.007	±250	100μA	70	Yes	Ind	4-20
	ISO121B	±4950	±5600[2]	160	115	0.5	10^{14}	2	±0.01	±0.005	±150	50μA	60	Yes	Ind	4-44

NOTES: All packages are DIPs. (1) Ind = –25°C to +85°C. Com = 0°C to +70°C. (2) Partial discharge voltage.

ISOLATION POWER SUPPLIES[1]

Boldface = NEW

Descrip	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test Peak	Input Voltage (VDC) min	Input Voltage (VDC) max	Leakage Current 240VAC 60Hz (μA)	Isolation Impedance (Ω)	Isolation Impedance (pF)	Current, Balanced Loads On All Outputs (mA) Rated	Current, Balanced Loads On All Outputs (mA) Max[1]	Sensitivity To Input Change (V/V)	Temp[2]	Pkg	Pg
Single ±15V Output	700	1500	4200	10	18	1	10^{10}	5	±3-30	±60	1.08	Ind	Mod	4-86
	700U	2000	5000	10	18	1	10^{10}	3	±3-30	±60	1.08	Ind	Mod	4-86
	PWS725	**2121**	**4000**	**7**	**18**	**1.2**	10^{12}	**9**	±15	±40	**1.15**	**Ind**	**DIP**	**4-65**
	PWS726	**4950**	**8000**	**7**	**18**	**1.2**	10^{12}	**9**	±15	±40	**1.15**	**Ind**	**DIP**	**4-65**
Dual ±15V Output	722	4950	8000	5	16	1	10^{10}	6	±3-40	±50	1.13	Ind	Mod	4-92
	PWS727	**2121**	**3394**	**10**	**18**	**1.5**	10^{14}	**8**	±15	±30	**1.15**	**Com**	**Mod**	**4-70**
	PWS728	**2121**	**3394**	**4.5**	**5.5**	**1.5**	10^{14}	**8**	±15	±30	**3.2**	**Com**	**Mod**	**4-73**
Quad ±15V Output	710	1000	3100	10	18	1	10^{10}	8	±9.5	±60	1.08	Ind	Mod	4-88
Quad ±8V Output	724	1000	3000	5	16	1	10^{10}	6	±3-16	±60	0.63	Ind	Mod	4-96
Multiple Output (1-8)	**PWS740**	**2121**	**4000**	**7**	**20**	**1.5**	10^{12}	**3**	**30[3]**	**60[3]**	**1.20**	Ind	**Sys[4]**	**4-76**
	PWS750	**2121**	**3394**	**4.5[5]**	**18[6]**	**1.5**	10^{14}	**8**	±15	**30**	**(7)**	**Com**	**Comp**	**4-83**

NOTES: (1) See complete Product Data Sheet for full specifications, especially regarding output current capabilities. (2) Ind = –25°C to +85°C. Com = 0°C to +70°C. (3) Per channel. (4) 1 TO-3 driver per 8 channels, plus 2 DIPs per channel. (5) 5V operation. (6) 15V operation. (7) 5V operation: 3.2; 15V operation: 1.15.

CAPACITOR-COUPLED, WITH POWER

Boldface = NEW

Descrip	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test, Peak	Isolation Mode Rejection, typ DC (dB)	Isolation Mode Rejection, typ 60Hz (dB)	Leakage Current at Test Voltage (μA)	Iso Impedance (Ω)	Iso Impedance (pF)	Gain Nonlinearity max (%)	Gain Nonlinearity typ (%)	Voltage Drift (±μV/°C) max	Bias Current max	±3dB Freq (kHz)	Temp[1]	Pg
1500VAC Input Power	**ISO103**	**2121**	**3394**	**160**	**100**	**1.0**	10^{12}	**9**		**0.01**	**100[2]**	**50μA**	**30**	**Ind**	**4-34**
1500VAC Output Power	**ISO113**	**2121**	**3394**	**160**	**100**	**1.0**	10^{12}	**9**		**0.01**	**100[2]**	**50μA**	**30**	**Ind**	**4-41**
2500VAC Input Power	**ISO107**	**3535**	**5656**	**160**	**100**	**1.0**	10^{12}	**9**		**0.01**	**100[2]**	**50μA**	**30**	**Ind**	**4-34**

NOTES: All packages are DIPs. (1) Ind = –25°C to +85°C.

CAPACITATIVELY COUPLED VOLTAGE-TO-FREQUENCY CONVERTER

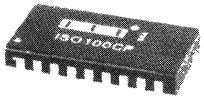
Boldface = NEW

Descrip	Model	Isolation Voltage (V) Cont Peak	Isolation Voltage (V) Pulse/ Test Peak	Leakage Current at Test Voltage (μA)	Isolation Impedance (Ω)	Isolation Impedance (pF)	Non-linearity at 1MHZ (typ)	Bias Current (max) (μA)	Operating Frequ (max) (kHz)	External Isolation Power Req	Temp[1]	Pg
1500V Isolation	**ISO108**	**2121**	**3394[2]**	**0.3 typ**	10^{12}	**3**	**0.01**	**250**	**4**	**Yes**	**Ind**	**4-38**

NOTES: Package is DIP. (1) Ind = –25°C to +85°C. (2) Partial discharge voltage.

BURR-BROWN®

ISO100



Miniature
Low Drift - Wide Bandwidth
ISOLATION AMPLIFIER

FEATURES

- EASY TO USE, SIMILAR TO AN OP AMP
  $V_{OUT}/I_{IN} = R_F$, Current Input
  $V_{OUT}/V_{IN} = R_F/R_{IN}$, Voltage Input
- 100% TESTED FOR BREAKDOWN
  750V Continuous Isolation Voltage
- ULTRA-LOW LEAKAGE, 0.3μA, max, at 240V/60Hz
- WIDE BANDWIDTH, 60kHz
- LOW COST
- 18-PIN DIP PACKAGE

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer sensing
  (thermocouple, RTD, pressure bridges)
  4mA to 20mA loops
  Motor and SCR control
  Ground loop elimination
- BIOMEDICAL MEASUREMENTS
- TEST EQUIPMENT
- DATA ACQUISITION

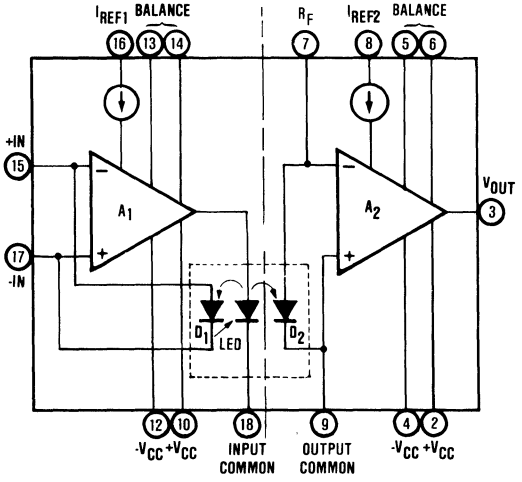
DESCRIPTION

The ISO100 is a miniature low cost optically-coupled isolation amplifier. High accuracy, linearity, and time-temperature stability are achieved by coupling light from an LED back to the input (negative feedback) as well as forward to the output. Optical components are carefully matched and the amplifier is actively laser-trimmed to assure excellent tracking and low offset errors.

The circuit acts as a current-to-voltage converter with a minimum of 750V (2500V test) between input and output terminals. It also effectively breaks the galvanic connection between input and output commons as indicated by the ultra-low 60Hz leakage current of 0.3μA at 250V. Voltage input operation is easily achieved by using one external resistor.

Versatility along with outstanding DC and AC performance provide excellent solutions to a variety of challenging isolation problems. For example, the ISO100 is capable of operating in many modes, including: noninverting (unipolar and bipolar) and inverting (unipolar and bipolar) configurations. Two precision current sources are provided to accomplish bipolar operation. Since these are not required for unipolar operation, they are available for external use (see Applications section).

Designs using the ISO100 are easily accomplished with relatively few external components. Since V_{OUT} of the ISO100 is simply $I_{IN}R_{OUT}$, gains can be changed by altering one resistor value. In addition, the ISO100 has sufficient bandwidth (DC to 60kHz) to amplify most industrial and test equipment signals.



International Airport Industrial Park - P O Box 11400 - Tucson, Arizona 85734 - Tel (602) 746-1111 - Twx 910-952-1111 - Cable BBRCORP - Telex 66-6491

PDS-456E

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±V_{CC} = 15VDC unless otherwise noted

PARAMETER	CONDITIONS	ISO100AP			ISO100BP			ISO100CP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ISOLATION											
Voltage,											
Rated Continuous, AC peak or DC[1]		750			•			•			V
Test Breakdown, DC	10sec	2500			•			•			V
Rejection[2] DC			5			•			•		pA/V
	R_{IN} =10kΩ, Gain = 100		146			•			•		dB
AC	60Hz, 480V, R_F = 1MΩ		400			•			•		pA/V
	R_{IN} = 10kΩ, Gain = 100		108			•			•		dB
Impedance			10^{12} || 2 5			•			•		Ω || pF
Leakage Current	240V, rms, 60Hz			0 3			•			•	μA, rms
OFFSET VOLTAGE (RTI)											
Input Stage (V_{OSI})											
Initial Offset				500			300			200	μV
vs Temperature				5			2			2	μV/°C
vs Input Power Supplies				105			•			•	dB
vs Time			1			•			•		μV/kHr
Output Stage (V_{OSO})											
Initial Offset				500			300			200	μV
vs Temperature				5			2			2	μV/°C
vs Output Power Supplies				105			•			•	dB
vs Time			1			•			•		μV/kHr
Common-Mode Rejection Ratio[2]	60Hz, R_F = 1MΩ		3			•			•		nA/V
	R_{IN} = 10kΩ, Gain = 100		90			•			•		dB
Common-Mode Range		±10			•			•			V
REFERENCE CURRENT SOURCES											
Magnitude											
Nominal		10 5	12	12 5	•	•	•	•	•	•	μA
vs Temperature				300			300			150	ppm/°C
vs Power Supplies			0 3	3		•	•		•	•	nA/V
Matching											
Nominal			50			•			•		nA
vs Temperature			150			•			•		ppm/°C
vs Power Supplies			0 3			•			•		nA/V
Compliance Voltage		-10		+15	•		•	•		•	V
Output Resistance			2 x 10^9			•			•		Ω
FREQUENCY RESPONSE											
Small Signal Bandwidth	Gain = 1V/μA		60			•			•		kHz
Full Power Bandwidth	Gain = 1V/μA, V_O = ±10V		5			•			•		kHz
Slew Rate		0 22	0 31		•	•		•	•		V/μsec
Settling Time	0 1%		100			•			•		μsec
TEMPERATURE RANGE											
Specification		-25		+85	•		•	•		•	°C
Operating		-40		+100	•		•	•		•	°C
Storage		-55		+100	•		•	•		•	°C
UNIPOLAR OPERATION											
GENERAL PARAMETERS											
Input Current Range											
Linear Operation		-20		-0 02	•		•	•		•	μA
Without Damage		-1		+1	•		•	•		•	mA
Input Impedance			0 1			•			•		Ω
Output Voltage Swing	R_L = 2kΩ, R_F = 1MΩ	-10		0	•		•	•		•	V
Output Impedance	DC, open-loop		1200			•			•		Ω
GAIN	V_O = R_F (I_{IN})										
Initial Error (Adjustable To Zero)			2	5		1	2		1	2	% FS
vs Temperature			0 03	0 07		0 01	0 05		0 005	0 03	%/°C
vs Time			0 05			•			•		%/kHr
Nonlinearity[3]			0 1	0 4		0 03	0 1		0 02	0 07	%
CURRENT NOISE	I_{IN} = 0 2μA										
0 01Hz to 10Hz			20			•			•		pA, p-p
10Hz			1			•			•		pA/√Hz
100Hz			0 7			•			•		pA/√Hz
1kHz			0 65			•			•		pA/√Hz
INPUT OFFSET CURRENT (I_{OS})											
Initial Offset			1	10		•	•		•	•	nA
vs Temperature			0 05			•			•		nA/°C
vs Power Supplies			0 1			•			•		nA/V
vs Time			100			•			•		pA/kHr

ELECTRICAL (CONT)

PARAMETER	CONDITIONS	ISO100AP			ISO100BP			ISO100CP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES											
Input Stage											
Voltage (rated performance)			±15			•			•		V
Voltage (derated performance)		±7		±18	•		•	•		•	V
Supply Current	I_{IN} = -0 02µA		±1 1	±2		•	•		•	•	mA
	I_{IN} = -20µA		+8, -1 1	+13, -2		•	•		•	•	mA
Output Stage											
Voltage (rated performance)			±15			•			•		V
Voltage (derated performance)		±7		±18	•		•	•		•	V
Supply Current	V_O = 0		±1 1	±2		•	•		•	•	mA
Short Circuit Current Limit				±40			•			•	mA
BIPOLAR OPERATION											
GENERAL PARAMETERS											
Input Current Range											
Linear Operation		-10		+10	•		•	•		•	µA
Without Damage		-1		+1	•		•	•		•	mA
Input Impedance			0 1			•			•		Ω
Output Voltage Swing	R_L = 2kΩ, R_F = 1MΩ	-10		+10	•		•	•		•	V
Output Impedance			1200			•			•		Ω
GAIN	$V_O = R_F \cdot I_{IN}$										
Initial Error (Adjustable To Zero)			2	5		1	2		1	2	% of FS
vs Temperature			0 03	0 07		0 01	0.05		0 005	0 03	%/°C
vs Time			0 05			•			•		%/kHr
Nonlinearity (3)			0 1	0 4		0 03	0 1		0 02	0 07	%
CURRENT NOISE	I_{IN} = 0 2µA										
0 01Hz to 10Hz			1 5			•			•		nA, p-p
10Hz			17			•			•		pA/√Hz
100Hz			7			•			•		pA/√Hz
1kHz			6			•			•		pA/√Hz
INPUT OFFSET CURRENT (I_{OS}, bipolar) (4)											
Initial Offset			40	200		20	70		10	35	nA
vs Temperature				3			2			1	nA/°C
vs Power Supplies				0 7			•			•	nA/V
vs Time			250			•			•		pA/kHr
POWER SUPPLIES											
Input Stage											
Voltage (rated performance)			±15			•			•		V
Voltage (derated performance)		±7		±18	•		•	•		•	V
Supply Current	I_{IN} = +10µA		+2, -1 1	+3,-2		•	•		•	•	mA
	I_{IN} = -10µA		+8, -1 1	+13,-2		•	•		•	•	mA
Output Stage											
Voltage (rated performance)			±15			•			•		V
Voltage (derated performance)		±7		±18	•		•	•		•	V
Supply Current	V_O = 0		±1 1	±2		•	•		•	•	mA
Short Circuit Current Limit				±40			•			•	mA

Same as ISO100AP

NOTES

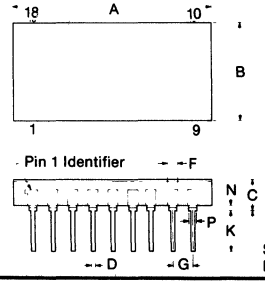
1 See Typical Performance Curves for temperature effects

2 See Theory of Operation section for definitions For dB see Ex 2, CM and HV errors

3 Nonlinearity is the peak deviation from a "best fit" straight line expressed as a percent of full scale output

4 Bipolar offset current includes effects of reference current mismatch and unipolar offset current

MECHANICAL



NOTE: Leads in true position within 0 01" (0.25mm) R at MMC at seating plane.

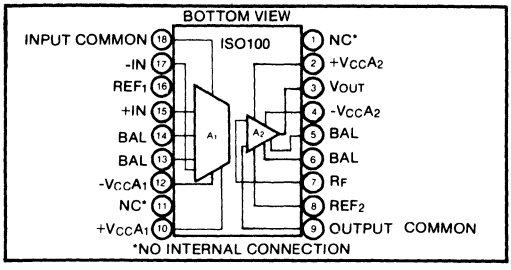
Pin numbers shown for reference only. Numbers are not marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.982	1.002	24.94	25.45
B	.480	.500	12.19	12.70
C	.148	.197	3.76	5.00
D	.016	.020	0.41	0.51
F	.050 TYP		1.27 TYP	
G	.095	105	2 41	2.67
J	.009	012	0.23	0.30
K	205 TYP		5.21 TYP	
L	.290	.310	7 37	7 87
N	.015	.035	0 38	0.89
P	040 TYP		1 02 TYP	

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±18V
Isolation Voltage	2500V
Input Current	±1mA
Storage Temperature Range	-55°C to +100°C
Lead Temperature soldering 10 seconds	+300°C
Output Short-circuit Duration	Continuous to ground

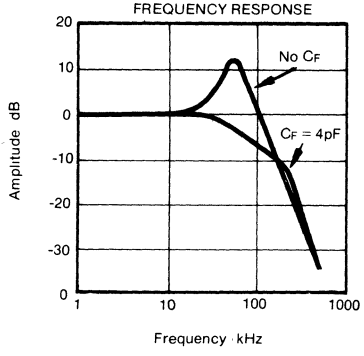
PIN CONFIGURATION



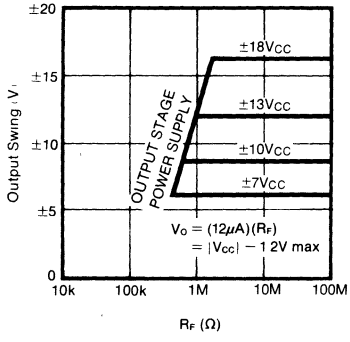
TYPICAL PERFORMANCE CURVES

T_A = +25°C, ±V_{CC} = 15VDC unless otherwise noted.

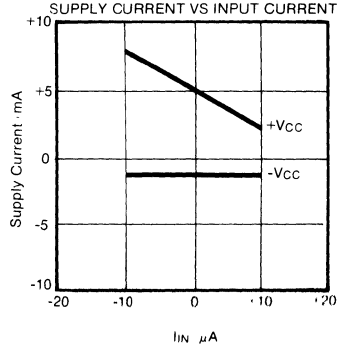
SMALL SIGNAL FREQUENCY RESPONSE



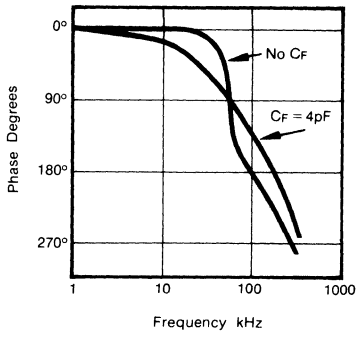
BIPOLAR OUTPUT SWING VS R_F



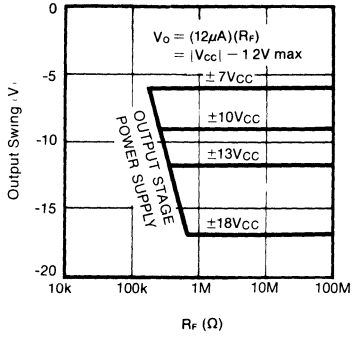
BIPOLAR INPUT STAGE SUPPLY CURRENT VS INPUT CURRENT



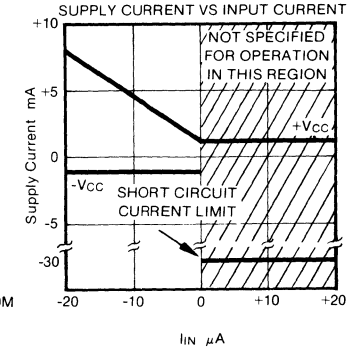
PHASE SHIFT VS FREQUENCY



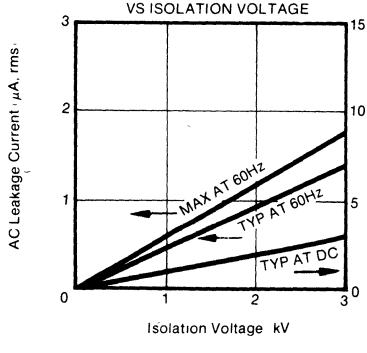
UNIPOLAR OUTPUT SWING VS R_F



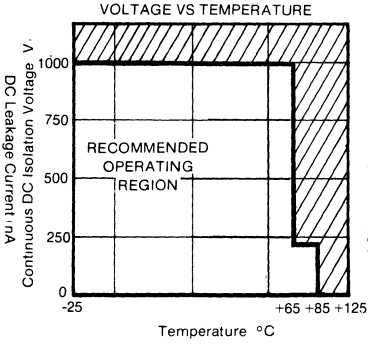
UNIPOLAR INPUT STAGE SUPPLY CURRENT VS INPUT CURRENT



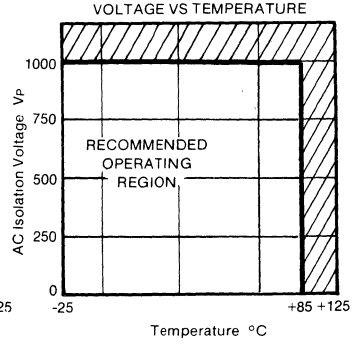
ISOLATION LEAKAGE CURRENT VS ISOLATION VOLTAGE

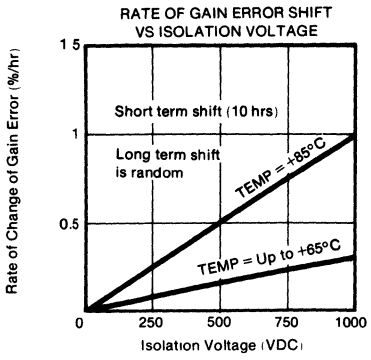


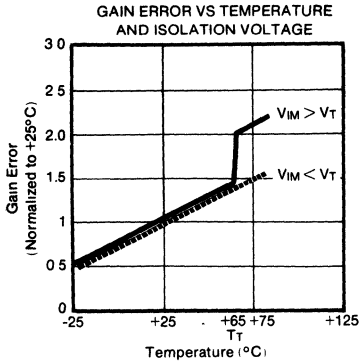
CONTINUOUS DC ISOLATION VOLTAGE VS TEMPERATURE



AC ISOLATION VOLTAGE VS TEMPERATURE







NOTES

V_T and T_T approximate the threshold for the indicated gain shift This is caused by the properties of the optical cavity

$T_T \approx +65°C$, $V_T \approx 200VDC$ Shift does not occur for AC voltages

V_{IM} = Isolation-mode Voltage
V_T = Threshold Voltage
T_T = Threshold Temperature

THEORY OF OPERATION

The ISO100 is fundamentally a unity gain current amplifier intended to transfer small signals between electrical circuits separated by high voltages or different references. In most applications an output voltage is obtained by passing the output current through the feedback resistor (R_F).

The ISO100 uses a single light emitting diode (LED) and a pair of photodiode detectors, coupled together, to isolate the output signal from the input.

Figure 1 shows a simplified diagram of the amplifier. I_{REF1} and I_{REF2} are required only for bipolar operation, to generate a midscale reference. The LED and photodiodes (D1 and D2) are arranged such that the same amount of light falls on each photodiode. Thus, the currents generated by the diodes match very closely. As a result, the transfer function depends upon optical match, rather than absolute performance. Laser-trimming of the components improves matching and enhances accuracy, while negative feedback improves linearity. Negative feedback around A1 occurs through the optical path formed by the LED and D1. The signal is transferred across the isolation barrier by the matched light path to D2.

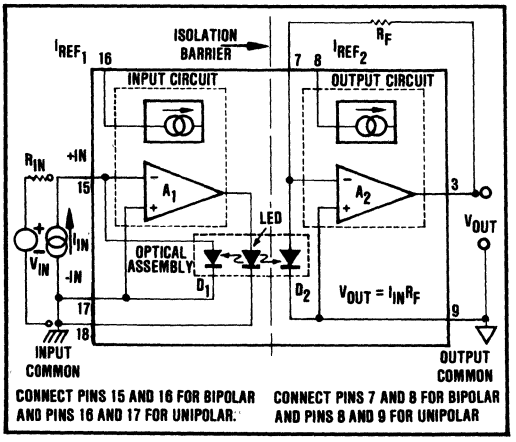


FIGURE 1. Simplified Block Diagram of the ISO100.

The overall ISO amplifier is noninverting (a positive going input produces a positive going output).

INSTALLATION AND OPERATING INSTRUCTIONS

UNIPOLAR OPERATION

In Figure 1, assume a current, I_{IN}, flows out of the ISO100 (I_{IN} must be negative in unipolar operation). This causes the voltage at pin 15 to decrease. Because the amplifier is inverting, the output of A1 increases, driving current through the LED. As the LED light output increases, D1 responds by generating an increasing current. The current increases until the sum of the currents in and out of the input node (-Input to A_1) is zero. At that point the negative feedback through D1 has stabilized the loop, and the current I_{D1} equals the input current plus the bias current. As a result no bias current flows in the source. Since D1 and D2 are matched ($I_{D1} = I_{D2}$), I_{IN} is replicated at the output via D2. Thus, A1 functions as a unity-gain current amplifier, and A2 is a current-to-voltage converter, as described below.

Current produced by D2 must either flow into A2 or R_F. Since A2 is designed for low bias current ($\approx$10nA) almost all of the current flows through R_F to the output. The output voltage then becomes;

$$V_O = (I_{D2})\,R_F = (I_{D1} \pm I_{OS})\,R_F \approx -(-I_{IN})\,R_F = I_{IN}R_F, \quad (1)$$

where, I_{OS} is the difference between A1 and A2 bias currents. For input voltage operation I_{IN} can be replaced by a voltage source (V_{IN}) and series resistor (R_{IN}) since the summing node of the op amp is essentially at ground. Thus, $I_{IN} = V_{IN}/R_{IN}$.

Unipolar operation does have some constraints, however. In this mode the input current must be negative so as to produce a positive output voltage from A1 to turn the LED on. A current more negative than 20nA is necessary to keep the LED turned on and the loop stabilized. When this condition is not met the output may be indeterminant. Many sensors generate unidirectional signals, e.g., photoconductive and photodiode devices, as well as some applications of thermocouples. However, other applications do require bipolar operation of the ISO100.

BIPOLAR OPERATION

To activate the bipolar mode, reference currents as shown in Figure 1, are attached to the input nodes of the op amps. The input stage stabilizes just as it did in unipolar operation. Assuming $I_{IN} = 0$, the photodiode has to supply all the I_{REF1} current. Again, due to symmetry, $I_{D1} = I_{D2}$. Since the two references are matched, the current generated by D2 will equal I_{REF2}. This results in no current flow in R_F, and the output voltage will be zero. When I_{IN} either adds or substracts current from the input node, the current D1 will adjust to satisfy $I_{D1} = I_{IN} + I_{REF1}$. Because I_{REF1} equals I_{REF2} and I_{D1} equals I_{D2}, a current equal to I_{IN} will flow in R_F. The output voltage is then $V_O = I_{IN}R_F$. The range of allowable I_{IN} is limited. Positive I_{IN} can be as large as I_{REF1} (10.5μA, min). At this point, D1 supplies no current and the loop opens. Negative I_{IN} can be as large as that generated by D1 with maximum LED output (recommended 10μA, max).

DC ERRORS

Errors in the ISO100 take the form of offset currents and voltages plus their drifts with temperature. These are shown in Figure 2.

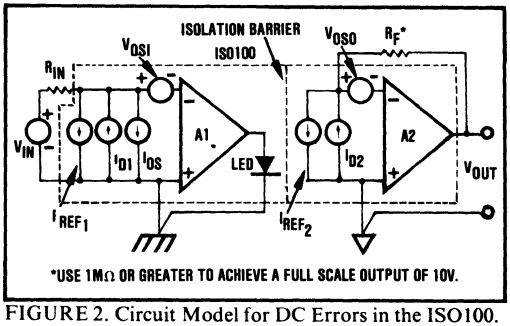


FIGURE 2. Circuit Model for DC Errors in the ISO100.

A1 and A2: are assumed to be ideal amplifiers.

V_{OSO} and V_{OSI}: are the input offset voltages of the output and input stage, respectively. V_{OSO} appears directly at the output, but, V_{OSI} appears at the output as

$$V_{OSI}\frac{R_F}{R_{IN}},$$

see equation (2).

I_{OS}: is the offset current. This is the current at the input necessary to make the output zero. It is equal to the combined effect of the difference between the bias currents of A1 and A2 and the matching errors in the optical components, in the unipolar mode.

I_{REF1} and I_{REF2}: are the reference currents that, when connected to the inputs, enable bipolar operation. The two currents are trimmed, in the bipolar mode, to minimize the $I_{OS\ bipolar}$ error.

I_{D1} and I_{D2}: are the currents generated by each photodiode in response to the light from the LED.

A_e: is the gain error.

$A_e = |$ Ideal gain/Actual gain$| - 1$

The output then becomes:

$$V_{OUT} = R_F[(\frac{V_{IN} \pm V_{OSI}}{R_{IN}} - I_{REF1} \pm I_{OS})(1 + A_e) + I_{REF2}] \pm V_{OSO} \quad (2)$$

The total input referred offset voltage of the ISO100 can be simplified in the unipolar case by assuming that $A_e = 0$ and $V_{IN} = 0$:

$$V_{OUT} \approx R_F\,[\frac{\pm V_{OSI}}{R_{IN}} \pm I_{OS\ unipolar}] \pm V_{OSO} \quad (3)$$

This voltage is then referred back to the input by dividing by R_F/R_{IN}.

$$V_{OS\ (RTI)} = (\pm V_{OSI}) \pm R_{IN}\,(I_{OS\ unipolar}) + V_{OSO}/(R_F/R_{IN}) \quad (4)$$

Example 1: (Refer to Figure 2 and Electrical Specifications Table)

Given: $I_{OS\ bipolar} = +35nA$
$R_{IN} = 100k\Omega$
$R_F = 1M\Omega$ (gain = 10)
$V_{OSI} = +200\mu V$
$V_{OSO} = +200\mu V$

Find: The total offset voltage error referred to the input and output when $V_{IN} = 0V$.

V_{OS} total RTI
$= \{[\pm V_{OSI} \pm R_{IN}\,(I_{OS\ bipolar}) - R_{IN}\,(I_{REF\ 1})]$
$[1 + A_e] + R_{IN}\,I_{REF\ 2}\} \pm V_{OSO}/(R_F/R_{IN})$
$= \{[+200\mu V + 100k\Omega\,(35nA) - 100k\Omega\,(12.5\mu A)]$
$[1.02] + 100k\Omega\,(12.5\mu A)\} +$
$200\mu V/(1M\Omega/100k\Omega)$
$= \{[0.2mV + 3.5mV - 1.25V]$
$[1.02] + 1.25V\} + 0.02mV$
$= -21.2mV$

V_{OS} total RTO
$= V_{OS}$ total RTI $\times\ R_F/R_{IN}$
$= -21.2mV \times 10$
$= -212mV$

Note: This error is dominated by $I_{OS\ bipolar}$ and the reference current times the gain error (which appears as an offset). The error for unipolar operation is much lower. The error due to offset current can be zeroed using circuits shown in Figures 6 and 7. The gain error is adjusted by trimming either R_F or R_{IN}.

COMMON-MODE AND HIGH VOLTAGE ERRORS

Figure 3 shows a model of the ISO100 that can be used to analyze common-mode and high voltage behavior.

Definitions of CMR and IMR

I_{OS} is defined as the input current required to make the ISO100's output zero. CMRR and IMRR in the ISO100 are expressed as conductances. CMRR defines the relationship between a change in the applied common-mode voltage (V_{CM}) and the change in I_{OS} required to maintain the amplifier's output at zero:

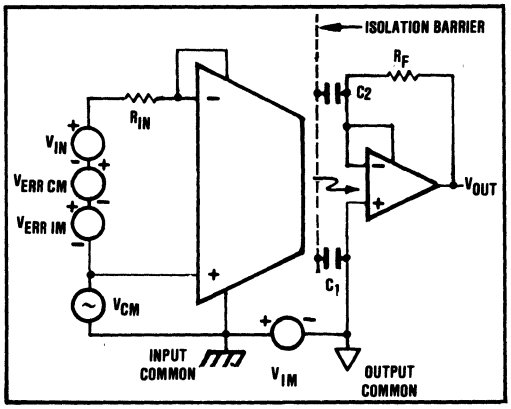


FIGURE 3. High Voltage Error Model.

$$CMRR\ (I\text{-mode}) = \Delta I_{OS}/\Delta V_{CM}\ \text{in nA/V} \quad (5)$$

$$CMRR\ (V\text{-mode}) = \left[\frac{\Delta I_{OS}}{\Delta V_{CM}}\right] R_{IN} = \frac{\Delta V_{ERR\ CM}}{\Delta V_{CM}}\ \text{in V/V} \quad (6)$$

IMRR defines the relationship between a change in the applied isolation mode voltage (V_{IM}) and the change in I_{OS} required to maintain the amplifier's output at zero:

$$IMRR\ (I\text{-mode}) = \frac{\Delta I_{OS}}{\Delta V_{IM}}\ \text{in pA/V} \quad (7)$$

$$IMRR\ (V\text{-mode}) = \left[\frac{\Delta I_{OS}}{\Delta V_{IM}}\right] R_{IN} = \frac{\Delta V_{ERR\ IM}}{\Delta V_{IM}}\ \text{in V/V} \quad (8)$$

CMRR & IMRR in V/V are a function of R_{IN}.

V_{IM} is the voltage between input common and output common.

V_{CM} is the common-mode voltage (noise that is present on both input lines, typically 60Hz).

V_{ERR} is the equivalent error signal, applied in series with the input voltage, which produces an output error identical to that produced by application of V_{CM} and V_{IM}.

CMRR and IMRR are the common-mode and isolation-mode rejection ratios, respectively.

TOTAL CAPACITANCE (C_1 and C_2) is distributed along the isolation barrier. Most of the capacitance is coupled to low impedance or noncritical nodes and affects only the leakage current. Only a small capacitance (C_2) couples to the input of the second stage, and contributes to IMRR.

Example 2: Refer to Figure 3 and Electrical Specification Table)

Given: V_{CM} = 1VAC peak at 60Hz, V_{IM} = 200VDC, CMRR = 3nA/V, IMRR = 5pA/V, R_{IN} = 100kΩ, R_F = 1MΩ (Gain = 10)

Find: The error voltage referred to the input and output when V_{IN} = 0V

$$V_{ERR\ RTI} = (V_{CM})(CMRR)(R_{IN}) + (V_{IM})(IMRR)(R_{IN})$$
$$= 1V\ (3nA/V)\ (100k\Omega) + 200V\ (5pA/V)(100k\Omega)$$
$$= 0.3mV + 0.1mV$$
$$= 0.4mV$$

$$V_{ERR\ RTO} = V_{ERR\ RTI}\ (R_F/R_{IN})$$
$$= 0.4mV\ (10)$$
$$= 4mV\ (\text{with DC IMRR})$$

(Note: This error is dominated by the CMRR term)

For purposes of comparing CMRR and IMRR directly with dB specifications, the following calculations can be performed:

$$CMRR\ \text{in V/V} = CMRR\ (\text{I-mode})(R_{IN})$$
$$= 3nA/V\ (100k) = 0.3mV/V$$

$$CMR = 20\ LOG\ (0.3mV/V) = -70dB\ \text{at 60Hz}$$

$$IMRR\ \text{in V/V} = IMRR\ (\text{I-mode})(R_{IN}) = 5pA/V(100k\Omega) = 0.5\mu V/V$$

$$IMR = 20\ LOG\ (0.5 \times 10^{-6} V/V) = -126dB\ \text{at DC}$$

Example 3:

In Example 2, V_{IM} is an AC signal at 60Hz and

$$IMRR = \frac{400pA}{V}$$

$$V_{ERR\ RTI} = V_{ERR\ CM} + V_{ERR\ IM}$$
$$= 0.3mV + 200V\ (400pA/V)(100k\Omega)$$
$$= 8.3mV$$
$$V_{ERR\ RTO} = 83mV\ (\text{with AC IMRR})$$

Example 4:

Given: Total error RTO from Examples 1 and 3 as 378mV worst case

Find: Percent error of +10V full scale output

$$\%\ \text{Error} = \frac{V_{ERR\ total}}{V_{FS}} \times 100$$
$$= \frac{378mV}{10V} \times 100$$
$$= 3.78\%$$

NOISE ERRORS

Noise errors in the unipolar mode are due primarily to the optical cavity. When the full 60kHz bandwidth is not needed, the output noise of the ISO100 can be limited by either a capacitor, C_F, in the feedback loop or by a low-pass filter following the output. This is shown in Figure 4. Noise in the bipolar mode is due primarily to the reference current sources, and can be reduced by the low-pass filters shown in Figure 5.

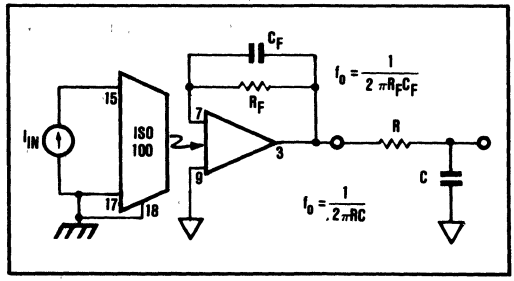


FIGURE 4. Two Circuit Techniques for Reducing Noise in the Unipolar Mode.

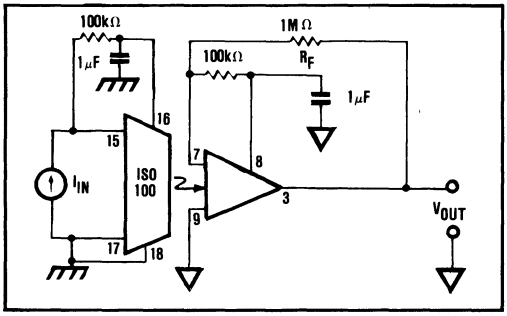


FIGURE 5. Circuit Technique for Reducing Noise from The Current Sources in the Bipolar-Mode.

OPTIONAL ADJUSTMENTS

There are two major sources of offset error: offset voltage and offset current. V_{OSI} and V_{OSO} of the input and output amplifiers can be adjusted independently using external potentiometers. An example is shown in Figure 17. Note that V_{OSO} (500μV, max) appears directly at the output, but V_{OSI} appears at the output multipled by gain (R_F/R_{IN}). In general, V_{OS} is small compared to the effect of I_{OS} (see Example 1). To adjust for I_{OS} use a circuit which intentionally unbalances the offset in one direction and then allows for adjustment back to zero.

Figure 6 shows how to adjust unipolar errors at zero input. The unipolar amplifier can be used down to zero input if it is made to be "slightly bipolar." By sampling the reference current with R_5 and R_6 the minimum current required to keep the input stage in the linear region of operation can be established. R_7 and R_8 are adjusted to cancel the offset created in the input stage. This brings the output to zero, when the input is zero. Although the amplifier can now operate down to zero input voltage, it has only a small portion of the current drain and noise that the true bipolar configuration would have.

Adjusting the bipolar errors is illustrated in Figure 7. Each of the errors are adjusted in turn. With V_{IN} = "open,", I_{OS} is trimmed by adjusting R_{10} to make the output zero. R_G is then adjusted to trim the gain error. The effects of offset voltage are removed by adjusting R_{14}.

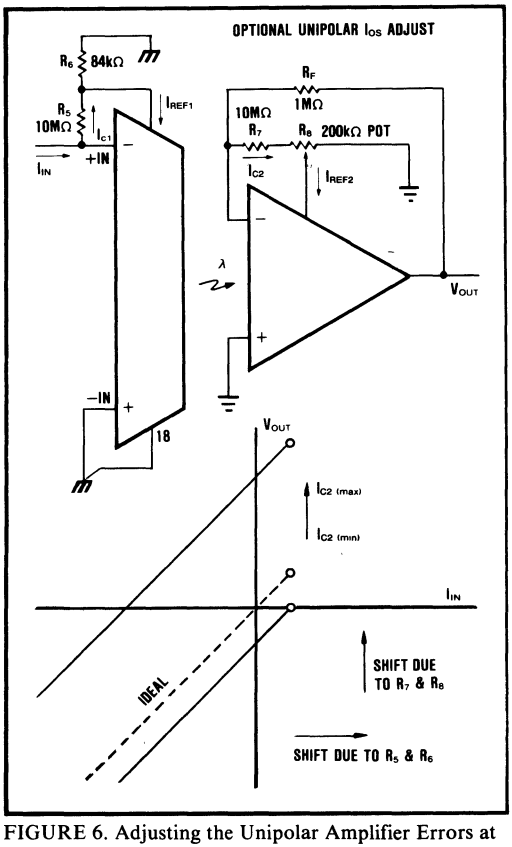


FIGURE 6. Adjusting the Unipolar Amplifier Errors at Zero Input.

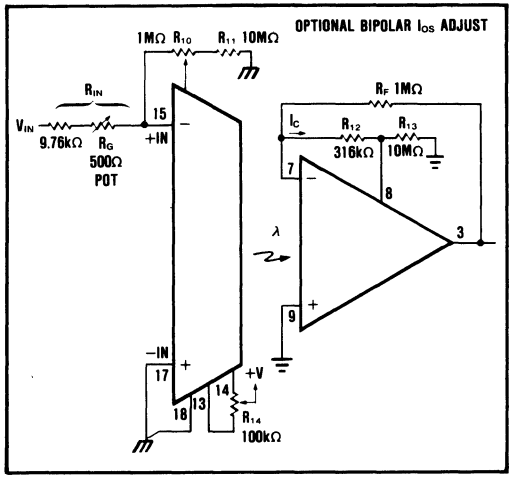


FIGURE 7. Adjusting the Bipolar Errors.

BASIC CIRCUIT CONNECTIONS

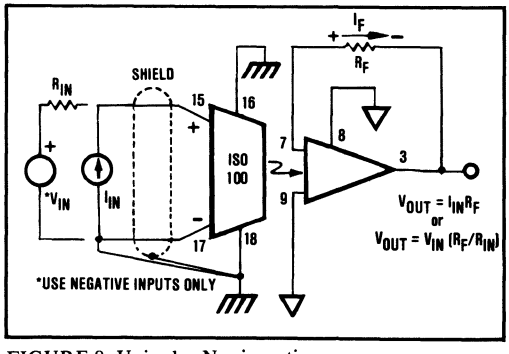


FIGURE 8. Unipolar Noninverting.

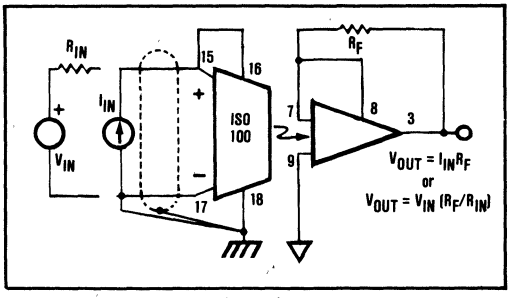


FIGURE 9. Bipolar Noninverting.

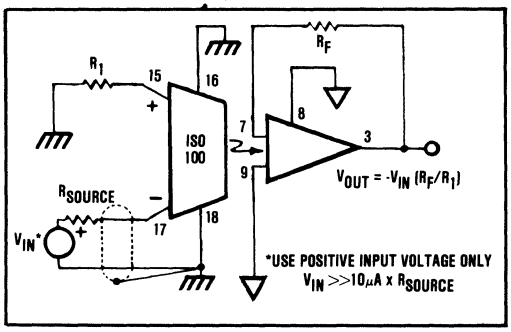


FIGURE 10. Unipolar Inverting.

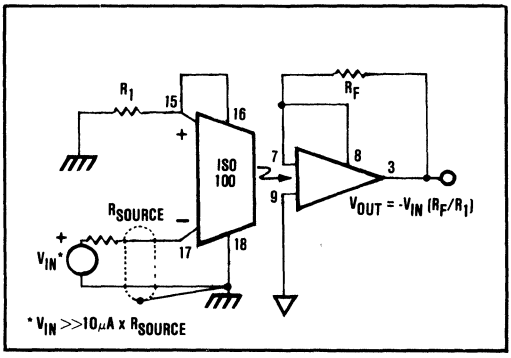


FIGURE 11. Bipolar Inverting.

APPLICATION INFORMATION

The small size, low offset and drift, wide bandwidth, ultra-low leakage, and low cost, make the ISO100 ideal for a variety of isolation applications. The basic mode of operation of the ISO100 will be determined by the type of signal and application.

Major points to consider when designing circuits with the ISO100.

1. Input Common (pin 18) and -IN (pin 17) should be grounded through separate lines. The Input Common can carry a large DC current and may cause feedback to the signal input
2. Use shielded or twisted pair cable at the input, for long lines.
3. Care should be taken to minimize external capacitance across the isolation barrier.
4. The distance across the isolation barrier, between external components, and conductor patterns, should be maximized to reduce leakage and arcing.
5. Although not an absolute requirement, the use of conformally-coated printed circuit boards is recommended.
6. When in the unipolar mode, the reference currents (pins 8 and 16) must be terminated. I_{IN} should be greater than 20nA to keep internal LED on.
7. The noise contribution of the reference currents will cause the bipolar mode to be noisier than the unipolar mode.
8. The maximum output voltage swing is determined by I_{IN} and R_F.

$$V_{SWING} = I_{IN_{max}} \times R_F$$

9. A capacitor (about 3pF) can be connected across R_1 to compensate for peaking in the frequency response. The peaking is caused by the pole generated by R_1 and the capacitance at the input of the output amplifier.

Figures 12 through 18 show applications of the ISO100.

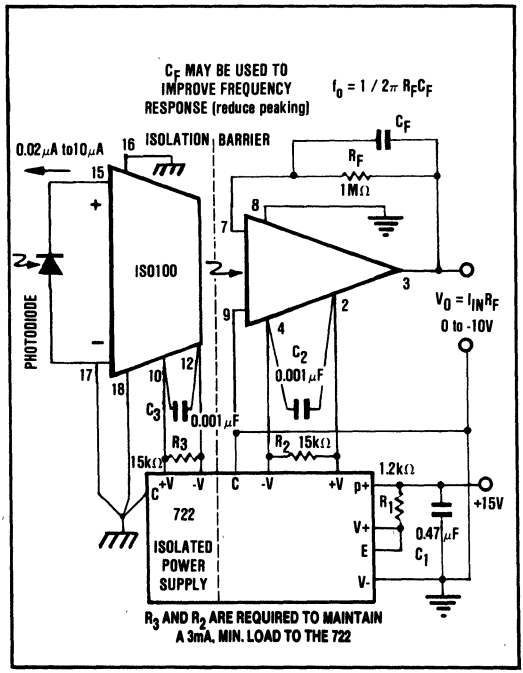


FIGURE 12. Two-Port Isolation Photodiode Amplifier Unipolar.

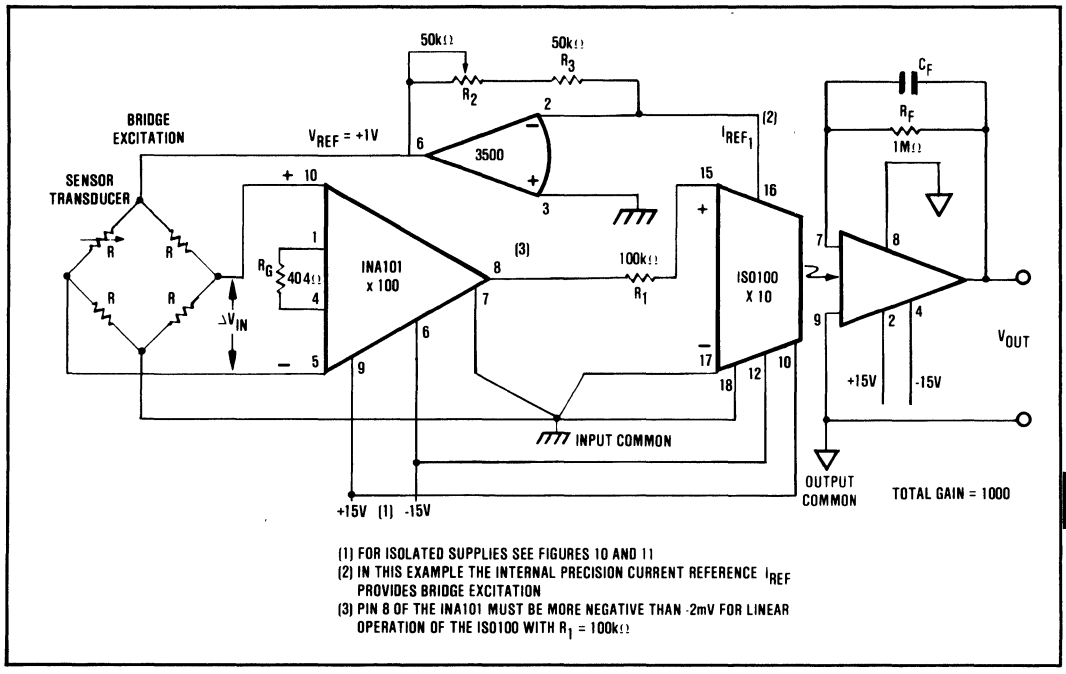


FIGURE 13. Precision Bridge Isolation Amplifier (Unipolar).

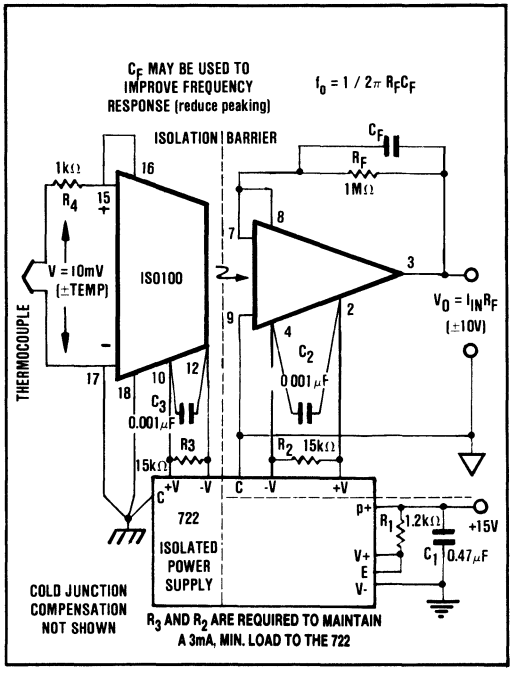


FIGURE 14. Three-Port Isolation Thermocouple Amplifier (Bipolar).

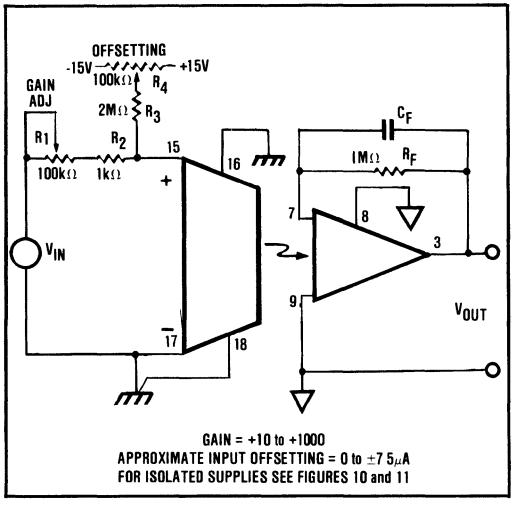


FIGURE 15. Isolated Test Equipment Amplifier (Unipolar with Offsetting).

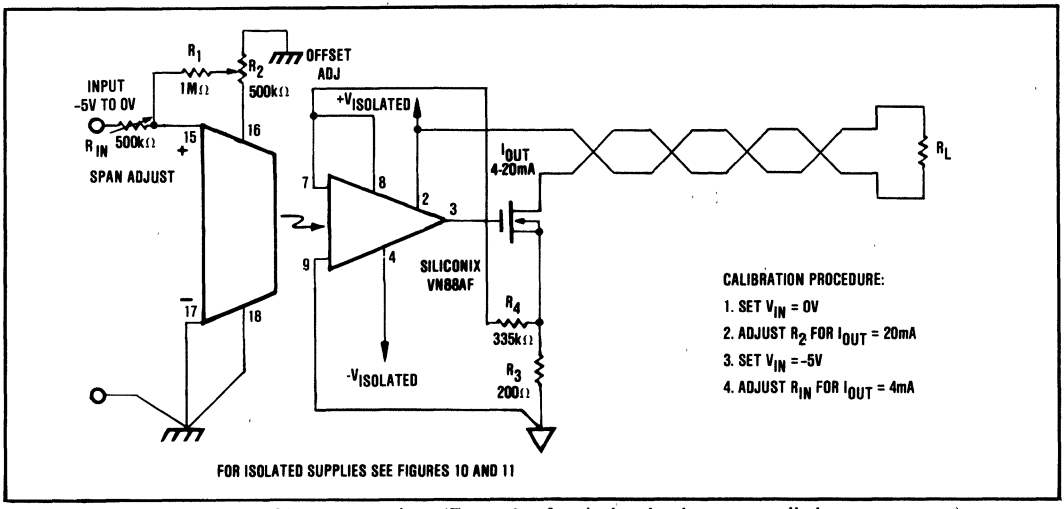


FIGURE 16. Isolated 4mA to 20mA Transmitter (Example of an isolated voltage controlled current source).

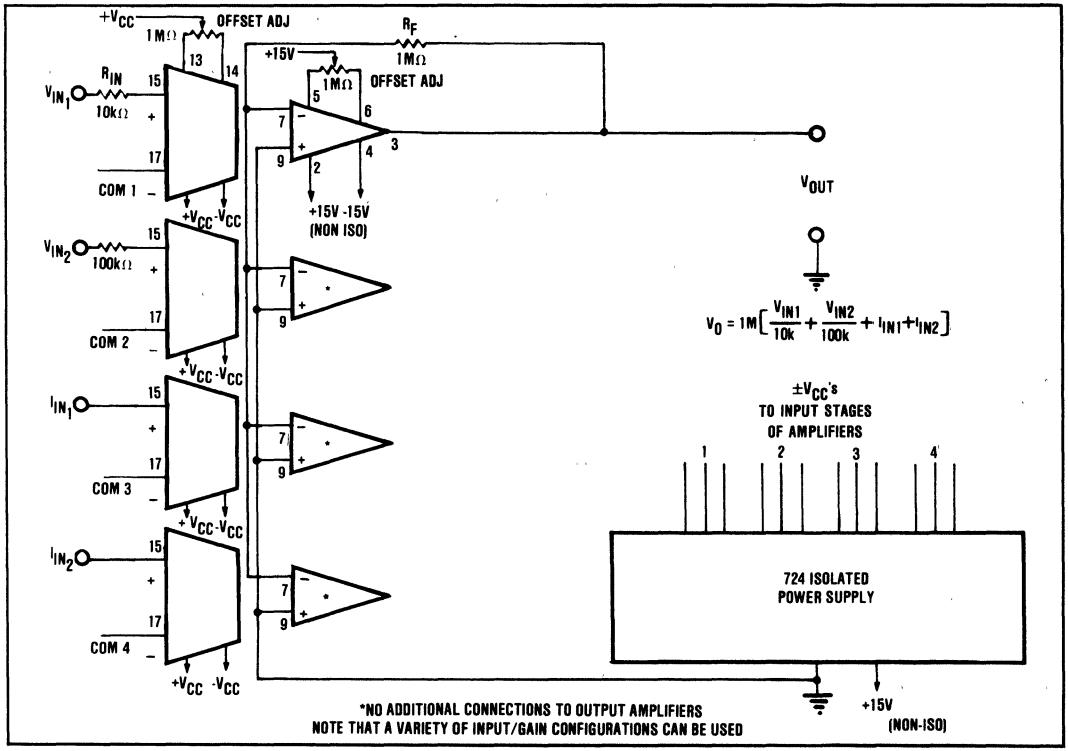


FIGURE 17. Four-Port Isolated Summing Amplifier (Unipolar).

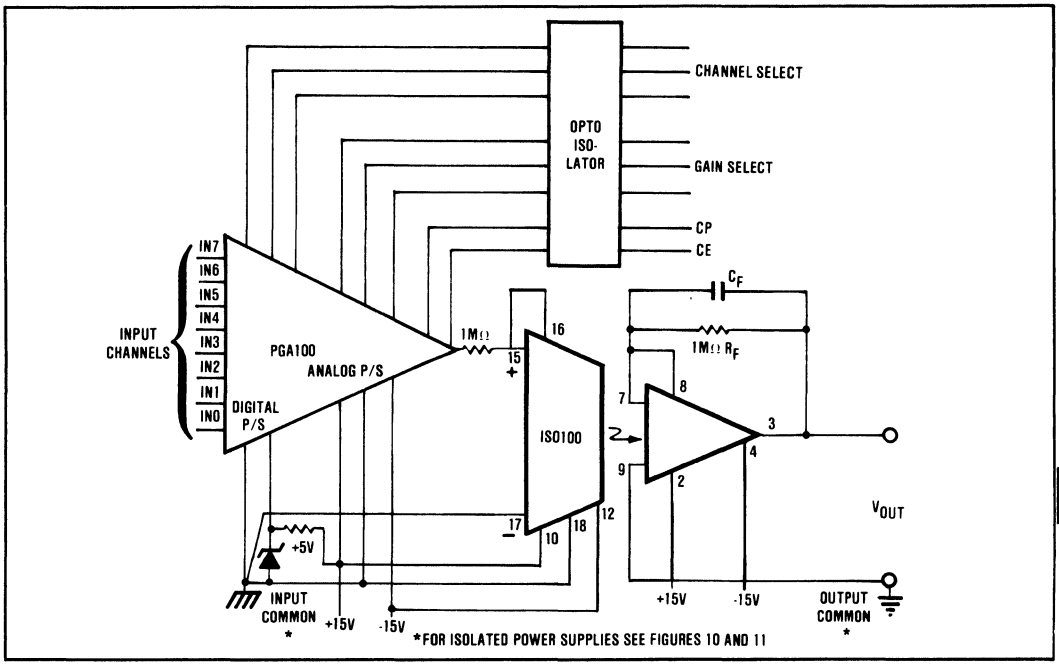


FIGURE 18. Multiple Channel Isolation Amplifier (Bipolar) with programmable Gain (Useful in Data Acquisition Systems).

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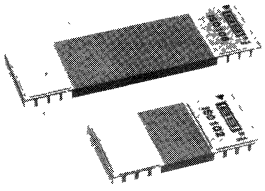

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- RUGGED BARRIER, HV CERAMIC CAPACITORS
- 100% TESTED FOR HIGH VOLTAGE BREAKDOWN
  ISO102: 4000Vrms/10s, 1500Vrms/1min
  ISO106: 8000Vpk/10s, 3500Vrms/1min
- ULTRA HIGH IMR: 125dB min at 60Hz, ISO106
- WIDE INPUT RANGE: −10V to +10V
- WIDE BANDWIDTH: 70kHz
- VOLTAGE REFERENCE OUTPUT: 5VDC

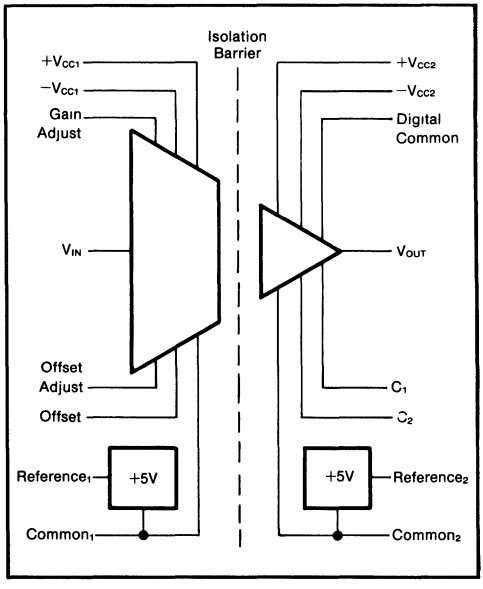
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer channel isolator for thermocouples, RTDs, pressure bridges, flow meters
- 4mA TO 20mA LOOP ISOLATION
- MOTOR AND SCR CONTROL
- GROUND LOOP ELIMINATION
- BIOMEDICAL/ANALYTICAL MEASUREMENTS
- POWER PLANT MONITORING
- DATA ACQUISITION/TEST EQUIPMENT ISOLATION
- MILITARY EQUIPMENT

DESCRIPTION

The ISO102 and ISO106 isolation buffer amplifiers are two members of a new series of low cost isolation products from Burr-Brown. They have the same electrical performance and differ only in continuous isolation voltage rating and package length. The ISO102 is rated for 1500Vrms in a 24-pin DIP. The ISO106 is rated for 3500Vrms in a 40-pin DIP. Both side-braze DIPs are 600 mil wide and have industry standard package dimensions with the exception of missing pins between input and output stages. This permits utilization of automatic insertion techniques in production. The three-chip hybrid with its generous high voltage spacing is easy to use (no external components are required).

Each buffer accurately isolates ±10V analog signals by digitally encoding the input voltage and uniquely coupling across a differential ceramic capacitive barrier. This design is nearly immune to variations in the barrier voltage. All elements necessary for operation are contained within the DIP. This provides low cost compact signal isolation in a hermetic package.



Covered by Patent Nos. 4,748,419 and others pending

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PDS-716B

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_{CC1} = V_{CC2} = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	ISO102, ISO106 ISO102B, ISO106B MIN	TYP	MAX	UNITS
ISOLATION					
Voltage					
Rated Continuous[1]					
ISO102: AC, 60Hz	T_{MIN} to T_{MAX}	1500			Vrms
DC	T_{MIN} to T_{MAX}	2121			VDC
ISO106: AC, 60Hz	T_{MIN} to T_{MAX}	3500			Vrms
DC	T_{MIN} to T_{MAX}	4950			VDC
Test Breakdown, AC, 60Hz					
ISO102	10 seconds	4000			Vrms
ISO106	10 seconds	8000			Vpk
Isolation-Mode Rejection[2]	V_{ISO} = Rated Continuous, 60Hz				
AC: ISO102		115	120		dB
			1	2	µVrms/V
ISO106		125	130		dB
			0 3	0 6	µVrms/V
DC		140	160		dB
			0.01	0 10	µVDC/V
Barrier Resistance			10^{14}		Ω
Barrier Capacitance			6		pF
Leakage Current	V_{ISO} = 240Vrms, 60Hz		0 5	1 0	µArms
INPUT					
Voltage Range	Rated Operation	−10		+10	V
Resistance		75	100		kΩ
Capacitive			5		pF
OUTPUT					
Voltage Range	Rated Operation	−10		+10	V
	Derated Operation	−12		+12	V
Current Drive		±5			mA
Short Circuit Current		9	20	50	mA
Ripple Voltage[6]	f = 0.5MHz to 1 5MHz		3		mVp-p
Resistance			0.3	1	Ω
Capacitive Load Drive Capability		10000			pF
Overload Recovery Time, 0.1%	$\|V_O\| > 12V$		30		µs
OUTPUT VOLTAGE NOISE					
Voltage f = 0.1Hz to 10Hz			50		µVp-p
f = 0.1Hz to 70kHz			16		µV/√Hz
Dynamic Range[7]: f = 0 1Hz to 70kHz	12-bit resolution, 1LSB, 20VFS		74		dB
f = 0 1Hz to 280Hz	16-bit resolution, 1LSB, 20VFS		96		dB
FREQUENCY RESPONSE					
Small Signal Bandwidth			70		kHz
Full Power Bandwidth, 0 1% THD	V_O = ±10V		5		kHz
Slew Rate	V_O = ±10V		0 5		V/µs
Settling Time, 0.1%	V_O = −10V to +10V		100		µs
Overshoot, Small Signal[8]	$C_1 = C_2 = 0$		40		%
VOLTAGE REFERENCES					
Voltage Output, Ref1, Ref2	No Load	+4 975	+5 00	+5 025	VDC
B Grade	No Load	+4 995	+5 00	+5 005	VDC
vs Temperature			±5	20	ppm/°C
vs Supplies			10		µV/V
vs Load			400	1000	µV/mA
Current Output		−0 1		+5	mA
Short Circuit Current		6	14	30	mA
POWER SUPPLIES					
Rated Voltage, $±V_{CC1}$, $±V_{CC2}$	Rated Performance		±15		V
Voltage Range		±10		±20	V
Quiescent Current $+V_{CC1}$	No Load		+11	+15	mA
$-V_{CC1}$			−9	−12	mA
$+V_{CC2}$			+25	+33	mA
$-V_{CC2}$			−15	−20	mA
Power Dissipation: $±V_{CC1}$			300	400	mW
$±V_{CC2}$			600	800	mW
TEMPERATURE RANGE					
Specification		−25		+85	*°C
Operating[9]		−55		+125	°C
Storage		−65		+150	°C
Thermal Resistance, θ_{JA}			40		°C/W

ELECTRICAL (CONT)

PARAMETER	CONDITIONS	ISO102 MIN	ISO102 TYP	ISO102 MAX	ISO102B MIN	ISO102B TYP	ISO102B MAX	UNITS
GAIN								
Nominal Gain			1			*		V/V
Initial Error[3]			±0 1	±0.25		0.07	0 13	% FSR
Gain vs Temperature			±20	±50		±12	±25	ppm FSR/°C
Nonlinearity[4]	V_O = 10V to +10V		±0.007	±0.012		±0.002	±0.003	% FSR
INPUT OFFSET VOLTAGE								
Initial Offset	V_{IN} = 0V		±25	±70		±15	±25	mV
vs Temperature			±250	±500		±150	±250	µV/°C
vs Power Supplies[5]	Input Stage, V_{CC1} = ±10V to ±20V	0	1 4	4.0	*	*	*	mV/V
	Output Stage, V_{CC2} = ±10V to ±20V	−4.0	−1.4	0	*	*	*	mV/V

PARAMETER	CONDITIONS	ISO106 MIN	ISO106 TYP	ISO106 MAX	ISO106B MIN	ISO106B TYP	ISO106B MAX	UNITS
GAIN								
Nominal Gain			1			*		V/V
Initial Error[3]			±0 1	±0 25		0.07	*	% FSR
Gain vs Temperature			±20	±50		±12	±25	ppm FSR/°C
Nonlinearity[4]	V_O = 10V to +10V		±0 04	±0 075		±0 007	±0 025	% FSR
INPUT OFFSET VOLTAGE								
Initial Offset	V_{IN} = 0V		±25	±70		*	*	mV
vs Temperature			±250	±500		±150	±250	µV/°C
vs Power Supplies[5]	Input Stage, V_{CC1} = ±10V to ±20V		3 7			*		mV/V
	Output Stage, V_{CC2} = ±10V to ±20V		−3 7			*		mV/V

NOTES. (1) 100% tested at rated continuous for 1 minute (2) Isolation-mode rejection is the ratio of the change in output voltage to a change in isolation barrier voltage It is a function of frequency as shown in the Typical Performance Curves This is specified for barrier voltage slew rates not exceeding 100V/µs. (3) Adjustable to zero FSR = Full Scale Range = 20V (4) Nonlinearity is the peak deviation of the output voltage from the best fit straight line. It is expressed as the ratio of deviation to FSR (5) Power Supply Rejection = change in V_{OS}/20V supply change (6) Ripple is the residual component of the barrier carrier frequency generated internally (7) Dynamic Range = FSR/(Voltage Spectral Noise Density × square root of User Bandwidth). (8) Overshoot can be eliminated by band-limiting (9) See Typical Performance Curve E for limitations

ABSOLUTE MAXIMUM RATINGS

Supply Without Damage	±20V
Input Voltage Range	±50V
Continuous Isolation Voltage Across Barrier	
ISO102	1500Vrms
ISO106	3500Vrms
Junction Temperature	+160°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Amplifier and Reference Output	
Short Circuit Duration	Continuous to Common

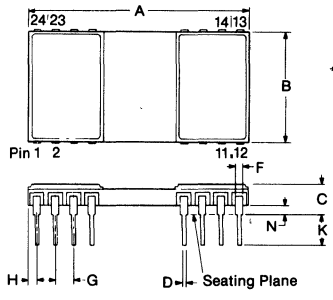
BURN-IN SCREENING

Burn-in screening is available for the ISO102 and ISO106. Burn-in duration is 160 hours at +85°C (or the equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

MECHANICAL

ISO102 24-Pin Double-Wide Hermetic DIP



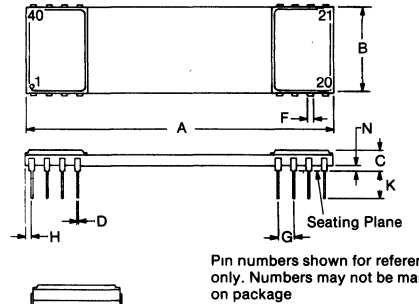
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1 190	1 210	30 23	30 73
B	580	600	14 73	15 24
C	140	185	3.56	4 70
D	015	021	0 38	0 53
F	030	060	0 76	1 52
G	100 BASIC		2 54 BASIC	
H	030	070	0 76	1 78
J	008	012	0 20	0 30
K	120	240	3 05	6 10
L	600 BASIC		15 24 BASIC	
M	—	10°	—	10°
N	025	060	0 64	1 52

CASE. Ceramic
WEIGHT 3 7g (0.13oz)

NOTE. Leads in true position within 0 01" (0.25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers may not be marked on package.

ISO106 40-Pin Double-Wide Hermetic DIP



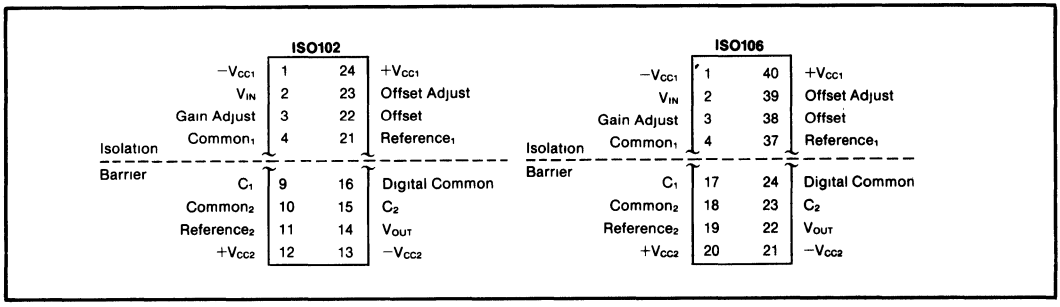
Pin numbers shown for reference only. Numbers may not be marked on package

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1 980	2 020	50 29	51 31
B	580	600	14 73	15 24
C	140	185	3 56	4 70
D	015	021	0 38	0 53
F	030	060	0 76	1 52
G	100 BASIC		2 54 BASIC	
H	030	070	0 76	1 78
J	008	012	0 20	0 30
K	120	240	3 05	6 10
L	600 BASIC		15 24 BASIC	
M	—	10°	—	10°
N	025	060	0 64	1 52

CASE Ceramic
WEIGHT 6 2g (0 22oz)

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane

PIN CONFIGURATION



PIN DESCRIPTIONS

$\pm V_{CC1}$, $Common_1$	Positive and negative power supply voltages and common (or ground) for the input stage $Common_1$ is the analog reference voltage for input signals.
$\pm V_{CC2}$, $Common_2$	Positive and negative power supply voltages and common (or ground) for the ouptut stage $Common_2$ is the analog reference voltage for output signals The voltage between $Common_1$ and $Common_2$ is the isolation voltage and appears across the internal high voltage barrier
V_{IN}	Signal input pin Input impedance is typically 100kΩ. The input range is rated for ±10V. The input level can actually exceed the input stage supplies Output signal swing is limited only by the output supply voltages
Gain Adjust	This pin is an optional signal input A series 5kΩ potentiometer between this pin and the input signal allows a guaranteed ±1 5% gain adjustment range. When gain adjustment is not required, the Gain Adjust should be left open Figure 4 illustrates the gain adjustment connection
$Reference_1$	+5V reference output This low drift zener voltage reference is necessary for setting the bipolar offset point of the input stage. **This pin must be strapped to either Offset or Offset Adjust to allow the isolation amplifier to function.** The reference is often useful for input signal conditioning circuits. See Typical Performance Curve H for the effect of offset voltage change with reference loading. $Reference_1$ is identical to, but independent of, $Reference_2$ This output is short circuit protected.
$Reference_2$	+5V reference output. This reference circuit is identical to, but independent of, $Reference_1$. It controls the bipolar offset of the output stage through an internal connection This output is short circuit protected.
Offset	Offset input **This input must be strapped to $Reference_1$** unless user adjustment of bipolar offset is required.
Offset Adjust	This pin is for optional offset control When connected to the $Reference_1$ pin through a 1kΩ potentiometer, ±150mV of adjustment range is guaranteed Under this condition, the Offset pin should be connected to the Offset Adjust pin When offset adjustment is not required, the Offset Adjust pin is left open See Figure 4
Digital Common	Digital common or ground. This separate ground carries currents from the digital portions of the output stage circuit. The best grounding practices require that digital common current does not flow in analog common connections In most systems the physical connection between analog and digital commons must be at the system power supplies terminal to insure digital noise is kept out of the analog signal Difference in potentials between the $Common_2$ and Digital Common pins can be ±1V See Figure 2
V_{OUT}	Signal output Because the isolation amplifier has unity gain, the output signal is ideally identical to the input signal The output is low impedance and is short-circuit-protected
C_1, C_2	Capacitors for small signal bandwidth control. These pins connect to the internal rolloff frequency controlling nodes of the output low-pass filter Additional capacitance added to these pins will modify the bandwidth of the buffer. C_2 is always twice the value of C_1 See Typical Performance Curve B for the relationship between bandwidth and C_1 and C_2. When no connections are made to these pins, the full small signal bandwidth is maintained. Be sure to shield C_1 and C_2 pins from high electric fields on the PC board This preserves AC Isolation Mode Rejection by reducing capacitive coupling effects

ORDERING INFORMATION

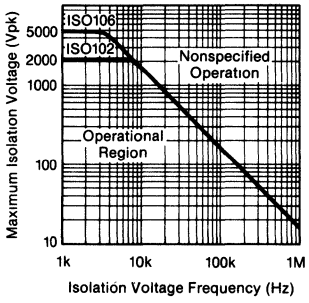
Model	Package	Temperature Range
ISO102	Ceramic	−25°C to +85°C
ISO102B	Ceramic	−25°C to +85°C
ISO106	Ceramic	−25°C to +85°C
ISO106B	Ceramic	−25°C to +85°C
BURN-IN SCREENING OPTION See text for details		
Model	**Package**	**Burn-In (160h)[1]**
ISO102-BI	Ceramic	+85°C
ISO102B-BI	Ceramic	+85°C
ISO106-BI	Ceramic	+85°C
ISO106B-BI	Ceramic	+85°C

NOTE (1) Or equivalent combination. See text

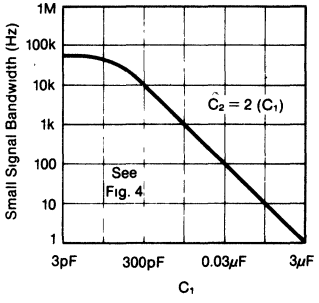
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted

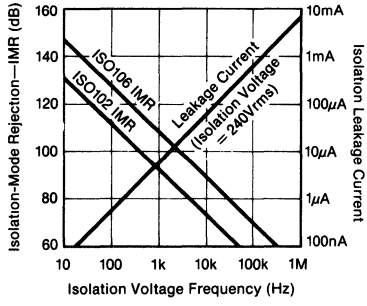
A. RECOMMENDED RANGE OF ISOLATION VOLTAGE



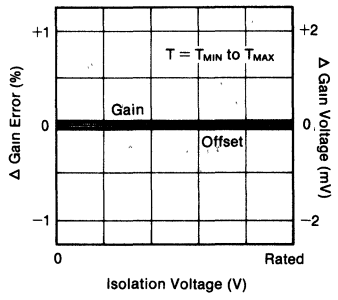
B. BANDWIDTH CONTROL



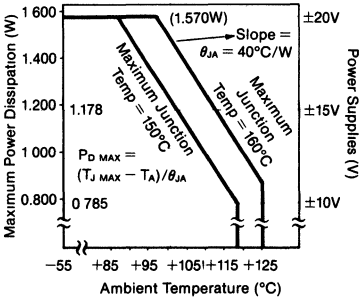
C. IMR/LEAKAGE VS FREQUENCY



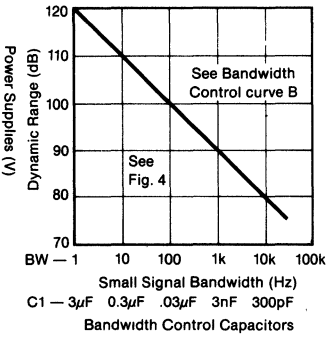
D GAIN ERROR/OFFSET ISOLATION VOLTAGE



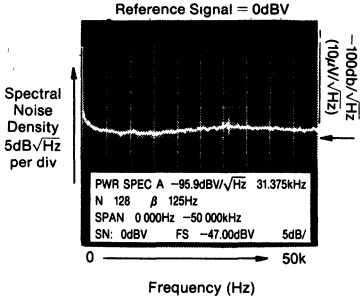
E POWER DISSIPATION VS TEMPERATURE



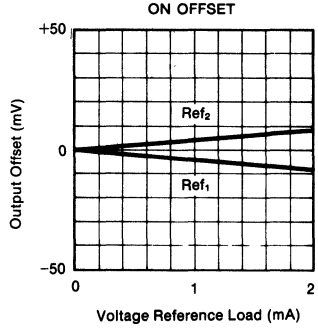
F DYNAMIC RANGE VS BANDWIDTH



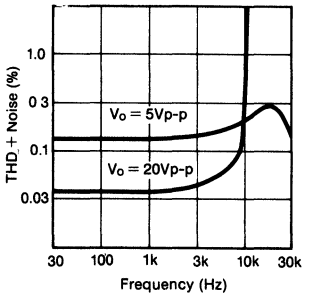
G. OUTPUT SPECTRAL NOISE DENSITY
Reference Signal = 0dBV



H. EFFECT OF REFERENCE LOADING ON OFFSET



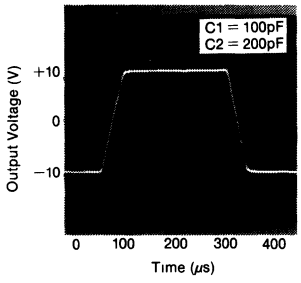
I TOTAL HARMONIC DISTORTION



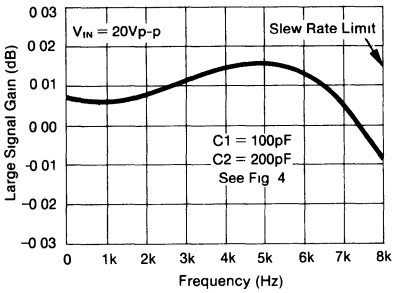
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

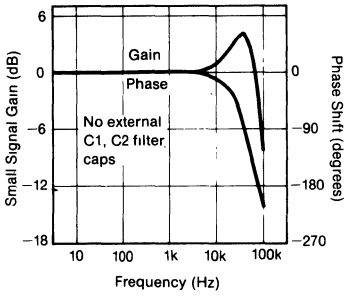
J LARGE SIGNAL TRANSIENT RESPONSE



K GAIN FLATNESS vs FREQUENCY



L GAIN/PHASE VS FREQUENCY



THEORY OF OPERATION

The ISO102 and ISO106 have no galvanic connection between the input and output. The analog input signal referenced to the input common is accurately duplicated at the output referenced to the output common. Because the barrier information is digital, potentials between the two commons can assume a wide range of voltages and frequencies without influencing the output signal. Signal information remains undisturbed until the slew rate of the barrier voltage exceeds 100V/μs. The amplifier is protected from damage for slew rates up to 100,000V/μs.

A simplified diagram of the ISO102 and ISO106 is shown in Figure 1. The design consists of an input voltage-controlled oscillator (VCO) also known as a voltage-to-frequency converter (VFC), differential capacitors, and output phase lock loop (PLL). The input VCO drives

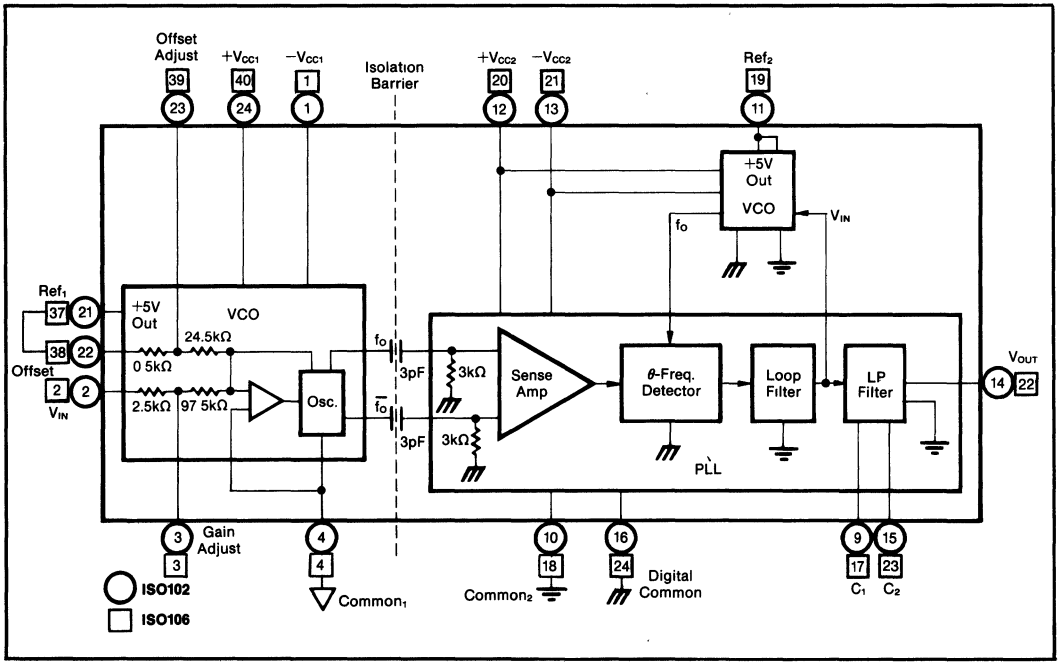


FIGURE 1. Simplified Diagram of ISO102 and ISO106.

digital levels directly into the two 3pF barrier capacitors. The digital signal is frequency modulated and appears differentially across the barrier while the externally applied isolation voltage appears common-mode.

A sense amplifier detects only the differential information. The output stage decodes the frequency modulated signal by the means of a PLL. The feedback of the PLL employs a second VCO that is identical to the encoder VCO. The PLL forces the second VCO to operate at the same frequency (and phase) as the encoder VCO; therefore, the two VCOs have the same input voltage. The input voltage of the decoder VCO serves as the isolation buffer's output signal after passing through a 100kHz second order active filter.

For a more detailed description of the internal operation of the ISO102 and ISO106 refer to *Proceedings of the 1987 International Symposium on Microelectronics* pages 202-206.

ABOUT THE BARRIER

For any isolation product, barrier composition is of paramount importance in achieving high reliability. Both the ISO102 and ISO106 utilize two 3pF high voltage ceramic coupling capacitors. They are constructed of tungsten thick film deposited in a spiral pattern on a ceramic substrate. Capacitor plates are buried in the package, making the barrier very rugged and hermetically sealed. Capacitance results from the fringing electric fields of adjacent metal runs. Dielectric strength exceeds 10kV and resistance is typically $10^{14}\Omega$. Input and output circuitry are contained in separate solder-sealed cavities, resulting in the industry's first fully hermetic hybrid isolation amplifier.

The ISO102 and ISO106 are free from partial discharge at rated voltages. Partial discharge is a form of localized breakdown that degrades the barrier over time. Since it does not bridge the space across the barrier, it is difficult to detect. Both isolation amplifiers have been extensively evaluated at high temperature and high voltage.

POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 2 shows the proper power supply and signal connections. Each supply should be AC-bypassed to Analog Common with 0.1μF ceramic capacitors as close to the amplifier as possible. Short leads will minimize lead inductance. A ground plane will also reduce noise problems. Signal common lines should tie directly to the common pin if a low impedance ground plane is not used. Refer to Digital Common in the Pin Descriptions table.

To avoid gain and isolation-mode rejection (IMR) errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance. Any capacitance across the barrier will increase AC leakage current and may degrade high frequency IMR. The schematic in Figure 3 shows the proper technique for wiring analog and digital commons together.

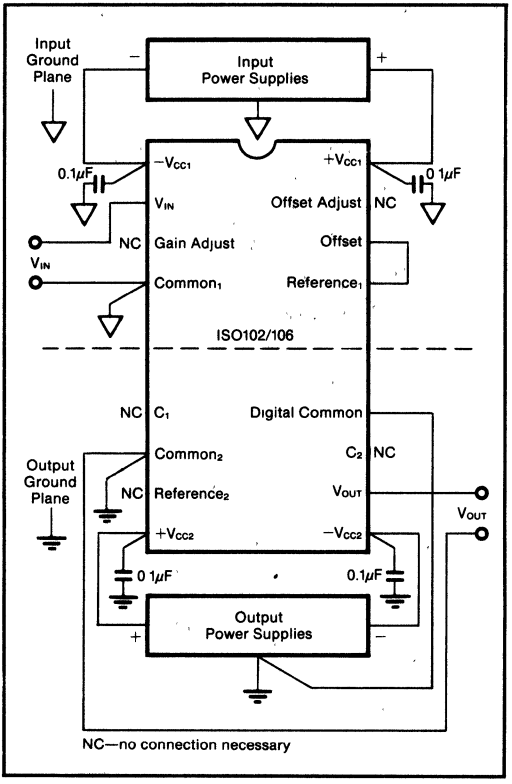


FIGURE 2. Power Supply and Signal Connection for ISO102 and ISO106.

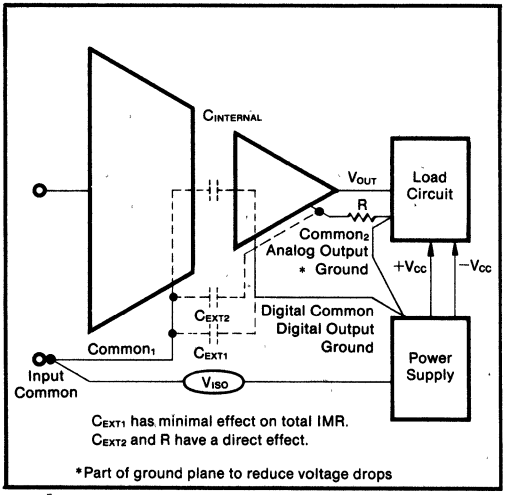


FIGURE 3. Technique for Wiring Analog and Digital Commons Together in the ISO102 and ISO106.

DISCUSSION OF SPECIFICATIONS

The ISO102 and ISO106 are unity gain buffer isolation amplifiers primarily intended for high level input voltages on the order of 1V to 10V. They may be preceded by operational, differential, or instrumentation amplifiers that precondition a low level signal on the order of millivolts and translate it to a high level.

ISOLATION-MODE REJECTION

The ISO102 and ISO106 provide exceptionally high isolation-mode rejection over a wide range of isolation-mode voltages and frequencies. The typical performance curves should be used to insure operation within the recommended range. The maximum barrier voltage allowed decreases as the frequency of the voltage increases. As with all isolation amplifiers, a change of voltage across the barrier will induce leakage current across the barrier. In the case of the ISO102 and ISO106, there exists a threshold of leakage current through the signal capacitors that can cause over-drive of the decoder's sense amplifier. This occurs when the slew rate of the isolation voltage reaches 100V/μs. The output will recover in about 50μs from transients exceeding 100V/μs.

Typical Performance Curve C indicates the expected isolation-mode rejection over a wide range of isolation voltage frequencies. Also plotted is the typical leakage current across the barrier at 240Vrms. The majority of the leakage current is between the input common pin and the output digital ground pin.

The ISO102 and ISO106 are intended to be continuously operated with fully rated isolation voltage and temperature without significant drift of gain and offset. See performance curve D for changes in gain and offset with isolation voltage.

SUPPLY AND TEMPERATURE RANGE

The ISO102 and ISO106 are rated for ±15V supplies; however, they are guaranteed to operate from ±10V to ±20V. Performance is also rated for an ambient temperature range of −25°C to +85°C. For operation outside this temperature range, refer to performance curve E to establish the maximum allowed supply voltage. Supply currents are fairly insensitive to changes in supply voltage or temperature. Therefore, the maximum current limits can be used in computing the maximum junction temperature under nonrated conditions.

OPTIONAL BANDWIDTH CONTROL

The following discussion relates optimum dynamic range performance to bandwidth, noise, and settling time.

The outputs of the ISO102 and ISO106 are the outputs of a second order low-pass Butterworth filter. Its low impedance output is rated for ±5mA drive and ±12V range with 10,000pF loads. The closed-loop bandwidth of the PLL is 70kHz, while the output filter is internally set at 100kHz. The output filter lowers the residual voltage of the barrier FM signal to below the noise floor of the output signal.

Two pins are available for optional modification of the filter's bandwidth. Only two capacitors are required. Performance curve B gives the value of C_1 (C_2 is equal to twice C_1) for the desired bandwidth. Figure 4 illustrates the optional connection of both capacitors.

A tradeoff can be achieved between the required signal bandwidth and system dynamic range. The noise floor of the output limits the dynamic range of the output signal. The noise power varies with the square root of the bandwidth of the buffer. It is recommended that the bandwidth be reduced to about twice the maximum signal bandwidth for optimum dynamic range as shown in performance curve F. The output spectral noise density measurement is displayed in performance curve G. The noise is flat to within 5dB$\sqrt{\text{Hz}}$ between 0.1Hz to 70kHz.

The overall AC gain of the buffer amplifiers is shown in performance curves K and L. Note that with C_1 = 100pF and C_2 = 200pF, the AC gain remains flat within ±0.01dB up to 7kHz. The total harmonic distortion for large signal sine wave outputs is plotted in performance curve I. The phase-lock-loop displays slightly nonuniform rise and fall edges under maximum slew conditions. Reducing the output filter bandwidth to below 70kHz smoothes the output signal and eliminates any overshoot. See the settling time performance curve J.

OPTIONAL OFFSET AND GAIN ADJUSTMENT

In many applications the factory-trimmed offset is adequate. For situations where reduced or modified gain and offset are required, adjustment of each is easy. The addition of two potentiometers as shown in Figure 4 provides for a two step calibration.

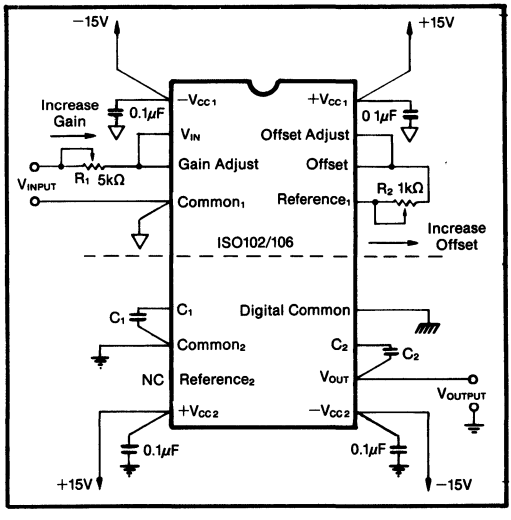


FIGURE 4. Optional Gain Adjust, Offset Adjust, and Bandwidth Control.

Offset should be adjusted first. Gain adjustment does not interfere with offset. The potentiometer's TCR adds only 2% to overall temperature drift.

The offset and gain adjustment procedures are as follows:

1. Set V_{IN} to 0V and adjust R_1 to desired offset at the output.
2. Set V_{IN} to full scale (not zero). Adjust R_2 for desired gain.

PRINTED CIRCUIT BOARD LAYOUT

The distance across the isolation barrier, between external components, and conductor patterns, should be maximized to reduce leakage and arcing at high voltages. Good layout techniques that reduce stray capacitance will assure low leakage current and high AC IMR. For some applications, applying conformal coating compound such as urethane is useful in maintaining good performance. This is especially true where dirt, grease or moisture can collect on the PC board surface, component surface, or component pins. Following this industry-accepted practice will give best results, particularly when circuits are operated or tested in a moisture-condensing environment. Optimum coating can be achieved by administering urethane under vacuum conditions. This allows complete coverage of all areas.

Figure 5 shows the recommended layout of the DEM102 demonstration board. This board contains the ISO102 and PWS725. The PWS725 is a DC-to-DC converter with a rated barrier voltage of 1500Vrms. It provides isolated power for the ISO102's input stage and other input circuitry that may be used. The DEM102 board illustrates the ease of use of these components. Notice that the ISO102's external high voltage spacing is maintained on both sides of the PC board layout. The placement of bypass capacitors, gain and offset potentiometers, and the PWS725's input ripple filter components are shown. The DEM106 layout in Figure 6 is similar to the DEM102. It contains the ISO106 and PWS726, which is rated for 3500Vrms. The schematic of both demonstration boards appears in Figure 7. Boards are available from Burr-Brown to facilitate fast, easy evaluation of electrical and isolation performance.

Isolation-mode rejection can be affected by the PC board layout. The most critical pins for obtaining maximum IMR are C_1 and C_2. These are the only high impedance nodes under normal operation and can be influenced by the barrier's voltage if not shielded. Grounded rings around the C_1 and C_2 contacts on the board greatly reduce high voltage electric fields at these pins. Maximum IMR is achieved when a ground plane is provided on both sides of the C_1, C_2 interconnect.

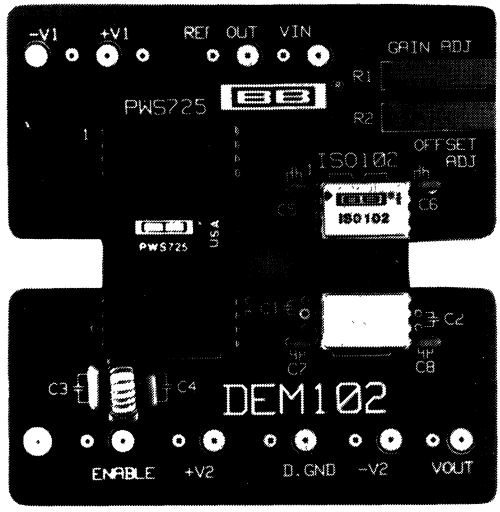


FIGURE 5. Recommended Layout for ISO102 and PWS725 (Demonstration Board DEM102).

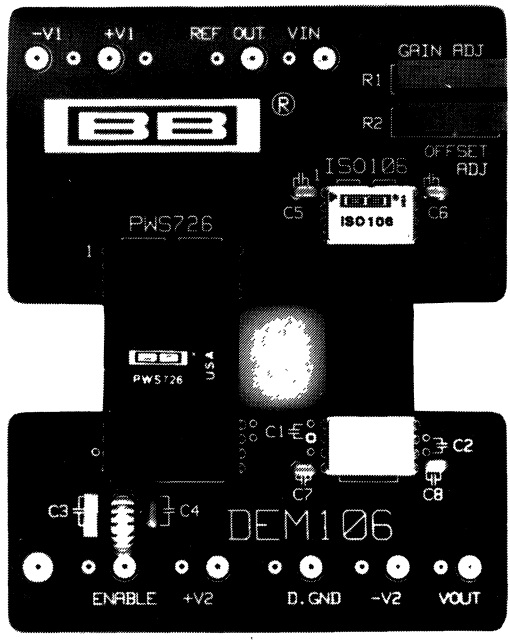


FIGURE 6. Recommended Layout for ISO106 and PWS726 (Demonstration Board DEM106).

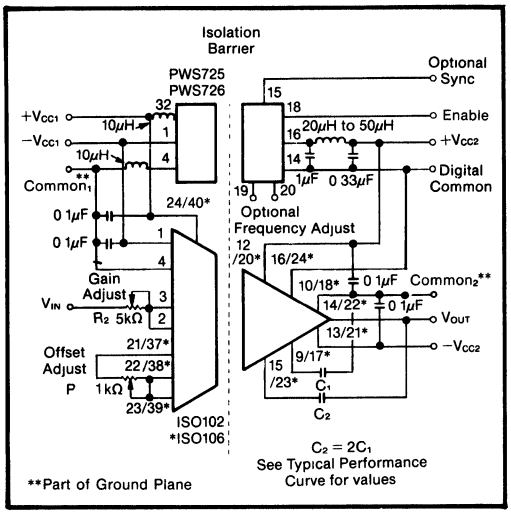


FIGURE 7. Schematic for Layout in Figures 5 and 6.

APPLICATIONS

The ISO102 and ISO104 isolation amplifiers are used in three categories of applications:

1. accurate isolation of signals from high voltage ground potentials,
2. accurate isolation of signals from severe ground noise, and
3. fault protection from high voltages in analog measurement systems.

Figures 8 through 18 show a variety of application circuits.

Additional discussion of application can be found in December 11, 1986 issue of *Electronic Design*, pages 91-96.

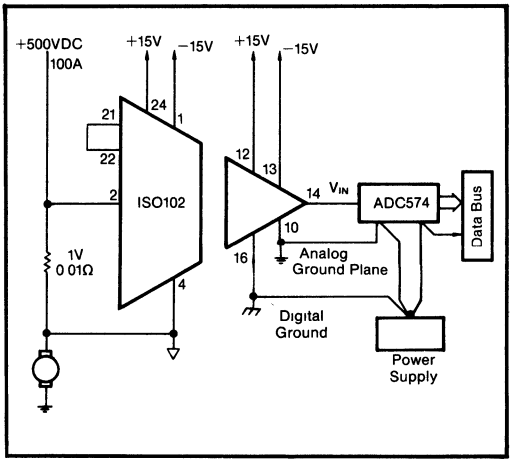


FIGURE 8. Isolated Power Current Monitor for Motor Circuit. (The ISO102 allows reliable safe measurement at high voltages.)

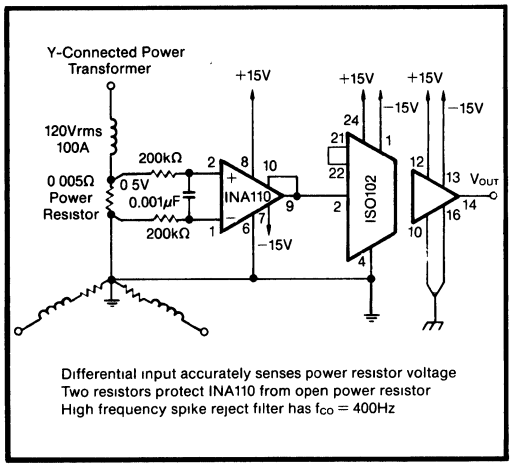


FIGURE 9. Isolated Power Line Monitor (0.5μA leakage current at 120Vrms.)

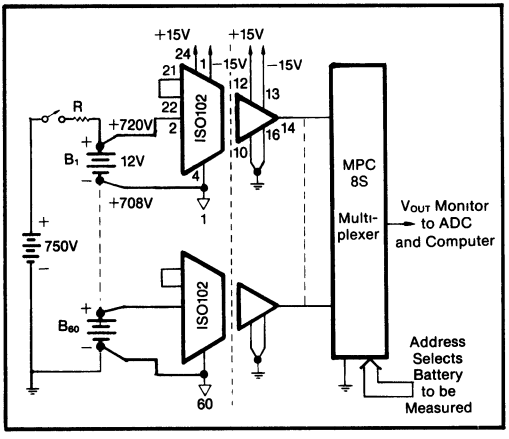


FIGURE 10. Battery Monitor for High Voltage Charging Circuit.

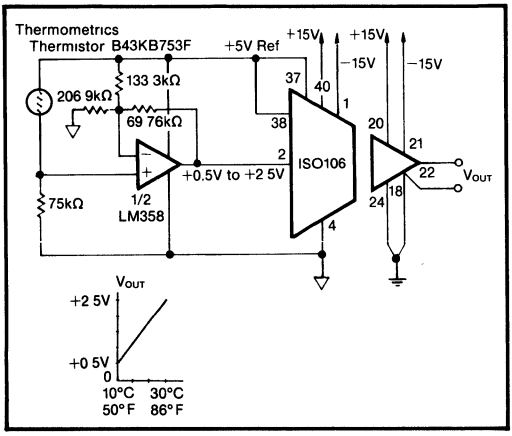


FIGURE 11. Isolated RTD Temperature Amplifier.

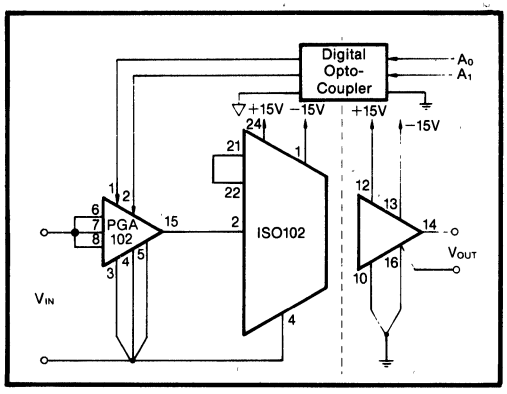


FIGURE 12. Programmable-Gain Isolation Channel with Gains of 1, 10, and 100.

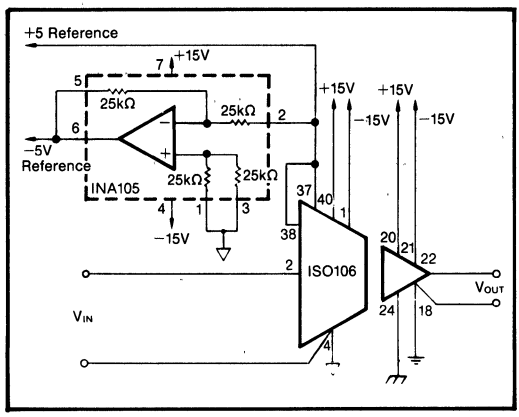


FIGURE 13. Isolation Amplifier with Isolated Bipolar Input Reference.

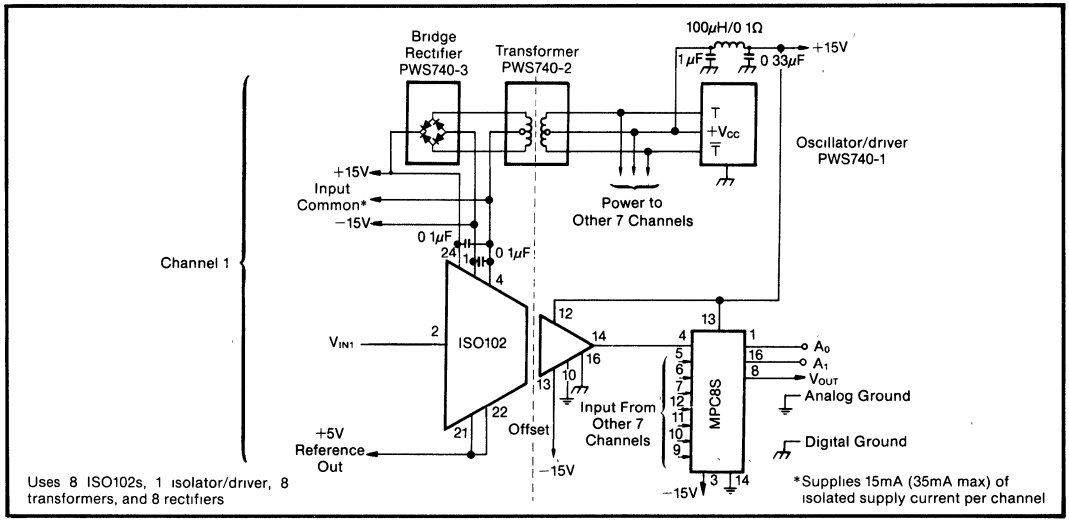


FIGURE 14. Low Cost Eight-Channel Isolation Amplifier Block with Channel-to-Channel Isolation.

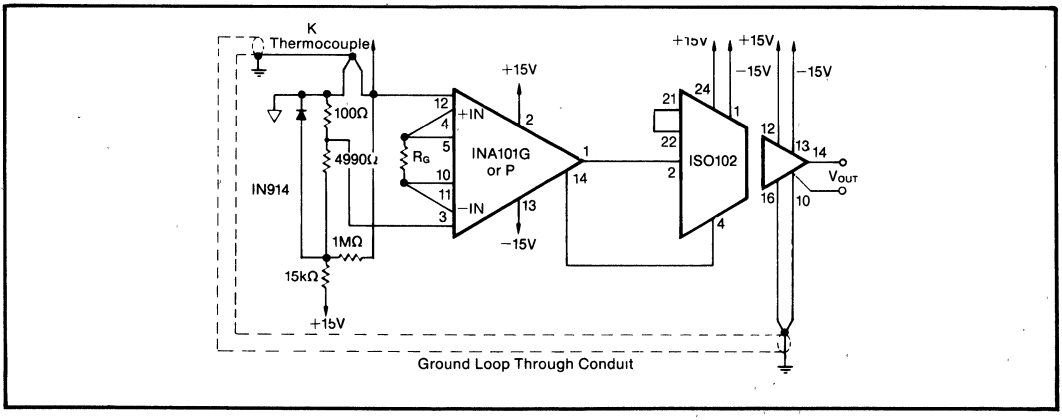


FIGURE 15. Thermocouple Amplifier with Ground Loop Elimination, Cold Junction Compensation, and Up-scale Burn-out.

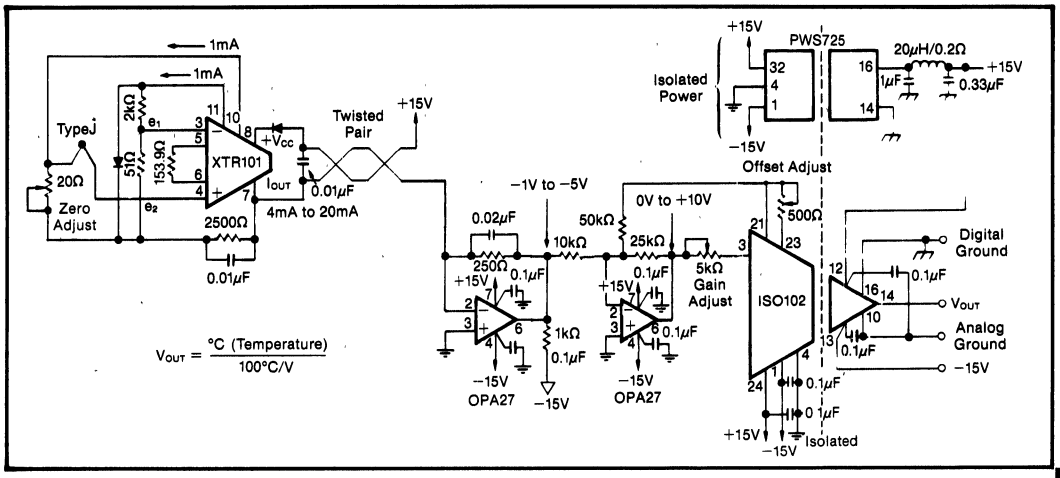


FIGURE 16. Remote Isolated Thermocouple Transmitter with Cold Junction Compensation.

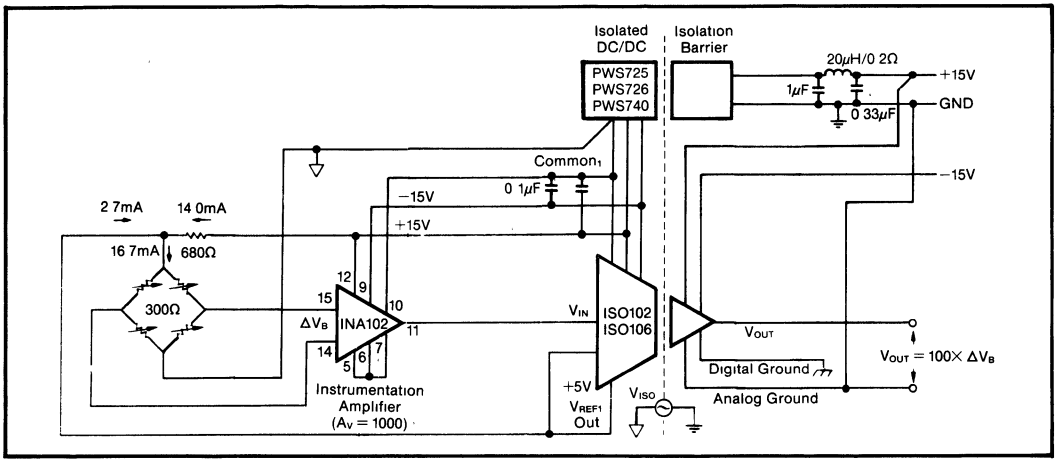


FIGURE 17. Isolated Instrumentation Amplifier for 300Ω Bridge. (Reference voltage from isolation amplifier is used to excite bridge.)

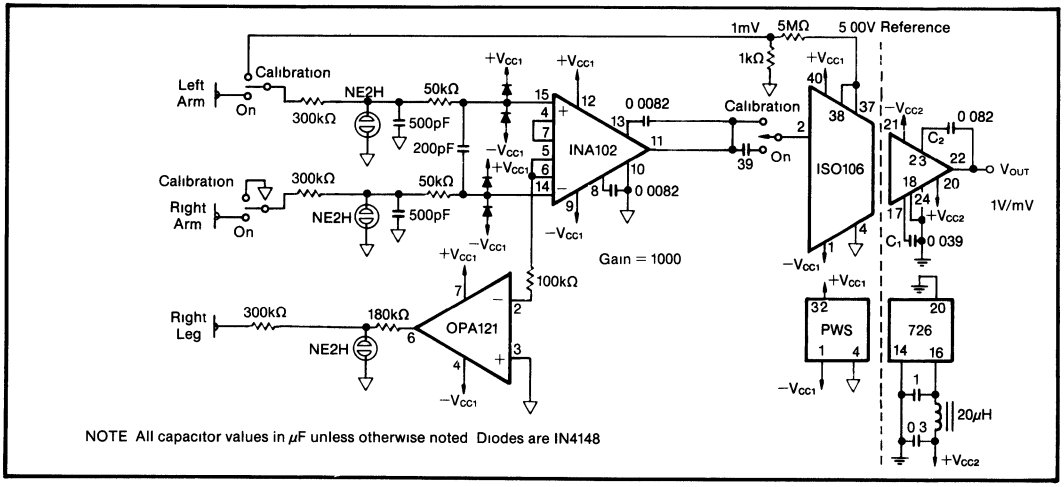


FIGURE 18. Right-Leg Driven ECG Amplifier (with defibrillator protection and calibrator).

AN ERROR ANALYSIS OF THE ISO102 IN A SMALL SIGNAL MEASURING APPLICATION

High accuracy measurements of low-level signals in the presence of high isolation mode voltages can be difficult due to the errors of the isolation amplifiers themselves.

This error analysis shows that when a low drift operational amplifier is used to preamplify the low-level source signal, a low cost, simple and accurate solution is possible.

In the circuit shown in Figure 19, a 50mV shunt is used to measure the current in a 500VDC motor. The OPA27 amplifies the 50mV by 200 × to 10V full scale. The output of the OPA27 is fed to the input of the ISO102, which is a unity-gain isolation amplifier. The 5kΩ and 1kΩ potentiometers connected to the ISO102 are used to adjust the gain and offset errors to zero as described in Discussion of Specifications.

Some Observations

The total errors of the op amp and the iso amp combined are approximately 0.11% of full-scale range (see Figure 20). If the op amp had not been used to preamplify the signal, the errors would have been 2.6% of FSR. Clearly, the small cost of adding the op amp buys a large performance improvement. Optimum performance, therefore, is obtained when the full ±10V range of the ISO102/106 is utilized.

The rms noise of the ISO102 with a 120Hz bandwidth is only 0.18mVrms, which is only 0.0018% of the 10V full-scale output. Therefore, even though the $16\mu V/\sqrt{Hz}$ noise spectral density specification may appear large compared to other isolation amplifiers, it does not turn out to be a significant error term. It is worth noting that even if the bandwidth is increased to 10kHz, the noise of the iso amp would only contribute 0.016%FSR error.

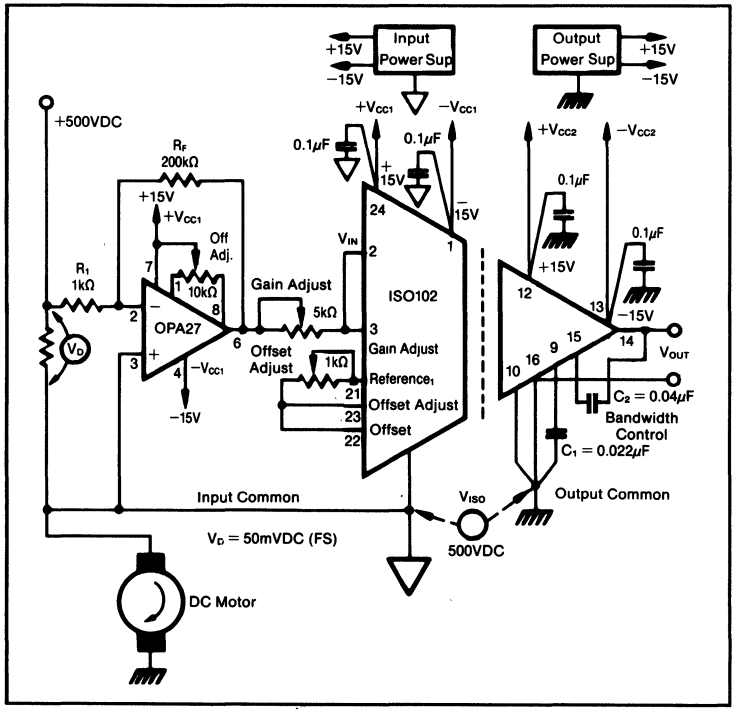


FIGURE 19. 50mV Shunt Measures Current in a 500VDC Motor.

The Errors Of The Op Amp At 25°C (Referred To Input, RTI)

$$V_{E\,(OPA)} = V_D \left[1 - \frac{1}{1 + \frac{1}{\beta A_{VOL}}}\right] + V_{OS}\left[1 + \frac{R_1}{R_F}\right] + I_B R_1 + P.S.R + Noise$$

$V_{E\,(OPA)}$ = Total Op Amp Error (RTI)

V_D = Differential Voltage (Full Scale) Across Shunt

$\left[1 - \frac{1}{1 + \frac{1}{\beta A_{VOL}}}\right]$ = Gain Error Due to Finite Open Loop Gain

β = Feedback Factor

A_{VOL} = Open Loop Gain at Signal Frequency

V_{OS} = Input Offset Voltage

I_B = Input Bias Current

P S R = Power Supply Rejection (μV/V) [Assuming a 5% change with ±15V supplies. Total error is twice that due to one supply]

Noise = 5nV$\sqrt{Hz}$ (for 1kΩ source resistance and 1kHz bandwidth)

$ERROR_{(OPA)}$ (RTI)		GAIN ERROR		OFFSET		P.S.R.		NOISE
$V_{E\,(OPA)}$	=	50mV $\left[1 - \frac{1}{1 + \frac{1}{10^6/200}}\right]$		$\left[0{,}025\text{mV}\left(1 + \frac{1}{200}\right) + 40 \times 10^{-9} \times 10^3\right]$		(20μV/V x 0 75V x 2)		[5nV$\sqrt{120}$ (nVrms)]
	=	0 01mV		[0,0251mV + 0,04mV]	+	0.03mV	+	0,055 × 10^{-3}mVrms
Error as % of FSR	=	0 02%	+	[0 05% + 0 08%]	+	0 06%	+	0 00011%
After Nulling								
	=	0 01mV	+	[0mV + 0mV]	+	0 03mV	+	0 055 × 10^{-3}mVrms
	=	0 10mV						
Error as % of FSR*	=	0 02%	+	[0% + 0%]	+	0 06%	+	0 00011%
	=	0 08% of 50mV						

*FSR = Full-Scale Range 50mV at input to op amp, or 10V at input (and output) of ISO amp

The Errors Of The ISO Amp At 25°C (RTI)

$$V_{E\,(ISO)} = \frac{1}{200}\left[\frac{V_{ISO}}{IMR} + V_{OS} + G\,E + Nonlinearity + P\,S\,R + Noise\right]$$

$V_{E\,(ISO)}$ = Total ISO Amp Error

IMR = Isolation Mode Rejection

V_{OS} = Input Offset Voltage

$V_{ISO} = V_{IMV}$ = Isolation Voltage = Isolation Mode Voltage

G E = Gain Error (% of FSR)

Nonlinearity = Peak-to-peak deviation of output voltage from best-fit straight line It is expressed as ratio based on full-scale range

P S R = Change in V_{OS}/10V × Supply Change

Noise = Spectral noise density × $\sqrt{\text{bandwidth}}$ It is recommended that bandwidth be limited to twice maximum signal bandwidth for optimum dynamic range

$ERROR_{(ISO)}$ (RTI)		IMR		V_{OS}		G.E.		NONLINEARITY		P.S.R.		NOISE
$V_{E\,(ISO)}$	=	$\frac{1}{200}\left[\frac{500\text{VDC}}{140\text{dB}}\right.$	+	70mV	+	20V × $\frac{0\,25}{100}$	+	$\frac{003}{100}$ × 20V		1 4mV x 0 75V x 2	+	16μV$\sqrt{120}$ (rms)$\left.\right]$
	=	$\frac{1}{200}$ [0 05mV	+	70mV	+	50mV	+	0 6mV	+	2 1mV	+	0 175mVrms]
Error as % of FSR	=	0 0005%	+	0 7%	+	0 5%	+	0 006%	+	0 021%	+	0 00175%
After Nulling												
$V_{E\,(ISO)}$	=	$\frac{1}{200}$ [0 05mV	+	0mV	+	0mV	+	6mV	+	2 1mV	+	0 175mVrms]
	=	$\frac{1}{200}$ (3 0mV)										
	=	0 03mV										
Error as % of FSR	=	0 0005%	+	0%	+	0%	+	0 006%	+	0 021%	+	0 00175%
	=	0 03% of 50mV										

Total Error	=	$V_{E\,(OPA)}$	+ $V_{E\,(ISO)}$
	=	0 10mV	+ 0 03mV
	=	0 08% of 50mV + 0 03% of 50mV	
	=	0 11% of 50mV	

FIGURE 20. Op Amp and Iso Amp Error Analysis.

BURR-BROWN®

ISO103
ISO107

ADVANCE INFORMATION
SUBJECT TO CHANGE

Low-Cost, High-Voltage, Internally Powered ISOLATION AMPLIFIER

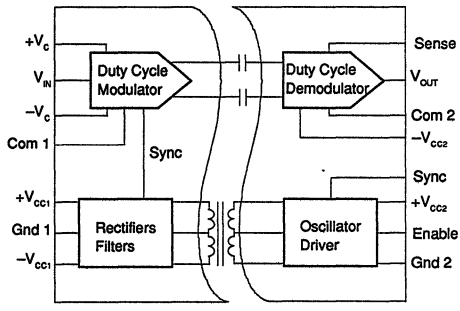
FEATURES

- **SIGNAL AND POWER IN ONE PACKAGE: Double-Wide ISO103, Triple-Wide ISO107**
- **CONTINUOUS AC BARRIER RATINGS: ISO103: 1500Vrms, ISO107: 2500Vrms**
- **WIDE INPUT SIGNAL RANGE: –10V to +10V**
- **WIDE BANDWIDTH: 30kHz Small Signal,10kHz Full Power**
- **BUILT-IN ISOLATED POWER: ±10V to ±18V Input, ±25mA Output**
- **MULTI-CHANNEL SYNCHRONIZATION CAPABILITY**

APPLICATIONS

- **MULTI-CHANNEL ISOLATED DATA ACQUISITION**
- **BIOMEDICAL INSTRUMENTATION**
- **POWER SUPPLY AND MOTOR CONTROL**
- **GROUND LOOP ELIMINATION**

ISO103/107 BLOCK DIAGRAM



DESCRIPTION

The ISO103 and ISO107 isolation amplifiers provide both signal and power across an isolation barrier. The products are differentiated by package size and barrier voltage rating. The ceramic side-brazed hybrid package contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel. A proprietary 800kHz oscillator chip, power MOSFET transformer drivers, patented square core wirebonded transformer, and single chip diode bridge provide power to the input side of the isolation amplifier as well as external loads up to ±25mA.

Extra features include short-circuit protection, soft start, multi-channel synchronization, ±10V to ±18V input supply range, and 1500Vrms (ISO103) or 2500Vrms (ISO107) isolation voltage rating.

The signal channel capacitively couples a duty cycle encoded signal across the ceramic high-voltage barrier built into the package. A proprietary transmitter/receiver pair of integrated circuits, laser trimmed at wafer level, are coupled through a pair of matched "fringe" capacitors. The result is a simple, reliable design that rejects common mode transients. The duty cycle modulator is synchronized to the DC/DC converter to eliminate beat frequency interference between the power converter and signal channel.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491 • FAX: (602) 889-1510

PDS-840

SPECIFICATIONS

ELECTRICAL

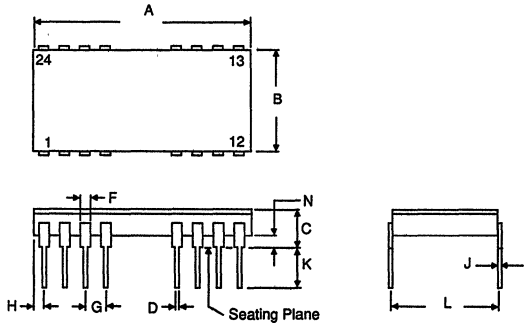
At T_A = +25°C and V_{CC2} = ±15V, ±15mA output current unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ISOLATION					
Rated Continuous Voltage					
ISO103 AC, 60Hz	T_{MIN} to T_{MAX}	1500			Vrms
DC	T_{MIN} to T_{MAX}	2121			VDC
ISO107 AC, 60Hz	T_{MIN} to T_{MAX}	2500			Vrms
DC	T_{MIN} to T_{MAX}	3500			VDC
Partial Discharge Test (1)					
ISO103	2400Vrms			5	pC
ISO107	4000Vrms			5	pC
Isolation-Mode Rejection	1500Vrms		100		dB
	2121VDC		160		dB
Barrier Impedance			10^{12} || 9		Ω || pF
Leakage Current	240Vrms		1		µA
GAIN					
Nominal			1		V/V
Initial Error			±0.1		% FSR
Gain vs Temperature			±20		ppm/°C
Nonlinearity			±0.01		% FSR
INPUT OFFSET VOLTAGE					
Initial Offset			20		mV
vs Temperature			100		µV/°C
vs Power Supplies	V_{CC2} = ±10V to ±18V		5		mV/V
INPUT					
Voltage Range			±10		V
Resistance			200		kΩ
SIGNAL OUTPUT					
Voltage Range			±10		V
Current Drive			±15		mA
Ripple Voltage			10		mVp-p
Capacitive Load Drive			1000		pF
Voltage Noise			4		µV/√Hz
FREQUENCY RESPONSE					
Small Signal Bandwidth			30		kHz
Slew Rate			1.5		V/µs
Settling Time	0.1%, –10/10V		50		µs
POWER SUPPLIES					
Rated Voltage, V_{CC2}			±15		V
Voltage Range		±10		±18	V
Input Current	I_O = ±15mA		+90/–3		mA
Ripple Current	No Filter		150		mAp-p
	C_{IN} = 1µF		60		mAp-p
	pi Filter		5		mAp-p
Rated Output Voltage			±15		V
Output Current	Balanced Load		±15		mA
	Single		30		mA
Load Regulation	Balanced Load		0.5		%/mA
Line Regulation			1.15		V/V
Output Voltage vs Temperature			10		mV/°C
Voltage Balance, $\pm V_{CC1}$			0.5		%
Voltage Ripple (800kHz)	No External Capacitors		60		mVp-p
Output Capacitive Load			1		µF
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–25		+85	°C
Storage		–25		+125	°C

NOTE: (1) Conforms to VDE0884 test methods. Tested at 1.6 x rated voltage; PD ≤ 5pC.

MECHANICAL

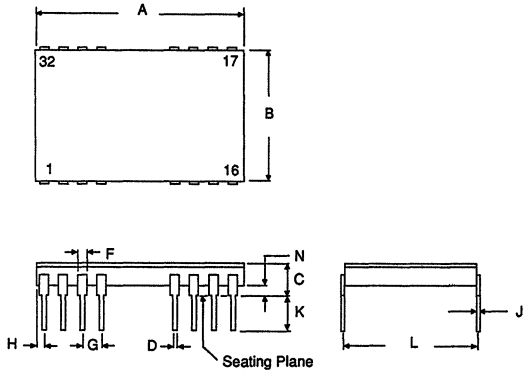
ISO103 — 24-Pin Double-Wide DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.180	1.220	29.97	30.99
B	.580	.600	14.73	15.24
C	.310	.370	7.87	9.40
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.600	.620	15.24	15.75
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ISO107 — 32-Pin Triple-Wide DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.310	.370	7.87	9.40
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.150	.185	3.81	4.70
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

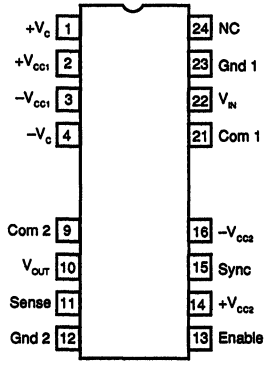
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ABSOLUTE MAXIMUM RATINGS

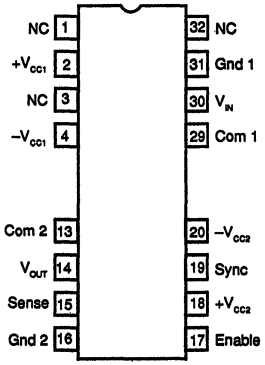
Supply Without Damage	±18V
V_{IN}, Sense Voltage	±50V
Signal Common to Gnd 2	±200mV
Enable, Sync	0V to +V_{CC2}
Continuous Isolation Voltage	
ISO103	1500Vrms
ISO107	2500Vrms
V_{ISO}, dv/dt	20kV/µs
Junction Temperature	150°C
Storage Temperature	–25°C to +125°C
Lead Temperature,10s	300°C
Output Short to Gnd 2 Duration	Continuous
±V_{CC1} to Gnd 1 Duration	Continuous

PIN CONFIGURATION

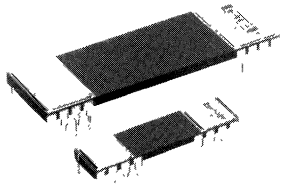
ISO103



ISO107



BURR-BROWN®



ISO108
ISO109

ADVANCE INFORMATION
SUBJECT TO CHANGE

Isolated
VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- ISOLATED VFC IN HERMETIC DIP
- HIGH-VOLTAGE AC RATINGS: ISO108: 1500Vrms, ISO109: 2500Vrms
- HIGH TRANSIENT IMMUNITY: 10kV/μs
- LOW BARRIER LEAKAGE CURRENT: 0.5μA
- HIGH LINEARITY AT HIGH FREQUENCY: 0.01% at 1MHz
- VOLTAGE REFERENCE OUTPUT: 5VDC
- MULTIPLEXED OUTPUT CAPABILITY

APPLICATIONS

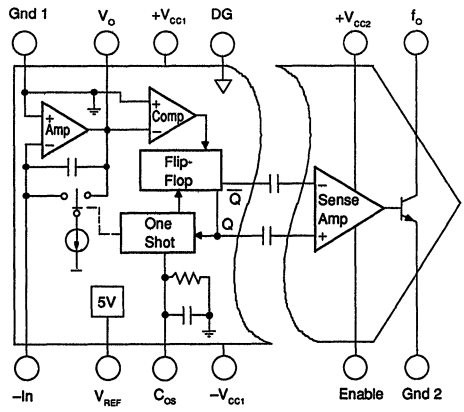
- ISOLATED A/D CONVERTER
- BIOMEDICAL DATA ACQUISITION
- PROCESS CONTROL
- INDUSTRIAL DATA ACQUISITION

DESCRIPTION

The ISO108 and ISO109 provide a high-speed VFC and isolated coupler in one hermetic DIP package. This represents a new function for diverse applications benefiting from A/D conversion with ground breaking.

The input VFC transmits a differential digital signal across the isolation barrier through matched 1pF ceramic capacitors built into the 24-pin single-wide (ISO108) and 40-pin double-wide (ISO109) packages. Excellent transient immunity is provided by the small barrier capacitor matching, patented sense amp design, and laser trimming.

Extra features include a voltage reference useful for offsetting and calibration, and a TTL-compatible enable input that provides for multiplexing multiple VFC outputs.



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PDS-841

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC1} = \pm 15V$, $V_{CC2} = 5V$ unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ISOLATION					
Rated Continuous Voltage					
ISO108: AC, 60Hz	T_{MIN} to T_{MAX}	1500			Vrms
DC	T_{MIN} to T_{MAX}	2121			VDC
ISO109: AC, 60Hz	T_{MIN} to T_{MAX}	2500			Vrms
DC	T_{MIN} to T_{MAX}	3500			VDC
Partial Discharge Test[1]					
ISO108	2400Vrms			5	pC
ISO109	4000Vrms			5	pC
Transient Immunity			10		kV/µs
Barrier Impedance			$10^{12} \parallel 3$		Ω || pF
Leakage Current	240Vrms		0.3		µA
TRANSFER FUNCTION					
Voltage-to-Frequency Mode					
Gain Error	1MHz		5		%
Linearity Error	FSR = 1MHz		0.01		%
Gain Drift	FSR = 1MHz		50		ppm/°C
PSRR			0.1		%/V
Input Current Range[2]	0 - FS Output	>0		250	µA
INTEGRATOR OP AMP					
V_{OS}			3		mV
V_{OS} Drift			30		µV/°C
I_B			50		nA
OPEN COLLECTOR OUTPUT					
V_{OL}	I_{OUT} = 10mA		0.4		V
I_{OH}	V_{OH} = 20V		0.1		µA
Fall Time			50		ns
REFERENCE VOLTAGE					
Accuracy		4.95	5.00	5.05	V
Drift			50		ppm/°C
Current Output			20		mA
PSRR			75		ppm/V
Output Impedance			1		Ω
POWER SUPPLY					
Voltage Range	$\pm V_{CC1}$	±8		±20	V
	$+V_{CC2}$	4.5		20	V
Quiescent Current	$\pm V_{CC1}$		+17/–15		mA
	$+V_{CC2}$		+12		mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–55		+125	°C
Storage		–65		+150	°C

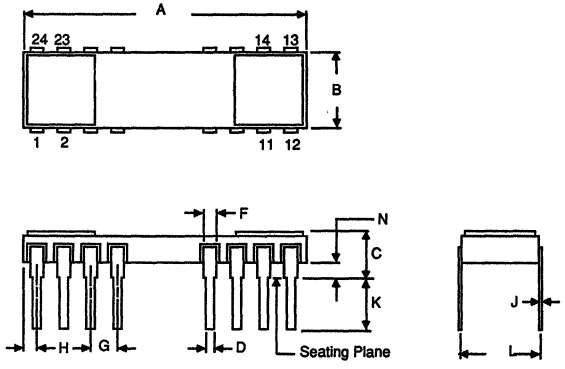
NOTES; (1) Conforms to VDE884 test methods. Tested at 1.6 x rated voltage; PD ≤ 5pC. (2) $V_{IN} = I_{IN} \times R_{IN}$.

ABSOLUTE MAXIMUM RATINGS

Supply Without Damage	±20V
–In, C_{OS}	$\pm V_{CC1}$
Enable	Gnd 2/V_{CC2}
V_{REF}, V_O to Gnd 1	Continuous
f_O Sink Current	50mA
Continuous Isolation Voltage	
ISO108	1500Vrms
ISO109	2500Vrms
Junction Temperature	+150°C
Storage Temperature	–65°C to +150°C
Lead Temperature, 10s	+300°C

MECHANICAL

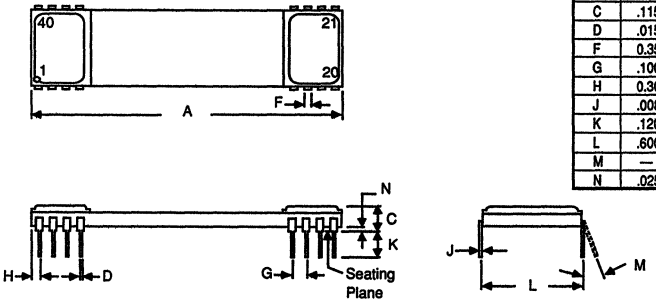
ISO108 — 24-Pin Single-Wide Hermetic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.190	1.210	30.23	30.73
B	.280	.300	7.11	7.62
C	.140	.185	3.56	4.70
D	.016	.020	0.41	0.51
F	.030	0.50	0.76	1.27
G	.100 BASIC		2.54 BASIC	
H	.035	.065	0.89	1.65
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.300 BASIC		7.62 BASIC	
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

ISO109 — 40-Pin Double-Wide Hermetic DIP

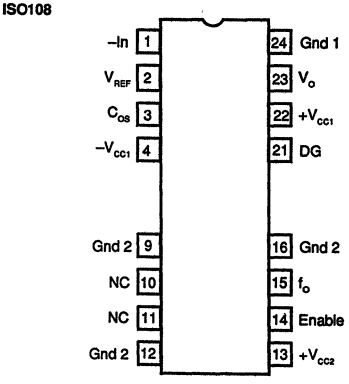


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.980	2.020	50.29	51.31
C	.115	.175	2.92	4.45
D	.015	.021	0.38	0.53
F	0.35	0.60	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	0.30	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

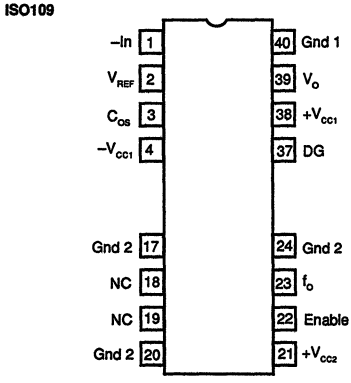
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

PIN CONFIGURATION

ISO108



ISO109



BURR-BROWN®

ISO113

ADVANCE INFORMATION
SUBJECT TO CHANGE

Low-Cost, High-Voltage, Internally Powered OUTPUT ISOLATION AMPLIFIER

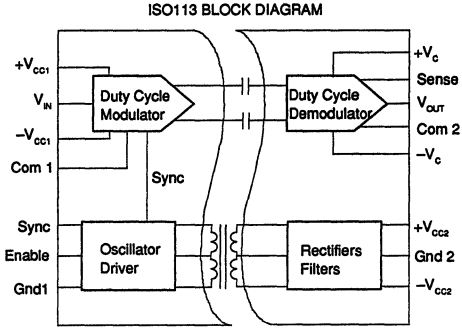
FEATURES

- SELF-CONTAINED ISOLATED SIGNAL AND OUTPUT POWER
- SMALL PACKAGE SIZE: Double-Wide DIP
- CONTINUOUS AC BARRIER RATING: 1500Vrms
- WIDE BANDWIDTH: 30kHz Small Signal,10kHz Full Power
- BUILT-IN ISOLATED OUTPUT POWER: ±10V to ±18V Input, ±25mA Output
- MULTICHANNEL SYNCHRONIZATION CAPABILITY

APPLICATIONS

- 4mA TO 20mA V/I CONVERTERS
- MOTOR AND VALVE CONTROLLERS
- ISOLATED RECORDER OUTPUTS
- MEDICAL INSTRUMENTATION OUTPUTS
- GAS ANALYZERS

ISO113 BLOCK DIAGRAM



DESCRIPTION

The ISO113 output isolation amplifier provides both signal and output power across an isolation barrier in a small double-wide DIP package. The ceramic side-brazed hybrid package contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel. A proprietary 800kHz oscillator chip, power MOSFET transformer drivers, patented square core wirebonded transformer, and a single chip diode bridge provide power to the output side of the isolation amplifier as well as external loads up to ±25mA.

Extra features include enable, soft start, short circuit protection, multiple channel synchronization, ±10V to ±18V supply range, and 1500Vrms isolation voltage rating. The signal channel capacitively couples a duty-cycle encoded signal across the ceramic high-voltage barrier built into the package. A proprietary transmitter/receiver pair of integrated circuits, laser trimmed at wafer level, are coupled through a pair of matched "fringe" capacitors. The result is a simple, reliable design that rejects common-mode transients. The duty cycle modulator is synchronized to the DC/DC converter to eliminate beat frequency interference between the power converter and signal channel.

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PDS-844

SPECIFICATIONS

ELECTRICAL

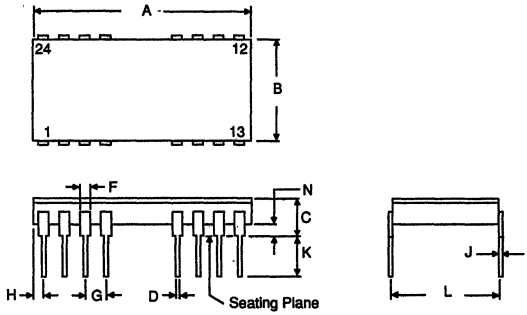
At T_A = +25°C and V_{CC1} = ±15V, Supply Output Load = ±15mA unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ISOLATION					
Rated Continuous Voltage					
AC, 60Hz	T_{MIN} to T_{MAX}	1500			Vrms
DC	T_{MIN} to T_{MAX}	2121			VDC
Partial Discharge Test [1]					
	2400Vrms			5	pC
Isolation-Mode Rejection	1500Vrms		100		dB
	2121VDC		160		dB
Barrier Impedance			10^{12} || 9		Ω || pF
Leakage Current	240Vrms		1		µA
GAIN					
Nominal			1		V/V
Initial Error			±0.1		% FSR
Gain vs Temperature			±20		ppm/°C
Nonlinearity			±0.01		% FSR
INPUT OFFSET VOLTAGE					
Initial Offset			20		mV
vs Temperature			100		µV/°C
vs Power Supplies	V_{CC1} = ±10 to ±18V		5		mV/V
INPUT					
Voltage Range			±10		V
Resistance			200		kΩ
SIGNAL OUTPUT					
Voltage Range			±10		V
Current Drive			±15		mA
Ripple Voltage			10		mVp-p
Capacitive Load Drive			1000		pF
Voltage Noise			4		µV/√Hz
FREQUENCY RESPONSE					
Small Signal Bandwidth			30		kHz
Slew Rate			1.5		V/µs
Settling Time	0.1%, −10/10V		50		µs
POWER SUPPLIES					
Rated Voltage, V_{CC1}			±15		V
Voltage Range		±10		±18	V
Input Current	I_O = ±15mA		+90/−3		mA
Ripple Current	No Filter		150		mAp-p
	C_{IN} = 1µF		60		mAp-p
	pi Filter		5		mAp-p
Rated Output Voltage			±15		V
Output Current	Balanced Load		±15		mA
	Single		30		mA
Load Regulation	Balanced Load		0.5		%/mA
Line Regulation			1.15		V/V
Output Voltage vs Temperature			10		mV/°C
Voltage Balance, ±V_{CC2}			0.5		%
Voltage Ripple (800KHz)	No External Capacitors		60		mVpp
Output Capacitive Load			1		µF
TEMPERATURE RANGE					
Specification		−25		+85	°C
Operating		−25		+85	°C
Storage		−25		+125	°C

NOTE: (1) Conforms to VDE0884 test methods.

MECHANICAL

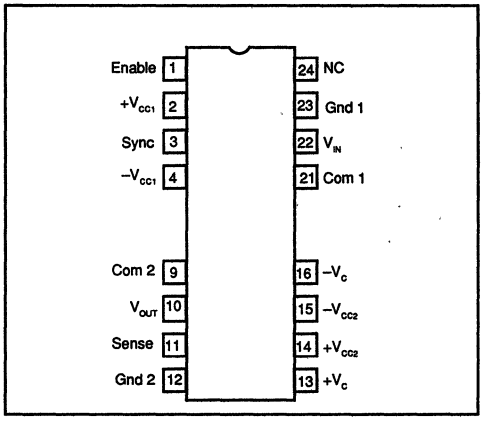
ISO113—24-Pin Double-Wide DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.180	1.220	29.97	30.99
B	.580	.600	14.73	15.24
C	.310	.370	7.87	9.40
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.600	.620	15.24	15.75
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

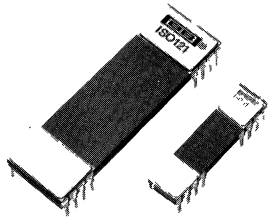
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Without Damage	±18V
V_{IN}, Sense Voltage	±50V
Com to Gnd (either input or output)	±200mV
Enable, Sync	Gnd to +V_{CC1}
Continuous Isolation Voltage	1500Vrms
V_{ISO}, dv/dt	20kV/µs
Junction Temperature	+150°C
Storage Temperature	–25°C to +125°C
Lead Temperature,10s	+300°C
Output Short to Gnd Duration	Continuous
±V_{CC2} to Gnd 2 Duration	Continuous

BURR-BROWN®



ISO120
ISO121

Precision Low Cost
ISOLATION AMPLIFIER

FEATURES

- 100% TESTED FOR PARTIAL DISCHARGE
- ISO120: Rated 1500Vrms
- ISO121: Rated 3500Vrms
- HIGH IMR: 115dB at 60Hz
- USER CONTROL OF CARRIER FREQUENCY
- LOW NONLINEARITY: ±0.01% max
- BIPOLAR OPERATION: $V_O = \pm 10V$
- 0.3"-WIDE 24-PIN HERMETIC DIP, ISO120
- SYNCHRONIZATION CAPABILITY

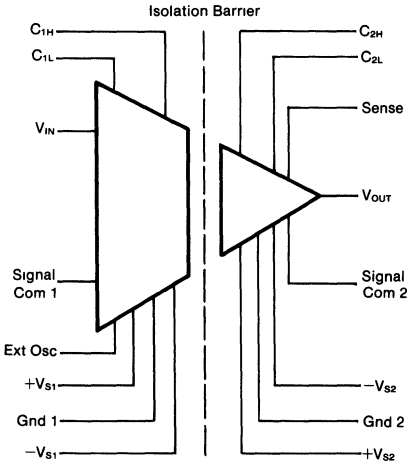
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL: Transducer Isolator for Thermocouples, RTDs, Pressure Bridges, and Flow Meters. 4mA to 20mA Loop Isolation
- GROUND LOOP ELIMINATION
- MOTOR AND SCR CONTROL
- POWER MONITORING
- ANALYTICAL MEASUREMENTS
- BIOMEDICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT

DESCRIPTION

The ISO120 and ISO121 are precision isolation amplifiers incorporating a novel duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2pF differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity, which results in excellent reliability and good high frequency transient immunity across the barrier. Both the amplifier and barrier capacitors are housed in a hermetic DIP. The ISO120 and ISO121 differ only in package size and isolation voltage rating.

These amplifiers are easy to use. No external components are required for 60kHz bandwidth. With the addition of two external capacitors, precision specifications of 0.01% max nonlinearity and 150μV/°C max V_{OS} drift are guaranteed with 6kHz bandwidth. A power supply range of ±4.5V to ±18V and low quiescent current make these amplifiers ideal for a wide range of applications.



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PDS-820C

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C. $V_{S1} = V_{S2} = \pm 15V$: and $R_L = 2k\Omega$ unless otherwise noted.

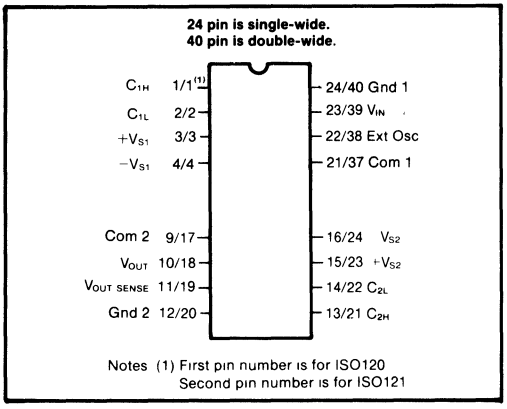
PARAMETER	CONDITIONS	ISO120BG, ISO121BG			ISO120G, ISO121G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ISOLATION								
Voltage Rated Continuous ISO120 AC 60Hz	T_{MIN} to T_{MAX}	1500			1500			Vrms
DC	T_{MIN} to T_{MAX}	2121			2121			VDC
ISO121: AC 60Hz	T_{MIN} to T_{MAX}	3500			3500			Vrms
DC	T_{MIN} to T_{MAX}	4950			4950			VDC
100% Test (AC 60Hz): ISO120	1s; Partial discharge ≤ 5pC	2500			2500			Vrms
ISO121	1s, Partial discharge ≤ 5pC	5600			5600			Vrms
Isolation Mode Rejection ISO120: AC 60Hz	1500Vrms		115			115		dB
DC			160			160		dB
ISO121 AC 60Hz	3500Vrms		115			115		dB
DC			160			160		dB
Barrier Impedance			10^{14}//2			10^{14}//2		Ω//pF
Leakage Current	V_{ISO} = 240Vrms, 60Hz		0 18	0 5		0 18	0 5	μArms
GAIN	$V_O = \pm 10V$							
Nominal Gain	$C_1 = C_2$ = 1000pF		1			1		V/V
Gain Error			±0 04	±0 1		±0 05	±0.25	% FSR
Gain vs Temperature			±5	±20		±10	±40	ppm/°C
Nonlinearity			±0 005	±0.01		±0.01	±0.05	% FSR
Nominal Gain	$C_1 = C_2 = 0$		1			1		V/V
Gain Error			±0.04	±0 25		±0.05	±0 25	% FSR
Gain vs Temperature			±40			±40		ppm/°C
Nonlinearity			±0.02	±0 1		±0.04	±0 1	% FSR
INPUT OFFSET VOLTAGE								
Initial Offset	$C_1 = C_2$ = 1000pF		±5	±25		±10	±50	mV
vs Temperature			±100	±150		±150	±400	μV/°C
Initial Offset	$C_1 = C_2 = 0$		±25	±100		±40	±100	mV
vs. Temperature			±250			±500		μV/°C
Initial Offset								
vs Supply	$\pm V_{S1}$ or $\pm V_{S2} = \pm 4$ 5V to ±18V		±2			±2		mV/V
Noise			4			4		μV/√Hz
INPUT								
Voltage Range[1]		±10	±15		±10	±15		V
Resistance			200			200		kΩ
OUTPUT								
Voltage Range		±10	±12.5		±10	±12.5		V
Current Drive		±5	±20		±5	±20		mA
Capacitive Load Drive			0.1			0.1		μF
Ripple Voltage[2]			10			10		mVp-p
FREQUENCY RESPONSE								
Small Signal Bandwidth	$C_1 = C_2 = 0$		60			60		kHz
	$C_1 = C_2$ = 1000pF		6			6		kHz
Slew Rate			2			2		V/μs
Settling Time	$V_O = \pm 10V$							
0.1%	C_2 = 100pF		50			50		μs
0 01%	$C_1 = C_2$ = 1000pF		350			350		μs
Overload Recovery Time[3]	50% Output Overload, $C_1 = C_2 = 0$		150			150		μs
POWER SUPPLIES								
Rated Voltage			15			15		V
Voltage Range		±4 5		±18	±4.5		±18	V
Quiescent Current: V_{S1}			±4.0	±5.5		±4.0	±5.5	mA
V_{S2}			±5.0	±6.5		±5.0	±6.5	mA
TEMPERATURE RANGE								
Specification		−25		85	−25		85	°C
Operating		−55		125	−55		125	°C
Storage		−65		150	−55		150	°C
θ_{JA}: ISO120			40			40		°C/W
ISO121			25			25		°C/W

NOTES: (1) Input voltage range = ±10V for V_{S1}, V_{S2} = ±4.5VDC to ±18VDC. (2) Ripple frequency is at carrier frequency. (3) Overload recovery is approximately three times the settling time for other values of C_2.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Between Supplies +V_{SS} to −V_{SS}) 36V	Continuous Isolation Voltage: ISO121 ..... 3500Vrms
V_{IN}, Sense Voltage ..... ±100V	V_{ISO}, dv/dt 20kv/μs
External Oscillator Input ..... ±25V	Junction Temperature ..... 150°C
Signal Common 1 to Ground 1 ..... ±1V	Storage Temperature ..... −65°C to +150°C
Signal Common 2 to Ground 2 ..... ±1V	Lead Temperature (soldering, 10s) ..... +300°C
Continuous Isolation Voltage: ISO120 ..... 1500Vrms	Output Short Duration ..... Continuous to Common

CONNECTION DIAGRAM



Notes (1) First pin number is for ISO120
Second pin number is for ISO121

ORDERING INFORMATION

Model	Package	Temperature Range
ISO120G	Cer. Her. DIP	-25°C to +85°C
ISO120BG	Cer. Her. DIP	-25°C to +85°C
ISO121G	Cer. Her. DIP	-25°C to +85°C
ISO121BG	Cer. Her. DIP	-25°C to +85°C

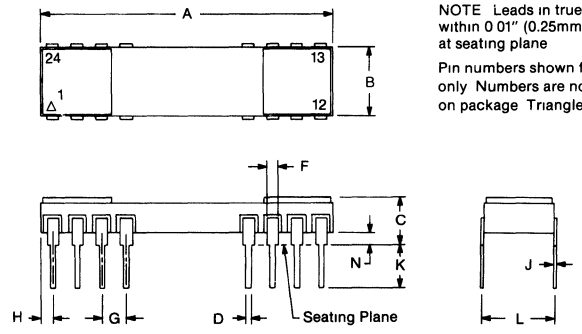
BURN-IN SCREENING OPTION
See text for details.

Model	Package	Burn-In Temp. (160h)(1)
ISO120G-BI	Cer. Her. DIP	+125°C
ISO120BG-BI	Cer Her DIP	+125°C
ISO121G-BI	Cer Her DIP	+125°C
ISO121BG-BI	Cer. Her. DIP	+125°C

NOTE: (1) Or equivalent combination. See text

MECHANICAL

ISO120 24-Pin Ceramic DIP

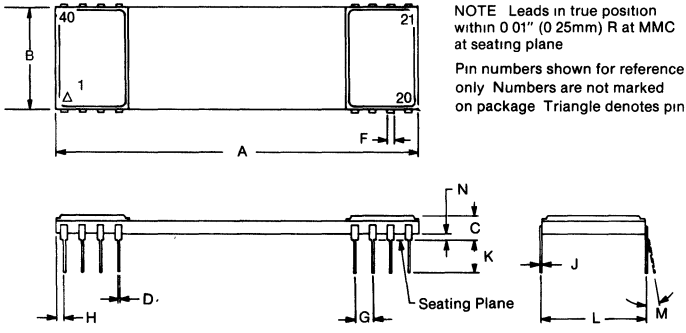


NOTE Leads in true position within 0 01" (0.25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers are not marked on package Triangle denotes pin 1

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 190	1 210	30 23	30 73
B	280	300	7 11	7 62
C	140	185	3 56	4 70
D	016	020	0 41	0 51
F	030	050	0 76	1 27
G	100 BASIC		2 54 BASIC	
H	035	065	0 89	1 65
J	009	012	0.23	0 30
K	165	185	4 19	4 70
K	300 BASIC		7 62 BASIC	
L	040	060	1 02	1 52

ISO121 40-Pin Ceramic DIP



NOTE Leads in true position within 0 01" (0 25mm) R at MMC at seating plane

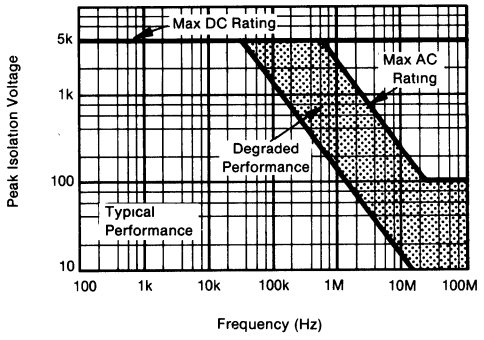
Pin numbers shown for reference only Numbers are not marked on package Triangle denotes pin 1

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 980	2 020	50 29	51 31
B	580	600	14 73	15 24
C	140	185	3 56	4 70
D	015	021	0 38	0 53
F	030	060	0 76	1 52
G	100 BASIC		2 54 BASIC	
H	030	070	0 76	1 78
J	008	012	0 20	0 30
K	120	240	3 05	6 10
L	600 BASIC		15 24 BASIC	
M	—	10°	—	10°
N	025	060	0 64	1 52

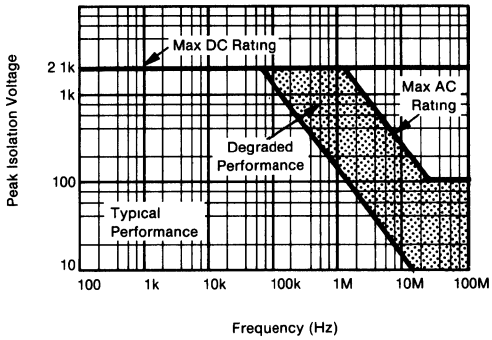
TYPICAL PERFORMANCE CURVES

At $T_A = +25°C$, $V_{S1} = V_{S2} = \pm 15V$, and $R_L = 2k\Omega$ unless otherwise noted.

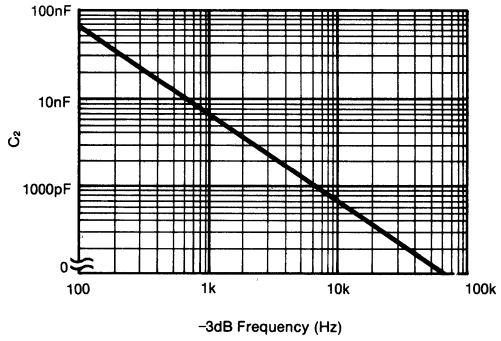
ISOLATION MODE VOLTAGE vs FREQUENCY ISO121



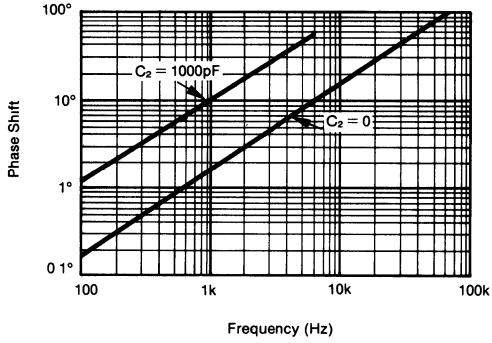
ISOLATION MODE VOLTAGE vs FREQUENCY ISO120



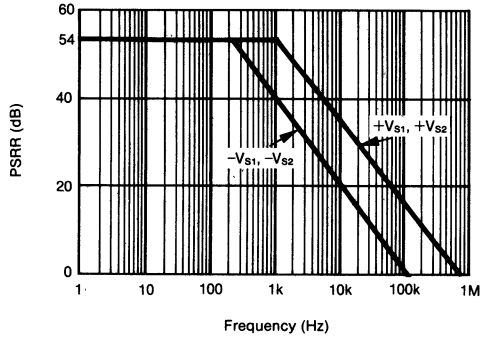
BANDWIDTH vs C_2



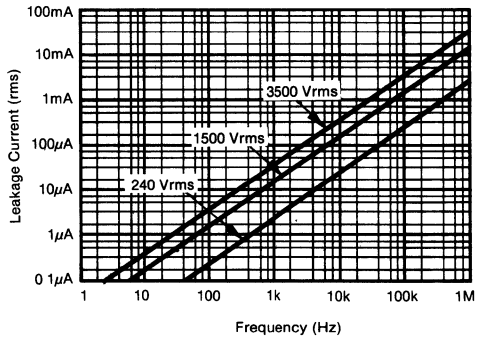
PHASE SHIFT vs C_2



PSRR vs FREQUENCY



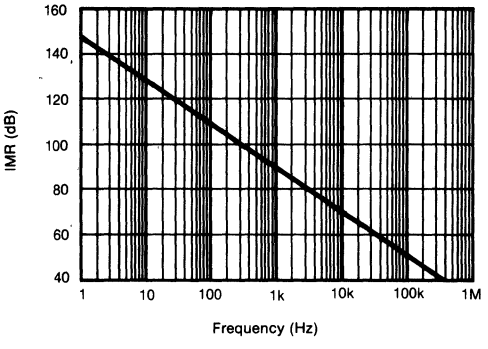
ISOLATION LEAKAGE CURRENT vs FREQUENCY



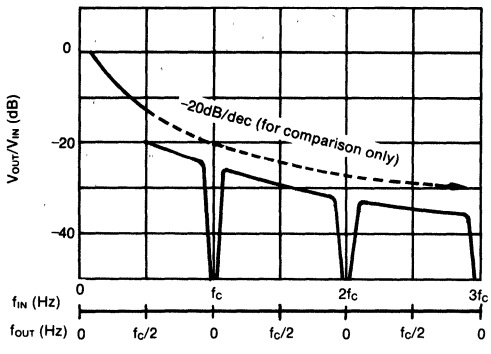
TYPICAL PERFORMANCE CURVES

At $T_A = +25°C$; $V_{S1} = V_{S2} = \pm 15V$; and $R_L = 2k\Omega$ unless otherwise noted.

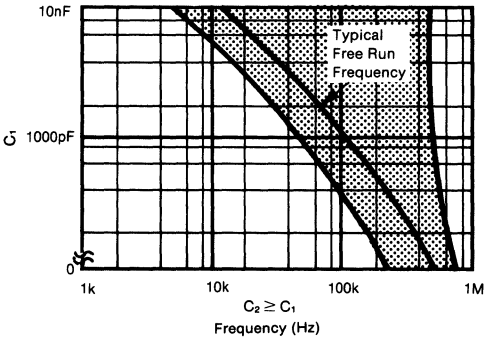
IMR vs FREQUENCY



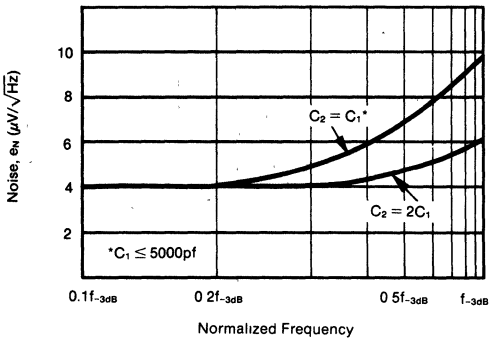
SIGNAL RESPONSE vs CARRIER FREQUENCY



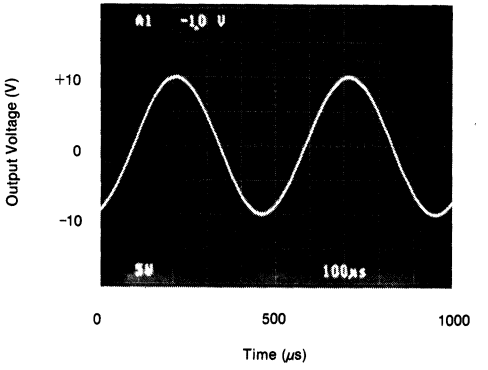
SYNCHRONIZATION RANGE @ 25°C
±4Vp SINE WAVE INPUT TO EXT OSC



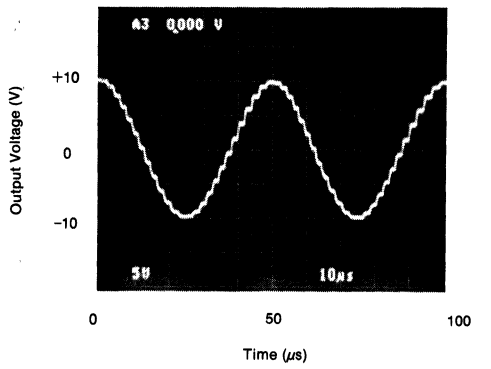
NOISE vs SMALL SIGNAL BANDWIDTH



SINE RESPONSE
(f = 2kHz, $C_2 = 0$)



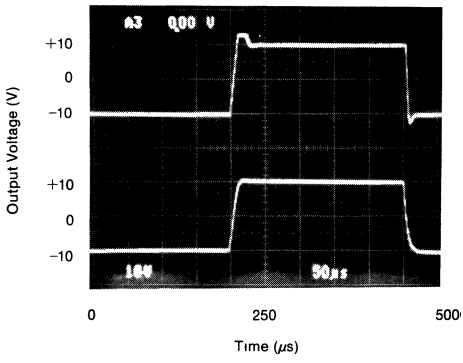
SINE RESPONSE
(f = 20kHz, $C_2 = 0$)



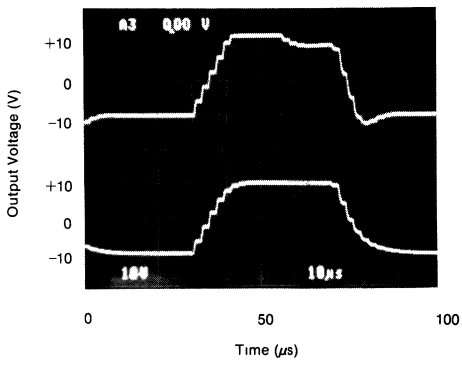
TYPICAL PERFORMANCE CURVES

At T_A = +25°C; V_{S1} = V_{S2} = ±15V; and R_L = 2kΩ unless otherwise noted

STEP RESPONSE



STEP RESPONSE



THEORY OF OPERATION

The ISO120 and ISO121 isolation amplifiers comprise input and output sections galvanically isolated by matched 1pF capacitors built into the ceramic barrier. The input is duty-cycle modulated and transmitted digitally across the barrier. The output section receives the modulated signal, converts it back to an analog voltage and removes the ripple component inherent in the demodulation. The input and output sections are fabricated together on a single wafer and laser-trimmed as a complete system for exceptional matching of circuitry common to both input and output sections.

FREE-RUNNING MODE

An input amplifier (A1, Figure 1) integrates the difference between the input current (V_{IN}/200kΩ) and a switched ±100μA current source. This current source is implemented by a switchable 200μA source and a fixed 100μA current sink. To understand the basic operation of the input section, assume that V_{IN} = 0. The integrator will ramp in one direction until the comparator threshold is exceeded. The comparator and sense amp will force the current source to switch; the resultant signal is a trianglar waveform with a 50% duty cycle. If V_{IN} changes, the duty cycle of the integrator will change to keep the average DC value at the output of A1 near zero volts. This action converts the input voltage to a duty-cycle modulated triangular waveform at the output of A1 with a frequency determined by the internal 150pF capacitor. The comparator generates a fast rise time square wave that is simultaneously fed back to keep A1 in charge balance and also across the barrier to a differential sense amplifier with high common-mode rejection characteristics. The sense amplifier drives a switched current source surrounding A2. The output stage balances the duty-cycle modulated current against the feedback current through the 200kΩ feedback resistor, resulting in an average value at the Sense pin equal to V_{IN}. The sample and hold amplifiers in the output feedback loop serve to remove undesired ripple voltages inherent in the demodulation process.

SYNCHRONIZED MODE

A unique feature of the ISO120 and ISO121 is the ability to synchronize the modulator to an external signal source. This capability is useful in eliminating troublesome beat frequencies in multi-channel systems and in rejecting AC signals and their harmonics. To use this feature, external capacitors are connected at C_1 and C_2 (Figure 1) to change the free-running carrier frequency. An external signal is applied to the Ext Osc pin. This signal forces the current source to switch at the frequency of the external signal. If V_{IN} is zero, and the external source has a 50% duty cycle, operation procedes as described above, except that the switching frequency is that of the external source. If the external signal has a duty cycle other than 50%, its average value is not zero. At startup, the current source does not switch until the integrator establishes an output equal to the average DC value of the external signal. At this point, the external signal is able to trigger the current source, producing a triangular waveform, symmetrical about the new DC value, at the output of A1. For V_{IN} = 0, this waveform has a 50% duty cycle. As V_{IN} varies, the waveform retains its DC offset, but varies in duty cycle to maintain charge balance around A1. Operation of the demodulator is the same as outlined above.

BASIC OPERATION

Signal and Power Connections

Figure 2 shows proper power and signal connections. Each power supply pin should be bypassed with a 1μF

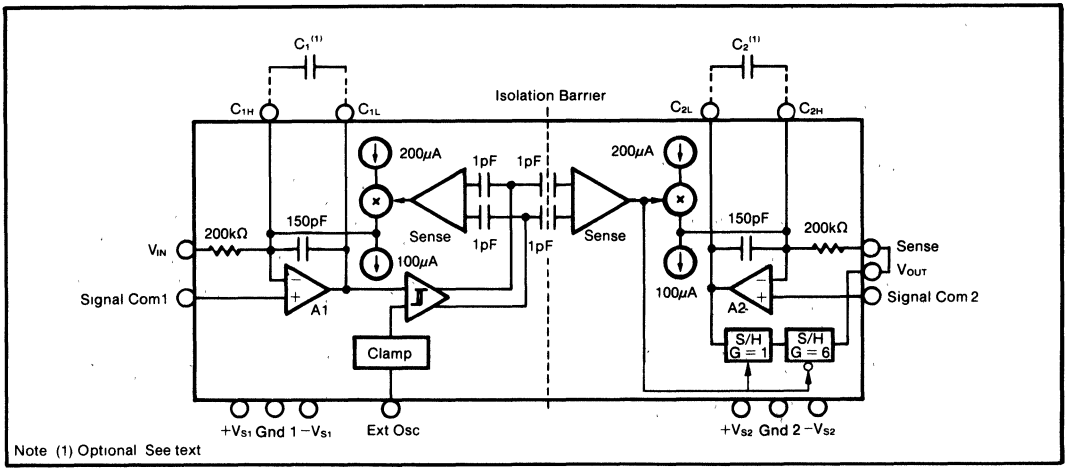


FIGURE 1. Block Diagram.

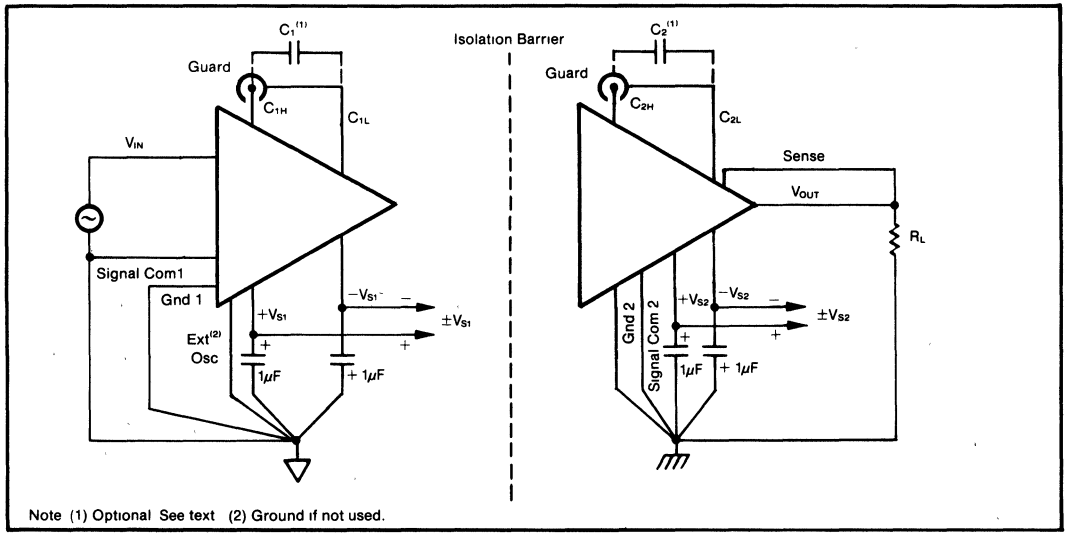


FIGURE 2. Power and Signal Connections.

tantalum capacitor located as close to the amplifier as possible. All ground connections should be run independently to a common point if possible. Signal Common on both input and output sections provide a high-impedance point for sensing signal ground in noisy applications. Signal Common must have a path to ground for bias current return and should be maintained within ±1V of Gnd. The ouptut sense pin may be connected directly to V_{OUT} or may be connected to a remote load to eliminate errors due to IR drops. Pins are provided for use of external integrator capacitors. The C_{1H} and C_{2H} pins are connected to the integrator summing junctions and are therefore particularly sensitive to external pickup. This sensitivity will most often appear as degraded IMR or PSR performance. AC or DC currents coupled into these pins results in $V_{ERROR} = I_{ERROR} \times 200k\Omega$ at the output. Guarding of these pins to their respective Signal Common, or C_{1L} and C_{2L} is strongly recommended. For similar reasons, long traces or physically large capacitors are not desirable. If wound-foil capacitors are used, the outside foil should be connected to C_{1L} and C_{2L}, respectively.

Optional Gain and Offset Adjustments

Rated gain accuracy and offset performance can be achieved with no external adjustments, but the circuit of Figure 3a may be used to provide a gain trim of ±0.5% for the values shown; greater range may be provided by increasing the size of R_1 and R_2. Every 2kΩ increase in R_1 will give an additional 1% adjustment range, with $R_2 \geq 2R_1$. If safety or convenience dictates location of the

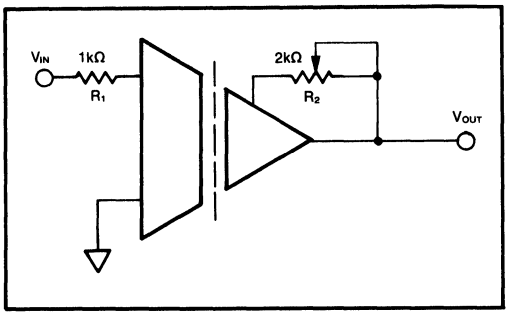


FIGURE 3a. Gain Adjust.

adjustment potentiometer on the other side of the barrier from the position shown in Figure 3a, the positions of R_1 and R_2 may be reversed. Gains greater than one may be obtained by using the circuit of Figure 3b. Note that the effect of input offset errors will be multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in inverse proportion to the increase in gain. In most instances, a precision gain block at the input of the isolation amplifier will provide better overall performance.

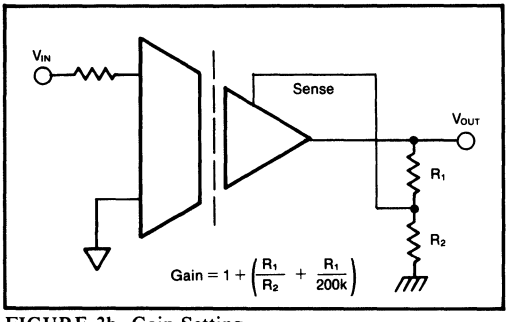


FIGURE 3b. Gain Setting.

Figure 4 shows a method for trimming V_{OS} of the ISO120 and ISO121. This circuit may be applied to either Signal Com (input or output) as desired for safety or convenience. With the values shown, ±15V supplies and unity gain, the circuit will provide ±150mV adjustment range and 0.25mV resolution with a typical trim potentiometer. The output will have some sensitivity to

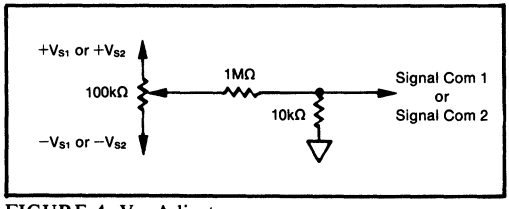


FIGURE 4. V_{OS} Adjust.

power supply variations. For a ±100mV trim, power supply sensitivity is 8mV/V at the output.

Carrier Frequency Considerations

As previously discussed, the ISO120 and ISO121 amplifiers transmit the signal across the iso-barrier by a duty-cycle modulation technique. This system works like any linear amplifier for input signals having frequencies below one half the carrier frequency, f_C. For signal frequencies above $f_C/2$, the behavior becomes more complex. The Signal Response vs Carrier Frequency performance curve describes this behavior graphically. The upper curve illustrates the response for input signals varying from DC to $f_C/2$. At input frequencies at or above $f_C/2$, the device generates an output signal component that varies in both amplitude and frequency, as shown by the lower curve. The lower horizontal scale shows the periodic variation in the frequency of the output component. Note that at the carrier frequency and its harmonics, both the frequency and amplitude of the response go to zero. These characteristics can be exploited in certain applications. It should be noted that when C_1 is zero, the carrier frequency is nominally 500kHz and the −3dB point of the amplifier is 60kHz. Spurious signals at the output are not significant under these circumstances unless the input signal contains significant components above 250kHz.

There are two ways to use these characteristics. One is to move the carrier frequency low enough that the troublesome signal components are attenuated to an acceptable level as shown in Signal Response vs Carrier Frequency. This in effect limits the bandwidth of the amplifier. The Synchronization Range performance curve shows the relationship between carrier frequency and the value of C_1. To maintain stability, C_2 must also be connected and must be equal to or larger in value than C_1. C_2 may be further increased in value for additional attentuation of the undesired signal components and provides the additional benefit of reducing the residual carrier ripple at the output. See the Bandwidth vs C_2 performance curve.

When periodic noise from external sources such as system clocks and DC/DC converters are a problem, ISO120 and ISO121 can be used to reject this noise. The amplifier can be synchronized to an external frequency source, f_{EXT}, placing the amplifier response curve at one of the frequency and amplitude nulls indicated in the Signal Response vs Carrier Frequency performance curve. For proper synchronization, choose C_1 as shown in the Synchronization Range performance curve. Remember that $C_2 \geq C_1$ is a necessary condition for stability of the isolation amplifier. This curve shows the range of lock at the fundamental frequency for a 4V sinusoidal signal source. The applications section shows the ISO120 and ISO121 synchronized to isolation power supplies, while Figure 5 shows circuitry with opto-isolation suitable for driving the Ext Osc input from TTL levels.

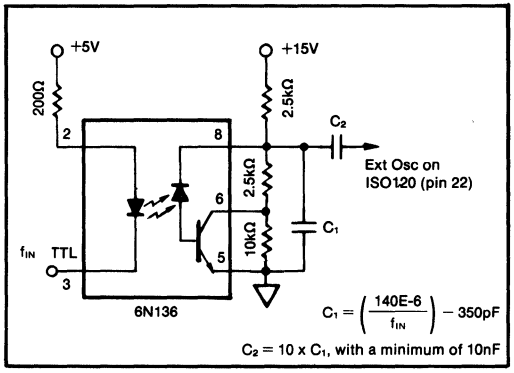


FIGURE 5. Synchronization with Isolated Drive Circuit for Ext Osc Pin.

ISOLATION MODE VOLTAGE

Isolation mode voltage (IMV) is the voltage appearing between isolated grounds Gnd 1 and Gnd 2. IMV can induce error at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds $f_C/2$, the output will display spurious outputs in a manner similar to that described above, and the amplifier response will be identical to that shown in the Signal Response vs Carrier Frequency performance curve. This occurs because IMV-induced errors behave like input-referred error signals. To predict the total IMR, divide the isolation voltage by the IMR shown in IMR vs Frequency performance curve and compute the amplifier response to this input-referred error signal from the data given in the Signal Response vs Carrier Frequency performance curve. Due to effects of very high-frequency signals, typical IMV performance can be achieved only when dV/dT of the isolation mode voltage falls below 1000V/μs. For convenience, this is plotted in the typical performance curves for the ISO120 and ISO121 as a function of voltage and frequency for sinusoidal voltages. When dV/dT exceeds 1000V/μs but falls below 20kV/μs, performance may be degraded. At rates of change above 20kV/μs, the amplifier may be damaged, but the barrier retains its full integrity. Lowering the power supply voltages below ±15V may decrease the dV/dT to 500V/μs for typical performance, but the maximum dV/dT of 20kV/μs remains unchanged.

Leakage current is determined solely by the impedance of the 2pF barrier capacitance and is plotted in the Isolation Leakage Current vs Frequency curve.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter time. The relationship between actual test voltage and the continuous derated maximum specification is an important one. Historically, Burr-Brown has chosen a deliberately conservative one: V_{TEST} = (2xACrms continuous rating) + 1000V for 10 seconds, followed by a test at rated ACrms voltage for one minute. This choice was appropriate for conditions where system transients are not well defined.

Recent improvements in high-voltage stress testing have produced a more meaningful test for determining maximum permissible voltage ratings, and Burr-Brown has chosen to apply this new technology in the manufacture and testing of the ISO120 and ISO121.

Partial Discharge

When an insulation defect such as a void occurs within an insulation system, the defect will display localized corona or ionization during exposure to high-voltage stress. This ionization requires a higher applied voltage to start the discharge and a lower voltage to maintain it or extinguish it once started. The higher start voltage is known as the inception voltage, while the extinction voltage is that level of voltage stress at which the discharge ceases. Just as the total insulation system has an inception voltage, so do the individual voids. A voltage will build up across a void until its inception voltage is reached, at which point the void will ionize, effectively shorting itself out. This action redistributes electrical charge within the dielectric and is known as partial discharge. If, as is the case with AC, the applied voltage gradient across the device continues to rise, another partial discharge cycle begins. The importance of this phenomenon is that, if the discharge does not occur, the insulation system retains its integrity. If the discharge begins, and is allowed to continue, the action of the ions and electrons within the defect will eventually degrade any organic insulation system in which they occur. The measurement of partial discharge is still useful in rating the devices and providing quality control of the manufacturing process. Since the ISO120 and ISO121 do not use organic insulation, partial discharge is non-destructive.

The inception voltage for these voids tends to be constant, so that the measurement of *total charge* being redistributed within the dielectric is a very good indicator of the size of the voids and *their likelihood of becoming an incipient failure.* The *bulk inception voltage,* on the other hand, varies with the insulation system, and the number of ionization defects and directly establishes the *absolute maximum voltage* (transient) that can be applied across the test device before destructive partial discharge can begin. Measuring the *bulk extinction voltage* provides a lower, more conservative voltage from which to derive a *safe continuous rating.* In production, measuring at a level somewhat below the expected inception voltage and then derating by a factor related to expectations about system transients is an accepted practice.

Partial Discharge Testing

Not only does this test method provide far more qualitative information about stress-withstand levels than did previous stress tests, but it provides quantitative measurements from which quality assurance and control measures can be based. Tests similar to this test have been

used by some manufacturers, such as those of high-voltage power distribution equipment, for some time, but they employed a simple measurement of RF noise to detect ionization. This method was not quantitative with regard to energy of the discharge, and was not sensitive enough for small components such as isolation amplifiers. Now, however, manufacturers of HV test equipment have developed means to quantify partial discharge. VDE, the national standards group in Germany and an acknowledged leader in high-voltage test standards, has developed a standard test method to apply this powerful technique. Use of partial discharge testing is an improved method for measuring the integrity of an isolation barrier.

To accommodate poorly-defined transients, the part under test is exposed to a voltage that is 1.6 times the continuous-rated voltage and must display ≤5pC partial discharge level in a 100% production test.

BURN-IN SCREENING

Burn-in screening is an option available for the ISO120 and ISO121 products. Burn-in duration is 160 hours at +125°C (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

APPLICATIONS

The ISO120 and ISO121 isolation amplifiers are used in three categories of applications:

1. Accurate isolation of signals from high voltage ground potentials,
2. Accurate isolation of signals from severe ground noise and,
3. Fault protection from high voltages in analog measurements.

Figures 6 through 11 show a variety of application circuits.

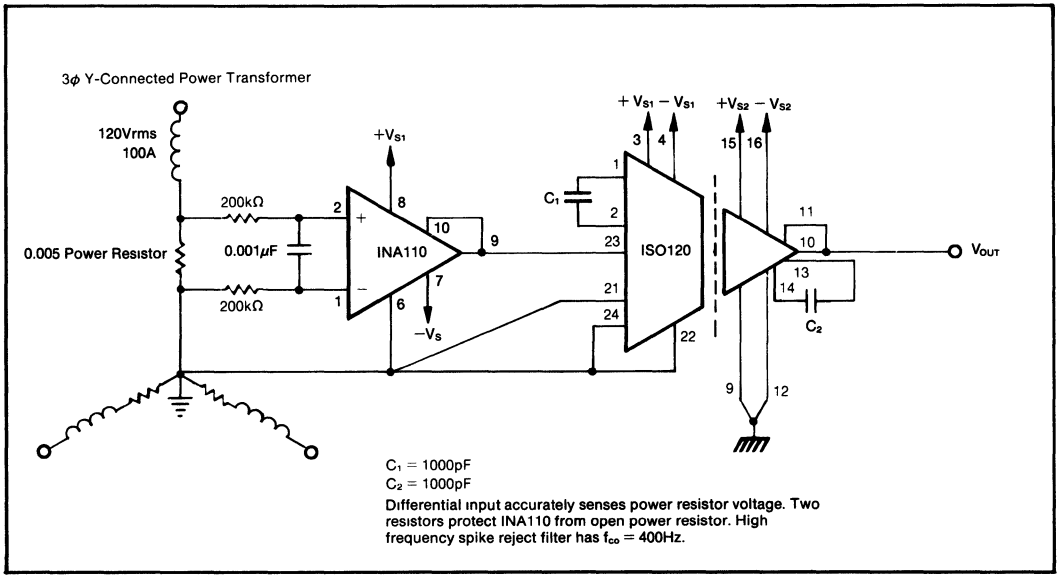


FIGURE 6. Isolated Powerline Monitor.

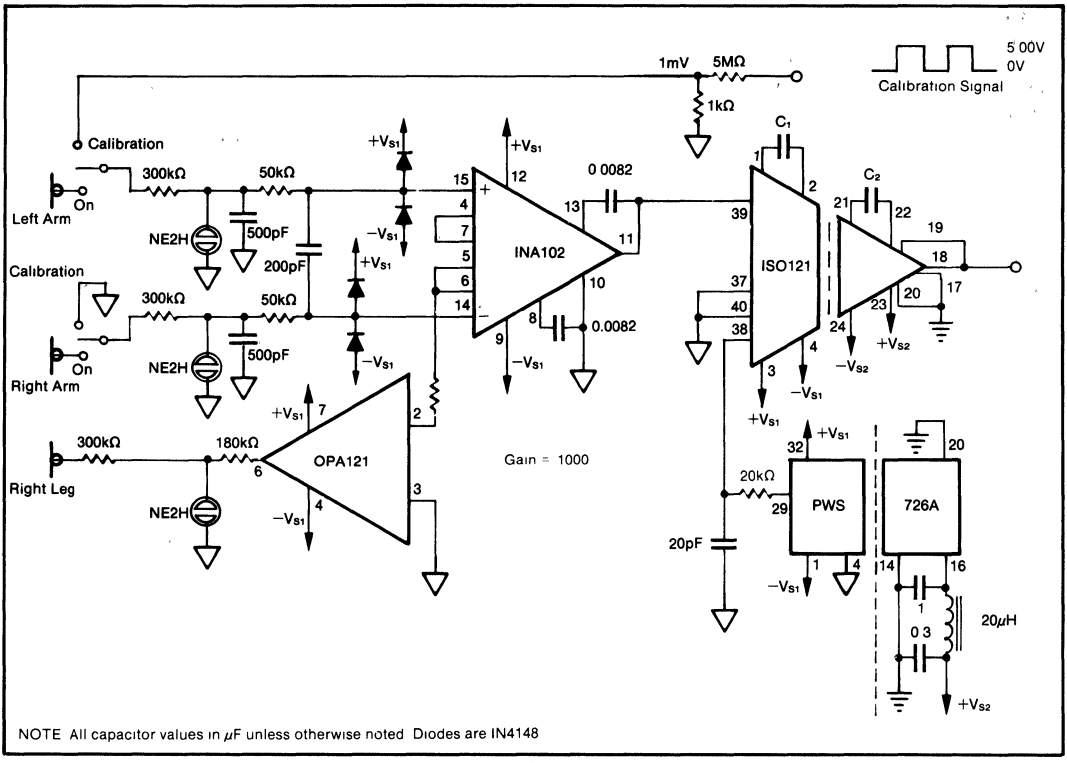


FIGURE 7. Right-Leg Driven ECG Amplifier (with defibrillator protection and calibrator).

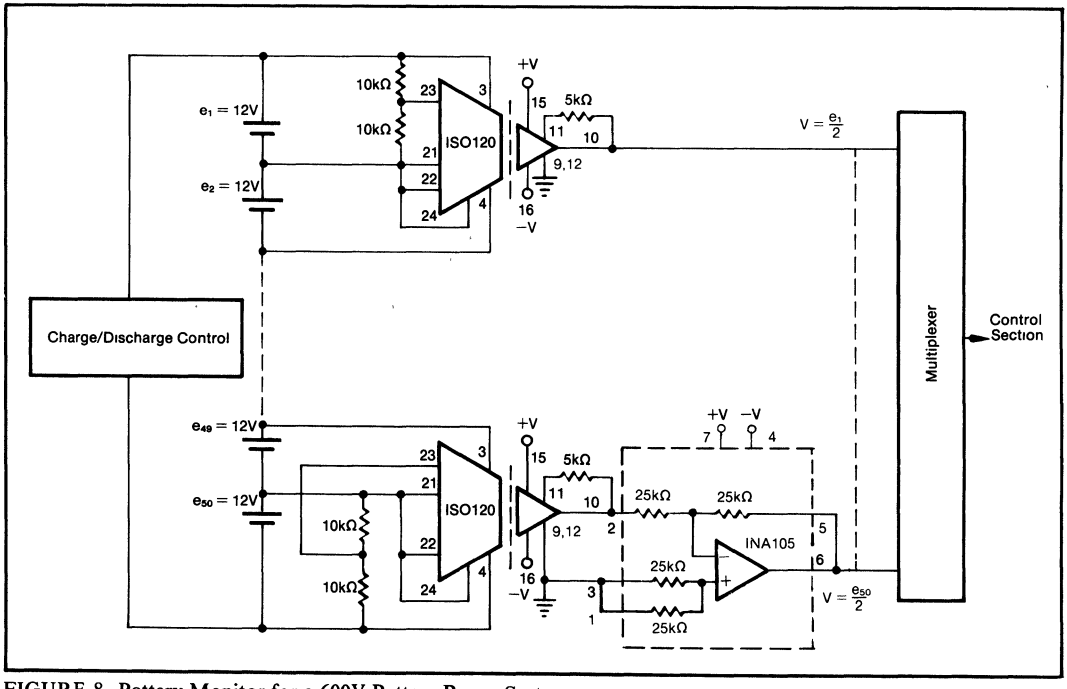


FIGURE 8. Battery Monitor for a 600V Battery Power System.

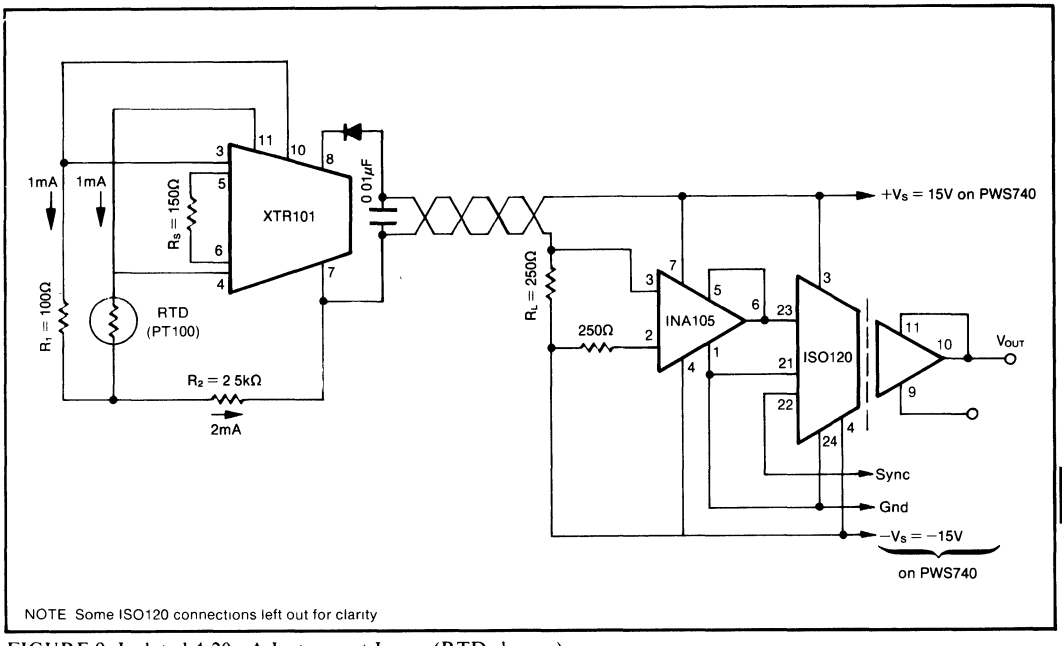


FIGURE 9. Isolated 4-20mA Instrument Loop. (RTD shown.)

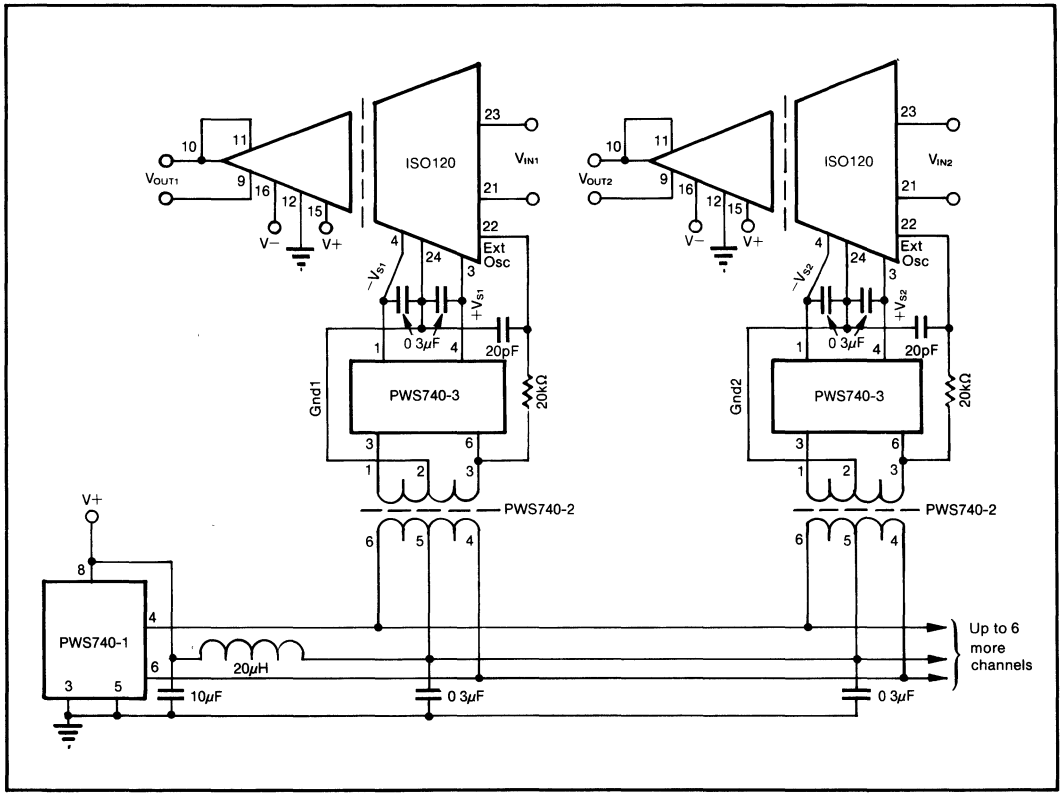


FIGURE 10. Synchronized-Multichannel Isolation System.

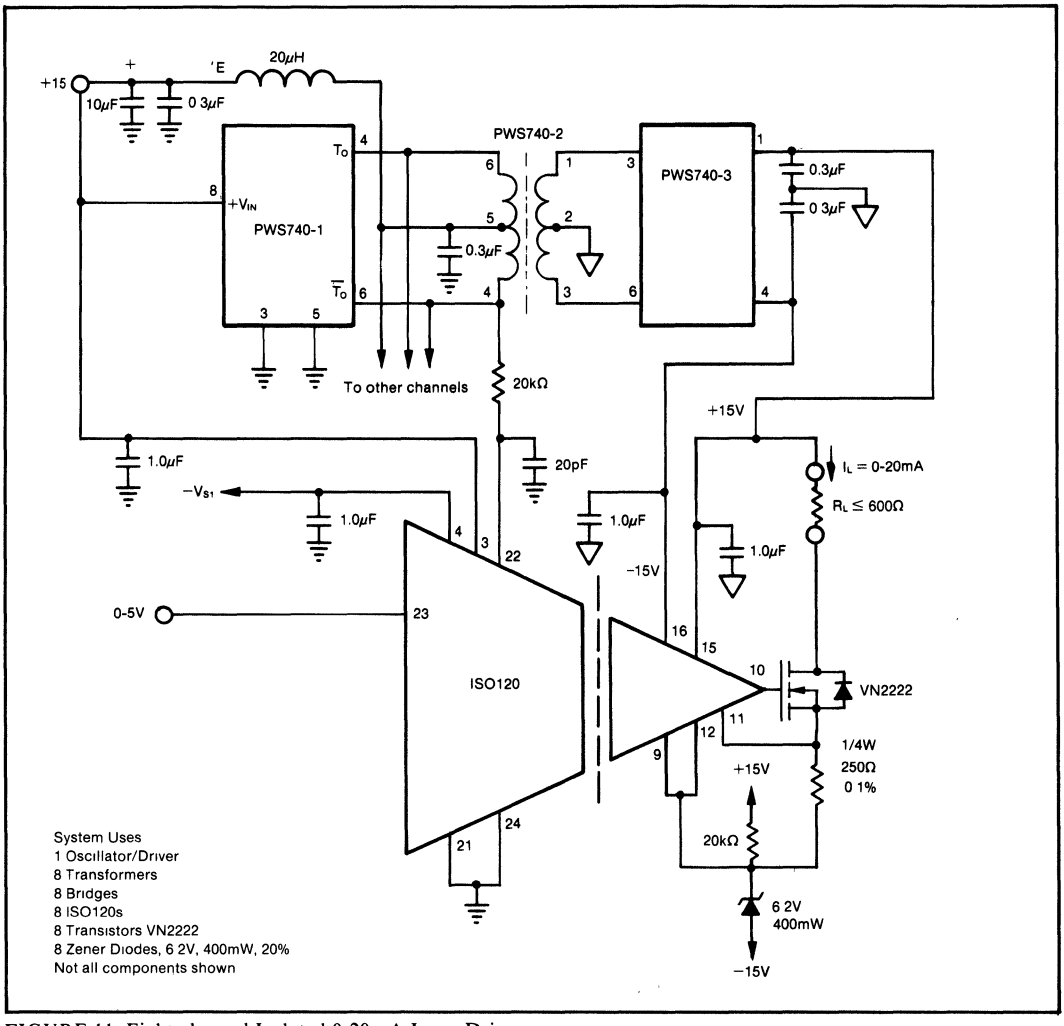


FIGURE 11. Eight-channel Isolated 0-20mA Loop Driver.

BURR-BROWN®

ISO122P

ADVANCE INFORMATION
SUBJECT TO CHANGE

Precision Lowest Cost ISOLATION AMPLIFIER

FEATURES

- 100 % TESTED FOR HIGH-VOLTAGE BREAKDOWN
- RATED 1500 Vrms
- HIGH IMR: 140dB at 60Hz
- BIPOLAR OPERATION: $V_O = \pm 10V$
- SINGLE-WIDE 16-PIN PLASTIC DIP
- EASE OF USE: Fixed Unity Gain Configuration

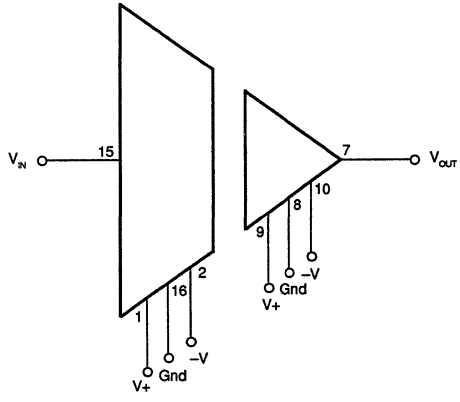
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL: Transducer Isolator, Isolator for Thermocouples, RTDs, Pressure Bridges, and Flow Meters, 4mA to 20mA Loop Isolation
- GROUND LOOP ELIMINATION
- MOTOR AND SCR CONTROL
- POWER MONITORING
- PC-BASED DATA ACQUISITION
- TEST EQUIPMENT
- VENDING MACHINES

DESCRIPTION

The ISO122P is a precision isolation amplifier incorporating a novel duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2pF differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity, resulting in excellent reliability and good high frequency transient immunity across the barrier. Both barrier capacitors are imbedded in the plastic body of the package.

The ISO122P is easy to use. No external components are required for operation. The key specification of 0.01% max nonlinearity is guaranteed, with up to 50kHz signal bandwidth and 200µV/°C max V_{OS} drift typical. A power supply range of ±4.5V to ±18V and quiescent current of ±4.5mA on V_{S1} and ±4.5mA on V_{S2} make these amplifiers ideal for a wide range of applications.



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PDS-857

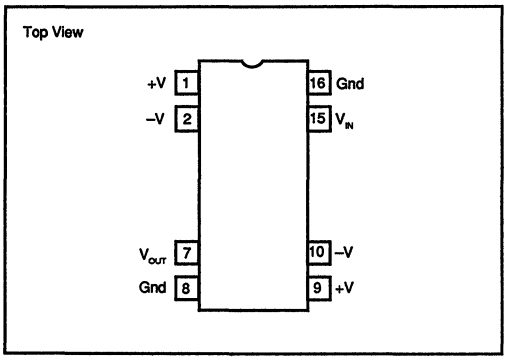
SPECIFICATIONS

At T_A = 25°C and $V_S1 = V_S2 = \pm15V$ unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ISOLATION					
Voltage Rated Continuous AC 60Hz		1500			VAC
100% Test 1	1s, 5pc PD	2400			VAC
Isolation Mode Rejection			140		dB
Barrier Impedance			10^{14} || 2		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms		0.18	0.5	µArms
GAIN	$V_O = \pm10V$				
Nominal Gain			1		V/V
Gain Error			±.05	±.30	%FSR
Gain vs Temperature			±10		ppm/°C
Nonlinearity			±.008	±.015	%FSR
INPUT OFFSET VOLTAGE					
Initial Offset			±5	±50	mV
vs Temperature			±200		µV/°C
vs Supply			±2		mV/V
Noise			4		µV/√Hz
INPUT					
Voltage Range		±10			V
Resistance			200		kΩ
OUTPUT					
Voltage Range		±10	±12		V
Current Drive		±5	±15		mA
Capacitive Load Drive			1000		pF
Ripple Voltage[2]			10		mVp-p
FREQUENCY RESPONSE					
Small Signal Bandwidth			50		kHz
Slew Rate			1.5		V/µs
Settling Time	$V_O = \pm10V$				
0.1%			50		µs
0.01%			150		µs
Overload Recover Time			150		µs
POWER SUPPLIES					
Rated Voltage			15		V
Voltage Range		±4.5		±18	V
Quiescent Current: V_{S1}			±4.5	±6.5	mA
V_{S2}			±4.5	±6.5	mA
TEMPERATURE RANGE					
Specification		0		70	°C
Operating		–25		85	°C
Storage		–25		85	°C
θ_{JA}			100		°C/W

NOTES: (1) Tested at 1.4 X rated, fail on 5pC partial discharge leakage current on five successive pulses. (2) Ripple frequency is at carrier frequency (500kHz).

CONNECTION DIAGRAM

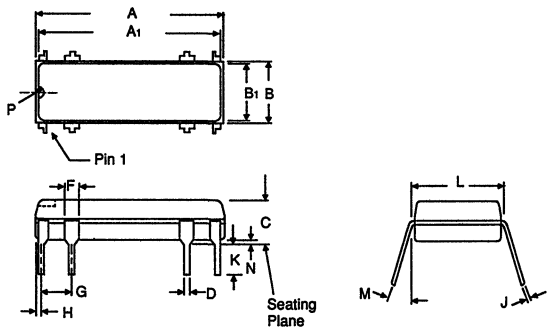


ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
V_{IN}	±100V
Continuous Isolation Voltage	1500Vrms
V_{ISO}, dv/dt	20kV/µs
Junction Temperature	+150°C
Storage Temperature	+85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short to Common	Continuous

MECHANICAL

P Package — Single-Wide 16-Pin Plastic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.740	.800	18.80	20.32
A1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.20	.050	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

THEORY OF OPERATION

The ISO122P isolation amplifier uses an input and an output section galvanically isolated by matched 1pF isolating capacitors built into the plastic package. The input is duty-cycle modulated and transmitted digitally across the barrier. The output section receives the modulated signal, converts it back to an analog voltage and removes the ripple component inherent in the demodulation. Input and output sections are fabricated, then laser trimmed for exceptional circuitry matching common to both input and output sections. The sections are then mounted on opposite ends of the package with the isolating capacitors mounted between the two sections.

MODULATOR

An input amplifier (A1, Figure 1) integrates the difference between the input current (V_{IN}/200kΩ) and a switched ±100µA current source. This current source is implemented by a switchable 200µA source and a fixed 100µA current sink.

To understand the basic operation of the modulator, assume that V_{IN} = 0.0V. The integrator will ramp in one direction until the comparator threshold is exceeded. The comparator and sense amp will force the current source to switch; the resultant signal is a triangular waveform with a 50% duty cycle. The internal oscillator forces the current source to switch at the 500kHz frequency. If V_{IN} changes, the duty cycle of the integrator will change to keep the average DC value at the output of A1 near zero volts

DEMODULATOR

The sense amplifier drives a switched current source into integrator A2. The output stage balances the duty-cycle modulated current against the feedback current through the 200kΩ feedback resistor, resulting in an average value at the V_{OUT} pin equal to V_{IN}. The sample and hold amplifiers in the output feedback loop serve to remove undesired ripple voltages inherent in the demodulation process.

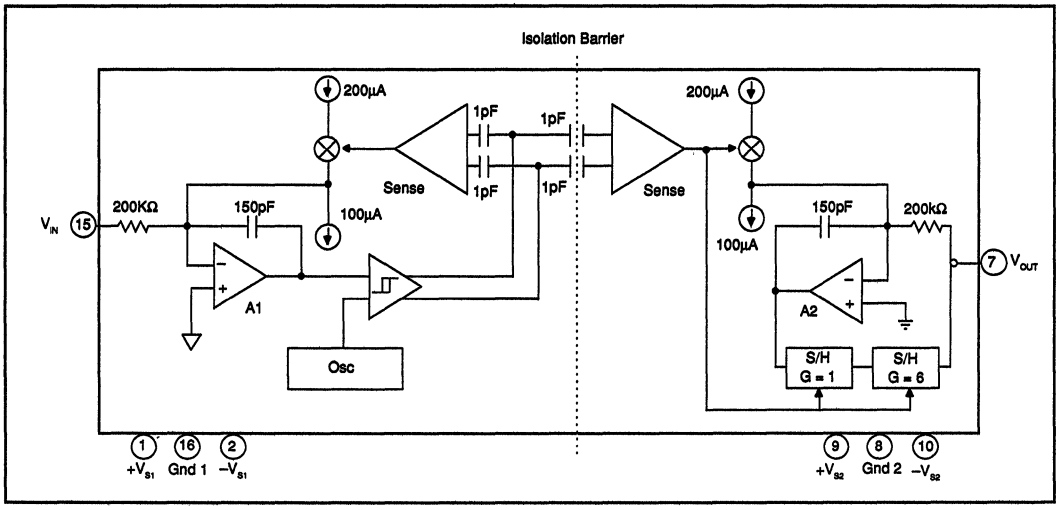


FIGURE 1. Block Diagram.

BASIC OPERATION

SIGNAL AND POWER CONNECTIONS

Each power supply pin should be bypassed with 1µF tantalum capacitors located as close to the amplifier as possible. The internal frequency of the modulator/demodulator is set at 500kHz by an internal oscillator. Therefore if it is desired to minimize any feedthrough noise (beat frequencies) from a DC/DC converter, use a pie filter on the supplies (See Figure 2).

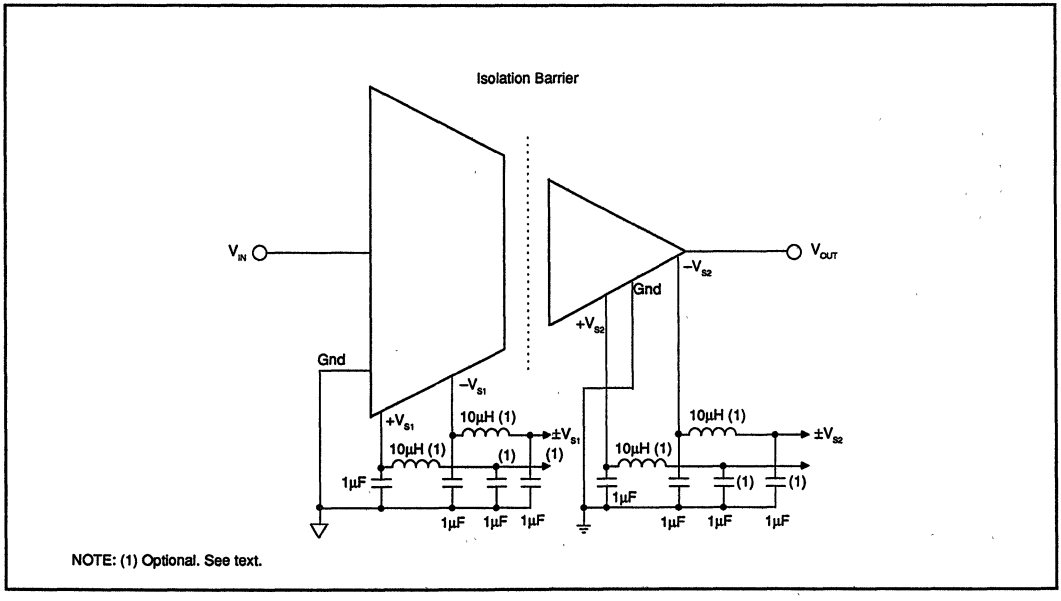


FIGURE 2. Applications Figure.

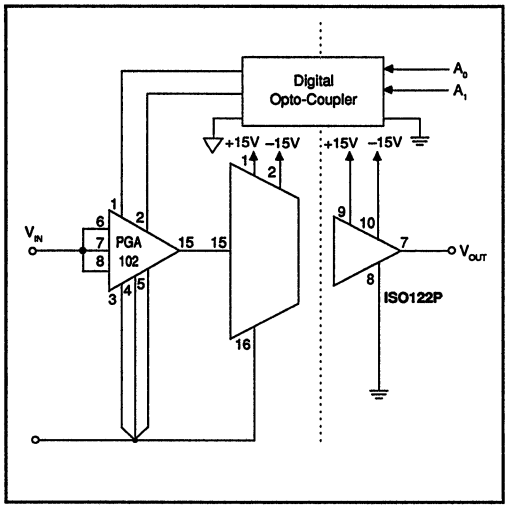


FIGURE 3. Programmable-Gain Isolation Channel with Gains of 1, 10, and 100.

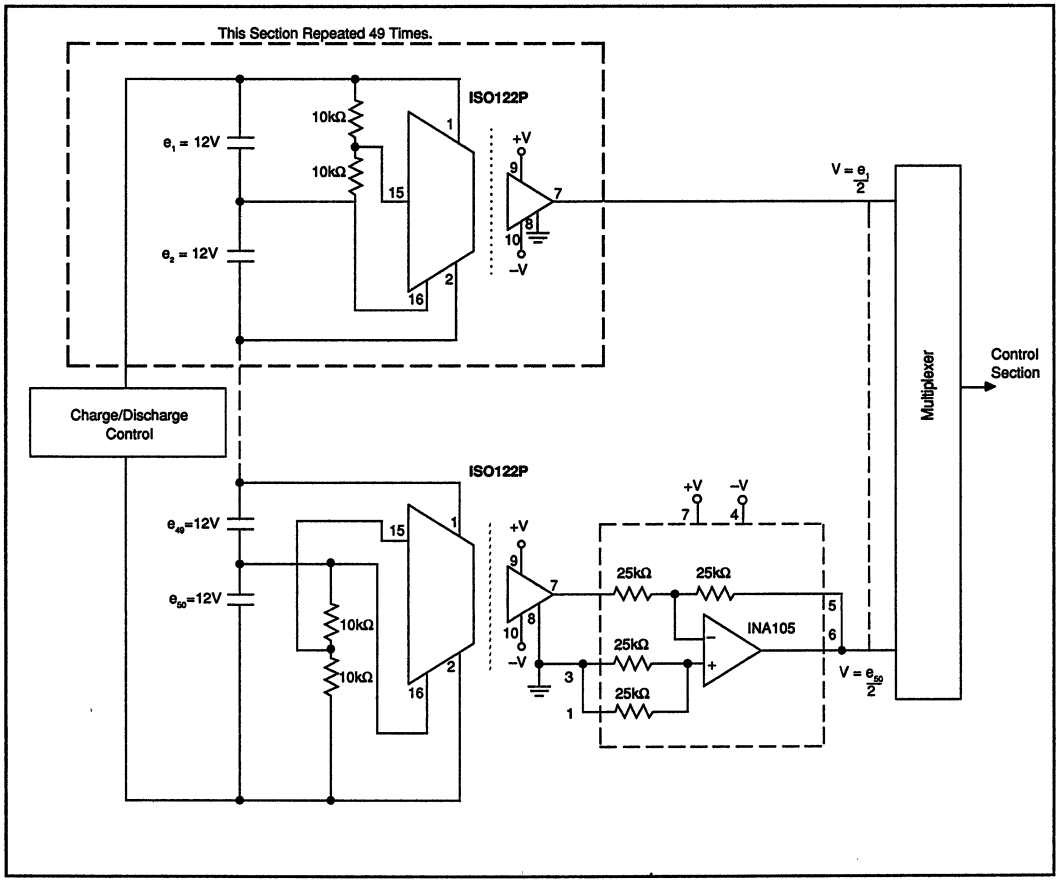


FIGURE 4. Battery Monitor for a 600V Battery Power System. (Derives the Input Power from the Battery.)

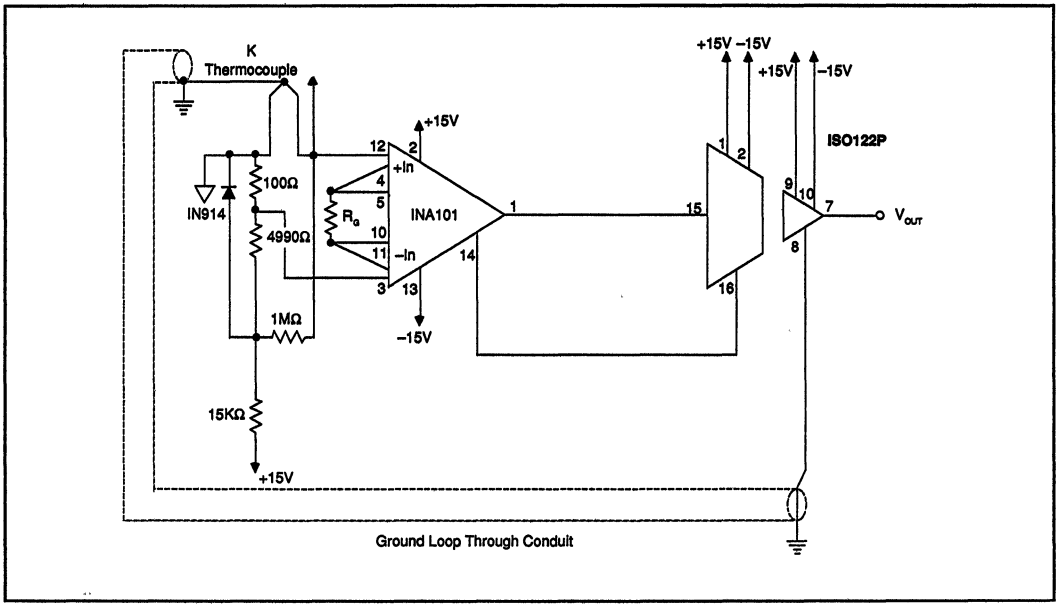


FIGURE 5. Thermocouple Amplifier with Ground Loop Elimination, Cold Junction Compensation, and Up-scale Burn-out.

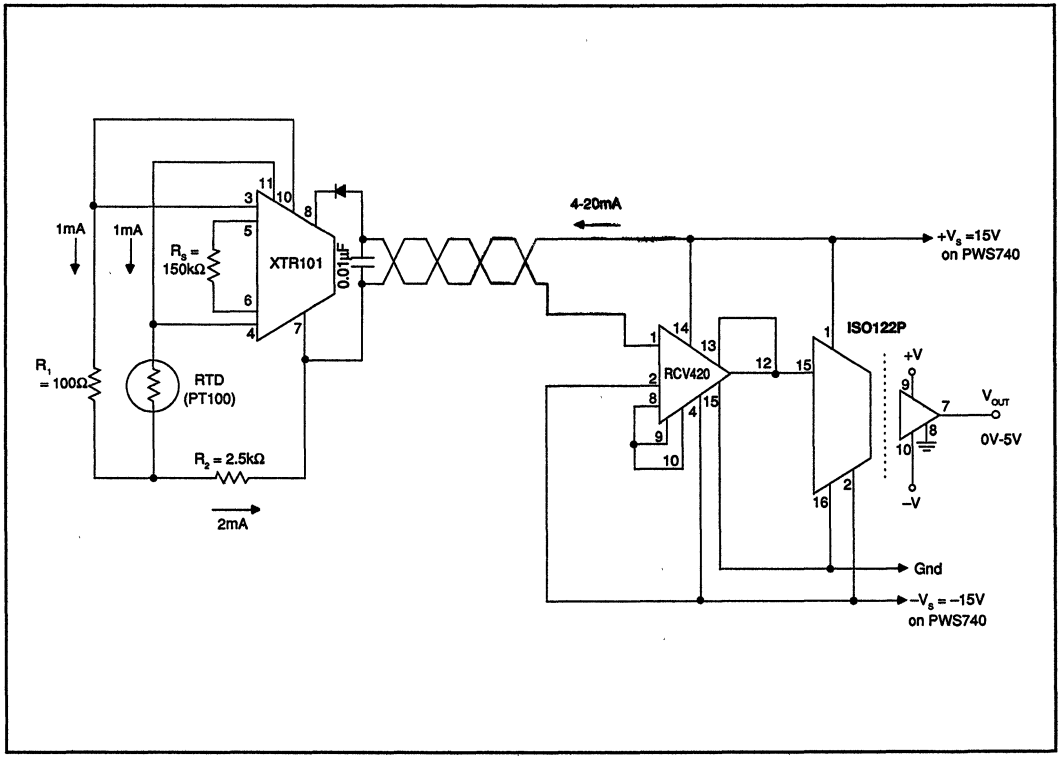


FIGURE 6. Isolated 4-20mA Instrument Loop. (RTD shown.)

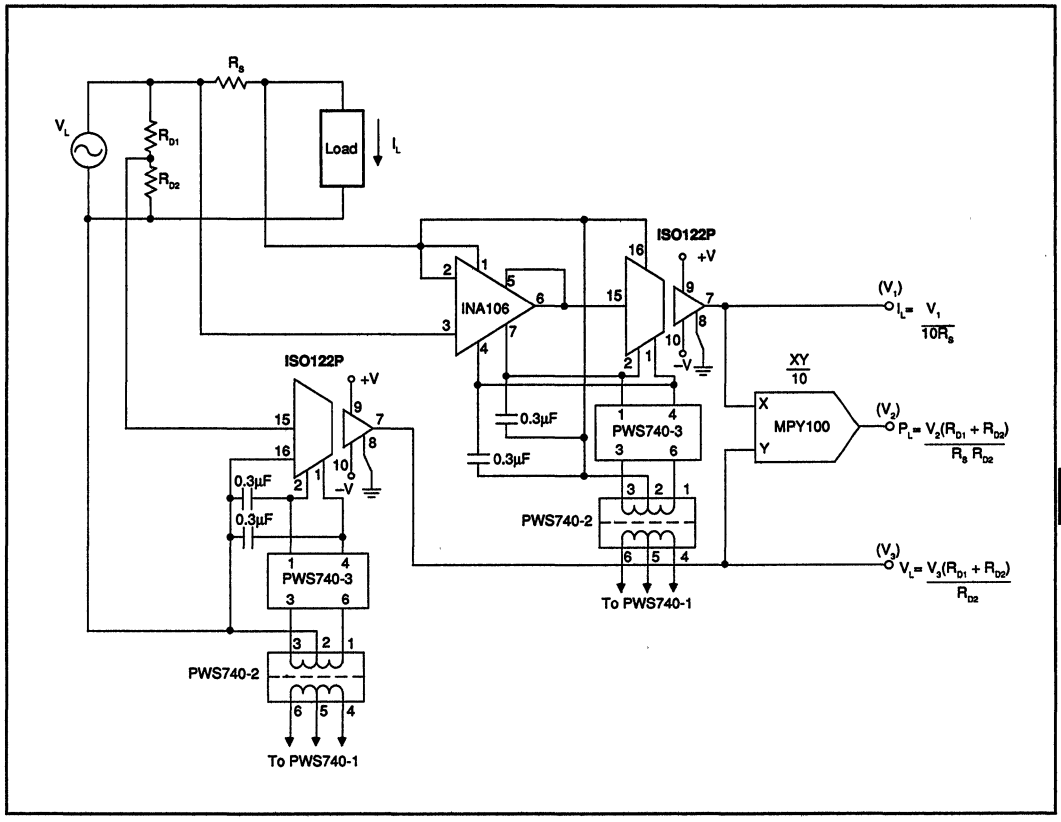


FIGURE 7. Isolated Power Line Monitor.

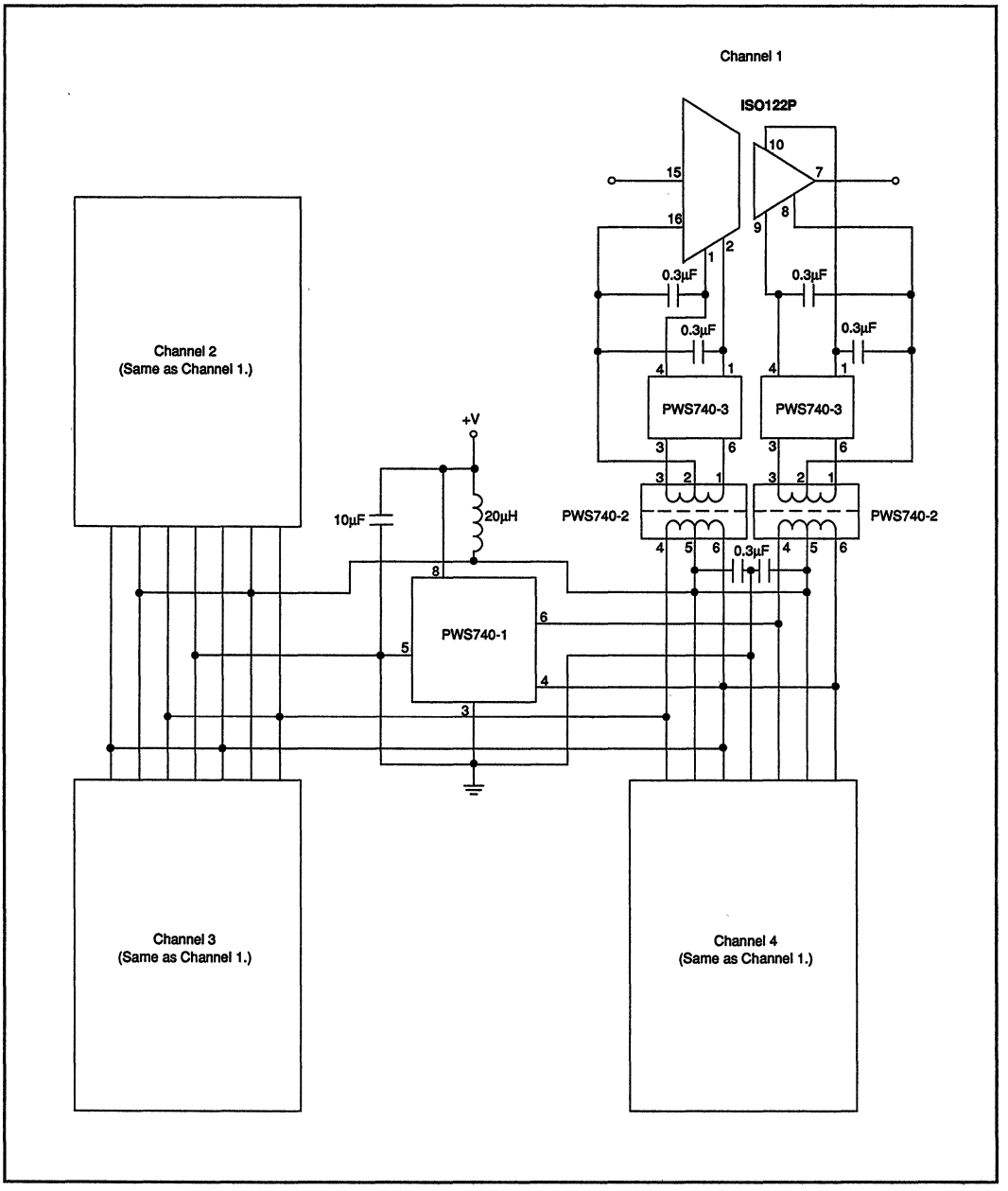
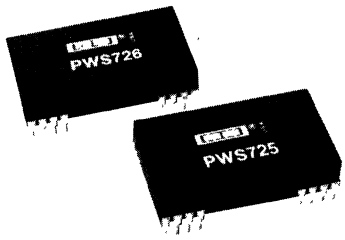


FIGURE 8. Three-Port, Low-Cost, Four-Channel Isolated, Data Acquisition System.

BURR-BROWN®



PWS725
PWS726

Isolated, Unregulated DC/DC CONVERTERS

FEATURES

- ISOLATED ±7 TO ±18VDC OUTPUT FROM SINGLE 7 TO 18VDC SUPPLY
- ±15mA OUTPUT AT RATED VOLTAGE ACCURACY
- HIGH ISOLATION VOLTAGE
  PWS725: 1500Vrms
  PWS726: 3500Vrms
- LOW LEAKAGE CAPACITANCE: 9pF
- LOW LEAKAGE CURRENT: 2μA, max, at 240VAC 50/60Hz
- HIGH RELIABILITY DESIGN
- AVAILABLE WITH OUTPUT SYNCHRONIZATION SIGNAL FOR USE WITH ISO120 AND ISO121
- PROTECTED AGAINST OUTPUT FAULTS
- COMPACT
- LOW COST
- EASY TO APPLY—FEW EXTERNAL PARTS

APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS EQUIPMENT
- TEST EQUIPMENT
- DATA ACQUISITION

DESCRIPTION

The PWS725 and PWS726 convert a single 7 to 18VDC input to bipolar voltages of the same value as the input voltage. The converters are capable of providing ±15mA at rated voltage accuracy and up to ±40mA without damage. (See Output Current Rating.)

The PWS725 and PWS726 converters provide reliable, engineered solutions where isolated power is required in critical applications. The high isolation voltage rating is achieved through use of a specially-designed transformer and physical spacing. An additional high dielectric-strength, low leakage transformer coating increases the isolation rating of the PWS726.

Reliability and performance are designed in. The bifilar wound, wirebonded transformer simultaneously provides lower output ripple than competing designs, and a higher performance/cost ratio. The soft-start oscillator/driver design assures full operation of the oscillator before either MOSFET driver turns on, protects the switches, and eliminates high inrush currents during turn-on. Input current sensing protects both the converter and the load from possible thermal damage during a fault condition.

Special design features make these converters especially easy to apply. The compact size allows dense circuit layout while maintaining critical isolation requirements. The Input Sync connection allows frequency synchronization of multiple converters. The Output Sync (PWS725A and PWS726A only) is available to synchronize ISO120 and ISO121 isolation amplifiers. The Enable input allows control over output power in instances where shutdown is desired to conserve power, such as in battery-powered equipment, or where sequencing of power turn-on/turn-off is desired.

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PDS-736B

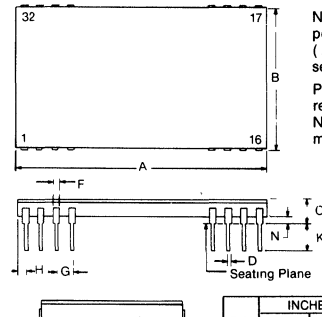
SPECIFICATIONS

ELECTRICAL

T_A = +25°C, C_L = 1 0μF ceramic, V_{IN} = 15VDC, operating frequency = 800kHz, V_{OUT} = ±15VDC, C_{IN} = 1.0μF ceramic, I_{OUT} = ±15mA, unless otherwise noted.

PARAMETERS	CONDITIONS	PWS725/725A			PWS726/726A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Rated Voltage			15			*		VDC
Input Voltage Range		7		18	*		*	VDC
Input Current	I_O = ±15mA		77			*		mA
Input Current Ripple	No external filtering		150			*		mAp-p
	L-C input filter, L_{IN} = 100μH, C_{IN} = 1μF(1)		5			*		mAp-p
	C only, C_{IN} = 1μF		60					mAp-p
ISOLATION								
Test Voltages	Input to output, 10 seconds	4000			8000			VDC
	Input to output, 60 seconds, minimum	1500			3500			Vrms
Rated Voltage	Input to output, continuous, AC 60Hz			1500			3500	Vrms
	Input to output, continuous DC			2121			4950	VDC
Isolation Impedance	Input to output		10^{12}‖9			*		Ω‖pF
Leakage Current	Input to output, 240Vrms, 60Hz		1 2		2 0	*	*	μA
OUTPUT								
Rated Output Voltage		14 25	15 00	15 75	*	*	*	VDC
Output Current	Balanced loads		15 0	40		*	*	mA
	Single-ended			80			*	mA
Load Regulation	Balanced loads, ±10mA < I_{OUT} < ±40mA			0 4			*	%/mA
Ripple Voltage (400kHz)	No external capacitor		60			*		mVp-p
	L_O = 10μH, C_O = 1μF (Figure 1)		10			*		mVp-p
	L_O = 0μH, C_O filter only		See Performance Curves					
Output Switching Noise	L_O = 10μH, C_O = 1 0μF		1			*		mVp-p
Output Capacitive Load	L_O = 100μH, C filter			10			*	μF
	C filter only			1			*	μF
Voltage Balance, V+, V−			0 04					%
Sensitivity to ΔV_{IN}			1 15					V/V
Output Voltage Temp Coefficient			10					mV/°C
Output Sync Signal PWS725A/PWS726A only	Square Wave, 50% duty cycle		30			*		V, p-p
TEMPERATURE								
Specification		−25		+85	*		*	°C
Operating		−25		+85	*		*	°C
Storage		−25		+125	*		*	°C

MECHANICAL

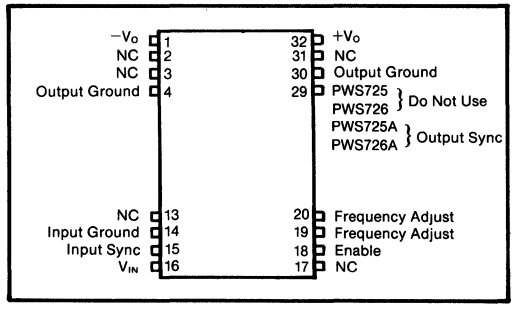


NOTE. Leads in true position within .010" (.25mm) R at MMC at seating plane

Pin numbers shown for reference only. Numbers are not marked on package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.310	.370	7.87	9.40
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.150	.185	3.81	4.70
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

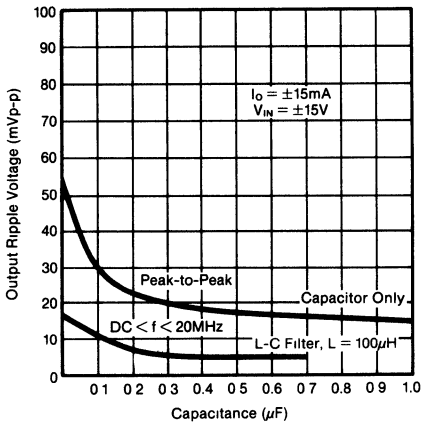
PIN CONFIGURATION



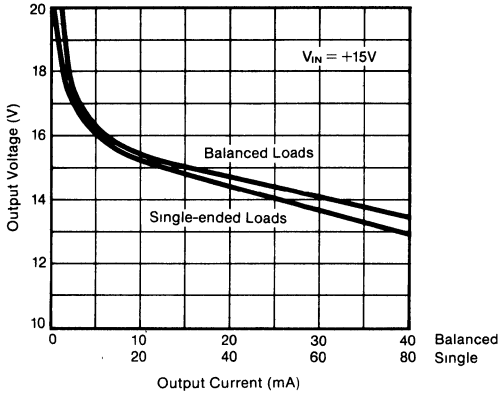
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted

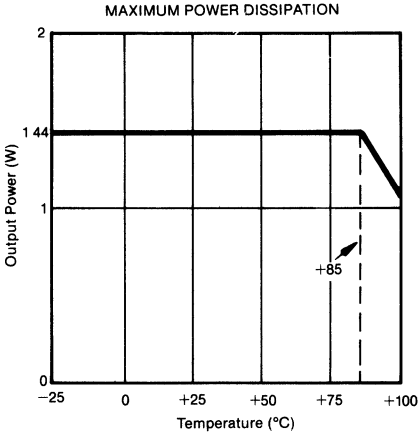
OUTPUT CAPACITANCE vs RIPPLE VOLTAGE



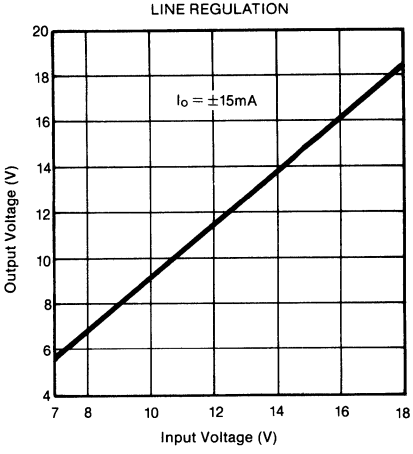
LOAD REGULATION



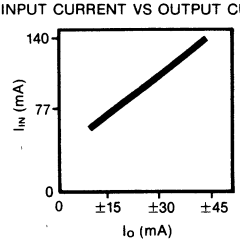
MAXIMUM POWER DISSIPATION



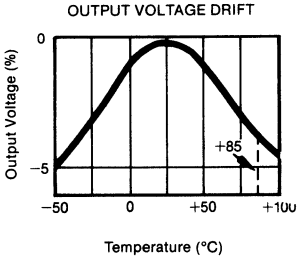
LINE REGULATION



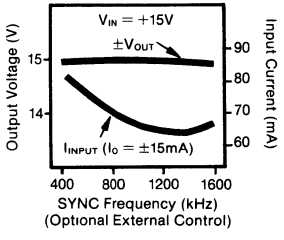
INPUT CURRENT VS OUTPUT CURRENT



OUTPUT VOLTAGE DRIFT



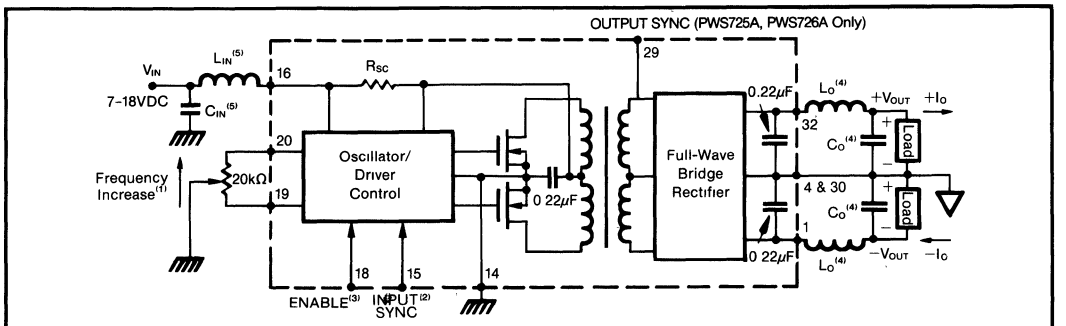
SYNC FREQUENCY VS INPUT CURRENT AND OUTPUT VOLTAGE



THEORY OF OPERATION

The PWS725 and the PWS726 DC-to-DC converters consist of a free-running oscillator, control and switch driver circuitry, MOSFET switches, a transformer, a bridge rectifier, and filter capacitors together in a 32-pin DIP (0.900 inches nominal) package. The control circuitry consists of current limiting, soft start, frequency adjust, enable, and synchronization features. See Figure 1.

In instances where several converters are used in a system, beat frequencies developed between the converters are a potential source of low frequency noise in the supply and ground paths. This noise may couple into signal paths. See Figures 2 and 3 for connection of INPUT SYNC pin. Converters can be synchronized and these beat frequencies avoided. The unit with the highest natural



NOTES (1) Frequency Adjust is optional, with pins 19 and 20 left open The normal switching frequency is 800kHz
(2) Leave INPUT SYNC pin open if unused, limit stray capacitance on INPUT SYNC pin to less than 50pF
(3) Leave ENABLE pin open or connect to V_{IN} if not used
(4) Optional output filtering, with $L_O = 0$, limit $C_O \leq 1\mu F$, with $L_O = 100\mu H$, limit $C_O \leq 10\mu F$, See Performance Curves for $L_O = 0$
(5) Optional input filtering, see Performance Curves for $L_{IN} = 0$
(6) CAUTION Do not connect pin 29 to low impedance loads (PWS725A, PWS726A) See Figure 5

FIGURE 1. PWS725/726 Functional Diagram.

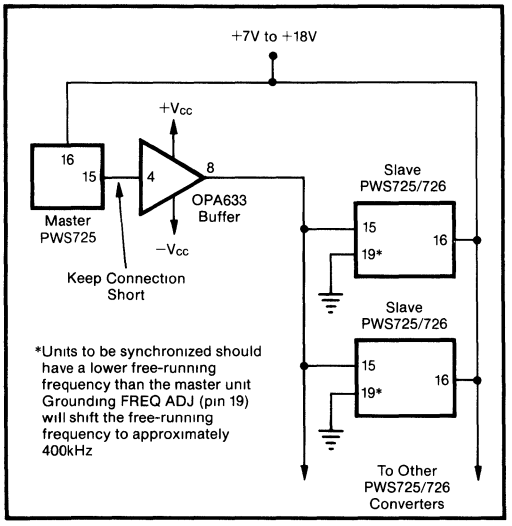


FIGURE 2. Synchronization of Multiple PWS725s or PWS726s from a Master Converter.

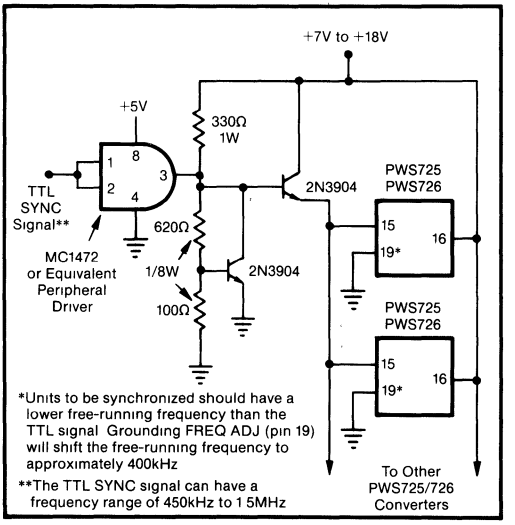


FIGURE 3. Synchronization of Multiple PWS725s or PWS726s from an External TTL Signal.

frequency will determine the synchronized running frequency. To avoid excess stray capacitance, the INPUT SYNC pin should not be loaded with more than 50pF. If unused, the INPUT SYNC must be left open.

Soft start circuitry protects the MOSFET switches during start up. This is accomplished by holding the gate-to-source voltage of both MOSFET switches low until the free-running oscillator is fully operational. In addition to the soft start circuitry, input current sensing also protects the MOSFET switches. This current limiting keeps the FET switches operating in their safe operating area under fault conditions or excessive loads. When either of these conditions occur, the peak input current exceeds a safe limit. The result is an approximate 5% duty cycle, 300μs drive period to the MOSFET switches. This protects the internal MOSFET switches as well as the external load from any thermal damage. When the fault or excessive load is removed, the converter resumes normal operation. A delay period of approximately 50μs incorporated in the current sensing circuitry allows the output filter capacitors to fully charge after a fault is removed. This delay period corresponds to a filter capacitance of no more than 1μF at either of the output pins. This provides full protection of the MOSFET switches and also sufficiently filters the output ripple voltage (see specification table). The current sensing circuitry is designed to provide thermal protection for the MOSFET switches over the operating temperature range as well. The low thermal resistance of the package (θ_{JC} = 10°C/W) ensures safe operation under rated conditions. When these rated conditions are exceeded, the unit will go into its shutdown mode.

An optional potentiometer can be connected between the two FREQUENCY ADJUST pins to trim the oscilla-

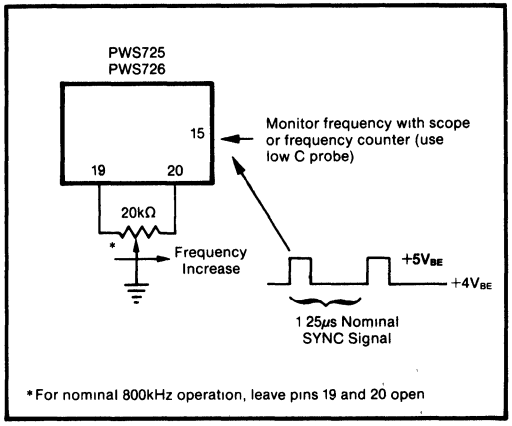


FIGURE 4. Frequency Adjustment Procedure.

tor operating frequency ±10% (see Figure 4). Care should be taken when trimming the frequency near the low frequency range. If the frequency is trimmed too low, the peak inductive currents in the primary will trip the input current sensing circuitry to protect the MOSFET switches from these peak inductive currents.

The ENABLE pin allows external control of output power. When this pin is pulled low, output power is disabled. Logic thresholds are TTL compatible. When not used, the Enable input may be left open or tied to V_{IN} (pin 16).

OUTPUT CURRENT RATING

The total current which can be drawn from the PWS725 or PWS726 is a function of total power being drawn from both outputs (see Functional Diagram). If one output is not used, then maximum current can be drawn from the other output. If both outputs are loaded, the total current must be limited such that:

$$|I_L+| + |I_L-| \leq 80mA$$

It should be noted that many analog circuit functions do not simultaneously draw full rated current from both the positive and negative supplies. For example, an operational amplifier may draw 13mA from the positive supply under full load while drawing only 3mA from the negative supply. Under these conditions, the PWS725/726 could supply power for up to five devices (80mA ÷ 16mA ≈ 5). Thus, the PWS725/726 can power more circuits than is at first apparent.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter period of time. The relationship between actual test conditions and the continuous derated maximum specification is an important one. Burr-Brown has chosen a deliberately conservative one: $VDC_{TEST} = (2 \times VACrms_{CONTINUOUS\ RATING}) + 1000V$ for ten seconds. This choice is appropriate for conditions where system transient voltages are not well defined.* Where the real voltages are well-defined or where the isolation voltage is not continuous, the user may choose a less conservative derating to establish a specification from the test voltage.

OUTPUT SYNC SIGNAL

To allow synchronization of an ISO120 or ISO121 isolation amplifier, the PWS725A and PWS726A have an OUTPUT SYNC signal at pin 29. It should be connected as shown in Figure 5 to keep capacitive loading of pin 29 to a minimum.

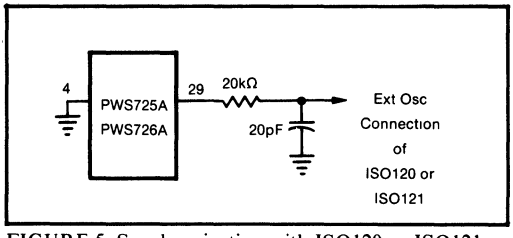


FIGURE 5. Synchronization with ISO120 or ISO121 Isolation Amplifier.

*Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS I-109 and ICS I-111.

BURR-BROWN®

PWS727

ADVANCE INFORMATION
SUBJECT TO CHANGE

Isolated, Unregulated DC/DC CONVERTER

FEATURES

- 100% TESTED FOR HIGH-VOLTAGE BREAKDOWN
- RATED 1500Vrms
- ±15mA OUTPUT AT RATED VOLTAGE ACCURACY
- COMPACT
- EASY TO APPLY
- FEW EXTERNAL PARTS

APPLICATIONS

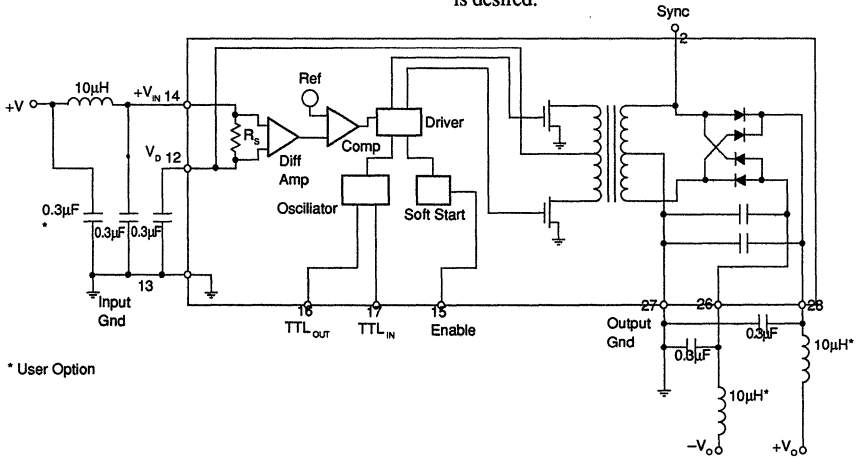
- INDUSTRIAL PROCESS CONTROL EQUIPMENT
- GROUND-LOOP ELIMINATION
- PC-BASED DATA ACQUISITION
- TEST EQUIPMENT
- VENDING MACHINES

DESCRIPTION

The PWS727 converts a single 10VDC to 18VDC input to bipolar voltages of the same value as the input voltage. The converters are capable of providing ±15mA at rated voltage accuracy and up to ±30mA without damage.

The PWS727 provides reliable, engineered solutions where isolated power is required. Special design features make these converters easy to use.

The compact size allows dense circuit layout, while maintaining critical isolation requirements. TTL_{IN} and TTL_{OUT} connections allow frequency synchronization of up to eight converters to a master converter. Synchronization to an external clock is also possible with the TTL_{IN} function. The Enable allows control over output power in instances where shutdown is desired to conserve power, or where sequential power turn on/turn off is desired.



* User Option

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PDS-839

SPECIFICATIONS

At T_A = 25°C and V_{IN} = +15V; Output Load = ±15mA unless otherwise noted

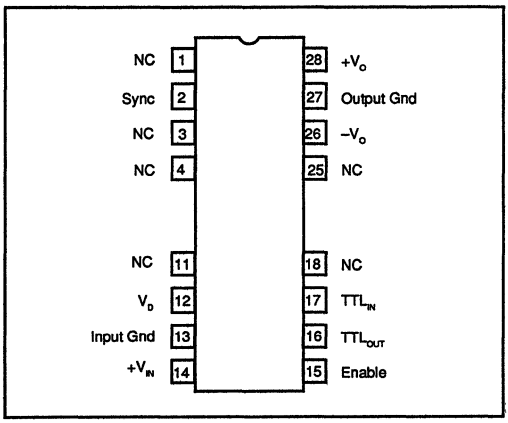
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ISOLATION					
Voltage Rated Continuous AC 60Hz		1500			VAC
100% Test [1]	1s, 5pC PD	2400			VAC
Barrier Impedance			10^{14} || 8		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms		1.0	1.5	µArms
INPUT					
Rated Voltage			15		V
Voltage Range		10		18	V
Current	±30mA Output	90	100	110	mA
Current Ripple	0.3 µF Capacitive Filter		150		mAp-p
	LC Input Filter		5		mAp-p
Current Limit	Outputs Shorted		250		mAp-p
OUTPUT					
Rated Output Voltage		±14.25	±15.00	±15.75	V
Output Current	Balanced Loads		±15	±30	mA
	Single-Ended			60	mA
Load Regulation	Balanced Loads			0.6	%/mA
	±10mA to ±40mA				
Ripple Voltage (800kHz)	0.3µF External Caps		9		mVp-p
	External Filter per Diagram				
Output Switching Noise			60		mVp-p
Output Capacitive Load			5		µF
Voltage Balance +V, –V			10		mV
Sensitivity to V_{IN}			1.15		V/V
Output VoltageTemp Coefficient			10		mV/°C
TEMPERATURE RANGE					
Specification		0		70	°C
Operating		–25		85	°C
Storage		–25		85	°C
θ_{JA}			100		°C/W

NOTES: (1) Tested at 1.6 x rated, fail on 5pC partial discharge leakage current on 5 successive pulses.

ORDERING INFORMATION

Basic Model Number — PWS727

PIN CONFIGURATION

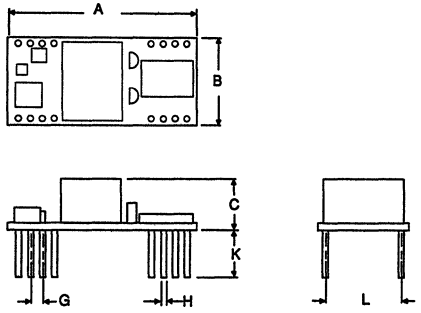


ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Continuous Isolation Voltage	1500Vrms
Junction Temperature	+150°C
Storage Temperature	+85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short-to-Common	Continuous

MECHANICAL

28-Pin Double-Wide DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.440	1.460	36.58	37.08
B	.690	.710	17.53	18.03
C	.390	.410	9.91	10.41
G	.100 BASIC		2.54 BASIC	
H	.020 BASIC		0.51 BASIC	
K	.190	.210	4.83	5.33
L	.600 BASIC		15.24 BASIC	

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package. Pin material and plating composition conform to method 2003 (solderability of MIL-STD-883 (except paragraph 3.2).

BURR-BROWN®

PWS728

ADVANCE INFORMATION
SUBJECT TO CHANGE

Isolated, Unregulated DC/DC CONVERTER

FEATURES

- 100% TESTED FOR HIGH-VOLTAGE BREAKDOWN
- RATED 1500Vrms
- ±15mA OUTPUT AT RATED VOLTAGE ACCURACY
- COMPACT
- EASY TO APPLY
- FEW EXTERNAL PARTS

APPLICATIONS

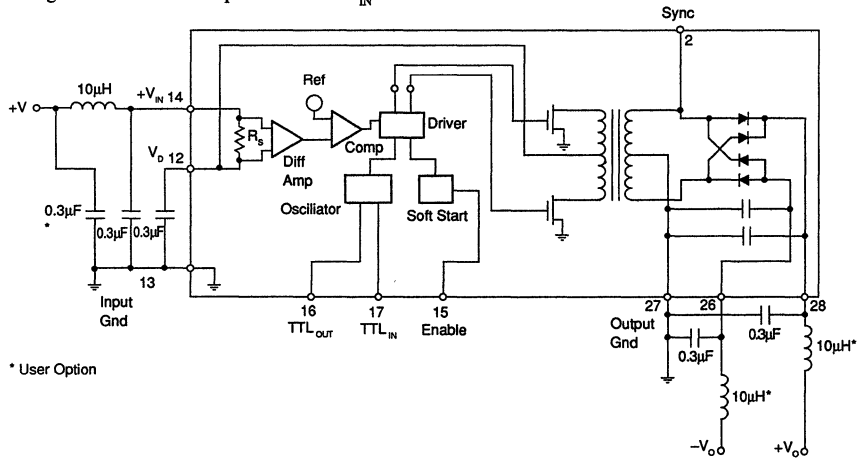
- INDUSTRIAL PROCESS CONTROL EQUIPMENT
- GROUND-LOOP ELIMINATION
- PC-BASED DATA ACQUISITION
- TEST EQUIPMENT
- VENDING MACHINES

DESCRIPTION

The PWS728 converts a single 5VDC input to ±15VDC. The converter is capable of providing ±15mA at rated voltage accuracy and up to ±30mA without damage.

The PWS728 provides reliable, engineered solutions where isolated power is required. Special design features make these converters easy to use.

The compact size allows dense circuit layout, while maintaining critical isolation requirements. TTL_{IN} and TTL_{OUT} connections allow frequency synchronization of up to eight converters to a master converter. Synchronization to an external clock is also possible with the TTL_{IN} function. The Enable allows control over output power in instances where shutdown is desired to conserve power, or where sequential power turn on/turn off is desired.



* User Option

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PDS-862

SPECIFICATIONS

At T_A = 25°C and V_{IN} = +5V; Output Load = ±15mA unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ISOLATION					
Voltage Rated Continuous AC 60Hz		1500			VAC
100% Test (1)	1s, 5pC PD	2400			VAC
Barrier Impedance			10^{14} || 8		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms		1.0	1.5	µArms
INPUT					
Rated Voltage			5		V
Voltage Range		4.5		5.5	V
Current	±30mA Output	110	130	150	mA
Current Ripple	0.3 µF Capacitive Filter		150		mAp-p
	LC Input Filter		5		mAp-p
Current Limit	Outputs Shorted		375		mAp-p
OUTPUT					
Rated Output Voltage		±14.25	±15.00	±15.75	V
Output Current	Balanced Loads		±15	±30	mA
	Single-Ended			60	mA
Load Regulation	Balanced Loads			2	%/mA
	±7mA to ±22mA				
Ripple Voltage (800kHz)	0.3µF External Caps		9		mVp-p
	External Filter per Diagram				
Output Switching Noise			60		mVp-p
Output Capacitive Load			5		µF
Voltage Balance +V, –V			10		mV
Sensitivity to V_{IN}			4.6		V/V
Output VoltageTemp Coefficient			10		mV/°C
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–25		+85	°C
Storage		–25		+85	°C
θ_{JA}			100		°C/W

NOTES: (1) Tested at 1.6 x rated, fail on 5pC partial discharge leakage current on 5 successive pulses.

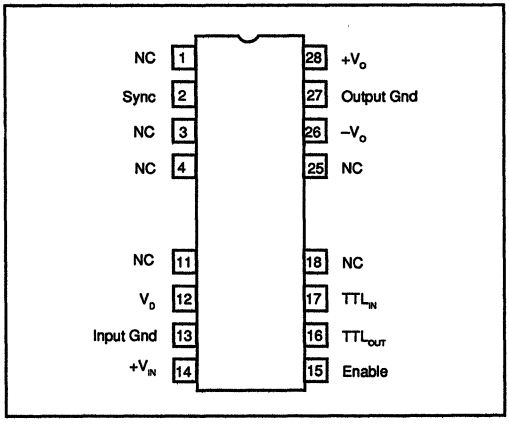
ORDERING INFORMATION

Basic Model Number — PWS728

ABSOLUTE MAXIMUM RATINGS

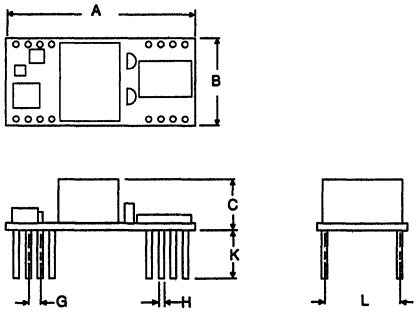
Supply Voltage	5.75V
Continuous Isolation Voltage	1500Vrms
Junction Temperature	+150°C
Storage Temperature	+85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short-to-Common	Continuous

PIN CONFIGURATION



MECHANICAL

28-Pin Double-Wide DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.440	1.460	36.58	37.08
B	.690	.710	17.53	18.03
C	.390	.410	9.91	10.41
G	.100 BASIC		2.54 BASIC	
H	.020 BASIC		0.51 BASIC	
K	.190	.210	4.83	5.33
L	.600 BASIC		15.24 BASIC	

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

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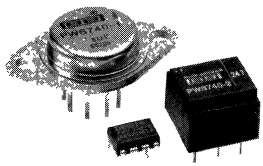


PWS740

Distributed Multichannel Isolated DC-TO-DC CONVERTER

FEATURES

- ISOLATED ±7 TO ±20VDC OUTPUTS
- BARRIER 100% TESTED AT 1500VAC, 60Hz
- LOWEST POSSIBLE COST PER CHANNEL
- MINIMUM PC BOARD SPACE
- 80% EFFICIENCY (8 CHANNELS, RATED LOADS)

APPLICATIONS

- INDUSTRIAL MEASUREMENT AND CONTROL
- DATA ACQUISITION SYSTEMS
- TEST EQUIPMENT

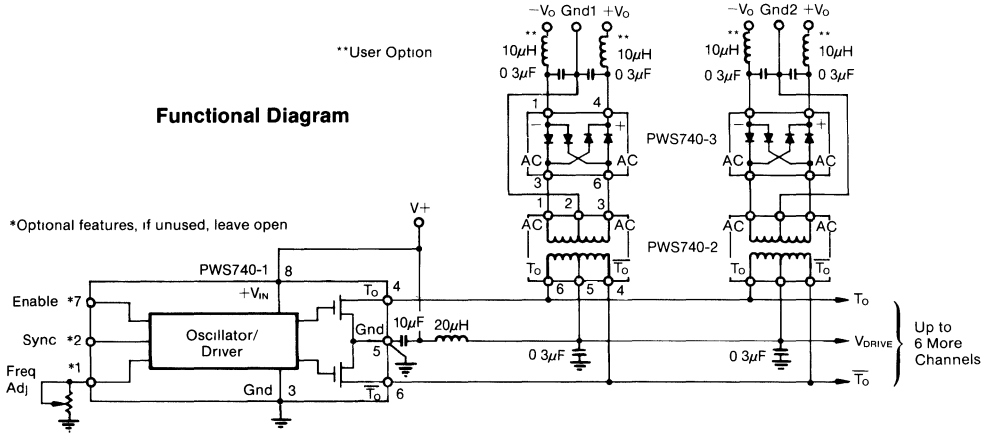
DESCRIPTION

The PWS740 is a multichannel, isolated DC-to-DC converter with a 1500VAC continuous isolation rating. The outputs track the input voltage to the converter over the range of 7 to 20VDC. The converter's modular design, comprising three components, minimizes the cost of isolated multichannel power for the user.

The PWS740-1 is a high-frequency (400kHz nominal) oscillator/driver, handling up to eight channels. This part is a hybrid containing an oscillator and two power FETs. It is supplied in a TO-3 case to provide the power dissipation necessary at full load. Transformer impedance limits the maximum input current to about 700mA at 15V input, well within the unit's thermal limits. A TTL-compatible ENABLE pin provides output shut-down if desired. A SYNC pin allows synchronization of several PWS740-1s.

The PWS740-2 is trifilar-wound isolation transformer using a ferrite core and is encapsulated in a plastic package, allowing a higher isolation voltage rating. The PWS740-3 is a high-speed rectifier bridge in a plastic 8-pin mini-DIP package. One PWS740-2 and one PWS740-3 are used per isolated channel.

Functional Diagram



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PDS-758B

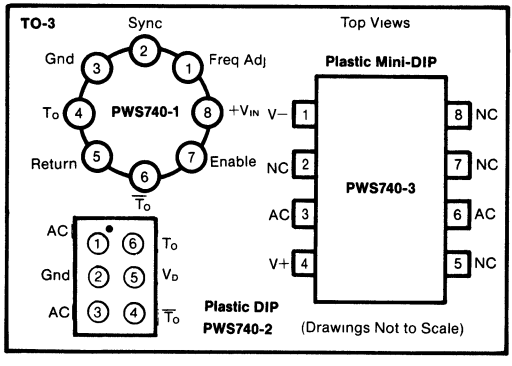
SPECIFICATIONS

ELECTRICAL

NOTE V_{IN} = 15V, output load on each of 8 channels = ±15mA, T_A = +25°C unless specified otherwise

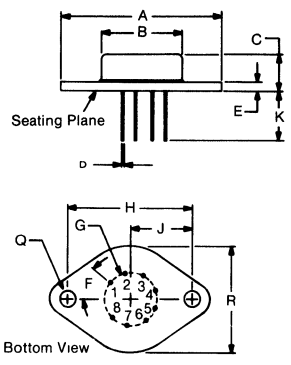
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
PWS740 SYSTEM					
ISOLATION					
Rated Voltage	Continuous, AC, 50/60Hz			1500	VACrms
	Continuous, DC			2121	VDC
Test Voltage	10s, minimum	4000			VACrms
Impedance	Measured from pin 2 to pin 5 of the PWS740-2		10^{12} || 3		Ω || pF
Leakage Current	240VACrms, 60Hz per channel		0 5	1 5	μA
INPUT					
Rated Voltage			15		VDC
Voltage Range		7		20	VDC
Current	±30mA output load on 8 channels, V_{IN} = 15V		520		mA
	Rated output load on 8 channels, V_{IN} = 15V		300		mA
Current Ripple	Full output load on 8 channels, V_{IN} = 15V with π filter on input		1		mA
OUTPUT					
Rated Voltage	±15mA output load on 8 channels	14 0	15 0	16 0	VDC
Voltage at Min Load	±1mA/channel		30		VDC
Voltage Range	±15mA output load on each channel	±7		±20	VDC
V_{OUT} vs Temp	±15mA output load on each channel		±0 05		V/°C
Load Regulation	±3mA < output load < ±30mA		0 25		V/mA
Tracking Regulation	V_{OUT}/V_{IN}		1 2		V/V
Ripple Voltage	See Typical Performance Curves				
Noise Voltage	See Theory of Operation				
Current $\|+I_{OUT}\| + \|-I_{OUT}\|$	Each channel			60	mA
TEMPERATURE					
Specification		−25		+85	°C
Operation		−25		+85	°C
PWS740-1 OSCILLATOR/DRIVER					
Frequency	V_{IN} = 15V	350	400	470	kHz
Supply		7 0	15 0	20 0	V
Enable	Drivers on	2 0		V_S	V
	Drivers off	0		0 8	V
PWS740-2 ISOLATION TRANSFORMER					
Isolation Test Voltage	10s, minimum	4000			VACrms
	60s, minimum	1500			VACrms
Rated Isolation Voltage	Continuous			1500	VACrms
Isolation Impedance			10^{12} || 3		Ω || pF
Isolation Leakage	240VAC		0 5	1 5	μA
Primary Inductance	400kHz, Pin 1 to Pin 5		300		μH
Winding Ratio	Primary/Secondary		68/76		
PWS740-3 DIODE BRIDGE					
Reverse Recovery	$I_F = I_R$ = 50mA		40		ns
Reverse Breakdown	I_R = 100μA	55			V
Reverse Current	V_R = 40V			1 5	μA
Forward Voltage	I_F = 100mA			1 6	V

PIN CONFIGURATIONS



MECHANICAL

TO-3

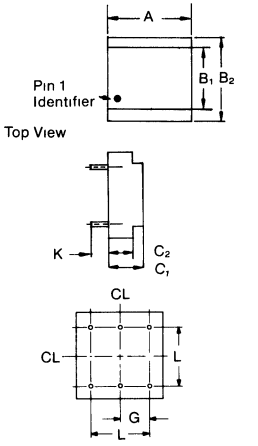


NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers may not be marked on package

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1 510	1 550	38 35	39 37
B	745	770	18 92	19 56
C	240	290	6 10	7 37
D	038	042	0 97	1 07
E	080	105	2 03	2 67
F	40° BASIC		40° BASIC	
G	500 BASIC		12 7 BASIC	
H	1 186 BASIC		30 12 BASIC	
J	593 BASIC		15 06 BASIC	
K	400	500	10 16	12 70
Q	151	161	3 84	4 09
R	980	1 020	24 89	25 91

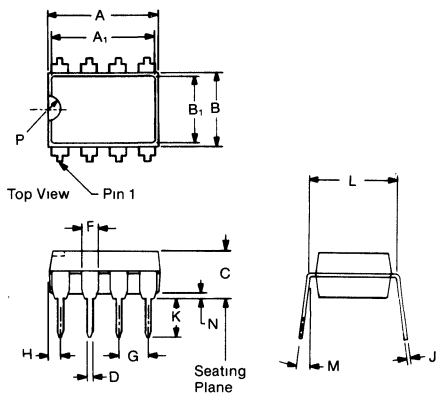
Plastic DIP



NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0 54	0 64	13 72	16 26
B_1	0 39	0 49	9 91	12 45
B_2	0 54	0 64	13 72	16 26
C_1	0 39	052	9 91	13 21
C_2	0 29	044	8 64	11 18
G	200 BASIC		5 08 BASIC	
K	0 11	0 21	2 79	5 33
G	400 BASIC		10 16 BASIC	

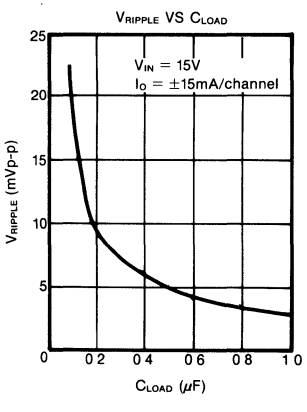
Plastic Mini-DIP

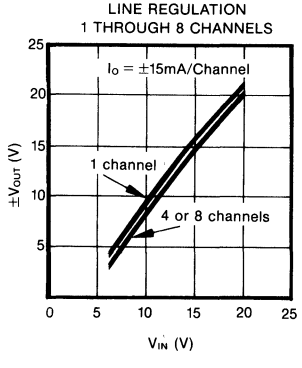


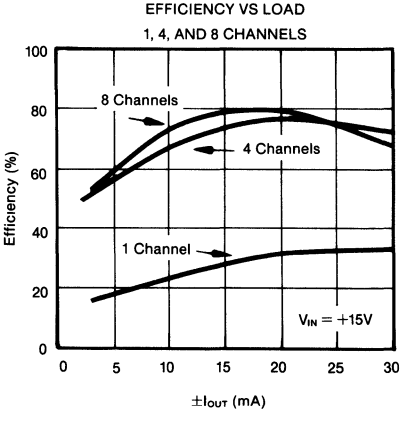
NOTE. Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	355	400	9 03	10 16
A_1	340	385	8 65	9 80
B	230	290	5 85	7 38
B_1	200	250	5 09	6 36
C	120	200	3 05	5 09
D	015	023	0 38	0 59
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	025	050	0 64	1 27
J	008	015	0 20	0 38
K	070	150	1 78	3 82
L	300 BASIC		7 63 BASIC	
M	0°	15°	0°	15°
N	010	030	0 25	0 76
P	025	050	0 64	1 27

TYPICAL PERFORMANCE CURVES

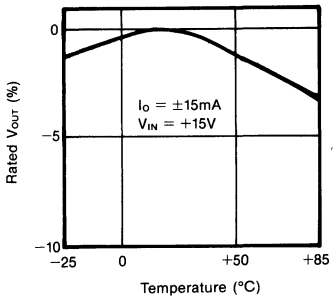




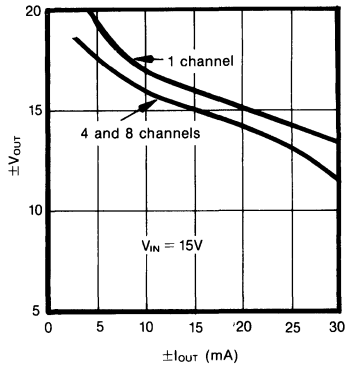


TYPICAL PERFORMANCE CURVES (CONT)

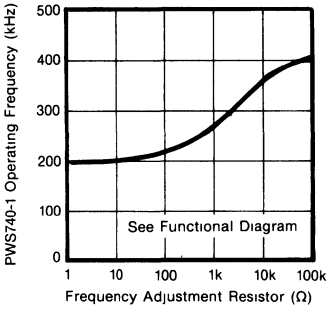
OUTPUT VOLTAGE DRIFT



LOAD REGULATION
1, 4 AND 8 CHANNELS



FREQUENCY ADJUSTMENT RANGE



PIN DESCRIPTIONS OF PWS740-1 DRIVER

$+V_{IN}$, RETURN, AND GND

These are the power supply pins. The ground connection, RETURN, for the N-channel MOSFET sources is brought out separately from the ground connection for the oscillator/driver chip. The waveform of the FETs' ground return current (and also the current in the V_{DRIVE} line) is an 800kHz sawtooth. A capacitor between $+V_{IN}$ and the FET ground provides a bypass for the AC portion of this current.

The power should never be instantaneously interrupted to the PWS740 system (i.e., a break in the line from V+, either accidental or by means of a series switch). Normal power-down of the V+ supply is not considered instantaneous. Should a rapid break in input power occur, however, the transformers' voltage will rapidly increase to maintain current flow. Such a voltage spike may damage the PWS740-1. The bypass capacitors at the $+V_{IN}$ pin of the PWS740-1 and the V_{DRIVE} pins of the transformers provide a path for the primary current if power is interrupted; however, total protection requires some type of bidirectional 1A voltage clamping at the $+V_{IN}$ pin. A low cost SA20A TransZorb® from General Semiconductor[1] or equivalent, which will clamp the $+V_{IN}$ pin between −.6V and +23V, is recommended.

T_O AND $\overline{T_O}$

These pins are the drains of the N-channel MOSFET switches which drive all the transformer primaries in parallel. The signals on these pins are 400kHz complementary square waves with twice the amplitude of the voltage at $+V_{IN}$. It is these lines that allow the power to be distributed to the individual high voltage isolation transformers. Without proper printed circuit board layout techniques, these lines could generate interference to analog circuits. See the next section on PCB layout.

ENABLE

A high TTL logic level on this pin activates the MOSFET driver circuitry. A low TTL level applied to the ENABLE pin shuts down all drive to the transformers and the output voltages go to zero (only the oscillator is unaffected). For continuous operation, the ENABLE pin can be left open or tied to a voltage between +2V and V+.

SYNCHRONIZATION

The SYNC pin is used to synchronize up to eight PWS740-1 oscillators. Synchronization is useful to prevent beat frequencies in the supply voltages. The SYNC pins of two or more PWS740-1s are tied together to force all units to the same frequency of oscillation. The resultant frequency is slightly higher than that of the highest unsynchronized unit. If this feature is not required, leave the SYNC pin open. The SYNC pin is sensitive to capacitance loading. 150pF or less is recommended. Also external parasitic capacitive feedback between either T_O and the SYNC pin can cause unstable operation (commonly seen as jitter in the T_O outputs). Keep SYNC connections and T_O lines as physically isolated as possible. Avoid shorting the SYNC pin directly to ground or supply potentials; otherwise, damage may result.

Figure 1 shows a method for synchronizing a greater number of PWS740-1 drivers. One unit is chosen as the master. Its synchronization signal, buffered by a high-speed unity gain amplifier can synchronize up to 20 slave units. Pin 1 of each slave unit must be grounded to assure synchronization. Minimize capacitive coupling between the buffered sync line and the outputs of the drivers, especially at the end of long lines. Capacitance to ground is not critical, but total stray capacitance between the sync line and switching outputs should be kept below 50pF. Where extreme line lengths are needed,

(1) General Semiconductor Industries Inc , 2001 W 10th Place, Tempe AZ 85281, 602-968-3101

TransZorb® General Semiconductor Industries Inc

such as between printed circuit boards, additional OPA633 buffers may be added to keep drive impedance at an acceptably low value. Because of temperature-influenced shifts in the switching levels, best operation of this circuit will occur when differences in ambient temperatures between the PWS740-1 drivers are minimized, typically within a 35°C range.

If larger temperature gradients are likely to occur, the user may wish to consider the synchronization method shown in Figure 2. This circuit is driven from an external TTL-compatible source such as a system clock or a simple free-running oscillator constructed of TTL gates. The output stage provides temperature compensation over the rated temperature range of the PWS740. The signal source frequency should be about 800kHz for rated performance, but may range from 500kHz to 2MHz with slightly reduced performance. Precautions with regard to circuit coupling and layout are the same as for the circuit of Figure 1. Repeaters using the OPA633 may be used for long line lengths. Symmetry and good high-frequency layout practice are important in successful application of both of these synchronization techniques.

FREQUENCY ADJUSTMENT

The FREQ ADJ pin may be connected to an external potentiometer to lower an unsynchronized PWS740-1 oscillator frequency. This may be useful if the frequency of the PWS740-1 is too close to some other signal's frequency in the system and beat interference is possible. See Typical Performance Curves. Use of this pin is not usually required; if not used, leave open for rated performance.

THEORY OF OPERATION

EXTERNAL FILTER COMPONENTS

Filter components are necessary to reduce the input ripple current and the output voltage noise. Without any input filtering, the sawtooth currents in the FET switches would flow in the V+ supply line. Since this AC current can be as great as 1A peak, voltage interference with other components using this supply line would likely occur. The input ripple current can be reduced to approximately 1mA peak with the addition of two components—a bypass capacitor between the $+V_{IN}$ pin and ground, and a series inductor in the V_{DRIVE} line. A 10μF tantalum capacitor is adequate for bypass. A parallel 0.33μF ceramic capacitor will extend the bandwidth of the tantalum. Additional bypass capacitors at each primary center-tap of the transformers are recommended. In general, the higher the capacitance, the lower the ripple, but the parasitic series inductance of the bypass capacitors will eventually be the limiting factor. The inductor value recommended is approximately 20μH. Greater reduction in ripple current is achieved with values up to 100μH; then physical size may become a concern. The inductor should be rated for at least 2A and its DC resistance should be less than 0.1Ω. An example of a low cost indicator is part number 51591 from Pulse Engineering[2].

Output voltage filtering is achieved with a 0.33μF capacitor connecting each V_{OUT} pin of the diode bridge to ground. Short leads and close placement of the capacitors to the unit provide optimum high frequency bypassing. The 800kHz output ripple should be below 5mVp-p. Higher frequency noise bursts are also present at the outputs. They coincide with the switch times and are approximately 20mV in amplitude. Inductance of 10μH or less in series with the output loads will significantly reduce the noise as seen by the loads.

PC BOARD LAYOUT CONSIDERATIONS

Multilayer printed circuit boards are recommended for PWS740 systems. Two-layer boards are certainly possible with satisfactory operation; however, three layers provide greater density and better control of interference from the FET switch signals. Should four-layer boards be required for other circuitry, the use of separate layers for power and ground planes, a layer for switching signals, and a layer for analog signals would allow the most straightforward layout for the PWS740 system. The following discussion pertains to a three- or four-layer board layout.

Critical consideration should go to minimizing electromagnetic radiation from the switching signal's lines, T_O and $\overline{T}_O$. You can identify the path of the switching current by starting at the $+V_{IN}$ pin. The dynamic component of the current is supplied primarily from the bypass capacitor. The high frequency current flows through the inductor and down the V_{DRIVE} line, through one side of the transformer windings, returning in the T_O

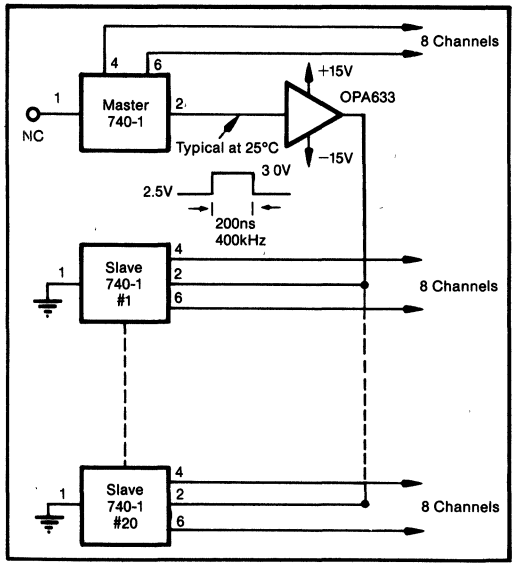


FIGURE 1. Master/Slave Synchronization of Multiple PWS740 Drivers.

(2) Pulse Engineering, PO Box 12235, San Diego CA 92112, 619-268-2400.

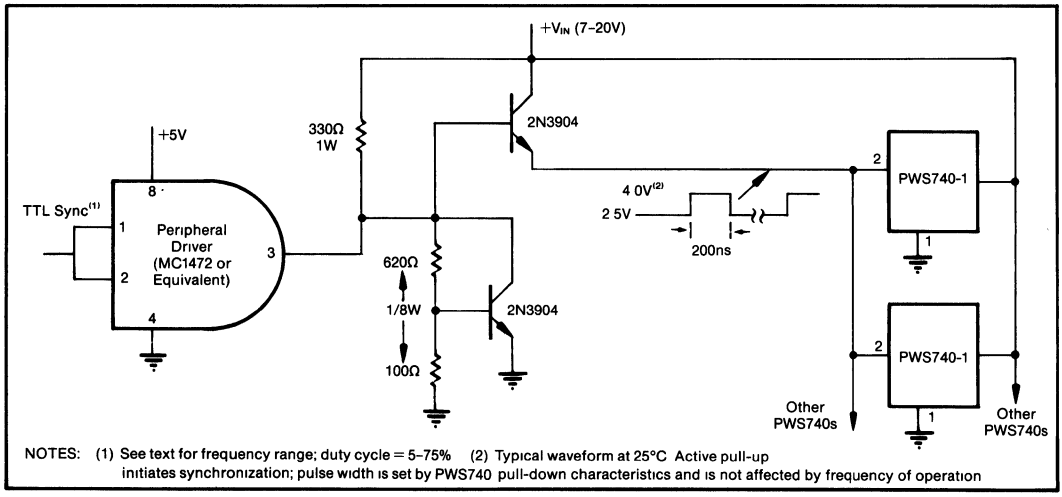


FIGURE 2. External Synchronization of Multiple PWS740 Drivers with TTL-Level Signals.

with the "on" FET switch, and then back up through the bypass capacitor. This current path defines a loop antenna which transmits magnetic energy. The magnetic field lines reinforce at the center of the loop, while the field lines from opposite points of the loop oppose each other outside the loop. Cancellation of magnetic radiation occurs when the loop is collapsed to two tightly spaced parallel line segments, each carrying the same current in opposite directions. For this reason, the printed circuit traces for both T_O connections should lay directly over a power plane forming the V_{DRIVE} connection. This plane need not extend much wider than T_O and $\overline{T_O}$. All of the current in the plane will flow directly under the T_O traces because this is the path of least inductance (and least radiation).

Another potential problem with the T_O lines is electric field radiation. Fortunately, the V_{DRIVE} plane is effective at terminating most of the field lines because of its proximity to these lines. Additional shielding can be obtained by running ground trace(s) along the T_O lines, which also facilitate minimum loop area connections for the transformer's center tap bypass capacitors.

The connections between the secondary (output side) of the transformer and the diode bridges should be kept as short as possible. Unnecessary stray capacitance on these lines could cause tuned circuit peaking to occur, resulting in a slight increase of output voltage.

The PWS740 is intended for use with the ISO102 isolation buffer (see Figure 3). Place the PWS740-2 transformer on the V_{OUT} side of the buffer rather than on the C_I (bandwidth control) side to prevent possible pickup of switch signal by the ISO102.

The best ground connection ties the ISO102 output analog common pin to the PWS740-1 ground pin with a ground plane. This is where a four-layer board design becomes convenient. The digital ground of the ISO102 can be connected to the ground plane or closer to the +V supply. If possible, you should include the analog components that the ISO102 drives on the same board. For example, if several ISO102s are mutliplexed to an analog/digital converter, then having all components sharing the same ground plane will signficantly simplify ground errors. Avoid connecting digital ground and the PWS740 ground together locally, leaving the ISO102 analog ground to be connected off of the board; the differential voltage between analog and digital ground may become too great.

OUTPUT CURRENT RATINGS

The PWS740-1 driver contains "soft-start" driver circuitry to protect the driver FETs and eliminate high inrush currents during turn-on. Because the PWS740 can have between one and eight channels connected, it was not possible to provide a suitable internal current limit within the driver. Instead, impedance-limiting protects the driver and transformer from overload. This means that the internal impedance of each PWS740-2 transformer is high enough that, when short-circuited at its output, it limits the current drawn from the driver to a safe value. In addition, the wire size and mass of the transformer are large enough that the transformer does not receive damage under continuous short-circuit conditions.

The PWS740-1 is capable of driving up to eight individual channels to their full current rating. The total current which can be drawn from each isolation channel is a function of total power being drawn from both DC V+ and V− outputs. For example, if one output is not used, then maximum current can be drawn from the other output. In all cases, the maximum total current that can be drawn from any individual channel is:

$$|I_L+| + |I_L-| \leq 60mA$$

It should be noted that many analog circuit functions do not simultaneously draw full rated current from both the

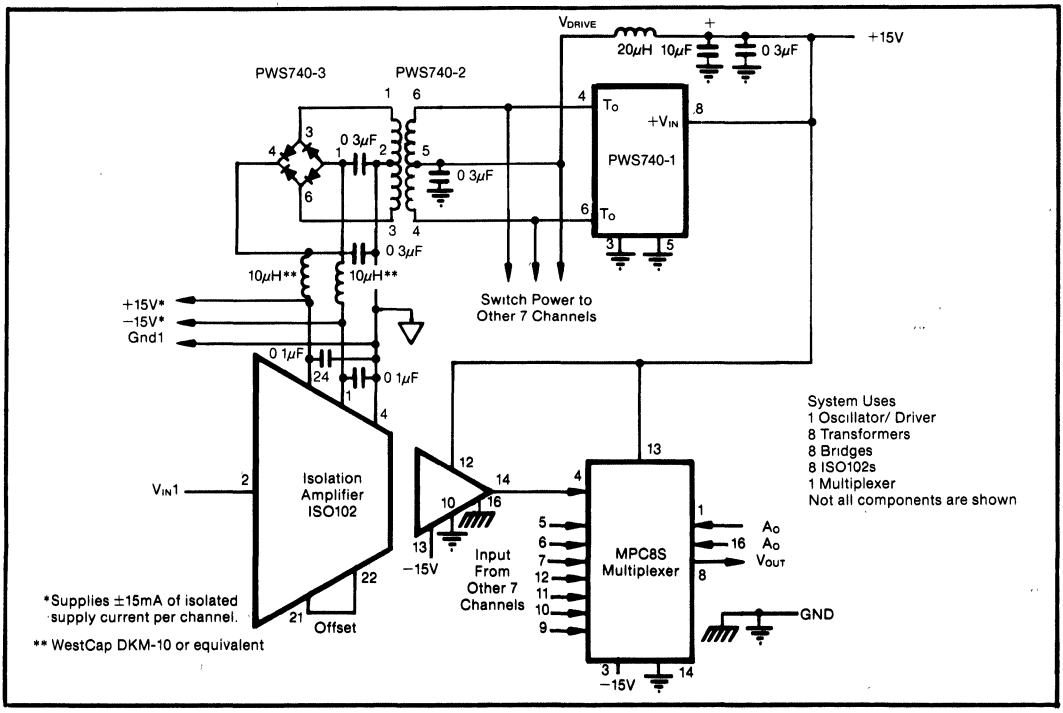


FIGURE 3. Low Cost Eight-Channel Isolation Amplifier Block with Channel-to-Channel Isolation.

positive and negative supplies. Thus, the PWS740 can power more circuits per channel than is first apparent. For example, an operational amplifier does not draw maximum current from both supplies simultaneously. If a circuit draws 10mA from the positive supply and 3mA from the negative supply, the PWS740 could power (60 ÷ 13) about four devices per channel.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter period of time. The relationship between actual test conditions and the continuous derated maximum specification is an important one. Burr-Brown has chosen a deliberately conservative one: $V_{TEST} = (2 \times V_{CONTINUOUS\ RATING}) + 1000V$. This choice is appropriate for conditions where system transient voltages are not well defined.[3] Where the real voltages are well-defined or where the isolation voltage is not continuous, the user may choose a less conservative derating to establish a specification from the test voltage.

(3) Reference National Electrical Manufacturers Association (NEMA) Standards part ICS I-109 and ICSI-111

BURR-BROWN®

PWS750 COMPONENTS

ADVANCE INFORMATION
SUBJECT TO CHANGE

Isolated, Unregulated DC/DC CONVERTER COMPONENTS

FEATURES

- 100% TESTED FOR HIGH-VOLTAGE BREAKDOWN
- COMPACT
- MULTICHANNEL OPERATION
- 5V OR 15V OPERATION

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL EQUIMENT
- GROUND-LOOP ELIMINATION
- PC-BASED DATA ACQUISITION
- VENDING MACHINES

DESCRIPTION

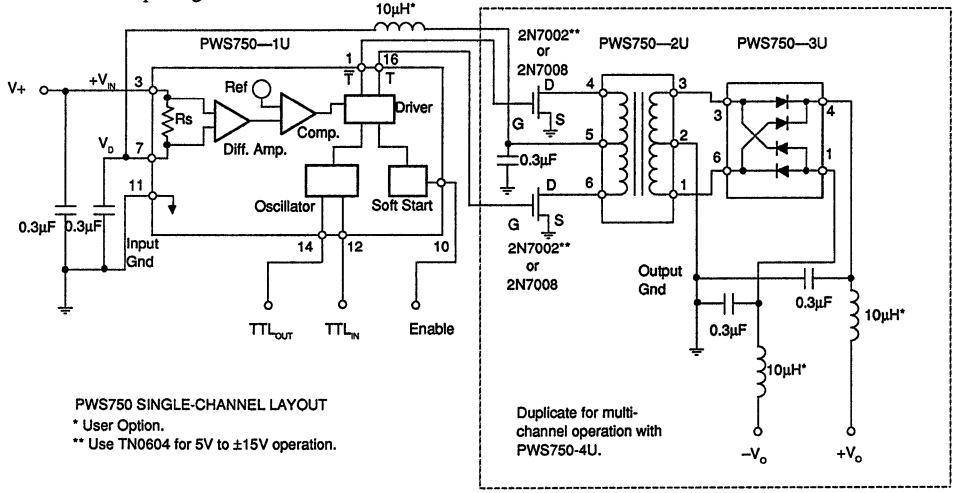
PWS750 components can be used to optimize the placement on a PC board or to build a multichannel isolated DC/DC converter. The parts are all surface mount, requiring minimal space to build the DC/DC converter. The modular design, comprising three components, minimizes the cost of isolated multichannel power.

PWS750-1U is a high-frequency (800kHz nominal) oscillator that can drive N-channel MOSFETs up to the size of a 1.3A 2N7010. The recommended MOSFET for individual transformer drives is the 2N7002, made by Siliconix. The PWS750-1U is supplied in a 16-pin double-wide SO package.

PWS750-2U and the PWS750-4U are bipolar-wound isolation transformers using a ferrite core and are encapsulated in plastic packages, allowing a higher isolation voltage rating.

The PWS750-3U is a high-speed rectifier bridge in a plastic 8-pin SO package.

One PWS750-2U and PWS750-3U and two 2N7002 or 2N7008 MOSFETs are used per isolated channel. When a PWS750-4U is used as the isolation transformer, then two TN0604s must be used, due to the higher currents in the primary.



PWS750 SINGLE-CHANNEL LAYOUT
* User Option.
** Use TN0604 for 5V to ±15V operation.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491 • FAX: (602) 889-1510

PDS-838

SPECIFICATIONS

ELECTRICAL

At T_A = 25°C; $+V_{IN}$ = +15V; and I_{OUT} = ±15mA balanced loads unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PWS750-1U OSCILLATOR					
Frequency	V_{IN} = 15V	725	800	875	kHz
Supply		10	15	18	V
	5V Operation	4.5	5	5.5	V
T, $\overline{T}$ Drive Current			50		mA peak
T, $\overline{T}$ Drive Voltage		3		7	V
PWS750-2U $+V_{IN}$ to $\pm V_{OUT}$ ISOLATION TRANSFORMER					
ISOLATION					
Voltage Rated Continuous AC 60Hz		1500			VAC
100% Test 1	1s, 5pC PD	2400			VAC
Barrier Impedance			10^{14} || 8		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms		1.0	1.5	µArms
Winding Ratio	Primary/Secondary		48/50		
PWS750-3U DIODE BRIDGE					
Reverse Recovery	If = Ir = 50mA		40		ns
Reverse Breakdown	Ir = 100µA	55			V
Reverse Current	Vr = 40V			1.5	µA
Forward Voltage	If = 100mA			1.6	V
PWS750-4U +5 V_{IN} TO ±15 V_{OUT} ISOLATION TRANSFORMER					
ISOLATION					
Voltage Rated Continuous AC 60Hz		1500			VAC
100% Test (1)	1s, 5pC PD	2400			VAC
Barrier Impedance			10^{14} || 8		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms		1.0	1.5	µArms
Winding Ratio	Primary/Secondary		24/76		

NOTES: (1) Tested at 1.6 X rated, fail on 5pC partial discharge leakage current on five successive pulses.

ORDERING INFORMATION

PWS750 X X

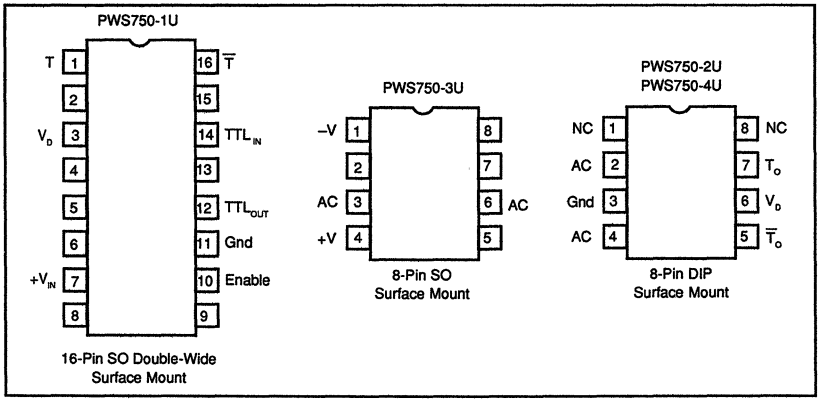
Basic Model Number

- PWS750-1U
- PWS750-2U
- PWS750-3U
- PWS750-4U

ABSOLUTE MAXIMUM RATINGS

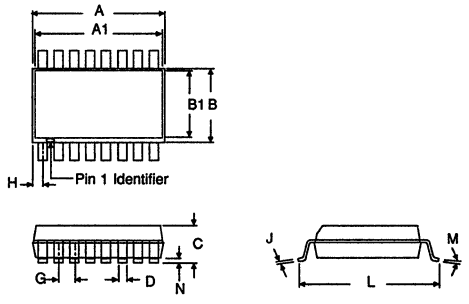
Supply Voltage	18V
Junction Temperature	150°C
Storage Temperature	85°C
Lead temperature (soldering, 10s)	+300°C
Max Load, Sum of Both Outputs (PWS750-2U, 4U)	60mA

PIN CONFIGURATIONS



MECHANICAL

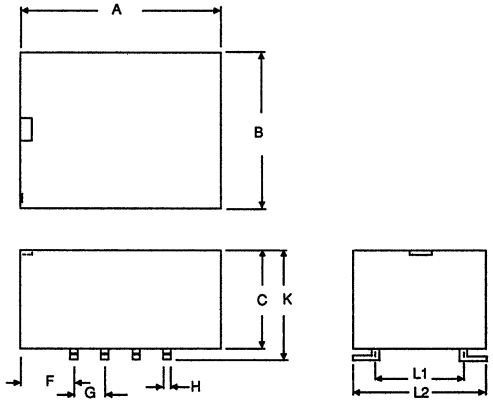
U Package—16-Pin SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.400	.416	10.16	10.57
A1	.388	.412	9.86	10.46
B	.286	.302	7.26	7.67
B1	.268	.286	6.81	7.26
C	.093	.109	2.36	2.77
D	.015	.020	0.38	0.51
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.391	.421	9.93	10.69
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

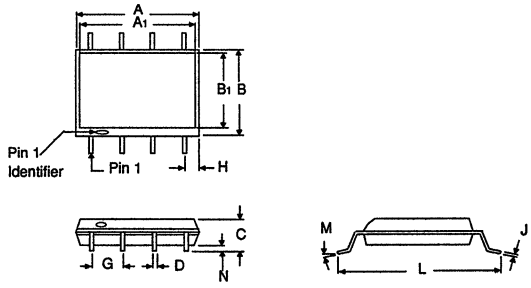
U Package—8-Pin DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.620	.640	15.78	16.26
B	.465	.485	11.81	12.32
C	.350	.370	8.89	9.40
F	.165	.185	4.19	4.70
G	.100 BASIC		2.54 BASIC	
H	.025 SQ		.635 SQ	
K	.370	.390	9.40	9.91
L1	.280	.300	7.11	7.62
L2	.465	.485	11.81	12.32

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

U Package—8-Pin SOIC



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.201	4.70	5.11
A1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

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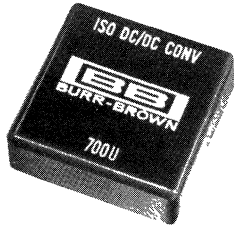


700/700U

ISOLATED DC-TO-DC CONVERTER

FEATURES

- HIGH BREAKDOWN VOLTAGE 5000V PEAK
- LOW LEAKAGE CAPACITANCE ≈ 3pF
- SHIELDED AND UNSHIELDED UNITS
- COMPLETELY SPECIFIED

APPLICATIONS

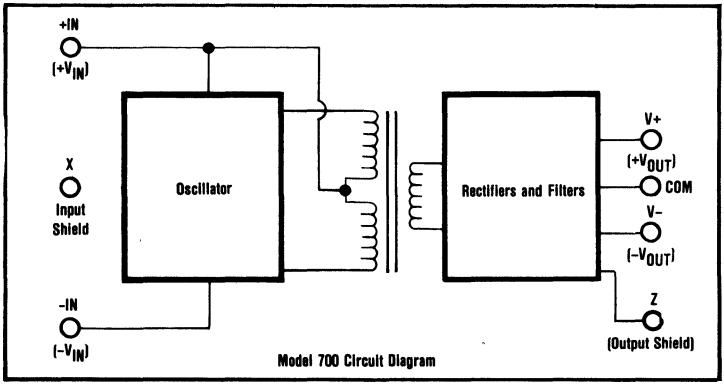
- INDUSTRIAL PROCESS CONTROL
- MEDICAL INSTRUMENTATION
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS

BENEFITS

- HIGH VOLTAGE RATING PROTECTS EXPENSIVE INSTRUMENTATION
- LOW LEAKAGE CURRENT PROTECTS HUMAN LIFE
- EXCELLENT ISOLATION CMR IMPROVES SYSTEM PERFORMANCE
- SHIELDING PREVENTS ELECTROSTACTIC AND EMI PROBLEMS

DESCRIPTION

The Model 700 converts a 10VDC to 18VDC input to a dual output of the same value as the input voltage. The internal hybrid integrated circuit reduces size and cost. A self-contained frequency stable 130kHz oscillator drives switching circuitry which is designed to minimize the common problem of spiking due to transformer saturation. Regulation and short circuit protection, if desired, can easily be added (see Figure 3). Models 700 and 700M have separate internal input and output shields. Models 700U and 700UM have no internal shields.



Model 700 Circuit Diagram

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PDS-328F

SPECIFICATIONS

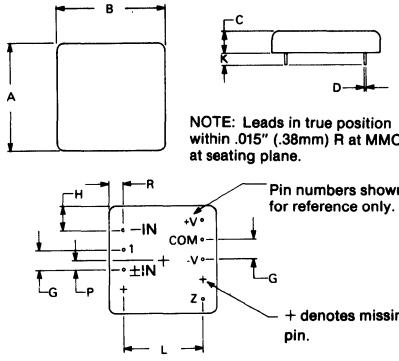
ELECTRICAL

Typical at 25°C with 15VDC supply unless otherwise noted.

MODEL	700/700M	700U/700UM
INPUT		
Voltage Range(1)	10V to 18V	
Current at ±3mA Load	20mA	
Current at ±30mA Load	±100mA, max	
Ripple Current at ±3mA Load	±3mA, peak	
Ripple Current at ±30mA Load	±100mA, peak	
ISOLATION(2)		
Voltage, Test, 5sec at 60Hz	4200V, p	5000V, p
Voltage, Continuous, derated	1500V, p	2000V, p
Impedance	10GΩ ‖ 5pF	10GΩ ‖ 3pF
Leakage Current at 240V/60Hz	1μA, max	1μA, max
OUTPUT		
V_{OUT} at ±3mA to ±30mA Load	$\pm V_{IN}$ with ±1V tolerance	
Operating Current total of both outputs	60mA, max	
Safe Nondestructive Current at 25°C	120mA, max	
Sensitivity to Input Voltage	1 08V/V	
Load Regulation	35mV/mA	
Ripple Voltage at ±3mA Load	±15mV, peak	
Ripple Voltage at ±30mA Load	±80mV, peak max	
Balance of +V and -V at +I = -I	±20mV	
TEMPERATURE RANGE		
Operating	-25°C to +85°C	
Storage	-55°C to +125°C	

NOTES.
1 Derate to 16V max between $+V_{IN}$ and $-V_{IN}$ above 70°C
2 A medical grade unit is available which is 100% screened to Patient Connected Circuit requirements for the leakage current (par. 27.5) and dielectric withstand voltage (par 31 11) of UL544 Specify 700M or 700UM.

MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1 075	1 135	27 31	28 83
B	1 075	1 135	27 31	28 83
C	350	410	8 89	10 41
D	038	042	0 97	1 07
G	200 BASIC		5 08 BASIC	
H	212	312	5 38	7 92
K	.170	350	4 32	8 89
L	800 BASIC		20 32 BASIC	
P	100 BASIC		2 54 BASIC	
R	112	212	2 84	5 38

Material: Black epoxy
Weight: 22.67gm (0.80oz)
Grid: 2.50mm (0.10")

NOTE: Input and Output circuits have separate shields.

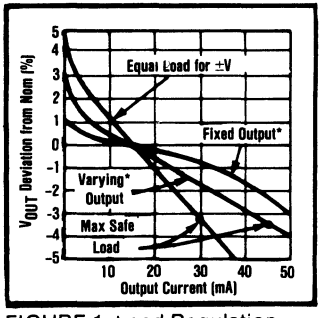


FIGURE 1. Load Regulation.

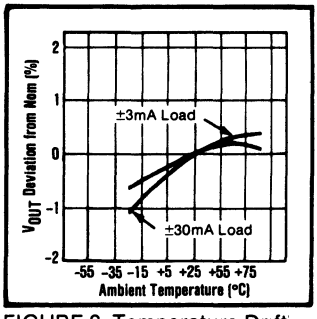


FIGURE 2. Temperature Drift.

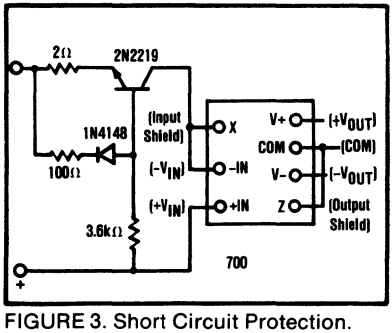


FIGURE 3. Short Circuit Protection.

*For one output with constant 15mA load and varying current on other output (A minimum load of 3mA is recommended for each output)

USE WITH ISOLATION AMPLIFIERS:

When the Model 700/700U is used with isolation amplifiers such as the Burr-Brown 3650 and 3652 special attention should be given to current ratings to avoid over designing. Since the isolation amplifiers do not draw maximum current simultaneously from the V+ and V− Model 700/700U terminals, it is possible to drive more isolation amplifiers per Model 700/700U than one might initially expect. The Model 700/700U is capable of providing a total output current of 60mA balanced or unbalanced between the two outputs. A minimum load of 3mA is recommended for each output.

BURR-BROWN

710

QUAD-ISOLATED DC-TO-DC CONVERTER

FEATURES

- FOUR ISOLATED ±10VDC to ±18VDC OUTPUTS
- DRIVES FOUR 3650/3652 ISOLATION AMPS
- HIGH BREAKDOWN VOLTAGE, 2200VDC TEST
- LOW LEAKAGE CAPACITANCE, 8pF
- LOW LEAKAGE CURRENT, 1μA @ 240V/60Hz
- LOW COST PER ISOLATED CHANNEL

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS

DESCRIPTION

The Model 710 converts a single 10VDC to 18VDC input into four dual-isolated outputs of the same value as the input voltage. The converter is capable of providing a total of 76mA at rated output voltage accuracy and can provide isolated power to four independently isolated 3650/3652 optically-coupled isolation amplifiers with the entire assembly mounted on one 5" x 7" card.

Extensive use is made of hybrid integrated circuits to reduce size and cost. A self-contained frequency stable 130kHz oscillator drives switching circuitry which is designed to minimize the common problem of spiking due to transformer saturation.

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PDS-367A

DESCRIPTION

OUTPUT CURRENT RATINGS

The Model 710 is capable of providing a total of 76mA of output current divided among its eight outputs. The maximum current available from any one output is shown in Figure 9. A minimum average current of 3mA is recommended for each output in order to maintain output voltage accuracy. Thus, the current may be balanced (such as +9.5mA and -9.5mA) or unbalanced (such as +16mA and -3mA). The best output voltage accuracy will be obtained under balanced conditions.

Channels may be connected in series or parallel for higher voltage or current. For parallel operation connection of channel 1 to 2 or channel 3 to 4 will result in lowest ripple.

In some cases the 710 may drive larger loads than would be apparent from a cursory examination of the specifications. For example, see Figures 1 and 2. The most total current drawn from the pair of $+V_o$ and $-V_o$ output is $I_{max} + I_Q$ (not 2 x I_{max}). For the 3650 this is a maximum of 12mA +1.2mA = 13.2mA (instead of 24mA).

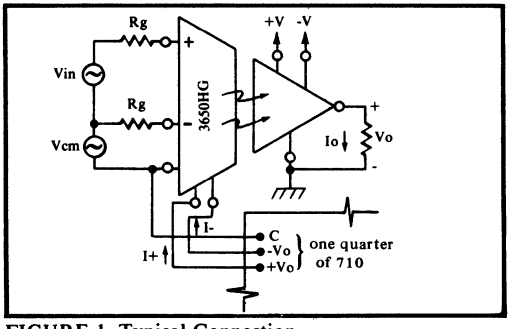


FIGURE 1. Typical Connection

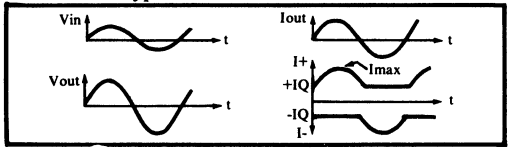


FIGURE 2. Waveforms

ISOLATION VOLTAGE RATINGS

It is important that the user understand the significance of the continuous derated isolation voltage specification and its relationship to the actual test voltage applied to the unit. Since a "continuous" test is impractical in a product manufacturing situation (implies infinite test duration) it is generally accepted practice to perform a production test at a higher voltage (i.e., higher than the continuous rating) for some shorter length of time.

The important consideration is then "what is the relationship between actual test conditions and the continuous derated minimum specification?" There are several rules of thumb used throughout the industry to establish this relationship. Burr-Brown has chosen a very conservative one: $V_{test} = (2 \times V_{continuous\ rating}) + 1000V$. This relationship is appropriate for conditions where the system transient voltages are not well defined.* Where the real voltages are well defined or where the isolation voltage is not continuous the user may choose to use a less conservative derating to establish a specification from the test voltage.

* Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS I-109 and ICS I-111.

SHORT CIRCUIT PROTECTION

The circuit in Figure 3 may be added to the input of the 710 in order to protect it from damage in situations where too much current is demanded from the outputs – such as a short circuit from an output to its common. The circuit limits the input current to approximately 100mA for an input voltage of 15VDC (for β of 2N2219 of 50).

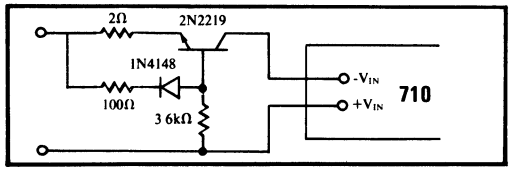


FIGURE 3. Short Circuit Protection

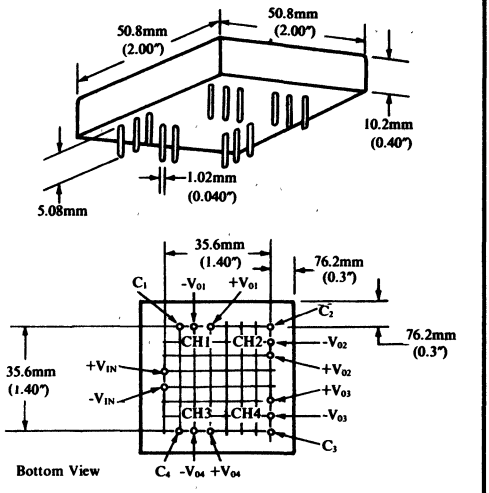
SPECIFICATIONS

Typical at 25°C with 15V supply unless otherwise noted.

ELECTRICAL

MODEL	710
INPUT	
Voltage Range[1][2]	10V to 18V
Current at Total Output Current of 24mA	40mA
Current at Total Output Current of 76mA	100mA, max.
Ripple at Total Output Current of 24mA	15mA, peak
Ripple at Total Output Current of 76mA	40mA, peak
ISOLATION[3]	
Voltage, Test, 5 sec.[4]	2200V, rms at 60Hz
Voltage, Continuous, derated, minimum[4]	600V, rms AC, 1000VDC
Impedance	10GΩ || 8pF
Leakage Current at 240V/60 Hz	1μA, max
OUTPUT	
Voltage Accuracy[5]	See Figure 8
Current for Rated Accuracy Total of all currents	76mA, max
Any one output	60mA, max
Total Safe Nondestructive Current at 25°C	1200mA, max
Sensitivity to Input Voltage	1.08V/V
Load Regulation[6]	75mV/mA
Ripple Voltage at ±3mA Load	±25mV, peak
Ripple Voltage at ±9.5mA Load	±80mV, peak max
Balance of +V and -V at +I = -I	±20mV
ΔV_{out} vs Temperature -25°C to +85°C	3.0%
TEMPERATURE RANGE	
Operating	-25°C to +85°C
Storage	-55°C to +110°C

MECHANICAL



Material: Black Epoxy
Weight: 25 grams (0.9 oz.)
Grid: 5.08mm (.20")
Pin: Material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

NOTES
1. Derate to 16V max between $+V_{IN}$ and $-V_{IN}$ above 70°C.
2. Operation down to 5V is possible with reduced output current and accuracy.
3. Isolation specifications are applicable to input to output isolation as well as channel to channel isolation.
4. See discussion on previous page; 2200V, rms ≃ 3000V peak.
5. A minimum output current of ±3mA per channel is recommended to maintain output voltage accuracy.
6. Load regulation for one channel with other channels at ±9.5mA load.

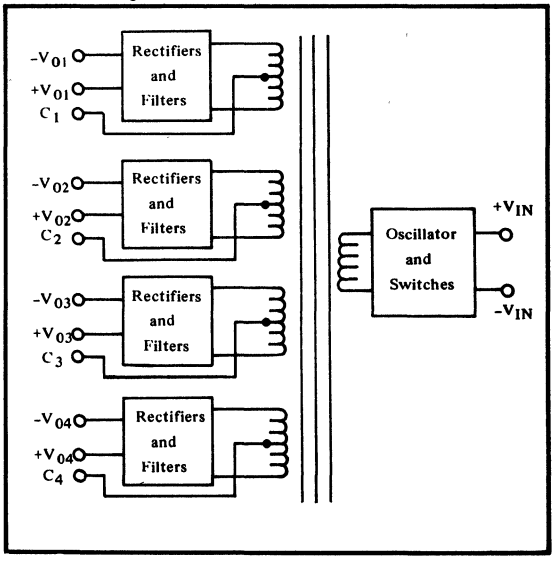


FIGURE 4. Functional Diagram

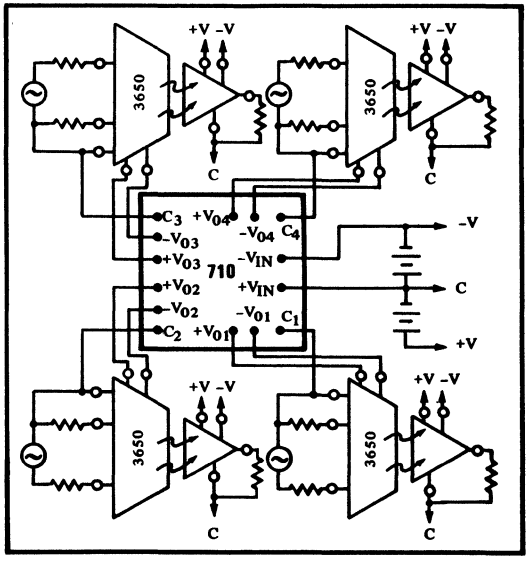


FIGURE 5. Typical Connection with Four 3650 Isolation Amplifiers.

TYPICAL PERFORMANCE CURVES

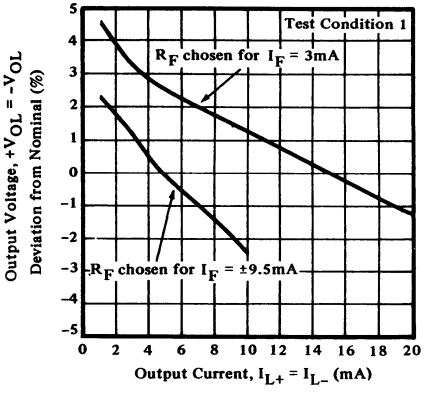


FIGURE 6. LOAD REGULATION - Balanced Load

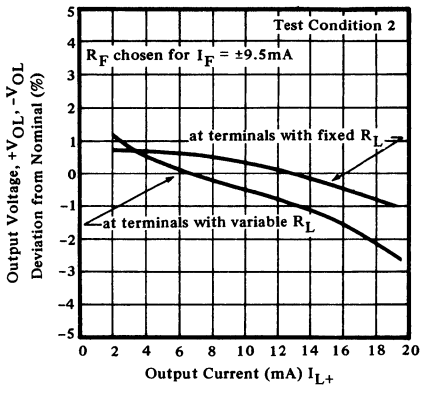


FIGURE 7. LOAD REGULATION - Unbalanced Load

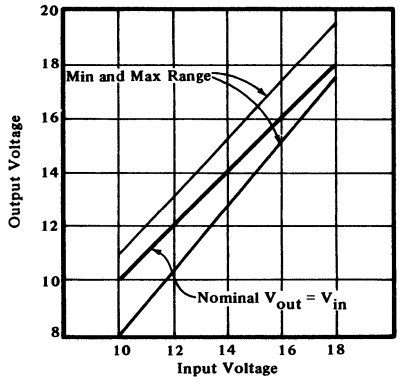


FIGURE 8. OUTPUT VOLTAGE ACCURACY VS INPUT VOLTAGE

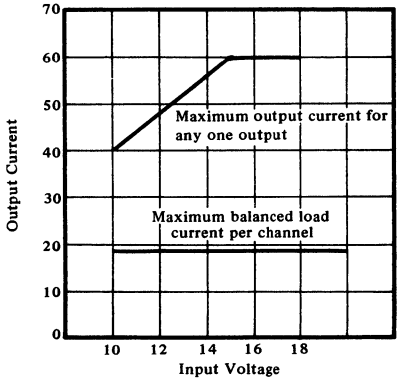


FIGURE 9. OUTPUT CURRENT RATINGS TO MAINTAIN OUTPUT VOLTAGE TOLERANCE

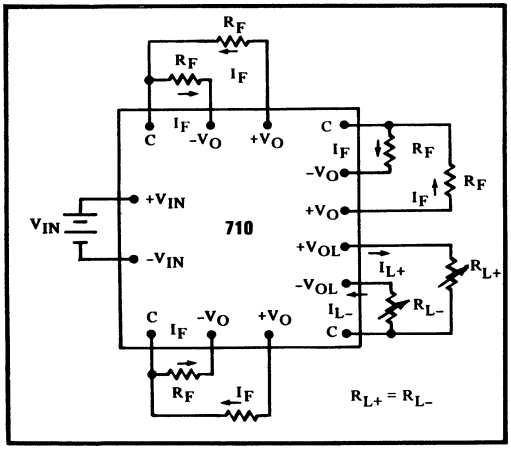


FIGURE 10. Test Condition 1: Balanced Load

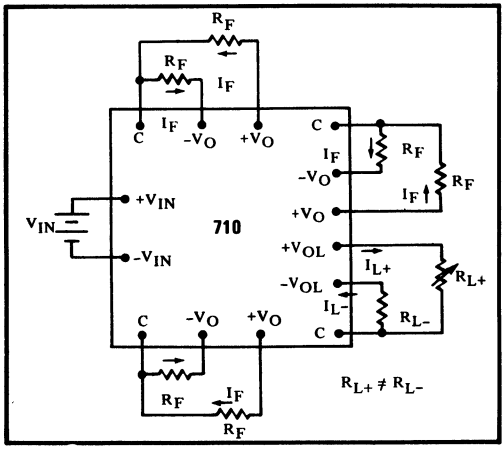


FIGURE 11. Test Condition 2: Unbalanced Load

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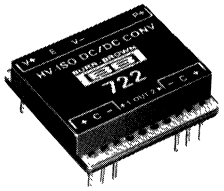


722

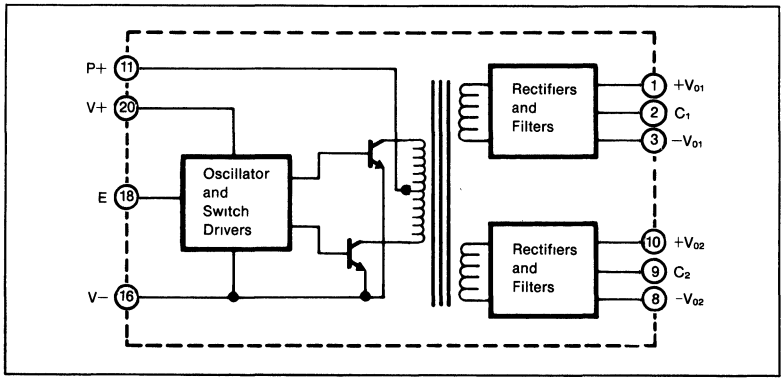
DUAL ISOLATED DC/DC CONVERTER

FEATURES

- DUAL ISOLATED ±5V TO ±16V OUTPUTS
- HIGH BREAKDOWN VOLTAGE, 8000V TEST
- LOW LEAKAGE CURRENT, <1μA AT 240V/60Hz
- LOW COST PER ISOLATED CHANNEL
- SMALL SIZE, 27.9mm x 27.9mm x 7.6mm (1.1" x 1.1" x 0.3")

APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS
- NUCLEAR INSTRUMENTATION



DESCRIPTION

The 722 converts a single 5VDC to 16VDC input into a pair of bipolar output voltages of the same value as the input voltage. The converter is capable of providing a total output current of 64mA at rated voltage accuracy and up to 200mA without damage.

The two output channels are isolated from the input and from each other. They may be connected independently, in series for higher output voltage or in parallel for higher output current, as a single channel isolated DC/DC converter.

Integrated circuit construction of the 722 reduces size and cost. High isolation breakdown voltages and low leakage currents are assured by special design and construction which includes use of a high dielectric strength, low leakage coating used on the internal assembly.

A self-contained 900kHz oscillator drives switching circuitry which is designed to eliminate the common problem of input current spiking due to transformer saturation or crossover switching.

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PDS-398E

DISCUSSION

OUTPUT CURRENT RATINGS

At rated output voltage accuracy, the 722 is capable of providing 64mA divided among its four outputs[1]. A minimum average output current of 3mA is recommended at each output to maintain voltage accuracy.

Output channels[2] may be connected in series or parallel for higher output voltage or current.

ISOLATION CONFIGURATIONS

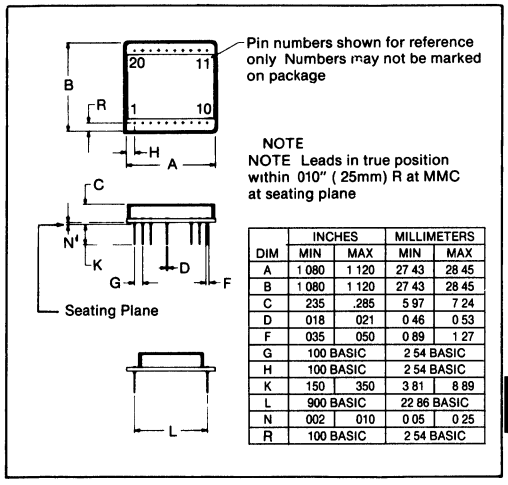
The fact that the two outputs of the 722 are isolated from the input and from each other allows both two-port and three-port isolation connections.

Figure 1 shows Burr-Brown's 3650 Optically Coupled Isolation Amplifier connected in three-port configuration. One of the 722 channels provides power to the 3650's input. The other channel supplies power to the 3650's output. The amplifier's input and output are isolated from each other and the system's power supply common. In this configuration the 722's channel-to-channel isolation specification applies to the amplifier input-to-output voltage.

Figure 3 illustrates how the 722 may provide isolated input power to the input stage of two 3650's connected in the two-port configuration. Power for the output stage is provided by the system +15V and -15V supplies. Input stages are isolated from each other and from the system supply. In this situation the 722's input-to-output isolation specification applies to the amplifiers' input-to-output voltages while the channel-to-channel 722 specification applies to the voltage existing between "I/P Com # 1" and "I/P Com # 2."

(1) "output" denotes a single output terminal (+V or -V) and its associated common
(2) "channel" denotes a pair of outputs (+V and -V) and their associated common

MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1 080	1 120	27 43	28 45
B	1 080	1 120	27 43	28 45
C	235	.285	5 97	7 24
D	018	021	0 46	0 53
F	035	050	0 89	1 27
G	100 BASIC		2 54 BASIC	
H	100 BASIC		2 54 BASIC	
K	150	350	3 81	8 89
L	900 BASIC		22 86 BASIC	
N	002	010	0 05	0 25
R	100 BASIC		2 54 BASIC	

SHORT CIRCUIT PROTECTION

The circuit in Figure 2 may be added to the input of the 722 to protect it from damage in situations where too much current is demanded from the outputs - such as a short circuit from an output to its common. The circuit limits input current to approximately 150mA for an input voltage of 15VDC (for β of 2N2219 of 50).

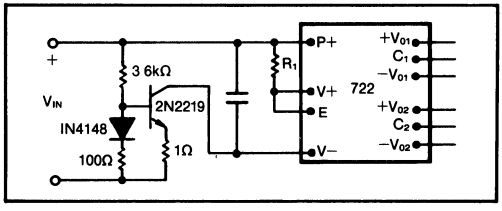


FIGURE 2. Short Circuit Protection

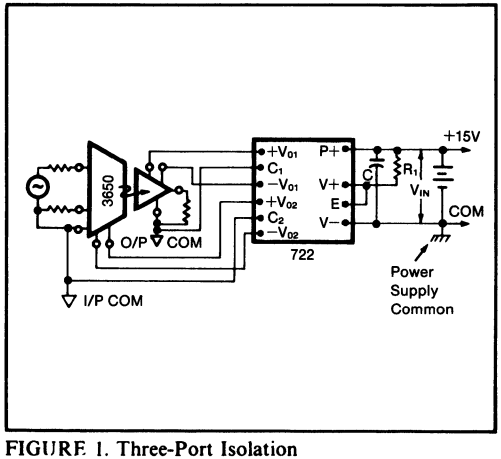


FIGURE 1. Three-Port Isolation

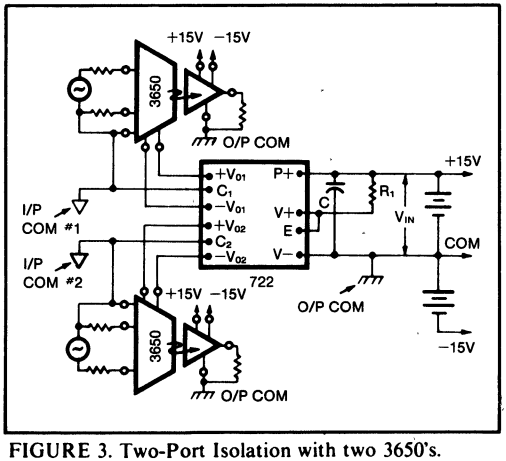


FIGURE 3. Two-Port Isolation with two 3650's.

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C, V_{IN} = 15VDC, C = 0.47μF, R_1 Selected per Typical Performance Curve.

PARAMETER	CONDITIONS	722			722BG			722MG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
Rated Input Voltage			15			*			*		VDC
Input Voltage Range[1]		5		16	*		*	*		*	VDC
Input Current	Total output current = 12mA		50			*			*		mA
	Total ouput current = 64mA		105	120		*	*		*	*	mA
	Total output current = 64mA at T_A = +85°C		120			*			*		mA
	Total output current = 160mA		—	—		225	275		—	—	mA
Input Ripple[2]	Total output current = 12mA		3			*			*		mA,pk
	Total output current = 64mA		6			*			*		mA,pk
	Total output current = 160mA		—			12			—		mA,pk
ISOLATION											
Test Voltages	Input-to-output, 5 seconds, min			8000			*			*	V,pk
	Input-to-output, 1 minute, min			—			—			2500	V,rms
	Channel-to-channel, 5 seconds, min			5000			*			*	V,pk
Rated Voltages	Input-to-output, continuous			3500			*			*	V
	Channel-to-channel, continuous			2000	*		*			*	V
Isolation Impedance	Input-to-output		10‖6			*			*		GΩ‖pF
Leakage Current[3]	Input-to-output, 240V, 60Hz			1			*			*	μA
OUTPUT											
Rated Output Voltages[4]	I_{LOAD} = 3mA per output	15 4		16 2	*		*	*		*	VDC
	I_{LOAD} = 16mA per output	14 3		16 2	*		*	*		*	VDC
	I_{LOAD} = 40mA per output	—	—	—	13 7	14.2	16.2	—	—	—	VDC
Output Current	Total of all outputs			200			*			*	mA
	Any one output[5]	3		100	*		*	*		*	mA
Load Regulation			Note 5			*			*		
Ripple Voltage	I_{LOAD} = 3mA per output		15			*			*		mV,pk
	I_{LOAD} = 16mA per output		35	100		*	*		*	*	mV,pk
	I_{LOAD} = 40mA per output		—			50			*		mV,pk
Tracking Error between Dual Outputs	Balanced loads		±100			*			*		mVDC
Sensitivity to Input Voltage Changes			1 13			*			*		V/V
Output Voltage Temperature Coefficient	$T_A = T_{SPECIFICATION\ RANGE}$		±0 02			*			*		%/°C
TEMPERATURE											
Specification	$I_{LOAD} \leq$ 16mA per output	−25		+85	*		*	*		*	°C
	$I_{LOAD} \leq$ 40mA per output	−25		+60	*		*	*		*	°C
Storage		−55		+125	*		*	*		*	°C
Junction Temperature				+125			*			*	°C

*Specifications same as 722

NOTES: (1) For ambient temperature above +70°C the input voltage is 12 5V (max) The input voltage remains 16V (max.) if case temperature is kept below +85°C. (2) External capacitor across "P+" to "V−" pins and 12" of #24 wire to V_{IN} (3) Reference UL544, paragraph 27 5, Leakage Current (4) See "Typical Performance Curves." (5) A minimum output current of 3mA at each output is recommended to maintain output voltage accuracy.

INSTALLATION AND OPERATING INSTRUCTIONS

Typical application connections for the 722 are shown in Figures 1 and 3. Primary power (V_{IN}) is applied at the "P+" and "V−" terminals. The common or ground for V_{IN} may be connected to either "P+" or "V−"; the only requirement is that "P+" and "V+" must be positive with respect to "V−."

Power for the internal oscillator and switch drivers is derived from the primary power by a voltage dropping resistor R_1. The value of R_1 as a function of V_{IN} is shown in the Typical Performance Curves section. Alternately, voltage for the "V+" terminal may be obtained from a separate source. "V+" should be +5V to +7.5V positive with respect to "V−." If a separate source is used, the "V+" input must be applied before the "P+" input to avoid possible damage to the unit. "P+" and "V+" must remain positive with respect to "V−" at all times (including transients). If necessary, diode clamps should be put across these inputs.

The "E" pin enables the converter when connected to "V+" and disables it when connected to "V−."

An external capacitor, "C," (0.47μF cermanic) is used to reduce input ripple. It should be connected as close to the "P+" and "V−" pins as practical. Input leads to these terminals should also be kept as short as possible. Since the 722 is not internally shielded, external shielding may be appropriate in applications where RFI at the 900kHz nominal oscillator frequency is a problem.

Each output is filtered with an internal 0.22μF capacitor. Output ripple voltage can be reduced below the specified value by adding external capacitors up to 10μF between each output and its common.

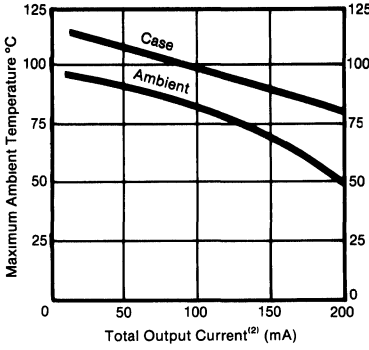
TYPICAL PERFORMANCE CURVES

Specifications at T_A = +25°C. V_{IN} = 15VDC. C = 0.47µF. R_1 selected per typical performance curve.

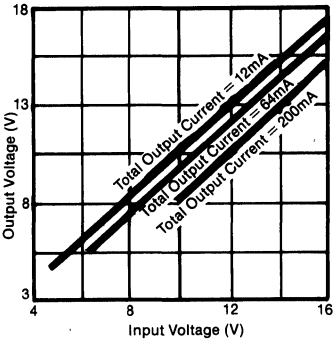
SELECTION OF R_1 OR EXTERNAL VOLTAGE V+ FOR MINIMUM INTERNAL POWER DISSIPATION

Input Voltage (V)	Maximum Output Current From Any Single Output		
	<16mA	16mA to 30mA	30mA
>13	1.3kΩ	820Ω	510Ω
11 to 13	820Ω	510Ω	200Ω
9 to 11	510Ω	200Ω	0Ω
8 to 9	200Ω	0Ω	—
<8	0Ω	—	—
→ $V+_{EXT}$	6.5V	7.5V	9.0V

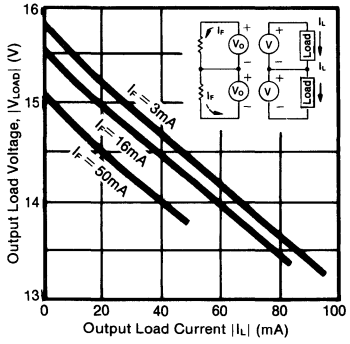
MAXIMUM SAFE OPERATING TEMPERATURE VS. TOTAL OUTPUT CURRENT



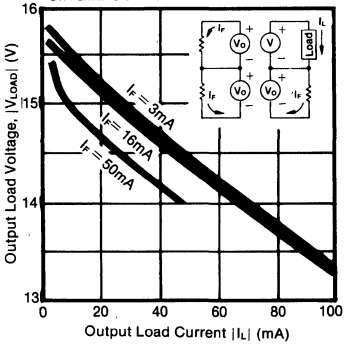
OUTPUT VOLTAGE VS. INPUT VOLTAGE



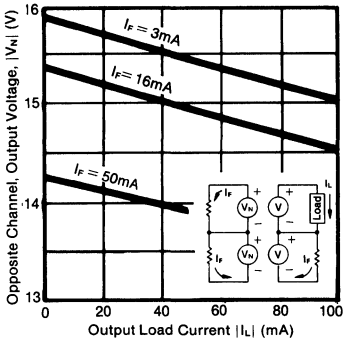
SINGLE-CHANNEL LOAD REGULATION



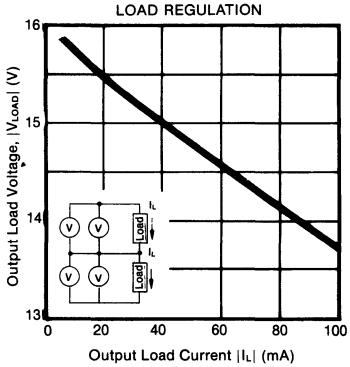
SINGLE OUTPUT LOAD REGULATION



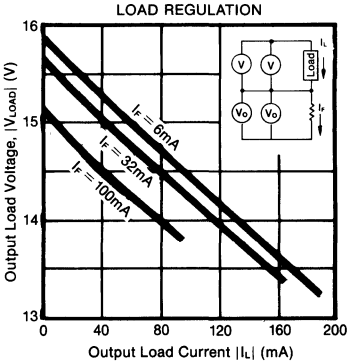
CHANNEL-TO-CHANNEL INTERACTION



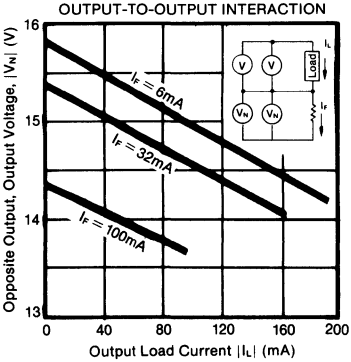
PARALLEL OUTPUT BALANCED LOAD REGULATION



PARALLEL OUTPUT UNBALANCED LOAD REGULATION



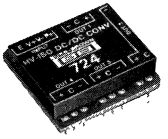
OUTPUT-TO-OUTPUT INTERACTION



NOTES (1) Using a 104mm × 19mm × 1.6 mm aluminum strip mounted to the bottom of the case with heat sink compound (2) Total output current is the sum of the currents for each individual output

BURR-BROWN®

724



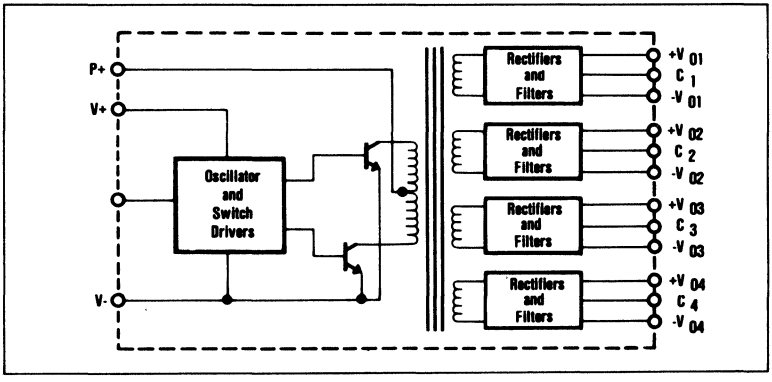
QUAD ISOLATED DC/DC CONVERTER

FEATURES

- QUAD ISOLATED ±8V OUTPUTS
- HIGH BREAKDOWN VOLTAGE, 3000V TEST
- LOW LEAKAGE CURRENT, <1μA AT 240V/60Hz
- LOW COST PER ISOLATED CHANNEL
- SMALL SIZE, 27.9mm x 27.9mm x 6.6mm (1.1" x 1.1" x 0.26")

APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS
- NUCLEAR INSTRUMENTATION



DESCRIPTION

The 724 converts a single 5VDC to 16VDC input into four pairs of bipolar output voltages of approximately half the input voltage. The converter is capable of providing a total output current of 128mA at rated voltage accuracy and up to 500mA without damage.

The four output channels are isolated from the input and from each other. They may be connected independently, in series for higher output voltage, or in parallel for higher output current as a single channel isolated DC/DC converter.

Integrated circuit construction of the 724 reduces size and cost. High isolation breakdown voltages and low leakage currents are assured by special design and construction which includes use of a high dielectric strength, low leakage coating used on the internal assembly.

A self-contained 800kHz oscillator drives switching circuitry which is designed to eliminate the common problem of input current spiking due to transformer saturation or crossover switching.

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PDS-405A

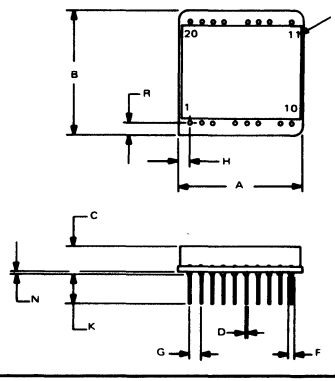
ELECTRICAL SPECIFICATIONS

At 25°C with V_{IN} = 15V, R_L = 1.3kΩ, C = 0.47μF unless noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT					
Input Voltage		5	15	16	VDC
Input Current	Σ I_{OUT} = 24mA		50		mA
	Σ I_{OUT} = 128mA, 25°C		110	125	mA
	Σ I_{OUT} = 128mA, 85°C		120		mA
Input Ripple[1][5]	Σ I_{OUT} = 24mA, C = 0.47μF		10		mA, pk
	Σ I_{OUT} = 128mA, C = 0.47μF			25	mA, pk
ISOLATION					
Test Voltage[2]	Input-to-output, 5sec min			3000	VDC
	Channel-to-channel, 5sec min			3000	VDC
Rated Voltage[2]	Input-to-output, continuous			1000	VDC
	Channel-to-channel, continuous			1000	VDC
Isolation Impedance	Input-to-output		10 ‖ 6		GΩ ‖ pF
Leakage Current	Input-to-output, 240V/60Hz			1.0	μA
OUTPUT					
Voltage[3]	At 15V input I_L = 3mA	8.0	8.5	9.0	V
	I_L = 16mA	7.5	7.9	8.3	V
Current for Rated Voltage	Total of all outputs			128	mA
	Any one output[4]	3			mA
Total Safe Nondestructive Current	Total of all outputs			500	mA
	Any one output			200	mA
Load Regulation[3]			Note 4		
Ripple Voltage[5]	I_L = 3mA		35		mV, pk
	I_L = 16mA			200	mV, pk
Difference of $+V_O$ and $-V_O$	$+I_L = -I_L$		±30		mV
Sensitivity to Input Voltage Change			0.63		V/V
Output Voltage Change Over Temperature	-25°C to +85°C		2		%
TEMPERATURE RANGE					
Operating		-25		+85	°C
Storage		-55		+125	°C

NOTES:
1. 0.47μF external capacitor across "P+" to "V-" pins and 12" of # 24 wire to V_{IN}.
2. See "Isolation Voltage Ratings" on preceding page. The input to output and channel to channel continuous AC rating is 700V, rms.
3. See "Typical Performance Curves."
4. A minimum output current of 3mA at each output is recommended to maintain output voltage accuracy.
5. Test bandwidth 10MHz, max.

MECHANICAL



Pin numbers shown for reference only
Numbers may not be marked on package

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.080	1.120	27.43	28.45
B	1.080	1.120	27.43	28.45
C	.235	.285	5.97	7.24
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.350	3.81	8.89
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.100 BASIC		2.54 BASIC	

NOTE
Leads in true position within .010" (.25mm) R at MMC at seating plane

PIN POSITION	PIN DESIGNATION
1	$+V_{O4}$
2	C_4
3	$-V_{O4}$
4	No pin present
5	$+V_{O3}$
6	C_3
7	$-V_{O3}$
8	No pin present
9	$+V_{O2}$
10	C_2
11	$-V_{O2}$
12	No pin present
13	$+V_{O1}$
14	C_1
15	$-V_{O1}$
16	No pin present
17	P+
18	V-
19	V+
20	E

DISCUSSION

OUTPUT CURRENT RATINGS

At rated output voltage accuracy, the 724 is capable of providing 128mA divided among its eight outputs[1]. A minimum average output current of 3mA is recommended at each output to maintain voltage accuracy.

Output channels[2] may be connected in series or parallel for higher output voltage or current.

ISOLATION CONFIGURATIONS

The fact that the four outputs of the 724 are isolated from the input and from each other allows both two-port and three-port isolation connections.

Figure 1 shows two of Burr-Brown's 3650 Optically Coupled Isolation Amplifiers connected in three-port configuration. Two of the 724 channels provide power to the 3650's inputs. The other channels supply power to both 3650's outputs. Each amplifier's input and output are isolated from each other and the system's power supply common. Isolation specification applies to the amplifier input-to-output voltage isolation specification.

Figure 2 illustrates how the 724 may provide isolated input power to the input stage of four 3650's connected in the two-port configuration. Power for the four output stages is provided by the system +15VDC and -15VDC supplies. Input stages are isolated from each other and from the system supply. In this situation the 724's isolation specification applies to the amplifier's input-to-output voltage and to the voltage existing between any two I/P COM terminals.

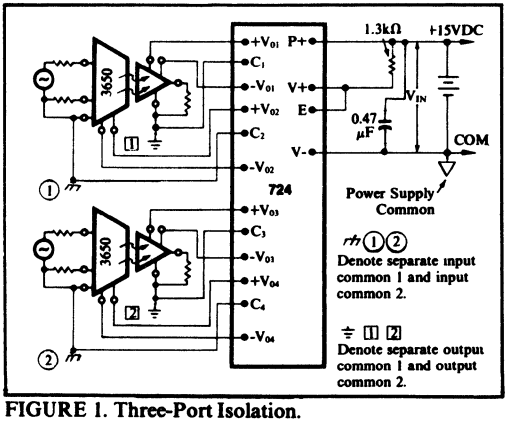


FIGURE 1. Three-Port Isolation.

ISOLATION VOLTAGE RATINGS

Since a "continuous" test is impractical in a product manufacturing situation (implies infinite test duration) it is generally accepted practice to perform a production test at a higher voltage (i.e., higher than the continuous rating) for some shorter length of time.

The important consideration is then "what is the relationship between actual test conditions and the continuous derated maximum specification?" There are several rules of thumb used throughout the industry to establish this relationship. Burr-Brown has chosen a very conservative one: $V_{test} = (2 \times V_{continuous\ rating}) + 1000V$. This relationship is appropriate for conditions where the system transient voltages are not well defined.[3] Where the real voltages are well defined or where the isolation voltage is not continuous the user may choose to use a less conservative derating to establish a specification from the test voltage.

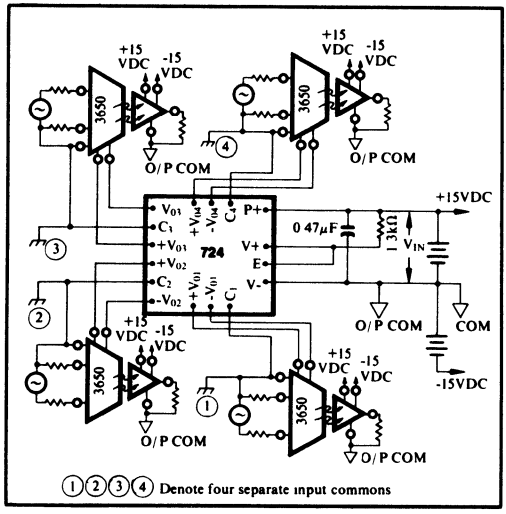


FIGURE 2. Two-Port Isolation with Four 3650's.

SHORT CIRCUIT PROTECTION

The circuit in Figure 3 may be added to the input of the 724 to protect it from damage in situations where too much current is demanded from the outputs - such as a short circuit from an output to its common. The circuit limits input current to approximately 150mA for an input voltage of 15VDC (for β of 2N2219 of 50).

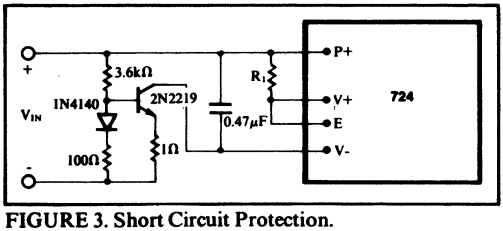


FIGURE 3. Short Circuit Protection.

(1) "output" denotes a single output terminal (+V or -V) and its associated common
(2) "channel" denotes a pair of outputs (+V and -V) and their associated common
(3) Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS 1-109 and ICS 1-111

INSTALLATION AND OPERATING INSTRUCTIONS

Typical application connections for the 724 are shown in Figures 1 and 2. Primary power (V_{IN}) is applied at the "P+" and "V-" terminals. The common or ground for V_{IN} may be connected to either "P+" or "V-"; the only requirement is that "P+" and "V+" must be positive with respect to "V-."

Power for the internal oscillator and switch drivers is derived from the primary power by a voltage dropping resistor R_1. The value of R_1 as a function of V_{IN} is shown in the "Typical Performance Curves" section. Alternately, voltage for the "V+" terminal may be obtained from a separate source. "V+" should be +5VDC to +7.5VDC positive with respect to "V-." If a separate source is used, the V+ input must be applied before the "P+" input to avoid possible damage to the unit. P+ and V+ must remain positive with respect to V- at all times (including transients). If necessary, diode clamps should be put across these inputs.

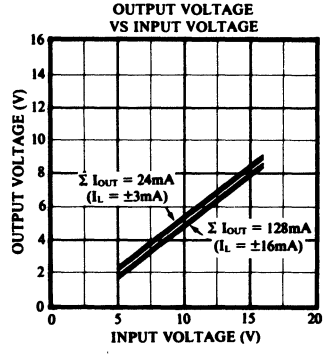
The "E" pin enables the converter when connected to "V+" and disables it when connected to "V-."

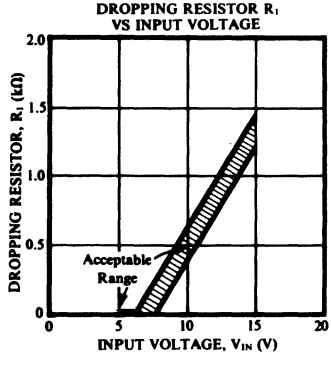
An external capacitor, "C", (0.47μF ceramic) is used to reduce input ripple. It should be connected as close to the "P+" and "V-" pins as practical. Input leads to these terminals should also be kept as short as possible. Since the 724 is not internally shielded, external shielding may be appropriate in applications where RFI at the 800kHz nominal oscillator frequency is a problem.

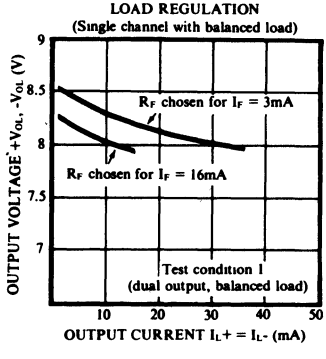
Each output is filtered with an internal 0.047μF capacitor. Output ripple voltage can be reduced below the specified value by adding external capacitors up to 10μF between each output and its common.

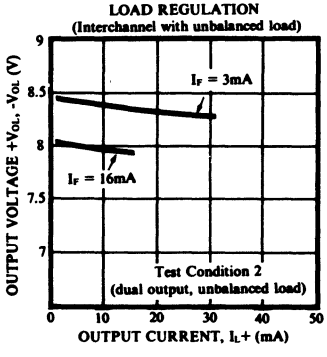
TYPICAL PERFORMANCE CURVES

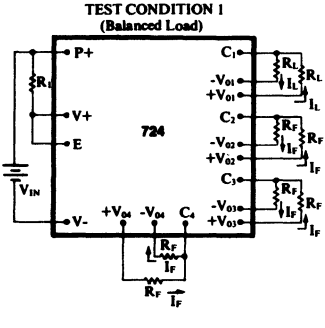
All specifications typical at 25°C unless otherwise noted

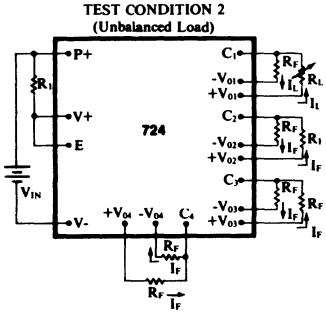












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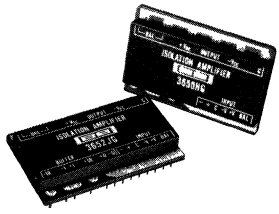


3650
3652

Optically-Coupled Linear ISOLATION AMPLIFIERS

FEATURES

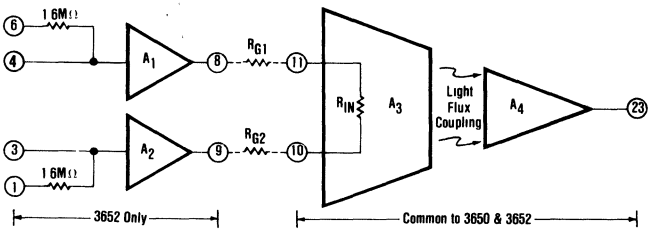
- BALANCED INPUT
- LARGE COMMON-MODE VOLTAGES
  ±2000V Continuous
  140dB Rejection
- ULTRA LOW LEAKAGE
  0.35μA max at 240V/60Hz
  1.8pF Leakage Capacitance
- EXCELLENT GAIN ACCURACY
  0.05% Linearity
  0.05%/1000Hours Stability
- WIDE BANDWIDTH
  15kHz ±3dB
  1.2V/μsec Slew Rate

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- DATA ACQUISITION
- INTERFACE ELEMENT
- BIOMEDICAL MEASUREMENTS
- PATIENT MONITORING
- TEST EQUIPMENT
- CURRENT SHUNT MEASUREMENT
- GROUND-LOOP ELIMINATION
- SCR CONTROLS

DESCRIPTION

The 3650 and 3652 are optically coupled integrated circuit isolation amplifiers. Prior to their introduction commercially available isolation amplifiers had been modular or rack mounted devices using transformer coupled modulation demodulation techniques. Compared to these earlier isolation amplifiers the 3650 and 3652 have the advantage of smaller size, lower cost, wider bandwidth and integrated circuit reliability. Also, because they use a DC analog modulation technique as opposed to a carrier type technique, they avoid the problems of electromagnetic interference (both transmitted and received) that most of the modular isolation amplifiers exhibit.



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PDS-3241

SPECIFICATIONS

ELECTRICAL

Typical at 25°C and ±15VDC supply voltages unless otherwise noted

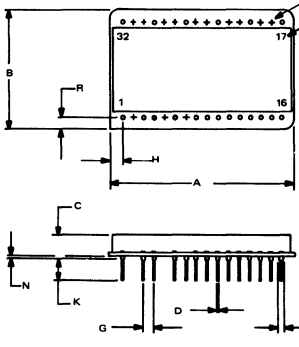
MODEL	3650MG/HG[1]	3650JG	3650KG	3652MG/HG[1]	3652JG
ISOLATION					
Isolation Voltage Rated Continuous, (min) Test Voltage, (min) 10sec duration	2000Vp or VDC 5000Vp				
Isolation-Mode Rejection, G = 10 DC 60Hz, 5000Ω source unbalance Leakage Current, 240V/60Hz Isolation Impedance Capacitance Resistance	140dB 120dB 0.35μA, max 1 8pF $10^{12}\Omega$				
GAIN					
Gain Equation for current sources for voltage sources	$G_1 = 10^6$Volt/Amp $G_V = \frac{10^6}{R_{G1} + R_{G2} + R_{IN}}$ V/V			$G_1 = 1\ 0057 \times 10^6$ Volt/Amp[2] $\frac{10^6}{R_{G1} + R_{G2} + R_{IN} + R_O}$ V/V	
Input Resistance, R_{IN}, max Buffer Output Impedance, R_O Gain Equation Error, max[3] Gain Nonlinearity Gain vs Temperature Gain vs Time	25Ω Not applicable 1 5% ±0.05% typ ±0.2% max 300ppm/°C ±0 05%/1000hrs	0 5% ±0 03% typ ±0.1% max 100ppm/°C	0 5% ±0 02% typ ±0 05% max 50ppm/°C	25Ω 90Ω ±30Ω 1.5%[4] ±0 05% typ ±0 2% max 300ppm/°C[4] ±0 05%/1000hrs	0 5%[4] ±0 05% typ ±0 1% max 200ppm/°C[4]
Frequency Response Slew Rate ±3dB Frequency Settling Time to ±0 01% to ±0 1%	0 7V/μsec min, 1 2V/μsec typ 15kHz 400μsec 200μsec				
INPUT STAGE[5]					
Input Offset Voltage at 25°C, max[3] vs Temperature, max vs Supply vs Time	±5mV ±25μV/°C 100μV/V 50μV/1000 hrs	±1mV ±10μV/°C	±0 5mV ±5μV/°C	±5mV ±50μV/°C 100μV/V 100μV/1000 hrs	±2mV ±25μV/°C
Input Bias Current at 25°C vs Temperature vs Supply	10nA typ, 40nA max 0 3nA/°C 0 2nA/V			10pA typ, 50pA max doubles every +10°C 1pA/V	
Input Offset Current vs Temperature vs Supply	effects included in output offset			10pA doubles every 10°C 1pA/V	
Input Impedance Differential Common-mode	"R_{IN}" = 25Ω max $10^9\Omega$			$10^{11}\Omega$ $10^{11}\Omega$	
Input Noise Voltage, 0 05Hz to 100Hz 10Hz to 10kHz	4μV, p-p 4μV, rms			8μV, p-p 5μV, rms	
Input Voltage Range Common-mode, linear operation, w/o damage, at +,- at +I, -I at +IR, -IR	±(| V| -5)V ±V Not applicable[6] Not applicable[6]			±(| V| -5) ±V ±300V for 10msec[7] ±3000V for 10msec[7]	
Differential, w/o damage, at +, - Differential, w/o damage, at +I, -I Differential, w/o damage, at +IR, -IR	±V Not applicable Not applicable			±V ±600V for 10msec[7] ±6000V for 10msec[7]	
Common-mode Rejection, 60Hz	90dB at 60Hz, 5kΩ imbalance			80dB at 60Hz, 5kΩ imbalance	
Power Supply (Input Stage Only) Voltage (at "+V" and "-V" Current Quiescent with ±10V output[7]	±8V to±18V ±1 2mA[8] +6 5mA or -6 5mA, typ +12mA or -12mA, max			±8V to ±18V ±3mA[8] +8.5mA or -8 5mA, typ +16mA or -16mA, max	

ELECTRICAL (cont)

MODEL	3650MG/HG[1]	3650JG	3650KG	3652MG/HG[1]	3652JG
OUTPUT STAGE					
Output Voltage, min	±10V			±10V	
Output Current, min	±5mA			±5mA	
Output Offset Voltage					
at 25°C max[3]	±25mV	±10mV	±10mV	±25mV	±10mV
vs Temperature, max	±900µV/°C	±450µV/°C	±300µV/°C	±900µV/°C	±450µV/°C
vs Supply		±500µV/V		±500µV/V	
vs Time		±1mV/1000hrs		±1mV/1000hrs	
Output Noise Voltage					
0 05Hz to 100Hz		50µV, p-p		50µV, p-p	
10Hz to 1kHz		65µV, rms		65µV, rms	
Power Supply (Output Stage Only)					
Voltage ("+V_{CC}" and "-V_{CC}")		±8V to ±18V			
Current					
Quiescent		±2 3mA typ, ±6mA max			
with ±5mA output, max		±11mA			
TEMPERATURE[9]					
Specification		0°C to 85°C			
Operating		-40°C to +100°C			
Storage		-55°C to +125°C			

NOTES. (1) All electrical and mechanical specifications of the 3650MG and 3652MG are identical to the 3650HG and 3652HG, respectively, except that the following specifications apply to the 3650MG and 3652MG: (a) isolation test voltage duration increased from 10sec minimum to 60sec minimum, (b) Input offset voltage at 25°C max. ±10mV; vs temp max: ±100µV/°C, (c) Output offset voltage at 25°C max: ±50mV; vs temp max ±1.8mV/°C (2) If used as 3650, see Installation and Operating Instructions (3) Trimmable to zero. (4) Gain error terms specified for inputs applied through buffer amplifiers (i e., ±1 or ±IR pins) (5) Input stage specifications at +I and −I inputs for 3652 unless otherwise noted (6) Maximum safe input current at either input is 10mA (7) Continuous rating is 1/3 pulse rating (8) Load current is drawn from one supply lead at a time; other supply current at quiescent level. For 3652 add 0 2mA/V of positive CMV (9) d/T/dt>1°C/minute below 0°C, and long-term storage above 100°C is not recommended. Also limit the repeated thermal cycles to be within the 0°C to +85°C temperature range

MECHANICAL



"+" denotes missing pins

Pin numbers shown for reference only Numbers may not be marked on package

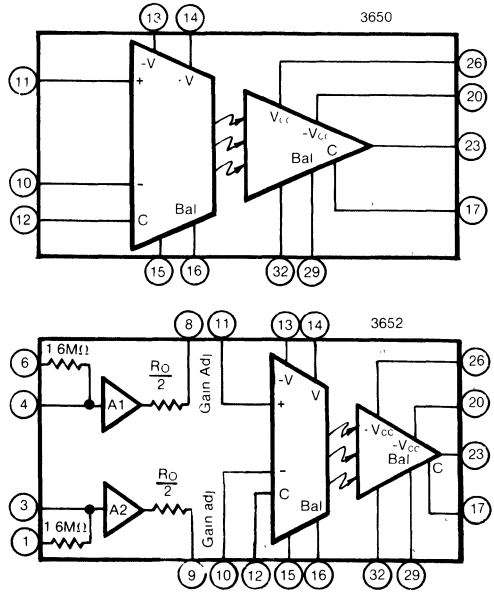
NOTE
Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.700	1 760	43.18	44.70
B	1 120	1 160	28.45	29 46
C	.170	230	4 32	5 84
D	018	021	0 46	0.53
F	035	050	0.89	1 27
G	.100 BASIC		2.54 BASIC	
H	110	130	2.79	3 30
K	150	250	3 81	6.35
L	900 BASIC		22 86 BASIC	
N	002	.010	0.05	0 25
R	.110	130	2 79	3 30

ORDER NUMBER.
3650MG 3652MG
3650HG 3652HG
3650JG 3652JG
3650KG

MATERIAL Alumina (ceramic)
WEIGHT 14 grams (0 5 oz)
MATING CONNECTOR: 2302MC (set of two, 16-pin strips)

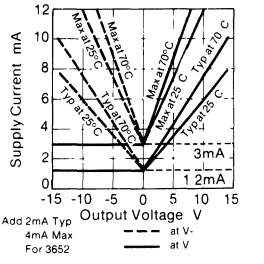
PIN CONNECTIONS



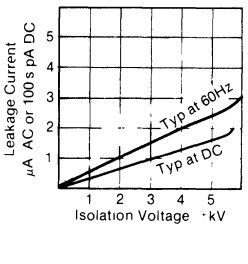
TYPICAL PERFORMANCE CURVES

Typical at 25°C and ±15VDC power supplies unless otherwise noted

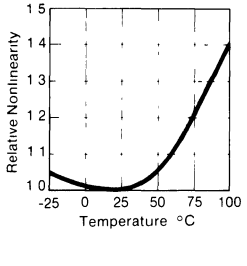
INPUT STAGE SUPPLY CURRENT VS OUTPUT VOLTAGE



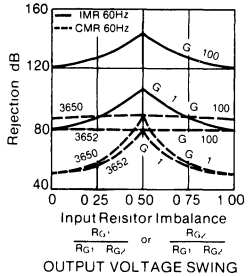
ISOLATION LEAKAGE CURRENT VS ISOLATION VOLTAGE



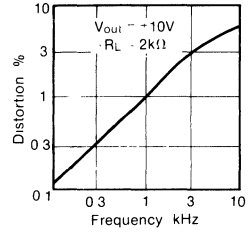
NORMALIZED LINEARITY VS TEMPERATURE



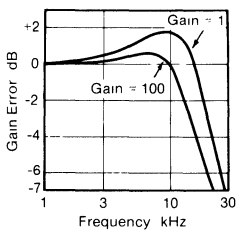
REJECTION VS RESISTOR IMBALANCE



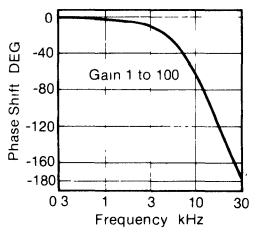
DISTORTION VS FREQUENCY



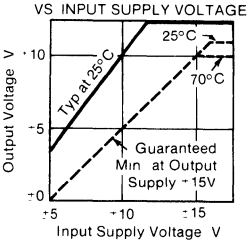
GAIN ERROR VS FREQUENCY



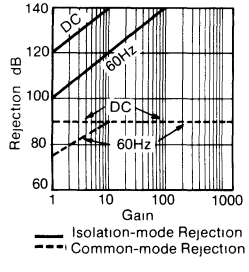
PHASE SHIFT VS FREQUENCY



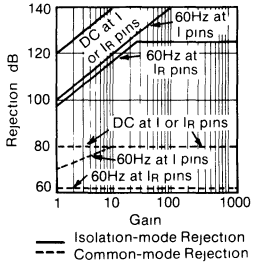
OUTPUT VOLTAGE SWING VS INPUT SUPPLY VOLTAGE



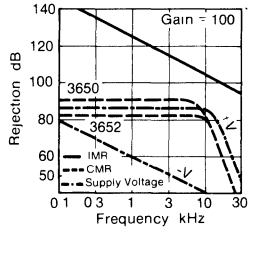
3650 COMMON-MODE AND ISOLATION-MODE REJECTION VS GAIN



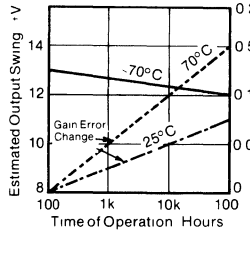
3652COMMON-MODE AND ISOLATION-MODE REJECTION VS GAIN



REJECTION VS FREQUENCY



OUTPUT VOLTAGE AND GAIN ERROR VS TIME



DEFINITIONS

ISOLATION-MODE VOLTAGE, V_{ISO}

The isolation-mode voltage is the voltage which appears across the isolation barrier, i.e., between the input common and the output common. (See Figure 1.)

Two isolation voltages are given in the electrical specifications; "rated continuous" and "test voltage". Since it is impractical on a production basis to test a "continuous" voltage (infinite test time is implied), it is generally accepted practice to test at a significantly higher voltage for some reasonable length of time. For the 3650 and the 3652 the "test voltage" is equal to 1000V plus two times the "rated continuous" voltage. Thus, for a continuous rating of 2000V each unit is tested at 5000V.

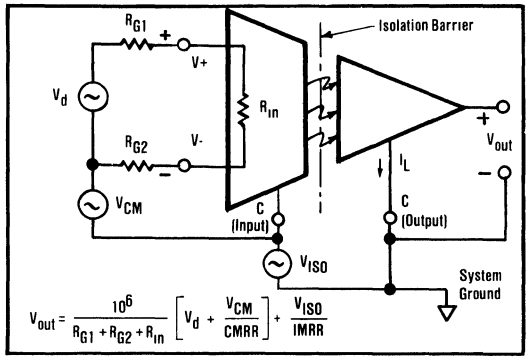


FIGURE 1. Illustration of Isolation-mode and Common-mode Specifications.

COMMON-MODE VOLTAGE, V_{CM}

The common-mode voltage is the voltage midway between the two inputs of the amplifier measured with respect to input common. It is the algebraic average of the voltage applied at the amplifiers' input terminals. In the circuit in Figure 5, $(V_+ + V_-)\ 2 = V_{CM}$. (Note: Many applications involve a large system "common-mode voltage." Usually in such cases the term defined here as "V_{CM}" is negligible and the system "common-mode voltage" is applied to the amplifier as "V_{ISO}" in Figure 1.)

ISOLATION-MODE REJECTION

The isolation-mode rejection is defined by the equation in Figure 1. The isolation-mode rejection is not infinite because there is some leakage across the isolation barrier due to the isolation resistance and capacitance.

NONLINEARITY

Nonlinearity is specified to be the peak deviation from a best straightline, expressed as a percent of peak-to-peak full scale output (i.e., ±10mV at 20V p-p ≈ 0.05%).

THEORY OF OPERATION

Prior to the introduction of the 3650 family optical isolation had not been practical in linear circuits. A single LED and photodiode combination, while useful in a wide range of digital isolation applications, has fundamental limitations - primarily nonlinearity and instability as a function of time and temperature.

The 3650 and 3652 use a unique technique to overcome the limitations of the single LED and photodiode isolator. Figure 2 is an elementary equivalent circuit for the 3650 which can be used to understand the basic operation without consideration the cluttering details of offset adjustment and biasing for bipolar operation.

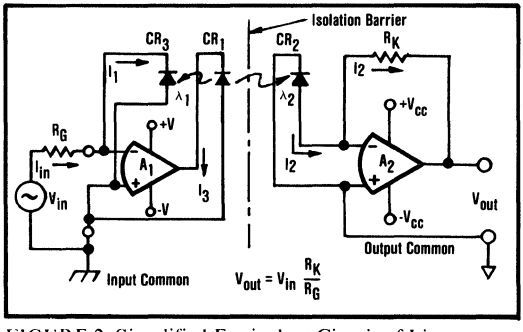


FIGURE 2. Simplified Equivalent Circuit of Linear Isolator.

Two matched photodiodes are used--one in the input (CR_3) and one in the output stage (CR_2) - - to greatly reduce nonlinearities and time - temperature instabilities. Amplifier A_1, LED CR_1, and photodiode CR_3 are used in a negative feedback configuration such that $I_1 = I_{in}\ R_G$ (where R_G is the user supplied gain setting resistor). Since CR_2 and CR_3 are closely matched and since they receive equal amounts of light from the LED CR_1 (i.e., $\lambda_1 = \lambda_2$), $I_2 = I_1 = I_{in}$. Amplifier A_2 is connected as a current-to-voltage converter with $V_{out} = I_2\ R_K$ where R_K is an internal 1MΩ scaling resistor. Thus the overall transfer function is:

$$V_{out} = V_{in}\ \frac{10^6}{R_G},\ (R_G \text{ in ohms})$$

This improved isolator circuit overcomes the primary limitations of the single LED and photodiode combination. The transfer function is now virtually independent of any degradation in the LED output as long as the two photodiodes and optics are closely matched*. Linearity is now a function of the accuracy of the matching and is further enhanced by the use of negative feedback in the input stage. Advanced laser trimming techniques are used to further compensate for residual matching errors.

* The only effect of decreased LED output is a slight decrease in full scale swing capability. See Typical Performance Curves.

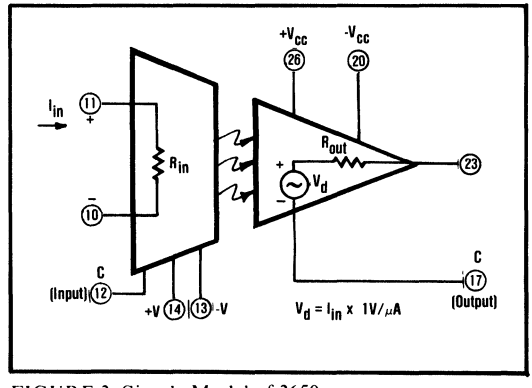


FIGURE 3. Simple Model of 3650.

A model of the 3650 suitable for simple circuit analysis is shown in Figure 3. The output is a current dependent voltage source, V_d, whose value depends on the input current. Thus, the 3650 is a transconductance amplifier with a gain of one volt per microamp. When voltage sources are used the input current is derived by using gain setting resistors in series with the voltage source (see Installation and Operating Instructions for details). R_{in} is the differential input impedance. The common-mode and isolation impedances are very high and are assumed to be infinite for this model.

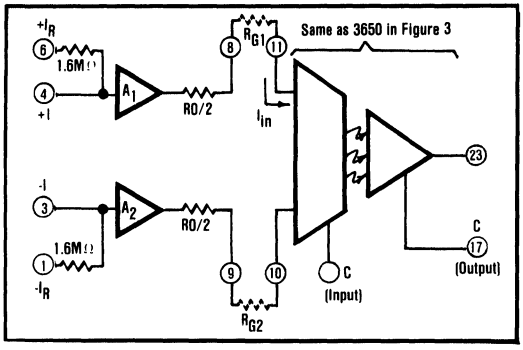


FIGURE 4. Simple Model of 3652.

A simplified model of the 3652 is shown in Figure 4. The isolation and output stages are identical to the 3650. Additional input circuitry consisting of FET buffer amplifiers and input protection resistors have been added to give higher differential and common-mode input impedance ($10^{11}\Omega$), lower bias currents (50pA) and overvoltage protection. The +IR and -IR inputs have a 10msec pulse rating of 6000V differential and 3000V common-mode (see Definitions for a discussion of common-mode and isolation-mode voltages.) The addition of the buffer amplifiers also creates a voltage-in voltage-out transfer function with the gain set by R_{G1} and R_{G2}.

INSTALLATION & OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

The power supply connections for the 3650 and 3652 are shown in Figure 5. When a DC DC converter is used for isolated power it is placed in a parallel with the isolation barrier of the amplifier. This can lower the isolation impedance and degrade the isolation-mode rejection of the overall circuit. Therefore, a high quality, low leakage DC DC converter such as the Burr-Brown Model 722 should be used.

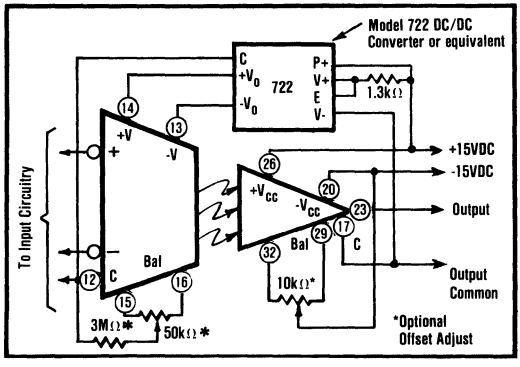


FIGURE 5. Power and Offset Adjust Connections.

OFFSET VOLTAGE ADJUSTMENTS

The offset nulling circuits are identical for the 3650 and 3652 and are shown in Figure 5. The offset adjust circuitry is optional and the units will meet the stated specifications with the BAL terminals unconnected. Provisions are available to null both the input and output stage offsets. If the amplifier is operated at a fixed gain, normally only one adjustment will be used; the output stage (10kΩ adjustment) for low gains and the input stage (50kΩ adjustment) for high gains.(>10).

Use the following procedure if it is desired to null both input and output components (for example, if the gain of the amplifier is to be switched). The input stage offset is first nulled (50kΩ adjustment) with the appropriate input signal pins connected to input common and the amplifier set at its maximum gain. The gain is then set to its minimum value and the output offset is nulled (10kΩ adjustment).

INPUT CONFIGURATIONS

Some possible input configurations for the 3650 and 3652 are shown in Figures 6a, 6b, 6c. Differential input sources are used in these examples. For situations with non-differential inputs the appropriate source term should be set to zero in the gain equations and replaced with a short in the diagrams.

Figure 6a shows the 3650 connected as a transconductance amplifier with input current sources. Voltage sources are shown in Figure 6b. In this case the voltages are converted to currents by R_{G1} and R_{G2}. As shown by the equations, they perform as gain setting resistors in the voltage transfer function. When a single voltage source is used it is recommended (but not essential) that the gain setting resistor remain split into two equal halves in order to minimize errors due to bias currents and common-mode rejection (see Typical Performance Curves).

Figure 6c illustrates the connections for the 3652 when the FET buffer amplifiers A_1 and A_2 are used. This configuration provides an isolation amplifier with high input impedance (both common-mode and differential) and good common-mode and isolation-mode rejection. It is a true isolated instrumentation amplifier which has many benefits for noise rejection when source impedance imbalances are present.

In the 3652 the voltage gain of the buffer amplifiers is slightly less than unity, but the gain of the output stage has been raised to compensate for this so that the overall transfer function from the ±I or ±IR inputs to the output is correct. It should be noted that A_1 and A_2 are buffer amplifiers. No summing can be done at the ±I or ±IR inputs. Figure 6c shows the +I and -I inputs used. If more input voltage protection is desired, then the +IR and -IR inputs should be used. This will increase the input noise due to the contribution from the 1.6MΩ resistors, but will provide additional differential and common-mode protection (10msec rating of 3kV).

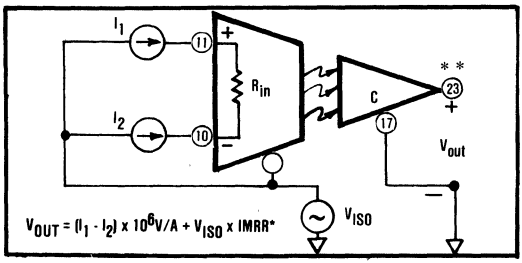


FIGURE 6a. 3650 With Differential Current Sources

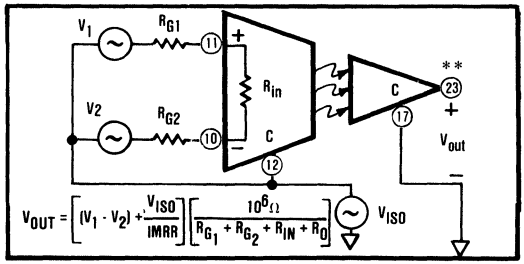


FIGURE 6b. 3650 With Differential Voltage Source.

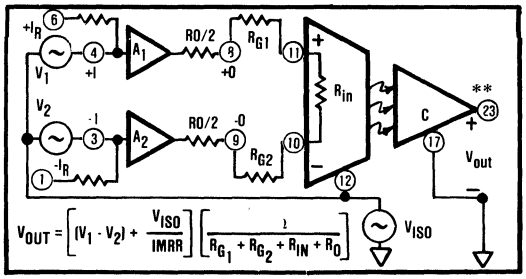


FIGURE 6c. 3652 with Differential Voltage Source.

*IMRR here is in pA/V, typically 5pA/V at 60Hz and 1pA/V at DC.
**The offset adjustment circuitry and power supply connections have been omitted for simplicity Refer to Figure 5 for details.

ERROR ANALYSIS

A model of the 3650 suitable for DC error analysis of offset voltage, voltage drift versus temperature, bias current, etc., is shown in Figure 7.

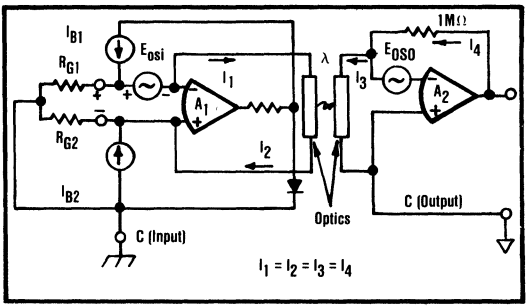


FIGURE 7. DC Error Analysis Model for 3650.

A_1 and A_2, the input and output stage amplifiers, are considered to be ideal. Separate external generators are used to model the offset voltages and bias currents. R_{in} is assumed to be small relative to R_{G1} and R_{G2} and is therefore omitted from the gain equation. The feedback configuration, optics and component matching are such that $I_1 = I_2 = I_3 = I_4$. A simple circuit analysis gives the following expression for the total output error voltage due to offset voltages and bias currents.

$$V_{out-total} = \frac{10^6}{R_{G1} + R_{G2}} \left[E_{osi} + (I_{B1} R_{G1} - I_{B2} R_{G2})\right] + E_{oso} \quad (1)$$

Offset current is defined as the difference between the two bias currents I_{B1} and I_{B2}. If $I_{B1} = I_B$ and $I_{B2} = I_B + I_{os}$, then, for $R_{G1} = R_{G2}$, $V_{out} - I_B = \frac{10^6 I_{os}}{2}$.

This component of error is not a function of gain and is therefore included as a part of E_{oso} specifications. The output errors due to the output stage bias current are also included in E_{oso}. This results in a very simple equation for the total error:

$$V_{out-total} = \frac{10^6 E_{osi}}{2R_{G1}} + E_{oso} \text{ (for } R_{G1} = R_{G2}). \quad (2)$$

In summary it should be noted that equation (2) should be used only when $R_{G1} = R_{G2}$. When $R_{G1} \neq R_{G2}$, equation (1) applies.

The effects of temperature may be analyzed by replacing the offset terms with their corresponding temperature gradient terms:

$V_{out} \rightarrow \Delta V_{out}/\Delta T$, $E_{osi} \rightarrow \Delta E_{osi}/\Delta T$, etc.

For a complete analysis of the effects of temperature, gain variations must also be considered.

OUTPUT NOISE

The total output noise is given by

$$E_n (RMS) = \sqrt{(E_{ni} G)^2 + (E_{no})^2}$$

where E_n (RMS) = total output noise
E_{ni} = RMS noise of the input stage
E_{no} = RMS noise of the output stage
$G = 10^6/(R_{G1} + R_{G2})$

E_{no} includes the noise contribution due to the optics and the noise currents of the output stage. Errors created by the noise current of the input stage are insignificant compared to other noise sources and are therefore omitted.

COMMON-MODE and ISOLATION-MODE REJECTION

The expression for the output error due to common-mode and isolation mode voltage is:

$$V_{out} = G\left[\frac{V_{cm}}{CMRR} + \frac{V_{iso}}{IMRR}\right]$$

GUARDING & PROTECTION

To preserve the excellent inherent isolation characteristics of these amplifiers, the following recommended practice should be noted:

1. Use shielded, twisted pair of cable at the input as with any instrumentation amplifier;
2. Care sould be taken to minimize external capacitance. A symmetrical layout of external components to achieve balanced capacitance from the input terminals to output common will preserve high IMR;
3. External components and conductor patterns should be at a distance equal to or greater than the distance between the input and output terminals, to prevent HV breakdown.
4. Though not an absolute requirement, the use of laminated or conformally coated printed circuit boards is recommended.

APPLICATIONS

Figure 8 shows a system where isolation amplifiers (3650) are used to measure the armature current and the armature voltage of a motor.

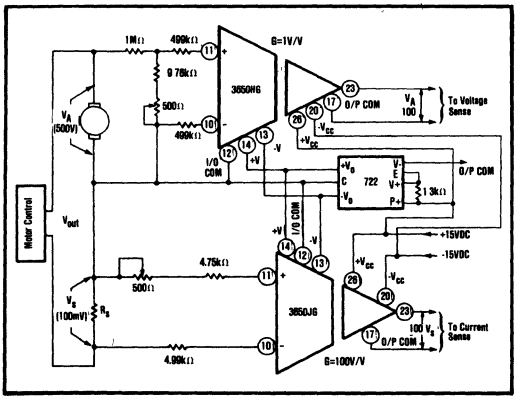


FIGURE 8. Isolated Armature Current and Voltage Sensor.

The armature current of the motor is converted to a voltage by the calibrated shunt R, and then amplifier (adjustable gain) and isolated by the 3650.

The armature voltage is sensed by the voltage divider (adjustable) shown and then amplified and isolated by the 3650.

The 3650 provides the advantage of accurate current measurement in the presence of high common-mode voltage. Both 3650's provide the advantage of isolating the motor ground from the control system ground. Isolated power is provided by an isolated DC/DC converter (BB Model 722 or equivalent).

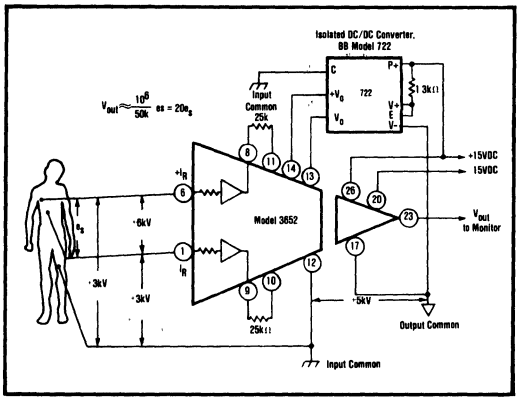


FIGURE 9. 3652 Used in Patient Monitoring Application (ECG, VCG, EMG Amplifier).

balanced input instrumentation amplifier with very high differential and common-mode impedance means that it can greatly reduce the common-mode noise pick up due to imbalance in lead impedances that often appear in patient monitoring situations. The 3kV and 6kV shown in Figure 9 are the 10msec pulse ratings of the +IR and -IR inputs for the common-mode and differential input voltages with respect to input common. The rating of the isolation barrier is 2000V, pk continuous. The non-recurrent pulse rating of the isolation barrier is 5000V, pk since each unit is factory tested at 5000V, pk. If the isolation barrier is to be subjected to higher voltages a gas filled surge voltage protection device can be used. For multichannel operation, two 3562's can be powered by one Model 722 isolated DC/DC converter. The total leakage current for both channels at 240V/60Hz would still be less than 2μA.

The block diagram in Figure 10 shows the use of isolation amplifiers in SCR control application.

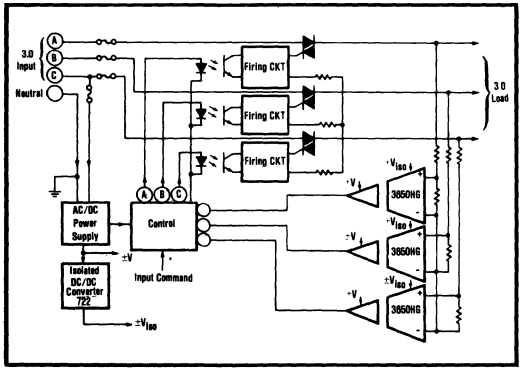
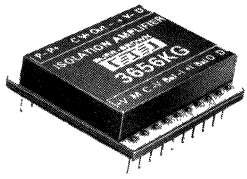


FIGURE 10. 3-Phase Bidirectional SCR Control with Voltage Feedback.

BURR-BROWN®

3656



Integrated Circuit - Transformer Coupled ISOLATION AMPLIFIER

FEATURES

- INTERNAL ISOLATED POWER
- 8000V ISOLATION TEST VOLTAGE
- 0.5μA MAX LEAKAGE AT 120V, 60Hz
- 3-PORT ISOLATION
- 125dB REJECTION AT 60Hz
- 1" x 1" x 0.25" CERAMIC PACKAGE

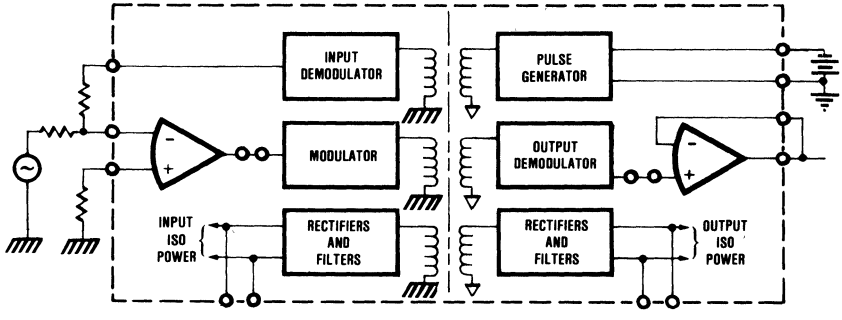
APPLICATIONS

- MEDICAL
  Patient monitoring and diagnostic instrumentation
- INDUSTRIAL
  Ground loop elimination and off-ground signal measurement
- NUCLEAR
  Input/output/power isolation

DESCRIPTION

The 3656 is the first amplifier to provide a total isolation function ... both signal and power isolation ... in integrated circuit form. This remarkable advancement in analog signal processing capability is accomplished by use of a patented modulation technique and minature hybrid transformer.

Versatility and performance are outstanding features of the 3656. It is capable of operating with three completely independent grounds (three-port isolation). In addition, the isolated power generated is available to power external circuitry at either the input or output. The uncommitted op amps at the input and the output allow a wide variety of closed-loop configurations to match the requirements of many different types of isolation applications.



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PDS-403D

THEORY OF OPERATION

Details of the 3656 are shown in Figure 1. The external connections shown, place it in its simplest gain configuration - unity gain, noninverting. Several other amplifier gain configurations and power isolation configurations are possible. See Installation and Operating Instructions and Applications sections for details.

Isolation of both signal and power is accomplished with a single miniature toroid transformer with multiple windings. A pulse generator operating at approximately 750kHz provides a two-part voltage waveform to transformer T_1. One part of the waveform is rectified by diodes D_1 through D_4 to provide the isolated power to the input and output stages (+V, -V and V+, V-). The other part of the waveform is modulated with input signal information by the modulator operating into the V_2 winding of the transformer.

The modulated signal is coupled by windings W_6 and W_7 to two matched demodulators - one in the input stage and one in the output stage - which generate identical voltages at their outputs, pins 10 and 11 (voltages identical with respect to their respective commons, pins 3 and 17). In the input stage the input amplifier A_1, the modulator and the input demodulator are connected in a negative feedback loop. This forces the voltage at pin 6 (connect as shown in Figure 1) to equal the input signal voltage applied at pin 7. Since the input and the output demodulators are matched and produce identical output voltages, the voltage at pin 11 (referenced to pin 17, the output common) is equal to the voltage at pin 10 (referenced to pin 3, the input common). In the output stage, output amplifier A_2 is connected as a unity gain buffer, thus the output voltage at pin 15 equals the output demodulator voltage at pin 11. The end result is an isolated output voltage at pin 15 equal to the input voltage at pin 7 with no galvanic connection between them.

Several amplifier and power connection variations are possible:

1. The input stage may be connected in various operational amplifier gain configurations.
2. The output stage may be operated at gains above unity.
3. The internally generated isolated voltages which provide power to A_1 and A_2 may be overridden and external supply voltages used instead.

Versatility and its three independent isolated grounds allow simple solutions to demanding analog signal conditioning problems. See the Installation and Operating Instructions and Applications sections for details.

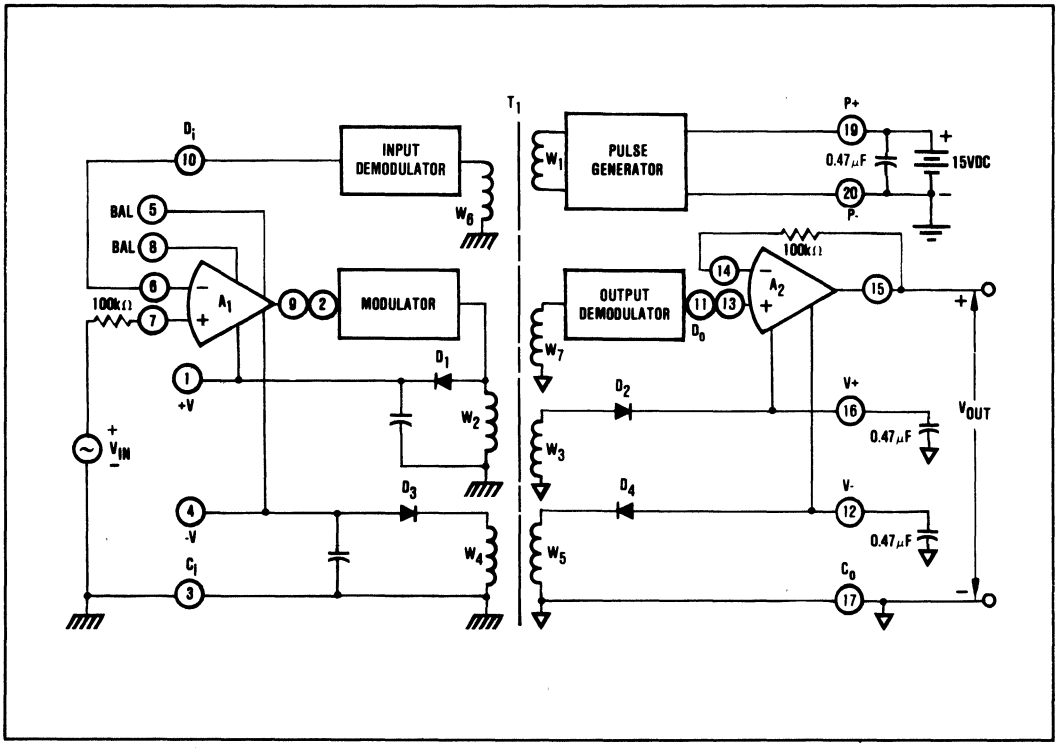


FIGURE 1. Block Diagram.

SPECIFICATIONS

ELECTRICAL

At +25°C, V± = 15VDC and 15VDC between P+ and P-, unless otherwise noted

PARAMETER	CONDITIONS	3656AG, BG, HG, JG, KG			UNITS
		MIN	TYP	MAX	
ISOLATION					
Voltage					
Rated Continuous(1), DC		3500 (1000)			VDC
Rate Continuous(2), AC		2000 (700)			V, rms
Test, 10sec(1)		8000 (3000)			VDC
Rejection	G_1 = 10V/V				
DC			160		dB
60Hz, < 100Ω in I/P Com(2)			125		dB
60Hz, 5kΩ in I/P Com(2)					
3656HG		108			dB
3656AG, BG, JG, KG		112			dB
Capacitance(1)			60 (63)		pF
Resistance(1)			10^{12} (10^{12})		Ω
Leakage Current	120V, 60Hz		0 28	0 5	μA
GAIN					
Equations	See Text				
Accuracy of Equations					
Initial(3) 3656HG	G < 100V/V			1 5	%
3656AG, JG, KG				1 0	%
3656BG				0 3	%
vs Temperature 3656HG				480	ppm/°C
3656AG, JG				120	ppm/°C
3656BG, KG				60	ppm/°C
vs Time			0 02 (1 + log khrs)		%
Nonlinearity	$R_A + R_F = R_B \geq 2M\Omega$				
External Supplies used at					
pins 12 and 16, 3656HG	Unipolar or Bipolar Output			±0 15	%
3656AG, JG, KG				±0 1	%
3656BG				±0 05	%
Internal Supplies used for	Bipolar Output Voltage				
Output Stage	Swing, Full Load(4)		±0 15		%
OFFSET VOLTAGE(5)	RTI				
Initial(3), 3656HG	15V_P between P+ and P-			±|4 + 40/G_1|	mV
3656AG, JG				±|2 + (20/G_1)|	mV
3656BG, KG				±|1 + (10/G_1)|	mV
vs Temperature, 3656HG				±|200 + (1000/G_1)|	μV/°C
3656JG				±|50 + (750/G_1)|	μV/°C
3656AG				±|25 + (500/G_1)|	μV/°C
3656KG				±|10 + (350/G_1)|	μV/°C
3656BG				±|5 + (350/G_1)|	μV/°C
vs Supply Voltage	Supply between P+ and P-				
3656HG				±|0 6 + (3 5/G_1)|	mV/V
3656AG, BG, JG, KG				±|0 3 + (2 1/G_1)|	mV/V
vs Current(6)			±|0 1 + (10/G_1)|	±|0 2 + (20/G_1)|	mV/mA
vs Time			±|10 + (100/G_1)| x (1 + log khrs)		μV
AMPLIFIER PARAMETERS	Apply to A1 and A2				
Bias Current(7)					
Initial				100	nA
vs Temperature			0 5		nA/°C
vs Supply			0 2		nA/V
Offset Current(7)			5	20	nA
Impedance	Common-mode		100 || 5		MΩ || pF
Input Noise Voltage	f_B = 0 05Hz to 100Hz		5		μV, p-p
	f_B = 10Hz to 10kHz		5		μV, rms
Input Voltage Range(8)					
Linear Operation	Internal Supply			±5	V
	External Supply			Supply -5V	V
Without Damage	Internal Supply			±8	V
	External Supply			Supply	V
Output Current	V_{OUT} = ±5V				
	±15V External Supply	±5			mA
	Internal Supply	±2 5			mA
	V_{OUT} = ±10V				
	±15V External Supply	±2 5			mA
	V_{OUT} = ±2V, $V_{P+, P-}$ = 8.5V				
	Internal Supply		±1		mA
Quiescent Current			150	450	μA

ELECTRICAL (CONT)

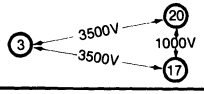
At +25°C, V± = 15VDC and 15VDC between P+ and P-, unless otherwise noted

PARAMETER	CONDITIONS	3656AG, BG, HG, JG, KG			UNITS
		MIN	TYP	MAX	
FREQUENCY RESPONSE					
±3dB Response	Small Signal		30		kHz
Full Power			1 3		kHz
Slew Rate	Direction measured at output	+0 1, -0 04			V/µsec
Settling Time	to 0 05%		500		µsec
OUTPUT					
Noise Voltage (RTI)	f_B = 0 05Hz to 100Hz		$\sqrt{(5.2 + (22/G_1)^2}$		µV, p-p
	f_B = 10Hz to 10kHz		$\sqrt{(5)^2 + (11/G_1)^2}$		µV, rms
Residual Ripple(9)			5		mV, p-p
POWER SUPPLY IN	at P+, P-				
Rated Performance			15		VDC
Voltage Range(10)	Derated Performance	8 5		16	VDC
Ripple Current(9)			10	25	mA, p-p
Quiescent Current(11)	Average		14	18	mA, DC
Current vs Load Current(12)	vs Currents from +V, -V, V+, V-		0 7		mA/mA
ISOLATED POWER OUT	at +V, -V, V+, V- pins(13)				
Voltage, no load	15V between P+ and P-	8 5	9 0	9 5	V
Voltage, full load	±5mA (10mA sum) load(12)	7 0	8 0	9 0	V
Voltage vs Power Supply	vs Supply between P+ and P-		0 66		V/V
Ripple Voltage(9)					
No load			40		mV, p-p
Full load	±5mA load		80	200	mV, p-p
TEMPERATURE RANGE					
Specification 3656AG, BG		-25		+85	°C
3656HG, JG, KG		0		+70	°C
Operation(10)		-55		+100	°C
Storage(14)		-65		+125	°C

NOTES:

1 Ratings in parenthesis and between P- (pin 20) and O/P Com (pin 17) Other isolation ratings are between I/P Com and O/P Com or I/P Com and P-
2 May be improved with proper shielding See Performance Curves
3 May be trimmed to zero
4 If output swing is unipolar, or if the output is not loaded, specification same as if external supply were used
5 Includes effects of A_1 and A_2 offset voltages and bias currents if recommended resistors used
6 Versus the sum of all external currents drawn from V+, V-, +V, -V (= ISO)
7 Effects of A_1 and A_2 bias currents and offset currents are included in Offset Voltage specifications
8 With respect to I/P Com (pin 3) for A_1 and with respect to O/P Com (pin 17) for A_2 CMR for A_1 and A_2 is 100dB, typical
9 In configuration of Figure 3 Ripple frequency approximately 750kHz Measurement bandwidth is 30kHz
10 Decreases linearly from 16VDC at 85°C to 12VDC at 100°C
11 Instantaneous peak current required from pins 19 and 20 at turn-on is 100mA for slow rising voltages (50msec) and 300mA for fast rises (50µsec)
12 Load current is sum drawn from +V, -V, V+, V- (= I_{ISO})
13 Maximum voltage rating at pins 1 and 4 is ±18VDC, maximum voltage rating at pins 12 and 16 is ±18VDC
14 Isolation ratings may degrade if exposed to 125°C for more than 1000 hours or 90°C for more than 50,000 hours

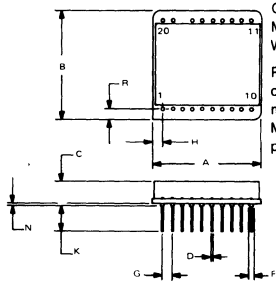
An example of the ratings for 3-port continuous isolation



PIN DESIGNATIONS

1	+V	11	OUTPUT DEMOD
2	MOD INPUT	12	V-
3	INPUT DEMOD COM	13	A_2 NONINVERTING INPUT
4	-V	14	A_2 INVERTING INPUT
5	BALANCE	15	A_2 OUTPUT
6	A_1 INVERTING INPUT	16	V+
7	A_1 NONINVERTING INPUT	17	OUTPUT DEMOD COM
8	BALANCE	18	NO PIN
9	A_1 OUTPUT	19.	P+
10	INPUT DEMOD	20	P-

MECHANICAL



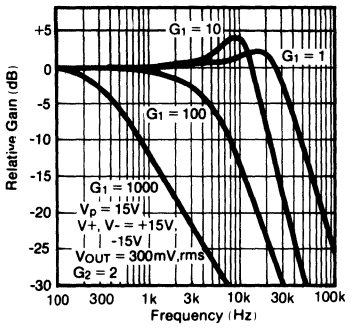
CASE Ceramic
MATING CONNECTOR None
WEIGHT 10 grams (0 35 oz)
PINS Pin material and plating composition to conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3 2)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 080	1 120	27 43	28 45
B	1 080	1 120	27 43	28 45
C	235	300	5 97	7 62
D	018	021	0 46	0 53
F	035	050	0 89	1 27
G	100 BASIC		2 54 BASIC	
H	100 BASIC		2 54 BASIC	
K	150	350	3 81	8 89
L	900 BASIC		22 86 BASIC	
N	002	010	0 05	0 25
R	100 BASIC		2 54 BASIC	

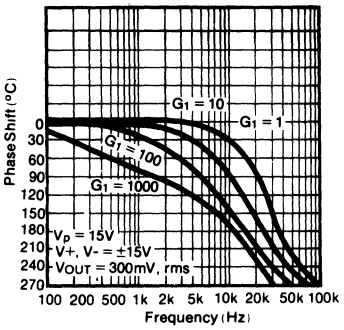
TYPICAL PERFORMANCE CURVES

All specifications typical at +25°C unless otherwise noted

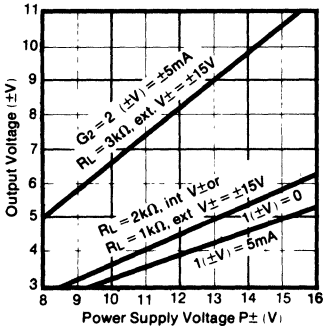
SMALL SIGNAL FREQUENCY RESPONSE



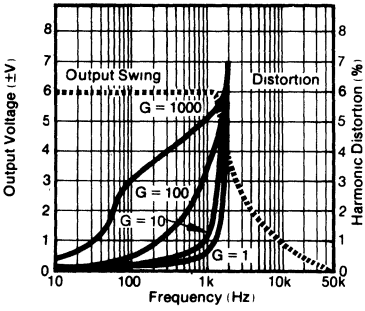
PHASE RESPONSE



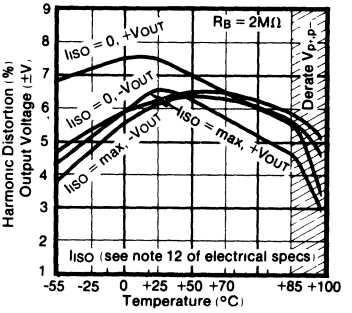
OUTPUT SWING VS SUPPLY VOLTAGE



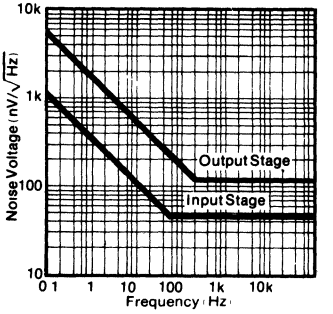
OUTPUT SWING AND DISTORTION VS FREQUENCY



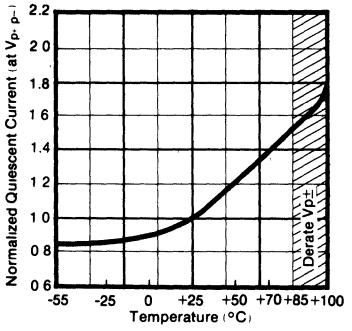
OUTPUT VOLTAGE SWING VS TEMPERATURE AND ISOLATED SUPPLY LOAD



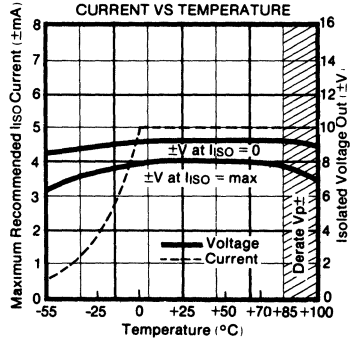
NOISE VOLTAGE VS FREQUENCY



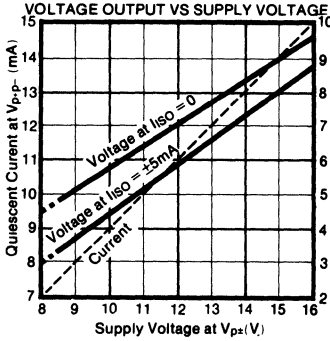
QUIESCENT CURRENT VS TEMPERATURE



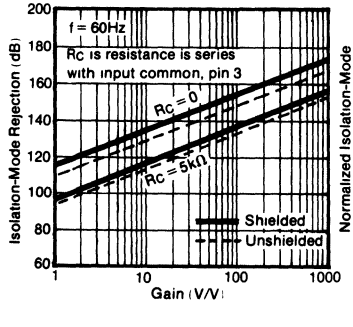
ISOLATED OUTPUT VOLTAGE AND CURRENT VS TEMPERATURE



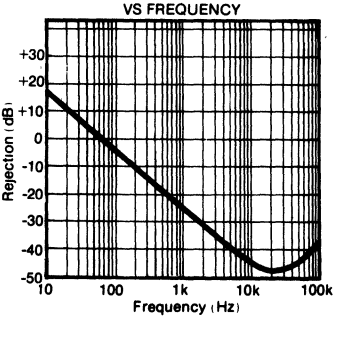
QUIESCENT CURRENT AND ISOLATED VOLTAGE OUTPUT VS SUPPLY VOLTAGE



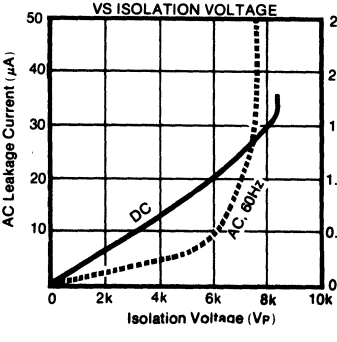
ISOLATION-MODE REJECTION VS GAIN



ISOLATION-MODE REJECTION VS FREQUENCY



AC AND DC LEAKAGE CURRENT VS ISOLATION VOLTAGE



INSTALLATION AND OPERATING INSTRUCTIONS

The 3656 is a very versatile device capable of being used in a variety of isolation and amplification configurations. There are several fundamental considerations that determine configuration and component value constraints:

1. Consideration must be given to the load placed on the resistance (pin 10 and pin 11) by external circuitry. Their output resistance is 100kΩ and a load resistor of 2MΩ or greater is recommended to prevent a voltage divider loading effect in excess of 5%.
2. Demodulator loadings should be closely matched so their output voltages will be equal. (Unequal demodulator output voltages will produce a gain error.) At the 2MΩ level, a matching error of 5% will cause an additional gain error of 0.25%.
3. Voltage swings at demodulator outputs should be limited to 5V. The output may be distorted if this limit is exceeded. This constrains the maximum allowed gains of the input and output stages. Note that the voltage swings at demodulator outputs are tested with 2MΩ load for a minimum of 5V.
4. Total current drawn from the internal isolated supplies must be limited to less than ±5mA per supply and limited to t total of 10mA. In other words, the combination of external and internal current drawn from the internal circuitry which feeds the +V, -V, V+ and V- pins should be limited to 5mA per supply (total current to +V, -V, V+ and V- limited to 10mA). The internal filter capacitors for ±V are 0.01μF. If more than 0.1mA is drawn to provide isolated power for external circuitry (see Figure 12), additional capacitors are required to provide adequate filtering. A minimum of 0.1μF/mA is recommended.
5. The input voltage at pin 7 (noninverting input to A_1) must not exceed the voltage at pin 4 (negative supply voltage for A_1) in order to prevent a possible lockup condition. A low leakage diode connected between pins 7 and 4, as shown in Figure 2, can be used to limit this input voltage swing.
6. Impedances seen by each amplifier's + and - input terminals should be matched to minimize offset voltages caused by amplifier input bias currents. Since the demodulators have a 100kΩ output resistance, the amplifier input not connected to the demodulator should also see 100kΩ.
7. All external filter capacitors should be mounted as close to the respective supply pins as is possible in order to prevent excessive ripple voltages on the supplies or at the output. (Optimum spacing is less than 0.5". Ceramic capacitors recommended.)

POWER AND SIGNAL CONFIGURATIONS

NOTE: Figures 2, 3 and 4 are used to illustrate both signal and power connection configurations. In the circuits shown, the power and signal configurations are independent so that any power configuration could be used with any signal configuration.

ISOLATED POWER CONFIGURATIONS

The 3656 is designed with isolation between the input, the output, and the power connections. The internally generated isolated voltages supplied to A_1 and A_2 may be overridden with external voltages greater than the internal supply voltages. These two features of 3656 provide a great deal of versatility in possible isolation and power supply hook-ups. When external supplies are applied, the rectifying diodes (D_1 through D_4) are reverse biased and the internal voltage sources are decoupled from the amplifiers (see Figure 1). Note that when external supplies are used, they must never be lower than the internal supply voltage.

Three-Port

The power supply connections in Figure 2 show the full three-port isolation configuration. The system has three separate grounds with no galvanic connections between them. The two external 0.47μF capacitors at pins 12 and 16 filter the rectified isolated voltage at the output stage. Filtering on the input stage is provided by internal capacitors. In this configuration continuous isolation voltage ratings are: 3500V between pins 3 and 17; 3500V between pins 3 and 19; 1000V between pins 17 and 19.

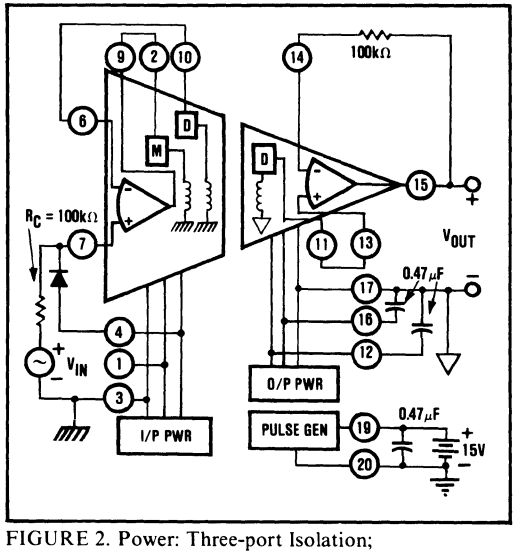


FIGURE 2. Power: Three-port Isolation; Signal: Unity-gain Noninverting.

Two-Port - Bipolar Supply

Figure 3 shows two-port isolation which uses an external bipolar supply with its common connected to the output stage ground (pin 17). One of the supplies (either + or - could be used) provides power to the pulse generator (pins 19 and 20). The same sort of configuration is possible with the external supplies connected to the input stage. With the connection shown, filtering at pins 12 and 16 is not required. In this configuration continuous isolation voltage rating is: 3500VDC between pins 3 and 17; not applicable between pins 17 and 19; 3500VDC between pins 3 and 19.

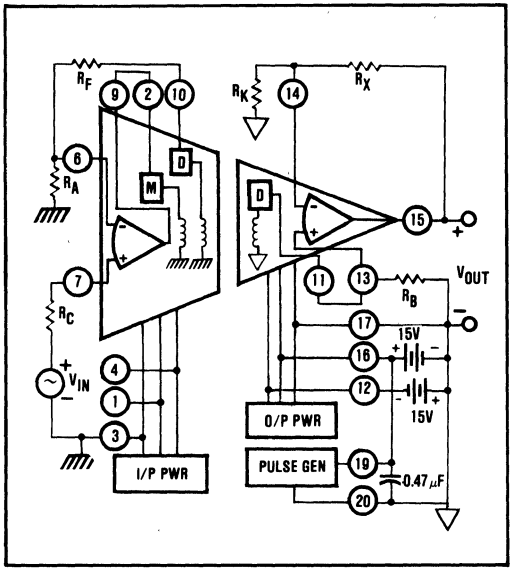


FIGURE 3. Power: Two-port, Dual Supply; Signal: Noninverting Gain.

Two-Port Single Supply

Figure 4 demonstrates two-port isolation using a single polarity supply connected to the output common (pin 17). The other polarity of supply for A_2 is internally generated (thus the filtering at pin 12). This isolated power configuration could be used at the input stage as well and either polarity of supply could be employed. In this configuration continuous isolation voltage rating is: 3500V between pins 3 and 17; 3500V between pins 3 and 19; not applicable between pins 17 and 19.

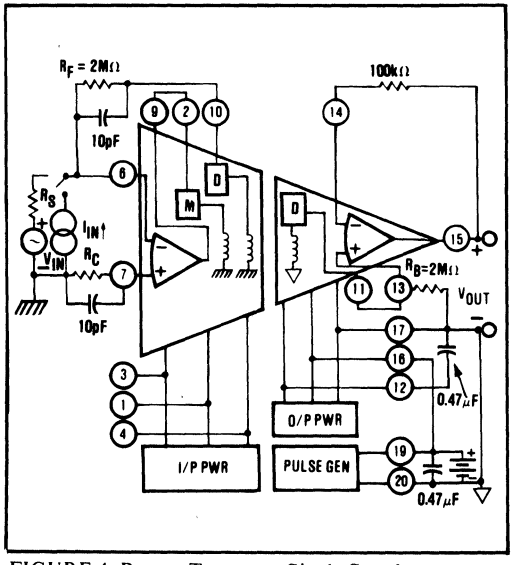


FIGURE 4. Power: Two-port, Single Supply; Signal: Inverting Gains.

SIGNAL CONFIGURATIONS

Unity Gain Noninverting

The signal path portion of Figure 2 shows the 3656 in its simplest gain configuration: unity gain noninverting. The two 100kΩ resistors provide balanced resistances to the inverting and noninverting inputs of the amplifiers. The diode prevents latch up in case the input voltage goes more negative than the voltage at pin 4.

Noninverting With Gain

The signal path portion of Figure 3 demonstrates two additional gain configurations: gain in the otuput stage and noninverting gain in the input stage. The following equations apply:

Total amplifier gain:

$$G = G_1 \bullet G_2 = V_{OUT} / V_{IN} \quad (1)$$

Input Stage:

$G_1 = 1 + (R_F / R_A)$ (Select G_1 to be less than 5V/ full scale V_{IN} to limit demodulator output to 5V) (2)

$R_A + R_F \geq 2M\Omega$ (Select to load input demodulator with at least 2MΩ) (3)

$$R_C = R_A \parallel (R_F + 100k\Omega) = \frac{R_A (R_F + 100k\Omega)}{R_A + R_F + 100k\Omega}$$

(Balance impedances seen by the + and - inputs of A_1 to reduce input offset caused by bias current) (4)

Output Stage:

$G_2 = 1 + (R_X / R_K)$ (Select ratio to obtain V_{OUT} between 5V and 10V full scale with V_{IN} at its maximum) (5)

$R_X \parallel R_K = 100k\Omega$ (Balance impedances seen by the + and - inputs of A_2 to reduce effect of bias current on the output offset) (6)

$R_B = R_A + R_F$ (Load output demodulator equal to input demodulator) (7)

Inverting Gain, Voltage or Current Input

The signal portion of Figure 4 shows two possible inverting input stage configurations: current and input and voltage input.

Input Stage:

For the voltage input case:

$G_1 = -R_F / R_S$ (Select G_1 to be less than 5V/full scale V_{IN} to limit the demodulator output voltage to 5V) (8)

$R_F = 2M\Omega$ (Select to load the demodulator with at least 2MΩ) (9)

$$R_C = R_S \parallel (R_F + 100k\Omega) = \frac{R_S (R_F + 100k\Omega)}{R_S + R_F + 100k\Omega}$$

(Balance the impedances seen by the + and - inputs of A_1). (10)

For the current input case:

$$V_{OUT} = -I_{IN} R_F \bullet G_2 \quad (11)$$

$$R_C = R_F \quad (12)$$

R_F may be made larger than 2MΩ if desired. The 10pF capacitors are used to compensate for the input capacitance of A_1 and to insure frequency stability.

Output Stage:

The output stage is the same as shown in equations (5), (6), and (7).

Illustrative Calculations:

The maximum input voltage is 100mV. It is desired to amplify the input signal for maximum accuracy. Non-inverting output is desired.

Input Stage:

Step 1

G_1 max = 5V/Max Input Signal = 5V 0.1V = 50V/V

With the above gain of 50V/V, if the input ever exceeds 100mV, it would drive the output to saturation. Therefore, it is good practice to allow reasonable input overrange.

So, to allow for 25% input overrange without saturation at the output, select;

$$G_1 = 40V/V$$

$$G_1 = 1 + (R_F + R_A) = 40$$

$$\therefore R_F \; R_A = 39 \quad (13)$$

Step 2

$R_A + R_F$ forms a voltage divider with the 100kΩ output resistance of the demodulator. To limit the voltage divider loading effect to no more than 5%, $R_A + R_F$ should be chosen to be at least 2MΩ. For most applications, the 2MΩ should be sufficiently large for $R_A + R_F$. Resistances greater than 2MΩ may help decrease the loading effect, but would increase the offset voltage drift.

The voltage divider with $R_A + R_F = 2M\Omega$ is $2M\Omega/(2M\Omega + 100k\Omega) = 2/(2 + 0.1) = 95.2\%$, i.e., the percent loading is 4.8%.

Choose $R_A + R_F = 2M\Omega$ (14)

Step 3

Solving equations (13) and (14)

$R_A = 50k\Omega$ and $R_F = 1.95M\Omega$

Step 4

The resistances seen by the + and - input terminals of the input amplifier A_1 should be closely matched in order to minimize offset voltage due to bias currents.

$$\therefore R_C = R_A \parallel (R_F + 100k\Omega)$$
$$= 50k\Omega \parallel (1.95M\Omega + 100k\Omega)$$
$$\approx 49k\Omega$$

Output Stage:

Step 5

$$V_{OUT} = V_{IN\,MAX} \bullet G_1 \bullet G_2$$

As discussed in Step 1, it is good practice to provide 25% input overrange.

So we will calculate G_2 for 10V output and 125% of the maximum input voltage.

$$\therefore V_{OUT} = (1.25 \times 0.1)(G_1)(G_2)$$

i.e., $10V = 0.125 \times 40 \times G_2$

$$\therefore G_2 = 10V/5V = 2V\ V$$

Step 6

$$G_2 = 1 + (R_X/R_K) = 2.0$$

$$\therefore R_X/R_K = 1.0$$

$$\therefore R_X = R_K \quad (15)$$

Step 7

The resistance seen by the + input terminal of the output stage amplifier A_2 (pin 13) is the output resistance 100kΩ of the output demodulator. The resistance seen by the (-) input terminal of A_2(pin14)should be matched to the resistance seen by the + input terminal.

The resistance seen by pin 14 is the parallel combination of R_X and R_K.

$$\therefore R_X \parallel R_K = 100k\Omega$$

i.e., $(R_X \bullet R_K/(R_X + R_K) = 100k\Omega$

i.e., $R_K/[1 + (R_K/R_X)] = 100k\Omega \quad (16)$

Step 8

Solving equations (15) and (16) $R_K = 20k\Omega$ and $R_X = 200k\Omega$.

Step 9

The otuput demodulator must be loaded equal to the input demodulator.

$$\therefore R_B = R_A + R_F = 2M\Omega$$

(See equation (14) above in Step 2)

Use the resistor values obtained in Steps 3, 4, 8 and 9, and connect the 3656 as shown in Figure 3.

OFFSET TRIMMING

Figure 5 shows an optional offset voltage trim circuit. It is important that $R_A + R_F = R_B$.

CASE 1: Input and output stages in low gain, use output potentiometer (R_2) only. Input potentiometer (R_1) may be disconnected. For example, unity gain could be obtained by setting $R_A = R_B = 20M\Omega$, $R_C = 100k\Omega$, $R_1 = 0$, $R_X = 100k\Omega$, and $R_K = \infty$.

CASE 2: Input stage in high gain and output stage in low gain, use input potentiometer (R_1) only. Output potentiometer (R_2) may be disconnected. For example, $G_1 = 100$ could be obtained by setting $R_F = 2M\Omega$, $R_B = 2M\Omega$ returned to pin 17, $R_A = 20k\Omega$, $R_X = 100k\Omega$, and $R_K = \infty$.

CASE 3: When it is necessary to perform a two-stage precision trim (to maintain a very small offset change under conditions of changing temperature and changing gain in A_1 and A_2), use step 1 to adjust the input stage and step 2 for the output stage. Carbon composition resistors are acceptable but potentiometers should be stable.

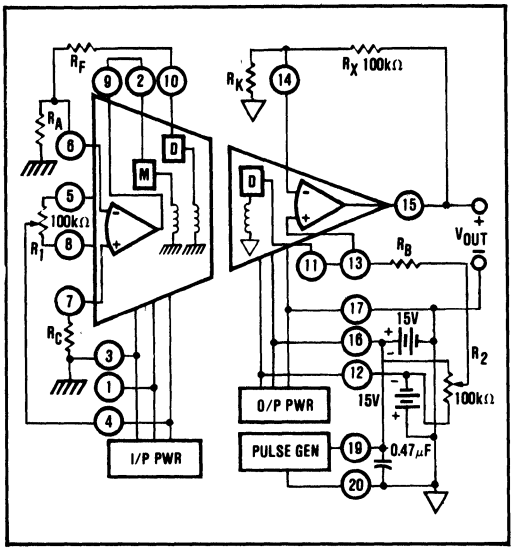


FIGURE 5. Optional Offset Voltage Trim.

Step 1: Input stage trim ($R_A = R_C = 20k\Omega$, $R_1 = R_B = 20M\Omega$, $R_X = 100k\Omega$, $R_K = \infty$, R_2 disconnected); A_1 high, A_2 low gain. Adjust R_1 for 0V ±5mV or desired setting at V_{OUT}, pin 15.

Step 2: Output stage trim ($R_A = R_B = 20M\Omega$, $R_C = 100k\Omega$, $R_F = 0$, $R_X = 100k\Omega$, $R_K = \infty$, R_1 and R_2 connected); A_1 low, A_2 low gain. Adjust R_2 for 0V ±1mV or desired setting at V_{OUT}, pin 15 (±1 f0mV approximate total range).

Note: Other circuit component values can be used with valid results.

APPLICATIONS

ECG AMPLIFIER

Although the features of the circuit shown in Figure 6 are important in patient monitoring applications, they may also be useful in other applications. The input circuitry uses an external, low quiescent current op amp (OPA21 type) powered by the isolated power of the input stage to form a high impedance instrumentation amplifier input (true three-wire input). R_3 and R_4 give the input stage amplifier of the 3656 a noninverting gain of 10 and an inverting gain of -9. R_1 and R_2 give the external amplifier a noninverting gain of 1 + 1 9. The inputs are applied to the noninverting inputs of the two amplifiers and the composite input stage amplifier has a gain of 10.

The 330kΩ, 1W, carbon resistors and diodes D_1 - D_4 provide protection for the input amplifiers from defibrillation pulses.

The output stage in Figure 6 is configured to provide a bandpass filter with a gain of 22.7 (68MΩ/3MΩ). The high-pass section (0.05Hz cutoff) is formed by the 1μF capacitor and 2MΩ resistor which are connected in series between the output demodulator and the inverting input of the output stage amplifier. The low-pass section (100Hz cutoff) is formed by the 68MΩ resistor and 22pF capacitor located in the feedback loop of the output stage. The diodes provide for quick recovery of the high-pass filter to overvoltages at the input. The 100kΩ pot and the 100MΩ resistor allow the output voltage to be trimmed to compensate for increased offset voltage caused by unbalanced impedances seen by the inputs of the output stage amplifier.

In many modern electrocardiographic systems, the

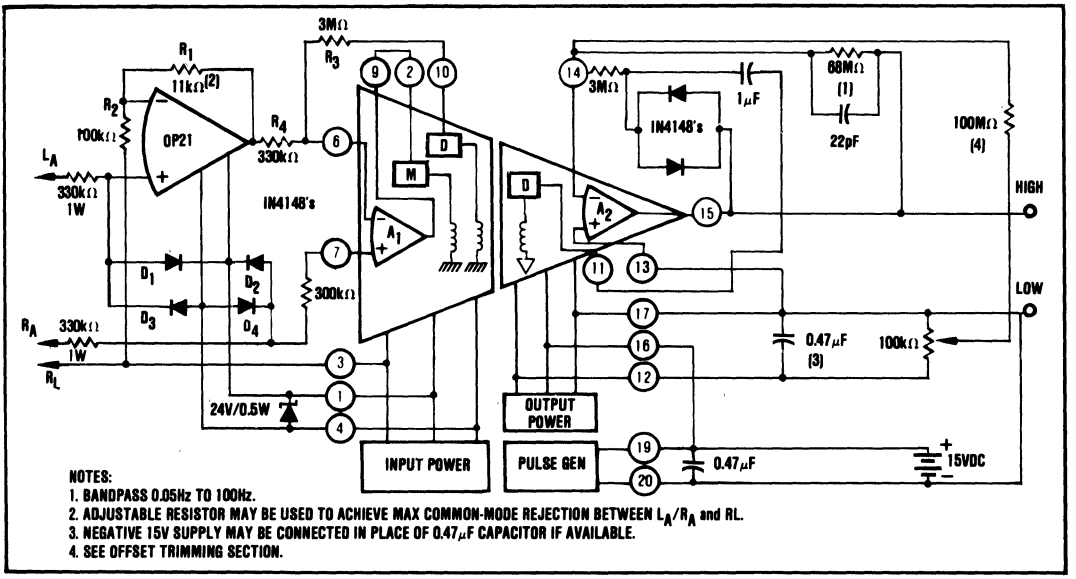


FIGURE 6. ECG Amplifier.

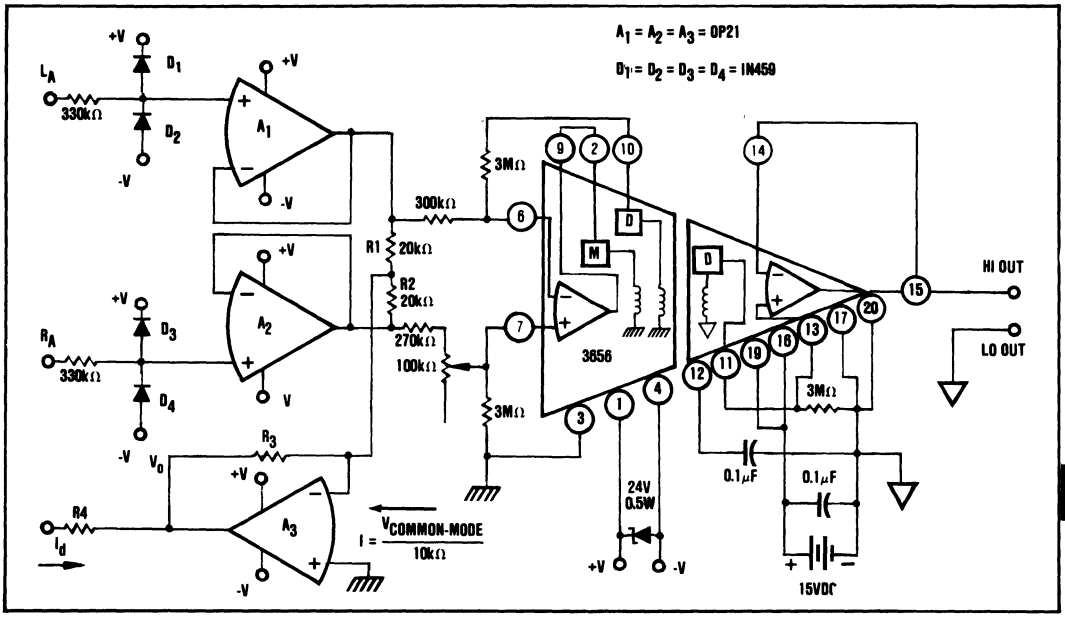


FIGURE 7. Driven Right-Leg ECG Amplifier.

patient is not grounded. Instead, the right-leg electrode is connected to the output of an auxiliary operational amplifier as shown in Figure 7. In this circuit, the common-mode voltage on the body is sensed by the two averaging resistors R_1 and R_2, inverted, amplified, and fed back to the right-leg through resistor R_4. This negative feedback drives the common-mode voltage to a low value. The body's displacement current i_d does not flow to ground, but rather to the output circuit of A_3. This reduces the pickup as far as the ECG amplifier is concerned and effectively grounds the patient.

The value of R_4 should be as large as practical to isolate the patient from ground. The resistors R_3 and R_4 may be selected by these equations:

$$R_3 = (R_1/2)\,(V_o/V_{CM}) \text{ and } R_4 = (V_{CM} - V_o)/I_d$$

$$(-10V \leq V_o \leq +10V \text{ and } -10V \leq V_{CM} \leq +10V)$$

where V_o is the output voltage of A_3 and V_{CM} is the common-mode voltage between the inputs L_A and R_A and the input common at pin 3 of the 3656.

This circuit has the added benefit of having higher common-mode rejection than the circuit in Figure 6 (approximately 10dB improvement).

BIPOLAR CURRENT OUTPUT

The three-port capability of the 3656 can be used to implement a current output isolation amplifier function, usually difficult to implement when grounded loads are involved. The circuit is shown in Figure 8 and the following equations apply:

$$G = I_{OUT}/V_{IN} = 1 + \frac{R_1}{R_A} \times \frac{R_2}{(R_1 + R_2) \bullet R_S}$$

$$I_{OUT} \leq \pm 2.5mA$$

$$V_L \leq \pm 4V \text{ (compliance)}$$

$$R_L \leq 1.6k\Omega$$

$$R_F + R_A = R_1 + R_2 \leq 2M\Omega$$

CURRENT OUTPUT - LARGER UNIPOLAR CURRENTS

A more practical version of the current output function is shown in Figure 9. If the circuit is powered from a source greater than 15V as shown,a three-terminal regulator should be used to provide 15V for the pulse generator (pins 19 and 20). The input stage is configured as a unity gain buffer, although other configurations such as current input could be used. The circuit uses the isolation feature between the output stage and the primary power supply to generate the output current configuration that can work into a grounded load. Note that the output transistors can only drive positive current into the load. Bipolar current output would require a second transistor and dual supply.

ISOLATED 4mA TO 20mA OUTPUT

Figure 10 shows the circuit of an expanded version of the isolated current output function. It allows any input voltage range to generate the 4mA to 20mA output excursion and is also capable of zero suppression. The "span" (gain) is adjusted by R_2 and the "zero" (4mA output for minimum input) is set by the 200kΩ pot in the output stage. A three-terminal 5V reference is used to provide a stable 4mA operating point. The reference is

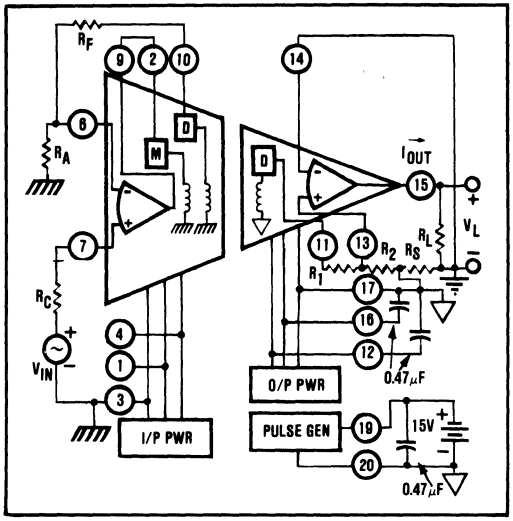


FIGURE 8. Bipolar Current Output.

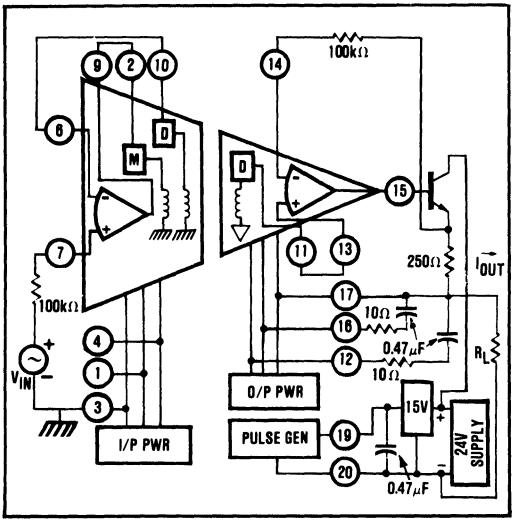


FIGURE 9. Isolated 1 to $5V_{IN}/4$ to 20mA I_{OUT}.

connected to insert an adjustable bias between the demodulator output and the noninverting input of the output stage.

DIFFERENTIAL INPUT

Figure 11 shows the proper connections for differential input configuration. The 3656 is capable of operating in this input configuration only for floating loads (i.e., the source V_{IN} has no connection to the ground reference established at pin 3). For this configuration the usual 2MΩ resistor used in the input stage is split into two halves, R_F and R_{F-}. The demodulator load (seen by pin 10 with respect to pin 3) is still 2MΩ for the floating load as shown. Notice pin 19 is common in Figure 11 whereas pin 20 is common in previous figures.

SERIES STRING SOURCE

Figure 12 shows a situation where a small voltage, which is part of a series string of other voltages, must be measured. The basic problem is that the small voltage to be measured is 500V above the system ground (i.e., a system common-mode voltage of 500V exists). The circuit converts this system CMV to an amplifier isolation mode voltage. Thus, the isolation voltage ratings and isolation-mode rejection specifications apply.

IMPROVED INPUT CHARACTERISTICS

In situations where it is desired to have better DC input amplifier characteristics than the 3656 normally provides it is possible to add a precision operational amplifier as shown in Figure 13. Here the instrumentation grade Burr-Brown 3510 is supplied from the isolated power of the input stage. The 3656 is configured as a unity-gain buffer. The gain of the 3510 stage must be chosen to limit its full scale output voltage to 5V and avoid overdriving the 3656's demodulators. Since the 3656 draws a

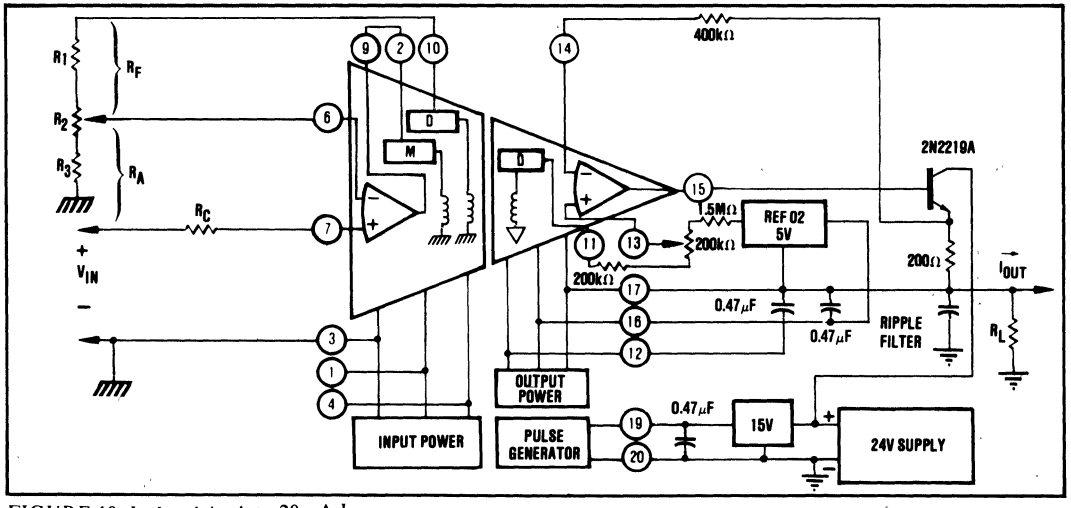


FIGURE 10. Isolated 4mA to 20mA I_{OUT}.

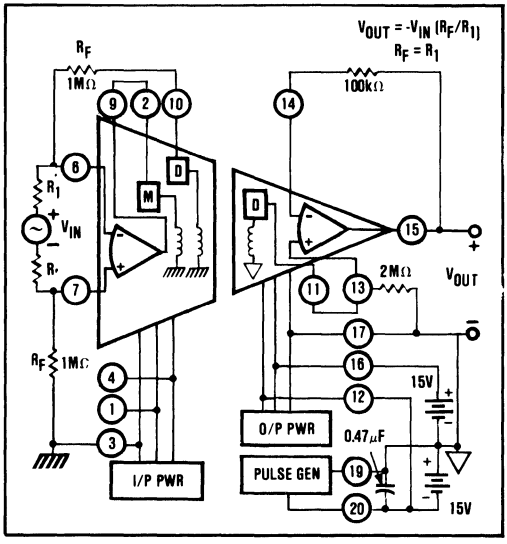


FIGURE 11. Differential Input, Floating Source.

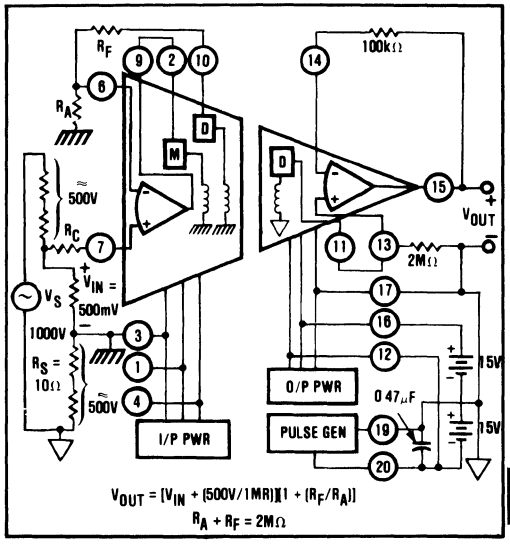


FIGURE 12. Series Source.

significant amount of supply current, extra filtering for the input supply is required as shown (2 x 0.47μF).

ELECTROMAGNETIC RADIATION

The transformer coupling used in the 3656 for isolation makes the 3656 a source of electromagnetic radiation unless it is properly shielded. Physical separation between the 3656 and sensitive components may not give sufficient attenuation by itself. In these applications the use of an electromagnetic shield is a must. A shield, Burr-Brown 100MS, is specially designed for use with the 3656 package. Note that the offset voltage appearing at pin 15 may change by 4mV to 12mV with use of the shield; however, this can be trimmed (see Offset Trimming section).

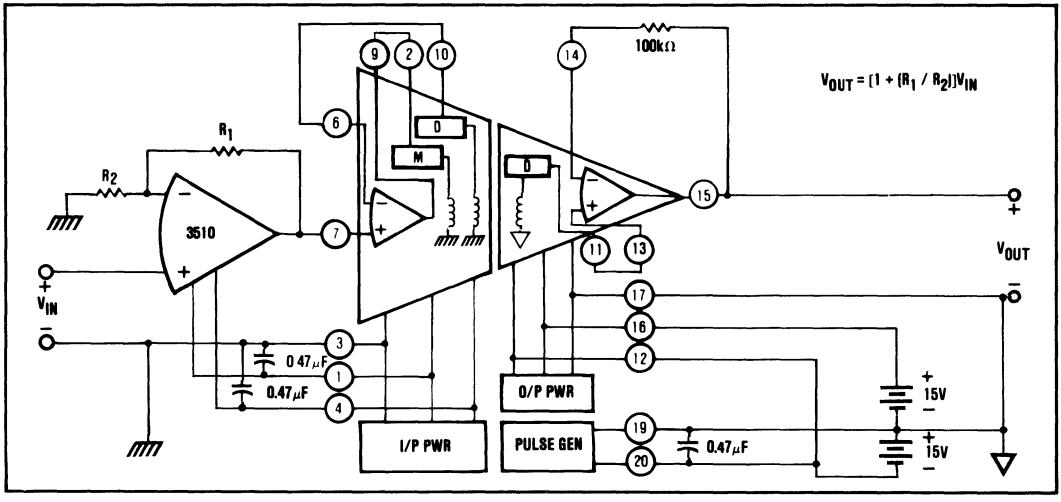
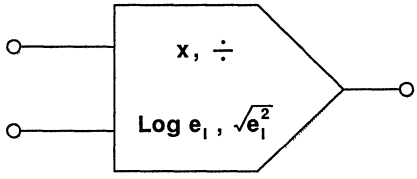


FIGURE 13. Isolator for Low-Level Signals.



ANALOG CIRCUIT FUNCTIONS

5

Analog circuits act as building blocks with which to perform a variety of instrumentation, computation, and control functions. They provide a broad range of versatile, proven, and ready to use computational functions for the designer to use in developing simple or complex systems. The analog circuit functions include multipliers, dividers, multifunction converters, true rms-to-DC converters, logarithmic amplifiers, voltage and window comparators, peak detectors, precision oscillators, and filters. The multifunction converters also provide multiply, divide, square root, exponentiation, roots, sine, cosine, arctangent, vector magnitude rms-to-DC and logarithmic amplifier functions.

The availability of these relatively complex functions as precise, versatile, easy-to-use, low-cost building blocks has broadened the scope of practical analog circuit systems and greatly simplified analog circuit designs. The names of most analog circuit functions are self-explanatory and describe the main functions they perform.

The functions are used mostly for processing and/or conditioning of analog signals, and for simulation of algebraic and/or trigonometric analog computations. The variety of applications these functions are effectively used for, are limited only by the designer's creative imagination. Some of the interesting applications where analog circuit functions have found wide acceptance are listed in the table on the following page.

Types of Applications	Recommended Analog Circuit Function
Analog simulation Algebraic and trigonometric computations Power series approximation, function fitting and linearizing Analog wave shaping	Multiplier, Divider, Multifunction Converter, Logarithmic Amplifier, Oscillator
VCO and AGC applications	Multiplier, Divider
Vector computation	Multifunction Converter, Multiplier
Power and energy measurements	Multiplier, rms-to-DC Converter
Modulation and demodulation	Multiplier, Divider
Signal compression	Logarithmic Amplifier
Log-antilog-log ratio computations	Logarithmic Amplifier
Light-related measurements	Logarithmic Amplifier
Analog signal conditioning	All circuit functions
Instrumentation and control systems	All circuit functions
Test equipment	All circuit functions
Transducer excitation	Oscillator
Signal reference	Oscillator
Alarm circuits	Voltage and Window Comparators
Bang-bang control applications	Voltage and Window Comparators
Control of limit stops	Voltage and Window Comparators
Analog memory and peak detection	Peak Detection

ANALOG CIRCUIT FUNCTIONS SELECTION GUIDES

The Selection Guides show parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

MULTIPLIERS/DIVIDERS

You can select accuracy from 0.25% max and up from this complete line of integrated circuit multipliers. Most provide full four-quadrant multiplication. All are laser-trimmed for accuracy—no trim pots are needed to meet specified performance. These compact models bring the cost of high performance down to acceptable levels.

MULTIPLIERS/DIVIDERS **Boldface = NEW**

Model	Transfer Function	Error at +25°C max (%)	Temp Coeff (%/°C)	Feed-through (mV)	Offset Voltage (mV)	1% BW (kHz)	Temp Range[1]	Pkg	Page
MPY100	$[(X-X_2)(Y-Y_2)/10]+Z_2$	±0.5	0.008	30	7	70	Ind	TO-100	5-26
MPY534	$[(X-X_2)(Y-Y_2)/10]+Z_2$	±0.25	0.008	0.05%	2	3MHz	Com	TO-100	5-34
MPY634M	$[(X-X_2)(Y-Y_2)/10]+Z_2$	±0.5	0.015	0.15%	2	10MHz	Ind	TO-100	5-41
MPY634P	$[(X-X_2)(Y-Y_2)/10]+Z_2$	±2.0	0.03	0.3%	25	10MHz	Ind	DIP	5-41
AD632	**$[(X-X_2)(Y-Y_2)/10]+Z_2$**	**±0.5**	**0.01**	**0.15**	**15**	**50**	**Ind**	**TO-100**	**5-6.**

NOTE: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C.

SPECIAL FUNCTIONS

This group of models offers many different functions that are the quick, easy way to solve a wide variety of analog computational problems. Most are in integrated circuit packages and are laser-trimmed for excellent accuracy.

SPECIAL FUNCTIONS

Function	Model	Description	Comments	Temp Range[1]	Pkg	Page
Multifunction Converter	4302	$Y(Z/X)^m$ This function may be used to multiply, divide, raise to powers, take roots and form sine and cosine functions.	Plastic Package.	Ind	DIP	5-109
	LOG100	$K \log (I_1/I_2)$	Optimized for log ratio of current inputs. Specified over six decades of input (1nA to 1mA), 55mV total error, 0.25% log conformity.	Com	DIP	5-18
Logarithmic Amplifier	4127G 4127P	$K \log (I_1/I_{REF})$	A more versatile part that contains an internal reference and a current inverter. 1% and 0.5% accuracy.	Com Com	DIP DIP	5-102 5-102
$\sqrt{\frac{1}{T}\int_0^T E_{IN}^2(t)\,dt}$	4341	True rms-to-DC conversion based on a log-antilog occupational approach.	Some external trimming required. Lower cost in plastic package. Pin compatible with 4340.	Ind	DIP	5-115
Peak Detector	4085	This is an analog memory circuit that holds and provides readout of a DC voltage equal to peak value of a complex input waveform.	Digital mode control provides reset capability and allows selection of peaks within a desired time interval. Maybe used to make peak-to-peak detector.	Com, Ind	DIP	5-94

NOTE: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C.

DIVIDERS

Using a special log/antilog committed divider design overcomes the major problem encountered when trying to use a multiplier in a divider circuit. Outstanding accuracy is maintained even at very low denominator voltages.

DIVIDERS

Model	Transfer Function	Input Range	Accuracy D = 250mV max (%)	Temp Coeff (%/°C)	0.5% BW (kHz)	Rated Output, min	Temp Range[1]	Pkg	Page
DIV100P	10 x N/D	250mV to 10V	0.25	0.2	15	±10V, ±5mA	Ind	DIP	5-10

NOTE: (1) Ind = –25°C to +85°C.

FREQUENCY PRODUCTS

This group of products consists of precision oscillators and active filters for both signal generation and attenuation. Both fixed frequency and user-selected frequency units are available.

FREQUENCY PRODUCTS

Function	Model	Description	Comments	Temp Range[1]	Pkg	Page
Oscillator	4423	Very-low cost in plastic package Provides resistor programmable quadrature outputs (sine and cosine wave outputs simultaneously available).	Frequency range: 0.002Hz to 20kHz. Frequency stability: 0.01%/°C. Quadrature phase error: ±0.1%.	Com	DIP	5-119
Universal Active Filter	UAF41 UAF21	These filters provide a complex pole pair. Based on state variable approach, low-pass, high-pass, and bandpass outputs are available.	Add only resistors to determine pole location (frequency and Q). Easily cascaded for complex filter responses.	Ind Ind	DIP DIP	5-82 5-74

NOTE: Com = 0°C to +70°C, Ind = –25°C to +85°C.

VOLTAGE REFERENCE

These products are precision voltage references that provide a +10V output. The output can be adjusted with minimal effect on drift or stability.

VOLTAGE REFERENCE

Model	Output (V)	Min Output (mA)	Max Drift (ppm/°C)	Power Supply (V)	Power Supply (mA)	Temp Range[1]	Pkg	Page
REF10M	±10.00 ±0.005	10	1	+13.5/35	4.5	Com	TO-99	5-49
REF101M	±10.00 ±0.005	10	1	+13.5/35	4.5	Com	TO-99	5-55

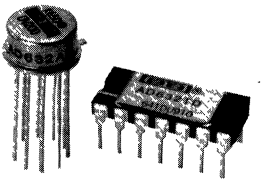
NOTE: (1) Com = 0°C to +70°C.

CURRENT REFERENCE — **Boldface = NEW**

Model	Output I (μA)	Compliance	Max Drift (ppm/°C)	Comments	Temp Range[1]	Pkg	Page
REF200M, P	**Dual 100±0.5**	**2.5V to 40V**	**25**	**Includes 0.5% accurate current mirror**	**Ind**	**DIP, TO-99**	**5-63**

NOTE: (1) Ind = –25°C to +85°C.

BURR-BROWN®



AD632

MILITARY VERSION AVAILABLE

Precision ANALOG MULTIPLIER

FEATURES

- ±0.5% MAX FOUR-QUADRANT ERROR
- ADJUSTABLE SCALE FACTOR: GAINS TO 10X
- STABLE AND RELIABLE MONOLITHIC CONSTRUCTION
- LOW COST
- LOW NOISE

APPLICATIONS

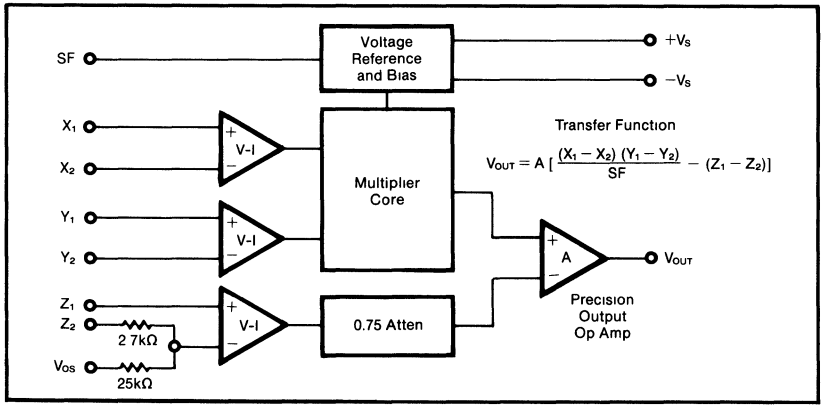
- PRECISION ANALOG-SIGNAL PROCESSING
- VOLTAGE-CONTROLLED FILTERS AND OSCILLATORS
- ALGEBRAIC AND TRIGONOMETRIC FUNCTION SYNTHESIS
- RATIO AND PERCENTAGE COMPUTATION

DESCRIPTION

The AD632 is a high accuracy, general purpose four-quadrant analog multiplier. Its accurate laser-trimmed transfer characteristics enable it to be used in a wide variety of applications with a minimum of external parts and trimming circuitry. Its differential X, Y, and Z inputs allow configuration as a multiplier, squarer, divider, square-rooter, and other functions while maintaining high accuracy.

Its features such as low temperature coefficients, excellent supply rejection and long-term stability of the on-chip thin-film resistors and reference circuitry maintain accuracy even under unfavorable conditions. The low noise of the AD632 enhances its use as a variable-gain differential-input amplifier with high common-mode rejection.

The AD632 has improved specifications over other industry standard devices. An accurate internal voltage reference provides precise setting of the scale factor. The differential Z input allows user-selected scale factors from 0.1 to 10 using external feedback resistors.



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PDS-760

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C $R_L \geq 2k\Omega$ and V_S = ±15VDC unless otherwise specified.

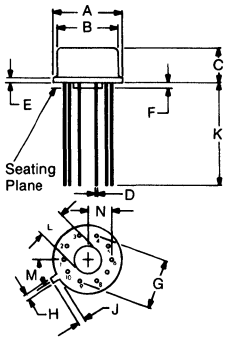
MODEL	AD632A			AD632B			AD632S			AD632T			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
MULTIPLIER PERFORMANCE													
Transfer Function		$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z_2$			*			*			*		
Total Error[1] (−10V ≤ X, Y ≤ +10V)			±1.0			±0.5			*			±0.5	%
T_A = min to max			±1.5			±1.0			±2.0			±1.0	%
Total Error vs. Temperature			±0.02			±0.01			*			±0.01	%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0 25			±0 1			*			±0.1		%
Temperature Coefficient of Scaling Voltage		±0 02			*			*				±0 005	%/°C
Supply Rejection (±15V, ±1V)		±0 01			*			*			*		%
Nonlinearity· X (X = 20Vp-p, Y = 10V)		±0 08	±0 5		*	±0 25		*	*		*	±0 25	%
Y (Y = 20Vp-p, X = 10V)		±0 01			*	±0 1		*			*	±0 1	%
Feedthrough[3], X (Y Nulled, X = 20Vp-p 50Hz)		±0 15	±0 3		±0 05	±0.15		*	*		±0 05	±0 15	%
Feedthrough[3], Y (X Nulled, Y = 20Vp-p 50Hz)		±0 01	±0.1		*	*		*	*		*	*	%
Output Offset Voltage		±5	±30		±2	±15		*	*		±2	±15	mV
Output Offset Voltage Drift		200	400		*	*			500			300	μV/°C
DYNAMICS													
Small Signal BW, (V_{OUT} = 0 1Vrms)		1			*			*			*		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		50			*			*			*		kHz
Slew Rate (V_{OUT} 20Vp-p)		20			*			*			*		V/μs
Settling Time (to 1%, ΔV_{OUT} = 20V)		2			*			*			*		μs
NOISE													
Noise Spectral Density SF = 10V		0.8			*			*			*		μV/√Hz
SF = 3V[4]		0.4			*			*			*		μV/√Hz
Wideband Noise. A = 10Hz to 5MHz		1.0			*			*			*		μVrms
P = 10Hz to 10kHz		90			*			*			*		μVrms
OUTPUT													
Output Voltage Swing	±11			*			*			*			V
Output Impedance (f ≤ 1kHz)		0.1			*			*			*		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			*			*			*		mA
Amplifier Open Loop Gain (f = 50Hz)		70			*			*			*		dB
INPUT AMPLIFIERS (X, Y and Z)													
Input Voltage Range													
Differential V_{IN} (V_{CM} = 0)		±10			*			*			*		V
Common-Mode V_{IN} (V_{DIFF} = 0)		±12			*			*			*		V
Offset Voltage X, Y		±5	±20		±2	±10		*	*		±2	±10	mV
Offset Voltage Drift X, Y		100			50			*			150		μV/°C
Offset Voltage Z		±5	±30		±2	±15		*	*		±2	±15	mV
Offset Voltage Drift Z		200	400		100	200			500			300	μV/°C
CMRR	60	80		70	90		*	*		70	90		dB
Bias Current		0 8	2		*	*		*	*		*	*	μA
Offset Current		0.1			*			*			*		μA
Differential Resistance		10			*			*			*		MΩ
DIVIDER PERFORMANCE													
Transfer Function ($X_1 > X_2$)		$\frac{10V(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$			*			*			*		
Total Error[1]													
X = 10V, −10V ≤ Z ≤ +10V		±0 75			±0 35			*			±0.35		%
X = 1V, −1V ≤ Z ≤ +1V		±2 0			±1 0			*			±1 0		%
0.10V ≤ X ≤ 10V, −10V ≤ Z ≤ 10V		±2 0			±1 0			*			±1.0		%
SQUARER PERFORMANCE													
Transfer Function		$\frac{(X_1 - X_2)^2}{(10V)} + Z_2$			*			*			*		
Total Error (−10V ≤ X ≤ 10V)		±0 6			±0 3			*			±0 3		%
SQUARE-ROOTER PERFORMANCE													
Transfer Function, ($Z_1 \leq Z_2$)		$\sqrt{10V(Z_2 - Z_1)} + X_2$			*			*			*		
Total Error (1V ≤ Z ≤ 10V)		±1 0			±0 5			*			±0.5		%
POWER SUPPLY SPECIFICATIONS													
Supply Voltage Rated Performance		±15			*			*			*		V
Operating	±8		±20	*		*	*		±22	*		±22	V
Supply Current, Quiescent		4	6		*	*		*	*		*	*	mA

*Specification same as AD632A.

NOTES: (1) Numbers given are percent of full-scale, ±10V (i.e., 0.01% = 1mV). (2) May be reduced down to 3V using external resistor between $-V_S$ and SF (3) Irreducible component due to nonlinearity excludes effect of offsets (4) Using external resistor adjusted to give SF = 3V

MECHANICAL

TO-100 Package

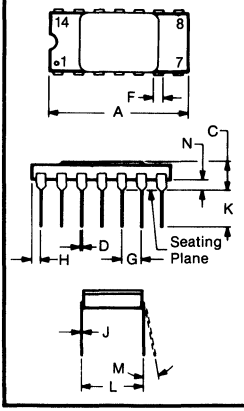


NOTE Leads in true position within 0.010" (0.25mm) R at MMC at seating plane

Pin numbers shown for reference only. Numbers may not be marked on package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.70	—
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

Ceramic Dual-In-Line



NOTE Leads in true position within 0.010" (0.25mm) R at MMC at seating plane

Pin numbers shown for reference only. Numbers may not be marked on package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.009	.060	0.23	1.52

ORDERING INFORMATION

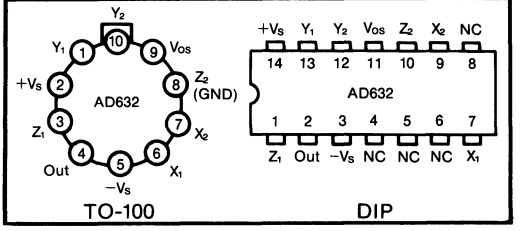
AD632 ( ) ( )

Basic Model Number

Performance Grade
- A, B 0°C to +70°C
- S, T −55°C to +125°C

Package Designator
- H TO-100 metal can
- D 14-pin ceramic DIP

PIN CONFIGURATION (TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

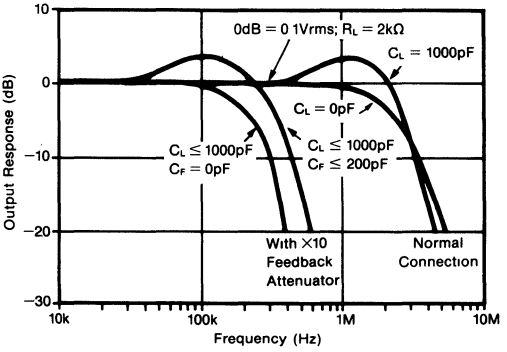
Parameter	AD632A, B	AD632S, T
Power Supply Voltage	±18	±22
Power Dissipation	500mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltage (all X, Y, and Z)	$\pm V_S$	*
Operating Temperature Range	0°C to +70°C	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	*
Lead Temperature (10s soldering)	300°C	*

*Specification same as AD632A

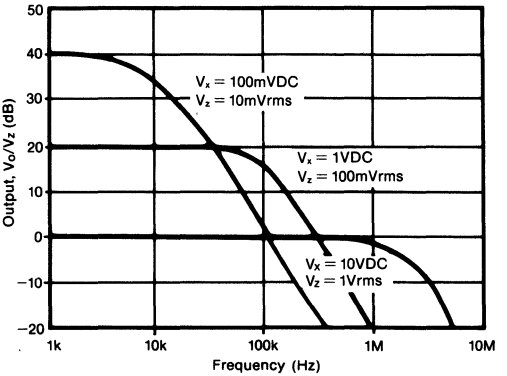
TYPICAL PERFORMANCE CURVES

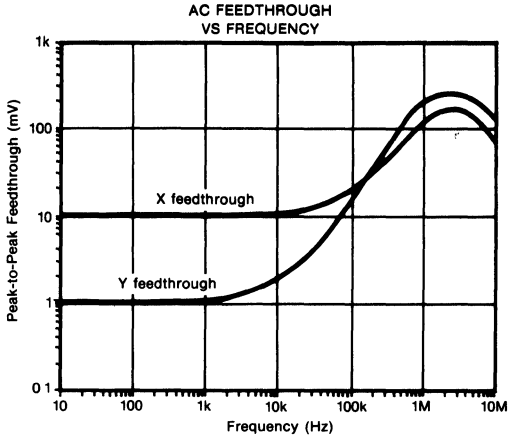
T_A = +25°C, V_S = ±15VDC unless otherwise noted.

FREQUENCY RESPONSE AS A MULTIPLIER



FREQUENCY RESPONSE VS DIVIDER DENOMINATOR INPUT VOLTAGE





THEORY OF OPERATION

BASIC MULTIPLIER CONNECTION

Figure 1 shows the basic connection as a multiplier. Accuracy is fully specified without any additional user-trimming circuitry. Some applications can benefit from trimming one or more of the inputs. The fully-differential inputs facilitate referencing the input quantities to the source-voltage-common terminal for maximum accuracy. They also allow use of simple offset voltage-trimming circuitry as shown on the X input.

The differential Z input allows an offset to be summed in V_{OUT}. In basic multiplier operation the Z_2 input serves as the output-voltage reference and should be connected to the ground reference of the driven system for maximum accuracy.

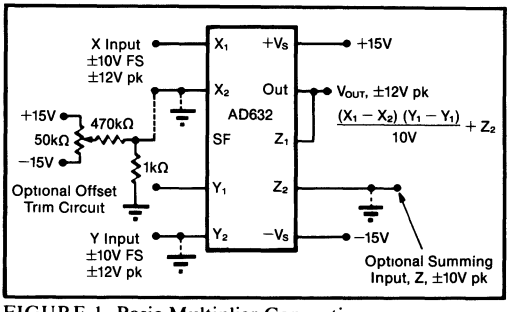


FIGURE 1. Basic Multiplier Connection.

Figure 2 shows a method of changing the effective SF of the overall circuit using an attenuator in the feedback connection to Z_1. This method puts the output amplifier in a higher gain and is thus accompanied by a reduction in bandwidth and an increase in output offset voltage. The larger output offset may be reduced by applying a trimming voltage to the high impedance input, Z_2.

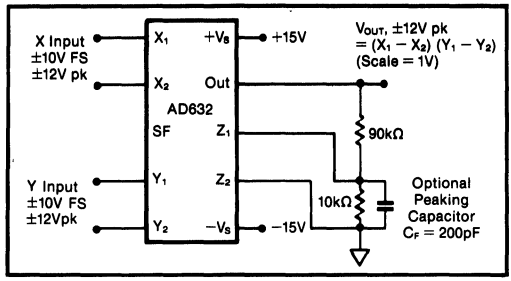


FIGURE 2. Connections for Scale-Factor of Unity.

DIVIDER OPERATION

The AD632 can be configured as a divider as shown in Figure 3. High-impedance differential inputs for the numerator and denominator are achieved at the Z and X inputs respectively. Feedback is applied to the Y_2 input, and Y_1 is normally referenced to output ground. Alternatively, as the transfer function implies, an input applied to Y_1 can be summed directly to V_{OUT}. Since the feedback connection is made to a multiplying input, the effective gain of the output op amp varies as a function of the denominator input voltage. Therefore the bandwidth of the divider function is proportional to the denominator voltage (see Typical Performance Curves).

Accuracy of the divider mode typically ranges from 0.75% to 2.0% for a 10 to 1 denominator range depending on device grade. Accuracy is primarily limited by input-offset voltages and can be significantly improved by trimming the offset of the X input. A trim voltage of ±3.5mV applied to the "low side" X input (X_2 for positive input voltages on X_1) can produce similar accuracies over a 1000 to 1 denominator range. To trim, apply a signal which varies from 100mV to 10V at a low frequency (less than 500Hz) to both inputs. An offset sine wave or ramp is suitable. Since the ratio of the quantities should be constant, the ideal output would be a constant 10V. Using AC coupling on an oscilloscope, adjust the offset control for minimum output voltage variation.

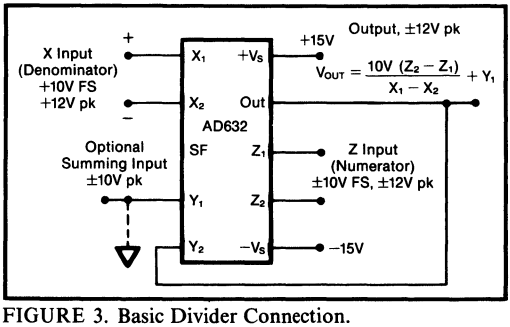


FIGURE 3. Basic Divider Connection.

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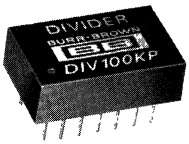
DIV100



ANALOG DIVIDER

FEATURES

- **HIGH ACCURACY**
  0.25% maximum error, 40:1 denominator range
- **TWO-QUADRANT OPERATION**
  Dedicated log-antilog technique
- **EASY TO USE**
  Laser-trimmed to specified accuracy - no external resistors needed
- **LOW COST**
- **DIP PACKAGE**

APPLICATIONS

- **DIVISION**
- **SQUARE ROOT**
- **RATIOMETRIC MEASUREMENT**
- **PERCENTAGE COMPUTATION**
- **TRANSDUCER AND BRIDGE LINEARIZATION**
- **AUTOMATIC LEVEL - AND GAIN - CONTROL**
- **VOLTAGE CONTROLLED AMPLIFIERS**
- **ANALOG SIMULATION**

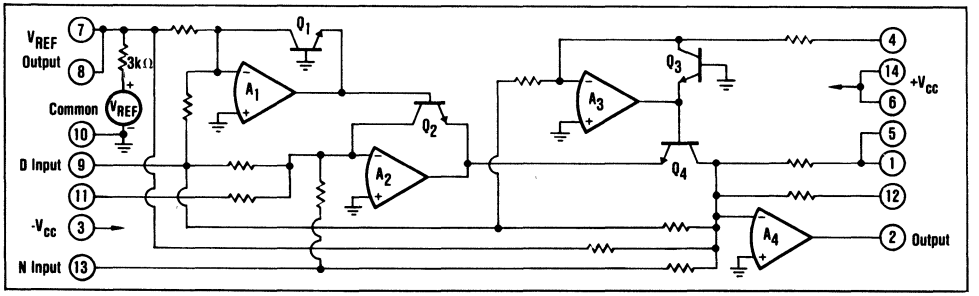
DESCRIPTION

The DIV100 is a precision two-quadrant analog divider offering superior performance over a wide range of denominator input. Its accuracy is nearly two orders of magnitude better than multipliers used for division. It consists of four operational amplifiers and logging transistors integrated into a single monolithic circuit and a laser-trimmed, thin-film resistor network. The electrical characteristics of these devices offer the user guaranteed accuracy without the need for external adjustment - the DIV100 is a complete, single package analog divider.

For those applications requiring higher accuracy than the DIV100 specifies the capability for optional adjustment is provided. These adjustments allow the user to set scale factor, feedthrough, and output-referred offsets for the lowest total divider error.

The DIV100 also gives the user a precision, temperature-compensated reference voltage for external use.

Designers of industrial process control systems, analytical instruments, or biomedical instrumentation will find the DIV100 easy to use and also a low cost, but highly accurate solution to their analog divider applications.



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PDS-427A

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and ±V_{CC} = 15VDC unless otherwise noted.

MODEL		DIV100HP			DIV100JP			DIV100KP			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TRANSFER FUNCTION			V_O = 10N/D			*			*		
ACCURACY	$R_L \geq 10k\Omega$										
Total Error											
Initial	0.25V ≤ D ≤ 10V, N ≤ | D |		0.7	1.0		0.3	0.5		0.2	0.25	% FSO(1)
vs. Temperature	1V ≤ D ≤ 10V, N ≤ | D |		0.02	0.05(2)		*	*		*	*	% FSO/°C
	0.25V ≤ D ≤ 1V, N ≤ | D |		0.06	0.2(2)		*	*		*	*	% FSO/°C
vs. Supply	0.25V ≤ D ≤ 10V, N ≤ | D |		0.15			*			*		% FSO/%
Warm-up time to rated performance			5			*			*		Minutes
AC PERFORMANCE	D = +10V										
Small-Signal Bandwidth	-3dB		350			*			*		kHz
0.5% Amplitude Error	Small-Signal		15			*			*		kHz
0.57° Vector Error	Small-Signal		1000			*			*		Hz
Full-Power Bandwidth	V_O = ±10V, I_O = ±5mA		30			*			*		kHz
Slew Rate	V_D = ±10V, I_O = ±5mA		2			*			*		V/µsec
Settling Time	ε = 1%, ΔV_O = 20V		15			*			*		µsec
Overload Recovery	50% Output Overload		4			*			*		µsec
INPUT CHARACTERISTICS											
Input Voltage Range											
Numerator	N ≤ | D |	±10			*			*			V
Denominator	D ≥ +250mV	+10			*			*			V
Input Resistance	Either Input		25			*			*		kΩ
OUTPUT CHARACTERISTICS											
Full-Scale Output (FSO)		±10			*			*			V
Rated Output											
Voltage	I_O = ±5mA	±10			*			*			V
Current	V_O = ±10V	±5			*			*			mA
Current Limit											
Positive			15	20(2)		*			*		mA
Negative			19	23(2)		*			*		mA
OUTPUT NOISE VOLTAGE	N = 0V										
f_B = 10Hz to 10kHz											
D = +10V			370			*			*		µV, rms
D = +250mV			1			*			*		mV, rms
REFERENCE VOLTAGE CHARACTERISTICS	$R_L \geq 10M\Omega$										
Output Voltage											
Initial	At +25°C	6.3(2)	6.6	6.9(2)	*	*	*	*	*	*	V
vs. Supply			±25			*			*		µV/V
Temperature Coefficient			±50			*			*		ppm/°C
Output Resistance			3			*			*		kΩ
POWER SUPPLY REQUIREMENTS											
Rated Voltage			±15			*			*		VDC
Operating Range	Derated Performance	±12		±20	*		*	*		*	VDC
Quiescent Current											
Positive Supply			5	7(2)		*	*		*	*	mA
Negative Supply			8	10(2)		*	*		*	*	mA
AMBIENT TEMPERATURE RANGE											
Specification		0		+70	*		*	*		*	°C
Operating Range	Derated Performance	-25		+85	*		*	*		*	°C
Storage		−40		+85	*		*	*		*	°C

*Same as DIV100HP.

NOTES: (1) FSO is the abbreviation for Full Scale Output. (2) This parameter is untested and is not guaranteed. This specification is established to a 90% confidence level. (3) See General Information section for discussion. (4) For supply voltages less than ±20VDC, the absolute maximum input voltage is equal to the supply voltage. (5) Short-circuit may be to ground only. Rating applies to an ambient temperature of +38°C at rated supply voltage.

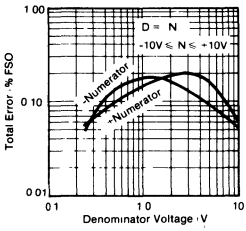
ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation(3)	600mW
Input Voltage Range(4)	±20VDC
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	−25°C to +85°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-Circuit Duration(3)(5)	Continuous
Junction Temperature	+175°C

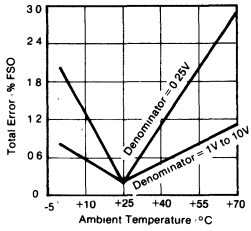
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted

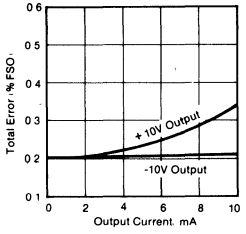
TOTAL ERROR VS DENOMINATOR VOLTAGE



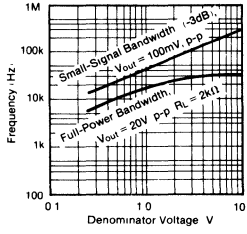
TOTAL ERROR VS AMBIENT TEMPERATURE



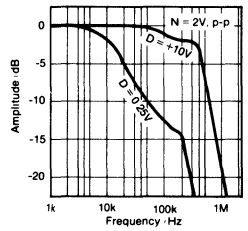
TOTAL ERROR VS OUTPUT CURRENT



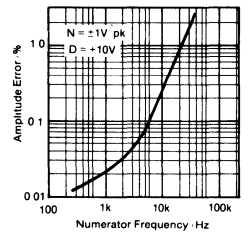
FREQUENCY RESPONSE VS DENOMINATOR VOLTAGE



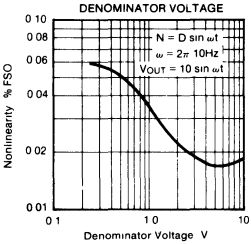
SMALL-SIGNAL FREQUENCY RESPONSE



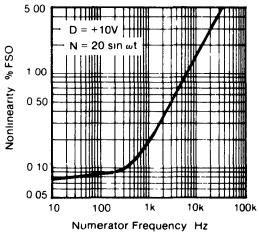
AMPLITUDE ERROR VS NUMERATOR FREQUENCY



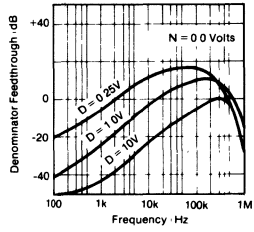
NONLINEARITY VS DENOMINATOR VOLTAGE



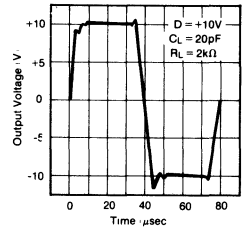
NONLINEARITY VS NUMERATOR FREQUENCY



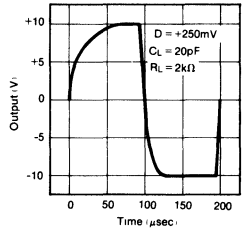
DENOMINATOR FEEDTHROUGH VS DENOMINATOR FREQUENCY



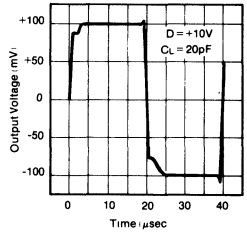
LARGE SIGNAL STEP RESPONSE



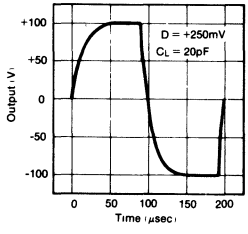
LARGE SIGNAL STEP RESPONSE



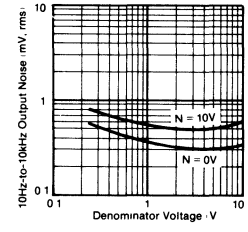
TRANSIENT RESPONSE



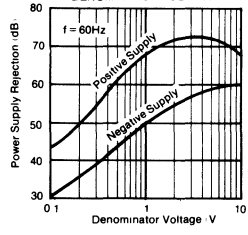
TRANSIENT RESPONSE



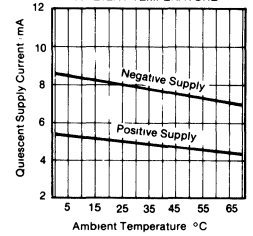
OUTPUT NOISE VS DENOMINATOR VOLTAGE



POWER SUPPLY REJECTION VS DENOMINATOR VOLTAGE

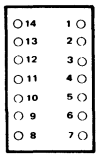


QUIESCENT CURRENT VS AMBIENT TEMPERATURE



PIN CONFIGURATION

1 Gain Error Adjust
2 Output
3 -V_{CC}
4 D Input Offset Adjust
5 Internally Connected to Pin 1
6 Internally Connected to Pin 14
7 Internally Connected to Pin 8
8 Reference Voltage
9 Denominator (D) Input
10 Common
11 N Input Offset Adjust
12 Output Offset Adjust
13 Numerator (N) Input
14 +V_{CC}



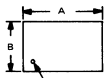
(Bottom View)

MECHANICAL

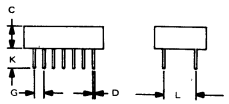
ORDER NUMBER { DIV100HP, DIV100JP, DIV100KP

CASE Epoxy
WEIGHT 2.7 Grams
CONNECTOR 0145MC

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92



NOTE
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane



Pin numbers shown for reference only. Numbers are not marked on package.

DEFINITIONS

TRANSFER FUNCTION

The ideal transfer function for the DIV100 is:

$V_{out} = 10 \frac{N}{D}$

where: N = Numerator input voltage
D = Denominator input voltage
10 = Internal scale factor

Figure 1 shows the operating region over the specified numerator and denominator ranges. Note that below the minimum denominator voltage (250mV) operation is undefined

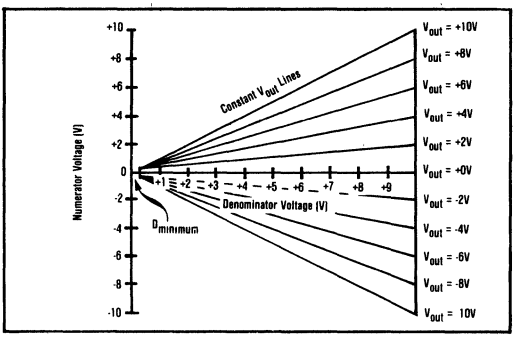


FIGURE 1. Operating Region.

ACCURACY

Accuracy is specified as a percentage of full-scale output (FSO). It is derived from the total error specification.

TOTAL ERROR

Total error is the deviation of the actual output from the ideal quotient 10N/D expressed in percent of FSO(10V); e.g., for the DIV100K:

$V_{out\ (actual)} = V_{out\ (ideal)} \pm$ total error,

where, Total error = 0.25% FSO = 25mV.

It represents the sum of all error terms normally associated with a divider: numerator nonlinearity, denominator nonlinearity, scale-factor error, output-referred numerator and denominator offsets, and the offset due to the output amplifier. Individual errors are not specified because it is their sum that affects the user's application.

SMALL-SIGNAL BANDWIDTH

Small-signal bandwidth is the frequency the output drops to 70% (-3dB) of its DC value. The input signal must be low enough in amplitude to keep the divider's output from becoming slew-rate limited. A rule-of-thumb is to make the output voltage 100mV, p-p, when testing this parameter. Small-signal bandwidth is directly proportional to denominator magnitude as described in the Typical Performance Curves.

0.5% AMPLITUDE ERROR

At high frequencies the input-to-output relationship is a complex function that produces both a magnitude and vector error. The 0.5% amplitude error is the frequency at which the magnitude of the output drops 0.5% from its DC value.

0.57° VECTOR ERROR

The 0.57° vector error is the frequency at which a phase error of 0.01 radians occurs. This is the most sensitive measure of dynamic error of a divider.

LINEARITY

Defining linearity for a nonlinear device may seem unnecessary; however, by keeping one input constant the output becomes a linear function of the remaining input. The denominator is the input that is held fixed with a divider. Nonlinearities in a divider add harmonic distortion to the output in the amount of:

$$\text{Percent Distortion} \approx \frac{\text{Percent Nonlinearity}}{\sqrt{2}}$$

FEEDTHROUGH

Feedthrough is the signal at the output for any value of denominator within its rated range, when the numerator input is zero. Ideally the output should be zero under this condition.

GENERAL INFORMATION

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the $+V_{CC}$ and $-V_{CC}$ pins to the power supply common. The connection of these capacitors should be as close to the DIV100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads of up to 1000pF, typically. Higher capacitive loads can be driven if a 22Ω carbon resistor is connected in series with the DIV100's output.

OVERLOAD PROTECTION

The DIV100 can be protected against accidental power supply reversal by putting a diode (1N4001, type) in series with each power supply line as shown in Figure 2. This precaution is necessary only in power systems that momentarily reverse polarity during turn-on or turn-off.

If this protection circuit is used, the accuracy of the DIV100 will be degraded by the power supply sensitivity specification. No other overload protection circuit is necessary. Inputs are internally protected against overvoltages and they are current-limited by at least a 10kΩ series resistor. The output is protected against short circuits to power supply common only.

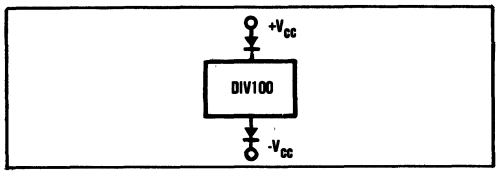


FIGURE 2. Overload Protection Circuit.

STATIC SENSITIVITY

No special handling is required. The DIV100 does not use MOS-type transistors. Furthermore, all external leads are protected by resistors against low energy electrostatic discharge (ESD).

INTERNAL POWER DISSIPATION

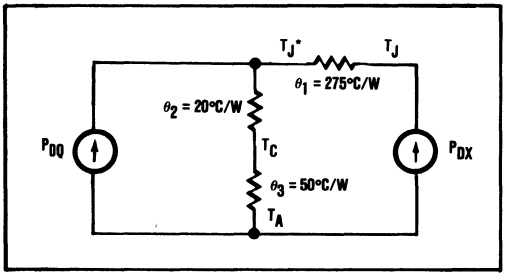


FIGURE 3. DIV100 Thermal Model.

Figure 3 is the thermal model for the DIV100 where:

P_{DQ} = Quiescent Power Dissipation
$= |+V_{CC}|\ I_{+QUIESCENT} + |-V_{CC}|\ I_{-QUIESCENT}$

P_{DX} = Worst case power dissipation in the output transistor
$= V_{CC}^2/4R_{LOAD}$ (for normal operation)
$= V_{CC}\ I_{(output\ limit)}$ (for short-circuit)

T_J = Junction Temperature (output loaded)
T_J* = Junction Temperature (no load)
T_C = Case Temperature
T_A = Ambient Temperature
θ = Thermal Resistance

This model is obviously not the simple one power source model that most linear device manufacturers give. It is, however, a more accurate model for a multidevice monolithic or hybrid integrated circuit.

The model in Figure 3 must be used in conjunction with the DIV100's absolute maximum ratings of internal power dissipation and junction temperature to determine the derated power dissipation capability of the package.

As an example of how to use this model, consider this problem:

Determine the highest ambient temperature at which the DIV100 may be operated with a continuous short circuit to ground. $V_{CC} = \pm 15VDC$.

$P_{D(max)} = 600mW$. $T_{J(max)} = +175°C$.

$T_A = T_{J(max)} - P_{DQ}(\theta_2 + \theta_3) - P_{DX(short=circuit)}(\theta_1+\theta_2+\theta_3)$
$= 175°C - 18°C - 119°C = 38°C$

$P_{D(actual)} = P_{DQ} + P_{DX(short=circuit)} \leqslant P_{D(max)}$
$= 255mW + 345mW = 600mW$

The conclusion is that the device will withstand a short-circuit up to $T_A = +38°C$ without exceeding either the 175°C or 600mW absolute maximum limits.

LIMITING OUTPUT VOLTAGE SWING

The negative output voltage swing should be limited to ±11V, maximum, to prevent polarity inversion and possible system instability. This should be done by limiting the input voltage range.

THEORY OF OPERATION

The DIV100 is a log-antilog divider consisting of four operational amplifiers and four logging transistors integrated into a single monolithic circuit. Its basic principal of operation can be seen by an analysis of the circuit in Figure 4.

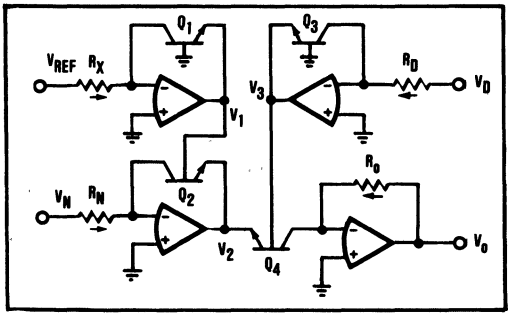


FIGURE 4. One-Quadrant Log-Antilog Divider.

The logarithmic equation for a biopolar transistor is:

$$V_{BE} = V_T \ln(I_c/I_s), \quad (1)$$

where: $V_T = kT/q$
k = Boltzmann's constant = 1.381×10^{-23}
T = Absolute temperature in degrees Kelvin
q = Electron charge = 1.602×10^{-19}
I_c = Collector current
I_s = Reverse saturation current

Applying equation (1) to the four logging transistors gives:

For Q_1:
$V_{BE} = V_B - V_E = V_T[\ln(V_{REF}/R_X - \ln I_s]$

This leads to:
$V_1 = -V_T[\ln(V_{REF}/R_X - \ln I_s]$

For Q_2:
$V_1 - V_2 = V_T[\ln(V_N/R_N) - \ln I_S]$

For Q_3:
$V_3 = -V_T[\ln(V_D/R_D) - \ln I_S]$

We have now taken the logarithms of the input voltage V_{REF}, V_N, and V_D. Applying equation (1) to Q_4 gives:
$V_3 - V_2 = V_T[\ln(V_o/R_o) - \ln I_s]$.

Assume V_T and I_s are the same for all four transistors (a reasonable assumption with a monolithic IC). Solving

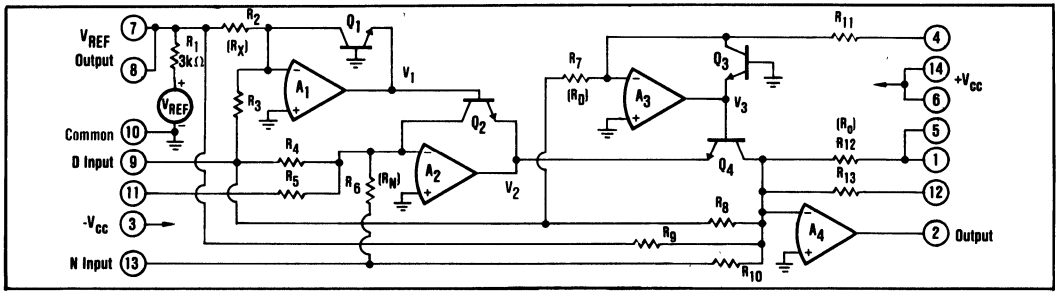


FIGURE 5. DIV100 Two-Quadrant Log-Antilog Circuit.

this last equation in terms of the previously defined variables and taking the antilogarithm of the result yields:

$$V_o = \frac{V_{REF} V_N R_o R_D}{V_D R_X R_N} \quad (2)$$

In the DIV100 $V_{REF} = 6.6V$, $R_o = R_X = R_D$, and R_X is such that the transfer function is:

$$V_o = 10\ N\ D \quad (3)$$

where: N = Numerator Voltage
D = Denominator Voltage

Figure 5 is a more detailed circuit diagram for the DIV100. In addition to the circuitry included in Figure 3, it also shows the resistors (R_3, R_4, R_8, R_9, and R_{10}) used for level-shifting. This converts the DIV100 to a two-quadrant divider.

The implementation of the transfer function is equation (3) is done using devices with real limitations. For example, the value of the D input must always be positive. If it isn't, Q_3 will no longer conduct, A_3 will become open loop, and its output and the DIV100 output will saturate. This limitation is further restricted in that if the D input is less than +250mV the errors will become substantial. It will still function, but its accuracy will be less.

Still another limitation is the value of the N input must always be equal to or less than the absolute value of the D input. From equation (3) it can be seen that if this limitation is not met V_o will try to be greater than the 10V output voltage limit of A_4.

A limitation that may not be obvious is the effect of source resistance. If the numerator or denominator inputs are driven from a source with more than 10Ω of output resistance, the resultant voltage divider will cause a significant output error. This voltage divider is formed by the source resistance and the DIV100 input resistance. With $R_{SOURCE} = 10\Omega$ and $R_{INPUT\ (DIV100)} = 25k\Omega$ an error of 0.04% results. This means that the best performance of the DIV100 is obtained by driving its inputs from operational amplifiers.

Note that the reference voltage is brought out to pins 7 and 8. This gives the user a precision, temperature-compensated reference for external use. Its open-circuit voltage is +6.6VDC, ±0.075V, typically. Its Thevenin equivalent resistance is 3kΩ. Since the output resistance is a relatively high value, an operational amplifier is necessary to buffer this source as shown in Figure 6. The external amplifier is necessary because current drawn through the 3kΩ resistor will effect the DIV100 scale factor.

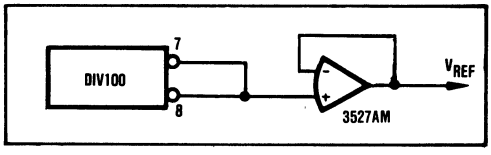


FIGURE 6. Buffered Precision Voltage Reference.

OPTIONAL ADJUSTMENTS

Figure 7 shows the connections to make to adjust the DIV100 for significantly better accuracy over its 40-to-1 denominator range.

The adjustment procedure is:

1. **Begin with R_1, R_2, and R_3 set to their mid-position.**
2. **With $|N| = D = 10.000V$, ±1mV, adjust R_1 for $V_o = +10.000V$, ±1mV. This sets the scale factor.**
3. **Set D to the minimum expected denominator voltage. With $N = -D$, adjust R_2 for $V_o = -10.000V$. This adjusts the output referred denominator offset errors.**
4. **With D still at its minimum expected value, make $N = D$. Adjust R_3 for $V_o = 10.000V$. This adjusts the output referred offset errors.**
5. **Repeat steps 2-4 until the best accuracy is obtained.**

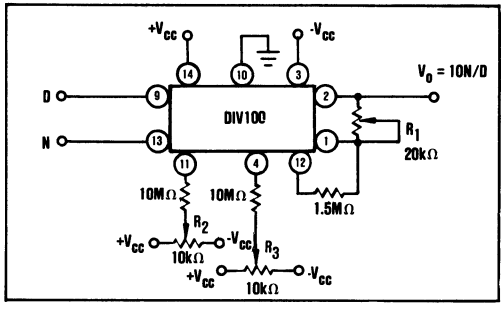


FIGURE 7. Connection Diagram for Optional Adjustments.

TYPICAL APPLICATIONS

CONNECTION DIAGRAM

Figure 8 is applicable to each application discussed in this section, except the square root mode.

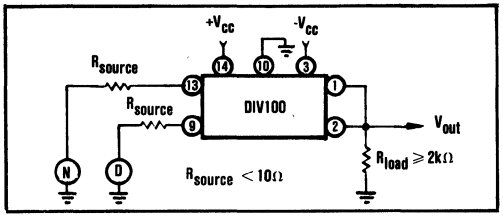


FIGURE 8. Connection Diagram - Divide Mode.

RATIOMETRIC MEASUREMENT

The DIV100 is useful for ratiometric measurements such as efficiency, elasticity, stress, strain, percent distortion, impedance magnitude, and fractional loss or gain. These ratios may be made for instantaneous, average, RMS, or peak values.

The advantage of using the DIV100 can be illustrated from the example shown in Figure 9.

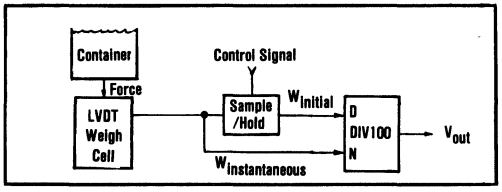


FIGURE 9. Weighing System - Fractional Loss.

The LVDT (Linear Variable Differential Transformer) weigh cell measures the force exerted on it by the weight of the material in the container. Its output is a voltage proportional to:

$$W = \frac{Fg}{a}$$

where: W = Weight of material
F = Force
g = Acceleration due to gravity
a = Acceleration (acting on body of weight W)

In a fractional loss weighing system the initial value of the material can be determined by the volume of the container and the density of the material. If this value is then held on the D-input to the DIV100 for some time interval, the DIV100 output will be a measure of the instantaneous fractional loss:

Loss (L) = $W_{INSTANTANEOUS}/W_{INITIAL}$

Note that by using the DIV100 in this application the common physical parameters of g and a have been eliminated from the measurement, thus eliminating the need for precise system calibration.

The output from a ratiometric measuring system may also be used as a feedback signal in an adaptive process control system. A common application in the chemical industry is in the ratio control of a gas and liquid flow as illustrated in Figure 10.

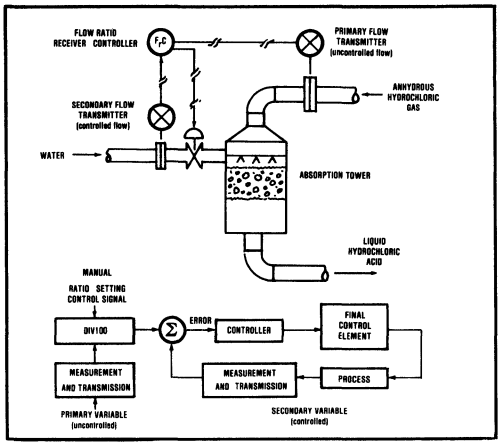


FIGURE 10. Ratio Control of Water to Hydrochloric Gas

PERCENTAGE COMPUTATION

A variation of the direct ratiometric measurements previously discussed is the need for percentage computation. In Figure 11 the DIV100 output varies as the percent deviation of the measured variable to the standard.

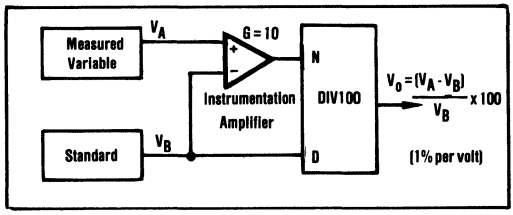


FIGURE 11. Percentage Computation.

TIME AVERAGING

The circuit in Figure 12 overcomes the fixed averaging interval and crude approximation of more conventional time averaging schemes.

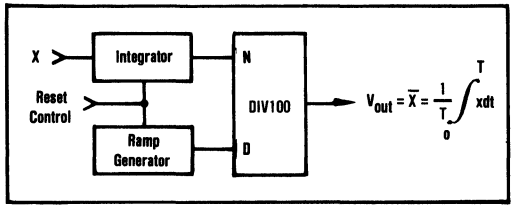


FIGURE 12. Time Averaging Computation Circuit.

BRIDGE LINEARIZATION

The bridge circuit in Figure 13 is fundamental to pressure, force, strain and electrical measurements. It can have one or more active arms whose resistance is a function of the physical quantity, property, or condition that is being measured; e.g., force of compression. For the sake of explanation the bridge in Figure 13 has only one active arm.

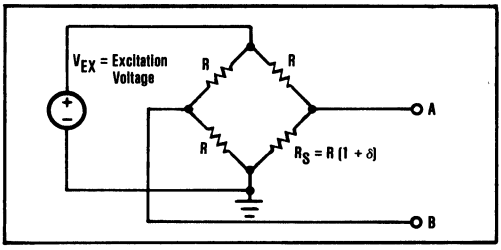


FIGURE 13. Bridge Circuit.

The differential output voltage V_{BA} is:

$$V_{BA} = V_B - V_A \quad \frac{-V_{IX}\delta}{2(2+\delta)},$$

a nonlinear function of the resistance change in the active arm. This nonlinearity limits the useful span of the bridge to perhaps ±10% variation in the measured parameter.

Bridge linearization is accomplished using the circuit in Figure 14. The instrumentation amplifier converts the differential output to a single-ended voltage needed to drive the divider. The voltage-divider string makes the numerator and denominator voltages:

$$N = \frac{-V_{IX}\delta R_{IN}}{(2R_1 + 3R_{in})(2+\delta)}, \text{and,}$$

$$D = \frac{2 V_{IX} R_{ID}}{(2R_1 + 3R_{ID})(2+\delta)}, \text{ respectively,}$$

where: R_{IN} = DIV100 numerator input resistance
R_{ID} = DIV100 denominator input resistance

Applying these voltages to the DIV100 transfer function gives:

$$V_o = 10N\ D \quad \frac{(2R_1 + 3R_{ID})(R_{IN}\delta)\ 10}{(2R_1 + 3R_{IN})(2R_{ID})},$$

which reduces to:

$V_o = -5\delta$

if the divider's input resistances are equal.

The nonlinearity of the bridge has been eliminated and the circuit output is independent of variations in the excitation voltage.

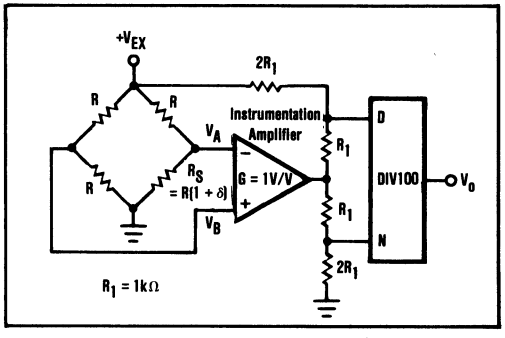


FIGURE 14. Bridge Linearization Circuit.

AUTOMATIC GAIN CONTROL

A simple AGC circuit using the DIV100 is shown in Figure 15. The numerator voltage may vary both positive and negative. The divider's output is half-wave rectified and filtered by D_1, R_3, and C_2. It is then compared to the DC reference voltage. If a difference exists the integrator sends a control signal to the denominator input to maintain a constant output, thus compensating for input voltage changes.

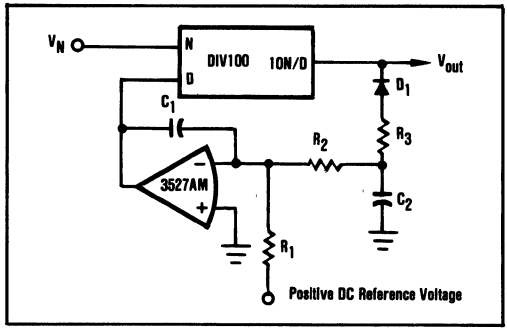


FIGURE 15. Automatic Gain Control Circuit.

VOLTAGE-CONTROLLED FILTER

Figure 16 shows how to use the DIV100 in the feedback loop of an integrator to form a voltage-controlled filter. The transfer function is:

$$\frac{V_{out(S)}}{V_{in(S)}} = \frac{K}{\tau S + 1}$$

where: $K = -R_2/R_1$

$$\tau = \frac{10\ R_2\ C}{V_{CONTROL}}$$

This circuit may be used as a single-pole low-pass active filter whose cutoff frequency is linearly proportional to the circuit's control voltage.

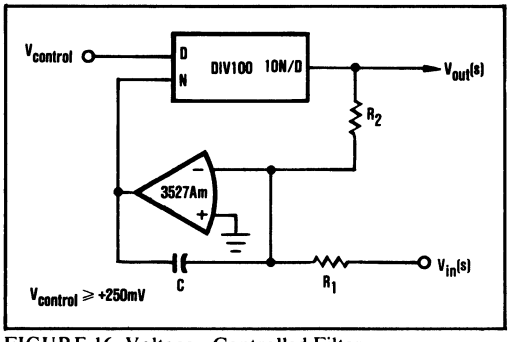


FIGURE 16. Voltage - Controlled Filter.

SQUARE ROOT

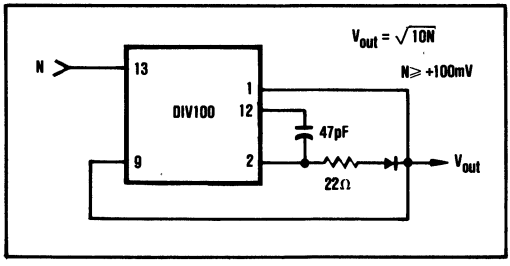


FIGURE 17. Connection Diagram for Square Root Mode.

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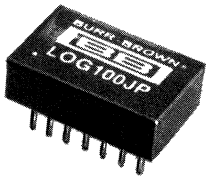


LOG100

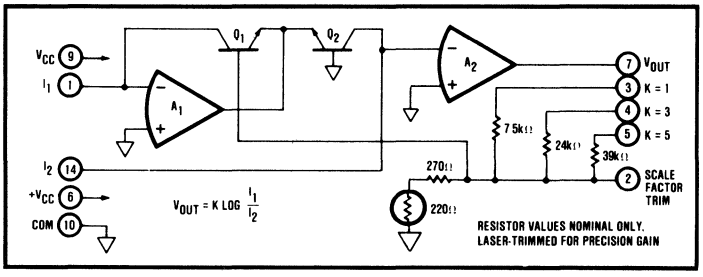
Precision LOGARITHMIC AND LOG RATIO AMPLIFIER

FEATURES

- HIGH ACCURACY
  0.37% FSO max Total Error over 5 decades
- GOOD LINEARITY
  0.1% max Log Conformity over 5 decades
- EASY TO USE
  Pin-selectable Gains
  Internal Laser-trimmed Resistors
- WIDE INPUT DYNAMIC RANGE
  6 Decades, 1nA to 1mA

APPLICATIONS

- LOG, LOG RATIO AND ANTILOG COMPUTATIONS
- ABSORBANCE MEASUREMENTS
- DATA COMPRESSION
- OPTICAL DENSITY MEASUREMENTS
- DATA LINEARIZATION
- CURRENT AND VOLTAGE INPUTS



DESCRIPTION

The LOG100 uses advanced integrated circuit technologies to achieve high accuracy, ease of use, low cost, and small size. It is the logical choice for your logarithmic-type computations. The amplifier has guaranteed maximum error specifications over the full six-decade input range (1nA to 1mA) and for all possible combinations of I_1 and I_2. Total error is guaranteed so that involved error computations are not necessary.

The circuit uses a specially designed compatible thin-film monolithic integrated circuit which contains amplifiers, logging transistors, and low drift thin-film resistors. The resistors are laser-trimmed for maximum precision. FET input transistors are used for the amplifiers whose low bias currents (1pA typical) permit signal currents as low as 1nA while maintaining guaranteed total errors of 0.37% FSO maximum.

Because scaling resistors are self-contained, scale factors of 1V, 3V or 5V per decade are obtained simply by pin selections. No other resistors are required for log ratio applications. The LOG100 will meet its guaranteed accuracy with no user trimming. Provisions are made for simple adjustments of scale factor, offset voltage, and bias current if enhanced performance is desired.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

ELECTRICAL

SPECIFICATIONS

Specifications at T_A = +25°C and $\pm V_{CC}$ = ±15V unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSFER FUNCTION			$V_{OUT} = K \text{ Log } (I_1/I_2)$		
Log Conformity Error[1]	Either I_1 or I_2				
Initial	1nA to 100µA (5 decades)		0.04	0 1	%
	1nA to 1mA (6 decades)		0.15	0.25	%
Over Temperature	1nA to 100µA (5 decades)		0 002		%/°C
	1nA to 1mA (6 decades)		0.001		%/°C
K Range[2]			1, 3, 5		V/decade
Accuracy			0 3		%
Temperature Coefficient			0 03		%/°C
ACCURACY					
Total Error[3]	K = 1,[4] Current Input Operation				
Initial	I_1, I_2 = 1mA			±55	mV
	I_1, I_2 = 100µA			±30	mV
	I_1, I_2 = 10µA			±25	mV
	I_1, I_2 = 1µA			±20	mV
	I_1, I_2 = 100nA			±25	mV
	I_1, I_2 = 10nA			±30	mV
	I_1, I_2 = 1nA			±37	mV
vs Temperature	I_1, I_2 = 1mA		±0 20		mV/°C
	I_1, I_2 = 100µA		±0.37		mV/°C
	I_1, I_2 = 10µA		±0.28		mV/°C
	I_1, I_2 = 1µA		±0.033		mV/°C
	I_1, I_2 = 100nA		±0.28		mV/°C
	I_1, I_2 = 10nA		±0.51		mV/°C
	I_1, I_2 = 1nA		±1.26		mV/°C
vs Supply	I_1, I_2 = 1mA		±4.3		mV/V
	I_1, I_2 = 100µA		±1.5		mV/V
	I_1, I_2 = 10µA		±0.37		mV/V
	I_1, I_2 = 1µA		±0.11		mV/V
	I_1, I_2 = 100nA		±0.61		mV/V
	I_1, I_2 = 10nA		±0.91		mV/V
	I_1, I_2 = 1nA		±2.6		mV/V
INPUT CHARACTERISTICS (of amplifiers A_1 and A_2)					
Offset Voltage					
Initial			±0.7	±5	mV
vs Temperature			±80		µV/°C
Bias Current					
Initial			1	5[5]	pA
vs Temperature			doubles every 10°C		
Voltage Noise	10Hz to 10kHz, RTI		3		µV, rms
Current Noise	10Hz to 10kHz RTI		0 5		pA, rms
AC PERFORMANCE					
3dB Response[6], I_2 = 10µA					
1nA	C_C = 4500pF		0 11		kHz
1µA	C_C = 150pF		38		kHz
10µA	C_C = 150pF		27		kHz
1mA	C_C = 50pF		45		kHz
Step Response[6]					
Increasing	C_C = 150pF				
1µA to 1mA			11		µsec
100nA to 1µA			7		µsec
10nA to 100nA			110		µsec
Decreasing	C_C = 150pF				
1mA to 1µA			45		µsec
1µA to 100nA			20		µsec
100nA to 10nA			550		µsec
OUTPUT CHARACTERISTICS					
Full Scale Output (FSO)		±10			V
Rated Output					
Voltage	I_{OUT} = ±5mA	±10			V
Current	V_{OUT} = ±10V	±5			mA
Current Limit					
Positive			12 5		mA
Negative			15		mA
Impedance			0 05		Ω
POWER SUPPLY REQUIREMENTS					
Rated Voltage			±15		VDC
Operating Range	Derated Performance	±12		±18	VDC
Quiescent Current			±7	±9	mA

ELECTRICAL (CONT'D)

Specifications at T_A = +25°C and $\pm V_{CC}$ = ±15V unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AMBIENT TEMPERATURE RANGE					
Specification	Derated Performance	0		+70	°C
Operating Range		-55		+125	°C
Storage		-55		+125	°C

NOTES
1 Log Conformity Error is the peak deviation from the best-fit straight line of the V_{OUT} vs log I_{IN} curve expressed as a percent of peak-to-peak full scale output
2 May be trimmed to other values See Applications section
3 The worst-case Total Error for any ratio of I_1/I_2 is the largest of the two errors when I_1 and I_2 are considered separately
4 Total Error at other values of K is K times Total Error for K = 1
5 Guaranteed by design Not directly measurable due to amplifier's committed configuration
6. 3dB and transient response are a function of both the compensation capacitor and the level of input current See Performance Curves.

ABSOLUTE MAXIMUM RATINGS

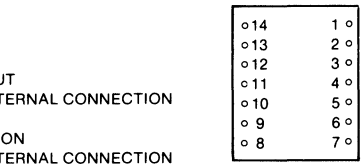
Supply	±18V
Internal Power Dissipation	600mV
Input Current	10mA
Input Voltage Range	±18V
Storage Temperature Range	-40°C to +85°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-circuit Duration	Continuous to ground
Junction Temperature	175°C

SCALE FACTOR PIN CONNECTIONS

K, V/decade	Connections
5	5 to 7
3	4 to 7
1 9	4 and 5 to 7
1	3 to 7
0 85	3 and 5 to 7
0 77	3 and 4 to 7
0 68	3 and 4 and 5 to 7

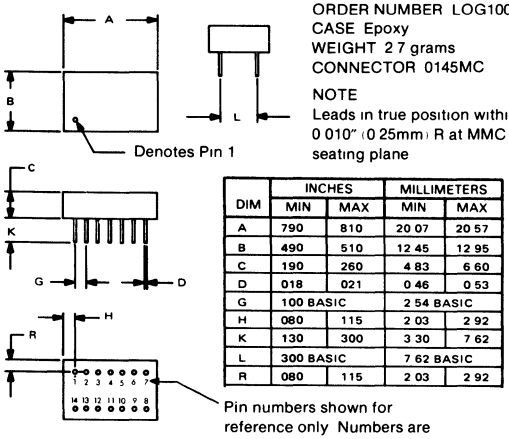
PIN CONFIGURATION

1 I_1 INPUT
2 SCALE FACTOR TRIM
3 K = 1
4 K = 3
5 K = 5
6 +V_{CC}
7 OUTPUT
8 NO INTERNAL CONNECTION
9 -V_{CC}
10 COMMON
11 NO INTERNAL CONNECTION
12 NO INTERNAL CONNECTION
13 NO INTERNAL CONNECTION
14 I_2 INPUT



(Bottom View)

MECHANICAL



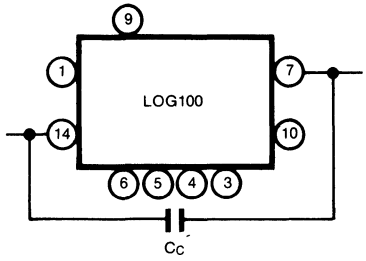
ORDER NUMBER LOG100JP
CASE Epoxy
WEIGHT 2 7 grams
CONNECTOR 0145MC

NOTE
Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	790	810	20 07	20 57
B	490	510	12 45	12 95
C	190	260	4 83	6 60
D	018	021	0 46	0 53
G	100 BASIC		2 54 BASIC	
H	080	115	2 03	2 92
K	130	300	3 30	7 62
L	300 BASIC		7 62 BASIC	
R	080	115	2 03	2 92

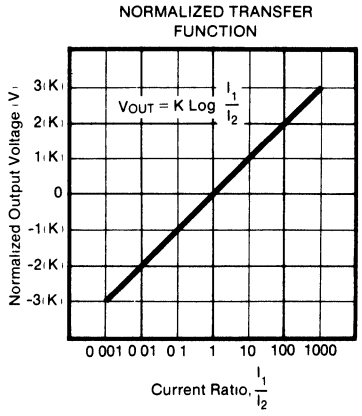
Pin numbers shown for reference only Numbers are not marked on package

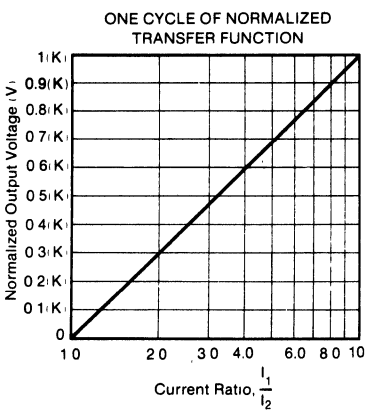
FREQUENCY COMPENSATION

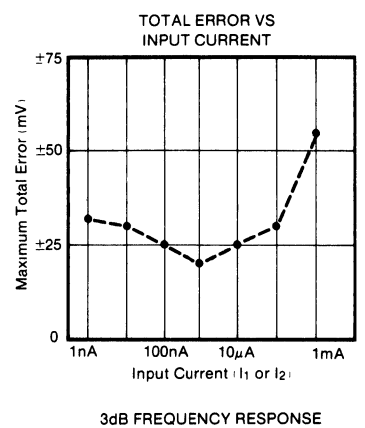


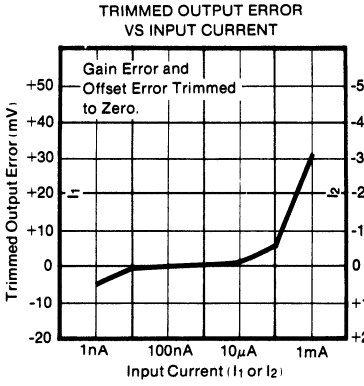
PERFORMANCE CURVES

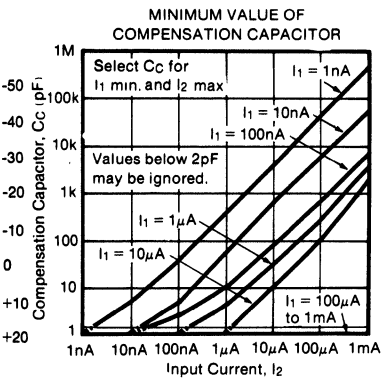
(Typical at T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.

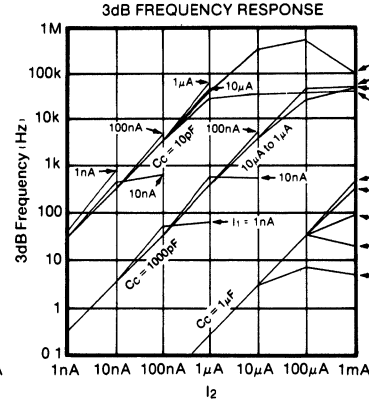












THEORY OF OPERATION

The base-emitter voltage of a bipolar transistor is

$$V_{BE} = V_T \ln \frac{I_c}{I_s} \quad \text{where:} \quad V_T = \frac{KT}{q} \tag{1}$$

K = Boltzman's constant = 1.381 x 10^{-23}

T = Absolute temperature in degrees Kelvin

q = Electron charge = 1.602 x 10^{-19} Coulombs

I_c = Collector current

I_s = Reverse saturation current

From the circuit in Figure 1, we see that

$$V_{OUT}' = V_{BE_1} - V_{BE_2} \tag{2}$$

Substituting (1) into (2) yields

$$V_{OUT}' = V_{T_1} \ln \frac{I_1}{I_{s_1}} - V_{T_2} \ln \frac{I_1}{I_{s_2}} \tag{3}$$

If the transistors are matched and isothermal and $V_{T_1} = V_{T_2}$, then (3) becomes

$$V_{OUT}' = V_T \left[\ln \frac{I_1}{I_s} - \ln \frac{I_2}{I_s} \right] \tag{4}$$

$$V_{OUT}' = V_T \ln \frac{I_1}{I_2} \quad \text{and since} \tag{5}$$

$$\ln X = 2.3 \log_{10} X \tag{6}$$

$$V_{OUT}' = n\, V_T \log \frac{I_1}{I_2} \tag{7}$$

where $n = 2.3$ (8)

also

$$V_{OUT} = V_{OUT}' \frac{R_1 + R_2}{R_1} \tag{9}$$

$$= \frac{R_1 + R_2}{R_1} n\, V_T \log \frac{I_1}{I_2} \tag{10}$$

or

$$V_{OUT} = K \log \frac{I_1}{I_2} \tag{11}$$

It should be noted that the temperature dependance associated with $V_T = KT/q$ is compensated by making R_1 a temperature sensitive resistor with the required positive temperature coefficient.

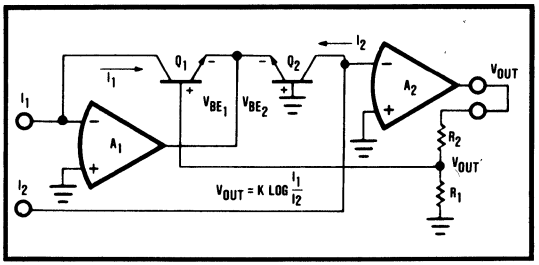


FIGURE 1. Simplified Model of Log Amplifier.

DEFINITION OF TERMS

TRANSFER FUNCTION

The ideal transfer function is $V_{OUT} = K \log \frac{I_1}{I_2}$

where

K = the scale factor with units of volts/decade

I_1 = numerator input current

I_2 = denominator input current.

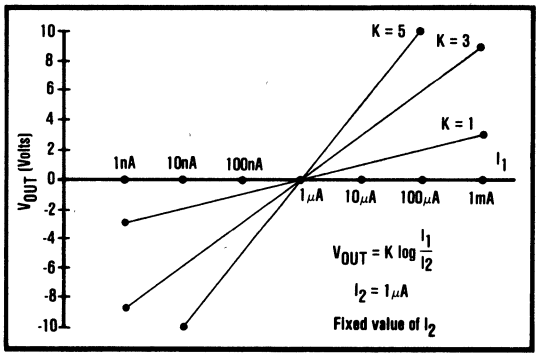


FIGURE 2. Transfer Function with Varying K and I_1.

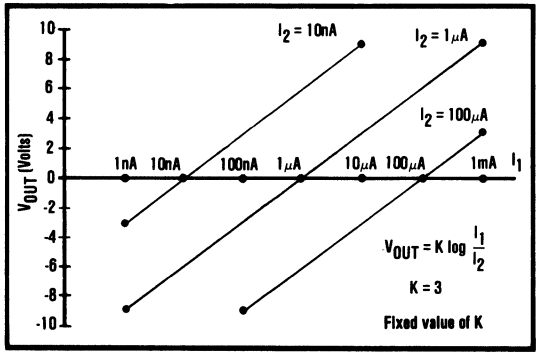


FIGURE 3. Transfer Function with Varying I_2 and I_1.

ACCURACY

Accuracy considerations for a log ratio amplifier are somewhat more complicated than for other amplifiers. The reason is that the transfer function is nonlinear and has two inputs, each of which can vary over a wide dynamic range. The accuracy for any combination of inputs is determined from the total error specification.

TOTAL ERROR

The total error is the deviation (expressed in mV) of the actual output from the ideal output of $V_{OUT} = K \log (I_1/I_2)$. Thus,

$V_{OUT\ (ACTUAL)} = V_{OUT\ (IDEAL)} \pm$ Total Error.

It represents the sum of all the individual components of error normally associated with the log amp when operated in the current input mode. The worst-case error for any given ratio of I_1/I_2 is the largest of the two errors when I_1 and I_2 are considered separately.

Example

I_1 varies over a range of 10nA to 1μA and I_2 varies from 100nA to 10μA. What is the maximum error?

Table I shows the maximum errors for each decade combination of I_1 and I_2.

TABLE I. I_1/I_2 and Maximum Errors.

I_2 (max error)* \ I_1 (max error)*	10nA (30mV)	100nA (25mV)	1μA (20mV)
100nA (25mV)	0.1 (30mV)	1 (25mV)	10 (25mV)
1μA (20mV)	0.01 (30mV)	0.1 (25mV)	1 (20mV)
10μA (25mV)	0.001 (30mV)	0.01 (25mV)	0.1 (25mV)

*Maximum errors are in parenthesis

Since the largest value of I_1/I_2 is 10 and the smallest is 0.001, K is set at 3V per decade so the output will range from +3V to -9V. The maximum total error occurs when I_1 = 10nA and is equal to K x 30mV. This represents a 0.75% of peak-to-peak FSO error $\frac{(3 \times 0.030)}{12} \times 100\% =$ 0.75% where the full scale output is 12V (from +3V to -9V).

ERRORS RTO AND RTI

As with any transfer function, errors generated by the function itself may be Referred-to-Output (RTO) or Referred-to-Input (RTI). In this respect log amps have a unique property:

> Given some error voltage at the log amp's output, that error corresponds to a constant percent of the input regardless of the actual input level.

Refer to: Yu Jen Wong and William E. Ott, "Function Circuits: Design & Applications", McGraw-Hill Book, 1976.

LOG CONFORMITY

Log conformity corresponds to linearity when V_{OUT} is plotted versus I_1/I_2 on a semilog scale. In many applications log conformity is the most important specification. This is true because bias current errors are negligible (1pA compared to input currents of 1nA and above) and the scale factor and offset errors may be trimmed to zero or removed by system calibration. This leaves log conformity as the major source of error.

Log conformity error is defined as the peak deviation from the best-fit straight line of the V_{OUT} versus log (I_1/I_2) curve. This is expressed as a percent of peak-to-peak full scale output. Thus, the nonlinearity error expressed in volts over m decades is

$$V_{OUT\ (NONLIN.)} = K\ 2Nm \text{ volts} \quad (12)$$

where N is the log conformity error, in percent.

INDIVIDUAL ERROR COMPONENTS

The ideal transfer function with current input is

$$V_{OUT} = K \log \frac{I_1}{I_2} \quad (13)$$

The actual transfer function with the major components of error is

$$V_{OUT} = K(1 \pm \Delta K) \log \frac{I_1 - I_{B_1}}{I_2 - I_{B_2}} \pm K\ 2Nm \pm V_{OS\ OUT} \quad (14)$$

The individual component of error is

ΔK = scale factor error (0.3%, typ)

I_{B_1} = bias current of A_1 (1pA, typ)

I_{B_2} = bias current of A_2 (1pA, typ)

N = log conformity error (0.05%, 0.1%, typ)

$V_{OS\ OUT}$ = output offset voltage (1mV, typ)

m = no. of decades over which N is specified: 0.05% for m = 5, 0.1% for m = 6

Example: what is the error with K = 3 when $I_1 = 1\mu A$ and $I_2 = 100nA$

$$V_{OUT} = 3(1 \pm 0.003) \log \frac{10^{-6} - 10^{-12}}{10^{-7} - 10^{-12}} \pm 3(2)(0.0005)\ 5 \pm 1mV \quad (15)$$

$$\approx 3.009 \log \frac{10^{-6}}{10^{-7}} + 0.015 + 0.001 \quad (16)$$

$$= 3.009\ (1) + 0.015 + 0.001 \quad (17)$$

$$= 3.025 \text{ volts} \quad (18)$$

Since the ideal output is 3.000V the error as a percent of reading is

$$\%\ \text{error} = \frac{0.025}{3} \times 100\% = 0.83\% \quad (19)$$

For the case of voltage inputs, the actual transfer function is

$$V_{OUT} = K(1 \pm \Delta K) \log \frac{\frac{V_1}{R_1} - I_{B_1} \pm \frac{E_{OS_1}}{R_1}}{\frac{V_2}{R_2} - I_{B_2} \pm \frac{E_{OS_2}}{R_2}} \pm K\ 2Nm \pm V_{OS\ OUT} \quad (20)$$

FREQUENCY RESPONSE

The 3dB frequency response of the LOG100 is a function of the magnitude of the input current levels and of the value of the frequency compensation capacitor. See Performance Curves for details.

The frequency response curves are shown for constant DC I_1 and I_2 with a small signal AC current on one of them.

The transient response of the LOG100 is different for increasing and decreasing signals. This is due to the fact that a log amp is a nonlinear gain element and has different gains at different levels of input signals. Frequency response decreases as the gain increases.

GENERAL INFORMATION

INPUT CURRENT RANGE

The stated input range of 1nA to 1mA is the range for specified accuracy. Smaller or larger input currents may be applied with decreased accuracy. Currents larger than 1mA result in increased nonlinearity. The 10mA absolute maximum is a conservative value to limit the power dissipation in the output stage of A_1 and the logging transistor. Currents below 1nA will result in increased errors due to the input bias currents of A_1 and A_2 (1pA typical). These errors may be nulled. See Optional Adjustments section.

FREQUENCY COMPENSATION

Frequency compensation for the LOG100 is obtained by connecting a capacitor between pins 7 and 14. The size of the capacitor is a function of the input currents as shown in the Performance Curves. For any given application the smallest value of the capacitor which may be used is determined by the maximum value at I_2 and the minimum value of I_1. Larger values of C_C will make the LOG100 more stable, but will reduce the frequency response.

SETTING THE REFERENCE CURRENT

When the LOG100 is used as a straight log amplifier I_2 is constant and becomes the reference current in the expression

$$V_{OUT} = K \log \frac{I_1}{I_{REF}}. \quad (21)$$

I_{REF} can be derived from an external current source (such as shown in Figure 4) or it may be derived from a voltage source with one or more resistors.

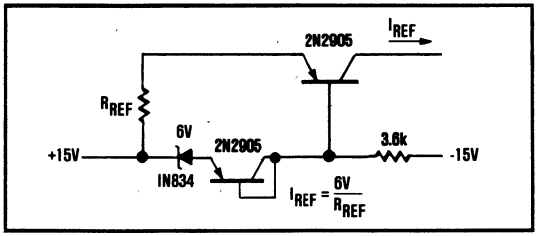


FIGURE 4. Temperature-Compensated Current Reference.

When a single resistor is used the value may be quite large when I_{REF} is small. If I_{REF} is 10nA and +15V is used

$$R_{IT} = \frac{15V}{10\,nA} = 1500M\Omega.$$

A voltage divider may be used to reduce the value of the resistor. When this is done one must be aware of possible errors caused by the amplifier's input offset voltage. This is shown in Figure 5.

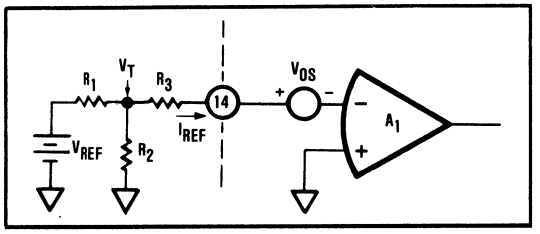


FIGURE 5. "T" Network for Reference Current.

In this case the voltage at pin 14 is not exactly zero, but is equal to the value of the input offset voltage of A_1 which ranges from zero to ±5mV. V_T must be kept much larger than 5mV in order to make this effect negligible. This concept also applies to pin 1.

OPTIONAL ADJUSTMENTS

The LOG100 will meet its specified accuracy with no user adjustments. If improved performance is desired the following optional adjustments may be made.

INPUT BIAS CURRENT

The circuit in Figure 6 may be used to compensate for the input bias currents of A_1 and A_2. Since the amplifiers have FET inputs with the characteristic bias current doubling every 10°C this nulling technique is practical only where the temperature is fairly stable.

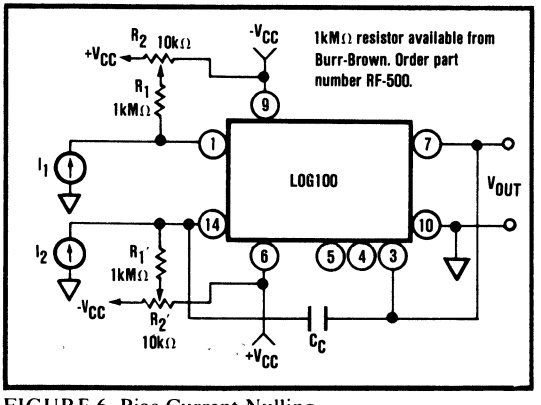


FIGURE 6. Bias Current Nulling.

OUTPUT OFFSET

The output offset may be nulled with the circuit in Figure 7. I_1 and I_2 are set equal at some convenient value in the range of 100nA to 100μA. R_1 is then adjusted for zero output voltage.

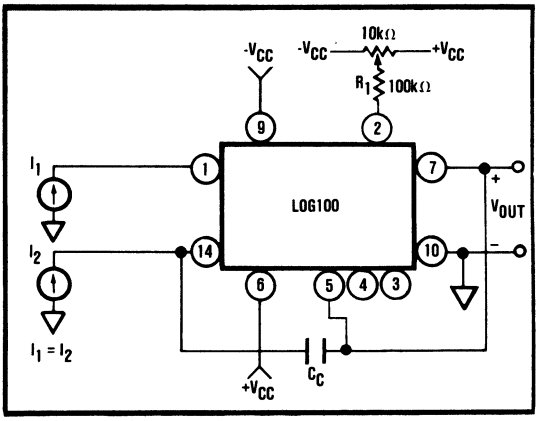


FIGURE 7. Output Offset Nulling.

ADJUSTMENTS OF SCALE FACTOR K

The value of K may be changed by increasing or decreasing the voltage divider resistor normally connected to the output, pin 7. To increase K put resistance in series between pin 7 and the appropriate scaling resistor pin (3, 4 or 5). To decrease K place a parallel resistor between pin 2 and either pin 3, 4 or 5.

APPLICATION INFORMATION

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the $+V_{CC}$ and $-V_{CC}$ pins to the power supply common. The connection of these capacitors should be as close to the LOG100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads of up to 100pF, typically. Higher capacitive loads can be driven if a 22Ω carbon resistor is connected in series with the LOG100's output. This resistor will, of course, form a voltage divider with other resistive loads.

CIRCUIT PROTECTION

The LOG100 can be protected against accidental power supply reversal by putting a diode (1N4001 type) in series with each power supply line as shown in Figure 8. This precaution is necessary only in power systems that momentarily reverse polarity during turn-on or turn-off. If this protection circuit is used, the accuracy of the LOG100 will be degraded slightly by the voltage drops across the diodes as determined by the power supply sensitivity specification.

The LOG100 uses small geometry FET transistors to achieve the low input bias currents. Normal FET handling techniques should be used to avoid damage caused by low energy electrostatic discharge (ESD).

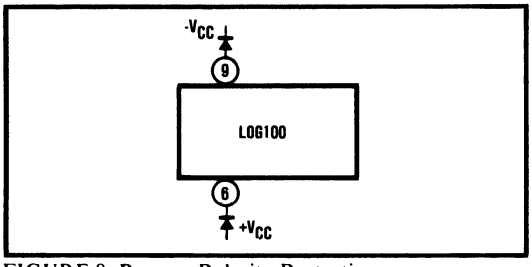


FIGURE 8. Reverse Polarity Protection.

LOG RATIO

One of the more common uses of log ratio amplifiers is to measure absorbance. A typical application is shown in Figure 9.

Absorbance of the sample is: $A = \log \frac{\lambda_1'}{\lambda_1}$ (22)

If $\lambda_2 = \lambda_1$ and D_1 and D_2 are matched $A \propto K \log \frac{I_1}{I_2}$. (23)

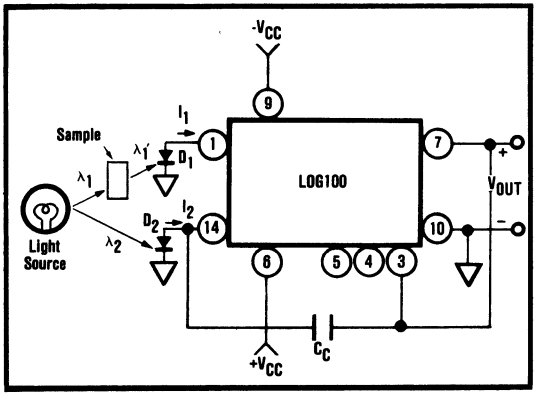


FIGURE 9. Absorbance Measurement

DATA COMPRESSION

In many applications the compressive effects of the logarithmic transfer function is useful. For example, a LOG100 preceding an 8-bit analog-to-digital converter can replace a more expensive 20-bit converter.

SELECTING OPTIMUM VALUES OF I_2 AND K

In straight log applications (as opposed to log ratio) both K and I_2 are selected by the designer. In order to minimize errors due to output offset and noise it is normally best to scale the log amp to use as much of the ±10V output range as possible. Thus, with the range of I_1 from $I_{1\,MIN}$ to $I_{1\,MAX}$;

For $I_{1\,MAX}$ $+10V = K \log I_{1\,MAX}/I_2$ (24)

For $I_{1\,MIN}$ $-10V = K \log I_{1\,MIN}/I_2$ (25)

Addition of these two equations and solving for I_2 shows that its optimum value, $I_{2\,OPT}$, is the geometric mean of $I_{1\,MAX}$ and $I_{1\,MIN}$.

$$I_{2\,OPT} = \sqrt{I_{1\,MAX} \times I_{1\,MIN}} \quad (26)$$

$$K_{OPT} = \frac{10}{\log \frac{I_{1\,MAX}}{I_{2\,OPT}}} \quad (27)$$

Since K is selectable in discrete steps, use the largest value of K available which does not exceed K_{OPT}.

NEGATIVE INPUT CURRENTS

The LOG100 will function only with positive input currents (conventional current flow into pins 1 and 14). Some current sources (such as photomultiplier tubes) provide negative input currents. In such situations the circuit in Figure 10 may be used.*

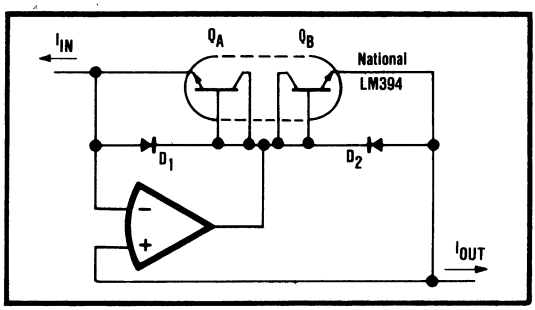


FIGURE 10. Current Inverter.

VOLTAGE INPUTS

The LOG100 gives the best performance with current inputs. Voltage inputs may be handled directly with series resistors, but the dynamic input range is limited to approximately three decades of input voltage by voltage noise and offsets. The transfer function of equation (20) applies to this configuration.

ANTILOG CONFIGURATION (an implicit technique)

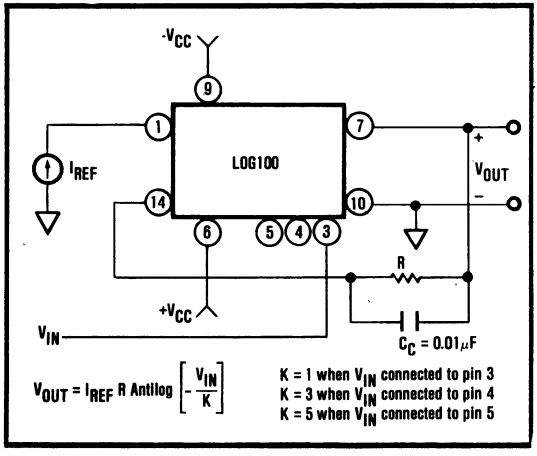
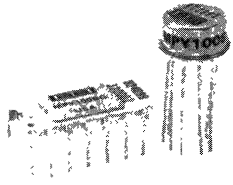


FIGURE 11. Connections for Antilog Function.

*More detailed information may be found in "Properly Designed Log Amplifiers Process Bipolar Input Signals" by Larry McDonald, EDN, 5 Oct 80, pp 99-102

BURR-BROWN®



MPY100

MILITARY & DIE VERSIONS AVAILABLE

MULTIPLIER-DIVIDER

FEATURES

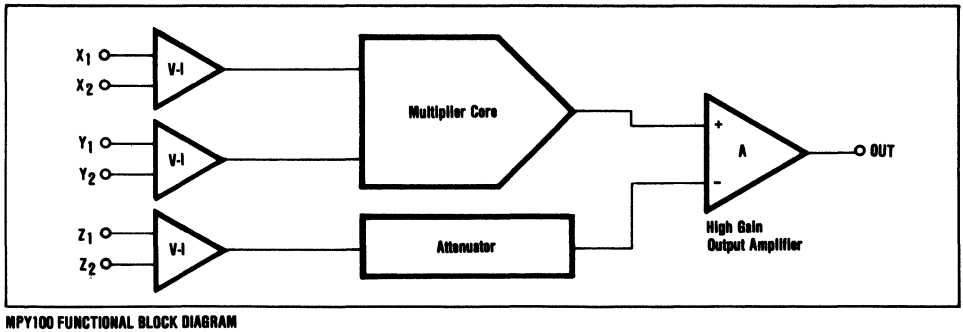
- LOW COST
- DIFFERENTIAL INPUT
- ACCURACY 100% TESTED AND GUARANTEED
- NO EXTERNAL TRIMMING REQUIRED
- LOW NOISE
  90μV, rms, 10Hz to 10kHz
- HIGHLY RELIABLE ONE-CHIP DESIGN
- DIP OR TO-100 TYPE PACKAGE
- WIDE TEMPERATURE OPERATION

APPLICATIONS

- MULTIPLICATION
- DIVISION
- SQUARING
- SQUARE ROOT
- LINEARIZATION
- POWER COMPUTATION
- ANALOG SIGNAL PROCESSING
- ALGEBRAIC COMPUTATION
- TRUE RMS-TO-DC CONVERSION

DESCRIPTION

The MPY100 multiplier-divider is a low cost precision device designed for general purpose application. In addition to four-quadrant multiplication, it also performs analog square root and division without the bother of external amplifiers or potentiometers. Laser-trimmed one-chip design offers the most in highly reliable operation with guaranteed accuracies. Because of the internal reference and pretrimmed accuracies the MPY100 does not have the restrictions of other low cost multipliers. It is available in both TO-100 and DIP ceramic packages.



MPY100 FUNCTIONAL BLOCK DIAGRAM

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_S$ = 15VDC unless otherwise noted.

MODEL		MPY100A			MPY100B/C			MPY100S			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
MULTIPLIER PERFORMANCE											
Transfer Function			$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$			*/*			*		
Total Error	-10V ≤ X, Y ≤ 10V										
Initial	T_A = +25°C			±2.0			±1.0/0.5			±0.5	% FSR
vs. Temperature	-25°C ≤ T_A ≤ +85°C		±0.017	±0.05		±0.008/0.008	±0.02/0.02				% FSR/°C
vs. Temperature	-55°C ≤ T_A ≤ +125°C								±0.025	±0.05	% FSR/°C
vs. Supply[1]			±0.05			*/*			*		% FSR/%
Individual Errors											
Output Offset											
Initial	T_A = +25°C		±50	±100		±10/7	±50/25		±7	±50mV	mV
vs. Temperature	-25°C ≤ T_A ≤ +85°C		±0.7	±2.0		±0.7/0.3	±2.0/±0.7				mV/°C
vs. Temperature	-55°C ≤ T_A ≤ +125°C								±0.3	±0.7	mV/°C
vs. Supply[1]			±0.25			*/*			*		mV/%
Scale Factor Error											
Initial	T_A = +25°C		±0.12			*/*			*		% FSR
vs. Temperature	-25°C ≤ T_A ≤ +85°C		±0,008			*/*					% FSR/°C
vs. Temperature	-55°C ≤ T_A ≤ +125°C								±0.008		% FSR/°C
vs. Supply[1]			±0.05			*/*			*		% FSR/%
Nonlinearity											
X Input	X = 20V, p-p; Y = ±10VDC		±0.08			*/*			*		% FSR
Y Input	Y = 20V, p-p; X = ±10VDC		±0.08			*/*			*		% FSR
Feedthrough	f = 50Hz										
X Input	X = 20V, p-p; Y = 0		100			30/30			30		mV, p-p
Y Input	Y = 20V, p-p; X = 0		6			*/*			*		mV, p-p
vs. Temperature	-25°C ≤ T_A ≤ +85°C		0.1			*/*					mV, p-p/°C
vs. Temperature	-55°C ≤ T_A ≤ +125°C								0.1		mV, p-p/°C
vs. Supply[1]			0.15			*/*			*		mV, p-p/%
DIVIDER PERFORMANCE											
Transfer Function	$X_1 > X_2$		$\frac{10\,(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$			*/*			*		
Total Error (with	X = 10V										
external adjustments)	-10V ≤ Z ≤+10V		±1.5			±0.75/0.35			±0.35		% FSR
	X = 1V										
	-1V ≤ Z ≤ +1V		±4.0			±2.0/1.0			±1.0		% FSR
	+0.2V ≤ X ≤ +10V										
	-10V ≤ Z ≤ +10V		±5.0			±2.5/1.0			±1.0		% FSR
SQUARER PERFORMANCE											
Transfer Function			$\frac{(X_1 - X_2)^2}{10} + Z_2$			*/*			*		
Total Error	-10V ≤ X ≤ +10V		±1.2			±0.6/0.3			±0.3		% FSR
SQUARE-ROOTER PERFORMANCE											
Transfer Function	$Z_1 < Z_2$		$+\sqrt{10(Z_2 - Z_1)} + X_2$			*/*			*		
Total Error	1V ≤ Z ≤ 10V		±2			±1/0.5			±0.5		% FSR
AC PERFORMANCE											
Small-Signal Bandwidth			550			*/*			*		kHz
1% Amplitude Error	Small-Signal		70			*/*			*		kHz
1% (0.57°) Vector Error	Small-Signal		5			*/*			*		kHz
Full Power Bandwidth	$\|V_o\|$ = 10V, R_L = 2kΩ		320			*/*			*		kHz
Slew Rate	$\|V_o\|$ = 10V, R_L = 2kΩ		20			*/*			*		V/μsec
Settling Time	ϵ = ±1%, ΔV_o = 20V		2			*/*			*		μsec
Overload Recovery	50% Output Overload		0.2			*/*			*		μsec
INPUT CHARACTERISTICS											
Input Voltage Range											
Rated Operation		±10			*/*			*			V
Absolute Maximum				±V_{CC}			*/*			*	V
Input Resistance	X, Y, Z[2]		10			*/*			*		MΩ
Input Bias Current	X, Y, Z		1.4			*/*			*		μA
OUTPUT CHARACTERISTICS											
Rated Output											
Voltage	I_o = ±5mA	±10			*/*			*			V
Current	V_o = ±10V	±5			*/*			*			mA
Output Resistance	f = DC		1.5			*/*			*		Ω
OUTPUT NOISE VOLTAGE	X = Y = 0										
f_o = 1Hz			6.2			*/*			*		μV/√Hz
f_o = 1kHz			0.6			*/*			*		μV/√Hz
1/f Corner Frequency			110			*/*			*		Hz
f_B = 5Hz to 10kHz			60			*/*			*		μV, rms
f_B = 5Hz to 5MHz			1.3			*/*			*		mV, rms
POWER SUPPLY REQUIREMENTS											
Rated Voltage			±15			*/*			*		VDC
Operating Range	Derated Performance	±8.5		±20	*/*		*/*	*		*	VDC
Quiescent Current			±5.5			*/*			*/*		mA

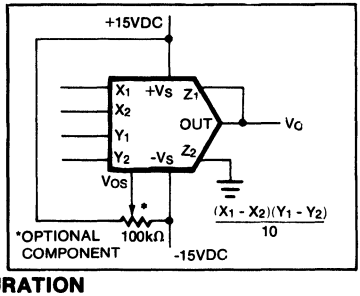
ELECTRICAL SPECIFICATIONS (CONT)

MODEL		MPY100A			MPY100B/C			MPY100S			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TEMPERATURE RANGE (Ambient)											
Specification	Derated Performance	-25		+85	*/*		*/*	-55		+125	°C
Operating Range		-55		+125	*/*		*/*	*		*	°C
Storage		-65		+150	*/*		*/*	*		*	°C

NOTES:
1. Includes effects of recommended null pots
2. Z_2 input resistance is 10MΩ, typical, with V_{OS} pin open. If V_{OS} pin is grounded or used for optional offset adjustment, the Z_2 input resistance may be as low as 25kΩ

*Same as MPY100A specification.
/ means B/C grades same as MPY100A specification

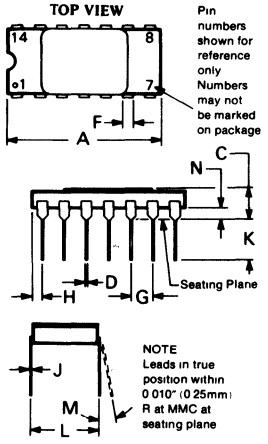
CONNECTION DIAGRAM



MECHANICAL

CERAMIC DUAL-IN-LINE PACKAGE

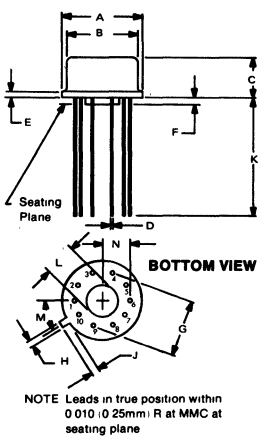
Order Number:
MPY100AG, MPY100BG
MPY100CG, MPY100SG



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	670	710	17.02	18.03
C	065	170	1.65	4.32
D	015	021	0.38	0.53
F	045	060	1.14	1.52
G	100 BASIC		2.54 BASIC	
H	025	070	0.64	1.78
J	008	012	0.20	0.30
K	120	240	3.05	6.10
L	300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	009	060	0.23	1.52

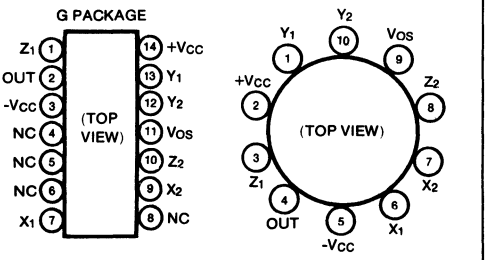
METAL CAN PACKAGE

Order Number:
MPY100AM, MPY100BM
MPY100CM, MPY100SM



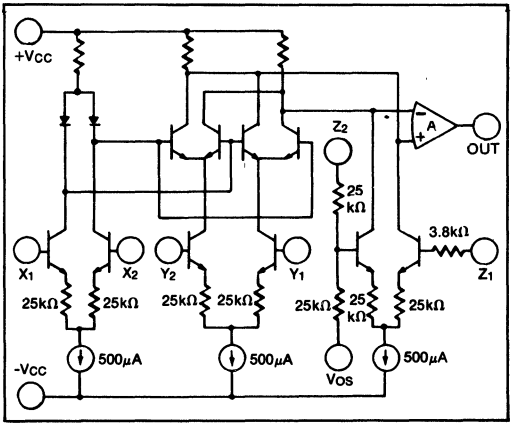
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	370	8.51	9.40
B	.305	335	7.75	8.51
C	165	185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.70	--
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	120	2.79	3.05

PIN CONFIGURATION

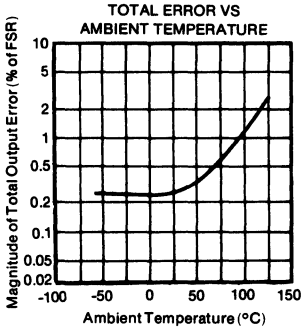


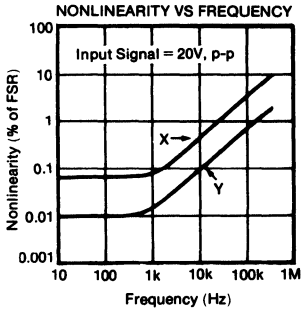
NOTES:
1. V_{OS} adjustment optional not normally recommended. V_{OS} pin may be left open or grounded.
2. All unused input pins should be grounded.

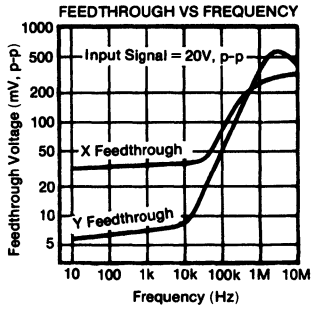
SIMPLIFIED SCHEMATIC

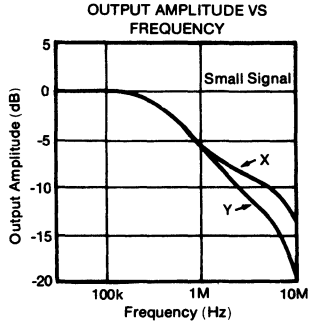


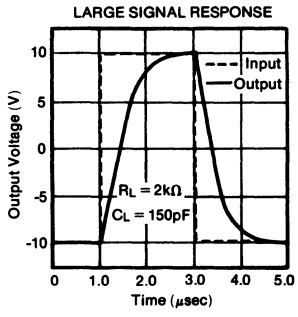
TYPICAL PERFORMANCE CURVES

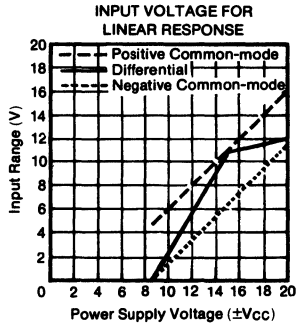


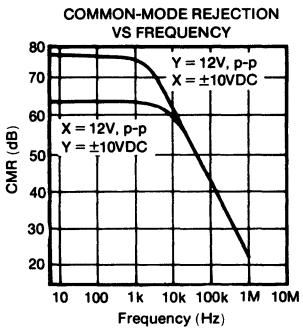


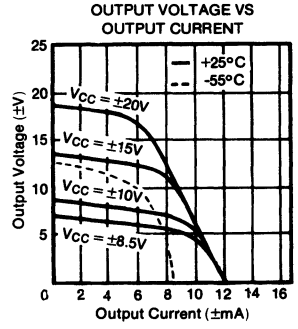


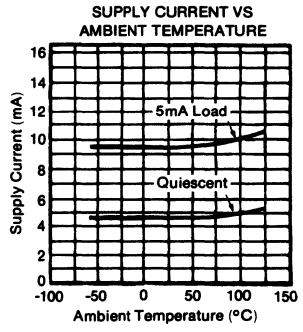












ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation(1)	500mW
Differential Input Voltage(2)	±40VDC
Input Voltage Range(2)	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-circuit Duration(3)	Continuous
Junction Temperature	+150°C

NOTES:
1. Package must be derated on θ_{JC} = 15°C/W and θ_{JA} = 165°C/W for the metal package and θ_{JC} = 35°C/W and θ_{JA} = 220°C/W for the ceramic package.
2. For supply voltages less than ±20VDC the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground only. Rating applies to +85°C ambient for the metal package and +65°C for the ceramic package.

APPLICATIONS INFORMATION

THEORY OF OPERATION

The MPY100 is a variable transconductance multiplier consisting of three differential voltage-to-current converters, a multiplier core and an output differential amplifier as illustrated in Figure 1.

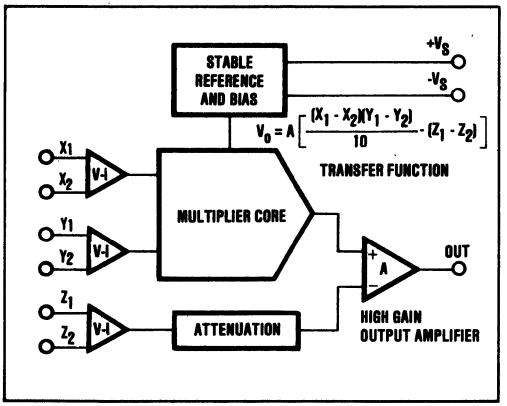


FIGURE 1. MPY100 Functional Block Diagram.

The basic principle of the transconductance multiplier can be demonstrated by the differential stage in Figure 2.

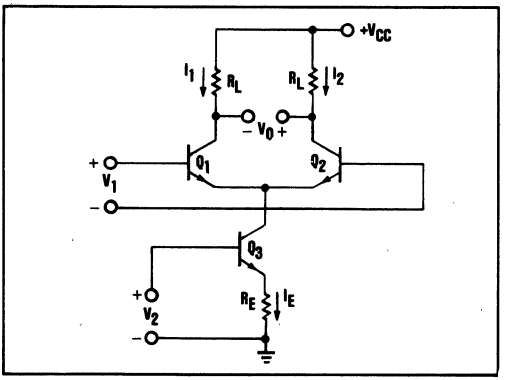


FIGURE 2. Basic Differential Stage as a Transconductance Multiplier.

For small values of the input voltage V_1 that are much smaller than V_T, the transistor's thermal voltage, the differential output voltage V_o is

$$V_o = g_m R_L V_1.$$

The transconductance g_m of the stage is given by:

$$g_m = I_E / V_T,$$

and is modulated by the voltage V_2 to give

$$g_m \approx V_2 / V_T R_E.$$

Substituting this into the original equation yields the overall transfer function

$$V_o = g_m R_L V_1 = V_1 V_2 (R_L / V_T R_E)$$

which shows the output voltage to be the product of the two input voltages, V_1 and V_2.

Variations in I_E due to V_2 cause a large common-mode voltage swing in the circuit. The errors associated with this common-mode voltage can be eliminated by using two differential stages in parallel and cross-coupling their outputs as shown in Figure 3.

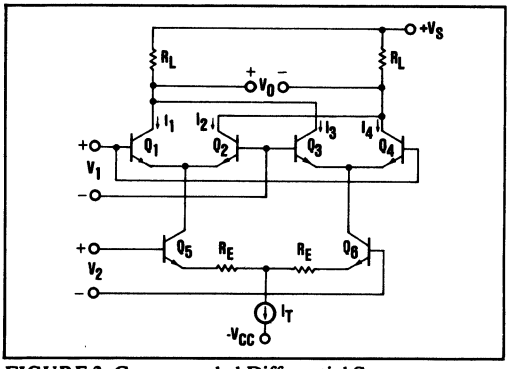


FIGURE 3. Cross-coupled Differential Stages as a Variable-transconductance Multiplier.

An analysis of the circuit in Figure 3 shows it to have the same overall transfer function as before:

$$V_o = V_1 V_2 (R_L / V_T R_E).$$

For input voltages larger than V_T the voltage-to-current transfer characteristics of the differential pair Q_1, Q_2 or Q_3 and Q_4 are no longer linear. Instead, their collector currents are related to the applied voltage V_1 as

$$\frac{I_1}{I_2} = \frac{I_3}{I_4} = e^{\frac{V_1}{V_t}}$$

The resultant nonlinearity can be overcome by developing V_1 logarithmically to exactly cancel the exponential relationship just derived. This is done by diodes D_1 and D_2 in Figure 4.

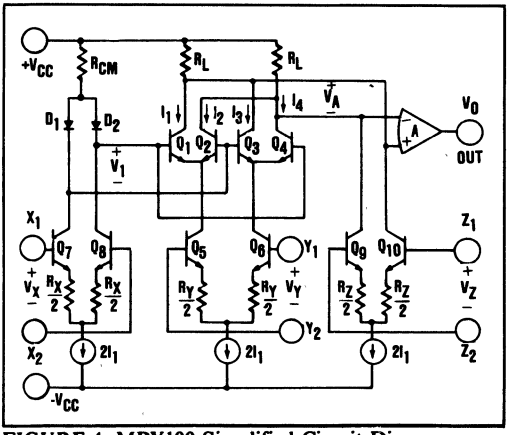


FIGURE 4. MPY100 Simplified Circuit Diagram.

The emitter degeneration resistors R_X and R_Y, in Figure 4, provide a linear conversion of the input voltages to differential current I_X and I_Y, where

$$I_X = V_X/R_X \text{ and } I_Y = V_Y/R_Y.$$

Analysis of Figure 4 shows the voltage V_A to be

$$V_A = (2R_L/I_1)(I_XI_Y).$$

Since I_X and I_Y are linearly related to the input voltages V_X and V_Y, V_A may also be written

$$V_A = KV_XV_Y$$

where K is a scale factor. In the MPY100, K is chosen to be 0.1.

The addition of the Z input alters the voltage V_A to

$$V_A = KV_XV_Y - V_Z.$$

Therefore, the output of the MPY100 is

$$V_o = A[KV_XV_Y - V_Z]$$

where A is the open-loop gain of the output amplifier. Writing this last equation in terms of the separate inputs to the MPY100 gives

$$V_o = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} - (Z_1 - Z_2)\right],$$

the transfer function of the MPY100.

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the $+V_{CC}$ and $-V_{CC}$ pins of the MPY100 to the power supply common. The connection of these capacitors should be as close to the MPY100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads to 1000pF in all modes, except the square root mode for which 50pF is a safe upper limit. Higher capacitive loads can be driven if a 100Ω resistor is connected in series with the MPY100's output.

DEFINITIONS

TOTAL ERROR (Accuracy)

Total error is the actual departure of the multiplier output voltage from the ideal product of its input voltages. It includes the sum of the effects of input and output DC offsets, gain error and nonlinearity.

OUTPUT OFFSET

Output offset is the output voltage when both inputs V_X and V_Y are zero volts.

SCALE FACTOR ERROR

Scale factor error is the difference between the actual scale factor and the ideal scale factor.

NONLINEARITY

Nonlinearity is the maximum deviation from a best straightline (curve fitting on input-output graph) expressed as a percent of peak-to-peak full scale output.

FEEDTHROUGH

Feedthrough is the signal at the output for any value of V_X or V_Y within the rated range, when the other input is zero.

SMALL SIGNAL BANDWIDTH

Small signal bandwidth is the frequency at which the output is down 3dB from its low-frequency value for a nominal output amplitude of 10% of full scale.

1% AMPLITUDE ERROR

The 1% amplitude error is the frequency the output amplitude is in error by 1%, measured with an output amplitude of 10% of full scale.

1% VECTOR ERROR

The 1% vector error is the frequency at which a phase error of 0.01 radians (0.57°) occurs. This is the most sensitive measure of dynamic error of a multiplier.

TYPICAL APPLICATIONS

MULTIPLICATION

Figure 5 shows the basic connection for four-quadrant multiplication.

The MPY100 meets all of its specifications without trimming. Accuracy can, however be improved over a limited range by nulling the output offset voltage using the 100kΩ optional balance potentiometer shown in Figure 5.

AC feedthrough may be reduced to a minimum by applying an external voltage to the X or Y input as shown in Figure 6.

Z_2, the optional summing input, may be used to sum a voltage into the output of the MPY100. If not used, this

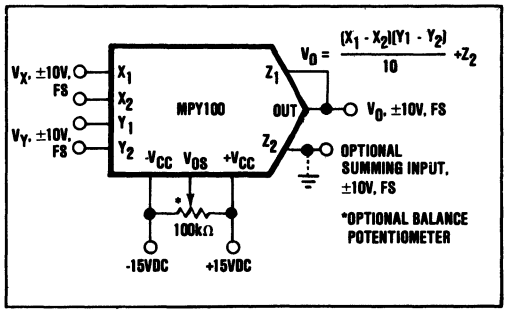


FIGURE 5. Multiplier Connection.

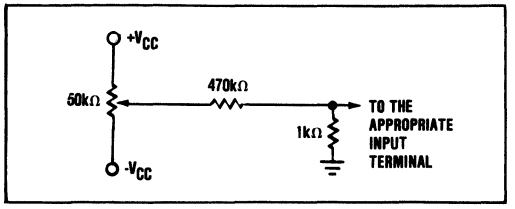


FIGURE 6. Optional Trimming Configuration.

terminal, as well as the X and Y input terminals, should be grounded. All inputs should be referenced to power supply common.

Figure 7 shows how to achieve a scale factor larger than the nominal 1/10. In this case, the scale factor is unity which makes the transfer function

$$V_o = KV_XV_Y = K(X_1 - X_2)(Y_1 - Y_2).$$

$$K = \frac{\left[1 + (R_1/R_2)\right]}{10}$$

$$0.1 \leq K \leq 1$$

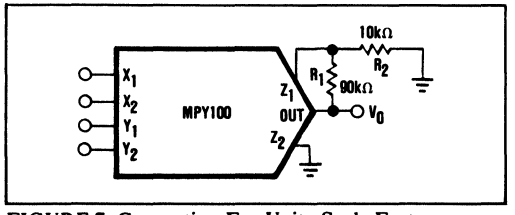


FIGURE 7. Connection For Unity Scale Factor.

This circuit has the disadvantage of increasing the output offset voltage by a factor of 10 which may require the use of the optional balance control as in Figure 1 for some applications. In addition, this connection reduces the small signal bandwidth to about 50kHz.

DIVISION

Figure 8 shows the basic connection for two-quadrant division. This configuration is a multiplier-inverted analog divider, i.e., a multiplier connected in the feedback loop of an operational amplifier. In the case of the MPY100 this operational amplifier is the output amplifier shown in Figure 1.

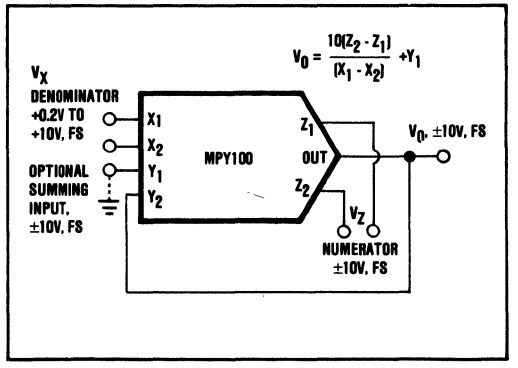


FIGURE 8. Divider Connection.

The divider error with a multiplier-inverted analog divider is approximately

$$\epsilon_{divider} = 10\,\epsilon_{multiplier}/(X_1 - X_2)$$

It is obvious from this error equation that divider error becomes excessively large for small values of $X_1 - X_2$. A 10-to-1 denominator range is usually the practical limit. If more accurate division is required over a wide range of denominator voltages, an externally generated voltage may be applied to the unused X-input (see Optional Trim Configuration). To trim, apply a ramp of +100mV to +1V at 100Hz to both X_1 and Z_1 if X_2 is used for offset adjustment, otherwise reverse the signal polarity, and adjust the trim voltage to minimize the variation in the output. An alternative to this procedure would be to use the Burr-Brown DIV100, a precision log-antilog divider.

SQUARING

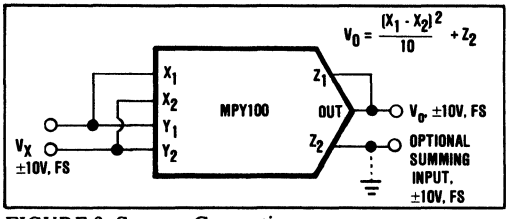


FIGURE 9. Squarer Connection.

SQUARE ROOT

Figure 10 shows the connection for taking the square root of the voltage V_Z. The diode prevents a latching condition which could occur if the input momentarily changed polarity. This latching condition is not a design flaw in the MPY100, but occurs when a multiplier is connected in the feedback loop of an operational amplifier to perform square root functions.

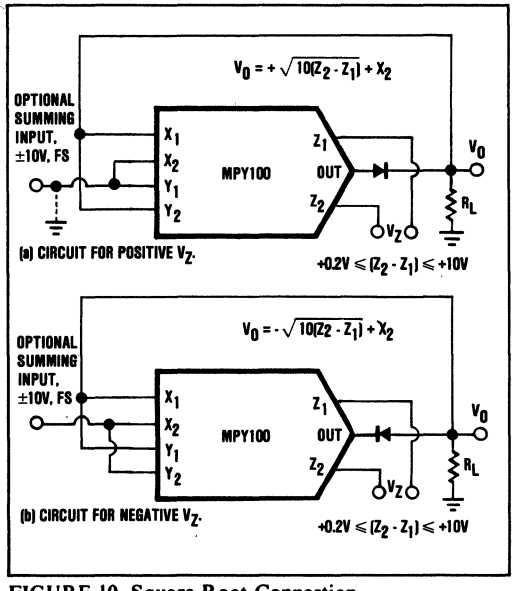


FIGURE 10. Square Root Connection.

The load resistance R_L must be in the range of $10k\Omega \leq R_L \leq 1M\Omega$. This resistance must be in the circuit as it provides the current necessary to operate the diode.

BRIDGE LINEARIZATION

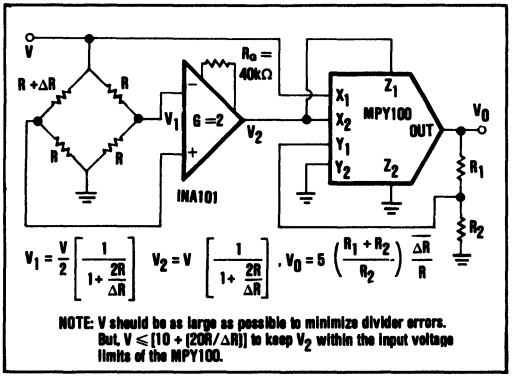


FIGURE 11. Bridge Linearization.

The use of the MPY100 to linearize the output from a bridge circuit makes the output V_o independent of the bridge supply voltage.

TRUE RMS-TO-DC CONVERSION

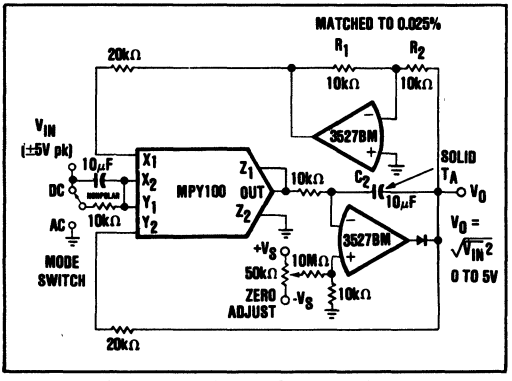


FIGURE 12. True RMS-to-DC Conversion.

The rms-to-DC conversion circuit of Figure 12 gives greater accuracy and bandwidth but with less dynamic range than most rms-to-DC converters.

PERCENTAGE COMPUTATION

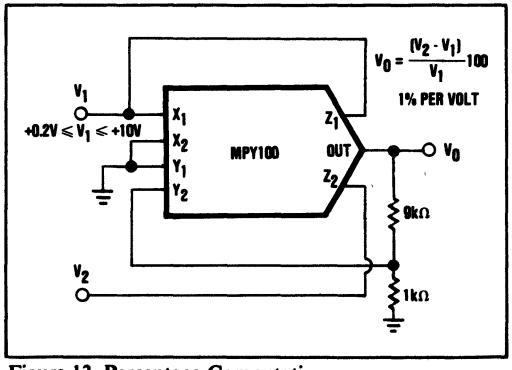


Figure 13. Percentage Computation.

The circuit of Figure 13 has a sensitivity of 1V/% and is capable of measuring 10% deviations. Wider deviation can be measured by decreasing the ratio of R_2/R_1.

SINE FUNCTION GENERATOR

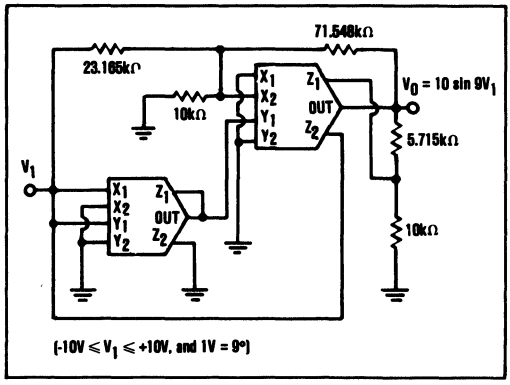


FIGURE 14. Sine Function Generator.

The circuit in Figure 14 uses implicit feedback to implement the following sine function approximation:

$$V_o = (1.5715V_1 - 0.004317V_1^3)/(1 + 0.001398V_1^2)$$
$$= 10 \sin (9V_1).$$

SINGLE-PHASE POWER MEASUREMENT

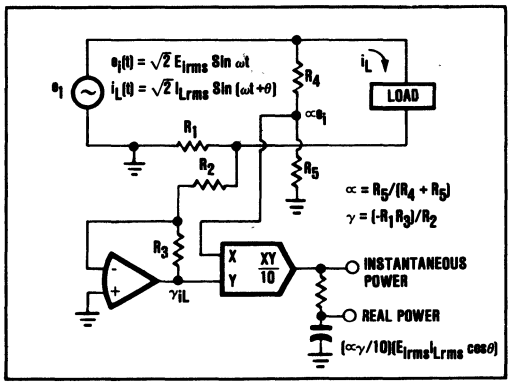


FIGURE 15. Single-Phase Instantaneous and Real Power Measurement.

MORE CIRCUITS

The theory and procedures for developing virtually any function generator or linearization circuit can be found in the Burr-Brown/McGraw Hill book "FUNCTION CIRCUITS - Design and Applications."

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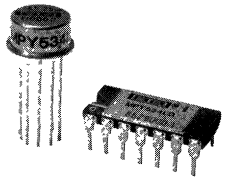


MPY534

MILITARY & DIE VERSIONS AVAILABLE

Precision ANALOG MULTIPLIER

FEATURES

- ±0.25% MAX 4-QUADRANT ERROR
- WIDE BANDWIDTH: 1MHz MIN, 3MHz TYP
- ADJUSTABLE SCALE FACTOR: GAINS TO 100
- STABLE AND RELIABLE MONOLITHIC CONSTRUCTION
- LOW COST

APPLICATIONS

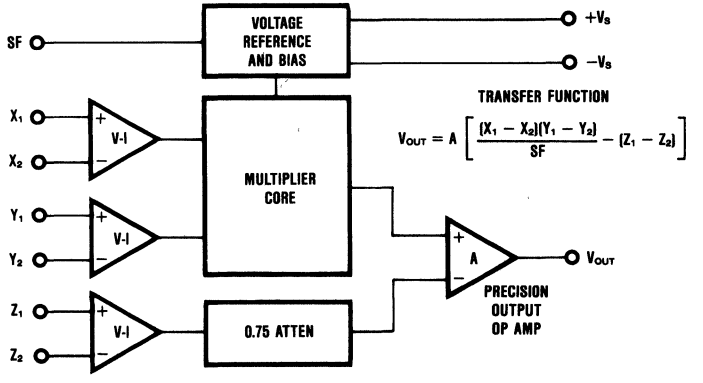
- PRECISION ANALOG SIGNAL PROCESSING
- VIDEO SIGNAL PROCESSING
- VOLTAGE CONTROLLED FILTERS AND OSCILLATORS
- MODULATION AND DEMODULATION
- RATIO AND PERCENTAGE COMPUTATION

DESCRIPTION

The MPY534 is a high accuracy, general purpose four-quadrant analog multiplier. Its accurately laser trimmed transfer characteristics make it easy to use in a wide variety of applications with a minimum of external parts and trimming circuitry. Its differential X, Y and Z inputs allow configuration as a multiplier, squarer, divider, square-rooter and other functions while maintaining high accuracy.

The wide bandwidth of this new design allows accurate signal processing at higher frequencies suitable for video signal processing. It is capable of performing IF and RF frequency mixing, modulation and demodulation with excellent carrier rejection and very simple feedthrough adjustment.

An accurate internal voltage reference provides precise setting of the scale factor. The differential Z input allows user selected scale factors from 0.1 to 10 using external feedback resistors.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_S = ±15VDC unless otherwise specified

MODEL	MPY534J			MPY534K			MPY534L			MPY534S			MPY534T			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
MULTIPLIER PERFORMANCE																
Transfer Function		*			$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z_2$			*			*			*		
Total Error[1]																
(−10V ≤ X, Y ≤ +10V)			±1 0			±0 5			±0 25			±1 0			*	%
T_A = min to max		±1 5			±1 0			±0 5				±2 0			±1 0	%
Total Error vs Temperature		±0 022			±0 015			±0 008				±0 02			±0 01	%/°C
Scale Factor Error																
(SF = 10 000V Nominal)[2]		±0 25			±0 1			*			±0 25			*		%
Temperature Coefficient of Scaling Voltage		±0 02			±0 01			±0 005			±0 02				±0 005	%/°C
Supply Rejection (±15V ±1V)		*			±0 01			*			*			*		%
Nonlinearity																
X (X = 20V pk-pk, Y = 10V)		±0 4			±0 2	±0 3		±0 10	±0 12		±0 4			*	*	%
Y (Y = 20V pk-pk, X = 10V)		*			±0 01	±0 1		±0 005	*		*			*	*	%
Feedthrough[3]																
X (Y Nulled, Y = 20V pk-pk, 50Hz)		±0 3			±0 15	±0 3		±0 05	±0 12		±0 3			*	*	%
Y (X Nulled, Y = 20V pk-pk, 50Hz)		*			±0 01	±0 1		±0 003	*		*			*	*	%
Output Offset Voltage		±5	±30		±2	±15		*	±10		±5	±30		*	*	mV
Output Offset Voltage Drift		200			100			*				500			300	µV/°C
DYNAMICS																
Small Signal BW, (V_{OUT} = 0 1V rms)	*	*		1	3		*	*		*	*		*	*		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		*			50			*			*			*		kHz
Slew Rate (V_{OUT} = 20V pk-pk)		*			20			*			*			*		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20V)		*			2			*			*			*		µs
NOISE																
Noise Spectral Density SF = 10V		*			0 8			*			*			*		µV/√Hz
Wideband Noise																
f = 10Hz to 5MHz		*			1			*			*			*		mVrms
f = 10Hz to 10kHz		*			90			*			*			*		µVrms
OUTPUT																
Output Voltage Swing	*			±11			*			*			*			V
Output Impedance (f ≤ 1kHz)		*			0 1			*			*			*		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		*			30			*			*			*		mA
Amplifier Open Loop Gain (f = 50Hz)		*			70			*			*			*		dB
INPUT AMPLIFIERS (X, Y and Z)																
Input Voltage Range																
Differential V_{IN} (V_{CM} = 0)		*			±12			*			*			*		V
Common-Mode V_{IN} (V_{DIFF} = 0) (see Typical Performance Curves)		*			±10			*			*			*		V
Offset Voltage X, Y		±5	±20		±2	±10		*	*		±5	±20		*	*	mV
Offset Voltage Drift X, Y		100			50			*			100			*		µV/°C
Offset Voltage Z		±5	±30		±2	±15		*	±10		±5	±30		*	*	mV
Offset Voltage Drift Z		200			100			*				500			300	µV/°C
CMRR	60	80		70	90		*	*		60	80		*	*		dB
Bias Current		*	*		0 8	2 0		*	*		*	*		*	*	µA
Offset Current		*			0 1			0 05	0 2		*	2 0		*	2 0	µA
Differential Resistance		*			10			*			*			*		MΩ
DIVIDER PERFORMANCE																
Transfer Function ($X_1 > X_2$)		*			$10V\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$											
Total Error[1]																
(X = 10V, −10V ≤ Z ≤ +10V)		±0 75			±0 35			±0 2			±0 75			*		%
(X − 1V, −1V ≤ Z ≤ +1V)		±2 0			±1 0			±0 8			±2 0			*		%
(0 1V ≤ X ≤ 10V, −10V ≤ Z ≤ 10V)		±2 5			±1 0			±0 8			±2 5			*		%

*Specifications same as for MPY534K

ELECTRICAL (CONT)

At T_A = +25°C and V_S = ±15VDC unless otherwise specified

MODEL	MPY534J			MPY534K			MPY534L			MPY534S			MPY534T			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SQUARE PERFORMANCE																
Transfer Function		*			$\frac{(X_1 - X_2)^2}{10V} + Z_2$			*			*			*		
Total Error (−10V ≤ X ≤10V)		0 6			±0.3			±0 2			±0 6			*		%
SQUARE-ROOTER PERFORMANCE																
Transfer Function ($Z_1 \leq Z_2$)		*			$\sqrt{10V(Z_2 - Z_1)} + X_2$			*			*			*		
Total Error[1] (1V ≤ Z ≤ 10V)		±1 0			±0 5			±0 25			±1 0			±0 5		%
POWER SUPPLY																
Supply Voltage																
Rated Performance		*			±15			*			*			*		VDC
Operating	*		*	±8		±18	*		*	*		±20	*		±20	VDC
Supply Current, Quiescent		*	*		4	6		*	*		*	*		*	*	mA
TEMPERATURE RANGE																
Operating	*		*	0		+70	*		*	−55		+125	−55		+125	°C
Storage	*		*	−65		+150	*		*	*		*	*		*	°C

*Specification same as for MPY534K

NOTES (1) Figures given are percent of full scale, ±10V (i e , 0 01% = 1mV) (2) May be reduced to 3V using external resistor between $-V_S$ and SF (3) Irreducible component due to nonlinearity, excludes effect of offsets

ABSOLUTE MAXIMUM RATINGS

Parameter	MPY534J, K, L	MPY534S, T
Power Supply Voltage	±18	±20
Power Dissipation	500mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltage (all X, Y and Z)	$\pm V_S$	*
Operating Temperature Range	0°C to +70°C	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	*
Lead Temperature (10s soldering)	300°C	*

*Specification same as for MPY534K

MPY534**

Grade Designation

J, K, L: 0 to 70°C

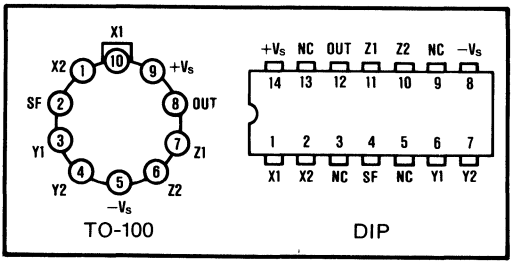
S, T: −55 to 125°C

Package Designation

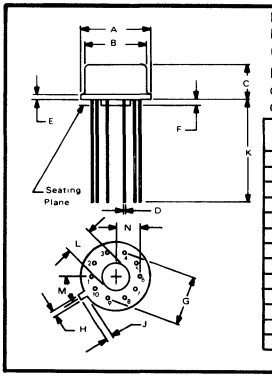
H = TO-100

D = DIP

PIN CONFIGURATION (TOP VIEW)



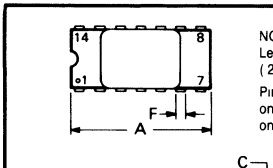
MECHANICAL



NOTE
Leads in true position within .010" (.25mm) R at MMT at seating plane

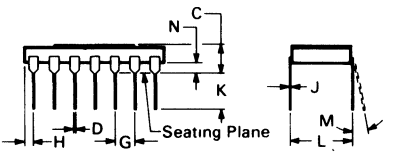
Pin numbers shown for reference only. Numbers may not be marked on package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.70	--
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05



NOTE
Leads in true position within .010" (.25mm) R at MMT at seating plane

Pin numbers shown for reference only. Numbers may not be marked on package

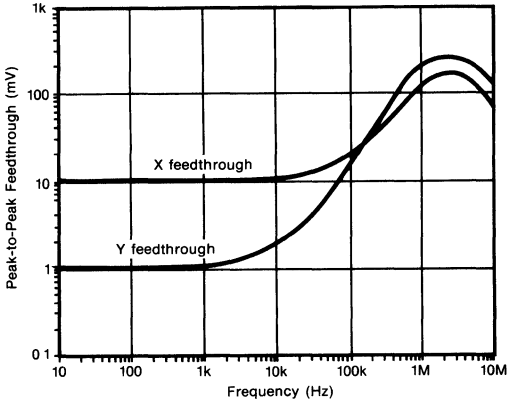


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.009	.060	0.23	1.52

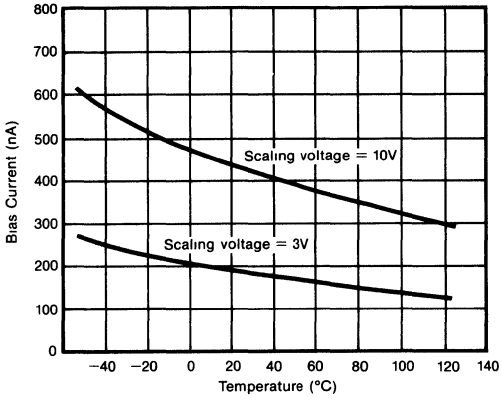
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15VDC unless otherwise noted

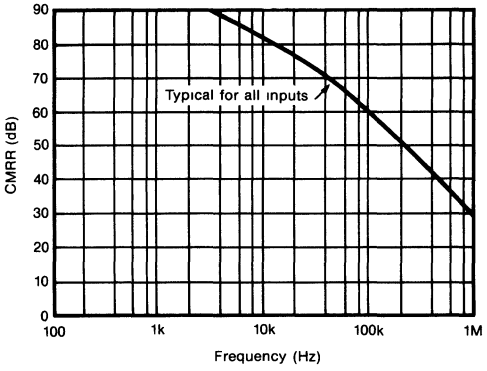
AC FEEDTHROUGH
VS FREQUENCY



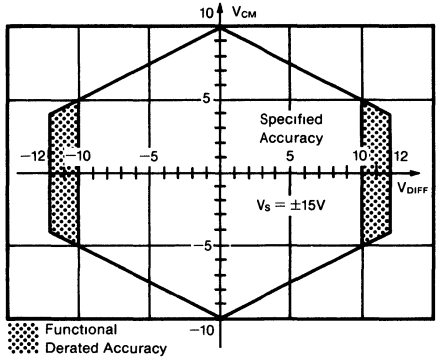
BIAS CURRENTS VS TEMPERATURE
(X, Y or Z inputs)



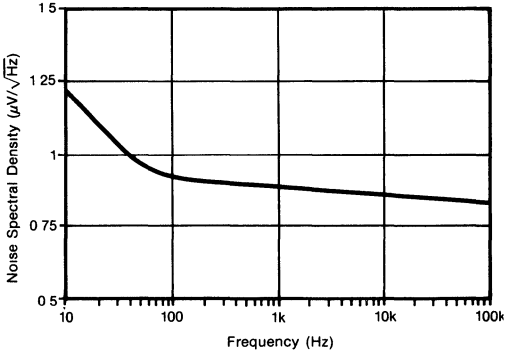
COMMON-MODE-REJECTION RATIO
VS FREQUENCY



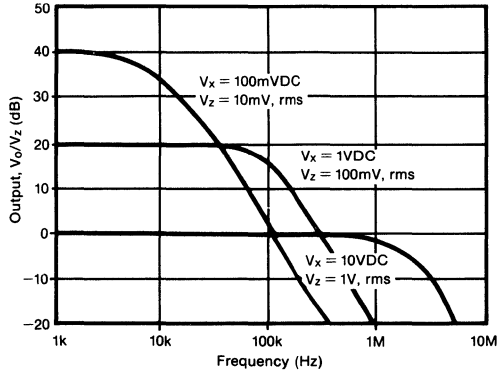
INPUT DIFFERENTIAL-MODE/
COMMON-MODE VOLTAGE



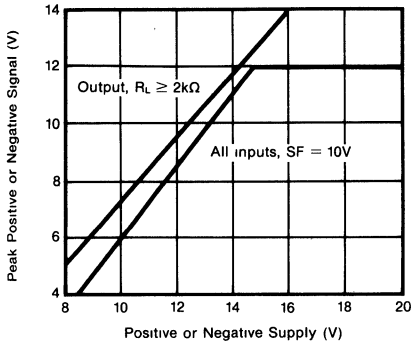
NOISE SPECTRAL DENSITY
VS FREQUENCY



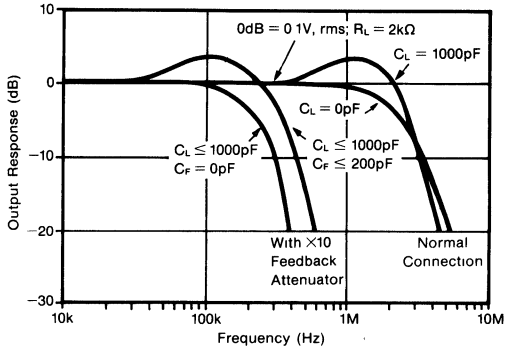
FREQUENCY RESPONSE VS
DIVIDER DENOMINATOR INPUT VOLTAGE



INPUT/OUTPUT SIGNAL RANGE
VS SUPPLY VOLTAGES



FREQUENCY RESPONSE
AS A MULTIPLIER



THEORY OF OPERATION

The transfer function for the MPY534 is:

$$V_{OUT} = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right]$$

where:

A = Open-loop gain of the output amplifier (Typically 85dB at DC).

SF = Scale Factor. Laser-trimmed to 10V but adjustable over a 3V to 10V range using external resistor.

X, Y, Z are input voltages. Full-scale input voltage is equal to the selected SF. (Max input voltage = ±1.25 SF.)

An intuitive understanding of transfer function can be gained by analogy to an op amp. By assuming that the open-loop gain, A, of the output amplifier is infinite, inspection of the transfer function reveals that any V_{OUT} can be created with an infinitesimally small quantity within the brackets. Then, an application circuit can be analyzed by assigning circuit voltages for all X, Y and Z inputs and setting the bracketed quantity equal to zero. For example, the basic multiplier connection in Figure 1, $Z_1 = V_{OUT}$ and $Z_2 = 0$. The quantity within the brackets then reduces to:

$$\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (V_{OUT} - 0) = 0$$

This approach leads to a simple relationship which can be solved for V_{OUT}.

The scale factor is accurately factory-adjusted to 10V and is typically accurate to within 0.1% or less. The scale factor may be adjusted by connecting a resistor or potentiometer between pin SF and the $-V_S$ power supply. The value of the external resistor can be approximated by:

$$R_{SF} = 5.4k\Omega\left[\frac{SF}{10 - SF}\right]$$

Internal device tolerances make this relationship accurate to within approximately 25%. Some applications can benefit from reduction of the SF by this technique. The reduced input bias current and drift achieved by this technique can be likened to operating the input circuitry in a higher gain, thus reducing output contributions to these effects. Adjustment of the scale factor does not affect bandwidth.

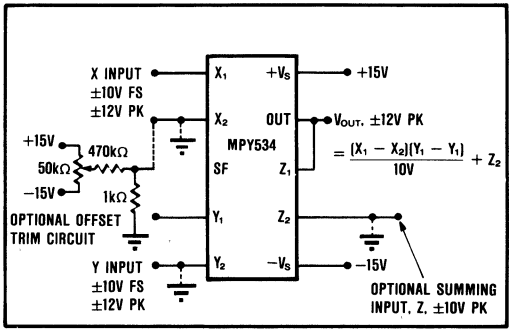


FIGURE 1. Basic Multiplier Connection.

The MPY534 is fully characterized at $V_S = \pm 15V$ but operation is possible down to ±8V with an attendant reduction of input and output range capability. Operation at voltages greater than ±15V allows greater output swing to be achieved by using an output feedback attenuator (Figure 2).

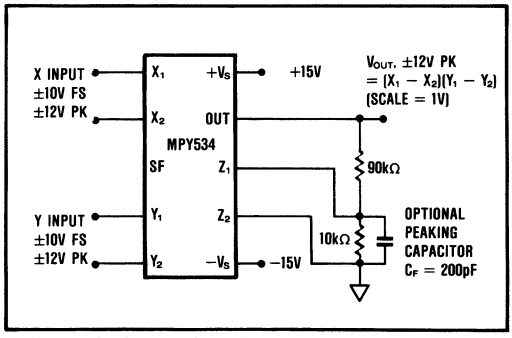


FIGURE 2. Connections for Scale-Factor of Unity.

BASIC MULTIPLIER CONNECTION

Figure 1 shows the basic connection as a multiplier. Accuracy is fully specified without any additional user trimming circuitry. Some applications can benefit from trimming one or more of the inputs. The fully differential inputs facilitate referencing the input quantities to the source voltage common terminal for maximum accuracy. They also allow use of simple offset voltage trimming circuitry as shown on the X input.

The differential Z input allows an offset to be summed in V_{OUT}. In basic multiplier operation the Z_2 input serves as the output voltage reference and should be connected to the ground reference of the driven system for maximum accuracy.

A method of changing (lowering) SF by connecting to the SF pin was discussed previously. Figure 2 shows another method of changing the effective SF of the overall circuit using an attenuator in the feedback connection to Z_1. This method puts the output amplifier in a higher gain and is thus accompanied by a reduction in bandwidth and an increase in output offset voltage. The larger output offset may be reduced by applying a trimming voltage to the high impedance input, Z_2.

The flexibility of the differential Z inputs allows direct conversion of the output quantity to a current. Figure 3 shows the output voltage differentially-sensed across a series resistor forcing an output-controlled current. Addition of a capacitor load then creates a time integration function useful in a variety of applications such as power computation.

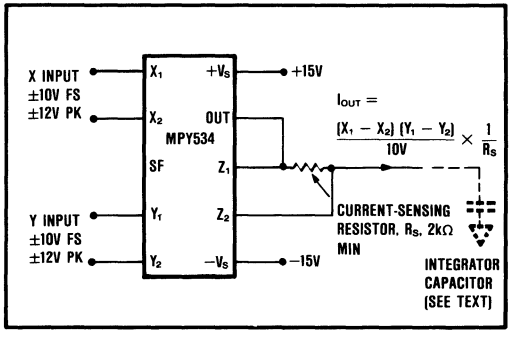


FIGURE 3. Conversion of Output to Current.

SQUARER CIRCUIT

Squarer operation is achieved by paralleling the X and Y inputs of the standard multiplier circuit. Inverted output can be achieved by reversing the differential input terminals of either the X or Y input. Accuracy in the squaring mode is typically a factor of two better than the specified multipler mode with maximum error occurring with small (less than 1V) inputs. Better accuracy can be achieved for small input voltage levels by using a reduced SF value.

DIVIDER OPERATION

The MPY534 can be configured as a divider as shown in Figure 4. High impedance differential inputs for the numerator and denominator are achieved at the Z and X inputs respectively. Feedback is applied to the Y_2 input, and Y_1 is normally referenced to output ground. Alternatively, as the transfer function implies, an input applied to Y_1 can be summed directly into V_{OUT}. Since the feedback connection is made to a multiplying input, the effective gain of the output op amp varies as a function of the denominator input voltage. Therefore the bandwidth of the divider function is proportional to the denominator voltage (see Typical Performance Curves).

Accuracy of the divider mode typically ranges from 0.75% to 2.0% for a 10 to 1 denominator range depending on device grade. Accuracy is primarily limited by input offset voltages and can be significantly improved by trimming the offset of the X input. A trim voltage of ±3.5mV applied to the "low side" X input (X_2 for positive input voltages on X_1) can produce similar accuracies over a 100 to 1 deonominator range. To trim, apply a signal which varies from 100mV to 10V at a low frequency (less than 500Hz) to both inputs. An offset sine wave or ramp is suitable. Since the ratio of the quantities should be constant, the ideal output would be a constant 10V. Using AC coupling on an oscilloscope, adjust the offset control for minimum output voltage variation.

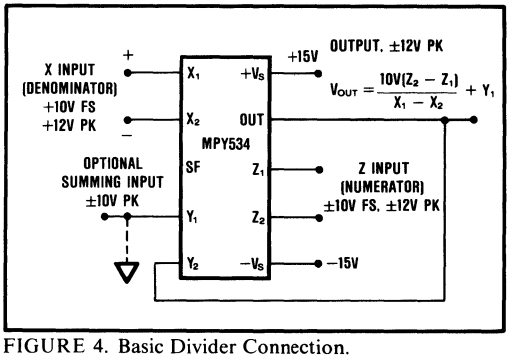


FIGURE 4. Basic Divider Connection.

SQUARE-ROOTER

A square-rooter connection is shown in Figure 5. Input voltage is limited to one polarity (positive for the connection shown). The diode prevents circuit latch-up

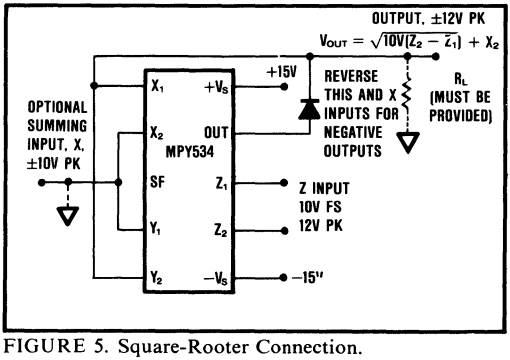


FIGURE 5. Square-Rooter Connection.

should the input go negative. The circuit can be configured for negative input and positive output by reversing the polarity of both the X and Y inputs. The output polarity can be reversed by reversing the diode and X input polarity. A load resistance of approximately 10kΩ must be provided. Trimming for improved accuracy would be accomplished at the Z input.

APPLICATIONS

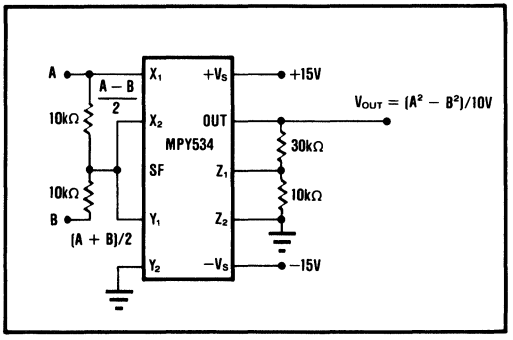


FIGURE 6. Difference-of-Squares.

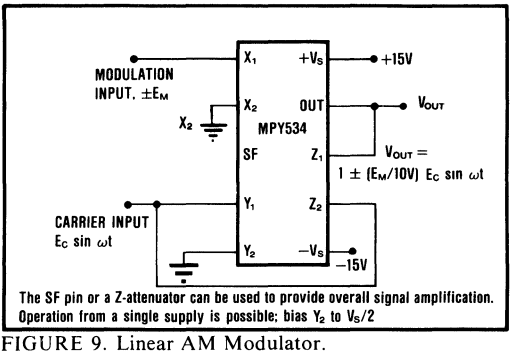


FIGURE 9. Linear AM Modulator.

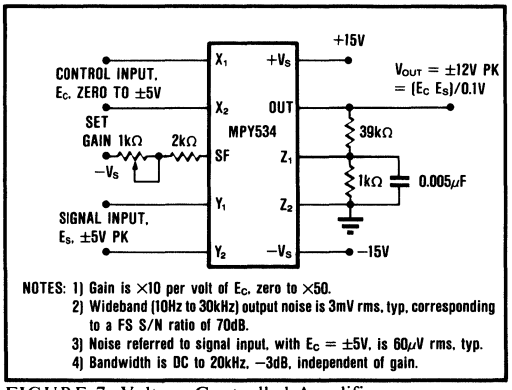


FIGURE 7. Voltage-Controlled Amplifier.

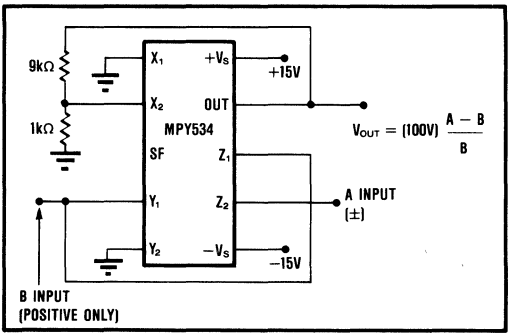


FIGURE 10. Percentage Computer.

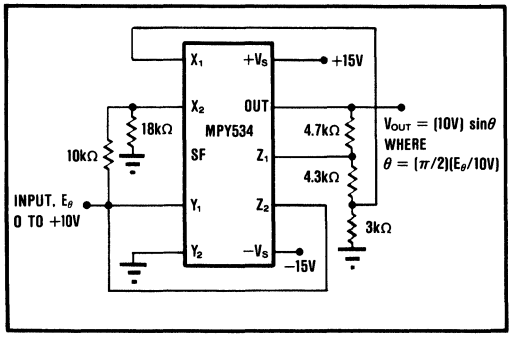


FIGURE 8. Sine-Function Generator.

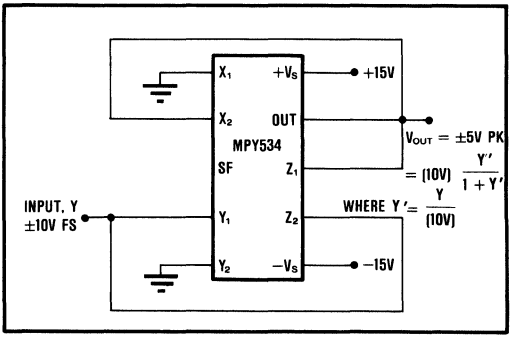


FIGURE 11. Bridge-Linearization Function.

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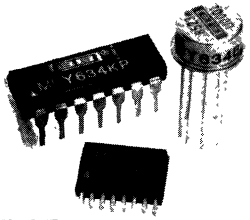


MPY634

Wide Bandwidth PRECISION ANALOG MULTIPLIER

FEATURES

- WIDE BANDWIDTH: 10MHz typ
- ±0.5% MAX FOUR-QUADRANT ERROR
- INTERNAL WIDE-BANDWIDTH OP AMP
- EASY TO USE
- LOW COST
- ENHANCED RELIABILITY SCREENING AVAILABLE

APPLICATIONS

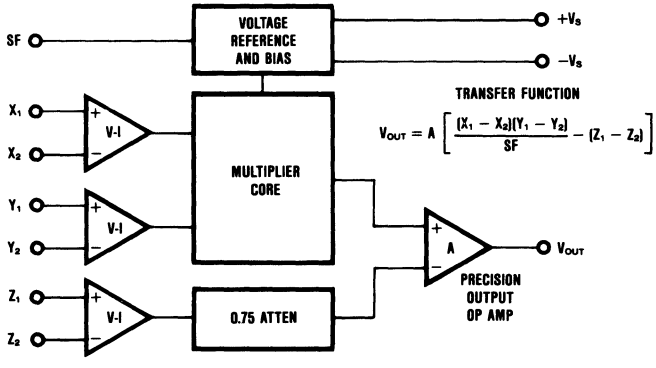
- PRECISION ANALOG SIGNAL PROCESSING
- MODULATION AND DEMODULATION
- VOLTAGE-CONTROLLED AMPLIFIERS
- VIDEO SIGNAL PROCESSING
- VOLTAGE-CONTROLLED FILTERS AND OSCILLATORS

DESCRIPTION

The MPY634 is a wide bandwidth, high accuracy, four-quadrant analog multiplier. Its accurately laser-trimmed multiplier characteristics make it easy to use in a wide variety of applications with a minimum of external parts, often eliminating all external trimming. Its differential X, Y, and Z inputs allow configuration as a multiplier, squarer, divider, square-rooter, and other functions while maintaining high accuracy.

The wide bandwidth of this new design allows signal processing at I.F., R.F., and video frequencies. The internal output amplifier of the MPY634 reduces design complexity compared to other high frequency multipliers and balanced modulator circuits. It is capable of performing frequency mixing, balanced modulation, and demodulation with excellent carrier rejection.

An accurate internal voltage reference provides precise setting of the scale factor. The differential Z input allows user-selected scale factors from 0.1 to 10 using external feedback resistors.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-636B

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_S = ±15VDC unless otherwise specified.

MODEL	MPY634KP/KU			MPY634AM			MPY634BM			MPY634SM			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
MULTIPLIER PERFORMANCE					$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z_2$								
Transfer Function		*						*			*		
Total Error[1]													
(−10V ≤ X, Y ≤ +10V)			±2 0			±1 0			±0 5			*	%
T_A = min to max		±2 5			±1 5			±1.0				±2 0	%
Total Error vs Temperature		±0 03			±0 022			±0 015				±0 02	%/°C
Scale Factor Error													
(SF = 10 000V Nominal)[2]		±0 25			±0 1			*			*		%
Temperature Coefficient of													
Scaling Voltage		±0 02			±0 01			±0 01			*		%/°C
Supply Rejection (±15V ±1V)		*			±0 01			*			*		%
Nonlinearity													
X (X = 20Vp-p, Y = 10V)		*			±0.4			0 2	±0.3		*		%
Y (Y = 20Vp-p, X = 10V)		*			±0 01			*	±0 1		*		%
Feedthrough[3]													
X (Y Nulled, Y = 20V													
p-p, 50Hz)		±0 3			±0 3			±0 15	±0 3		*		%
Y (X Nulled, Y = 20V													
p-p, 50Hz)		*			±0 01			*	±0 1		*		%
Both Inputs (500kHz, 1V rms)													
Unnulled	40[4]	50		45	55		*	60		*	*		dB
Nulled	55[4]	60		55	65		60	70		*	*		dB
Output Offset Voltage		±50	±100		±5	±30		*	±15		*	*	mV
Output Offset Voltage Drift		*			±200			±100			*	±500	μV/°C
DYNAMICS													
Small Signal BW,													
(V_{OUT} = 0 1V rms)	6[4]	*		8	10		*	*		6	*		MHz
1% Amplitude Error													
(C_{LOAD} = 1000pF)		*			100			*			*		kHz
Slew Rate (V_{OUT} = 20Vp-p)		*			20			*			*		V/μs
Settling Time													
(to 1%, ΔV_{OUT} = 20V)		*			2			*			*		μs
NOISE													
Noise Spectral Density													
SF = 10V		*			0 8			*			*		$\mu V/\sqrt{Hz}$
Wideband Noise													
f = 10Hz to 5MHz		*			1			*			*		mVrms
f = 10Hz to 10kHz		*			90			*			*		μVrms
OUTPUT													
Output Voltage Swing	*			±11			*			*			V
Output Impedance (f ≤ 1kHz)		*			0 1			*			*		Ω
Output Short Circuit Current													
(R_L = 0, T_A = min to max)		*			30			*			*		mA
Amplifier Open Loop Gain													
(f = 50Hz)		*			85			*			*		dB
INPUT AMPLIFIERS (X, Y and Z)													
Input Voltage Range													
Differential V_{IN} (V_{CM} = 0)		*			±12			*			*		V
Common-Mode V_{IN} (V_{DIFF} = 0)		*			±10			*			*		V
(see Typical Performance Curves)													
Offset Voltage X, Y		±25	±100		±5	±20		±2	±10		*	*	mV
Offset Voltage Drift X, Y		200			100			50			*		μV/°C
Offset Voltage Z		±25	±100		±5	±30		±2	±15		*	*	mV
Offset Voltage Drift Z		*			200			100				500	μV/°C
CMRR	*	*		60	80		70	90		*	*		dB
Bias Current		*	*		0 8	2.0		*	*		*	*	μA
Offset Current		*			0.1			*			*	2 0	μA
Differential Resistance		*			10			*			*		MΩ
DIVIDER PERFORMANCE													
Transfer Function ($X_1 > X_2$)		*			$10V\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$			*			*		
Total Error[1] untrimmed													
(X = 10V, −10V ≤ Z ≤ +10V)		1 5			±0.75			±0.35			±0 75		%
(X = 1V, −1V ≤ Z ≤ +1V)		4 0			±2 0			±1.0			*		%
(0 1V ≤ X ≤ 10V, −10V ≤													
Z ≤ 10V)		5 0			±2 5			±1 0			*		%

ELECTRICAL (CONT)

At T_A = +25°C and V_S = ±15VDC unless otherwise specified

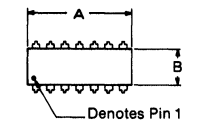
MODEL	MPY634KP/KU			MPY634AM			MPY634BM			MPY634SM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SQUARE PERFORMANCE					$\frac{(X_1 - X_2)^2}{10V} + Z_2$								
Transfer Function		*						*			*		
Total Error (−10V ≤ X ≤10V)		±1 2			±0 6			±0 3			*		%
SQUARE-ROOTER PERFORMANCE													
Transfer Function ($Z_1 \leq Z_2$)		*			$\sqrt{10V(Z_2 - Z_1)} + X_2$			*			*		
Total Error[1] (1V ≤ Z ≤ 10V)		±2 0			±1 0			±0 5			*		%
POWER SUPPLY													
Supply Voltage													
Rated Performance		*			±15			*			*		VDC
Operating	*		*	±8		±18	*		*	*		±20	VDC
Supply Current, Quiescent		*	*		4	6		*	*		*	*	mA
TEMPERATURE RANGE													
Specification	*[5]		*[5]	−25		+85	*		*	−55		+125	°C
Storage	−40		+85	−65		+150	*		*	*		*	°C

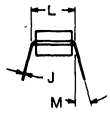
*Specification same as for MPY634AM.

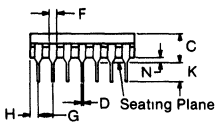
NOTES: (1) Figures given are percent of full scale, ±10V (i e , 0.01% = 1mV). (2) May be reduced to 3V using external resistor between $-V_S$ and SF (3) Irreducible component due to nonlinearity, excludes effect of offsets. (4) KP grade only (5) KP grade only 0°C to +70°C for KU grade

MECHANICAL

PLASTIC DUAL-IN-LINE



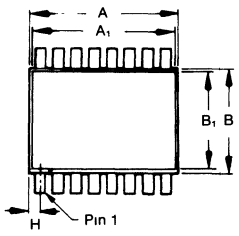


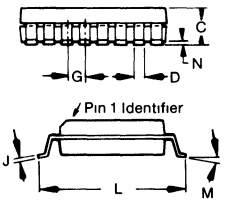


NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	660	785	16 76	19 94
B	220	280	5 59	7 11
C	—	200	—	5 08
D	015	023	0 38	0 58
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	030	095		
J	008	015	0 20	0 38
K	100	—	2 54	—
L	300 BASIC		7 62 BASIC	
M	—	15°	—	15°
N	020	050	0 51	1 27

SMALL OUTLINE SURFACE MOUNT

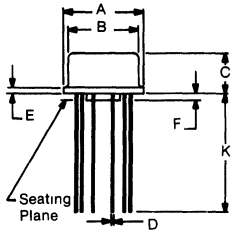




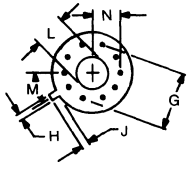
NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	400	416	10 16	10 57
A_1	388	412	9 86	10 46
B	286	302	7 26	7 67
B_1	.268	286	6 81	7 26
C	093	109	2 36	2 77
D	015	020	0 38	0 51
G	050 BASIC		1 27 BASIC	
H	022	038	0 56	0 97
J	008	012	0 20	0 30
L	391	421	9 93	10 69
M	5° TYP		5° TYP	
N	000	012	0 00	0 30

METAL TO-100



NOTE· Leads in true position within 0.01" (0 25mm) R at MMC at seating plane.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	335	370	8 51	9 40
B	305	335	7 75	8 51
C	165	185	4 19	4 70
D	016	021	0 41	0 53
E	010	040	0 25	1 02
F	010	040	0 25	1 02
G	230 BASIC		5 84 BASIC	
H	028	034	0 71	0 86
J	029	045	0 74	1 14
K	500	—	12 70	—
L	120	160	3 05	4 06
M	36° BASIC		36° BASIC	
N	110	120	2 79	3 05

ABSOLUTE MAXIMUM RATINGS

Parameter	MPY634AM/BM	MPY634KP/KU	MPY634SM
Power Supply Voltage	±18	*	±20
Power Dissipation	500mW	*	*
Output Short-Circuit to Ground	Indefinite	*	*
Input Voltage (all X, Y and Z)	$\pm V_S$	*	*
Temperature Range·			
Operating	−25/+85°C	*	−55/+125°C
Storage	−65/+150°C	−40/+85°C	*
Lead Temperature (10s soldering)	+300°C	*	*
SOIC 'KU' Package		+260°C	

* Specification same as for MPY634AM/BM

ORDERING INFORMATION

MPY634 ( ) ( ) (/QM)

Basic Model Number

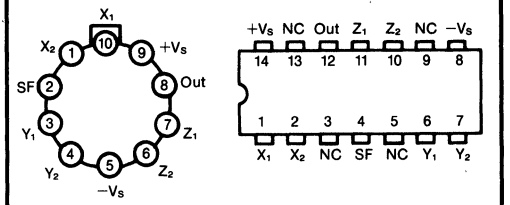
Performance Grade
- K −25°C to +85°C ('U' package 0°C to +70°C)[1]
- A −25°C to +85°C
- B −25°C to +85°C
- S −55°C to +125°C

Package Code
- M TO-100 metal
- P Plastic 14-pin DIP
- U 16-pin SOIC

Enhanced reliability screening (/QM option) available on MPY634SM Contact your Burr-Brown representative for information

NOTE (1) Performance grade identifier may not be marked Blank denotes "K" grade

PIN CONFIGURATIONS (TOP VIEW)



TO-100: MPY634AM/BM/SM **DIP: MPY634KP**

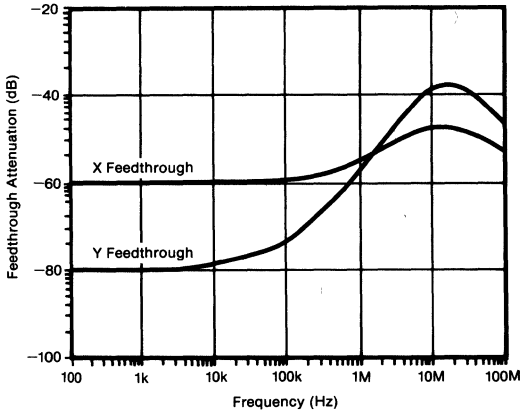
X1 Input	1	16	−VS
X2 Input	2	15	NC
NC	3	14	Output
Scale Factor	4	13	Z2 Input
NC	5	12	Z2 Input
Y1 Input	6	11	NC
Y2 Input	7	10	VS
NC	8	9	NC

SOIC: MPY634KU

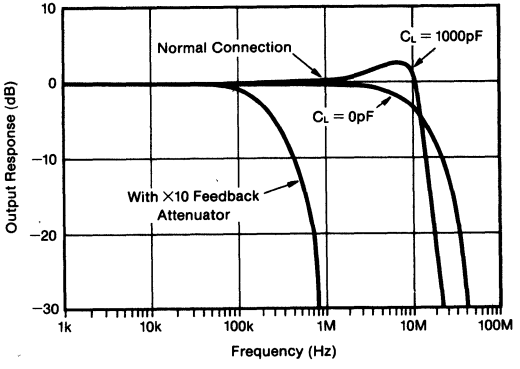
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15VDC unless otherwise noted

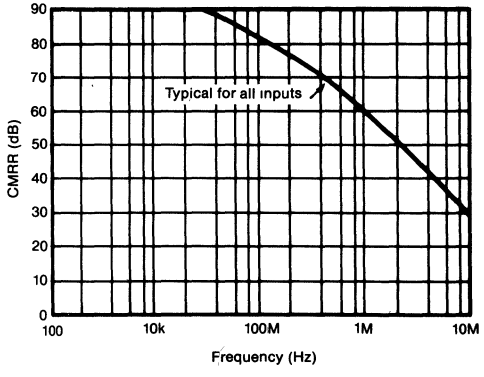
FEEDTHROUGH VS FREQUENCY



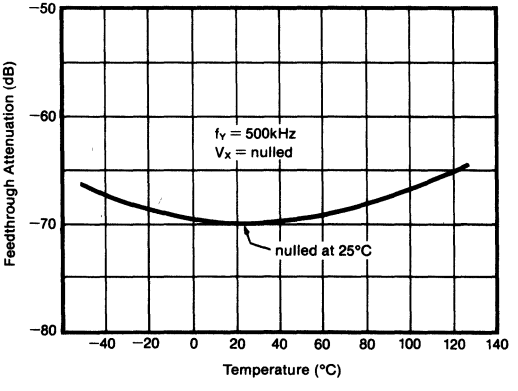
FREQUENCY RESPONSE AS A MULTIPLIER



COMMON-MODE REJECTION RATIO VS FREQUENCY



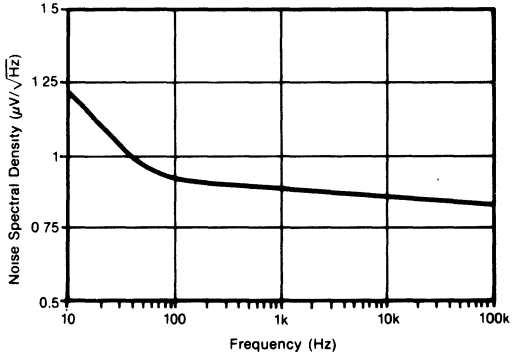
FEEDTHROUGH VS TEMPERATURE



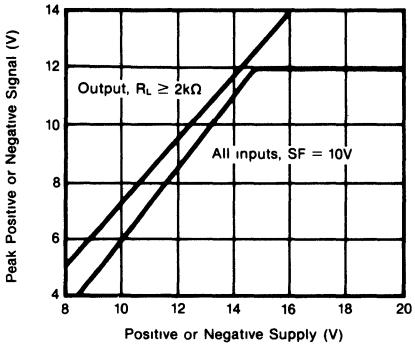
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15VDC unless otherwise noted.

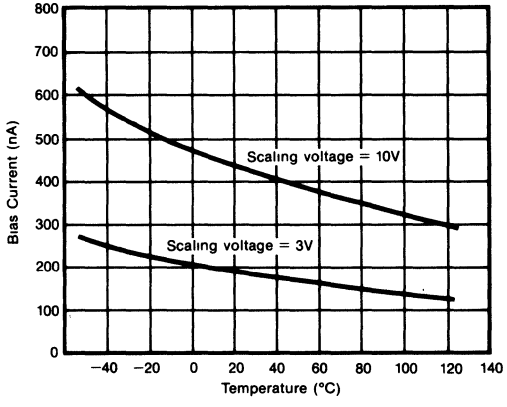
NOISE SPECTRAL DENSITY VS FREQUENCY



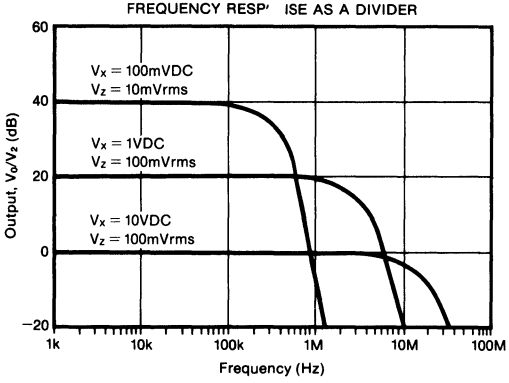
INPUT/OUTPUT SIGNAL RANGE VS SUPPLY VOLTAGES



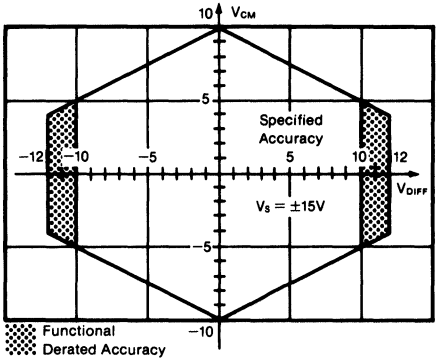
BIAS CURRENTS VS TEMPERATURE (X, Y or Z inputs)



FREQUENCY RESPONSE AS A DIVIDER



INPUT DIFFERENTIAL-MODE/ COMMON-MODE VOLTAGE



THEORY OF OPERATION

The transfer function for the MPY634 is:

$$V_{OUT} = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right]$$

where:

A = open-loop gain of the output amplifier (typically 85dB at DC).

SF = Scale Factor. Laser-trimmed to 10V but adjustable over a 3V to 10V range using external resistors.

X, Y, Z are input voltages. Full-scale input voltage is equal to the selected SF. (Max input voltage = ±1.25 SF.)

An intuitive understanding of transfer function can be gained by analogy to the op amp. By assuming that the open-loop gain, A, of the output operational amplifier is infinite, inspection of the transfer function reveals that any V_{OUT} can be created with an infinitesimally small quantity within the brackets. Then, an application circuit can be analyzed by assigning circuit voltages for all X, Y and Z inputs and setting the bracketed quantity equal to zero. For example, the basic multiplier connection in Figure 1, $Z_1 = V_{OUT}$ and $Z_2 = 0$. The quantity within the brackets then reduces to:

$$\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (V_{OUT} - 0) = 0$$

This approach leads to a simple relationship which can be solved for V_{OUT} to provide the closed-loop transfer function.

The scale factor is accurately factory adjusted to 10V and is typically accurate to within 0.1% or less. The scale factor may be adjusted by connecting a resistor or potentiometer between pin SF and the $-V_S$ power supply. The value of the external resistor can be approximated by:

$$R_{SF} = 5.4k\Omega \left[\frac{SF}{10 - SF}\right]$$

Internal device tolerances make this relationship accurate to within approximately 25%. Some applications can benefit from reduction of the SF by this technique. The reduced input bias current, noise, and drift achieved by this technique can be likened to operating the input circuitry in a higher gain, thus reducing output contributions to these effects. Adjustment of the scale factor does not affect bandwidth.

The MPY634 is fully characterized at $V_S = \pm 15V$ but operation is possible down to $\pm 8V$ with an attendant reduction of input and output range capability. Operation at voltages greater than $\pm 15V$ allows greater output swing to be achieved by using an output feedback attenuator (Figure 1).

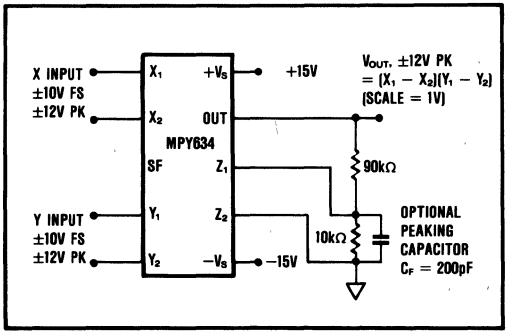


FIGURE 1. Connections for Scale-Factor of Unity.

As with any wide bandwidth circuit, the power supplies should be bypassed with high frequency ceramic capacitors. These capacitors should be located as near as practical to the power supply connections of the MPY634. Improper bypassing can lead to instability, overshoot, and ringing in the output.

BASIC MULTIPLIER CONNECTION

Figure 2 shows the basic connection as a multiplier. Accuracy is fully specified without any additional user-trimming circuitry. Some applications can benefit from trimming of one or more of the inputs. The fully differential inputs facilitate referencing the input quantities to the source voltage common terminal for maximum accuracy. They also allow use of simple offset voltage trimming circuitry as shown on the X input.

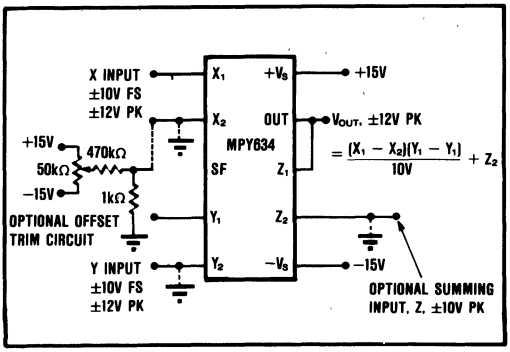


FIGURE 2. Basic Multiplier Connection.

The differential Z input allows an offset to be summed in V_{OUT}. In basic multiplier operation the Z_2 input serves as the output voltage ground reference and should be connected to the ground of the driven system for maximum accuracy.

A method of changing (lowering) SF by connecting to the SF pin was discussed previously. Figure 1 shows an alternative method of changing the effective SF of the overall circuit by using an attenuator in the feedback connection to Z_1. This method puts the output amplifier in a higher gain and is thus accompanied by a reduction in bandwidth and an increase in output offset voltage. The larger output offset may be reduced by applying a trimming voltage to the high impedance input, Z_2.

The flexibility of the differential Z inputs allows direct conversion of the output quantity to a current. Figure 3 shows the output voltage differentially-sensed across a series resistor forcing an output-controlled current. Addition of a capacitor load then creates a time integration function useful in a variety of applications such as power computation.

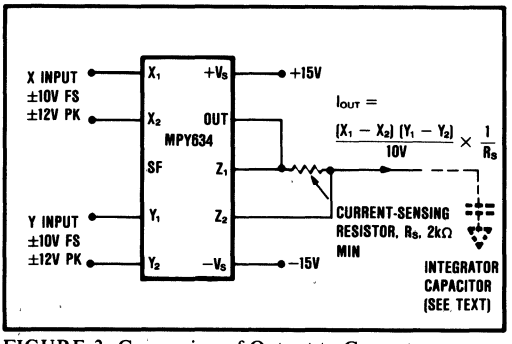


FIGURE 3. Conversion of Output to Current.

SQUARER CIRCUIT (FREQUENCY DOUBLER)

Squarer, or frequency doubler, operation is achieved by paralleling the X and Y inputs of the standard multiplier circuit. Inverted output can be achieved by reversing the differential input terminals of either the X or Y input. Accuracy in the squaring mode is typically a factor of

two better than the specified multiplier mode with maximum error occurring with small (less than 1V) inputs. Better accuracy can be achieved for small input voltage levels by reducing the scale factor, SF.

DIVIDER OPERATION

The MPY634 can be configured as a divider as shown in Figure 4. High impedance differential inputs for the numerator and denominator are achieved at the Z and X inputs respectively. Feedback is applied to the Y_2 input, and Y_1 is normally referenced to output ground. Alternatively, as the transfer function implies, an input applied to Y_1 can be summed directly into V_{OUT}. Since the feedback connection is made to a multiplying input, the effective gain of the output op amp varies as a function of the denominator input voltage. Therefore, the bandwidth of the divider function is proportional to the denominator voltage (see Typical Performance Curves).

Accuracy of the divider mode typically ranges from 1.0% to 2.5% for a 10 to 1 denominator range depending on device grade. Accuracy is primarily limited by input offset voltages and can be significantly improved by trimming the offset of the X input. A trim voltage of ±3.5mV applied to the "low side" X input (X_2 for positive input voltages on X_1) can produce similar accuracies over a 100 to 1 denominator range. To trim, apply a signal which varies from 100mV to 10V at a low frequency (less than 500Hz). An offset sine wave or ramp is suitable. Since the ratio of the quantities should be constant, the ideal output would be a constant 10V. Using AC coupling on an oscilloscope, adjust the offset control for minimum output voltage variation.

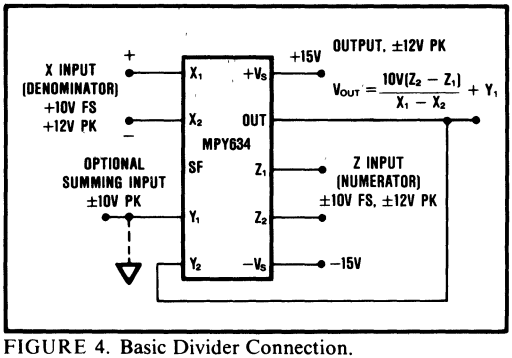


FIGURE 4. Basic Divider Connection.

SQUARE-ROOTER

A square-rooter connection is shown in Figure 5. Input voltage is limited to one polarity (positive for the connection shown). The diode prevents circuit latch-up should the input go negative. The circuit can be configured for negative input and positive output by reversing the polarity of both the X and Y inputs. The output polarity can be reversed by reversing the diode and X input polarity. A load resistance of approximately 10kΩ must be provided. Trimming for improved accuracy would be accomplished at the Z input.

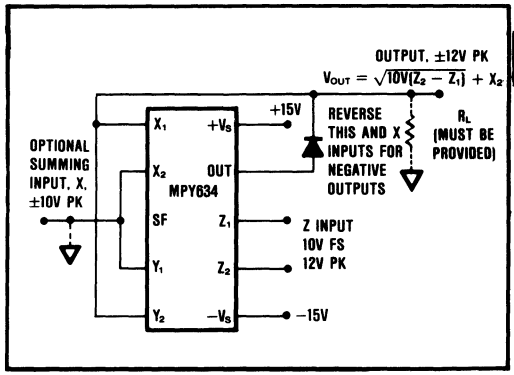


FIGURE 5. Square-Rooter Connection.

APPLICATIONS

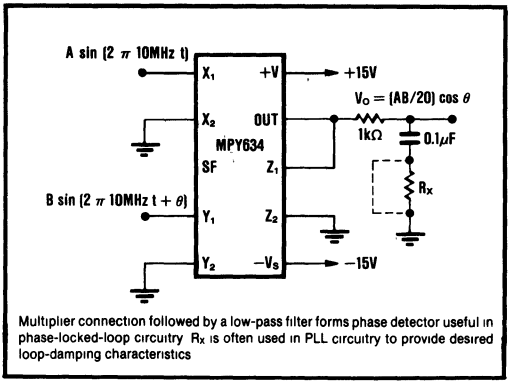


FIGURE 6. Phase Detector.

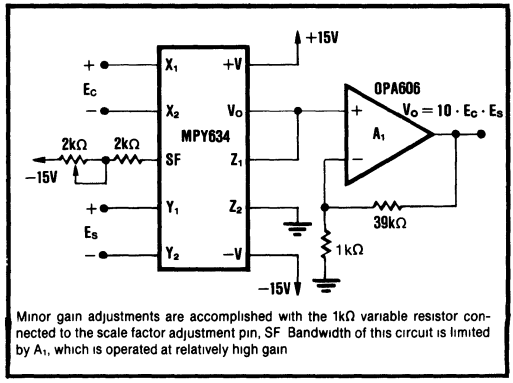
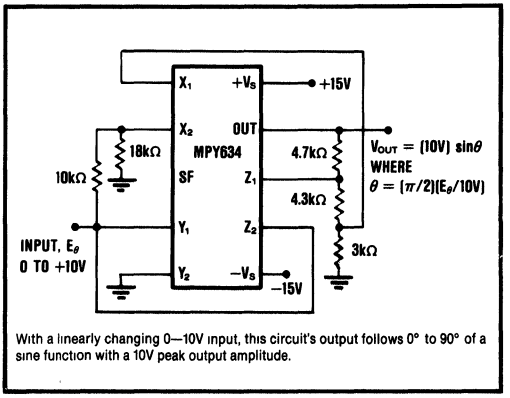
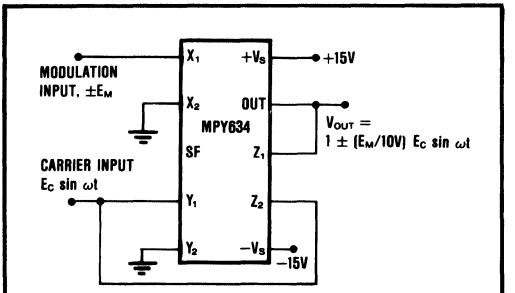


FIGURE 7. Voltage-Controlled Amplifier.



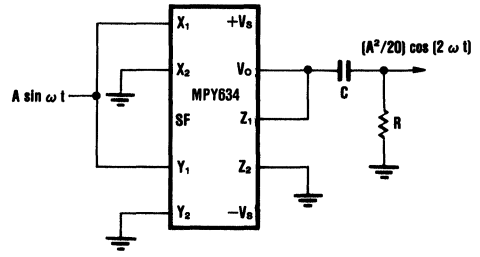
With a linearly changing 0—10V input, this circuit's output follows 0° to 90° of a sine function with a 10V peak output amplitude.

FIGURE 8. Sine-Function Generator.

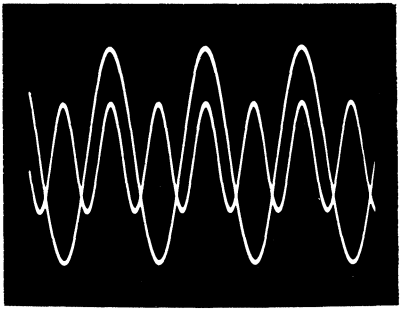


By injecting the input carrier signal into the output through connection to the Z_2 input, conventional amplitude modulation is achieved. Amplification can be achieved by use of the SF pin, or Z attenuator (at the expense of bandwidth)

FIGURE 9. Linear AM Modulator.



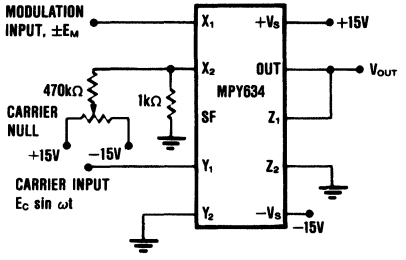
Squaring a sinusoidal input creates an output frequency of twice that of the input. The DC output component is removed by AC-coupling the output.



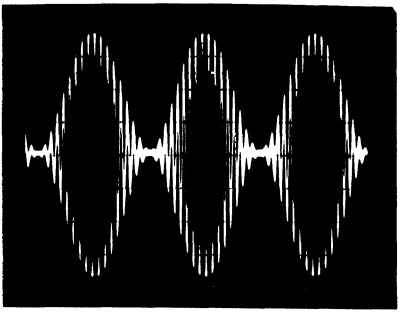
FREQUENCY DOUBLER

INPUT SIGNAL: 20Vp-p, 200kHz
OUTPUT SIGNAL: 10Vp-p, 400kHz

FIGURE 10. Frequency Doubler.



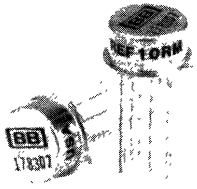
The basic multiplier connection performs balanced modulation. Carrier rejection can be improved by trimming the offset voltage of the modulation input. Better carrier rejection above 2MHz is typically achieved by interchanging the X and Y inputs (carrier applied to the X input).



CARRIER: f_C = 2MHz, AMPLITUDE = 1Vrms
SIGNAL: f_S = 120kHz, AMPLITUDE = 10V peak

FIGURE 11. Balanced Modulator.

BURR-BROWN®



REF10

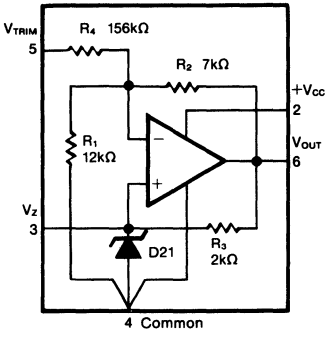
Precision VOLTAGE REFERENCE

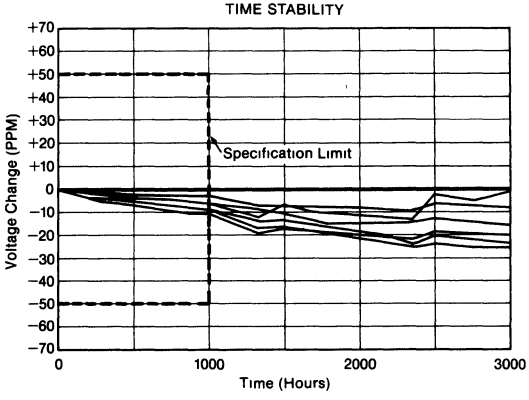
FEATURES

- +10.00V OUTPUT
- HIGH ACCURACY, ±0.005V untrimmed
- VERY-LOW DRIFT, 1ppm/°C max
- EXCELLENT STABILITY, 10ppm/1000hrs typ
- LOW NOISE, 6μV, p-p typ. 0.1Hz to 10Hz
- WIDE SUPPLY RANGE, up to 35V

APPLICATIONS

- PRECISION CALIBRATED VOLTAGE STANDARD
- TRANSDUCER EXCITATION
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETERS
- TEST EQUIPMENT





DESCRIPTION

The REF10 is a precision voltage reference which provides a +10.00V output. The drift is laser-trimmed to 1ppm/°C max (KM grade) over the full specification range. This is in contrast to some references which guarantee drift over a limited portion of their specification temperature range. The REF10 achieves its precision without a heater. This results in low quiescent current, fast warm-up, excellent stability, and low noise.

The output can be adjusted with minimal effect on drift or stability. Single supply operation over 13.5V to 35V supply range and excellent overall specifications make the REF10 an ideal choice for the most demanding applications such as precision system standards, D/A and A/D references, transducer excitation etc.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-528A

SPECIFICATIONS

ELECTRICAL

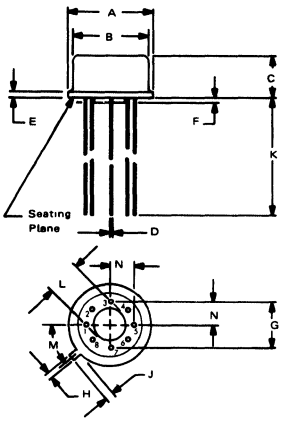
At T_A = +25°C and +15VDC power supply unless otherwise noted.

PARAMETER	CONDITION	REF10JM/KM/RM/SM MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE					
Initial	T_A = +25°C	9.995	10.000	10.005	V
Trim Range[1]		−0.100		+0.250	V
vs Temperature[2] KM	0°C to +70°C			1	ppm/°C
JM	0°C to +70°C			3	ppm/°C
SM	−55°C to +125°C			3	ppm/°C
RM	−55°C to +125°C			6	ppm/°C
vs Supply (line regulation)	V_{CC} = 13.5 to 35V		0.001	0.002	%/V
vs Output Current (load regulation)	I_L = 0 to ±10mA		0.001	0.002	%/mA
vs Time[3]	T_A = +25°C		10	±50	ppm/1000 hrs
NOISE	0.1Hz to 10Hz		6	25	µV p-p
OUTPUT CURRENT	Source or Sink	±10			mA
INPUT VOLTAGE RANGE		13.5		35	V
QUIESCENT CURRENT	I_{OUT} = 0		4.5	6	mA
WARM-UP TIME	To 0.1%		10		µs
TEMPERATURE RANGE					
Specification JM, KM		0		+70	°C
RM, SM		−55		+125	°C
Operating JM, KM		−25		+85	°C
RM, SM		−55		+125	°C
Storage		−65		+125	°C

NOTES (1) Trimming the offset voltage will affect the drift slightly. See Installation and Operating Instructions for details (2) The "box method" is used to specify output voltage drift vs temperature. See the Discussion of Performance section. (3) Sample tested with power applied continuously.

MECHANICAL

TO-99 PACKAGE



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane

Pin numbers shown for reference only. Numbers not marked on package

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	335	370	8 51	9 40
B	305	335	7 75	8 51
C	165	185	4 19	4 70
D	016	.021	0 41	0 53
E	010	040	0 25	1 02
F	010	040	0 25	1 02
G	200 BASIC		5 08 BASIC	
H	.028	034	0 71	0 86
J	029	045	0 74	1 14
K	.500	--	12 7	--
L	110	160	2 79	4 06
M	45° BASIC		45° BASIC	
N	095	105	2 41	2 67

WEIGHT: 1 gram

ORDERING INFORMATION

REF10 X M

Basic Model Number

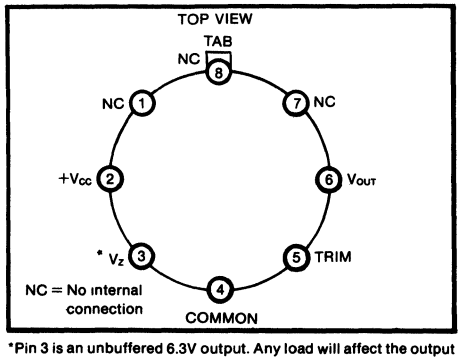
Performance Grade Code
- J, K: −0°C to +70°C
- R, S: −55°C to +125°C

Package Code
- TO-99

ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V
Power Dissipation at +25°C	200mW
Operating Temperature Range	
REF10JM/KM	−25°C to +85°C
REF10RM/SM	−55°C to +125°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Short-Circuit Protection at +25°C to Common or +15VDC	Continuous

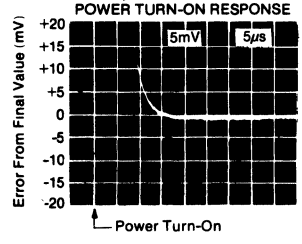
PIN CONFIGURATION



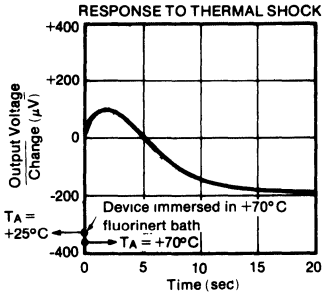
*Pin 3 is an unbuffered 6.3V output. Any load will affect the output voltage and drift. A load of 1µA on pin 3 will typically change the output voltage by 50µV and the drift by 0.1ppm/°C.

TYPICAL PERFORMANCE CURVES

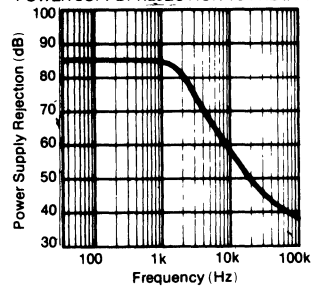
POWER TURN-ON RESPONSE



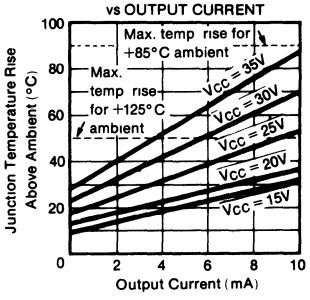
RESPONSE TO THERMAL SHOCK



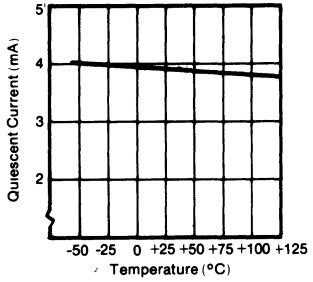
POWER SUPPLY REJECTION VS FREQUENCY



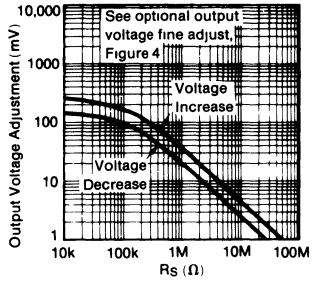
JUNCTION TEMPERATURE RISE vs OUTPUT CURRENT



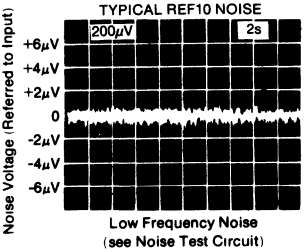
QUIESCENT CURRENT VS TEMPERATURE



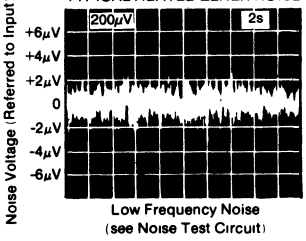
OUTPUT VOLTAGE ADJUSTMENT vs Rs



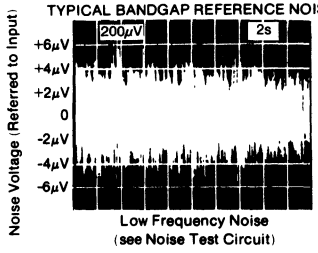
TYPICAL REF10 NOISE

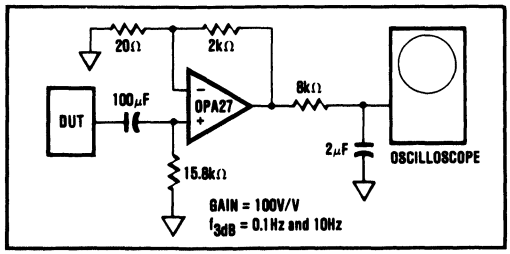


TYPICAL HEATED ZENER NOISE



TYPICAL BANDGAP REFERENCE NOISE





NOISE TEST CIRCUIT

THEORY OF OPERATION

The following discussion refers to the diagram on the first page.

In operation, approximately 6.3V is applied to the noninverting input of op amp A_1 by zener diode DZ_1. This voltage is amplified by A_1 to produce the 10.00V output. The gain is determined by R_1 and R_2: $G = (R_1 + R_2)/R_1$. R_1 and R_2 are actively laser-trimmed to produce an exact 10.00V output. The zener operating current is derived from the regulated output voltage through R_3. This feedback arrangement provides closely regulated zener current. R_3 is actively laser-trimmed to set the zener current to a level which results in low drift at the output of A_1. R_4 allows user-trimming of the output voltage by providing for a small external adjustment of amplifier gain. Since the TCR of R_4 closely matches the TCR of the gain setting resistors, the voltage trim has minimal effect on the drift of the reference.

DISCUSSION OF PERFORMANCE

The REF10 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry—the "butterfly method" and the "box method." The REF10 is specified with the more commonly used box method. The "box" is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

For the REF10 each J and K unit is tested at temperatures of 0°C, +25°C, +50°C, and +70°C and each R and S unit is tested at −55°C, −25°C, 0°C, +25°C, +50°C, +75°C, +100°C and +125°C. The minimum and maximum test voltages must meet this condition:

$$\left[\frac{(V_{OUT\ max} - V_{OUT\ min})/10V}{T_{high} - T_{low}}\right] \times 10^6 \leq \text{drift specification}$$

This assures the user that the variations of output voltage that occur as the temperature changes within the specification range T_{low} to T_{high} will be contained within a box whose diagonal has a slope equal to the maximum specified drift. Since the shape of the actual drift curve is not known, the vertical position of the box is not exactly known either. It is, however, bounded by $V_{Upper\ Bound}$ and $V_{Lower\ Bound}$ (see Figure 1).

Figure 1 uses the REF10KM as an example. It has a drift specification of 1ppm/°C maximum and a specification temperature range of 0°C to +70°C. The "box" height (V_1 to V_2) is 700μV and upper bound and lower bound voltages are a maximum of 700μV away from the voltage at +25°C.

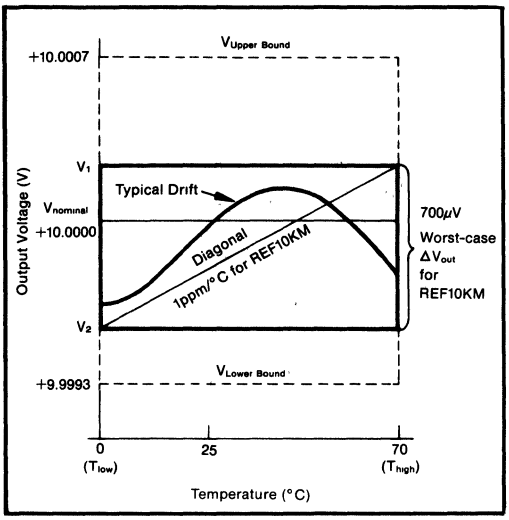


FIGURE 1. REF10KM Output Voltage Drift.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF10. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated being sure to minimize interconnection resistances.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figure 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.01ppm/°C

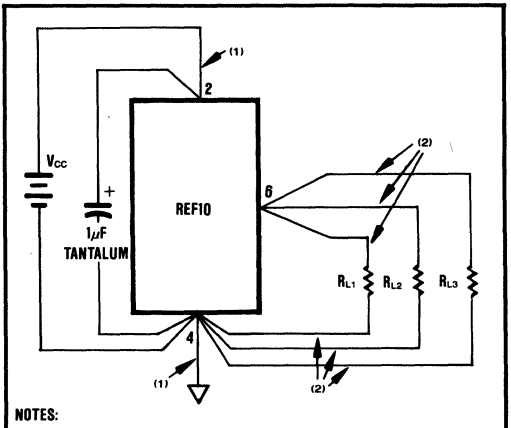


FIGURE 2. REF10 Installation.

per mV of trimmed voltage. In the circuit in Figure 3 any mismatch in TCR between the two sections of the potentiometer will also affect drift but the effect of the ΔTCR is reduced by a factor of 40 by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a range of approximately +250mV to −100mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R_S and the internal resistors can introduce some slight drift. This effect is minimized if R_S is kept significantly larger than the 156kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.

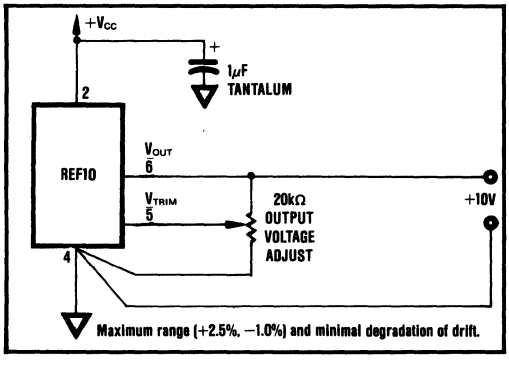


FIGURE 3. REF10 Optional Output Voltage Adjust.

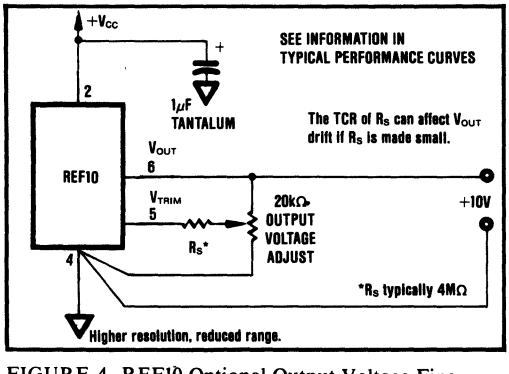


FIGURE 4. REF10 Optional Output Voltage Fine Adjust.

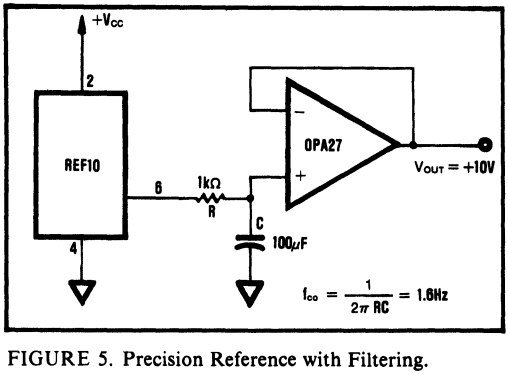


FIGURE 5. Precision Reference with Filtering.

APPLICATION INFORMATION

High accuracy, extremely-low drift, and small size make the REF10 ideal for demanding instrumentation and system voltage reference applications. Since no heater is required, low power supply current designs are readily achievable. Also the REF10 has lower output noise and much faster warm-up times than heated references, permitting high precision without extra power or additional supplies. It should be considered that operating any integrated circuit at an elevated temperature will reduce its MTTF.

A variety of application circuits are shown in Figures 5 through 11.

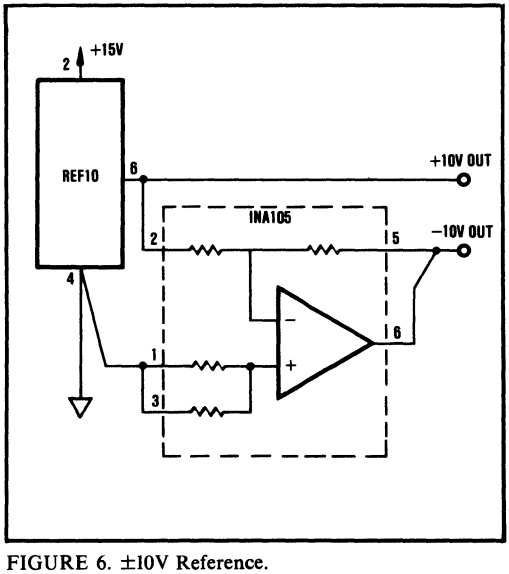


FIGURE 6. ±10V Reference.

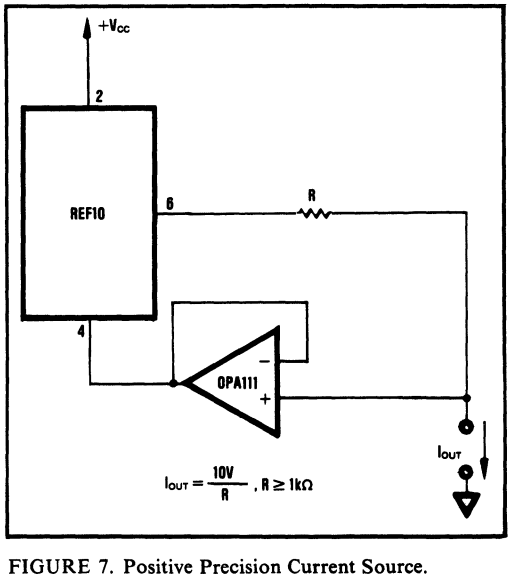


FIGURE 7. Positive Precision Current Source.

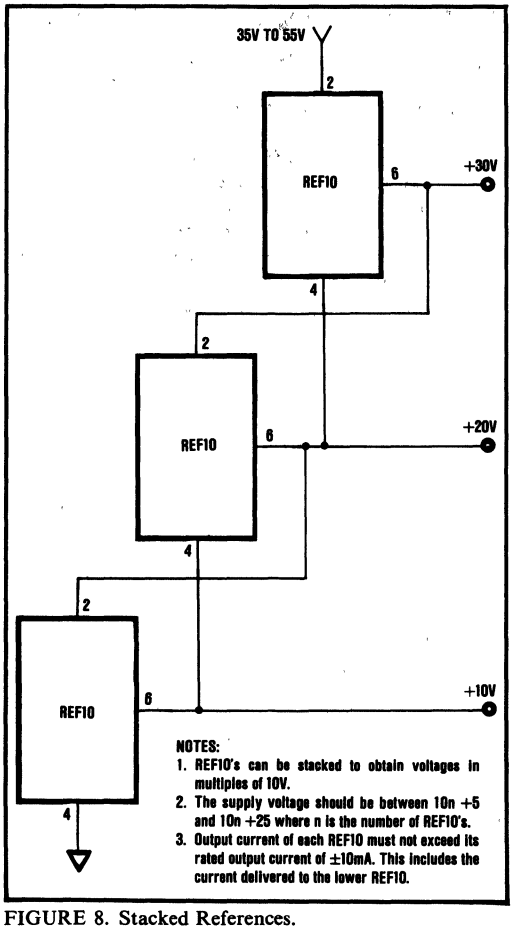


FIGURE 8. Stacked References.

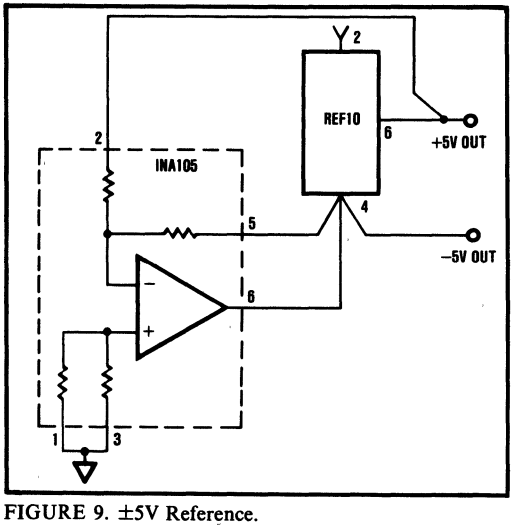


FIGURE 9. ±5V Reference.

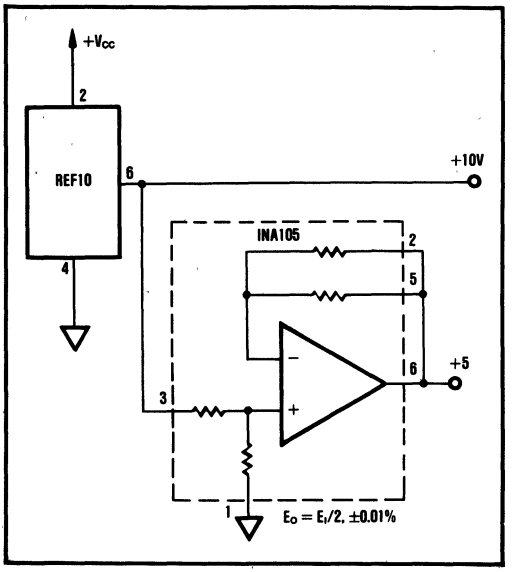


FIGURE 10. +5V and +10V Reference.

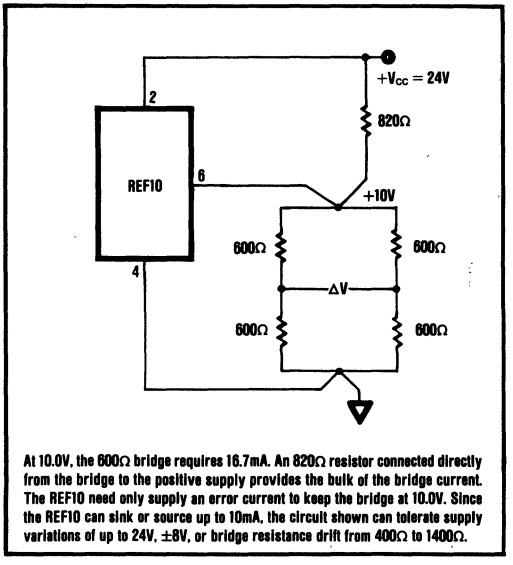
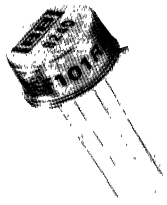


FIGURE 11. +10V Reference with Output Current Boost Using a Resistor to Drive a 600Ω Bridge.

BURR-BROWN®



REF101

Precision VOLTAGE REFERENCE

FEATURES

- +10.00V OUTPUT
- HIGH ACCURACY, ±0.005V
- VERY LOW DRIFT, 1ppm/°C max
- EXCELLENT STABILITY, 50ppm/1000hrs.
- LOW NOISE, 6μV, p-p typ, 0.1Hz to 10Hz
- WIDE SUPPLY RANGE, up to 35V
- LOW QUIESCENT CURRENT, 6mA max
- USEFUL MATCHED RESISTOR PAIR INCLUDED

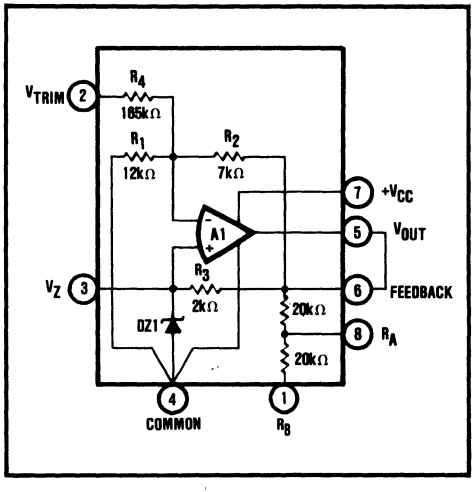
APPLICATIONS

- PRECISION CALIBRATED VOLTAGE STANDARD
- TRANSDUCER EXCITATION
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETERS
- TEST EQUIPMENT

DESCRIPTION

The REF101 is a precision voltage reference which provides a +10.00V output. The drift is laser-trimmed to 1ppm/°C max (KM grade) over the full specification range. This is in contrast to some references which guarantee drift over a limited portion of their specification temperature range. The REF101 achieves its precision without a heater. This results in low quiescent current (4.5mA typ), fast warm-up (1msec to 0.1%), excellent stability (50ppm/1000hrs typ), and low noise (25μV, p-p max, 0.1Hz to 10Hz).

The output can be adjusted with minimal effect on drift or stability. Additionally, the REF101 contains a matched pair of user-accessible precision 20kΩ resistors which are useful in a variety of applications. Single supply operation over 13.5V to 35V supply range and excellent overall specifications make the REF101 an ideal choice for the most demanding applications such as precision system standards, D/A and A/D references, transducer excitation etc.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-485B

SPECIFICATIONS

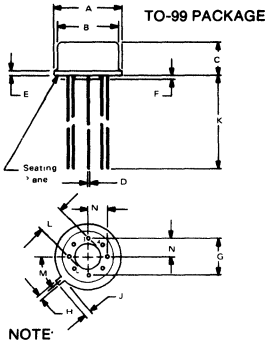
ELECTRICAL

At T_A = +25°C and +15VDC power supply unless otherwise noted.

PARAMETER	CONDITION	REF101JM/KM/RM/SM MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE					
Initial	T_A = +25°C	9 995	10 000	10.005	V
Trim Range(1)		-0.100		+0 250	V
vs Temperature(2)					
KM	0°C to +70°C			1	ppm/°C
JM	0°C to +70°C			2	ppm/°C
SM	-55°C to +125°C			3	ppm/°C
RM	-55°C to +125°C			6	ppm/°C
vs Supply (line regulation)	V_{CC} = 13 5 to 35V		0 001	0 002	%/V
vs Output Current					
(load regulation)	I_L = 0 to ±10mA		0 001	0.002	%/mA
vs Time	T_A = +25°C		50		ppm/1000 hrs
NOISE	0.1Hz to 10Hz		6	25	µV p-p
OUTPUT CURRENT	Source or Sink	±10			mA
INPUT VOLTAGE RANGE		13.5		35	V
QUIESCENT CURRENT	I_{OUT} = 0		4.5	6	mA
WARM-UP TIME	To 0 1%		10		µsec
UNCOMMITTED RESISTORS					
Resistance			20		kΩ
Match			±0.01	±0.05	%
TCR			50		ppm/°C
TCR Tracking			2		ppm/°C
TEMPERATURE RANGE					
Specification					
JM, KM		0		+70	°C
RM, SM		-55		+125	°C
Operating					
JM, KM		-25		+85	°C
RM, SM		-55		+125	°C
Storage		-65		+125	°C

NOTES.
1. Trimming the offset voltage will affect the drift slightly. See Installation and Operating Instructions for details.
2. The "box method" is used to specify output voltage drift vs temperature. See the Discussion of Performance section.

MECHANICAL



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers not marked on package.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	335	370	8 51	9 40
B	305	335	7 75	8 51
C	165	185	4 19	4 70
D	016	021	0 41	0 53
E	010	040	0 25	1 02
F	010	040	0 25	1 02
G	200 BASIC		5 08 BASIC	
H	028	034	0 71	0 86
J	029	045	0 74	1 14
K	500	-	12 7	
L	110	160	2 79	4 06
M	45° BASIC		45° BASIC	
N	095	105	2 41	2 67

WEIGHT: 1 gram
ORDER: REF101JM, REF101KM
REF101RM, REF101SM

ORDERING INFORMATION

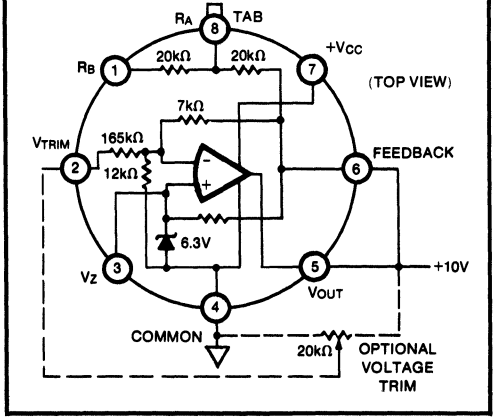
REF101 X M

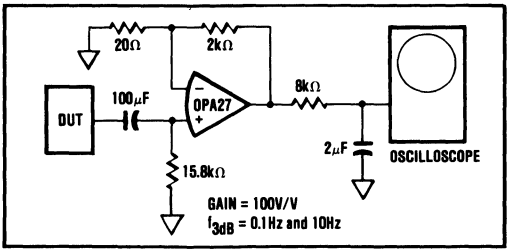
Basic Model Number
Performance Grade Code
J, K -25°C to +85°C
R, S -55°C to +125°C
Package Code
TO-99

ABSOLUTE MAXIMUM RATINGS

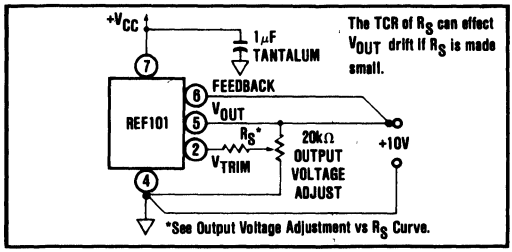
Input Voltage 40V
Power Dissipation at +25°C 200mW
Operating Temperature Range
REF101JM/KM ..... -25°C to +85°C
REF101RM/SM ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +125°C
Lead Temperature (soldering, 10sec) ..... +300°C
Short-Circuit Protection at +25°C
To Common or +15VDC ..... Continuous

PIN CONFIGURATION





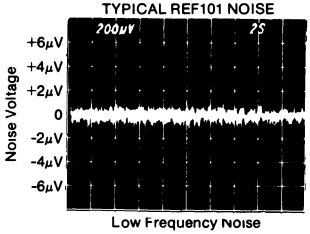
NOISE TEST CIRCUIT



OPTIONAL OUTPUT VOLTAGE FINE ADJUSTMENT CIRCUIT.

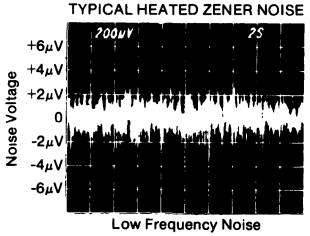
TYPICAL PERFORMANCE CURVES

TYPICAL REF101 NOISE



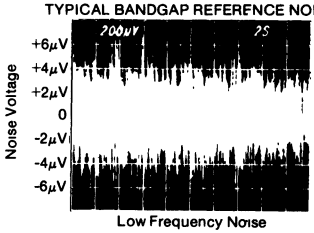
Low Frequency Noise
(see Noise Test Circuit)

TYPICAL HEATED ZENER NOISE



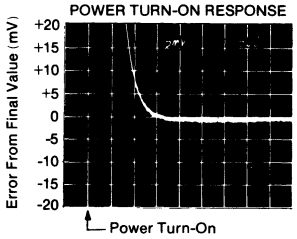
Low Frequency Noise
(see Noise Test Circuit)

TYPICAL BANDGAP REFERENCE NOISE

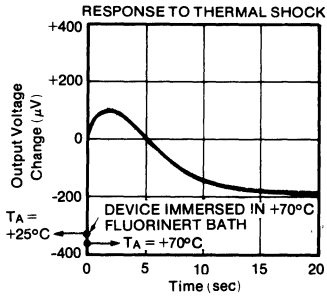


Low Frequency Noise
(see Noise Test Circuit)

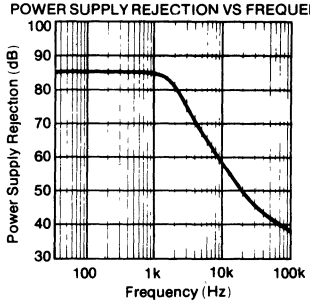
POWER TURN-ON RESPONSE



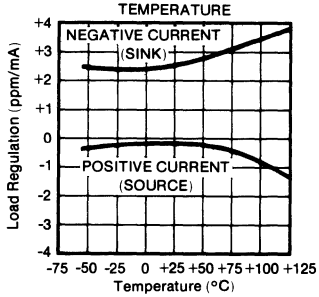
RESPONSE TO THERMAL SHOCK



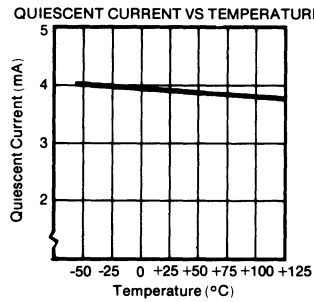
POWER SUPPLY REJECTION VS FREQUENCY



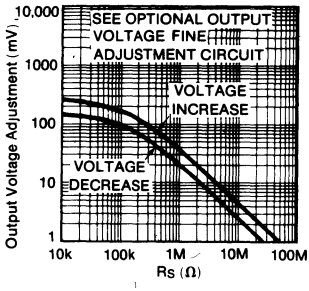
LOAD REGULATION VS TEMPERATURE



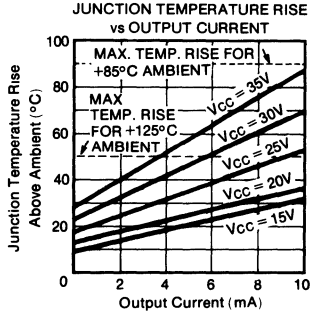
QUIESCENT CURRENT VS TEMPERATURE



OUTPUT VOLTAGE ADJUSTMENT vs RS



JUNCTION TEMPERATURE RISE vs OUTPUT CURRENT



THEORY OF OPERATION

The following discussion refers to the diagram on the first page.

In operation, approximately 6.3V is applied to the noninverting input of op amp A_1 by zener diode DZ_1. This voltage is amplified by A_1 to produce the 10.00V output. The gain is determined by R_1 and R_2: $G = (R_1 + R_2)/R_1$. R_1 and R_2 are actively laser-trimmed to produce an exact 10.00V output. The zener operating current is derived from the regulated output voltage through R_3. This feedback arrangement provides closely regulated zener current. R_3 is actively laser-trimmed to set the zener current to a level which results in low drift at the output of A_1. The adjustment of output voltage and zener current is interactive and several iterations may be used to achieve the desired results. R_4 allows user-trimming of the output voltage by providing for a small external adjustment of amplifier gain. Since the TCR of R_4 closely matches the TCR of the gain setting resistors, the voltage trim has minimal effect on the drift of the reference.

DISCUSSION OF PERFORMANCE

The REF101 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry — the "butterfly method" and the "box method". Neither of these methods is entirely satisfactory in cases where the drift versus temperature is relatively nonlinear as is the case with most voltage references. The REF101 is specified with the more commonly used box method. The "box" is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

For the REF101 each J and K unit is tested at temperatures of 0°C, +25°C, +50°C, and +70°C and each R and S unit is tested at -55°C, -25°C, 0°C, +25°C, +50°C, +75°C, +100°C and +125°C. The minimum and maximum test voltages must meet this condition.

$$\left[\frac{(V_{OUT\ max} - V_{OUT\ min})/10V}{T_{high} - T_{low}}\right] \times 10^6 \leqslant \text{drift specification}$$

This assures the user that the variations of output voltage that occur as the temperature changes within the specification range T_{low} to T_{high} will be contained within a box whose diagonal has a slope equal to the maximum specified drift. Since the shape of the actual drift curve is not known, the vertical position of the box is not exactly known either. It is, however, bounded by $V_{Upper\ Bound}$ and $V_{Lower\ Bound}$ (see Figure 1).

Figure 1 uses the REF101KM as an example. It has a drift specification of 1ppm/°C maximum and a specification temperature range of 0°C to +70°C. The "box" height (V_1 to V_2) is 700μV and upper bound and lower bound voltages are a maximum of 700μV away from the voltage at +25°C.

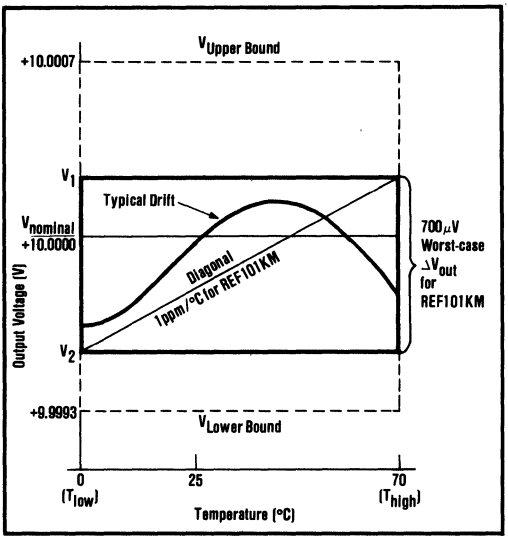


FIGURE 1. REF101KM Output Voltage Drift.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF101. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated being sure to minimize interconnection resistances.

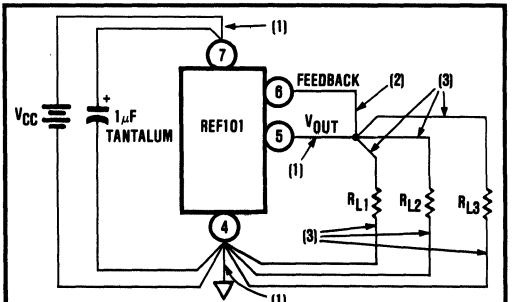


FIGURE 2. REF101 Basic Circuit Connection.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.01ppm/°C per mV of trimmed voltage. In the circuit in Figure 3 any mismatch in TCR between the two sections of the potentiometer will also affect drift but the effect of the ΔTCR is reduced by a factor of 40 by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a range of approximately +250mV to -100mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R_S and the internal resistors can introduce some slight drift. This effect is minimized if R_S is kept significantly larger than the 165kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.

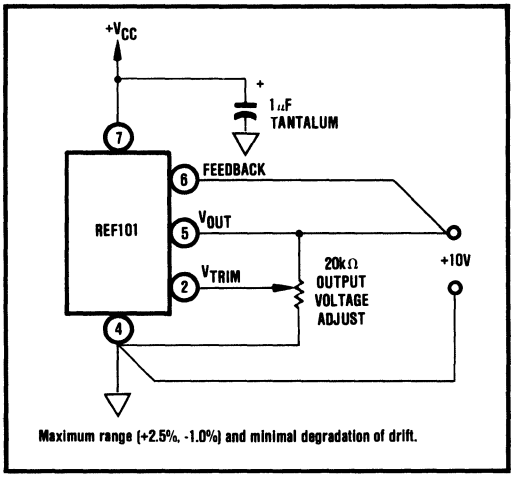


FIGURE 3. REF101 Optional Output Voltage Adjust.

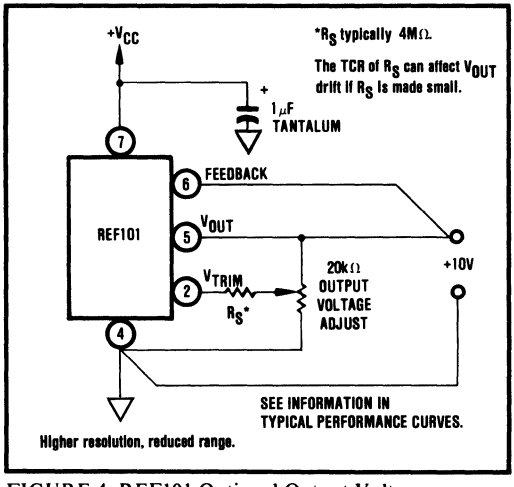


FIGURE 4. REF101 Optional Output Voltage Fine Adjust.

APPLICATION INFORMATION

High accuracy, extremely-low drift, and small size make the REF101 ideal for demanding instrumentation and system voltage reference applications. Since no heater is required, low power supply current designs are readily achievable. Also the REF101 has lower output noise and much faster warm-up times (1msec to 0.1%) than heated references, permitting high precision without extra power from additional supplies. It should be considered that operating any integrated circuit at an elevated temperature will reduce its MTTF.

A variety of application circuits are shown in Figures 5 through 19.

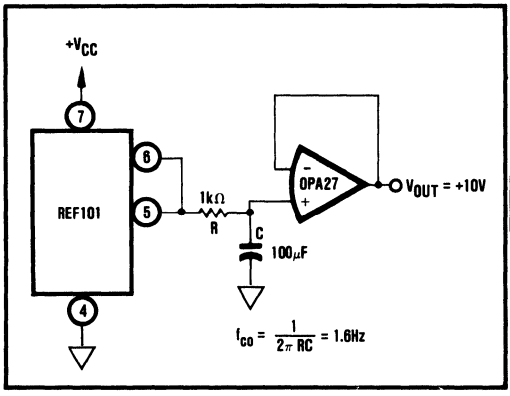


FIGURE 5. Precision Reference with Filtering.

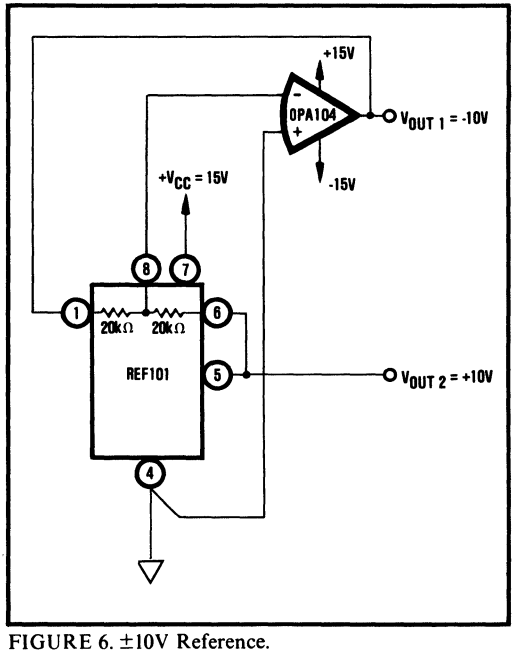


FIGURE 6. ±10V Reference.

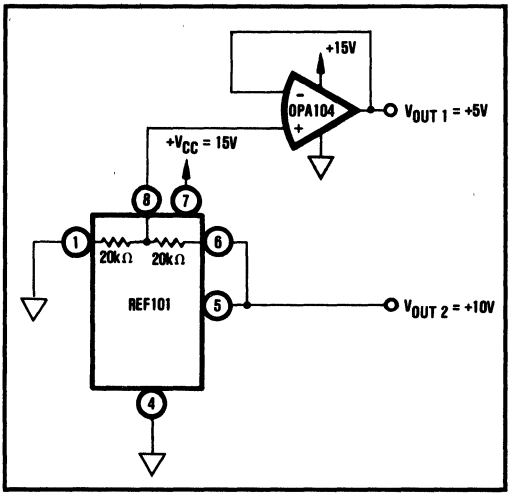


FIGURE 7. +10V and +5V Reference.

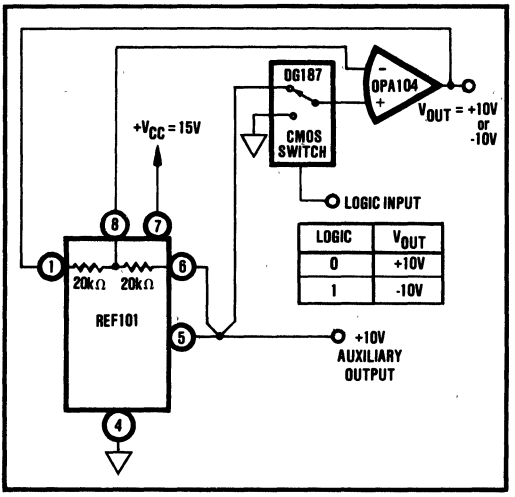


FIGURE 9. Digitally-Controlled Bipolar Precision Reference.

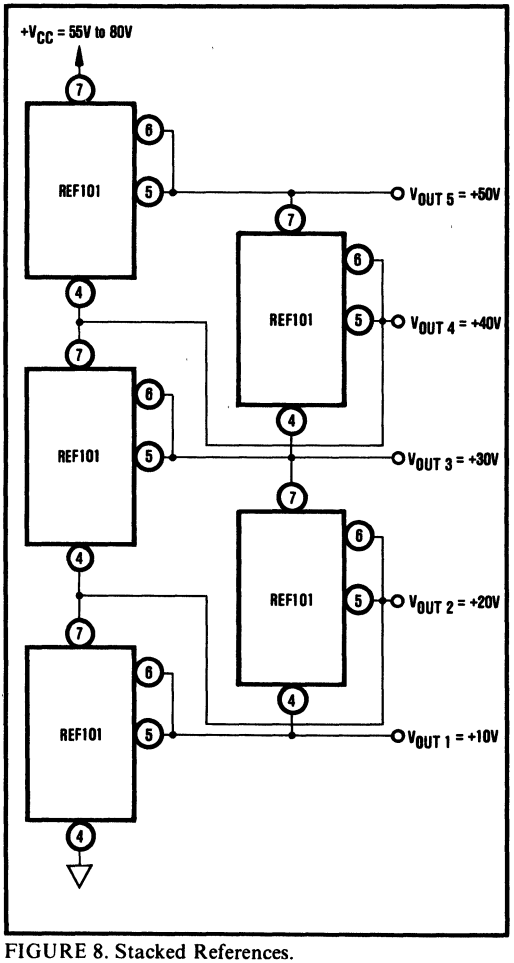


FIGURE 8. Stacked References.

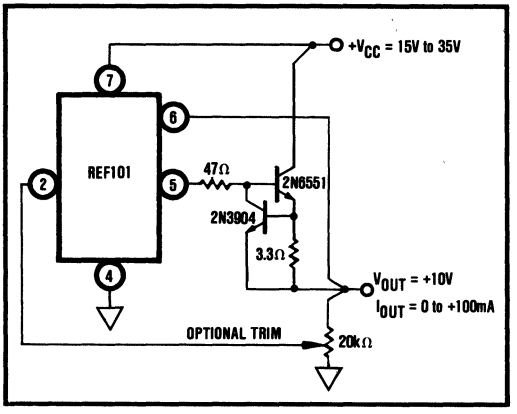


FIGURE 10. +10V Reference with Boosted Output Current to 100mA.

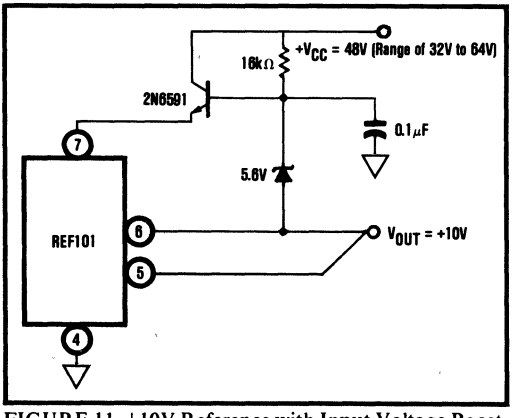


FIGURE 11. +10V Reference with Input Voltage Boost for 48V Operation.

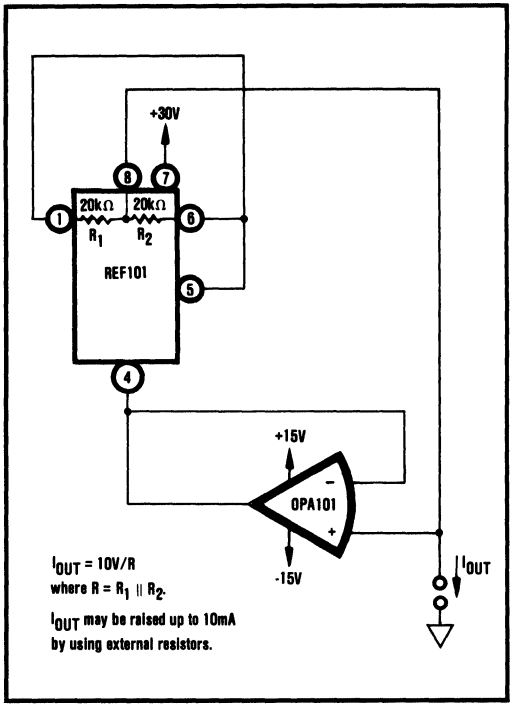


FIGURE 12. Positive Precision 1mA Current Source.

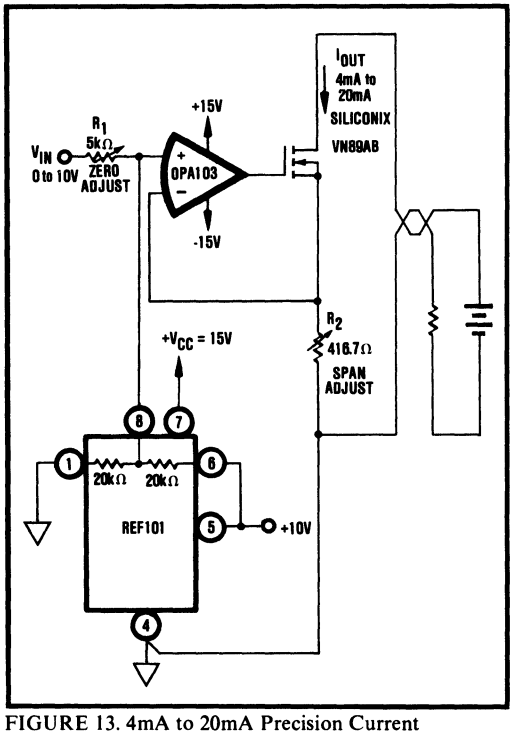


FIGURE 13. 4mA to 20mA Precision Current Transmitter.

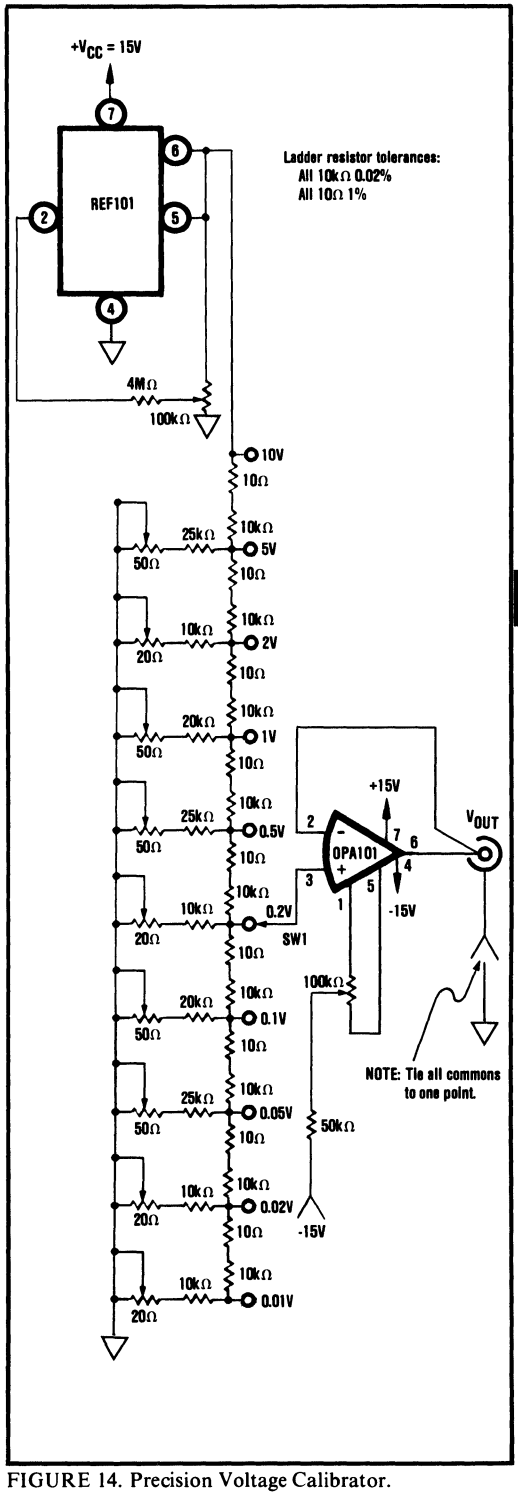


FIGURE 14. Precision Voltage Calibrator.

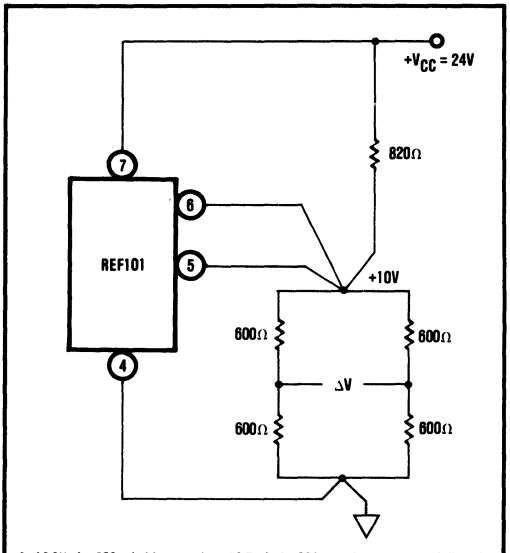


FIGURE 15. +10V Reference with Output Current Boost Using a Resistor to Drive a 600Ω Bridge.

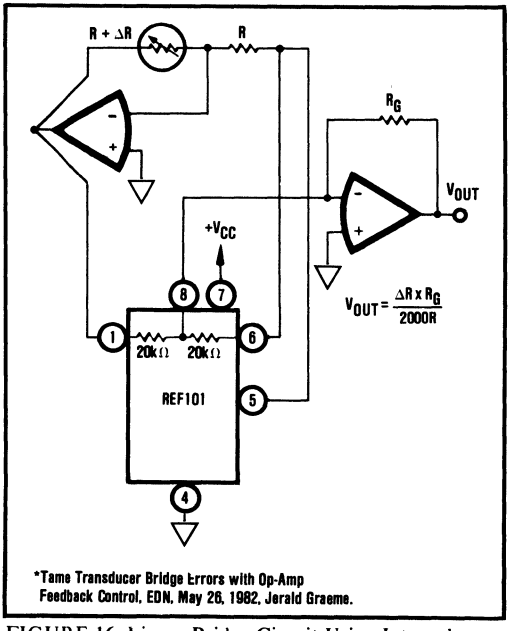


FIGURE 16. Linear Bridge Circuit Using Internal Precision Resistors of the REF101 as the Bridge Completion Network.

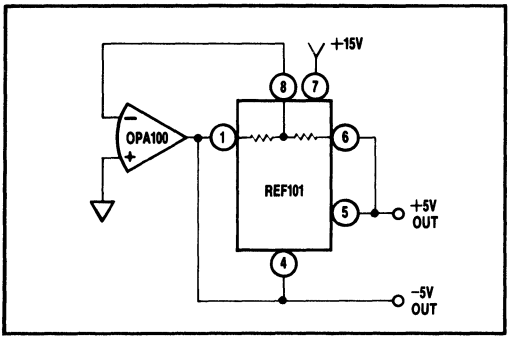


FIGURE 17. ±5V Reference.

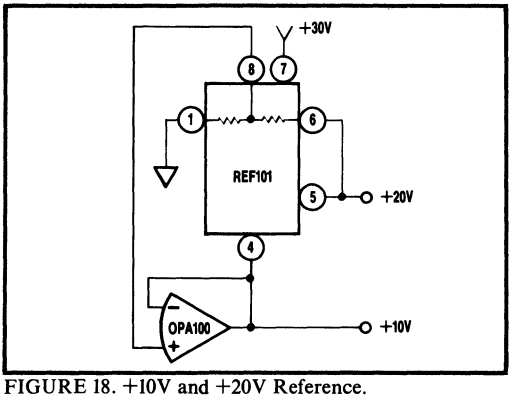


FIGURE 18. +10V and +20V Reference.

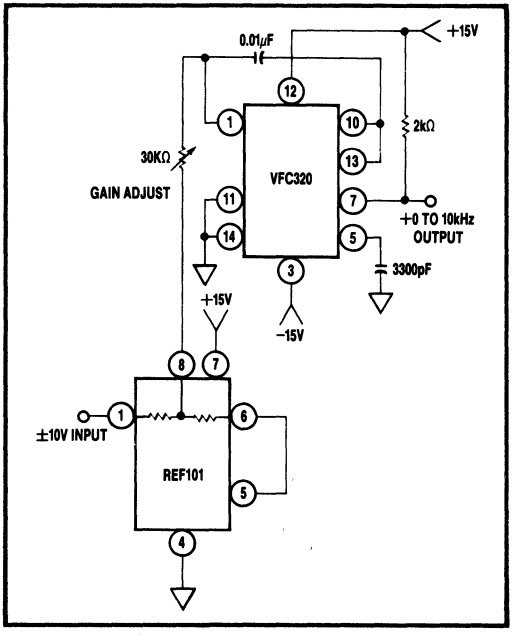
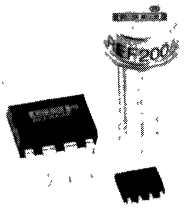


FIGURE 19. Bipolar Input Voltage to Frequency Converter.

BURR-BROWN®



REF200

DUAL CURRENT SOURCE

FEATURES

- COMPLETELY FLOATING: No Common Connection
- HIGH ACCURACY: 100µA ±0.5%
- LOW TEMPERATURE COEFFICIENT: ±25ppm/°C
- WIDE VOLTAGE COMPLIANCE: 2.5V TO 40V
- ALSO INCLUDES CURRENT MIRROR

APPLICATIONS

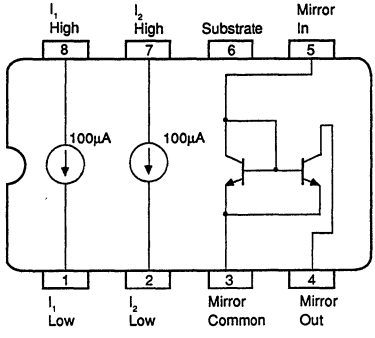
- SENSOR EXCITATION
- BIASING CIRCUITRY
- OFFSETTING CURRENT LOOPS
- LOW VOLTAGE REFERENCES
- CHARGE-PUMP CIRCUITRY
- HYBRID MICROCIRCUITS

DESCRIPTION

The REF200 combines three circuit building-blocks on a single monolithic chip—two 100µA current sources and a current mirror. The sections are dielectrically isolated, making them completely independent. The performance of each section is individually measured and laser-trimmed to achieve high accuracy with low cost.

The sections can be pin-strapped for currents of 50µA, 100µA, 200µA, 300µA or 400µA. External circuitry can be used to obtain virtually any current. These and many other circuit techniques are shown in the Applications section of this Data Sheet.

The REF200 is available in plastic 8-pin mini-DIP, TO-99, and SOIC packages. Die are also available.



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PDS-851

SPECIFICATIONS

ELECTRICAL

T_A = 25°C, V_S = 15V unless otherwise noted.

		REF200AM, AP, AU			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**UNITS**
CURRENT SOURCES					
Current Accuracy			±0.1	±0.5	%
Current Match			±0.05	±0.5	%
Temperature Drift	Specified Temp Range		25		ppm/°C
Output Impedance	2.5V to 40V	20	100		MΩ
	3.5V to 30V	200	500		MΩ
Noise	BW = 0.1Hz to 10Hz		1		nA p–p
	f = 10kHz		20		pA/√Hz
Voltage Compliance (1%)	T_{MIN} to T_{MAX}		See Curves		
Capacitance			10		pF
CURRENT MIRROR	I = 100µA unless otherwise noted.				
Gain		0.995	1	1.005	
Temperature Drift			25		ppm/°C
Impedance (output)	2V to 40V	40	100		MΩ
Nonlinearity	I = 0µA to 250µA		0.05		%
Input Voltage			1.4		V
Output Compliance Voltage			See Curves		
Frequency Response (–3dB)	Transfer		5		MHz
TEMPERATURE RANGE					
Specification					
AP, AU, AM		–25		+85	°C
Operating					
AP, AU		–40		+85	°C
AM		–55		+125	°C
Storage					
AP, AU,		–40		+125	°C
AM		–60		+150	°C

AP AND AU SPECIFICATIONS ARE PRELIMINARY AND SUBJECT TO CHANGE

ORDERING INFORMATION

Model [1]	Package	Temperature Range
REF200AM	TO-99	–25°C to +85°C
REF200AP	Plastic DIP	–25°C to +85°C
REF200AU	Plastic SOIC	–25°C to +85°C
BURN-IN SCREENING OPTION See text for details.		
Model [1]	**Package**	**Burn-In Temp (160h) [2]**
REF200AM-BI	TO-99	+125°C
REF200AP-BI	Plastic DIP	+85°C
REF200AU-BI	Plastic SOIC	+85°C

NOTE: (1) Grade designation "A" may not be marked. Absence of grade designation indicates A grade. (2) Or equivalent combination of time and temperature. See text.

ABSOLUTE MAXIMUM RATINGS

Applied Voltage	–6V to +40V
Reverse Current	–350µA
Voltage between any two sections	±80V
Operating Temperature	
M Package	–65°C to +150°C
P and U Packages	–40°C to +85°C
Storage Temperature	
M Package	–65°C to +150°C
P and U Packages	–40°C to +125°C

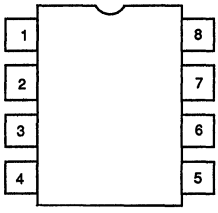
BURN-IN SCREENING

Burn-in screening is available on the REF200. Burn-in duration is 160 hours at +85°C (+125°C for M package), or at an equivalent combination of time and temperature according to the Arrhenius equation using 1eV activation energy.

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

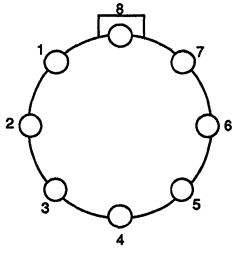
PIN CONFIGURATION

Top View — **P, U Packages**



1) I_1 Low
2) I_2 Low
3) Mirror Common
4) Mirror Output
5) Mirror Input
6) Substrate
7) I_2 High
8) I_1 High

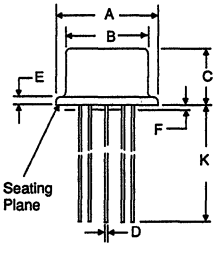
Top View — **M Package**

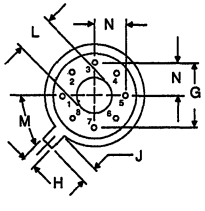


1) I_1 Low
2) I_2 Low
3) Mirror Common
4) Mirror Output
5) Mirror Input
6) Substrate
7) I_2 High
8) I_1 High

MECHANICAL

M Package — Metal TO-99

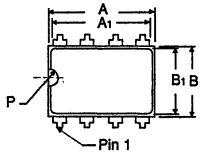


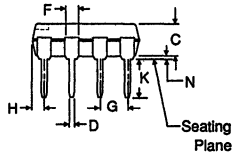


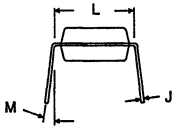
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

P Package — 8-Pin Plastic DIP





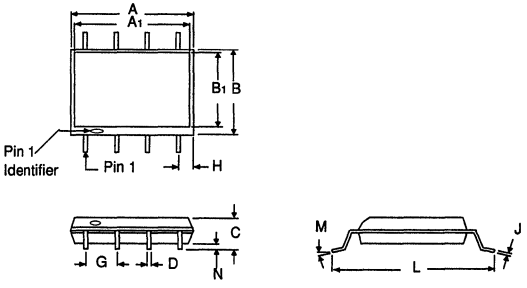


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.355	.400	9.03	10.16
A1	.340	.385	8.65	9.80
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.025	.050	0.64	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

MECHANICAL

U Package — 8-Pin SOIC



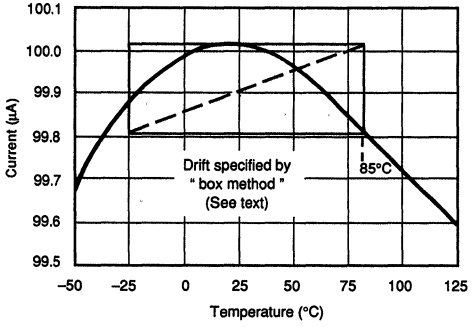
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.201	4.70	5.11
A1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B1	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

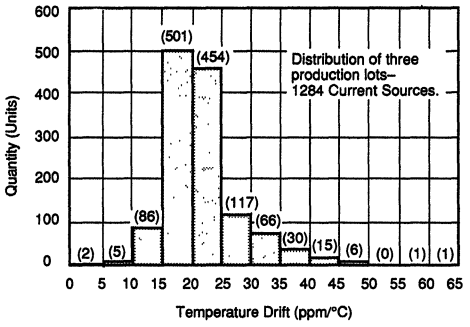
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = +15V unless otherwise noted.

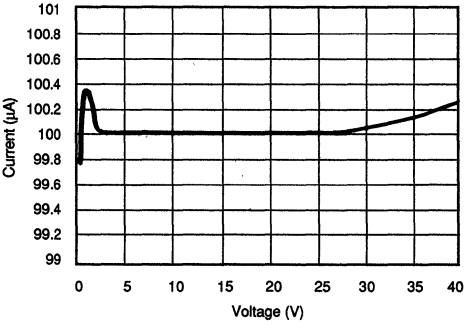
CURRENT SOURCE
TYPICAL DRIFT vs TEMPERATURE



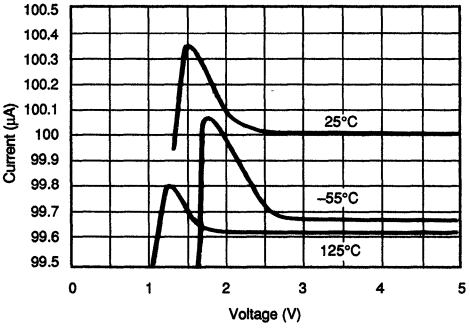
CURRENT SOURCE
TEMPERATURE DRIFT DISTRIBUTION



CURRENT SOURCE
OUTPUT CURRENT vs VOLTAGE



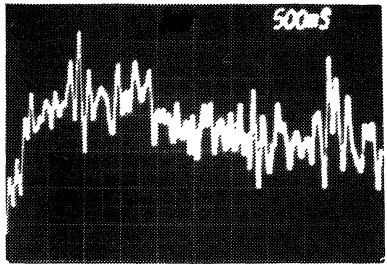
CURRENT SOURCE
OUTPUT CURRENT vs VOLTAGE



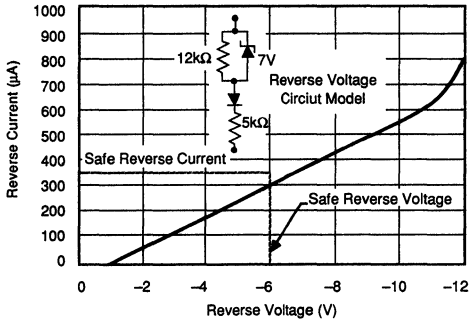
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = +15V unless otherwise noted.

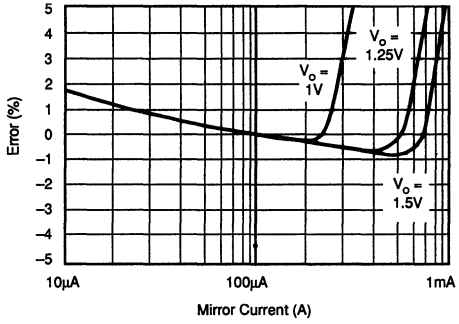
CURRENT SOURCE
CURRENT NOISE (0.1Hz to 10Hz)



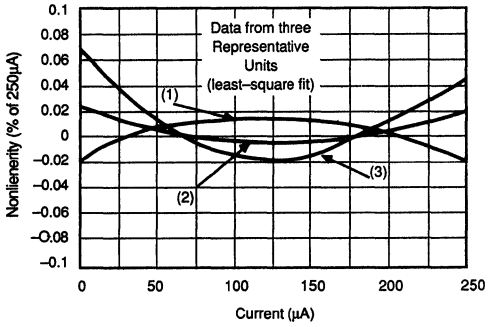
CURRENT SOURCE
REVERSE CURRENT vs REVERSE VOLTAGE



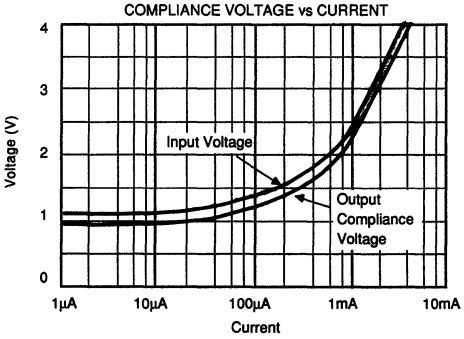
MIRROR GAIN ERROR vs CURRENT



MIRROR TRANSFER NONLINEARITY



MIRROR INPUT VOLTAGE/OUTPUT
COMPLIANCE VOLTAGE vs CURRENT



APPLICATIONS INFORMATION

The three circuit sections of the REF200 are electrically isolated from one another using a dielectrically isolated fabrication process. A substrate connection is provided (pin 6), which is isolated from all circuitry. Still, this pin should be connected to a defined circuit potential to assure that rated performance is achieved. The preferred connection is to the most positive constant potential in your system. In most analog systems this would be $+V_S$.

Although sections of the REF200 may be left unconnected, they should preferably be connected to ground or the positive power supply. Connect one or all terminals of an unused section to an appropriate node.

Drift performance is specified by the "box method," as illustrated in the Current vs Temperature plot of the typical performance curves. The upper and lower current extremes measured over temperature define the top and bottom of the box. The sides are determined by the specified temperature range of the device. The drift of the unit is the slope of the diagonal—typically 25ppm/°C from –25°C to +85°C.

If the current sources are subjected to reverse voltage, a protection diode may be required. A reverse voltage circuit model of the REF200 is shown in the Reverse Current vs Reverse Voltage Curve. If reverse voltage is limited to less than 6V *or* reverse current is limited to less than 350µA, no protection circuitry is required. A parallel diode (Figure 2a) will protect the device by limiting the reverse voltage across the current source to approximately 0.7V. In some applications, a series diode may be preferable (Figure 2b) because it allows no reverse current. This will, however, reduce the compliance voltage range by one diode drop.

Applications for the REF200 are limitless. A collection of circuits is shown to illustrate some techniques.

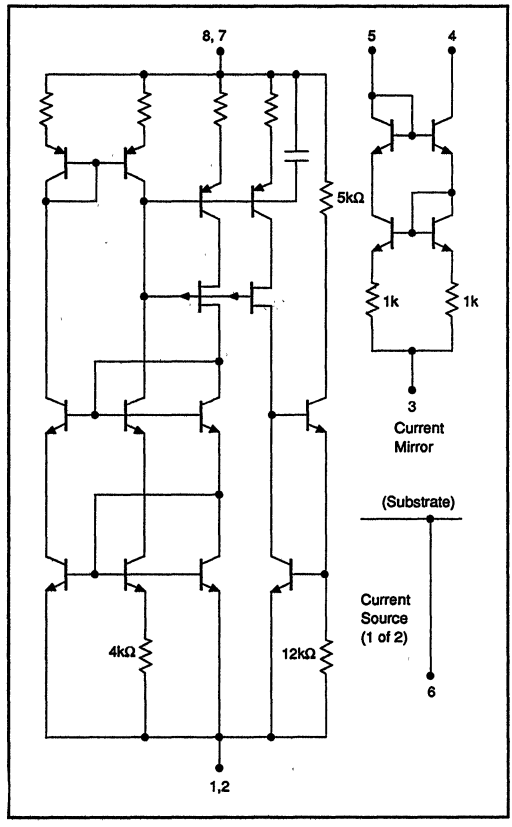


FIGURE 1. Simplified Circuit Diagram.

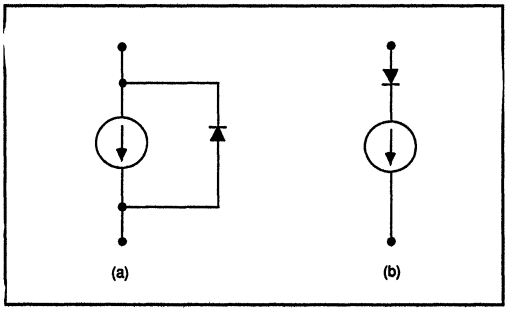


FIGURE 2. Reverse Voltage Protection.

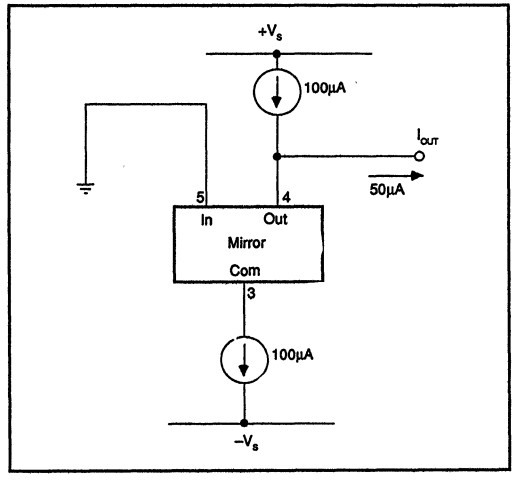


FIGURE 3. 50µA Current Source.

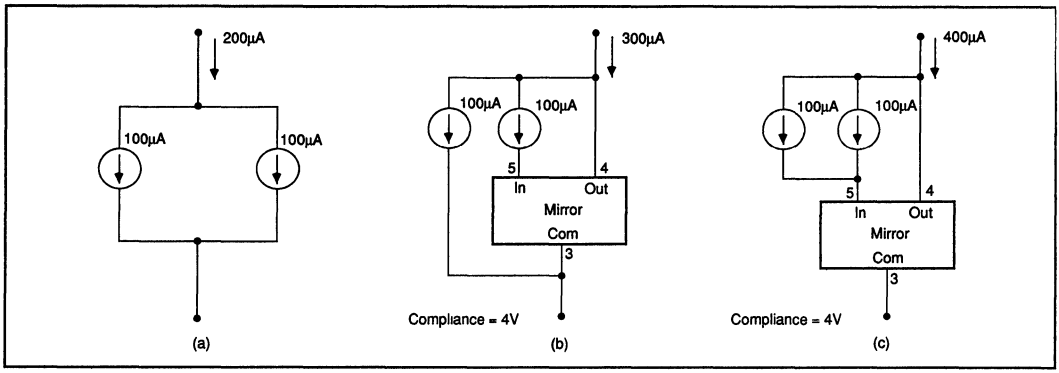


FIGURE 4. 200µA, 300µA, and 400µA Floating Current Sources.

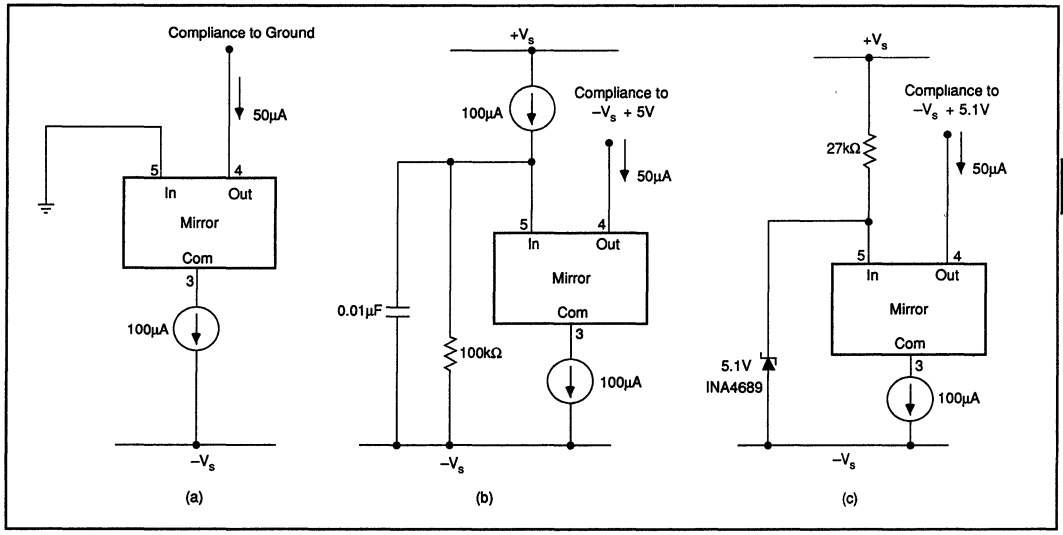


FIGURE 5. 50µA Current Sinks.

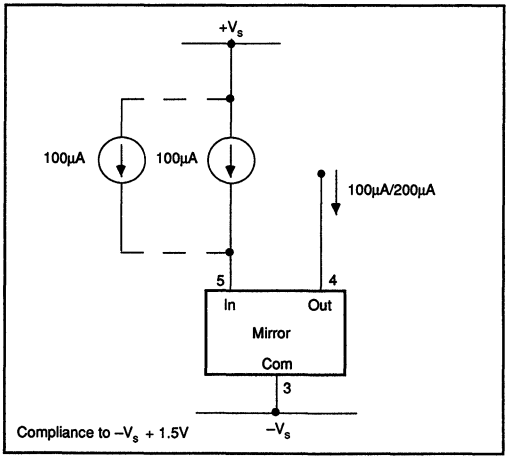


FIGURE 6. Improved Low-Voltage Compliance.

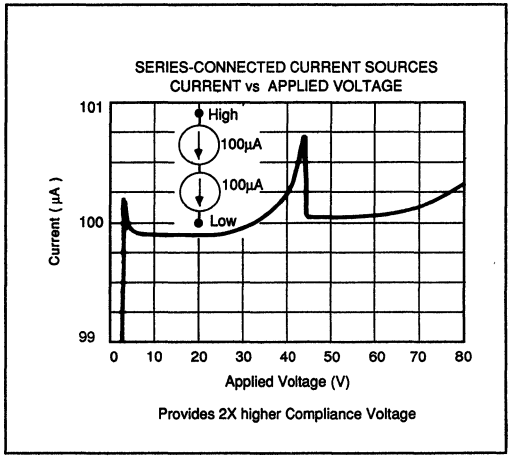
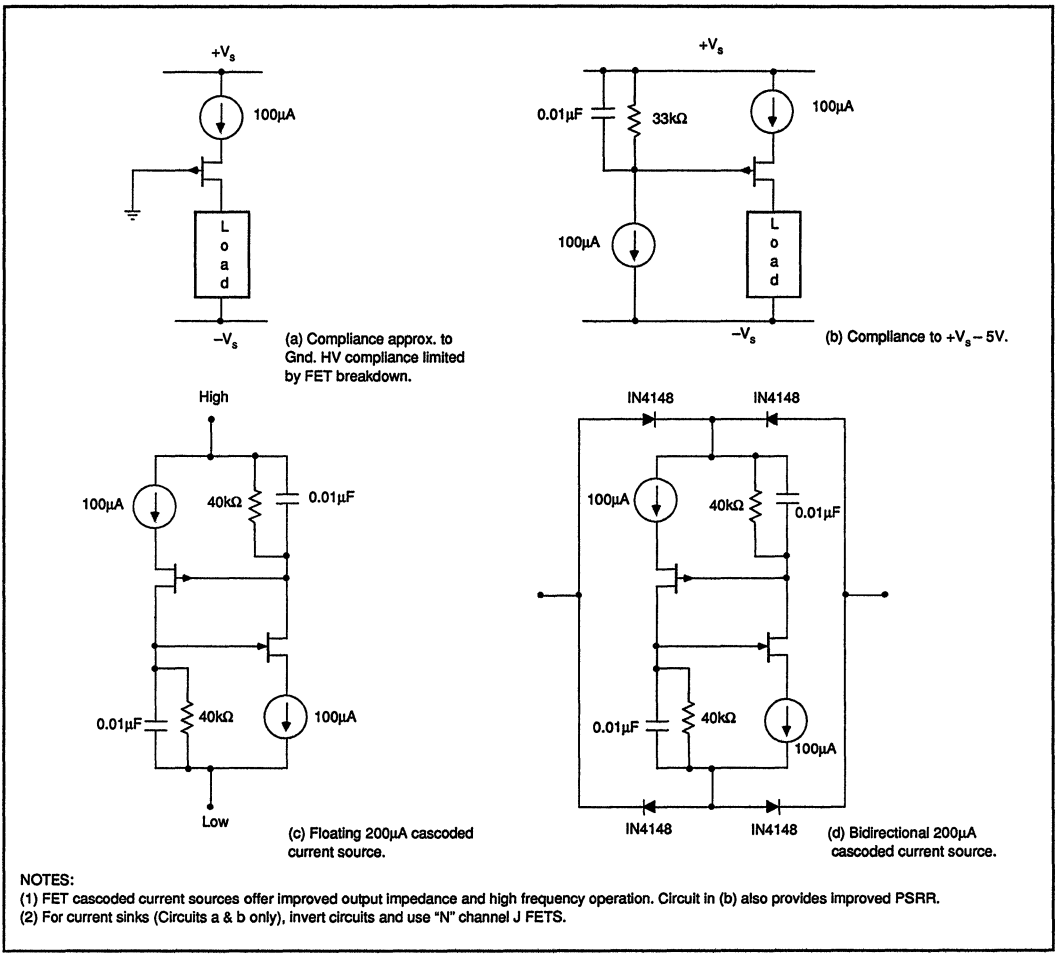


FIGURE 7. 100µA Current Source—80V Compliance.



NOTES:
(1) FET cascoded current sources offer improved output impedance and high frequency operation. Circuit in (b) also provides improved PSRR.
(2) For current sinks (Circuits a & b only), invert circuits and use "N" channel J FETS.

FIGURE 8. FET Cascode Circuits.

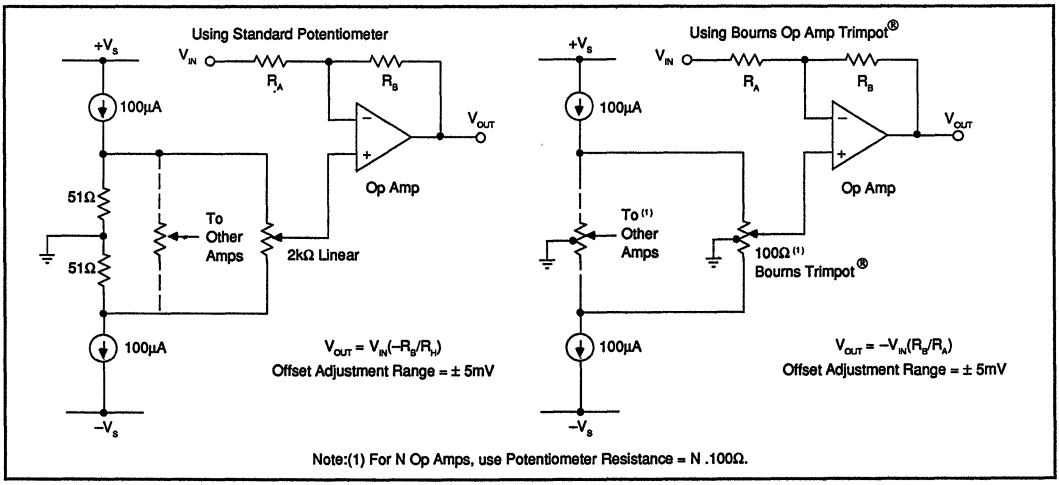
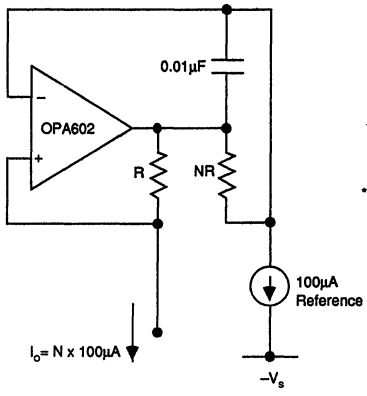


FIGURE 9. Op Amp Offset Adjustment Circuits.



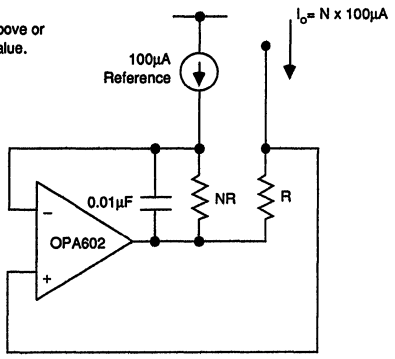
(a)

FEATURES:
(1) Adjustable to values above or below current reference value.

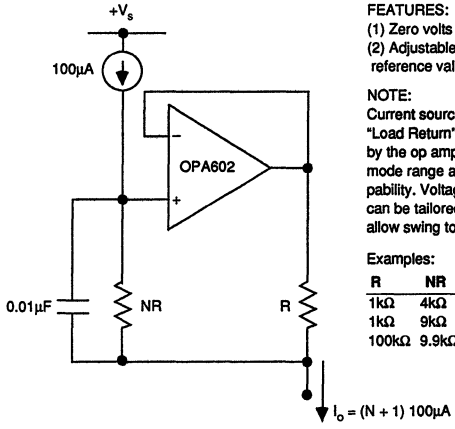
Examples:

NR	R	I_{OUT}
100Ω	10MΩ	1nA*
10kΩ	1mΩ	1µA
10kΩ	1kΩ	1mA

* Use OPA128 Op Amp



(b)



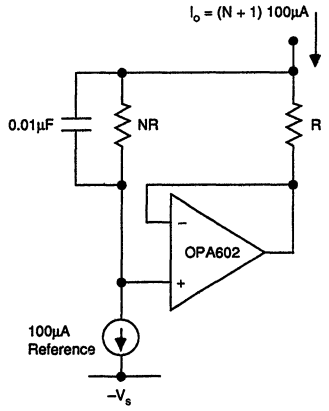
(c)

FEATURES:
(1) Zero volts shunt compliance.
(2) Adjustable only to values above reference value.

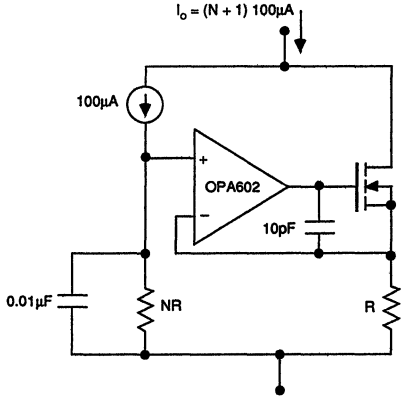
NOTE:
Current source/sink swing to the "Load Return" rail is limited only by the op amps input common mode range and output swing capability. Voltage drop across "R" can be tailored for any amplifier to allow swing to zero volts from rail.

Examples:

R	NR	I_{OUT}
1kΩ	4kΩ	500µA
1kΩ	9kΩ	1mA
100kΩ	9.9kΩ	10mA



(d)



(e)

I_o = 100µA (N + 1). Compliance ≈ 3.5V with 0.1V across R_L. Max I_o limited by FET. For I_o = 1A, R = 0.1Ω, NR = 1kΩ.

FIGURE 10. Adjustable Current Sources.

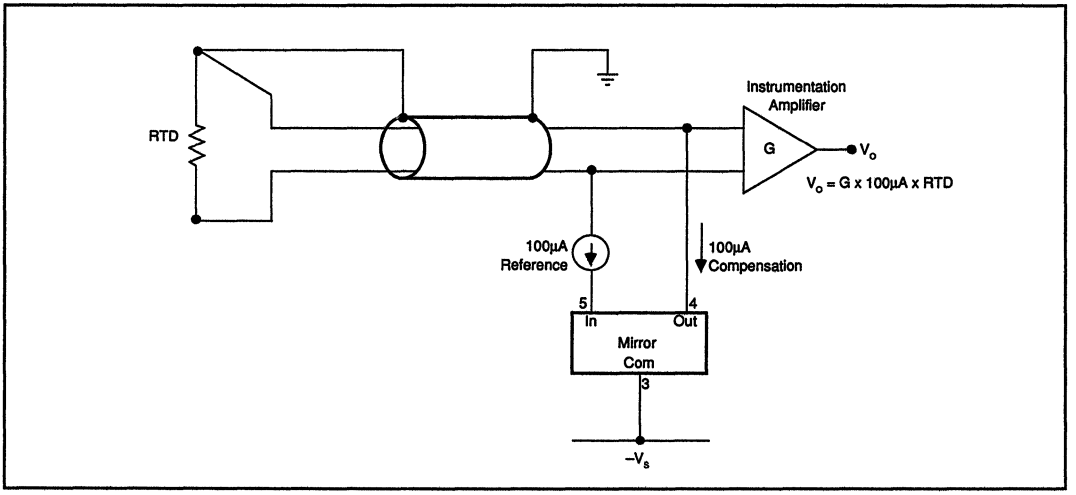


FIGURE 11. RTD Excitation With Three Wire Lead Resistance Compensation.

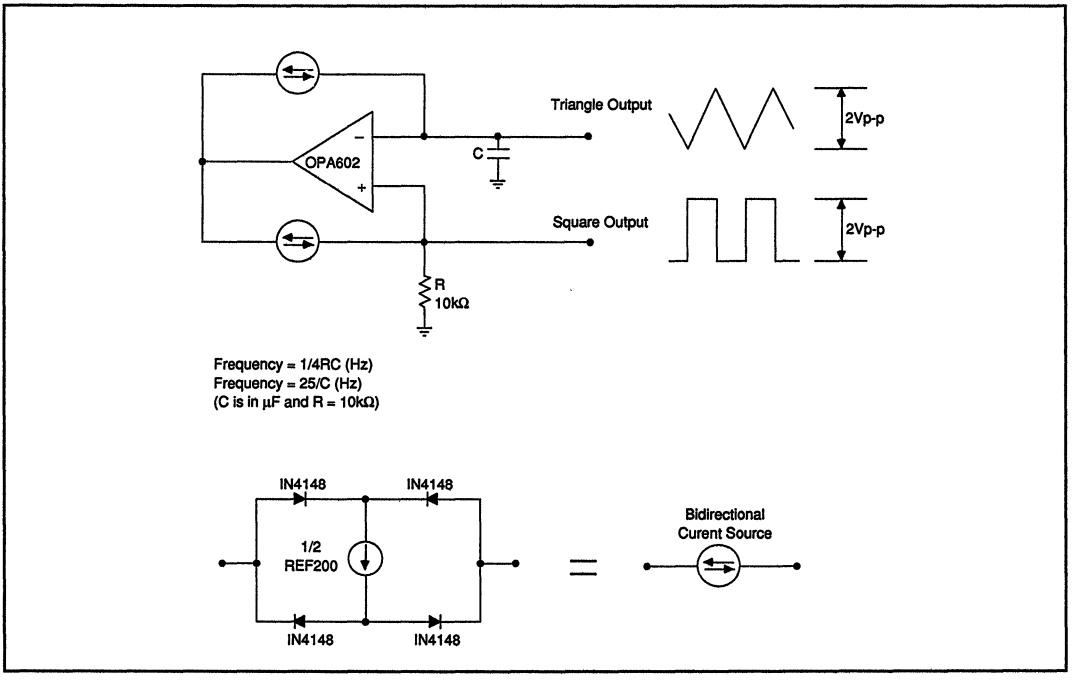


FIGURE 12. Precision Triangle Waveform Generator.

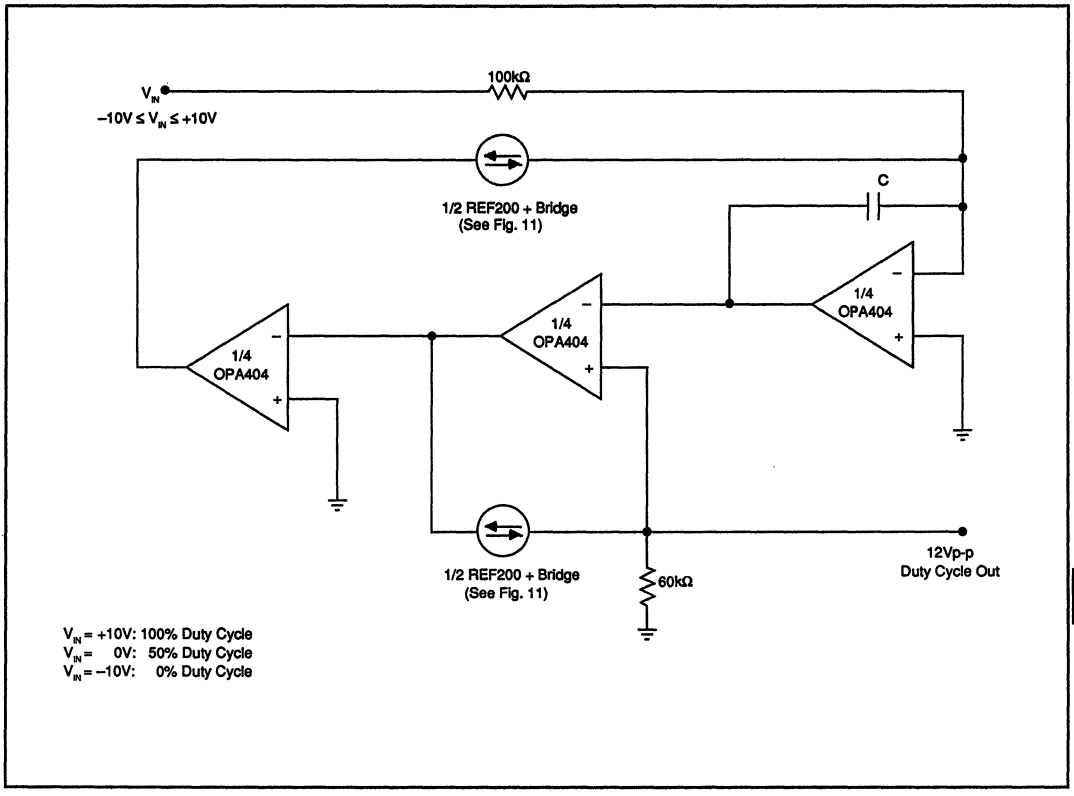


FIGURE 13. Precision Duty-Cycle Modulator.

For More Applications, Request Product Data Sheet PDS-851.

BURR-BROWN®

UAF11
UAF21

UNIVERSAL ACTIVE FILTERS

FEATURES

- SAVES DESIGN TIME
  - User-tuneable frequency, Q-factor, gain
  - Calculate only three resistance values
  - Design directly from this data sheet
  - Completely characterized parameters
- IMPROVED PERFORMANCE
  - Wide frequency ranges
  - UAF11 - 0.001Hz to 20kHz
  - UAF21 - 0.001Hz to 200kHz
  - 1% frequency accuracy
  - Q range of 0.5 to 500
  - Reliable hybrid construction
  - NPO capacitors and thin-film resistors

APPLICATIONS

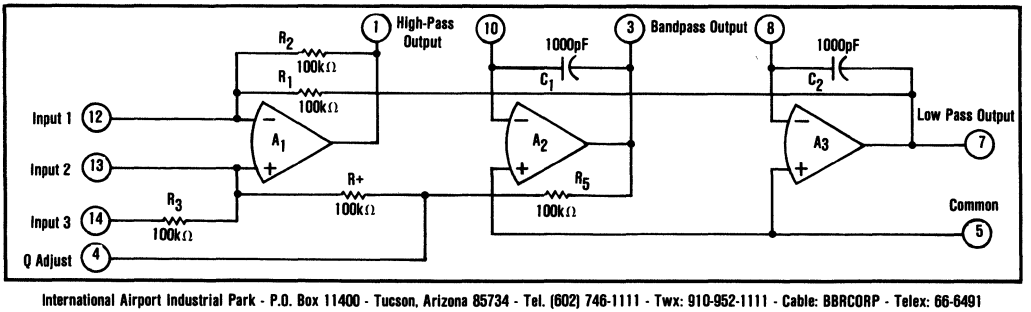
- FILTER CONFIGURATIONS
  - Butterworth
  - Bessel
  - Chebyschev
- FILTER FUNCTIONS
  - Low pass
  - High pass
  - Bandpass
  - Band reject

DESCRIPTION

The UAF11's and UAF21's are low cost universal active filters. These versatile units can easily be tailored to any active filter application using the extensive information provided in this data sheet. UAF's are excellent choices for use in communications equipment, test equipment (engine analyzers, aircraft and automotive test, medical test, etc.), servo systems, process control equipment, sonar and many others.

The UAF11's and UAF21's are complete two-pole active filters with the addition of four external resistors that provide the user easy control of the Q-factor, resonant frequency and gain. Any complex filter response can be obtained by cascading these units. Three separate outputs provide low-pass, high-pass, and bandpass transfer functions. A band-reject (notch) transfer function may be realized simply by summing the high-pass and low-pass outputs.

Since these UAF's are so versatile and flexible, they can be stocked by the user in quantity for use as building blocks whenever the requirement arises. This means instant availability and the UAF purchases may be made in volume to take advantage of quantity price discounts.



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PDS-295G

SPECIFICATIONS

ELECTRICAL

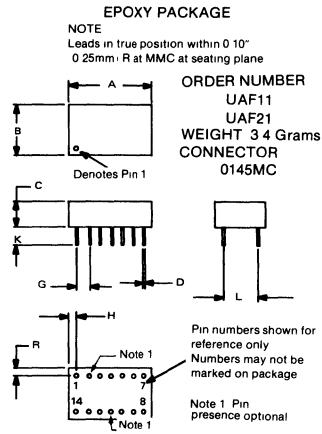
Typical at +25°C and with rated supply unless otherwise noted.

MODEL	UAF11	UAF21(1)	UNITS
INPUT			
Input Bias Current	±100	±15	nA
Input Voltage Range	±10	±10	V
Input Resistance	100k	100k	Ω
TRANSFER CHARACTERISTICS			
Frequency Range (f_o)	0 001 to 20k	0 001 to 200k	Hz
f_o Accuracy(2)	±1	±1	%
f_o Stability(3) (over temp range)	±0.005	±0.005	%/°C
Q Range(4)	0 5 to 500	0 5 to 500	--
Q Stability(5)			
at f_o Q ≤ 10^4	±0 025	±0 01	%/°C
at f_o Q ≤ 10^5	±0 1	±0 025	%/°C
Gain Range	0 1 to 50	0 1 to 50	--
OUTPUT			
Slew Rate	0 6	6 0	V/μsec
Peak-to-Peak Output Swing(6)			
f_o ≤ 10kHz	20	20	V
f_o ≤ 20kHz	10	20	V
f_o ≤ 100kHz	2	20	V
Output Offset			
(at low-pass output with unity gain)	±10	±10	mV
Output Impedance	2	10	Ω
Noise(7)	200	200	μV, rms
Output Current(8)	10	10	mA
POWER SUPPLIES			
Rated Power Supplies	±15	±15	V
Power Supply Range(9)	±5 to ±18	±5 to ±18	V
Supply Current at ±15V (Quiescent)	±12, max	±12, max	mA
TEMPERATURE RANGE			
Specification: Epoxy	−25 to +85	−25 to +85	°C
Storage. Epoxy	−40 to +85	−40 to +85	°C

NOTES

1 The UAF21 includes two internal 0 002μF power supply capacitors
2 Repeatability of f_o using 0 1% frequency determining resistors
3 T C R of external frequency determining resistors must be added to this figure
4 Derated 50% from maximum - see Typical Performance Curves
5 Q stability varies with both the value of Q and the resonant frequency f_o
6 Low-pass output - see Typical Performance Curves
7 Measured at the bandpass output with Q = 50 over DC to 50kHz
8 The current required to drive R_{F1} and R_{F2} (external) as well as C_1 and C_2 must come from this current
9 For supplies below ±10V, Q max will decrease slightly, filters will operate below ±5V

MECHANICAL

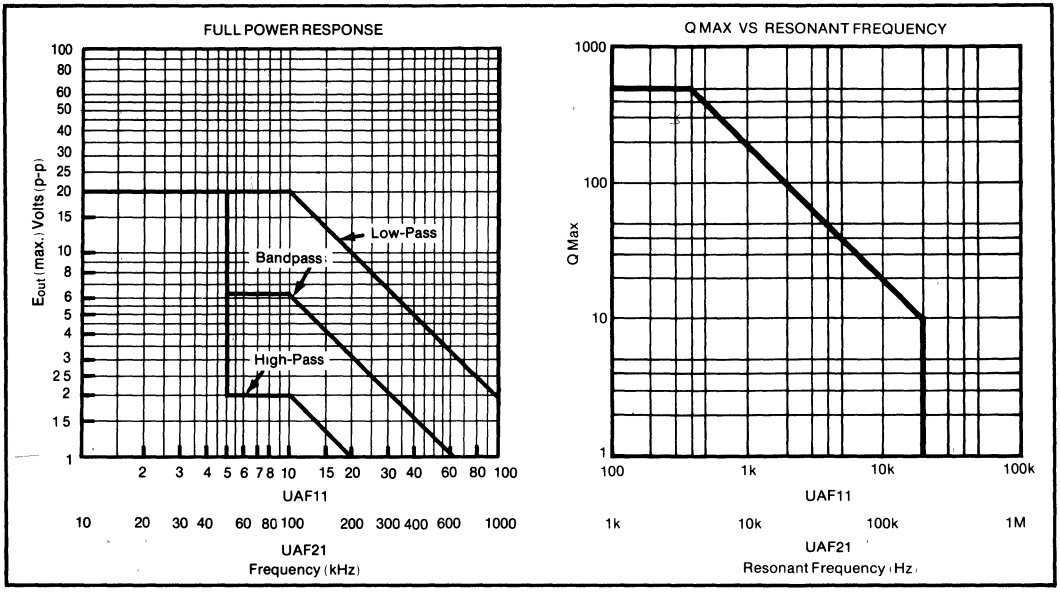


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	790	810	20.07	20.57
B	490	510	12 45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0 46	0 53
G	100 BASIC		2 54 BASIC	
H	.080	.115	2 03	2 92
K	130	300	3 30	7 62
L	.300 BASIC		7 62 BASIC	
R	080	115	2 03	2 92

PIN CONNECTIONS

Pin 1 High-Pass Output
Pin 2 Optional Pin
Pin 3. Bandpass Output
Pin 4 Q Adjust Point
Pin 5 Common
Pin 6 +Supply
Pin 7 Low-Pass Output
Pin 8 Frequency Adjust
Pin 9 -Supply
Pin 10 Frequency Adjust
Pin 11 Optional Pin
Pin 12 Input 1
Pin 13 Input 2
Pin 14 Input 3

TYPICAL PERFORMANCE CURVES



APPLICATIONS INFORMATION

TRANSFER FUNCTION

The UAF21 uses the state variable technique to produce a basic second order transfer function. The equation describing the three outputs available are:

$$T(\text{Low-Pass}) = \frac{A_{LP}\omega_o^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{Bandpass}) = \frac{A_{BP}(\omega_o/Q)s}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{High-Pass}) = \frac{A_{HP}\,s^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

where $\omega_o = 2\pi f_o$.

To obtain band reject characteristics the low-pass and high-pass outputs are summed to form a pair of $j\omega$ axis zeros:

$$T(\text{Band-Reject}) = \frac{A\,(s^2 + \omega_o^2)}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

where $A_{LP} = A_{HP} = A$.

The state variable approach uses two op amp integrators and a summing amplifier to provide simultaneous low-pass, bandpass and high-pass responses. One UAF is required for each two poles of low-pass or high-pass filters and for each pole-pair of bandpass or band-reject filters.

DESIGN PROCEDURE SUMMARY

These procedures give the design steps for the proper application of a UAF and for the selection of the external components. More detailed information on filter theory pertinent to some of the steps can be found in the reference sources listed in Table I.

TABLE I. Useful References.

1 Tobey, Gene, et al, Operational Amplifiers. Design and Applications, Chapter 8, McGraw-Hill Book Company, 1971

2 Wong, Yu Jen, and William Ott Function Circuits: Design and Applications, Chapter 6, McGraw-Hill Book Company, 1976

3 Daniels, Richard W Approximation Methods for Electronic Filter Design, McGraw-Hill Book Company, 1974

4 Zyerev, Anatol I Handbook of Filter Synthesis, John Wiley and Sons, 1967

5 Temes, Gabor C , and Sanjit K Mitra Modern Filter Theory and Design, John Wiley and Sons, 1973

Burr-Brown also manufactures a line of completely self-contained active filters called the ATF76 series. These are available in most popular transfer functions with from 2- to 8-pole responses. They contain all necessary components and do not require any user design effort.

DESIGN STEPS

1. Choose the type of function (low-pass, bandpass, etc.), type of response (Butterworth, Bessel, etc.), number of poles, and cutoff frequency based on the particular application.

   If the transfer function is band-reject see Band-Reject Transfer Function before proceeding to step 2.

2. Determine the normalized low-pass filter parameters (f_n and Q) based on the type of response and number of poles selected in step 1. See Normalized Low-Pass Parameters.

3. If the actual response desired is low-pass go to step 4. For other responses a transformation of variables must be made (low-pass to bandpass or low-pass to high-pass). See Low-Pass Transformation.

4. Determine the actual (denormalized) cutoff frequency, f_o, by multiplying f_n by the actual desired cutoff frequency. See Denormalization of Parameters.
5. Pick the desired UAF configuration (noninverting, inverting or bi-quad). See Configuration Selection Guide and UAF Configurations and Design Equations.
6. Decide whether to use design equations "A" or "B". See Design Equations "A" and "B".
7. Calculate R_{F1} and R_{F2}. See Natural Frequency and UAF Configurations and Design Equations.
8. Determine Q_P. See Q_P Procedure.
9. Select the desired gain for each UAF and calculate the corresponding R_G and R_Q. See Gain (A) and UAF Configurations and Design Equations.

BAND-REJECT TRANSFER FUNCTION

The band-reject is achieved by summing the high-pass and low-pass UAF outputs. Either of the configurations in Figures 2 and 3 can be used to provide the band-reject function if they are used as shown in Figure 1.

The 15kΩ resistor is adjusted for maximum rejection. The circuit in Figure 3 is applicable when using design equations "A" ($A_{LP} = A_{HP}$). When design equations "B" are used ($A_{LP} = 10A_{HP}$), the resistor at pin 7 must be 10 times the resistor at pin 1 to obtain equal pass-band gains above and below f_n.

In either case, the four external UAF resistors (R_G, R_Q, R_{F1} and R_{F2}) should be calculated for f_o and Q of the band-reject filter desired and for A_{LP} to equal the desired pass-band gain. An input constraint is that the input voltage times A_{BP} must not exceed the rated peak-to-peak voltage of the bandpass output, or clipping will result.

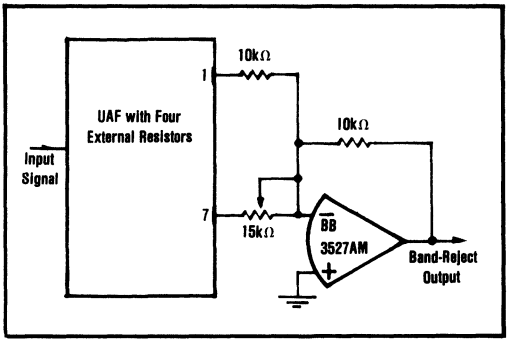


FIGURE 1. Band-Reject Configuration.

NORMALIZED LOW-PASS PARAMETERS

Usual active filter design procedure involves using normalized low-pass parameters. Table II is provided to assist in this step for the more common filter responses. Table III is a FORTRAN program which allows f_n and Q to be calculated for any desired ripple and number of poles for the Chebyschev response. Program inputs are the number of poles (N) and the peak-to-peak ripple (R). Program outputs are f_n and Q, which are used exactly as the values taken from Table II.

TABLE II. Low-Pass Filter Parameters.

Number of Poles	Butterworth		Bessel		Chebysev 0.5 dB Ripple		Chebysev 2 dB Ripple	
	f_n(1)	Q	f_n(1)	Q	f_n(2)	Q	f_n(2)	Q
2	1.0	0.70711	1.2742	0.57735	1.23134	0.86372	0.907227	1.1286
3	1.0	--	1.32475	--	0.626456	--	0.368911	--
	1.0	1.0	1.44993	0.69104	1.068853	1.7062	0.941326	2.5516
4	1.0	0.54118	1.43241	0.52193	0.597002	0.70511	0.470711	0.9294
	1.0	1.3065	1.60594	0.80554	1.031270	2.9406	0.963678	4.59388
5	1.0	--	1.50470	--	0.362320	--	0.218308	--
	1.0	0.61805	1.55876	0.56354	0.690483	1.1778	0.627017	1.77509
	1.0	1.61812	1.75812	0.91652	1.017735	4.5450	0.97579	7.23228
6	1.0	0.51763	1.60653	0.51032	0.396229	0.68364	0.31611	0.9016
	1.0	0.70711	1.69186	0.61120	0.768121	1.8104	0.730027	2.84426
	1.0	1.93349	1.90782	1.0233	1.011446	6.5128	0.982828	10.4616
7	1.0	--	1.68713	--	0.256170	--	0.155410	--
	1.0	0.55497	1.71911	0.53235	0.503863	1.0916	0.460853	1.64642
	1.0	0.80192	1.82539	0.66083	0.822729	2.5755	0.797114	4.11507
	1.0	2.2472	2.05279	1.1263	1.008022	8.8418	0.987226	14.2802
8	1.0	0.50980	1.78143	0.50599	0.296736	0.67658	0.237699	0.89236
	1.0	0.60134	1.85314	0.55961	0.598874	1.6107	0.571925	2.5327
	1.0	0.89998	1.95645	0.71085	0.861007	3.4657	0.842486	5.58354
	1.0	2.5629	2.19237	1.2257	1.005984	11.5308	0.990142	18.6873

1 -3dB frequency
2 Frequency at which amplitude response passes through the ripple band.

TABLE III. Low-Pass Chebyschev Program.

```
      PI=3.1415926536
      COMPLEX P(10)
      READ 5, N, R
    5 FORMAT (I2,F8.6)
      A=SQRT(EXP(R/4.3429448)-1.)
      B=1./A
      AN=ALOG(B+SQRT(B**2.-1.))
      AN=AN/FLOAT(N)
      J=MOD(N, 2)+N/2
      DO 10K=1, J
      RP=SINH(AN)*SIN(PI*FLOAT(2*K-1)/FLOAT(2*N))
      XIP=COSH(AN)*COS(PI*FLOAT(2*K-1)/FLOAT(2*N))
      WN=SQRT(RP**2+XIP**2)
      Q=-WN/(2*RP)
      P(K)=CMPLX(WN,Q)
      IF(MOD(N,2).NE.0 AND K.EQ.J)GO TO 15
      PRINT 20, P(K)
      GO TO 10
   15 F=REAL(P(K))
      PRINT 30, F
   10 CONTINUE
   20 FORMAT (2X"FN="E20.8"Q="E20.8)
   30 FORMAT (2X"FN = "E20.8)
      STOP
      END
```

NOTE Language variations between computers may require modification of this program

Note that for bandpass and high-pass filters complex conjugate pole pairs in the actual filter correspond to single poles in the normalized low-pass model. Thus four poles in Table II would correspond to four-pole pairs in a bandpass or high-pass filter.

Filters with an odd number of poles show one f_n with no corresponding Q value. This represents a simple RC network that is required for odd pole filters. This RC network with a cutoff frequency equal to f_n times the overall filter cutoff frequency should be placed in series with the first UAF two-pole section. An external op amp and RC network can be used for this purpose.

The cutoff frequency determined by the Table II filter parameters is (1) the -3dB frequency of the Butterworth response and of the Bessel response and (2) the frequency at which the amplitude response of the Chebyschev filters passes through the maximum ripple band (to enter the stop band).

LOW-PASS TRANSFORMATION

Low-Pass to High-Pass

The following simple transformation may be used for high-pass filters:

$$f_n \text{ (high-pass)} = \frac{1}{f_n \text{ (low-pass)}}$$

$$Q \text{ (high-pass)} = Q \text{ (low-pass)}$$

Low-Pass to Bandpass

The low-pass to bandpass transformation to generate f_n (bandpass) and Q (bandpass) is much more complicated. It is tedious to do by hand but can be accomplished with the FORTRAN program given in Table IV. This program automates the tranformation

$$s = p/2 \pm \sqrt{(p/2)^2 - 1.}$$

TABLE IV. Low-Pass to Bandpass Transformation Program.

```
    COMPLEX P,S,U
    READ 5, FN, Q, QBP
  5 FORMAT (3F12.5)
    Y=FN*SQRT(1.-1(./(Q*2.))**2)
    X=-FN/Q*2.)
    P=CMPLX(X,Y)
    U=CONJG(P)
    DO 30 I=1,2
    S=P/(2*QBP)
    P=S**2-1
    T=ATAN2(AIMAG(P),REAL(P))
    IF (T.GE.0.)GO TO 10
    T=2.*3.14159+T
 10 T=T/2.
    A=SQRT(CABS(P))*COS(T)
    B=SQRT(CABS(P))*SIN(T)
    S=S+CMPLX(A,B)
    FN=CABS(S)
    Q=-FN/(2.*REAL(S))
    PRINT 20,FN,Q
 20 FORMAT (2X"FN="F12.5"Q="F12 5)
    IF(AIMAG(U) EQ.0.)GO TO 40
 30 P=U
 40 STOP
    END
```

NOTE. Language variations between computers may require modification of this program.

Program Inputs

1. f_n - From Table II for the low-pass filter of interest
2. Q - From Table II
3. Q_{BP} - Desired Q of the bandpass filter

For filters with an odd number of poles a Q of 0.5 should be used where Q is not given in Table II. Enter 10^5 for Q when transforming zeros on the imaginary axis.

The program transforms each low-pass pole into a bandpass pole pair. Thus a three-pole low-pass input, would result in the pole positions for a three-pole pair bandpass filter requiring three UAF stages.

DENORMALIZATION OF PARAMETERS

Table II shows filter parameters for many 2- to 8-pole normalized low-pass filters. The Q and the normalized undamped natural frequency, f_n for each two-pole section are shown. The Q values do not have to be denormalized and may be used directly as described in the Design Procedure Summary. f_n must be denormalized by multiplying it by the desired cutoff frequency of the actual overall filter to obtain the required frequency, f_o for the design formulas. As an example, consider a 4-pole low-pass Bessel filter with a cutoff frequency of 1000Hz. The first stage would be designed to an $f_o$of 1432.41Hz and a Q of 0.52193 while the second stage would have an f_o of 1605.94Hz and Q of 0.80554. To combine the two stages into the composite filter the low-pass output of the first stage (pin 9) would be connected to the input resistors (R_G) of the second stage.

CONFIGURATION SELECTION GUIDE

It is possible to configure the UAF three different ways. Each configuration produces features that may or may not be desirable for a specific application. The selection guide in Table V is given to assist in determining the most advantageous configuration for a particular application.

UAF CONFIGURATIONS AND DESIGN EQUATIONS

Noninverting Configuration

For applications requiring a bandpass gain of 1V/V, the internal resistor R_3 may be used (input at pin 14) as the gain resistor R_G; thus, only three external resistors are needed to configure the filter.

To use equations "B" connect an 11kΩ resistor between pins 12 and 1. Use equations "B" for frequencies above 8kHz or when R_Q from equations "A" becomes a negative value.

SIMPLIFIED DESIGN EQUATIONS "A"

$f_o < 5kHz$ (UAF11) or 50kHz (UAF21)

1. $R_{F1} = R_{F2} = 10^9/\omega_o = 1.59 \times 10^8/f_o$
2. $A_{BP} = QA_{LP} = QA_{HP}$
3. $R_Q = 10^5/(2Q_P - A_{BP} - 1)$
4. $R_G = (2Q_P - A_{BP} + 1)\ 10^5/A_{BP}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o > 5kHz$ (UAF11) or 50kHz (UAF21)

1. $R_{F1} = R_{F2} = 3.16 \times 10^8/\omega_o = 5.03 \times 10^7/f_o$
2. $A_{BP} = Q/3.16\ A_{LP} = 3.16Q\ A_{HP}$
3. $R_Q = 10^5/(3.48Q_P - A_{BP} - 1)$
4. $R_G = (3.48Q_P - A_{BP} + 1)\ 10^5/A_{BP}$

Inverting Configuration

SIMPLIFIED DESIGN EQUATIONS "A"

$f_o < 5kHz$ (UAF11) or 50kHz (UAF21)

1. $R_{F1} = R_{F2} = 10^9/\omega_o = 1.59 \times 10^8/f_o$
2. $A_{BP} = Q\ A_{LP} = Q\ A_{HP}$
3. $R_G = 10^5\ Q_P/A_{BP}$
4. $R_Q = 2 \times 10^5/(2Q_P + A_{BP} - 1)$

	NONINVERTING INPUT	INVERTING INPUT	BI-QUAD
Outputs Available	BP, LP and HP	BP, LP and HP	BP and LP
Inverted Outputs	BP	HP and LP	BP and LP
Q & Gain Independent of Frequency Resistors?	Yes	Yes	No
Type of Q Variation With Changes in R_F	Constant Q	Constant Q	Constant bandwidth
Other Advantages	May be used with only three external resistors (use internal R_3 as R_G)		R_G and R_Q are small at high frequencies
Parameter Limitations	$2Q_P - A_{BP} > 1$ ($f_o < 8kHz$) $3\ 48Q_P - A_{BP} > 1$ ($f_o > 8kHz$)	$2Q_P + A_{BP} > 1$ ($f_o < 8kHz$) $3\ 48Q_P + A_{BP} > 1$ ($f_o > 8kHz$)	None

Summary The Bi-Quad filter is particularly useful as a bandpass filter if the filter bandwidth must be kept constant as the center frequency is varied If Q must be kept constant (i.e , constant Q of a bandpass or maintaining constant response of a low-pass or high-pass) one of the other two configurations should be used The Bi-Quad also has the advantage that R_G and R_Q are smaller than R_G and R_Q of the other two configurations (this is especially useful at high frequencies). The noninverting input configuration has the advantage that for $A_{BP} = 1$, $R_G = 100k\Omega$, therefore R_3 (internal) may be used so that only three external resistors are needed (R_{F1}, R_{F2}, R_Q)

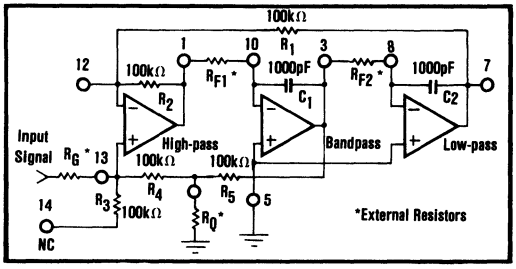


FIGURE 2. Noninverting Configuration.

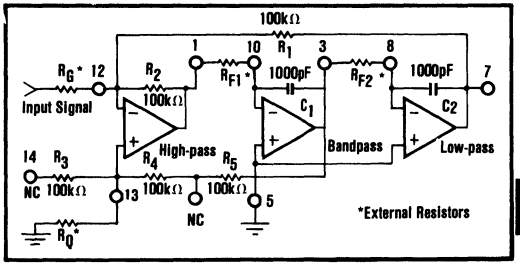


FIGURE 3. Inverting Configuration.

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o > 5kHz$ (UAF11) or 50kHz (UAF21)

1. $R_{F1} = R_{F2} = 3.16 \times 10^8/\omega_o = 5.03 \times 10^7/f_o$
2. $A_{BP} = Q_P/3\ 16 = 3.16Q_P\ A_{HP}$
3. $R_G = 3.16 \times 10^4\ Q_P/A_{BP}$
4. $R_Q = 2 \times 10^3/(3.48Q_P + A_{BP} - 1)$

Bi-QUAD Configuration

SIMPLIFIED DESIGN EQUATIONS "A"

$f_o < 5kHz$ (UAF11) or 50kHz (UAF21)

1. $R_{F1} = R_{F2} = 10^9/\omega_o = 1.59 \times 10^8/f_o$
2. $Q\ A_{LP} = A_{BP}$
3. $R_Q = Q_P R_{F1}$
4. $R_G = R_Q/A_{BP}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o > 5kHz$ (UAF11) or 50kHz (UAF21)

1. $R_{F1} = R_{F2} = 3.16 \times 10^8/\omega_o = 5.03 \times 10^7/f_o$
2. $Q\ A_{LP} = A_{BP}$
3. $R_Q = 3.16\ Q_P\ R_{F1}$
4. $R_G = R_Q/A_{BP}$

Design Equations "A" and "B"

1. For f_o below 8kHz, either of equations "A" or "B" may be used.
2. For f_o above 8kHz, equations "B" must be used. If equations "A" were used above 8kHz, the filter could become unstable.
3. Equations "A" are for the UAF as it is supplied. When using equations "B", a 11kΩ resistor must be placed in parallel with R_2 (between pins 12 and 1).

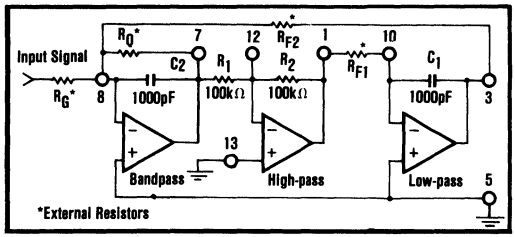


FIGURE 4. Bi-Quad Configuration.

4. The values of R_{F1} and R_{F2} calculated with equations "B" are approximately one-third of those calculated with equations "A". Thus there may be an advantage in using equations "B" at low frequencies. Using equations "B" would require use of one more resistor, but that would not alter or affect filter performance in any manner.
5. Using the negative gain values for A_{LP} or A_{HP} or A_{BP} could result in the negative values for resistors R_G and R_Q. So the absolute value of the gain should always be used in the equations.
6. Under some circumstances the value of R_Q using equations "A" will be negative. If this occurs, use design equations "B".

Natural Frequency (f_o)

1. f_o for each one pole-pair bandpass filter is the center frequency (f_c). f_c is defined as $f_c = \sqrt{f_1 f_2}$ where f_1 is the lower -3dB point and f_2 is the upper -3dB point of the pole-pair response.

2. To obtain f_o below 100Hz using practical resistor values, capacitors may be paralleled with C1 and C2 to reduce the size of R_{F1} and R_{F2}. If capacitors are added in parallel,

$$R_{F1}\text{ (new)} = R_{F2}\text{ (new)} = R_{F1}\text{ (old)}\ \frac{1000pF}{C + 1000pF}$$

where R_F (new) is the new lower value frequency resistor, C is the value of the two external capacitors placed across C1 and C2 (between pins 10 and 3 and pins 8 and 7 and R_{F1} (old) is the value calculated in the simplified design equations.

Q-Factor

1. For bandpass filters $Q = \frac{f_o}{3dB\text{ bandwidth}}$
2. When designing low-pass filters of more than two poles, best results will be obtained if the two pole sections with lower Q are followed by the sections with higher Q. This will eliminate any possibility of clipping due to high gain ripple in high Q sections.

Q_P Procedure

1. If the "f_o times Q" product is greater than 10^4 (or 10^5 for the UAF21), it is possible for the measured filter Q to be different from the calculated value of Q. This effect is the result of nonideal characteristics of operational amplifiers. It can be compensated for by introducing the parameter Q_P into the design equations.
2. Calculate the f_o Q product for the filter. If the product is above 10^4Hz (or 10^5 for the UAF21), locate the corresponding f_oQ_P product on the curve in Figure 5. Divide f_oQ_P by f_o to obtain Q_P. Use Q_P as indicated in the design equations. For f_oQ products below 10^4Hz (or 10^5 for the UAF21), $Q_P = Q$.

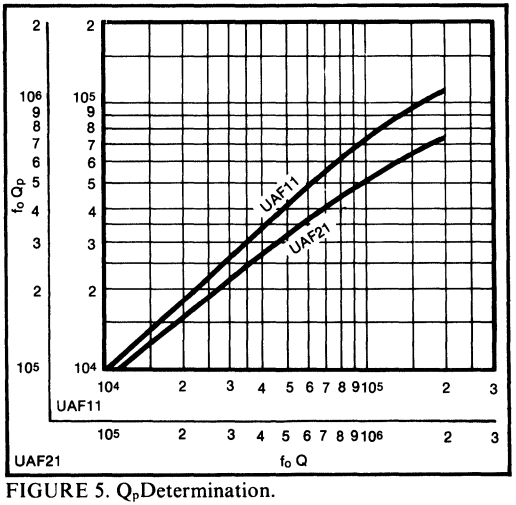


FIGURE 5. Q_PDetermination.

Gain (A)

1. The gain (V/V) of each filter section is:
   A_{LP} - for low-pass output - gain at DC
   A_{BP} - for bandpass output - gain at f_o
   A_{HP} - for high-pass output - gain at high frequencies.
2. Refer to the Typical Performance Curves for full power response. When selecting the gain, insure the limits of the curve are not exceeded for the desired voltage range.

DETAILED TRANSFER FUNCTION EQUATIONS

The following equations show the action of all the internal and external UAF filter components. They are not required for the regular design procedure but could be used if a detailed analysis is required.

NONINVERTING INPUT CONFIGURATION

1. $\omega_o^2 = R_2/(R_1 R_{F1} C_1 R_{F2} C_2)$
2. $Q = \left(1 + \frac{R_E}{R_G}\right)\left(\frac{R_1}{R_1 + R_2}\right)(1 + 10^5/R_Q)\sqrt{\frac{R_2 R_{F1} C_1}{R_1 R_{12} C_2}}$
3. $R_E = 10^5 + 10^5\ R_Q/(10^5 + R_Q)$
4. $Q\ A_{LP} = Q\ A_{HP}\ R_1/R_2 = A_{BP}\sqrt{R_1 R_{11} C_1/(R_2 R_{12} C_2)}$
5. $A_{BP} = 10^5\ (2 + 10^5/R_Q)/R_G$

INVERTING INPUT CONFIGURATION

1. $\omega_o^2 = R_2/(R_1 R_{F1} C_1 R_{F2} C_2)$
2. $Q = R_P\ (1 + 2 \times 10^5/R_Q)\sqrt{R_{F1} C_1/(R_1 R_2 R_{F2} C_2)}$
3. $Q\ A_{LP} = Q\ R_1\ A_{HF}/R_2 = A_{BP}\sqrt{R_1 R_{F1} C_1/(R_2 R_{F2} C_2)}$
4. $A_{BP} = \sqrt{R_1 R_2 R_{F2} C_2/(R_{F1} C_1)}\ \ Q/R_G$
5. $1/R_P = 1/R_1 + 1/R_2 + 1/R_G$

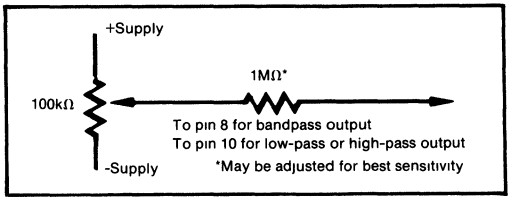
BI-QUAD CONFIGURATION

1. $\omega_o^2 = R_2/(R_1 R_{F1} C_1 R_{F2} C_2)$
2. $Q = R_Q C_2\ \omega_o$
3. $Q\ A_{LP}/(\omega_o R_{12} C2) = A_{HP} = R_Q/R_G$

Offset Error Adjustment

DC offset errors will be minimized by grounding pin 5 through a resistor equal to 1/2 the value of R_{F1} or R_{F2}. The DC offset adjustment shown here may be used if required.

Offset errors will increase with increases in R_F.



Design Example

It is desired to design a 5-pole Bessel, Low-Pass Filter with $f_o = 3.3$kHz and $A_{LP} = 1$. We will use the UAF11 to implement this filter.

From Table II the following values of f_n and Q are obtained.

Complex Poles:
$f_n = 1.55876$
$Q = 0.56354$
$f_n = 1.75812$
$Q = 0.91652$
Simple Pole:
$f_n = 1.50470$

Using the above shown values of f_n and Q, we now will proceed to design the three stages of filter separately.

Any one of the three configurations can be used. We will select inverting configuration.

For Stage 1.

$f_o = 3.3kHz \times f_n = 3.3kHz \times 1.55876 = 5144Hz$

Since $f_o > 5kHz$, equations "B" would be used, thus an 11kΩ resistor must be connected between pins 12 and 1.

$$R_{F1} = R_{F2} = \frac{5.03 \times 10^7}{5144} = 9778\Omega$$

$$f_oQ = 5144 \times 0.56354 = 2.9 \times 10^3$$

$f_oQ < 10^4$, $\therefore Q_P = Q = 0.56354$

$$A_{BP} = \frac{Q_P}{3.16} \quad A_{LP} = \frac{0.56354}{3.16} \times 1 = 0.17834$$

$$R_G = \frac{3.16 \times 10^4 Q_P}{A_{BP}} = \frac{3.16 \times 10^4 \times 0.56354}{0.17834} = 99.85k\Omega$$

$$R_Q = \frac{2 \times 10^5}{3.48Q_P + A_{BP}-1} = \frac{2 \times 10^5}{3.48 \times 0.56354 + 0.17834 - 1} = 175.52k\Omega$$

For Stage 2.

$f_o = 3.3kHz \times f_n = 3.3kHz \times 1.75812 = 5802Hz$

Since $f_o > 5kHz$, equations "B" would again be used, and an 11kΩ resistor would be connected between pins 12 and 1 of the second UAF stage.

$$R_{F1} = R_{F2} = \frac{5.03 \times 10^7}{5802} = 8669\Omega$$

$$f_oQ = 5802 \times 0.91652 = 5.32 \times 10^3$$

$f_oQ < 10^4$, $\therefore Q_P = Q = 0.91652$

$$A_{BP} = \frac{Q_P}{3.16} \quad A_{LP} = \frac{0.91652}{3.16} \times 1 = 0.29004$$

$$R_G = \frac{3.16 \times 10^4 Q_P}{A_{BP}} = \frac{3.16 \times 10^4 \times 0.91652}{0.29004} = 99.86k\Omega$$

$$R_Q = \frac{2 \times 10^5}{(3.48 Q_P + A_{BP}-1)} = \frac{2 \times 10^5}{(3.48 \times 0.91652 + 0.29004 - 1)} = 80.66k\Omega$$

For Stage 3.

$f = 3.3kHz \times f_n = 3.3kHz \times 1.50470 = 4966Hz$

For the simple pole,

$$RC = \frac{1}{2\pi f} = \frac{1}{2\pi \times 4966} = 3.2049 \times 10^{-5}$$

3300pF (or any convenient value)

$$R = \frac{3.2049 \times 10^{-5}}{3300 \times 10^{-12}} = 9.71k\Omega$$

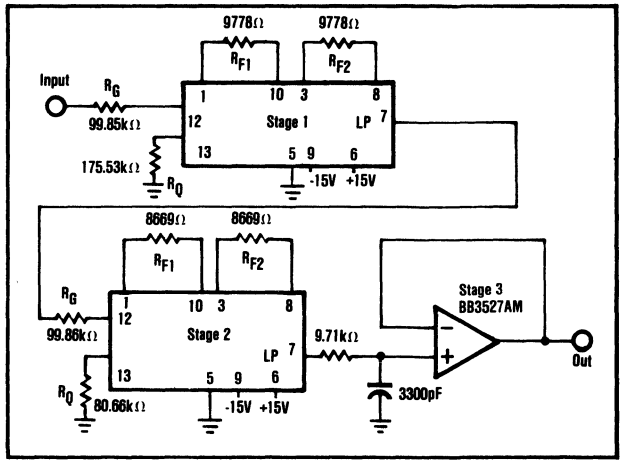
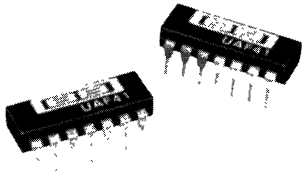


FIGURE 6. Overall Circuit.

BURR-BROWN®

UAF41



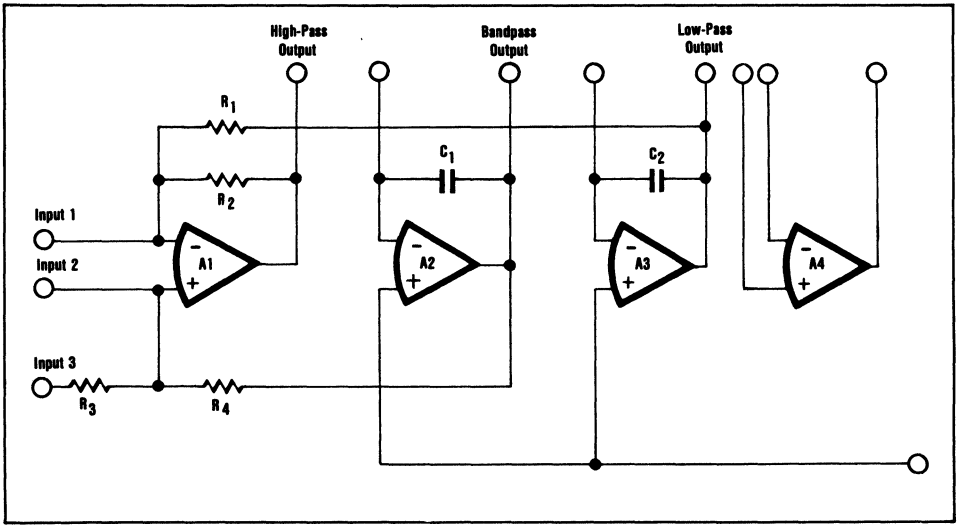
UNIVERSAL ACTIVE FILTER

FEATURES

- LOW COST
- SMALL SIZE
  Single wide DIP package
- FULLY CHARACTERIZED PARAMETERS
- HYBRID CONSTRUCTION
- IMPROVED PERFORMANCE
  1% frequency accuracy
  Q range of 0.5 to 500
  NPO capacitors and thin-film resistors
  Uncommitted op amp included

BENEFITS

- SAVES PRINTED CIRCUIT BOARD SPACE
- SAVES DESIGN TIME
  Calculate only four resistance values
  Design directly from this data sheet
  Versatile building block for filter design
- HIGH RELIABILITY
- HIGH STABILITY



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PDS-359D

DESCRIPTION

The UAF41 is a versatile two-pole active filter. It uses a three operational amplifier double integrator feedback loop to generate a complex pole pair (two conjugate poles). The location of the poles in the complex plane (and thus the natural frequency and Q) are determined by external, user supplied resistors. Either three or four resistors are used depending on the particular configuration chosen.

The UAF41 produces three transfer functions simultaneously - low-pass, high-pass, and bandpass - which are available at three separate outputs. The fourth basic transfer function - the band-reject or notch - can be obtained simply by summing the high-pass and low-pass outputs using the uncommitted amplifier (A4) contained in the UAF41. The uncommitted op amp can also be used to add a single-pole response for complex filters requiring an odd number of poles.

More complex higher-order filters can readily be obtained by cascading UAF's. This is easily done with the UAF41 since the high input impedance and low output impedance associated with the operational amplifiers used prevents the series connected stages from interacting (e.g., no frequency pull due to following stage loading). This data sheet contains the design procedures for an easy selection of resistor values for the stagger tuning of cascaded stages.

The versatility of the UAF41 makes it a general purpose building block for a wide variety of active filter applications. Its universal nature, ease of use, small size, and low cost allows the user the convenience of keeping units on hand for immediate use whenever a filter requirement arises.

TRANSFER FUNCTION

The UAF41 uses the state variable technique to produce a basic second order transfer function. The equations describing the three outputs available are:

$$T(\text{Low-Pass}) = \frac{A_{LP}\omega_o^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{Bandpass}) = \frac{A_{BP}\,(\omega_o/Q)s}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{High-Pass}) = \frac{A_{HP}\,s^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

To obtain band-reject characteristics the low-pass and high-pass outputs are summed to form a pair of $j\omega$ axis zeros:

$$T(\text{Band-Reject}) = \frac{A\,(s^2 + \omega_o^2)}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

where $A_{LP} = A_{HP} = A$.

The state variable approach uses two op amp integrators (A2 and A3 in the simplified schematic below) and a summing amplifier (A1) to provide simultaneous low-pass, bandpass, and high-pass responses. One UAF41 is required for each two poles of low-pass or high-pass filters and for each pole-pair of bandpass or band-reject filters.

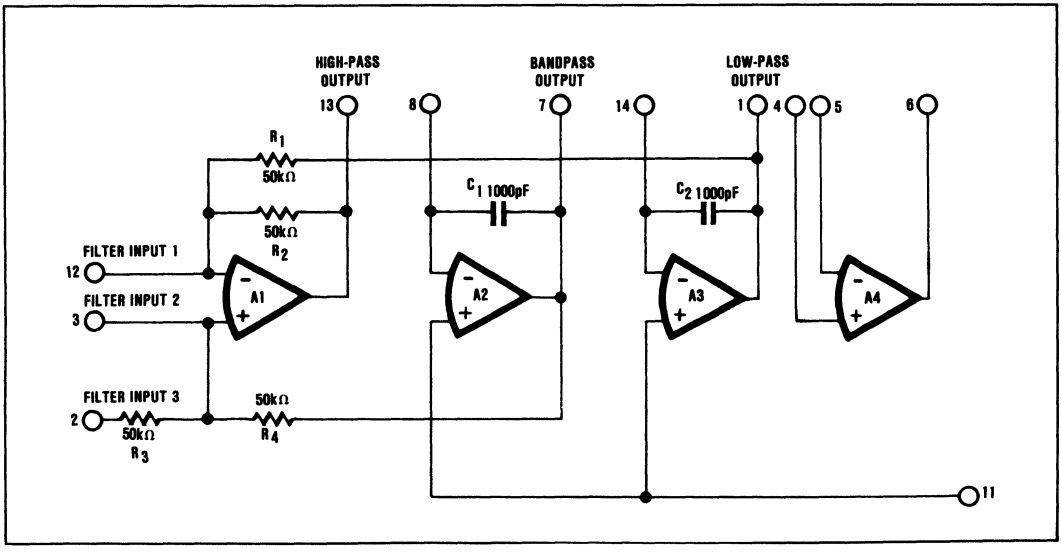


FIGURE 1. UAF41 Schematic.

SPECIFICATIONS

ELECTRICAL

Typical at 25°C and with rated supply unless otherwise noted

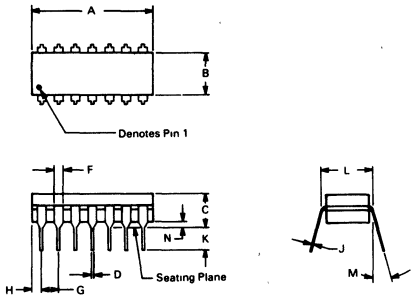
MODEL	UAF41
INPUT	
Input Bias Current	±40nA
Input Voltage Range	±10V
Input Resistance(1)	50kΩ
TRANSFER CHARACTERISTICS	
Frequency Range (f_o)	0.001Hz to 25kHz
f_o Accuracy(2), max	±1%
f_o Stability(3)	±0.002%/°C
Q Range(4)	0.5 to 500
Q Stability(5)	
@ f_o Q ≤ 10^4	±0 01%/°C
@ f_o Q ≤ 10^5	±0.025%/°C
Q Repeatability at f_o Q ≤ 10^5	±10%
Gain Range	0 1V/V to 50V/V
OUTPUT	
Peak-to-Peak Output Swing(6)	20V
Output Offset(7)	
(at L.P. output with unity gain)	±20mV
Output Impedance	1Ω
Noise(8)	200μV, rms
Output Current(9)	5mA
UNCOMMITTED AMP CHARACTERISTICS	
Input Offset Voltage	5mV
Input Bias Current	40nA
Input Impedance	1MΩ
Large Signal Voltage Gain	85dB
Output Current	5mA
POWER SUPPLIES	
Rated Power Supplies	±15VDC
Power Supply Range(10)	±5VDC to ±18VDC
Supply Current @ ±15V (Quiescent), max	7mA
TEMPERATURE RANGE	
Specification Temperature Range	-25°C to +85°C
Storage Temperature Range	-25°C to +85°C

NOTES:

1. For noninverting input configuration with A_{BP} * 1.
2. The tolerance of external frequency determining resistors must be added to this figure.
3. T.C.R. of external frequency determining resistors must be added to this figure.
4. See Performance Curves for Q_{max} vs F curve.
5. Q stability varies with both the value of Q and the resonant frequency f_o
6. See Performance Curves for full power response curve.
7. $R_{F1} = R_{F2} < 100k\Omega$ at low-pass output with unity gain.
8. Measured at the bandpass output with Q @ 50 over DC to 50kHz.
9. The current required to drive R_{F1} and R_{F2} (external) as well as C1 and C2 must come from this current.
10. For supplies below ±10V, Q_{max} will decrease slightly; filters will operate below ±5V.

MECHANICAL

14-Pin Plastic DIP Package



NOTE
Leads in true position within .010" (.25mm) R @ MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	660	785	16 76	19 94
B	220	280	5 59	7 11
C	–	200	–	5 08
D	015	023	0 38	0 58
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	030	095		
J	008	015	0 20	0 38
K	100	–	2 54	–
L	300 BASIC		7 62 BASIC	
M	–	15°	–	15°
N	020	050	0 51	1 27

ROW SPACING: 7 63mm (0.300")
WEIGHT 1 1 grams max

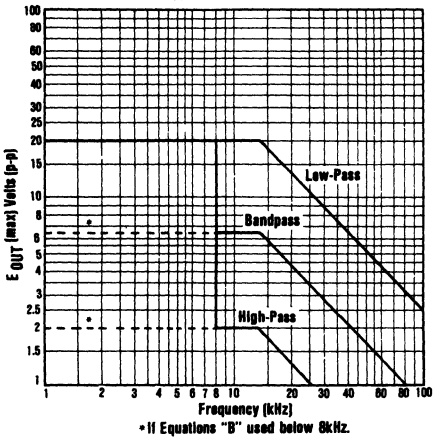
Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

PIN CONNECTIONS

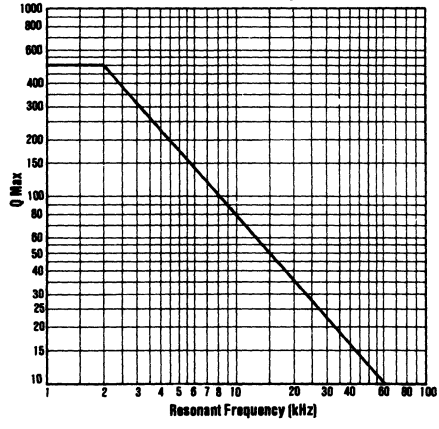
Pin 1 - LOW-PASS OUTPUT
Pin 2 - FILTER INPUT 3
Pin 3 - FILTER INPUT 2
Pin 4 - AUXILIARY AMP + INPUT
Pin 5 - AUXILIARY AMP - INPUT
Pin 6 - AUXILIARY AMP OUTPUT
Pin 7 - BANDPASS OUTPUT
Pin 8 - FREQUENCY ADJUST
Pin 9 - NEGATIVE SUPPLY
Pin 10 - POSITIVE SUPPLY
Pin 11 - COMMON
Pin 12 - FILTER INPUT 1
Pin 13 - HIGH-PASS OUTPUT
Pin 14 - FREQUENCY ADJUST

TYPICAL PERFORMANCE CURVES

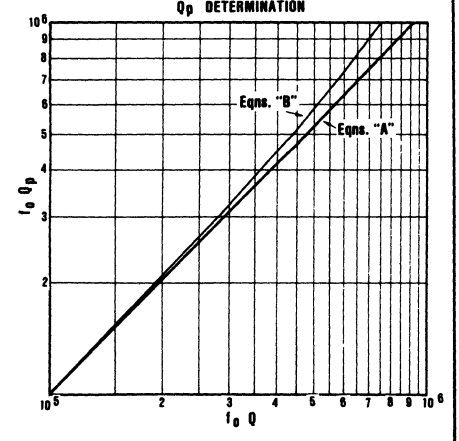
FULL POWER RESPONSE



Q MAX VS RESONANT FREQUENCY



Q_P DETERMINATION



DESIGN PROCEDURE SUMMARY

This summary gives the design steps for the proper application of UAF41s and for the selection of the external components. More detailed information on filter theory pertinent to some of the steps can be found in the reference sources listed on last page.

DESIGN STEPS:

1. Choose the type of function (low-pass, bandpass, etc.), type of response (Butterworth, Bessel, etc.), number of poles, and cutoff frequency based on the particular application.

   If the transfer function is band-reject see Band-Reject Transfer Function before proceeding to step 2.
2. Determine the normalized low-pass filter parameters (f_n and Q) based on the type of response and number of poles selected in step 1. See Normalized Low-Pass Parameters.
3. If the actual response desired is low-pass go to step 4. For other responses a transformation of variables must be made (low-pass to bandpass or low-pass to high-pass). See Low-Pass Transformation.
4. Determine the actual (denormalized) cutoff frequency, f_o, by multiplying f_n by the actual desired cutoff frequency. See Denormalization of Parameters.
5. Pick the desired UAF configuration (noninverting, inverting or bi-quad) see Configuration Selection Guide and UAF41 Configuration and Design Equations.
6. Decide whether to use design equations "A" or "B". See Design Equations "A" and "B".
7. Calculate R_{F1} and R_{F2}. See Natural Frequency and UAF Configurations and Design Equations.
8. Determine Q_P. See Q_P Procedure.
9. Select the desired gain for each UAF and calculate the corresponding R_G and R_Q. See Gain (A) and UAF41 Configurations and Design Equations.

NORMALIZED LOW-PASS PARAMETERS

Usual active filter design procedure involves using normalized low-pass parameters. Table I is provided to assist in this step for the more common filter responses. Table II is a BASIC program which allows f_n and Q to be calculated for any desired ripple and number of poles for the Chebyschev response. Consult the reference on last page for other information.

Note that for bandpass and high-pass filters, complex conjugate pole pairs in the actual filter correspond to single poles in the normalized low-pass model. Thus **four poles** in Table I would correspond to **four-pole pairs** (eight poles) in a bandpass or high-pass filter.

Filters with an odd number of poles show one f_n with no corresponding Q value. This represents a simple RC network that is required for odd pole filters. This RC network with a cutoff frequency equal to f_n times the overall filter cutoff frequency should be placed in series with the first UAF two-pole section. The uncommitted internal op amp with an external RC network can be used for this purpose.

The cutoff frequency determined by the Table I filter parameters is (1) the -3dB frequency of the Butterworth response and of the Bessel response and (2) the frequency at which the amplitude response of the Chebyschev filters passes through the maximum ripple band (to enter the stop band). A filter that is designed as a low-pass filter will not give the corresponding response as a band-pass filter.

TABLE I. Low-Pass Filter Parameters.

NUMBER OF POLES	BUTTERWORTH		BESSEL		CHEBYSCHEV 0.5dB RIPPLE		CHEBYSCHEV 2dB RIPPLE	
	fn(1)	Q	fn(1)	Q	fn(2)	Q	fn(2)	Q
2	1.0	0.70711	1.2742	0.57735	1.23134	0.86372	0.907227	1.1286
3	1.0	----	1.32475	----	0.626456	----	0.368911	----
	1.0	1.0	1.44993	0.69104	1.068853	1.7062	0.941326	2.5516
4	1.0	0.54118	1.43241	0.52193	0.597002	0.70511	0.470711	0.9294
	1.0	1.3065	1.60594	0.80554	1.031270	2.9406	0.963678	4.59388
5	1.0	----	1.50470	----	0.362320	----	0.218308	----
	1.0	0.61805	1.55876	0.56354	0.690483	1.1778	0.627017	1.77509
	1.0	1.61812	1.75812	0.91652	1.017735	4.5450	0.97579	7.23228
6	1.0	0.51763	1.60653	0.51032	0.396229	0.68364	0.31611	0.9016
	1.0	0.70711	1.69186	0.61120	0.768121	1.8104	0.730027	2.84426
	1.0	1.93349	1.90782	1.0233	1.011446	6.5128	0.982828	10.4616
7	1.0	----	1.68713	----	0.256170	----	0.155410	----
	1.0	0.55497	1.71911	0.53235	0.503863	1.0916	0.460853	1.64642
	1.0	0.80192	1.82539	0.66083	0.822729	2.5755	0.797114	4.11507
	1.0	2.2472	2.05279	1.1263	1.008022	8.8418	0.987226	14.2802
8	1.0	0.50980	1.78143	0.50599	0.296736	0.67657	0.237699	0.89236
	1.0	0.60134	1.83514	0.55961	0.598874	1.6107	0.571925	2.5327
	1.0	0.89998	1.95645	0.71085	0.861007	3.4657	0.842486	5.58354
	1.0	2.5629	2.19237	1.2257	1.005984	11.5305	0.990142	18.6873

(1) -3 dB Frequency
(2) Frequency at which amplitude response passes through the ripple band.

NORMALIZED LOW-PASS CHEBYSCHEV

Table II gives a BASIC program for the determination of f_n and Q for a general normalized Chebyschev low-pass filter of any ripple and number of poles. Program inputs are the number of poles (N) and the peak-to-peak ripple (R). Program outputs are f_n and Q, which are used exactly as the values taken from Table I.

BAND-REJECT TRANSFER FUNCTION

The band-reject is achieved by summing the high-pass and low-pass UAF outputs. Either of the configurations in Figures 3 and 4 can be used to provide the band-reject function if they are used as shown in Figure 2.

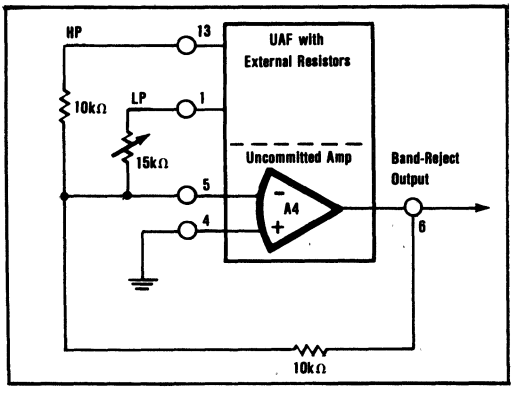
The 15kΩ resistor is adjusted for maximum rejection. The circuit in Figure 2 is applicable when using design equations "A" ($A_{LP} = A_{HP}$). When design equations "B" are used ($A_{LP} = 10A_{HP}$), the resistor at pin 1 must be 10 times the resistor at pin 13 to obtain equal pass-band gains above and below f_n.

In either case, the four external UAF resistors (R_G, R_Q, R_{F1} and R_{F2}) should be calculated for f_o and Q of the

band-reject filter desired and for A_{LP} to equal the desired pass-band gain. An input constraint is that the input voltage times A_{BP} must not exceed the rated peak-to-peak voltage of the bandpass output, or clipping will result. Note that the band-reject function is suitable only for a single UAF section. In a multi-section filter the inputs to successive stages are "preconditioned" by the preceding stages.

TABLE II. Low-Pass Chebyschev Program.

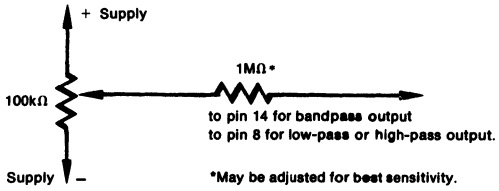
```
110 REM THIS IS A NORMALIZED LOW-PASS CHEBYSCHEV PROGRAM
120 REM BY BARRY A. EHRMAN
130 PRINT "NORMALLIZED CHEBYSCHEV"
140 PRINT "LOW-PASS FILTER"
150 PRINT
160 PRINT "BY BARRY A. EHRMAN"
170 PRINT
180 PRINT
185 PI=3.1415927
190 PRINT "NUMBER OF POLES?"
200 INPUT N
210 PRINT
220 PRINT "PEAK-TO -PEAK RIPPLE IN DB?"
230 INPUT R
240 PRINT
250 A=SQR(EXP(R/4.3429448)-1)
260 B=1/A
270 AN=LOG(B+SQR(B^2+1))
280 AN=AN/N
290 L=INT(N/2)
300 J=INT((N+1)/2)
310 FOR K=1 TO J
320 RP=((EXP(AN)-EXP(-AN))/2)*SIN(PI*((2*K)-1)/(2*N))
330 XIP=((EXP(AN)+EXP(-AN))/2)*COS(PI*((2*K)-1)/(2*N))
340 WN=SQR(RP^2+XIP^2)
350 Q=WN/(2*RP)
360 IF L<>J AND K=J THEN 410
370 PRINT "FN= ";WN
380 PRINT "Q = ";Q
390 PRINT
400 GOTO 430
410 PRINT "FN= ";WN
420 PRINT "Q =  RC POLE "
430 NEXT K
440 END
```



OFFSET ERROR ADJUSTMENT

DC offset errors will be minimized by grounding pin 3 through a resistor equal to 1/2 the value of R_{F1} or R_{F2}. The DC offset adjustment shown here may be used if required.

Offset errors will increase with increases in R_F.



LOW-PASS TRANSFORMATION

LOW-PASS TO HIGH-PASS

The following simple transformation may be used for high-pass filters:

$$f_n \text{ (high-pass)} = \frac{1}{f_n \text{ (low-pass)}}$$

$$Q \text{ (high-pass)} = Q \text{ (low-pass)}$$

LOW-PASS TO BANDPASS

The low-pass to bandpass transformation to generate f_n (bandpass) and Q (bandpass) is much more complicated. It is tedious to do by hand but can be accomplished with the BASIC program given in Table III. This program automates the transformation

$$s = p/2 \pm \sqrt{(p/2)^2 - 1}.$$

TABLE III. Low-Pass to Bandpass BASIC Transformation Program. (See last page of this PDS).

PROGRAM INPUTS:

1. f_n - From Table I for the low-pass filter of interest
2. Q - From Table I
3. Q_{BP} - Desired Q of the bandpass filter

For filters with an odd number of poles a Q of 0.5 should be used where Q is not given in Table I. Enter 10^5 for Q when transforming zeros on the imaginary axis.

The program transforms each low-pass pole into a bandpass pole pair. Thus a three-pole low-pass input, would result in the pole positions for a three-pole pair bandpass filter requiring three UAF stages.

DENORMALIZATION OF PARAMETERS

Table I shows filter parameters for many 2- to 8-pole normalized low-pass filters. The Q and the normalized undamped natural frequency, f_n for each two-pole section are shown. The Q values do not have to be denormalized and may be used directly as described in the Design Procedure Summary. f_n must be denormalized by multiplying it by the desired cutoff frequency of the actual overall filter to obtain the required frequency, f_o for the design formulas. As an example, consider a 4-pole low-pass Bessel filter with a cutoff frequency of 1000Hz. The first stage would be designed to an f_o of 1432.41Hz and a Q of 0.52193 while the second stage would have an f_o of 1605.94Hz and a Q of 0.80554. To combine the two stages into the composite filter the low-pass output of the first stage (pin 1) would be connected to the input resistors (R_G) of the second stage.

DESIGN EQUATIONS "A" AND "B"

1. For f_o below 8kHz, either of equations "A" or "B" may be used.
2. For f_o above 8kHz, equations "B" must be used. If equations "A" were used above 8kHz, the filter could become unstable.
3. Equations "A" are for the UAF as it is supplied. When using equations "B", a 5.49kΩ resistor must be placed in parallel with R_2 (between pins 12 and 13).
4. The values of R_{F1} and R_{F2} calculated with equations "B" are approximately one-third of those calculated with equations "A". Thus there may be an advantage in using equation "B" at low frequencies. Using equation "B" would require use of one more resistor, but that would not alter or affect filter performance in any manner.
5. Using the negative gain values for A_{LP} or A_{HP} or A_{BP} could result in the negative values for resistors R_G and R_Q. So the absolute value of the gain should always be used in the equations.

GAIN (A)

1. The gain (V/V) of each filter section is:
   A_{LP} - for low-pass output - gain at DC
   A_{BP} - for bandpass output - gain at f_o
   A_{HP} - for high-pass output - gain at high frequencies.
2. Refer to Performance Curves for full power response. When selecting the gain, insure that the limits of the curve are not exceeded for the desired voltage range.

NATURAL FREQUENCY (f_o)

1. f_o for each one pole-pair bandpass filter is the center frequency (f_C). f_C is defined as $f_C = \sqrt{f_1 f_2}$ where f_1 is the lower -3dB point and f_2 is the upper -3dB point of the pole pair response.
2. To obtain f_o below 100Hz using practical resistor values, capacitors may be paralleled with C1 and C2 to reduce the size of R_{F1} and R_{F2}. If capacitors are added in parallel,

$$R_{F1}\text{ (new)} = R_{F2}\text{ (new)} = R_{F1}\text{ (old)}\ \frac{1000pF}{C + 1000pF}$$

where R_F (new) is the new lower value frequency resistor, C is the value of the two external capacitors placed across C1 and C2 (between pins 7 and 8 and pins 1 and 14 and R_{F1} (old) is the value calculated in the simplified design equations.

Q-FACTOR

1. For bandpass filters $Q = \dfrac{f_o}{\text{3dB bandwidth}}$
2. When designing low-pass filters of more than two poles, best results will be obtained if the two pole sections with lower Q are followed by the sections with higher Q. This will eliminate any possibility of clipping due to high gain ripple in high Q sections.
3. Q repeatability (Q change from unit-to-unit) is typically ±5% for f_oQ products less than 10^4. The Q repeatability error increases as the f_oQ product increases to approximately ±10% for f_oQ products near 10^5.

Q_P PROCEDURE

1. If the "f_o times Q" product is greater than 10^5, it is possible for the measured filter Q to be different from the calculated value of Q. This effect is the result of non-ideal characteristics of operational amplifiers. It can be compensated for by introducing the parameter Q_P into the design equations.
2. Calculate the f_oQ product for the filter. If the product is above 10^5Hz, locate the corresponding f_oQ_P product in the Performance Curves. Divide f_oQ_P by f_o to obtain Q_P. Use Q_P as indicated in the design equations. For f_oQ products below 10^5Hz, Q_P = Q.

CONFIGURATION SELECTION GUIDE

It is possible to configure the UAF41 three different ways. Each configuration produces features that may or may not be desirable for a specific application. This selection guide is given to assist in determining the most advantageous configuration for a particular application.

	NONINVERTING INPUT	INVERTING INPUT	BI QUAD
Outputs Available	BP, LP and HP	BP, LP and HP	BP and LP
Outputs Inverted with respect to the Input	BP	HP and LP	BP and LP
Q & Gain Independent of Frequency Resistors?	Yes	Yes	No
Type of Q Variation With Changes in R_F	Constant Q	Constant Q	Constant Bandwidth
Other Advantages	May eliminate one external resistor (use internal R_3 as R_G)		R_G and R_Q are small at high frequencies. Easy single-supply operation.
Parameter Limitations	$2\,Q_p - A_{BP} > 1$ (Eqns. "A") $3.48\,Q_p - A_{BP} > 1$ (Eqns. "B")	$2\,Q_p + A_{BP} > 1$ (Eqns. "A") $3.48\,Q_p + A_{BP} > 1$ (Eqns. "B")	No HP Output

Summary: The Bi-Quad filter is particulary useful as a bandpass filter if the filter bandwidth must be kept constant as the center frequency is varied. If Q must be kept constant (i.e., constant Q of a bandpass or maintaining a constant response of a low-pass or high-pass) one of the other two configurations should be used. The Bi-Quad also has the advantage that R_G and R_Q are smaller than with the other two configurations (this is especially useful at high frequencies). The noninverting input configuration has the advantage that for $A_{BP} = 1$, $R_G = 50k\Omega$; therefore R_3 (internal) may be used so that only three external resistors are needed (R_{F1}, R_{F2}, R_Q). For single supply operation of the UAF41 in bi-quad filters, bias pin 3 and pin 11 to 1/2 $+V_{CC}$.

UAF41 CONFIGURATIONS AND DESIGN EQUATIONS

NONINVERTING INPUT CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$

2. $A_{BP} = Q\,A_{LP} = Q\,A_{HP}$

3. $R_G = \frac{5.0 \times 10^4\,Q}{A_{BP}\,Q_P}$

4. $R_Q = \frac{5.0 \times 10^4}{2Q_P - \frac{A_{BP}\,Q_P}{Q} - 1}$

SIMPLIFIED DESIGN EQUATIONS "B" †

Must be used for $f_o > 8kHz$

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$

2. $A_{BP} = \frac{Q}{3.16}\,A_{LP} = 3.16\,Q\,A_{HP}$

3. $R_G = \frac{5.0 \times 10^4\,Q}{A_{BP}\,Q_P}$

4. $R_Q = \frac{5.0 \times 10^4}{3.48Q_p - \frac{A_{BP}\,Q_P}{Q} - 1}$

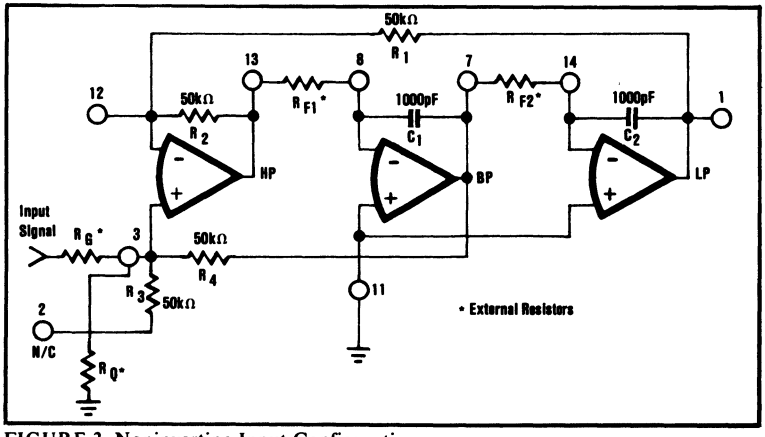


FIGURE 3. Noninverting Input Configuration.

INVERTING INPUT CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$

2 $A_{BP} = Q_P A_{LP} = Q_P A_{HP}$

3. $R_G = \frac{5.0 \times 10^4 Q_P}{A_{BP}}$

4 $R_Q = \frac{5.0 \times 10^4}{2Q_P + A_{BP} - 1}$

SIMPLIFIED DESIGN EQUATIONS "B" †

Must be used for $f_o > 8$kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$

2. $A_{BP} = \frac{Q_P}{3.16} A_{LP} = 3.16\, Q_P A_{HP}$

3. $R_G = \frac{1.58 \times 10^4 Q_P}{A_{BP}}$

4 $R_Q = \frac{5.0 \times 10^4}{3.48 Q_P + A_{BP} - 1}$

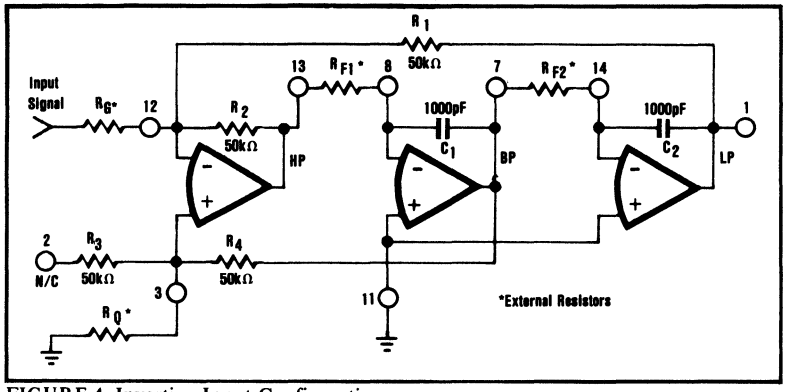


FIGURE 4. Inverting Input Configuration.

BI-QUAD CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

1 $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$

2 $A_{BP} = Q A_{LP}$

3 $R_Q = Q_P R_{F1}$ *

4. $R_G = \frac{R_Q}{A_{BP}}$

SIMPLIFIED DESIGN EQUATIONS "B" †

Must be used for $f_o > 8$kHz

1 $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$

2 $A_{BP} = 3.16\, Q A_{LP}$

3. $R_Q = 3.16\, Q_P R_{F1}$

4 $R_G = \frac{R_Q}{A_{BP}}$

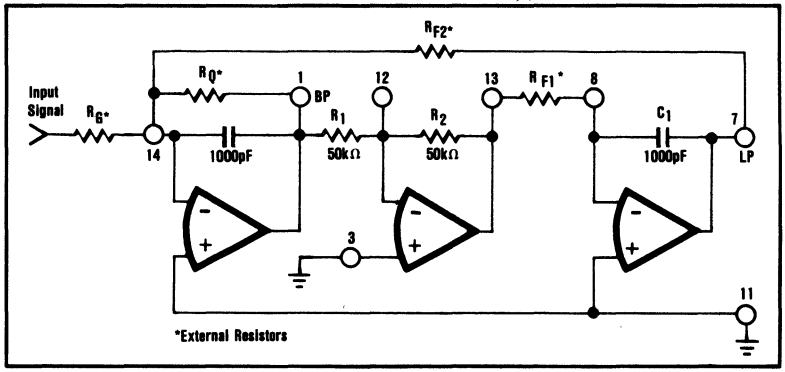


FIGURE 5. Bi-Quad Configuration.

† To use equations "B" connect a 5.49kΩ resistor between pins 12 and 13.
Equations "B" are also valid for frequencies below 8kHz.

DETAILED TRANSFER FUNCTION EQUATIONS

The following equations show the action of all the internal and external UAF41 filter components. They are not required for the regular design procedure but could be used if a detailed analysis is required.

NONINVERTING INPUT CONFIGURATION

1. $\omega_o^2 = \frac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = \frac{1 + \frac{R_4 (R_G + R_Q)}{R_G R_Q}}{1 + \frac{R_2}{R_1}} \left(\frac{R_2 R_{F1} C_1}{R_1 R_{F2} C_2}\right)^{1/2}$

3. $Q A_{LP} = Q A_{HP} \left(\frac{R_1}{R_2}\right) = A_{BP} \left(\frac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$

4. $A_{LP} = \frac{1 + \frac{R_1}{R_2}}{R_G \left(\frac{1}{R_G} + \frac{1}{R_Q} + \frac{1}{R_4}\right)}$

5. $A_{HP} = \frac{R_2}{R_1} A_{LP} = \frac{1 + \frac{R_2}{R_1}}{R_G \left(\frac{1}{R_G} + \frac{1}{R_Q} + \frac{1}{R_4}\right)}$

6. $A_{BP} = \frac{R_4}{R_G}$

INVERTING INPUT CONFIGURATION

1. $\omega_o^2 = \frac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = \left(1 + \frac{R_4}{R_Q}\right) \frac{1}{\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_G}\right)} \left(\frac{R_{F1} C_1}{R_1 R_2 R_{F2} C_2}\right)^{1/2}$

3. $Q A_{LP} = Q A_{HP} \left(\frac{R_1}{R_2}\right) = A_{BP} \left(\frac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$

4. $A_{LP} = \frac{R_1}{R_G}$

5. $A_{HP} = \frac{R_2}{R_1} A_{LP} = \frac{R_2}{R_G}$

6. $A_{BP} = \left(1 + \frac{R_4}{R_Q}\right) \frac{1}{R_G \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_G}\right)}$

BI-QUAD CONFIGURATION

1 $\omega_o^2 = \frac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

*2 $Q = R_Q C_2 \omega_o$

3. $A_{BP} = \frac{Q A_{LP}}{\omega_o R_{F2} C_2} = \frac{R_Q}{}$

ACTIVE FILTER DESIGN EXAMPLES USING THE DESIGN PROCEDURE OUTLINED IN DESIGN STEPS SECTION.

Example 1.

It is desired to design a three-pole, 0.5dB ripple, Chebyschev High-Pass Filter; the cutoff frequency f_c = 2kHz, Gain $A_{HP} = +1$.

Step 1.

The type of transfer function (high-pass), the type of response (Chebyschev), number of poles (3), and the cut off frequency (f_c) are chosen depending upon the particular application and are stated in the example.

Step 2.

Normalized low-pass filter parameters f_n and Q are obtained from Table I (or from program shown in Table II).

Complex Poles:
$f_n = 1.068853$
$Q = 1.7062$
Simple Pole:
$f_n = 0.626456$

Step 3.

Now, since the actual response desired is high-pass, the low-pass to high-pass transformation must be made as previously discussed in Low-Pass Transformation.

$$f_n \text{ (high-pass)} = \frac{1}{f_n \text{ (low-pass)}}, \quad Q_{HP} = Q_{LP}$$

$\therefore$ For Complex Poles:

$$f_n = \frac{1}{1.068853} = 0.935582$$

and Q = 1.7062

For Simple Pole: $f_n = \frac{1}{0.626456} = 1.596281$

Step 4.

Now, determine the actual (denormalized) frequency.
$f_o = f_c \times f_n = 2\text{kHz} \times 0.935582 = 1871.2\text{Hz}$

Step 5.

Refer to the Configuration Selection Guide. Since the gain required is positive, the HP output is not inverted with respect to the input. Therefore, the noninverting input configuration must be selected. Note that the HP output is not available with the Bi-Quad configuration.

Step 6.

Since $f_o < 8\text{kHz}$, Equations "A" would be used.

Step 7.

For the Complex Poles Stage of the filter, using the equations "A".

$$R_{F1} = R_{F2} = \frac{1.592 \times 10^8}{1871.2} = 85.08\text{k}\Omega$$

Step 8.

$f_o Q = 1871.2 \times 1.7062 = 3.19 \times 10^3$

$\therefore f_o Q < 10^5$

$\therefore Q_P = Q = 1.7062$

Step 9.

$A_{BP} = Q_P \times A_{HP} = 1.7062 \times 1 = 1.7062$

$$R_G = \frac{5.0 \times 10^4 \times 1.7062}{1.7062 \times 1.7062} = 29.3\text{k}\Omega$$

$$R_Q = \frac{5.0 \times 10^4}{2 \times 1.7062 - 1.7062 - 1} = 70.8\text{k}\Omega$$

The above obtained resistor values are for the complex pole pair of the first stage of the required active filter. The simple pole obtained as outlined below, using the uncommitted op amp in the UAF41 makes the second stage of the required filter.

For the simple pole f_n was obtained in step 3.

$f_n = 1.596281$

The actual (denormalized) frequency = $f_c \times f_n$

$= 2\text{kHz} \times 1.596281 = 3192.6\text{Hz}$

Now, $f = \frac{1}{2\pi RC}$

$$\therefore RC = \frac{1}{2\pi f} = \frac{1}{2\pi \times 3192.6} = 4.9851 \times 10^{-5}$$

Choosing C = 2200pF (or any convenient value),

$$R = \frac{4.9851 \times 10^{-5}}{2200 \times 10^{-12}} = 22.66\text{k}\Omega$$

Note:

R and/or C may be chosen in any convenient manner to obtain the desired RC product.

The overall circuit for the required filter is shown below:

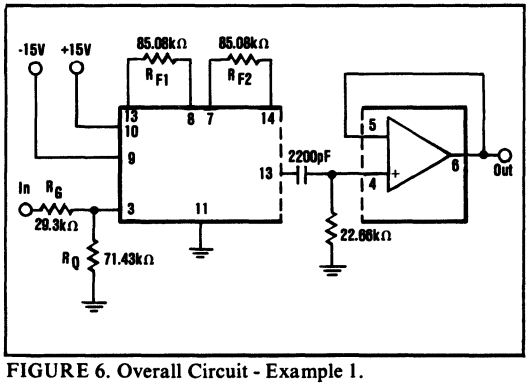


FIGURE 6. Overall Circuit - Example 1.

Example 2.

It is desired to design a 4-pole Butterworth, Bandpass Filter, with Q = 25, f_c = 19kHz and A_{BP} = 1.

Using the computer program shown in Table III, the following values of f_n and Q are obtained.

$$f_n = 1.0142435,\ Q = 35.36541$$

and

$$f_n = 0.9859565,\ Q = 35.35886$$

Using the above shown values of Q and f_n, we now will proceed to design the two stages of filter separately. Composite gain will be ≤1. Any one of the three configurations shown in the Configuration Selection Guide can be used. We will select the noninverting input configuration.

For Stage 1.

$f_o = 19kHz \times f_n = 19kHz \times 1.0142435 = 19270.6Hz$

Since $f_o > 8kHz$, equations "B" would be used.

$$R_{F1} = R_{F2} = \frac{5.033 \times 10^7}{19270.6} = 2.6118k\Omega$$

$$f_oQ = 19270.6 \times 35.36541 = 6.815136 \times 10^5$$

Since $f_oQ \geq 10^5$, locate the corresponding f_oQ_P from the Performance Curves.

Divide f_oQ_P by f_o to obtain Q_P.

Thus $Q_P = 48.78$

$$R_G = \frac{5.0 \times 10^4 \times 35.36541}{1 \times 48.78} = 36.25k\Omega$$

$$R_Q = \frac{5.0 \times 10^4}{3.48 \times 47.78 - \frac{48.78}{35.37} - 1} = 298.7\Omega$$

For Stage 2.

Following the same procedure as shown for Stage 1 above, the values shown below are obtained.

$f_oQ = 6.624 \times 10^5$, using the Performance Curves,

$Q_P = 48.04$

$R_{F1} = R_{F2} = 2.6867k\Omega$

$R_G = 36.8k\Omega$

and $R_Q = 303.4\Omega$

The overall circuit for the required filter is shown below.

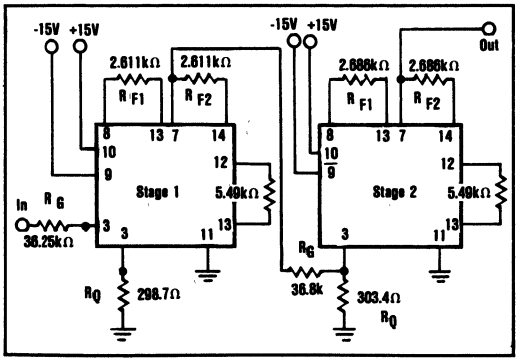


FIGURE 7. Overall Circuit - Example 2.

Example 3.

It is desired to design a 5-pole Bessel, Low-Pass Filter with f_c = 3.3kHz and A_{LP} = 1.

From Table I the following values of f_o and Q are obtained.

Complex Poles:

$f_n = 1.55876$, $Q = 0.56354$

$f_n = 1.75812$, $Q = 0.91652$

Simple Pole:

$f_n = 1.50470$

Using the above shown values of f_n and Q, we now will proceed to design the three stages of filter separately.

Any one of the three configurations can be used. We will select inverting configuration.

For Stage 1.

$f_o = 3.3kHz \times f_n = 3.3kHz \times 1.55876 = 5144Hz$

Since $f_o < 8kHz$, equations "A" would be used.

$$R_{F1} = R_{F2} = \frac{1.592 \times 10^8}{5144} = 30.95k\Omega$$

$$f_oQ = 5144 \times 0.56354 = 2.9 \times 10^3$$

$f_oQ < 10^5$, $\therefore Q_P = Q = 0.56354$

$A_{BP} = Q_P\ A_{LP} = 0.56354 \times 1 = 0.56354$

$$R_G = \frac{5 \times 10^4 \times 0.56354}{0.56354} = 50k\Omega$$

$$R_Q = \frac{5 \times 10^4}{2 \times 0.56354 + 0.56354 - 1} = 72.4k\Omega$$

For Stage 2.

$f_o = 3.3kHz \times f_n = 3.3kHz \times 1.75812 = 5802Hz$

Since $f_o > 8kHz$, equations "A" would be used.

$$R_{F1} = R_{F2} = \frac{1.592 \times 10^8}{5802} = 27.44k\Omega$$

$$f_oQ = 5802 \times 0.91652 = 5.32 \times 10^3$$

$f_oQ > 10^5$, $\therefore Q_P = Q = 0.91652$

$A_{BP} = Q_P\ A_{LP} = 0.91652 \times 1 = 0.91652$

$$R_G = \frac{5 \times 10^4 \times 0.91652}{0.91652} = 50k\Omega$$

$$R_Q = \frac{5 \times 10^4}{2 \times 0.91652 + 0.91652 - 1} = 28.58k\Omega$$

For Stage 3.

$f = 3.3kHz \times f_n = 3.3kHz \times 1.50470 = 4966Hz$

For the simple pole,

$$RC = \frac{1}{2\pi f} = \frac{1}{2\pi \times 4966} = 3.2049 \times 10^{-5}$$

3300pF (or any convenient value)

$$R = \frac{3.2049 \times 10^{-5}}{3300 \times 10^{-12}} = 9.71k\Omega$$

The overall circuit is shown below.

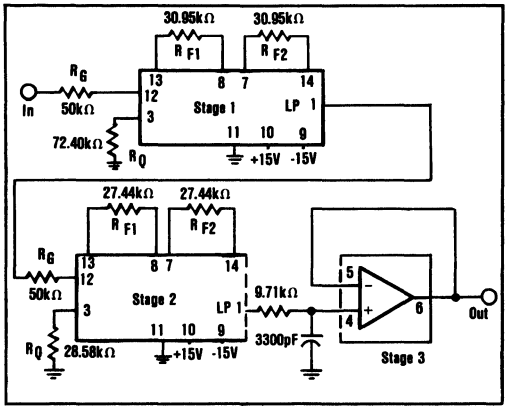


FIGURE 8. Overall Circuit - Example 3.

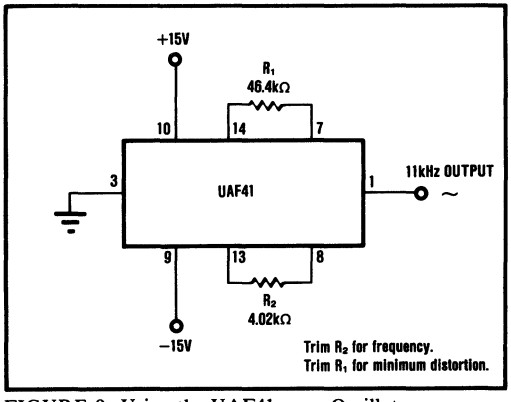


FIGURE 9. Using the UAF41 as an Oscillator.

USEFUL REFERENCES

1. G.E. Tobey, J.G. Graeme and L.P. Huelsman, Operational Amplifiers: Design and Applications, (Chapter 8) McGraw Hill Book Co., 1971.
2. Yu Jen Wong, William E. Ott, Function Circuits: Design and Applications, (Chapter 6) McGraw Hill Book Co., 1976.
3. Richard W. Daniels, Approximation Methods for Electronic Filter Design, McGraw Hill Book Co., 1974.
4. Anatol I. Zverev, Handbook of Filter Synthesis, John Wiley and Sons Inc., New York, N.Y., 1967
5. Gabor C. Temes, Sanjit K. Mitra, Modern Filter Theory and Design, John Wiley and Sons, New York, N.Y., 1973

TABLE III. Low-Pass to Bandpass BASIC Transformation Program.

```
20  INPUT "FN, Q, AND Q(BANDPASS)";F,Q,QBP
30  Y=F*SQR(1-(1/(2*Q))^2)
40  X= -F/(2*Q)
50  PX=X:PY=Y
60  FOR I= 1 TO 2
70  SX=PX/(2*QBP):SY=PY/(2*QBP)
80  PX=(SX^2-SY^2)-1:PY=2*SX*SY
90  T=ATN(PY/PX)
95  T=T-3.1415926#
100 IF T >0 THEN 120
110 T = 2*3.1415926# + T
120 T=T/2
130 A=SQR(SQR(PX^2 + PY^2))*COS(T)
140 B=SQR(SQR(PX^2 + PY^2))*SIN(T)
150 SX=SX+A:SY=SY+B
160 F=SQR(SX^2 +SY^2)
170 Q= -F/(2*SX)
180 PRINT "FN=";F;"Q=";Q
190 IF Y=O THEN 220
200 PX=X:PY= -Y
210 NEXT I
220 STOP
230 END
```

BURR-BROWN®

4085

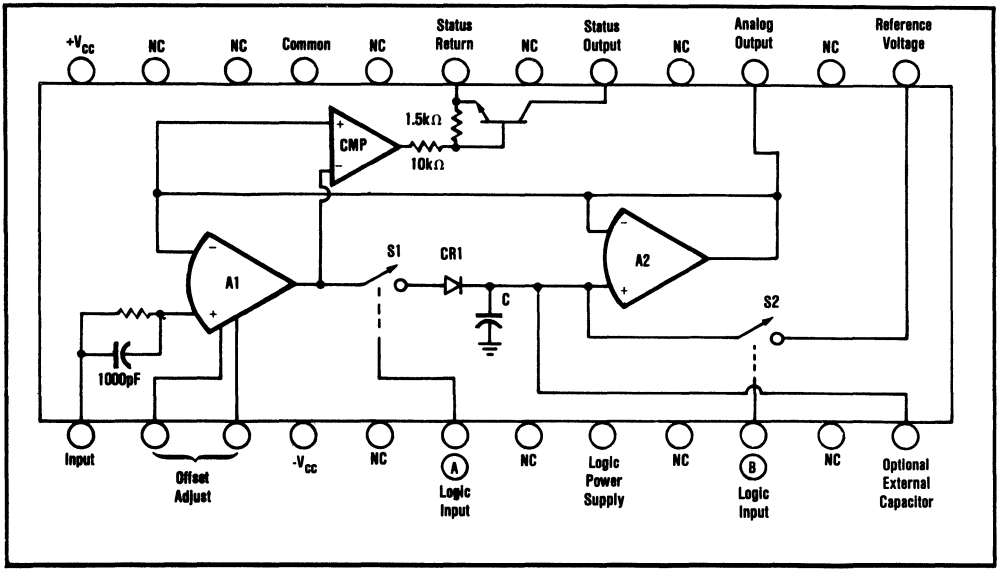
HYBRID MICROCIRCUIT PEAK DETECTOR

FEATURES:

- STORES TRANSIENT VOLTAGES
- COMPLETELY SELF-CONTAINED
- ACCURATE TO ±0.01%
- LOW DROOP ERRORS
- SMALL DIP PACKAGE

DESCRIPTION

The 4085 is a specialized sample/hold amplifier that tracks an input signal until a maximum amplitude is reached. That maximum value is held at the analog output, and the digital Status output indicates that a peak has been detected. The unit can then be commanded to hold that value, ignoring additional peaks, or reset to a user-specified reference voltage. The 4085 detects positive-going peaks from -10V to +10V and is available in a hermetic metal package and a low-cost ceramic package. Three models are available, specified for temperature ranges 0 to +70°C (4085KG), -25°C to +85°C (4085BM), and -55°C to +125°C (4085SM).



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-379A

SPECIFICATIONS

ELECTRICAL

Specification at T_A = +25°C and ±15VDC and +5VDC power supplies unless otherwise noted

MODEL	4085 MIN	4085 TYP	4085 MAX	UNITS
ANALOG INPUT				
Signal Inputs				
Operating Range	±10	|Vcc|-3		V
Absolute Maximum Range			±Vcc	V
Input Offset Voltage (adjustable to zero)			2	mV
Input Offset Voltage Drift		15	50	µV/°C
Input Bias Current		15	50	pA
Input Resistance		1		GΩ
Input Capacitance		8		pF
DIGITAL INPUT				
Logic Levels				
Logic "1"	+2 4 at 50nA, max			V
Logic "0"			+0 8 at 100µA, max	V
Truth Table	Logic Input A		Logic Input B	
Peak Detect Mode	1		0	
Hold Mode	0		0	
Reset	0		1	
TRANSFER CHARACTERISTICS				
Voltage Gain		1 0		V/V
ACCURACY				
DC Voltage Gain Error			±0 01	% of FSR(1)
Dynamic Accuracy to 300Hz		±0 01	±0 02	% of FSR
Dynamic Accuracy to 100Hz			±0 01	% of FSR
Temperature Coefficient of Gain Error		±3		ppm/°C
Feedthrough			±0 05	% of Step
Droop (all units at T_A = +25°C)(2)			±0 06	mV/msec
T_A = +70°C, 4085KG			±0 5	mV/msec
T_A = +85°C, 4085BM			±1 2	mV/msec
T_A = +125°C, 4085SM			±12 0	mV/msec
Power Supply Sensitivity, ±Vcc			±0 005	%/% Supply Variation
Logic Supply			±0 005	%/% Supply Variation
DYNAMIC PERFORMANCE				
Acquisition Time (BM, SM)			500	µsec
Acquisition Time (KG)			800	µsec
Slew Rate		0 5		V/µsec
Charge Offset(3)		0 5	1	mV
Status Delay at 500Hz		0 7	1	msec
Status Delay at 100Hz		1 2	2	msec

MODEL	4085 MIN	4085 TYP	4085 MAX	UNITS
ANALOG OUTPUT				
Voltage Range	±10	|Vcc|-3		V
Output Current	5			mA
Output Resistance		0 2	0 5	Ω
Output Noise 10Hz to 100kHz		30		µV, rms
Output Load Capacitance	50	100		pF
STATUS OUTPUT				
Collector-emitter Voltage			+30	V
Collector Current			20	mA
DC Current Gain	50	100		mA/mA
V_{BE}		0 65		V
REFERENCE VOLTAGE				
Operating Range	±10	|Vcc|-3		V
Absolute Maximum Range			±Supply	V
Discharge Current(4)	5		30	mA
POWER SUPPLY REQUIREMENTS				
Rated Voltage		±15		V
Operating Range	±8		±18	V
Current Drain (I_{OUT} = 0)			±20	mA
Rated Logic Supply Voltage(5)		+5 0 ±0 5		V
Logic Supply Current				
(Logic A & B high)		3 0 ±0 3		mA
(Logic A & B = 0V)		4 4 ±0 5		mA
TEMPERATURE RANGE				
Specification				
4085KG	0		+70	°C
4085BM	-25		+85	°C
4085SM	-55		+125	°C
Operating				
4085KG	-25		+85	°C
4085BM	-55		+90	°C
4085SM	-55		+125	°C
Storage				
4085KG	-30		+90	°C
4085BM	-60		+100	°C
4085SM	-60		+150	°C

NOTES

1 FSR = Full Scale Range, 20V for the 4085

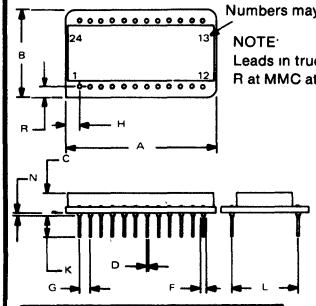
2. Equation for droop. Droop (mV/msec) = $$\frac{100pA \times 2^{\left(\frac{T - 25°C}{11}\right)}}{3300pF + C_{EXT}\ (pF)}$$

3 Charge Offset is the charge transferred from the holding capacitor when the 4085 is switched to the hold mode

4 Any circuitry connected to the reference pin should be capable of sinking the desired discharge current of the internal 3300pF holding capacitor plus any external capacitor The discharge current range is the current limit imposed by an internal FET switch It does not imply that the I_{DSS} of external circuitry must be designed to limit current to this range

5. Logic Supply, pin 8, may be connected to higher supply voltages for operation with MOS or CMOS logic. Refer to "Operating Instructions"

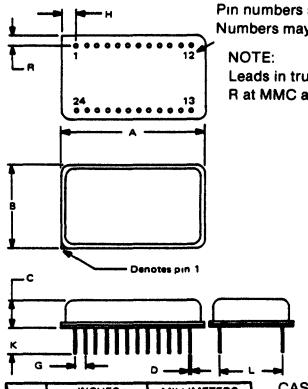
MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	.085	.105	2.16	2.67

ORDER NUMBER
4085KG

CASE: Black Ceramic (alumina)
MATING CONNECTOR: 245MC
WEIGHT: 8.4 grams (0.3 oz)

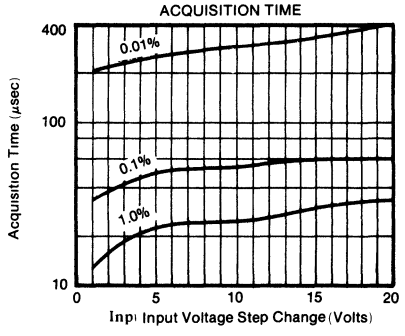


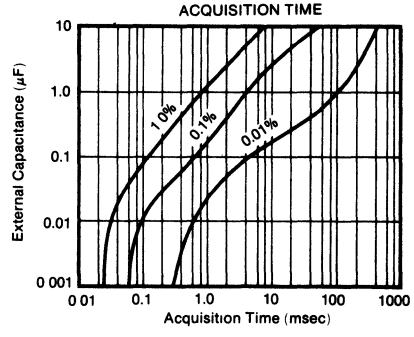
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

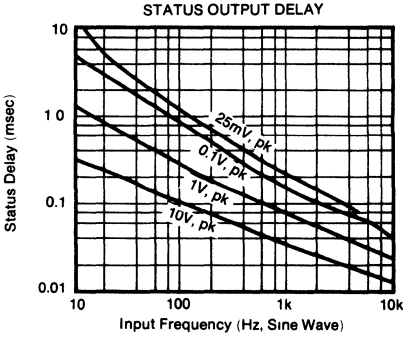
ORDER NUMBER:
4085BM
4085SM

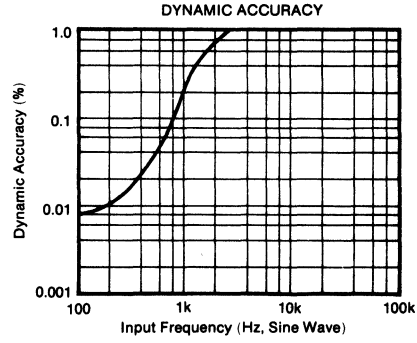
CASE: Kovar, Gold or Nickel plated
MATING CONNECTOR: 245MC
WEIGHT: 8.4 grams (0.3 oz)

TYPICAL PERFORMANCE CURVES









THEORY OF OPERATION

In the Peak Detect Mode (S1 closed, S2 open), the analog output tracks the analog input until a peak value is reached. When the input voltage falls below the magnitude of the peak voltage, CR1 becomes reversed biased, and the feedback loop between A1 and A2 is broken. At this point, the status output transistor turns on and the magnitude of the peak voltage is held on the analog output. In the Hold Mode (S1 open, S2 open), the current charging path from the output of A1 to the capacitor is opened. The output voltage is equal to the voltage stored in the capacitor even though the input voltage may become larger than the peak voltage. In the Reset Mode (S1 open, S2 open), the voltage on the capacitor will charge to whatever voltage is applied to the reference voltage input. If both S1 and S2 are closed at the same time, the output of A1 will be connected to the reference voltage input through a low impedance. This represents an illegal mode of operation, but will cause no damage to the unit.

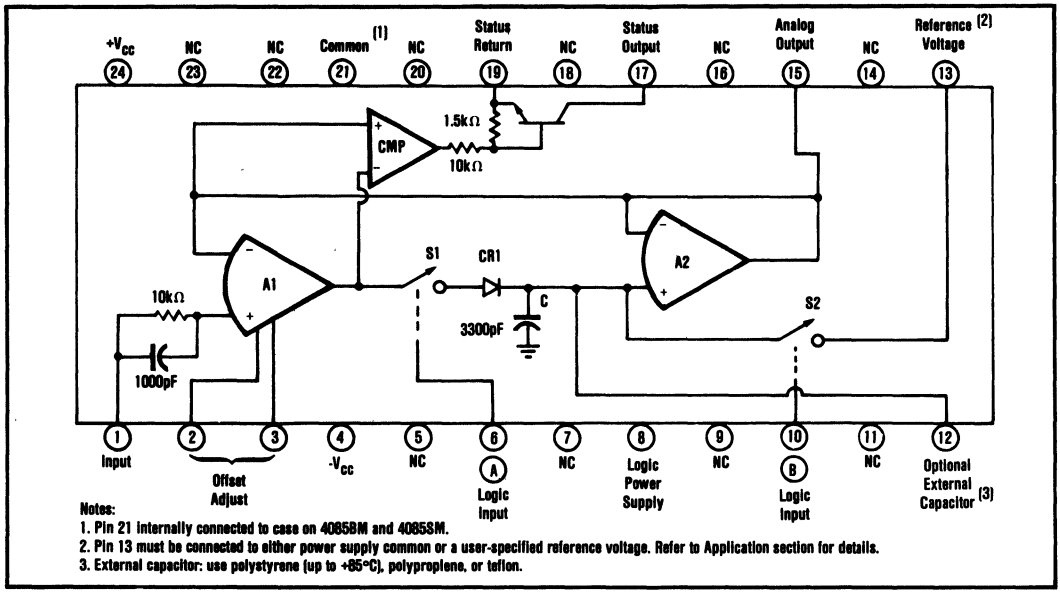


FIGURE 1. 4085 Functional Diagram and Pin Configuration.

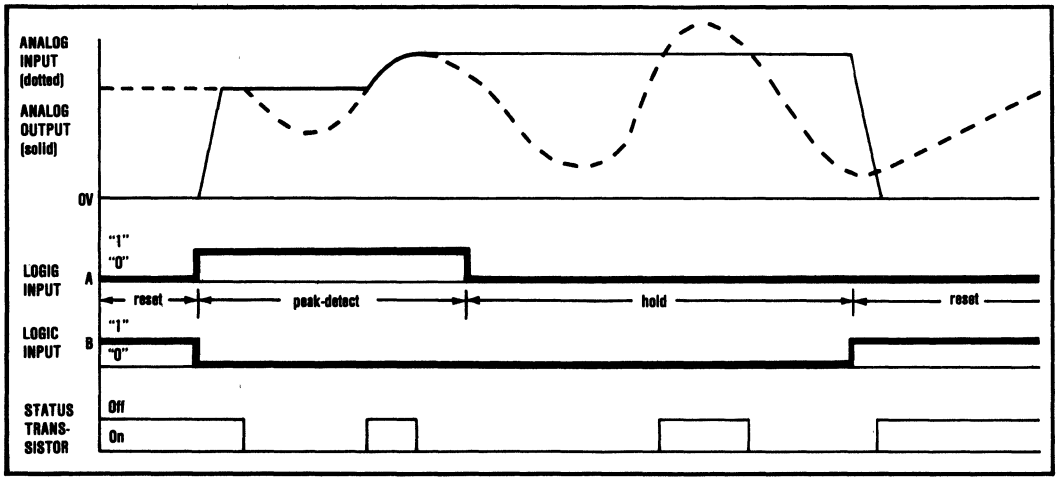


FIGURE 2. Timing Diagram For Peak-Detect Operation.

OPERATING INSTRUCTIONS

OFFSET VOLTAGE ADJUSTMENT

The ±2mV input offset voltage of the 4085 may be nulled to zero by using the circuit shown in Figure 3. With the 4085 in the Peak Detect Mode (logic input A = "1", logic input B = "0") apply zero volts to pin 1. Adjust the potentiometer until the output voltage is zero volts. Disconnect pin 12 after adjustment is made.

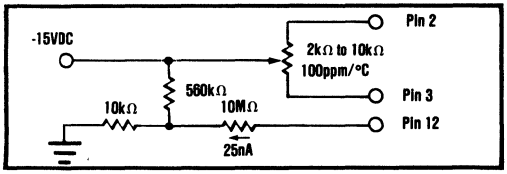


FIGURE 3. Offset Adjust Circuit.

POWER SUPPLY CONSIDERATIONS

The 4085 will operate as specified with power supplies from ±8VDC to ±18VDC. To minimize noise pickup, the supply inputs should be decoupled with 1μF tantalum capacitors located physically close to the unit.

DIGITAL INPUTS AND LOGIC SUPPLY

The digital inputs may be driven with TTL or CMOS logic. Pin 8 should be tied to the logic supply. The logic supply voltage (V_L) may also be provided by connecting pin 8 through a resistor of value R (kΩ) = 1.67 (V_{CC} - V_L)/V_L to the +V_{CC} ($V_{CC} \geq V_L$). The logic threshold voltage is equal to 0.4V_L - 0.7V.

INPUT FREQUENCY BANDWIDTH LIMITING

It is recommended that the input bandwidth be limited as much as possible by an RC section such as that shown in Figure 4. This is to limit noise spikes at the input that may cause erroneous readings. If detecting large pulse heights, a 5μsec time constant should be used. This will not degrade acquisition time or tracking accuracy for frequencies up to 500Hz. For input frequencies greater than 500Hz, a smaller time constant may be used.

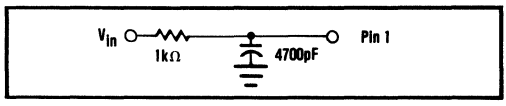


FIGURE 4. Input Bandwidth Limiting.

STATUS OUTPUT CHARACTERISTICS

The open-collector, open-emitter output transistor is a small signal, medium speed switching transistor similar to a 2N2222. To facilitate driving a variety of devices, the configuration of the status output has been left to the user's discretion.

The internal comparator shown in the block diagram (Figure 1) has an output characteristic as follows. Input signal track: $Z_{out} \approx \infty$; peak hold: V_{out} = +V_{CC} - 0.5V.

Several configurations are illustrated in Figures 5, 6, and 7. "Inverting" means logic "0" = peak has been detected. "Noninverting" means logic "1" = peak has been detected.

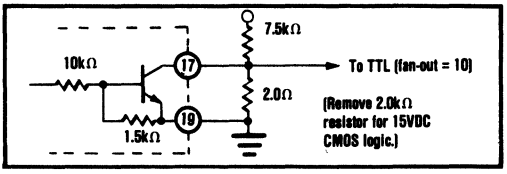


FIGURE 5. Inverting TTL (CMOS) Status Output.

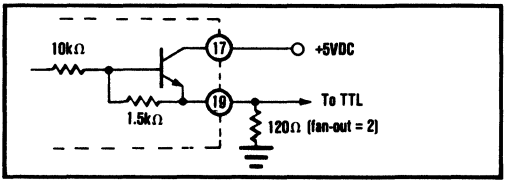


FIGURE 6. Noninverting TTL Status Output.

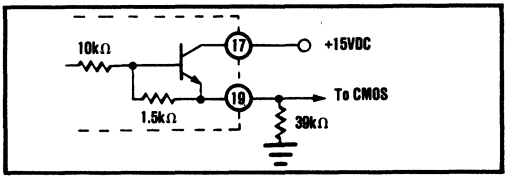


FIGURE 7. Noninverting CMOS Status Output.

DESIGNING IN HYSTERESIS

It may be desirable in some situations to have hysteresis in the circuit such that small peaks will not be detected, eliminating jitter in the Status output. This is possible through external components connected as shown in Figure 8. After a peak is detected, the input voltage must be slightly greater (determined by R1/R2) than the previous peak to cause the output to resume tracking the input. This hysteresis voltage is expressed by:

$$V_H = \frac{(V_{in} - V_E - 0.9V)\,R1}{R1 + R2}$$

The emitter voltage of the status transistor should be tied to a voltage sufficiently lower than the lowest expected peak to allow proper operation.

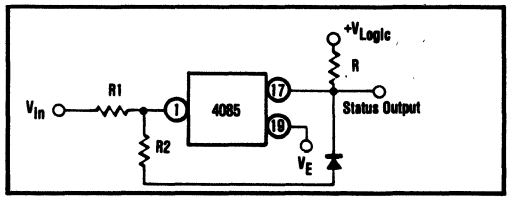


FIGURE 8. Hysteresis.

APPLICATIONS

PEAK CATCHER

This circuit detects and holds the first peak it encounters. After the first peak is detected, it automatically is switched to the Hold Mode. To reset the circuit for catching another peak, a 10μsec or longer positive logic pulse should occur at the Release Input. This will reset the peak detector to the desired voltage and put it in the peak-detect mode.

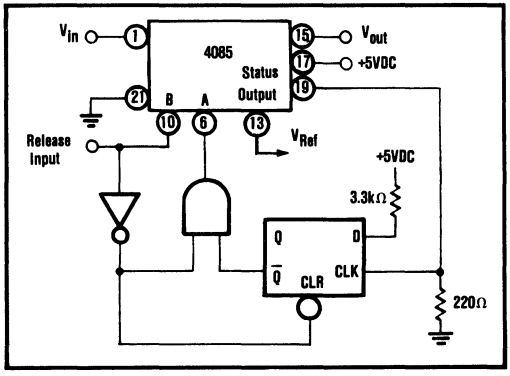


FIGURE 9. Peak Catcher.

NO-RIPPLE, FAST-SETTLING RMS-DC CONVERTER

If a waveform is known, the rms value of the signal may be computed from the peak value. In this circuit, the rms value is computed by the output amplifier from the peak value held by the 4085. The output in the circuit shown is updated manually. It may be updated automatically by replacing the switch circuit with an oscillator plus timing logic.

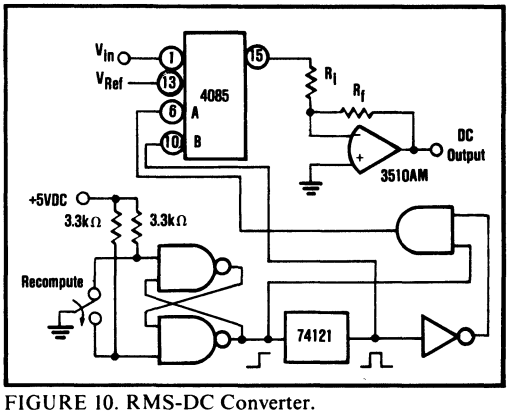


FIGURE 10. RMS-DC Converter.

INTERFACING TO A/D CONVERTER

Interfacing to an A/D converter is straightforward. The gating of the A/D converter command allows a conversion only if a peak has been detected and permits completion of each conversion. If a peak occurs while the A/D is converting, it will not be detected.

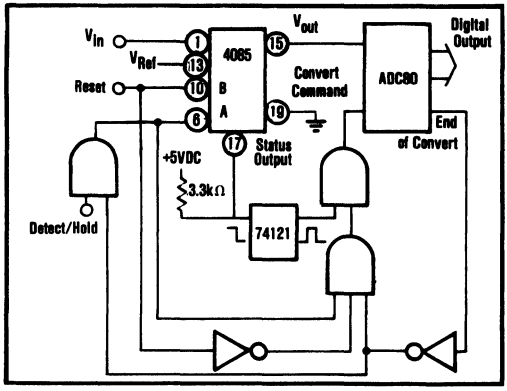


FIGURE 11. A/D Converter Interface.

PEAK-TO-PEAK DETECTOR

Figure 12 shows a circuit that will display the peak-to-peak voltage of an input waveform. The Status Output indicates that both positive and negative peaks have been detected and that the output is valid. The resistors around A3 should be matched to insure good common-mode rejection.

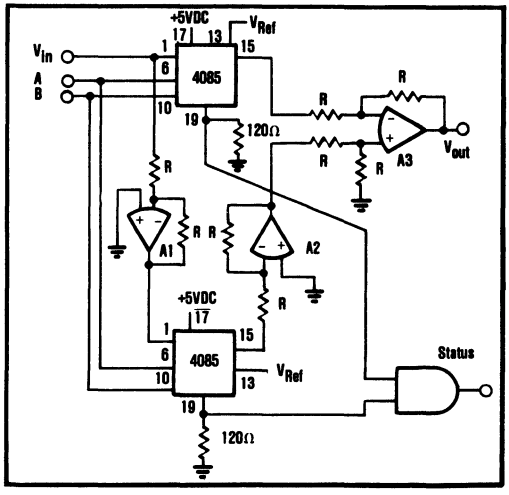


FIGURE 12. Peak-to-Peak Detector.

REFERENCE VOLTAGE

In the Reset Mode the voltage applied to pin 13 places an initial charge on the holding capacitor at the input to A2 (see Figure 1). This threshold voltage may be any value between positive and negative 10 volts. For most applications pin 13 will be tied to power supply common. This sets V_{Ref} to 0 volts. The 4085 will then capture peaks greater than 0 volts.

Pin 13 must be connected to either power supply common or to a user-specified reference voltage. If this connection is not made the 4085 will appear to have excessive droop.

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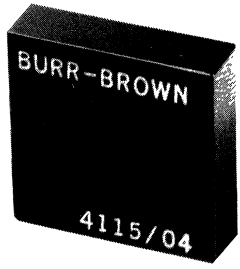


4115/04

WINDOW COMPARATOR

FEATURES

- ADJUSTABLE LIMITS FOR "HIGH", "LOW", AND "GO"
- UP TO 200mA LOAD CAPABILITY (each output)
- INPUT PROTECTION

APPLICATIONS

- PRODUCTION LINE TESTING
- TEMPERATURE CONTROLS
- INDUSTRIAL ALARMS
- LEVEL DETECTORS/CONTROLS

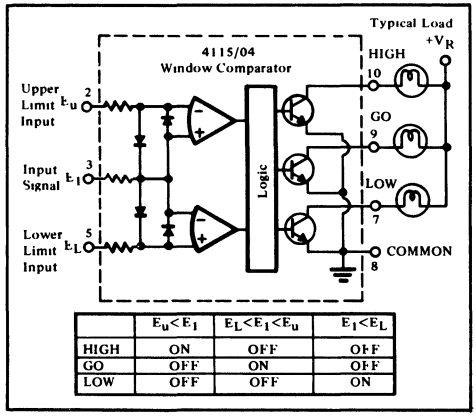
DESCRIPTION

Model 4115/04 is a hybrid IC window comparator in a double width DIP. The unit has three inputs - one for a voltage that sets the upper limit, another for a voltage that sets the lower limit, and a signal input. There are three mutually exclusive outputs - HIGH, LOW and GO. When an output is ON it will sink up to 200mA of current. This input diode protected device is designed to work with input voltages of up to ±10VDC, and will not be harmed by voltages to ±15VDC. The 4115/04 will drive a variety of loads including lamps, relays, MOS circuitry, and high noise immunity logic as well as DTL and TTL devices.

INSTALLATION

Separate connections should be made from each power supply common (+15VDC, -15VDC and V_R) to the 4115/04 common (pin 8).

To avoid unwanted pickup or chattering it may be necessary to include bypass capacitors from the ±15VDC supply pins (13 and 14) to the module common pin (8).



	$E_u<E_I$	$E_L<E_I<E_u$	$E_I<E_L$
HIGH	ON	OFF	OFF
GO	OFF	ON	OFF
LOW	OFF	OFF	ON

Model 4115/04 Transfer Characteristics.

International Airport Industrial Park • P.O. Box 11400 • Tucson, Arizona 85734 • Tel.: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491

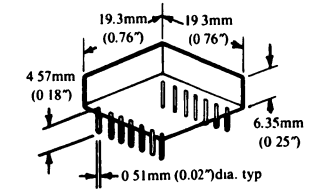
ELECTRICAL SPECIFICATIONS

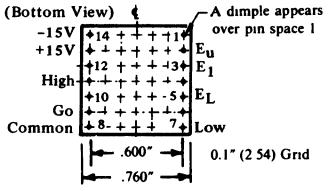
Typical performance at 25°C and with rated supply unless otherwise noted.

MODEL	4115/04	Units
INPUT		
All Inputs	±10V into 6kΩ (min)	
Maximum Safe Input	±15	V
ACCURACY		
D.C. Resolution (min)	±0.2	mV
Voltage Offset (referred to input)		
at 25°C (max)	±2	mV
vs Temperature (max)	±30	μV/°C
Over Temperature Range (max)	±7	mV
vs Power Supply	±50	μV/V
Switching Speed		
Total Switching Time at 30mV		
Overdrive	300	μsec
OUTPUT		
Impedance to COMMON from all Outputs		
OFF state	> 1	MΩ
ON state	3	Ω
Load Supply Voltage (V_R)	0 to +30	V
Load Current		
Steady State	+200	mA
Transient (absolute maximum)		
1 Second Duration	+400	mA
Saturation Voltage (V_{CE}) (max)		
at 200mA	0.7	V
TEMPERATURE RANGE		
Rated Specifications	-25 to +85	°C
Derated Performance	-40 to +85	°C
Storage	-55 to +100	°C
POWER SUPPLY REQUIREMENTS		
Rated Supply Voltage	±15	VDC
Derated Performance	±12 to ±18	VDC
Quiescent Drain (max)	±30	mA

To achieve best results use stable quiet reference sources and drive signal input from low impedance source. Noise and drift in input sources readily masks the inherently high resolution of the device.

MECHANICAL SPECIFICATIONS





WEIGHT 0.24 oz (6.80 grams)
MATERIAL Black Exoxy
PIN Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
CONNECTOR Fits any commercial dual-in-line connector

BURR-BROWN ®

4127

LOGARITHMIC AMPLIFIER

FEATURES

- **ACCEPTS INPUT VOLTAGES OR CURRENTS OF EITHER POLARITY**
- **WIDE INPUT DYNAMIC RANGE**
  6 Decades of current
  4 Decades of voltage
- **VERSATILE**
  Log, antilog, and log ratio capability
- **SMALL SIZE**
  Double wide DIP
- **LOW COST**

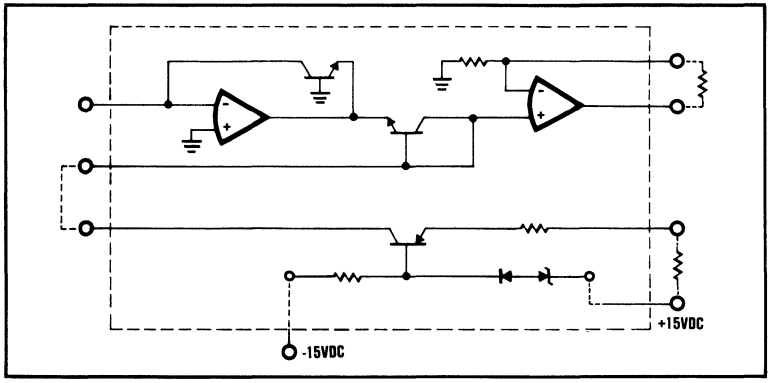
DESCRIPTION

Packaged in a ceramic double wide DIP, the 4127 is the first hybrid logarithmic amplifier that accepts signals of either polarity from current or voltage sources. A special purpose monolithic chip, developed specifically for logarithmic conversions, functions accurately for up to six decades of input current and four decades of input voltage. In addition, a newly developed current inverter and a precise internal reference allow pin programming of the 4127 as a logarithmic, log ratio, or antilog amplifier.

To further increase its versatility and reduce your system cost, the 4127 has an uncommitted operational amplifier in its package that can be used as a buffer, inverter, filter, or gain element.

The 4127 is available with initial accuracies (log conformity) of 0.5% and 1.0%, and operates over an ambient temperature range of -10°C to +70°C.

With its versatility and high performance, the 4127 has many applications in signal compression, transducer linearization, and phototube buffering. Manufacturers of medical equipment, analytical instruments, and process control instrumentation will find the 4127 a low cost solution to many signal processing problems.



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PDS-346E

SPECIFICATIONS

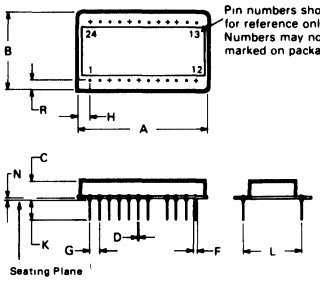
ELECTRICAL

Typical specifications at +25°C with rated supplies unless otherwise noted.

MODEL	4127KG	4127JG
ACCURACY(1), % of FSR		
Current Source Input, 1nA to 1mA	0.5% max	1% max
Voltage Input, 1mV to 10V	0.5% max	1% max
INPUT		
Current Source Input, Pin 4	+1nA to +1mA	
Current Source Input, Pin 7	-1nA to -1mA	
Reference Current Input, Pin 2	+1μA to +1mA	
Absolute Maximum Inputs	±10mA or ±Supply Volts	
OUTPUT		
Voltage	±10V	
Current	±5mA	
Impedance	10Ω	
FREQUENCY RESPONSE		
-3dB Small Signal at Current Input		
of 100μA	90kHz	
of 10μA	50kHz	
of 1μA	5kHz	
of 100nA	250Hz	
of 10nA	80Hz	
Step Response to within ±1% of		
Final Value (I_R = 1μA, A = 5)	10msec	
STABILITY		
Scale Factor Drift (ΔA/°C)	±0.0005A/°C	
Reference Current Drift (ΔI_R/°C)	±0.001 I_R/°C for $I_R \geq 1\mu A$	
	±0.003 I_R/°C for 400nA < I_R < 1μA	
Input Offset Current Drift (ΔI_S/°C)	10pA at +25°C, Doubles Every 10°C	
Input Offset Voltage Drift	±10μV/°C	
Accuracy vs. Supply Variation		
Reference Current	±0.001I_R/V	
Input Offset Voltage	±300μV/V	
Input Noise - Current Input	1pA, rms, 10Hz to 10kHz	
Input Noise - Voltage Input	10μV, rms, 10Hz to 10kHz	
UNCOMMITTED OP AMP CHARACTERISTICS		
Input Offset Voltage	5mV	
Input Bias Current	40nA	
Input Impedance	1MΩ	
Large Signal Voltage Gain	85dB	
Output Current	5mA	
TEMPERATURE RANGE		
Specification	0°C to +60°C	
Operating	-10°C to +70°C	
Storage	-55°C to +125°C	
POWER SUPPLY REQUIREMENTS		
Rated Supply Voltages	±15VDC	
Supply Voltage Range	±14VDC to ±16VDC	
Supply Current Drain		
at Quiescent, max	±20mA	
at Full Load, max	±26mA	

NOTE
1 Log conformity at 25°C

MECHANICAL



NOTE
Leads in true position within .010" (.25mm) R @ MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	.085	.105	2.16	2.67

CASE: Ceramic
MATING CONNECTOR 245MC
WEIGHT 56 grams (2 oz.)
ORDER NUMBER 4127KG
4127JG

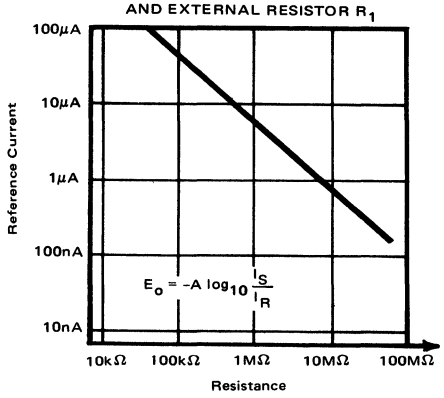
PIN CONNECTIONS

1 I_{REF} OUTPUT
2 I_{REF} INPUT
3 NO PIN PRESENT
4. +I INPUT *
5 CURRENT INVERTER OUTPUT*
6. NO PIN PRESENT
7. CURRENT INVERTER INPUT
8 NO PIN PRESENT
9 OP AMP +INPUT
10 OP AMP -INPUT
11 OP AMP OUTPUT
12. NO PIN PRESENT
13. MAKE NO CONNECTION
14. NEGATIVE SUPPLY
15 NO PIN PRESENT
16. NO PIN PRESENT
17 NO PIN PRESENT
18. LOG OUTPUT
19 GAIN ADJUST
20 NO PIN PRESENT
21 COMMON
22 POSITIVE SUPPLY
23. I_{REF} BIAS
24 NO PIN PRESENT

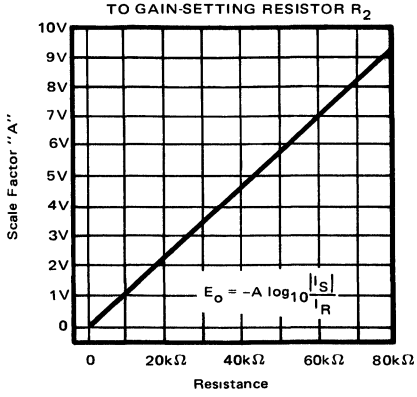
*Pins 4 and 5 are internally connected

TYPICAL PERFORMANCE CURVES

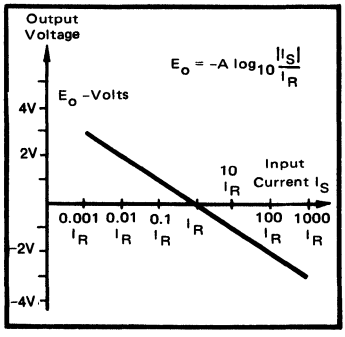
RELATIONSHIP OF REFERENCE CURRENT I_R AND EXTERNAL RESISTOR R_1



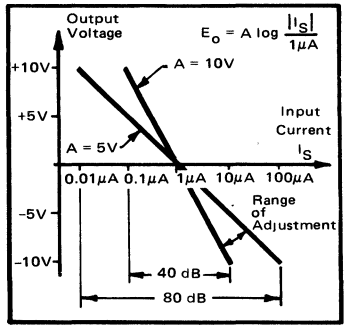
RELATIONSHIP OF SCALE FACTOR "A" TO GAIN-SETTING RESISTOR R_2



LOG RELATIONSHIP OF $\frac{|I_S|}{I_R}$ AND OUTPUT VOLTAGE IN TERMS OF "A"



RELATIONSHIP OF $\frac{|I_S|}{I_R}$ TO OUTPUT VOLTAGE FOR I_R = 1μA AND A = 5V AND 10V



DISCUSSION OF SPECIFICATIONS

ACCURACY

The deviation from the ideal output voltage defined as a percent of the full scale output voltage.

INPUT/OUTPUT RANGE

The log relationships of $-A \log \frac{I_S}{I_R}$ and $-A \log \frac{E_S}{I_R R}$ are subject to the constraints specified. The 4127 can be operated with inputs lower than those given, but the accuracy will be degraded.

FREQUENCY RESPONSE

The small-signal frequency response varies considerably with signal level and scaling, so the frequency response is specified under several different operating conditions.

STABILITY

The use of a monolithic transistor quad and low-drift op amps minimizes drift, but some drift remains in the scale-factor, reference current, and input offset. Input offset consists of a bias current plus the op amp input voltage offset divided by the signal source resistance. Also, there is some slight drift in conformity to the log function and in output amplifier offset, but this is generally negligible.

THEORY OF OPERATION

The 4127 is a complete logarithmic amplifier that can be pin-programmed to accept input currents or voltages of either polarity. By making use of the internal current inverter, reference current generator, log ratio element, and uncommitted op amp, you can generate a variety of logarithmic functions, including the log ratio of two signals, the logarithm of an input signal, or the antilog of an input signal. The unique FET-input current-inverting element removes the polarity limitations present in most conventional log amplifiers.

Utilizing the inherent exponential characteristics of transistor functions, the 4127 calculates accurate log functions for input currents from 1nA to 1mA, or input voltages from 1mV to 10V. Carefully matched monolithic quad transistors and temperature sensitive gain elements are used to produce a log amplifier with excellent temperature characteristics.

A functional diagram of the 4127 circuit is shown in Figure 1. In addition to the basic log amplifier, the 4127 contains a separate internal current source, a current inverter, and an uncommitted operational amplifier. The current inverter accurately converts negative input current to a positive current of equal magnitude.

The 4127 is capable of accurately logging input current over a 120dB range but to use this full range, good shielding practice must be followed. A current source input is, by definition, a high impedance source and is therefore subject to electrostatic pickups.

The input op amps A_1 and A_3 have FET input stages for low noise and very-low input bias current. The op amp A_1 will make the collector current of Q_1 equal to the signal input current I_S, and the collector current of Q_2 will be the reference input current I_R.

From the semiconductor junction characteristics, the base-to-emitter voltage will be

$$V_{BE} \approx \frac{m K T}{q} \ln \frac{I_C}{I_L}$$, where I_C = Collector current
I_L = Reverse saturation current
q, m, K = Constants
T = Absolute temperature

$$\text{So } E_1 = -\frac{m K T_1}{q} \ln \frac{I_S}{I_{L1}} \text{ and } E_2 - E_1 = \frac{m K T_2}{q} \ln \frac{I_R}{I_{L2}}$$

If the transistors Q_1 and Q_2 are at the same temperature and have matched characteristics then

$$E_2 = \frac{m K T}{q} \left[\ln \frac{I_R}{I_L} - \ln \frac{I_S}{I_L} \right]$$

$$E_2 = \frac{-m K T}{q} \ln \frac{I_S}{I_R}$$

The output op amp A_2 provides a voltage gain of approximately $(R_T + R_2)/R_T$, and the value of $(mKT)/q$ is about 26mV at room temperature. Since resistor R_T varies with temperature to compensate for gain drift, the output voltage E_o expressed as a log will be

$$E_o = -A \log_{10} \frac{I_S}{I_R}$$

$$\text{where } A \approx \frac{R_T + R_2}{R_T} (26 \text{ mV}) \frac{1}{0.434}, \quad R_T \approx 520\Omega$$

The external resistor R_1 sets the reference current I_R and resistor R_2 sets the scale-factor "A". R_1 and R_2 must be trimmed to the desired values, but the approximate relationships are shown in Typical Performance Curves.

The relationship between the input current I_S and the output voltage E_o in terms of the externally adjusted parameters I_R and "A" is illustrated in Typical Performance Curves. This relationship is, of course, restricted to values of I_S between 1nA and 1mA and output voltages of less than ±10V.

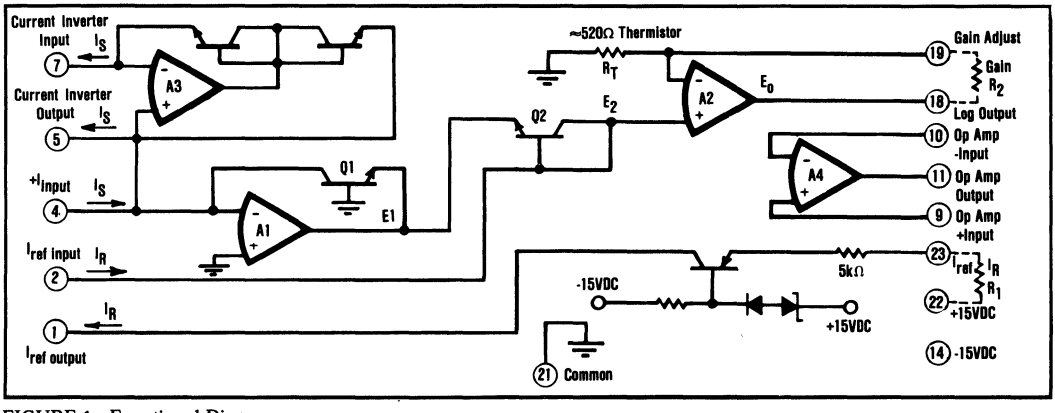


FIGURE 1. Functional Diagram.

CHOOSING THE OPTIMUM SCALE FACTOR AND REFERENCE CURRENT

To minimize the effects of output offset and noise, it is usually best to use the full ±10V output range. Once an output range of ±10V has been chosen, then "A" and I_R can be determined from the min/max of the input current I_S.

$$E_o = -A \log \frac{I_S}{I_R}, \text{ where } I_{min} < I_S < I_{max}$$

The output range of ±10V for an input range of I_{min} to I_{max} means that

$$+10 = -A \log \frac{I_{min}}{I_R} \text{ and } -10 = -A \log \frac{I_{max}}{I_R}$$

Adding these two equations together

$$\log \frac{I_{max} I_{min}}{I_R^2} = 0, \text{ or } I_R = \sqrt{I_{max} I_{min}}$$

The value for A can be found from:

$$10 = A \log \frac{I_{max}}{\sqrt{I_{max} I_{min}}}$$

In terms of the input current range for I_S, the values for I_R and A that will provide a full ±10V output swing are:

$$I_R = \sqrt{I_{max} I_{min}} \text{ and } A = \frac{10}{\log \frac{I_{max}}{I_R}}$$

Example: Assume that I_{min} is +10nA and I_{max} is +100μA.

This is an 80dB range.

$$I_R = \sqrt{I_{max} I_{min}} = \sqrt{(10^{-4})\ (10^{-8})} = 10^{-6}, \text{ or } 1\mu A.$$

$$\frac{I_{max}}{I_R} = \frac{10^{-4}}{10^{-6}} = 100$$

$$\log \frac{I_{max}}{I_R} = 2 \quad \text{So } A = 5$$

For an I_R of 1μA and A of 5,

$$E_o = -5 \log \frac{I_S}{1\mu A}$$

CONNECTION DIAGRAMS

Transfer function is $E_o = -A \log \frac{I_1}{I_R}$ where I_1 is a positive input current and I_R is the resistor-programmed internal reference current (see Figure 2).

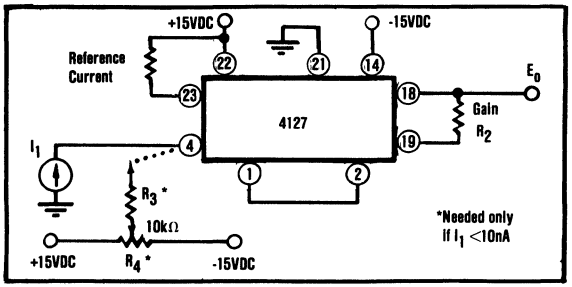


FIGURE 2. Transfer Function When I_1 is Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing The Optimum Scale Factor and Reference Current.
2. Apply $I_1 = I_R$, adjust R_1 such that $E_o = 0$.
3. Apply $I_1 = I_{max}$, adjust R_2 for the proper output voltage.
4. Repeat steps 2 and 3 if necessary.
5. Ignore this step if $I_{1min} \geq 10nA$. Otherwise, apply $I_1 = 1nA$, make $R_3 = 1k\Omega$* and adjust R_4 for the proper output voltage.

Transfer function is $E_o = -A \log \frac{|I_1|}{I_R}$ where I_1 is a negative input current and I_R is the resistor-programmed internal reference current (see Figure 3).

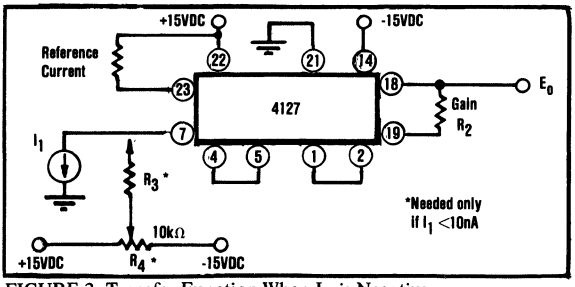


FIGURE 3. Transfer Function When I_1 is Negative.

ADJUSTMENT PROCEDURE

1. Refer to Choosing The Optimum Scale Factor and Reference Current.
2. Apply $|I_1| = I_R$ adjust R_1 such that $E_o = 0$.
3. Apply $|I_1| = I_{max}$, adjust R_2 for the proper output voltage.
4. Repeat steps 2 and 3 if necessary.
5. Ignore this step if $|I_{1min}| \geq 10nA$. Otherwise, apply $|I_1| = 1nA$, make $R_3 = 1k\Omega$* and adjust R_4 for the proper output voltage.

*Single resistor recommended. Voltage divider network difficult to use due to amplifier offset voltage. RF500-108, 1GΩ resistor available from Burr-Brown.

CONNECTION DIAGRAMS [CONT]

Transfer function is $E_0 = -A \log \frac{E_1}{R_4 I_R}$, where E_1 is a positive input voltage and I_R is the resistor-programmed internal reference current (see Figure 4).

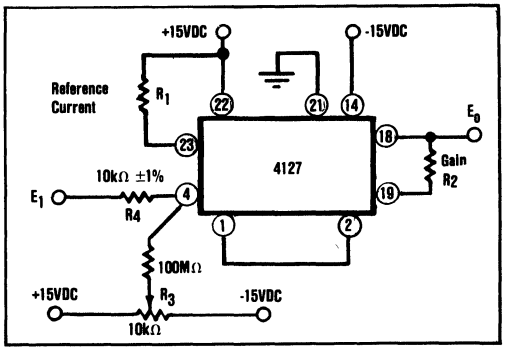


FIGURE 4. Transfer Function When E_1 is Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing The Optimum Scale Factor and Reference Current.
2. Apply $E_1 = I_R$ (10kΩ), adjust R_1 such that $E_0 = 0$.
3. Apply $E_1 = E_{max}$, adjust R_2 for the proper output voltage.
4. Apply $E_1 = E_{min}$, adjust R_3 for the proper output.
5. Repeat steps 2 through 4 if necessary.

Transfer function is $E_0 = -A \log \frac{|E_1|}{R_4 I_R}$, where E_1 is a negative input voltage and I_R is the resistor-programmed internal reference current (see Figure 5).

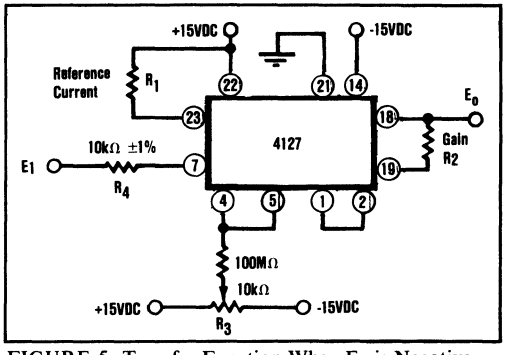


FIGURE 5. Transfer Function When E_1 is Negative.

ADJUSTMENT PROCEDURE

1. Refer to Choosing The Optimum Scale Factor and Reference Current.
2. Apply $|E_1| = I_R$ (10kΩ), adjust R_1 such that $E_0 = 0$.
3. Apply $|E_1| = E_{max}$, adjust R_2 for the proper output voltage.
4. Apply $|E_1| = E_{min}$, adjust R_3 for the proper output.
5. Repeat steps 2 through 4 if necessary.

Transfer function is $E_0 = -A \log \frac{|I_1|}{|I_2|}$ with I_1 and I_2 negative; $|I_1| \geq 1nA, |I_2| \geq 1\mu A$ (see Figure 6).

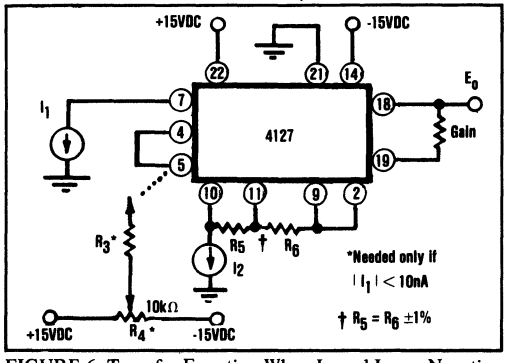


FIGURE 6. Transfer Function When I_1 and I_2 are Negative.

ADJUSTMENT PROCEDURE

1. Refer to Choosing The Optimum Scale Factor and Reference Current.
2. No further adjustment is necessary if I_1 min ≥ 10nA, otherwise connect the R_3 and R_4 network, with R_4 =10kΩ and $R_3 = 10^9\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of ±5mV, it is not practical to use a T - network to replace R_3.

Transfer function is $E_O = -A \log \frac{|I_1|}{I_2}$ with I_1 negative, I_2 positive; $|I_1| \geq 1nA$, $I_2 \geq 1\mu A$ (see Figure 7).

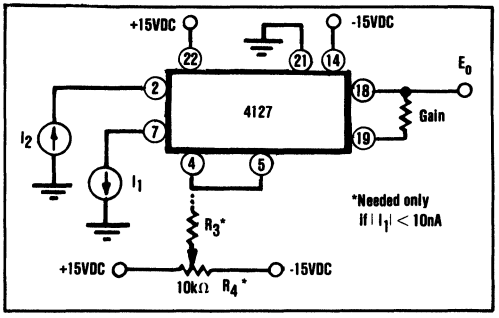


FIGURE 7. Transfer Function When I_1 is Negative, I_2 is Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing The Optimum Scale Factor and Reference Current.
2. No further adjustment is necessary if $|I_1|$min $\geq$ 10nA, otherwise connect the R_3 and R_4 network, with $R_4 = 10k\Omega$ and $R_3 = 10^9\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of $\pm$5mV, it is not practical to use a T - network to replace R_3.

Transfer function is $E_O = -A \log \frac{I_1}{I_2}$ with I_1 and I_2 positive; $I_1 \geq 1nA$, $I_2 \geq 1\mu A$ (see Figure 8).

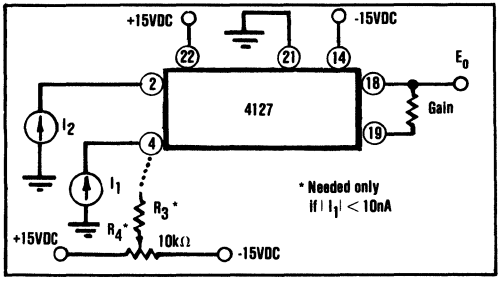


FIGURE 8. Transfer Function When I_1 and I_2 are Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. No further adjustment is necessary if I_1 min $\geq$ 10nA, otherwise connect the R_3 and R_4 network, with $R_4 = 10k\Omega$ and $R_3 = 10^9\Omega$. Adjust R4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of $\pm$5mV, it is not practical to use a T - network to replace R_3.

ANTILOG OPERATION

The 4127 can also perform the antilog function. The output is connected through a resistor R_O into the current input, pin 4. The input signal is connected through a gain resistor to pin 19 as shown in Figure 9.

These connections form an implicit loop for computing the antilog function. From the block diagram of Figure 1, the voltage at the inverting input of the output amplifier A2 must equal E_2, so

$$E_2 \approx \frac{R_T}{R_T + R_2} E_S, \quad R_T \approx 520\Omega$$

Since the output is connected through R_O to pin 4, the current I_S will equal E_O/R_O and E_2 will be

$$E_2 = -\frac{m K T}{q} \ln \frac{E_O}{R_O I_R}$$

Combining expressions for E_2 gives the relationship

$$\frac{R_T}{R_T + R_2} E_S = -\frac{m K T}{q} \ln \frac{E_O}{R_O I_R}$$

$$-\frac{E_S}{A} = \log \frac{E_O}{R_O I_R}$$

where

$$A \approx \frac{R_T + R_2}{R_T} (26mV) \frac{1}{0.434}$$

$$E_O = R_O I_R \text{ Antilog} - \frac{E_S}{A}$$

Setting R_O and I_R will set the scale factor. For example, an R_O of 1MΩ and I_R of 1μA will give a scale factor of unity and

$$E_O = \text{Antilog} - \frac{E_S}{A}$$

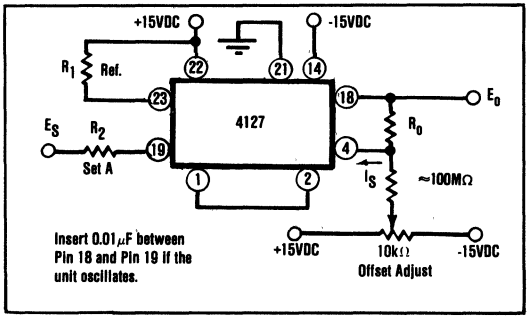


FIGURE 9. Antilog Operation.

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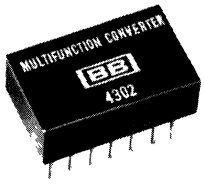


4302

Low Cost MULTIFUNCTION CONVERTER

FEATURES

- LOW COST
- SMALL PACKAGE - Dual-in-line
- RELIABLE HYBRID CONSTRUCTION
- VERSATILE

FUNCTIONS	ACCURACY
MULTIPLY	±0.25%
DIVIDE	±0.25%
SQUARE	±0.03%
SQUARE ROOT	±0.07%
EXPONENTIATE	±0.15% (m = 5)
ROOTS	±0.2% (m = .2)
SINE θ	±0.5%
COSINE θ	±0.8%
TAN $^{-1}$ (Y/X)	±0.6%
$\sqrt{X^2 + Y^2}$	±0.07%

Typical accuracies expressed as a % of output full scale (+10VDC) at 25°C

DESCRIPTION

Burr-Brown's multifunction converter model 4302 is a low cost solution to many analog conversion needs. Much more than just another multiplier/divider, the 4302 out performs many analog circuit functions with a very high degree of accuracy at a very low total cost to the user.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-326D

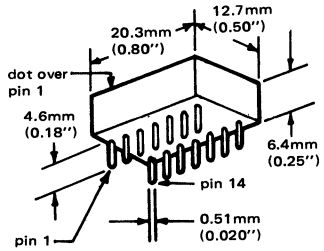
SPECIFICATIONS

Performance typical at 25°C and with rated supply unless otherwise noted.

ELECTRICAL

MODEL	4302
TRANSFER FUNCTION	$E_O = V_Y \left(\frac{V_Z}{V_X}\right)^m$
RATED OUTPUT	
Voltage	+10.0 V
Current	5 mA
INPUT	
Signal Range	$0 \leqslant (V_X, V_Y, V_Z) \leqslant +10$ V
Absolute Maximum	$(V_X, V_Y, V_Z) \leqslant \pm 18$ V
Impedance (X/Y/Z)	100 kΩ/90 kΩ/100 kΩ
EXPONENT RANGE	
Roots ($0.2 \leqslant m < 1$)	$m = \frac{R_2}{R_1 + R_2}$ Refer to Functional Diagram below
Powers ($1 < m \leqslant 5$)	$m = \frac{R_1 + R_2}{R_2}$
($m = 1$)	$R_1 = 0\ \Omega$, R_2 not used
POWER REQUIREMENTS	
Rated Supply	±15 VDC
Range	±12 to ±18 VDC
Quiescent Current	±10 mA
TEMPERATURE RANGE	
Operating	−25°C to +85°C
Storage	−25°C to +85°C

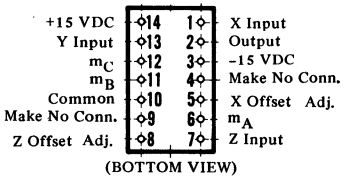
MECHANICAL



Row Spacing: 7.6mm (0.300")
Weight: 3.4 grams (0.12 oz.)
Connector: 14-pin DIP
0145MC

Pin material and plating composition conform to Method 208 (solderability) of Mil-Std-202.

PIN CONNECTIONS



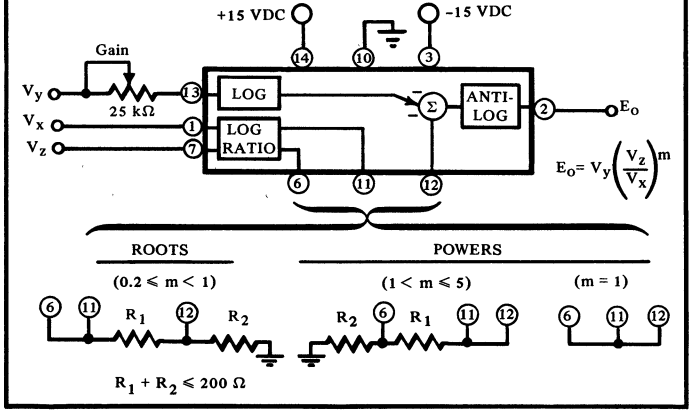
(BOTTOM VIEW)

General specifications for the Model 4302 Multifunction Converter are presented on this page. These specifications characterize the 4302 as a versatile three input multifunction converter.

The following pages are applications oriented to help you apply the 4302 to your particular circuit function need. These pages contain dedicated circuit configurations in order to produce the functions of: multiplication, division, exponentiation, square rooting, squaring, sine, cosine, arctangent, and vector algebra.

It is the purpose of this product data sheet to enable you to apply the 4302 to your analog conversion needs quickly and efficiently.

4302 FUNCTIONAL DIAGRAM



Many of the following circuit configurations using the 4302 require a reference voltage for scaling purposes. The reference voltage is shown to be +15 VDC (+15 VDC REF.) since in most cases the +15 VDC power source for the 4302 has sufficient time and temperature related stability to achieve the specified typical accuracies.

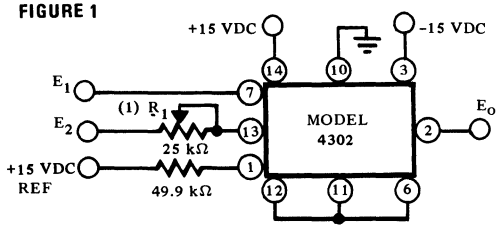
If the particular supplies which are available for powering the 4302 do not have the necessary stability for the required conversion accuracy, an additional +15 VDC precision supply may be required.

MULTIPLIER/DIVIDER FUNCTIONS

MULTIPLIER

In multiplier applications the 4302 provides high accuracy at a low cost. The 4302 accepts inputs up to +10 VDC and provides a typical accuracy of ±0.25% of full scale.

FIGURE 1



(1) Set R_1 so that with $E_1 = E_2 = +10.00$ VDC, $E_o = +10.00$ VDC.

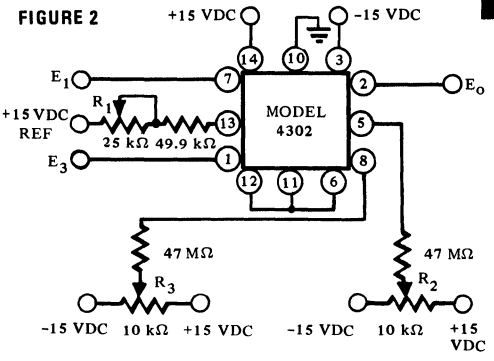
Transfer Function	$E_o = +\frac{E_1 E_2}{10}$
ACCURACY	
Total Errors	
Typical at +25°C	±25 mV
Maximum at +25°C	±50 mV
(for input range)	$\begin{cases} 0.03V \leq E_1 \leq 10\ V \\ 0.01\ V \leq E_2 \leq 10\ V \end{cases}$ *
vs. Temperature	±1 mV/°C
Offset Errors ($E_1 = E_2 = 0$)	
Output Offset (at 25°C)	±10 mV
vs. Temperature	±0.2 mV/°C
NOISE (10 Hz to 1 kHz)	100 µV rms
BANDWIDTH (E_1, E_2)	
Small Signal (-3 dB)	500 kHz
Full Output	60 kHz

DIVIDER

As a divider, the 4302 outperforms many of the multiplier/dividers on the market at a much lower cost. In the divider configuration the 4302 boasts a typical conversion accuracy of ±0.25% of full scale.

Transfer Function	$E_o = +10\ (E_1/E_3)$
ACCURACY	
Total Errors	
Typical at +25°C	±25 mV
Maximum at +25°C	±50 mV
(for $E_1 \leq E_3$ and input range)	$\begin{cases} 0.03V \leq E_1 \leq 10\ V \\ 0.1\ V \leq E_3 \leq 10\ V \end{cases}$ *
vs. Temperature	±1 mV/°C
Offset Errors ($E_1 = 0$, $E_3 = +10$ V)	
Output Offset (at 25°C)	±10 mV
vs. Temperature	±1 mV/°C
NOISE (10 Hz to 1 kHz)	
$E_3 = +10$ V	100 µV rms
$E_3 = +0.1$ V	300 µV rms
BANDWIDTH (E_1, E_3)	
Small Signal (-3 dB)	500 kHz
Full Output	
($E_3 = +10$ V)	60 kHz

FIGURE 2



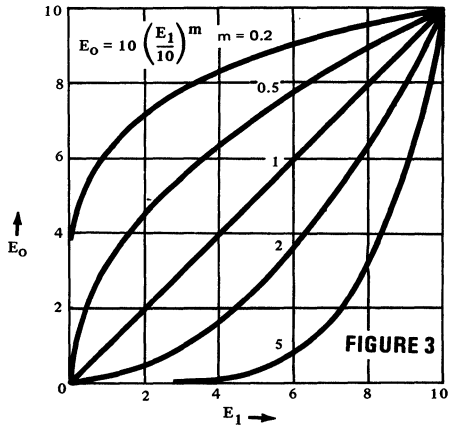
NOTES:
(1) Set R_1 so that with $E_1 = E_3 = +10.00$ VDC, $E_o = +10.00$ VDC.
(2) Set R_2 so that with $E_1 = E_3 = +0.10$ VDC, $E_o = +10.00$ VDC.
(3) Set R_3 so that with $E_1 = +0.01$ VDC and with $E_3 = +0.10$ VDC, $E_o = +1.00$ VDC.
(4) Repeat steps 1 through 3 as necessary to achieve the specified output voltages.

* The input voltage may be extended below 0.03V by connecting a 0.047 µF capacitor between pins 11 and 5, causing a slight reduction in bandwidth. (Multiply and Divide Modes).

EXPONENTIAL FUNCTIONS

Model 4302 may be used as exponentiator over a range of exponents from 0.2 to 5. The exponents 0.5 and 2, square rooting and squaring respectively, are often used functions and are treated below. Other values of exponents (m) may be useful in terms of linearization of nonlinear functions or simply for producing the mathematical conversions. Characteristics of m = 0.2 and m = 5 are presented on the right. For other values of m the curves presented in Figure 3 may be used to interpolate the error for a nonspecified value of m.

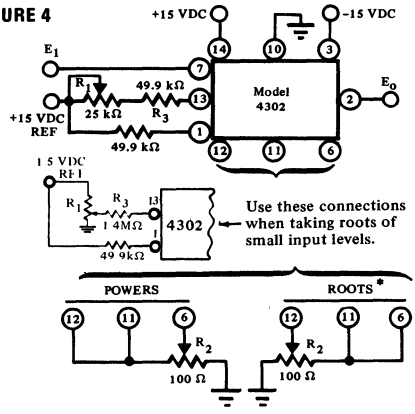
Transfer Function	$E_o = 10\left(\frac{E_1}{10}\right)^m$
Total Conversion Error (typical)	
m = 0.2	
0.5 VDC < $E_1 \leq$ 10 VDC	±2 m VDC
0.1 VDC < $E_1 \leq$ 0.5 VDC	±25 m VDC
m = 5	
1.0 VDC < $E_1 \leq$ 10 VDC	±15 m VDC
Exponent Range (continuous)	$0.2 \leq m \leq 5$
Input Voltage Range	0 to +10 VDC
Output Voltage Range	0 to +10 VDC



Exponentiator Transfer Characteristics

NOTES:
(1) Connect a 100 Ω potentiometer as shown in Figure 4 for either roots ($0.2 \leqslant m < 1$) or powers ($1 < m \leqslant 5$).
(2) Set R_1 so that with E_1 = +10.00 VDC, E_o = +10.00 VDC.
(3) Select a + DC voltage level (E_1) such that the output voltage (E_o), as acted upon by the desired exponent, will not exceed +10.00 VDC. A level which is mid-range for input values of interest is an appropriate one to use. Set R_2 so that the output voltage (E_o) is the value expected for the chosen values of input (E_1) and exponent (m).

FIGURE 4



(4) Repeat steps (2) through (4) as necessary.

* When taking roots of smaller input levels, a modified transfer equation [$E_o = (10E_1)^m$] will provide improved conversion accuracy. To achieve this transfer function: 1) apply a +1.5 VDC REF in place of the +15 VDC REF shown in Figure 4., 2) make R_3 a 1.40 MΩ resistor, and rearrange R_1 and R_3 as 1.5VDC REF and 3) follow all notes except in note (2) apply +0.10VDC to pin 7 to set R_1 to E_o = +1.00VDC.

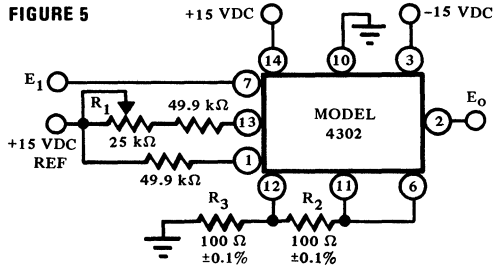
SQUARE ROOT

As a Square Rooter (m = 0.5), the 4302 provides a typical total conversion accuracy of ±0.07%. Refer to Figure 5 and notes for connections and adjustments respectively.

Transfer Function	$E_o = 10\sqrt{\frac{E_1}{10}}$
Total Conversion Error (Typical)	
0.5 VDC < E_1 ⩽ 10 VDC	±7 mV
0.02 VDC < E_1 ⩽ 0.5 VDC	±55 mV
Input Voltage Range	0 to +10 VDC
Output Voltage Range	0 to +10 VDC

NOTES:
(1) Connect pins 12, 11, and 6 together. Set R_1 such that with E_1 = +10.00 VDC; E_o = +10.00 VDC.
(2) Connect 100 Ω resistors as shown in Figure 5.
(3) For greater conversion accuracy, R_2 & R_3 may be replaced by a potentiometer as shown in Figure 4.

FIGURE 5



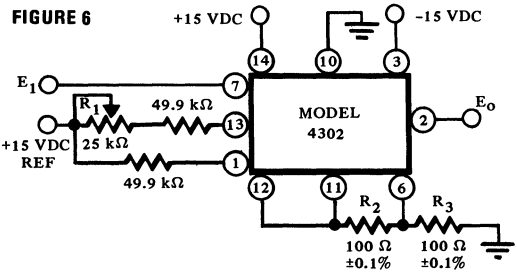
SQUARE

Configured as a Square Function Converter (m = 2), the 4302 produces high conversion accuracies of typically 0.03%. Please refer to Figure 6 and accompanying notes.

Transfer Function	$E_o = 10\left(\frac{E_1}{10}\right)^2$
Total Conversion Error (typical)	
0.1 VDC ⩽ E_1 ⩽ 10 VDC	±3 mV
Input Voltage Range	0 to +10 VDC
Output Voltage Range	0 to +10 VDC

NOTES:
(1) Set R_1 such that with E_1 = +10.00 VDC, E_o = +10.00 VDC.
(2) Connect 100 Ω resistors as shown in Figure 6.
(3) For greater conversion accuracy R_2 & R_3 may be replaced by a potentiometer as shown in Figure 4.

FIGURE 6



TRIGONOMETRIC FUNCTIONS

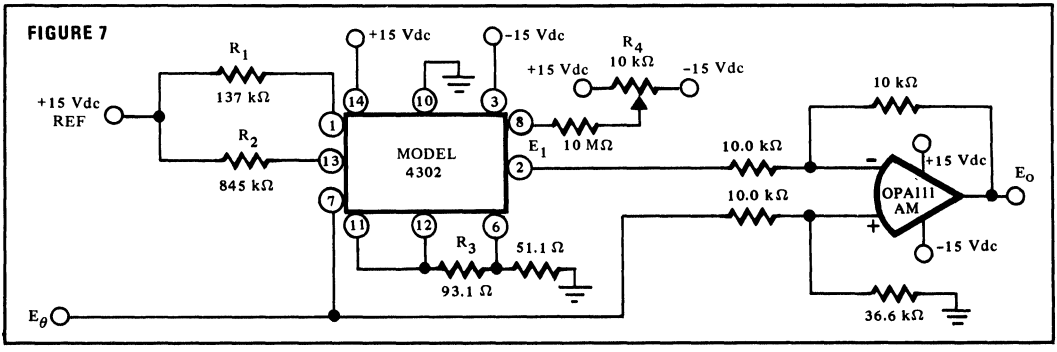
SINE

Sine functions can be accurately generated from input voltage levels representing angular displacement from 0 to 90°. Model 4302 configured as in Figure 7 will produce the sine power series approximations with modified coefficients to typically better than ±0.5% of full scale. In this circuit, the 4302 is scaled so that when $\theta = 0$, $E_O = 0$ VDC, and when $\theta = 90$, $E_O = 10$ VDC.

NOTES:
(1) Adjust R_4 if needed so that $E_1 < 1$ m VDC when $E_\theta = 0$.
(2) Adjust R_2 so that $E_1 = +0.8045$ VDC when $E_\theta = +5.00$ VDC.
(3) Adjust R_3 so that $E_1 = +5.709$ VDC when $E_\theta = +10.00$ VDC.
(4) Repeat steps (2) and (3) as necessary.

Transfer Function	$E_O = 10 \text{ Sin } 9E_\theta$
Power Series Approximation $E_O = 1.5708E_\theta - 1.5924\left(\frac{E_\theta}{6.366}\right)^{2.827}$	
Total Conversion Error (typical)	±50 mV
Input Voltage Range ($0 \leq \theta \leq 90^O$)	0 to +10 VDC
Output Voltage Range ($0 \leq \sin\theta \leq 1$)	0 to +10 VDC

FIGURE 7



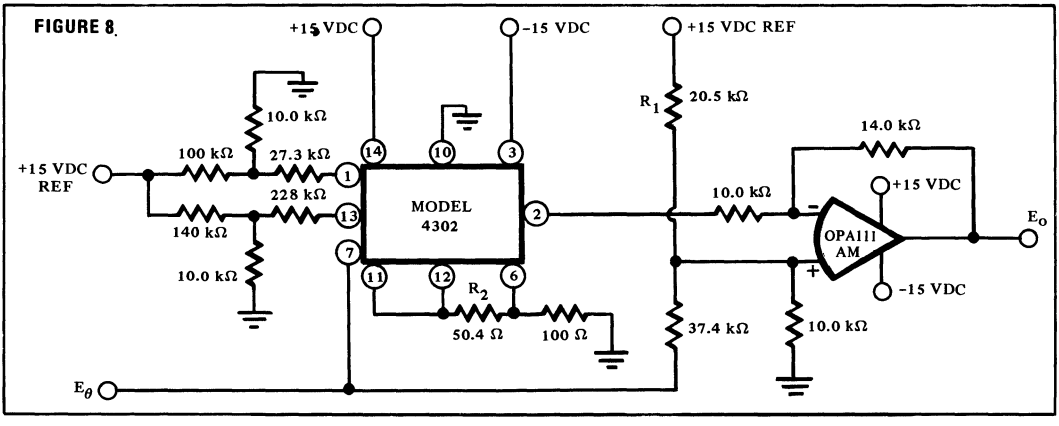
COSINE

Connected as in Figure 2, the Model 4302 will generate a cosine function of the input voltage. Typical accuracies of ±0.8% can be expected from this configuration.

NOTES:
(1) Adjust R_1 so that $E_O = +10.00$ VDC when $E_\theta = 0$.
(2) Adjust R_2 so that $E_O = 0$ when $E_\theta = +10.00$ VDC.

Transfer Function	$E_O = 10 \cos 9E_\theta$
Power Series Approximation $E_O = 10 + 0.3652\,E_\theta - 0.4276E^{1.504}$	
Total Conversion Error (typical)	±80 mV
Input Voltage Range ($0 \leq \theta \leq 90^O$)	0 VDC to +10 VDC
Output Voltage Range ($1 \leq \cos\theta \leq 0$)	+10 VDC to 0 VDC

FIGURE 8



ARCTANGENT

Model 4302 and the associated circuitry shown below will produce the inverse tangent of a ratio. This application is particularly well suited to conversion from rectangular coordinates to polar coordinates where

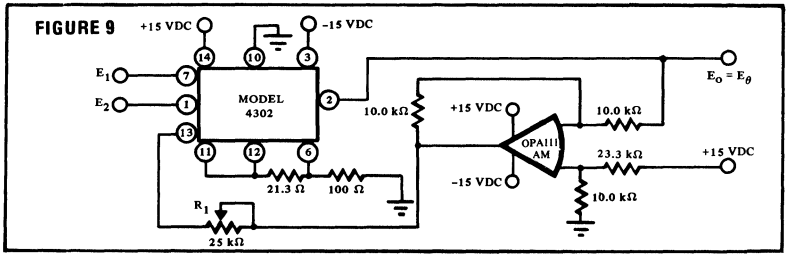
$$E_\theta = \tan^{-1}\frac{E_Y}{E_X}$$

The accuracy of conversion depends upon the levels of the input signals. Please refer to table at right.

NOTE:
(1) Set R_1 so that with $E_1 = E_2 = +10.00$ VDC, $E_o = +4.500$ VDC ±1 mVDC.

Transfer Function	$E_o = \tan^{-1}\left(\frac{[E_1]}{[E_2]}\right)$
Power Series Approximation	$E_o = \frac{\left(\frac{[E_1]}{[E_2]}\right)^{1.2125}}{1+\left(\frac{[E_1]}{[E_2]}\right)^{1.2125}}(90^o)$
Total Conversion Error	
$2 < E_1, E_2 \leq 10$ VDC	±55 m VDC
$0.1 < E_1, E_2 \leq 2$ VDC	±65 m VDC
$0.03 < E_1, E_2 \leq 0.1$ VDC	±340 m VDC
Input Voltage Range (E_1, E_2)	+0.01 VDC to +10 VDC
Output Voltage Range $0 \leq E_\theta \leq 90^o$	0 VDC to +9 VDC

FIGURE 9



VECTOR MAGNITUDE FUNCTION

The model 4302 will produce the square root of the sum of the squares of two inputs. This function is companion to the arctangent of a ratio for the conversion of rectangular to polar coordinates.

Transfer Function	$E_o = \sqrt{E_1^2 + E_2^2}$
Input Voltage Range E_1	0 to +10VDC
E_2	-10VDC to +10VDC
(refer to notes 1 and 2)	
Output Voltage Range	0 to +10VDC
Conversion Error	±7m VDC

NOTES:
1. Figure 10 shows one practical way to implement the transfer function $E_o=\sqrt{E_1^2+E_2^2}$ using 4302. It shows use of model 3501A op amp. Model 3501's rated output is ±10V. This limits the range of E_1 and E_2, such that the conditions $E_1 \leq \sqrt{100 - E_2}$ and $|E_2| \leq (5 - E_1^2/20)$ and $\sqrt{E_1^2 + E_2^2} \leq 10$ are always satisfied.
(a) The above conditions imply, $0V \leq E_1 \leq 10V$ and $-5V \leq E_2 \leq 5V$
(b) The above conditions also imply that for applications where $E_1 = |E_2|$ the range would be limited to 4.142V max.
2. Use of model 3627 as shown in Figure 11 would directly substitute the eight 10kΩ resistors and the two model 3501A op amps. This would reduce the number of components needed to implement vector magnitude function and reduce overall cost.

FIGURE 10

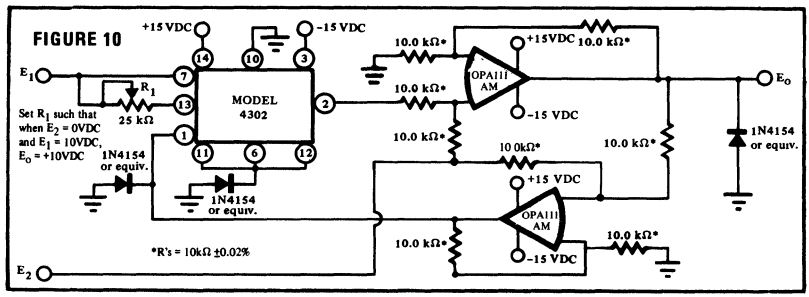
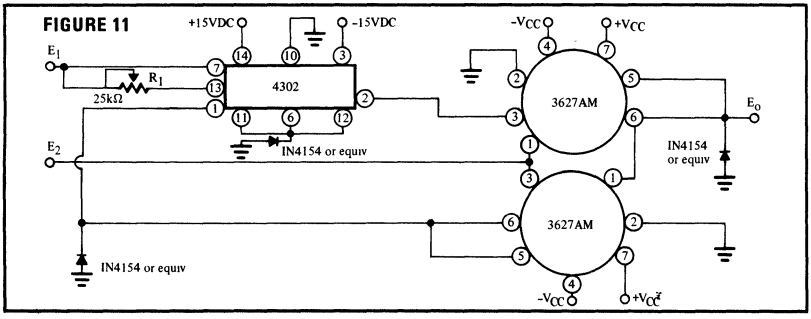
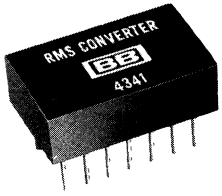


FIGURE 11



BURR-BROWN®

4341



Low Cost
TRUE RMS-TO-DC CONVERTER

FEATURES

- **LOW COST**
- **HIGH ACCURACY**
  ±0.2% ±2mV
- **HIGH RELIABILITY**
  Hybrid construction

DESCRIPTION

The Burr-Brown Model 4341 RMS-to-DC Converter features low cost without sacrificing performance. The 4341 computes a DC voltage proportional to the true rms value of signals which may be complex waveforms, DC levels, or a combination of both.

The input and output are fully protected against overvoltages and short circuits. Provisions for the external adjustment of gain, offset voltage, DC-reversal error, and frequency response make the 4341 versatile enough to fill the majority of your applications.

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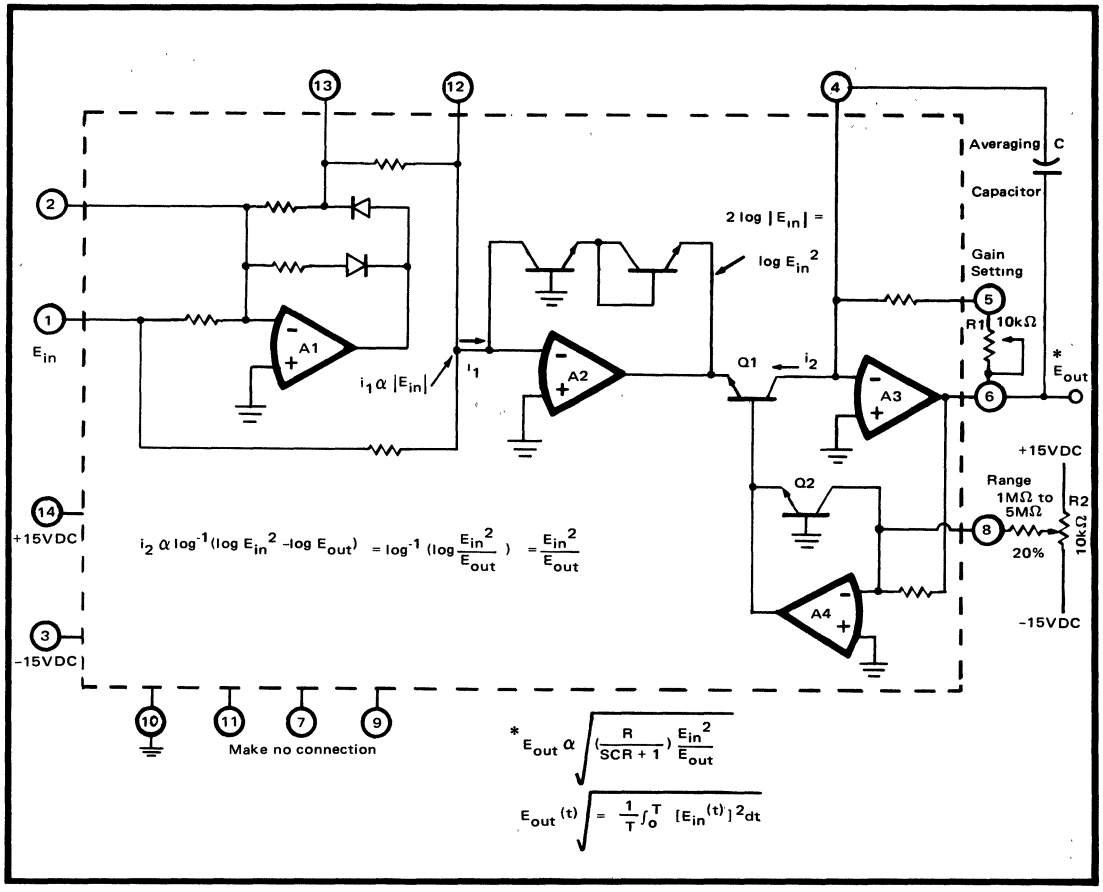


FIGURE 1. Simplified Schematic.

THEORY OF OPERATION

The true rms value of a time-varying signal E (t) over a time period T is

$$E_{rms} = \sqrt{1/T \int T/o\,[E(t)]^2\,dt}$$

The required operations are squaring, averaging and square rooting. A simplified schematic diagram of the 4341 is shown in Figure 1. The A1 circuit produces a current i_1 which is proportional to the rectified input voltage. The A2 circuit is a logarithmic amplifier which produces a voltage proportional to 2 log E_{in} or log E_{in}^2. The logarithmic gain of the A2 circuit is derived from the inherent exponential characteristics of transistor junctions. By using proprietary monolithic components, the circuit provides an accurate log function over many decades which is relatively insensitive to temperature variations. Amplifier A4 uses the same techniques as A2 to generate log E_{out}.

Transistor Q1 produces a collector current i_2 proportional to the antilog of its base-emitter voltage such that

$$i_2 \alpha \log^{-1} (\log E_{in}^2 - \log E_{out})$$
$$= \log^{-1} (\log E_{in}^2/E_{out}) = E_{in}^2/E_{out}$$

The A3 circuit which contains the external capacitor takes the time average of the i_2 signal and produces E_{out} which is directly proportional to the rms value of E_{in}.

Figures 2 and 3 show the effects of the external filter capacitor on ripple magnitude and response time. As the frequency of the input approaches DC, the 4341 begins to act like a full wave rectifier such that the output is the absolute value of the input. While the 4341 will accurately convert DC input voltages, the averaging capacitor must be made very large to minimize ripple at low frequencies.

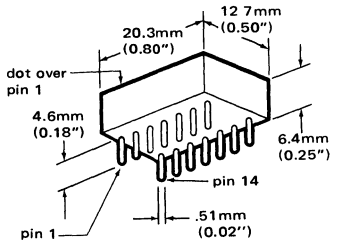
ELECTRICAL SPECIFICATIONS

Typical at 25°C with rated supply voltages, unless otherwise noted.

MODEL	4341
TRANSFER FUNCTION	$I_{out}(DC) = 1/T \int_0^T E_{in}^2(t)\,dt$
INPUT	
Peak Operating Voltage	±10V
Absolute Maximum Voltage	±Supply
Impedance	5kΩ
OUTPUT	
Voltage	0 to +10V
Current	+5mA, min
Resistance	1Ω, max
BANDWIDTH	
±1% of Theoretical Output	80kHz
-3dB	450kHz
CONVERSION ACCURACY[2]	
Input: 500mV, rms to 5.0V, rms Input: DC to 10kHz Sine Wave	±0.5% of Reading, max[1]
Input, 10mV, rms to 7V, rms Input: DC to 20kHz	±2mV ±0.2% Reading
STABILITY	
Accuracy vs. Temperature	±0.1mV ±0.01% of Reading/°C
Accuracy vs. Supply Voltage	±0.1mV ±0.01% of Reading/% of Supply Voltage Change
TEMPERATURE RANGE	
Operating	−25°C to +85°C
Storage	−40°C to +85°C
POWER REQUIREMENTS	
Rated Voltage	±15VDC
Voltage Range	±14VDC to ±16VDC
Quiescent Current	±12mA, typ./±24mA, max

NOTES:
1. After standard trim procedure (see below)
2. Model 4341 will convert DC inputs. Lower frequency AC inputs require a large value of averaging capacitor to minimize ripple at output. (see Figure 2).

MECHANICAL



Row Spacing. 7.6mm (0.30")
Weight: 3.4 grams (0.12 oz.)
Connector 14-Pin DIP
0145MC

Pin material and plating composition conform to Method 208 (solderability) of Mil-Std-202.

STANDARD TRIM PROCEDURE

If the 4341 is used to measure sine waves or distorted sine waves, only two trims are needed to achieve an accuracy of ±0.5% of reading from 500mV, rms to 5V, rms up to 10kHz. Refer to Figure 1.

1. Set E_{in} = 5.000V, rms ±0.02% and adjust R1 such that E_o = 5.000VDC ±2mV.
2. Set E_{in} = 500mV, rms ±0.02% and adjust R2 such that E_o = 500mVDC ±0.2mV.
3. Repeat Step 1.

CHOOSING THE AVERAGING CAPACITOR

A single-pole low-pass RC filter provides the averaging function. The time constant is 1/2 RC where R is 10kΩ when the 4341 is adjusted for unity gain. To select the best value of C, make a tradeoff between output ripple and response time. Figure 2 shows the ripple magnitude vs. frequency for several typical values of capacitor. Response time vs. capacitor value is shown in Figure 3. (Note that rise times and fall times are different for the same value of capacitor).

While the ripple magnitude for signals other than sine waves can be analytically determined, it is tedious. The fastest method of choosing C is to apply a representative input signal and observe the output for various value of C. C can be 100's of microfarads, but should have a leakage current less than 0.1μA to minimize gain errors. With very large values of C, the input signals with frequencies approaching DC level could be averaged. Since the output is always a positive voltage, C can be polar capacitor.

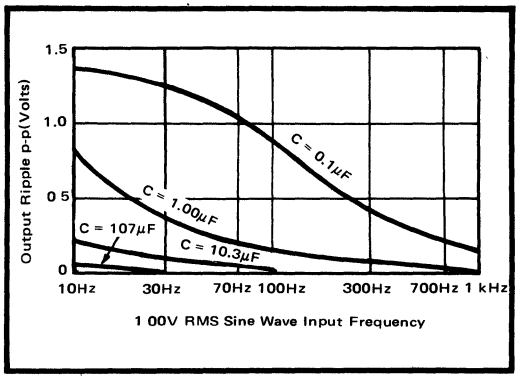


FIGURE 2. Output Ripple Magnitude vs. Input Signal Frequency.

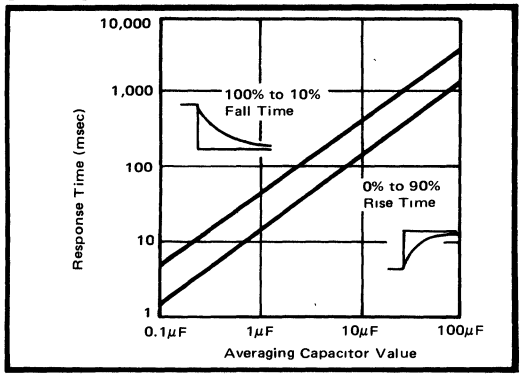


FIGURE 3. Response Time vs. Value of Averaging Capacitor.

EXPANDED TRIM PROCEDURE FOR GREATER ACCURACY

If the 4341 is used in applications to measure complex waveforms, the following expanded trim procedure is recommended. (Refer to Figure 4).

First set all potentiometers at mid turn position.

1. DC Reversal Error - Apply +10.000V ±1mV and -10.000V ±1mV to E_{in} alternatively, adjust R5 such that E_o readings are the same ±2mV.
2. Gain Adjustment - Apply E_{in} = +10.000VDC ±1mV, adjust R1 such that E_o = +10.000VDC ±1mV.
3. Input Offset - Apply +10.0mV ±0.1mV and -10.0mV ±0.1mV to E_{in}, adjust R4 such that E_o readings are the same ±0.1mV.
4. Offset - Ground E_{in}, adjust R3 such that E_o = 0 ±0.1mV. Repeat Step (3).
5. Low Level Accuracy - Apply E_{in} = +10.0mV ±0.1mV, adjust R2 such that E_o = +10.0mV ±0.1mV.

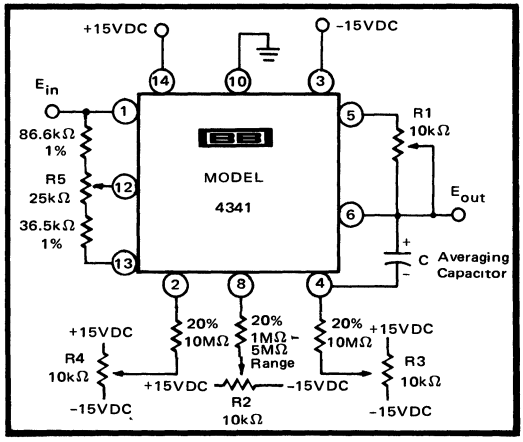


FIGURE 4. Expanded Trim Procedure (High Accuracy Applications).

NONUNITY GAINS

Gain values greater than unity can be achieved by inserting resistor R_x between pin 5 and pin 6. $R_x \simeq (A^2 - 1) \times 10k + 2k$ where A is the desired value of gain ($1 < A \leq 10$). (R_x is in ohms).

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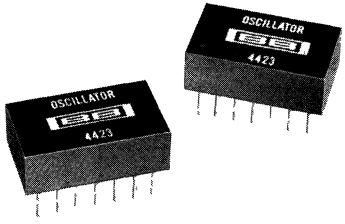

4423

PRECISION QUADRATURE OSCILLATOR

FEATURES

- SINE AND COSINE OUTPUTS
- RESISTOR-PROGRAMMABLE FREQUENCY
- WIDE FREQUENCY RANGE: 0.002Hz to 20kHz
- LOW DISTORTION: 0.2% max up to 5kHz
- EASY ADJUSTMENTS
- SMALL SIZE
- LOW COST

DESCRIPTION

The Model 4423 is a precision quadrature oscillator. It has two outputs 90 degrees out of phase with each other, thus providing sine and cosine wave outputs available at the same time. The 4423 is resistor programmable and is easy to use. It has low distortion (0.2% max up to 5kHz) and excellent frequency and amplitude stability.

The Model 4423 also includes an uncommitted operational amplifier which may be used as a buffer, a level shifter, or as an independent operational amplifier. The 4423 is packaged in a versatile, small, low-cost DIP package.

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SPECIFICATIONS

Prices and Specifications subject to change without notice

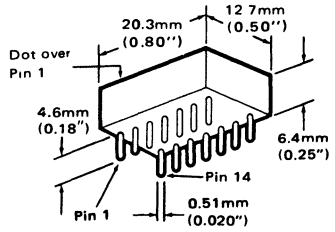
Specifications typical at 25°C and ±15VDC Power Supply Unless Otherwise Noted

ELECTRICAL

	MIN	TYP	MAX	UNITS
FREQUENCY				
Initial Frequency (no adjustments)	20.0k	20 5	21 0k	Hz
Frequency Range (using 2 R's only)	2k		20k	Hz
Frequency Range (using 2 R's and 2 C's)	.0.002		20k	Hz
Accuracy of Frequency Equation*		±1	±5	%
Stability vs Temperature		±50	±100	ppm/°C
Quadrature Phase Error		±0.1		degree
DISTORTION				
Sine Output (pin 1)				
0.002Hz to 5kHz			0 2	%
5kHz to 20kHz			0 5	%
Cosine Output (pin 7)				
0.002Hz to 5kHz		0.2		%
5kHz to 20kHz		0.8		%
Distortion vs Temperature		0.015		%/°C
OUTPUT				
Amplitude (Sine)				
At 20 kHz	6.5	7	7 5	V rms
vs Temperature		0.05		%/°C
vs Supply		0.4		V/V
Output Current	1.5	5		mA
Output impedance			1	Ω
UNCOMMITTED OP AMP				
Input Offset Voltage		1.5		mV
Input Bias Current		275		nA
Input Impedance		1		MΩ
Open Loop Gain		90		dB
Output Current	5			mA
POWER SUPPLY				
Rated Supply Voltage		±15		VDC
Supply Voltage Range	±12		±18	VDC
Quiescent Current		±9	±18	mA
TEMPERATURE RANGE				
Specifications	0		+70	°C
Operation	-25		+85	°C
Storage	-55		+125	°C

* May be trimmed for better accuracy.

MECHANICAL



ROW SPACING - 7.6 (0.300")
WEIGHT - 3.4 gms (0.12 oz)
CONNECTOR - 14 pin DIP connector

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

PIN CONNECTIONS

1. E_1, Sine Output
2. Frequency Adjustment
3. Frequency Adjustment
4. +In, Uncommitted Op Amp
5. -In, Uncommitted Op Amp
6. Output, Uncommitted Op Amp
7. E_2, Cosine Output
8. Frequency Adjustment
9. $-V_{CC}$, -15VDC
10. $+V_{CC}$, +15VDC
11. Common
12. Frequency Adjustment
13. Frequency Adjustment
14. Frequency Adjustment

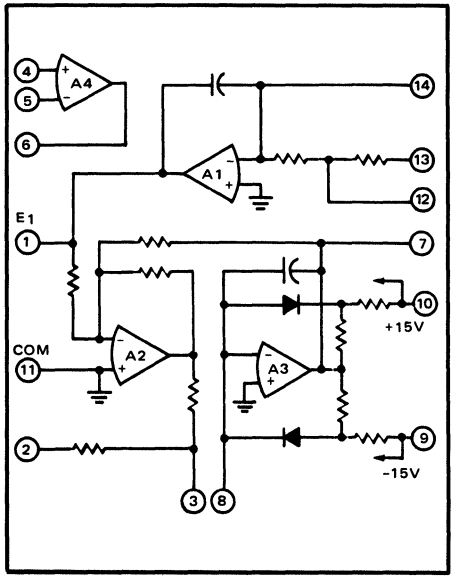


FIGURE 1. Equivalent Circuit.

TYPICAL PERFORMANCE CURVES

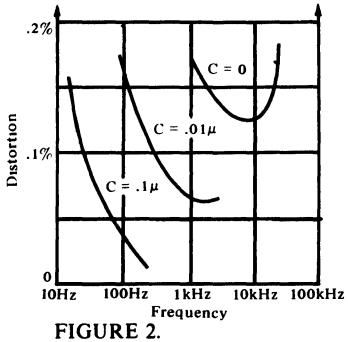


FIGURE 2.

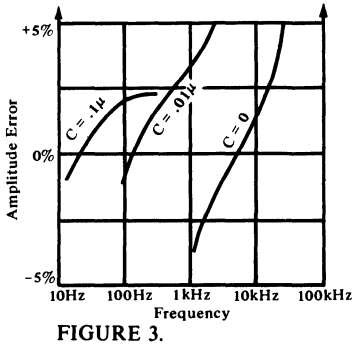


FIGURE 3.

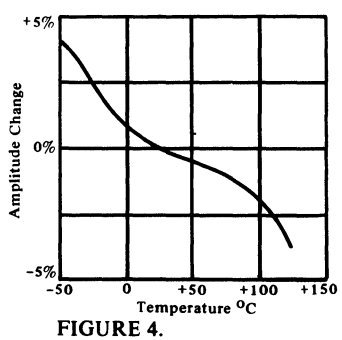


FIGURE 4.

EXTERNAL CONNECTIONS

1. 20 kHz Quadrature Oscillator

The 4423 does not require any external component to obtain a 20 kHz quadrature oscillator. The connection diagram is as shown in Figure 5.

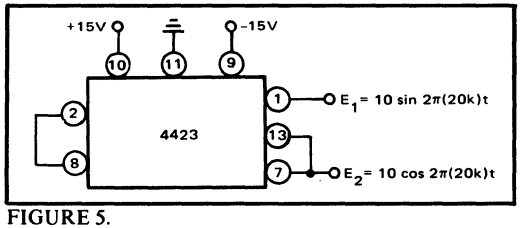


FIGURE 5.

2. Resistor Programmable Quadrature Oscillator

For resistor programmable frequencies in the 2 kHz to 20 kHz frequency range, the connection diagram is shown in Figure 6. Note that only two resistors of equal value are required. The resistor R can be expressed by,

$$R = \frac{3.785f}{42.05 - 2f}$$, R in kΩ, f in kHz

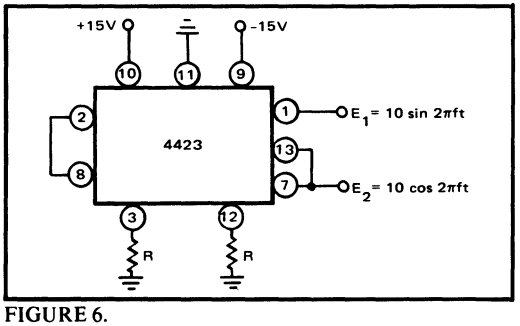


FIGURE 6.

3. Quadrature Oscillator Programmable to 0.002 Hz

For oscillator frequencies below 2000 Hz, use of two capacitors of equal value and two resistors of equal value as shown in Figure 7 is recommended. Connections shown in Figure 7 can be used to get oscillator frequency in the 0.002 Hz to 20 kHz range.

The frequency f can be expressed by:

$$f = \frac{42.05\ R}{(C + 0.001)\ (3.785 + 2R)}$$

where, f is in Hz
C is in μF
and R is in kΩ

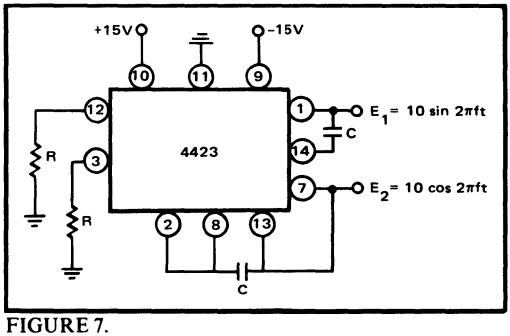


FIGURE 7.

For best results, the capacitor values shown in Table I should be selected with respect to their frequency ranges.

f	20 kHz to 2 kHz	2 kHz to 200 Hz	200 Hz to 20 Hz
C	0	0.01μF	0.1μF
20 Hz to 2 Hz	2 Hz to 0.2 Hz	0.2 Hz to 0.02 Hz	0.02 Hz to 0.002 Hz
1μF	10μF	100μF	1000μF

TABLE I.

After selecting the capacitor for a particular frequency the value of the required resistor can be obtained by using the resistor selection curve shown in Figure 8 or by the expression:

$$R = \frac{3.785f\ (C + 0.001)}{42.05 - 2f\ (C + 0.001)}$$

where,
R is in kΩ
f is in Hz
and C is in μF

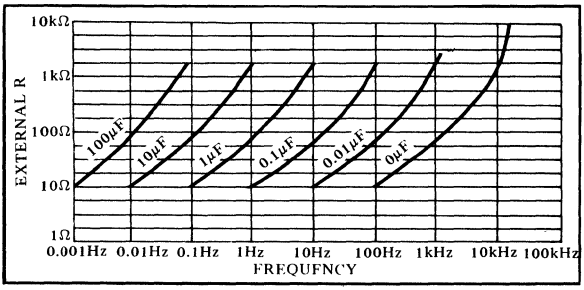


FIGURE 8.

The curves shown in Figure 8 are provided only as a nomographic design aid. The selection of capacitor values is not limited to the values shown in Figure 8. Any suitable combination of R and C values which satisfies the expression relating R, F and C as shown above, would work satisfactorily with the 4423.

NOTES ON TYPES OF CAPACITORS TO USE:

There are various kinds of capacitors available for use. There are polarized, also known as DC capacitors and non-polarized, also known as AC capacitors available. Of these two types, the polarized capacitors cannot be used with 4423 to set the frequencies.

Commonly available non-polarized capacitors include NPO ceramic, silver mica, teflon, polystyrene, polycarbonate, mylar, ceramic disc etc. A comparison is shown in Table II.

	Capacitance Range (μF)	Temperature Coefficients ppm/°C	Dissipation Factor (%)
NPO Ceramic	5pF - 0 1 μF	30	0 05
Silver Mica	5pF - 0 047 μF	60	0 05
Teflon	0 001 - 100 μF	200	0 01
Polystyrene	0 001 - 500 μF	100	0 03
Polycarbonate	0 001 - 1000 μF	90	0 08
Metalized Teflon	0 001 - 100 μF	60	0 1
Metalized Polycarbonate	0 001 - 1000 μF	10	0 4
Mylar	0.001 - 1000 μF	700	0.7
Metalized Mylar	0 001 - 2000 μF	700	1
Ceramic Disc	5pF - 0 5 μF	10,000	3

TABLE II.

For use with the 4423 oscillator, the choice of capacitors depends mainly on the user's application, error budget and cost budget. Note that the specifications of 4423 do not include the error contribution of the external components. The errors sourced by external components normally have to be added to the 4423 specifications.

As a general selection criteria we recommend the use of the above table. Start from the top of the list in the above table. If the capacitor is found unsuitable due to it being too large in size, too expensive, or is not easily available, then move down in the list for the next best selection. In any case do not choose or use any capacitors with dissipation factors greater than 1%. Such a capacitor would stop 4423 oscillation.

DISSIPATION FACTOR (DF)

A capacitor can be modeled by an ideal capacitor in parallel with an internal resistor whose value depends on its dissipation factor (DF). Mathematically, the internal resistor R is given by,

$$R = \frac{1}{2\pi f\, C(DF)}$$

where R is in Ω, f is the Hz, and C is in farads.

For example, the DF of ceramic disc capacitors is of the order of 3%, which for a 0.01 μF capacitor would look like having an internal resistor of 530kΩ at 1 kHz. The 530 kΩ value resistor is small enough to stop the 4423 oscillator from oscillating.

Some capacitor manufacturers use the terms "Power Factor" (PF) or "Q Factor" (Q) instead of the term "Dissipation Factor". These terms are similar in meaning and are mathematically related by,

$$(PF) = \frac{(DF)}{\sqrt{1 + (DF)^2}} \quad ; \quad Q = \frac{1}{(DF)}$$

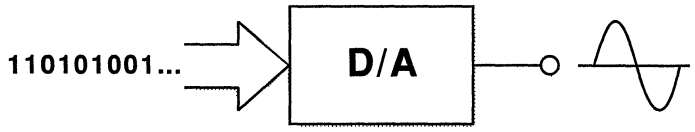
OSCILLATION AMPLITUDE

It takes a finite time to build up the amplitude of the oscillation to its final full scale value. There is a relationship between the amplitude build-up time and the frequency. The lower the frequency, the longer the amplitude build-up time. For example, typically it takes 250 seconds at 1 Hz, 30 seconds at 10 Hz, 4 seconds at 100 Hz, 400 milliseconds at 1 kHz, and 40 milliseconds at 10 kHz oscillator frequencies.

There are two methods available to shorten this normal amplitude build-up time. But there is also a relationship between the amplitude build-up time and distortion at final amplitude value. When the amplitude build-up time is shortened, the distortion can get worse.

One method to shorten the amplitude build-up time is to connect a resistor between pin 3 and pin 14. The lower this resistor is the shorter will be the time to build up amplitude of the oscillation, and worse will be the distortion of the output waveform. For example, a 100kΩ resistor would shorten the amplitude build up time from 15 seconds to 1 second at 20 Hz frequency, but the distortion could be degraded from tpically 0.05% to 0.5%.

The other method is to momentarily insert a 1kΩ resistor via a reset switch betwen pin 3 and pin 14. The amplitude of oscillation is built up instantaneously when the reset switch is pushed. There will be no degradation of distortion with this method since the 1kΩ resistor does not remain in the circuit continuously.



DIGITAL-TO-ANALOG CONVERTERS

Burr-Brown offers a broad variety of Digital-to-Analog (D/A) converter products engineered to meet the most critical requirements for stability and reliability.

General purpose instrumentation D/As range in resolution from 12 to 18 bits. These models include industry standard products—many originated by Burr-Brown—as well as more complete, higher accuracy solutions. Burr-Brown's products are carefully designed and manufactured to minimize product variations, making them ideal for test equipment, process control, and other industrial and analytical applications.

PCM D/A converters are designed and tested to deliver excellent dynamic performance. The resolutions of these products are 16 and 18 bits. Typical applications are compact disc players, digital frequency synthesis, and telecommunications systems.

High-speed D/A converters offer very fast settling current output. Models are available with TTL or ECL logic inputs. These products are ideal for very high frequency synthesis and control systems.

DIGITAL-TO-ANALOG CONVERTERS SELECTION GUIDES

The Selection Guides show parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

INSTRUMENTATION DIGITAL-TO-ANALOG CONVERTERS — **Boldface = NEW**

Description	Model	Resolution (Bits)	Linearity Error (%FSR)	Settling Time (µs)	Output Range (V)	Temp Range[1]	Pkg[2]	Q, BI[3] Screen	Page
Very High Resolution	**DAC729**	**18**	**±0.00075**	**5**	**5,10,20 U/B[4]**	**Com**	**HCD**	**Q, BI**	**6.1-80**
High Resolution	DAC700	16	±0.0015	1	–2mA U	Com, Ind, Mil	HCD	Q, BI	6.1-43
	DAC701	16	±0.0015	8	10 U	Com, Ind, Mil	HCD	Q, BI	6.1-43
	DAC702	16	±0.0015	1	±1mA B	Com, Ind, Mil	HCD,PDIP	Q, BI	6.1-43
	DAC703	16	±0.0015	8	±10 B	Com, Ind, Mil	HCD,PDIP, SOIC	Q, BI	6.1-43
High Resolution	DAC70BH	16	±0.003	1	±1mA, 0 to –2mA U/B	Ind	HCD	Q, BI	6.1-5
	DAC71	16	±0.003	8	±1mA, –2mA, 10, 20 U/B	Com	HCD	Q, BI	6.1-13
	DAC72BH	16	±0.003	1	±1mA, –2mA, 10, 20 U/B	Ind	HCD	Q, BI	6.1-5
Bus Interface, High Resolution	DAC705	16	±0.003	8	±5V	Com, Ind, Mil	HCD	Q, BI	6.1-53
	DAC706	16	±0.003	1	±1mA	Com, Ind, Mil	HCD	Q, BI	6.1-53
	DAC707	16	±0.003	8	±10 B	Com, Ind, Mil	HCD, PDIP	Q, BI	6.1-53
	DAC708	16	±0.003	1	±1mA, U/B 0 to –2mA	Com, Ind, Mil	HCD	Q, BI	6.1-53
	DAC709	16	±0.003	8	±5,±10,10 U/B	Com, Ind, Mil	HCD	Q, BI	6.1-53
Dual, Bus Interface, High Resolution	**DAC725**	**16**	**±0.003**	**8**	**±5,±10,10 B**	**Com, Ind**	**HCD, PDIP**	**Q, BI**	**6.1-72**
Low Cost, High Resolution	DAC710	16	±0.003	8 typ	±1mA	Com	HCD		6.1-65
	DAC711	16	±0.003	8 typ	±10	Com	HCD		6.1-65
	DAC1600	16	±0.003	8 typ	±10 B	Com	PDIP		6.1-108
Low Cost, Bus Interface	DAC811	12	±0.006	4	±5,±10,10 U/B	Com, Ind, Mil	HCD, PDIP, SOIC	Q, BI	6.1-90
	DAC1201	12	±0.018	4 typ	±5,±10,10 U/B	Com	PDIP		6.1-103
CMOS, Industry Std	**DAC7541A**	**12**	**±0.012**	**1**	**Multiplying**	**Com, Ind, Mil**	**HCD, PDIP, SOIC**	**Q, BI**	**6.1-112**
	DAC7545	**12**	**±0.012**	**2**	**Multiplying**	**Com, Ind, Mil**	**HCD, PDIP, SOIC**	**Q, BI**	**6.1-120**

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) HCD = Hermetic Ceramic DIP, PDIP = Plastic DIP, SOIC = Surface Mount Package. (3) Q indicates that optional reliability screening is available for the model. BI indicates that an optional 160 hour burn-in is available for the model. (4) U/B indicates the output voltage polarity range for the model: U = unipolar, B = bipolar.

(Continued on next page.)

INSTRUMENTATION DIGITAL-TO-ANALOG CONVERTERS (Continued)

Description	Model	Resolution (Bits)	Linearity Error (%FSR)	Settling Time (µs)	Output Range (V)	Temp Range[1]	Pkg[2]	Q, BI[3] Screen	Page
Bus Interface	**DAC8012**	**12**	**±0.012**	**1**	**Multiplying**	**Com, Ind, Mil**	**HCD, PDIP, SOIC**	**Q, BI**	**6.1-127**
Lowest Cost Industry Std	DAC1200	12	±0.018	0.3, 3 typ	±1mA,–2mA, 10,20 U/B		PDIP		6.1-99
Low Cost Industry Std	DAC80	12	±0.012	0.3, 3 typ	±1mA,–2mA, 10,20 U/B	Com,Ind	HCD, PDIP	Q, BI	6.1-27
	DAC85H	12	±0.012	0.3, 3 typ	±1mA,–2mA, 10,20 U/B	Com,Ind	HCD	Q, BI	6.1-35
Mlitary Temp Industry Std	DAC87H	12	±0.012	0.3, 3 typ	±1mA,–2mA, 10,20 U/B	Mil	HCD	Q, BI	6.1-35

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) HCD = Hermetic Ceramic DIP, PDIP = Plastic DIP, SOIC = Surface Mount Package. (3) Q indicates that optional reliability screening is available for the model. BI indicates that an optional 160 hour burn-in is available for the model. (4) U/B indicates the output voltage polarity range for the model: U = unipolar, B = bipolar.

AUDIO, COMMUNICATIONS, DSP DIGITAL-TO-ANALOG CONVERTERS **Boldface = NEW**

Model	Resolution (Bits)	Linearity Error (%FSR)	Settling Time (µs)	Output Range (V)	Temp Range[1]	Pkg[2]	Q, BI[3] Screen	Page
DAC63	12	±0.012	50ns	±5, 10mA	Ind	24-p HDIP	NA	6.2-135
DAC65	**12**	**±0.012**	**40ns**	**±1.2, ±6.35mA**	**Ind**	**24-p HDIP**	**Q**	**6.2-143**
DAC812	12	±0.012	50ns	±5, 10mA	Ind	24-p HDIP	NA	6.2-146

Model	Resolution (Bits)	Max THD+N (V_{OUT} = ±FS)	Output Range (V)	Input Format	Supply Range (V)	Pkg	Power Dissipation (mW)	Page
PCM53	16	–88dB (JG)	±10 (–V) –88dB (JP) –92dB (KP)	Parallel ±1mA (–I)	±15, +5	24-p DIP	600	6.2-152
PCM54	16	–82dB (HP)	±3,±1mA –88dB (JP) –92dB (KP)	Parallel	±5 to ±12	28-p DIP	300	6.2-164
PCM55	16	–82dB (HP)	±3,±1mA –88dB (JP)	Parallel	±5 to ±12	24-p SOIC	125	6.2-164

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) HCD = Hermetic Ceramic DIP, PDIP = Plastic DIP, SOIC = Surface Mount Package. (3) Q indicates that optional reliability screening is available for the model. BI indicates that an optional 160 hour burn-in is available for the model. (4) U/B indicates the output voltage polarity range for the model: U = unipolar, B = bipolar.

(Continued on next page.)

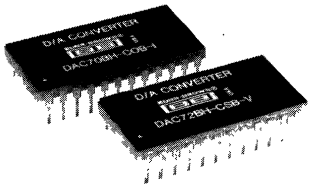
Model	Resolution (Bits)	Max THD+N (V_{OUT} = ±FS)	Output Range (V)	Input Format	Supply Range (V)	Pkg	Power Dissipation (mW)	Page
PCM56	**16**	**–82dB (P) –88dB (P-J) –92dB (P-K)**	**±3, ±1mA**	**Serial Latched**	**±5 to ±12**	**16-p DIP**	**260**	**6.2-172**
PCM60	**16**	**–82dB (P) –88dB (P-J) –92dB (P-K)**	**2.8Vp-p 2-Channel**	**Serial Latched**	**+5**	**24-p SOIC**	**50**	**6.2-186**
PCM58	**18**	**–92dB (P) –94dB (P-J) –96dB (P-K)**	**±1mA**	**Serial Latched**	**+5, –12**	**28-p DIP**	**400**	**6.2-180**
PCM64	**18**	**–96dB**	**±1mA**	**Parallel**	**+5, –15**	**42-p "Shrink" DIP**	**400**	**6.2-194**

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) HCD = Hermetic Ceramic DIP, PDIP = Plastic DIP, SOIC = Surface Mount Package. (3) Q indicates that optional reliability screening is available for the model. BI indicates that an optional 160 hour burn-in is available for the model. (4) U/B indicates the output voltage polarity range for the model: U = unipolar, B = bipolar.

MODELS STILL AVAILABLE BUT NOT FEATURED IN THIS BOOK

DAC10HT
DAC90BG
DAC90SG
DAC800P-CBI-V
DAC800P-CBI-I
DAC800-CBI-V
DAC800-CBI-I
DAC850-CBI-V
DAC850-CBI-I
DAC851-CBI-V
DAC851-CBI-I

BURR-BROWN®



DAC70BH
DAC72BH

Monolithic 16-Bit DIGITAL-TO-ANALOG CONVERTERS

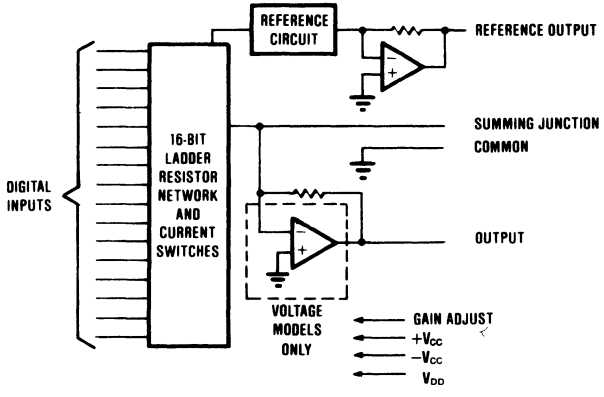
FEATURES

- 16-BIT RESOLUTION
- ±0.003% MAXIMUM NONLINEARITY
- LOW DRIFT ±7ppm/°C, (TYPICAL)
- MONOLITHIC CONSTRUCTION
- EXACT DAC70/72 HYBRID REPLACEMENT
- MONOTONIC (AT 14 BITS) OVER FULL SPECIFICATION TEMPERATURE RANGE
- CURRENT AND VOLTAGE MODELS

DESCRIPTION

The DAC70BH/72BH are complete 16-bit digital-to- analog converters that include a precision buried-zener voltage reference and a low-noise, fast-setting output operational amplifier (voltage output models), all on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 14-bit monotonicity over the entire specified temperature range but also a maximum end-point linearity error of ±0.003% of full-scale range. Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C-, 54/74HC-compatible over the entire temperature range. Outputs of 0 to +10V, ±10V, 0 to −2mA, and ±1mA are available.

These D/A converters are packaged in hermetic 24-pin ceramic side-brazed packages.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-626A

SPECIFICATIONS

ELECTRICAL

Typical at T_A = +25°C and rated power supplies unless otherwise noted.

MODEL	DAC70BH			DAC72BH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution, CSB, COB			16			*	Bits
Digital Inputs[1]: V_{IH}	+2.4		+5 5	*		*	V
V_{IL}	0		+0.4	*		*	V
I_{IH} V_I = +2.7V			+40			*	µA
I_{IL} V_I = +0.4V			−1.6			*	mA
TRANSFER CHARACTERISTICS							
ACCURACY[2]							
Linearity Error At +25°C			±0.003			*	% of FSR[3]
Gain Error[4]: Voltage					±0.05	±0.15	%
Current			±0.05		±0.05	±0.25	%
Offset Error[4]: Voltage, Unipolar					±0.10	±2	mV
Bipolar						±10	mV
Current, Unipolar			±1			*	µA
Bipolar			±1			±5	µA
Monotonicity Temperature Range (14 bits)	−25		+85	*		*	°C
DRIFT (OVER SPECIFIED TEMPERATURE RANGE)							
Total Bipolar Drift (Includes							
Gain, Offset, and Linearity Drift):[5] Voltage					±5	±11	ppm-of FSR/°C
Current		±10			*	±40	ppm of FSR/°C
Total Error Over Temperature Range:							
Voltage, Unipolar						±0.072	% of FSR
Bipolar						±0.072	% of FSR
Current, Unipolar		±0 12				±0.24	% of FSR
Bipolar		±0.12				±0.24	% of FSR
Gain: Voltage					±5	±20	ppm/°C
Current			±7			±47	ppm/°C
Offset. Voltage, Unipolar					±1	±2	ppm of FSR/°C
Bipolar						±8	ppm of FSR/°C
Current, Unipolar		±1				±1	ppm of FSR/°C
Bipolar			±5			±35	ppm of FSR/°C
Differential Linearity over Temperature		±1				±1	ppm of FSR/°C
Linearity over Temperature			±2			±1	ppm of FSR/°C
SETTLING TIME[6]							
Voltage Models (to ±0.003% of FSR)							
Output: 20V Step					5	10	µs
1LSB Step[7]					3	5	µs
Slew Rate					10		V/µA
Switching Transient[8]					500		mV
Current Models (to ±0.003% of FSR)							
Output, 2mA step: 10Ω to 100Ω load		15				1	µs
1kΩ load		50				3	µs
OUTPUT							
ANALOG OUTPUT							
Voltage Models							
Ranges: CSB					0 to +10		V
COB					±10		V
Output Current				±5			mA
Output Impedance (DC)					0.05		Ω
Short Circuit Duration					Indefinite to Common		
Current Models							
Ranges: CSB		0 to −2			*		mA
COB		±1			*		mA
Output Impedance: Unipolar		4.0			*		kΩ
Bipolar		2.45			*		kΩ
Compliance		±2.5			*		V
INTERNAL VOLTAGE REFERENCE	6.0	6.3	6.6	*	*	*	V
Maximum External Current		±200				±200	µA
Temperature Coefficient of Drift		±7			±10		ppm/°C

ELECTRICAL (CONT)

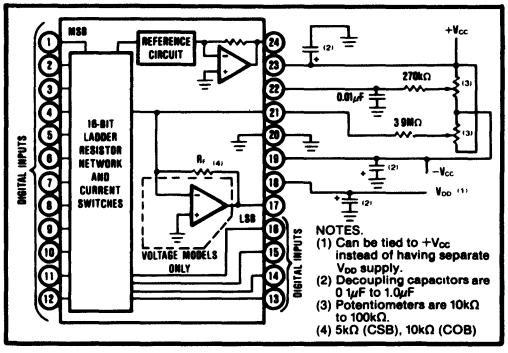
Typical at T_A = +25°C and rated power supplies unless otherwise noted.

MODEL	DAC70BH			DAC72BH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
POWER SUPPLY SENSITIVITY							
Unipolar Offset: ±15VDC		± 0001			*		% of FSR/% V_{CC}
+5VDC		± 0001			*		% of FSR/% V_{DD}
Bipolar Offset: ±15VDC		± 0004			*		% of FSR/% V_{CC}
+5VDC		±.0001			*		% of FSR/% V_{DD}
Gain: ±15VDC		±0 001			*		% of FSR/% V_{CC}
+5VDC		± 0005			*		% of FSR/% V_{DD}
POWER SUPPLY REQUIREMENTS							
Voltage	±14 5, +4.75	±15.0, +5.0	±15.5, +5.25	*	*	*	VDC
Supply Drain: ±15VDC (no load)		±20			*	±30	mA
+5VDC (logic supply)		+5			*	±10	mA
TEMPERATURE RANGE							
Specification	−25		+85	*		*	°C
Storage	−60		+150	*		*	°C

*Specification same as DAC70

NOTES: (1) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC, and 54/74HTC compatible over the operating voltage range of V_{DD} = +5V to +15V and over the specified temperature range. The input switching threshold remains at the TTL threshold of 1 4V over the supply range of V_{DD} = +5V to +15V. (2) Current-output models are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all parameters except settling time. (3) FSR means full-scale range and is 20V for the ±10V range (COB-V), 10V for the 0 to +10V range (CSB-V) FSR is 2mA for the ±1mA range (COB-I) and the 0 to −2mA range (CSB-I) (4) Adjustable to zero with external trim potentiometer (5) With gain and zero errors adjusted to zero at +25°C (6) Maximum represents the 3σ limit. Not 100% tested for this parameter. (7) LSB is for 14-bit resolution. (8) At the major carry, 7FFF$_H$ to 8000$_H$ and 8000$_H$ to 7FFF$_H$

CONNECTION DIAGRAM

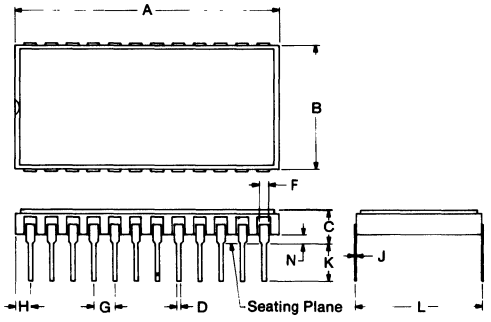


PIN ASSIGNMENTS

I Models	Pin No	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
Bit 12	12	Bit 12
Bit 13	13	Bit 13
Bit 14	14	Bit 14
Bit 15	15	Bit 15
(LSB) Bit 16	16	Bit 16 (LSB)
R_F	17	V_{OUT}
+5VDC	18	+5VDC
-15VDC	19	-15VDC
COMMON	20	COMMON
I_{OUT}	21	SUMMING JUNCTION
GAIN ADJUST	22	GAIN ADJUST
+15VDC	23	+15VDC
6 3V REF OUT	24	6.3V REF. OUT

MECHANICAL

H Package–24-Pin Hermetic Ceramic



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 238	1 262	31 45	32 05
B	586	602	14 88	15.29
C	160	196	4.06	4 98
D	016	020	0.41	0 51
F	038	042	0 97	1 07
G	.100 BASIC		2 54 BASIC	
H	067	.085	1.70	2 16
J	008	012	0 20	0 30
K	170 BASIC		4 32 BASIC	
L	600 BASIC		15 24 BASIC	
N	040	060	1 02	1 52

ABSOLUTE MAXIMUM SPECIFICATIONS

+V_{CC} to Common	0V to +16.5V
−V_{CC} to Common	0V to −16.5V
+V_{DD} to Common	0V to +16.5V
Logic Inputs to Common	0V to V_{DD}
Maximum Power Dissipation	1000mW
Lead Temperature (10s)	300°C

ORDERING INFORMATION

MODELS	
Complementary Offset Binary Coding	
DAC70BH-COB-I	I_{OUT} DAC
DAC70BH-COB-IBI	Burn-in Option[1]
DAC72BH-COB-I	I_{OUT} DAC
DAC72BH-COB-IBI	Burn-in Option[1]
DAC72BH-COB-V	V_{OUT} DAC
DAC72BH-COB-VBI	Burn-in Option[1]
Complementary Straight Binary Coding	
DAC70BH-CSB-I	I_{OUT} DAC
DAC70BH-CSB-IBI	Burn-in Option[1]
DAC72BH-CSB-I	I_{OUT} DAC
DAC72BH-CSB-IBI	Burn-in Option[1]
DAC72BH-CSB-V	V_{OUT} DAC
DAC72BH-CSB-VBI	Burn-in Option[1]

NOTE. 1) 160 hours at 85°C or equivalent. See text

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC70BH/72BH accept complementary digital input codes in either binary format (CSB, Unipolar or COB, Bipolar). The COB models may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

TABLE I. Digital Input Codes.

	Analog Output		
Digital Input Codes	Complementary Straight Binary (CSB)	Complementary Offset Binary (COB)	Complementary Two's Complement (CTC)*
0000_H	+Full Scale	+Full Scale	-1LSB
$7FFF_H$	+1/2 Full Scale	Bipolar Zero	-Full Scale
8000_H	+1/2 Full Scale -1LSB	-1LSB	+Full Scale
$FFFF_H$	Zero	-Full Scale	Bipolar Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (all bits ON point and all bits OFF point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output step sizes can be between 1/2LSB and 3/2LSB when the input changes from one adjacent input state to the next. A negative DLE specification of no more than −1LSB (−0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC70BH/72BH are specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by : (1) testing the end point differences for each D/A at t_{min}, +25°C and t_{max}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Offset Drift

Offset drift is a measure of the change in the output with $FFFF_H$ applied to the digital inputs over the specified temperature range. The maximum change in offset at t_{min} or t_{max} is referenced to the offset error at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per degree centigrade (ppm of FSR/°C).

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2LSB for 14 bits) for two input conditions: a full-scale range change of 20V (COB) or 10V (CSB) and a 1LSB change at the "major carry," the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next).

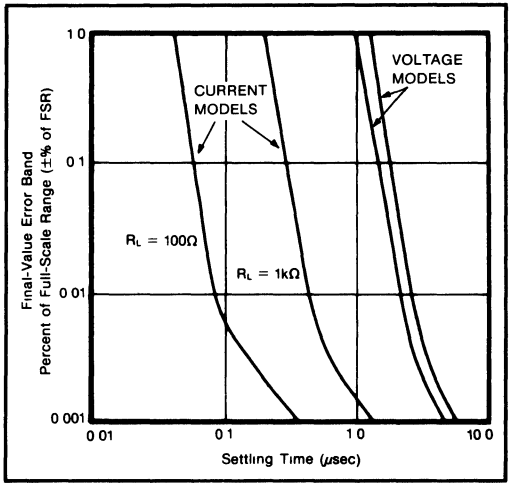


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

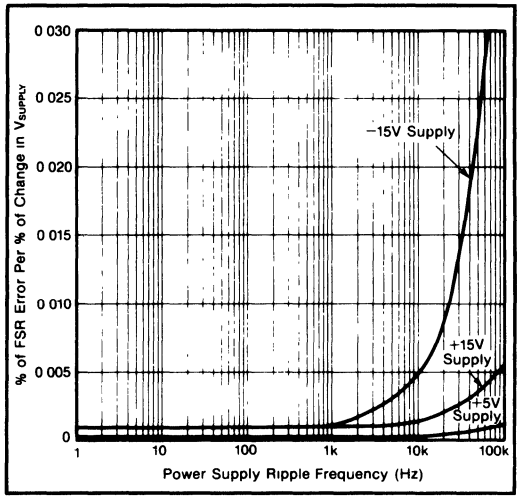


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

Current Output

Settling times are specified to ±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

REFERENCE SUPPLY

All models have an internal low-noise +6.3V reference voltage derived from an on-chip buried zener diode. This reference voltage is available to the user. A minimum of 200μA is available for external loads. Since the output impedance of the reference output is typically 1Ω, the external load should remain constant.

If a varying load is to be driven by the reference supply, an external buffer amplifier is recommended to drive the load in order to isolate the Bipolar Offset (connected internally to the reference) from load variations.

BURN-IN SCREENING

Burn-in screening is an option available for the entire DAC70BH/72BH family of products. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add " BI" to the base model number.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF to 10μF tantalum recommended) should be located close to the DAC70BH/72BH. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 510kΩ resistors (20% carbon or better) should be located close to the DAC70BH/72BH to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ. A 0.001μF to 0.01μF ceramic capacitor should be connected from Gain Adjust (pin 22) to common to prevent noise pickup. Refer to

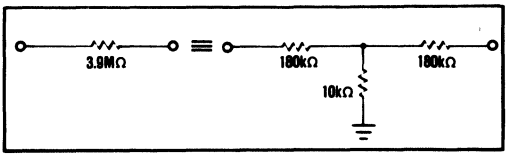


FIGURE 3. Equivalent Resistances.

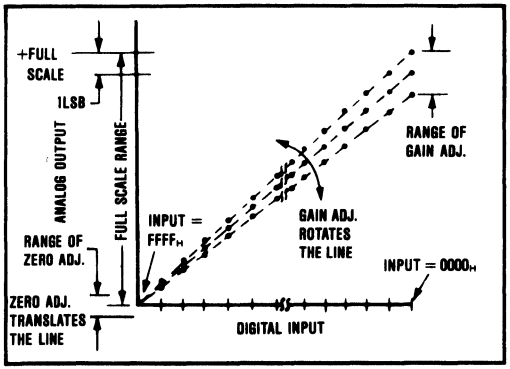


FIGURE 4. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

Figures 4 and 5 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters.

OFFSET ADJUSTMENT

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the offset potentiometer for zero output.

For bipolar (COB) configurations, apply the digital input code that should produce the maximum negative output voltage. The COB model is internally connected for a 20V FSR range where the maximum negative output voltage is −10V. See Table II for corresponding codes and the Connection Diagram for offset adjustment connections. Offset adjust should be made prior to gain adjust.

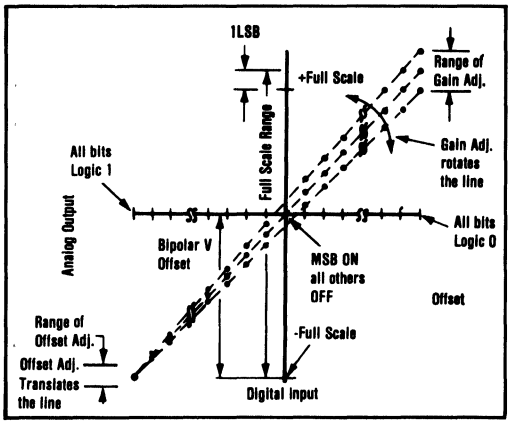


FIGURE 5. Relationship of Offset and Gain Adjustments for a Bipolar D A Converter.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output voltage. Adjust the gain potentiomenter for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagram for gain adjustment connections.

INSTALLATION CONSIDERATIONS

This D/A converter family is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bit 15 and 16 should be connected to V_{DD} through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and

TABLE II. Digital Input and Analog Output Relationships.

VOLTAGE OUTPUT MODELS						
	Analog Output					
	Unipolar			Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μV)	153	305	610	305	610	1224
0000$_H$ (V)	+9 99985	+9 99969	+9 99939	+9.99969	+9.99939	+9 99878
FFFF$_H$ (V)	0	0	0	−10.0000	−10.0000	−10.0000
CURRENT OUTPUT MODELS						
	Analog Output					
	Unipolar			Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μA)	0 031	0.061	0.122	0 031	0 061	0.122
0000$_H$ (mA)	−1 99997	−1 99994	−1 99988	−0 99997	−0.99994	−0.99988
FFFF$_H$ (mA)	0	0	0	+1 00000	+1 00000	+1 00000

connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 18 inches of wire will produce a 1LSB error in the analog output voltage!

In Figures 6, 7, and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2, simply introduces a gain error and can be removed during initial calibration. R_3 is part of R_L, if the output voltage is sensed at Common, and therefore introduces no error. If R_L is variable, then R_2 should be less than $R_{L\min}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if $R_{L\min}$ is 5kΩ, then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_4 is negligible.

In many applications it is impractical to sense the output voltage at the output pin. Sensing the output voltage at the system ground point is permissible with the DAC70 family because the D/A converter is designed to have a constant return current of approximately 2mA flowing from Common. The variation in this current is under 20μA (with changing input codes), therefore R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 ($R_4 \times$ 2mA) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figures 6, 7, and 8.

Figures 7 and 8 show two methods of connecting the current output models with external precision output op amps. By sensing the output voltage at the load resistor

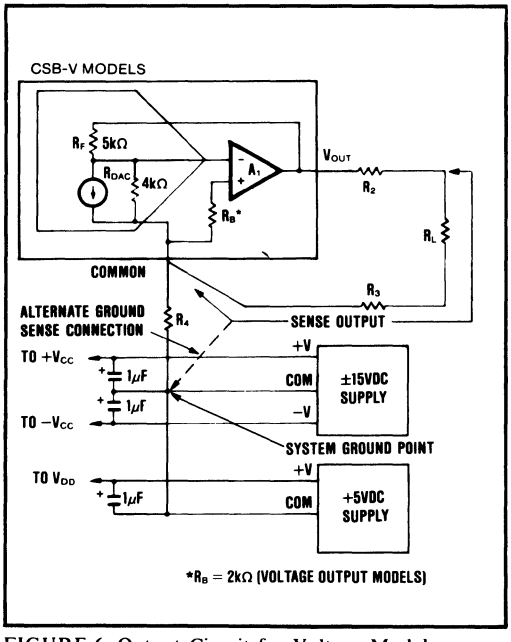


FIGURE 6. Output Circuit for Voltage Models.

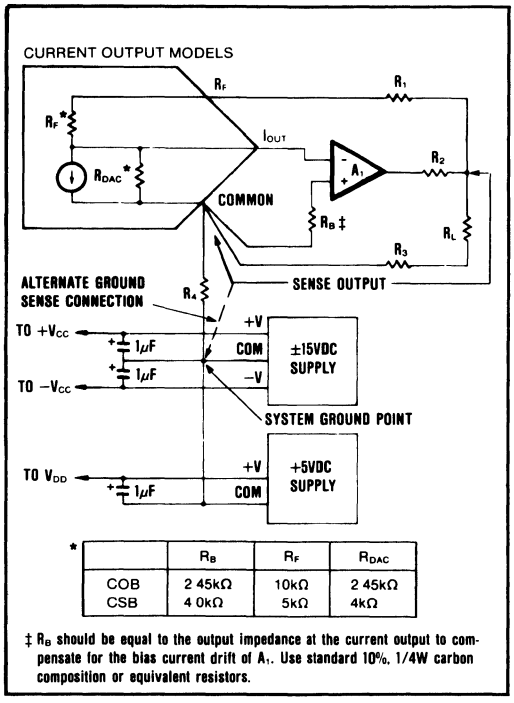


FIGURE 7. Preferred External Op Amp Configuration.

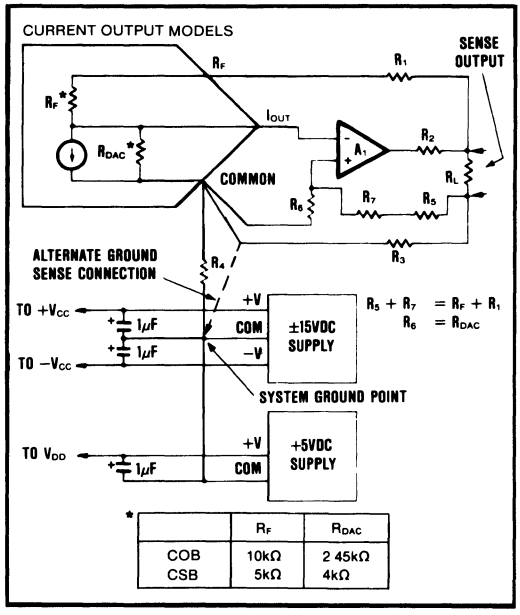


FIGURE 8. Differential Sensing Output Op Amp Configuration.

(i.e., by connecting R_F to the output of A_1 at R_L), the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

If the output cannot be sensed at Common or the system ground point as mentioned above, the differential output circuit shown in Figure 8 is recommended. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible, the circuit of Figure 8 can be reduced to the one shown in Figure 7. Again the effect of R_4 is negligible. The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a single lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT DACs

The DAC70BH/72BH current output models will drive the summing junction of an op amp to produce an output voltage as shown in Figure 9. Use of the internal feedback resistor is required to obtain specified gain accuracy and low gain drift.

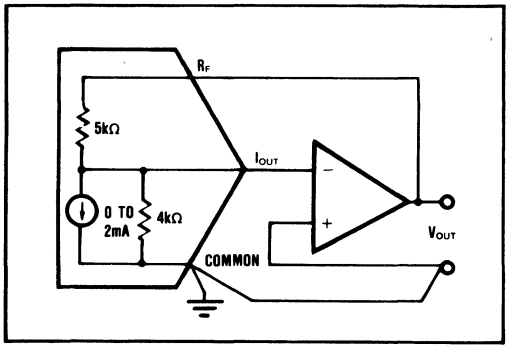


FIGURE 9. External Op Amp Using Internal Feedback Resistors.

Current output models can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±50ppm/°C. The resistors in the D/A converter ratio track to ±1ppm/°C but their absolute TCR may be as high as ±50ppm/°C.

An alternative method of scaling the output voltage of the D/A converter and preserving the low gain drift is shown in Figure 10.

OUTPUTS LARGER THAN 20-VOLT RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and −2mA for unipolar voltage ranges (see Figure 11). Use protection diodes as shown when a high voltage op amp is used.

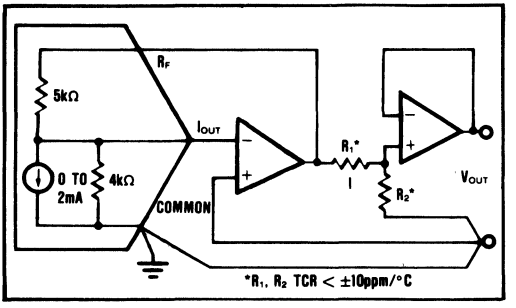


FIGURE 10. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift.

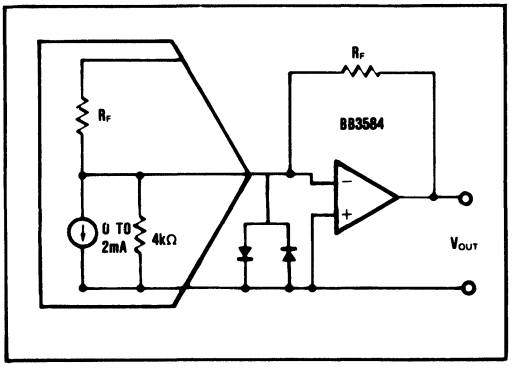
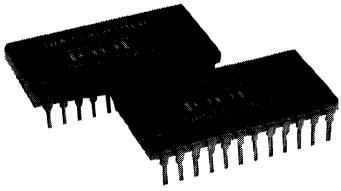


FIGURE 11. External Op Amp Using External Feedback Resistors.

BURR-BROWN®



DAC71

Monolithic 16-Bit DIGITAL-TO-ANALOG CONVERTER

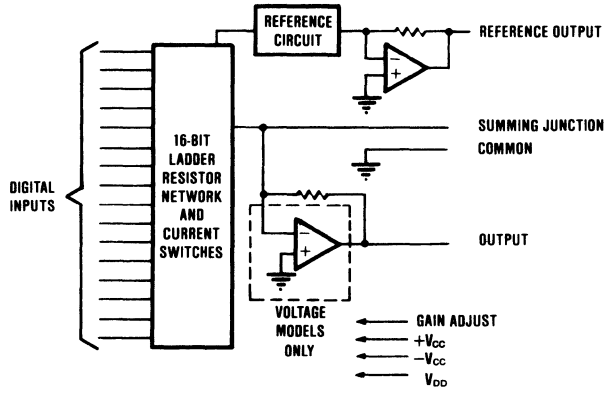
FEATURES

- 16-BIT RESOLUTION
- ±0.003% MAXIMUM NONLINEARITY
- LOW DRIFT ±7ppm/°C, (TYPICAL)
- MONOLITHIC CONSTRUCTION
- EXACT DAC71 HYBRID REPLACEMENT
- MONOTONIC (AT 14 BITS) OVER FULL SPECIFICATION TEMPERATURE RANGE
- CURRENT AND VOLTAGE MODELS

DESCRIPTION

The DAC71 is a complete 16-bit digital-to- analog converter that includes a precision buried-zener voltage reference and a low-noise, fast-setting output operational amplifier (voltage output models), all on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 14-bit monotonicity over the entire specified temperature range but also a maximum end-point linearity error of ±0.003% of full-scale range. Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C-, 54/74HC-compatible over the entire temperature range. Outputs of 0 to +10V, ±10V, 0 to −2mA, and ±1mA are available.

This D/A converter is packaged in a hermetic 24-pin ceramic side-brazed package.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-613C

SPECIFICATIONS

ELECTRICAL

Typical at T_A = +25°C and rated power supplies unless otherwise noted

MODEL	DAC71			UNITS
	MIN	TYP	MAX	
INPUT				
DIGITAL INPUT				
Resolution, CSB, COB			16	Bits
Digital Inputs[1]				
V_{IH}	+2 4		+5 5	V
V_{IL}	0		+0 4	V
I_{IH} V_I = +2 7V			+40	µA
I_{IL} V_I = +0 4V			−1 6	mA
TRANSFER CHARACTERISTICS				
ACCURACY[2]				
Linearity Error At +25°C			±0 003	% of FSR[3]
Gain Error[4] Voltage		±0 01	±0 10	%
Current		±0 05	±0 25	%
Offset Error[4]				
Voltage Unipolar		±0 10	±2	mV
Voltage Bipolar			±5	mV
Current Unipolar			±1	µA
Current Bipolar			±5	µA
Monotonicity Temperature				
Range (14 bits)	0		+70	°C
DRIFT (OVER SPECIFIED TEMPERATURE RANGE)				
Total Bipolar Drift (Includes Gain, Offset, and Linearity Drift)[5]				
Voltage		±7	±15	ppm of FSR/°C
Current		±15	±50	ppm of FSR/°C
Total Error Over Temperature Range				
Voltage, Unipolar			±0 083	% of FSR
Voltage, Bipolar			±0 071	% of FSR
Current, Unipolar			±0 23	% of FSR
Current, Bipolar			±0 23	% of FSR
Gain Voltage			±20	ppm/°C
Current			±60	ppm/°C
Offset Voltage, Unipolar		±1	±2	ppm of FSR/°C
Voltage, Bipolar			±10	ppm of FSR/°C
Current, Unipolar			±1	ppm of FSR/°C
Current, Bipolar			±40	ppm of FSR/°C
Differential Linearity over Temperature			±2	ppm of FSR/°C
Linearity over Temperature			±2	ppm of FSR/°C
SETTLING TIME[6]				
Voltage Models (to ±0 003% of FSR)				
Output 20V Step		5	10	µs
1LSB Step[7]		3	5	µs
Slew Rate		10		V/µs
Switching Transient[8]		500		mV
Current Models (to ±0 003% of FSR)				
Output, 2mA step				
10Ω to 100Ω load			1	µs
1kΩ load			3	µs

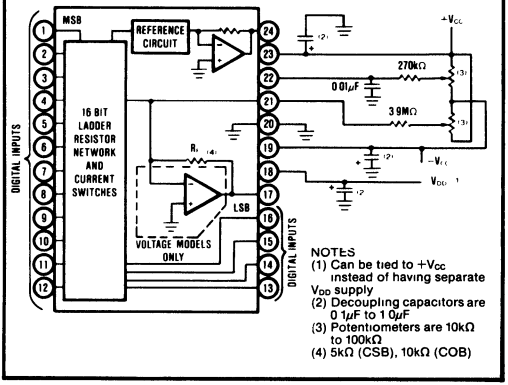
MODEL	DAC71			UNITS
	MIN	TYP	MAX	
OUTPUT				
ANALOG OUTPUT				
Voltage Models				
Ranges CSB		0 to +10		V
COB		±10		V
Output Current	±5			mA
Output Impedance (DC)		0 05		Ω
Short Circuit Duration		Indefinite to Common		
Current Models				
Ranges CSB		0 to −2		mA
COB		±1		mA
Output Impedance				
Unipolar		4 0		kΩ
Bipolar		2 45		kΩ
Compliance		±2 5		V
INTERNAL VOLTAGE REFERENCE	6 0	6 3	6 6	V
Maximum External Current		±200		µA
Temperature Coefficient of Drift		±10		ppm/°C
POWER SUPPLY SENSITIVITY				
Unipolar Offset ±15VDC		± 0001		% of FSR/% V_{CC}
+5VDC		± 0001		% of FSR/% V_{DD}
Bipolar Offset ±15VDC		± 0004		% of FSR/% V_{CC}
+5VDC		± 0001		% of FSR/% V_{DD}
Gain ±15VDC		±0 001		% of FSR/% V_{CC}
+5VDC		± 0005		% of FSR/% V_{DD}
POWER SUPPLY REQUIREMENTS				
Voltage	±14 5, +4 75	±15 0, +5 0	±15 5, +5 25	VDC
Supply Drain				
±15VDC (no load)		±20	±30	mA
+5VDC (logic supply)		+5	+10	mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Storage	−60		+150	°C

NOTES (1) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC, and 54/74HTC compatible over the operating voltage range of V_{DD} = +5V to +15V and over the specified temperature range The input switching threshold remains at the TTL threshold of 1 4V over the supply range of V_{DD} = +5V to +15V. (2) Current-output models are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all parameters except settling time (3) FSR means full-scale range and is 20V for the ±10V range (COB-V), 10V for the 0 to +10V range (CSB-V). FSR is 2mA for the ±1mA range (COB-I) and the 0 to −2mA range (CSB-I) (4) Adjustable to zero with external trim potentiometer (5) With gain and zero errors adjusted to zero at +25°C. (6) Maximum represents the 3σ limit Not 100% tested for this parameter. (7) LSB is for 14-bit resolution (8) At the major carry, $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$

PIN ASSIGNMENTS

I Models	Pin No	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
Bit 12	12	Bit 12
Bit 13	13	Bit 13
Bit 14	14	Bit 14
Bit 15	15	Bit 15
(LSB) Bit 16	16	Bit 16 (LSB)
R_F	17	V_{OUT}
+5VDC	18	+5VDC
-15VDC	19	-15VDC
COMMON	20	COMMON
I_{OUT}	21	SUMMING JUNCTION
GAIN ADJUST	22	GAIN ADJUST
+15VDC	23	+15VDC
6 3V REF OUT	24	6 3V REF OUT

CONNECTION DIAGRAM



ORDERING INFORMATION

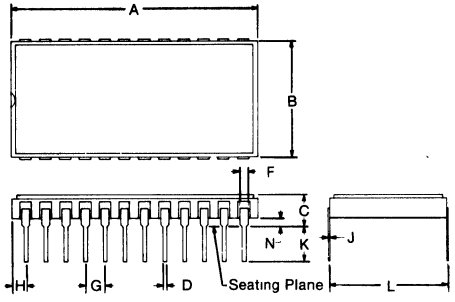
MODELS	
Complementary Offset Binary Coding	
DAC71-COB-I	I_{OUT} DAC
DAC71-COB-I-BI	Burn-in Option[1]
DAC71-COB-V	V_{OUT} DAC
DAC71-COB-I-BI	Burn-in Option[1]
Complementary Straight Binary Coding	
DAC71-CSB-I	I_{OUT} DAC
DAC71-CSB-I-BI	Burn-in Option[1]
DAC71-CSB-V	Standard V_{OUT} DAC
DAC71-CSB-I-BI	Burn-in Option[1]

NOTE 1) 160 hours at 85°C or equivalent See text

MECHANICAL

H Package-24-Pin Hermetic Ceramic

NOTES:
1. Leads in true position within 0.01" (.25mm) R and MMC at seating plane.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 238	1 262	31 45	32 05
B	586	602	14 88	15 29
C	160	196	4 06	4 98
D	016	020	0 41	0 51
F	038	042	0 97	1 07
G	100 BASIC		2 54 BASIC	
H	067	085	1 70	2 16
J	008	012	0 20	0 30
K	170 BASIC		4 32 BASIC	
L	600 BASIC		15 24 BASIC	
N	040	060	1 02	1 52

ABSOLUTE MAXIMUM SPECIFICATIONS

$+V_{CC}$ to Common	0V to +16.5V
$-V_{CC}$ to Common	0V to -16 5V
$+V_{DD}$ to Common	0V to +16 5V
Logic Inputs to Common	0V to V_{DD}
Maximum Power Dissipation	1000mW
Lead Temperature (10s)	300°C

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC71 accepts complementary digital input codes in either binary format (CSB, Unipolar or COB, Bipolar). The COB models may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

TABLE I. Digital Input Codes.

Digital Input Codes	Analog Output		
	Complementary Straight Binary (CSB)	Complementary Offset Binary (COB)	Complementary Two's Complement (CTC)*
0000_H	+ Full Scale	+ Full Scale	−1LSB
$7FFF_H$	±1/2Full Scale	Bipolar Zero	− Full Scale
8000_H	+1/2 Full Scale −1LSB	−1LSB	+ Full Scale
$FFFF_H$	Zero	− Full Scale	Bipolar Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (all bits ON point and all bits OFF point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output step sizes can be between 1/2LSB and 3/2LSB when the input changes from one adjacent input state to the next. A negative DLE specification of no more than −1LSB (−0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC71 is specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by: (1) testing the end point differences for each D/A at t_{MIN}, +25°C and t_{MAX}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Offset Drift

Offset drift is a measure of the change in the output with $FFFF_H$ applied to the digital inputs over the specified temperature range. The maximum change in offset at t_{MIN} or t_{MAX} is referenced to the offset error at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per degree centigrade (ppm of FSR/°C).

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

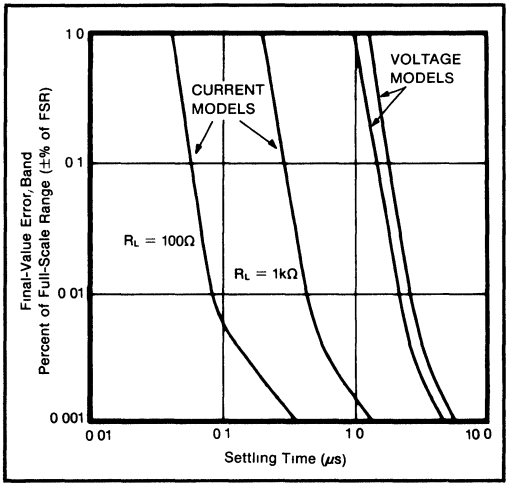


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2LSB for 14 bits) for two input conditions: a full-scale range change of 20V (COB) or 10V (CSB) and a 1LSB change at the "major carry," the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next).

Current Output

Settling times are specified to ±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply

($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). I is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

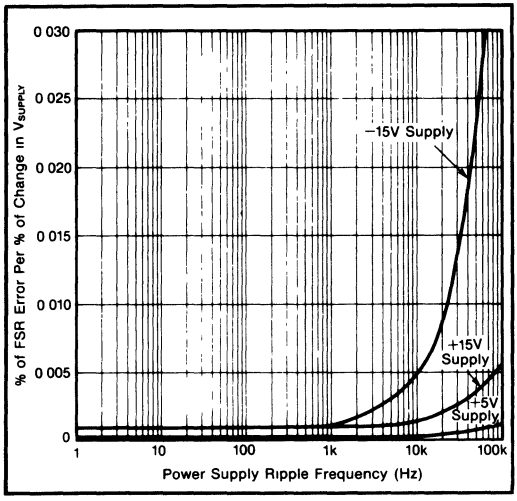


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

REFERENCE SUPPLY

All models have an internal low-noise +6.3V reference voltage derived from an on-chip buried zener diode. This reference voltage is available to the user. A minimum of 200μA is available for external loads. Since the output impedance of the reference output is typically 1Ω, the external load should remain constant.

If a varying load is to be driven by the reference supply, an external buffer amplifier is recommended to drive the load in order to isolate the Bipolar Offset (connected internally to the reference) from load variations.

BURN-IN SCREENING

Burn-in screening is an option available for the entire DAC71 family of products. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF to 10μF tantalum recommended) should be located close to the DAC71. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 510kΩ resistors (20% carbon or better) should be located close to the DAC71 to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ. A 0.001μF to 0.01μF ceramic capacitor should be connected from Gain Adjust (pin 22) to common to prevent noise pickup. Refer to Figures 4 and 5 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters.

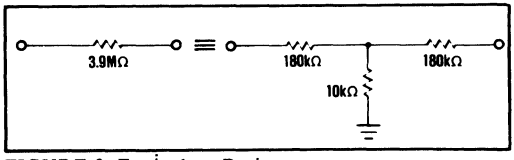


FIGURE 3. Equivalent Resistances.

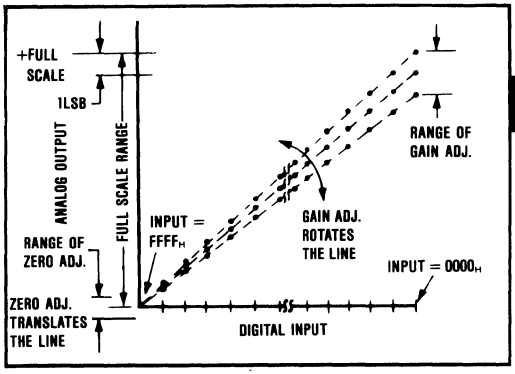


FIGURE 4. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

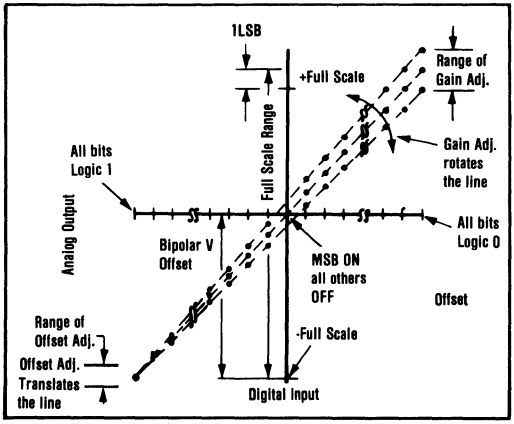


FIGURE 5. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

TABLE II. Digital Input and Analog Output Relationships.

VOLTAGE OUTPUT MODELS						
	Analog Output					
	Unipolar			Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μV)	153	305	610	305	610	1224
0000_H (V)	+9 99985	+9 99969	+9 99939	+9 99969	+9 99939	+9 99878
$FFFF_H$ (V)	0	0	0	−10 0000	−10 0000	−10 0000
CURRENT OUTPUT MODELS						
	Analog Output					
	Unipolar					
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μA)	0 031	0 061	0 122	0 031	0.061	0 122
0000_H (mA)	−1 99997	−1 99994	−1 99988	−0 99997	−0 99994	−0 99988
$FFFF_H$ (mA)	0	0	0	+1 00000	+1 00000	+1 00000

OFFSET ADJUSTMENT

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the offset potentiometer for zero output.

For bipolar (COB) configurations, apply the digital input code that should produce the maximum negative output voltage. The COB model is internally connected for a 20V FSR range where the maximum negative output voltage is −10V. See Table II for corresponding codes and the Connection Diagram for offset adjustment connections. Offset adjust should be made prior to gain adjust.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output voltage. Adjust the gain potentiomenter for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagram for gain adjustment connections.

INSTALLATION CONSIDERATIONS

This D/A converter is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bits 15 and 16 should be connected to V_{DD} through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a ±10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 18 inches of wire will produce a 1LSB error in the analog output voltage!

In Figures 6, 7, and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed during initial calibration. R_3 is part of R_L, if the output voltage is sensed at Common, and therefore introduces no error. If R_L is variable, then R_2 should be less than $R_{L\ MIN}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if $R_{L\ MIN}$ is 5kΩ, then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_4 is negligible.

In many applications it is impractical to sense the output voltage at the output pin. Sensing the output voltage at the system ground point is permissible with the DAC71 because the D/A converter is designed to have a constant

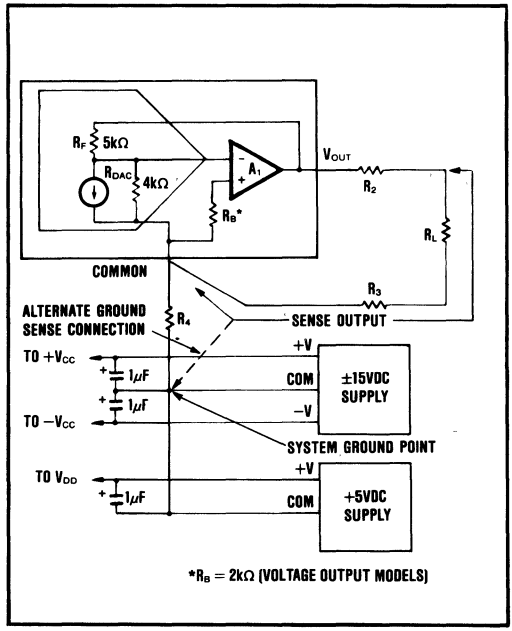


FIGURE 6. Output Circuit for Voltage Models.

return current of approximately 2mA flowing from Common. The variation in this current is under 20μA (with changing input codes), therefore R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 ($R_4 \times 2mA$) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figures 6, 7, and 8.

Figures 7 and 8 show two methods of connecting the current output models with external precision output op amps. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A_1 at R_L), the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

If the output cannot be sensed at Common or the system ground point as mentioned above, the differential output circuit shown in Figure 8 is recommended. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible, the circuit of Figure 8 can be reduced to the one shown in Figure 7. Again the effect of R_4 is negligible.

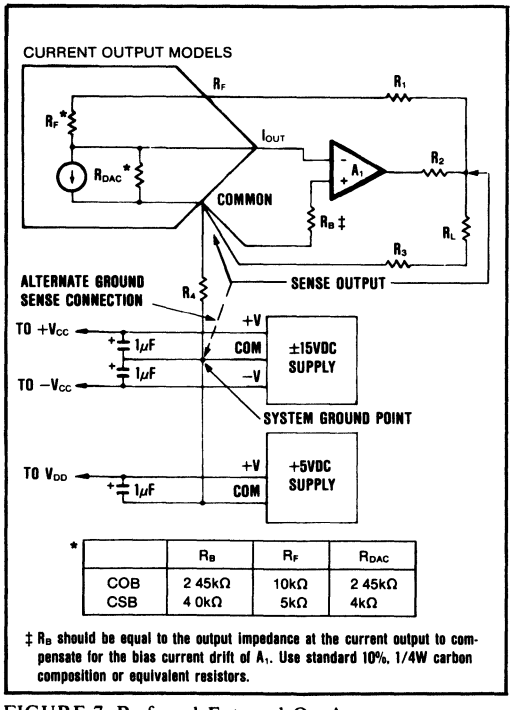


FIGURE 7. Preferred External Op Amp Configuration.

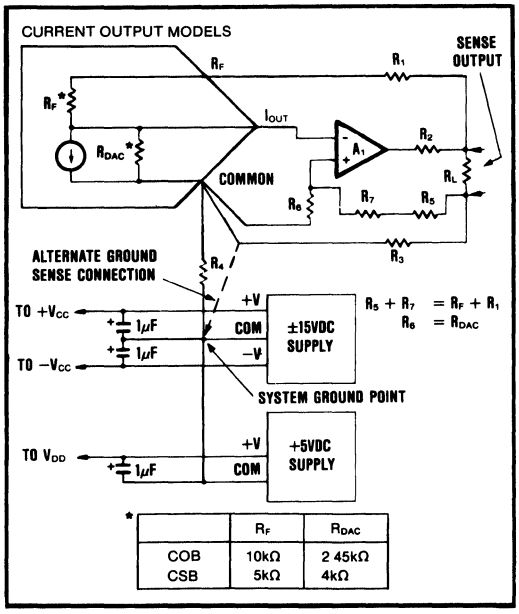


FIGURE 8. Differential Sensing Output Op Amp Configuration.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a single lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT DACs

The DAC71 current output models will drive the summing junction of an op amp to produce an output voltage as shown in Figure 9. Use of the internal feedback resistor is required to obtain specified gain accuracy and low gain drift.

Current output models can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±50ppm/°C. The resistors in the D/A converter ratio track to ±1ppm/°C but their absolute TCR may be as high as ±50ppm/°C.

An alternative method of scaling the output voltage of the D/A converter and preserving the low gain drift is shown in Figure 10.

OUTPUTS LARGER THAN 20V RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and −2mA for unipolar voltage ranges (see Figure 11). Use protection diodes as shown when a high voltage op amp is used.

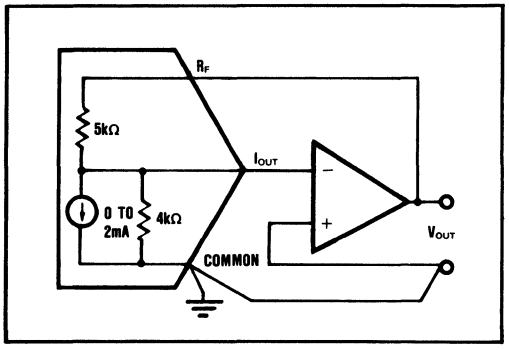


FIGURE 9. External Op Amp Using Internal Feedback Resistors.

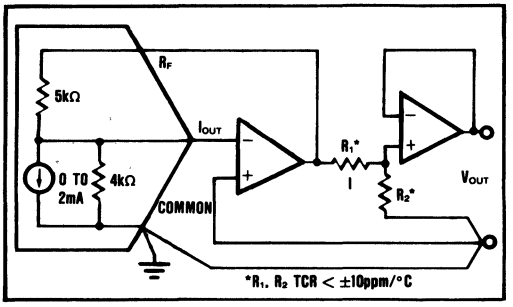


FIGURE 10. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift.

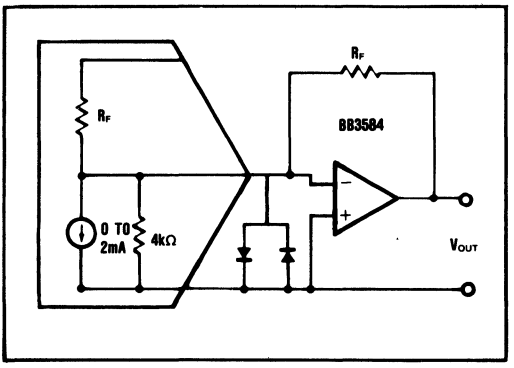
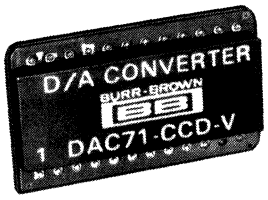


FIGURE 11. External Op Amp Using External Feedback Resistors.

BURR-BROWN®

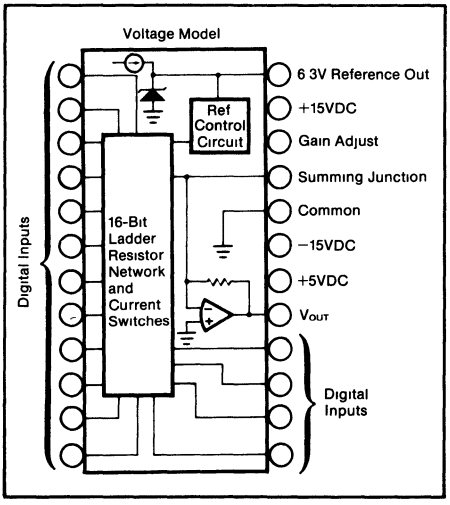


DAC71-CCD

High Resolution
16-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 16-BIT, 4-DIGIT RESOLUTION
- ±0.005% MAXIMUM NONLINEARITY
- LOW DRIFT, ±7ppm/°C TYPICAL
- CURRENT AND VOLTAGE MODELS
- LOW COST



DESCRIPTION

The DAC71 is a high quality 16-bit hybrid IC D/A converter available in a 24-pin dual-in-line ceramic package.

The DAC71 with internal reference and optional output amplifier offers a maximum linearity error of ±0.005% of FSR at room temperature and a maximum gain drift of ±20ppm/°C over a temperature range of 0°C to +70°C.

The DAC71-CCD accepts complementary 4-digit BCD TTL-compatible input codes.

Packaged within the DAC71 are fast-settling switches and stable laser-trimmed thin-film resistors that let you select two output ranges: 0 to +10VDC (DAC71-CCD-V) and 0 to −1.25mA (DAC71-CCD-I).

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-671

SPECIFICATIONS

ELECTRICAL

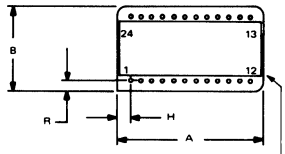
Typical at $T_A = 25°C$ and rated power supplies unless otherwise noted

MODEL	DAC71-CCD			
	MIN	TYP	MAX	UNITS
INPUT				
DIGITAL INPUT				
Resolution		4		Digits
Logic Levels (TTL-Compatible)[1]				
Logical "1" (at +40μA)	+2 4		+5 5	VDC
Logical "0" (at −1 6mA)	0		+0 4	VDC
TRANSFER CHARACTERISTICS				
ACCURACY				
Linearity Error at 25°C			±0 005	% of FSR[2]
Gain Error[3] Voltage		±0 01	±0 1	%
Current		±0 05	±0 25	%
Offset Error[3] Voltage, Unipolar		±0 1	±2	mV
Current, Unipolar			±1	μA
Monotonicity, Temperature Range (14 bits)	0		+50	°C
DRIFT (Over specified temp range)				
Total Error over Temperature Range[4]				
Voltage, Unipolar			±0 063	% of FSR
Current, Unipolar			±0 23	% of FSR
Gain Voltage			±20	ppm/°C
Current			±60	ppm/°C
Offset Voltage, Unipolar		±1	±2	ppm of FSR/°C
Current, Unipolar			±1	ppm of FSR/°C
Differential Linearity over Temperature			±2	ppm of FSR/°C
Linearity Error over Temperature			±2	ppm of FSR/°C
SETTLING TIME				
Voltage Model (to ±0 005% of FSR)				
Output 20V Step		5	10	μs
1LSB Step[5]		3	5	μs
Slew Rate		20		V/μs
Current Model (to ±0.005% of FSR)				
Output 2mA step, 10Ω to 100Ω Load			1	μs
1kΩ Load			3	μs
Switching Transient		500		mV
OUTPUT				
ANALOG OUTPUT				
Voltage Model				
Range		0 to +10		V
Output Current	±5			mA
Output Impedance (DC)		0 05		Ω
Short-Circuit Duration		Indefinite to Common		
Current Model				
Range		0 to −1 25		mA
Output Impedance, Unipolar		15		kΩ
Compliance		±2.5		V
INTERNAL REFERENCE VOLTAGE	6 0	6 3	6 6	V
Maximum External Current[6]			±200	μA
Temperature Coefficient of Drift			±10	ppm/°C
POWER SUPPLY SENSITIVITY				
Unipolar Offset ±15VDC		±0 001		% of FSR/%V_S
+15VDC		±0 001		% of FSR/%V_S
Gain ±15VDC		±0 001		% of FSR/%V_S
+5VDC		±0 0005		% of FSR/%V_S
POWER SUPPLY REQUIREMENTS				
Voltage	±14 5, +4.75	±15, +5	±15 5, +5.25	VDC
Supply Drain ±15VDC (no load)		±25	±35	mA
+5VDC (logic supply)		±20	±35	mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating (double above Drift Specs)	−25		+85	°C
Storage	−55		+100	°C

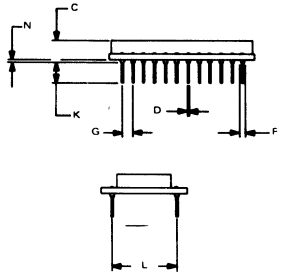
*NOTES (1) Adding external CMOS hex buffers CD4009A will provide 15VDC CMOS input compatibility. The percent change in output ΔV_O as logic 0 varies from 0 0V to +0 4V and logic 1 changes from +2 4V to +5 0V on all inputs is less than 0 006% of FSR (2) FSR means Full Scale Range and is 20V for ±10V range, 10V for ±5V range, etc (3) Adjustable to zero with external trim potentiometer (4) With gain and offset errors adjusted to zero at 25°C (5) LSB is for 14-bit resolution (6) Maximum with no degradation of specifications

MECHANICAL

NOTE Leads in true position within 0.10" (0.25mm) R at MMC at seating plane



Pin numbers shown for reference only
Numbers may not be marked on package



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 310	1 360	33 27	34 54
B	770	810	19 56	20 57
C	150	210	3 81	5 33
D	018	021	0 46	0 53
F	035	050	0 89	1 27
G	100 BASIC		2 54 BASIC	
H	110	130	2 79	3 30
K	150	250	3 81	6 35
L	600 BASIC		15 24 BASIC	
N	002	010	0 05	0 25
R	0 85	105	2 16	2 67

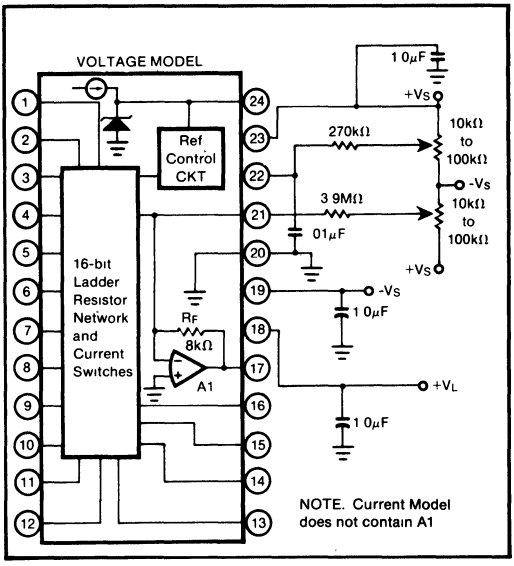
CASE. Ceramic

MATING CONNECTOR: 245MC

WEIGHT. 8·4 grams (0 3 oz)

HERMETICITY: Conforms to method 1014, condition C, step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

CONNECTION DIAGRAM



PIN ASSIGNMENTS

I Model	Pin	V Model
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
Bit 12	12	Bit 12
Bit 13	13	Bit 13
Bit 14	14	Bit 14
Bit 15	15	Bit 15
(LSB) Bit 16	16	Bit 16 (LSB)
RF	17	VOUT
+5VDC	18	+5VDC
-15VDC	19	-15VDC
COMMON	20	COMMON
IOUT	21	SUMMING JUNCTION
GAIN ADJUST	22	GAIN ADJUST
+15VDC	23	+15VDC
6 3V REF OUT	24	6 3V REF OUT

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC71 accepts comlementary digital input codes in decimal (CCD) format (see Table I).

TABLE I. Digital Input Codes.

	DIGITAL INPUT CODES		
CCD MODELS		CCD Complementary Coded Decimal 4 Digits	*Invert the MSB of the COB code with an external inverter to obtain CTC code
	F S bits ON 0110 0110 All Bits OFF 1111 1111	+Full Scale Zero	

ACCURACY

Linearity

This specification describes one of the truest measures of D/A converter accuracy. As defined it means that the analog output will not vary by more than ±0.005% max (CCD) from a straight line drawn through the end points (all bits ON and all bits OFF) at +25°C.

Differential Linearity

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can be anywhere from 1/2LSB to 3/2LSB when the input changes from one adjacent input stage to the next.

Monotonicity

Monotonicity over 0°C to +50°C is guaranteed. This insures that the analog output will increase or remain the same for increasing 14-bit input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (see Figure 1). Gain Drift is established by:

1. testing the end point differences for each DAC71 model at +25°C and the appropriate specification temperature extremes;

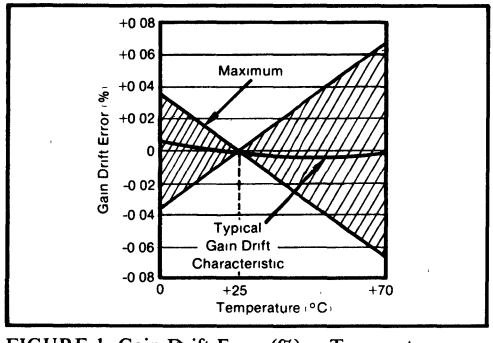


FIGURE 1. Gain Drift Error (%) vs Temperature.

2. calculating the gain error with respect to the +25°C value; and
3. dividing by the temperature change. This is expressed in ppm/°C.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range.

The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 2).

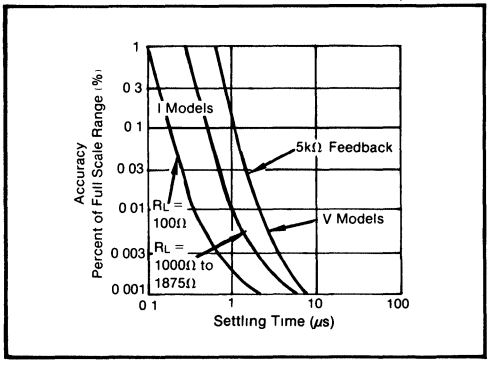


FIGURE 2. Full Scale Range Settling Time vs Accuracy.

Voltage Output Models

Settling times are specified to ±0.005% of FSR; one for maximum full scale range changes of 20V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111 . . . 11 to 1000 . . . 00), the point at which the worst-case settling time occurs.

Current Output Models

Two settling times are specified to ±0.005% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the output of the current models while maintaining specified accuracy. The typical compliance voltage of all current output models is +2.5V and maximum safe voltage swing permitted without damage is +5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 3).

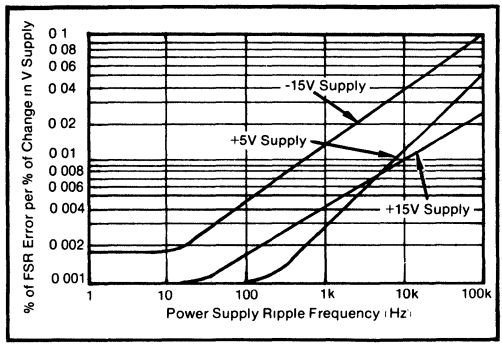


FIGURE 3. Power Supply Rejection vs Power Supply Ripple Frequency.

REFERENCE SUPPLY

All DAC71 models are supplied with an internal +6.3V reference voltage supply. This reference voltage (pin 24) has a tolerance of ±5% and is connected internally for specified operation. The zener is selected for a Gain Drift of typically ±3ppm/°C and is burned-in for a total of 168 hours for guaranteed reliability. This reference may also be used externally but the current drain is limited to 200μA. An external buffer amplifier is recommended if the DAC71 internal reference is used externally in order to provide a constant load to the reference supply output.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the DAC71. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (20% carbon or better) should be located close to the DAC71 to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted in place of the 3.9MΩ. A 0.001μF to 0.01μF ceramic

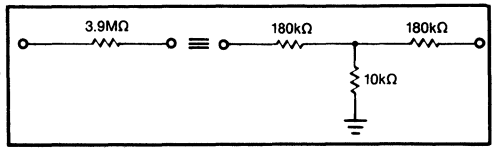


FIGURE 4. Equivalent Resistances.

capacitor should be connected from Gain Adjust (pin 22) to common to prevent noise pickup. Refer to Figure 5 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters.

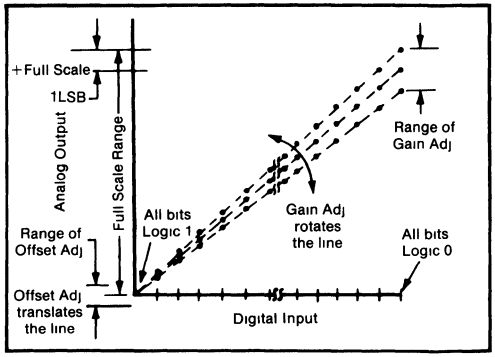


FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

Offset Adjustment

For unipolar configurations, apply the digital input code that should produce zero potential output and adjust the offset potentiometer for zero output.

See Table II for corresponding codes and the Connection Diagram for offset adjustment connections. Offset adjust should be made prior to gain adjust.

TABLE II. Digital Input and Analog Output Relationships.

DIGITAL INPUT CODE	OUTPUT CODE			
	VOLTAGE		CURRENT	
	16-Bit Resolution	14-Bit Resolution	16-Bit Resolution	14-Bit Resolution
Complementary Binary Coded Decimal CCD	4-Digit Resolution	N A	4-Digit Resolution	N A
0 to -10V or 0 to -1 25mA				
One LSB	-1 0mV		0 125μA	
Full Scale 0110 0110	-9 999V		-1 24987mA	
All Bits OFF 1111 1111	Zero		Zero	

Gain Adjustment

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagram for gain adjustment connections.

INSTALLATION CONSIDERATIONS

Figure 6 shows the connection diagram for a voltage output DAC71. Lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L) is constant. R_2 simply introduces a gain error that can be removed during initial calibration. R_3 is part of R_L if the output voltage is sensed at Common (pin 20) and therefore introduces no error. If R_L is variable then R_2 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is $5k\Omega$, then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the DAC71 for optimum performance.

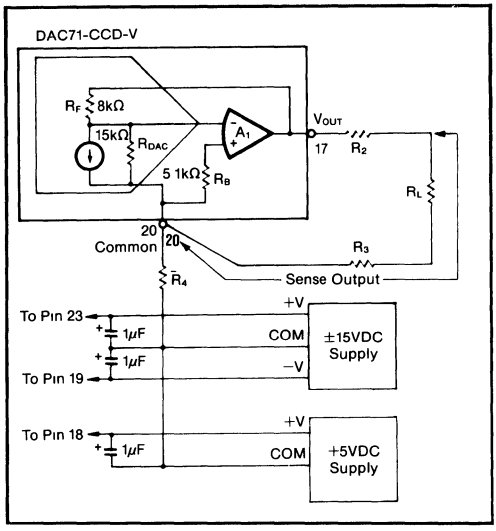


FIGURE 6. Output Circuit for Voltage Models.

Figures 7 and 8 show two methods of connecting current model DAC71s with the external precision output op amps. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A_1 at R_1) the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated during initial calibration. The effect of R_2 is negligible because it is inside the feedback loop of the

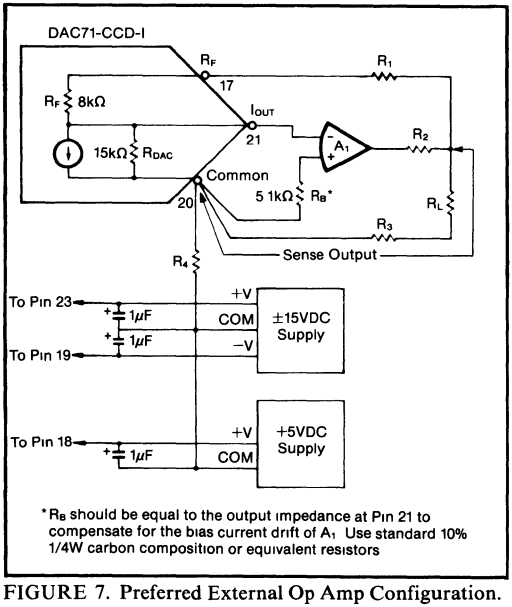


FIGURE 7. Preferred External Op Amp Configuration.

output op amp and is therefore greatly reduced by the loop gain. If the output cannot be sensed at Common (pin 20), then the differental output circuit shown in Figure 8 is recommended. In this circuit the output voltage is sensed at the load common and not at the DAC common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_1. Note that if R_3 is negligible, the circuit of Figure 8 can be reduced to the one shown in Figure 8 because $R_8 = (R_7 + R_5) \parallel R_6$. In all three circuits the effect of R_4 is negligible.

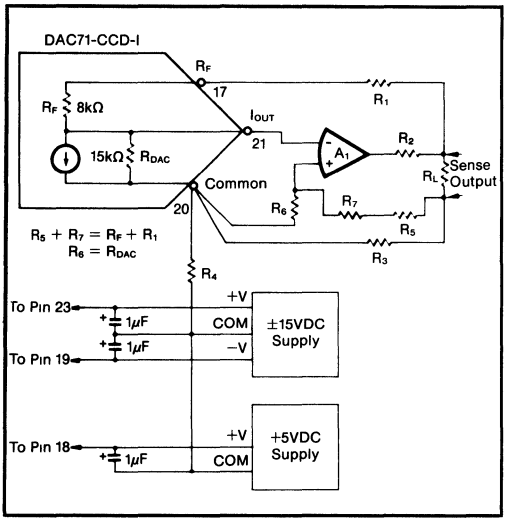


FIGURE 8. Differential Sensing Output Op Amp Configuration.

The DAC71 and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area. Therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

NOTE: It is recommended that the digital input lines of the DAC71 be driven from inverters or buffers of TTL input registers to obtain specified accuracy.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT DAC

The DAC71-CCD-I is a current output device and will drive the summing junction of an op amp to produce an output voltage (see Figure 9). The op amp output voltage is:

$$V_{OUT} = -I_{OUT} R_F$$

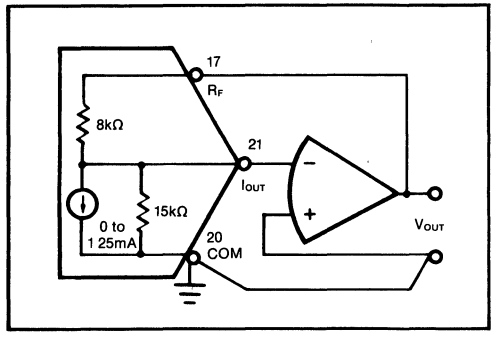


FIGURE 9. External Op Amp Using Internal Feedback Resistors.

where I_{OUT} is the DAC71 output current and R_F is the feedback resistor. Use of the internal feedback resistor (pin 17) is required to obtain specified gain accuracy and low gain drift.

The DAC71 can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±25ppm/°C. The resistors in the DAC71 are chosen for ratio tracking of ±1ppm/°C and not absolute TCR (which may be as high at ±25ppm/°C).

An alternative method of scaling the output voltage of the DAC71 and preserving the low gain drift is shown in Figure 10.

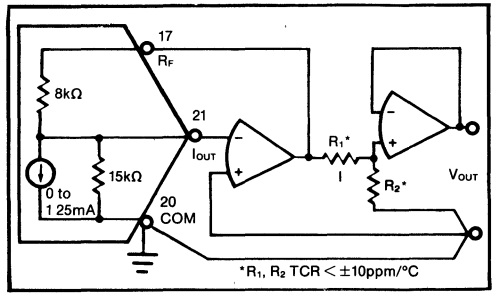
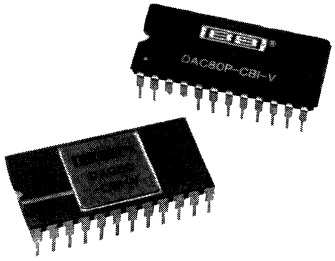


FIGURE 10. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift.

BURR-BROWN®



DAC80
DAC80P

AVAILABLE IN DIE FORM

Monolithic 12-Bit DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- INDUSTRY STANDARD PINOUT
- LOW POWER DISSIPATION: 345mW
- FULL ±10V SWING WITH V_{CC} = ±12VDC
- DIGITAL INPUTS ARE TTL- AND CMOS-COMPATIBLE
- GUARANTEED SPECIFICATIONS WITH ±12V AND ±15V SUPPLIES
- SINGLE-CHIP DESIGN
- ±1/2LSB MAXIMUM NONLINEARITY, 0°C to +70°C
- GUARANTEED MONOTONICITY, 0°C to +70°C
- TWO PACKAGE OPTIONS: Hermetic side-brazed ceramic and low-cost molded plastic
- SETTLING TIME: 4μs max to ±0.01% of Full Scale

DESCRIPTION

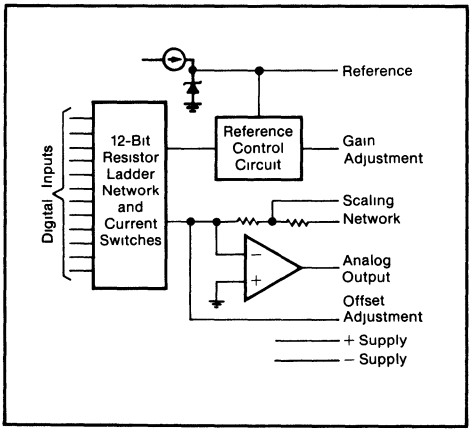
This monolithic digital-to-analog converter is pin-for-pin equivalent to the industry standard DAC80, first introduced by Burr-Brown. Its single-chip design includes the output amplifier and provides a highly stable reference capable of supplying up to 2.5mA to an external load without degradation of D/A performance.

This converter uses proven circuit techniques to provide accurate and reliable performance over temperature and power supply variations. The use of a buried zener diode as the basis for the internal reference contributes to the high stability and low noise of the device. Advanced methods of laser trimming result in precision output current and output amplifier feedback resistors, as well as low integral and differential linearity errors. Innovative circuit design enables the DAC80 to operate at supply voltages as low as ±11.4V with no loss in performance or accuracy over any range of output voltage. The lower power dissipation of this 118-mil by 121-mil chip results in higher reliability and greater long term stability.

Burr-Brown has further enhanced the reliability of the monolithic DAC80 by offering a hermetic, side-brazed, ceramic package. In addition, ease of use has been enhanced by eliminating the need for a +5V logic power supply.

For applications requiring both reliability and low cost, the DAC80P in a molded plastic package offers the same electrical performance over temperature as the ceramic model. The DAC80P is available with either voltage or current output.

For designs that require a wider temperature range, see Burr-Brown models DAC85H and DAC87H. For designs that require complementary coded decimal inputs, see Burr-Brown model DAC80-CCD-V (-I).



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable. BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

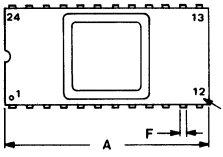
Typical at +25°C and $\pm V_{CC}$ = 12V or 15V unless otherwise noted

MODEL	DAC80			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUT				
Resolution			12	Bits
Logic Levels (0°C to +70°C)[1]				
V_{IH} (Logic "1")	+2		+16 5	VDC
V_{IL} (Logic "0")	0		+0.8	VDC
I_{IH} (V_{IN} = +2 4V)			+20	μA
I_{IL} (V_{IN} = +0.4V)			−180	μA
ACCURACY (at +25°C)				
Linearity Error		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	±3/4	LSB
Gain Error[2]		±0 1	±0 3	%
Offset Error[2]		±0 05	±0 15	% of FSR[3]
DRIFT (0°C to +70°C)[4]				
Total bipolar drift (includes gain, offset, and linearity drifts)		±10	±25	ppm of FSR/°C
Total Error Over 0°C to +70°C[5]				
Unipolar		±0 06	±0.15	% of FSR
Bipolar		±0 06	±0 12	% of FSR
Gain Including Internal Reference		±10	±30	ppm/°C
Excluding Internal Reference		±5	±10	ppm/°C
Unipolar Offset		±1	±3	ppm of FSR/°C
Bipolar Offset		±7	±15	ppm of FSR/°C
Differential Linearity 0°C to +70°C		±1/2	±3/4	LSB
Linearity Error 0°C to +70°C		±1/4	±1/2	LSB
Monotonicity Guaranteed	0		+70	°C
CONVERSION SPEED, V_{OUT} models				
Settling Time to ±0 01% of FSR				
For FSR change (2kΩ ‖ 500pF load)				
with 10kΩ Feedback		3	4	μs
with 5kΩ Feedback		2	3	μs
For 1LSB Change		1		μs
Slew Rate	10			V/μs
CONVERSION SPEED, I_{OUT} models				
Settling Time to ±0 01% of FSR				
For FSR change. 10Ω to 100Ω load		300		ns
1kΩ load		1		μs
ANALOG OUTPUT, V_{OUT} models				
Ranges		±2 5, ±5, ±10, +5, +10		V
Output Current[6]	±5			mA
Output Impedance (DC)		0 05		Ω
Short Circuit to Common, Duration[7]		Indefinite		
ANALOG OUTPUT, I_{OUT} models				
Ranges. Bipolar	±0.96	±1 0	±1 04	mA
Unipolar	−1.96	−2 0	−2 04	mA
Output Impedance Bipolar	2.6	3.2	3 7	kΩ
Unipolar	4 6	6 6	8 6	kΩ
Compliance	−2 5		+2 5	V
REFERENCE VOLTAGE OUTPUT	+6.23	+6 30	+6 37	V
External Current (constant load)			2 5	mA
Drift vs Temperature		±10	±20	ppm/°C
Output Impedance		1		Ω
POWER SUPPLY SENSITIVITY				
V_{CC} = ±12VDC or ±15VDC		±0 002	±0.006	% FSR/ % V_{CC}
POWER SUPPLY REQUIREMENTS				
$\pm V_{CC}$	±11.4		±16 5	VDC
Supply Drain (no load). $+V_{CC}$		8	12	mA
$-V_{CC}$		15	20	mA
Power Dissipation (V_{CC} = ±15VDC)		345	480	mW
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating	−25		+85	°C
Storage. Plastic DIP	−60		+100	°C
Ceramic DIP	−65		+150	°C

NOTES (1) Refer to "Logic Input Compatibility" section (2) Adjustable to zero with external trim potentiometer. (3) FSR means full scale range and is 20V for ±10V range, 10V for ±5V range for V_{OUT} models; 2mA for I_{OUT} models (4) To maintain drift spec, internal feedback resistors must be used (5) Includes the effects of gain, offset and linearity drift Gain and offset errors externally adjusted to zero at +25°C. (6) For $\pm V_{CC}$ less than ±12VDC, limit output current load to ±2.5mA to maintain ±10V full scale output voltage swing For output range of ±5V or less, the output current is ±5mA over entire $\pm V_{CC}$ range (7) Short circuit current is 40mA, max

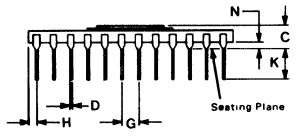
MECHANICAL

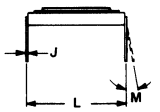
Hermetic Ceramic 24-Lead DIP



NOTE
Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers may not be marked on package





PIN Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3 2)

HERMETICITY Conforms to Method 1014, Condition A1 or A2 (fine leak) and Condition C (gross leak). Metal lid of package is connected to $-V_{CC}$ internally

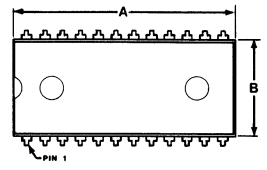
CASE Ceramic

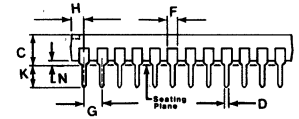
MATING CONNECTOR 0245MC

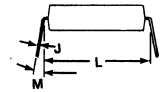
WEIGHT 4 1 grams (0 15 oz)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 185	1 215	30 10	30 86
C	105	170	2 67	4 32
D	015	021	0 38	0 53
F	035	060	0 89	1 52
G	100 BASIC		2 54 BASIC	
H	030	070	0 76	1 78
J	008	012	0 20	0 30
K	120	240	3 05	6 10
L	600 BASIC		15 24 BASIC	
M	–	10°		10°
N	025	060	0 64	1 52

Molded Plastic 24-Lead DIP







NOTE
Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

PIN Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3 2)

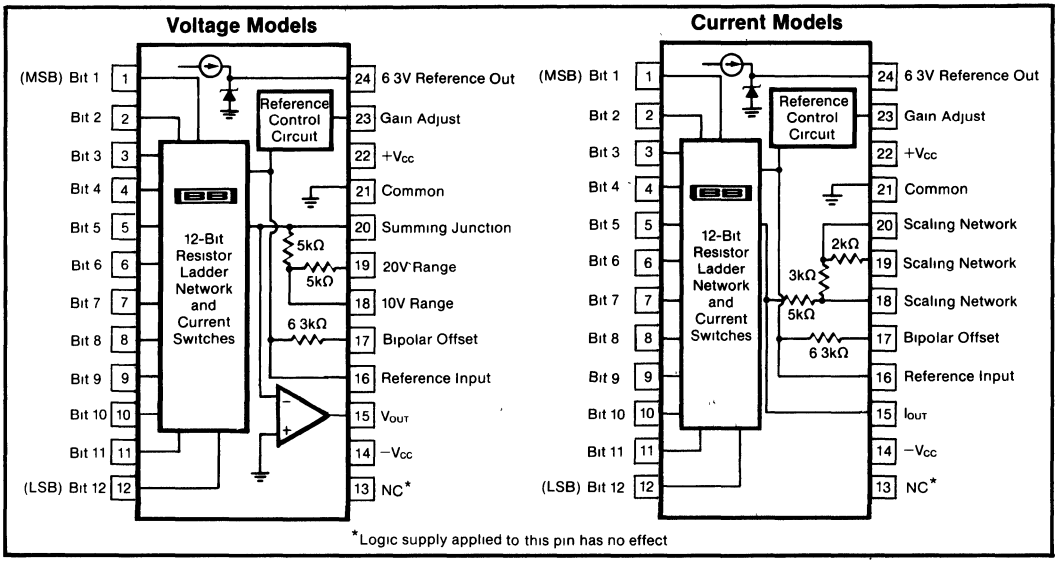
CASE Plastic

MATING CONNECTOR 0245MC

WEIGHT 3 7 grams (0 13 oz)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.238	1.263	31.32	32.58
B	.598	.675	13.67	14.61
C	.166	.224	4.20	5.70
D	.016	.023	0.36	0.58
F	.048	.062	1.09	1.57
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.132	2.54	3.35
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.022	0 46	0.56

FUNCTIONAL DIAGRAM AND PIN ASSIGNMENTS



*Logic supply applied to this pin has no effect

BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information table. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

ABSOLUTE MAXIMUM RATINGS

+Vcc to Common	0V to +18V
−Vcc to Common	0V to −18V
Digital Data Inputs to Common	−1V to +18V
Reference Output to Common	±Vcc
Reference Input to Common	±Vcc
Bipolar Offset to Common	±Vcc
10V Range R to Common	±Vcc
20V Range R to Common	±Vcc
External Voltage to DAC Output	−5V to +5V
Lead Temperature, Soldering	+300°C, 10s
Max Junction Temperature	165°C
Thermal Resistance, θ_{JA}: Plastic DIP	100°C/W
Ceramic DIP	65°C/W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Model	Package	Output
DAC80-CBI-I	Ceramic DIP	Current
DAC80Z-CBI-I	Ceramic DIP	Current
DAC80-CBI-V	Ceramic DIP	Voltage
DAC80Z-CBI-V	Ceramic DIP	Voltage
DAC80P-CBI-I	Plastic DIP	Current
DAC80P-CBI-V	Plastic DIP	Voltage
BURN-IN SCREENING OPTION		
Model	**Package**	**Burn-In Temp. (160h)(1)**
DAC80-CBI-V-BI	Ceramic DIP	+125°C
DAC80P-CBI-V-BI	Plastic DIP	+85°C

NOTE (1) Or equivalent combination See text

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC80 accepts complementary binary digital input codes. The CBI model may be connected by the user for any one of three complementary codes: CSB, COB, or CTC (see Table I).

TABLE I. Digital Input Codes.

DIGITAL INPUT	ANALOG OUTPUT		
MSB LSB ↓ ↓	CSB Compl Straight Binary	COB Compl. Offset Binary	CTC* Compl Two's Compl
000000000000	+Full Scale	+Full Scale	-1LSB
011111111111	+1/2 Full Scale	Zero	-Full Scale
100000000000	1/2 Full Scale -1LSB	-1LSB	-Full Scale
111111111111	Zero	-Full Scale	Zero

* Invert the MSB of the COB code with an external inverter to obtain CTC code.

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC80 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0°C to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a 0°C to +70°C range is guaranteed in the DAC80 to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each DAC80 model at 0°C, +25°C and +70°C; 2) calculating the gain error with respect to the 25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications both with and without internal reference.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, +25°C and +70°C. The maximum change in Offset is referenced to the Offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC80 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

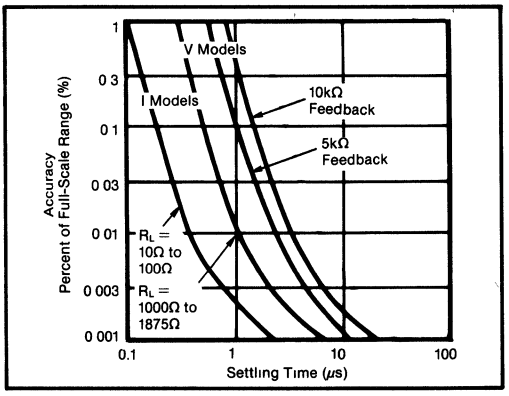


FIGURE 1. Full Scale Range Settling Time vs Accuracy.

Voltage Output Models

Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

Current Output Models

Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω to 1875Ω. Internal resistors are provided for connecting nominal load resistances of approximately 1000Ω to 1800Ω for output voltage range of ±1V and 0 to −2V (see Figures 11 and 12).

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is ±2.5V. Maximum safe voltage range of ±1V and 0 to −2V. (See Figures 11 and 12).

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages (see Figure 2).

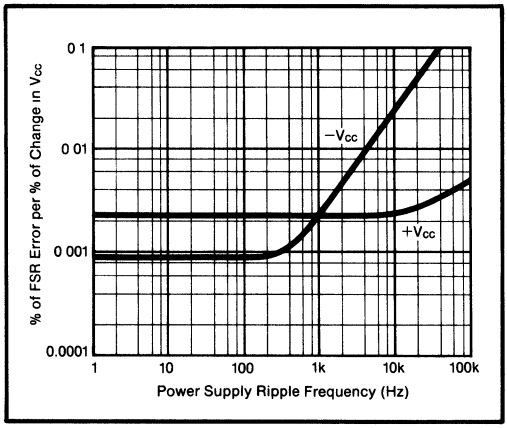


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

REFERENCE SUPPLY

All DAC80 models are supplied with an internal 6.3V reference voltage supply. This voltage (pin 24) has a tolerance of ±1% and must be connected to the Reference Input (pin 16) for specified operation. This reference may be used externally also, but external current drain is limited to 2.5mA.

If a varying load is to be driven, an external buffer amplifier is recommended to drive the load in order to isolate bipolar offset from load variations. Gain and bipolar offset adjustments should be made under constant load conditions.

LOGIC INPUT COMPATIBILITY

DAC80 digital inputs are TTL, LSTTL and 4000B, 54/74HC CMOS compatible. The input switching threshold remains at the TTL threshold over the entire supply range.

Logic "0" input current over temperature is low enough to permit driving DAC80 directly from outputs of 4000B and 54/74C CMOS devices.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Connect power supply voltages as shown in Figure 3. For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown. These capacitors (1μF tantalum) should be located close to the DAC80.

±12V OPERATION

All DAC80 models can operate over the entire power supply range of ±11.4V to ±16.5V. Even with supply levels dropping to ±11.4V, the DAC80 can swing a full ±10V range, provided the load current is limited to ±2.5mA. With power supplies greater than ±12V, the DAC80 output can be loaded up to ±5mA. For output swing of ±5V or less, the output current is ±5mA, min. over the entire V_{CC} range.

No bleed resistor is needed from $+V_{CC}$ to pin 24, as was needed with prior hybrid Z versions of DAC80. Existing ±12V applications that are being converted to the monolithic DAC80 must omit the resistor to pin 24 to insure proper operation.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 3 and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the DAC80 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted.

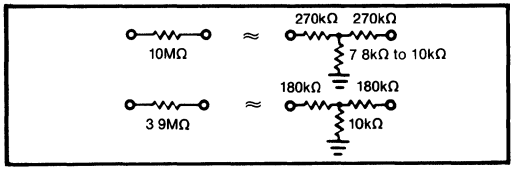


FIGURE 4. Equivalent Resistances.

Existing applications that are converting to the monolithic DAC80 must change the gain trim resistor on pin 23 from 33MΩ to 10MΩ to insure sufficient adjustment range. Pin 23 is a high impedance point and a 0.001μ1F to 0.01μF ceramic capacitor should be connected from this pin to Common (pin 21) to prevent noise pickup. Refer to Figure 5 for relationship of Offset and Gain adjustments to unipolar and bipolar D/A operation.

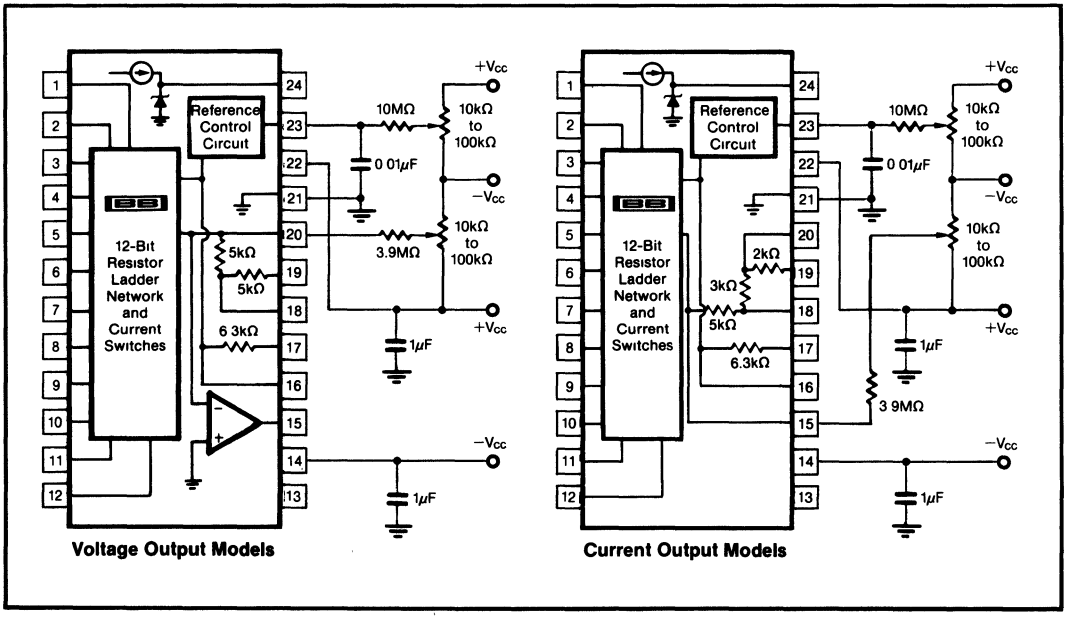


FIGURE 3. Power Supply and External Adjustment Connection Diagrams

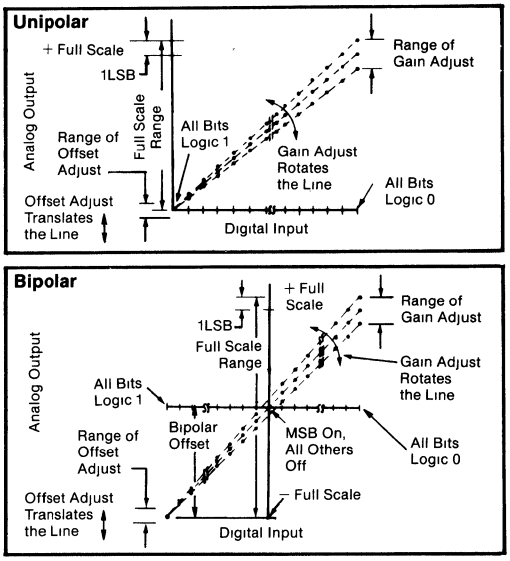


FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar and Bipolar D/A Converter.

Offset Adjustment

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is −10V. See Table II for corresponding codes.

TABLE II. Digital Input/Analog Output.

DIGITAL INPUT	ANALOG OUTPUT			
	VOLTAGE *		CURRENT	
MSB LSB	0 to +10V	±10V	0 to -2mA	±1mA
000000000000	+9 9976V	+9 9951V	-1 9995mA	-0 9995mA
011111111111	+5 0000V	0 0000V	-1 0000mA	0 0000mA
100000000000	+4 9976V	-0 0049V	-0 9995mA	+0 0005mA
111111111111	0 0000V	-10 0000V	0 0000mA	+1 000mA
One LSB	2 44mV	4 88mV	0 488μA	0.488μA

*To obtain values for other binary ranges
0 to +5V range divide 0 to +10V range values by 2
±5V range divide ±10V range values by 2
±2 5V range divide ±10V range values by 4

Gain Adjustment

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output. Adjust the Gain potentiometer for this positive full scale output. See Table II for positive full scale voltages and currents.

VOLTAGE OUTPUT MODELS

Output Range Connections

Internal scaling resistors provided in the DAC80 may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. See Figure 6.

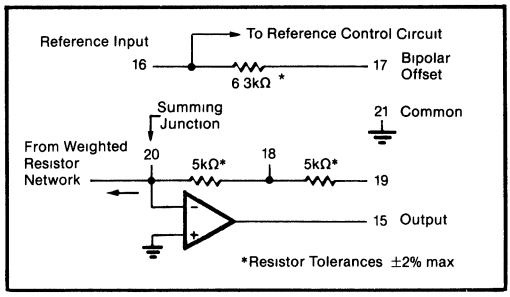


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

Gain and offset drift are minimized because of the thermal tracking of the scaling resistors with other internal device components. Connections for various output voltage ranges are shown in Table III. Settling time for a full-scale range change is specified as 4μs for the 20V range and 3μs for the 10V range.

TABLE III. Output Voltage Range Connections for Voltage Models.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	NC	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

CURRENT OUTPUT MODELS

The resistive scaling network and equivalent output circuit of the current model differ from the voltage model and are shown in Figures 7 and 8.

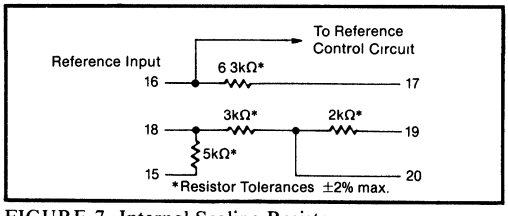


FIGURE 7. Internal Scaling Resistors.

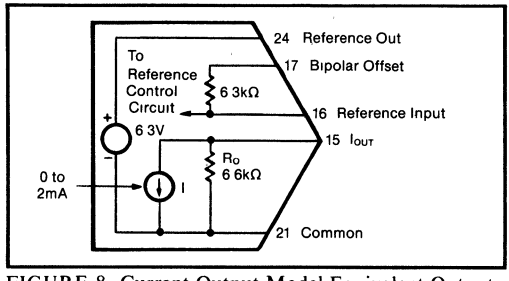


FIGURE 8. Current Output Model Equivalent Output Circuit.

Internal scaling resistors (Figure 7) are provided to scale an external op amp or to configure load resistors for a voltage output. These connections are described in the following sections.

If the internal resistors are not used for voltage scaling, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift.

Driving An External Op Amp

The current output model DAC80 will drive the summing junction of an op amp used as a current-to-voltage converter to produce an output voltage. See Figure 9.

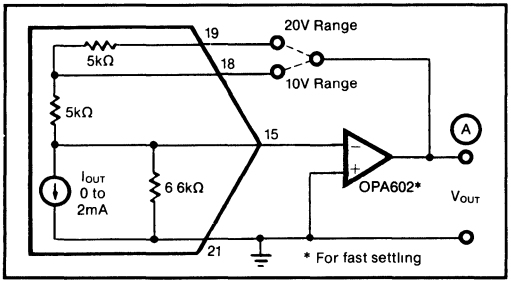


FIGURE 9. External Op-Amp—Using Internal Feedback Resistors.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current output model DAC80 provides output voltage ranges the same as the voltage model DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table IV.

TABLE IV. Voltage Range of Current Output

Output Range	Digital Input Codes	Connect (A) to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	(A)	24
±5V	COB or CTC	18	15	NC	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	15	24

Output Larger Than 20V Range

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and −2mA for unipolar voltage ranges. See Figure 10. Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C plus R_F drift to total drift.

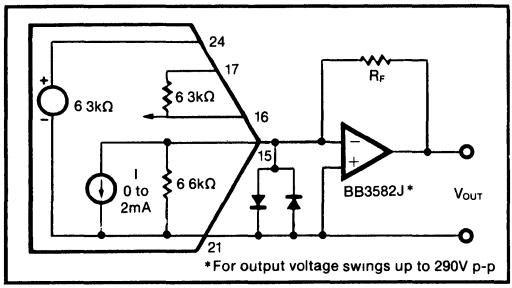


FIGURE 10. External Op-Amp—Using External Feedback Resistors.

Driving a Resistive Load Unipolar

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 11 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA\ [(R_L \times R_O) \div (R_L + R_O)]$$

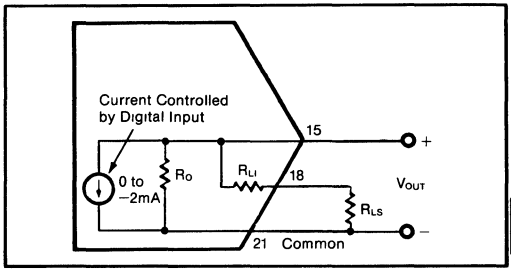


FIGURE 11. Current Output Model Equivalent Circuit Connected for Unipolar Voltage Output with Resistive Load.

The unipolar output impedance R_O equals 6.6kΩ (typ) and R_{LI} is the internal load resistance of 968Ω (derived by connecting pin 15 to pin 20 and pin 18 to 19). By choosing $R_{LS} = 210Ω$, $R_L = 1178Ω$. R_L in parallel with R_O yields 1kΩ total load. This gives an output range of 0 to −2V. Since R_O is not exact, initial trimming per Figure 3 may be necessary; also R_{LS} may be trimmed.

Driving a Resistive Load Bipolar

The equivalent output circuit for a bipolar output voltage range is shown in Figure 12, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA\ [(R_O \times R_L) \div (R_O + R_L)]$$

By connecting pin 17 to 15, the output current becomes bipolar (±1mA) and the output impedance R_O becomes 3.2kΩ (6.6kΩ in parallel with 6.3kΩ). R_{LI} is 1200Ω (derived by connecting pin 15 to 18 and pin 18 to 19). By choosing $R_{LS} = 255Ω$, $R_L = 1455Ω$. R_L in parallel with R_O yields 1kΩ total load. This gives an output range of ±1V. As indicated above, trimming may be necessary.

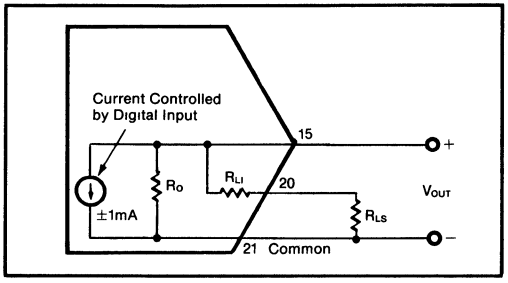
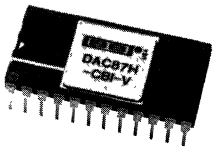


FIGURE 12. Current Output Model Connected for Bipolar Output Voltage with Resistive Load.

BURR-BROWN®



DAC85H
DAC87H

MILITARY VERSION AVAILABLE

Monolithic 12-Bit DIGITAL-TO-ANALOG CONVERTERS

FEATURES

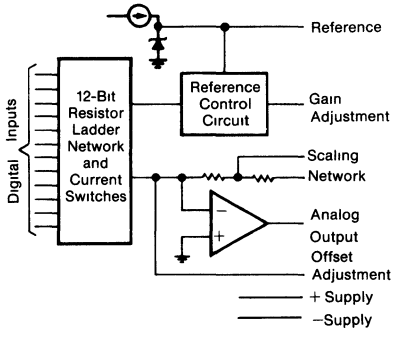
- INDUSTRY STANDARD PINOUT
- LOW POWER DISSIPATION: 345mW
- FULL ±10V SWING WITH V_{CC} = ±12VDC
- DIGITAL INPUTS ARE TTL- AND CMOS-COMPATIBLE
- GUARANTEED SPECIFICATIONS WITH ±12V AND ±15V SUPPLIES
- SINGLE-CHIP DESIGN
- ±1/2LSB MAXIMUM NONLINEARITY, −55°C to +125°C
- GUARANTEED MONOTONICITY, −55°C TO +125°C
- PACKAGE: Hermetic Side-brazed Ceramic DIP
- SETTLING TIME: 4μs max to ±0.01% of Full Scale

DESCRIPTION

These monolithic digital-to-analog converters are pin-for-pin equivalent to the industry standard DAC85 and DAC87 first introduced by Burr-Brown. Their single-chip design includes the output amplifier and provides a highly stable reference capable of supplying up to 2.5mA to an external load without degradation of D/A performance.

These converters use proven circuit techniques to provide accurate and reliable performance over temperature and power supply variations. The use of a buried zener diode as the bias for the internal reference contributes to the high stability and low noise of the device. Advanced methods of laser trimming result in precision output current and output amplifier feedback resistors, as well as low integral and differential linearity errors. Innovative circuit design enables the DAC85 and DAC87 to operate at supply voltages as low as ±11.4V with no loss in performance or accuracy over any range of output voltage. Ease of use has been enhanced by eliminating the need for a +5V logic power supply. The lower power dissipation of the 118 mil by 121 mil chip results in higher reliability and greater long term stability.

Both models are available in a hermetic, side-brazed, ceramic DIP. The DAC85H is specified over the industrial temperature range of −25°C to +85°C. The DAC87H is specified over the entire military temperature range of −55°C to +125°C.



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PDS-681A

SPECIFICATIONS

ELECTRICAL

Typical at +25°C and $\pm V_{CC}$ = 12V or 15V unless otherwise noted

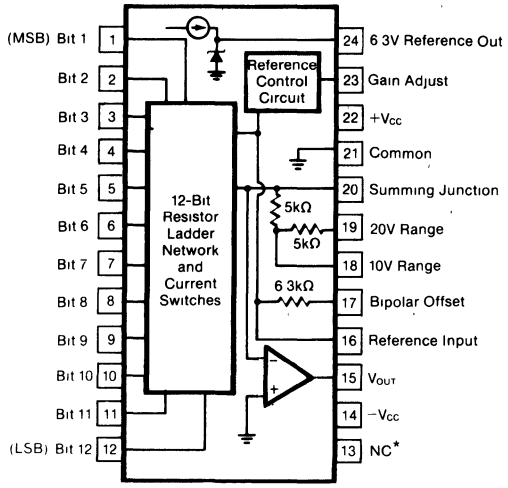
MODEL	DAC85H			DAC87H			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUT							
Resolution			12			*	Bits
Logic Levels (0°C to +70°C)[1]							
V_{IH} (Logic "1")	+2		+16 5	*		*	VDC
V_{IL} (Logic "0")	0		+0 8	*		*	VDC
I_{IH} (V_{IN} = +2 4V)			+20			*	µA
I_{IL} (V_{IN} = +0 4V)			−180			*	µA
ACCURACY (at 25°C)							
Linearity Error		±1/4	±1/2		*	*	LSB
Differential Linearity Error		±1/2	±3/4		*	*	LSB
Gain Error[2]		±0 1	±0 2			±0 1	%
Offset Error[2]		±0 5	±0 1			±0 05	% of FSR[3]
DRIFT (over specification temperature range)[4]							
Total bipolar drift (includes gain, offset, and linearity drifts)		±10	±25			±30	ppm of FSR/°C
Total Error (over specification temperature range[5] Unipolar			±0.2			*	% of FSR
Bipolar			±0 12			±0.2	% of FSR
Gain. Including Internal Reference			±20			*	ppm/°C
Excluding Internal Reference		±5	±10		*	*	ppm/°C
Unipolar Offset			±3			*	ppm of FSR/°C
Bipolar Offset			±10			*	ppm of FSR/°C
Differential Linearity			±3/4			*	LSB
Linearity Error		±1/4	±1/2		*	*	LSB
Monotonicity Guaranteed	−25		+85	−55		+125	°C
CONVERSION SPEED, V_{OUT} models							
Settling Time to ±0.012% of FSR							
For FSR change (2kΩ ‖ 500pF load):							
with 10kΩ Feedback		3	4		*	*	µs
with 5kΩ Feedback		2	3		*	*	µs
For 1LSB Change		1			*		µs
Slew Rate	10			*			V/µs
CONVERSION SPEED, I_{OUT} models							
Settling Time to ±0.01% of FSR							
For FSR change: 10Ω to 100Ω load		300			*		ns
1kΩ load		1			*		µs
ANALOG OUTPUT, V_{OUT} models							
Ranges		±2.5, ±5, ±10, +5, +10			*		V
Output Current[6]	±5			*			mA
Output Impedance (DC)		0.05			*		Ω
Short Circuit to Common, Duration[7]		Indefinite			*		
ANALOG OUTPUT, I_{OUT} models							
Ranges: Bipolar	±0.96	±1.0	±1.04	*	*	*	mA
Unipolar	−1.96	−2.0	−2.04	*	*	*	mA
Output Impedance. Bipolar	2.6	3.2	3.7	*	*	*	kΩ
Unipolar	4.6	6.6	8 6	*	*	*	kΩ
Compliance	−2.5		+2.5	*		*	V
REFERENCE VOLTAGE OUTPUT	+6.23	+6 30	+6.37	*	*	*	V
External Current (constant load)			2.5			*	mA
Drift vs Temperature			±20			±10	ppm/°C
Output Impedance		1			*		Ω
POWER SUPPLY SENSITIVITY							
V_{CC} = ±12VDC or ±15VDC		±0 002	±0.006		*	±0 004	% FSR/ % V_{CC}
POWER SUPPLY REQUIREMENTS							
$\pm V_{CC}$	±11 4		±16.5	*		*	VDC
Supply Drain (no load) $+V_{CC}$		8	12		*	*	mA
$-V_{CC}$		15	20		*	*	mA
Power Dissipation (V_{CC} = ±15VDC)		345	480		*	*	mW
TEMPERATURE RANGE							
Specification	−25		+85	−55		+125	°C
Storage	−65		+150	*		*	°C

*Specification same as DAC85H

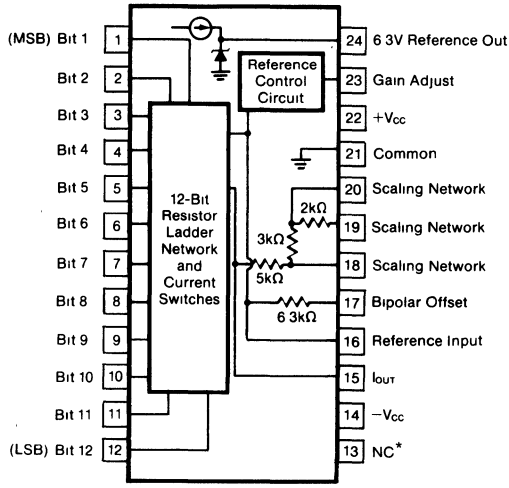
NOTES (1) Refer to "Logic Input Compatibility" section (2) Adjustable to zero with external trim potentiometer. (3) FSR means full scale range and is 20V for ±10V range, 10V for ±5V range for V_{OUT} models, 2mA for I_{OUT} models. (4) To maintain drift spec, internal feedback resistors must be used (5) Includes the effects of gain, offset and linearity drift Gain and offset errors externally adjusted to zero at +25°C (6) For $\pm V_{CC}$ less than ±12VDC, limit output current load to ±2 5mA to maintain ±10V full scale output voltage swing For output range of ±5V or less, the output current is ±5mA over entire $\pm V_{CC}$ range (7) Short circuit current is 40mA, max

FUNCTIONAL DIAGRAMS AND PIN ASSIGNMENTS

Voltage Models



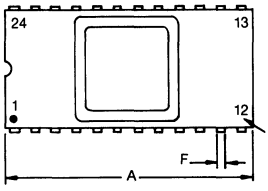
Current Models



*Logic supply applied to this pin has no effect

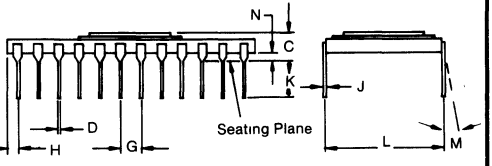
MECHANICAL

PACKAGE (Hermetic DIP)



NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane Pin numbers shown for reference only Numbers many not be marked on package Metal lid of package is connected to −Vcc internally

CASE Ceramic



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1 185	1 215	30 10	30 86
C	105	170	2 67	4 32
D	015	021	38	53
F	035	060	0 89	1 52
G	100 BASIC		2 54 BASIC	
H	030	070	0 76	1 78
J	008	012	0 20	0 30
K	120	240	3 05	6 10
L	600 BASIC		15 42 BASIC	
M	—	10°	—	10°
N	025	060	0 64	1 52

MATING CONNECTOR 0245MC

WEIGHT 4 1 grams (0 15 oz)

PIN Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3 2)

HERMETICITY Conforms to Method 1014, Condition A1 or A2 (fine leak) and Condition C (gross leak)

ABSOLUTE MAXIMUM RATINGS

+Vcc to Common	0V to +18V
−Vcc to Common	0V to −18V
Digital Data Inputs to Common	−1V to +18V
Reference Output to Common	±Vcc
Reference Input to Common	±Vcc
Bipolar Offset to Common	±Vcc
10V Range R to Common	±Vcc
20V Range R to Common	±Vcc
External Voltage to DAC Output	−5V to +5V
Max Junction Temperature	165°C
Lead Temperature, Soldering	+300°C, 10s
Thermal Resistance, θ_{JA}	65°C/W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Model	Output
DAC85H-CBI-I	Current
DAC85H-CBI-IBI[1]	Current
DAC85H-CBI-I/QM[2]	Current
DAC85H-CBI-V	Voltage
DAC85H-CBI-VBI	Voltage
DAC85H-CBI-V/QM	Voltage
DAC87H-CBI-V	Voltage
DAC87H-CBI-VBI	Voltage
DAC87H-CBI-V/QM	Voltage

NOTES (1) BI indicates burn-in screening option at +125°C for 160h or equivalent See text for details. (2) QM indicates environmental screening See text for details

ENVIRONMENTAL SCREENING

/QM Screening

Burr-Brown /QM models are environmentally-screened versions of our standard industrial products, designed to provide enhanced reliability. The screening, tabulated below, is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified below. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

Screening Flow For /QM Models

Screen	MIL-STD-883 Method	Condition	Comments
Internal Visual	2010	B	
High Temperature Storage (Stabilization Bake)	1008	C	+150°C, 24hrs
Temperature Cycling	1010	C	−65 to +150°C, 10 cycles
Burn-in	1015	B	+125°C, 160hrs
Constant Acceleration	2001	E	30,000 Gs
Hermeticity Fine Leak Gross Leak	 1014 1014	 A1 or A2 C	 5×10^{-8} atm cc/sec 60psig, 2hrs
External Visual	2009		

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC85H Series accepts complementary binary digital input codes. The CBI model may be connected by the user for any one of three complementary codes: CSB, COB, or CTC (see Table I).

TABLE I. Digital Input Codes.

Digital Input	Analog Output		
MSB ↓ LSB ↓	CSB Complementary Straight Binary	COB Complemen. Offset Binary	CTC* Complemen. Two's Complement
000000000000	+Full Scale	+Full Scale	−1LSB
011111111111	+1/2 Full Scale	Zero	−Full Scale
100000000000	1/2 Full Scale −1LSB	−1LSB	+Full Scale
111111111111	Zero	−Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC85H Series is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over the specification temperature range is guaranteed in the DAC85H Series to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each DAC85H Series model at minimum temperature, +25°C and maximum temperature; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications both with and without internal reference.

Offset drift is a measure of the actual change in output over the specification temperature range with all "1"s on the input. The offset is measured at +25°C, minimum temperature and maximum temperature. The maximum change in Offset is referenced to the Offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC85H Series model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

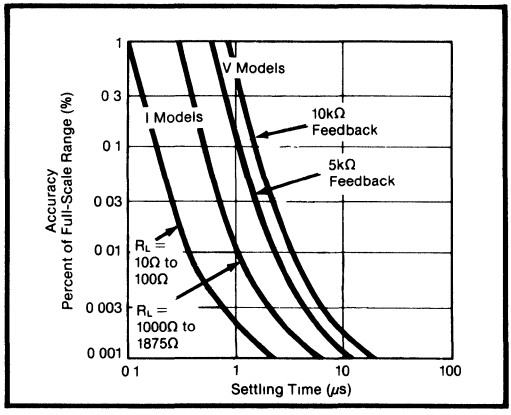


FIGURE 1. Full Scale Range Settling Time vs Accuracy.

Voltage Output Models

Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

Current Output Models

Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω to 1875Ω. Internal resistors are provided for connecting nominal load resistances of approximately 1000Ω to 1800Ω for output voltage range of ±1V and 0 to −2V. See Figure 11.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is ±2.5V. Maximum safe voltage swing permitted without damage to the DAC85H Series is ±5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages (see Figure 2).

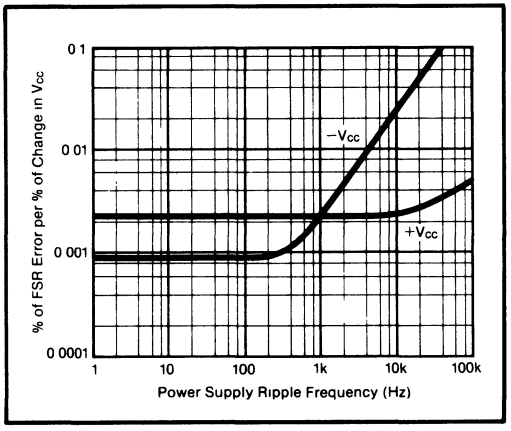


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

REFERENCE SUPPLY

All DAC85H Series models are supplied with an internal 6.3V reference voltage supply. This voltage (pin 24) has a tolerance of ±1% and must be connected to the Reference Input (pin 16) for specified operation. This reference may be used externally also, but external current drain is limited to 2.5mA.

If a varying load is to be driven, an external buffer amplifier is recommended to drive the load in order to isolate bipolar offset from load variations. Gain and bipolar offset adjustments should be made under constant load conditions.

LOGIC INPUT COMPATIBILITY

DAC85H Series digital inputs are TTL, LSTTL and 4000B, 54/74HC CMOS compatible. The input switching threshold remains at the TTL threshold over the entire supply range.

Logic "0" input current over temperature is low enough to permit driving DAC85H Series directly from outputs of 4000B and 54/74C CMOS devices.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Connect power supply voltages as shown in Figure 3. For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown. These capacitors (1μF tantalum) should be located close to the DAC85H Series.

±12V OPERATION

All DAC85H Series models can operate over the entire power supply range of ±11.4V to ±16.5V. Even with supply levels dropping to ±11.4V, the DAC can swing a full ±10V range, provided the load current is limited to ±2.5mA. With power supplies greater than ±12V, the DAC output can be loaded up to ±5mA. For output swing of ±5V or less, the output current is ±5mA, min. over the entire V_{CC} range.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 3 and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the DAC to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted.

Existing applications that are converting to the monolithic DAC85H Series must change the gain trim resistor on pin 23 from 18MΩ to 10MΩ to insure sufficient adjustment range. Pin 23 is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Common (pin 21) to prevent noise pickup. Refer to Figure 5 for relationship of Offset and Gain adjustments to unipolar and bipolar D/A operation.

Offset Adjustment

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

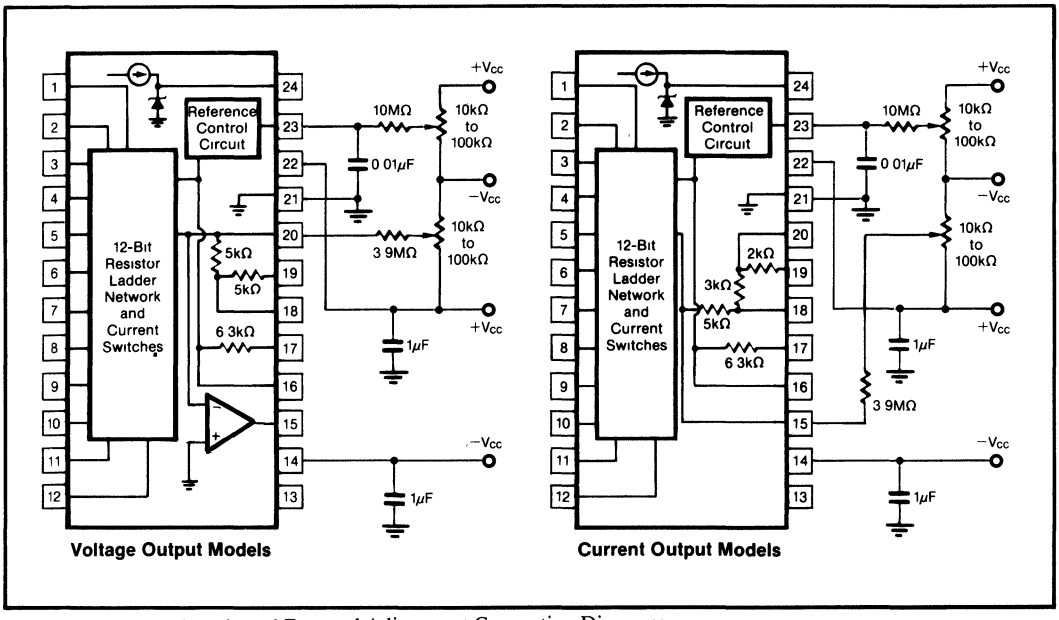


FIGURE 3. Power Supply and External Adjustment Connection Diagrams.

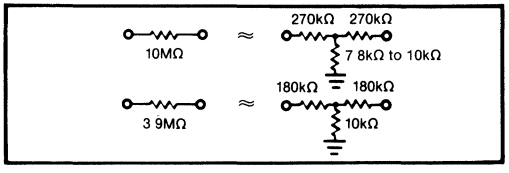


FIGURE 4. Equivalent Resistances.

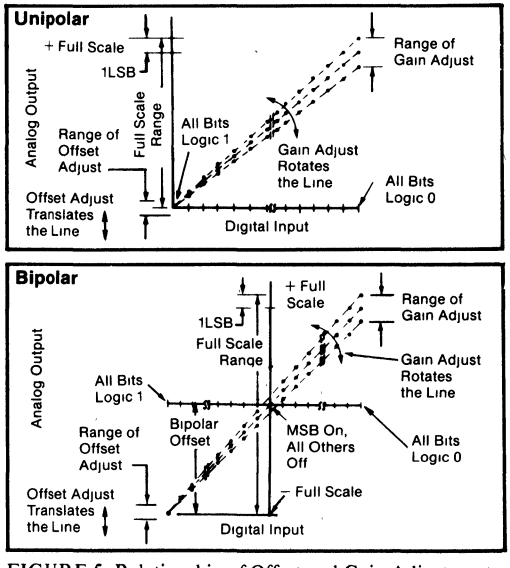


FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar and Bipolar D/A Converter.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is −10V. See Table II for corresponding codes.

Gain Adjustment

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output. Adjust the Gain potentiometer for this positive full scale output. See Table II for positive full scale voltages and currents.

TABLE II. Digital Input/Analog Output.

DIGITAL INPUT	ANALOG OUTPUT			
	VOLTAGE*		CURRENT	
MSB LSB	0 to +10V	±10V	0 to -2mA	±1mA
000000000000	+9 9976V	+9 9951V	-1 9995mA	-0 9995mA
011111111111	+5 0000V	0 0000V	-1 0000mA	0 0000mA
100000000000	+4 9976V	-0 0049V	-0 9995mA	+0 0005mA
111111111111	0 0000V	-10 0000V	0 0000mA	+1 000mA
One LSB	2 44mV	4 88mV	0 488μA	0.488μA

*To obtain values for other binary ranges
0 to +5V range divide 0 to +10V range values by 2
±5V range: divide ±10V range values by 2
±2 5V range divide ±10V range values by 4

VOLTAGE OUTPUT MODELS

Output Range Connections

Internal scaling resistors provided in the DAC85H Series may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. See Figure 6.

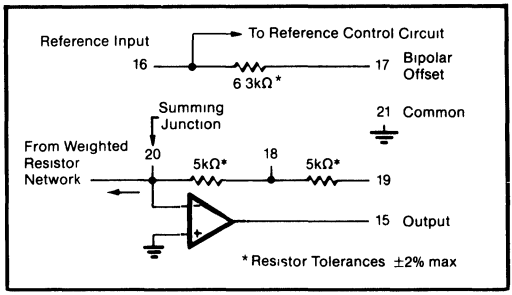


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

Gain and offset drift are minimized because of the thermal tracking of the scaling resistors with other internal device components. Connections for various output voltage ranges are shown in Table III. Settling time for a full-scale range change is specified as 4μs for the 20V range and 3μs for the 10V range.

TABLE III. Output Voltage Range Connections for Voltage Models.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	NC	24
±2 5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

CURRENT OUTPUT MODELS

The resistive scaling network and equivalent output circuit of the current model differ from the voltage model and are shown in Figures 7 and 8.

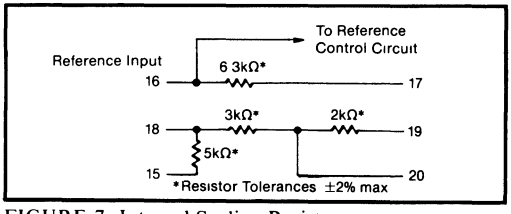


FIGURE 7. Internal Scaling Resistors.

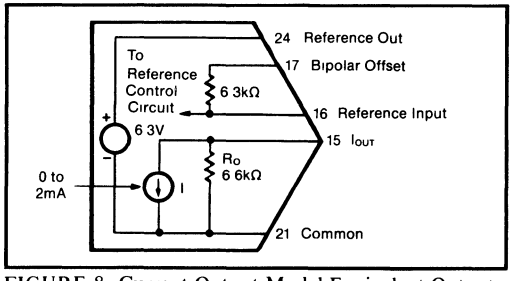


FIGURE 8. Current Output Model Equivalent Output Circuit.

Internal scaling resistors (Figure 7) are provided to scale an external op amp or to configure load resistors for a voltage output. These connections are described in the following sections.

If the internal resistors are not used for voltage scaling, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift.

Driving An External Op Amp

The current output model DAC85H will drive the summing junction of an op amp used as a current-to-voltage converter to produce an output voltage. See Figure 9.

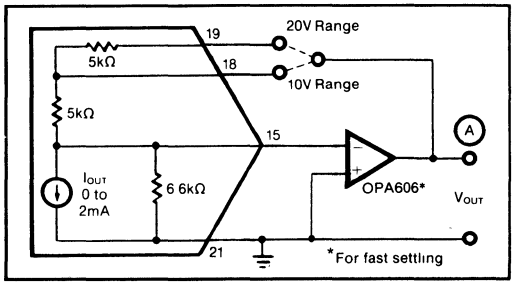


FIGURE 9. External Op Amp—Using Internal Feedback Resistors.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC85H output current and R_F is the feedback resistor. Using the internal feedback resistors of the current output model DAC85H provides output voltage ranges the same as the voltage model DAC85H. To obtain the desired output voltage range when connecting an external op amp, refer to Table IV.

TABLE IV. Voltage Range of Current Output

Output Range	Digital Input Codes	Connect (A) to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	(A)	24
±5V	COB or CTC	18	15	NC	24
±2 5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	15	24

Output Larger Than 20V Range

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and −2mA for unipolar voltage ranges. See Figure 10. Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C plus R_F drift to total drift.

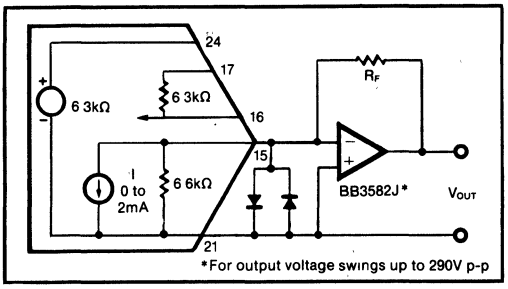


FIGURE 10. External Op Amp—Using External Feedback Resistors.

Driving a Resistive Load Unipolar

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 11 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA\ [(R_L \times R_O) \div (R_L + R_O)]$$

The unipolar output impedance R_O equals 6.6kΩ (typ) and R_{LI} is the internal load resistance of 968Ω (derived by connecting pin 15 to pin 20 and pin 18 to 19). By choosing $R_{LS} = 210\Omega$, $R_L = 1178\Omega$. R_L in parallel with R_O yields 1kΩ total load. This gives an output range of 0 to −2V. Since R_O is not exact, initial trimming per Figure 3 may be necessary; also R_{LS} may be trimmed.

BURN-IN SCREENING

Burn-in screening is an option available for the DAC85BH and DAC87BH. Burn-in duration is 160 hours at +125°C ambient temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "BI" to the base model number.

Driving a Resistive Load Bipolar

The equivalent output circuit for a bipolar output voltage range is similar to Figure 11, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA\ [(R_O \times R_L) \div (R_O + R_L)]$$

By connecting pin 17 to 15, the output current becomes bipolar (±1mA) and the output impedance R_O becomes 3.2kΩ (6.6kΩ || 6.3kΩ). R_{LI} is 1200Ω (derived by connecting pin 15 to 18 and pin 18 to 19). By choosing $R_{LS} =$ 255Ω (for a bipolar output connect R_{LS} between pin 20 and pin 21), $R_L = 1455\Omega$. R_L in parallel with R_O yields 1kΩ total load. This gives an output range of ±1V. As indicated above, trimming may be necessary.

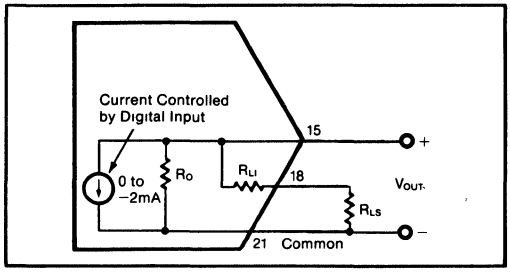


FIGURE 11. Current Output Model Equivalent Circuit Connected for Unipolar Voltage Output with Resistive Load.

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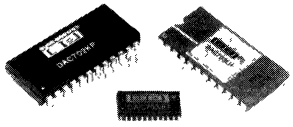


DAC700/702
DAC701/703

MILITARY VERSION AVAILABLE

Monolithic 16-Bit DIGITAL-TO-ANALOG CONVERTERS

FEATURES

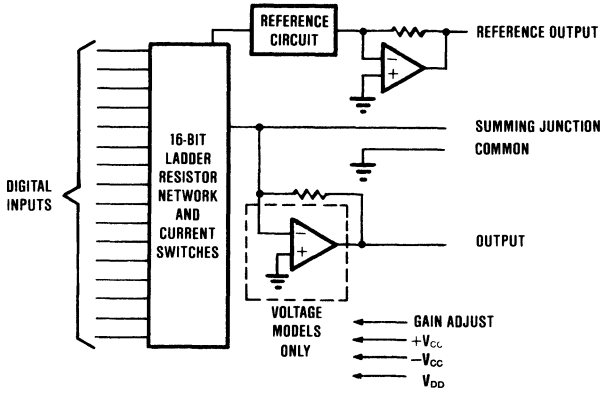
- MONOLITHIC CONSTRUCTION
- V_{OUT} AND I_{OUT} MODELS
- HIGH ACCURACY:
  Linearity Error ±0.0015% of FSR max
  Differential Linearity Error ±0.003% of FSR max
- MONOTONIC (at 15 bits) OVER FULL SPECIFICATION TEMPERATURE RANGE
- PIN-COMPATIBLE WITH DAC70, DAC71, DAC72
- LOW COST
- DUAL-IN-LINE PLASTIC AND HERMETIC CERAMIC
- /QM ENVIRONMENTAL SCREENING AVAILABLE
- BURN-IN PROGRAM AVAILABLE (-BI)

DESCRIPTION

This is another industry first from Burr-Brown—a complete 16-bit digital-to-analog converter that includes a precison buried-zener voltage reference and a low-noise, fast-settling output operational amplifier (voltage output models), all on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 15-bit monotonicity over the entire specified temperature range but also a maximum end-point linearity error of ±0.0015% of full-scale range. Total full-scale gain drift is limited to ±10ppm/°C maximum (LH and CH grades).

Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C- and 54/74HC-compatible over the entire temperature range. Outputs of 0 to +10V, ±10V, 0 to −2mA, and ±1mA are available.

These D/A converters are packaged in hermetic 24-pin ceramic side-brazed or molded plastic. The DIP-packaged parts are pin-compatible with the voltage and current output DAC71 and DAC72 model families. The DAC700 and DAC702 are also pin-compatible with the DAC70 model family. In addition, the DAC703 is offered in a 24-pin SOIC package for surface mount applications.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and rated power supplies unless otherwise noted

MODEL	DAC702/703J			DAC700/701/702/703K			DAC700/701/702/703B, S			DAC700/701/702/703L, C			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT													
DIGITAL INPUT													
Resolution			16			*			*			*	Bits
Digital Inputs[1]													
V_{IH}	+2.4		$+V_{CC}$	*		*	*		*	*		*	V
V_{IL}	−1 0		+0.8	*		*	*		*	*		*	V
I_{IH}, V_I = +2 7V			+40			*			*			*	μA
I_{IL}, V_I = +0 4V		−0 35	−0 5		*	*		*	*		*	*	mA
TRANSFER CHARACTERISTICS													
ACCURACY[2]													
Linearity Error[4]		±0.0015	±0.006		*	±0 003		*	*		±0 00075	±0 0015	% of FSR[3]
Differential Linearity Error[4]		±0.003	±0.012		*	±0 006		*	*		±0.0015	±0 003	% of FSR
Differential Linearity Error at Bipolar Zero (DAC702/703)[4]					±0 003	±0 006		±0 0015	±0 003		*	*	% of FSR
Gain Error[5]		±0 07	±0.30		*	±0.15		±0 05	±0 10		*	*	%
Zero Error[5][6]		±0 05	±0.10		*	*		*	*		*	*	% of FSR
Monotonicity Over Spec Temp Range	13			14			*			15			Bits
DRIFT (over specification temperature range)													
Total Error Over Temperature Range (all models)[7]		±0 08			*	±0 15		±0 05	±0 10		*	*	% of FSR
Total Full Scale Drift													
DAC700/701		±10			*	±30		±8 5	±18		±6	±13	ppm of FSR/°C
DAC702/703		±10			*	±25		±7	±15		*	*	ppm of FSR/°C
Gain Drift (all models)		±10	±30		*	±25		±7	±15		±5	±10	ppm/°C
Zero Drift													
DAC700/701					±2 5	±5		±1 5	±3		*	*	ppm of FSR/°C
DAC702/703		±5	±15		*	±12		±4	±10		±2 5	±5	ppm of FSR/°C
Differential Linearity Over Temp [4]			±0 012			+0 009, −0 006			*			+0 006, −0 003	% of FSR
Linearity Error Over Temp [4]			±0 012			±0 006			*			±0 003	% of FSR
SETTLING TIME (to ±0 003% of FSR)[8]													
DAC701/703 (V_{OUT} models)													
Full Scale Step, 2kΩ load		4			*	8		*	*		*	*	μsec
1LSB Step at Worst-Case Code[9]		2 5			*			*			*		μsec
Slew Rate		10			*			*			*		V/μsec
DAC700/702 (I_{OUT} models)													
Full Scale Step (2mA), 10 to 100Ω load		350			*	1000		*	*		*	*	nsec
1kΩ load		1			*	3		*	*		*	*	μsec
OUTPUT													
VOLTAGE OUTPUT MODELS													
DAC701 (CSB Code)					0 to +10			*					V
DAC703 (COB Code)		±10			*			*			*		V
Output Current	±5			*			*			*			mA
Output Impedance		0 15			*			*			*		Ω
Short Circuit to Common Duration		Indefinite			*			*			*		
CURRENT OUTPUT MODELS													
DAC700 (CSB Code)[10]					0 to −2			*			*		mA
Output Impedance[10]					4			*			*		kΩ
DAC702 (COB Code)[10]		±1			*			*			*		mA
Output Impedance[10]		2 45			*			*			*		kΩ
Compliance Voltage		±2 5			*			*			*		V

ELECTRICAL (CONT)

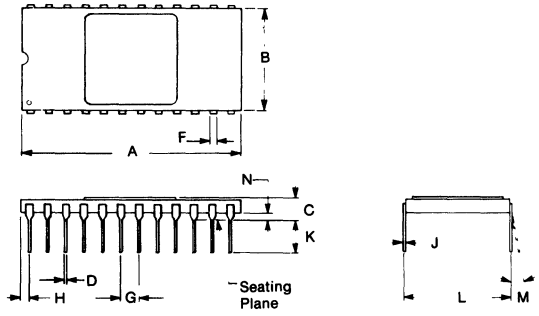
MODEL	DAC702/703J			DAC700/701/702/703K			DAC700/701/702/703B, S			DAC700/701/702/703L, C			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
REFERENCE VOLTAGE													
Voltage		+6.3		+6.0	+6.3	+6.6	+6.24	+6.3	+6.36	*	*	*	V
Source Current Available for External Loads		+2.5		+1.5	*		*	*		*	*		mA
Temperature Coefficient		±10			*	±25		*	±15		*	*	ppm/°C
Short Circuit to Common Duration		Indefinite			*			*			*		
POWER SUPPLY REQUIREMENTS													
Voltage: $+V_{CC}$	13.5	15	16 5	*	*	*	*	*	*	*	*	*	V
$-V_{CC}$	13.5	15	16 5	*	*	*	*	*	*	*	*	*	V
V_{DD}	+4.5	+5	+16.5	*	*	*	*	*	*	*	*	*	V
Current (no load):													
DAC700/702 (I_{OUT} models)													
$+V_{CC}$		+10			*	+25		*	*		*	*	mA
$-V_{CC}$		−13			*	−25		*	*		*	*	mA
V_{DD}		+4			*	+8		*	*		*	*	mA
DAC701/703 (V_{OUT} models)													
$+V_{CC}$		+16			*	+30		*	*		*	*	mA
$-V_{CC}$		−18			*	−30		*	*		*	*	mA
V_{DD}		+4			*	+8		*	*		*	*	mA
Power Dissipation (V_{DD} = +5.0V)[11]													
DAC700/702		365			*	790		*	630		*	*	mW
DAC701/703		530			*	940		*	780		*	*	mW
Power Supply Rejection:													
$+V_{CC}$		±0.0015	±0.006		*	*		*	±0.003		*	*	% of FSR/%V_{CC}
$-V_{CC}$		±0.0015	±0.006		*	*		*	±0 003		*	*	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001		*	*		*	*		*	*	% of FSR/%V_{DD}
TEMPERATURE RANGE													
Specification.													
B, C grades							−25		+85	*		*	°C
S grades							−55		+125				°C
J, K, L grades	0		+70	*		*				0		+70	°C
Storage. Ceramic				−60		+150	*		*	*		*	°C
Plastic, SOIC	−60		+100	*		*							°C

*Specification same as model to the left.

NOTES (1) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC, and 54/74HTC compatible over the operating voltage range of V_{DD} = +5V to +15V and over the specified temperature range The input switching threshold remains at the TTL threshold of 1 4V over the supply range of V_{DD} = +5V to +15V As logic "0" and logic "1" inputs vary over 0V to +0 8V and +2.4V to +10V respectively, the change in the D/A converter output voltage will not exceed ±0 0015% of FSR for the LH and CH grades, ±0.003% of FSR for the BH grade and ±0 006% of FSR for the KG grade (2) DAC700 and DAC702 (current-output models) are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all parameters except settling time (3) FSR means full-scale range and is 20V for the ±10V range (DAC703), 10V for the 0 to +10V range (DAC701). FSR is 2mA for the ±1mA range (DAC700) and the 0 to +2mA range (DAC702) (4) ±0 0015% of full-scale range is equivalent to 1LSB in 15-bit resolution ±0 003% of full-scale range is equivalent to 1LSB in 14-bit resolution ±0 006% of full-scale range is equivalent to 1LSB in 13-bit resolution (5) Adjustable to zero with external trim potentiometer Adjusting the gain potentiometer rotates the transfer function around the zero point (6) Error at input code $FFFF_H$ for DAC700 and DAC701, $7FFF_H$ for DAC702 and DAC703 (7) With gain and zero errors adjusted to zero at +25°C (8) Maximum represents the 3σ limit Not 100% tested for this parameter (9) At the major carry, $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$ (10) Tolerance on output impedance and output current is ±30% (11) Power dissipation is an additional 40mW when V_{DD} is operated at +15V

MECHANICAL

H Package

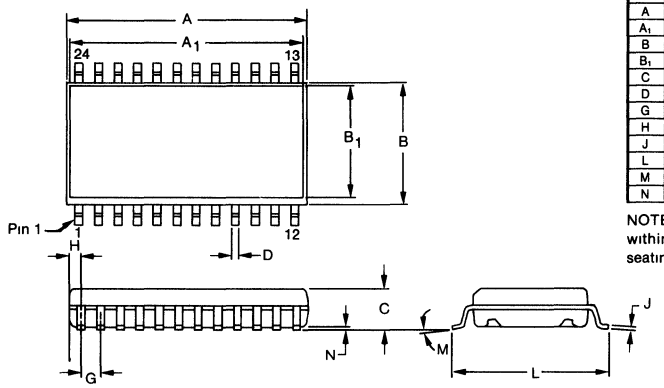


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 185	1 215	30 10	30 86
B	600	620	15 24	15 75
C	125	171	3 18	4 34
D	015	021	0 38	0 53
F	035	060	0 89	1 52
G	100 BASIC		2 54 BASIC	
H	030	070	0 76	1 78
J	008	012	0 20	0 30
K	120	240	3 05	6 10
L	600 BASIC		15 24 BASIC	
M	—	10°	—	10°
N	025	060	0.64	1 52

NOTE Leads in true position within .010" (25mm) R at MMC at seating plane

MECHANICAL

U Package (DAC703 Only)

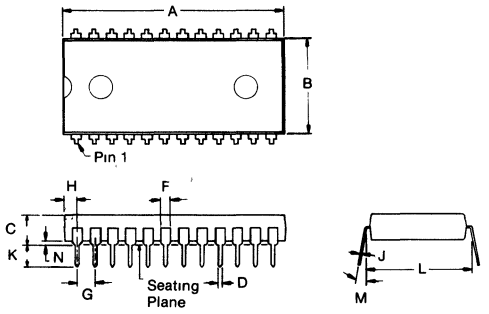


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	602	618	15 29	15 70
A_1	595	618	15 11	15 70
B	286	302	7 26	7 67
B_1	270	285	6.86	7 24
C	093	108	2 36	2 74
D	015	019	0 38	0 48
G	050 BASIC		1 27 BASIC	
H	026	034	0 66	0 86
J	008	012	0 20	0 30
L	390	422	9 91	10 72
M	0°	10°	0°	10°
N	000	012	0 00	0 30

NOTE Leads in true position within 0 01" (0.25mm) R at MMC at seating plane

MECHANICAL

P Package



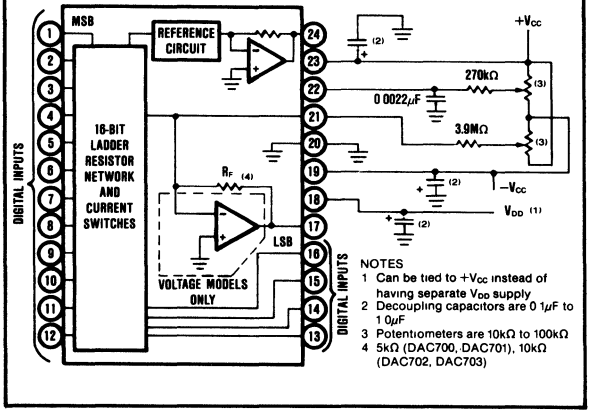
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 233	1 283	31 32	32 59
B	538	575	13 67	14 61
C	169	224	4 29	5 70
D	015	023	0 38	0 58
F	043	062	1 09	1 57
G	100 BASIC		2 54 BASIC	
H	030	090	0 76	2 29
J	008	015	0 20	0 38
K	100	132	2 54	3 35
L	600 BASIC		15 24 BASIC	
M	0°	15°	0°	15°
N	018	022	0 46	0.56

NOTE Leads in true position within 010" (25mm) R at MMC at seating plane

PIN ASSIGNMENTS

Pin #	H and P Packages	
	DAC700/702	DAC701/703
1	Bit 1 (MSB)	Bit 1 (MSB)
2	Bit 2	Bit 2
3	Bit 3	Bit 3
4	Bit 4	Bit 4
5	Bit 5	Bit 5
6	Bit 6	Bit 6
7	Bit 7	Bit 7
8	Bit 8	Bit 8
9	Bit 9	Bit 9
10	Bit 10	Bit 12
11	Bit 11	Bit 11
12	Bit 12	Bit 12
13	Bit 13	Bit 13
14	Bit 14	Bit 14
15	Bit 15	Bit 15
16	Bit 16 (LSB)	Bit 16 (LSB)
17	$R_{FEEDBACK}$	V_{OUT}
18	V_{DD}	V_{DD}
19	$-V_{CC}$	$-V_{CC}$
20	Common	Common
21	I_{OUT}	Summing Junction (Zero Adjust)
22	Gain Adjust	Gain Adjust
23	$+V_{CC}$	$+V_{CC}$
24	+6 3V Reference Output	+6 3V Reference Output

CONNECTION DIAGRAMS



NOTES
1 Can be tied to $+V_{CC}$ instead of having separate V_{DD} supply
2 Decoupling capacitors are 0 1μF to 1 0μF
3 Potentiometers are 10kΩ to 100kΩ
4 5kΩ (DAC700, DAC701), 10kΩ (DAC702, DAC703)

ORDERING INFORMATION

Model	Package	Output Configuration	Temperature Range	Linearity Error, max at 25°C (% of FSR)	Gain Drift max, (ppm/°C)
DAC702JP, DAC703JP	Plastic DIP	±1mA, ±10V	0°C to +70°C	±0.006	±30
DAC702KP, DAC703KP	Plastic DIP	±1mA, ±10V	0°C to +70°C	±0.003	±25
DAC700KH, DAC701KH	Ceramic DIP	0 to −1mA, 0 to +10V	0°C to +70°C	±0 003	±25
DAC702KH, DAC703KH	Ceramic DIP	±1mA, ±10V	0°C to +70°C	±0.003	±25
DAC700BH, DAC701BH	Ceramic DIP	0 to −1mA, 0 to +10V	−25°C to +85°C	±0.003	±15
DAC702BH, DAC703BH	Ceramic DIP	±1mA, ±10V	−25°C to +85°C	±0 003	±15
DAC700BH/QM, DAC701BH/QM	Ceramic DIP	0 to −1mA, 0 to +10V	−25°C to +85°C	±0 003	±15
DAC702BH/QM, DAC703BH/QM	Ceramic DIP	±1mA, ±10V	/QM screening	±0 003	±15
DAC700LH, DAC701LH	Ceramic DIP	0 to −2mA, 0 to +10V	0°C to +70°C	±0 0015	±10
DAC700CH, DAC701CH	Ceramic DIP	0 to −2mA, 0 to +10V	−25°C to +85°C	±0.0015	±10
DAC700SH, DAC701SH	Ceramic DIP	0 to −1mA, 0 to +10V	−55°C to +125°C	±0.003	±15
DAC702LH, DAC703LH	Ceramic DIP	±1mA, ±10V	0°C to +70°C	±0 0015	±10
DAC702CH, DAC703CH	Ceramic DIP	±1mA, ±10V	−25°C to +85°C	±0 0015	±10
DAC702SH, DAC703SH	Ceramic DIP	±1mA, ±10V	−55°C to +125°C	±0 003	±15
DAC700SH/QM, DAC701SH/QM	Ceramic DIP	0 to −1mA, 0 to +10V	−55°C to +125°C	±0 003	±15
DAC702SH/QM, DAC703SH/QM	Ceramic DIP	±1mA, ±10V	/QM screening	±0 003	±15

BURN-IN SCREENING OPTION
See text for details

Model	Package	Output Configuration	Temperature Range	Linearity Error, max at 25°C (% of FSR)	Burn-In Temp. (160h)[1]
DAC702JP-BI	Plastic DIP	±1mA	0°C to +70°C	±0 006	85°C
DAC703JP-BI	Plastic DIP	±10V	0°C to +70°C	±0 006	85°C
DAC702KP-BI	Plastic DIP	±1mA	0°C to +70°C	±0 003	85°C
DAC703KP-BI	Plastic DIP	±10V	0°C to +70°C	±0 003	85°C
DAC703JU	Plastic SOIC	±10V	0°C to +70°C	±0 006	85°C
DAC703KU	Plastic SOIC	±10V	0°C to +70°C	±0 003	85°C
DAC703JU-BI	Plastic SOIC	±10V	0°C to +70°C	±0.006	85°C
DAC703KU-BI	Plastic SOIC	±10V	0°C to +70°C	±0 003	85°C
DAC700KH-BI	Ceramic DIP	0 to −1mA	0°C to +70°C	±0 003	85°C
DAC700LH-BI	Ceramic DIP	0 to −2mA	0°C to +70°C	±0 0015	85°C
DAC700BH-BI	Ceramic DIP	0 to −1mA	−25°C to +85°C	±0 003	85°C
DAC700CH-BI	Ceramic DIP	0 to −2mA	−25°C to +85°C	±0 0015	85°C
DAC700SH-BI	Ceramic DIP	0 to −1mA	−55°C to +125°C	±0 003	125°C
DAC701KH-BI	Ceramic DIP	0 to +10V	0°C to +70°C	±0 003	85°C
DAC701LH-BI	Ceramic DIP	0 to +10V	0°C to +70°C	±0 0015	85°C
DAC701BH-BI	Ceramic DIP	0 to +10V	−25°C to +85°C	±0 003	85°C
DAC701CH-BI	Ceramic DIP	0 to +10V	−25°C to +85°C	±0.0015	85°C
DAC701SH-BI	Ceramic DIP	0 to +10V	−55°C to +125°C	±0 003	125°C
DAC702KH-BI	Ceramic DIP	±1mA	0°C to +70°C	±0.003	85°C
DAC702LH-BI	Ceramic DIP	±1mA	0°C to +70°C	±0 0015	85°C
DAC702BH-BI	Ceramic DIP	±1mA	−25°C to +85°C	±0 003	85°C
DAC702CH-BI	Ceramic DIP	±1mA	−25°C to +85°C	±0 0015	85°C
DAC702SH-BI	Ceramic DIP	±1mA	−55°C to +125°C	±0 003	125°C
DAC703KH-BI	Ceramic DIP	±10V	0°C to +70°C	±0 003	85°C
DAC703LH-BI	Ceramic DIP	±10V	0°C to +70°C	±0 0015	85°C
DAC703BH-BI	Ceramic DIP	±10V	−25°C to +85°C	±0 003	85°C
DAC703CH-BI	Ceramic DIP	±10V	−25°C to +85°C	±0 0015	85°C
DAC703SH-BI	Ceramic DIP	±10V	−55°C to +125°C	±0 003	125°C

NOTE. (1) Or equivalent combination of time and temperature

ABSOLUTE MAXIMUM RATINGS

+V_{CC} to Common ..... 0V, +18V
−V_{CC} to Common ..... 0V, −18V
V_{DD} to Common ..... 0V, +18V
Digital Data Inputs to Common ..... −1V, +18V
Reference Out to Common ..... Indefinite Short to Common
External Voltage Applied to R_F (DAC700/702) ..... ±18V
External Voltage Applied to D/A Output
(DAC701/703) ..... −5V to +5V

V_{OUT} (DAC701/703) ..... Indefinite Short to Common
Power Dissipation 1000mW
Storage Temperature ..... −60°C to +150°C
Lead Temperature (soldering, 10s) ..... 300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device Exposure to absolute maximum conditions for extended periods may affect device reliability

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC700/701/702/703 accept complementary digital input codes in either binary format (CSB, Unipolar or COB, Bipolar). The COB models DAC702/703 may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

TABLE I. Digital Input Codes.

Digital Input Codes	Analog Output		
	DAC700/701 Complementary Straight Binary (CSB)	DAC702/703 Complementary Offset Binary (COB)	DAC702/703 Complementary Two's Complement (CTC)*
0000_H	+ Full Scale	+ Full Scale	−1LSB
$7FFF_H$	+1/2 Full Scale	Bipolar Zero	− Full Scale
8000_H	+1/2 Full Scale −1LSB	−1LSB	+ Full Scale
$FFFF_H$	Zero	− Full Scale	Bipolar Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (all bits ON point and all bits OFF point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output step sizes can be between 1/2LSB and 3/2LSB when the input changes from one adjacent input state to the next. A negative DLE specification of no more than −1LSB (−0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC700/701/702/703 are specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by: (1) testing the end point differences for each D/A at t_{min}, +25°C and t_{max}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Zero Drift

Zero drift is a measure of the change in the output with $FFFF_H$ (DAC700 and DAC701) applied to the digital inputs over the specified temperature range. For the bipolar models, zero is measured at $7FFF_H$ (bipolar zero) applied to the digital inputs. This code corresponds to zero volts (DAC703) or zero milliamps (DAC702) at the analog output. The maximum change in offset at t_{min} or t_{max} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per degree centigrade (ppm of FSR/°C).

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

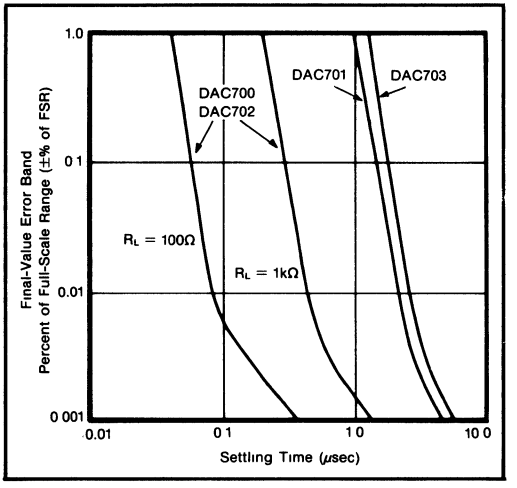


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2 LSB for 14 bits) for two input conditions: a full-scale range change of 20V (DAC703) or 10V (DAC701) and a 1LSB change at the "major carry," the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next).

Current Output

Settling times are specified to±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2).

It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

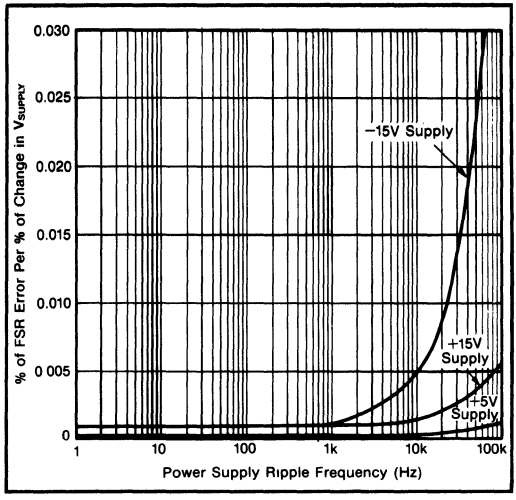


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

REFERENCE SUPPLY

All models have an internal low-noise +6.3V reference voltage derived from an on-chip buried zener diode. This reference voltage, available to the user, has a tolerance of ±5% (KH models) and ±1% (BH models). A minimum of 1.5mA is available for external loads. Since the output impedance of the reference output is typically 1Ω, the external load should remain constant.

If a varying load is to be driven by the reference supply, an external buffer amplifier is recommended to drive the load in order to isolate the Bipolar Offset (connected internally to the reference) from load variations.

BURN-IN SCREENING

Burn-in screening is an option available for the entire DAC700 through DAC703 family of products. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

Model	Temp. Range	Burn-In Screening
DAC703KU-BI	0°C to +70°C	160 hours at 85°C
DAC700BH-BI	−25°C to +85°C	160 hours at 85°C
DAC702SH-BI	−55°C to +125°C	160 hours at 125°C

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

ENVIRONMENTAL SCREENING /QM Screening

Screening Flow For /QM Models

Screen	MIL-STD-883 Method	Condition	Comments
Internal Visual	2010	B	
High Temperature Storage (Stabilization Bake)	1008	C	+150°C, 24hrs
Temperature Cycling	1010	C	−65 to +150°C, 10 cycles
Burn-in	1015	B	+125°C, 160hrs
Constant Acceleration	2001	E	30,000 Gs
Hermeticity Fine Leak Gross Leak	 1014 1014	 A1 or A2 C	 5×10^{-8} atm cc/sec 60psig, 2hrs
External Visual	2009		

Burr-Brown /QM models are environmentally-screened versions of our standard industrial products, designed to provide enhanced reliability. The screening, tabulated below, is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified below. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1μF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should

be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ part. A 0.001μF to 0.01μF ceramic capacitor should be connected from Gain Adjust to Common to prevent noise pickup. Refer to Figures 4 and 5 for the relationship of zero and gain adjustments to unipolar and bipolar D/A converters.

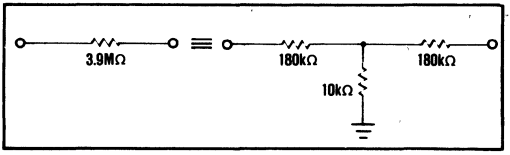


FIGURE 3. Equivalent Resistances.

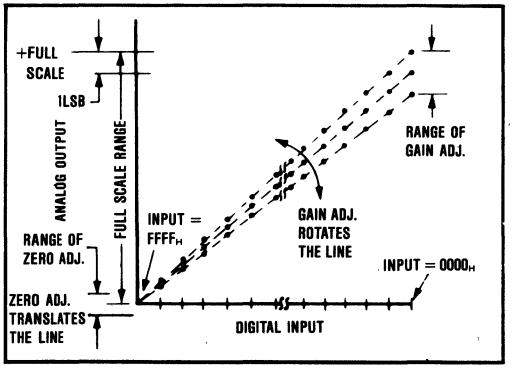


FIGURE 4. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters, DAC700 and DAC701.

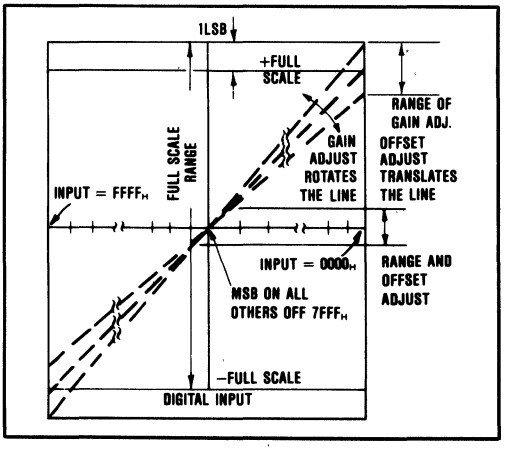


FIGURE 5. Relationship of Zero and Gain Adjustments for Bipolar D/A converters, DAC702 and DAC703.

Zero Adjustment

For unipolar (CSB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that produces zero output voltage or current. See Table II for corresponding codes and the Connection Diagram for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagram for gain adjustment circuit connections.

INSTALLATION CONSIDERATIONS

This D/A converter family is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bit 15 and bit 16 should be connected to V_{DD} through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 18 inches of wire will produce a 1LSB error in the analog output voltage!

In Figures 6, 7, and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed during initial calibration. R_3 is part of R_L, if the output voltage is sensed at Common, and therefore introduces no error. If R_L is variable, then R_2 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is 5kΩ, then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_4 is negligible.

In many applications it is impractical to sense the output voltage at the output pin. Sensing the output voltage at the system ground point is permissible with the DAC700 family because the D/A converter is designed to have a constant return current of approximately 2mA flowing from Common. The variation in this current is under 20μA (with changing input codes), therefore R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 ($R_4 \times$ 2mA) appears as a zero error and can be removed with

TABLE II. Digital Input and Analog Output Relationships.

VOLTAGE OUTPUT MODELS						
	Analog Output					
	DAC701 Unipolar			DAC703 Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μV)	153	305	610	305	610	1224
0000H (V)	+9 99985	+9 99969	+9.99939	+9.99960	+9 99939	+9.99878
FFFFH (V)	0	0	0	−10.0000	−10.0000	−10 0000
CURRENT OUTPUT MODELS						
	Analog Output					
	DAC700 Unipolar			DAC702 Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μA)	0.031	0 061	0.122	0 031	0.061	0.122
0000H (mA)	−1.99997	−1.99994	−1 99988	−0.99997	−0.99994	−0.99988
FFFFH (mA)	0	0	0	+1.00000	+1 00000	+1.00000

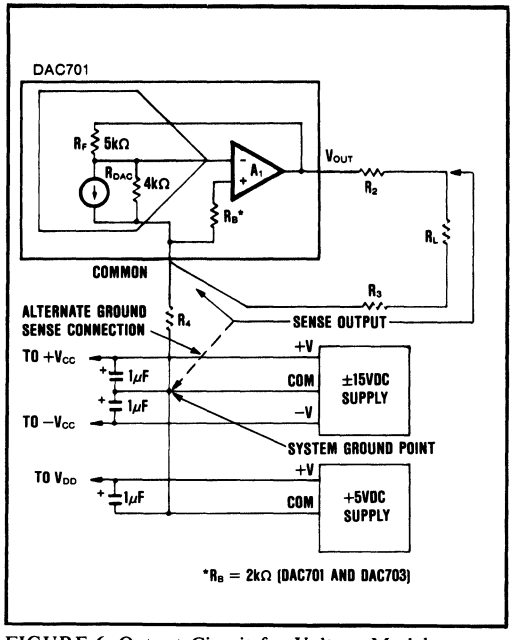


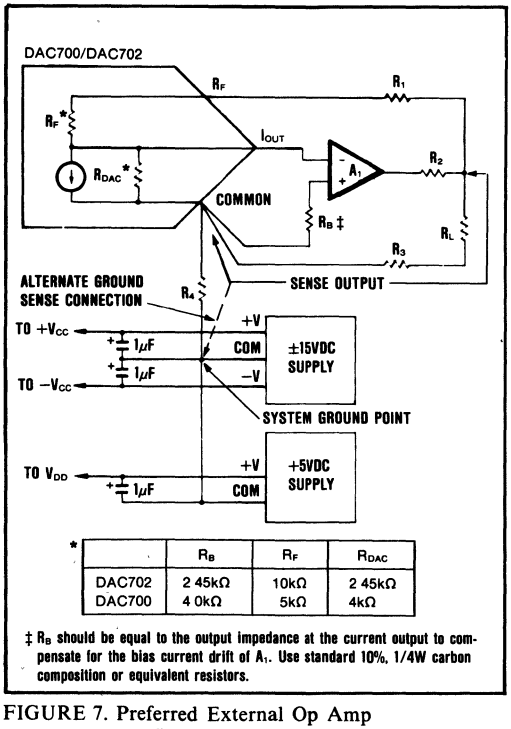
FIGURE 6. Output Circuit for Voltage Models.

the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figures 6, 7, and 8.

Figures 7 and 8 show two methods of connecting the current output models (DAC700 or DAC702) with external precision output op amps. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A_1 at R_L), the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

If the output cannot be sensed at Common or the system ground point as mentioned above, the differential output circuit shown in Figure 8 is recommended. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible, the circuit of Figure 8 can be reduced to the one shown in Figure 7. Again the effect of R_4 is negligible.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close

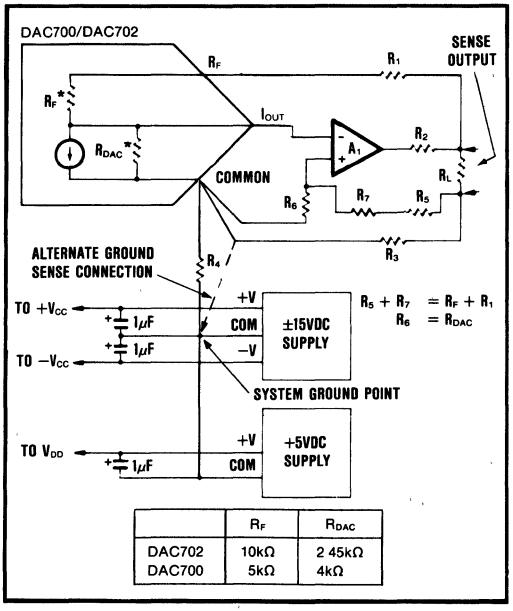


*	RB	RF	RDAC
DAC702	2 45kΩ	10kΩ	2 45kΩ
DAC700	4 0kΩ	5kΩ	4kΩ

‡ RB should be equal to the output impedance at the current output to compensate for the bias current drift of A1. Use standard 10%, 1/4W carbon composition or equivalent resistors.

FIGURE 7. Preferred External Op Amp Configuration.

together. This reduces the external magnetic field along with any radiation. Also, if a single lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.



	R_F	R_{DAC}
DAC702	10kΩ	2 45kΩ
DAC700	5kΩ	4kΩ

FIGURE 8. Differential Sensing Output Op Amp Confjguration.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT D/As

DAC700 and DAC702 are current output devices and will drive the summing junction of an op amp to produce an output voltage as shown in Figure 9. Use of the internal feedback resistor is required to obtain specified gain accuracy and low gain drift.

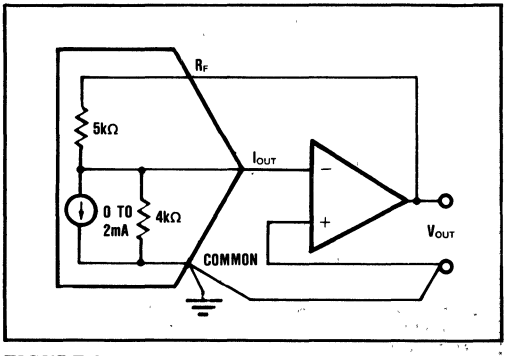


FIGURE 9. External Op Amp Using Internal Feedback Resistors.

DAC700 or DAC702 can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±50ppm/°C. The resistors in the DAC700 and DAC702 ratio track to ±1ppm/°C but their absolute TCR may be as high as ±50ppm/°C.

An alternative method of scaling the output voltage of the D/A converter and preserving the low gain drift is shown in Figure 10.

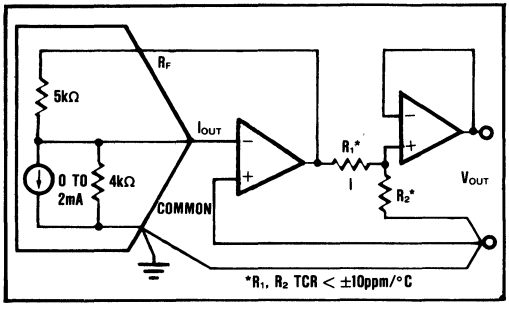


FIGURE 10. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift.

OUTPUTS LARGER THAN 20-VOLT RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and −2mA for unipolar voltage ranges (see Figure 11). Use protection diodes as shown when a high voltage op amp is used.

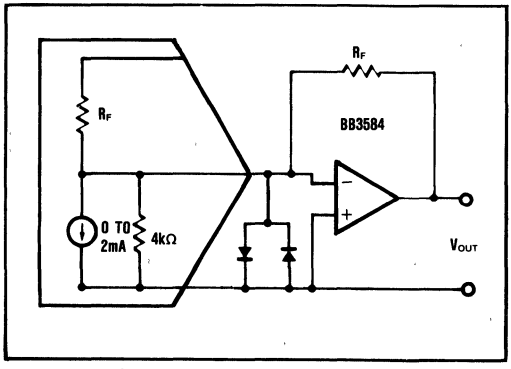
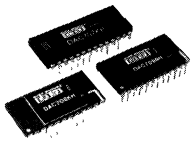


FIGURE 11. External Op Amp Using External Feedback Resistors.

BURR-BROWN®



DAC705/706/707
DAC708/709

Microprocessor-Compatible 16-BIT DIGITAL-TO-ANALOG CONVERTERS

FEATURES

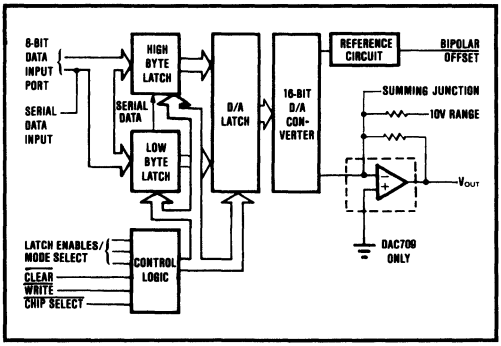
- TWO-CHIP CONSTRUCTION
- HIGH-SPEED 16-BIT PARALLEL, 8-BIT (BYTE) PARALLEL, AND SERIAL INPUT MODES
- DOUBLE-BUFFERED INPUT REGISTER CONFIGURATION
- V_{OUT} AND I_{OUT} MODELS
- HIGH ACCURACY:
  Linearity Error ±0.003% of FSR max
  Differential Linearity Error ±0.006% of FSR max
- MONOTONIC (TO 14 BITS) OVER SPECIFIED TEMPERATURE RANGE
- HERMETICALLY SEALED
- LOW COST PLASTIC VERSIONS AVAILABLE (DAC707JP/KP)

DESCRIPTION

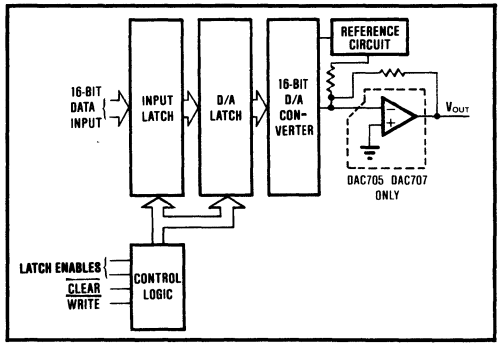
The DAC708 and DAC709 are 16-bit converters designed to interface to an 8-bit microprocessor bus. 16-bit data is loaded in two successive 8-bit bytes into parallel 8-bit latches before being transferred into the D/A latch. The DAC708 and DAC709 are current and voltage output models respectively and are in 24-pin hermetic DIPs. Input coding is Binary Two's Complement (bipolar) or Unipolar Straight Binary (unipolar, when an external logic inverter is used to invert the MSB). In addition, the DAC708/-709 can be loaded serially (MSB first).

The DAC705, DAC706, and DAC707 are designed to interface to a 16-bit bus. Data is written into a 16-bit latch and subsequently the D/A latch. The DAC705 and DAC707 are voltage output models. DAC706 is a current output model. Outputs are bipolar only (current or voltage) and input coding is Binary Two's Complement (BTC).

All models have Write and Clear control lines as well as input latch enable lines. In addition, DAC708 and DAC709 have Chip Select control lines. In the bipolar mode, the Clear input sets the D/A latch to give zero voltage or current output. They are all 14-bit accurate and are complete with reference, and for the DAC705, DAC707, and DAC709, a voltage output amplifier. All models are available with an optional burn-in, or environmental screening.



DAC708/709 Block Diagram



DAC705/706/707 Block Diagram

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable. BBRCORP - Telex: 66-6491

PDS-557D

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_{CC} = ±15V, V_{DD} = +5V, and after a 10-minute warm-up unless otherwise noted.

MODEL	DAC707JP			DAC705/706/707/708/709KH, DAC707KP			DAC705/706/707/708/ 709BH, SH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT										
DIGITAL INPUT										
Resolution			16			*			*	Bits
Bipolar Input Code (all models)		Binary Two's Complement			*			*		
Unipolar Input Code[1] (DAC708/709 only)					Unipolar Straight Binary			*		
Logic Levels[2] V_{IH}	+2.0		+5 5	*		*	*		*	V
V_{IL}	−1.0		+0 8	*		*	*		*	V
I_{IH} (V_I = +2 7V)			1			*			*	μA
I_{IL} (V_I = +0 4V)			1			*			*	μA
TRANSFER CHARACTERISTICS										
ACCURACY[3]										
Linearity Error		±0 003	±0 006		±0 0015	±0 003		*	*	% of FSR[4]
Differential Linearity Error[5]		±0.0045	±0 012		±0 003	±0.006		*	*	% of FSR
at Bipolar Zero[5, 6]					±0.003	±0.006		±0 0015	±0 003	% of FSR
Gain Error[7]		±0.07	±0 30		*	±0 15		±0 05	±0.10	%
Zero Error[7]		±0 05	±0 1		*	*		*	*	% of FSR
Monotonicity Over Spec Temp Range	13			14			14			Bits
Power Supply Sensitivity· $+V_{CC}$, $-V_{CC}$		±0.0015	±0.006		*	*		*	±0 003	% of FSR/%V_{CC}
V_{DD}		±0 0001	±0 001		*	*		*	*	% of FSR/%V_{DD}
DRIFT (over Spec Temp range[3])										
Total Error over Temp Range[8]		±0.08			*	±0.15		*	±0.10	% of FSR
Total Full Scale Drift		±10			*	±25		*	±15	ppm of FSR/°C
Gain Drift		±10	±30		*	±25		±7	±15	ppm/°C
Zero Drift· Unipolar (DAC708/709 only)					±2 5	±5		±1 5	±3	ppm of FSR/°C
Bipolar (all models)		±5	±15		*	±12		±4	±10	ppm of FSR/°C
Differential Linearity Over Temp[5]			±0.012			+0 009, −0.006			*	% of FSR
Linearity Error Over Temp[5]			±0 012			±0 006			*	% of FSR
SETTLING TIME (to ±0.003% of FSR)[9]										
Voltage Output Models										
Full Scale Step (2kΩ load)		4			*	8		*	8	μs
1LSB Step at Worst Case Code[10]		2.5			*	4		*	4	μs
Slew Rate		10			*			*		V/μs
Current Output Models										
Full Scale Step (2mA). 10 to 100Ω load					350			*		ns
1kΩ load					1			*		μs
OUTPUT										
VOLTAGE OUTPUT MODELS										
Output Voltage Range										
DAC709: Unipolar (USB Code)					0 to +10			*		V
Bipolar (BTC Code)					±5, ±10			*		V
DAC707 Bipolar (BTC Code)		±10			*			*		V
DAC705 Bipolar (BTC Code)					±5			*		V
Output Current	±5			*			*			mA
Output Impedance		0 15			*			*		Ω
Short Circuit to Common Duration		Indefinite			*			*		
CURRENT OUTPUT MODELS										
Output Current Range (±30% typ)										
DAC708 Unipolar (USB Code)					0 to −2			*		mA
Bipolar (BTC Code)					±1			*		mA
DAC706 Bipolar (BTC Code)					±1					mA
Unipolar Output Impedance (±30% typ)					4.0			*		kΩ
Bipolar Output Impedance (±30% typ)					2.45			*		kΩ
Compliance Voltage					±2 5			*		V
POWER SUPPLY REQUIREMENTS										
Voltage (all models) $+V_{CC}$	+13.5	+15	+16.5	*	*	*	*	*	*	V
$-V_{CC}$	−13.5	−15	−16 5	*	*	*	*	*	*	V
V_{DD}	+4 5	+5	+5.5	*	*	*	*	*	*	V
Current (No load, +15V supplies)										
Current Output Models. $+V_{CC}$					+10	+25		*	*	mA
$-V_{CC}$					−13	−25		*	*	mA
V_{DD}					+5	+10		*	*	mA
Voltage Ouptut Models: $+V_{CC}$		+16	+30		*	*		*	*	mA
$-V_{CC}$		−18	−30		*	*		*	*	mA
V_{DD}		+5	+10		*	*		*	*	mA

ELECTRICAL (CONT)

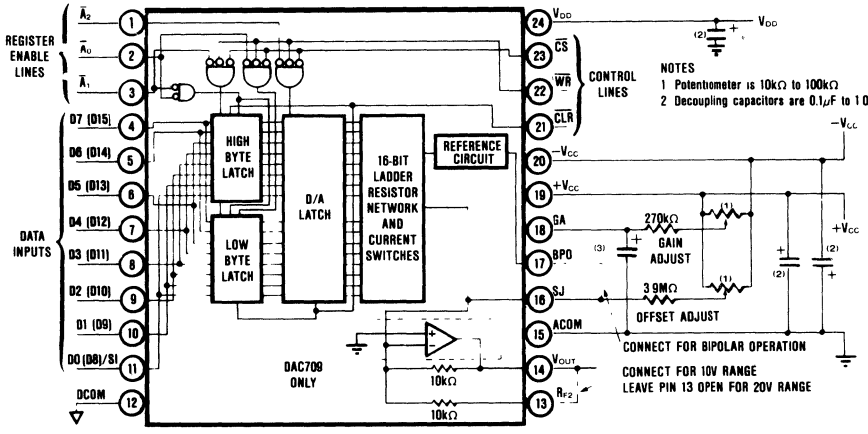
MODEL	DAC707JP			DAC705/706/707/708/709KH, DAC707KP			DAC705/706/707/708/ 709BH, SH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS (CONT)										
Power Dissipation (±15V supplies)										
Current Output Models					370	800		*	*	mW
Voltage Output Models		535			*	950		*	*	mW
TEMPERATURE RANGE										
Specification BH grades							−25		+85	°C
JP, KP, KH grades	0		+70	*		*				°C
SH grades							−55		+125	°C
Storage Ceramic				−65		+150	−65		+150	°C
Plastic	−60		+100	*		*				°C

*Specification same as for models in column to the left

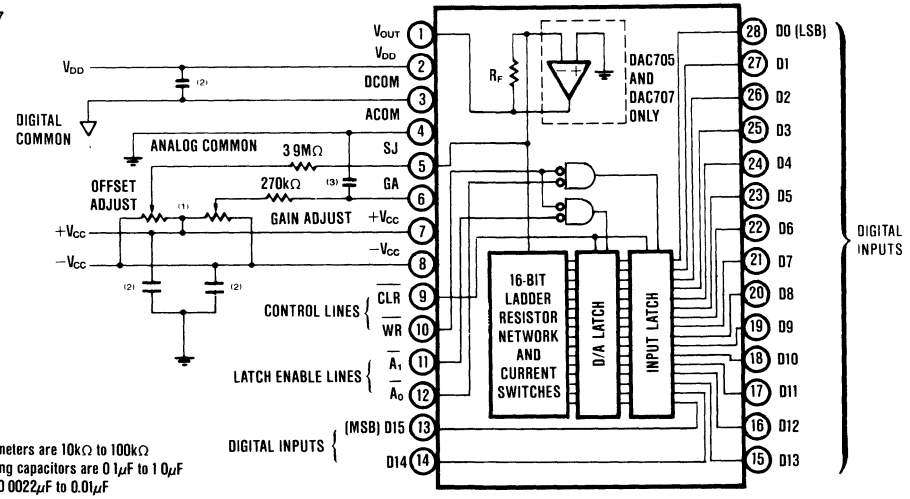
NOTES (1) MSB must be inverted externally prior to DAC708/709 input (2) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC and 54/74HTC compatible over the specified temperature range (3) DAC706 and DAC708 (current-output models) are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all tests (4) FSR means Full Scale Range For example, for ±10V output, FSR = 20V (5) ±0 0015% of Full Scale Range is equal to 1 LSB in 16-bit resolution ±0 003% of Full Scale Range is equal to 1 LSB in 15-bit resolution ±0 006% of Full Scale Range is equal to 1 LSB in 14-bit resolution (6) Error at input code 0000_H (For unipolar connection on DAC708/709, the MSB must be inverted externally prior to D/A input) (7) Adjustable to zero with external trim potentiometer Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point (8) With gain and zero errors adjusted to zero at +25°C (9) Maximum represents the 3σ limit Not 100% tested for this parameter (10) The bipolar worst-case code change is $FFFF_H$ to 0000_H and 0000_H to $FFFF_H$ For unipolar (DAC708/709 only) it is $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$

CONNECTION DIAGRAMS

DAC708/709



DAC705/706/707

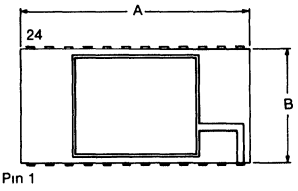


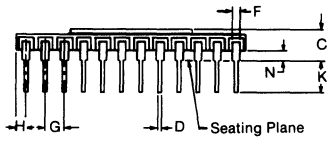
DESCRIPTION OF PIN FUNCTIONS

DAC705/706/707		Pin	DAC708/709	
Designator	Description	#	Designator	Description
V_{OUT} (DAC707 and DAC705) R_F (DAC706)	Voltage output for DAC707 (±10V) and DAC705 (±5V) or an internal feedback resistor for use with an external output op amp for the DAC706.	1	A_2	Latch enable for D/A latch (Active low)
V_{DD}	Logic supply (+5V)	2	A_0	Latch enable for "low byte" input (Active low) When both A_0 and A_1 are logic "0", the serial input mode is selected and the serial input is enabled
DCOM	Digital common	3	A_1	Latch enable for "high byte" input (Active low) When both A_0 and A_1 are logic "0", the serial input mode is selected and the serial input is enabled
ACOM	Analog common	4	D7 (D15)	Input for data bit 7 if enabling low byte (LB) latch or data bit 15 if enabling the high byte (HB) latch
SJ (DAC705 and DAC707) I_{OUT} (DAC706)	Summing junction of the internal output op amp for the DAC705 and DAC707, or the current output for the DAC706 Offset adjust circuit is connected to the summing junction of the output amplifier Refer to Block Diagram	5	D6 (D14)	Input for data bit 6 if enabling LB latch or data bit 14 if enabling the HB latch
GA	Gain adjust pin Refer to Connection Diagram for gain adjust circuit	6	D5 (D13)	Data bit 5 (LB) or data bit 13 (HB)
$+V_{CC}$	Positive supply voltage (+15V)	7	D4 (D12)	Data bit 4 (LB) or data bit 12 (HB)
$-V_{CC}$	Negative supply voltage (−15V)	8	D3 (D11)	Data bit 3 (LB) or data bit 11 (HB)
CLR	Clear line. Sets the input latch to zero and sets the D/A latch to the input code that gives bipolar zero on the D/A output (Active low)	9	D2 (D10)	Data bit 2 (LB) or data bit 10 (HB)
WR	Write control line (Active low)	10	D1 (D9)	Data bit 1 (LB) or data bit 9 (HB)
A_1	Enable for D/A converter latch (Active low)	11	D0 (D8)/SI	Data bit 0 (LB) or data bit 8 (HB) Serial input when serial mode is selected
A_0	Enable for input latch (Active low)	12	DCOM	Digital common
D15 (MSB)	Data bit 15 (Most Significant Bit)	13	R_{F2}	Feedback resistor for internal or external operational amplifier Connect to pin 14 when a 10V output range is desired Leave open for a 20V output range
D14	Data bit 14	14	V_{OUT} R_{F1} (DAC708)	Voltage output for DAC709 or feedback resistor for use with an external output op amp for the DAC708 Refer to Connection Diagram for connection of external op amp to DAC708
D13	Data bit 13	15	ACOM	Analog common
D12	Data bit 12	16	SJ (DAC709) I_{OUT} (DAC708)	Summing junction of the internal output op amp for the DAC709, or the current output for the DAC708 Refer to Connection Diagram for connection of external op amp to DAC708
D11	Data bit 11	17	BPO	Bipolar offset Connect to pin 16 when operating in the bipolar mode Leave open for unipolar mode
D10	Data bit 10	18	GA	Gain adjust pin
D9	Data bit 9	19	$+V_{CC}$	Positive supply voltage (+15V)
D8	Data bit 8	20	$-V_{CC}$	Negative supply voltage (−15V)
D7	Data bit 7	21	CLR	Clear line. Sets the high and low byte input registers to zero and, for bipolar operation, sets the D/A register to the input code that gives bipolar zero on the D/A output (In the unipolar mode, invert the MSB prior to the D/A)
D6	Data bit 6	22	WR	Write control line
D5	Data bit 5	23	CS	Chip select control line
D4	Data bit 4	24	V_{DD}	Logic supply (+5V)
D3	Data bit 3	25	No pin	
D2	Data bit 2	26	No pin	(The DAC708 and DAC709 are in 24-pin packages)
D1	Data bit 1	27	No pin	
D0 (LSB)	Data bit 0 (Least Significant Bit)	28	No pin	

MECHANICAL

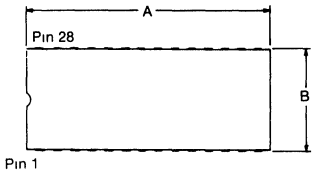
DAC708/709

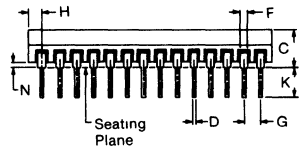




DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 190	1 210	30 23	30 73
B	580	600	14 73	15 24
C	140	185	3 56	4 70
D	016	020	0 41	0 51
F	030	050	0 76	1 27
G	100 BASIC		2 54 BASIC	
H	035	065	0 89	1 65
J	009	012	0 23	0 30
K	165	185	4 19	4 70
L	600 BASIC		15 24 BASIC	
N	040	060	1 02	1 52

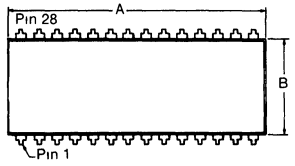
DAC705/706/707

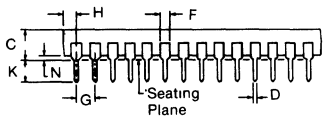




DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 386	1 465	35 20	37 21
B	610 BASIC		15 49 BASIC	
C	160	205	4 06	5 21
D	015	019	38	48
F	045	055	1 14	1 40
G	100 BASIC		2 54 BASIC	
H	035	095	89	2 41
J	009	012	23	30
K	155	195	3 94	4 05
L	600 BASIC		15 42 BASIC	
N	020	060	51	1 52

DAC707JP/KP

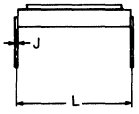


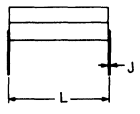


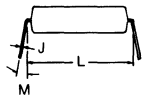
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 440	1 500	36 58	38 10
B	0 475	0 520	12 07	13 20
C	0 170	0 225	4 32	5 72
D	0 016	0 024	0 40	0 60
F	0 047	0 065	1 20	1 65
G	0 100 BASIC		2 54 BASIC	
H	0 050	0 100	1 27	2 54
J	0 008	0 014	0 20	0 35
K	0 130	0 154	3 30	3 90
L	0 600 BASIC		15 24 BASIC	
M	0°C	15°C	0°C	15°C
N	0 020	0 024	0 51	0 61

NOTE Leads in true position within 010" (25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers are not marked on package







ABSOLUTE MAXIMUM RATINGS

V_{DD} to COMMON ..... 0V, +15V
+V_{CC} to COMMON ..... 0V, +18V
−V_{CC} to COMMON ..... 0V, −18V
Digital Data Inputs to COMMON ..... −0 5V, V_{DD} +0.5
DC Current any Input ..... ±10mA
Reference Out to COMMON .. Indefinite Short to COMMON
V_{OUT} (DAC707, DAC709) ..... Indefinite Short to COMMON

External Voltage Applied to R_F (pin 1, DAC706; pin 13 or 14, DAC708) ..... ±18V
External Voltage Applied to D/A Output (pin 1, DAC707; pin 14, DAC708) ..... ±5V
Power Dissipation 1000mW
Storage Temperature ..... −60°C to +150°C
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.
Lead Temperature (Soldering, 10s) ..... 300°C

ORDERING INFORMATION

Model	Temperature Range	Input Configuration	Output Configuration
DAC705KH	0°C to +70°C	16-bit port	±5V output
DAC705KH-BI	0°C to +70°C	16-bit port	±5V output
DAC705BH	–25°C to +85°C	16-bit port	±5V output
DAC705BH-BI	–25°C to +85°C	16-bit port	±5V output
DAC705BH/QM	–25°C to +85°C	16-bit port	±5V output
DAC705SH	–55°C to +125°C	16-bit port	±5V output
DAC705SH-BI	–55°C to +125°C	16-bit port	±5V output
DAC705SH/QM	–55°C to +125°C	16-bit port	±5V output
DAC706KH	0°C to +70°C	16-bit port	±1mA output
DAC706KH-BI	0°C to +70°C	16-bit port	±1mA output
DAC706BH	–25°C to +85°C	16-bit port	±1mA output
DAC706BH-BI	–25°C to +85°C	16-bit port	±1mA output
DAC706BH/QM	–25°C to +85°C	16-bit port	±1mA output
DAC706SH	–55°C to +125°C	16-bit port	±1mA output
DAC706SH-BI	–55°C to +125°C	16-bit port	±1mA output
DAC706SH/QM	–55°C to +125°C	16-bit port	±1mA output
DAC707JP	0°C to +70°C	16-bit port	±10V output
DAC707JP-BI	0°C to +70°C	16-bit port	±10V output
DAC707KP	0°C to +70°C	16-bit port	±10V output
DAC707KP-BI	0°C to +70°C	16-bit port	±10V output
DAC707KH	0°C to +70°C	16-bit port	±10V output
DAC707KH-BI	0°C to +70°C	16-bit port	±10V output
DAC707BH	–25°C to +85°C	16-bit port	±10V output
DAC707BH-BI	–25°C to +85°C	16-bit port	±10V output
DAC707BH/QM	–25°C to +85°C	16-bit port	±10V output
DAC707SH	–55°C to +125°C	16-bit port	±10V output
DAC707SH-BI	–55°C to +125°C	16-bit port	±10V output
DAC707SH/QM	–55°C to +125°C	16-bit port	±10V output
DAC708KH	0°C to +70°C	8-bit port	±1mA output
DAC708KH-BI	0°C to +70°C	8-bit port	±1mA output
DAC708BH	–25°C to +85°C	8-bit port	±1mA output
DAC708BH-BI	–25°C to +85°C	8-bit port	±1mA output
DAC708BH/QM	–25°C to +85°C	8-bit port	±1mA output
DAC708SH	–55°C to +125°C	8-bit port	±1mA output
DAC708SH-BI	–55°C to +125°C	8-bit port	±1mA output
DAC708SH/QM	–55°C to +125°C	8-bit port	±1mA output
DAC709KH	0°C to +70°C	8-bit port	±10V output
DAC709KH-BI	0°C to +70°C	8-bit port	±10V output
DAC709BH	–25°C to +85°C	8-bit port	±10V output
DAC709BH-BI	–25°C to +85°C	8-bit port	±10V output
DAC709BH/QM	–25°C to +85°C	8-bit port	±10V output
DAC709SH	–55°C to +125°C	8-bit port	±10V output
DAC709SH-BI	–55°C to +125°C	8-bit port	±10V output
DAC709SH/QM	–55°C to +125°C	8-bit port	±10V output

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

For bipolar operation, the DAC705/706/707/708/709 accept positive-true binary two's complement input code. For unipolar operation (DAC708/709 only) the input code is positive-true straight-binary provided that the MSB input is inverted with an external inverter. See Table I.

TABLE I. Digital Input Codes.

Digital Input Codes	Analog Output	
	Unipolar Straight Binary[1] (DAC708/709 only, connected for Unipolar operation)	Binary Two's Complement (Bipolar operation; all models)
$7FFF_H$	+1/2 Full Scale −1 LSB[2]	+Full Scale
0000_H	Zero	Zero
$FFFF_H$	+Full Scale	−1LSB
8000_H	+1/2 Full Scale	−Full Scale

(1) MSB must be inverted externally (2) Assumes MSB is inverted externally

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (−Full Scale point and +Full Scale point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output when the input changes from one adjacent code to the next. A differential linearity error specification of ±1/2LSB means that the output step size can be between 1/2LSB and 3/2LSB when the input changes between adjacent codes. A negative DLE specification of −1LSB maximum (−0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC705/706/707/708/709 are specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by: (1) testing the end point differences at t_{min}, +25°C and t_{max}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Zero Drift

Zero drift is a measure of the change in the output with 0000_H applied to the D/A converter inputs over the specified temperature range. (For the DAC708/709 in unipolar mode, the MSB must be inverted.) This code corresponds to zero volts (DAC705/707 and DAC709) or zero milliamps (DAC706 and DAC708) at the analog output. The maximum change in offset at t_{min} or t_{max} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in FSR/°C.

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

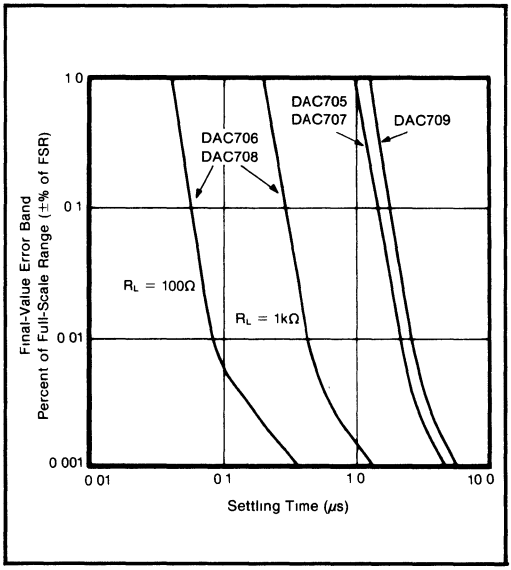


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2 LSB for 14 bits) for two input conditions: a full-scale range change of 20V (±10V) or 10V (±5V or 0 to 10V) and a 1LSB change at the "major carry", the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next.)

Current Output

Settling times are specified to±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

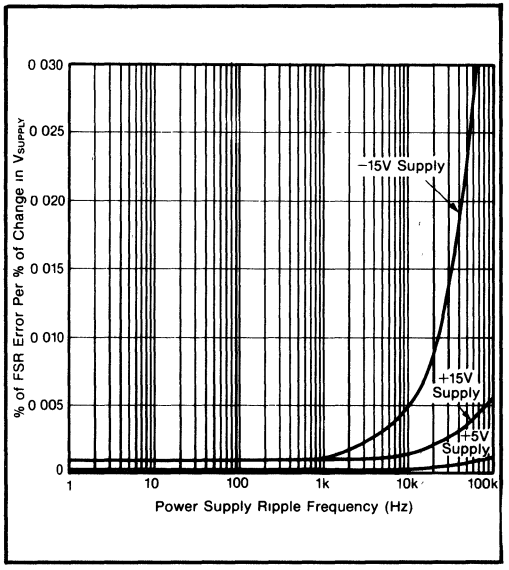


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1μF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ resistor. A 0.001μF to 0.01μF ceramic capacitor should be connected from GAIN ADJUST to ANALOG COMMON to prevent noise pickup. Refer to Figures 4 and 5 for the relationship of zero and gain adjustments to unipolar D/A converters.

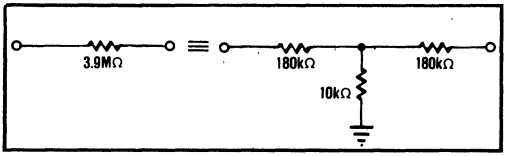


FIGURE 3. Equivalent Resistances.

Zero Adjustment

For unipolar (USB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (BTC) configurations, apply the digital input code that produces zero output voltage or current. See Table II for corresponding codes and connection diagrams for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

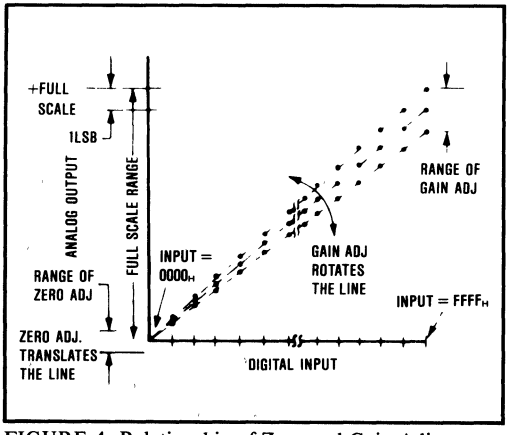


FIGURE 4. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters, DAC708 and DAC709.

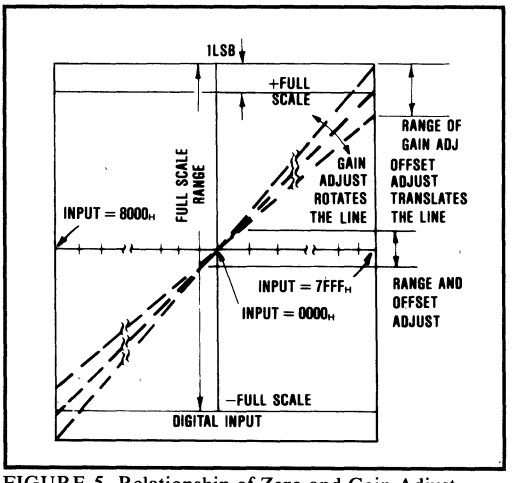


FIGURE 5. Relationship of Zero and Gain Adjustments for Bipolar D/A Converters, DAC705/706/707 and DAC708/709.

TABLE II. Digital Input And Analog Output Voltage/Current Relationships.

VOLTAGE OUTPUT MODELS												
Digital Input Code	Analog Output *Unipolar, 0 to +10V			Units	Digital Input Code	Analog Output Bipolar, ±10V			Analog Output Bipolar, ±5V			Units
	16-Bit	15-Bit	14-Bit			16-Bit	15-Bit	14-Bit	16-Bit	15-Bit	14-Bit	
One LSB	153	305	610	μV	One LSB	305	610	1224	153	305	610	μV
$FFFF_H$	+9 99985	+9 99969	+9 99939	V	$7FFF_H$	+9 99960	+9 99939	+9 99878	+4 99980	+4 99970	+4 99939	V
0000_H	0	0	0	V	8000_H	−10 0000	−10.0000	−10 0000	−5 0000	−5 0000	−5 0000	V

CURRENT OUTPUT MODELS									
Digital Input Code	Analog Output *Unipolar, 0 to −2mA			Units	Digital Input Code	Analog Output Bipolar, ±1mA			Units
	16-Bit	15-Bit	14-Bit			16-Bit	15-Bit	14-Bit	
One LSB	0 031	0 061	0 122	μA	One LSB	0 031	0 061	0 122	μA
$FFFF_H$	−1 99997	−1 99994	−1 99988	mA	$7FFF_H$	−0 99997	−0 99994	−0 99988	mA
0000_H	0	0	0	mA	8000_H	+1 00000	+1 00000	+1 00000	mA

*MSB assumed to be inverted externally

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages and the Connection Diagrams for gain adjustment circuit connections.

INTERFACE LOGIC AND TIMING

DAC708/709

The signals CHIP SELECT ($\overline{CS}$), WRITE ($\overline{WR}$), register enables ($\overline{A_0}$, $\overline{A_1}$, and $\overline{A_2}$) and CLEAR ($\overline{CLR}$), provide the control functions for the microprocessor interface. They are all active in the "low" or logic "0" state. $\overline{CS}$ must be low to access any of the registers. $\overline{A_0}$ and $\overline{A_1}$ steer the input 8-bit data byte to the low- or high-byte input latch respectively. $\overline{A_2}$ gates the contents of the two input latches through to the D/A latch in parallel. The contents are then applied to the input of the D/A converter. When $\overline{WR}$ goes low, data is strobed into the latch or latches which have been enabled.

The serial input mode is activated when both $\overline{A_0}$ and $\overline{A_1}$ are logic "0" simultaneously. The D0 (D8)/SI input data line accepts the serial data MSB first. Each bit is clocked in by a $\overline{WR}$ pulse. Data is strobed through to the D/A latch by $\overline{A_2}$ going to logic "0" the same as in the parallel input mode.

Each of the latches can be made "transparent" by maintaining its enable signal at logic "0". However, as stated above, when both $\overline{A_0}$ and $\overline{A_1}$ are logic "0" at the same time, the serial mode is selected.

The $\overline{CLR}$ line resets both input latches to all zeros and sets the D/A latch to 0000_H. This is the binary code that gives a null, or zero, at the output of the D/A in the bipolar mode. In the unipolar mode, activating $\overline{CLR}$ will cause the output to go to one-half of full scale.

The maximum clock rate of the latches is 10MHz. The minimum time between write (WR) pulses for successive enables is 20ns. In the serial input mode (DAC708 and DAC709), the maximum rate at which data can be clocked into the input shift register is 10MHz.

The timing of the control signals is given in Figure 6.

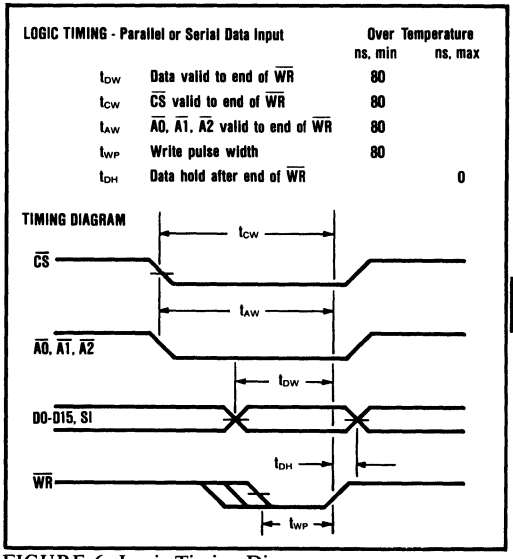


FIGURE 6. Logic Timing Diagram.

DAC706/707

The DAC705/706/707 interface timing is the same as that described above except instead of two 8-bit separately-enabled input latches, it has a single 16-bit input latch enabled by $\overline{A_0}$. The D/A latch is enabled by $\overline{A_1}$. Also, there is no serial-input mode and no CHIP $\overline{SELECT}$ ($\overline{CS}$) line.

INSTALLATION CONSIDERATIONS

Due to the extremely-high accuracy of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms

of a system layout, the resistance of typical 1 ounce copper-clad printed circuit board material is approximately 1/2mΩ per square. In the example above, a 10 milliinch-wide conductor 60 milliinches long would cause a 1LSB error.

In Figures 7 and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed with gain calibration. R_3 is part of R_L if the output voltage is sensed at ANALOG COMMON.

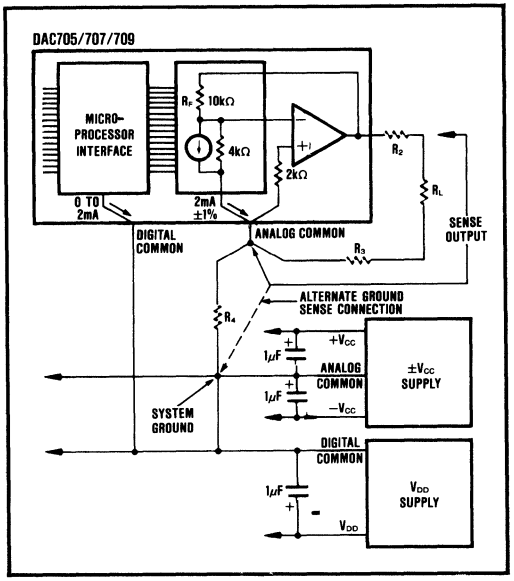


FIGURE 7. DAC705/707/709 Bipolar Output Circuit (Voltage Out).

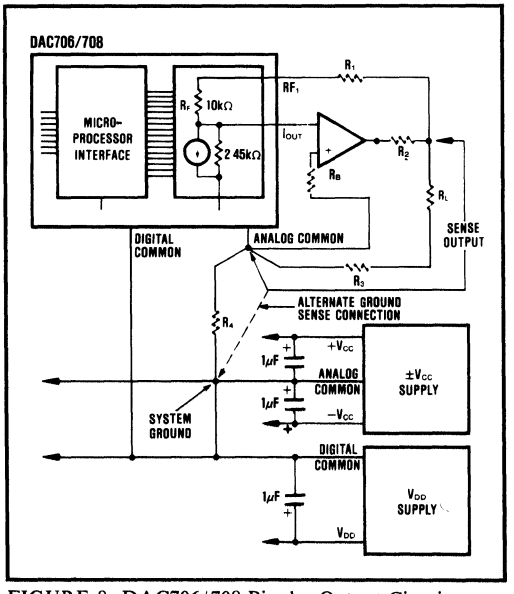


FIGURE 8. DAC706/708 Bipolar Output Circuit (with External Op Amp).

Figures 8 and 9 show two methods of connecting the currrent output model with an external precision output op amp. By sensing the output voltage at the load resistor (connecting R_F to the output of the amplifier at R_L) the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

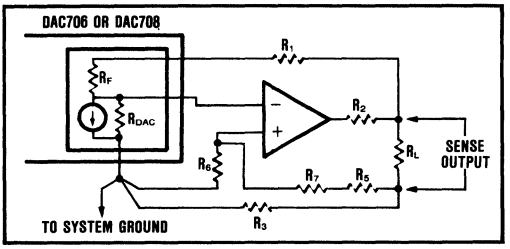


FIGURE 9. Alternate Connection for Ground Sensing at the Load (Current Output Models).

In many applications it is impractical to sense the output voltage at ANALOG COMMON. Sensing the output voltage at the system ground point is permissible because these converters have separate analog and digital common lines and the analog return current is a near-constant 2mA and varies by only 10μA to 20μA over the entire input code range. R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 is constant and appears as a zero error that can be nulled with the zero calibration adjustment.

Another approach senses the output at the load as shown in Figure 9. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection across R_L. The effect of R_4 is negligible as explained previously.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small flux-capture cross section for any external field.

BURN-IN SCREENING

Burn-in screening is an option available for the entire DAC705 through DAC709 family of products. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

Model	Temp. Range	Burn-In Screening
DAC705KH-BI	0°C to +70°C	160 hours at 85°C
DAC705BH-BI	−25°C to +85°C	160 hours at 85°C
DAC705SH-BI	−55°C to +125°C	160 hours at 125°C

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model.

ENVIRONMENTAL SCREENING

/QM Screening

All BH and SH models are available with Burr-Brown's /QM environmental screening for enhanced reliability. The screening, tabulated below, is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified below. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

SCREENING FLOW FOR /QM MODELS

Screen	MIL-STD-883 Method	Condition	Comments
Internal Visual	2017	B	
High Temperature Storage (Stabilization Bake)	1008	C	+150°C, 24hrs
Temperature Cycling	1010	C	−65 to +150°C, 10 cycles
Burn-in	1015	B	+125°C, 160hrs
Constant Acceleration	2001		
28-pin pkg		B	10,000G
24-pin pkg		E	30,000G
Hermeticity			
Fine Leak	1014	A1 or A2	
28-pin pkg			2×10^{-7} atmcc/sec
24-pin pkg			5×10^{-8} atmcc/sec
Gross Leak	1014	C	60psig, 2hr
External Visual	2009		

APPLICATIONS

LOADING THE DAC709 SERIALLY ACROSS AN ISOLATION BARRIER

A very useful application of the DAC709 is in achieving low-cost isolation that preserves high accuracy. Using the serial input feature of the input register pair, only three signal lines need to be isolated. The data is applied to pin 11 in a serial bit stream, MSB first. The WR input is used as a data strobe, clocking in each data bit. A RESET signal is provided for system startup and reset. These three signals are each optically isolated. Once the 16 bits of serial data have been strobed into the input register pair, the data is strobed through to the D/A register by the "carry" signal out of a 4-bit binary synchronous counter that has counted the 16 WR pulses used to clock in the data. The circuit diagram is given in Figure 10.

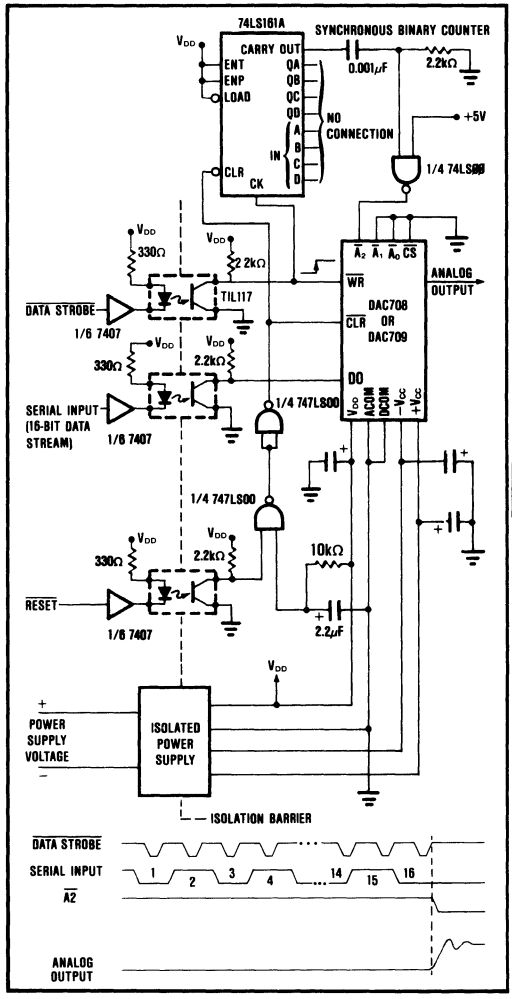


FIGURE 10. Serial Loading of Electrically Isolated DAC708/709.

CONNECTING MULTIPLE DAC707s TO A 16-BIT MICROPROCESSOR BUS

Figure 11 illustrates the method of connecting multiple DAC707s to a 16-bit microprocessor bus. The circuit shown has two DAC707s and uses only one address line to select either the input register or the D/A register. An external address decoder selects tne desired converter.

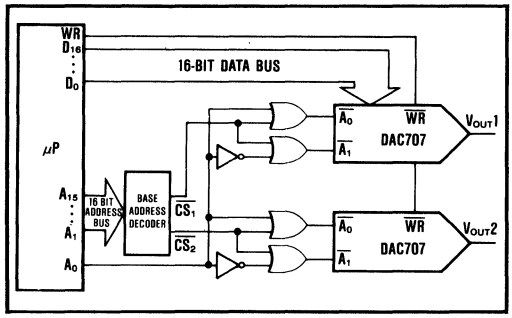


FIGURE 11. Connecting Multiple DAC707s to a 16-Bit Microprocessor.

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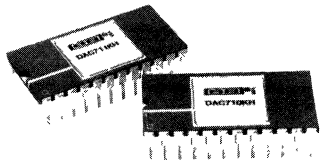


DAC710
DAC711

Monolithic 16-Bit
ROBOTICS DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- DESIGNED SPECIFICALLY FOR CLOSED-LOOP SERVO-CONTROL APPLICATIONS
- MONOTONIC TO 15 BITS OVER TEMPERATURE
- MONOLITHIC CONSTRUCTION
- V_{OUT} AND I_{OUT} MODELS
- PIN-COMPATIBLE WITH DAC702, DAC703
- VERY-LOW COST FOR MULTIPLE-CHANNEL APPLICATIONS

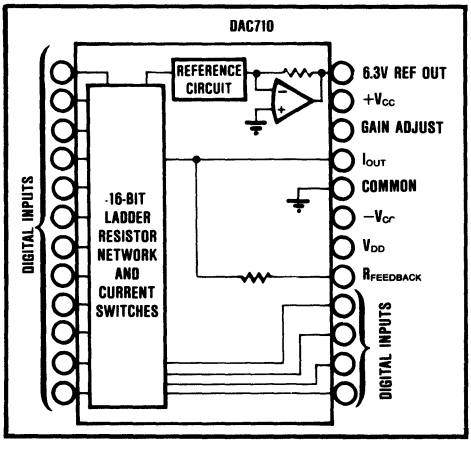
DESCRIPTION

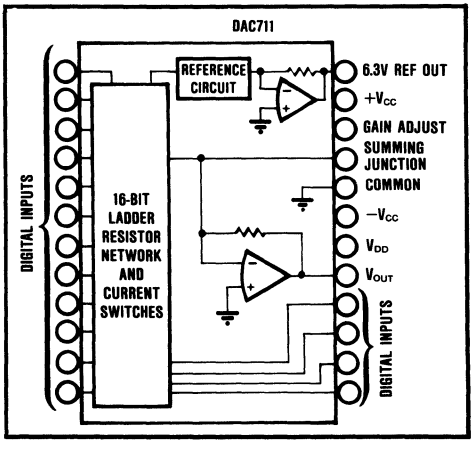
Robotics, numerical controllers, and other applications that involve the driving of servomotors require D/A converters that have very-good differential linearity around the zero output point. The DAC710KH (current output) and DAC711KH (voltage output) have been optimized for this characteristic.

DAC710 and DAC711 are complete 16-bit D/A converters on one chip. They include a precision buried-zener voltage reference, a fast settling operational amplifier (DAC711 only) as well as the D/A converter circuits. A combination of current switch design techniques accomplishes a guaranteed monotonicity of 15 bits around Bipolar Zero over the entire specification temperature range, 0°C to +70°C.

Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C-, and 54/74HC-compatible over the entire temperature range. Outputs are ±10V for the DAC711KH and ±1mA for the DAC710KH.

This D/A family is pin-compatible with the voltage and current output DAC703 and DAC702 model families. These D/A converters are packaged in 24-pin ceramic side-brazed packages that are hermetically sealed.





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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and rated power supplies and after 10 minutes of warm-up time unless otherwise noted

MODEL	DAC710KH/DAC711KH			UNITS
	MIN	TYP	MAX	
INPUT				
DIGITAL INPUT				
Resolution			16	Bits
Digital Inputs[1]: V_{IH}	+2 4		+V_{CC}	V
V_{IL}	−1 0		+0 8	V
I_{IH}, V_I = +2 7V			+40	μA
I_{IL}, V_I = +0 4V		−0 35	−0 5	mA
TRANSFER CHARACTERISTICS				
ACCURACY[2]				
Differential Linearity Error (near bipolar zero)[4][5]			+0 006, −0 003	% of FSR[3]
Monotonicity (near bipolar zero)[4]	15			Bits
Linearity Error			±0 0045	% of FSR
Gain Error[6]		±0 15	±0 30	%
Bipolar Zero Error[6][7]		±0 05	±0 1	% of FSR
DRIFT (over specification temperature range)				
Differential Linearity Error (near bipolar zero) over Temperature[4][5]			+0 009, −0 003	% of FSR
Monotonicity (near bipolar zero) over Temperature[4]	15			Bits
Linearity Error over Temperature			±0 009	% of FSR
Gain Drift		±25	±50	ppm/°C
Bipolar Zero Drift		±5	±12	ppm of FSR/°C
SETTLING TIME (to ±0 003% of FSR)[8]				
DAC711 (V_{OUT} Models)				
Full Scale Step (2kΩ load)		4	8	μsec
For 1LSB Step Change at Worst-Case Code[9]		2 5	4	μsec
Slew Rate		10		V/μsec
DAC710 (I_{OUT} Models)				
Full Scale Step (2mA) 10Ω to 100Ω load		350		nsec
1kΩ load		1		μsec
OUTPUT				
VOLTAGE OUTPUT				
DAC711		±10		V
Output Current	±5			mA
Output Impedance		0 15		Ω
Short Circuit to Common Duration		Indefinite		
CURRENT OUTPUT				
DAC710				
Output Range (±30% typ)		±1		mA
Output Impedance (±30% typ)		4 0		kΩ
Compliance	−2 5		+2 5	V
REFERENCE VOLTAGE				
Voltage		+6 3		V
Source Current Available for External Loads		+2 5		mA
Short Circuit to Common Duration		Indefinite		
POWER SUPPLY REQUIREMENTS				
Voltage +V_{CC}	+13 5	+15	+16 5	V
−V_{CC}	−13 5	−15	−16 5	V
V_{DD}	+4 5	+5	+16 5	V
Current (No Load)				
DAC711 (V_{OUT} Model): +V_{CC}		+16	+30	mA
−V_{CC}		−18	−30	mA
V_{DD}		+4	+8	mA
DAC710 (I_{OUT} Model) +V_{CC}		+10	+25	mA
−V_{CC}		−13	−25	mA
V_{DD}		+4	+8	mA
Power Dissipation (V_{DD} = +5 0V)[10]: DAC711		530	940	mW
DAC710		365	790	mW
Power Supply Rejection +V_{CC}		±0 003	±0 006	% of FSR/%V_{CC}
−V_{CC}		±0 003	±0.006	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001	% of FSR/%V_{DD}
TEMPERATURE RANGE				
Specification	0		+70	°C
Storage	−60		+150	°C

NOTES (1) Digital inputs are TTL-, LSTTL-, 54/74C-, 54/74HC-, and 54/74HTC-compatible over the operating voltage range of V_{DD} = +5V to +15V and over the specified temperature range The input switching threshold remains at the TTL threshold of 1 4V over the supply range of V_{DD} = +5V to +15V As logic "0" and logic "1" inputs vary over 0V to +0 8V and +2 4V to +10V, respectively, the change in the D/A converter output voltage will not exceed ±0 006% of FSR (2) DAC710KH is specified and tested with an external output operational amplifier using the internal feedback resistor in all parameters except settling time (3) FSR means Full Scale Range and is 20V for the DAC711KH and 2mA for the DAC710KH (4) This specification is for ±2048 consecutive codes around the bipolar zero code, that is, from $77FF_H$ to $87FF_H$ (5) ±0 003% of FSR is 1LSB for 15-bit resolution (6) Adjustable to zero with external trim potentiometer Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point (7) Error at input code $7FFF_H$, bipolar zero (8) Maximum represents the 3σ limit Not 100% tested for this parameter (9) At the major carry, $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$ (10) Power dissipation is an additional 40mW when V_{DD} is operated at +15V

ORDERING INFORMATION

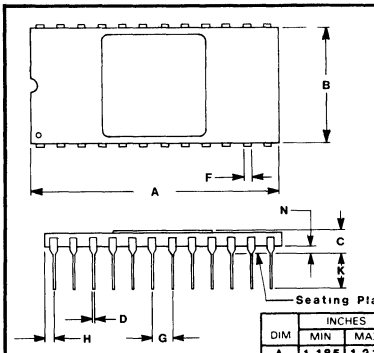
Model	Package	Temperature Range	Output
DAC710KH	Hermetic Ceramic	0°C to +70°C	Current, ±1mA
DAC711KH	Hermetic Ceramic	0°C to +70°C	Voltage
BURN-IN SCREENING OPTION See text for details			
Model	**Package**	**Temperature Range**	**Burn-In Temp. (160h)[1]**
DAC710KH-BI	Hermetic Ceramic	0°C to +70°C	85°C
DAC711KH-BI	Hermetic Ceramic	0°C to +70°C	85°C

NOTE (1) Or equivalent combination of time and temperature

PIN ASSIGNMENTS

Pin No.	Function DAC710	Function DAC711
1	Bit 1 (MSB)	Bit 1 (MSB)
2	Bit 2	Bit 2
3	Bit 3	Bit 3
4	Bit 4	Bit 4
5	Bit 5	Bit 5
6	Bit 6	Bit 6
7	Bit 7	Bit 7
8	Bit 8	Bit 8
9	Bit 9	Bit 9
10	Bit 10	Bit 10
11	Bit 11	Bit 11
12	Bit 12	Bit 12
13	Bit 13	Bit 13
14	Bit 14	Bit 14
15	Bit 15	Bit 15
16	Bit 16 (LSB)	Bit 16 (LSB)
17	$R_{FEEDBACK}$	V_{OUT}
18	V_{DD}	V_{DD}
19	$-V_{CC}$	$-V_{CC}$
20	Common	Common
21	I_{OUT}	Summing Junction (Zero Adjust)
22	Gain Adjust	Gain Adjust
23	$+V_{CC}$	$+V_{CC}$
24	+6 3V Ref Out	+6 3V Ref Out

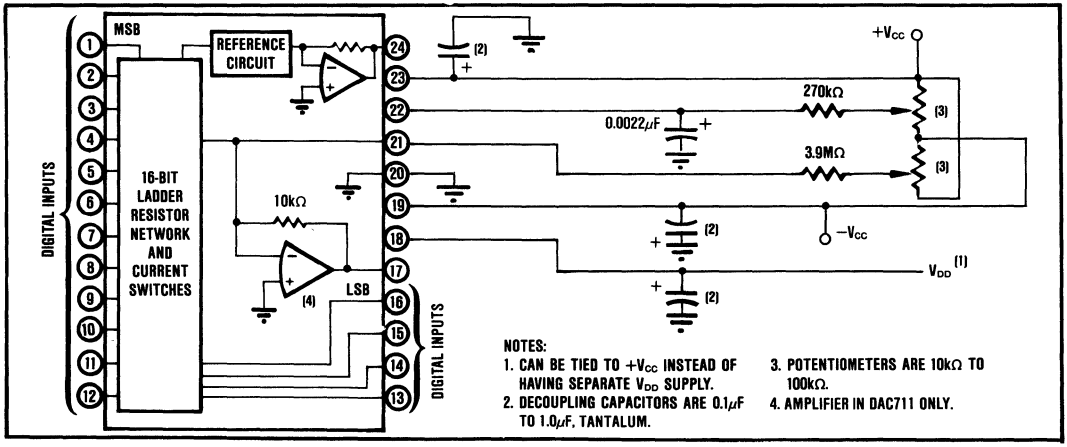
MECHANICAL



NOTE
Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.185	1.215	30.10	30.86
B	.600	.620	15.24	15.75
C	.125	.171	3.18	4.34
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	- -	10°	- -	10°
N	.025	.060	0.64	1.52

CONNECTION DIAGRAM



NOTES:
1. CAN BE TIED TO $+V_{CC}$ INSTEAD OF HAVING SEPARATE V_{DD} SUPPLY.
2. DECOUPLING CAPACITORS ARE 0.1μF TO 1.0μF, TANTALUM.
3. POTENTIOMETERS ARE 10kΩ TO 100kΩ.
4. AMPLIFIER IN DAC711 ONLY.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to Common ..... 0V to +18V
$+V_{CC}$ to Common ..... 0V to +18V
$-V_{CC}$ to Common ..... 0V to −18V
Digital Data Inputs (pins 1-16) to Common ..... −1V to +18V
Reference out (pin 24)
to Common ..... Indefinite Short to Common
External Voltage Applied to R_F (pin 21, DAC710KH) ..... ±18V
External Voltage Applied
to D/A Output (pin 17, DAC711KH) ..... −5V to +5V
V_{OUT} (pin 17, DAC711) ..... Indefinite Short to Common
Power Dissipation 1000mW
Storage Temperature ..... −60°C to +150°C
Lead Temperature (soldering, 10s) ..... 300°C

NOTE Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device Exposure to absolute maximum conditions for extended periods may affect device reliability

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC710/711KH accept complementary binary digital input codes in bipolar format. They may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

ACCURACY

Linearity

Linearity error is the deviation of the analog output from a straight line drawn through the end points (all bits ON point and all bits OFF point).

Differential Linearity

For servomotor control applications, differential linearity error (DLE) is one of the most important performance measures of a D/A converter. DLE is the deviation from an ideal 1LSB change in the output when the input changes from one adjacent code to the next. A differential linearity error specification of +0.006% of FSR maximum means that an output step size can be between 1LSB and 3LSB (at 15 bits) when the input changes between adjacent codes. A DLE specification of −0.003% maximum ensures 15-bit monotonicity.

Monotonicity

When a D/A converter is monotonic, the analog output increases or remains the same for an increasing input digital code. For ±2048 consecutive codes around bipolar zero, the DAC710KH and DAC711KH are monotonic to 15 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts-per-million per degree centigrade (ppm/°C). Gain drift is established by (1) testing the end point difference for each D/A at t_{min}, +25°C and t_{max} (2) calculating the gain error with respect to the +25°C value, and (3) dividing by the temperature change.

Zero Drift

Zero drift is a measure of the change in the output with $7FFF_H$ (bipolar zero) applied to the digital inputs. This code corresponds to 0V (DAC711KH) or 0mA (DAC710KH) at the analog output. The maximum change in offset at t_{min} or t_{max} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in parts-per-million of full-scale range per degree centigrade (ppm of FSR/°C).

TABLE I. Digital Input Codes.

Digital Input Codes	Analog Output	
	Complementary Offset Binary (COB)	* Complementary Two's Complement (CTC)
0000_H	+ Full Scale	−1LSB
$7FFF_H$	Bipolar Zero	− Full Scale
8000_H	−1LSB	+ Full Scale
$FFFF_H$	− Full Scale	Bipolar Zero

* Invert the MSB of the COB code with an external inverter to obtain CTC code.

SETTLING TIME

Settling time of the D/A is the total time required for the output to settle within an error band around its final value after a change in input. Refer to Figure 1 for typical values.

Voltage Output, DAC711KH

Settling times are specified to ±0.003% of FSR for two input conditions: a full-scale range change of 20V and a ±0.006% of FSR (±1LSB in 14 bits) change at the major carry, the point at which the worst-case setting time occurs.

Current Output, DAC710KH

Settling times are specified to ±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output while maintaining specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2).

REFERENCE SUPPLY

All models have an internal +6.3V reference voltage derived from an on-chip buried-zener diode. This reference voltage, available at pin 24, has a tolerance of ±5%. A minimum of 1.5mA is available for external loads. Gain and Zero adjustments should be made under constant load conditions.

If a varying load is to be driven by the reference supply, an external buffer amplifier is recommended to drive the load in order to isolate the bipolar offset (connected internally to the reference) from load variations.

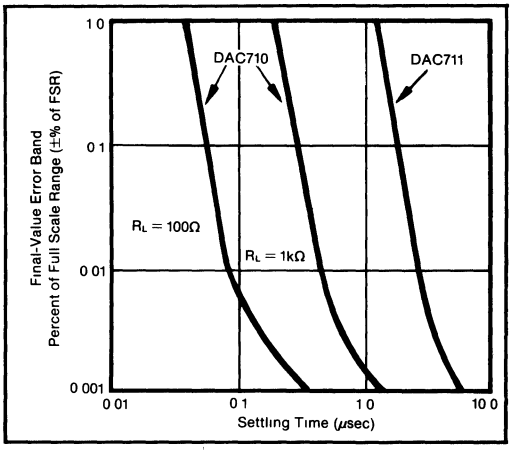


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

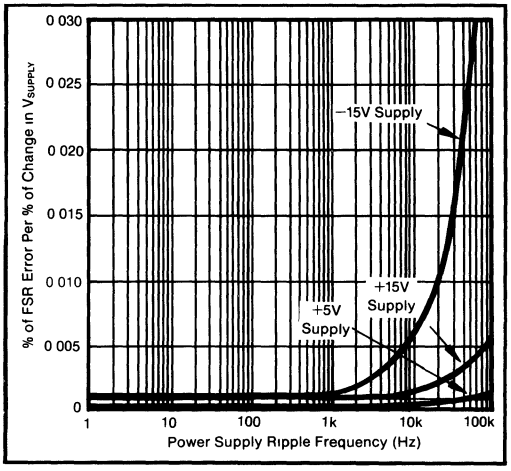


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. The 1μF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ part. A 0.001μF to 0.01μF ceramic capacitor should be connected (even if GAIN ADJUST is not used) from GAIN ADJUST (pin 22) to COMMON to prevent noise pickup. Refer to Figure 4 for the relationship of zero and gain adjustments.

Zero Adjustment

Apply the digital input code ($7FFF_H$) that produces zero output voltage or current. See Table II for corresponding codes and the Connection Diagram for zero adjustment circuit connections. Zero calibration should be made before Gain calibration.

Gain Adjustment

Apply the digital input code (0000_H) that gives the maximum positive output voltage or current. Adjust the gain potentiometer for this positive full-scale voltage or current. See Table II for positive full-scale values and the Connection Diagram for gain adjustment circuit connections.

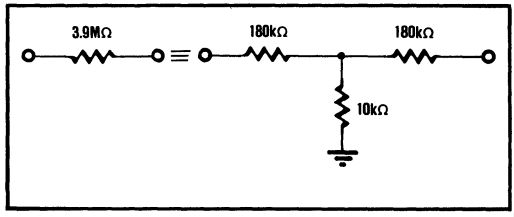


FIGURE 3. Equivalent Resistances.

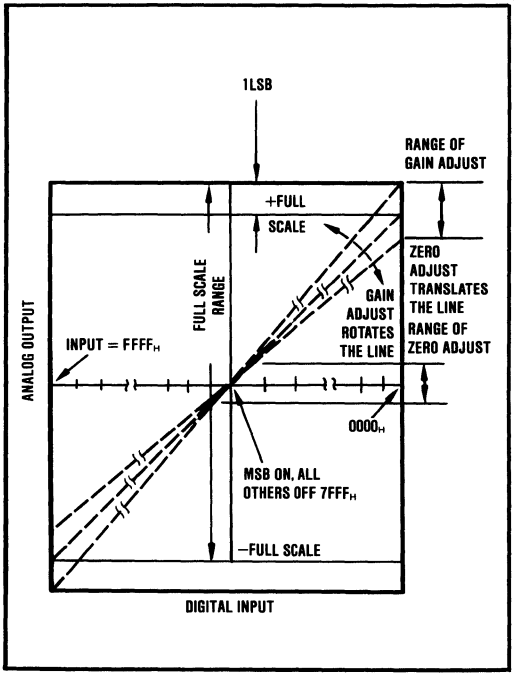


FIGURE 4. Relationship of Zero and Gain Adjustments.

TABLE II. Digital Input and Analog Output Relationships.

Digital Input Code	Analog Output							
	DAC710 Current Output				DAC711 Voltage Output			
	16-bit	15-bit	14-bit	Units	16-bit	15-bit	14-bit	Units
1LSB	0.031	0 061	0.122	μA	305	610	1224	μV
0000_H	−0 99997	−0 99994	−0.99988	mA	+9.99960	+9.99939	+9.99878	V
$7FFF_H$	0.00000	0 00000	0.00000	mA	0 00000	0 00000	0 00000	V
$FFFF_H$	+1 00000	+1 00000	+1.00000	mA	−10 0000	−10 0000	−10.0000	V

INSTALLATION CONSIDERATIONS

Due to the extremely high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Ignoring contact resistance, less than six inches of wire will produce a 1LSB error in the analog output voltage!

In Figures 5, 6, and 7, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance (R_L) is constant, R_2 simply introduces a gain error and can be removed during initial calibration. R_3 is part of R_L, if the output voltage is sensed at COMMON (pin 20), and therefore introduces no error. If R_L is variable, then R_2 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is 5kΩ, then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_4 is negligible.

In many applications it is impractical to sense the output voltage at pin 20. Sensing the output voltage at the system ground point is permissible with the DAC710/711 because the D/A converter is designed to have a constant return current of approximatley 2mA flowing from pin 20. The variation in this current is under 20μA (with changing input codes), therefore R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 ($R_4 \times 2mA$) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figures 5, 6, and 7.

Figures 6 and 7 show two methods of connecting the current output model (DAC710KH) with external precision output operational amplifiers. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A_1 at R_L), the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain. If the output cannot be sensed at COMMON (pin 20), or the system ground point as mentioned above, then the differential output circuit shown in Figure 7 is recommended. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible, the circuit of Figure 7 can be reduced to the one shown in Figure 6. Again, the effect of R_4 is negligible.

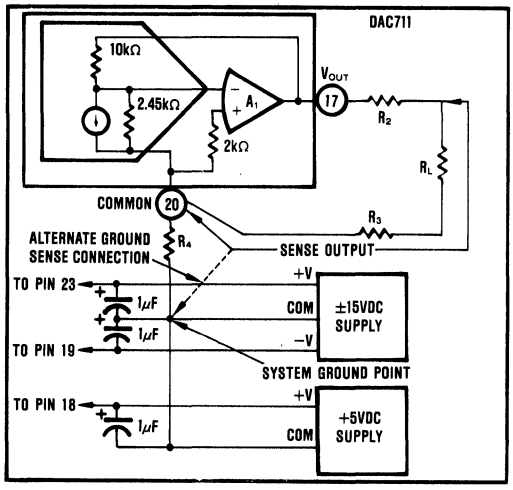


FIGURE 5. Output Circuit for DAC711.

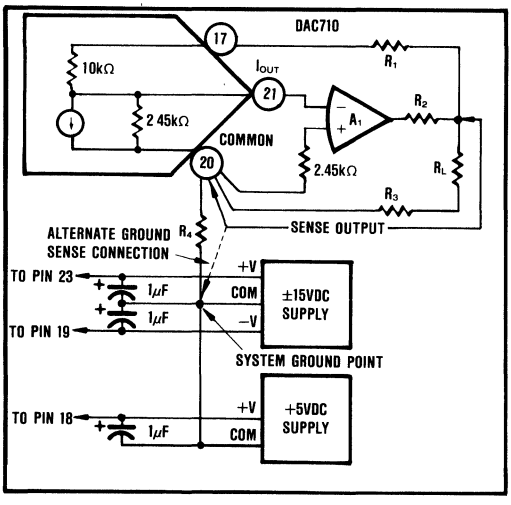


FIGURE 6. Preferred External Op Amp Configuration for DAC710.

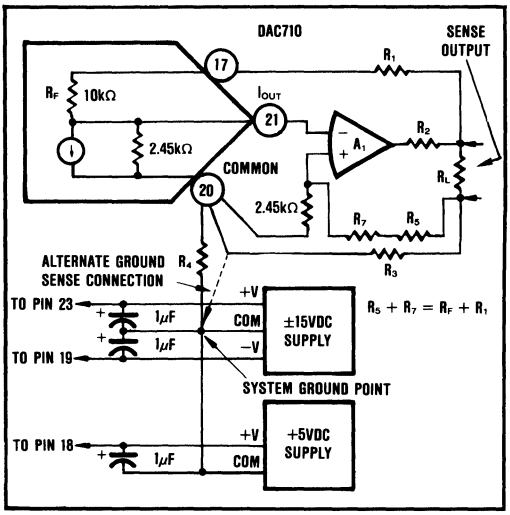


FIGURE 7. Differential Sensing Output Op Amp Configuration for DAC710.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation pickup is small loop area. If a signal lead and its return conductor are wired close together, they present a small flux-capture cross section for external fields.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT D/A'S

DAC710KH is a current output device and will drive the summing junction of an op amp to produce an output voltage as shown in Figure 8. Use of the internal feedback resistor (pin 17) is required to obtain specified gain accuracy and low gain drift.

DAC710KH can be scaled for any desired voltage range with an external feedback resistor at the expense of increased drift with temperature. The resistors in the DAC710KH ratio track to ±1ppm/°C but their absolute TCR may be as high as ±50ppm/°C.

An alternative method of scaling the output voltage of the D/A converter and preserving the low gain drift is shown in Figure 9.

OUTPUTS LARGER THAN 20V RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use an I_{OUT} value of ±1mA to calculate the output voltage range (see Figure 10). Use protection diodes as shown when a high voltage op amp is used.

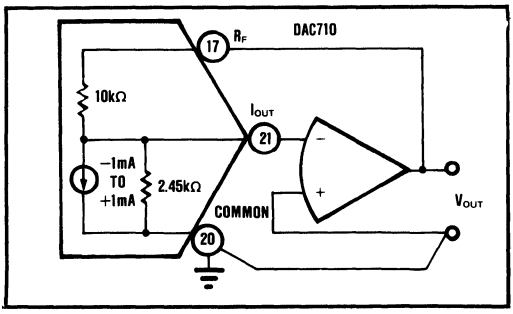


FIGURE 8. External Op Amp Using Internal Feedback Resistors (DAC710).

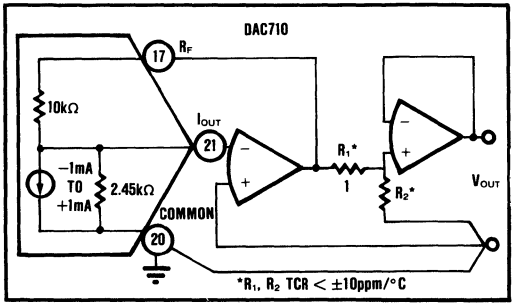


FIGURE 9. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift (DAC710).

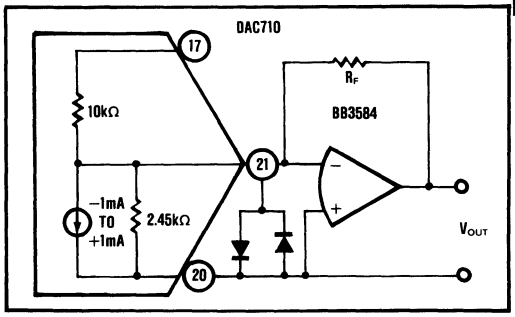


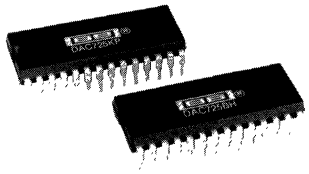
FIGURE 10. External Op Amp Using External Feedback Resistors (DAC710).

BURN-IN SCREENING

Burn-in screening is an option available for the entire DAC711 family of products. Burn-in duration is 160 hours at 85°C (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

BURR-BROWN®



DAC725

Dual 16-Bit DIGITAL-TO-ANALOG CONVERTER

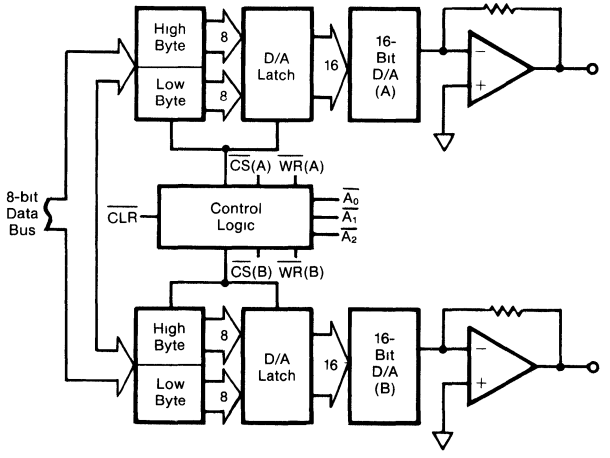
FEATURES

- COMPLETE DUAL V_{OUT} DAC
- DOUBLE-BUFFERED INPUT REGISTER
- HIGH-SPEED DATA INPUT (Serial or Parallel)
- HIGH ACCURACY (±0.003% Linearity Error)
- 14-BIT MONOTONICITY OVER TEMPERATURE
- PLASTIC AND CERAMIC PACKAGES
- CLEAR INPUT TO SET ZERO OUTPUT

DESCRIPTION

The DAC725 is a dual 16-bit DAC, complete with internal reference and output op amps. The DAC725 is designed to interface to an 8-bit microprocessor bus. The hybrid construction minimizes the digital feedthrough typically associated with products that combine the digital bus interface circuitry with high-accuracy analog circuitry.

The 16-bit data word is loaded into either of the DACs in two 8-bit bytes per 16-bit word. The versatility of the control lines allow the data word to be directed to either DAC, in any order. The voltage-out DACs are dedicated to a bipolar output voltage of ±10V. The output is immediately set to 0V when the Clear command is given. This feature, combined with the bus interfacing and complete DAC circuitry, makes the DAC725 ideal for automatic test equipment, power control, servo systems, and robotics applications.



International Airport Industrial Park - P.O Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-757A

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_{CC} = ±15V, V_{DD} = +5V, and after a 10-minute warm-up unless otherwise noted

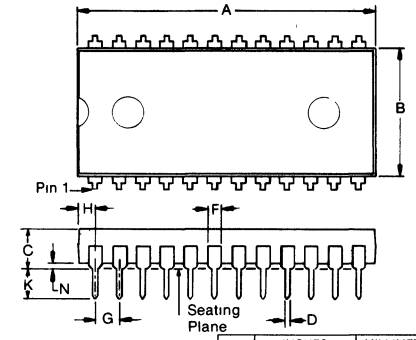
MODEL	DAC725JP, AH			DAC725KP, BH			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT							
DIGITAL INPUT							
Resolution			16			*	Bits
Bipolar Input Code		Binary Twos Complement			*		
Logic Levels[1] V_{IH}	+2 0		+5 5	*		*	V
V_{IL}	−1 0		+0 8	*		*	V
I_{IH} (V_I = +2 7V)			1			*	μA
I_{IL} (V_I = +0 4V)			1			*	μA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error		±0 003	±0 006		±0 0015	±0 003	% of FSR[2]
Differential Linearity Error[3]		±0 0045	±0 012		±0 003	±0 006	% of FSR
at Bipolar Zero[4]					±0 003	±0 006	% of FSR
Gain Error[5]		±0 07	±0 2		*	±0 15	%
Bipolar Zero Error[5]		±0 05	±0 1		*	*	% of FSR
Monotonicity Over Temperature Range	13			14			Bits
Power Supply Sensitivity ±V_{CC}		±0 0015	±0 006		*	*	% of FSR/%V_{CC}
V_{DD}		±0 0001	±0 001		*	*	% of FSR/%V_{DD}
DRIFT (Over Spec Temp Range)							
Gain Drift							
DAC725JP, KP		±10			*		ppm/°C
DAC725AH, BH		±10	±25		*	±15	ppm/°C
Bipolar Zero Drift							
DAC725JP, KP		±5			*		ppm of FSR/°C
DAC725AH, BH		±5	±15		*	±10	ppm of FSR/°C
Differential Linearity Error Over Temp[3]			±0 012			+0 009	% of FSR
						−0 006	% of FSR
Linearity Error Over Temp[3]			±0 012			±0 006	% of FSR
SETTLING TIME (to ±0 003% of FSR)[6]							
20V Step (2kΩ load)		4			*	8	μs
1LSB Step at Worst-Case Code[7]		2 5			*	4	μs
Slew Rate		10			*		V/μs
OUTPUT							
Output Voltage Range[8]	±10			*			V
Output Current	±5			*			mA
Output Impedance		0 15			*		Ω
Short Circuit to Common Duration		Indefinite			*		
POWER SUPPLY REQUIREMENTS							
Voltage +V_{CC}	+11 4	+15	+16 5	*	*	*	V
−V_{CC}	−11 4	−15	−16 5	*	*	*	V
V_{DD}	+4 5	+5	+5 5	*	*	*	V
Current (No load, ±15V supplies) +V_{CC}		+29	+35		*	*	mA
−V_{CC}		−35	−40		*	*	mA
V_{DD}		+6	+10		*	*	mA
Power Dissipation (±15V supplies)		920	1175		*	*	mW
TEMPERATURE RANGE							
Specification							
DAC725JP, KP	0		+70	*		*	°C
DAC725AH, BH	−25		+85	*		*	°C
Storage	−60		+150	*		*	°C

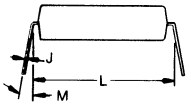
*Specification same as DAC725JP/AH except where listed separately

NOTES (1) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC and 54/74HTC compatible over the specification temperature range (2) FSR means Full-Scale Range For example, for ±10V output, FSR = 20V (3) ±0 0015% of FSR is equal to 1LSB in 16-bit resolution ±0 003% of FSR is equal to 1LSB in 15-bit resolution ±0 006% of FSR is equal to 1LSB in 14-bit resolution (4) Error at input code 0000_H (BTC) (5) Adjustable to zero with external trim potentiometer Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point (6) Maximum represents the 3σ limit Not tested for this parameter (7) The bipolar worst-case code change is $FFFF_H$ to 0000_H (BTC) (8) Minimum supply voltage for ±10V output swing is approximately ±13V Output swing for ±12V supplies is at least ±9V

MECHANICAL

P Package - 28-pin Plastic DIP

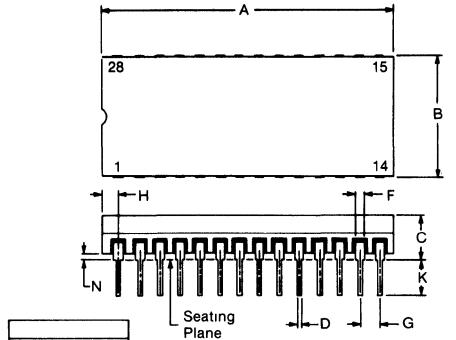


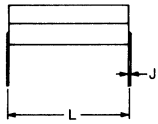


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 440	1 500	36 58	38 10
B	0 475	0 520	12 07	13 21
C	0 170	0 225	4 32	5 72
D	0 016	0 024	0 41	0 61
F	0 047	0 065	1 20	1 65
G	0 100 BASIC		2 54 BASIC	
H	0 050	0 100	1 27	2 54
J	0 008	0 014	0 20	0 36
K	0 130	0 154	3 30	3 91
L	0 600 BASIC		15 24 BASIC	
M	0°C	15°C	0°C	15°C
N	0 020	0 024	0 51	0 61

NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

H Package - 28-pin Ceramic



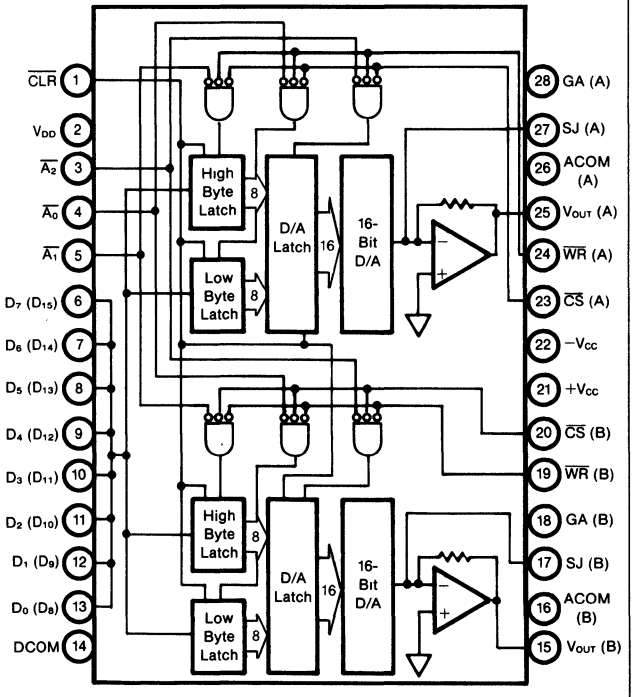


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 386	1 465	35 20	37 21
B	610 BASIC		15 49 BASIC	
C	160	205	4 06	5 21
D	015	019	38	48
F	045	055	1 14	1 40
G	100 BASIC		2 54 BASIC	
H	035	095	89	2 41
J	009	012	23	30
K	155	195	3 94	4 05
L	600 BASIC		15 42 BASIC	
N	020	060	51	1 52

NOTE Leads in true position within .010" (.25mm) R at MMC at seating plane

Pin numbers shown for reference only. Numbers are not marked on package

CONNECTION DIAGRAM



Pin	Designator	Description
1	$\overline{CLR}$	Clear line. Sets the D/A register to 0000 (hex), which gives bipolar zero on the D/A output
2	V_{DD}	Logic supply (+5V)
3	$\overline{A_2}$	Latch enable for D/A latch (active low)
4	$\overline{A_0}$	Latch enable for "low byte" input (active low)
5	$\overline{A_1}$	Latch enable for "high byte" input (active low)
6	D_7 (D_{15})	Input for data bit 7 if enabling low byte (LB) latch, or data bit 15 if enabling the high byte (HB) latch
7	D_6 (D_{14})	Input for data bit 6 if enabling LB latch, or data bit 14 if enabling HB latch
8	D_5 (D_{13})	Data bit 5 (LB) or data bit 13 (HB)
9	D_4 (D_{12})	Data bit 4 (LB) or data bit 12 (HB)
10	D_3 (D_{11})	Data bit 3 (LB) or data bit 11 (HB)
11	D_2 (D_{10})	Data bit 2 (LB) or data bit 10 (HB)
12	D_1 (D_9)	Data bit 1 (LB) or data bit 9 (HB)
13	D_0 (D_8)	Data bit 0 (LB) or data bit 8 (HB).
14	DCOM	Digital common
15	V_{OUT} (B)	Voltage output for DAC B
16	ACOM (B)	Analog common for DAC B
17	SJ (B)	Summing junction of the internal op amp for DAC B
18	GA (B)	Gain adjust pin for DAC B
19	$\overline{WR}$ (B)	Write control line for DAC B
20	$\overline{CS}$ (B)	Chip select control line for DAC B
21	$+V_{CC}$	Positive supply voltage (+15V)
22	$-V_{CC}$	Negative supply voltage (−15V)
23	$\overline{CS}$ (A)	Chip select control line for DAC A
24	$\overline{WR}$ (A)	Write control line for DAC A
25	V_{OUT} (A)	Voltage output for DAC A
26	ACOM (A)	Analog common for DAC A
27	SJ (A)	Summing junction of the internal op amp for DAC A
28	GA (A)	Gain adjust pin for DAC A

ABSOLUTE MAXIMUM RATINGS

V_{DD} to COMMON	0V, +15V
$+V_{CC}$ to COMMON	0V, +18V
$-V_{CC}$ to COMMON	0V, −18V
Digital Data Inputs to COMMON	−0 5V, V_{DD} +0 5
DC Current any Input	±10mA
Reference Out to COMMON	Indefinite Short to COMMON
V_{OUT}	Indefinite Short to COMMON
External Voltage Applied to R_F	±18V
External Voltage Applied to D/A Output	±5V
Power Dissipation	2000mW
Storage Temperature	−60°C to +150°C
Lead Temperature (soldering, 10s)	300°C

NOTE These devices are sensitive to electrostatic discharge Appropriate I C handling procedures should be followed

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device Exposure to absolute maximum conditions for extended periods may affect device reliability

ORDERING INFORMATION

Model	Package	Temperature Range
DAC725JP	Plastic DIP	0°C to +70°C
DAC725KP	Plastic DIP	0°C to +70°C
DAC725AH	Ceramic	-25°C to +85°C
DAC725BH	Ceramic	-25°C to +85°C

BURN-IN SCREENING OPTION
See text for details

Model	Package	Burn-In Temp. (160h)[1]
DAC725JP-BI	Plastic DIP	+70°C
DAC725KP-BI	Plastic DIP	+70°C
DAC725AH-BI	Ceramic	+85°C
DAC725BH-BI	Ceramic	+85°C

NOTE. (1) Or equivalent combination See text

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC725 accepts positive-true binary twos complement input code, as shown in Table I. The data is loaded into either DAC, 8 bits at a time. The data may also be clocked into the device in a serial format.

TABLE I. Digital Input Codes.

Digital Input Codes	Analog Output Binary Twos Complement (Bipolar Operation, All Models)
$7FFF_H$	+ Full Scale
0000_H	Zero
$FFFF_H$	− 1 LSB
8000_H	− Full Scale

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (minus full-scale point and plus full-scale point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output when the input changes from one adjacent code to the next. A differential linearity error specification of ±1/2LSB means that the output step size can be between 1/2LSB and 3/2LSB when the input changes between adjacent codes. A negative DLE specification of −1LSB maximum (−0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC725 is specified to be monotonic to 14 bits over the entire specification range.

BURN-IN SCREENING

Burn-in screening is an option available for both the plastic and ceramic packaged DAC725. Burn-in duration is 160 hours at the temperatures listed below, or at an equivalent combination of time and temperature according to the Arrhenius equation using 1eV activation energy.

Plastic "-BI"models: +70°C
Ceramic "-BI" models: +85°C

In order to limit the juction temperature of the internal semiconductor devices below the Absolute Maximum Rating, the burn-in temperatures should be as shown. All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by:

(1) testing the end point differences at t_{MIN}, +25°C and t_{MAX},
(2) calculating the gain error with respect to the +25°C value, and
(3) dividing by the temperature change.

The DAC725 is specified for Maximum Gain and Offset values at temperature. This tells the system designer the maximum that can be expected over temperature, regardless of room temperature values.

Zero Drift

Zero drift is a measure of change in the output with 0000_H applied to the D/A converter inputs over the specified temperature range. This code corresponds to zero volts analog output.

The maximum change in offset at t_{MIN} or t_{MAX} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in FSR/°C.

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its

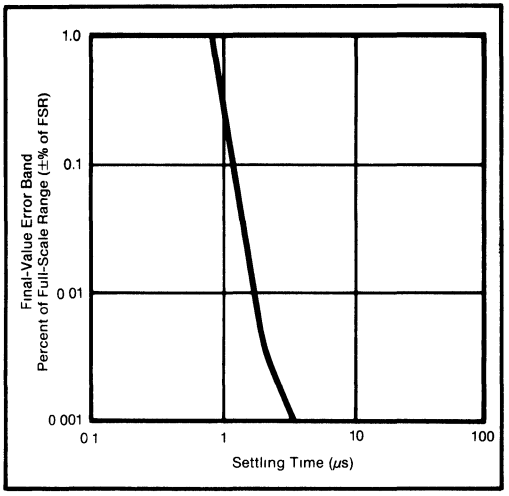


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

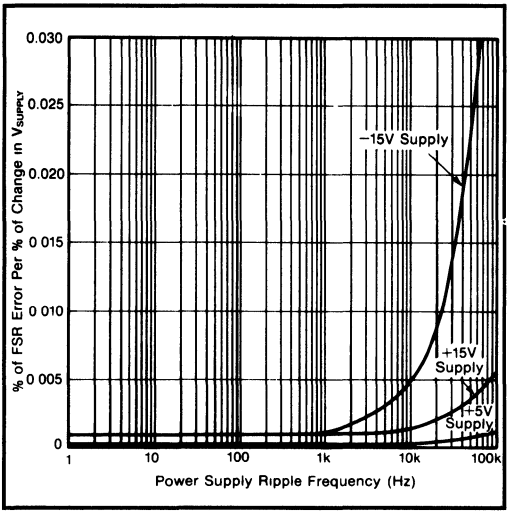


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

Settling times are specified to ±0.003% of FSR (±1/2LSB for 14 bits) for two input conditions: a full-scale range change of 20V (±10V), and a 1LSB change at the "major carry," the point at which the worst-case settling time occurs. This is the worst-case point since all of the input bits change when going from one code to the next.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1μF to 10μF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ resistor. A 0.001μF to 0.01μF low-leakage film capacitor should be connected from Gain Adjust to Analog Common to prevent noise pickup. Refer to Figure 4 for relationship of Offset and Gain adjustments.

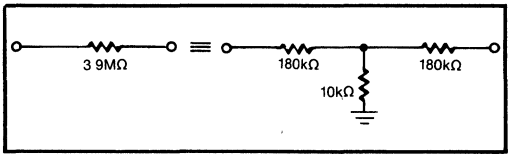


FIGURE 3. Equivalent Resistances.

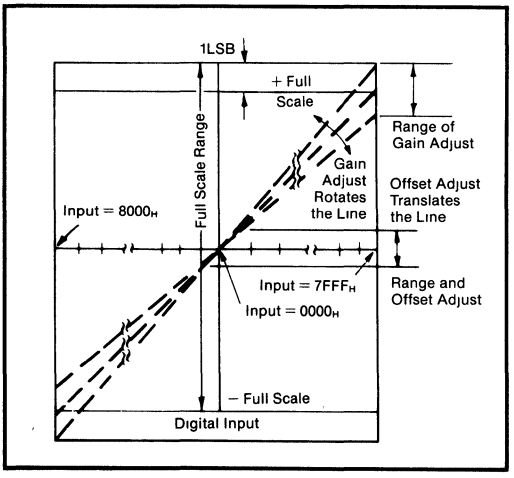


FIGURE 4. Relationship of Zero and Gain Adjustments for the DAC725.

Zero Adjustment

By loading the code 0000_H, the DAC will force zero volts. Offset is adjusted by using the circuit of Figure 5. An alternate method would be to use the $\overline{CLR}$ control to set the DAC to zero volts. Zero calibration should be made before gain calibration.

Gain Adjustment

To adjust the gain of the DAC725, set the DAC to $7FFF_H$ for both DACs. Adjust the gain of each DAC to obtain the full scale voltage of +9.99969V as shown in Table II.

TABLE II. Digital Input and Analog Output Voltages.

Digital Input Code	Bipolar, ±10V			Units
	16 Bits	15 Bits	14 Bits	
One LSB	305	610	1224	μV
$7FFF_H$	+9 99969	+9 99939	+9 99878	V
8000_H	−10 0000	−10 0000	−10 0000	V

INTERFACE LOGIC AND TIMING

The control logic functions are chip select ($\overline{CS}$[A] or $\overline{CS}$[B]), write ($\overline{WR}$[A] or $\overline{WR}$[B]), latch enable ($\overline{A_0}$, $\overline{A_1}$, $\overline{A_2}$), and clear ($\overline{CLR}$). These pins provide the control functions for the microprocessor interface. There is a write and a chip select for both DAC A and for DAC B channels. This allows the 8-bit data word to be latched from the data bus to the input latch or from the input latch to the DAC latch, of DAC A, DAC B, or both.

The latch enable lines control which latch is being loaded. Line $\overline{A_1}$ in combination with $\overline{WR}$ and $\overline{CS}$ enables the high byte of the DAC channel to be latched through the byte latch. The $\overline{A_0}$ line in conjunction with the $\overline{WR}$ and $\overline{CS}$, latches the data for the low byte. When $\overline{A_2}$, $\overline{CS}$, $\overline{WR}$ are low at the same time, the data is latched through the D/A latch and the DAC changes output voltage. Each latch may be made transparent by maintaining its enable signal at logic "0".

The serial data mode is activated when both the $\overline{A_0}$ and $\overline{A_1}$ are at logic low simultaneously. The data (MSB first) is clocked in to pin 13 with clock pulses on the $\overline{WR}$ pin. The data is then latched through to the DAC as a complete 16-bit word selected by $\overline{A_2}$.

TABLE III. Truth Table of Data Transfers.

$\overline{A_0}$	$\overline{A_1}$	$\overline{A_2}$	$\overline{WR}$(A)	$\overline{CS}$(A)	
1	1	0	0	0	DAC latch enabled, Channel A
1	0	1	0	0	Input latch high byte enabled, Channel A
1	0	0	0	0	High byte flows through to DAC, Channel A
0	1	1	0	0	Low byte latched from data bus, Channel A
0	1	0	0	0	Low byte flows through to DAC, Channel A
0	0	1	1	1	Serial input mode for byte latches
X	X	X	1	0	No data is latched
X	X	X	0	1	No data is latched
"1" or "0" indicates TTL Logic Level Channel A shown					

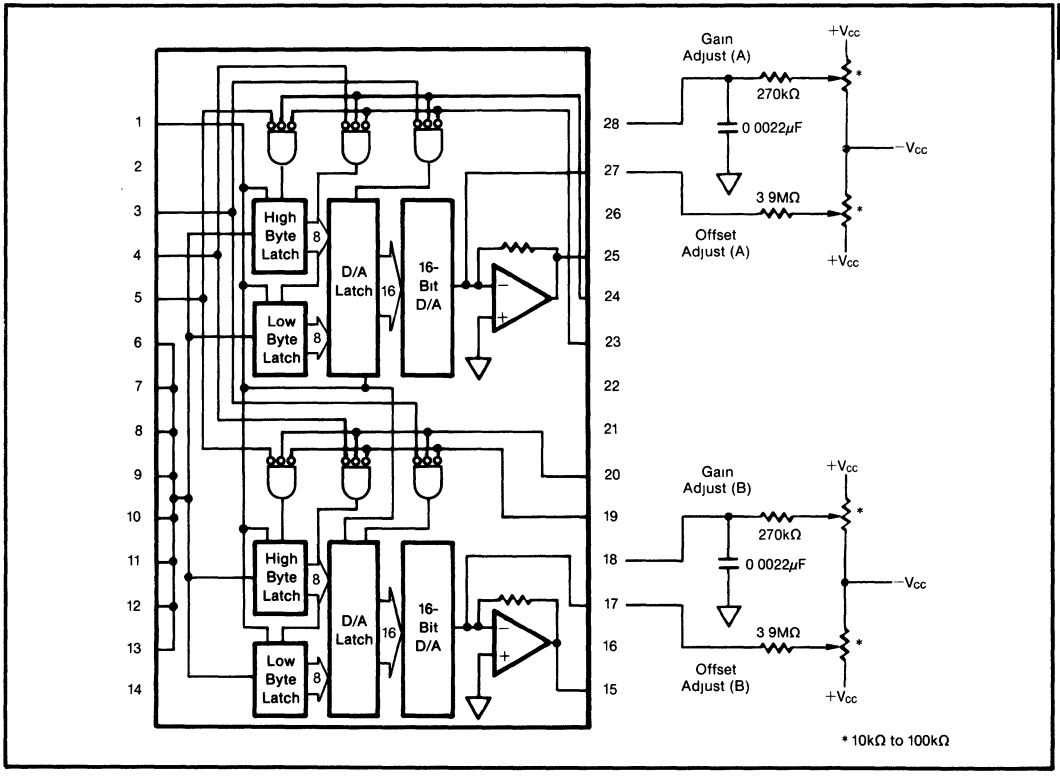


FIGURE 5. Connections for Gain and Offset Adjust.

The $\overline{CLR}$ line resets both input latches to all zeros and sets the DAC latch to 0000_H. This is the binary code that gives a null, or zero, at the output of the DAC.

The maximum clock rate of the latches is 10MHz. The minimum time between the write ($\overline{WR}$) pulses for successive enables is 20ns. In the serial input mode, the maximum rate at which data can be clocked into the input shift register is 10MHz. The timing of the control signals is given in Figure 6.

Logic Timing—Parallel or Serial Data Input

		Over Temperature	
		ns, min	ns, max
t_{DW}	Data valid to end of $\overline{WR}$	80	
t_{CW}	$\overline{CS}$ valid to end of $\overline{WR}$	80	
t_{AW}	$\overline{A_0}$, $\overline{A_1}$, $\overline{A_2}$ valid to end of $\overline{WR}$	80	
t_{WP}	Write pulse width	80	
t_{DH}	Data hold after end of $\overline{WR}$		0

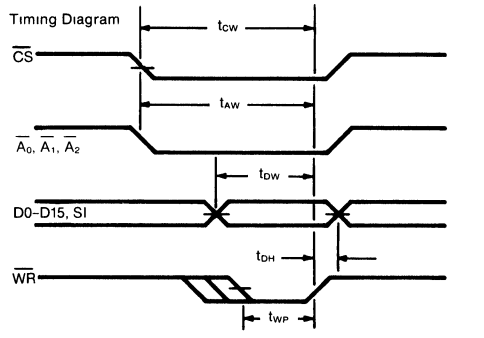


FIGURE 6. Logic Timing Diagram.

INSTALLATION CONSIDERATIONS

Because of the extremely high accuracy of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of typical 1 ounce copper-clad printed circuit board material is approximately 1/2mΩ per square. In the example above, a 10 milliinch-wide conductor 60 milliinches long would cause a 1LSB error in R_2 and R_3 of Figure 7.

In Figure 7, lead and contact resistances are represented as R_2 through R_6. As long as the load resistance (R_L) remains constant, the resistances R_2 and R_3 will appear as gain errors when the output is sensed across the load. If the output is sensed at the DAC725 output terminal and the system analog common, R_2 and R_3 appear in series with R_L. R_4 has a current through it that varies by only 1% of the nominal 2mA current for all code

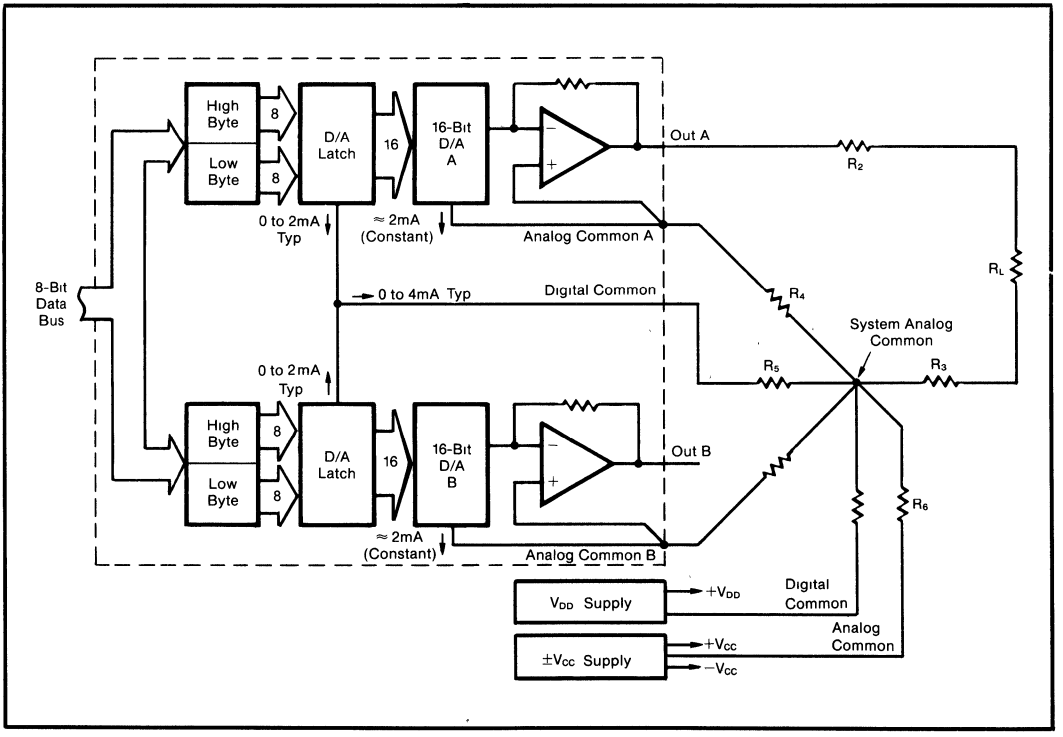


FIGURE 7. System Wiring Example.

combinations. This IR drop causes an offset error, and is calibrated out as an offset error.

The current through the digital common varies directly with the digital code that is loaded into the DAC. The current is not the same for each code. If this IR drop is allowed to modulate the analog common, there may be code-dependent errors in the analog output.

The IR drop across R_6 may cause accuracy problems if the analog commons of several circuits are "daisey chained" along the power supply analog common. All analog sense lines should be referenced to the system analog common.

APPLICATIONS

WAVEFORM GENERATION

The DAC725 has attributes that make it ideal for very low distortion waveform synthesis. Due to special design techniques, the feedthrough energy is much lower than that found in other D/A converters available today. In addition to the low feedthrough glitch energy, the input logic will operate with data rates of 10MHz. This makes the DAC725 ideal for waveform synthesis.

PROGRAMMABLE POWER SUPPLIES

The DAC725 is an excellent choice for programmable power supply applications. The DAC outputs may be programmed to track or oppose each other. If the load is floating, and can be driven differentially, the dynamic range will be 17 bits, because the full-scale range doubles for the same sized LSB. The clear line ($\overline{CLR}$) sets both DAC outputs to zero, and would be used at power-up to bring the system up in a safe state. The $\overline{CLR}$ line could also be used if an over-power state is sensed.

ISOLATION

The DAC725 has the ability to accept serial input data, which means that only six optoisolators are needed for two DACs. The data is clocked into the input latch using the $\overline{WR}$ pin. The 16-bit data word is latched into the DAC selected by $\overline{A_2}$. When $\overline{A_0}$ and $\overline{A_1}$ are simultaneously low, the serial mode is enabled.

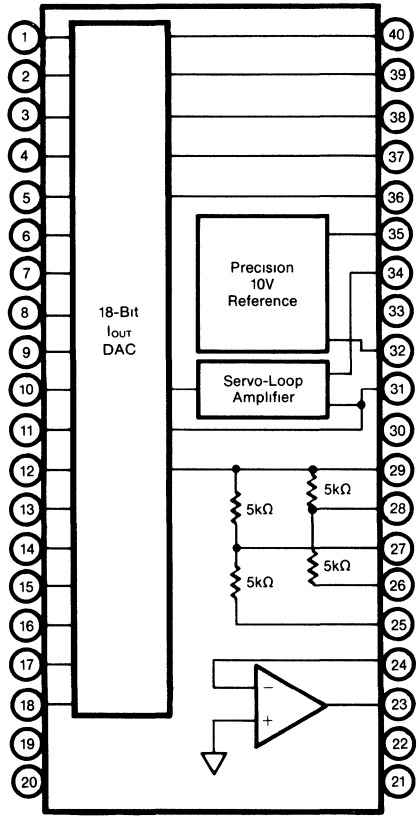
BURR-BROWN®

DAC729

Ultra-High Resolution
18-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 16-BIT LINEARITY GUARANTEED (K GRADE)
- USER ADJUSTABLE TO 18-BIT LINEARITY
- PRECISION INTERNAL REFERENCE
- FAST SETTLING, LOW NOISE INTERNAL OP AMP
- LOW DRIFT
- HERMETIC 40-PIN CERAMIC PACKAGE
- I_{OUT} OR V_{OUT} OPERATION



DESCRIPTION

The DAC729 sets the standard in very high accuracy digital-to-analog conversion. It is supplied from the factory at a guaranteed linearity of 16 bits, and is user-adjustable to 18-bit linearity (1LSB = FSR/262144).

To attain this high level of accuracy, the design takes advantage of Burr-Brown's thin-film monolithic DAC process, dielectric op amp process, hybrid capabilities, and advanced test and laser-trim techniques.

The DAC729 hybrid layout is specifically partitioned to minimize the effects of external load-current-induced thermal errors. The op amp design consists of a fast settling precision op amp with a current buffer within the feedback loop. This buffer isolates the load from the precision op amp, which results in a fast settling (8μs to 16 bits) output. The standard 40-pin package offers full hermeticity, contributing to the excellent reliability of the DAC729.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_{CC} = ±15V, V_{DD} = +5V, using internal reference op amp, unless otherwise noted COB = ±10V FSR, CSB = 0V to +10V FSR, 30 minute warm-up.

PARAMETER	DAC729JH MIN	DAC729JH TYP	DAC729JH MAX	DAC729KH MIN	DAC729KH TYP	DAC729KH MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution		18			*		Bits
Digital Inputs[1]: V_{IH}	+2 4		$+V_L$	*		*	V
V_{IL}	0		+0 8	*		*	V
I_{IH}, V_{IN} = +2.7V			+5 0			*	µA
I_{IL}, V_{IN} = +0 4V			−300			*	µA
TRANSFER CHARACTERISTICS[2]							
ACCURACY							
Linearity Error[3]			±0 0015			±0 00076	% of FSR[4]
Differential Linearity Error			±0 003			±0 0015	% of FSR
Gain Error[5]		±0 05	±0 10		*	*	%
Offset Error[5] Voltage, COB[6]		±5	±10		*	*	mV
CSB[6]		±3	±5		*	*	mV
Current, COB			±5			*	µA
CSB			±1			*	µA
Power Supply Sensitivity, Unipolar ±15VDC		±0 0001	±0 0005		*	*	% of FSR/%V_S
+5VDC		±0 0001	±0 0005		*	*	% of FSR/%V_S
Bipolar Offset, ±15VDC		±0 0004	±0 0015		*	*	% of FSR/%V_S
+5VDC		±0 0001	±0.0005		*	*	% of FSR/%V_S
Bipolar Gain ±15VDC		±0 0005	±0 0015		*	*	% of FSR/%V_S
+5VDC		±0 0001	±0 0005		*	*	% of FSR/%V_S
Output Noise (10Hz to 100kHz), Voltage Bipolar Offset		29			*		µVrms
Bipolar Gain		37			*		µVrms
Current Bipolar Offset		2 9			*		nArms
Bipolar Gain		3.0			*		nArms
Monotonicity (0°C to +70°C)	15	16		16	17		Bits
Differential Linearity Adjustment Resolution[7]		18			*		Bits
DRIFT (Over Specification Temperature Range)							
Gain Drift (Excluding Reference Drift)		±3	±5		*	*	ppm/°C
Offset Drift (Excluding Reference Drift) COB (Bipolar)		±2	±5		*	*	ppm of FSR/°C
CSB (Unipolar)		±2	±3		*	*	ppm of FSR/°C
Linearity Error (at 0°C and +70°C)		±0.3	±1 0		±0 3	±0 5	ppm of FSR/°C
Differential Linearity Error (at 0°C and +70°C)		±0.5	±2 0		±0 5	±1 0	ppm of FSR/°C
STABILITY, LONG TERM (at +25°C)							
Gain (Exclusive of Reference)		±5			±5		ppm/1000hr
Offset: COB (Exclusive of Reference)		±5			±5		ppm of FSR/1000hr
CSB		±5			±5		ppm of FSR/1000hr
Linearity		±2			±2		ppm of FSR/1000hr
Reference		±5			±5		ppm/1000hr
OUTPUT							
VOLTAGE OUTPUT MODE							
Ranges COB		±2.5, ±5, ±10			*		V
CSB		0 to +10, 0 to +5			*		V
Output Current	±5			*			mA
Output Impedance		0 15			*		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common		
CURRENT OUTPUT MODE							
COB Ranges		±1 0			*		mA
Output Impedance		2 86			*		kΩ
CSB Ranges		0 to −2			*		mA
Output Impedance		4.0			*		kΩ
Output Current Tolerance			±0 1			*	% of FSR
Compliance Voltage		−1 to +5			*		V
SETTLING TIME (To ±0 00076% of FSR)[9]							
Voltage (Load = 2kΩ ‖ 100pF) Full-Scale Step		5	8		*	*	µs
1LSB Step (Major Carry)[10]		4	7		*	*	µs
Slew Rate		20			*		V/µs
Switching Transient Peak		500			*		mV
Switching Transient Energy		0.45			*		V-µs
Current Full-Scale Step (2mA × 10Ω ‖ 1pF)		300			*		ns
REFERENCE							
Output (pin 32): Voltage	+9.990	+10.000	+10.010	*	*	*	V
Source Current[11]			+4 0			*	mA
Temperature Coefficient		±2	±4		*	*	ppm/°C
Short-Circuit Duration		Indefinite to Common			Indefinite to Common		
Power Supply Sensitivity		0.00025	0.003		*	*	%/V

ELECTRICAL (CONT)

PARAMETER	DAC729JH MIN	DAC729JH TYP	DAC729JH MAX	DAC729KH MIN	DAC729KH TYP	DAC729KH MAX	UNITS
POWER SUPPLY REQUIREMENTS							
Voltage $+V_{CC}$	+13 5	+15	+16 5	*	*	*	V
$-V_{CC}$	−16 5	−15	−13 5	*	*	*	V
V_{DD}	+4 75	+5	+5 25	*	*	*	V
Current $+V_{CC}$		+30	+40		*	*	mA
$-V_{CC}$		−45	−60		*	*	mA
V_{DD}		+18	+25		*	*	mA
Power Dissipation (Rated Supplies)		1 22	1 63		*	*	W
ENVIRONMENTAL SPECIFICATIONS							
Temperature Range Specification	0		+70	*		*	°C
Storage	−60		+150	*		*	°C

*Specification same as DAC729JH

NOTES (1) TTL and CMOS compatible (2) Specified for V_{OUT} mode using the internal op amp (3) ±0 00076% of full-scale range is 1/2LSB for 16-bit resolution (4) FSR means full-scale range, 20V for ±10V range, etc (5) Adjustable to zero error with an external potentiometer (6) COB is complementary offset binary (bipolar), CSB is complementary straight binary (unipolar) (7) Using the MSB adjustment circuit, the user may improve the DAC linearity to 1/2LSB of this specification (8) With gain and offset errors adjusted to zero at 25°C (9) Maximum represents 3 sigma limit, not 100% production tested (10) At the major carry, 20000 to 1FFFF Hex and from 1FFFF to 20000 Hex (11) Maximum with no degradation in specifications External loads must be constant

ABSOLUTE MAXIMUM RATINGS

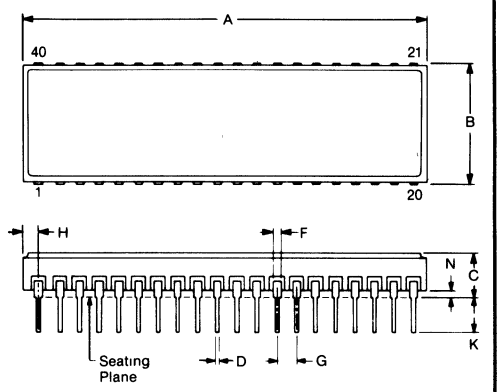
V_{DD} to Common ..... 0V to +7V
$+V_{CC}$ to Common ..... 0V to +18V
$-V_{CC}$ to Common ..... 0V to −18V
Digital Data Inputs (pins 1-18) to Common ..... −0 5V to V_{DD}
Reference Voltage In (Pin 31) ..... +9V to +11V
Reference Out (pin 32) to Common .... Indefinite Short to Common
External Voltage Applied to D/A Output (pin 29) ..... −5V to +5V
External Voltage Applied to Feedback Resistors
(pins 25, 26, 27, 28) ..... −15V to +15V
V_{OUT} (pin 23) ..... Indefinite Short to Common
Power Dissipation 3000mW
Storage Temperature ..... −60°C to +150°C
Lead Temperature, Soldering ..... +300°C, 10s

CAUTION These devices are sensitive to electrostatic discharge Appropriate I C handling procedures should be followed Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device Exposure to absolute maximum conditions for extended periods may affect device reliability

PIN CONNECTIONS

(MSB) Bit 1	1	40	V_{POT}
Bit 2	2	39	Bit 1 Adjust
Bit 3	3	38	Bit 2 Adjust
Bit 4	4	37	Bit 3 Adjust
Bit 5	5	36	Bit 4 Adjust
Bit 6	6	35	Reference Adjust
Bit 7	7	34	Gain Adjust
Bit 8	8	33	Reference Common
Bit 9	9	32	Reference Out
Bit 10	10	31	Reference In
Bit 11	11	30	Analog Common
Bit 12	12	29	I_{OUT}
Bit 13	13	28	5kΩ Feedback
Bit 14	14	27	5kΩ Feedback
Bit 15	15	26	10kΩ Feedback
Bit 16	16	25	10kΩ Feedback
Bit 17	17	24	Summing Junction
(LSB) Bit 18	18	23	V_{OUT}
V_{DD} (5V)	19	22	$+V_{CC}$ (15V)
Digital Common	20	21	$-V_{CC}$ (15V) ,

MECHANICAL



NOTE Leads in true position within 0 01" (0 25mm) R at MMC at seating plane

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1 980	2 040	50 29	51 82
B	610	630	15 49	16 00
C	150	200	3 81	5 08
D	016	020	0 41	0 51
F	050 TYP		1 27 TYP	
G	100 BASIC		2 54 BASIC	
H	030	070	0 76	1 78
J	009	012	0 23	0 30
K	155	195	3 94	4 95
L	600 BASIC		15 24 BASIC	
N	040	060	1 02	1 52

BURN-IN SCREENING

Burn-in screening is an option available for the DAC729 family of products. Burn-in duration is 160 hours at 85°C (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

THEORY OF OPERATION

The DAC729 is an 18-bit digital-to-analog converter system, including a precision reference, low noise, fast settling operational amplifier, and an 18-bit current source/DAC chip contained in a hermetic 40-pin ceramic dual-in-line package. Refer to Figure 11 for a schematic diagram of the DAC729.

THE INTERNAL REFERENCE

The reference consists of a very low temperature coefficient closed-loop reference zener circuit that has been temperature-drift-compensated by laser-trimming a zener current to achieve less than 1ppm/°C temperature drift of V_{REF}

By strapping pin 32 (Reference Out) to pin 31 (Reference In), the DAC will be properly biased from the internal reference. The internal reference may be fine adjusted using pin 35 as shown in Figure 7. The reference has an output buffer that will supply 4mA for use external to the DAC729. This load must remain constant because changing load on the reference may change the reference current to the DAC.

In systems where several components need to track the same system reference, the DAC729 may be used with an external 10V reference, however, the internal reference has lower noise (6μVp-p) and better stability than other references available.

THE OPERATIONAL AMPLIFIER

To support a DAC of this accuracy, the operational amplifier must have a maximum gain-induced error of less than 1/3LSB, independent of output swing (the op amp must be linear!). To support 15 bits (1/2-bit linearity) the op amp must have a gain of 130,000V/V. For 18 bits, the minimum gain is well over 500,000V/V. Since thermal feedback is the major limitation of gain for mono op amps, the amplifier was designed as a high gain, fast settling mono op amp, followed by a monolithic, unity-gain current buffer to isolate the thermal effects of external loads from the input stage gain transistors. The op amp and buffer are separated from the DAC chip, minimizing thermally-induced linearity errors in the DAC circuit. The op amp, like the reference, is not dedicated to the DAC729. The user may want to add a network, or select a different amplifier. The DAC729 internal op amp is intended to be the best choice for accuracy, settling time, and noise.

THE DAC CHIP

The heart of the DAC729 is a monolithic current source and switch integrated circuit. The absolute linearity, differential linearity, and the temperature performance of the DAC729 are the result of the design, which utilizes the excellent element matching of the current sources and switch transistors to each other, and the tracking of the current setting resistors to the feedback resistors. Older discrete designs cannot achieve the performance of this monolithic DAC design.

The two most significant bits are binarily weighted inter-digitated current sources. The currents for bits 3 through 18 are scaled with both current source weighting and an R-2R ladder. The circuit design is optimized for low noise and low superposition error, with the current sources arranged to minimize both code-dependent thermal errors and IR drop errors. As a result, the superposition errors are typically less than 20μV.

The DAC chip is biased from a servo amplifier feeding into the base line of the current sources. This servo amplifier sets the collector current to be mirrored and scaled in the DAC chip current sources, as shown in Figure 11. The reference current for the servo is established by the reference voltage applied to pin 31 feeding an internal resistor (20kΩ) to the virtual ground of the servo amplifier.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC729 accepts complementary digital input codes in either binary format (CSB for Unipolar or COB for Bipolar; see Table I).

TABLE I. Digital Input Coding.

Digital Input	DAC Analog Output			
	COB	20V FSR	CSB	10V FSR
00 0000 0000 0000 0000	+ Full Scale	9 999924V	+ Full Scale	9 999962V
11 1111 1111 1111 1111	− Full Scale	−10V	− Full Scale	0V

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points (all bits ON point and all bits OFF point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output step sizes can be between 1/2LSB and 3/2LSB when the input changes from one adjacent input state to the next. A negative DLE specification of no more than −1LSB (−0.0015% for 16-bit resolution) insures monotonicity to 16 bits.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC729KH is specified to be monotonic to 16 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale

range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is measured by: (1) testing the end point differences for each D/A at t_{MIN}, +25°C, and t_{MAX}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Offset Drift

Offset drift is a measure of the change in the output with $3FFFF_H$ applied to the digital inputs over the specified temperature range. The maximum change in offset at t_{MIN} or t_{MAX} is referenced to the offset error at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full-scale range per degree centigrade (ppm of FSR/°C).

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Settling time includes the slew time of the op amp.

VOLTAGE OUTPUT

Settling times are specified to ±0.00076% of FSR scale range change of 20V (COB) or 10V (CSB) and a 1LSB change at the "major carry," the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next.)

CURRENT OUTPUT

Settling times are specified to ±0.00076% of FSR for a full-scale range change with an output load resistance of 10Ω.

COMPLIANCE VOLTAGE

Compliance voltage applies only to the current output mode of operation. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified linearity.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter full-scale output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 1). It is specified for DC or low frequency changes. The typical performance curve in Figure 1 shows the effect of high frequency changes in power supply voltages using internal reference, DAC, and op amp.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in Figure 2. These capacitors (1μF to 10μF tantalum recommended) should be located at the DAC729.

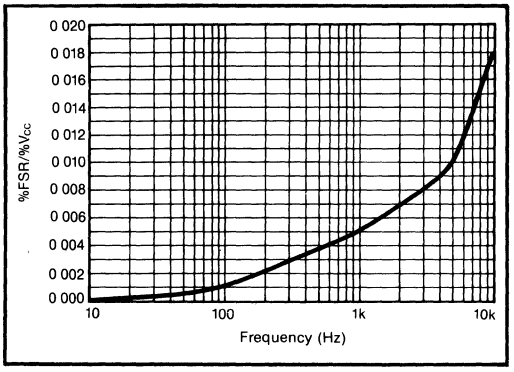


FIGURE 1. Power Supply Sensitivity vs Frequency Using Internal Reference and Op Amp.

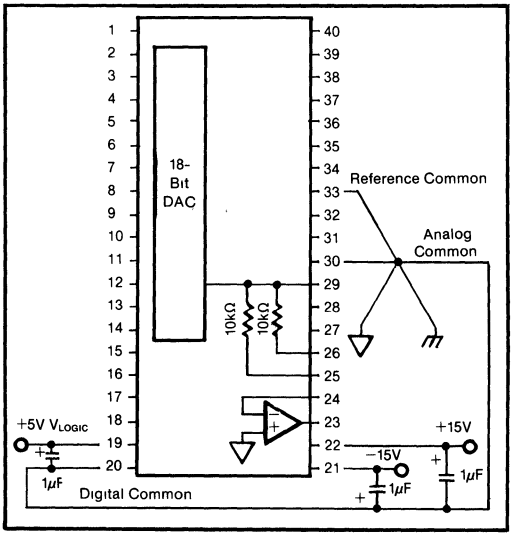


FIGURE 2. Ground Connections and Supply Bypass.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in Figure 3 and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 510kΩ resistors (20% carbon or better) should be located close to the DAC729 to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted in place of the 3.9MΩ. A 0.001μF to 0.01μF capacitor should be connected from Gain Adjust (pin 34) to common to shunt noise pickup. This capacitor should be a low leakage film type (such as Mylar or Teflon).

Refer to Figures 5 and 6 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters.

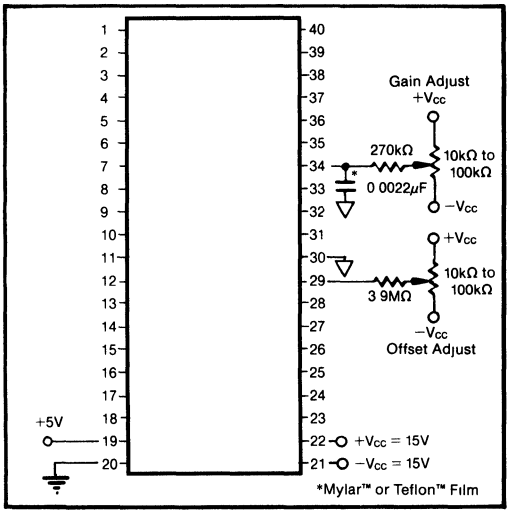


FIGURE 3. Gain and Offset Adjust Hook-Up.

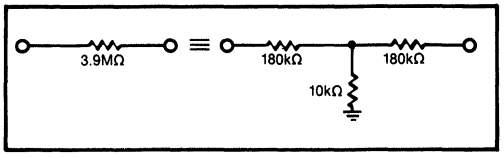


FIGURE 4. Equivalent Resistances.

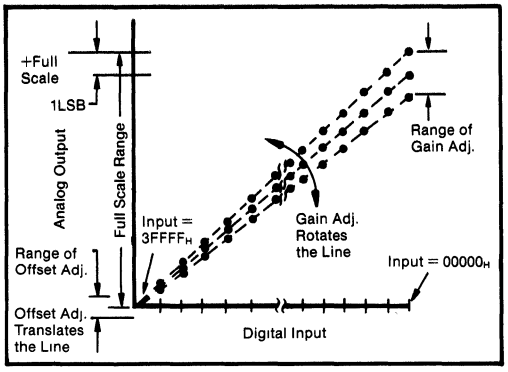


FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

OFFSET ADJUSTMENT

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the offset potentiometer for zero output.

For bipolar (COB) configurations, apply the digital input code that should produce the maximum negative output voltage. See Table II for corresponding codes and Figures 2 and 3 for offset adjustment connections. Offset adjust should be made prior to gain adjust.

Mylar™, Teflon™ E I du Pont de Nemours & Co

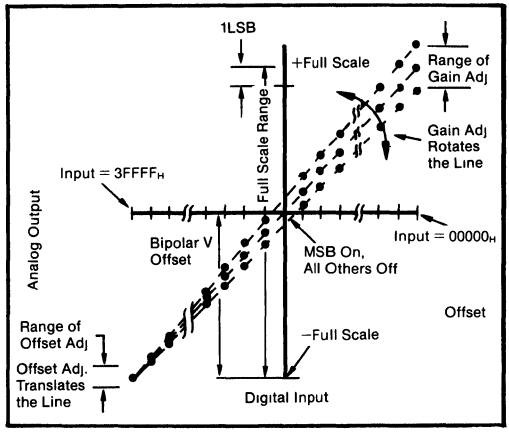


FIGURE 6. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output voltage. Adjust the gain potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages and Figure 3 for gain adjustment connections.

TABLE II. Output Range Connections and Gain Adjust Voltage.

Output Range	Code	Connect Pin 23	Connect Pin 31	Connect Pin 24	Gain Adjust	
					16 Bits	18 Bits
±10V	COB	to Pin 25	to Pin 26	to Pin 29	9.9969V	9.99992V
±5V	COB	to Pin 27	to Pin 26	to Pin 29	4.9998V	4 99996V
±2.5V	COB	to Pin 27	to Pin 26	to Pins 29 & 25	2 4992V	2 49998V
0 to 10V	CSB	to Pins 25 & 26	N/C	to Pin 29	9.9998V	9.99996V
0 to 5V	CSB	to Pins 27 & 28	N/C	to Pin 29	4 9999V	4.99998V

REFERENCE ADJUSTMENT

The internal reference may be fine adjusted using pin 35 as shown in Figure 7. Adjusting the reference has a similar effect on the DAC as gain adjust, except the transfer characteristic rotates around bipolar zero for a bipolar connection as shown in Figure 8.

LAYOUT/APPLICATIONS SUGGESTIONS

Obviously, the management of IR drops, power supply noise, thermal stability, and environmental noise becomes much more critical as the accuracy of the system increases. The DAC729 has been designed to minimize these applications problems to a large degree. The basics of "Kelvin sensing" and "holy point" grounding will be the most important considerations in optimizing the absolute accuracy of the system. Figure 9 shows the proper connection of the DAC with the holy-point ground and the Kelvin-sensed-output connection at the load.

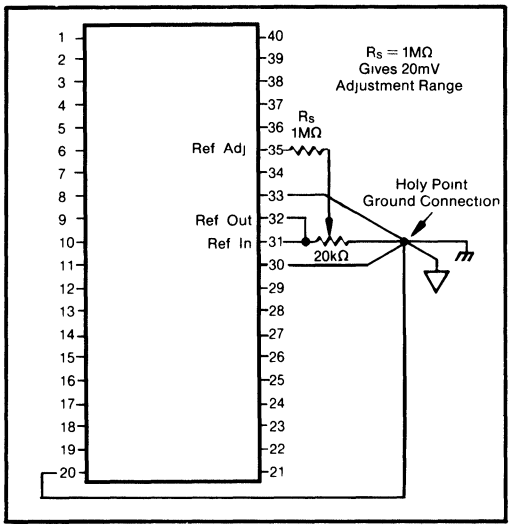


FIGURE 7. V_{REF} Adjust.

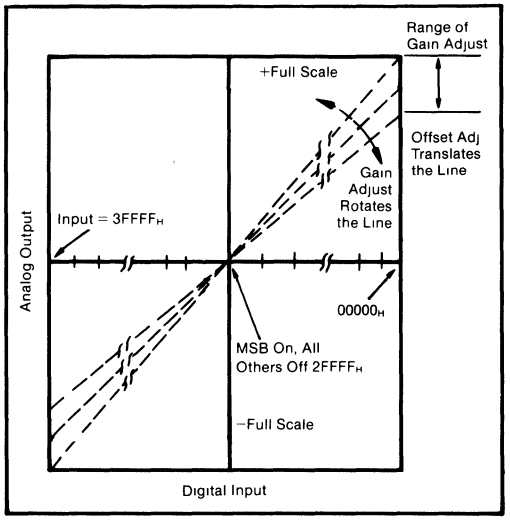


FIGURE 8. Effect of V_{REF} Adjust on a COB Connected DAC729.

The DAC729 has three separate supply common (ground) pins. Reference common (pin 33) carries the return current from the internal reference and the output I/V converter common. The current in pin 33 is stable and independent of code or load. Digital common (pin 20) carries the variable currents of the biasing circuits. Analog common (pin 30) is the termination of the R-2R ladder and also carries the "waste current" from the off side of the current switches. These three ground pins must be star connected to system ground for the DAC to bias properly and accurately. Good ground connections are essential, because an IR drop of just 39μV completely swamps out a 10V FSR 18-bit LSB.

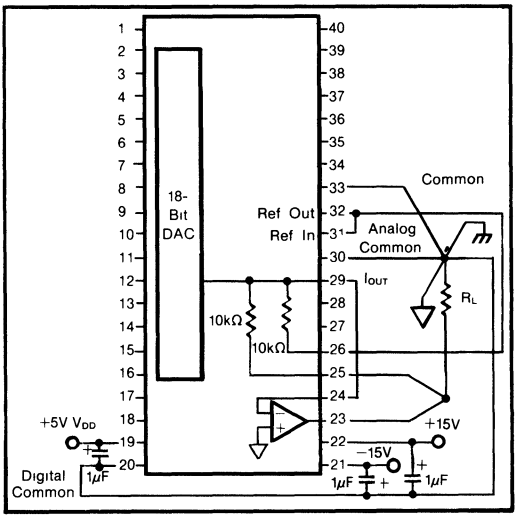


FIGURE 9. Typical Hook-Up Diagram with "Holy Point" Ground and Kelvin Sense Load, Using Internal Op Amp and Reference.

When the application is such that the DAC must control loads of greater than ±5mA with rated accuracy, it is recommended that an external op amp or op amp buffer combination be used to dissipate the variable power external to the DAC729. This minimizes the temperature variations on the precision D/A converter. Figure 10 illustrates a method of connecting the external amplifier for ±10V operation, while using an external reference.

When driving loads to greater than ±10V, care must be taken that the internal resistors are never exposed to greater than ±10V, and that the summing junction is

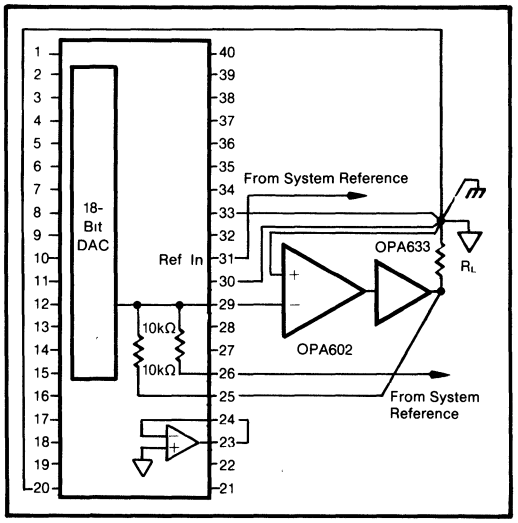


FIGURE 10. Using an External Op Amp with Buffer and External Reference for ±10V Output.

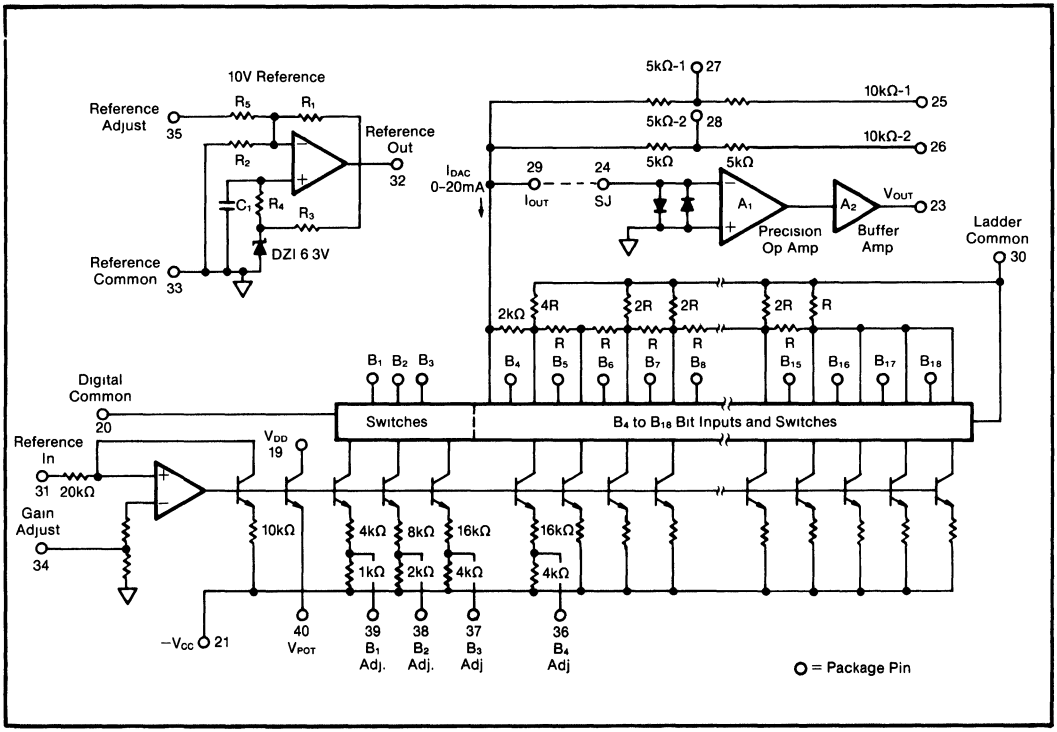


FIGURE 11. DAC729 Simplified Schematic.

clamped to insure that the voltage never exceeds ±5V. Clamping the summing junction with diodes (parallel opposing connection) to ground will give the best transient response and settling times.

TRUE 18-BIT PERFORMANCE (DIFFERENTIAL LINEARITY ADJUSTMENT)

To take full advantage of the DAC729's accuracy, the four MSBs have adjustment capabilities. A simplified schematic (Figure 11) shows the internal structure of the DAC current source and the adjustment input terminal. The suggested network for adjusting the linearity is shown in Figure 12. This circuit has nearly twice the range that is required for the DAC729JH. The range is intentionally narrow so as to minimize the effect of temperature drift or stability problems in the potentiometers. The potentiometers are biased in an identical fashion to the internal DAC current sources to minimize power supply sensitivity and drift over temperature. Low leakage capacitors such as Mylar or Teflon film are essential.

The linearity adjustment requires a digital voltmeter with 7 digits of resolution on the 10V range (1μV resolution) and excellent linearity. For the DAC, 1LSB of the 0V to 10V scale (10 FSR) is 38μV. To be 1/2LSB linear, the measurement must resolve 19μV. The meter must be properly calibrated and linear to 1ppm of range.

With the DAC connected for 0 to 10V output (Figure 13), the adjustment procedure is to set the DAC code and measure as follows.

FOURTH MSB ADJUSTMENT (Pin 36)
1. Set Code = 11 1100 0000 0000 0000
2. Measure V_{OUT}
3. Set Code = 11 1011 1111 1111 1111
4. Measure V_{OUT} and record the difference.
5. Adjust 4th MSB potentiometer to make difference +38μV.
6. Repeat steps 1 through 5 to confirm.

THIRD MSB ADJUSTMENT (Pin 37)
1. Set Code = 11 1000 0000 0000 0000
2. Measure V_{OUT}
3. Set Code = 11 0111 1111 1111 1111
4. Measure V_{OUT} and record the difference.
5. Adjust 3rd MSB potentiometer to make difference +38μV.
6. Repeat steps 1 through 5 to confirm.

SECOND MSB ADJUSTMENT (Pin 38)
1. Set Code = 11 0000 0000 0000 0000
2. Measure V_{OUT}
3. Set Code = 10 1111 1111 1111 1111
4. Measure V_{OUT} and record the difference.
5. Adjust 2nd MSB potentiometer to make difference +38μV.
6. Repeat steps 1 through 5 to confirm.

MSB ADJUSTMENT (Pin 39)

1. Set Code = 10 0000 0000 0000 0000
2. Measure V_{OUT}
3. Set Code = 01 1111 1111 1111 1111
4. Measure V_{OUT} and record the difference.
5. Adjust the MSB potentiometer to make difference $+38\mu V$.
6. Repeat steps 1 through 5 to confirm.

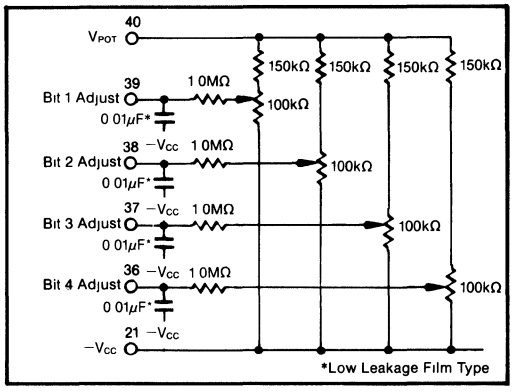


FIGURE 12. Differential Linearity Adjustment Circuit for the 4MSBs.

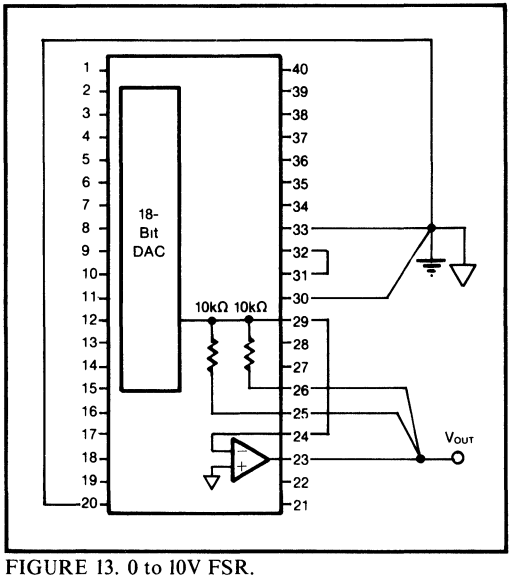


FIGURE 13. 0 to 10V FSR.

APPLICATIONS

The DAC729 is the DAC of choice for applications requiring very high resolution, accuracy, and wide dynamic range.

DIGITAL AUDIO

The excellent linearity and differential linearity are ideal for PCM professional audio and waveform generation applications.

The DAC729 offers superb dynamic range. Dynamic range is a measure of the ratio of the smallest signals the converter can produce to the full-scale range, usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6dB per bit. For the DAC729 the theoretical range is 108dB! The actual dynamic range is limited by noise (signal-to-noise) and linearity errors. The DAC729's $6\mu V$ typical noise floor, fast settling op amp, and adjustable 18-bit linearity minimize the limitation.

Total harmonic distortion (THD) is the measure of the magnitude and distribution of the linearity error, differential linearity error, noise, and quantization error. The THD is defined as the ratio of the square root of the sum of the squares of the harmonics to the values of the input fundamental frequency. The rms value of a DAC error can be shown to be

$$\epsilon_{rms} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2}$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the DAC729 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \frac{\epsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\% \quad (2)$$

where E rms is the rms signal-voltage level.

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

The DAC729 has demonstrated THD of 0.0009% at full scale (at 1kHz). This is the level of distortion that is desired to test other professional audio products, making the DAC729 ideal for professional audio test equipment.

The ability to adjust the linearity of the 4MSBs, the 18-bit resolution, fast settling and low noise give the DAC729 unmatched performance.

AUTOMATIC TEST EQUIPMENT

The pin functions of the DAC729 are convenient for use in automatic test equipment systems. The ability to use internal or external reference and internal or external op amp means versatility for the system designer. For example, in automatic test systems with several DACs and ADCs, it is desirable to operate all of the high accuracy converters from the same reference, improving the tracking characteristics of those components to one another. The reference in the DAC729 is a very stable precision reference, and is suitable for use as the system reference.

Test systems, and other large systems are the ideal application for a DAC of this accuracy, because the DAC will be calibrated in the environment in which it will be used. Since the environment is very stable, the manual calibration (Figure 12) may be adequate. However, highly automated systems will go to an automatic calibration routine. Replacing the potentiometers in Figure 12 with V_{OUT} DACs, and using sample and difference measurements, the major carry bit weights can be measured, and external DACs used to adjust the differential linearity of the DAC729. A successive approximation routine yields the fastest calibration. The output voltage of the external DACs will have to be level shifted, as the bit adjustment potentiometer must be able to achieve $-V_{CC}$ to give the full adjust range.

Because the DAC729 feedback resistors have a tolerance of ±0.1%, the output range can be rescaled slightly with small-value fixed external resistors to give convenient ranges. A popular range is 0V to +10.24V which gives even 5mV steps at 11 bits. In this case the LSB size is 39.06μV. Figure 14 shows how to connect two 240Ω resistors in series with the internal 10kΩ resistors to give a 0V to 10.24V full-scale range. Another convenient range might be 0V to +10.48576V which gives an even 40μV LSB step size.

THE HEART OF AN 18-BIT ADC

The DAC729 makes a good building block in ADC applications. The key to ADC accuracy is differential linearity of the DAC. The ability to adjust to 18-bit linearity, coupled with the fast settling time of the DAC729 makes the design cycle for an 18-bit successive approximation ADC much faster, and the production more consistent. Figure 15 shows the DAC as the heart of a successive approximation ADC. The clock and successive approximation register could be implemented in 7400 series TTL, as a simple gate-array or standard cell, or part of a local processor.

With the DAC out of the way, the comparator is the toughest part of the ADC design. To resolve an 18-bit LSB, and interface to a TTL logic device, the comparator must have a gain of 500kV/V (5X actual) as well as low hysteresis, low noise, and low thermally induced offsets. With this much gain, a slow comparator may be desired to reduce the risk of instability.

The feedback resistors of the DAC are the input scaling resistors of the ADC. An OPA602 and an OPA633 make an excellent buffer for the input signal, giving a very high input impedance to the signal (minimizing IR drop) while maintaining the linearity.

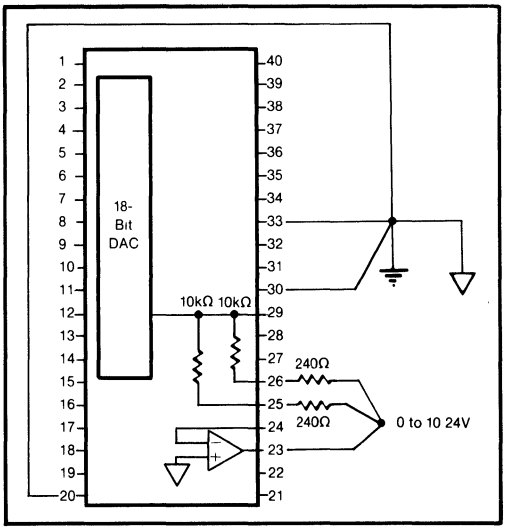


FIGURE 14. 0V to 10.24V Using Internal Op Amp and Internal Reference.

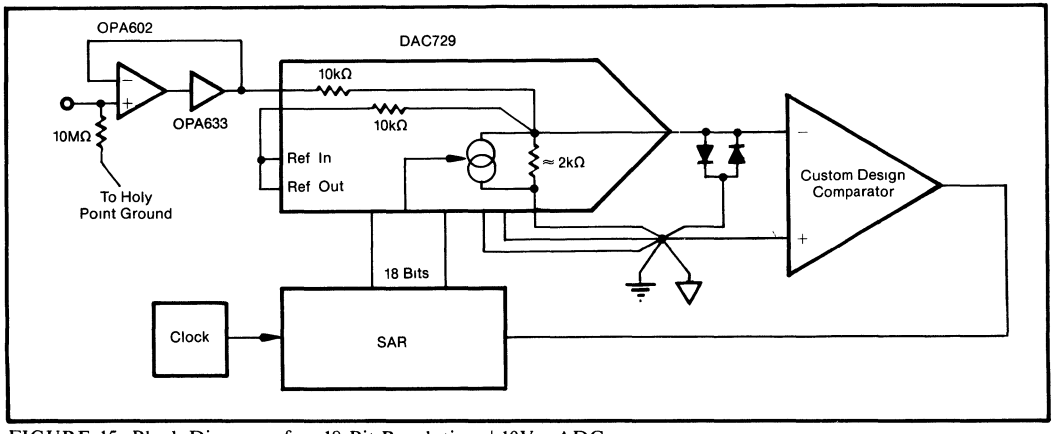


FIGURE 15. Block Diagram of an 18-Bit Resolution ±10V_{IN} ADC.

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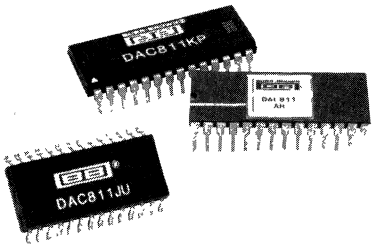


DAC811

AVAILABLE IN DIE FORM

Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **SINGLE INTEGRATED CIRCUIT CHIP**
- **MICROCOMPUTER INTERFACE: DOUBLE-BUFFERED LATCH**
- **VOLTAGE OUTPUT: ±10V, ±5V, +10V**
- **MONOTONICITY GUARANTEED OVER TEMPERATURE**
- **±1/2LSB MAXIMUM NONLINEARITY OVER TEMPERATURE**
- **GUARANTEED SPECIFICATIONS AT ±12V AND ±15V SUPPLIES**
- **TTL/5V CMOS-COMPATIBLE LOGIC INPUTS**

DESCRIPTION

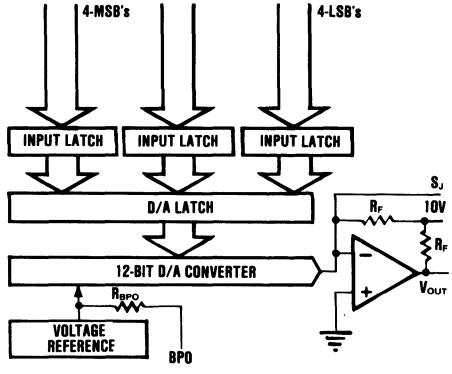
The DAC811 is a complete single-chip integrated circuit microcomputer-compatible 12-bit digital-to-analog converter. The chip includes a precision voltage reference, microcomputer interface logic, double-buffered latch, and a 12-bit D/A converter with a voltage output amplifier. Fast current switches and a laser-trimmed thin-film resistor network provide a highly accurate and fast D/A converter.

Microcomputer interfacing is facilitated by a double-buffered latch. The input latch is divided into three 4-bit nybbles to permit interfacing to 4-, 8-, 12- or 16-bit buses and to handle right- or left-justified data. The 12-bit data in the input latches is transferred to the D/A latch to hold the output value.

Input gating logic is designed so that loading the last nybble or byte of data can be accomplished simultaneously with the transfer of data (previously stored in adjacent latches) from adjacent input latches to the D/A latch. This feature avoids spurious analog output values while using an interface technique that saves computer instructions.

The DAC811 is laser trimmed at the wafer level and is specified to ±1/4LSB maximum linearity error (B, K, and S grades) at 25°C and ±1/2LSB maximum over the temperature range. All grades are guaranteed monotonic over the specification temperature range.

The DAC811 is available in six performance grades and three package types, as well as offering environmentally screened versions for enhanced reliability. DAC811J and K are specified over the temperature range of 0°C to +70°C; DAC811A and B are specified over −25°C to +85°C; DAC811R and S are specified over −55°C to +125°C. DAC811J and K are packaged in a reliable 28-pin plastic DIP or plastic SOIC package, while DAC811A, B, R, and S are available in a 28-pin 0.6-inch wide dual-in-line hermetically-sealed ceramic side-brazed package (H package).



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PDS-503E

SPECIFICATIONS

ELECTRICAL

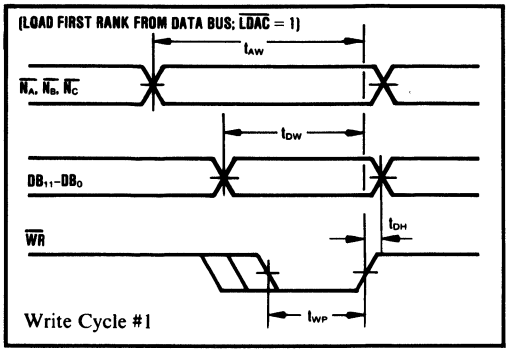
T_A = +25°C $\pm V_{CC}$ = 12V or 15V unless otherwise noted

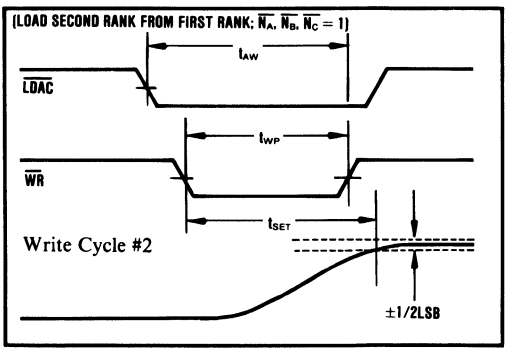
MODEL	DAC811AH, JP, JU			DAC811BH, KP, KU			DAC811RH			DAC811SH			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT													
DIGITAL INPUT													
Resolution			12			*			*			*	Bits
Codes[1]		USB, BOB			*			*			*		
Digital Inputs Over Temperature Range[2]													
V_{IH}	+2 0		+15	*		*	*		*	*		*	VDC
V_{IL}	0 0		+0 8	*		*	*		*	*		*	VDC
I_{IH}, V_I = +2 7V			+10			*			*			*	μA
I_{IL}, V_I = +0 4V			±20			*			*			*	μA
Digital Interface Timing Over Temperature Range													
t_{WP}, $\overline{WR}$ pulse width	50			*			*			*			nsec
t_{AW}1, $\overline{N_X}$ and $\overline{LDAC}$ valid to end of $\overline{WR}$	50			*			*			*			nsec
t_{DW}, data valid to end of $\overline{WR}$	80			*			*			*			nsec
t_{DH}, data valid hold time	0			*			+10			*			nsec
TRANSFER CHARACTERISTICS													
ACCURACY													
Linearity Error		±1/4	±1/2		±1/8	±1/4		±1/4	±1/2		±1/8	±1/4	LSB
Differential Linearity Error		±1/2	±3/4		±1/4	±1/2		±1/2	±3/4		±1/4	±1/2	LSB
Gain Error[3]		±0 1	±0 2		*	*		*	*		*	*	%
Offset Error[3,4]		±0 05	±0 15		*	*		*	*		*	*	% of FSR[5]
Monotonicity		Guaranteed			*			*			*		
Power Supply Sensitivity, $+V_{CC}$		±0 001	±0 003		*	*		*	*		*	*	% of FSR/%V_{CC}
$-V_{CC}$		±0 002	±0 006		*	*		*	*		*	*	% of FSR/%V_{CC}
V_{DD}		±0 0005	±0 0015		*	*		*	*		*	*	% of FSR/%V_{DD}
DRIFT (over specification temperature range)[10]													
Gain		±10	±30		±10	±20		±15	±30		±15	±30	ppm/°C
Unipolar Offset		±5	±10		±5	±7		±5	±10		±5	±7	ppm of FSR/°C
Bipolar Zero		±5	±10		±5	±7		±5	±10		±5	±7	ppm of FSR/°C
Linearity Error Over Temperature Range		±1/2	±3/4		±1/4	±1/2		±1/2	±3/4		±1/4	±1/2	LSB
Monotonicity Over Temperature Range		Guaranteed			*			*			*		
CONVERSION SPEED													
SETTLING TIME[6] (to within ±0 01% of FSR of final value, 2kΩ load)													
For Full Scale Range Change, 20V Range		3	4		*	*		*	*		*	*	μsec
10V Range		3	4		*	*		*	*		*	*	μsec
For 1LSB Change at Major Carry[7]		1			*			*			*		μsec
Slew Rate[6]	8	12		*	*		*	*		*	*		V/μsec
OUTPUT													
ANALOG OUTPUT													
Voltage Range ($\pm V_{CC}$ = 15V)[8], Unipolar		0 to +10			*			*			*		V
Bipolar		±5, ±10			*			*			*		V
Output Current	±5			*			*			*			mA
Output Impedance (at DC)		0 2			*			*			*		Ω
Short Circuit to Common Duration		Indefinite			*			*			*		
REFERENCE VOLTAGE													
Voltage	+6 2	+6 3	+6 4	*	*	*	*	*	*	*	*	*	V
Source Current Available for External Loads	+2 0			*			*			*			mA
Temperature Coefficient		±10	±30		±10	±20		±10	±30		±10	±20	ppm/°C
Short Circuit to Common Duration		Indefinite			*			*			*		
POWER SUPPLY REQUIREMENTS													
Voltage, $+V_{CC}$	+11 4	+15	+16 5	*	*	*	*	*	*	*	*	*	VDC
$-V_{CC}$	−11 4	−15	−16 5	*	*	*	*	*	*	*	*	*	VDC
V_{DD}	+4 5	+5	+5 5	*	*	*	*	*	*	*	*	*	VDC
Current (no load), $+V_{CC}$		+16	+25		*	*	*	*	*	*	*	*	mA
$-V_{CC}$		−23	−35		*	*	*	*	*	*	*	*	mA
V_{DD}		+8	+15		*	*	*	*	*	*	*	*	mA
Potential at DCOM with Respect to ACOM[9]			±0 5			*			*			*	V
Power Dissipation		625	800		*	*		*	*		*	*	mW
TEMPERATURE RANGE													
Specification J, K	0		+70	*		*							°C
A, B	−25		+85	*		*							°C
R, S							−55		+125	*		*	°C
Storage J, K	−60		+100	*		*							°C
A, B, R, S	−65		+150	*		*	*		*	*		*	°C

*Same as specification to immediate left

NOTES (1) USB = Unipolar Straight Binary, BOB = Bipolar Offset Binary (2) Refer to Logic Input Compatibility section (3) Adjustable to zero with external trim potentiometer (4) Error at input code 000_{16} for both unipolar and bipolar ranges (5) FSR means Full Scale Range and is 20V for the ±10V range (6) Maximum represents the 3σ limit Not 100% tested for this parameter (7) At the major carry, $7FF_{16}$ to 800_{16} and 800_{16} to $7FF_{16}$ (8) Minimum supply voltage required for ±10V output swing is ±13 5V Output swing for ±11 4V supplies is at least −8V to +8V (9) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications (10) Drift for the DAC811KU is identical to the JU grade on SOIC only, guaranteed

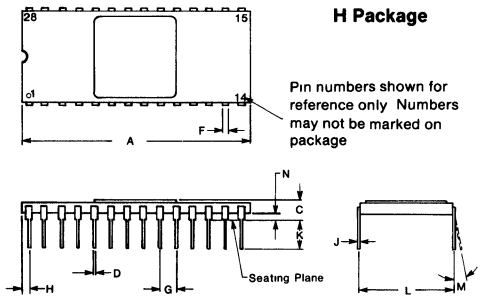
TIMING DIAGRAMS





MECHANICAL

H Package



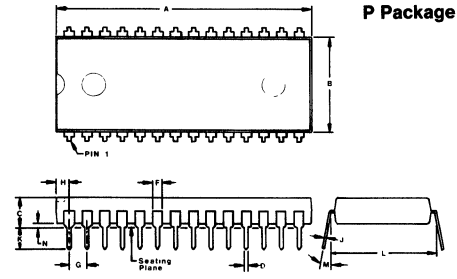
Pin numbers shown for reference only Numbers may not be marked on package

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1 386	1 414	35 20	35 92
C	108	166	2 74	4 22
D	015	021	0 38	0 53
F	035	060	0 89	1 52
G	100 BASIC		2 54 BASIC	
H	036	064	0 91	1 63
J	008	012	0 20	0 30
K	120	240	3 05	6 10
L	600 BASIC		15 24 BASIC	
M	—	10°	—	10°
N	025	060	0 64	1 52

NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

CASE Ceramic, hermetic
MATING CONNECTOR 2803MC
WEIGHT 4 8gm (0 17oz)

P Package

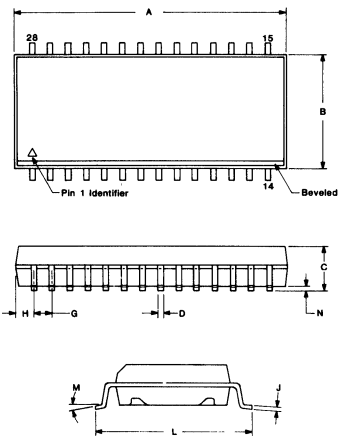


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1 400	1 460	35 56	37 08
B	0 530	0 575	13 46	14 61
C	0 169	0 224	4 29	5 69
D	0 015	0 023	0 38	0 58
F	0 043	0 065	1 09	1 65
G	0 100 BASIC		2 54 BASIC	
H	0 030	0 090	0 76	2 29
J	0 008	0 015	0 20	0 38
K	0 100	0 136	2 54	3 45
L	0 600 BASIC		15 24 BASIC	
M	0°C	15°C	0°C	15°C
N	0 018	0 022	0 46	0 56

NOTE
Leads in true position within 010" (25mm) R at MMC at seating plane

CASE Ceramic, hermetic
MATING CONNECTOR 2803MC
WEIGHT 4 3gm (0 15oz)

U Package



NOTE Leads in true position within 010" (25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers may not be marked on package

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	700	716	17 78	18 19
B	286	302	7 26	7 67
C	093	109	2 36	2 77
D	016 BASIC		0 41 BASIC	
G	050 BASIC		1 27 BASIC	
H	022	038	0 56	0 97
J	008	012	0 20	0 30
L	398	414	10 11	10 52
M	5° TYP		5° TYP	
N	000	012	0 00	0 30

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$	0 to +18V
$-V_{CC}$ to ACOM	0 to −18V
V_{DD} to DCOM	0 to +7V
V_{DD} to ACOM	±7V
ACOM to DCOM	±7V
Digital Inputs (pins 2-14, 16-19) to DCOM	−0 4V to +18V
External Voltage Applied to 10V Range Resistor	±12V
REF OUT	Indefinite short to ACOM
External Voltage Applied to DAC Output	−5 to +5V
Power Dissipation	1000mW
Lead Temperature, Soldering	+300°C, 10s
Max Junction Temperature	165°C
Thermal Resistance, θ_{JA}: Plastic DIP & SOIC	100°C/W
Ceramic DIP	65°C/W

PIN NOMENCLATURE

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	V_{DD}	Logic Supply, +5V	14	D_4	DATA, Bit 5
2	$\overline{WR}$	WRITE, command signal to load latches Logic low loads latches	15	DCOM	DIGITAL COMMON, V_{DD} supply return
3	$\overline{LDAC}$	LOAD D/A CONVERTER, enables $\overline{WR}$ to load the D/A latch Logic low enables	16	D_0	DATA, Bit 1, LSB
4	$\overline{N_A}$	NYBBLE A, enables $\overline{WR}$ to load input latch A (the most significant nybble Logic low enables	17	D_1	DATA, Bit 2
5	$\overline{N_B}$	NYBBLE B, enables $\overline{WR}$ to load input latch B Logic low enables	18	D_2	DATA, Bit 3
6	$\overline{N_C}$	NYBBLE C, enables $\overline{WR}$ to load input latch C (the least significant nybble) Logic low enables	19	D_3	DATA, Bit 4
7	D_{11}	DATA, Bit 12, MSB, positive true	20	$+V_{CC}$	Analog Supply Input, +15V or +12V
8	D_{10}	DATA, Bit 11	21	$-V_{CC}$	Analog Supply Input, −15V or −12V
9	D_9	DATA, Bit 10	22	GAIN ADJ	To externally adjust gain
10	D_8	DATA, Bit 9	23	ACOM	ANALOG COMMON, $\pm V_{CC}$ supply return
11	D_7	DATA, Bit 8	24	V_{out}	D/A converter voltage output
12	D_6	DATA, Bit 7	25	10V RANGE	Connect to pin 24 for 10V Range
13	D_5	DATA, Bit 6	26	SJ	SUMMING JUNCTION of output amplifier
			27	BPO	BIPOLAR OFFSET Connect to pin 26 for Bipolar Operation
			28	REF OUT	6 3V reference output

ORDERING INFORMATION

Model	Package	Temperature Range	Linearity Error, max (+25°C)	Gain Drift (ppm/°C)
DAC811JP	Plastic DIP	0°C to +70°C	±1/2LSB	30
DAC811JU	Plastic SOIC	0°C to +70°C	±1/2LSB	30
DAC811KP	Plastic DIP	0°C to +70°C	±1/4LSB	20
DAC811KU	Plastic SOIC	0°C to +70°C	±1/4LSB	20
DAC811AH	Ceramic DIP	−25°C to +85°C	±1/2LSB	30
DAC811AH/QM	Ceramic DIP	−25°C to +85°C	±1/2LSB	30
DAC811BH	Ceramic DIP	−25°C to +85°C	±1/4LSB	20
DAC811BH/QM	Ceramic DIP	−25°C to +85°C	±1/4LSB	20
DAC811RH	Ceramic DIP	−55°C to +125°C	±1/2LSB	30
DAC811RH/QM	Ceramic DIP	−55°C to +125°C	±1/2LSB	30
DAC811SH	Ceramic DIP	−55°C to +125°C	±1/4LSB	20
DAC811SH/QM	Ceramic DIP	−55°C to +125°C	±1/4LSB	±1

BURN-IN SCREENING OPTION
See text for details

Model	Package	Temperature Range	Linearity Error, max (+25°C)	Gain Drift, (ppm/°C)
DAC811JP-BI	Plastic DIP	0°C to +70°C	±1/2LSB	30
DAC811JU-BI	Plastic SOIC	0°C to +70°C	±1/2LSB	30
DAC811KP-BI	Plastic DIP	0°C to +70°C	±1/4LSB	20
DAC811KU-BI	Plastic SOIC	0°C to +70°C	±1/4LSB	20

NOTE (1) Or equivalent combination of time and temperature

DISCUSSION OF SPECIFICATIONS

INPUT CODES

The DAC811 accepts positive true binary input codes. DAC811 may be connected by the user for any one of the following codes: USB (unipolar straight binary), BOB (bipolar offset binary) or, using an external inverter on the MSB line, BTC (binary two's complement). See Table I.

DIGITAL INPUT	ANALOG OUTPUT		
MSB ↓ LSB ↓	USB Unipolar Straight Binary	BOB Bipolar Offset Binary	BTC* Binary Two's Complement
111111111111	+Full Scale	+Full Scale	−1 LSB
100000000000	+1/2 Full Scale	Zero	−Full Scale
011111111111	1/2 Full Scale −1 LSB	−1 LSB	+Full Scale
000000000000	Zero	−Full Scale	Zero

*Invert the MSB of the BOB code with external inverter to obtain BTC code

TABLE I. Digital Input Codes.

LINEARITY ERROR

Linearity Error as used in D/A converter specifications by Burr-Brown is the deviation of the analog output from a straight line drawn between the end points (inputs all "1's" and all "0's"). The DAC811 linearity error is specified at ±1/4LSB (max) at +25°C for B, K, and S grades and ±1/2LSB (max) for A, J, and R grades.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the input changes from one state to the next. Monotoni-

city requires that DLE be less than 1LSB over the temperature range of interest.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital inputs. All grades of DAC811 are monotonic over their specification temperature range.

DRIFT

Gain drift is a measure of the change in the full scale range output over the specification temperature range. Drift is expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by testing the full scale range value (e.g., +FS minus −FS) at high temperature, +25°C, and low temperature; calculating the error with respect to the +25°C value and dividing by the temperature change.

Unipolar offset drift is a measure of the change in output with all 0's on the input over the specification temperature range. Offset is measured at high temperature, +25°C, and low temperature. The maximum change in offset referred to the +25°C value divided by the temperature change is the offset drift. It is expressed in parts per million of full scale range per degree centigrade (ppm of FSR/°C).

Bipolar zero drift is measured at a digital input of 800_{16}, the code that gives zero volts output for bipolar operation.

SETTLING TIME

Settling Time is the total time (including slew time) for the output to settle within an error band around its final value after a change in input. Three settling times are specified to ±0.01% of Full Scale Range (FSR): two for maximum full scale range changes of 20V and 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry ($7FF_{16}$ to 800_{16} and 800_{16} to $7FF_{16}$), the input transition at which worst-case settling time occurs.

REFERENCE SUPPLY

DAC811 contains an on-chip 6.3V reference. This voltage (pin 28) has a tolerance of ±0.1V. The reference output may be used to drive external loads, sourcing at least 2.0mA. This current should be constant for best performance of the D/A converter.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR output change per percent of change in either the positive, negative, or logic supply voltages about the nominal voltages. Figure 1 shows typical power supply rejection versus power supply ripple frequency.

BURN-IN SCREENING

Burn-in screening is an option available for the plastic-DIP and plastic-SOIC package versions of the DAC811. Burn-in duration is 160 hours at 85°C (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

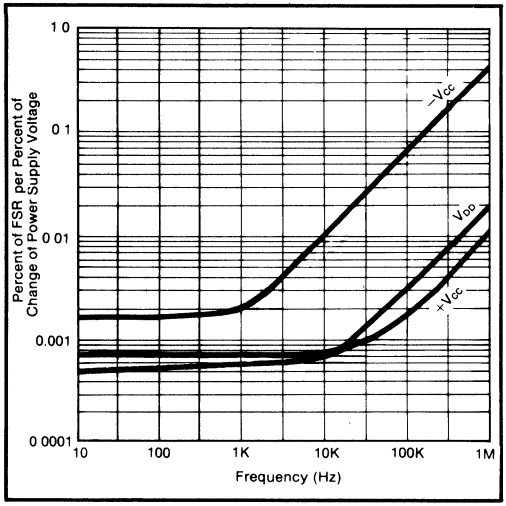


FIGURE 1. Power Supply Rejection versus Power Supply Ripple Frequency.

/QM SCREENING

Burr-Brown /QM models are environmentally screened versions of our ceramic-package versions of Model DAC811, designed to provide enhanced reliability. The screening, tabulated below, is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified below. Burr-Brown's detailed procedures may very slightly, model-to-model from those in MIL-STD-883.

SCREENING FLOW FOR DAC811/QM

Screen	MIL-STD-883 Method	Condition
Internal Visual	2010	B
High Temperature Storage (Stabilization Bake)	1008	C (150°C, 24Hr)
Temperature Cycling	1010	C
Burn-in	1015	B (160h at 125°C)
Constant Acceleration	2001	E
Hermeticity Fine Leak Gross Leak	1014 1014	A1 or A2 C
External Visual	2009	

OPERATION

DAC811 is a complete single IC chip 12-bit D/A converter. The chip contains a 12-bit D/A converter, voltage reference, output amplifier, and microcomputer-compatible input logic as shown in Figure 2.

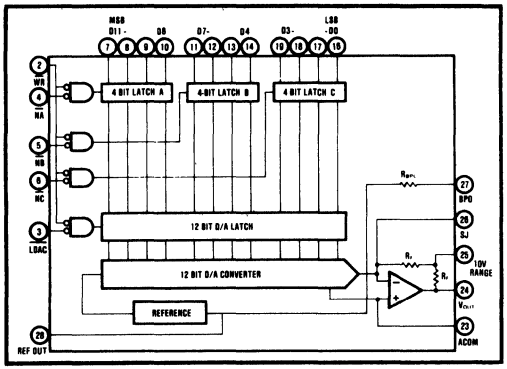


FIGURE 2. DAC811 Block Diagram.

INTERFACE LOGIC

Input latches A, B, and C hold data temporarily while a complete 12-bit word is assembled before loading into the D/A register. This double-buffered organization prevents the generation of spurious analog output values. Each register is independently addressable.

These input latches are controlled by $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ and $\overline{WR}$. $\overline{N_A}$, $\overline{N_B}$, and $\overline{N_C}$ are internally NORed with $\overline{WR}$ so that the input latches transmit data when both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ are at logic "0". When either $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) or $\overline{WR}$ go to logic "1", the input data is latched into the input registers and held until both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ go to logic "0".

The D/A latch is controlled by $\overline{LDAC}$ and $\overline{WR}$. $\overline{LDAC}$ and $\overline{WR}$ are internally NORed so that the latches transmit data to the D/A switches when both $\overline{LDAC}$ and $\overline{WR}$ are at logic "0". When either $\overline{LDAC}$ or $\overline{WR}$ are at logic "1", the data is latched in the D/A latch and held until $\overline{LDAC}$ and $\overline{WR}$ go to logic "0".

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When any one of the control signals returns to logic "1", the data is latched. A truth table for all latches is given in Table II.

TABLE II. DAC811 Interface Logic Truth Table.

$\overline{WR}$	$\overline{N_A}$	$\overline{N_B}$	$\overline{N_C}$	$\overline{LDAC}$	OPERATION
1	X	X	X	X	No Operation
0	0	1	1	1	Enables Input Latch 4MSB's
0	1	0	1	1	Enables Input Latch 4 Middle Bits
0	1	1	0	1	Enables Input Latch 4 LSB's
0	1	1	1	0	Loads D/A Latch From Input Latches
0	0	0	0	0	All Latches Transparent

"X" = Don't Care

GAIN AND OFFSET ADJUSTMENTS

Figures 3 and 4 illustrate the relationship of Offset and Gain adjustments to unipolar and bipolar D/A converter output.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output and adjust the Offset potentiometer for zero output. For bipolar (BOB, BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is −10V. See Table III for corresponding codes.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the Gain potentiometer for this positive full scale voltage. See Table III for positive full scale voltages.

±12V OPERATION

The DAC811 is fully specified for operation on ±12V power supplies. However, in order for the output to swing to ±10V, the power supplies must be ±13.5V or greater. When operating with ±12V supplies, the output

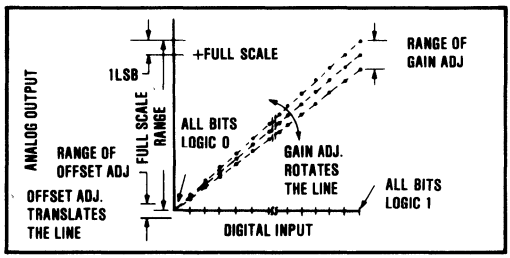


FIGURE 3. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter

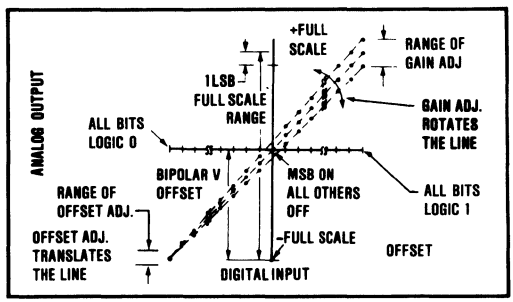


FIGURE 4. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

TABLE III. Digital Input/Analog Output, $\pm V_{CC} = \pm 15V$.

DIGITAL INPUT	ANALOG OUTPUT VOLTAGE		
	0 to +10V	±5V	±10V
12-Bit Resolution MSB ↓ LSB ↓			
111111111111	+9 9976V	+4 9976V	+9 9951V
100000000000	+5 0000V	0 0000V	0 0000V
011111111111	+4 9976V	−0.0024V	−0 0049V
000000000000	0.0000V	−5 0000V	−10 0000V
1LSB	2.44mV	2 44mV	4 88mV

swing should be restricted to ±8V in order to meet specifications.

LOGIC INPUT COMPATIBILITY

The DAC811 digital inputs are TTL, LSTTL, and 54/74HC CMOS-compatible over the operating range of V_{DD}. The input switching threshold remains at the TTL threshold over the supply range.

The logic input current over temperature is low enough to permit driving the DAC811 directly from the outputs of 4000B and 54/74C CMOS devices.

INSTALLATION

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram, Figure 5.

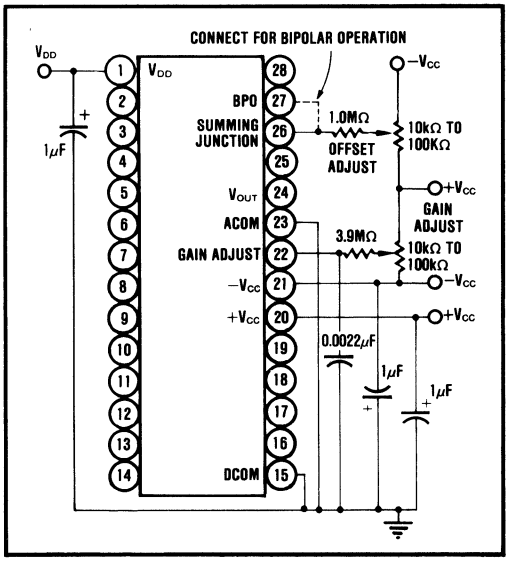


FIGURE 5. Power Supply, Gain, and Offset Potentiometer Connections.

These capacitors (1μF tantalum recommended) should be located close to the DAC811.

The DAC811 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. The Analog Common (pin 23) and Digital Common (pin 15) should be connected together at one point. Separate returns minimize current flow in low level signal paths if properly connected. Logic return currents are not added into the analog signal return path. A ±0.5V difference between ACOM and DCOM is permitted for specified operation. High frequency noise on DCOM with respect to ACOM may permit noise to be coupled through to the analog output, therefore, some caution is required in applying these common connections.

The Analog Common is the high quality return for the D/A converter and should be connected directly to the analog reference point of the system. The load driven by the output amplifier should be returned to the Analog Common.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 5. TCR of the potentiometers should be 100 ppm/°C or less. The 1.0MΩ and 3.9MΩ resistors (20% carbon or better) should be located close to the DAC811 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 6, may be substituted in each case. The Gain Adjust (pin 22) is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Analog Common to reduce noise pickup in all applications, including those not employing external gain adjustment.

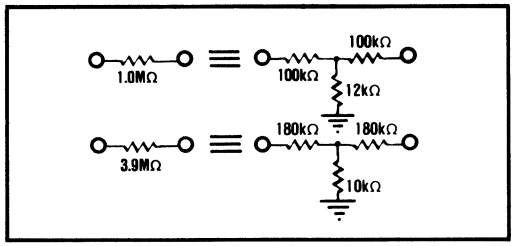


FIGURE 6. Equivalent Resistances.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC811 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or unipolar output voltage range of 0 to +10V. The 20V range (±10V bipolar range) is internally connected. Refer to Figure 7. Connections for the output ranges are listed in Table IV.

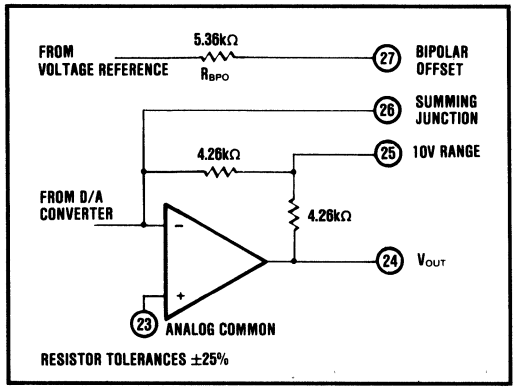


FIGURE 7. Output Amplifier Voltage Range Scaling Circuit.

Table IV. Output Range Connections.

Output Range	Digital Input Codes	Connect Pin 25 To	Connect Pin 27 To
0 to +10V	USB	24	23
±5V	BOB or BTC	24	26
±10V	BOB or BTC	NC	26

APPLICATIONS

MICROCOMPUTER BUS INTERFACING

The DAC811 interface logic allows easy interface microcomputer bus structures. The control signal $\overline{WR}$ is derived from external device select logic and the I/O Write or Memory Write (depending upon the system design) signals from the microcomputer.

The latch enable lines $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ and $\overline{LDAC}$ determine which of the latches are enabled. It is permissible to enable two or more latches simultaneously as shown in some of the following examples.

The double-buffered latch permits data to be loaded into the input latches of several DAC811's and later strobed into the D/A latch of all D/A's simultaneously updating all analog outputs. All the interface schemes shown below use a base address decoder. If blocks of memory are unused, the base address decoder can be simplified or eliminated altogether. For instance if half the memory space is unused, address line A_{15} of the microcomputer can be used as the chip select control.

4-BIT INTERFACE

An interface to a 4-bit microcomputer is shown in Figure 8. Each DAC811 occupies four address locations. A 74LS139 provides the two to four decoder and selects these with the base address. Memory Write ($\overline{WR}$) of the microcomputer is connected directly to the $\overline{WR}$ pin of the DAC811. A 8205 decoder is an alternative device to use instead of the 74LS139.

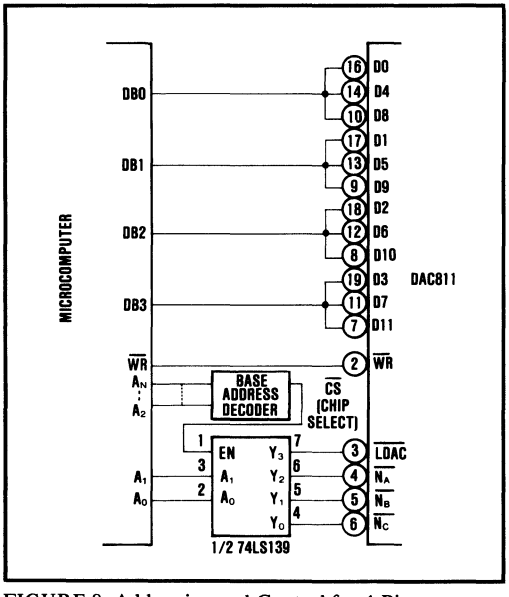


FIGURE 8. Addressing and Control for 4-Bit Microcomputer Interface.

8-BIT INTERFACE

The control logic of DAC811 permits interfacing to right- or left-justified data formats illustrated in Figure 9. When a 12-bit D/A converter is loaded from an 8-bit bus, two bytes of data are required. Figures 10 and 11 show an addressing scheme for right-justified and left-justified data respectively. The base address is decoded from the high-order address bits. A_0 and A_1 address the appropriate latches. Note that adjacent addresses are used. For the right-justified case $X10_{16}$ loads the 8 LSB's and $X01_{16}$ loads the 4MSB's and simultaneously transfers input latch data to the D/A latch. Addresses $X00_{16}$ and $X11_{16}$ are not used.

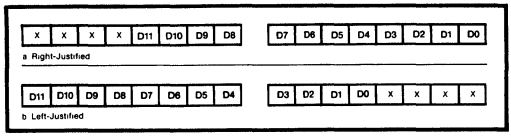


FIGURE 9. 12-Bit Data Formats for 8-Bit Systems.

Left-justified data is handled in a similar manner, shown in Figure 11. The DAC811 still occupies two adjacent locations in the microcomputer's memory map.

INTERFACING MULTIPLE DAC811's IN 8-BIT SYSTEMS

Many applications require that the outputs of several D/A converters be updated simultaneously such as

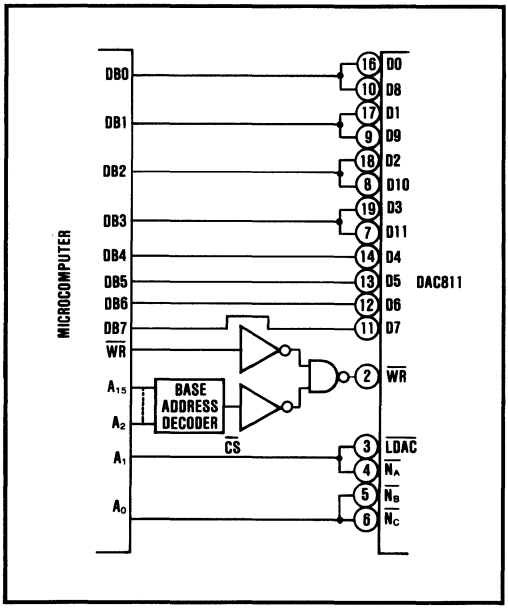


FIGURE 10. Right-Justified Data Bus Interface.

automatic test systems. The interface shown in Figure 12 uses a 74LS138 decoder to decode a set of eight adjacent addresses to load the input latches of four DAC811's. The example shows a right-justified data format.

A ninth address using A_3 causes all DAC811's to be updated simultaneously. If a particular DAC811 is always loaded last, for instance, D/A #4, A_3 is not needed, thus saving 8 address spaces for other uses. Incorporate A_3 into the Base Address Decoder, remove the inverter, connect the common $\overline{LDAC}$ line to $\overline{N_C}$ of D/A #4, and connect G1 of the 74LS138 to +5V.

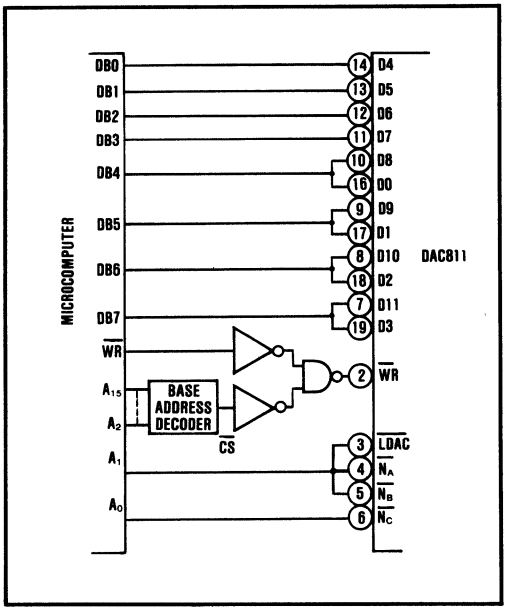


FIGURE 11. Left-Justified Data Bus Interface.

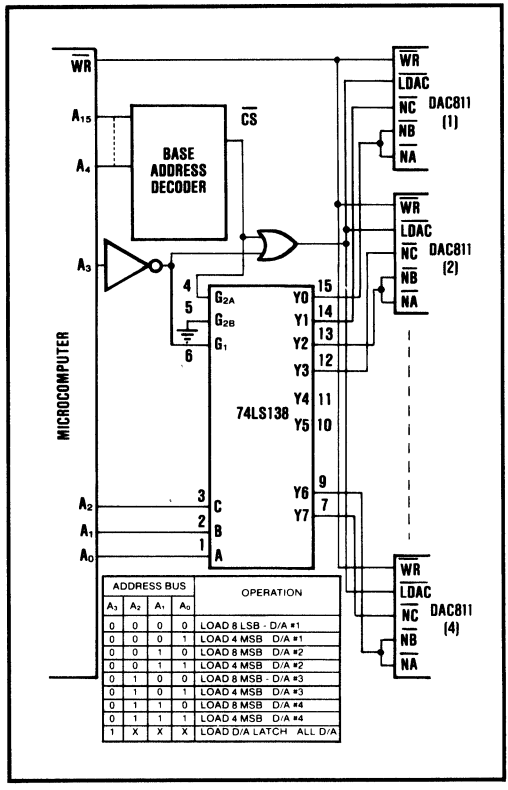


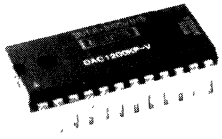
FIGURE 12. Interfacing Multiple DAC 811's to an 8-Bit Bus.

12- AND 16-BIT MICROCOMPUTER INTERFACE

For this application the input latch enable lines, $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ are tied low, causing the latches to be transparent. The D/A latch, and therefore DAC 811, is selected by the address decoder and strobed by $\overline{WR}$.

BURR-BROWN®

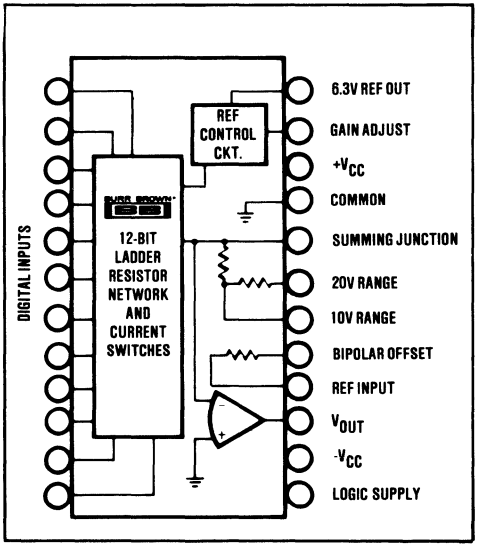
DAC1200KP-V



Integrated Circuit
12-Bit Resolution
DIGITAL-TO-ANALOG CONVERTER

FEATURES

- COMPLETE D/A CONVERTER:
  INTERNAL REFERENCE
  ±10V OUTPUT OPERATIONAL AMPLIFIER
- ±1/2LSB LINEARITY ERROR
- MONOTONICITY GUARANTEED 0°C TO +70°C
- SETTLING TIME 7μs, MAX
- ±12V to ±15V POWER SUPPLY OPERATION
- 24-PIN MOLDED PLASTIC DIP
- LOWEST COST 12-BIT DAC



DESCRIPTION

The low price of DAC1200KP-V makes this 12-bit resolution D/A converter the best value available for commercial applications.

The DAC1200 offers TTL input compatibility, guaranteed monotonicity over 0°C to +70°C and settling time of 7μsec maximum. It comes complete with internal reference and output operational amplifier.

This precision component is made possible using Burr-Brown's proprietary monolithic integrated circuit process which has been optimized for converter circuits. A stable subsurface reference zener, laser-trimmed thin-film ladder resistors, and high speed current switches combine to give superior performance over the rated temperature range.

DAC1200 is priced and specified for applications where high resolution and monotonocity are the key application parameters and where tightly specified performance over temperature is not required. Because of the low price, it is feasible to use a 12-bit D/A converter for new applications in communications systems, control systems, medical systems, electronic games and personal computer peripherals.

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SPECIFICATIONS

ELECTRICAL

Typical at +25°C and $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V unless otherwise noted

MODEL	DAC1200KP-V	UNITS
INPUTS		
DIGITAL INPUTS		
Input Code[1]	CSB, COB	
Resolution	12	Bits
Digital Logic Inputs[2]:		
V_{IH}, min to max	+2.4 to $+V_{DD}$	V
V_{IL}, min to max	0 to +0.8	V
I_{IH}, V_I = +2.7V, max	+20	μA
I_{IL}, V_I = +0.4V, max	−400	μA
TRANSFER CHARACTERISTICS		
ACCURACY		
Linearity Error, max[3]	±0.018	% of FSR[4]
Differential Linearity Error, max	±0 024	% of FSR
Gain Error, max[5][6]	±0 3	%
Unipolar Offset Error[5][7]	±20	mV
Bipolar Offset Error, max[5][8]	±40	mV
Monotonicity Over 0°C to +70°C[9]	12	Bits
Sensitivity of Gain to Power Supply Variations:		
$+V_{CC}$ and $-V_{CC}$	±0 003	% of FSR/%V_{CC}
V_{DD}	±0 0002	% of FSR/%V_{DD}
TEMPERATURE COEFFICIENTS		
Gain	±10	ppm/°C
Bipolar Offset	±8	ppm of FSR/°C
SETTLING TIME to ±0.012% of FSR[10]		
20V Step and 2kΩ Load, max	7	μsec
OUTPUT		
ANALOG OUTPUT		
Voltage Range, min	±2.5, ±5, ±10, +5, +10	V
Current, min[11][12]	±5	mA
Impedance	0.05	Ω
REFERENCE OUTPUT		
Voltage[13]	+6.3	V_{DD}
Source Current Available for External Loads, max	+1 5	mA
Temperature Coefficient	±10	ppm/°C
POWER SUPPLY REQUIREMENTS		
RATED VOLTAGE		
$+V_{CC}/-V_{CC}$[14]	+15/−15	V
V_{DD}[15]	+5	V
CURRENT (no load), max[16]		
$+V_{CC}/-V_{CC}$	+12/−25	mA
V_{DD}	+10	mA
TEMPERATURE RANGE		
For parameters specified over temp, min to max	0 to +70	°C
Storage, min to max	−60 to +100	°C

NOTES: (1) CSB = Complementary Straight Binary (unipolar), COB = Complementary Offset Binary (bipolar). (2) Digital inputs are TTL-compatible for V_{DD} over the range of +4 5V to $+V_{CC}$. Digital input specs are guaranteed over 0°C to +70°C. These specs are tested at 25°C only (3) ±0.018% of FSR is 3/4LSB at 12 bits. (4) FSR means Full Scale Range and is 20V for a ±10V range. (5) Adjustable to zero with external potentiometer. (6) Adjusting the Gain Adjust potentiometer rotates the transfer function about 0V for unipolar operation and about minus full scale (−FS) for bipolar operation (7) Error at input code FFF_H for unipolar operation (output at 0V). (8) Error at input code FFF_H for bipolar operation (output at minus full scale, −FS) (9) Guaranteed. Tested at 25°C only. (10) Guaranteed. Not tested (11) For operation with supply voltages of less than ±13V, load current must be limited to 1mA. (12) Output may be indefinitely shorted to Common without damage (13) Tolerance is ±5%. (14) Range of operation is ±11.4V to ±16 5V. (15) V_{DD} may be operated up to $+V_{CC}$ Digital input logic threshold remains at +1.4V over the V_{DD} range. (16) Typical power supply currents are about 70% of the maximum.

ABSOLUTE MAXIMUM RATINGS

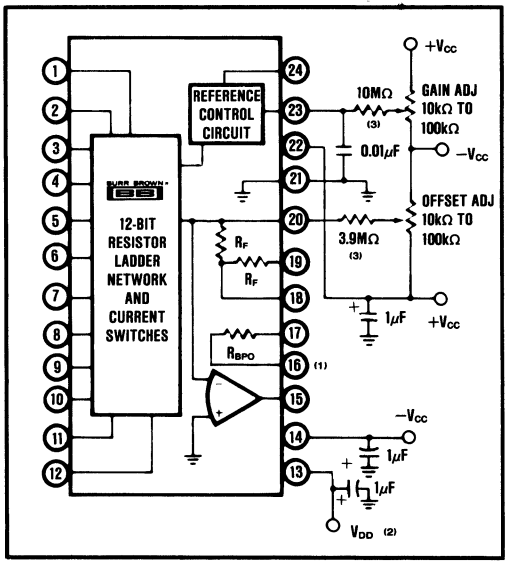
$+V_{CC}$ to Common	0 to +18V
$-V_{CC}$ to Common	0 to −18V
V_{DD} to Common	0 to +7V
Digital Inputs (pins 1—12) to Common	−0.4V to +18V
External Voltage Applied to Range Resistors	±12V
REF OUT	Indefinite short to Common
External Voltage Applied to Analog Output	−5V to +5V
Power Dissipation	1000mW
Operating Temperature	0 to +70°C
Storage Temperature	−60°C to +100°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability

PIN ASSIGNMENTS

Pin	Description	Pin	Description
1	Bit 1 (MSB)	13	Logic Supply, V_{DD}
2	Bit 2	14	$-V_{CC}$
3	Bit 3	15	V_{OUT}
4	Bit 4	16	Reference Input
5	Bit 5	17	Bipolar Offset
6	Bit 6	18	10V Range
7	Bit 7	19	20V Range
8	Bit 8	20	Summing Junction
9	Bit 9	21	Common
10	Bit 10	22	$+V_{CC}$
11	Bit 11	23	Gain Adjust
12	Bit 12 (LSB)	24	6 3V Reference Out

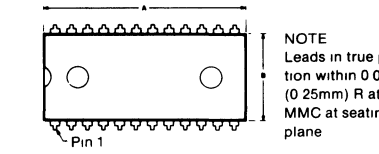
CONNECTION DIAGRAM



	Output Voltage Range Connections				
Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB	19	20	15	24
±5	COB	18	20	NC	24
±2 5V	COB	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

NOTES. (1) Pin 16 is used only to connect the bipolar offset resistor An external reference voltage may not be used. (2) If connected to $+V_{CC}$, which is permissible, power dissipation increases 75mW typ, 100mW max. (3) Values shown are for ±15V supplies For supplies below ±13 5V use 2 7MΩ in place of 3 9MΩ and 7 5MΩ in place of 10MΩ

MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.233	1.283	31.32	32.59
B	.538	575	13 67	14 61
C	.169	.224	4.29	5.69
D	015	.023	0.38	0.58
F	.043	.062	1.09	1.57
G	100 BASIC		2.54 BASIC	
H	.030	090	0.76	2 29
J	.008	.015	0.20	0 38
K	.100	.132	2.54	3 35
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	018	022	0 46	0.56

CASE Plastic
MATING CONNECTOR 0245MC
WEIGHT 3.7 grams (0 13 oz)

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagrams. These capacitors (1μF to 10μF tantalum) should be located close to the DAC1200.

±12V OPERATION

The DAC1200 is fully specified for operation on ±12V power supplies. However, to use the ±10V and 0 to +10V ranges of the voltage output models, the power supplies must be ±13V or greater. All other voltage output ranges and all current output ranges provide satisfactory operation with ±11.4V supplies. The supplies should be balanced to obtain optimum performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in the connection diagrams and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the DAC1200 to prevent noise pick-up. For operation with supplies of less than ±13.5V, use 2.7MΩ and 7.5MΩ resistors in place of the 3.9MΩ and 10MΩ resistors, respectively. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 1, may be substituted in each case. The Gain Adjust (pin 23) is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Common (pin 21) to reduce noise pick-up. Figures 2 and 3 illustrate the relationship of Offset and Gain adjustments to unipolar and bipolar D/A converter output.

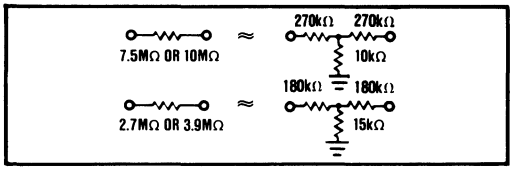


FIGURE 1. Equivalent Resistances.

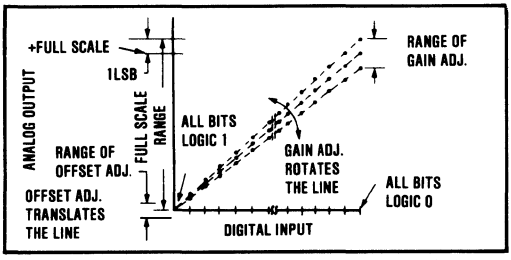


FIGURE 2. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

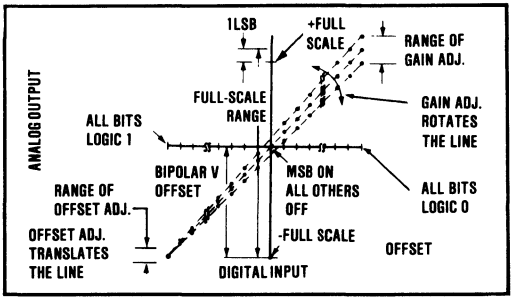


FIGURE 3. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

Offset Adjustment: For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full-scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is −10V. See Table I for corresponding codes. Offset should be adjusted before gain.

Gain Adjustment: For either unipolar or bipolar configurations, apply the digital input that should give the

maximum positive voltage output. Adjust the Gain potentiometer for this positive full-scale voltage. See Table I for positive full-scale voltages.

TABLE I. Digital Input/ Analog Output.

Digital Input	Analog Output	
MSB LSB ↓ ↓	0 to + 10V	±10V
000000000000	+9 9976V	+9 9951V
011111111111	+5 0000V	0 0000V
100000000000	+4 9976V	−0 0049V
111111111111	0 0000V	−10 0000V
One LSB	2 44mV	4 88mV

To obtain values for other ranges
0 to +5V range: divide 0 to +10V range values by 2
±5V range divide ±10V range values by 2
±2 5V range divide ±10V range values by 4.

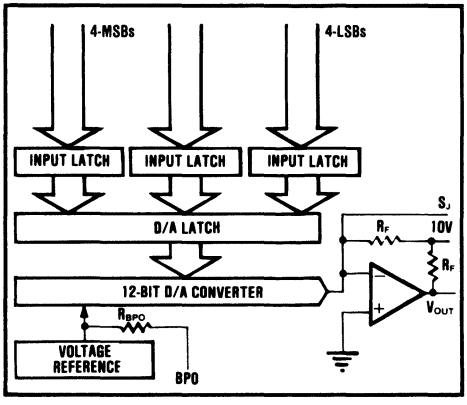
BURR-BROWN®

DAC1201KP-V

Monolithic Microprocessor-Compatible 12-Bit Resolution DIGITAL-TO-ANALOG CONVERTER

FEATURES

- COMPLETE D/A CONVERTER:
  INTERNAL REFERENCE
  ±10V OUTPUT OPERATIONAL AMPLIFIER
- MICROPROCESSOR INTERFACE LOGIC FOR A 4-, 8-, 12- OR 16-BIT BUS
- MONOTONICITY GUARANTEED 0°C to +70°C
- SETTLING TIME 7μs, MAX
- ±12V to ±15V POWER SUPPLY OPERATION
- 28-PIN MOLDED PLASTIC DIP
- LOWEST COST BUFFERED 12-BIT DAC



DESCRIPTION

The low price of DAC1201KP makes this 12-bit resolution D/A converter the best value available for commercial applications requiring a microprocessor interface.

The DAC1201 features microprocessor interface logic, TTL input compatibility, guaranteed monotonicity over 0°C to +70°C and settling time of 7μs maximum.

The interface logic is partitioned in 4-bit nibbles permitting 4-, 8-, 12- and 16-bit bus interface connections for right- or left-justified input words. Dual rank latches permit flexible timing operations for microprocessor control of the DAC1201.

This precision component is made possible using Burr-Brown's proprietary monolithic integrated circuit process which has been optimized for converter circuits. A stable subsurface reference zener, laser-trimmed thin-film ladder resistors, and high speed current switches combine to give superior performance over the rated temperature range.

DAC1201 is priced and specified for applications where high resolution and monotonocity are the key application parameters and where tightly specified performance over temperature is not required. Because of the low price, it is feasible to use this 12-bit D/A converter for new applications in communications systems, electronic controllers, medical instrumentation, electronic games and personal computer peripherals.

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PDS-621B

SPECIFICATIONS

ELECTRICAL

Typical at +25°C and $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V unless otherwise noted

MODEL	DAC1201KP-V	UNITS
INPUTS		
DIGITAL INPUTS		
Input Code[1]	USB, BOB	
Resolution	12	Bits
Digital Logic Inputs[2]		
V_{IH}, min to max	+2 4 to $+V_{CC}$	V
V_{IL}, min to max	0 to +0.8	V
I_{IH}, V_I = +2 7V, max	+20	μA
I_{IL}, V_I = +0 4V, max	±30	μA
TRANSFER CHARACTERISTICS		
ACCURACY		
Linearity Error, max[3]	±0 018	% of FSR[4]
Differential Linearity Error, max	±0 024	% of FSR
Gain Error, max[5][6]	±0.3	%
Unipolar Offset Error[5][7]	±20	mV
Bipolar Offset Error, max[5][8]	±40	mV
Monotonicity Over 0°C to +70°C[9]	12	Bits
Sensitivity of Gain to Power Supply Variations:		
$+V_{CC}$ and $-V_{CC}$	±0.002	% of FSR/%V_{CC}
V_{DD}	±0.006	% of FSR/%V_{DD}
TEMPERATURE COEFFICIENTS		
Gain	±10	ppm/°C
Bipolar Zero[10]	±6	ppm of FSR/°C
SETTLING TIME (to ±0.012% of FSR)[11]		
20V step and 2kΩ load, max	7	μs
OUTPUT		
ANALOG OUTPUT		
Voltage Range, min[12]	±5, ±10, +10	V
Current, min[13]	±5	mA
Impedance	0.2	Ω
REFERENCE OUTPUT		
Voltage[14]	+6.3	V
Source Current Available for External Loads, max	+1.5	mA
Temperature Coefficient	±10	ppm/°C
POWER SUPPLY REQUIREMENTS		
RATED VOLTAGE		
$+V_{CC}/-V_{CC}$[15][16]	+15/−15	V
V_{DD}[17]	+5	V
CURRENT (no load), max[18]		
$+V_{CC}/-V_{CC}$	+25/−35	mA
V_{DD}	+15	mA
TEMPERATURE RANGE		
For parameters specified over temp, min to max	0 to +70	°C
Storage, min to max	−60 to +100	°C

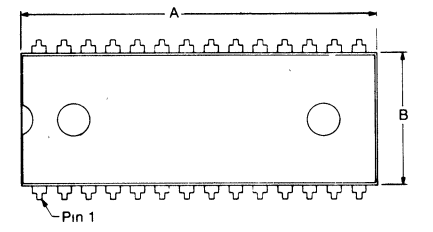
NOTES: (1) USB = Unipolar Straight Binary, BOB = Bipolar Offset Binary. (2) Digital inputs are TTL-compatible for V_{DD} over the range of +4.5V to 5.5V. Digital input specs are guaranteed over 0°C to +70°C. The specs are tested at 25°C only. (3) ±0.018% of FSR is 3/4LSB for 12 bits (4) FSR means Full-Scale Range and is 20V for a ±10V range. (5) Adjustable to zero with external potentiometer. (6) Adjusting the Gain Adjust potentiometer rotates the transfer function about 0V for unipolar operation and about minus full scale (−FS) for bipolar operation. (7) Error at input code 000_H for unipolar operation (output at 0V). (8) Error at input code 000_H for bipolar operation (output at minus full scale, −FS). (9) Guaranteed Tested at 25°C only. (10) Drift at 0V output for bipolar operation (input code 100_H). (11) Guaranteed. Not tested. (12) Minimum supply voltage required for ±10V output swing ±13.5V. Output swing for ±11.4V supplies is at least −8V to +8V. (13) Output may be indefinitely shorted to Common without damage. (14) Tolerance is ±5%. (15) The maximum voltage separation between ACOM and DCOM without affecting accuracy is ±0.5V. (16) Range of operation is ±11 4V to ±16.5V. (17) Range of operation is +4.5V to +5.5V. (18) Typical power supply currents are approximately 70% of the maximum.

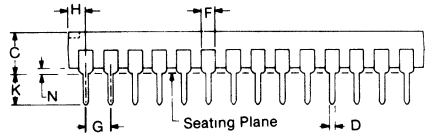
ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to ACOM	0 to +18V
$-V_{CC}$ to ACOM	0 to −18V
V_{DD} to DCOM	0 to +7V
V_{DD} to ACOM	±7V
ACOM to DCOM	±7V
Digital Inputs (pins 2-14, 16-19) to DCOM	−0 4V to +18V
External Voltage Applied to 10V Range Resistor	±12V
REF OUT	Indefinite short to ACOM
External Voltage Applied to Analog Output	−5V to +5V
Power Dissipation	1000mW
Operating Temperature	0°C to +70°C
Storage Temperature	−60°C to +100°C

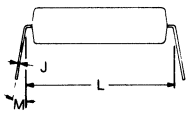
NOTE Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device Exposure to absolute maximum conditions for extended periods may affect device reliability

MECHANICAL





DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1 400	1 460	35 56	37 08
B	530	575	13 46	13 67
C	169	224	4 29	5 70
D	015	023	0 38	0 58
F	043	065	1 09	1 65
G	100 BASIC		2 54 BASIC	
H	030	090	0 76	2 29
J	008	015	0 20	0 38
K	100	136	2 54	3 46
L	600 BASIC		15 24 BASIC	
M	0°	15°	0°	15°
N	018	022	0 46	0 56



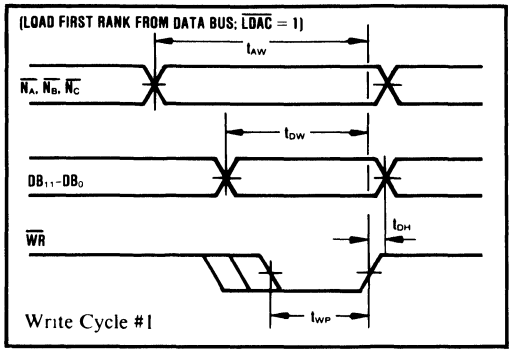
NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

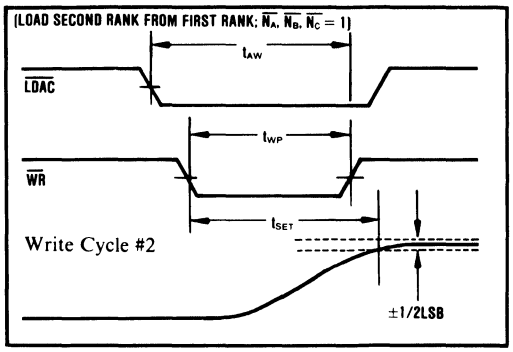
CASE Plastic

MATING CONNECTOR 2803MC

WEIGHT 4 3gm (0 15oz)

TIMING DIAGRAMS





Digital Interface Timing Over Temperature Range

t_{WP}, $\overline{WR}$ pulse width, min	50ns	t_{DW}, data valid to end of $\overline{WR}$, min	80ns
$t_{AW}1$, $\overline{N_X}$ and $\overline{LDAC}$ valid to end of $\overline{WR}$, min	50ns	t_{DH}, data valid hold time, min	0ns

PIN NOMENCLATURE

PIN	NAME	FUNCTION
1	V_{DD}	Logic Supply, +5V
2	$\overline{WR}$	WRITE, command signal to load latches Logic low loads latches
3	$\overline{LDAC}$	LOAD D/A CONVERTER, enables $\overline{WR}$ to load the D/A latch Logic low enables
4	$\overline{N_A}$	NYBBLE A, enables $\overline{WR}$ to load input latch A (the most significant nybble Logic low enables
5	$\overline{N_B}$	NYBBLE B, enables $\overline{WR}$ to load input latch B Logic low enables
6	$\overline{N_C}$	NYBBLE C, enables $\overline{WR}$ to load input latch C (the least significant nybble) Logic low enables
7	D_{11}	DATA, Bit 12, MSB, positive true
8	D_{10}	DATA, Bit 11
9	D_9	DATA, Bit 10
10	D_8	DATA, Bit 9
11	D_7	DATA, Bit 8
12	D_6	DATA, Bit 7
13	D_5	DATA, Bit 6
14	D_4	DATA, Bit 5
15	DCOM	DIGITAL COMMON, V_{DD} supply return
16	D_0	DATA, Bit 1, LSB
17	D_1	DATA, Bit 2
18	D_2	DATA, Bit 3
19	D_3	DATA, Bit 4
20	$+V_{CC}$	Analog Supply Input, +15V or +12V
21	$-V_{CC}$	Analog Supply Input, −15V or −12V
22	GAIN ADJ	To externally adjust gain
23	ACOM	ANALOG COMMON, $\pm V_{CC}$ supply return
24	V_{out}	D/A converter voltage output
25	10V RANGE	Connect to pin 24 for 10V Range
26	SJ	SUMMING JUNCTION of output amplifier
27	BPO	BIPOLAR OFFSET Connect to pin 26 for Bipolar Operation
28	REF OUT	6 3V reference output

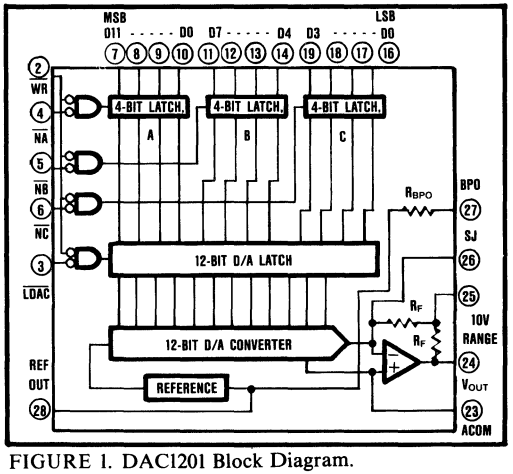


FIGURE 1. DAC1201 Block Diagram.

OPERATION

INTERFACE LOGIC

Input latches A, B, and C hold data temporarily while a complete 12-bit word is assembled before loading into the D/A register. This double-buffered organization prevents the generation of spurious analog output values. Each register is independently addressable.

These input latches are controlled by $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ and $\overline{WR}$. $\overline{N_A}$, $\overline{N_B}$, and $\overline{N_C}$ are internally NORed with $\overline{WR}$ so that the input latches transmit data when both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ are at logic "0". When either $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) or $\overline{WR}$ go to logic "1", the input data is latched into the input registers and held until both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ go to logic "0".

The D/A latch is controlled by $\overline{LDAC}$ and $\overline{WR}$. $\overline{LDAC}$ and $\overline{WR}$ are internally NORed so that the latches

transmit data to the D/A switches when both $\overline{LDAC}$ and $\overline{WR}$ are at logic "0". When either $\overline{LDAC}$ or $\overline{WR}$ are at logic "1", the data is latched in the D/A latch and held until $\overline{LDAC}$ and $\overline{WR}$ go to logic "0".

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When any one of the control signals returns to logic "1", the data is latched. A truth table for all latches is given in Table I.

TABLE I. DAC1201 Interface Logic Truth Table.

WR	N_A	N_B	N_C	LDAC	Operation
1	X	X	X	X	No Operation
0	0	1	1	1	Enables Input Latch 4MSBs
0	1	0	1	1	Enables Input Latch 4 Middle Bits
0	1	1	0	1	Enables Input Latch 4LSBs
0	1	1	1	0	Loads D/A Latch From Input Latches
0	0	0	0	0	All Latches Transparent

"X" = Don't Care.

GAIN AND OFFSET ADJUSTMENTS

Figures 2 and 3 illustrate the relationship of Offset and Gain adjustments to unipolar and bipolar D/A converter output.

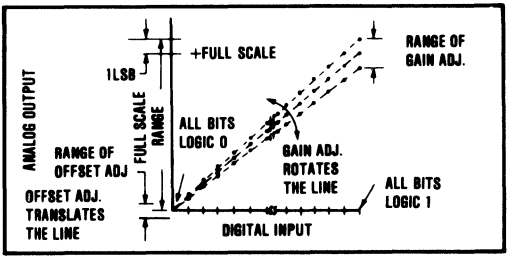


FIGURE 2. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

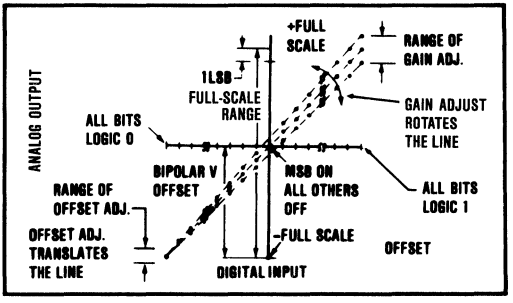


FIGURE 3. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output and adjust the Offset potentiometer for zero output. For bipolar (BOB, BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full-scale voltage. Example: If the full-scale range is connected for 20V, the maximum negative output voltage is −10V. See Table II for corresponding codes.

TABLE II. Digital Input/Analog Output, $\pm V_{CC} = \pm 15V$.

Digital Input	Analog Output		
12-Bit Resolution MSB LSB	0 to + 10V	±5V	±10V
111111111111	+9 9976V	+4.9976V	+9 9951V
100000000000	+5 0000V	0.0000V	0 0000V
011111111111	+4 9976V	−0.0024V	−0 0049V
000000000000	0.0000V	−5 0000V	−10 0000V
1LSB	2 44mV	2 44mV	4 88mV

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the Gain potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages.

±12V OPERATION

The DAC1201 is fully specified for operation on ±12V power supplies. However, in order for the output to swing to ±10V, the power supplies must be ±13.5V or greater. When operating with ±12V supplies, the output swing should be restricted to ±8V in order to meet specifications.

INSTALLATION

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram, Figure 4.

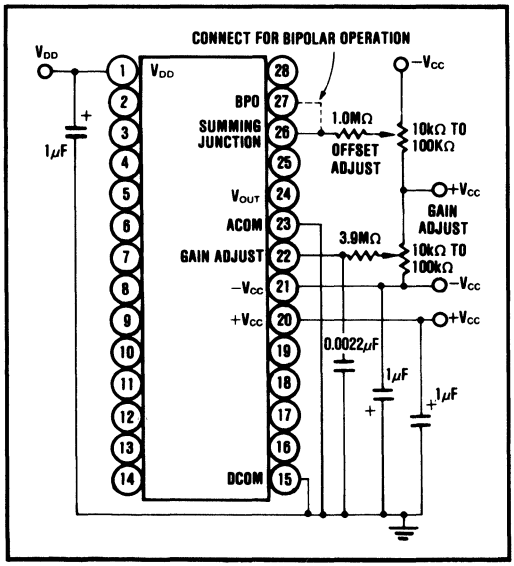


FIGURE 4. Power Supply, Gain, and Offset Potentiometer Connections.

These capacitors (1μF to 10μF tantalum recommended) should be located close to the DAC1201.

The DAC1201 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. The Analog Common (pin 23) and Digital Common (pin 15) should be connected together at one point. Separate returns minimize current flow in low-level signal paths if properly connected. Logic return currents are not added into the analog signal return path. A ±0.5V difference between ACOM and DCOM is permitted for specified operation. High frequency noise on DCOM with respect to ACOM may permit noise to be coupled through to the analog output; therefore, some caution is required in applying these common conections.

The Analog Common is the high quality return for the D/A converter and should be connected directly to the analog reference point of the system. The load driven by the output amplifier should be returned to the Analog Common.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 4. TCR of the potentiometers should be 100ppm/°C or less. The 1.0MΩ and 3.9MΩ resistors (20% carbon or better) should be located close to the DAC1201 to prevent noise pick-up. If it is not convenient to use these high value resistors, and equivalent "T" network, as shown in Figure 5, may be substituted in each case. The Gain Adjust (pin 22) is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Analog Common to reduce noise pick-up in all applications, including those not employing external gain adjustment.

OUTPUT RANGE CONNECTIONS

Internal-scaling resistors provided in the DAC1201 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or unipolar output voltage range of 0 to +10V. The 20V range (±10V bipolar range) is internally connected. Refer to Figure 6. Connections for the output ranges are listed in Table III.

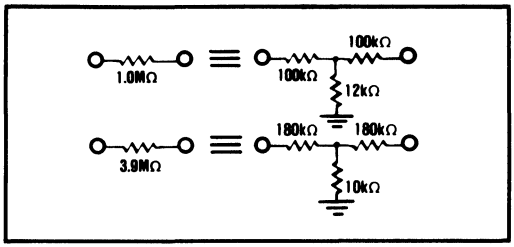


FIGURE 5. Equivalent Resistances.

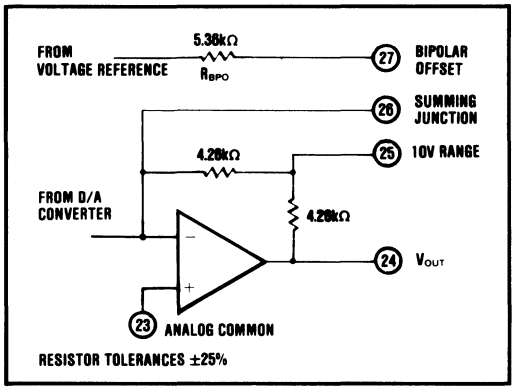


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

TABLE III. Output Range Connections.

Output Range	Digital Input Codes	Connect Pin 25 To	Connect Pin 27 To
0 to +10V	USB	24	23
±5V	BOB or BTC	24	26
±10V	BOB or BTC	NC	26

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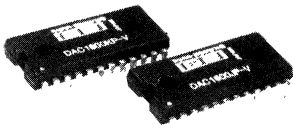


DAC1600

FOR COMMERCIAL APPLICATIONS

Monolithic 16-Bit Resolution DIGITAL-TO-ANALOG CONVERTER

FEATURES

- COMPLETE D/A CONVERTER:
  INTERNAL REFERENCE
  ±10V OUTPUT OPERATIONAL AMPLIFIER
- 14-BIT ACCURACY (K GRADE):
  ±0.003% FSR LINEARITY ERROR
  14-BIT MONOTONICITY GUARANTEED 0°C to +70°C
- SETTLING TIME 10μs, MAX
- ±15V POWER SUPPLY OPERATION
- 24-PIN MOLDED PLASTIC DIP

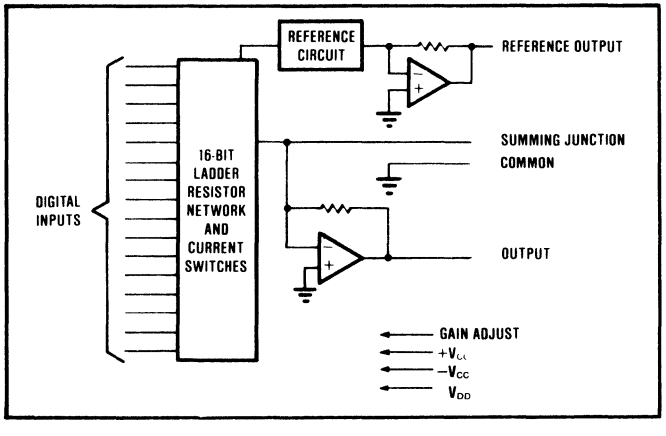
DESCRIPTION

The low prices of DAC1600JP and DAC1600KP make these very-high resolution D/A converters the best value available.

The DAC1600 family offers TTL input compatibility, guaranteed monotonicity (13-bit, J grade; 14-bit, K grade) over 0°C to +70°C and settling time of 10μsec maximum.

This precision component is made possible using Burr-Brown's proprietary monolithic integrated circuit process which has been optimized for converter circuits. A stable subsurface reference zener, laser-trimmed thin-film ladder resistors, and high speed current switches combine to give superior performance over the rated temperature range.

The DAC1600 is priced and specified for applications where high resolution and monotonocity are the key application parameters and where tightly-specified performance over temperature is not required. Because of the low price, it is feasible to use a 16-bit D/A converter for new applications in communications systems, electronic controllers, electronic games, and personal computer peripherals.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable BBRCORP - Telex. 66-6491

SPECIFICATIONS

ELECTRICAL

Typical at +25°C. $\pm V_{CC}$ = 15V, V_{DD} = +5V unless otherwise noted.

MODEL	DAC1600JP-V	DAC1600KP-V	UNITS
INPUTS			
DIGITAL INPUTS			
Input Code[1]	COB		
Resolution, max	16	*	Bits
Digital Logic Inputs[2]			
V_{IH}, min to max	+2 4 to +V_{DD}	*	V
V_{IL}, min to max	−1.0 to +0 8	*	V
I_{IH}, V_I = +2 7V, max	+40	*	µA
I_{IL}, V_I = +0.4V, max	−0 5	*	mA
TRANSFER CHARACTERISTICS			
ACCURACY			
Linearity Error, max[3]	±0 006	±0 003	% of FSR[4]
Differential Linearity Error, max	±0 012	±0.006	% of FSR
Gain Error, max[5][6]	±0 3	*	%
Bipolar Zero Error, max[5]	40	*	mW
Monotonicity Over 0°C to +70°C[7]	13	14	Bits
Sensitivity of Gain to Power Supply Variations			
±V_{CC}	±0.002	*	% of FSR/%V_{CC}
V_{DD}	±0 0002	*	% of FSR/%V_{DD}
TEMPERATURE COEFFICIENTS			
Gain	±10	*	ppm/°C
Bipolar Zero	±5	*	ppm of FSR/°C
SETTLING TIME (to ±0 003% of FSR)[8], 10V step and 2kΩ load, max	10	*	µsec
OUTPUT			
ANALOG OUTPUT			
Voltage Range, min	±10	*	V
Current, min[9]	±5	*	mA
Impedance	0 15	*	Ω
REFERENCE OUTPUT			
Voltage[10]	+6 3	*	V
Source Current Available for External Loads, max	+1 5	*	mA
Temperature Coefficient	±10	*	ppm/°C
POWER SUPPLY REQUIREMENTS			
RATED VOLTAGE			
±V_{CC}[11]	15	*	V
V_{DD}[12]	+5	*	V
CURRENT, max[13]			
±V_{CC}	35	*	mA
V_{DD}	8	*	mA
TEMPERATURE RANGE			
For parameters specified over temp, min/max	0 to +70	*	°C
Storage, min/max	−60 to +100	*	°C

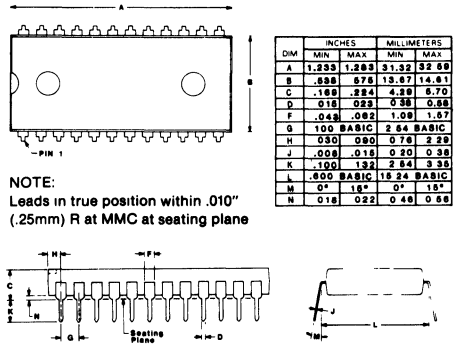
NOTES (1) COB = Complementary Offset Binary (2) Digital inputs are TTL-compatible for V_{DD} over the range of +4 5V to +V_{CC} Digital input specs are guaranteed over 0°C to +70°C These specs are tested at 25°C only (3) ±0 003% of FSR is 1/2LSB at 14 bits (4) FSR means Full Scale Range and is 20V for a ±10V range (5) Adjustable to zero with external potentiometer. (6) Adjusting the gain potentiometer rotates the transfer function around Bipolar Zero, 0V (Input Code 7FFF$_H$) (7) Guaranteed Tested at 25°C only (8) Guaranteed Not tested (9) Output may be indefinitely shorted to Common without damage (10) Tolerance is ±5% (11) Range of operation is ±13 5V to ±16 5V (12) V_{DD} may be operated up to +V_{CC}. Digital input logic threshold remains at +1 4V over the V_{DD} range (13) Typical power supply currents are about 50% of the maximum

ABSOLUTE MAXIMUM RATINGS

+V_{CC} to Common	0V, +18V
−V_{CC} to Common	0V, −18V
V_{DD} to Common	0V, +18V
Digital Data Inputs to Common	−1V, +18V
Reference Out to Common	Indefinite Short to Common
External Voltage Applied to D/A Output	−5V to +5V
V_{OUT}	Indefinite Short to Common
Power Dissipation	1000mW
Storage Temperature	−60°C to +100°C

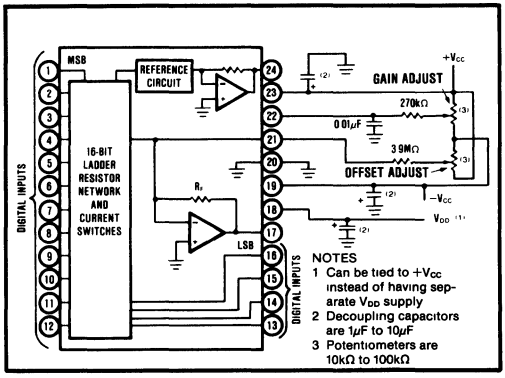
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.233	1.283	31.32	32 69
B	.538	575	13.67	14.61
C	.160	.224	4.06	5.70
D	018	023	0 38	0.58
F	.040	.062	1.06	1.57
G	100 BASIC		2 54 BASIC	
H	030	080	0 76	2 29
J	.008	.015	0 20	0 38
K	.100	132	2 54	3 35
L	.600 BASIC		15 24 BASIC	
M	0°	15°	0°	15°
N	018	022	0 46	0 56

CONNECTION DIAGRAM



ORDERING INFORMATION

Model	Linearity Error & Monotonicity for
DAC1600JP-V	13 bits
DAC1600KP-V	14 bits

PIN ASSIGNMENTS

Pin	Description	Pin	Description
1	Bit 1 (MSB)	13	Bit 13
2	Bit 2	14	Bit 14
3	Bit 3	15	Bit 15
4	Bit 4	16	Bit 16 (LSB)
5	Bit 5	17	V_{OUT}
6	Bit 6	18	V_{DD}
7	Bit 7	19	$-V_{CC}$
8	Bit 8	20	Common
9	Bit 9	21	Summing Junction (Zero Adjust)
10	Bit 10	22	Gain Adjust
11	Bit 11	23	$+V_{CC}$
12	Bit 12	24	+6.3V Reference Output

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1μF to 10μF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 1, may be substituted in place of the 3.9MΩ part. A 0.001μF to 0.01μF ceramic capacitor should be connected from Gain Adjust to Common to prevent noise pickup. See Figure 2 for relationship of zero and gain adjustment.

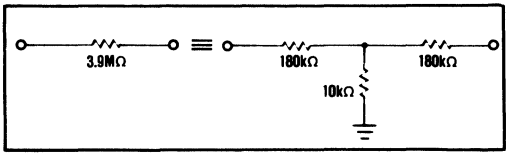


FIGURE 1. Equivalent Resistances.

Zero Adjustment

Apply the digital input code that produces zero output voltage or current. See Table I for corresponding codes and the Connection Diagram for zero adjustment circuit connections. Zero calibration should be made before gain calibration.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table I for positive full scale voltages and the Connection Diagram for gain adjustment circuit connections.

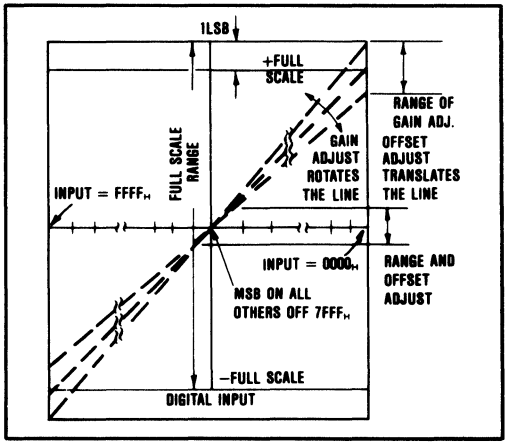


FIGURE 2. Relationship of Zero and Gain Adjustment.

TABLE I. Calibration Table.

Digital Input	Description	Analog Output		
		16-bit	15-bit	15-bit
One LSB	One LSB	305μV	610μV	1224μV
0000$_H$	+ Full Scale	+9.99960V	9.99939V	+9.99878V
7FFF$_H$	Bipolar Zero	0V	0V	0V
FFFF$_H$	– Full Scale	–10.00000V	–10.00000V	–10.00000V

INSTALLATION CONSIDERATIONS

This D/A converter family is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bit 15 and bit 16 should be connected to V_{DD} through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a 20V full-scale range, 1LSB is 305μV. With a load current of 5mA, series wiring and connector resistances of only 60mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a sytem layout, the resistance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 18 inches of wire will produce a 1/2LSB error in the analog output voltage!

In Figure 3 lead and contact resistances are represented by R_1 through R_3. As long as the load resistance R_L is constant, R_1 simply introduces a gain error and can be removed during initial calibration. R_2 is part of R_L, if the output voltage is sensed at Common, and therefore introduces no error. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_3 is negligible.

In many applications it is impractical to sense the output voltage at the output pin. Sensing the output voltage at the system ground point is permissible with the DAC1600 family because the D/A converter is designed to have a constant return current of approximately 2mA flowing from Common. The variation in this current is under 20μA (with changing input codes), therefore R_3 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_3 ($R_3 \times 2mA$) appears as zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figure 3.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a single lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

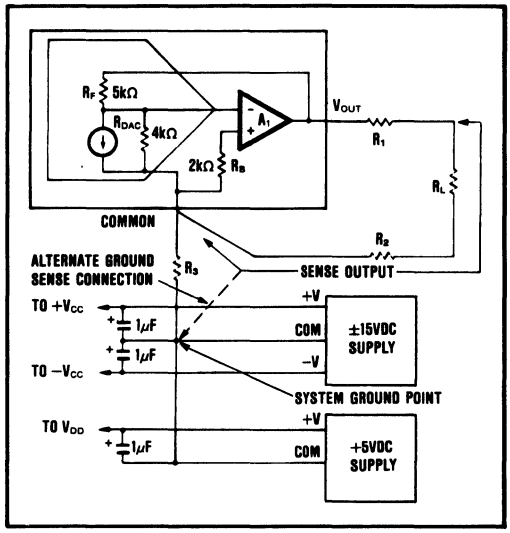
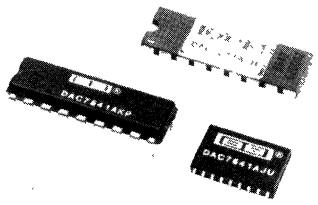


FIGURE 3. Output Circuit.

BURR-BROWN®



DAC7541A

AVAILABLE IN DIE FORM

Low Cost 12-Bit CMOS Four-Quadrant Multiplying DIGITAL-TO-ANALOG CONVERTER

FEATURES

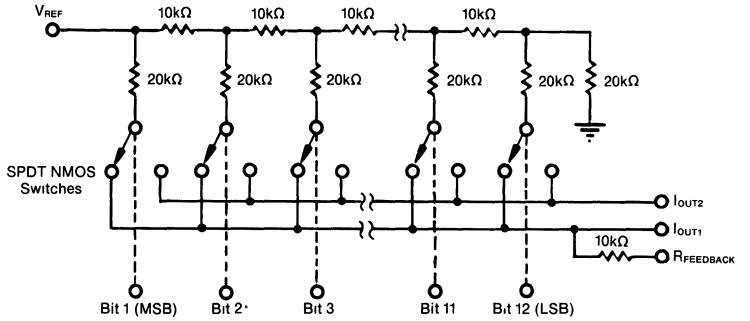
- FULL FOUR-QUADRANT MULTIPLICATION
- 12-BIT END-POINT LINEARITY
- DIFFERENTIAL LINEARITY ±1/2LSB MAX OVER TEMPERATURE (K/B/T GRADES)
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- TTL-/CMOS-COMPATIBLE
- SINGLE +5V TO +15V SUPPLY
- LATCH-UP RESISTANT
- 7521/7541/7541A REPLACEMENT
- PACKAGES: HERMETIC DIP, PLASTIC DIP, PLASTIC SOIC
- LOW COST

DESCRIPTION

The Burr-Brown DAC7541A is a low cost 12-bit, four-quadrant multiplying digital-to-analog converter. Laser-trimmed thin-film resistors on a monolithic CMOS circuit provide true 12-bit integral and differential linearity over the full specified temperature ranges.

The DAC7541A is a direct, improved pin-for-pin replacement for 7521, 7541, and 7541A industry standard parts. In addition to standard 18-pin plastic and hermetic ceramic packages, the DAC7541A is also available in a surface-mount plastic 18-pin SOIC.

FUNCTIONAL DIAGRAM



Digital Inputs (DTL/TTL/CMOS compatible)
Logic A switch is closed to I_{OUT1} for its digital input in a "high" state.

Switches shown for digital inputs "high"

International Airport Industrial Park • P.O. Box 11400 • Tucson, Arizona 85734 • Tel.: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491

PDS-639A

SPECIFICATIONS

ELECTRICAL

At +25°C, $+V_{DD}$ = +12V or +15V, V_{REF} = +10V, $V_{PIN\ 1} = V_{PIN\ 2}$ = 0V unless otherwise specified

MODEL		DAC7541A			
PARAMETER	GRADE	T_A = +25°C	$T_A = T_{MIN}, T_{MAX}$[1]	UNITS	TEST CONDITIONS/COMMENTS
ACCURACY					
Resolution	All	12	12	Bits	
Relative Accuracy	J, A, S	±1	±1	LSB max	±1LSB = ±0 024% of FSR
	K, B, T	±1/2	±1/2	LSB max	±1/2LSB = ±0 012% of FSR
Differential Non-linearity	J, A, S	±1	±1	LSB max	All grades guaranteed monotonic to
	K, B, T	±1/2	±1/2	LSB max	12 bits, T_{MIN} to T_{MAX}
Gain Error	J, A, S	±6	±8	LSB max	Measured using internal R_{FB} and includes
	K, B, T	±1	±3	LSB max	effect of leakage current and gain T C
					Gain error can be trimmed to zero
Gain Temperature Coefficient					
(ΔGain/ΔTemperature)	All		5	ppm/°C max	Typical value is 2ppm/°C
Output Leakage Current Out_1 (Pin 1)	J, K	±5	±10	nA max	All digital inputs = 0V
	A, B	±5	±10	nA max	
	S, T	±5	±200	nA max	
Out_2 (Pin 2)	J, K	±5	±10	nA max	All digital inputs = V_{DD}
	A, B	±5	±10	nA max	
	S, T	±5	±200	nA max	
REFERENCE INPUT					
Voltage (Pin 17 to GND)	All	−10/+10	−10/+10	V min/max	
Input Resistance (Pin 17 to GND)	All	7-18	7-18	kΩ min/max	Typical input resistance = 11kΩ
					Typical input resistance temperature
					coefficient is −50ppm/°C
DIGITAL INPUTS					
V_{IH} (Input **High** Voltage)	All	2 4	2 4	V min	
V_{IL} (Input **Low** Voltage)	All	0 8	0.8	V max	
I_{IN} (Input Current)	All	±1	±1	μA max	Logic inputs are MOS gates
					I_{IN} typ (25°C) = 1nA
C_{IN} (Input Capacitance)[2]	All	8	8	pF max	V_{IN} = 0V
POWER SUPPLY REJECTION					
ΔGain/ΔV_{DD}	All	±0 01	±0 02	% per % max	V_{DD} = +11 4V to +16V
POWER SUPPLY					
V_{DD} Range	All	+5 to +16	+5 to +16	V min to V max	Accuracy is not guaranteed over this range
I_{DD}	All	2	2	mA max	All digital inputs V_{IL} or V_{IH}
		100	500	μA max	All digital inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not production tested
V_{DD} = +15V, V_{REF} = +10V except where stated, $V_{PIN\ 1} = V_{PIN\ 2}$ = 0V, output amp is OPA606 except where stated

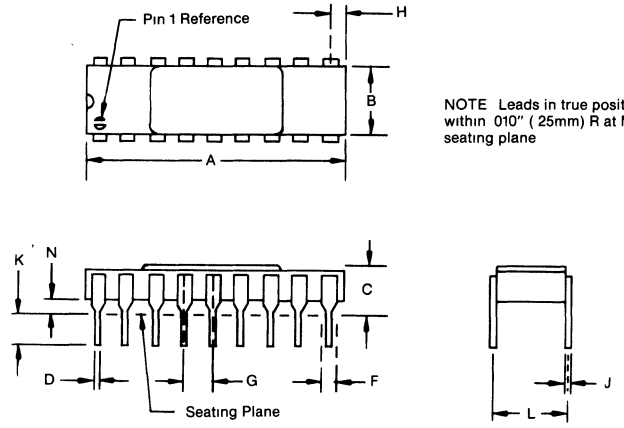
PROPAGATION DELAY (from Digital Input change to 90% of Final Analog Output)	All	100	—	ns typ	Out_1 Load = 100Ω, C_{EXT} = 13pF Digital Inputs = 0V to V_{DD} or V_{DD} to 0V
DIGITAL-TO-ANALOG GLITCH IMPULSE	All	1000	—	nV-s typ	V_{REF} = 0V, all digital inputs 0V to V_{DD} or V_{DD} to 0V Measured using OPA606 as output amplifier
MULTIPLYING FEEDTHROUGH ERROR (V_{REF} to Out_1)	All	1.0	—	mVp-p max	V_{REF} = ±10V, 10kHz sine wave
OUTPUT CURRENT SETTLING TIME	All	0 6	—	μs typ	To 0 01% of Full Scale Range Out_1 load = 100Ω, C_{EXT} = 13pF
	All	1 0	—	μs max	Digital inputs 0V to V_{DD} or V_{DD} to 0V
OUTPUT CAPACITANCE					
$C_{OUT\ 1}$ (Pin 1)	All	100	100	pF max	Digital Inputs = V_{IH}
$C_{OUT\ 2}$ (Pin 2)	All	60	60	pF max	Digital Inputs = V_{IH}
$C_{OUT\ 1}$ (Pin 1)	All	70	70	pF max	Digital Inputs = V_{IL}
$C_{OUT\ 2}$ (Pin 2)	All	100	100	pF max	Digital Inputs = V_{IL}

NOTES (1) Temperature ranges are 0 to +70°C for JP, KP, JU and KU versions; −25°C to +85°C for AH, BH versions, −55°C to +125°C for SH, TH versions (2) Guaranteed by design but not production tested

MECHANICAL

H Package–18-Pin Hermetic DIP

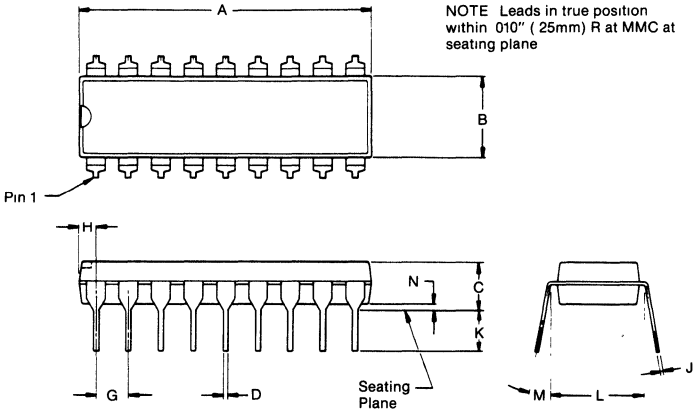
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	960	—	24 38
B	220	310	5 59	7 87
C	—	200	—	5 08
D	014	023	0 36	0 58
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	—	098	—	2 49
J	008	015	0 20	0 38
K	125	200	3 18	5 08
L	290	320	7 37	8 13
N	015	080	0 38	2 03



NOTE Leads in true position within 010" (25mm) R at MMC at seating plane

P Package–18-Pin Plastic DIP

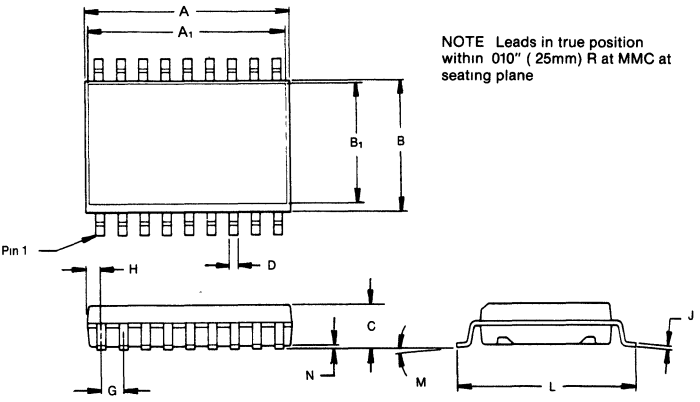
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	840	940	21 34	23 88
B	240	280	6 10	7 11
C	—	210	—	5 33
D	014	022	0 36	0 56
G	100 BASIC		2 54 BASIC	
H	040	060	1 02	1 52
J	008	015	0 20	0 38
K	115	150	2 92	3 81
L	280	300	7 11	7 62
M	0°	10°	0°	10°
N	0 020	0 050	0 51	1 27



NOTE Leads in true position within 010" (25mm) R at MMC at seating plane

U Package–18-Pin Plastic SOIC

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	450	466	11 43	11 84
A_1	443	446	11 25	11 33
B	286	302	7 26	7 67
B_1	270	285	6 86	7 24
C	093	108	2 36	2 74
D	015	019	0 38	0 48
G	050 BASIC		1 27 BASIC	
H	026	034	0 66	0 86
J	008	012	0 20	0 30
L	390	422	9 91	10 72
M	0°	10°	0°	10°
N	000	012	0 00	0 30



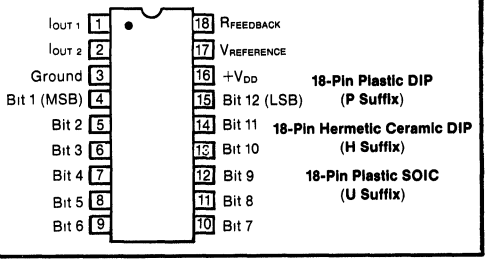
NOTE Leads in true position within 010" (25mm) R at MMC at seating plane

ABSOLUTE MAXIMUM RATINGS*

V_{DD} (pin 16) to Ground	+17V
V_{REF} (pin 17) to Ground	±25V
V_{RFB} (pin 18) to Ground	±25V
Digital Input Voltage (pins 4-15) to Ground	−0.4V, V_{DD}
$V_{PIN\ 1}$, $V_{PIN\ 2}$ to Ground	−0.4V, V_{DD}
Power Dissipation (any package):	
To +75°C	450mW
Derates above +75°C	−6mW/°C
Lead Temperature (soldering, 10s)	+300°C
Storage Temperature: Ceramic Package	+150°C
Plastic Package	+125°C

*Stresses above those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONNECTIONS



CAUTION

The DAC7541A is an ESD (electrostatic discharge) sensitive device. The digital control inputs have a special FET structure, which turns on when the input exceeds the supply by 18V, to minimize ESD damage. However, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

BURN-IN SCREENING

Burn-in screening is an option available for the models in the Ordering Information table. Burn-in duration is 160 hours at the indicated temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

ORDERING INFORMATION

Model	Package	Temperature Range	Relative Accuracy (LSB)	Gain Error (LSB)
DAC7541AJP	Plastic DIP	0°C to +70°C	±1	±6
DAC7541AKP	Plastic DIP	0°C to +70°C	±1/2	±1
DAC7541AJU	Plastic SOIC	0°C to +70°C	±1	±6
DAC7541AKU	Plastic SOIC	0°C to +70°C	±1/2	±1
DAC7541AAH	Hermetic DIP	-25°C to +85°C	±1	±6
DAC7541ABH	Hermetic DIP	-25°C to +85°C	±1/2	±1
DAC7541ASH	Hermetic DIP	-55°C to +125°C	±1	±6
DAC7541ATH	Hermetic DIP	-55°C to +125°C	±1/2	±1

BURN-IN SCREENING OPTION
See text for details

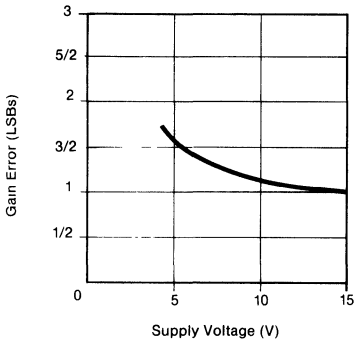
Model	Package	Temperature Range	Relative Accuracy (LSB)	Burn-In Temp. (160 Hours)[1]
DAC7541AJP-BI	Plastic DIP	0°C to +70°C	±1	+85°C
DAC7541AKP-BI	Plastic DIP	0°C to +70°C	±1/2	+85°C
DAC7541AJU-BI	Plastic SOIC	0°C to +70°C	±1	+85°C
DAC7541AKU-BI	Plastic SOIC	0°C to +70°C	±1/2	+85°C
DAC7541AAH-BI	Hermetic DIP	-25°C to +85°C	±1	+125°C
DAC7541ABH-BI	Hermetic DIP	-25°C to +85°C	±1/2	+125°C
DAC7541ASH-BI	Hermetic DIP	-55°C to +125°C	±1	+125°C
DAC7541ATH-BI	Hermetic DIP	-55°C to +125°C	±1/2	+125°C

NOTE (1) Or equivalent combination of time and temperature

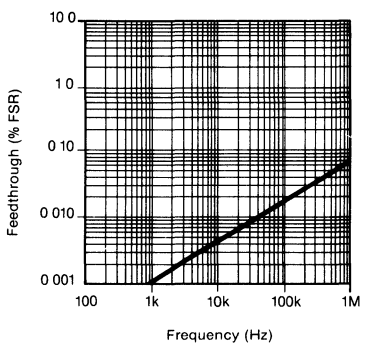
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{DD} = +15V unless otherwise noted

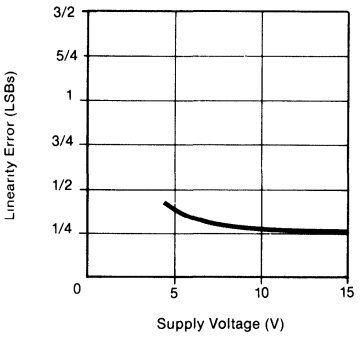
GAIN ERROR VS SUPPLY VOLTAGE



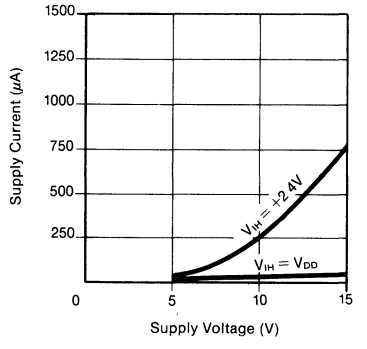
FEEDTHROUGH ERROR VS FREQUENCY



LINEARITY VS SUPPLY VOLTAGE



SUPPLY CURRENT VS SUPPLY VOLTAGE



DISCUSSION OF SPECIFICATIONS

Relative Accuracy

This term (also known as linearity) describes the transfer function of analog output to digital input code. The linearity error describes the deviation from a straight line between zero and full scale.

Differential Nonlinearity

Differential Nonlinearity is the deviation from an ideal 1LSB change in the output, from one adjacent output state to the next. A differential nonlinearity specification of ±1.0LSB guarantees monotonicity.

Gain Error

Gain error is the difference in measure of full-scale output versus the ideal DAC output. The ideal output for the DAC7541A is $-(4095/4096) \times (V_{REF})$. Gain error may be adjusted to zero using external trims.

Output Leakage Current

The measure of current which appears at Out_1 with the DAC loaded with all zeros, or at Out_2 with the DAC loaded to all ones.

Multiplying Feedthrough Error

This is the AC error output due to capacitive feedthrough from $V_{REFERENCE}$ to Out_1 with the DAC loaded to all zeros. This test is performed at 10kHz.

Output Current Settling Time

This is the time required for the output to settle to a tolerance of ±0.5LSB of final value from a change in code of all zeros to all ones, or all ones to all zeros.

Propagation Delay

This is the measure of the delay of the internal circuitry and is measured as the time from a digital code change to the point at which the output reaches 90% of final value.

Digital-to-Analog Glitch Impulse

This is the measure of the area of the glitch energy measured in nV-seconds. Key contributions to glitch energy are digital word-bit timing differences, internal circuitry timing differences, and charge injected from digital logic.

The measurement is performed with $V_{REFERENCE}$ = Ground, an OPA606 as the output op amp, and C_1 (phase compensation) = 0pF.

Monotonicity

Monotonicity assures that the analog output will increase or stay the same for increasing digital input codes. The DAC7541A is guaranteed monotonic to 12 bits.

Power Supply Rejection

Power supply rejection is the measure of the sensitivity of the output (full scale) to a change in the power supply voltage.

CIRCUIT DESCRIPTION

The DAC7541A is a 12-bit multiplying D/A converter consisting of a highly stable thin-film R-2R ladder network and 12 pairs of current steering switches on a monolithic chip. Most applications require the addition of a voltage or current reference and an output operational amplifer.

A simplified circuit of the DAC7541A is shown in Figure 1. The R-2R inverted ladder binarily divides the input currents that are switched between $I_{OUT\ 1}$ and $I_{OUT\ 2}$ bus lines. This switching allows a constant current to be maintained in each ladder leg independent of the input code.

The input resistance at $V_{REFERENCE}$ (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the $V_{REFERENCE}$ pin is constant, the reference terminal can be driven by a reference voltage or a reference current, AC or DC, of positive or negative polarity.

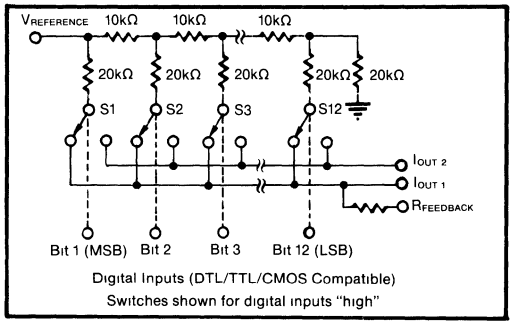


FIGURE 1. Simplified DAC Circuit.

EQUIVALENT CIRCUIT ANALYSIS

Figures 2 and 3 show the equivalent circuits for all digital inputs low and high respectively. The reference current is switched to $I_{OUT\ 2}$ when all inputs are low and $I_{OUT\ 1}$ when inputs are high. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate; the 1/4096 current source represents the constant one-bit current drain through the ladder terminating resistor. The output capacitance is dependent upon the digital input code, and is therefore modulated between the low and high values.

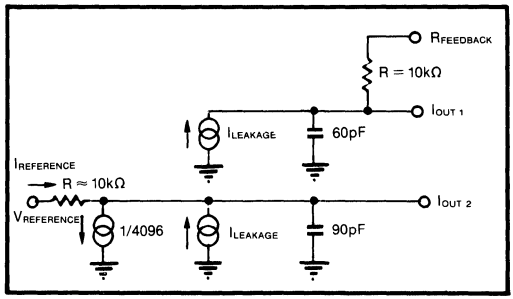


FIGURE 2. DAC7541A Equivalent Circuit (All Inputs Low).

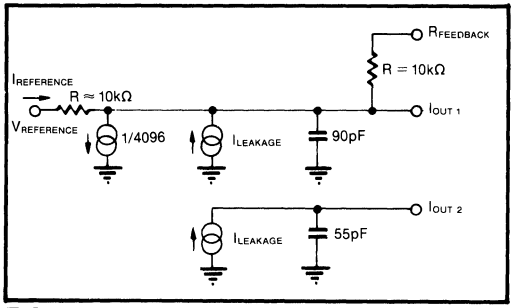


FIGURE 3. DAC7541A Equivalent Circuit (All Inputs High).

DYNAMIC PERFORMANCE

Output Impedance

The output resistance, as in the case of the output capacitance, is also modulated by the digital input code. The resistance looking back into the $I_{OUT\ 1}$ terminal may be anywhere between 10kΩ (the feedback resistor alone when all digital inputs are low) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is high).The static accuracy and dynamic performance will be affected by this modulation. The gain and phase stability of the output amplifier, board layout, and power supply decoupling will all affect the dynamic performance of the DAC7541A. The use of a compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifier's feedback resistor to provide the necessary phase compensation to critically dampen the output. See Figures 4 and 6.

APPLICATIONS

OP AMP CONSIDERATIONS

The input bias current of the op amp flows through the feedback resistor, creating an error voltage at the output of the op amp. This will show up as an offset through all

codes of the transfer characteristics. A low bias current op amp such as the OPA606 is recommended.

Low offset voltage and V_{OS} drift are also important. The output impedance of the DAC is modulated with the digital code. This impedance change (approximately 10kΩ to 30kΩ) is a change in closed-loop gain to the op amp. The result is that V_{OS} will be multiplied by a factor of one to two depending on the code. This shows up as a linearity error. Offset can be adjusted out using Figure 4. Gain may be adjusted using Figure 5.

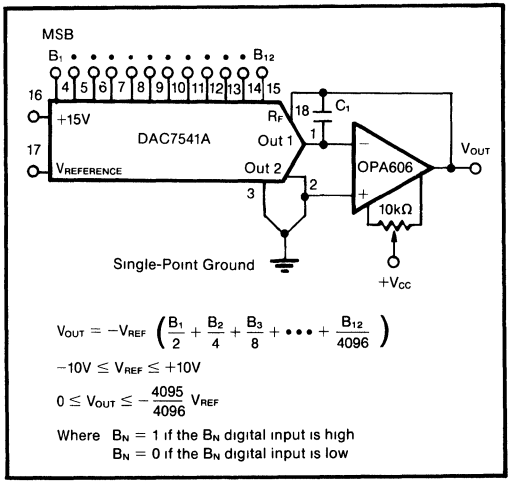


FIGURE 4. Basic Connection With Op Amp V_{OS} Adjust: Unipolar (two-quadrant) Multiplying Configuration.

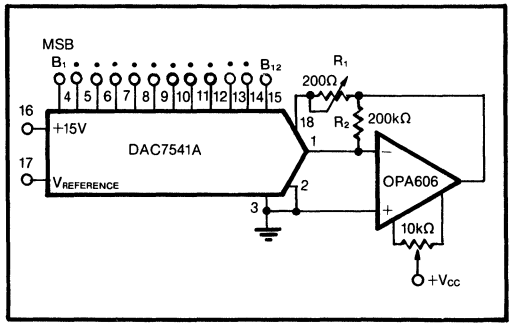


FIGURE 5. Basic Connection with Gain Adjust (allows adjustment up or down).

UNIPOLAR BINARY OPERATION (TWO-QUADRANT MULTIPLICATION)

Figure 4 shows the analog circuit connections required for unipolar binary (two-quadrant multiplication) operation. With a DC reference voltage or current (positive or negative polarity) applied at pin 17, the circuit is a unipolar D/A converter. With an AC reference voltage or current, the circuit provides two-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table I.

C_1 phase compensation (10 to 25pF) in Figure 4 may be required for stability when using high speed amplifiers. C_1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at Out_1.

TABLE I. Unipolar Codes.

Binary Input	Analog Output
MSB LSB	
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096)
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	0 Volts

R_1 in Figure 5 provides full scale trim capability—load the DAC register to 1111 1111 1111, adjust R_1 for $V_{OUT} = -V_{REF}$ (4095/4096). Alternatively, full scale can be ajdusted by omitting R_1 and R_2 and trimming the reference voltage magnitude.

BIPOLAR FOUR-QUADRANT OPERATION

Figure 6 shows the connections for bipolar four-quadrant operation. Offset can be adjusted with the A_1 to A_2 summing resistor, with the input code set to 1000 0000 0000. Gain may be adjusted by varying the feedback resistor of A_2. The input/output relationship is shown in Table II.

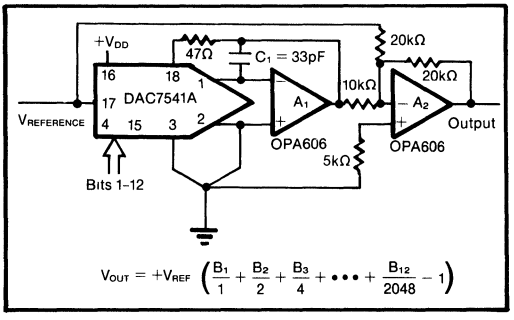


FIGURE 6. Bipolar Four-Quadrant Multiplier.

TABLE II. Bipolar Codes.

Binary Input	Analog Output
MSB LSB	
1111 1111 1111	$+V_{REF}$ (2047/2048)
1000 0000 0000	0 Volts
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048)

DIGITALLY CONTROLLED GAIN BLOCK

The 7541A may be used in a digitally controlled gain block as shown in Figure 7. This circuit gives a range of gain from one (all bits = one) to 4096 (LSB = one). The transfer function is:

$$V_{OUT} = \frac{-V_{IN}}{\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \bullet\bullet\bullet + \frac{B_{12}}{4096}\right)}$$

All bits off is an illegal state, as division by zero is impossible (no op amp feedback). Also, errors increase as gain increases, and errors are minimized at major carries (only one bit on at a time).

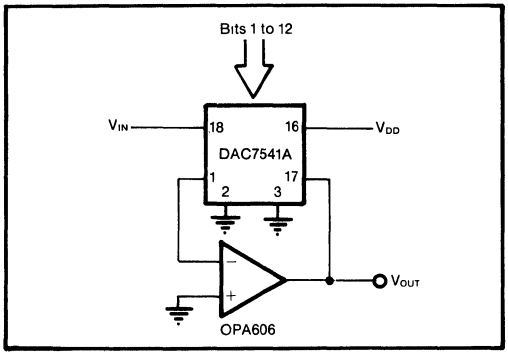
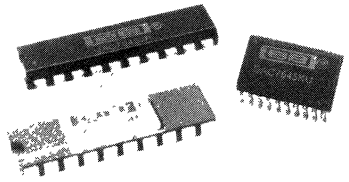


FIGURE 7. Digitally Programmable Gain Block.

BURR-BROWN®



DAC7545

CMOS 12-Bit Multiplying DIGITAL-TO-ANALOG CONVERTER Microprocessor Compatible

FEATURES

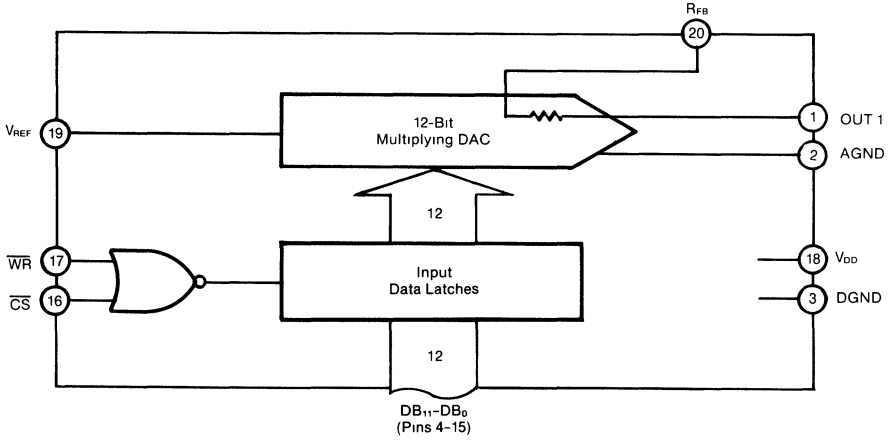
- FOUR-QUADRANT MULTIPLICATION
- LOW GAIN TC: 2PPM/°C typ
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- SINGLE 5V TO 15V SUPPLY
- TTL/CMOS LOGIC COMPATIBLE
- LOW OUTPUT LEAKAGE: 10nA max
- LOW OUTPUT CAPACITANCE: 70pF max
- DIRECT REPLACEMENT FOR AD7545, PM-7545

DESCRIPTION

The DAC7545 is a low-cost CMOS, 12-bit four-quadrant multiplying, digital-to-analog converter with input data latches. The input data is loaded into the DAC as a 12-bit data word. The data flows through to the DAC when both the chip select ($\overline{CS}$) and the write ($\overline{WR}$) pins are at a logic low.

Laser-trimmed thin-film resistors and excellent CMOS voltage switches provide true 12-bit integral and differential linearity. The device operates on a single +5V to +15V supply and is available in 20-pin side-brazed DIP, 20-pin plastic DIP or a 20-lead plastic SOIC package. Devices are specified over the commercial, industrial, and military temperature ranges and are available with additional reliability screening.

The DAC7545 is well suited for battery or other low power applications because the power dissipation is less than 0.5mW when used with CMOS logic inputs and $V_{DD} = +5V$.



International Airport Industrial Park - P O Box 11400 - Tucson, Arizona 85734 - Tel (602) 746-1111 - Twx 910-952-1111 - Cable BBRCORP - Telex. 66-6491

PDS-747A

SPECIFICATIONS

ELECTRICAL

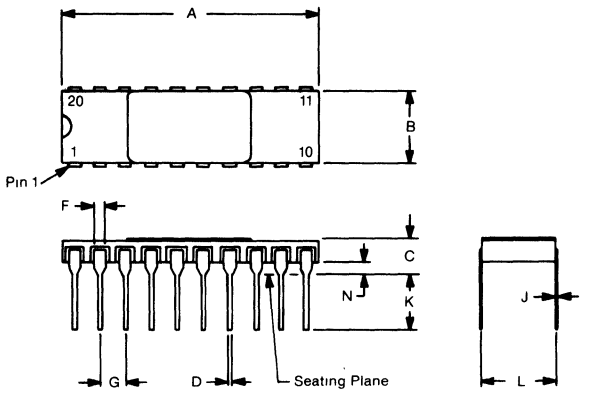
V_{REF} = +10V, $V_{OUT\,1}$ = 0V, ACOM = DCOM unless otherwise specified

MODEL		DAC7545					
		V_{DD} = +5V		V_{DD} = +15V		UNITS	
PARAMETER	GRADE	T_A = +25°C	T_{MIN}-T_{MAX}[1]	T_A = +25°C	T_{MIN}-T_{MAX}[1]	(max)	TEST CONDITIONS/COMMENTS
STATIC PERFORMANCE							
Resolution	All	12	12	12	12	Bits	
Relative Accuracy	J, A, S	±2	±2	±2	±2	LSB	
	K, B, T	±1	±1	±1	±1	LSB	
	L, C, U	±1/2	±1/2	±1/2	±1/2	LSB	
	GL, GC, GU	±1/2	±1/2	±1/2	±1/2	LSB	
Differential Nonlinearity	J, A, S	±4	±4	±4	±4	LSB	10-bit monotonic, T_{MIN} to T_{MAX}
	K, B, T	±1	±1	±1	±1	LSB	12-bit monotonic, T_{MIN} to T_{MAX}
	L, C, U	±1	±1	±1	±1	LSB	12-bit monotonic, T_{MIN} to T_{MAX}
	GL, GC, GU	±1	±1	±1	±1	LSB	12-bit monotonic, T_{MIN} to T_{MAX}
Gain Error (with internal R_{FB})[2]	J, A, S	±20	±20	±25	±25	LSB	D/A register loaded with FFF_H Gain error is adjustable using the circuits in Figures 2 and 3
	K, B, T	±10	±10	±15	±15	LSB	
	L, C, U	±5	±6	±10	±10	LSB	
	GL, GC, GU	±1	±2	±6	±7	LSB	
Gain Temperature Coefficient[3] (ΔGain/ΔTemperature)	All	±5	±5	±10	±10	ppm/°C	Typical value is 2ppm/°C for V_{DD} = +5V
DC Supply Rejection[3] (ΔGain/ΔV_{DD})	All	0 015	0 03	0 01	0 02	%/%	ΔV_{DD} = ±5%
Output Leakage Current at Out 1	J, K, L, GL	10	50	10	50	nA	DB_0-DB_{11} = 0V, $\overline{WR}$, $\overline{CS}$ = 0V
	A, B, C, GC	10	50	10	50	nA	
	S, T, U, GU	10	200	10	200	nA	
DYNAMIC PERFORMANCE							
Current Settling Time[3]	All	2	2	2	2	μs	To 1/2LSB Out_1 load = 100Ω DAC output measured from falling edge of $\overline{WR}$ $\overline{CS}$ = 0V
Propagation Delay[3] (from digital input change to 90% of final analog output)	All	300		250		ns	Out_1 load = 100Ω C_{EXT} = 13pF[4]
Glitch Energy	All	400		250		nV-s[5]	V_{REF} = ACOM
AC Feedthrough at $I_{OUT\,1}$[6]	All	5	5	5	5	mVp-p[5]	V_{REF} = ±10V, 10kHz sine wave
REFERENCE INPUT							
Input Resistance (pin 19 to AGND)	All	7 25	7 25	7 25	7 25	kΩ[7] kΩ	Input resistance TC = 300ppm/°C[5]
AC OUTPUTS							
Output Capacitance[3] $C_{OUT\,1}$	All	70	70	70	70	pF	DB_0-DB_{11} = 0V, $\overline{WR}$, $\overline{CS}$ = 0V
$C_{OUT\,2}$	All	200	200	200	200	pF	DB_0-DB_{11} = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0V
DIGITAL INPUTS							
V_{IH} (Input **High** Voltage)	All	2 4	2 4	13 5	13 5	V[7]	
V_{IL} (Input **Low** Voltage)	All	0.8	0 8	1 5	1 5	V	
I_{IN} (Input Current)[8]	All	±1	±10	±1	±10	μA	V_{IN} = 0 or V_{DD}
Input Capacitance[3] DB_0-DB_{11}	All	5	5	5	5	pF	V_{IN} = 0V
$\overline{WR}$ $\overline{CS}$	All	20	20	20	20	pF	V_{IN} = 0V
SWITCHING CHARACTERISTICS[9]							
Chip Select to Write Setup Time t_{CS}	All	280 200	380 270	180 120	200 150	ns[7] ns[5]	See Timing Diagram
Chip Select to Write Hold Time, t_{CH}	All	0	0	0	0	ns[7]	
Write Pulse Width, t_{WR}	All	250 175	400 280	160 100	240 170	ns[7] ns[5]	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
Data Setup Time, t_{DS}	All	140 100	210 150	90 60	120 80	ns[7] ns[5]	
Data Hold Time, t_{DH}	All	10	10	10	10	ns[7]	
POWER SUPPLY, I_{DD}	All	2	2	2	2	mA	All digital inputs V_{IL} or V_{IH}
	All	100	500	100	500	μA	All digital inputs 0V or V_{DD}
	All	10	10	10	10	μA[5]	All digital inputs 0V or V_{DD}

NOTES: (1) Temperature ranges—J, K, L, GL: 0°C to +70°C. A, B, C, GC: −25°C to +85°C S, T, U, GU. −55°C to +125°C (2) This includes the effect of 5ppm max. gain TC (3) Guaranteed but not tested. (4) DB_0-DB_{11} = 0V to V_{DD} or V_{DD} to 0V. (5) Typical (6) Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix H) to DGND. (7) Minimum. (8) Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA (9) Sample tested at +25°C to ensure compliance

MECHANICAL

20-Pin Hermetic DIP (H Suffix)

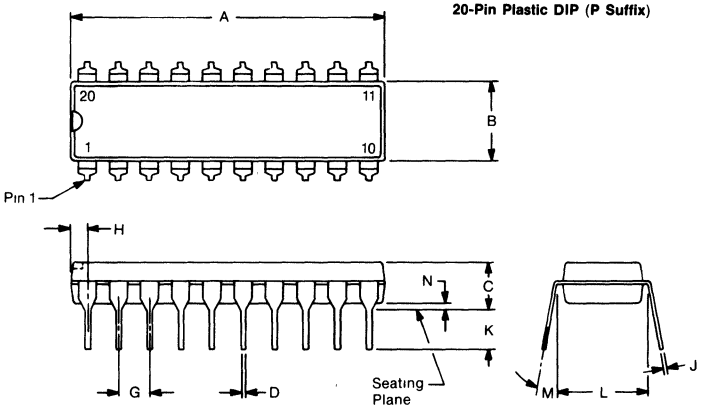


NOTE Leads in true position within 0.010" (0.25mm) R at MMC at seating plane

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.990	1.010	25.15	25.65
B	.285	.305	7.24	7.75
C	.100	.140	2.54	3.56
D	.016	.020	0.41	0.51
F	.054 TYP		1.37 TYP	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.31
K	.170 BASIC		4.32 BASIC	
L	.300	.320	7.62	8.13
N	.025	.045	0.64	1.14

20-Pin Plastic DIP (P Suffix)

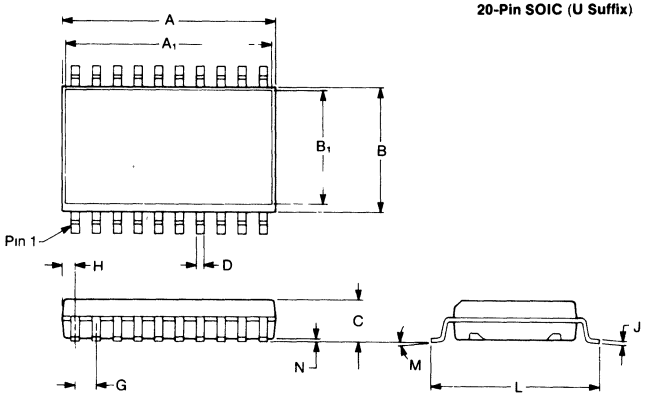


NOTE Leads in true position within 0.010" (0.25mm) R at MMC at seating plane

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.980	1.020	24.89	25.91
B	.240	.280	6.10	7.11
C	—	.210	—	5.33
D	.014	.022	0.36	0.56
G	.100 BASIC		2.54 BASIC	
H	.040	.060	1.02	1.52
J	.008	.015	0.20	0.38
K	.115	.150	2.92	3.81
L	.280	.300	7.11	7.62
M	0°	10°	0°	10°
N	.000	.020	0.00	0.51

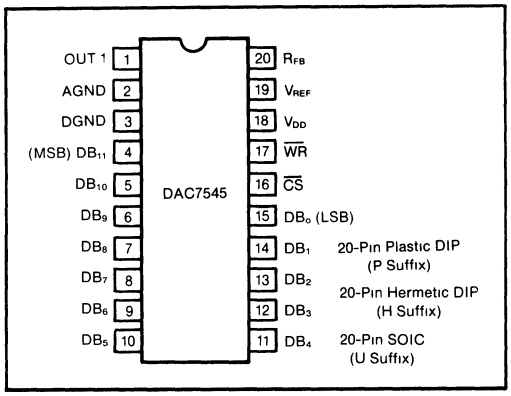
20-Pin SOIC (U Suffix)



NOTE Leads in true position within 0.010" (0.25mm) R at MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.502	.518	12.75	13.16
A_1	.495	.518	12.57	13.16
B	.286	.302	7.26	7.67
B_1	.270	.285	6.86	7.24
C	.093	.108	2.36	2.74
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.026	.034	0.66	0.86
J	.008	.012	0.20	0.30
L	.390	.422	9.91	10.72
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

PIN DESIGNATIONS



ABSOLUTE MAXIMUM RATINGS*

T_A = +25°C unless otherwise noted.

V_{DD} to DGND ..... −0.3V, +17
Digital Input to DGND ..... −0.3V, V_{DD}
V_{RFB}, V_{REF}, to DGND ..... ±25V
$V_{PIN\ 1}$ to DGND ..... −0.3V, V_{DD}
AGND to DGND ..... −0.3V, V_{DD}
Power Dissipation Any Package to +75°C ... 450mW
Derates above +75°C by ... 6mW/°C
Operating Temperature:
Commercial—J, K, L, GL ..... 0°C to +70°C
Industrial—A, B, C, GC ..... −25°C to +85°C
Military—S, T, U, GU ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

***NOTE:** Stresses above those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

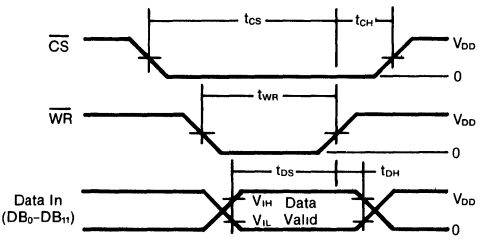
Model	Package	Temperature Range	Relative Accuracy (LSB)	Gain Error (LSB) V_{DD} = +5V
DAC7545JP	Plastic DIP	0°C to +70°C	±2	±20
DAC7545KP	Plastic DIP	0°C to +70°C	±1	±10
DAC7545LP	Plastic DIP	0°C to +70°C	±1/2	±5
DAC7545GLP	Plastic DIP	0°C to +70°C	±1/2	±1
DAC7545JU	Plastic SOIC	0°C to +70°C	±2	±20
DAC7545KU	Plastic SOIC	0°C to +70°C	±1	±10
DAC7545LU	Plastic SOIC	0°C to +70°C	±1/2	±5
DAC7545GLU	Plastic SOIC	0°C to +70°C	±1/2	±1
DAC7545AH	Ceramic Side Braze DIP	−25°C to +85°C	±2	±20
DAC7545BH	Ceramic Side Braze DIP	−25°C to +85°C	±1	±10
DAC7545CH	Ceramic Side Braze DIP	−25°C to +85°C	±1/2	±5
DAC7545GCH	Ceramic Side Braze DIP	−25°C to +85°C	±1/2	±1
DAC7545SH	Ceramic Side Braze DIP	−55°C to +125°C	±2	±20
DAC7545TH	Ceramic Side Braze DIP	−55°C to +125°C	±1	±10
DAC7545UH	Ceramic Side Braze DIP	−55°C to +125°C	±1/2	±5
DAC7545GUH	Ceramic Side Braze DIP	−55°C to +125°C	±1/2	±1

BURN-IN SCREENING OPTION
See text for details

Model	Package	Temperature Range	Relative Accuracy (LSB)	Burn-In Temp. (160 Hours)[1]
DAC7545JP-BI	Plastic DIP	0°C to +70°C	±2	+85°C
DAC7545KP-BI	Plastic DIP	0°C to +70°C	±1	+85°C
DAC7545LP-BI	Plastic DIP	0°C to +70°C	±1/2	+85°C
DAC7545GLP-BI	Plastic DIP	0°C to +70°C	±1/2	+85°C
DAC7545JU-BI	Plastic SOIC	0°C to +70°C	±2	+85°C
DAC7545KU-BI	Plastic SOIC	0°C to +70°C	±1	+85°C
DAC7545LU-BI	Plastic SOIC	0°C to +70°C	±1/2	+85°C
DAC7545GLU-BI	Plastic SOIC	0°C to +70°C	±1/2	+85°C
DAC7545AH-BI	Ceramic Side Braze DIP	−25°C to +85°C	±2	+125°C
DAC7545ABH-BI	Ceramic Side Braze DIP	−25°C to +85°C	±1	+125°C
DAC7545CH-BI	Ceramic Side Braze DIP	−25°C to +85°C	±1/2	+125°C
DAC7545GCH-BI	Ceramic Side Braze DIP	−25°C to +85°C	±1/2	+125°C
DAC7545SH-BI	Ceramic Side Braze DIP	−55°C to +125°C	±2	+125°C
DAC7545TH-BI	Ceramic Side Braze DIP	−55°C to +125°C	±1	+125°C
DAC7545UH-BI	Ceramic Side Braze DIP	−55°C to +125°C	±1/2	+125°C
DAC7545GUH-BI	Ceramic Side Braze DIP	−55°C to +125°C	±1/2	+125°C

NOTE. (1) Or equivalent combination of time and temperature.

WRITE CYCLE TIMING DIAGRAM



Mode Selection	
Write Mode	Hold Mode
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to Data Bus (DB_0-DB_{11}) inputs	Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB_0-DB_{11}) is locked out, DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state

NOTES
V_{DD} = +5V, $t_R = t_F$ = 20ns
V_{DD} = +15V, $t_R = t_F$ = 40ns
All input signal rise and fall times measured from 10% to 90% of V_{DD}
Timing measurement reference level is $(V_{IH} + V_{IL})/2$

BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information table. Burn-in duration is 160 hours at the indicated temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

ESD PROTECTION

The design of the DAC7545 includes ESD protection circuitry for the digital inputs. High voltage static charges are shunted to the supply and ground rails. However, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or rails. The foam or rails should be discharged to the destination socket before devices are removed.

DISCUSSION OF SPECIFICATIONS

Relative Accuracy

This term (also known as end point linearity) describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line after zero and full scale have been adjusted.

Differential Nonlinearity

Differential nonlinearity is the deviation from an ideal 1LSB change in the output, for adjacent input code changes. A differential nonlinearity specification of 1LSB guarantees monotonicity.

Gain Error

Gain error is the difference in measure of full-scale output versus the ideal DAC output. The ideal output for the DAC7545 is $-(4095/4096)$ (V_{REF}). Gain error may be adjusted to zero using external trims as shown in the applications section.

Output Leakage Current

The current which appears at OUT 1 with the DAC loaded with all zeros.

Multiplying Feedthrough Error

The AC output error due to capacitive feedthrough from V_{REF} to OUT 1 with the DAC loaded with all zeros. This test is performed using a 10kHz sine wave.

Output Current Settling Time

The time required for the output to settle within ±0.5LSB of final value from a change in code of all zeros to all ones, or all ones to all zeros.

Propagation Delay

The delay of the internal circuitry is measured as the time from a digital code change to the point at which the output reaches 90% of final value.

Digital-To-Analog Glitch Impulse

The area of the glitch energy measured in nanovolt-seconds. Key contributions to glitch energy are internal circuitry timing differences and charge injected from digital logic. The measurement is performed with V_{REF} = GND and an OPA600 as the output op amp and C_1 (phase compensation) = 0pF.

Monotonicity

Monotonicity assures that the analog output will increase or stay the same for increasing digital input codes. The DAC7545 is guaranteed monotonic to 12 bits, except the J, A, S grades are specified to be 10-bit monotonic.

Power Supply Rejection

Power supply rejection is the measure of the sensitivity of the output (full scale) to a change in the power supply voltage.

CIRCUIT DESCRIPTION

Figure 1 shows a simplified schematic of the digital-to-analog converter portion of the DAC7545. The current from the V_{REF} pin is switched from $I_{OUT\,1}$ to AGND by the FET switch. This circuit architecture keeps the resistance

at the reference pin constant and equal to R_{LDR}, so the reference could be provided by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to ±20V even with V_{DD} = 5V. The R_{LDR} is equal to "R" and is typically 11kΩ.

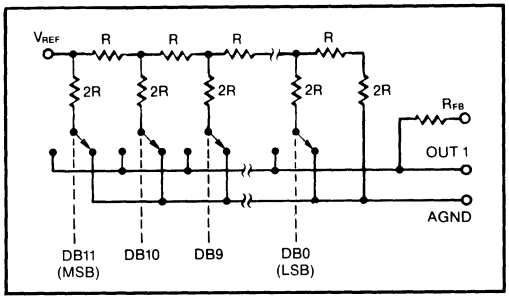


FIGURE 1. Simplified DAC Circuit of the DAC7545.

The output capacitance of the DAC7545 is code dependent and varies from a minimum value (70pF) at code 000H to a maximum (200pF) at code FFFH.

The input buffers are CMOS inverters, designed so that when the DAC7545 is operated from a 5V supply (V_{DD}), the logic threshold is TTL-compatible. Being simple CMOS inverters, there is a range of operation where the inverters operate in the linear region and thus draw more supply current than normal. Minimizing this transition time through the linear region and insuring that the digital inputs are operated as close to the rails as possible will minimize the supply drain current.

APPLICATIONS

UNIPOLAR OPERATION

Figure 2 shows the DAC7545 connected for unipolar operation. The high-grade DAC7545 is specified for a 1LSB gain error, so gain adjust is typically not needed. However, the resistors shown are for adjusting full-scale errors. The value of R_1 should be minimized to reduce the effects of mismatching temperature coefficients between the internal and external resistors. A range of adjustment of 1.5 times the desired range will be adequate. For example, for a DAC7545JP, the gain error is specified to be ±25LSB. A range of adjustment of ±37LSB will be adequate. The equation below results in a value of 458Ω for the potentiometer (use 500Ω).

$$R_1 = \frac{R_{LADDER}}{4096} \ (3 \times \text{Gain Error})$$

The addition of R_1 will cause a negative gain error. To compensate for this error, R_2 must be added. The value of R_2 should be one-third the value of R_1.

The capacitor across the feedback resistor is used to compensate for the phase shift due to stray capacitances of the circuit board, the DAC output capacitance, and op amp input capacitance. Eliminating this capacitor will result in excessive ringing and an increase in glitch energy. This capacitor should be as small as possible to minimize settling time.

The circuit of Figure 2 may be used with input voltages up to ±20V as long as the output amplifier is biased to

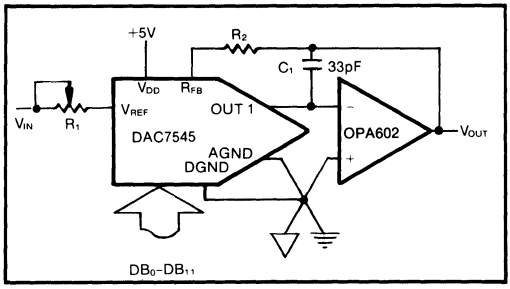


FIGURE 2. Unipolar Binary Operation.

handle the excursions. Table I represents tha analog output for four codes into the DAC for Figure 2.

TABLE I. Unipolar Codes.

Binary Code	Analog Output
MSB LSB	
1111 1111 1111	$-V_{IN}$ (4095/4096)
1000 0000 0000	$-V_{IN}$ (2048/4096) = $-1/2V_{IN}$
0000 0000 0001	$-V_{IN}$ (1/4096)
0000 0000 0000	0 Volts

BIPOLAR OPERATION

Figure 3 and Table II illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code. The inverter U_1 on the MSB line converts twos complement input code to offset binary code. The inverter U_1 may be omitted if the inversion is done in software.

R_3, R_4, and R_5 must match within 0.01% and should be the same type of resistors (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R_3 value to R_4 causes both offset and full-scale error. Mismatch of R_5 to R_4 and R_3 causes full-scale error.

TABLE II. Twos Complement Code Table for Circuit of Figure 3.

Data Input	Analog Output
MSB LSB	
0111 1111 1111	$+V_{IN}$ (2047/2048)
0000 0000 0001	$+V_{IN}$ (1/2048)
0000 0000 0000	0 Volts
1111 1111 1111	$-V_{IN}$ (1/2048)
1000 0000 0000	$-V_{IN}$ (2048/2048)

DIGITALLY CONTROLLED GAIN BLOCK

Figure 4 shows a circuit for a digitally controlled gain block. The feedback for the op amp is made up of the FET switch and the R-2R ladder. The input resistor to the gain block is the R_{FB} of the DAC7545. Since the FET switch is in the feedback loop, a "zero code" into the

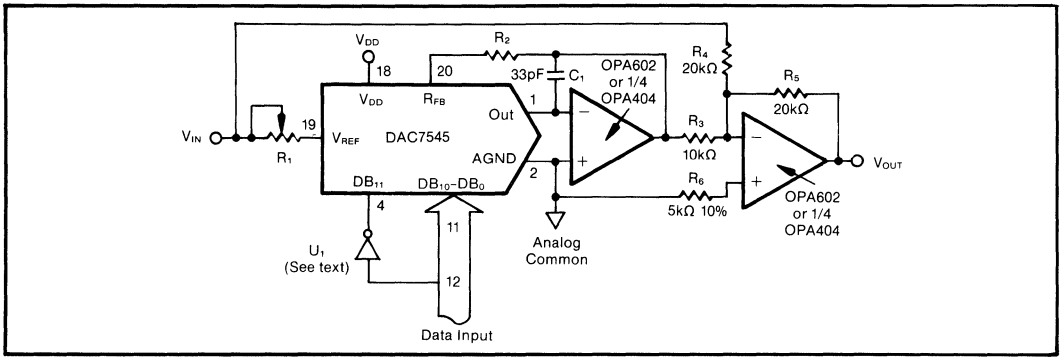


FIGURE 3. Bipolar Operation (Twos Complement Code).

DAC will result in the op amp having no feedback, and a saturated op amp output.

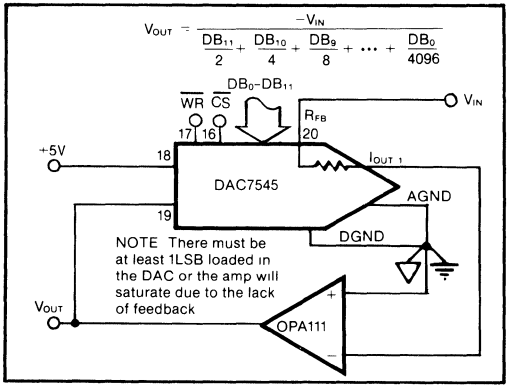


FIGURE 4. Digitally Controlled Gain Block.

APPLICATIONS HINTS

CMOS DACs such as the DAC7545 exhibit a code-dependent out resistance. The effect of this is a code-dependent differential nonlinearity at the amplifier output which depends on the offset voltage V_{OS} of the amplifier. Thus linearity depends upon the potential of I_{OUT} and AGND being exactly equal to each other. Usually the DAC is connected to an external op amp with its noninverting input connected to AGND. The op amp selected should have a low input bias current and low V_{OS} and V_{OS} drift over temperature. The op amp offset voltage should be less than $(25 \times 10^{-6})(V_{REF})$ over operating conditions. Suitable op amps are the Burr-Brown OPA37 and the OPA111 for fixed reference applications and low bandwidth requirements. The OPA37 has low V_{OS} and will not require an offset trim. For wide bandwidth, high slew rate, or fast settling applications, the Burr-Brown OPA602, 1/4 OPA404, or OPA606 are recommended.

Unused digital inputs should be connected to V_{DD} or to DGND. This prevents noise from triggering the high impedance digital input. It is suggested that the unused digital inputs also be given a path to ground or V_{DD} through a 1MΩ resistor to prevent the accumulation of static charge if the PC card is unplugged from the system. In addition, in systems where the AGND to DGND connection is on a backplane, it is recommended that two diodes be connected in inverse parallel between AGND and DGND.

INTERFACING TO MICROPROCESSORS

The DAC7545 can be directly interfaced to either an 8- or 16-bit microprocessor through its 12-bit wide data latch using the $\overline{CS}$ and $\overline{WR}$ controls.

An 8-bit processor interface is shown in Figure 5. It uses two memory addresses, one for the lower 8 bits and one for the upper 4 bits of data into the DAC via the latch.

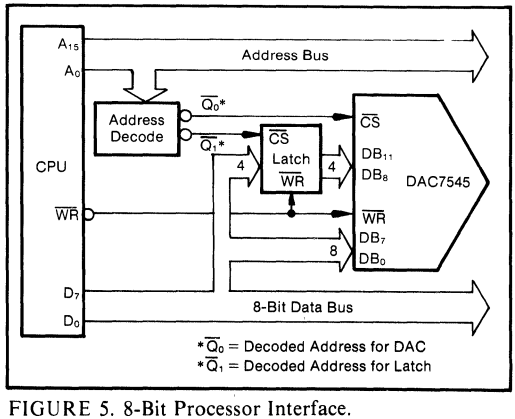
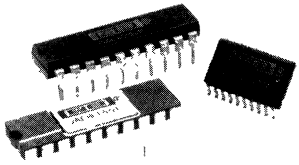


FIGURE 5. 8-Bit Processor Interface.

BURR-BROWN®



DAC8012

CMOS 12-Bit Multiplying DIGITAL-TO-ANALOG CONVERTER With Memory

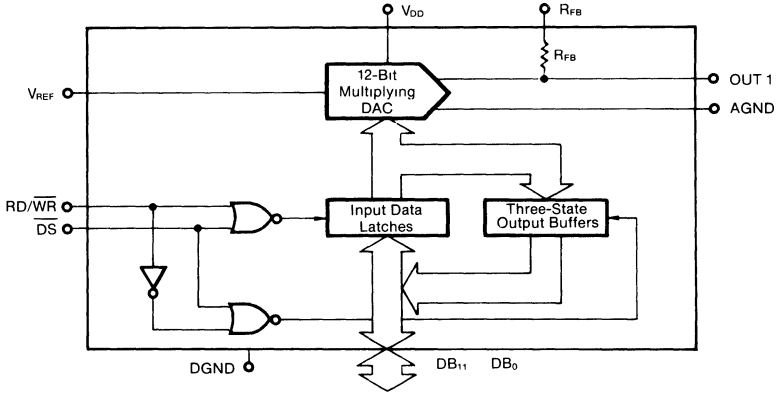
FEATURES

- DATA READBACK CAPABILITY
- FOUR-QUADRANT MULTIPLICATION
- LOW GAIN TC: 2PPM/°C typ
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- SINGLE 5V TO 15V SUPPLY
- LOW OUTPUT LEAKAGE (10nA max)
- LOW OUTPUT CAPACITANCE (70pF max)
- DIRECT REPLACEMENT FOR PMI DAC8012

DESCRIPTION

The DAC8012 is a CMOS, 12-bit, four-quadrant multiplying, digital-to-analog converter with input data latches and 3-state readback capabilities. The input data is loaded into the DAC as a 12-bit data word. The data is loaded into the DAC from the bus when both the data strobe ($\overline{DS}$) and the read/write ($RD/\overline{WR}$) pins are held low. Data may be read back from the DAC by holding $\overline{DS}$ low and ($RD/\overline{WR}$) high. This readback feature enables the user to monitor the state of multiple DACs on a single bi-directional bus.

Laser-trimmed thin-film resistors and excellent CMOS voltage switches provide true 12-bit integral and differential linearity. The device operates on a single +5V to +15V supply and is available in 20-pin side-brazed DIP, 20-pin plastic DIP or a 20-lead plastic SOIC package. Devices are specified over the commercial, industrial, and military temperature ranges and are available with additional reliability screening.



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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{REF} = +10V, $V_{OUT\,1}$ = 0V, AGND = DGND = 0V unless otherwise noted

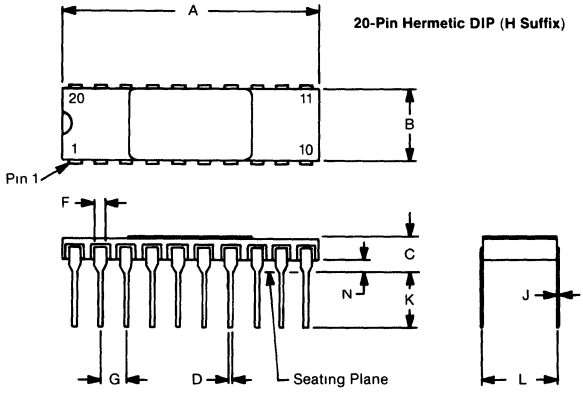
PARAMETER	CONDITIONS	DAC8012B, K, T[1] MIN	DAC8012B, K, T[1] TYP	DAC8012B, K, T[1] MAX	DAC8012A, J, S[1] MIN	DAC8012A, J, S[1] TYP	DAC8012A, J, S[1] MAX	UNITS
V_{DD} = +5V or +15V								
STATIC ACCURACY								
Resolution		12			12			Bits
Relative Accuracy	T_A = Full temperature range			±1/2			±1	LSB
Differential Nonlinearity[2]	T_A = Full temperature range			±1			±1	LSB
Gain Error[3][4]	T_A = +25°C			±1			±3	LSB
	T_A = Full temperature Range			±2			±4	LSB
Gain Temperature Coefficient ΔGain/ΔTemperature[5][6]				±5			±5	ppm/°C
DC Supply Rejection ΔGain/ΔV_{DD}[5]	T_A = +25°C (ΔV_{DD} = ±5%)			0 002			0 002	%/%
	T_A = Full temperature range (ΔV_{DD} = ±5%)			0 004			0 004	%/%
Output Leakage Current at OUT 1	T_A = +25°C, RD/WR = DS = 0V, all digital inputs = 0V			10			10	nA
	T_A = Full temperature range S, T versions			200			200	nA
	T_A = Full temperature range J, K, A, B versions			25			25	nA
DYNAMIC PERFORMANCE								
Propagation Delay[5][7][8]	T_A = +25°C (OUT 1 Load = 100Ω, C_{EXT} = 13pF)			300			300	ns
Current Settling Time[5][8]	T_A = Full temperature range (to 1/2 LSB) $I_{OUT\,1}$ Load = 100Ω			1			1	µs
Glitch Energy[5], V_{REF} = AGND	T_A = +25°C			400			400	nVs
	T_A = Full temperature range			500			500	nVs
AC Feedthrough at $I_{OUT\,1}$[5][11]	T_A = Full temperature range, V_{REF} = ±10V, f = 10kHz			5			5	mVp-p
REFERENCE INPUT Input Resistance (Pin 19 to GND)[12]	T_A = Full temperature range	7	11	15	7	11	15	kΩ
V_{DD} = +5V								
ANALOG OUTPUTS	T_A = Full temperature range							
Output Capacitance[5]	V_{DD} = +5V or +15V							
$C_{OUT\,2}$	DB_0-DB_{11} = 0V, RD/WR = DS = 0V			70			70	pF
$C_{OUT\,1}$	DB_0-DB_{11} = V_{DD}, RD/WR = DS = 0V			150			150	pF
DIGITAL INPUTS								
Input High Voltage	T_A = Full temperature range	2 4			2 4			V
Input Low Voltage	T_A = Full temperature range			0 8			0 8	V
Input Current[9]	T_A = +25°C			1			1	µA
	T_A = Full temperature range			10			10	µA
Input Capacitance[5] DB_0-DB_{11}	T_A = Full temperature range			12			12	pF
RD/WR, DS	T_A = Full temperature range			6			6	pF
DIGITAL OUTPUTS								
Output High Voltage	I_O = 400µA	4 0			4 0			V
Output Low Voltage	I_O = −1 6mA			0 4			0 4	V
Three-State Output Leakage Current				10			10	µA
SWITCHING CHARACTERISTICS[10]	See timing diagram							
Write to Data Stobe Setup Time	T_A = +25°C	0			0			ns
	T_A =Full temperature range	0			0			ns
Data Strobe to Write Hold Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Read to Data Strobe Setup Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Data Strobe to Read Hold Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Write Mode Data Strobe Width	T_A = +25°C	180			180			ns
	T_A = Full temperature range	250			250			ns
Read Mode Data Strobe Width	T_A = +25°C	220			220			ns
	T_A = Full temperature range	290			290			ns
Data Setup Time	T_A = +25°C	210			210			ns
	T_A = Full temperature range	250			250			ns
Data Hold Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Data Strobe to Output Valid Time[5]	T_A = +25°C			300			300	ns
	T_A = Full temperature range			400			400	ns
Output Active Time from Deselection[5]	T_A = +25°C			215			215	ns
	T_A = Full temperature range			375			375	ns
POWER SUPPLY	T_A = Full temperature range (all digital inputs V_{INL} or V_{INH})			2			2	mA
Supply Current	T_A = Full temperature range (all digital inputs 0V or V_{DD})		10	100		10	100	µA

ELECTRICAL CHARACTERISTICS (CONT)

PARAMETER	CONDITIONS	DAC8012B, K, T[1]			DAC8012A, J, S[1]			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
	V_{DD} = +15V							
DIGITAL INPUTS								
Input High Voltage	T_A = Full temperature range	13.5			13.5			V
Input Low Voltage	T_A = Full temperature range			1.5			1.5	V
Input Current[9]	T_A = +25°C			1			1	µA
	T_A = Full temperature range			10			10	µA
Input Capacitance[5] DB_0-DB_{11}	T_A = Full temperature range			12			12	pF
RD/WR, DS	T_A = Full temperature range			10			10	pF
DIGITAL OUTPUTS								
Output High Voltage	I_O = 3mA	13.5			13.5			V
Output Low Voltage	I_O = −3mA			1.5			1.5	V
Three-State Output Leakage Current				10			10	µA
SWITCHING CHARACTERISTICS[10]	See Timing Diagram							
Write to Data Strobe Setup Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Data Strobe to Write Hold Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Read to Data Strobe Setup Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Data Strobe to Read Hold Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Write Mode Data Strobe Width	T_A = +25°C	100			100			ns
	T_A = Full temperature range	120			120			ns
Read Mode Data Strobe Width	T_A = +25°C	110			110			ns
	T_A = Full temperature range	150			150			ns
Data Setup Time	T_A = +25°C	90			90			ns
	T_A = Full temperature range	120			120			ns
Data Hold Time	T_A = +25°C	0			0			ns
	T_A = Full temperature range	0			0			ns
Data Strobe to Output Valid Time	T_A = +25°C			180			180	ns
	T_A = Full temperature range			220			220	ns
Output Active Time for Deselection	T_A = +25°C			180			180	ns
	T_A = Full temperature range			250			250	ns
POWER SUPPLY								
Supply Current	T_A = Full temperature range (all digital inputs V_{INL} or V_{INH})			2			2	mA
	T_A = Full temperature range (all digital inputs 0V or V_{DD})		10	100		10	100	µA

NOTES (1) T_A = −55°C to +125°C for S, T grades T_A = −25°C to +85°C for A, B grades T_A = 0°C to +70°C for J, K grades (2) 12-bit monotonic over full temperature range (3) Includes the effects of 5ppm max gain TC (4) Using internal R_{FB} DAC register loaded with 1111 1111 1111 (5) **Guaranteed** but **not tested** (6) Typical value is 2ppm/°C for V_{DD} = +5V (7) From digital input change to 90% of final analog output (8) All digital inputs = 0V to V_{DD}, or V_{DD} to 0V (9) Logic inputs are MOS gates, typical input current (at +25°C) is less than 1nA (10) Sample tested at +25°C to ensure compliance (11) Feedthrough can further be reduced by connecting the metal lid on the sidebraze package (Suffix H) to DGND (12) Resistor T C = +100ppm/°C max

MECHANICAL

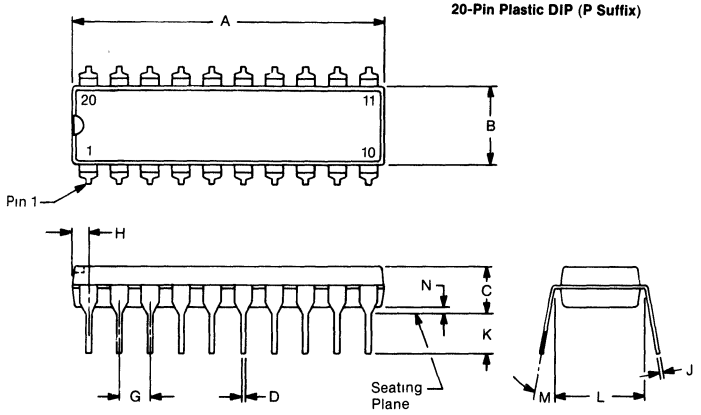


NOTE Leads in true position within 0.010" (0.25mm) R at MMC at seating plane

Pin numbers shown for reference only. Numbers may not be marked on package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.990	1.010	25.15	25.65
B	.285	.305	7.24	7.75
C	.100	.140	2.54	3.56
D	.016	.020	0.41	0.51
F	.054 TYP		1.37 TYP	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.31
K	.170 BASIC		4.32 BASIC	
L	.300	.320	7.62	8.13
N	.025	.045	0.64	1.14

20-Pin Plastic DIP (P Suffix)

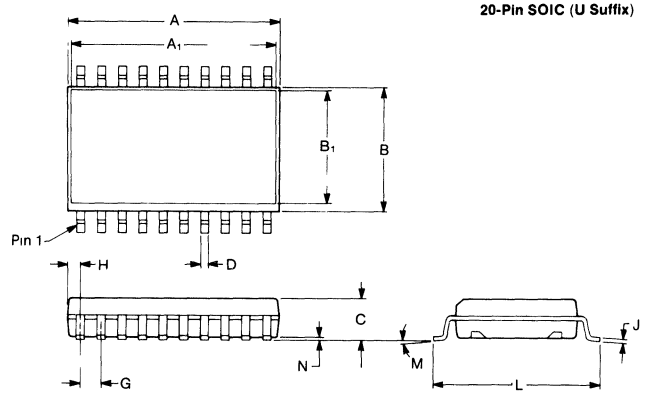


NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers may not be marked on package

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	980	1 020	24 89	25 91
B	240	280	6 10	7 11
C	—	210	—	5 33
D	014	022	0 36	0 56
G	100 BASIC		2 54 BASIC	
H	040	060	1 02	1 52
J	008	015	0 20	0 38
K	115	150	2 92	3 81
L	280	300	7 11	7 62
M	0°	10°	0°	10°
N	000	020	0 00	0 51

20-Pin SOIC (U Suffix)

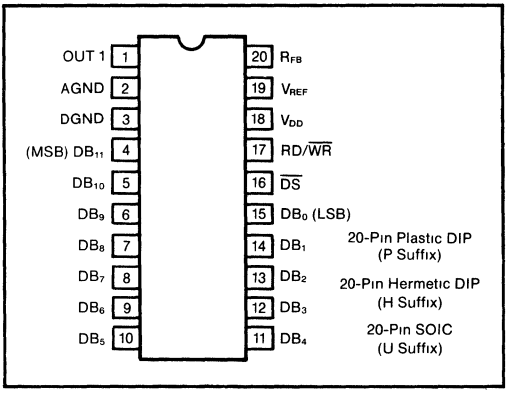


NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers may not be marked on package

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	502	518	12 75	13 16
A_1	495	518	12 57	13 16
B	286	302	7 26	7 67
B_1	270	285	6 86	7 24
C	093	108	2 36	2 74
D	015	019	0 38	0 48
G	050 BASIC		1 27 BASIC	
H	026	034	0 66	0 86
J	008	012	0 20	0 30
L	390	422	9 91	10 72
M	0°	10°	0°	10°
N	000	012	0 00	0 30

PIN DESIGNATIONS



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted)

V_{DD} to DGND ..... −0 3V, +17V
Digital Input Voltage to DGND ..... −0 3V, V_{DD}
AGND to DGND ..... −0 3V, V_{DD}
V_{RFB}, V_{REF} to DGND ..... ±25V
$V_{PIN\ 1}$ to DGND ..... −0 3V, V_{DD}
Power Dissipation (any package) to +75°C 450mW
Derates Above +75°C by ..... 6mW/°C
Operating Temperature Range
Military Grades S, T ..... −55°C to +125°C
Industrial Grades A, B ..... −25°C to +85°C
Commercial Grades J, K ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

CAUTION

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation at or above this specification is not implied Exposure to above maximum rating conditions for extended periods may affect device reliability
2 Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}
3. The digital inputs are zener protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use Use proper antistatic handling procedures
4 Remove power before inserting or removing units from their sockets

ORDERING INFORMATION

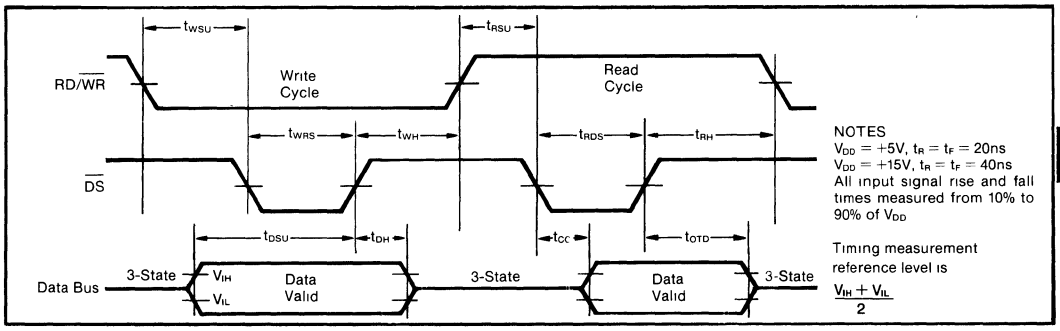
Model	Package	Temperature Range	Relative Accuracy (LSB)	Gain Error (LSB)
DAC8012JP	Plastic DIP	0°C to +70°C	±1	±3
DAC8012KP	Plastic DIP	0°C to +70°C	±1/2	±1
DAC8012JU	Plastic SOIC	0°C to +70°C	±1	±3
DAC8012KU	Plastic SOIC	0°C to +70°C	±1/2	±1
DAC8012AH	Side-brazed ceramic DIP	-25°C to +85°C	±1	±3
DAC8012BH	Side-brazed ceramic DIP	-25°C to +85°C	±1/2	±1
DAC8012SH	Side-brazed ceramic DIP	-55°C to +125°C	±1	±3
DAC8012TH	Side-brazed ceramic DIP	-55°C to +125°C	±1/2	±1

BURN-IN SCREENING OPTION
See text for details

Model	Package	Temperature Range	Relative Accuracy (LSB)	Burn-In Temp. (160 Hours)[1]
DAC8012JP-BI	Plastic DIP	0°C to +70°C	±1	+85°C
DAC8012KP-BI	Plastic DIP	0°C to +70°C	±1/2	+85°C
DAC8012JU-BI	Plastic SOIC	0°C to +70°C	±1	+85°C
DAC8012KU-BI	Plastic SOIC	0°C to +70°C	±1/2	+85°C
DAC8012AH-BI	Side-brazed ceramic DIP	-25°C to +85°C	±1	+125°C
DAC8012BH-BI	Side-brazed ceramic DIP	-25°C to +85°C	±1/2	+125°C
DAC8012SH-BI	Side-brazed ceramic DIP	-55°C to +125°C	±1	+125°C
DAC8012TH-BI	Side-brazed ceramic DIP	-55°C to +125°C	±1/2	+125°C

NOTE (1) Or equivalent combination of time and temperature

TIMING DIAGRAM



BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information table. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

ESD PROTECTION

The design of the DAC8012 includes ESD protection circuitry for the digital inputs. High voltage static charges are shunted to the supply and ground rails. However, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or rails. The foam or rails should be discharged to the destination socket before devices are removed.

DISCUSSION OF SPECIFICATIONS

Relative Accuracy

This term (also known as end point linearity) describes the transfer function of analog output to digital input code. Relative accuracy describes the deviation from a straight line after zero and full scale have been adjusted.

Differential Nonlinearity

Differential nonlinearity is the deviation from an ideal 1LSB change in the output, for adjacent input code changes. A differential nonlinearity specification of 1LSB guarantees monotonicity.

Gain Error

Gain error is the difference in measure of full-scale output versus the ideal DAC output. The ideal output for the DAC8012 is $-(4095/4096)$ (V_{REF}). Gain error may be adjusted to zero using external trims as shown in the applications section.

Output Leakage Current

The current which appears at OUT_1 with the DAC loaded with all zeros.

Multiplying Feedthrough Error

The AC output error due to capacitive feedthrough from V_{REF} to OUT_1 with the DAC loaded with all zeros. This test is performed using a 10kHz sine wave.

Output Current Settling Time

The time required for the output to settle within ±1/2LSB of final value from a change in code of all zeros to all ones, or all ones to all zeros.

Propagation Delay

The delay of the internal circuitry is measured as the time from a digital code change to the point at which the output reaches 90% of final value.

Digital-To-Analog Glitch Impulse

The area of the glitch energy measured in nanovolt-seconds. Key contributions to glitch energy are internal circuitry timing differences and charge injected from digital logic. The measurement is performed with V_{REF} = GND.

Monotonicity

Monotonicity assures that the analog output will increase or stay the same for increasing digital input codes. The DAC8012 is guaranteed monotonic to 12 bits.

Power Supply Rejection

Power supply rejection is the measure of the sensitivity of the output (full scale) to a change in the power supply voltage.

CIRCUIT DESCRIPTION

DIGITAL-TO-ANALOG SECTION

Figure 1 shows a simplified schematic of the digital-to-analog portion of the DAC8012. The current from the V_{REF} pin is switched from $I_{OUT\ 1}$ to AGND by the FET switch for that bit. This circuit architecture keeps the resistance at the reference pin constant and equal to R_{LDR}, so the reference could be provided by either a voltage or current, AC or DC, positive or negative polarity, and have a voltage range up to ±20V even with V_{DD} = 5V. The R_{LDR} is equal to "R" and is typically 11kΩ.

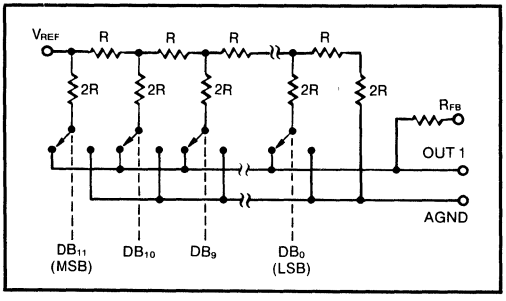


FIGURE 1. Simplified Circuit of the DAC8012.

The output capacitance of the DAC8012 is code dependent and varies from a minimum value (70pF) at code 000_H to a maximum (200pF) at code FFF_H.

DIGITAL SECTION

Figure 2 shows the basic current switch. Figure 3 shows the schematic of the input/output buffers. When the $\overline{DS}$ and the RD/$\overline{WR}$ are held low, the latches are transparent and pass data from the data bus to the DAC. When the $\overline{DS}$ is held low and the RD/$\overline{WR}$ line is held high, the three-state buffer becomes active and the data at the DAC is presented to the digital input/output lines for data readback.

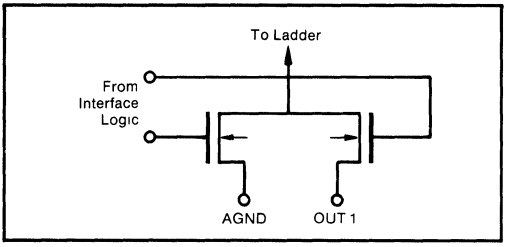


FIGURE 2. N-Channel Current Steering Switch.

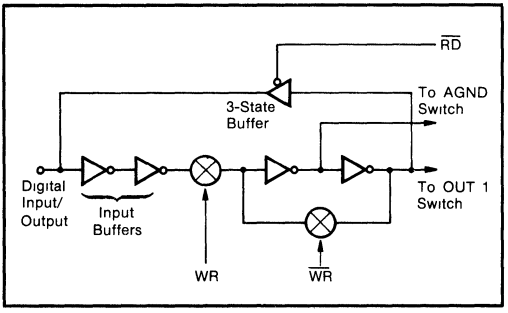


FIGURE 3. Digital Input/Output Structure.

The input buffers are CMOS inverters, designed so that when the DAC8012 is operated from a 5V supply (V_{DD}), the logic threshold is TTL compatible. Being simple CMOS inverters, there is a range of operations where the inverters operate in the linear region and thus draw more supply current than normal. Minimizing the transition time through the linear region and insuring that the digital inputs are operated as close to the rails as possible will minimize the supply drain current.

APPLICATIONS

UNIPOLAR OPERATION

Figure 4 shows the DAC8012 connected for unipolar operation. The high-grade DAC8012 is specified for a 1LSB gain error, so gain adjust is typically not needed.

However, the resistors shown are for adjusting full-scale errors. The value of R_1 should be minimized to reduce the effects of mismatching temperature coefficients between the internal and external resistors. A range of adjustment of 1.5 times the desired range will be adequate. For example, for a DAC8012JP, the gain error is specified to be ±3LSB. A range of adjustment of ±4.5LSB will be adequate. The equation shows a minimum value of 33Ω for the potentiometer.

$$R_1 = (R_{LADDER} / 4096) \times (3 \times \text{Gain Error})$$

The addition of R_1 will cause a negative gain error. To compensate for this error, R_2 must be added. The value of R_2 should be one-third the value of R_1.

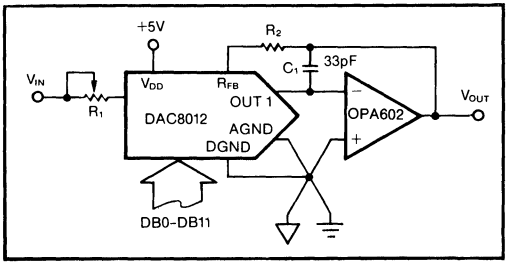


FIGURE 4. Unipolar Binary Operation.

The capacitor across the feedback resistor is used to compensate for the phase shift due to stray capacitances of the circuit board, the DAC output capacitance, and op amp input capacitance. Eliminating this capacitor will result in excessive ringing and an increase in glitch energy in higher speed applications. This capacitor should be as small as possible to minimize settling time.

The circuit of Figure 4 may be used with input voltages up to ±20V as long as the output amplifier is biased to handle the excursions. Table I represents the analog output for four codes into the DAC for Figure 4.

TABLE I. Unipolar Output Code for Figure 4.

Binary Code	Analog Output
MSB ↓ ↓ LSB	
1111 1111 1111	$-V_{IN}$ (4095/4096)
1000 0000 0000	$-V_{IN}$ (2048/4096) = $-1/2V_{IN}$
0000 0000 0001	$-V_{IN}$ (1/4096)
0000 0000 0000	0 Volts

BIPOLAR FOUR-QUADRANT OPERATION

Figure 5 and Table II illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code. The inverter U_1 on the MSB line converts twos complement input code to offset binary code. The inverter U_1 may be omitted if the inversion is done in software.

R_3, R_4, and R_5 must match within 0.01% and should be the same type of resistors (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R_3 value to R_4 causes both offset and full-scale error. Mismatch of R_5 to R_4 and R_3 causes full-scale error.

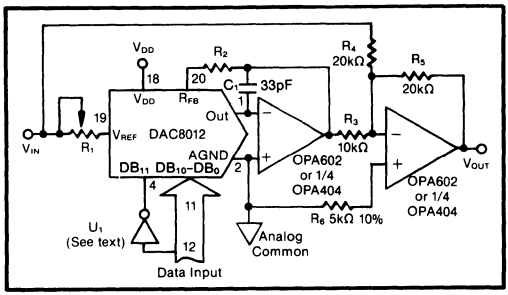


FIGURE 5. Bipolar Operation (Twos Complement Code).

TABLE II. Twos Complement Code Table for Circuit of Figure 5.

Data Input	Analog Output
MSB ↓ ↓ LSB	
0111 1111 1111	$+V_{IN}$ (2047/2048)
0000 0000 0001	$+V_{IN}$ (1/2048)
0000 0000 0000	0 Volts
1111 1111 1111	$-V_{IN}$ (1/2048)
1000 0000 0000	$-V_{IN}$ (2048/2048)

DIGITALLY CONTROLLED GAIN BLOCK

Figure 6 shows a circuit for a digitally controlled gain block. The feedback for the op amp is made up of the FET switch and the R-2R ladder. The input resistor to the gain block is the R_{FB} of the DAC8012. Since the FET switch is in the feedback loop, a "zero code" into the DAC will result in the op amp having no feedback and a saturated op amp output. The DAC8012 readback feature makes the DAC8012 especially good for this configuration when an automatic gain or automatic calibration routine is used. If the logic were set up to calibrate a value via logic external to the processor (successive approximation register), then when the calibration is done, the processor could read the DAC8012 to store away the calibration code.

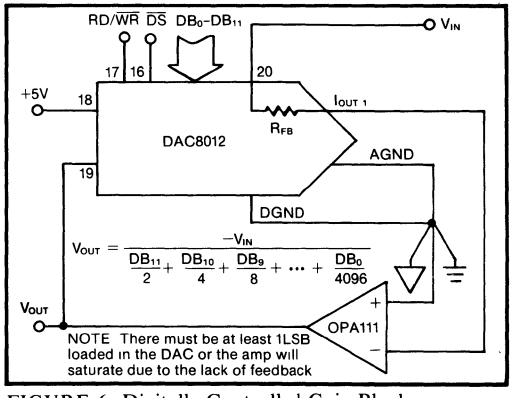


FIGURE 6. Digitally Controlled Gain Block.

APPLICATIONS HINTS

CMOS DACs such as the DAC8012 exhibit a code-dependent output resistance. The effect of this is a code-dependent differential nonlinearity at the amplifier output which depends on the offset voltage V_{OS} of the amplifier. Thus linearity depends upon the potential of I_{OUT} and AGND being exactly equal to each other. Usually the DAC is connected to an external op amp with its noninverting input connected to AGND. The op amp selected should have a low input bias current and low V_{OS} and V_{OS} drift over temperature. The op amp offset voltage should be less than (25×10^{-6}) (V_{REF}) over operating conditions. Suitable op amps are the Burr-Brown OPA37 and the OPA111 for fixed reference applications and low bandwidth requirements. The OPA37 has low V_{OS} and will not require an offset trim. For wide bandwidth, high slew rate, or fast settling applications, the Burr-Brown OPA602, 1/4 OPA404, or OPA606 are recommended.

Unused digital inputs should be connected to V_{DD} or to DGND. This prevents noise from triggering the high impedance digital input. It is suggested that the unused digital inputs also be given a path to ground or V_{DD} through a 1MΩ resistor to prevent the accumulation of static charge if the PC card is unplugged from the system. In addition, in systems where the AGND to DGND connection is on a backplane, it is recommended that two diodes be connected in inverse parallel between AGND and DGND.

INTERFACING TO MICROPROCESSORS

Figure 7 shows the DAC8012 interfaced to a 16-bit microprocessor. The interface requires only address decoding to select the DAC to be written to or read from.

Figure 8 shows an interface scheme for using the DAC8012 with an 8-bit microprocessor. The data for the first 4 bits are written and latched into the external write latch and the next 8 bits are presented on the bus. The DAC8012 is then instructed to pass the data through the internal DAC latch ($\overline{WR}$ + $\overline{DS}$) and all 8 bits are transferred into the DAC. Reading data back is done in the same manner.

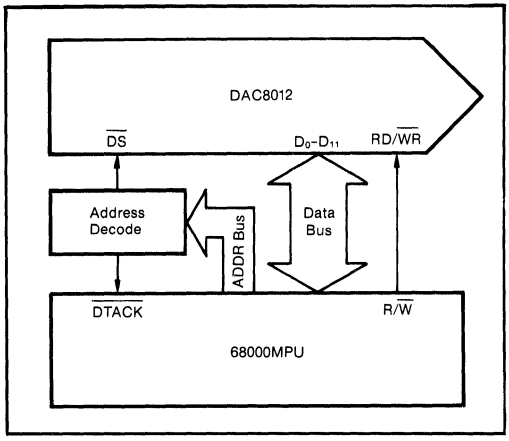


FIGURE 7. 16-Bit Microprocessor to DAC8012 Interface.

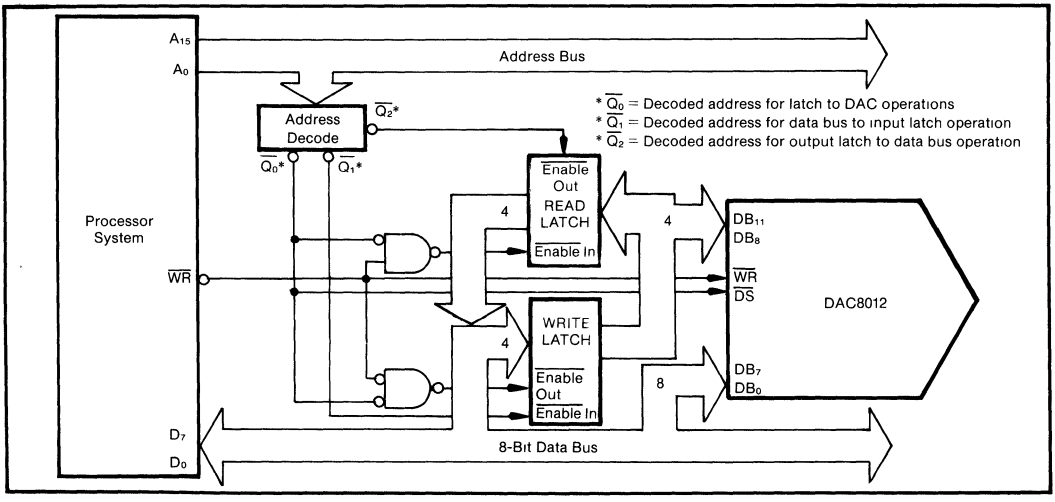
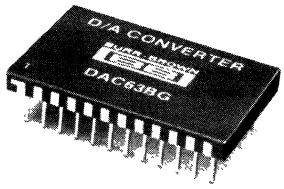


FIGURE 8. 8-Bit Processor to DAC8012 Interface.

BURR-BROWN®



DAC63

Ultra-High Speed DIGITAL-TO-ANALOG CONVERTER

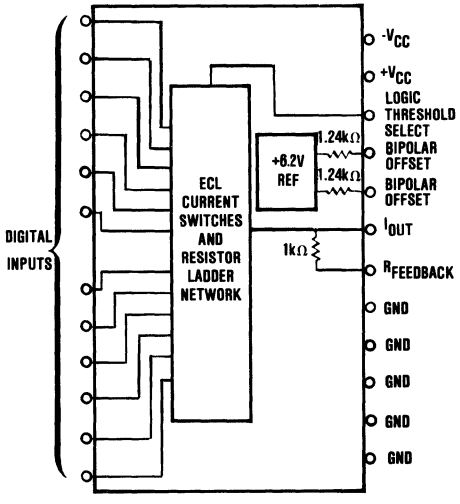
FEATURES

- 12-BIT RESOLUTION AND ACCURACY
- 30nsec SETTLING TIME (MAJOR CARRY)
- ECL-COMPATIBLE INPUTS
- LOW GLITCH ENERGY
- ±30ppm/°C MAX GAIN DRIFT
- LINEARITY ERROR LESS THAN ±1/2LSB OVER SPECIFIED TEMP RANGE
- ADJUSTABLE LOGIC THRESHOLD FOR IDEAL SWITCHING
- INTERNALLY-BYPASSED SUPPLY LINES TO MINIMIZE SETTLING TIME
- INTERNAL FEEDBACK RESISTOR FOR EXCELLENT THERMAL TRACKING
- INDUSTRIAL AND MILITARY GRADES
- HIGH RELIABILITY SCREENING AVAILABLE

DESCRIPTION

The DAC63 is an ultra-fast-settling 12-bit current output D/A converter in a 24-pin dual-in-line package. The inputs are ECL-compatible and the output settles in 30nsec, typ (40nsec, max for C and T grades) to within ±0.012% of Full Scale Range for an MSB change. The DAC63 utilizes a monolithic 12-bit switch chip and a stable thin-film-on-sapphire resistor network to achieve fast settling time and excellent stability over temperature and time. Because of the close thermal tracking of the current-switching transistors (all on one monolithic chip), the possibility of thermal-tail settling time problems are eliminated. An internal applications resistor for use with an external output op amp is included to convert the output current to insure excellent tracking and therefore lower drift. The linearity is guaranteed to be within ±1/2LSB over the specified temperature range of −25°C to +85°C for the CG, CM, BG, and BM grades and −55°C to +125°C for SM and TM grades. Gain drift is ±30ppm/°C max and bipolar offset drift is ±10ppm of FSR/°C max (high grades). Also included internally is a +6.2V reference. An output voltage compliance range of +2.0V to −0.5V allows the generation of an output voltage without using an external output amplifier. The device is available in both metal and ceramic bottom-brazed packages.

FUNCTIONAL DIAGRAM



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PDS-439B

SPECIFICATIONS

ELECTRICAL

At +25°C and rated supplies unless otherwise specified

MODEL	DAC63CG/CM/TM			DAC63BG/BM/SM			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT							
DIGITAL INPUT							
Resolution			12			•	Bits
Logic Inputs[1]		ECL-compatible			•		
Logic "1" Voltage	−0 78	−0 90	−0 96	•	•	•	V
Current	6 0		33 0	•		•	μA
Logic "0" Voltage	−1 62	−1 75	−1 85	•	•	•	V
Current		10 0			•		nA
Logic Threshold Voltage	−1 20	−1 33	−1 40	•	•	•	V
Current			0 25			•	mA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error			±0 012			•	% of FSR[3]
Differential Linearity Error			±0 012			•	% of FSR
Gain Error[2]		±0 02	±0 1		•	•	%
Offset Error[2] Unipolar		±0 01	±0 04		•	•	% of FSR
Bipolar		±0 02	±0 1		•	•	% of FSR
Monotonicity Temp Range (min)							
CG, CM, BG, BM	−25		+85	•		•	°C
TM, SM	−55		+125	•		•	°C
SETTLING TIME (into 150Ω)							
1LSB Change							
Settling to ±0 012% of FSR							
CM/TM, BM/SM		30	40		40	50	nsec
CG, BG		30	40		35	45	nsec
Full Scale Change							
Settling to ±1% of FSR		17			20		nsec
±0 1% of FSR		30			•		nsec
±0 024% of FSR							
CM/TM, BM/SM		55	65		65	75	nsec
CG, BG		35	50		40	55	nsec
±0 012% of FSR							
CM/TM, BM, SM		70			80		nsec
CG, BG		40			•		nsec
Glitch Energy[4]		250			•		LSB/nsec
DRIFT (over specified temp range)							
Gain		±15	±30		±20	±40	ppm/°C
Offset Unipolar		±0 3	±0 6		±0 5	±1	ppm/°C
Bipolar			±10			±15	ppm/°C
Linearity Error							
(over specified temp range)			±0 012			±0 025	% of FSR
Differential Linearity Error							
(over specified temp range)			±0 025			±0 05	% of FSR
OUTPUT							
ANALOG OUTPUT							
Output Current		0 to 10, ±5			•		mA
Output Voltage Ranges							
with External Op Amp		0 to +10, ±5			•		V
without External Op Amp[5]		0 to +1 5, ±0 5			•		V
Output Impedance without							
External Op Amp							
Unipolar Positive		150			•		Ω
Negative		200			•		Ω
Bipolar		170			•		Ω
Compliance Voltage	-0 5		+2 0	•		•	V
POWER SUPPLIES AND REFERENCE							
Internal Reference Voltage		+6 2			•		V
Internal Reference Drift		±15			•		ppm/°C
Power Supply Voltages	+13	±15	±18	•	•	•	V
Power Supply Current +15V		26	31		•	•	mA
-15V		38	46		•	•	mA
Power Supply Sensitivity +15V		±0 0035			•		%/%ΔV
−15V		±0 0004			•		%/%ΔV
Power Dissipation		960	1160		•	•	mW

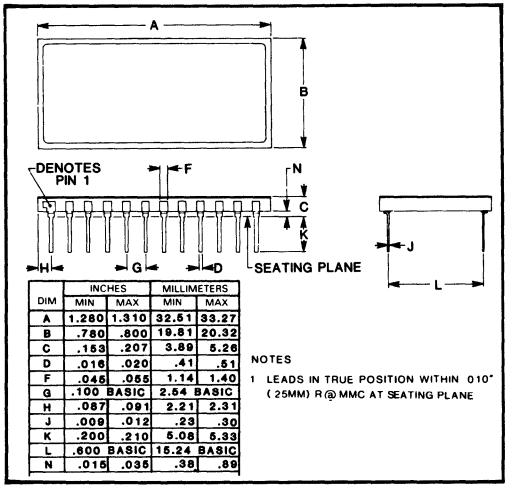
ELECTRICAL (CONT)

MODEL	DAC63CG/CM/TM			DAC63BG/BM/SM			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
PHYSICAL CHARACTERISTICS							
TEMPERATURE RANGE							
Specification. CG, CM, BG, BM	−25		+85	*		*	°C
TM, SM	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C
PACKAGE							
CG, BG	24-pin DIP bottom-brazed ceramic						
CM, TM, BM, SM	24-pin DIP metal						

*Specification same as for DAC63CG/CM/TM

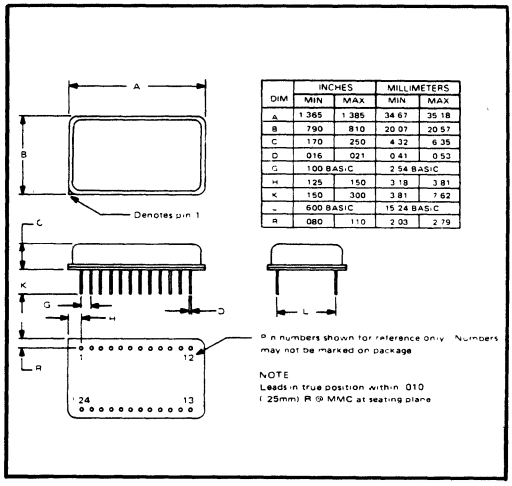
NOTES (1) Logic input voltages and currents are dependent on the logic threshold voltage The logic input values given in each column are correct for the logic threshold voltage given in that column (2) When used with an external output op amp or when the internal impedances/resistors are used as the load (3) FSR is Full Scale Range, which is 10mA for both the DAC63BG and DAC63CG (4) Refer to Output Glitch section (5) Refer to Figures 8 and 9

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.280	1.310	32.51	33.27
B	.780	.800	19.81	20.32
C	.153	.207	3.89	5.26
D	.016	.020	.41	.51
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.087	.091	2.21	2.31
J	.009	.012	.23	.30
K	.200	.210	5.08	5.33
L	.600 BASIC		15.24 BASIC	
N	.015	.035	.38	.89

NOTES
1 LEADS IN TRUE POSITION WITHIN .010" (.25MM) R@MMC AT SEATING PLANE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

PIN ASSIGNMENTS

Pin No	Function
1	Bit 1 (MSB)
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7
8	Bit 8
9	Bit 9
10	Bit 10
11	Bit 11
12	Bit 12 (LSB)
13	GND
14	GND
15	GND
16	GND
17	GND
18	Feedback Resistor Connection
19	Current Output
20	Bipolar Offset
21	Bipolar Offset
22	Logic Threshold
23	+15VDC
24	-15VDC

DISCUSSION OF SPECIFICATIONS

ACCURACY

Linearity of a D/A converter is one of the true measures of its performance. The linearity error of the DAC63 is specified over its entire temperature range. The analog output will not vary by more than ±1/2LSB from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over the specified temperature range is guaranteed to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for the DAC63 at t_{min}, +25°C, and t_{max}; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications (includes internal reference).

Offset Drift is a measure of the actual change in output around zero over the specified temperature range. The offset is measured at t_{min}, +25°C, and t_{max}. The maximum change in Offset is referenced to the Offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of the DAC63 is +2.0V and −0.5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltage. To insure precision operation, each supply lead should be bypassed to ground as close to the unit as possible with a 1μF CS-type tantalum capacitor.

GROUNDING

Care must be exercised when grounding the DAC63 (pins 13, 14, 15, 16, and 17). In order to preserve the stated linearity and accuracy specifications it is necessary to use the ground pins as the analog ground reference point. Any voltage drop that develops between any of these five pins and the actual ground reference point will degrade the performance of the DAC63. To achieve fast settling performance it is recommended that pins 13 through 17 be returned directly to a ground plane (see Figure 1). The analog ground should be located as close to the DAC63 as possible. Otherwise, the accuracy will be degraded by the voltage drop in the ground lines.

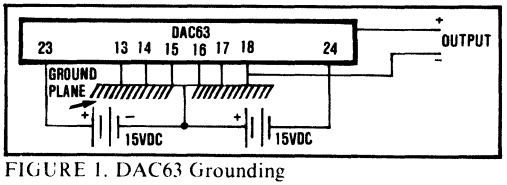


FIGURE 1. DAC63 Grounding

DIGITAL INTERFACE, LOGIC THRESHOLD, AND NOISE IMMUNITY

The DAC63 is compatible with conventional ECL logic families such as ECL 10,000. The circuit diagram shows that the equivalent circuit of each DAC63 digital input is the base of one side of a differential amplifier. The logic 1 input voltage is −0.85V with a typical input current of 8μA. The logic 0 input voltage is −1.75V with an input current of less than 8nA.

The Logic Threshold function of the DAC63 is very important in dealing with noise in the ECL input-driving circuitry. The ECL 10,000 logic family has a noise immunity of 125mV maximum. It has a temperature coefficient of −1.4mV/°C and a power supply sensitivity of 16mV/%ΔV. With a realistic condition of a 5% power supply variation and a 25°C temperature change, the noise immunity would be degraded to 10mV. In addition, a precision D/A converter is more susceptible to noise than is the ECL logic. Noise at levels acceptable to the logic can couple through the D/A, resulting in an unacceptably noisy output.

Through the logic threshold input, the threshold voltage of the DAC63 is dynamically adjusted as the temperature and power supplies vary to give maximum noise immunity at the analog output over a wide range of conditions.

If an MC10115 line receiver (or similar logic function) is used to drive the DAC63 input, the logic threshold pin can be driven by the V_{BB} output of the ECL gate. Refer to an ECL 10,000 data book for more detail. Figure 2 shows alternate methods for generating the drive signal for logic threshold, pin 22.

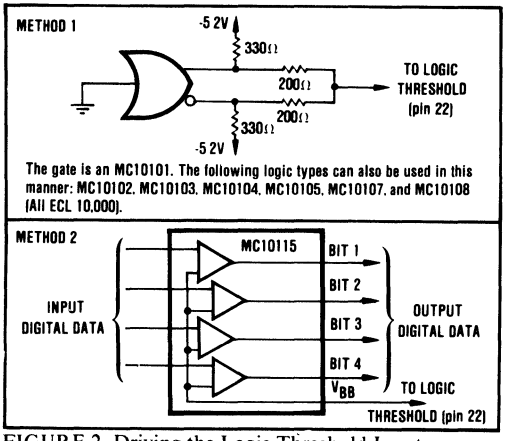


FIGURE 2. Driving the Logic Threshold Input.

SETTLING TIME

Settling time for the DAC63 is the total time required for the output to settle within an error band around its final value after a digital input change. This time includes the digital delay of the internal switches.

The settling time of the DAC63 is determined by digitizing the output waveform produced by toggling the inputs between 011111111111 and 100000000000 continuously and verifying the output settles to within ±1/2LSB in the specified time. The testing technique used is described in detail in Application Note AN-115 which can be obtained from the factory.

Figure 3 shows a typical settling time curve of the DAC63 versus output error. This curve is for full-scale digital code changes. Figure 4 is a photograph showing typical output response characteristics of the DAC63.

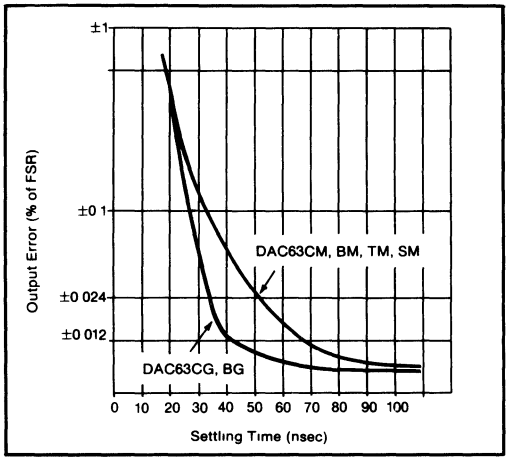


FIGURE 3. Output Error vs Settling Time (typical).

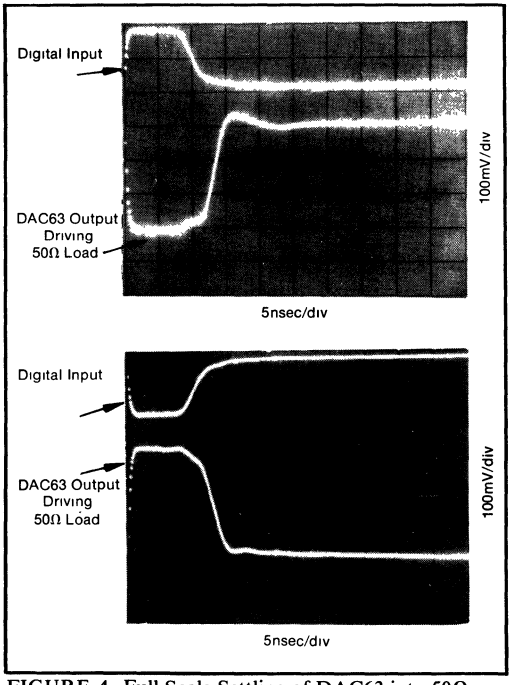


FIGURE 4. Full Scale Settling of DAC63 into 50Ω Load.

In order to achieve minimum settling time it is necessary to observe the following good high frequency construction techniques:

1. The power supplies, including the logic threshold input (pin 22), should be bypassed by 1μF CS-type tantalum capacitors.
2. Use a ground plane to connect common ground points.
3. Remove the ground plane from underneath signal lines where it would add capacitance.
4. Separate analog and digital signal leads to avoid coupling of the digital signal into the analog paths.
5. Bring the source of the digital driving signal as close to the inputs of the DAC63 as possible. If the digital inputs are not clean it will be necessary to reshape them using registers or line drivers. Figure 6 shows how to interface the DAC63 to an input register. It is recommended that the logic power line be bypassed near the digital logic circuitry as a further measure to achieve clean signals.
6. If possible, the DAC63 should be soldered directly into the printed circuit board since connector lead length will cause ringing in the output.

OUTPUT GLITCH

"Glitch" is defined as the difference in the waveforms at the output of the DAC if there is data skew and if there is not. The measurement of glitch is accomplished by measuring the area between these two waveforms.

An output glitch of less than 250LSB-nsec is achievable with the DAC63 because it employs ECL circuitry with current switches that have virtually identical delay times for logic signals making either positive or negative transitions. A glitch results when the digital data changes from one code to the next and the bits do not all switch at the same time. The delay time between the earliest and latest switching bits is called skew time. Typically during the skew time of the digital data, which includes the DAC switching, the digital code is undefined and the DAC output can go to any voltage between the full scale extremes. The glitch creates a noisy output which can be troublesome in some applications such as precision displays and complex waveform generation. Figure 5 is a photograph of a scope trace of the DAC output with a glitch occurring at the major carry transition.

The DAC63 design has been optimized for low glitch energy. However, a further reduction in the output glitch can be achieved by adjusting the skew of the higher order bits of the driving circuitry and by adjusting the logic threshold. This can be done by connecting a variable capacitor from the data lines to ground on each of the first three significant bits (more than three lines may be adjusted if desired). Refer to Figure 6. It will be necessary to create a driving digital code pattern that causes a major carry transition around these bits. It is convenient to use a digital ramp from a counter for this purpose. Initially set the logic threshold exactly half-way between logic 1 and a logic 0. This will be about −1.3V. Then

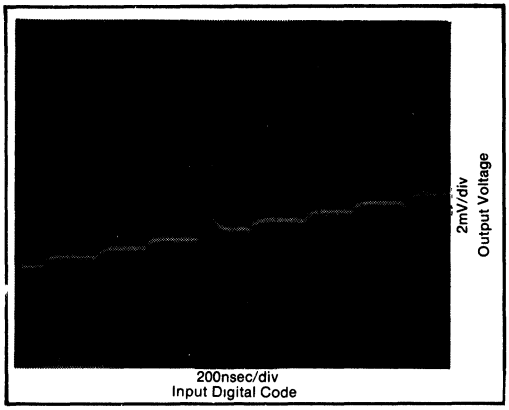


FIGURE 5. Typical Glitch Repsonse of DAC63 at Major Carry Transition with a 1.6V Full Scale Range.

examine the major carry transition associated with bit 3 and adjust the capacitor for minimum glitch. Make the same adjustment to bit 2 and then to bit 1. If done in this order, interactions will be minimized. Finally, fine tune the response by adjusting the logic threshold voltage (pin 22) for minimum glitch. It may be necessary to repeat this procedure once or twice for complete optimization.

OUTPUT CONFIGURATIONS AND APPLICATIONS INFORMATION

The DAC63 contains two 1.24kΩ resistors for generating the bipolar offset current and a 1kΩ resistor which is primarily used as the feedback resistor when used with an external op amp. This thin-film network is constructed on sapphire to provide excellent temperature tracking capability inherent in thin-film networks. These internal resistors along with other internal resistors cause the DAC63 output, in any mode, to be a ratiometric product of the reference. The feedback resistor has very low power sensitivity so that linearity is maintained independent of digital code changes. Because this resistor is constructed on a sapphire network, it is possible to have both superior tracking and low capacitance. Figure 7 shows the DAC63 connected to an external op amp in unipolar and bipolar modes. With the Burr-Brown model OPA600 it is possible to achieve settling times to ±0.01% accuracy in 150nsec. Many of the output accuracy and linearity specifications are given when connected to an external op amp.

For highest speed operation, the DAC63 should be used without an external op amp. Figures 8 and 9 show how to connect the DAC63 for bipolar and positive unipolar

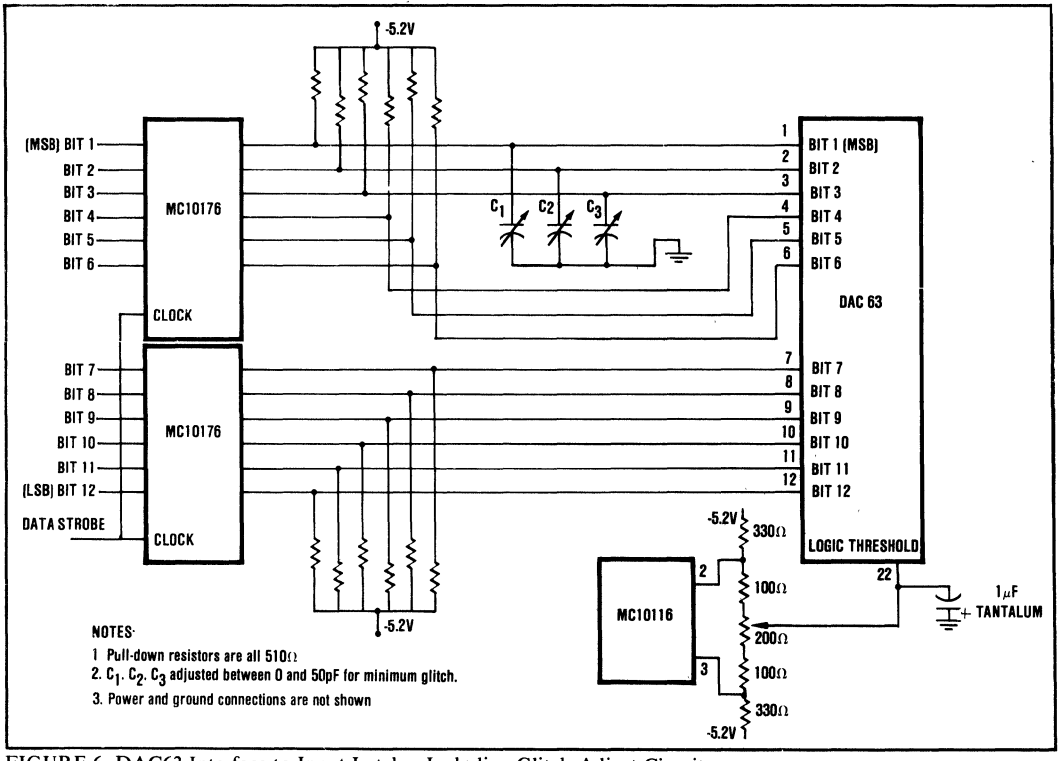
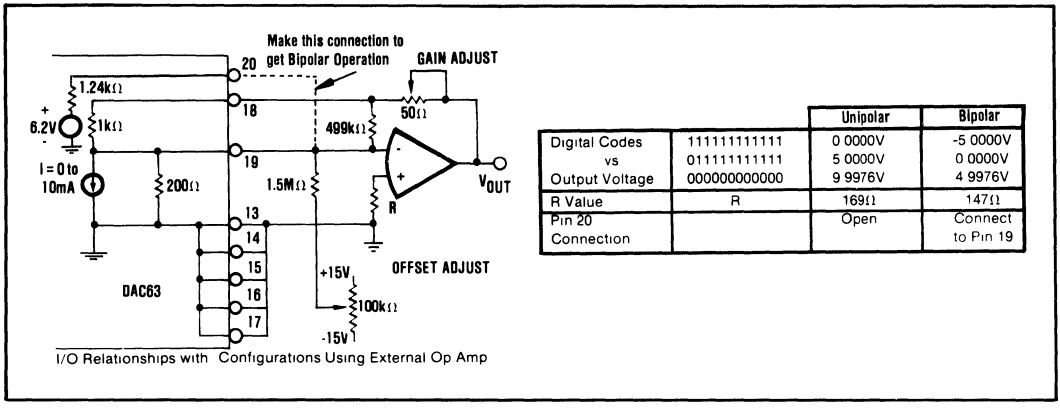


FIGURE 6. DAC63 Interface to Input Latches Including Glitch-Adjust Circuitry.

operation. Figure 10 illustrates how to connect the DAC63 to construct a fast A/D converter. The ADC attempts to create a null at the DAC output, so it is possible to clamp the output voltage with a pair of diodes, thereby avoiding the negative compliance limit.



		Unipolar	Bipolar
Digital Codes vs Output Voltage	111111111111	0 0000V	-5 0000V
	011111111111	5 0000V	0 0000V
	000000000000	9 9976V	4 9976V
R Value	R	169Ω	147Ω
Pin 20 Connection		Open	Connect to Pin 19

FIGURE 7. Bipolar and Unipolar Output Connections when Used with External Op Amp.

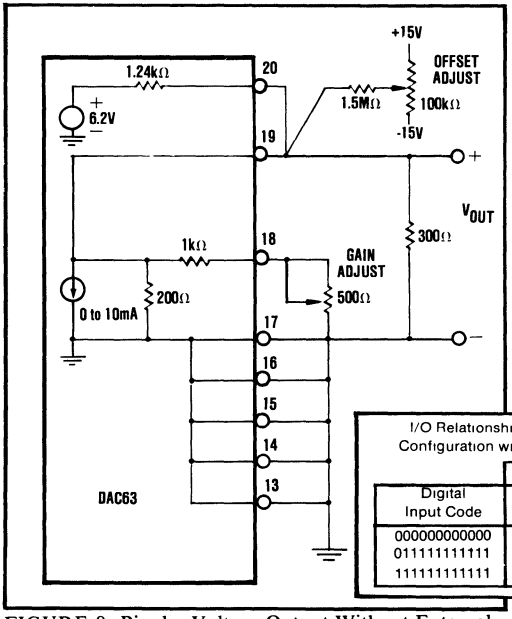


FIGURE 8. Bipolar Voltage Output Without External Op Amp.

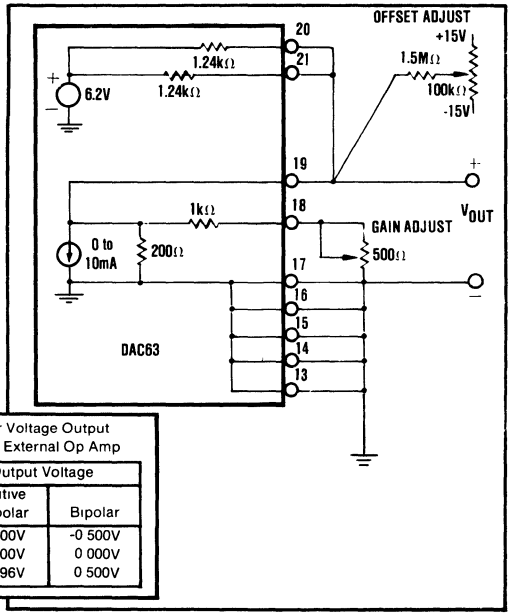


FIGURE 9. Positive Unipolar Voltage Output Without External Op Amp.

I/O Relationships for Voltage Output Configuration without External Op Amp

Digital Input Code	Output Voltage: Positive Unipolar	Output Voltage: Bipolar
000000000000	0 0000V	-0 500V
011111111111	0 7500V	0 000V
111111111111	1 4996V	0 500V

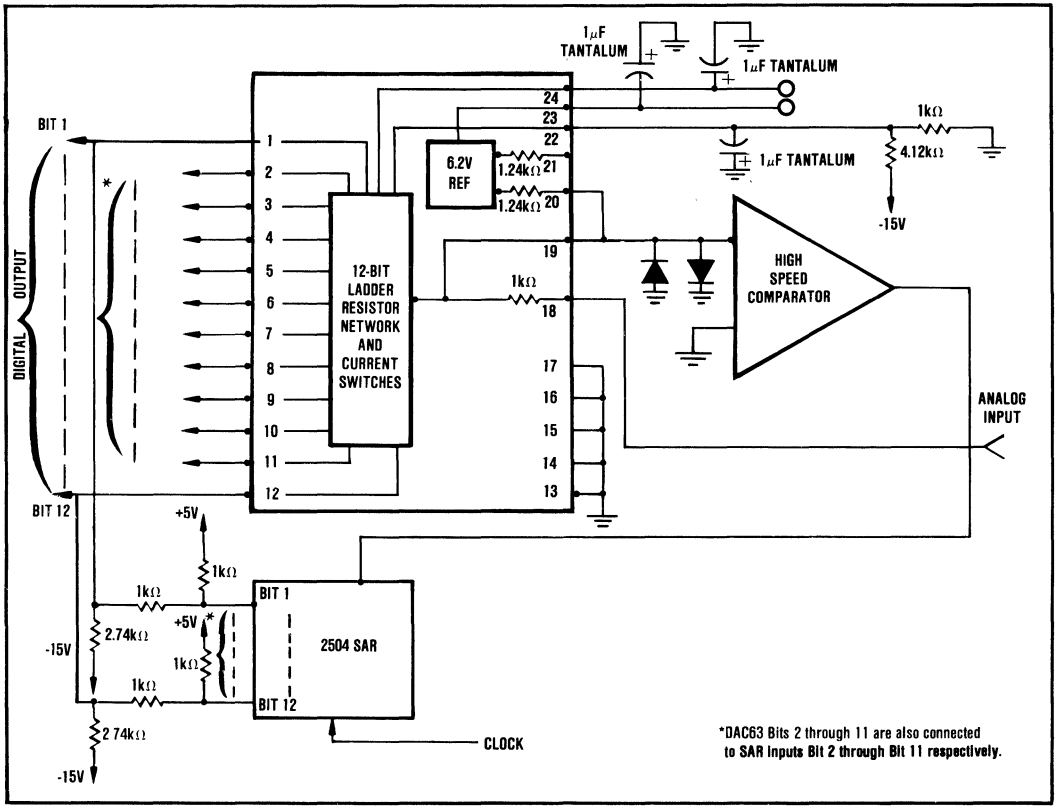


FIGURE 10. DAC63 Used in a Fast A/D Converter.

BURR - BROWN®

DAC65

ADVANCE INFORMATION SUBJECT TO CHANGE

12-Bit Video DIGITAL-TO-ANALOG CONVERTER

FEATURES

- FAST SETTLING: 35ns (0.012%)
- INTEGRAL LINEARITY ERROR: 1/4 LSB
- DIFFERENTIAL LINEARITY ERROR: 1/4 LSB
- HIGH SPECTRAL PURITY: –65dBC
- MONOLITHIC
- 24-PIN DIP PACKAGE
- 0°C TO +70°C AND –55° TO +125°C

APPLICATIONS

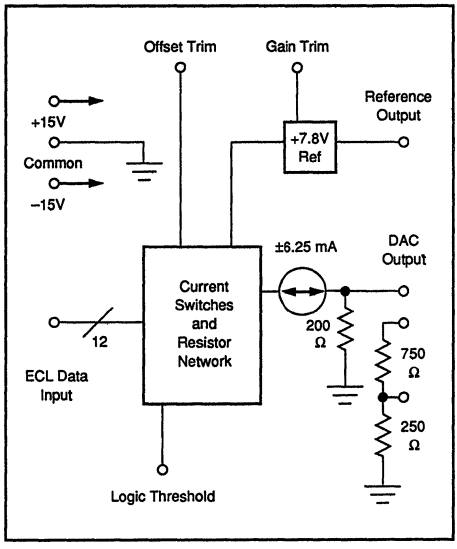
- DIRECT DIGITAL FREQUENCY SYNTHESIZERS
- FAST ATE SYSTEMS
- ARBITRARY WAVEFORM GENERATORS
- HIGH-RESOLUTION VIDEO GRAPHICS
- DIGITAL-TO-ANALOG RECONSTRUCTION
- SPREAD SPECTRUM LOCAL OSCILLATOR

DESCRIPTION

The DAC65 is a fast-settling monolithic 12-bit digital-to-analog converter. Excellent linearity and accuracy are achieved with laser trimmed thin film nichrome resistor networks. The DAC features bipolar output voltage or current. It includes an internal voltage reference and a resistor network which can be used with an external op amp.

Low harmonic distortion and spurious products together with a low quantizing noise floor make the DAC65 a good choice for direct digital frequency synthesizer applications. High accuracy and low gain drift allow its use in high-speed test equipment designs. Low-noise ECL logic is used to preserve clean analog output spectral performance.

The DAC65 is available in two temperature ranges: OC to +70C (JG and KG) and –55C to +125C (SG). It is packaged in a 24-pin ceramic DIP.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491 • FAX: (602) 889-1510

PDS-866

SPECIFICATIONS

ELECTRICAL

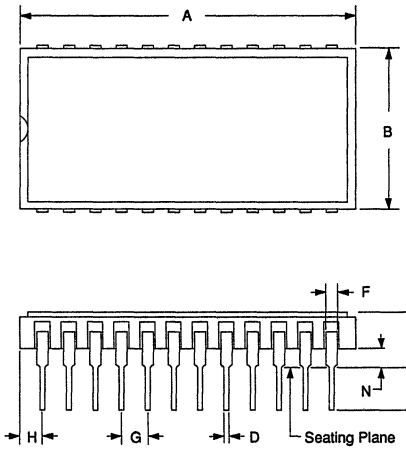
T_C = +25°C, $\pm V_{CC}$ = ±15V, AND 5-MINUTE WARM-UP IN A NORMAL CONVECTION ENVIRONMENT UNLESS OTHERWISE NOTED.

PARAMETER	CONDITIONS	DAC65JG MIN	DAC65JG TYP	DAC65JG MAX	DAC65KG/SG MIN	DAC65KG/SG TYP	DAC65KG/SG MAX	UNITS
INPUTS								
DIGITAL INPUT								
Resolution				12			*	Bits
ECL Logic Input Levels: V_{IL}	I_{IL}	–1.15		–0.88	*		*	V
V_{IH}	I_{IH}	–1.81		–1.475	*		*	V
I_{IL}	V_{IL}	0.5	1.2	2.0	*	*	*	mA
I_{IH}	V_{IH}	0.5	1.2	2.0	*	*	*	mA
Logic Threshold: Voltage		–1.2	–1.3	–1.4	*	*	*	V
Current		1.5	2.3	3.2	*	*	*	mA
TRANSFER CHARACTERISTICS								
ACCURACY								
Linearity Error				±1/2			±1/4	LSB
Differential Linearity Error				±3/4			±1/2	LSB
Bipolar Gain Error			±0.12	±1		±0.08	±0.125	%FSR(1)
Trim Range	R_{TRIM} = 10kΩ		±5			*		mV
Bipolar Zero Error			±0.12	±0.2		±0.08	±0.125	%FSR
Trim Range	R_{TRIM} = 10kΩ		±3			*		mV
Monotonicity			Guaranteed			Guaranteed		
Power Supply Rejection	$\pm V_{CC}$ = ±14V to ±16V		–0.0012	±0.1		*	±0.0035	%FSR/%V_{CC}
SETTLING TIME								
Voltage Output:	R_L = 200Ω (Internal)							
1LSB Change								
Settling to ±0.012% FSR			30	40		30	40	ns
Full Scale Change								
Settling to ±1% FSR			17			17		ns
±0.1% FSR			23			23		ns
±0.024% FSR			30			30		ns
±0.012% FSR			35			35		ns
Glitch Energy	Major Carry		250			*		LSB/ns
DRIFT								
Bipolar Gain	T_{MIN} to T_{MAX}		±15			±20		ppm FSR/°C
Bipolar Offset	T_{MIN} to T_{MAX}		±0.3			±0.5		ppm/°C
Linearity Error	T_{MIN} to T_{MAX}			±.74			±.5	LSB
Differential Linearity Error	T_{MIN} to T_{MAX}			±1			±.75	LSB
REFERENCE								
Reference Output Voltage		+6.24	+7.8	+9.36		*		V
Reference Temperature Drift	T_{MIN} to T_{MAX}		±15			*		ppm/°C
OUTPUT								
ANALOG OUTPUT								
Bipolar Output Current	R_L = 0Ω		±6.25			*		mA
Bipolar Output Voltage	R_L = ∞		±1.2			*		V
Output Impedance			200			*		Ω
Internal Resistors: R_1	Pin 18 to pin 20		750			*		Ω
R_2	Pin 18 to pin 15		250			*		Ω
Ratio Accuracy	R_1/R_2		0.01			*		%
Absolute Accuracy	R_1, R_2		0.25			*		%
POWER SUPPLIES								
Rated Voltage	$\pm V_{CC}$		±15			*		V
Derated Performance	$\pm V_{CC}$	±13		±16	*		*	V
Current Quiescent: $+I_{CC}$	V_O = + Full-Scale		24			24		mA
$-I_{CC}$	V_O = + Full-Scale		54			54		mA
Power Dissipation	V_O = + Full-Scale		1.2			*	*	W
TEMPERATURE RANGE								
Specification JG,KG	Case Temperature	0		+70	0		+70	°C
SG					–55		+125	°C
Operating JG, KG	Case Temperature	–25		+85	–25		+85	°C
SG					–55		+125	°C
θ_{JC}			10			10		°C/W
θ_{JA}			25			25		°C/W

NOTES: * Same specifications as for DAC65JG. (1) FSR means Full Scale Range which is 2.5Vp-p. (2) Refer to Output Glitch section.

MECHANICAL

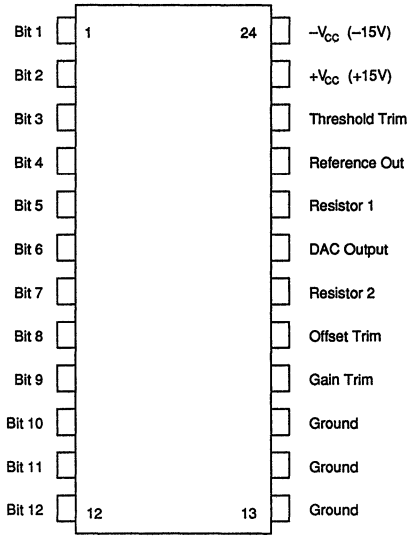
G Package—24-Pin Ceramic DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.238	1.262	31.45	32.05
B	.586	.602	14.88	15.29
C	.160	.196	4.06	4.98
D	.160	.196	4.06	4.98
F	.038	.042	0.97	1.07
G	.100	BASIC	2.54	BASIC
H	.067	.085	1.70	2.16
I	.008	.012	0.12	0.30
J	.008	.012	0.20	0.30
K	.170	BASIC	4.32	BASIC
L	.600	BASIC	15.24	BASIC
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. May not be marked on package. Case: Ceramic. Weight: 4.4 grams (0.16oz)

PIN CONFIGURATION



ORDERING INFORMATION

DAC65 ( ) ( ) Q

Basic Model Number

Performance Grade Code
- J, K: 0°C to +70°C Case Temperature
- S: –55°C to +125°C Case Temperature

Package Code
- G: 24-Pin Ceramic DIP

Reliability Screening
- Q: Q-Screened

ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±18V
Logic Input	0V to –5.2V
Case Temperature	–55°C to +125°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +165°C

Stresses above these ratings may permanently damage the device.

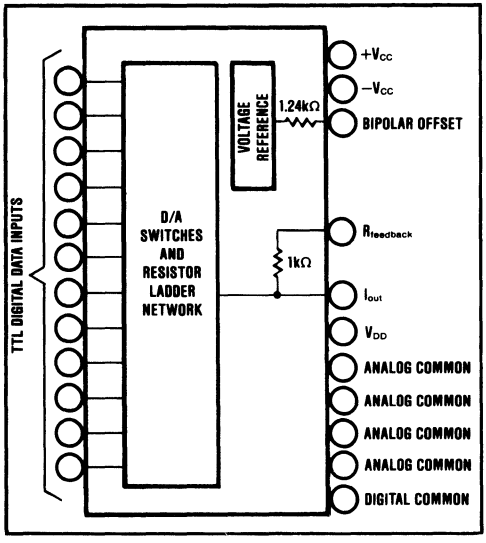
BURR-BROWN®

DAC812

Ultra-High Speed DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 12-BIT RESOLUTION AND ACCURACY
- 55nsec CURRENT OUTPUT SETTLING TIME
- TTL-COMPATIBLE INPUTS
- MONOTONIC OVER ENTIRE TEMPERATURE RANGE
- LINEARITY ERROR LESS THAN ±1/2LSB OVER TEMPERATURE RANGE (C GRADE)
- HERMETIC METAL PACKAGE



DESCRIPTION

The DAC812 is an ultra-fast-settling 12-bit current-output D/A converter with TTL-compatible inputs packaged in a 24-pin dual-wide dual-in-line hermetic metal package.

The current output settles to ±0.012% of full scale range in 55nsec, typical (65nsec, max., C grade; 80nsec, max., B grade).

The DAC812 utilizes a monolithic 12-bit switch chip with stable, compatible thin-film resistors to achieve fast settling time and excellent stability over temperature and time. An internal applications resistor for use with an external op amp is included to convert the output current into a voltage for 0V to +10V or −5V to +5V ranges.

An output voltage compliance range of +4V to −4V allows the generation of an output voltage without using an external output amplifier.

The DAC812 comes in two drift grades. The linearity error of the C grade is guaranteed to be within ±1/2LSB over the temperature range of −25°C to +85°C. Gain drift of the C grade is ±20ppm/°C (max) and bipolar offset drift is ±10ppm of FSR/°C (max). The B grade has a linearity error of ±1LSB over the temperature range and a maximum gain drift and bipolar offset drift of ±40ppm/°C and ±15ppm/°C, respectively.

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SPECIFICATIONS

ELECTRICAL

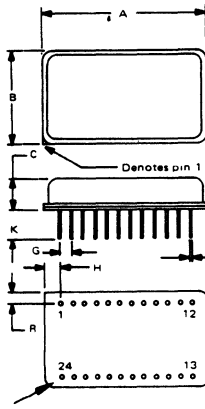
At T_A = +25°C, rated power supplies, and after 5-minute warm-up unless otherwise noted

MODEL	DAC812CM			DAC812BM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT							
DIGITAL INPUT							
Resolution, CSB, COB			12			*	Bits
Logic Inputs. V_{IH}	+2.0		+5.25	*		*	V
V_{IL}	0 0		+0.8	*		*	V
I_{IH}, V_I = +2 7V			+40			*	µA
I_{IL}, V_I = +0 4V			−1 8			*	mA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error		±0.006	±0.012		±0.009	±0 018	% of FSR[1]
Differential Linearity Error			±0.012			±0.018	% of FSR
Gain Error[2]		±0.03	±0.1		*	*	%
Offset Error[2] Unipolar		±0.02	±0.04		*	*	% of FSR
Bipolar		±0.03	±0.1		*	*	% of FSR
Monotonicity Temp. Range (min)	−25		+85	*		*	°C
CONVERSION SPEED							
Settling Time to ±1/2LSB into 150Ω							
For FSR Change		55	65		*	80	nsec
For 1LSB Change		25			*		nsec
DRIFT							
Gain		±10	±20		±20	±40	ppm/°C
Offset: Unipolar		±0.25	±0.5		±0 5	±1	ppm of FSR/°C
Bipolar			±10			±15	ppm of FSR/°C
Linearity Error	±0 012 over Temp. Range (max)			±0 025 over Temp. Range (max)			% of FSR
Differential Linearity Error	±0 025 over Temp Range (max)			±0 04 over Temp. Range (max)			% of FSR
OUTPUT							
ANALOG OUTPUT							
Output Current Unipolar		0 to −10			*		mA
Bipolar		−5 to +5			*		mA
Output Voltage Ranges							
with External Op Amp. Unipolar		0 to +10			*		V
Bipolar		−5 to +5			*		V
Output Impedance: Unipolar		170			*		Ω
Bipolar		150			*		Ω
Output Compliance	−4		+4	*		*	V
POWER SUPPLIES							
Power Supply Sensitivity. $+V_{CC}$			±0.004			*	%FSR/%V_{CC}
$-V_{CC}$			±0 001			*	%FSR/%V_{CC}
V_{DD}			±0.0002			*	%FSR/%V_{DD}
Power Supply Voltages $+V_{CC}$	+11 4	+15	+18	*	*	*	V
$-V_{CC}$	−18	−15	−14	*	*	*	V
V_{DD}	+4.5	+5	+5 5	*	*	*	V
Power Supply Current $+V_{CC}$		+30	+40		*	*	mA
$-V_{CC}$		−40	−50		*	*	mA
V_{DD}		+25	+40		*	*	mA
Power Dissipation		1.2	1.6		*	*	W
PHYSICAL CHARACTERISTICS							
TEMPERATURE RANGE							
Specification	−25		+85	*		*	°C
Storage	−55		+150	*		*	°C
PACKAGE	24-pin Hermetic Metal DIP 0.6" Pin Row Spacing						

*Specification the same as for DAC812CM

NOTES: (1) FSR is full-scale range. (2) Adjustable to zero with external potentiometer. Gain error is specified for unadjusted operation using internal resistor network. See Figure 5 and Figure 6.

MECHANICAL



NOTE
Leads in true position within .010" (.25mm) R at MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

Pin numbers shown for reference only. Numbers may not be marked on package

PIN ASSIGNMENTS

Pin	Function	Pin	Function
1	Bit 1 (MSB, Data Input)	14	Digital Common (V_{DD} Common)
2	Bit 2	15	Analog Common ($\pm V_{CC}$ Common)
3	Bit 3	16	Analog Common
4	Bit 4	17	Analog Common
5	Bit 5	18	Analog Common
6	Bit 6	19	V_{DD} (Logic Supply)
7	Bit 7	20	I_{OUT} (Current Output)
8	Bit 8	21	R_f (Application Resistor)
9	Bit 9	22	BPO (Bipolar Offset)
10	Bit 10	23	$-V_{CC}$ (Negative Analog Supply)
11	Bit 11	24	$+V_{CC}$ (Positive Analog Supply)
12	Bit 12 (LSB)		
13	No connection		

DISCUSSION OF SPECIFICATIONS

ACCURACY

Linearity of a D/A converter is one of the true measures of its performance. The linearity error of the DAC812 is specified over its entire temperature range. The analog output will not vary by more than ±1/2LSB (±1LSB for the BM model) from a best-fit straight line over the specified temperature range of −25°C to +85°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a −25°C to +85°C range is guaranteed to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by 1) testing the end point differences for the DAC812 at t_{min}, +25°C, and t_{max}; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications (includes internal reference).

Offset Drift is a measure of the actual change in output around the minus full-scale point over the specified temperature range. The offset is measured at t_{min}, +25°C, and t_{max}. The maximum change in Offset is referenced to the Offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of the DAC812 is ±4.0V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages. To insure precision operation, each supply lead should be bypassed to ground as close to the unit as possible with a 1μF CS-type tantalum capacitor.

GROUNDING

Care must be exercised when grounding the DAC812 (pins 14, 15, 16, 17, and 18). In order to preserve the stated linearity and accuracy specifications it is necessary to use the ground pins as the analog ground reference point. Any voltage drop that develops between any of these five pins and the actual ground reference point will degrade the performance of the DAC812. To achieve fast settling performance it is recommended that pins 14 through 18 be returned directly to a ground plane (see Figure 1). The analog ground should be located as close to the DAC812 as possible. Otherwise, the accuracy will be degraded by the voltage drop in the ground lines.

SETTLING TIME

Settling time for the DAC812 is the total time required for the output to settle within an error band around its

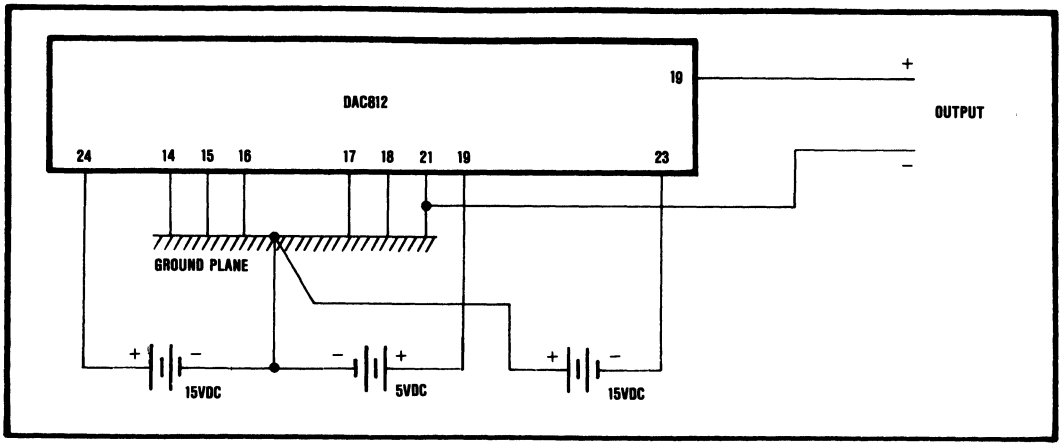


FIGURE 1. DAC812 Grounding Using Feedback Resistor to Generate Output Voltage.

final value after a digital input change. This time includes the digital delay of the internal switches.

Figure 2 shows a typical settling time curve of the DAC812 versus output error. This curve is for full-scale digital code changes. Figures 3 and 4 show typical measured settling time characteristics of the DAC812.

In order to achieve the minimum settling time, it is necessary to observe the following good high frequency construction techniques.

1. The power supplies should be bypassed by 1μF CS-type tantalum capacitors.
2. Use a ground plane to connect common ground points.
3. Remove the ground plane from underneath signal lines where it would add capacitance.
4. Keep analog and digital signal lines physically separated to avoid coupling of the digital signal into the analog paths.

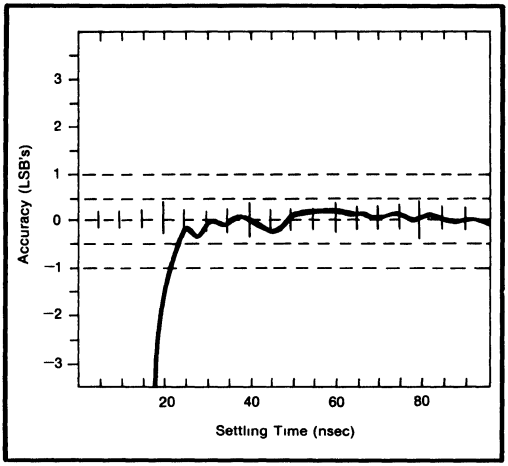


FIGURE 3. Typical DAC812 Negative-to-Positive Full-Scale Output Characteristic.

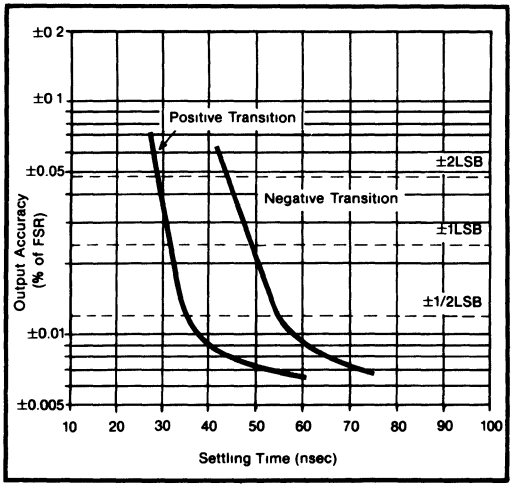


FIGURE 2. DAC812 Typical Settling Time vs. Accuracy

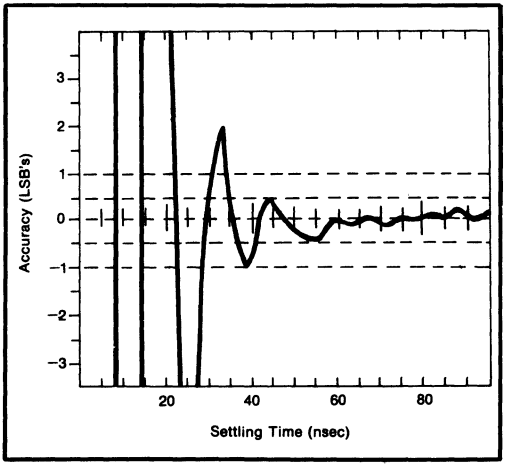


FIGURE 4. Typical Positive-to-Negative Full-Scale Output Characteristic.

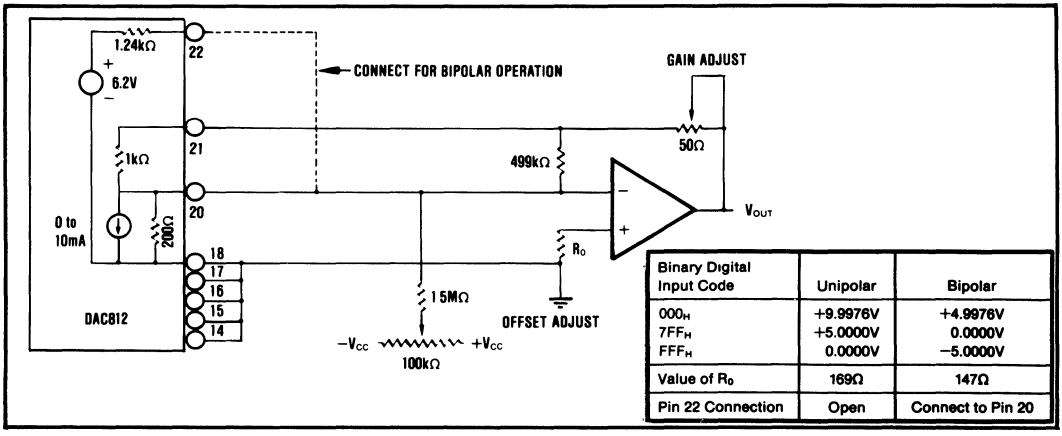
5. Bring the source of the digital driving signal as close to the inputs of the DAC812 as possible. If the digital inputs are not clean it will be necessary to reshape them using registers or line drivers. It is recommended that the logic power line be bypassed near the digital logic circuitry as a further measure to achieve clean signals.
6. If possible, the DAC812 should be soldered directly into the printed circuit board since connector lead length will cause ringing in the output.

OUTPUT CONFIGURATIONS AND APPLICATIONS INFORMATION

The DAC812 contains a 1.24kΩ resistor for generating the bipolar offset current and a 1kΩ resistor which is used as the feedback resistor when used with an external op amp. This thin-film network is constructed on sapphire to provide excellent temperature tracking capability inherent in thin-film networks. These internal resistors along with other internal resistors cause the DAC812 output, in any mode, to be a ratiometric product of the reference. The feedback resistor has very low power sensitivity so that linearity is maintained independent of digital-code changes. Because this resistor is constructed on a sapphire network, it is possible to have both superior tracking and low capacitance.

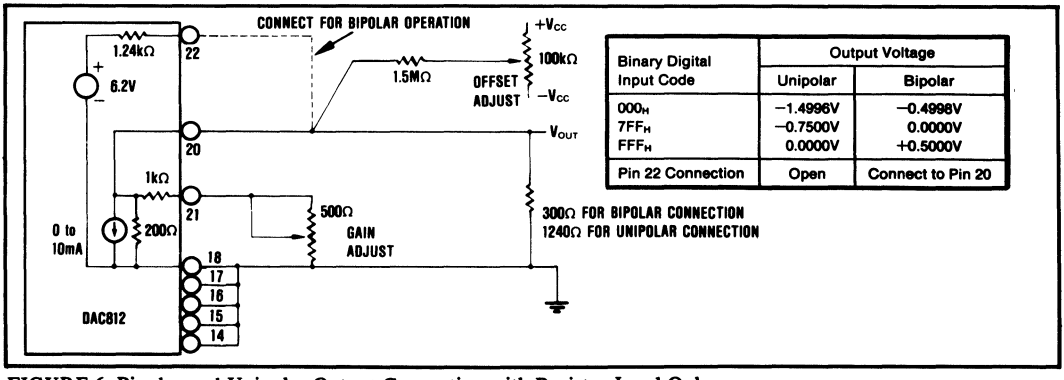
Figure 5 shows the DAC812 connected to an external op amp in unipolar and bipolar modes. When the op amp is a Burr-Brown model OPA600 it is possible to achieve settling times to 0.1% accuracy in 150nsec. Output accuracy and linearity specifications are given when connected to an external op amp.

For highest speed operation, the DAC812 should be used without an external op amp. Figure 6 shows how to connect the DAC812 for bipolar and unipolar operation. Figure 7 illustrates how to connect the DAC812 to construct a fast A/D converter.



Binary Digital Input Code	Unipolar	Bipolar
000_H	+9.9976V	+4.9976V
$7FF_H$	+5.0000V	0.0000V
FFF_H	0.0000V	−5.0000V
Value of R_O	169Ω	147Ω
Pin 22 Connection	Open	Connect to Pin 20

FIGURE 5. Bipolar and Unipolar Output Connections with External Op Amp.



Binary Digital Input Code	Output Voltage	
	Unipolar	Bipolar
000_H	−1.4996V	−0.4998V
$7FF_H$	−0.7500V	0.0000V
FFF_H	0.0000V	+0.5000V
Pin 22 Connection	Open	Connect to Pin 20

FIGURE 6. Bipolar and Unipolar Output Connection with Resistor Load Only.

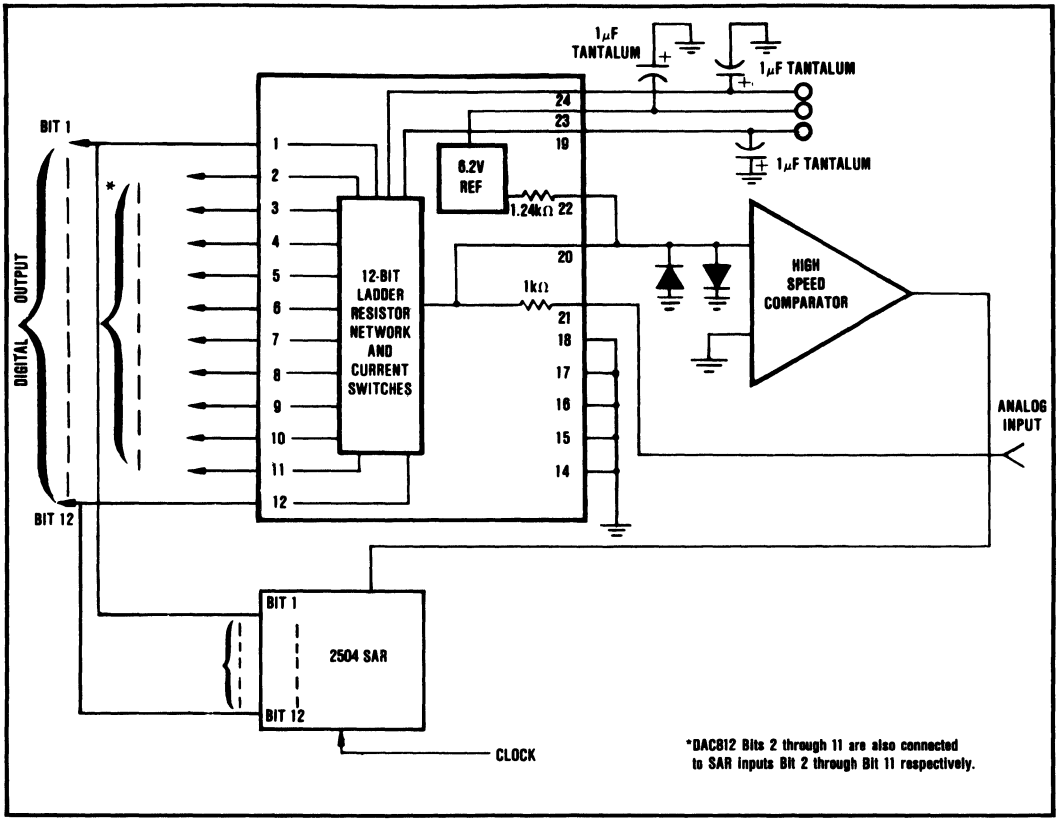


FIGURE 7. DAC812 Used in a Fast A/D Converter.

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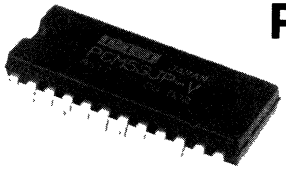


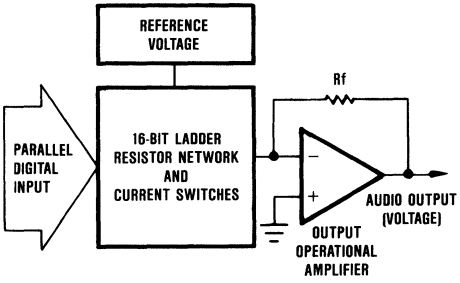
PCM53JP, KP

DESIGNED FOR AUDIO

16-Bit Monolithic DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW COST
- NO EXTERNAL COMPONENTS REQUIRED
- 16-BIT RESOLUTION
- 16-BIT MONOTONICITY, typ
- 0.001% OF FSR TYP DIFFERENTIAL LINEARITY ERROR
- 0.0025% max THD (FS Input, KP Grade, 16 Bits)
- 0.02% max THD (−20dB Input, KP Grade, 16 Bits)
- 3μsec SETTLING TIME, typ
- 96dB DYNAMIC RANGE
- ±10V AUDIO OUTPUT
- EIAJ STC-007 COMPATIBLE
- INDUSTRY-STANDARD PINOUT
- COMPACT, PLASTIC DIP PACKAGE



DESCRIPTION

The PCM53 family of converters are state-of-the-art, fully monolithic, digital-to-analog converters that are designed and specified for digital audio applications. These devices employ a segmented architecture and ultra-stable, nichrome (NiCr), thin-film, well-matched resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature range.

The PCM53 converters are completely self-contained with stable, low noise, internal, zener voltage reference; high speed current switches; resistor ladder network; and fast-settling, low noise, output operational amplifier all on a single monolithic chip. A special, open-loop reference circuit helps provide the fast settling time required for critical audio applications. The converters can be operated using two power supplies (±15V) instead of three separate supplies. Few external components are necessary for operation, and all critical specifications are 100% tested. This helps to assure the user of high system reliability and outstanding overall system performance.

The current output models settle to within ±0.006% of FSR final value in typically 350nsec in response to a full-scale change in the digital input code.

These converters are packaged in a high-quality molded plastic package and have passed operating life tests under simultaneous high-pressure, high-temperature and high humidity conditions.

The letters V and I (e.g. PCM53JP-V and PCM53KP-I) refer to the voltage-output and current-output models respectively.

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PDS-575

SPECIFICATIONS

ELECTRICAL

T_A = +25°C rated power supplies unless otherwise noted

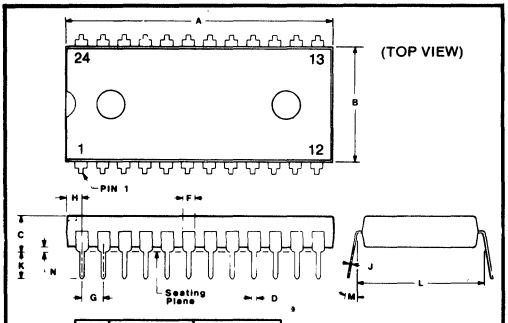
MODEL	PCM53JP-I, -V			PCM53KP-I, -V			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT							
DIGITAL INPUT							
Resolution		16			*		Bits
Dynamic Range		96			*		dB
Logic Levels (TTL/CMOS Compatible Logic "1" at +40μA	+2 4		+V_{CC}	*		*	VDC
Logic "0" at −0 5mA	0		+0 8	*		*	VDC
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error		±0 1	±2 5		*	±1 0	%
Bipolar Zero Error[1]		±10	±200		*	±50	mV
Differential Linearity Error at Bipolar Zero		0 001	0 005		*	0 003	% of FSR[2]
Noise (rms) (20Hz to 20kHz) at Bipolar Zero (V_{OUT} models)		30	60		*	*	μV
TOTAL HARMONIC DISTORTION[3] (16-Bit Resolution)							
V_o = ±FS at f = 420Hz		0 002	0 004		*	0 0025	%
V_o = −20dB at f = 420Hz		0 02	0 04		*	0 02	%
V_o = −60dB at f = 420Hz		1 9	4 0		*	2 0	%
MONOTONICITY		16			*		Bits
DRIFT (0°C to +70°C)							
Total Bipolar Drift (includes gain, offset, and linearity drift)		±25	±150		*	*	ppm of FSR/°C
		±0 1	±0 68		*	*	% of FSR
		±0 01	±0 06		*	*	dB
Bipolar Zero Drift		±4	±20		*	*	ppm of FSR/°C
SETTLING TIME (to ±0 006% of FSR)							
Voltage Models Output 10V Step		3			*		μsec
1LSB Step		1			*		μsec
Current Models Output (1mA Step) 10Ω to 100Ω Load		350			*		nsec
1kΩ Load[4]		350			*		nsec
Deglitcher Delay (THD Test)[5]		2 5	4 0		*	*	μsec
Slew Rate		10			*		V/μsec
WARM-UP TIME	1			*			Min
OUTPUT							
ANALOG OUTPUT							
Voltage Models Output Voltage Range	±9 75	±10	±10 25	±9 90	*	±10 1	V
Output Current	±5			*			mA
Output Impedance		0 1			*		Ω
Short-Circuit Duration		Indefinite to Common			*		
Current Models Output Current Range(±30%)		±1			*		mA
Output Impedance (±30%)		2 4			*		kΩ
POWER SUPPLY							
SENSITIVITY							
+V_{CC}		±0 001			*		% of FSR/%V_{CC}
−V_{CC}		±0 001			*		% of FSR/%V_{CC}
V_{DD}		±0 001			*		% of FSR/%V_{CC}
POWER SUPPLY REQUIREMENTS							
Voltage ±V_{CC}[6]	±14 25	±15	±15 75	*	*	*	VDC
V_{DD}[6]	+4 75	+5	+15 75	*	*	*	VDC
(V_{DD} may be connected to +V_{CC} supply voltage Result is slightly increased total power dissipation of approximately 40mW)							
Supply Drain (no load) +V_{CC}[6]		+18	+30		*	*	mA
−V_{CC}[6]		−18	−30		*	*	mA
V_{DD}[6]		+4	+10		*	*	mA
TEMPERATURE RANGE							
Specification	0		+70	*		*	°C
Operating	−25		+85	*		*	°C

NOTES (1) Adjustable to zero with external potentiometer (2) FSR means Full-Scale Range and is 20V for ±10V voltage output models and 2mA for ±1mA current output models (3) The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit A block diagram of a measurement circuit is shown in Figure 2 Burr-Brown may calculate THD from the measured linearity errors using equation 2 in the section on "Total Harmonic Distortion," but specifies that the maximum THD measured with the circuit shown in Figure 2 will be less than the limits indicated (4) Measured with an active clamp to provide a low impedance for approximately 200nsec (5) Deglitcher or Sample/Hold delay used in THD measurement test circuit See Figures 2 and 3 (6) See Connection Diagram and Pin Assignments

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages	±18VDC
Input Logic Voltage	−1V to +Supply Voltage
Storage Temperature	−55°C to +100°C
Lead Temperature During Soldering	10sec at +300°C

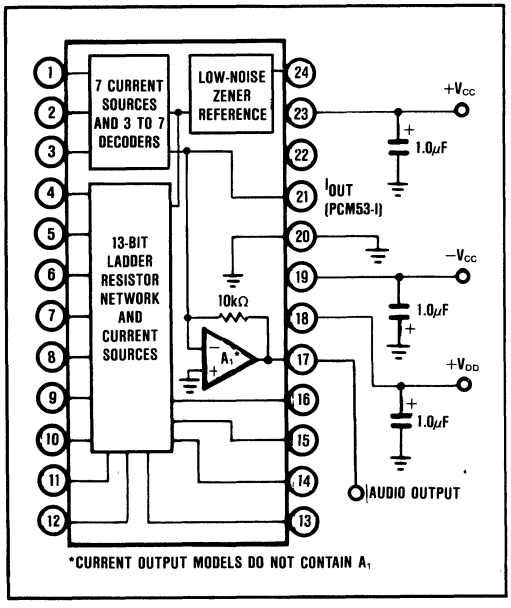
MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.233	1.263	31.32	32.59
B	.535	.575	13.67	14.61
C	.169	.224	4.29	5.70
D	.015	.023	0.38	0.58
F	.043	.062	1.09	1.57
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.132	2.54	3.35
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.022	0.46	0.56

NOTE
Leads in true position within 0.10" (0.25mm R at MMC at seating plane.

CONNECTION DIAGRAM



*CURRENT OUTPUT MODELS DO NOT CONTAIN A1

PIN ASSIGNMENTS

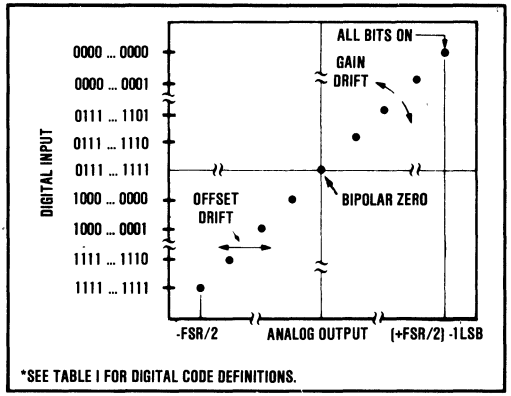
Pin No.	PCM53KP-V, PCM53JP-V	PCM53KP-I, PCM53JP-I
1	Bit 1 (MSB)	Bit 1 (MSB)
2	Bit 2	Bit 1
3	Bit 3	Bit 3
4	Bit 4	Bit 4
5	Bit 5	Bit 5
6	Bit 6	Bit 6
7	Bit 7	Bit 7
8	Bit 8	Bit 8
9	Bit 9	Bit 9
10	Bit 10	Bit 10
11	Bit 11	Bit 11
12	Bit 12	Bit 12
13	Bit 13	Bit 13
14	Bit 14	Bit 14
15	Bit 15	Bit 15
16	Bit 16 (LSB)	Bit 16 (LSB)
17	±10V Audio Out	R_f (10kΩ ±30%)
18	V_{DD}	V_{DD}
19	$-V_{CC}$	$-V_{CC}$
20	Common	Common
21	Summing Junction	I_{OUT}, ±1mA ±30% (Audio Output)
22	Test Point	Test Point
23	$+V_{CC}$	$+V_{CC}$
24	Reference Out (+6.3V)	Reference Out (+6.3V)

ORDERING INFORMATION

Model No.	Output Configuration
PCM53JP-I	±1mA
PCM53KP-I	±1mA
PCM53JP-V	±10V
PCM53KP-V	±10V

THEORY OF OPERATION AND AUDIO SPECIFICATIONS

The transfer function of an ideal binary D/A converter is a set of discrete output levels that lie on a straight line as shown in Figure 1. The number of possible discrete output levels, or resolution, is equal to 2^n where n is the number of digital inputs or "bits". The PCM53 has 2^{16} or 65,536 possible output levels. Another method of expressing resolution that is useful in audio applications is Dynamic Range.



*SEE TABLE I FOR DIGITAL CODE DEFINITIONS.

FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

DYNAMIC RANGE

The Dynamic Range is a measure of the ratio of the smallest signals the converter can produce to the full-scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 × n, or about 96dB for a 16-bit converter. The actual, or useful, dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit. However, this does point out that a resolution of at least 16 bits is required to obtain a 90dB minimum dynamic range, regardless of the accuracy of the converter. Another specification that is useful for audio applications is Total Harmonic Distortion (THD).

TOTAL HARMONIC DISTORTION

THD is useful in audio applications and is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quantization Error. To be useful, THD should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications.

The THD is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency and is expressed in percent or dB. A block diagram of the test circuit used to measure the THD of the PCM53 is shown in Figure 2. A timing diagram of the control logic is shown in Figure 3.

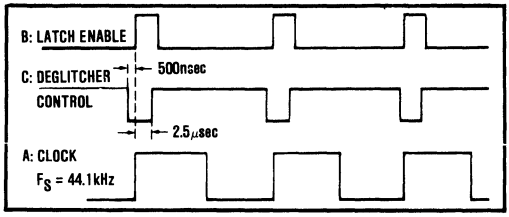


FIGURE 3. Control Logic Timing for PCM53 Distortion Test Circuit.

If we assume that the error due to the test circuit is negligible, then the rms value of the PCM53 error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2} \qquad (1)$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the PCM53 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \frac{\epsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\% \qquad (2)$$

where E_{rms} is the rms signal-voltage level.

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of

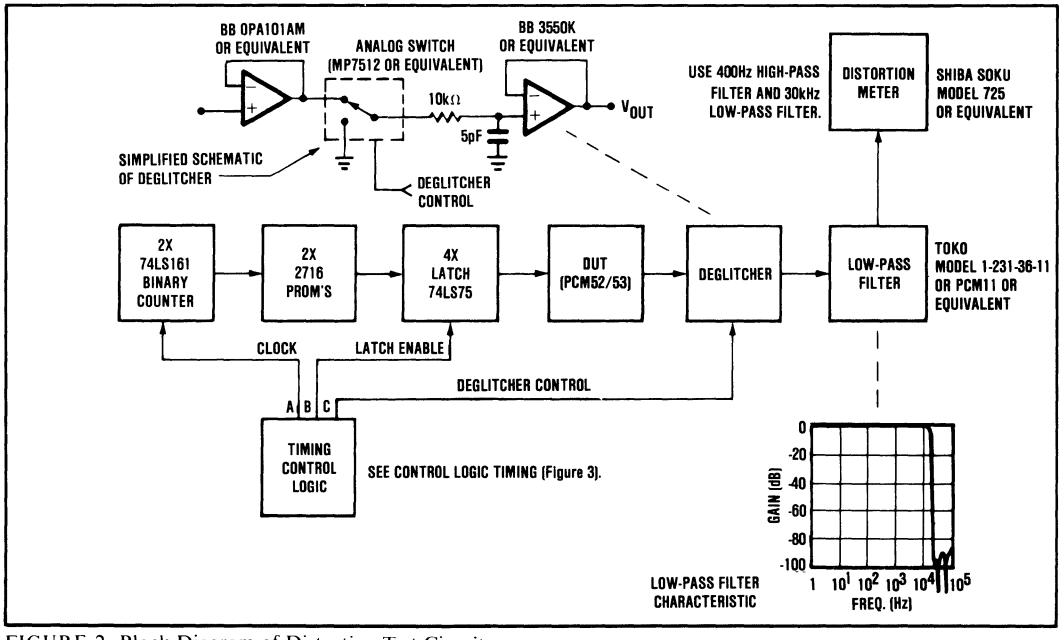


FIGURE 2. Block Diagram of Distortion Test Circuit.

the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

For the PCM53 the test period was chosen to be 22.7μsec (44.1kHz) which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 420Hz and the amplitude of the input signal is 0dB, −20dB, and −60dB down from full scale.

Figure 4 shows the typical THD as a function of output voltage.

Figure 5 shows typical THD as a function of frequency.

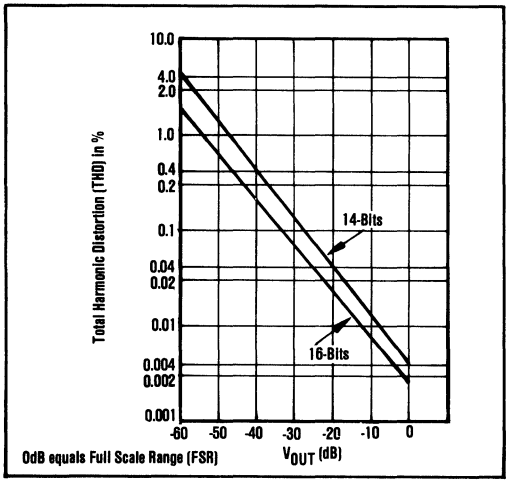


FIGURE 4. Total Harmonic Distortion (THD) vs V_{OUT}.

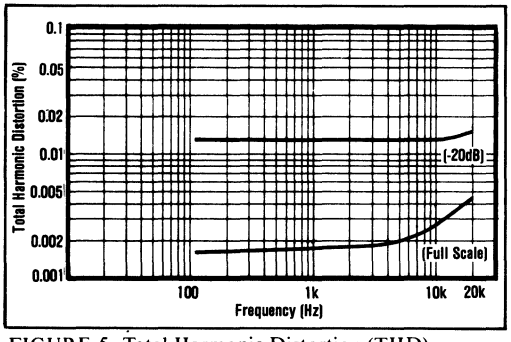


FIGURE 5. Total Harmonic Distortion (THD) vs Frequency.

DIGITAL INPUT CODES

The PCM53 accepts complementary digital input codes in binary format. It may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes. See Table I.

TABLE I. Digital Input Codes.

DIGITAL INPUT CODES				
			COB	CTC*
	MSB	LSB	Complementary Offset Binary	Complementary Two's Complement
All bits ON	0000	000	+Full Scale	-1LSB
Mid Scale	0111	111	Zero	-Full Scale
All bits OFF	1111	111	-Full Scale	Zero
	1000	000	-1LSB	+Full Scale

*A TTL inverter must be connected between the MSB input signal and bit 1 (pin 1) to obtain CTC input code

DETAILED THEORY OF OPERATION

In the basic design, the three functions represented by the complete D/A converter—the voltage reference, the output amplifier, and the converter—are distributed among six major circuit blocks (Figure 6). Three blocks—the open loop reference, the current-offset circuit, and the reference output amplifier—perform the reference functions. The D/A conversion is performed by two circuits called the upper converter and the lower converter, which are combined into the voltage output by the on-chip output op amp.

The prime requirements for a D/A converter circuit designed for PCM audio applications are that it have low differential linearity error and monotonicity and that it stay that way over a useful temperature range. To obtain this performance at 14 to 16 bits, the converter combines segmentation with multiple R-2R networks.

The upper converter, which generates the three most significant bits, is made up of seven equal current sources (Q_1 R_{E1} through Q_7 R_{E7}), each providing 0.25mA. Together the sources form the upper converter current, I_{DACU}.

The three binary-coded MSBs (bits 1, 2, and 3) are decoded by a three-to-seven-line circuit, which sequentially selects the equal current sources as the binary code formed by the bits changes through the eight values (000 to 111). Thus, as the code ranges through its values, I_{DACU} changes from 0 to 1.75mA. This scheme ensures monotonicity, reduces initial matching and tracking requirements, and cuts the tracking errors that occur with temperature and time.

Averaging Transistor and Resistor Shifts

To further improve the tolerance of the upper converter to time and temperature change, the seven equal currents are turned on in the following order: Q_4, Q_2, Q_7, Q_5, Q_1, Q_6, Q_3. This sequence, which produces the zero-to-full-scale output, averages the shifts that occur in transistor parameters and in the value of the emitter resistors.

The 13 least significant bits are produced by the lower converter, which uses nine more equal-current sources for the nine middle bits and emitter area rationing for the 4LSBs. However, rather than being summed directly by the current of the upper converter (which would have required $2^{16} - 1$ equal current sources) the current sour-

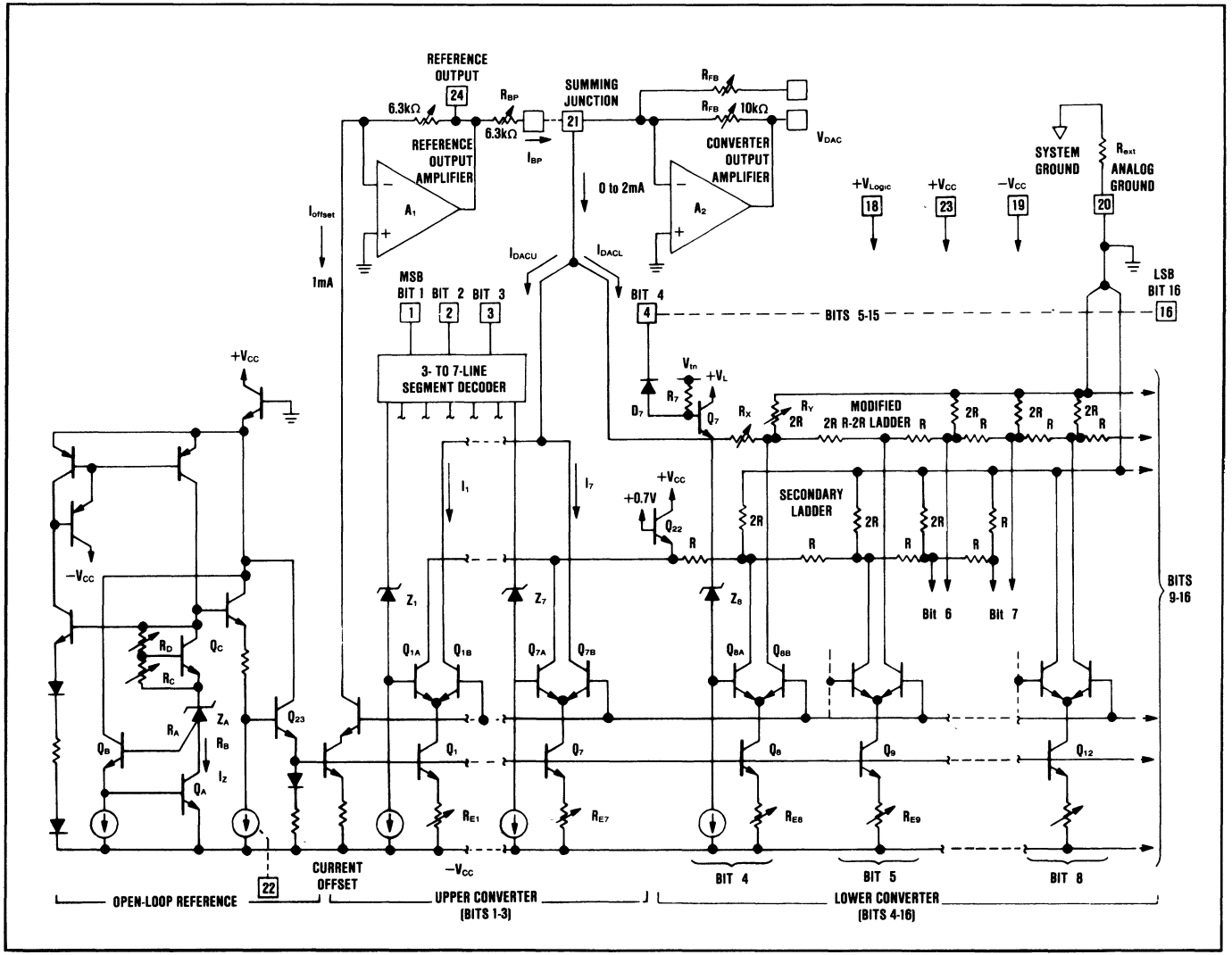


FIGURE 6. Simplified Circuit Diagram of the PCM53 16-bit Digital-to-Analog Converter.

ces are further divided binarily by a pair of R-2R networks, called the modified R-2R ladder and the secondary ladder. By diverting the LSB currents through the modified ladder, the lower converter produces I_{DACL}. This current consists of $2^{13} - 1$ discrete, 30nA steps for each 0.25mA segment of the upper converter. I_{DACU} and I_{DACL} are added at the summing junction, SJ, to form the I_{DAC}, which has a range that varies between 0 and 1.99997mA.

The modified R-2R ladder is superior to a conventional R-2R ladder because its output can be increased or decreased by laser-trimming of its output resistors (R_X and R_Y). Such trimming does not change the binary current division in the ladder. The gain of the lower converter can then be trimmed relative to the gain of the upper converter without interacting or in any way affecting the linearity of the lower converter.

The initial values of the 16 current sources are determined by the voltage at the output of the reference (the emitter of Q_{23}), but the sources are set to the same value when the emitter resistors (R_1–R_{16}) are laser-trimmed. The sources are turned on and off by a differential switch pair (such as Q_{8A}–Q_{8B}) driven by the low-power Schottky TTL-compatible input circuit (typical of D_7, R_7, Q_7, Z_8).

Constant Power

To maintain 16-bit performance, the on-chip power dissipation—and therefore the chip temperature—must be kept constant during code changes. Therefore the current from both the ON side (Q_{1B}) and the OFF side (Q_{1A}) of each differential switch pair in the upper converter should come from $+V_{CC}$, rather than one from $+V_{CC}$ and one from ground. The on-side currents (when the bits are on) come from $+V_{CC}$ and flow through A_2 and the feedback resistor, R_{FB}, to the summing junction to form I_{DACU}. Transistor Q_{22} is used to provide the off-side current with a similar path to $+V_{CC}$. In the lower converter, the secondary R-2R ladder, which is connected between the OFF side of the differential switches and Q_{22}, provides the same function by keeping the $+V_{CC}$ current and the analog ground current constant with code changes.

The secondary ladder also significantly reduces linearity errors that would otherwise be caused by external ground wiring. Indeed, the secondary ladder makes possible the use of a single ground pin, which is the only way to make all the connections in a 24-pin package.

Most converters use a closed-loop op amp for precision DC biasing of their current sources. However, switching transients can cause excessive settling time in the op amp. To ensure minimum settling time, the PCM53 uses an open-loop reference circuit, which incidentally does not require space-consuming capacitors for frequency compensation or suppression of switching transients.

The reference voltage is generated by a Kelvin-sensed buried zener diode. Kelvin sensing is used because the elements of the buried zener, R_A and R_B, have a large and nonlinear temperature coefficient. The Kelvin-sensed connection removes from the reference path the large voltage drop, R_BI_Z, caused by the 1mA zener current I_Z. Instead it substitutes the voltage drop produced across R_A by the base current of Q_B.

Since this base current is only 1μA, the drop is negligible, and the true zener breakdown, V_Z is sensed. In addition great care was taken to ensure that all temperature-sensitive parts of the open-loop reference were laid out along lines of thermal equilibrium, to prevent thermal settling tails.

High-Speed Output Amplifier

In voltage-output models, the output amplifier, A_2, which sums all of the output currents and converts them into the output voltage, V_{DAC}, must be just as accurate as the reference and current sources and just as fast as the switching circuits.

The amplifier is very fast, and it is well behaved when driving a capacitive load. It slews at 10V/μsec and typically settles to 0.003% of final value in less than 4μsec for a 20V step. For a step of 1LSB at the major carry, it settles in 1.5μsec. The thermal tails caused by temperature gradients and resistor self-heating are less than 0.001% of full scale.

Thermal tails occur when thermal gradients across the chip change as signal levels change. For example, when driving a load the output stage of the amplifier and its feedback resistor generate more heat at the full-scale output voltage than at zero. Therefore the temperature-sensitive differential input stage, which is close by on the chip, uses cross-coupled transistors and resistors to equalize thermal gradients.

To achieve a ±10V output swing when operating from ±15V, the output stage of the amplifier uses two transistor pairs connected in series. This scheme is necessary because the breakdown voltage of the npn transistors is limited to 20V by the semiconductor process.

In addition, the output stage is biased in a class AB condition, so that current is always flowing. Continuous current flow is essential to ensure that the open-loop gain, A_O, and closed-loop output impedance, R_O, remain constant for both positive and negative full-scale output swings at 103dB and 0.03Ω, respectively. With lesser performance, errors would occur. If, for example, A_O changed from 94dB to 100dB for an output swing of −10V to +10V respectively, the output error would change by 100μV, and the change would be nonlinear. Likewise a nonlinear error approaching 200μV would occur if R_O changed from 0.04Ω to 0.08Ω.

DISCUSSION OF SPECIFICATIONS

The PCM53 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for a D/A converter in audio applications are Total Harmonic Distortion, Differential Linearity Error, Bipolar Zero Error, parameter shifts with time and temperature and settling time effects on accuracy.

The PCM53 is factory-trimmed and tested for all critical key specifications.

The accuracy of a D/A converter is described by the transfer function shown in Figure 1. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Offset or Bipolar Zero errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the bipolar zero point and Offset drift shifts the line left or right over the operating temperature range. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The converter is designed so that these drifts are in opposite directions. This way the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage.

BIPOLAR ZERO ERROR

Initial Bipolar Zero Error (Bit 1 "ON" and all other bits "OFF") is the deviation from zero volts out and is factory-trimmed to typically ±10mV at +25°C. This error may be trimmed to zero by connecting the external trim potentiometer shown in Figure 8.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from an ideal 1LSB change from one adjacent output state to the next. DLE is important in audio applications because excessive DLE at Bipolar Zero (at the "major carry") can result in audible crossover distortion for low level output signals. Initial DLE on the PCM53 is factory-trimmed to typically ±0.001% of FSR.

STABILITY WITH TIME AND TEMPERATURE

The parameters of a D/A converter designed for audio applications should be stable over a relatively wide temperature range and over long periods of time to avoid undesirable periodic readjustment. The most important parameters are Bipolar Zero Error, Differential Linearity Error, and Total Harmonic Distortion. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The PCM53 is designed so that these drifts are in opposite directions so that the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage. Both DLE and THD are dependent upon the matching and tracking of resistor ratios and upon V_{BE} and h_{FE} of the current-source transistors. The PCM53 was designed so that any absolute shift in these components has virtually no effect on DLE or THD. The resistors are made of identical links of ultra-stable nichrome thin-film. The current density in these resistors is very low to further enhance their stability.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The PCM53 power supply sensitivity is specified for ±0.01% of FSR/%V_{CC} for all supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with the DAC. See also Power Supply Connections paragraph in the Installation and Operating Instructions section.

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 7).

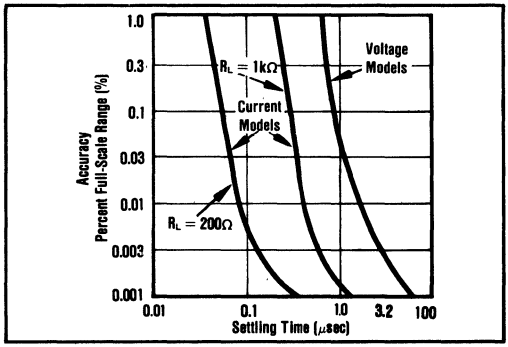


FIGURE 7. Full Scale Range Settling Time vs Accuracy.

Settling times are specified to ±0.006% of FSR; one for a large output voltage change of 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 10000...00), the point at which the worst-case settling time occurs.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the PCM53.

EXTERNAL BIPOLAR ZERO ADJUST (OPTIONAL)

In some applications the Bipolar Zero Error (offset) may require adjustment. This error may be adjusted to zero by installing an external potentiometer as shown in Figure 8. The potentiometer should have adequate resolution, at least 10 turns for full-scale adjustment.

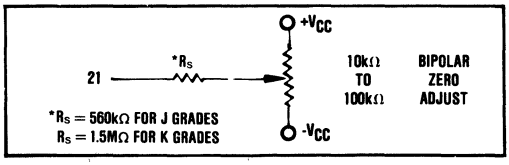


FIGURE 8. Optional External Bipolar Zero Adjust.

The TCR of the potentiometer should be 100ppm/°C or less. The series resistor, R_S (20% carbon or better) should be located close to the PCM53 to prevent noise pickup. Refer to Figure 9 for the relationship of Bipolar Zero adjust on the D/A converter transfer function.

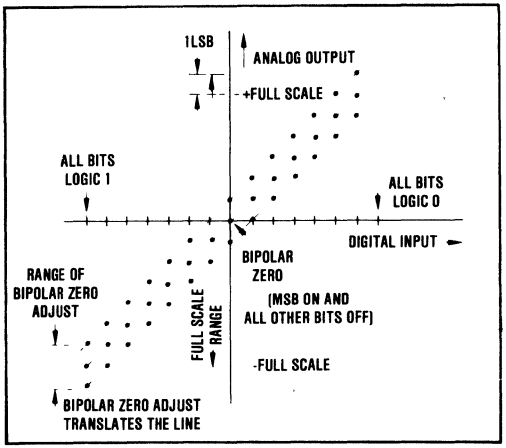


FIGURE 9. Effect of Bipolar Zero Adjustment on a Bipolar D/A Converter Transfer Function.

ADJUSTMENT PROCEDURE

Apply the digital input code that should produce zero volts output (bit 1 or MSB "ON" and all other bits "OFF"). Adjust the bipolar zero potentiometer until zero volts is obtained.

Table II shows the ideal plus and minus full scale voltages and LSB values for both 14- and 16-bits resolution.

TABLE II. Digital Input and Analog Output Relationship.

DIGITAL INPUT CODE	OUTPUT			
	Voltage Model		Current Model	
	16-Bit Resolution	14-Bit Resolution	16-Bit Resolution	14-Bit Resolution
Complementary Bipolar Offset Binary (COB) ±10V (PCM53)				
One LSB	+305μV	+1 22mV	0 031μA	0 122μA
All Bits On 00 00	+9 99969V	+9 99878V	−0 99997mA	−0 99988mA
All Bits Off 11 11	−10 00000V	−10 00000V	−1 00000mA	+1 00000mA

INSTALLATION CONSIDERATIONS

If 14-bit resolution is desired, bit 15 (pin 15) and bit 16 (pin 16) should be connected to V_{DD} through a 1kΩ resistor to insure that these bits remain off.

Figure 10 shows the connection diagram for a PCM53-V. Figures 11 and 12 show connection diagrams for PCM53-I models.

Lead and contact resistances are represented by R_1 through R_3. As long as the load resistance (R_L) is constant, R_1 simply introduces a gain error. R_2 is part of R_1 if the output voltage is sensed at Common (pin 20) and therefore introduces no error. If R_L is variable, then R_1 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. R_L should be located as close as possible to the PCM53 for optimum performance.

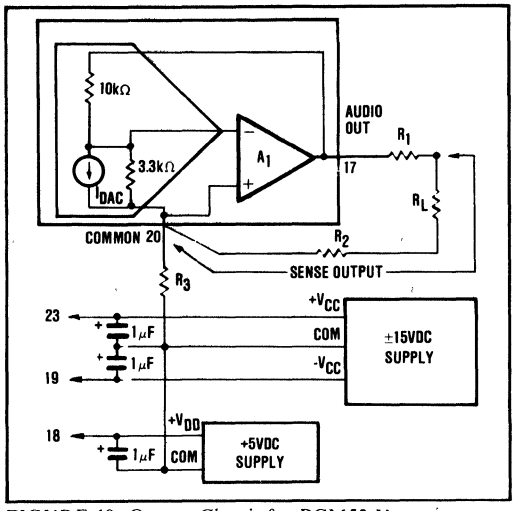


FIGURE 10. Output Circuit for PCM53-V.

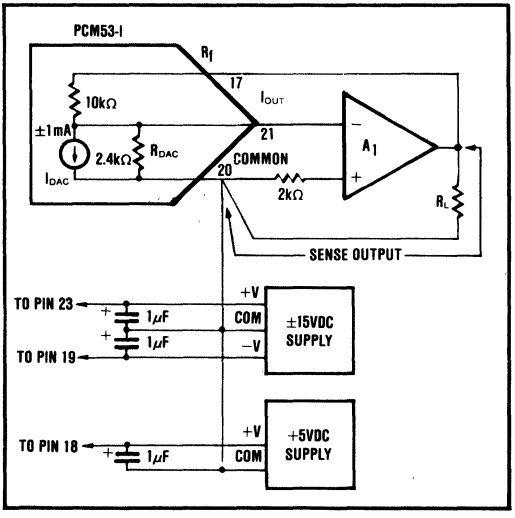


FIGURE 11. Preferred External Op Amp Configuration Using PCM53-I.

The PCM53 and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

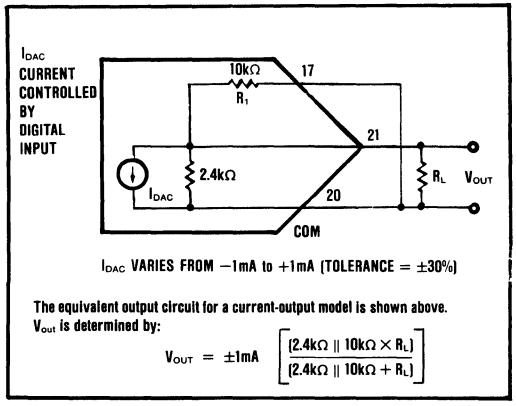


FIGURE 12. Driving a Resistive Load With PCM53-I.

Figures 11 and 12 show connection diagrams for PCM53-I models.

APPLICATIONS

Figures 13 and 14 show a circuit diagram and timing diagram of a single PCM53-V used to obtain both left and right channel audio output in a typical digital audio system. The Sony CX-7934 and associated LSI logic contain all of the required circuitry for error detection, correction, and formatting of the digital data obtained from the Compact Disc prior to sending this information to the D/A converter. The CX-7934 is used in a parallel output mode where the left and right channel parallel data are time-shared. Since the digital inputs of the PCM53 are TTL-compatible, they can be connected directly to the parallel outputs of the CX-7934. Only a single inverter is required (Bit 1) to convert the two's complement output code of the CX-7934 to offset binary. The audio output of the PCM53-V is alternately time-shared between the left and right channels. The design is greatly simplified because the PCM53-V is a complete D/A converter.

A sample/hold amplifier, or "deglitcher", is required at the output of the D/A converter for both the left and right channel, as shown in Figure 15. The S/H amplifier for the left channel is composed of A_2, SW_1, and associated circuitry. A_2 is used as an integrator to hold the analog voltage in C_1. Since the source and drain of the FET switch operates at a virtual ground when "C" and "B" are closed in the sample mode, there is no increase in distortion caused by the modulation effect of R_{on} by the audio signal.

Figure 16 shows the deglitcher control signals for both the left and right channels which are produced by the timing control logic. A delay of 2.5μsec (tω) is provided to eliminate the glitch and allow the output of the PCM53-V to settle within a small error band around its

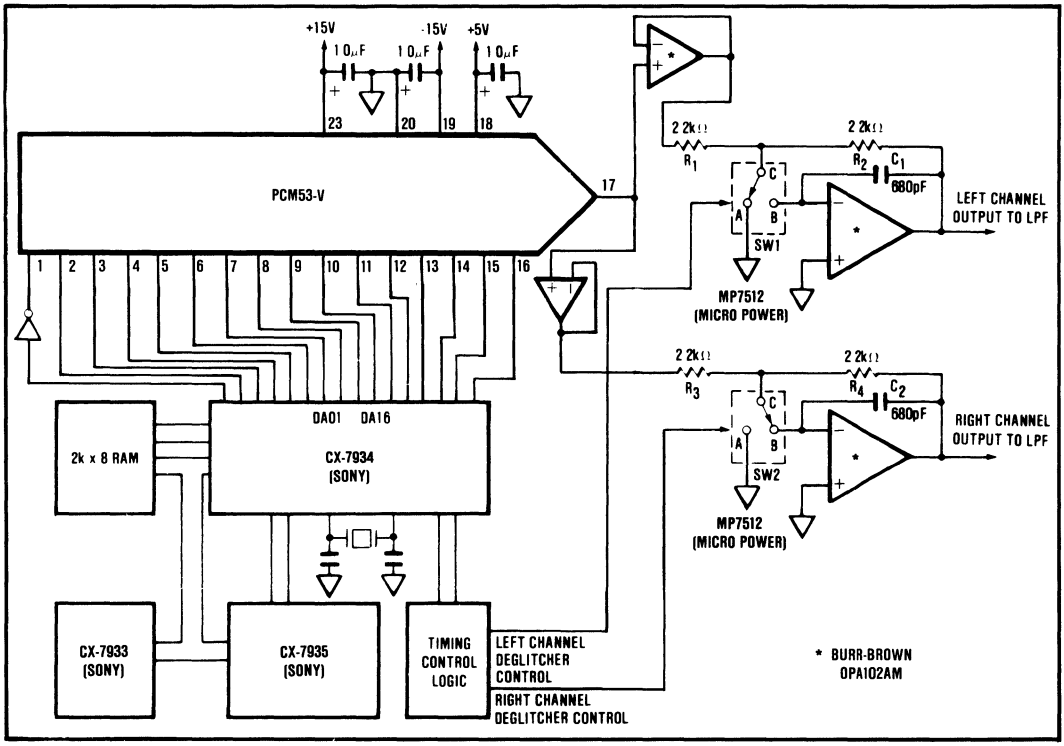


FIGURE 13. A Single PCM52/53 Used to Obtain Both Left and Right Channel Output in a Typical Digital Audio System.

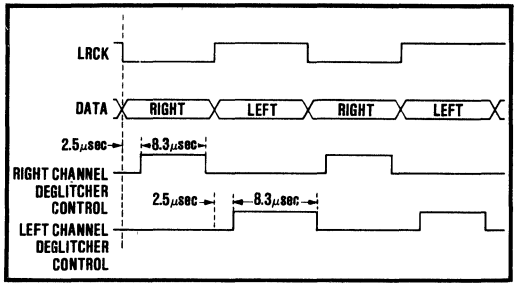


FIGURE 14. Timing Diagram for the Digital Audio System Using PCM53 and Sony LSI Logic.

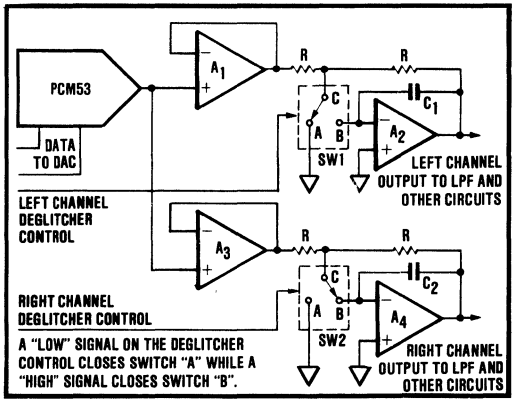


FIGURE 15. A Sample/Hold Amplifier (Deglitcher) is Required at the Digital-to-Analog Output for Both Left and Right Channels.

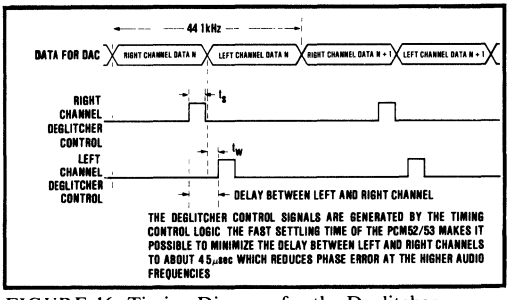


FIGURE 16. Timing Diagram for the Deglitcher Control Signals.

final value before connecting it to the channel output.

Due to the fast settling time of the PCM53-V, it is possible to minimize the delay between the left channel and right channel outputs when using a single D/A converter for both channels. This is important because the left and right channel data is recorded in phase and use of a slower D/A converter would result in significant phase error at the higher audio frequencies.

A low-pass filter is required at the S/H output to remove all unwanted frequency components caused by the sampling frequency as well as the discrete nature of the D A converter output. The filter must have a flat amplitude response over the entire audio band (0 to 20kHz) and a very-high attenuation above 20kHz. Most previous digital audio circuits used a high-order (9–13 pole) analog filter. However, the phase response of an analog filter with these amplitude characteristics is nonlinear and can disturb the pulse-shaped characteristics of the transients contained in music.

SECOND-GENERATION SYSTEMS

One method of avoiding this problem and obtaining a linear phase response is to use an oversampling digital filter technique as shown in Figure 17. The Yamaha YM-3511 and YM-2201 LSI chips provide all of the functions described for the Sony chip set and, in addition, contain an onboard digital oversampling filter which effectively multiplies the sampling frequency by a factor of two and sends the parallel data at a rate of 88.2kHz to the D/A converter. Since the offset binary parallel data is directly available from the YM-2201, no external inverter is required. Furthermore, since the deglitcher control signal is also available from the YM-2201, no external timing control logic is required for most applications. The timing diagram for this circuit is shown in Figure 18.

This circuit requires a very fast D/A converter since the sampling frequency is multiplied by a factor of two or more. This technique results in intermodulation products being created, by mixing the sampling frequency and components of the audio frequency, that are far outside the audio band of 0 to 20kHz. These unwanted frequencies are easily removed by a low-order linear-phase analog filter following the deglitcher circuit, since a sharp amplitude response is not required. A single PCM53-V can be used for both the left and right channel as long as the oversampling rate of the digital filter is two. An oversampling rate of four can be used if a separate PCM53 is used for each channel. This would reduce the complexities of the analog filter required even further (at the expense of an additional D/A converter).

Another factor to consider when choosing a D/A converter for digital audio applications is that the linearity of the total harmonic distortion versus output signal should be good since a change in the background noise level can be audible. The design of the PCM53 ensures that the linearity of the total harmonic distortion versus output signal level is very good over the full range of amplitude and frequencies. Also, no special grounding or shielding techniques are required to obtain good signal-to-noise ratio with the PCM53. Some converters require a high frequency clock which can couple to the analog output of the D/A converter through the output wiring and ground circuitry.

The PCM53 D/A converters provide a complete solution to one of the most critical portions of a digital audio system. Since the sound of the system can be affected by the D/A converter more than any other single component, the selection of which converter to use should be made with care.

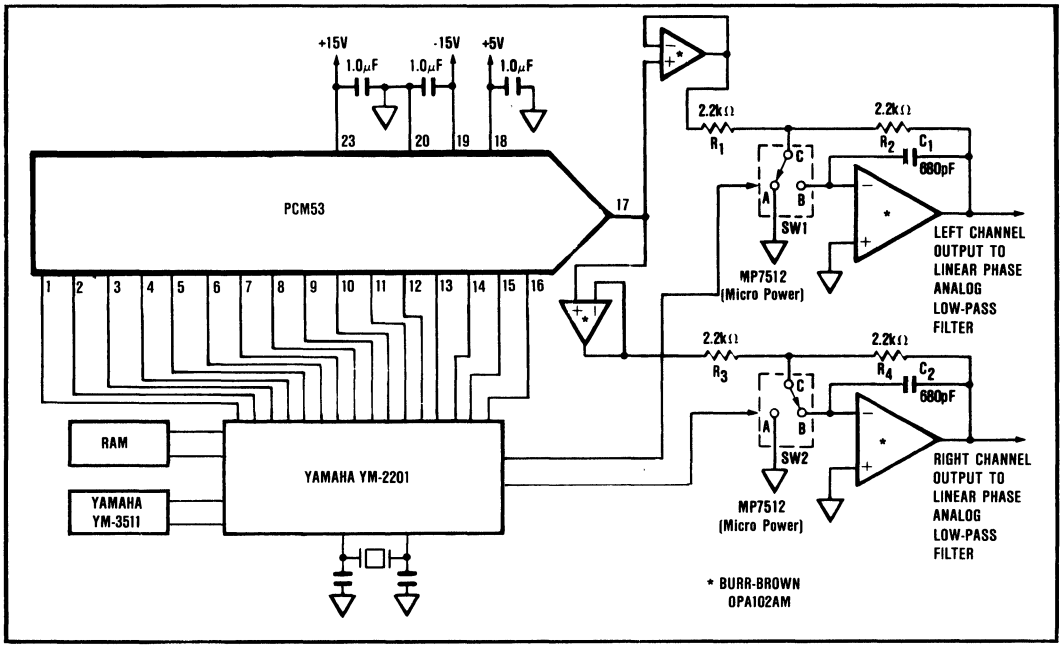


FIGURE 17. Oversampling Digital-Filter Technique Using Yamaha LSI.

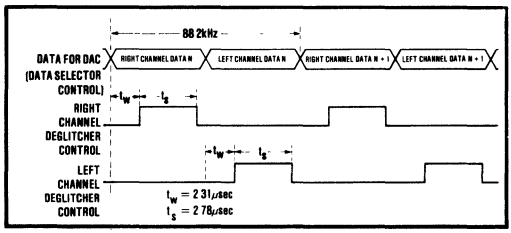


FIGURE 18. Timing Diagram for Digital Oversampling Technique when using Yamaha LSI.

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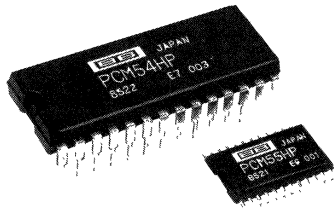


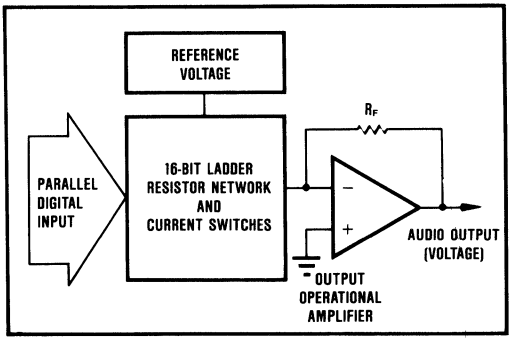
PCM54
PCM55

DESIGNED FOR AUDIO

16-Bit Monolithic DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- LOW COST
- NO EXTERNAL COMPONENTS REQUIRED
- 16-BIT RESOLUTION
- 15-BIT MONOTONICITY, TYP
- 0.001% of FSR TYP DIFFERENTIAL LINEARITY ERROR
- 0.0025% MAX THD (FS Input, KP Grade, 16 Bits)
- 0.02% MAX THD (−20dB Input, KP Grade, 16 Bits)
- 3μs SETTLING TIME, TYP (Voltage Out)
- 96dB DYNAMIC RANGE
- ±3V or ±1mA AUDIO OUTPUT
- EIAJ STC-007-COMPATIBLE
- OPERATES ON ±5V (PCM55) to ±12V (PCM54) SUPPLIES
- PINOUT ALLOWS I_{OUT} OPTION
- PLASTIC DIP PACKAGE (PCM54)
- PLASTIC MINI-FLATPAK (PCM55)



DESCRIPTION

The PCM54 and PCM55 family of converters are state-of-the-art, fully monotonic, digital-to-analog converters that are designed and specified for digital audio applications. These devices employ ultra-stable nichrome (NiCr) thin-film resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature.

These converters are completely self-contained with a stable, low noise, internal, zener voltage reference; high speed current switches; a resistor ladder network; and a fast settling, low noise, output operational amplifier all on a single monolithic chip. The converters are operated using two power supplies that can range from ±5V (PCM55) to ±12V (PCM54). Power dissipation with ±5V supplies is typically less than 200mW. Also included is a provision for external adjustment of the MSB error (differential linearity error at bipolar zero, PCM54 only) to further improve THD specifications if desired. Few external components are necessary for operation, and all critical specifications are 100% tested. This helps assure the user of high system reliability and outstanding overall system performance.

A current output (I_{OUT}) wiring option is provided. This output typically settles to within ±0.006% of FSR final value in 350ns (in response to a full-scale change in the digital input code).

These converters are packaged in high-quality molded plastic packages and have passed operating life tests under simultaneous high-pressure, high-temperature, and high-humidity conditions.

The PCM54 is packaged in 28-pin plastic DIP package. The PCM55 is available in a 24-pin plastic mini-flatpak.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel (602) 746-1111 - Twx 910-952-1111 - Cable BBRCORP - Telex 66-6491

SPECIFICATIONS

ELECTRICAL

At +25°C, ±V_{CC} = 12V, unless otherwise noted

MODEL	PCM54HP			PCM54JP			PCM54KP			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUT										
Resolution		16			*			*		Bits
Dynamic Range		96			*			*		dB
Logic Levels (TTL/CMOS Compatible):										
V_{IH}	+2.4		+5.25	*		*	*		*	V
V_{IL}	0		+0.8	*		*	*		*	V
I_{IH}, V_{IN} = +2.7V			+40			*			*	µA
I_{IL}, V_{IN} = + 0.4V			−0.5			*			*	mA
TRANSFER CHARACTERISTICS										
ACCURACY										
Gain Error		±2			*			*		%
Bipolar Zero Error		±30			*			*		mV
Differential Linearity Error at Bipolar Zero[1]		±0.001			*			*		% FSR[2]
Noise (rms) (20Hz to 20kHz) at Bipolar Zero		12			*			*		µV
TOTAL HARMONIC DISTORTION[3]										
(16-bit resolution)										
V_O = ±FS at f = 991Hz		0 002	0.008		*	0.004		*	0 0025	%
V_O = −20dB at f = 991Hz		0 02	0.04		*	*		0.1	0 02	%
V_O = −60dB at f = 991Hz		2.0	4.0		*	*		1.0	2 0	%
MONOTONICITY		15			*			*		Bits
SETTLING TIME (to ±0.006% of FSR)										
Voltage Output: 6V Step		3			*			*		µs
1LSB Step		1			*			*		µs
Current Output (1mA Step): 10Ω to 100Ω Load		350			*			*		ns
1kΩ Load[4]		350			*			*		ns
Deglitcher Delay (THD Test)[5]		2 5	4.0		*	*		*	*	µs
Slew Rate		10			*			*		V/µs
WARM-UP TIME	1			*			*			Min
ANALOG OUTPUT										
Voltage Output: Bipolar Range		±3.0			*			*		V
Output Current	±2.0			*			*			mA
Output Impedance		0.1			*			*		Ω
Short-Circuit Duration	Indefinite to Common				*			*		
Current Output:[6]										
Bipolar Range (±30%)		±1			*			*		mA
Bipolar Output Impedance (±30%)		1 2			*			*		kΩ
POWER SUPPLY REQUIREMENTS										
Voltage: +V_{CC}	+4 75	+12	+15.75	*	*	*	*	*	*	V
−V_{CC}	−4.75	−12	−15.75	*	*	*	*	*	*	V
Supply Drain: +V_{CC}		+13	+20		*	*		*	*	mA
−V_{CC}		−16	−25		*	*		*	*	mA
TEMPERATURE RANGE										
Operating	0		+70	*		*	*		*	°C
Storage	−55		+100	*		*	*		*	°C

*Specification same as PCM54HP

NOTES. (1) Externally adjustable. If external adjustment is not used, connect a 0.01µF capacitor to Common to reduce noise pickup. (2) FSR means Full-Scale Range and is 6V for ±3V output (3) The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit Burr-Brown may calculate THD from the measured linearity errors using equation 2 in the section on "Total Harmonic Distortion" but specifies that the maximum THD measured with the circuit shown in Figure 2 will be less than the limits indicated. (4) Measured with an active clamp to provide a low impedance for approximately 200ns. (5) Deglitcher or sample/hold delay used in THD measurement test circuit. See Figures 2 and 3. (6) Output amplifier disconnected

SPECIFICATIONS

ELECTRICAL

At +25°C, $\pm V_{CC}$ = 5V, unless otherwise noted.

MODEL	PCM55HP			PCM55JP			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DIGITAL INPUT							
Resolution		16			*		Bits
Dynamic Range		96			*		dB
Logic Levels (TTL/CMOS Compatible) V_{IH}	+2 4		+5.25	*		*	V
V_{IL}	0		+0.8	*		*	V
I_{IH}, V_{IN} = +2 7V			+40			*	μA
I_{IL}, V_{IN} = + 0 4V			−0.5			*	mA
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error		±2 0			*		%
Bipolar Zero Error		±30			*		mV
Differential Linearity Error at Bipolar Zero[1]		±0 001			*		% FSR[2]
Noise (rms) (20Hz to 20kHz) at Bipolar Zero		12			*		μV
TOTAL HARMONIC DISTORTION[3](16-bit resolution)							
V_O = ±FS at f = 991Hz		0 002	0.008		*	0 004	%
V_O = −20dB at f = 991Hz		0.02	0.04		*	*	%
V_O = −60dB at f = 991Hz		1 9	4 0		*	*	%
MONOTONICITY		15			*		Bits
DRIFT							
Total Bipolar Drift		±25			*		ppm of FSR/°C
Drift Over Operating Temperature Range		±0.1			*		%
Bipolar Zero Drift		±4			*		ppm of FSR/°C
SETTLING TIME (to ±0.006% of FSR)							
Voltage Output. 6V Step		3			*		μs
1LSB Step		1			*		μs
Current Output (1mA Step) 10Ω to 100Ω Load		350			*		ns
1kΩ Load[4]		350			*		ns
Deglitcher Delay (THD Test)[5]		2 5	4.0		*	*	μs
Slew Rate		10			*		V/μs
WARM-UP TIME	1			*			Min
ANALOG OUTPUT							
Voltage Output Bipolar Range		±3 0			*		V
Output Current	±2 0			*			mA
Output Impedance		0.1			*		Ω
Short-Circuit Duration		Indefinite to Common			*		
Current Output[6] Bipolar Range (±30%)		±1			*		mA
Bipolar Output Impedance (±30%)		1.2			*		kΩ
POWER SUPPLY REQUIREMENTS							
Voltage +V_{CC}	+4 75	+5	+7 5	*	*	*	V
−V_{CC}	−4 75	−5	−7 5	*	*	*	V
Supply Drain +V_{CC}		+13	+20		*	*	mA
−V_{CC}		−16	−25		*	*	mA
TEMPERATURE RANGE							
Operating	0		+70	*		*	°C
Storage	−55		+100	*		*	°C

*Specification same as PCM55HP

NOTES: (1) FSR means Full-Scale Range and is 6V for ±3V output. (2) Externally adjustable. If external adjustment is not used, connect a 0.01μF capacitor to Common to reduce noise pickup (3) The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit. Burr-Brown may calculate THD from the measured linearity errors using equation 2 in the section on "Total Harmonic Distortion" but specifies that the maximum THD measured with the circuit shown in Figure 2 will be less than the limits indicated. (4) Measured with an active clamp to provide a low impedance for approximately 200ns (5) Deglitcher or sample/hold delay used in THD measurement test circuit. See Figures 2 and 3 (6) Output amplifier disconnected I_{OUT} application. Close the feedback around the amplifier by connecting output of amplifier to the minus input

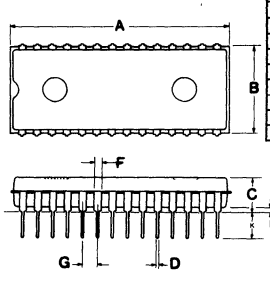
PIN ASSIGNMENTS

Pin	PCM54-DIP	Pin	PCM54-DIP
1	Trim	15	Bit 13
2	Bit 1 (MSB)	16	Bit 14
3	Bit 2	17	Bit 15
4	NC	18	Bit 16 (LSB)
5	Bit 3	19	V_{OUT}
6	Bit 4	20	R_{FB}
7	Bit 5	21	SJ
8	Bit 6	22	Common
9	Bit 7	23	I_{OUT}
10	Bit 8	24	NC
11	Bit 9	25	I_{BPO}
12	Bit 10	26	$+V_{CC}$
13	Bit 11	27	MSB Adjust
14	Bit 12	28	$-V_{CC}$

Pin	PCM55-Flatpak	Pin	PCM55-Flatpak
1	Bit 1 (MSB)	13	Bit 13
2	Bit 2	14	Bit 14
3	Bit 3	15	Bit 15
4	Bit 4	16	Bit 16
5	Bit 5	17	Voltage Output
6	Bit 6	18	Feedback Resistor
7	Bit 7	19	Summing Junction
8	Bit 8	20	Common
9	Bit 9	21	Current Output
10	Bit 10	22	Bipolar Offset
11	Bit 11	23	$+V_{CC}$
12	Bit 12	24	$-V_{CC}$

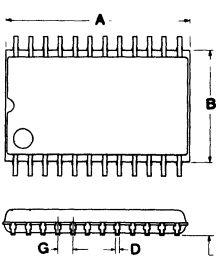
MECHANICAL OUTLINES

PCM54



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	----	1.441	----	36.60
B	----	.575	----	14.60
C	----	.224	----	5.70
D	.018	.019	0.47	0.49
F	.047	.055	1.20	1.40
G	.090	.110	2.29	2.79
J	.008	.015	0.20	0.38
K	.100	----	2.54	----
L	----	.600	----	15.24
M	0°	15°	0°	15°
N	.020	----	0.51	----

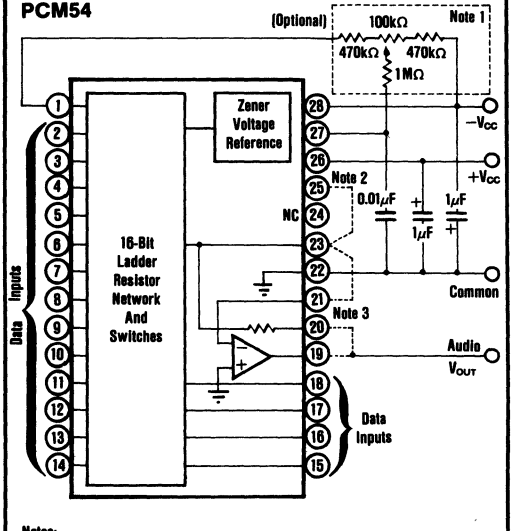
PCM55



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.614	.630	15.60	16.00
B	.346	.362	8.80	9.20
C	——	.098	——	2.50
D	.012	.020	0.30	0.50
G	.046	.054	1.17	1.37

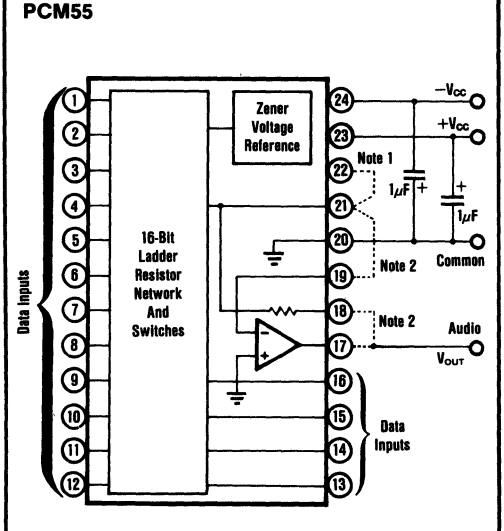
CONNECTION DIAGRAMS

PCM54



Notes:
(1) MSB error (BPZ differential linearity error) can be adjusted to zero using this external circuit.
(2) Connect for bipolar operation ($+V_{CC} \geq 8.5V$ for unipolar operation).
(3) Connect for V_{OUT} operation. When V_{OUT} amp is not being used (I_{OUT} mode), terminate with an external 3kΩ feedback resistor between pin 19 and pin 21 and a 1kΩ resistor between pin 21 and pin 22 to reduce possible noise effects.

PCM55



Notes:
(1) Connect for bipolar operation ($+V_{CC} \geq 8.5V$ for unipolar operation).
(2) Connect for V_{OUT} operation. When V_{OUT} amp is not being used (I_{OUT} mode), terminate with an external 3kΩ feedback resistor between pin 17 and pin 19 and a 1kΩ resistor between pin 19 and pin 20 to reduce possible noise effects.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages	±18VDC
Input Logic Voltage	−1V to +5 5V
Power Dissipation	PCM54 800mW, PCM55 400mW
Storage Temperature	−55°C to +100°C
Lead Temperature During Soldering	10s at +300°C

ORDERING INFORMATION

Model	THD at FS	Package
PCM54HP	0 008	28-pin DIP
JP	0 004	28-pin DIP
KP	0 0025	28-pin DIP
PCM55HP	0 008	24-lead mini flat pak
JP	0 004	24-lead mini flat pak

DISCUSSION OF SPECIFICATIONS

The PCM54 and PCM55 are specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for a D/A converter in audio applications are Total Harmonic Distortion, Differential Linearity Error, Bipolar Zero Error, parameter shifts with time and temperature, and settling time effects on accuracy.

The PCM54 and PCM55 are factory-trimmed and tested for all critical key specifications.

The accuracy of a D/A converter is described by the transfer function shown in Figure 1. Digital input to analog output relationship is shown in Table I. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Gain drift over temperature rotates the line (Figure 1) about the bipolar zero point and Offset drift shifts the line left or right over the operating temperature range. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The converter is designed so that these drifts are in opposite directions. This way the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage.

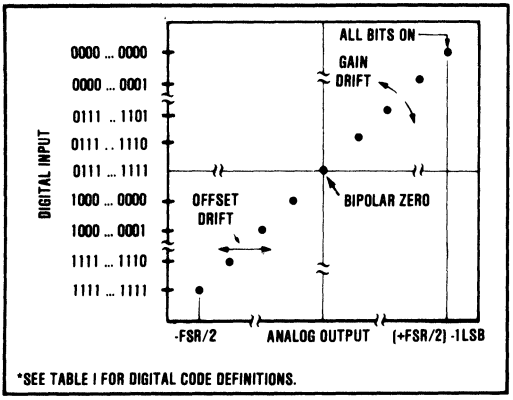


FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

DIGITAL INPUT CODES

The PCM54 and PCM55 accept complementary digital input codes in any of three binary formats (CSB, unipolar; or COB, bipolar; or CTC, Complementary Two's Complement, bipolar). See Table II.

TABLE II. Digital Input Codes.

Digital Input Codes	Analog Output		
	Complementary Straight Binary (CSB)	Complementary Offset Binary (COB)	Complementary Two's Complement (CTC)*
0000_H	+ Full Scale	+ Full Scale	−1LSB
$7FFF_H$	+1/2Full Scale	Bipolar Zero	− Full Scale
8000_H	+1/2 Full Scale −1LSB	−1LSB	+ Full Scale
$FFFF_H$	Zero	− Full Scale	Bipolar Zero

Invert the MSB of the COB code with an external inverter to obtain CTC code

TABLE I. Digital Input to Analog Output Relationship.

VOLTAGE OUTPUT MODE						
	Analog Output					
	Unipolar*			Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μV)	91.6	183	366	91 6	183	366
0000_H (V)	+5 99991	+5 99982	+5.99963	+2 99991	+2 99982	+2 99963
$FFFF_H$ (V)	0	0	0	−3 0000	−3 0000	−3 0000
CURRENT OUTPUT MODE						
	Analog Output					
	Unipolar			Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μA)	0.031	0.061	0.122	0.031	0.061	0.122
0000_H (mA)	−1.99997	−1 99994	−1.99988	−0.99997	−0.99994	−0.99988
$FFFF_H$ (mA)	0	0	0	+1.00000	+1.00000	+1.00000

*NOTE: $+V_{CC}$ must be at least +8.5VDC to allow output to swing to +6.0VDC.

BIPOLAR ZERO ERROR

Initial Bipolar Zero Error (Bit 1 "ON" and all other bits "OFF") is the deviation from 0V out and is factory-trimmed to typically ±10mV at +25°C.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from an ideal 1LSB change from one adjacent output state to the next. DLE is important in audio applications because excessive DLE at Bipolar Zero (at the "major carry") can result in audible crossover distortion for low level output signals. Initial DLE on the PCM54 and PCM55 is factory trimmed to typically ±0.001% of FSR. This error is adjustable to zero using the circuit shown in the connection diagram (PCM54 only).

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy.

The PCM54 and PCM55 power supply sensitivity is shown by Figure 2. Normally, regulated power supplies with 1% or less ripple are recommended for use with the DAC. See also Power Supply Connections paragraph in the Installation and Operating Instructions section.

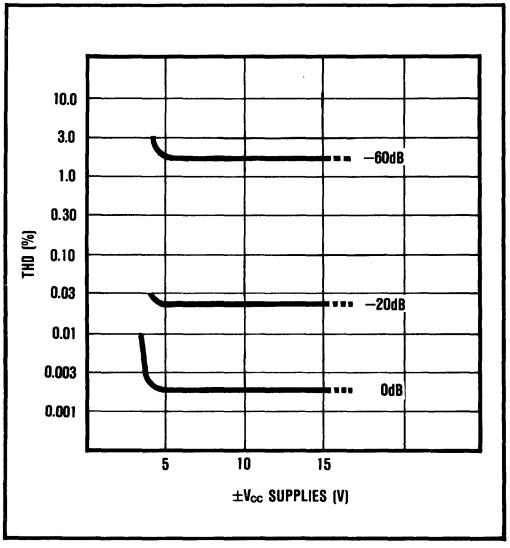


FIGURE 2. Effects of ±V_{CC} on Total Harmonic Distortion (PCM54JP; V_{CC}s with approximately 2% ripple).

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 3).

Settling times are specified to ±0.006% of FSR; one for a large output voltage change of 3V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111 . . . 11 to 10000.00), the point at which the worst-case settling time occurs.

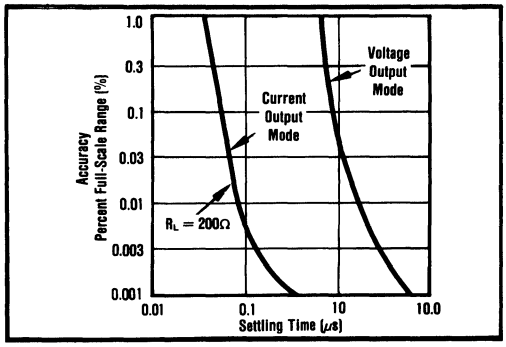


FIGURE 3. Full Scale Range Settling Time vs Accuracy.

STABILITY WITH TIME AND TEMPERAURE

The parameters of a D/A converter designed for audio applications should be stable over a relatively wide temperature range and over long periods of time to avoid undesirable periodic readjustment. The most important parameters are Bipolar Zero Error, Differential Linearity Error, and Total Harmonic Distortion. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The PCM54 and PCM55 are designed so that these drifts are in opposite directions so that the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage. Both DLE and THD are dependent upon the matching and tracking of resistor ratios and upon V_{BE} and h_{FE} of the current-source transistors. The PCM54 and PCM55 were designed so that any absolute shift in these components has virtually no effect on DLE or THD. The resistors are made of identical links of ultra-stable nichrome thin-film. The current density in these resistors is very low to further enhance their stability.

DYNAMIC RANGE

The Dynamic Range is a measure of the ratio of the smallest signals the converter can produce to the full-scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 × n, or about 96dB for a 16-bit converter. The actual, or useful, dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit. However, this does point out that a resolution of at least 16 bits is required to obtain a 90dB minimum dynamic range, regardless of the accuracy of the converter. Another specification that is useful for audio applications is Total Harmonic Distortion (THD).

TOTAL HARMONIC DISTORTION

THD is useful in audio applications and is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quan-

tization Error. To be useful, THD should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications.

The THD is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency and is expressed in percent or dB. The rms value of the PCM54/55 error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2} \quad (1)$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the PCM54 or PCM55 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \frac{\epsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\% \quad (2)$$

where E_{rms} is the rms signal-voltage level.

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

For the PCM54/55 the test period was chosen to be 22.7μs (44.1kHz) which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 420Hz and the amplitude of the input signal is 0dB, −20dB, and −60dB down from full scale.

Figure 4 shows the typical THD as a function of output voltage.

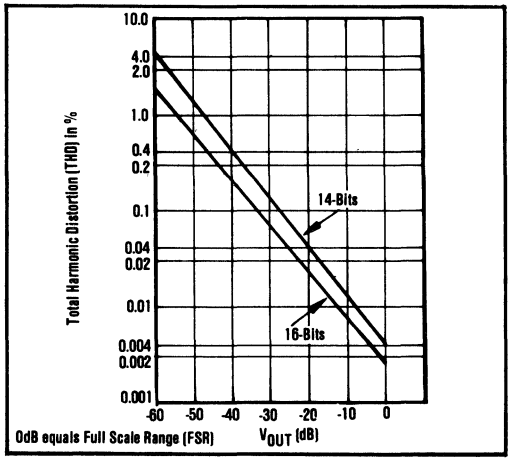


FIGURE 4. Total Harmonic Distortion (THD) vs V_{OUT}.

Figure 5 shows typical THD as a function of frequency.

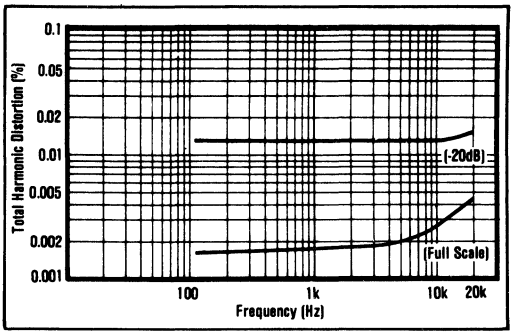


FIGURE 5. Total Harmonic Distortion (THD) vs Frequency.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the converter.

MSB ERROR ADJUSTMENT PROCEDURE (OPTIONAL)

The MSB error of the PCM54 and PCM55 can be adjusted to make the differential linearity error (DLE) at BPZ essentially zero. This is important when the signal output levels are very low because zero crossing noise (DLE at BPZ) becomes very significant when compared to the small code changes occurring in the LSB portion of the converter.

Differential linearity error at bipolar zero is guaranteed to meet data sheet specifications without any external adjustment. However, a provision has been made for an optional adjustment of the MSB linearity point which makes it possible to eliminate DLE error at BPZ (PCM54 only). Two procedures are given to allow either static or dynamic adjustment. The dynamic procedure is preferred because of the difficulty associated with the static method (accurately measuring 16-bit LSB steps).

To statically adjust DLE at BPZ, refer to the circuit shown in Figure 6 or the PCM54 connection diagram. After allowing ample warm-up time (20–30 minutes) to assure stable operation of the PCM54, select input code 8000 hexadecimal (all bits on except the MSB). Measure the audio output voltage using a 6-1/2 digit voltmeter and record it. Change the digital input code to 7FFF hexadecimal (all bits off except the MSB). Adjust the 100kΩ potentiometer to make the audio output read 92μV more than the voltage reading of the previous code (a 1LSB step = 92μV).

A much simpler method is to dynamically adjust the DLE at BPZ. Again, refer to Figure 6 or the PCM54 connection diagram for circuitry and component values. Assuming the device has been installed in a digital audio application circuit, send the appropriate digital input to produce a −60dB level sinusoidal output. While measuring the THD of the audio circuit output, adjust the 100kΩ potentiometer until a minimum level of distortion is observed.

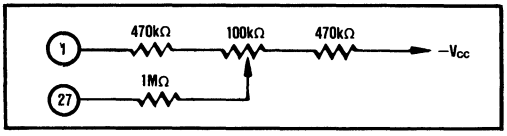


FIGURE 6. MSB Differential Linearity at Bipolar Zero Adjustment Circuit (optional).

INSTALLATION CONSIDERATIONS

If the optional external MSB error circuitry is used (PCM54), a potentiometer with adequate resolution and a TCR of 100ppm/°C or less is required. Also, extra care must be taken to insure that no leakage path (either AC or DC) exists to pin 27 (PCM54). If the circuit is not used, pin 1 (PCM54) should be terminated to common with a 0.01μF capacitor.

The PCM converter and the wiring to its connectors should be located to provide the optimum isolation from sources of RFI and EMI. The important consideration in the elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they represent a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

APPLICATIONS

A sample/hold amplifier, or "deglitcher", is required at the output of the D/A converter for both the left and right channel, as shown in Figure 7. The S/H amplifier for the left channel is composed of A_2, SW_1, and associated circuitry. A_2 is used as an integrator to hold the analog voltage in C_1. Since the source and drain of the FET switch operates at a virtual ground when "C" and "B" are closed in the sample mode, there is no increase in distortion caused by the modulation effect of R_{ON} by the audio signal.

Figure 8 shows the deglitcher control signals for both the left and right channels which are produced by the timing control logic. A delay of 2.5μs (tω) is provided to eliminate the glitch and allow the output of the PCM54-V to settle within a small error band around its final value before connecting it to the channel output.

Due to the fast settling time of the PCM54-V, it is possible to minimize the delay between the left channel and right channel outputs when using a single D/A converter for both channels. This is important because the left and right channel data is recorded in phase and use of a slower D/A converter would result in signficant phase error at the higher audio frequencies.

A low-pass filter is required at the S/H output to remove all unwanted frequency components caused by the sampling frequency as well as the discrete nature of the D/A converter output. The filter must have a flat amplitude response over the entire audio band (0 to 20kHz) and a very-high attenuation above 20kHz. Most previous digital audio circuits used a high-order (9–13 pole) analog filter. However, the phase response of an analog filter with these amplitude characteristics is nonlinear and can disturb the pulse-shaped characteristics of the transients contained in music.

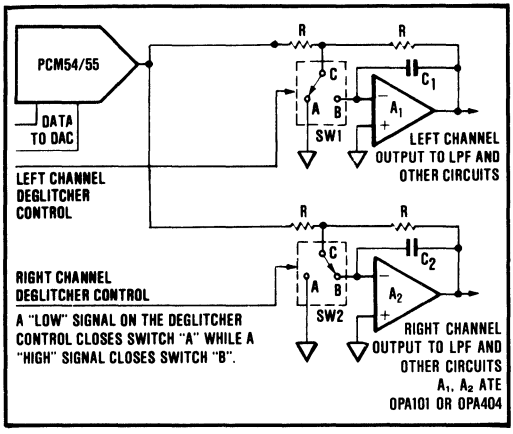


FIGURE 7. A Sample/Hold Amplifier (Deglitcher is Required at the Digital-to-Analog Output for Both Left and Right Channels.

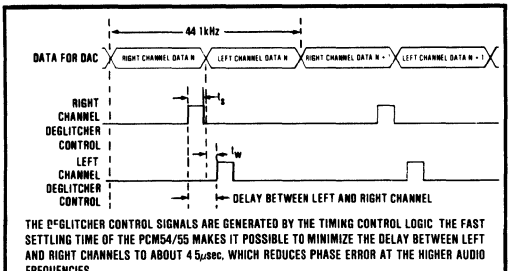


FIGURE 8. Timing Diagram for the Deglitcher Control Signals.

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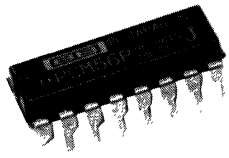


PCM56P

DESIGNED FOR AUDIO

Serial Input 16-Bit Monolithic DIGITAL-TO-ANALOG CONVERTER

FEATURES

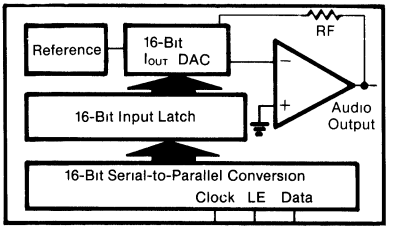
- SERIAL INPUT
- LOW COST
- NO EXTERNAL COMPONENTS REQUIRED
- 16-BIT RESOLUTION
- 15-BIT MONOTONICITY, TYP
- 0.001% OF FSR TYP DIFFERENTIAL LINEARITY ERROR
- 0.0025% MAX THD (FS Input, K Grade, 16 Bits)
- 0.02% MAX THD (−20dB Input, K Grade, 16 Bits)
- 1.5μs SETTLING TIME, TYP (Voltage Out)
- 96dB DYNAMIC RANGE
- ±3V or ±1mA AUDIO OUTPUT
- EIAJ STC-007-COMPATIBLE
- OPERATES ON ±5V to ±12V SUPPLIES
- PINOUT ALLOWS I_{OUT} OPTION
- PLASTIC DIP PACKAGE

DESCRIPTION

The PCM56P is a state-of-the-art, fully monotonic, digital-to-analog converter that is designed and specified for digital audio applications. This device employs ultra-stable nichrome (NiCr) thin-film resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature.

This converter is completely self-contained with a stable, low noise, internal zener voltage reference; high speed current switches; a resistor ladder network; and a fast settling, low noise output operational amplifier all on a single monolithic chip. The converters are operated using two power supplies that can range from ±5V to ±12V. Power dissipation with ±5V supplies is typically less than 200mW. Also included is a provision for external adjustment of the MSB error (differential linearity error at bipolar zero) to further improve total harmonic distortion (THD) specifications if desired. Few external components are necessary for operation, and all critical specifications are 100% tested. This helps assure the user of high system reliability and outstanding overall system performance.

The PCM56P is packaged in a high-quality 16-pin molded plastic DIP package and has passed operating life tests under simultaneous high-pressure, high-temperature, and high-humidity conditions.



International Airport Industrial Park - P.O Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx. 910-952-1111 - Cable: BBRCORP - Telex 66-6491

SPECIFICATIONS

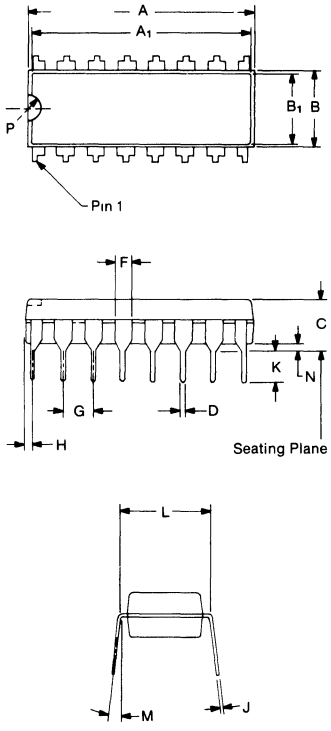
ELECTRICAL

Typical at +25°C and nominal power supply voltages of ±5V unless otherwise noted

MODEL	PCM56P/-J/-K			
	MIN	TYP	MAX	UNITS
INPUT				
DIGITAL INPUT				
Resolution		16		Bits
Digital Inputs[1] V_{IH}	+2 4		$+V_L$	V
V_{IL}	0		+0 8	V
I_{IH}, V_{IN} = +2 7V			+1 0	µA
I_{IL}, V_{IN} = +0 4V			−50	µA
Input Clock Frequency	10 0			MHz
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error		±2 0		%
Bipolar Zero Error		±30		mV
Differential Linearity Error		±0 001		% of FSR[2]
Noise (rms, 20Hz to 20kHz) at Bipolar Zero (V_{OUT} models)		6		µV
TOTAL HARMONIC DISTORTION				
V_O = ±FS at f = 991Hz PCM56P-K		0 002	0 0025	%
PCM56P-J		0 002	0 004	%
PCM56P		0 002	0 008	%
V_O = −20dB at f = 991Hz PCM56P-K		0 018	0 020	%
PCM56P-J		0 018	0 040	%
PCM56P		0 018	0 040	%
V_O = −60dB at f = 991Hz PCM56P-K		1 8	2 0	%
PCM56P-J		1 8	4 0	%
PCM56P		1 8	4 0	%
MONOTONICITY		15		Bits
DRIFT (0°C to +70°C)				
Total Drift[3]		±25		ppm of FSR/°C
Bipolar Zero Drift		±4		ppm of FSR/°C
SETTLING TIME (to ±0 006% of FSR)				
Voltage Output 6V Step		1 5		µs
1LSB		1 0		µs
Slew Rate		12		V/µs
Current Output, 1mA Step 10Ω to 100Ω load		350		ns
1kΩ load[4]		350		ns
WARM-UP TIME	1			Min
OUTPUT				
Voltage Output Configuration Bipolar Range		±3 0		V
Output Current	±8 0			mA
Output Impedance		0 10		Ω
Short Circuit Duration	Indefinite to Common			
Current Output Configuration				
Bipolar Range (±30%)		±1 0		mA
Output Impedance (±30%)		1 2		kΩ
POWER SUPPLY REQUIREMENTS[5]				
Voltage $+V_S$ and $+V_L$	+4 75	+5 00	+13 2	V
$-V_S$ and $-V_L$	−4 75	−5 00	−13 2	V
Supply Drain (No Load) +V ($+V_S$ and $+V_L$ = +5V)		+10 0	+17 0	mA
−V ($-V_S$ and $-V_L$ = −5V)		−25 0	−35 0	mA
+V ($+V_S$ and $+V_L$ = +12V)		+12 0		mA
−V ($-V_S$ and $-V_L$ = −12V)		−27 0		mA
Power Dissipation V_S and V_L = ±5V		175	260	mW
V_S and V_L = ±12V		468		mW
TEMPERATURE RANGE				
Specification	0		+70	°C
Operation	−25		+70	°C
Storage	−60		+100	°C

NOTES (1) Logic input levels are TTL/CMOS-compatible (2) FSR means full-scale range and is equivalent to 6V (±3V) for PCM56 in the V_{OUT} mode (3) This is the combined drift error due to gain, offset, and linearity over temperature (4) Measured with an active clamp to provide a low impedance for approximately 200ns (5) All specifications assume $+V_S$ connected to $+V_L$ and $-V_S$ connected to $-V_L$ If supplies are connected separately, $-V_L$ must not be more negative than $-V_S$ supply voltage to assure proper operation No similar restriction applies to the value of $+V_L$ with respect to $+V_S$

MECHANICAL



NOTE Leads in true position within .010" (25mm) R at MMC at seating plane

PINS Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragrah 3 2)

CASE Plastic

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	740	800	18 80	20 32
A_1	725	785	18 42	19 94
B	230	290	5 85	7 38
B_1	200	250	5 09	6 36
C	120	200	3 05	5 09
D	015	023	0 38	0 59
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	0 02	0 05	0 51	1 27
J	008	015	0 20	0 38
K	070	150	1 78	3 82
L	300 BASIC		7 63 BASIC	
M	0°	15°	0°	15°
N	010	030	0 25	0 76
P	025	050	0 64	1 27

ORDERING INFORMATION

Model	THD at FS (%)
PCM56P	0 008 Max
PCM56P-J	0 004
PCM56P-K	0 0025

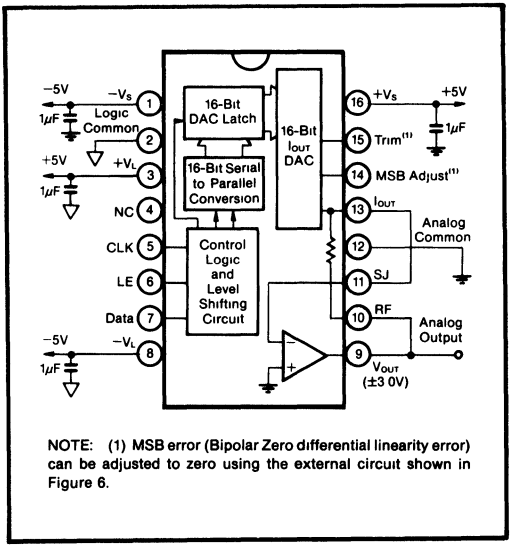
PIN ASSIGNMENTS

1	$-V_S$	Analog Negative Supply
2	LOG COM	Logic Common
3	$+V_L$	Logic Positive Supply
4	NC	No Connection
5	CLK	Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Supply
9	V_{OUT}	Voltage Output
10	RF	Feedback Resistor
11	SJ	Summing Junction
12	ANA COM	Analog Common
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trim-pot Terminal
16	$+V_S$	Analog Positive Supply

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages	±16VDC
Input Logic Voltage	−1V to $+V_S/+V_L$
Power Dissipation	. 850mW
Operating Temperature	−25°C to +70°C
Storage Temperature	−60°C to +100°C
Lead Temperature During Soldering	. 10s at 300°C

CONNECTION DIAGRAM



NOTE: (1) MSB error (Bipolar Zero differential linearity error) can be adjusted to zero using the external circuit shown in Figure 6.

DISCUSSION OF SPECIFICATIONS

The PCM56P is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for a D/A converter in audio applications are Total Harmonic Distortion, Differential Linearity Error, Bipolar Zero Error, parameter shifts with time and temperature, and settling time effects on accuracy.

The PCM56P is factory-trimmed and tested for all critical key specifications.

The accuracy of a D/A converter is described by the transfer function shown in Figure 1. Digital input to analog output relationship is shown in Table I. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Gain drift over temperature rotates the line (Figure 1) about the bipolar zero point and Offset drift shifts the line left or right over the operating temperature range. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The converter is designed so that these drifts are in opposite directions. This way the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage.

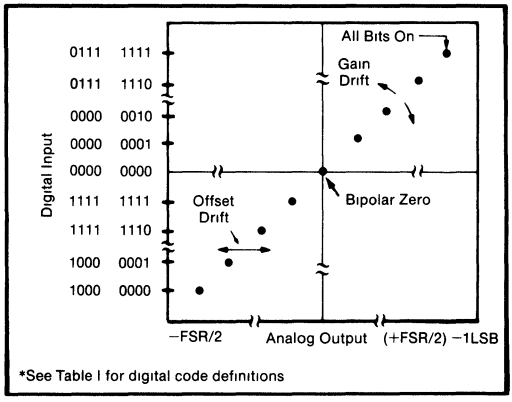


FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

TABLE I. Digital Input to Analog Output Relationship.

Digital Input	Analog Output		
Binary Twos Complement (BTC)	DAC Output	Voltage (V), V_{OUT} Mode	Current (mA), I_{OUT} Mode
7FFF Hex	+ Full Scale	+2 999908	−0 999970
8000 Hex	− Full Scale	−3 000000	+1 000000
0000 Hex	Bipolar Zero	0 000000	0 000000
FFFF Hex	Zero − 1LSB	−0 000092	+0 030500µA

DIGITAL INPUT CODES

The PCM56P accepts serial input data (MSB first) in the Binary Twos Complement (BTC) form. Refer to Table I for input output relationships.

BIPOLAR ZERO ERROR

Initial Bipolar Zero Error (Bit 1 "on" and all other bits "off") is the deviation from 0V out and is factory-trimmed to typically ±30mV at +25°C.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from an ideal 1LSB change from one adjacent output state to the next. DLE is important in audio applications because excessive DLE at Bipolar Zero (at the "major carry") can result in audible crossover distortion for low level output signals. Initial DLE on the PCM56P is factory trimmed to typically ±0.001% of FSR. The MSB DLE is adjustable to zero using the circuit shown in Figure 6.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy.

The PCM56P power supply sensitivity is shown by Figure 2. Normally, regulated power supplies with 1% or less ripple are recommended for use with the DAC. See also Power Supply Connections paragraph in the Installation and Operating Instructions section.

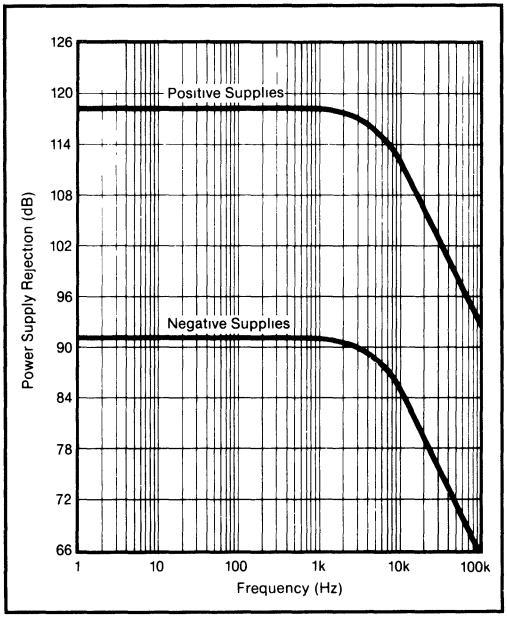


FIGURE 2. Power Supply Sensitivity.

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 3).

Settling times are specified to ±0.006% of FSR: one for a large output voltage change of 6V and one for a 1LSB change. The 1LSB change is measured at the major carry (0000 hex to ffff hex), the point at which the worst-case settling time occurs.

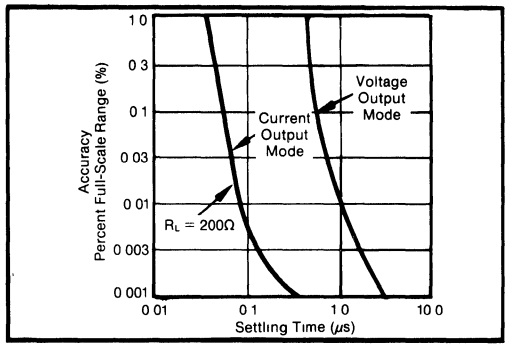


FIGURE 3. Full Scale Range Settling Time vs Accuracy.

STABILITY WITH TIME AND TEMPERATURE

The parameters of a D/A converter designed for audio applications should be stable over a relatively wide temperature range and over long periods of time to avoid undesirable periodic readjustment. The most important parameters are Bipolar Zero Error, Differential Linearity Error, and Total Harmonic Distortion. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The PCM56P is designed so that these drifts are in opposite directions so that the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage. Both DLE and THD are dependent upon the matching and tracking of resistor ratios and upon V_{BE} and h_{FE} of the current-source transistors. The PCM56P was designed so that any absolute shift in these components has virtually no effect on DLE or THD. The resistors are made of identical links of ultra-stable nichrome thin-film. The current density in these resistors is very low to further enhance their stability.

DYNAMIC RANGE

The Dynamic Range is a measure of the ratio of the smallest signals the converter can produce to the full-scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately $6 \times n$, or about 96dB of a 16-bit converter. The actual, or useful, dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit. However, this does point out that a resolution of at least 16 bits is required to obtain a 90dB minimum dynamic range, regardless of the accuracy of the converter. Another specification that is useful for audio applications is Total Harmonic Distortion.

TOTAL HARMONIC DISTORTION

THD is useful in audio applications and is a measure of the magnitude and distribution of the Linearity Error,

Differential Linearity Error, and Noise, as well as Quantization Error. To be useful, THD should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications.

The THD is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency and is expressed in percent or dB. The rms value of the PCM56P error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{1/n \sum_{i=1}^{n} [E_L(i) + E_Q(i)]^2} \qquad (1)$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the PCM56P at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \epsilon_{rms}/E_{rms} \qquad (2)$$

$$= \frac{\sqrt{1/n \sum_{i=1}^{n} [E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\%$$

where E_{rms} is the rms signal-voltage level.

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

For the PCM56P the test period was chosen to be 22.7μs (44.1kHz), which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 991Hz and the amplitude of the input signal is 0dB, −20dB, and −60dB down from full scale.

Figure 4 shows the typical THD as a function of output voltage.

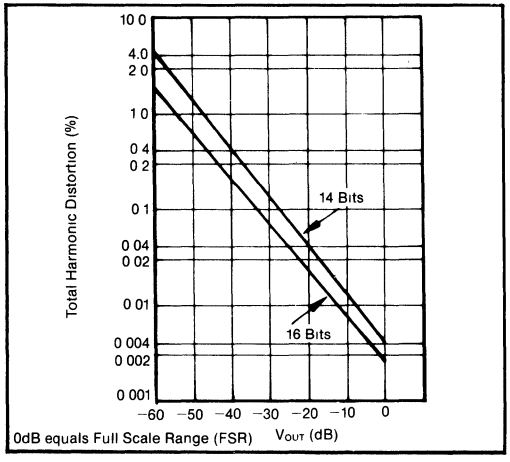


FIGURE 4. Total Harmonic Distortion (THD) vs V_{OUT}.

Figure 5 shows typical THD as a function of frequency.

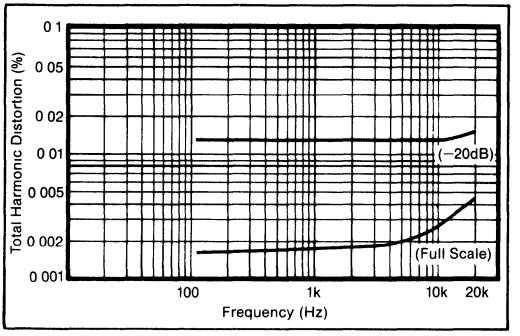


FIGURE 5. Total Harmonic Distortion (THD) vs Frequency.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the converter.

MSB ERROR ADJUSTMENT PROCEDURE (OPTIONAL)

The MSB error of the PCM56P can be adjusted to make the differential linearity error (DLE) at BPZ essentially zero. This is important when the signal output levels are very low, because zero crossing noise (DLE at BPZ) becomes very significant when compared to the small code changes occurring in the LSB portion of the converter.

Differential linearity error at bipolar zero and THD are guaranteed to meet data sheet specifications without any external adjustment. However, a provision has been made for an optional adjustment of the MSB linearity point which makes it possible to eliminate DLE error at BPZ. Two procedures are given to allow either static or dynamic adjustment. The dynamic procedure is preferred because of the difficulty associated with the static method (accurately measuring 16-bit LSB steps).

To statically adjust DLE at BPZ, refer to the circuit shown in Figure 6 or the PCM56 connection diagram.

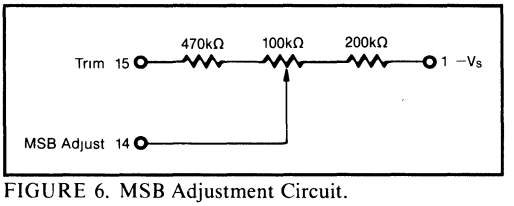


FIGURE 6. MSB Adjustment Circuit.

After allowing ample warm-up time (5–10 minutes) to assure stable operation of the PCM56, select input code FFFF hexadecimal (all bits on except the MSB). Measure the audio output voltage using a 6-1/2 digit voltmeter and record it. Change the digital input code to 0000 hexadecimal (all bits off except the MSB). Adjust the 100kΩ potentiometer to make the audio output read 92μV more than the voltage reading of the previous code (a 1LSB step = 92μV).

A much simpler method is to dynamically adjust the DLE at BPZ. Again, refer to Figure 6 for circuitry and component values. Assuming the device has been installed in a digital audio application circuit, send the appropriate digital input to produce a −80dB level sinusoidal output. While measuring the THD of the audio circuit output, adjust the 100kΩ potentiometer until a minimum level of distortion is observed.

INPUT TIMING CONSIDERATIONS

Figures 7 and 8 refer to the input timing required to interface the inputs of PCM56P to a serial input data stream. Serial data is accepted in Binary Twos Complement (BTC) with the MSB being loaded first. Data is clocked in on positive going clock (CLK) edges and is latched into the DAC input register on negative going latch enable (LE) edges.

The latch enable input must be high for at least one clock cycle before going low, and then must be held low for at least one clock cycle. The last 16 data bits clocked into the serial input register are the ones that are transferred to the DAC input register when latch enable goes low. In other words, when more than 16 clock cycles occur between a latch enable, only the data present during the last 16 clocks will be transferred to the DAC input register.

One requirement for clocking in all 16 bits is the necessity for a "17th" clock pulse. This automatically occurs when the clock is continuous (last bit shifts in on the first bit of the next data word). When the clock is stopped before the "17th" clock cycle occurs, however, the last serial input shift will not occur (the MSB will be in the bit 2 position). In any application where clock is noncontinuous, attention must be given to providing enough clocks to fully input the data word.

Figure 7 refers to the general input format required for the PCM56P. Figure 8 shows the specific relationships between the various signals and their timing constraints.

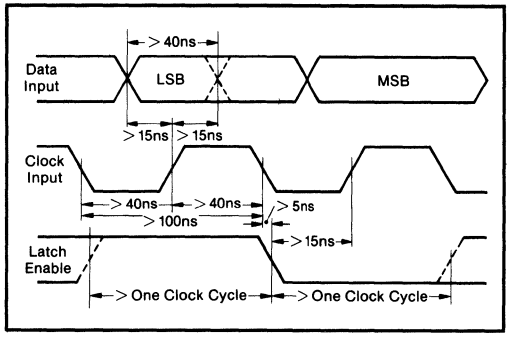
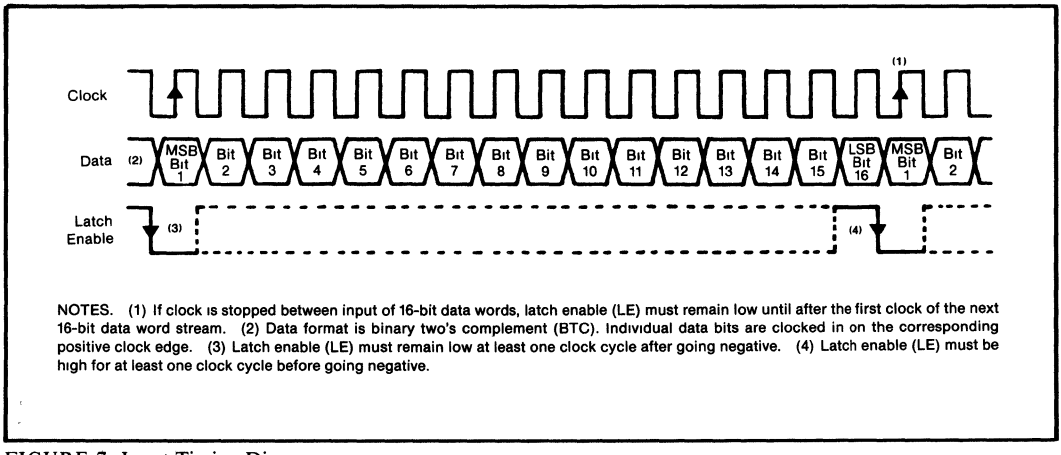


FIGURE 8. Input Timing Relationships.

INSTALLATION CONSIDERATIONS

If the optional external MSB error circuitry is used, a potentiometer with adequate resolution and a TCR of 100ppm/°C or less is required. Also, extra care must be taken to insure that no leakage path (either AC or DC) exists to pin 14. If the circuit is not used, pins 14 and 15 should be left open.

The PCM converter and the wiring to its connectors should be located to provide the optimum isolation from sources of RFI and EMI. The important consideration in the elimination of RF radiation or pickup is loop area;



NOTES. (1) If clock is stopped between input of 16-bit data words, latch enable (LE) must remain low until after the first clock of the next 16-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch enable (LE) must remain low at least one clock cycle after going negative. (4) Latch enable (LE) must be high for at least one clock cycle before going negative.

FIGURE 7. Input Timing Diagram.

therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together, they represent a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

APPLICATIONS

Figures 9 and 10 show a circuit and timing diagram for a single PCM56P used to obtain both left- and right-channel output in a typical digital audio system. The audio output of the PCM56P is alternately time-shared between the left and right channels. The design is greatly simplified because the PCM56P is a complete D/A converter requiring no external reference or output op amp.

A sample/hold (S/H) amplifier, or "deglitcher" is required at the output of the D/A for both the left and right channel, as shown in Figure 9. The S/H amplifier for the left channel is composed of A_1, SW_1, and associated circuitry. A_1 is used as an integrator to hold the analog voltage in C_1. Since the source and drain of the FET swtich operate at a virtual ground when "C" and "B" are connected in the sample mode, there is no increase in distortion caused by the modulation effect of R_{ON} by the audio signal.

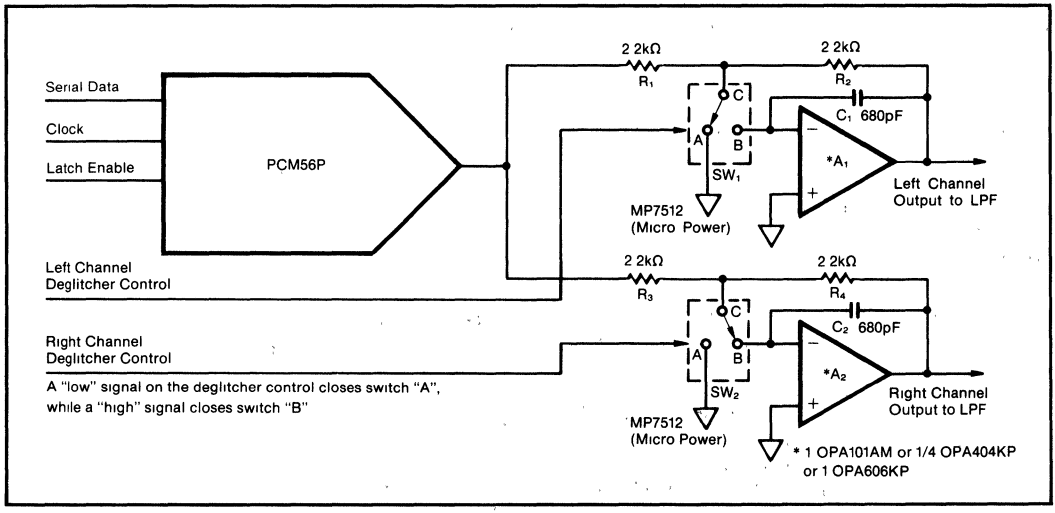


FIGURE 9. A Sample/Hold Amplifier (Deglitcher) is Required at the Digital-to-Analog Output for Both Left and Right Channels.

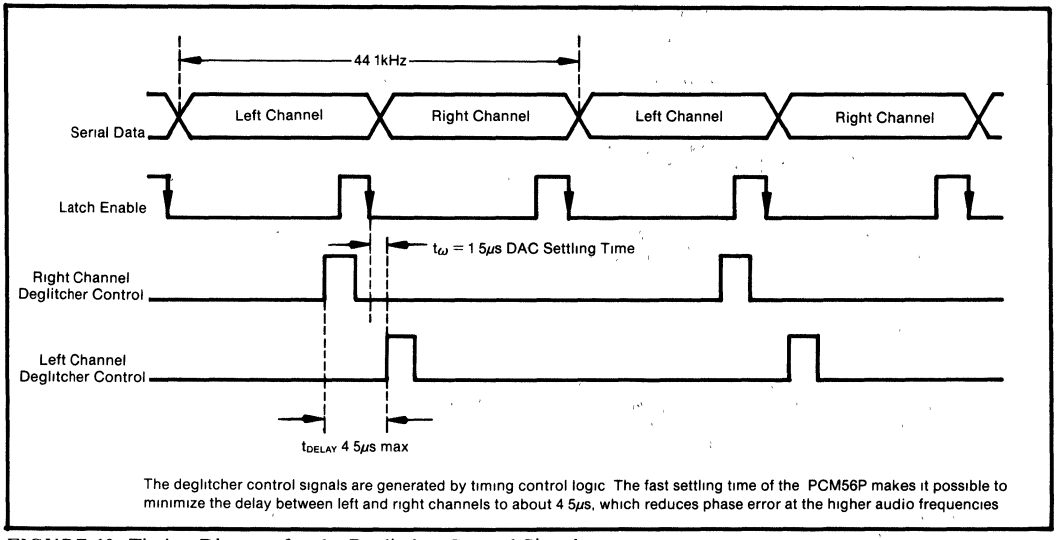


FIGURE 10. Timing Diagram for the Deglitcher Control Signals.

Figure 10 shows the deglitcher controls for both left and right channels which are produced by timing control logic. A delay of 1.5μs (tω) is provided to allow the output of the PCM56P to settle within a small error band around its final value before connecting it to the channel output. Due to the fast settling time of the PCM56P it is possible to minimize the delay between the left- and right-channel outputs when using a single D/A converter for both channels. This is important because the right- and left-channel data are recorded in-phase and the use of a slower D/A converter would result in significant phase error at higher frequencies.

The obvious solution to the phase shift problem in a two-channel system would be to use two D/A converters (one per channel) and time the outputs to change simultaneously. Figure 11 shows a block diagram of the final test circuitry used for PCM56P. It should be noted that no deglitching circuitry is required on the DAC output to meet specified THD performance. This means that when one PCM56P is used per channel, the need for all the sample/hold and controls circuitry associated with a single DAC (two-channel) design is effectively eliminated. The PCM56P is tested to meet its THD specifications without the need for output deglitching.

A low-pass filter is required after the PCM56P to remove all unwanted frequency components caused by the sampling frequency as well as those resulting from the discrete nature of the D/A output. This filter must have a flat frequency response over the entire audio band (0–20kHz) and a very high attenuation above 20kHz. Most previous digital audio circuits used a higher order (9–13 pole) analog filter. However, the phase response of an analog filter with these amplitude characteristics is nonlinear and can disturb the pulse-shaped characteristic transients contained in music.

SECOND GENERATION SYSTEMS

One method of avoiding the problems associated with a higher order analog filter would be to use digital filter oversampling techniques. Oversampling by a factor of two would move the sampling frequency (88.2kHz) out to a point where only a simple low-order phase-linear analog filter is required after the deglitcher output to remove unwanted intermodulation products. In a digital compact disc application, various VLSI chips perform the functions of error detection/correction, digital filtering, and formatting of the digital information to provide the clock, latch enable, and serial input to the PCM56P. These VLSI chips are available from several sources (Sony, Yamaha, Signetics, etc.) and are specifically optimized for digital audio applications.

Oversampled circuitry requires a very fast D/A converter since the sampling freuqency is multiplied by a factor of two or more (for each output channel). A single PCM56P can provide two-channel oversampling at a 4X rate (176.4kHz/channel) and still remain well within the settling time requirements for maintaining specified THD performance. This would reduce the complexities of the analog filter even further from that used in 2X oversampling circuitry.

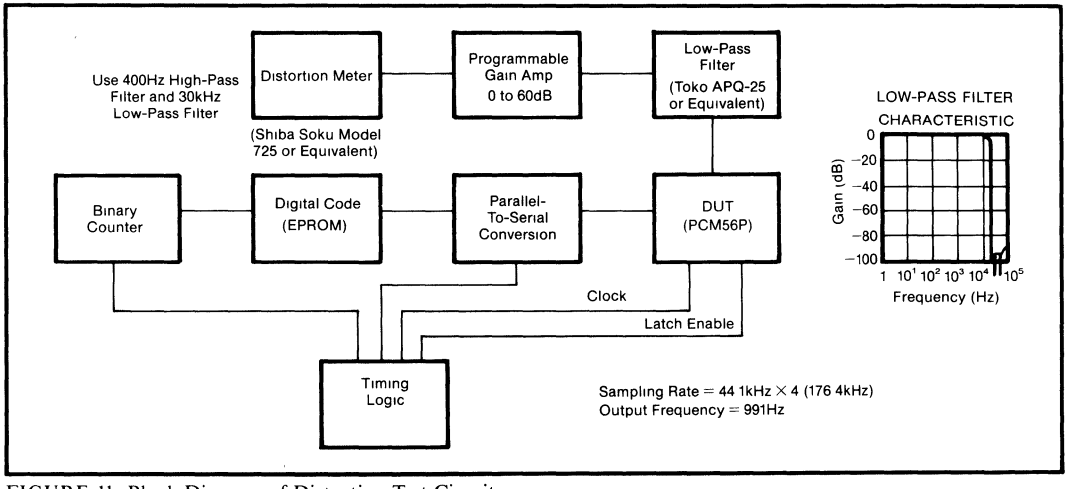


FIGURE 11. Block Diagram of Distortion Test Circuit.

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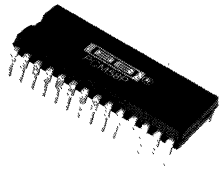


PCM58P

Precision, 18-Bit Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

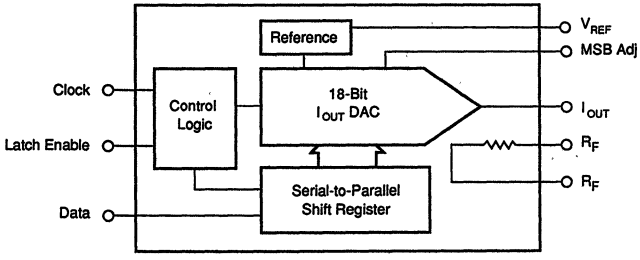
FEATURES

- 18-BIT MONOLITHIC AUDIO D/A CONVERTER
- VERY LOW MAX THD+N: –96dB Without External Adjustment; PCM58P-K
- SERIAL INPUT FORMAT 100% COMPATIBLE WITH INDUSTRY STD 16-BIT PCM56P
- VERY FAST SETTLING, GLITCH-FREE CURRENT OUTPUT (200ns)
- LOW-NOISE SCHMITT TRIGGER LOGIC INPUT CIRCUITRY
- COMPLETE WITH REFERENCE
- RELIABLE PLASTIC 28-PIN DIP PACKAGE

DESCRIPTION

The PCM58P is a complete, precision 18-bit digital-to-analog converter with ultra-low distortion over a very wide frequency range. The latched serial input data format of the PCM58P is totally based on the widely successful 16-bit PCM56P format (with the addition of two more data bits). The PCM58P features a very low noise and fast settling current output. The PCM58P is an excellent example of "latest generation" technology in the ever growing BURR-BROWN PCM product family of low-cost/high performance data converters.

The PCM58P comes in a 28-pin plastic DIP package. A provision is made for external adjustment of the four MSBs to further improve the PCM58P's specifications, if desired. Applications include very low distortion frequency synthesis and high-end consumer and professional digital audio applications.



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PDS-868

SPECIFICATIONS

ELECTRICAL

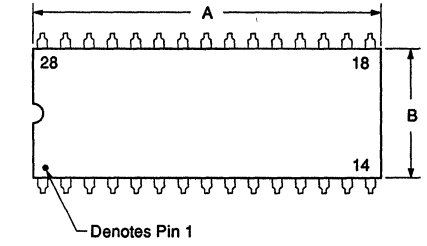
All Specifications at 25°C, and $\pm V_{CC}$ = +5.0V and –12.0V unless otherwise noted.

PARAMETER	CONDITIONS	PCM58P/P-J/P-K MIN	TYP	MAX	UNITS
RESOLUTION				18	BITS
DYNAMIC RANGE			108		dB
INPUT					
DIGITAL INPUT					
Logic Family			TTL/CMOS Compatible		
Logic Level: V_{IH}		+2.0		$+V_{CC}$	V
V_{IL}		0.0		0.8	V
I_{IH}	V_{IH} = +2.7V			+1.0	µA
I_{IL}	V_{IL} = +0.4V			–50	µA
Data Format			Serial BTC[1]		
Input Clock Frequency		16.9	20		MHz
DYNAMIC CHARACTERISTICS					
TOTAL HARMONIC DISTORTION + N[2]	Without MSB Adjustments				
PCM58P:					
f = 991Hz (0dB)[3]	f_S = 176.4kHz[4]		–94	–92	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–74	–72	dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–40	–34	dB
PCM58P-J:					
f = 991Hz (0dB)	f_S = 176.4kHz		–96	–94	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–80	–74	dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–40	–34	dB
PCM58P-K					
f = 991Hz (0dB)	f_S = 176.4kHz		–100	–96	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–82	–80	dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–42	–40	dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±1	±2	%
Bipolar Zero Error[5]			±10		mV
Gain Drift	0°C to 70°C		25		ppm/°C
Bipolar Zero Drift	0°C to 70°C		4		ppm of FSR/°C
Warm-up Time		1			Minute
IDLE CHANNEL SNR[6]	20Hz to 20KHz at BPZ[7]		+126		dB
POWER SUPPLY REJECTION			+72		dB
OUTPUT					
ANALOG OUTPUT					
Output Range		±0.98	±1.0	±1.02	mA
Output Impedance			1.2		kΩ
Internal Rfeedback			3		kΩ
Settling Time	1mA Step		200		ns
Glitch Energy		Meets all THD+N Specs Without External Deglitching			
POWER SUPPLY REQUIREMENTS					
$+V_{CC}$ Supply Voltage		+4.75	+5.00	+5.50	V
$-V_{CC}$ Supply Voltage		–10.8	–12.0	–13.2	V
Supply Current $+I_{CC}$	$+V_{CC}$ = +5.0V		+10		mA
$-I_{CC}$	$-V_{CC}$ = –12.0V		–30		mA
Power Dissipation			410		mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–30		+70	°C
Storage		–60		+100	°C

NOTES: (1) Binary Two's Complement coding. (2) Ratio of (Distortion$_{RMS}$ + Noise$_{RMS}$) / Signal$_{RMS}$. (3) D/A converter output frequency/signal level. (4) D/A converter sample frequency (4 x 44.1kHz; 4 times oversampling). (5) Offset error at bipolar zero. (6) Measured using an OPA27 and 10kΩ feedback and an A-weighted filter. (7) Bipolar Zero.

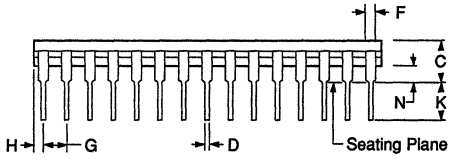
MECHANICAL

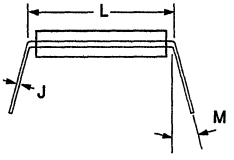
P Package—28-Pin Plastic DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.350	1.450	34.29	36.83
B	.520	.575	13.21	14.61
C	.169	.224	4.29	5.70
D	.015	.023	0.38	0.58
F	.043	.062	1.09	1.57
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.150	2.54	3.81
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.040	0.46	1.02

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers are shown for reference only. Numbers may not be marked on package. Case: plastic, Weight: 4.3 grams (0.15oz.)

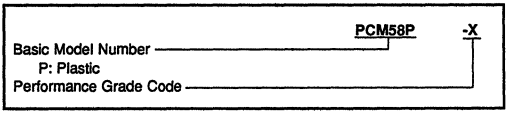




PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
P1	Decoupling Capacitor	CAP
P2	+Vcc Voltage Supply	$+V_{CC}$
P3	Decoupling Capacitor	CAP
P4	Decoupling Capacitor	CAP
P5	Bipolar Offset Point	BPO
P6	Current DAC I_{OUT}	I_{OUT}
P7	Feedback Resistor	R_{F1}
P8	Analog Common	ACOM
P9	$-V_{CC}$ Voltage Supply	$-V_{CC}$
P10	Feedback Resistor	R_{F2}
P11	Digital Common	DCOM
P12	No Connection	NC
P13	$+V_{CC}$ Voltage Supply	$+V_{CC}$
P14	No Connection	NC
P15	Decoupling Capacitor	CAP
P16	Clock	CLK
P17	DAC Latch Enable	LE
P18	No Connection	NC
P19	Data Input	DATA
P20	$-V_{CC}$ Voltage Supply	$-V_{CC}$
P21	No Connection	NC
P22	No Connection	NC
P23	No Connection	NC
P24	Bit 4 Adjust	B4 ADJ
P25	Bit 3 Adjust	B3 ADJ
P26	Bit 2 Adjust	B2 ADJ
P27	Bit 1 (MSB) Adjust	B1 ADJ
P28	Bit Adjust V_{POT}	V_{POT}

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS

$\pm V_{cc}$ Supply Voltages	+6V; −16V
Input Logic Voltage	−1V to $+V_{cc}$
Storage Temperature	−60°C to +100°C
Lead Temperature during soldering	10s at +300°C

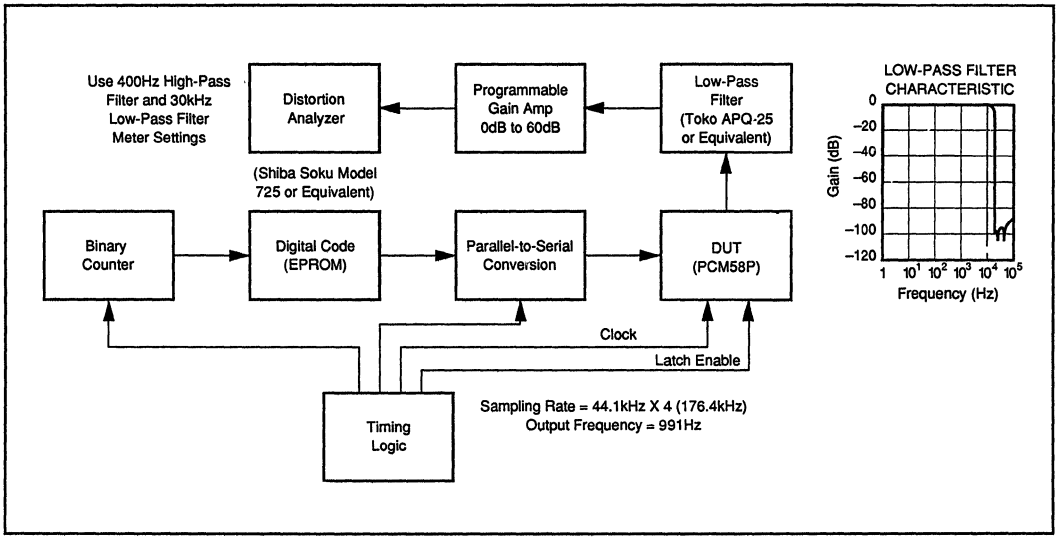


FIGURE 1. PCM58P Production THD+N Test Setup.

DISCUSSION OF SPECIFICATIONS

TOTAL HARMONIC DISTORTION + NOISE

The key specification for the PCM58P is total harmonic distortion plus noise. Digital data words are read into the PCM58P at four times the standard audio sampling frequency of 44.1kHz or 176.4kHz such that a sinewave output of 991Hz is realized. For production testing the output of the DAC goes to a programmable gain amplifier to provide gain at lower signal output test levels and then through a 20kHz low pass filter before being fed into an analog type distortion analyzer. See Figure 1, which shows a block diagram of the production THD+N test setup.

In terms of signal measurement, THD+N is the ratio of $Distortion_{RMS}$ + $Noise_{RMS}$ / $Signal_{RMS}$ expressed in dB. For the PCM58P, THD+N is 100% tested at three different output levels using the test setup shown in Figure 1. It is significant to note that this test setup does not include any output deglitching circuitry. This means the PCM58P meets even it's –60dB THD+N specification without use of external deglitchers.

ABSOLUTE LINEARITY

Even though absolute integral and differential linearity specs are not given for the PCM58P, the extremely low THD+N performance is typically indicative of 15-bit to 16-bit integral linearity in the DAC depending on the grade specified. The relationship between THD+N and linearity, however, is not such that an absolute linearity specification for every individual output code can be guaranteed.

IDLE CHANNEL SNR

Another appropriate spec for a digital audio converter is idle channel signal to noise ratio (idle channel SNR). This is the ratio of the noise on the DAC output at bipolar zero in relation to the full scale range of the DAC. The output of the DAC is band-limited from 20Hz to 20kHz and an A-weighted filter is applied to make this measurement. The idle channel SNR for the PCM58P is typically greater than +126dB, making it ideal for low-noise applications.

OFFSET, GAIN, AND TEMPERATURE DRIFT

Although the PCM58P is primarily meant for use in dynamic applications, specifications are also given for more traditional DC parameters such as gain error, bipolar zero offset error, and temperature gain drift and offset drift.

TIMING CONSIDERATIONS

The PCM58P accepts TTL compatible logic input levels. Noise immunity is enhanced by the use of Schmitt trigger input architectures on all input signal lines. The data format of the PCM58P is binary two's complement (BTC) with the most significant bit (MSB) being first in the serial input bit stream. Table 1 describes the exact input data to voltage output coding relationship. Any number of bits can precede the 18 bits to be loaded as only the last 18 will be transferred to the parallel DAC register after LE (P17; latch enable) has gone low.

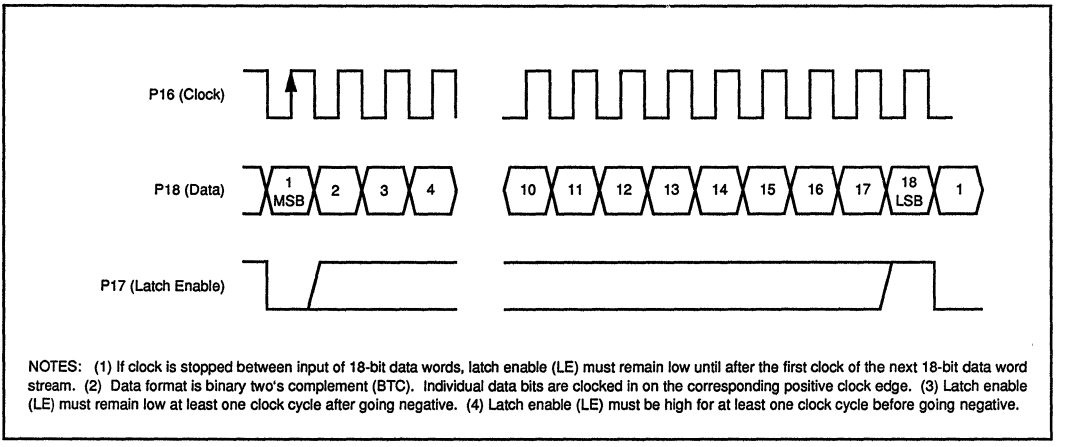
The individual DAC serial input data bit shifts transfer are triggered on positive CLK edges. The serial to parallel data transfer to the DAC occurs on the falling edge of LE (P17). Refer to Figure 2 for graphical relationships of these signals.

MAXIMUM CLOCK RATE

The maximum clock rate of 16.9mHz for the PCM58P is derived by multiplying the standard audio sample rate of 44.1kHz times sixteen (16X oversampling) times the standard audio word bit length of 24 (44.1kHz x 16 x 24 = 16.9mHz). Note that this clock rate accommodates a 24-bit word length, even though only 18 bits are actually being used.

TABLE I. PCM60P Input/Output Relationships.

DIGITAL INPUT	ANALOG OUTPUT		
Binary Two's Complement (BTC)	DAC Output	Voltage (V) V_{out} Mode	Current (mA) I_{out} Mode
3FFFF Hex	+FS	+2.9999943	–0.9999981
20000 Hex	BPZ	0.0000000	0.0000000
1FFFF Hex	BPZ – 1LSB	–0.0000057	+0.0000019
00000 Hex	–FS	–3.0000000	+1.0000000



NOTES: (1) If clock is stopped between input of 18-bit data words, latch enable (LE) must remain low until after the first clock of the next 18-bit data word stream. (2) Data format is binary two's complement (BTC). Individual data bits are clocked in on the corresponding positive clock edge. (3) Latch enable (LE) must remain low at least one clock cycle after going negative. (4) Latch enable (LE) must be high for at least one clock cycle before going negative.

FIGURE 2. PCM58P Timing Diagram.

"STOPPED-CLOCK" OPERATION

The PCM58P is normally operated with a continuous clock input signal. If the clock is to be stopped in between input data words, the last 18-bits shifted in are not actually shifted from the serial register to the latched parallel DAC register until LE (latch enable) goes low. If the clock input (P16, CLK) is stopped between data words, LE (P17) must remain low until after the first clock cycle of the next data word to insure proper DAC operation. In either case, the setup and hold times for DATA and LE must still be observed as shown in Figure 3.

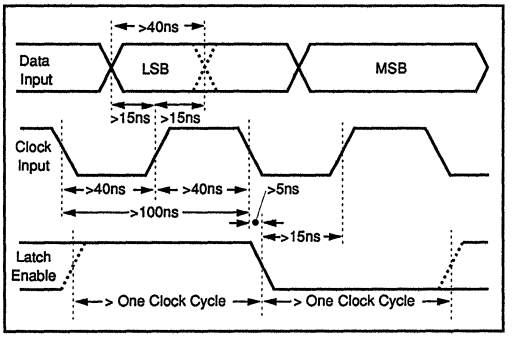


FIGURE 3. PCM58P Setup and Hold Timing Diagram.

INSTALLATION

Refer to Figure 4 for proper connection of the PCM58P in the voltage-out mode using the internal feedback resistor. The feedback resistor connections (P7 and P10) should be connected to ACOM (P8) if not used. The PCM58P requires only a +5V and –12V supply. It is very important that these supplies be as "clean" as possible to reduce coupling of supply noise to the output. Power supply decoupling capacitors shown in Figure 4 should be used, regardless of how good the supplies are to maximize power supply rejection. All grounds should be connected to the analog ground plane as close to the PCM58P as possible.

FILTER CAPACITOR REQUIREMENTS

As shown in Figure 4, other various decoupling capacitors are required around the supply and reference points with no special tolerances being required. Placement of all capacitors should be as close to the appropriate pins of the PCM58P as possible to reduce noise pickup from surrounding circuitry.

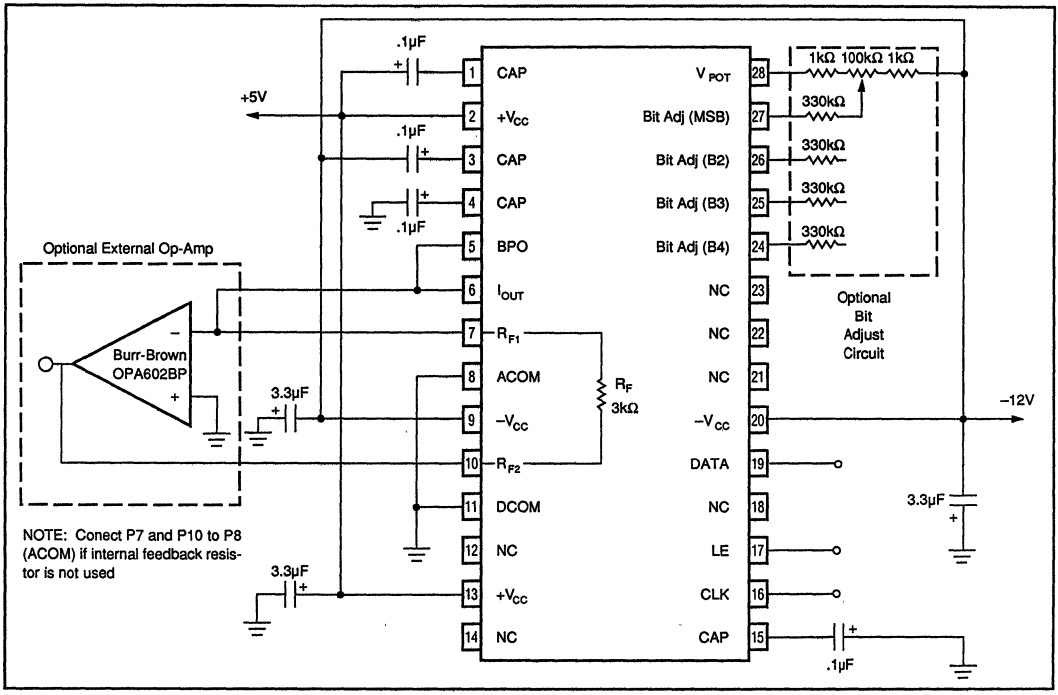


FIGURE 4. PCM58P Connection Diagram.

MSB ADJUSTMENT CIRCUITRY

With the optional bit adjustment circuitry shown in Figure 4, even greater performance can be realized by reducing the first four major bit carry output errors to zero. The most important adjustment for low level outputs would be the step between BPZ (bipolar zero; MSB on, all other bits off) and the code, which is one LSB less than BPZ (MSB off, all other bits on), since every crossing of zero would go through this bipolar major carry point. This MSB bit adjustment would be made by outputing a very low level signal sine wave and calibrating the 100kΩ potentiometer circuit connected to P28 and P27 while monitoring the THD+N of the PCM58P until peak performance is observed.

Bits 2 through 4 can also be adjusted if desired to obtain optimum full-scale output THD+N performance. An additional 100kΩ potentiometer adjustment circuit is required for every additional bit to be adjusted. If bit adjustment is not performed, the respective pins on the PCM58P should be left open.

Once bit adjustment is performed, the reference voltage at VPOT (P28) will track the internal reference, insuring that the THD+N performance of the PCM58P will remain unaffected by external temperature changes.

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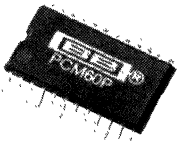


PCM60P

16-Bit CMOS Monolithic Audio DIGITAL-TO-ANALOG CONVERTER

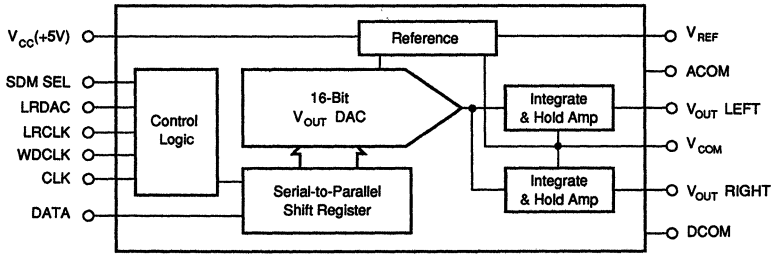
FEATURES

- LOW COST 16-BIT 2-CHANNEL CMOS MONOLITHIC D/A CONVERTER
- SINGLE SUPPLY +5V OPERATION
- 50mW POWER DISSIPATION
- GLITCH-FREE VOLTAGE OUTPUTS
- LOW DISTORTION: –86dB MAX THD+N
- COMPLETE WITH REFERENCE
- SERIAL INPUT FORMAT
- SINGLE OR DUAL DAC MODE OPERATION
- PLASTIC 24-PIN SOIC PACKAGE

DESCRIPTION

The PCM60P is a low cost, dual output 16-bit CMOS digital-to-analog converter. The PCM60P features true glitch-free voltage outputs and requires only a single +5V supply. The PCM60P doesn't require an external reference. Total power dissipation is less than 50mW max. Low maximum Total Harmonic Distortion + Noise (–86dB max; PCM60P-J) is 100% tested. Either one or two channel output modes are fully user selectable.

The PCM60P comes in a space-saving 24-pin plastic SOIC package. PCM60P accepts a serial data input format and is compatible with other BURR-BROWN PCM products such as the industry standard PCM56P.



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PDS-869A

SPECIFICATIONS

ELECTRICAL

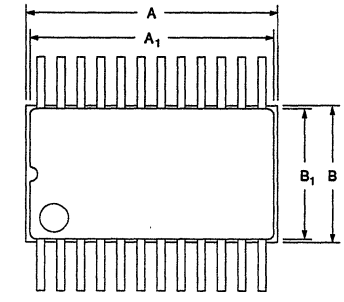
All Specifications at 25°C, and $+V_{CC}$ = +5.00V unless otherwise noted.

PARAMETER	CONDITIONS	PCM60P/P-J MIN	PCM60P/P-J TYP	PCM60P/P-J MAX	UNITS
RESOLUTION				16	Bits
DYNAMIC RANGE			96		dB
INPUT					
DIGITAL INPUT					
Logic Family			TTL Compatible CMOS		
Logic Level: V_{IH}	I_{IH} = +40µA max	+2.4		+5.25	V
V_{IL}	I_{IL} = –40µA max	0.0		0.8	V
Data Format			Serial BTC[1]		
Input Clock Frequency		8.5			MHz
DYNAMIC CHARACTERISTICS					
TOTAL HARMONIC DISTORTION + N[2]					
PCM60P:					
f = 991Hz (0dB)[3]	f_S = 176.4kHz[4]		–88	–82	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–68		dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–28		dB
PCM60P-J:					
f = 991Hz (0dB)	f_S = 176.4kHz		–92	–86	dB
f = 991Hz (–20dB)	f_S = 176.4kHz		–68		dB
f = 991Hz (–60dB)	f_S = 176.4kHz		–28		dB
CHANNEL SEPARATION		+80	+85		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error	V_{OUT} = 2.8 Vp-p		±2	±10	%
Gain Mismatch	Channel to Channel		±1		%
Bipolar Zero Error[5]			±30		mV
Gain Drift	0°C to 70°C		100		ppm/°C
Warm-up Time		1			minute
IDLE CHANNEL SNR[6]	20—20kHz; with A-weighted filter		+90		dB
OUTPUT					
ANALOG OUTPUT					
Output Range			2.8		Vp-p
Output Impedance			2		Ω
Short Circuit Duration	To Be Determined				
Settling Time	Sufficient to Meet 176.4kHz THD+N Specs				
Glitch Energy	Meets all THD+N Specs Without External Output Deglitching				
POWER SUPPLY REQUIREMENTS					
$+V_{CC}$ Supply Voltage		+4.75	+5.00	+5.25	V
Supply Current			+9.5		mA
Power Dissipation	V_{CC} = +5.00V			50	mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating		–30		+70	°C
Storage		–60		+100	°C

NOTE: 1) Binary Two's Complement coding. (2) Ratio of ($Distortion_{RMS}$ + $Noise_{RMS}$) / $Signal_{RMS}$. (3) D/A converter output frequency/signal level (on both left and right channels). (4) D/A converter sample frequency (4 x 44.1kHz; 4 times oversampling per channel). (5) Offset error at bipolar zero. (6) Ratio of output at BPZ (Bipolar Zero) to the full scale range using a 20kHz low pass filter in addition to an A-weighted filter.

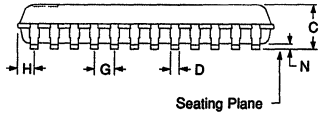
MECHANICAL

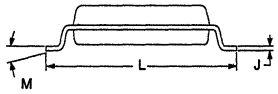
P Package—24-Pin SOIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.614	.630	15.60	16.00
A_1	.610	TYP	15.5	TYP
B	.328	.346	8.33	8.80
B_1	.331	TYP	8.4	TYP
C	—	.098	—	2.50
D	.012	.020	0.30	0.50
G	.046	.054	1.17	1.37
H	.075	.115	1.91	2.92
J	.0039	.010	0.10	0.26
L	.453	.476	11.5	12.1
M	0°	TYP	0°	TYP
N	.0039		0.10	

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin material and plating composition conform to method 2003 solderability of MIL-STD-883 (except paragraph 3.2)





PIN ASSIGNMENTS

PIN	DESCRIPTION	MNEMONIC
P1	Left/Right Clock	LRCLK
P2	Word Clock	WDCLK
P3	Clock	CLK
P4	Data	DATA
P5	No Connection	NC
P6	No Connection	NC
P7	Digital Common	DCOM
P8	Analog Common	ACOM
P9	No Connection	NC
P10	Left Channel V_{OUT}	L CH Out
P11	Output Common	VCOM
P12	Right Channel V_{OUT}	R CH Out
P13	$+V_{CC}$ Analog Supply	$+V_{CC}$
P14	$+V_{CC}$ Analog Supply	$+V_{CC}$
P15	Reference Decouple	C_{REF}
P16	No Connection	NC
P17	VREF Sense	V_{REF} SEN
P18	Voltage Reference	V_{REF}
P19	$+V_{CC}$ Analog Supply	$+V_{CC}$
P20	$+V_{CC}$ Analog Supply	$+V_{CC}$
P21	$+V_{CC}$ Digital Supply	$+V_{CC}$
P22	No Connection	NC
P23	Single DAC Mode	SDM SEL
P24	Left/Right DAC Select	LRDAC

ORDERING INFORMATION

PCM60P -X

Basic Model Number
P: Plastic
Performance Grade Code

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	+10V
Input Logic Voltage	–3V to +5.25V
Power Dissipation	50mW
Operating Temperature	–30°C to +70°C
Storage Temperature	–60°C to +100°C
Lead Temperature (soldering, 10s)	+300°C

PACKAGE PIN NUMBERS				SERIAL	LEFT	RIGHT
P23 SDM SEL	P24 LRDAC	P1 LRCLCK	P2 WDCLK	DATA WORD INPUT	CHANNEL OUTPUT	CHANNEL OUTPUT
0	X	0	0	Right	Hold	Hold
0	X	0	1	Right	Integrate	Hold
0	X	1	0	Left	Hold	Hold
0	X	1	1	Left	Hold	Integrate
1	0	0	0	Inhibited	V_{COM}	Hold
1	0	0	1	Inhibited	V_{COM}	Hold
1	0	1	0	Left	V_{COM}	Integrate
1	0	1	1	Left	V_{COM}	Integrate
1	1	0	0	Right	V_{COM}	Hold
1	1	0	1	Right	V_{COM}	Hold
1	1	1	0	Inhibited	V_{COM}	Integrate
1	1	1	1	Inhibited	V_{COM}	Integrate

NOTE: Positive edge of CLK (P3) latches LRCLK (P1), WDCLK (P2), and DATA (P4).

TABLE I. PCM60P Logic Truth Table.

THEORY OF OPERATION

The PCM60P is a dual output, 16-bit CMOS digital-to-analog audio converter. The PCM60P, complete with internal reference, has two glitch-free voltage outputs and requires only a single +5V power supply. Output modes using either one or two channels per DAC are user selectable. The PCM60P accepts a serial data input format that is compatible with other BURR-BROWN PCM products such as the industry standard PCM56P.

ONE DAC TWO-CHANNEL OPERATION

Normally, the PCM60P is operated with a continuous clock input in a two-channel output mode. This mode is selected when SDM SEL is held low (P23; single DAC mode select). Refer to the truth table shown by Table 1 for exact control logic relationships. Data for left and right channel output is loaded alternately into the PCM60P while the control logic switches the left and right output amplifiers between the appropriate integrate and hold modes. Data word latching is controlled by WDCLK (P2; word clock) and channel selec-

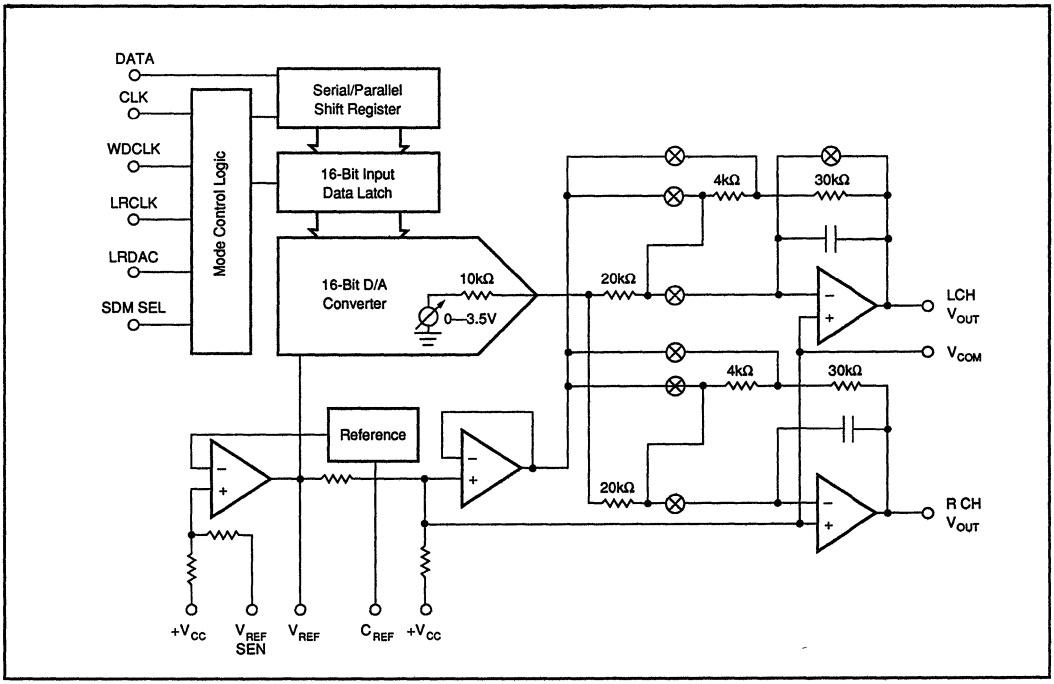


FIGURE 1. PCM60P Block Diagram

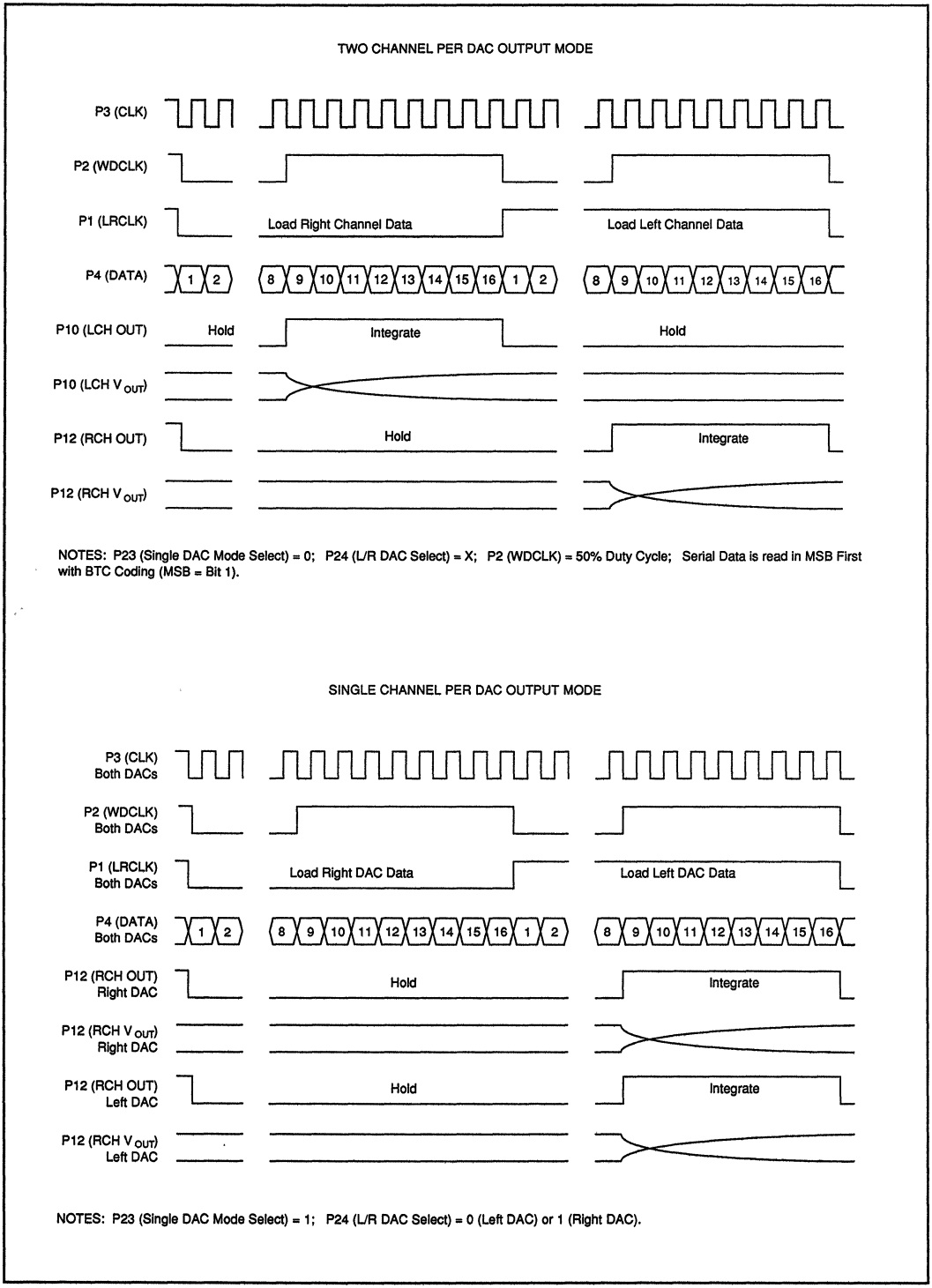


FIGURE 2. PCM60P Timing Diagram.

DIGITAL INPUT	ANALOG OUTPUT	
Binary Two's Complement (BTC)	DAC Output (V)	Voltage (V) V_{out} Mode
7FFF Hex	+FS	+3.5629443
0000 Hex	BPZ	+2.1629871
FFFF Hex	BPZ – 1	+0.7629871
8000 Hex	–FS	+1.1000000
2E5B Hex	VCOM	+2.6700000

TABLE II.PCM60P Input/Output Relationships.

tion is made by LRCLK (P1; left/right clock). The block diagram in Figure 1 shows how a single DAC output provides switched output to both integrate and hold amplifiers. Figure 2 shows the timing for the single DAC two-channel mode of operation. Output between left and right channels in this mode is not in phase. See Figure 3 for proper connection of the PCM60P in the two-channel DAC mode.

TWO DAC TWO-CHANNEL OPERATION

In phase, two-channel output can be obtained by using two PCM60Ps and choosing the single DAC mode (setting P23 SDM SEL high). With the use of a high or low input level on LRDAC (P24; left/right DAC select), each DAC can have its right channel output dedicated to either left or right data input with no additional input signals being required to latch the appropriate data from an alternating L/R data word input stream. In the single DAC mode, the PCM60P's left channel output is disabled and held at $+V_{COM}$. In this mode both DACs share common inputs for DATA, CLK, WDCLK, and LRCLK. Otherwise circuit connection is the same as the two-channel DAC mode, with the exception of LRDAC whose level selects whether the single DAC will output dedicated left or right channel data.

INTEGRATE & HOLD OUTPUT AMPLIFIERS

The PCM60P incorporates integrate and hold amplifiers on each output channel. This allows a single, very fast DAC to feed both amplifiers and reduce circuit complexity. It also serves to block the output glitch from the DAC to the individual channel outputs and effectively makes the PCM60P outputs "glitch-free." The PCM60P is a single +5V supply device with a voltage output swing of 2.8Vp–p The outputs swing asymmetrically around VCOM ($+V_{CC}$ – 2.33V). See Table II for exact input/output relationships. Since true CMOS amplifiers are used on the PCM60P, the load resistance on the outputs should not be less than 100KΩ and the capacitive loads should not exceed 100pf. For maximum low-distortion performance, output buffer amplifiers should be considered.

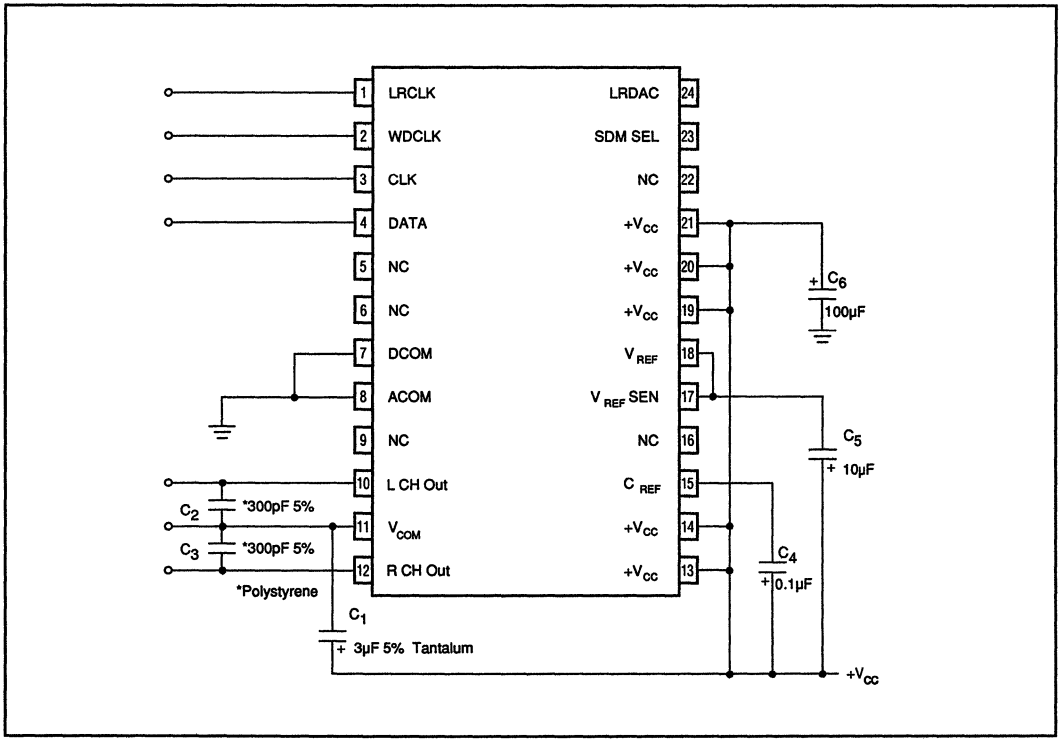


FIGURE 3. PCM60P Connection Diagram.

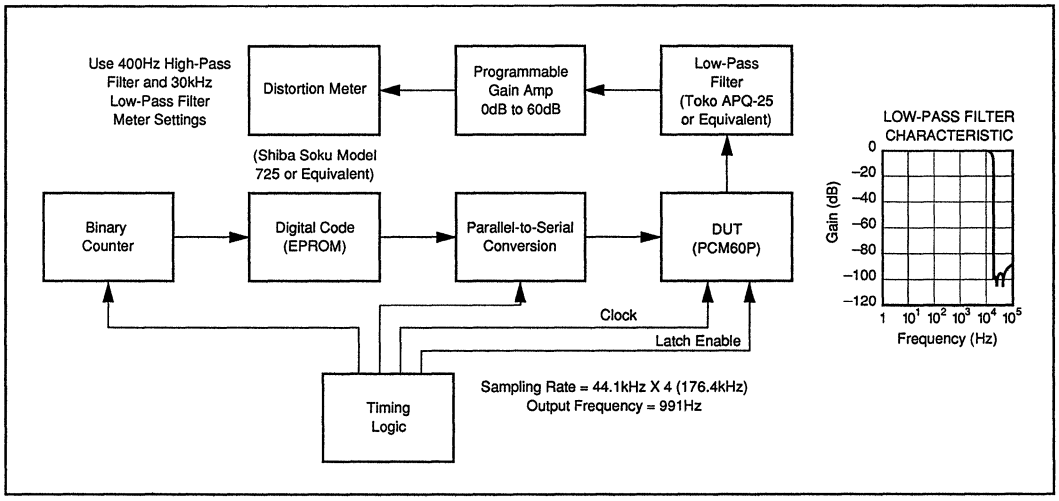


FIGURE 4. THD + N Test Setup Diagram.

DISCUSSION OF SPECIFICATIONS

TOTAL HARMONIC DISTORTION + NOISE

The key specification for the PCM60P is total harmonic distortion plus noise. Digital data words are read into the PCM60P at four times the standard audio sampling frequency of 44.1kHz or 176.4kHz for each channel such that a sine-wave output of 991Hz is realized. For production testing the output of the DAC goes to a programmable gain amplifier to provide gain at lower signal output test levels and then through a 20kHz low pass filter before being fed into an analog type distortion analyzer. Figure 4 shows a block diagram of the production THD+N test setup.

In terms of signal measurement, THD+N is the ratio of $DISTORTION_{RMS}$ + $NOISE_{RMS}$ / $SIGNAL_{RMS}$ expressed in dB. For the PCM60P, THD+N is 100% tested at three different output levels using the test setup shown in Figure 4. It is significant to note that this circuit does not include any output deglitching circuitry. This means the PCM60P meets even its –60dB THD+N specification without use of external deglitchers.

ABSOLUTE LINEARITY

Even though absolute integral and differential linearity specs are not given for the PCM60P, the extremely low THD+N performance is typically indicative of 14-bit to 15-bit integral linearity in the DAC depending on the grade specified. The relationship between THD+N and linearity, however, is not such that an absolute linearity specification for every individual output code can be guaranteed.

IDLE CHANNEL SNR

Another appropriate spec for a digital audio converter is idle channel signal to noise ratio (idle channel SNR). This is the ratio of the noise on either DAC output at bipolar zero in relation to the full scale range of the DAC. The output of the DAC is band limited from 20Hz to 20kHz and an A-weighted filter is applied to make this measurement.

OFFSET, GAIN, AND TEMPERATURE DRIFT

The PCM60P is specified for other important parameters such as channel separation and gain mismatch between output channels. And although the PCM60P is primarily meant for use in dynamic applications, typical specs are also given for more traditional DC parameters such as gain error, bipolar zero offset error, and temperature gain drift.

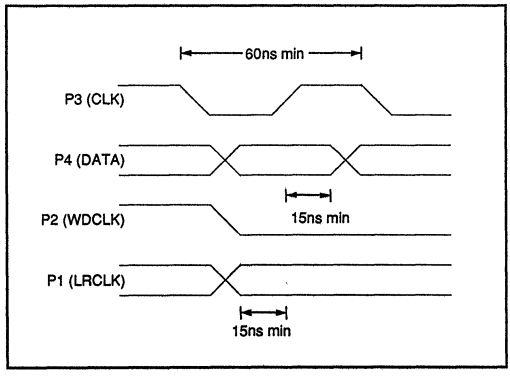


FIGURE 5. PCM60P Setup and Hold Timing Diagram

TIMING CONSIDERATIONS

The data format of the PCM60P is binary two's complement (BTC) with the most significant bit (MSB) being first in the serial input bit stream. Table 2 describes the exact input data to voltage output coding relationship. Any number of bits can proceed the 16-bits to be loaded as only the last 16 will be transferred to the parallel DAC register on the first positive edge of CLK (P3; clock input) after WDCLK (P2; word clock) has gone low. All inputs to the PCM60P are TTL level compatible.

WDCLK DUTY CYCLE

The input signal that controls when data is loaded and how long each output is in the integrate mode is WDCLK (P2). It is therefore recommended that a 50% (high) duty cycle be maintained on WDCLK. This will ensure that each output will have enough time to reach it's final output value, and that the output level of each channel will be within the gain mismatch specification. Refer to Figure 2 for exact timing relationships of WDCLK to CLK and LRCLK and the outputs of the PCM60P. The WDCLK can be high longer than 50% as long as setup and hold times shown in Figure 5 are observed and the time high is roughly equivalent for both left and right channels.

SETUP AND HOLD TIMES

The individual serial data bit shifts, and the serial to parallel data transfer, and left/right control are triggered on positive CLK edges. The setup time required for DATA, WDCLK, and LRCLK to be latched by the next positive going CLK is 15ns minimum. A minimum hold time of 15ns is also required after the positive going CLK edge for each data bit to be shifted into the serial input register. Refer to Figure 5 for the timing relationship of these signals.

MAXIMUM CLOCK RATE

The 100% tested maximum clock rate of 8.47mHz for the PCM60P is derived by multiplying the standard audio sample rate of 44.1kHz times eight (4X oversampling times two channels) times the standard audio word bit length of 24 (44.1kHz x 4 x 2 x 24 = 8.47mHz). Note that this clock rate accommodates a 24-bit word length, even though only 16 bits are actually being used.

"STOPPED-CLOCK" OPERATION

The PCM60P is normally operated with a continuous clock input signal. If the clock is to be stopped in between input data words, the last 16-bits shifted in are not actually shifted from the serial register to the latched parallel DAC register until the first clock after the one used to input bit 16 (LSB). This means the data is not shifted into the DHC latch until the start of the next 16-bit data word input unless at least one additional clock accompanies the 16 used to serially shift in data in the first place. In either case, the setup and hold times for DATA, WDCLK, and LRCLK must still be observed.

INSTALLATION

The PCM60P only requires a single +5V supply. The +5V supply, however, is used in deriving the internal reference. It is therefore very important that this supply be as "clean" as possible to reduce coupling of supply noise to the outputs. If a good analog supply is available at greater than +5V, a zener diode can be used to obtain a stable +5V supply. A 100µF decoupling capacitor as shown in Figure 3 should be used regardless of how good the +5V supply is to maximize power supply rejection. All grounds should be connected to the analog ground plane as close to the PCM60P as possible.

FILTER CAPACITOR REQUIREMENTS

As shown in Figure 3, CREF (P15) and VREF SEN (P17) should have decoupling capacitors of .1µF (C4) and 10µF (C5) to $+V_{CC}$ respectively with no special tolerance being required. To maximize channel separation between left and right channels, 5% 300pF capacitors (C2 and C3) between V_{COM} and left and right channel outputs are required in addition to a 5% 3µF capacitor (C1) between V_{COM} (P11) and +5V. The ratio of 10K to 1 is the important factor here for proper circuit operation. Placement of all capacitors should be as close to the appropriate pins of the PCM60P as possible to reduce noise pickup from surrounding circuitry.

APPLICATIONS

Probably the most popular use of the PCM60P is in applications requiring single power supply operation. For example, the PCM60P is ideal for automotive compact disk (CD) and digital audio tape (DAT) playback units. To use a more complex bipolar DAC requiring ±5V supplies in the +12V application for example would require driving a stable "floating" ground and regulating the +12V to +10V. The single supply CMOS PCM60P would only require a +5V zener diode to regulate its 50mW max supply. The outputs could be AC coupled to the rest of the circuit for perfectly acceptable high dynamic performance. The PCM60P is ideal in any application requiring a minimum of additional circuitry as well as ultra low-power CMOS performance.

Of course, the PCM60P is the D/A converter of choice in any application requiring very low power dissipation. Portable battery powered test and measurement equipment requiring very low distortion digital to analog converters would be ideal applications for the CMOS PCM60P with its 50mW max power dissipation.

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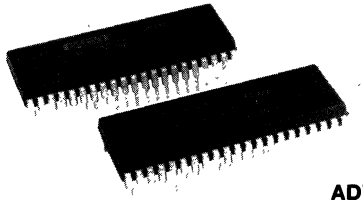


PCM64P

ADVANCE INFORMATION
Subject to Change

18-Bit Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 18-BIT MONOLITHIC AUDIO D/A CONVERTER
- LOW −96dB MAX THD+N AT FS (16-BIT LINEARITY WITH EXTERNAL ADJUST)
- VERY FAST SETTLING CURRENT OUTPUT (200ns)
- PARALLEL INPUTS, 42-PIN PLASTIC "SHRINK" DIP
- USER PROVIDES 10V REFERENCE AND OP AMP TO OPTIMIZE COST EFFECTIVENESS
- −15V, +5V SUPPLIES, 415mW POWER DISSIPATION

APPLICATIONS

- HIGH ACCURACY DIRECT DIGITAL WAVEFORM SYNTHESIS
- PROFESSIONAL AND HIGH END DIGITAL AUDIO

DESCRIPTION

The PCM64JP/KP is a precision 18-bit digital-to-analog converter that features 16-bit linearity and ultra low distortion over a very wide frequency range. It is based on the highly accurate and stable 18-bit DAC729. The PCM64P greatly reduces cost by allowing the user to supply an external reference and current-to-voltage converter. This enables optimum cost/performance designs to be achieved when the very good temperature drift and stability specifications of the DAC729 are not necessarily required.

The PCM64P comes in a 42-pin double-wide plastic "shrink" DIP package. Applications include very low distortion frequency synthesis and very high end consumer and professional digital audio applications.

International Airport Industrial Park • P.O. Box 11400 • Tucson, Arizona 85734 • Tel.: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491

PDS-786

SPECIFICATIONS

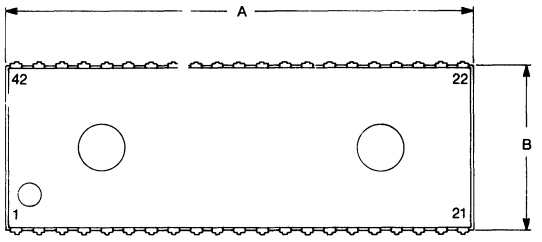
ELECTRICAL

All specifications at +25°C, $+V_{DD}$ = +5.00V, and $-V_{CC}$ = −15.0V unless otherwise noted

PARAMETER	CONDITIONS	PCM64P MIN	PCM64P TYP	PCM64P MAX	UNITS
RESOLUTION				18	Bits
DYNAMIC RANGE			108		dB
INPUT					
DIGITAL INPUT					
Logic Family			TTL Compatible		
Logic Level V_{IH}	I_{IH} = +10µA	+2.4		+5.25	V
V_{IL}	I_{IL} = −300µA	0.0		+0.8	V
Data Format			Parallel CSB, COB, CTC[1]		
DYNAMIC CHARACTERISTICS					
TOTAL HARMONIC DISTORTION + NOISE[2]	F_S = 176.4kHz with external bits 1-4 adjust[3]				
F = 991Hz (0dB)			−100	−96	dB
F = 991Hz (−20dB)			−86	−82	dB
F = 991Hz (−60dB)			−46	−42	dB
TOTAL HARMONIC DISTORTION + NOISE	F_S = 176.4kHz without external bits adjust				
F = 991Hz (0dB)			−96	−93	dB
F = 991Hz (−20dB)			−78	−76	dB
F = 991Hz (−60dB)			−38	−36	dB
NOISE	20Hz to 20kHz at bipolar zero			3	nArms
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error				±0.5	%
Bipolar Zero Error				±6.0	µA
DRIFT					
Gain	0°C to +70°C		±10		ppm/°C
Bipolar Zero	0°C to +70°C		±2		ppm of FSR/°C
POWER SUPPLY SENSITIVITY					
$+V_{CC}$			±0.003		%FSR/%V_{CC}
$-V_{CC}$			±0.003		%FSR/%V_{CC}
$+V_{DD}$			±0.001		%FSR/%V_{DD}
WARM-UP TIME				1	minute
OUTPUT					
ANALOG OUTPUT					
Output Range[4]		−1.00		+1.00	mA
Internal $R_{FEEDBACK}$			10k, 10k, 5k, 5k		Ω
Output Impedance			3.0		kΩ
SETTLING TIME					
1mA Step	10Ω to 100Ω load		200		ns
REFERENCE REQUIREMENTS					
REFERENCE INPUT					
Input Voltage		9.9	10	10.1	V
Input Current	Unipolar			1	mA
Input Current	Bipolar			2	mA
POWER SUPPLY REQUIREMENTS					
Voltage Range $-V_{CC}$		−14.5		−15.5	V
$+V_{DD}$		+4.75		+5.25	V
Current $-V_{CC}$			−22		mA
$+V_{DD}$			+17		mA
Power Dissipation	$-V_{CC}$ = −15V, V_{DD} = +5V		415		mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Storage		−50		+100	°C

NOTES (1) CTC code requires external inversion of MSB bit input (2) Ratio of Distortion rms + Noise rms/Signal rms (3) F_S = Sample rate of DAC (4 × 44.1kHz) (4) Tolerance of I_{OUT} and $R_{FEEDBACK}$ is approximately ±1%

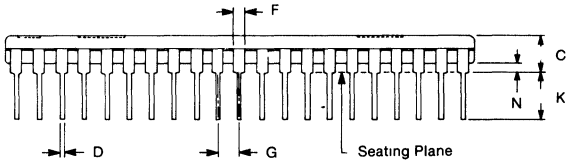
MECHANICAL

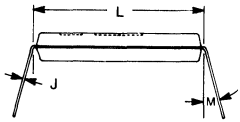


NOTE Leads in true position within 0 01" (0 25mm) R at MMC at seating plane.

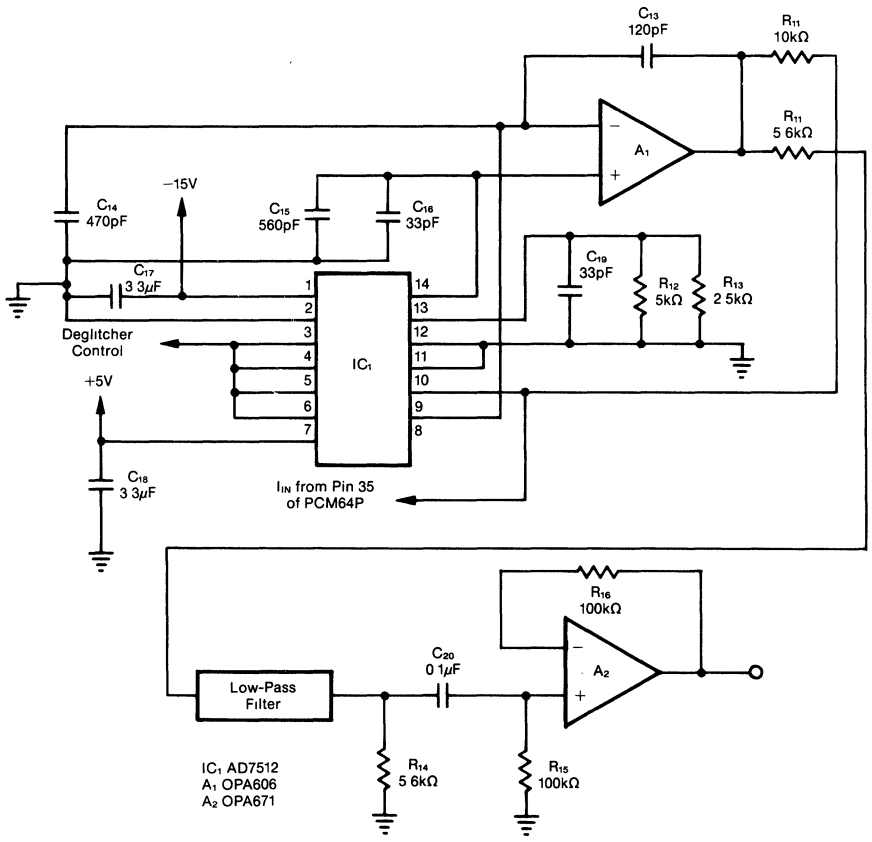
Pin numbers shown for reference only Numbers may not be marked on package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		1 520		38 60
B		575		14 60
C		200		5 10
D	0165	023	0 38	0 58
F	039 TYP		1 00 TYP	
G	070 BASIC		1 78 BASIC	
J	007	014	0 18	0 36
K	1 00		2 54	
L	600 TYP		15 24 TYP	
M	0°C	15°C	0°C	15°C
N	020		0 51	

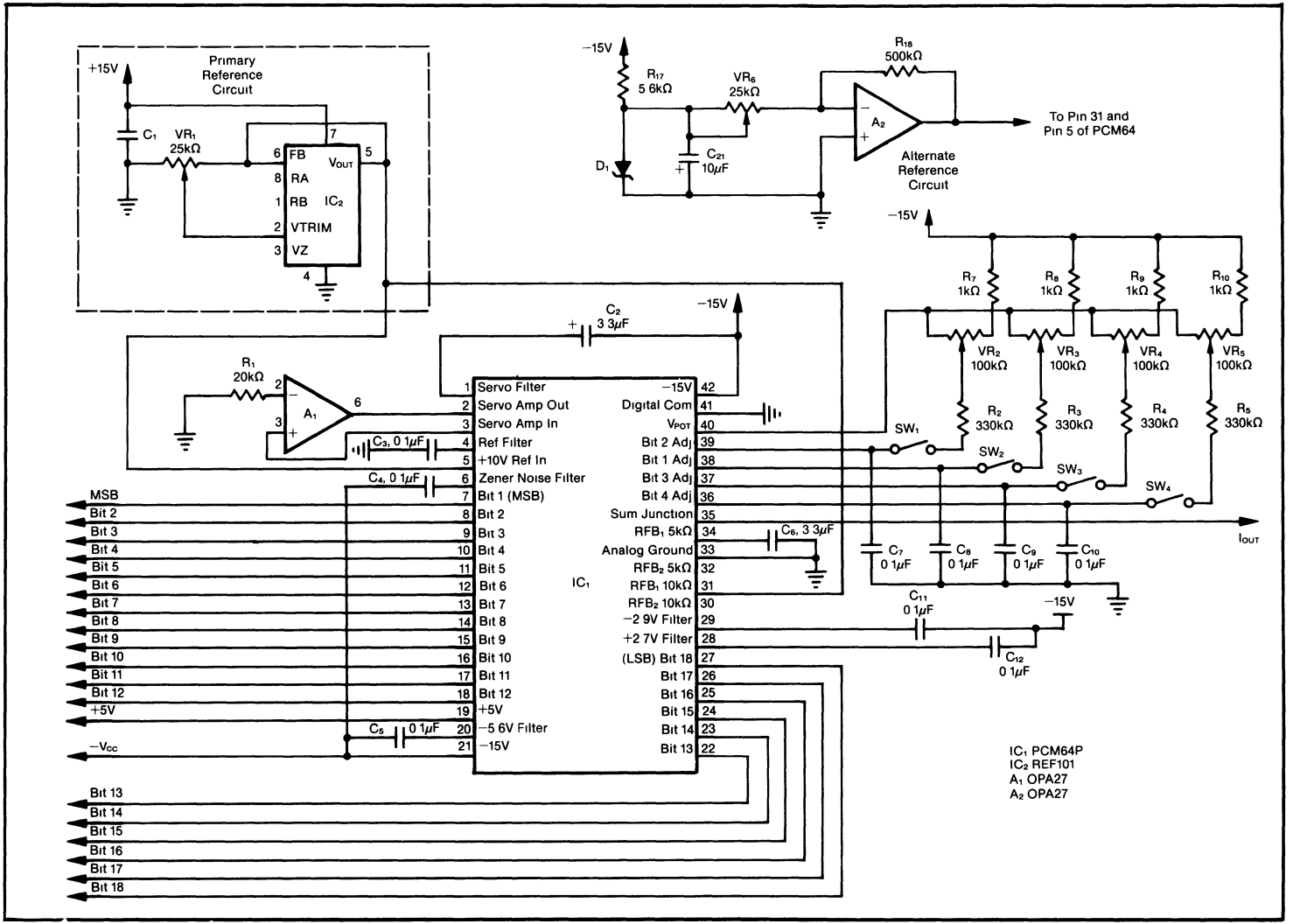


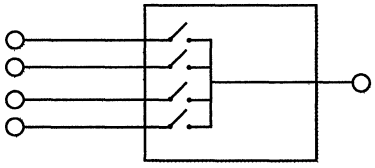


OUTPUT DEGLITCHING CIRCUITRY



CONNECTION DIAGRAM





ANALOG MULTIPLEXERS

Use Burr-Brown analog multiplexers to realize a very low cost-per-channel solution to multiple-channel data conversion or analog distribution systems designs. Two types are offered—a low-cost, high-quality family of devices ranging from 4 to 16 channels that can accommodate either single-ended or differential signals, and a very fast switching family, single-ended or differential, for high-throughput rate applications. All are TTL- and CMOS-compatible, have input protection in excess of the maximum power supply voltages, and can be operated singly or in multi-tiered matrices.

7

ANALOG MULTIPLEXERS SELECTION GUIDE

The Selection Guide shows parameters for all grades. Refer to the Product Data Sheet for additional information. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book*.

ANALOG MULTIPLEXERS — **Boldface = NEW**

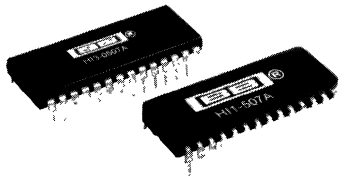
Description	Model	Channels	Input Range (V)	On Resistance max (Ω)	Settling Time (to 0.01%)	Temp Range[1]	Pkg[2]	Page
Protected Inputs	**HI3-0506A-5**	**16-channel single ended**	**±15**	**1.8k**	**3.5µs**	**Com**	**28-p PDIP**	**7-3**
	HI1-0506A-5	**16-channel single ended**	**±15**	**1.8k**	**3.5µs**	**Com**	**28-p CDIP**	**7-3**
	HI1-0506A-2	**16-channel single ended**	**±15**	**1.5k**	**3.5µs**	**Mil**	**28-p CDIP**	**7-3**
	HI3-0507A-5	**8-channel differential**	**±15**	**1.8k**	**3.5µs**	**Com**	**28-p PDIP**	**7-3**
	HI1-0507A-5	**8-channel differential**	**±15**	**1.8k**	**3.5µs**	**Com**	**28-p CDIP**	**7-3**
	HI1-0507A-2	**8-channel differential**	**±15**	**1.5k**	**3.5µs**	**Mil**	**28-p CDIP**	**7-3**
	HI3-0508A-5	**8-channel single ended**	**±15**	**1.8k**	**3.5µs**	**Com**	**16-p PDIP**	**7-13**
	HI1-0508A-5	**8-channel single ended**	**±15**	**1.8k**	**3.5µs**	**Com**	**16-p CDIP**	**7-13**
	HI1-0508A-2	**8-channel single ended**	**±15**	**1.5k**	**3.5µs**	**Mil**	**16-p CDIP**	**7-13**
	HI3-0509A-5	**4-channel differential**	**±15**	**1.8k**	**3.5µs**	**Com**	**16-p PDIP**	**7-13**
	HI1-0509A-5	**4-channel differential**	**±15**	**1.8k**	**3.5µs**	**Com**	**16-p CDIP**	**7-13**
	HI1-0509A-2	**4-channel differential**	**±15**	**1.5k**	**3.5µs**	**Mil**	**16-p CDIP**	**7-13**
High Speed	MPC800KG	16 single or 8 differential	±15	750	800ns	Com	CDIP	7-23
	MPC800SG	16 single or 8 differential	±15	750	800ns	Mil	CDIP	7-23
	MPC801KG	8 single or 4 differential	±15	750	800ns	Com	CDIP	7-30
	MPC801SG	8 single or 4 differential	±15	750	800ns	Mil	CDIP	7-30

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Mil = –55°C to +125°C. (2) CDIP = Ceramic DIP, PDIP = Plastic DIP.

MODELS STILL AVAILABLE BUT NOT FEATURED IN THIS BOOK

MPC16S
MPC4D
MPC8S
MPC8D

BURR-BROWN®



HI-506A
HI-507A

MILITARY & DIE VERSIONS AVAILABLE

Single-Ended 16-Channel/Differential 8-Channel CMOS ANALOG MULTIPLEXERS

FEATURES

- ANALOG OVERVOLTAGE PROTECTION: 70Vp-p
- NO CHANNEL INTERACTION DURING OVERVOLTAGE
- ESD RESISTANT
- BREAK-BEFORE-MAKE SWITCHING
- ANALOG SIGNAL RANGE: ±15V
- STANDBY POWER: 7.5mW typ
- TRUE SECOND SOURCE

DESCRIPTION

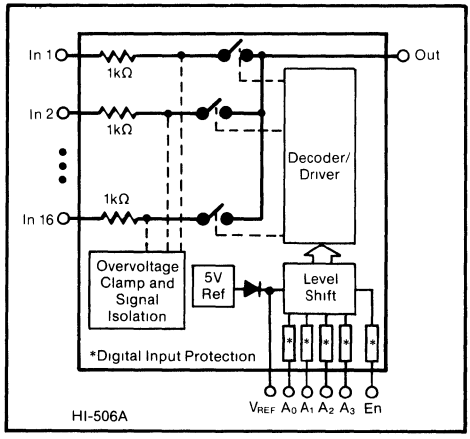
The HI-506A is a 16-channel single-ended analog multiplexer and the HI-507A is an 8-channel differential multiplexer.

The HI-506A and HI-507A multiplexers have input overvoltage protection. Analog input voltages may exceed either power supply voltage without damaging the device or disturbing the signal path of other channels. The protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand 70Vp-p signal levels and standard ESD tests. Signal sources are protected from short circuits should multiplexer power loss occur; each input presents a 1kΩ resistance under this condition. Digital inputs can also sustain continuous faults up to 4V greater than either supply voltage.

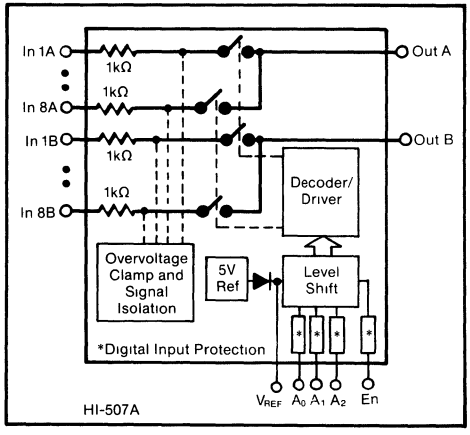
These features make the HI-506A and HI-507A ideal for use in systems where the analog signals orginate from external equipment or separately powered sources.

The HI-506A and HI-507A are fabricated with Burr-Brown's dielectrically isolated CMOS technology. The multiplexers are available in a hermetic ceramic DIP or plastic DIP. Commercial (0°C to +75°C) and military (−55°C to +125°C) versions are available.

FUNCTIONAL DIAGRAMS



HI-506A



HI-507A

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx 910-952-1111 - Cable BBRCORP - Telex 66-6491

PDS-774A

SPECIFICATIONS

ELECTRICAL

Supplies = +15V, −15V, V_{REF} (Pin 13) = Open, V_{AH} (Logic Level High) = +4 0V, V_{AL} (Logic Level Low) = +0.8V unless otherwise specified.

PARAMETER	TEMP	HI-506A-2/HI-507A-2 MIN	HI-506A-2/HI-507A-2 TYP	HI-506A-2/HI-507A-2 MAX	HI-506A-5/HI-507A-5 MIN	HI-506A-5/HI-507A-5 TYP	HI-506A-5/HI-507A-5 MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range	Full	−15		+15	−15		+15	V
R_{ON}, On Resistance[1]	+25°C		1 2	1 5		1 5	1 8	kΩ
	Full		1 5	1 8		1 8	2 0	kΩ
I_S (OFF), Off Input Leakage Current	+25°C		0 03			0 03		nA
	Full			50			50	nA
I_D (OFF), Off Output Leakage Current	+25°C		0 1			0 1		nA
HI-506A	Full			300			300	nA
HI-507A	Full			200			200	nA
I_D (OFF) with Input Overvoltage Applied[2]	+25°C		4 0			4 0		nA
	Full			2 0				μA
I_D (ON), On Channel Leakage Current	+25°C		0 1			0 1		nA
HI-506A	Full			300			300	nA
HI-507A	Full			200			200	nA
I_{DIFF} Differential Off Output Leakage Current (HI-507A Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold TTL Drive	Full			0 8			0 8	V
V_{AH}, Input High Threshold[3]	Full	4 0			4 0			V
V_{AL} MOS Drive [4]	+25°C			0 8			0 8	V
V_{AH}	+25°C	6 0			6 0			V
I_A, Input Leakage Current (High or Low)[5]	Full			1 0			1 0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0 5			0 5		μs
	Full			1 0			1 0	μs
t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0 1%)	+25°C		1 2			1 2		μs
(0 01%)	+25°C		3 5			3 5		μs
"OFF Isolation"[6]	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-506A	+25°C		50			50		pF
HI-507A	+25°C		25			25		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0 1			0 1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7 5			7 5		mW
I+, Current Pin 1[7]	Full		0 5	2 0		0 5	2 0	mA
I−, Current Pin 27[7]	Full		0 02	1 0		0 02	1 0	mA

NOTES (1) V_{OUT} = ±10V, I_{OUT} = −100μA (2) Analog overvoltage = ±33V (3) To drive from DTL/TTL circuits 1kΩ pull-up resistors to +5 0V supply are recommended (4) V_{REF} = +10V (5) Digital input leakage is primarily due to the clamp diodes Typical leakage is less than 1nA at 25°C (6) V_{EN} = 0 8V, R_L = 1kΩ, C_L = 15pF, V_S = 7Vrms, f = 100kHz Worst-case isolation occurs on channel 4 due to proximity of the output pins (7) V_{EN}, V_A = 0V or 4 0V

TRUTH TABLES

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

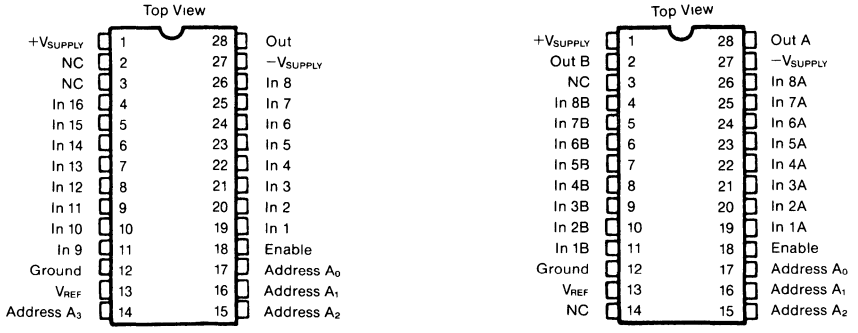
A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

ABSOLUTE MAXIMUM RATINGS[1]

Voltage between supply pins 44V
V_{REF} to ground, V+ to ground 22V
V− to ground 25V
Digital input overvoltage
V_{EN}, V_A $V_{SUPPLY}(+)$ ..... +4V
$V_{SUPPLY}(-)$ ..... −4V
or 20mA, whichever occurs first
Analog input overvoltage
V_S $V_{SUPPLY}(+)$ ..... +20V
$V_{SUPPLY}(+)$ ..... −20V
Continuous current, S or D 20mA
Peak current, S or D
(pulsed at 1ms, 10% duty cycle max) 40mA
Power dissipation* 2 0W
Operating temperature range
HI-506A/507A-2 ..... −55°C to +125°C
HI-506A/507A-5 ..... 0°C to +75°C
Storage temperature range ..... −65°C to +150°C
*Derate 20 0mW/°C above T_A = +75°C

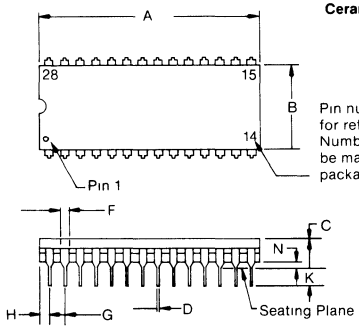
NOTES 1 Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired Functional operation under any of these conditions is not necessarily implied

PIN CONFIGURATIONS



MECHANICALS

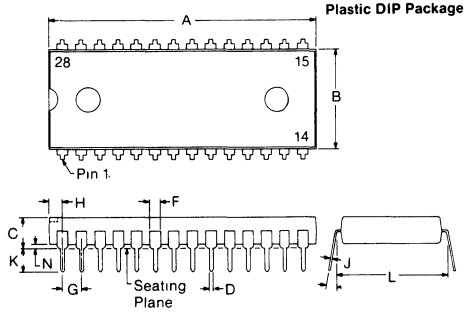
Ceramic DIP Package



NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 360	1 470	34 54	37 34
B	500	550	12 70	13 97
C	—	200	—	5 08
D	015	021	0 38	0 53
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	030	095	0 76	2 41
J	007	013	0 18	0 33
K	100	—	2 54	—
L	600 BASIC		15 24 BASIC	
M	—	15°	—	15°
N	020	090	0 51	2 29

Plastic DIP Package



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 350	1 450	34 29	36 83
B	520	575	13 21	14 61
C	169	224	4 29	5 70
D	015	023	0 38	0 58
F	043	062	1 09	1 57
G	100 BASIC		2 54 BASIC	
H	030	090	0 76	2 29
J	008	015	0 20	0 38
K	100	150	2 54	3 81
L	600 BASIC		15 24 BASIC	
M	0°	15°	0°	15°
N	018	040	0 46	1 02

NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

Pin numbers are shown for reference only numbers may not be marked on package

CASE Plastic
MATING CONNECTOR 2803MC
WEIGHT 4 3 grams (0 15oz)

ORDERING INFORMATION

Model	Package	Temperature Range	Description
HI3-0506A-5	28-Pin Plastic DIP	0°C to +75°C	16-Channel Single-Ended
HI1-0506A-5	28-Pin Ceramic DIP	0°C to +75°C	16-Channel Single-Ended
HI1-0506A-2	28-Pin Ceramic DIP	−55°C to +125°C	16-Channel Single-Ended
HI3-0507A-5	28-Pin Plastic DIP	0°C to +75°C	8-Channel Differential
HI1-0507A-5	28-Pin Ceramic DIP	0°C to +75°C	8-Channel Differential
HI1-0507A-2	28-Pin Ceramic DIP	−55°C to +125°C	8-Channel Differential

BURN-IN SCREENING OPTION
See text for details

Model	Package	Temperature Range	Burn-In Temp. (160 Hours)(1)
HI3-0506A-5-BI	28-Pin Plastic DIP	0°C to +75°C	+85°C
HI1-0506A-5-BI	28-Pin Ceramic DIP	0°C to +75°C	+125°C
HI1-0506A-2-BI	28-Pin Ceramic DIP	−55°C to +125°C	+125°C
HI3-0507A-5-BI	28-Pin Plastic DIP	0°C to +75°C	+85°C
HI1-0507A-5-BI	28-Pin Ceramic DIP	0°C to +75°C	+125°C
HI1-0507A-2-BI	28-Pin Ceramic DIP	−55°C to +125°C	+125°C

NOTE (1) Or equivalent combination of time and temperature

DISCUSSION OF PERFORMANCE

DC CHARACTERISTICS

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resisitive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of $10^8\Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000Ω source resistance will present less than 0.001% loading error and 10kΩ source resistance will increase source loading error to 0.01% with a 10^8 load impedance.

Input resistive loading errors are determined by the following relationship: (see Figure 1)

Source and Multiplexer Resistive Loading Error

$$\epsilon\ (R_S + R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where R_S = source resistance
R_L = load resistance
R_{ON} = multiplexer ON resistance

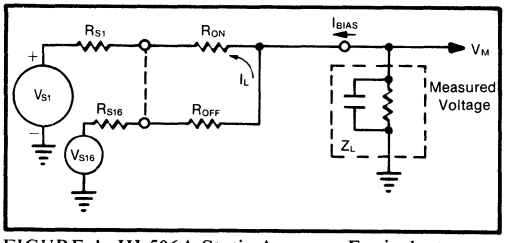


FIGURE 1. HI-506A Static Accuracy Equivalent Circuit.

Input Offset Voltage

Bias current generates an input OFFSET voltage as a result of the IR drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA will generate an offset voltage of 20μV if a 1kΩ source is used. In general, for the HI-506A, the OFFSET voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L)\ (R_{ON} + R_S)$$

where I_B = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_S = Source resistance

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full-scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differenital impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differenital errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low-level multiplexing applications.

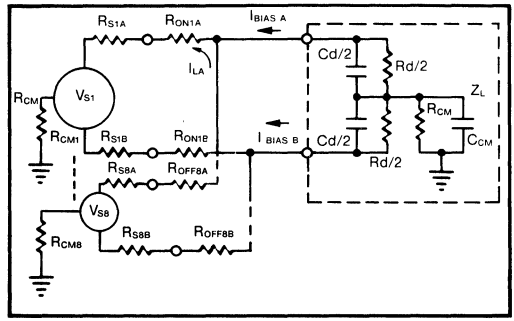


FIGURE 2. HI-507A Static Accuracy Equivalent Circuit.

Load (Output Device) Characteristics

- Use devices with very low bias current. Generally, FET input amplifiers should be used for low-level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be $10^{10}\Omega$ or higher.

Source Characteristics

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resitive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the HI-507A is used for multiplexing high-level signals of 1V to 10V full-scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

DYNAMIC CHARACTERISTICS

Settling Time

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer

Governed by the charge transfer relation $i = C\,(dV/dt)$, the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figures 3 and 4. Using this relationship, one can see that the amplitude of the switching transients seen at the source and load decrease

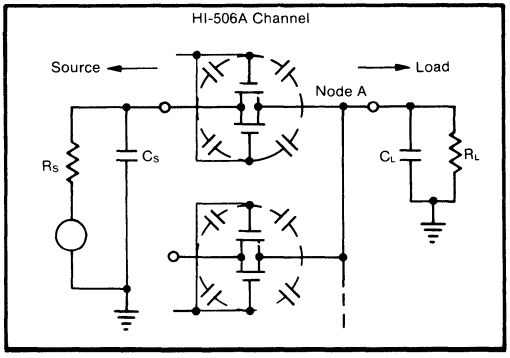


FIGURE 3. Settling Time Effects—HI-506A.

proportionally as the capacitance of the load and source increase. The tradeoff for reduced switching transient amplitude is increased settling time. In effect, the amplitude of the transients seen at the source and load are:

$$dV_L = (i/C)\,dt$$

where $i = C\,(dV/dt)$ of the CMOS FET switches
C = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in the Typical Performance Curves. This graph shows the settling time for a 20V step change on the input. The

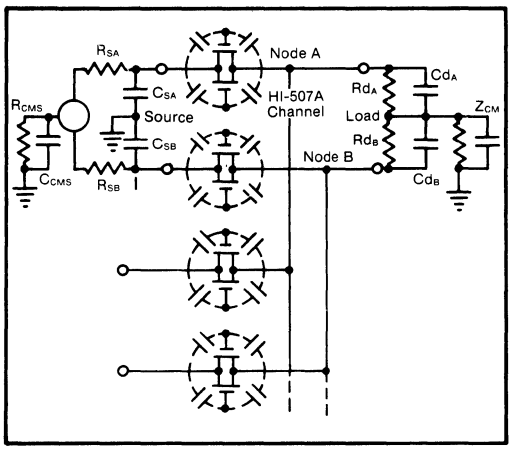


FIGURE 4. Settling and Common-Mode Effects—HI-507A.

settling time for smaller step changes on the input will be less than that shown in the curve.

Switching Time

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

Crosstalk

Crosstalk is the amount of signal feedthrough from the seven (HI-507A) or 15 (HI-506A) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance and junction capacitances in series with the R_{ON} and R_S impedances of the ON channel. Crosstalk is measured with a 20Vp-p 1000Hz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

Common-Mode Rejection (HI-507A Only)

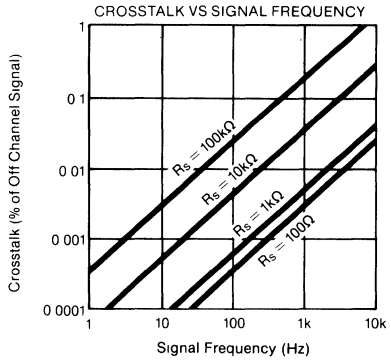
The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the HI-507A protection is provided for common-mode signals of ±20V above the power supply voltages with no damage to the analog switches.

The CMR of the HI-507A and Burr-Brown's INA110 Instrumentation Amplifier (G = 100) is 110dB at DC to 10Hz with a 6dB/octave rolloff to 70dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown INA110 Instrumentation Amplifier connected for gains of 500, 100, and 10.

Factors which will degrade multiplexer and system DC CMR are:

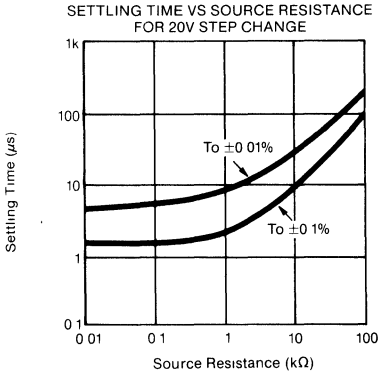
- Amplifier bias current and differential impedance mismatch
- Load impedance mismatch
- Multiplexer impedance and leakage current mismatch
- Load and source common-mode impedance

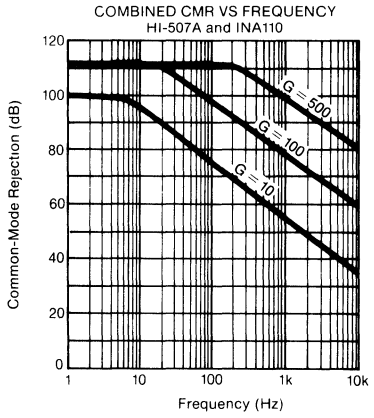
AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal ines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.



TYPICAL DYNAMIC PERFORMANCE CURVES

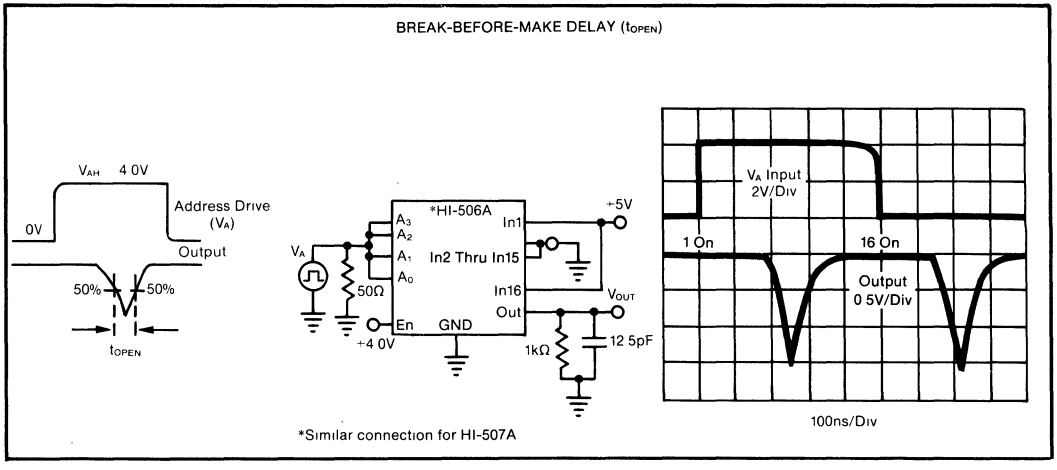
Typical at +25°C unless otherwise noted



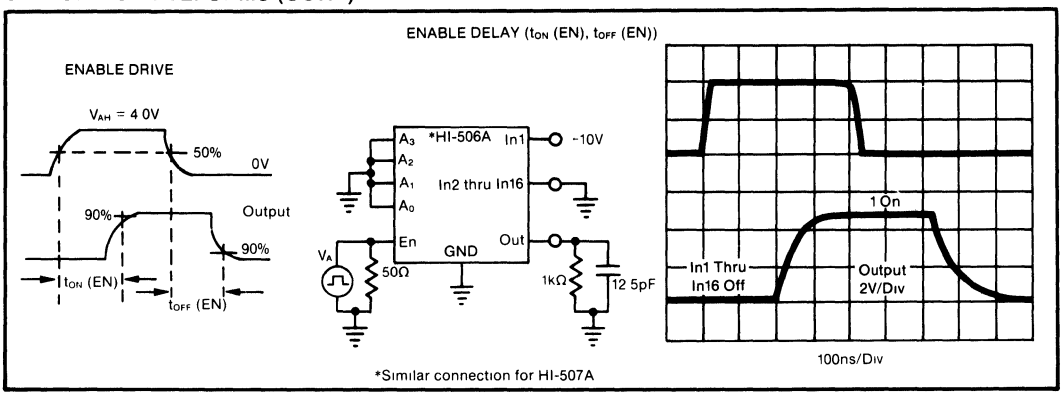


SWITCHING WAVEFORMS

Typical at +25°C unless otherwise noted

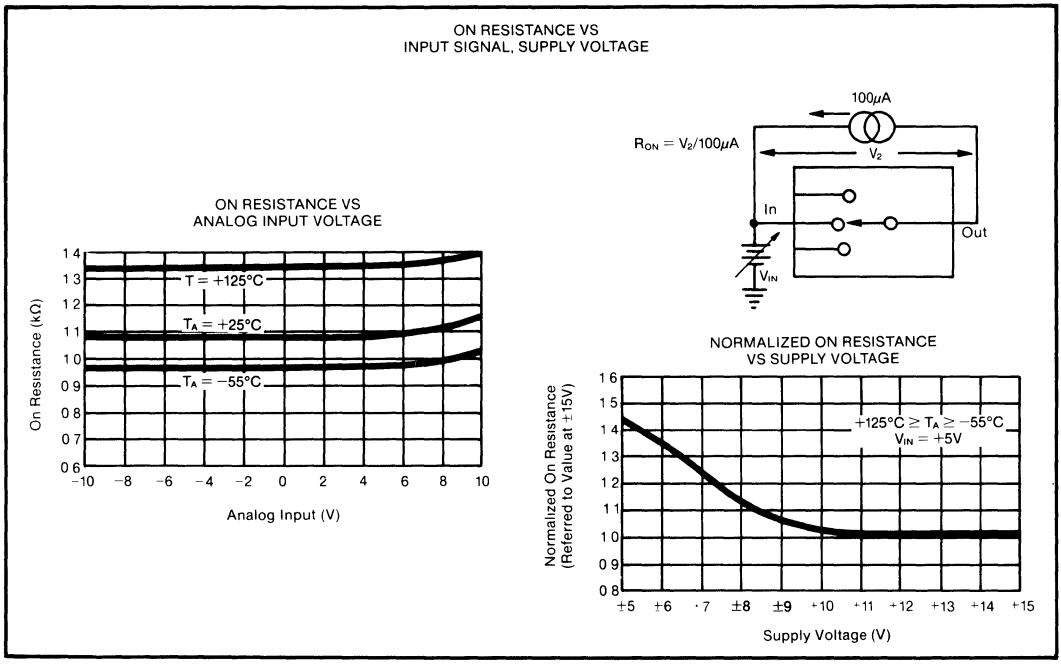


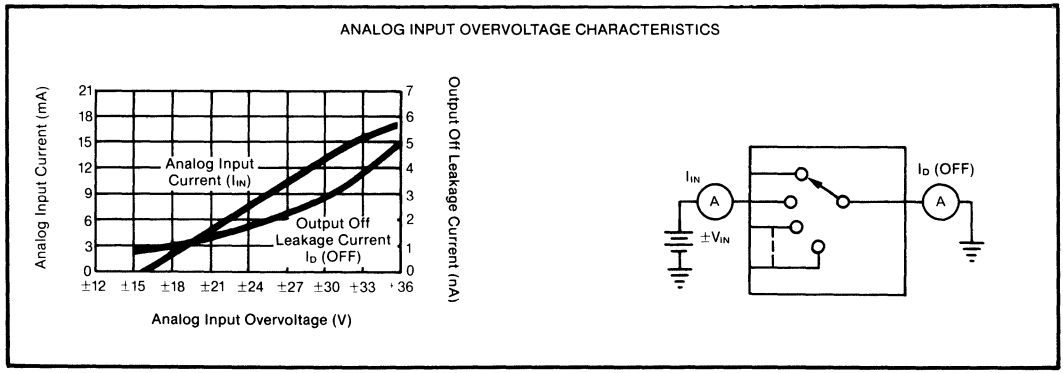
SWITCHING WAVEFORMS (CONT)



PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

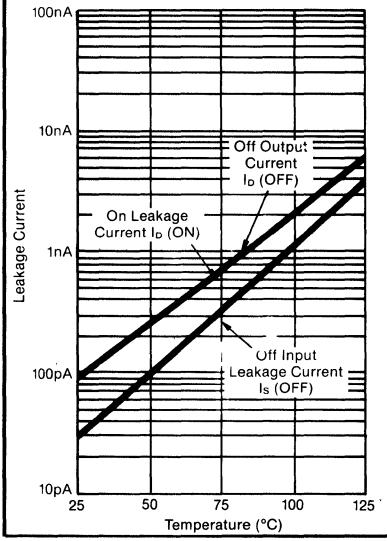
Unless otherwise specified T_A = +25°C, V_S = ±15V, V_{AH} = +4V, V_{AL} = 0.8V and V_{REF} = Open

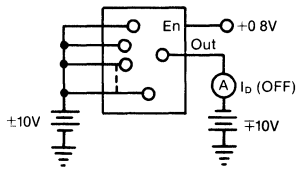




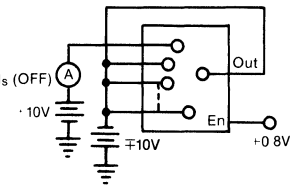
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (CONT)

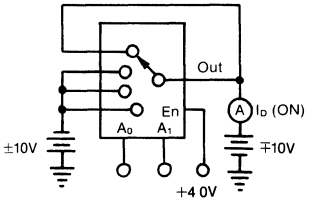
LEAKAGE CURRENT VS TEMPERATURE





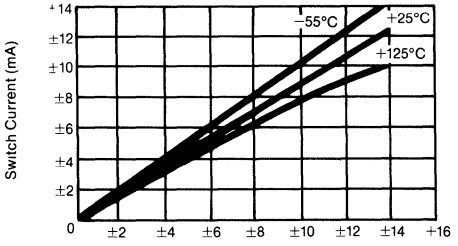
Test Circuit No 6*

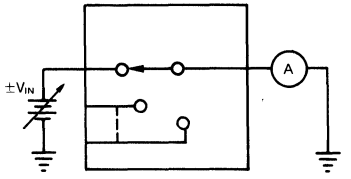




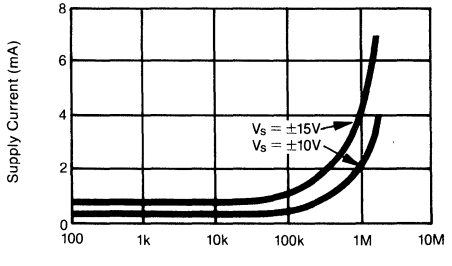
NOTE (1) Two measurements per channel +10V/−10V and −10V/+10V (Two measurements per device for I_D(OFF) +10V/−10V and −10V/+10V)

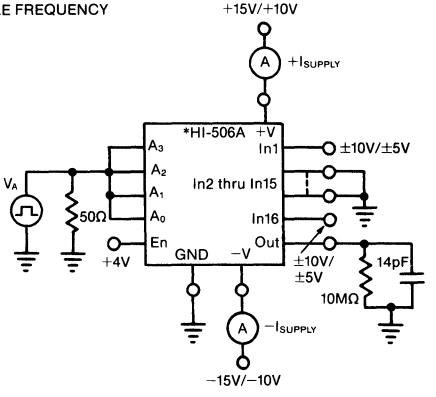
ON-CHANNEL CURRENT VS VOLTAGE



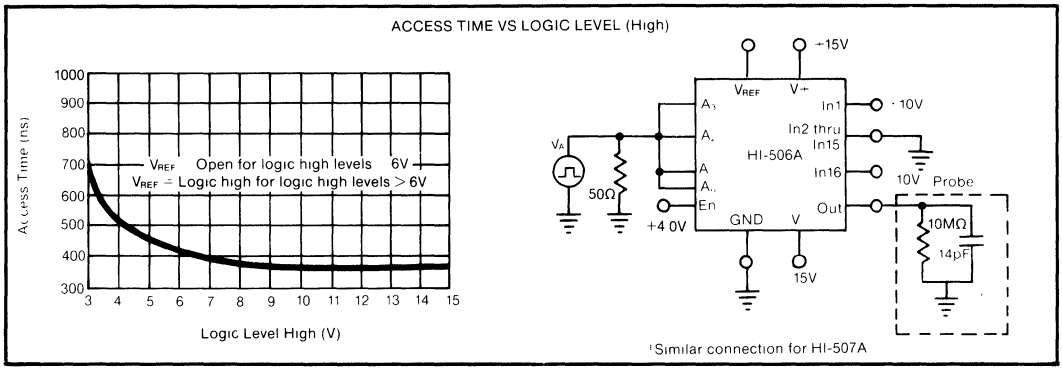


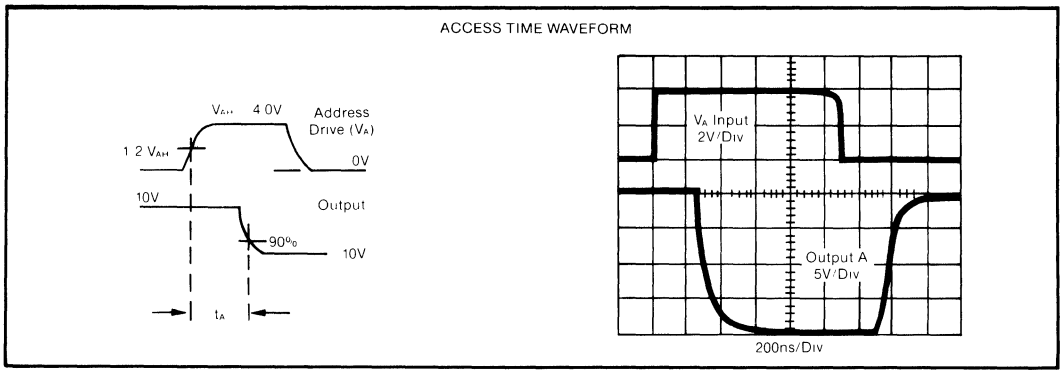
SUPPLY CURRENT VS TOGGLE FREQUENCY





*Similar connection for HI-507A





INSTALLATION AND OPERATING INSTRUCTIONS

The ENABLE input, pin 18, is included for expansion of the number of channels on a single node as illustrated in Figure 5. With ENABLE line at a logic 1, the channel is selected by the 3-bit (HI-507A) or 4-bit (HI-506A) Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to +V supply.

If the +15V and/or −15V supply voltage is absent or shorted to ground, the HI-507A and HI-506A multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded.

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull-up resistors are recommended (see Typical Performance Curves, Access Time).

To preserve common-mode rejection of the HI-507A, use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

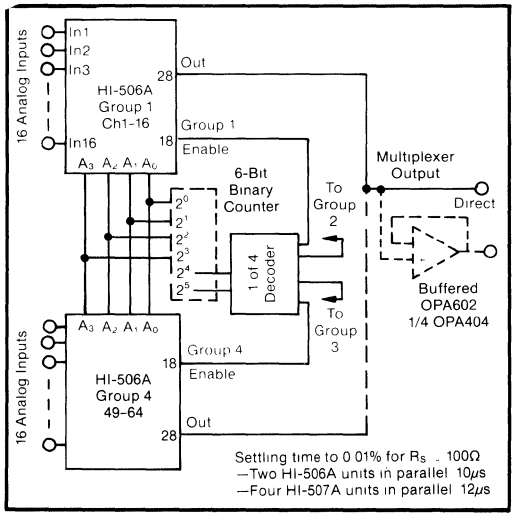


FIGURE 5. 32- to 64-Channel, Single-Tier Expansion.

CHANNEL EXPANSION

Single-Ended Multiplexer (HI-506A)

Up to 64 channels (four multiplexers) can be connected to a single node, or up to 256 channels using 17 HI-506A multiplexers on a two-tiered structure as shown in Figures 5 and 6.

Differential Multiplexer (HI-507A)

Single or multitiered configurations can be used to expand multiplexer channel capacity up to 64 channels using a 64 × 1 or an 8 × 8 configuration.

Single-Node Expansion

The 64 × 1 configuration is simply eight (HI-507A) units tied to a single node. Programming is accomplished with a 6-bit counter, using the 3LSBs of the counter to control Channel Address inputs A_0, A_1 and A_2 and the 3MSBs of the counter to drive an 8-of-1 decoder. The 8-of-1 decoder then is used to drive the ENABLE inputs (pin 18) of the HI-507A multiplexers.

Two-Tier Expansion

Using an 8 × 8 two-tier structure for expansion to 64 channels, the programming is simplified. The 6-bit counter output does not require an 8-of-1 decoder. The 3LSBs of the counter drive the A_0, A_1 and A_2 inputs of the eight first-tier multiplexers and the 3MSBs of the counter are applied to the A_0, A_1 and A_2 inputs of the second-tier multiplexer.

Single vs Multitiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced OFFSET), better CMR, and a more reliable configuration if a channel should fail ON in the single-node configuration, data cannot be taken from any channel, whereas only one channel group is failed (8 or 16) in the multitiered configuration.

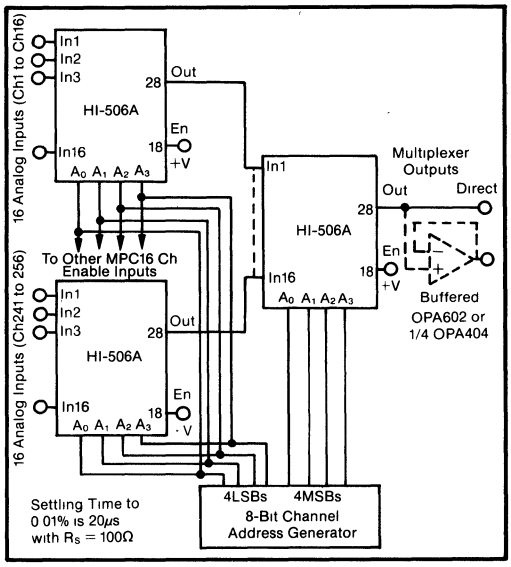


FIGURE 6. Channel Expansion Up to 256 Channels Using 16 × 16 Two-Tiered Expansion.

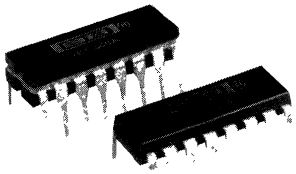
BURN-IN SCREENING

Burn-in screening is an option available for both plastic and ceramic package CMOS HI-050XA analog multiplexers. Burn-in duration is 160 hours at the temperature (or equivalent combination of time and temperature) indicated below:

Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are 100% electrically tested after burn-in is completed. To order burn-in, add "-BI" to the base model number.

BURR-BROWN®



HI-508A
HI-509A

MILITARY & DIE VERSIONS AVAILABLE

Single-Ended 8-Channel/Differential 4-Channel CMOS ANALOG MULTIPLEXERS

FEATURES

- ANALOG OVERVOLTAGE PROTECTION: 70Vp-p
- NO CHANNEL INTERACTION DURING OVERVOLTAGE
- ESD RESISTANT
- BREAK-BEFORE-MAKE SWITCHING
- ANALOG SIGNAL RANGE: ±15V
- STANDBY POWER: 7.5mW typ
- TRUE SECOND SOURCE

DESCRIPTION

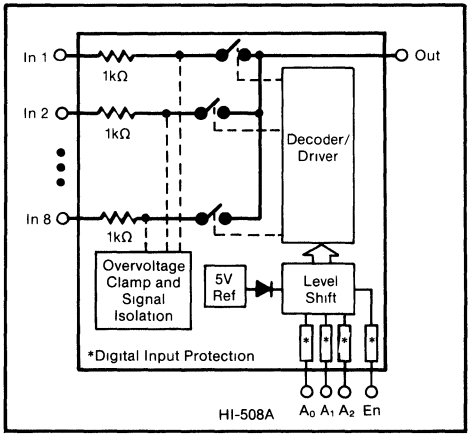
The HI-508A is an 8-channel single-ended analog multiplexer and the HI-509A is a 4-channel differential multiplexer.

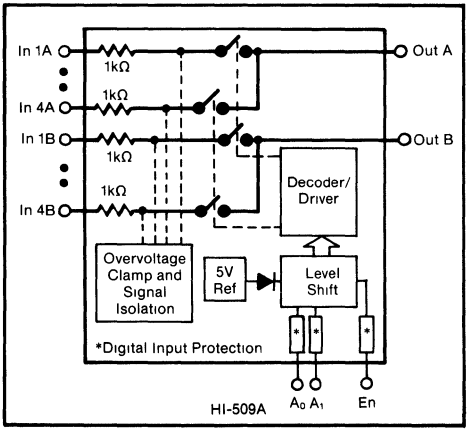
The HI-508A and HI-509A multiplexers have input overvoltage protection. Analog input voltages may exceed either power supply voltage without damaging the device or disturbing the signal path of other channels. The protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand 70Vp-p signal levels and standard ESD tests. Signal sources are protected from short circuits should multiplexer power loss occur; each input presents a 1kΩ resistance under this condition. Digital inputs can also sustain continuous faults up to 4V greater than either supply voltage.

These features make the HI-508A and HI-509A ideal for use in systems where the analog signals originate from external equipment or separately powered sources.

The HI-508A and HI-509A are fabricated with Burr-Brown's dielectrically isolated CMOS technology. The multiplexers are available in a hermetic ceramic DIP or plastic DIP. Commercial (0°C to +75°C) and military (−55°C to +125°C) versions are available.

FUNCTIONAL DIAGRAMS





International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-775A

SPECIFICATIONS

ELECTRICAL

Supplies = +15V, −15V, V_{AH} (Logic Level High) = +4 0V, V_{AL} (Logic Level Low) = +0 8V unless otherwise specified

PARAMETER	TEMP	HI-508/HI-509A-2 MIN	HI-508/HI-509A-2 TYP	HI-508/HI-509A-2 MAX	HI-508/HI-509A-5 MIN	HI-508/HI-509A-5 TYP	HI-508/HI-509A-5 MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range	Full	−15		+15	−15		+15	V
R_{ON}, On Resistance[1]	+25°C		1 2	1 5		1 5	1 8	kΩ
	Full		1 5	1 8		1 8	2 0	kΩ
I_S (OFF), Off Input Leakage Current	+25°C		0 03			0 03		nA
	Full			50			50	nA
I_D (OFF), Off Output Leakage Current	+25°C		0 1			0 1		nA
HI-508A	Full			200			200	nA
HI-509A	Full			100			100	nA
I_D (OFF) with Input Overvoltage Applied[2]	+25°C		4 0			4 0		nA
	Full			2 0				μA
I_D (ON), On Channel Leakage Current	+25°C		0 1			0 1		nA
HI-508A	Full			200			200	nA
HI-509A	Full			100			100	nA
I_{DIFF} Differential Off Output Leakage Current (HI-509A Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0 8			0 8	V
V_{AH}, Input High Threshold[3]	Full	4 0			4 0			V
I_A, Input Leakage Current (High or Low)[4]	Full			1 0			1 0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0 5			0 5		μs
	Full			1 0			1 0	μs
t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0 1%)	+25°C		1 2			1 2		μs
(0 01%)	+25°C		3 5			3 5		μs
"OFF Isolation"[5]	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-508A	+25°C		25			25		pF
HI-509A	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0 1			0 1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7 5			7 5		mW
I+, Current[6]	Full		0 5	2 0		0 5	2 0	mA
I−, Current[6]	Full		0 02	1 0		0 02	1 0	mA

NOTES (1) $V_{OUT} = \pm 10V$, $I_{OUT} = -100\mu A$ (2) Analog overvoltage = ±33V (3) To drive from DTL/TTL circuits, 1kΩ pull-up resistors to +5 0V supply are recommended (4) Digital input leakage is primarily due to the clamp diodes Typical leakage is less than 1nA at 25°C (5) $V_{EN} = 0$ 8V, $R_L = 1k\Omega$, $C_L = 15pF$, $V_S = 7Vrms$, f = 100kHz Worst-case isolation occurs on channel 4 due to proximity of the output pins (6) V_{EN}, V_A = 0V or 4 0V

TRUTH TABLES

HI-508A

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

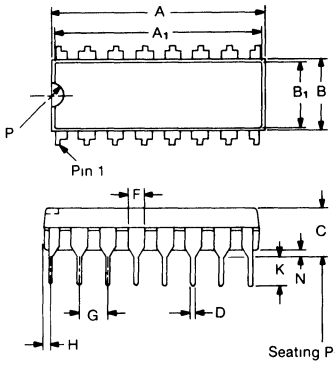
A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

ABSOLUTE MAXIMUM RATINGS[1]

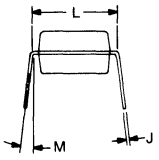
Voltage between supply pins 44V
V+ to ground 22V
V− to ground 25V
Digital input overvoltage V_{EN}, V_A V_{SUPPLY} (+) ..... +4V
V_{SUPPLY} (−) ..... −4V
or 20mA, whichever occurs first
Analog input overvoltage V_S V_{SUPPLY} (+) ..... +20V
V_{SUPPLY} (−) ..... −20V
Continuous current, S or D 20mA
Peak current, S or D (pulsed at 1ms, 10% duty cycle max) 40mA
Power dissipation* 1 28W
Operating temperature range HI-508A/509A-2 ... −55°C to +125°C
HI-508A/509A-5 ..... 0°C to +75°C
Storage temperature range ..... −65°C to +150°C
*Derate 12 8mW/°C above T_A = +75°C

NOTE (1) Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired Functional operation under any of these conditions is not necessarily implied

MECHANICAL



Plastic DIP Package

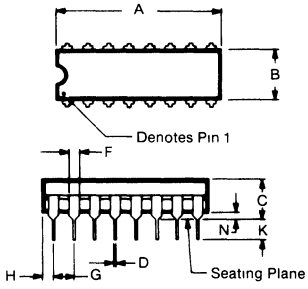


NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

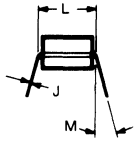
PINS Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3 2)

CASE Plastic

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	740	800	18 80	20 32
A_1	725	785	18 42	19 94
B	230	290	5 85	7 38
B_1	200	250	5 09	6 36
C	120	200	3 05	5 09
D	015	023	0 38	0 59
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	0 02	0 05	0 51	1 27
J	008	015	0 20	0 38
K	070	150	1 78	3 82
L	300 BASIC		7 63 BASIC	
M	0°	15°	0°	15°
N	010	030	0 25	0 76
P	025	050	0 64	1 27



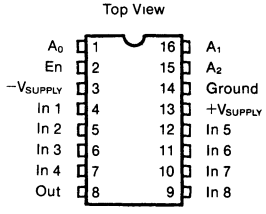
Ceramic DIP Package



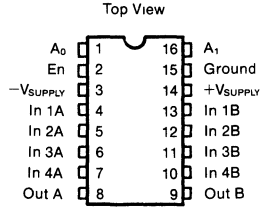
NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	760	885	19 30	22 48
B	220	280	5 59	7 11
C	—	200	—	5 08
D	015	023	0 38	0 58
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	030	095	0 76	2 41
J	008	015	0 20	0 38
K	100	—	2 54	—
L	300 BASIC		7 62 BASIC	
M	—	15°	—	15°
N	020	050	0 51	1 27

PIN CONFIGURATIONS



HI1-508A (ceramic)
HI3-508A (plastic)



HI1-509A (ceramic)
HI3-509A (plastic)

ORDERING INFORMATION

Model	Package	Temperature Range	Description
HI3-0508A-5	16-Pin Plastic DIP	0°C to +75°C	8-Channel Single-Ended
HI1-0508A-5	16-Pin Ceramic DIP	0°C to +75°C	8-Channel Single-Ended
HI1-0508A-2	16-Pin Ceramic DIP	−55°C to +125°C	8-Channel Single-Ended
HI3-0509A-5	16-Pin Plastic DIP	0°C to +75°C	4-Channel Differential
HI1-0509A-5	16-Pin Ceramic DIP	0°C to +75°C	4-Channel Differential
HI1-0509A-2	28-Pin Ceramic DIP	−55°C to +125°C	4-Channel Differential

BURN-IN SCREENING OPTION
See text for details

Model	Package	Temperature Range	Burn-In Temp. (160 Hours)(1)
HI3-0508A-5-BI	16-Pin Plastic DIP	0°C to +75°C	+85°C
HI1-0508A-5-BI	16-Pin Ceramic DIP	0°C to +75°C	+125°C
HI1-0506A-2-BI	16-Pin Ceramic DIP	−55°C to +125°C	+125°C
HI3-0509A-5-BI	16-Pin Plastic DIP	0°C to +75°C	+85°C
HI1-0509A-5-BI	16-Pin Ceramic DIP	0°C to +75°C	+125°C
HI1-0509A-2-BI	16-Pin Ceramic DIP	−55°C to +125°C	+125°C

NOTE (1) Or equivalent combination of time and temperature

DISCUSSION OF PERFORMANCE

DC CHARACTERISTICS

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resisitive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of $10^8\Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000Ω source resistance will present less than 0.001% loading error and 10kΩ source resistance will increase source loading error to 0.01% with a 10^8 load impedance.

Input resistive loading errors are determined by the following relationship: (see Figure 1)

Source and Multiplexer Resistive Loading Error

$$\epsilon\ (R_S + R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where R_S = source resistance
R_L = load resistance
R_{ON} = multiplexer ON resistance

Input Offset Voltage

Bias current generates an input OFFSET voltage as result of the IR drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA will generate an offset voltage of 20μV if a 1kΩ source is used. In general, for the HI-508A, the OFFSET voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L)(R_{ON} + R_S)$$

where I_B = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_S = Source resistance

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full-scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differenital impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differenital errors.

The effects of these errors can be minimized by following the general guidelines described in this section, especially for low-level multiplexing applications. Refer to Figure 2.

Load (Output Device) Characteristics

- Use devices with very low bias current. Generally, FET input amplifiers should be used for low-level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load Impedances, differenital and common-mode, should be $10^{10}\Omega$ or higher.

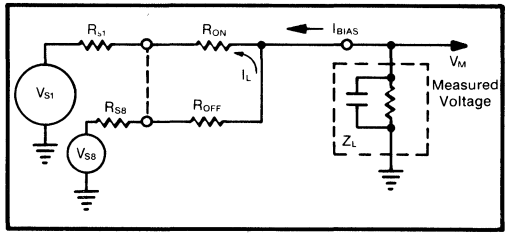


FIGURE 1. HI-508A DC Accuracy Equivalent Circuit.

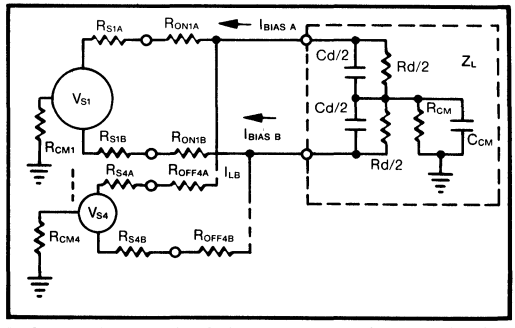


FIGURE 2. HI-509A DC Accuracy Equivalent Circuit.

Source Characteristics

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the HI-509A is used for multiplexing high-level signals of ±1V to ±10V full-scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

DYNAMIC CHARACTERISTICS

Settling Time

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer.

Governed by the charge transfer relation $i = C\,(dV/dt)$, the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figures 3 and 4. Using this relationship, one can see that the amplitude of the switching transients, seen at the source and load, decrease proportionally as the capacitance of the load and source increase. The tradeoff for reduced switching transient amplitude is increased settling time. In effect, the amplitude of the transients seen at the source and load are:

$$dV_L = (i/C)\,dt$$

where $i = C\,(dV/dt)$ of the CMOS FET switches
C = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in the Typical Performance Curves. This graph shows the settling time for a 20V step change on the input. The settling time for smaller step changes on the input will be less than that shown in the curve.

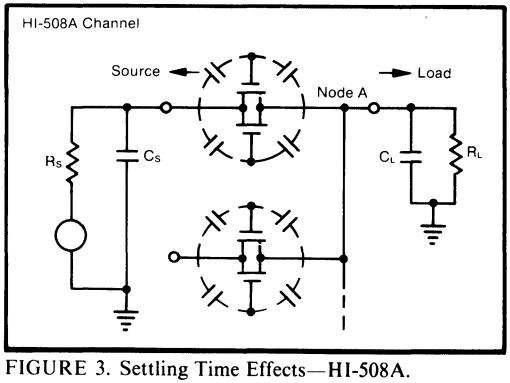


FIGURE 3. Settling Time Effects—HI-508A.

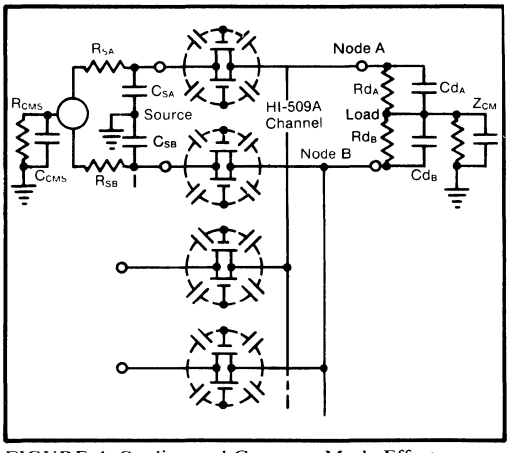


FIGURE 4. Settling and Common-Mode Effects—HI-509A.

Switching Time

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

Crosstalk

Crosstalk is the amount of signal feethrough from the three (HI-509A) or seven (HI-508A) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel OFF resistance and junction capacitances in series with the R_{ON} and R_S impedances of the ON channel. Crosstalk is measured with a 20Vp-p 1kHz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

Common-Mode Rejection (HI-509A Only)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the HI-509A, protection is provided for common-mode signals of ±20V above the power supply voltages with no damage to the analog switches.

The CMR of the HI-509A and Burr-Brown's INA110 Instrumentation Amplifier is 110dB at DC to 10Hz (G = 100) with a 6dB/octave rolloff to 70dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown model INA110 Instrumentation Amplifier connected for gains of 10, 100, and 500.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch
- Load impedance mismatch
- Multiplexer impedance and leakage current mismatch
- Load and source common-mode impedance

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer-to-amplifier wiring must be minimized. Use twisted-shielded-pair signal lines wherever possible.

BURN-IN SCREENING

Burn-in screening is an option available for both plastic and ceramic package CMOS HI-050XA analog multiplexers. Burn-in duration is 160 hours at the temperature (or equivalent combination of time and temperature) indicated below:

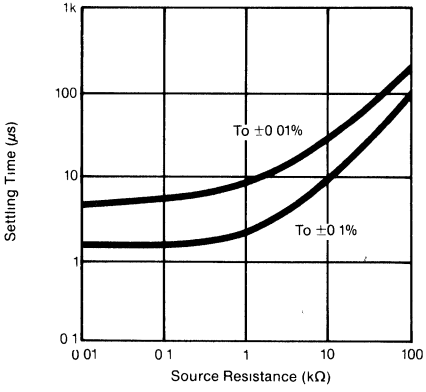
Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are 100% electrically tested after burn-in is completed. To order burn-in, add "-BI" to the base model number.

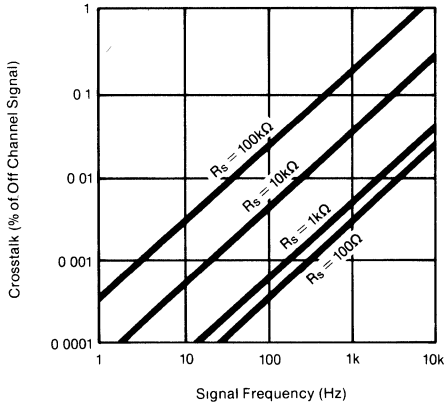
TYPICAL DYNAMIC PERFORMANCE CURVES

Typical at +25°C unless otherwise noted

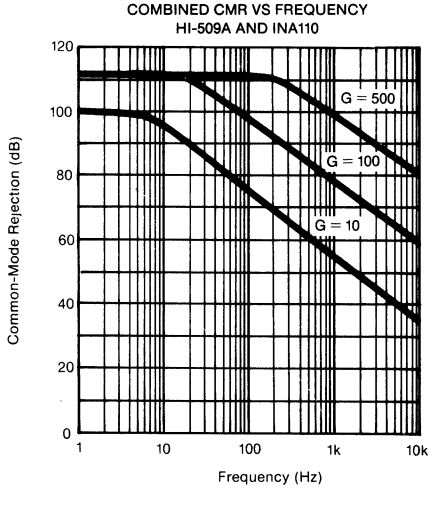
SETTLING TIME VS SOURCE RESISTANCE FOR 20V STEP CHANGE



CROSSTALK VS SIGNAL FREQUENCY



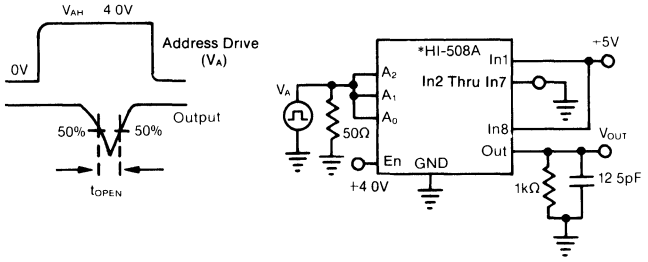
COMBINED CMR VS FREQUENCY HI-509A AND INA110



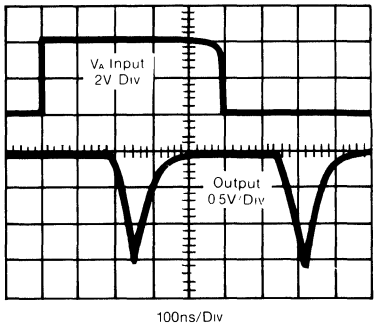
SWITCHING WAVEFORMS

Typical at +25°C unless otherwise noted

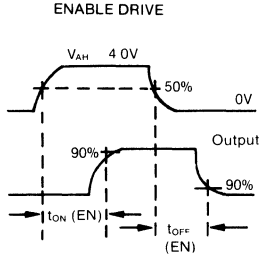
BREAK-BEFORE-MAKE DELAY (t_{OPEN})

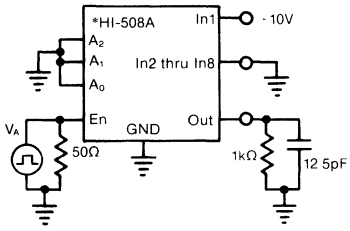


Similar connection for HI-509A

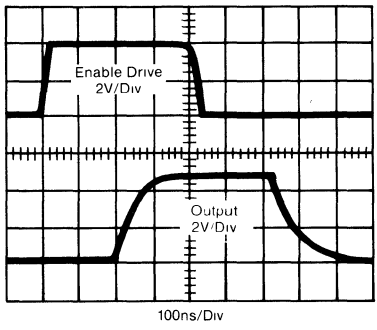


ENABLE DELAY (t_{ON} (EN), t_{OFF} (EN))





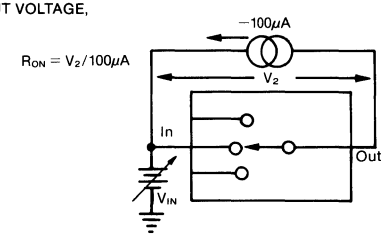
*Similar connection for HI-509A



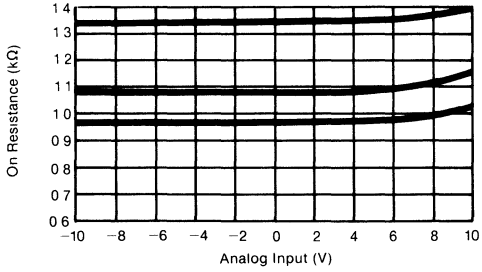
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

Unless otherwise specified $T_A = +25$, $V_S = \pm15V$, $V_{AH} = +4V$, $V_{AL} = 0\ 8V$ and V_{REF} = Open

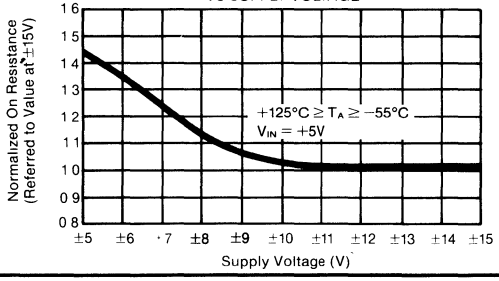
ON RESISTANCE VS ANALOG INPUT VOLTAGE, SUPPLY VOLTAGE



ON RESISTANCE VS ANALOG INPUT VOLTAGE

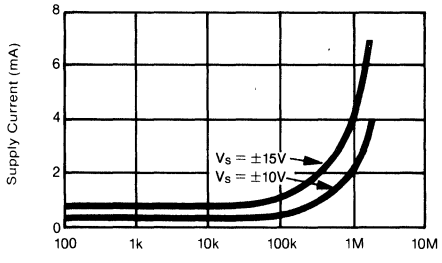


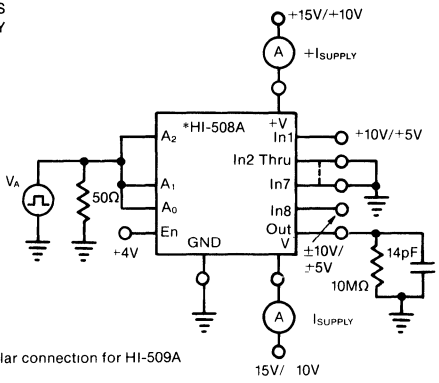
NORMALIZED ON RESISTANCE VS SUPPLY VOLTAGE



PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (CONT)

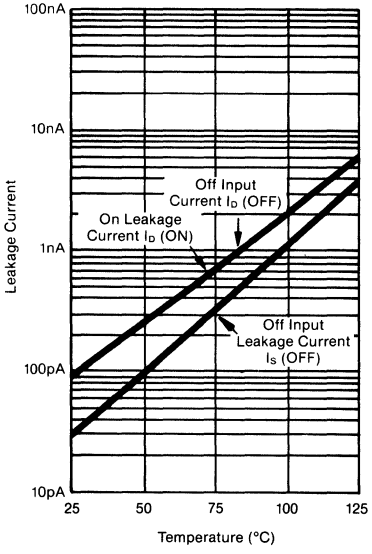
SUPPLY CURRENT VS
TOGGLE FREQUENCY

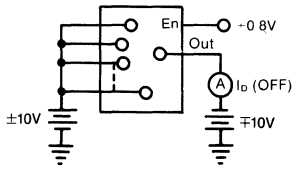


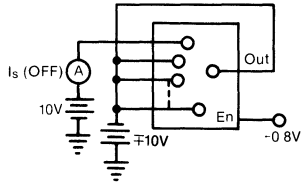


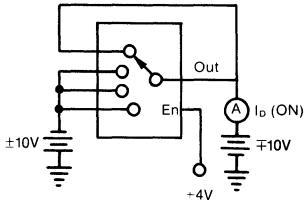
*Similar connection for HI-509A

LEAKAGE CURRENT VS
TEMPERATURE



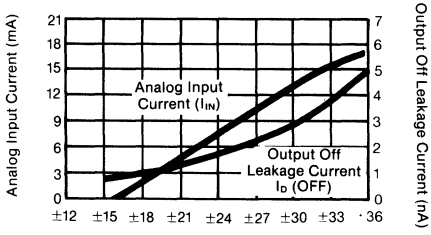


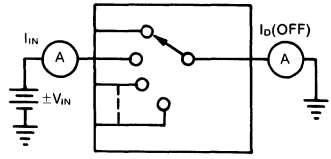




NOTE (1) Two measurements per channel +10V/−10V and −10V/+10V (Two measurements per device for I_D(OFF) +10V/−10V and −10V/+10V)

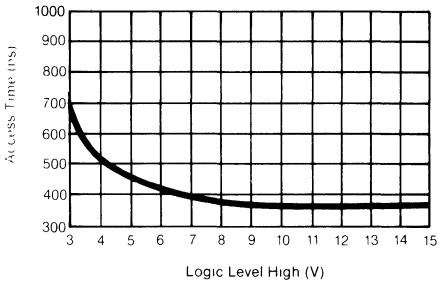
ANALOG INPUT
OVERVOLTAGE CHARACTERISTICS

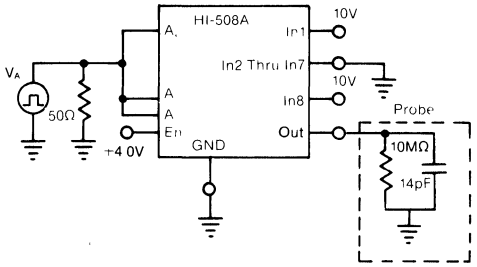




PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (CONT)

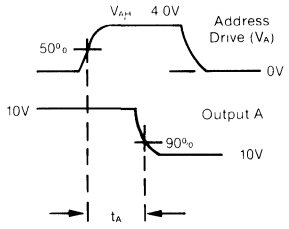
ACCESS TIME VS
LOGIC LEVEL (High)

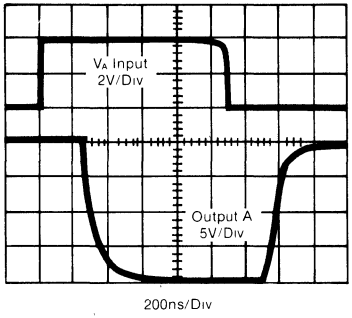




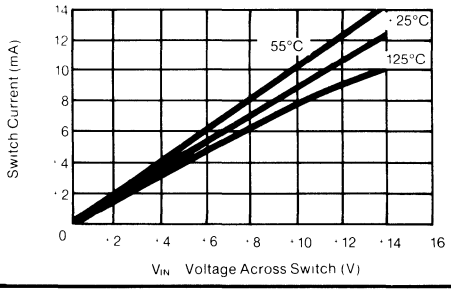
*Similar connection for HI-509A

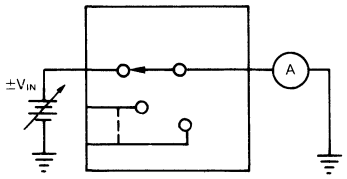
ACCESS TIME





ON-CHANNEL CURRENT
VS VOLTAGE





INSTALLATION AND OPERATING INSTRUCTIONS

The ENABLE input, pin 2, is included for expansion of the number of channels on a single node as illustrated in Figure 5. With ENABLE line at a logic 1, the channel is selected by the 2-bit (HI-509A) or 3-bit (HI-508A) Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Adddress Lines are active. If the ENABLE line is not to be used, simply tie it to $+V_{SUPPLY}$.

If the +15V and/or −15V supply voltage is absent or shorted to ground, the HI-509A and HI-508A multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded.

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull-up resistors are recommended.

To preserve common-mode rejection of the HI-509A, use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as closely as possible to system analog common or to the common-mode guard driver.

CHANNEL EXPANSION

Single-Ended Multiplexer (HI-508A)

Up to 32 channels (four multiplexers) can be connected to a single node, or up to 64 channels using nine HI-508A multiplexers on a two-tiered structure as shown in Figures 5 and 6.

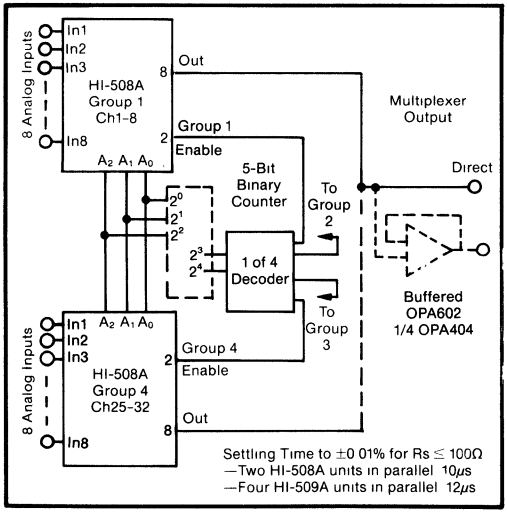


FIGURE 5. 32-Channel, Single-Tier Expansion.

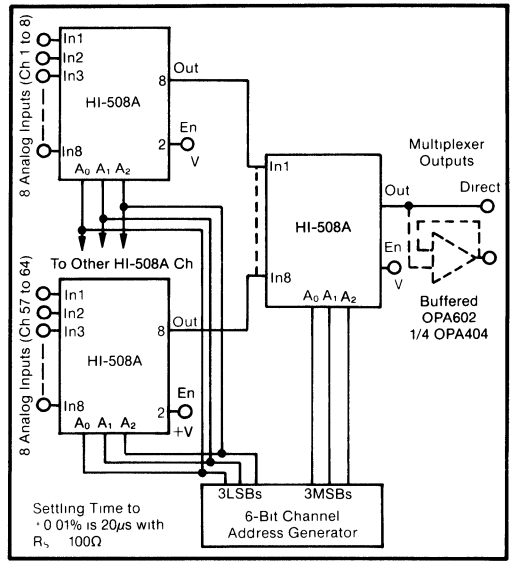


FIGURE 6. Channel Expansion Up to 64 Channels Using 8 × 8 Two-Tiered Expansion.

Differential Multiplexer (HI-509A)

Single or multitiered configurations can be used to expand multiplexer channel capacity up to 32 channels using a 32 × 1 or 16 channels using a 4 × 4 configuration.

Single-Node Expansion

The 32 × 1 configuration is simply eight (HI-509A) units tied to a single node. Programming is accomplished with a 5-bit counter, using the 2LSBs of the counter to control Channel Address inputs A_0 and A_1 and the 3MSBs of the counter to drive a 1-of-8 decoder. The 1-of-8 decoder then is used to drive the ENABLE inputs (pin 2) of the HI-509A multiplexers.

Two-Tier Expansion

Using a 4 × 4 two-tier structure for expansion to 16 channels, the programming is simplified. A 4-bit counter output does not require a 1-of-8 decoder. The 2LSBs of the counter drive the A_0 and A_1 inputs of the four first-tier multiplexers and the 2MSBs of the counter are applied to the A_0 and A_1 inputs of the second-tier multiplexer.

Single vs Multitiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced OFFSET), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single-node configuration, data cannot be taken from any channel, whereas only one channel group is failed (4 or 8) in the multitiered configuration.

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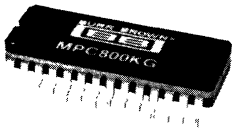
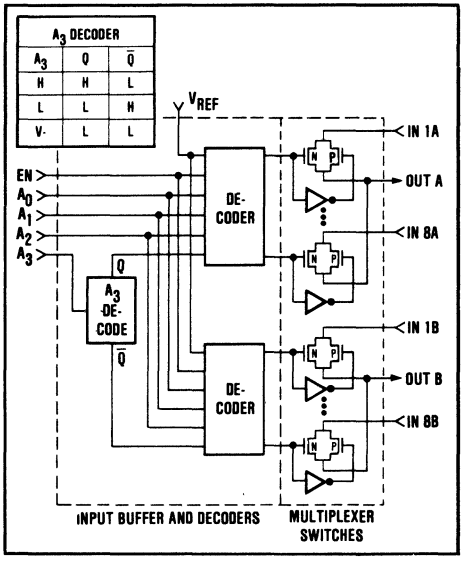


High Speed
CMOS ANALOG MULTIPLEXER

FEATURES

- HIGH SPEED
  - 100nsec access time
  - 800nsec settling to 0.01%
  - 250nsec settling to 0.1%
- USER-PROGRAMMABLE
  - 16-channel single-ended or
  - 8-channel differential
- SELECTABLE TTL or CMOS COMPATIBILITY
- WILL NOT SHORT SIGNAL SOURCES
  - Break-before-make switching
- SELF-CONTAINED WITH INTERNAL CHANNEL ADDRESS DECODER
- 28-PIN HERMETIC DUAL-IN-LINE PACKAGE



DESCRIPTION

The MPC800 is a high speed multiplexer that is user-programmable for 16-channel single-ended operation or 8-channel differential operation and for TTL or CMOS compatibility.

The MPC800 features a self-contained binary address decoder. It also has an enable line which allows the user to inhibit the entire multiplexer thereby facilitating channel expansion by adding additional multiplexers.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, low ON resistance, high OFF resistance, low feedthrough capacitance, and fast settling time.

Two models are available, the MPC800KG for operation from 0°C to +75°C and the MPC800SG for operation from -55°C to +125°C.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-463A

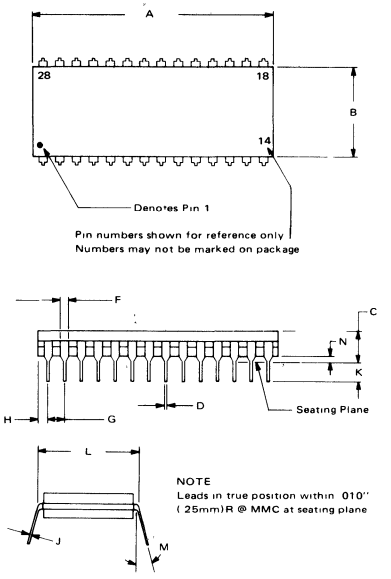
SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 15V, unless otherwise noted

MODEL	MPC800KG, MPC800SG			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT				
ANALOG INPUT				
Voltage Range	-15		+15	V
Maximum Overvoltage	-V_{CC} -2		+V_{CC}, +2	V
Number of Input Channels				
Differential	8			
Single-Ended	16			
Reference Voltage Range(1)	6		10	V
ON Characteristics(2)				
ON Resistance (R_{ON}) at +25°C		620	750	Ω
Over Temperature Range		700	1000	Ω
R_{ON} Drift vs Temperature	See Typical Performance Curves			
R_{ON} Mismatch		< 10		Ω
ON Channel Leakage		0 04		nA
Over Temperature Range		0 6	100	nA
ON Channel Leakage Drift	See Typical Performance Curves			
OFF Characteristics				
OFF Isolation		90		dB
OFF Channel Input Leakage		0 01		nA
Over Temperature Range		0 38	50	nA
OFF Channel Input Leakage Drift	See Typical Performance Curves			
OFF Channel Output Leakage		0 035		nA
Over Temperature Range		0 48	100	nA
OFF Channel Output Leakage Drift	See Typical Performance Curves			
Output Leakage (All channels disabled)(3)		0 02		nA
Output Leakage with Overvoltage				
+16V Input		< 0 35		mA
-16V Input		< 0 65		mA
DIGITAL INPUTS				
Over Temperature Range				
TTL(4)				
Logic "0" (V_{AL})			0 8	V
Logic "1" (V_{AH})	2 4			V
I_{AH}		0 05	1	μA
I_{AL}		4	25	μA
TTL Input Overvoltage	-6		6	V
CMOS				
Logic "0" (V_{AL})			0 3V_{REF}	V
Logic "1" (V_{AH})	0 7 V_{REF}			V
CMOS Input Overvoltage	-2		+V_{CC} +2	V
Address A_3 Overvoltage	-V_{CC} -2		+V_{CC} +2	V
Digital Input Capacitance		5		pF
Channel Select(5)				
Single-Ended	4-bit binary code one of 16			
Differential	3-bit binary code one of 8			
Enable	Logic "0" inhibits all channels			
POWER REQUIREMENTS				
Over Temperature Range				
Rated Supply Voltage		±15		V
Maximum Voltage Between Supply Pins			33	V
Total Power Dissipation		525		mW
Allowable Total Power Dissipation(6)			1200	mW
Supply Drain (+25°C)				
At 1MHz Switching Speed		+35, -39		mA
At 100kHz Switching Speed		+25, -29		mA
DYNAMIC CHARACTERISTICS				
Gain Error		< 0 0003		%
Cross Talk(7)	See Typical Performance Curves			
T_{OPEN} (Break before make delay)		20		nsec
Access Time at +25°C		100	150	nsec
Over Temperature Range		120	200	nsec
Settling Time(8)				
to 0 1% (20mV)		250		nsec
to 0 01% (2mV)		800		nsec
Common-Mode Rejection (Differential)				
DC		> 125		dB
60Hz		> 75		dB
Channel Input Capacitance, C_S (off)		2 5		pF
Channel Output Capacitance, C_O (off)		18		pF
Input to Output Capacitance, C_{DS} (off)		0 02		pF

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 360	1 475	34 54	37 47
B	500	550	12 70	13 97
C	---	220	-	5 59
D	015	021	0 38	0 53
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	030	095	0 76	2 41
J	007	013	0 18	0 33
K	100	- -	2 54	-
L	.600 BASIC		15 24 BASIC	
M	- -	15°		15°
N	020	090	0 51	2 29

PIN CONFIGURATION

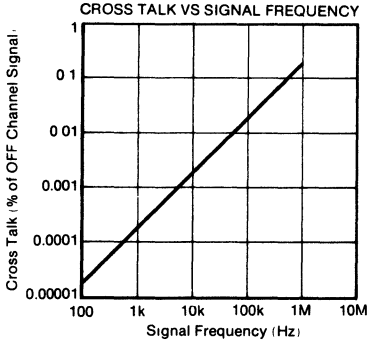
TOP VIEW

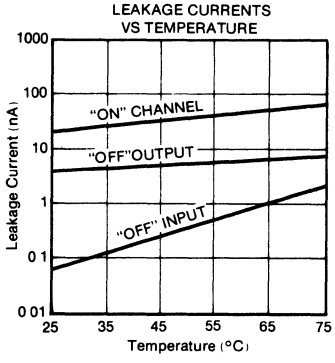
+V_{CC}	1	28	OUT A
OUT B	2	27	-V_{CC}
NC	3	26	IN 8/8A
IN16/8B	4	25	IN7/7A
IN15/7B	5	24	IN6/6A
IN14/6B	6	23	IN5/5A
IN13/5B	7	22	IN4/4A
IN12/4B	8	21	IN3/3A
IN11/3B	9	20	IN2/2A
IN10/2B	10	19	IN1/1A
IN9/1B	11	18	ENABLE
GND	12	17	A_0
V_{REF}	13	16	A_1
A_3	14	15	A_2

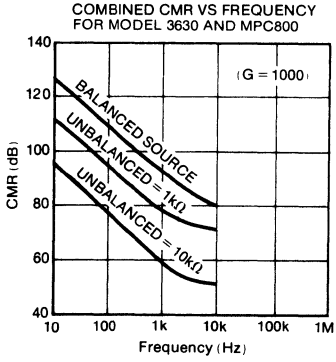
MODEL	MPC800KG, MPC800SG			
PARAMETER	MIN	TYP	MAX	UNITS
TEMPERATURE				
MPC800KG				
Specification	0		+75	°C
Storage	-65		+150	°C
MPC800SG				
Specification	-55		+125	°C
Storage	-65		+150	°C

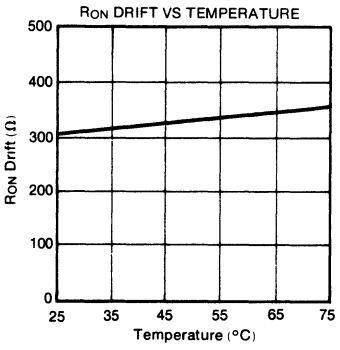
NOTES.
1 Reference voltage controls noise immunity, normally left open for TTL compatibility and connected to V_{DD} for CMOS compatibility
2 $V_{IN} = \pm 10V$, $I_{OUT} = 100\mu A$
3 Single-ended mode
4. Logic levels specified for V_{REF} (pin 13) open
5 For single-ended operation, connect output A (pin 28) to output B (pin 2) and use A_3 (pin 14) as an address line For differential operation connect A_3 to $-V_{CC}$
6 Derate 8mW/°C above $T_A = +75°C$
7 10V, p-p, sine wave on all unused channels See Typical Performance Curves
8 For 20V step input to ON channel, into 1kΩ load

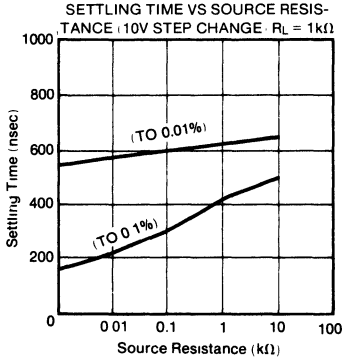
TYPICAL PERFORMANCE CURVES











DISCUSSION OF PERFORMANCE

STATIC TRANSFER ACCURACY

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current, and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

RESISTIVE LOADING ERRORS

The source and load impedances will determine the ON resistance loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of $10^8\Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000Ω source resistance will present less than 0.002% loading error and 10kΩ source resistance will increase source loading error 0.02% with a $10^8\Omega$ load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1):

Source and Multiplexer Resistive Loading Error

$$\epsilon\ (R_S + R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where $R_S = R_{source}$
R_L = Load Resistance
R_{ON} = Multiplexer ON resistance

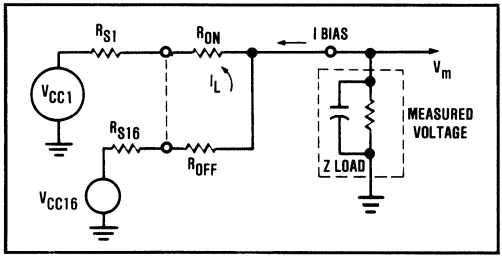


FIGURE 1. MPC800 Static Accuracy Equivalent Circuit (Single-ended Operation).

Input Offset Voltage

Bias and leakage currents generate an input Offset voltage as a result of the I_B drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA, a leakage current of 1nA, and an ON resistance of 700Ω will generate an offset voltage of 19μV if a 1000Ω source is used, and 118μV if a 10kΩ source is used. In general, for the MPC800 the Offset voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L)(R_{ON} + R_{source}) \text{ where}$$

I_B = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{source} = Source resistance

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low level signals with full scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications.

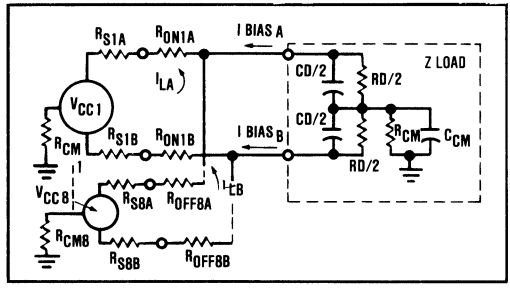


FIGURE 2. MPC800 Static Accuracy Equivalent Circuit (Differential Operation).

Load (Output Device) Characteristics

- Use devices with very low bias current. Generally, FET input amplifiers should be used for low level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be $10^{10}\Omega$ or higher.

Source Characteristics

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC800 is used for multiplexing high level signals of 1V to 10V full scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low level signal applications

SETTLING TIME

Settling time is the time required for the multiplexer to reach and maintain an output within a specified error band of its final value in response to a step input The settling time of the MPC800 is primarily due to the channel capacitance and a combination of resistances which include the source and load resistances.

If the parallel combination of the source and load resistance times the total channel capacitance is kept small, then the settling time is primarily affected by internal RC's. For the MPC800 the internal capacitance is approximately 20pF differential or 40pF single-ended With external capacitance neglected, the time constant of source resistance in parallel with load resistance and the internal capacitance should be kept less than 40nsec This means the source resistance should be kept to less than 2kΩ (assume high load resistance) to maintain fast settling times

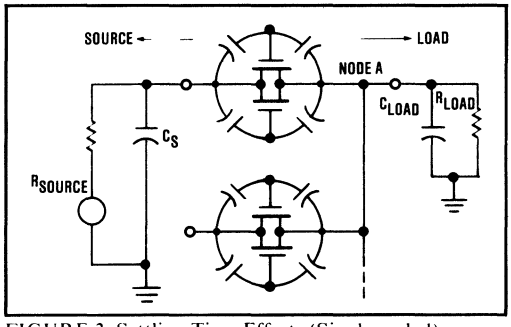


FIGURE 3. Settling Time Effects (Single-ended).

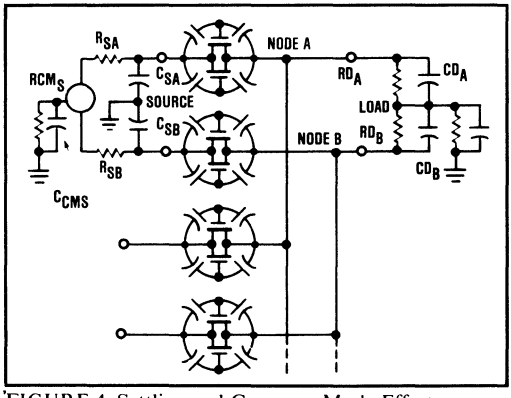


FIGURE 4. Settling and Common-Mode Effects (Differential).

ACCESS TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the 7 differential or 15 single-ended OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance, and junction capacitances in series with the R_{ON} and R_{source} impedances of the ON channel. Crosstalk is measured with a 20V, pk-pk, 1000Hz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

COMMON-MODE REJECTION (DIFFERENTIAL MODE ONLY)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. Protection is provided for common-mode signals of ±2V above the power supply voltages with no damage to the analog switches.

The CMR of the MPC800 and Burr-Brown's model 3630 Instrumentation Amplifier is 120dB at DC to 10Hz with a 6dB/octave rolloff to 80dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown model 3630 instrumentation amplifier connected for a gain of 1000 and with source unbalance of 10kΩ, 1kΩ and no unbalance.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch.

- Load impedance mismatch.
- Multiplexer impedance and leakage current mismatch.
- Load and source common-mode impedance.

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

INSTALLATION & OPERATING INSTRUCTIONS

The ENABLE input, pin 18, is included for expansion of the number of channels on a single-node as illustrated in Figure 5. With the ENABLE line at a logic 1, the channel is selected by the Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to logic 1.

For the best settling time, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pullup resistors are recommended.

To preserve common-mode rejection of the MPC800 use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

LOGIC LEVELS

The logic level is user-programmable as either TTL-compatible by leaving the V_{REF} (pin 13) open or CMOS-compatible by connecting the V_{REF} to V_{DD} (CMOS supply voltage).

16-CHANNEL SINGLE-ENDED OPERATION

To use the MPC800 as a 16-channel single-ended multiplexer, output A (pin 28) is connected to output B (pin 2) to form a single output, then all four address lines (A_0, A_1, A_2 and A_3) are used to address the correct channel.

The MPC800 can also be used as a dual 8-channel single-ended multiplexer by not connecting output A and B, but then only one channel in one of the multiplexers can be addressed at a time.

8-CHANNEL DIFFERENTIAL OPERATION

To use the MPC800 as an 8-channel differential multiplexer, connect address line A_3 to $-V_{CC}$ then use the remaining three address lines (A_0, A_1 and A_2) to address the correct channel. The differential inputs are the pairs of A_1 and B_1, A_2 and B_2, etc.

TRUTH TABLES

MPC800 used as 16-channel single-ended multiplexer or 8-channel dual multiplexer.

USE A_3 AS DIGITAL ADDRESS INPUT					"ON" CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	NONE	NONE
H	L	L	L	L	1A	NONE
H	L	L	L	H	2A	NONE
H	L	L	H	L	3A	NONE
H	L	L	H	H	4A	NONE
H	L	H	L	L	5A	NONE
H	L	H	L	H	6A	NONE
H	L	H	H	L	7A	NONE
H	L	H	H	H	8A	NONE
H	H	L	L	L	NONE	1B
H	H	L	L	H	NONE	2B
H	H	L	H	L	NONE	3B
H	H	L	H	H	NONE	4B
H	H	H	L	L	NONE	5B
H	H	H	L	H	NONE	6B
H	H	H	H	L	NONE	7B
H	H	H	H	H	NONE	8B

For 16-channel single-ended function, tie "out A" to "out B, for dual 8-channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low

MPC800 used as 8-channel differential multiplexer.

A_3 CONNECT TO $-V_{CC}$				"ON" CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

CHANNEL EXPANSION

Single-tier Expansion

Up to four MPC800's can be connected to a single node to form a 64-channel single-ended multiplexer or up to eight MPC800's can be connected to two nodes to form a 64-channel differential multiplexer. Programming is accomplished with a six-bit address and a 1 of 4 decoder for 64-channel single-ended expansion (see Figure 5) or an eight-bit address and a 1 of 8 decoder for 64-channel

differential expansion. The decoder drives the enable inputs of the MPC800, turning on only one multiplexer at a time.

Two-tier Expansion

Up to seventeen MPC800's can be connected in a two-tier structure to form a 256-channel single-ended multiplexer (see Figure 6) or up to nine MPC800's can be connected in a two-tier structure to form a 64-channel differential multiplexer. Programming is accomplished with a 8-bit address.

Single vs Multitiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced Offset), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single-node configuration, data cannot be taken from any channel, whereas only one-channel group is failed (8 or 16) in the multitiered configuration.

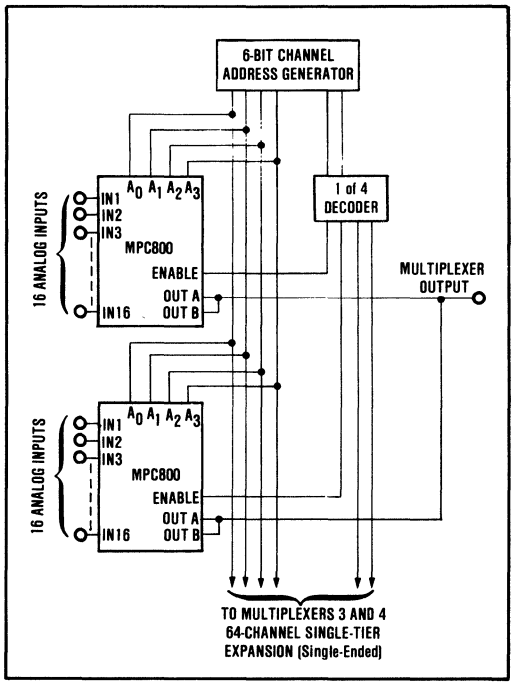


FIGURE 5. 32- to 64-Channel, Single-tier Expansion.

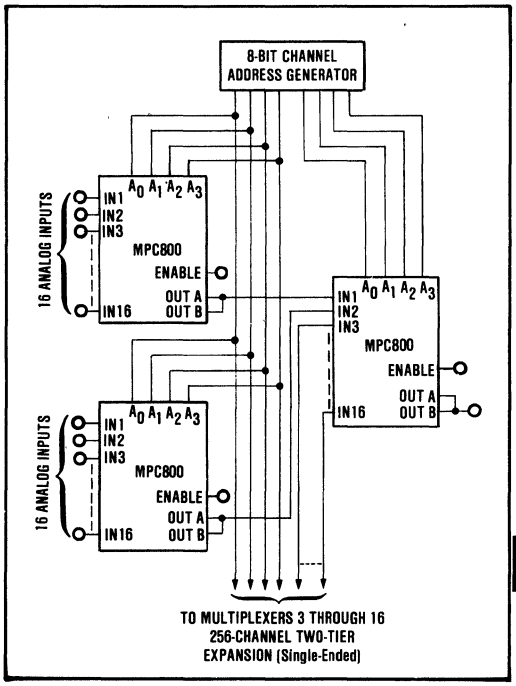
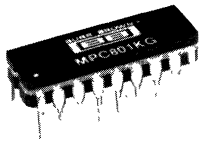


FIGURE 6. Channel Expansion up to 256 Channels using 16 x 16 Two-tiered Expansion.

BURR-BROWN®

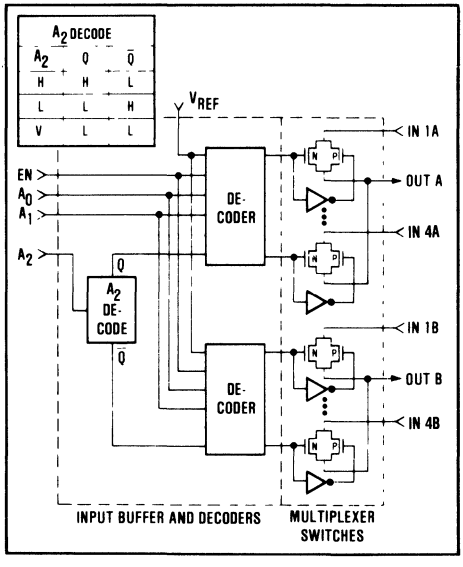
MPC801



High Speed
CMOS ANALOG MULTIPLEXER

FEATURES

- HIGH SPEED
  - 80nsec access time
  - 800nsec settling to 0.01%
  - 250nsec settling to 0.1%
- USER-PROGRAMMABLE
  - 8-channel single-ended or
  - 4-channel differential
- SELECTABLE TTL or CMOS COMPATIBILITY
- WILL NOT SHORT SIGNAL SOURCES
  - Break-before-make switching
- SELF-CONTAINED WITH INTERNAL CHANNEL ADDRESS DECODER
- 18-PIN HERMETIC DUAL-IN-LINE PACKAGE



DESCRIPTION

The MPC801 is a high speed multiplexer that is user-programmable for 8-channel single-ended operation or 4-channel differential operation and for TTL or CMOS compatibility.

The MPC801 features a self-contained binary address decoder. It also has an enable line which allows the user to inhibit the entire multiplexer thereby facilitating channel expansion by adding additional multiplexers.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, low ON resistance, high OFF resistance, low feedthrough capacitance, and fast settling time.

Two models are available, the MPC801KG for operation from 0°C to +75°C and the MPC801SG for operation from -55°C to +125°C.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS464A

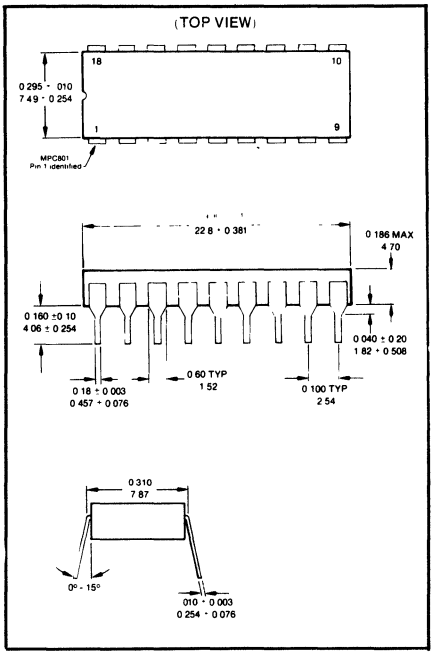
SPECIFICATIONS

ELECTRICAL

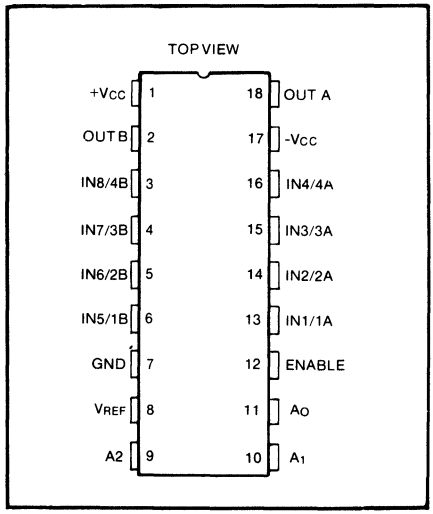
At T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted

MODEL	MPC801KG, MPC801SG			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT				
ANALOG INPUT				
Voltage Range	-15		+15	V
Maximum Overvoltage	$-V_{CC}$ -2		$+V_{CC}$ +2	V
Number of Input Channels				
Differential	4			
Single-Ended	8			
Reference Voltage Range(1)	6		10	V
ON Characteristics(2)				
ON Resistance (R_{ON}) at +25°C		500	750	Ω
Over Temperature Range		700	1000	Ω
R_{ON} Drift vs Temperature	See Typical Performance Curves			
R_{ON} Mismatch		< 10		Ω
ON Channel Leakage		0 1		nA
Over Temperature Range		0 3	50	nA
ON Channel Leakage Drift	See Typical Performance Curves			
OFF Characteristics				
OFF Isolation		90		dB
OFF Channel Input Leakage		0 05		nA
Over Temperature Range		0 6	50	nA
OFF Channel Input Leakage Drift	See Typical Performance Curves			
OFF Channel Output Leakage		0 1		nA
Over Temperature Range		0 30	50	nA
OFF Channel Output Leakage Drift	See Typical Performance Curves			
Output Leakage (All channels disabled)(3)		0 02		nA
Output Leakage with Overvoltage				
+16V Input		< 0 35		mA
-16V Input		< 0 65		mA
DIGITAL INPUTS				
Over Temperature Range				
TTL(4)				
Logic "0" (V_{AL})			0 8	V
Logic "1" (V_{AH})	2 4			V
I_{AH}		0 05	1	µA
I_{AL}		4	20	µA
TTL Input Overvoltage	-6		6	V
CMOS				
Logic "0" (V_{AL})			0 3V_{REF}	V
Logic "1" (V_{AH})	0 7 V_{REF}			V
CMOS Input Overvoltage	-2		$+V_{CC}$ +2	V
Address A_2 Overvoltage	$-V_{CC}$ -2		$+V_{CC}$ +2	V
Digital Input Capacitance		5		pF
Channel Select(5)				
Single-Ended	3-bit binary code one of 8			
Differential	2-bit binary code on of 4			
Enable	Logic "0" inhibits all channels			
POWER REQUIREMENTS				
Over Temperature Range				
Rated Supply Voltage		±15		V
Maximum Voltage Between Supply Pins			33	V
Total Power Dissipation		360		mW
Allowable Total Power Dissipation(6)			725	mW
Supply Drain +25°C				
At 1MHz Switching Speed		+14, -12 5		mA
At 100kHz Switching Speed		+12 5,-12 5		mA
DYNAMIC CHARACTERISTICS				
Gain Error		< 0 0003		%
Cross Talk(7)	See Typical Performance Curves			
T_{OPEN} (Break before make delay)		20		nsec
Access Time at 25°C		80	125	nsec
Over Temperature Range		110	150	nsec
Settling Time(8)				
to 0 1% (20mV		250		nsec
to 0 01% 2mV		800		nsec
Common-Mode Rejection Differential				
DC		> 125		dB
60Hz		> 75		dB
OFF Channel Input Capacitance, C_S off		1 9		pF
OFF Channel Output Capacitance C_O off		10		pF
OFF Input to Output Capacitance, C_{DS} off		0 02		pF

MECHANICAL



PIN CONFIGURATION

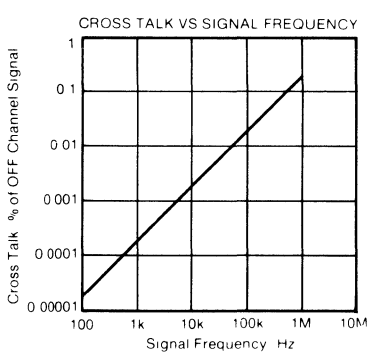


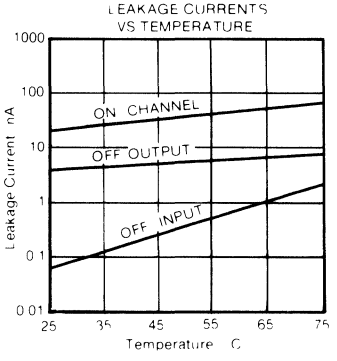
ELECTRICAL (CONT)

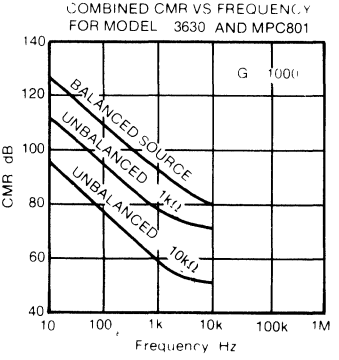
MODEL	MCP801KG, MPC801SG			
PARAMETER	MIN	TYP	MAX	UNITS
TEMPERATURE				
MPC801KG				
Specification	0		+75	°C
Storage	−65		+150	°C
MPC801SG				
Specification	−55		+125	°C
Storage	−65		+150	°C

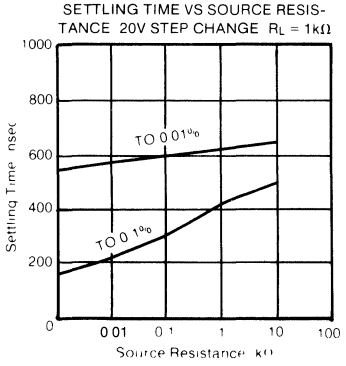
NOTES
1 Reference voltage controls noise immunity normally left open for TTL compatibility and connected to V_{DD} for CMOS compatibility
2 V_{IN} ±10V I_{OUT} 100μA
3 Single-ended mode
4 Logic levels specified for V_{REF} = pin 8 open
5 For single-ended operation connect output A pin 18 to output B pin 2 and use A_2 pin 9 as an address line For differential operation connect A_2 to $-V_{CC}$
6 Derate 8mW/°C above T_A = +75°C
7 10V p-p sine wave on all unused channels See Typical Performance Curves
8 For 20V step input to ON channel, into 1kΩ load

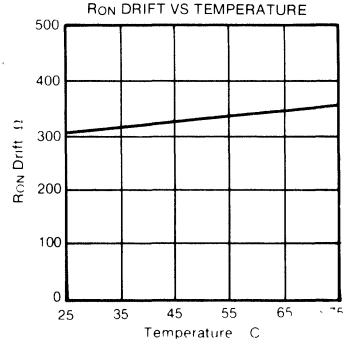
TYPICAL PERFORMANCE CURVES











DISCUSSION OF PERFORMANCE

STATIC TRANSFER ACCURACY

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current, and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

RESISTIVE LOADING ERRORS

The source and load impedances will determine the ON resistance loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of $10^8\Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000Ω source resistance will present less than 0.002% loading error and 10kΩ source resistance will increase source loading error 0.02% with a $10^8\Omega$ load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1):

Source and Multiplexer Resistive Loading Error

$$\epsilon\,(R_S + R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_I} \times 100\% \text{ where}$$

$R_S = R_{source}$
R_I = Load resistance
R_{ON} = Multiplexer ON resistance.

Input Offset Voltage

Bias and leakage currents generate an input Offset voltage as a result of the I_R drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA, a leakage current of 1nA, and an ON resistance of 700Ω will generate an offset voltage of 19μV if a 1000Ω source is used, and 118μV if a 10kΩ is used. In general, for the MPC801 the Offset voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_I)(R_{ON} + R_{source}) \text{ where}$$

I_B = Bias Current of device multiplexer is driving
I_I = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{source} = Source resistance.

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low level signals with full scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications.

Load (Output Device) Characteristics

- Use devices with very low bias current. Generally, FET input amplifiers should be used for low level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be $10^{10}\Omega$ or higher.

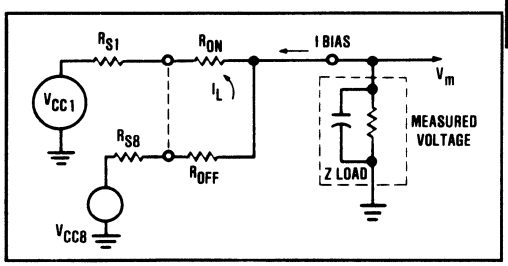


FIGURE 1. MPC801 Static Accuracy Equivalent Circuit (Single-ended Operation).

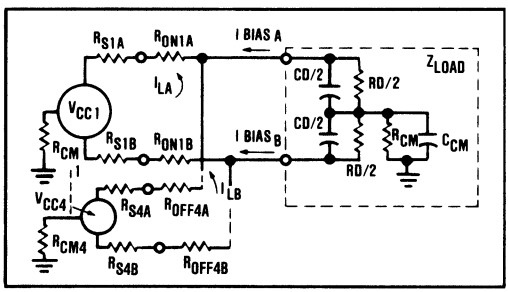


FIGURE 2. MPC801 Static Accuracy Equivalent Circuit (Differential Operation).

Source Characteristics

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC801 is used for multiplexing high level signals of 1V to 10V full scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low level signal applications

SETTLING TIME

Settling time is the time required for the multiplexer to reach and maintain an output within a specified error band of its final value in response to a step input. The settling time of the MPC801 is primarily due to the channel capacitance and a combination of resistances which include the source and load resistances.

If the parallel combination of the source and load resistance times the total channel capacitance is kept small, then the settling time is primarily affected by internal RC's. For the MPC801 the internal capacitance is approximately 10pF differential or 20pF single-ended.

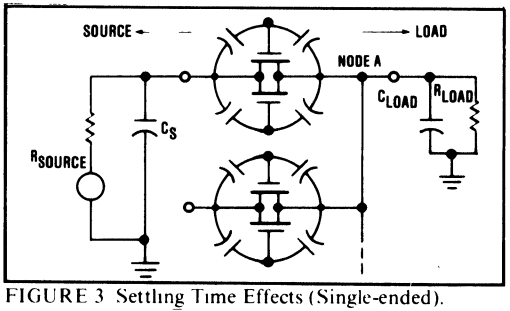


FIGURE 3 Settling Time Effects (Single-ended).

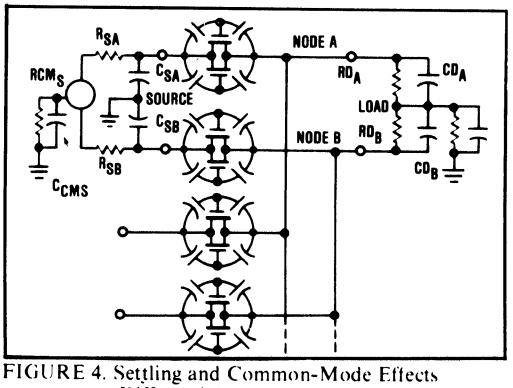


FIGURE 4. Settling and Common-Mode Effects (Differential).

With external capacitance neglected, the time constant of source resistance in parallel with load resistance and the internal capacitance should be kept less than 40nsec. This means the source resistance should be kept to less than 4kΩ (assume high load resistance) to maintain fast settling times.

ACCESS TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the 3 differential or 7 single-ended OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance, and junction capacitances in series with the R_{ON} and R_{source} impedances of the ON channel. Crosstalk is measured with a 20V, pk-pk, 1000Hz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

COMMON-MODE REJECTION (DIFFERENTIAL MODE ONLY)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. Protection is provided for common-mode signals of ±2V above the power supply voltages with no damage to the analog switches.

The CMR of the MPC801 and Burr-Brown's model 3630 Instrumentation Amplifier is 120dB at DC to 10Hz with a 6dB/octave rolloff to 80dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown model 3630 instrumentation amplifier connected for a gain of 1000 and with source unbalance of 10kΩ, 1kΩ and no unbalance.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch.
- Load impedance mismatch.
- Multiplexer impedance and leakage current mismatch.

- Load and source common-mode impedance.

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

INSTALLATION & OPERATING INSTRUCTIONS

The ENABLE input, pin 12, is included for expansion of the number of channels on a single-node as illustrated in Figure 5. With the ENABLE line at a logic 1, the channel is selected by the Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to logic 1.

For the best settling time, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pullup resistors are recommended.

To preserve common-mode rejection of the MPC801 use twisted-shielded pair wire for signal lines and inter-tier connections and or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

LOGIC LEVELS

The logic level is user-programmable as either TTL-compatible by leaving the V_{RH} (pin 8) open or CMOS-compatible by connecting the V_{RH} to V_{DD} (CMOS supply voltage).

8-CHANNEL SINGLE-ENDED OPERATION

To use the MPC801 as an 8-channel single-ended multiplexer, output A (pin 18) is connected to output B (pin 2) to form a single output, then all three address lines (A_0, A_1, and A_2) are used to address the correct channel.

The MPC801 can also be used as a dual channel single-ended multiplexer by not connecting output A and B, but then only one channel in one of the multiplexers can be addressed at a time.

4-CHANNEL DIFFERENTIAL OPERATION

To use the MPC801 as an 4-channel differential multiplexer, connect address line A_2 to $-V_{CC}$ then use the remaining two address lines (A_0 and A_1) to address the correct channel. The differential inputs are the pairs of A_1 and B_1, A_2 and B_2, etc.

TRUTH TABLES

MPC801 used as 8-channel single-ended multiplexer or 4-channel dual multiplexer.

USE A_2 AS DIGITAL ADDRESS INPUT				"ON" CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	NONE
H	L	L	H	2A	NONE
H	L	H	L	3A	NONE
H	L	H	H	4A	NONE
H	H	L	L	NONE	1B
H	H	L	H	NONE	2B
H	H	H	L	NONE	3B
H	H	H	H	NONE	4B

For 8-channel single-ended function, tie "out A" to "out B", for dual 4-channel function use the A_2 address pin to select between MUX A and MUX B, where MUX A is selected with A_2 low

MPC801 used as 4-channel differential multiplexer.

A_2 CONNECT TO $-V_{CC}$			"ON" CHANNEL TO	
ENABLE	A_1	A_0	OUT A	OUT B
L	X	X	NONE	NONE
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

CHANNEL EXPANSION

Single-tier Expansion

Up to eight MPC801's can be connected to a single node to form a 64-channel single-ended multiplexer or up to eight MPC801's can be connected to two nodes to form a 32-channel differential multiplexer. Programming is accomplished with a 6-bit address and a 1 of 8 decoder (Figure 5). The decoder drives the enable inputs of the MPC801, turning on only one multiplexer at a time.

Two-tier Expansion

Up to nine MPC801's can be connected in a two-tier structure to form a 64-channel single-ended multiplexer (Figure 6) or up to five MPC801's can be connected in a two-tier structure to form a 16-channel differential multiplexer. Programming is accomplished with a 6-bit address.

SINGLE VS MULTITIERED CHANNEL EXPANSION

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced Offset), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single-

node configuration, data cannot be taken from any channel, whereas only one channel group is failed (4 or 8) in the multitiered configuration.

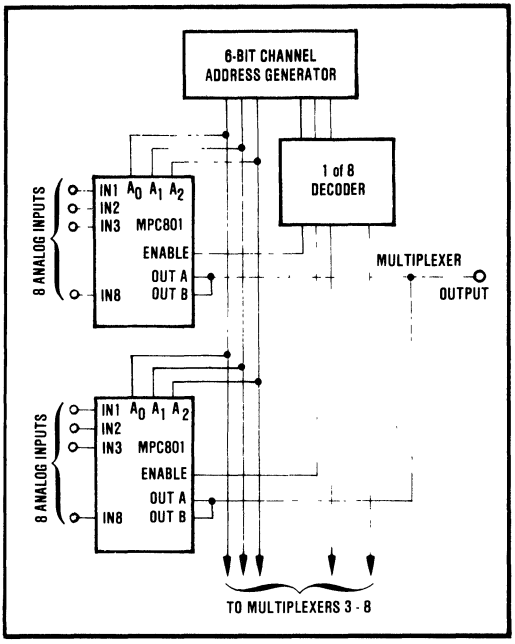


FIGURE 5. 64-Channel, Single-Tier, Single-Ended Expansion.

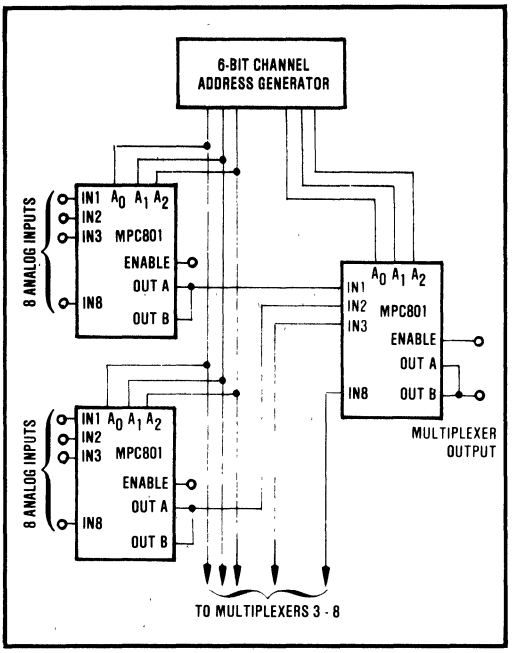
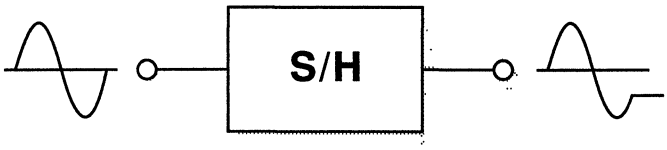


FIGURE 6. 64-channel, Two-Tier, Single-Ended Expansion.



SAMPLE / HOLD AMPLIFIERS

Sample/hold amplifiers are a key part of the complete data acquisition solution. For any application requiring use of a sample/hold amplifier, consider the variety of products listed in the following Selection Guides. Products range from the SHC298, a low cost solution for your medium-speed 12-bit system, to the SHC600, a high-speed sample/hold optimized for high-bandwidth requirements.

Use of a carefully selected sample/hold can increase the sampling bandwidth of an analog-to-digital converter by up to four orders of magnitude, while insuring that an accurate value of the signal is captured at a specific point in time. In many applications not viewed as requiring high bandwidth data acquisition, optimum performance and cost may still be achieved by using combinations of very high speed multiplexers, sample/holds, and analog-to-digital converters.

8

SAMPLE / HOLD AMPLIFIERS
SELECTION GUIDES

The Selection Guides show parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

SAMPLE/HOLD AMPLIFIERS — **Boldface = NEW**

Description	Model	Gain Error (%)	Offset Error (mV)	Charge Offset (mV)	Acq Time (µs max)	Droop Rate (µV/ms)	Temp Range[1]	Pkg[2]	Q, BI[3] Screen	Page
Fast, High Accuracy	SHC76	±0.02	±3	±6 typ	3	1	Ind, Com, Mil	HMD	—	8-3
Fast, Industry Std	SHC85	±0.01	±2	±2 max	4.5	125	Com, Mil	HMD	Q	8-7
Low Cost, Fast Industry Std	SHC5320	NA	±0.5	±1 typ	1.5	0.5	Com, Mil	HCD	BI	8-32
Lowest Cost Industry Std	**SHC298**	**±0.01**	±7	**±25 max**	**10**	**100**	**Com, Ind**	**PDIP, MC, SOIC**	**BI**	**8-11**

HIGH-SPEED SAMPLE/HOLD AMPLIFIERS — **Boldface = NEW**

Description	Model	Gain Error (%)	Offset Error (mV)	Ampl BW –3dB, (MHz)	Acq Time (µs max)	Droop Rate (µV/µs)	Temp Range[1]	Input Range (Vp-p)	Pkg[2]	Q[3] Screen	Page
High Speed with Buffer	SHC803	±0.1	±3	16	0.35	±5	Ind	20	HDIP	Q	8-26
High Speed	SHC804	±0.1	±3	16	0.35	±5	Ind	20	HDIP	Q	8-26
Ultra-High Speed	SHC600	±0.1	±5	70	0.05	±180	Ind	2.5	CDIP	Q	8-18
	SHC601	**±2**	**±50**	**100**	**0.022**	**±100**	**Ind**	**2.5**	**CDIP**	**Q**	**8-22**
Very High Accuracy, Fast	**SHC702**	**±0.1**	±3	**3**	**0.8**	±2	**Ind**	**20**	**24-p DIP**	—	**9.2-118**

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) MC = Metal Can, PDIP = Plastic DIP, HCD = Hermetic Ceramic DIP, CD = Ceramic DIP, HMD = Hermetic Metal DIP, SOIC = Surface Mount Package. (3) Q indicates optional reliability screening is available for this model. BI indicates that an optional 160 hour burn-in is available for the model.

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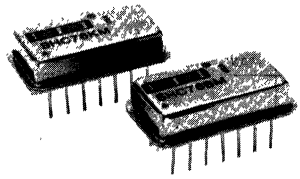


SHC76

SAMPLE/HOLD AMPLIFIER

FEATURES

- FAST (6μs max) ACQUISITION TIME (14-bit)
- APERTURE JITTER 400ps
- TYPICAL POWER DISSIPATION LESS THAN 250mW
- COMPATIBLE WITH HIGH RESOLUTION A/D CONVERTERS ADC76, PCM75, AND ADC71

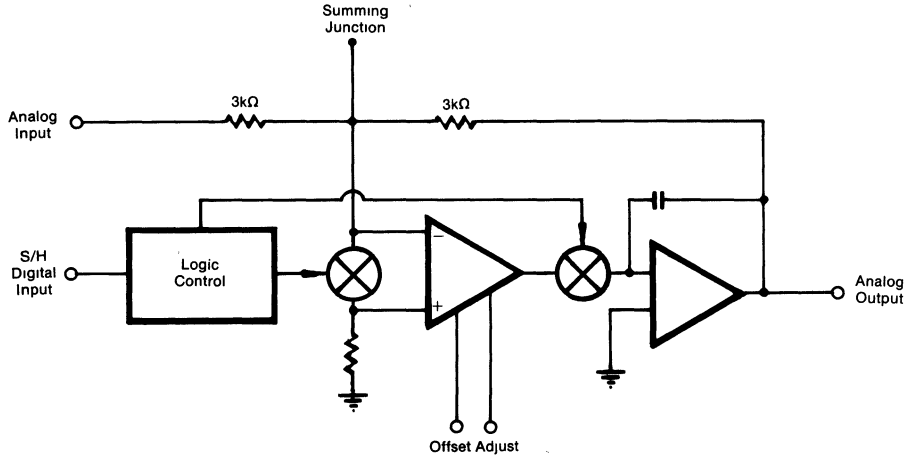
DESCRIPTION

The SHC76 is a fast, high-accuracy hybrid sample/-hold circuit suitable for use in high-resolution data acquisition systems.

The SHC76 is complete with internal hold capacitor and incorporates an internal compensation network which minimizes sample-to-hold charge offset. The SHC76 is configured as a unity-gain inverter.

High-resolution converters such as the ADC76 and ADC71 are compatible with SHC76 in forming complete, 14-bit accurate analog-to-digital conversion systems.

The SHC76 comes in a 14-pin single-wide hermetic metal DIP. Power supply requirements are specified from ±14.5 V to ±15.5V with guaranteed operation from ±11.4V to ±18V. Input voltage range is ±10V. The SHC76 is available in two temperature ranges: KM, for 0°C to +70°C; and BM, for −25°C to +85°C operation.



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PDS-641A

SPECIFICATIONS

ELECTRICAL

Typical at +25°C and nominal power supply voltage of ±15V unless otherwise noted

MODEL	SHC76KM/BM			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
ANALOG INPUT				
Voltage Range	±10			V
Overvoltage, no damage			±15	V
Impedance		3000		Ω
DIGITAL INPUT				
(TTL-Compatible)				
Track Mode, Logic "1"	2 0		5.5	V
Hold Mode, Logic "0"	0		0.8	V
I_{IH}, V_{IH} = 2 4V			400	μA
I_{IL}, V_{IL} = 0 4V			1000	μA
ANALOG OUTPUT				
Voltage		±10		V
Current		5		mA
Short-Circuit Current		20		mA
Impedance		1		Ω
DC ACCURACY/STABILITY				
Gain		−1.00		V/V
Gain Error		±0 01	±0 02	%
Gain Nonlinearity				
(±10V Output Track)		±0 001		%
Gain Temperature Coefficient		1	5	ppm/°C
Offset Voltage[1]			±3	mV
Output Offset at T_{MIN}, T_{MAX}				
(Track)		±6		mV
TRACK MODE DYNAMICS				
Frequency Response				
Small Signal (−3dB)		1.5		MHz
Full Power Bandwidth		0.5		MHz
Slew Rate		30		V/μs
Noise in Track Mode				
(DC to 1 0MHz)		200		μV rms
TRACK-TO-HOLD SWITCHING				
Aperture Time		30		ns
Aperture Uncertainty (Jitter)		0.4		ns
Offset Step (Pedestal)		±2	±4	mV
Pedestal at Temp				
KM grade		±4		mV
BM grade		±6		mV
Switching Transient				
Amplitude		200		mV
Settling to 1mV		0.5	2	μs
Settling to 0.3mV		1.0	3	μs
HOLD MODE DYNAMICS				
Droop Rate		0.1	1 0	μV/μs
Droop Rate at T_{MAX}			100	μV/μs
Feedthrough Rejection				
(10V p-p, 20kHz)	74	86		dB
HOLD-TO-TRACK DYNAMICS				
Acquisition Time				
To ±0 01% of 20V		1.5	3.0	μs
To ±0 003% of 20V		4.0	6.0	μs
POWER REQUIREMENTS				
Nominal Voltages for Rated				
Performance	±14 5	±15 0	±15.5	V
Operating Range[2]	±11 4		±18.0	V
Power Supply Rejection		100		μV/V
Supply Current. $+V_S$		15	20	mA
$-V_S$		−4	−10	mA
Power Dissipation		300	500	mW
TEMPERATURE RANGE				
Operating KM grade	0		+70	°C
BM grade	−25		+85	°C
Storage	−55		+125	°C

NOTES (1) Adjustable to zero with external circuit. (2) Operating to derated performance with $V_{IN} < V_S - 5V$

ABSOLUTE MAXIMUM RATINGS[1]

Voltage Between $+V_{CC}$ and $-V_{CC}$ Terminals 40V
Input Voltage . . . . . Actual Supply Voltage
Differential Input Voltage . . . . . ±24V
Digital Input Voltage . . . . . −0 5V to +5.5V
Output Current, continuous[2] . . . . . ±20mA
Internal Power Dissipation 450mW
Storage Temperature Range . . . . . $-65°C < T_A < +150°C$
Output Short-Circuit Duration[3] . . . . . Momentary to Common
Lead Temperature (soldering, 10 seconds) . . . . . 300°C

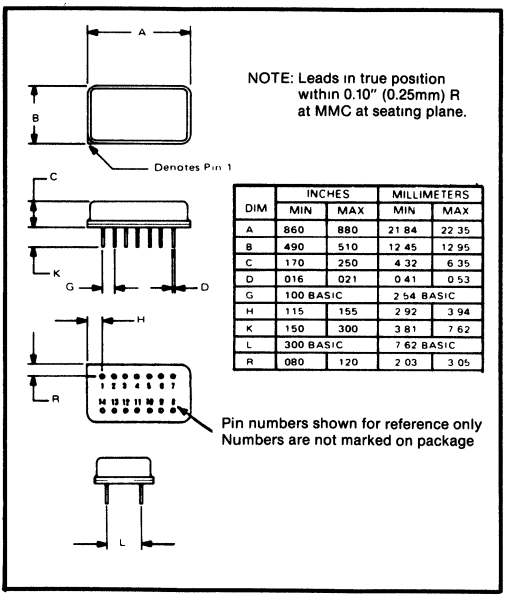
CAUTION These devices are sensitive to electrostatic discharge Appropriate I C handling procedures should be followed.

NOTES (1) Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired Functional operation under any of these conditions is not necessarily implied (2) Internal power dissipation may limit output current to less than +20mA (3) **WARNING: This device cannot withstand even a momentary short circuit to either supply.**

PIN ASSIGNMENTS

Pin	Description	Pin	Description
1	Digital Input	8	Analog Output
2	No Connection	9	Offset Adjust
3	No Connection	10	No Connection
4	Digital Ground	11	+15V Supply
5	No Connection	12	Summing Junction
6	Analog Ground	13	Analog Input
7	Offset Adjust	14	−15V Supply

MECHANICAL

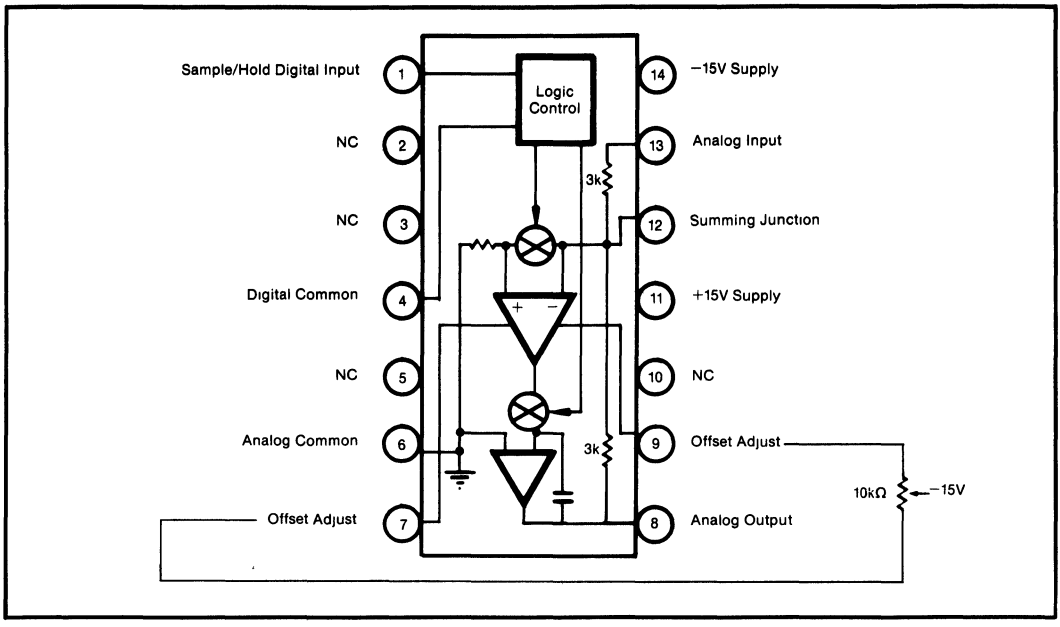


NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	860	880	21 84	22 35
B	490	510	12 45	12 95
C	170	250	4 32	6 35
D	016	021	0 41	0 53
G	100 BASIC		2 54 BASIC	
H	115	155	2 92	3 94
K	150	300	3 81	7 62
L	300 BASIC		7 62 BASIC	
R	080	120	2 03	3 05

Pin numbers shown for reference only
Numbers are not marked on package

MECHANICAL



DISCUSSION OF SPECIFICATIONS

THROUGHPUT NONLINEARITY

Defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by Offset and Gain adjustments.

GAIN ERROR

The difference between the input and output voltage magnitude (in the Sample mode) due to the amplifier gain errors.

DROOP RATE

The voltage decay at the output when in the Hold mode due to storage capacitor and FET switch leakage current and the input bias current of the output amplifier.

FEEDTHROUGH

The amount of output voltage change caused by an input voltage change when the sample/hold is in the Hold mode.

APERTURE DELAY TIME

The time required to switch from Sample to Hold. The time is measured from the 50% point of the Hold mode control transisition to the time at which the output stops tracking the input.

APERTURE UNCERTAINTY TIME

The nonrepeatibility of aperture delay time.

ACQUISITION TIME

The time required for the sample/hold output to settle within a given error band of its final value when the sample/hold is switched from Hold to Sample.

CHARGE OFFSET (PEDESTAL)

The output voltage change that results from charge coupled into the Hold capacitor through the gate capacitance of the switching field effect transistor. This charge appears as an offset at the output.

SAMPLE-TO-HOLD SWITCHING TRANSIENT

The switching transient which appears on the output when the sample/hold is switched from Sample to Hold. Both the magnitude and the settling time of the transient are specified.

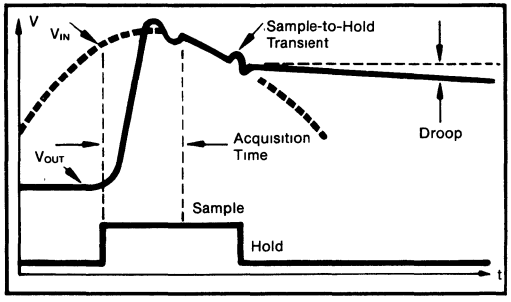


FIGURE 1. Definition of Acquisition Time, Droop and Sample-to-Hold Transient.

SAMPLED DATA ACQUISITION SYSTEM CALCULATIONS

The rated accuracy of an A/D converter in combination with the aperture uncertainty of a sample/hold determine the maximum theoretical input slew rate (frequency) of a given sampled data system.

Sine Wave $f_{MAX} = (2^{-N} \text{ FSR}) \div (2 \pi \text{ A t})$

A = max Input Signal Amplitude (peak-to-peak)
FSR = Full-Scale Range of A/D Converter
t = Aperture Uncertainty of S/H (jitter)
N = Number of Bits Accuracy

Given below are the maximum input frequencies of two A/D converters in conjunction with the SHC76:

SHC76 **13-bit** Sine Wave f_{MAX} =

$(0.000122 \times 20V) \div (2 \times \pi \times 20V \times 0.4ns)$

= 48.6kHz

SHC76 **14-bit** Sine Wave f_{MAX} =

$(0.000061 \times 20V) \div (2 \times \pi \times 20V \times 0.4ns)$

= 24.3kHz

The maximum throughput rate is determined by adding all critical conversion process times together. Throughput rate cannot exceed the maximum input frequency determined by the accuracy and jitter specs without degrading system performance. Two samples per period of a sine wave are required to satisfy the Nyquist sampling theorem. A low-pass filter is required to cut off frequencies higher than the maximum throughput frequency to prevent aliasing errors from occurring.

Throughput f_{MAX} (2 samples) =

1 ÷ [2 (S/H acquisition time + S/H settling time + A/D conversion time)]

Table I is a listing of various A/D throughput rates using the SHC76 S/H amplifier (assuming two samples per period).

TABLE I. A/D Converter Throughput Rates.

Converter	Accuracy (Bits)	Conversion Speed (μs)	Resolution (Bits)	Throughput f_{MAX} (kHz)
ADC76KG	14	17	16	19 2
	14	16	15	20 0
	14	15	14	20.8
ADC76JG	13	17	16	23 8
	13	16	15	25.0
	13	15	14	26 3
ADC71KG	14	57	16	7 58
	14	54	15	7 94
	14	50	14	8 47
ADC71JG	13	57	16	8 20
	13	54	15	8.62
	13	50	14	9 26

APPLICATIONS

Figures 2 and 3 show the SHC76 in combination with an ADC76 and ADC71 to provide 14-bit accurate A/D conversion systems.

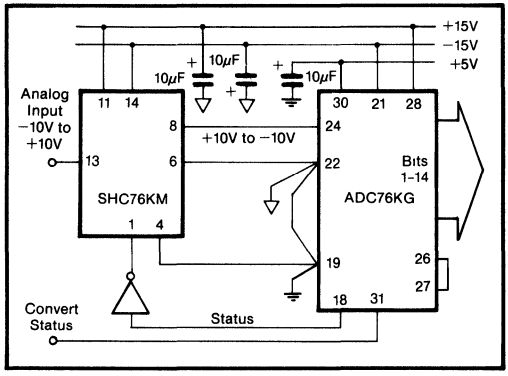


FIGURE 2. A 20kHz A/D Conversion System (14-bit accurate).

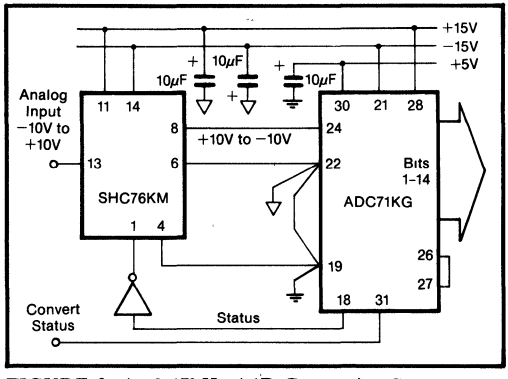


FIGURE 3. An 8.47kHz A/D Conversion System (14-bit accurate).

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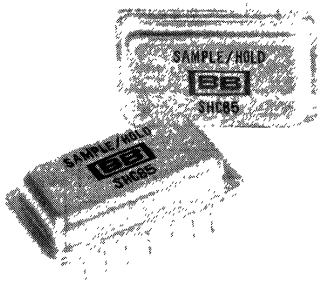
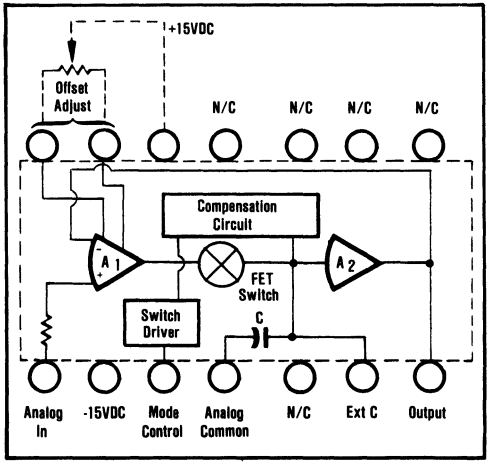


SHC85
SHC85ET

Fast IC
SAMPLE/HOLD AMPLIFIERS

FEATURES

- 14-PIN DIP PACKAGE
- 5μsec ACQUISITION TIME
- COMPLETE WITH HOLDING CAPACITOR
- ±0.01% ACCURACY
- −55°C TO +125°C TEMPERATURE RANGE (SHC85ET)



DESCRIPTION

The SHC85 is designed to acquire and hold up to ±10VDC analog signals to an accuracy of ±0.01% of full scale range in 5μsec for a 20-volt step or 4.5μsec for a 10VDC step. Featuring internally compensated circuits normally found only in more expensive and larger sample/holds, the SHC85 offers ultra-liner performance and fast acquisition speeds for the most demanding data acquisition and control applications.

Two models are available: the SHC85 is specified for 0°C to 70°C operation, and the SHC85ET is specified for -55°C to +125°C operation.

The SHC85/SHC85ET are well suited for use in:

Data Acquisition Systems
Data Distribution Systems
Analog Delay Circuits
Pulse Amplitude Modulation Circuits
Waveform Amplitude Measurement

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PDS-321A

SPECIFICATIONS

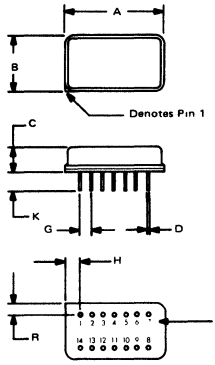
Typical at 25°C with rated supply and a 1000pF internal capacitor unless otherwise noted

ELECTRICAL

MODELS	SHC85	SCH85ET	UNITS
INPUT			
ANALOG INPUT			
Voltage Range	±10	±10	V
Maximum Safe Input Signal	±15	±15	V
Resistance	10^8	10^8	Ω
Bias Current	50	50	nA
DIGITAL INPUT (TTL Compatible)			
Mode Control	Voltage	Current	
"Sample" - Logic "1"	+2 0V < e < +8V	50nA	
"Hold" - Logic "0"	0V < e < +0.8V	-50μA	
TRANSFER CHARACTERISTICS			
ACCURACY (25°C)			
Dynamic Nonlinearity, max	±0.01	±0 01	% of 20V
At min "Hold" Time	1000	1000	μsec
Gain	+1 0	+1 0	V/V
Gain Error	±0 01	±0 01	% of 20V
Throughput Offset, max (adjust to zero)	2	2	mV
Droop Rate, max	0 5	0 5	mV/msec
Droop Rate, typical	0 125	0 125	mV/msec
Throughput Nonlinearity	±0.005	±0 005	% of 20V
Noise, rms (10Hz to 100kHz)	100	100	μV
Supply Rejection (0 to 50kHz)	100	100	μV/V
ACCURACY DRIFT			
Gain Drift	±2	±2	ppm of 20V/°C
Offset Drift	±25	±25	μV/°C
Droop Rate			
At 70°C, max	10	10	mV/msec
At +125°C, max	--	200	mV/msec
DYNAMIC CHARACTERISTICS			
Bandwidth (Full Power)(1)	200	200	kHz
Output Slew Rate	20	20	V/μsec
Aperture Time	30	30	nsec
Acquisition Time (to ±0.01%)			
10V Step, max	4 5	4.5	μsec
20V Step, max	5.0	5 0	μsec
Feedthrough in Hold Mode	±0 005	±0 005	% of step change
Charge Offset, max, at 0V Input	±2	±2	mV
Sample-to-Hold Transient			
Peak Amplitude	50	50	mV
Settling to 1mV	0 5	0 5	μsec
OUTPUT			
ANALOG OUTPUT			
Voltage Range	±10	±10	V
Current Range	±10	±10	mA
Impedance	0 1	0 1	Ω
TEMPERATURE			
Specification	0 to +70	-55 to +125	°C
Storage	-55 to +125	-55 to +125	°C
POWER SUPPLY			
Rated Voltage	±15	±15	VDC
Range	±14.5 to ±15.5	±14.5 to ±15.5	VDC
Current	±13	±13	mA

NOTE
1. Small signal bandwidth is 3MHz

MECHANICAL



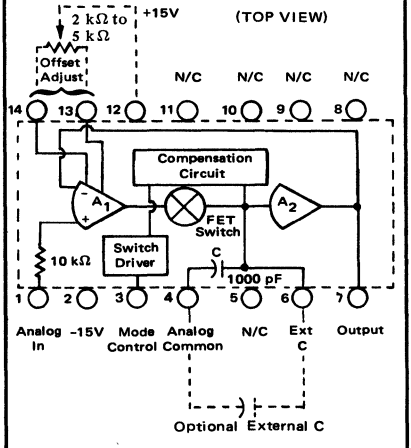
NOTE: Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	860	880	21 84	22 35
B	490	510	12 45	12 95
C	170	250	4 32	6 35
D	016	021	0 41	0 53
G	100 BASIC		2 54 BASIC	
H	115	155	2 92	3 94
K	150	300	3 81	7 62
L	300 BASIC		7 62 BASIC	
R	080	120	2 03	3 05

Case Kovar
Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 except paragraph 3 2. Mating Connector 0145MC

CONNECTION DIAGRAM



NOTE: Pins 5, 8, 9, 10 and 11 are not internally connected.

DEFINITION OF SPECIFICATIONS

DYNAMIC NONLINEARITY

This is the total nonadjustable input to output error. This specification includes throughput nonlinearity and errors due to droop, thermal transients and feedthrough, in short, all errors that cannot be adjusted to zero for a 10V input change after a 5μsec acquisition time and a 1msec hold time. Offset errors must be adjusted to zero by the offset control and gain errors must be adjusted to zero by a gain adjustment elsewhere in the system (gain adjust not included in SHC85).

GAIN ACCURACY

The difference due to amplifier gain errors between Input and Output voltage when in the "sample" mode.

DROOP RATE

The voltage decay at the output when in the "hold" mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH

The amount of the input voltage change that appears at the output when the amplifier is in the "hold" mode (see Figure 1).

THROUGHPUT - NONLINEARITY

The total charge offset and gain nonlinearity. That is, the inaccuracy due to these two errors that cannot be corrected by gain and offset adjustments. Throughput - nonlinearity is specified over the 20V input range.

THROUGHPUT OFFSET

The sum of sample offset and charge offset.

CHARGE OFFSET

The offset that results from charge transferred from the holding capacitor to the gate capacitance of the switching FET. This charge is partially restored by a special compensation circuit when the unit goes into the "hold" mode.

ACQUISITION TIME

The time required for the output to settle to its final value within a given error band, when the Mode control is switched from "hold" to "sample" (see Figure 2).

APERTURE TIME

The time required to switch from "sample" to "hold". The time is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input

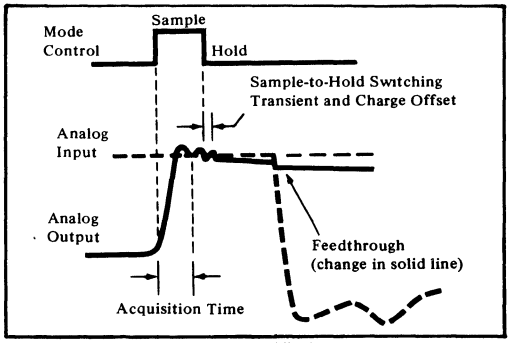


FIGURE 1. Example of Specifictions.

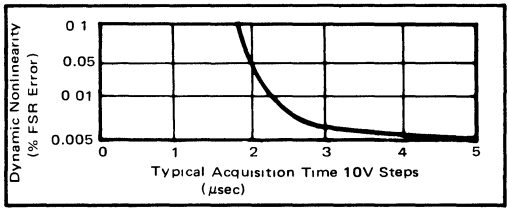


FIGURE 2. Acquisition Time vs Full Scale Range Error.

OPERATING INSTRUCTIONS

OPTIONAL EXTERNAL CAPACITOR SELECTION

The value of the external capacitor determines the droop, charge offset and acquisition time of the sample/hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table.

Figure 3 shows the behavior of acquisition time with added external capacitance. The behavior of droop with external C is determined by:

$$\text{Droop} = dv\ dt = (0.5 \times 10^{-9})\ (1000\text{pF} + C_{ext})$$

Capacitors with high insulation resistance and low dielectric absorption, such as teflon or polystyrene should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize leakage currents from the capacitor; this will minimize droop errors.

OFFSET ADJUSTMENT

Connect a 2kΩ to 5kΩ multiturn potentiometer with a TCR of 150ppm °C or less as shown in the Connection Diagram. The offset should be adjusted with the input grounded. During the adjustment, the sample hold should be switching continuously between the "sample" and the "hold" mode. The error should then be adjusted to zero where the unit is in the "hold" mode. In this way, charge offset as well as amplifier offset will be adjusted.

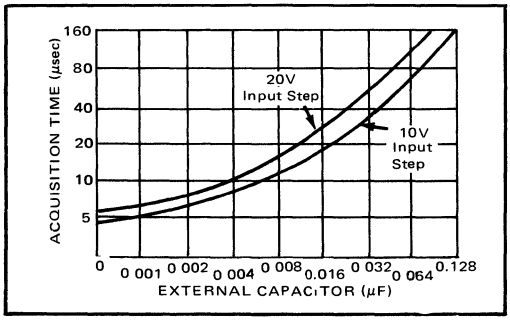
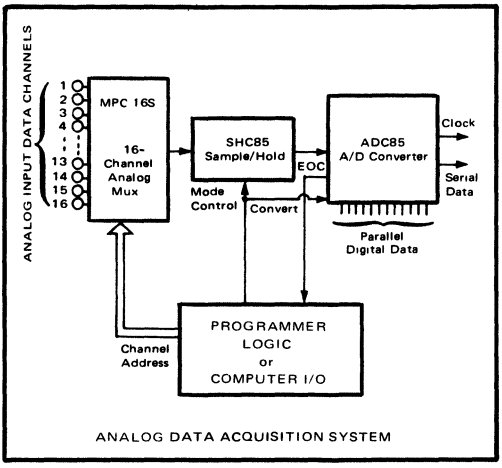


FIGURE 3. Acquisition Time vs External Capacitor.

APPLICATIONS

DATA ACQUISITION SYSTEM

The SHC85 makes an excellent device for reducing aperture time in a data acquisition system. When combined with Burr-Brown's 16-channel MPC-16S Analog Multiplexer and ADC85 10- or 12-bit A D Converter, you can have a compact 16-channel data acquisition system with 50kHz to 65kHz throughput sampling rates and 0.02 percent (RSS) system accuracy.



ANALOG DATA ACQUISITION SYSTEM

SIMULTANEOUS SAMPLE/HOLD

Time correlation of sampled data signals may be implemented by using one sample, hold for each analog signal prior to input to an analog multiplexer. The SCH85 low aperture time of 30nsec practically eliminated channel-to-channel time slew. The throughput sampling rate and the number of data channels will determine the maximum Hold time and hence, the worst-case droop error of the sample hold in the last channel to be sampled prior to the next "refresh" or sample hold command. This droop error may be minimized by adding external capacitance to the SHC85 as shown in Figure 3.

The droop error is computed by:

MAX DROOP ERROR (CHANNEL N)=(T x n) (Droop rate)

Where T = 1 System Sampling Rate and n = number of multiplexer data channels.

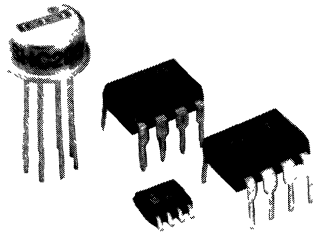
EXAMPLE:

For a 10-bit, 32-channel system with throughput sample rate of 50kHz, assuming no external capacitance, the droop error of channel N is:

Droop Error (E_D) = [(1 50kΩ) x 32][(500 x 10^{-3})] = 320μV.

For ±10V input signal range and 10-bit resolution, the resolution of ±1 2LSB is ±9.77mV. This droop error is less than 0.016LSB (negligible), and no external C need be added to reduce the droop of the SHC85.

BURR-BROWN®

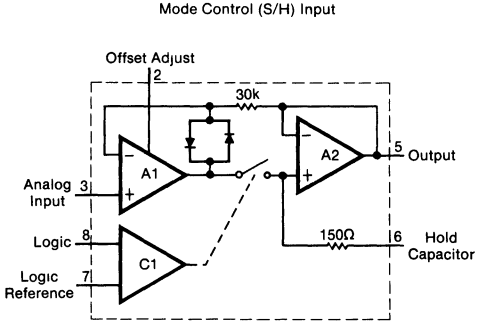


SHC298
SHC298A

Monolithic
SAMPLE/HOLD AMPLIFIER

FEATURES

- 12-BIT THROUGHPUT ACCURACY
- LESS THAN 10μs ACQUISITION TIME
- WIDEBAND NOISE LESS THAN 20μVrms
- RELIABLE MONOLITHIC CONSTRUCTION
- $10^{10}\Omega$ INPUT RESISTANCE
- TTL/CMOS-COMPATIBLE LOGIC INPUT



DESCRIPTION

The SHC298 and SHC298A are high-performance monolithic sample/hold amplifiers featuring high DC accuracy with fast acquisition times and a low droop rate. Dynamic performance and holding performance can be optimized with proper selection of the external holding capacitor. With a 1000pF holding capacitor, 12-bit accuracy can be achieved with a 6μs acquisition time. Droop rates less than 5mV/min are possible with a 1μF holding capacitor.

These sample/holds will operate over a wide supply voltage ranging from ±5V to ±18V with very little change in performance. A separate Offset Adjust pin is used to adjust the offset in either the Sample or the Hold modes. The fully differential logic inputs have low input current, and are compatible with TTL, 5V CMOS, and CMOS logic families.

The SHC298AM is available in a hermetically sealed 8-pin TO-99 package and is specified over a temperature range from −25°C to +85°C. The SHC298JP and SHC298JU are 8-pin plastic DIP and SOIC packaged parts specified over 0°C to +70°C.

The SHC298AJP, specified over 0°C to +70°C, is available in an 8-pin plastic DIP. The SHC298A grade features improved Gain and Offset Error, improved drift over temperature, and faster Acquisition Time.

The SHC298 family is a price-performance bargain. It is well suited for use with several 12-bit A/D converters in data acquisition systems, data distribution systems, and analog delay circuits.

International Airport Industrial Park • P.O. Box 11400 • Tucson, Arizona 85734 • Tel.: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491

PDS-373C

SPECIFICATIONS

ELECTRICAL

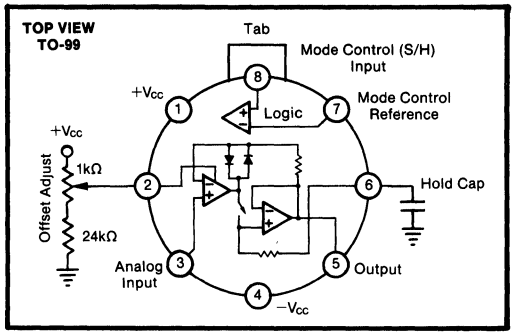
Specifications at T_J = +25°C, ±15V supplies, 1000pF holding capacitor, −11.5V ≤ V_{IN} ≤ +11.5, R_L = 10kΩ, Logic Reference Voltage = 0V, and Logic Voltage = 2.5V unless otherwise noted

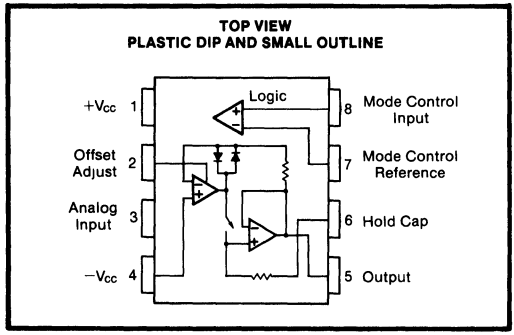
PARAMETER	SHC298AM/JP/JU MIN	SHC298AM/JP/JU TYP	SHC298AM/JP/JU MAX	SHC298AJP MIN	SHC298AJP TYP	SHC298AJP MAX	UNITS
INPUT							
ANALOG INPUT							
Resistance		10^{10}			*		Ω
Bias Current[1]		10	50		*	25	nA
DIGITAL INPUT	Pin 7		Pin8		Circuit State		
Mode Control Truth Table	0V		+2.4V		Sample (Track)		
	0V		+0.8V		Hold		
	+2.4V		+2.8V		Hold		
	+0.8V		+2.8V		Sample (Track)		
Mode Control and Mode Control Reference Input Current			10				μA
Differential Logic Threshold	0.8	1.4	2.4				V
TRANSFER CHARACTERISTICS							
ACCURACY (+25°C)							
Throughput Nonlinearity for Hold Time < 1ms		±0.010	±0.015		*	*	% of 20V
Gain		+1.0			*		V/V
Gain Error		±0.004	±0.010		±0.001	±0.005	%
Input Voltage Offset (adjust to zero)[1]		±2	±7		±1	±2	mV
Droop Rate[1]		±30	±200		*	±100	μV/ms
Charge Offset[2]		±15	±25		*	*	mV
Noise (rms) 10Hz to 100kHz		10	20		*	*	μV
Power Supply Rejection		±25	±100		*	*	μV/V
ACCURACY DRIFT							
Gain Drift		3	4		1	2	ppm/°C
Input Offset Drift		15	70		*	25	μV/°C
Charge Offset Drift C= 1000pF		50	150		*	*	μV/°C
Charge Offset Drift C = 10,000pF		20	50		*	*	μV/°C
Droop Rate at T_J = +85°C		1	10		*	*	mV/ms
DYNAMIC CHARACTERISTICS							
Full Power Bandwidth, C = 1000pF	75	125		*	*		kHz
Full Power Bandwidth, C = 10,000pF	10	16		*	*		kHz
Output Slew Rate, C = 1000pF	7	10		*	*		V/μs
Output Slew Rate, C = 10,000pF	1.4	2		*	*		V/μs
Aperture Time Negative Input Step		200	250		*	*	ns
Positive Input Step		150	200		*	*	ns
Acquisition Time (C = 1000pF). to ±0.01%, 10V step		6	10		*	*	μs
to ±0.01%, 20V step		8	12		*	*	μs
to ±0.1%, 10V step		5	9		4	6	μs
to ±0.1%, 20V step		7	11		*	*	μs
Sample/Hold Transient: Peak Amplitude		160			*		mV
Settling to 1mV		1.0	1.5		*	*	μs
Feedthrough (Response to 10V Input Step)		±0.007	±0.015		±0.004	±0.0075	% of 20V
OUTPUT							
ANALOG OUTPUT							
Voltage Range	±11.5			*			V
Current Range	±2			*			mA
Impedance (in hold mode)		0.5	4		*	*	Ω
POWER SUPPLY							
Rate Voltage		±15			*		VDC
Range	±5.0		±18	*		*	VDC
Current[1]		±4.5	±6.5		*	*	mA

*Same as specifications for SHC298AM/JP/JU

NOTES. (1) These parameters guaranteed over a supply voltage range of ±5V to = ±18V. (2) Charge offset is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01μF hold capacitor Magnitude of the charge offset is inversely proportional to hold capacitor value.

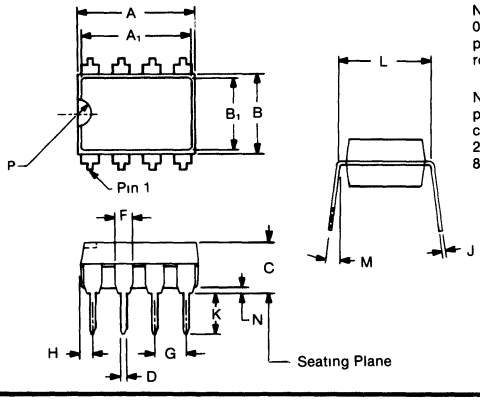
PIN DESIGNATIONS





MECHANICAL

"P" Package—Plastic DIP



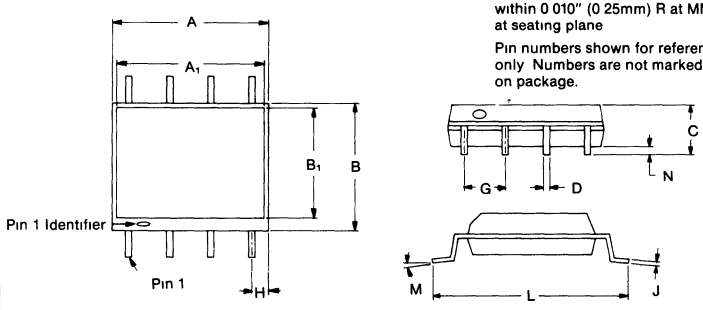
NOTE Leads in true position within 0 01" (0 25mm) R at MMC at seating plane Pin numbers shown for reference only

Numbers may not be marked on package Pin material an plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3 2)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	355	400	9 03	10 16
A_1	340	384	8 64	9 78
B	230	290	5 85	7 37
B_1	200	250	5 09	6 36
C	120	200	3 05	5 09
D	015	023	0 38	0 59
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	025	050	0 64	1 27
J	006	015	0 20	0 38
K	070	150	1 78	3 82
L	300 BASIC		7 63 BASIC	
M	0°	15°	0°	15°
N	010	030	0 25	0 76
P	025	050	0 64	1 27

θ_{JA} = 130°C/W

"U" Package—Small Outline Surface Mount



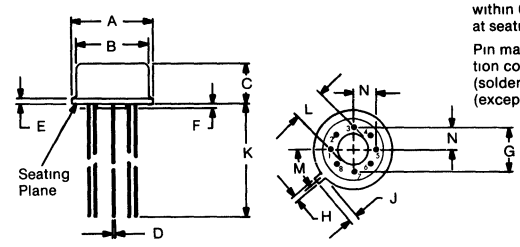
NOTE. Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers are not marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	185	201	4 70	5 11
A_1	178	201	4 52	5 11
B	146	162	3 71	4 11
B_1	130	149	3 30	3 78
C	054	145	1 37	3 69
D	015	019	0 38	0 48
G	050 BASIC		1 27 BASIC	
H	018	026	0 46	0 66
J	008	012	0 20	0 30
L	220	252	5 59	6 40
M	0°	10°	0°	10°
N	000	012	0 00	0 30

θ_{JA} = 150°C/W

"M" Package—TO-99



NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3 2)

θ_{JA} = 150°C/W
θ_{JC} = 45°C/W

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	335	370	8 51	9 40
B	305	335	7 75	8 51
C	165	185	4 19	4 70
D	016	021	0 41	0 53
E	010	040	0 25	1 02
F	010	040	0 25	1 02
G	200 BASIC		5 08 BASIC	
H	028	034	0 71	0 86
J	029	045	0 74	1 14
K	500	—	12 7	—
L	110	160	2 79	4 06
M	45° BASIC		45° BASIC	
N	095	105	2 41	2 67

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Power Dissipation (Package Limitation) 500mW
Junction Temperature, $T_{J\ MAX}$
AM ..... 125°C
JP, JU ..... 100°C
Operating Temperature Range ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Input Voltage ..... Equal to Supply Voltage
Logic-to-Logic Reference Differential Voltage[1] ..... +7V, −30V
Output Short Circuit Duration ..... Indefinite
Hold Capacitor Short Circuit Duration 10s
Lead Temperature (soldering, 10s) ..... 300°C

NOTE (1) Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply

BURN-IN SCREENING

Burn-in screening is available for both plastic and TO-99 metal can packages. Burn-in duration is 160 hours at the temperature (or equivalent combination of time and temperature) indicated below:

Plastic "-BI" models: +85°C
TO-99 "-BI" models: +125°C

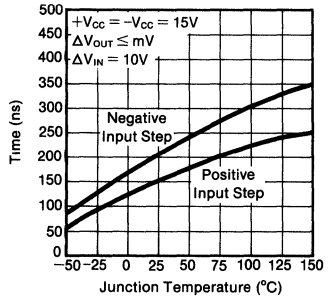
All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

ORDERING INFORMATION

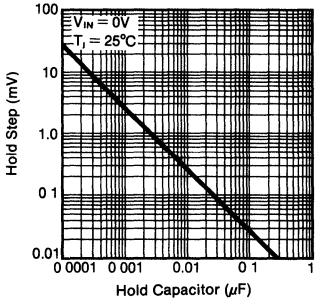
Model	Package	Temperature Range
SHC298AM	TO-99	-25°C to +85°C
SHC298JP	8-pin DIP	0°C to +70°C
SHC298JU	8-lead SOIC	0°C to +70°C
SHC298AJP	8-pin DIP	0°C to +70°C
BURN-IN SCREENING OPTION See text for details		
Model	**Package**	**Temperature Range**
SHC298AM-BI	TO-99	-25°C to +85°C
SHC298JP-BI	8-pin DIP	0°C to +70°C
SHC298JU-BI	8-lead SOIC	0°C to +70°C
SHC298AJP-BI	8-pin DIP	0°C to +70°C

TYPICAL PERFORMANCE CURVES

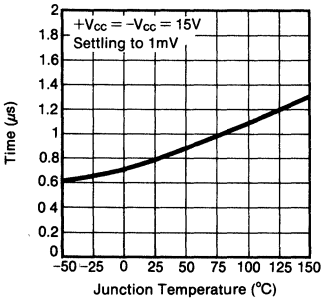
APERTURE TIME



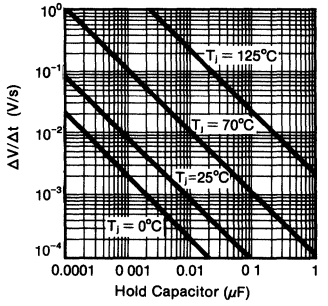
CHARGE OFFSET



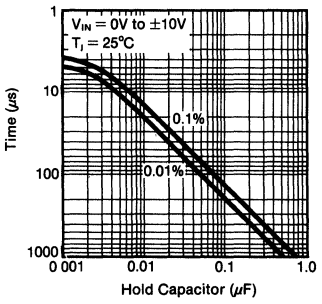
SAMPLE-TO-HOLD TRANSIENT SETTLING TIME



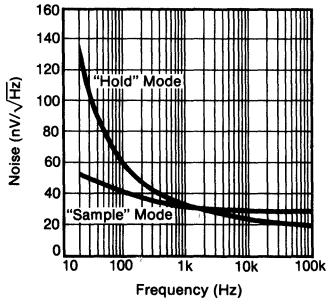
OUTPUT DROOP RATE

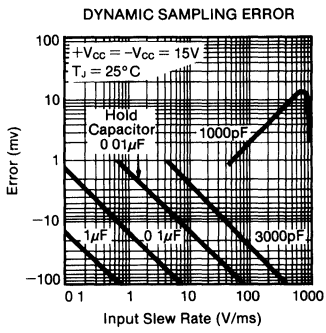


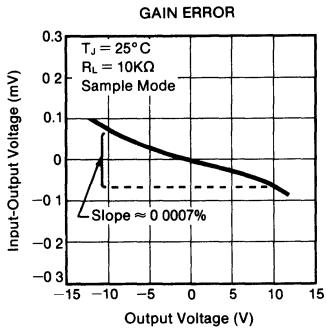
ACQUISITION TIME

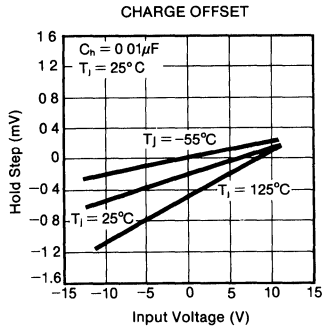


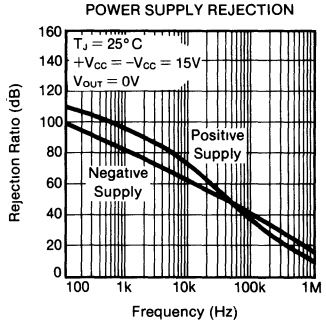
OUTPUT NOISE

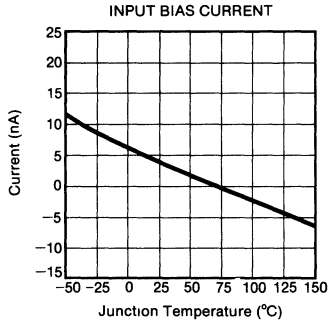


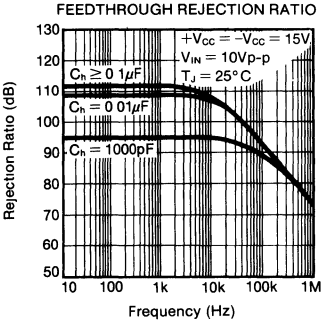


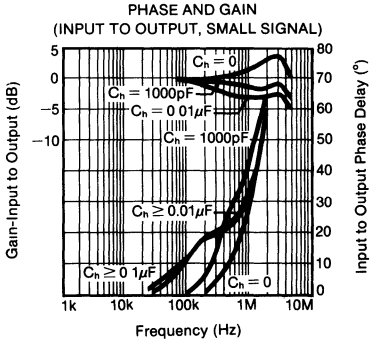


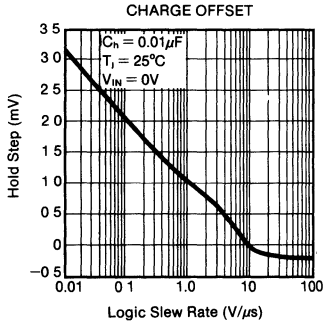












DISCUSSION OF SPECIFICATIONS

THROUGHPUT NONLINEARITY

Throughput nonlinearity is defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, 1ms of droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by offset and gain adjustments. Throughput nonlinearity is tested with a 1000pF holding capacitor, 10V input changes, 10μs acquisition time, and 1ms Hold time (see Figure 1).

GAIN ACCURACY

Gain Accuracy is the difference between Input and Output voltage (when in the Sample mode) due to amplifier gain errors.

DROOP RATE

Droop Rate is the voltage decay at the output when in the Hold mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH

Feedthrough is the amount of the input voltage change that appears at the output when the amplifier is in the Hold mode.

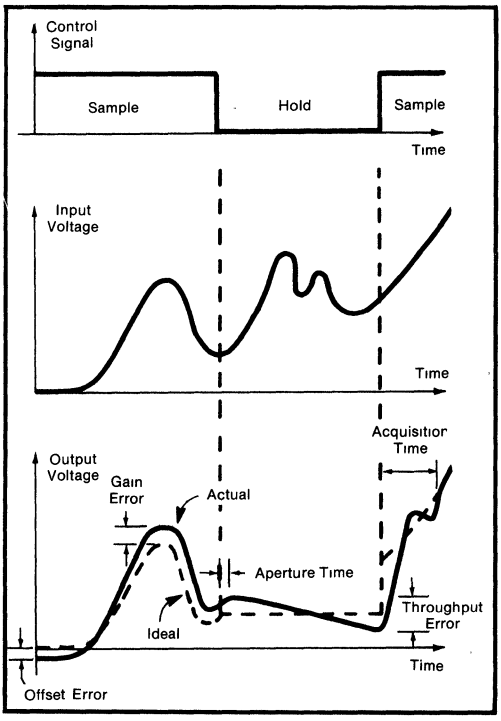


FIGURE 1. Sample Hold Errors.

APERTURE TIME

Aperture Time is the time required to switch from Sample to Hold. The time is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

ACQUISITION TIME

Acquisition Time is the time required for the sample/hold output to settle within a given error band of its final value when the mode control is switched from Hold to Sample.

CHARGE OFFSET

Charge Offset is the offset that results from the charge coupled through the gate capacitance of the switching FET. This charge is coupled into the storage capacitor when the FET is switched to the "hold" mode.

OPERATING INSTRUCTIONS

EXTERNAL CAPACITOR SELECTION

Capacitors with high insulation resistance and low dielectric absorption, such as teflon, polystyrene or polypropylene units, should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize AC and DC leakage currents from the capacitor to reduce chage offset and droop errors.

The value of the external capacitor determines the droop, charge offset and acquisition time of the Sample/Hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table for a 0.001μF capacitor. With a capacitor of 0.01μF the droop will reduce to approximately 2.5μV/ms and the charge offset to approximately 1.5mV. The behavior of acquisition time with changes in external capacitance is shown in the Typical Performance Curves.

OFFSET ADJUSTMENT

The offset should be adjusted with the input grounded. During the adjustment, the sample/hold should be switching continuously between the Sample and the Hold mode. The error should then be adjusted to zero when the unit is in the Hold mode. In this way, charge offset as well as amplifier offset will be adjusted. When a 0.001μF capacitor is used, it will not be possible to adjust the full offset error at the sample/hold. It should be adjusted elsewhere in the system.

APPLICATIONS

DATA ACQUISITION

The SHC298 may be used to hold data for conversion with an analog-to-digital converter or used to provide Pulse Amplitude Modulation (PAM) data output (see Figures 2 and 3).

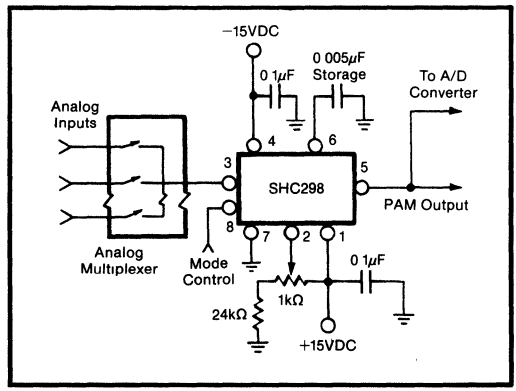


FIGURE 2. Data Acquisition.

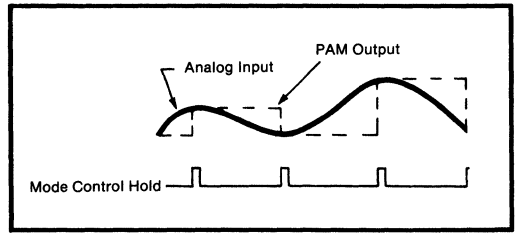


FIGURE 3. PAM Output.

DATA DISTRIBUTION

The SHC298 may be used to hold the output of a digital-to-analog converter whose digital inputs are multiplexed (see Figure 4).

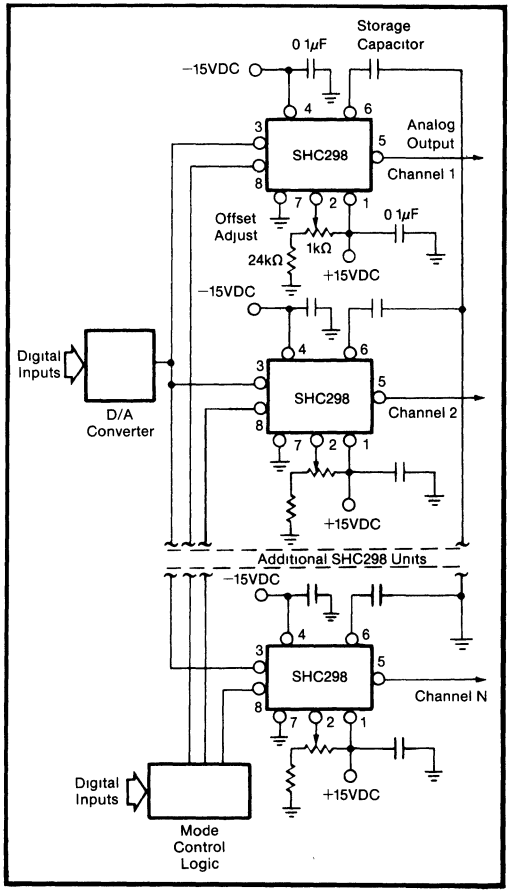


FIGURE 4. Data Distribution.

TEST SYSTEMS

The SHC298 is also well suited for use in test systems to acquire and hold data transients for human operators or for other parts of the test system such as comparators, digital voltmeters, etc.

With a 0.1μF storage capacitor, the output may be held 10 seconds with less than 0.1% error. With a 1μF storage capacitor, the output may be held more than 15 minutes with less than 1% error.

CAPACITIVE LOADING

SHC298 is sensitive to capacitive loading on the output and may oscillate. When driving long lines, a buffer should be used.

HIGH SPEED DATA ACQUISITION

The minimum sample time for one channel in a data acquisition system is usually considered to be the acquisition time of the sample/hold plus the conversion time of the analog-to-digital converter. If two or more sample/holds are used with a high-speed multiplexer, the acquisition time of the sample/hold can be virtually eliminated. While the first channel is in hold and switched on to the ADC, the multiplexer may be addressed to the next channel. The second sample/hold will have acquired this data by the time the conversion is complete. Then, the sample/holds reverse roles and another channel is addressed (see Figure 5) Fow low-level systems, and instrumentation amplifier and double-ended multiplexer may be connected to the sample/hold inputs. The settling time of the multiplexer, instrumentation amplifier, and sample/hold can be eliminated from the channel conversion time as before.

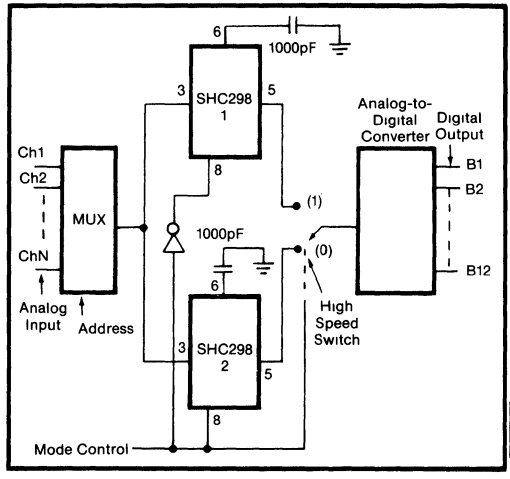


FIGURE 5 "Ping-Pong" Sample Holds.

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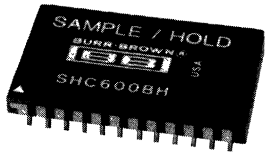


SHC600BH

Ultra-High Speed SAMPLE/HOLD AMPLIFIER

FEATURES

- CLOSED-LOOP OUTPUT AMPLIFIER
- ±0.01% FSR LINEARITY max
- ACQUISITION TIME (2.5V STEP):
  1% FSR 17ns typ
  0.1% FSR 27ns typ
  0.02% FSR 40ns typ
- 300V/μs SLEW RATE
- 24-PIN CERAMIC DIP
- VERY LOW DISTORTION

APPLICATIONS

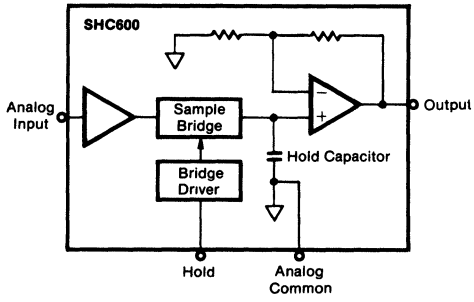
- SUCCESSIVE-APPROXIMATION ADCs
- IMPROVING FLASH ADCs
- WAVEFORM DIGITIZERS
- VIDEO
- PEAK DETECTORS
- BOXCAR INTEGRATORS
- DOWN CONVERTERS

DESCRIPTION

The SHC600 is a high speed sample/hold amplifier designed for use in ultra-fast, 12-bit data acquisition and signal processing systems. It acquires input step changes of 2.5V to 1% accuracy in 17ns and 0.02% accuracy in 40ns, typically. The closed-loop output amplifier provides a maximum linearity error of ±0.01% with a low output impedance of 0.4Ω. The gain has been optimized to drive 100Ω loads with a gain error of less than ±0.1%.

In the sample mode the SHC600 operates as a unity-gain buffer with a small signal bandwidth of 70MHz. Input voltage range is ±2V.

The hold command is ECL-compatible.



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PDS-644A

SPECIFICATIONS

ELECTRICAL

At +25°C and rated power supplies and 100Ω in parallel with 3pF load unless otherwise specified

PARAMETER	SHC600BH MIN	SHC600BH TYP	SHC600BH MAX	UNITS
SAMPLE/HOLD INPUTS				
ANALOG				
Voltage Range		±1.25	±2	V
R_{IN}		1.5		MΩ
Input Bias Current		20	35	μA
DIGITAL (ECL Compatible)				
V_{IH} (HOLD)	−1.1		−0.8	V
V_{IL} (SAMPLE)	−1.8		−1 5	V
I_{IH}, V_{IN} = −1 1V			265	μA
I_{IL}, V_{IN} = −1 8V	0.5			μA
SAMPLE/HOLD OUTPUT				
Voltage Range		±1 25	±2	V
Output Current	±40			mA
Short Circuit Protection		Momentary (1s)		
Output Impedance (at DC)		0 4		Ω
Noise in Track Mode (wideband 200MHz into 50Ω load)		400		μVrms
SAMPLE/HOLD TRANSFER CHARACTERISTICS				
DC ACCURACY/STABILITY				
Gain		+1		V/V
Gain Error		±0.1		%
Temperature Coefficient		±5	±20	ppm/°C
Linearity Error (±1 25V Input)		±0.002	±0 01	% of FSR[1]
Zero Offset		±2	±5	mV
Temperature Coefficient		±50	±150	μV/°C
Power Supply Sensitivity of Offset: V_{DD1} (+5V)		±1	±3	mV/V
V_{DD2} (−5 2V)		±4	±13	mV/V
$+V_{CC}$ (+15V)		±5	±10	mV/V
$-V_{CC}$ (−15V)		±9	±15	mV/V
HOLD-TO-TRACK (SAMPLE) DYNAMICS				
Acquisition Time (with 2 5V step)[1] To within ±1% of FSR (25mV)		17	25	ns
To within ±0 1% of FSR (2.5mV)		27	35	ns
To within ±0 02% of FSR (0.5mV)		40	50	ns
Switch Delay Time		2		ns
TRACK (SAMPLE)-TO-HOLD DYNAMICS				
Aperture Delay Time		4	8	ns
Aperture Uncertainty (jitter)		5	9	ps (rms)
Offset Step (pedestal)		±2	±10	mV
Temperature Coefficient		±30	±60	μV/°C
Sensitivity to V_{DD2} (−5.2V)		±2.5	±10	mV/V
Switch Delay Time		2		ns
SwitchingTransient Amplitude		7	20	mVpk
Settling to within ±1mV		10	15	ns
TRACK (SAMPLE) MODE DYNAMICS				
Frequency Response: Full Power Bandwidth		40		MHz
Small Signal Bandwidth		70		MHz
Output Slew Rate	200	300		V/μs
Harmonic Distortion (2.5Vp-p input at 4MHz). R_L = 200Ω		−78		dB
R_L = 50Ω		−65		dB
HOLD MODE DYNAMICS				
Droop Rate at +25°C case temp		±60	±180	μV/μs
at +85°C case temp		±1 5	±4	mV/μs
Feedthrough Rejection. 2.5V p-p input at 1MHz	62			dB
at 10MHz	58			dB
POWER SUPPLY REQUIREMENTS				
Supply Voltages. V_{DD1}	+4.75	+5.0	+5.25	V
V_{DD2}	−4.95	−5.2	−5.46	V
$+V_{CC}$	+14.25	+15	+15 75	V
$-V_{CC}$	−14.25	−15	−15 75	V
Quiescent Current: V_{DD1}		40	55	mA
V_{DD2}		−93	−120	mA
$+V_{CC}$		30	45	mA
$-V_{CC}$		−15	−25	mA
Power Dissipation		1.3	2.0	W
TEMPERATURE RANGE				
Specification (case temperature)	−25		+85	°C
Storage	−55		+125	°C

NOTES: (1) FSR means Full-Scale Range. For SHC600 FSR= 2.5V.

PIN ASSIGNMENTS

1	V_{DD1} (+5V)	13	Analog Input
2	V_{DD2} (−5 2V)	14	NIC*
3	NIC*	15	NIC*
4	V_{DD2} (−5.2V)	16	NIC*
5	Hold Command	17	NIC*
6	Digital Common	18	Analog Common
7	Power Common	19	Analog Common
8	$+V_{CC}$ (+15V)	20	NIC*
9	NIC*	21	NIC*
10	V_{DD2} (−5.2V)	22	$+V_{CC}$ (+15V)
11	Power Common	23	NIC*
12	$-V_{CC}$ (−15V)	24	Analog Output

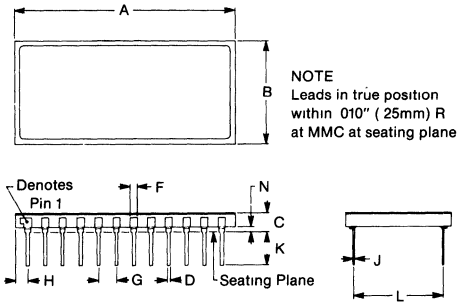
* NIC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	16 5V
V_{DD1}	+7.0V
V_{DD2}	−7 0V
Analog Input	±5 0V
Logic Input	V_{DD2} to +0 5V
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	−40°C to +100°C

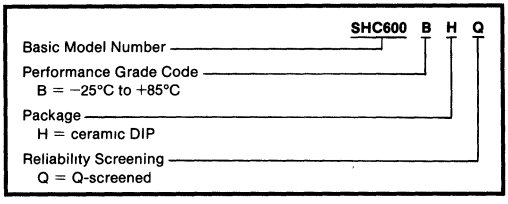
Stresses above these ratings may cause permanent damage to the device.

MECHANICAL



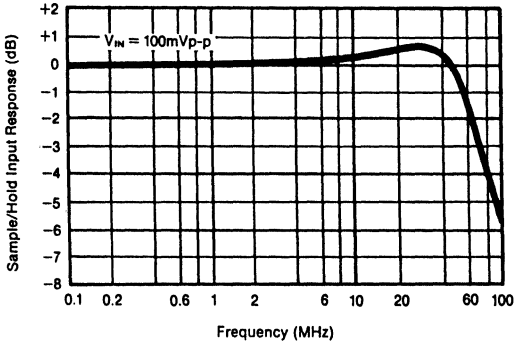
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 280	1 310	32 51	33 27
B	780	800	19 81	20 32
C	153	207	3 89	5 26
D	016	020	41	51
F	045	055	1 14	1 40
G	100 BASIC		2 54 BASIC	
H	087	091	2 21	2 31
J	009	012	23	30
K	200	210	5 08	5 33
L	600 BASIC		15 24 BASIC	
N	015	035	38	89

ORDERING INFORMATION



TYPICAL PERFORMANCE CURVE

ANALOG INPUT BANDWIDTH



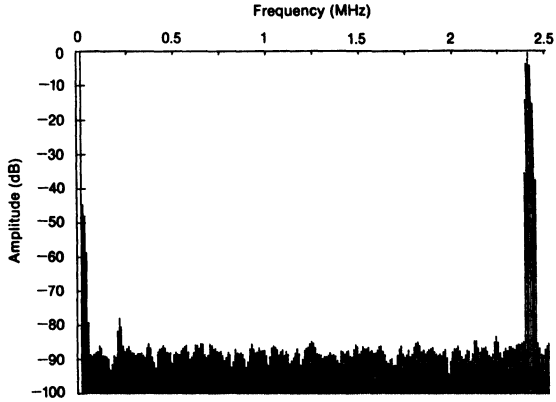
THEORY OF OPERATION

The SHC600 is a high-speed sample/hold amplifier with low distortion, fast acquisition time and very low aperture uncertainty (jitter). A diode bridge sampling switch is used to achieve an acceptable compromise between speed and accuracy. The diode bridge switching transients are buffered from the analog input by a high input impedance buffer amplifier. Since the hold capacitor does not appear in the feedback of the diode bridge output buffer, the capacitor can acquire the signal in 25ns. The low-bias-current output buffer droop appears as only an offset error and does not affect linearity.

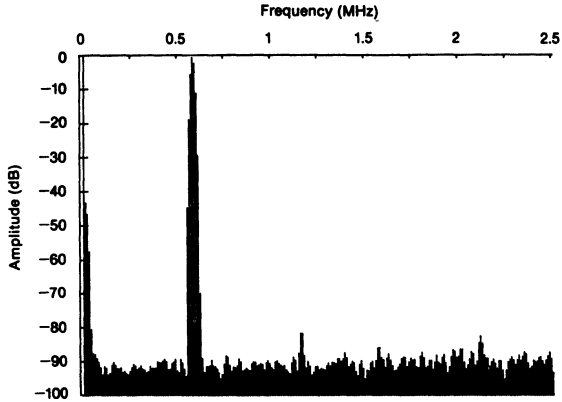
TYPICAL FFT SPECTRAL PERFORMANCE

All FFT data: 512-point FFT, 10-sample average; minimum 4-sample Blackman-Harris Window. Tested in ADC600K high speed ADC.

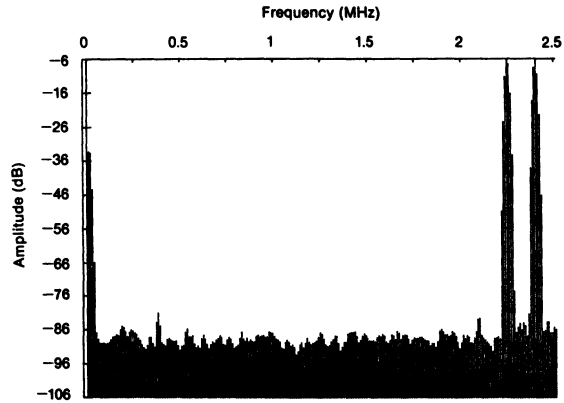
Sample Rate = 5MHz, Input Voltage = Full-Scale (0dB)



	Level re: Full-Scale (dB)
2.4121MHz Fundamental =	−0.6
Harmonics: 2f =	−77.9
3f =	−83.1
4f =	−85.3
SINAD =	67.3dB
TND =	−68.5dBC
THD =	−73.3dBC



	Level re: Full-Scale (dB)
0.5859MHz Fundamental =	−0.7
Harmonics: 2f =	−81.4
3f =	−87.2
4f =	−87.0
SINAD =	69.6dB
TND =	−70.7dBC
THD =	−76.1dBC



	Level re: Full-Scale (dB)
F_1: 2.2461MHz =	−6.3
F_2: 2.4023MHz =	−6.4
Peak Envelope =	−0.7
IMD: 0.3809MHz =	−81.2
2.0996MHz =	−82.9
2.4707MHz =	−83.9

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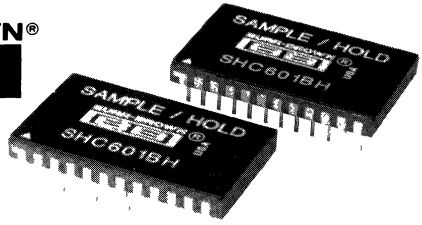


SHC601BH

Ultra-High Speed SAMPLE/HOLD AMPLIFIER

FEATURES

- 100MHz SAMPLE RATE
- ±0.02% MAX LINEARITY ERROR
- ACQUISITION TIME (2.5V STEP):
  1% FSR 8ns
  0.1% FSR 12ns
  0.02% FSR 22ns
- 350V/μs SLEW RATE
- 900 FEMTO SECONDS RMS APERTURE UNCERTAINTY
- REPLACES HTS-0010

APPLICATIONS

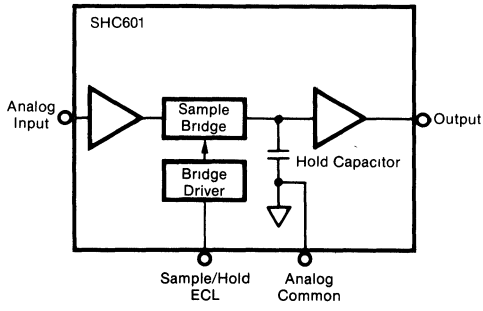
- IMPROVING FLASH ADCs
- WAVEFORM DIGITIZERS
- VIDEO PROCESSORS
- PEAK DETECTORS
- BOXCAR INTEGRATORS
- DOWN CONVERTERS
- DAC DEGLITCHING

DESCRIPTION

The SHC 601 is a high speed sample/hold amplifier designed for use in ultra-fast, 12-bit data acquisition and signal processing systems. It acquires input step changes of 2.5V to 1% accuracy in 8ns and 0.02% accuracy in 22ns, typically. The open-loop output amplifier provides a maximum linearity error of ±0.02% with an output impedance of 10Ω.

A 100MHz sample rate and extremely low aperture uncertainty (0.9ps rms) make the SHC601 suitable for RF signal processing applications.

In the sample (track) mode the SHC601 operates as a unity-gain buffer with a small signal bandwidth of 115MHz.



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PDS-784

SPECIFICATIONS

ELECTRICAL

At +25°C ambient temperature, 10 SCFM airflow, and rated power supplies unless otherwise specified

PARAMETER	SHC601BH MIN	SHC601BH TYP	SHC601BH MAX	UNITS
SAMPLE/HOLD INPUTS				
ANALOG				
Voltage Range		±1 25	±2	V
R_{IN}		100		kΩ
Input Bias Current		25	75	μA
DIGITAL (ECL Compatible) V_{IH} (HOLD)	−1 1		−0.8	V
V_{IL} (SAMPLE)	−1 8		−1 5	V
I_{IH}, V_{IN} = −1 1V			265	μA
I_{IL}, V_{IN} = −1 8V	0 5			μA
SAMPLE/HOLD OUTPUT				
Voltage Range		±1 25	±2	V
Output Current	±40			mA
Short Circuit Protection		None		
Output Impedance (at DC)		10		Ω
Noise in Track Mode (wideband 100MHz into 50Ω load)		400		μVrms
SAMPLE/HOLD TRANSFER CHARACTERISTICS				
DC ACCURACY/STABILITY				
Gain, $R_L = \infty$[1]	0 96	0 98	1 00	V/V
Gain Temperature Coefficient		±28	±40	ppm/°C
Linearity Error (±1 25V Input)		±0 0095	±0 02	% of FSR[2]
Zero Offset		±2	±5	mV
Temperature Coefficient		±80	±175	μV/°C
Power Supply Sensitivity of Offset V_{DD1} (+5V)		±2		mV/V
V_{DD2} (−5 2V)		±4		mV/V
$+V_{CC}$ (+15V)		±11		mV/V
$-V_{CC}$ (−15V)		±20		mV/V
HOLD-TO-TRACK (SAMPLE) DYNAMICS; R_L = 100Ω, C_L = 3pF				
Acquisition Time (with 2 5V step)[2]. To within ±1% of FSR (25mV)		8	11	ns
To within ±0 1% of FSR (2 5mV)		12	16	ns
To within ±0 02% of FSR (0 5mV)		22		ns
Switch Delay Time		1 5		ns
TRACK (SAMPLE)-TO-HOLD DYNAMICS; R_L = 100Ω, C_L = 3pF				
Aperture Delay Time		4	7	ns
Aperture Uncertainty (Jitter)		0 9		ps (rms)
Offset Step (pedestal)		±5	±20	mV
Temperature Coefficient		±50	±140	μV/°C
Sensitivity to V_{DD2} (−5 2V)		±0 6		mV/V
Switch Delay Time		1 5		ns
SwitchingTransient Amplitude		7	25	mVpk
Settling to within ±1mV		9	14	ns
TRACK (SAMPLE) MODE DYNAMICS				
Frequency Response Full Power Bandwidth (V_O = 2 5Vp-p)	38	45		MHz
Small Signal Bandwidth (V_O = 100mVp-p)	100	115		MHz
Output Slew Rate	±300	±350		V/μs
Harmonic Distortion (2Vp-p input at 20MHz) $R_L \geq 250\Omega$		−55		dBC
HOLD MODE DYNAMICS				
Droop Rate at +25°C case temp		±20	±100	μV/μs
at +85°C case temp		±0 9	±2	mV/μs
Feedthrough Rejection 2 5Vp-p input, R_L = 100Ω, C_L = 3pF at 10MHz	65	77		dB
POWER SUPPLY REQUIREMENTS				
Supply Voltages V_{DD1}	+4 75	+5 0	+5 25	V
V_{DD2}	−4 95	−5 2	−5 4	V
$+V_{CC}$	+14 25	+15	+15 75	V
$-V_{CC}$	−14 25	−15	−15 75	V
Quiescent Current V_{DD1} (+5V)		16	25	mA
V_{DD2} (−5 2V)		60	85	mA
$+V_{CC}$ (+15V)		30	40	mA
$-V_{CC}$ (−15V)		27	40	mA
Power Dissipation (I_{OUT} = 0mA)		1 25	1 7	W
TEMPERATURE RANGE				
Specification[3]	−25		+85	°C
Storage	−55		+125	°C

NOTES (1) Gain Accuracy Gain = R_L (0 98V/V)/(R_L + 10Ω) (2) FSR means Full-Scale Range For SHC601 FSR= 2 5V (3) SHC601BH is tested and specified in a forced air environment with a 10 SCFM airflow For a normal convection environment θ_{JC} = 28 7°C/W and θ_{CA} = 23 3°C/W Case temperature is measured on top surface of package

PIN ASSIGNMENTS

1	V_{DD1} (+5V)	13	Analog Input
2	V_{DD2} (−5 2V)	14	NIC*
3	NIC*	15	NIC*
4	V_{DD2} (−5 2V)	16	NIC*
5	Hold Command	17	NIC*
6	Digital Common	18	Analog Common
7	Power Common	19	Analog Common
8	$+V_{CC}$ (+15V)	20	NIC*
9	NIC*	21	NIC*
10	V_{DD2} (−5 2V)	22	$+V_{CC}$ (+15V)
11	Power Common	23	NIC*
12	$-V_{CC}$ (−15V)	24	Analog Output

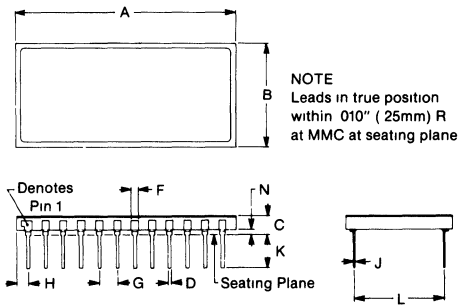
* NIC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$	16 5V
V_{DD1}	+7 0V
V_{DD2}	−7 0V
Analog Input	±5 0V
Logic Input	V_{DD2} to +0 5V
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	−40°C to +100°C

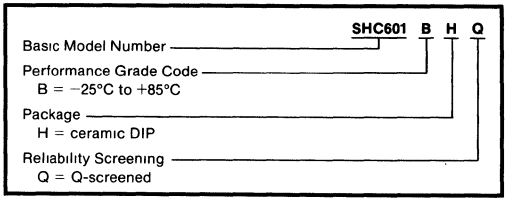
Stresses above these ratings may cause permanent damage to the device.

MECHANICAL



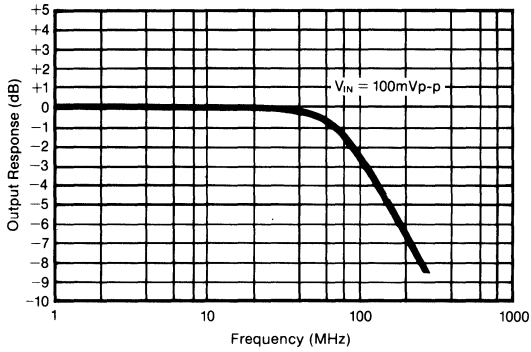
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 280	1 310	32 51	33 27
B	780	800	19 81	20 32
C	153	207	3 89	5 26
D	016	020	41	51
F	045	055	1 14	1 40
G	100 BASIC		2 54 BASIC	
H	087	091	2 21	2 31
J	009	012	23	30
K	200	210	5 08	5 33
L	600 BASIC		15 24 BASIC	
N	015	035	38	89

ORDERING INFORMATION

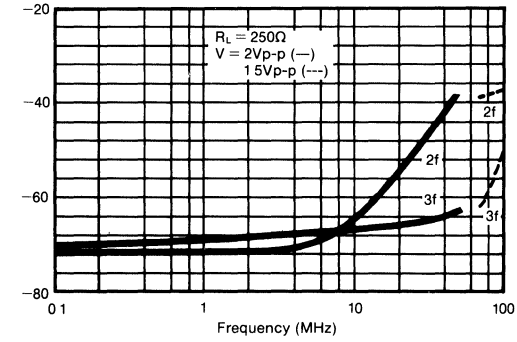


TYPICAL PERFORMANCE CURVES

ANALOG INPUT BANDWIDTH



HARMONIC DISTORTION VS FREQUENCY



THEORY OF OPERATION

The SHC601 is a high-speed sample/hold amplifier with low distortion, fast acquisition time and very low aperture uncertainty (jitter). A diode bridge sampling switch is used to achieve an acceptable compromise between speed and accuracy. The diode bridge switching transients are buffered from the analog input by a high input impedance buffer amplifier. Since the hold capacitor does not appear in the feedback of the diode bridge output buffer, the capacitor can acquire the signal in 8ns. The low-bias-current output buffer droop appears only as an offset error and does not affect linearity.

LAYOUT

Each power supply pin should be bypassed with a 1μF tantalum capacitor connected directly from each pin to a heavy copper ground plane. All unused pins should be connected to ground and input and output connections should be short and direct in keeping with the high frequency performance of the SHC601.

Good RF layout techniques should be used—a heavy two ounce copper ground plane is strongly recommended. Wire-wrap or "prototype" boards will not give satisfactory performance.

Longer input/output traces or capacitive loads (such as a flash ADC) may require decoupling with a series resistor of 10Ω to 50Ω.

DISCUSSION OF PERFORMANCE

HARMONIC DISTORTION

Figure 1 shows the harmonic distortion at various frequency ranges. Figure 2 is a block diagram of the Harmonic Distortion Test.

APERTURE JITTER

An ECL signal with rising and falling edges of 1V/ns is applied to both the S/H input and the analog input (see Figure 3). A delay line is used to compensate for the aperture delay time and can be made up of various coax lengths or by using a calibrated line such as an Allen Avionics Model VRM011. Because of the variation in the other cable lengths, coax (A) length may have to be adjusted to locate the sample and hold point at the midpoint of the signal transition.

In this test the midpoint of the ECL signal is held; approximately −1.3V. Once the cable delays have been adjusted, the scope presentation will consist of noise due to aperture jitter on the held value of −1.3V. The peak-to-peak value of the noise band around the held value, divided by four, gives the approximate rms value of the noise. When divided by the rate of change of the input signal, the result will be aperture jitter.

It is important that the rate of change used is the effective slew rate seen at the switching mechanism inside the SHC601. For example, this signal will be slower than the pulse generator slew rate due to the slew rate limitations of an input buffer. The effective slew rate is determined by measuring the amount the held value changes versus a known change in delay of the delay line.

For example:

Effective Slew Rate = 0.35V/ns

Noise band = 1.4mVp-p = 0.35mVrms

If rms noise is in mV and slew rate in V/ns, the jitter will be in ps rms:

(0.35mVrms) ÷ (0.35V/ns) = 1ps rms

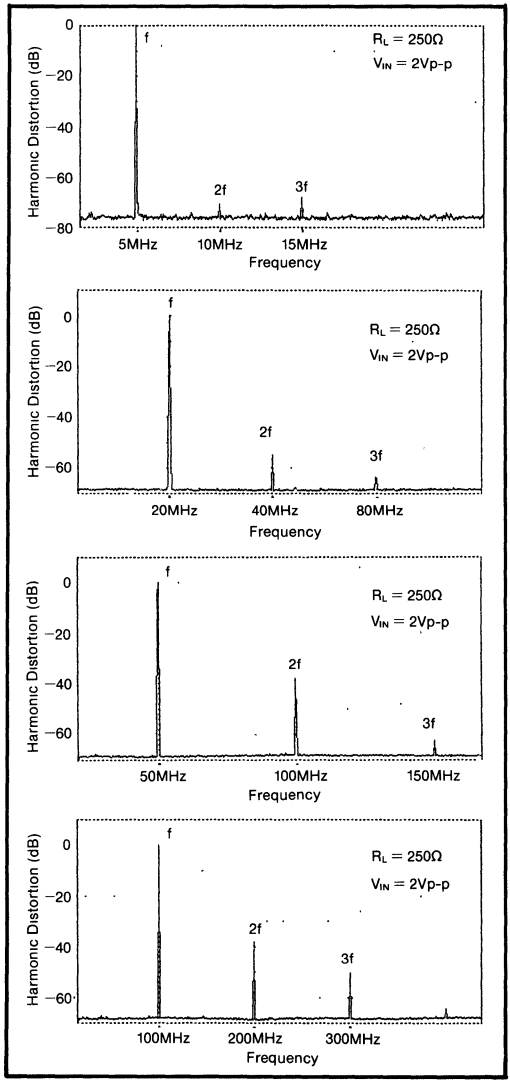


Figure 1. Harmonic Distortion vs Frequency.

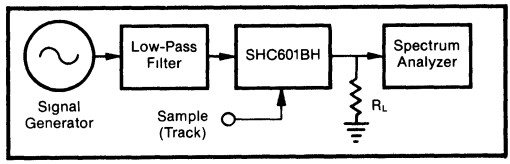


Figure 2. Harmonic Distortion Test Block Diagram.

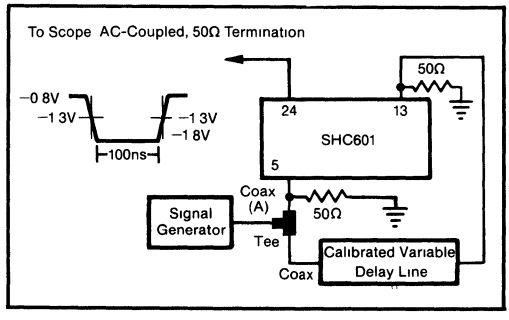


Figure 3. Aperture Jitter Test Circuit.

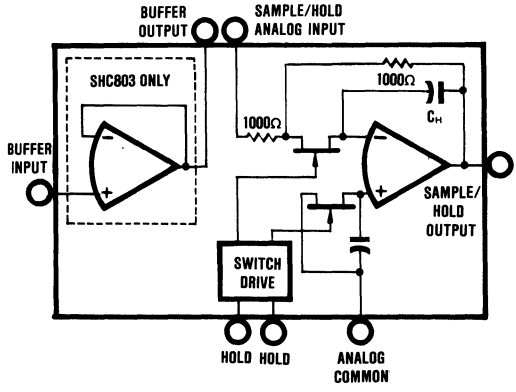
BURR-BROWN®

SHC803BM, CM
SHC804BM, CM

Ultra-High Speed SAMPLE/HOLD AMPLIFIER

FEATURES

- 350nsec max ACQUISITION TIME
- ±0.01% THROUGHPUT NONLINEARITY
- 150nsec max SAMPLE-TO-HOLD SETTLING TIME
- INPUT BUFFER (SHC803)
- 24-PIN HERMETICALLY-SEALED METAL PACKAGE



DESCRIPTION

The SHC803 and SHC804 are high speed sample/hold amplifiers designed for use in fast 12-bit data acquisition systems and signal processing systems. The SHC803 contains a fast-settling unity-gain amplifier for buffering high impedance sources or for use with CMOS multiplexers.

The SHC804 acquires a 10V signal change in less than 350nsec to ±1/2LSB at 12 bits. Throughput nonlinearity error is guaranteed to be within ±1/2LSB for 12-bit systems. Stability over temperature is excellent, with only ±5ppm/°C of gain drift and ±4ppm of FSR/°C of charge offset drift over the −25 to +85°C temperature range.

The ±25psec maximum aperture uncertainty of SHC803 and SHC804 permits sampling (to ±0.01% of Full Scale Range) of signals with rates of change of up to 100V/μsec. These sample/holds have been optimized for use with Burr-Brown's high speed 12-bit analog-to-digital converter, model ADC803. Together these components are capable of accurately digitizing fast changing signals at sample rates as high as 500k samples per second.

The digital inputs (HOLD and $\overline{\text{HOLD}}$) are TTL-compatible. Power supply requirements are ±15V and +5V and the specification temperature range is −25°C to +85°C. The SHC803 and SHC804 are packaged in a 24-pin dual-in-line hermetic metal package. SHC804 is pin-compatible with other sample/holds on the market with similar performance characteristics.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-512C

SPECIFICATIONS

ELECTRICAL

At +25°C, rated power supplies and a 1kΩ output load unless otherwise specified

MODEL	SHC803/SHC804BM			SHC803/804CM			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
SAMPLE/HOLD INPUTS [without input buffer]							
ANALOG							
Voltage Range	±10.25	±11		*	*		V
R_{IN}		1.00			*		kΩ
DIGITAL [HOLD, $\overline{HOLD}$]							
V_{IH}	+2.0			*			V
V_{IL}			+0.8			*	V
I_{IH}, V_{IN} = +2.7V			+60			*	µA
I_{IL}, V_{IN} = +0.4V			−1.2			*	mA
SAMPLE/HOLD TRANSFER CHARACTERISTICS [without input buffer]							
ACCURACY							
Sample Mode							
Gain		−1			*		V/V
Gain Error			±0.1			*	%
Temperature Coefficient		±3	±10		±1	±5	ppm/°C
Linearity Error		±0.001	±0.005		*	*	% of FSR[1]
Zero Offset		±1	±5		±0.5	±3	mV
Temperature Coefficient		±1	±2.5		±0.5	±1.5	ppm of FSR/°C
Hold Mode							
Charge Offset		±2	±10		±1	±5	mV
Temperature Coefficient		±3	±10		±2	±4	ppm of FSR/°C
Droop Rate at +25°C		±0.5	±5		*	*	µV/µsec
+85°C			±0.5			±0.1	mV/µsec
Throughput Nonlinearity			±0.01			*	% of FSR
Power Supply Sensitivity[2] $\pm V_{CC}$			±0.002			*	% of FSR/%V_{CC}
V_{DD}			±0.003			*	% of FSR/%V_{DD}
DYNAMIC CHARACTERISTICS							
Acquisition Time (with 10V step)							
to within ±0.1% (±10mV)		220			*		nsec
±0.01% (±1mV)		250	350		*	*	nsec
Sample-to-Hold Settling Time							
to within ±0.01% (±1mV)		100	150		*	*	nsec
Sample-to-Hold Transient Amplitude		60	150		*	*	mV_{peak}
Aperture Delay Time[3]		15	25		*	*	nsec
Aperture Uncertainty		±10	±25		*	*	psec
Sample Mode. Output Slew Rate		160			*		V/µsec
Full Power Bandwidth		1			*		MHz
Small Signal Bandwidth		16			*		MHz
Hold Mode Feedthrough Rejection							
(10V square wave input)	±0.03	±0.005		*	*		%
SAMPLE/HOLD OUTPUT							
Voltage Range	±10.25	±11		*	*		V
Output Current	±50			*			mA
Short Circuit Protection		Indefinite to Common			*		
Output Impedance (at DC)		0.01	0.1		*	*	Ω
INPUT BUFFER CHARACTERISTICS [SHC803 only]							
INPUT							
Offset Voltage		±1/2	±5		*	*	mV
vs Temperature		±1.5	±2.5		*	*	ppm of FSR/°C
Bias Current			±25			*	nA
Impedance		10^9‖5			*		Ω‖pF
V_{IN} Range	±10.25	±11		*	*		V
DYNAMIC CHARACTERISTICS							
Full Power Bandwidth		320			*		kHz
Slew Rate[4]		10			*		V/µsec
Settling Time[4] to ±2mV for 10V Step		2.5			*		µsec
OUTPUT							
V_{OUT} Range	±10.25			*			V
Output Current	±10.25			*			mA

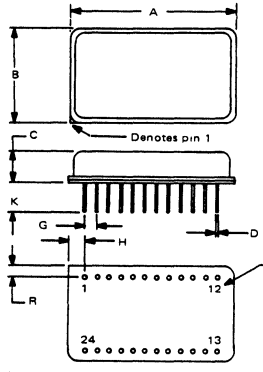
ELECTRICAL [CONT]

MODEL	SHC803/SHC804BM			SHC803/804CM			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS							
Rated Voltage ±V_{CC}	±13 5	±15	±16 5	*	*	*	V
V_{DD}	+4 75	+5 00	+5 25	*	*	*	V
Quiescent Current (no load)							
SHC804 +V_{CC}		30	35		*	*	mA
−V_{CC}		15	20		*	*	mA
V_{DD}		5	10		*	*	mA
SHC803 +V_{CC}		33	40		*	*	mA
−V_{CC}		18	25		*	*	mA
V_{DD}		5	10		*	*	mA
Power Dissipation SHC804		700	875		*	*	mW
SHC803		790	1100		*	*	mW
TEMPERATURE RANGE							
Specification	−25		+85	*		*	°C
Storage	−55		+125	*		*	°C

*Specification same as SHC803/SHC804BM.

NOTES (1) FSR means Full Scale Range and is 20V for SHC803 and SHC804 (2) Sensitivity of Offset plus Charge Offset (3) With respect to HOLD For $\overline{\text{HOLD}}$ add 5nsec typical (4) With buffer connected to the sample/hold amplifier

MECHANICAL



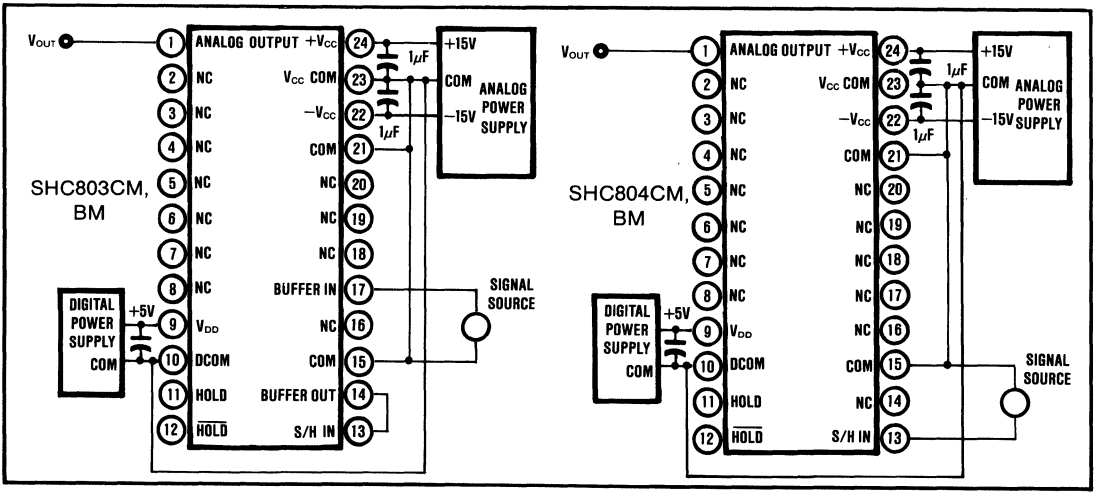
CASE Nickel-plated steel
MATING CONNECTOR 245MC
WEIGHT 8 4 grams (0.3oz)
HERMETICITY Conforms to method 1014 Condition C Step 1 (fluorocarbon) of MIL-STD-883 (gross leak)

Pin numbers shown for reference only
Numbers may not be marked on package

NOTE Leads in true position within .010" (.25mm) R at MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 365	1 385	34 67	35 18
B	790	810	20 07	20.57
C	170	250	4 32	6 35
D	016	021	0 41	0.53
G	100 BASIC		2 54 BASIC	
H	125	150	3 18	3 81
K	150	300	3 81	7 62
L	600 BASIC		15 24 BASIC	
R	080	110	2 03	2 79

CONNECTION DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Input Overvoltage ..... ±15V
$+V_{CC}$ to V_{CC} COMMON ..... 0 to +18V
$-V_{CC}$ to V_{CC} COMMON ..... 0 to −18V
Voltage on Digital Inputs
(pins 11 and 12) .....−0.5V to +7V
Power Dissipation 1500mW
V_{DD} to DCOM .....−0.5V
Analog Output .... Indefinite Short to V_{CC} COM

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PIN ASSIGNMENTS

Pin	Name	Description
1	Sample/Hold Output	Analog voltage output
2	NC	Not connected
3	NC	Not connected
4	NC	Not connected
5	NC	Not connected
6	NC	Not connected
7	NC	Not connected
8	NC	Not connected
9	V_{DD}	Logic supply
10	DCOM	Logic supply common
11	HOLD	Logic "1" = HOLD
12	$\overline{\text{HOLD}}$	Logic "0" = HOLD
13	S/H In	SHC804 input, for SHC803 connect pin 13 to pin 14
14	Buffer Out, SHC803 only	Not connected for SHC804
15	COM	Signal common
16	NC	Not connected
17	Buffer In, SHC803 only	Not connected for SHC804
18	NC	Not connected
19	NC	Not connected
20	NC	Not connected
21	COM	Signal Common
22	$-V_{CC}$	−15V supply
23	V_{CC} COM	Analog power common, connected to case
24	$+V_{CC}$	+15V supply

DISCUSSION OF SPECIFICATIONS

Throughput Nonlinearity is defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by Offset and Gain adjustments.

Gain Error is the difference between the input and output voltage magnitude (in the Sample mode) due to the amplifier gain errors.

Droop Rate is the voltage decay at the output when in the Hold mode due to storage capacitor and FET switch leakage current and the input bias current of the output amplifier.

Feedthrough is the amount of output voltage change caused by an input voltage change when the sample/hold is in the Hold mode.

Aperture Delay Time is the time required to switch from Sample to Hold. The time is measured from the 50% point of the Hold mode control transition to the time at which the output stops tracking the input.

Aperture Uncertainty Time is the nonrepeatibility of aperture delay time.

Acquisition Time is the time required for the sample/hold output to settle to within a given error band of its final value when the sample/hold is switched from Hold to Sample.

Charge Offset (Pedestal) is the output voltage change that results from charge coupled into the Hold capacitor through the gate capacitance of the switching field effect transistor. This charge appears as an offset at the output.

Sample-to-Hold Switching Transient is the switching transient which appears on the output when the sample/hold is switched from Sample to Hold. Both the magnitude and the settling time of the transient are specified.

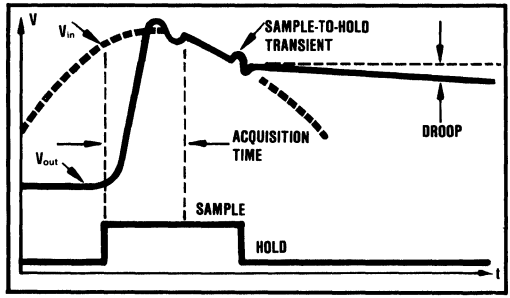


FIGURE 1. Definition of Acquisition Time, Droop and Sample-to-Hold Transient.

OPERATION

A simplified circuit diagram of SHC803/804 is shown on page 1. The SHC803 includes a noninverting unity-gain op amp to serve as a source-impedance buffer when the sample/hold is used with CMOS analog multiplexers. The SHC804 and SHC803 are identical except for this buffer.

In the Sample (track) mode the circuit acts as a unity-gain inverting amplifier. In the Hold mode, the capacitor, C_H, holds the value of the output at the time the unit was switched to the Hold mode. Additional circuits compensate for switching transients and provide switch leakage current cancellation. The amplifier provides high current drive and low output impedance to external loads.

GAIN, OFFSET, CHARGE OFFSET

SHC803 and SHC804 have been internally-trimmed to eliminate the need for external trim potentiometers for Gain, Offset (in Sample mode) and Charge Offset (Pedestal). System Gain and Offset errors can be adjusted elsewhere in the system, at an input amplifier preceding the sample/hold, or at an analog-to-digital converter following the sample/hold.

INSTALLATION

GROUNDING AND BYPASSING

SHC803 and SHC804 have four COMMON pins (pins 10, 15, 21, and 23) and all must be tied together and connected to the system analog common ($V_{CC}COM$) as close to the package as possible. It is preferable to have a large ground plane surrounding the sample/hold and have all four common pins soldered directly to it. Note that the metal case is internally connected to pin 23; therefore, care must be taken to avoid a ground loop if the case is allowed to contact the ground plane.

Most digital return currents pass through pin 10. Noise from the switch-drive circuit may couple directly into the main op amp summing junction, a very noise-sensitive node. Care must be taken to insure that no voltage differences occur between pin 10 and the other common pins. This is the reason pin 10 must be connected directly to the ground plane.

For the same reason, the logic supply should be kept as free of noise as possible. $\pm V_{CC}$ supply lines (pins 24 and 22) are internally bypassed to common with 0.01μF capacitors. It is recommended that the user install additional external 0.1μF to 1μF tantalum bypass capacitors at each supply pin.

SAMPLE/HOLD CONTROL

A TTL logic "0" at pin 11 (or a logic "1" at pin 12) switches the SHC803/804 into the Sample (track) mode. In this mode, the device acts as a unity-gain inverting amplifier, the output following the inverse of the input. A logic "1" at pin 11 (or a logic "0" at pin 12) will switch the SHC803/804 into the Hold mode. The output voltages will be held constant at the value present when the Hold command is given.

If pin 11 is used, pin 12 must be connected to the DCOM (pin 10). If pin 12 is used, pin 11 must be tied to V_{DD}. Using the HOLD and $\overline{\text{HOLD}}$ inputs as a logic function may adversely affect the charge offset (pedestal). A clean digital signal (no overshoot) at the HOLD or $\overline{\text{HOLD}}$ inputs will also reduce charge offset errors. Pins 11 and 12 present less than one standard TTL load (two LSTTL loads) to the digital drive circuit.

OUTPUT LOADING

Care must be taken when loading the output of the SHC803/804 to avoid possible oscillations, current limiting and performance variations over temperature.

The maximum capacitive load to avoid oscillations is about 300pF. Recommended resistive load is 500Ω or more, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω in parallel with capacitive loads up to 100pF. Higher capacitances will affect acquisition and settling times.

ANALOG SIGNAL SOURCE CONSIDERATIONS

The output impedance of the signal source driving the SHC804 will affect the accuracy of the sample and hold operation both statically (at DC) and dynamically. The ouput impedance of the signal source should be low and remain low over a wide bandwidth. A small capacitor at the driving source may help to improve the charge offset errors that are affected by dynamic source impedance.

SHC803 BUFFER AMPLIFIER

The buffer amplifier incorporated in the SHC803 provides appropriate drive characteristics to the sample/hold amplifier. Again a 20pF to 50pF capacitor added to the output of the buffer amplifier may improve charge offset performance.

The buffer amplifier is optimized for fast settling with $10V_{p-p}$ signals. However, for step input signals greater than 10V, a protection network (Figure 2) is required to prevent the buffer from overload, resulting in excessive settling time.

The data sheet for the Burr-Brown model ADC803 analog-to-digital converter contains a sample printed circuit board layout incorporating many of the above considerations.

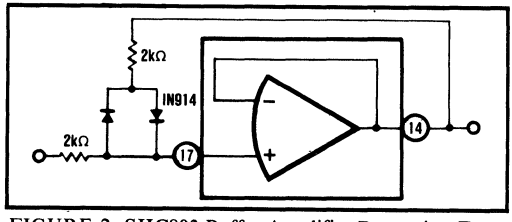


FIGURE 2. SHC803 Buffer Amplifier Protection For Input Steps Greater Than 10V.

APPLICATIONS

SIGNAL DIGITIZATION

Sample/hold amplifiers are commonly used to hold input voltages to an A/D converter constant during conversion. Digitizing errors result if the analog signal being digitized varies excessively during conversion.

For example, the Burr-Brown ADC803 is a 12-bit successive-approximation converter with a 1.5μsec conversion time. To insure the accuracy of the output data, the analog input signal to the A/D converter must not change more than 1/2LSB during the conversion.

The maximum rate of change for sine wave inputs is $dv/dt\ (max) = 2\pi Af(V/sec)$. If one allows a 1/2LSB change (2.44mV) for a ±10V input swing to the A/D converter, the allowable input rate-of-change limit would be 2.44mV/1.5μsec = 1.63mV/μsec. Thus the sampled sinusoidal signal frequency limit is

$$f = (1.63 \times 10^3)/2\pi A = 259/A(Hz)$$

where A is the amplitude of the sine wave. For a ±10V sine wave this corresponds to a frequency of 26Hz.

A sample/hold in front of the A/D converter "freezes" the converter's input signal whenever it is necessary to make a conversion. The rate-of-change limitation calculated above no longer exists. If a sample/hold has acquired an input signal and is tracking it, the sample/hold can be commanded to hold at any instant. There is

a short delay between the time the hold command is asserted and the time the circuit actually holds. This delay is called aperture delay. The hold command signal can usually be advanced in time to cause the amplifier to hold when one wants it to hold.

The uncertainty in aperture delay, called aperture jitter, is a key consideration. For the SHC803/804 there is a 25psec maximum period during which the input signal should not change, for example, more than 1/2LSB for 12-bit systems. For a ±10V input range (1/2LSB = 2.44mV), the input signal rate of change limitation is 2.44mV/25psec = 97.6V/μsec. The equivalent input sine wave frequency is

$$f = 97.6 \times 10^6 / 2\pi A = 15.5/A(MHz),$$

60,000 times higher than using the A/D alone.

However, there are other considerations. The resampling rate of an ADC803 is 1.5μsec (A/D conversion time) + 0.3μsec (sample/hold acquisition time) = 1.8μsec. If one samples a sine wave at the Nyquist rate this permits sampling a frequency of 278kHz. The above analysis assumed that the droop rate of the sample/hold is negligible—less than 1/2LSB during the conversion time—and that the large signal bandwidth response of the sample/hold causes negligible waveform distortion.

USING THE SHC804 WITH THE ADC803

ADC803 is a 1.5μsec, 12-bit successive approximation A/D converter. Its input circuitry has been designed to minimize high frequency current transients that appear at the input of successive approximation A/D converters. The SHC803 and SHC804 have been designed with a fast-settling, low output-impedance amplifier to further minimize the effects of high frequency transient currents present in an output load.

A typical SHC804/ADC803 connection for high-speed digitization is illustrated in Figure 3. A short delay must occur before the A/D start command is asserted since the ADC803 makes its first conversion decision 100nsec after the start command is asserted. Because the SHC804 sample-to-hold settling time is 150nsec (maximum) the additional delay required is about 50nsec. This can be achieved using a one-shot or by using the delay provided by the six inverters of a hex inverter integrated circuit. This combination can be triggered at rates of over 500k samples per second.

Using the input buffer of the SHC803 provides a high input impedance sample/hold for CMOS analog multiplexers such as the high speed Burr-Brown MPC800. The high input impedance of the SHC803 buffer minimizes DC errors caused by the ON resistance of the multiplexer switches and/or relatively high impedance signal sources (Figure 4). The multiplexer can be switched to a new channel as soon as the SHC803 is switched to the Hold mode. The multiplexer/buffer combination settles to the new input value during the sample/hold acquisition time and A/D conversion time. This "overlap" technique results in little or no loss in throughput rate.

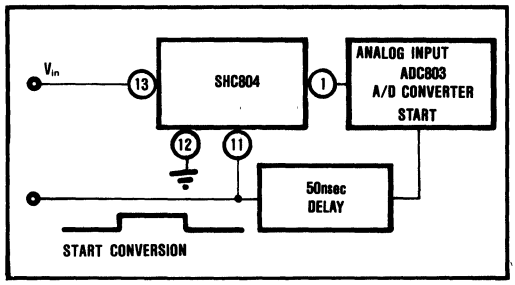


FIGURE 3. SHC804 and ADC803 Provide Sampling Rates Over 500k Samples Per Second.

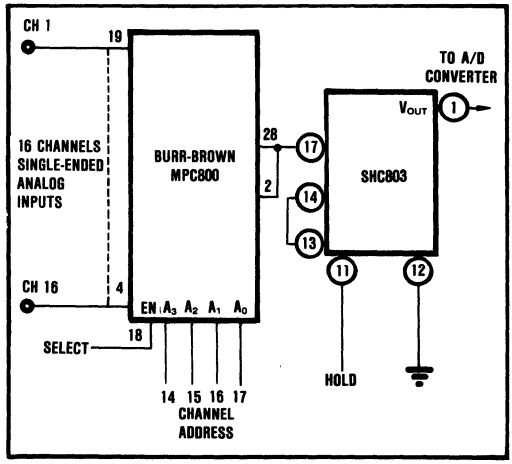
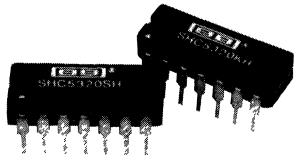


FIGURE 4. Using SHC803 With The MPC800 Analog Multiplexer.

BURR-BROWN®



SHC5320

High Speed Bipolar Monolithic SAMPLE/HOLD AMPLIFIER

FEATURES

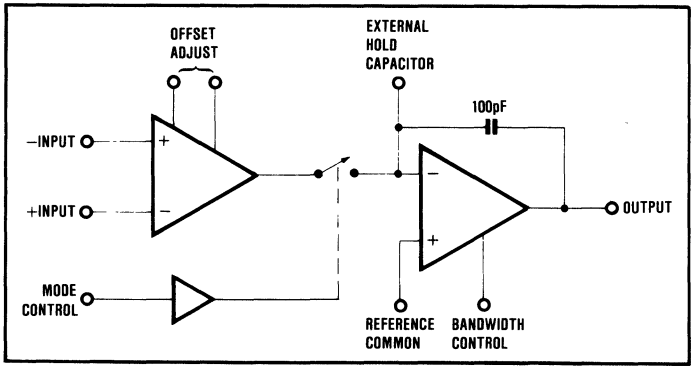
- 1.5μsec max ACQUISITION TIME TO 0.01%
- 250nsec max HOLD MODE SETTLING TIME
- 0.5μV/μsec max DROOP RATE AT +25°C
- TWO TEMPERATURE RANGES:
  0°C to +75°C (KH)
  −55°C to +125°C (SH)
- FULL DIFFERENTIAL INPUTS
- INTERNAL HOLDING CAPACITOR
- 14-PIN CERAMIC DIP PACKAGE

DESCRIPTION

The SHC5320 is a bipolar monolithic sample/hold circuit designed for use in precision high-speed data acquisition applications.

The circuit employs an input tranconductance amplifier capable of providing large amounts of charging current to the holding capacitor, thus enabling fast acquisition times. It also incorporates a low leakage analog switch and an output integrating amplifier with input bias current optimized to assure low droop rates. Since the analog switch always drives into a load at virtual ground, charge injection into the holding capacitor is constant over the entire input voltage range. As a result, the charge offset (pedestal voltage) resulting from this charge injection can be adjusted to zero by use of the offset adjustment capability. The device includes an internal holding capacitor to simplify ease of application; however, provision is also made to add additional external capacitance to improve the output voltage droop rate.

The SHC5320 is manufactured using a dielectric isolation process which minimizes stray capacitance (enabling higher-speed operation), and eliminates latch-up associated with substrate SCRs. The SHC5320KH features fully specified operation over the temperature range of 0°C to +75°C, while the SHC5320SH operates over the temperature range of −55°C to +125°C. The device requires ±15V supplies for operation, and is packaged in a reliable 14-pin ceramic dual-in-line package.



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PDS-585B

SPECIFICATIONS

ELECTRICAL

At +25°C, rated power supplies, gain = +1, and with internal holding capacitor, unless otherwise noted

MODEL	SHC5320KH			SHC5320SH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS							
ANALOG							
Voltage Range	±10			*			V
Common-Mode Range	±10			*			V
Input Resistance	1	5		*	*		MΩ
Input Capacitance			3			*	pF
Bias Current		±100	±300		±70	±200	nA
Bias Current Over Temperature Range			±300			±200	nA
Offset Current		±30	±300		*	±100	nA
Offset Current Over Temperature Range			±300			±100	nA
DIGITAL (over temperature range)							
V_{IH} (Logic "1")	2 0			*			V
V_{IL} (Logic "0")			0 8			*	V
I_{IH} (V_I = +5V)			0 1			*	μA
I_{IL} (V_I = 0V)			4			10	μA
Logic "0" = SAMPLE							
Logic "1" = HOLD							
OUTPUT CHARACTERISTICS							
Voltage Range	±10			*			V
Current	±10			*			mA
Output Impedance (Hold Mode)		1			*		Ω
Capacitance Load for Stability		300			*		pF
Noise, DC to 10MHz Sample Mode		125	200		*	*	μV rms
Hold Mode		125	200		*	*	μV rms
DC ACCURACY/STABILITY							
Gain, Open Loop, DC	3×10^5	2×10^6		10^6	*		V/V
Input Offset Voltage		±0 5			±0 2		mV
Input Offset Voltage Over Temperature Range			±1 5			±2	mV
Input Offset Voltage Drift		±5	±20		*	±15	μV/°C
CMRR[1]	72	90		80	*		dB
Power Supply Rejection[2] $+V_{CC}$	80			*			dB
$-V_{CC}$	65			*			dB
HOLD-TO-SAMPLE MODE DYNAMIC CHARACTERISTICS							
Acquisition Time, A = −1, 10V Step[3]							
to ±0 01%		1	1 5		*	*	μsec
to ±0 1%		0 8	1 2		*	*	μsec
SAMPLE MODE							
Gain-bandwidth Product (Gain = +1)[4]							
C_H = 100pF		2			*		MHz
C_H = 1000pF		180			*		kHz
Full Power Bandwidth[5]		600			*		kHz
Slew Rate[6]		45			*		V/μsec
Rise Time[4]		100			*		nsec
Overshoot[4]		15			*		%
SAMPLE-TO-HOLD MODE DYNAMIC CHARACTERISTICS							
Aperture Time[7]		25			*		nsec
Effective Aperture Time	−50	−25	0	*	*	*	nsec
Aperture Uncertainty (Aperture Jitter)		0 3			*		nsec
Charge Offset (Pedestal)[8] (adjustable to zero)		1			*		mV
Charge Transfer[8]		0 1	0 5		*	*	pC
Sample-to-Hold Transient Settling Time							
to ±0 01% of FSR		165	250		*	*	nsec
HOLD MODE							
Droop[8]		0 08	0 5		*	*	μV/μsec
Droop at Maximum Temperature		1 2	100		17	*	μV/μsec
Drift Current[8]		8	50		*	*	pA
Drift Current at Maximum Temperature		0 12	10		1 7	*	nA
Feedthrough, 10V p-p, 100kHz sinewave		2			*		mV
POWER SUPPLIES							
$+V_{CC}$	+14 5	+15	+16	*	*	*	V
$-V_{CC}$	−14 5	−15	−16	*	*	*	V
$+I_{CC}$ ($+V_{CC}$ = 15V)[9]		11	13		*	*	mA
$-I_{CC}$ ($-V_{CC}$ = 15V)[9]		−11	−13		*	*	mA

ELECTRICAL (CONT)

MODEL	SHC5320KH			SHC5320SH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE							
Specification	0		+75	−55		+125	°C
Storage	−65		+150				°C

*Specification same as grade to the left

NOTES (1) V_{CM} = ±5VDC (2) Based on a ±0 5V swing for each supply with all other supplies held constant (3) V_O - 10V step, R_L 2kΩ, C_L 50pF (4) V_O = 200mV p-p, R_L = 2kΩ, C_L = 50pF (5) V_{IN} = 20V p-p, R_L = 2kΩ, C_L = 50pF, unattenuated output (6) V_O 20V step, R_L 2kΩ, C_L 50pF (7) Simulated only, not tested (8) V_{IN} - 0V, V_{IH} – +3 5V, t_R ≤ 20nsec (V_{IL} to V_{IH}) (9) Specified for zero differential input voltage between pins 1 and 2 Supply current will increase with differential input (as may occur in the Hold mode) to approximately +28mA average at 20V differential

ABSOLUTE MAXIMUM RATINGS[1]

Voltage Between $+V_{CC}$ and $-V_{CC}$ Terminals	40V
Input Voltage	Actual Supply Voltage
Differential Input Voltage	±24V
Digital Input Voltage	+8V, −15V
Output Current, continuous[2]	±20mA
Internal Power Dissipation	450mW
Storage Temperature Range	−65°C < T_A < +150°C
Output Short-circuit Duration[3]	None
Lead Temperature (soldering, 10 seconds)	300°C

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

NOTES (1) Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired Functional operation under any of these conditions is not necessarily implied (2) Internal power dissipation may limit output current to less than +20mA (3) **WARNING: This device cannot withstand even a momentary short circuit to either supply.**

PIN ASSIGNMENTS

Pin 1	−Input	14	Mode Control
2	+Input	13	Supply Common
3	Offset Adjust	12	NC
4	Offset Adjust	11	External Hold Capacitor
5	$-V_{CC}$	10	NC
6	Reference Common	9	$+V_{CC}$
7	Output	8	Bandwidth Control

BURN-IN SCREENING

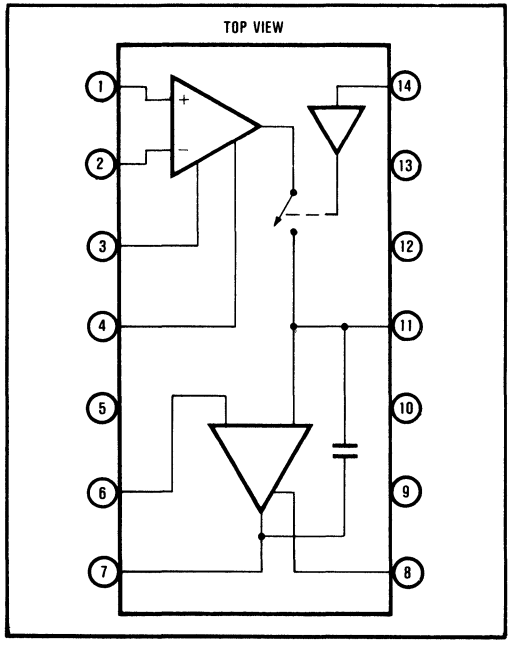
Burn-in screening is an option available for the models in the Ordering Information table. Burn-in duration is 160 hours at the indicated temperature (or equivalent combination of time and temperature).

ORDERING INFORMATION

Model	Temperature Range	Input Offset Over Temp. Range
SHC5320KH	0°C to +75°C	±1 5mW
SHC5320SH	0°C to +75°C	±2mW
BURN-IN SCREENING OPTION See text for details		
Model	**Temperature Range**	**Burn-In Temp (160 hours)[1]**
SHC5320KH-BI	0°C to +75°C	+125°C
SHC5320SH-BI	0°C to +75°C	+125°C

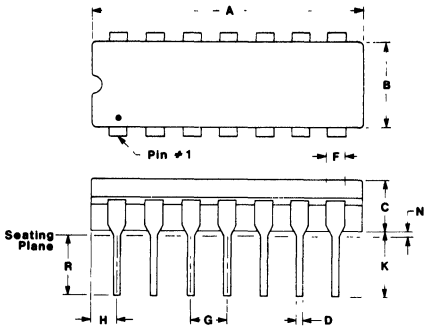
NOTE (1) Or equivalent combination of time and temperature

CONNECTION DIAGRAM



All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

MECHANICAL



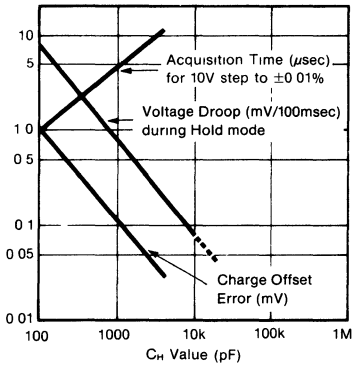
NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	.790	–	20.07
B	.220	.310	5.59	7.87
C	–	.185	–	4.70
D	.014	.023	0.36	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	–	.098	–	2.49
J	.008	.012	0.20	0.30
K	.140	.260	3.56	6.60
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.015	.060	0.38	1.52
R	.125	.200	3.18	5.08

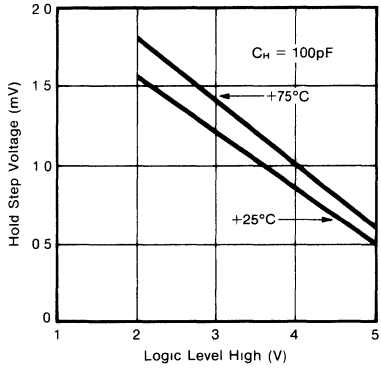
TYPICAL PERFORMANCE CURVES

$\pm V_{CC}$ = 15V

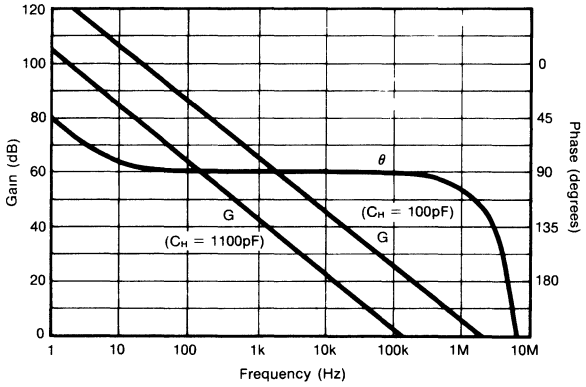
TYPICAL SAMPLE/HOLD PERFORMANCE AS FUNCTION OF HOLDING CAPACITOR



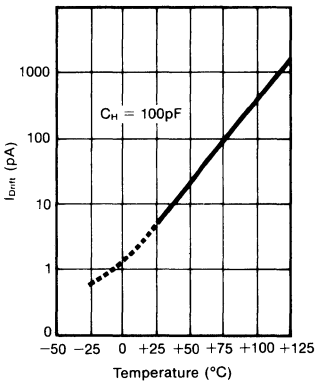
CHARGE OFFSET VS MODE CONTROL (V_{IH}) VOLTAGE



OPEN-LOOP GAIN AND PHASE RESPONSE



DRIFT CURRENT VS TEMPERATURE



DISCUSSION OF SPECIFICATIONS

WHAT IS A SAMPLE/HOLD AMPLIFIER?

A sample/hold amplifier (also sometimes called a track-and-hold amplifier) is a circuit that captures and holds an analog voltage at a specific point in time under control of an external circuit, such as a microprocessor. This type of circuit has many applications; however, its primary use is in data acquisition systems which require that the voltage be captured and held during the analog-to-digital conversion process. Use of a sample/hold effectively increases the bandwidth of a data acquisition system by a significant amount. For further discussion of this capability, refer to "Signal Digitization" in the

Applications section of this data sheet.

The ideal sample/hold amplifier in its simplest form contains four primary components as illustrated in Figure 1, although in actual practice they may not be internally connected exactly as shown. Amplifier A_1, the input buffer, provides a high impedance load to the source circuit and supplies charging current to the holding capacitor C_H. Switch S_1 opens and closes under external control to gate the buffered input signal to the holding circuit or to remove it so that the most recently sampled signal will be held. Amplifier A_2 serves to present a high impedance load to the holding capacitor and to provide a low impedance voltage source for external loads. A

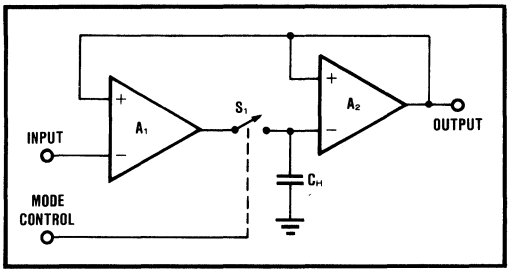


FIGURE 1. Ideal Sample/Hold Amplifier.

minimum of three terminals are provided for the user: input, output, and mode control (or sample/hold control). When S_1 is closed, the output signal follows the input signal, subject to errors imposed by amplifier bandwidth and other errors as discussed below. When S_1 is opened, the voltage stored on the holding capacitor will be held indefinitely (in the ideal case), and will appear at the output of the circuit until S_1 is again closed under command of the mode control signal.

The following discussion of specifications covers the critical types of errors which may be experienced in applications of a sample/hold amplifier. These errors are depicted graphically in Figure 2, and in the Typical Performance Curves.

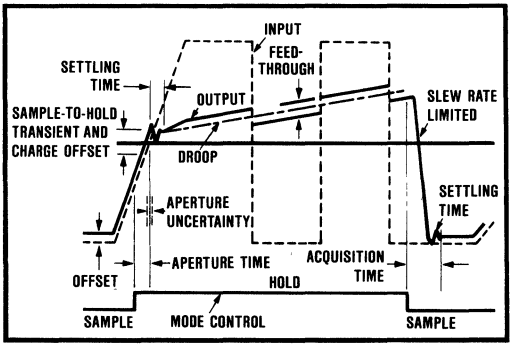


FIGURE 2. Illustration of Sample/Hold Specifications.

Acquisition Time is the time required for the sample/hold output to settle within a given error band of its final value after the sample mode is initiated. Included in this time are effects of switch delay time, slew rate of the buffer amplifier, and settling time for a specified change in held voltage value. Slew rate limitations of the buffer amplifier will cause actual acquisition time to be highly dependent on the amplitude of the voltage to be acquired, relative to the value already held by the capacitor. Therefore, proper specification of sample/hold amplifier performance includes definition of both output value step size and required error band accuracy.

Aperture Time (or aperture delay time) is the time required for switch S_1 to open and remove the charging signal from the capacitor after the mode control signal has changed from "sample" to "hold". This time is measured from the 50% point of the Hold mode transition to the time at which the output stops tracking the input. This parameter is very important in applications for which the input signal is changing very rapidly when the Hold mode is initiated.

Effective Aperture Time is the difference in propagation delay times of the analog signal and the mode control signal from their respective input pins to switch S_1. This time may be negative, zero, or positive. A negative value indicates that the mode control propagation delay is shorter than the analog propagation delay, with the result that the analog value present on the capacitor at the time the switch opens occurred earlier than the application of the mode control signal by the amount of the effective aperture delay time.

Aperture Uncertainty (or aperture jitter) is the variation observed in the aperture time over a large number of observations. This parameter is important when the analog input is a rapidly changing signal, as aperture uncertainty contributes to lack of knowledge (at the output) about the true value of the input at the precise time the Hold mode is initiated. The maximum input frequency for a given acceptable error contribution due to aperture uncertainty is

$$f_{max} = \text{Maximum Fractional Error} / 2\pi t_u$$

where Maximum Fractional Error (MFE) is the ratio of the maximum allowable error voltage to peak voltage, and t_u is the aperture uncertainty time. For a bipolar ±10V signal and a maximum uncertainty error of 1/2LSB in a 12-bit system, the MFE is equal to $1/2LSB \div V_{PEAK} = 2.44mV \div 10V = 0.000244V/V$, since 1/2LSB = 2.44mV for a 20V full-scale range.

For the same system operating with a unipolar 0V to 10V signal, MFE would be 0.000122V/V.

Charge Offset (pedestal) is the output voltage change that results from charge transfer into the hold capacitor through stray capacitance when the Hold mode command is given. This charge appears as an offset voltage at the output, and in some sample/hold amplifiers may be a function of the input voltage.

Charge offset is specified for the SHC5320 using only the internal holding capacitor. When an external capacitor is added, charge offset is calculated as Charge Transfer (pC) divided by total hold capacitance. Charge Transfer is also specified for the SHC5320, and total hold capaci-

tance is the sum of the internal hold capacitor value (100pF) and the external hold capacitor. Since charge transfer is not a function of analog input voltage for the SHC5320, this error may be removed by means of the offset adjustment capability of the amplifier.

Droop Rate is the change in output voltage over time during the Hold mode as a result of hold capacitor leakage, switch leakage, and bias current of the output amplifier. Droop rate varies with temperature and the quality of the external holding capacitor, if used. Careful circuit layout is also required to minimize droop.

Drift Current is the net leakage current affecting the hold capacitor during the Hold mode. With knowledge of the drift current, droop can be calculated as:

$$\text{Droop (V/sec)} = I_D(\text{pA}) / C_H(\text{pF})$$

Hold Mode Feedthrough is the fraction of the input signal which appears at the output while in the Hold mode. It is primarily a function of switch capacitance, but may also be increased by poor layout practices.

Hold Mode Settling Time is the time required for the sample-to-hold transient to settle within a specified error band.

OPERATING INSTRUCTIONS

OFFSET ADJUSTMENT

The offset should be adjusted with the input grounded. During the adjustment, the sample/hold should be switching continuously between the Sample and the Hold modes. The offset should then be adjusted to zero output for the periods when the amplifier is in the Hold mode. In this way, the effects of both amplifier offset and charge offset will be accounted for.

SAMPLE/HOLD CONTROL

A TTL logic "0" applied to pin 14 switches the SHC5320 into the Sample (track) mode. In this mode, the device acts as an amplifier which exhibits normal operational amplifier behavior, with the relationship of output to input signal depending upon the circuit configuration selected (see the Installation section below). Application of a logic "1" to pin 14 switches the SHC5320 into the Hold mode, with the output voltage held constant at the value present when the hold command is given. Pin 14 presents less than one LSTTL load to the driving circuit throughout the full operating temperature range.

ADDITION OF AN EXTERNAL CAPACITOR

The SHC5320 contains an internal 100pF MOS holding capacitor, sufficient for most high-speed applications. If improved droop performance is desired (with increased acquisition time), additional capacitance may be added between pins 7 and 11. If an external holding capacitor C_H is used, then a noise-bandwidth capacitor with a value of $0.1C_H$ should be connected from pin 8 to ground. The exact value and type of this bandwidth capacitor are not critical.

Teflon® DuPont Corporation

Capacitors with high insulation resistance and low dielectric absorption, such as Teflon® or polystyrene units, should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize leakage currents from the capacitor to minimize droop errors.

The value of the external capacitor determines the droop, charge offset, and acquisition time of the sample/hold. Both droop and charge offset will vary linearly with total hold capacitance from the values given in the specification table for the internal 100pF capacitor. The behavior of acquisition time versus total hold capacitance is shown in the Typical Performance Curves.

OUTPUT PROTECTION

In order to optimize high-frequency performance of this device, output protection is not included. This high-frequency performance is mandatory for a good sample/hold, which must absorb high-frequency changes in load current when driving a successive-approximation A/D converter. Due to the lack of output protection, the output circuit will not tolerate an indefinite short to common, but a momentary short is permissible. The output should never be shorted to supply.

INSTALLATION

LAYOUT PRECAUTIONS

Since the holding capacitor is connected to virtual ground at one end (pin 11) and to a low-impedance voltage source at the other (pin 7), the SHC5320 does not require the use of guard rings and other careful layout techniques which are required by many sample/hold circuits. However, normal good layout practice should be observed, minimizing the possibility of leakage paths across the holding capacitor. As in all digital-analog circuits, analog signal lines on the circuit board should cross digital signal paths at right angles whenever possible.

GROUNDING AND BYPASSING

Pin 6 (REFERENCE COMMON) should be connected to the system analog signal common as close to the unit as possible. Likewise, pin 13 (SUPPLY COMMON) should be connected to the system supply common. If the system design prevents running these two common lines separately, they should be connected together close to the unit, preferably to a large ground plane surrounding the sample/hold. Bypass capacitors (0.01μF to 0.1μF ceramic in parallel with 1μF to 10μF tantalum) should be connected from each power supply terminal of the device to pin 13 (SUPPLY COMMON).

OFFSET ADJUSTMENT

Offset adjustment capability may be achieved by connecting a 10kΩ, 10-turn potentiometer as illustrated in Figure 3.

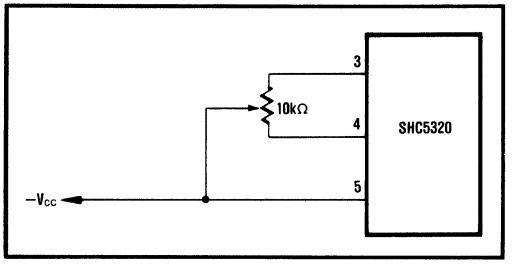


FIGURE 3. Connection of Offset Adjustment Potentiometer.

NONINVERTING MODE

The most common application of the SHC5320 will utilize the connection illustrated in Figure 4. In this mode of operation, the sample/hold will operate as a unity-gain noninverting amplifier when in the Sample mode, and the output signal will track the input. The high bandwidth of the SHC5320 and the large open-loop gain assure that gain error will be minimized.

When sampling lower-amplitude signals, the SHC5320 may also be connected as a noninverting amplifier with gain, as illustrated in Figure 5. In this circuit the gain of the amplifier is equal to $1 + R_2/R_1$ when sampling.

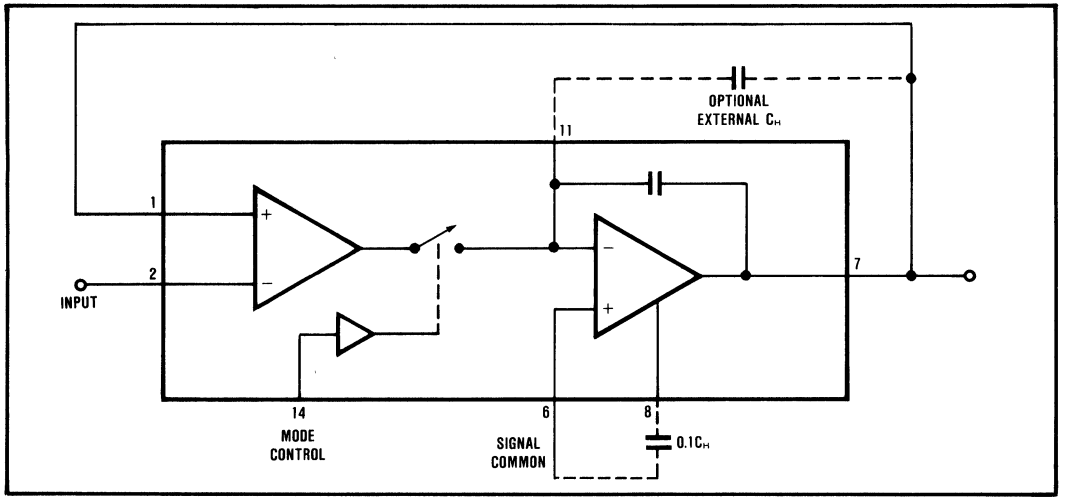


FIGURE 4. Noninverting Unity-Gain Connections.

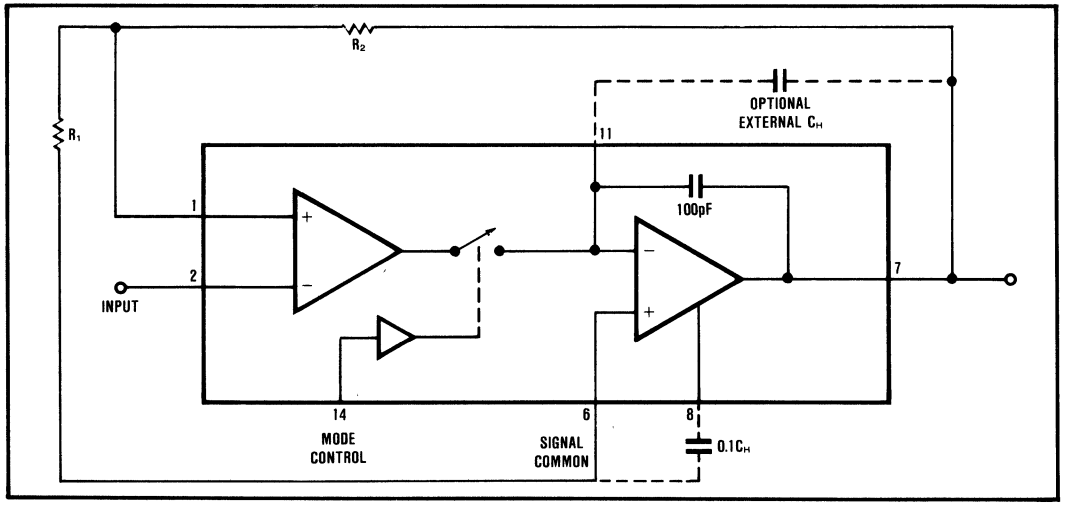


FIGURE 5. Noninverting Configuration with Gain = $1 + R_2/R_1$.

INVERTING MODE

Unlike most sample/holds, the SHC5320 may also be connected to act as an inverting amplifier, as shown in Figure 6. For this configuration, the gain is equal to $-R_2/R_1$.

For further discussions of operational amplifiers and how to use them, consult the Burr-Brown/McGraw-Hill Electronics Series of reference books, available through your local Burr-Brown sales office.

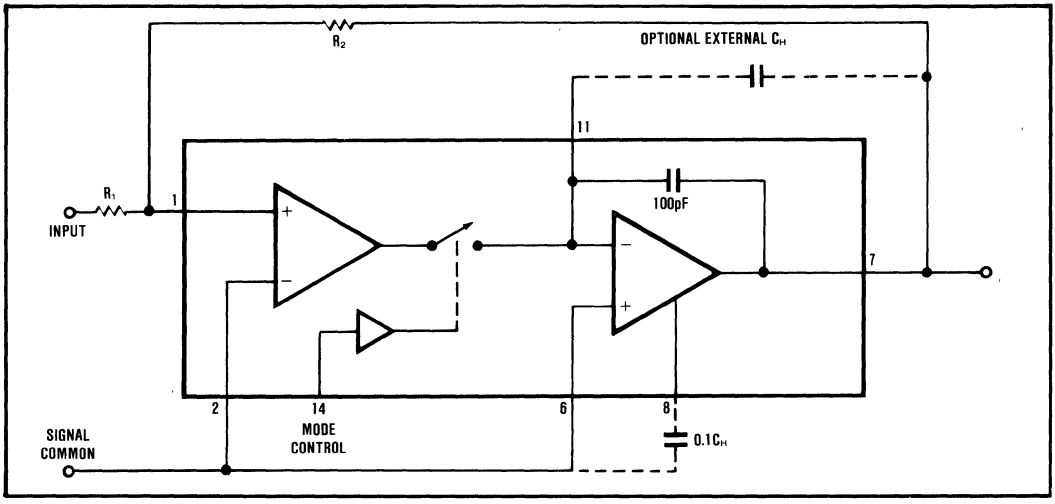


FIGURE 6. Inverting Configuration with Gain = $-(R_2/R_1)$.

INPUT OVERLOAD PROTECTION

It is possible that the input transconductance amplifier of the SHC5320 will saturate when the unit is in the Hold mode, due to a nonzero differential signal appearing between pins 1 and 2. This differential signal may be the result of a rapidly changing input signal or application of a new channel from an input multiplexer. When the input buffer is saturated in this fashion, acquisition time may be degraded because of the time required for the buffer to recover from saturation. In addition, the input buffer, which is designed to provide large amounts of charging current to the output integrator, may draw large amounts of supply current which may exceed 40mA peak in some applications. For these reasons, it is desirable to limit the differential voltage which may appear at the summing junction of the input buffer. Figures 7 and 8 illustrate possible methods of providing this voltage limitation for the inverting and noninverting configurations. The diodes may be Schottky diodes, which will provide the fastest clamping action and lowest clamping voltage, but fast signal diodes such as 1N914 will also work in most applications. In each configuration the value of R_1 should be large enough to avoid excessive loading of the input signal source. Similarly, R_2 should have a value of 2kΩ or greater to insure sufficient load current capability from the sample/hold. If the value of R_2 becomes too large, however, the added capacitance of the diodes may change the sample/hold phase response enough to cause oscillation.

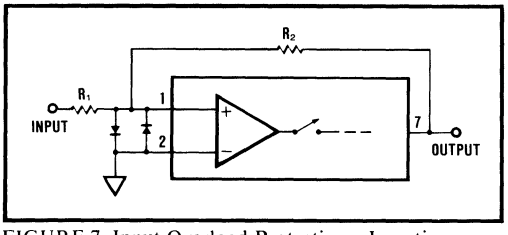


FIGURE 7. Input Overload Protection—Inverting Configuration.

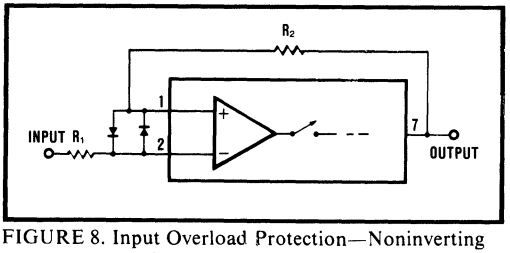


FIGURE 8. Input Overload Protection—Noninverting Configuration.

APPLICATIONS

SIGNAL DIGITIZATION

Sample/hold amplifiers are normally used to hold input voltages to an A/D converter constant during conversion. Digitizing errors result if the analog signal being digitized varies excessively during conversion.

For example, the Burr-Brown ADC80H-AH-12 is a 12-bit successive-approximation converter with a 25μsec conversion time. To insure the accuracy of the output data, the analog input signal to the A/D converter must not change more than 1/2LSB during conversion.

The maximum rate of change of a sine wave of frequency, f, is dv/dt (max) = $2\pi Af$(V/sec). If one allows a 1/2LSB change (2.44mV) for a ±10V input swing to the A/D converter, the allowable input rate-of-change limit would be 2.44mV/25μsec = 0.0976mV/μsec. Thus the sampled sinusoidal signal frequency limit is

$$f = (0.0976 \times 10^3)/2\pi A = 15.5/A \text{ (Hz)},$$

where A is the peak amplitude of the sine wave. For a ±10V sine wave, this corresponds to a frequency of 1.6Hz, hardly acceptable for the majority of sampled data systems.

However, a sample/hold in front of the A/D converter "freezes" the converter's input signal whenever it is necessary to make a conversion. The rate-of-change limitation calculated above no longer exists. If a sample/hold has acquired an input signal and is tracking it, the sample/hold can be commanded to hold it at any instant in time. There is a short delay (aperture delay) between the time the hold command is asserted and the time the circuit actually holds. The hold command signal can usually be advanced in time (or delayed, in the case of negative effective aperture delay) to cause the amplifier to hold the signal actually desired.

Aperture uncertainty (also called aperture jitter) is also a key consideration. For the SHC5320 there is a 300psec period during which the signal should not change more than the amount allowed for aperture uncertainty in the system error budget, perhaps 1/2LSB for a 12-bit system. For a ±10V input range (1/2LSB = 2.44mV), the input signal rate of change limitation is 2.44mV/0.3nsec = 8.13mV/nsec. The equivalent input sine wave frequency is

$$f = 8.13 \times 10^6 / 2\pi A = 1.29/A \text{ (MHz)},$$

a factor of almost 84,000 higher than using the A/D alone.

However, there are other considerations. The resampling rate of an ADC80H/SHC5320 combination is 26.5μsec (25μsec A/D conversion time plus 1.5μsec S/H acquisition time). Sampling a sine wave at the Nyquist rate, this permits a maximum input signal frequency of 37.7kHz. The above analysis assumes that the droop rate of the sample/hold is negligible—less than 1/2LSB during the conversion time—and that the large signal bandwidth response of the sample/hold causes negligible waveform distortion. Both of these assumptions are valid for the SHC5320 in this application.

DATA ACQUISITION

The SHC5320 may be used to hold data for analog-to-digital conversion or may be used to provide pulse-amplitude modulation (PAM) data output (see Figures 9 and 10).

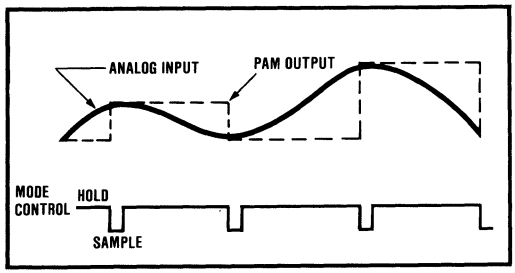


FIGURE 10. PAM Output.

DATA DISTRIBUTION

The SHC5320 may be used to hold the output of a digital-to-analog converter and distribute several different analog voltages to different loads (see Figure 11).

HIGH-SPEED DATA ACQUISITION

The minimum sample time for one channel in a data acquisition system is usually considered to be the acquisition time of the sample/hold plus the conversion time of the A/D converter. If two or more sample/holds are used with a multiplexer (such as the Burr-Brown MPC8S or MPC16S) as shown in Figure 12, the acquisition time of the sample/hold can be virtually eliminated. While the first channel is in hold and switched into the A/D converter, the multiplexer may be addressed to the next channel. The second sample/hold will have acquired this signal by the time the conversion is complete. Then, the sample/holds reverse roles and another channel is addressed. In low level systems an instrumentation amplifier (such as the Burr-Brown INA101) and a differential multiplexer (such as the Burr-Brown MPC4D or MPC8D) may be required in front of the sample/hold. The settling and acquisition times of the multiplexer, instrumentation amplifier, and sample/hold can be eliminated from the total conversion time as before by operating in this overlapped mode with the sample/holds.

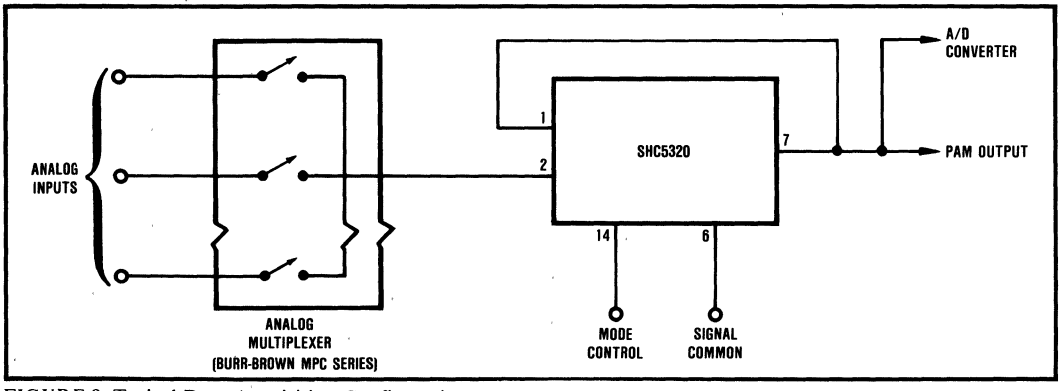


FIGURE 9. Typical Data Acquisition Configuration.

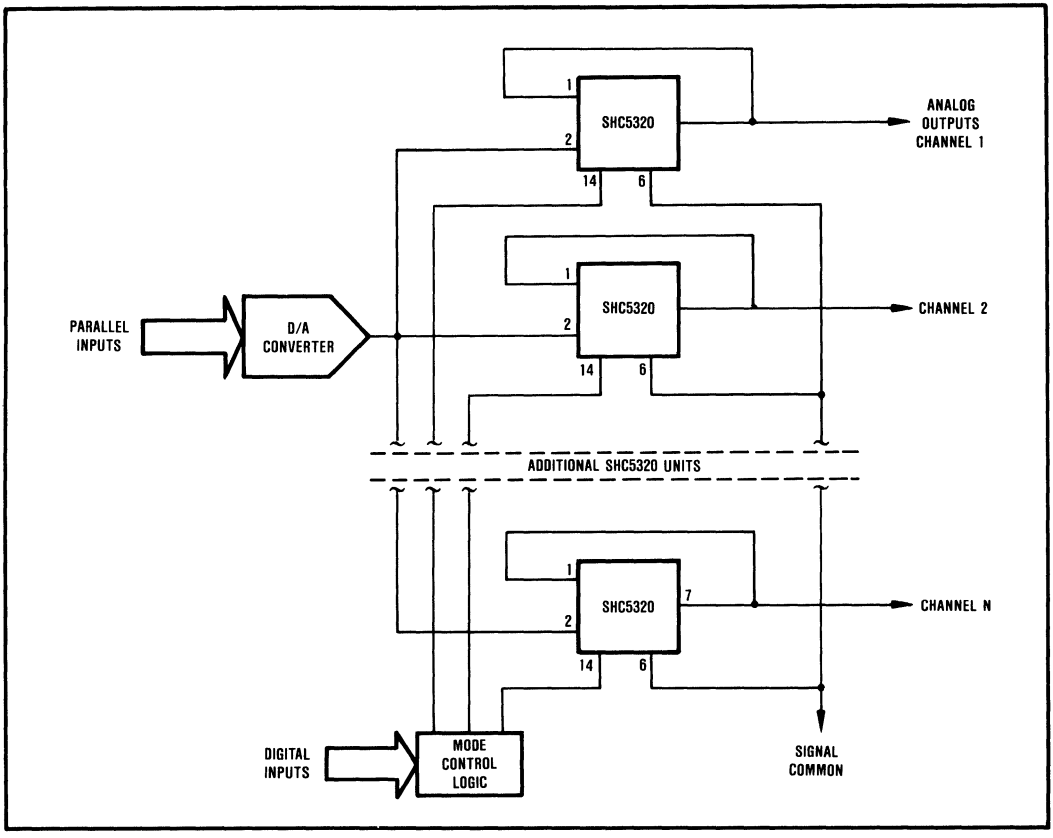


FIGURE 11. Typical Data Distribution Configuration.

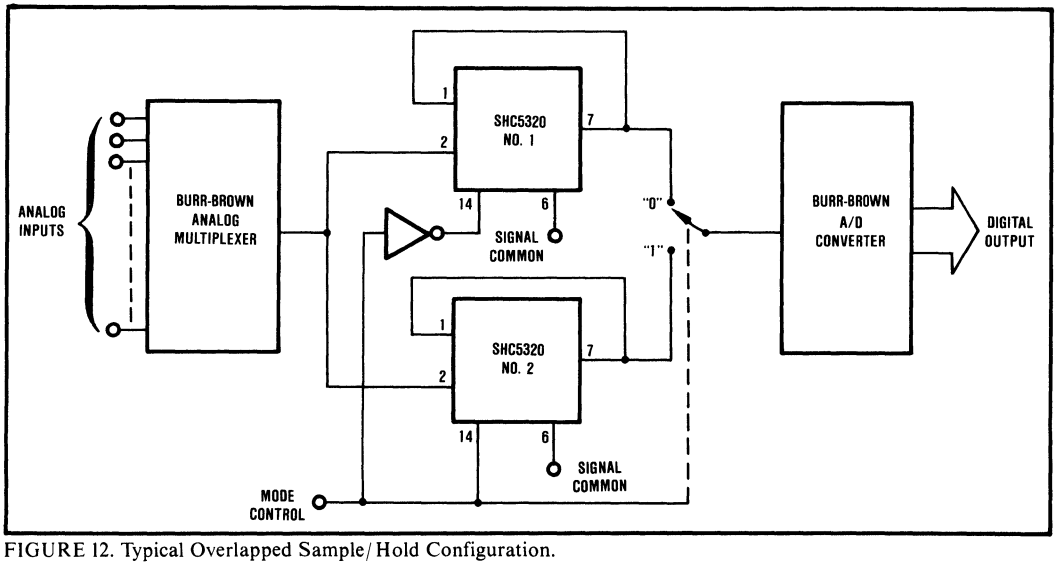
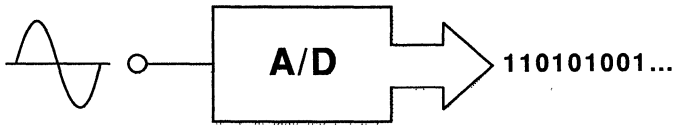


FIGURE 12. Typical Overlapped Sample/Hold Configuration.



ANALOG-TO-DIGITAL CONVERTERS

The Burr-Brown Analog-to-Digital (A/D) converter product line offers a broad selection of devices that enable you to choose the performance and price range ideally suited for your application. For example, the high-performance 12-bit ADC80, which converts to 12-bit accuracy in 25μs, was originated by Burr-Brown in 1975 and has become an industry standard. The recently introduced ADC603 is a 12-bit, 10MHz A/D converter that offers the industry's highest performance for RF signal processing applications. A high-resolution converter, the ADC76, converts 16 bits to ±0.003% absolute accuracy in only 15μs and is packaged in a 32-pin triple-wide dual-in-line package. Another performance category is total harmonic distortion for audio digital recording.

All devices are complete and fully specified, with a track record of high reliability proven both in the field as well as in internal qualification testing.

9

ANALOG-TO-DIGITAL CONVERTERS SELECTION GUIDES

The Selection Guide shows parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

INSTRUMENTATION ANALOG-TO-DIGITAL CONVERTERS — **Boldface = NEW**

Description	Model	Resolution (Bits)	Linearity Error (%FSR)	Input Range (V)	Conv Time (µs)	NMC Resolution	Temp Range[1]	Pkg[2]	Q, BI[3] Screen	Page
Serial Output	ADC804	12	±0.012	5,10,20 U/B[4]	17	12	Mil,Ind,Com	HCD	Q, BI	9.1-78
Low Cost	ADC574A	12	±0.012	10, 20 U/B	25	12	Mil,Ind,Com	HCD, PDIP	Q, BI	9.1-52
Data-Bus	ADC674	12	±0.012	10, 20 U/B	15	12	Mil,Ind,Com	HCD, PDIP	Q, BI	9.1-62
Interface	**ADC774**	**12**	**±0.012**	**10, 20 U/B**	**8**	**12**	**Mil,Ind,Com**	**HCD, PDIP**	**Q, BI**	**9.1-75**
Sampling	**ADS807**	**12**	**±0.012**	**10, 20 U/B**	**10**	**12**	**Mil,Ind,Com**	**HCD**	**Q, BI**	**9.1-86**
Data-Bus	**ADS808**	**12**	**±0.012**	**10, 20 U/B**	**10**	**12**	**Mil,Ind,Com**	**HCD**	**Q, BI**	**9.1-86**
Interface										
Low Cost	ADC80AG	12	±0.012	5, 10, 20 U/B	25	12	Ind	HCD	Q, BI	9.1-20
	ADC80MAH	**12**	**±0.012**	**5, 10, 20 U/B**	**25**	**12**	**Ind**	**HCD**	**Q, BI**	**9.1-36**
Medium Speed,	**ADC84KG**	**12**	**±0.012**	**5, 10, 20 U/B**	**10**	**12**	**Ind**	**HCD**	**Q, BI**	**9.1-44**
Low Cost	**ADC85H**	**12**	**±0.012**	**5, 10, 20 U/B**	**10**	**12**	**Com**	**HCD**	**Q, BI**	**9.1-44**
Medium Speed, Low Cost, Mil Temp	**ADC87H**	**12**	**±0.012**	**5, 10, 20 U/B**	**10**	**12**	**Mil**	**HCD**	**Q, BI**	**9.1-44**
High-Resolution Data-Bus Interface	**ADC700**	**16**	**±0.003**	**5, 10, 20 U/B**	**17**	**14**	**Mil, Ind, Com**	**HCD**	**BI**	**9.1-72**
High	ADC71	16	±0.003	5, 10, 20 U/B	50	14	Ind, Com	CD	Q, BI	9.1-4
Resolution	ADC72	16	±0.003	5, 10, 20 U/B	50	14	Ind, Com	MC	Q, BI	9.1-4
	ADC76	16	±0.003	5, 10, 20 U/B	17	14	Ind, Com	CD, MC	Q, BI	9.1-12

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) HCD = Hermetic Ceramic DIP, PDIP = Plastic DIP, CD = Ceramic DIP, MC = Metal Can. (3) Q indicates optional reliability screening is available for this model. BI indicates that an optional 160 hour burn-in is available for this model. (4) U/B indicates the input voltage range for the model: U = unipolar, B = bipolar.

Description	Model	Resolution (Bits)	Linearity Error (%FSR)	Input Range (V)	Conv Time (µs)	THD+N (Typ dB)	Temp Range[1]	Pkg[2]	Q[3] Screen	Page
Ultra-High Speed	**ADC600**	**12**	**±0.012**	**±1.25**	**0.1**	**68**	**Com, Ind**	**Module**		**9.2-89**
	ADC603	**12**	**±0.012**	**±1.25**	**0.1**	**68**	**Com, Mil**	**Special HDIP**		**9.2-110**
High Speed	ADC803	12	±0.012	10V/20V	1.5	NA	Ind, Mil	HMD	Q	9.2-124
	ADC601	**12**	**±0.012**	**10V/20V**	**1.0**	**70**	**Ind, Mil**	**HCD**		**9.2-107**
Very High Accuracy, High Speed	**ADC701**	**16**	**±0.0035**	**10V/20V**	**1.5**	**94**	**Com**	**40-p DIP**	—	**9.2-118**

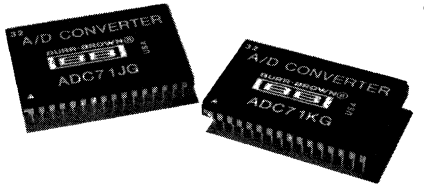
	Model	Resolution (Bits)	Typical Linearity	Input Range (V)	Conv Time (µs)	Max THD+N (V_{IN} = ±FS)	Output Format	Pkg	Page
High Performance	PCM75	16	15-Bit 14-Bit	±2.5, ±5 ±10V	17	–84dB (JG) –88dB (KG)	Parallel or Serial	32-p DIP	9.2-136
Low Cost	**PCM78**	**16**	**14-Bit**	**±1.25**	**4**	**68**	**Serial**	**28-p DIP**	**9.2-145**

NOTES: (1) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (2) HCD = Hermetic Ceramic DIP, HMD = Hermetic Metal DIP. (3) Q indicates optional reliability screening is available for this model.

MODELS STILL AVAILABLE BUT NOT FEATURED IN THIS BOOK

ADC10HT
ADC82AG
ADC82AM
ADC806

BURR-BROWN®



ADC71
ADC72

16-Bit
ANALOG-TO-DIGITAL CONVERTER

FEATURES

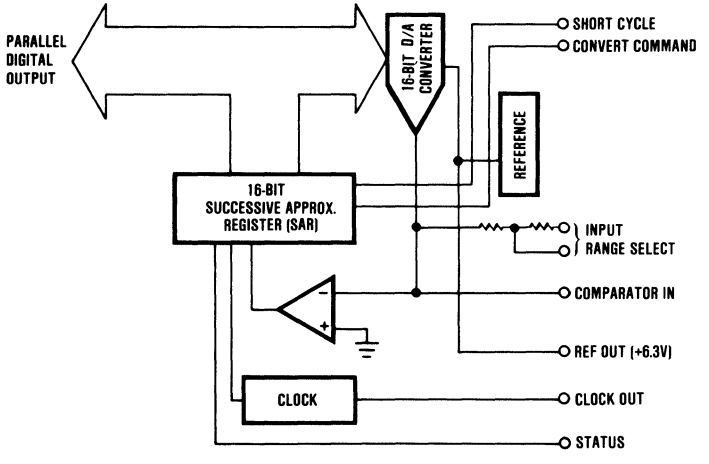
- 16-BIT RESOLUTION
- ±0.003% MAXIMUM NONLINEARITY
- COMPACT DESIGN
  32-pin Ceramic or Hermetic Metal Package
- FAST CONVERSION SPEED
  50μs Maximum
- LOW COST

DESCRIPTION

The ADC71 and ADC72 are low cost, high quality, 16-bit successive approximation analog-to-digital converters. They use state-of-the-art IC and laser-trimmed thin-film components and are packaged in either a convenient 32-pin ceramic or metal dual-in-line package. The converter is complete with internal reference, clock, comparator, and thin-film scaling resistors, which allow selection of analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

Data is available in parallel and serial form with corresponding clock and status output. All digital inputs and outputs are TTL-compatible.

Power supply voltages are ±15VDC and +5VDC.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At +25°C and rated power supplies unless otherwise noted.

MODEL	ADC71J, K/ADC72J, K			ADC72A, B			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			16			16	Bits
INPUTS							
ANALOG							
Voltage Ranges: Bipolar		±2.5, ±5, ±10			±2 5, ±5, ±10		V
Unipolar		0 to +5, 0 to +10, 0 to +20			0 to +5, 0 to +10, 0 to +20		V
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			2 5		kΩ
0 to +10V, ±5.0V		5			5		kΩ
0 to +20V, ±10V		10			10		kΩ
DIGITAL[1]							
Convert Command	Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion)						
Logic Loading	1						TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error[2]		±0 1	±0 2		±0 1	±0 2	%
Offset[2]							
Unipolar		±0 05	±0 1		±0 05	±0 1	% of FSR[3]
Bipolar		±0 1	±0.2		±0 1	±0 2	% of FSR
Linearity Error. K, B			±0 003			±0 003	% of FSR
J, A			±0 006			±0 006	% of FSR
Inherent Quantization Error		±1/2			±1/2		LSB
Differential Linearity Error		±0 003			±0 003		% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			0 003		% of FSR/%V_S
+5VDC		0 001			0.001		% of FSR/%V_S
CONVERSION TIME[4]							
14 Bits			50			50	μs
WARM-UP TIME	10			10			min
DRIFT							
Gain (ADC71)			±15				
Gain (ADC72)		±10	±20		±7	±15	ppm/°C
Offset							
Unipolar		±2	±4			±2	ppm of FSR/°C
Bipolar		±8	±10		±5	±10	ppm of FSR/°C
Linearity		±2	±3			±2	ppm of FSR/°C
No Missing Codes Temp Range							
JG, JM, AM (13 bits)	0		+50	0		+50	°C
KG, KM, BM (14 bits)	±10		+40	+10		+40	°C
OUTPUT							
DIGITAL DATA							
(All codes complementary)							
Parallel							
Output Codes[5]. Unipolar		CSB					
Bipolar		COB, CTC[6]					
Output Drive			2				TTL Loads
Serial Data Code (NRZ)		CSB, COB					
Output Drive			2				TTL Loads
Status	Logic "1" during conversion						
Status Output Drive			2			2	TTL Loads
Clock Output Drive			2			2	TTL Loads
Frequency[7]	350		350				kHz
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6 6	6.0	6 3	6 6	V
Max External Current							
with No Degradation of Specs			±200			±200	μA
Temp Coefficient (ADC72)			±10			±5	ppm/°C
Temp Coefficient (ADC71)			±10				ppm/°C

SPECIFICATIONS

ELECTRICAL (CONT)

At +25°C and rated power supplies unless otherwise noted.

MODEL	ADC71J, K/ADC72J, K			ADC72A, B			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Power Consumption		550			550		mW
Rated Voltage, Analog	±14.5	±15	±15.5	±14.5	±15	±15.5	VDC
Rated Voltage, Digital	+4.75	+5	+5.25	+4.75	+5	+5.25	VDC
Supply Drain +15VDC		+45			+45		mA
Supply Drain −15VDC		−35			−35		mA
Supply Drain +15VDC		+70			+70		mA
TEMPERATURE RANGE							
Specification	0		+70	−25		+85	°C
Operating (derated specs)	−25		+85	−55		+85	°C
Storage	−55		+125	−55		+125	°C

NOTES:

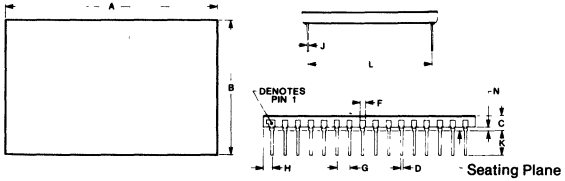
1 DTL/TTL compatible, i e , Logic "0" = 0 8V, max Logic "1" = 2 0V, min for inputs For digital outputs Logic "0" = +0 4V, max Logic "1" = 2 4V, min
2 Adjustable to zero
3. FSR means Full Scale Range For example, unit connected for ±10V range has 20V FSR
4 Conversion time may be shortened with "Short Cycle" set for lower resolution, see "Additional Connections Required" section
5 See Table I CSB - Complementary Straight Binary COB - Complementary Offset Binary CTC - Complementary Two's Complement
6. CTC coding obtained by inverting MSB (Pin 1)

MECHANICAL

G Package–32-Pin Ceramic

NOTE Leads in true position within 0 10" (0 25mm) R at MMC at seating plane

Pin numbers shown for reference only
Numbers may not be marked on package



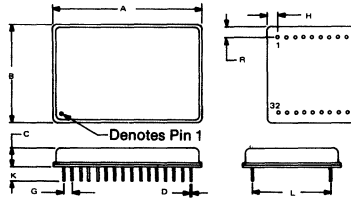
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 678	1.712	42 62	43.48
B	1.079	1 101	27 41	27.97
C	180	210	4 57	5 33
D	016	.020	41	51
F	045	055	1 14	1.40
G	100 BASIC		2 54 BASIC	
H	089	106	2 26	2 69
J	009	.012	23	30
K	200	210	5 08	5 33
L	900 BASIC		22 86 BASIC	
N	015	035	38	89

CASE. Ceramic
MATING CONNECTOR: 2302MC
WEIGHT: 13 grams (0 46 oz)

HERMETICITY Conforms to Method 1014, Condition C, Step 1 (fluorocarbon) of MIL-STD-883 (gross leak)

M Package– 32-Pin Hermetic Metal DIP

NOTE Leads in true position within .010" (25mm) R at MMC at seating plane



Pin numbers shown for reference only. Numbers may not be marked on package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.720	1 760	43 69	44.70
B	1 120	1 160	28.45	29.46
C	0 170	0.250	4.32	6.35
D	0.16	0.021	0.41	0 53
G	100 BASIC		2.54 BASIC	
H	0 100	0.140	2 54	3.56
K	0.150	0.300	3 81	7.62
L	900 BASIC		22 86 BASIC	
R	0 100	0.140	2 54	3.56

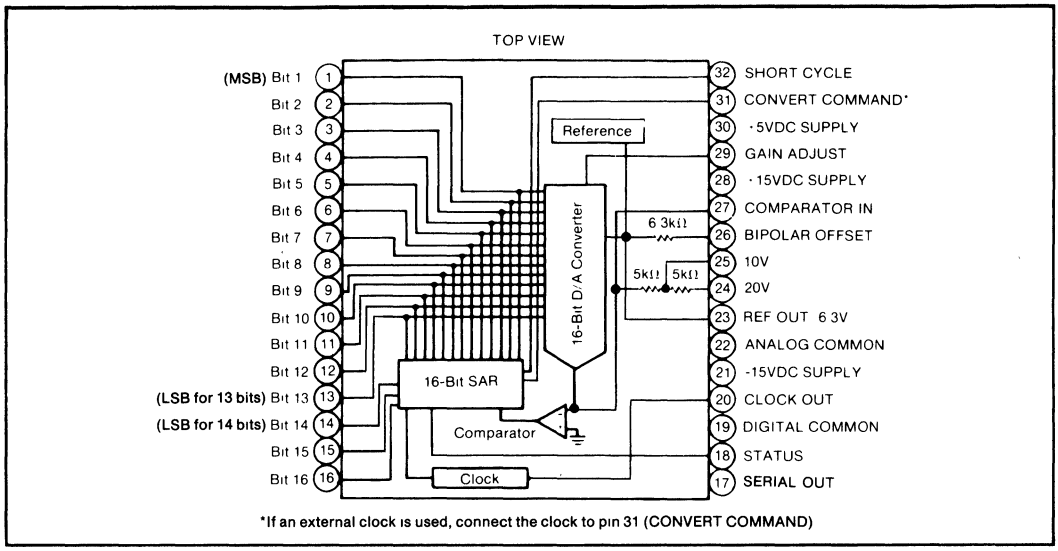
CASE Nickel-plated kovar
MATING CONNECTOR 2302MC
WEIGHT: 13 grams (0.46 oz.)

Contrasting glass seal or square corner denotes pin 1

ABSOLUTE MAXIMUM SPECIFICATIONS

$+V_{CC}$ to Common	0V to +16.5V
$-V_{CC}$ to Common	0V to −16.5V
$+V_{DD}$ to Common	0V to +7V
Analog Common to Digital Common	±0.5V
Logic Inputs to Common	0V to V_{DD}
Maximum Power Dissipation	1000mW
Lead Temperature (10s)	300°C

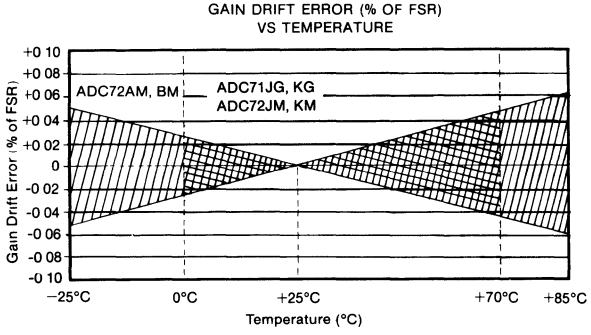
CONNECTION DIAGRAM

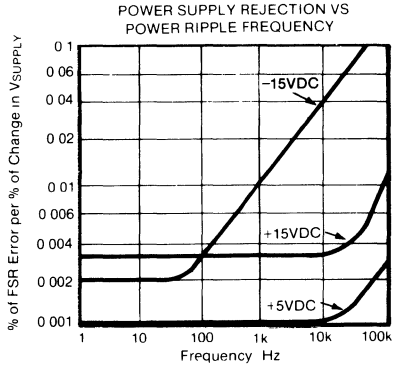


ORDERING INFORMATION

Model	Temperature Range	Nonlinearity
ADC71JG	0°C to +70°C	±0 006% FSR
ADC71KG	0°C to +70°C	±0 003% FSR
ADC72JM	0°C to +70°C	±0 006% FSR
ADC72KM	0°C to +70°C	±0 003% FSR
ADC72AM	-25°C to +85°C	±0 006% FSR
ADC72BM	-25°C to +85°C	±0 003% FSR

TYPICAL PERFORMANCE CURVES





DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2 LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A

Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB.

The ADC71/72 is also monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that these converters will have no missing codes over a specified temperature range when short-cycled for 14-bit operation.

TIMING CONSIDERATIONS

The timing diagram (Figure 2) assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output). Figures 2a and 2b are timing diagrams showing the relationship of serial data to clock and valid data to status.

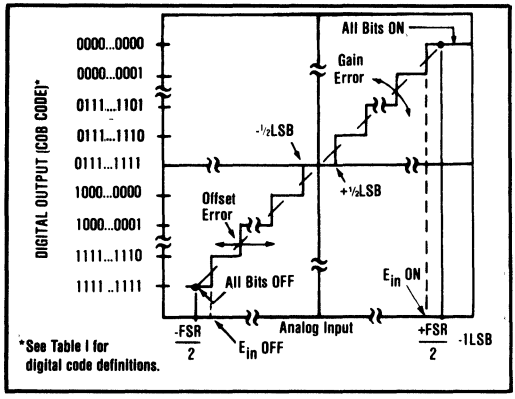


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter

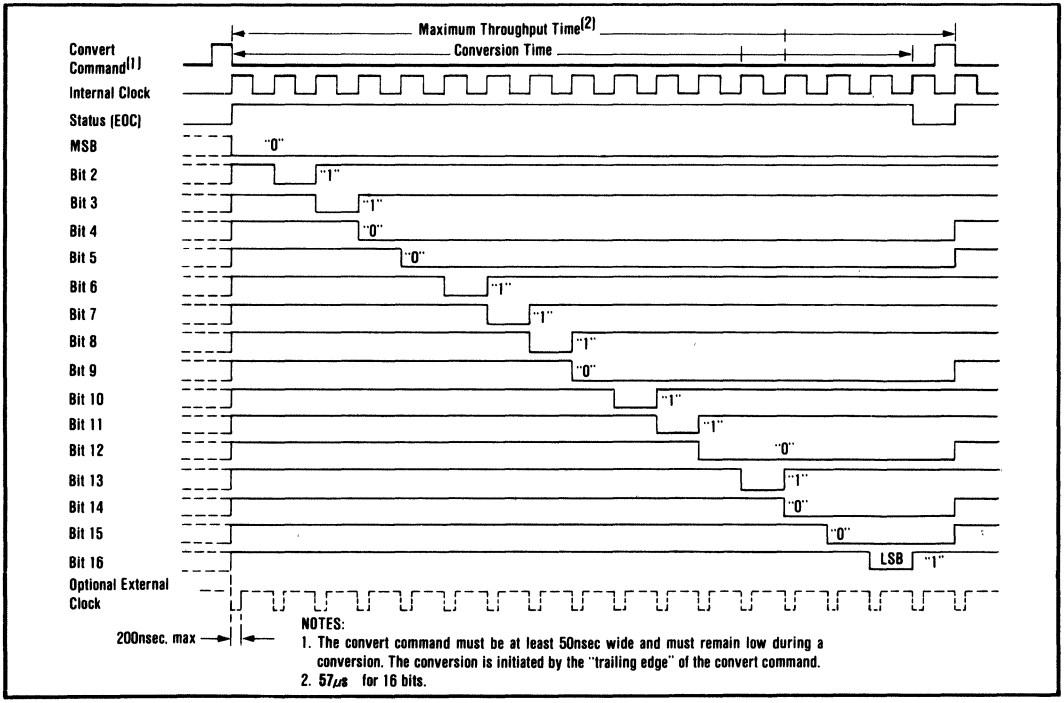


FIGURE 2. ADC71/72 Timing Diagram.

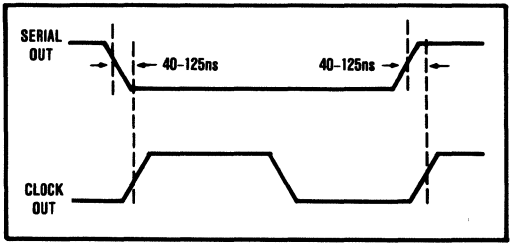


FIGURE 2a. Timing Relationship of Serial Data to Clock.

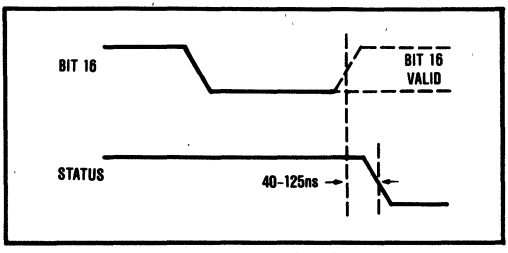


FIGURE 2b. Timing Relationship of Valid Data to Status.

DEFINITION OF DIGITAL CODES

PARALLEL DATA

Two binary codes are available on the ADC71/72 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (Pin 1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 12-, 13- and 14-bit resolutions. Figure 3 shows the connections for 14-bit resolution, parallel data output, with ±10V input.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line: CSB and COB. The serial data is available only during conversion and appears with MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagrams of Figures 2 and 2a. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary BIN Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As	±10V	±5V	±2 5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB(1) or CTC(2)	COB(1) or CTC(2)	COB(1) or CTC(2)	CSB(3)	CSB(3)	CSB(3)
One Least Significant Bit LSB	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 12	4 88mV	2 44mV	1 22mV	2 44mV	1 22mV	4 88mV
	n = 13	2 44mV	1 22mV	610µV	1 22mV	610µV	2 44mV
	n = 14	1 22mV	610µV	305µV	610µV	305µV	1 22mV
Transition Values							
MSB LSB							
000 000(4)	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2 5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011 111	Mid Scale	0	0	0	+5V	+2 5V	+10V
111 110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2 5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

(1) COB = Complementary Offset Binary
(2) CTC = Complementary Two's Complement - obtained by inverting the most significant bit MSB (Pin 1)
(3) CSB = Complementary Straight Binary
(4) Voltages given are the nominal value for transition to the code specified

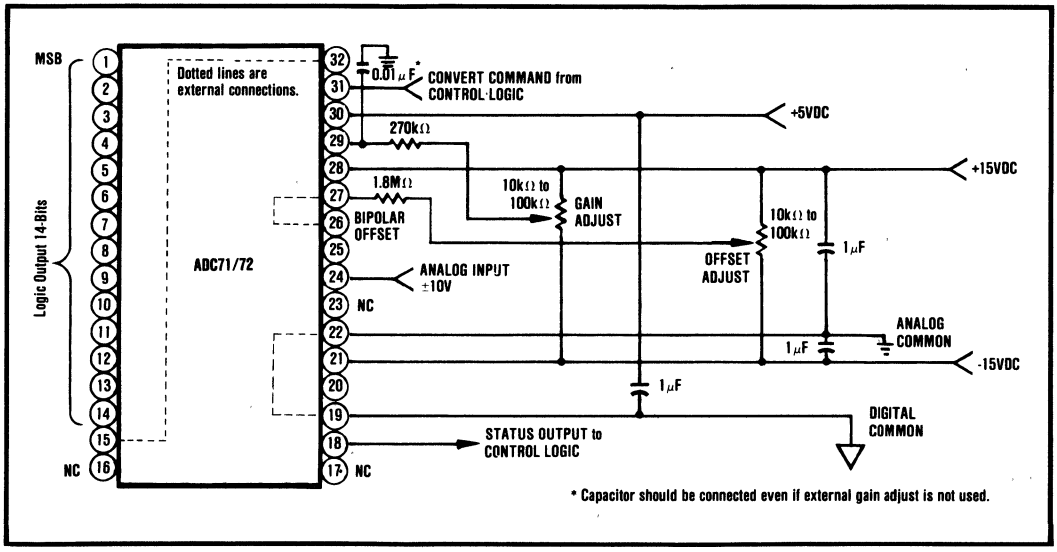


FIGURE 3. ADC71/72 Connections For: ±10V Analog Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

DISCUSSION OF SPECIFICATIONS

The ADC71/72 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. This ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.1% of FSR (typically ±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 6 and 7.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The power supply sensitivity is specified for ±0.003% of FSR/%ΔV_S for ±15V supplies and ±0.001% of FSR/%ΔV_S for +5V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling and Figure 4.

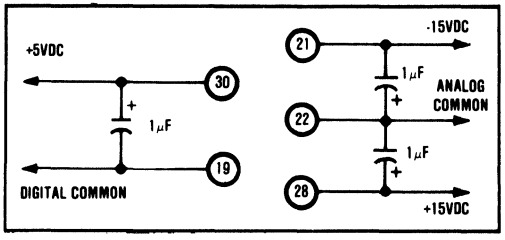


FIGURE 4. Recommended Power Supply Decoupling.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC71/72 but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor patterns and a 0.01µF to 0.1µF non-polarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital commons returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (Pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum capacitors as shown in Figure 4 to obtain noise free operation. These capacitors should be located close to the ADC.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 5 for circuit details.

TABLE II. ADC72 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Sig	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Sig	24

*Obtained by inverting MSB Pin 1

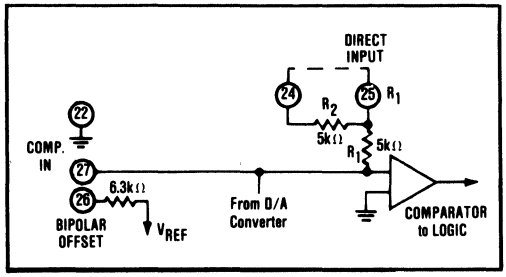


FIGURE 5. ADC71/72 Input Scaling Circuit.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 6 and 7. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and Pin 27 (Offset Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

OFFSET - Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 6. **Sweep the input through the end point transition voltage that should cause an output transition to all bits Off (E_{IN}^{OFF}).**

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

GAIN - Connect the Gain adjust potentiometer as shown in Figure 7. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}

Table I details the transition voltage levels required.

CONVERT COMMAND CONSIDERATIONS

Convert command resets the converter whenever taken high. This insures a valid conversion on the first conversion after power-up.

Convert command must stay low during a conversion unless it is desired to reset the converter during a conversion.

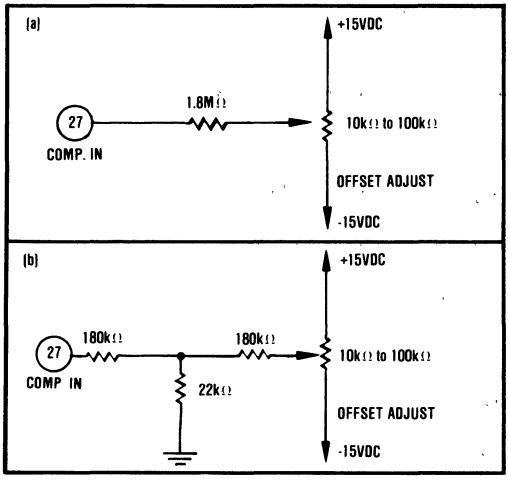


FIGURE 6. Two Methods of Connecting Optional Offset Adjust with a 0.4% of FSR Range of Adjustment.

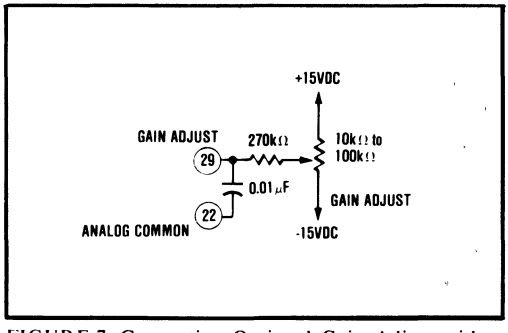


FIGURE 7. Connecting Optional Gain Adjust with a 0.2% Range of Adjustment.

ADDITIONAL CONNECTIONS REQUIRED

The ADC71/72 may be operated at faster speeds for resolutions less than 14 or 13 bits, depending on the model selected, by connecting the Short-Cycle Input, pin 32, as shown in Table III. Conversion speeds, linearity, and resolutions are show for reference.

TABLE III Short-Cycle Connections and Specifications for 12- to 14-Bit Resolutions

Resolution (Bits)	16	14	13	12
Connect Pin 32 to	Open	Pin 15	Pin 14	Pin 13
Maximum Conversion Speed (μsec)(1)	57	50	46.5	43
Maximum Nonlinearity at 25°C (% of FSR)	0.003(2)	0.003(2)	0.006	0.006

NOTES
1. Max conversion time to maintain specified nonlinearity error
2. BM and KM models only

OUTPUT DRIVE

Normally all ADC71/72 logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

HEAT DISSIPATION

The ADC71/72 dissipates approximately 1.3 watts (typical) and the packages have a case-to-ambient thermal resistance (θ_{CA}) of 25°C/W. For operation above 70°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. See Figure 8 for θ_{CA} requirement above 70°C. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the case can be achieved using a silicone heat sink compound. On a 0.062" thick PC card with a 16 square inch (min.) area, this technique will allow operation to 85°C.

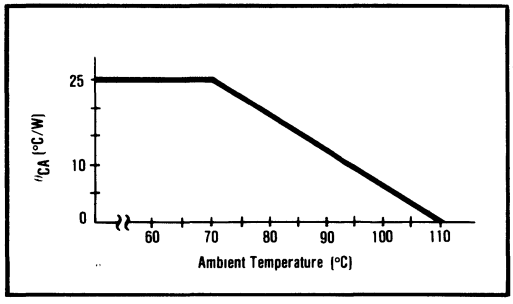


FIGURE 8. θ_{CA} Requirement Above 70°C

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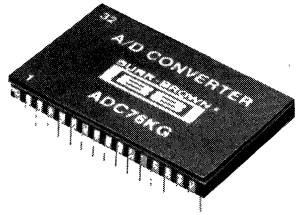


ADC76

16-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 16-BIT RESOLUTION
- LINEARITY ERROR ±0.003% MAX (KM, BM)
- NO MISSING CODES GUARANTEED FROM 0°C TO +70°C
- 15μs CONVERSION TIME (15-BIT)
- SERIAL AND PARALLEL OUTPUTS
- COMPACT DESIGN
  32-pin Ceramic or Hermetic Metal Package
- LOW COST

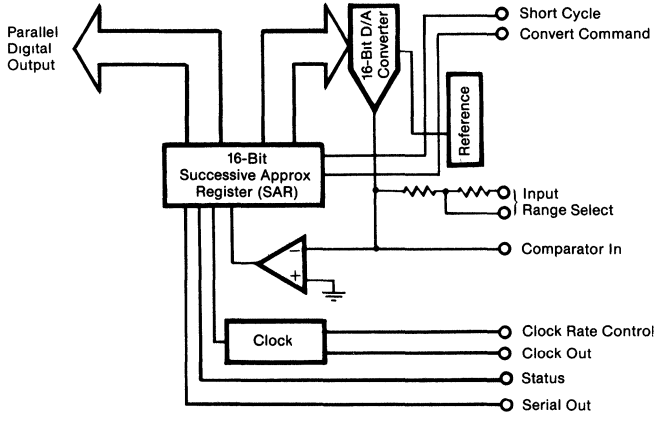
DESCRIPTION

The ADC76 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. The ADC76 uses state-of-the-art IC and laser-trimmed thin-film components and is packaged in a convenient 32-pin dual-in-line package. The converter is complete with internal reference, short cycling capabilities, serial output, and thin-film scaling resistors, which allow selection of analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

It is specified for operation over two temperature ranges: 0°C to +70°C (J, K) and −25°C to +85°C (A, B).

Data is available in parallel and serial form with corresponding clock and status output. All digital inputs and outputs are TTL-compatible.

Power supply voltages are ±15VDC and +5VDC.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-843

SPECIFICATIONS

ELECTRICAL

At +25°C and rated power supplies unless otherwise noted.

MODEL	ADC76J, K			ADC76A, B			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			*	Bits
ANALOG INPUTS							
Voltage Ranges Bipolar		±2 5, ±5, ±10			*		V
Unipolar		0 to +5, 0 to +10, 0 to +20			*		V
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			*		kΩ
0 to +10V, ±5.0V		5			*		kΩ
0 to +20V, ±10V		10			*		kΩ
DIGITAL INPUTS[1]							
Convert Command	Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion)						
Logic Loading		1				*	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error[2]		±0 1	±0 2		*	*	%
Offset Error. Unipolar[2]		±0.05	±0.1		*	*	% of FSR[3]
Bipolar[2]		±0.1	±0.2		*	*	% of FSR
Linearity Error: K, B			±0 003			*	% of FSR
J, A			±0.006			*	% of FSR
Inherent Quantization Error		±1/2			*		LSB
Differential Linearity Error		±0 003			*		% of FSR
Noise (3σ, p-p)		±0 003			*		% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			*		% of FSR/%V_S
+5VDC		0 001			*		% of FSR/%V_S
CONVERSION TIME[4]							
14 Bits			15			*	μs
15 Bits			16			*	μs
16 Bits			17			*	μs
WARM-UP TIME	5			*			min
DRIFT							
Gain			±15			*	ppm/°C
Offset: Unipolar		±2	±4		*	*	ppm of FSR/°C
Bipolar			±10			*	ppm of FSR/°C
Linearity		±2	±3		*	*	ppm of FSR/°C
No Missing Codes Temp Range							
J, A (14-bit)	0		+70	0		+70	°C
K, B (13-bit)	0		+70	−25		+85	°C
OUTPUT							
DIGITAL DATA							
(All codes complementary)							
Parallel							
Output Codes[5]: Unipolar		CSB			*		
Bipolar		COB, CTC[6]			*		
Output Drive			2			*	TTL Loads
Serial Data Code (NRZ)		CSB, COB			*		
Output Drive			2			*	TTL Loads
Status	Logic "1" during conversion				*		
Status Output Drive			2			*	TTL Loads
Internal Clock: Clock Output Drive			2			*	TTL Loads
Frequency[7]	933		1400	*		*	kHz
POWER SUPPLY REQUIREMENTS							
Power Consumption		0.525			*		W
Rated Voltage: Analog	±14.5	±15	±15 5	*	*	*	VDC
Digital	+4.75	+5	+5.25	*	*	*	VDC
Supply Drain: +15VDC		+14			*		mA
−15VDC		−17			*		mA
+5VDC		+10			*		mA
TEMPERATURE RANGE							
Specification	0		+70	−25		+85	°C
Storage	−55		+125	*		*	°C

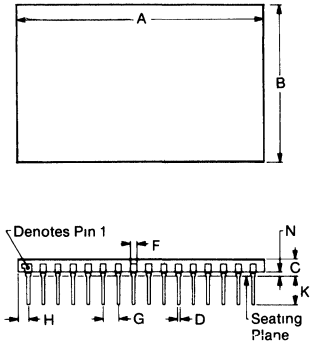
*Specification same as ADC76J, K.

NOTES. (1) DTL/TTL compatible, i.e , Logic "0" = 0.8V, max, Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = 0 4V, max, Logic "1" = 2.4V, min. (2) Adjustment to zero See "Optional External Gain and Offset Adjustment" section. (3) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR (4) Conversion time may be shortened with "Short Cycle" set for lower resolution and with use of Clock Rate

Control. See "Optional Conversion Time Adjustment" section. The Clock Rate Control (pin 23) should be connected to Digital Common for specified conversion time. Short Cycle (pin 32) should be left open for 16-bit resolution or connected to the n + 1 digital output for n-bit resolution. For example, connect Short Cycle to Bit 15 (pin 15) for 14-bit resolution. For resolutions less than 16 bits, pin 32 should also be tied to +5V through a 2kΩ resistor. (5) See Table I. CSB—Complementary Straight Binary, COB—Complementary Offset Binary, CTC—Complementary Two's Complement. (6) CTC coding obtained by inverting MSB (pin 1). (7) Adjustable with Clock Rate Control from approximately 933kHz to 1.4MHz. See Figures 12 and 13 and Table III.

MECHANICAL

G Package-32-Pin Ceramic



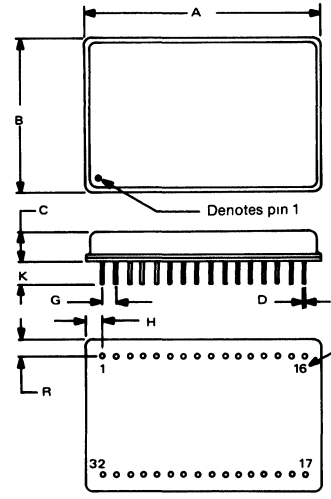
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.678	1 712	42.62	43 48
B	1 079	1 101	27 41	27 97
C	180	210	4 57	5 33
D	016	020	41	51
F	045	055	1.14	1 40
G	100 BASIC		2 54 BASIC	
H	089	106	2 26	2 69
J	009	012	23	30
K	200	210	5 08	5 33
L	900 BASIC		22 86 BASIC	
N	015	035	38	.89

NOTE Leads in true position within 0 010" (0 25mm) R at MMC at seating plane

Pin numbers shown for reference only
Numbers may not be marked on package

CASE Ceramic
MATING CONNECTOR 2302MC
WEIGHT 13 grams (0 46 oz)
HERMETICITY Conforms to Method 1014, Condition C, Step 1 (fluorocarbon) of MIL-STD-883 (gross leak)

M Package-32-Pin Hermetic Metal DIP



NOTE
Leads in true position within 010"
(25mm) R at MMC at seating plane

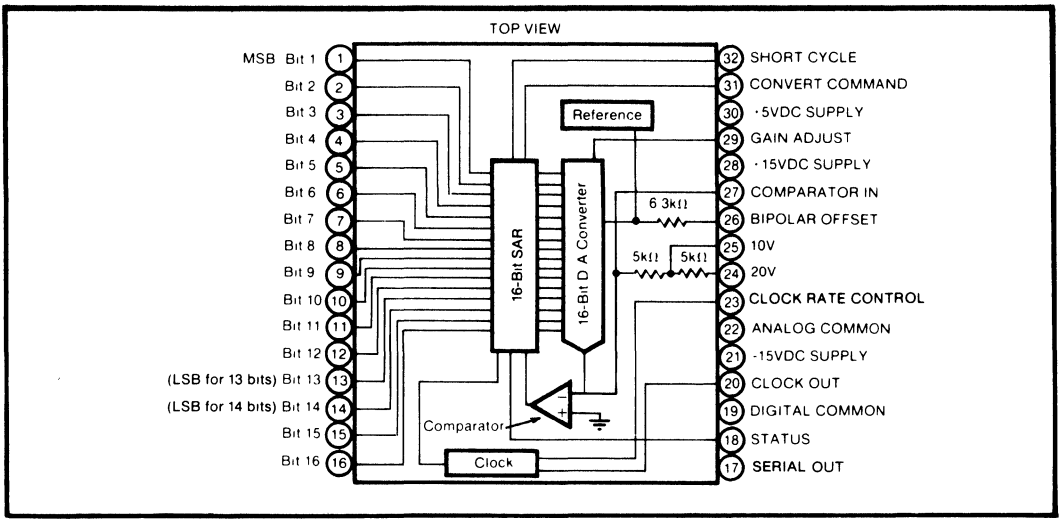
Pin numbers shown for reference only
Numbers may not be marked on package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 720	1 760	43 69	44 70
B	1.120	1 160	28.45	29 46
C	0 170	0 250	4 32	6 35
D	0 16	0 021	0 41	0 53
G	100 BASIC		2 54 BASIC	
H	0 100	0.140	2.54	3 56
K	0 150	0 300	3 81	7 62
L	900 BASIC		22 86 BASIC	
R	0 100	0 140	2 54	3 56

ABSOLUTE MAXIMUM SPECIFICATIONS

$+V_{CC}$ to Common	0V to +16.5V
$-V_{CC}$ to Common	0V to −16.5V
$+V_{DD}$ to Common	0V to +7V
Analog Common to Digital Common	±0.5V
Logic Inputs to Common	0V to V_{DD}
Maximum Power Dissipation	1000mW
Lead Temperature (10s)	300°C

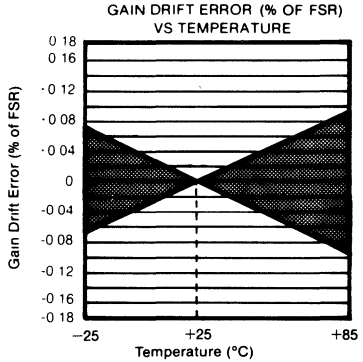
CONNECTION DIAGRAM

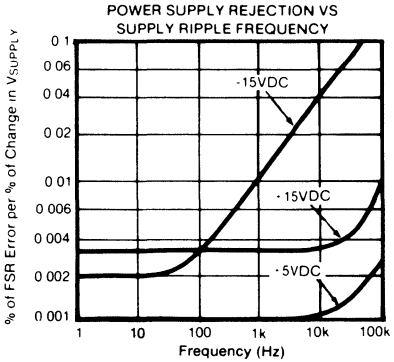


ORDERING INFORMATION

Model	1-24	25-99	100-249
ADC76JG (16-bit)	$167 70	$153 40	$117.70
ADC76JM (13-bit)	175 00	147 00	126 00
ADC76KG (16-bit)	192 50	173 60	141 50
ADC76KM (14-bit)	220 00	185 00	158 00
ADC76AM (13-bit)	255 00	214 00	252 00
ADC76BM (14-bit)	300 00	252 00	216 00

TYPICAL PERFORMANCE CURVES





THEORY OF OPERATION

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the

width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB.

The ADC76 is also Monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that this converter will have no missing codes over a specified temperature range when short cycled for 14-bit operation.

TIMING CONSIDERATIONS

The timing diagram in Figure 2 assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output). Figures 3 and 4 are timing diagrams showing the relationship of serial data to clock and valid data to status.

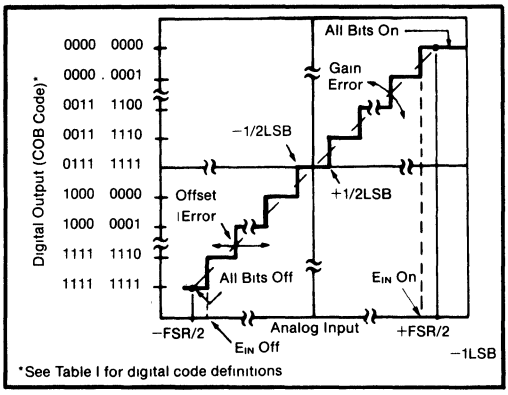


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

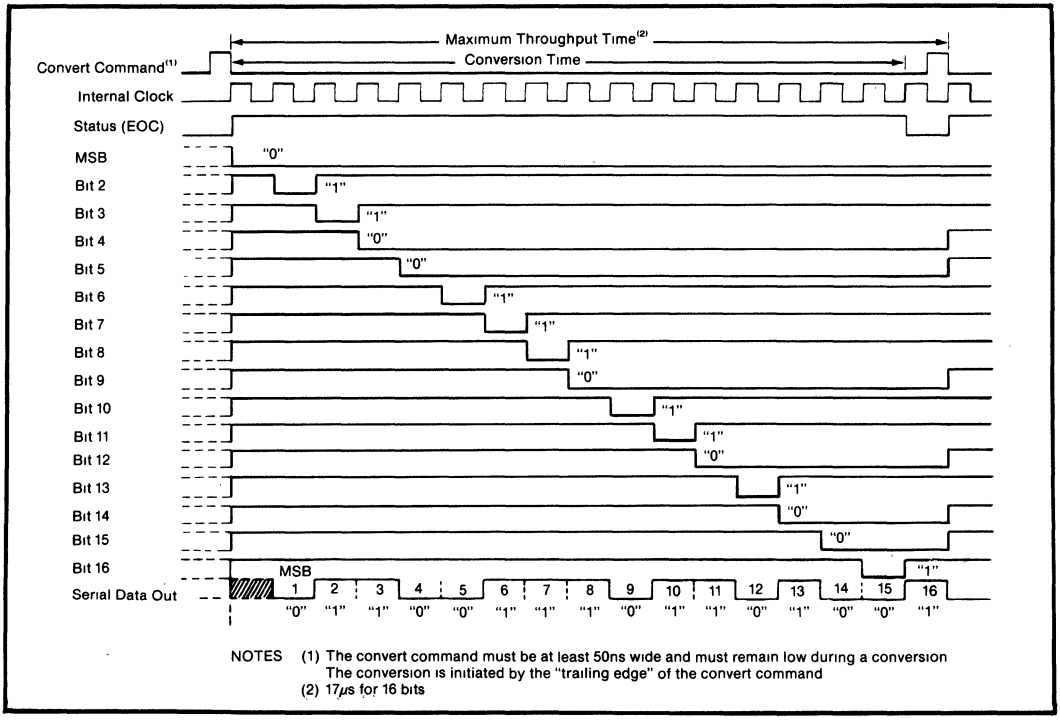


FIGURE 2. ADC76 Timing Diagram.

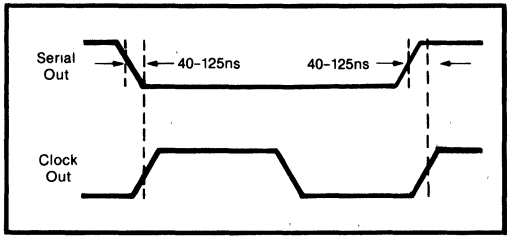


FIGURE 3. Timing Relationship of Serial Data to Clock.

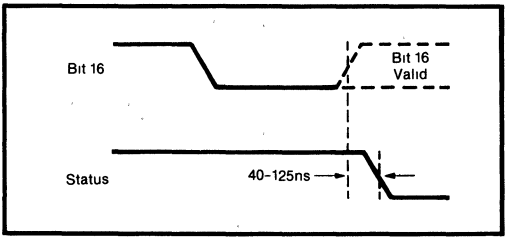


FIGURE 4. Timing Relationship of Valid Data to Status.

DIGITAL CODES

Parallel Data

Two binary codes are available on the ADC76 parallel output: they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges, and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (pin 1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 12-, 13- and 14-bit resolutions. Figure 5 shows the connections for 14-bit resolution, parallel data output, with ±10V input.

Serial Data

Two straight binary (complementary) codes are available on the serial output line; they are CSB and COB. The serial data is available only during conversion and appears with MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagrams of Figures 2 and 3. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As	±10V	+5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB(1) or CTC(2)	COB(1) or CTC(2)	COB(1) or CTC(2)	CSB(3)	CSB(3)	CSB(3)
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	n = 13	2.44mV	1.22mV	610µV	1.22mV	610µV	2.44mV
	n = 14	1.22mV	610µV	305µV	610µV	305µV	1.22mV
Transition Values							
MSB LSB							
000 000(4)	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011 111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111 110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

NOTES (1) COB = Complementary Offset Binary
(2) Complementary Two's Complement—obtained by inverting the most significant bit, MSB (pin 1)
(3) CSB = Complementary Straight Binary
(4) Voltages given are the nominal value for transition to the code specified.

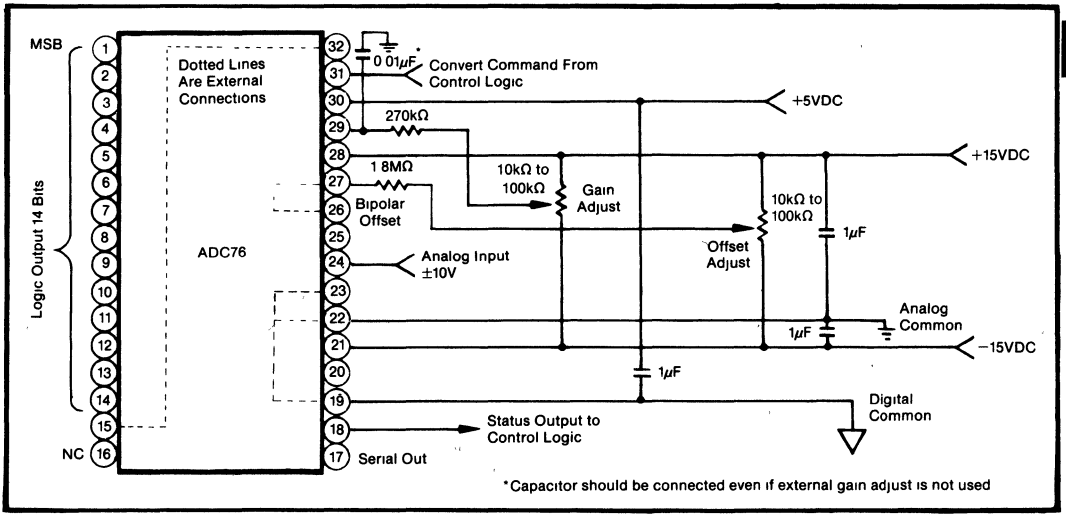


FIGURE 5. ADC76 Connections for: ±10V Analog Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

DISCUSSION OF SPECIFICATIONS

The ADC76 is specified to meet critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. This ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 10 and 11.

POWER SUPPLY SENSITIVITY

Changes in the DC power supply voltages will affect accuracy. The ADC76 power supply sensitivity is specified at ±0.003% of FSR/%V_S for the ±15V supplies and ±0.0015% of FSR/%V_S for the +5V supply. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling, and Figure 7.

LINEARITY ERROR

Linearity error is not adjustable and is the most meaningful indicator of A/D converter accuracy. Linearity is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter.

DIFFERENTIAL LINEARITY ERROR

Differential linearity describes the step size between transition values. A differential linearity error of ±0.003% of FSR indicates that the size of any step may not vary from the ideal step size by more than 0.003% of Full Scale Range.

ACCURACY VERSUS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC76 are shown in Figure 6.

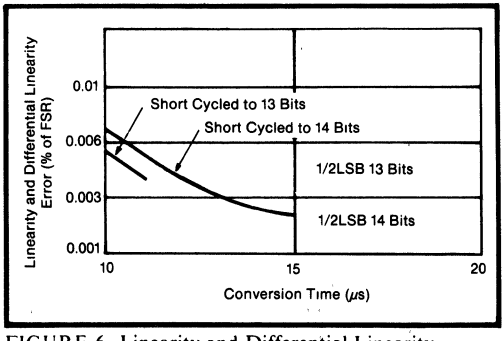


FIGURE 6. Linearity and Differential Linearity Versus Conversion Time.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC76, but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01µF to 0.1µF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic capacitors as shown in Figure 7 to obtain noise free operation. These capacitors should be located close to the ADC.

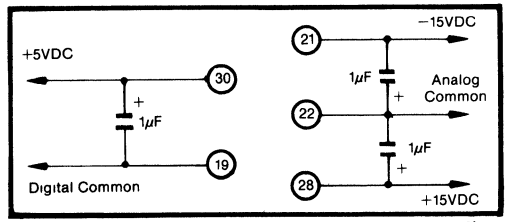


FIGURE 7. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 8 for circuit details.

TABLE II. ADC76 Input Scaling Connections

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
·10V	COB or CTC*	27	Input Sig	24
·5V	COB or CTC*	27	Open	25
·2.5V	COB or CTC*	27	Pin 27	25
0 to ·5V	CSB	22	Pin 27	25
0 to ·10V	CSB	22	Open	25
0 to ·20V	CSB	22	Input Sig	24

*Obtained by inverting MSB pin 1

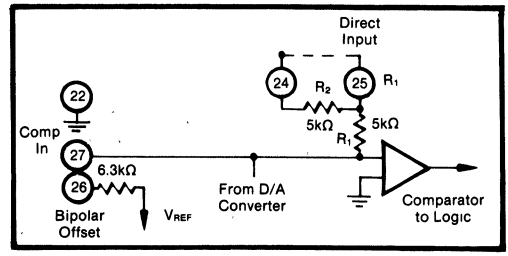


FIGURE 8. ADC76 Input Scaling Circuit.

OUTPUT DRIVE

Normally all ADC76 logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

INPUT IMPEDANCE

The input signal to the ADC76 should be low impedance, such as the output of an op amp, to avoid any errors due to the relatively low input impedance of the ADC76.

If this impedance is not low, a buffer amplifier should be added between the input signal and the direct input to the ADC76 as shown in Figure 9.

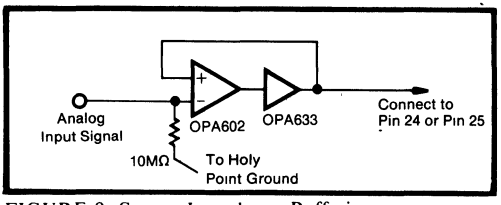


FIGURE 9. Source Impedance Buffering.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 10 and 11. Multiturn potentiometers with 100ppm/°C or better TCRs are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and pin 27 (Offset Adjust) may be left open if no external adjustment is required; however, pin 29 should always be bypassed with 0.01μF to Analog Common.

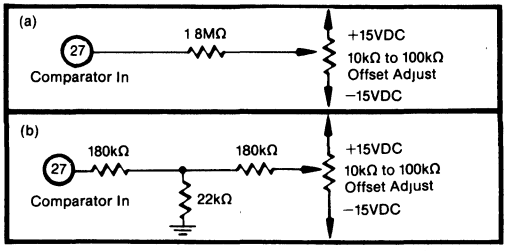


FIGURE 10. Two Methods of Connecting Optional Offset Adjust.

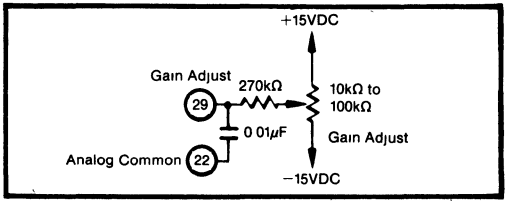


FIGURE 11. Connecting Optional Gain Adjust.

ADJUSTMENT PROCEDURE

Offset—Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 10. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}), Figure 1.

Adjust the Offset potentiometer Until the actual end point transition voltage occurs at (E_{IN}^{OFF}). The ideal transition voltage values of the input are given in Table I.

Gain—Connect the Gain adjust potentiometer as shown in Figure 11. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at (E_{IN}^{ON}).

Table I details the transition voltage levels required.

CONVERT COMMAND CONSIDERATIONS

Convert command resets the converter whenever taken high. This insures a valid conversion on the first conversion after power-up.

Convert command must stay low during a conversion unless it is desired to reset the converter during a conversion.

OPTIONAL CONVERSION TIME ADJUSTMENT

The ADC76 may be operated with faster conversion times for resolutions less than 14 bits by connecting the Short Cycle (pin 32) as shown in Table III. Typical conversion times for the resolution and connections are indicated.

TABLE III. Short Cycle Connections for 12- to 16-Bit Resolutions.

Resolution (Bits)	16	15	14	13	12
Connect Pin 32 to	Open	Pin 16	Pin 15	Pin 14	Pin 13
Typical Conversion Time	17μs	16μs	15μs	13μs	12μs

Clock Rate Control may be connected to an external multiturn trim potentiometer with a TCR of ±10ppm/°C or less as shown in Figure 12. The typical conversion time versus the Clock Rate Control voltage is shown in Figure 13. The effect of varying the conversion time and the resolution on Linearity Error and Differential Linearity Error is shown in Figure 6.

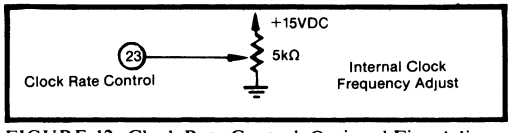


FIGURE 12. Clock Rate Control, Optional Fine Adjust.

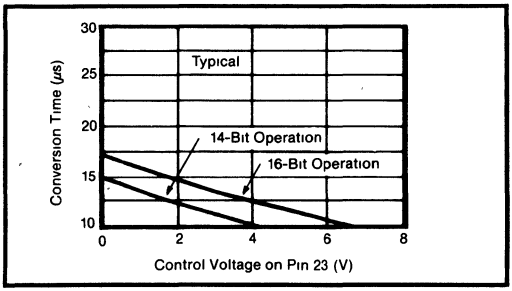


FIGURE 13. Conversion Time vs Clock Rate Control Voltage.

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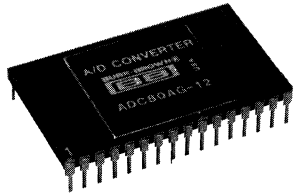


ADC80AG

General Purpose ANALOG-TO-DIGITAL CONVERTER

FEATURES

- INDUSTRY-STANDARD 12-BIT ADC
- LOW COST
- ±0.012% LINEARITY
- 25μs MAX CONVERSION TIME
- ±12V or ±15V OPERATION
- NO MISSING CODES −25°C to +85°C
- HERMETIC 32-PIN PACKAGE
- PARALLEL AND SERIAL OUTPUTS
- 595mW MAX DISSIPATION

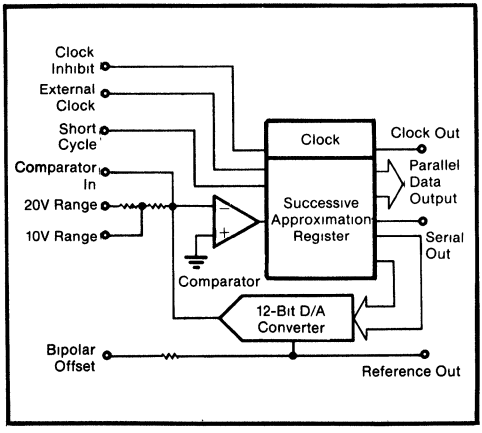
DESCRIPTION

The ADC80 is a 12-bit successive-approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom designed for freedom from latch-up and optimum AC performance. It is complete with a comparator, a monolithic 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, and a CMOS logic chip containing the successive approximation register (SAR), clock, and all other associated logic functions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial endpoint accuracies of better than ±0.12% (±1/2LSB).

The maximum conversion time of 25μs makes the ADC80 ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 40kHz. In addition, the ADC80 may be short-cycled for faster conversion speed with reduced resolution, and an external clock may be used to synchronize the converter to the system clock or to obtain higher-speed operation.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC80 operates equally well with either ±15V or ±12V analog power supplies, and also requires use of a +5V logic power supply. However, unlike many ADC80-type products, a +5V analog power supply is not required. It is packaged in a hermetic 32-pin side-brazed ceramic dual-in-line package.



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PDS-676

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V unless otherwise specified

MODEL	ADC80AG			UNITS
	MIN	TYP	MAX	
RESOLUTION				
ADC80AG-12, ADC80-AGZ-12 [1]			12	Bits
ADC80AG-10			10	Bits
INPUT				
ANALOG				
Voltage Ranges Unipolar		0 to +5, 0 to +10		V
Bipolar		±2 5, +5, +10		V
Impedance 0 to +5V, ±2 5V	2 45	2 5	2 55	kΩ
0 to +10V, +5V	4 9	5	5 1	kΩ
±10V	9 8	10	10 2	kΩ
DIGITAL				
Logic Characteristics (Over specification temperature range)				
V_{IH} (Logic "1")	2 0		5 5	V
V_{IL} (Logic "0")	- 0 3		+0 8	V
I_{IH} (V_{IN} = +2 7V)			150	μA
I_{IL} (V_{IN} = +0 4V)			500	μA
Convert Command Pulse Width [2]	100		2000	ns
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error [3]		±0 1	±0 3	% of FSR [4]
Offset Error [3] Unipolar		±0 05	±0 2	% of FSR
Bipolar		±0 1	±0 3	% of FSR
Linearity Error ADC80AG-12, ADC80AGZ-12			±0 012	% of FSR
ADC80AG-10			±0 048	% of FSR
Differential Linearity Error		±1/2	±3/4	LSB
Inherent Quantization Error		±1/2		LSB
POWER SUPPLY SENSITIVITY				
11 4V ≤ ± V_{CC} ≤ 16 5V		±0 003	±0 009	% of FSR/%V_{CC}
+4 5V ≤ V_{DD} ≤ +5 5V		±0 002	±0 005	% of FSR/%V_{DD}
DRIFT				
Total Accuracy, Bipolar [5]		±10	±23	ppm/°C
Gain		±15	±30	ppm/°C
Offset Unipolar		±3		ppm of FSR/°C
Bipolar		±7	±15	ppm of FSR/°C
Linearity Error Drift		±1	±3	ppm of FSR/°C
Differential Linearity over Temperature Range			±3/4	LSB
No Missing Code Temperature Range	-25		+85	°C
Monotonicity Over Temperature Range		Guaranteed		
CONVERSION TIME [6]				
ADC80AG-12, ADC80AGZ-12	15	22	25	μs
ADC80AG-10	13	20	22	μs
OUTPUT				
DIGITAL (Bits 1-12, Clock Out, Status, Serial Out)				
Output Codes [7]				
Parallel Unipolar		CSB		
Bipolar		COB, CTC		
Serial (NRZ) [8]		CSB, COB		
Logic Levels Logic 0 (I_{SINK} ≤ 3 2mA)			+0 4	V
Logic 1 (I_{SOURCE} ≤ 80μA)	+2 4			V
Internal Clock Frequency		545		kHz
INTERNAL REFERENCE VOLTAGE				
Voltage	+6 2	+6 3	+6 4	V
Source Current Available for External Loads [9]	200			μA
Temperature Coefficient		±10	±30	ppm/°C
POWER SUPPLY REQUIREMENTS (For all models)				
Voltage ±V_{CC}	±11 4	±15	±16 5	V
V_{DD}	+4 5	+5 0	+5 5	V
Current +I_{CC}		5	8 5	mA
-I_{CC}		21	26	mA
I_{DD}		11	15	mA
Power Dissipation (±V_{CC} = 15V)		450	595	mW
Thermal Resistance, θ_{JA}		50		°C/W
TEMPERATURE RANGE (Ambient)				
Specification	-25		+85	°C
Operating (derated specs)	-55		+125	°C
Storage	-65		+150	°C

NOTES (1) ADC80AGZ-12 is not recommended for new designs Standard ADC80AG-12 now meets the extended power supply range of the ADC80AGZ-12 (2) Accurate conversion will be obtained with any convert command pulse width of greater than 100ns, however, it must be limited to 2μs (max) to assure the specified conversion time (3) Gain and offset errors are adjustable to zero See "Optional External Gain and Offset Adjustment" section (4) FSR means Full-Scale Range and is 20V for ±10V range, 10V for ±5V and 0 to +10V ranges, etc (5) Includes drift due to linearity, gain, and offset drifts (6) Conversion time is specified using internal clock For operation with an external clock see "Clock Options" section This converter may also be short-cycled to less than 12-bit resolution for shorter conversion time, see "Short Cycle Feature" section (7) CSB means Complementary Straight Binary, COB means Complementary Offset Binary, and CTC means Complementary Two's Complement coding See Table I for additional information (8) NRZ means Non-Return-to-Zero coding (9) External loading must be constant during conversion, and must not exceed 200μA for guaranteed specification

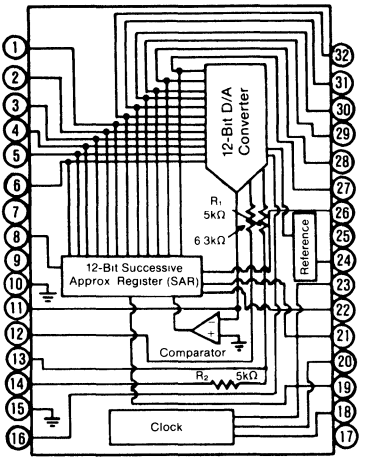
CONNECTION DIAGRAM

Pin 1 - Bit 6
Pin 2 - Bit 5
Pin 3 - Bit 4
Pin 4 - Bit 3
Pin 5 - Bit 2
Pin 6 - Bit 1(MSB)
Pin 7 - N/C *
Pin 8 - Bit 1 ($\overline{MSB}$)
Pin 9 - +5V Digital Supply
Pin 10 - Digital Common
Pin 11 - Comparator In
Pin 12 - Bipolar Offset
Pin 13 - R1 10V Range
Pin 14 - R2 20V Range
Pin 15 - Analog Common
Pin 16 - Gain Adjust

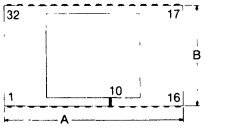
Pin 32 - Bit 7
Pin 31 - Bit 8
Pin 30 - Bit 9
Pin 29 - Bit 10 (LSB—10 Bits)
Pin 28 - Bit 11
Pin 27 - Bit 12 (LSB—12 Bits)
Pin 26 - Serial Out
Pin 25 - $-V_{CC}$
Pin 24 - Ref Out (+6 3V)
Pin 23 - Clock Out
Pin 22 - Status
Pin 21 - Short Cycle
Pin 20 - Clock Inhibit
Pin 19 - External Clock
Pin 18 - Convert Command
Pin 17 - $+V_{CC}$

* +5V applied to pin 7 has no effect on circuit

TOP VIEW

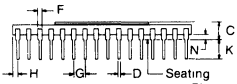


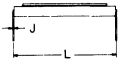
MECHANICAL



Leads in true position within .010" (25MM) R at MMC at Seating Plane

Seal ring is connected to Pin 10





DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.138	.186	3.51	4.72
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

Pin numbers shown for reference only Numbers may not be marked on package

CASE Ceramic, hermetic
MATING CONNECTOR 2302MC
WEIGHT 7 3gm (0 26oz)

ORDERING INFORMATION

Model	Resolution (bits)
ADC80AG-10	10
ADC80AG-12	12
ADC80AG-12Q[1]	12
ADC80AGZ-12[2]	12

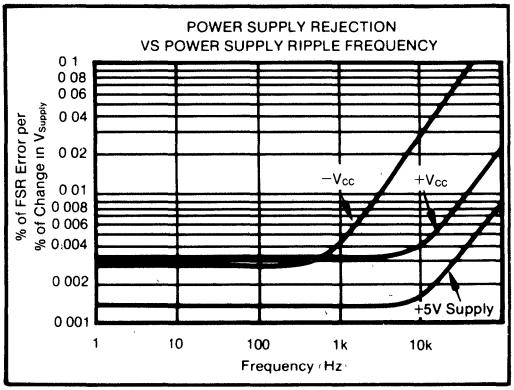
NOTES (1) Q suffix indicates Environmental Screening, see Table IV for details (2) ADC80AGZ-12 is not recommended for new designs Standard ADC80AG-12 now meets the extended power supply range of the ADC80AGZ-12

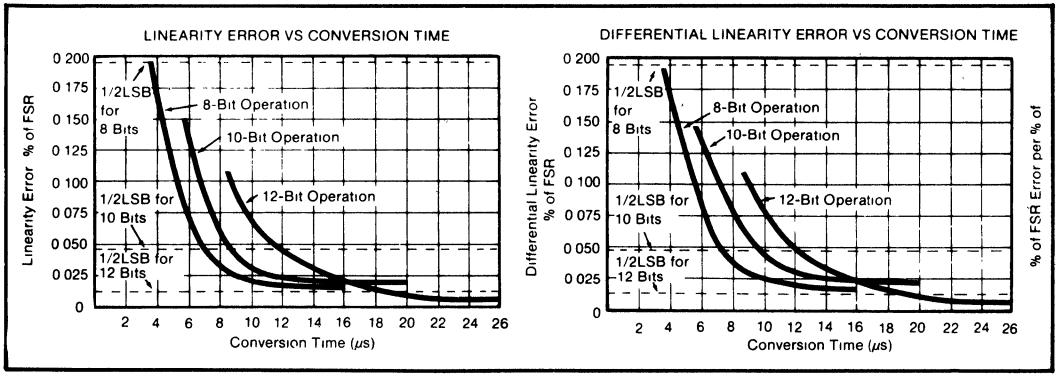
ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Analog Common . . . . . 0 to +16 5V
$-V_{CC}$ to Analog Common . . . . . 0 to −16 5V
V_{DD} to Digital Common . . . . . 0 to +7V
Analog Common to Digital Common . . . . . ±0 5V
Logic Inputs (Convert Command, Clock In) to Digital Common . . . . . −0 3V to V_{DD} +0 5V
Analog Inputs (Analog In, Bipolar Offset) to Analog Common . . . . . ±16 5V
Reference Output . . . . . Indefinite Short to Common, Momentary Short to V_{CC}
Lead Temperature, Soldering . . . . . +300°C, 10s

CAUTION These devices are sensitive to electrostatic discharge Appropriate I C handling procedures should be followed Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device Exposure to absolute maximum conditions for extended periods may affect device reliability

TYPICAL PERFORMANCE CURVES





DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Under this definition of linearity (sometimes referred to as integral linearity), ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale, providing a signficantly better definition of converter accuracy than the best-straight-line-fit definition of linearity employed by some manufacturers.

The zero or minus full-scale value is located at an analog input value 1/2LSB before the first code transition (FFF_H to FFE_H). The plus full-scale value is located at an analog value 3/2LSB beyond the last code transition (001_H to 000_H). See Figure 1 which illustrates these relationships. A linearity specification which guarantees ±1/2LSB maximum linearity error assures the user that no code transition will differ from the ideal transition value by more than ±1/2LSB.

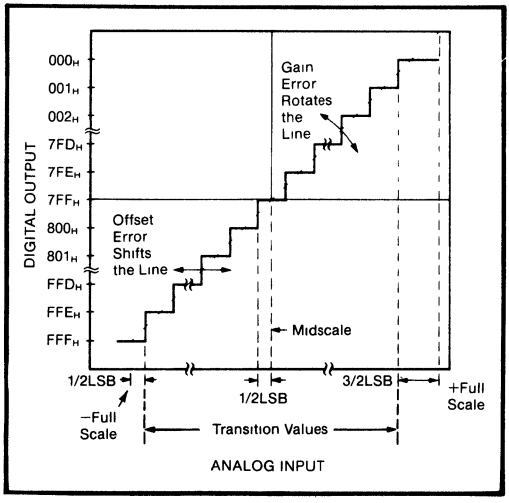


FIGURE 1. ADC80 Transfer Characteristic Terminology.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V operation), the minus full-scale value of −10V is 2.44mV below the first code transition (FFF_H to FFE_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (001_H to 000_H at +9.99268V). Ideal transitions occur 1LSB (4.88mV) apart, and the ±1/2LSB linearity specification guarantees that no actual transition will vary from the ideal by more than 2.44mV. The LSB weights, transition values, and code definitions for each possible ADC80 analog input signal range are described in Table I.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary Output	Input Voltage Range and LSB Values					
Analog Input Voltage Range	Defined As	±10V	±5V	±2 5V	0 to +10V	0 to +5V
Code Designation		COB* or CTC**	COB or CTC	COB or CTC	CSB***	CSB
One Least Significant Bit (LSB)	$FSR/2^n$	$20V/2^n$	$10V/2^n$	$5V/2^n$	$10V/2^n$	$5V/2^n$
	n = 8	78 13mV	39 06mV	19 53mV	39 06mV	19 53mV
	n = 10	19 53mV	9 77mV	4 88mV	9 77mV	4 88mV
	n = 12	4 88mV	2 44mV	1 22mV	2 44mV	1 22mV
Transition Values MSB LSB						
001_H to 000_H	+Full Scale	+10V − 3/2LSB	+5V − 3/2LSB	+2 5V − 3/2LSB	+ 10V − 3/2LSB	+5V − 3/2LSB
800_H to $7FF_H$	Mid Scale	0	0	0	+5V	+ 2 5V
FFF_H to FFE_H	−Full Scale	−10V + 1/2LSB	−5V + 1/2LSB	−2 5V + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

*COB = Complementary Offset Binary **CTC = Complementary Two's Complement—obtained by using the complement of the most significant bit (MSB) MSB is available on pin 8
***CSB = Complementary Straight Binary

CODE WIDTH (QUANTUM)

Code width (or quantum) is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB, which for 12-bit operation with a 20V span is equal to 4.88mV. Refer to Table I for LSB values for other ADC80 input ranges.

DIFFERENTIAL LINEARITY ERROR AND NO MISSING CODES

Differential linearity error is the difference between an ideal 1LSB code width (quantum) and the actual code width. A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input is increased throughout the range, requiring that every input quantum must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur but the converter may still be monotonic. Thus, no missing codes represent a more stringent definition of performance than does monotonicity. ADC80 is guaranteed to have no missing codes to 12-bit resolution over its full specification temperature range.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

UNIPOLAR OFFSET ERROR

An ADC80 connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value, and is applicable only to converters operating in the unipolar mode.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset at the first transition value above the minus full-scale value. The ADC80 follows this convention. Thus, bipolar offset error for the ADC80 is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB above minus full scale.

GAIN ERROR

The last output code transition (001_H to 000_H) occurs for an analog input value 3/2LSB below the nominal plus full-scale value. Gain error is the deviation of the actual analog value at the last transition point from the ideal value.

ACCURACY DRIFT VS TEMPERATURE

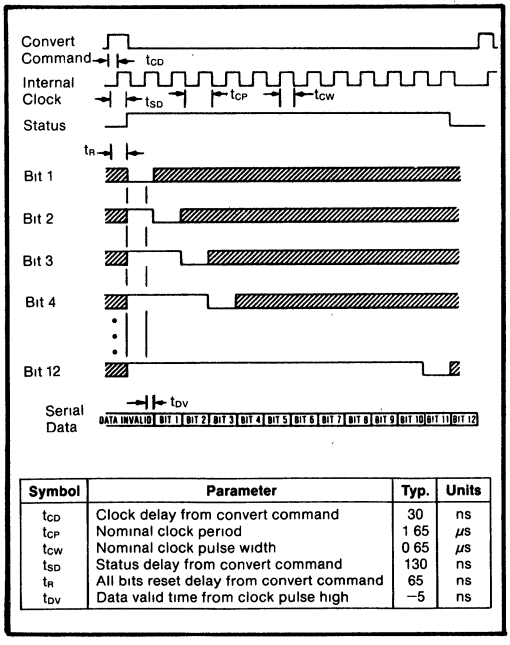
The temperature coefficients for gain, unipolar offset, and bipolar offset specify the maximum change from the actual 25°C value to the value at the extremes of the Specification temperature range. The temperature coefficient applies independently to the two halves of the temperature range above and below +25°C.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC80 assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the plus full-scale value. This change, of course, results in a proportional change in all code transition values (i.e., a gain error). The specification describes the maximum change in the plus full-scale value from the initial value for independent changes in each power supply voltage.

TIMING CONSIDERATIONS

Timing relationships of the ADC80 are shown in Figure 2. It should be noted that although the convert command pulse width must be between 100ns and 2μs to obtain the specified conversion time with internal clock, the ADC80 will accept longer convert commands with no loss of accuracy, assuming that the analog input signal is stable.



Symbol	Parameter	Typ.	Units
t_{CD}	Clock delay from convert command	30	ns
t_{CP}	Nominal clock period	1 65	μs
t_{CW}	Nominal clock pulse width	0 65	μs
t_{SD}	Status delay from convert command	130	ns
t_R	All bits reset delay from convert command	65	ns
t_{DV}	Data valid time from clock pulse high	−5	ns

FIGURE 2. ADC80 Timing Diagram (nominal values at +25°C with internal clock).

In this situation, the actual indicated conversion time (during which status is high) for 12-bit operation will be equal to approximately 1μs less than the sum of the factory-set conversion time and the length of the convert command. The code returned by the converter at the end of the conversion will accurately represent the analog input to the converter at the time the status returns to the

low state. In addition, although the initial state of the converter will be indeterminate when power is first applied, it is designed to time-out and be ready to accept a convert command within approximately 25μs after power-up, provided that either an external clock source is present or the internal clock is not inhibited.

During conversion, the decision as to the proper state of any bit (bit "n") is made on the rising edge of clock pulse "n + 1". Thus, a complete conversion requires 13 clock pulses with the status output dropping from logic "1" to logic "0" shortly after the rising edge of the 13th clock pulse, and with valid output data ready to be read at that time. A new conversion may not be initiated until 50ns after the fall of the last clock pulse (pulse 13 for 12-bit operation).

Additional convert commands applied during conversion will be ignored.

DEFINITION OF DIGITAL CODES

Parallel Data

Three binary codes are available on the ADC80 parallel output; all three are complementary codes, meaning that logic "0" is true. The available codes are complementary straight binary (CSB) for unipolar input signal ranges, and complementary offset binary (COB) and complementary two's complement (CTC) for bipolar input signal ranges. CTC coding is obtained by complementing bit 1 (the MSB) of the COB code; the complement of bit 1 is available on pin 8.

Serial Data

Two (complementary) straight binary codes are available on the serial output of the ADC80; as in the parallel case, they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values of Table I also apply to the serial data output, except that the CTC code is not available. All clock pulses available from the ADC80 have equal pulse widths to facilitate transfer of the serial data into external logic devices without external shaping.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected together internally in the ADC80, but should be connected together as close to the unit as possible, preferably to an analog common ground plane beneath the converter. If these common lines must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog input lines and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common. If external gain and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC80 as possible.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 1μF to 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation: Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC80 will be driving into a nominal DC input impedance of 2.5kΩ to 10kΩ depending upon the range selected. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

INPUT SCALING

The ADC80 offers five standard input ranges: 0V to +5V, 0V to +10V, ±2.5V, ±5V, and ±10V. The input range should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the converter. Select the appropriate input range as indicated by Table II. The input circuit architecture is illustrated in Figure 3. External padding resistors can be added to modify the factory-set input ranges (such as addition of a small external input resistor to change the 10V range to a 10.24V range). Alternatively, the gain range of the converter may easily be increased a small amount by use of a low temperature coefficient potentiometer in series with the analog input signal or by decreasing the value of the gain adjust series resistor in Figure 5.

TABLE II. ADC80 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0 to +5V	CSB	15	Pin 11	13
0 to +10V	CSB	15	Open	13

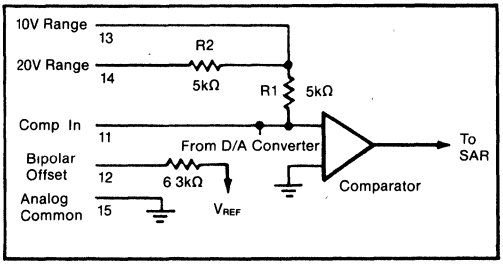


FIGURE 3. ADC80 Input Scaling Circuit.

CALIBRATION

Optional External Gain And Offset Adjustments

Gain and offset errors may be trimmed to zero using external offset and gain trim potentiometers connected to the ADC80 as shown in Figures 4 and 5 for both unipolar and bipolar operation. Multiturn potentiometers with 100ppm/°C or better TCR are recommended for minimum drift over temperature and time. These pots may be of any value between 10kΩ and 100kΩ. All fixed resistors should be 20% carbon or better. Although not necessary in some applications, pin 16 (Gain Adjust) should be preferably bypassed with a 0.01μF nonpolarized capacitor to analog common to minimize noise pickup at this high impedance point, even if no external adjustment is required.

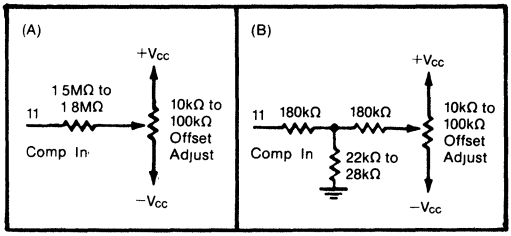


FIGURE 4. Two Methods of Connecting Optional Offset Adjust.

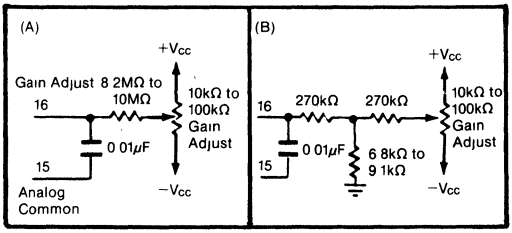


FIGURE 5. Two Methods of Connecting Optional Gain Adjust.

Adjustment Procedure

OFFSET—Connect the offset potentiometer as shown in Figure 4. Set the input voltage to the nominal zero or minus full-scale voltage plus 1/2LSB. For example, referring to Table I, this value is −10V +2.44mV or −9.99756V for the −10V to +10V range.

With the input voltage set as above, adjust the offset potentiometer until an output code is obtained which is alternating between FFE_H and FFF_H with approximately 50% occurrence of each of the two codes. In other words, the potentiometer is adjusted until bit 12 (the LSB) indicates a true (logic "0") condition approximately half the time.

GAIN—Connect the gain adjust potentiometer as shown in Figure 5. Set the input voltage to the nominal plus full-scale value minus 3/2LSB. Once again referring to Table I, this value is +10V −7.32mV or +9.99268V for the −10V to +10V range. Adjust the gain potentiomter until the output code is alternating between 000_H and 001_H with an approximate 50% duty cycle. As in the case of offset adjustment, this procedure sets the converter end-point transitions to a precisely known value.

CLOCK OPTIONS

The ADC80 is extremely versatile in that it can be operated in several different modes with either internal or external clock. Most of these options can be implemented with inexpensive TTL logic as shown in Figures 6 through 9. When operating with an external clock, the conversion time may be as short as 15μs (800kHz external clock frequency) with assured performance within specified limits. When operating with the internal clock, pin 19 (external clock input) and pin 20 (clock inhibit) may be left unconnected. No external pull-ups are required due to the inclusion of pull-up resistors in the ADC80. Pin 20 (clock inhibit) must be grounded for use with an external clock, which is applied to pin 19.

SHORT-CYCLE FEATURE

A short-cycle input (pin 21) permits the conversion to be terminated after any number of desired bits has been converted, allowing shorter conversion times in applications not requiring full 12-bit resolution. In these situations, the short-cycle pin should be connected to the bit output pin of the next bit after the desired resolution. For example, when 10-bit resoltion is desired, pin 21 is connected to pin 28 (bit 11). In this example, the conversion cycle terminates and status is reset after the bit 10 decision. Short-cycle pin connections and associated maximum 12-, 10-, and 8-bit conversion times (with internal clock) are shown in Table III. Also shown are recommended minimum conversion times (external clock) for these conversion lengths to obtain the stated accuracies. The ADC80 is not factory-tested for these external clock conversion speeds and the product is not guaranteed to achieve the stated accuracies under these operating conditions; the recommended values are offered as an aid to the user.

TABLE III. Short-Cycle Connections and Conversion Times for 8-, 10-, and 12-Bit Resolutions—ADC80.

Resolution (Bits)	12	10	8
Connect pin 21 to	Pin 9 or NC	Pin 28	Pin 30
Maximum Conversion Time[1] Internal Clock (μs)	25	22	18
Minimum Conversion Time[1] External Clock (μs)	15	13	10
Maximum Linearity Error At +25°C (% of FSR)	0 012	0 048	0 20

NOTE (1) Conversion time to maintain ±1/2LSB linearity error

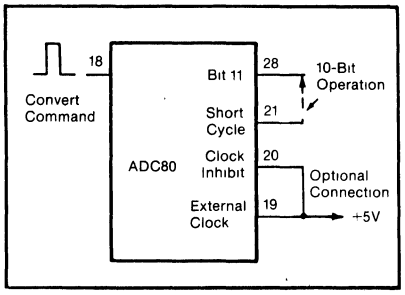


FIGURE 6. Internal Clock—Normal Operating Mode. (Conversion initiated by the rising edge of the convert command. The internal clock runs only during conversion.)

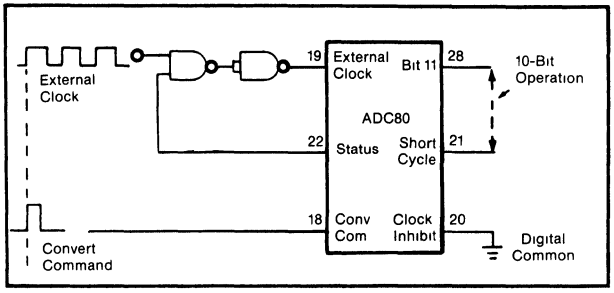


FIGURE 7. Continuous External Clock. (Conversion initiated by rising edge of convert command. The convert command must be synchronized with clock.)

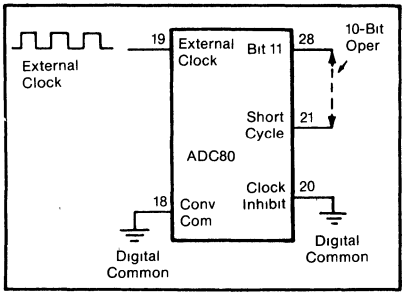


FIGURE 8. Continuous Conversion with External Clock. (Conversion is initiated by 14th clock pulse. Clock runs continuously.)

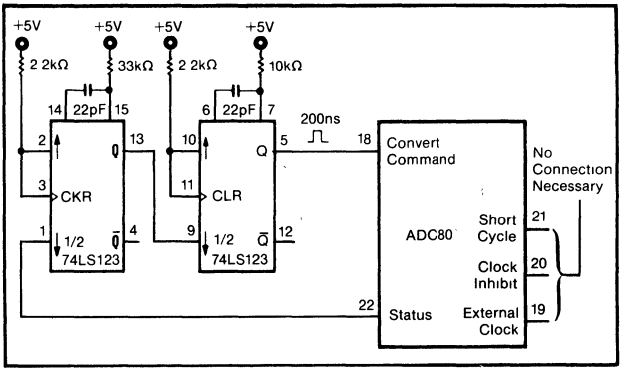


FIGURE 9. Continuous Conversion with 600ns between Conversions. (Circuit insures that conversion will start when power is applied.)

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown Q models are environmentally screened versions of our standard industrial products, designed to provide enhanced reliability. The screening illustrated in Table IV is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient way of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

TABLE IV. Screening Flow for ADC80AG-12Q.

Screen	MIL-STD-883 Method, Condition	Screening Level
Internal Visual	Burr-Brown QC4118	
High Temperature Storage (Stabilization Bake)	1008, C	24 hour, +150°C
Temperature Cycling	1010, C	10 cycles, −65°C to +150°C
Constant Acceleration	2001, A	5000 G
Electrical Test	Burr-Brown test procedure	
Burn-in	1015, B	160 hour, +125°C, steady-state
Hermeticity Fine Leak Gross Leak	 1014, A1 or A2 1014, C	 5×10^{-7} atm cc/s bubble test only, preconditioning omitted
Final Electrical	Burr-Brown test procedure	
Final Drift	Burr-Brown test procedure	
External Visual	Burr-Brown QC5150	

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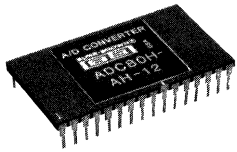


ADC80H*

AVAILABLE IN DIE FORM

***Not Recommended for New Designs. Use ADC80AG.**

General Purpose ANALOG-TO-DIGITAL CONVERTER

FEATURES

- PIN-COMPATIBLE WITH INDUSTRY STANDARD ADC80
- <600mW POWER DISSIPATION
- 15μsec CONVERSION TIME WITH EXTERNAL CLOCK
- 25μSEC MAXIMUM CONVERSION TIME
- ±0.012% INTEGRAL LINEARITY
- 12-BIT RESOLUTION
- FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES
- NO MISSING CODES −25°C TO +85°C
- PARALLEL AND SERIAL OUTPUTS
- 32-PIN HERMETIC PACKAGE

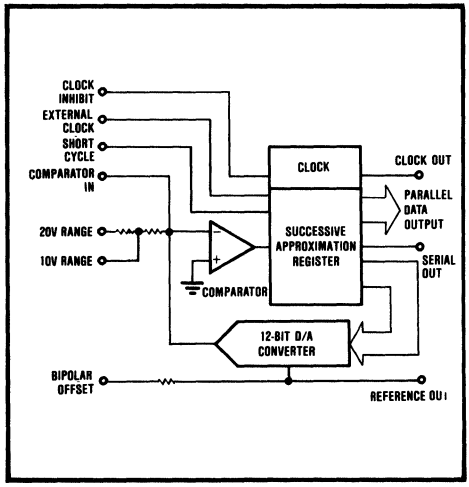
DESCRIPTION

The ADC80H is a 12-bit successive-approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom designed for freedom from latch-up and optimum AC performance. It is complete with a comparator, a monolithic 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, and a CMOS logic chip containing the successive approximation register (SAR), clock, and all other associated logic functions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial end-point accuracies of better than ±0.012% (±1/2LSB). Like the industry standard ADC80, the ADC80H is completely specified for −25°C to +85°C operation.

The maximum conversion time of 25μsec makes the ADC80H ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 40kHz. In addition, the ADC80H may be short-cycled for faster conversion speed with reduced resolution, and an external clock may be used to synchronize the converter to the system clock or to obtain higher-speed operation.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC80H operates equally well with either ±15V or ±12V analog power supplies, and also requires use of a +5V logic power supply. However, unlike other ADC80-type products, a +5V analog power supply is not required. It is packaged in a hermetic 32-pin side-brazed ceramic dual-in-line package.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V unless otherwise specified

MODEL	ADC80H-AH-12			UNITS
	MIN	TYP	MAX	
RESOLUTION			12	Bits
INPUT				
ANALOG				
Voltage Ranges Unipolar		0 to +5, 0 to +10		V
Bipolar		±2 5, ±5, ±10		V
Impedance 0 to +5V, ±2 5V		2 3		kΩ
0 to +10V, +5V		4 6		kΩ
±10V		9 2		kΩ
DIGITAL				
Logic Characteristics (Over specification temperature range)				
V_{IH} (Logic "1")	2.0		5.5	V
V_{IL} (Logic "0")	−0.3		+0 8	V
I_{IH} (V_{IN} = +2 7V)			−150	μA
I_{IL} (V_{IN} =+0.4V)			500	μA
Convert Command Pulse Width[1]	100		2000	nsec
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error[2]		±0 1	±0.3	% of FSR[3]
Offset Error[2]: Unipolar		±0.05	±0.2	% of FSR
Bipolar		±0.1	±0.3	% of FSR
Linearity Error			±0.012	% of FSR
Differential Linearity Error			±3/4	LSB
Inherent Quantization Error		1/2		LSB
POWER SUPPLY SENSITIVITY				
+13.5V ≤ +V_{CC} ≤ +16.5V or +11.4V ≤ +V_{CC} ≤ +12.6V		±0.003	±0.009	% of FSR/%V_{CC}
−16.5V ≤ −V_{CC} ≤ −13.5V or −12.6V ≤ −V_{CC} ≤ −11.4V		±0.003	±0.009	% of FSR/%V_{CC}
+4.5V ≤ V_{DD} ≤ +5.5V		±0.002	±0.005	% of FSR/%V_{DD}
DRIFT				
Total Accuracy, Bipolar[4]		±10	±23	ppm/°C
Gain		±15	±30	ppm/°C
Offset: Unipolar		±3		ppm of FSR/°C
Bipolar		±7	±15	ppm of FSR/°C
Linearity Error Drift		±1	±3	ppm of FSR/°C
Differential Linearity over Temperature Range			±3/4	LSB
No Missing Code Temperature Range	−25		+85	°C
Monotonicity Over Temperature Range		Guaranteed		
CONVERSION TIME[5]	15	22	25	μsec
OUTPUT				
DIGITAL(Bits 1-12, Clock Out, Status, Serial Out)				
Output Codes[6]				
Parallel. Unipolar		CSB		
Bipolar		COB, CTC		
Serial (NRZ)[7]		CSB, COB		
Logic Levels Logic 0 (I_{sink} ≤ 3.2mA)			+0.4	V
Logic 1 (I_{source} ≤ 80μA)	+2.4V			V
Internal Clock Frequency		545		kHz
INTERNAL REFERENCE VOLTAGE				
Voltage	+6 2	+6.3	+6 4	
Source Current Available for External Loads[8]	200			μA
Temperature Coefficient		±10	±30	ppm/°C
POWER SUPPLY REQUIREMENTS				
Voltage, ±V_{CC}	±11 4	±15	±16 5	V
V_{DD}	+4 5	+5 0	+5 5	V
Current, +I_{CC}		5	8.5	mA
−I_{CC}		21	26	mA
I_{DD}		11	15	mA
Power Dissipation (±V_{CC} = 15V)		450	595	mW
TEMPERATURE RANGE (Ambient)				
Specification	−25		+85	°C
Storage	−65		+150	°C

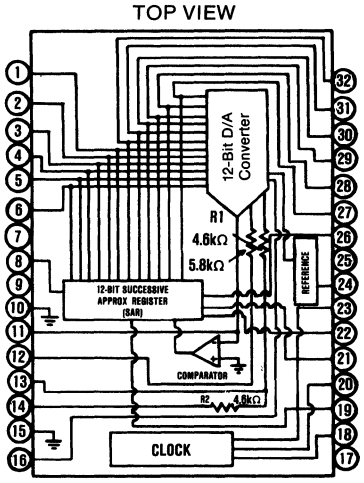
NOTES (1) Accurate conversion will be obtained with any convert command pulse width of greater than 100nsec; however, it must be limited to 2μsec (max) to assure the specified conversion time (2) Gain and offset errors are adjustable to zero See "Optional External Gain and Offset Adjustments" section (3) FSR means Full-Scale Range and is 20V for ±10V range, 10V for ±5V and 0 to +10V ranges, etc (4) Includes drift due to linearity, gain, and offset drifts (5) Conversion time is specified using internal clock For operation with an external clock see "Clock Options" section This converter may also be short-cycled to less than 12-bit resolution for shorter conversion time, see "Short Cycle Feature" section (6) CSB means Complementary Straight Binary, COB means Complementary Offset Binary, and CTC means Complementary Two's Complement coding See Table I for additional information (7) NRZ means non-return-to-zero coding (8) External loading must be constant during conversion, and must not exceed 200μA for guaranteed specification

CONNECTION DIAGRAM

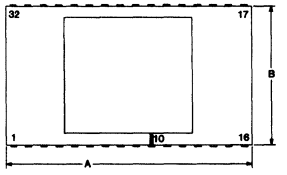
Pin 1 - Bit 6
Pin 2 - Bit 5
Pin 3 - Bit 4
Pin 4 - Bit 3
Pin 5 - Bit 2
Pin 6 - Bit 1(MSB)
Pin 7 - N/C
Pin 8 - Bit 1 ($\overline{\text{MSB}}$)
Pin 9 - +5V Digital Supply
Pin 10 - Digital Common
Pin 11 - Comparator In
Pin 12 - Bipolar Offset
Pin 13 - R1 10V Range
Pin 14 - R2 20V Range
Pin 15 - Analog Common
Pin 16 - Gain Adjust

Pin 32 - Bit 7
Pin 31 - Bit 8
Pin 30 - Bit 9
Pin 29 - Bit 10
Pin 28 - Bit 11
Pin 27 - Bit 12 (LSB)
Pin 26 - Serial Out
Pin 25 - $-V_{CC}$
Pin 24 - Ref Out (+6 3V)
Pin 23 - Clock Out
Pin 22 - Status
Pin 21 - Short Cycle
Pin 20 - Clock Inhibit
Pin 19 - External Clock
Pin 18 - Convert Command
Pin 17 - $+V_{CC}$

TOP VIEW



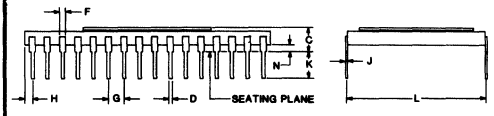
MECHANICAL



Leads in true position within .010" (.25MM) R at MMC at Seating Plane

Pin numbers shown for reference only Numbers may not be marked on package

S/R is connected to Pin 10



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.138	.186	3.51	4.72
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

CASE Ceramic, hermetic
MATING CONNECTOR 2302MC
WEIGHT 7 3gm (0 26oz)

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Analog Common ..... 0 to +16 5V
$-V_{CC}$ to Analog Common ..... 0 to −16 5V
V_{DD} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±0 5V
Logic Inputs (Convert Command, Clock In) to Digital Common ..... −0 3V to V_{DD} +0 5V
Analog Inputs (Analog In, Bipolar Offset) to Analog Common ..... ±16 5V
Reference Output ..... Indefinite Short to Common, Momentary Short to V_{CC}
Power Dissipation 1000mW
Lead Temperature, Soldering ..... +300°C, 10sec
Thermal Resistance, θ_{JA} ..... 60°C/W

CAUTION These devices are sensitive to electrostatic discharge Appropriate I C handling procedures should be followed

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device Exposure to absolute maximum conditions for extended periods may affect device reliability

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Under this definition of linearity (sometimes referred to as integral linearity), ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale, providing a significantly better definition of converter accuracy than the best-straight-line-fit definition of linearity employed by some manufacturers.

The zero or minus full-scale value is located at an analog input value 1/2LSB before the first code transition (FFF_H to FFE_H). The plus full-scale value is located at an analog value 3/2LSB beyond the last code transition (001_H to 000_H). See Figure 1 which illustrates these relationships. A linearity specification which guarantees ±1/2LSB maximum linearity error assures the user that no code transition will differ from the ideal transition value by more than ±1/2LSB.

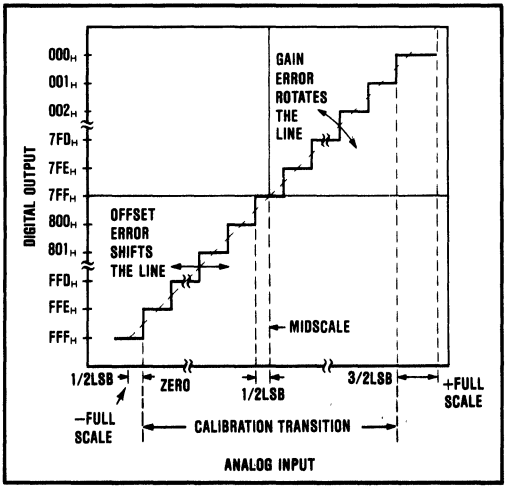


FIGURE 1. ADC80H Transfer Characteristic Terminology.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V operation), the minus full-scale value of −10V is 2.44mV below the first code transition (FFF_H to FFE_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (001_H to 000_H at +9.99268V). Ideal transitions occur 1LSB (4.88mV) apart, and the ±1/2LSB linearity specification guarantees that no actual transition will vary from the ideal by more than 2.44mV. The LSB weights, transition values, and code definitions for each possible ADC80H analog input signal range are described in Table I.

CODE WIDTH (QUANTUM)

Code width (or quantum) is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB, which for 12-bit operation with a 20V span is equal to 4.88mV. Refer to Table I for LSB values for other ADC80H input ranges.

DIFFERENTIAL LINEARITY ERROR AND NO MISSING CODES

Differential linearity error is a definition of the difference between an ideal 1LSB code width (quantum) and the actual code width. A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input is increased throughout the range, requiring that every input quantum must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur but the converter may still be monotonic. Thus, no missing codes represent a more stringent definition of performance than does monotonicity. ADC80H is guaranteed to have no missing codes to 12-bit resolution over its full specification temperature range.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

UNIPOLAR OFFSET ERROR

An ADC80H connected for uniplolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value, and is applicable only to converters operating in the unipolar mode.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset at the first transition value above the minus full-scale value. The ADC80H follows this convention. Thus, bipolar offset error for the ADC80H is

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	Input Voltage Range and LSB Values					
Analog Input Voltage Range	Defined As	±10V	±5V	±2 5V	0 to +10V	0 to +5V
Code Designation		COB* or CTC**	COB or CTC	COB or CTC	CSB***	CSB
One Least Significant Bit (LSB)	FSR/2^n	20V/2^n	10V/2^n	5V/2^n	10V/2^n	5V/2^n
	n = 8	78 13mV	39 06mV	19 53mV	39 06mV	19 53mV
	n = 10	19 53mV	9 77mV	4.88mV	9 77mV	4 88mV
	n = 12	4 88mV	2 44mV	1 22mV	2 44mV	1 22mV
Transition Values MSB LSB						
001_H to 000_H	+Full Scale	+10V − 3/2LSB	+5V − 3/2LSB	+2 5V − 3/2LSB	+ 10V − 3/2LSB	+5V − 3/2LSB
800_H to $7FF_H$	Mid Scale	0	0	0	+5V	+ 2 5V
FFF_H to FFE_H	−Full Scale	−10V + 1/2LSB	−5V + 1/2LSB	−2 5V + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

*COB = Complementary Offset Binary **CTC = Complementary Two's Complement—obtained by using the complement of the most significant bit ($\overline{MSB}$) $\overline{MSB}$ is available on pin 8
***CSB = Complementary Straight Binary

defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB above minus full scale.

GAIN ERROR

The last output code transition (001_H to 000_H) occurs for an analog input value 3/2LSB below the nominal plus full-scale value. Gain error is the deviation of the actual analog value at the last transition point from the ideal value.

ACCURACY DRIFT VS TEMPERATURE

The temperature coefficients for gain, unipolar offset, and bipolar offset specify the maximum change from the actual 25°C value to the value at the extremes of the specification range. The temperature coefficient applies independently to the two halves of the temperature range above and below +25°C.

POWER SUPPLY SENSITIVITY

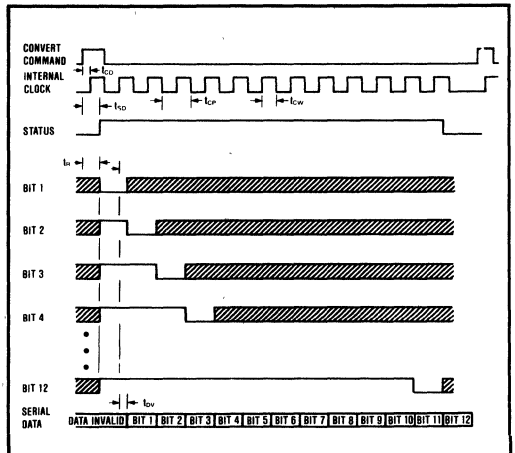
Electrical specifications for the ADC80H assume the application of the rated power supply voltages of+5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the plus full-scale value. This change, of course, results in a proportional change in all code transition values (i.e. a gain error). The specification describes the maximum change in the plus full-scale value from the initial value for independent changes in each power supply voltage.

TIMING CONSIDERATIONS

Timing relationships of the ADC80H are shown in Figure 2. It should be noted that although the convert command pulse width must be between 100nsec and 2μsec to obtain the specified conversion time with internal clock, the ADC80H will accept longer convert commands with no loss of accuracy, assuming that the analog input signal is stable.In this situation, the actual indicated conversion time (during which status is high) for 12-bit operation will be equal to approximately 1μsec less than the sum of the factory-set conversion time and the length of the convert command. The code returned by the converter at the end of the conversion will accurately represent the analog input to the converter at the time the convert command returns to the low state. In addition, although the initial state of the converter will be indeterminate when power is first applied, it is designed to time-out and be ready to accept a convert command within approximately 25μsec after power-up, provided that either an external clock source is present or the internal clock is not inhibited.

During conversion, the decision as to the proper state of any bit (bit "n") is made on the rising edge of clock pulse "n + 1". Thus, a complete conversion requires 13 clock pulses with the status output dropping from logic "1" to logic "0" shortly after the rising edge of the 13th clock pulse, and with valid output data ready to be read at that time. A new conversion may not be initiated until 50nsec after the fall of the last clock pulse (pulse 13 for 12-bit operation).

Additional convert commands applied during conversion will be ignored.



Symbol	Parameter	Typ.	Units
t_{CD}	Clock delay from convert command	30	nsec
t_{CP}	Nominal clock period	1.65	μsec
t_{CW}	Nominal clock pulse width	0.65	μsec
t_{SD}	Status delay from convert command	130	nsec
t_R	All bits reset delay from convert command	65	nsec
t_{DV}	Data valid time from clock pulse high	−35	nsec

FIGURE 2. ADC80H Timing Diagram (nominal values at +25°C with internal clock).

DEFINITION OF DIGITAL CODES

Parallel Data

Three binary codes are available on the ADC80H parallel output; all three are complementary codes, meaning that logic "0" is true. The available codes are complementary straight binary (CSB) for unipolar input signal ranges, and complementary offset binary (COB) and complementary two's complement (CTC) for bipolar input signal ranges. CTC coding is obtained by complementing bit 1 (the MSB) relative to its normal state for CSB or COB coding; the complement of bit 1 is available on pin 8.

Serial Data

Two (complementary) straight binary codes are available on the serial output of the ADC80H; as in the parallel case, they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values of Table I also apply to the serial data output, except that the CTC code is not available. All clock pulses available from the ADC80H have equal pulse widths to facilitate transfer of the serial data into external logic devices without external shaping.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected together internally in the ADC80H, but should be connected together as close to the unit as possible, preferably to an analog common ground plane beneath the converter. If these common lines must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog input lines and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common. If external gain and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC80H as possible.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 1μF to 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC80H will be driving into a nominal DC input impedance of 2.3kΩ to 9.2kΩ depending upon the range selected. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

INPUT SCALING

The ADC80H offers five standard input ranges: 0V to +5V, 0V to +10V, ±2.5V, ±5V, and ±10V. The input range should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the converter. Select the appropriate input range as indicated by Table II. The input circuit architecture is illustrated in Figure 3. Use of external padding resistors to modify the factory-set input ranges (such as addition of a small external input resistor to change the 10V range to a 10.24V range) will require matching of the external fixed resistor values to individual devices, due to the large tolerance of the internal input resistors. Alternatively, the gain range of the converter may easily be increased a small amount by use of a low temperature coefficient potentiometer in series with the analog input signal or by the decreasing the value of the gain adjust series resistor in Figure 5.

TABLE II. ADC80H Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0 to +5V	CSB	15	Pin 11	13
0 to +10V	CSB	15	Open	13

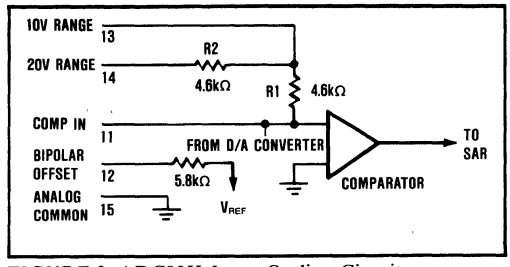


FIGURE 3. ADC80H Input Scaling Circuit.

CALIBRATION

Optional External Gain And Offset Adjustments

Gain and offset errors may be trimmed to zero using external offset and gain trim potentiometers connected to the ADC80H as shown in Figures 4 and 5 for both unipolar and bipolar operation. Multiturn potentiometers with 100ppm/°C or better TCR are recommended for minimum drift over temperature and time. These

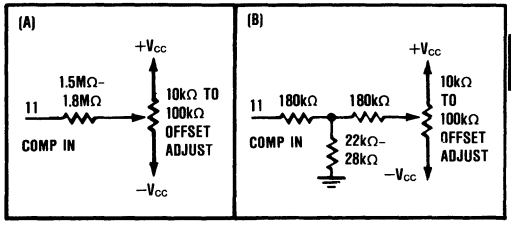


FIGURE 4. Two Methods of Connecting Optional Offset Adjust.

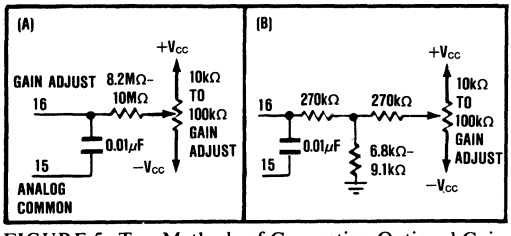


FIGURE 5. Two Methods of Connecting Optional Gain Adjust.

pots may be of any value between 10kΩ and 100kΩ. All fixed resistors should be 20% carbon or better. Although not necessary in some applications, pin 16 (Gain Adjust) should be preferably bypassed with a 0.01μF nonpolarized capacitor to analog common to minimize noise pickup at this high impedance point, even if no external adjustment is required.

Adjustment Procedure

OFFSET—Connect the offset potentiometer as shown in Figure 4. Set the input voltage to the nominal zero or minus full-scale voltage plus 1/2LSB. For example, referring to Table I, this value is −10V +2.44mV or −9.99756V for the −10V to +10V range.

With the input voltage set as above, adjust the offset potentiometer until an output code is obtained which is alternating between FFE_H and FFF_H with approximately 50% occurence of each of the two codes. In other words, the potentiometer is adjusted until bit 12 (the LSB) indicates a true (logic "0") condition approximately half the time.

GAIN—Connect the gain adjust potentiometer as shown in Figure 5. Set the input voltage to the nominal plus full-scale value minus 3/2LSB. Once again referring to Table I, this value is +10V −7.32mV or +9.99268V for the −10V to +10V range. Adjust the gain potentiometer until the output code is alternating between 000_H and 001_H with an approximate 50% duty cycle. As in the case of offset adjustment, this procedure sets the converter end-point transition to a precisely known value.

CLOCK OPTIONS

The ADC80H is extremely versatile in that it can be operated in several different modes with either internal or external clock. Most of these options can be implemented with inexpensive TTL logic as shown in Figures 6 through 9. When operating with an external clock, the conversion time may be as short as 15μsec (800kHz external clock frequency) with assured performance within specified limits. When operating with the internal clock, pin 19 (external clock input) and pin 20 (clock inhibit) may be left unconnected. No external pull-ups are required due to the inclusion of pull-up resistors in the ADC80H. Pin 20 (clock inhibit) must be grounded for use with an external clock, which is applied to pin 19.

SHORT-CYCLE FEATURE

A short-cycle input (pin 21) permits the conversion to be terminated after any number of desired bits has been converted, allowing shorter conversion times in applica-

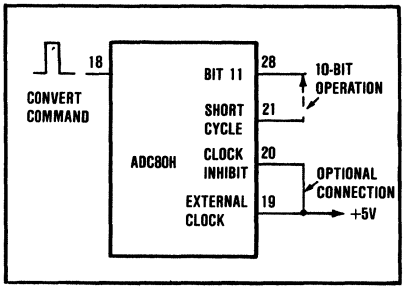


FIGURE 6. Internal Clock—Normal Operating Mode. (Conversion initiated by the rising edge of the convert command. The internal clock runs only during conversion.)

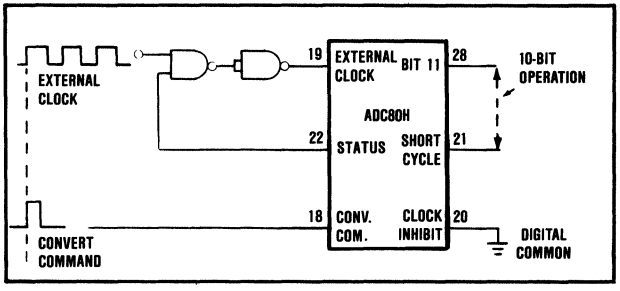


FIGURE 7. Continuous External Clock. (Conversion initiated by rising edge of convert command. The convert command must be synchronized with clock.)

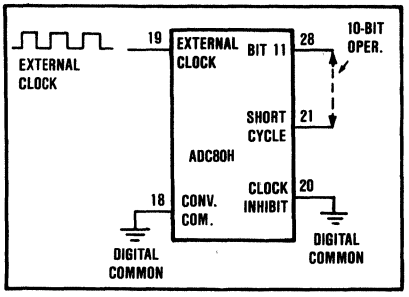


FIGURE 8. Continuous Conversion with External Clock. (Conversion is initiated by 14th clock pulse. Clock runs continuously.)

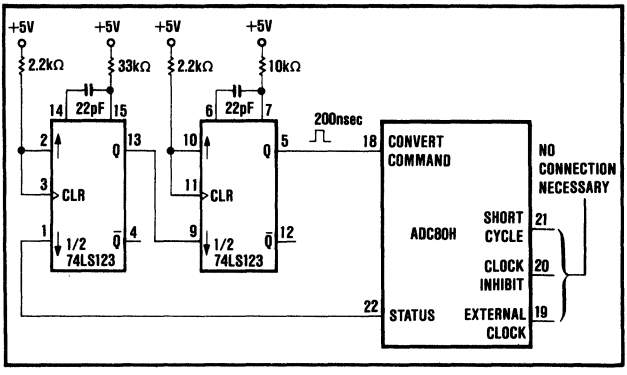


FIGURE 9. Continuous Conversion with 600nsec between Conversions. (Circuit insures that conversion will start when power is applied.)

tions not requiring full 12-bit resolution. In these situations, the short-cycle pin should be connected to the bit output pin of the next bit after the desired resolution. For example, when 10-bit resolution is desired, pin 21 is connected to pin 28 (bit 11). In this example, the conversion cycle terminates and status is reset after the bit 10 decision. Short-cycle pin connections and associated maximum 12-, 10-, and 8-bit conversion times (with internal clock) are shown in Table III. Also shown are recommended minimum conversion times (external clock) for these conversion lengths to obtain the stated accuracies. The ADC80H is not factory-tested for these external clock conversion speeds and the product is not guaranteed to achieve the stated accuracies under these operating conditions; the recommended values are offered as an aid to the user.

TABLE III. Short-Cycle Connections and Conversion Times for 8-, 10-, and 12-Bit Resolutions—ADC80H.

Resolution (Bits)	12	10	8
Connect pin 21 to	Pin 9 or NC	Pin 28	Pin 30
Maximum Conversion Time[1] Internal Clock (μsec)	25	22	18
Minimum Conversion Time[1] External Clock (μsec)	15	13	10
Maximum Linearity Error At +25°C (% of FSR)	0.012	0.048	0.20

NOTE (1) Conversion time to maintain ±1/2LSB linearity error

ENVIRONMENTAL SCREENING

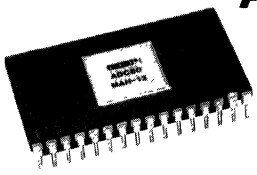
The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown Q models are environmentally screened versions of our standard industrial products, designed to provide enhanced reliability. The screening illustrated in Table IV is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient way of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

TABLE IV. Screening Flow for ADC80H-AH-12Q

Screen	MIL-STD-883 Method, Condition	Screening Level
Internal Visual	Burr-Brown QC4118	
High Temperature Storage (Stabilization Bake)	1008, C	24 hour, +150°C
Temperature Cycling	1010, C	10 cycles, −65°C to +150°C
Constant Acceleration	2001, A	5000 G
Electrical Test	Burr-Brown test procedure	
Burn-in	1015, B	160 hour, +125°C, steady-state
Hermeticity Fine Leak Gross Leak	1014, A1 or A2 1014, C	5×10^{-7} atm cc/sec bubble test only, preconditioning omitted
Final Electrical	Burr-Brown test procedure	
Final Drift	Burr-Brown test procedure	
External Visual	Burr-Brown QC5150	

BURR-BROWN®

ADC80MAH-12



AVAILABLE IN DIE FORM

Monolithic 12-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- INDUSTRY-STANDARD 12-BIT ADC
- MONOLITHIC CONSTRUCTION
- LOW COST
- ±0.012% LINEARITY
- 25μs MAX CONVERSION TIME
- ±12V or ±15V OPERATION
- NO MISSING CODES −25°C to +85°C
- HERMETIC 32-PIN PACKAGE
- PARALLEL OR SERIAL OUTPUTS
- 705mW MAX DISSIPATION

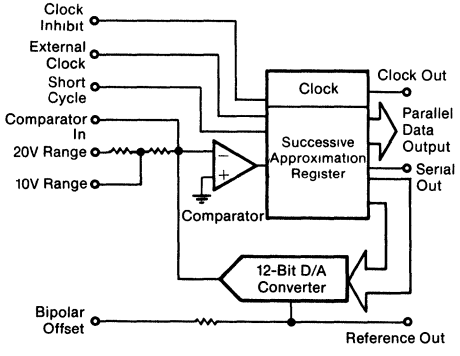
DESCRIPTION

The ADC80MAH-12 is a 12-bit single-chip successive-approximation analog-to-digital converter for low cost converter applications. It is complete with a comparator, a 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, a successive approximation register (SAR), clock, and all other associated logic functions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial end-point accuracies of better than ±0.12% (±1/2LSB).

The maximum conversion time of 25μs makes the ADC80MAH-12 ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 40kHz. In addition, this A/D converter may be short-cycled for faster conversion speed with reduced resolution, and an external clock may be used to synchronize the converter to the system clock or to obtain higher-speed operation. The convert command circuits have been redesigned to allow simplified free-running operation with internal or external clock.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC80MAH-12 operates equally well with either ±15V or ±12V analog power supplies, and also requires use of a +5V logic power supply. However, unlike many ADC80-type products, a +5V analog power supply is not required. It is packaged in a hermetic 32-pin side-brazed ceramic dual-in-line package.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex. 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V unless otherwise specified

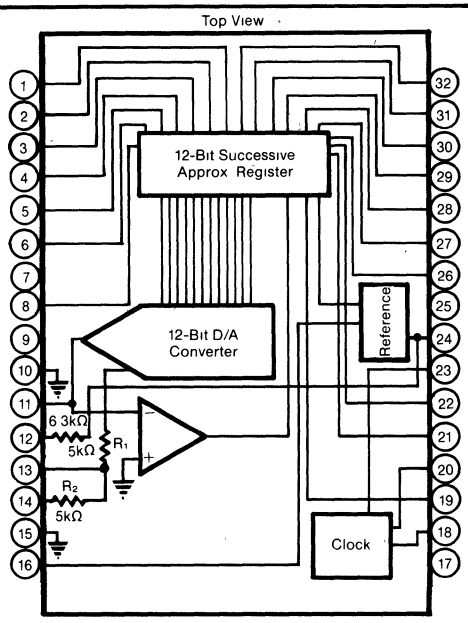
MODEL	ADC80MAH-12			
	MIN	TYP	MAX	UNITS
RESOLUTION			12	Bits
INPUT				
ANALOG				
Voltage Ranges Unipolar		0 to +5, 0 to +10		V
Bipolar		±2 5, ±5, ±10		V
Impedance 0 to +5V, ±2 5V	2 45	2 5	2 55	kΩ
0 to +10V, ±5V	4 9	5	5 1	kΩ
±10V	9 8	10	10 2	kΩ
DIGITAL				
Logic Characteristics (Over specification temperature range)				
V_{IH} (Logic "1")	2 0		5 5	V
V_{IL} (Logic "0")	−0 3		+0 8	V
I_{IH} (V_{IN} = +2 7V)			20	μA
I_{IL} (V_{IN} = +0 4V)	−20			μA
Convert Command Pulse Width[1]	100ns		20	μs
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error[2]		±0 1	±0 3	% of FSR[3]
Offset Error[2] Unipolar		±0 05	±0 2	% of FSR
Bipolar		±0 1	±0 3	% of FSR
Linearity Error			±0 012	% of FSR
Differential Linearity Error		±1/2	±3/4	LSB
Inherent Quantization Error		±1/2		LSB
POWER SUPPLY SENSITIVITY				
11 4V ≤ ± V_{CC} ≤ 16 5V		±0 003	±0 009	% of FSR/%V_{CC}
+4 5V ≤ V_{DD} ≤ +5 5V		±0 002	±0 005	% of FSR/%V_{DD}
DRIFT				
Total Accuracy, Bipolar[4]		±10	±23	ppm/°C
Gain		±15	±30	ppm/°C
Offset Unipolar		±3		ppm of FSR/°C
Bipolar		±7	±15	ppm of FSR/°C
Linearity Error Drift		±1	±3	ppm of FSR/°C
Differential Linearity over Temperature Range			±3/4	LSB
No Missing Code Temperature Range	−25		+85	°C
Monotonicity Over Temperature Range		Guaranteed		
CONVERSION TIME[5]		22	25	μs
OUTPUT				
DIGITAL (Bits 1–12, Clock Out, Status, Serial Out)				
Output Codes[6]				
Parallel Unipolar		CSB		
Bipolar		COB, CTC		
Serial (NRZ)[7]		CSB, COB		
Logic Levels Logic 0 (I_{SINK} ≤ 3 2mA)			+0 4	V
Logic 1 (I_{SOURCE} ≤ 80μA)	+2 4			V
Internal Clock Frequency		520		kHz
INTERNAL REFERENCE VOLTAGE				
Voltage	+6 20	+6 3	+6 40	V
Source Current Available for External Loads[8]	200			μA
Temperature Coefficient		±10	±30	ppm/°C
POWER SUPPLY REQUIREMENTS				
Rated Supply Voltages		+5, ±12 or ±15		V
Supply Ranges ±V_{CC}	±11 4		±16 5	V
V_{DD}	+4.5		+5 5	V
Supply Drain +I_{CC} (+V_{CC} = 15V)		8 5	11	mA
−I_{CC} (−V_{CC} = 15V)		21	24	mA
I_{DD} (V_{CC} = 5V)		30	36	mA
Power Dissipation (±V_{CC} = 15V, V_{DD} = 5V)		593	705	mW
Thermal Resistance, θ_{JA}		50		°C/W
TEMPERATURE RANGE (Ambient)				
Specification	−25		+85	°C
Operating (derated specs)	−55		+125	°C
Storage	−65		+150	°C

NOTES: (1) Accurate conversion will be obtained with any convert command pulse width of greater than 100ns, however, it must be limited to 20μs (max) to assure the specified conversion time. (2) Gain and offset errors are adjustable to zero See "Optional External Gain and Offset Adjustment" section. (3) FSR means Full-Scale Range and is 20V for ±10V range, 10V for ±5V and 0 to +10V ranges, etc (4) Includes drift due to linearity, gain, and offset drifts (5) Conversion time is specified using internal clock For operation with an external clock see "Clock Options" section. This converter may also be short-cycled to less than 12-bit resolution for shorter conversion time, see "Short Cycle Feature" section (6) CSB means Complementary Straight Binary, COB means Complementary Offset Binary, and CTC means Complementary Two's Complement coding See Table I for additional information (7) NRZ means Non-Return-to-Zero coding (8) External loading must be constant during conversion, and must not exceed 200μA for guaranteed specification

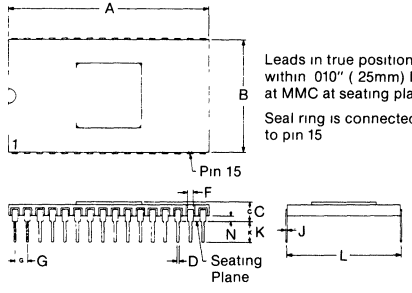
CONNECTION DIAGRAM

Pin 1	Bit 6	Pin 32	Bit 7
Pin 2	Bit 5	Pin 31	Bit 8
Pin 3	Bit 4	Pin 30	Bit 9
Pin 4	Bit 3	Pin 29	Bit 10 (LSB—10 Bits)
Pin 5	Bit 2	Pin 28	Bit 11
Pin 6	Bit 1 (MSB)	Pin 27	Bit 12 (LSB—12 Bits)
Pin 7	N/C*	Pin 26	Serial Out
Pin 8	Bit 1 (MSB)	Pin 25	$-V_{CC}$
Pin 9	+5V Digital Supply	Pin 24	Reference Out (+6 3V)
Pin 10	Digital Common	Pin 23	Clock Out
Pin 11	Comparator In	Pin 22	Status
Pin 12	Bipolar Offset	Pin 21	Short Cycle
Pin 13	R1 10V Range	Pin 20	Clock Inhibit
Pin 14	R2 20V Range	Pin 19	External Clock
Pin 15	Analog Common	Pin 18	Convert Command
Pin 16	Gain Adjust	Pin 17	$+V_{CC}$

* +5V applied to pin 7 has no effect on circuit



MECHANICAL



Leads in true position within .010" (.25mm) R at MMC at seating plane

Seal ring is connected to pin 15

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.584	1.616	40.23	41.05
B	.885	.905	22.48	22.99
C	.124	.166	3.15	4.22
D	.016	.020	0.41	0.51
F	.045	.055	1.14	1.40
G	100 BASIC		2.54 BASIC	
J	.009	.012	0.23	0.30
K	.165	.175	4.19	4.45
L	.900 BASIC		22.86 BASIC	
N	.040	.060	1.02	1.52

CASE Ceramic, hermetic
MATING CONNECTOR 2302MC
WEIGHT 8.4gm (0.29oz)

ORDERING INFORMATION

Model	Resolution (bits)
ADC80MAH-12	12
ADC80MAH-12/QM[1]	12
BURN-IN SCREENING OPTION	
Model	**Burn-In Temp. (160h)[2]**
ADC80MAH-12-BI	+125°C

NOTE (1) Environmental Screening, see Table IV (2) Or equivalent See text

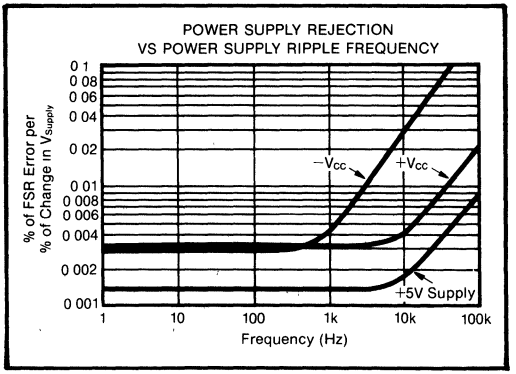
ABSOLUTE MAXIMUM RATINGS

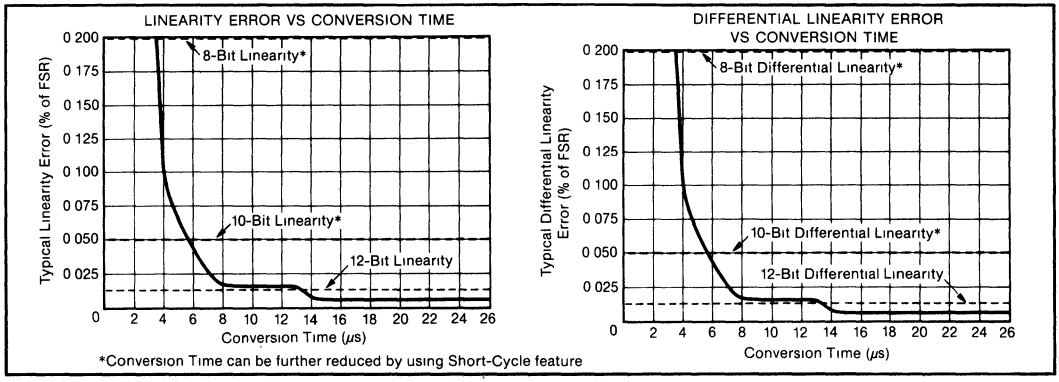
$+V_{CC}$ to Analog Common . . . . . 0 to +16.5V
$-V_{CC}$ to Analog Common . . . . . 0 to −16.5V
V_{DD} to Digital Common . . . . . 0 to +7V
Analog Common to Digital Common . . . . . ±0.5V
Logic Inputs (Convert Command, Clock In) to Digital Common . . . . . −0.3V to $+V_{CC}$
Analog Inputs (Analog In, Bipolar Offset) to Analog Common . . . . . ±16.5V
Reference Output . . . . . Indefinite Short to Common, Momentary Short to V_{CC}
Lead Temperature, Soldering . . . . . +300°C, 10s
Maximum Junction Temperature . . . . . +160°C

CAUTION These devices are sensitive to electrostatic discharge. Appropriate I C handling procedures should be followed

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device Exposure to absolute maximum conditions for extended periods may affect device reliability

TYPICAL PERFORMANCE CURVES





DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Under this definition of linearity (sometimes referred to as integral linearity), ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale, providing a significantly better definition of converter accuracy than the best-straight-line-fit definition of linearity employed by some manufacturers.

The zero or minus full-scale value is located at an analog input value 1/2LSB before the first code transition (FFF_H to FFE_H). The plus full-scale value is located at an analog value 3/2LSB beyond the last code transition (001_H to 000_H). See Figure 1 which illustrates these relationships. A linearity specification which guarantees ±1/2LSB maximum linearity error assures the user that no code transition will differ from the ideal transition value by more than ±1/2LSB.

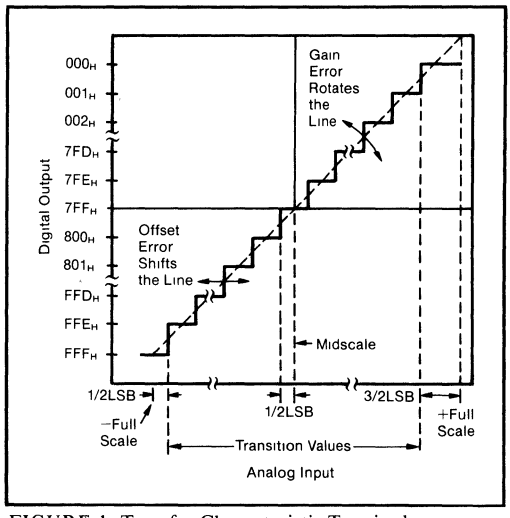


FIGURE 1. Transfer Characteristic Terminology.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V operation), the minus full-scale value of −10V is 2.44mV below the first code transition (FFF_H to FFE_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (001_H to 000_H at +9.99268V). Ideal transitions occur 1LSB (4.88mV) apart, and the ±1/2LSB linearity specification guarantees that no actual transition will vary from the ideal by more than 2.44mV. The LSB weights, transition values, and code definitions for each possible ADC80 analog input signal range are described in Table I.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary Output	Input Voltage Range and LSB Values					
Analog Input Voltage Range	Defined As	±10V	±5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB[1] or CTC[2]	COB or CTC	COB or CTC	CSB[3]	CSB
One Least Significant Bit (LSB)	FSR/2^n	20V/2^n	10V/2^n	5V/2^n	10V/2^n	5V/2^n
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values						
MSB LSB						
001_H to 000_H	+ Full Scale	+10V − 3/2LSB	+5V − 3/2LSB	+2.5V − 3/2LSB	+10V − 3/2LSB	+5V − 3/2LSB
800_H to $7FF_H$	Midscale	0	0	0	+5V	+2.5V
FFF_H to FFE_H	− Full Scale	−10V + 1/2LSB	−5V + 1/2LSB	−2.5V + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

NOTES (1) COB = Complementary Offset Binary (2) CTC = Complementary Two's Complement—obtained by using the complement of the most significant bit (MSB) $\overline{MSB}$ is available on pin 8 (3) CSB = Complementary Straight Binary

CODE WIDTH (QUANTUM)

Code width (or quantum) is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB, which for 12-bit operation with a 20V span is equal to 4.88mV. Refer to Table I for LSB values for other ADC80 input ranges.

DIFFERENTIAL LINEARITY ERROR AND NO MISSING CODES

Differential linearity error is the difference between an ideal 1LSB code width (quantum) and the actual code width. A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input is increased throughout the range, requiring that every input quantum must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur but the converter may still be monotonic. Thus, no missing codes represent a more stringent definition of performance than does monotonicity. ADC80 is guaranteed to have no missing codes to 12-bit resolution over its full specification temperature range.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

UNIPOLAR OFFSET ERROR

An ADC80 connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value, and is applicable only to converters operating in the unipolar mode.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset at the first transition value above the minus full-scale value. The ADC80 follows this convention. Thus, bipolar offset error for the ADC80 is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB above minus full scale.

GAIN ERROR

The last output code transition (001_H to 000_H) occurs for an analog input value 3/2LSB below the nominal plus full-scale value. Gain error is the deviation of the actual analog value at the last transition point from the ideal value.

ACCURACY DRIFT VS TEMPERATURE

The temperature coefficients for gain, unipolar offset, and bipolar offset specify the maximum change from the actual 25°C value to the value at the extremes of the Specification temperature range. The temperature coefficient applies independently to the two halves of the temperature range above and below +25°C.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC80 assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the plus full-scale value. This change, of course, results in a proportional change in all code transition values (i.e., a gain error). The specification describes the maximum change in the plus full-scale value from the initial value for independent changes in each power supply voltage.

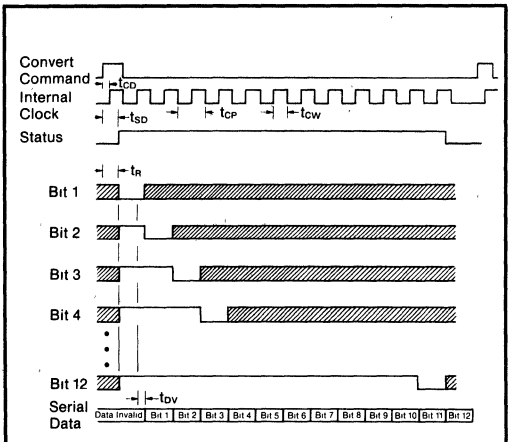
TIMING CONSIDERATIONS

Timing relationships of the ADC80 are shown in Figure 2.

During conversion, the decision as to the proper state of any bit (bit "n") is made on the rising edge of clock pulse "n + 1". Thus, a complete conversion requires 13 clock pulses with the status output dropping from logic "1" to logic "0" shortly after the falling edge of the 13th clock pulse, and with valid output data ready to be read at that time.

Additional convert commands applied during conversion will be ignored.

Status remains high until after the falling edge of the 13th clock pulse. This allows direct use of status for latching parallel data.



Symbol	Parameter	Typ.	Units
t_{CD}	Clock delay from convert command	153	ns
t_{CP}	Nominal clock period	1 81	µs
t_{CW}	Nominal clock pulse width	0 87	µs
t_{SD}	Status delay from convert command	186	ns
t_R	All bits reset delay from convert command	141	ns
t_{DV}	Data valid time from clock pulse high	−15	ns

FIGURE 2. Timing Diagram (nominal values at +25°C with internal clock).

DEFINITION OF DIGITAL CODES

Parallel Data

Three binary codes are available on the ADC80 parallel output; all three are complementary codes, meaning that logic "0" is true. The available codes are complementary straight binary (CSB) for unipolar input signal ranges, and complementary offset binary (COB) and complementary two's complement (CTC) for bipolar input signal ranges. CTC coding is obtained by complementing bit 1 (the MSB) relative to its normal state for CSB or COB coding; the complement of bit 1 is available on pin 8.

Serial Data

Two (complementary) straight binary codes are available on the serial output of the ADC80; as in the parallel case, they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values of Table I also apply to the serial data output, except that the CTC code is not available. All clock pulses available from the ADC80 have equal pulse widths to facilitate transfer of the serial data into external logic devices without external shaping.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected together internally in the ADC80, but should be connected together as close to the unit as possible, preferably to an analog common ground plane beneath the converter. If these common lines must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog input lines and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common. If external gain and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC80 as possible. Capacitive loading on comparator and input pins should be kept to a minimum to maintain converter performance.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 1μF to 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC80 will be driving into a nominal DC input impedance of 2.3kΩ to 9.2kΩ depending upon the range selected. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

INPUT SCALING

The ADC80 offers five standard input ranges: 0V to +5V, 0V to +10V, ±2.5V, ±5V, and ±10V. The input range should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the converter. Select the appropriate input range as indicated by Table II. The input circuit architecture is illustrated in Figure 3. External padding resistors can be added to modify the factory-set input ranges (such as addition of a small external input resistor to change the 10V range to a 10.24V range). Alternatively, the gain range of the converter may easily be increased a small amount by use of a low temperature coefficient potentiometer in series with the analog input signal or by decreasing the value of the gain adjust series resistor in Figure 5.

TABLE II. Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0 to +5V	CSB	15	Pin 11	13
0 to +10V	CSB	15	Open	13

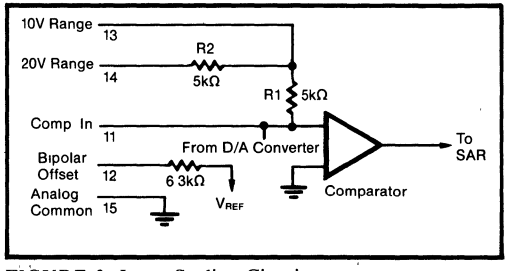


FIGURE 3. Input Scaling Circuit.

CALIBRATION

Optional External Gain And Offset Adjustments

Gain and offset errors may be trimmed to zero using external offset and gain trim potentiometers connected to the ADC80 as shown in Figures 4 and 5 for both unipolar and bipolar operation. Multiturn potentiometers with 100ppm/°C or better TCR are recommended for minimum drift over temperature and time. These pots may be of any value between 10kΩ and 100kΩ. All fixed resistors should be 20% carbon or better. Although not necessary in some applications, pin 16 (Gain Adjust) should be preferably bypassed with a 0.01μF nonpolarized capacitor to analog common to minimize noise pickup at this high impedance point, even if no external adjustment is required.

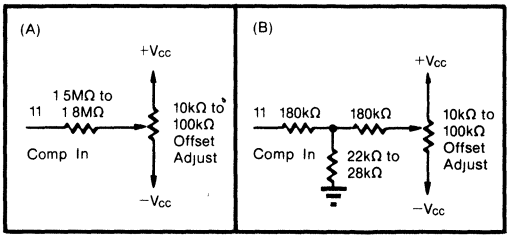


FIGURE 4. Two Methods of Connecting Optional Offset Adjust.

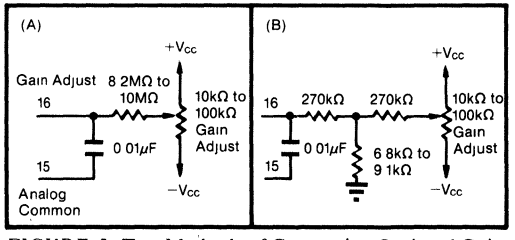


FIGURE 5. Two Methods of Connecting Optional Gain Adjust.

Adjustment Procedure

OFFSET—Connect the offset potentiometer as shown in Figure 4. Set the input voltage to the nominal zero or minus full-scale voltage plus 1/2LSB. For example, referring to Table I, this value is −10V +2.44mV or −9.99756V for the −10V to +10V range.

With the input voltage set as above, adjust the offset potentiometer until an output code is obtained which is alternating between FFE_H and FFF_H with approximately 50% occurrence of each of the two codes. In other words, the potentiometer is adjusted until bit 12 (the LSB) indicates a true (logic "0") condition approximately half the time.

GAIN—Connect the gain adjust potentiometer as shown in Figure 5. Set the input voltage to the nominal plus full-scale value minus 3/2LSB. Once again referring to Table I, this value is +10V −7.32mV or +9.99268V for the −10V to +10V range. Adjust the gain potentiometer until the output code is alternating between 000_H and 001_H with an approximate 50% duty cycle. As in the case of offset adjustment, this procedure sets the converter end-point transitions to a precisely known value.

CLOCK OPTIONS AND SHORT CYCLE FEATURE

The ADC80 is extremely versatile in that it can be operated in several different modes with either internal or external clock. Most of these options can be implemented with inexpensive TTL logic as shown in Figures 6 through 9. Pin 20 (clock inhibit) must be grounded for use with an external clock, which is applied to pin 19.

A short-cycle input (pin 21) permits the conversion to be terminated after any number of desired bits has been converted, allowing shorter conversion times in applications not requiring full 12-bit resolution. In these situations, the short-cycle pin should be connected to the bit output pin of the next bit after the desired resolution. For example, when 10-bit resolution is desired, pin 21 is connected to pin 28 (bit 11). In this example, the conversion cycle terminates and status is reset after the bit 10 decision. Short-cycle pin connections and associated maximum 12-, 10-, and 8-bit conversion times (with internal clock) are shown in Table III. Shorter conversion times are possible with an external clock applied to pin 19. With increasing clock speed, linearity performance will begin to degrade as indicated in the Typical Performance Curves. These curves should be used only as guidelines because guaranteed performance is specified and tested only with the internal clock.

TABLE III. Short-Cycle Connections and Conversion Times for 8-, 10-, and 12-Bit Resolutions—ADC80MAH-12.

Resolution (Bits)	12	10	8
Connect pin 21 to	Pin 9 or NC	Pin 28	Pin 30
Maximum Conversion Time[1] Internal Clock (μs)	25	22	18
Maximum Linearity Error at +25°C (% of FSR)	0 012	0 048	0 20

NOTE (1) Conversion time to maintain ±1/2LSB linearity error

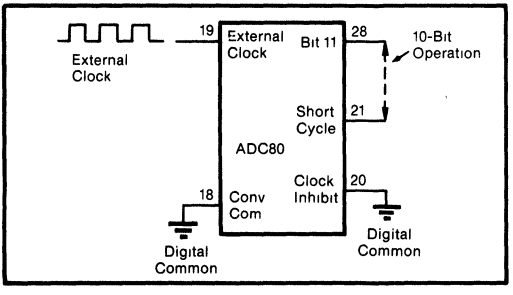


FIGURE 6. Continuous Conversion with External Clock. (Conversion is initiated by 14th clock pulse. Clock runs continuously.)

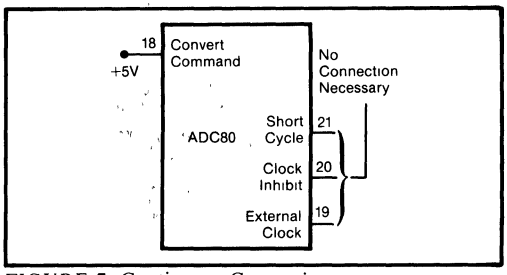


FIGURE 7. Continuous Conversion.

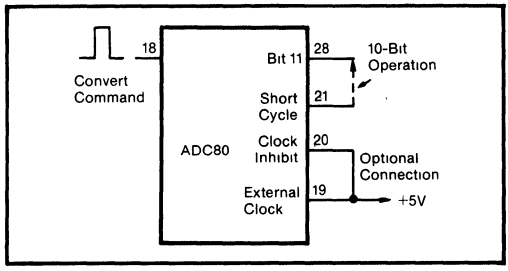


FIGURE 8. Internal Clock—Normal Operating Mode. (Conversion initiated by the rising edge of the convert command. The internal clock runs only during conversion.)

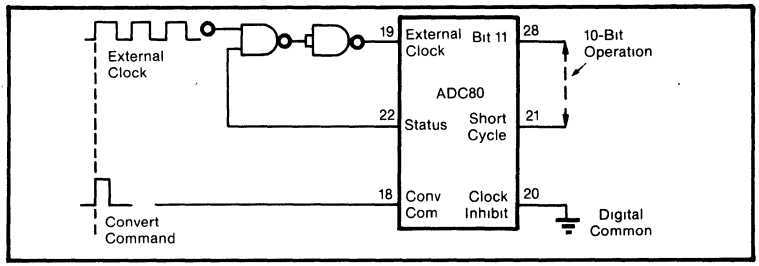


FIGURE 9. Continuous External Clock. (Conversion intitiated by rising edge of convert command. The convert command must be synchronized with clock.)

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown Q models are environmentally screened versions of our standard industrial products, designed to provide enhanced reliability. The screening illustrated in Table IV is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient way of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

BURN-IN SCREENING

Burn-in screening is an option available for the ADC80MAH. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

TABLE IV. Screening Flow for ADC80MAH-12/QM.

Screen	MIL-STD-883 Method, Condition	Screening Level
Internal Visual	2010	
High Temperature Storage (Stabilization Bake)	1008, C	24 hour, +150°C
Temperature Cycling	1010, C	10 cycles, −65°C to +150°C
Constant Acceleration	2001, A	5000 G
Electrical Test	Burr-Brown test procedure	
Burn-in	1015, B	160 hour, +125°C, steady state
Hermeticity Fine Leak Gross Leak	 1014, A1 or A2 1014, C	 5×10^{-7} atm cc/s bubble test only, pre-conditioning omitted
Final Electrical	Burr-Brown test procedure	
Final Drift	Burr-Brown test procedure	
External Visual	2009	

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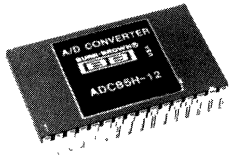


ADC84
ADC85H
ADC87H

IC ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- INDUSTRY STANDARD 12-BIT A/D CONVERTERS
- COMPLETE WITH CLOCK AND INPUT BUFFER
- HIGH SPEED CONVERSION: 10μs (max)
- REDUCED CHIP COUNT—HIGH RELIABILITY
- LOWER POWER DISSIPATION: 450mW (typ)
- ±0.012% MAX LINEARITY
- THREE TEMPERATURE RANGES:
  0°C to +70°C
  −25°C to +85°C
  −55°C to +125°C
- NO MISSING CODES OVER FULL TEMPERATURE RANGE
- PARALLEL AND SERIAL OUTPUTS
- ±12V or ±15V POWER SUPPLY OPERATION
- HERMETIC 32-PIN CERAMIC SIDE-BRAZED DIP

DESCRIPTION

The ADC85H Series of analog-to-digital converters utilize state-of-the-art IC and laser-trimmed thin-film components, and are packaged in a 32-pin hermetic side-brazed package.

Complete with internal reference and input buffer amplifier, they offer versatility and performance formerly offered only in larger modular or rack-mount packages.

Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V or 0 to +10V. Gain and offset errors may be externally trimmed to zero, offering initial accuracies of better than ±0.012% (±1/2LSB).

The fast 10μs conversion speed for 12-bit resolution makes these ADCs excellent for a wide range of applications where system throughput sampling rates of 100kHz are required. In addition, they may be short cycled and the clock rate control may be used to obtain faster conversion speeds at lower resolutions.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are CMOS/TTL-compatible. Power supply voltages are ±12VDC or ±15VDC and +5VDC.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-714A

SPECIFICATIONS

ELECTRICAL

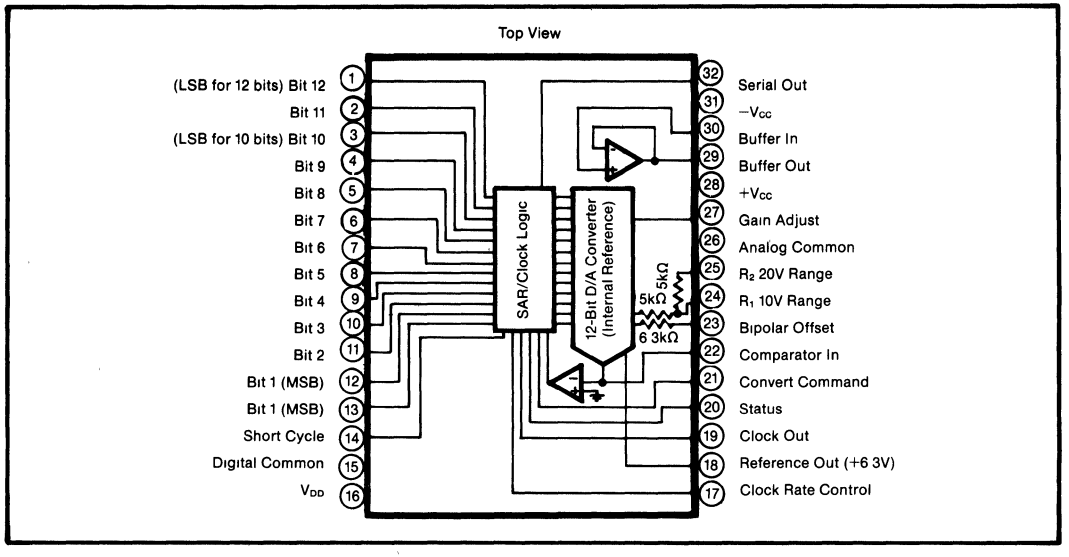
Specified at +25°C and rated supplies unless otherwise noted

MODEL	ADC84KG-12[1]			ADC85H-12			ADC87H-12			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			*			*	Bits
INPUTS										
ANALOG										
Voltage Ranges Bipolar		±2.5, ±5, ±10			*			*		V
Unipolar		0 to +5, 0 to +10			*			*		V
Impedance (Direct Input) 0 to +5V, ±2 5V	2 45	2 5	2 55	*	*	*	*	*	*	kΩ
0 to +10V, ±5V	4 9	5	5 1	*	*	*	*	*	*	kΩ
±10V	9 8	10	10 2	*	*	*	*	*	*	kΩ
Buffer Amplifier Impedance	100			*			*			MΩ
Bias Current		50			*			*		nA
Settling Time to 0 01% for 20V step[2]		2			*			*		µs
DIGITAL[3]										
Convert Command		Positive pulse 50ns (min), trailing edge initiates conversion								
Logic Loading		1			*			*		TTL Load
TRANSFER CHARACTERISTICS										
ACCURACY										
Gain Error[4]		±0 1	±0 25		*	*		*	*	%
Offset Error[4] Unipolar		±0 05	±0 2		*	*		*	*	% of FSR[5]
Bipolar		±0 1	±0 25		*	*		*	*	% of FSR
Linearity Error[6]			±0 012			*			*	% of FSR
Inherent Quantization Error		±0 5			*			*		LSB
Differential Linearity Error		±0 5			*			*		LSB
No Missing Codes Temperature Range	0		+70	−25		+85	−55		+125	°C
POWER SUPPLY SENSITIVITY										
Gain and Offset ±15V		±0 004			*			*		% of FSR/%V_S
+5V		±0 001			*			*		% of FSR/%V_S
DRIFT										
Gain			±30			±15			±15	ppm/°C
Offset Unipolar		±3			±3				±5	ppm of FSR/°C
Bipolar			±15			±7			±10	ppm of FSR/°C
Linearity			±3			±2			±2	ppm of FSR/°C
Monotonicity		Guaranteed			*			*		
CONVERSION TIME			10			*			*	µs
DIGITAL OUTPUT[3]										
(All Codes Complementary)										
Parallel Output Codes Unipolar		CSB			*			*		
Bipolar		COB, CTC			*			*		
Output Drive		2			*			*		TTL Loads
Serial Data Codes (NRZ)		CSB, COB			*			*		
Output Drive		2			*			*		TTL Loads
Status		Logic "1" during conversion			*			*		
Output Drive		2			*			*		TTL Loads
Internal Clock Output Drive		2			*			*		TTL Loads
Frequency[7]		1 35			*			*		MHz
INTERNAL REFERENCE VOLTAGE										
Reference Output	+6 2	+6 3	+6 4	*	*	*	*	*	*	V
Max External Current With No Degradation			200			*			*	µA
Tempco of Drift			±20		±5	±10		±5	±10	ppm/°C
POWER SUPPLY REQUIREMENTS										
Rated Supply Voltages		+5, ±12 or ±15			*			*		V
Supply Ranges V_{DD}	+4 75		+5 25	*		*	*		*	V
$\pm V_{CC}$	±11 4		±16 5	*		*	*		*	V
Supply Drain $+I_{CC}$			20			*			*	mA
$-I_{CC}$			25			*			*	mA
I_{DD}			10			*			*	mA
Total Power Dissipation		450	725		*	*		*	*	mW
TEMPERATURE RANGE										
Specification	0		+70	−25		+85	−55		+125	°C
Operating (with Derated Specs)	−25		+85	−55		+125				°C
Storage	−65		+150	*		*	*		*	°C
PACKAGE	Hermetic Ceramic				*			*		

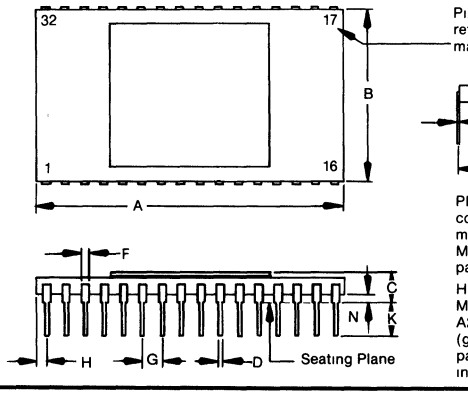
*Specification is the same as ADC84KG-12

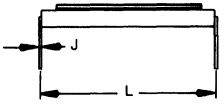
NOTES: (1) Model ADC84KG-10 is the same as model ADC84KG-12 except for the following: (a) Resolution: 10 bits (max), (b) Linearity Error: ±0.048% of FSR (max), (c) Conversion Time: 6μs (max), (d) Internal Clock Frequency: 1.9MHz (typ). (2) If the buffer is used, delay Convert Command until amplifier settles. (3) DTL/TTL compatible. For digital inputs Logic "0" = 0.8V (max) and Logic "1" = 2.0V min. For digital outputs Logic "0" = 0.4V (max) and Logic "1" = 2.4V (min). (4) Adjustable to zero. (5) FSR means Full Scale Range. (6) The error shown is the same as ±1/2LSB max linearity error in % of FSR. (7) Internal clock is externally adjustable.

CONNECTION DIAGRAM—ADC85H SERIES



MECHANICAL





Pin numbers shown for reference only Pin numbers may not be marked on package

PIN Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3 2)

HERMETICITY Conforms to Method 1014, Condition A1 or A2 (fine leak) and Condition C (gross leak) Metal lid of package is connected to $-V_{CC}$ internally

NOTE Leads in true position within .010" (0 25mm) R at MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 580	1 620	40 13	41 15
B	880	900	22 35	22 86
C	138	186	3 51	4 72
D	016	020	0 41	0 51
F	040 TYP		1 02 TYP	
G	100 BASIC		2 54 BASIC	
H	044	056	1 12	1 42
J	009	012	0 23	0 30
K	165	185	4 19	4 70
L	900	920	22 86	23 37
N	040	060	1 02	1 52

ORDERING INFORMATION

Model	Resolution (Bits)	Temperature Range
ADC84KG-10	10	0°C to +70°C
ADC84KG-12	12	0°C to +70°C
ADC85H-12	12	−25°C to +85°C
ADC85HQ-12*	12	−25°C to +85°C
ADC87H-12	12	−55°C to +125°C
ADC87HQ-12*	12	−55°C to +125°C

* Environmental screening See Table II

ORDERING INFORMATION

BURN-IN SCREENING OPTION

See text

Model	Burn-In Temp. (160h)(1)
ADC84KG-12-BI	+125°C
ADC85H-12-BI	+125°C
ADC87H-12-BI	+125°C

NOTE (1) Or equivalent combination See text

THEORY OF OPERATION

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits OFF) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB ±1/2LSB.

The ADC84, ADC85H and ADC87H are also monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that these converters will have no missing codes over a specified temperature range. Figure 2 is the timing diagram.

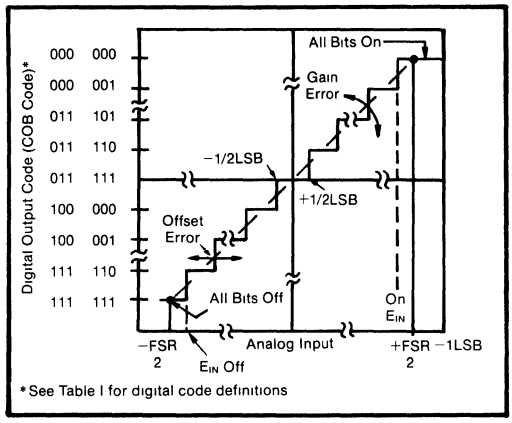


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

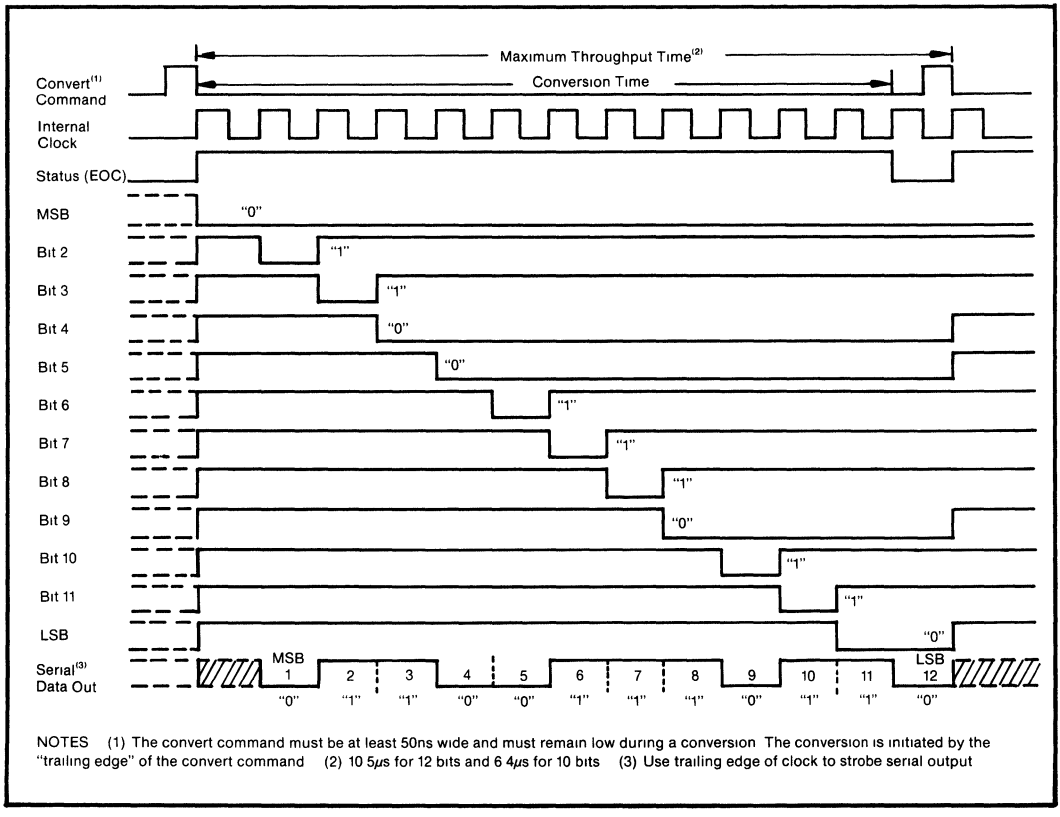


FIGURE 2. Timing Diagram.

DIGITAL CODES

Parallel Data

Three binary codes are available on the ADC85H series parallel output:

- complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges;
- complementary two's complement (CTC) for bipolar input signal ranges;
- complementary offset binary (COB) for bipolar input signal ranges.

Table I describes the LSB, transition values and code definitions for each possible analog input signal range for 8-, 10-, and 12-bit resolutions.

Serial Data

Two straight binary (complementary) codes are available on the serial output line; they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary Output	Input Voltage Range and LSB Values					
Analog Input Voltage Ranges	Defined As	±10V	±5V	±2 5V	0 to +10V	0 to +5V
Code Designation		COB[1] or CTC[2]	COB[1] or CTC[2]	COB[1] or CTC[2]	CSB[3]	CSB[3]
One Least Significant Bit (LSB)	FSR/2^n	20V/2^n	10V/2^n	5V/2^n	10V/2^n	5V/2^n
	n = 8	78 13mV	39 06mV	19 53mV	39 06mV	19 53mV
	n = 10	19 53mV	9 77mV	4 88mV	9 77mV	4 88mV
	n = 12	4 88mV	2 44mV	1 22mV	2 44mV	1 22mV
Transition Values MSB LSB						
000 000[4]	+Full Scale	+10V − 3/2LSB	+5V − 3/2LSB	+2 5V − 3/2LSB	+10V − 3/2LSB	+5V − 3/2LSB
011 111	Mid Scale	0	0	0	+5V	+2 5V
111 110	−Full Scale	−10V + 1/2LSB	−5V + 1/2LSB	−2 5V + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

NOTES (1) COB = Complementary Offset Binary (2) CTC = Complementary Two's Complement—obtained by using the complement of the most-significant bit (MSB) MSB is available on pin 13 (3) Complementary Straight Binary (4) Voltages given are the nominal value for transition to the code specified

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes. Burr-Brown Q models are environmentally screened versions of our standard industrial products, designed to provide enhanced reliability. The screening illustrated in Table II is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient way of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

TABLE II. Screening for ADC85HQ-12 and ADC87HQ-12.

Screen	MIL-STD-883 Method, Condition	Screening Level
Internal Visual	Burr-Brown QC4118*	
High Temperature Storage (Stabilization Bake)	1008, C	24 hour, +150°C
Temperature Cycling	1010, C	10 cycles, −65°C to +150°C
Constant Acceleration	2001, A	5000 G
Burn-in	1015, B	160 hour, +125°C steady-state
Electrical Test	Burr-Brown test procedure	
Hermeticity Fine Leak Gross Leak	1014, A1 or A2 1014, C	5×10^{-7} atm cc/s bubble test only, preconditioning omitted
Final Electrical	Burr-Brown test procedure	
Final Drift	Burr-Brown test procedure	
External Visual	QC5150*	

* Available upon request

DISCUSSION OF SPECIFICATIONS

The ADC85H series is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. These ADCs are factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 6 and 7.

ACCURACY DRIFT VS TEMPERATURE

Three major drift parameters degrade A/D converter accuracy over temperature: gain, offset and linearity drift. The worst-case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum-squared (RSS) or Iσ errors as follows:

$$RSS = \sqrt{\epsilon g^2 + \epsilon o^2 + \epsilon e^2}$$

where ϵg = gain drift error (ppm /°C)
ϵo = offset drift error (ppm of FSR/°C)
ϵe = linearity error (ppm of FSR/°C)

For the ADC85H-12 operating in the unipolar mode, the total RSS drift is ±15.42ppm/°C and for bipolar operation the total RSS drift is ±16.7ppm/°C.

ACCURACY VS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. The power supply sensitivity specification is a measure of how much the plus full-scale value will change from the initial value for independent changes in each power supply. This change results in a proportional change in all code transition values (i.e., a gain error).

The conversion speeds are specified for a maximum linearity error of ±1/2LSB with the internal clock. Faster conversion speeds are possible but at a sacrifice in linearity (see Clock Rate Control Alternate Connections).

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. Normally, regulated power supplies with 1% or less ripple are recommended for use with these ADCs. See Layout Precautions and Power Supply Decoupling.

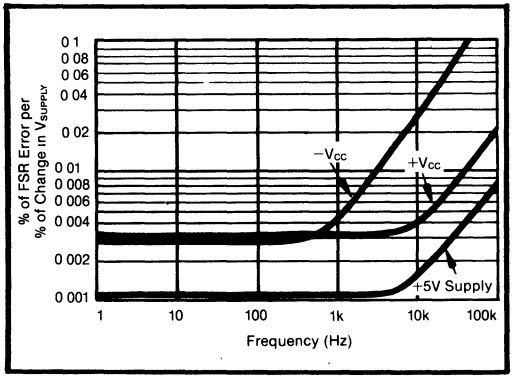


FIGURE 3. Power Supply Rejection vs Power Supply Ripple Frequency.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected internally in the ADC85H series, but should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC. If these grounds must be run separately, use a wide conductor pattern and a **0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance** analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 4 to reduce noise during operation. These capacitors should be located close to the ADC. 1μF electrolytic type capacitors should by bypassed with 0.01μF ceramic capacitors for improved high frequency performance.

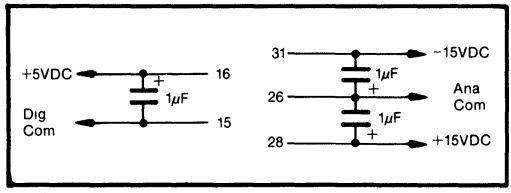


FIGURE 4. Recommended Power Supply Decoupling.

ANALOG SIGNAL SOURCE IMPEDANCE

The output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier or a sample/hold. For instance, a 741 operational amplifier will not be fast enough to accurately drive this ADC. Recommended amplifiers include the Burr-Brown models OPA602 and OPA111.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table III. See Figure 5 for circuit details.

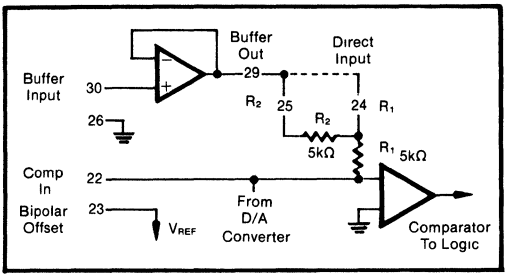


FIGURE 5. Input Scaling Circuit.

TABLE III. Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 23 To Pin	Connect Pin 25 To	For Buffered Input[1] Connect Pin 29 To Pin	For Direct Input[2] Connect Input Signal To Pin
±10V	COB or CTC	22	Input Signal[3]	25	25
±5V	COB or CTC	22	Open	24	24
±2.5V	COB or CTC	22	Pin 22	24	24
0 to +5V	CSB	26	Pin 22	24	24
0 to +10V	CSB	26	Open	24	24

NOTES: (1) Connect to pin 29 or input signal as shown in next two columns. (2) **If the buffer amplifier is not used, pin 30 must be connected to ground (pin 26).** (3) The input signal is connected to pin 30 if the buffer amplifier is used.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 6 and 7. Multiturn potentiometers with 100ppm/°C or better TCRs are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 27 (Gain Adjust) should be bypassed with 0.01μF to reduce noise pickup and Pin 22 (Offset Adjust) may be left open if no external adjustment is required.

Adjustment Procedure

OFFSET—Connect the Offset potentiometer as shown in Figure 6. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

GAIN—Connect the Gain adjust potentiometers as shown in Figure 7. Sweep the input through the end point transition voltage that should cause an output transition voltage to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

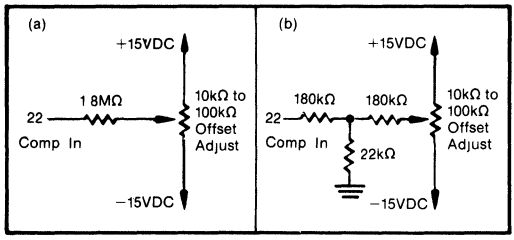


FIGURE 6. Two Methods of Connecting Optional Offset Adjust.

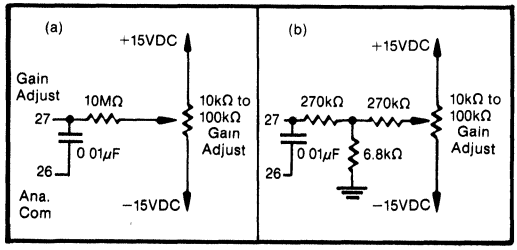


FIGURE 7. Two Methods of Connecting Optional Gain Adjust.

Clock Rate Control Alternate Connections

If adjustment of the Clock Rate is desired for faster conversion speeds, the Clock Rate Control may be connected to an external multiturn trim potentiometer with TCR of ±100ppm/°C or less as shown in Figure 8. If the potentiometer is connected to −15VDC, conversion time can be increased as shown in Figure 8. If these adjustments are used, delete the connections shown in Table IV for pin 17. See Typical Performance Curves for nonlinearity error vs. clock frequency, and Figure 9 for the effect of the control voltage on clock speed. Operation with clock rate control voltage of less than −1VDC is not recommended.

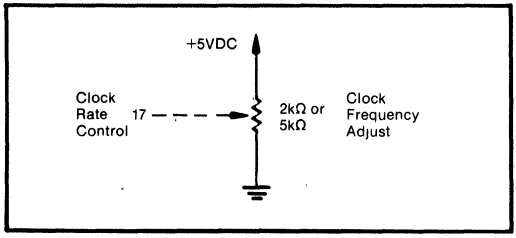


FIGURE 8. 12-Bit Clock Rate Control Optional Fine Adjust.

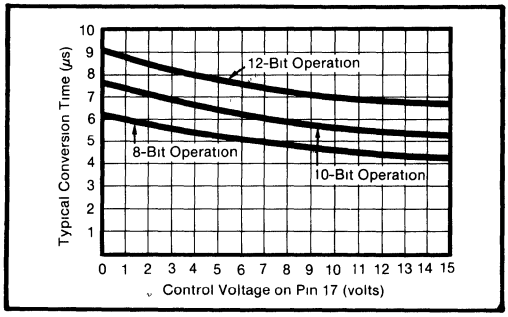


FIGURE 9. Conversion Time vs Clock Speed Control.

Additional Connections Required

The ADC85H series may be operated at faster speeds for resolutions less than 12 bits by connecting the Short Cycle input, pin 14, as shown in Table IV. Conversion speeds, linearity and resolution are shown for reference. Specifications for 10-bit units assume connections as shown below.

Converter Initialization

On power-up, the state of the ADC internal circuitry is indeterminate. One conversion cycle is required to initialize the converter after power is applied.

TABLE IV. Short Cycle Connections and Specifications for 8- to 12-Bit Resolution.

Resolution (Bits)	12	10	8
Connect Pin 17 to [1]	Pin 15	Pin 28	Pin 28
Connect Pin 14 to	Pin 16	Pin 2	Pin 4
Maximum Conversion Speed (μs)[2]	10	6	4 5
Maximum Nonlinearity at 25°C (% of FSR)	0 012[3]	0 048[4]	0 20[4]

NOTES (1) Connect only if clock rate control is not used (2) Maximum conversion speeds to maintain ±1/2LSB nonlinearity error (3) 12-bit models only. (4) 10- or 12-bit models

Output Drive

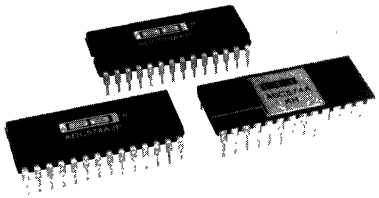
Normally all ADC84, ADC85H, and ADC87H logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information detail. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

BURR-BROWN®



ADC574A

Microprocessor-Compatible ANALOG-TO-DIGITAL CONVERTER

FEATURES

- COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, OR 16-BIT MICROPROCESSOR BUS INTERFACE
- IMPROVED PERFORMANCE SECOND SOURCE FOR 574A-TYPE A/D CONVERTERS
  - Conversion Time: 25μs max
  - Bus Access Time: 150ns max
  - A_0 Input: Bus Contention During Read Operation Eliminated
- DUAL IN-LINE PLASTIC AND HERMETIC CERAMIC
- FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES
- NO MISSING CODES OVER TEMPERATURE:
  - 0°C to +75°C: ADC574AJH, KH, JP, KP Grades
  - −55°C to +125°C: ADC574ASH, TH Grades

DESCRIPTION

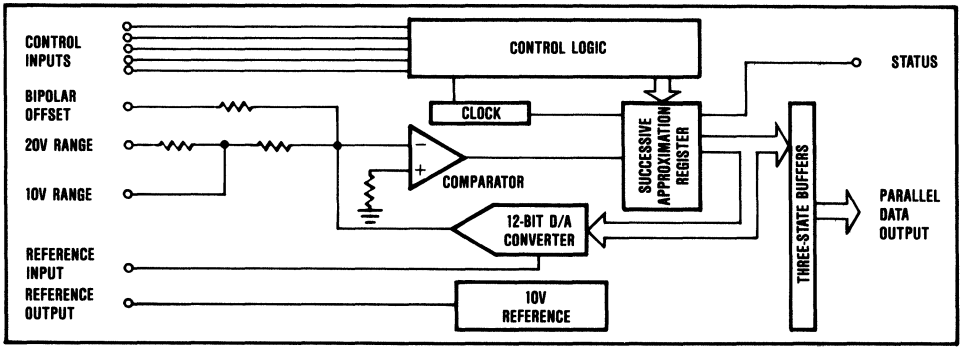
The ADC574A is a 12-bit successive approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 25μs maximum.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC574A, available in both industrial and military temperature ranges, requires supply voltages of +5V and ±12V or ±15V. It is packaged in a 28-pin plastic DIP, or hermetic side-brazed ceramic DIP.



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PDS-550C

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified

MODEL	ADC574AJP, ADC574AJH, ADC574ASH			ADC574AKP, ADC574AKH, ADC574ATH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			*	Bits
INPUTS							
ANALOG							
Voltage Ranges: Unipolar		0 to +10, 0 to +20			*		V
Bipolar		±5, ±10			*		V
Impedance 0 to +10V, ±5V	4 7	5	5.3	*	*	*	kΩ
±10V, 0V to +20V	9 4	10	10 6	*	*	*	kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/8)							
Over Temperature Range							
Voltages Logic 1	+2 0		+5 5	*		*	V
Logic 0	−0 5		+0.8	*		*	V
Current	−5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (adjustable to zero)			±2			*	LSB
Bipolar Offset Error (adjustable to zero)			±10			±4	LSB
Full-Scale Calibration Error[1]							
(adjustable to zero)			±0 25			*	% of FS[2]
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
Inherent Quantization Error		±1/2			*		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	LSB
S, T Grades			±1			±1/2	LSB
Full-Scale Calibration Error							
Without Initial Adjustment[1]. J, K Grades			±0 47			±0 37	% of FS
S, T Grades			±0 75			±0.5	% of FS
Adjusted to zero at +25°C: J, K Grades			±0 22			±0.12	% of FS
S, T Grades			±0 5			±0.25	% of FS
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
TEMPERATURE COEFFICIENTS (T_{MIN} to T_{MAX})[3]							
Unipolar Offset. J, K Grades			±10			±5	ppm/°C
S, T Grades			±5			±2.5	ppm/°C
Max Change All Grades			±2			±1	LSB
Bipolar Offset All Grades			±10			±5	ppm/°C
Max Change: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration J, K Grades			±45			±25	ppm/°C
S, T Grades			±50			±25	ppm/°C
Max Change: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration							
+13.5V < V_{CC} < +16.5V or +11 4V < V_{CC} < +12 6V			±2			±1	LSB
−16 5V < V_{EE} < −13 5V or −12.6V < V_{EE} < −11.4V			±2			±1	LSB
+4.5V < V_{LOGIC} < +5.5V			±1/2			*	LSB
CONVERSION TIME[4]							
8-Bit Cycle	10	13	17	*	*	*	µs
12-Bit Cycle	15	20	25	*	*	*	µs
OUTPUTS							
DIGITAL (DB_{11} — DB_0, STATUS)							
(Over Temperature Range)							
Output Codes. Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels. Logic 0 (I_{SINK} = 1.6mA)			+0 4			*	V
Logic 1 (I_{SOURCE} = 500µA)	+2.4			*			V
Leakage, Data Bits Only, High-Z State	−5	0 1	+5	*	*	*	µA
Capacitance		5			*		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+9.9	+10.0	+10 1	*	*	*	V
Source Current Available for External Loads[5]	2.0			*			mA

ELECTRICAL (CONT)

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified

MODEL	ADC574AJP, ADC574AJH, ADC574ASH			ADC574AKP, ADC574AKH, ADC574ATH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Voltage. V_{CC}	+11.4		+16.5	*		*	V
V_{EE}	−11 4		−16.5	*		*	V
V_{LOGIC}	+4 5		+5.5	*		*	V
Current I_{CC}		3.5	5		*	*	mA
I_{EE}		15	20		*	*	mA
I_{LOGIC}		9	15		*	*	mA
Power Dissipation (±15V Supplies)		325	450		*	*	mW
TEMPERATURE RANGE (Ambient T_{MIN}, T_{MAX})							
Specification. J, K Grades	0		+75	*		*	°C
S, T Grades	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C

*Same specification as ADC574AJP, AJH, ASH

NOTES (1) With fixed 50Ω resistor from REF OUT to REF IN This parameter is also adjustable to zero at +25°C (see Optional External Full Scale and Offset Adjustments section) (2) FS in this specification table means Full Scale Range That is, for a ±10V input range, FS means 20V, for a 0 to +10V range, FS means 10V The term Full Scale for these specifications instead of Full-Scale Range is used to be consistent with other vendors' 574 and 574A type specification tables (3) Using internal reference (4) See Controlling the ADC574A section for detailed information concerning digital timing (5) External loading must be constant during conversion The reference output requires no buffer amplifier with either ±12V or ±15V power supplies

ORDERING INFORMATION

Model	Package (DIP)	Temperature Range	Linearity Error, max (T_{MIN} to T_{MAX})
ADC574AJP	Plastic	0°C to +75°C	±1LSB
ADC574AKP	Plastic	0°C to +75°C	±1/2LSB
ADC574AJH	Ceramic	0°C to +75°C	±1LSB
ADC574AKH	Ceramic	0°C to +75°C	±1/2LSB
ADC574ASH	Ceramic	−55°C to +125°C	±1LSB
ADC574ATH	Ceramic	−55°C to +125°C	±1/2LSB
BURN-IN SCREENING OPTION See text for details			
Model	**Package (DIP)**	**Temperature Range**	**Burn-In Temp. (160 Hours)(1)**
ADC574AJP-BI	Plastic	0°C to +75°C	+85°C
ADC574AKP-BI	Plastic	0°C to +75°C	+85°C
ADC574AJH-BI	Ceramic	0°C to +75°C	+125°C
ADC574AKH-BI	Ceramic	0°C to +75°C	+125°C
ADC574ASH-BI	Ceramic	−55°C to +125°C	+125°C
ADC574ATH-BI	Ceramic	−55°C to +125°C	+125°C

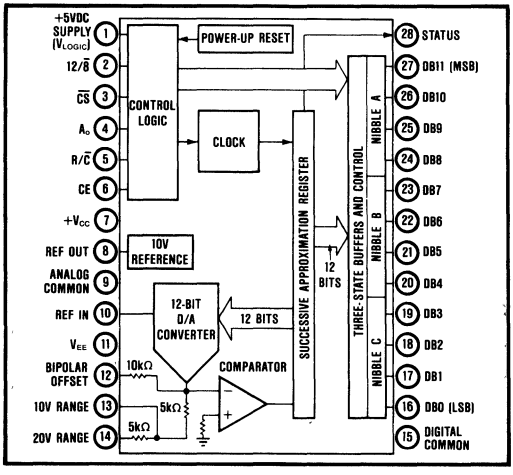
NOTE (1) Or equivalent combination of time and temperature

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to −16 5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$)
to Digital Common ..... −0.5V to V_{LOGIC} +0 5V
Analog Inputs (REF IN, BIP OFF., $10V_{IN}$)
to Analog Common..... ±16 5V
$20V_{IN}$ to Analog Common ..... ±24V
REF OUT ..... Indefinite Short to Common, Momentary Short to V_{CC}
Max Junction Temperature..... +165°C
Power Dissipation..... 1000mW
Lead Temperature (soldering, 10s)..... +300°C
Thermal Resistance, θ_{JA}. Ceramic..... 50°C/W
Plastic ..... 100°C/W

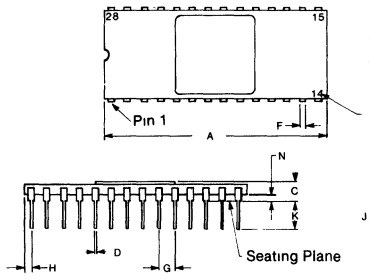
CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

CONNECTION DIAGRAM



H Package [Ceramic]

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 386	1 414	35 20	35 92
C	108	166	2 74	4 22
D	015	021	0 38	0 53
F	035	060	0 89	1 52
G	100 BASIC		2 54 BASIC	
H	036	064	0 91	1 63
J	008	012	0 20	0 30
K	120	240	3 05	6 10
L	600 BASIC		15 24 BASIC	
M	—	10°	—	10°
N	025	060	0 64	1 52



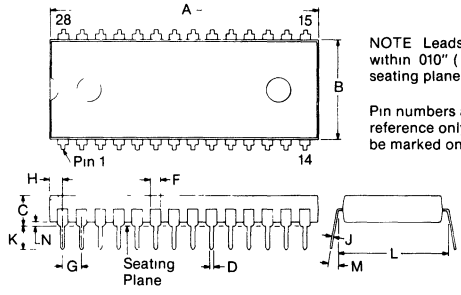
NOTE Leads in true position within 0 01" (0 25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers may not be marked on package

CASE Ceramic, hermetic
WEIGHT 4 8 grams (0 17 oz)

P Package [Plastic]

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 350	1 450	34 29	36 83
B	520	575	13 21	14 61
C	169	224	4 29	5 70
D	015	023	0 38	0 58
F	043	062	1 09	1 57
G	100 BASIC		2 54 BASIC	
H	030	090	0 76	2 29
J	008	015	0 20	0 38
K	100	150	2 54	3 81
L	600 BASIC		15 24 BASIC	
M	0°	15°	0°	15°
N	018	040	0 46	1 02



NOTE Leads in true position within 010" (25mm) R at MMC at seating plane

Pin numbers are shown for reference only Numbers may not be marked on package

CASE Plastic
WEIGHT 4.3 grams (0 15oz)

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale. The zero value is located at an analog input value 1/2LSB before the first code transition (000_H to 001_H). The full-scale value is located at an analog value 3/2LSB beyond the last code transition (FFE_H to FFF_H) (see Figure 1).

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V), the zero value of −10V is 2.44mV below the first code transition (000_H to 001_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (FFE_H to FFF_H at +9.99268) (see Table I).

NO MISSING CODES (DIFFERENTIAL LINEARITY ERROR)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically-increasing sequence as the analog input is increased throughout the range. Thus, every input code width (quantum) must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur.

ADC574AKP, KH, and TH grades are guaranteed to have no missing codes to 12-bit resolution over their respective specification temperature ranges.

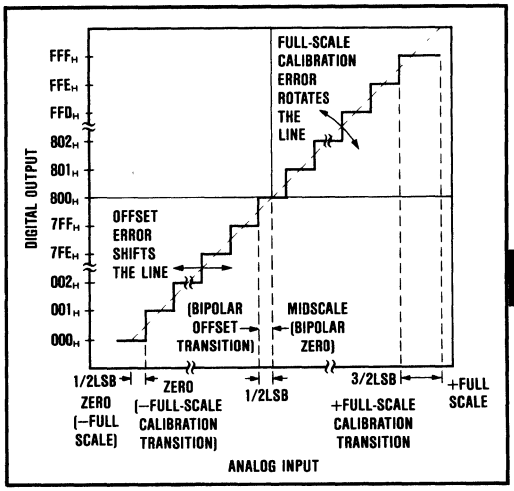


FIGURE 1. ADC574A Transfer Characteristic Terminology.

UNIPOLAR OFFSET ERROR

An ADC574A connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value. The unipolar offset temperature coefficient specifies the change of this transition value versus a change in ambient temperature.

TABLE I. Input Voltages, Transition Values, and LSB Values.

Binary (BIN) Output	Input Voltage Range and LSB Values				
Analog Input Voltage Range	Defined As	±10V	+5V	0 to +10V	0 to +20V
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{10V}{2^n}$	$\frac{20V}{2^n}$
	n = 8	78.13mV	39.06mV	39 06mV	78 13mV
	n = 12	4 88mV	2 44mV	2 44mV	4 88mV
Output Transition Values					
FFE_H to FFF_H	+ Full-Scale Calibration	+10V − 3/2LSB	+5V − 3/2LSB	+10V − 3/2LSB	+10V − 3/2LSB
$7FF_H$ to 800_H	Midscale Calibration (Bipolar Offset)	0 − 1/2LSB	0 − 1/2LSB	+5V − 1/2LSB	±10V − 1/2LSB
000_H to 001_H	Zero Calibration (− Full-Scale Calibration)	−10V + 1/2LSB	−5V + 1/2LSB	0 to + 1/2LSB	0 to +1/2LSB

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The ADC574A specification, however, follows the terminology defined for the 574 converter several years ago. Thus, bipolar offset is located near the midscale value of 0V (bipolar zero) at the output code transition $7FF_H$ to 800_H.

Bipolar offset error for the ADC574A is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB below 0V. The bipolar offset temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

FULL SCALE CALIBRATION ERROR

The last output code transition (FFE_H to FFF_H) occurs for an analog input value 3/2LSB below the nominal full-scale value. The full scale calibration error is the deviation of the actual analog value at the last transition point from the ideal value. The full-scale calibration temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC574A assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the full-scale calibration value. This change, of course, results in a proportional change in all code transition values (i.e. a gain error). The specification describes the maximum change in the full-scale calibration value from the initial value for a change in each power supply voltage.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset and bipolar offset specify the maximum change from the +25°C value to the value at T_{MIN} or T_{MAX}.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

CODE WIDTH (QUANTUM)

Code width, or quantum, is defined as the range of analog input values for which a given otuput code will occur. The ideal code width is 1LSB.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADC574A, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common. Analog common (pin 9) typically carries +8mA.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 should still be connected together at the converter; a single wide conductor pattern then connects these two pins to the system common. In either case, the common return of the analog input signal should be referenced to pin 9 of the ADC. This prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC574A as possible. If no trim adjustments are used, the fixed resistors should likewise be as close as possible.

POWER SUPPLY DECOUPLING

Logic and analog power supplies should be bypassed with 10μF tantalum type capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC574A will be driving into a nominal DC input impedance of either 5kΩ or 10kΩ. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

RANGE CONNECTIONS

The ADC574A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, and ±10V. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of the two is left unconnected. Full-scale and offset adjustments are described below.

To operate the converter with a 10.24V (2.5mV LSB) or 20.48V (5mV LSB) input range, insert a 120Ω 1% metal-film resistor in series with pin 13 for the 10.24V range, or a 240Ω 1% metal-film resistor in series with pin 14 for the 20.48V range. Offset and gain adjustments are still performed as described below. However, you must recalculate full-scale adjustment voltages proportionately. A fixed metal-film resistor can be used because the input impedance of the ADC574A is trimmed to less than ±6% of the nominal value.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADC574A as shown in Figures 2 and 3 for unipolar and bipolar operation.

CALIBRATION PROCEDURE—UNIPOLAR RANGES

If adjustment of unipolar offset and full scale is not required, replace R_2 with a 50Ω, 1% metal film resistor and connect pin 12 to pin 9, omitting the adjustment network.

If adjustment is required, connect the converter as shown in Figure 2. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 20V range) that causes the output code to be DB0 ON (high). Adjust potentiometer R_1 until DB0 is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale value minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1—DB11 are ON and DB0 is toggling ON and OFF.

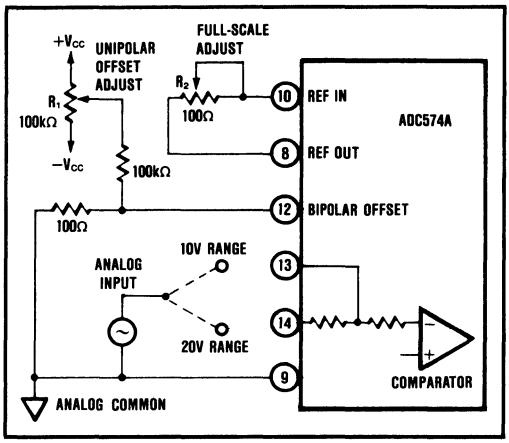


FIGURE 2. Unipolar Configuration.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, the potentiometers may be replaced by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 3. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (−4.9988V for the ±5V range, −9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

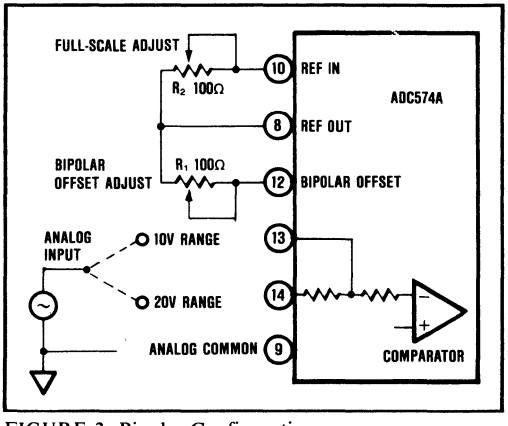


FIGURE 3. Bipolar Configuration.

CONTROLLING THE ADC574A

The Burr-Brown ADC574A can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the ouptut data when ready—choosing either 12 bits all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is listed in Table III.

TABLE III. Control Input Truth Table.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

TABLE II. ADC574A Control Line Functions.

Pin Designation	Definition	Function
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data 0-1 edge may be used to initiate a conversion
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data 1-0 edge may be used to initiate a conversion
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8 or 12-bit conversions 1-0 edge may be used to initiate a conversion Must be high ("1") to read output data 0-1 edge may be used to initiate a read operation
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode When reading output data in two 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte)
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously 12/$\overline{8}$ = "0" will enable the MSB's or LSB's as determined by the A_0 line

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to V_{LOGIC} (+5V). The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case the R/$\overline{C}$ pulse must remain low for a minimum of 50ns.

Figure 4 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 5 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the ouptut data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Table IV lists timing specifications for stand-alone operation.

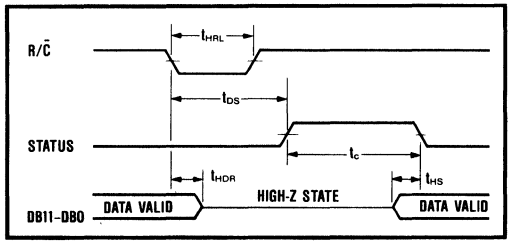


FIGURE 4. R/$\overline{C}$ Pulse Low — Outputs Enabled After Conversion.

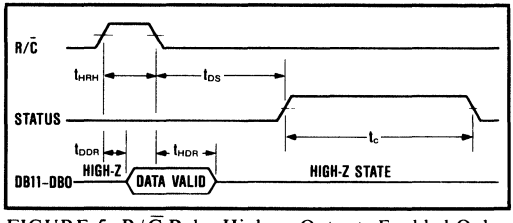


FIGURE 5. R/$\overline{C}$ Pulse High — Outputs Enabled Only While R/$\overline{C}$ Is High.

TABLE IV. Stand-Alone Mode Timing.

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	300	400	1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is low. If all 12 bits are read following an 8-bit conversion, the 3LSBs (DB0–DB2) will be low (logic 0) and DB3 will be high (logic 1). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter is commanded to initiate conversion by a transition occurring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change states simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 6. The specifications for timing are contained in Table V.

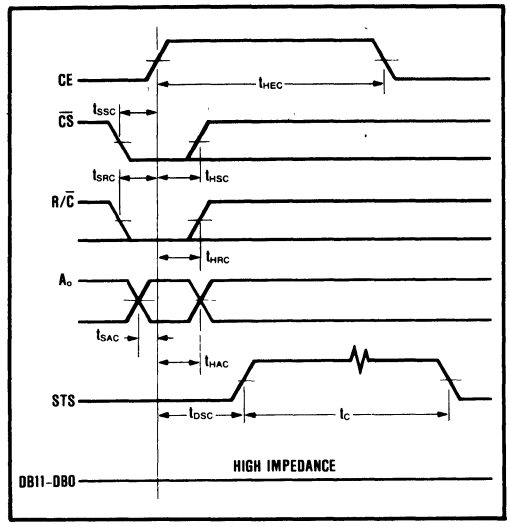


FIGURE 6. Conversion Cycle Timing.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

TABLE V. Timing Specifications.

Symbol	Parameter	Min	Typ	Max	Units
Convert Mode					
t_{DSC}	STS delay from CE		60	200	ns
t_{HEC}	CE Pulse width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE setup	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns
t_C	Conversion time, 12 bit cycle	15	20	25	μs
	8 bit cycle	10	13	17	μs
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE setup	0			ns
t_{SAR}	A_0 to CE setup	50	25		ns
t_{HSR}	$\overline{CS}$ valid after CE low	0			ns
t_{HRR}	R/$\overline{C}$ high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns
t_{HS}	STS delay after data valid	300	400	1000	ns

NOTE Specifications are at +25°C and measured at 50% level of transitions

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 7 and Table V for timing relationships and specifications.

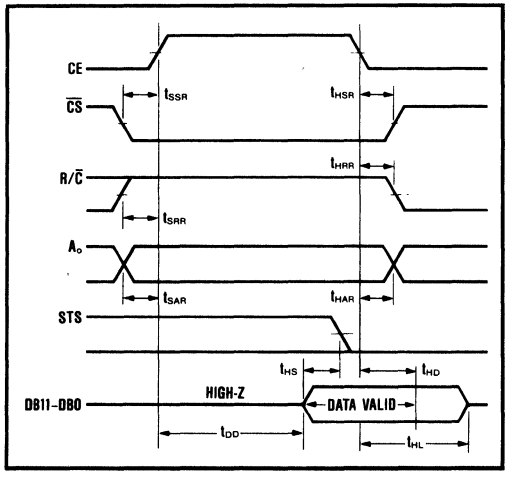


FIGURE 7. Read Cycle Timing.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is high, all 12 output lines (DB0–DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored.

When 12/$\overline{8}$ is low, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the read cycle. Connection of the ADC574A to an 8-bit bus for transfer of left-justified data is illustrated in Figure 8. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

When A_0 is low, the byte addressed contains the 8MSBs. When A_0 is high, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 8. The design of the ADC574A guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together as illustrated in Figure 9 cannot be enabled at the same time.

In the majority of applications the read operation will be attempted only after the conversion is complete and the STATUS output has gone low. In those situations requiring the earliest possible access to the data, the read may be started as much as 1.15μs (t_{DD} max + t_{HS} max) before STATUS goes low. Refer to Figure 7 for these timing relationships.

BURN-IN SCREENING

Burn-in screening is available for both plastic and ceramic package ADC574As. Burn-in duration is 160 hours at the temperature (or equivalent combination of time and temperature) indicated below:

Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are 100% electrically tested after burn-in is completed. To order burn-in, add "-BI" to the base model number (e.g., ADC574AKP-BI). See Ordering Information for pricing.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 8. 12-Bit Data Format for 8-Bit Systems.

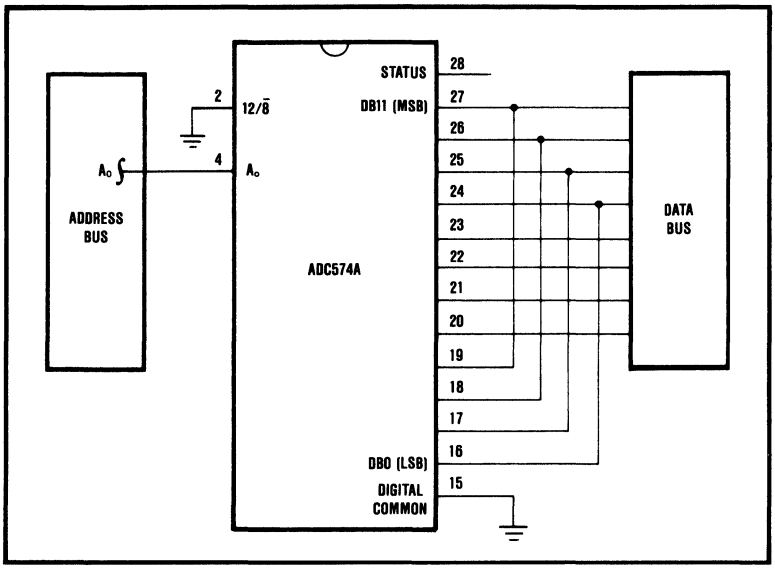


FIGURE 9. Connection to an 8-bit Bus.

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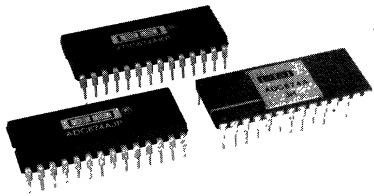


ADC674A

Microprocessor-Compatible ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, OR 16-BIT MICROPROCESSOR BUS INTERFACE**
- **IMPROVED PERFORMANCE SECOND SOURCE FOR ADC574A/674A-TYPE A/D CONVERTERS**
  - **Conversion Time: 15μs max**
  - **Bus Access Time: 150ns max**
  - **A_0 Input: Bus Contention During Read Operation Eliminated**
- **FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES**
- **NO MISSING CODES OVER TEMPERATURE:**
  - **0°C to +75°C: ADC674AJH, KH, JP, KP Grades**
  - **−55°C to +125°C: ADC674ASH, TH Grades**

DESCRIPTION

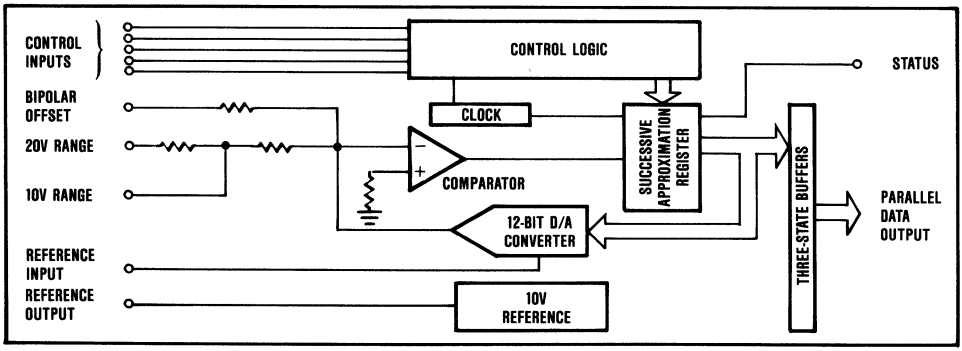
The ADC674A is a 12-bit successive approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 15μs maximum.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC674A, available in both industrial and military temperature ranges, requires supply voltages of +5V and ±12V or ±15V. It is packaged in a 28-pin plastic DIP, or hermetic side-brazed ceramic DIP.



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PDS-551C

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified.

MODEL	ADC674AJP, ADC674AJH, ADC674ASH			ADC674AKP, ADC674AKH, ADC674ATH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			*	Bits
INPUTS							
ANALOG							
Voltage Ranges Unipolar		0 to +10, 0 to +20			*		V
Bipolar		±5, ±10			*		V
Impedance. 0 to +10V, ±5V	4.7	5	5 3	*	*	*	kΩ
±10V, 0V to +20V	9 4	10	10 6	*	*	*	kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/8) Over Temperature Range							
Voltages Logic 1	+2.0		+5 5	*		*	V
Logic 0	−0 5		+0.8	*		*	V
Current	−5	0 1	+5	*	*	*	μA
Capacitance		5			*		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (adjustable to zero)			±2			*	LSB
Bipolar Offset Error (adjustable to zero)			±10			±4	LSB
Full-Scale Calibration Error[1] (adjustable to zero)			±0.25			*	% of FS[2]
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
Inherent Quantization Error		±1/2			*		LSB
T_{MIN} to T_{MAX}							
Linearity Error J, K Grades			±1			±1/2	LSB
S, T Grades			±1			±1/2	LSB
Full-Scale Calibration Error							
Without Initial Adjustment[1]: J, K Grades			±0.47			±0 37	% of FS
S, T Grades			±0.75			±0 5	% of FS
Adjusted to zero at +25°C. J, K Grades			±0 22			±0 12	% of FS
S, T Grades			±0.5			±0 25	% of FS
No Missing Codes Resolution (Diff Linearity)	11			12			Bits
TEMPERATURE COEFFICIENTS (T_{MIN} to T_{MAX})[3]							
Unipolar Offset J, K Grades			±10			±5	ppm/°C
S, T Grades			±5			±2 5	ppm/°C
Max Change All Grades			±2			±1	LSB
Bipolar Offset: All Grades			±10			±5	ppm/°C
Max Change J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration J, K Grades			±45			±25	ppm/°C
S, T Grades			±50			±25	ppm/°C
Max Change J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration							
+13 5V < V_{CC} < +16 5V or +11.4V < V_{CC} < +12 6V			±2			±1	LSB
−16.5V < V_{EE} < −13 5V or −12 6V < V_{EE} < −11 4V			±2			±1	LSB
+4.5V < V_{LOGIC} < +5 5V			±1/2			*	LSB
CONVERSION TIME[4]							
8-Bit Cycle	6	8	10	*	*	*	μs
12-Bit Cycle	9	12	15	*	*	*	μs
OUTPUTS							
DIGITAL (DB_{11} — DB_0, STATUS) (Over Temperature Range)							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{SINK} = 1 6mA)			+0.4			*	V
Logic 1 (I_{SOURCE} = 500μA)	+2.4			*			V
Leakage, Data Bits Only, High-Z State	−5	0.1	+5	*	*	*	μA
Capacitance		5			*		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+9.9	+10.0	+10.1	*	*	*	V
Source Current Available for External Loads[5]	2.0			*			mA

ELECTRICAL (CONT)

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified

MODEL	ADC674AJP, ADC674AJH, ADC674ASH			ADC674AKP, ADC674AKH, ADC674ATH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Voltage V_{CC}	+11.4		+16.5	*		*	V
V_{EE}	−11.4		−16.5	*		*	V
V_{LOGIC}	+4.5		+5.5	*		*	V
Current I_{CC}		3.5	5		*	*	mA
I_{EE}		15	20		*	*	mA
I_{LOGIC}		9	15		*	*	mA
Power Dissipation (±15V Supplies)		325	450		*	*	mW
TEMPERATURE RANGE (Ambient T_{MIN}, T_{MAX})							
Specification J, K Grades	0		+75	*		*	°C
S, T Grades	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C

*Same specification as ADC674AJP, AJH, ASH.

NOTES (1) With fixed 50Ω resistor from REF OUT to REF IN This parameter is also adjustable to zero at +25°C (see Optional External Full Scale and Offset Adjustments section) (2) FS in this specification table means Full Scale Range That is, for a ±10V input range, FS means 20V, for a 0 to +10V range, FS means 10V The term Full Scale for these specifications instead of Full-Scale Range is used to be consistent with other vendors' 674A type specification tables (3) Using internal reference (4) See Controlling the ADC674A section for detailed information concerning digital timing (5) External loading must be constant during conversion The reference output requires no buffer amplifier with either ±12V or ±15V power supplies

ORDERING INFORMATION

Model	Package (DIP)	Temperature Range	Linearity Error, max (T_{MIN} to T_{MAX})
ADC674AJP	Plastic	0°C to +75°C	±1LSB
ADC674AKP	Plastic	0°C to +75°C	±1/2LSB
ADC674AJH	Ceramic	0°C to +75°C	±1LSB
ADC674AKH	Ceramic	0°C to +75°C	±1/2LSB
ADC674ASH	Ceramic	−55°C to +125°C	±1LSB
ADC674ATH	Ceramic	−55°C to +125°C	±1LSB
BURN-IN SCREENING OPTION See text for details.			
Model	**Package (DIP)**	**Temperature Range**	**Burn-In Temp. (160 Hours)[1]**
ADC674AJP-BI	Plastic	0°C to +75°C	+85°C
ADC674AKP-BI	Plastic	0°C to +75°C	+85°C
ADC674AJH-BI	Ceramic	0°C to +75°C	+125°C
ADC674AKH-BI	Ceramic	0°C to +75°C	+125°C
ADC674ASH-BI	Ceramic	−55°C to +125°C	+125°C
ADC674ATH-BI	Ceramic	−55°C to +125°C	+125°C

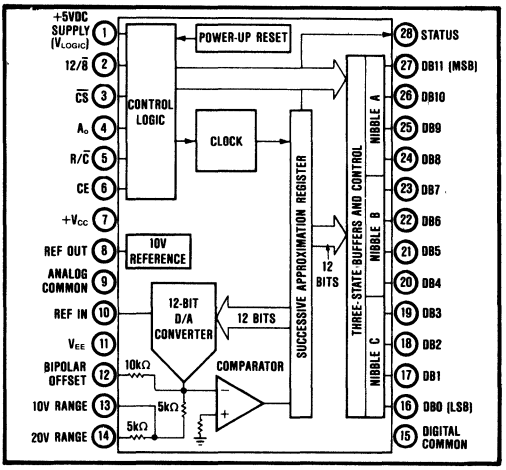
NOTE (1) Or equivalent combination of time and temperature

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to −16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common ..... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to Analog Common ..... ±16.5V
$20V_{IN}$ to Analog Common ..... ±24V
REF OUT ..... Indefinite Short to Common, Momentary Short to V_{CC}
Max Junction Temperature ..... +165°C
Power Dissipation 1000mW
Lead Temperature (soldering, 10s) ..... +300°C
Thermal Resistance, θ_{JA}: Ceramic ..... 50°C/W
Plastic ..... 100°C/W

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

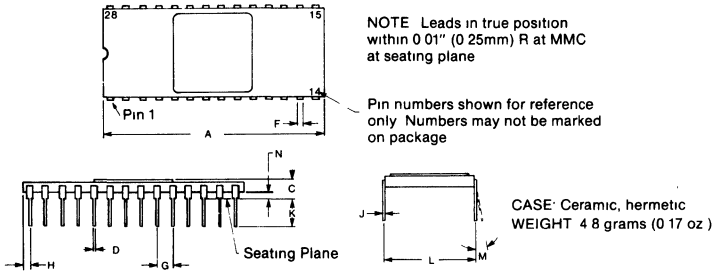
CONNECTION DIAGRAM



MECHANICAL

H Package [Ceramic]

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1 386	1 414	35 20	35 92
C	108	166	2 74	4 22
D	015	021	0 38	0 53
F	035	060	0 89	1 52
G	100 BASIC		2 54 BASIC	
H	036	064	0 91	1 63
J	008	012	0 20	0 30
K	120	240	3 05	6 10
L	600 BASIC		15 24 BASIC	
M	—	10°	—	10°
N	025	060	0 64	1 52



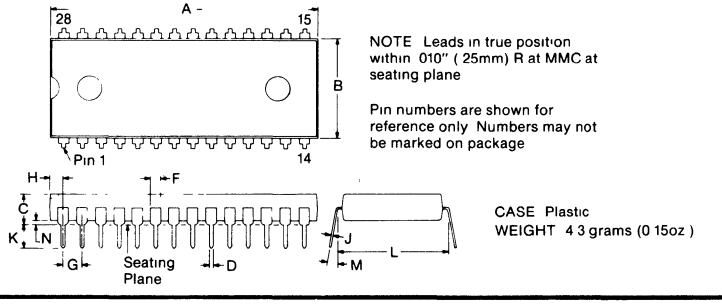
NOTE Leads in true position within 0 01" (0 25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers may not be marked on package

CASE Ceramic, hermetic
WEIGHT 4 8 grams (0 17 oz)

P Package [Plastic]

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1 350	1 450	34 29	36 83
B	520	575	13 21	14 61
C	169	224	4 29	5 70
D	015	023	0 38	0 58
F	043	062	1 09	1 57
G	100 BASIC		2 54 BASIC	
H	030	090	0 76	2 29
J	008	015	0 20	0 38
K	100	150	2 54	3 81
L	600 BASIC		15 24 BASIC	
M	0°	15°	0°	15°
N	018	040	0 46	1 02



NOTE Leads in true position within 010" (25mm) R at MMC at seating plane

Pin numbers are shown for reference only Numbers may not be marked on package

CASE Plastic
WEIGHT 4 3 grams (0 15oz)

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale. The zero value is located at an analog input value 1/2LSB before the first code transition (000_H to 001_H). The full-scale value is located at an analog value 3/2LSB beyond the last code transition (FFE_H to FFF_H) (see Figure 1).

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V), the zero value of −10V is 2.44mV below the first code transition (000_H to 001_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (FFE_H to FFF_H at +9.99268) (see Table I).

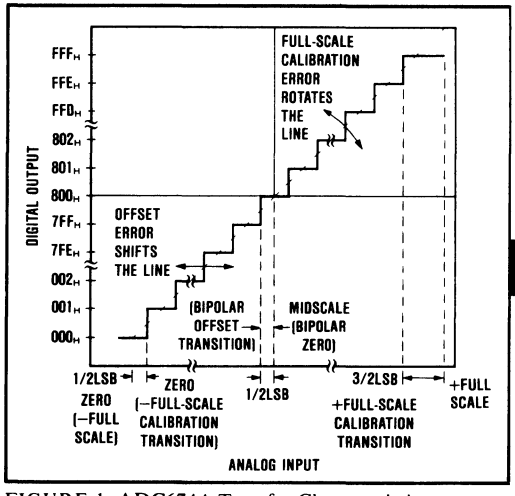


FIGURE 1. ADC674A Transfer Characteristic Terminology.

NO MISSING CODES (DIFFERENTIAL LINEARITY ERROR)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically-increasing sequence as the analog input is increased throughout the range. Thus, every input code width (quantum) must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur.

ADC674AKP, KH, and TH grades are guaranteed to have no missing codes to 12-bit resolution over their respective specification temperature ranges.

UNIPOLAR OFFSET ERROR

An ADC674A connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value. The unipolar offset temperature coefficient specifies the change of this transition value versus a change in ambient temperature.

TABLE I. Input Voltages, Transition Values, and LSB Values.

Binary (BIN) Output	Input Voltage Range and LSB Values				
Analog Input Voltage Range	Defined As.	±10V	+5V	0 to +10V	0 to +20V
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$ n = 8 n = 12	$\frac{20V}{2^n}$ 78 13mV 4 88mV	$\frac{10V}{2^n}$ 39 06mV 2.44mV	$\frac{10V}{2^n}$ 39 06mV 2 44mV	$\frac{20V}{2^n}$ 78 13mV 4 88mV
Output Transition Values					
FFE_H to FFF_H	+ Full-Scale Calibration	+10V − 3/2LSB	+5V − 3/2LSB	+10V − 3/2LSB	+10V − 3/2LSB
$7FF_H$ to 800_H	Midscale Calibration (Bipolar Offset)	0 − 1/2LSB	0 − 1/2LSB	+5V − 1/2LSB	±10V − 1/2LSB
000_H to 001_H	Zero Calibration (− Full-Scale Calibration)	−10V + 1/2LSB	−5V + 1/2LSB	0 to + 1/2LSB	0 to +1/2LSB

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The ADC674A specification, however, follows the terminology defined for the 574 converter several years ago. Thus, bipolar offset is located near the midscale value of 0V (bipolar zero) at the output code transition $7FF_H$ to 800_H.

Bipolar offset error for the ADC674A is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB below 0V. The bipolar offset temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

FULL SCALE CALIBRATION ERROR

The last output code transition (FFE_H to FFF_H) occurs for an analog input value 3/2LSB below the nominal full-scale value. The full scale calibration error is the deviation of the actual analog value at the last transition point from the ideal value. The full-scale calibration temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC674A assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the full-scale calibration value. This change, of course, results in a proportional change in all code transition values (i.e. a gain error). The specification describes the maximum change in the full-scale calibration value from the initial value for a change in each power supply voltage.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset and bipolar offset specify the maximum change from the +25°C value to the value at T_{MIN} or T_{MAX}.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

CODE WIDTH (QUANTUM)

Code width, or quantum, is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADC674A, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common. Analog common (pin 9) typically carries +8mA.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 should still be connected together at the converter; a single wide conductor pattern then connects these two pins to the system common. In either case, the common return of the analog input signal should be referenced to pin 9 of the ADC. This prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC674A as possible. If no trim adjustments are used, the fixed resistors should likewise be as close as possible.

POWER SUPPLY DECOUPLING

Logic and analog power supplies should be bypassed with 10μF tantalum type capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC674A will be driving into a nominal DC input impedance of either 5kΩ or 10kΩ. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

RANGE CONNECTIONS

The ADC674A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, and ±10V. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of the two is left unconnected. Full-scale and offset adjustments are described below.

To operate the converter with a 10.24V (2.5mV LSB) or 20.48V (5mV LSB) input range, insert a 120Ω 1% metal-film resistor in series with pin 13 for the 10.24V range, or a 240Ω 1% metal-film resistor in series with pin 14 for the 20.48V range. Offset adjustments are still performed as described below. A fixed metal-film resistor can be used because the input impedance of the ADC674A is trimmed to typically less than ±2% of the nominal value.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADC674A as shown in Figures 2 and 3 for unipolar and bipolar operation.

CALIBRATION PROCEDURE—UNIPOLAR RANGES

If adjustment of unipolar offset and full scale is not required, replace R_2 with a 50Ω, 1% metal film resistor and connect pin 12 to pin 9, omitting the adjustment network.

If adjustment is required, connect the converter as shown in Figure 2. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 20V range) that causes the output code to be DB0 ON (high). Adjust potentiometer R_1 until DB0 is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale value minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1-DB11 are ON and DB0 is toggling ON and OFF.

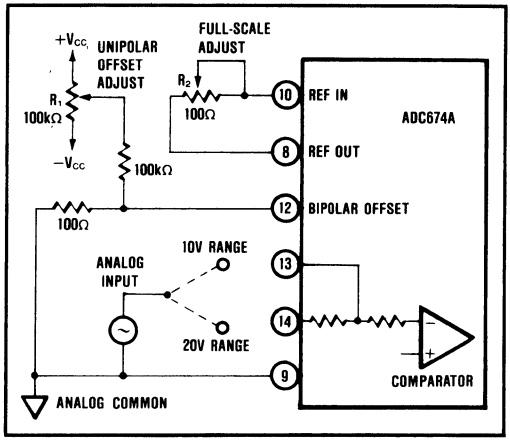


FIGURE 2. Unipolar Configuration.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, the potentiometers may be replaced by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 3. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (−4.9988V for the ±5V range, −9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

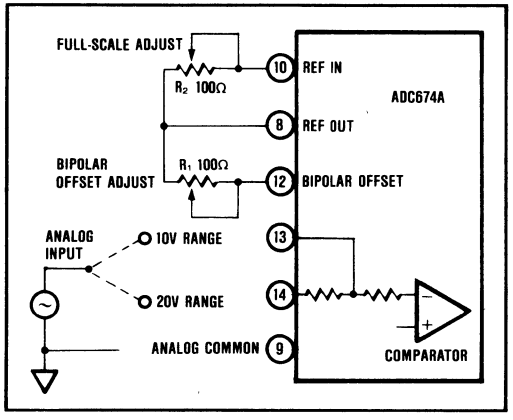


FIGURE 3. Bipolar Configuration.

CONTROLLING THE ADC674A

The Burr-Brown ADC674A can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the ouptut data when ready—choosing either 12 bits all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is listed in Table III.

TABLE III. Control Input Truth Table.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

TABLE II. ADC674A Control Line Functions.

Pin Designation	Definition	Function
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data 0-1 edge may be used to initiate a conversion
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data 1-0 edge may be used to initiate a conversion
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8 or 12-bit conversions 1-0 edge may be used to initiate a conversion Must be high ("1") to read output data 0-1 edge may be used to initiate a read operation
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in two 8-bit bytes, a_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte)
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ - "1" enables all 12 output bits simultaneously 12/$\overline{8}$ = "0" will enable the MSB's or LSB's as determined by the A_0 line

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to V_{LOGIC} (+5V). The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case the R/$\overline{C}$ pulse must remain low for a minimum of 50nsec.

Figure 4 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 5 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the output data from the previous conversion is enabled during the positive portion of R/C. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in Table IV.

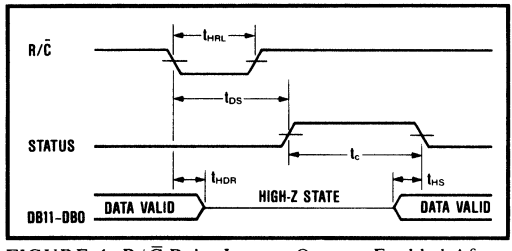


FIGURE 4. R/$\overline{C}$ Pulse Low — Outputs Enabled After Conversion.

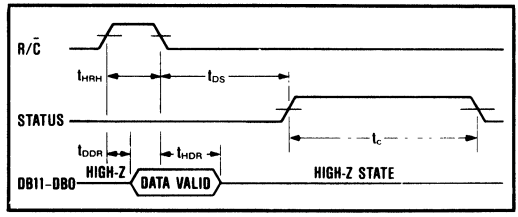


FIGURE 5. R/$\overline{C}$ Pulse High - Outputs Enabled Only While R/$\overline{C}$ Is High.

TABLE IV. Stand-Alone Mode Timing.

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	300	400	1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is low. If all 12 bits are read following an 8-bit conversion, the 3LSBs (DB0–DB2) will be low (logic 0) and DB3 will be high (logic 1). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter is commanded to initiate conversion by a transition occurring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change states simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50nsec prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 6. The specifications for timing are contained in Table V.

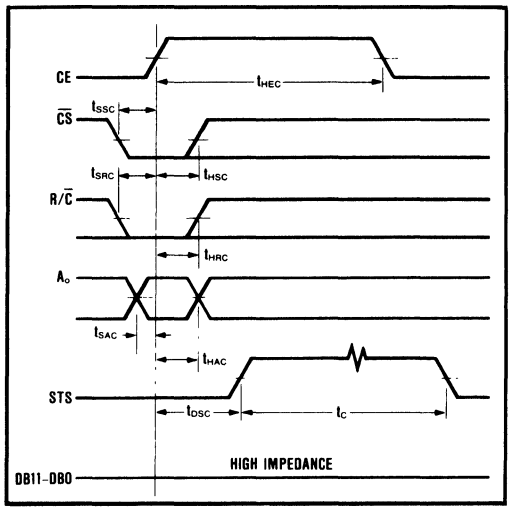


FIGURE 6. Conversion Cycle Timing.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

TABLE V. Timing Specifications.

Symbol	Parameter	Min	Typ	Max	Units
Convert Mode					
t_{DSC}	STS delay from CE		60	200	ns
t_{HEC}	CE Pulse width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE setup	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns
t_C	Conversion time, 12 bit cycle	9	12	15	µs
	8 bit cycle	6	8	10	µs
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE setup	0			ns
t_{SAR}	A_0 to CE setup	50	25		ns
t_{HSR}	$\overline{CS}$ valid after CE low	0			ns
t_{HRR}	R/$\overline{C}$ high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns
t_{HS}	STS delay after data valid	100	300	600	ns

NOTE Specifications are at +25°C and measured at 50% level of transitions

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 7 and Table V for timing relationships and specifications.

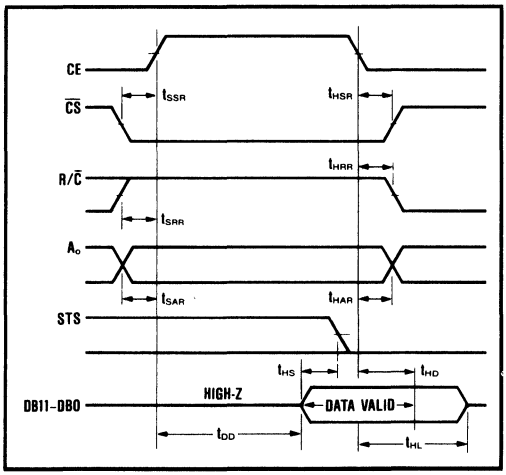


FIGURE 7. Read Cycle Timing.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is high, all 12 output lines (DB0 DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored.

When 12/$\overline{8}$ is low, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the read cycle. Connection of the ADC674A to an 8-bit bus for transfer of left-justified data is illustrated in Figure 9. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

When A_0 is low, the byte addressed contains the 8MSBs. When A_0 is high, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 8. The design of the ADC674A guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together as illustrated in Figure 9 cannot be enabled at the same time.

In the majority of applications the read operation will be attempted only after the conversion is complete and the STATUS output has gone low. In those situations requiring the earliest possible access to the data, the read may be started as much as 750nsec (t_{DD} max + t_{HS} max) before STATUS goes low. Refer to Figure 7 for these timing relationships.

BURN-IN SCREENING

Burn-in screening is available for both plastic and ceramic package ADC674As. Burn-in duration is 160 hours at the temperature (or equivalent combination of time and temperature) indicated below:

Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are 100% electrically tested after burn-in is completed. To order burn-in, add "-BI" to the base model number (e.g., ADC674AKP-BI). See Ordering Information for pricing.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 8. 12-Bit Data Format for 8-Bit Systems.

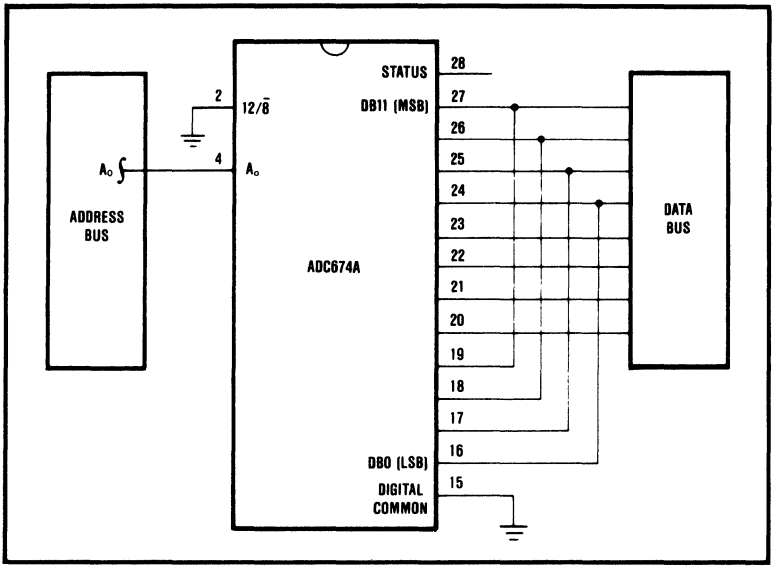


FIGURE 9. Connection to an 8-bit Bus.

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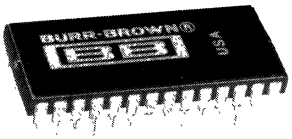


ADC700

ADVANCE INFORMATION
SUBJECT TO CHANGE

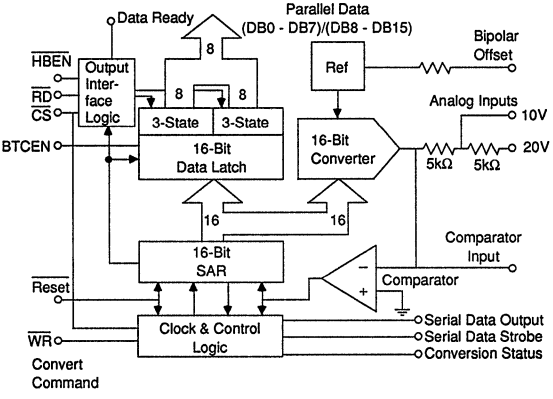
16-Bit Resolution A/D CONVERTER With Microprocessor Interface

FEATURES

- COMPLETE WITH REFERENCE, CLOCK, 8-BIT PORT MICROPROCESSOR INTERFACE
- OUTPUT BUFFER LATCH FOR IMPROVED INTERFACE TIMING FLEXIBILITY
- CONVERSION TIME: 15µs max (0°C to 70°C, –25°C to +85°C); 20µs max (–55°C to +125°C)
- LINEARITY ERROR: ±0.003%FSR max (K, S Grades)
- NO MISSING CODES TO 14 BITS OVER TEMPERATURE (K, S Grades)
- SPECIFIED OPERATION AT ±12V AND ±15V POWER SUPPLIES
- PARALLEL AND SERIAL DATA OUTPUT
- SMALL PACKAGE: 28-Pin DIP

APPLICATIONS

- PRECISION CONTROL
- HIGH-RESOLUTION DATA ACQUISITION
- MICROPROCESSOR-DRIVEN DATA ACQUISITION SYSTEMS
- WAVEFORM ANALYSIS INSTRUMENTATION



DESCRIPTION

ADC700 is a 16-bit resolution successive approximation analog-to-digital converter. It is complete with a self-contained reference, internal clock and complete digital interface, including output data latch and three-state output drivers for operation with microprocessors and microcontrollers.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Gain and Zero errors may be externally trimmed to zero. Internal scaling resistors are provided for selection of analog input ranges of 0V to +5V, 0V to +10V, 0V to +20V, ±2.5V, ±5V, and ±10V.

Conversion time is factory set at for 15µs max over temperature for a 16-bit conversion over the industrial temperature range, –25°C to +85°C; 20µs max for the military temperature range.

After a conversion is complete, output data is stored in a latch separate from the successive approximation logic. This permits starting the next conversion before the data from the previous conversion is read. Data is available in two 8-bit bytes from TTL-compatible three-state output drivers. Output data is coded in Straight Binary for unipolar input signals and Bipolar Offset Binary or Twos Complement for bipolar input signals. BOB or BTC is selected by a logic function available on one of the pins.

The ADC700, available in commercial, industrial, and military temperature ranges, requires supply voltages of +5V, ±12V, or ±15V. It is packaged in a hermetic 28-pin side-braze ceramic DIP.

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PDS-856

SPECIFICATIONS

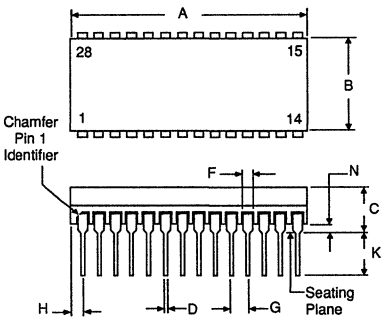
T_A = 25°C and at rated supplies: V_{DD} = +5V, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = −12V or −15V unless otherwise noted.

MODEL	ADC700JH/AH/RH			ADC700KH/BH/SH			
PARAMETERS	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
RESOLUTION			16			*	BITS
ANALOG INPUTS							
Voltage Ranges							
Bipolar		±2.5, ±5, ±10			*		V
Unipolar		0 to +5, 0 to +10, 0 to +20			*		V
Impedance (Direct Input)							
0V to +5V, ±2.5V		2.5 ±1%			*		kΩ
0V to +10V, ±5V		5 ±1%			*		kΩ
0V to +20V, ±10V		10 ±1%			*		kΩ
DIGITAL SIGNALS (Over Specification Temperature Range)							
Inputs							
Logic Levels [1]							
V_{IH}	+2.0		+5.5	*		*	V
V_{IL}	0		+0.8	*		*	V
I_{IH}(V_I = +2.7V)			±10			*	µA
I_{IL}(V_I = +0.4V)			±20			*	µA
Outputs							
Logic Levels							
V_{OL}(I_{OL} = −1.6mA)			+0.4			*	V
V_{OH}(I_{OH} = +20uA)	+2.4			*			V
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error			±0.003			±0.003	% of FSR[2]
Differential Linearity Error		±0.003			±0.0015		% of FSR
Gain Error[3]		±0.1	±0.2		*	*	%
Zero Error[3]							
Bipolar Zero		±0.1	±0.2		*	*	% of FSR
Unipolar Zero		±0.05	±0.1		*	*	% of FSR
Inherent Quantization Error		±1/2			*		LSB
Noise at Transitions (3σp-p)		±0.001			*		% of FSR
Power Supply Sensitivity							
$+V_{CC}$		±0.0015			*		%FSR/%V_{CC}
$-V_{CC}$		±0.0015			*		%FSR/%V_{CC}
V_{DD}		±0.0001			*		%FSR/%V_{DD}
CONVERSION TIME							
16-bits			15			20	µs
WARM-UP TIME	5			*			min
DRIFT (Over Specification Temperature Range)							
Gain Drift		±8			*		ppm/°C
Zero Drift							
Bipolar Zero		±5			*		ppm of FSR/°C
Unipolar Zero		±2			*		ppm of FSR/°C
Linearity Drift		±1			*		ppm of FSR/°C
OUTPUT							
DATA CODES[4]							
Unipolar Parallel		USB			*		
Bipolar Parallel[5]		BTC, BOB			*		
Serial Output (NRZ)		USB, BOB			*		
POWER SUPPLY REQUIREMENTS							
Voltage Range							
$+V_{CC}$	+11.4	+15	+16	*	*	*	VDC
$-V_{CC}$	−11.4	−15	−16	*	*	*	VDC
V_{DD}	+4.75	+5	+5.25	*	*	*	VDC
Current[6]							
$+V_{CC}$		+10	+12		*	*	mA
$-V_{CC}$		−28	−33		*	*	mA
V_{DD}		+15	+18		*	*	mA
Power Dissipation		645	765		*	*	mW
TEMPERATURE RANGE							
Specification							
J, K Grades	0		+70	*		*	°C
A, B Grades	−25		+85	*		*	°C
R, S Grades	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C

NOTES: (1) TTL, LSTTL, and 5V CMOS compatible. (2) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (3) Externally adjustable to zero. (4) USB — Unipolar Straight Binary; BTC — Binary Twos Complement; BOB — Bipolar Offset Binary; NRZ — Non Return to Zero. (5) BTC/BOB is pin selectable with pin 23, BTCEN. (6) Max supply current is specified at rated supply voltages.

MECHANICAL

H Package — 28-Pin Ceramic DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	.610 BASIC		15.49 BASIC	
C	.160	.205	4.06	5.21
D	.015	.019	0.38	0.48
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.055	.095	1.40	2.41
J	.009	.012	0.23	0.30
K	.155	.195	3.94	4.95
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

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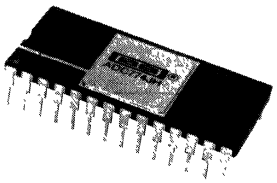


ADC774

ADVANCE INFORMATION SUBJECT TO CHANGE

Microprocessor-Compatible ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, OR 16-BIT MICROPROCESSOR BUS INTERFACE**
- **IMPROVED PERFORMANCE SECOND SOURCE FOR HI774-TYPE A/D CONVERTER**
  - **Conversion Time: 8.5μs max**
  - **Bus Access Time: 150ns**
- **FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES**
- **NO MISSING CODES OVER TEMPERATURE:**
  - **0°C to +75°C: ADC774JH, KH Grades**
  - **–55°C to +125°C: ADC774SH, TH Grades**

DESCRIPTION

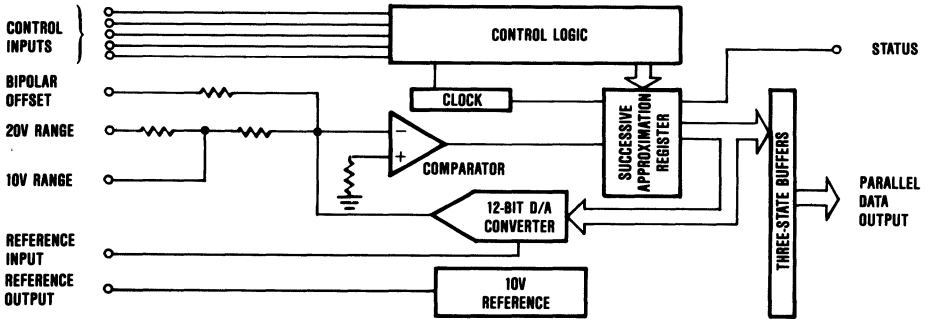
The ADC774 is a 12-bit successive approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 8.5μs maximum.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC774, available in both industrial and military temperature ranges, requires supply voltages of +5V and ±12V or ±15V. It is packaged in a 28-pin plastic DIP, or hermetic side-brazed ceramic DIP.



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PDS-835

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified.

MODEL	ADC774JH, ADC774SH			ADC774KH, ADC774TH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			*	Bits
INPUTS							
ANALOG							
Voltage Ranges. Unipolar		0 to +10, 0 to +20			*		V
Bipolar		±5, ±10			*		V
Impedance· 0 to +10V, ±5V	4 7	5	5 3	*	*	*	kΩ
±10V, 0V to +20V	9.4	10	10.6	*	*	*	kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/8)							
Over Temperature Range							
Voltages Logic 1	+2 0		+5.5	*		*	V
Logic 0	−0.5		+0.8	*		*	V
Current	−5	0.1	+5	*	*	*	μA
Capacitance		5			*		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (adjustable to zero)			±2			*	LSB
Bipolar Offset Error (adjustable to zero)			±10			±4	LSB
Full-Scale Calibration Error[1]							
(adjustable to zero)			±0.3			*	% of FS[2]
No Missing Codes Resolution (Diff Linearity)	11			12			Bits
Inherent Quantization Error		±1/2			*		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	LSB
S, T Grades			±1			±1/2	LSB
Full-Scale Calibration Error							
Without Initial Adjustment[1]: J, K Grades			±0.5			±0.4	% of FS
S, T Grades			±0.8			±0.5	% of FS
Adjusted to zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
TEMPERATURE COEFFICIENTS (T_{MIN} to T_{MAX})[3]							
Unipolar Offset: J, K Grades			±10			±5	ppm/°C
S, T Grades			±5			±2.5	ppm/°C
Max Change: All Grades			±2			±1	LSB
Bipolar Offset: All Grades			±10			±5	ppm/°C
Max Change: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration· J, K Grades			±45			±25	ppm/°C
S, T Grades			±50			±25	ppm/°C
Max Change: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration							
+13 5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V			±2			±1	LSB
−16 5V < V_{EE} < −13 5V or −12 6V < V_{EE} < −11.4V			±2			±1	LSB
+4.5V < V_{LOGIC} < +5 5V			±1/2			*	LSB
CONVERSION TIME							
8-Bit Cycle		4.6	5.2		*	*	μs
12-Bit Cycle		7.5	8.5		*	*	μs
OUTPUTS							
DIGITAL (DB_{11} — DB_0, STATUS)							
(Over Temperature Range)							
Output Codes. Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels. Logic 0 (I_{SINK} = 1 6mA)			+0.4			*	V
Logic 1 (I_{SOURCE} = 500μA)	+2 4			*			V
Leakage, Data Bits Only, High-Z State	−5	0 1	+5	*	*	*	μA
Capacitance		5			*		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+9.9	+10.0	+10 1	*	*	*	V
Source Current Available for External Loads[6]	2.0			*			mA

ELECTRICAL (CONT)

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified.

MODEL	ADC774JH, ADC774SH			ADC774KH, ADC774TH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Voltage V_{CC}	+11.4		+16 5	*		*	V
V_{EE}	−11.4		−16.5	*		*	V
V_{LOGIC}	+4 5		+5.5	*		*	V
Current: I_{CC}		3.5	5		*	*	mA
I_{EE}		15	20		*	*	mA
I_{LOGIC}		9	15		*	*	mA
Power Dissipation (±15V Supplies)		325	450		*	*	mW
TEMPERATURE RANGE (Ambient. T_{MIN}, T_{MAX})							
Specification: J, K Grades	0		+75	*		*	°C
S, T Grades	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C

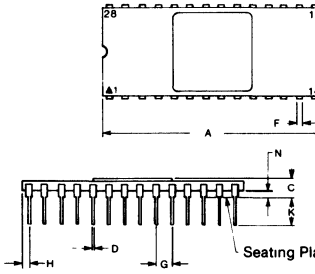
*Same specification as ADC774JH, SH

NOTES (1) With fixed 50Ω resistor from REF OUT to REF IN This parameter is also adjustable to zero at +25°C (2) FS in this specification table means Full Scale Range That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V The term Full Scale for these specifications instead of Full-Scale Range is used to be consistent with other vendors' specification tables. (3) Using internal reference (4) External loading must be constant during conversion The reference output requires no buffer amplifier with either ±12V or ±15V power supplies

MECHANICAL

H Package [Ceramic]

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 386	1 414	35 20	35 92
C	108	166	2 74	4 22
D	015	021	0 38	0 53
F	035	060	0 89	1 52
G	100 BASIC		2 54 BASIC	
H	036	064	0 91	1 63
J	008	012	0 20	0 30
K	120	240	3 05	6 10
L	600 BASIC		15 24 BASIC	
M	—	10°	—	10°
N	025	060	0 64	1 52



NOTE Leads in true position within 0 01" (0 25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers may not be marked on package

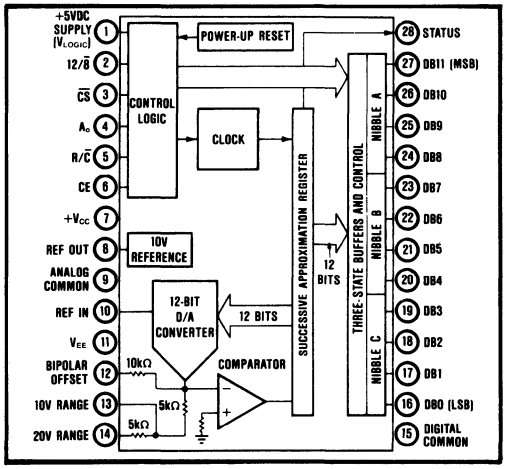
CASE Ceramic, hermetic
WEIGHT 4 8 grams (0 17 oz)

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common ..... 0 to +16 5V
V_{EE} to Digital Common ..... 0 to −16 5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/8, R/$\overline{C}$) to Digital Common ..... −0 5V to V_{LOGIC} +0 5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to Analog Common ..... ±16 5V
$20V_{IN}$ to Analog Common ..... ±24V
REF OUT ..... Indefinite Short to Common, Momentary Short to V_{CC}
Max Junction Temperature ..... +165°C
Power Dissipation 1000mW
Lead Temperature (soldering, 10s) ..... +300°C
Thermal Resistance, θ_{JA} Ceramic ..... 50°C/W

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

CONNECTION DIAGRAM



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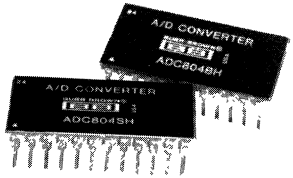


ADC804

Serial Output ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 17μsec CONVERSION TIME
- SERIAL OUTPUT—Ideal for applications requiring isolation or long-distance data transmission
- <500mW POWER DISSIPATION
- 24-PIN DUAL-WIDE HERMETIC PACKAGE
- FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES
- ±0.012% INTEGRAL LINEARITY
- 12-BIT RESOLUTION
- TWO TEMPERATURE RANGES AVAILABLE:
  ADC804BH for −25°C to +85°C Operation
  ADC804SH for −55°C to +125°C Operation
- NO MISSING CODES −25°C TO +85°C

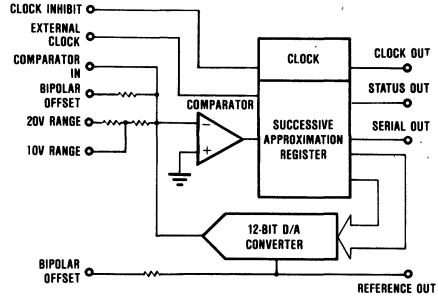
DESCRIPTION

The ADC804 is a 12-bit successive approximation analog-to-digital converter, custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a comparator, a monolithic 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, and a CMOS logic chip containing the successive approximation register (SAR), clock, and all other associated logic funtions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial end-point accuracies of better than ±0.012% (±1/2LSB). The ADC804 has two grades, one completely specified for −25°C to +85°C operation (ADC804BH), and the other for −55°C to +125°C operation (ADC804SH).

The maximum conversion time of 17μsec makes the ADC804 ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 59kHz. In addition, an external clock may be used to synchronize the converter to the system clock or to obtain faster operation. As an added benefit for ADC80 users employing the serial output capability, the ADC804 is designed to replace or provide an alternate source to ADC80 with a minimum of circuit board changes and it provides a 40% reduction in conversion time.

Data is available in serial form with corresponding clock and status signals. Elimination of the parallel output capability enables the ADC804 to be the smallest fully self-contained 12-bit ADC available today. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC804 operates equally well with either ±15V or ±12V analog power supplies, and also requires use of a +5V logic supply. It is packaged in a hermetic 24-pin side-brazed ceramic dual-in-line package.



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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V unless otherwise specified

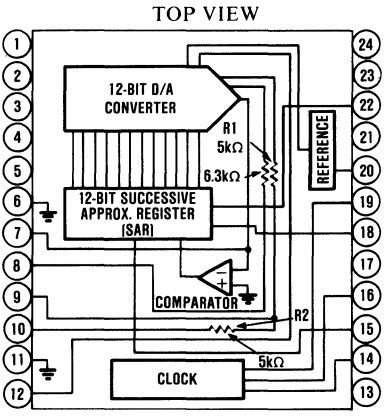
MODEL	ADC804BH			ADC804SH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			*	Bits
INPUT							
ANALOG							
Voltage Ranges Unipolar		0 to +5, 0 to +10			*		V
Bipolar		±2 5, ±5, ±10			*		V
Impedance 0 to +5V, ±2 5V		2 3			*		kΩ
0 to +10V, +5V		4 6			*		kΩ
±10V		9 2			*		kΩ
DIGITAL							
Logic Characteristics (over specification temperature range)							
V_{IH} (logic "1")	2 0		5 5	*		*	V
V_{IL} (logic "0")	−0 3		+0 8	*		*	V
I_{IH} (V_{IN} = +2 7V)			−150			*	μA
I_{IL} (V_{IN} =+0 4V)			500			*	μA
Convert Command Pulse Width	100		1200	*		*	nsec
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error[1]		±0 1	±0 3		*	*	% of FSR[2]
Offset Error[1] Unipolar		±0 05	±0 2		*	*	% of FSR
Bipolar		±0 1	±0 3		*	*	% of FSR
Linearity Error			±0 012			*	% of FSR
Differential Linearity Error			±1			*	LSB
Inherent Quantization Error		1/2			*		LSB
POWER SUPPLY SENSITIVITY							
+13 5V ≤ +V_{CC} ≤ +16 5V or +11 4V ≤ +V_{CC} ≤ +12 6V		±0.003	±0 009		*	*	% of FSR/%V_{CC}
−16 5V ≤ −V_{CC} ≤ −13 5V or −12 6V ≤ −V_{CC} ≤ −11 4V		±0 003	±0 009		*	*	% of FSR/%V_{CC}
+4 5V ≤ V_{DD} ≤ +5 5V		±0 002	±0.005		*	*	% of FSR/%V_{DD}
DRIFT							
Total Accuracy, Bipolar[3]		±10	±23		*	*	ppm/°C
Gain		±15	±30		*	*	ppm/°C
Offset Unipolar		±3			*		ppm of FSR/°C
Bipolar		±7	±15		*	*	ppm of FSR/°C
Linearity Error Drift		±1	±3		*	*	ppm of FSR/°C
Differential Linearity over Temperature Range			+1, −3/4			*	LSB
No Missing Code Temperature Range	−25		+85	−55		+125	°C
Monotonicity Over Temperature Range		Guaranteed			Guaranteed		
CONVERSION TIME[4]		15	17		*	*	μsec
OUTPUTS							
DIGITAL(Clock Out, Status, Serial Out)							
Output Codes, Serial (NRZ)[5]		CSB,COB			*		
Logic Levels. Logic 0 (I_{sink} ≤ 3 2mA)			+0 4			*	V
Logic 1 (I_{source} ≤ 80μA)	+2.4			*			V
Internal Clock Frequency		92 3			*		kHz
INTERNAL REFERENCE VOLTAGE							
Voltage	+6 2	+6 3	+6 4	*	*	*	V
Source Current Available for External Loads[6]	200			*			μA
Temperature Coefficient		±10	±30		*	*	ppm/°C
POWER SUPPLY REQUIREMENTS							
Voltage, ±V_{CC}	±11 4	±15	±16 5	*	*	*	V
V_{DD}	+4 5	+5 0	+5 5	*	*	*	V
Current, +I_{CC}		5	8 5		*	*	mA
−I_{CC}		21	26		*	*	mA
I_{DD}		11	15		*	*	mA
Power Dissipation (±V_{CC} = 15V)		450	595		*	*	mW
TEMPERATURE RANGE (Ambient)							
Specification	−25		+85	−55		+125	°C
Storage	−65		+150	*		*	°C

*Same as specification for ADC804BH

NOTES (1) Gain and offset errors are adjustable to zero See "Optional External Gain and Offset Adjustments" section (2) FSR means full-scale range and is 20V for ±10V Range, 10V for ±5V and 0 to +10V ranges, etc (3) Includes drift due to linearity, gain, and offset drifts (4) Conversion time is specified using internal clock For operation with an external clock see "Clock Options" section (5) CSB means Complementary Straight Binary, and COB means Complementary Offset Binary, NRZ means non-return-to-zero coding See Table I for additional information (6) External loading must be constant during conversion, and must not exceed 200μA for guaranteed specifications

CONNECTION DIAGRAM

Pin 1 - N/C
Pin 2 - N/C
Pin 3 - N/C
Pin 4 - N/C
Pin 5 - V_{DD}
Pin 6 - Digital Common
Pin 7 - Comparator In
Pin 8 - Bipolar Offset
Pin 9 - R1 10V Range
Pin 10 - R2 20V Range
Pin 11 - Analog Common
Pin 12 - Gain Adjust
Pin 24 - N/C
Pin 23 - N/C
Pin 22 - Serial Out
Pin 21 - $-V_{CC}$
Pin 20 - Reference Out (+6.3V)
Pin 19 - Clock Out
Pin 18 - Status
Pin 17 - N/C
Pin 16 - Clock Inhibit
Pin 15 - External Clock
Pin 14 - Convert Command
Pin 13 - $+V_{CC}$



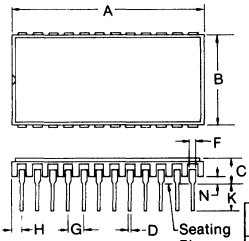
ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Analog Common ..... 0 to +16.5V
$-V_{CC}$ to Analog Common ..... 0 to −16.5V
V_{DD} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±0.5V
Logic Inputs (Convert Command, Clock In) to Digital Common ..... −0.3V to V_{DD} +0.5V
Analog Inputs (Analog In, Bipolar Offset) to Analog Common ..... ±16.5V
Reference Output ..... Indefinite Short to Common, Momentary Short to V_{CC}
Power Dissipation 1000mW
Lead Temperature, Soldering ..... +300°C, 10sec
Thermal Resistance, θ_{JA} ..... 60°C/W

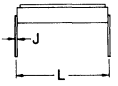
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

MECHANICAL



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.238	1.262	31.45	32.05
B	.586	.602	14.88	15.29
C	.160	.196	4.06	4.98
D	.016	.020	0.41	0.51
F	.038	.042	0.97	1.07
G	.100 BASIC		2.54 BASIC	
H	.067	.085	1.70	2.16
J	.008	.012	0.20	0.30
K	.170 BASIC		4.32 BASIC	
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

ORDERING INFORMATION

Model	Temperature Range
ADC804BH	-25°C to +85°C
ADC804BHQ	-25°C to +85°C
ADC804SH	-55°C to +125°C
ADC804SHQ	-55°C to +125°C
BURN-IN SCREENING OPTION See text for details	
Model	**Burn-In Temp. (160h)[1]**
ADC804BH-BI	+125°C
ADC804SHQ	+125°C

NOTE: Or equivalent combination. See text

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Under this definition of linearity (sometimes referred to as integral linearity), ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale, providing a significantly better definition of converter accuracy than the best-straight-line-fit definition of linearity employed by some manufacturers. The zero or minus full-scale value is located at an analog input value 1/2LSB before the first code transition (FFF_H to FFE_H). The plus full-scale value is located at an analog value 3/2LSB beyond the last code transition (001_H to 000_H). See Figure 1, which illustrates these relationships. A linearity specification which guarantees ±1/2LSB maximum linearity error assures the user that no code transition will differ from the ideal transition value by more than ±1/2LSB.

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V operation), the minus full-scale value of −10V is 2.44mV below the first code transition (FFF_H to FFE_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (001_H to 000_H at +9.99268V). Ideal transitions occur 1LSB (4.88mV) apart, and the ±1/2LSB linearity specification guarantees that no actual transition will vary from the ideal by more than 2.44mV. The LSB weights, transition values, and

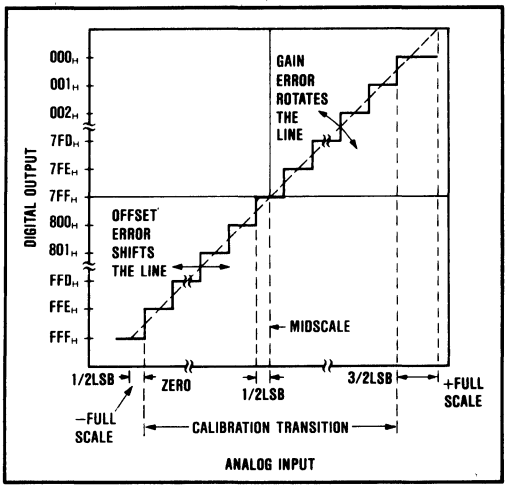


FIGURE 1. ADC804 Transfer Characteristic Terminology.

code definitions for each possible ADC804 analog input signal range are described in Table I.

CODE WIDTH (QUANTUM)

Code width (or quantum) is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB, which for 12-bit operation with a 20V span is equal to 4.88mV. Refer to Table I for LSB values for other ADC804 input ranges.

DIFFERENTIAL LINEARITY ERROR AND NO MISSING CODES

Differential linearity error is a definition of the difference between an ideal 1LSB code width (quantum) and the actual code width. A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input is increased throughout the range, requiring that every input quantum must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur but the converter may still be monotonic. Thus, no missing codes represent a more stringent definition of performance than does monotonicity. The ADC804BH is guaranteed to have no missing codes to 12-bit resolution over its full specification temperature range of −25°C to +85°C, and the ADC804SH displays no missing codes over the temperature range of −55°C to +125°C.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

UNIPOLAR OFFSET ERROR

An ADC804 connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value, and is applicable only to converters operating in the unipolar mode.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset at the first transition value above the minus full-scale value. The ADC804 follows this convention. Thus, bipolar offset error for the ADC804 is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB above minus full scale.

GAIN ERROR

The last output code transition (001_H to 000_H) occurs for an analog input value 3/2LSB below the nominal plus full-scale value. Gain error is the deviation of the actual analog value at the last transition point from the ideal value.

ACCURACY DRIFT VS TEMPERATURE

The temperature coefficients for gain, unipolar offset, and bipolar offset specify the maximum change from the actual 25°C value to the value at the extremes of the specification range. The temperature coefficient applies independently to the two halves of the temperature range above and below +25°C.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC804 assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the plus full-scale value. This change, of

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

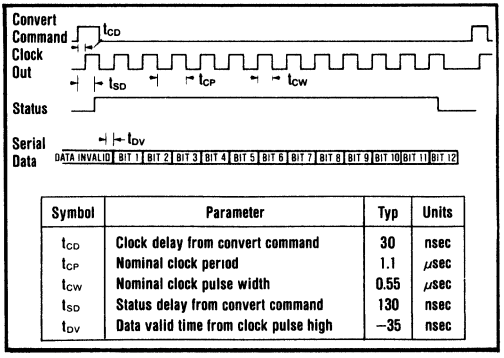
Binary (BIN) Output	Input Voltage Range and LSB Values					
Analog Input Voltage Range	Defined As	±10V	±5V	±2 5V	0 to +10V	0 to +5V
Code Designation		COB*	COB*	COB*	CSB**	CSB**
One Least Significant Bit (LSB)	FSR/2^n n = 12	20V/2^n 4 88mV	10V/2^n 2 44mV	5V/2^n 1 22mV	10V/2^n 2 44mV	5V/2^n 1 22mV
Transition Values MSB LSB						
001_H to 000_H	+Full Scale	+10V − 3/2LSB	+5V − 3/2LSB	+2 5V − 3/2LSB	+ 10V − 3/2LSB	+5V − 3/2LSB
800_H to $7FF_H$	Mid Scale	0	0	0	+5V	+ 2 5V
FFF_H to FFE_H	−Full Scale	−10V + 1/2LSB	−5V + 1/2LSB	−2 5V + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

*COB = Complementary Offset Binary **CSB = Complementary Straight Binary

course, results in a proportional change in all code transition values (i.e. a gain error). The specification describes the maximum change in the plus full-scale value from the initial value for independent changes in each power supply voltage.

TIMING CONSIDERATIONS

Timing relationships of the ADC804 are shown in Figure 2. It should be noted that although the convert command pulse width must be between 100nsec and 1.2μsec to obtain the specified conversion time with internal clock, the ADC804 will accept longer convert commands with no loss of accuracy, assuming that the



Symbol	Parameter	Typ	Units
t_{CD}	Clock delay from convert command	30	nsec
t_{CP}	Nominal clock period	1.1	μsec
t_{CW}	Nominal clock pulse width	0.55	μsec
t_{SD}	Status delay from convert command	130	nsec
t_{DV}	Data valid time from clock pulse high	−35	nsec

FIGURE 2. ADC804 Timing Diagram (normal values at +25°C with internal clock).

analog input signal is stable. In this situation, the actual indicated conversion time (during which status is high) for 12-bit operation will be equal to approximately 600nsec less than the sum of the factory-set conversion time and the length of the convert command. The code returned by the converter at the end of the conversion will accurately represent the analog input to the converter at the time the convert command returns to the low state. In addition, although the initial state of the converter will be indeterminate when power is first applied, it is designed to time-out and be ready to accept a convert command within approximately 15μsec after power-up, provided that either an external clock source is present or the internal clock is not inhibited.

During conversion, the decision as to the proper state of any bit (bit "n") is made on the rising edge of clock pulse " n + 1". Thus, a complete conversion requires 13 clock pulses with the status output dropping from logic "1" to logic "0" shortly after the rising edge of the thirteenth clock pulse. A new conversion may not be initiated until 50nsec after the fall of the thirteenth clock pulse. Additional convert commands applied during conversion will be ignored.

DEFINITION OF DIGITAL CODES

Two binary codes are available on the serial output of the ADC804, complementary straight binary (CSB) for unipolar input signal ranges, and complementary offset binary (COB) for bipolar input ranges. Both are complementary codes, meaning that logic "0" is true. Serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. All clock pulses available from the ADC804 have a nominal pulse width of 550nsec to facilitate transfer of the serial data into external logic devices without external shaping.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected together internally in the ADC804 but should be connected together as close to the unit as possible, preferably to an analog common ground plane beneath the converter. If these common lines must be run separately, use a wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog input lines and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common. If external gain and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC804 as possible.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 1μF to 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC804 will be driving into a nominal DC input impedance of 2.5kΩ to 10kΩ. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

INPUT SCALING

The ADC804 offers five standard input ranges: 0V to+5V, 0V to +10V, ±2.5V, ±5V, and ±10V. The input range should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the converter. Select the appropriate

input range as indicated by Table II. The input circuit architecture is illustrated in Figure 3. Use of external padding resistors to modify the factory-set input ranges (such as addition of a small external input resistor to change the 10V range to a 10.24V range) will require matching of the external fixed resistor values to individual devices, due to the large tolerance of the internal input resistors. Alternatively, the gain range of the converter may be easily increased a small amount by use of a low temperature coefficient potentiometer in series with the analog input signal or by decreasing the value of the gain adjust series resistor in Figure 6.

TABLE II. ADC804 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 8 To Pin	Connect Pin 10 To	Connect Input Signal To
±10V	COB	7	Input Signal	10
±5V	COB	7	Open	9
±2 5V	COB	7	Pin 7	9
0 to +5V	CSB	11	Pin 7	9
0 to +10V	CSB	11	Open	9

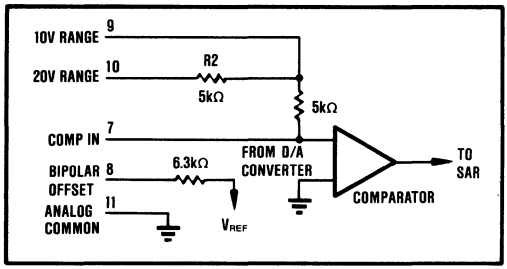


FIGURE 3. ACD804 Input Scaling Circuit.

REPLACEMENT OF ADC80

As illustrated in Figure 4, a circuit board configured for use of the ADC80 serial output capability may be very easily adapted to also use the ADC804, or to achieve space savings due to the smaller package of the ADC804. The pin assignments of the ADC804 have been chosen to allow it to fit neatly into one corner of the ADC80

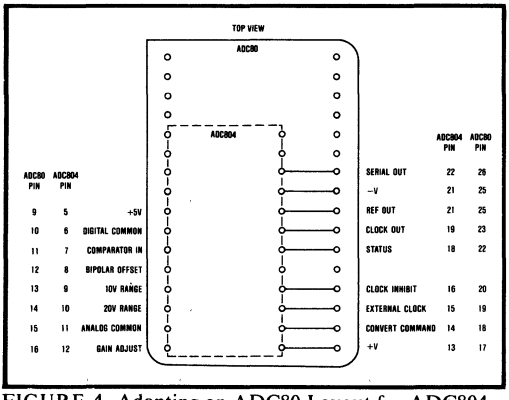


FIGURE 4. Adapting an ADC80 Layout for ADC804.

layout. When replacing ADC80 with ADC804, a board space improvement of approximately 1.25 square inches (8.06cm^2) is obtained.

CALIBRATION

Optional External Gain and Offset Adjustments

Gain and offset errors may be trimmed to zero using external offset and gain trim potentiometers connected to the ADC804 as shown in Figures 5 and 6 for both unipolar and bipolar operation. Multiturn potentiometers with 100ppm/°C or better TCR are recommended for minimum drift over temperature and time. These potentiometers may be of any value between 10kΩ and 100kΩ. All fixed resistors should be 20% carbon or better. Although not necessary in some applications, pin 12 (Gain Adjust) should be preferably bypassed with a 0.01μF nonpolarized capacitor to analog common to minimize noise pickup at this high impedance point, even if no external adjustment is required.

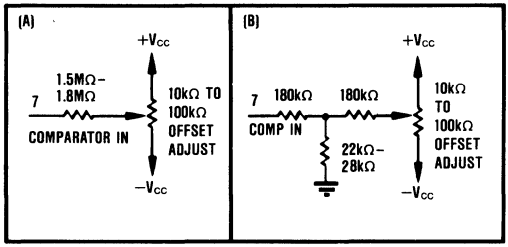


FIGURE 5. Two Methods of Connecting Optional Offset Adjust.

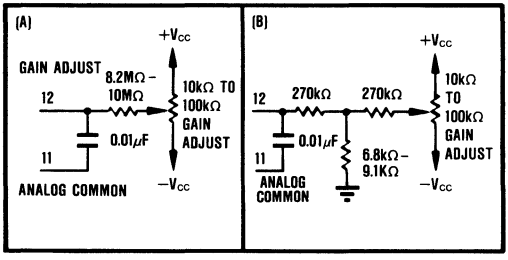


FIGURE 6. Two Methods of Connecting Optional Gain Adjust.

Adjustment Procedure

OFFSET—Connect the offset potentiometer as shown in Figure 5. Set the input voltage to the nominal zero or minus full-scale voltage plus 1/2LSB. For example, referring to Table I, this value is −10V + 2.44mV or −9.99756V for the −10V to +10V range.

With the input voltage set as above, adjust the offset potentiometer until an output code is obtained which is alternating between FFE_H and FFF_H with approximately 50% occurrence of each of the two codes. In other words, the potentiomter is adjusted until bit 12 (the LSB) indicates a true (logic "0") condition approximately half the time.

GAIN—Connect the gain adjust potentiometer as shown in Figure 6. Set the input voltage to the nominal plus full-scale value minus 3/2LSB. Once again referring to Table I, this value is +10V − 7.32mV or +9.99268V for the −10V to +10V range. Adjust the gain potentiometer until the output code is alternating between 000_H and 001_H with an approximate 50% duty cycle. As in the case of offset adjustment, this procedure sets the converter end-point transition to a precisely known value.

CLOCK OPTIONS

The ADC804 is extremely versatile in that it can be operated with either internal or external clock. Thus, use of an available system clock enables synchronization of the converter to the rest of the system to optimize performance in a noisy environment.

When operating with the internal clock, pin 15 (external clock input) and pin 16 (clock inhibit) may be left unconnected. No external pull-ups are required due to the inclusion of pull-up resistors in the ADC804. Pin 16 (clock inhibit) must be grounded for use with an external clock, which is applied to pin 15.

See Figures 7 through 10 for diagrams to implement the various clock options.

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown Q models

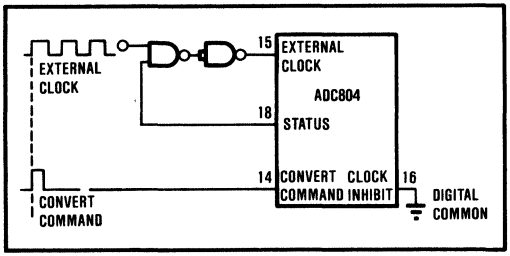


FIGURE 8. Continuous External Clock. (Conversion initiated by rising edge of convert command. The convert command must be synchronized with clock.)

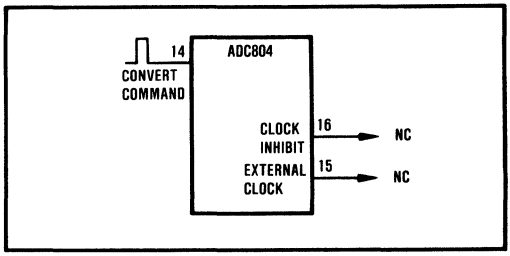


FIGURE 7. Internal Clock—Normal Operating Mode. (Conversion initiated by the rising edge of the convert command. The internal clock runs only during conversion.)

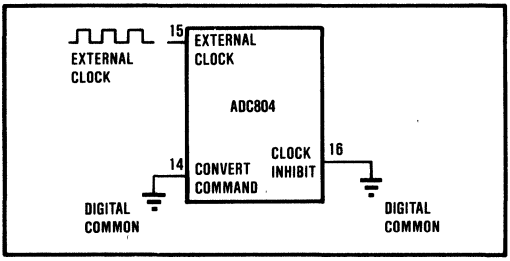


FIGURE 9. Continuous Conversion with external Clock. (Conversion is initiated by 14th clock pulse. Clock runs continuously.)

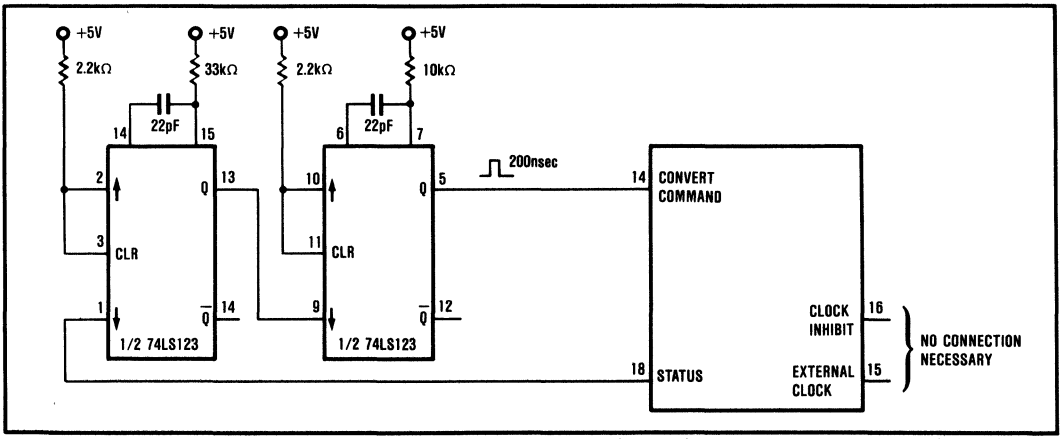


FIGURE 10. Continuous Conversion with 200nsec between Conversions Using Internal Clock. (Circuit insures that the conversion process will start when power is applied.)

are environmentally-screened versions of our standard industrial products, designed to provide enhanced reliability. The screening illustrated in Table III is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

BURN-IN SCREENING

Burn-in screening is an option available for the ADC804. Burn-in duration is 160 hours at +125°C ambient temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "BI" to the base model number.

TABLE III. Screening Flow for ADC804xHQ

Screen	MIL-STD-883 Method, Condition	Screening Level
Internal Visual	Burr-Brown QC4118	
High Temperature Storage (Stabilization Bake)	1008, C	24 hour, +150°C
Temperature Cycling	1010, C	10 cycles, −65°C to +150°C
Constant Acceleration	2001, A	5000 G
Electrical Test	Burr-Brown test procedure	
Burn-in	1015, B	160 hour, +125°C, steady-state
Hermeticity Fine Leak Gross Leak	 1014, A1 or A2 1014, C	 5×10^{-7} atm cc/sec bubble test only, preconditioning omitted
Final Electrical	Burr-Brown test procedure	
Final Drift	Burr-Brown test procedure	
External Visual	Burr-Brown QC4118	

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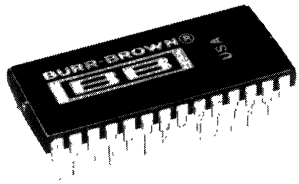


ADS807
ADS808

ADVANCE INFORMATION
SUBJECT TO CHANGE

12-Bit Resolution Sampling A/D Converter

FEATURES

- **COMPLETE WITH REFERENCE, CLOCK AND THREE-STATE OUTPUTS**
- **INTERNAL SAMPLE/HOLD AMPLIFIER**
- **100kHz SAMPLING RATE**
- **PIN COMPATIBLE WITH INDUSTRY STANDARDS: ADC574, ADC674, ADC774 Non-sampling A/D Converters**
- **POWER DISSIPATION: 660mW**
- **PACKAGE: 28-Pin DIP**

DESCRIPTION

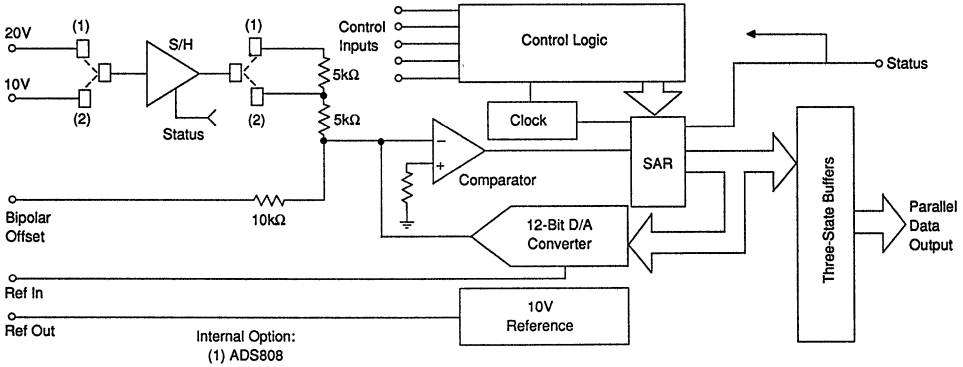
ADS807 and ADS808 are complete 12-bit sampling A/D converters. Each contains a complete ADC774 A/D converter plus an internal sample/hold. They also have an internal buried-zener reference, internal clock, and three-state output drivers. The ADS807/808 are specified at 100kHz sampling rate.

The sample/hold has a 1µs acquisition time to ±0.01% for a 10V input step change. Aperture Time is 25ns and Aperture Uncertainty is 300ps. AC performance is completely specified, Harmonic Distortion, Signal-to-Noise Ratio. 11-bit and 12-bit integral linearity grades are available.

The ADS807, with a full-scale input range of 10V, can be pin-strapped for 0V to +10V or ±5V analog input ranges. The ADS808 has an input range of ±10V.

The ADS807/808 are available in a 28-pin side-braze hermetic double-wide DIP packages and are specified over 0°C to +70°C, and –55°C to +125°C temperature ranges.

The ADS807/808 are excellent high-speed replacements for A/D and sample/hold combinations that use the industry standard 574 pinout.



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SPECIFICATIONS

T_A = +25°C. Sampling Frequency: f_S = 100kHz, $+V_{CC}$ = +15V, $-V_{CC}$ = −15V, V_{DD} = +5V.

	ADS807/808JH[1]			ADS807/808KH			ADS807/808RH			ADS807/808SH			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
RESOLUTION			12			*			*			*	BITS
INPUT													
ANALOG INPUT													
Voltage Range[1]													
ADS807		0 to +10V, ±5V			*			*			*		V
ADS808		±10V			*			*			*		V
Impedance	1	5		*	*		*	*		*	*		MΩ
Bias Current			±400			*			*			*	nA
At T_{MIN} or T_{MAX}			±400			*			*			*	nA
DIGITAL INPUTS (Over Temperature Range)													
Logic Levels (TTL Compatible)													
V_{IL}	−1.0		+0.8	*		*	*		*	*		*	V
V_{IH}	+2.0		+5.5	*		*	*		*	*		*	V
I_{IL} (V_I = +0.4V)	−5			*			*			*			µA
I_{IH} (V_I = +2.7V)			+5			*			*			*	µA
TRANSFER CHARACTERISTICS													
DC ACCURACY													
Full Scale Error[2] [3]			±0.3			*			*			*	%
Change to T_{MIN} or T_{MAX} [5]			±0.5			±0.4			±0.8			±0.6	%
Linearity Error			±0.024			±0.012			±0.024			±0.012	% FSR[4]
T_{MIN} to T_{MAX}			±0.024			±0.012			±0.024			±0.012	% FSR
No Missing Codes Resolution			11			12			11			12	Bits
T_{MIN} to T_{MAX}			11			12			11			12	Bits
Unipolar Zero			±3			±2			±3			±2	LSB
Bipolar Zero			±10			±5			±10			±5	LSB
AC CHARACTERISTICS													
In-Band Harmonics & Spurious Noise													
f = DC to 100kHz (0dB)		−77			−80			−77			−80		dBC
Two-tone Intermodulation Distortion													
f1 = 46.5kHz (−6dB)		−75			−78			−75			−78		dBC
f2 = 48.8kHz (−6dB)													
Signal to Noise and Distortion Ratio		68			70			68			70		dB
SAMPLING DYNAMICS													
Aperture Delay		25			*			*			*		ns
Aperture Uncertainty(Jitter)		300			*			*			*		ps, rms
REFERENCE OUTPUT													
Voltage	9.9	10.0	10.1	*	*	*	*	*	*	*	*	*	V
Source Current Available for External Loads (18)	2			*			*			*			mA
DIGITAL TIMING (Over Temperature)													
T_{HRL} Low R/$\overline{C}$ Pulse Width	50			*			*			*			ns
T_{DS} Status Delay from R/$\overline{C}$			200			*			*			*	ns
T_{HDR} Data Valid after R/$\overline{C}$ Low	25			*			*			*			ns
T_{HS} Status Delay after Data Valid	100	200	400	*	*	*	*	*	*	*	*	*	ns
T_{HRH} High R/$\overline{C}$ Pulse Width	150			*			*			*			ns
T_{DDR} Data Access Time			150			*			*			*	ns

ELECTRICAL SPECIFICATIONS (CONT)

T_A = +25°C. Sampling Frequency: f_S = 100kHz, $+V_{CC}$ = +15V, $-V_{CC}$ = −15V, V_{DD} = +5V.

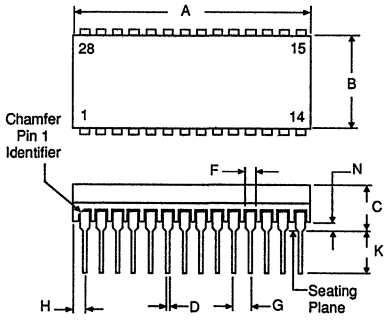
	ADS807/808JH[1]			ADS807/808KH			ADS807/808RH			ADS807/808SH			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL OUTPUTS (Over Temperature)													
Format		Parallel		*			*			*			
Coding		Bipolar Offset Binary (BOB)		*			*			*			
Logic Levels (3-state output, TTL compatible)													
V_{OL} (I_{SINK} = 1.6mA)	0.0		+0.4	*		*	*		*	*		*	V
V_{OH} (I_{SOURCE} = 500µA)	+2.4		+5.0	*		*	*		*	*		*	V
$I_{LEAKAGE}$ (High Z State)	−5	−0.1		+5	*	*	*	*	*	*	*	*	µA
POWER SUPPLIES													
Rated Voltage													
$+V_{CC}$	+14.5	+15	+16	*	*	*	*	*	*	*	*	*	V
$-V_{CC}$	−14.5	−15	−16	*	*	*	*	*	*	*	*	*	V
V_{DD}	+4.75	+5.0	+5.25	*	*	*	*	*	*	*	*	*	V
Current[6]													
$+V_{CC}$		15	18		*	*		*	*		*	*	mA
$-V_{CC}$		26	33		*	*		*	*		*	*	mA
V_{DD}		9	15		*	*		*	*		*	*	mA
Power Consumption		660	850		*	*		*	*		*	*	mW
TEMPERATURE RANGE													
Specification	0		+70	*		*	*		*	*		*	°C
Storage	−65		+150	*		*	*		*	*		*	°C

*Specifications same as ADS807/808JH.

NOTES: (1) ADS807: For input ranges −5V to +5V, 0 to +10V. ADS808: For input range ±10V. (2) Adjustable to zero with external potentiometer. (3) Specifications assume a fixed 50Ω resistor between Ref Out (Pin 8) and Ref In (Pin 10). Full Scale Error is the difference between the ideal and the actual input voltage at which the digital output makes a transition from FFE_{16} to FFF_{16}. Ideally this transition point should occur at an analog input voltage 1−1/2 LSB below the nominal full scale voltage. (4) FSR means Full Scale Range. For ADS807, FSR = 10V; for ADS808 FSR = 20V. (5) Change specifications for unipolar offset, bipolar zero and full-scale error correspond to the change from the initial value (at 25°C) to the value at T_{MIN} or T_{MAX}. (6) Max supply current is specified at rated supply voltages.

MECHANICAL

H Package — 28-Pin Ceramic DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	.610 BASIC		15.49 BASIC	
C	.160	.205	4.06	5.21
D	.015	.019	0.38	0.48
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.055	.095	1.40	2.41
J	.009	.012	0.23	0.30
K	.155	.195	3.94	4.95
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

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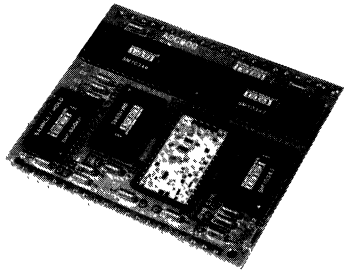


ADC600

12-BIT ULTRA-HIGH SPEED A/D CONVERTER

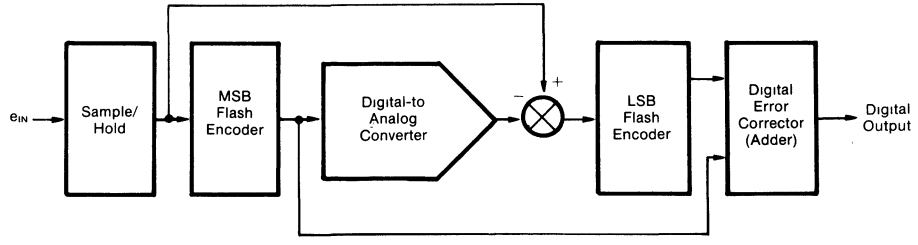
FEATURES

- HIGH RESOLUTION: 12 bits
- SAMPLE RATE: DC to 10MHz
- HIGH SINAD RATIO: 67dB
- LOW HARMONIC DISTORTION: −71dB
- LOW INTERMODULATION DISTORTION: −70dB
- INPUT RANGE: ±1.25V
- COMPLETE SUBSYSTEM: Contains Sample/Hold and Reference
- LOW DISSIPATION: 8.5W
- 0°C TO +70°C AND −25°C TO +85°C
- DIGITAL SIGNAL PROCESSING
- RADAR SIGNAL ANALYSIS
- TRANSIENT SIGNAL RECORDING
- FFT SPECTRUM ANALYSIS
- HIGH-SPEED DATA ACQUISITION
- JAM-RESISTANT SYSTEMS
- SIGINT, ECM, AND EW SYSTEMS
- DIGITAL COMMUNICATIONS
- DIGITAL OSCILLOSCOPES

DESCRIPTION

The ADC600 is an ultra-high speed analog-to-digital converter capable of digitizing signals at any rate from DC to 10 megasamples per second. Outstanding dynamic range has been achieved by minimizing noise and distortion.

The ADC600 is a two-step subranging ADC subsystem containing an ADC, sample/hold amplifier, voltage reference, timing, and error-correction circuitry. Laser-trimmed ceramic submodules are mounted on a 17-square-inch multilayer PC motherboard. Logic is ECL.



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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, 10MHz sampling rate, R_S = 50Ω, $\pm V_{CC}$ = 15V, V_{DD1} = +5V, V_{DD2} = −5.2V, and 15-minute warmup in normal convection environment, unless otherwise noted

PARAMETER	CONDITIONS	ADC600K MIN	ADC600K TYP	ADC600K MAX	ADC600B MIN	ADC600B TYP	ADC600B MAX	UNITS
RESOLUTION				12			*	Bits
INPUTS								
ANALOG								
Input Range	Full scale	−1.25		+1.25	*		*	V
Input Impedance			1.5			*		MΩ
Input Capacitance			5			*		pF
DIGITAL								
Logic Family			ECL 10k-Compatible			*		
Convert Command			Negative Edge			*		
Pulse Width		10			*			ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	F = 200Hz		±0.1	±0.5		*	*	% FSR
Input Offset	DC		±0.1	±0.5		*	*	% FSR[1]
Integral Linearity Error	F = 200Hz			1.25			*	LSB
Differential Linearity Error	F = 200Hz. 68.3% of all codes			0.25			*	LSB
	99.7% of all codes			1.00			*	LSB
	100% of all codes			+1.25			*	LSB
				−1.00			*	LSB
Missing Codes				none			*	
CONVERSION CHARACTERISTICS								
Sample Rate		DC		10M	*		*	Samples/s
Conversion Time	First conversion	115	150	160	*	*	*	ns
DYNAMIC CHARACTERISTICS								
Differential Linearity Error	F = 4.9MHz 68.3% of all codes			0.5			*	LSB
	99.7% of all codes			1.5			*	LSB
	100% of all codes			2.0			*	LSB
Total Harmonic Distortion[2]								
F = 4.8MHz (0dB)	F_S = 10MHz		−71			*		dBC[3]
F = 0.58MHz (0dB)			−74			*		dBC
F = 2.4MHz (0dB)	F_S = 5MHz		−73			*		dBC
F = 0.58MHz (0dB)			−74.5			*		dBC
Two-Tone Intermodulation Distortion[2][4]								
F = 4.88MHz (−6dB)	F_S = 10MHz		−70.5			*		dBC
4.65MHz (−6dB)								
F = 2.40MHz (−6dB)	F_S = 5MHz		−74.5			*		dBC
2.25MHz (−6dB)								
Signal-to-Noise and Distortion (SINAD) Ratio								
F = 4.8MHz (0dB)	F_S = 10MHz		66.8			*		dB
F = 0.58MHz (0dB)			68.6			*		dB
F = 2.4MHz (0dB)	F_S = 5MHz		67.2			*		dB
F = 0.58MHz (0dB)			69			*		dB
Aperture Time			6			*		ns
Aperture Jitter			5			*		ps RMS
Analog Input Bandwidth								
Small Signal	−20dB input		70			*		MHz
Full Power	0dB input		40			*		MHz
OUTPUTS								
Logic Family			ECL with pull-down to $-V_{DD2}$ (see text)					
Logic Coding			Offset Binary, Twos Complement					
Logic Levels	Logic "LO"		−1.7			*		V
	Logic "HI"		−0.9			*		V
EOC Delay Time	Data Out to DV	5	35		*	*		ns
Tr and Tf	20% to 80%		5			*		ns
Data Valid Pulse Width	50%	5	8		*	*		ns
POWER SUPPLY REQUIREMENTS								
Supply Voltages $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		−14.25	−15	−15.75	*	*	*	V
V_{DD1}		+4.75	+5	+5.25	*	*	*	V
V_{DD2}		−4.95	−5.2	−5.46	*	*	*	V
Supply Currents $+V_{CC}$	Operating		75			*		mA
$-V_{CC}$			45			*		mA
V_{DD1}			400			*		mA
V_{DD2}			900			*		mA
Power Consumption	Operating		8.5			*		W

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

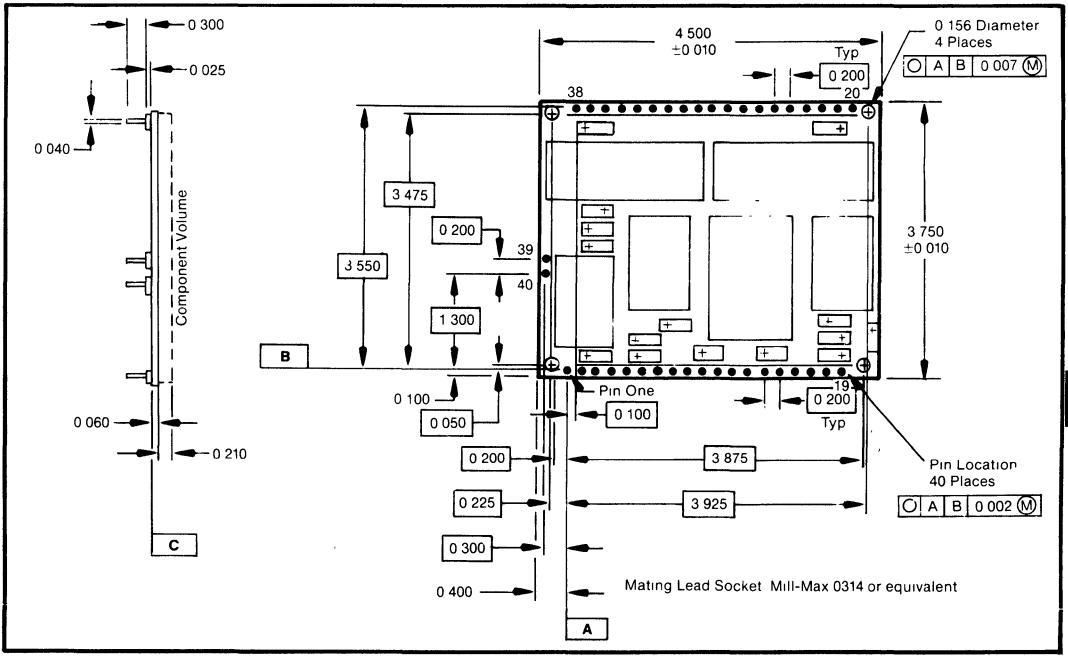
$\pm V_{CC}$ = 15V, V_{DD1} = +5V, V_{DD2} = −5 2V, R_S = 50Ω, 15-minute warmup, and $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted

PARAMETER	CONDITIONS	ADC600K MIN	ADC600K TYP	ADC600K MAX	ADC600B MIN	ADC600B TYP	ADC600B MAX	UNITS
TEMPERATURE RANGE								
Specification	T_{CASE} max	0		+70	−25		+85	°C
Storage	$T_{AMBIENT}$	−40		+100	*		*	°C
ACCURACY								
Gain Error	F - 200Hz		±30			*		ppm/°C
Input Offset	DC		±50			*		µV/°C
Integral Linearity Error	F 200Hz			1 5			*	LSB
Differential Linearity Error	F 200Hz							
	63% of all codes			0 5			*	LSB
	98% of all codes			1 25			*	LSB
	100% of all codes			1 5			*	LSB
Sample Rate		DC		10	*		*	MHz

*Same as ADC600K

NOTE (1) FSR full-scale range 2 5Vp-p (2) Units with tested and guaranteed distortion specifications are available on special order—inquire (3) dBC level referred to carrier (input signal ≈ 0dB), F = input signal frequency, F_S = sampling frequency (4) IMD is referred to the larger of the two input test signals If referred to the peak envelope signal (≈ 0dB), the intermodulation products will be 6dB lower

MECHANICAL



ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±16 5V
V_{DD1}	+7 0V
V_{DD2}	−7 0V
Analog Input	±5 0V
Logic Input	V_{DD2} to +0 5V
Case Temperature	100°C
Junction Temperature(1)	150°C
Storage Temperature	−40°C to +100°C

Stresses above these ratings may cause permanent damage to the device

(1) See Table I for thermal resistance data

ORDERING INFORMATION

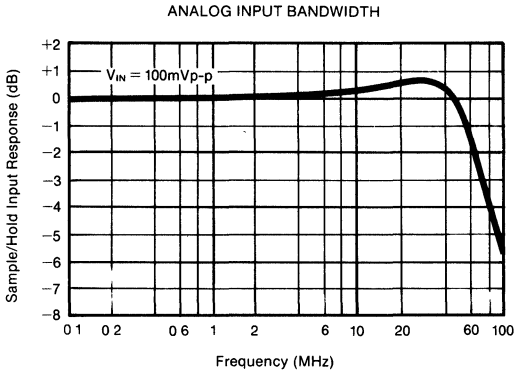
ADC600 X Q

- Basic Model Number
- Performance Grade Code
  - K = 0°C to +70°C
  - B = −25°C to +85°C
- Reliability Screening
  - Q = Q-Screened

PIN ASSIGNMENTS

1	Common	21	Common
2	$-V_{CC}$ (−15V)	22	Data Valid
3	V_{DD2} (−5.2V)	23	Bit 12 (LSB)
4	V_{DD1} (+5V)	24	Bit 11
5	$+V_{CC}$ (+15V)	25	Bit 10
6	Common	26	Bit 9
7	V_{DD2} (−5.2V)	27	Bit 8
8	V_{DD1} (+5V)	28	Bit 7
9	Common	29	Bit 6
10	V_{DD2} (−5.2V)	30	Bit 5
11	Common	31	Bit 4
12	Common	32	Bit 3
13	$+V_{CC}$ (+15V)	33	Bit 2
14	$-V_{CC}$ (−15V)	34	Bit 1 (MSB)
15	V_{DD2} (−5.2V)	35	$\overline{\text{Bit 1}}$ ($\overline{\text{MSB}}$)
16	V_{DD1} (+5V)	36	V_{DD2} (−5.2V)
17	Common	37	Common
18	V_{DD2} (−5.2V)	38	Convert Command
19	V_{DD1} (+5V)	39	Analog Input
20	V_{DD2} (−5.2V)	40	Analog Input Return

TYPICAL PERFORMANCE CURVE



THEORY OF OPERATION

The ADC600 is a two-step subranging analog-to-digital converter. This architecture is shown in Figure 1. The major system building blocks are: Sample/Hold Amplifier, MSB Flash encoder, DAC and Error Amplifier, LSB Flash Encoder, Digital Error Corrector, and Timing Circuits. The ADC600 uses individually tested and laser-trimmed submodules mounted on a four-layer motherboard to integrate this complex circuit into a complete analog-to-digital converter subsystem with state-of-the-art performance.

Conceptually, the subranging technique is simple: sample and hold the input signal, convert to digital with a coarse ADC, convert back to analog with a coarse-resolution (but high-accuracy) DAC, subtract this voltage from the S/H output, amplify this "remainder," convert to digital with a second coarse ADC, and combine the digital output from the first ADC (MSB) with the digital output from the second ADC (LSB). In practice, however, achieving high conversion speed without sacrificing accuracy is a difficult task.

The analog input signal is sampled by a high-speed sample/hold amplifier with low distortion, fast acquisition time and very low aperture uncertainty (jitter). A diode bridge sampling switch is used to achieve an acceptable compromise between speed and accuracy. The diode bridge switching transients are buffered from the analog input by a high input impedance buffer amplifier. Since the hold capacitor does not appear in the feedback of the diode bridge output buffer the capacitor can acquire the signal in 25ns. The low-bias-current output buffer is then required to settle to only the resolution (7 bits) of the first (MSB) flash encoder in 25ns while an additional 60ns is allowed for settling to the resolution (12 bits) of the second (LSB) flash encoder. Sample/hold droop appears as only an offset error and does not affect linearity.

Both the MSB and the LSB flash encoder (ADC) are high-speed 7-bit resolution converters formed by parallel-connecting two 6-bit flash ADCs as shown in Figure 2. The DAC +10V reference is also used to generate reference voltages for the MSB and LSB encoders to compensate drift errors. Buffering and scaling are performed by I_{C1} and I_{C2}. Laser-trimming is used to minimize voltage offset errors and optimize gain (input full-scale range) symmetry.

The subtraction DAC is an ECL 7-bit resolution DAC with 14-bit accuracy. Laser-trimmed thin-film nichrome resistors on sapphire and high-speed bipolar circuitry allow the DAC output to settle to 14-bit accuracy in only 25ns.

A "remainder" or coarse conversion-error voltage is generated by resistively subtracting the DAC output from the output of the sample/hold amplifier. Before the second (LSB) conversion, the "remainder" is amplified by a wideband fast-settling amplifier with a gain of 32V/V. To prevent overload on large amplitude transients, a high-speed FET switch blanks the amplifier input from the beginning of the S/H acquisition time to end of the MSB encoder update time.

The timing circuits shown in Figure 3 supply all the critical timing signals necessary for proper operation of the ADC600. Some noncritical timing signals are also generated in the digital error correction circuitry. Timing signals are laser-trimmed for both pulse width and delay. The ECL logic timing delay is stable over a wide range of temperatures and power supply voltages. Basic timing is derived from the output of a three-stage shift register driven by a synchronized 20MHz oscillator.

The convert command pulse is differentiated by IC_1 to allow triggering by pulses from as narrow as 5ns to as wide as 75% duty cycle. This differentiated signal sets flip-flop IC_2, placing the S/H back into its sample mode.

The output of the third stage of the shift register is also differentiated by IC_8 and used to generate a strobe for the LSB flash encoder. R_1 is laser-trimmed to generate a precise 8ns pulse while the oscillator frequency is adjusted to trim the strobe pulse delay. IC_4 and IC_5 comprise the

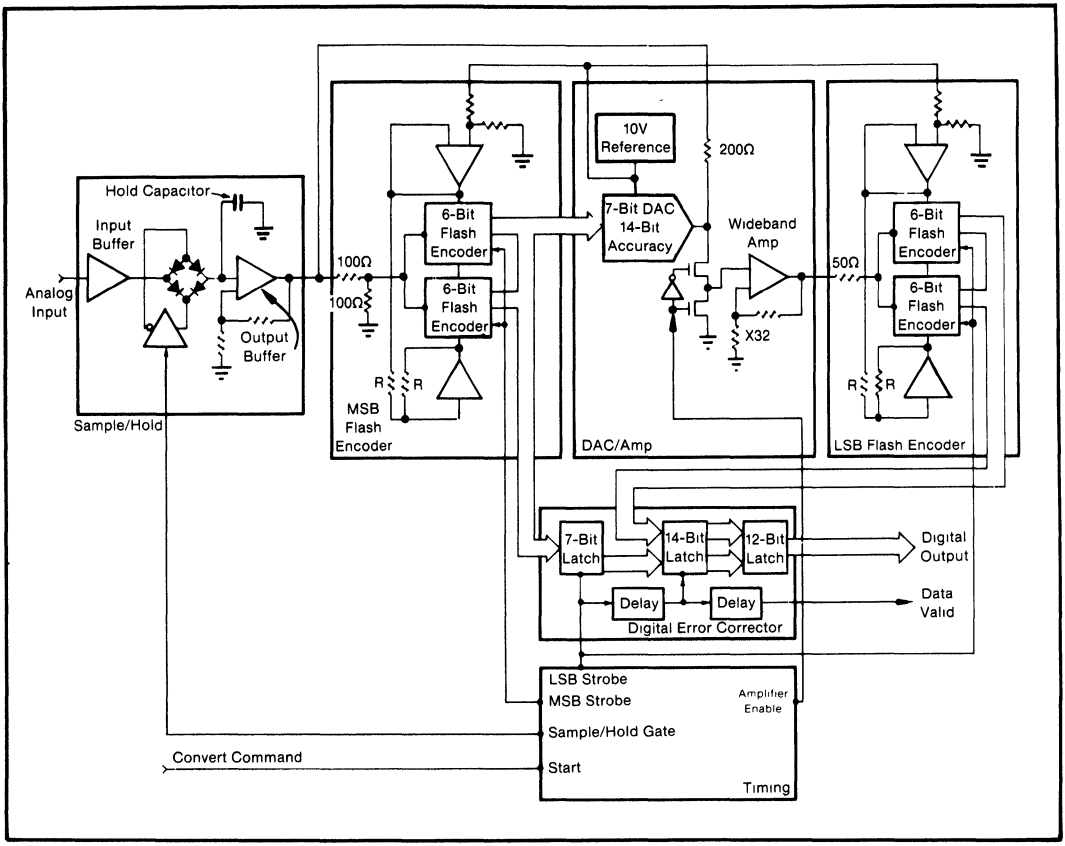


Figure 2. Block Diagram of the 12-Bit 10MHz ADC600.

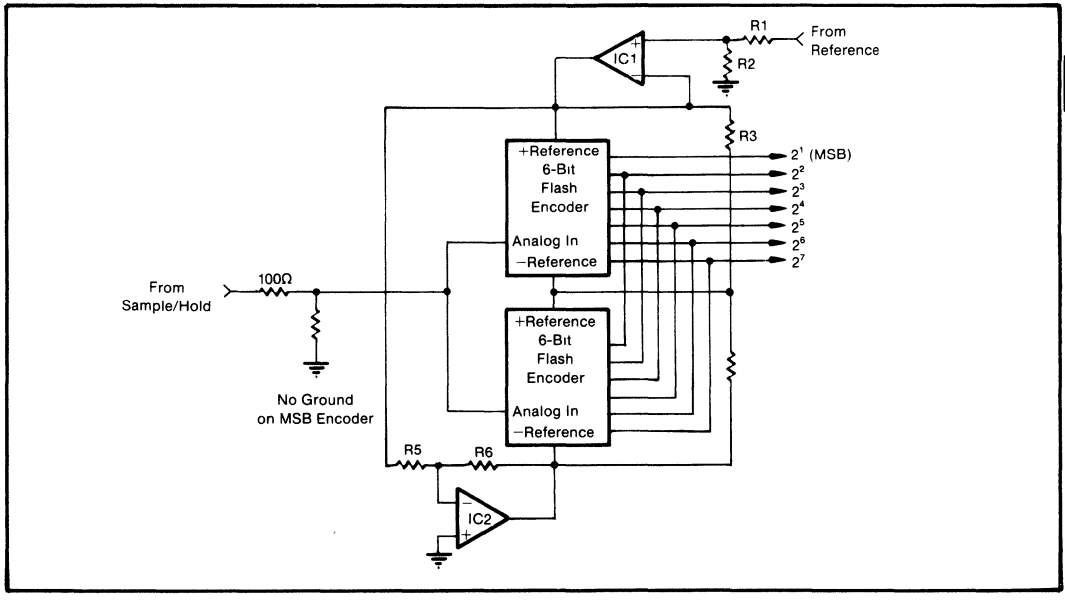


Figure 3. 7-Bit Flash Encoder.

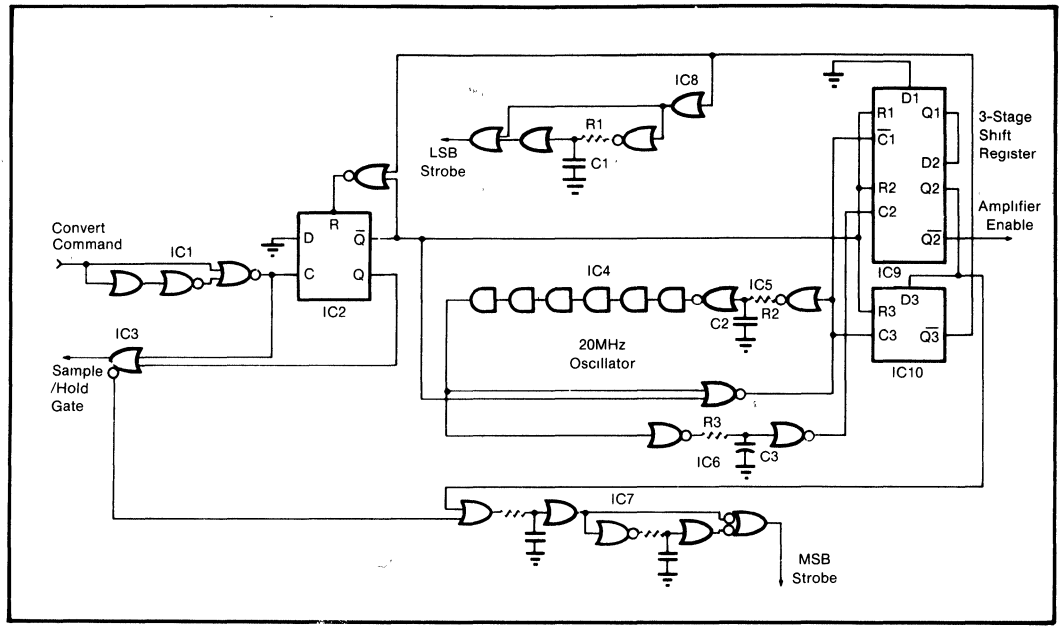


FIGURE 3. Schematic of Timing Module.

principal elements of a 20MHz ring oscillator. R_2 and C_2 add additional delay and allow laser-trimming for the LSB delay. A blanking pulse to prevent error amplifier overload is generated by the second stage of the shift register. Proper timing is generated by laser-trimming R_3 which, along with C_3 forms a delay element along with two gates of IC_6.

A strobe pulse of the MSB flash encoder is generated and trimmed in a similar circuit using IC_7. This technique generates a variable width S/H gate pulse which is determined by the conversion command pulse period minus the fixed 67ns ADC conversion time ADC600 conversion rates are therefore possible above the 10MHz specification but S/H acquisition time is sacrificed and accuracy is rapidly degraded.

The output of the MSB encoder is read into a separate 7-bit latch at the same time the LSB encoder is being strobed. The latched MSB data, along with the LSB data, is then read into a 14-bit latch 30ns after the leading edge of the LSB strobe and before being applied to the adder, where the actual error correction takes place. This latch eliminates any critical timing problems that would result when the converter is operated at the maximum conversion rate.

The function of the digital error correction circuitry (Figure 4) is to assemble the 7-bit words from the two flash encoders into a 12-bit output word. In addition, the circuit uses the LSB flash encoder strobe to generate timing strobes for both data registers. A data valid (DV) pulse is also generated which is used to indicate when output data can be latched into an external register. This DV pulse is delayed 5ns after the output data has settled to allow a sufficient set-up time for an external ECL data latch.

The 14-bit register output is then sent to a 12-bit adder where the final data output word is created. The MSB data forms the most significant seven bits of a 12-bit word, with the last five bits being assigned zeros. In a similar fashion, the LSB data from the least significant bits form the other input to the adder with the first five bits being assigned zeros. As two 12-bit words are being added, the output of the adder could exceed 12 bits in range; however, the final data output is only a 12-bit word, so a means of detecting an overrange is included.

To prevent reading erroneous data, the converter data output reads all ones for a full-scale positive input or overrange and reads all zeros for a negative full-scale input or overrange. The data output does not "roll-over" if the converter input exceeds its specified full-scale range of ±1.25V.

DISCUSSION OF PERFORMANCE

DYNAMIC PERFORMANCE TESTING

The ADC600 is a very high performance converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a Fast Fourier Transform (FFT) to the ADC digitial output will provide data on all important dynamic performance parameters: total harmonic distortion (THD), signal-to-noise raito (SNR) or the more severe signal-to-noise-and-distortion ratio (SINAD), total noise and distortion (TND), and intermodulation distortion (IMD).

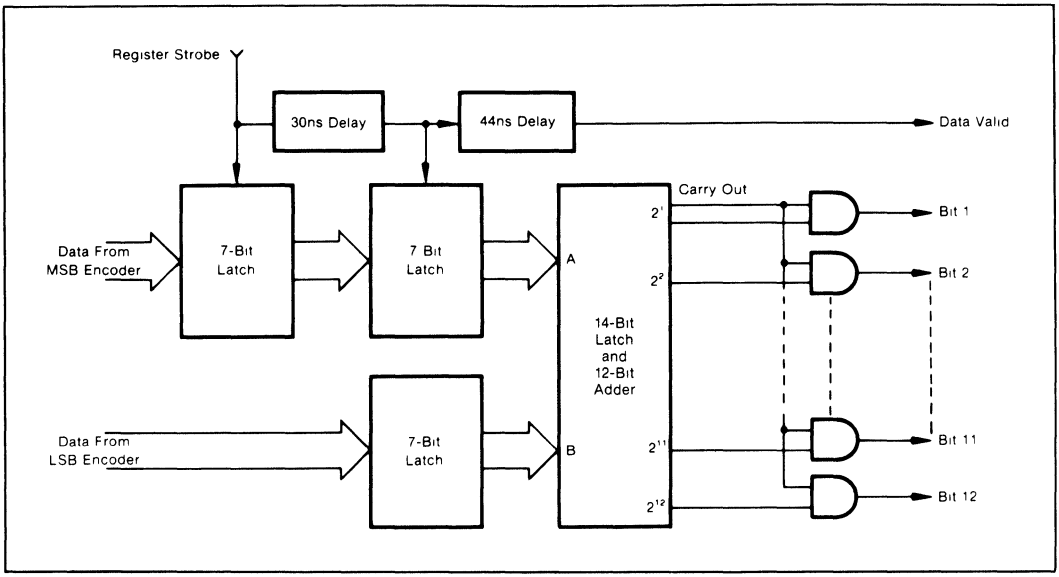


FIGURE 4. Block Diagram of Digital Error Corrector.

A test setup for performing high-speed FFT testing of analog-to-digital converters is shown in Figure 5. This was used to generate the typical FFT performance curves shown on pages 10 through 13.

To preserve measurement accuracy, a very low side-lobe window must be applied to the digital data before executing an FFT. A commonly used window such as the Hanning window is not appropriate for testing high performance converters; a minimum four-sample Blackman-Harris window is strongly recommended.[1] To assure that the majority of codes are exercised in the ADC600 (12 bits), a ten-sample average of 512-point FFTs is taken.

Dynamic Performance Definitions

1. Signal-to-Noise-and-Distortion[2] Ratio (SINAD):

$$10 \log \frac{\text{sine wave signal power}}{\text{noise + harmonic power}}$$

2. Total Harmonic Distortion (THD):

$$10 \log \frac{\text{harmonic power (first nine harmonics)}}{\text{sinewave signal power}}$$

3. Total Noise Distortion (TND):

$$10 \log \frac{\text{noise power}}{\text{sinewave signal power}}$$

4. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{IMD product power}}{\text{sinewave signal power}}$$

IMD is referenced[3] to the larger of the test signals f_1 or f_2.

Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The "0" frequency bin (DC) is not included in these calculations as it is of little importance in dynamic signal processing applications.

Attention to test set-up details can prevent errors that contribute to poor test results. Important points to remember when testing high performance converters are:

1. The ADC analog input must not be overdriven. Using a signal amplitude slightly lower than FSR will allow a small amount of "headroom" so that noise will not overrange the ADC and "hard limit" on signal peaks.
2. Two-tone tests can produce signal envelopes that exceed FSR. Set each test signal to slightly less than −6dB to prevent "hard limiting" on peaks.
3. Low-pass filtering (or bandpass filtering) of test signal generators is absolutely necessary for THD and IMD tests. An easily built LC low-pass filter (Figure 6) will eliminate harmonics from the test signal generator.
4. Test signal generators must have exceptional noise performance (better than −155dBC) to achieve accurate SNR measurements[4]. Good generators together with fifth-order elliptical bandpass filters are recommended for SNR and SINAD tests.
5. The analog input of the ADC600 should be terminated directly at the input pin sockets with the correct filter terminating impedance (50Ω or 75Ω) or it should be driven by an OPA600 buffer. Short leads are necessary to prevent digital noise pickup.
6. A low-noise (jitter) clock signal (convert command) generator is required for good ADC dynamic performance. A recommended interface circuit is shown in Figure 7. Short leads are necessary to preserve fast ECL rise times.
7. Two-tone testing will require isolation between test signal generators to prevent IMD generation in the test generator output circuits. An active summing amplifier using an OPA600 is shown in Figure 8. This circuit will provide excellent performance from DC to

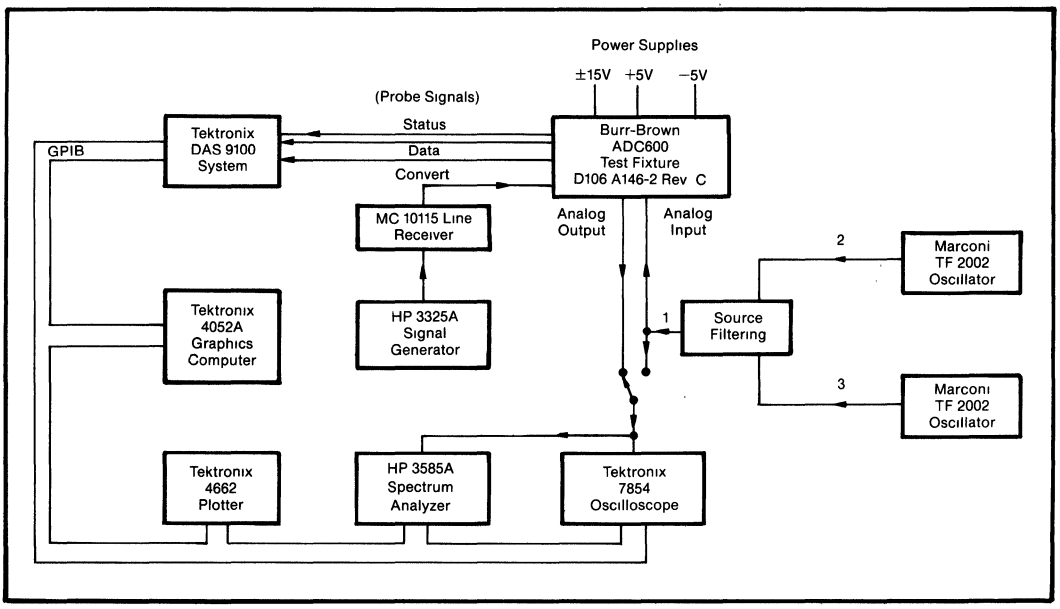


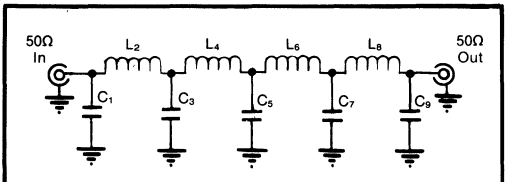
FIGURE 5. Test Setup for High Speed FFT Testing.

5MHz with harmonic and intermodulation distortion products typically better than −70dBC. A passive hybrid transformer signal combiner can also be used (Figure 9) over a range of about 1MHz to 30MHz. The port-to-port isolation will be ≈ 45dB between signal generators and the input-output insertion loss will be ≈ 6dB.

8. A very low side-lobe window must be used for FFT calculation. A minimum four-sample Blackman-Harris window function is recommended.[1]
9. Digital data must be latched into an external ECL 12-bit register only by the Data Valid output pulse. Due to the possibility of improper timing, output data **cannot** be latched by using the convert command!
10. Do not overload the data output logic. These outputs are already provided with internal 680Ω pull-down resistors tied to −5.2V.
11. A well-designed, clean PC board layout will assure proper operation and clean spectral response[5][6]. Proper grounding and bypassing, short lead lengths and separation of analog and digital signals and ground returns are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance, but a two-sided PC board with large, heavy (2oz-foil) ground planes can give excellent results, if carefully designed.

    Prototyping "plug-boards" or wire-wrap boards will not be satisfactory.

NOTES.
1. *On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform*, Fredric J Harris Proceedings of the IEEE, Vol 66, No 1, January 1978, pp 51-83
2. SINAD test includes harmonics whereas SNR does not include these important spurious products
3. If IMD is referenced to peak envelope power, an improvement of 6dB
4. *Test Report FFT Characterization of Burr-Brown ADC600K*, Signal Conversion Ltd., Swansea, Wales, U K
5. MECL System Design Handbook, 3rd Edition, Motorola Corp
6. Motorola MECL, Motorola Corp.



9th Order 0.5dB Ripple
Tchebychev Low-Pass Filter

Attenuation at 2× cutoff frequency = 90dB

Cutoff frequency = −3dB frequency, to convert cutoff frequency to −0.5dB frequency, multiply all LC values by 0.9897

Cutoff Freq. (MHz)	C_1 (pF)	C_3 (pF)	C_5 (pF)	C_7 (pF)	C_9 (pF)	L_2 (μH)	L_4 (μH)	L_6 (μH)	L_8 (μH)
5.0	1134.6	1729.2	1765.6	1729.2	1134.6	2.056	2.216	2.216	2.056
2.5	2269	3458	3531	3458	2269	4.11	4.43	4.43	4.11
1.25	4538	6917	7062	6917	4538	8.23	8.86	8.86	8.23
0.625	9077	13,833	14,125	13,833	9077	16.45	17.73	17.73	16.45

FIGURE 6. Ninth-Order Harmonic Filter.

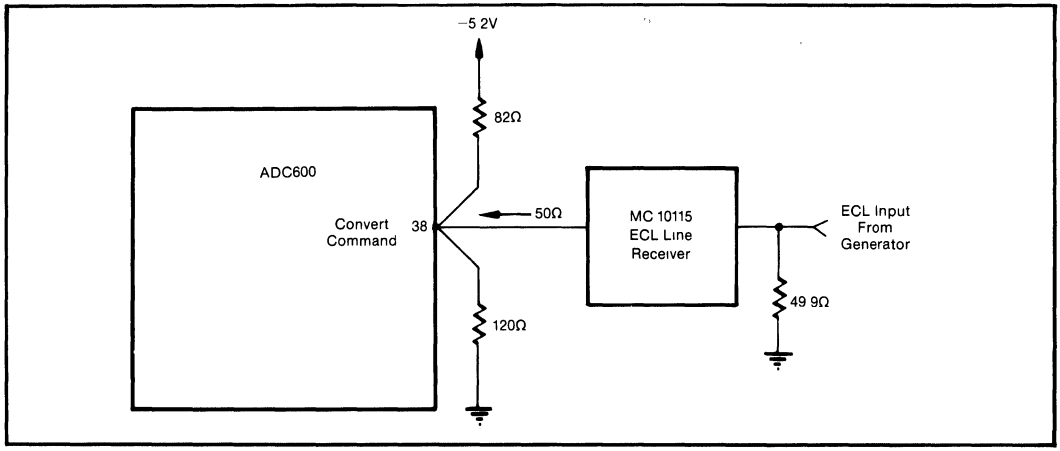


FIGURE 7. Optional Convert Command Interface Circuit.

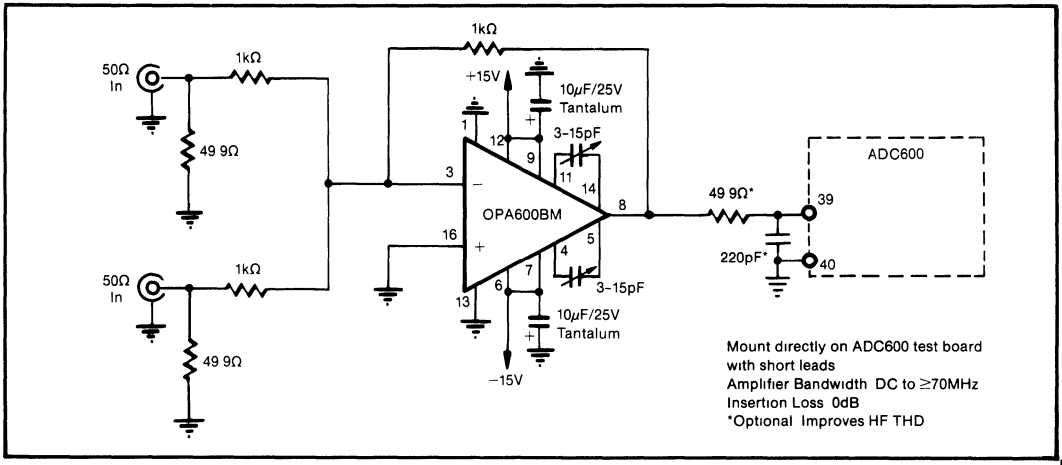


FIGURE 8. Active Signal Combiner.

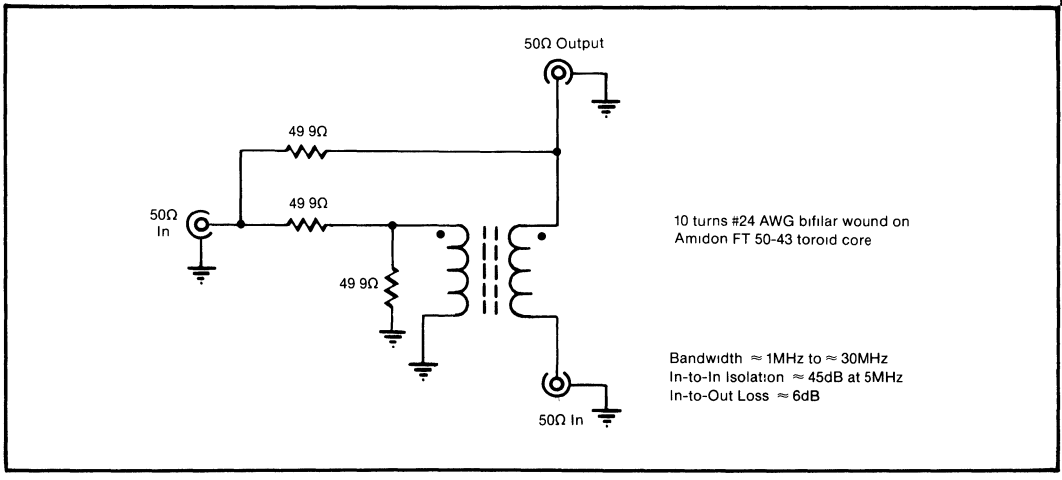
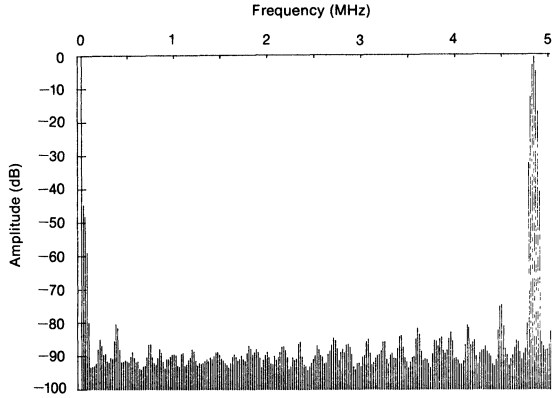


FIGURE 9. Passive Signal Combiner.

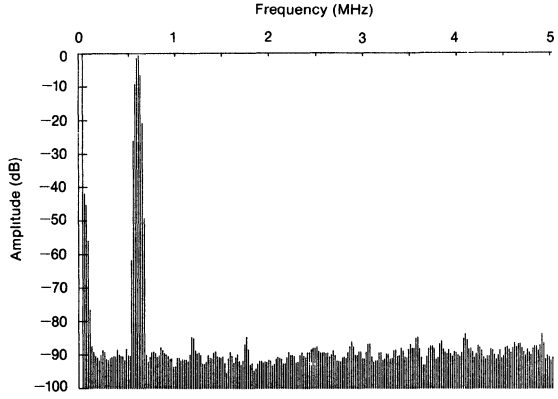
TYPICAL FFT SPECTRAL PERFORMANCE

All FFT data 512-point FFT, 10-sample average; minimum 4-sample Blackman-Harris Window

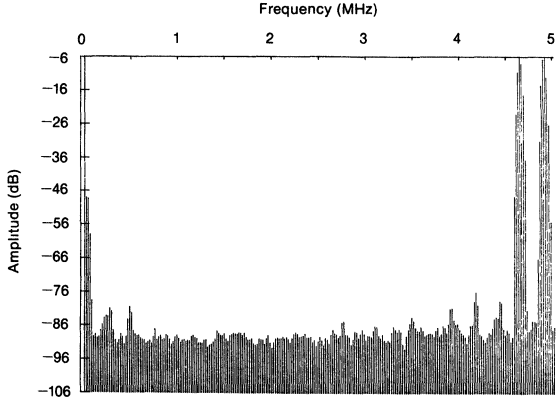
Sample Rate = 10MHz, Input Voltage = Full-Scale (0dB)



	Level re Full-Scale (dB)
4 8438MHz Fundamental	−0 7
Harmonics 2f	−80 5
3f	−74 7
4f	−86 6
SINAD	67 2dB
TND	−69 5dBC
THD	−71 0dBC



	Level re Full-Scale (dB)
0 6055MHz Fundamental	−0 6
Harmonics 2f	−84 7
3f	−84 6
4f	−87 5
SINAD	69 6dB
TND	−70 7dBC
THD	−76 4dBC

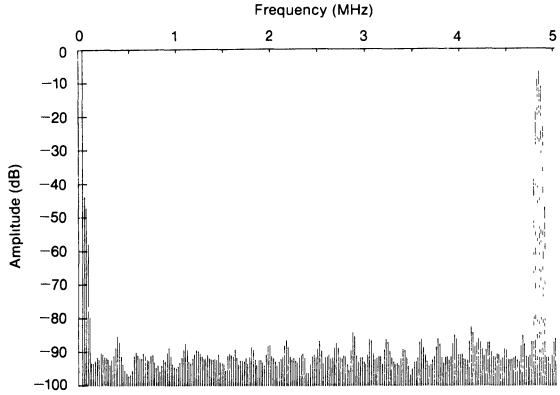


	Level re Full-Scale (dB)
F_1 4 9219MHz	−6.3
F_2 4 6484MHz	−6 3
Peak Envelope	−0 6
IMD 0 4883MHz	−80.8
4 1797MHz	−76 3
4 4336MHz	−78.9

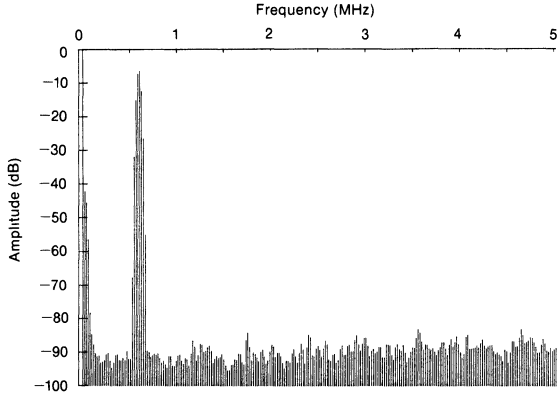
TYPICAL FFT SPECTRAL PERFORMANCE (CONT)

All FFT data 512-point FFT, 10-sample average, minimum 4-sample Blackman-Harris Window

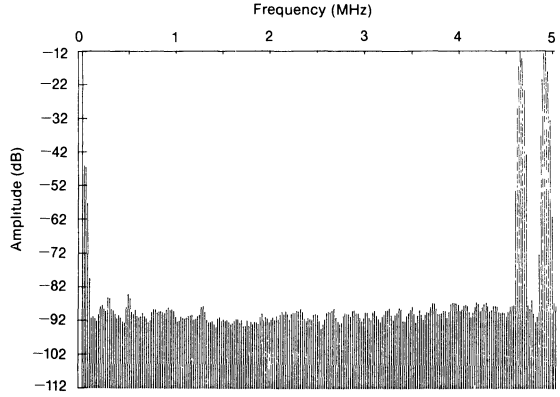
Sample Rate = 10MHz, Input Voltage = Half-Scale (−6dB)



	Level re Full-Scale (dB)
4 8438MHz Fundamental	−6 8
Harmonics 2f	−85 4
3f	−89 1
4f	−90 1
SINAD	64 0dB
TND	−65.2dBC
THD	−70.2dBC



	Level re Full-Scale (dB)
0 6055MHz Fundamental	−6 5
Harmonics 2f	−86 6
3f	−84 2
4f	−84 9
SINAD	63 7dB
TND	−65 1dBC
THD	−69 2dBC

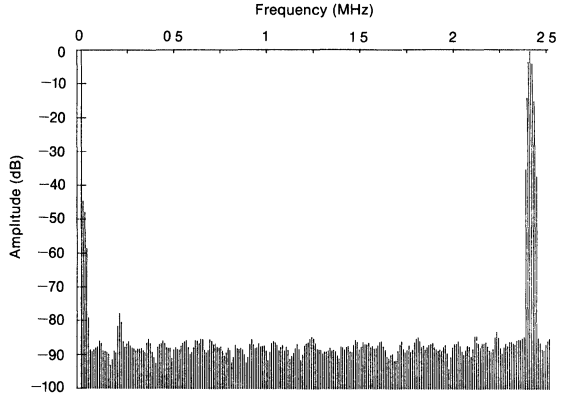


	Level re Full-Scale (dB)
F_1 4 9219MHz	−12 35
F_2 4 6484MHz	−12 45
Peak Envelope	−6.7
IMD 0 2734MHz	−85 5
0 4883MHz	−84 5
4 7656MHz	−86 3

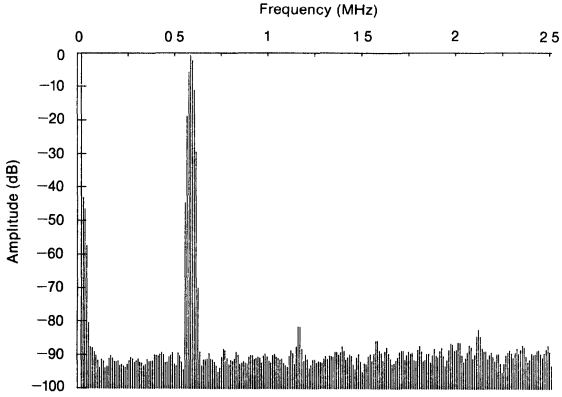
TYPICAL FFT SPECTRAL PERFORMANCE (CONT)

All FFT data 512-point FFT, 10-sample average, minimum 4-sample Blackman-Harris Window.

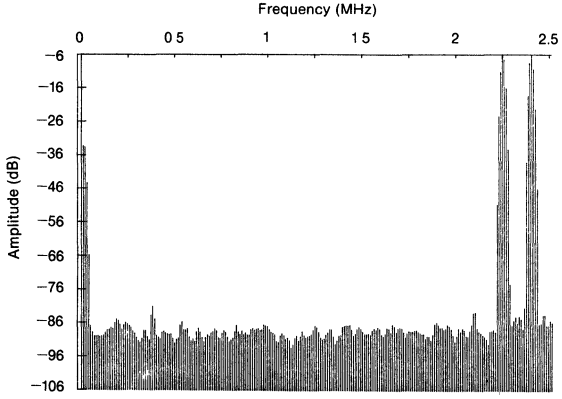
Sample Rate = 5MHz, Input Voltage = Full-Scale (0dB)



	Level re Full-Scale (dB)
2 4121MHz Fundamental	−0 6
Harmonics 2f	−77 9
3f	−83 1
4f	−85 3
SINAD	67 3dB
TND	−68 5dBC
THD	−73 3dBC



	Level re Full-Scale (dB)
0 5859MHz Fundamental	−0 7
Harmonics 2f	−81 4
3f	−87 2
4f	−87 0
SINAD	69 6dB
TND	−70 7dBC
THD	−76.1dBC

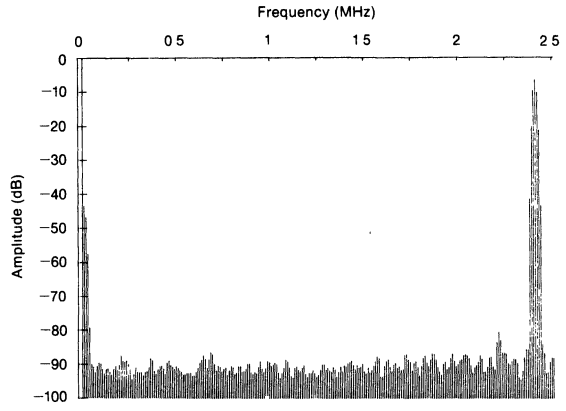


	Level re Full-Scale (dB)
F_1 2 2461MHz	−6 3
F_2 2 4023MHz	−6 4
Peak Envelope	−0 7
IMD 0 3809MHz	−81 2
2 0996MHz	−82 9
2 4707MHz	−83 9

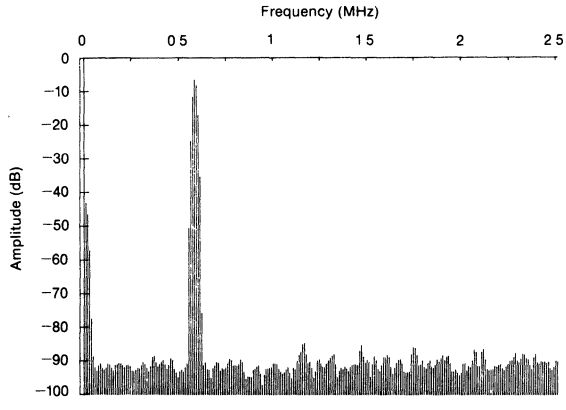
TYPICAL FFT SPECTRAL PERFORMANCE (CONT)

All FFT data 512-point FFT, 10-sample average, minimum 4-sample Blackman-Harris Window

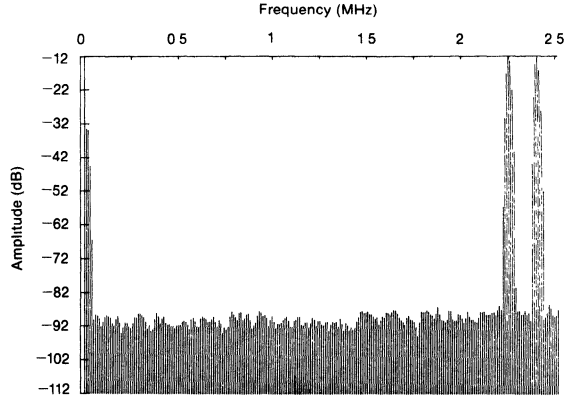
Sample Rate = 5MHz, Input Voltage = Half-Scale (−6dB)



	Level re Full-Scale (dB)
2 4121MHz Fundamental =	−6 6
Harmonics 2f =	−87 6
3f =	−80 4
4f =	−88 3
SINAD =	64 3dB
TND =	−65 7dBC
THD =	−69 9dBC



	Level re Full-Scale (dB)
0 5859MHz Fundamental =	−6.6
Harmonics 2f =	−84 6
3f =	−85 9
4f =	−87 8
SINAD =	64 8dB
TND =	−65 9dBC
THD =	−71 3dBC



	Level re Full-Scale (dB)
F_1: 2.2461MHz =	−12 4
F_2: 2.4023MHz =	−12.4
Peak Envelope =	−6.8
IMD: 1.6406MHz =	−87 5
1 8750MHz =	−86.7
2.4609MHz =	−86.0

DIGITIZING INPUT WAVEFORMS

The response of the ADC600 is illustrated by the digitized waveforms of Figure 10. The 4.99MHz sine wave near the Nyquist limit is virtually identical to much lower frequency sine wave input. The under-sampled 19.999MHz sine wave illustrates the ADC600's excellent analog input full-power bandwidth. Figure 11 shows a block diagram of this high-speed digitizer.

HISTOGRAM TESTING

Histogram testing is used to test differential nonlinearity of the ADC600. This system block diagram is shown in Figure 12 and histogram test results for a typical converter are shown in Figure 13. Note that differential nonlinearity is 1/2LSB at 200Hz and it shows virtually no degradation near the Nyquist limit of 5MHz; there are no missing codes present and the peak nonlinearity does not exceed 1LSB. Histogram testing is a useful performance indicator as the width of all codes can be determined.

SPECTRUM ANALYZER TESTING

A beat-frequency technique (Figure 14) can be used to view digitized waveforms on an oscilloscope and, with care, this technique can also be used for testing high-speed ADC dynamic characteristics with an analog spectrum analyzer.

In this method a test signal is digitized by the ADC600 and the output digital data is latched into an external ECL latch by the converter Data Valid output pulse driving a divide-by-N counter. The holding register drives a 12-bit video-speed DAC which reconstructs the digital signal back into an analog replica of the ADC600 input. This analog signal also includes distortion products and noise resulting from the digitization, which can be viewed on an ordinary RF spectrum analyzer. Typical results are shown in Figures 15 and 16.

It is important to realize that the distortion and noise measured by this technique include not only that from the ADC600, but also the entire analog-to-analog test

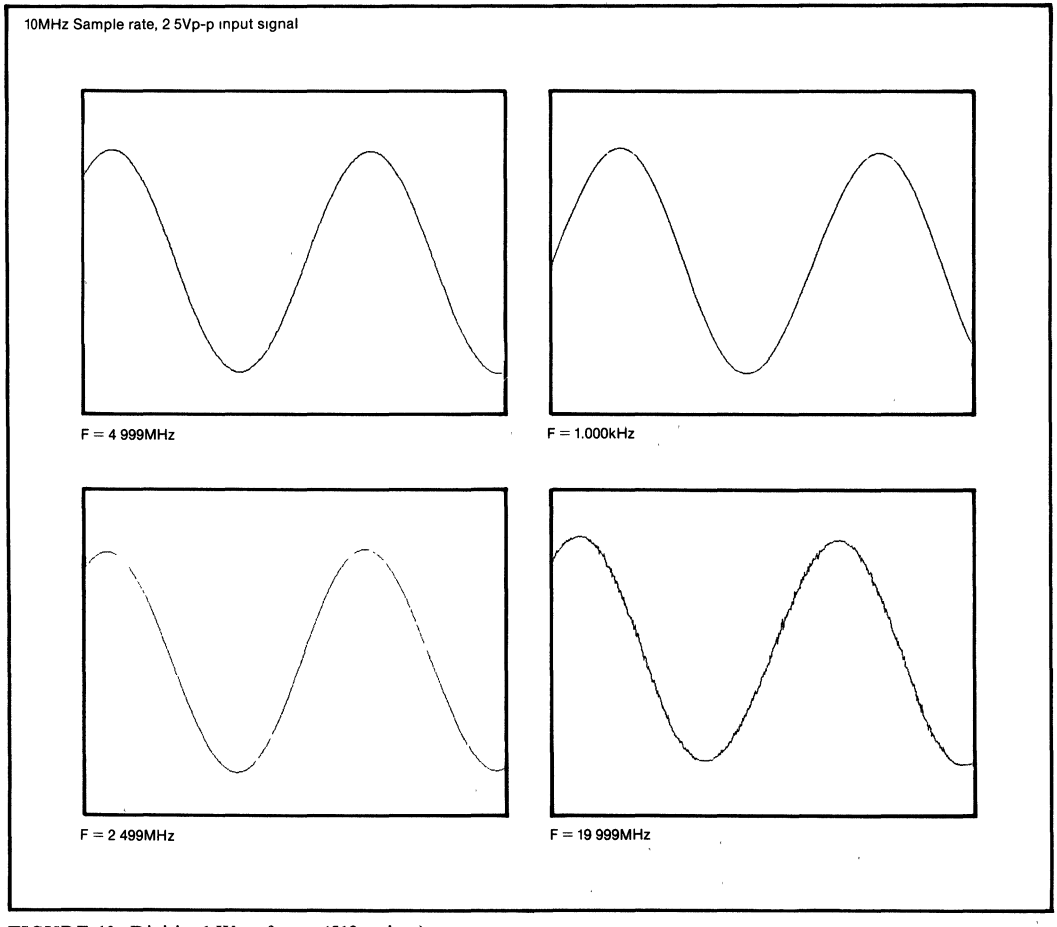


FIGURE 10. Digitized Waveforms (512 points).

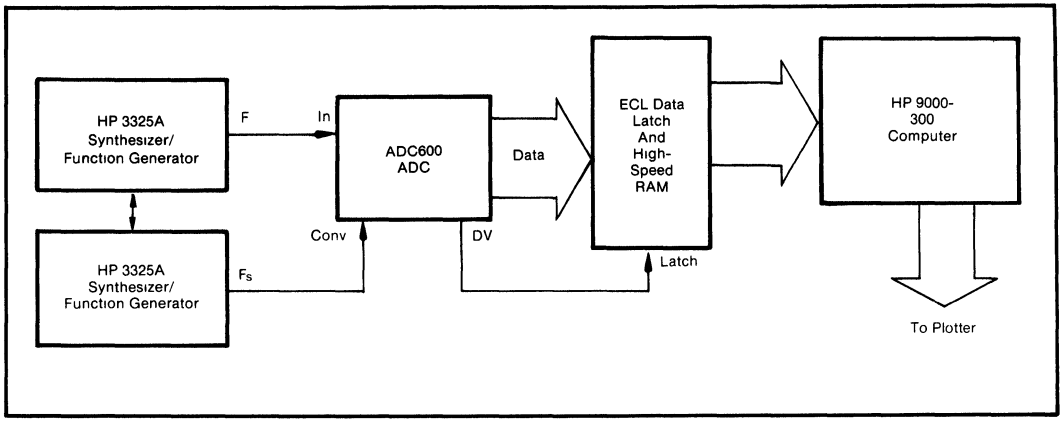


FIGURE 11. High-Speed Digitizer.

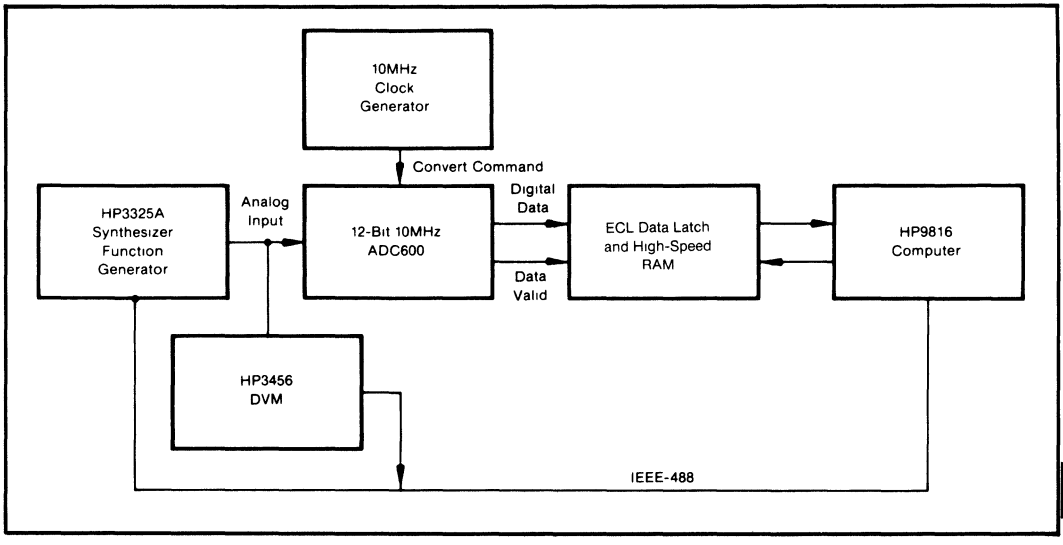


FIGURE 12. Block Diagram of Histogram Test.

system. Nonlinearity of the reconstruction circuit must be very low to measure a high performance ADC, and this places severe requirements on the DAC, deglitcher, and buffer amplifiers.

Using the high-speed video DAC63 in the analog reconstruction circuit allows excellent test circuit linearity to be achieved. Clocking the DAC (demodulating) at f_C/N allows a longer settling time and keeps linearity high in the digital-to-analog portion of the test circuit. Spectrum analyzer dynamic range can be a limiting factor in this method and a sharp notch filter can be used to attenuate the high-level fundamental frequency. Attenuating the fundamental allows the spectrum analyzer to be used on a more sensitive range without generating distortion products within the input of the analyzer.

Note that even though the signal is demodulated at a frequency of sample rate/N (here N = 2 or 4), the distortion products still maintain a correct frequency relationship to the fundamental. While this analog technique shows excellent performance, it cannot exclude some distortion products unavoidably generated within the analog reconstruction portion of the test system. For this reason, the digital FFT technique is capable of more accurate high-speed analog/digital converter dynamic performance measurements.

TIMING

The ADC600 generates all necessary timing signals in laser-trimmed submodules. Only the timing between Convert Command, Output Data, and Data Valid must

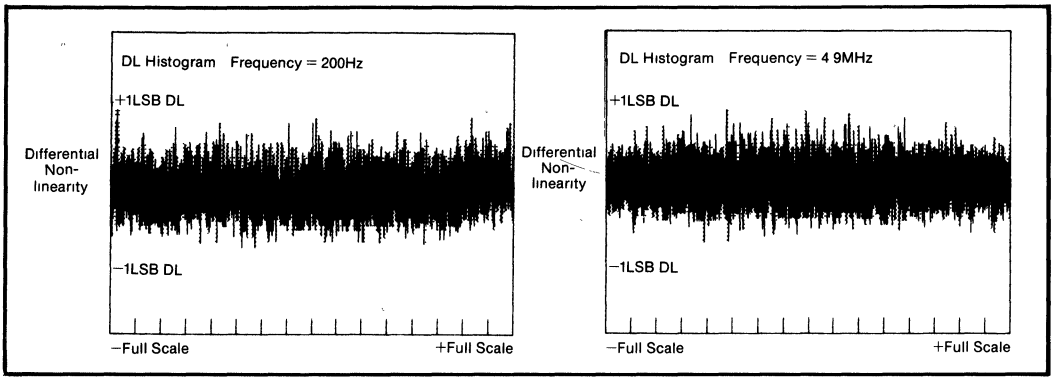


FIGURE 13. Histogram Test Results (10MHz Sample Rate).

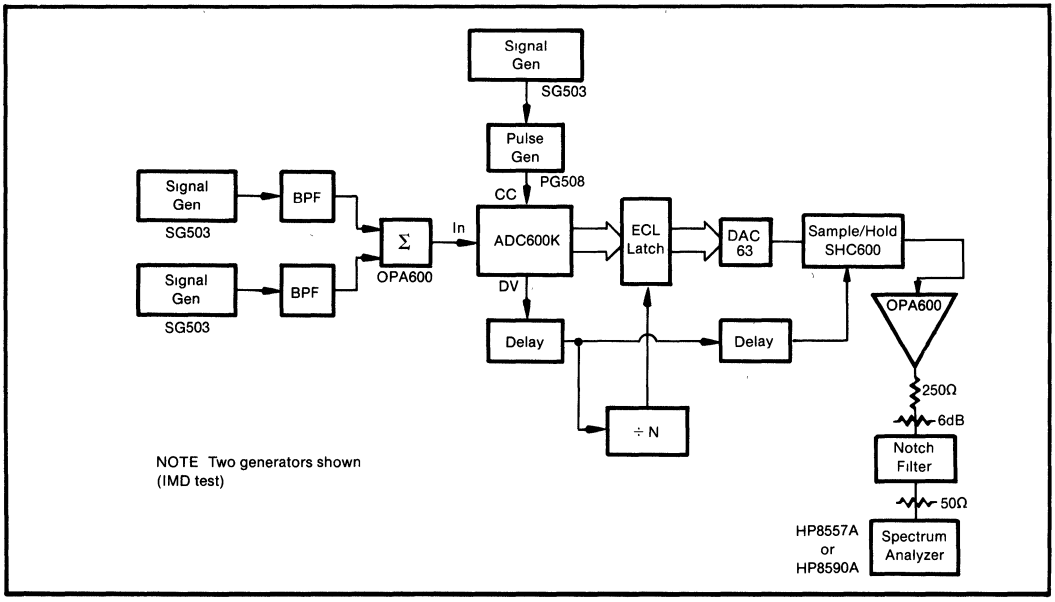


FIGURE 14. Analog-to-Analog Spectral Analysis by Beat-Frequency Techniques.

be considered. Proper timing is shown in Figure 17. The output data **cannot** be timed by the conversion clock, since the data from the 12-bit adder is not guaranteed until the Data Valid pulse is generated.

Data should be latched into an external 12-bit ECL register that can operate reliably with a set-up time of 5ns minimum (Figure 18).

Logic conversion to TTL can be accomplished by logic level translator ICs (such as 10125 or 10124), but care must be exercised, since TTL is very noisy and maintaining a clean analog signal can be difficult. To preserve the low noise of ECL logic, any conversion to TTL should be done on a separate circuit board which is driven by differential ECL drivers.

1. FAST™ Applications Handbook, 1987. Fairchild Semiconductor Corp.
2. *Fairchild Advanced CMOS Technology*, Technology Seminar Notes, 1985.
3. *Impedance Matching Tweaks Advance CMOS IC Testing*, Gerald C. Cox, Electronic Design, April, 1987
4. *Grounding for Electromagnetic Compatibility*, Jerry H Bogar, Design News, 23 February, 1987.

THERMAL REQUIREMENTS

The ADC600 is tested and specified over a temperature range of 0°C to +70°C (K grade) and −25°C to +85°C (B grade). The converters are tested in a forced-air environment with a 10 SCFM air flow. The ADC600 can be operated in a normal convection ambient-air environment if submodule case temperature does not exceed the upper limit of its specification.[1]

High junction temperature can be avoided by using forced-air cooling, but it is not required at moderate ambient temperatures. Worst-case junction temperature (θ_{JC}) and top-surface submodule (θ_{CA}) are presented in Table I to aid the designer in determining cooling requirements.

1 *Maximizing Heat Transfer from PCBs*, Machine Design, March 26, 1987, Jeilong Chung

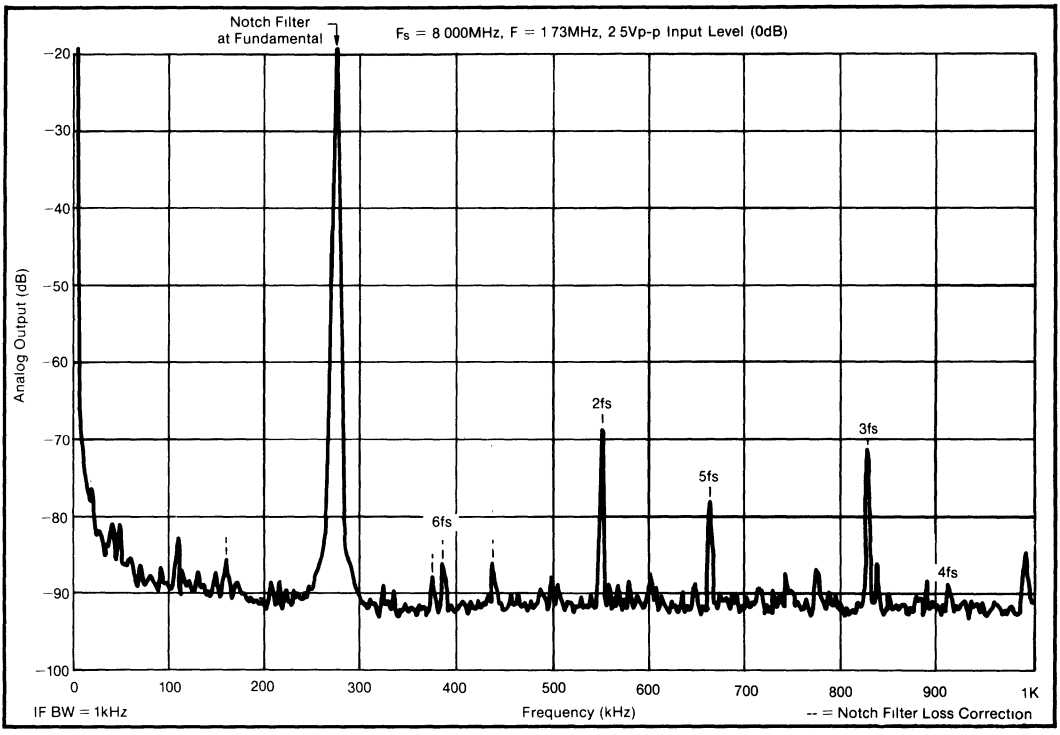


FIGURE 15. Analog-to-Analog Harmonic Distortion.

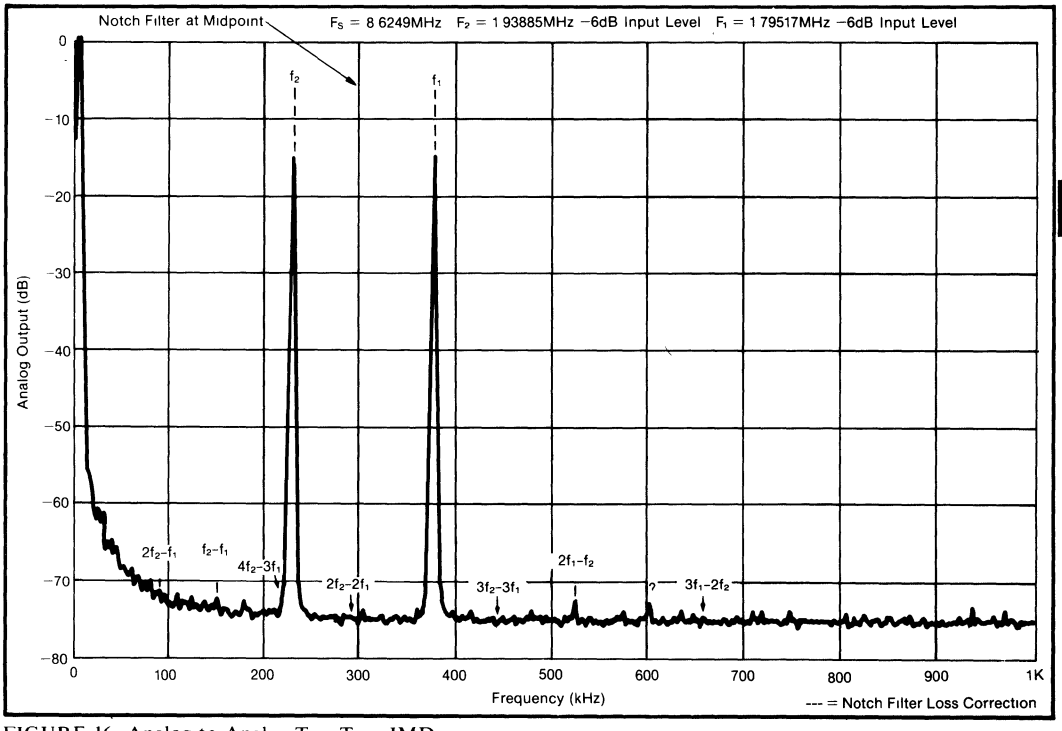


FIGURE 16. Analog-to-Analog Two-Tone IMD.

TABLE I. Cooling Requirement Factors.

Submodule	Power Dissipation (W)	25°C Ambient Air Normal Convection θ_{JC} (°C/W)	θ_{CA} (°C/W)	DIP Package Type
SHC600	1 5	28 7	23 3	24-pin
SM10343	1 6	17 5	24 4	24-pin
SM10344	1 6	10 6	21 3	32-pin
SM10345	1 6	17 5	21 9	24-pin
SM10346	2 1	8 6	16 7	40-pin
SM10347	1 1	17 3	28 2	40-pin

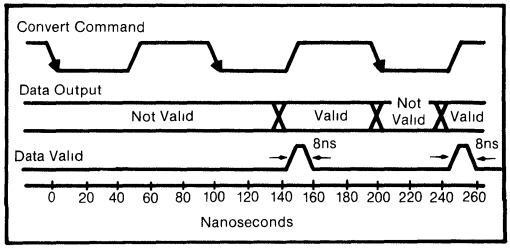


FIGURE 17. ADC600 Timing Diagram.

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown Q models are environmentally-screened versions of our standard industrial products, designed to provide enhanced reliability. The screening illustrated in Table II is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient way of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883. Table III shows the board-level screening flow for ADC600Q.

TABLE II. Screening Flow for ADC600Q (active components).

Screen	MIL-STD-883, Method, Condition	Screening Level
Internal Visual	Burr-Brown QC4118	
Electrical Test	Burr-Brown test procedure	
High Temperature Storage (Stabilization Bake)	1008	24 hour, +125°C
Temperature Cycling	1010	10 cycles, −55°C to −125°C
Constant Acceleration	2001, A	2000 G, Y Axis only
Burn-In	1015, D	160 hour, +85 or +70°C, steady-state
Hermeticity Fine Leak Gross Leak	1014, C	bubble test only, preconditioning omitted
Final Electrical	Burr-Brown test procedure	
External Visual	Burr-Brown QC5150	

TABLE III. Screening Flow for ADC600Q (board level).

Screen	MIL-STD-883, Method, Condition	Screening Level
External Visual	Burr-Brown QC Specification	
Electrical Test	Burr-Brown Data Sheet	
Stabilization Bake	1008	24 hour, +125°C
Burn-In	1015, D	160 hour, +85°C or +70°C steady-state
Final Electrical	Burr-Brown Data Sheet	
Final External Visual	Burr-Brown QC Specification	

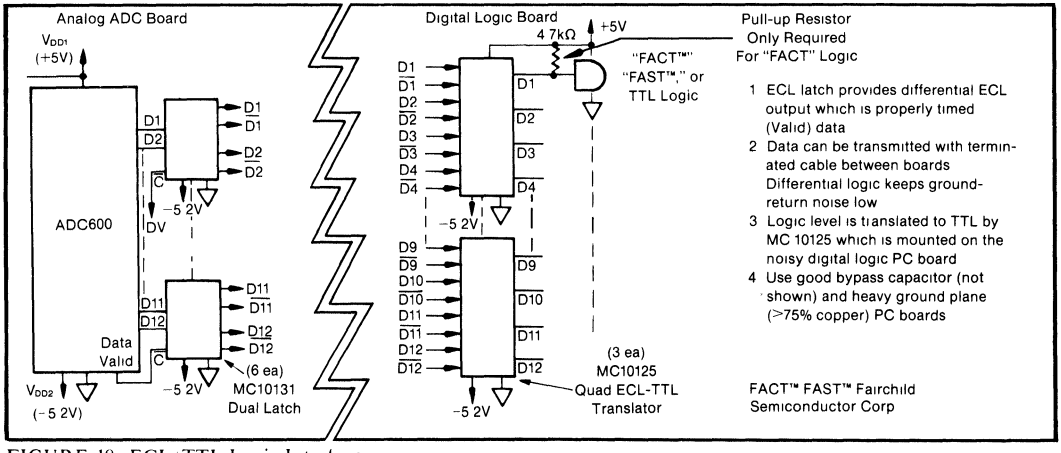


FIGURE 18. ECL/TTL Logic Interface.

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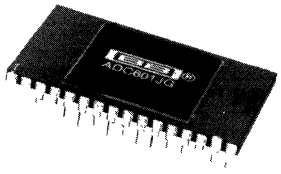


ADC601

ABRIDGED DATA SHEET
REQUEST COMPLETE DATA SHEET
FROM BURR-BROWN SALES OFFICE

12-Bit 900ns ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 12-BIT RESOLUTION
- ±0.012% LINEARITY ERROR
- NO MISSING CODES –55°C to +125°C (S GRADE)
- CONVERSION TIME: 900ns
- 2-CHIP DESIGN
- 32-PIN CERAMIC DIP PACKAGE

DESCRIPTION

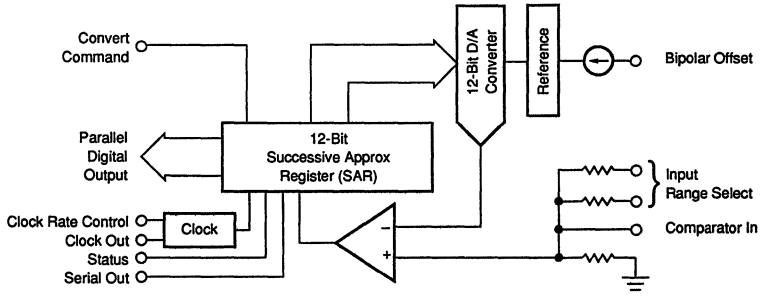
The ADC601 is a high speed Duolithic™ (two integrated circuits) successive approximation analog-to-digital converter. This unique two-chip design utilizes a bipolar thin film IC to preserve high speed analog accuracy and a high speed CMOS IC to perform digital logic control.

It is complete with internal reference, clock and comparator and is packaged in a 32-pin ceramic DIP. Conversion time is set at the factory to 900ns. Serial and parallel output performance is guaranteed with no missing codes over the full input voltage, power supply, and temperature operating temperature range. The gain and offset errors may be externally adjusted to zero.

Internal scaling resistors are provided for the selection of analog signal input ranges of 0V to +10V, ±5V and ±10V. The ADC601's input is specifically designed to be easily driven with minimal disturbance to the driving amplifier.

Output codes are available in complementary binary for unipolar inputs and bipolar offset binary for bipolar inputs.

All digital input and outputs are TTL-compatible. Power supply requirements are ±15V and +5V.



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PDS-867

SPECIFICATIONS

ELECTRICAL

T_C = +25°C, 900ns conversion time, $\pm V_{CC}$ = 15V, $+V_{DD}$ = +5v, and 6-minute warm-up in a normal convection environment unless otherwise noted.

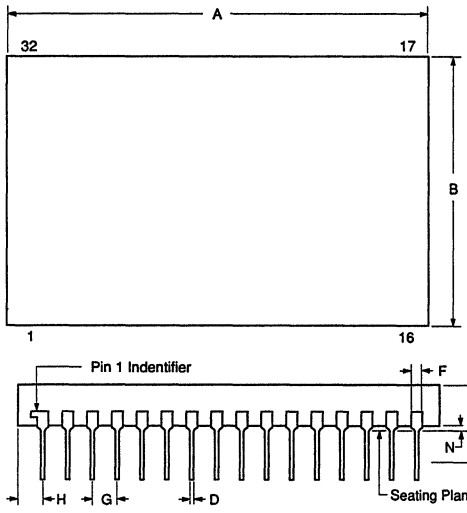
PARAMETER	CONDITIONS	ADC601JG MIN	ADC601JG TYP	ADC601JG MAX	ADC601KG/SG MIN	ADC601KG/SG TYP	ADC601KG/SG MAX	UNITS
RESOLUTION				12			*	Bits
INPUTS								
ANALOG								
Voltage Ranges: Bipolar	Full Scale		±5, ±10			*		V
Unipolar	Full Scale		0 to –10			*		V
Impedance: –10V to 0V, ±5V			1.4			*		kΩ
±10V			2.4			*		kΩ
DIGITAL								
Convert Command	Logic "0 to 1" starts conversion. Logic "1 to 0" resets logic with minimum "0" of 50ns.							
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error[1]			±0.08			±0.04		%
Offset Error[1]: Unipolar	DC		±0.07			±0.05		% of FSR[2]
Bipolar	DC		±0.02			*		% of FSR
Linearity Error:								
0.9µs Conversion Time			±0.024			±0.012		% of FSR
Differential Linearity Error:								
0.9µs Conversion Time			±0.024			*		% of FSR
CONVERSION TIME								
Factory Set			0.9	1.0		*	*	µs
DRIFT								
Gain	T_{MIN} to T_{MAX}		±15			±10		ppm of FSR/°C
Offset: Unipolar	T_{MIN} to T_{MAX}		±3			±2		ppm of FSR/°C
Bipolar	T_{MIN} to T_{MAX}		±5			±3		ppm of FSR/°C
OUTPUT								
DIGITAL DATA								
Parallel								
Output Codes: Unipolar			Complementary Straight Binary					
Bipolar			Bipolar Offset Binary					
Status			Logic "1" during Conversion					
Internal Clock:								
Frequency (without external clock adjustment)			15			*		MHz
POWER SUPPLY REQUIREMENTS								
Power Consumption			1.5			*		W
Rated Voltage: Analog ($\pm V_{CC}$)		±14.25	±15.0	±15.75	*	*	*	VDC
Digital ($+V_{DD}$)		+4.75	+5.0	+5.25	*	*	*	VDC
TEMPERATURE RANGE								
Specification	T_{CASE} JG,KG	0		+70	*		*	°C
	SG				–55		+125	°C

* Same specifications as for ADC601JG

NOTES: (1) Adjustable to zero. (2) FSR means Full Scale Range. For example, unit connected for ±10V has 20V FSR. (3) Conversion time is factory-set to approximately 900ns (+25°C). No missing Codes is guaranteed over T_{MIN} to T_{MAX}

MECHANICAL

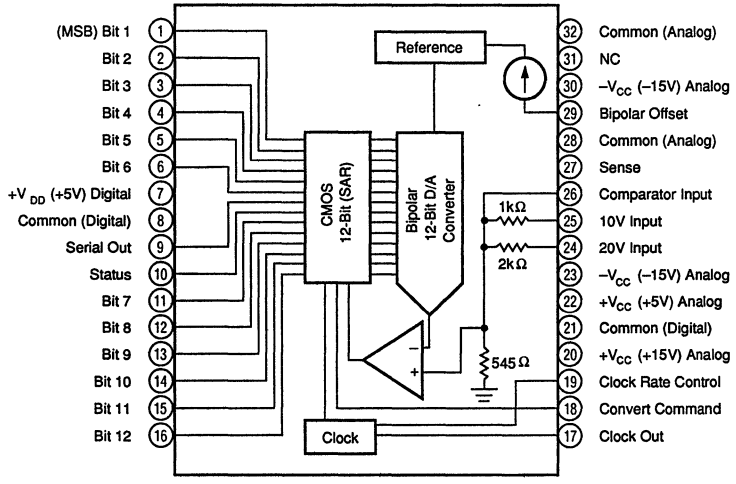
G Package— 32-Pin Ceramic DIP



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.678	1.712	42.62	43.48
B	1.079	1.101	27.41	27.97
C	.180	.210	4.57	5.33
D	.016	.020	0.41	0.51
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.089	.106	2.26	2.69
J	.009	.012	0.23	0.30
K	.200	.210	5.08	5.33
L	.900 BASIC		22.86 BASIC	
N	.015	.035	.38	.89

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin material and plating composition conform to method 2003 (solderability of MIL-STD-883 (except paragraph 3.2). Hermeticity Conforms to Method 1014, Condition condition C, (fluorocarbon) of MIL-STD-883 (gross leak).

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

V_{CC}	±18V
V_{DD}	+7V
Digital Inputs	+5.5V
Analog Inputs	±15
Comparator Input	–3.7V to +0.7V
Operating Temperature: Ambient	+125°C
Case	+135°C
Storage Temperature	–65°C to +150°C

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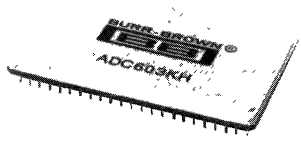


ADC603

ABRIDGED DATA SHEET
REQUEST COMPLETE DATA SHEET FROM BURR-BROWN SALES OFFICE

12-BIT 10MHz SAMPLING ANALOG-TO-DIGITAL CONVERTER

FEATURES

- HIGH SPURIOUS-FREE DYNAMIC RANGE
- SAMPLE RATE: DC to 10MHz
- HIGH SIGNAL/NOISE RATIO: 68.2dB
- HIGH SINAD RATIO: 66dB
- LOW HARMONIC DISTORTION: –69.6dBC
- LOW INTERMOD. DISTORTION: –77.7dBC
- COMPLETE SUBSYSTEM: Contains Sample/Hold and Reference
- 46-PIN DIP PACKAGE
- 0°C TO +70°C AND –55°C TO +125°C

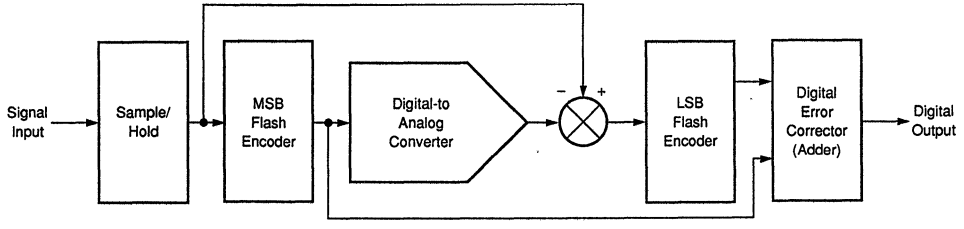
APPLICATIONS

- DIGITAL SIGNAL PROCESSING
- RADAR SIGNAL ANALYSIS
- TRANSIENT SIGNAL RECORDING
- FFT SPECTRUM ANALYSIS
- HIGH-SPEED DATA ACQUISITION
- IR IMAGING SYSTEMS
- DIGITAL RECEIVERS
- SIGINT, ESM, AND EW SYSTEMS
- DIGITAL OSCILLOSCOPES

DESCRIPTION

The ADC603 is an high performance analog-to-digital converter capable of digitizing signals at any rate from DC to 10 megasamples per second. Outstanding spurious-free dynamic range has been achieved by minimizing noise and distortion. Complete static and dynamic test results are furnished with each KH and SH grade unit at no additional cost.

The ADC603 is a two-step subranging ADC sub-system containing an ADC, sample/hold amplifier, voltage reference, timing, and error-correction circuitry in a 46–pin hybrid DIP package. Logic is TTL. Two temperature ranges are available: 0 °C to +70°C (JH, KH) and –55°C to +125°C (RH, SH). A fully militarized version (ADC603SH/883B) is available from Burr-Brown's Military Products Division.



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SPECIFICATIONS

ELECTRICAL

T_C = +25°C, 10MHz sampling rate, R_S= 50Ω, $\pm V_{CC}$= ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, and 15–minute warmup in convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC603JH/RH MIN	ADC603JH/RH TYP	ADC603JH/RH MAX	ADC603KH/SH MIN	ADC603KH/SH TYP	ADC603KH/SH MAX	UNITS
RESOLUTION				12			12	BITS
INPUTS								
ANALOG								
Input Range	Full scale	–1.25		+1.25	*		*	V
Input Impedance			1.5			*		MΩ
Input Capacitance			5			*		pF
DIGITAL								
Logic Family				TTL Compatible				
Convert Command	Start Conversion			Positive Edge				
Pulse Width	t = Conversion Period	10		t–20	*		*	ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 200Hz		±0.2	±2		±0.1	± 1	%FSR[1]
Input Offset	DC		±0.2	±2		*	±0.75	%FSR
Integral Linearity Error	f = 200Hz		0.75			0.5	1	LSB
Differential Linearity Error	f = 200Hz: 68.3% of all codes		0.3			0.25	0.5	LSB
	99.7% of all codes		0.4			0.3	0.65	LSB
	100% of all codes		0.5			0.4	0.75	LSB
Missing Codes			none			none		
Power Supply Rejection	$\Delta +V_{CC}$ = ±10%		±0.03			*	±0.07	%FSR/%
	$\Delta -V_{CC}$= ±10%		±0.04			*	±0.07	%FSR/%
	$\Delta +V_{DD1}$= ±10%		±0.004			*	±0.03	%FSR/%
	$\Delta -V_{DD2}$= ±10%		±0.01			*	±0.03	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		10M	DC		10M	Samples/s
Pipeline Delay	Logic Selectable		1, 2 or 3 Convert Command Periods					
DYNAMIC CHARACTERISTICS								
Differential Linearity Error	f = 4.9MHz: 68.3% of all codes		0.3			*	0.5	LSB
	99.7% of all codes		0.75			0.5	1.0	LSB
	100% of all codes		1.0			0.6	1.25	LSB
Total Harmonic Distortion[2]								
f = 5.00MHz (–0.5dB)	f_S = 9.99MHz		–68			–69.6	–64	dBC[3]
f = 100kHz			–70			–72.1	–66	dBC
Two-Tone Intermodulation Distortion[2][4]								
f = 2.20MHz (–6.5dB)	f_S = 8.006MHz		–75			–77.7	–71	dBC
f = 2.50MHz (–6.5dB)								
Signal-to-Noise and Distortion (SINAD) Ratio								
f = 5.00MHz (–0.5dB)	f_S = 9.99MHz		65		62	66.0		dB
f = 100kHz (–0.5dB)			67		64	68.5		dB
Signal-to-Noise Ratio (SNR)								
f = 5.00MHz (–0.5dB)	f_S = 9.99MHz		67		64	68.2		dB
f = 100kHz (–0.5dB)			68		66	70.1		dB
Aperture Time			5			*	9	ns
Aperture Jitter			9			*	20	ps RMS
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB input		70		50	*		MHz
Full Power	0dB input		40		30	*		MHz
Overload Recovery Time	2x Full-Scale input		80			*	140	ns
OUTPUTS								
Logic Family				TTL Compatible				
Logic Coding	Logic Selectable		Two's Complement or Inverted Two's Complement					
Logic Levels	Logic "LO" I_{OL} = –3.2mA	0	+0.3	+0.8	0	+0.3	+0.5	V
	Logic "HI" I_{OH} = 160µA	+2.4	+3.5	+5.0	+2.4	+3.5	+5.0	V
EOC Delay Time	Data Out to DV	5	35		5	35		ns
Tri-State Enable/Disable Time	I_{OL} = –6.4mA, 50% In to 50% Out		37	100		37	100	ns
Data Valid Pulse Width		20	45	60	20	45	60	ns
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	+14.25	+15	+15.75	V
$-V_{CC}$		–14.25	–15	–15.75	–14.25	–15	–15.75	V
$+V_{DD1}$		+4.75	+5	+5.25	+4.75	+5	+5.25	V
$-V_{DD2}$		–4.95	–5.2	–5.46	–4.95	–5.2	–5.46	V
Supply Currents: $+I_{CC}$	Operating		+60			+60	+80	mA
$-I_{CC}$			–60			–60	–80	mA
$+I_{DD1}$			+280			+280	+330	mA
$-I_{DD2}$			–565			–565	–630	mA
Power Consumption	Operating		6.1			6.1		W

* Same as ADC603JH/RH.

SPECIFICATIONS

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

$\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = −5.2V, R_S = 50Ω, 15-minute warmup, and $T_C = T_{MIN}$ to T_{MAX}, unless otherwise noted.

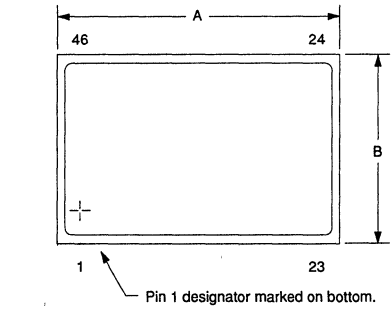
PARAMETER	CONDITIONS	ADC603JH/RH MIN	ADC603JH/RH TYP	ADC603JH/RH MAX	ADC603KH/SH MIN	ADC603KH/SH TYP	ADC603KH/SH MAX	UNITS
TEMPERATURE RANGE								
Specification	T_{CASE} max JH,KH	0		+70	*		*	°C
	RH,SH	−55		+125	*		*	°C
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 200Hz		±0.4	±2		*	±1.5	%FSR
Input Offset	DC		±0.4	±2		*	±1	%FSR
Integral Linear Error	f = 200Hz		0.75			0.6	1.25	LSB
Differential Linearity Error	f = 200Hz: 68.3% of all codes		0.4			0.3	0.6	LSB
	99.7% of all codes		0.5			0.4	0.75	LSB
	100% of all codes		0.75			0.6	1	LSB
Missing Codes			none			*		
Power Supply Rejection	Δ $+V_{CC}$ = ±10%		±0.04			*	±0.08	%FSR/%
	Δ $-V_{CC}$ = ±10%		±0.05			*	±0.08	%FSR/%
	Δ $+V_{DD1}$ = ±10%		±0.004			*	±0.05	%FSR/%
	Δ $-V_{DD2}$ = ±10%		±0.02			*	±0.05	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		10M	DC		10M	Samples/s
DYNAMIC CHARACTERISTICS								
Differential Linearity Error	f = 4.9MHz: 68.3% of all codes		0.5			0.4	0.75	LSB
	99.7% of all codes		1			0.6	1.25	LSB
	100% of all codes		1.25			0.7	1.5	LSB
Total Harmonic Distortion[2]								
f = 5.00MHz (−0.5dB)	f_S = 9.99MHz		−67			−68.8	−62	dBC
f = 100kHz			−69			−69.5	−64	dBC
Two-Tone Intermodulation Distortion								
f = 2.20MHz (−6.5dB)	f_S = 8.006MHz		−72			−74.4	−68	dBC
2.500MHz (−6.5dB)								
Signal-to-Noise and Distortion (SINAD) Ratio								
f = 5.00MHz (−0.5dB)	f_S = 9.99MHz		65		60	65.4		dB
f = 100kHz (−0.5dB)			66		62	66.5		dB
Signal-to-Noise Ratio (SNR)								
f = 5.00MHz (−0.5dB)	f_S = 9.99MHz		67		62	68.0		dB
f = 100kHz (−0.5dB)			68		64	69.5		dB
Aperture Delay Time			6			*	10	ns
Aperture Jitter			10			*	20	ps RMS
Analog Input Bandwidth (−3dB)								
Small Signal	−20dB input		70		50	*		MHz
Full Power	0dB input		40		30	*		MHz
Overload Recovery Time	2x Full-Scale input		80			*		ns
OUTPUTS								
Logic Levels	Logic "LO", I_{OL} = -6.4mA	0	+0.3	+0.8	*	*	+0.5	V
	Logic "HI", I_{OH} = 160µA	+2.4	+3.5	+5.0	*	*	*	V
EOC Delay Time	Data Out to DV	5	35		*	*		ns
Tri-State Enable/Disable Time	I_{OL} = −6.4mA, 50% In to 50% Out		42	100		*	*	ns
Data Valid Pulse Width		20	45	60	*	*	*	ns
POWER SUPPLY REQUIREMENTS								
Supply Currents: $+I_{CC}$	Operating		+65			*	+80	mA
$-I_{CC}$			−61			*	−80	mA
$+I_{DD1}$			+285			*	+333	mA
$-I_{DD2}$			−570			*	−630	mA
Power Consumption	Operating		6.1			*		W

* Same as ADC603JH/RH.

NOTES: (1) FSR: Full-Scale Range = 2.5Vp-p. (2) Units with tested and guaranteed distortion specifications are available on special order—inquire. (3) dBC = level refered to carrier-input signal = 0dB); F = input frequency; F_S = sampling frequency. (4) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 6dB lower.

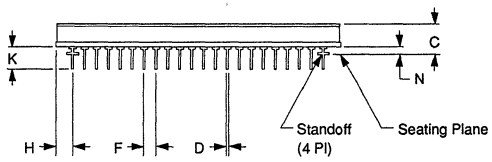
MECHANICAL

H Package— Metal and Ceramic



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.370	2.420	60.20	61.47
B	1.560	1.610	39.62	40.89
C	.200	.260	5.08	6.60
D	.018 DIA BASIC		0.46 DIA BASIC	
F	.100 BASIC		2.54 BASIC	
H	.075	.115	1.91	2.92
K	.150	.190	3.81	4.83
L	1.300	BASIC	33.02	BASIC
M	—	10°	—	10°
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin material and plating composition conform to method 2003 (solderability of MIL-STD-883 (except paragraph 3.2)



PIN ASSIGNMENTS

1	Common (Case)	46	Common (Analog)
2	DNC	45	Analog Signal In
3	$+V_{DD1}$ (+5V) Analog	44	$+V_{CC}$ (+15V) Analog
4	S/H Out	43	$-V_{CC}$ (–15V) Analog
5	A/D In	42	$-V_{DD2}$ (–5.2V) Analog
6	$-V_{DD2}$ (–5.2V) Analog	41	DNC
7	DNC	40	DNC
8	DNC	39	DNC
9	Bit 1(MSB)	38	DNC
10	Bit 2	37	Gain Adjust
11	Bit 3	36	Offset Adjust
12	Bit 4	35	Common (Analog)
13	Bit 5	34	$+V_{CC}$ (+15V) Analog
14	Bit 6	33	$-V_{CC}$ (–15V) Analog
15	Bit 7	32	Common (Analog)
16	Bit 8	31	$-V_{DD2}$ (–5.2V) Digital
17	Bit 9	30	$+V_{DD1}$ (+5V) Analog
18	Bit 10	29	1 Pipeline Delay In
19	Bit 11	28	0 Pipeline Delay In
20	Bit 12 (LSB)	27	Output Logic Invert In
21	$+V_{DD1}$ (+5V) Digital	26	Common (Digital)
22	Data Valid Output	25	Tri-State Enable In
23	Common (Digital)	24	Convert Command In

ORDERING INFORMATION

ADC603 ( ) H /MIL

Basic Model Number

Performance Grade Code
- J, K: 0°C to +70°C Case Temperature
- R, S: –55°C to +125°C Case Temperature

Package Code
- H: Metal and Ceramic

Reliability Screening
- /MIL: High Reliability

ABSOLUTE MAXIMUM RATINGS

$\pm V_{cc}$	±16.5V
$+V_{DD1}$	+7.0V
$\pm V_{DD2}$	-7.0V
Analog Input	±5.0V
Logic Input	–0.5V to $+V_{DD1}$
Case Temperature	+125°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +165°C

Stresses above these ratings may permanently damage the device.

Screening Flow for ADC603/MIL.

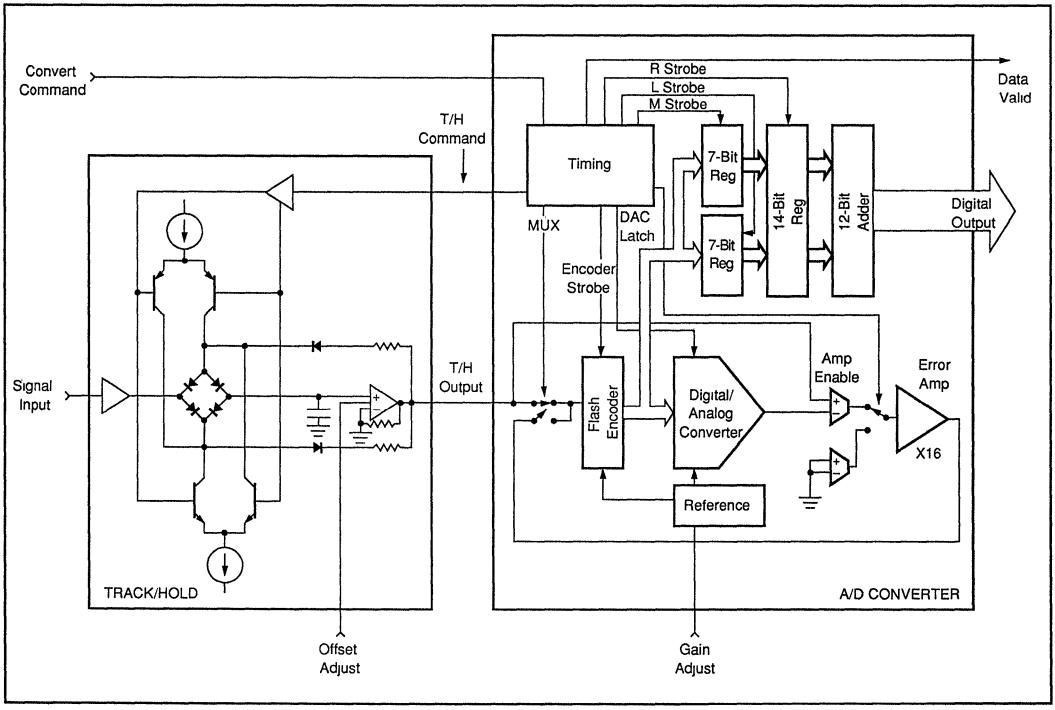
Screen	MIL-STD-883, Method, Condition	Screening Level
Internal Visual	2017	
Electrical Test	Burr-Brown test procedure	
High Temperature Storage (Stabilization Bake)	1008	24 hour, +125°C
Temperature Cycling	1010	10 cycles, –55°C to –125°C
Constant Acceleration	2001,A	2000G; Y Axis only
Burn-In	1015, D	160 hour, +125°C, steady-state
Hermeticity: Fine Leak Gross Leak	1014, C	bubble test only, preconditioning omitted
Final Electrical	Burr-Brown test procedure	
External Visual	2009	

Pipeline Delay Selection Logic.

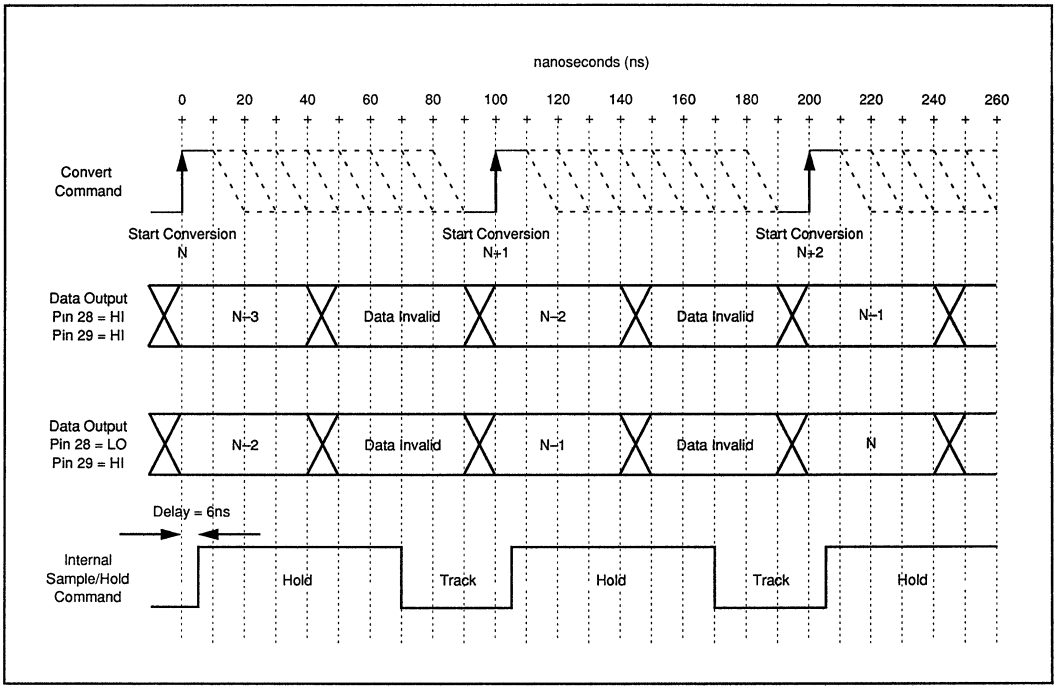
Pin Number	Data Latched by Convert Command		Data Latched by Data Valid Strobe
	N–3	N–2	N–1
28	HI	LO	HI
29	HI	HI	LO

Digital Data Logic Coding.

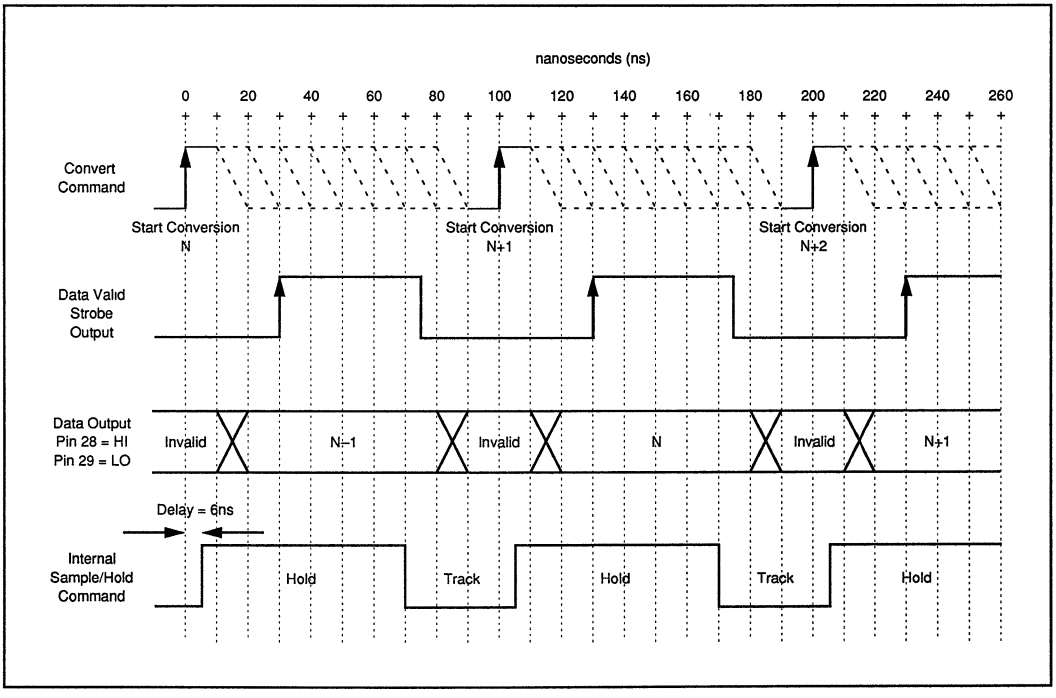
Input Voltage	Digital Data Output Logic Coding	
	Binary Two's Complement (BTC) Pin 27 = LO	Inverted Binary Two's Complement (BTC) Pin 27 = HI
+FS (+1.25V)	011111111111	100000000000
+FS –1 LSB	011111111110	100000000001
+3/4 FS	000111111111	111000000000
+1/2 FS	001111111111	110000000000
+1 LSB	000000000000	111111111111
Bipolar Zero	111111111111	000000000000
–1 LSB	111111111110	000000000001
–1/2 FS	101111111111	010000000000
–3/4 FS	100111111111	011000000000
–FS – 1LSB	100000000001	011111111110
–FS (–1.25V)	100000000000	011111111111
	MSB LSB	MSB LSB



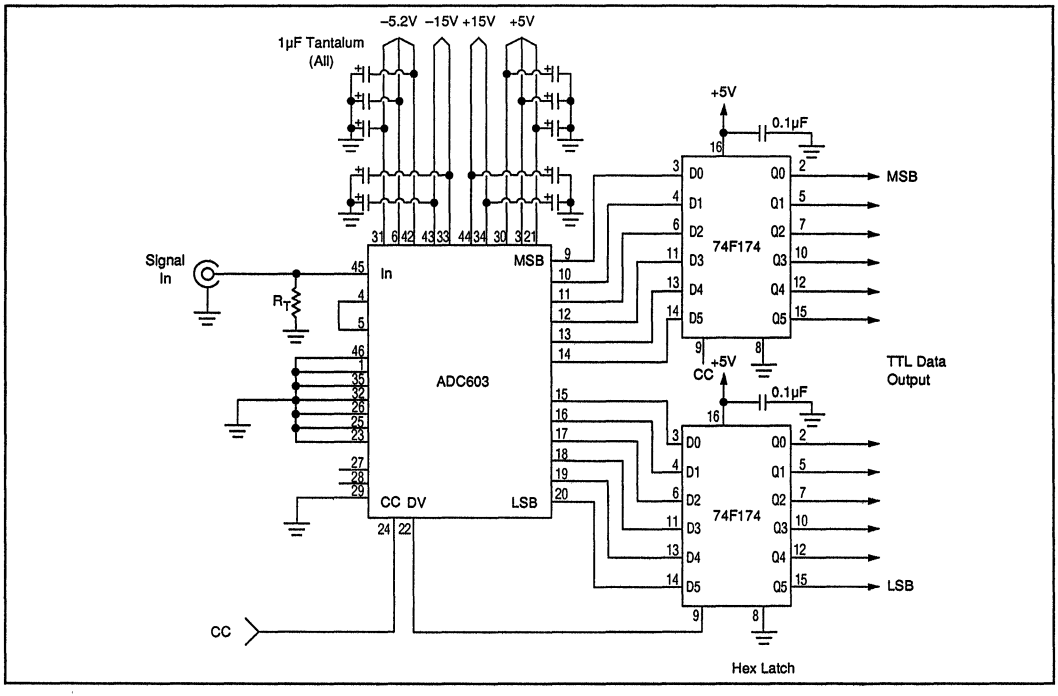
ADC603 BLOCK DIAGRAM—A Two-step Subranging Architecture.



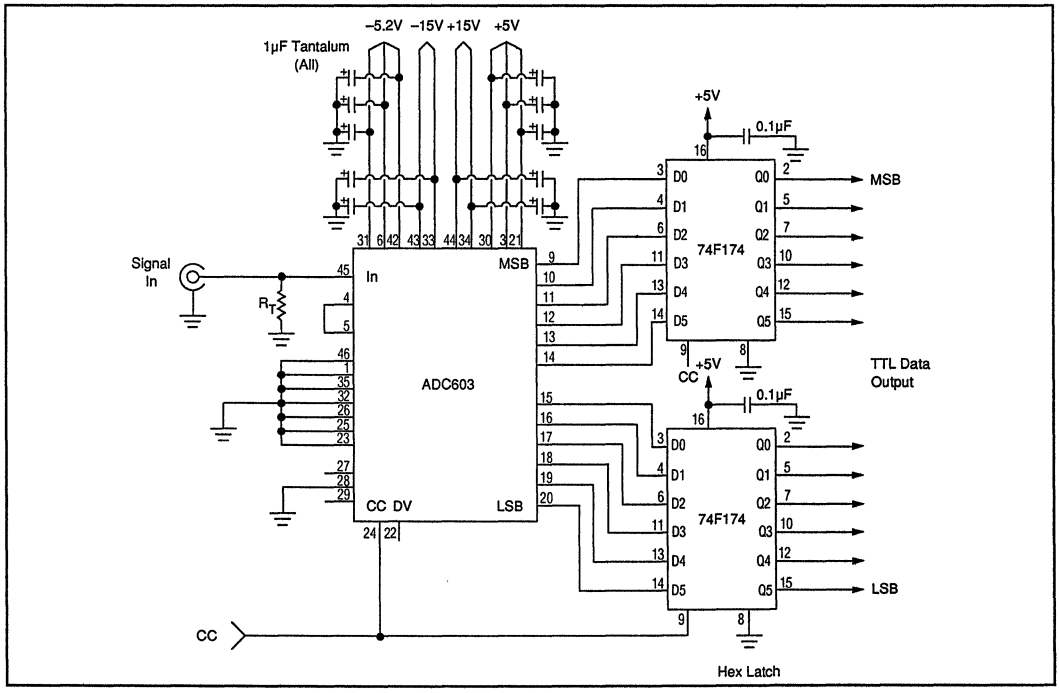
TIMING DIAGRAM—Convert Command Strobe Timing.



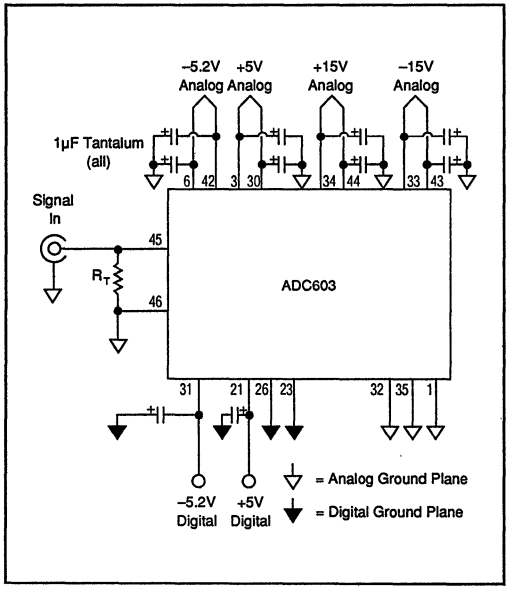
TIMING DIAGRAM—Data Valid Strobe Timing.



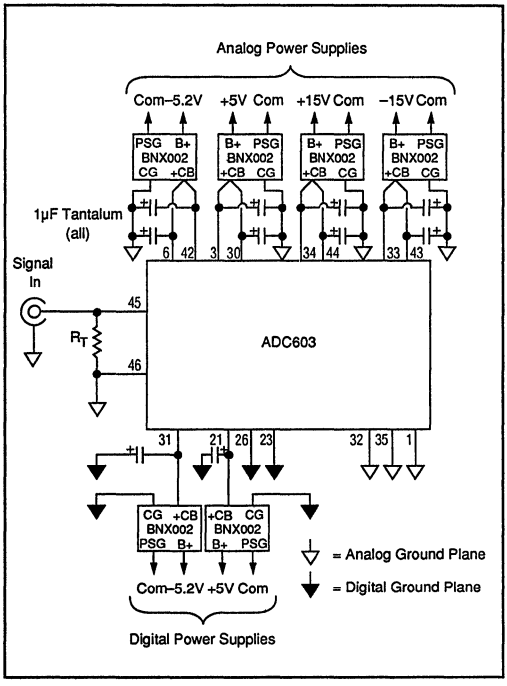
INTERFACE CIRCUIT—Digital Output Strobed by Data Valid Pulse. Supply Connection Shown: Power Supplies and Grounds Shared by Analog and Digital Pins.



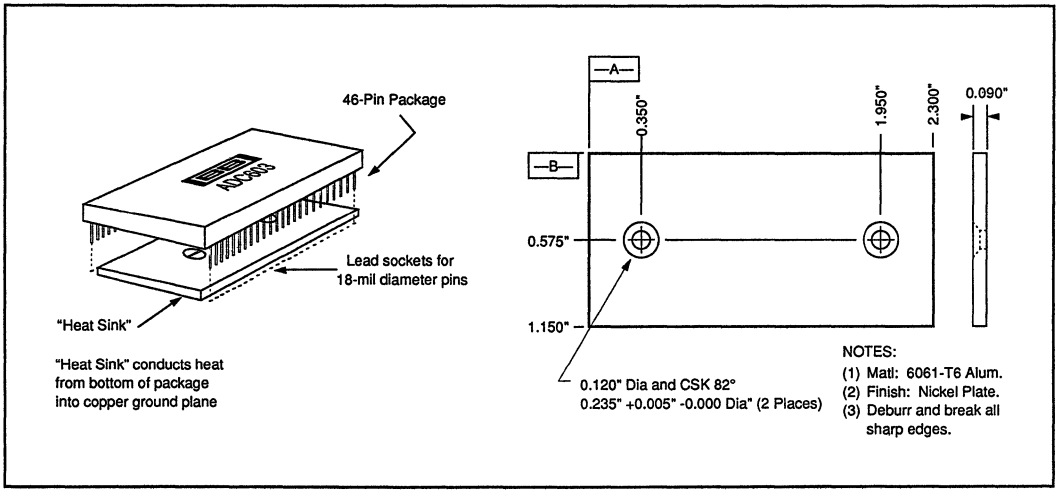
INTERFACE CIRCUIT—Digital Output Strobed by Convert Command Pulse. Supply Connection Shown: Power Supplies and Grounds Shared by Analog and Digital Pin:



POWER SUPPLY CONNECTIONS.
Supply Connection Shown: Separate Analog and Digital Power Supplies and Ground Planes.

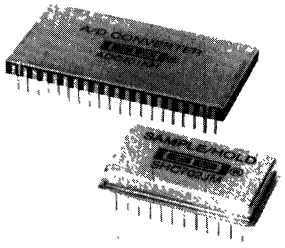


POWER SUPPLY CONNECTIONS.
Supply Connection Shown: Separate Analog and Digital Power Supplies and Ground Planes with Noise Filtering. (Recommended Circuit)



HEAT SINK—Transfers Heat from the DIP Package into a Copper Ground Plane.

BURR-BROWN®



ADC701
SHC702

ABRIDGED DATA SHEET
REQUEST COMPLETE DATA SHEET
FROM BURR-BROWN SALES OFFICE

16-Bit 500kHz SAMPLING A/D CONVERTER SYSTEM

FEATURES

- CONVERSION RATE: DC TO 500kHz
- NO MISSING CODES AT 16 BITS
- SPURIOUS-FREE DYNAMIC RANGE: 107dB
- LOW NONLINEARITY: ±0.0015%
- SELECTABLE INPUT RANGES: ±5V, ±10V, 0 to +10V, 0 to +5V, –10V to 0
- LOW POWER DISSIPATION: 2.8W typical Including Sample/Hold
- METAL AND CERAMIC DIP PACKAGES

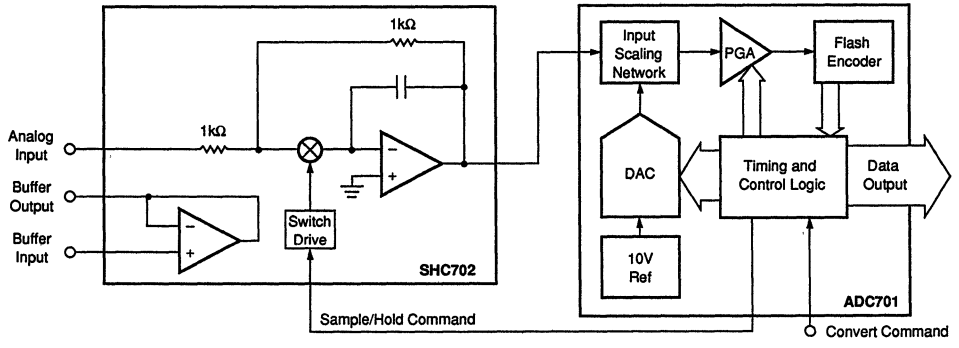
APPLICATIONS

- MEDICAL IMAGING
- SONAR
- PROFESSIONAL AUDIO RECORDING
- AUTOMATIC TEST EQUIPMENT
- HIGH PERFORMANCE FFT SPECTRUM ANALYSIS
- ULTRASOUND SIGNAL PROCESSING
- HIGH SPEED DATA ACQUISITION
- REPLACES DISCRETE MODULAR ADCs

DESCRIPTION

The ADC701 is a very high speed 16-bit analog-to-digital converter based on a three-step subranging architecture. Outstanding dynamic performance is achieved with the SHC702 companion Sample/Hold amplifier. Both devices use hybrid construction for applications where reliability, small size, and low power consumption are especially important.

Excellent linearity and stability are assured through use of a new ultra-precise monolithic D/A converter and a low-drift reference circuit. Custom monolithic op amps provide very high bandwidth and low noise in all sections of the analog signal path. Logic is CMOS/TTL compatible and is designed for maximum flexibility.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491 • FAX: (602) 889-1510

PDS-877

SPECIFICATIONS

ELECTRICAL (ADC701 ONLY)

T_A = +25°C, 500kHz sampling rate, $\pm V_{CC}$ = ±15V, $\pm V_{DD1}$ = ±5V, $+V_{DD2}$ = +5V, and five minute warmup in a convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC701JH MIN	ADC701JH TYP	ADC701JH MAX	ADC701KH MIN	ADC701KH TYP	ADC701KH MAX	UNITS
RESOLUTION				16			*	Bits
INPUTS								
ANALOG								
Voltage Ranges	Unipolar		0 to +5, 0 to +10, −10 to 0					V
	Bipolar		±5, ±10					V
Resistance	0 to +5V Range	2.45	2.5	2.55	*	*	*	kΩ
	0 to +10V, −10 to 0, ±5V Ranges	4.9	5.0	5.1	*	*	*	kΩ
	±10V Range	9.8	10.0	10.2	*	*	*	kΩ
Input Capacitance	All Ranges		5			*		pF
DIGITAL								
Logic Family			TTL-Compatible CMOS					
Convert Command	Start Conversion		Rising Edge					
Pulse Width	t = Conversion Period	50		t − 50				ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error[1]	0 to +10V Range		±0.03	±0.1		*	*	%
	±10V Range		±0.03	±0.1		*	*	%
Power Supply Sensitivity of Gain	All Ranges, All Supplies		±0.005	±0.1		*	*	%/V
Input Offset Error[1]	0 to +10V Range		±1	±3		*	*	mV
	±10V Range		±5	±10		*	*	mV
Power Supply Sensitivity of Offset	All Ranges, All Supplies		±0.006	±0.1		*	*	%FSR/V
Integral Linearity Error[2]			±0.002	±0.003		±0.0015	*	%FSR[3]
Differential Linearity Error[2]			±0.0006	±0.0012		*	*	%FSR
No Missing Codes			Guaranteed			Guaranteed		
Noise	$R_{SOURCE} \leq 50\Omega$		0.5			*		LSB RMS
CONVERSION CHARACTERISTICS								
Sample Rate	Unadjusted	DC		500	*		*	kHz
Conversion Time[4]	Unadjusted		1.45	1.5		*	*	µs
OUTPUTS								
DIGITAL								
Logic Family			TTL-Compatible CMOS					
Data Coding	Unipolar Ranges		Straight Binary					
	Bipolar Ranges		Offset Binary					
Logic "0" Levels (V_{OL})	$I_{OL} \leq 3.2$mA		0.1	0.4		*	*	V
Logic "1" Levels (V_{OH})	$I_{OH} \leq 80\mu$A	4.0	4.9		*	*		V
Data Valid Setup Time Before Strobe	Both Edges	75	125		*	*		ns
INTERNAL REFERENCE								
Voltage	$R_{LOAD} \geq 5k\Omega$	+9.995	+10.000	+10.005	*	*	*	V
Current Available to External Loads		2	5		*	*		mA
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		−14.25	−15	−15.75	*	*	*	V
$+V_{DD1}$		+4.75	+5	+5.25	*	*	*	V
$-V_{DD1}$		−4.25	−5	−6.0	*	*	*	V
$+V_{DD2}$		+4.25	+5	+5.25	*	*	*	V
Supply Currents: $+I_{CC}$	Operating		25	30		*	*	mA
$-I_{CC}$			33	45		*	*	mA
$+I_{DD1}$			45	55		*	*	mA
$-I_{DD1}$			37	50		*	*	mA
$+I_{DD2}$			133	150		*	*	mA
Power Dissipation	Nominal Voltages		1.95	2.3		*	*	W
PERFORMANCE OVER TEMPERATURE								
Specification Temperature Range	T_A min to T_A max	+15		+55	0		+70	°C
Gain Error	All Ranges		±10	±15		*	*	ppm/°C
Input Offset Error	All Unipolar Ranges		±1	±5		*	*	ppm FSR/°C
	All Bipolar Ranges		±1	±5		*	*	ppm FSR/°C
Integral Linearity Error[2]			±0.2			*	±0.5	ppm/°C
Differential Linearity Error[2]			±0.05			*	±0.3	ppm/°C
No Missing Codes			Typical			Guaranteed		
Reference Output Drift			±3			*		ppm/°C
Drift of Conversion Time	Unadjusted		+3	+4		*	*	ns/°C
Sample Rate	With Clock Adjustment	DC		500	*		*	kHz

* Same specifications as ADC701JH.

SPECIFICATIONS

ELECTRICAL (SHC702 ONLY)

T_A = +25°C, 500kHz sampling rate, $\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, and five minute warmup in a convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	SHC702JM MIN	SHC702JM TYP	SHC702JM MAX	UNITS
INPUTS (Without Input Buffer)					
ANALOG					
Voltage Range		±10.25	±11		V
Resistance		0.98	1.00	1.02	kΩ
Capacitance			3		pF
DIGITAL					
Logic Family			LSTTL		
Input Loading			2		LSTTL Loads
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain	R_{SOURCE} = 0Ω		–1		V/V
Gain Error	R_{SOURCE} = 0Ω		±0.02	±0.1	%
Linearity Error	Sample Mode		±0.0003		%FSR
Offset Error	Sample Mode		±0.5	±3	mV
Charge Offset (Pedestal) Error	Sample/Hold Mode, $R_{SOURCE} \leq 50\Omega$		±0.5	±5	mV
Droop Rate	Hold Mode		±0.2	±2	µV/µs
Dynamic Nonlinearity	Sample/Hold Mode		±0.0005		%FSR
Power Supply Sensitivity	Offset Plus Charge Offset, All Supplies		±0.003		%FSR/V
DYNAMIC CHARACTERISTICS					
Acquisition Time	10V step to ±150µV		600		ns
	5V step to ±150µV		500		ns
Sample-to-Hold Settling Time[5]	to ±150µV		120		ns
Aperture Delay Time			20		ns
Aperture Uncertainty (Jitter)			10	25	ps RMS
Slew Rate			150		V/µs
Small Signal Bandwidth	V_{IN} = ±1V		3.1		MHz
Full-Power Bandwidth	V_{IN} = ±10V		2		MHz
Feedthrough Rejection	Hold Mode, 10Vp-p Square Wave Input		0.001		%
OUTPUT					
Voltage Range	$R_{LOAD} \geq 1k\Omega$	±10.25	±11		V
Output current		±40			mA
Short Circuit Protection	R_{LOAD} = 0Ω		Indefinite		
Output Impedance	DC		0.01	0.1	Ω
INPUT BUFFER CHARACTERISTICS					
INPUT					
Impedance			$10^{13} \| \| 3$		Ω||pF
Bias Current	V_{IN} = ±10V		±2	±15	pA
Offset Voltage	$R_{SOURCE} \leq 10k\Omega$		±0.3	±1.5	mV
Voltage Range		±10.25	±11		V
DYNAMIC CHARACTERISTICS					
Slew Rate		20	35		V/µs
Full-Power Bandwidth	V_{IN} = ±10V		570		kHz
Settling Time	10V step to ±150µV		1.7		µs
OUTPUT					
Output Current		±15	±20		mA
Short Circuit Protection	R_{LOAD} = 0Ω		Indefinite		
POWER SUPPLY REQUIREMENTS					
Voltage: $+V_{CC}$	Operating	+13.5	+15	+16.5	V
$-V_{CC}$		–13.5	–15	–16.5	V
$+V_{DD1}$		+4.75	+5	+5.25	V
Current: $+I_{CC}$	Operating		33	40	mA
$-I_{CC}$			18	25	mA
$+I_{DD1}$			5	10	mA
Power Dissipation	Nominal Voltages		790	950	mW
PERFORMANCE OVER TEMPERATURE					
Specification Temperature Range	T_A min to T_A max	–25		+85	°C
Sample/Hold Gain Error	R_{SOURCE} = 0Ω		±1	±5	ppm/°C
Sample/Hold Offset Error	$R_{SOURCE} \leq 50\Omega$		±10	±30	µV/°C
Sample/Hold Charge Offset Error	$R_{SOURCE} \leq 50\Omega$		±10	±80	µV/°C
Droop Rate				±50	µV/µs
Buffer Offset Error	$R_{SOURCE} \leq 10k\Omega$		±3	±15	µV/C

NOTES: (1) Adjustable to zero. Tested and guaranteed for 0 to +10V and ±10V ranges only. (2) Peak-to-peak based on 99.9% of all codes. (3) FSR means full-scale range and depends on the input range selected. (4) ADC conversion time is defined as the time that the Sample/Hold must remain in the Hold mode, i.e. the duration of the Sample/Hold command. This time must be added to the Sample/Hold acqusition time to obtain the total system throughput time. (5) Given for reference only — this time overlaps with the ADC701 conversion time and does not affect system throughput rate.

SPECIFICATIONS

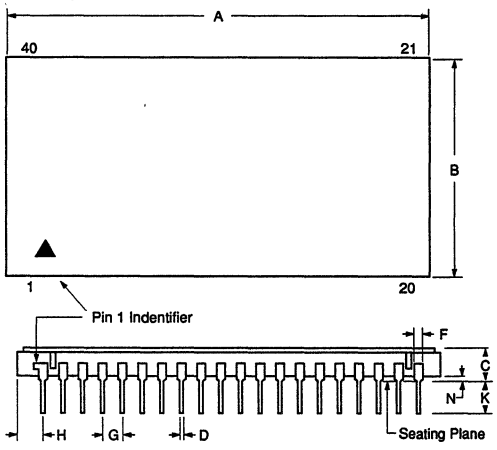
ELECTRICAL (COMBINED ADC701/SHC702)

T_A = +25°C, 500kHz sampling rate, $\pm V_{CC}$ = ±15V, $\pm V_{DD1}$ = ±5V, $+V_{DD2}$ = +5V, and five minute warmup in a convection environment, ±5V input range unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Sample Rate	Unadjusted	DC		500	kHz
Dynamic Nonlinearity			±0.002		%FSR
Total Harmonic Distortion (THD)	f_{IN} = 20kHz (–0.3dB)		0.00068		%
	f_{IN} = 199kHz (–0.2dB)		0.0078		%
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 20 kHz (–0.3dB)		107.1		dB
	f_{IN} = 199kHz (–12dB)		93.8		dB
Two-Tone Intermodulation Distortion (IMD)	f_1 = 195kHz (–6.5dB), f_2 = 200kHz (–6.5dB)		–81.4		dBC
	f_1 = 195kHz (–12.5dB), f_2 = 200kHz (–12.5dB)		–86.2		dBC
Signal-to-Noise-Ratio (SNR)	f_{IN} = 5kHz (–0.5dB)		93		dB
Total Power Dissipation	Operating		2.8	3.25	W

MECHANICAL (ADC701)

H Package— Metal and Ceramic



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	2.075	2.115	52.71	53.72
B	1.080	1.100	27.43	27.94
C	.145	.175	3.68	4.45
D	.018 TYP		0.46 TYP	
F	.040 TYP		1.02 TYP	
G	.100 TYP		2.54 TYP	
H	.093	.103	2.36	2.62
J	.020 BASIC		0.51 BASIC	
K	.205 BASIC		5.21 BASIC	
L	.900 BASIC		22.86 BASIC	
N	.015	.035	0.38	0.89

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

PIN ASSIGNMENTS (ADC701)

1	Bit 1/9 (Bit 1 = MSB)	40	$-V_{DD1}$ (–5V) Digital
2	Bit 2/10	39	Common (Analog)
3	Bit 3/11	38	$+V_{DD1}$ (+5V) Analog
4	Bit 4/12	37	Reference (Gain) Adjust
5	Bit 5/13	36	+10V Reference Output[2]
6	Bit 6/14	35	Common (Reference)
7	Bit 7/15	34	DNC
8	Bit 8/16	33	Common (Analog)
9	DNC[4]	32	+10V Reference Input[2]
10	$+V_{DD2}$ (+5V) Digital	31	Input D [1]
11	Common (Digital)	30	Input C [1]
12	Data Strobe	29	Common (Signal)
13	High/Low Byte Select	28	Input B [1]
14	Convert Command	27	Input A [1]
15	Sample/Hold Control[3]	26	$-V_{CC}$ (–15V) Analog
16	Common (Digital)	25	Common (Power)
17	Common (Digital)	24	$+V_{CC}$ (+15V) Analog
18	Clock Adjust	23	DNC
19	Common (Digital)	22	Offset Adjust
20	$+V_{DD2}$ (+5V) Digital	21	Offset Adjust

NOTES: (1) Refer to Input Connection Table. (2) Reference Input is normally connected to Reference Output, unless an external 10V reference is used. (3) Sample/Hold Control goes high to activate Hold mode. (4) DNC = Do Not Connect.

ADC701 INPUT CONNECTION TABLE

INPUT RANGE:	CONNECT V_{IN} TO	CONNECT REF IN TO
0 to +10V	Input A and Input D	—
±10V	Input A	Input D
±5V	Input A and Input B	Input D
–10V to 0	Input A and Input B	Input C and Input D
0 to +5V	Input B and Input C	—

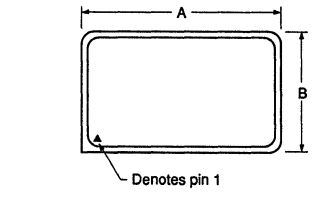
ABSOLUTE MAXIMUM RATINGS (ADC701)

$\pm V_{CC}$	±18V
$\pm V_{DD1}$, $+V_{DD2}$	±7V, +7V
Analog Input	$\pm V_{CC}$
Logic Input	–0.5V to ($+V_{DD2}$ + 0.3V)
Logic Output	±25mA
Case Temperature	+150°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +165°C
Power Dissipation	3W

Stresses above these ratings may permanently damage the device.

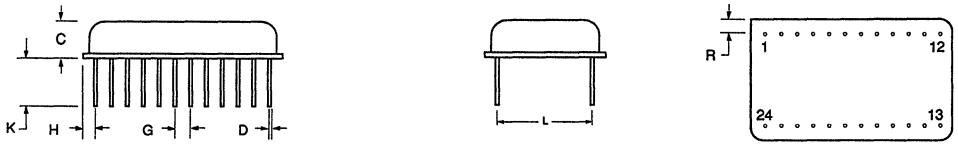
MECHANICAL (SHC702)

M Package— Metal



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.79	.810	20.07	20.57
C	.170	.25	4.32	6.35
D	.016	.021	.41	.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin material and plating composition conform to method 2003 (solderability of MIL-STD-883 (except paragraph 3.2)



PIN ASSIGNMENTS (SHC702)

1	Sample/Hold Output	24	$+V_{cc}$ (+15V) Analog
2	NC[3]	23	Common (Power)
3	NC	22	$-V_{cc}$ (–15V) Analog
4	NC	21	Common (Analog)
5	NC	20	NC
6	NC	19	NC
7	NC	18	NC
8	NC	17	Buffer Amp Input[2]
9	$+V_{DD1}$ (+5V) Analog	16	NC
10	Common (Digital)	15	Common (Signal)
11	Hold Input[1]	14	Buffer Amp Output
12	$\overline{\text{Hold}}$ Input[1]	13	Analog Input

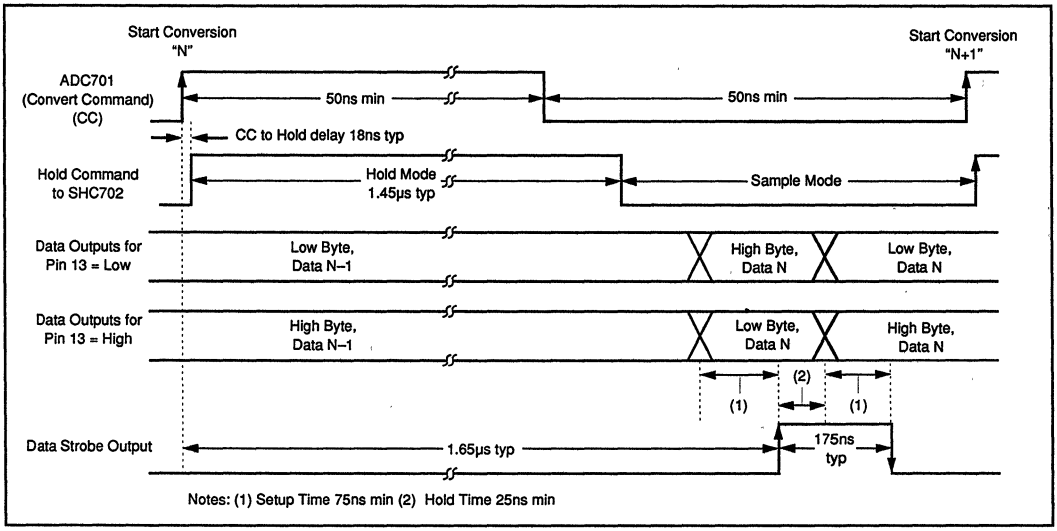
NOTES: (1) Hold mode is activated only when pin 12 is low and pin 11 is high. For normal use with ADC701, pin 12 is grounded and pin 11 is connected to ADC701 Sample/Hold control (ADC701 pin 15). (2) If the buffer amp is not used, pin 17 should be grounded. (3) NC = No Internal Connection.

ABSOLUTE MAXIMUM RATINGS (SHC702)

$\pm V_{cc}$	±18V
$+V_{DD1}$	+7V
Analog and Buffer Inputs	$\pm V_{cc}$
Outputs	Indefinite Short to Common
Logic Inputs	–0.5V to ($+V_{DD1}$ + 0.3V)
Case Temperature	+150°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +165°C
Power Dissipation	1.5W

Stresses above these ratings may permanently damage the device.

SYSTEM TIMING DIAGRAM



ADC701 DIGITAL I/O

Refer to the system timing diagram (page 5). The conversion process is initiated by a rising edge on the Convert Command input. This will immediately bring the Sample/Hold Command output to a logic high state (HOLD mode).

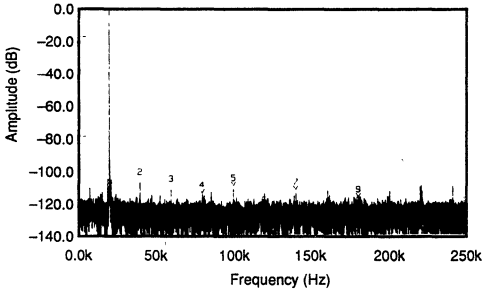
After the ADC701 conversion is completed (approximately 1.5µs after the Convert Command edge), the Sample/Hold Command falls to a low state, enabling the sample/hold to begin acquisition of the next input sample. However, the ADC701 internal clock continues to run so that the output data may be processed.

There are two methods of reading data from the ADC:

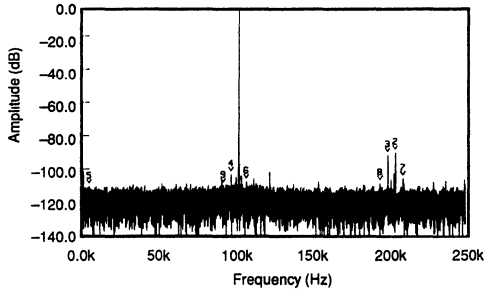
1) Strobed Output—This will usually be the easiest and fastest method. The data are presented sequentially as high and low bytes of the total 16 bit word. The sequence HIGH-LOW or LOW-HIGH is controlled by the state of the High/Low Byte Select input (Pin 13). The first byte is valid on the rising edge of the Data Strobe output; the second byte is valid on the falling edge.

2) Polled Output—With this method the user waits until the Data Strobe output falls, and then manually selects high and low output data by means of the High/Low Byte Select input (Pin 13). This polling procedure may be carried out during the subsequent ADC conversion cycle, but two precautions must be observed: First, the user should avoid switching the High/Low Byte Select immediately before or after the next Convert Command. This will prevent digital switching noise from coupling into the system at the instant of analog sampling. Second, the polling sequence must be completed before the ADC begins to strobe out data from the subsequent conversion.

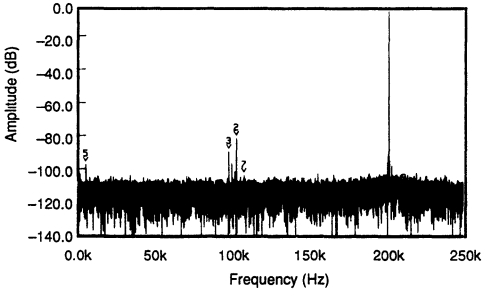
TYPICAL DYNAMIC PERFORMANCE (ADC701/SHC702)[1]



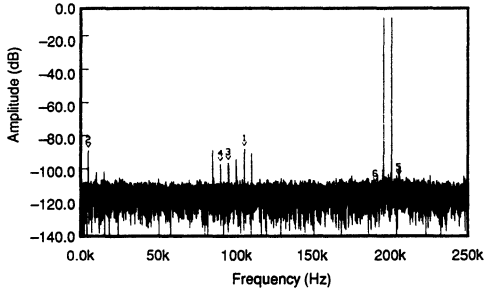
Input Frequency	19.9890136719 kHz		
Fundamental	–0.3 dB	4th Harmonic	–115.6 dB
2nd Harmonic	–107.5 dB	5th Harmonic	–111.2 dB
3rd Harmonic	–111.5 dB	6th Harmonic	–124 5 dB



Input Frequency	100.982666016 kHz		
Fundamental	–0.5 dB	4th Harmonic	–102.5 dB
2nd Harmonic	–89.1 dB	5th Harmonic	–110.2 dB
3rd Harmonic	–90.5 dB	6th Harmonic	–106.8 dB



Input Frequency	199.005126953 kHz		
Fundamental	–0.7 dB	4th Harmonic	–111 5 dB
2nd Harmonic	–81.4 dB	5th Harmonic	–97.0 dB
3rd Harmonic	–89.4 dB	6th Harmonic	–112.5 dB



Frequency 1	194.976806641 kHz		
Frequency 2	199.981689453 kHz		
f_1	–6.8 dB	3> $f_1 + 2f_2$	–96.0 dB
f_2	–6.4 dB	4> $2f_1 + f_2$	–96.8 dB
1> $f_1 + f_2$	–87.7 dB	5> $f_1 - 2f_2$	–104.9 dB
2> $f_1 - f_2$	–88.8 dB	6> $2f_1 - f_2$	–109.0 dB

NOTE: (1) Sampling Rate = 500.0000000000 kHz. 16,384 point FFT, non-windowed. Noise floor limited by synthesized generators.

BURR-BROWN®

ADC803

High-Speed ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 12-BIT RESOLUTION
- ±0.012% LINEARITY ERROR MAXIMUM (C GRADE)
- NO MISSING CODES −55°C to +125°C (S GRADE)
- HIGH SINAD RATIO: 72dB
- LOW HARMONIC DISTORTION: −73dB
- CONVERSION TIME: 500ns, 8 bits
  670ns, 10 bits
  1.5μs, 12 bits

DESCRIPTION

The ADC803 is a high speed successive approximation analog-to-digital converter utilizing state-of-the-art IC and laser-trimmed thin film components.

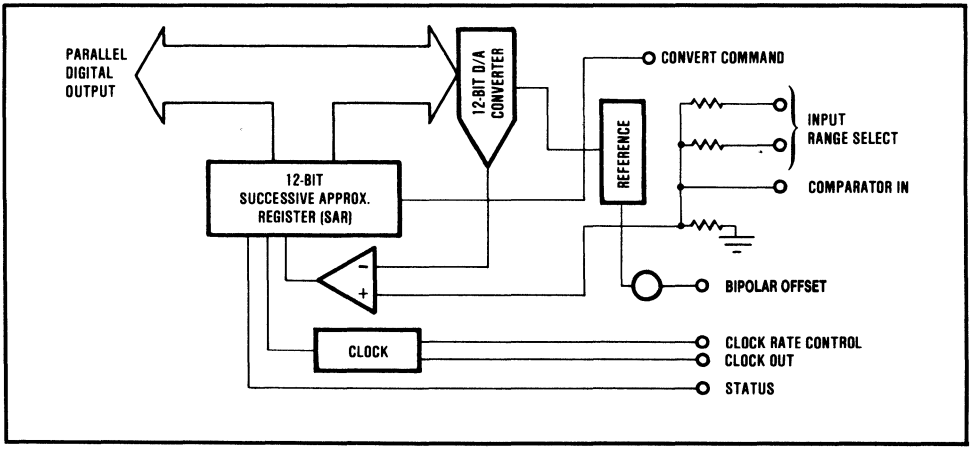
It is complete with internal reference, clock, and comparator and is packaged in a 32-pin metal package. Conversion time is set at the factory to 1.5μs.

With user-adjusted conversion time set at 1μs, ±1LSB accuracy can be achieved. The gain and offset errors may be externally trimmed to zero.

Internal scaling resistors are provided for the selection of analog signal input ranges of 0V to -10V, ±5V, and ±10V.

Output codes available are complementary binary for unipolar inputs and bipolar offset binary for bipolar inputs.

All digital inputs and outputs are TTL-compatible. Power supply requirements are ±15V and +5V.



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PDS-493D

SPECIFICATIONS

ELECTRICAL

At +25°C, rated power supplies, 1.5μs conversion time, and after 6-minute warm-up unless otherwise noted.

MODEL	ADC803CM			ADC803BM			ADC803SM			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			12			12	Bits
INPUTS										
ANALOG										
Voltage Ranges Bipolar		±5, ±10			*			*		V
Unipolar		0 to −10			*			*		V
Impedance −10V to 0V, ±5V		1.4			*			*		kΩ
±10V		2.4			*			*		kΩ
DIGITAL										
Convert Command		Negative pulse 50ns wide (min) trailing edge (0 to 1) initiates conversion								
Logic Loading			4			*		*		TTL Loads
TRANSFER CHARACTERISTICS										
ACCURACY										
Gain Error[1]		±0.04	±0.1		±0.08	±0.2		+0.04	+0.1	%
Offset Error[1] Unipolar		±0.05	±0.2		±0.07	±0.3		*	*	% of FSR[2]
Bipolar		±0.02	±0.1		*	±0.2		*	*	% of FSR
Linearity Error										
1.5μs Conversion Time		±0.009	±0.012			±0.020		±0.012	±0.015	% of FSR
1.0μs Conversion Time		±0.015	±0.020		±0.020					% of FSR
Differential Linearity Error										
1.5μs Conversion Time		±0.012	±0.015			±0.020		*	*	% of FSR
1.0μs Conversion Time			±0.024		±0.024			*		% of FSR
Inherent Quantization Error		1/2			*			*		LSB
POWER SUPPLY SENSITIVITY										
Gain and Offset +15VDC		±0.0036			*			*		% of FSR/%V_{CC}
−15VDC		±0.0005			*			*		% of FSR/%V_{CC}
+5VDC		±0.001			*			*		% of FSR/%V_{DD}
Conversion Time +15VDC		±0.7			*			*		%/%V_{CC}
−15VDC		None			*			*		%/%V_{CC}
+5VDC		±0.8			*			*		%/%V_{DD}
CONVERSION TIME										
Factory Set	1.3		1.5	*		*	*		*	μs
Range of Adjustments	0.8		2.2	*		*	*		*	μs
DRIFT										
Gain		±10	±30		±15	*		*	*	ppm of FSR/°C
Offset Unipolar		±2	±7		±3	*		*	*	ppm of FSR/°C
Bipolar		±3	±10		±5	*		*	*	ppm of FSR/°C
Linearity Error										
−25°C to +85°C										
1.5μs Conversion Time		±0.012	±0.018			±0.024			*	% of FSR
1.0μs Conversion Time		±0.015			±0.020				*	% of FSR
−55°C to +125°C										
1.7μs Conversion Time, max[4]								±.015	±.024	% of FSR
Differential Linearity Error										
−25°C to +85°C										
1.5μs Conversion Time		±0.012	±0.018			±0.024				% of FSR
1.0μs Conversion Time		±0.015			±0.024					% of FSR
−55°C to +125°C										
1.7μs Conversion Time, max[4]								±.015	±.024	% of FSR
Conversion Time		±0.1			*			*		% of FSR
No Missing Code Temp Range										
1.5μs Conversion Time	−25		+85	*		*				°C
1.7μs Conversion Time, max[4]							−55		+125	°C

ADC803 dynamic performance characteristics are described in a report titled "Analogue-to-Digital Converter Performance Tests Using the Fast Fourier Transform" by R. A. Belcher, University College of Swansea, Wales, U.K. (available from Burr-Brown on letterhead request)

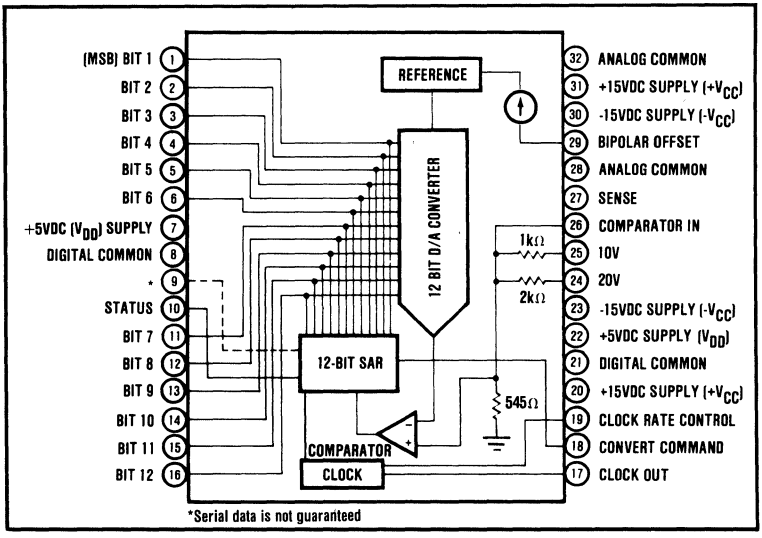
ELECTRICAL (CONT)

MODEL	ADC803CM			ADC803BM			ADC803SM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT										
DIGITAL DATA										
Parallel										
Output Codes Unipolar	Complementary Straight Binary				*			*		
Bipolar	Bipolar Offset Binary				*			*		
Output Drive	6			*			*			TTL Loads
Status	Logic "1" during Conversion				*			*		
Status Output Drive	6			*			*			TTL Loads
Internal Clock										
Clock Output Drive	3			*			*			TTL Loads
Frequency (without external clock adjustment)		8			*			*		MHz
POWER SUPPLY REQUIREMENTS										
Power Consumption										
Rated Voltage Analog ($\pm V_{CC}$)	±14 25	±15 0	±15 75	*	*	*	*	*	*	VDC
Digital (V_{DD})	+4 75	+5 0	+5 25	*	*	*	*	*	*	VDC
Supply Drain +15V		+27	+32		*	*		*	*	mA
−15V		−38	−55		*	*		*	*	mA
+5V		+180	+210		*	*		*	*	mA
TEMPERATURE RANGE (AMBIENT)										
Specification	−25		+85	*		*	−55		+125	°C
Storage	−55		+125	*		*	*		*	°C

*Same specification as for ADC803CM

NOTES (1) Adjustable to zero See Optional Gain and Offset Adjustment section (2) FSR means Full Scale Range For example, unit connected for ±10V has 20V FSR (3) See Optional Clock Rate Control section For faster conversion time at less resolution, see section on External Short Cycle (4) Conversion time is factory-set at approximately 1 4μs at +25°C As temperature increases, the conversion time increases At +125°C the conversion time will be no more than 1 7μs No Missing Codes is guaranteed over −55°C to +125°C provided the conversion time is allowed to increase with temperature

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

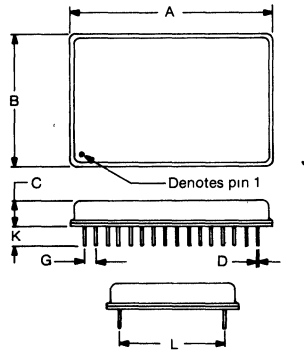
Analog Supply Voltage To Analog Common	±18V
Digital Supply Voltage To Digital Common	+7V
Digital Controls Inputs	+5 5V
Analog Inputs	±15V
Operating Temperature Ambient	+125°C
Case	+135°C
Storage Temperature	+125°C

ORDERING INFORMATION

ADC803 X M Q

- Basic Model Number
- Performance Grade Code
  - B, C = −25°C to +85°C
  - S = −55°C to +125°C
- Package Code
  - M = Metal DIP
- Reliability Screening
  - Q = Q-Screened

MECHANICAL



Pin numbers shown for reference only
Numbers may not be marked on package

Pin 1 can be identified from bottom of unit by either a contrasting color of glass seal or a square corner Case is tied to Digital Common
NOTE Leads in true position within 0 10" (0 25mm) R at MMC at seating plane Pin 8 connected to case

PINS Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3 2)
CASE Kovar, Nickel plated
HERMETICITY Gross Leak Test
MATING CONNECTOR 2302MC Set of two 16-pin strips
WEIGHT 13 grams (0 46 oz)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 720	1 760	43 69	44 70
B	1 120	1 160	28 45	29 46
C	170	250	4 32	6 35
D	016	021	0 41	0 53
G	100 BASIC		2 54 BASIC	
H	100	140	2 54	3 56
K	150	300	3 81	7 62
L	900 BASIC		22 86 BASIC	
R	100	140	2 54	3 56

THEORY OF OPERATION

The accuracy of a successive approximation analog-to-digital converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry matching and tracking properties of the ladder and scaling networks, power supply rejection, reference errors and the dynamic errors of the DAC and comparator. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the transfer function (Figure 1) about the zero point and Offset drift shifts the transfer function left or right over the operating temperature range. Linearity error is not adjustable but it is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the best fit straight line transfer function of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB. The ADC803 is guaranteed to have no missing codes over the specified temperature range.

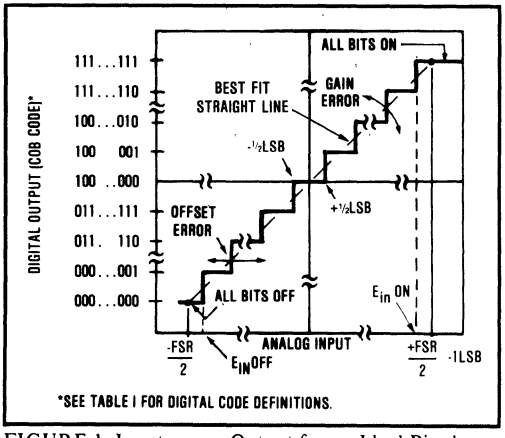


FIGURE 1. Input versus Output for an Ideal Bipolar A/D Converter.

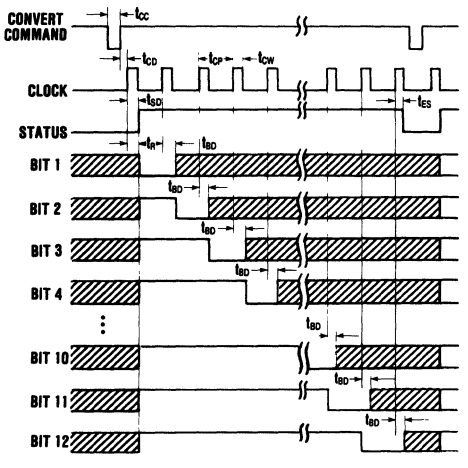
TIMING CONSIDERATIONS

The timing diagram (Figure 2) shows the relationship between the convert command, clock and outputs. The digital output word is positive true logic for bipolar operation and complementary logic for unipolar operation.

The following are some important notes on the ADC803 timing. The times given are typical unless otherwise noted. Nominal maximum and minimum times are also given in Figure 2.

1. When power is first applied, the status of the ADC803 will be undetermined. A CONVERT COMMAND must be applied to initialize the ADC803.
2. The CONVERT COMMAND must be low at least 50nsec prior to the "0" to "1" edge that starts a conversion.
3. The clock runs continuously when the initial CONVERT COMMAND goes high and whenever the CONVERT COMMAND is high thereafter. It does not run when CONVERT COMMAND is low. It may be beneficial to keep CONVERT COMMAND low except during conversions to limit the digital noise induced in the ground and power supply lines.
4. The clock starts 25ns after the "0" to "1" transition of the CONVERT COMMAND.
5. **Parallel Output Data:** The Successive Approximation Register (SAR) is reset 26ns after the leading edge of the first clock period in the conversion cycle. The MSB is set to logic "0" and all other bits are set to logic "1". The bits are determined in succession starting with the MSB, Bit 1, as shown in Figure 2. Each bit will be valid 26ns after its corresponding clock pulse.

   The falling edge of the STATUS signal should not be used to strobe parallel data out of the ADC803



Time Period	Min* (ns)	Max* (ns)
t_{CC}	50	—
t_{CD}	15	40
t_{CP}**	100	125
t_{CW}	17	25
t_{SD}	10	38
t_R	10	38
t_{BD}	10	38
t_{ES}	10	38

*Nominal
**Without external adjustment

FIGURE 2. ADC803 Timing Diagram.

directly. The table in Figure 2 indicates that the falling edge of STATUS may occur prior to bit 12 data becoming valid.

6. STATUS goes high 26ns after the leading edge of the first clock pulse and goes low 18ns after the leading edge of the last clock pulse.
7. Bit 12 will become valid at about the same time STATUS goes low and a new conversion can be initiated at anytime after the output data has been read.
8. The converter may be restarted during a conversion. When CONVERT COMMAND makes a "0" to "1" transition after the minimum set-up time, the SAR will be reset and a new conversion will start regardless of the state of the converter prior to the CONVERT COMMAND being received.

Figures 3, 4, and 5 are photographs of the actual pulse shapes and relationships.

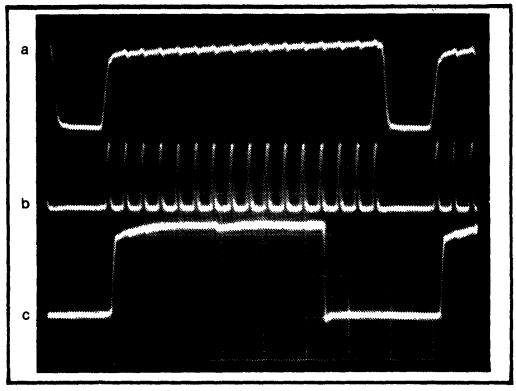


FIGURE 3. Photo of (a) Convert Command, (b) Clock, and (c) Status (200ns/div).

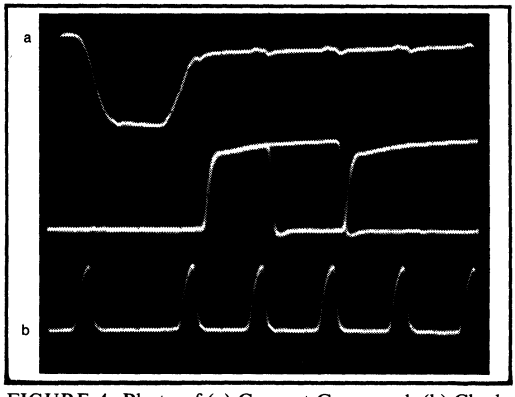


FIGURE 4. Photo of (a) Convert Command, (b) Clock (50ns/div).

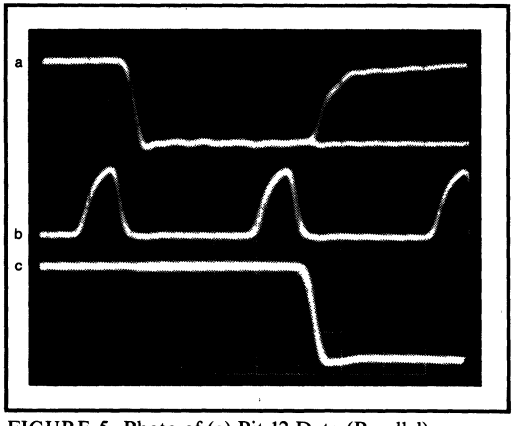


FIGURE 5. Photo of (a) Bit-12 Data (Parallel), (b) Clock, and (c) Status (20ns/div).

DIGITAL CODES
Parallel Data

Two binary codes are available on the ADC803 parallel output; they are complementary straight binary (Logic "0" true) for unipolar input signal ranges and bipolar offset binary (Logic "1" true) for bipolar input signal ranges. Binary two's complement may be obtained for bipolar input ranges by inverting the MSB. It should be noted that for unipolar input ranges -10 volts is full scale.

Table I shows the LSB, transition values, and code definitions for each possible analog signal range.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Analog Input Voltage Range	±10V	±5V	0 to -10V
Code Designation	BOB(1) or BTC(2)	BOB or BTC	CSB(3)
One Least Significant Bit (LSB)	4 88mV	2 44mV	2 44mV
Transition Values MSB LSB(4)			
000...000	-10V + 1/2LSB	-5V + 1/2LSB	-10V + 3/2LSB
000...001			
011...111	-1/2LSB	-1/2LSB	-5V + 1/2LSB
100...000			
111...110	+10V - 3/2LSB	+5V - 3/2LSB	−1/2LSB
111. .111			

NOTES 1 BOB = Bipolar Offset Binary
2 BTC = Binary Two's Complement (obtained by inverting the most significant bit (pin 1))
3 CSB = Complementary Straight Binary
4 Voltages given are the nominal value for the transition from the next lower code

Serial Data (NRZ)

ADC803 serial data operation is not guaranteed. To operate in serial output mode a pin-for-pin replacement ADC806 is recommended.

DISCUSSION OF SPECIFICATIONS

The ADC803 is specified to meet critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are Linearity, Drift, Gain and Offset errors, and Conversion speed effects on accuracy. This ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.05% of FSR at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 10, 11, and 12.

ACCURACY VERSUS CONVERSION TIME

In successive approximation A/D converters, the conversion time affects Linearity and Differential Linearity errors. Conversion time and its effect on Linearity and Differential Linearity errors for the ADC803 are shown in Figure 6.

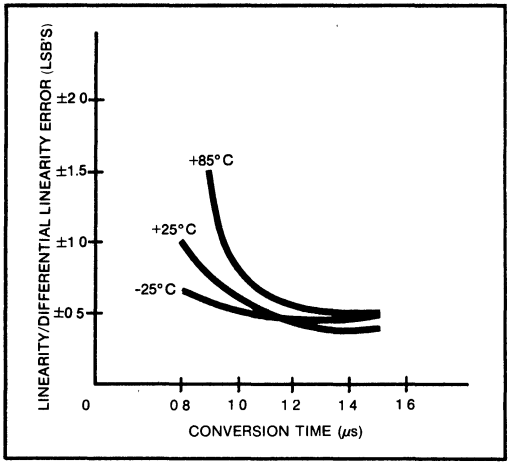


FIGURE 6. Linearity and Differential Linearity Error versus Conversion Time.

POWER SUPPLY SENSITIVITY

Changes in the DC power supply voltages will affect accuracy. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling, and Figure 7.

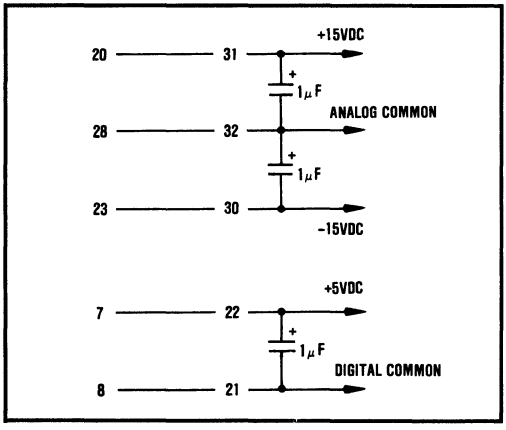


FIGURE 7. Recommended Power Supply Decoupling.

LINEARITY ERROR

Linearity error is not adjustable by the user. Linearity is the deviation of an actual bit transition from the best fit straight line value at any level over the range of the A/D converter.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity describes the step size between transition values. A Differential Linearity error of

±1/2LSB indicates that the size of any step may not vary from 1LSB by more than ±1/2LSB.

ENVIRONMENTAL SCREENING

Q screening is now available for all models of the ADC803 family. The Q-screened versions have the same specifications as the unscreened versions listed in the Specifications table.

Q Screening

Burr-Brown Q-screened models are environmentally-screened versions of our standard industrial products, designed to provide enhanced reliability. The screening, tabulated below, is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient method of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those listed below. Burr-Brown's detailed procedures may vary slightly from those of MIL-STD-883.

SCREENING FLOW FOR ADC803Q

Screen	Method Burr-Brown or MIL-STD-883	Condition
Internal Visual	Burr-Brown QC4118	
High Temperature Storage (Stabilization Bake)	1008	B (150°C, 24hr)
Temperature Cycling	1010	B (10cy, −55°C to +125°C)
Constant Acceleration	2001	(2000G, Y1 axis)
Burn-in ADC803BMQ, CMQ ADC803SMQ	1015	D (160 hrs, +85°C) (160 hrs, +125°C)
Electrical Test	Burr-Brown Test Specification	
Hermeticity Fine Leak	1014	A1 or A2 (Helium, 5×10^{-7}cc/s)
Gross Leak	1014	C
Final Electrical	Burr-Brown Test Specification	
External Visual	Burr-Brown QC5150	

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

The ADC803 is a high speed analog-to-digital converter which requires more layout precautions than general purpose products.

The ADC803 has two pins for analog common, two pins for digital common, and two pins for each power supply input. Each pair of these pins must be connected together externally. The connection between the digital supply pins and the connection between the digital common pins must be as short as possible. The analog and digital commons are not connected together internally in the ADC803, but should be connected together externally to a ground plane.

Connecting all commons to a ground plane at the ADC803 is the best method to minimize noise and dissipate heat. Pin 8 (Digital Common) is internally connected to the case.

The ADC803 also has an analog common Sense input (pin 27) for the analog input. This sense pin must be connected to analog common as close to the input signal source as possible or connected to the ground plane. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. Special attention should be taken to ensure that the clock noise on the +5V supply line does not couple into the analog inputs.

The Comparator input (pin 26) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by analog common or ±15VDC supply patterns. The Clock Output (pin 17) is sensitive to stray capacitance; capacitance on this pin could alter the clock wave shape.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 1μF tantalum capacitors as shown in Figure 8 to obtain noise-free operation. These capacitors should be located close to the ADC.

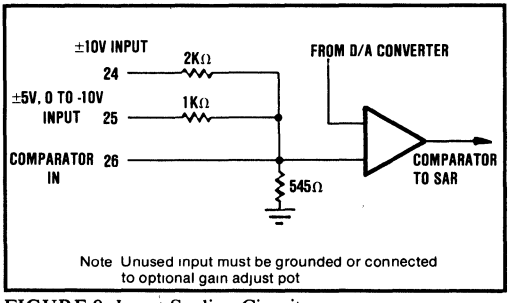


FIGURE 8. Input Scaling Circuit.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signals as shown in Table II. See Figure 8 for circuit details.

OUTPUT DRIVE

All ADC803 outputs except the clock will drive six TTL loads; the clock will drive three TTL loads. If long digital lines must be driven, external logic buffers are required particularly for the clock which is sensitive to capacitive loading.

TABLE II. ADC803 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 29 To	With Gain Adjust	Connect Pin 24 To	Connect Pin 25 To
±10V	BOB or BTC*	26	Yes	40Ω resistor in series with input signal	Gain Adjust Potentiometer
			No	Input Signal	Analog Common
±5V	BOB or BTC*	26	Yes	Gain Adjust Potentiometer	10Ω resistor in series with input signal
			No	Analog Common	Input Signal
0 to −10V	CSB	Analog Common	Yes	Gain Adjust Potentiometer	10Ω resistor in series with input signal
			No	Analog Common	Input Signal

*Obtained by inverting MSB (pin 1) externally

INPUT IMPEDANCE

The source impedance to the ADC803 should be low, such as the output of an op amp, to avoid any errors due to the relatively low input impedance of the ADC803.

If this impedance is not low, a buffer amplifier should be added between the input signal and the ADC803 input as shown in Figure 9.

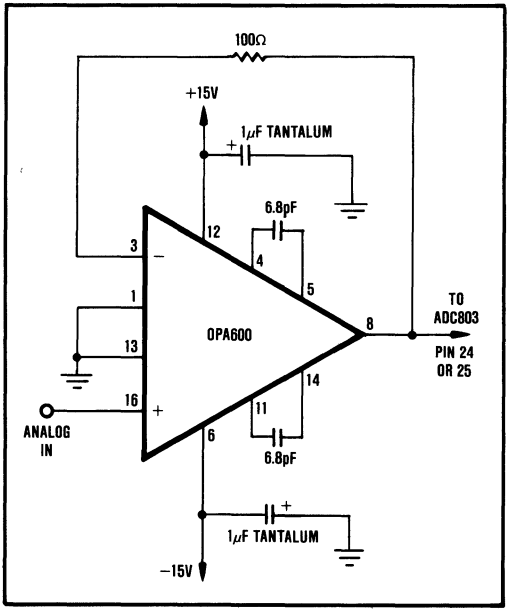


FIGURE 9. Source Impedance Buffering.

A common problem with successive approximation A/D converters is the transients in input current caused by the comparator input being switched back and forth. This requires a fast settling amplifier to drive the input.

The ADC803 comparator is connected in a differential mode (see Figure 8), greatly reducing the size of the input transients. The user, therefore, may use a fast settling wideband operational amplifier to drive the ADC803. The small signal settling time of the amplifier should be less than 100ns.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external trim potentiometers connected to the ADC as shown in Figures 10, 11, and 12. For proper gain adjust range a series resistor must be connected to the analog input pin as specified in Table II and shown in Figures 11 and 12. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. All resistors should be ±1% metal film or better. If the Offset adjust is not used, pin 26 should be left open except for bipolar operation when it is connected to pin 29. If the Gain adjust is not used, the unused input (pin 24 or 25) must be grounded to meet specified gain accuracy.

Adjustment Procedure

Refer to Table I for LSB voltages and transition values.

Unipolar offset - connect the offset potentiometer and resistors as shown in Figure 11, sweep the input through the end point transition voltage, from 111...110 to 111...111. Adjust the Offset potentiometer until the actual end point transition voltage occurs at -1/2LSB.

Bipolar offset - connect the offset potentiometer and resistors as shown in Figure 10. Sweep the input through zero and adjust the offset potentiometer until the transition from 0111 1111 1111 to 1000 0000 0000 occurs at −1/2LSB.

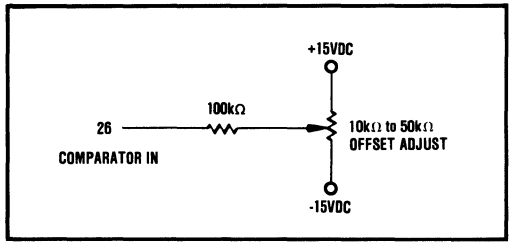


FIGURE 10. Optional Offset Adjust

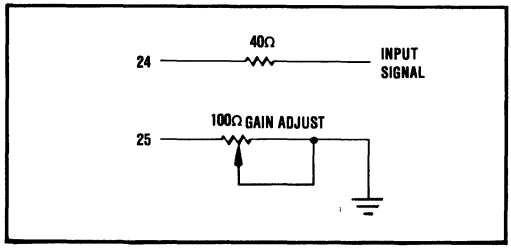


FIGURE 11. Optional Gain Adjust for ±10V Bipolar Operation.

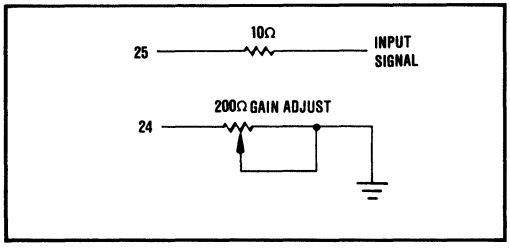


FIGURE 12. Optional Gain Adjust for ±5V Bipolar or 0 to -10V Unipolar Operation.

Gain - connect the Gain potentiometer as shown in Figure 11 or 12. Sweep the input through the end point transition voltage that should cause an output transition from 000...000 to 000...001. Adjust the Gain potentiometer until this transition occurs at the correct end point transition voltage as given in Table I.

OPTIONAL CLOCK RATE CONTROL

The clock is factory-set for a conversion time between 1.3μs and 1.5μs. By use of the optional Clock Rate Control as shown in Figure 13, the Conversion time can be adjusted down to 0.8μs for 12-bit resolution. If the optional Clock Rate Control is not used, pin 19 should be left open. Figure 14 shows Conversion Time versus Clock Rate Control voltage and Figure 6 shows Differential Linearity error versus Conversion time.

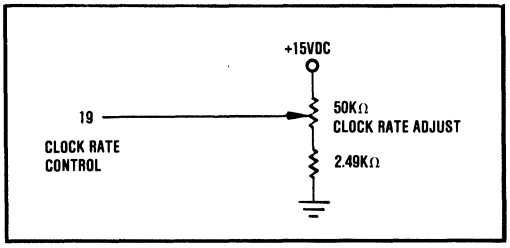


FIGURE 13. Optional Clock Rate Control.

POWER DISSIPATION

The ADC803 dissipates approximately 1.9W (typical) and the package has a case-to-ambient thermal resistance (θ_{CA}) of 25°C/W. For operation above +85°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. See Figure 15 for θ_{CA} requirements above +85°C. Improved thermal contact with the PC card copper ground plane under the case can be achieved using a silicone heat sink compound. On a 0.062" thick PC card with a 16-square-inch (minimum) area, this technique will allow operation to +100°C. Forced air plus heat sink is recommended for +125°C operation.

EXTERNAL SHORT CYCLE

If less than 12 bits of resolution is required, the cycle time of the ADC803 can be shortened with the addition of two external components as shown in Figure 16. This circuit will create a shortened status signal directly proportional

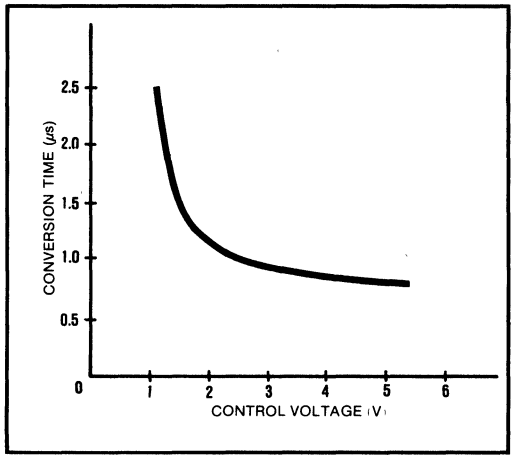


FIGURE 14. Conversion Time versus Clock Rate Control Voltage.

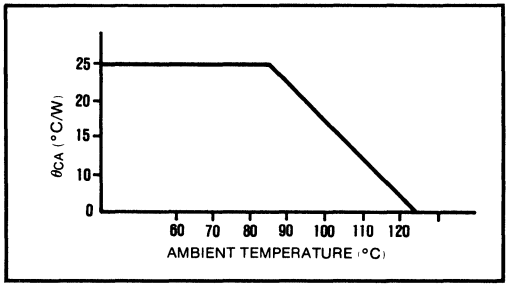


FIGURE 15. θ_{CA} Requirement Above +85°C.

to the reduction of resolution. For n bits of resolution, the n+1 bit is used to create the falling edge of the shortened status signal. It is possible to obtain the equivalent of a 10-bit converter with 670ns conversion time and an 8-bit converter with 500ns conversion time using this short cycle technique and the external clock rate control shown in Figure 13. To begin a new conversion, simply give the converter a new convert command pulse. The SAR will reset and a new conversion will begin.

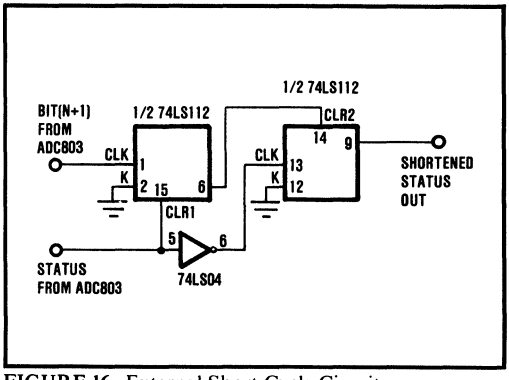


FIGURE 16. External Short Cycle Circuit.

TESTING OF THE ADC803

In order to validate the test results of the ADC803 obtained during final test, the customer must take extreme care in the design and layout of his test fixtures. Proper grounding, correct routing of analog and digital signals and power supply bypassing are crucial in achieving successful results.

ANALOG GROUND, DIGITAL GROUND, SENSE

Figure 17 shows a simplified model of the ADC depicting proper analog and digital grounding. Several analog and digital ground pins have been provided to allow for optimizing the internal layout of the ADC. As will be explained in more detail later, analog and digital grounds should be connected together only at one point by an extremely low resistive and inductive connection (a ground plane is ideal). A special analog ground called "sense" has been provided to eliminate the voltage drop that would otherwise be in the ground return of the R-2R ladder. Measuring the input signal with respect to the sense terminal makes the measurement independent of the impedance that is developed in the connection between the sense terminal and the analog ground, pin 28.

ANALOG-TO-DIGITAL CONVERTER TEST TECHNIQUE

A very effective way of determining the DC performance of an ADC is by using the "servo loop method." The block diagram of this technique is shown in Figure 18. This measurement system automatically locates the analog voltage that causes the digital output to alternate between the desired code and the adjacent code. The computer is programmed to place the desired code on the I/O bus which is one set of inputs to the digital comparator. The other set of inputs to this comparator is the digital output of the ADC. Depending upon the result of this comparison, the integrator is directed to change its output until an equilibrium state is achieved. Once in equilibrium, the DVM measures the analog input to the ADC and transmits the information to the computer via the IEEE-488 bus. The test program checks all the desired code combinations, verifying the performance of the ADC. Test time will range from 10 seconds to several minutes depending on the speed of the test program, settling time of the DVM, and number of codes to be checked.

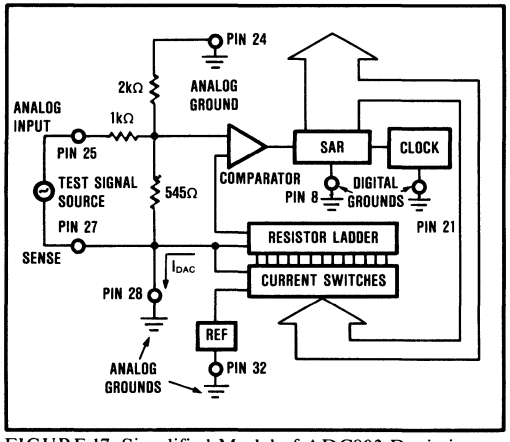


FIGURE 17. Simplified Model of ADC803 Depicting Proper Analog and Digital Ground.

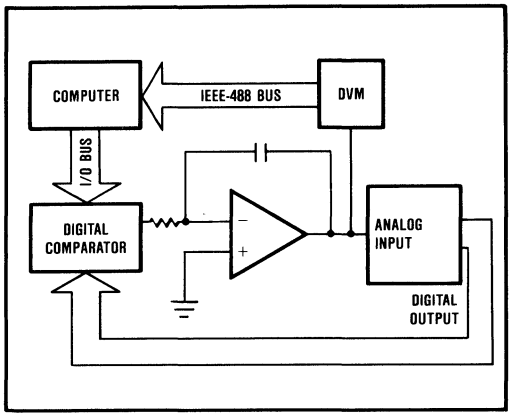


FIGURE 18. Servo Loop Analog-to-Digital Tester.

GROUND LOOPS

Figure 19 illustrates the interaction that occurs between the analog and digital grounds when an ADC is connected into a test circuit. This interaction is created by ground loops. The circuit in Figure 19 shows how ground loops are created when the ADC tester combines digital and analog portions of the circuit together—in this case, the test signal generator (analog) and the digital circuitry that detects the ADC code which corresponds to the analog signal (digital). The ground loop exists when the digital ground connection between the ADC and the tester is in parallel with the analog grounds that connect the tester with the ADC. When the connection is made in this manner some of the digital current is diverted into the analog signal return, which creates a code-dependent error signal due to the resistance in the analog signal return. This error distorts the linearity measurement and induces hysterisis. The error can be substantially reduced if the analog and digital grounds are isolated from each other in the ADC tester.

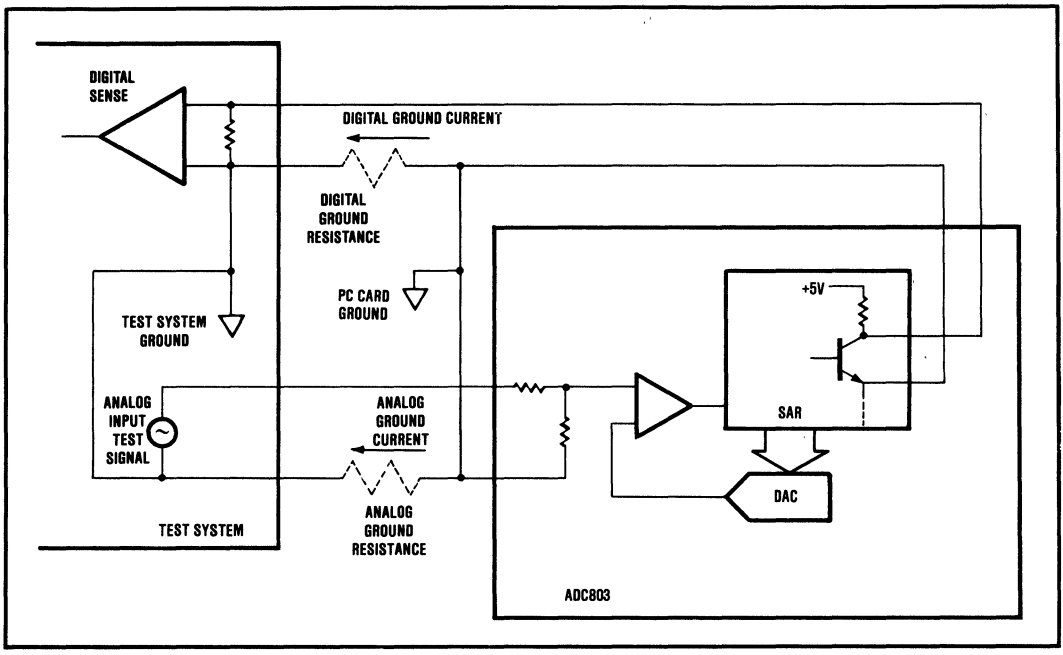


FIGURE 19. Ground Loop Interaction Between Analog and Digital Grounds When ADC Is Connected Into Test Circuit.

BEAT FREQUENCY TEST

A "beat frequency test" applied to an ADC803 with a companion sample/hold illustrates both an effective means of testing the high frequency performance of such a system and demonstrating that the ADC803 with its associated sample/hold is capable of digitizing high frequency signals cleanly. A sample/hold must be used when performing this test to hold the input of the ADC803 constant during the conversion time. Figure 20 is a block diagram of the beat frequency test setup.

The beat frequency test is useful for being able to rapidly determine whether there are any serious problems with the ADC. In this test the input frequency is set at slightly less than one-half the sampling rate. The slight difference is selected to allow the sample point to vary by 1LSB, or less, on successive samples. The data is clocked into a low frequency reconstruction DAC at one-half the sampling rate to enable viewing on an oscilloscope. Figure 21 is a photograph of the response to a full-scale input sine wave centered around the MSB and Figure 22 is a photograph of the response of a small signal sine wave centered around the MSB. For comparison, a photograph (Figure 23) is included which shows the response of the ADC803 to a 125Hz input signal which is the same as the beat frequency.

Figure 24 is the PC card layout that was used for the beat frequency test. This layout demonstrates some of the layout practices that must be followed when using a high speed ADC like the ADC803.

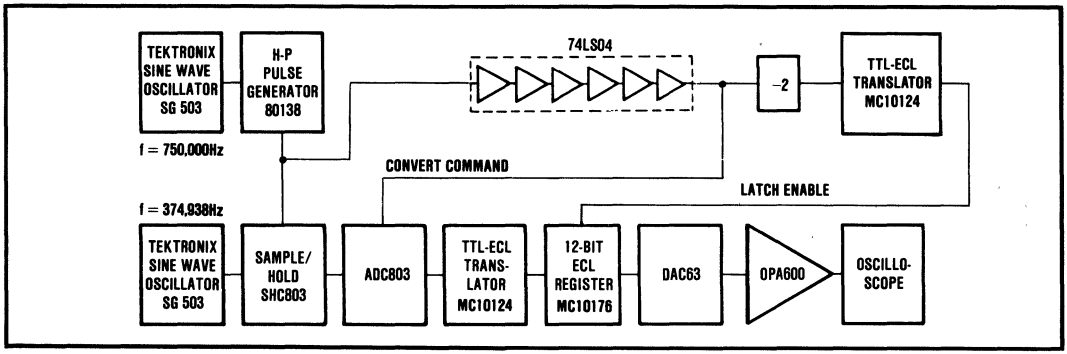


FIGURE 20. Block Diagram of Beat Frequency Test Circuit.

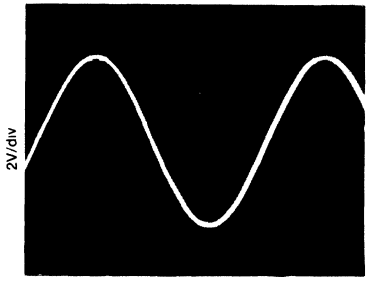


FIGURE 21. Beat Frequency Test Response of Full Scale Sine Wave Input.

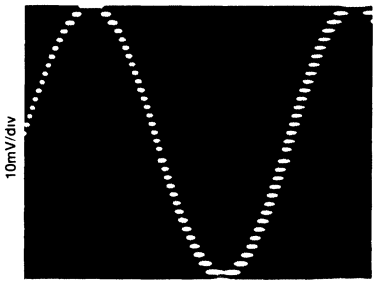


FIGURE 22. Beat Frequency Test Response of Small Signal Sine Wave Input.

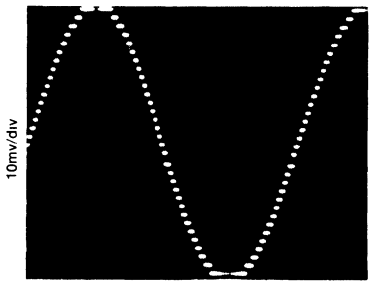
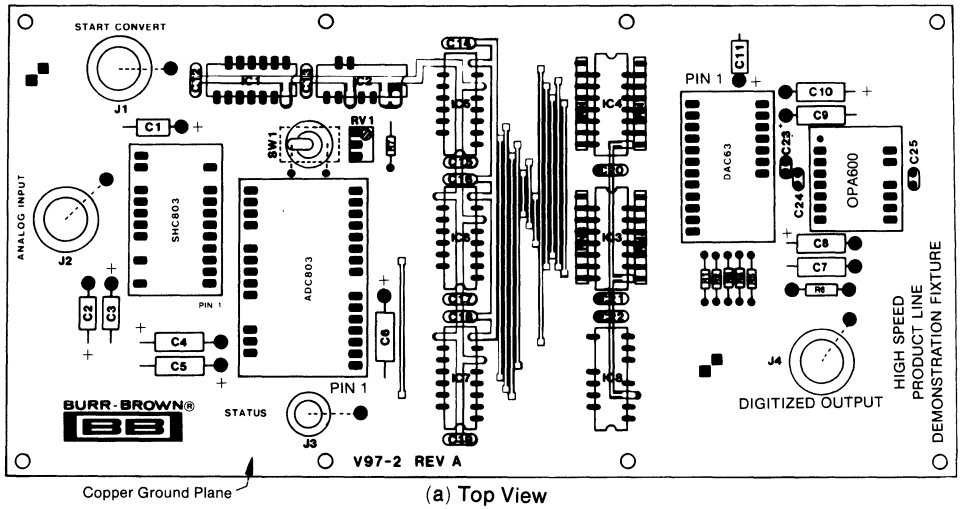
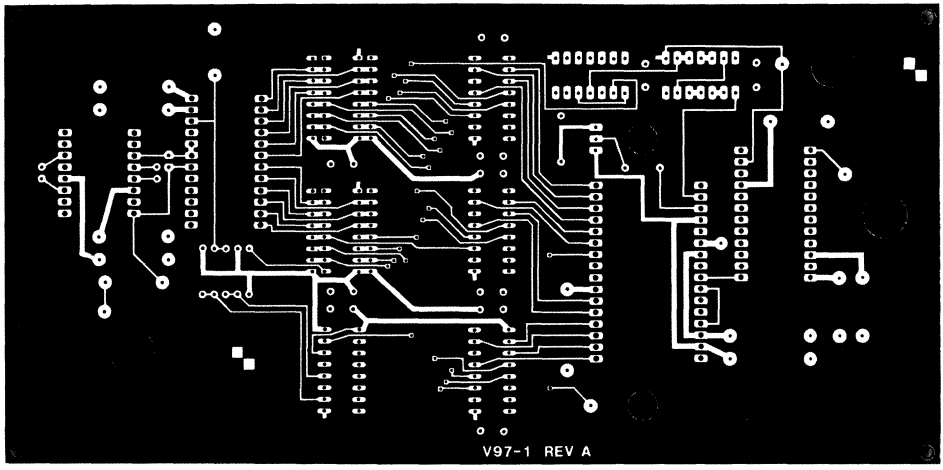


FIGURE 23. Response of Small Signal 125Hz Sine Wave Input.



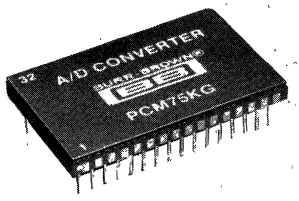
(a) Top View



(b) Bottom View

FIGURE 24. PC Board Layout for Beat Frequency Test Fixture.

BURR-BROWN®



PCM75
DESIGNED FOR AUDIO

16-Bit Hybrid ANALOG-TO-DIGITAL CONVERTER

FEATURES

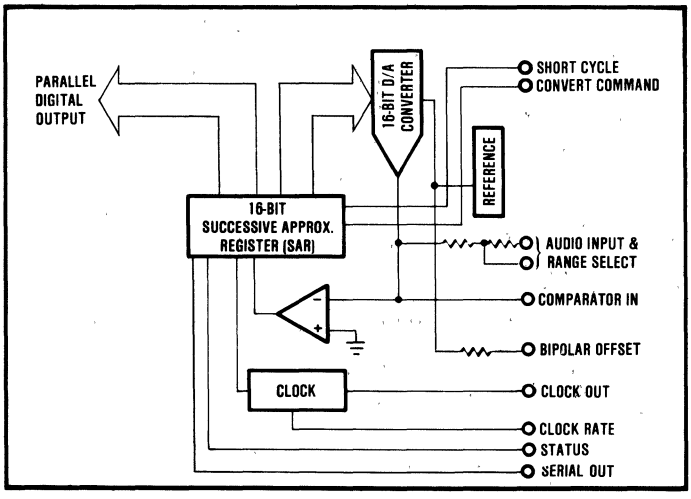
- 16-BIT RESOLUTION
- 90dB DYNAMIC RANGE
- 0.004% THD (FS Input, 16 Bits)
- 0.02% MAX THD (-15dB, 16 Bits)
- 17μs MAX CONVERSION TIME (16 Bits)
- 15μs MAX CONVERSION TIME (14 Bits)
- 10μs CONVERSION TIME (Reduced Specs)
- EIAJ STC-007-COMPATIBLE

DESCRIPTION

The PCM75 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. The PCM75 uses state-of-the-art IC and laser-trimmed thin-film components and is packaged in a bottom-brazed ceramic 32-pin dual-in-line package. The converter is complete with internal reference and clock.

The PCM75 is designed for PCM audio applications and is compatible with EIAJ STC-007 specifications.

The conversion time can be reduced from 15μs to 10μs with some increase in distortion. Distortion is specified on the data sheet to assure performance in critical audio applications.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx 910-952-1111 - Cable BBRCORP - Telex 66-6491

PDS-624A

SPECIFICATIONS

ELECTRICAL

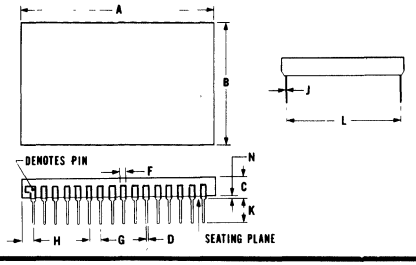
At 25°C and rated power supplies unless otherwise noted

MODEL	PCM75KG			PCM76JG			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			*	Bits
DYNAMIC RANGE[1]		90			*		dB
INPUT							
ANALOG							
Voltage Ranges, Bipolar		±2 5, ±5, ±10			*		V
Impedance (Direct Input)							
0 to +5V, ±2 5V		2 5			*		kΩ
0 to +10V, ±5V		5			*		kΩ
0 to +20V, ±10V		10			*		kΩ
DIGITAL[2]							
Convert Command		Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion)					
Logic Loading			1			*	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error		±0 1[3]			*		%
Offset Error, Bipolar		±0 1[3]			*		% of FSR[4]
Differential Linearity Error (major carry)		±0 0015			±0 003		% of FSR
Inherent Quantization Error		±1/2			*		LSB
TOTAL HARMONIC DISTORTION + NOISE[1]							
V_{IN} = ±FS at f = 400Hz							
14-Bit Resolution		0 006			0 008		%
16-Bit Resolution		0 004			0.006		%
V_{IN} = −15dB at f = 400Hz							
14-Bit Resolution		0 025			0.03	0 05	%
16-Bit Resolution		0.015	0 02		0 021		%
POWER SUPPLY SENSITIVITY							
±15VDC		0 003			*		% of FSR/%V_S
+5VDC		0.001			*		% of FSR/%V_S
CONVERSION TIME[5]							
14 Bits			15			*	µs
16 Bits			17				µs
WARM-UP TIME	5			*			min
DRIFT							
Gain			±20			*	ppm/°C
Offset, Bipolar			±15			*	ppm of FSR/°C
OUTPUT							
DIGITAL (all codes complementary)							
Parallel							
Bipolar Output Codes[6]		COB, CTC[7]			*		
Output Drive	2			*			TTL Loads
Serial Data Code (NRZ)		CSB, COB			*		
Output Drive			2			*	TTL Loads
Status		Logic "1" during conversion			*		
Status Output Drive	2			*			TTL Loads
Internal Clock: Output Drive	2			*			TTL Loads
Frequency[8]		933			*		kHz
POWER SUPPLY REQUIREMENTS							
Power Consumption		0 525			*		W
Rated Voltage: Analog	±14.5	±15	±15.5	*	*	*	VDC
Digital	+4 75	+5	+5.25	*	*	*	VDC
Supply Drain. +15VDC		+14			*		mA
−15VDC		−17			*		mA
+5VDC		+10			*		mA
TEMPERATURE RANGE							
Specification	0		+70	*		*	°C
Operating (derated specs)	−25		+85	*		*	°C
Storage	−55		+100	*		*	°C

*Specification same as PCM75KG.

NOTES. (1) The measurement of Total Harmonic Distortion + Noise (THD+N) and Dynamic Range is highly dependent on the characteristics of the sample/hold amplifier, the digital-to-analog converter, the deglitcher, and the low-pass filter. To accurately measure THD+N and Dynamic Range, the accuracy of each device should be better than 16-bit accuracy. A block diagram showing the measurement technique Burr-Brown uses is shown in Figure 6. (2) DTL/TTL compatible, i.e., Logic "0" = 0.8V max. Logic "1" = 2.0V min for inputs. For digital outputs Logic "0" = +0.4V max. Logic "1" = 2.4V min. (3) Adjustable to zero (see "Optional External Gain and Offset Adjustment"). (4) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (5) Conversion time may be shortened with "Short Cycle" set for lower resolution and with use of Clock Rate Control. See "Additional Optional Connections" section. The Clock Rate Control (pin 23) should be connected to Digital Common for specified max conversion time. Short Cycle (pin 32) should be left open for 16-bit resolution or connected to the n + 1 digital output for n-bit resolution. For example, connect Short Cycle to bit 15 (pin 15) for 14-bit resolution. (6) See Table I. CSB—Complementary Straight Binary, COB—Complementary Offset Binary, CTC—Complementary Two's Complement. (7) CTC coding obtained by inverting MSB (pin 1). (8) Adjustable with Clock Rate Control from approximately 933kHz to 1.4MHz. See Figures 14 and 15 and Table III.

MECHANICAL



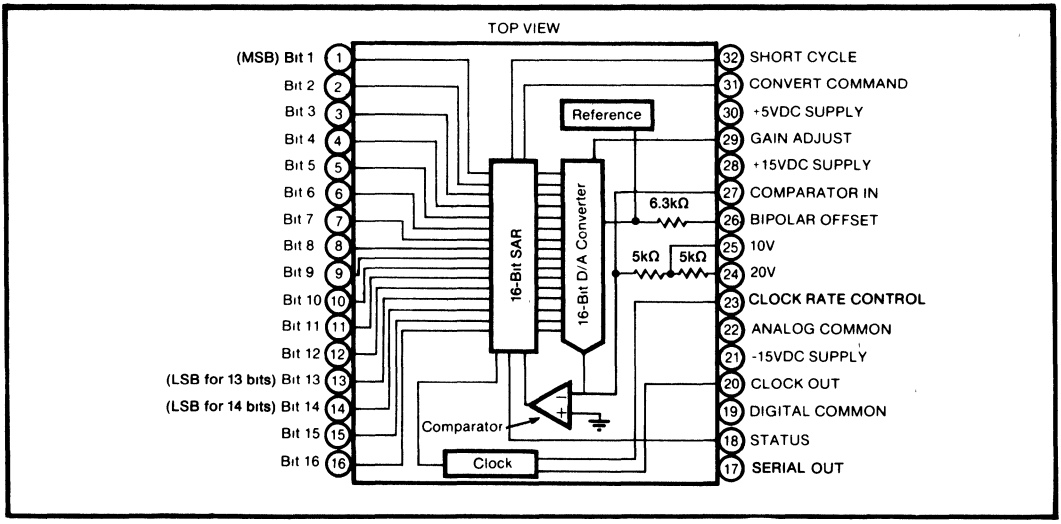
Pin numbers shown for reference only. Numbers may not be marked on package.

CASE. Ceramic
WEIGHT: 13 grams (0.46oz.)
HERMETICITY
Conforms to method 1014 condition C step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.678	1.712	42.62	43.48
B	1.079	1.101	27.41	27.97
C	.180	.210	4.57	5.33
D	.016	.020	.41	.51
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.089	.106	2.26	2.69
J	.009	.012	.23	.30
K	.200	.210	5.08	5.33
L	.900 BASIC		22.86 BASIC	
N	.015	.035	.38	.89

LEADS IN TRUE POSITION WITHIN .010" (.25MM) R @ MMC AT SEATING PLANE

CONNECTION DIAGRAM



THEORY OF OPERATION

The accuracy of a successive-approximation A/D converter is described by the transfer function shown in Figure 1. All successive-approximation A/D converters have an inherent Quantization Error ±1/2LSB. The remaining errors in the A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off), and Offset drift shifts the line left or right over the operating temperature range. Total Harmonic Distortion (THD) is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quantization Error, that is useful in Audio Applications. To be useful, THD should be specified for both high level and low level input

signals. This error is unadjustable and is the most meaningful indicator of A/D converter accuracy for Audio Applications. The resolution of an A/D converter can be expressed in terms of Dynamic Range. The Dynamic Range is a measure of the ratio of the smallest signals the converter can resolve to the full scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 x n, where n is the number of bits of resolution, or 96dB for a 16-bit converter. The actual or useful dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit.

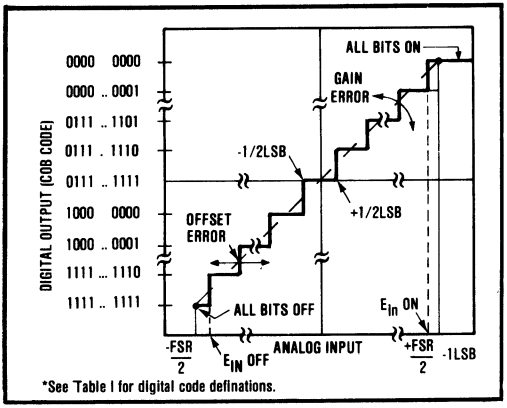


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram in Figure 2 assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output). Figures 3 and 4 are timing diagrams showing the relationship of serial data to clock and valid data to status.

DEFINITION OF DIGITAL CODES

Parallel Data

Two binary codes are available on the PCM75 parallel output, they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (pin1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 14-, 15- and 16-bit resolutions. Figure 5 shows the connections for 14-bit resolution, parallel data output, with ±5V input.

Serial Data

Two straight binary (complementary) codes are available on the serial output line; they are CSB and COB. The serial data is available only during conversion and appears with MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

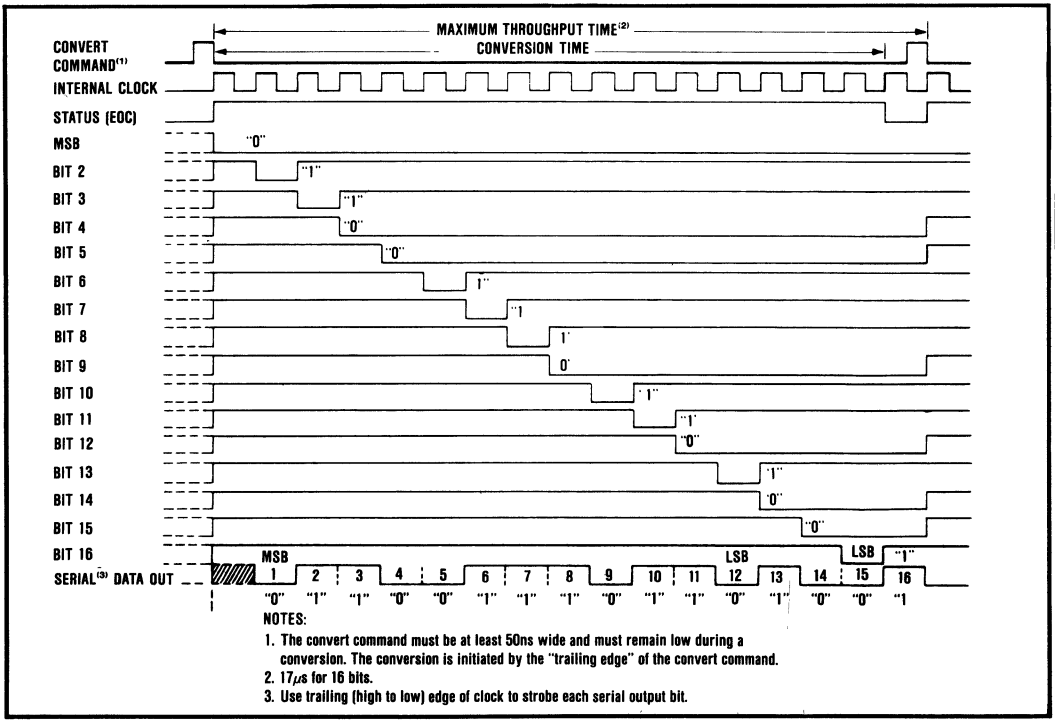


FIGURE 2. Timing Diagram.

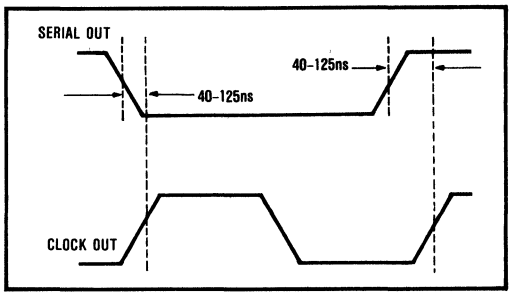


FIGURE 3. Timing Relationship of Serial Data to Clock.

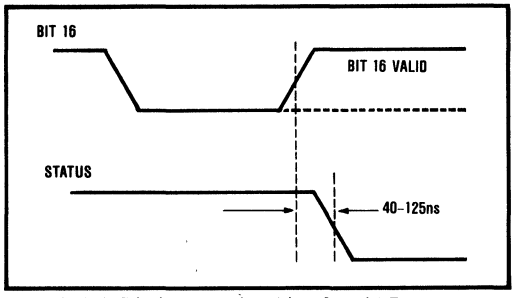


FIGURE 4. Timing Relationship of Valid Data to Status.

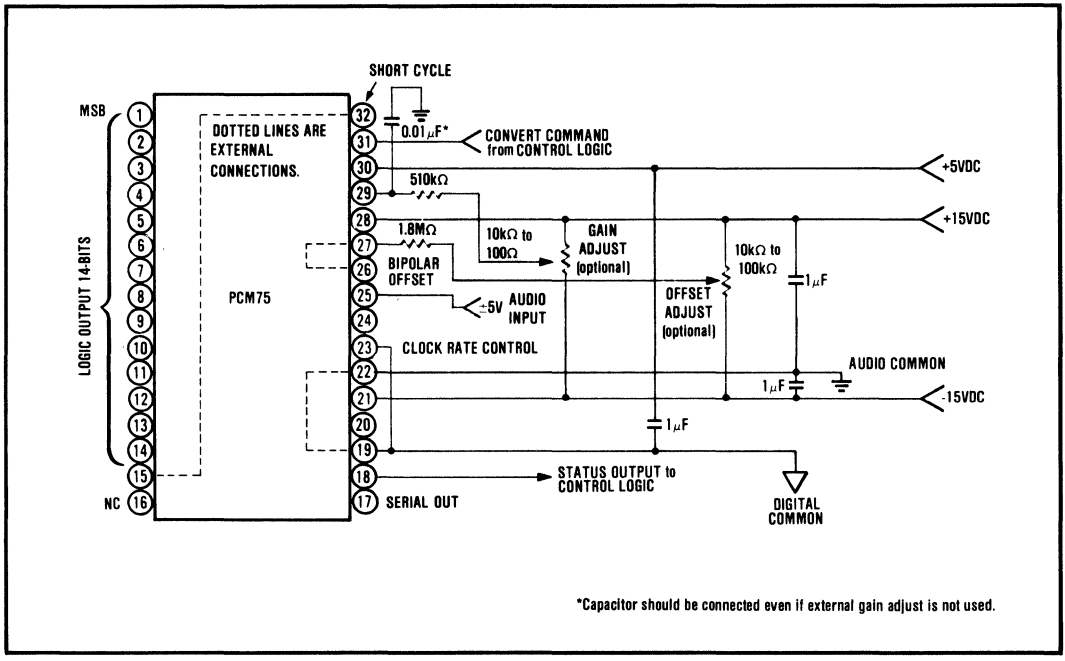


FIGURE 5. PCM75 Connections for: ±5V Audio Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary BIN Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Audio Input Voltage Range	Defined As	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB(1) or CTC(2)	COB(1) or CTC(2)	COB(1) or CTC(2)	CSB(3)	CSB(3)	CSB(3)
One Least Significant Bit LSB	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
n = 16		305µV	153µV	77µV	153µV	77µV	305µV
n = 15		610µV	305µV	153µV	305µV	153µV	610µV
n = 14		1.22mV	610µV	305µV	6.0µV	305µV	1.22mV
Transition Values MSB LSB							
000 000(4)	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011 111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111 110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 +1/2LSB	0 +1/2LSB	0 +1/2LSB

(1) COB = Complementary Offset Binary
(2) CTC = Complementary Two's Complement - obtained by inverting the most significant bit MSB pin 1
(3) CSB = Complementary Straight Binary
(4) Voltages given are the nominal value for transition to the code specified

DISCUSSION OF SPECIFICATIONS

The PCM75 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter in audio applications are total harmonic distortion, drift, gain and offset errors, and conversion time effects on accuracy. The ADC is factory-trimmed and tested for all critical key specifications.

CONVERT COMMAND CONSIDERATIONS

Convert command resets the converter whenever taken high. This insures a valid conversion on the first conversion after power-up.

Convert command must stay low during a conversion unless it is desired to reset the converter during a conversion.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory trimmed to typically ±0.1% of FSR (typically ±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 12 and 13.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The PCM75 power supply sensitivity is specified for ±0.003% of FSR/V, for ±15VDC supplies and ±0.0015% of FSR/V, for +5VDC supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling, and Figure 9.

TOTAL HARMONIC DISTORTION

The Total Harmonic Distortion (THD) is defined as the ratio of the square root of the sum of the squares of the value of the rms harmonics to the value of the rms fundamental and is expressed in percent or dB. A block diagram of the test circuit used to measure the THD of the PCM75 is shown in Figure 6 along with a timing diagram for the control logic. If we assume that the error due to the test circuit is negligible, then the rms value of the PCM75 error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} [E_I(i) + E_Q(i)]^2}$$

where N is the number of samples, $E_I(i)$ is the linearity error of the PCM75 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \frac{\epsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N} [E_I(i) + E_Q(i)]^2}}{E_{rms}} \times 100\%$$

This expression indicates that there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the A/D is directly correlated to the THD because the digital output words from the A/D vary according to the amplitude and frequency of the sine wave input as well as the sampling frequency.

For the PCM75 the test sampling period was chosen to be 22.7μs, which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 400Hz and the amplitude of the input signal is 0dB (full scale) and −15dB.

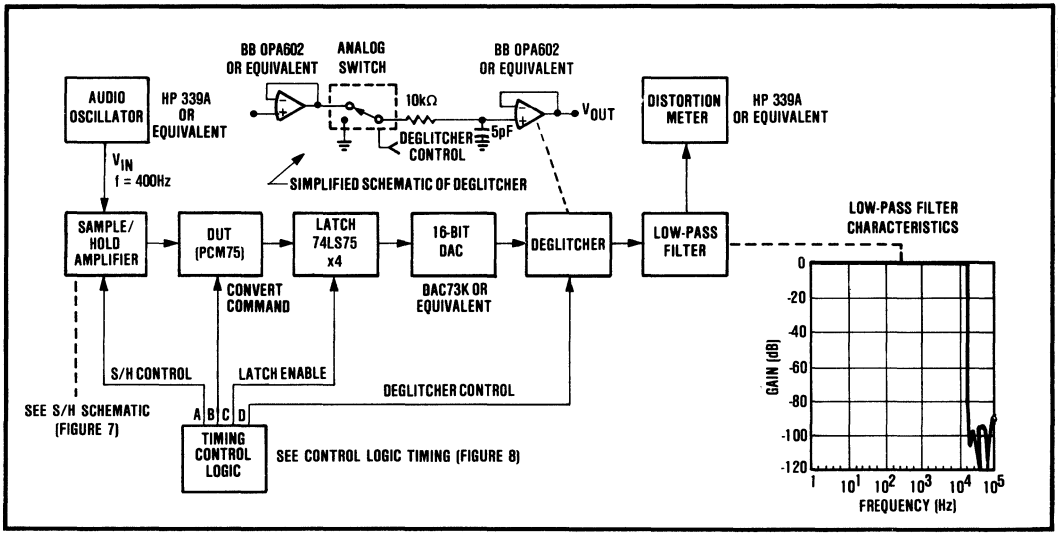


FIGURE 6. Block Diagram of Distortion Test Circuit.

ACCURACY VS CONVERSION TIME

Figures 16 and 17 show the relationship of THD vs input voltage level for the PCM75 with both 14-bit and 16-bit resolution. Notice that the distortion level is reduced by increasing the resolution from 14 to 16 bits due to the reduced quantization error.

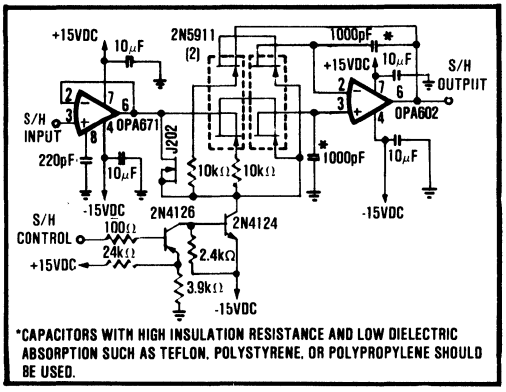


FIGURE 7. Schematic of Sample/Hold Amplifier.

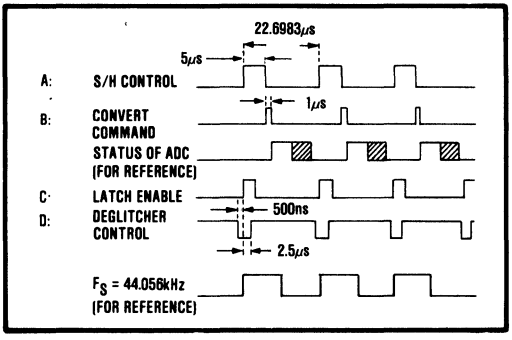


FIGURE 8. Control Logic Timing for PCM75 Distortion Test Circuit.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and Digital Common are not connected internally in the PCM75 but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic capacitors as shown in Figure 9 to obtain noise free operation. These capacitors should be located close to the ADC. Bypass the 1μF electrolytic type capacitors with 0.01μF ceramic capacitors for improved high frequency performance.

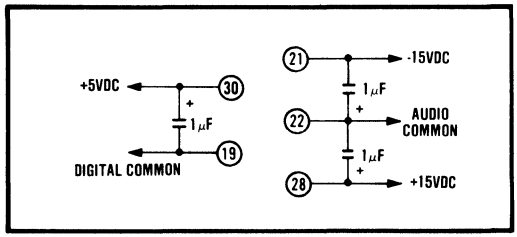


FIGURE 9. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 10 for circuit details.

TABLE II. PCM75 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Sig	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Sig	24

*Obtained by inverting MSB pin 1

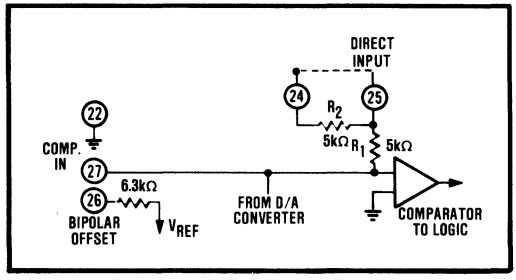


FIGURE 10. PCM75 Input Scaling Circuit.

INPUT IMPEDANCE

The input signal to the PCM75 should come from a low impedance source, such as the output of an op amp, to avoid any errors due to the relatively low input impedance of the PCM75.

If this impedance is not low, a buffer amplifier should be added between the input signal and the direct input to the PCM75 as shown in Figure 11.

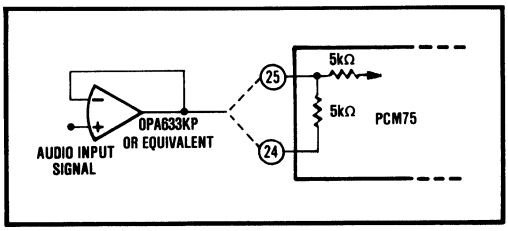


FIGURE 11. Buffer Amplifier for PCM75 Input.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 12 and 13. Multiturn potentiometers with 100ppm/°C or better TCRs are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and pin 27 (Offset Adjust) may be left open if no external adjustment is required; however, pin 29 should always be bypassed with 0.01μF to Audio Common.

ADJUSTMENT PROCEDURE

OFFSET—Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 12. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

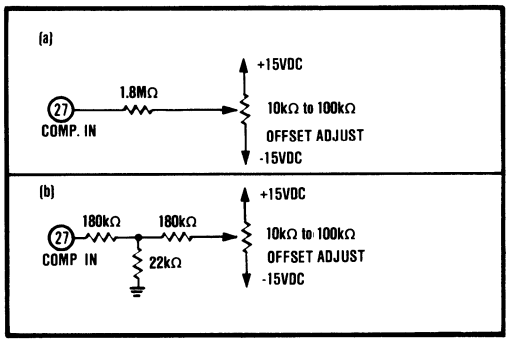


FIGURE 12. Two Methods of Connecting Optional Offset Adjust.

GAIN—Connect the Gain adjust potentiometer as shown in Figure 13. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

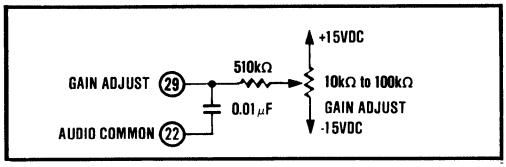


FIGURE 13. Connecting Optional Gain Adjust.

OUTPUT DRIVE

Normally all PCM75 logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

ADDITIONAL OPTIONAL CONNECTIONS

The PCM75 may be operated with faster conversion times for resolutions less than 14 bits, if a higher THD is acceptable, by connecting Short Cycle (pin 32) as shown in Table III. Typical conversion times for the resolution and connections are indicated.

TABLE III. Short Cycle Connections for 14- to 16-Bit Resolutions.

Resolution (Bits)	16	15	14
Connect Pin 32 to	Open	Pin 16	Pin 15
Conversion Time (Typical) μsec	17	16	15

The Clock Rate pin may be connected to an external multiturn trim potentiometer with a TCR of ±100ppm/°C or less as shown in Figure 14. The typical conversion time vs the Clock Rate Control voltage is shown in Figure 15. The effect of varying the conversion time and the resolution on the total harmonic distortion is shown in Figures 16 and 17.

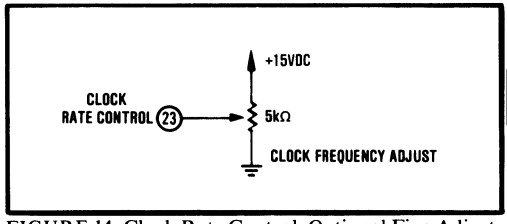


FIGURE 14. Clock Rate Control, Optional Fine Adjust.

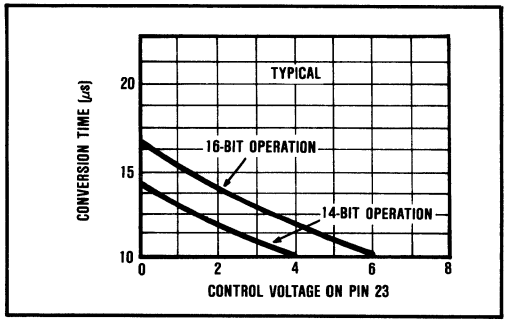


FIGURE 15. Conversion Time vs Clock Rate Control Voltage.

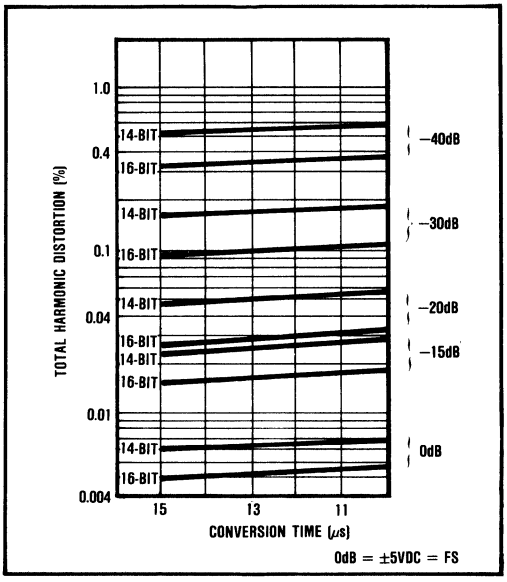


FIGURE 16. Total Harmonic Distortion vs Conversion Time.

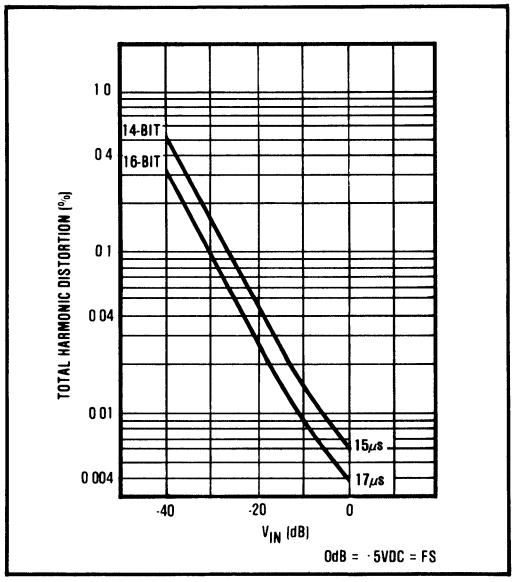
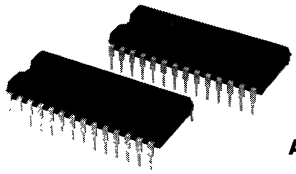


FIGURE 17. Total Harmonic Distortion vs Input Voltage Level.

BURR-BROWN®

PCM78P



ADVANCE INFORMATION SUBJECT TO CHANGE

16-Bit Audio ANALOG-TO-DIGITAL CONVERTER

FEATURES

- LOW COST/HIGH PERFORMANCE 16-BIT AUDIO A/D CONVERTER
- FAST 5μs MAX CONVERSION TIME (4μs typ)
- VERY LOW THD+N (TYP −88dB at FS; MAX −82dB)
- ±3V INPUT RANGE (INTERFACES EASILY TO SAMPLE/HOLD AMPLIFIERS)
- TWO SERIAL OUTPUT MODES SIMPLIFY INTERFACING REQUIREMENTS
- COMPLETE WITH INTERNAL REFERENCE AND CLOCK IN 28-PIN PLASTIC DIP
- ±5V TO ±12V SUPPLY RANGE (600mW POWER DISSIPATION)

APPLICATIONS

- DSP DATA ACQUISITION
- TEST INSTRUMENTATION
- SAMPLING KEYBOARD SYNTHESIZERS
- DIGITAL AUDIO TAPE
- BROADCAST AUDIO RECORDING
- TELECOMMUNICATIONS

DESCRIPTION

The PCM78P is a 16-bit A/D converter which is specifically designed and tested for dynamic applications. It features very fast, low distortion performance (4μs/−88dB THD+N typical) and comes complete with internal clock and reference circuitry. The PCM78P comes in a reliable, low cost 28-pin plastic package and data output is available in several user-selectable serial output formats. One of the major markets for the PCM78P is digital audio tape (DAT) recorders. Many other similar applications such as digital signal processing and telecom applications are equally well served by the PCM78P.

The PCM78P is a successive approximation type A/D that uses fast bipolar circuitry for the precision analog portion of the converter and very low-power CMOS for all other logic/clock functions. The PCM78P has truly been optimized for maximum dynamic performance and very low cost. This gives it the best price/performance ratio of any A/D converter available to date for high-resolution signal acquisition applications.

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PDS-787

SPECIFICATIONS

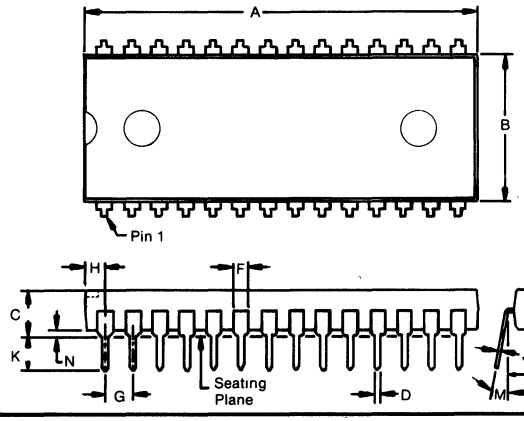
ELECTRICAL

All specifications at +25°C, $+V_{DD}$ = +5.00V, and $\pm V_{CC}$ = ±12.0V unless otherwise noted

PARAMETER	CONDITIONS	PCM78P MIN	PCM78P TYP	PCM78P MAX	UNITS
RESOLUTION				16	Bits
INPUT/OUTPUT					
ANALOG INPUT					
Input Range		−3.00		+3.00	V
Input Impedance			1.5		kΩ
DIGITAL INPUT/OUTPUT					
Logic Family			TTL-Compatible CMOS		
Logic Level V_{IH}	I_{IH} = +40µA	+2.0		+5.5	V
V_{IL}	I_{IL} = −100µA	0.0		+0.8	V
V_{OH}	I_{OH} = 2TTL Loads	+2.4			V
V_{OL}	I_{OL} = 2TTL Loads			+0.4	V
Data Format			Serial BOB or BTC		
Convert Command			Negative Edge[1]		
Pulse Width		50			ns
CONVERSION TIME			4	5	µs
DYNAMIC CHARACTERISTICS					
SIGNAL-TO-NOISE RATIO[2]	F_S = 200kHz/T_{CONV} = 4µs[3]				
F = 1kHz (0dB)	BW = 20kHz		−90		dB[4]
F = 10kHz (0dB)	BW = 100kHz		−80		dB
TOTAL HARMONIC DISTORTION[5]	F_S = 200kHz/T_{CONV} = 4µs				
F = 1kHz (0dB)	BW = 20kHz		−91		dB
F = 19kHz (0dB)	BW = 20kHz		−90		dB
F = 10kHz (0dB)	BW = 100kHz		−90		dB
F = 90kHz (0dB)	BW = 100kHz		−89		dB
TOTAL HARMONIC DISTORTION + NOISE[6]	F_S = 200kHz/T_{CONV} = 4µs				
F = 1kHz (0dB)	BW = 20kHz		−88	−82	dB
F = 1kHz (−20dB)	BW = 20kHz		−74	−68	dB
F = 1kHz (−60dB)	BW = 20kHz		−34		dB
F = 19kHz (0dB)	BW = 20kHz		−87		dB
F = 10kHz (0dB)	BW = 100kHz		−82		dB
F = 90kHz (0dB)	BW = 100kHz		−81		dB
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain Error			±2		%
Bipolar Zero Error			±20		mV
Linearity Error	Differential		±0.002		% of FSR[7]
Linearity Error	Integral		±0.003		% of FSR
Missing Codes			None		14 Bits[8]
DRIFT					
Gain	0°C to +70°C		±25		ppm/°C
Bipolar Zero	0°C to +70°C		±4		ppm of FSR/°C
POWER SUPPLY SENSITIVITY					
$+V_{CC}$			±0.003		%FSR/%V_{CC}
$-V_{CC}$			±0.003		%FSR/%V_{CC}
$+V_{DD}$			±0.001		%FSR/%V_{DD}
WARM-UP TIME				1	Minute
POWER SUPPLY REQUIREMENTS					
Voltage Range $+V_{CC}$		+4.75		+15.6	V
$-V_{CC}$		−4.75		−15.6	V
$+V_{DD}$		+4.75		+5.25	V
Current $+V_{CC}$	$+V_{CC}$ = +12.0V		+15		mA
$-V_{CC}$	$-V_{CC}$ = −12.0V		−21		mA
$+V_{DD}$	$+V_{DD}$ = +5.00		+7		mA
Power Dissipation	$\pm V_{CC}$ = ±12.0V		575		mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Storage		−50		+100	°C

NOTES. (1) When convert command is high, converter is in a halt/reset mode. Actual conversion begins on negative edge. (2) Ratio of Noise rms/Signal rms (3) F = input frequency; F_S = sample frequency (PCM78P and SHC702 in combination); BW = bandwidth of output (based on FFT or actual analog reconstruction using a 20kHz low-pass filter). (4) Referred to input signal level. (5) Ratio of Distortion rms/Signal rms (6) Ratio of Distortion rms + Noise rms/Signal rms. (7) FSR. Full-Scale Range = 6.0Vp-p. (8) Typically no missing codes at 14-bit resolution.

MECHANICAL



NOTE Leads in true position within 0.010" (0.25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers are not marked on package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1 400	1 460	35 56	37 08
B	0 530	0 575	13 46	14 61
C	0.169	0 224	4 29	5 69
D	0 015	0 023	0 38	0 58
F	0 043	0 065	1 09	1 65
G	0 100 BASIC		2 54 BASIC	
H	0 030	0 090	0 76	2 29
J	0 008	0 015	0 20	0 38
K	0 100	0 136	2 54	3 45
L	0 600 BASIC		15 24 BASIC	
M	0°C	15°C	0°C	15°C
N	0 018	0 022	0 46	0 56

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Analog Common	0 to +16 5V
$-V_{CC}$ to Analog Common	0 to −16 5V
$-V_{DD}$ to Digital Common	0 to +7 0V
Analog Common to Digital Common	±0 5V
Logic Inputs to Digital Common	−0 3V to V_{DD} +0 5V
Analog In to Analog Common	±16 5V
Lead Temperature, (soldering, 10s)	+300°C

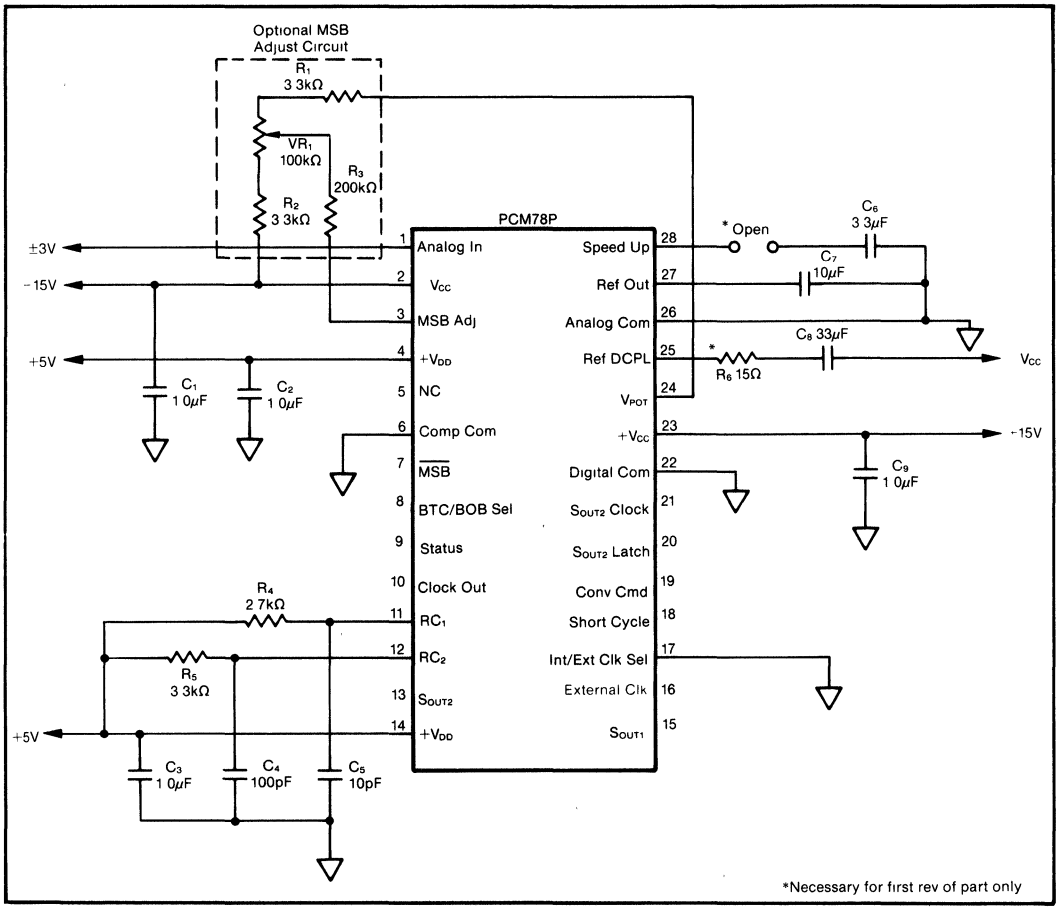
INPUT/OUTPUT RELATIONSHIPS

ANALOG INPUT	CONDITION	DIGITAL OUTPUT	
		BTC	BOB
+2 999908V	+Full Scale	7FFF Hex	FFFF Hex
−3 000000V	−Full Scale	8000 Hex	0000 Hex
0 000000V	Bipolar Zero	0000 Hex	8000 Hex
−0 000092V	Zero − 1LSB	FFFF Hex	7FFF Hex

PIN DESCRIPTIONS

PIN	NAME	I/O	DESCRIPTION
1	Analog In	Input	Analog Signal Input (1 5kΩ input impedance)
2	$-V_{CC}$		Analog power supply (−5V to −15V)
3	MSB Adjust	Input	Internal adjustment point to allow adjustment of MSB major carry.
4	$+V_{DD}$		Power connection for comparator (+5V).
5	No Connection		No internal connection
6	Comparator Common		Comparator common connection
7	MSB	Output	Parallel output of bit 1 (MSB) for use in offset adjustments.
8	BTC/BOB Select	Input	Twos complement (open) or straight binary (grounded) data output format selection.
9	Status	Output	Output signal held high until conversion is complete
10	Clock Out	Output	Internal clock output generated from RC network on pins 11 and 12 (also present when external clock is used lagging external clock by ≈ 24ns and same duty cycle).
11	R_1C_1		RC connection point used to generate the internal clock (tied to +5V with a 5kΩ resistor when external clock option is used) Sets clock pulse width.
12	R_2C_2		RC connection point used to generate the internal clock (tied to +5V with 5kΩ resistor when external clock option is used) Sets clock period.
13	S_{OUT2}	Output	Internal shift register containing the previous conversion result (alternate latched data output mode)
14	$+V_{DD}$		Power connection for +5V logic supply
15	S_{OUT1}	Output	Primary real-time data output synchronized to clock out.
16	External Clock	Input	External clock input point (internal clock must be disabled)
17	Int/Ext Clock Select	Input	Selects internal or external clock mode (low = internal; open = external).
18	Short Cycle	Input	Terminates conversion at less than 16-bits (open for 16-bit mode).
19	Convert Command	Input	Starts conversion process (can optionally be generated internally).
20	S_{OUT2} Latch	Input	Latches previous conversion result for readout (must be issued with the S_{OUT2} clock to initiate latch and an internal convert command).
21	S_{OUT2} Clock	Input	Used to read out internally latched data from previous conversion.
22	Digital Common		Digital grounding pin.
23	$+V_{CC}$		Analog supply connection (+5V to +15V).
24	V_{POT}	Output	Voltage output for optional adjustment of the MSB transition.
25	Reference Decouple		Reference decoupling point.
26	Analog Common		Analog grounding pin.
27	Reference Out	Output	Should not be used except as shown in connection diagram.
28	Speed Up		Connection point for a capacitor.

CONNECTION DIAGRAM



TIMING REQUIREMENTS

As shown in the Timing Diagram, the PCM78 requires 17 clock cycles to complete a conversion. To calculate the clock frequency necessary for a given conversion time, the following equation may be used:

$$f_{CLOCK} = \frac{17}{\text{Conversion Time}}$$

Using S_{OUT1} With Internal Clock

The falling edge of the Convert Command gates the internal oscillator on after a slight delay, typically 75ns. The rising edge of this internal clock sets the Status line high and resets the SAR. Data is clocked out of S_{OUT1} on the subsequent 16 rising edges of the clock.

The internal clock is available on pin 10, Clock Out. The frequency and duty cycle of this clock is set by R_1C_1 and R_2C_2. R_1C_1 sets the duty cycle of the clock, which should be between 20% to 80%, and may be set to 50% for simplicity. The relationship between duty cycle and external part values is:

Duty Cycle (in ns) = $32 + 1.3193R_1C_1$ R in kΩ; C in pF.

The period of the clock is set by R_2C_2 and may be calculated by:

Clock Period (in ns) = $220 + 1.3293R_2C_2$ R in kΩ; C in pF.

These equations are approximate; if highly accurate time bases are required, use of an external clock is recommended.

Using S_{OUT1} With External Clock

The external clock is applied at pin 16, and the Int/Ext Clock Select (pin 17) should be left open. An internal pull-up resistor assures that the logical state of an open pin is "1." The Convert Command should be timed so the falling edge of the Convert Command occurs before a rising edge of the Exernal Clock, since the conversion begins when this happens (recommended delay is 50ns). If the Convert Command's falling edge occurs after or exactly at the same time as the External Clock's rising

edge, the conversion will not begin until the next rising edge of the External Clock.

The Clock Out function is a gated form of the External Clock, i.e., the 17 clock cycles used in the conversion are present on this pin during conversion. This allows use of a continuous External Clock, with Clock Out being the clock that the converter is actually using for conversion. Note that this is simply a delayed (~24ns) version of the external clock, and will have the same frequency and duty cycle.

Using S_{OUT2} Latch

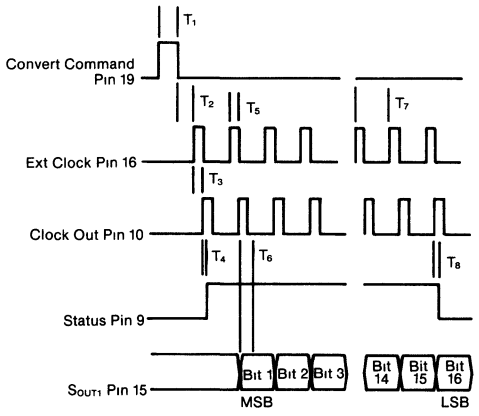
As shown in the Timing (Optional) Diagram, the S_{OUT2} Latch enables the user to latch data from the previous conversion and read it out at higher speed than the Convert Clock. This feature allows the converter to easily interface to digital filtering necessary for over-sampling.

In this mode, the PCM78 generates its own internal Convert Command when the S_{OUT2} Clock goes high within ±50ns of S_{OUT2} Latch going low; the external Convert Command may not be used, and pin 19 must be grounded. The Timing Diagram shows the recommended timing for using this mode. After the S_{OUT2} Latch control signal goes low, data from the SAR is loaded into the S_{OUT2} Latch on the next rising edge of the Conversion Clock (internal or external), since the SAR will reset itself prior to the latching if the Convert Clock rises before the S_{OUT2} Clock. This condition is avoided as long as the frequency of S_{OUT2} Clock is at least 1.5 times that of the conversion clock.

The internal Convert Command is generated upon S_{OUT2} Latch going low, and its falling edge occurs upon the first falling edge of S_{OUT2} Clock after S_{OUT2} Latch goes low. S_{OUT2} Latch should remain low for at least two cycles of S_{OUT2} Clock to ensure proper latching.

The data read out on S_{OUT2} is from the conversion previously performed, while the data that is present on S_{OUT1} is the real-time readout of the successive approximation as it occurs.

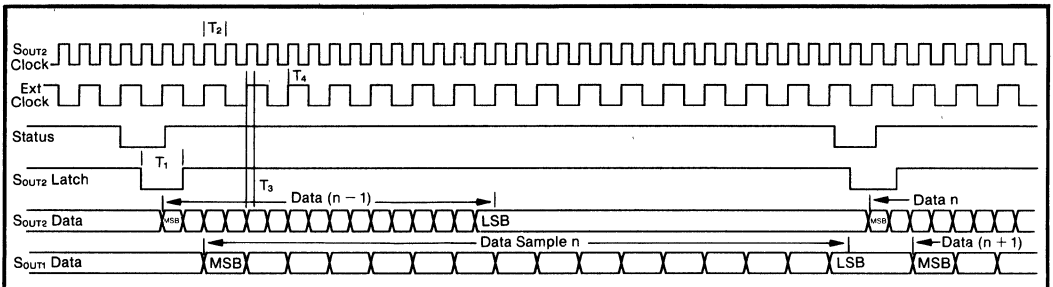
TIMING



TIME	DESCRIPTION	Time (ns) MIN	TYP	MAX
T_1	Convert Command Pulse	50	100	
T_2	External Clock Delay		50	70
T_3	Clock Output Delay		24	
T_4	Clock/Status Start Delay		10	30
T_5	Clock Pulse Width	50	125	
T_6	Clock Out/Data Valid		20	50
T_7	External Clock Cycle	200	300	
T_8	Clock/Status End Delay		10	30

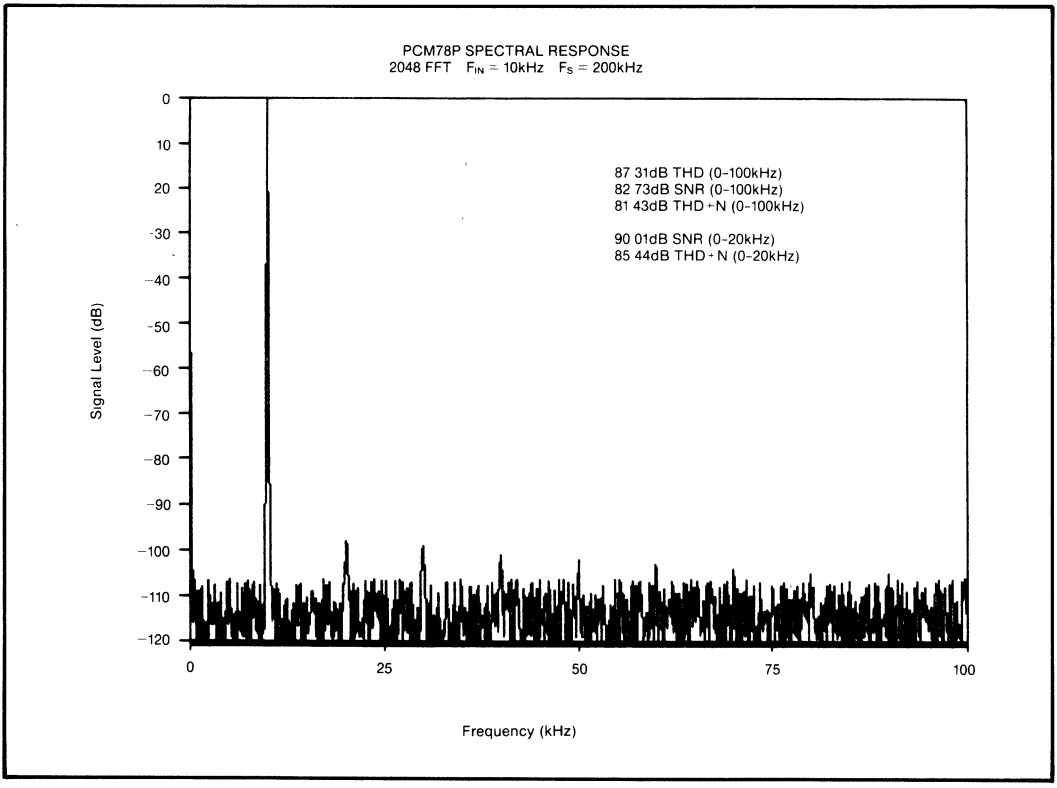
NOTE (1) External clock (Pin 16) not required when internal clock is selected using INT/EXT CLK SEL (Pin 17). Timing is provided here to show relationship between external clock input (Pin 16) and clock output (Pin 10) when an external clock is used. If internal clock is used add T_2 and T_3 together to get the convert command to clock out time delay.

TIMING (OPTIONAL)



TIME	DESCRIPTION	Time (ns) MIN	TYP	MAX
T_1	S_{OUT} Low Pulse Width	200		
T_2	S_{OUT2} Clock Cycle	100		
T_3	Clock Out/Data Valid		5	40
T_4	S_{OUT2} CLK/EXT Clock Delay	0		100

TYPICAL FFT SPECTRAL RESPONSE



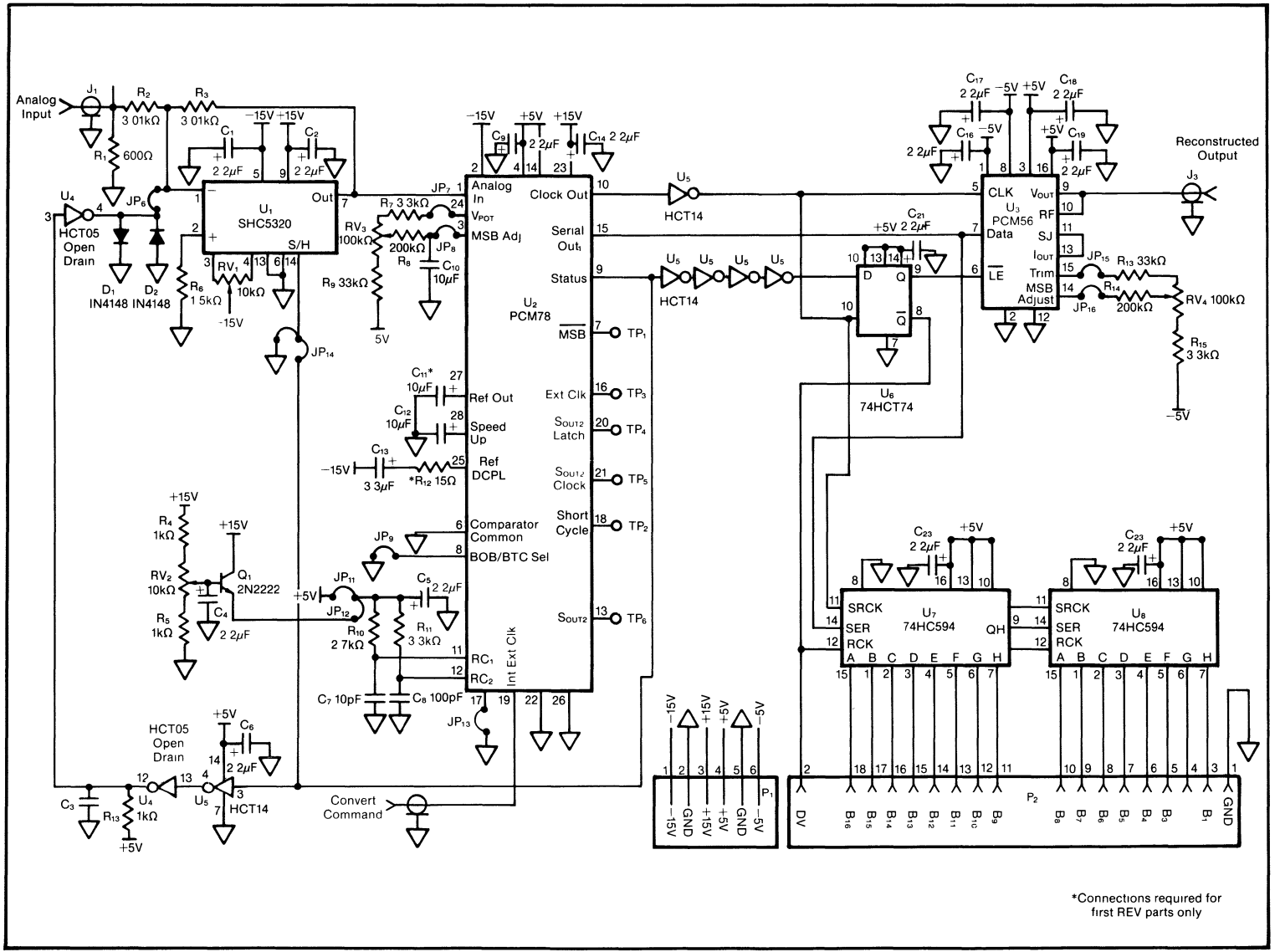


FIGURE 1. Circuit Schematic for Demonstration Fixture (DEM1122).

VOLTAGE-TO-FREQUENCY CONVERTERS

Voltage-to-frequency converters provide a simple, low-cost way of converting analog signals into digital form. They provide an important alternative to other analog-to-digital conversion techniques. Their integrating input properties make them an appropriate choice when operating in noisy environments. The combination of high accuracy and linearity, low temperature drift, and monotonicity often provide performance characteristics unattainable with other techniques.

Since an analog quantity represented as a frequency is inherently serial data, it is easily handled in large multi-channel systems. Frequency information can be transmitted over long lines with excellent noise immunity using low cost digital line transmitters and receivers. Isolation can be accomplished with optical or transformer couplers without loss in accuracy. Outputs from multiple VFCs can be gated to common counter circuitry with simple digital logic. Low-cost isolation is obtained when a VFC is used together with a DC/DC converter and a single optical coupler.

Burr-Brown monolithic voltage-to-frequency converters provide industry-standard performance and reliability in such applications as precision test and measurement equipment, data acquisition systems, communications equipment, and process control.

10

VOLTAGE-TO-FREQUENCY CONVERTERS SELECTION GUIDE

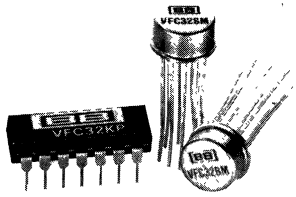
The Selection Guide shows parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book*.

VOLTAGE-TO-FREQUENCY CONVERTERS — **Boldface = NEW**

Description	Model	Frequency Range (kHz)	V_{IN} Range (V)	Linearity, max (% of FSR)	Tempco, max (ppm of FSR/°C)	Temp Range[1]	Pkg	Page
Low-Cost Monolithic	VFC32P VFC32M	User-selected 500kHz, max	User-selected	±0.01 at 10kHz ±0.05 at 100kHz	75 typ ±100	Com Ind	DIP TO-100	10-3 10-3
Low-Cost Complete	VFC42 VFC52	0 to 10 0 to 100	0 to +10 0 to +10	±0.01 ±0.05	±100 ±150	Ind Ind	DIP DIP	10-12 10-12
Precision Monolithic	VFC62 VFC320	User-selected, 1MHz max	User-selected	±0.002 at 10kHz ±0.002 at 10kHz	±20 ±20	Ind Ind	DIP, TO-100 for Both	10-18 10-54
Synchronized Monolithic	VFC100G	Clock Programmed, 2MHz max	0 to +10	0.1 at 1MHz	±50	Ind	DIP	10-26
	VFC101N	**Clock Programmed, 2MHz max**	**0 to +10, 0 to +5, 0 to +8, –5 to +5**	**±0.02 at 100kHz**	**±40**	**Ind**	**PLCC**	**10-41**
High-Performance	**VFC110**	**User-selected 4MHz max**	**0 to +10**	**±0.05 at 1MHz**	**±50**	**Ind**	**DIP**	**10-52**

NOTES: (1) Com = 0°C to +70°C, Ind = –25°C to +85°C.

BURR-BROWN®



VFC32

MILITARY & DIE VERSIONS AVAILABLE

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- RELIABLE MONOLITHIC CONSTRUCTION
- HIGH LINEARITY:
  ±0.01% max at 10kHz FS
  ±0.05% max at 100kHz FS
- V/F or F/V CONVERSION
- 6-DECADE DYNAMIC RANGE
- VOLTAGE OR CURRENT INPUT
- OUTPUT TTL/CMOS COMPATIBLE

APPLICATIONS

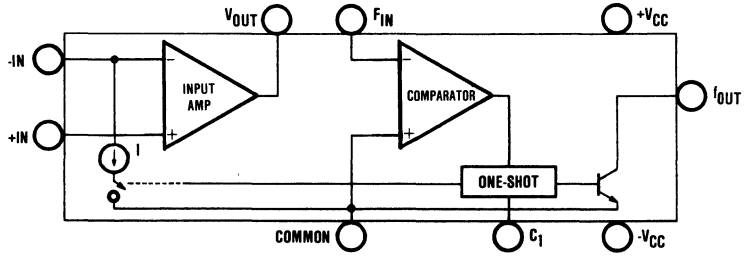
- INEXPENSIVE A/D AND D/A CONVERTER
- DIGITAL PANEL METERS
- TWO-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY
- FM MOD/DEMOD OF TRANSDUCER SIGNALS
- PRECISION LONG TERM INTEGRATOR
- HIGH RESOLUTION OPTICAL LINK
- AC LINE FREQUENCY MONITOR
- MOTOR SPEED MONITOR

DESCRIPTION

The VFC32 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital output is an open collector and the digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with TTL and CMOS logic families.

The converter requires two external resistors and two external capacitors to operate. Full scale frequency and input voltage are determined by one resistor (in series with —IN) and two capacitors (one-shot timing and input amplifier integration). High linearity is achieved with relatively few external components, e.g., ±0.01% at 10kHz. The other resistor is a non-critical open collector pull-up (f_{OUT} to $+V_{CC}$).

The VFC32 is available in three models and two package configurations. The TO-100 versions are hermetically sealed, and specified for the −25°C to +85°C and −55°C to +125°C ranges. The plastic DIP and SOIC are specified from 0°C to +70°C.



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PDS-372E

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC power supply unless otherwise noted

CHARACTERISTICS	CONDITIONS	VFC32KP, KU MIN	VFC32KP, KU TYP	VFC32KP, KU MAX	VFC32BM MIN	VFC32BM TYP	VFC32BM MAX	VFC32SM MIN	VFC32SM TYP	VFC32SM MAX	UNITS
INPUT (V/F CONVERTER)	$F_{OUT} = V_{IN} / 7.5\ R_1C_1$, Figure 6										
Voltage Range[1]											
Positive Input		>0		+0.25mA x R_1	*		*	*		*	V
Negative Input		>0		-10	*		*	*		*	V
Current Range[1]		>0		+0.25	*		*	*		*	mA
Bias Current											
Inverting Input			20	100		*	*		*	*	nA
Noninverting Input			100	250		*	*		*	*	nA
Offset Voltage[2]			1	4		*	*		*	*	mV
Differential Impedance		300 || 10	650 ||10		*	*		*		kΩ || pF
Common-mode Impedance		300 || 3	500 || 3		*	*		*	*		MΩ || pF
INPUT (F/V CONVERTER)	$V_{OUT} = 7.5\ R_1C_1\ F_{IN}$, Figure 9										
Impedance		50 || 10	150 || 10		*	*		*	*		kΩ || pF
Logic "1"			+1.0		*		*	*		*	V
Logic "0"			−0.05		*		*	*		*	V
Pulse-width Range		0.1		150k/F_{MAX}	*		*	*		*	μsec
ACCURACY											
Linearity Error[3]	0.01Hz ≤ oper freq ≤ 10kHz		±0.005	±0.010[4]		*	*		*	*	% of FSR[5]
	0.1Hz ≤ oper freq ≤ 100kHz		±0.025	±0.05		*	*		*	*	% of FSR
	0.5Hz ≤ oper freq ≤ 500kHz		±0.05			*			*		% of FSR
Offset Error Input Offset Voltage[2]			1	4		*	*		*	*	mV
Offset Drift[6]			±3			*			*		ppm of FSR/°C
Gain Error[2]			5			*	*		*	*	% of FSR
Gain Drift[6]	f = 10kHz		±75			±50	±100		±70	±150	ppm/°C
Full Scale Drift (offset drift & gain drift)[6][7]	f = 10kHz		±75			±50	±100		±70	±150	ppm of FSR/°C
Power Supply Sensitivity	f = DC, ±V_{CC} = 12VDC to 18VDC			±0.015			*			*	% of FSR/%
OUTPUT (V/F CONVERTER) (open collector output)											
Voltage, Logic "0"	I_{SINK} = 8mA	0	0.2	0.4	*	*	*	*	*	*	V
Leakage Current, Logic "1"	V_O = 15V		0.01	1.0		*	*		*	*	μA
Voltage, Logic "1"	External pull-up resistor required (see Figure 4)			V_{PU}			*			*	V
Pulse Width	For Best Linearity		0.25/F_{MAX}			*			*		sec
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF			400			*			*	nsec
OUTPUT (F/V CONVERTER) V_{OUT}											
Voltage	$I_O \leq$ 7mA	0 to +10			*			*			V
Current	$V_O \leq$ 7VDC	+10			*			*			mA
Impedance	Closed loop			1			*			*	Ω
Capacitive Load	Without oscillation			100			*			*	pF
DYNAMIC RESPONSE											
Full Scale Frequency				500[8]	*			*			kHz
Dynamic Range		6			*			*			decades
Settling Time	(V/F) to specified linearity for a full scale input step		[9]			*			*		
Overload Recovery	< 50% overload		[9]			*			*		
POWER SUPPLY											
Rated Voltage			±15								V
Voltage Range		±11		±20					*		V
Quiescent Current			±5.5	±6.0		*	*		*		mA
TEMPERATURE RANGE											
Specification		0		+70	-25		+85	-55		+125	°C
Operating		-25		+85	-55		+125	-55		+125	°C
Storage		-25		+85	-65		+150	-65		+150	°C

*Specification the same as VFC32KP

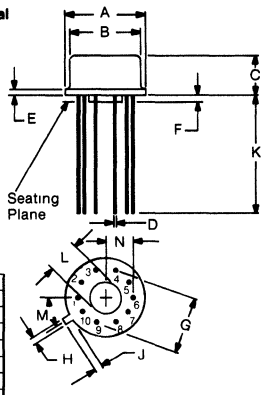
NOTES
1 A 25% duty cycle (0 25mA input current) is recommended where possible to achieve best linearity
2 Adjustable to zero See Offset and Gain Adjustment section
3 Linearity error is specified at any operating frequency from the straight line intersecting 90% of full scale frequency and 0 1% of full scale frequency See Discussion of Specifications section
Above 200kHz, it is recommended all grades be operated below +85°C
4. ±0 015% of FSR for negative inputs shown in Figure 7 Positive inputs are shown in Figure 6
5 FSR = Full Scale Range (corresponds to full scale frequency and full scale input voltage
6 Exclusive of external components' drift
7 Positive drift is defined to be increasing frequency with increasing temperature
8 For operation above 200kHz up to 500kHz, see Discussion of Specifications and Installation and Operation sections
9 One pulse of new frequency plus 1μsec

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±22
Output Sink Current (F_{OUT})	50mA
Output Current (V_{OUT})	+20mA
Input Voltage, –Input	±Supply
Input Voltage, +Input	±Supply
Comparator Input	±Supply
Storage Temperature Range.	
VFC32BM, SM	–65°C to +150°C
VFC32KP, KU	–25°C to +85°C

MECHANICAL

VFCBM, VFC32SM-TO-100 Metal

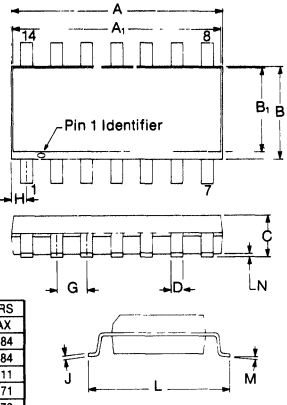


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	335	370	8 51	9 40
B	305	335	7 75	8 51
C	165	185	4 19	4 70
D	016	021	0 41	0 53
E	010	040	0 25	1 02
F	010	040	0 25	1 02
G	230 BASIC		5 84 BASIC	
H	028	034	0 71	0 86
J	029	045	0 74	1 14
K	500	—	12 70	—
L	120	160	3 05	4 06
M	36° BASIC		36° BASIC	
N	110	120	2 79	3 05

NOTE Leads in true position within 0 01" (0 25mm) R at MMC at seating plane

Pin numbers shown for reference only Numbers may not be marked on package

VFC32KU - Plastic SOIC



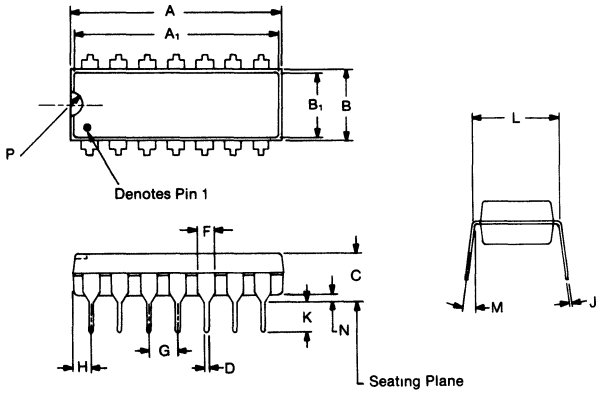
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	332	348	8 44	8 84
A_1	325	348	8 26	8 84
B	146	162	3 71	4 11
B_1	128	146	3 25	3 71
C	052	068	1 32	1 73
D	014	019	0 36	0 48
G	050 BASIC		1 27 BASIC	
H	016	024	0 41	0 61
J	008	012	0 20	0 30
L	226	246	5 74	6 25
M	5° TYP		5° TYP	
N	000	012	0 00	0 30

NOTE Leads in true position within 0 01" (0 25mm) R at MMC at seating plane

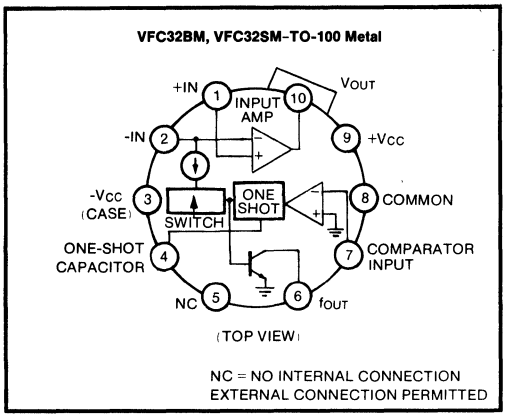
VFC32KP-Plastic DIP

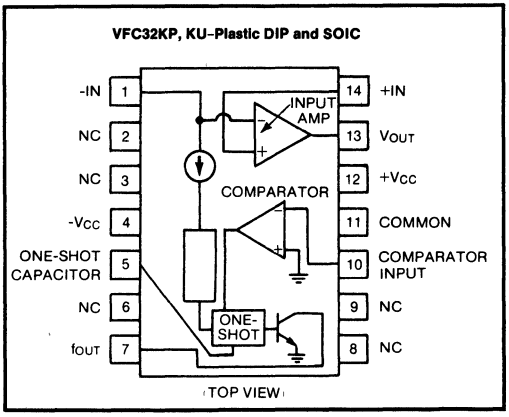
NOTE Leads in true position within 0 01" (0 25mm) R at MMC at seating plane

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	700	800	17 78	20 32
A_1	685	785	17 40	19 94
B	230	290	5.85	7 38
B_1	200	250	5 09	6 36
C	120	200	3 05	5 09
D	015	023	0 38	0 59
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	050	100	1 27	2 54
J	008	015	0 20	0 38
K	070	150	1 78	3 82
L	300 BASIC		7 63 BASIC	
M	0°	15°	0°	15°
N	010	030	0 25	0 76
P	025	050	0 64	1 27



PIN CONFIGURATIONS





DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (90% of full scale input or frequency and 0.1% of full scale called zero). Linearity is the true measure of voltage-to-frequency converter's performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. For a given full scale frequency, the linearity error decreases with decreasing operating frequency as shown in Figure 2. Also, best linearity is achieved at lower gains ($\Delta F_{OUT}/\Delta V_{IN}$) with operation as close to the chosen full scale frequency as possible.

The high linearity of the VFC32 makes the device an excellent choice for use as the front end of A/D converters with 8- to 12-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire serial data transmission).

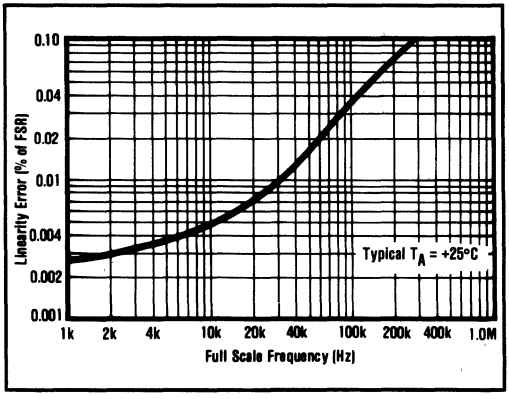


FIGURE 1. Linearity Error vs Full Scale Frequency. (25% Duty Cycle)

FREQUENCY STABILITY vs TEMPERATURE

The full scale frequency drift of the VFC32 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 100kHz, and this should be taken into account for

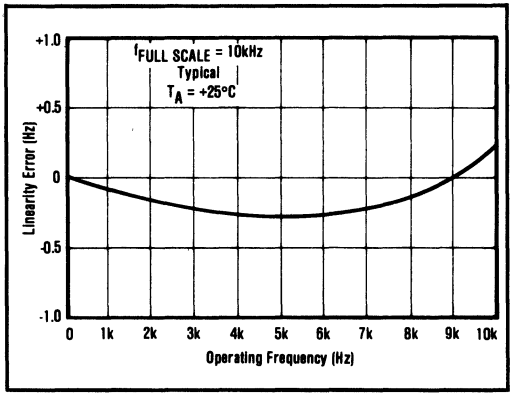


FIGURE 2. Linearity Error vs Operating Frequency. (25% Duty Cycle)

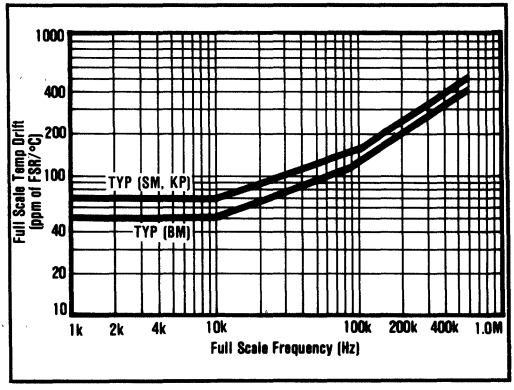


FIGURE 3. Full Scale Drift vs Full Scale Frequency. (25% Duty Cycle)

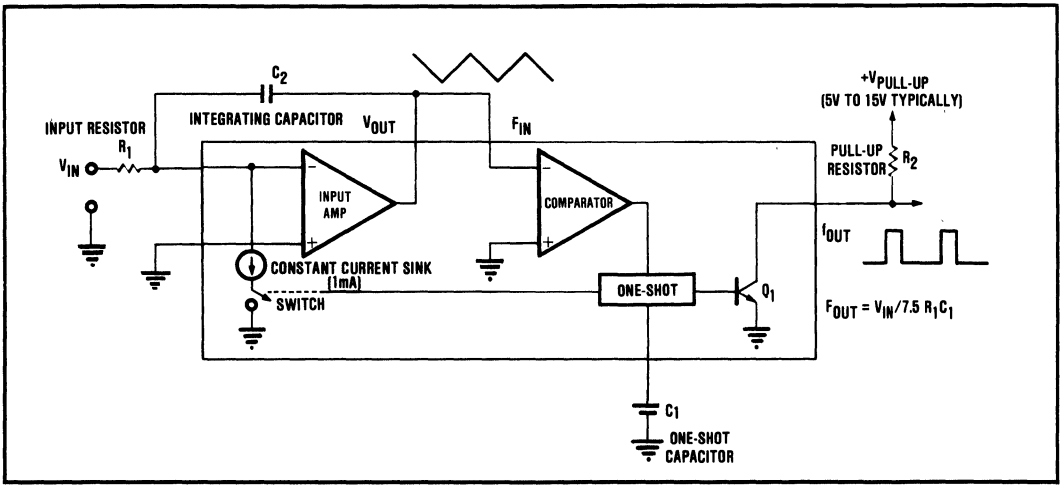


FIGURE 4. Functional Block Diagram of the VFC32.

specific applications. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially R_1 and C_1) must be added to the drift of the VFC32. Above 200kHz, it is recommended all grades be operated below +85°C. Higher duty cycle (up to 50%) and higher output transistor collector current (up to 15mA) will be required. Linearity will, however, be degraded.

RESPONSE

Response of the VFC32 to changes in input signal level is specified for a full scale step, and is 1 microsecond plus 1 pulse of the new frequency. For a 10 volt input signal step with the VFC32 operating at 100kHz full scale, the settling time to within ±0.01% of full scale is 11 microseconds.

THEORY OF OPERATION

The VFC32 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage in Figure 4.

Essentially, the input amplifier acts as an integrator that produces a 2-part ramp. The first part is a function of the input voltage, and the second part dependent on the current sink. When a positive input voltage is applied at V_{IN}, a constant current will flow through the input resistor, causing the voltage at f_{IN} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_1$. During this time, the constant current sink is disabled by the switch. Note, this period is only dependent on V_{IN} and integrating components. When the ramp reaches a voltage close to zero, the comparator will cause the one-shot to fire. The one-shot period is determined by an internal 7.5V reference and C_1. The f_{OUT} signal will then change logic states, going from a "0" to a "1", and the switch will close, enabling the constant current sink. The ramp voltage will then change direction and begin to ramp up. Since V_{IN}/R_1 is always set up to be less than 1 mA, the current in the integrating capacitor will flow toward the summing junction, and the ramp voltage rate of change will be;

$$\frac{dV}{dt} = \frac{\frac{V_{IN}}{R_1} - 1mA}{C_2}$$

Before the ramp voltage can saturate the input amplifier, the one-shot will reset, disabling the current sink, changing the output state back to logic "0", and restarting the cycle. Since the integrating capacitor C_2 affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to V_{IN}/R_1, since this parameter will add directly to the gain error of the VFC. C_1, which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.

To operate the VFC32 as a highly linear frequency-to-voltage converter, open the connection between V_{OUT} and f_{IN}, and connect V_{IN} to V_{OUT}. The input frequency should be coupled through a capacitor to f_{IN}, and a positive output voltage proportional to f_{IN} will be generated at the V_{OUT} connection. For details see Installation and Operating Instructions.

The total VFC period is determined by the following equations, which is shown graphically in Figure 5.

$$f_o = \frac{1}{t}$$

$$t = t_1 + t_2 \text{ and } i = c\, dv/dt$$

$$t = \Delta V_{OUT}\, t_1 \frac{C_2}{V_{IN}/(R_1)} + \Delta V_{OUT}\, t_2 \frac{C_2}{V_{IN}/(R_1) - 1mA}$$

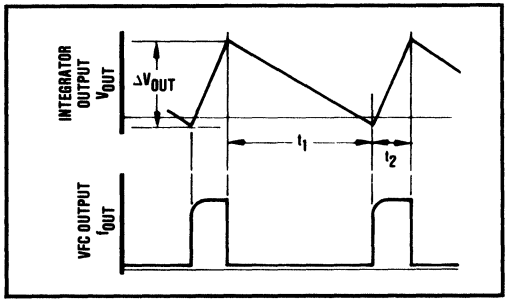


FIGURE 5. Integrator and VFC Output Timing.

and:

$$-\Delta V_{OUT}t_1 = +\Delta V_{OUT}t_2$$

$$t_2 = C_1 \frac{7.5V}{1mA}$$

The equations reduce to:

$$f_o = \frac{V_{IN}}{7.5(R_1)\,C_1}$$

DUTY CYCLE

The duty cycle (D) of the VFC is the ratio of the one-shot period (t_2) or pulse width, PW, to the total VFC period ($t_1 + t_2$). It is measured at the full scale input voltage, which gives the full scale output frequency, F_{FS}.

$$D = \frac{t_2}{t_1 + t_2} = PW \times F_{FS}$$

$$PW = \frac{D}{F_{FS}}$$

Duty cycle is related to the maximum input current and the 1mA (nominal) current sink. By reducing the equations for t_2 and f_o:

$$D = \frac{V_{IN}\ max/(R_1)}{1mA} = \frac{I_{IN}\ max}{1mA}$$

A 25% duty cycle or less is recommended to achieve the best linearity. This corresponds to a maximum input current of 0.25mA. However, for frequencies above 200kHz a higher duty cycle (up to 50%) will provide more stable high temperature operation at a sacrifice in linearity.

In general, designs with the VFC32 include: (1) Choosing F_{MAX}, (2) Choosing the duty cycle (D = 0.25 typically), (3) Determining the one-shot PW, and (4) Calculating C_1, C_2, R_1, R_2, and R_3.

INSTALLATION AND OPERATING INSTRUCTIONS

The VFC32 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.

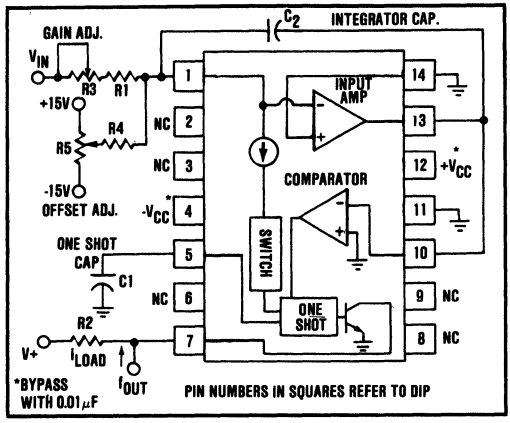


FIGURE 6. Connection Diagram for V/F Conversion, Positive Input Voltages.

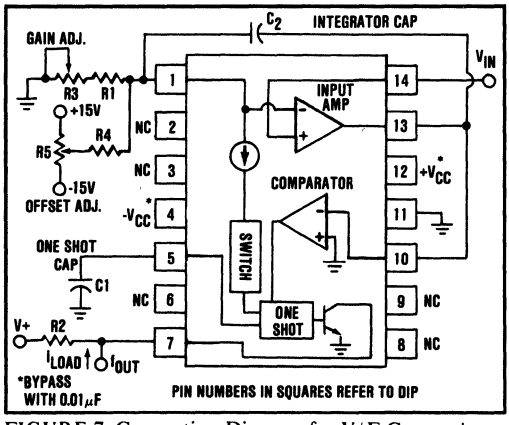


FIGURE 7. Connection Diagram for V/F Conversion, Negative Input Voltages.

Differential inputs are also possible (in Figure 7 lift ground on R_3 and drive R_3 and pin 14 differentially). Note, no CMR will be present.

The full scale frequency and full scale input voltage (current) are established by the selection of values for R1, C2, and C1. Most applications will require a gain adjustment pot (R3), but the offset adjust network (R4, R5) can be omitted if input offset voltages of 1mV to 4mV can be tolerated. R2 is an output pull up resistor and its value depends on the pull up voltage and output drive requirements.

EXTERNAL COMPONENT SELECTION CRITERIA

One-shot Capacitor, C1. This capacitor determines the duration of the output pulse, and is a function of the full scale frequency, according to this equation:

$$C1(pF) = 33 \times 10^6 / f_{MAX} - 30$$

Above 425kHz use 47pF

Select the closest standard value to the capacitance given by the equation. The initial tolerance of this capacitor is

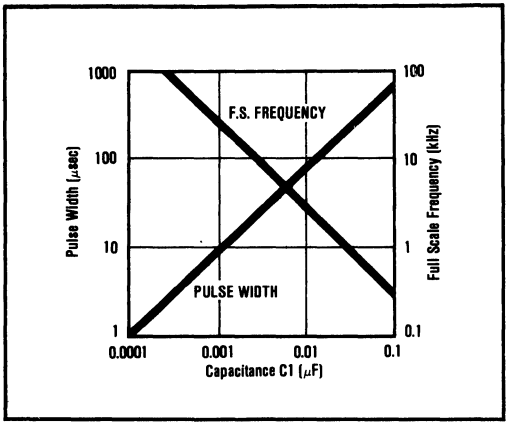


FIGURE 8. Output Pulse Width (D = 0.25) and Full Scale Frequency vs External One-shot Capacitance.

not critical since R3 will be adjusted to remove initial gain errors. The temperature drift is critical, since it will add directly to the errors in the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize the parasitic capacitance at this connection to the VFC32 and C1 should be mounted as close as possible. Figure 8 shows pulse width and FS frequency for various values of C1.

Input Resistor R1 and R3. R1 and R3 determine the magnitude of the current which charges the integrator capacitor. It is a function of the full scale input voltage, according to this equation for 25% duty cycle.

$$R1\ (k\Omega)\ [90\% - \%\ \text{tolerance C1}] \times V_{IN}\ \text{max}/0.25mA$$

R1 is scaled down by [1-(initial C1 tolerance + 0.1)] to allow the addition of a series gain adjusting pot, R3.

$$R_3\ (k\Omega) = V_{IN}\ \text{max}/0.25mA - R_1$$

R1 should have a very low temperature coefficient since this drift adds directly to the errors in the transfer function. If the input signal is a current rather than a voltage, R1 and R3 should be replaced with a short circuit, and the full scale input current should be 0.25mA (25% duty cycle). Removal of gain error then requires adjustment of C1.

Integrating Capacitor C2. C2 is a function of the full scale frequency, according to this equation:

$$C_2(\mu F) = 10^2/f_{MAX}\ \text{below 100kHz}$$
$$0.001\mu F\ \text{min above 100kHz}$$

Select the closest standard value to the capacitance given by the equation. The initial tolerance and temperature stability are not critical since these errors do no affect the transfer function. Since the leakage current of the capacitor introduces a gain error, select a capacitor with leakage that is small compared to the full scale input current e.g., 0.25mA. A mylar type is recommended.

Output Pull Up Resistor R2. The open collector output can sink up to 8mA and still be TTL-compatible. Select R2 according to this equation:

$$R_2\ \text{min}\ (\Omega) = V_{PULLUP}/(8mA - i_{LOAD})$$

A 10% carbon composition resistor is suitable for use as R2.

Operation above 200kHz up to 500kHz requires higher duty cycles up to 50% (I_{IN} = 0.5mA) and a pull-up resistor that permits 15mA to flow in the output transistor. At this speed, capacitive loading should be minimized to 100pF or less to allow the output voltage time to rise to logic one. Due to the large collector current, the logic zero may rise above +0.4V. This may require an interface circuit such as diode clamp or voltage comparator for coupling to TTL inputs. Note, that linearity will degrade. Also, it is recommended to stay below +85°C at high frequencies.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC32 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses -0.6V. Choose C3 for appropriate value of t (see Figure 9). For input signals with amplitudes less than 5V, pin 10 should be biased closer to zero, to insure that the input signal at pin 10 crosses the -0.6V threshold. Errors are nulled following the procedure given on this page, using 0.001X full scale frequency to null offset, and full scale frequency to null the gain error. Use equations from V/F calculations to find R_1, R_3, R_4, R_5, C_1 and C_2.

POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC32 is 0.015% of FSR/% max. To maintain ±0.015% conversion,

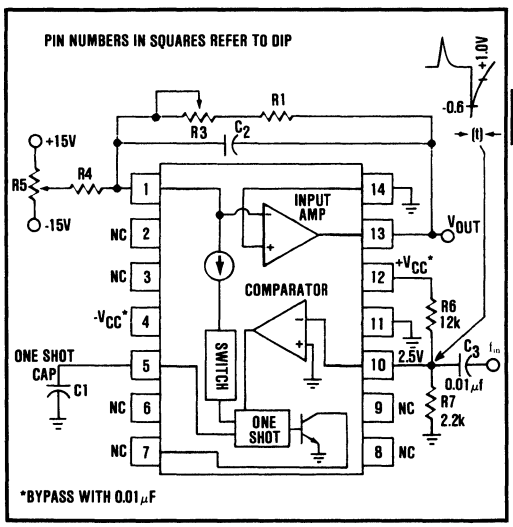


FIGURE 9. Connection Diagram for F/V Conversion.

power supplies which are stable to within ±1% are recommended. These supplies should be bypassed as close as possible to the converter with 0.01μF capacitors.

Current in the f_{OUT} pin (logic sink current) flows in the common connection (pin 11 of DIP package). It is advisable to separate this common lead ground from the analog ground associated with the integrator input to avoid errors produced by logic current flowing through any ground return impedance.

Trimming Components R3, R4, R5.

R5 nulls the offset voltage of the input amplifier. It should have a series resistance between 10kΩ and 100kΩ and a temperature coefficient less than 100ppm/°C. R4 can be a 20% carbon composition resistor with a value of 10MΩ.

R3 nulls the gain errors of the converter and compensates for initial tolerances of R1 and C1. Its total resistance should be at least 20% of R1, if R1 is selected 10% low (see R1 equation). Its temperature coefficient should be no greater than five times that of R1, to maintain a low drift of the R3 - R1 series combination.

OFFSET AND GAIN ADJUSTMENT PROCEDURES

To null errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 X full scale.
2. Adjust R5 for proper output.
3. Apply the full scale input voltage.
4. Adjust R3 for proper output.
5. Repeat steps 1 through 4.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

DESIGN EXAMPLE

Given a full scale input of +10V, select the values of R_1, R_2, R_3, C_1, and C_2 for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

Selecting C_1

$C_1 = 33 \times 10^6 / f_{MAX} - 30$
$= 33 \times 10^6 / 100kHz - 30$
$= 300pF$

Choose a 300pF NPO ceramic capacitor with ±1% tolerance.

Selecting R_1 and R_3 (for D = 0.25; for D = 0.5 use 0.5mA)

$R_1 = [90\% - \%\text{ tolerance of } C_1] \times V_{IN}\text{ max} / 0.25mA$
$= [0.9 - 0.1] \times 10V / 0.25mA$
$= 32k\Omega$

Choose a 32.4kΩ metal film resistor with ±1% tolerance.

$R_3 = 10V / 0.25mA - R_1$
$= 8k\Omega$

Choose a 10kΩ cermet potentiometer

Selecting C_2

$C_2 = 10^2 / F_{MAX}$
$= 10^2 / 100kHz$
$= 0.001\mu F$

Choose a 0.001μF mylar capacitor with ±5% tolerance.

Selecting R_2

$R_2 = V_{PULLUP} / (8mA - i_{LOAD})$
$= 5V / (8mA - 1.6mA)$, one TTL-load = 1.6mA
$= 781\Omega$

Choose a 750Ω 1/4-watt carbon composition resistor with ±5% tolerance.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC32 ideal for a variety of VFC applications. High accuracy allows the VFC32 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 12-bits.

Figures 10 - 14 show typical applications of the VFC32.

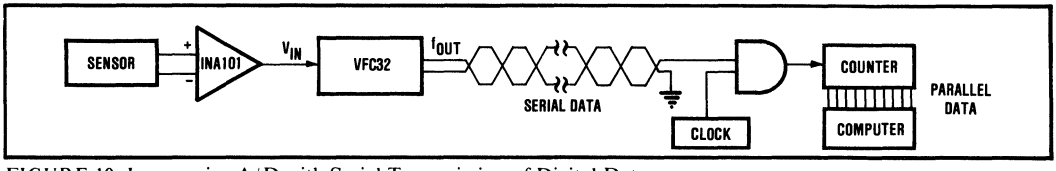


FIGURE 10. Inexpensive A/D with Serial Transmission of Digital Data.

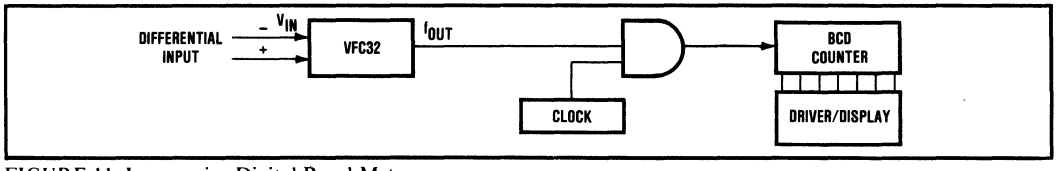


FIGURE 11. Inexpensive Digital Panel Meter.

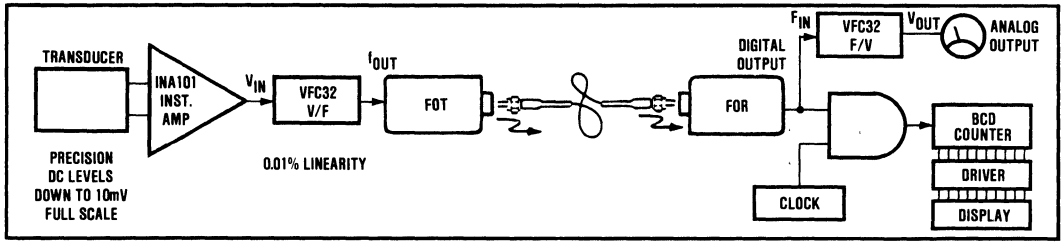


FIGURE 12. Remote Transducer Readout via Fiber Optic Link (analog and digital output).

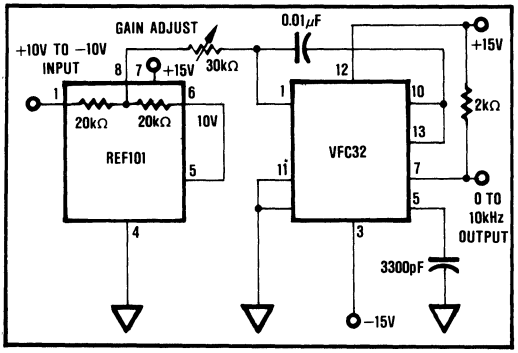


FIGURE 13. Bipolar input is accomplished by offsetting the input to the VFC with a reference voltage. Accurately matched resistors in the REF101 provide a stable half-scale output frequency at zero volts input.

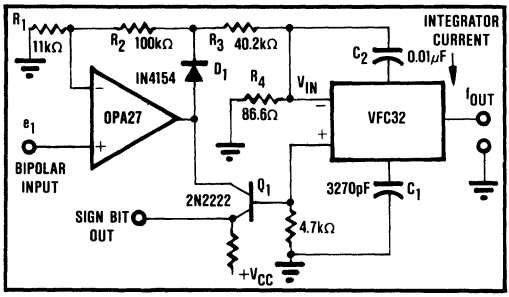


FIGURE 14. Absolute value circuit with the VFC32. Op amp, D_1 and Q_1 (its base-emitter junction functioning as a diode) provide full-wave rectification of bipolar input voltages. VFC output frequency is proportional to $|e_1|$. The sign bit output provides indication of the input polarity.

BURR-BROWN®

VFC42
VFC52

VOLTAGE-TO-FREQUENCY AND FREQUENCY-TO-VOLTAGE CONVERTER

FEATURES

- V/F OR F/V CONVERSION
- TWO FREQUENCY RANGES
  10kHz (VFC42)
  100kHz (VFC52)
- LOW NONLINEARITY
  ±0.01% max (VFC42)
  ±0.05% max (VFC52)
- MINIMAL EXTERNAL COMPONENTS REQUIRED
  Add only one external resistor for V/F operation
- 6 DECADE DYNAMIC RANGE
- OUTPUT DTL/TTL/CMOS COMPATIBLE

DESCRIPTION

VFC42 and VFC52 are hybrid microcircuits which can be connected as voltage-to-frequency or frequency-to-voltage converters. They provide a simple, low cost method of converting analog signals into an equivalent digital form. The digital output is an open collector which can be made compatible with DTL, TTL, or CMOS logic. The output is a train of constant-amplitude, constant-width pulses whose repetition rate is proportional to the amplitude of the analog input voltage. In the frequency-to-voltage mode the pulses become the input and the proportional DC voltage, the output.

Both models are offered in epoxy (−25°C to +85°C) and hermetic metal (−25°C to +85°C and −55°C to +125°C) 14-pin DIP packages.

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PDS-390C

THEORY OF OPERATION

VFC42 and VFC52 hybrid voltage-to-frequency converters provide a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. To understand the circuit's operation see Figure 1.

The input amplifier is connected in an integrator configuration. When a positive input voltage is applied at V_{IN}, a constant current flows through the input resistor causing voltage at f_{IN} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_2$. During this time the constant current sink is disabled by the switch. When the ramp reaches zero volts, the comparator causes the one-shot to fire. The f_{out} signal then changes states, going from logic 0 to logic 1 and the switch closes, enabling the constant current sink. Ramp voltage then changes direction and begins to ramp up. Since V_{IN}/R_1 is always set to be less than 1mA, current in the integrating capacitor flows toward the summing junction and ramp voltage range of change will be

$$\frac{dV}{dt} = \frac{\left(\frac{V_{in}}{R_1}\right) - 1mA}{C_2}$$

Before the ramp voltage can saturate the input amplifier, the one-shot resets, disabling the current sink, changing the output state back to logic 0 and restarting the cycle.

To operate VFC42 and VFC52 as highly linear frequency-to-voltage converters, open the connection between V_{OUT} and F_{IN} and connect V_{IN} to V_{OUT}. The input frequency should be coupled through a capacitor to f_{IN}. A positive output voltage proportional to f_{IN} will be generated at the V_{OUT} connection. An external capacitor connected between pins 13 and 14 (paralleling C2) should be added to reduce output ripple. Refer to Operating Instructions for detailed information on F/V operation.

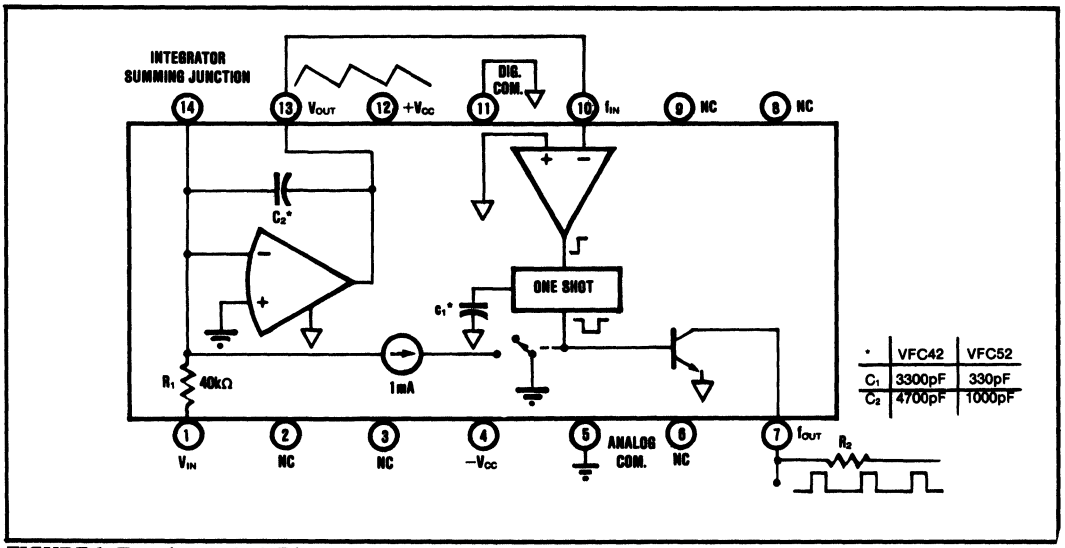


FIGURE 1. Functional Block Diagram.

DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity, the maximum deviation of the actual transfer function from a straight line drawn between the end points (full scale input and zero input), is the true measure of a FVC's performance and is a function of full scale frequency. The high linearity of VFC42 and VFC52 makes these devices an excellent choice for use in A/D converters with 10 (0.05%) and 12 bit (0.012%) accuracy and for highly accurate analog data transfer over long lines in noisy environments.

FREQUENCY STABILITY VS TEMPERATURE

Frequency stability vs temperature is expressed as parts per million of full scale range per °C. Since frequency drift is a function of the specified temperature range, the "SM" models will meet the lower drift specifications of the "BM" models over the narrower −25°C to +85°C temperature range. Error sources do not drift linearly over temperature, consequently the units drift much less at higher temperatures.

RESPONSE TIME

Response time of VFC42 and VFC52 to input signal level changes is specified for a full scale step and is 1μsec plus 1 period of the new frequency. Typical settling time to within rated linearity for a positive input voltage step of +10V is 101μsec for VFC42 and 11μsec for VFC52.

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C, and ±15VDC power supplies unless otherwise noted.

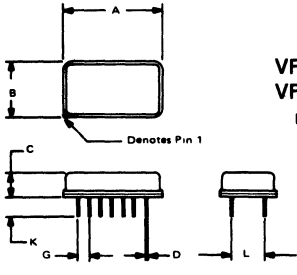
MODEL	VFC42			VFC52			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Full Scale Frequency		10			100		kHz
INPUT							
Analog Input (V/F)							
Voltage Range	0		10	0		+10	V
Current Range	0		+0.25	0		+0.25	mA
Input Bias Current (pin 14) Inverting Input		6	8		6	8	nA
Input Offset Voltage (trimmable to zero)		100	200		100	200	µV
Input Impedance (pin 1)	32	40	48	32	40	48	kΩ
Frequency Input (F/V) (pin 10)							
Logic Levels: Logic "0"	$-V_{CC}$		−0.6	$-V_{CC}$		−0.6	V
Logic "1"	+1.0		$+V_{CC}$	+1.0		$+V_{CC}$	V
Pulse Width Range (t_2, Fig. 6)	0.1		15	0.1		1.5	µsec
Impedance	1 ‖ 10	1.2 ‖ 10		1 ‖ 10	1.2 ‖ 10		MΩ ‖ pF
TRANSFER CHARACTERISTICS							
Transfer Functions	$f_{OUT} = V_{IN}$ (1.00 × 10^3) $V_{OUT} = f_{IN}$ (10 × 10^{-4})			$f_{OUT} = V_{IN}$ (1.00 × 10^4) $V_{OUT} = f_{IN}$ (10 × 10^{-5})			Hz VDC
Accuracy							
Full Scale Gain (adjustable to zero)		0 1	0.2		0.1	0.2	%
Linearity Error: 0.01Hz ≤ F ≤ 10kHz		0.005	0.01				% of FSR[1]
0.1Hz ≤ F ≤ 100kHz					0.025	0.05	% of FSR
Offset Error (pin 1)		0 001	0.002		0.001	0.002	% of FSR
Power Supply Sensitivity[2]			0.015			0.015	% of FSR/%
Temperature Stability							
Analog Input							
Full Scale Drift (gain and offset)							
Grade: BP (hot/cold)[3]		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
BM		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
SM		±30/±60	±50/±100		±30/±60	±50/±150	ppm/°C
Offset Drift							
Grade: BP		±1	±3		±1	±3	ppm of FSR/°C
BM		±1	±3		±1	±3	ppm of FSR/°C
SM		±1	±3		±1	±3	ppm of FSR/°C
Frequency Input							
Full Scale Drift (gain and offset)							
Grade. BP (hot/cold)[3]		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
BM		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
SM		±30/±60	±50/±100		±30/±60	±50/±150	ppm/°C
Dynamic Response							
Settling Time to within linearity specification for full scale input step	1 period of new frequency + 1µsec			1 period of new frequency + 1µsec			
Overload Recovery Time	1 period of new frequency + 1µsec			1 period of new frequency + 1µsec			
OUTPUT							
Voltage Output							
Voltage Range (I_O ≤ 5mA)	0 to +10			0 to +10			V
Output Current (V_O ≤ 7V)	+10			+10			mA
Output Impedance (closed loop)			1			1	Ω
Capacitive Load			100			100	pF
Frequency Output (open collector)							
Pulse Characteristics: Logic "1"			$+V_{PULL-UP}$			$+V_{PULL-UP}$	V
Logic "0" (at I_O ≤ −8mA)	0		+0.4	0		+0.4	V
Pulse Width	20	25		2.0	2.5		µsec
Output Sink Current (Logic "0", ≤ 0 4V)			8			8	mA
Output Leakage Current (Logic "1")			1			1	µA
Fall Time (I_{OUT} = −5mA, C_{LOAD} = 500pF)			400			400	nsec
POWER SUPPLY REQUIREMENTS							
Rated Supplies		±15			±15		V
Supply Range	±9		±20	±9		±20	V
Supply Drain (independent of operating frequency)		±6.5	±7.5		±6.5	±7.5	mA
TEMPERATURE RANGE							
Specification: BP, BM	−25		+85	−25		+85	°C
SM	−55		+125	−55		+125	°C
Operating: BM, SM	−55		+125	−55		+125	°C
BP	−55		+100	−55		+100	°C
Storage. BM, SM	−55		+125	−55		+125	°C
BP	−25		+85	−25		+85	°C

NOTES: (1) % of FSR = % of Full Scale Range. (2) Rated at full scale input and ±15V supplies. (3) Hot = +20°C to highest rated temperature; cold = lowest rated temperature to +20°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±22V
Output Sink Current (F_{output})	50mA
Output Current (V_{output})	+20mA
Input Voltage, Pin 14	±Supply
Input Voltage, Pin 1	±Supply
Storage Temperature Range	
Grade: BM, SM	−55°C to +125°C
BP	−25°C to +85°C

MECHANICAL



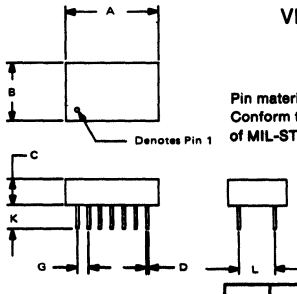
VFC42BM, VFC42SM
VFC52BM, VFC52SM

Hermetic Metal Package
14-Pin DIP

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	860	880	21 84	22 35
B	490	510	12 45	12 95
C	170	250	4 32	6 35
D	016	021	0 41	0 53
G	100 BASIC		2.54 BASIC	
H	115	155	2 92	3 94
K	150	300	3 81	7 62
L	300 BASIC		7 62 BASIC	
R	080	120	2 03	3 05

Pin numbers shown for reference only
Numbers are not marked on package

Tolerance (inches): .xxx ±0.005; .xx ±0.02
Connector: 14-pin DIP (145MC)
Case Material: Base - gold plated kovar, Cap - nickel-plated kovar or steel
Pin material and plating compositions: Conforms to MIL-STD-883, Method 2003 (solderability) except paragraph 3.2 (aging).
Hermeticity: Conforms to MIL-STD-883, Method 1014, Condition C, Step 1, Fluorocarbon (gross leak).



VFC42BP, VFC52BP

Epoxy Package
14-Pin DIP

Pin material and plating composition:
Conform to Method 2003 (solderability)
of MIL-STD-883 (except paragraph 3.2).

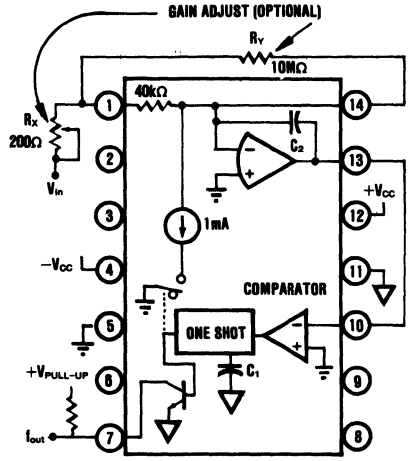
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

Pin numbers shown for reference only.
Numbers are not marked on package.

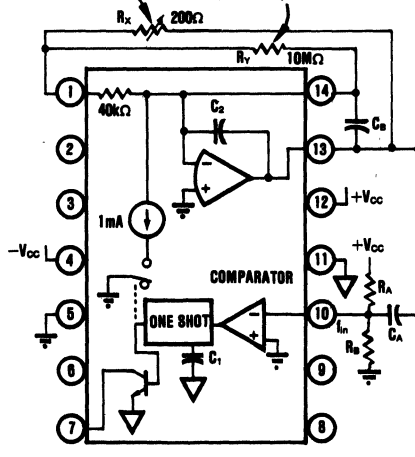
Tolerance (inches): .xxx ±0.005
.xx ±0.02
Connector: 14-pin DIP (145MC)
Case Material: Epoxy

CONNECTION DIAGRAMS

V/F Operation



F/V Operation



OPERATING INSTRUCTIONS

VFC42 and VFC52 can be connected for either V/F or F/V operation. Only one external component, the output pull-up resistor, is required for V/F operation. F/V operation requires the pull-up resistor and input biasing components. Gain error is the most significant error in either configuration and may be nulled out with the optional trim circuit (R_X and R_Y). The offset error is laser trimmed at the factory and no external adjustment is required.

Power Supply Consideration: Power supplies stable to within ±1% are recommended to maintain conversion accuracy. Each supply should be bypassed with 0.01μF capacitors located as close to the VFC as possible.

VOLTAGE-TO-FREQUENCY OPERATION

Calculating the Value of Pull-Up Resistor, R_P: The open collector output can be used to drive DTL, TTL, CMOS or discrete circuits. The maximum collector current allowed for TTL circuits in logic 0 is 8mA. R_P may be calculated by this equation:

$$R_P \text{ min} = V \text{ pull-up}/(8mA - i_{LOAD}).$$

A 10% carbon composition resistor is suitable for this purpose. The collector current may be as great as 30mA if a logic 0 voltage of 1.0V is tolerable.

Gain Adjustment Procedure: Connect R_X and R_Y as shown in Connection Diagram. Apply positive full scale voltage to the input and adjust R_X until 10kHz ±1Hz (VFC42) or 100kHz ±10Hz (VFC52) is obtained at f_{OUT}. R_X and R_Y should have temperature coefficients of <500ppm. These external components will add less than 5ppm/°C to temperature drift.

FREQUENCY-TO-VOLTAGE OPERATION

Input Characteristics: VFC42 and VFC52 can be connected as frequency-to-voltage converters as shown in Connection Diagram. f_{IN} should be a positive pulse train with minimum pulse width of 1.0μsec and rise and fall times of ≤ 300nsec. The input train (f_{IN}) is differential and applied to the input of the comparator (pin 10) (see Figure 2). Threshold voltage of the comparator lies between −0.6 and +1.0V. When comparator input is less than −0.6V it triggers the one-shot.

Selecting R_A, R_B, and C_A Input components R_A, R_B and C_A are selected so that the trigger voltage (V_T) is more negative than −0.6V and transition time (t_2) is between 0.3μsec and 15μsec for VFC42 and between 0.3μsec and 1.5μsec for VFC52. Table I give values for input components for several common signal sources. Values for R_A, R_B and C_A may be selected by the user when input signal characteristics differ from those listed. Conditions described above for trigger voltage and transition time must be observed.

TABLE I. F/V Input Component Selection

Input Type	V_{INPUT} (V)		V_{BIAS}	VFC42			VFC52		
	Low	High	(V)	R_A (kΩ)	R_B (kΩ)	C_A (pF)	R_A (kΩ)	R_B (Ω)	C_A (pF)
TTL	≤+0.4	≥+2.8	+1.1	12	1.0	1000	8.2	680	680
5V CMOS	≤+0.5	≥+4.5	+1.2	18	1.6	2200	9.1	820	680
10V CMOS	≤+1.0	≥+9.0	+1.1	12	1.0	2200	6.2	510	680
15V CMOS	≤+1.5	≥+13.5	+1.1	12	1.0	2200	6.2	510	680

Equations to calculate trigger voltage and transition time are:

$$V_T = V_B + V_{in}(e^{-t_1/\tau} - 1)$$

$$t_2 = -\tau \ln\left[\frac{1 - V_B}{V_{in}(e^{-t_1/\tau} - 1)}\right]$$

V_B = Bias voltage on pin 10

V_{in} = Input pulse amplitude

t_1 = Input pulse width

τ = Time constant of R_A, R_B C_A as connected

If input pulse amplitude is greater than $+V_{CC} - 1V$, a voltage larger than $+V_{CC}$ will be applied to pin 10. Since this may damage the unit, a diode connected across R_A with the cathode tied to $+V_{CC}$ is required.

Output Characteristics: Selecting C_B: Output ripple voltage amplitude is inversely proportional to the input frequency and to the value of the integrating capacitance, $C_2 + C_B$. Conversely, time required for the output to settle is directly proportional to the value of $C_2 + C_B$ and is least with small values of $C_2 + C_B$. There is, therefore, a trade-off between output ripple amplitude and output settling time.

Because ripple amplitude is greatest at lowest input frequency it is at this point where the trade-off will usually be made. Ripple voltage and integrating capacitance value are related in this manner:

$$C_B = \frac{-(25 \times 10^{-6})t_{sec}}{\ln\left[1 - \frac{V_{Ripple}}{30V}\right]} \text{ farads}$$

where t is equal to 25μsec in the VFC42 and 2.5μsec in the VFC52 and C is the integrating capacitance.

Calculating output response time versus integrating capacitance is an iterative process and is plotted in Figure 3. These curves are for zero to full scale input frequency transitions. If faster response time with lower ripple voltage is desired, a low-pass filter can be connected in series with the output.

Gain Adjustment Procedure: Connect R_X and R_Y as shown in Connection Diagram. Apply full scale frequency to the input and adjust R_X until the full scale voltage is +10V ±1mV (discounting ripple). R_X and R_Y should have temperature coefficients of < 500ppm. These external components will add less than 5ppm/°C to temperature drift.

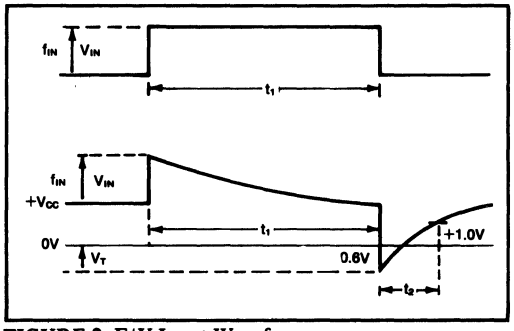


FIGURE 2. F/V Input Waveforms.

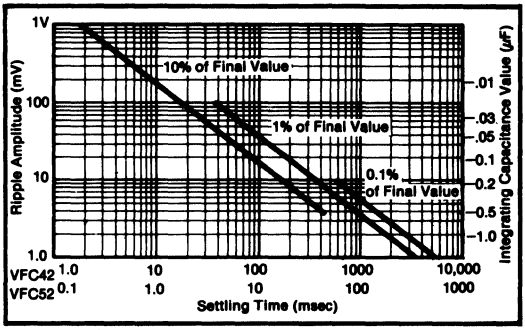


FIGURE 3. F/V Mode Output Settling Time vs. Ripple Voltage Amplitude for Full Scale Frequency Change.

APPLICATION

VFC42 and VFC52 can be used to convert analog data into a digital pulse train for transmission over long lines through high EMI environments. Illustrated in Figure 4 is a V/F, F/V combination that can be used to transmit analog data of 0 to +10V over a 100Ω shielded, twisted-pair. The voltage ripple amplitude at the output will be 10mV for a 10V output and the settling time for a full scale 0 to +10V change is 60 milliseconds.

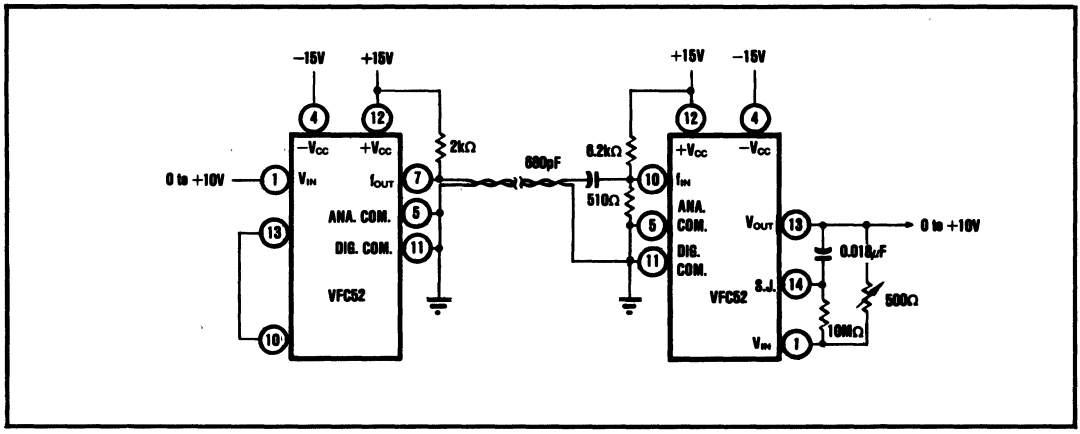


FIGURE 4. V/F, F/V Data Transmission Circuit.

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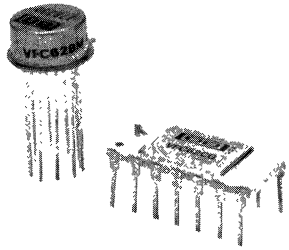


VFC62

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- HIGH LINEARITY, 12 to 14 bits
  ±0.005% max at 10kHz FS
  ±0.03% max at 100kHz FS
  ±0.1% typ at 1MHz FS
- 6-DECADE DYNAMIC RANGE
- 20ppm/°C max GAIN DRIFT
- OUTPUT DTL/TTL/CMOS COMPATIBLE
- ACTIVE PULL-UP OUTPUT

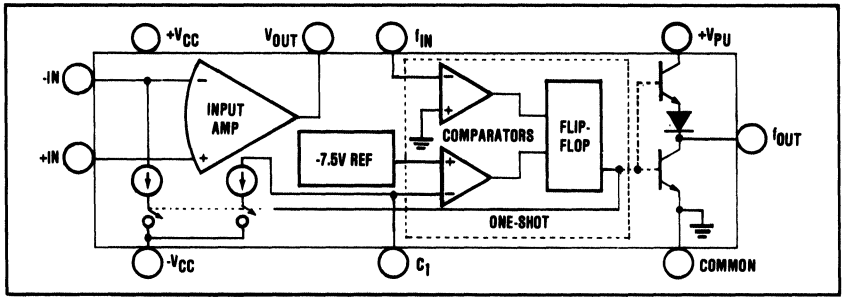
APPLICATIONS

- INEXPENSIVE A/D AND D/A CONVERTER
- DIGITAL PANEL METERS
- 2-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY
- FM MOD/DEMOD OF TRANSDUCER SIGNALS
- PRECISION LONG TERM INTEGRATOR
- HIGH RESOLUTION OPTICAL LINK FOR ISOLATION
- AC LINE FREQUENCY MONITOR
- MOTOR SPEED MONITOR AND CONTROL

DESCRIPTION

The VFC62 monolithic voltage-to-frequency and frequency-to voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. In the noise-immune digital form the analog signal may be transmitted long distances without degradation. It may be converted to a binary number with a counter or microprocessor or may be returned to analog form using a frequency-to-voltage converter.

The digital output is an active pull-up type which provides better load driving capability than the usual open collector outputs. Output pulses are DTL, TTL and CMOS compatible. High accuracy (±0.005% max nonlinearity at 10kHz) is achieved with relatively few external components. Only one resistor and two capacitors are required.



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PDS-484D

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC power supply unless otherwise noted

CHARACTERISTICS	CONDITIONS	VFC62BG/BM/SM MIN	VFC62BG/BM/SM TYP	VFC62BG/BM/SM MAX	VFC62CG/CM MIN	VFC62CG/CM TYP	VFC62CG/CM MAX	UNITS
V/F CONVERTER $f_{OUT} = V_{IN}/7\ 5\ R_1C_1$, Figure 4								
INPUT TO OP AMP								
Voltage Range(1)	Fig 4 with $e_2 = 0$	> 0		Note 2	*		*	V
	Fig 4 with $e_1 = 0$	< 0		-10	*		*	V
Current Range(1)	$I_{IN} = V_{IN}/R_{IN}$	+0.25		+750	*		*	µA
Bias Current								
Inverting Input			4	8		*	*	nA
Noninverting Input			10	30		*	*	nA
Offset Voltage(3)				±0 15			*	mV
Offset Voltage Drift			±5			*		µV/°C
Differential Impedance		300 ‖ 5	650 ‖ 5		*	*		kΩ ‖ pF
Common-mode								
Impedance		300 ‖ 3	500 ‖ 3		*	*		kΩ ‖ pF
ACCURACY								
Linearity Error(1)(4)(5)	Fig 4 with e_2 + = 0(6)							
	0 01Hz ≤ f_{OUT} ≤ 10kHz		±0 004	±0 005		±0.0015	±0 002	% of FSR
	0 1Hz ≤ f_{OUT} ≤ 100kHz		±0 008	±0.03		*	*	% of FSR
	1Hz ≤ f_{OUT} ≤ 1MHz		±0 1			*		% of FSR
Offset Error	Input Offset Voltage(3)			±15			*	ppm of FSR
Offset Drift(7)			±0 5			*		ppm of FSR/°C
Gain Error(3)			±5	±10			*	% of FSR
Gain Drift(7)	f = 10kHz			50			20	ppm of FSR/°C
Full Scale Drift	f = 10kHz			50			20	ppm of FSR/°C
(offset drift & gain drift(7)(8)(9)								
Power Supply Sensitivity	±V_{CC} = 14VDC to 18VDC			±0.015			*	% of FSR/%
DYNAMIC RESPONSE								
Full Scale Frequency	C_{LOAD} ≤ 50pF			1			*	MHz
Dynamic Range		6			*			decades
Settling Time	(V/F) to specified linearity for a full scale input step		Note 10			*		
Overload Recovery	< 50% overload		Note 10			*		
ACTIVE PULL-UP OUTPUT								
Voltage, Logic "0"	I_{SINK} = 8mA, max			0 4			*	V
Voltage, Logic "1"		V_{PU} - 2 6		V_{PU}	*		*	V
Duty Cycle at FS	For Best Linearity		25			*		%
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF		100			*		nsec
F/V CONVERTER V_{OUT} = 7.5 R_1C_1 F_{IN}, Figure 9								
INPUT TO COMPARATOR								
Impedance		50 ‖ 10	150 ‖ 10		*	*		kΩ ‖ pF
Logic "1"		+1.0		+V_{CC}	*		*	V
Logic "0"		-V_{CC}		-0.05	*		*	V
Pulse-width Range		0 25			*			µsec
OUTPUT FROM OP AMP								
Voltage	I_O = 6mA	0 to +10			*	*		V
Current	V_O = 7VDC	+10			*			mA
Impedance	Closed-loop			0 1			*	Ω
Capacitive Load	Without oscillation			100			*	pF
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range, V_{CC}		±13		±20	*		*	V
Pull-up Voltage		+3 5		+V_{CC}	*		*	V
Quiescent Current	not including load current		±6	±7 5		*	*	mA
TEMPERATURE RANGE								
Specification								
B and C Grades				-25 to +85				°C
S Grade				-55 to +125				°C
Operating								
B and C Grades				-25 to +85				°C
S Grade				-55 to +125				°C
Storage		-65		+150	-65		+150	°C

*Specification the same as for VFC62BG/BM/SM

NOTES
1. A 25% duty cycle at full scale (0.25mA input current) is recommended where possible to achieve best linearity.
2. Determined by R_{IN} and full scale current range constraints.
3. Adjustable to zero. See Offset and Gain Adjustment section
4. Linearity error at any operating frequency is defined as the deviation from a straight line drawn between the full scale frequency and 0 1% of full scale frequency See Discussion of Specifications section
5. When offset and gain errors are nulled, at an operating temperature, the linearity error determines the final accuracy.
6. For e_1 = 0 typical linearity errors are 0.01% at 10kHz, 0 2% at 100kHz
7. Exclusive of external components drift
8. FSR = Full Scale Range (corresponds to full scale frequency and full scale input voltage).
9. Positive drift is defined to be increasing frequency with increasing temperature.
10. One pulse of new frequency plus 50nsec typical

ABSOLUTE MAXIMUM RATINGS

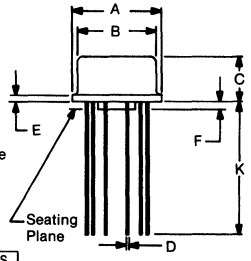
Supply Voltages	±20V
Output Sink Current at f_{OUT}	50mA
Output Current at V_{OUT}	+20mA
Input Voltage, -Input	±V_{CC}
Input Voltage, +Input	±V_{CC}
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	+300°C

MECHANICAL

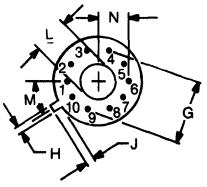
VFC62BM, CM/SM TO-100 PACKAGE

NOTE: Leads in true position within .010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.



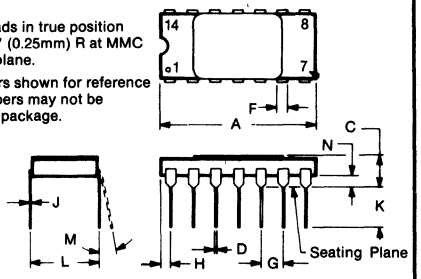
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	370	8 51	9 40
B	305	335	7 75	8 51
C	165	185	4 19	4 70
D	.016	.021	0.41	0 53
E	010	040	0.25	1 02
F	.010	.040	0 25	1 02
G	230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	029	.045	0 74	1.14
K	.500	—	12.70	—
L	120	160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05



VFC62BG/CG CERAMIC DUAL-IN-LINE

NOTE: Leads in true position within .010" (0.25mm) R at MMC at seating plane.

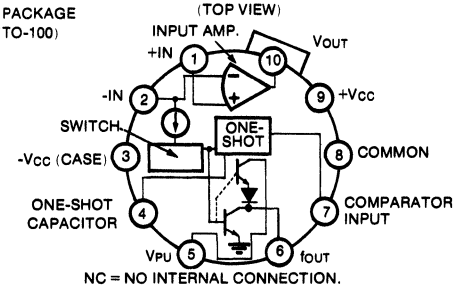
Pin numbers shown for reference only. Numbers may not be marked on package.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	670	710	17.02	18.03
C	.065	170	1.65	4 32
D	.015	.021	0 38	0.53
F	045	.060	1 14	1 52
G	100 BASIC		2 54 BASIC	
H	.025	.070	0.64	1.78
J	.008	012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.009	.060	0.23	1.52

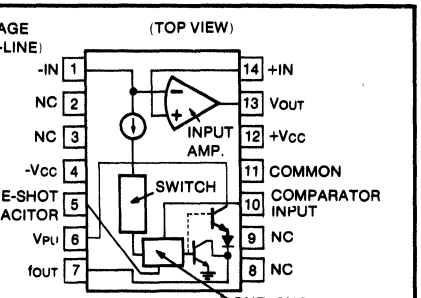
PIN CONFIGURATIONS

M PACKAGE (TO-100) (TOP VIEW)



NC = NO INTERNAL CONNECTION.
EXTERNAL CONNECTION PERMITTED.

G PACKAGE (DUAL-IN-LINE) (TOP VIEW)



(TOP VIEW)

DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (100% full scale input or frequency and 0.1% of full scale called zero). Linearity is the most demanding measure of voltage-to-frequency converter performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. Once the full scale frequency is chosen, the linearity is a function of operating frequency as it varies between zero and full scale. Examples for 10kHz full scale are shown in Figure 2. Best linearity is achieved at lower gains ($\Delta f_{OUT}/\Delta V_{IN}$) with operation as close to the chosen full scale frequency as possible.

The high linearity of the VFC62 makes the device an excellent choice for use as the front end of A/D converters with 12- to 14-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire digital transmission).

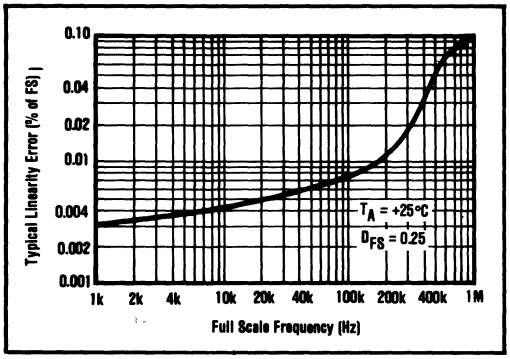


FIGURE 1. Linearity Error vs Full Scale Frequency.

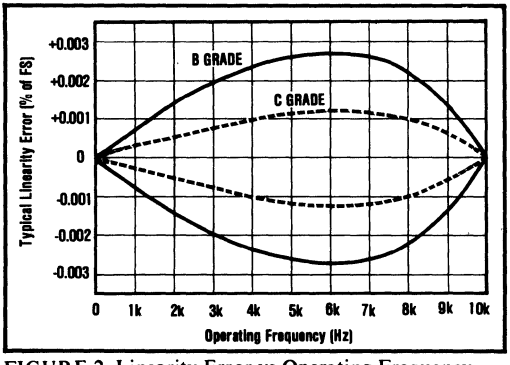


FIGURE 2. Linearity Error vs Operating Frequency.

FREQUENCY STABILITY VS TEMPERATURE

The full scale frequency drift of the VFC62 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 10kHz. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially R_1 and C_1) must be added to the drift of the VFC62.

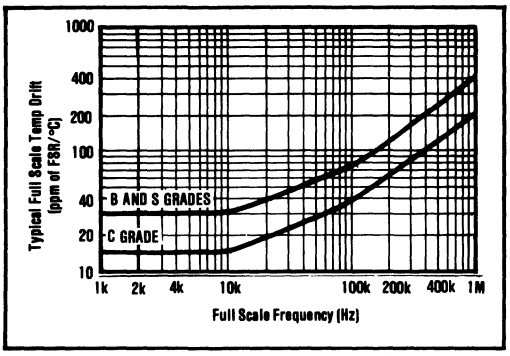


FIGURE 3. Full Scale Drift vs Full Scale Frequency.

RESPONSE

Response of the VFC62 to changes in input signal level is specified for a full scale step, and is 50nsec plus 1 pulse of the new frequency. For a 10V input signal step with the VFC62 operating at 100kHz full scale, the settling time to within ±0.01% of full scale is 10μsec.

THEORY OF OPERATION

The VFC62 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. The circuit shown in Figure 4 is composed of an input amplifier, two comparators and a flip-flop (forming a one-shot), two switched current sinks, and an active pull-up output transistor stage. Essentially the input amplifier acts as an integrator that produces a two-part ramp. The first part is a function of the input voltage, and the second part is dependent on the input voltage and current sink. When a positive input voltage is applied at V_{IN}, a current will flow through the input resistor, causing the voltage at V_{OUT} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_1$. During this time the constant current sink is disabled by the switch. Note, this period is only dependent on V_{IN} and the integrating components.

When the ramp reaches a voltage close to zero, comparator A sets the flip-flop. This closes the current sink switches as well as changing f_{OUT} from logic 0 to logic 1. The ramp now begins to ramp up, and 1mA charges through C_1 until V_{C1} = -7.5V. Note this ramp period is dependent on the 1mA current sink, connected to the negative input of the op amp, as well as the input voltage. At this -7.5V threshold comparator B resets the flip-flop, and the ramp voltage begins to ramp down again before the input amplifier has a chance to saturate. In effect the comparators and flip-flop form a one-shot whose period is determined by the internal reference and a 1mA current sink plus the external capacitor, C_1. After the one-shot resets, f_{OUT} changes back to logic 0 and the cycle begins again.

The transfer function for the VFC62 is derived as follows

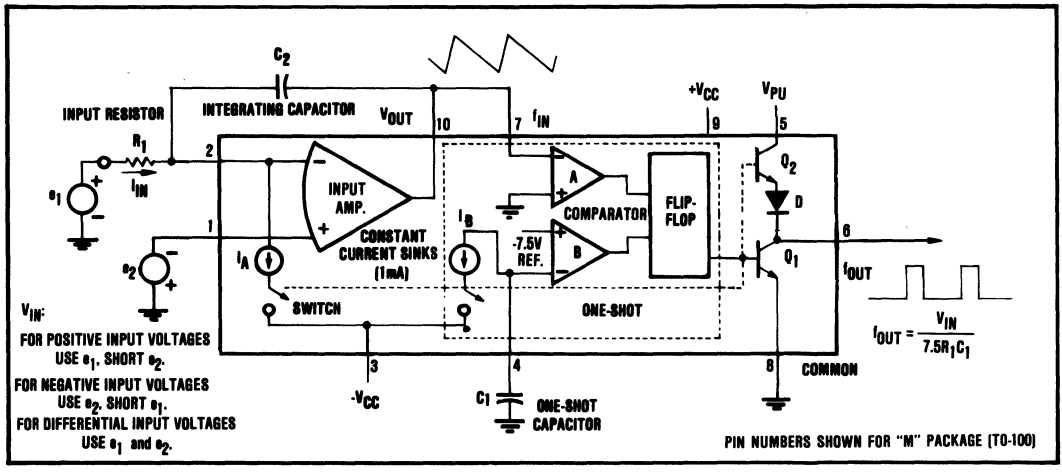


FIGURE 4. Functional Block Diagram of the VFC62.

for the circuit shown in Figure 4. Detailed waveforms are shown in Figure 5.

$$f_{OUT} = \frac{1}{t_1 + t_2} \quad (1)$$

In the time $t_1 + t_2$, the integrator capacitor C_2 charges and discharges but the net voltage change is zero.

$$\text{Thus } \Delta Q = 0 = I_{IN}\, t_1 + (I_{IN} - I_A)\, t_2 \quad (2)$$

$$\text{So that } I_{IN}\,(t_1 + t_2) = I_A\, t_2 \quad (3)$$

$$\text{But since } t_1 + t_2 = \frac{1}{f_{OUT}} \text{ and } I_{IN} = \frac{V_{IN}}{R_1} \quad (4), (5)$$

$$f_{OUT} = \frac{V_{IN}}{I_A R_1 t_2} \quad (6)$$

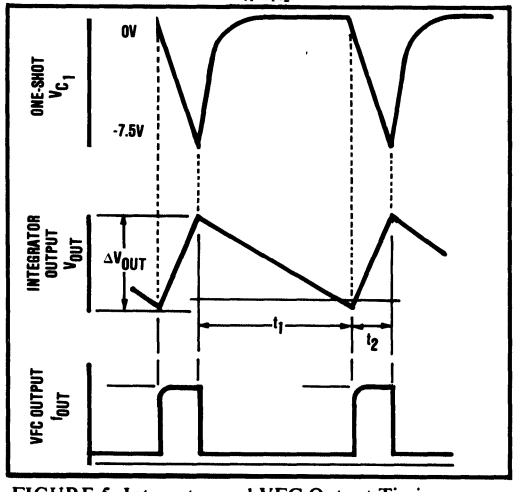


FIGURE 5. Integrator and VFC Output Timing.

In the time t_2, I_B charges the one-shot capacitor C_1 until its voltage reaches -7.5V and trips comparator B.

$$\text{Thus } t_2 = \frac{C_1\, 7.5}{I_B} \quad (7)$$

$$\text{Using (7) in (6) yields } f_{OUT} = \frac{V_{IN}}{7.5\, R_1 C_1} \times \frac{I_B}{I_A} \quad (8)$$

$$\text{Since } I_A = I_B \text{ the result is}$$

$$f_{OUT} = \frac{V_{IN}}{7.5\, R_1 C_1} \quad (9)$$

Since the integrating capacitor, C_2, affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to I_{IN}, since this parameter will add directly to the gain error of the VFC. C_1, which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.

The operation of the VFC62 as a highly linear frequency-to-voltage converter, follows the same theory of operation as the voltage-to-frequency converter. e_1 and e_2 are shorted and F_{IN} is disconnected from V_{OUT}. F_{IN} is then driven with a signal which is sufficient to trigger comparator A. The one-shot period will then be determined by C_1 as before, but the cycle repetition frequency will be dictated by the digital input at F_{IN}.

DUTY CYCLE

The duty cycle (D) of the VFC is the ratio of the one-shot period (t_2) or pulse width, PW, to the total VFC period ($t_1 + t_2$). For the VFC62, t_2 is fixed and $t_1 + t_2$ varies as the input voltage. Thus the duty cycle is a function of the input voltage. Of particular interest is the duty cycle at full scale frequency, D_{FS}, which occurs at full scale input. D_{FS} is a user-determined parameter which affects linearity.

$$D_{FS} = \frac{t_2}{t_1 + t_2} = PW \times f_{FS}$$

Best linearity is achieved when D_{FS} is 25%. By reducing equations (7) and (9) it can be shown that

$$D_{FS} = \frac{V_{IN}\ max\ /\ R_1}{1mA} = \frac{I_{IN}\ max}{1mA}$$

Thus $D_{FS} = 0.25$ corresponds to $I_{IN}\ max = 0.25mA$.

INSTALLATION AND OPERATING INSTRUCTIONS

VOLTAGE-TO-FREQUENCY CONVERSION

The VFC62 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.

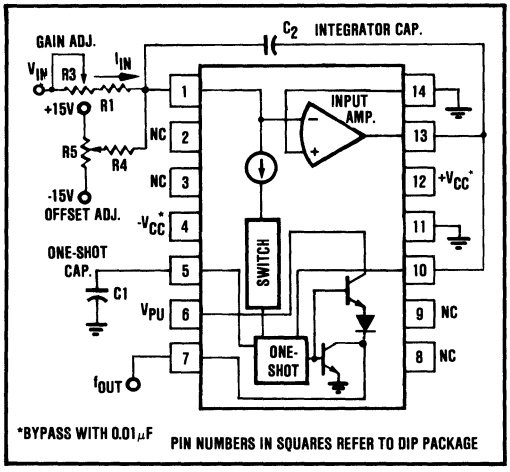


FIGURE 6. Connection Diagram for V/F Conversion, Positive Input Voltages.

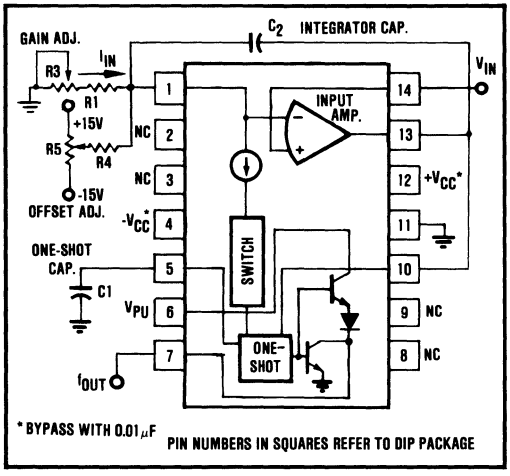


FIGURE 7. Connection Diagram for V/F Conversion, Negative Input Voltages.

EXTERNAL COMPONENT SELECTION

In general the design sequence consists of: (1) choosing f_{MAX}, (2) choosing the duty cycle at full scale ($D_{FS} = 0.25$ typically), (3) determining the input resistor, R_1 (Figure 4), (4) calculating the one-shot capacitor, C_1, and (5) selecting the integrator capacitor C_2.

Input Resistors R_1 and R_3

The input resistance (R_1 and R_3 in Figures 6 and 7) is calculated to set the desired input current at full scale input voltage. This is normally 0.25mA to provide a 25% duty cycle at full scale input and output. Values other than $D_{FS} = 0.25$ may be used but linearity will be affected. The nominal value of R_1 is

$$R_1 = \frac{V_{IN}\ max}{0.25mA} \qquad (10)$$

If gain trimming is to be done, the nominal value is reduced by the tolerance of C_1 and the desired trim range. R_1 should have a very-low temperature coefficient since its drift adds directly to the errors in the transfer function.

One-Shot Capacitor, C_1

This capacitor determines the duration of the one-shot pulse. From equation (9) the nominal value is

$$C_{1\ nom} = \frac{V_{IN}}{7.5\ R_1\ f_{OUT}} \qquad (11)$$

For the usual 25% duty at $f_{MAX} = V_{IN}/R_1 = 0.25mA$ there is approximately 15pF of residual capacitance so that the design value is

$$C_1\ (pF) = \frac{33 \times 10^6}{f_{FS}} - 15 \qquad (12)$$

where f_{FS} is the full scale output frequency in Hz. The temperature drift of C_1 is critical since it will add directly to the errors of the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize stray capacitance associated with C_1. It should be mounted as close to the VFC62 as possible. Figure 8 shows pulse width and full scale frequency for various values of C_1 at $D_{FS} = 25\%$.

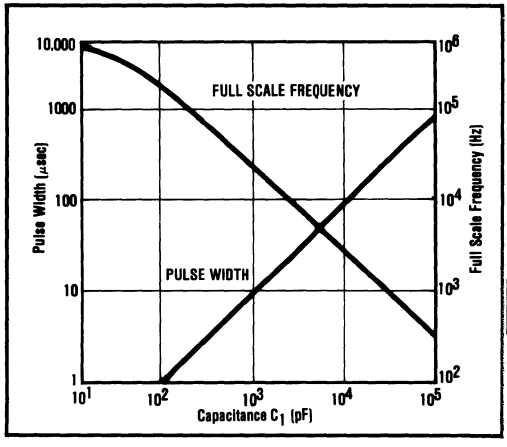


FIGURE 8. Output Pulse Width ($D_{FS} = 0.25$) and Full Scale Frequency vs External One-shot Capacitance.

Integrating Capacitor, C_2

Since C_2 does not occur in the V/F transfer function equation (9), its tolerance and temperature stability are not important; however, leakage current in C_2 causes a gain error. A ceramic type is sufficient for most applications. The value of C_2 determines the amplitude of V_{OUT}. Input amplifier saturation, noise levels for the comparators and slew rate limiting of the integrator

determine a range of acceptable values,

$$C_2\,(\mu F) = \begin{cases} \frac{100}{f_{FS}}\ ;\ \text{if } f_{FS} \leqslant 100\text{kHz} \\ 0.001;\ \text{if } 100\text{kHz} < f_{FS} \leqslant 500\text{kHz} \\ 0.0005;\ \text{if } f_{FS} > 500\text{kHz} \end{cases} \quad (13)$$

Trimming Components R_3, R_4, R_5

R_5 nulls the offset voltage of the input amplifier. It should have a series resistance between 10kΩ and 100kΩ and a temperature coefficient less than 100ppm/°C. R_4 can be a 10% carbon film resistor with a value of 10MΩ.

R_3 nulls the gain errors of the converter and compensates for intitial tolerances of R_1 and C_1. Its total resistance should be at least 20% of R_1, if R_1 is selected 10% low. Its temperature coefficient should be no greater than five times that of R_1, to maintain a low drift of the R_3 - R_1 series combination.

OFFSET AND GAIN ADJUSTMENT PROCEDURES

To null errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 x full scale.
2. Adjust R_5 for proper output.
3. Apply the full scale input voltage.
4. Adjust R_3 for proper output.
5. Repeat steps 1 through 4.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC62 is 0.015% of FSR/% maximum. To maintain ±0.015% conversion, power supplies which are stable to within ±1% are recommended. These supplies should be bypassed as close as possible to the converter with 0.01μF capacitors.

Internal circuitry causes some current to flow in the common connection (pin 11 on DIP package). Current flowing into the f_{OUT} pin (logic sink current) will also contribute to this current. It is advisable to separate this common lead ground from the analog ground associated with the integrator input to avoid errors produced by these currents flowing through any ground return impedance.

DESIGN EXAMPLE

Given a full scale input of +10V, select the values of R_1, R_2, R_3, C_1, and C_2 for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

Selecting C_1 ($D_{FS} = 0.25$)

$C_1 = [(33 \times 10^6)/f_{MAX}] - 15$ $\quad [(66 \times 10^6)/f_{MAX}] - 15$ if $D_{FS} = 0.5$

$= [(33 \times 10^6)/100\text{kHz}] - 15$

$= 315\text{pF}$

Choose a 300pF NPO ceramic capacitor with 1% to 10% tolerance.

Selecting R_1 and R_3 ($D_{FS} = 0.25$)

$R_1 + R_3 = V_{IN}\ \text{max}/0.25\text{mA}$ $\quad V_{IN}\ \text{max}/0.5\text{mA}$ if $D_{FS} = 0.5$

$= 10\text{V}/0.25\text{mA}$

$= 40\text{k}\Omega$

Choose 32.4kΩ metal film resistor with 1% tolerance and R_3 = 10kΩ cermet potentiometer.

Selecting C_2

$C_2 = 10^2/F_{max}$

$= 10^2/100\text{kHz}$

$= 0.001\mu\text{F}$

Choose a 0.001μF capacitor with ±5% tolerance.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC62 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses zero. Choose C_3 to make t = 0.1T (see Figure 9). For input signals with amplitudes less than 5V, pin 10 should be biased closer to zero to insure that the input signal at pin 10 crosses the zero threshold. Errors are nulled following the procedure given on this page, using 0.001 x full scale frequency to null offset, and full scale frequency to null the gain error. Use equations from V/F calculations to find R_1, R_3, R_4, R_5, C_1 and C_2.

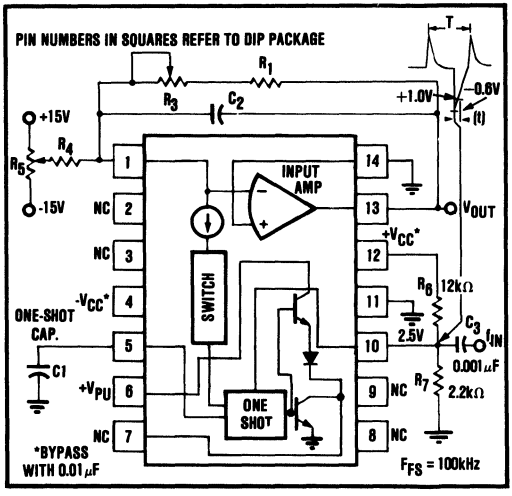


FIGURE 9. Connection Diagram for F/V Conversion.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC62 ideal for a variety of VFC applications. High accuracy allows the VFC62 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 14 bits.

Figures 10 - 14 show typical applications of the VFC62.

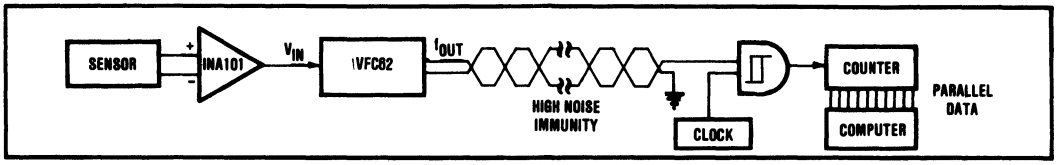


FIGURE 10. Inexpensive A/D with Two-Wire Digital Transmission Over Twisted Pair.

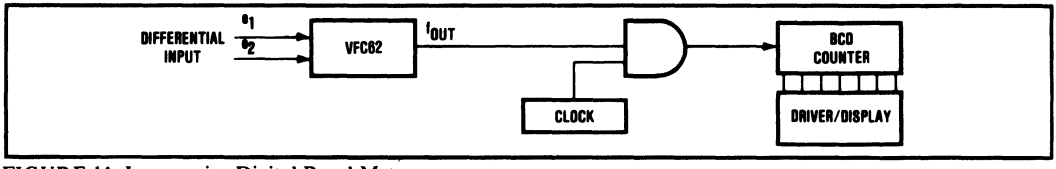


FIGURE 11. Inexpensive Digital Panel Meter.

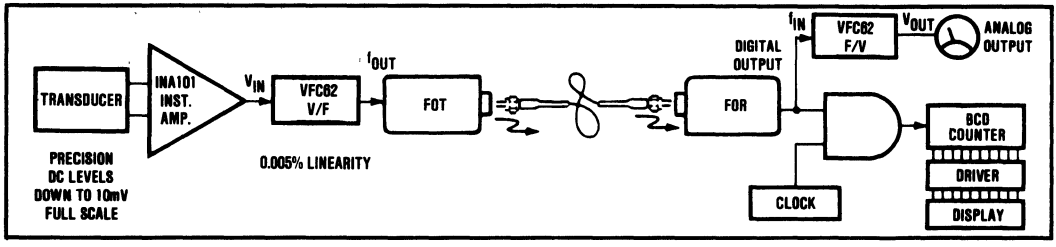


FIGURE 12. Remote Transducer Readout via Fiber Optic Link (analog and digital output).

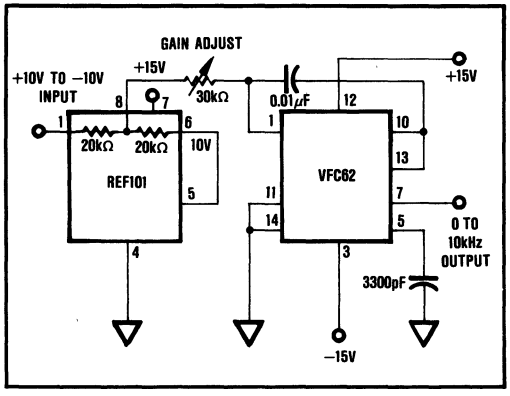


FIGURE 13. Bipolar input is accomplished by offsetting the input to the VFC with a reference voltage. Accurately matched resistors in the REF101 provide a stable half-scale output frequency at zero volts input.

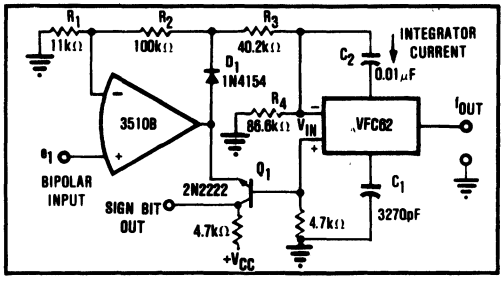


FIGURE 14. Absolute value circuit with the VFC62. Op amp, D_1 and Q_1 (its base-emitter junction functioning as a diode) provide full-wave rectification of bipolar input voltages. VFC output frequency is proportional to $|e_1|$. The sign bit output provides indication of the input polarity.

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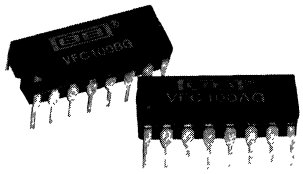


VFC100

AVAILABLE IN DIE FORM

Synchronized VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- FULL-SCALE FREQUENCY SET BY SYSTEM CLOCK, NO CRITICAL EXTERNAL COMPONENTS REQUIRED
- PRECISION 10V FULL-SCALE INPUT, 0.5% MAX GAIN ERROR
- ACCURATE 5V REFERENCE VOLTAGE
- EXCELLENT LINEARITY, 0.02% MAX AT 100kHz FS
  0.1% MAX AT 1MHz FS
- VERY-LOW GAIN DRIFT, 50ppm/°C

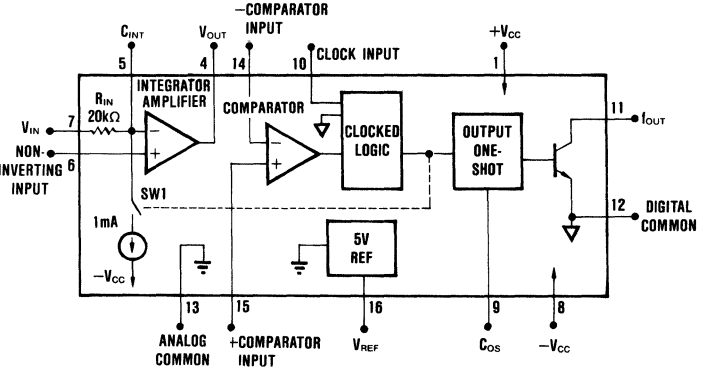
APPLICATIONS

- A/D CONVERSION
- PROCESS CONTROL
- DATA ACQUISITION
- VOLTAGE ISOLATION

DESCRIPTION

The VFC100 voltage-to-frequency converter is an important advance in VFCs. The well-proven charge balance technique is used, however, the critical reset integration period is derived from an external clock frequency. The external clock accurately sets an output full-scale frequency, eliminating error and drift from the external timing components required for other VFCs. A precision input resistor is provided which accurately sets a 10V full-scale input voltage. In many applications the required accuracy can be achieved without external adjustment.

The open collector active-low output provides fast fall time on the important leading edge of output pulses, and interfaces easily with TTL and CMOS circuitry. An output one-shot circuit is particularly useful to provide optimum output pulse widths for optical couplers and transformers to achieve voltage isolation. An accurate 5V reference is also provided which is useful for applications such as offsetting for bipolar input voltages, exciting bridges and sensors, and autocalibration schemes.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC supplies unless otherwise noted

PARAMETER	CONDITIONS	VFC100AG/SG MIN	VFC100AG/SG TYP	VFC100AG/SG MAX	VFC100BG MIN	VFC100BG TYP	VFC100BG MAX	UNITS
TRANSFER FUNCTION								
Voltage-to-Frequency Mode	$f_{OUT} = f_{CLOCK} \times (V_{IN}/20V)$							
Gain Error[1]	FSR = 100kHz		±0 5	±1		±0 2	±0 5	% of FSR
Linearity Error	FSR = 100kHz, over temp		±0 01	±0.025		"	±0 02	% of FSR
	FSR = 500kHz, C_{OS} = 60pF		±0 015			"	±0 05	% of FSR
	FSR = 1MHz, C_{OS} = 60pF		±0 025			"	±0 1	% of FSR
Gain Drift[2]	FSR = 100kHz		±70	±100		±30	±50	ppm of FSR/°C
Referred to Internal V_{REF}			10	±25		10	±15	ppm of FSR/°C
Offset Referred to Input			±1	±3		±1	±2	mV
Offset Drift			±12	±100		±6 5	±25	µV/°C
Power Supply Rejection	Full supply range		0 01			"		%/V
Response Time	to Step Input Change		One period of new output frequency plus one clock period					
Current-to-Frequency Mode	$f_{OUT} = f_{CLOCK} \times (I_{IN}/1mA)$							
Gain Error			±0 5	±1		±0 2	±0 5	% of FSR
Gain Drift[2]			±120	±200		±80	±140	ppm of FSR/°C
Frequency-to-Voltage Mode[3]	$V_{OUT} = 20V \times (f_{IN}/f_{CLOCK})$							
Gain Accuracy[1]	FSR = 100kHz		±0 5	±1		±0 2	±0 5	%
Linearity	FSR = 100kHz		±0 01	±0 025		"	±0 02	%
Input Resistor (R_{IN})								
Resistance		19 8	20	20 2	"	"	"	kΩ
Temperature Coefficient (T_C)[2]			±50	±100		"	"	ppm/°C
INTEGRATOR OP AMP								
V_{OS}[1]			±150	±1000		"	"	µV
V_{OS} Drift			±5			"		µV/°C
I_B			±50	±100		±25	±50	nA
I_{OS}			100	200		50	100	nA
A_{OL}	Z_{LOAD} = 5KΩ/10000pF	100	120		"	"		dB
CMRR		80	105		"	"		dBV
CM Range		−7 5		+0 1	"		"	V
V_{OUT} Range	Z_{LOAD} = 5kΩ/10000pF	−0 2		+12		"	"	V
Bandwidth			14			"		MHz
COMPARATOR INPUTS								
Input Current (operating)	$-11V < V_{COMPARATOR} < +V_{CC} - 2V$			5			"	µA
CLOCK INPUT (referenced to digital common)								
Frequency (maximum operating)			4 0			"		MHz
Threshold Voltage			1 4			"		V
	Over temperature	0 8		2 0	"		"	V
Voltage Range (operating)		$-V_{CC}$ + 2V		$+V_{CC}$	"		"	V
Input Current	$-V_{CC} < V_{CLOCK} < +V_{CC}$		0 5	5		"	"	µA
Rise Time				2			"	µsec
OPEN COLLECTOR OUTPUT (referenced to digital common)								
V_{OL}	I_{OUT} = 10mA			0 4			"	V
I_{OL}				15			"	mA
I_{OH} (off leakage)	V_{OH} = 30V		01	10		"	"	µA
Delay Time, positive clock edge to output pulse			300			"		nsec
Fall Time			100			"		nsec
Output Capacitance			5			"		pF
OUTPUT ONE-SHOT								
	Nominal PW_{OUT} = (5nsec/pF) × C_{OS} − 90nsec							
Pulse Width Out	C_{OS} = 300pF	1	1 4	2	"	"	"	µsec
REFERENCE VOLTAGE								
Accuracy	No load	4 90	5 0	5 10	4 95	"	5 05	V
Drift[2]			±60	±150		±40	±100	ppm/°C
Current Output	(Sourcing capability)	10				"		mA
Power Supply Rejection				0 015			0 015	%/V
Output Impedance			0 5	2		"	"	Ω
POWER SUPPLY								
Rated Voltage			±15			"		V
Operating Voltage Range (see Figure 9)	$+V_{CC}$	+7 5		+28 5	"		"	V
	$-V_{CC}$	−7 5		−28 5	"		"	V
Total Supply	$+V_{CC} - (-V_{CC})$	15		36	"		"	V
Digital Common		$-V_{CC}$ + 2		$+V_{CC} - 4$	"		"	V
Quiescent Current $+I_{CC}$	Over temperature		10 6	15		"	"	mA
$-I_{CC}$			9 6	15		"	"	mA

ELECTRICAL (CONT)

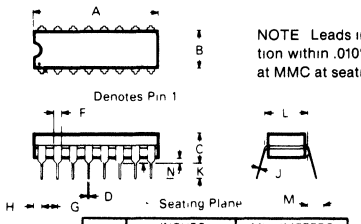
At T_A = +25°C and ±15VDC supplies unless otherwise noted

PARAMETER	CONDITIONS	VFC100AG/SG MIN	VFC100AG/SG TYP	VFC100AG/SG MAX	VFC100BG MIN	VFC100BG TYP	VFC100BG MAX	UNITS
TEMPERATURE RANGE								
Specification	AG/BG	−25		+85	*		*	°C
	SG	−55		+125				°C
Storage	AG/BG/SG	−65		+150	*		*	°C
θ Junction—ambient			150			*		°C/W
θ Junction—case			100			*		°C/W

*Specification same as AG grade

NOTES (1) Offset and gain error can be trimmed to zero See text. (2) Specified by the box method. (Max. − Min.) ÷ (Avg × ΔT) (3) Refer to detailed timing diagram in Figure 16 for frequency input signal timing requirements

MECHANICAL



NOTE Leads in true position within .010" (25mm) R at MMC at seating plane

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	760	885	19 30	22 48
B	220	280	5 59	7 11
C		200		5 08
D	015	023	0 38	0 58
F	030	070	0 76	1 78
G	100 BASIC		2 54 BASIC	
H	030	095	0 76	2 41
J	008	015	0 20	0 38
K	100		2 54	
L	300 BASIC		7 62 BASIC	
M		15°		15°
N	020	050	0 51	1 27

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($+V_{CC}$ to $-V_{CC}$)	36V
$+V_{CC}$ to Analog Common	28V
$-V_{CC}$ to Analog Common	28V
Integrator Out Short-Circuit-to-Ground	Indefinite
Integrator Differential Input	±10V
Integrator Common-Mode Input	$-V_{CC}$ +5V to +2V
V_{IN} (pin 7)	$\pm V_{CC}$
Clock Input	$\pm V_{CC}$
V_{REF} Out Short-Circuit-to-Ground	Indefinite
Pin 9 (C_{OS})	0 to $+V_{CC}$
f_{OUT} (referred to digital common)	−0 5V to 36V
Digital Common	$\pm V_{CC}$
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering 10sec)	300°C

ORDERING INFORMATION

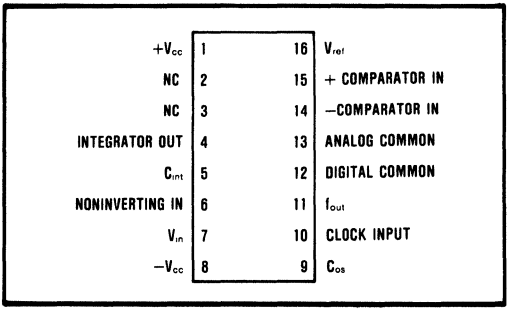
VFC100 (X) G

Basic Model Number

Performance Code
A, B = −25°C to +85°C
S = −55°C to +125°C

Ceramic Package

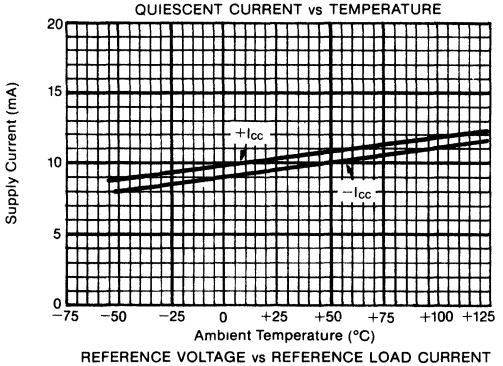
PIN CONFIGURATION



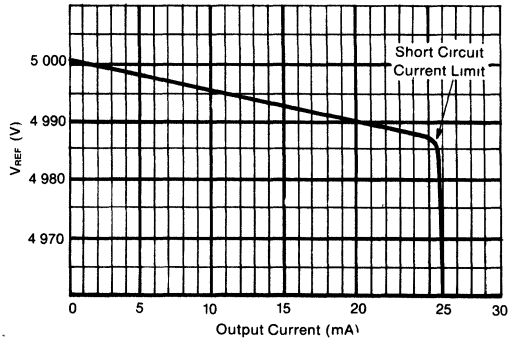
TYPICAL PERFORMANCE CURVES

At +25°C, $\pm V_{CC}$ = 15VDC, and in circuit of Figure 1 unless otherwise specified

QUIESCENT CURRENT vs TEMPERATURE



REFERENCE VOLTAGE vs REFERENCE LOAD CURRENT



THEORY OF OPERATION

The VFC100 monolithic voltage-to-frequency converter provides a digital pulse train output with an average frequency proportional to the analog input voltage. The output is an active low pulse of constant duration, with a repetition rate determined by the input voltage. Falling edges of the output pulses are synchronized with rising edges of the clock input.

Operation is similar to a conventional charge balance VFC. An input operational amplifier (Figure 1) is configured as an integrator so that a positive input voltage causes an input current to flow in R_{IN}. This forces the integrator output to ramp negatively. When the output of the integrator crosses the reference voltage (5V), the comparator trips, activating the clocked logic circuit. Once activated, the clocked logic awaits a falling edge of the clock input, followed by a rising edge (see Figure 2). On the rising edge, switch S1 is closed for one complete clock cycle, causing the reset current, I_1 to switch to the integrator input. Since I_1 is larger than the input current, I_{IN}, the output of the integrator ramps positively during the one clock cycle reset period. The clocked logic circuitry also generates a VFC output pulse during the reset period.

Unlike conventional VFC circuits, the VFC100 accurately derives its reset period from an external clock frequency. This eliminates the critical timing capacitor required by other VFC circuits. One period (from rising edge to rising edge) of the clock input determines the integrator reset period.

When the negative-going integration of the input signal crosses the comparator threshold, integration of the input signal will continue until the reset period can start (awaiting the necessary transitions of the clock). Output pulses are thus made to align with rising edges of the external clock. This causes the instantaneous output frequency to be a subharmonic of the clock frequency. The average frequency, however, will be an accurate analog of the input voltage.

A full scale input of 10V (or an input current of 0.5mA) causes a nominal output frequency equal to one half the

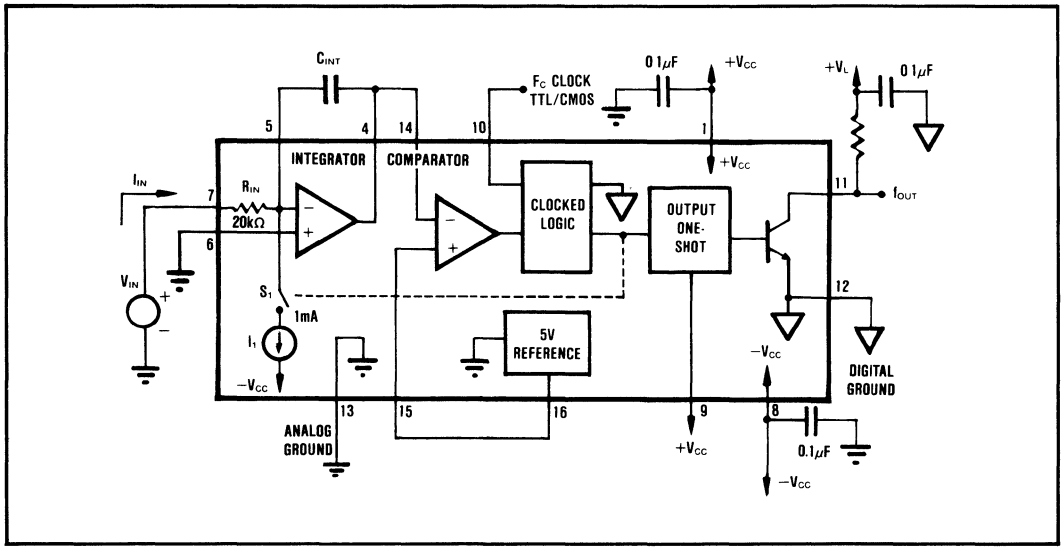


FIGURE 1. Circuit Diagram for Voltage-to-Frequency Mode.

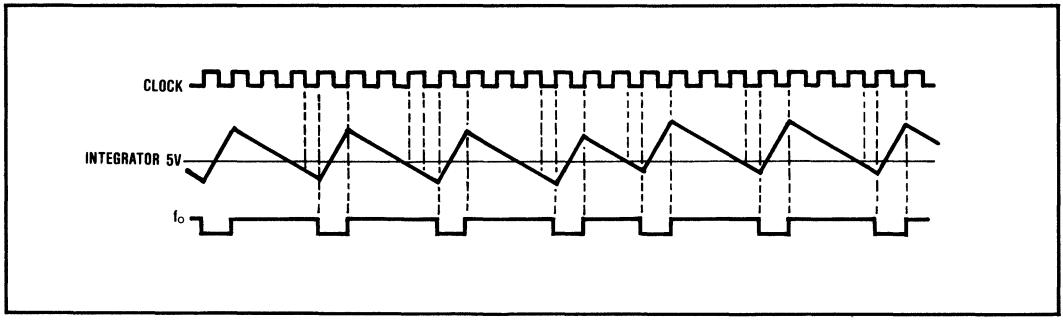


FIGURE 2. Timing Diagram for Voltage-to-Frequency Mode.

clock frequency. The transfer function is

$$f_{OUT} = (V_{IN}/20V)\, f_{CLOCK}$$

Figure 3 shows the transfer function graphically. Note that inputs above 10V (or 0.5mA) do not cause an increase in the output frequency. This is an easily detectable indication of an overrange input. In the overrange condition, the integrator amplifier will ramp to its negative output swing limit. When the input signal returns to within the linear range, the integrator amplifier will recover and begin ramping upward during the reset period.

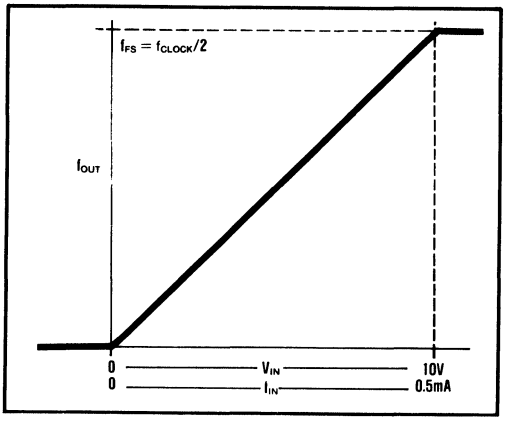


FIGURE 3. Transfer Function for Voltage-to-Frequency Mode.

INSTALLATION AND OPERATING INSTRUCTIONS

The integrator capacitor C_{INT} (see Figure 1) affects the magnitude of the integrator voltage waveform. Its absolute accuracy is not critical since it does not affect the transfer function. This allows a wide range of capacitance to produce excellent results. Figure 4 facilitates choosing an appropriate standard value to assure that the integrator waveform voltage is within acceptable limits. Good dielectric absorption properties are required to achieve best linearity. Mylar®, polycarbonate, mica, polystyrene, Teflon® and glass types are appropriate choices. The choice in a given application will depend on the particular value and size considerations. Ceramic capacitors vary considerably from type to type and some produce significant nonlinearities. Polarized capacitors should not be used.

Deviation from the nominal recommended +1V to −0.75V integrator voltage (as controlled by the integrator capacitor value) is permissible and will have a negligible effect on VFC operation. Certain situations may make deviations from the suggested integrator swing highly desirable. Smaller integrator voltages, for instance, allow more "headroom" for averaging noisy input signals. The VFC is a fully integrating input converter, able to reject large levels of interfering noise. This ability is limited only by the output voltage swing range of the integrator amplifier. By setting a small integrator voltage swing using a large C_{INT} value, larger levels of noise can be integrated without output saturation and loss of accuracy. For instance, with a 50kHz full-scale output and C_{INT} = 0.1μF, the circuit in Figure 1 can accurately average an input through the full 0 to 10V input range with 1V p-p superimposed 60Hz noise.

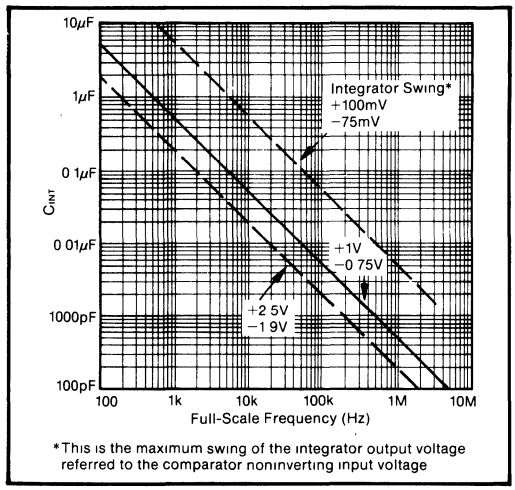


FIGURE 4. Integrator Capacitor Selection Graph.

The integrator output voltage should not be allowed to exceed +12V or −0.2V, otherwise saturation of the operational amplifier could cause inaccuracies. Operation with positive power supplies less than +15V will limit the output swing of the integrator operational amplifier. Smaller integrator voltage waveforms may be required to avoid output saturation of the integrator amplifier. See "Power Supply Considerations" for information on low voltage operation.

The maximum integrator voltage swing requirement is nearly symmetrical about the comparator threshold voltage (see Figure 12). One-third greater swing is required above the threshold than below it. Maximum demand on positive integrator swing occurs at low scale, while the negative swing is greatest just below full scale.

CLOCK INPUT

The clock input is TTL- and CMOS-compatible. Its input threshold is approximately 1.4V (two diode voltage drops) referenced to digital ground (pin 12). The clock "high" input may be standard TLL or may be as high as $+V_{CC} - 2V$. A CMOS clock should be powered from a voltage source at least 2V below the VFC100's $+V_{CC}$ to prevent overdriving the clock input. Alternatively, a resistive voltage divider may be used to limit the clock voltage swing to $+V_{CC} - 2V$ maximum. The clock input has a high input impedance, so no special drivers are required. Rise time in the transition region from 0.5V to 2V must be less than 2μsec for proper operation.

OUTPUT

The frequency output is an open collector current-sink transistor. Output pulses are active low such that the

output transistor is on only during the reset integration period (see Shortened Output Pulses). This minimizes power dissipation over the full frequency range and provides the fastest logic edge at the beginning of the output pulse where it is most desirable.

Interface to a logic circuit would normally be made using a pull-up resistor to the logic power supply. Selection of the pull-up resistor should be made such that no more than 15mA flows in the output transistor. The actual choice of the pull-up resistor may depend on the full-scale frequency and the stray capacitance on the output line. The rising edge of an output pulse is determined by the RC time constant of the pull-up resistor and the stray capacitance. Excessive capacitance will produce a rounding of the output pulse rising edge, which may create problems driving some logic circuits. If long lines must be driven, a buffer or digital line transmitter circuit should be used.

The synchronized nature of the VFC100 makes viewing its output on an oscilloscope somewhat tricky. Since all output pulses align with the clock, it is best to trigger and view the clock on one of the input channels and the output can then be viewed on another oscilloscope channel. Depending on the VFC input voltage, the output waveform may appear as if the oscilloscope is not properly triggered. The output might best be visualized by imagining a constant output frequency which is locked to a submultiple of the clock frequency with occasional extra pulses or missing pulses to create the necessary average frequency. It is these extra or missing pulses that make the output waveform appear as if the oscilloscope is not properly triggered. This is normal. Experimentation with the input voltage and oscilloscope triggering will generally allow a stable view of the output and provides an understanding of its nature.

SHORTENED OUTPUT PULSES

In normal operation, the negative output pulse duration is equal to one period of the clock input. Shorter output pulses may be useful in driving optical couplers or transformers for voltage isolation or noise rejection. This can be accomplished by connecting capacitor C_{OS} as shown in Figure 5. Pin 9 may be connected to $+V_{CC}$, deactivating the output one-shot circuit. The value of C_{OS} is chosen according to the curve in Figure 6. Output pulses cannot be made to exceed one clock period in duration. Thus, a C_{OS} value which would create an output pulse which is longer than one period of the clock will have the same effect as disabling the one-shot, causing the output pulse to last one clock period. The minimum practical pulse width of the one-shot circuit is approximately 100nsec. Using C_{OS} to generate shorter output pulses does not affect the output frequency or the gain equation.

REFERENCE VOLTAGE

Excellent gain drift is achieved by use of a precision internal 5V reference. This reference is brought to an external pin and can be used for a variety of purposes. It is used to offset the noninverting comparator input in voltage-to-frequency mode (although a precise voltage is not requried for this function). It is very useful in many other applications such as offsetting the input to handle bipolar input signals. It can source up to 10mA and sink

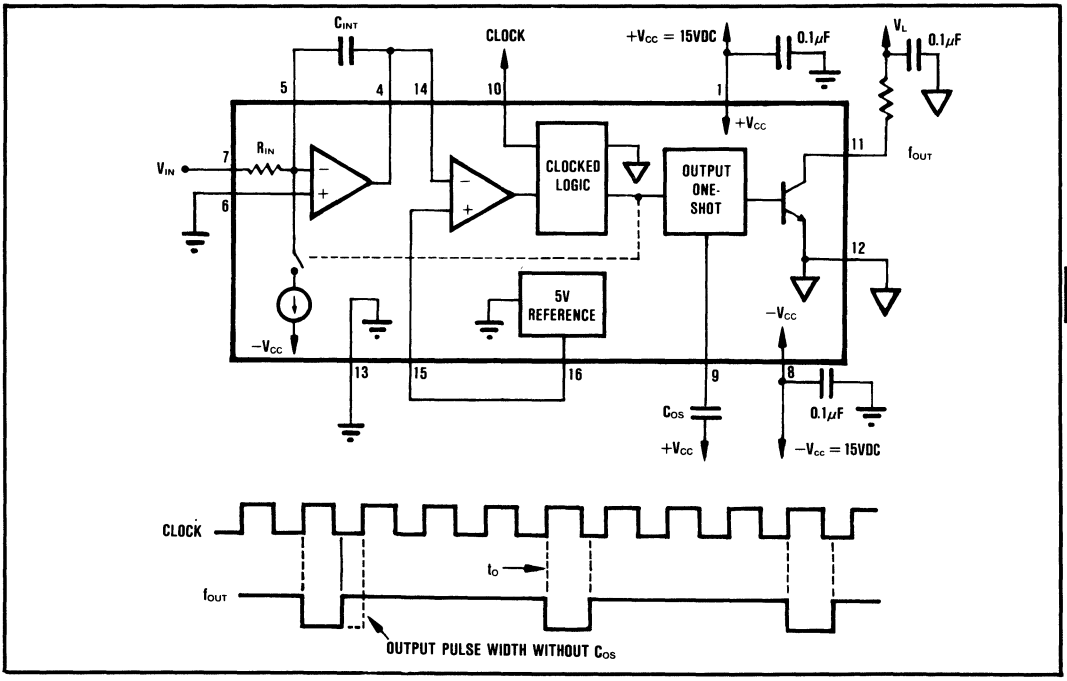


FIGURE 5. Circuit and Timing Diagram for Shortened Output Pulses.

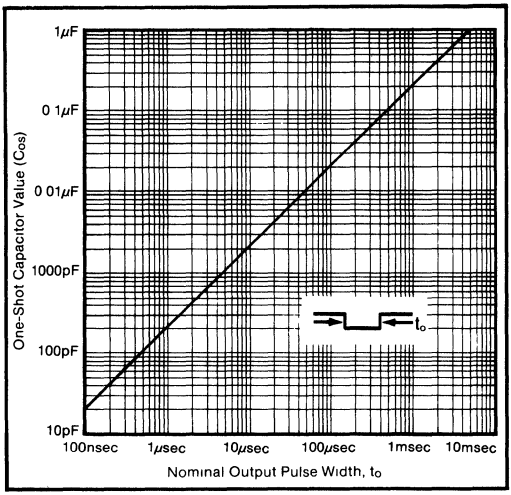


FIGURE 6. Output One-Shot Capacitor Selection Graph.

100μA. Heavy loading of the reference will change the gain of the VFC as well as affecting the external reference voltage. For instance, a 10mA load interacting with a 0.5Ω typical output impedance will change the VFC gain equation and reference voltage by 0.1%.

Figure 7 shows the reference used to offset the VFC transfer function to convert a −5V to +5V input to zero to 500kHz output. The circuit in Figure 8 uses the reference to excite a 300Ω bridge transducer. R_1 provides the majority of the current to the bridge while the V_{RLF} output supplies the balance and accurately controls the bridge voltage. The VFC gain is inversely proportional to the reference voltage, V_{RLF}. Since the bridge gain is directly proportional to its excitation voltage, the two equal and opposite effects cancel the effect of reference voltage drift on gain.

The reference output amplifier is specifically designed for excellent transient response to provide precision in a noisy environment. Although not required for normal operation, a 0.05μF bypasss capacitor from the reference

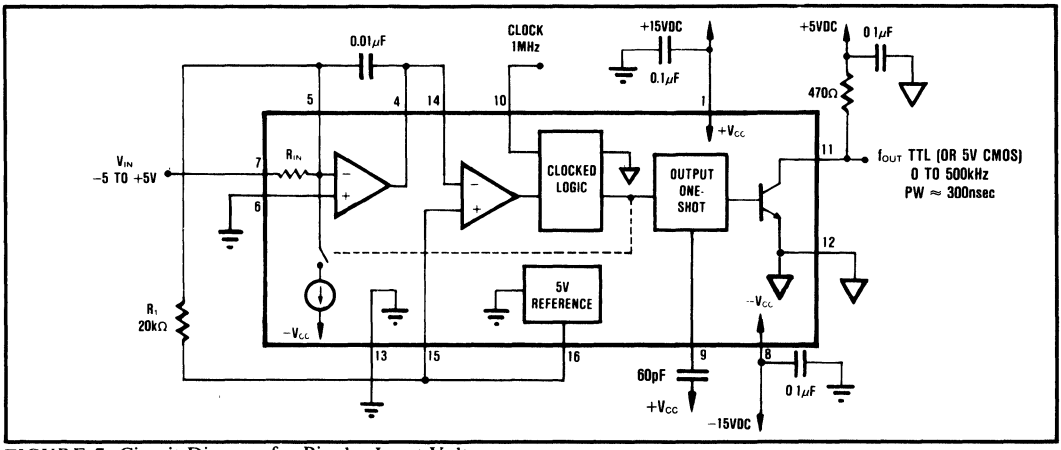


FIGURE 7. Circuit Diagram for Bipolar Input Voltages.

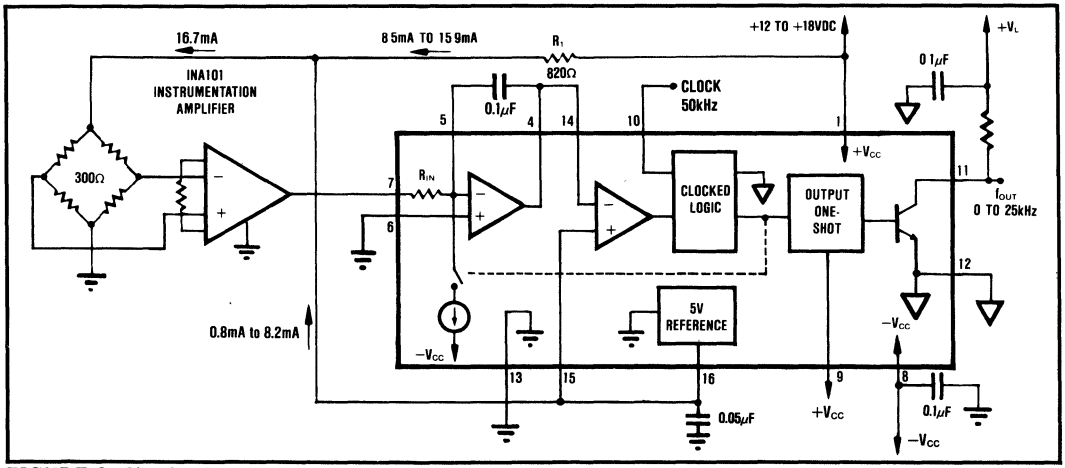


FIGURE 8. Circuit Diagram for Bridge Excitation Using V_{REF}.

output to analog ground (pin 13) may improve the rejection of digital noise from external circuitry.

OTHER INPUT VOLTAGE RANGES

The internal input resistor, $R_{IN} = 20k\Omega$, sets a full-scale input of 10V. Other input ranges can be created by using an external gain set resistor connected to pin 5. Since the excellent temperature drifts of the VFC100 are achieved by careful matching of internal temperature coefficients, use of an external gain set resistor will generally degrade this drift. Using an external resistor to set the gain, the resulting gain drift would be equal to the sum of the external resistor drift and the specified current gain drift of the VFC100. Different voltage input ranges are best implemented by using the internal input resistor, R_{IN}, in series or parallel with a high quality external resistor, thus maintaining as much of the precision temperature tracking as possible.

For best drift performance, the adjustment range of a fine gain trim should be made as narrow as practical. R_1 and R_2 in Figure 9 allow gain adjustment over a ±1% range (adequate to trim the 100kHz FS gain error to zero) and will not significantly affect the drift performance of the VFC100. R_3,R_4,and R_5 allow trimming of the integrator amplifier input offset voltage. The adjustment range is determined by the ratio of R_4 to R_5. Accurate end-point calibration would be performed by first adjusting the offset trim so that zero volts input just causes all output pulses to cease. The gain trim is then adjusted for the proper full-scale output frequency with an accurate full-scale output frequency with an accurate full scale input voltage.

by using the internal input resistor and a clock frequency of 10 times the desired full-scale output frequency.

LINEARITY PERFORMANCE

The linearity of the VFC100 is specified as the worst-case deviation from a straight line defined by low scale and high scale endpoint measurements. This worst-case deviation is expressed as a percentage of the 10V full-scale input. All units are tested and guaranteed for the specified level of performance.

Linearity performance and gain error change with full-scale operating fequency as shown in Figure 10. Figure 11 shows the typical shape of the nonlinearity at 100kHz full scale. Integrator voltage swing (determined by C_{INT}) has a minor effect on linearity. Small integrator voltage swing typically leads to best linearity performance.

Best linearity performance at high full-scale frequencies (above 500kHz) is obtained by using short output pulses

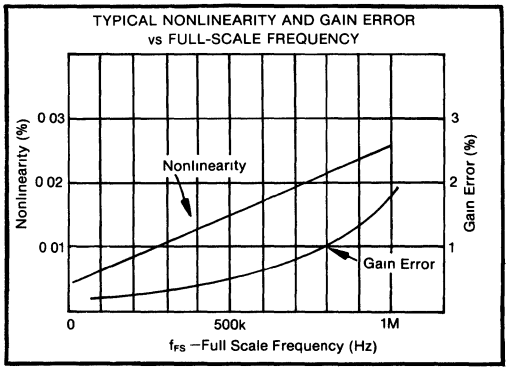


FIGURE 10. Nonlinearity and Gain Error vs Full Scale Frequency.

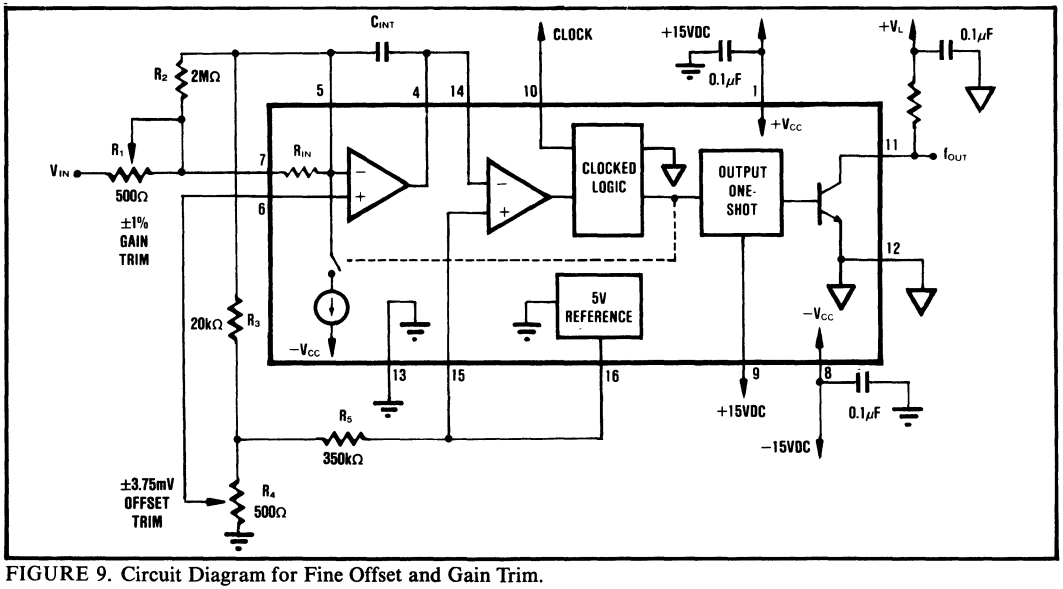


FIGURE 9. Circuit Diagram for Fine Offset and Gain Trim.

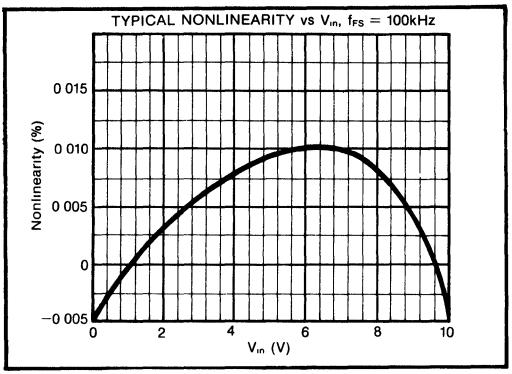


FIGURE 11. Typical Nonlinearity vs V_{IN}.

with a one-shot capacitor of 60pF. As with any high-frequency circuit, careful attention to good power supply bypassing techniques (see "Power Supplies and Grounding") is also required.

TEMPERATURE DRIFT

Conventional VFC circuits are affected significantly by external component temperature drift. Drift of the external input resistor and timing capacitor required with these devices may easily exceed the specified drift of the VFC itself.

When used with its internal input resistor, the gain drift of the complete VFC100 circuit is totally determined by the performance of the VFC100. Gain drift is specified at a full scale output frequency of 100kHz. Conventional VFC circuits usually specify drift at 10kHz and degrade significantly at higher operating frequency. The VFC-100's gain drift remains excellent at higher operating frequency, typically remaining within specification at f_{FS} = 1MHz.

Drift of the external clock frequency directly affects the output frequency, but by using a common clock for the VFC and counting circuitry this drift can be cancelled (see Counting the Output).

POWER SUPPLIES AND GROUNDING

Separate analog and digital grounds are provided on the VFC100 and it is important to separate these grounds to attain greatest accuracy. Logic sink current flowing in the f_{OUT} pin is returned to the digital ground. If this "noisy" current were allowed to flow in analog ground, errors could be created. Although analog and digital grounds may eventually be connected together at a common point in the circuitry, separate circuit connections to this common point can reduce the error voltages created by varying currents flowing through the ground return impedance. The +5V V_{REF} pin is referenced to analog ground.

The power supplies should be well bypassed using capacitors with low impedance at high frequency. A value of 0.1μF is adequate for most circuit layouts.

The VFC100 is specified for a nominal supply voltage of ±15V. Supply voltages ranging from ±7.5V to ±18V may be used. Either supply can be up to 28V as long as the total of both does not exceed 36V. Steps must be taken, however, to assure that the integrator output does not exceed its linear range. Although the integrator output is capable of 12V output swing with 15V power supplies, with 7.5V supplies, output swing will be limited to approximately 4.5V. In this case, the comparator input

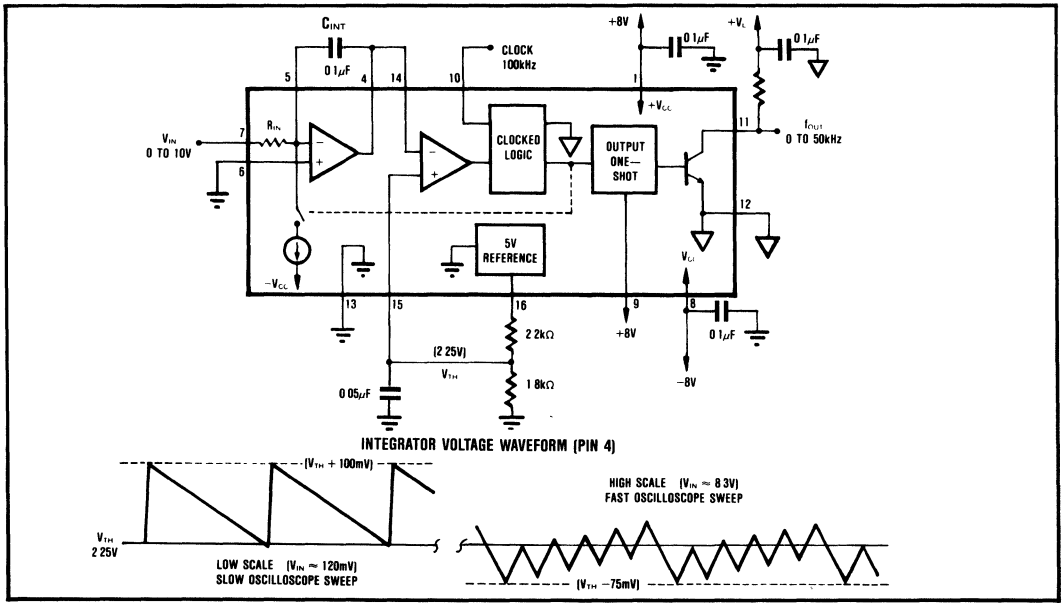


FIGURE 12. Circuit Diagram and Integrator Voltage Waveform for Low Power Supply Voltage Operation.

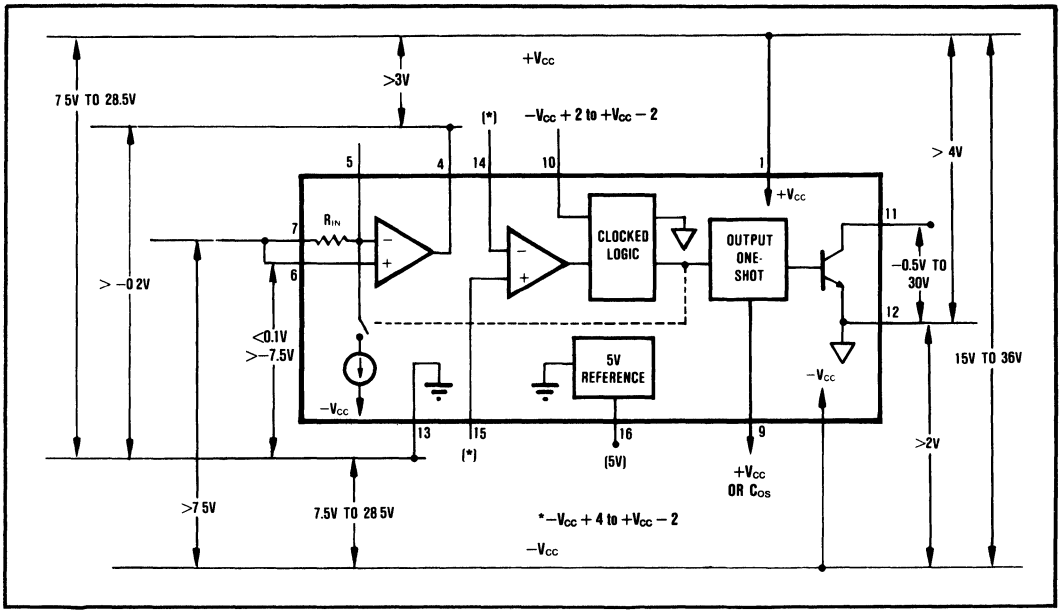


FIGURE 13. Relationships of Allowable Voltages.

cannot be offset by directly connecting to the 5V reference output pin. The comparator input must be connected to a lower voltage point (approximately 2V). This allows the integrator output to operate around a lower voltage point, assuring linear operation. This threshold voltage does not affect the accuracy or drift of the VFC as long as it is not noisy. It should not be made too small, however, or the negative output limitation of the integrator (−0.2V) may cause saturation. Additionally, a large integrator capacitor may be used to limit the required integrator waveform swing to approximately 100mV (see Integrator Capacitor).

Figure 12 shows a circuit for operating from the minimum power supplies, avoiding saturation of the integrator amplifier and loss of accuracy. C_{INT} is chosen for a +100mV to −75mV integrator voltage swing (referred to the noninverting comparator input). The offset voltage applied to the comparator's noninverting input is derived from a resistive voltage divider from V_{REF}.

The relationships of the allowable operating voltage ranges on important pins is shown in Figure 13. Note that the integrator amplifier output cannot swing more than 0.2V below ground. Although this is not "normal" for an operational amplifier, a special internal design of this type optimizes high frequency performance. It is this charactersitic which necessitates the offsetting of the noninverting comparator input in voltage-to-frequency mode to avoid negative output swing.

COUNTING THE OUTPUT

In evaluation and use of the VFC100, you may want to measure the output frequency with a frequency counter. Since synchronization of the VFC100 causes it to await a clock edge for any given output pulse, the output frequency is essentially quantized. The quantized steps are equal to one clock period of the counting gate period. The quantizing error can be made arbitrarily small by counting with long gate times. For instance, a one second counter gate period and a 100kHz full-scale frequency has a one part in 100,000 resolution. Many of the more sophisticated laboratory frequency counters, however, use period measurement schemes to count the input frequency quickly. These instruments work equally well, but the gate period must be set appropriately to achieve the desired count resolution. Short gate periods will produce many digits of "accuracy" in the display, but the results may be very inaccurate.

Figure 14 is a typical system application showing a basic counting technique. A 0 to 10V input is converted to a 0 to 100kHz frequency output. The VFC's clock is divided by M = 4000 to produce a gate period for the counter circuit. The resulting VFC count, N, is insensitive to variations in the actual clock frequency. The input voltage represented by the resulting count is

$$V_{IN} = (N/M)\ 20V$$

Resolution is related to the number of counts at full scale, or one-half the number of clock pulses in the gate period.

The integrating nature of the VFC is important in achieving accurate conversions. The integrating period is equal to the counting period. This can be used to great advantage to reject unwanted signals of a known frequency. Figure 15 shows that response nulls occur at the inverse of the integration period and its multiples. If 60Hz is to be rejected, for instance, the counting period

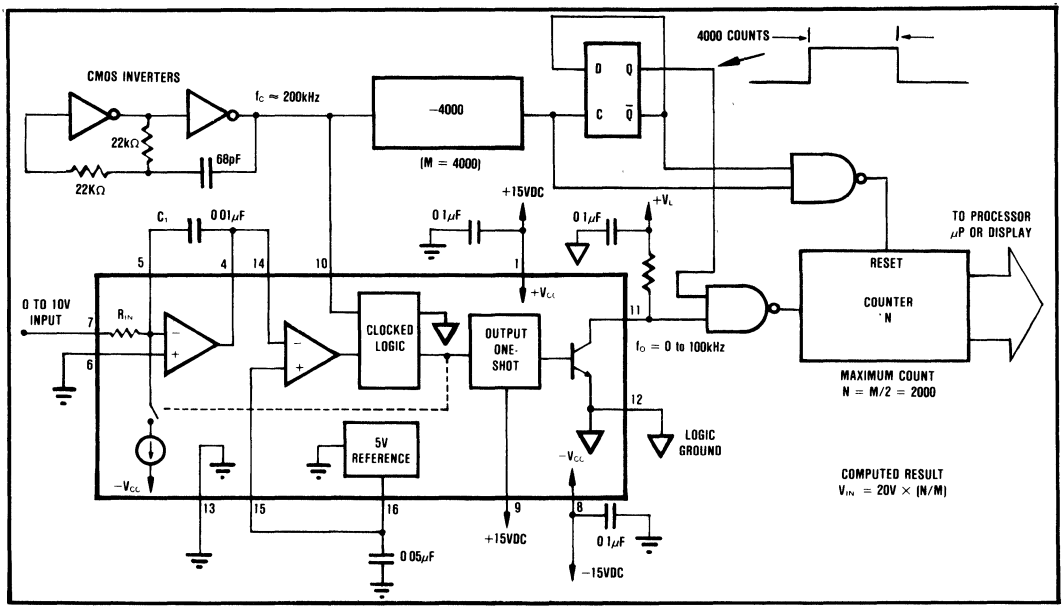


FIGURE 14. Diagram of a Voltage-to-Frequency Converter and Counter System.

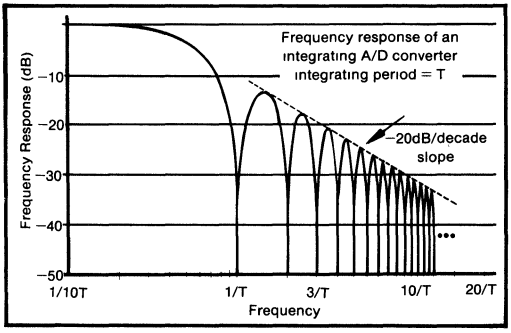


FIGURE 15. Frequency Response of an Integrating Analog-to-Digital Converter.

should be made equal to, or a multiple of 1/60 of a second.

FREQUENCY-TO-VOLTAGE MODE

The VFC100 can also function as a frequency-to-voltage converter by applying an input frequency to the comparator input as shown in Figure 16. The input resistor, R_{IN}, is connected as a feedback resistor. The voltage at the integrator amp output is proportional to the ratio of the input frequency to the clock frequency. The transfer function is

$$V_{OUT} = (f_{IN}/f_{CLOCK})\ 20V$$

This transfer function is complementary to the voltage-to-frequency mode transfer function, making voltage-to-frequency-to-voltage conversions simple and accurate.

Direct coupling of the input frequency to the comparator is easily accomplished by driving both comparators with complementary frequency input signals. Alternatively, one of the comparator inputs can be biased at half the logic voltage (using V_{REF} and a voltage divider) and the other input driven directly.

The proper timing of the input frequency waveform is shown in Figure 16. The input pulse should go low for one clock cycle, centered around a falling edge of the clock. The minimum acceptable input pulse width must fall no later than 200nsec before a negative clock edge and rise no sooner than 200nsec after the falling clock edge. An input pulse which remains low for more than one falling edge of the clock will produce incorrect output voltages. Positive (active high) input pulses can be accepted by reversing the connections to pins 14 and 15. Figure 17 shows a digital conditioning circuit which will accept any input duty cycle and provide the proper pulse width to the comparator. Each rising edge at this circuit's input generates the required negative pulse at the inverting comparator input. The noninverting comparator is driven by a complementary signal.

The integrator amplifier output is designed to drive up to 10,000pF and 5kΩ loads in frequency-to-voltage mode. This allows driving long lines in a large system.

Ripple voltage in the voltage output is unavoidable and is inversely proportional to the value of the integrator capacitor. Figure 18 shows the output ripple and settling time as a function of the C_{INT} value.

The ripple frequency is equal to the input frequency. Its magnitude can be reduced by using a large integrator capacitor value, but at the sacrifice of slow settling time at the voltage output in response to an input frequency change. The settling time constant is equal to $R_{IN} \times C_{INT}$. A better compromise between output ripple and settling time can be achieved by using a moderately low integra-

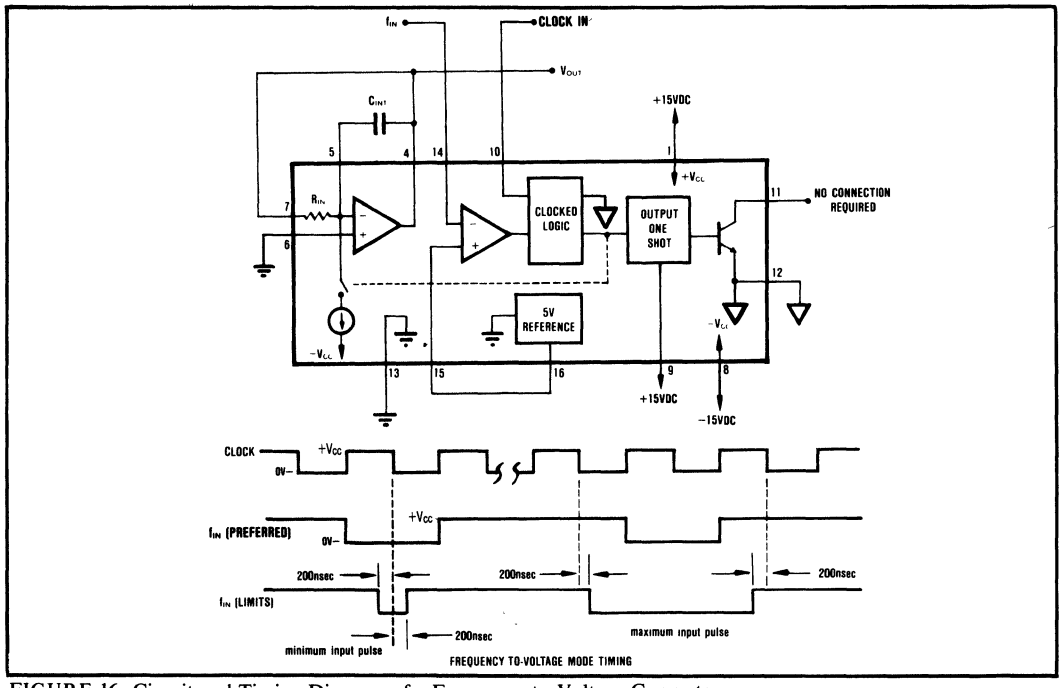


FIGURE 16. Circuit and Timing Diagram of a Frequency-to-Voltage Converter.

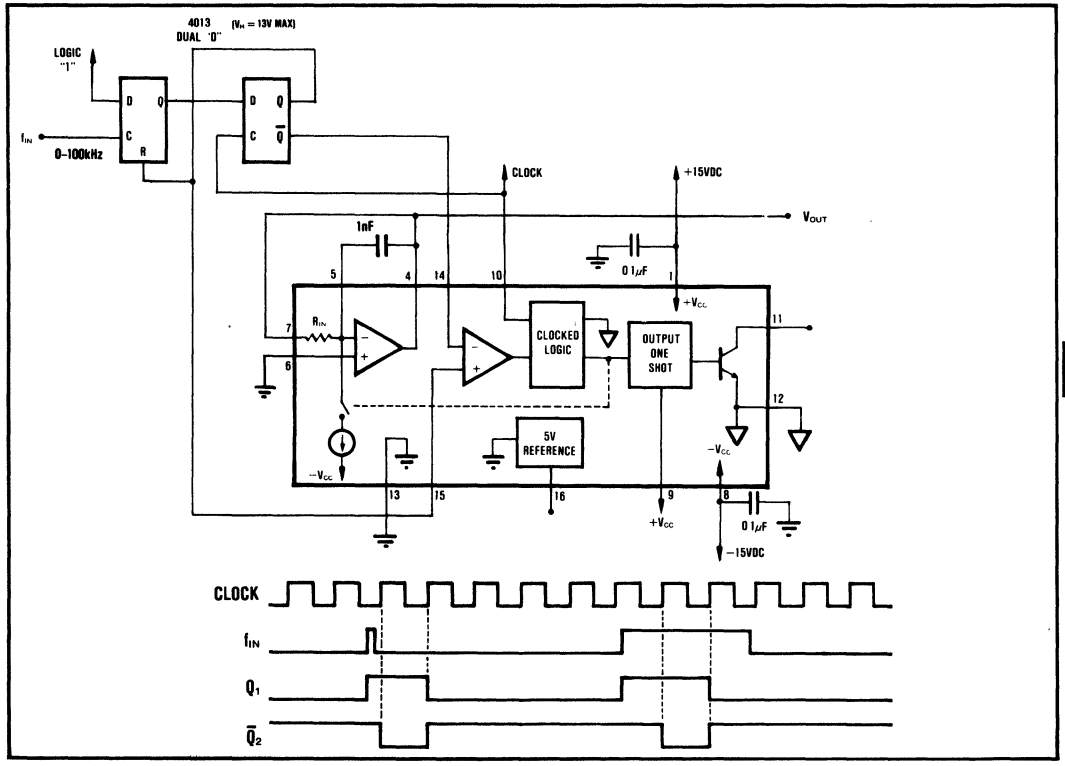


FIGURE 17. Digital Timing Input Conditioning Circuit for Frequency-to-Voltage Operation.

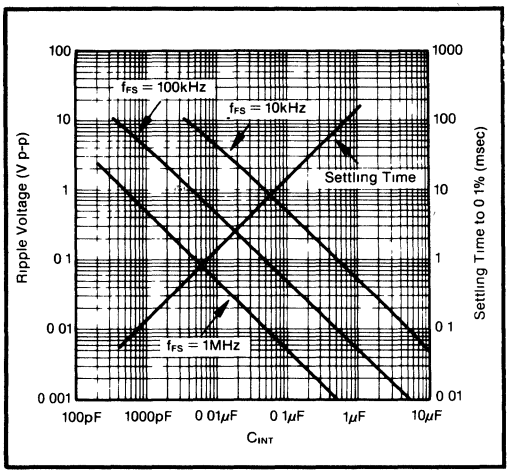


FIGURE 18. Frequency-to-Voltage Mode Output Ripple and Settling Time vs Integrator Capacitance.

tor capacitor value and adding a low-pass filter on the analog output. The cutoff frequency of the filter should be made below the lowest expected input frequency to the frequency-to-voltage converter.

The system in Figure 20 makes use of both voltage-to-frequency and frequency-to-voltage mode to send a signal across an optically-isolated barrier. This technique is useful not only for providing safety in the presence of high voltages, but for creating high noise rejection in electrically noisy environments. The use of a common clock frequency causes the two devices to have complementary transfer functions, which minimizes errors.

Optical coupling is facilitated by use of the output one-shot feature. The output pulse is shortened (see Shortened Output Pulses) to allow for the relatively slow turn-off time of the LED. The timing diagram in Figure 19 shows how the accumulated delay of both optical couplers could produce too long an input pulse for the frequency-to-voltage converter, VFC_2 of Figure 20.

An output filter is used to reduce the ripple in the output of VFC_2. In order to most effectively filter the output, both input and output VFCs are offset. By connecting R_1 to V_{REF}, an accurate offset is created in the voltage-to-frequency function. Zero volts input now creates a 10kHz output. This offset is subtracted in the frequency-to-voltage conversion on the output side, by V_{REF} and R_5.

MORE PULSE POSITION RESOLUTION

Since output pulses must always align with clock edges, the instantaneous output frequency is quantized and

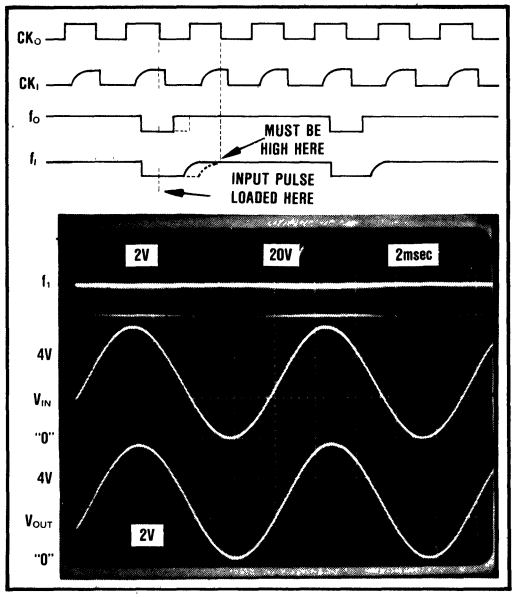


FIGURE 19. Timing Diagram and Oscilloscope Photo of Isolated Voltage-to-Frequency/ Frequency-to-Voltage System.

appears to have phase jitter. This effect can be greatly reduced by using a high speed clock so that available clock edges come more frequently. This would also create a high full-scale frequency, but the technique shown in Figure 21 offers an alternative. A high speed clock is used to produce high resolution of the output pulse position, but a low full-scale frequency can be programmed.

When an output pulse is generated, the next rising edge of the high frequency clock is delayed for a programmable number of clock counts. Since the integrator reset period (which sets the full-scale range) is determined by the time from rising edge to rising edge at the VFC's clock input once the comparator is tripped, the effective clock frequency is $f_{CLOCK}/16$. The circuit shown can be programmed for any N from 2 to 16. Since an output pulse must propagate through the VFC before the next rising edge of the clock arrives, maximum clock frequency is limited by the delay time shown in the timing diagram.

With output pulses now able to align with greater resolution, the output has lower phase jitter. Using this technique, the output is suitable for ratiometric (period measurement) type counting. This counting technique achieves the maximum possible resolution for short gate periods (see Burr-Brown Application Note AN-130).

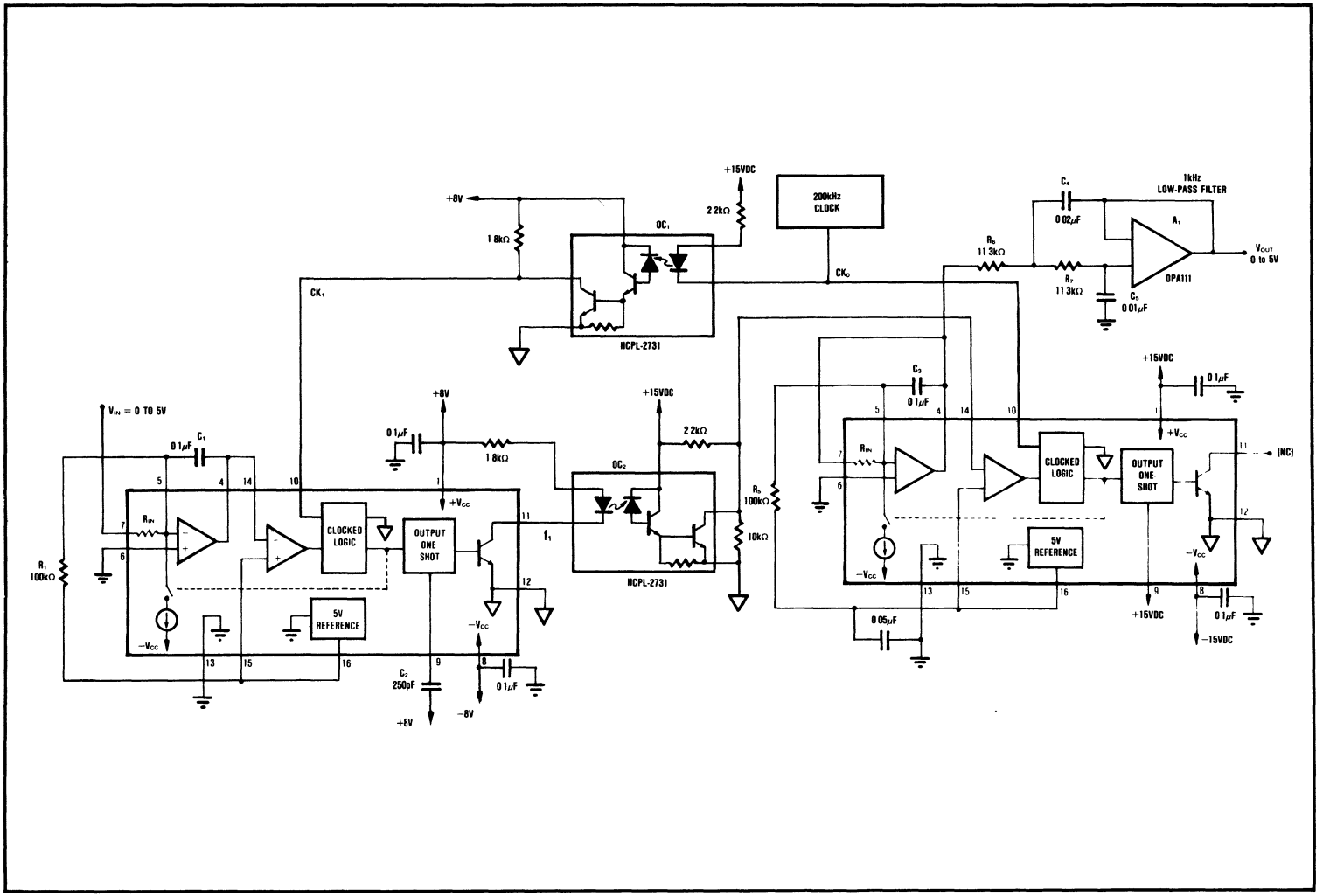


FIGURE 20. Circuit Diagram of Isolated Voltage-to-Frequency/Frequency-to-Voltage System.

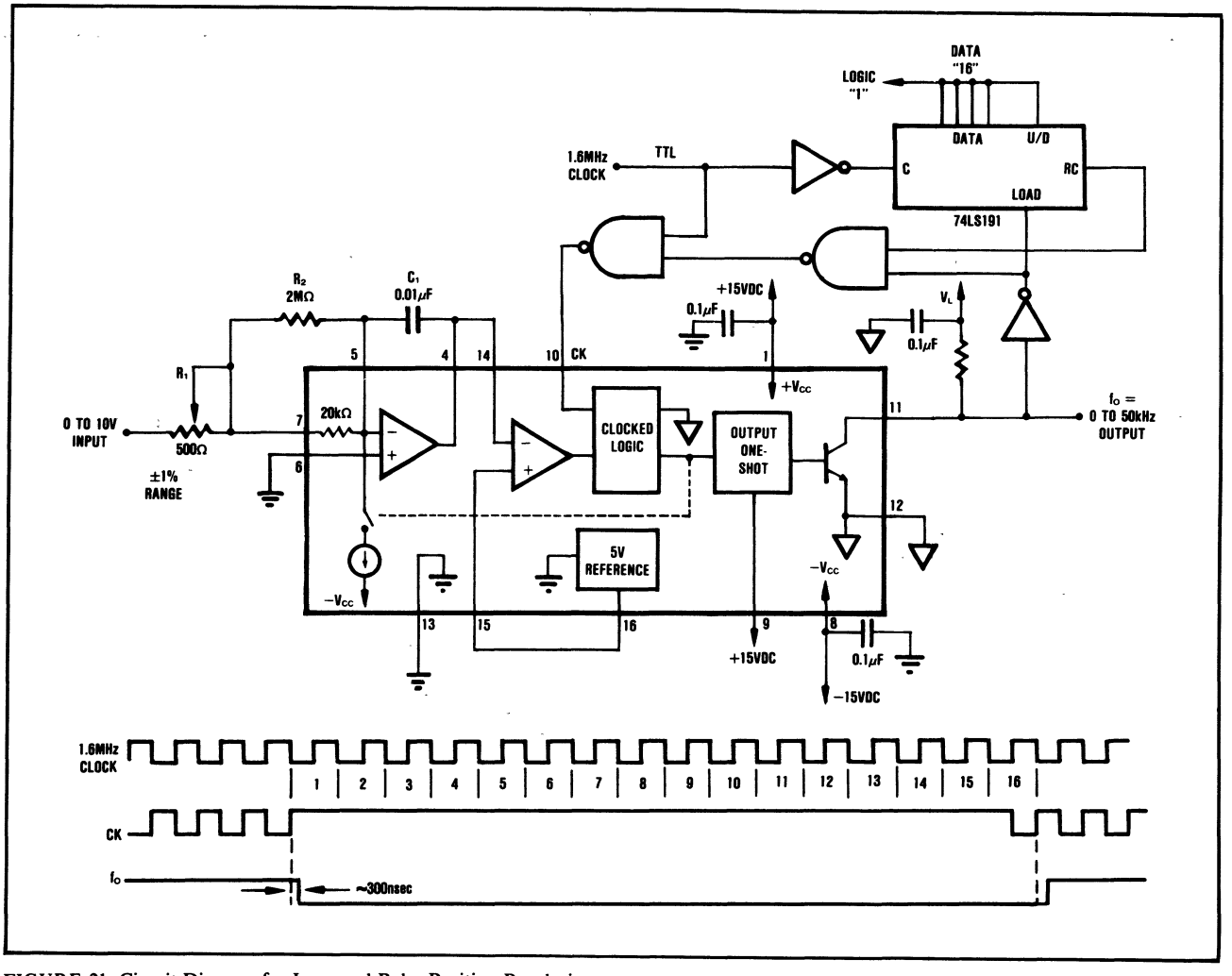


FIGURE 21. Circuit Diagram for Increased Pulse Position Resolution.

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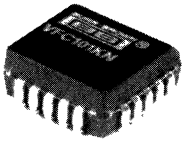


VFC101

AVAILABLE IN DIE FORM

Synchronized VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- FULL-SCALE FREQUENCY SET BY SYSTEM CLOCK
- MULTIPLE INPUT RANGES: 5V, 8V, 10V FULL SCALE
- ACCURATE 5V REFERENCE VOLTAGE
- LOW NONLINEARITY: 0.02% AT 100kHz FS
- LOW GAIN DRIFT: 40ppm/°C

APPLICATIONS

- INTEGRATING A/D CONVERTER
- MULTICHANNEL DATA ACQUISITION
- FREQUENCY-TO-VOLTAGE CONVERSION
- VOLTAGE ISOLATION

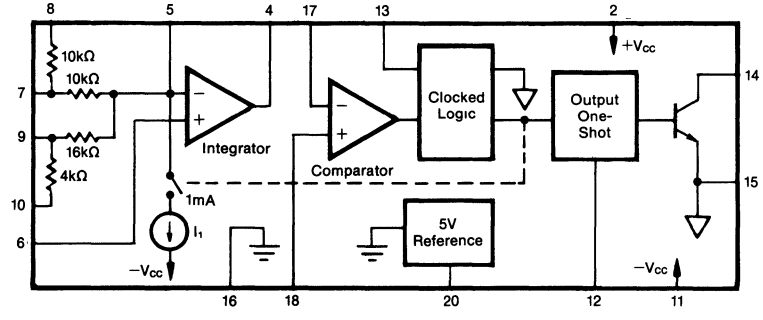
DESCRIPTION

The VFC101 voltage-to-frequency converter provides features and performance unique in integrated circuit VFCs. It uses the proven charge-balance technique with internal digital logic to control the critical reference integration period. Reference timing is derived from an external clock signal which accurately sets the full-scale frequency. This technique eliminates the errors and drift from external timing components which are required with other VFCs. Internal resistors provide accurate full-scale input ranges of 5V, 8V or 10V inputs without external resistors or trimming.

An accurate 5V reference voltage output is useful for bridge or sensor excitation. With simple pin interconnections, it can provide half-scale offset to allow bipolar input voltages.

The open-collector frequency output interfaces easily to CMOS or TTL circuitry. Output one-shot circuitry may be used to optimize the output pulse width for optical couplers or transformers.

The VFC101 is packaged in a surface-mount 20-pin PLCC (plastic leaded chip carrier) package.



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PDS-779A

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC supplies unless otherwise noted.

PARAMETER	CONDITIONS	VFC101JN MIN	VFC101JN TYP	VFC101JN MAX	VFC101KN MIN	VFC101KN TYP	VFC101KN MAX	UNITS
TRANSFER FUNCTION								
Voltage-to-Frequency Mode	$f_{OUT} = f_{CLOCK}$ ($V_{IN}/2V_{FS}$)							
Gain Error[1]	FSR = 100kHz		±0 3	±0 5		*	*	% of FSR
Linearity Error	FSR = 100kHz, over temp		±0.01	±0.025		*	±0.02	% of FSR
	FSR = 500kHz, C_{OS} = 60pF		±0.02	±0.05		*	*	% of FSR
	FSR = 1MHz, C_{OS} = 60pF		±0.05	±0.1		*	*	% of FSR
Gain Drift[2]	FSR = 100kHz		±50	±80		±30	±40	ppm of FSR/°C
Referred to Internal V_{REF}			10	±25		*	±15	
Offset Referred to Input			±1	±3		*	±2	mV
Offset Drift			±12	±100		±6.5	±25	µV/°C
Power Supply Rejection	Full supply range			0.02			0.015	%/V
Response Time	To Step Input Change		One period of new output frequency plus one clock period					
Frequency-to-Voltage Mode	$V_{OUT} = 2V_{FS}\ f_{IN}/f_{CLOCK}$							
Gain Accuracy[1]	FSR = 100kHz		±0 3	±0 5		*	*	%
Linearity	FSR = 100kHz		±0 01	±0 025		*	±0.02	%
Input Resistors								
Resistance			±30			*		%
Temperature Coefficient (T_C)[2]			±50	±100		*	*	ppm/°C
INTEGRATOR OP AMP								
V_{OS}[1]			±150	±1000		*	*	µV
V_{OS} Drift			±5	±25		*	±15	µV/°C
I_B			±50	±100		±25	±50	nA
I_{OS}			100	200		50	100	nA
A_{OL}	Z_{LOAD} = 5kΩ/10,000pF	100	120		*	*		dB
CMRR		80	105		*	*		dB
CM Range		−7.5		+0 1	*		*	V
V_{OUT} Range	Z_{LOAD} = 5kΩ/10,000pF	−0.2		+12	*		*	V
Bandwidth			14			*		MHz
COMPARATOR INPUTS								
Input Bias Current (I_B)	$-V_{CC} + 4V < V_{IN} < +V_{CC}$			5			*	µA
CLOCK INPUT (referenced to digital common)								
Frequency (maximum operating)			4.0			*		MHz
Threshold Voltage			1 4			*		V
	Over temperature	0.8		2.0	*		*	V
Voltage Range		$-V_{CC} + 3$		$+V_{CC}$	*		*	V
Input Current			0.5	5		*	*	µA
Rise Time				2			*	µs
OPEN COLLECTOR OUTPUT (referenced to digital common)								
V_{OL}	I_{OUT} = 10mA			0.4			*	V
I_{OL}				15			*	mA
I_{OH} (off leakage)	V_{OH} = 30V		0.01	10		*	*	µA
Delay Time, positive clock edge to output pulse			300			*		ns
Fall Time			100			*		ns
Output Capacitance			5			*		pF
OUTPUT ONE-SHOT								
Pulse Width Out	Nominal PW_{OUT} = (5ns/pF) × C_{OS} − 90ns, C_{OS} = 300pF	1	1.4	2	*	*	*	µs
REFERENCE VOLTAGE								
Accuracy	No load	4.90	5.0	5.10	4 95	*	5.05	V
Drift[2]			±60	±105		±40	±55	ppm/°C
Current Output (sourcing)		10			*			mA
Power Supply Rejection				0.015			*	%/V
Output Impedance			0 5	2		*	*	Ω

ELECTRICAL (CONT)

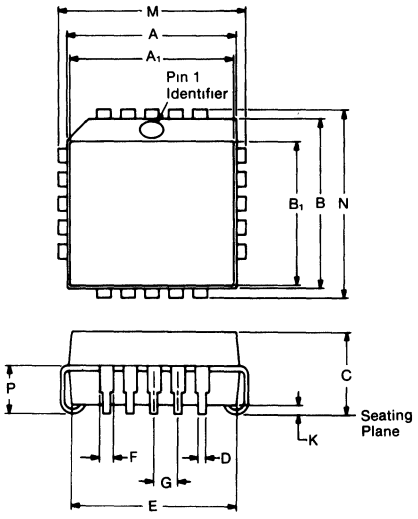
At T_A = +25°C and ±15VDC supplies unless otherwise noted

PARAMETER	CONDITIONS	VFC101JN MIN	VFC101JN TYP	VFC101JN MAX	VFC101KN MIN	VFC101KN TYP	VFC101KN MAX	UNITS
POWER SUPPLY								
Rated Voltage			±15			*		V
Operating Voltage Range	$+V_{CC}$	+7.5		+28.5	*		*	V
	$-V_{CC}$	−7.5		−28 5	*		*	V
Total Supply	$+V_{CC} - (-V_{CC})$	15		36	*		*	V
Digital Common		$-V_{CC} + 2$		$+V_{CC} - 4$	*		*	V
Quiescent Current $+I_{CC}$	Over temperature		10 6	15		*	*	mA
$-I_{CC}$			9 6	15		*	*	mA
TEMPERATURE RANGE								
Specification		0		+70	*		*	°C
Storage		−65		+150	*		*	°C
θ Junction-Ambient			90			*		°C/W
θ Junction-Case			35			*		°C/W

*Specification same as JN grade

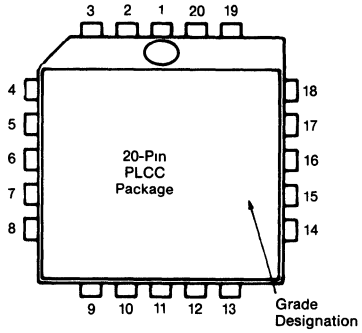
NOTES (1) Offset and gain error can be trimmed to zero (2) Specified by the box method: (Max − Min) ÷ (Avg × ΔT)

MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	350	356	8 89	9 04
A_1	338	344	8 59	8 74
B	350	356	8 89	9 04
B_1	290	330	7 37	8 38
C	165	180	4 19	4 57
D	013	021	0 33	0 53
E	290	330	7 37	8 38
F	026	032	0 66	0 81
G	050 BASIC		1 27 BASIC	
K	020	—	0 51	—
M	385	395	9 78	10 03
N	385	395	9 78	10 03
P	090	120	2 29	3 05

PIN CONFIGURATION



1	NC
2	$+V_{CC}$ Power Supply
3	NC
4	V_{OUT} Integrator Amp Output
5	C_{INT}, Integrator Inverting Input
6	$+V_{IN}$, Integrator Noninverting Input
7	V_{IN}, 5V FS
8	V_{IN}, 10V FS
9	V_{IN}, 8V FS
10	V_{IN}, 10V FS
11	$-V_{CC}$ Power Supply
12	C_{OS}, Output One-Shot Capacitor
13	f_{CLOCK} Input
14	f_{OUT} Frequency Output
15	Digital Ground
16	Analog Ground
17	− Comparator Input
18	+ Comparator Input
19	NC
20	V_{REF} +5V Reference Output

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($+V_{CC}$ to $-V_{CC}$)	36V
$+V_{CC}$ to Analog Common	28V
$-V_{CC}$ to Analog Common	28V
Integrator Out Short-Circuit-to-Ground	Indefinite
Integrator Differential Input	±10V
Integrator Common-Mode Input	$-V_{CC}$ +5V to +2V
V_{IN} (pins 7, 8, 9, 10)	$\pm V_{CC}$
Clock Input	$\pm V_{CC}$
V_{REF} Out Short-Circuit-to-Ground	Indefinite
C_{OS} (pin 12)	0 to $+V_{CC}$
f_{OUT} (referred to digital common)	−0.5V to 36V
Digital Common	$\pm V_{CC}$
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering 10s)	300°C

ORDERING INFORMATION

VFC101 ( ) N

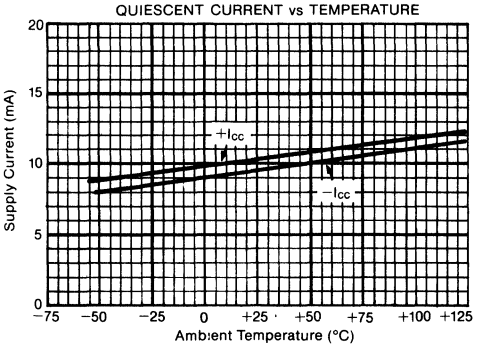
Basic Model Number

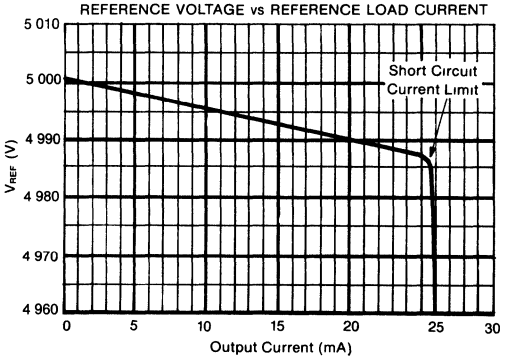
Performance Code
J, K: 0°C to +70°C
(no grade designation indicates J grade)

Plastic Leaded Chip Carrier Package
(no package designation indicates N package)

TYPICAL PERFORMANCE CURVES

At +25°C, $\pm V_{CC}$ = 15VDC, and in circuit of Figure 1 unless otherwise specified





THEORY OF OPERATION

The VFC101 monolithic voltage-to-frequency converter provides a digital pulse train output with an average frequency proportional to the analog input voltage. The output is an active low pulse of constant duration, with a repetition rate determined by the input voltage. Falling edges of the output pulses are synchronized with rising edges of the clock input.

Operation is similar to a conventional charge-balance VFC. An input operational amplifier (Figure 1) is configured as an integrator so that a positive input voltage causes an input current to flow in C_{INT}. This forces the integrator output to ramp negatively. When the output of the integrator crosses the reference voltage (5V), the comparator trips, activating the clocked logic circuit. Once activated, the clocked logic awaits a falling edge of the clock input, followed by a rising edge (see Figure 2). On the rising edge, switch SW_1 is closed for one complete clock cycle, causing the reset current, I_1, to switch to the integrator input. Since I_1 is larger than the input current, I_{IN}, the output of the integrator ramps positively during the one clock cycle reset period. The clocked logic circuitry also generates a VFC output pulse during the reset period.

Unlike conventional VFC circuits, the VFC101 accurately derives its reset period from an external clock frequency. This eliminates the critical timing capacitor required by other VFC circuits. One period (from rising edge to rising edge) of the clock input determines the integrator reset period.

When the negative-going integration of the input signal crosses the comparator threshold, integration of the input signal will continue until the reset period can start (awaiting the necessary transitions of the clock). Output pulses are thus made to align with rising edges of the external clock. This causes the instantaneous output frequency to be a subharmonic of the clock frequency. The average frequency, however, will be an accurate analog of the input voltage.

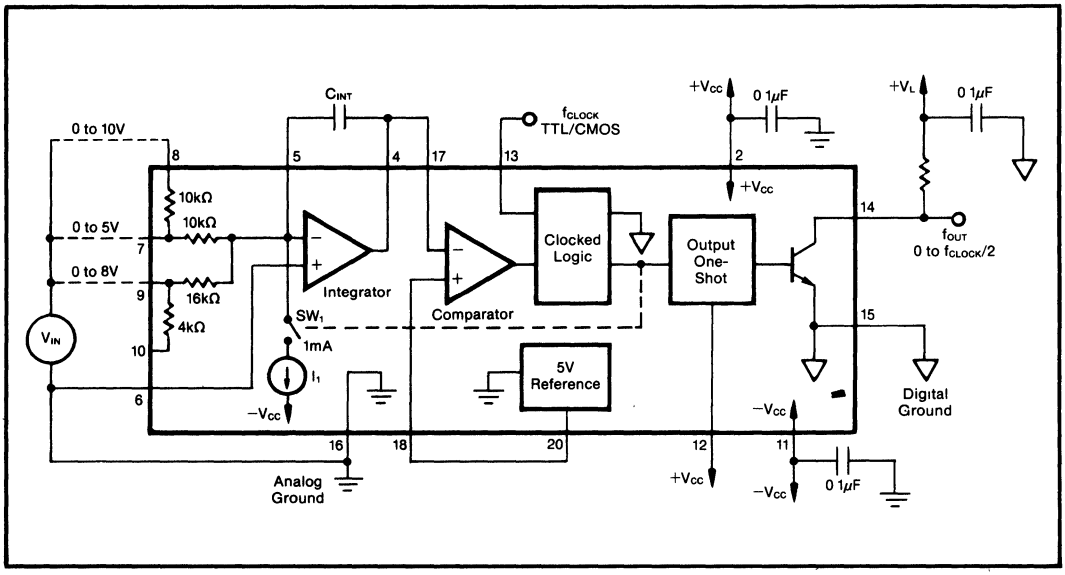


FIGURE 1. Basic Voltage-to-Frequency Operations.

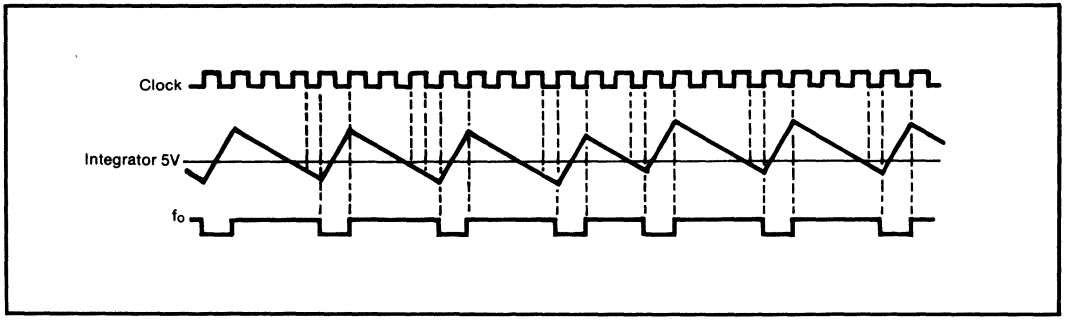


FIGURE 2. Timing Diagram for Voltage-to-Frequency Mode.

A full-scale input causes a nominal output frequency equal to one-half the clock frequency. The transfer function is $f_{OUT} = (V_{IN}/2V_{FS})\ f_{CLOCK}$.

Input voltages greater than V_{FS} cause the output frequency to limit at half the clock frequency. Negative inputs cause all output pulses to cease. The full-scale input voltage, V_{FS}, is determined by the input pin used:

Pin #	V_{FS}
8	10V
10	10V
9	8V
7	5V
7*	2 5V

*Pin 8 connected to pin 5

One of the useful functions made possible by the VFC101's multiple input resistors is shown in Figure 3. By connecting one 10V input to the 5V V_{REF} output, the other 10V input pin functions as a bipolar input. A −5V to +5V input range causes a zero to $f_{CLOCK}/2$ output frequency range. Accurate ratio matching and temperature tracking of the input resistors provides improved stability of the half-scale offset.

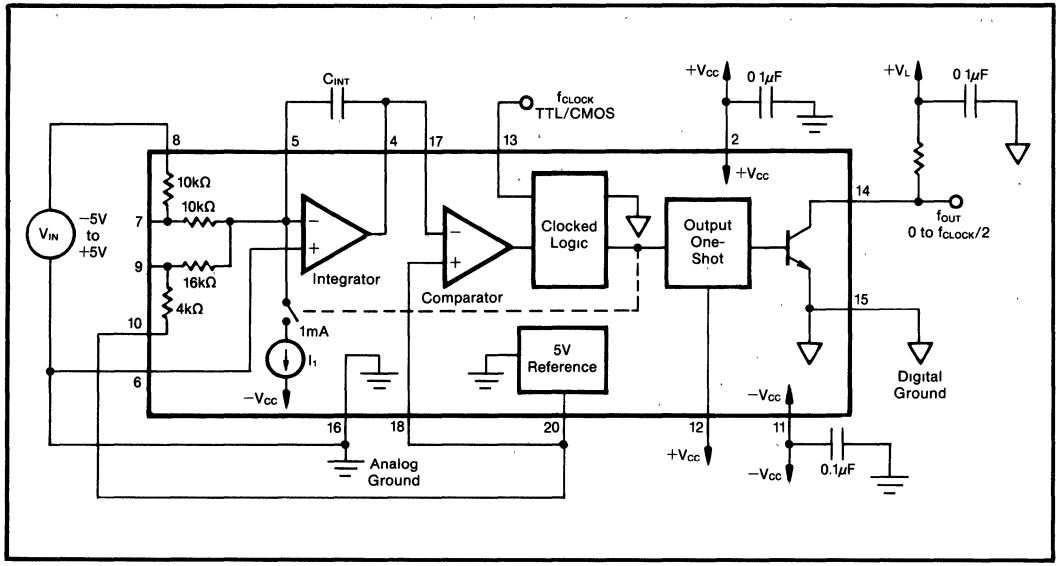


FIGURE 3. Offset for Bipolar Input Voltages.

INSTALLATION AND OPERATING INSTRUCTIONS

The integrator capacitor C_{INT} (see Figure 1) affects the magnitude of the integrator voltage waveform. Its absolute accuracy is not critical since it does not affect the transfer function. This allows a wide range of capacitance to produce excellent results. Figure 4 facilitates choosing an appropriate standard value to assure that the integrator waveform voltage is within acceptable limits. Good dielectric absorption properties are required to achieve best linearity. Mylar™, polycarbonate, mica, polystyrene, Teflon™ and glass types are appropriate choices. The choice in a given application will depend on the particular value and size considerations. Ceramic capacitors vary considerably from type to type and some produce significant nonlinearities. Polarized capacitors should not be used.

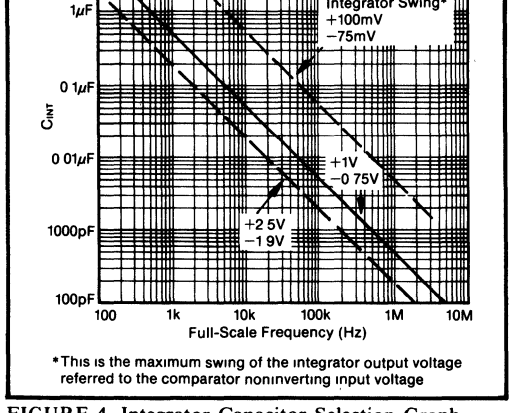


FIGURE 4. Integrator Capacitor Selection Graph.

Deviation from the nominal recommended +1V to −0.75V integrator voltage (as controlled by the integrator capacitor value) is permissible and will have a negligible effect on VFC operation. Certain situations may make deviations from the suggested integrator swing highly desirable. Smaller integrator voltages, for instance, allow more "headroom" for averaging noisy input signals. The VFC is a fully integrating input converter, able to reject large levels of interfering noise. This ability is limited only by the output voltage swing range of the integrator amplifier. By setting a small integrator voltage swing using a large C_{INT} value, larger levels of noise can be integrated without output saturation and loss of accuracy. For instance, with a 50kHz full-scale output and $C_{INT} = 0.1\mu F$, the circuit in Figure 1 can accurately average an input through the full 0 to 10V input range with 1Vp-p superimposed 60Hz noise.

The integrator output voltage should not be allowed to exceed +12V or −0.2V, otherwise saturation of the operational amplifier could cause inaccuracies. Operation with positive power supplies less than +15V will limit the output swing of the integrator operational amplifier. Smaller integrator voltage waveforms may be required to avoid output saturation of the integrator amplifier. See "Power Supplies and Grounding" for information on low-voltage operation.

The maximum integrator voltage swing requirement is nearly symmetrical about the comparator threshold voltage (see Figure 9). One-third greater swing is required

above the threshold than below it. Maximum demand on positive integrator swing occurs at low scale, while the negative swing is greatest just below full scale.

CLOCK INPUT

The clock input is TTL- and CMOS-compatible. Its input threshold is approximately 1.4V (two diode voltage drops) referenced to digital ground (pin 15). The clock "high" input pay be standard TTL or may be as high as $+V_{CC}$. The clock input has a high input impedance, so no special drivers are required. Rise time in the transistion region from 0.5V to 2V must be less than 2μs for proper operation.

OUTPUT

The frequency output is an open collector current-sink transistor. Output pulses are active low such that the output transistor is on only during the reset integration period (see Shortened Output Pulses). This minimizes power dissipation over the full frequency range and provides the fastest logic edge at the beginning of the output pulse where it is most desirable.

Interface to a logic circuit would normally be made using a pull-up resistor to the logic power supply. Selection of the pull-up resistor should be made such that no more than 15mA flows in the output transistor. The actual choice of the pull-up resistor may depend on the full-scale frequency and the stray capacitance on the output line. The rising edge of an output pulse is determined by the RC time constant of the pull-up resistor and the stray capacitance. Excessive capacitance will produce a rounding of the output pulse rising edge, which may create problems driving some logic circuits. If long lines must be driven, a buffer or digital line transmitter circuit should be used.

The synchronized nature of the VFC101 makes viewing its output on an oscilloscope somewhat tricky. Since all output pulses align with the clock, it is best to trigger and view the clock on one of the input channels and the output can then be viewed on another oscilloscope channel. Depending on the VFC input voltage, the output waveform may appear as if the oscilloscope is not properly triggered. The output might best be visualized by imagining a constant output frequency which is locked to a submultiple of the clock frequency with occasional extra pulses or missing pulses to create the necessary average frequency. It is these extra or missing pulses that make the output waveform appear as if the oscilloscope is not properly triggered. This behavior amounts to a frequency or phase jitter in the output, making frequency detection with most phase-locked loop circuitry impractical. For the same reason, fast period measurement (ratiometric counting) will not provide a stable reading. The output frequency must be measured (averaged) for N counts of f_{CLOCK} to achieve a stable N counts of resolution.

SHORTENED OUTPUT PULSES

In normal operation, the negative output pulse duration is equal to one period of the clock input. Shorter output pulses may be useful in driving optical couplers or transformers for voltage isolation or noise rejection. This can be accomplished by connecting capacitor C_{OS} as shown in Figure 5. Pin 12 may be connected to $+V_{CC}$, deactivating the output one-shot circuit. The value of C_{OS} is chosen according to the curve in Figure 6. Output pulses cannot be made to exceed one clock period in duration. Thus, a C_{OS} value which would create an

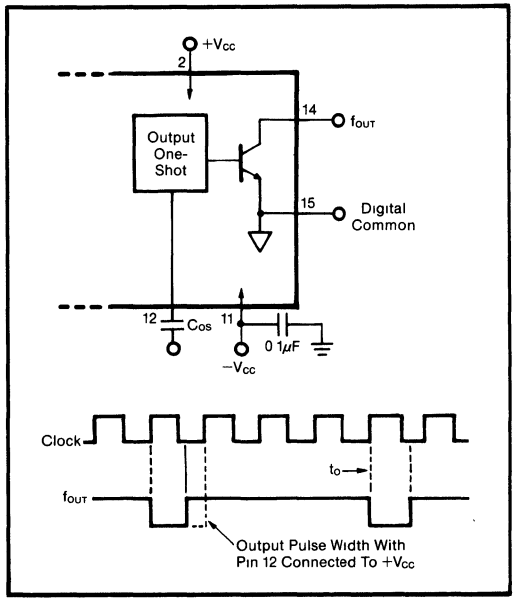


FIGURE 5. Circuit and Timing Diagram for Shortened Output Pulses.

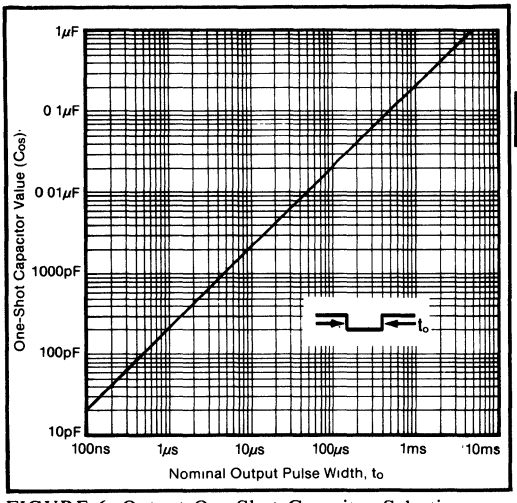


FIGURE 6. Output One-Shot Capacitor Selection Graph.

output pulse which is longer than one period of the clock will have the same effect as disabling the one-shot, causing the output pulse to last one clock period. The minimum practical pulse width of the one-shot circuit is approximately 100ns. Using C_{OS} to generate shorter output pulses does not affect the output frequency or the gain equation.

REFERENCE VOLTAGE

Low gain drift is achieved by use of a precision internal 5V reference. This reference is brought to an external pin and can be used for a variety of purposes. It is used to offset the noninverting comparator input in voltage-to-frequency mode (although a precise voltage is not required for this function). It is very useful in many other applications such as offsetting the input to handle bipolar input signals. It can source up to 10mA and sink 100μA. Heavy loading of the reference will change the gain of the VFC as well as affecting the external reference voltage. For instance, a 10mA load interacting with a 0.5Ω typical output impedance will change the VFC gain equation and reference voltage by 0.1%.

LINEARITY PERFORMANCE

The linearity of the VFC101 is specified as the worst-case deviation from a straight line defined by low scale and high-scale endpoint measurements. This worst-case deviation is expressed as a percentage of the 10V full-scale input. All units are tested and guaranteed for the specified level of performance.

Linearity performance and gain error change with full-scale operating frequency as shown in Figure 7. Figure 8 shows the typical shape of the nonlinearity at 100kHz full scale. Integrator voltage swing (determined by C_{INT}) has a minor effect on linearity. Small integrator voltage swing typically leads to best linearity performance.

Best linearity performance at high full-scale frequencies (above 500kHz) is obtained by using short output pulses with a one-shot capacitor of 60pF. As with any high-frequency circuit, careful attention to good power supply bypassing techniques (see "Power Supplies and Grounding") is also required.

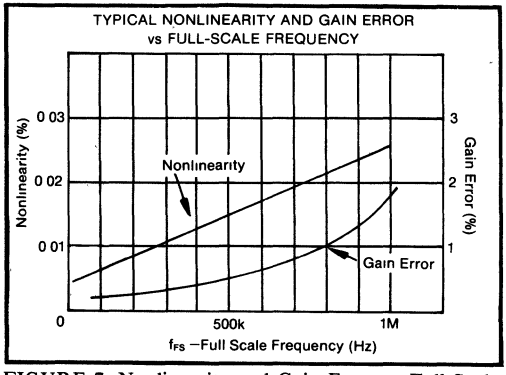


FIGURE 7. Nonlinearity and Gain Error vs Full-Scale Frequency.

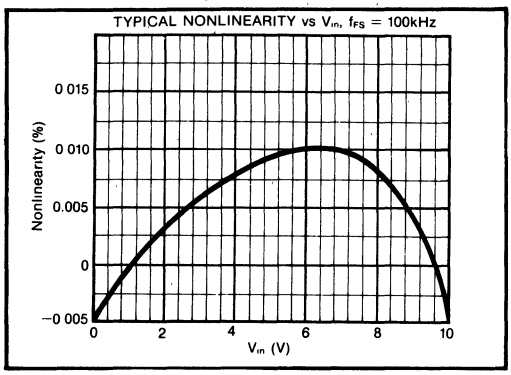


FIGURE 8. Typical Nonlinearity vs V_{IN}.

TEMPERATURE DRIFT

Conventional VFC circuits are affected significantly by external component termperature drift. Drift of the external input resistor and timing capacitor required with these devices may easily exceed the specified drift of the VFC itself.

When used with its internal input resistors, the gain drift of the complete VFC101 circuit is totally determined by the performance of the VFC101. Gain drift is specified at a full-scale output frequency of 100kHz. Conventional VFC circuits usually specify drift at 10kHz and degrade significantly at higher operating frequency. The VFC101's gain drift remains excellent at higher operating frequency, typically remaining within specification at f_{FS} = 1MHz.

Drift of the external clock frequency directly affects the output frequency, but by using a common clock for the VFC and counting circuitry, this drift can be cancelled.

POWER SUPPLIES AND GROUNDING

Separate analog and digital grounds are provided on the VFC101 and it is important to separate these grounds to attain greatest accuracy. Logic sink current flowing in the f_{OUT} pin is returned to the digital ground. If this "noisy" current were allowed to flow in analog ground, errors could be created. Although analog and digital grounds may eventually be connected together at a common point in the circuitry, separate circuit connections to this common point can reduce the error voltages created by varying currents flowing through the ground return impedance. The +5V V_{REF} pin is referenced to analog ground.

The power supplies should be well bypassed using capacitors with low impedance at high frequency. A value of 0.1μF is adequate for most circuit layouts.

The VFC101 is specified for a nominal supply voltage of ±15V. Supply voltages ranging from ±7.5V to ±18V may be used. Either supply can be up to 28V as long as the total of both does not exceed 36V. Steps must be taken, however, to assure that the integrator output does not exceed its linear range. Although the integrator output is capable of 12V output swing with 15V power supplies, with 7.5V supplies, output swing will be limited

to approximately 4.5V. In this case, the comparator input cannot be offset by directly connecting to the 5V reference output pin. The comparator input must be connected to a lower voltage point (approximately 2V). This allows the integrator output to operate around a lower voltage point, assuring linear operation. This threshold voltage does not affect the accuracy or drift of the VFC as long as it is not noisy. It should not be made too small, however, or the negative ouptut limitation of the integrator (−0.2V) may cause saturation. Additionally, a large integrator capacitor may be used to limit the required integrator waveform swing to approxmiately 100mV (see Figure 4).

Figure 9 shows a circuit for operating from the minimum power supplies, avoiding saturation of the integrator amplifier and loss of accuracy. C_{INT} is chosen for a

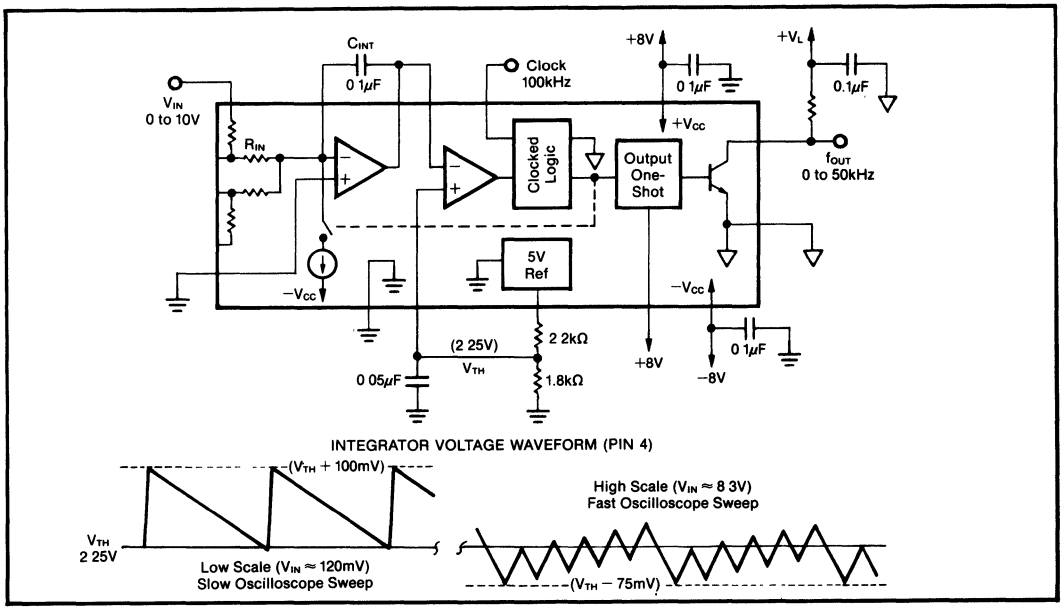


FIGURE 9. Circuit Diagram and Integrator Voltage Waveform for Low Power Supply Voltage Operation..

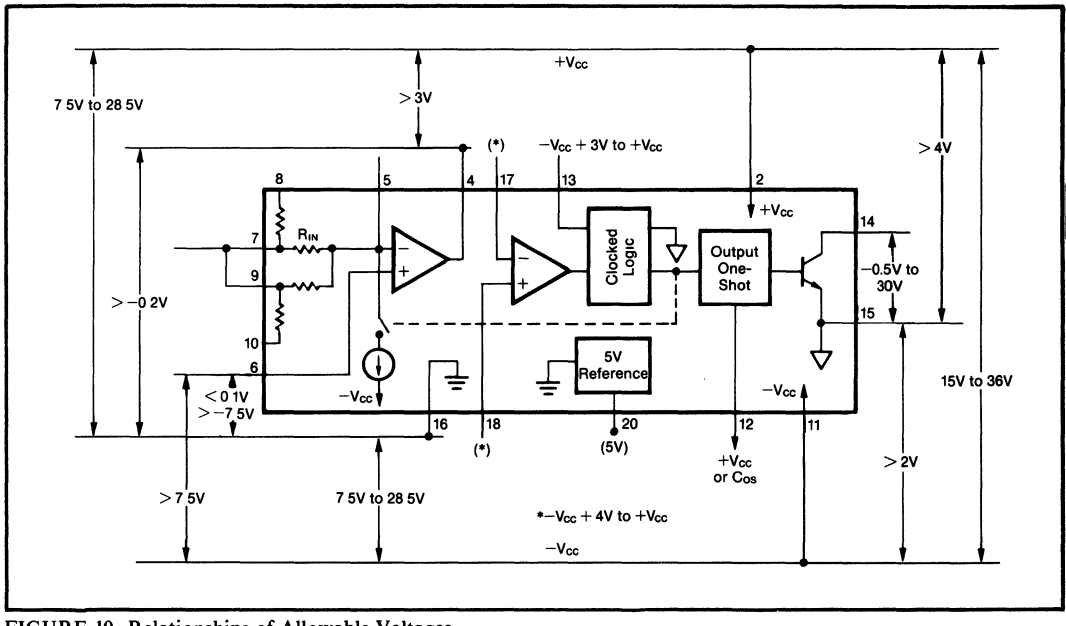


FIGURE 10. Relationships of Allowable Voltages.

+100mV to −75mV integrator voltage swing (referred to the noninverting comparator input). The offset voltage applied to the comparator's noninverting input is derived from a resistive voltage divider from V_{REF}.

The relationships of the allowable operating voltage ranges on important pins is shown in Figure 10. Note that the integrator amplifier output cannot swing more than 0.2V below ground. Although this is not "normal" for an operational amplifier, a special internal design of this type optimizes high-frequency performance. It is this characteristic which necessitates the offsetting of the noninverting comparator input in voltage-to-frequency mode to avoid negative output swing.

FREQUENCY-TO-VOLTAGE MODE

The VFC101 can also function as a frequency-to-voltage converter by applying an input frequency to the comparator input as shown in Figure 11. The input resistor, R_{IN}, is connected as a feedback resistor. The voltage at the integrator amp output is proportional to the ratio of the input frequency to the clock frequency. The transfer function is

$$V_{OUT} = (f_{IN}/f_{CLOCK})\ 20V$$

This transfer function is complementary to the voltage-to-frequency mode transfer function, making voltage-to-frequency-to-voltage conversions simple and accurate.

Direct coupling of the input frequency to the comparator is easily accomplished by driving both comparators with complementary frequency input signals. Alternatively, one of the comparator inputs can be biased at half the logic voltage (using V_{REF} and a voltage divider) and the other input driven direclty.

The proper timing of the input frequency waveform is shown in Figure 11. The input pulse should go low for one clock cycle, centered around a falling edge of the clock. The minimum acceptable input pulse width must fall no later than 200ns before a negative clock edge and rise no sonner than 200ns after the falling clock edge. An input pulse which remains low for more than one falling edge of the clock will produce incorrect output voltages. Positive (active high) input pulses can be accepted by reversing the connections to pins 14 and 15. Figure 12 shows a digital conditioning circuit which will accept any input duty cycle and provide the proper pulse width to the comparator. Each rising edge at this circuit's input generates the required negative pulse at the inverting comparator input. The noninverting comparator is driven by a complementary signal.

The integrator amplifier output is designed to drive up to 10,000pF and 5kΩ loads in frequency-to-voltage mode. This allows driving long lines in a large system.

Ripple voltage in the voltage output is unavoidable and is inversely proportional to the value of the integrator capacitor. Figure 13 shows the output ripple and settling time as a function of the C_{INT} value.

The ripple frequency is equal to the input frequency. Its magnitude can be reduced by using a large integrator capacitor value, but at the sacrifice of slow settling time

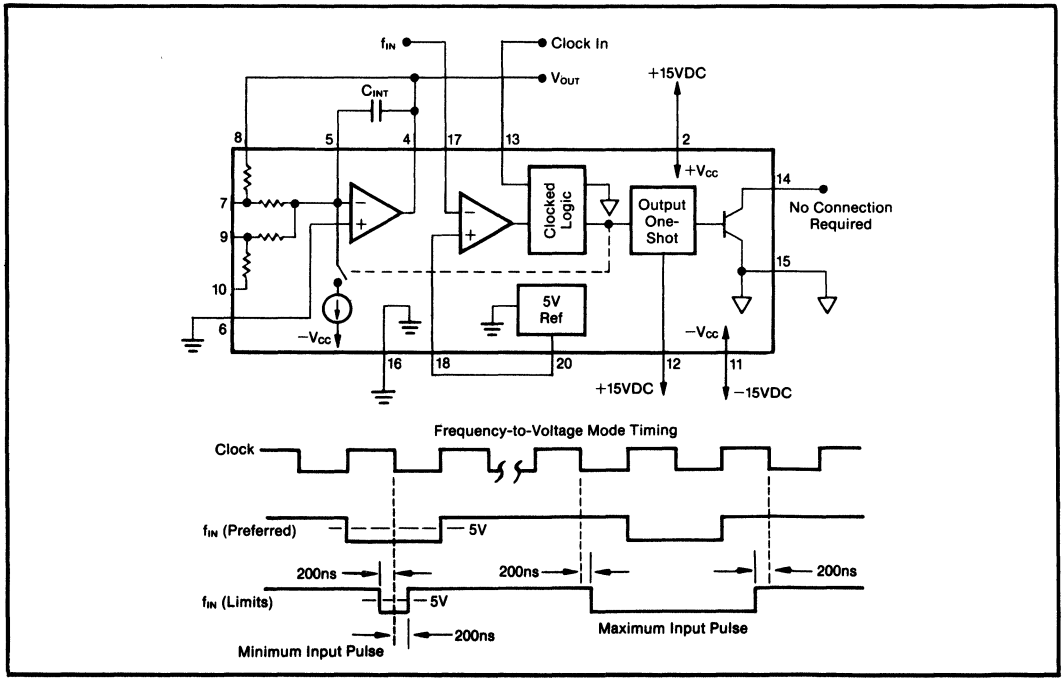


FIGURE 11. Circuit and Timing Diagram of a Frequency-to-Voltage Converter.

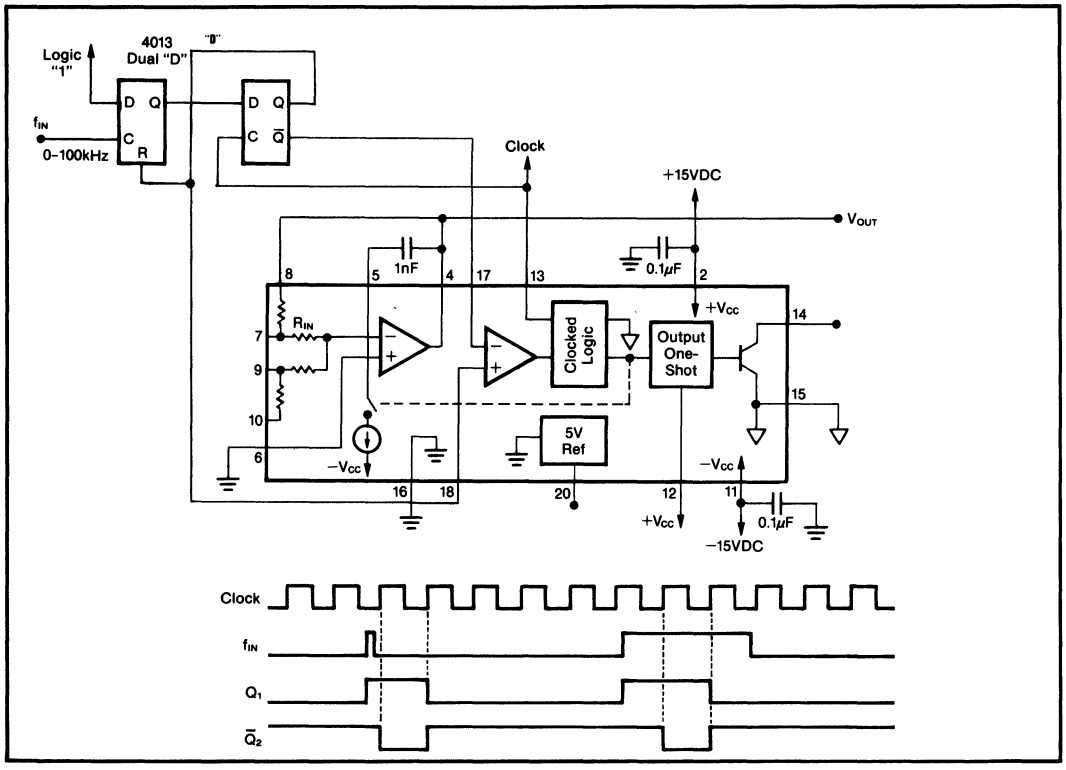


FIGURE 12. Digital Timing Input Conditioning Circuit for Frequency-to-Voltage Operation.

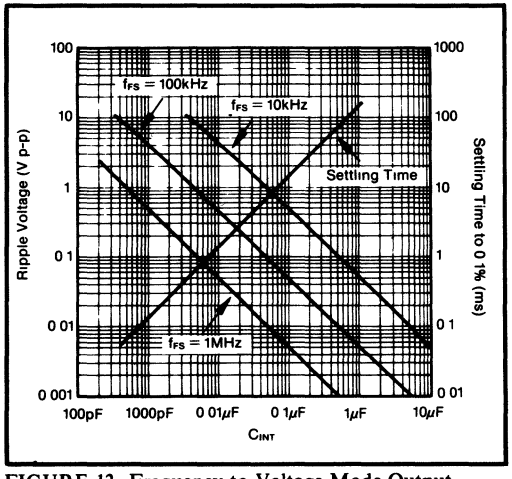


FIGURE 13. Frequency-to-Voltage Mode Output Ripple and Settling Time vs Integrator Capacitance.

at the voltage output in response to an input frequency change. The settling time constant is equal to $R_{IN} \times C_{INT}$. A better compromise between output ripple and settling time can be achieved by using a moderately low integrator capacitor value and adding a low-pass filter on the analog output. The cutoff frequency of the filter should be made below the lowest expected input frequency to the frequency-to-voltage converter.

NOTE: Several useful applications circuits may be found in the VFC100 product data sheet. These require only minor adaptation to the different pinout and input resistor configurations of the VFC101.

Mylar™, Teflon™ E.I. du Pont de Nemours & Co.

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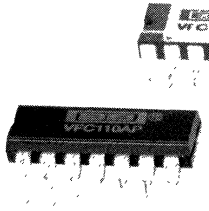


VFC110

ADVANCE INFORMATION
SUBJECT TO CHANGE

High-Frequency VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- HIGH FREQUENCY OPERATION: 4MHz FS max
- EXCELLENT LINEARITY: ±0.05% max at 1MHz ±0.05% typ at 2MHz
- PRECISION 5V REFERENCE
- DISABLE PIN

APPLICATIONS

- INTEGRATING A/D CONVERSION
- PROCESS CONTROL
- VOLTAGE ISOLATION
- VOLTAGE-CONTROLLED OSCILLATOR
- FM TELEMETRY

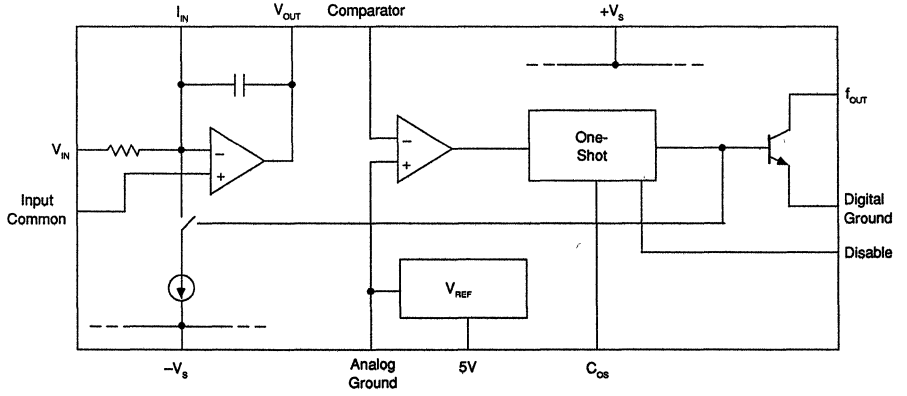
DESCRIPTION

The VFC110 Voltage-to-Frequency Converter is a third-generation VFC offering improved features and performance. These include higher frequency operation, an on-board precision 5V reference and a Disable function.

The precision 5V reference and can be used for offsetting the VFC transfer function, as well as exciting transducers or bridges. The Disable pin allows several VFCs' outputs to be paralleled, multiplexed, or simply to shut off the VFC. The open-collector frequency output is TTL/CMOS-compatible. The output may be isolated by using an opto-coupler or transformer.

Internal input resistor, one-shot and integrator capacitors simplify applications circuits. These components are trimmed for a full-scale output frequency of 4MHz at 10V input. No additional components are required for many applications.

The VFC100 is packaged in plastic and ceramic 14-pin DIPs. Industrial and military temperature range grade-outs are available.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491 • FAX: (602) 889-1510

PDS-861

SPECIFICATIONS

At T_A = +25°C and V_S = ±15V unless otherwise noted.

MODEL	VFC110BG			VFC110AG/SG/AP			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
VOLTAGE TO FREQUENCY OPERATION							
Nonlinearity, f_{FS} = 100kHz		0.005	0.01		0.01	0.05	%FS
f_{FS} = 1MHz		0.01	0.05			0.1	%FS
f_{FS} = 2MHz		0.015			*		%FS
f_{FS} = 4MHz		1			*		%FS
Gain Error, f = 1MHz			5			*	%
Gain Drift, f = 1MHz			50			100	ppm/°C
Relative to V_{REF}		50			100		ppm/°C
PSRR			0.05			0.1	%/V
INPUT							
Full Scale Input		250	500		*	*	µA
I_B		15	30		20	60	nA
V_{OS}			3			3	mV
V_{OS} Drift		35			*		µV/°C
OPEN COLLECTOR OUTPUT							
V_O Low			0.4			*	V
$I_{LEAKAGE}$		0.1	1		*	*	µA
Fall Time		25				*	ns
Delay to Rise		25				*	ns
REFERENCE VOLTAGE							
Voltage	4.95	5.00	5.05	*	*	*	V
Voltage Drift			20			50	ppm/°C
Load Regulation, I_O = 0 to 10mA		3	10		*	*	mV
PSRR, V_S = ±8 to ±18V		5			*		mV/V
Current Limit		15			*		mA
DISABLE INPUT							
V_{HIGH}	2.0			*			V
V_{LOW}			0.4			*	V
I_{HIGH}		0.1			*		µA
I_{LOW}		1			*		µA
POWER SUPPLY							
Voltage	±8	±15	±18	*	*	*	V
Current		13	16		*	*	mA
TEMPERATURE RANGE							
Specified							
AG, BG, AP	–25		+85	*		*	°C
SG	–55		+125				°C
Storage							
AG, BG, SG	–65		+150	*		*	°C
AP	–40		+125	*		*	°C

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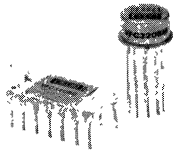


VFC320

MILITARY & DIE VERSIONS AVAILABLE

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- HIGH LINEARITY, 12 to 14 bits
  - ±0.005% max at 10kHz FS
  - ±0.03% max at 100kHz FS
  - ±0.1% typ at 1MHz FS
- V/F OR F/V CONVERSION
- 6-DECADE DYNAMIC RANGE
- 20ppm/°C max GAIN DRIFT
- OUTPUT DTL/TTL/CMOS COMPATIBLE

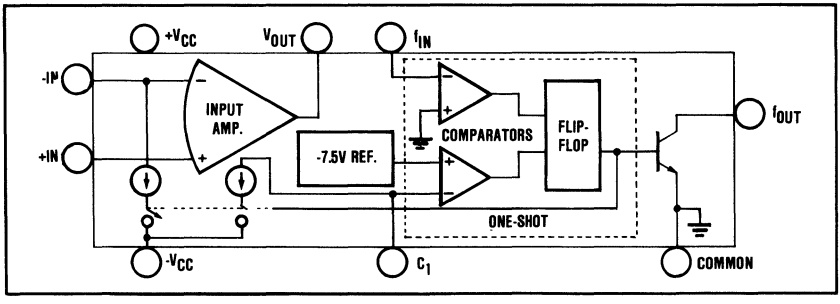
APPLICATIONS

- INEXPENSIVE A/D AND D/A CONVERTER
- DIGITAL PANEL METERS
- TWO-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY
- FM MOD/DEMOD OF TRANSDUCER SIGNALS
- PRECISION LONG TERM INTEGRATOR
- HIGH RESOLUTION OPTICAL LINK FOR ISOLATION
- AC LINE FREQUENCY MONITOR
- MOTOR SPEED MONITOR AND CONTROL

DESCRIPTION

The VFC320 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital output is an open collector and the digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with DTL, TTL, and CMOS logic families.

High linearity (0.005%, max at 10kHz FS) is achieved with relatively few external components. Two external resistors and two external capacitors are required to operate. Full scale frequency and input voltage are determined by a resistor in series with -IN and two capacitors (one-shot timing and input amplifier integration). The other resistor is a non-critical open collector pull-up (f_{OUT} to $+V_{CC}$). The VFC320 is available in three performance/temperature grades and two package configurations. The TO-100 versions are hermetically sealed, and specified for the -25°C to +85°C and -55°C to +125°C ranges, and the dual-in-line units are specified from -25°C to +85°C.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-483D

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC power supply unless otherwise noted.

CHARACTERISTICS	CONDITIONS	VFC320BG/BM/SM MIN	VFC320BG/BM/SM TYP	VFC320BG/BM/SM MAX	VFC320CG/CM MIN	VFC320CG/CM TYP	VFC320CG/CM MAX	UNITS
V/F CONVERTER $F_{OUT} = V_{IN}/7.5\ R_1C_1$, Figure 4								
INPUT TO OP AMP								
Voltage Range(1)	Fig. 4 with $e_2 = 0$	>0		Note 2				V
	Fig. 4 with $e_1 = 0$	<0		-10				V
Current Range(1)	$I_{IN} = V_{IN}/R_{IN}$	+0.25		+750	•		•	µA
Bias Current								
Inverting Input			4	8		•	•	nA
Noninverting Input			10	30		•	•	nA
Offset Voltage(3)				±0.15			•	mV
Offset Voltage Drift			±5			•		µV/°C
Differential Impedance		300 ‖ 5	650 ‖ 5		•	•		kΩ ‖ pF
Common-mode Impedance		300 ‖ 3	500 ‖ 3		•	•		kΩ ‖ pF
ACCURACY								
Linearity Error(1)(4)(5)	Fig. 4 with $e_2 = 0$(6)							
	0.01Hz ≤ f_{OUT} ≤ 10kHz		±0.004	±0.005		±0.0015	±0.002	% of FSR
	0.1Hz ≤ f_{OUT} ≤ 100kHz		±0.008	±0.030		•	•	% of FSR
	1Hz ≤ f_{OUT} ≤ 1MHz		±0.1			•		% of FSR
Offset Error Input Offset Voltage(3)				±15			•	ppm of FSR
Offset Drift(7)			±0.5			•		ppm of FSR/°C
Gain Error(3)			±5	±10		•	•	% of FSR
Gain Drift(7)	f = 10kHz			50			20	ppm of FSR/°C
Full Scale Drift (offset drift & gain drift)(7)(8)(9)	f = 10kHz			50			20	ppm of FSR/°C
Power Supply Sensitivity	±V_{CC} = 14VDC to 18VDC			±0.015			•	% of FSR/%
DYNAMIC RESPONSE								
Full Scale Frequency	C_{LOAD} ≤ 50pF			1			•	MHz
Dynamic Range		6			•			decades
Settling Time	(V/F) to specified linearity for a full scale input step		Note 10			•		
Overload Recovery	< 50% overload		Note 10			•		
OPEN COLLECTOR OUTPUT								
Voltage, Logic "0"	I_{SINK} = 8mA, max			0.4			•	V
Leakage Current, Logic "1"	V_O = 15V		0.01	1.0		•	•	µA
Voltage, Logic "1"	External pull-up resistor required (see Figure 4)			V_{PU}			•	V
Duty Cycle at FS	For Best Linearity		25			•		%
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF		100	•		•		ns
F/V CONVERTER $V_{OUT} = 7.5\ R_1C_1\ F_{IN}$, Figure 9								
INPUT TO COMPARATOR								
Impedance		50 ‖ 10	150 ‖ 10		•	•		kΩ ‖ pF
Logic "1"		+1.0		+V_{CC}	•		•	V
Logic "0"		-V_{CC}		-0.05	•		•	V
Pulse-width Range		0.25			•			µs
OUTPUT FROM OP AMP								
Voltage	I_O = 7mA	0 to +10			•			V
Current	V_O = 7VDC	+10			•			mA
Impedance	Closed-loop			0.1			•	Ω
Capacitive Load	Without oscillation			100			•	pF
POWER SUPPLY								
Rated Voltage			±15			•		V
Voltage Range		±13		±20	•		•	V
Quiescent Current			±6.5	±7.5		•	•	mA
TEMPERATURE RANGE								
Specification								
B and C Grades		−25		+85	•		•	°C
S Grade		−55		+125				°C
Operating								
B and C Grades		−25		+85	•		•	°C
S Grade		−55		+125				°C
Storage		−65		+150	•		•	°C

*Specification the same as for VFC320BG/BM/SM.

NOTES
1. A 25% duty cycle at full scale (0.25mA input current) is recommended where possible to achieve best linearity.
2. Determined by R_{IN} and full scale current range constraints.
3. Adjustable to zero. See Offset and Gain Adjustment section.
4. Linearity error at any operating frequency is defined as the deviation from a straight line drawn between the full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section.
5. When offset and gain errors are nulled, at an operating temperature, the linearity error determines the final accuracy.
6. For $e_1 = 0$ typical linearity errors are 0.01% at 10kHz, 0.2% at 100kHz, 0.1% at 1MHz.
7. Exclusive of external components' drift.
8. FSR = Full Scale Range (corresponds to full scale and full scale input voltage).
9. Positive drift is defined to be increasing frequency with increasing temperature.
10. One pulse of new frequency plus 50nsec typical.

ABSOLUTE MAXIMUM RATINGS

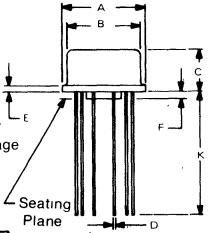
Supply Voltages	±20V
Output Sink Current at f_{OUT}	50mA
Output Current at V_{OUT}	+20mA
Input Voltage, -Input	$\pm V_{CC}$
Input Voltage, +Input	$\pm V_{CC}$
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	+300°C

MECHANICAL

VFC320BM/CM/SM TO-100 PACKAGE

NOTE
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane

Pin numbers shown for reference only. Numbers may not be marked on package.

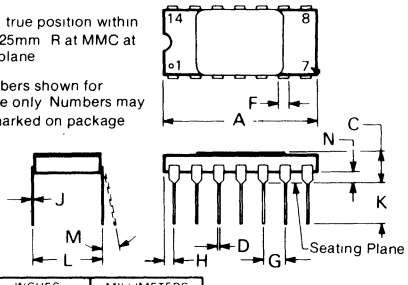


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
	.335	.370	8.51	9.40
	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.70	
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

VFC320BG/CG CERAMIC DUAL-IN-LINE

NOTE
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane

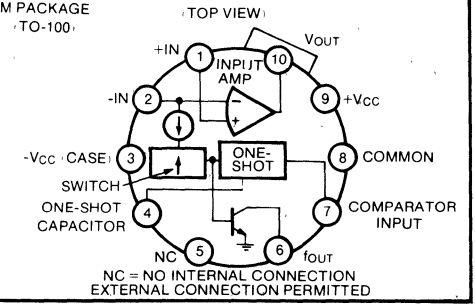
Pin numbers shown for reference only. Numbers may not be marked on package.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M		10°		10°
N	.009	.060	0.23	1.52

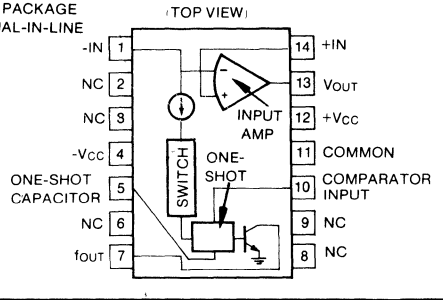
PIN CONFIGURATIONS

M PACKAGE (TO-100) (TOP VIEW)



NC = NO INTERNAL CONNECTION
EXTERNAL CONNECTION PERMITTED

G PACKAGE (DUAL-IN-LINE) (TOP VIEW)



DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (100% full scale input or frequency and 0.1% of full scale called zero). Linearity is the most demanding measure of voltage-to-frequency converter performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. Once the full scale frequency is chosen, the linearity is a function of operating frequency as it varies between zero and full scale. Examples for 10kHz full scale are shown in Figure 2. Best linearity is achieved at lower gains ($\Delta f_{OUT}/\Delta V_{IN}$) with operation as close to the chosen full scale frequency as possible.

The high linearity of the VFC320 makes the device an excellent choice for use as the front end of A/D converters with 12- to 14-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire digital transmission).

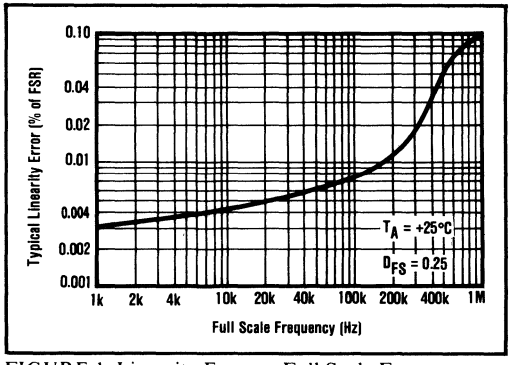


FIGURE 1. Linearity Error vs Full Scale Frequency.

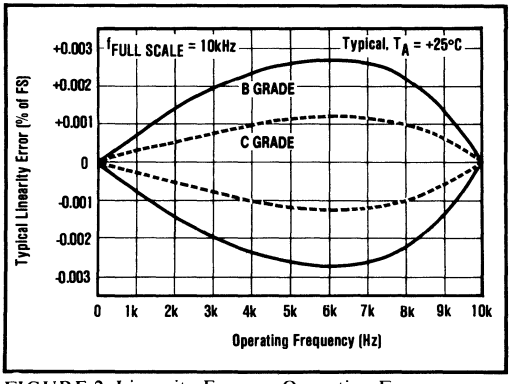


FIGURE 2. Linearity Error vs Operating Frequency.

FREQUENCY STABILITY VS TEMPERATURE

The full scale frequency drift of the VFC320 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 10kHz. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially R_1 and C_1) must be added to the drift of the VFC320.

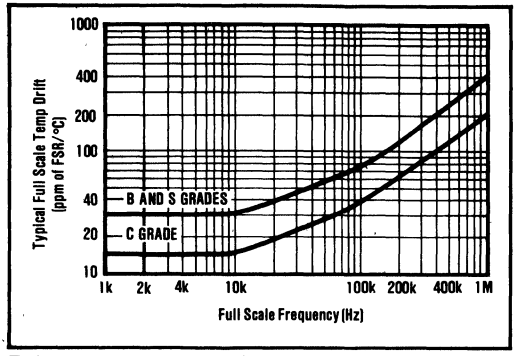


FIGURE 3. Full Scale Drift vs Full Scale Frequency.

RESPONSE

Response of the VFC320 to changes in input signal level is specified for a full scale step, and is 50nsec plus 1 pulse of the new frequency. For a 10V input signal step with the VFC320 operating at 100kHz full scale, the settling time to within ±0.01% of full scale is 10μs.

THEORY OF OPERATION

The VFC320 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. The circuit shown in Figure 4 is composed of an input amplifier, two comparators and a flip-flop (forming a one-shot), two switched current sinks, and an open collector output transistor stage. Essentially the input amplifier acts as an integrator that produces a two-part ramp. The first part is a function of the input voltage, and the second part is dependent on the input voltage and current sink. When a positive input voltage is applied at V_{IN}, a current will flow through the input resistor, causing the voltage at V_{OUT} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_1$. During this time the constant current sink is disabled by the switch. Note, this period is only dependent on V_{IN} and the integrating components.

When the ramp reaches a voltage close to zero, comparator A sets the flip-flop. This closes the current sink switches as well as changing f_{OUT} from logic 0 to logic 1. The ramp now begins to ramp up, and 1mA charges through C_1 until V_{C1} = -7.5V. Note this ramp period is dependent on the 1mA current sink, connected to the negative input of the op amp, as well as the input voltage. At this -7.5V threshold point at C_1, comparator B resets the flip-flop, and the ramp voltage begins to ramp down again before the input amplifier has a chance to saturate. In effect the comparators and flip-flop form a one-shot whose period is determined by the internal reference and a 1mA current sink plus the external capacitor, C_1. After the one-shot resets, f_{OUT} changes back to logic 0 and the cycle begins again.

The transfer function for the VFC320 is derived for the

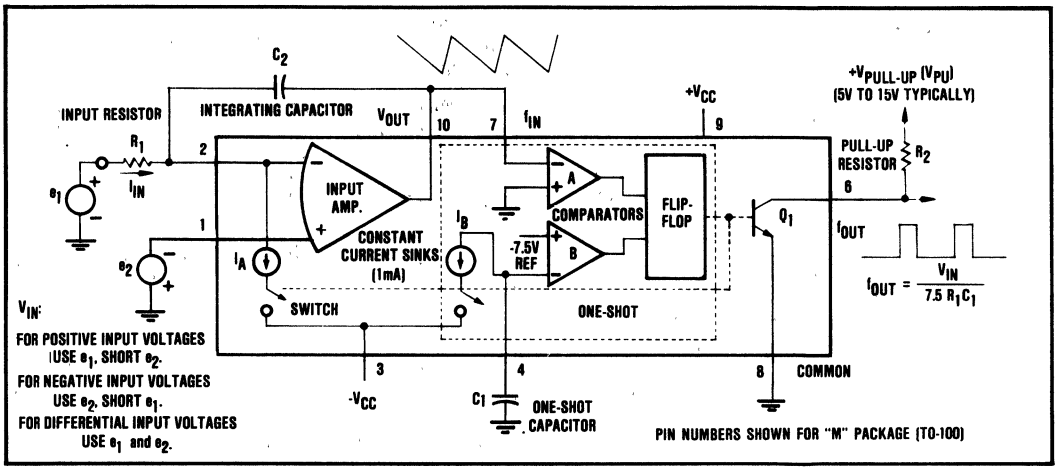


FIGURE 4. Functional Block Diagram of the VFC320.

the circuit shown in Figure 4. Detailed waveforms are shown in Figure 5.

$$f_{OUT} = \frac{1}{t_1 + t_2} \quad (1)$$

In the time t ∴ + t| the integrator capacitor C_2 charges and discharges but the net voltage change is zero.

$$\text{Thus } \Delta Q = 0 = I_{IN}\, t_1 + (I_{IN} - I_A)\, t_2 \quad (2)$$

$$\text{So that } I_{IN}\,(t_1 + t_2) = I_A\, t_2 \quad (3)$$

$$\text{But since } t_1 + t_2 = \frac{1}{f_{OUT}} \text{ and } I_{IN} = \frac{V_{IN}}{R_1} \quad (4), (5)$$

$$f_{OUT} = \frac{V_{IN}}{I_A R_1 t_2} \quad (6)$$

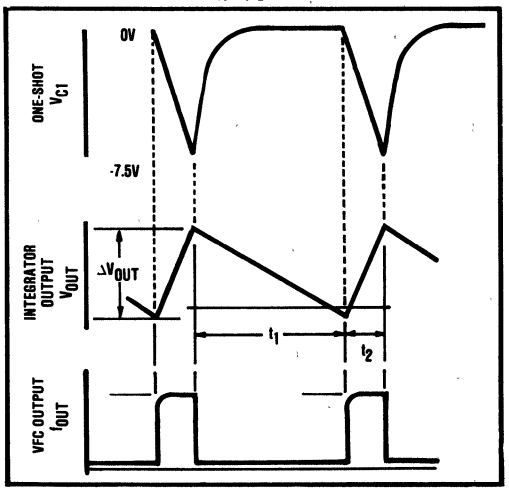


FIGURE 5. Integrator and VFC Output Timing.

In the time t_2, I_B charges the one-shot capacitor C_1 until its voltage reaches -7.5V and trips comparator B.

$$\text{Thus } t_2 = \frac{C_1\, 7.5}{I_B} \quad (7)$$

$$\text{Using (7) in (6) yield } f_{OUT} = \frac{V_{IN}}{7.5\, R_1 C_1} \times \frac{I_B}{I_A} \quad (8)$$

Since $I_A = I_B$ the result is

$$f_{OUT} = \frac{V_{IN}}{7.5\, R_1 C_1} \quad (9)$$

Since the integrating capacitor, C_2, affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to I_{IN}, since this parameter will add directly to the gain error of the VFC. C_1, which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.

The operation of the VFC320 as a highly linear frequency-to-voltage converter, follows the same theory of operation as the voltage-to-frequency converter. e_1 and e_2 are shorted and F_{IN} is disconnected from V_{OUT}. F_{IN} is then driven with a signal which is sufficient to trigger comparator A. The one-shot period will then be determined by C_1 as before, but the cycle repetition frequency will be dictated by the digital input at F_{IN}.

DUTY CYCLE

The duty cycle (D) of the VFC is the ratio of the one-shot period (t_2) or pulse width, PW, to the total VFC period ($t_1 + t_2$). For the VFC320, t_2 is fixed and $t_1 + t_2$ varies as the input voltage. Thus the duty cycle, D, is a function of the input voltage. Of particular interest is the duty cycle at full scale frequency, D_{FS}, which occurs at full scale input. D_{FS} is a user determined parameter which affects linearity.

$$D_{FS} = \frac{t_2}{t_1 + t_2} = PW \times f_{FS}$$

Best linearity is achieved when D_{FS} is 25%. By reducing equations (7) and (9) it can be shown that

$$D_{FS} = \frac{V_{IN}\ max\ /\ R_1}{1mA} = \frac{I_{IN}\ max}{1mA}$$

Thus $D_{FS} = 0.25$ corresponds tc I_{IN} max = 0.25mA.

INSTALLATION AND OPERATING INSTRUCTIONS

VOLTAGE-TO-FREQUENCY CONVERSION

The VFC320 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.

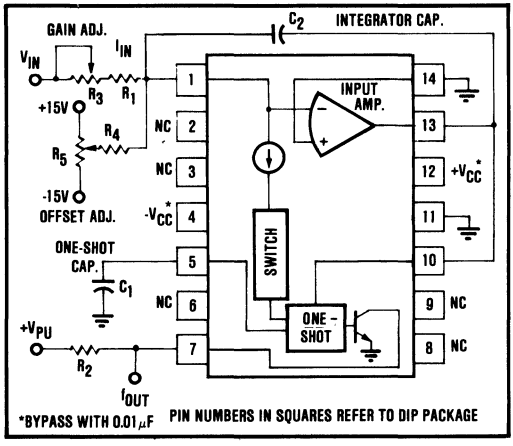


FIGURE 6. Connection Diagram for V/F Conversion, Positive Input Voltages.

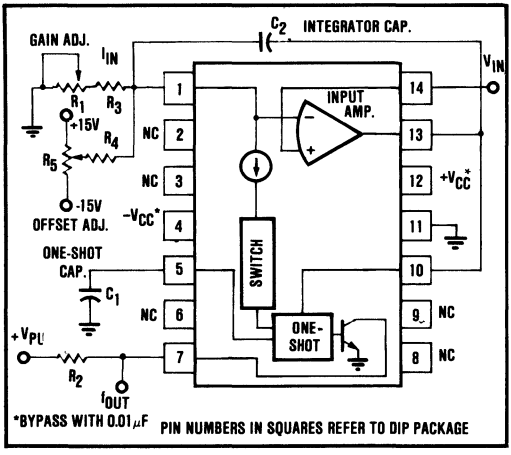


FIGURE 7. Connection Diagram for V/F Conversion, Negative Input Voltages.

EXTERNAL COMPONENT SELECTION

In general the design sequence consists of: (1) choosing f_{MAX}, (2) choosing the duty cycle at full scale ($D_{FS} = 0.25$ typically), (3) determining the input resistor, R_1 (Figure 4), (4) calculating the one-shot capacitor, C_1, (5) selecting the integrator capacitor C_2, and (6) selecting the output pull-up resistor, R_2.

Input Resistors R_1 and R_3

The input resistance (R_1 and R_3 in Figures 6 and 7) is calculated to set the desired input current at full scale input voltage. This is normally 0.25mA to provide a 25% duty cycle at full scale input and output. Values other than $D_{FS} = 0.25$ may be used but linearity will be affected. The nominal value is R_1 is

$$R_1 = \frac{V_{IN}\ max}{0.25mA} \qquad (10)$$

If gain trimming is to be done, the nominal value is reduced by the tolerance of C_1 and the desired trim range. R_1 should have a very-low temperature coefficient since its drift adds directly to the errors in the transfer function.

One-Shot Capacitor, C_1

This capacitor determines the duration of the one-shot pulse. From equation (9) the nominal value is

$$C_{1\ nom} = \frac{V_{IN}}{7.5\ R_1\ f_{OUT}} \qquad (11)$$

For the usual 25% duty at $f_{MAX} = V_{IN}/R_1 = 0.25mA$ there is approximately 15pF of residual capacitance so that the design value is

$$C_1(pF) = \frac{33 \times 10^6}{f_{FS}} - 15 \qquad (12)$$

where f_{FS} is the full scale output frequency in Hz. The temperature drift of C_1 is critical since it will add directly to the errors of the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize stray capacitance associated with C_1. It should be mounted as close to the VFC320 as possible. Figure 8 shows pulse width and full scale frequency for various values of C_1 at $D_{FS} = 25\%$.

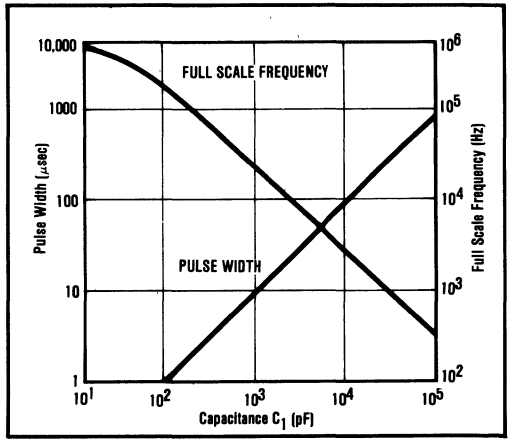


FIGURE 8. Output Pulse Width ($D_{FS} = 0.25$) and Full Scale Frequency vs External One-shot Capacitance.

Integrating Capacitor, C_2

Since C_2 does not occur in the V/F transfer function equation (9), its tolerance and temperature stability are not important; however, leakage current in C_2 causes a gain error. A ceramic type is sufficient for most applications. The value of C_2 determines the amplitude of V_{OUT}. Input amplifier saturation, noise levels for the comparators and slew rate limiting of the integrator

determine a range of acceptable values,

$$C_2\,(\mu F) = \begin{cases} 100/f_{FS};\ \text{if } f_{FS} \leq 100\text{kHz} \\ 0.001;\ \text{if } 100\text{kHz} < f_{FS} \leq 500\text{kHz} \\ 0.0005;\ \text{if } f_{FS} > 500\text{kHz} \end{cases} \quad (13)$$

Output Pull Up Resistor R_2.

The open collector output can sink up to 8mA and still be TTL-compatible. Select R_2 according to this equation:

$$R_2 \text{ min } (\Omega) = V_{PULLUP}/(8\text{mA} - i_{LOAD})$$

A 10% carbon film resistor is suitable for use as R_2.

Trimming Components R_3, R_4, R_5

R_5 nulls the offset voltage of the input amplifier. It should have a series resistance between 10kΩ and 100kΩ and a temperature coefficient less than 100ppm/°C. R_4 can be a 10% carbon film resistor with a value of 10MΩ.

R_3 nulls the gain errors of the converter and compensates for intitial tolerances of R_1 and C_1. Its total resistance should be at least 20% of R_1, if R_1 is selected 10% low. Its temperature coefficient should be no greater than five times that of R_1, to maintain a low drift of the R_3 - R_1 series combination.

OFFSET AND GAIN ADJUSTMENT PROCEDURES

To null errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 x full scale.
2. Adjust R_5 for proper output.
3. Apply the full scale input voltage.
4. Adjust R_3 for proper output.
5. Repeat steps 1 through 4.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC320 is 0.015% of FSR/% max. To maintain ±0.015% conversion, power supplies which are stable to within ±1% are recommeded. These supplies should be bypassed as close as possible to the converter with 0.01μF capacitors.

Internal circuitry causes some current to flow in the common connection (pin 11 on DIP package). Current flowing into the f_{OUT} pin (logic sink current) will also contribute to this current. It is advisable to separate this common lead ground from the analog ground associated with the integrator input to avoid errors produced by these currents flowing through any ground return impedance.

DESIGN EXAMPLE

Given a full scale input of +10V, select the values of R_1, R_2, R_3, C_1, and C_2 for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

Selecting C_1 ($D_{FS} = 0.25$)

$C_1 = [(33 \times 10^6)/f_{MAX}] - 15$ $\quad [(66 \times 10^6)/f_{MAX}] - 15$ if $D_{FS} = 0.5$

$= [(33 \times 10^6)/100\text{kHz}] - 15$

$= 315\text{pF}$

Choose a 300pF NPO ceramic capacitor with 1% to 10% tolerance.

Selecting R_1 and R_3 ($D_{FS} = 0.25$)

$R_1 + R_3 = V_{IN}\text{ max}/0.25\text{mA}$ $\quad V_{IN}\text{ max}/0.5\text{mA}$ if $D_{FS} = 0.5$

$= 10\text{V}/0.25\text{mA}$

$= 40\text{k}\Omega$

Choose 32.4kΩ metal film resistor with 1% tolerance and R_3 = 10kΩ cermet potentiometer.

Selecting C_2

$C_2 = 10^2/F_{max}$

$= 10^2/100\text{kHz}$

$= 0.001\mu\text{F}$

Choose a 0.001μF capacitor with ±5% tolerance.

Selecting R_2

$R_2 = V_{PULLUP}/(8\text{mA} - i_{LOAD})$

$= 5\text{V}/(8\text{mA} - 1.6\text{mA})$, one TTL-load = 1.6mA

$= 781\Omega$

Choose a 750Ω 1/4-watt carbon compensation resistor with ±5% tolerance.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC320 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses zero. Choose C_3 to make t = 0.1t (see Figure 9). For input signals with amplitudes less than 5V, pin 10 should be biased closer to zero, to insure that the input signal at pin 10 crosses the zero threshold. Errors are nulled following the procedure given on this page, using 0.001 x full scale frequency to null offset, and full scale frequency to null the gain error. Use equations from V/F calculations to find R_1, R_3, R_4, R_5, C_1 and C_2.

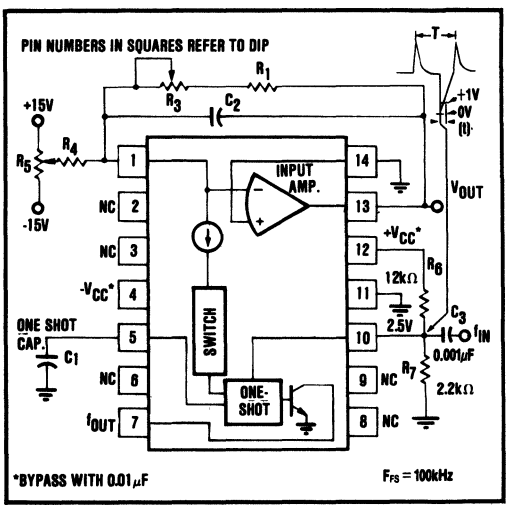


FIGURE 9. Connection Diagram for F/V Conversion.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC320 ideal for a variety of VFC applications. High accuracy allows the VFC320 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 14 bits.

Figures 10 - 14 show typical applications of the VFC320.

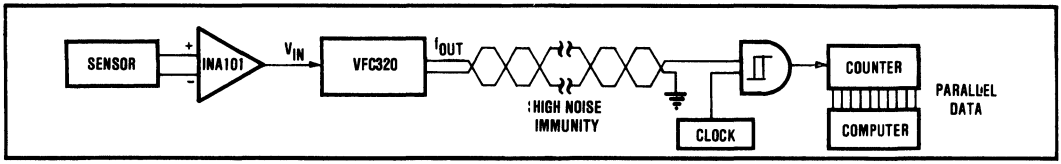


FIGURE 10. Inexpensive A/D with Two-Wire Digital Transmission Over Twisted Pair.

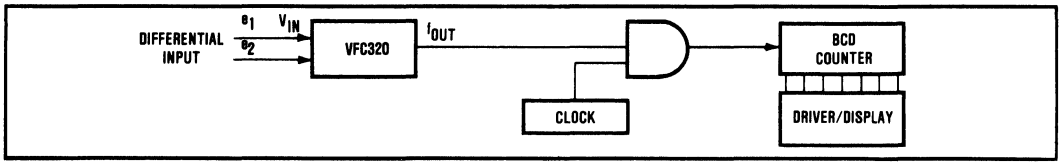


FIGURE 11. Inexpensive Digital Panel Meter.

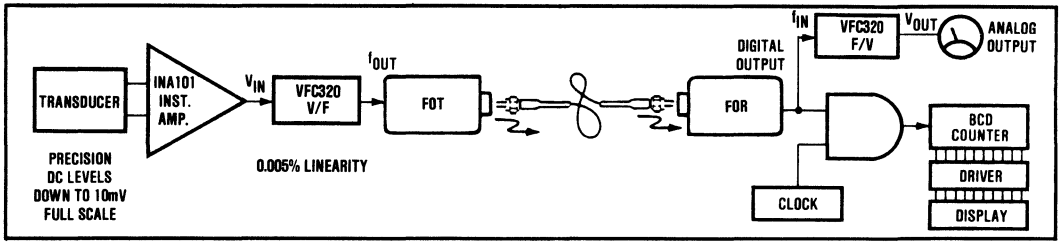


FIGURE 12. Remote Transducer Readout via Fiber Optic Link (analog and digital output).

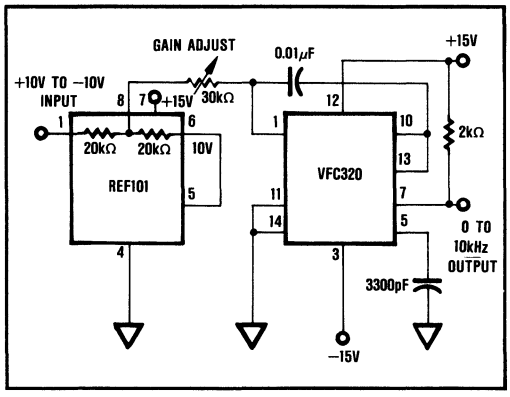


FIGURE 13. Bipolar input is accomplished by offsetting the input to the VFC with a reference voltage. Accurately matched resistors in the REF101 provide a stable half-scale output frequency at zero volts input.

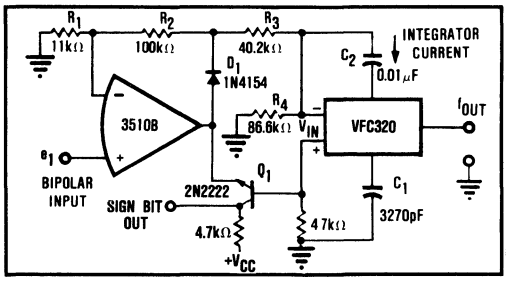
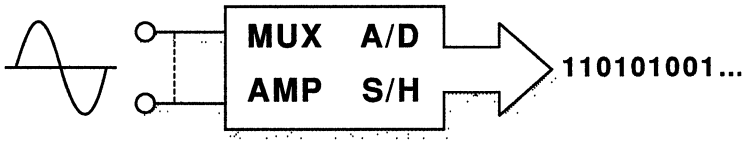


FIGURE 14. Absolute value circuit with the VFC320. Op amp, D_1 and Q_1 (its base-emitter junction functioning as a diode) provide full-wave rectification of bipolar input voltages. VFC output frequency is proportional to $|e_1|$. The sign bit output provides indication of the input polarity.



DATA ACQUISITION COMPONENTS

If your system requires data acquisition and conversion, you may want to consider one of our system data modules (SDM). These products contain a multiplexer, A/D converter, and timing and control logic, with instrumentation amplifiers and sample/hold circuits also available.

As with all Burr-Brown conversion products, these units are designed to provide a total solution. They are very popular in applications requiring rapid design turnaround because they offer a fully optimized analog circuit layout. Typical applications include industrial measurement and control (such as process monitoring), test equipment, and any other application requiring total guaranteed performance with a minimum of utilized space.

11

DATA ACQUISITION COMPONENTS SELECTION GUIDE

The Selection Guide shows parameters for the high grade. Refer to the Product Data Sheet for a full selection of grades. Models shown in **boldface** are new products introduced since publication of the previous *Burr-Brown IC Data Book.*

DATA ACQUISITION COMPONENTS **Boldface = NEW**

Model	Channels	Resolution (Bits)	Linearity Error (%FSR)	Input Range (V)[1]	Throughput Rate (kHz)	Temp Range[2]	Pkg[3]	Page
SDM862	**16 single ended**	**12**	**±0.012**	**10, 20 U/B**	**33**	**Com, Ind, Mil**	**LCC, PGA**	**11-3**
SDM863	**8 differential**	**12**	**±0.012**	**10, 20 U/B**	**33**	**Com, Ind, Mil**	**LCC, PGA**	**11-3**
SDM872	**16 single ended**	**12**	**±0.012**	**10, 20 U/B**	**50**	**Com, Ind, Mil**	**LCC, PGA**	**11-3**
SDM873	**8 differential**	**12**	**±0.012**	**10, 20 U/B**	**50**	**Com, Ind, Mil**	**LCC, PGA**	**11-3**

NOTES: (1) U/B indicates the input voltage range for the model: U = unipolar, B = bipolar. (2) Temperature Range: Com = 0°C to +70°C, Ind = –25°C to +85°C, Mil = –55°C to +125°C. (3) LCC = Hermetic 0.95" (typ) square Leadless Chip Carrier, PGA = Hermetic 1.1" (typ) square Pin Grid Array.

MODELS STILL AVAILABLE BUT NOT FEATURED IN THIS BOOK

SDM854AG
SDM854BG
SDM856JG
SDM856KG
SDM857JG
SDM857KG

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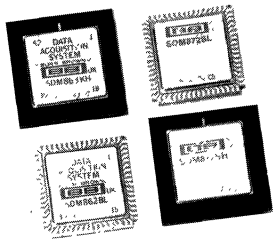


SDM862
SDM863
SDM872
SDM873

16 Single Ended/8 Differential Input 12-BIT DATA ACQUISITION SYSTEMS

FEATURES

- COMPLETE 12-BIT DATA ACQUISITION SYSTEM IN A MINIATURE PACKAGE
- INPUT RANGES SELECTABLE FOR UNIPOLAR OR BIPOLAR OPERATION
- THROUGHPUT RATES:

	862/3	872/3
8-BIT ACCURACY:	45kHz	67kHz
12-BIT ACCURACY:	33kHz	50kHz

- SELECTABLE GAINS OF 1, 10, AND 100
- FULL MICROPROCESSOR COMPATIBLE INTERFACE
- GUARANTEED NO MISSING CODES OVER TEMPERATURE
- SURFACE-MOUNT OR PIN GRID ARRAY PACKAGE OPTIONS
- FULL SPECIFICATION OVER THREE TEMPERATURE RANGES:
  0 TO +70°C
  −25 TO +85°C
  −55 TO +125°C

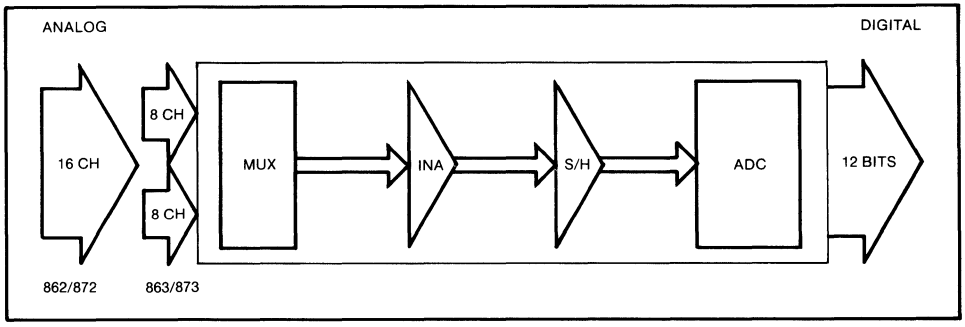
DESCRIPTION

16 Single-Ended Inputs:	SDM862	SDM872
8 Differential Inputs:	SDM863	SDM873
33kHz Throughput Rate:	SDM862	SDM863
50kHz Throughput Rate:	SDM872	SDM873

The SDM components are complete, pin-compatible, data acquisition systems housed in a hermetically sealed 1"-square leadless chip carrier or a 1.1"-square pin grid array. The small package outlines and low power consumption provide an ideal data acquisition solution when space is at a premium.

The devices comprise of an input multiplexer, instrumentation amplifier with selectable gains, sample/hold amplifier and A/D converter with microprocessor interface and three-state buffers.

The SDM family will accept unipolar or bipolar voltage inputs in the range 0 to +10V, ±5V and ±10V. For low-level signals, jumper-selectable gains of 10 or 100 can be applied. The number of input channels can be expanded by the addition of multiplexers. System integration is simplified by the microprocessor interface and the facility of the sample/hold amplifier being controlled directly by the A/D converter.



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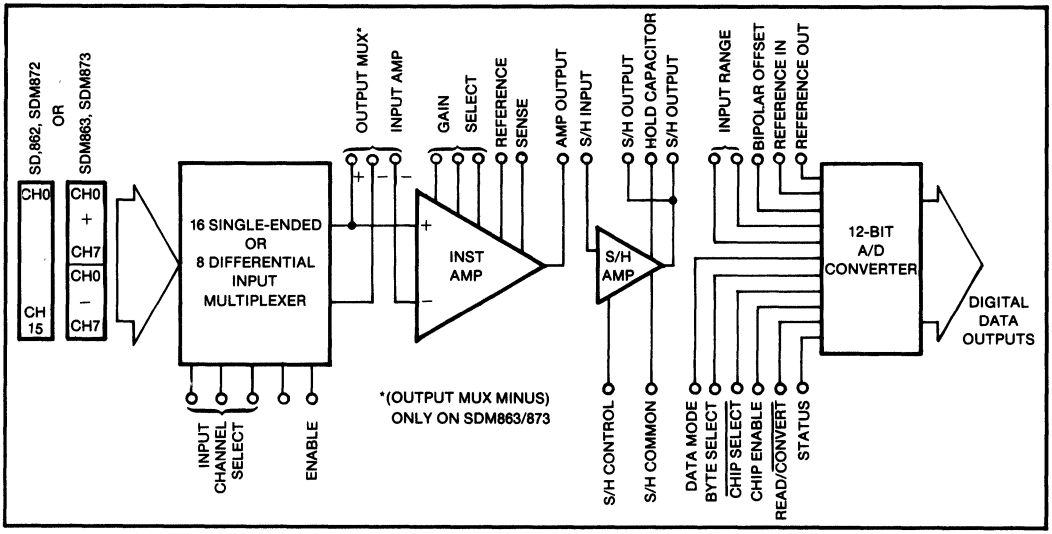


SPECIFICATIONS

ELECTRICAL

At 25°C, V_{CC} = ±15V, V_{DD} = 5V, external sample/hold capacitor of 4700pF. All grades are burned-in at +125°C for 48 hours min

	SDM862/863/872/873 J, A, R			SDM862/863/872/873 K, B, S			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			*	BITS
INPUT							
ANALOG							
Voltage Ranges. Bipolar			±5, ±10				V
Unipolar			0-10				V
Input Impedance: On Channel		10^{10}			*		Ω
Off Channel		10^{10}			*		Ω
Input Capacitance: On Channel		20			*		pF
Off Channel		20			*		pF
CMRR (20VDC to 1kHz)	80	85		*	*		dB
Crosstalk (20Vp-p, 1kHz)[1]		–85	–80		*	*	dB
Feedthrough (at 1kHz)[1]		–85	–80		*	*	dB
Offset (channel to channel) G = 1 [2]		30	100		*	*	µV
Input Bias Current/Channel		1	5		*	*	nA
Input Voltage Range [3]	+10	+11		*	*		V
	–10	–15		*	*		V
DIGITAL							
MUX Input Channel Select. Logic '1' (2V)		5	30		*	*	µA
Logic '0' (0.8V)		5	30		*	*	µA
S/H Command: Logic '1' (2V)		0 2			*		nA
Logic '0' (0 8V)		5	30		*	*	µA
ADC Section: Logic '1' (2.4V)			10			*	µA
Logic '0' (0.8V)			10			*	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Integral Linearity [4]			±0.024			±0.012	%FSR
Differential Linearity [4]			±0.024			±0.012	%FSR
Gain Error [5]: G = 1		0.7			*		%
: G = 100		0.9			*		%
Unipolar Offset Error [5]		16			*		mV
Bipolar Offset Error [5]		50			*		mV
Noise Error							
(Measured at S/H Output) G = 1		0.5	1		*	*	mVp-p
Droop Rate		50	500		*	*	µV/ms
Temperature Coefficients.							
Unipolar Offset			20			15	ppm of FSR/°C
Bipolar Offset			30			25	ppm of FSR/°C
Full-scale Calibration			60			35	ppm of FSR/°C

SPECIFICATIONS

ELECTRICAL

At 25°C, $V_{CC} = \pm 15V$, $V_{DD} = 5V$, external sample/hold capacitor of 4700pF

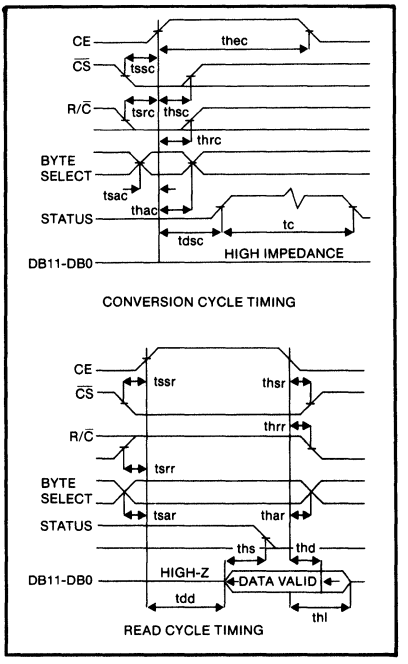
	SDM862/863/872/873 J, A, R			SDM862/863/872/873 K, B, S			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
SYSTEM TIMINGS							
ADC Conversion Time SDM862/SDM863	15	20	25	*	*	*	µs
SDM872/SDM873	9	12	15	*	*	*	µs
S/H Aperture Delay		50			*		ns
S/H Aperture Uncertainty		2			*		ns
TIMING							
Acquisition Time (to 0 01% of final value for full scale step)		5			*		µs
Throughput (Serial Mode)							
SDM862/SDM863			22			*	kHz
SDM872/SDM873			28			*	kHz
(Overlap Mode)							
SDM862/SDM863			33			*	kHz
SDM872/SDM873			50			*	kHz
MULTIPLEXER[6]							
Switching time (between channels)		+1 5			*		µS
Settling time (10V step to 0 02%)		2 5			*		µS
Enable time 'ON'		1	2		*	*	µS
'OFF'		0 25	0 5		*	*	µS
INSTRUMENTATION AMPLIFIER[6]							
Settling time (20V step to 0 01%)							
G = 1		5	12 5		*	*	µS
G = 10		3	7 5		*	*	µS
G = 100		4	7 5		*	*	µS
Slew rate	12	17		*	*		V/µS
S/H AMPLIFIER[6]							
Acquisition time (10V step to 0 01%)		5			*		µS
Aperture delay		50			*		nS
Hold mode settling time		1 5			*		µS
Slew rate		10			*		V/µS
OUTPUT							
DIGITAL DATA							
Output Codes Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels Logic 0 (sink = 1 6mA)			+0 4			*	V
Logic 1 (source = 500µA)	+2 4			*			V
Leakage (Data Bits Only), High-Z State	−5	0 1	+5	*	*	*	µA
POWER SUPPLY REQUIREMENTS							
Rated Voltage. Analog ($\pm V_{CC}$)	14 25	15	15 75	*	*	*	VDC
Digital (VDD)	4 75	5	5 25	*	*	*	VDC
Supply Drain +15V		28	40		*	*	mA
−15V		36	45		*	*	mA
+5V		8	15		*	*	mA
Power Dissipation		1	1 4		*	*	W
TEMPERATURE RANGE							
Operating Temperature Range							
JH, KH/JL, KL	0		70	*		*	°C
AH, BH/AL, BL	−25		+85	*		*	°C
RH, SH/RL, SL	−55		+125	*		*	°C
Storage Temperature Range	−65		+150	*		*	°C

* Specification same as SDM862/863/872/873J, A, R grades

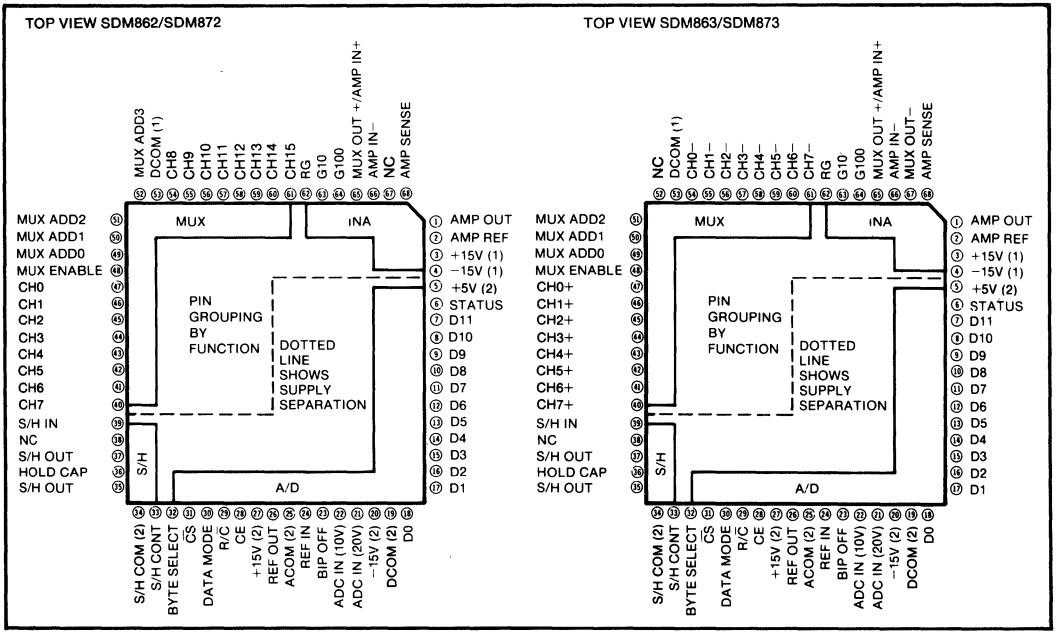
NOTES (1) Measured at the sample and hold output (2) Measured with all input channels grounded. (3) The range of voltage on any input with respect to common over which accuracy and leakage current is guaranteed (4) Applicable over full operating temperature range NO MISSING CODES GUARANTEED OVER TEMPERATURE RANGE (5) Adjustable to zero using external potentiometer or select-on-test resistor (6) Specifications are at +25°C and measured at 50% level of transition

DIGITAL TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
CONVERT MODE					
tdsc	Status delay from CE		100	200	nS
thec	CE Pulse width	50	30		nS
tssc	CS to CE setup	50	20		nS
thsc	CS low during CE high	50	20		nS
tsrc	R/C to CE setup	50	0		nS
thrc	R/C low during CE high	50	20		nS
tsac	Byte select to CE setup	0	0		nS
thac	Byte selected valid during CE high	50	20		nS
tc 86X	Conversion time. 12 bit cycle	15	20	25	µS
	8 bit cycle	10	13	17	µS
tc 87X	Conversion time 12 bit cycle	9	12	15	µS
	8 bit cycle	6	8	10	µS
READ MODE					
tdd	Access time from CE		75	150	nS
thd	Data valid after CE low	25	35		nS
thl	Output float delay		100	150	nS
tssr	CS to CE setup	50	0		nS
tsrr	R/C to CE setup	0	0		nS
tsar	Byte select to CE setup	50	25		nS
thsr	CS valid after CE low	0	0		nS
thrr	R/C high after CE low	0	0		nS
thar	Byte select valid after CE low	50	25		nS
ths 86X	Status delay after data valid	300	500	1000	nS
ths 87X	Status delay after data valid	100	300	600	nS



PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

+VCC TO ACOM	−0 5V TO +16V	ANALOG INPUT SIGNAL RANGE	+ VCC + 20V TO − VCC − 20V
− VCC TO ACOM	+0 5V TO −16V	DIGITAL INPUT SIGNAL	− 0 5V TO + VDD
+ VDD TO DCOM	−0 5V TO +5 5V	ACOM TO DCOM	± 1V

PIN DESIGNATION	DEFINITION	COMMENTS SDM8X2 = SDM862 or SDM872
CH0 to CH15 CH0 to CH7 (+, −) (PINS 40 to 47, 54 to 61)	Channel Inputs	Analog Inputs (Total 16) for single-ended and differential operation. Unused inputs must be connected to analog common.
MUX OUT+/AMP IN+ (PIN 65)	MULTIPLEXER "HI" OUTPUT	On the SDM8X2 this is the multiplexer output. On the SDM8X3 it is the output of the positive selected inputs. It is connected internally to the positive input of the instrumentation amplifier.
MUXOUT (PIN 67)	MULTIPLEXER "LO" OUTPUT	This pin is used on the SDM8X3 only. It should be connected to the negative input of the instrumentation amplifier.
AMPIN (PIN 66)	Negative Input of Instrumentation Amplifier	On the SDM8X2 this should be connected to analog common On the SDM8X3 it should be connected to Muxout—(Pin 67).
AMPOUT (PIN 1)	Output of instrumentation amplifier	This pin should be connected to the input of the S/H amplifier (Pin 39).
AMP SENSE (PIN 68)	Output sense line of instrumentation amplifier.	This pin will normally be connected direct to AMP OUT (Pin 1).
AMP REF (PIN 2)	Reference for amplifier output	This pin will normally be connected to analog common. Care should be taken to minimize tracking and contact resistance to analog common to optimize system accuracy.
S/H OUT (PINS 35/37)	Output of sample/hold amplifier	Two pins are provided to facilitate a guard ring around the hold capacitor pin. These pins should be connected to either ADC in (20V) or ADC in (10V) depending on the desired range.
HOLD CAP (PIN 36)	Connection for hold capacitor on S/H amplifier	The tracking to the hold capacitor should be as short as possible and a guard ring employed using Pins 35 and 37.
ADC IN (20V); ADC IN (10V) (PINS 21, 22)	Inputs to A/D converter	Connect to S/H amplifier output. Use appropriate Pin for desired range.
RG, G10, G100 (PINS 62, 63, 64)	Gain setting Pins on instrumentation amplifier	For Gain = 1, no connections. For Gain = 10, connect G10 to RG. For Gain = 100, connect G100 to RG.
REF OUT (PIN 26)	10V Reference voltage	This is the reference voltage for the A/D converter.
REF IN, BIP OFF (PINS 24, 23)	Reference input and offset input to A/D converter	Connect trim potentiometers (or select-on-test resistors) to these pins for unipolar or bipolar operation as shown in Figures 12, 13.
S/H IN (PIN 39)	Input to sample/hold amplifier	Connect to amp out (Pin 1).
MUX ENABLE (PIN 48)	Multiplex enable/disable	Logic '1' on this pin will enable a selected channel on the internal multiplexer. Logic '0' de-selects all channels.
MUX ADD0 to MUX ADD3 (PINS 49 to 52)	Address inputs for channel selection	These address lines select a particular channel as specified in Figure 24.
S/H CONT (PIN 33)	Track/Hold control on S/H amplifier	Logic '1' holds an analog value for conversion by the A/D converter. This line may be controlled by the status (Pin 6) of the converter to simplify external timing control.
S/H COM (PIN 34)	Reference for S/H logic control	Connect to digital common
D0 to D11 (PINS 7 to 18)	3-state digital outputs	The 12- or 8-bit result of a conversion is available as output on these pins (D0-LSB, D11-MSB).
STATUS (PIN 6)	Status of A/D conversion	This output is at logic '1' while the internal A/D converter is carrying out a conversion. This pin may be used to directly control the S/H amplifier.
CE (PIN 28)	Chip enable	This input must be at logic '1' to either initiate a conversion or read output data (see Figures 10, 17, 18, 19, 20).
$\overline{CS}$ (PIN 31)	Chip select	This input must be at logic '0' to either initiate a conversion or read output data (see Figures 10, 17, 18, 19, 20).
R/$\overline{C}$ (PIN 29)	Read/convert	Data can be read when this pin is logic '1' or a conversion can be initiated when this pin is logic '0'. This pin is typically connected to the R/$\overline{W}$ control line of a microprocessor-based system (see Figures 10, 17, 18, 19, 20).
DATA MODE (PIN 30)	Select 12 or 8 Bit Data	When data mode is at logic '1' all 12 output data bits are enabled simultaneously. When data mode is at logic '0' MSBs and LSBs are controlled by byte select (Pin 32).
BYTE SELECT (PIN 32)	Byte address, short cycle	When reading output data, byte select at logic '0' enables the 8 MSBs. Byte select at logic '1' enables the 4 LSBs. The 4 LSBs can therefore be connected to four of the MSB lines for inter-connection to an 8-bit bus. In start convert mode, logic '0' enables a 12-bit conversion while logic '1' will short cycle the conversion to 8 bits (see Figure 10).
+15V(1),+15V(2)(PINS 3, 27)	Power Supply	Connect to +15V supply using decoupling as indicated in Figures 15, 16.
−15V(1),−15V(2)(PINS 4, 20)	Power Supply	Connect to −15V supply using decoupling as indicated in Figures 15, 16.
ACOM(2) (PIN 25)	Analog common	Analog common connection. Note that a common (including digital common) should be connected together at one point close to the device
DCOM (1) (PIN 53)	Reference for Mux logic control.	Connect to digital common.
+5V (PIN 5)	Logic power supply	Connect to +5V digital supply line with decoupling as in Figures 15, 16.
DCOM(2) (PIN 19)	Reference for A/D converter control lines	Connect to S/H common at one point close to device.
NC (PIN 38)	No internal connection	

SYSTEM DESCRIPTION

The SDM comprises four circuit elements—an input-protected multiplexer, an instrumentation amplifier, a sample/hold amplifier, and an analog-to-digital converter.

INSTALLATION

MULTIPLEXER

The SDM family has a choice of input multiplexers (MUX).

SDM862 and SDM872: 16 single-ended inputs
SDM863 and SDM873: 8 differential inputs

The select inputs are designed for use with TTL and CMOS logic levels and do not require pull-up resistors to ensure break-before-make operation.

On all models, the analog inputs may be expanded using the enable control. See Figure 1. When the enable is at a logic "0," the internal MUX is disabled, allowing additional multiplexers to be connected in parallel. The limiting factor for the number of additional multiplexers is the cumulative effect of leakage current flowing in the signal source impedance, causing offset errors.

Differential inputs will generally eliminate the noise associated wtih common system grounds, but care must be taken to ensure that neither of the differential inputs exceed the maximum input range. Otherwise, signal distortion will result. A return path for the input bias currents must always be provided. This prevents the charging of stray capacitances in applications using floating sources, such as transformers and thermocouples. Multiplexer inputs are protected from overvoltage, as indicated in the electrical specifications, and should be current limited to 25mA. To avoid signal distortion on the selected channel, MUX inputs that are not selected should have their input voltages limited to between $-V_{CC}$ and $+V_{CC}-4V$, as voltages outside of these values can turn on the non-selected channel. A graph of this characteristic is shown in Figure 2 with a possible circuit solution where it is known that the input voltages will exceed the above values.

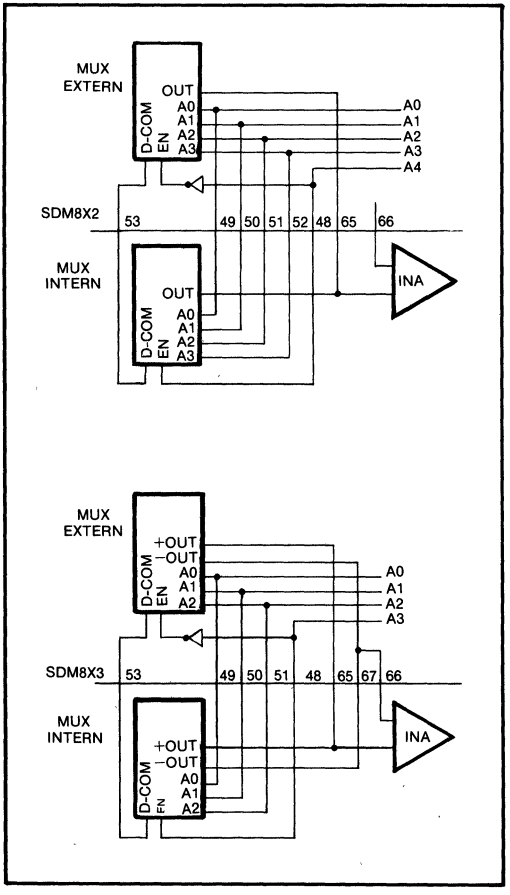


FIGURE 1. External Multiplexer Connections for Differential and Single-Ended Operation.

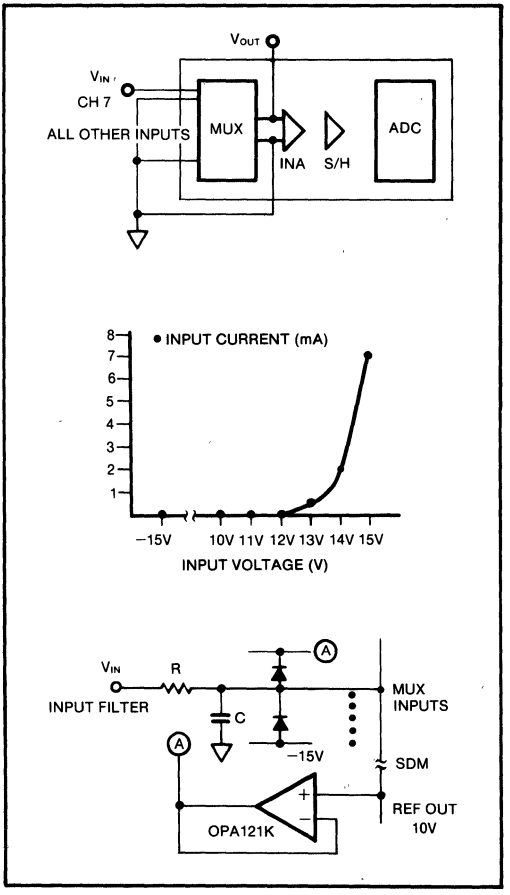


FIGURE 2. MUX Inputs With Limited Input Voltages and Possible Circuit Solution for Non-limited Cases.

Where high-speed operation is required and channels require rapid sampling, then it is important to buffer the inputs against the effect of current sharing between the MUX output capacitance and the input filter capacitance. See Figure 3.

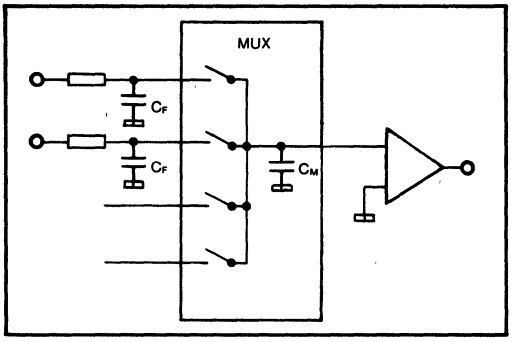


FIGURE 3. Filter and MUX Capacitance.

All data acquisition systems using a MUX require consideration of the errors that may be introduced by MUX output capacitance. The applications information explains this more fully in the input filtering section.

Shown in Figure 4 is an application that demonstrates the flexibility of signal conditioning and gives the opportunity to use a higher bandwidth filter. Diodes shown are low leakage types (1na). The low output impedance of the amplifiers reduces the time taken to charge MUX capacitance C_M.

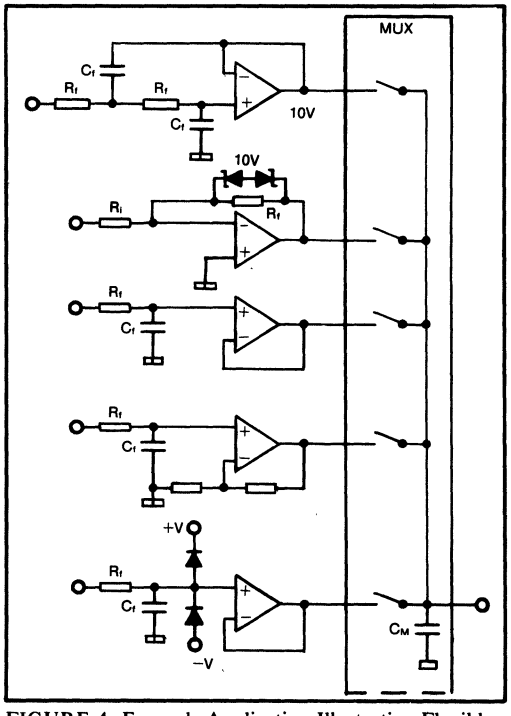


FIGURE 4. Example Application Illustrating Flexible Signal Conditioning.

INSTRUMENT AMPLIFIER

The instrument amplifier (INA) presents a very high input impedance to the signal source, eliminating gain errors introduced by voltage divider action between the source output impedance and SDM input impedance. Where the differential models are used, the INA performs the differential to single-ended conversion required to drive the sample/hold amplifier. Gains may be set by using external jumpers, to values of 1 (no jumper), 10 and 100. For gains other than these presets, the following formula may be used to find an external resistor value to add in series with the G = 10 or G = 100 jumpers.

$$R_{ext} = \frac{40\ K\Omega}{G-1} - Ri$$

Where Ri = 4444Ω, G = 10 input.
404Ω, G = 100 input.

It should be noted that the internal gain set resistors have a ±20% tolerance and ±20ppm/°C drift.

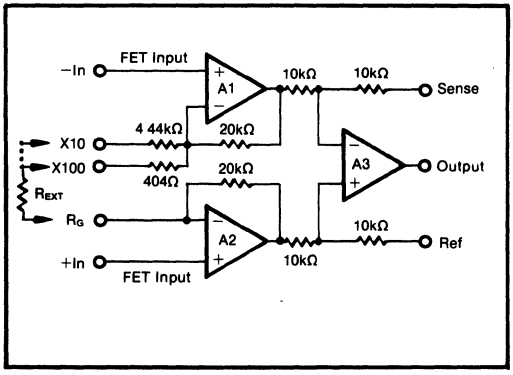


FIGURE 5. Use External Gain Set Resistor.

Where it is necessary to keep the input amplifiers from saturating or increasing the overall gain, then the gain of the output amplifier can be increased from unity by using the circuit in Figure 6.

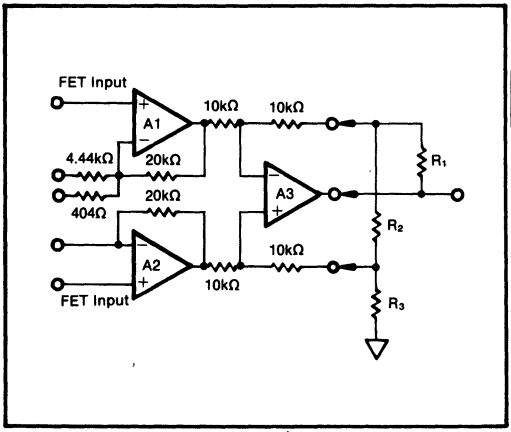


FIGURE 6. Increasing Output Amplifier Gain.

The values of the resistors in Figure 6 are in the following table.

O/P gain	R_1 & R_3 ohms	R_2 ohms
2	1200	2740
5	1000	511
10	1500	340

Matching of R_1 and R_3 is required to maintain high common mode rejection (CMR), R_2 sets the gain and may be varied without effect on CMR.

To ensure that the effects of temperature are minimized when altering the gain with external components, it is very important to use low tempco resistors. When connecting the output sense, ensure that series resistance is minimized because resistance present will degrade CMR.

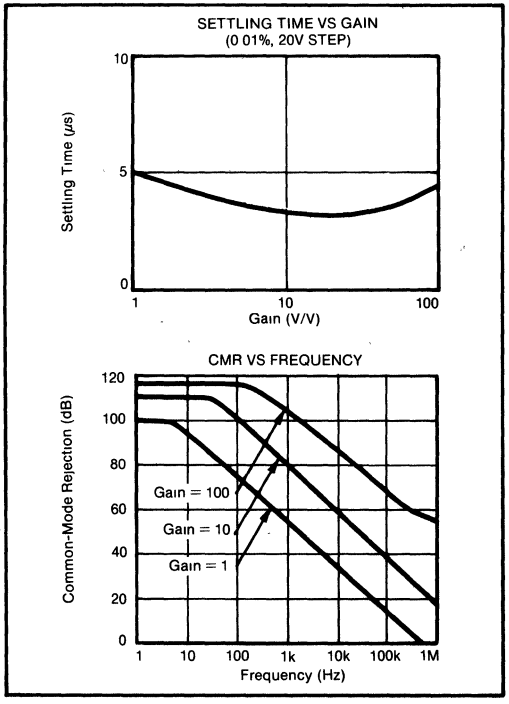


FIGURE 7. Typical INA Settling Time and CMR.

Some applications may require programmable gains. This may be realized with Figure 8.

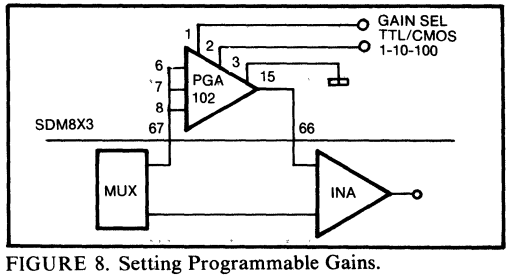


FIGURE 8. Setting Programmable Gains.

SAMPLE/HOLD AMPLIFIER

The Sample/Hold amplifier (S/H) is used to track the incoming signal and "hold" the required instantaneous value so that it does not change while the ADC is carrying out its conversion. Timing for the S/H may be derived from the STATUS output of the ADC, with care being taken to comply with the SDM timing considerations.

Capacitors with high insulation resistance and low dielectric absorption such as Teflon™, polystyrene or polypropylene should be used as storage elements. (Polystyrene should not be used above +80°C.) Teflon™ is recommended for high temperature operation. Care should be taken in the printed circuit layout to minimize stray capacitance and leakage currents from the capacitor to minimize charge offset and droop errors. The use of a guard ring driven by the S/H output around the pin connecting to the hold capacitor is recommended. (Refer to the application board layout for an example of this.)

The value of the external hold capacitor determines the droop rate, charge offset and acquisition time of the S/H, Figure 9. Droop rate for the SDM is specified with a hold capacitor value of 4700pf. There is a trade-off between acquisition time and droop rate, as the hold capacitor is increased in value it takes longer to charge, and hence there is a corresponding increase in acquisition time and reduction in droop rate. The droop rate is determined by the amount of leakage present in the SDM, board leakage and the dielectric absorption of the hold capacitance. The hold capacitor is also a compensation element for the S/H and should not be reduced below 2nf for good stability. The offset error in sample mode is not affected by the hold capacitor. However, during the transition to hold mode there is approximately 5pC of charge injected into the hold capacitor, causing an offset error that has been nulled for use with a 5nf hold capacitor. Any other value for the hold capacitor will cause a minor but fixed hold mode offset to be introduced, and is proportional to the change in value from 5nf. Therefore the SDM should be offset nulled with the S/H in hold mode.

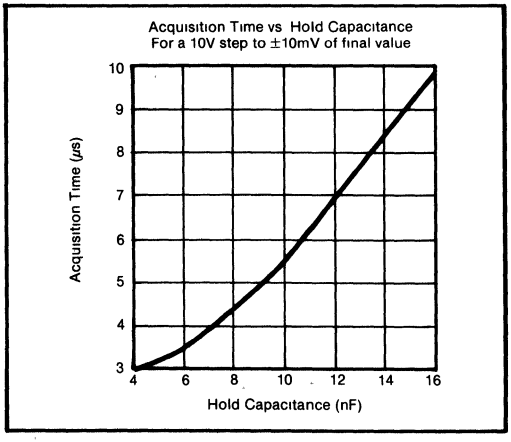


FIGURE 9. Acquisition Time vs. Hold Capacitance for a 10V Step Settling to ±10mV of Final Value.

ANALOG-TO-DIGITAL CONVERTER

This circuit element converts the analog voltage presented by the sample/hold amplifier to a digital number in binary format under control of the digital signals detailed in Figure 10. The converter can convert unipolar and bipolar signals in the range 10V and 20V. It can be calibrated to remove gain and offset errors from the entire system. The converter contains its own clock, voltage reference, and microprocessor interface with 3-state outputs. The converter will normally be used to digitize signals to 12-bit resolution, but it can be short-cycled to provide 8-bit resolution at higher speed. The digital output is compatible with 8- or 16-bit data buses, the data format being selected by control signals as detailed in Figure 10.

CE	$\overline{CS}$	R/$\overline{C}$	DATA MODE	BYTE SELECT	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↓	0	0	X	0	Initiate 12-bit conversion
↓	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

FIGURE 10. Control Input Truth Table.

OPERATING INSTRUCTIONS

OPERATING MODES

The SDM can operate in one of two modes, namely serial and overlap, as shown in Figure 11. In serial mode, control of the device is such that a multiplexer channel X is first selected, time is then allowed for the instrumentation amplifier to settle, the sample/hold amplifier is set to HOLD mode and finally a conversion is carried out. This procedure is then repeated for channel Y. Faster throughput can be obtained using overlap mode. While a conversion is being carried out by the ADC on a voltage from channel X held on the sample/hold, channel Y is selected and the multiplexer and instrumentation amplifier allowed to settle. In this way, the total throughput time is limited only by the sum of the sample/hold acquisition time and the ADC conversion time.

CALIBRATION - UNIPOLAR

If adjustment of unipolar offset and gain are not required, then the gain set potentiometer in Figure 12 (Unipolar operation) may be replaced with a 50Ω, 1% metal film resistor, and the offset network replaced with a connection from pin 23 to ground.

CALIBRATION - BIPOLAR

If adjustment of bipolar offset and gain are not required then the gain set and offset potentiometers in Figure 13 (Bipolar operation) may both be replaced with 50Ω, 1% metal film resistors.

CALIBRATION - GENERAL

The input voltage ranges of the ADC are 0–10V, ±5V and ±10V. Calibration in all ranges is achieved by adjusting the offset and gain potentiometers (indicated in Figures 12 and 13) such that the 000 to 001 code transition takes place at +1/2LSB from full-scale negative (–FS) and the FFE to FFF transition takes place at –3/2LSB from full-scale positive (+FS). The procedure is therefore to select the required range from Figure 14, apply the specified (–FS+1/2LSB) voltage to any selected input channel and adjust the offset potentiometer for the 000 to 001 transition. The (+FS–3/2LSB) voltage should then be applied to the same channel and the gain potentiometer adjusted for the FFE to FFF transition. The offset should always be made before the gain adjustment.

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS

It should be noted that the multiplexer/instrumentation amplifier section and sample/hold plus ADC section of the SDM have separate power connections. This is to enable more flexible grounding techniques to be implemented, Figures 15, 16. It also facilitates the use of independent decoupling of the analog front-end power supply, and the ADC plus associated digital circuitry power supply if desired. In this way, a separately decoupled analog front-end can be made to be substantially more immune to power supply noise generated by the ADC circuitry than if the power supplies to the two sections were directly connected. This feature is important where low-level signals are in use or high input signal noise immunity is desired.

The output section has three grounds:
Pin 25 Analog Common, A/D Converter
Pin 34 S/H Amp digital input reference
Pin 19 Digital Common, A/D Converter

The input section has one ground:
Pin 53 Common for digital MUX-inputs and power supply decoupling.

All grounds have to be interconnected externally to the SDM, and it is recommended that all grounds are connected via one track to a single point as close as possible to the SDM. To check that the grounding structure is correct, the ground tracking should be sketched and a grounding "tree" should result whereby all grounds route to a central point.

In general, layout should be such that analog and digital tracks are separated as much as possible with coupling between analog and digital lines minimized by careful layout. For instance, if the lines must cross they should do so at right angles to each other. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

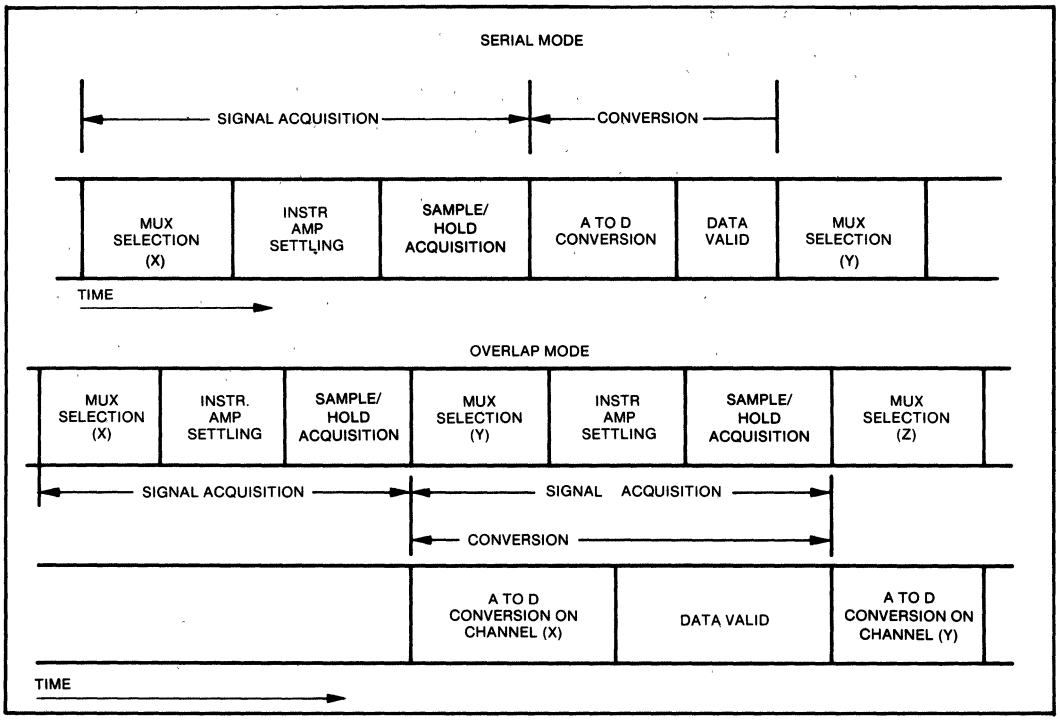


FIGURE 11. Serial and Overlap Modes of Operation.

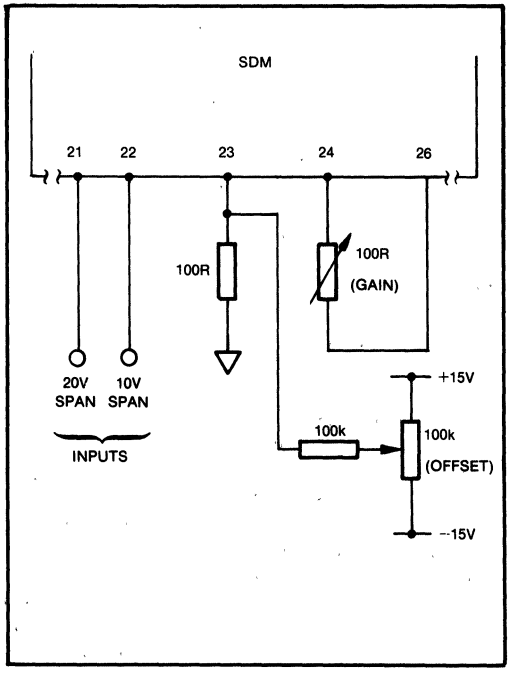


FIGURE 12. Unipolar Calibration.

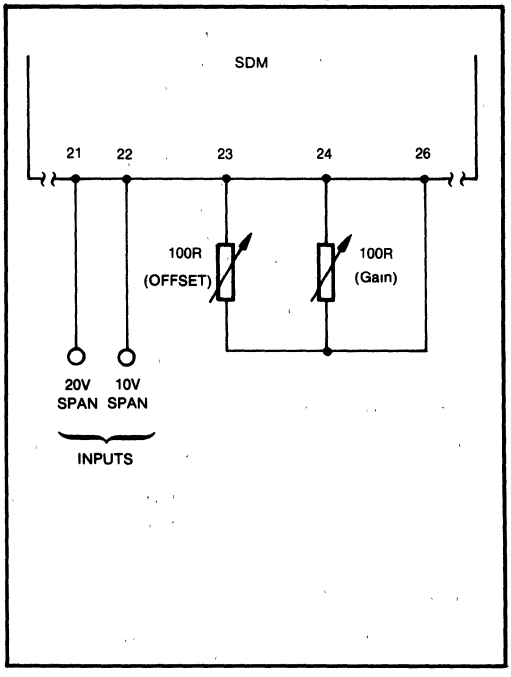


FIGURE 13. Bipolar Calibration.

FULL-SCALE RANGE	000 TO 001 TRANSITION VOLT.	FFE TO FFF TRANSITION VOLT.	1LSB EQUALS
0–10V	+0 0012V	+9 9963V	2 44mV
±5V	−4 9988V	+4 9963V	2 44mV
±10V	−9 9976V	+9 9927V	4 88mV

FIGURE 14. Code Transition Ranges.

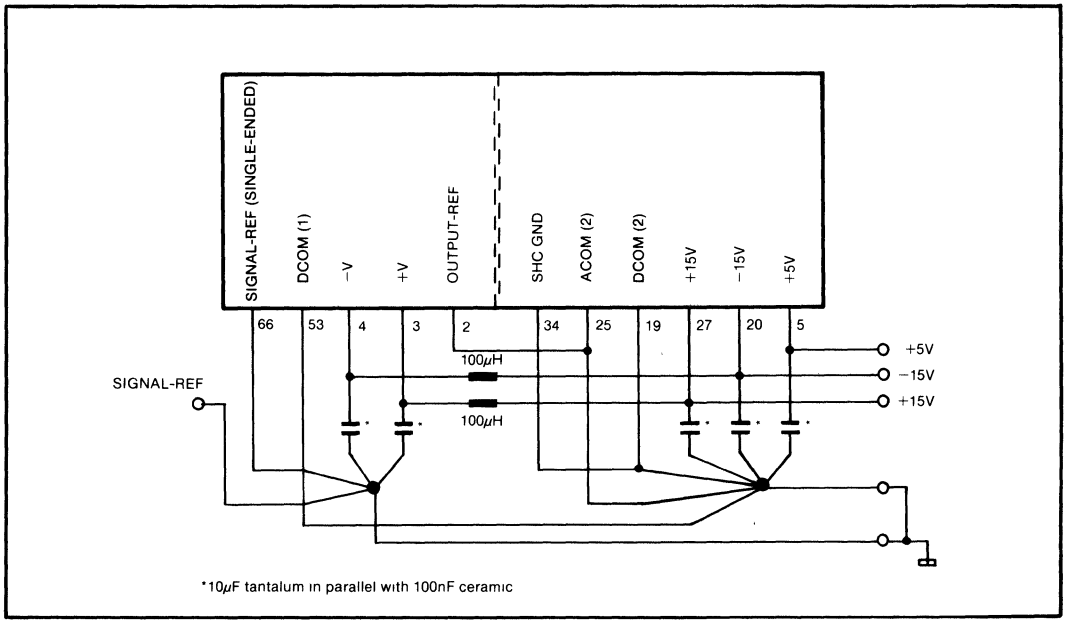


FIGURE 15. Recommended Decoupling of Power Supplies.

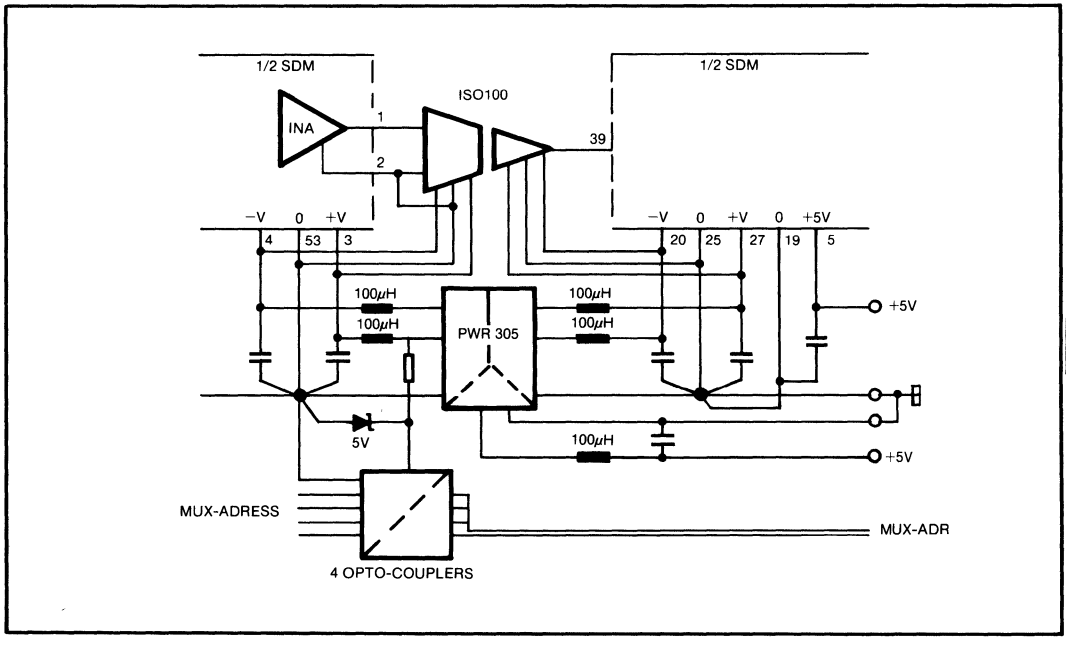


FIGURE 16. Galvanic Isolation Between Analog and Digital Signals.

CONTROLLING THE SDM

The Burr-Brown SDM family can be easily interfaced to most microprocessor systems, as shown in Figures 17-20.

The microprocessor may control each conversion, or the converter may operate in a stand-alone mode controlled only by the R/$\overline{C}$ input.

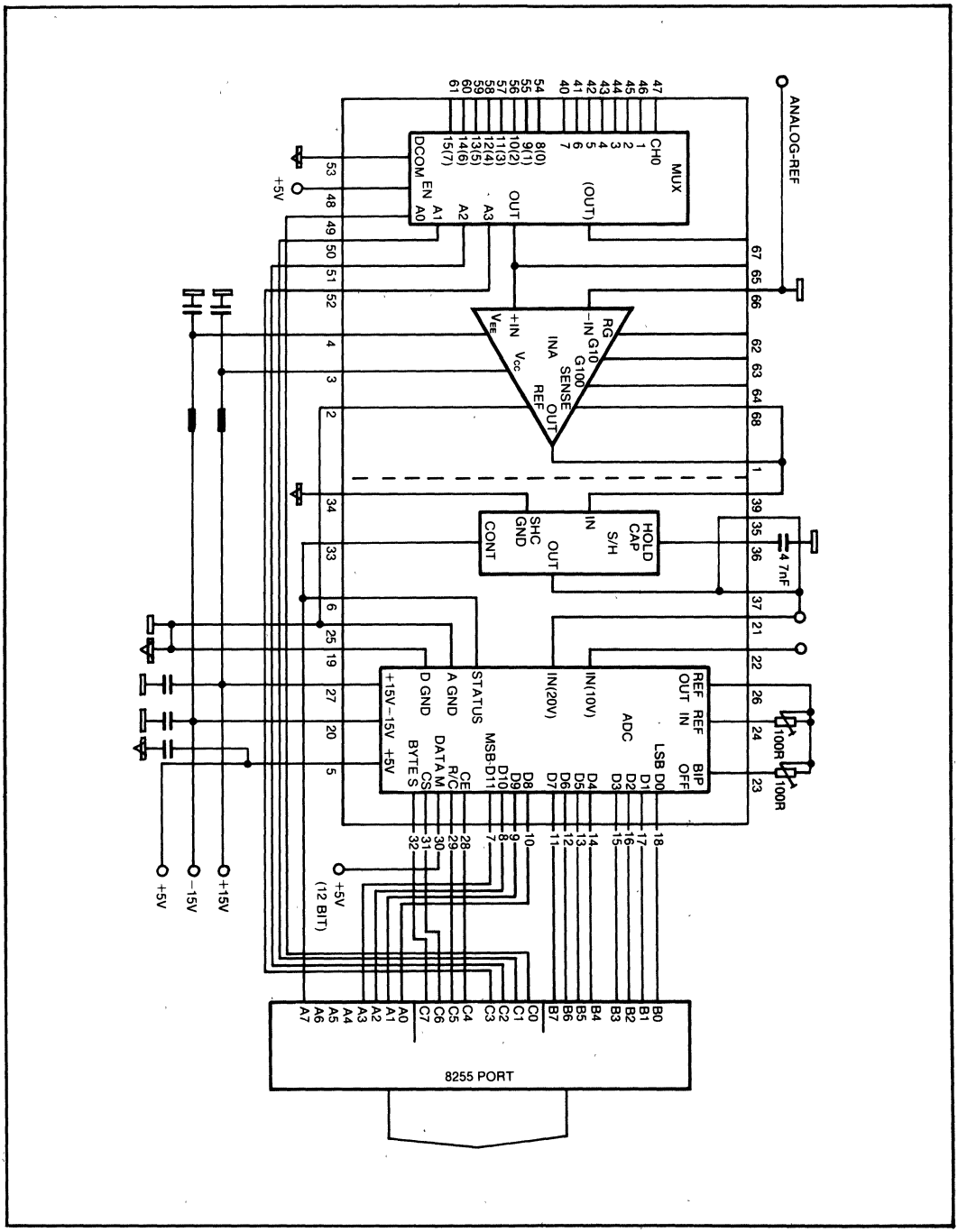


FIGURE 17. The SDM Connected to an Input/Output Port.

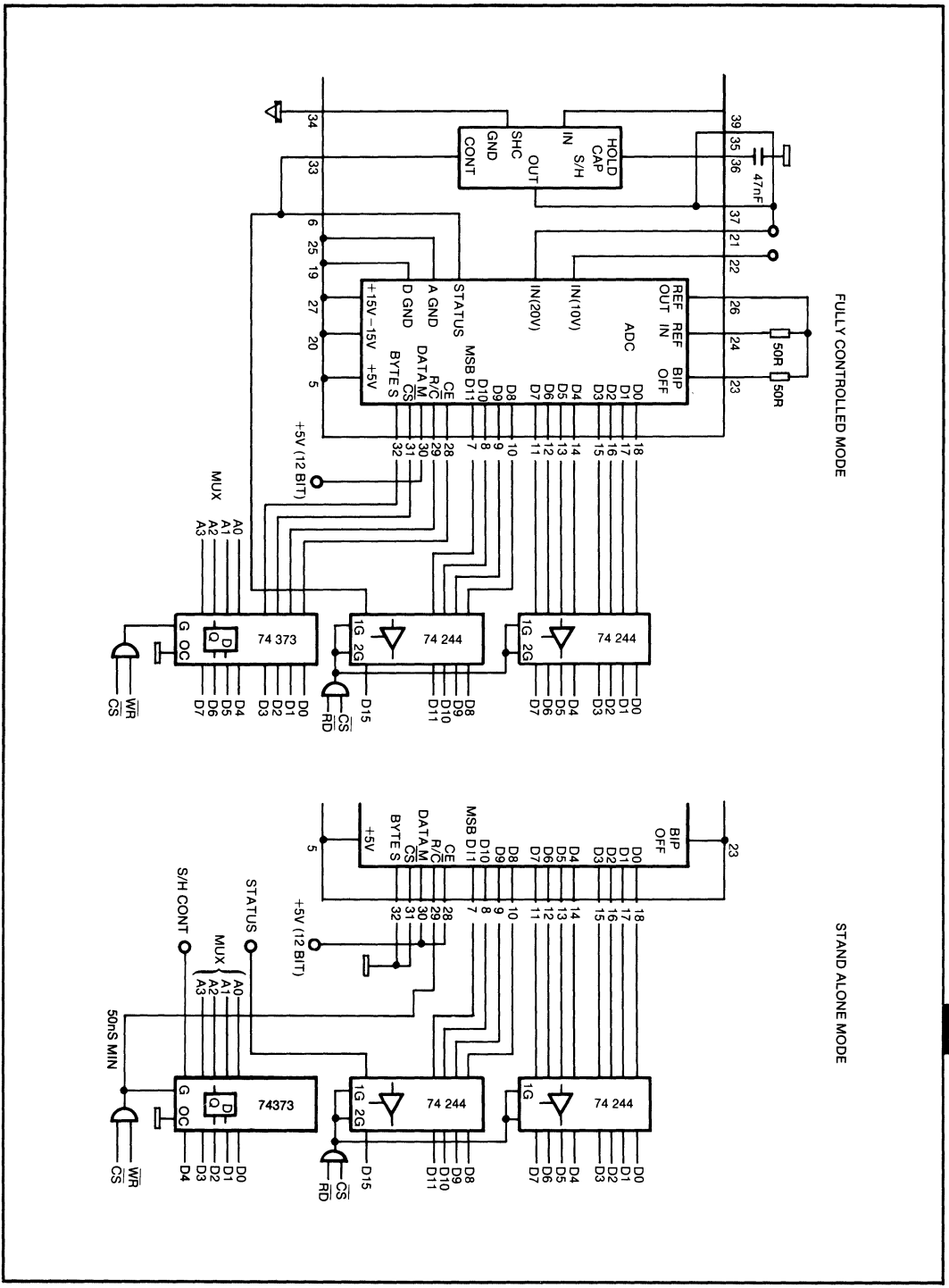


FIGURE 18. The SDM Connected to a 16-Bit-BUS.

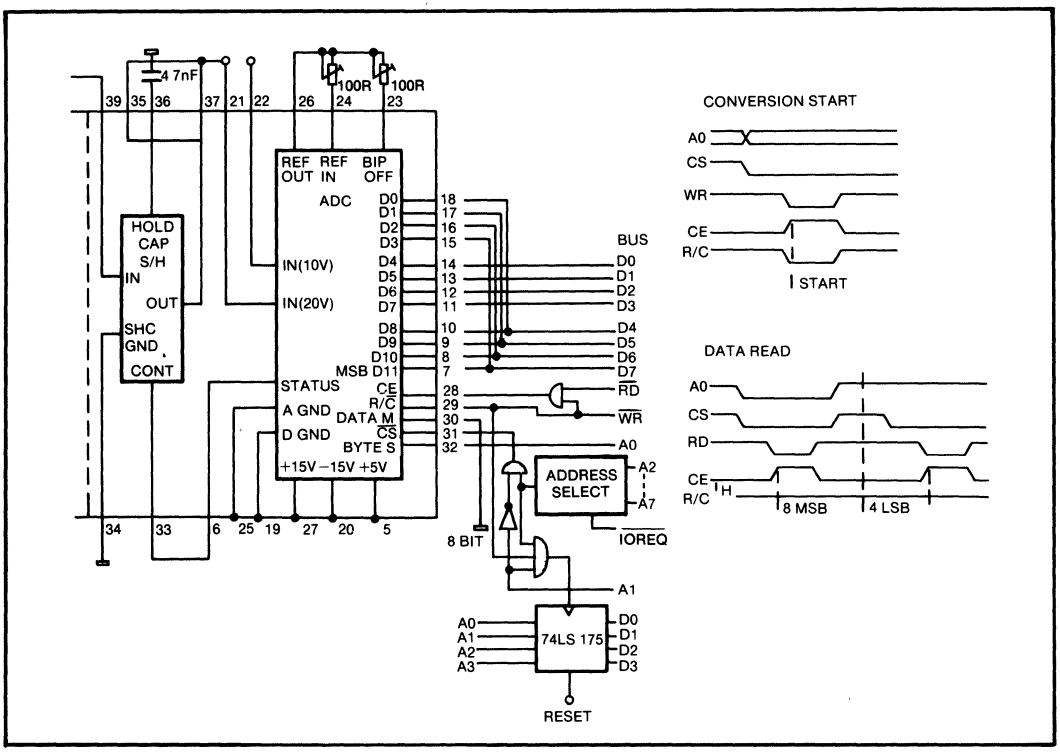


FIGURE 19. SDM on the Z80 BUS.

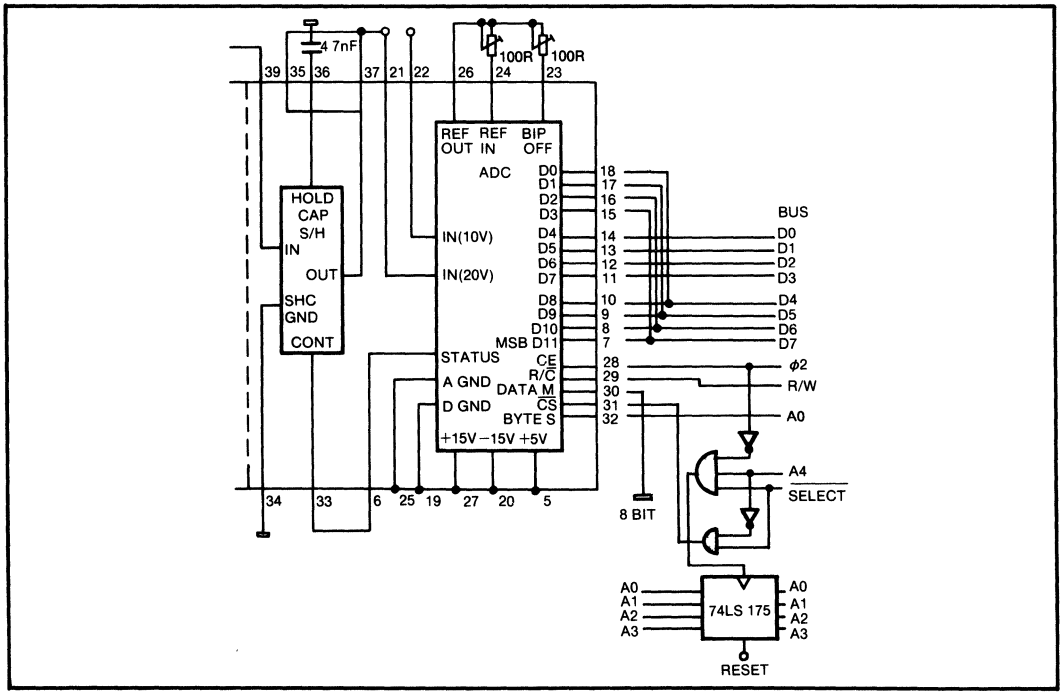


FIGURE 20. SDM on the 6502 BUS.

STAND-ALONE OPERATION

The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and BYTE SELECT are connected to LOW and CE and DATA MODE are connected to HIGH. The output data are presented as 12-bit words.

Conversion is initiated by a High-to-Low transition of R/C. The three-state data output buffers are enabled when R/C is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In each case the R/C pulse must remain low for a minimum of 50ns.

Figure 21 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 22 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the output data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high impedance state until the next occurence of a high R/$\overline{C}$ pulse. Table I lists timing specifications for stand-alone operation.

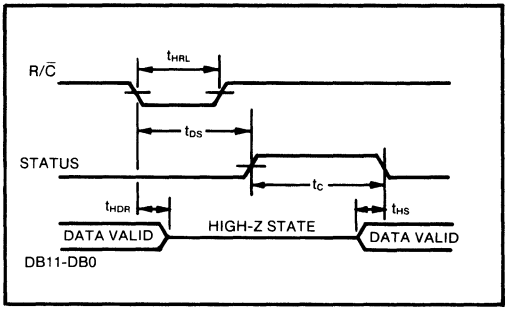


FIGURE 21. R/$\overline{C}$ Pulse Low—Outputs Enabled After Conversion.

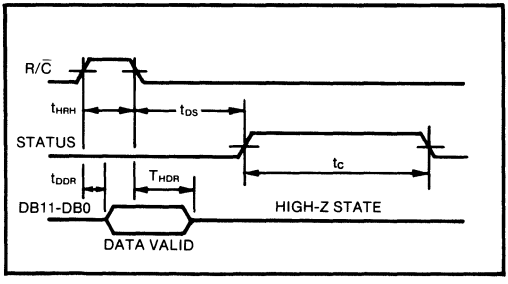


FIGURE 22. R/$\overline{C}$ Pulse High—Outputs Enabled Only Where R/$\overline{C}$ is High.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/C Pulse Width	50			nS
t_{DS}	STS Delay from R/C			200	nS
t_{HDR}	Data Valid After R/C Low	25			nS
t_{HS} 86X	STS Delay After Data Valid	300	500	1000	nS
t_{HS} 87X		100	300	600	nS
t_{HRH}	High R/C Pulse Width	150			nS
t_{DDR}	Data Access Time			150	nS

TABLE I. Stand-Alone Mode Timing.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the BYTE SELECT input, which is latched upon receipt of a conversion start transition. BYTE SELECT is latched because it is also involved in enabling the output buffers. No other control inputs are latched. If BYTE SELECT is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if BYTE SELECT is low. If all 12 bits are read following an 8-bit conversion, the 3LSBs (DB0-DB2) will be low (logic 0) and DB3 will be high (logic 1).

Conversion Start

A conversion is initiated by a transition on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$)—refer to Figure 10. The last of the three to reach the required state start the conversion and thus all three may be dynamically controlled. If necessary, they may change state simultaneously, and the nominal delay time is independent of which input actually starts the conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Conversion Cycle Timing of the Digital Specifications.

The STATUS output indicates the state of the converter by being high only during a conversion. During this time the three-state output buffers remain in a high-impedance state, and therefore, data is not valid. During this period additional transitions of the three control inputs will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if BYTE SELECT changes state after the beginning of conversion, any additional start conversion transition will latch the new state of BYTE SELECT, possibly resulting in an incorrect conversion length (8 bit versus 12 bits) for that conversion.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four conditions are met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. In this condition the data lines are enabled according to the state of the inputs DATA MODE and BYTE SELECT. See Read Cycle Timing for timing relationships and specification.

In most applications the DATA MODE input will be hardwired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When DATA MODE is high, all 12

outputs lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus and the state of the BYTE SELECT is ignored.

When DATA MODE is low, the data is presented in the form of two 8-bit bytes, with selection of each byte by the state of BYTE SELECT during the read cycle.

The BYTE SELECT input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

When BYTE SELECT is low, the byte addressed contains the 8MSBs. When BYTE SELECT is high, the byte addressed contains the 4LSBs from the conversion followed by four zeros that have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 23. The design of the SDM guarantees that the BYTE SELECT input may be toggled at any time without damage to the output buffers occuring.

In the majority of applications, the read operation will be attempted only after the conversion is complete and the status output has gone low. In those situations requiring the fastest possible access to the data, the read may be started as much as (t_{DD} max + t_{HS} max) before STATUS goes low. Refer to Read Cycle Timing for these timing relationships.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
SDM	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 23. 12-Bit Data Format for 8-Bit Systems (connected as Figures 19 and 20).

APPLICATIONS INFORMATION

For the engineer who wishes to evaluate the SDM family, Burr-Brown has designed printed circuit boards on a single 'Eurocard' (shown here for LCC only). These boards enable the design engineer to experiment with various accuracy improvement techniques which are described below. Special consideration has been given to the grounding and circuit layout techniques required when dealing with 12-bit analog signals.

The printed circuit board has been designed so that the solutions to several of the problems likely to be encountered by the user can be examined.

It should not be thought that every user is required to adopt all of the techniques used on the circuit board. In many applications very few external components will be required. However, in following the application guidelines illustrated by the circuitry and accompanying notes, the designer will be able to select and adapt the solutions most suited to their own particular application or problem area.

Provisions for the following are made on the LCC PC board:

— 68 pin LCC socket (Burr-Brown Part No. MC 0068).
— 8 differential or 16 single-ended inputs.
— Input filtering with overvoltage protection for each channel.
— Socket for quad D-type flip-flop 74175 (MUX address latches).
— 7 additional I.C. sockets for easy interfacing to various BUS systems (connection by wire wrap techniques).
— 2 voltage regulators (15 volts).
— LC power supply decoupling.

The Layout pays particular attention to the requirements when operating with precision analog signals. This requires strict separation of the analog and digital areas. Analog and digital commons are totally separated and connected together only at the commons of the supply voltage. All common lines are low resistance and low inductance.

SUPPLY VOLTAGES

In order to avoid coupling between the external supply voltage 15 volt supplies, 2 voltage regulators (78M15, 79L15) are provided on the PC board. The unregulated supply voltage may vary from ±17 volts to ±25 volts.

The MUX/INA section and SHC/ADC section of the SDM have separate supply lines which can be inductively decoupled. This is recommended in order to suppress the high frequency noise which comes from the ADC during conversion.

The power supply rejection of the instrumentation amplifier reduces with increasing frequency. If high frequency noise on the supplies is not decoupled it will be injected into the signal path and cause errors. This effect can be

SDM862/872						SDM863/873				
MUX ADD3	MUX ADD2	MUX ADD1	MUX ADD0	MUX Enable	Channel Selected	MUX ADD2	MUX ADD1	MUX ADD0	MUX Enable	Channel Pair Selected
X	X	X	X	L	NONE	X	X	X	L	NONE
L	L	L	L	H	0	L	L	L	H	0
L	L	L	H	H	1	L	L	H	H	1
L	L	H	L	H	2	L	H	L	H	2
L	L	H	H	H	3	L	H	H	H	3
L	H	L	L	H	4	H	L	L	H	4
L	H	L	H	H	5	H	L	H	H	5
L	H	H	L	H	6	H	H	L	H	6
L	H	H	H	H	7	H	H	H	H	7
H	L	L	L	H	8			—		
H	L	L	H	H	9			—		
H	L	H	L	H	10			—		
H	L	H	H	H	11			—		
H	H	L	L	H	12			—		
H	H	L	H	H	13			—		
H	H	H	L	H	14			—		
H	H	H	H	H	15			—		

FIGURE 24. Channel Select Truth Table.

particularly pronounced when using the 'overlap' mode since the instrumentation amplifier is settling to a new analog value while the ADC is still carrying out the previous conversion.

The digital supply voltage is +5 volts and is also LC-filtered.

All supply lines are bypassed with a 10μF tantalum and a 100nF ceramic capacitor situated **as close as possible** to the package.

If the voltage regulators for the ±15 volts are not used, small inductors for decoupling of the supply voltages are recommended. If inductors are not fitted a dynamic ground loop will be created from supply lines via bypass capacitors to analog common.

INPUT PROTECTION

The multiplexer is protected up to an input voltage which can exceed the supply voltage by a maximum of 20 volts. This means, that with ±15 volts supply voltage, the input voltage can be ±35 volts without damage. This is also the case when the supply voltages are switched off (0 volts). The maximum input voltage can then be ±20 volts. For higher overvoltage protection a series resistor has to be used. The current via the multiplexer should be limited to a maximum of 1mA. For example, a 10kΩ series resistor would give an additional 10 volts overprotection.

For much higher overvoltages (e.g. 100 volts), high value series resistors cannot be used as offset errors would result. In practice, a combination of series resistors and diodes is used. The diodes are connected to ±15 volts and will conduct whenever the input voltage exceeds the ±15 volts supply voltage. The diodes are selected by signal source impedance, as well as filter resistance, as the diode leakage current across the series resistor can cause offset and linearity errors. In this circuit, IN4148 together with 10kΩ are used.

INPUT FILTER

Processor noise can be induced in the analog ground. Input filtering is therefore recommended for analog data aquisition. Such high frequency noise signals can cause dynamic overload of the instrumentation amplifier resulting in non-linear behavior. This leads directly to digitizing errors.

The design of the filter takes into account the characteristics of the SDM and of the signal source.

The following points have to be considered:

— The stray capacitance, output capacitance of the multiplexer and input capacitance of the instrument amplifier (60-80pf) has to be discharged in order to minimize errors caused by 'charge sharing.'

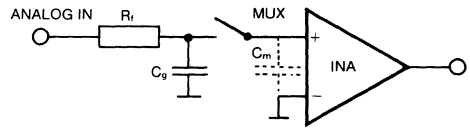
— The series resistor limits the current in the protection diodes, but it also has to be selected for the required filter time constant.

— The noise rejection of the filter has to be >80db in order to satisfy a 12-bit A/D conversion.

As well as considering the above, different calculations have to be carried out for single and differential input signals.

Single-Ended Measurement

R_f limits the maximum input current through the protection diodes. In this case, R_f has been chosen as 10kΩ and together with the capacitor C_g, forms the input filter time constant (C_g = 0.47μF). The time constant must be chosen according to the requirements of the input signal bandwidth and noise rejection. The multiplexer capacitance (C_m) is discharged mainly by C_g. This means C_g has to be sufficiently large compared with C_m or charged via R_f prior to re-sampling of the signal.

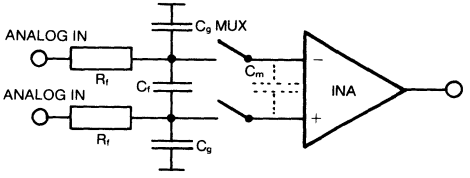


Differential Measurement

Capacitor C_f is used for limiting the input signal frequency. The bandwidth is calculated as follows:

$$F_g = \frac{1}{4\pi R_f C_f} \qquad \text{IF } C_f >> C_g$$

When selecting the value of C_f, it should be noted that C_m has to be discharged when switching the multiplexer channels. This means that the voltage error of C_f (induced by 'charge sharing' with C_m) has to be smaller than 1LSB. Therefore, C_f should have a minimum value of a 0.47μF. The resistors R_f, together with the source impedance have to be sufficiently small in order to recharge C_f prior to signal sampling. This prevents errors in the signal value caused by the charge stored on C_m by the previously selected channel.



The 2 capacitors C_g form together with R_f a common-mode filter. This filter greatly improves accuracy in a noisy environment (decrease of common-mode rejection of instrumentation amplifier with increasing frequency). For good filter operation, both time constants R_f. C_g should match each other within 2%. Additional errors will be induced by a mismatch.

Selected values are: $C_f = 0.47\mu F$, $C_g = 10nF$, $R_f = 10k\Omega$. The filter reduces the signal slew rate so that the instrumentation amplifier can follow the voltage variation of the signal with the noise component eliminated.

In general, all measurements which require more than a gain of 10 should be done in differential mode. Single ended measurements should be limited to applications where current sources are measured via shunts or where signal voltages in the range of some volts are available.

Bus-Interface

As the outputs of the SDM are BUS compatible, only a few I.C.s are necessary to interface to various BUS systems. For such interfacing, 4 off 14-pin and 3 off 16-pin I.C. sockets are provided. Wiring is by wire wrap to the BUS connector.

Setting of Various Modes

Circuit board positions are provided for the connection of 'jumpers' as follows:

J1, J2—ADC analog input voltage settings.
J3—Set for differential (SDM8X3) or single ended (SMD8X2) operation.
J4—Instrumentation amplifier gain settings.

(a) 16 input channels, single ended:
—Use SDM8X2
—Consider single-ended filtering
—Connect J3 (pin 66) to common

(b) Differential inputs
—Use SDM8X3
—Consider differential filtering
—Connect J3 (pin 66) to pin 67

(c) Analog input

±10 volts	Connect J1 to pin 21
	Connect J2 to pot P2 (100Ω)
±5 volts	Connect J1 to pin 22
	Connect J2 to pot P2 (100Ω)
0 to +10 volts:	Connect J1 to pin 22
	Connect J2 to junction of R_1/R_2

(d) Gain of instrumentation amplifier

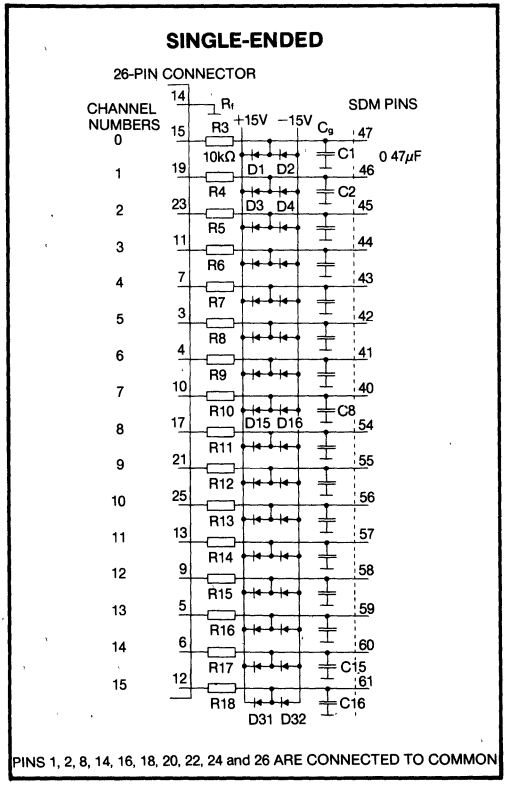
G = 1	Jumper J4 open
G = 10	Jumper J4 to pin 63
G = 100	Jumper J4 to pin 64

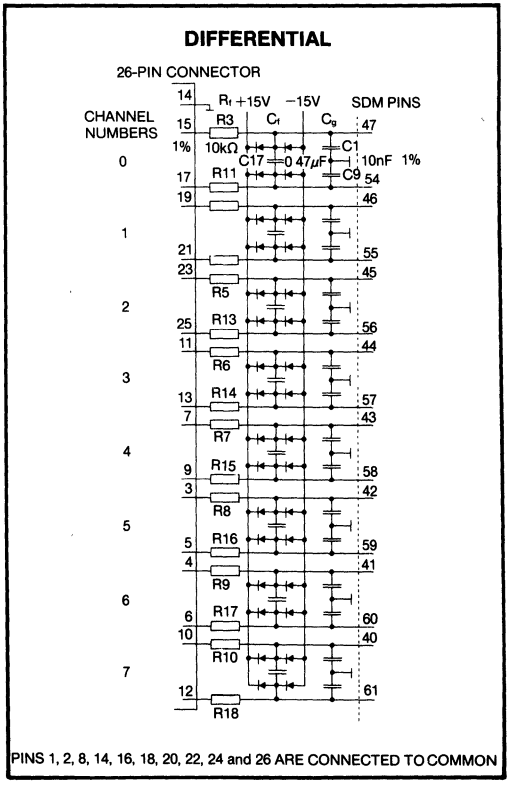
Other gains: use additional resistor between pin 62 and pin 63

Gain equation: $R_g = \frac{40k\Omega}{G-1} - 4.444k\Omega$

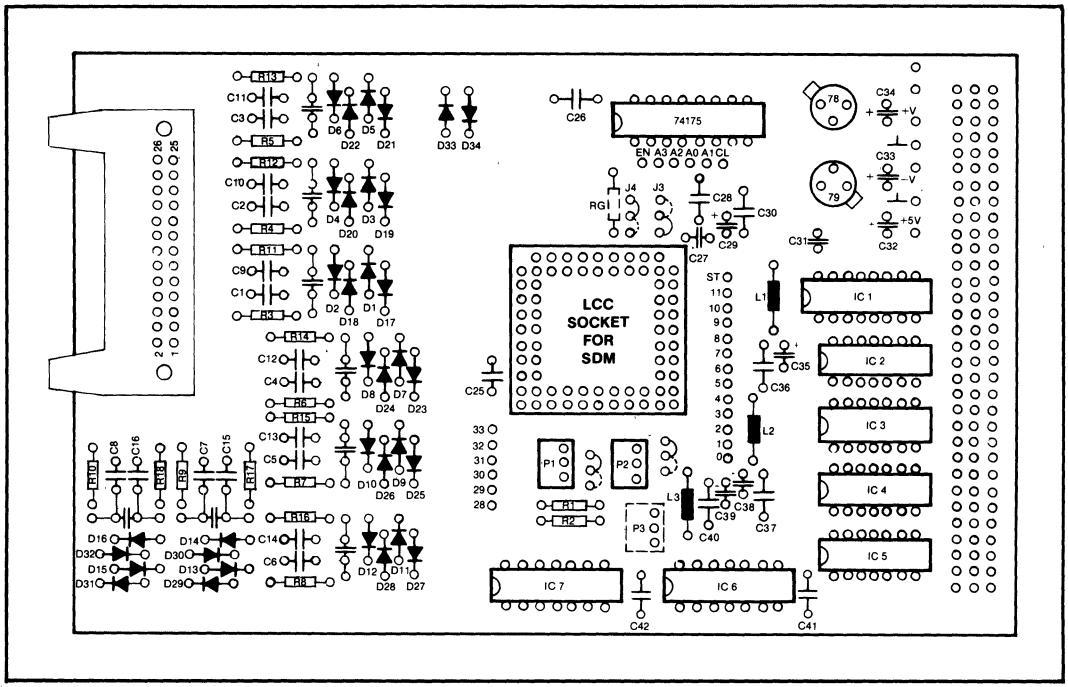
Low tempco is recommended in order to minimize gain drift.

INPUT FILTER AND PROTECTION CIRCUITRY

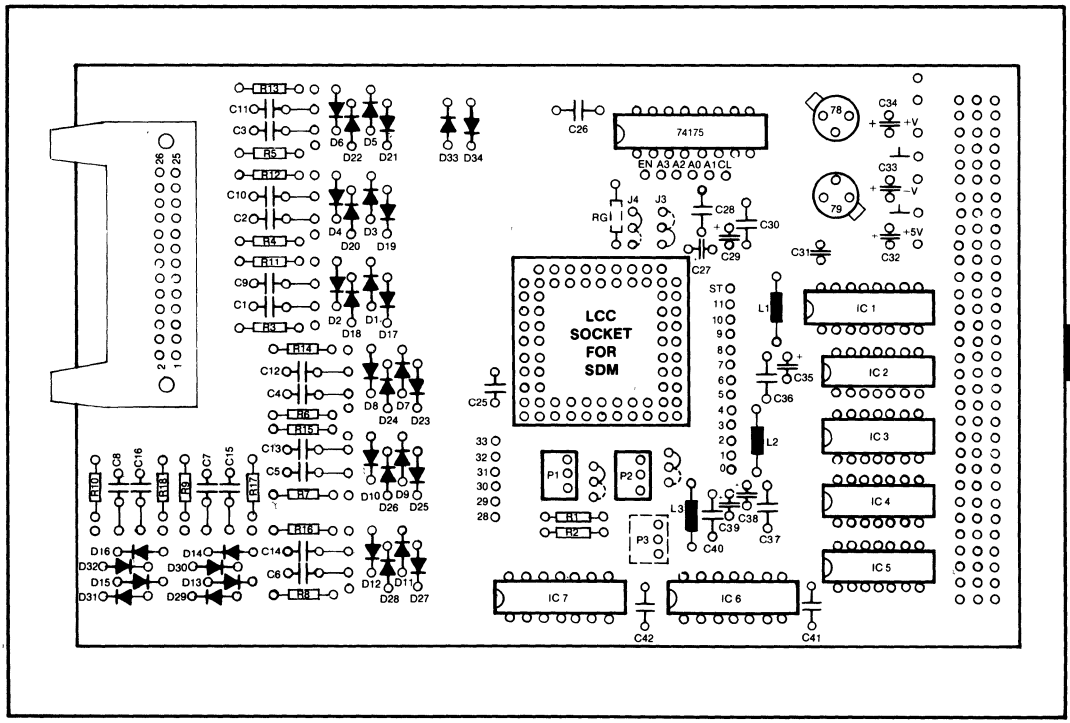




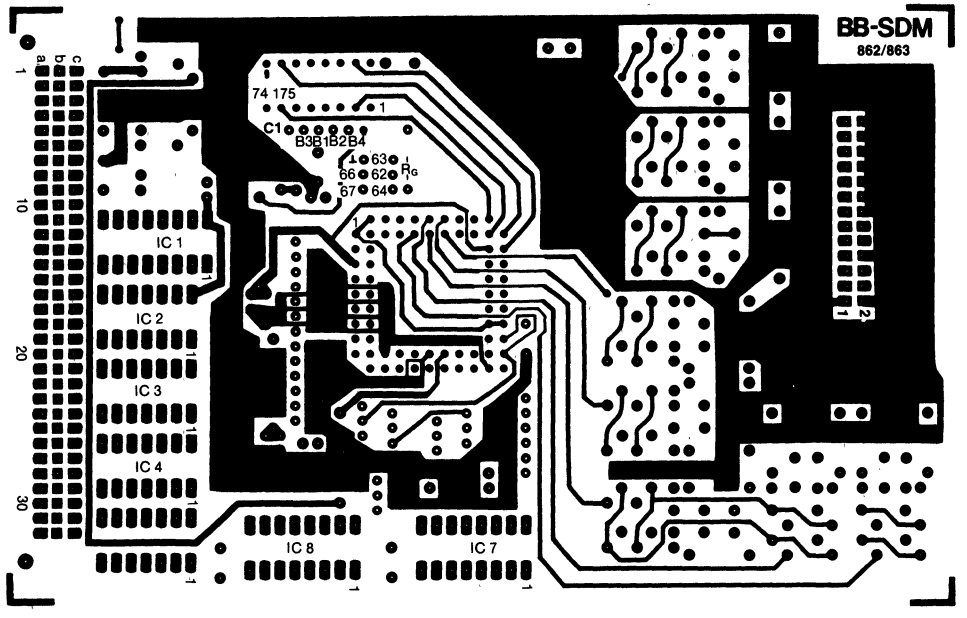
P.C.B. COMPONENT LAYOUT FOR DIFFERENTIAL OPERATION



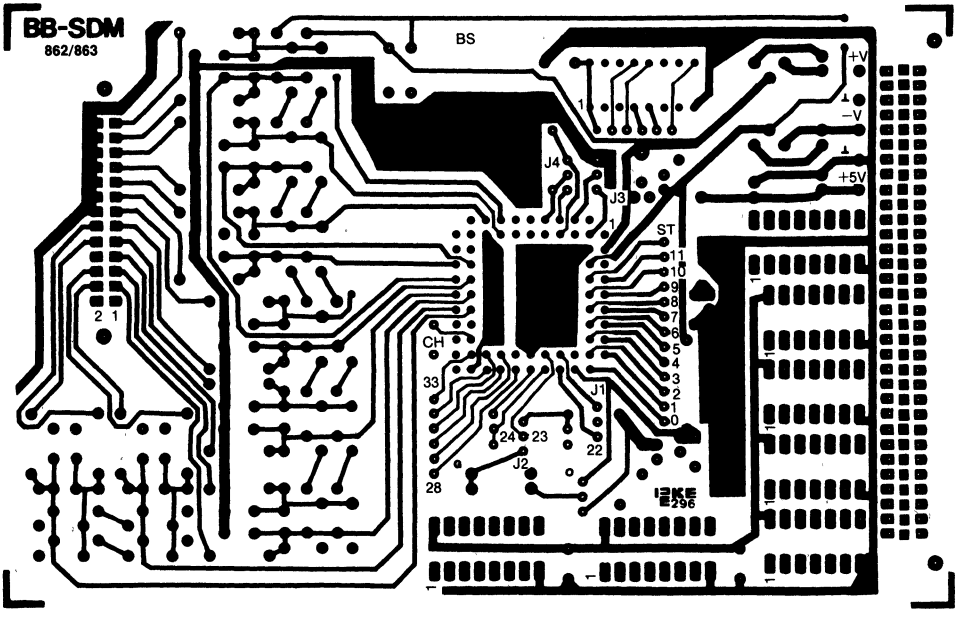
P.C.B. COMPONENT LAYOUT FOR SINGLE-ENDED OPERATION



P.C.B. LAYOUT

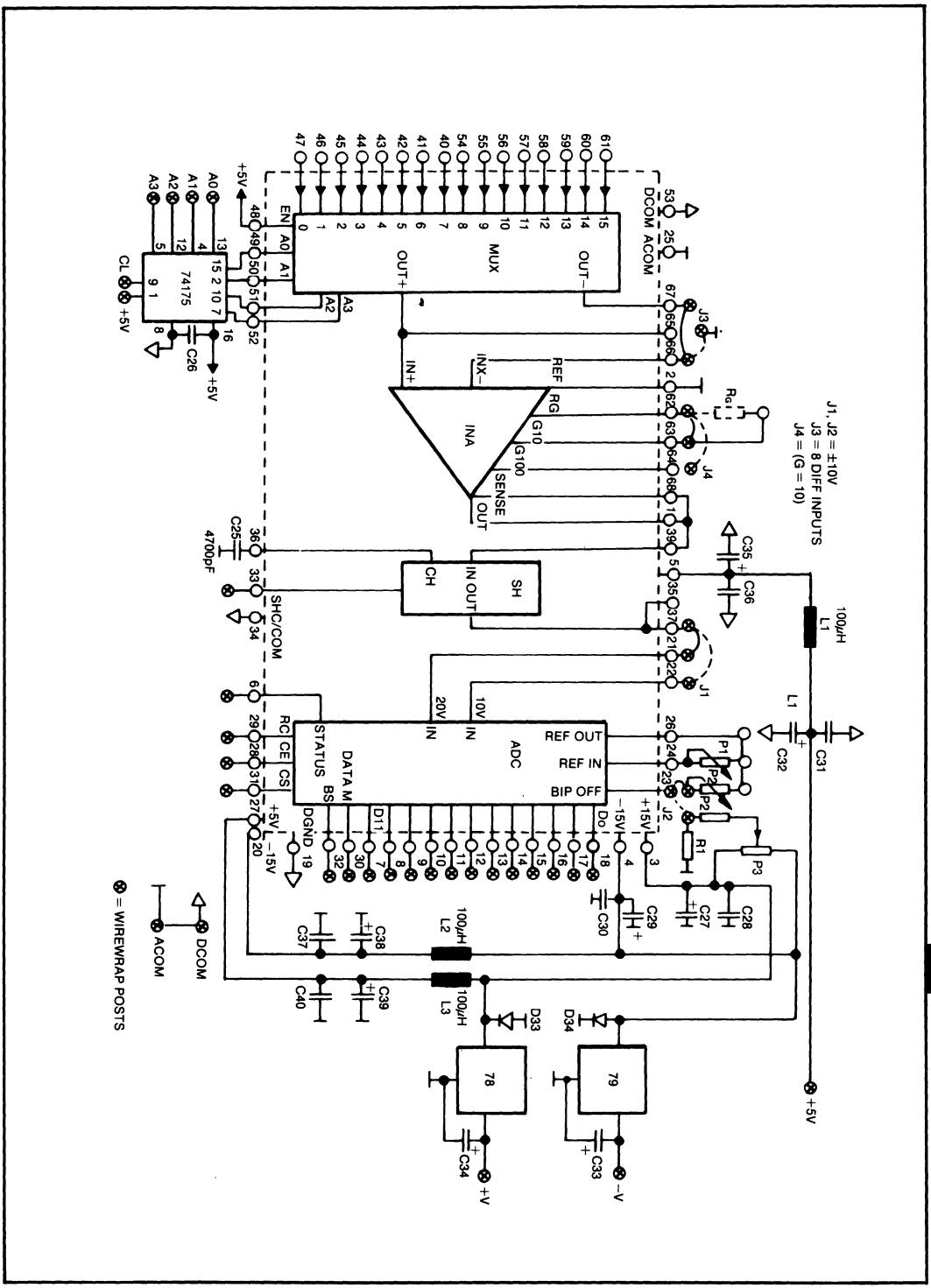


NOTE NOT SUITABLE FOR PGA PACKAGE

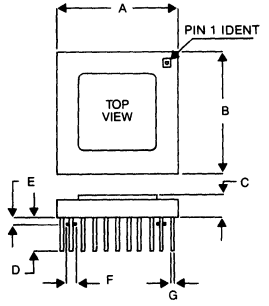


NOTE NOT SUITABLE FOR PGA PACKAGE

CIRCUIT DIAGRAM—SDM P.C. BOARD



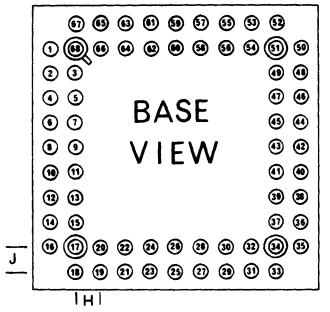
P.G.A. MECHANICAL OUTLINE



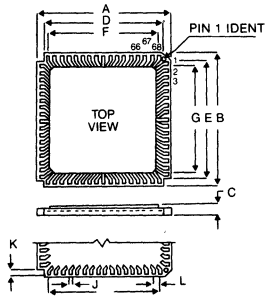
H PACKAGE

Terminations: Gold plated KOVAR
Case: Black ceramic with gold plated nickel lid
Hermeticity: Gross leak test
Weight: 9 grms (0.32oz)

DIM	INCHES MIN	INCHES MAX	MILLIMETRES MIN	MILLIMETRES MAX
A	1 087	1 109	27 610	28 169
B	1 087	1 109	27 610	28 169
C	095	120	2 413	3 048
D	162	198	4 115	5 029
E	045	055	1 143	1 397
F	045	055	1 143	1 397
G	016	020	406	508
H	100 BASIC		2 540 BASIC	
J	100 BASIC		2 540 BASIC	



L.C.C. MECHANICAL OUTLINE



Terminations: Gold plated nickel on refractory metallization
Case: Ceramic with gold plated nickel lid
Hermeticity: Gross leak test.
Weight: 4.2 grams (0 15oz)

DIM	INCHES MIN	INCHES MAX	MILLIMETRES MIN	MILLIMETRES MAX
A	945	965	24 003	24 511
B	945	965	24 003	24 511
C	076	094	1 934	2 388
D	841	859	21 361	21 819
E	841	859	21 361	21 819
F	755	785	19 177	19 939
G	755	785	19 177	19 939
H	800 BASIC		20 320 BASIC	
J	027	033	686	838
K	045 BASIC		1 143 BASIC	
L	050 BASIC		1 270 BASIC	

P.C.B. COMPONENTS PARTS LIST

R1		100kΩ	C26	10nF Ceramic	P3		100kΩ **0–10 volts range only**
R2		100Ω For 0–10 Volts settling	C27, C29, C35	10μF Tantalum (Decoupling)	L1	L3	100μH (Decoupling)
R3	R18	10kΩ 1%	C32, C38, C39		D1	D32	1N4148 (Input Protection Diodes)
C1	C16	0 47μF—Single ended input mode	C28, C30, C31	100nF Ceramic (Decoupling)	D33, D34		1N4007
		10nF 1%—Differential input mode	C36, C37, C40		78		MC78M15CG
C17	C24	0 47μF—Differential input mode	C33, C34	0 33μF Tantalum	79		MC79L15CG
C25		4 700pF (Polypropylene, Polystyrene or Teflon™)	P1	100Ω	**74175**		74LS175
			P2	100Ω **±5 volts, ±10 volts range only**	LCC Socket		MC0068

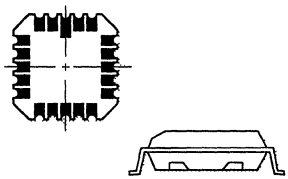
UNLESS OTHERWISE MARKED—RESISTORS ARE 1/4W, 5%, CAPACITORS ARE 10%

ORDERING INFORMATION[1]

Model	Input	LCC, PGA Pkg.	Accuracy [% FSR]	Throughput	Temp. Range [°C]	Model	Input	LCC, PGA Pkg.	Accuracy [% FSR]	Throughput	Temp. Range [°C]
SDM862J[2]	16SE	L, H	±0.024	33kHz	0 to +70	SDM863J	8DIF	L, H	±0.024	33kHz	0 to +70
SDM862K	16SE	L, H	±0.012	33kHz	0 to +70	SDM863K	8DIF	L, H	±0.012	33kHz	0 to +70
SDM862A	16SE	L, H	±0.024	33kHz	−25 to +85	SDM863A	8DIF	L, H	±0 024	33kHz	−25 to +85
SDM862B	16SE	L, H	±0.012	33kHz	−25 to +85	SDM863B	8DIF	L, H	±0 012	33kHz	−25 to +85
SDM862R	16SE	L, H	±0.024	33kHz	−55 to +125	SDM863R	8DIF	L, H	±0 024	33kHz	−55 to +125
SDM862S	16SE	L, H	±0 012	33kHz	−55 to +125	SDM863S	8DIF	L, H	±0 012	33kHz	−55 to +125
SDM872J	16SE	L, H	±0 024	50kHz	0 to +70	SDM873J	8DIF	L, H	±0.024	50kHz	0 to +70
SDM872K	16SE	L, H	±0.012	50kHz	0 to +70	SDM873K	8DIF	L, H	±0.012	50kHz	0 to +70
SDM872A	16SE	L, H	±0 024	50kHz	−25 to +85	SDM873A	8DIF	L, H	±0.024	50kHz	−25 to +85
SDM872B	16SE	L, H	±0 012	50kHz	−25 to +85	SDM873B	8DIF	L, H	±0.012	50kHz	−25 to +85
SDM872R	16SE	L, H	±0 024	50kHz	−55 to +125	SDM873R	8DIF	L, H	±0.024	50kHz	−55 to +125
SDM872S	16SE	L, H	±0 012	50kHz	−55 to +125	SDM873S	8DIF	L, H	±0 012	50kHz	−55 to +125

NOTES (1) LCC Evaluation Board Part Number: PC862/863-1 PGA Evaluation Board Part Number: PC862/863-2 (2) 16 single-ended inputs, LCC package, with accuracy of 0.024% FSR, Temp Range of 0°C to 70°C and throughput of 33kHz = SDM862JL

Teflon™ E.I. du Pont de Nemours & Co.



SURFACE MOUNT COMPONENTS

Burr-Brown offers a wide variety of integrated circuit types in surface mount packages. These packages permit denser layouts on one or both sides of a PC board, often saving 50% or more of the space normally required for these functions. Many of these miniature devices also fit inside transducer cavities and may be used in modules or hybrid circuits. Burr-Brown concentrates primarily on two package types with a variety of sizes and number of leads:

SOIC

Plastic small-outline package with gull-wing leads on 1.27mm centers. For example, the SOIC-8 has 8 leads.

LCC

Ceramic leadless chip carrier with terminals on 1.27mm centers. For example, the LCC-20 has 20 terminals.

STAY UP TO DATE

Burr-Brown is continuously adding to its offering of products available in surface mount packages. Contact your local Burr-Brown salesperson or representative. See the inside back cover of this Data Book.

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SMALL-OUTLINE IC PACKAGES

Model	Device Type	Description	Package
DAC703JU/KU	Digital-to-Analog Converter	16-Bit, V_{OUT}	SOIC-24
DAC811JU/KU	Digital-to-Analog Converter	12-Bit, µp-Compatible	SOIC-28
DAC7541AJU/AKU	Digital-to-Analog Converter	12-Bit, CMOS	SOIC-18
DAC7545JU/KU	Digital-to-Analog Converter	12-Bit, CMOS, Buffered	SOIC-20
DAC8012KU	Digital-to-Analog Converter	12-Bit, CMOS, Latched	SOIC-20
INA101KU	Instrumentation Amplifier	Precision, Monolithic	SOIC-16
INA102KU	Instrumentation Amplifier	Low Power	SOIC-16
INA105KU	Instrumentation Amplifier	Unity Gain, Differential	SOIC-8
INA110KU	Instrumentation Amplifier	Fast, FET Input	SOIC-16
MPY634KU	Precision Analog Multiplier	Wide Bandwidth	SOIC-16
OPA27/37GU	Operational Amplifier	Ultra-Low Noise	SOIC-8
OPA121KU	Operational Amplifier	Low Cost, ***Difet*** ®	SOIC-8
OPA404KU	Operational Amplifier	Quad, High-Speed, Precision ***Difet***	SOIC-16
OPA602AU	Operational Amplifier	High-Speed, Precision ***Difet***	SOIC-8
PCM55HP/JP	Digital-to-Analog Converter	16-Bit, Digital Audio	SOIC-24
SHC298JU	Sample/Hold Amplifier	Low Cost, Monolithic	SOIC-8
VFC32KU	V-to-F and F-to-V Converter	Low Cost, Monolithic	SOIC-14
XTR101AU	Current Transmitter/Converter	Two-Wire, 4-20mA	SOIC-16
XTR110KU	Current Transmitter/Converter	Voltage-to-Current Converter	SOIC-16

NOTE: Electrical and mechanical specifications for SOIC parts are contained in the Product Data Sheets in this Data Book. Use the Model Index on the inside front cover.

Difet ® Burr-Brown Corp.

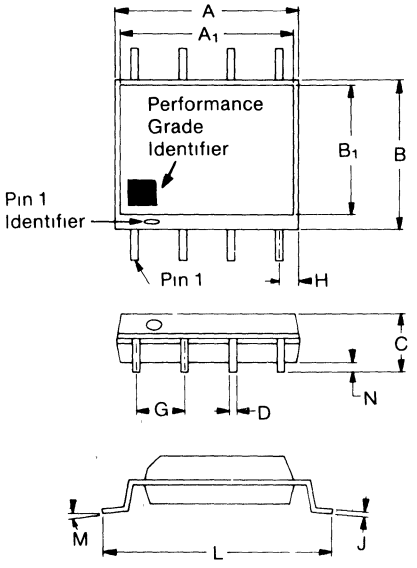
LEADLESS CHIP CARRIER PACKAGES

Model	Device Type	Description	Package
4213L	Analog Multiplier/Divider	Precision	LCC-20
AD515L	Operational Amplifier	Electrometer	LCC-20
DAC700-703BL	Digital-to-Analog Converter	16-Bit, Monolithic	LCC-28
DAC703L	Digital-to-Analog Converter	16-Bit Monolithic, Military	LCC-28
DAC811L	Digital-to-Analog Converter	12-Bit, µP-Compatible	LCC-28
DAC850L	Digital-to-Analog Converter	12-Bit, Monolithic	LCC-28
DAC851L	Digital-to-Analog Converter	12-Bit, MIL Temp	LCC-28
DAC870L	Digital-to-Analog Converter	12-Bit, Military	LCC-28
INA101L	Instrumentation Amplifier	Precision, Monolithic	LCC-20
INA102L	Instrumentation Amplifier	Low Power	LCC-20
INA105L	Instrumentation Amplifier	Unity Gain, Differential	LCC-20
INA110L	Instrumentation Amplifier	Fast, FET Input	LCC-20
INA258L	Instrumentation Amplifier	Precision, Military	LCC-20
MPY100L	Analog Multiplier/Divider	Low Cost	LCC-20
MPY534L	Precision Analog Multiplier	Low Cost, Monolithic	LCC-20
MPY634L	Precision Analog Multiplier	Wide Bandwidth	LCC-20
OPA27/37L	Operational Amplifier	Ultra-Low Noise	LCC-20
OPA111L	Operational Amplifier	Precision, ***Difet***	LCC-20
OPA121L	Operational Amplifier	Low Cost, ***Difet***	LCC-20
OPA128L	Operational Amplifier	Electrometer Grade	LCC-20
OPA404L	Operational Amplifier	High Speed, Quad	LCC-20
OPA2111L	Operational Amplifier	Precision, Dual	LCC-20
REF10L	Precision Voltage Reference	Ultra-Stable	LCC-20
REF101L	Precision Voltage Reference	Low Drift	LCC-20
SDM862/863L	Data Acquisition System	12-Bit, 16-Channel, 33kHz Throughput	LCC-68
SDM872/873L	Data Acquisition System	12-Bit, 16-Channel, 50kHz Throughput	LCC-68
VFC32L	V-to-F and F-to-V Converter	Low Cost, Monolithic	LCC-20
VFC62L	V-to-F and F-to-V Converter	Precision, Monolithic	LCC-20
VFC100L	V-to-F and F-to-V Converter	Synchronized	LCC-20
VFC101JN/KN	V-to-F and F-to-V Converter	Synchronized, Multiple Input	PLCC-20
VFC320L	V-to-F and F-to-V Converter	Precision, Monolithic	LCC-20
XTR101L	Current Transmitter/Converter	Two-Wire, 4-20mA	LCC-20
XTR110L	Current Transmitter/Converter	Voltage-to-Current Converter	LCC-20

NOTE: Electrical and mechanical specifications for LCC parts are contained in separate Product Data Sheets. To obtain copies, contact your local Burr-Brown salesperson or representative. See the inside back cover for a listing of sales offices.

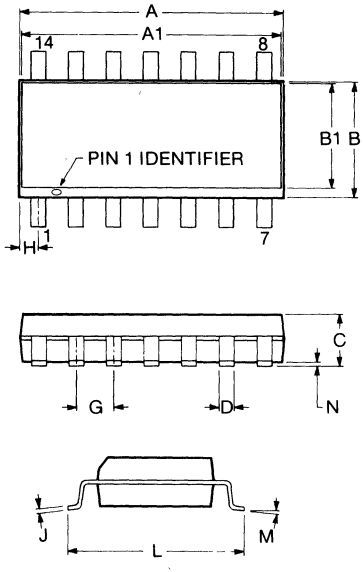
SURFACE MOUNT PACKAGE OUTLINES AND DIMENSIONS

Plastic SOIC-8 Package



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	185	201	4 70	5 11
A_1	178	201	4 52	5 11
B	146	162	3 71	4 11
B_1	130	149	3 30	3 78
C	054	145	1 37	3 69
D	015	019	0 38	0 48
G	050 BASIC		1 27 BASIC	
H	018	026	0 46	0 66
J	008	012	0 20	0 30
L	220	252	5 59	6 40
M	0°	10°	0°	10°
N	000	012	0 00	0 30

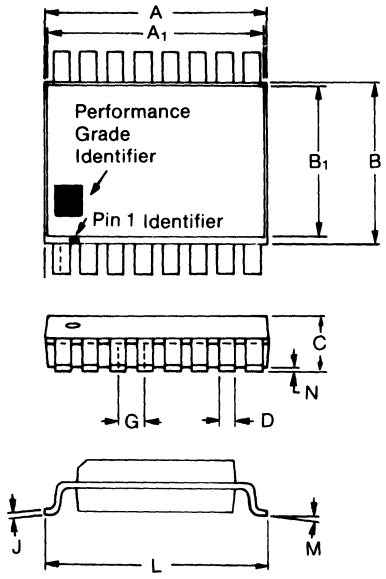
Plastic SOIC-14 Package



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	332	348	8 44	8 84
A1	325	348	8 26	8 84
B	146	162	3 71	4 11
B1	128	146	3 25	3 71
C	052	068	1.32	1 73
D	014	019	0 36	0 48
G	050 BASIC		1 27 BASIC	
H	016	024	0 41	0 61
J	008	012	0 20	0 30
L	226	246	5 74	6 25
M	5° TYP		5° TYP	
N	000	012	0 00	0 30

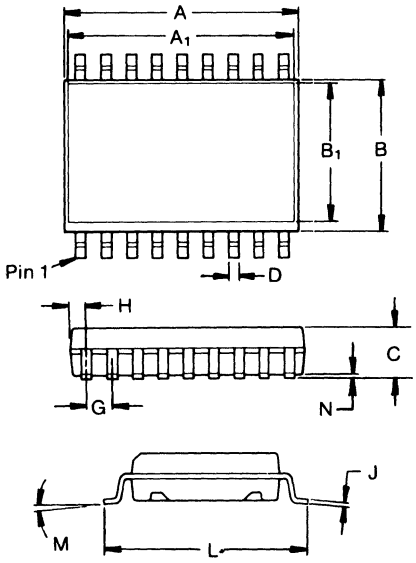
NOTES: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

Plastic SOIC-16 Package



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.400	416	10 16	10.57
A_1	.388	.412	9.86	10.46
B	286	302	7 26	7.67
B_1	.268	286	6.81	7.26
C	093	109	2.36	2.77
D	.015	.020	0.38	0.51
G	.050 BASIC		1 27 BASIC	
H	.022	038	0.56	0.97
J	008	012	0.20	0.30
L	391	421	9.93	10 69
M	5° TYP		5° TYP	
N	000	012	0.00	0.30

Plastic SOIC-18 Package

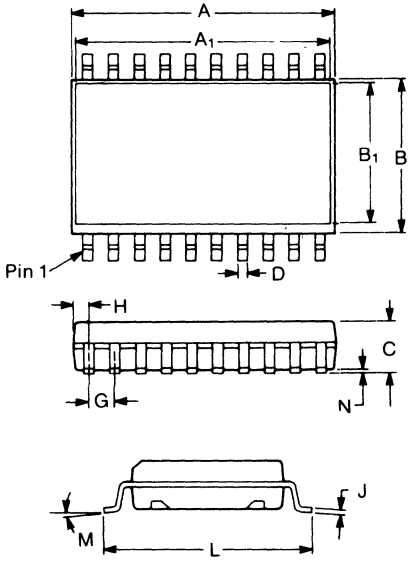


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	450	.466	11 43	11.84
A_1	443	.466	11.25	11.84
B	286	.302	7 26	7.67
B_1	.270	.285	6.86	7.24
C	.093	108	2.36	2.74
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	026	.034	0.66	0.86
J	008	.012	0.20	0.30
L	.390	.422	9.91	10.72
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

NOTES: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

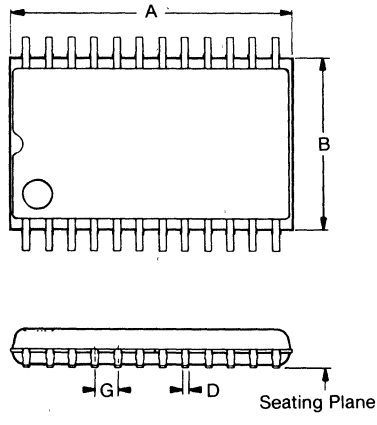
SURFACE MOUNT PACKAGE OUTLINES AND DIMENSIONS

Plastic SOIC-20 Package



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	502	518	12.75	13 16
A_1	495	.518	12.57	13 16
B	286	302	7 26	7 67
B_1	270	285	6 86	7 24
C	093	108	2.36	2 74
D	015	.019	0 38	0.48
G	050 BASIC		1.27 BASIC	
H	.026	034	0.66	0 86
J	.008	.012	0 20	0.30
L	390	.422	9.91	10 72
M	0°	10°	0°	10°
N	000	.012	0 00	0.30

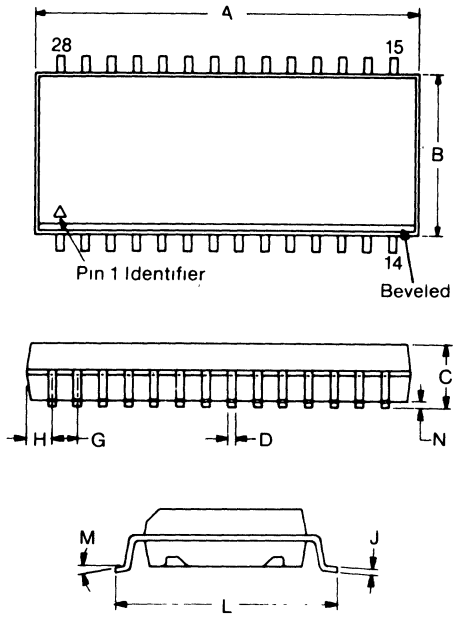
Plastic SOIC-24 Package



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	614	630	15 60	16 00
B	346	362	8 80	9 20
C	—	098	—	2 50
D	012	020	0 30	0 50
G	046	054	1 17	1 37

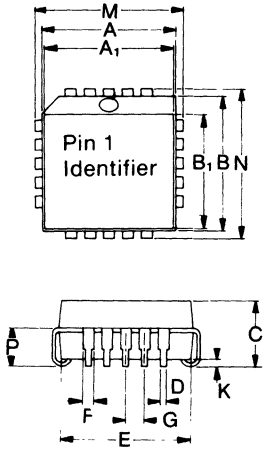
NOTES: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

Plastic SOIC-28 Package



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	700	716	17 78	18 19
B	286	302	7 26	7.67
C	093	109	2 36	2.77
D	016 BASIC		0 41 BASIC	
G	050 BASIC		1 27 BASIC	
H	022	038	0 56	0 97
J	008	012	0 20	0 30
L	398	414	10 11	10 52
M	5° TYP		5° TYP	
N	000	012	0 00	0 30

Plastic PLCC-20 Package

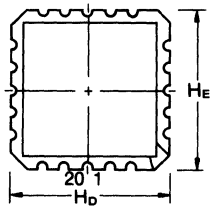


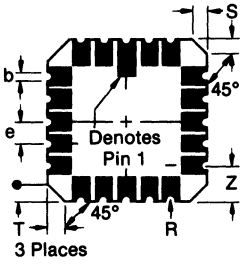
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	350	356	8 89	9 04
A_1	338	.344	8 59	8 74
B	350	356	8 89	9 04
B_1	.290	330	7 37	8.38
C	165	180	4 19	4 57
D	013	.021	0 33	0 53
E	290	330	7 37	8 38
F	026	032	0 66	0.81
G	.050 BASIC		1 27 BASIC	
K	.020	—	0 51	—
M	385	.395	9 78	10 03
N	.385	.395	9.78	10.03
P	.090	120	2.29	3 05

NOTES: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

SURFACE MOUNT PACKAGE OUTLINES AND DIMENSIONS

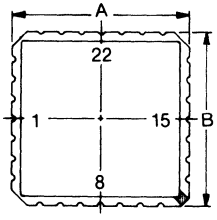
Ceramic LCC-20 Package

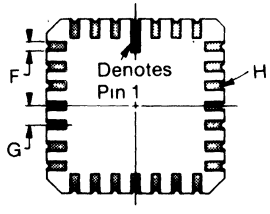


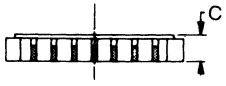


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
H_D	.345	.360	8.76	9.14
H_E	.345	.360	8.76	9 14
A_2	.064	.100	1.63	2.54
b	.022	.028	0.56	0.71
e	.050 BASIC		1.27 BASIC	
R	.008R TYP		0.20R TYP	
S	.020 TYP		0.508 TYP	
T	040 TYP		1.016 TYP	
Z	.075 TYP		1.91 TYP	

Ceramic LCC-28 Package



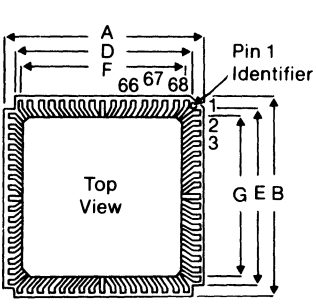


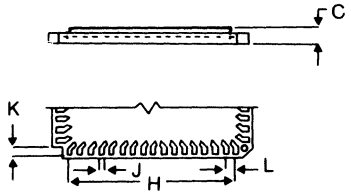


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	442	458	11 23	11 63
B	442	458	11 23	11.63
C	064	100	1.63	2.54
F	.022	.028	0.56	0 71
G	050 BASIC		1 27 BASIC	
H	008 R TYP		0 20 R TYP	

NOTES: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

Ceramic LCC-68 Package

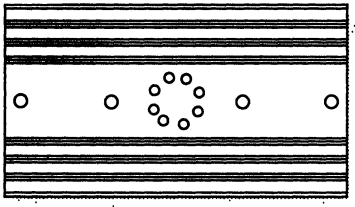




DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	945	965	24.003	24 511
B	945	965	24 003	24.511
C	076	094	1.934	2 388
D	841	.859	21 361	21 819
E	841	859	21 361	21 819
F	.755	785	19.177	19.939
G	755	785	19.177	19.939
H	800 BASIC		20.320 BASIC	
J	027	033	.686	838
K	045 BASIC		1.143 BASIC	
L	.050 BASIC		1.270 BASIC	

Terminations: Gold plated nickel on refractory metallization.
Case: White ceramic with gold plated nickel lid.
Hermeticity: Gross leak test.
Weight: 4.2 grams (0.15oz).

NOTES: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



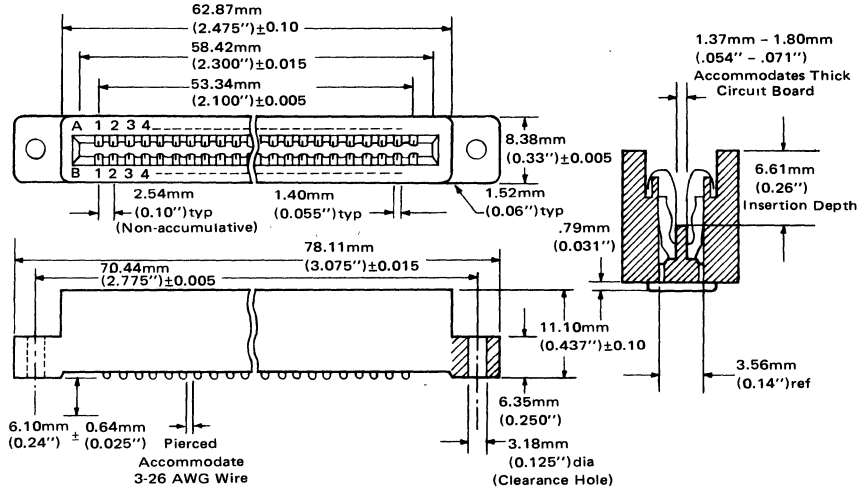
ACCESSORIES

This section contains illustrations and information on various mating connectors and heat sinks available for use with Burr-Brown products. The type of connector or heat sink required by the product is specified in the Product Data Sheet.

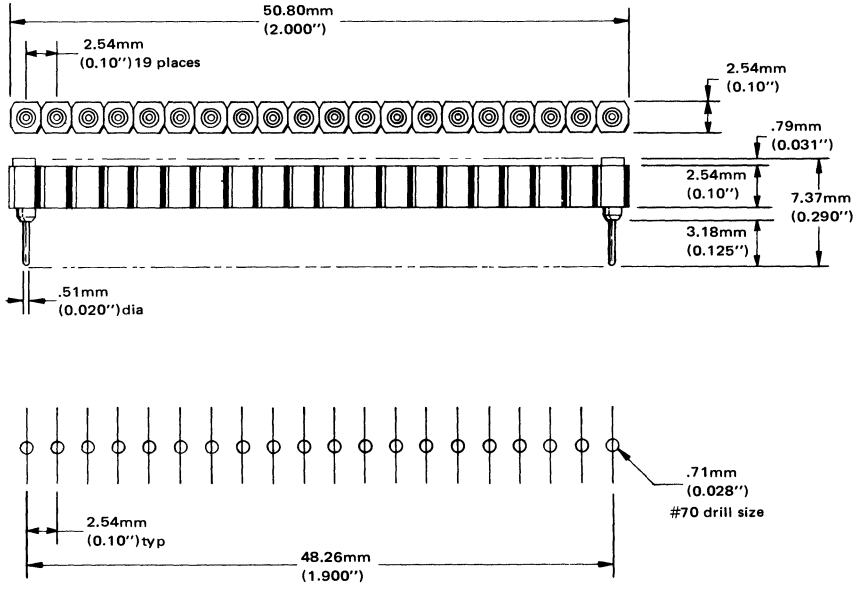
13

MATING CONNECTORS

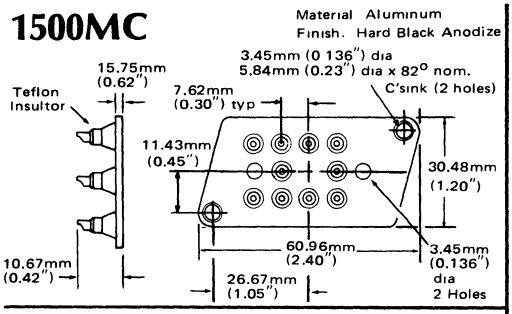
2201MC



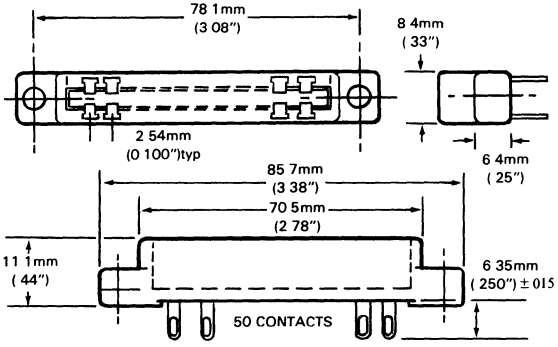
2350MC



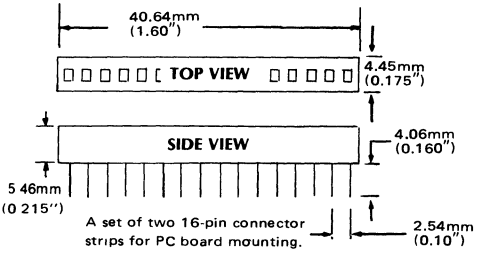
1500MC



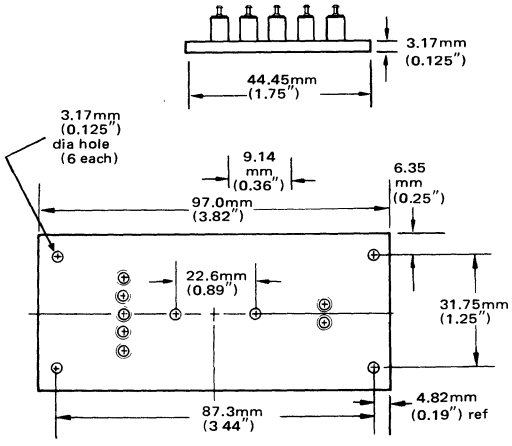
2250MC



2302MC



2800MC

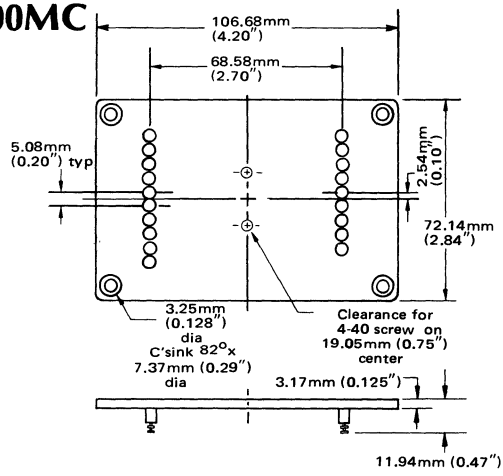


2401MC

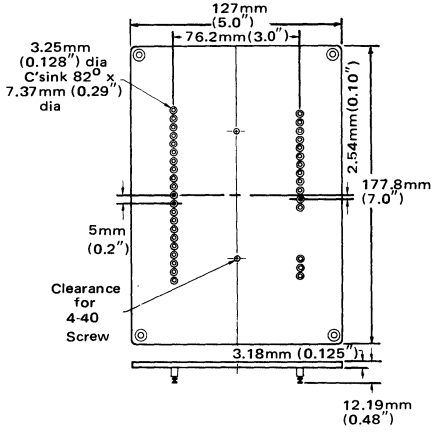
Identical to 2302MC except each connector strip length is 45.72mm (1.80")

A set of four 18-pin connector strips for PC board mounting.

4400MC

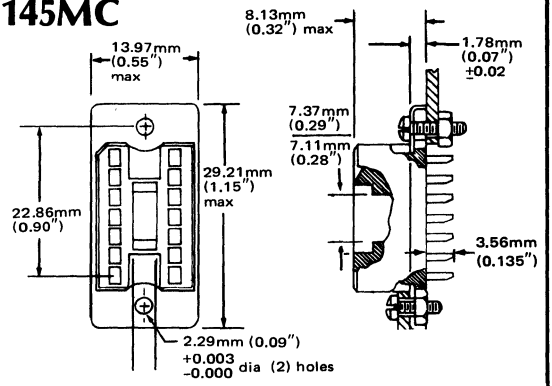


4800MC

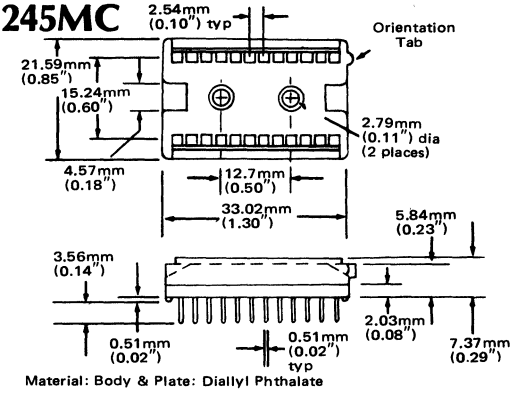


MATING CONNECTORS

145MC

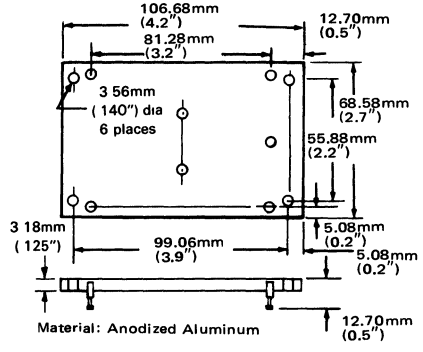


245MC



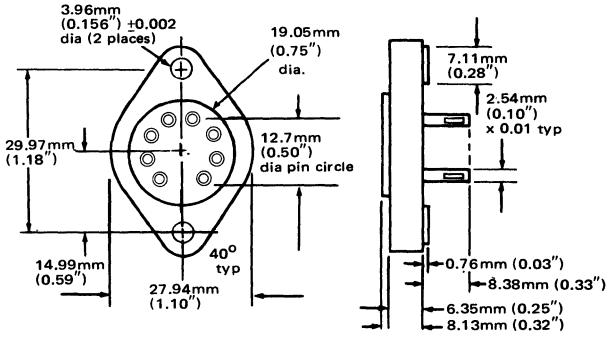
Material: Body & Plate: Diallyl Phthalate

548MC

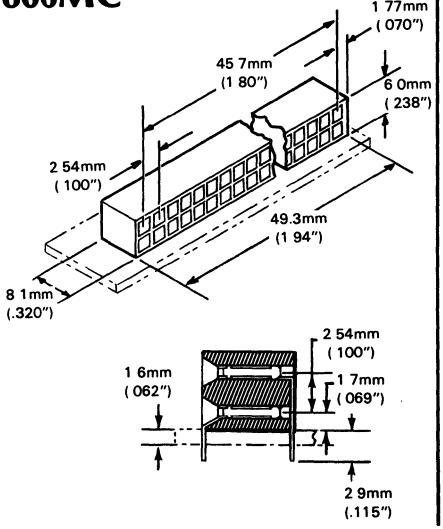


Material: Anodized Aluminum

803MC

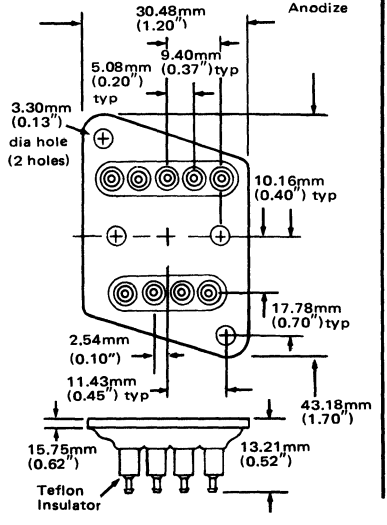


806MC

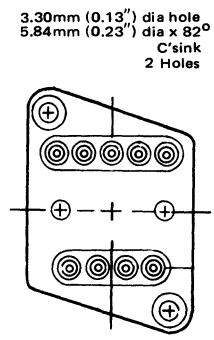


1200MC

Material: Aluminum
Finish: Hard Black Anodize



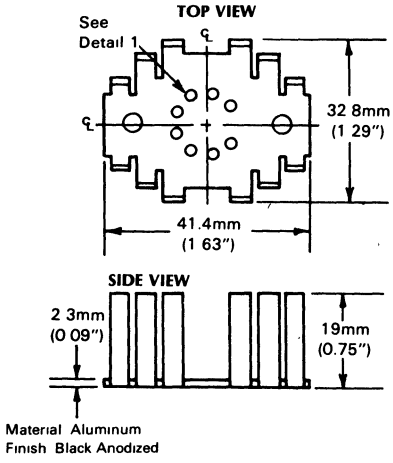
1400MC*



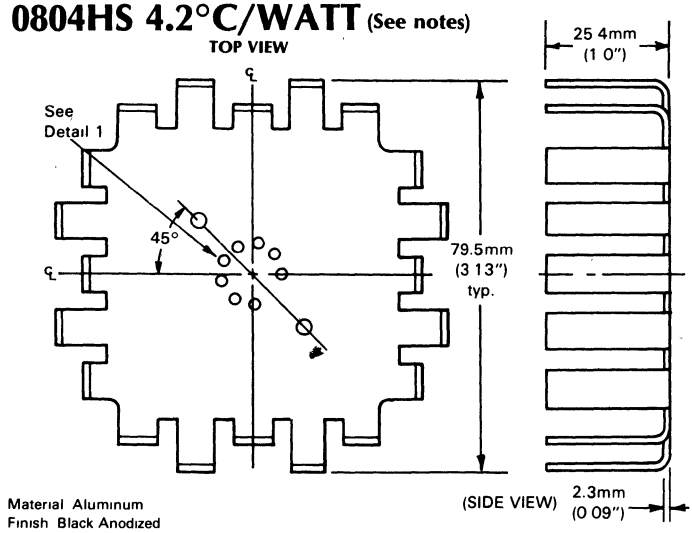
Material: Aluminum
Finish: Hard Black Anodize

* Identical to 1200MC except for mounting holes.

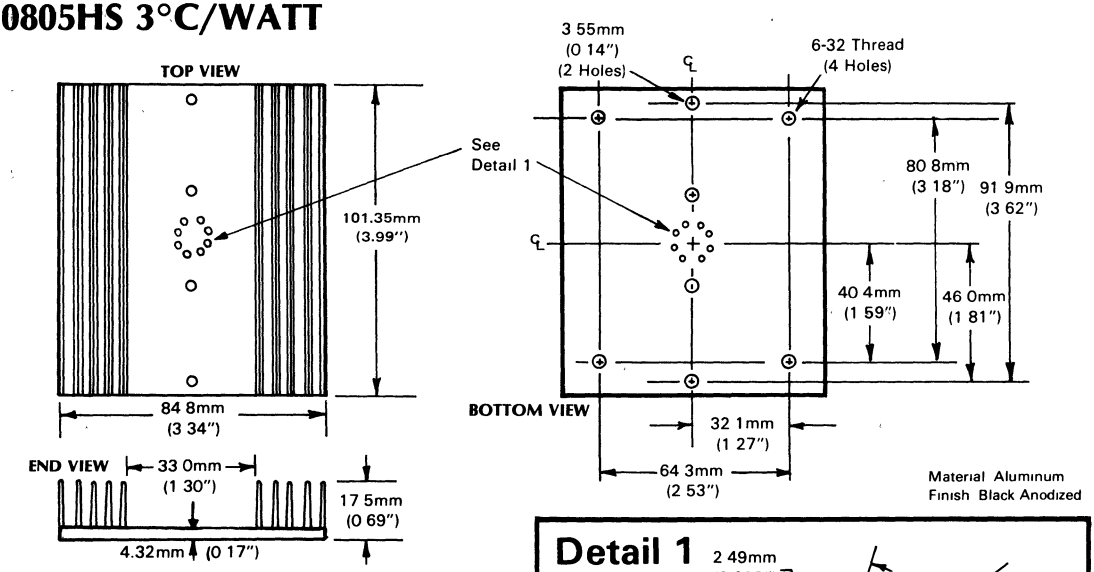
0803HS 12°C/WATT
(See notes)



0804HS 4.2°C/WATT (See notes)



0805HS 3°C/WATT

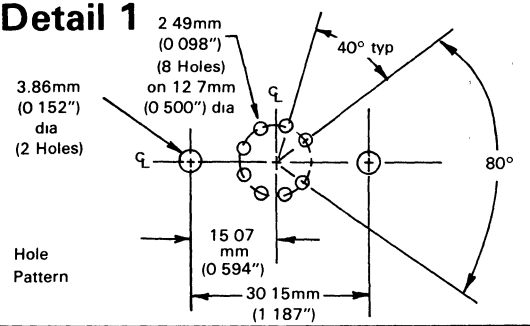


*NOTES

1 Thermal resistance specified are for natural connection Heatsinks 0803HS and 0804HS are mounted on 6" x 6" x 1/16" G-10 PC board

2 A thin-film of heatsink compound (Dow Corning 340 or equivalent) between the heatsink and the TO-3 device is recommended

Detail 1



BURR-BROWN®

0807HS

SKIRTED THERMAL SHIELD

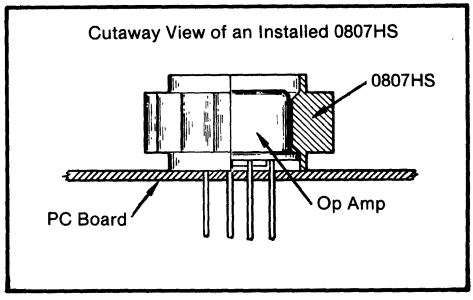
(U.S. Patent 4,636,916)

FEATURES

- IMPROVES AMPLIFIER LOW FREQUENCY NOISE
- IMPROVES AMPLIFIER SHORT-TERM STABILITY
- FITS ALL JEDEC-STANDARD TO-5-SIZE PACKAGES (TO-99, TO-100)

APPLICATIONS

- LOW NOISE OP AMPS
- LOW NOISE INSTRUMENTATION AMPLIFIERS



DESCRIPTION

The 0807HS is a skirted heat sink designed to fit over standard TO-5-size packages (TO-99 and TO-100). Its skirt fits flush against the printed circuit to shield the package leads from air currents. As a heat sink, it increases thermal mass and decreases package temperature rise. When properly applied, the 0807HS will result in substantially improved low frequency noise performance, as shown in Figure 1.

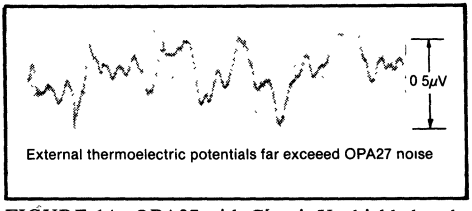


FIGURE 1A. OPA27 with Circuit Unshielded and Exposed to Normal Lab Bench-Top Air Currents.

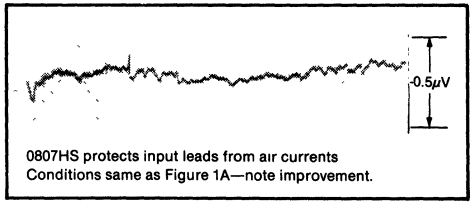
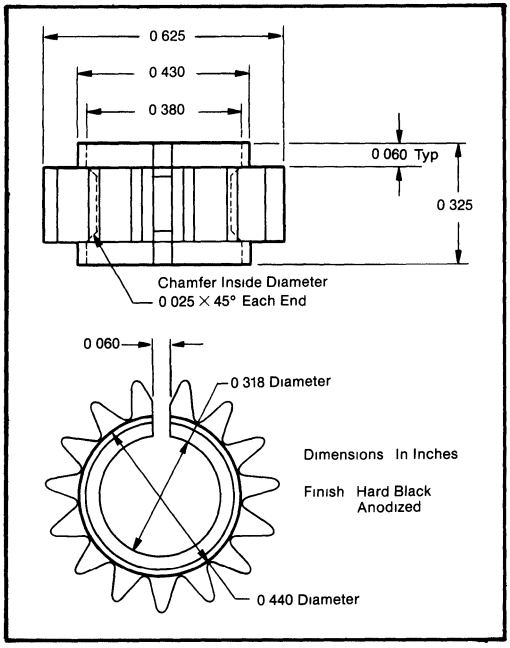


FIGURE 1B. OPA27 with Heat Sink and 0807HS.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-701

MECHANICAL



THEORY OF OPERATION

All metals exhibit an electrical potential accompanying a thermal gradient. This is known as the Thompson thermoelectric effect. When any two dissimilar metals are joined, a thermocouple is formed—the Seebeck effect.

In all semiconductor packages, thermocouples are formed at various interfaces. In "TO-" style packages, significant thermocouples are formed between the gold or nickel plating and the Kovar leads. Thermocouples are also formed between the leads and the solder connections to the printed circuit.

If thermal gradients are properly matched—at the amplifier inputs—the thermocouple errors will cancel. In practice, mismatches occur. Even under laboratory conditions, the errors produced can be several tenths of microvolts—well above the levels achievable with low noise amplifiers. At the output of a high gain amplifier, the error will appear as low frequency noise or short term input offset error.

In a "TO-" package, much of the heat is conducted away through the leads. The resultant thermal gradient between the package and the printed circuit can be a major source of thermal error. Air currents can cool one lead more than another, resulting in mismatched thermal gradients. The 0807HS reduces these errors in two ways. It acts as a heat sink to lower package temperature rise and thereby lower the thermal gradient (see Figure 2). It also shields the package leads from air currents.

Thermal gradients can also be generated by external heat sources such as a nearby device with significant heat rise. Under severe conditions, these errors can be many times greater than those produced under laboratory conditions. To minimize these errors, the 0807HS acts as a thermal "short circuit," minimizing the gradient across the package leads.

Finally, by increasing the thermal mass of the package, the 0807HS minimizes short term temperature changes of the package. Package temperature fluctuations produce input offset drift, which can appear as low frequency noise at the output of a high gain amplifier.

INSTALLATION

Install the 0807HS after other components have been installed, and the board cleaned. Align the slot of the heat sink with the package tab and press in place. It may be necessary to expand the heat sink slightly with a tapered tool, such as the blade of a screwdriver, to ease installation. The 0807HS is symmetrical and either side can go up.

Of course, other sources of thermoelectric error may occur. Careful printed circuit layout, use of low thermal EMF solder, and thermal shielding of the printed circuit back side may be needed to achieve the desired performance.

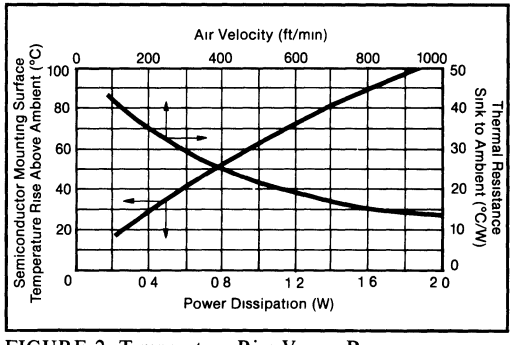
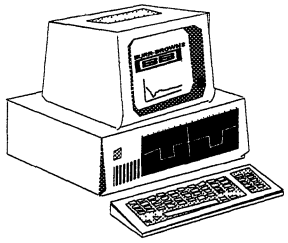


FIGURE 2. Temperature Rise Versus Power.

ORDERING INFORMATION

Model number 0807HS



OTHER BURR-BROWN PRODUCTS

COMPONENT PRODUCTS

Burr-Brown has two component product groups whose offerings are described in separate data books—Military Products and Power Sources. These products are briefly described in this section. For more information and a copy of these other data books, contact your local Burr-Brown salesperson or representative. See the inside back cover.

HIGHER LEVEL PRODUCTS

In addition to designing and manufacturing precision microcircuits, Burr-Brown also excels in microelectronic-based systems used in data acquisition, signal conditioning, measurement, and control. This section contains a sampling of these other high-quality products. If you want additional information, contact your local Burr-Brown salesperson or representative.

BURR-BROWN POWER SUPPLIES AND THE *POWER SOURCES HANDBOOK*

Burr-Brown offers a wide selection of power conversion products. Hundreds of standard and unique DC/DC converters ranging from DIP sizes through high wattage, wide-range modular packages are available. They are summarized in tables on the following three pages. All of these models carry Burr-Brown's guarantee of high quality and reliability and are included in their own publication, *Burr-Brown Power Sources Handbook.*

The *Burr-Brown Power Sources Handbook* contains detailed Product Data Sheets for all of Burr-Brown's power conversion products. In addition, it includes supplementary data, such as an extensive selection guide, discussion of the advanced reliability programs available, a glossary of power conversion terminology, and application notes for effective use of these products. Information on obtaining modified and custom models is also included.

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HIGH-ISOLATION DC/DC CONVERTERS **Boldface = NEW**

Model	Rated Isolation Voltage (VDC)	Rated Power (Watts)	Features
PWR1726	**3500**	**1.5**	**High Isolation**
PWR70	2000	3	Small Size
PWR74	1500	3	Multichannel
PWR13XX Series	**1270**	**1**	**DIP Package**
PWR71	1000	3	Multichannel
PWR72	1000	3	Wide Input Range
PWR1XX Series	1000	450mW	General Purpose
PWR2XX Series	1000	1.5	General Purpose
PWR3XX Series	1000	2	Multichannel
PWR4XX Series	1000	3	Small Size
PWR6XX Series	1000	2	Regulated
PWR7XX Series	1000	5	Regulated
PWR1017	1000	3	Multichannel

DIP-PACKAGED DC/DC CONVERTERS **Boldface = NEW**

Model	Regulation	Internal Filtering	Features
PWR11XX Series	**No**	**Yes**	**Filtered**
PWR13XX Series	**No**	**No**	**High Isolation**
PWR59XX Series	**Yes**	**Yes**	**Filtered**

MULTICHANNEL DC/DC CONVERTERS **Boldface = NEW**

Model	Number of Channels	Number of Outputs Per Channel	Rated Power (Watts)	Features
PWR1017	4	2	3	8 Outputs
PWR71	4	2	3	Small Size
PWR5XX Series	4	1 or 2	4	Small Size
PWR8XX Series	2	3 Total	5	5 ±12 or 5 ±15 V_{OUT}
PWR74	2	2	3	High Isolation
PWR3XX Series	2	1 or 2	2	Small Size
PWR53XX Series	**1 or 2**	**1 or 2**	**15**	**Wide Input Range**

LOW-NOISE DC/DC CONVERTERS

Boldface = NEW

Model	Noise Out (mVp-p) Typ	Noise Out (mVp-p) Max	Rated Power (Watts)	Features
PWR1546A		**1.0**	**5**	**Ultra-Low Noise**
PWR62XX Series	**15**		**5.2**	**ECL Power**
PWR59XX Series	**20**		**2**	**DIP Package**
PWR6XX Series	30		3	Regulated
PWR7XX Series	30		5	Regulated
PWR74	40	100	3	High Isolation
PWR1726	**50**		**1.5**	**High Isolation**
PWR11XX Series	**50**		**3**	**DIP Package**
PWR1XX Series	50		2	General Purpose
PWR3XX Series	50		2	Multichannel
PWR53XX Series		**75**	**15**	**Wide Input Range**
PWR2XX Series	75		1.5	General Purpose
PWR70		80	3	High Isolation
PWR71		100	3	Multichannel
PWR4XX Series		100	3	Small Size
PWR1017		100	3	Multichannel
PWR72		150	3	Wide Input Range

WIDE-INPUT-RANGE DC/DC CONVERTERS

Boldface = NEW

Model	Input Range (VDC)	Rated Power (Watts)	Features
PWR53XX Series	**9-18**	**15**	**Single, Dual, & Triple Outputs**
	18-36	**15**	**Single, Dual, & Triple Outputs**
	36-72	**15**	**Single, Dual, & Triple Outputs**
PWR72	5-22	3	Dual Outputs

REGULATED DC/DC CONVERTERS

Boldface = NEW

Model	Regulation Line (%)	Regulation Load (%)	Rated Power (Watts)	Features
PWR1546A	**±0.02**	**0.02**	**5**	**Low Noise**
PWR6XX Series	±0.02	0.04	3	General Purpose
PWR7XX Series	±0.02	0.04	5	General Purpose
PWR510X	±0.02	0.04	9	General Purpose
PWR62XX Series	**±0.04**	**0.06**	**5.2**	**ECL Power**
PWR59XX Series	**±0.3**	**0.4**	**2**	**DIP Package**
PWR53XX Series	**±0.2**	**1.0**	**15**	**Wide Input Range**

UNREGULATED DC/DC CONVERTERS **Boldface = NEW**

Model	Rated Power (Watts)	Package Size (Inches)	Features
PWR1XX Series	450mW	1.0 x 1.0 x 0.4	General Purpose
PWR13XX Series	**1**	**24-pin DIP**	**High Isolation**
PWR2XX Series	1.5	1.0 x 1.0 x 0.4	General Purpose
PWR1726	**1.5**	**1.2 x 1.6 x 0.4**	**High Isolation**
PWR11XX Series	**2**	**24-pin DIP**	**Filtered**
PWR3XX Series	2	1.0 x 1.0 x 0.4	Multichannel
PWR70	3	1.0 x 1.0 x 0.4	High Isolation
PWR71	3	2.0 x 2.0 x 0.4	Multichannel
PWR72	3	1.0 x 1.0 x 0.4	Wide Input Range
PWR74	3	1.0 x 1.0 x 0.4	Multichannel
PWR4XX Series	3	1.0 x 1.0 x 0.4	General Purpose
PWR1017	3	2.0 x 2.0 x 0.4	Multichannel
PWR5XX Series	4	1.2 x 1.6 x 0.4	Multichannel
PWR8XX Series	5	1.2 x 1.6 x 0.4	Multichannel

DC/DC CONVERTERS BY WATTAGE **Boldface = NEW**

Model	Rated Power (Watts)	Package Size (Inches)	Features
PWR53XX Series	**15**	**2.0 x 2.0 x 0.4**	**Triple Output**
PWR510X	9	2.0 x 2.0 x 0.4	Regulated
PWR62XX Series	**5.2**	**2.0 x 2.0 x 0.4**	**ECL Power**
PWR7XX Series	5	2.0 x 2.0 x 0.4	Regulated
PWR1546A	**5**	**2.0 x 2.0 x 0.4**	**Ultra-Low Noise**
PWR8XX Series	5	1.2 x 1.6 x 0.4	Multichannel

MILITARY PRODUCTS DIVISION

Burr-Brown's Military Products Division manufactures precision signal conditioning and data conversion components for use in military applications such as navigation, guidance, control, electronic counter measures, intelligence, and communications. We offer a growing line of diversified high-reliability military products, including operational amplifiers, A/D and D/A converters, analog multipliers, and voltage-to-frequency converters. Additionally, the Military Products Division is responsible for all microcircuit dice sales. (For your convenience, components in this Data Book that are also available in military and die form are marked as such.)

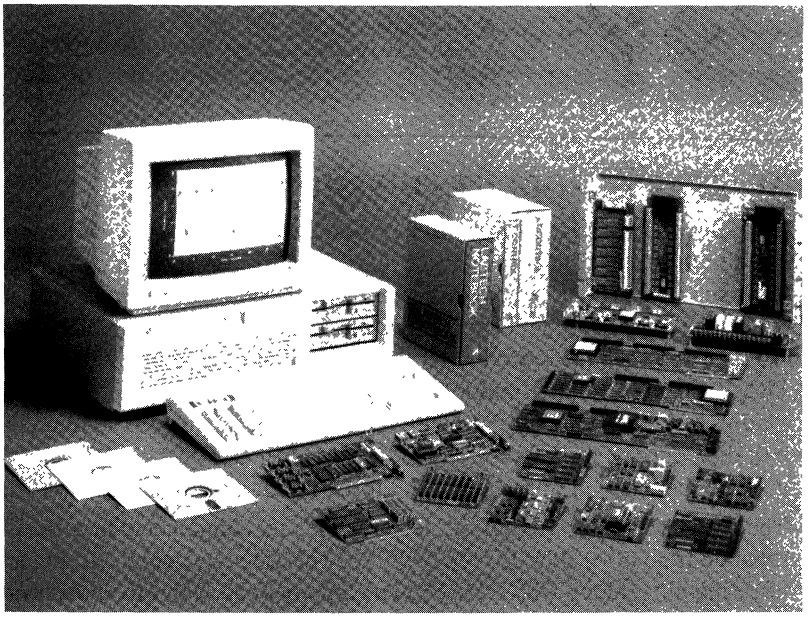
The Military Products Division manufactures its components in a facility separate from other Burr-Brown facilities. This separate manufacturing and test capability, along with Burr-Brown's microcircuit wafer manufacturing and thick-film facilities, are certified to the requirements of MIL-STD-976 and MIL-STD-1772. This means that all manufacturing operations for all Military Products Division components — from design, through raw materials, wafer processing, assembly and test to final product inspection, and shipment — are performed in strict accordance with MIL-STD-883, and full compliance with Appendices A and G of MIL-M-38510.

All monolithic and hybrid "/883B" or "/B" models are compliant to the requirements of the current revision of MIL-STD-883 for compliant Non-JAN devices. Quality Conformance Inspection (QCI) is performed to the requirements of Methods 5005 or 5008. This is detailed in the individual Product Data Sheets for Military components.

Environmental control of the manufacturing clean rooms meet or exceed the requirements of FED-STD-209 for particle count. ESD (electrostatic discharge) procedures are fully observed by Military Products Personnel through every stage of material handling, product assembly, testing, storage, and shipment.

All this results in products with reliability and quality that is built-in, not screened from commercial lots. This provides customers with microcircuits that meet the full intent of military requirements.

In addition, custom screening, testing, and marking of standard products can be accommodated, such as class-S type screening, etc. Consult the Military Products Division or your local Burr-Brown salesperson or representative for additional information.

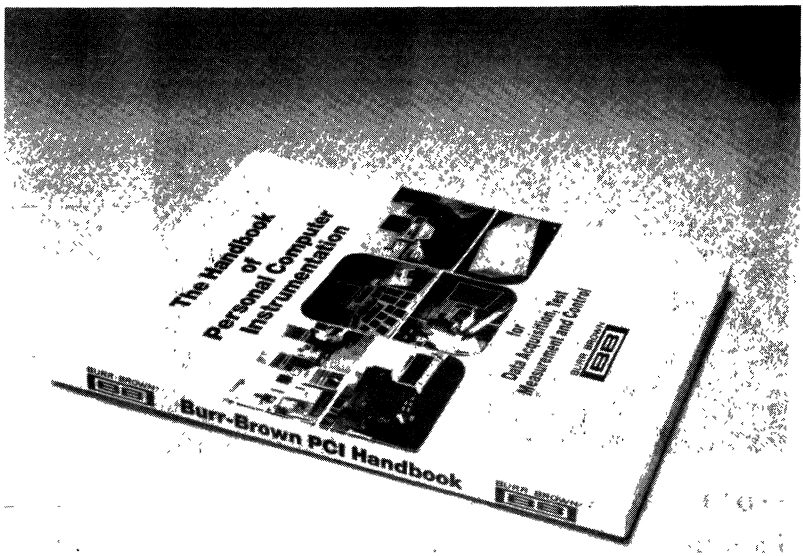


PCI-20000 SERIES: Personal Computer Instrumentation. . .
For Data Acquisition, Test Measurement, And Control

The new PCI-20000 gives you modular I/O you can never outgrow. Component modularity gives you the most cost-effective, expandable PC instrumentation system available today—and tomorrow. The PCI-20000 is an exciting new generation of instrumentation for IBM and bus-compatible personal computers. It lets you start small and add plug-in channels and functions only as requirements grow. You never pay for more I/O than you need.

The key is component modularity. Carrier boards plug directly into the PC expansion slots and provide power, communications, mounting mechanisms and optional digital I/O capability. Versatile I/O modules plug into the carrier and perform the data acquisition, test, measurement, and control functions your systems requires. You can choose from 15 different modules now, with many more planned for the future. Carriers accept two or three modules. A family of termination panels simplify wiring and bring signals to and from the system.

Hundreds of possible systems can be configured now, even more later. Combine components now to meet exact requirements for analog and digital I/O, counter, timer, and pulse functions. Change components later to add capacity and functions for future needs. Your system will always be at its optimum price/performance level. Extensive software is available.



HANDBOOK OF PERSONAL COMPUTER INSTRUMENTATION: For Data Acquisition, Test Measurement, And Control

Contains: A **tutorial section** describing in practical terms, the theory and philosophy of using personal computer instrumentation for data acquisition, test, measurement, and control.

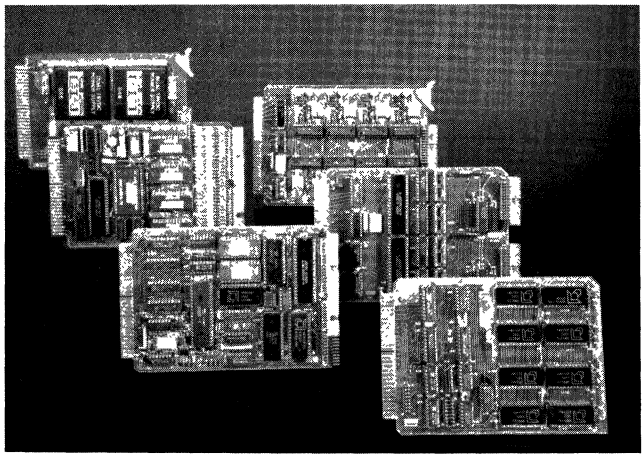
An **application section** complete with dozens of diagrams, showing specifically how you can use personal computer instrumentation in more ways than you ever thought possible.

Written by leading experts who design and use intelligent instrumentation systems, this section is the (sweet) heart of the handbook with plenty of down-to-earth advice about how to apply PCI.

A **software section** that describes and references the wide range of packages that are readily available from vendors, and from software houses often overlooked by some firms.

There's more. Much more. Including guides on how to configure a system and technical specifications for specific PCI hardware and software. Contact your local Burr-Brown saleperson or representative for your copy.

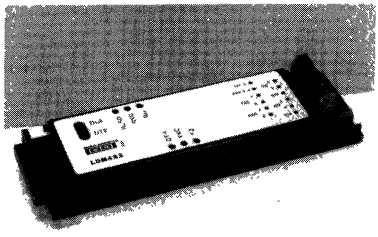
STD BUS & DATA COMMUNICATIONS PRODUCTS

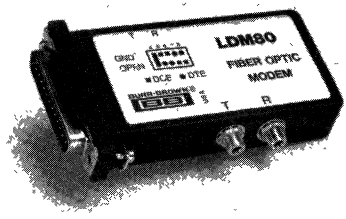


STD BUS INDUSTRIAL I/O PRODUCTS

The Burr-Brown STD Bus products provide the most cost-effective tool for solving the applications-oriented problems of process control and system integration.

The modularity and simplicity offered by this well-defined standard have led to the development of a complete line of STD Bus products. The line includes a disk controller and operating system, a Z80 CPU with onboard DMA, various memory boards, a 32-channel 12-bit A/D converter, two CRT controllers, and IEEE-488 interface card, and two types of discrete I/O cards.





DATA COMMUNICATIONS PRODUCTS

Burr-Brown Data Communications products provide the most cost-effective tool for solving the local data communications problems for industrial and institutional facilities.

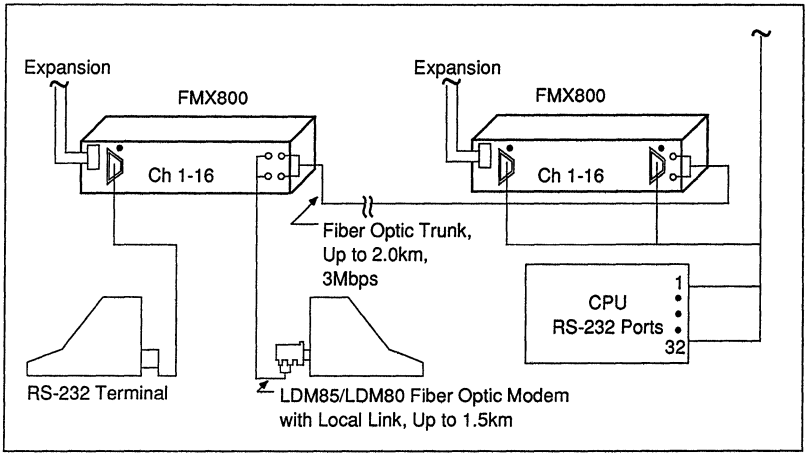
Limited distance and Fiber Optic Modems provide extension of RS-232 ports up to several miles. In addition, electrical isolation for wire units is provided by transformers and optical couplers, eliminating ground loops,

equipment damage, and noise pickup. Surge suppression devices are internally mounted on all field inputs and outputs. The LDM422 (left) serves as a Limited Distance Modem and as an RS-232-to-RS-422 converter with multipoint capability. It has two complete high speed transmit and receive for data and handshake. It features 1000V isolation and surge protection.

Fiber optic modems offer the maximum in isolation and EMI/RFI immunity. The LDM80 (right) is signal powered from RS-232 ports transmits up to 3.5km at 19.2Kbits per second. The LDM85 is a unique multipoint-capable modem with data rates to 5Mbits per second.

Other products include:

LDM35—Signal-Powered Limited-Distance Modem.
LDM70—High Speed Ruggedized Industrial Modem.
APA120—Personal-Computer-Based Protocol Analyzer.



DATA MULTIPLEXER

As illustrated above, the FMX800 fiber optic multiplexer family provides a three megabaud link between separate buildings and clusters of computers or terminal ports. A single FMX800 chassis allows up to 16 19.2Kbaud ports to be extended through a single pair of glass fibers. Up to three expansion units make the channel count 64. All channels may operate full duplex at the maximum RS-232.V.24 data rate of 19.2kbaud. Control signals Request To Send (RTS), Clear To Send (CTS), Data Set Ready (DSR), and Data Terminal Ready (DTR) are continuously scanned and carried through the trunk line to provide remote handshake capability.

COMPONENT TERMINALS

WHY REINVENT AN OPERATOR INTERFACE?

Is your microprocessor-based equipment used or serviced by human beings? If so, you may be interested in a new line of operator interface terminals from Burr-Brown. The operator interface provides the way for an operator to setup and run equipment; it may also provide diagnostic/service access for a repairman.

For most new products, the operator interface is custom designed because no off-the-shelf product has been available which adequately addresses this need. This means that engineering resources are needed, which will place an additional demand on already limited manpower. The availability now of commercial/industrial operator interfaces allows companies to concentrate their resources in the area of their greatest expertise, and therefore, to get the best return on engineering investment.

Operator interfaces are used in a variety of equipment. There are numerous controller applications such as machine controllers, motor controllers, process controllers, HVAC controllers, programmable controllers, and motion controllers. Other applications include operator interface for instruments, test machines, data acquisition systems, weighing systems, imaging systems, and medical equipment.

Consider these issues when looking for an operator interface:

Display

Is it easily readable in your operating environment?

Keyboard

Is the tactile response appropriate for your needs? Can the keys be clearly marked for your application?

Operation

Will the units operate in a mode that is convenient in your application?

Communications

What interface do you need? RS-232C is a good choice for many applications. RS-422 is useful for distances of greater than 50 feet or for electrically noisy environments.

Package

Will the package fit into your equipment, aesthetically and physically? Is it easy to mount? Does the package need to be sealed?

Environment

Under what conditions must the unit operate?

Burr-Brown has recently introduced a line of operator interface terminals, the TM2500 and the TM2700, which use standard ASCII communications. They are low cost, easy-to-use, easy-to-design-in units. In many applica-

tions it is no longer necessary to design an expensive long-lead-time custom operator interface. These units provide a large liquid-crystal display with a wide viewing angle. The terminals go through an automatic self-test every time power is applied. The keyboard offers excellent tactile response, providing a numeric keypad, six user-programmable function keys, and six control keys. The function keys are back-lighted under host computer control. They can also be programmed to transmit any sequence of up to four characters. Each function key has a label area adjoining it so that the user can easily customize each key.

The terminals operate in one of three modes. In character mode, a character is transmitted as each key is pressed. The character may be echoed to the display as defined. In the block mode, all characters are internally buffered and displayed as keys are pressed. The entire line of data is then transmitted when the enter key is pressed. The polled mode is the third way to operate these units. In the polled mode, data is entered as in the block mode; however, the data is not transmitted until the host processor requests it. Another option in this mode is to assign each terminal an address so that a number of terminals may be committed to the same host interface line.

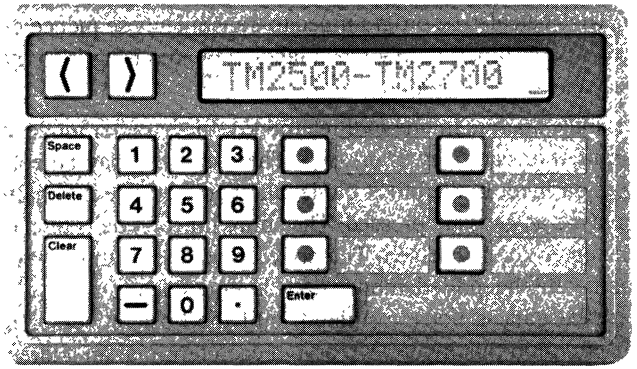
Other options include baud rate, line termination, turnaround delay, display viewing angle, hand check protocol, local echo, key repeat, and key click. All options are user selectable and stored in nonvolatile EEPROM.

The TM2500 is available with an RS-232C interface, while the TM2700 is provided with an RS-422 interface.

These microterminals provide an easy-to-use, off-the-shelf interface in many new equipment designs.

BURR-BROWN®

TM2500
TM2700



OEM MICROTERMINALS

BENEFITS/FEATURES

- MINIMIZES DEVELOPMENT TIME AND EXPENSE
- LARGE, HIGH CONTRAST 16-CHARACTER LCD DISPLAY
- 80-CHARACTER DISPLAY BUFFER
- SIX PROGRAMMABLE BACKLIT FUNCTION KEYS
- POSITIVE TACTILE FEEDBACK KEYBOARD
- EASILY CUSTOMIZED LABELS
- ADJUSTABLE VIEWING ANGLE
- NONVOLATILE CONFIGURATION STORAGE
- POWERUP SELF-TEST
- ALL OPTIONS USER-SELECTABLE

APPLICATIONS

- OPERATOR PANEL
- SERVICE/DIAGNOSTIC DEVICE
- DATA COLLECTION TERMINAL

DESCRIPTION

The TM2500/TM2700 are low cost, compact, industrial data entry and display terminals. They are designed to be used as operator panels, as well as service and diagnostic equipment. The terminals can also be used as a simple keyboard entry data collection terminal. The TM2500 and TM2700 are similar units, differing only in communications interface—RS-232C on the TM2500 and RS-422 on the TM2700.

Both terminals are lightweight, 10.5 ounces, and are enclosed within a 4.102″ × 7.102″ × 1.060″ case. The terminals have six backlit programmable function keys. Space is provided to customize the keyboard and function keys with company logos and function labels. The compact size of the TM2500/TM2700 makes them ideal for applications where space is at a premium.

The TM2700 is recommended for electrically noisy environments, multidrop applications, and where communication distances of more than 50 feet are required. Fifteen command sequences are used by the host to control these terminals. Burr-Brown's 25 years of experience in developing and producing OEM products has ensured that the design of the TM2500/TM2700 is focused on the needs of potential and existing customers.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-739A

KEYBOARD

A numeric keypad with six programmable function keys is provided for operator input. The keys are widely spaced for ease of entry. The silicon rubber keyboard provides environmental sealing with good tactile feedback. A unique characteristic of the keyboard is that each function key is backlit. The backlighting is under host computer control to give maximum flexibility to the operator. The keyboard also features key click and key repeat functions. If an invalid key is pressed, the terminal responds with an audible tone.

DISPLAY

The display is a 16-character LCD with large, easy to read characters. An 80-character display buffer with scroll keys allows the operator to slide the 16-character window across the 80-character line. The high contrast display on the terminals provides sufficient alphanumeric display capability for most panel-mount applications.

CASE

The case for the TM2500/TM2700 is designed for either surface or recessed mounting. The keyboard and display are sealed in the ABS plastic case so that when properly mounted, the terminal is protected against dust and moisture.

SPECIFICATIONS

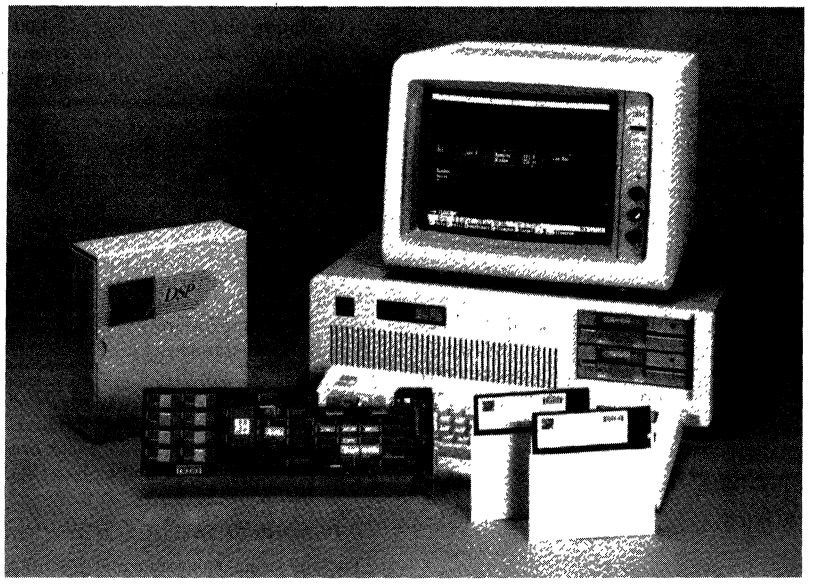
Display	16-character alphanumeric LCD with adjustable viewing angle
Character Size	0.38″ (9.66mm) character height
Display Buffer	80 characters
Keyboard	Sealed molded silicon rubber
Scrolling Keys	Two, manual
Keypad	Numeric
Number of Keys	24
Operation Life	1,000,000 operations
Function Keys	Six, programmable, backlit
Indicators	Audible tone, flashing display, 6 LEDs
Communications	TM2500—RS-232C, point-to-point; TM2700—RS-422, multidrop up to 32 terminals
Power	5VDC or 7.5 to 10VDC at 250mA max, TM2500 350mA max, TM2700
Baud Rate	300, 1200, 9600
Modes	Character and block
Operating Temperature	0°C to +50°C (32° F to 122° F)
Storage Temperature	−20°C to +70°C (−4° F to +158° F)
Dimensions	4.102″ × 7.102″ × 1.060″
Weight	10.5 ounces
Mounting	Flush or surface mounted
Case	Dust and moisture sealed ABS plastic

ENVIRONMENTAL QUALIFICATIONS

The following environmental qualification tests were performed on TM2500/TM2700:

Altitude	50,000 feet nonoperational, 15,000 feet operational
Temperature Rating	−20°C to +70°C storage, 0°C to +50°C operational
Keypad Service Life	One million operations
Vibration	Search—5–55Hz in three planes, Cycling—55–500–55Hz at 3G
Mechanical Shock	30G with duration of 11ms
Radio Interference	Meets FCC Class A compliance
Conducted Interference	Meets FCC Class A compliance
Radio Susceptibility	2.0V per meter over 14kHz–10GHz in vertical or horizontal sweep
Bench Drop Test	4″ or 45° pivot drop to 1-5/8″-thick bench top
Package Drop Test	Certified by the National Safe Transit Association

DIGITAL SIGNAL PROCESSING
DEVELOPMENT TOOLS & REAL-TIME PRODUCTS



Burr-Brown's PC-based DSP development tools and products dramatically reduce the development cycle of new designs using digital signal processing.

First, the development tools provide an efficient, user-friendly interface for creating algorithms and "proving" designs on real-time hardware.. The component modules, then, provide a straightforward, cost-effective method for integrating the solution into production runs of the overall design. Following are just a few of the tools Burr-Brown currently offers:

DSPlay ™ — Simulates the Design

The *DSPlay* Software Package transforms the PC into a powerful Digital Signal Processing workstation. The package provides you with a graphic editor for creating block diagrams, which then translate into DSP algorithms. When you have created the block diagram, or "FlowGram™," the software will then execute the algorithm and display the data at any point in the signal flow.

The package features more than 70 DSP and related block functions including real signal acquisition. To complete the package, a utilities menu provides filter design programs, text editor, and DOS commands.

For most engineers, *DSPlay* offers an extremely practical tool in concepting and designing DSP solutions.

DSPlay XL/32 — The Software to Emulate and Prove the Design

The *DSPlay* XL/32 Software Package provides the same user interface as *DSPlay* with one notable difference—XL generates highly efficient code for AT&T's (WE®) DSP32 processor and, therefore, provides the way to quickly demonstrate or prove a design.

Once generated in XL, the block diagram simulating the program may be executed in real-time by downloading it directly to Burr-Brown's PC-based processor board, *DSPeed*™. The necessary ADC/DAC interface code is already present.

In addition to filter-design programs, text editor, and DOS commands, *DSPlay* XL/32 features a built-in assembler and debugger enabling the user to write and include custom block functions.

Although specifically designed to run with the *DSPeed* (ZPB32) board, *DSPlay* XL/32 can also be used to generate code for any DSP32 application.

The Hardware to Execute the Design—The *DSPeed* Processor

DSPeed is a PC-based DSP Floating Point Processor board capable of performing complex 1024-point FFT's in less than 10ms!

The board integrates AT&T's DSP32 Digital Signal Processor on a full-size PC card, increasing the PC's computing power by orders of magnitude. This computing power improvement, coupled with the board's two separate high-speed buffered serial data busses and 64KB of SRAM, enable the PC to process signals in real-time.

DSPeed is supplied with a software utilities program for downloading and executing any program written for the DSP32. The utilities allow for breakpoints, and for the viewing registers, accumulators, and memory.

The standard version of *DSPeed*, the ZPB32, is provided with a 250ns processor. For faster processing, a 160ns part is optionally available; Order part number ZPB32-HS.

ZPB100 — The Analog Interface

The ZPB100 provides low cost, real-time analog input and output. The board implements an input amplifier, anti-aliasing filter, 15-bit ADC , 15-bit DAC, smoothing filter, and output filter onto a half-size PC board. The board features separate serial data busses for direct connection to the *DSPeed* board. With these features, the ZPB100 is ideal for development in speech or telecommunications applications.

DSPlay™, *DSPeed*™, FlowGram™ Burr-Brown Corp.
WE® AT&T Corp.

COMPONENT MODULES — COST-EFFECTIVE INTEGRATION

ZPP1001 — "Zero Chip Interface" High-Performance ADC

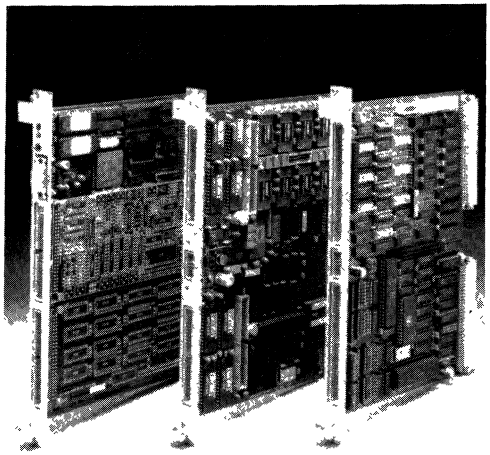
The ZPP1001 provides a 16-bit resolution, 14-bit linear, 150kHz ADC with direct connection—no glue logic required—to AT&T's Digital Signal Processors (DSP16, DSP32, DSP32C). Two modules can be cascaded for dual-channel operation.

ZPP2001 — "Zero Chip Interface" High-Performance DAC

The ZPP1001 provides a 16 bit resolution, 14-bit linear, 150kHz DAC with direct connection—no glue logic required—to AT&T's Digital Signal Processors (DSP16, DSP32, DSP32C). Two modules can be cascaded for dual-channel operation.

Other design and integration tools for the PC and other bus structures are currently in development. If you need to find the shortest route from DSP development to integration, call a Burr-Brown applications engineer at (602) 746-1111.

VMEbus BOARDS



Analog and Digital I/O and Digital Signal Processing Boards for VMEbus Systems.

Burr-Brown first introduced VMEbus products in 1983 and now manufactures a comprehensive line of specialized products for the industrial instrumentation, control, and automation markets. Using Burr-Brown high performance data conversion products (for example the ADC803) we are able to offer products that set new performance standards in the VMEbus market. When these are operated with the digital signal processing boards, a wide range of applications can be addressed.

THE SYSTEM APPROACH

We've taken a system approach in the design of the bus interface. This ensures software compatibility between the boards as well as giving the system designer a wide range of VMEbus features:

- Configuration A24, D16, DTB slave.
- Address block selectable within 16Mb memory space.
- Short addressing available if required (64 bytes).
- 7-level interrupt priority selection.
- Full interrupt vector selection—8 lines (256 options).
- Double Eurocard format, 160mm x 233mm.

SUPPORT DOCUMENTATION

Each VMEbus board is fully supported with a comprehensive operating manual. In addition to detailed set-up and operating instructions, the manual includes schematics and assembly language software written for the 68000 processor.

TOP-QUALITY BURR-BROWN VMEbus PRODUCTS

In addition to the full QC inspection of incoming components, the boards are subjected to a comprehensive temperature-cycled burn-in (8 cycles between –20°C and +50°C).

Exhaustive tests before and after burn-in ensure that any problems are identified before the product leaves the factory.

MORE INFORMATION

You can get additional information on VMEbus products from the Industrial Systems Products Group by calling (602) 746-1111.

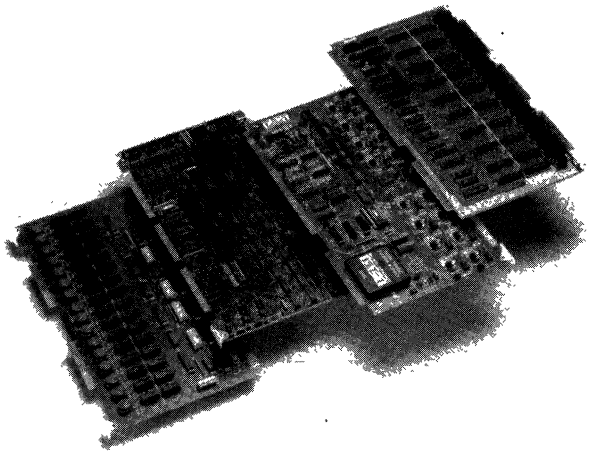
VMEbus PRODUCTS

Model	Description
General-Purpose Analog I/O Boards	
MPV901	32 SE/16 DIF inputs. 12-bit resolution. Optional outputs and software-programmable amplifier.
MPV904	16 voltage outputs. 12-bit resolution. (Current output option MPV908.)
MPV906	64 SE/32 DIF isolated input. 12-bit resolution. TTL I/O expansion module.
MPV907	32 SE/16 DIF inputs. 12-bit resolution. TTL I/O expansion module.
High-Performance Analog I/O Boards	
MPV911	8 inputs. 16-bit resolution. Swinging buffer RAM.
MPV950	16 inputs. 330kHz sampling rate.
MPV952	8 inputs. 330kHz sampling rate. Swinging buffer RAM.
MPV954	8 outputs. 858kHz sampling rate. Dual port RAM.
Intelligent Analog & Digital I/O Boards	
MPV940 Family	68000 controller with 512Kb DRAM. Analog and digital I/O modules and expansion boards available.
Digital I/O Boards	
MPV902/MPV903	32-channel relay output with 0.5A or 1.5A relay contacts.
MPV910	32-channel. 600VDC isolation.
MPV930	48-channel TTL I/O. Output readback. Status LEDs.
Digital Signal Processing (DSP) Boards	
SPV100	DSP CPU Board. TMS32010 processor. Swinging buffer RAM.
SPV120	DSP CPU Board. TMS32020 processor. Two RS-232 ports, auxiliary I/O ports, DMA controller, RAM, ROM, and EPROM. Supplied with EPROM-based monitor.
SPV125	DSP CPU Board. TMS320C25 processor. Two RS-232 ports, auxiliary I/O ports, on-board DMAC, dual port memory supplied with EPROM-based monitor.
MPV121	Module carrier for SPV120 analog I/O modules.
MPV960	DSP CPU board. TMS32010 processor. 4-channel analog input, simultaneous sampling, 100kHz sampling rate.
MPV990	4-channel anti-aliasing filter for MPV960.

Software

PSOS and VERSADOS Drivers for most boards
DSP Applications Software
Development Software for TMS320 CPUs

MULTIBUS I/O BOARDS



Analog and Digital Input/Output Boards for IEEE-796 Compatible Microcomputer Systems.

Burr-Brown offers a complete selection of general-purpose and special-function subsystem-level I/O boards for industrial, process, and laboratory data acquisition, monitoring, and control applications.

OFF-THE-SHELF SYSTEM SOLUTIONS

Burr-Brown Multibus boards can be configured into complete, high-performance I/O systems quickly and economically. Results? Cost-effective working systems in-place or ready for market in time to meet demanding application and customer schedules.

MORE INFORMATION

You can get additional information on Multibus products from the Industrial Systems Products Group by calling (602) 746-1111.

FEATURES

- Low cost
- Easy to program
- Memory or I/O mapped
- 48-hour burn-in at 70°C
- Analog outputs
- Relay outputs
- Isolated discrete inputs
- Analog inputs:
  - 12-bit resolution
  - Software, resistor gain setting
  - Low/high level signals
  - High-channel density
  - High speed
  - Input voltage protection, isolation

CROSS-REFERENCE INFORMATION

HOW TO USE

The following table has been arranged for your convenience. Use it when you have another manufacturer's part and want to find the closest equivalent Burr-Brown part. Other manufacturers are listed alphabetically, with their model numbers listed alphanumerically within each company name.

We have listed has three levels of equivalency: P/P means Pin for Pin. The part is a true second source. F/E means Functional Equivalent. The model offers a very similar function and very similar performance, but is not pin for pin. C/P means Closest Part. The part has similar function and similar performance, but significant differences exist.

When you have identified the corresponding Burr-Brown model, see if its Product Data Sheet is in this book by using the Model Index on the inside front cover. For models not included in this Data Book, request the Product Data Sheet from your local Burr-Brown salesperson or representative. They are listed on the inside back cover.

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CROSS-REFERENCE INFORMATION

Company	Model	Burr-Brown Model[1]	Description	Equivalency[2]
Analog Devices	433	4302	Multifunction Converter	F/E
Analog Devices	436	4204/4206	Analog Divider	F/E
Analog Devices	757	LOG100	Log Amp	F/E
Analog Devices	AD OP-07	OPA27	Op Amp	F/E
Analog Devices	AD OP-27	OPA27	Op Amp	P/P
Analog Devices	AD OP-37	OPA37	Op Amp	P/P
Analog Devices	AD101A	3508J	Op Amp	C/P
Analog Devices	AD171	3582	High Voltage Op Amp	C/P
Analog Devices	AD202	3656	Isolation Amp	F/E
Analog Devices	AD202	ISO102/106	Isolation Amp	C/P
Analog Devices	AD202	ISO120/121	Isolation Amp	C/P
Analog Devices	AD204	ISO102/106	Isolation Amp	C/P
Analog Devices	AD210	3656	Isolation Amp	F/E
Analog Devices	AD289	3650/56	Isolation Amp	F/E
Analog Devices	AD289	ISO100	Isolation Amp	C/P
Analog Devices	AD289	ISO102/106	Isolation Amp	C/P
Analog Devices	AD293	3656	Isolation Amp	F/E
Analog Devices	AD293	ISO102/106	Isolation Amp	C/P
Analog Devices	AD294	3656	Isolation Amp	F/E
Analog Devices	AD294	ISO102/106	Isolation Amp	C/P
Analog Devices	AD295	3656	Isolation Amp	F/E
Analog Devices	AD346	SHC804	Sample/Hold	F/E
Analog Devices	AD363	SDM854	Data Acq System	C/P
Analog Devices	AD363	SDM856	Data Acq System	C/P
Analog Devices	AD363	SDM857	Data Acq System	C/P
Analog Devices	AD363	SDM872	Data Acq System	C/P
Analog Devices	AD364	SDM873	Microperipheral	C/P
Analog Devices	AD376	ADC76	A/D Converter	P/P
Analog Devices	AD380	OPA605	Op Amp	C/P
Analog Devices	AD381	OPA606	Op Amp	P/P
Analog Devices	AD382	OPA605	Op Amp	C/P
Analog Devices	AD389	SHC76	Sample/Hold	P/P
Analog Devices	AD503	OPA121	Op Amp	P/P
Analog Devices	AD504	3510	Op Amp	F/E
Analog Devices	AD506	OPA121	Op Amp	P/P
Analog Devices	AD507	3508	Op Amp	P/P
Analog Devices	AD509	3507	Op Amp	P/P
Analog Devices	AD510	OPA27	Op Amp	P/P
Analog Devices	AD515	AD515	Op Amp	P/P
Analog Devices	AD517	OPA27	Op Amp	F/E
Analog Devices	AD518	3507	Op Amp	F/E
Analog Devices	AD521	INA101	Precision Inst Amp	F/E
Analog Devices	AD524	INA101	Precision Inst Amp	F/E
Analog Devices	AD524	INA102	Precision Inst Amp	F/E
Analog Devices	AD524	INA110	Precision Inst Amp	P/P
Analog Devices	AD532	MPY100	Analog Multiplier	F/E
Analog Devices	AD533	MPY100	Analog Multiplier	F/E
Analog Devices	AD534	MPY534	Analog Multiplier	P/P
Analog Devices	AD535	MPY534	Analog Divider	F/E

NOTES: (1) See Model Index, inside front cover. (2) P/P = Pin for Pin. A true second source. F/E = Functional Equivalent. Very similar function and performance, but not pin for pin. C/P = Closest Part. Similar function and performance, with significant differences.

Company	Model	Burr-Brown Model[1]	Description	Equivalency[2]
Analog Devices	AD536	4341	RMS/DC	F/E
Analog Devices	AD537	VFC32	V/F Converter	C/P
Analog Devices	AD539	MPY634	Wideband Analog Multiplier	C/P
Analog Devices	AD542	OPA121/3542	Op Amp	F/E
Analog Devices	AD544	OPA606	Op Amp	F/E
Analog Devices	AD545	OPA121/111	Op Amp	P/P
Analog Devices	AD547	OPA111	Op Amp	F/E
Analog Devices	AD548	OPA111/121	FET Op Amp	F/E
Analog Devices	AD549	OPA128	Op Amp, Electrometer FET	F/E
Analog Devices	AD565	DAC80	D/A Converter	C/P
Analog Devices	AD565	DAC85H	D/A Converter	C/P
Analog Devices	AD565	DAC87H	D/A Converter	C/P
Analog Devices	AD566	DAC80	D/A Converter	C/P
Analog Devices	AD566	DAC85H	D/A Converter	C/P
Analog Devices	AD566	DAC87H	D/A Converter	C/P
Analog Devices	AD567	DAC811	D/A Converter Latched	F/E
Analog Devices	AD569	DAC709	D/A Converter Latched	C/P
Analog Devices	AD572	ADC84	A/D Converter	F/E
Analog Devices	AD572	ADC85H	A/D Converter	F/E
Analog Devices	AD574	ADC574	A/D Converter	P/P
Analog Devices	AD578	ADC803	A/D Converter	F/E
Analog Devices	AD581	REF10	Voltage Reference	C/P
Analog Devices	AD582	SHC298	Sample/Hold	C/P
Analog Devices	AD582	SHC5320	Sample/Hold	F/E
Analog Devices	AD583	SHC5320	Sample/Hold	F/E
Analog Devices	AD584	REF101	Voltage Reference	C/P
Analog Devices	AD585	SHC5320	Sample/Hold	F/E
Analog Devices	AD587	REF10	Voltage Reference	F/E
Analog Devices	AD587	REF101	Voltage Reference	F/E
Analog Devices	AD588	REF101	Voltage Reference	C/P
Analog Devices	AD606	INA101	Precision Inst Amp	F/E
Analog Devices	AD611	OPA121	Op Amp	F/E
Analog Devices	AD611/2/4	3606	Programmable Gain IA	F/E
Analog Devices	AD611/2/4	PGA200/201	Programmable Gain IA	F/E
Analog Devices	AD624	INA101	Precision Inst Amp	F/E
Analog Devices	AD624	INA102	Precision Inst Amp	F/E
Analog Devices	AD624	INA110	Precision Inst Amp	P/P
Analog Devices	AD625	INA101	Precision Inst Amp	F/E
Analog Devices	AD632	MPY100	Analog Multiplier	F/E
Analog Devices	AD633	MPY634	Analog Multiplier	C/P
Analog Devices	AD642	OPA2111	Op Amp	C/P
Analog Devices	AD644	OPA2111	Op Amp	C/P
Analog Devices	AD647	OPA2111	Op Amp	F/E
Analog Devices	AD648	OPA2111	FET Op Amp, Dual	F/E
Analog Devices	AD650	VFC320	V/F Converter	C/P
Analog Devices	AD651	VFC100	V/F Converter Synchronized	P/P
Analog Devices	AD654	VFC32	V/F Converter	C/P
Analog Devices	AD667	DAC811	D/A Converter Latched	F/E
Analog Devices	AD683	SHC803/804	Sample/Hold	F/E

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CROSS-REFERENCE INFORMATION

Company	Model	Burr-Brown Model[1]	Description	Equivalency[2]
Analog Devices	AD693	XTR101	Two-Wire Current Loop Transmitter	F/E
Analog Devices	AD711	OPA602	FET Op Amp	P/P
Analog Devices	AD712	OPA2111	Dual 711	C/P
Analog Devices	AD744	OPA605	Op Amp	
Analog Devices	AD2700	REF10	Voltage Reference	C/P
Analog Devices	AD2701	REF101	Voltage Reference	C/P
Analog Devices	AD2702	REF101	Voltage Reference	C/P
Analog Devices	AD2710	REF10	Voltage Reference	F/E
Analog Devices	AD2712	REF101	Voltage Reference	C/P
Analog Devices	AD3554	3554	Op Amp, Wide Bandwidth	P/P
Analog Devices	AD3860	DAC811	D/A Converter	C/P
Analog Devices	AD6012	DAC80	D/A Converter	C/P
Analog Devices	AD6012	DAC85H	D/A Converter	C/P
Analog Devices	AD6012	DAC87H	D/A Converter	C/P
Analog Devices	AD7501	HI-508A	MUX	F/E
Analog Devices	AD7501	MPC8S	MUX	F/E
Analog Devices	AD7502	HI-509A	MUX	F/E
Analog Devices	AD7502	MPC4D	MUX	F/E
Analog Devices	AD7506	HI-506A	MUX	P/P
Analog Devices	AD7506	MPC16S	MUX	P/P
Analog Devices	AD7507	HI-507A	MUX	P/P
Analog Devices	AD7507	MPC8D	MUX	P/P
Analog Devices	AD7521	DAC85H	D/A Converter	C/P
Analog Devices	AD7521	DAC7541A	D/A Converter	P/P
Analog Devices	AD7531	DAC85H	D/A Converter	C/P
Analog Devices	AD7531	DAC7541A	D/A Converter	P/P
Analog Devices	AD7541	DAC7541A	D/A Converter	P/P
Analog Devices	AD7542	DAC811	D/A Converter Latched	C/P
Analog Devices	AD7545	DAC7545	D/A Converter Latched	P/P
Analog Devices	AD7546	DAC706	D/A Converter Latched	F/E
Analog Devices	AD7546	DAC707	D/A Converter Latched	F/E
Analog Devices	AD7548	DAC811	D/A Converter Latched	C/P
Analog Devices	ADADC80	ADC80AG	A/D Converter	P/P
Analog Devices	ADADC84	ADC84	A/D Converter	P/P
Analog Devices	ADADC85	ADC85	A/D Converter	P/P
Analog Devices	ADC1103	ADC803	A/D Converter	F/E
Analog Devices	ADC1130	ADC71/72	A/D Converter	C/P
Analog Devices	ADC1131	ADC71/72	A/D Converter	C/P
Analog Devices	ADC1140	ADC71/72	A/D Converter	C/P
Analog Devices	ADC1140	ADC76	A/D Converter	C/P
Analog Devices	ADC1140	PCM75	A/D Converter	C/P
Analog Devices	ADLH0032	OPA605	Op Amp	C/P
Analog Devices	ADLH0033	OPA633	Voltage Buffer	F/E
Analog Devices	ADVFC32	VFC32	V/F Converter	P/P
Analog Devices	ADDAC71	DAC71	D/A Converter	P/P
Analog Devices	ADDAC71	DAC700/703	D/A Converter	P/P
Analog Devices	ADDAC72	DAC72	D/A Converter	P/P
Analog Devices	ADDAC72	DAC700/703	D/A Converter	P/P
Analog Devices	ADDAC80	DAC80	D/A Converter	P/P

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CROSS-REFERENCE INFORMATION

Company	Model	Burr-Brown Model[1]	Description	Equivalency[2]
Analog Devices	ADDAC80	DAC80P	D/A Converter	P/P
Analog Devices	ADDAC85	DAC85H	D/A Converter	P/P
Analog Devices	ADDAC87	DAC87H	D/A Converter	P/P
Analog Devices	CAV1210	ADC600	A/D Converter	F/E
Analog Devices	DAS1128	SDM856	Data Acq System	F/E
Analog Devices	DAS1128	SDM873	Data Acq System	F/E
Analog Devices	DAC1136	DAC729+0729MC	D/A Converter	P/P
Analog Devices	HAS-050	3554	Op Amp	C/P
Analog Devices	HAS-1202	ADC803	A/D Converter	F/E
Analog Devices	HAS-1202A	ADC803	A/D Converter	C/P
Analog Devices	HDS1240	DAC63	D/A Converter	F/E
Analog Devices	HOS-050	3554	Op Amp, Wide Bandwidth	C/P
Analog Devices	HOS-060	3554	Op Amp, Wide Bandwidth	C/P
Analog Devices	HOS-100	OPA633	Buffer Amp, Wide Bandwidth	P/P
Analog Devices	HOS-200	OPA633	Buffer Amp, Wide Bandwidth	F/E
Analog Devices	HT0025	SHC600	Sample/Hold	F/E
Analog Devices	HTC0300	SHC803	Sample/Hold	F/E
Analog Devices	HTC0300	SHC804	Sample/Hold	P/P
Analog Devices	HTS0010	SHC600	Sample/Hold	F/E
Analog Devices	SHA1A	SHC85	Sample/Hold	F/E
Analog Devices	SHA2A-5A	SHC804	Sample/Hold	F/E
Analog Devices	SHA2A-5A	SHM60	Sample/Hold	F/E
Analog Devices	SHA21	SHC803	Sample/Hold	F/E
Analog Devices	SHC85	SHC85	Sample/Hold	P/P
Analogic	MP1814	DAC70	D/A Converter	F/E
Analogic	MP1814	DAC700/703	D/A Converter	F/E
Analogic	MP1914	DAC70	D/A Converter	F/E
Analogic	MP1914	DAC700/703	D/A Converter	F/E
Analogic	MP6812	SDM863	Data Acq System	F/E
Analogic	MP6812	SDM856/857	Data Acq System	F/E
Analogic	MP6812	SDM873	Data Acq System	F/E
Analogic	MP8014	ADC76	A/D Converter	F/E
Analogic	MP8014	PCM75	A/D Converter	F/E
Analogic	MP8016	ADC76	A/D Converter	F/E
Analogic	MP8016	PCM75	A/D Converter	F/E
Analogic	MP8116	DAC729	D/A Converter	F/E
Analogic	MP8116	DAC729	D/A Converter	F/E
Analogic	MP8116	DAC729	D/A Converter	F/E
Apex	PA-01	OPA511	High Current O/A	P/P
Apex	PA-02	OPA541	Fast Power Op Amp	C/P
Apex	PA-07	OPA512	High Current O/A	C/P
Apex	PA-08	3583	High Voltage O/A	C/P
Apex	PA-10	OPA512	Power Op Amp, Low Power ver PA-12	F/E
Apex	PA-11	OPA511	High Current O/A	P/P
Apex	PA-12	OPA512	High Current O/A	P/P
Apex	PA-51	OPA501	High Current O/A	P/P
Apex	PA-61	OPA512	Power Op Amp, Higher V ver PA-51	C/P
Apex	PA-73	3573	High Current O/A	P/P
Apex	PA-80/1/2	3580/81/82	High Voltage Op Amp	P/P

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CROSS-REFERENCE INFORMATION

Company	Model	Burr-Brown Model[1]	Description	Equivalency[2]
Apex	PA83	3583	High Voltage O/A	P/P
Apex	PA84	3584	High Voltage O/A	P/P
Beckman	877-80	DAC80	D/A Converter	P/P
Beckman	877-85	DAC85H	D/A Converter	P/P
Beckman	877-85	DAC87H	D/A Converter	P/P
Beckman	7580	DAC80	D/A Converter	P/P
Calex	175	INA101	Inst Amp	F/E
Calex	176J	INA101	Inst Amp	F/E
Calex	176K	INA101	Inst Amp	F/E
Calex	176L	INA101	Inst Amp	F/E
Calex	178	INA101	Inst Amp	F/E
Datel	ADC-EH12B3	ADC803	A/D Converter	C/P
Datel	ADC-HX12B	ADC84/85H	A/D Converter	P/P
Datel	ADC511	ADC601	D/A Converter	F/E
Datel	ADC810/811	ADC803	A/D Converter	F/E
Datel	ADC817/827	ADC803	A/D Converter	F/E
Datel	DAC-71	DAC71	D/A Converter	P/P
Datel	DAC-71	DAC700/703	D/A Converter	P/P
Datel	DAC-72	DAC72	D/A Converter	P/P
Datel	DAC-72	DAC700/703	D/A Converter	P/P
Datel	DAC-HF12	DAC63	D/A Converter	F/E
Datel	DAC-HF12B	DAC812	D/A Converter	C/P
Datel	DAC-HK12B	DAC811	D/A Converter Latched	F/E
Datel	DAC-HP16	DAC71/72	D/A Converter	P/P
Datel	DAC-HP16	DAC701/703	D/A Converter	P/P
Datel	DAC-HY12	DAC80	D/A Converter	P/P
Datel	DAC-HZ12B	DAC85H/87H	D/A Converter	P/P
Datel	DAC612	DAC811	D/A Converter Latched	C/P
Datel	HDAS-8	SDM857	Data Acq System	F/E
Datel	HDAS-16	SDM857	Data Acq System	F/E
Datel	MDAS-8D	SDM854	Data Acq System	C/P
Datel	MDAS-8D	SDM856/857	Data Acq System	C/P
Datel	MDAS-8D	SDM873	Data Acq System	F/E
Datel	MDAS-16	SDM872	Data Acq System	C/P
Datel	MX-808	HI-508A	MUX	P/P
Datel	MX-808	MPC8S	MUX	P/P
Datel	MX-818	MPC801	MUX	P/P
Datel	MX-1606	MPC16S	MUX	P/P
Datel	MX1616	MPC800	MUX	P/P
Datel	MXD-409	HI-509A	MUX	P/P
Datel	MXD-409	MPC4D	MUX	P/P
Datel	MXD-807	HI-507A	MUX	P/P
Datel	MXD-807	MPC8D	MUX	P/P
Datel	SHM-6	SHC803/804	Sample/Hold	C/P
Datel	SHM-6	SHC5320	Sample/Hold	C/P
Datel	SHM-9	SHC85	Sample/Hold	C/P
Datel	SHM-9	SHC5320	Sample/Hold	C/P

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CROSS-REFERENCE INFORMATION

Company	Model	Burr-Brown Model[1]	Description	Equivalency[2]
Datel	SHM-20	SHC5320	Sample/Hold	P/P
Datel	SHM360/361	SHC601	Sample/Hold	F/E
Datel	SHM-4860	SHC803	Sample/Hold	C/P
Datel	SHM-4860	SHC804	Sample/Hold	P/P
Datel	SHM-HU	SHC803	Sample/Hold	C/P
Datel	SHM-HU	SHC804	Sample/Hold	C/P
Datel	SHM-HU	SHM60	Sample/Hold	C/P
Datel	SHM-IC-1	SHC298	Sample/Hold	C/P
Datel	SHM-IC-1	SHC5320	Sample/Hold	F/E
Datel	SHM-LM-2	SHC298	Sample/Hold	P/P
DDC	ADC00401	ADC803	A/D Converter	F/E
DDC	ADC00403	ADC803	A/D Converter	F/E
DDC	ADC4450	ADC803	A/D Converter	F/E
DDC	ADH-051	ADC803	A/D Converter	C/P
DDC	ADH8516	ADC803	A/D Converter	F/E
DDC	ADH8585	ADC85H	A/D Converter	P/P
DDC	ADH8586	ADC85H	A/D Converter	F/E
DDC	ADH8586	ADC87H	A/D Converter	F/E
DDC	DAC-S	DAC85H	D/A Converter Latched	P/P
DDC	DAC-SL	DAC811	D/A Converter Latched	F/E
DDC	DAC87	DAC87H	D/A Converter Latched	P/P
DDC	DAC02701	DAC811	D/A Converter Latched	F/E
DDC	THA-0523	SHC803	Sample/Hold	F/E
DDC	THA-0523	SHC804	Sample/Hold	P/P
Elantek	EL2003	OPA633	Voltage Buffer	P/P
Elantek	EL2007	OPA541	Fast Power Amp	C/P
Harris	HA-2400	OPA201	Op Amp	C/P
Harris	HA-2420	SHC5320	Sample/Hold	C/P
Harris	HA-2425	SHC5320	Sample/Hold	C/P
Harris	HA-2500	3507	Op Amp	F/E
Harris	HA-2510	3507	Op Amp	F/E
Harris	HA-2520	3507	Op Amp	P/P
Harris	HA-2539	OPA605	Op Amp	C/P
Harris	HA-2540	OPA605	Op Amp	C/P
Harris	HA-2541	OPA605	Op Amp	C/P
Harris	HA-2542	OPA605	Op Amp	C/P
Harris	HA-2600	3507	Op Amp	C/P
Harris	HA-2620	3508	Op Amp	P/P
Harris	HA-2630	3553	Buffer	C/P
Harris	HA-2640/45	OPA445	Op Amp, High Voltage, Low Current	C/P
Harris	HA-2650	OPA2111	Op Amp	C/P
Harris	HA-4156	OPA404	Op Amp	C/P
Harris	HA-4741	OPA404	Op Amp	C/P
Harris	HA-5002	OPA633	Voltage Buffer	C/P
Harris	HA-5033	OPA633	Voltage Buffer	P/P
Harris	HA-5062	OPA2111	Op Amp	C/P
Harris	HA-5064	OPA404	Op Amp	F/E
Harris	HA-5082	OPA2111	Op Amp	F/E

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CROSS-REFERENCE INFORMATION

Company	Model	Burr-Brown Model[1]	Description	Equivalency[2]
Harris	HA-5084	OPA404	Op Amp	F/E
Harris	HA-5100	OPA606	Op Amp	C/P
Harris	HA-5102	OPA2111	Op Amp	C/P
Harris	HA-5104	OPA404	Op Amp	F/E
Harris	HA-5110	3551	Op Amp	F/E
Harris	HA-5112	OPA2111	Op Amp	C/P
Harris	HA-5114	OPA404	Op Amp	F/E
Harris	HA-513/-35	OPA27	Op Amp	F/E
Harris	HA-5141	OPA21	Op Amp	C/P
Harris	HA-5142	OPA2111	Op Amp	C/P
Harris	HA-5144	OPA404	Op Amp	C/P
Harris	HA-5147	OPA37	Op Amp	F/E
Harris	HA-5160	OPA602	Op Amp, Fast FET	F/E
Harris	HA-5170	OPA111	Op Amp	F/E
Harris	HA-5180	OPA111	Op Amp	P/P
Harris	HA-5190	OPA605	Op Amp	C/P
Harris	HA-5320	SHC5320	Sample/Hold	P/P
Harris	HA-5330	SHC803	Sample/Hold	C/P
Harris	HA-OP07	OPA27	Op Amp	F/E
Harris	HA-OP27	OPA27	Op Amp	P/P
Harris	HA-OP37	OPA37	Op Amp	P/P
Harris	HI-506	HI-506A	MUX	P/P
Harris	HI-506	MPC16S	MUX	P/P
Harris	HI-507	HI-507A	MUX	P/P
Harris	HI-507	MPC8D	MUX	P/P
Harris	HI-508	HI-508A	MUX	P/P
Harris	HI-508	MPC8S	MUX	P/P
Harris	HI-509	HI-509A	MUX	P/P
Harris	HI-509	MPC4D	MUX	P/P
Harris	HI-516	MPC800	MUX	P/P
Harris	HI-518	MPC801	MUX	P/P
Harris	HI-574A	ADC574A	A/D Converter	P/P
Harris	HI-674A	ADC674A	A/D Converter	P/P
Harris	HI-5660	DAC80	D/A Converter	C/P
Harris	HI-5660	DAC85H/87H	D/A Converter	C/P
Harris	HI-5680	DAC80	D/A Converter	P/P
Harris	HI-5680	DAC80	D/A Converter	P/P
Harris	HI-5685	DAC85H	D/A Converter	P/P
Harris	HI-5687	DAC87H	D/A Converter	P/P
Harris	HI-5690	DAC80	D/A Converter	C/P
Harris	HI-5695	DAC85H/87H	D/A Converter	C/P
Harris	HI-5811	DAC811	D/A Converter	P/P
Harris	HI-DAC16	DAC71/72	D/A Converter	F/E
Harris	HI-DAC16	DAC700/703	D/A Converter	F/E
Harris	LF353	OPA2111	Op Amp	P/P
Harris	LM118	3507	Op Amp	C/P
Hybrid	DAC331	DAC7541A	D/A Converter	F/E
Hybrid	DAC336-12	DAC811	D/A Converter Latched	F/E

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Company	Model	Burr-Brown Model[1]	Description	Equivalency[2]
Hybrid	DAC347	DAC7541A	D/A Converter	F/E
Hybrid	DAC377	DAC729	D/A Converter	C/P
Hybrid	DAC391	DAC812	D/A Converter	C/P
Hybrid	DAC9332-16	DAC708/709	D/A Converter Latched	F/E
Hybrid	DAC9349	DAC80	D/A Converter	C/P
Hybrid	DAC9377	DAC705/707	D/A Converter Latched	F/E
Hybrid	HS346	SHC85	Sample/Hold	C/P
Hybrid	HS346	SHC5320	Sample/Hold	C/P
Hybrid	HS3120	DAC811	D/A Converter Latched	F/E
Hybrid	HS3160	DAC700/703	D/A Converter	C/P
Hybrid	HS3860	DAC811	D/A Converter Latched	F/E
Hybrid	HS7541	DAC7541A	D/A Converter	P/P
Hybrid	HS7545	DAC7545	D/A Converter Latched	P/P
Hybrid	HS9338	DAC811	D/A Converter Latched	F/E
Hybrid	HS9377	DAC707	D/A Converter Latched	F/E
Hybrid	HS9378	DAC707	D/A Converter Latched	F/E
Hybrid	HS9410	SDM872	Data Acq System	C/P
Hybrid	HS9576	ADC76	A/D Converter	P/P
Hybrid	HSDAC80	DAC80	D/A Converter	P/P
Hybrid	HSDAC87	DAC87H	D/A Converter	P/P
Hybrid	HSDAC87	DAC811	D/A Converter	F/E
Hytek	HY6110	PGA200	Precision Prog Gain Amp	C/P
Hytek	HY6110	PGA100/102	Precision Prog Gain Amp	C/P
Intech	AD1201	ADC601	A/D Converter	F/E
Intersil	AD7521	DAC7541A	D/A Converter	P/P
Intersil	AD7531	DAC7541A	D/A Converter	P/P
Intersil	AD7541	DAC7541A	D/A Converter	P/P
Intersil	ICH8515	OPA541	Power Op Amp	C/P
Intersil	ICL7134	DAC708/709	D/A Converter Latched	C/P
Intersil	ICL7145	DAC705/707	D/A Converter Latched	C/P
Intersil	ICL7146	DAC811	D/A Converter Latched	C/P
Intersil	ICL7605/06	INA102	Precision Inst Amp	F/E
Intersil	ICL7605/06	INA101	Precision Inst Amp	F/E
Intersil	IH5108	HI-508A	MUX	P/P
Intersil	IH5108	MPC8S	MUX	P/P
Intersil	IH5108	MPC801	MUX	F/E
Intersil	IH5110-15	SHC298	Sample/Hold	C/P
Intersil	IH5208	HI-507A	MUX	P/P
Intersil	IH5208	MPC4D	MUX	P/P
Intersil	IH5208	MPC801	MUX	F/E
Intersil	IH6108	HI-508A	MUX	P/P
Intersil	IH6108	MPC8S	MUX	P/P
Intersil	IH6108	MPC801	MUX	F/E
Intersil	IH6116	HI-506A	MUX	P/P
Intersil	IH6116	MPC16S	MUX	P/P
Intersil	IH6116	MPC800	MUX	F/E

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CROSS-REFERENCE INFORMATION

Company	Model	Burr-Brown Model[1]	Description	Equivalency[2]
Intersil	IH6216	HI-507A	MUX	P/P
Intersil	IH6216	MPC8D	MUX	P/P
LTC	LF155A	OPA156A	Op Amp	P/P
LTC	LF156A	OPA156A	Op Amp	P/P
LTC	LH2108A	OPA2111	Op Amp	C/P
LTC	LM101A	3510	Op Amp	C/P
LTC	LM107	3510	Op Amp	C/P
LTC	LM108	OPA21	Op Amp	C/P
LTC	LM118	3507	Op Amp	F/E
LTC	LT118A	3507	Op Amp	F/E
LTC	LT1001	OPA27	Op Amp	F/E
LTC	LT1002	OPA2111	Op Amp	C/P
LTC	LT1007	OPA27	Op Amp	P/P
LTC	LT1008	OPA21	Op Amp	C/P
LTC	LT1010	OPA633	Voltage Buffer	C/P
LTC	LT1012	OPA21	Op Amp	C/P
LTC	LT1013	OPA2111	Op Amp	C/P
LTC	LT1014	OPA404	Quad Op Amp	C/P
LTC	LT1019XX-10	REF10	Voltage Reference	C/P
LTC	LT1021	REF10	Voltage Reference	F/E
LTC	LT1022	OPA606	Op Amp	P/P
LTC	LT1023	OPA606	Op Amp	C/P
LTC	LT1024	OPA2111	Op Amp	C/P
LTC	LT1028	OPA27	Op Amp	
LTC	LT1037	OPA37	Op Amp	P/P
LTC	LT1055	OPA606	Op Amp	P/P
LTC	LT1056	OPA606	Op Amp	P/P
LTC	LT1057	OPA2111	Dual Op Amp, FET	C/P
LTC	LT1058	OPA404	Quad Op Amp, FET	F/E
LTC	OP 05	OPA27	Op Amp	F/E
LTC	OP 07	OPA27	Op Amp	F/E
LTC	OP 15	OPA606	Op Amp	P/P
LTC	OP 16	OPA606	Op Amp	P/P
LTC	OP 27	OPA27	Op Amp	P/P
LTC	OP 37	OPA37	Op Amp	P/P
LTC	OP 227	OPA2111	Op Amp	C/P
LTC	OP 237	OPA2111	Op Amp	C/P
LTC	REF-01	REF10	Voltage Reference	F/E
Maxim	AD565	DAC80	D/A Converter	C/P
Maxim	AD7521	DAC7541A	D/A Converter	P/P
Maxim	AD7531	DAC7541A	D/A Converter	P/P
Maxim	AD7541	DAC7541A	D/A Converter	P/P
Maxim	AD7541A	DAC7541A	D/A Converter	P/P
Maxim	AD7545	DAC7545	D/A Converter	P/P
Maxim	AM6012	DAC80	D/A Converter	C/P
Maxim	BB3553	3553	Voltage Buffer	P/P
Maxim	BB3554	3554	Op Amp, Wide Bandwidth	P/P
Maxim	HI-0508	HI-508A	MUX	P/P

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CROSS-REFERENCE INFORMATION

Company	Model	Burr-Brown Model[1]	Description	Equivalency[2]
Maxim	HI-0509	HI-508A	MUX	P/P
Maxim	LH0101	OPA541	Power Op Amp	C/P
Maxim	MAX358	HI-508A	MUX	P/P
Maxim	MAX359	HI-509A	MUX	P/P
Micro Networks	DACHK	DAC811	D/A Converter Latched	F/E
Micro Networks	MN0300A	SHC803/804	Sample/Hold	F/E
Micro Networks	MN375/376	SHC803/804	Sample/Hold	F/E
Micro Networks	MN379	SHC600	Sample/Hold	F/E
Micro Networks	MN574A	ADC574A	A/D Converter	P/P
Micro Networks	MN2020	PGA100/102	Precision Prog Gain AMP	C/P
Micro Networks	MN2020	PGA200	Precision Prog Gain AMP	C/P
Micro Networks	MN3300	DAC71/72	D/A Converter	P/P
Micro Networks	MN3300	DAC700/703	D/A Converter	P/P
Micro Networks	MN3310	DAC71/72	D/A Converter	P/P
Micro Networks	MN3310	DAC700/703	D/A Converter	P/P
Micro Networks	MN3660	DAC811	D/A Converter Latched	C/P
Micro Networks	MN3850	DAC85H/87H	D/A Converter	P/P
Micro Networks	MN3860	DAC811	D/A Converter Latched	F/E
Micro Networks	MN5200	ADC84/85H	A/D Converter	F/E
Micro Networks	MN5210-14	ADC84/85	A/D Converter	F/E
Micro Networks	MN5245	ADC803	A/D Converter	F/E
Micro Networks	MN5245/46	ADC601	A/D Converter	F/E
Micro Networks	MN5280/82	ADC71/72	A/D Converter	C/P
Micro Networks	MN5290/91	ADC76	A/D Converter	C/P
Micro Networks	MN5610	ADC84/85H	A/D Converter	F/E
Micro Networks	MN7100	SDM872	Data Acq System	F/E
Micro Networks	MN7130	MP22/32	Microperipheral	F/E
Micro Networks	MN7150	SDM873	Data Acq System	F/E
Micro Networks	MN7150	SDM872	Data Acq System	F/E
Micro Networks	MNADC80	ADC80	A/D Converter	P/P
Micro Networks	MNADC84/85	ADC84/85H	A/D Converter	P/P
Micro Networks	MNADC87	ADC87H	A/D Converter	P/P
Micro Networks	MNDAC80	DAC80	D/A Converter	P/P
Micro Networks	MNDAC80	DAC800	D/A Converter	P/P
Micro Networks	MNDAC85	DAC85H/87H	D/A Converter	P/P
Micro Networks	MNDAC87	DAC87H	D/A Converter	P/P
Micro Networks	MNDAC88	DAC811	D/A Converter Latched	F/E
Micro Power Systems	MP574	ADC574A	A/D Converter	P/P
Micro Power Systems	MP7506	HI-506A	MUX	P/P
Micro Power Systems	MP7506	MPC16S	MUX	P/P
Micro Power Systems	MP7507	HI-507A	MUX	P/P
Micro Power Systems	MP7507	MPC8D	MUX	P/P
Micro Power Systems	MP7508	HI-508A	MUX	P/P
Micro Power Systems	MP7508	MPC8S	MUX	P/P
Micro Power Systems	MP7509	HI-509A	MUX	P/P
Micro Power Systems	MP7509	MPC4D	MUX	P/P
Micro Power Systems	MP7531	DAC7541A	D/A Converter	P/P

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CROSS-REFERENCE INFORMATION

Company	Model	Burr-Brown Model[1]	Description	Equivalency[2]
Micro Power Systems	MP7541A	DAC7541A	D/A Converter	P/P
Micro Power Systems	MP7542	DAC7545	D/A Converter Latched	C/P
Micro Power Systems	MP7545	DAC7541A	D/A Converter	P/P
Micro Power Systems	MP7616	DAC700/703	D/A Converter	C/P
Micro Power Systems	MP7621	DAC7541A	D/A Converter	P/P
Micro Power Systems	MP7622	DAC7545	D/A Converter Latched	C/P
Micro Power Systems	MP7623	DAC7541A	D/A Converter	P/P
Micro Power Systems	MP9331-16	DAC708/709	D/A Converter Latched	F/E
Micro Power Systems	MP9377-16	DAC705/707	D/A Converter Latched	F/E
Micro Power Systems	REF10	REF10	Voltage Reference	P/P
National Semiconductor	AD7521	DAC7541A	D/A Converter	P/P
National Semiconductor	AD7531	DAC7541A	D/A Converter	P/P
National Semiconductor	ADC1080	ADC80	A/D Converter	P/P
National Semiconductor	ADC1280	ADC80	A/D Converter	P/P
National Semiconductor	DAC1208	DAC811	D/A Converter Latched	F/E
National Semiconductor	DAC1218	DAC7541A	D/A Converter	F/E
National Semiconductor	DAC1219	DAC7541A	D/A Converter	F/E
National Semiconductor	DAC1230	DAC811	D/A Converter Latched	F/E
National Semiconductor	DAC1280	DAC80	D/A Converter	P/P
National Semiconductor	DAC1280	DAC80	D/A Converter	P/P
National Semiconductor	DAC1285	DAC85H/87H	D/A Converter	P/P
National Semiconductor	DAC1286	DAC80	D/A Converter	P/P
National Semiconductor	DAC1287	DAC85H/87H	D/A Converter	P/P
National Semiconductor	LF155A	OPA156A	Op Amp	P/P
National Semiconductor	LF156A	OPA156A	Op Amp	P/P
National Semiconductor	LF157A	OPA606	Op Amp	F/E
National Semiconductor	LF198-398	SHC298	Sample/Hold	P/P
National Semiconductor	LF351	OPA156A	Op Amp	P/P
National Semiconductor	LF353	OPA2111	Op Amp	C/P
National Semiconductor	LF400C	OPA606	Op Amp	F/E
National Semiconductor	LF411	OPA602	Op Amp	P/P
National Semiconductor	LF412A	OPA2111	Op Amp	F/E
National Semiconductor	LF441A	OPA121	Op Amp	F/E
National Semiconductor	LF442A	OPA2111	Op Amp	F/E
National Semiconductor	LF444A	OPA404	Op Amp	P/P
National Semiconductor	LF11508	HI-508A	MUX	P/P
National Semiconductor	LF11509	HI-509A	MUX	P/P
National Semiconductor	LF13741	OPA121	Op Amp	P/P
National Semiconductor	LH0002	3553	Buffer	C/P
National Semiconductor	LH0003	3507	Op Amp	C/P
National Semiconductor	LH0004	3580	Op Amp	C/P
National Semiconductor	LH0005	OPA605	Op Amp	C/P
National Semiconductor	LH0022	OPA121	Op Amp	P/P
National Semiconductor	LH0023	SHC298	Sample/Hold	C/P
National Semiconductor	LH0024	3551	Op Amp	F/E
National Semiconductor	LH0032	OPA605	Op Amp	C/P
National Semiconductor	LH0033	OPA633	Voltage Buffer	F/E
National Semiconductor	LH0042	OPA121	Op Amp	P/P
National Semiconductor	LH0043	SHC298	Sample/Hold	C/P

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CROSS-REFERENCE INFORMATION

Company	Model	Burr-Brown Model[1]	Description	Equivalency[2]
National Semiconductor	LH0044	OPA27	Op Amp	F/E
National Semiconductor	LH0052	OPA111	Op Amp	P/P
National Semiconductor	LH0053	SHC85	Sample/Hold	F/E
National Semiconductor	LH0053	SHC5320	Sample/Hold	C/P
National Semiconductor	LH0063	3553	Op Amp	F/E
National Semiconductor	LH0084	PGA200/201	Precision Prog Gain AMP	F/E
National Semiconductor	LH0086	PGA100/102	Precision Prog Gain AMP	F/E
National Semiconductor	LH0101	OPA541	High-Current Op Amp	C/P
National Semiconductor	LH740A	OPA121	Op Amp	P/P
National Semiconductor	LH2011	OPA2111	Op Amp	C/P
National Semiconductor	LH2101A	OPA2111	Op Amp	C/P
National Semiconductor	LH2108A	OPA2111	Op Amp	C/P
National Semiconductor	LH4001	OPA633	Voltage Buffer	C/P
National Semiconductor	LM11	OPA21	Op Amp	C/P
National Semiconductor	LM12	OPA541	High Current Op Amp	C/P
National Semiconductor	LM101A	3510	Op Amp	C/P
National Semiconductor	LM107	3510	Op Amp	C/P
National Semiconductor	LM108A	OPA21	Op Amp	C/P
National Semiconductor	LM112	3510	Op Amp	C/P
National Semiconductor	LM118	3507	Op Amp	C/P
National Semiconductor	LM131/331	VFC32	V/F Converter	C/P
National Semiconductor	LM143	3580	Op Amp	C/P
National Semiconductor	LM144	3580	Op Amp	C/P
National Semiconductor	LM158A/358	OPA2111	Op Amp	C/P
National Semiconductor	LM163	INA101	Precision Inst Amp	F/E
National Semiconductor	LM163	INA102	Precision Inst Amp	F/E
National Semiconductor	LM216A	OPA21	Op Amp	C/P
National Semiconductor	LM363	INA101HP	Precision Inst Amp	F/E
National Semiconductor	LM607	OPA27/37	Op Amp	C/P
National Semiconductor	LM675	OPA511	High Current Op Amp	C/P
National Semiconductor	LM709A	3507	Op Amp	C/P
National Semiconductor	LM725A	3510	Op Amp	F/E
National Semiconductor	LM747A	OPA2111	Op Amp	C/P
National Semiconductor	LM748	3510	Op Amp	C/P
National Semiconductor	LM837	OPA404	Op Amp, Quad	C/P
National Semiconductor	LM1558	OPA2111	Op Amp	C/P
National Semiconductor	LM2904	OPA2111	Op Amp	C/P
National Semiconductor	LMC660	OPA404	CMOS Quad	C/P
PMI	AMP-01	INA101	Precision Inst Amp	F/E
PMI	AMP-01	INA102	Precision Inst Amp	F/E
PMI	AMP-05	INA110	Precision Inst Amp	F/E
PMI	MUX08	HI-508A	MUX	P/P
PMI	MUX08	MPC8S	MUX	P/P
PMI	MUX16	HI-506A	MUX	P/P
PMI	MUX16	MPC16S	MUX	P/P
PMI	MUX24	HI-509A	MUX	P/P
PMI	MUX24	MPC4D	MUX	P/P
PMI	MUX28	HI-507A	MUX	P/P

NOTES: (1) See Model Index, inside front cover. (2) P/P = Pin for Pin. A true second source. F/E = Functional Equivalent. Very similar function and performance, but not pin for pin. C/P = Closest Part. Similar function and performance, with significant differences.

CROSS-REFERENCE INFORMATION

Company	Model	Burr-Brown Model[1]	Description	Equivalency[2]
PMI	MUX28	MPC8D	MUX	P/P
PMI	OP-01	OPA606	Op Amp	C/P
PMI	OP-04	OPA2111	Op Amp	C/P
PMI	OP-05	OPA27	Op Amp	F/E
PMI	OP-06	OPA37	Op Amp	C/P
PMI	OP-07	OPA27	Op Amp	F/E
PMI	OP-08	OPA111	Op Amp	C/P
PMI	OP-10	OPA2111	Op Amp	C/P
PMI	OP-12	OPA21	Op Amp	F/E
PMI	OP-14	OPA2111	Op Amp	C/P
PMI	OP-15	OPA606	Op Amp	P/P
PMI	OP-16	OPA606	Op Amp	P/P
PMI	OP-17	OPA606	Op Amp	F/E
PMI	OP-20	OPA21	Op Amp	C/P
PMI	OP-21	OPA21	Op Amp	P/P
PMI	OP-27	OPA27	Op Amp	P/P
PMI	OP-37	OPA37	Op Amp	P/P
PMI	OP-41	OPA111	Op Amp, FET	F/E
PMI	OP-42	OPA602	FET Op Amp, Fast	F/E
PMI	OP-43	OPA111	Op Amp, FET	F/E
PMI	OP-50	OPA27	Op Amp	C/P
PMI	OP-77	OPA27	Op Amp, Precision Bipolar	C/P
PMI	OP-80	OPA128	Op Amp, Electrometer FET	F/E
PMI	OP-90	OPA21	Op Amp, Micropower	C/P
PMI	OP-207	OPA2111	Op Amp	C/P
PMI	OP-215	OPA2111	Op Amp	C/P
PMI	OP-220	OPA2111	Op Amp	C/P
PMI	OP-221	OPA2111	Op Amp, Dual Low Power	C/P
PMI	OP-227	OPA2111	Op Amp, Dual OP-27	C/P
PMI	OP-400	OPA404	Quad Op Amp	C/P
PMI	OP-420	OPA404	Op Amp, Quad Low Power	C/P
PMI	OP-421	OPA404	Op Amp, Quad Low Power	C/P
PMI	OP-470	OPA404	Quad Low Noise Op Amp	C/P
PMI	PM108A	OPA21	Op Amp	F/E
PMI	PM155A	OPA156A	Op Amp	P/P
PMI	PM156A	OPA156A	Op Amp	P/P
PMI	PM157A	OPA606	Op Amp	F/E
PMI	PM725	OPA27	Op Amp	F/E
PMI	PM747	OPA2111	Op Amp	C/P
PMI	PM2108A	OPA2111	Op Amp	C/P
PMI	PM7541	DAC7541A	D/A	P/P
PMI	PM7545	DAC7545	D/A	P/P
PMI	PM8012	DAC8012	D/A	P/P
PMI	REF10	REF10	Voltage Reference	P/P
PMI	SMP-10	SHC298	Sample/Hold	F/E
PMI	SMP-11	SHC298	Sample/Hold	F/E
PMI	SMP-81	SHC5320	Sample/Hold	C/P
Raytheon	LM101A	3510	Op Amp	C/P

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Company	Model	Burr-Brown Model[1]	Description	Equivalency[2]
Raytheon	LM358	OPA2111	Op Amp	C/P
Raytheon	OP-05	OPA27	Op Amp	F/E
Raytheon	OP-07	OPA27	Op Amp	F/E
Raytheon	OP-27	OPA27	Op Amp	P/P
Raytheon	OP-37	OPA37	Op Amp	P/P
Raytheon	OP-47	OPA37	Op Amp	F/E
Raytheon	RC714	OPA27	Op Amp	P/P
Raytheon	RC747	OPA2111	Op Amp	C/P
Raytheon	RC1458	OPA2111	Op Amp	C/P
Raytheon	RC2041	OPA2111	Op Amp	C/P
Raytheon	RC2043	OPA2111	Op Amp	C/P
Raytheon	RC3078	OPA21	Op Amp	C/P
Raytheon	RC4136	OPA404	Op Amp	C/P
Raytheon	RC4153	VFC320	V/F Converter	C/P
Raytheon	RC4156	OPA404	Op Amp	C/P
Raytheon	RC4558	OPA2111	Op Amp	C/P
Raytheon	RC4559	OPA2111	Op Amp	C/P
Raytheon	RC4560	OPA2111	Op Amp	C/P
Raytheon	RC4562	OPA2111	Op Amp	C/P
Raytheon	RC4739	OPA2111	Op Amp	C/P
Raytheon	RC5532	OPA2111	Op Amp	C/P
Raytheon	RC5534	OPA37	Op Amp	F/E
Siliconix	DG506	HI-506A	MUX	P/P
Siliconix	DG506	MPC16S	MUX	P/P
Siliconix	DG507	HI-507A	MUX	P/P
Siliconix	DG507	MPC8D	MUX	P/P
Siliconix	DG508	HI-508A	MUX	P/P
Siliconix	DG508	MPC8S	MUX	P/P
Siliconix	DG509	HI-509A	MUX	P/P
Siliconix	DG509	MPC4D	MUX	P/P
Sprague	VLN-3755	OPA2541	Power Op Amp, Dual	C/P
Teledyne-Philbrick	1480	3583	High Voltage O/A	P/P
Teledyne-Philbrick	TP4002	DAC71/72H	D/A Converter	F/E
Teledyne-Philbrick	TP4002	DAC701/703	D/A Converter	F/E
Teledyne-Philbrick	TP4160	ADC10HT	A/D Converter	F/E
Teledyne-Philbrick	TP4855	SHC803	Sample/Hold	F/E
Teledyne-Philbrick	TP4860	SHC803	Sample/Hold	F/E
Teledyne-Philbrick	TP4860	SHC804	Sample/Hold	P/P
Teledyne-Philbrick	TPADC85	ADC84/85H	A/D Converter	P/P
Teledyne-Philbrick	TPADC87	ADC87H	A/D Converter	P/P
VTC	VA033	OPA633	Voltage Buffer, Wideband	P/P
Zeltex	ADA160Q	DAC729	D/A Converter	F/E
Zeltex	ZAD354	DAC71/72	D/A Converter	F/E
Zeltex	ZAD7100	ADC803	A/D Converter	F/E
Zeltex	ZAD7400	ADC76	A/D Converter	F/E
Zeltex	ZAD8000	DAC70BH	D/A Converter	F/E
Zeltex	ZAD8000	DAC700/702	D/A Converter	F/E

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CROSS-REFERENCE INFORMATION

Company	Model	Burr-Brown Model[1]	Description	Equivalency[2]
Zeltex	ZD354	DAC71/72	D/A Converter	F/E
Zeltex	ZD354	DAC700/702	D/A Converter	F/E
Zeltex	ZD364	DAC71/72	D/A Converter	F/E
Zeltex	ZD364	DAC701/703	D/A Converter	F/E
Zeltex	ZD384	DAC71/72	D/A Converter	F/E
Zeltex	ZD384	DAC701/703	D/A Converter	F/E
Zeltex	ZD394	DAC71/72	D/A Converter	F/E
Zeltex	ZD394	DAC701/703	D/A Converter	F/E
Zeltex	ZDA160	DAC729	D/A Converter	F/E

NOTES: (1) See Model Index, inside front cover. (2) P/P = Pin for Pin. A true second source. F/E = Functional Equivalent. Very similar function and performance, but not pin for pin. C/P = Closest Part. Similar function and performance, with significant differences.

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