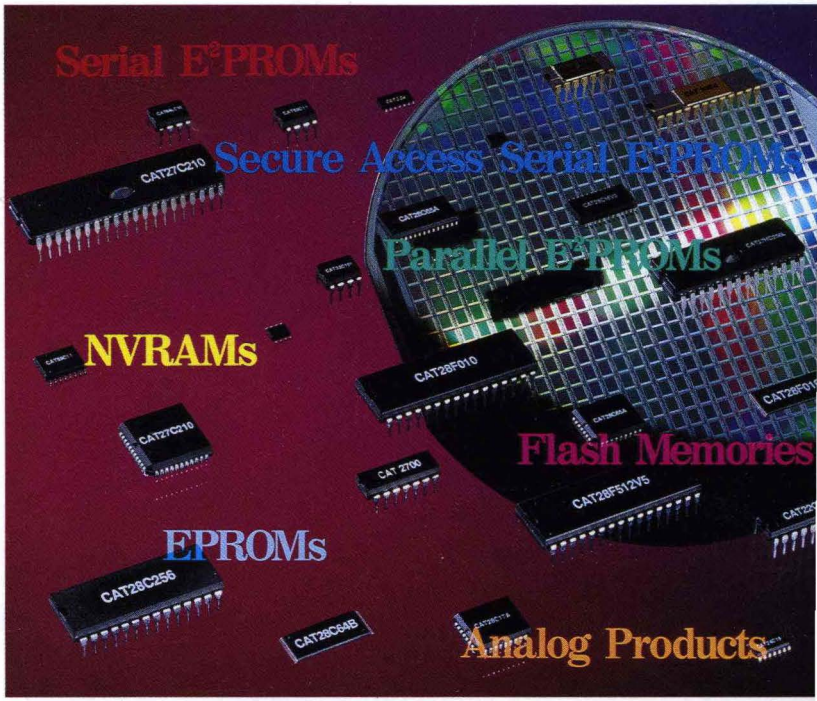
CATALYST SEMICONDUCTOR

Data Book 92/93

92/93 Data Book



CATALYST SEMICONDUCTOR

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92/93 Data Book

Corporate Message

Catalyst Semiconductor, Inc. is a technology leader in CMOS nonvolatile memories and is dedicated to the development of next generation memory products and their applications.

The Catalyst Corporate Mission Statement is:

- Use state of the art nonvolatile memory technology to produce innovative leading edge products and obtain a leadership position in all reprogrammable product markets.
- Adopt a global manufacturing strategy by using strategic partners to produce cost-effective, high quality products.
- Provide excellent service to customers worldwide and enter into mutually beneficial, long-term partnership agreements.

Catalyst Semiconductor is in the business of providing integrated circuits which enhance your electronic systems' performance, thereby giving you a competitive edge in your marketplace. In our view, you, our customer, have not simply purchased ICs; you've secured our commitment to your company and your business. Since our inception in 1985, we have found that relationships based on this commitment result in the development of trust, support and mutual prosperity. Such is the foundation of long-term corporate partnerships, and these are what the future of Catalyst is being designed to secure.

Thank you for considering Catalyst memory products.

David W. Sear
President & C.O.O.

B.K. Marya
Chairman of the Board & C.E.O.

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Product Selection Guide

SERIAL E²PROMs

2-Wire Bus Structure (Data Book Section 2)

Device	Temp. Range	Compatibility	Size (Organization)	I_{CC} (Max/ Standby)	Max Clock Freq.	# Pins	Pkg Types	Voltage
CAT24C02	C, I	Xicor	2K Bit (256 x 8)	3mA/4µA	100kHz	8 14	P, J J	5 V
CAT24LC02	C, I	Xicor	2K Bit (256 x 8)	3mA/4µA	100kHz	8 14	P, J J	3–6 V
CAT24C02A	C, I	Xicor	2K Bit (256 x 8)	3mA/4µA	100kHz	8 14	P, J J	5 V
CAT24LC02A	C, I	Xicor	2K Bit (256 x 8)	3mA/4µA	100kHz	8 14	P, J J	3–6 V
CAT24C04	C, I	Xicor	4K Bit (512 x 8)	3mA/4µA	100kHz	8 14	P, J J	5 V
CAT24LC04	C, I	Xicor	4K Bit (512 x 8)	3mA/4µA	100kHz	8 14	P, J J	3–6 V
CAT24C08	C, I	Xicor	8K Bit (1024 x 8)	3mA/4µA	100kHz	8 14	P, J J	5 V
CAT24LC08	C, I	Xicor	8K Bit (1024 x 8)	3mA/4µA	100kHz	8 14	P, J J	3–6 V
CAT24C16	C, I	Xicor	16K Bit (2048 x 8)	3mA/4µA	100kHz	8 14	P, J J	5 V
CAT24LC16	C, I	Xicor	16K Bit (2048 x 8)	3mA/4µA	100kHz	8 14	P, J J	3–6 V
CAT24C32	C, I	Xicor 24C16 UPGRADE	32K Bit (4096 x 8)	3mA/4µA	100kHz	8 14	P J	5 V

Note:
(1) All I²C devices offered in ZERO Power™ (I_{SBZ} = 0µA) version.
(2) Catalyst Semiconductor is licenced by Philips Corporation to carry the I²C Bus Protocol.
(3) All Serial E²PROMs offered in High Endurance Version ("H").
(4) For information on military temperature devices, please contact the factory.

SERIAL E²PROMs

3-Wire Bus Structure (Data Book Section 3)

Device	Temp. Range	Compatibility	Size (Organization)	I_{CC} (Max/ Standby)	Max Clock Freq.	# Pins	Pkg Types	Voltage
CAT93C46A	C, I	National 93C46	1K Bit (64x16)	3mA/100µA	1MHz	8	P, K, J, S	5 V
CAT93C46B	C, I	National 93C46	1K Bit (x8 or x16)	3mA/100µA	1MHz	8	P, K, J, S	5 V
CAT93C46	C, I	National 93C46	1K Bit (x8 or x16)	3mA/100µA	1MHz	8	P, K, J, S	5 V
CAT33C101	C, I	National 93C46 UPGRADE	1K Bit (x8 or x16)	2mA/50µA	250kHz	8	P, K, J, S	3 V
CAT32C101	C	National 93C46 UPGRADE	1K Bit (x8 or x16)	2mA/2µA	250kHz	8	P, K, J	2.2 V
CAT93C56	C, I	National 93C56	2K Bit (x8 or x16)	3mA/100µA	1MHz	8	P, K, S	5 V
CAT93LC56	C, I	National 93C56 UPGRADE	2K Bit (x8 or x16)	2mA/50µA	250kHz	8	P, K, S	3 V
CAT35C102	C, I	National 93C46 UPGRADE	2K Bit (x8 or x16)	3mA/100µA	1MHz	8	P, K, S	5 V
CAT33C104	C, I	National 93C66 UPGRADE	4K Bit (x8 or x16)	2mA/50µA	250kHz	8	P, K, S	3 V
CAT35C104	C, I	National 93C66	4K Bit (x8 or x16)	3mA/100µA	1MHz	8	P, K, S	5 V
CAT33C108	C I	National 93C66 UPGRADE	8K Bit (x8 or x16)	2mA/10µA 3mA/10µA	1MHz	8	P, K, S	3 V
CAT35C108	C I	National 93C66 UPGRADE	8K Bit (x8 or x16)	3mA/10µA 4mA/10µA	3MHz	8	P, K, S	5 V
CAT33C116	C I	National 93C66 UPGRADE	16K Bit (x8 or x16)	2mA/10µA 3mA/10µA	1MHz	8	P, K, S	3 V
CAT35C116	C I	National 93C66 UPGRADE	16K Bit (x8 or x16)	3mA/10µA 4mA/10µA	3MHz	8	P, K, S	5 V

SERIAL E²PROMs

SPI Bus Structure (Data Book Section 4)

Device	Temp. Range	Compatibility	Size (Organization)	I_{CC} (Max/ Standby)	Max Clock Freq.	# Pins	Pkg Types	Voltage
CAT64LC10	C, I	Asahi	1K Bit (64 x 16)	1mA/3µA	1MHz	8	P, J, S	2.5–5.5 V
CAT64LC20	C, I	Asahi	2K Bit (128 x 16)	1mA/3µA	1MHz	8	P, J, S	2.5–5.5 V
CAT64LC40	C, I	Asahi	4K Bit (256 x 16)	1mA/3µA	1MHz	8	P, J, S	2.5–5.5 V

Note:
(1) All SPI devices offered in ZERO Power™ (I_{SBZ} = 0µA) Version.
(2) All Serial E²PROMs offered in High Endurance Version ("H").
(3) For information on military temperature devices, please contact the factory.

SERIAL E²PROMs

4-Wire Bus Structure (Data Book Section 5)

Device	Temp. Range	Compatibility	Size (Organization)	I_{CC} (Max/ Standby)	Max Clock Freq.	# Pins	Pkg Types	Voltage
CAT59C11	C, I	Microchip 5911	1K Bit (x8 or x16)	5mA/100µA	1MHz	8	P, K	5 V
CAT35C202	C I	Microchip 5911 UPGRADE	2K Bit (x8 or x16)	3mA/100µA 4mA/100µA	1MHz	8	P, K	5 V

SECURE ACCESS SERIAL E²PROMs (Data Book Section 6)

Device	Temp. Range	Protocol	Size (Organization)	I_{CC} (Max/ Standby)	Max Clock Freq.	# Pins	Pkg Types	Voltage
CAT33C704	C, I	Synchronous	4K Bit (x8 or x16)	3mA/250µA	1MHz	8 16	P J	3 V
CAT35C704	C, I			3mA/250µA	3MHz			5 V
CAT33C804A-B	C, I	UART Compatible		3mA/250µA	5MHz			3 V
CAT35C804A-B	C, I			3mA/250µA	5MHz			5 V

PARALLEL E²PROMs (Data Book Section 7)

Device	Temp. Range	Size (Organization)	Access Time (ns)	I_{CC} (Max/ Standby)	# Pins	Pkg Types	Voltage
CAT28C16A	C, I	16K Bit (2Kx8)	200	25mA/100µA	24 24	P K, J	5 V
CAT28C16V3	C	16K Bit (2Kx8)	700	10mA/50µA	32	N	3 V
CAT28C17A	C, I	16K Bit (2Kx8)	200	25mA/100µA	28 32	P, K, J N	5 V
CAT28C64A	C, I	64K Bit (8Kx8)	150/200/250	30mA/100µA	28	P, J, K	5V
CAT28C65A	C, I	64K Bit (8Kx8)	150/200/250	30mA/100µA	32	N	5 V
CAT28C64B	C I	64K Bit (8Kx8)	120/150/200 150/200	25mA/100µA	28	P, J, K	5 V
CAT28C65B	C I	64K Bit (8Kx8)	120/150/200 150/200	25mA/100µA	32	N, T	5 V
CAT28C256	C, I	256K Bit (32Kx8)	200/250/300	30mA/150µA	28 32	P N	5 V

Note:
(1) All Serial E²PROMs offered in High Endurance version ("H").
(2) For information on military temperature devices, please contact the factory.

FLASH MEMORIES (Data Book Section 8)

Device	Temp. Range	Size (Organization)	Access Time (ns)	I_{CC} (Max/ Standby)	# Pins	Pkg Types	Voltage
CAT28F512	C, I	512K Bit (64Kx8)	120/150/200	30mA/100µA	32	P, N, T	12 V
CAT28F512V5	C, I	512K Bit (64Kx8)	120/150/200	120mA/100µA	32	P, N, T	5 V
CAT28F010	C, I	1M Bit (128Kx8)	120/150/200	30mA/100µA	32	P, N, T	12 V
CAT28F010V5	C, I	1M Bit (128Kx8)	120/150/200	120mA/100µA	32	P, N, T	5 V
CAT28F020	C, I	2M Bit (256Kx8)	120/150/200	30mA/100µA	32	P, N, T	12 V

EPROMs (Data Book Section 9)

Device	Temp. Range	Size (Organization)	Access Time (ns)	I_{CC} (Max/ Standby)	# Pins	Pkg Types	Programming Voltage
CAT27HC256L	C I	256K Bit (32Kx8)	55/70/90/120 70/90/120	50mA/100µA 60mA/100µA	28 32	D, P (OTP) E, N (OTP)	12.5 V
CAT27C210	C I	1M Bit (64Kx16)	150/170/200/250 170/200/250	50mA/100µA 60mA/100µA	40 44	D, P (OTP) N (OTP)	12.5 V

NVRAMs (Data Book Section 10)

Device	Temp. Range	Compatibility	Size (Organization)	I_{CC} (Max/ Standby	Access Time (ns)	# Pins	Pkg Types
CAT22C10	C, I	Xicor	256 Bit (64x4)	40mA/30µA	200/300	18 20	P J
CAT22C12	C, I	Xicor	1K Bit (256x4)	50mA/30µA	200/300	18	P
CAT24C44	C, I	Xicor	256 Bit (16x16) Serial	20mA/30µA	1MHz	8 8	P J

Note:
(1) For information on military temperature devices, please contact the factory.

ANALOG PRODUCTS (Data Book Section 11)

DACs

Device	Temp. Range	Bits Resolution	Settling Time (ns)	Linearity Error (LSB)	Data Latch	NV Mem.	# DACs /Pkg	Pkg Types
CAT104A	C	12	40	0.5	No	No	1	C
CAT104B	C	12	40	1.0	No	No	1	C
CAT105A	C	12	40	0.5	Yes	No	1	C
CAT105B	C	12	40	1.0	Yes	No	1	C
CAT504	C, I	8	10 (µs)	1.0	Yes	Yes	4	P, J
CAT505	C, I	8	10 (µs)	1.0	Yes	Yes	4	P, J
CAT506A	C	12	25	0.5	Yes	No	1	C
CAT506B	C	12	25	1.0	Yes	No	1	C

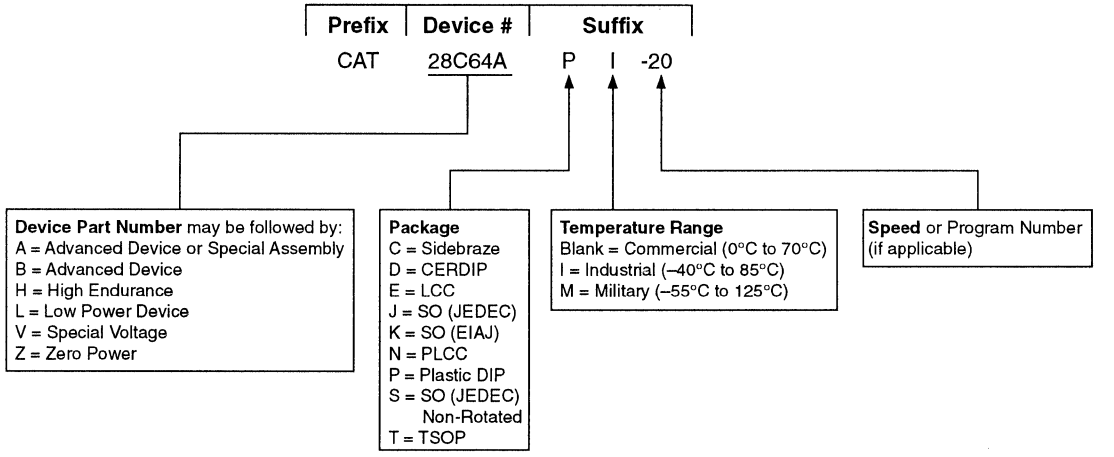
VOLTAGE REFERENCES

Device	Temp. Range	Output Voltage	Output Error (mV)	Adjustment Range (%)	Drift with Temp. (ppm/°C)	Pkg Types
CAT507	C, I	+5	15	6	3	P, D
CAT508	C, I	–5	15	6	3	P, D
CAT2700	C, I	+10	2.5	0.2	3	P, D
CAT2701	C, I	–10	2.5	0.2	3	P, D

Note:
(1) For information on military temperature devices, please contact the factory.

Ordering Tree (Part Number Description)

Explanation of Catalyst's Part Number Code



5010 FHD ORDERING INFORMATION

Note:
(1) Refer to Section 15 for a detailed listing of Catalyst part numbers by product type.
(2) The device used in the above example is a CAT28C64API-20 (Plastic DIP, Industrial temperature, 200ns Access Time).

CATALYST SEMICONDUCTOR

Product Information 1

2-Wire Bus Serial E^2PROMs 2

3-Wire Bus Serial E^2PROMs 3

SPI Bus Serial E^2PROMs 4

4-Wire Bus Serial E^2PROMs 5

Secure Access Serial E^2PROMs 6

Parallel E^2PROMs 7

Flash Memories 8

EPROMs 9

NVRAMs 10

Analog Products 11

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Quality and Reliability 13

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General Information 15

Contents

SECTION 2 2-WIRE BUS SERIAL E^2PROMS

CAT24C02/CAT24C02I	256 x 8	2K-Bit	2-1
CAT24LC02/CAT24LC02I	256 x 8	2K-Bit	2-9
CAT24C02A/CAT24C02AI	256 x 8	2K-Bit	2-17
CAT24LC02A/CAT24LC02AI	256 x 8	2K-Bit	2-25
CAT24C04/CAT24C04I	512 x 8	4K-Bit	2-33
CAT24LC04/CAT24LC04I	512 x 8	4K-Bit	2-41
CAT24C08/CAT24C08I	1024 x 8	8K-Bit	2-49
CAT24LC08/CAT24LC08I	1024 x 8	8K-Bit	2-57
CAT24C16/CAT24C16I	2048 x 8	16K-Bit	2-65
CAT24LC16/CAT24LC16I	2048 x 8	16K-Bit	2-73
CAT24C32/CAT24C32	4096 x 8	32K-Bit	2-81

CAT24C02/CAT24C02I

2K-Bit SERIAL E²PROM

FEATURES

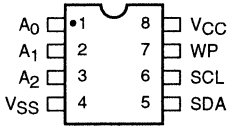
- I²C Bus Compatible*
- Low Power CMOS Technology
- Hardware Write Protect
- 8 Byte Page Write Buffer
- Self-Timed Write Cycle with Auto-Clear
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- 8 pin DIP, 8 pin SO or 14 pin SO Package
- ZERO Power™ Version (CAT24C02Z) Available
- Optional High Endurance Device Available

DESCRIPTION

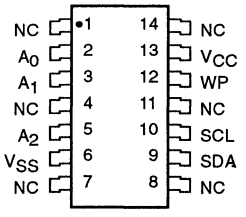
The CAT24C02/CAT24C02I is a 2K bit Serial CMOS E²PROM internally organized as 256 x 8 bits. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24C02/CAT24C02I features an 8-byte page write buffer and a special write protection feature. The device operates via the I²C bus serial interface and is available in 8 pin DIP, 8 pin SO or 14 pin SO packages.

PIN CONFIGURATION

DIP Package

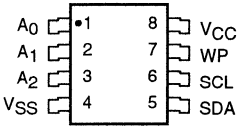


SO Package



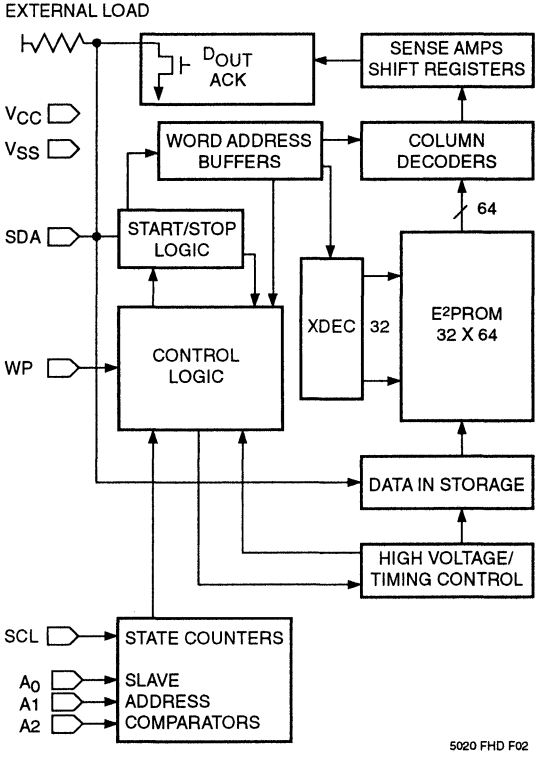
5027 FHD F01

SO Package



5020 FHD F01

BLOCK DIAGRAM



5020 FHD F02

PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
WP	Write Protect
VCC	+5V Power Supply
VSS	Ground

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

TD 5020

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT24C02 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT24C02I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

		Limits				
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{CC}	Power Supply Current			3	mA	f_{SCL} = 100 KHz
I_{SB}	Standby Current V_{CC} = 5.5V			4	µA	V_{IN} = GND or V_{CC}
I_{SBZ}(5)	Standby Current V_{CC} = 5.5V			0	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	–1.0		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A0, A1, A2, SCL)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Standby Current (I_{SBZ}) = 0µA (<900nA) for the CAT24C02Z.

A.C. CHARACTERISTICS

CAT24C02 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT24C02I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max	Units
F_{SCL}	Clock Frequency		100	KHz
T_I(3)	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5	µs
t_{BUF}(3)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		ns
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R(3)	SDA and SCL Rise Time		1	µs
t_F(3)	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Power-Up Timing(3)(6)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Write Cycle Limits

Symbol	Parameter	Min.	Typ.	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(6) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT24C02/CAT24C02I supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24C02/CAT24C02I operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated. A maximum of 8 devices may be connected to the bus as determined by the device address inputs A0, A1, and A2.

PIN DESCRIPTIONS

SCL: Serial Clock
The serial clock input clocks all data transferred into or out of the device.

SDA: Serial Data/Address
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

A0, A1, A2: Device Address Inputs
These inputs set the device address within the slave address. They must be connected to either V_{SS} or V_{CC}.

WP: Write Protect
If the WP pin is tied to V_{CC} the entire memory array becomes READ only. If the WP pin is tied to V_{SS} normal read/write operations are allowed to the device. This feature protects the device from inadvertent programming.

Figure 1. Bus Timing

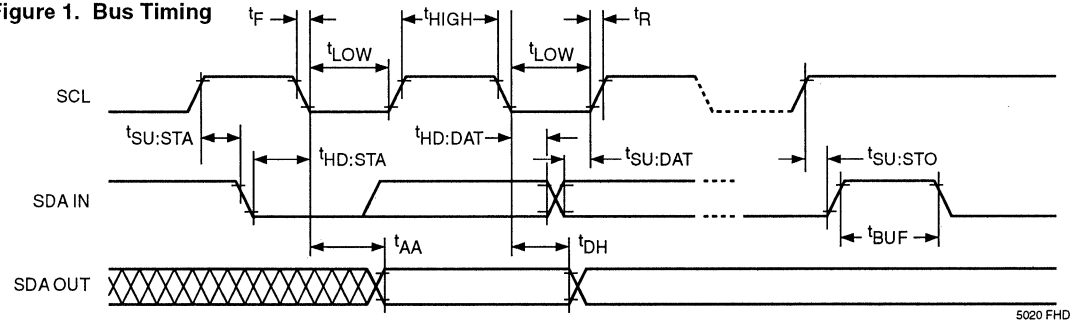


Figure 2. Write Cycle Timing

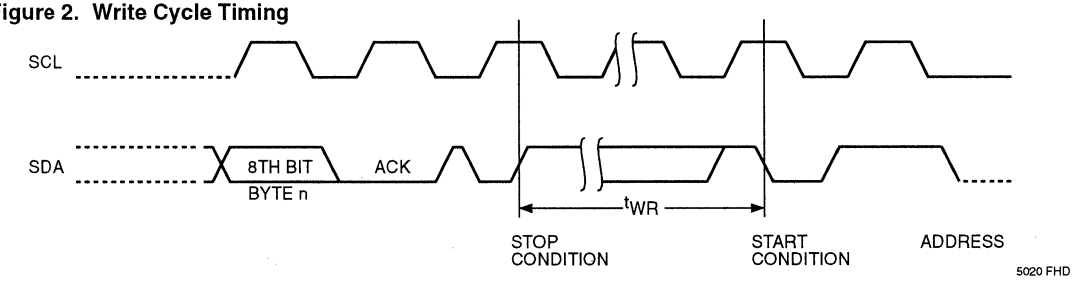
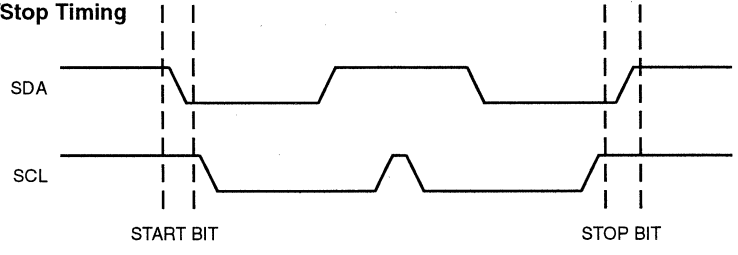


Figure 3. Start/Stop Timing



I²C BUS PROTOCOL

The following defines the features of the I²C bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24C02/CAT24C02I monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1010 for the CAT24C02/CAT24C02I (see Fig. 5). The next three significant bits (A2, A1, A0) are the device address bits and define which device the Master is accessing. Up to eight CAT24C02/CAT24C02I devices may be individually addressed by the system. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition, the CAT24C02/CAT24C02I monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24C02/CAT24C02I then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the eight bits of data.

The CAT24C02/CAT24C02I responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each eight bit byte.

When the CAT24C02/CAT24C02I begins a READ mode it transmits eight bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24C02/CAT24C02I will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Figure 4. Acknowledge Timing

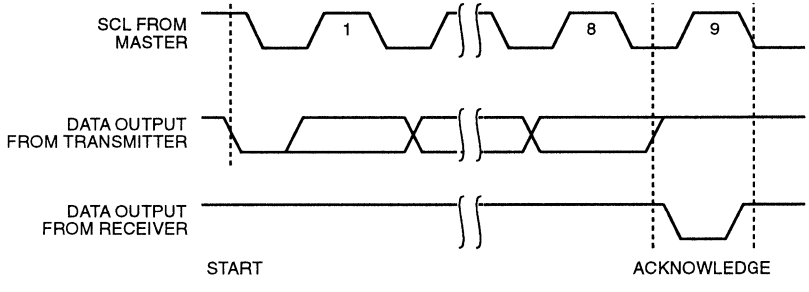


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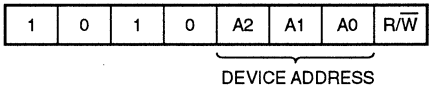
Figure 5. Slave Address Bits



5022 FHD F07

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24C02/CAT24C02I. After receiving another acknowledge from the Slave, the Master device transmits the data byte to be written into the addressed memory location. The CAT24C02/CAT24C02I acknowledges once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24C02/CAT24C02I writes up to 8 bytes of data, in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial word is transmitted, the Master is allowed to send up to 7 additional bytes. After each byte has been transmitted the CAT24C02/CAT24C02I will respond with an acknowledge, and internally increment the three low order address bits by one. The high order bits remain unchanged.

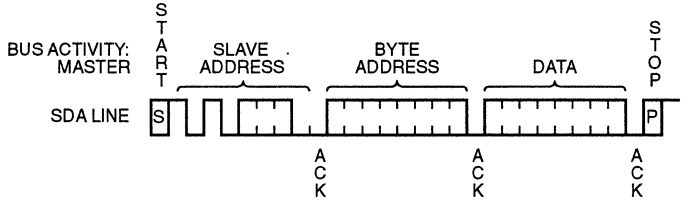
If the Master transmits more than 8 bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all eight bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24C02/CAT24C02I in a single write cycle.

Acknowledge Polling

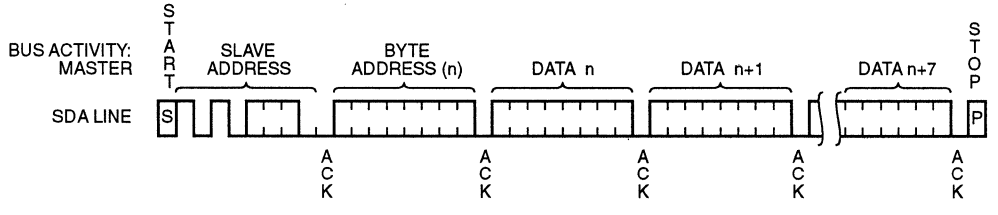
The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24C02/CAT24C02I initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24C02/CAT24C02I is still busy with the write operation, no ACK will be returned. If the CAT24C02/CAT24C02I has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Figure 6. Byte Write Timing



5020 FHD F08

Figure 7. Page Write Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

5020 FHD F09

WRITE PROTECTION

The Write Protection feature allows the user to protect against inadvertent programming of the memory array. If the WP pin is tied to V_{CC}, the entire memory array is protected and becomes read only. The CAT24C02/ CAT24C02I will accept both slave and byte addresses, but the memory location accessed is protected from programming by the device's failure to send an acknowledge after the first byte of data is received.

READ OPERATIONS

The READ operation for the CAT24C02/CAT24C02I is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

Immediate Address Read

The CAT24C02/CAT24C02I's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=255, then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24C02/CAT24C02I receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Selective Read

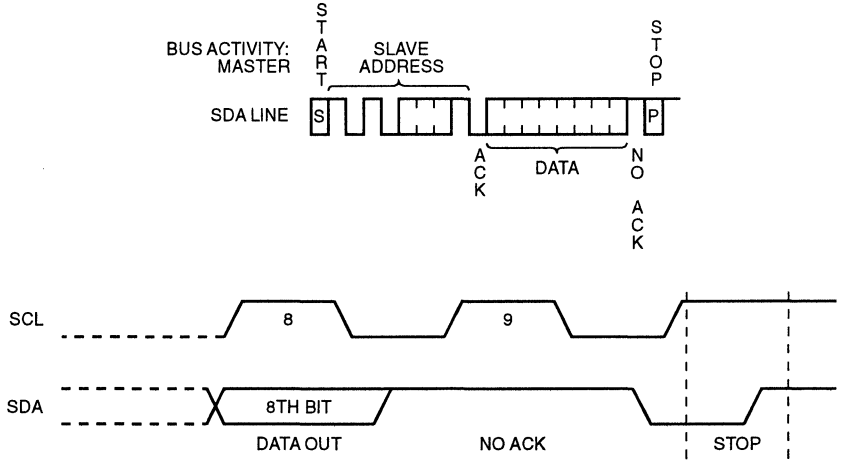
Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24C02/CAT24C02I acknowledges the word address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24C02/CAT24C02I then responds with its acknowledge and sends the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24C02/CAT24C02I sends the initial eight bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24C02/CAT24C02I will continue to output an eight bit byte for each acknowledge sent by the Master. The operation will terminate operation when the Master fails to respond with an acknowledge, thus sending the STOP condition.

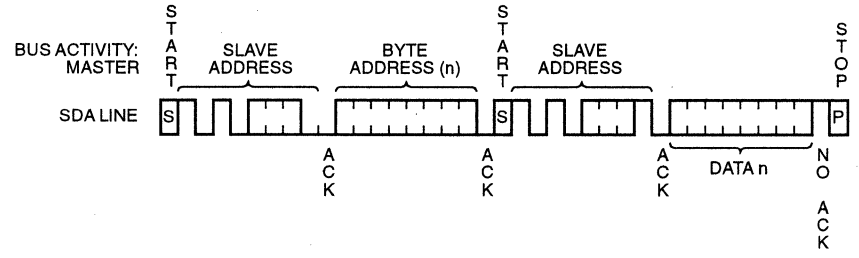
The data being transmitted from the CAT24C02/ CAT24C02I is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24C02/CAT24C02I address bits so that the entire memory array can be read during one operation. If more than the 256 bytes are read out, the counter will "wrap around" and continue to clock out data bytes.

Figure 8. Immediate Address Read Timing



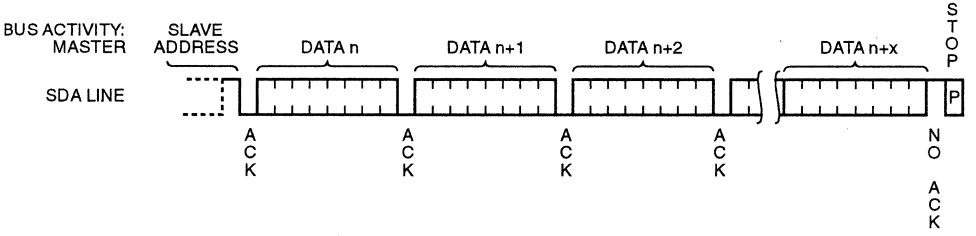
5020 FHD F10

Figure 9. Selective Read Timing



5020 FHD F11

Figure 10. Sequential Read Timing



5020 FHD F12

CAT24LC02/CAT24LC02I

2K-Bit SERIAL E²PROM

FEATURES

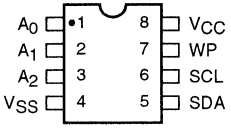
- I²C Bus Compatible*
- Low Power CMOS Technology
- Hardware Write Protect
- 8 Byte Page Write Buffer
- Self-Timed Write Cycle with Auto-Clear
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- 8 pin DIP, 8 pin SO or 14 pin SO Package
- 3 to 6 Volt Operation
- ZERO Power™ Version (CAT24LC02Z) Available
- Optional High Endurance Device Available

DESCRIPTION

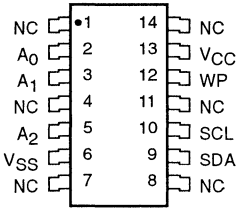
The CAT24LC02/CAT24LC02I is a 2K bit Serial CMOS E²PROM internally organized as 256 x 8 bits. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24LC02/CAT24LC02I features an 8-byte page write buffer and a special write protection feature. The device operates via the I²C bus serial interface and is available in 8 pin DIP, 8 pin SO or 14 pin SO packages.

PIN CONFIGURATION

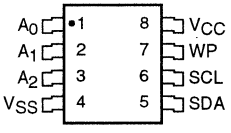
DIP Package



SO Package



SO Package



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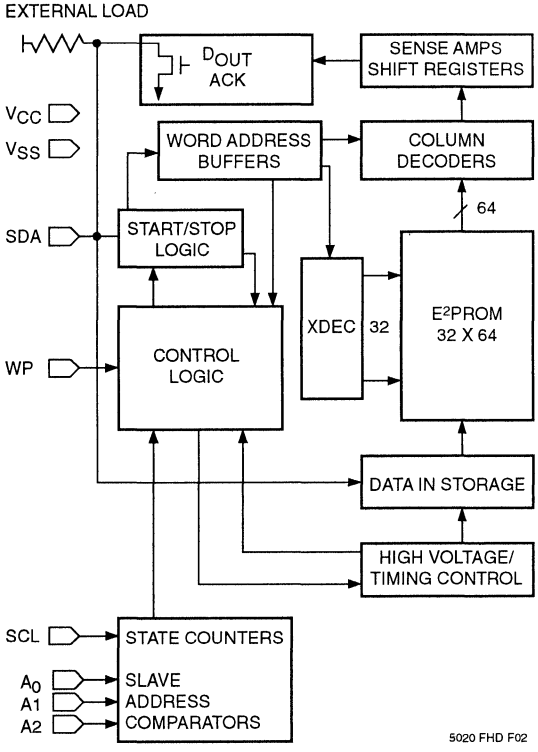
BLOCK DIAGRAM



5020 FHD F02

PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
WP	Write Protect
V_{CC}	+3V to +6V Power Supply
V_{SS}	Ground

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

TD 5021

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT24LC02 T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
CAT24LC02I T_A = –40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current			3	mA	f_{SCL} = 100 KHz
I_{SB}	Standby Current V_{CC} = 6V			4	µA	V_{IN} = GND or V_{CC}
I_{SBZ}(5)	Standby Current V_{CC} = 6V			0	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	–1.0		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A0, A1, A2, SCL)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Standby Current (I_{SBZ}) = 0µA (<900nA) for the CAT24LC02Z.

A.C. CHARACTERISTICS

CAT24LC02 T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
CAT24LC02I T_A = –40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max	Units
F_{SCL}	Clock Frequency		100	KHz
T_I(3)	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5	µs
t_{BUF}(3)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		ns
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R(3)	SDA and SCL Rise Time		1	µs
t_F(3)	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Power-Up Timing(3)(6)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Write Cycle Limits

Symbol	Parameter	Min.	Typ.	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(6) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT24LC02/CAT24LC02I supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24LC02/CAT24LC02I operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated. A maximum of 8 devices may be connected to the bus as determined by the device address inputs A0, A1, and A2.

PIN DESCRIPTIONS

SCL: Serial Clock
The serial clock input clocks all data transferred into or out of the device.

SDA: Serial Data/Address
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

A0, A1, A2: Device Address Inputs
These inputs set the device address within the slave address. They must be connected to either V_{SS} or V_{CC}.

WP: Write Protect
If the WP pin is tied to V_{CC} the entire memory array becomes READ only. If the WP pin is tied to V_{SS} normal read/write operations are allowed to the device. This feature protects the device from inadvertent programming.

Figure 1. Bus Timing

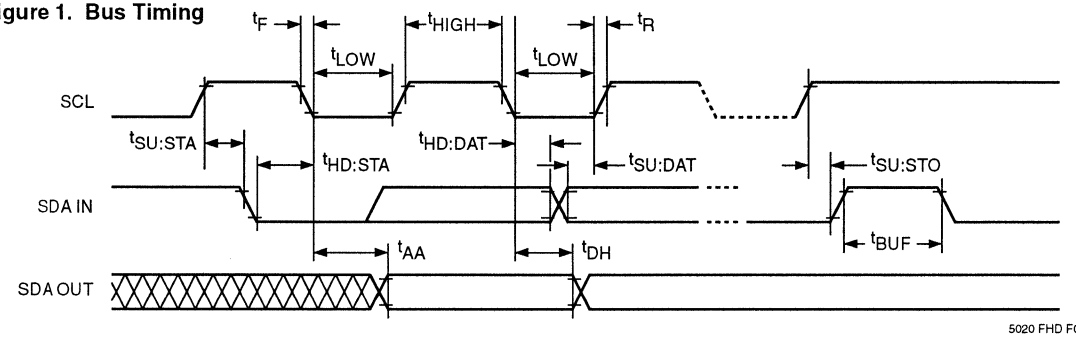


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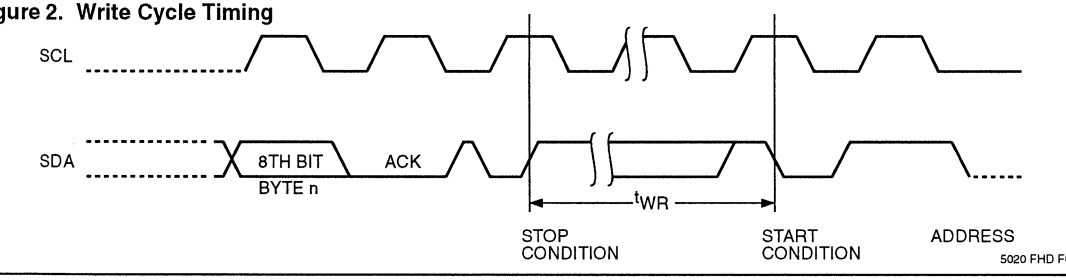
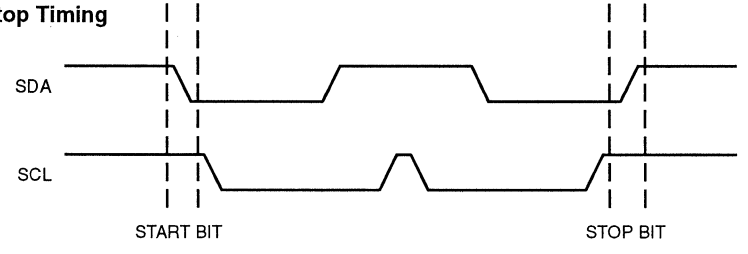
Figure 2. Write Cycle Timing



5020 FHD F04

Figure 3. Start/Stop Timing



5020 FHD F05

I²C BUS PROTOCOL

The following defines the features of the I²C bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24LC02/CAT24LC02I monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1010 for the CAT24LC02/CAT24LC02I (see Fig. 5). The next three significant bits (A2, A1, A0) are the device address bits and define which device the Master is accessing. Up to eight CAT24LC02/CAT24LC02I devices may be individually addressed by the system. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition, the CAT24LC02/CAT24LC02I monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24LC02/CAT24LC02I then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

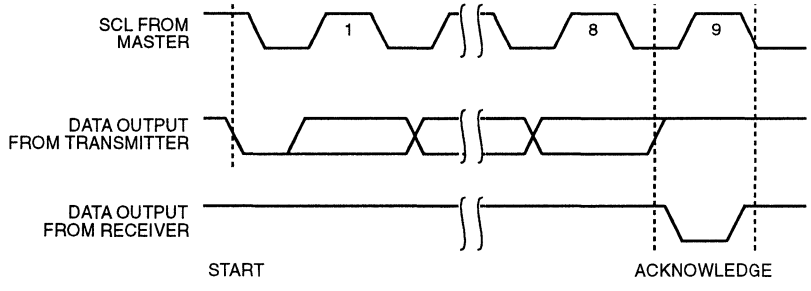
Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the eight bits of data.

The CAT24LC02/CAT24LC02I responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each eight bit byte.

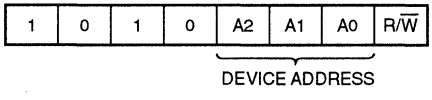
When the CAT24LC02/CAT24LC02I begins a READ mode it transmits eight bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24LC02/CAT24LC02I will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Figure 4. Acknowledge Timing



5020 FHD F06

Figure 5. Slave Address Bits



5022 FHD F07

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24LC02/CAT24LC02I. After receiving another acknowledge from the Slave, the Master device transmits the data byte to be written into the addressed memory location. The CAT24LC02/CAT24LC02I acknowledges once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24LC02/CAT24LC02I writes up to 8 bytes of data, in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial word is transmitted, the Master is allowed to send up to 7 additional bytes. After each byte has been transmitted the CAT24LC02/CAT24LC02I will respond with an acknowledge, and internally increment the three low order address bits by one. The high order bits remain unchanged.

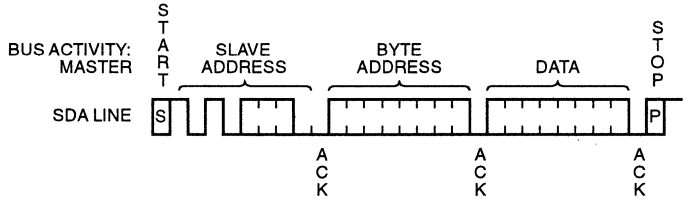
If the Master transmits more than 8 bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all eight bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24LC02/CAT24LC02I in a single write cycle.

Acknowledge Polling

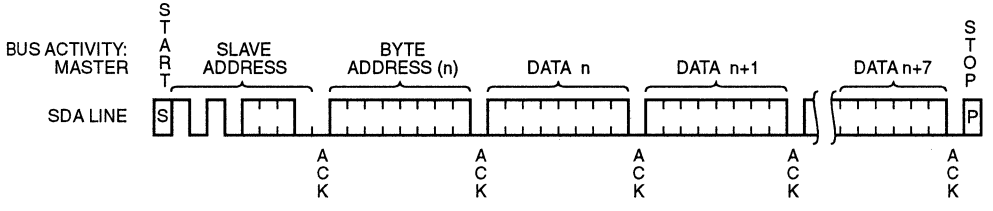
The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24LC02/CAT24LC02I initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24LC02/CAT24LC02I is still busy with the write operation, no ACK will be returned. If the CAT24LC02/CAT24LC02I has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Figure 6. Byte Write Timing



5020 FHD F08

Figure 7. Page Write Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

5020 FHD F09

WRITE PROTECTION

The Write Protection feature allows the user to protect against inadvertent programming of the memory array. If the WP pin is tied to V_{CC}, the entire memory array is protected and becomes read only. The CAT24LC02/CAT24LC02I will accept both slave and byte addresses, but the memory location accessed is protected from programming by the device's failure to send an acknowledge after the first byte of data is received.

READ OPERATIONS

The READ operation for the CAT24LC02/CAT24LC02I is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

Immediate Address Read

The CAT24LC02/CAT24LC02I's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=255, then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24LC02/CAT24LC02I receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Selective Read

Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24LC02/CAT24LC02I acknowledges the word address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24LC02/CAT24LC02I then responds with its acknowledge and sends the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24LC02/CAT24LC02I sends the initial eight bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24LC02/CAT24LC02I will continue to output an eight bit byte for each acknowledge sent by the Master. The operation will terminate operation when the Master fails to respond with an acknowledge, thus sending the STOP condition.

The data being transmitted from the CAT24LC02/CAT24LC02I is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24LC02/CAT24LC02I address bits so that the entire memory array can be read during one operation. If more than the 256 bytes are read out, the counter will "wrap around" and continue to clock out data bytes.

Figure 8. Immediate Address Read Timing

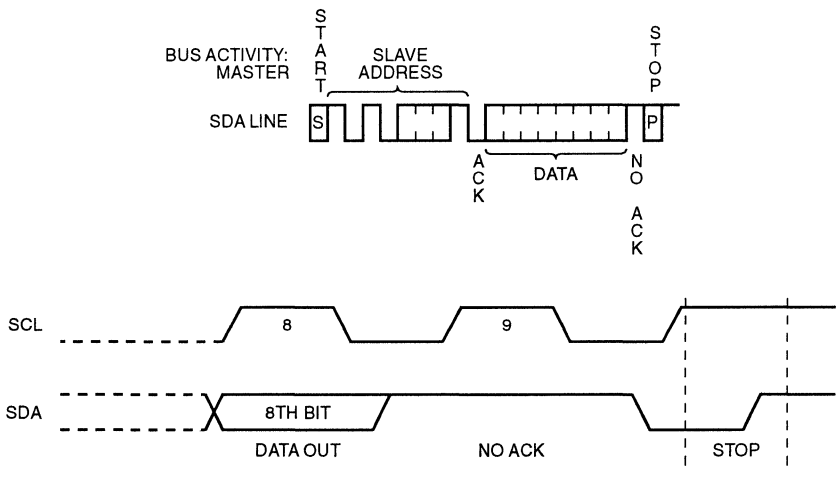
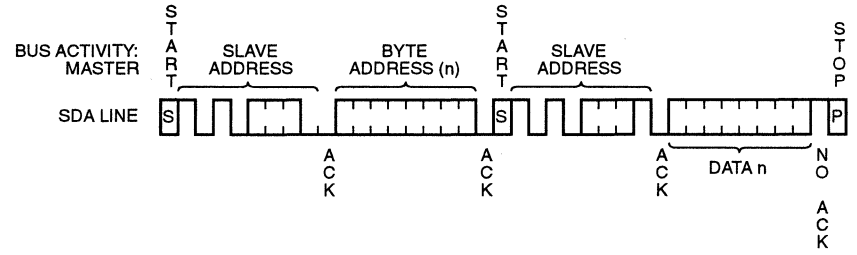
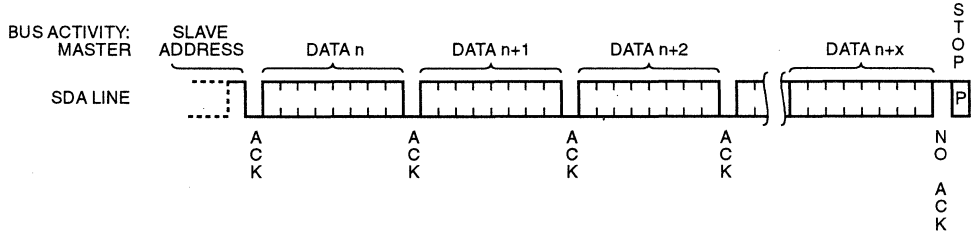


Figure 9. Selective Read Timing



5020 FHD F11

Figure 10. Sequential Read Timing



5020 FHD F12

CATALYST SEMICONDUCTOR

CAT24C02A/CAT24C02AI

2K-Bit SERIAL E²PROM

FEATURES

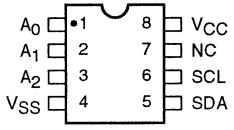
- I²C Bus Compatible*
- Low Power CMOS Technology
- 8 Byte Page Write Buffer
- Self-Timed Write Cycle with Auto-Clear
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- 8 pin DIP, 8 pin SO or 14 pin SO Package
- ZERO Power™ Version (CAT24C02AZ) Available
- Optional High Endurance Device Available

DESCRIPTION

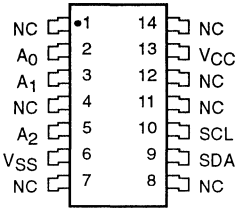
The CAT24C02A/CAT24C02AI is a 2K bit Serial CMOS E²PROM internally organized as 256 x 8 bits. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24C02A/CAT24C02AI features an 8-byte page write buffer. The device operates via the I²C bus serial interface and is available in 8 pin DIP, 8 pin SO or 14 pin SO packages.

PIN CONFIGURATION

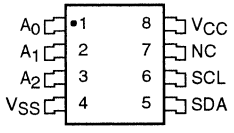
DIP Package



SO Package



SO Package



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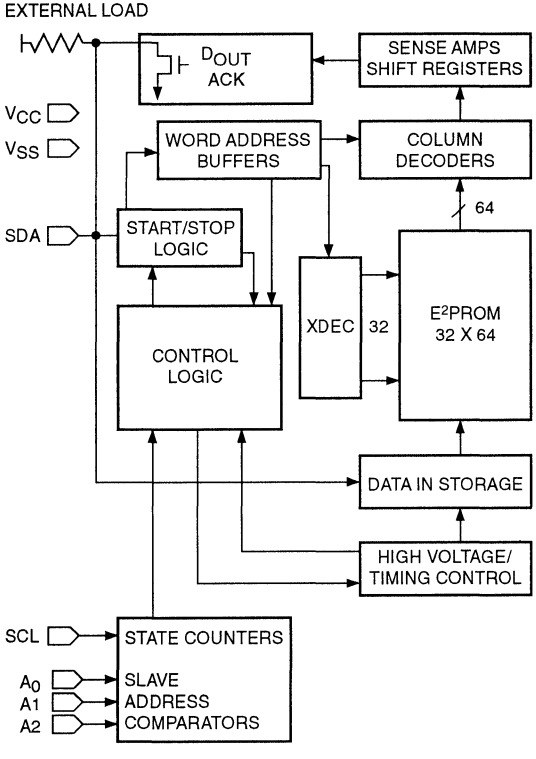
BLOCK DIAGRAM



5020 FHD F02

PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
NC	No Connect
VCC	+5V Power Supply
VSS	Ground

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

TD 5029

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT24C02A T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT24C02AI T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current			3	mA	f_{SCL} = 100 KHz
I_{SB}	Standby Current V_{CC} = 5.5V			4	µA	V_{IN} = GND or V_{CC}
I_{SBZ}(5)	Standby Current V_{CC} = 5.5V			0	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	–1.0		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A0, A1, A2, SCL)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may understoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Standby Current (I_{SBZ}) = 0µA (<900nA) for the CAT24C02AZ.

A.C. CHARACTERISTICS

CAT24C02A T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT24C02AI T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max	Units
F_{SCL}	Clock Frequency		100	KHz
T_I(3)	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5	µs
t_{BUF}(3)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		ns
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R(3)	SDA and SCL Rise Time		1	µs
t_F(3)	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Power-Up Timing(3)(6)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Write Cycle Limits

Symbol	Parameter	Min.	Typ.	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(6) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT24C02A/CAT24C02AI supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24C02A/CAT24C02AI operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated. A maximum of 8 devices may be connected to the bus as determined by the device address inputs A0, A1, and A2.

PIN DESCRIPTIONS

SCL: Serial Clock
The serial clock input clocks all data transferred into or out of the device.

SDA: Serial Data/Address
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

A0, A1, A2: Device Address Inputs
These inputs set the device address within the slave address. They must be connected to either V_{SS} or V_{CC}.

Figure 1. Bus Timing

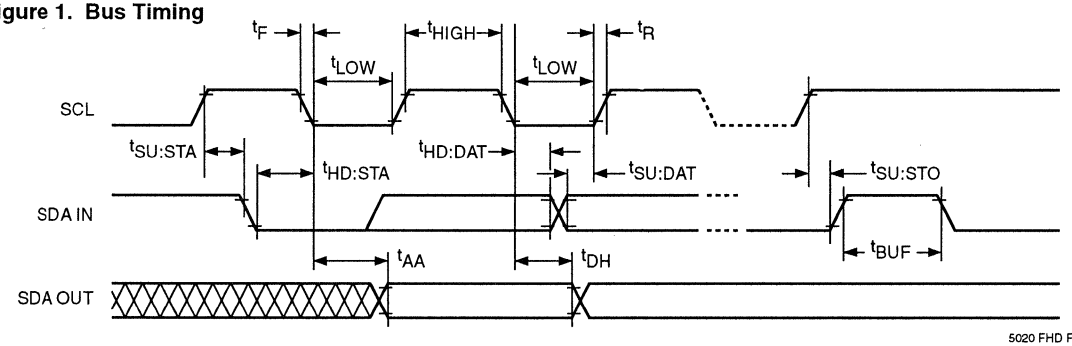


Figure 2. Write Cycle Timing

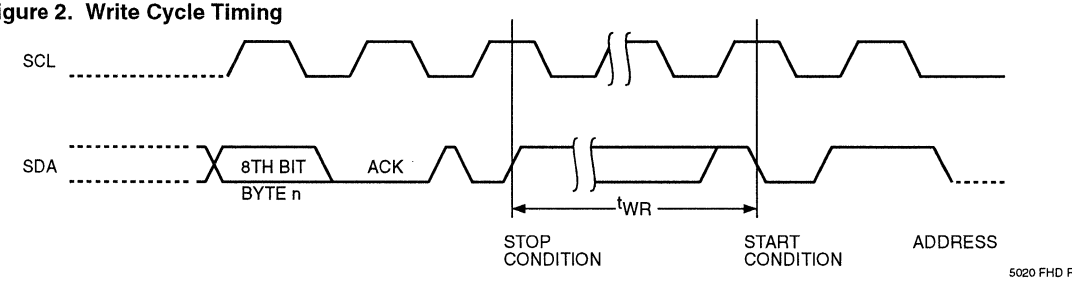
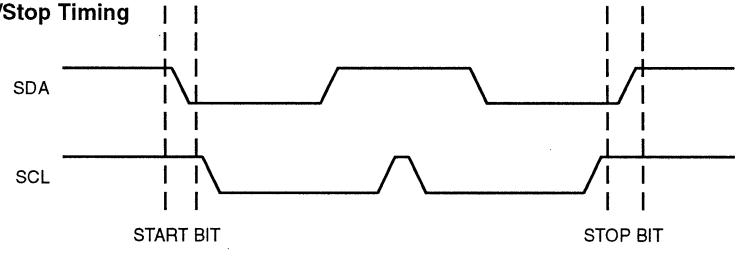


Figure 3. Start/Stop Timing



I²C BUS PROTOCOL

The following defines the features of the I²C bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24C02A/CAT24C02AI monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1010 for the CAT24C02A/CAT24C02AI (see Fig. 5). The next three significant bits (A2, A1, A0) are the device address bits and define which device the Master is accessing. Up to eight CAT24C02A/CAT24C02AI devices may be individually addressed by the system. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition, the CAT24C02A/CAT24C02AI monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24C02A/CAT24C02AI then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the eight bits of data.

The CAT24C02A/CAT24C02AI responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each eight bit byte.

When the CAT24C02A/CAT24C02AI begins a READ mode it transmits eight bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24C02A/CAT24C02AI will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Figure 4. Acknowledge Timing

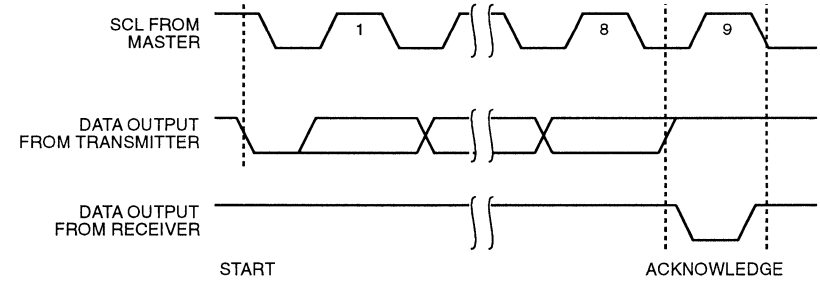


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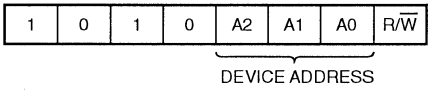
Figure 5. Slave Address Bits



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WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24C02A/CAT24C02AI. After receiving another acknowledge from the Slave, the Master device transmits the data byte to be written into the addressed memory location. The CAT24C02A/CAT24C02AI acknowledges once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24C02A/CAT24C02AI writes up to 8 bytes of data, in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial word is transmitted, the Master is allowed to send up to 7 additional bytes. After each byte has been transmitted the CAT24C02A/CAT24C02AI will respond with an acknowledge, and internally increment the three low order address bits by one. The high order bits remain unchanged.

If the Master transmits more than 8 bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all eight bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24C02A/CAT24C02AI in a single write cycle.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24C02A/CAT24C02AI initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24C02A/CAT24C02AI is still busy with the write operation, no ACK will be returned. If the CAT24C02A/CAT24C02AI has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Figure 6. Byte Write Timing

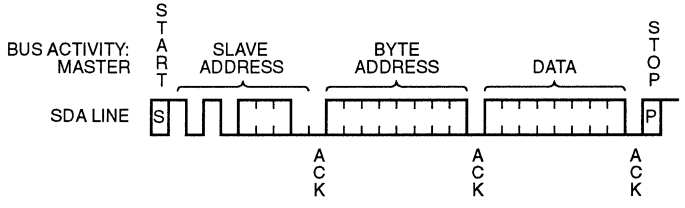

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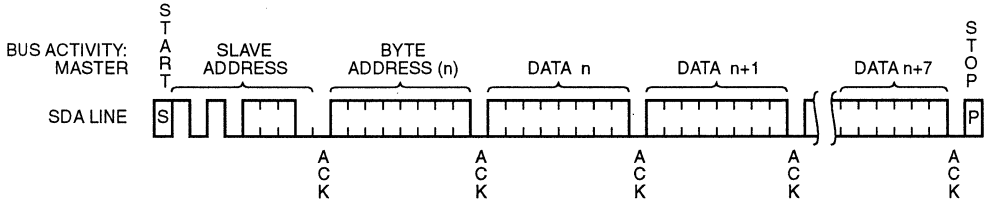
Figure 7. Page Write Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

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READ OPERATIONS

The READ operation for the CAT24C02A/CAT24C02AI is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

Immediate Address Read

The CAT24C02A/CAT24C02AI's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=255, then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24C02A/CAT24C02AI receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Selective Read

Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24C02A/CAT24C02AI acknowledges the word address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24C02A/CAT24C02AI then responds with its acknowledge and sends the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24C02A/CAT24C02AI sends the initial eight bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24C02A/CAT24C02AI will continue to output an eight bit byte for each acknowledge sent by the Master. The operation will terminate operation when the Master fails to respond with an acknowledge, thus sending the STOP condition.

The data being transmitted from the CAT24C02A/CAT24C02AI is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24C02A/CAT24C02AI address bits so that the entire memory array can be read during one operation. If more than the 256 bytes are read out, the counter will "wrap around" and continue to clock out data bytes.

Figure 8. Immediate Address Read Timing

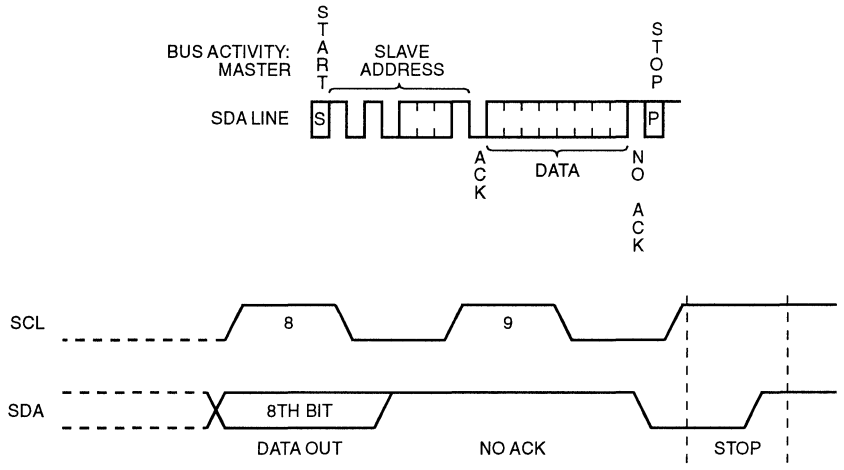

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Figure 9. Selective Read Timing

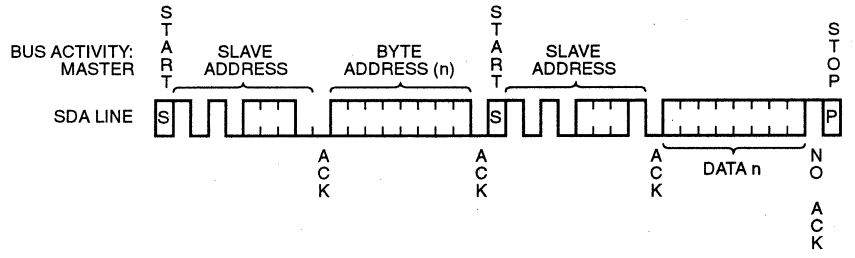

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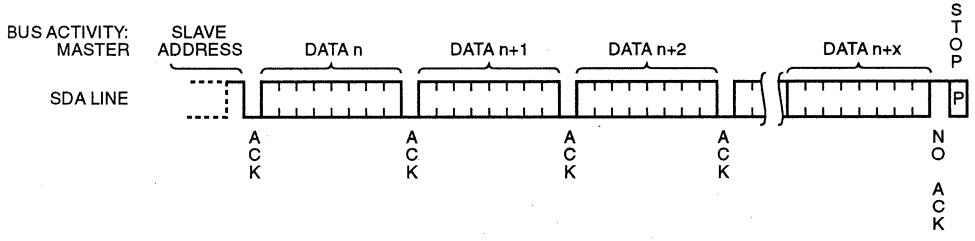
Figure 10. Sequential Read Timing



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CATALYST SEMICONDUCTOR

CAT24LC02A/CAT24LC02AI

2K-Bit SERIAL E²PROM

FEATURES

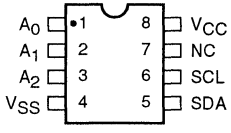
- I²C Bus Compatible*
- Low Power CMOS Technology
- 8 Byte Page Write Buffer
- Self-Timed Write Cycle with Auto-Clear
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- 8 pin DIP, 8 pin SO or 14 pin SO Package
- 3 to 6 Volt Operation
- ZERO Power™ Version (CAT24LC02AZ) Available
- Optional High Endurance Device Available

DESCRIPTION

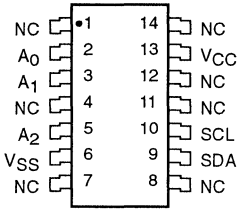
The CAT24LC02A/CAT24LC02AI is a 2K bit Serial CMOS E²PROM internally organized as 256 x 8 bits. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24LC02A/CAT24LC02AI features an 8-byte page write buffer. The device operates via the I²C bus serial interface and is available in 8 pin DIP, 8 pin SO or 14 pin SO packages.

PIN CONFIGURATION

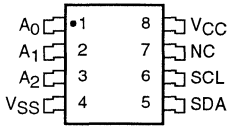
DIP Package



SO Package



SO Package



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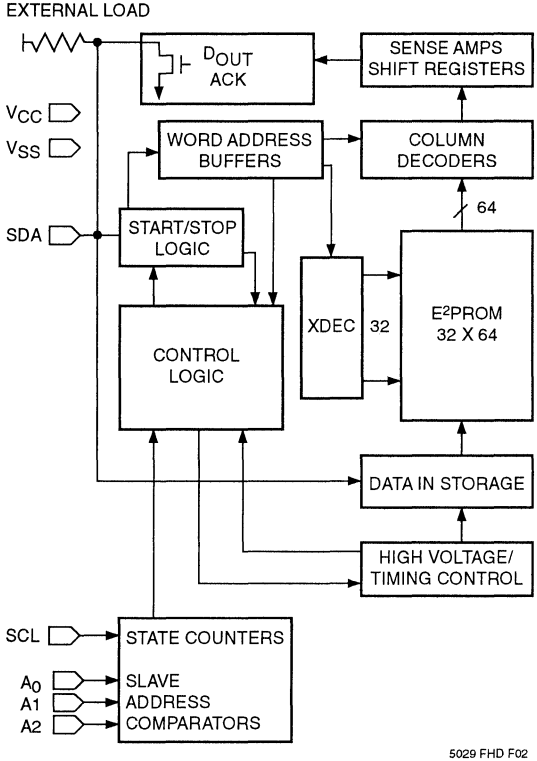
BLOCK DIAGRAM



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PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
NC	No Connect
V_{CC}	+3V to +6V Power Supply
V_{SS}	Ground

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

TD 5030

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to + 7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT24LC02A T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
CAT24LC02AI T_A = –40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current			3	mA	f_{SCL} = 100 KHz
I_{SB}	Standby Current V_{CC} = 6V			4	µA	V_{IN} = GND or V_{CC}
I_{SBZ}(5)	Standby Current V_{CC} = 6V			0	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	–1.0		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A0, A1, A2, SCL)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Standby Current (I_{SBZ}) = 0µA (<900nA) for the CAT24LC02AZ.

A.C. CHARACTERISTICS

CAT24LC02A T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
CAT24LC02AI T_A = –40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max	Units
F_{SCL}	Clock Frequency		100	KHz
T_I(3)	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5	µs
t_{BUF}(3)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		ns
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R(3)	SDA and SCL Rise Time		1	µs
t_F(3)	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Power-Up Timing(3)(6)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Write Cycle Limits

Symbol	Parameter	Min.	Typ.	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(6) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT24LC02A/CAT24LC02AI supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24LC02A/CAT24LC02AI operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated. A maximum of 8 devices may be connected to the bus as determined by the device address inputs A0, A1, and A2.

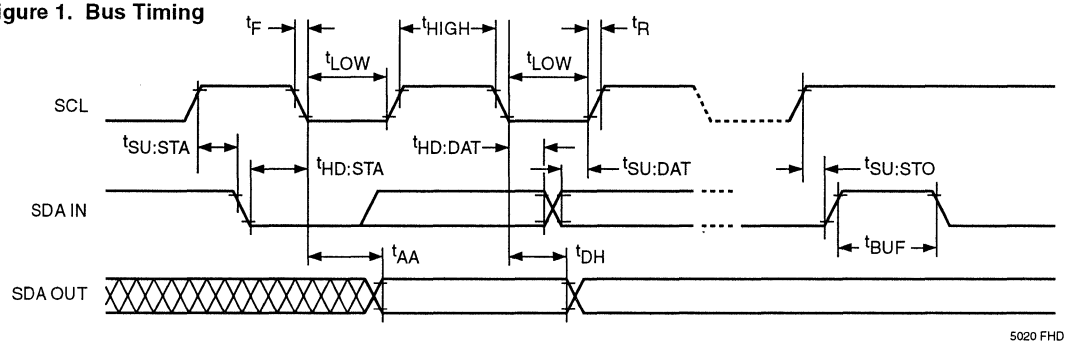
PIN DESCRIPTIONS

SCL: Serial Clock
The serial clock input clocks all data transferred into or out of the device.

SDA: Serial Data/Address
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

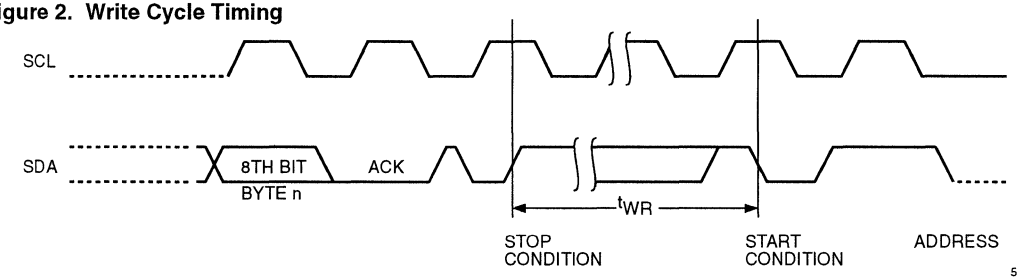
A0, A1, A2: Device Address Inputs
These inputs set the device address within the slave address. They must be connected to either V_{SS} or V_{CC}.

Figure 1. Bus Timing



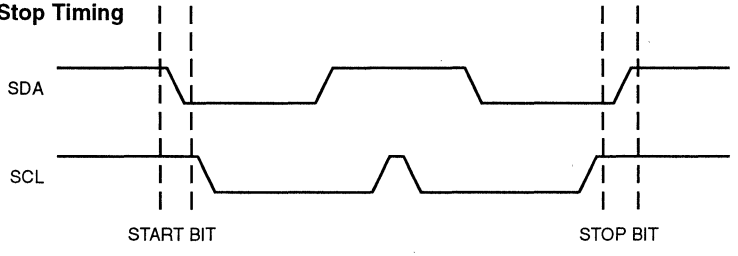
5020 FHD F03

Figure 2. Write Cycle Timing



5020 FHD F04

Figure 3. Start/Stop Timing



5020 FHD F05

I²C BUS PROTOCOL

The following defines the features of the I²C bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24LC02A/CAT24LC02AI monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1010 for the CAT24LC02A/CAT24LC02AI (see Fig. 5). The next three significant bits (A2, A1, A0) are the device address bits and define which device the Master is accessing. Up to eight CAT24LC02A/CAT24LC02AI devices may be individually addressed by the system. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition, the CAT24LC02A/CAT24LC02AI monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24LC02A/CAT24LC02AI then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

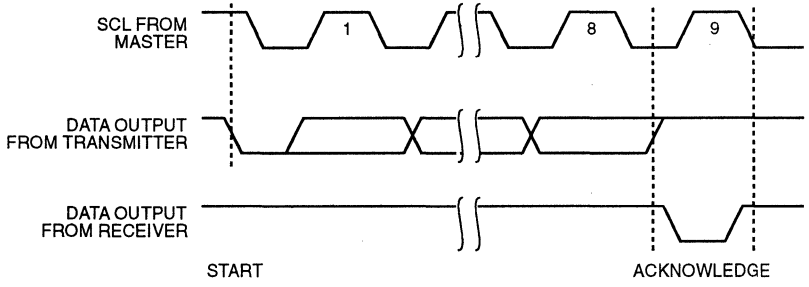
Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the eight bits of data.

The CAT24LC02A/CAT24LC02AI responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each eight bit byte.

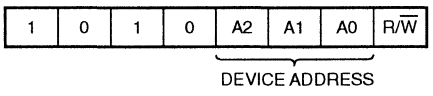
When the CAT24LC02A/CAT24LC02AI begins a READ mode it transmits eight bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24LC02A/CAT24LC02AI will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Figure 4. Acknowledge Timing



5020 FHD F06

Figure 5. Slave Address Bits



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WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24LC02A/CAT24LC02AI. After receiving another acknowledge from the Slave, the Master device transmits the data byte to be written into the addressed memory location. The CAT24LC02A/CAT24LC02AI acknowledges once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24LC02A/CAT24LC02AI writes up to 8 bytes of data, in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial word is transmitted, the Master is allowed to send up to 7 additional bytes. After each byte has been transmitted the CAT24LC02A/CAT24LC02AI will respond with an acknowledge, and internally increment the three low order address bits by one. The high order bits remain unchanged.

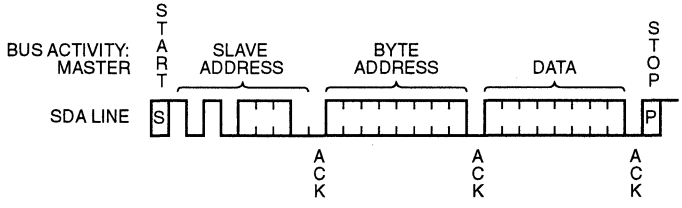
If the Master transmits more than 8 bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all eight bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24LC02A/CAT24LC02AI in a single write cycle.

Acknowledge Polling

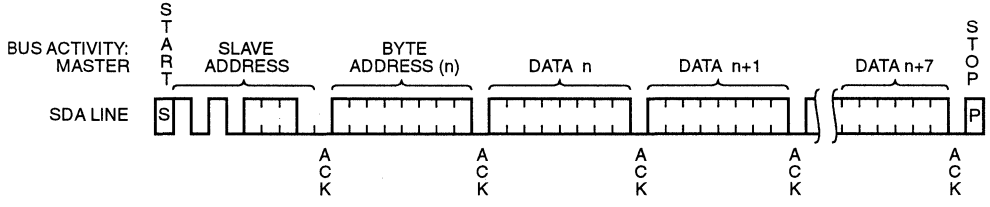
The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24LC02A/CAT24LC02AI initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24LC02A/CAT24LC02AI is still busy with the write operation, no ACK will be returned. If the CAT24LC02A/CAT24LC02AI has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Figure 6. Byte Write Timing



5020 FHD F08

Figure 7. Page Write Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

5020 FHD F09

READ OPERATIONS

The READ operation for the CAT24LC02A/CAT24LC02AI is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

Immediate Address Read

The CAT24LC02A/CAT24LC02AI's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=255, then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24LC02A/CAT24LC02AI receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Selective Read

Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24LC02A/CAT24LC02AI acknowledges the word address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24LC02A/CAT24LC02AI then responds with its acknowledge and sends the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

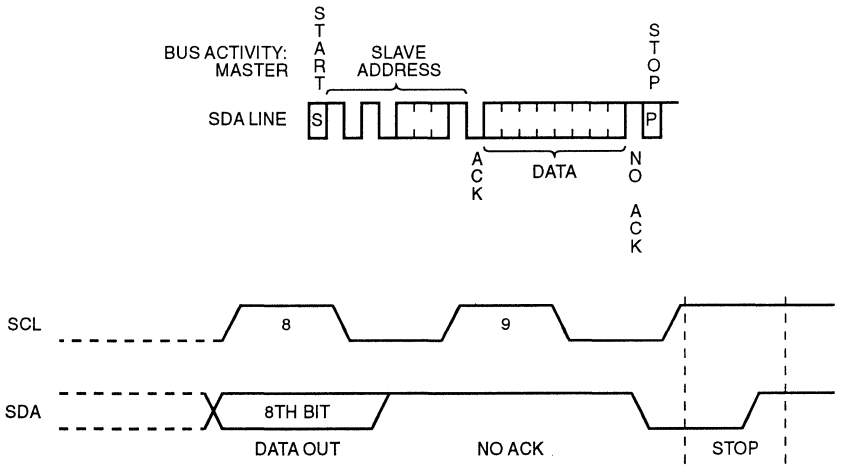
Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24LC02A/CAT24LC02AI sends the initial eight bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24LC02A/CAT24LC02AI will continue to output an eight bit byte for each acknowledge sent by the Master. The operation will terminate operation when the Master fails to respond with an acknowledge, thus sending the STOP condition.

The data being transmitted from the CAT24LC02A/CAT24LC02AI is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24LC02A/CAT24LC02AI address bits so that the entire memory array can be read during one operation. If more than the 256 bytes are read out, the counter will "wrap around" and continue to clock out data bytes.

2

Figure 8. Immediate Address Read Timing



5020 FHD F10

Figure 9. Selective Read Timing

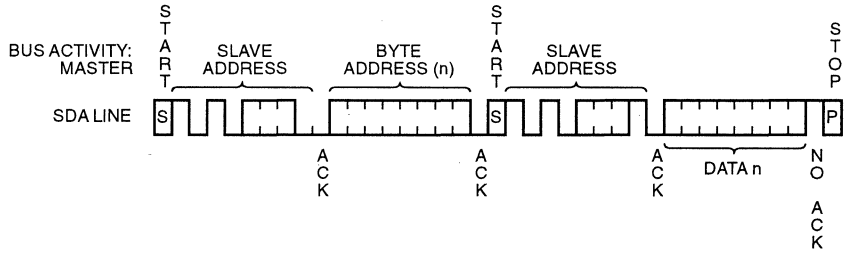


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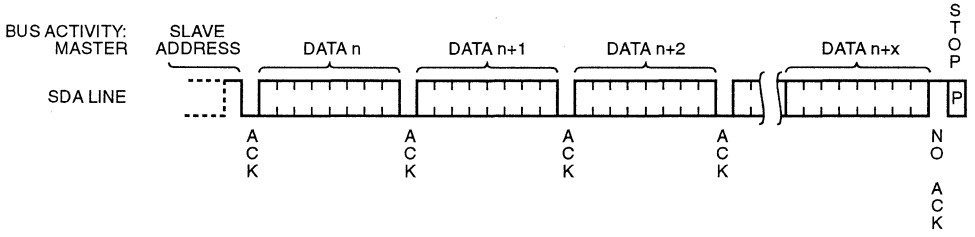
Figure 10. Sequential Read Timing



5020 FHD F12

CAT24C04/CAT24C04I

4K-Bit SERIAL E²PROM

FEATURES

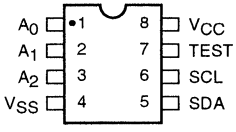
- I²C Bus Compatible*
- Low Power CMOS Technology
- 16 Byte Page Write Buffer
- Self-Timed Write Cycle with Auto-Clear
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- 8 pin DIP, 8 pin SO or 14 pin SO Package
- ZERO Power™ Version (CAT24C04Z) Available
- Optional High Endurance Device Available

DESCRIPTION

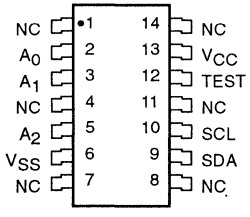
The CAT24C04/CAT24C04I is a 4K bit Serial CMOS E²PROM internally organized as 512 x 8 bits. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24C04/CAT24C04I features a 16 byte page write buffer. The device operates via the I²C bus serial interface and is available in 8 pin DIP, 8 pin SO and 14 pin SO packages.

PIN CONFIGURATION

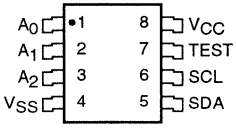
DIP Package



SO Package

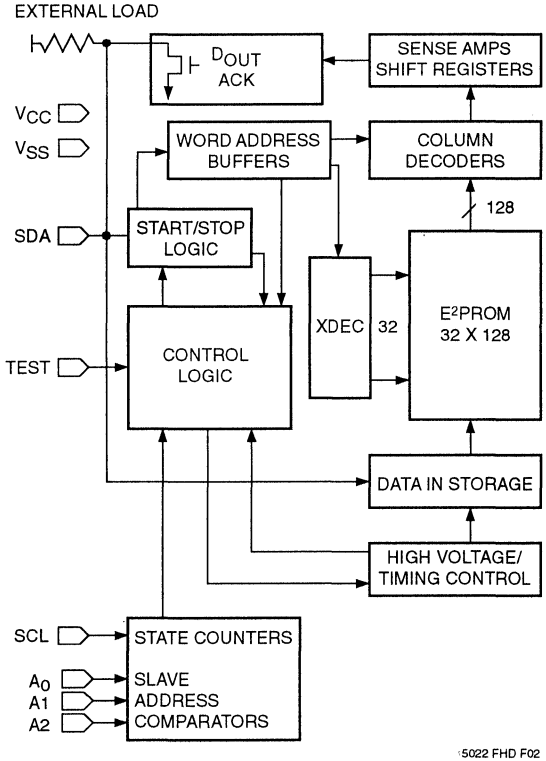


SO Package



5022 FHD F01

BLOCK DIAGRAM



5022 FHD F02

PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
TEST	Connect to V_{SS}
V_{CC}	+5V Power Supply
V_{SS}	Ground

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

TD 5022

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with
Respect to Ground(1) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation
Capability (T_a = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT24C04 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT24C04I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

		Limits				
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{CC}	Power Supply Current			3	mA	f_{SCL} = 100 KHz
I_{SB}	Standby Current V_{CC} = 5.5V			4	µA	V_{IN} = GND or V_{CC}
I_{SBZ}(5)	Standby Current V_{CC} = 5.5V			0	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	–1.0		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A0, A1, A2, SCL)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Standby Current (I_{SBZ}) = 0µA (<900nA) for the CAT24C04Z.

A.C. CHARACTERISTICS

CAT24C04 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT24C04I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max	Units
F_{SCL}	Clock Frequency		100	KHz
T_i(3)	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5	µs
t_{BUF}(3)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		ns
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R(3)	SDA and SCL Rise Time		1	µs
t_F(3)	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Power-Up Timing(3)(6)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Write Cycle Limits

Symbol	Parameter	Min.	Typ.	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(6) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT24C04/CAT24C04I supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24C04/CAT24C04I operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated. A maximum number of four devices may be connected to the bus as determined by the device address inputs A2, A1.

PIN DESCRIPTIONS

SCL: Serial Clock
The serial clock input clocks all data transferred into or out of the device.

SDA: Serial Data/Address
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

A0:
A0 is unused by the CAT24C04/CAT24C04I but must be connected to V_{SS} to insure proper operation of the device.

A1, A2:
The inputs set the device address within the slave address bits. They must be connected to either V_{SS} or V_{CC}.

TEST:
The test pin is for Catalyst internal use only. The customer should connect this pin to V_{SS} during normal operations.

Figure 1. Bus Timing

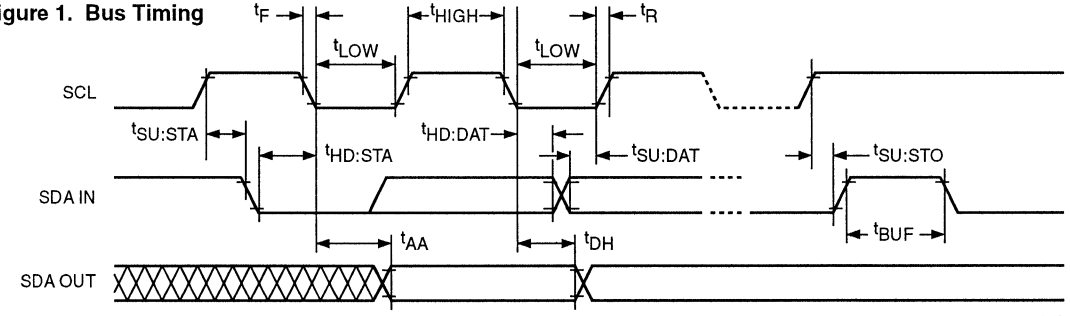


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Figure 2. Write Cycle Timing

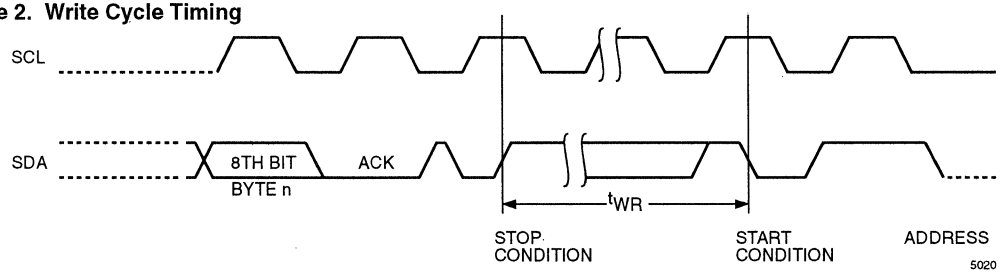

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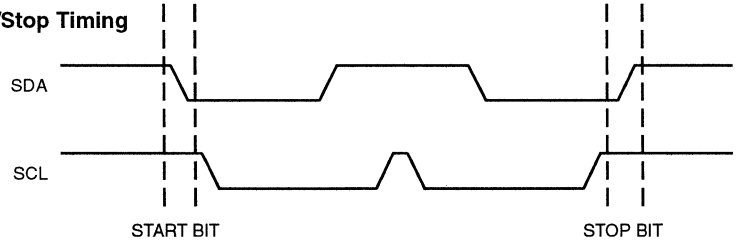
Figure 3. Start/Stop Timing



5020 FHD F05

I²C BUS PROTOCOL

The following defines the features of the I²C bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24C04/CAT24C04I monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1010 for the CAT24C04/CAT24C04I (see Fig. 5). The next two significant bits (A2, A1) are the device address bits and define which device the Master is accessing. Up to four CAT24C04/CAT24C04I devices may be individually addressed by the system. The A0 bit of the slave address selects which 2K array of memory is being addressed. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0 a Write operation is selected.

After the Master sends a START condition, the CAT24C04/CAT24C04I monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24C04/CAT24C04I then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

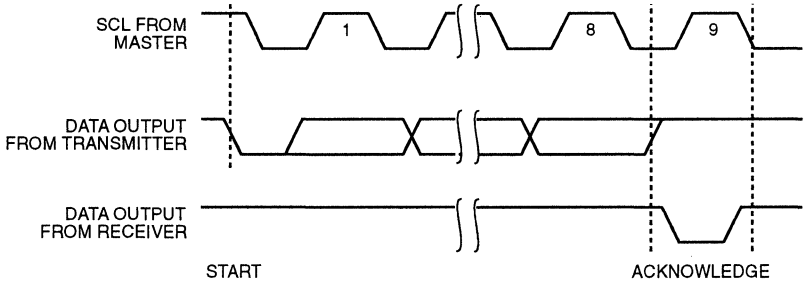
Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the eight bits of data.

The CAT24C04/CAT24C04I responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each eight bit byte.

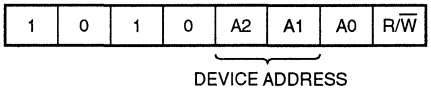
When the CAT24C04/CAT24C04I begins a READ mode it transmits eight bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24C04/CAT24C04I will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Figure 4. Acknowledge Timing



5020 FHD F06

Figure 5. Slave Address Bits



5022 FHD F08

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24C04/CAT24C04I. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT24C04/CAT24C04I acknowledges once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24C04/CAT24C04I writes up to 16 bytes of data, in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to 15 additional bytes. After each byte has been transmitted the CAT24C04/CAT24C04I will respond with an acknowledge, and internally increment the four low order address bits by one. The high order bits remain unchanged.

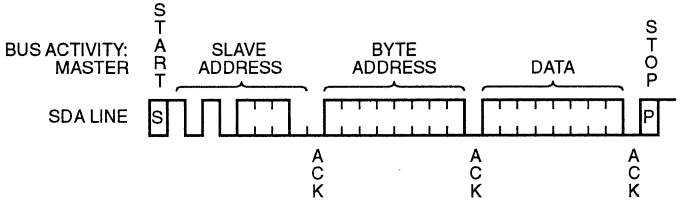
If the Master transmits more than 16 bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all 16 bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24C04/CAT24C04I in a single write cycle.

Acknowledge Polling

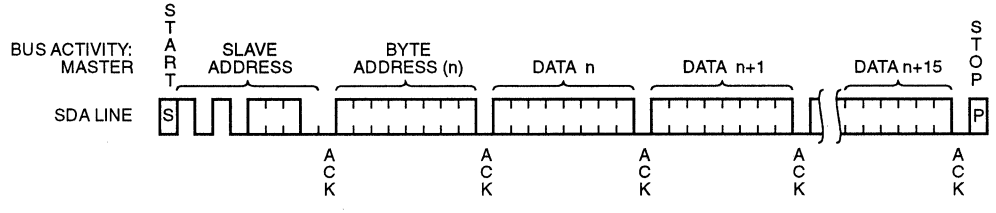
The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24C04/CAT24C04I initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24C04/CAT24C04I is still busy with the write operation, no ACK will be returned. If the CAT24C04/CAT24C04I has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Figure 6. Byte Write Timing



5020 FHD F08

Figure 7. Page Write Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

5022 FHD F09

READ OPERATIONS

The READ operation for the CAT24C04/CAT24C04I is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

Immediate Address Read

The CAT24C04/CAT24C04I's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=511, then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24C04/CAT24C04I receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Selective Read

Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24C04/CAT24C04I acknowledges the byte address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24C04/CAT24C04I then responds with its acknowledge and sends the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24C04/CAT24C04I sends the initial eight bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24C04/CAT24C04I will continue to output an eight bit byte for each acknowledge sent by the Master. The operation will terminate when the Master fails to respond with an acknowledge thus sending the STOP condition.

The data being transmitted from the CAT24C04/CAT24C04I is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24C04/CAT24C04I address bits so that the entire memory array can be read during one operation. If more than the 512 bytes are read out, the counter will 'wrap around' and continue to clock out data bytes.

2

Figure 8. Immediate Address Read Timing

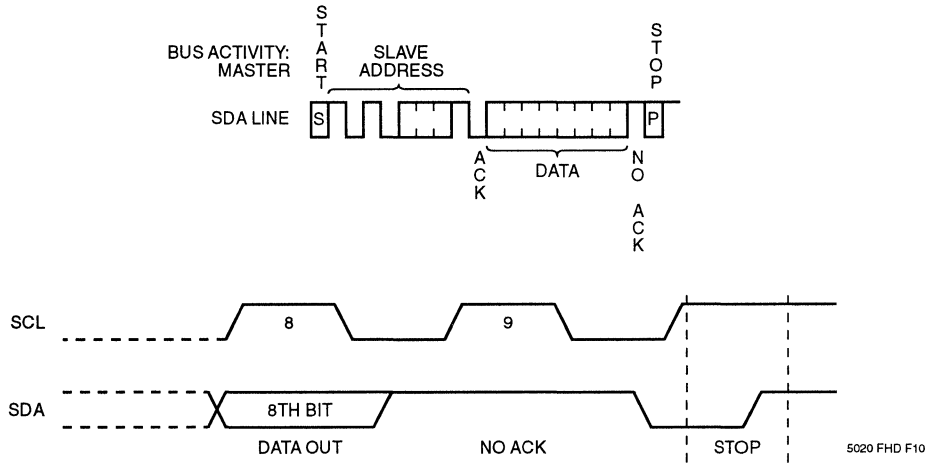


Figure 9. Selective Read Timing

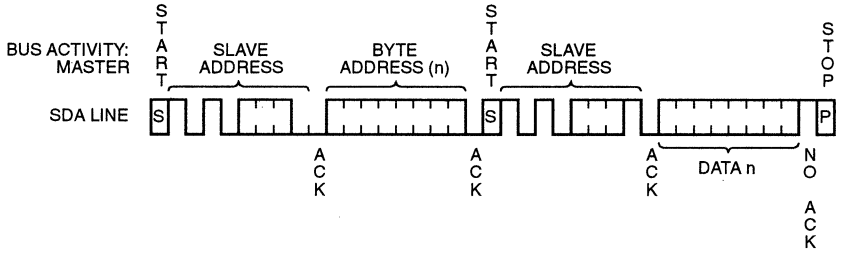


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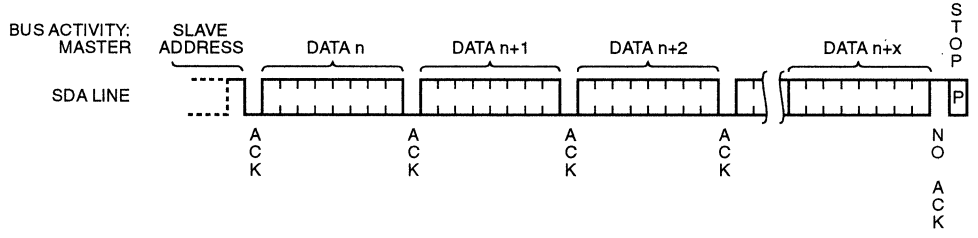
Figure 10. Sequential Read Timing



5020 FHD F12

CAT24LC04/CAT24LC04I

4K-Bit SERIAL E²PROM

FEATURES

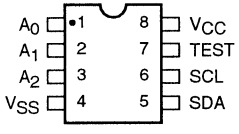
- I²C Bus Compatible*
- Low Power CMOS Technology
- 16 Byte Page Write Buffer
- Self-Timed Write Cycle with Auto-Clear
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- 8 pin DIP, 8 pin SO or 14 pin SO Package
- 3 to 6 Volt Operation
- ZERO Power™ Version (CAT24LC04Z) Available
- Optional High Endurance Device Available

DESCRIPTION

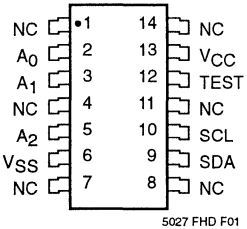
The CAT24LC04/CAT24LC04I is a 4K bit Serial CMOS E²PROM internally organized as 512 x 8 bits. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24LC04/CAT24LC04I features a 16 byte page write buffer. The device operates via the I²C bus serial interface and is available in 8 pin DIP, 8 pin SO and 14 pin SO packages.

PIN CONFIGURATION

DIP Package



SO Package



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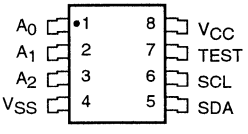
SO Package

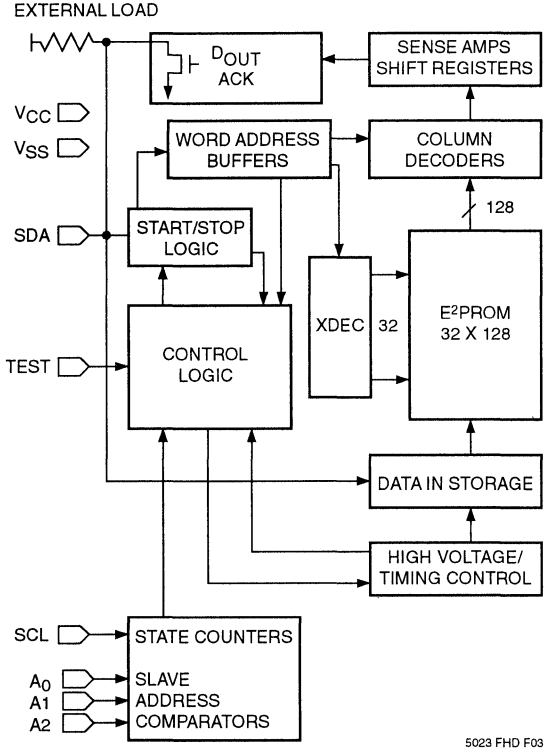


5020 FHD F01

PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
TEST	Connect to V_{SS}
V_{CC}	+3V to +6V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



5023 FHD F03

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

TD 5023

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT24LC04 T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
CAT24LC04I T_A = –40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current			3	mA	f_{SCL} = 100 KHz
I_{SB}	Standby Current V_{CC} = 6V			4	µA	V_{IN} = GND or V_{CC}
I_{SBZ}(5)	Standby Current V_{CC} = 6V			0	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	–1.0		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A0, A1, A2, SCL)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. To more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Standby Current (I_{SBZ}) = 0µA (<900nA) for the CAT24LC04Z.

A.C. CHARACTERISTICS

CAT24LC04 T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
CAT24LC04I T_A = –40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max	Units
F_{SCL}	Clock Frequency		100	KHz
T_I(3)	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5	µs
t_{BUF}(3)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		ns
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R(3)	SDA and SCL Rise Time		1	µs
t_F(3)	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Power-Up Timing(3)(6)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Write Cycle Limits

Symbol	Parameter	Min.	Typ.	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Notes:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(6) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT24LC04/CAT24LC04I supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24LC04/CAT24LC04I operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

PIN DESCRIPTIONS

SCL: Serial Clock
The serial clock input clocks all data transferred into or out of the device.

SDA: Serial Data/Address
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

A0:
A0 is unused by the CAT24LC04/CAT24LC04I but must be connected to V_{SS} to insure proper operation of the device.

A1, A2:
The inputs set the device address within the slave address bits. They must be connected to either V_{SS} or V_{CC}.

TEST:
The test pin is for Catalyst internal use only. The customer should connect this pin to V_{SS} during normal operations.

Figure 1. Bus Timing

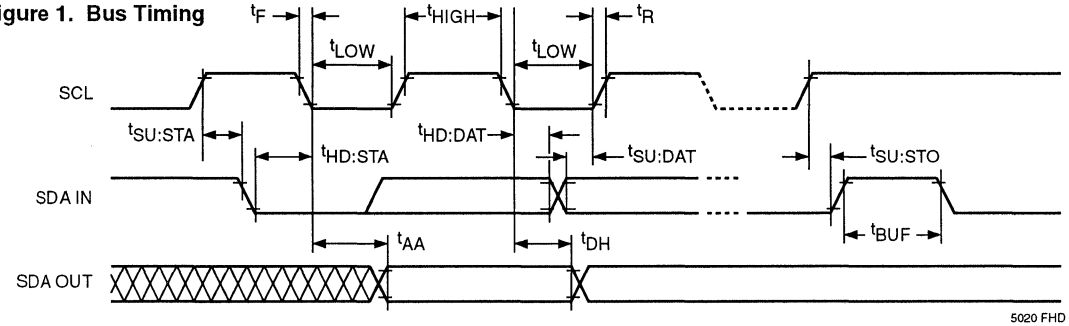


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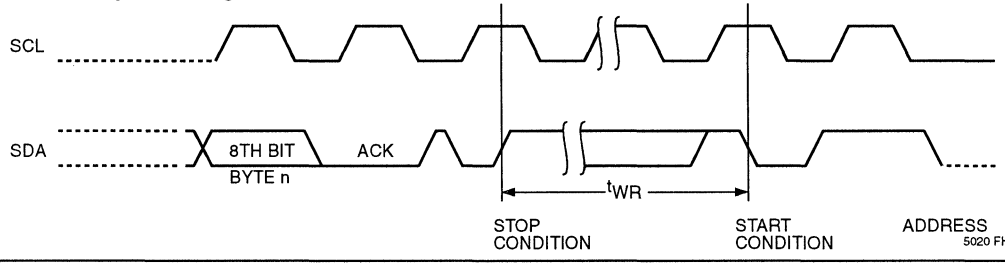
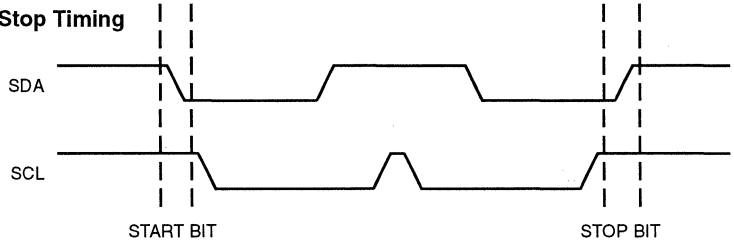
Figure 2. Write Cycle Timing



5020 FHD F04

Figure 3. Start/Stop Timing



5020 FHD F05

I²C BUS PROTOCOL

The following defines the features of the I²C bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24LC04/CAT24LC04I monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1010 for the CAT24LC04/CAT24LC04I (see Fig. 5). The next two significant bits (A2, A1) are the device address bits and define which device the Master is accessing. Up to four CAT24LC04/CAT24LC04I devices may be individually addressed by the system. The A0 bit of the slave address selects which 2K array of memory is being addressed. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0 a Write operation is selected.

After the Master sends a START condition, the CAT24LC04/CAT24LC04I monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24LC04/CAT24LC04I then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

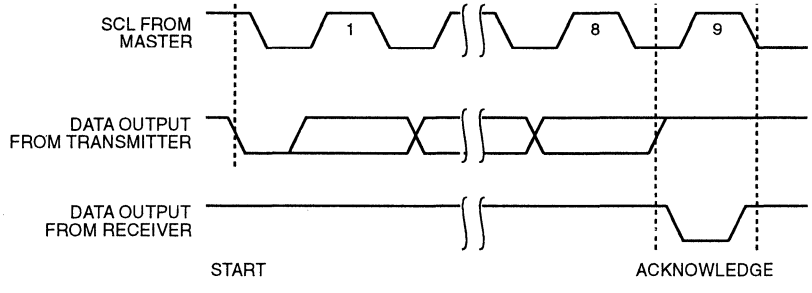
Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the eight bits of data.

The CAT24LC04/CAT24LC04I responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each eight bit byte.

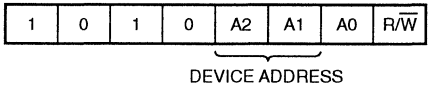
When the CAT24LC04/CAT24LC04I begins a READ mode it transmits eight bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24LC04/CAT24LC04I will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Figure 4. Acknowledge Timing



5020 FHD F06

Figure 5. Slave Address Bits



5022 FHD F08

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24LC04/CAT24LC04I. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT24LC04/CAT24LC04I acknowledges once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24LC04/CAT24LC04I writes up to 16 bytes of data, in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to 15 additional bytes. After each byte has been transmitted the CAT24LC04/CAT24LC04I will respond with an acknowledge, and internally increment the four low order address bits by one. The high order bits remain unchanged.

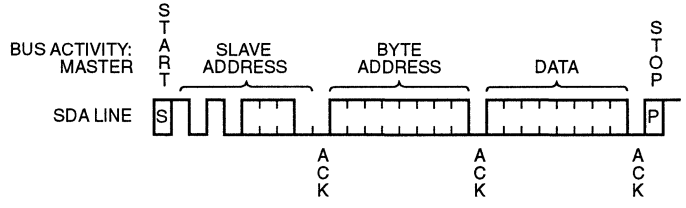
If the Master transmits more than 16 bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all 16 bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24LC04/CAT24LC04I in a single write cycle.

Acknowledge Polling

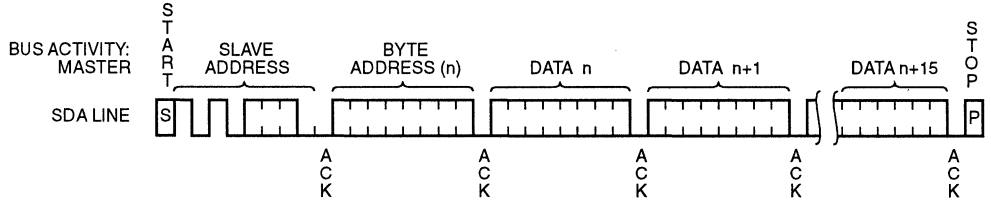
The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24LC04/CAT24LC04I initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24LC04/CAT24LC04I is still busy with the write operation, no ACK will be returned. If the CAT24LC04/CAT24LC04I has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Figure 6. Byte Write Timing



5020 FHD F08

Figure 7. Page Write Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

5022 FHD F09

READ OPERATIONS

The READ operation for the CAT24LC04/CAT24LC04I is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

Immediate Address Read

The CAT24LC04/CAT24LC04I's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=511, then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24LC04/CAT24LC04I receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Selective Read

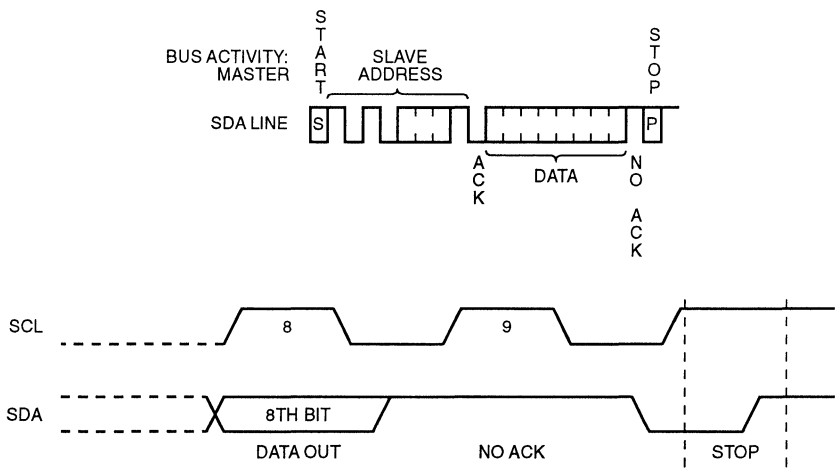
Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24LC04/CAT24LC04I acknowledges the byte address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24LC04/CAT24LC04I then responds with its acknowledge and sends the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24LC04/CAT24LC04I sends the initial eight bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24LC04/CAT24LC04I will continue to output an eight bit byte for each acknowledge sent by the Master. The operation will terminate when the Master fails to respond with an acknowledge thus sending the STOP condition.

The data being transmitted from the CAT24LC04/CAT24LC04I is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24LC04/CAT24LC04I address bits so that the entire memory array can be read during one operation. If more than the 512 bytes are read out, the counter will 'wrap around' and continue to clock out data bytes.

Figure 8. Immediate Address Read Timing



5020 FHD F10

Figure 9. Selective Read Timing

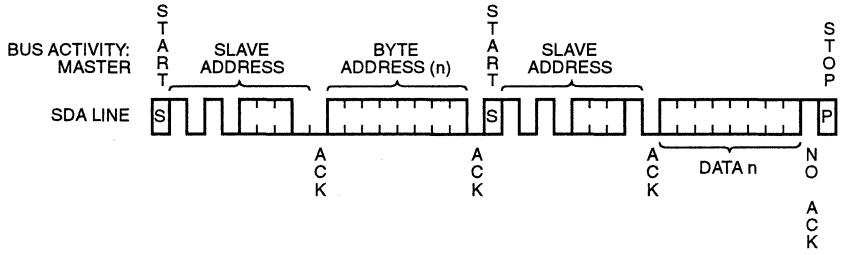


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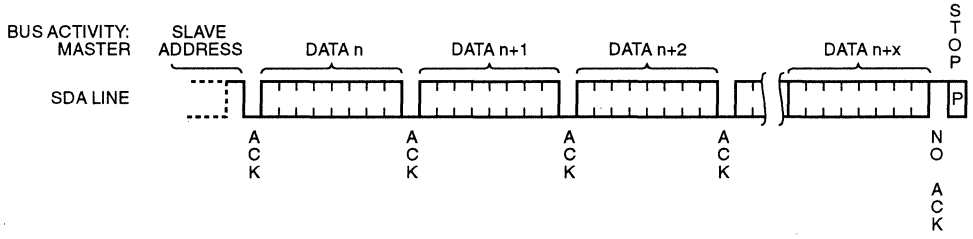
Figure 10. Sequential Read Timing



5020 FHD F12

CATALYST SEMICONDUCTOR

CAT24C08/CAT24C08I

8K-Bit SERIAL E²PROM

FEATURES

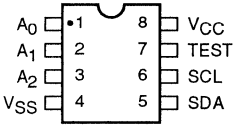
- I²C Bus Compatible*
- Low Power CMOS Technology
- 16 Byte Page Write Buffer
- Self-Timed Write Cycle with Auto-Clear
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- 8 pin DIP, 8 pin SO or 14 pin SO Package
- ZERO Power™ Version (CAT24C08Z) Available
- Optional High Endurance Device Available

DESCRIPTION

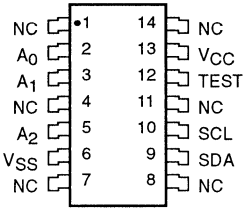
The CAT24C08/CAT24C08I is a 8K bit Serial CMOS E²PROM internally organized as 1024 x 8 bits. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24C08/CAT24C08I features a 16 byte page write buffer. The device operates via the I²C bus serial interface and is available in 8 pin DIP, 8 pin SO and 14 pin SO packages.

PIN CONFIGURATION

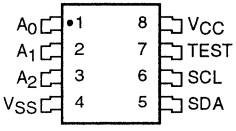
DIP Package



SO Package



SO Package



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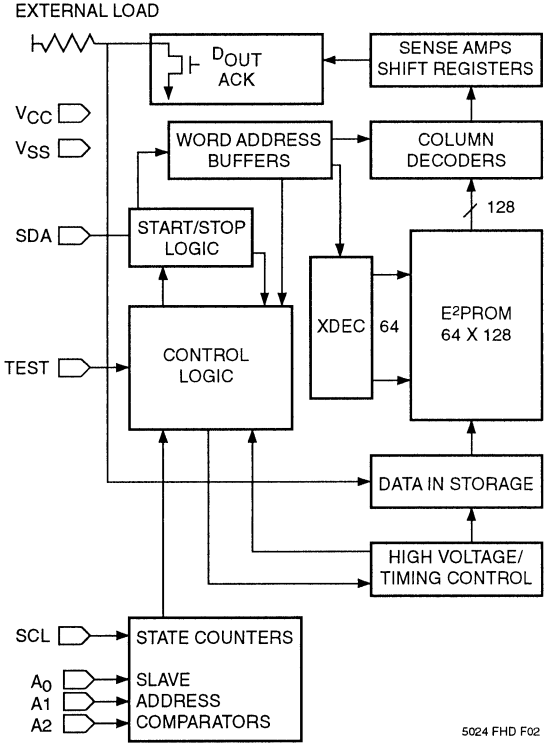
BLOCK DIAGRAM



5024 FHD F02

PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
TEST	Connect to V_{SS}
V_{CC}	+5V Power Supply
V_{SS}	Ground

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

TD 5024

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (T_a = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT24C08 T_A = 0°C to +70°C, V_{CC} = +5V to +10%, unless otherwise specified.
CAT24C08I T_A = –40°C to +85°C, V_{CC} = +5V to +10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current			3	mA	f_{SCL} = 100 KHz
I_{SB}	Standby Current V_{CC} = 5.5V			4	µA	V_{IN} = GND or V_{CC}
I_{SBZ}(5)	Standby Current V_{CC} = 5.5V			0	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	–1.0		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A0, A1, A2, SCL)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may understoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Standby Current (I_{SBZ}) = 0µA (<900nA) for the CAT24C08Z.

A.C. CHARACTERISTICS

CAT24C08 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT24C08I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max	Units
F_{SCL}	Clock Frequency		100	KHz
T_I(3)	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5	µs
t_{BUF}(3)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		ns
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R(3)	SDA and SCL Rise Time		1	µs
t_F(3)	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Power-Up Timing(3)(6)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Write Cycle Limits

Symbol	Parameter	Min.	Typ.	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Notes:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(6) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT24C08/CAT24C08I supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24C08/CAT24C08I operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated. A maximum number of two devices may be connected to the bus as determined by the device address input A2.

PIN DESCRIPTIONS

SCL: Serial Clock
The serial clock input clocks all data transferred into or out of the device.

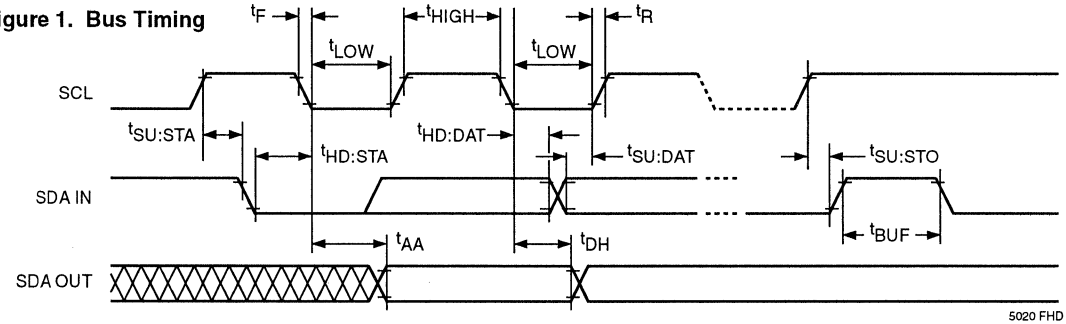
SDA: Serial Data/Address
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

A0, A1:
These pins are unused by the CAT24C08/CAT24C08I but must be connected to V_{SS} to insure proper operation of the device.

A2:
This input sets the device address within the slave address bits. It must be connected to either V_{SS} or V_{CC}.

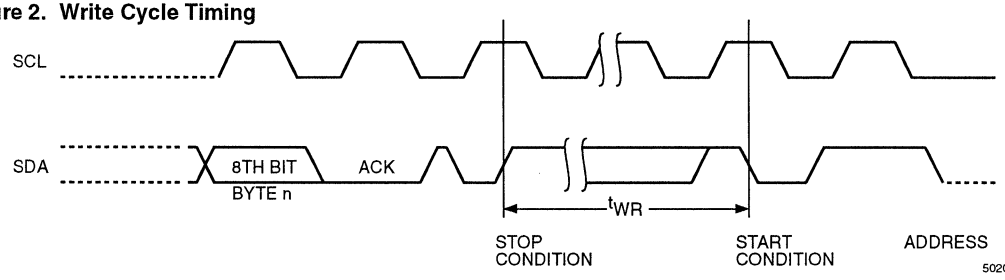
TEST:
The test pin is for Catalyst internal use only. The customer should connect this pin to V_{SS} during normal operations.

Figure 1. Bus Timing



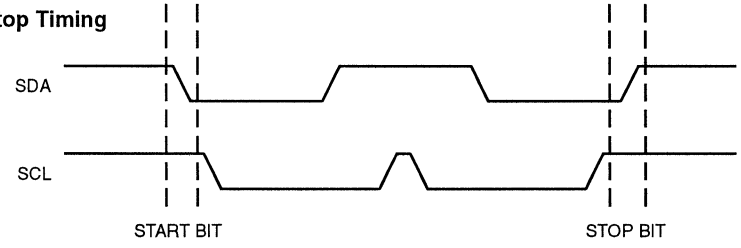
5020 FHD F03

Figure 2. Write Cycle Timing



5020 FHD F04

Figure 3. Start/Stop Timing



5020 FHD F05

I²C BUS PROTOCOL

The following defines the features of the I²C bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24C08/CAT24C08I monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1010 for the CAT24C08/CAT24C08I (see Fig. 5). The next significant bit (A2) is the device address bit and defines which device the Master is accessing. Two CAT24C08/CAT24C08I devices may be individually addressed by the system. The next two bits of the slave address (A1, A0) selects which 2K array of memory is being addressed. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0 a Write operation is selected.

After the Master sends a START condition, the CAT24C08/CAT24C08I monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24C08/CAT24C08I then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

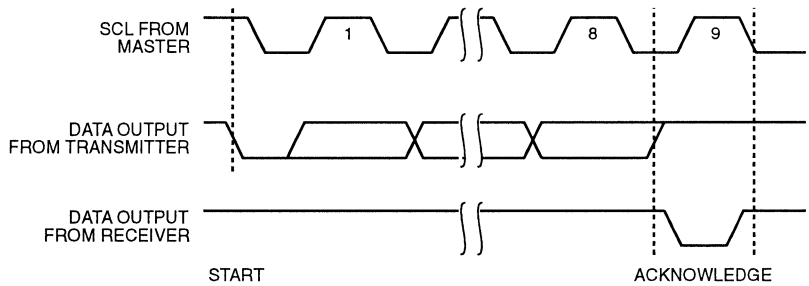
Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the eight bits of data.

The CAT24C08/CAT24C08I responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each eight bit byte.

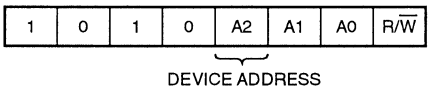
When the CAT24C08/CAT24C08I begins a READ mode it transmits eight bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24C08/CAT24C08I will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Figure 4. Acknowledge Timing



5020 FHD F06

Figure 5. Slave Address Bits



5024 FHD F07

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24C08/CAT24C08I. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT24C08/CAT24C08I acknowledges once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24C08/CAT24C08I writes up to 16 bytes of data, in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to 15 additional bytes. After each byte has been transmitted the CAT24C08/CAT24C08I will respond with an acknowledge, and internally increment the four low order address bits by one. The high order bits remain unchanged.

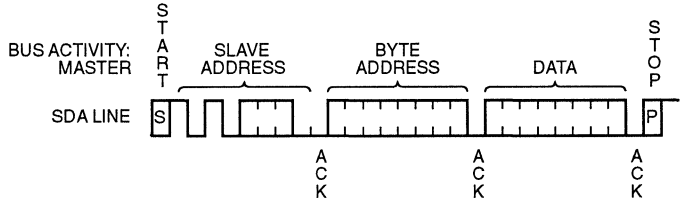
If the Master transmits more than 16 bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all 16 bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24C08/CAT24C08I in a single write cycle.

Acknowledge Polling

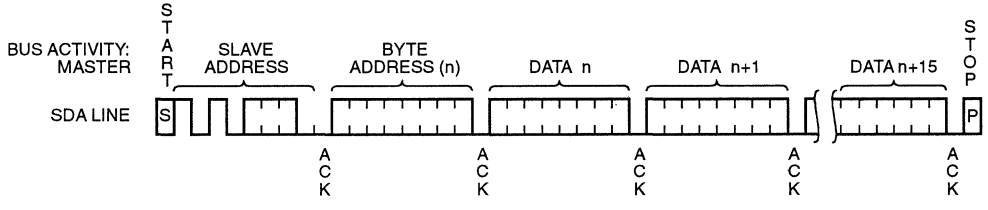
The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24C08/CAT24C08I initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24C08/CAT24C08I is still busy with the write operation, no ACK will be returned. If the CAT24C08/CAT24C08I has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Figure 6. Byte Write Timing



5020 FHD F08

Figure 7. Page Write Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

5022 FHD F09

READ OPERATIONS

The READ operation for the CAT24C08/CAT24C08I is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

Immediate Address Read

The CAT24C08/CAT24C08I's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=1023, then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24C08/CAT24C08I receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Selective Read

Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24C08/CAT24C08I acknowledges the byte address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24C08/CAT24C08I then responds with its acknowledge and sends the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

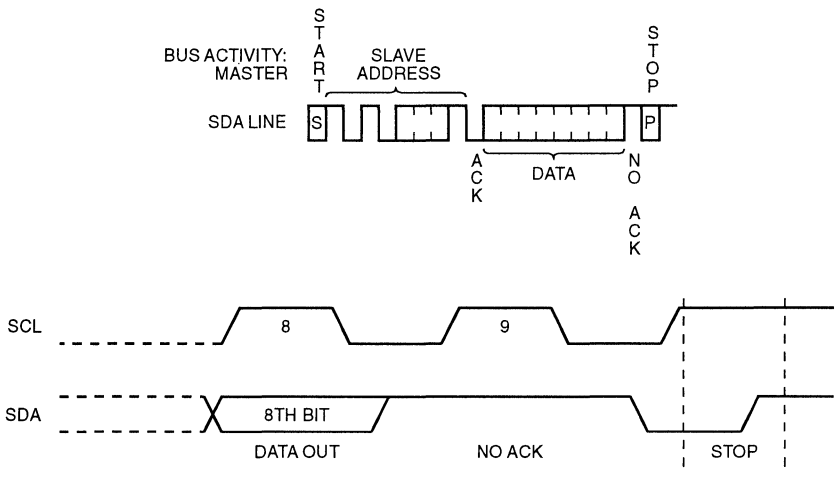
Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24C08/CAT24C08I sends the initial eight bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24C08/CAT24C08I will continue to output an eight bit byte for each acknowledge sent by the Master. The operation will terminate when the Master fails to respond with an acknowledge thus sending the STOP condition.

The data being transmitted from the CAT24C08/CAT24C08I is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24C08/CAT24C08I address bits so that the entire memory array can be read during one operation. If more than the 1024 bytes are read out, the counter will 'wrap around' and continue to clock out data bytes.

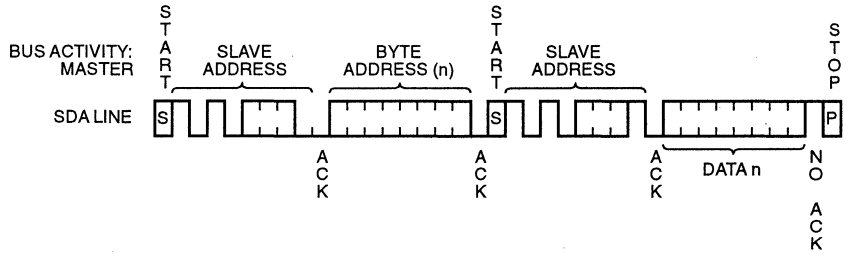
2

Figure 8. Immediate Address Read Timing



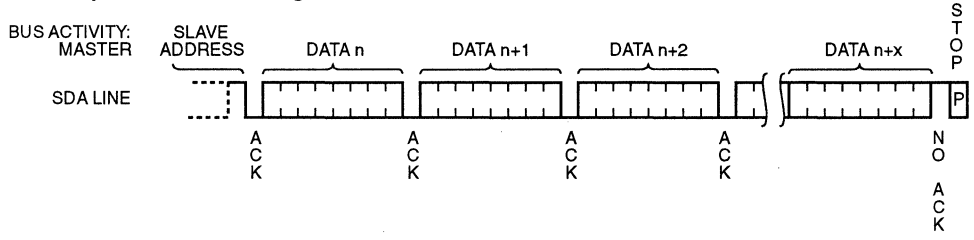
5020 FHD F10

Figure 9. Selective Read Timing



5020 FHD F11

Figure 10. Sequential Read Timing



5020 FHD F12

CAT24LC08/CAT24LC08I

8K-Bit SERIAL E²PROM

FEATURES

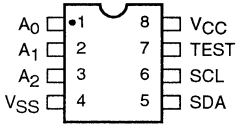
- I²C Bus Compatible*
- Low Power CMOS Technology
- 16 Byte Page Write Buffer
- Self-Timed Write Cycle with Auto-Clear
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- 8 pin DIP, 8 pin SO or 14 pin SO Package
- 3 to 6 Volt Operation
- ZERO Power™ Version (CAT24LC08Z) Available
- Optional High Endurance Device Available

DESCRIPTION

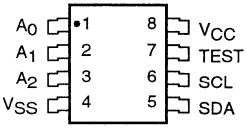
The CAT24LC08/CAT24LC08I is a 8K bit Serial CMOS E²PROM internally organized as 1024 x 8 bits. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24LC08/CAT24LC08I features a 16 byte page write buffer. The device operates via the I²C bus serial interface and is available in 8 pin DIP, 8 pin SO and 14 pin SO packages.

PIN CONFIGURATION

DIP Package

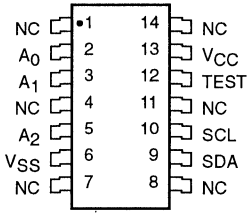


SO Package



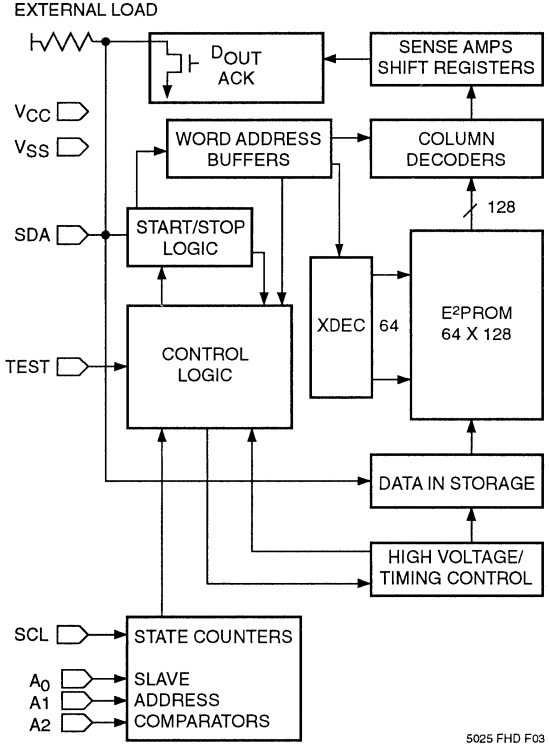
5023 FHD F01

SO Package



5023 FHD F02

BLOCK DIAGRAM



5025 FHD F03

PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
TEST	Connect to V_{SS}
V_{CC}	+3V to +6V Power Supply
V_{SS}	Ground

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

TD 5025

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT24LC08 T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
CAT24LC08I T_A = –40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current			3	mA	f_{SCL} = 100 KHz
I_{SB}	Standby Current V_{CC} = 6V			4	µA	V_{IN} = GND or V_{CC}
I_{SBZ}(5)	Standby Current V_{CC} = 6V			0	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	–1.0		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A0, A1, A2, SCL)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. To more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Standby Current (I_{SBZ}) = 0µA (<900nA) for the CAT24LC08Z.

A.C. CHARACTERISTICS

CAT24LC08 T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
CAT24LC08I T_A = –40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max	Units
F_{SCL}	Clock Frequency		100	KHz
T_I(3)	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5	µs
t_{BUF}(3)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		ns
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R(3)	SDA and SCL Rise Time		1	µs
t_F(3)	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Power-Up Timing(3)(6)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Write Cycle Limits

Symbol	Parameter	Min.	Typ.	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Notes:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(6) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT24LC08/CAT24LC08I supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24LC08/CAT24LC08I operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated. A maximum number of two devices may be connected to the bus as determined by the device address input A2.

PIN DESCRIPTIONS

SCL: Serial Clock
The serial clock input clocks all data transferred into or out of the device.

SDA: Serial Data/Address
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

A0, A1:
These pins are unused by the CAT24LC08/CAT24LC08I but must be connected to V_{SS} to insure proper operation of the device.

A2:
This input sets the device address within the slave address bits. It must be connected to either V_{SS} or V_{CC}.

TEST:
The test pin is for Catalyst internal use only. The customer should connect this pin to V_{SS} during normal operations.

Figure 1. Bus Timing

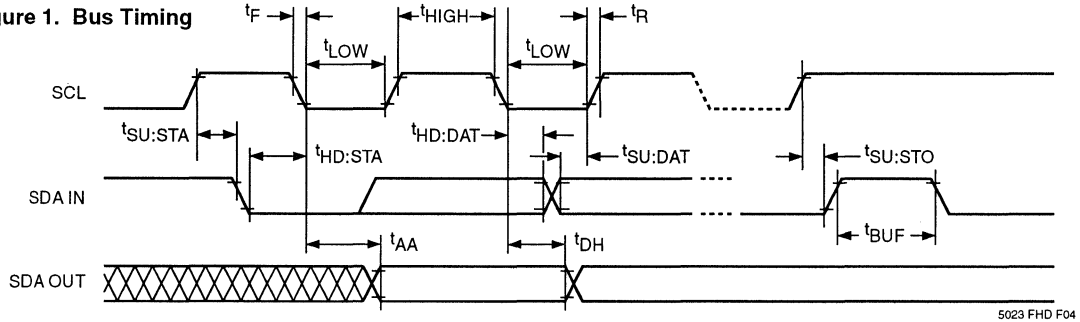


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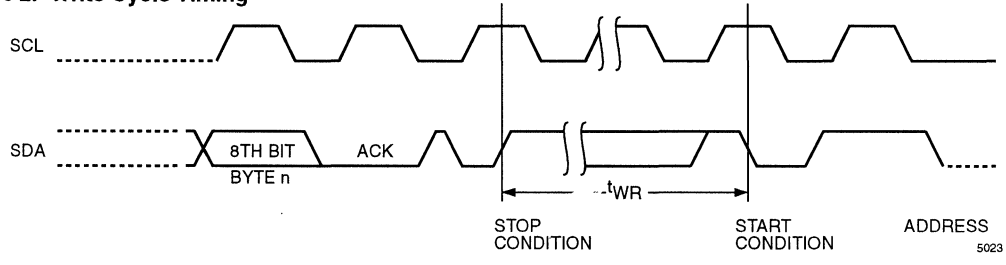
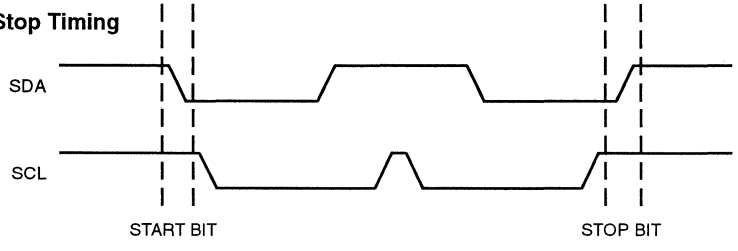
Figure 2. Write Cycle Timing



5023 FHD F05

Figure 3. Start/Stop Timing



5020 FHD F05

I²C BUS PROTOCOL

The following defines the features of the I²C bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24LC08/CAT24LC08I monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1010 for the CAT24LC08/CAT24LC08I (see Fig. 5). The next significant bit (A2) is the device address bit and defines which device the Master is accessing. Two CAT24LC08/CAT24LC08I devices may be individually addressed by the system. The next two bits of the slave address (A1, A0) selects which 2K array of memory is being addressed. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0 a Write operation is selected.

After the Master sends a START condition, the CAT24LC08/CAT24LC08I monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24LC08/CAT24LC08I then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

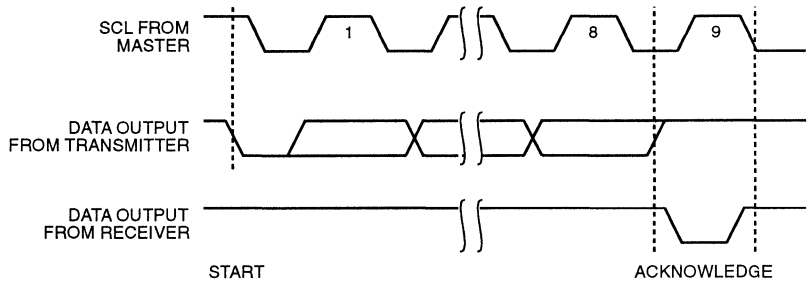
Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the eight bits of data.

The CAT24LC08/CAT24LC08I responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each eight bit byte.

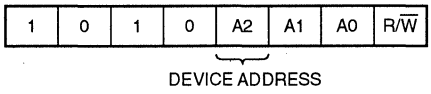
When the CAT24LC08/CAT24LC08I begins a READ mode it transmits eight bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24LC08/CAT24LC08I will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Figure 4. Acknowledge Timing



5020 FHD F06

Figure 5. Slave Address Bits



5024 FHD F07

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24LC08/CAT24LC08I. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT24LC08/CAT24LC08I acknowledges once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24LC08/CAT24LC08I writes up to 16 bytes of data, in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to 15 additional bytes. After each byte has been transmitted the CAT24LC08/CAT24LC08I will respond with an acknowledge, and internally increment the four low order address bits by one. The high order bits remain unchanged.

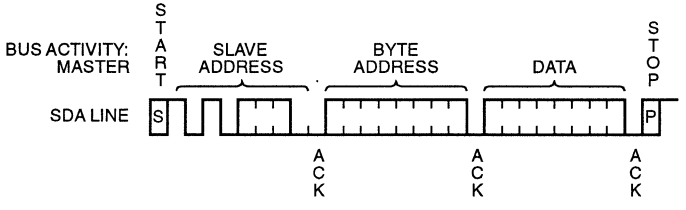
If the Master transmits more than 16 bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all 16 bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24LC08/CAT24LC08I in a single write cycle.

Acknowledge Polling

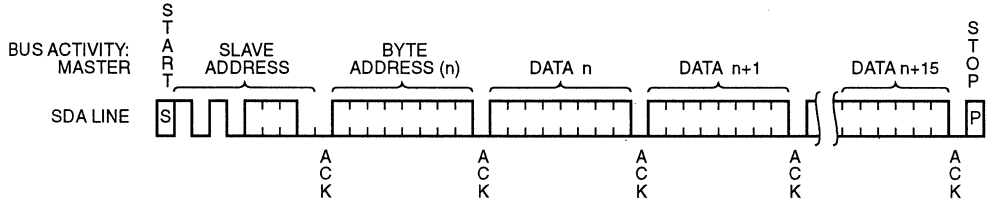
The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24LC08/CAT24LC08I initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24LC08/CAT24LC08I is still busy with the write operation, no ACK will be returned. If the CAT24LC08/CAT24LC08I has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Figure 6. Byte Write Timing



5020 FHD F08

Figure 7. Page Write Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

5022 FHD F09

READ OPERATIONS

The READ operation for the CAT24LC08/CAT24LC08I is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

Immediate Address Read

The CAT24LC08/CAT24LC08I's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=1023, then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24LC08/CAT24LC08I receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Selective Read

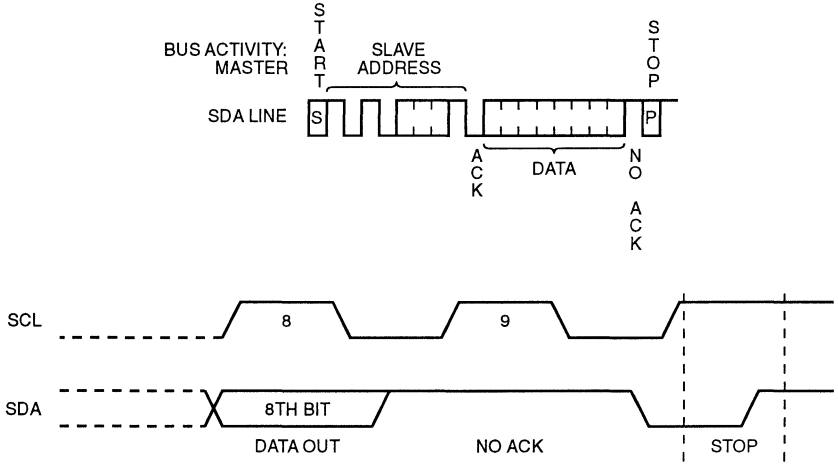
Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24LC08/CAT24LC08I acknowledges the byte address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24LC08/CAT24LC08I then responds with its acknowledge and sends the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24LC08/CAT24LC08I sends the initial eight bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24LC08/CAT24LC08I will continue to output an eight bit byte for each acknowledge sent by the Master. The operation will terminate when the Master fails to respond with an acknowledge thus sending the STOP condition.

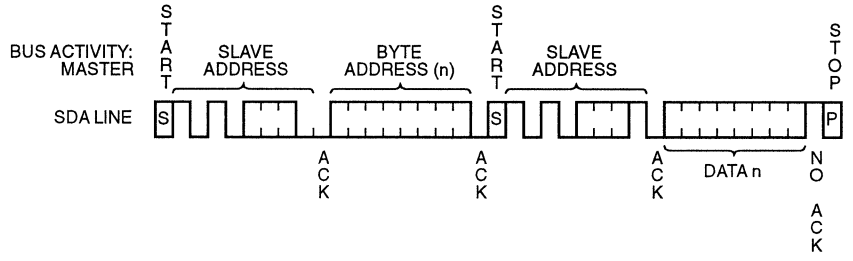
The data being transmitted from the CAT24LC08/CAT24LC08I is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24LC08/CAT24LC08I address bits so that the entire memory array can be read during one operation. If more than the 1024 bytes are read out, the counter will 'wrap around' and continue to clock out data bytes.

Figure 8. Immediate Address Read Timing



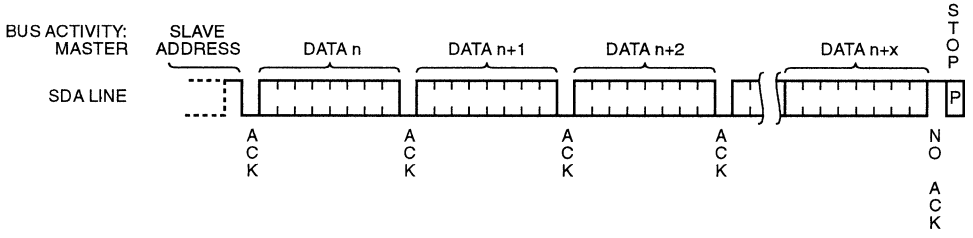
5020 FHD F10

Figure 9. Selective Read Timing



5020 FHD F11

Figure 10. Sequential Read Timing



5020 FHD F12

CAT24C16/CAT24C16I

16K-Bit SERIAL E²PROM

FEATURES

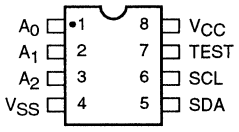
- I²C Bus Compatible*
- Low Power CMOS Technology
- 16 Byte Page Write Buffer
- Self-Timed Write Cycle with Auto-Clear
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- 8 pin DIP, 8 pin SO or 14 pin SO Package
- ZERO Power™ Version (CAT24C16Z) Available
- Optional High Endurance Device Available

DESCRIPTION

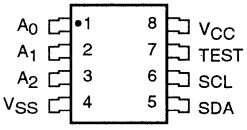
The CAT24C16/CAT24C16I is a 16K bit Serial CMOS E²PROM internally organized as 2048 x 8 bits. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24C16/CAT24C16I features a 16 byte page write buffer. The device operates via the I²C bus serial interface and is available in 8 pin DIP, 8 pin SO and 14 pin SO packages.

PIN CONFIGURATION

DIP Package

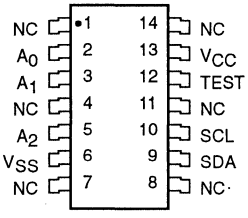


SO Package



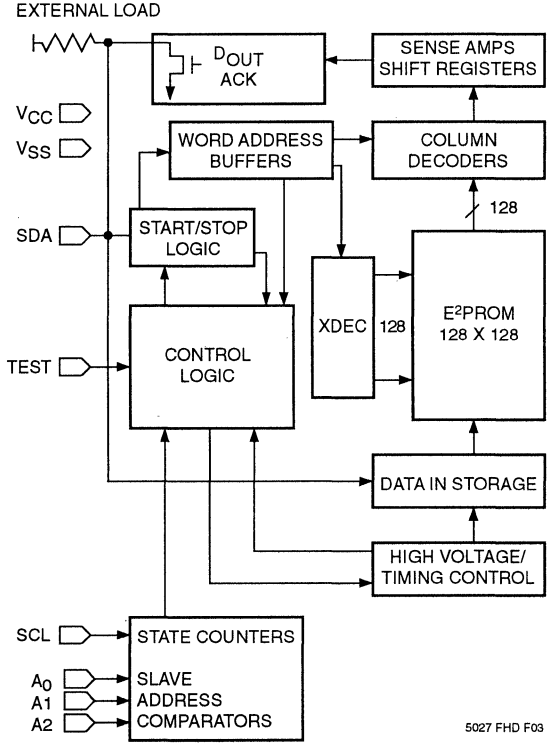
5023 FHD F01

SO Package



5023 FHD F02

BLOCK DIAGRAM



5027 FHD F03

PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
TEST	Connect to VSS
VCC	+5V Power Supply
VSS	Ground

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

TD 5027

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT24C16 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT24C16I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current			3	mA	f_{SCL} = 100 KHz
I_{SB}	Standby Current V_{CC} = 5.5V			4	µA	V_{IN} = GND or V_{CC}
I_{SBZ}(5)	Standby Current V_{CC} = 5.5V			0	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	–1.0		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A0, A1, A2, SCL)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. To more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Standby Current (I_{SBZ}) = 0µA (<900nA) for the CAT24C16Z.

A.C. CHARACTERISTICS

CAT24C16 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT24C16I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max	Units
F_{SCL}	Clock Frequency		100	KHz
T_I(3)	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5	µs
t_{BUF}(3)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		ns
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R(3)	SDA and SCL Rise Time		1	µs
t_F(3)	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Power-Up Timing(3)(6)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Write Cycle Limits

Symbol	Parameter	Min.	Typ.	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Notes:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(6) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT24C16/CAT24C16I supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24C16/CAT24C16I operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

PIN DESCRIPTIONS

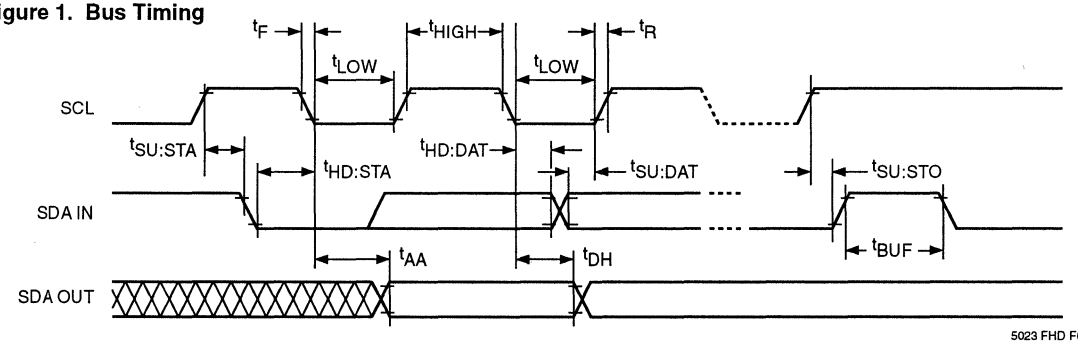
SCL: Serial Clock
The serial clock input clocks all data transferred into or out of the device.

SDA: Serial Data/Address
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

A0, A1, A2: Device Address Inputs
These pins are unused by the CAT24C16/CAT24C16I, but must be connected to V_{SS} to insure proper operation of the device.

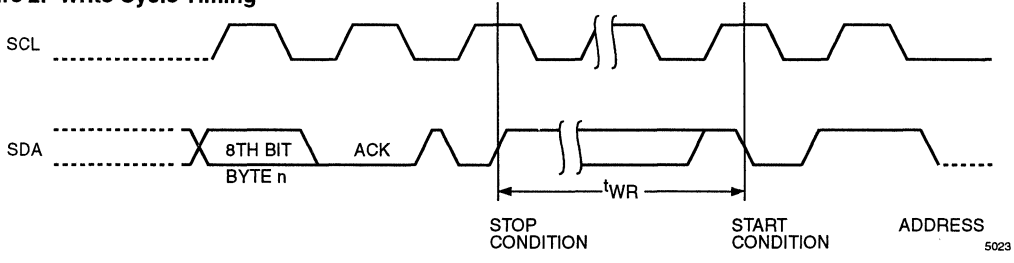
TEST: The test pin is for Catalyst internal use only. The customer should connect this pin to V_{SS} during normal operations.

Figure 1. Bus Timing



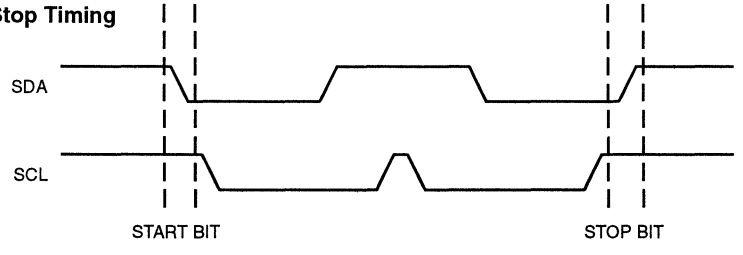
5023 FHD F04

Figure 2. Write Cycle Timing



5023 FHD F05

Figure 3. Start/Stop Timing



5020 FHD F05

I²C BUS PROTOCOL

The following defines the features of the I²C bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24C16/CAT24C16I monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1010 for the CAT24C16/CAT24C16I (see Fig. 5). The next three bits of the slave address (A2, A1, A0) selects which 2K array of memory is being addressed. Only one CAT24C16/CAT24C16I may be accessed by the system. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0 a Write operation is selected.

After the Master sends a START condition, the CAT24C16/CAT24C16 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24C16/CAT24C16I then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

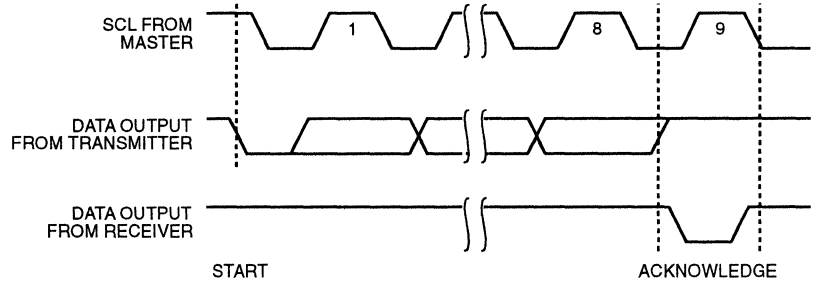
Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the eight bits of data.

The CAT24C16/CAT24C16I responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each eight bit byte.

When the CAT24C16/CAT24C16I begins a READ mode it transmits eight bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24C16/CAT24C16I will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Figure 4. Acknowledge Timing



5020 FHD F06

Figure 5. Slave Address Bits

1	0	1	0	A2	A1	A0	R/$\overline{W}$

5027 FHD F07

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24C16/CAT24C16I. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT24C16/CAT24C16I acknowledges once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24C16/CAT24C16I writes up to 16 bytes of data, in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to 15 additional bytes. After each byte has been transmitted the CAT24C16/CAT24C16I will respond with an acknowledge, and internally increment the four low order address bits by one. The high order bits remain unchanged.

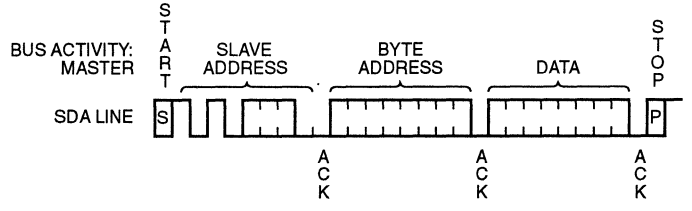
If the Master transmits more than 16 bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all 16 bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24C16/CAT24C16I in a single write cycle.

Acknowledge Polling

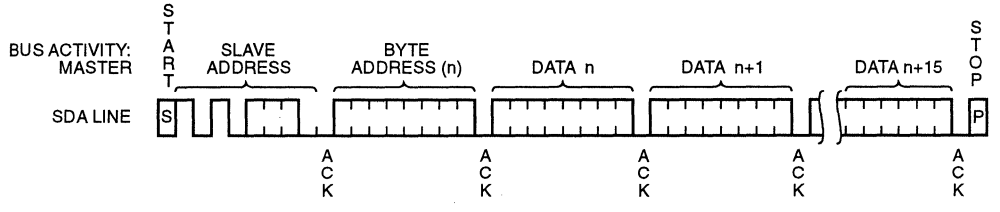
The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24C16/CAT24C16I initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24C16/CAT24C16I is still busy with the write operation, no ACK will be returned. If the CAT24C16/CAT24C16I has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Figure 6. Byte Write Timing



5020 FHD F08

Figure 7. Page Write Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

5022 FHD F09

READ OPERATIONS

The READ operation for the CAT24C16/CAT24C16I is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

Immediate Address Read

The CAT24C16/CAT24C16I's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=2047, then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24C16/CAT24C16I receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Selective Read

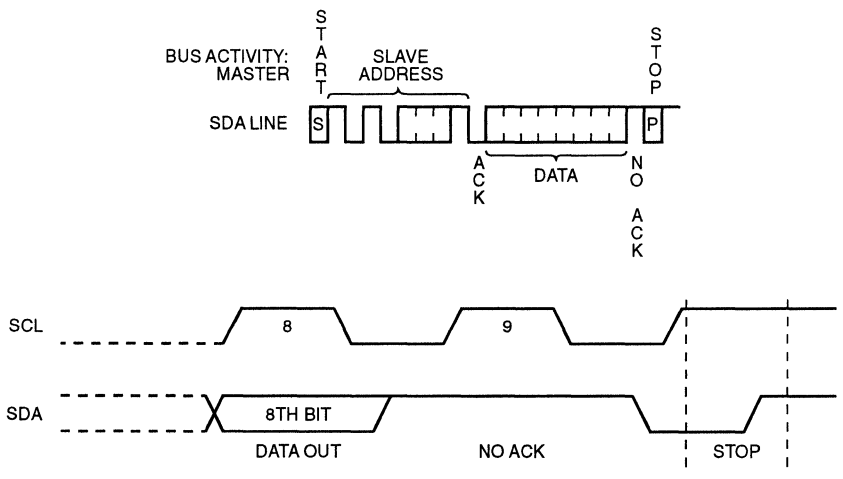
Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24C16/CAT24C16I acknowledges the byte address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24C16/CAT24C16I then responds with its acknowledge and sends the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24C16/CAT24C16I sends the initial eight bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24C16/CAT24C16I will continue to output an eight bit byte for each acknowledge sent by the Master. The operation will terminate when the Master fails to respond with an acknowledge thus sending the STOP condition.

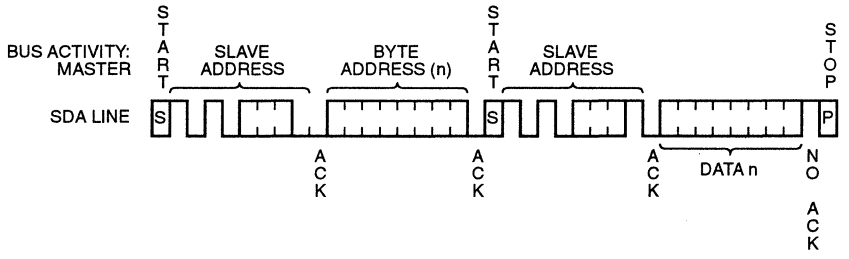
The data being transmitted from the CAT24C16/CAT24C16I is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24C16/CAT24C16I address bits so that the entire memory array can be read during one operation. If more than the 2048 bytes are read out, the counter will 'wrap around' and continue to clock out data bytes.

Figure 8. Immediate Address Read Timing



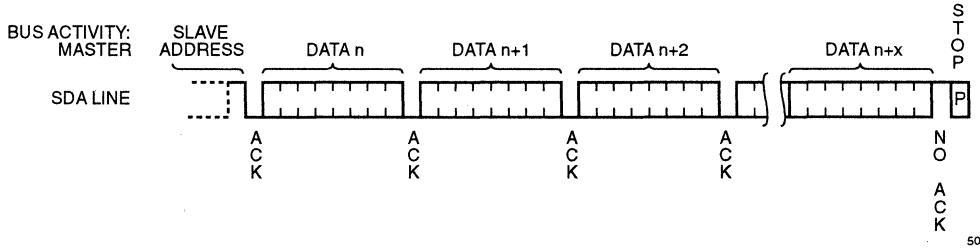
5020 FHD F10

Figure 9. Selective Read Timing



5020 FHD F11

Figure 10. Sequential Read Timing



5020 FHD F12

CAT24LC16/CAT24LC16I

16K-Bit SERIAL E²PROM

FEATURES

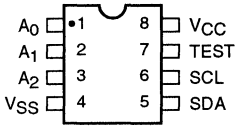
- I²C Bus Compatible*
- Low Power CMOS Technology
- 16 Byte Page Write Buffer
- Self-Timed Write Cycle with Auto-Clear
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- 8 pin DIP, 8 pin SO or 14 pin SO Package
- 3 to 6 Volt Operation
- ZERO Power™ Version (CAT24LC16Z) Available
- Optional High Endurance Device Available

DESCRIPTION

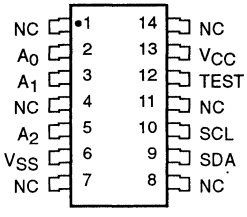
The CAT24LC16/CAT24LC16I is a 16K bit Serial CMOS E²PROM internally organized as 2048 x 8 bits. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24LC16/CAT24LC16I features a 16 byte page write buffer. The device operates via the I²C bus serial interface and is available in 8 pin DIP, 8 pin SO and 14 pin SO packages.

PIN CONFIGURATION

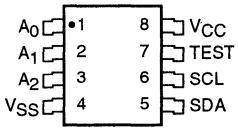
DIP Package



SO Package

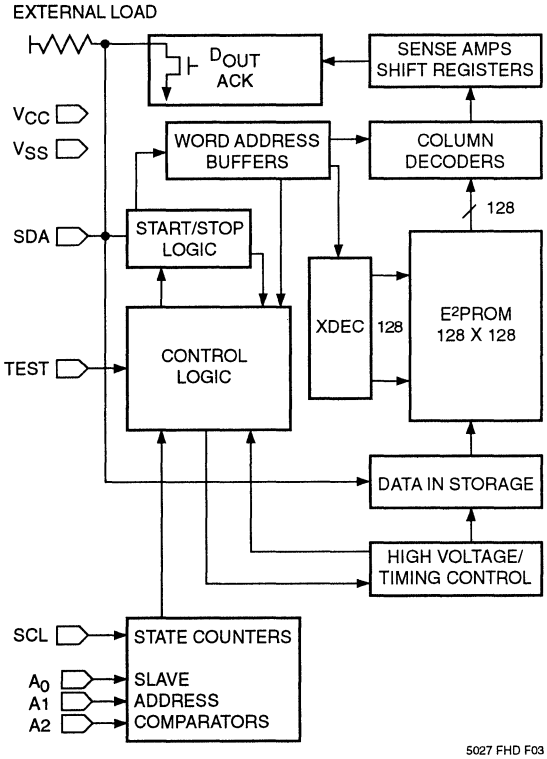


SO Package



5022 FHD F01

BLOCK DIAGRAM



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PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
TEST	Connect to VSS
VCC	+3V to +6V Power Supply
VSS	Ground

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

TD 5026

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT24LC16 T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
CAT24LC16I T_A = –40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current			3	mA	f_{SCL} = 100 KHz
I_{SB}	Standby Current V_{CC} = 6V			4	µA	V_{IN} = GND or V_{CC}
I_{SBZ}(5)	Standby Current V_{CC} = 6V			0	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	–1.0		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A0, A1, A2, SCL)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Standby Current (I_{SBZ}) = 0µA (<900nA) for the CAT24LC16Z.

A.C. CHARACTERISTICS

CAT24LC16 T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
CAT24LC16I T_A = –40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max	Units
F_{SCL}	Clock Frequency		100	KHz
T_I(3)	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5	µs
t_{BUF}(3)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		ns
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R(3)	SDA and SCL Rise Time		1	µs
t_F(3)	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Power-Up Timing(3)(6)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Write Cycle Limits

Symbol	Parameter	Min.	Typ.	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(6) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT24LC16/CAT24LC16I supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24LC16/CAT24LC16I operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

PIN DESCRIPTIONS

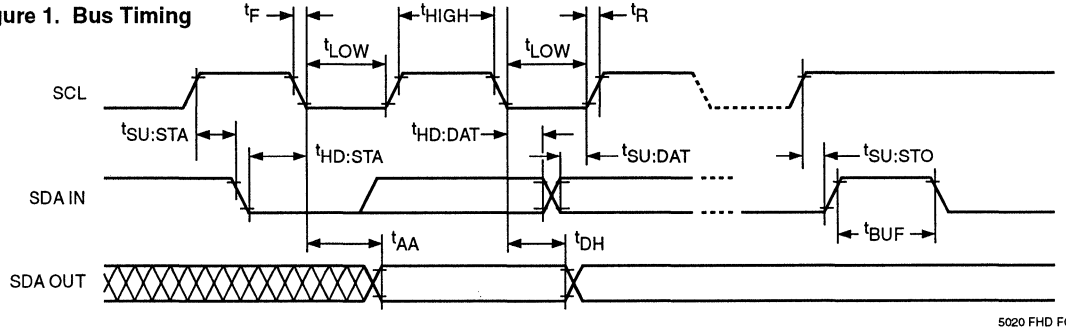
SCL: Serial Clock
The serial clock input clocks all data transferred into or out of the device.

SDA: Serial Data/Address
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

A0, A1, A2: Device Address Inputs
These pins are unused by the CAT24LC16/CAT24LC16I, but must be connected to V_{SS} to insure proper operation of the device.

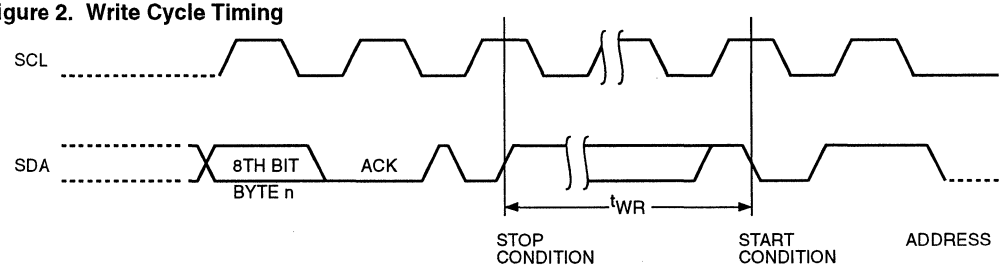
TEST: The test pin is for Catalyst internal use only. The customer should connect this pin to V_{SS} during normal operations.

Figure 1. Bus Timing



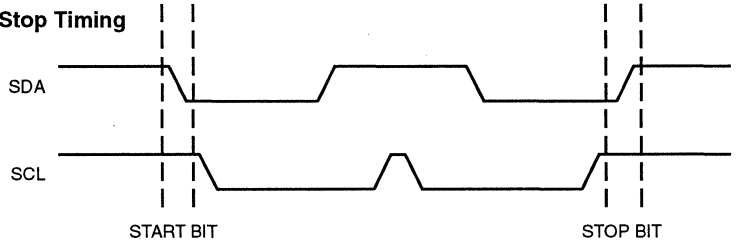
5020 FHD F03

Figure 2. Write Cycle Timing



5020 FHD F04

Figure 3. Start/Stop Timing



5020 FHD F05

I²C BUS PROTOCOL

The following defines the features of the I²C bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24LC16/CAT24LC16I monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1010 for the CAT24LC16/CAT24LC16I (see Fig. 5). The next three bits of the slave address (A2, A1, A0) selects which 2K array of memory is being addressed. Only one CAT24LC16/CAT24LC16I may be accessed by the system. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0 a Write operation is selected.

After the Master sends a START condition, the CAT24LC16/CAT24LC16 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24LC16/CAT24LC16I then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

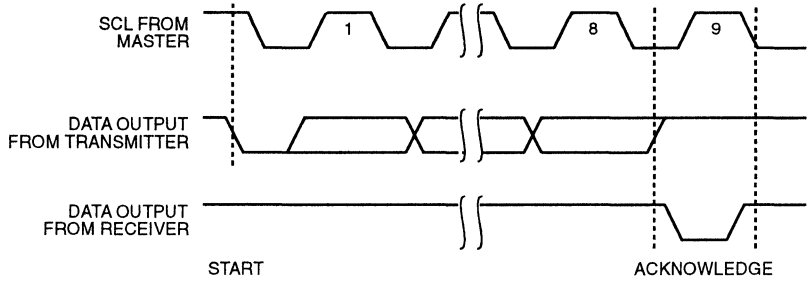
Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the eight bits of data.

The CAT24LC16/CAT24LC16I responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each eight bit byte.

When the CAT24LC16/CAT24LC16I begins a READ mode it transmits eight bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24LC16/CAT24LC16I will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Figure 4. Acknowledge Timing



5020 FHD F06

Figure 5. Slave Address Bits

1	0	1	0	A2	A1	A0	R/$\overline{W}$

5027 FHD F07

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24LC16/CAT24LC16I. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT24LC16/CAT24LC16I acknowledges once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24LC16/CAT24LC16I writes up to 16 bytes of data, in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to 15 additional bytes. After each byte has been transmitted the CAT24LC16/CAT24LC16I will respond with an acknowledge, and internally increment the four low order address bits by one. The high order bits remain unchanged.

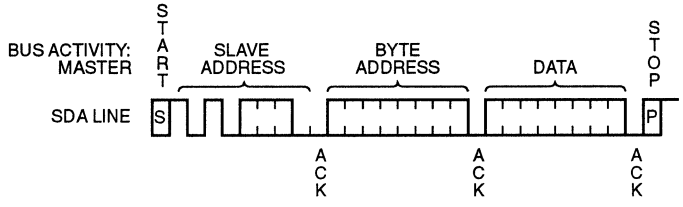
If the Master transmits more than 16 bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all 16 bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24LC16/CAT24LC16I in a single write cycle.

Acknowledge Polling

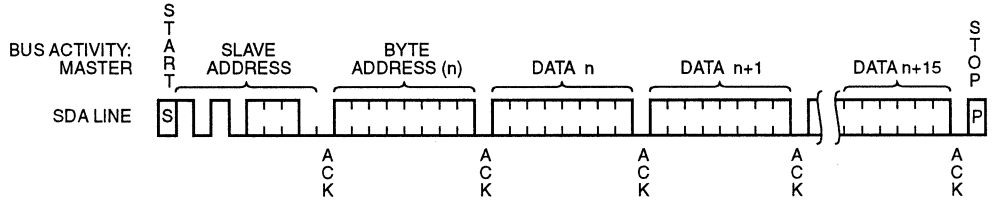
The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24LC16/CAT24LC16I initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24LC16/CAT24LC16I is still busy with the write operation, no ACK will be returned. If the CAT24LC16/CAT24LC16I has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Figure 6. Byte Write Timing



5020 FHD F08

Figure 7. Page Write Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

5026 FHD F09

READ OPERATIONS

The READ operation for the CAT24LC16/CAT24LC16I is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

Immediate Address Read

The CAT24LC16/CAT24LC16I's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=2047, then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24LC16/CAT24LC16I receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Selective Read

Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24LC16/CAT24LC16I acknowledges the byte address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24LC16/CAT24LC16I then responds with its acknowledge and sends the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

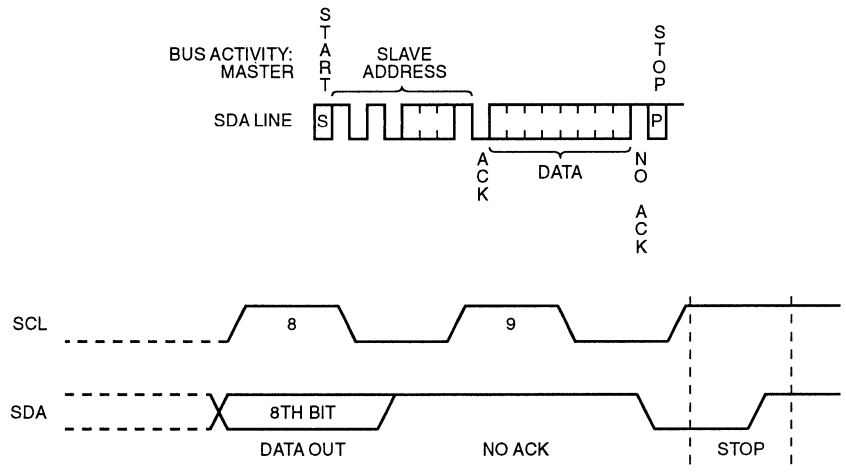
Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24LC16/CAT24LC16I sends the initial eight bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24LC16/CAT24LC16I will continue to output an eight bit byte for each acknowledge sent by the Master. The operation will terminate when the Master fails to respond with an acknowledge thus sending the STOP condition.

The data being transmitted from the CAT24LC16/CAT24LC16I is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24LC16/CAT24LC16I address bits so that the entire memory array can be read during one operation. If more than the 2048 bytes are read out, the counter will 'wrap around' and continue to clock out data bytes.

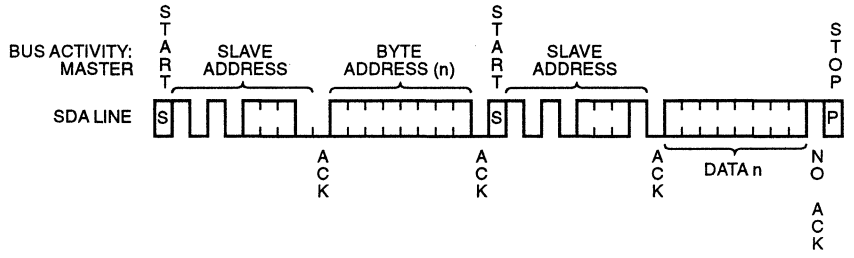
2

Figure 8. Immediate Address Read Timing



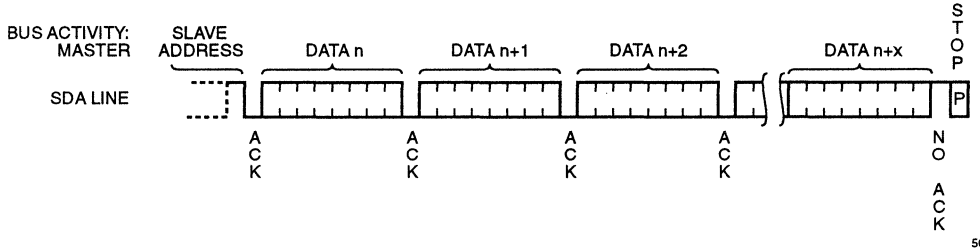
5020 FHD F10

Figure 9. Selective Read Timing



5020 FHD F11

Figure 10. Sequential Read Timing



5020 FHD F12

CAT24C32/CAT24C32I

32K-Bit SERIAL E²PROM

FEATURES

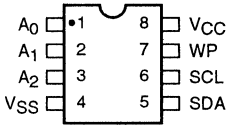
- I²C Bus Compatible*
- Low Power CMOS Technology
- 32 Byte Page Write Buffer
- Self-Timed Write Cycle with Auto-Clear
- Hardware Block Write Protect
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- 8 pin DIP or 14 pin SO Package
- ZERO Power™ Version (CAT24C32Z) Available
- Optional High Endurance Device Available

DESCRIPTION

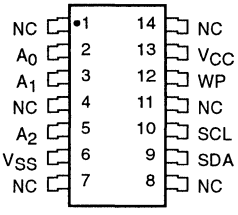
The CAT24C32/CAT24C32I is a 32K bit Serial CMOS E²PROM internally organized as 4096 x 8 bits. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24C32/CAT24C32I features a 32 byte page write buffer. The device operates via the I²C bus serial interface and is available in 8 pin DIP and 14 pin SO packages.

PIN CONFIGURATION

DIP Package



SO Package



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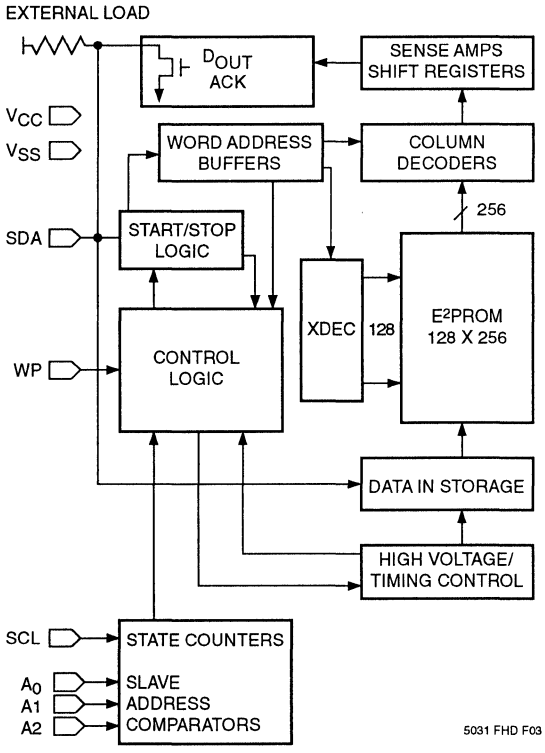
PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
WP	Write Protect
V_{CC}	+5V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



5031 FHD F03

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

TD 5031

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT24C32 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT24C32I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current			3	mA	f_{SCL} = 100 KHz
I_{SB}	Standby Current V_{CC} = 5.5V			4	µA	V_{IN} = GND or V_{CC}
I_{SBZ}(5)	Standby Current V_{CC} = 5.5V			0	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	–1.0		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A0, A1, A2, SCL)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. To more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Standby Current (I_{SBZ}) = 0µA (<900nA) for the CAT24C32Z.

A.C. CHARACTERISTICS

CAT24C32 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT24C32I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max	Units
F_{SCL}	Clock Frequency		100	kHz
T_I(3)	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5	µs
t_{BUF}(3)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		ns
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R(3)	SDA and SCL Rise Time		1	µs
t_F(3)	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Power-Up Timing(3)(6)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Write Cycle Limits

Symbol	Parameter	Min.	Typ.	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Notes:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(6) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT24C32/CAT24C32I supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24C32/CAT24C32I operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

PIN DESCRIPTIONS

SCL: Serial Clock
The serial clock input clocks all data transferred into or out of the device.

SDA: Serial Data/Address
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

A0, A1, A2: Device Address Inputs
These pins define the address of 1 out of 8 slave devices. In the Block Write Protect version, they define the block or blocks of memory to be protected.

WP: Write Protect
If the WP pin is tied to V_{CC}, the entire memory array becomes READ only. If the WP pin is tied to V_{SS} normal read/write operations are allowed to the device. This feature protects the device from inadvertant programming.

Figure 1. Bus Timing

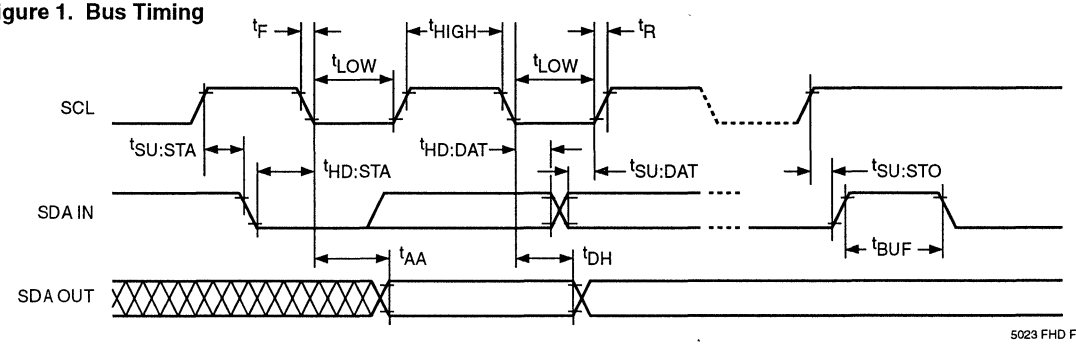


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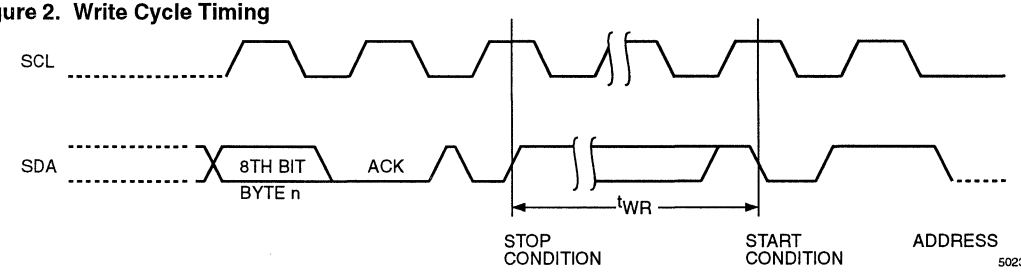
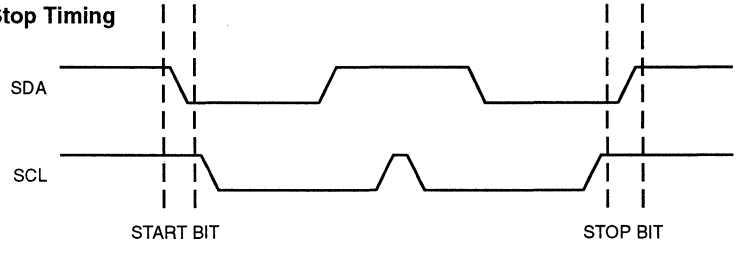
Figure 2. Write Cycle Timing



5023 FHD F05

Figure 3. Start/Stop Timing



5020 FHD F05

I²C BUS PROTOCOL

The following defines the features of the I²C bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24C32/CAT24C32I monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1011 for the CAT24C32/CAT24C32I (see Fig. 5). The next three significant bits (A2, A1, A0) are the device address bits and define which device the Master is accessing. Up to eight CAT24C32/CAT24C32I devices may be individually addressed by the system. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0 a Write operation is selected.

After the Master sends a START condition, the CAT24C32/CAT24C32I monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24C32/CAT24C32I then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

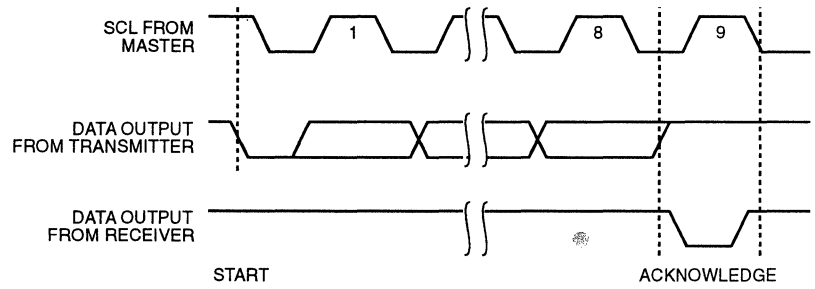
Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the eight bits of data.

The CAT24C32/CAT24C32I responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each eight bit byte.

When the CAT24C32/CAT24C32I begins a READ mode it transmits eight bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24C32/CAT24C32I will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Figure 4. Acknowledge Timing



5020 FHD F06

Figure 5. Slave Address Bits

1	0	1	1	A2	A1	A0	R/$\overline{W}$

5031 FHD F07

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24C32/CAT24C32I. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT24C32/CAT24C32I acknowledges once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24C32/CAT24C32I writes up to 32 bytes of data, in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to 31 additional bytes. After each byte has been transmitted the CAT24C32/CAT24C32I will respond with an acknowledge, and internally increment the five low order address bits by one. The high order bits remain unchanged.

If the Master transmits more than 32 bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all 32 bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24C32/CAT24C32I in a single write cycle.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24C32/CAT24C32I initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24C32/CAT24C32I is still busy with the write operation, no ACK will be returned. If the CAT24C32/CAT24C32I has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Figure 6. Byte Write Timing

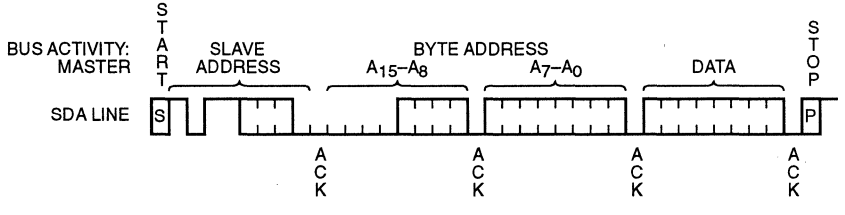
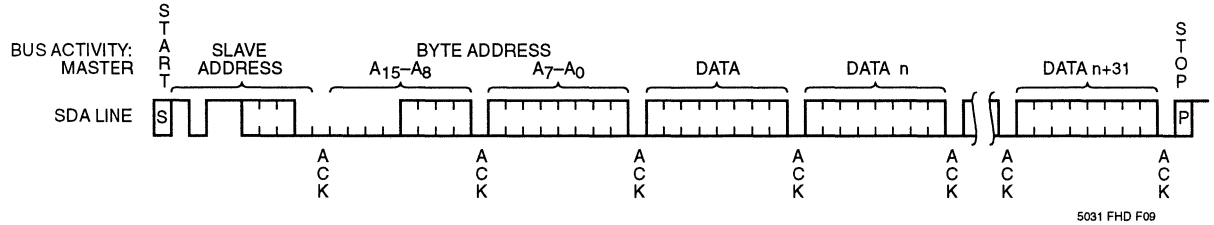


Figure 7. Page Write Timing



READ OPERATIONS

The READ operation for the CAT24C32/CAT24C32I is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

Immediate Address Read

The CAT24C32/CAT24C32I's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=4095, then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24C32/CAT24C32I receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Selective Read

Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24C32/CAT24C32I acknowledges the byte address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24C32/CAT24C32I then responds with its acknowledge and sends the eight bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24C32/CAT24C32I sends the initial eight bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24C32/CAT24C32I will continue to output an eight bit byte for each acknowledge sent by the Master. The operation will terminate when the Master fails to respond with an acknowledge thus sending the STOP condition.

The data being transmitted from the CAT24C32/CAT24C32I is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24C32/CAT24C32I address bits so that the entire memory array can be read during one operation. If more than the 4096 bytes are read out, the counter will 'wrap around' and continue to clock out data bytes.

Figure 8. Immediate Address Read Timing

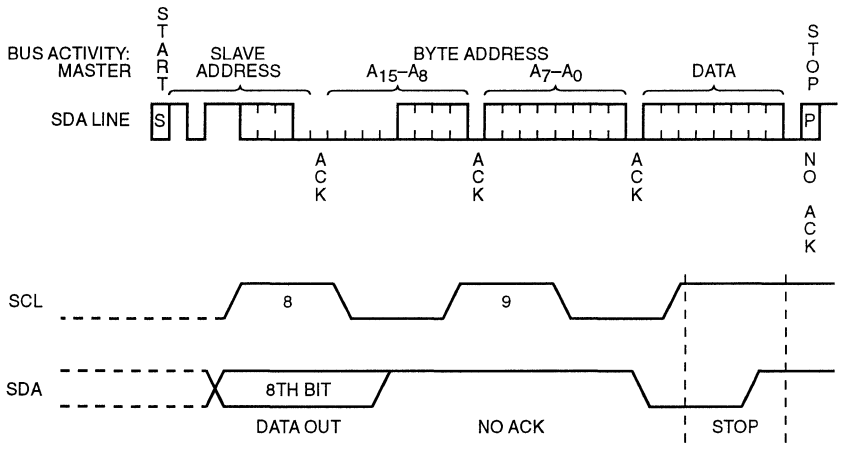


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Figure 9. Selective Read Timing

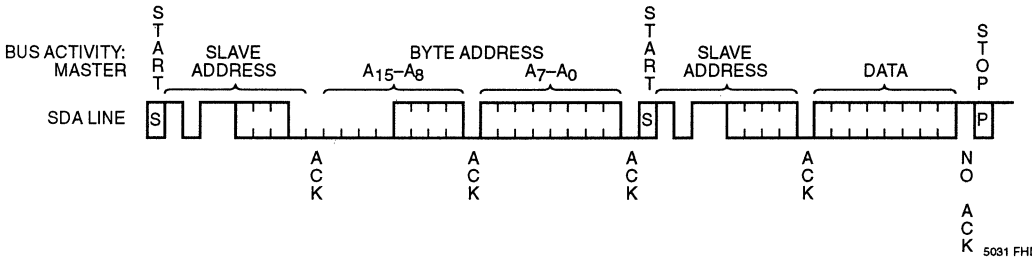
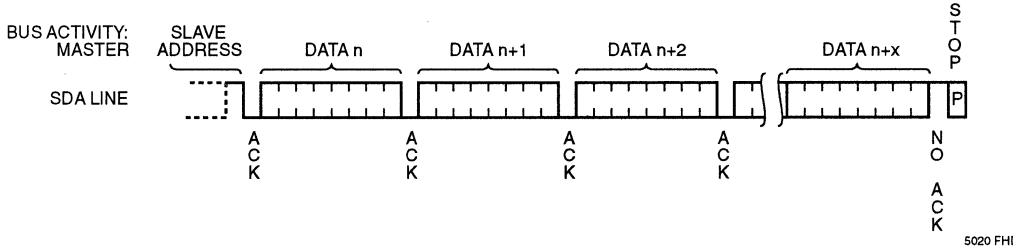


Figure 10. Sequential Read Timing



CATALYST SEMICONDUCTOR

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CAT93C46/CAT93C46I ..... 64 x 16, 128 x 8 ..... 1K-Bit 3-1

CAT93C46A/CAT93C46AI ..... 64 x 16 ..... 1K-Bit 3-9

CAT93C46B/CAT93C46BI ..... 64 x 16, 128 x 8 ..... 1K-Bit 3-17

CAT33C101/CAT33C101I ..... 64 x 16, 128 x 8 ..... 1K-Bit 3-25

CAT32C101 ..... 64 x 16, 128 x 8 ..... 1K-Bit 3-33

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CAT35C102/CAT35C102I ..... 128 x 16, 256 x 8 ..... 2K-Bit 3-57

CAT33C104/CAT33C104I ..... 256 x 16, 512 x 8 ..... 4K-Bit 3-65

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CAT33C116/CAT33C116I ..... 1024 x 16, 2048 x 8 ..... 16K-Bit 3-97

CAT35C116/CAT35C116I ..... 1024 x 16, 2048 x 8 ..... 16K-Bit 3-105

CAT93C46/CAT93C46I

1K-Bit SERIAL E²PROM

FEATURES

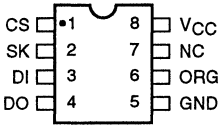
- High Speed Operation: 1MHz
- Low Power CMOS Technology
- Single 5V Supply
- 64 x 16 or 128 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

DESCRIPTION

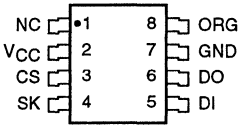
The CAT93C46 and CAT93C46I are 1K bit Serial E²PROM memory devices which can be configured as either 64 registers by 16 bits (ORG pin at V_{CC}) or 128 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C46/CAT93C46I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION

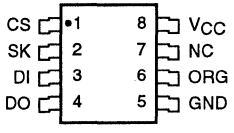
DIP Package



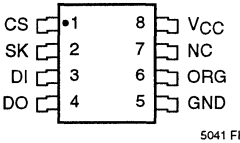
SO Package J



SO Package S



SO Package K



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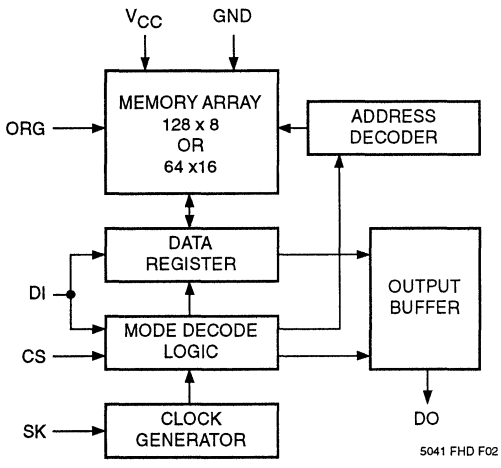
PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+5V Power Supply
GND	Ground
NC	No Connection
ORG	Memory Organization

Note: When the ORG pin is connected to V_{CC}, the 64 x 16 organization is selected. When it is connected to ground, the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64 x 16 organization.

BLOCK DIAGRAM



5041 FHD F02

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT93C46 T_A= 0°C to +70°C, V_{CC} = +5V±10%, unless otherwise specified.
CAT93C46I T_A= –40°C to +85°C, V_{CC} = +5V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	Power Supply Current (Operating)			3	mA	DI = 0.0V, SK = 5.0V V_{CC} = 5.0V, CS = 5.0V, Output Open
I_{CC2}	Power Supply Current (Standby)			100	µA	V_{CC} = 5.5V, CS = 0V DI = 0V SK = 0V
I_{LI}	Input Leakage Current			2	µA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current (Including ORG Pin)			10	µA	V_{OUT} = 0V to 5.5V, CS = 0V
V_{IH}	High Level Input Voltage	2.0		V_{CC} + 1	V	
V_{IL}	Low Level Input Voltage	–0.1		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1mA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1 0	A6–A0	A5–A0			Read Address AN–A0
ERASE	1	1 1	A6–A0	A5–A0			Clear Address AN–A0
WRITE	1	0 1	A6–A0	A5–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	0 0	11XXXXX	11XXXX			Write Enable
EWDS	1	0 0	00XXXXX	00XXXX			Write Disable
ERAL	1	0 0	10XXXXX	10XXXX			Clear All Addresses
WRAL	1	0 0	01XXXXX	01XXXX	D7–D0	D15–D0	Write All Addresses

3

A.C. CHARACTERISTICS

CAT93C46 T_A= 0°C to +70°C, V_{CC} = +5V±10%, unless otherwise specified.
CAT93C46I T_A= –40°C to +85°C, V_{CC} = +5V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	50			ns	
t_{CSH}	CS Hold Time	0			ns	
t_{DIS}	DI Setup Time	100			ns	C_L = 100pF
t_{DIH}	DI Hold Time	100			ns	V_{OL} = 0.8V, V_{OH} = 2.0V
t_{PD1}	Output Delay to 1			500	ns	V_{IL} = 0.45V, V_{IH} = 2.4V
t_{PD0}	Output Delay to 0			500	ns	
t_{HZ}(3)	Output Delay to High-Z			100	ns	
t_{EW}	Program/Erase Pulse Width			10	ms	
t_{CSMIN}	Minimum CS Low Time	250			ns	
t_{SKHI}	Minimum SK High Time	100			ns	
t_{SKLOW}	Minimum SK Low time	660			ns	
t_{SV}	Output Delay to Status Valid			500	ns	C_L = 100pF
SK_{MAX}	Maximum Clock Frequency	DC		1	MHz	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.

DEVICE OPERATION

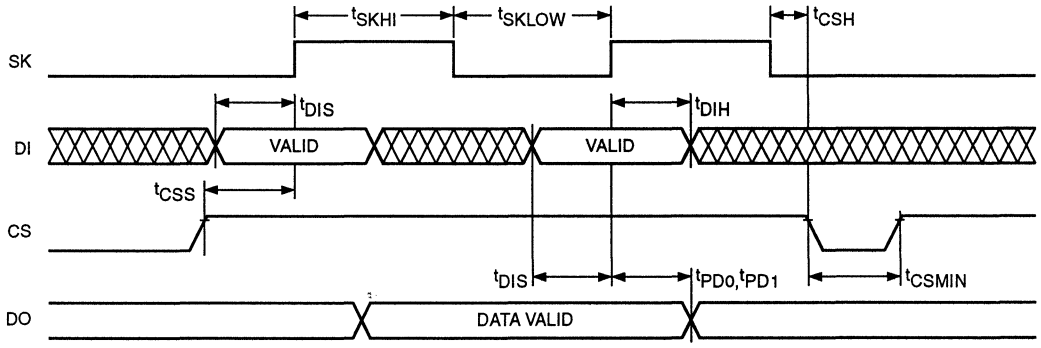
The CAT93C46/CAT93C46I is a 1024 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C46/CAT93C46I can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Seven 9 bit instructions (10 bit instruction in 128 by 8 organization) control the reading, writing and erase operations of the device. The CAT93C46/CAT93C46I operates on a single 5V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

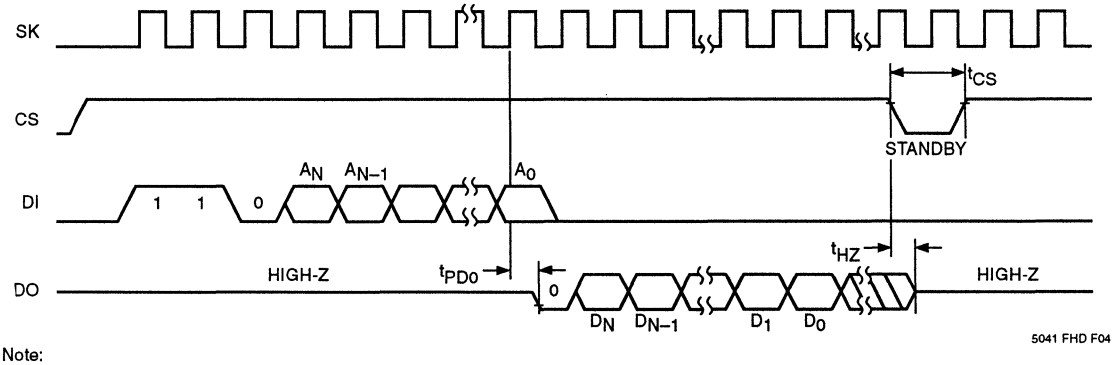
The format for all instructions sent to the CAT93C46/CAT93C46I is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 6 bit address (7 bit address when organized as 128 x 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 x 8).

Figure 1. Sychronous Data Timing (5)



5041 FHD F03

Figure 2. Read Instruction Timing (5)



5041 FHD F04

Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

At power-down, when V_{CC} falls below a threshold of approximately 3.5V, the data protection circuitry inhibits the erase and write instructions and a write disable (EWDS) is executed internally.

NOTE: This device will accept a start bit that is generated when both SK and DI are high with respect to a low to high transition of CS.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C46/CAT93C46I will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Write

After receiving a WRITE command, address and the data, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46/CAT93C46I can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent.

Erase

Upon receiving an ERASE command and address, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46/CAT93C46I

3

Figure 3. Write Instruction Timing (5)

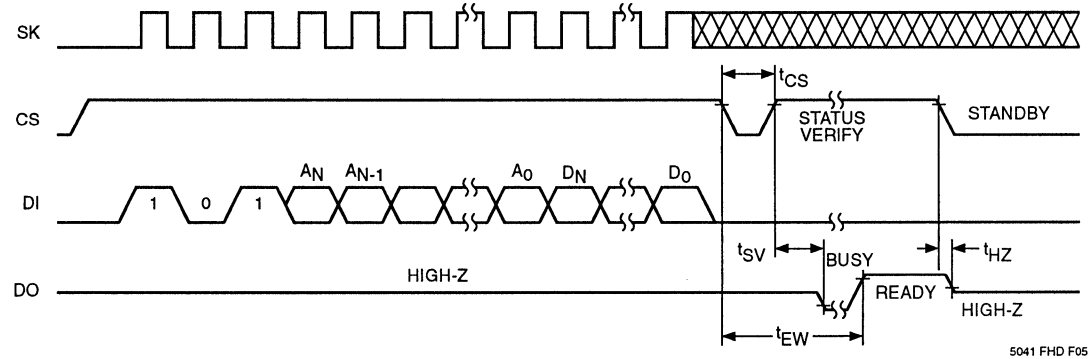
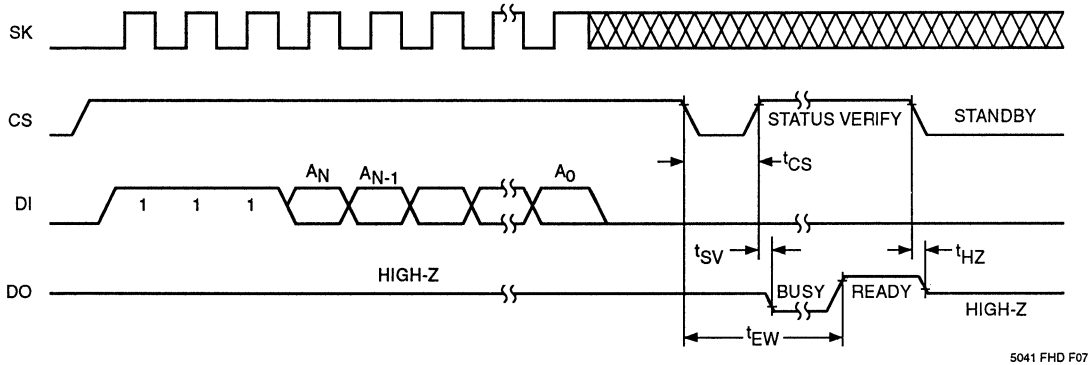


Figure 4. Erase Instruction Timing (5)



Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

Erase/Write Enable and Disable

The CAT93C46/CAT93C46I powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46/CAT93C46I write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}).

The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46/CAT93C46I can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Write All

Upon receiving a WRAL command and data, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46/CAT93C46I can be determined by selecting the device and polling the DO pin. It IS necessary for all memory locations to be cleared before the WRAL command is executed.

Figure 5. EWEN/EWDS Instruction Timing (5)

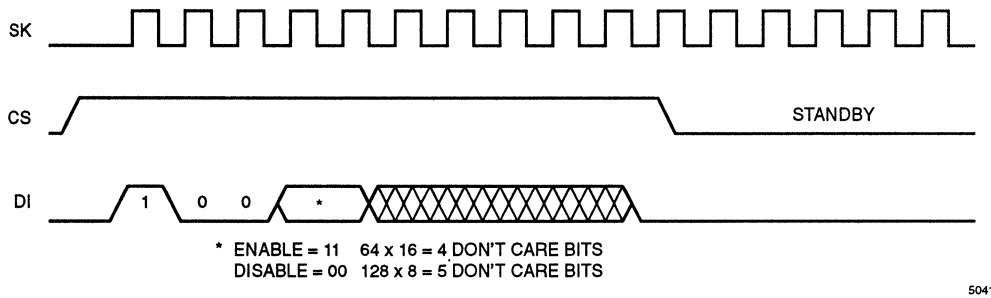
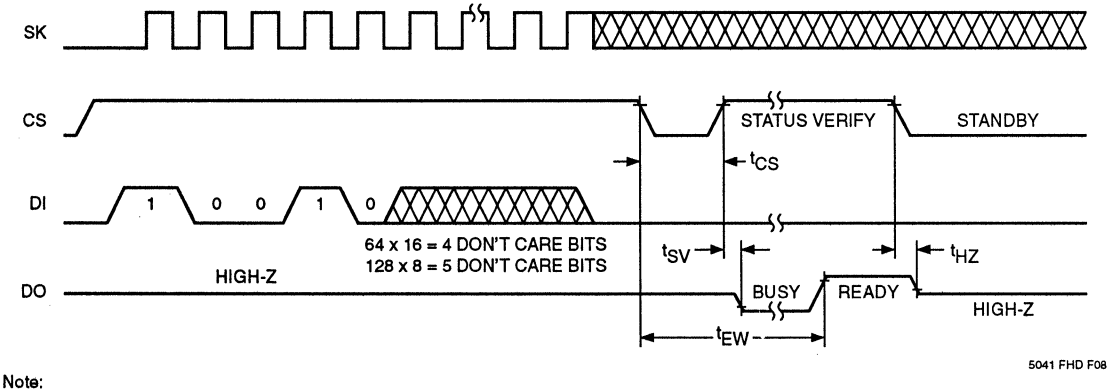


Figure 6. ERAL Instruction Timing (5)



Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

Start Bit Timing

The CAT93C46/CAT93C46I features an alternate start bit timing where the device will accept a start bit that is generated when both SK and DI are high with respect to a low to high transition of CS (see Figure 8). This allows the user to send instructions from microprocessors that transmit and receive data using a sequence of 8 clock cycles only. Once this start bit is generated all subsequent data is clocked into the device on the positive clock edge of SK.

Figure 7. WRAL Instruction Timing (5)

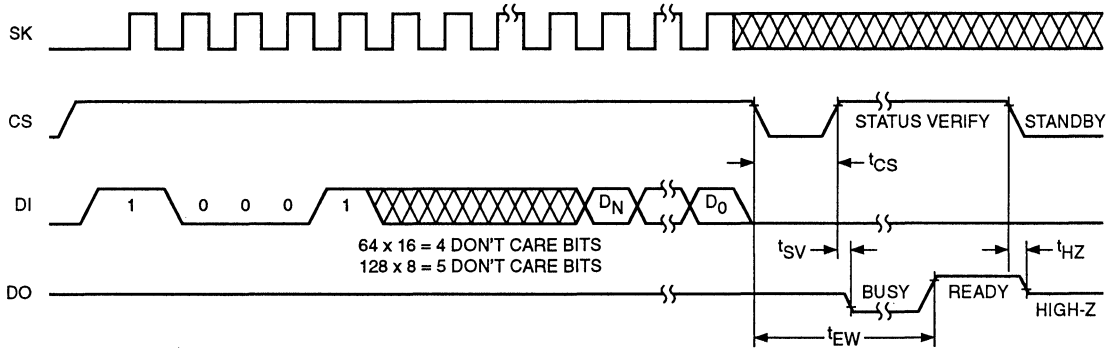
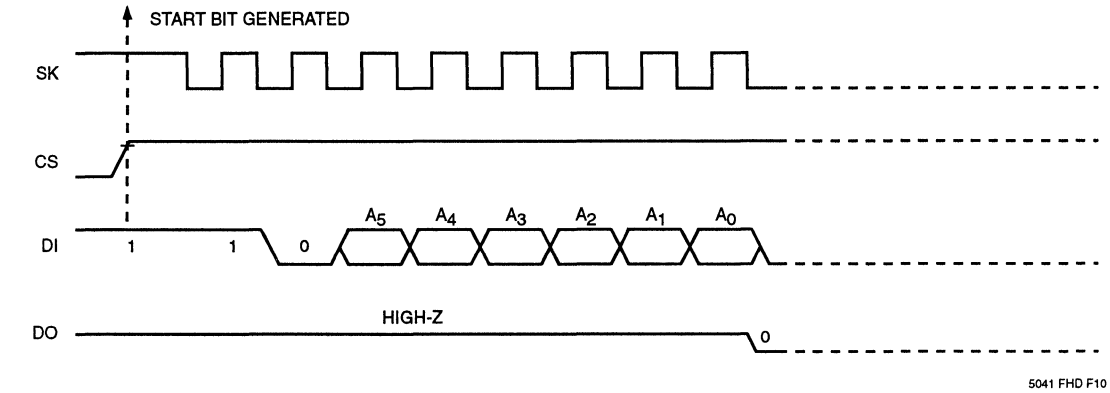


Figure 8. Alternate Start Bit Timing Example: Read Instruction (x 16) (5)



Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

CAT93C46A/CAT93C46AI

1K-Bit SERIAL E²PROM

FEATURES

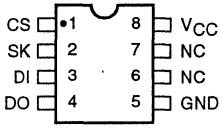
- High Speed Operation: 1MHz
- Low Power CMOS Technology
- Single 5V Supply
- 64 x 16 Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

DESCRIPTION

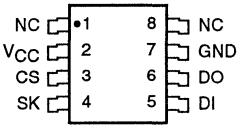
The CAT93C46A and CAT93C46AI are 1K bit Serial E²PROM memory devices which are configured as 64 registers by 16 bits. Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C46A/CAT93C46AI is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION

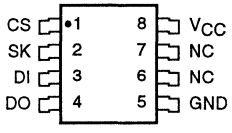
DIP Package



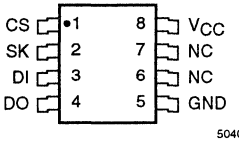
SO Package J



SO Package S



SO Package K



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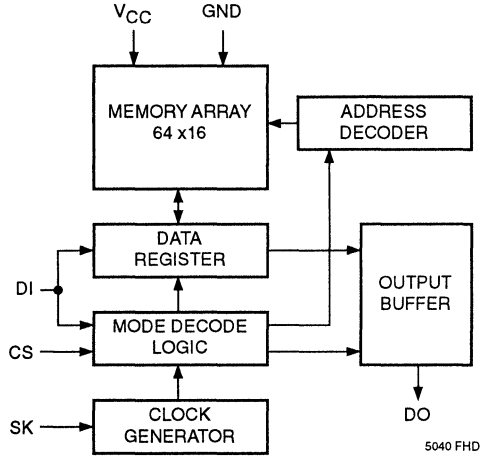
PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+5V Power Supply
GND	Ground
NC	No Connection

BLOCK DIAGRAM



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TD 5040

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT93C46A T_A= 0°C to +70°C, V_{CC} = +5V±10%, unless otherwise specified.
CAT93C46AI T_A= –40°C to +85°C, V_{CC} = +5V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	Power Supply Current (Operating)			3	mA	DI = 0.0V, SK = 5.0V V_{CC} = 5.0V, CS = 5.0V, Output Open
I_{CC2}	Power Supply Current (Standby)			100	µA	V_{CC} = 5.5V, CS = 0V DI = 0V SK = 0V
I_{LI}	Input Leakage Current			2	µA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 0V to 5.5V, CS = 0V
V_{IH}	High Level Input Voltage	2.0		V_{CC} + 1	V	
V_{IL}	Low Level Input Voltage	–0.1		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1mA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address	Data	Comments
READ	1	1 0	A5–A0		Read Address AN–A0
ERASE	1	1 1	A5–A0		Clear Address AN–A0
WRITE	1	0 1	A5–A0	D15–D0	Write Address AN–A0
EWEN	1	0 0	11XXXX		Write Enable
EWDS	1	0 0	00XXXX		Write Disable
ERAL	1	0 0	10XXXX		Clear All Addresses
WRAL	1	0 0	01XXXX	D15–D0	Write All Addresses

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A.C. CHARACTERISTICS

CAT93C46A T_A= 0°C to +70°C, V_{CC} = +5V±10%, unless otherwise specified.
CAT93C46AI T_A= –40°C to +85°C, V_{CC} = +5V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	50			ns	
t_{CSH}	CS Hold Time	0			ns	
t_{DIS}	DI Setup Time	100			ns	C_L = 100pF
t_{DIH}	DI Hold Time	100			ns	V_{OL} = 0.8V, V_{OH} = 2.0V
t_{PD1}	Output Delay to 1			500	ns	V_{IL} = 0.45V, V_{IH} = 2.4V
t_{PD0}	Output Delay to 0			500	ns	
t_{HZ}(3)	Output Delay to High-Z			100	ns	
t_{EW}	Program/Erase Pulse Width			10	ms	
t_{CSMIN}	Minimum CS Low Time	250			ns	
t_{SKHI}	Minimum SK High Time	100			ns	
t_{SKLOW}	Minimum SK Low time	660			ns	
t_{SV}	Output Delay to Status Valid			500	ns	C_L = 100pF
SK_{MAX}	Maximum Clock Frequency	DC		1	MHz	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.

DEVICE OPERATION

The CAT93C46A/CAT93C46AI is a 1024 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C46A/CAT93C46AI is organized as 64 registers by 16 bits. Seven 9 bit instructions control the reading, writing and erase operations of the device. The CAT93C46A/CAT93C46AI operates on a single 5V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the CAT93C46A/CAT93C46AI is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 6 bit address, and for write operations, a 16 bit data field.

Figure 1. Sychronous Data Timing

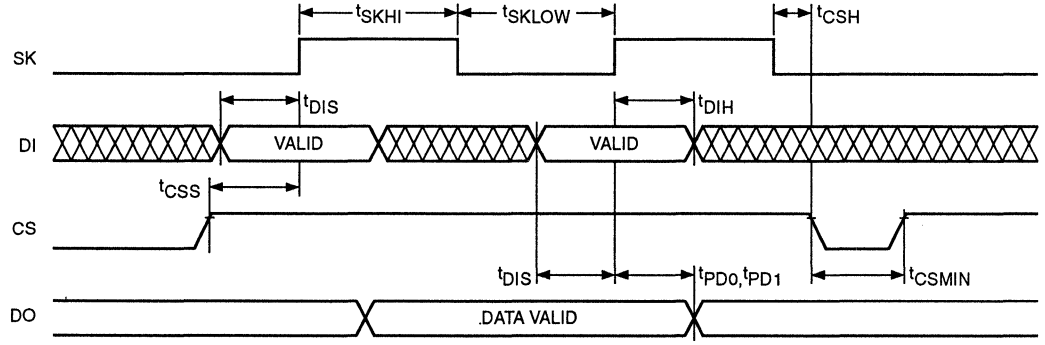

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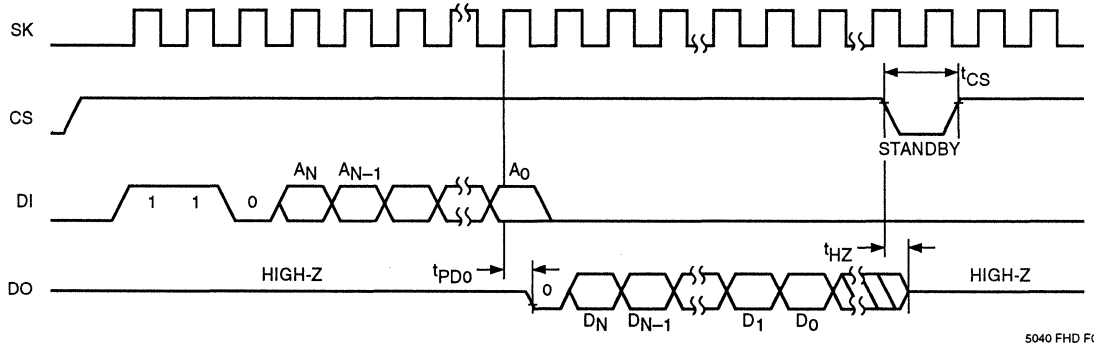
Figure 2. Read Instruction Timing



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At power-down, when V_{CC} falls below a threshold of approximately 3.5V, the data protection circuitry inhibits the erase and write instructions and a write disable (EWDS) is executed internally.

NOTE: This device will accept a start bit that is generated when both SK and DI are high with respect to a low to high transition of CS.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C46A/CAT93C46AI will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Write

After receiving a WRITE command, address and the data, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46A/CAT93C46AI can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent.

Erase

Upon receiving an ERASE command and address, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46A/CAT93C46AI

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Figure 3. Write Instruction Timing

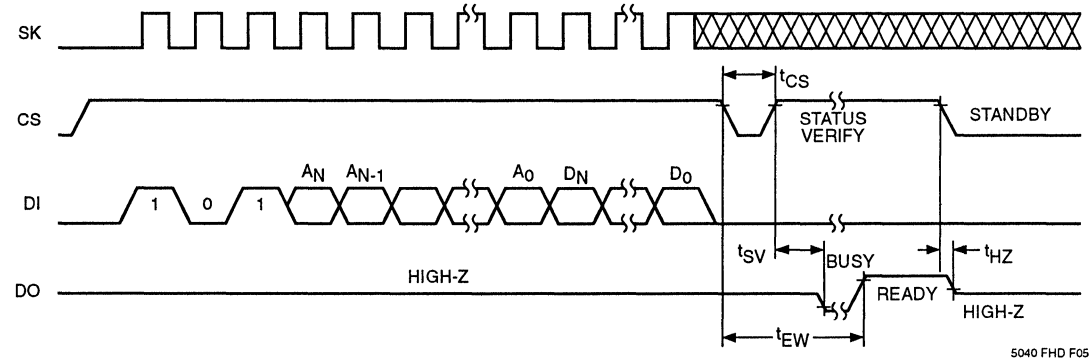
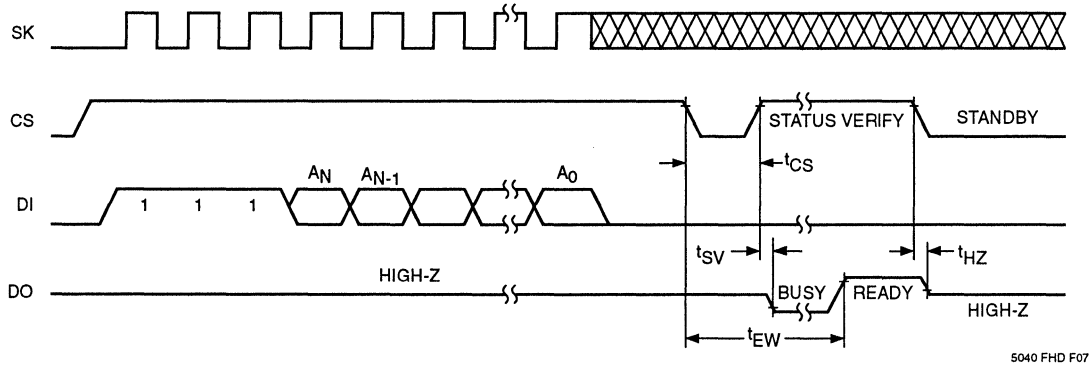


Figure 4. Erase Instruction Timing



can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

Erase/Write Enable and Disable

The CAT93C46A/CAT93C46AI powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46A/CAT93C46AI write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}).

The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46A/CAT93C46AI can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Write All

Upon receiving a WRAL command and data, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46A/CAT93C46AI can be determined by selecting the device and polling the DO pin. It IS necessary for all memory locations to be cleared before the WRAL command is executed.

Figure 5. EWEN/EWDS Instruction Timing

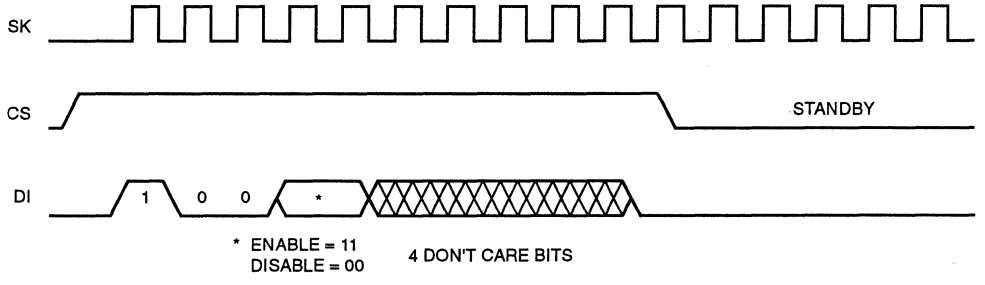


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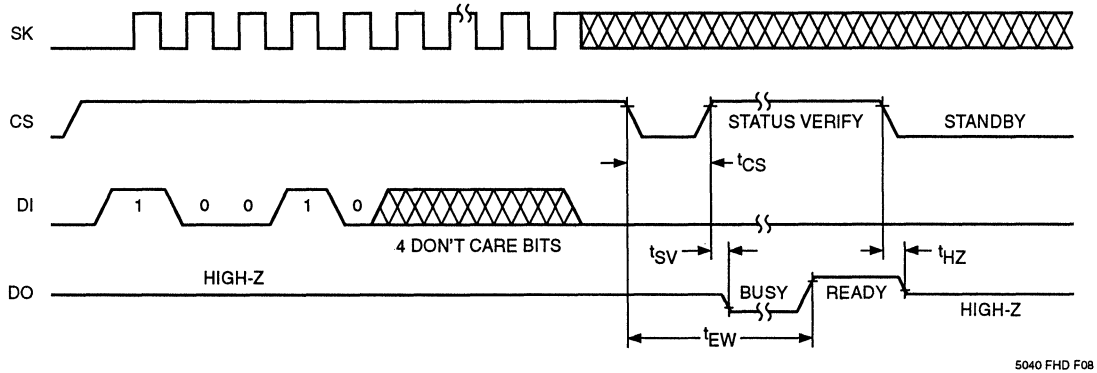
Figure 6. ERAL Instruction Timing



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Start Bit Timing

The CAT93C46A/CAT93C46AI features an alternate start bit timing where the device will accept a start bit that is generated when both SK and DI are high with respect to a low to high transition of CS (see Figure 8). This allows the user to send instructions from microprocessors that transmit and receive data using a sequence of 8 clock cycles only. Once this start bit is generated all subsequent data is clocked into the device on the positive clock edge of SK.

Figure 7. WRAL Instruction Timing

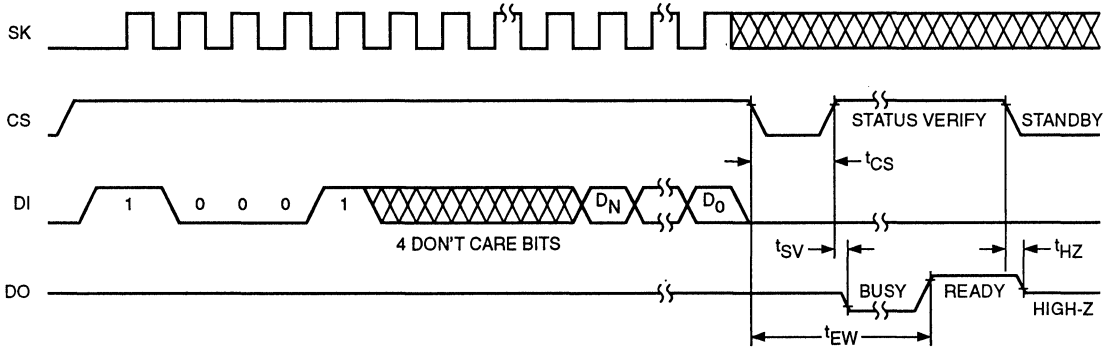

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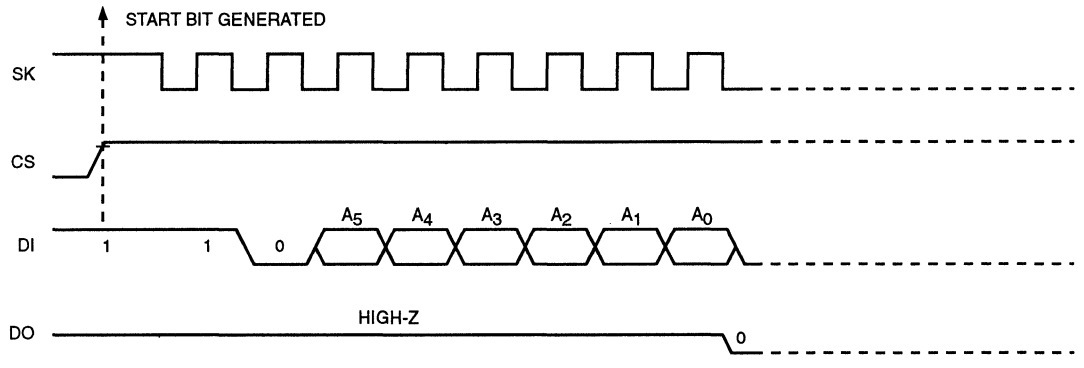
Figure 8. Alternate Start Bit Timing Example: Read Instruction



5040 FHD F10

CAT93C46B/CAT93C46BI

1K-Bit SERIAL E²PROM

FEATURES

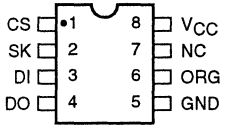
- High Speed Operation: 1MHz
- Low Power CMOS Technology
- Single 5V Supply
- 64 x 16 or 128 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

DESCRIPTION

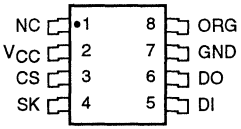
The CAT93C46B and CAT93C46BI are 1K bit Serial E²PROM memory devices which can be configured as either 64 registers by 16 bits (ORG pin at V_{CC}) or 128 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C46B/CAT93C46BI is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION

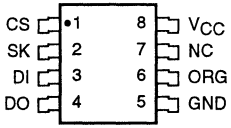
DIP Package



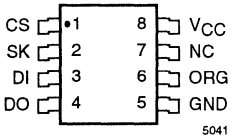
SO Package J



SO Package S



SO Package K



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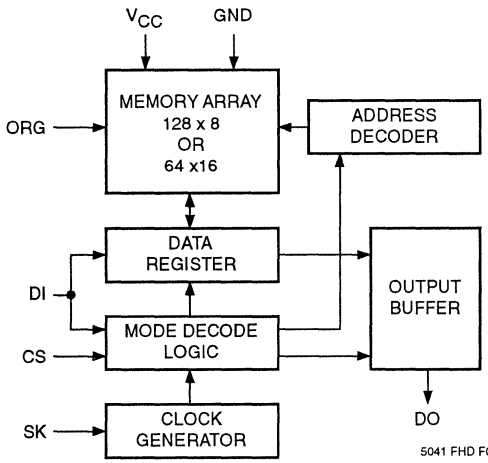
PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+5V Power Supply
GND	Ground
NC	No Connection
ORG	Memory Organization

Note: When the ORG pin is connected to V_{CC}, the 64 x 16 organization is selected. When it is connected to ground, the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64 x 16 organization.

BLOCK DIAGRAM



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TD 5051

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT93C46B T_A= 0°C to +70°C, V_{CC} = +5V±10%, unless otherwise specified.
CAT93C46BI T_A= –40°C to +85°C, V_{CC} = +5V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	Power Supply Current (Operating)			3	mA	DI = 0.0V, SK = 5.0V V_{CC} = 5.0V, CS = 5.0V, Output Open
I_{CC2}	Power Supply Current (Standby)			100	µA	V_{CC} = 5.5V, CS = 0V DI = 0V SK = 0V
I_{LI}	Input Leakage Current			2	µA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current (Including ORG Pin)			10	µA	V_{OUT} = 0V to 5.5V, CS = 0V
V_{IH}	High Level Input Voltage	2.0		V_{CC} + 1	V	
V_{IL}	Low Level Input Voltage	–0.1		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1mA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1 0	A6–A0	A5–A0			Read Address AN–A0
ERASE	1	1 1	A6–A0	A5–A0			Clear Address AN–A0
WRITE	1	0 1	A6–A0	A5–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	0 0	11XXXXX	11XXXX			Write Enable
EWDS	1	0 0	00XXXXX	00XXXX			Write Disable
ERAL	1	0 0	10XXXXX	10XXXX			Clear All Addresses
WRAL	1	0 0	01XXXXX	01XXXX	D7–D0	D15–D0	Write All Addresses

3

A.C. CHARACTERISTICS

CAT93C46B T_A= 0°C to +70°C, V_{CC} = +5V±10%, unless otherwise specified.
CAT93C46BI T_A= –40°C to +85°C, V_{CC} = +5V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	50			ns	
t_{CSH}	CS Hold Time	0			ns	
t_{DIS}	DI Setup Time	100			ns	C_L = 100pF
t_{DIH}	DI Hold Time	100			ns	V_{OL} = 0.8V, V_{OH} = 2.0V
t_{PD1}	Output Delay to 1			500	ns	V_{IL} = 0.45V, V_{IH} = 2.4V
t_{PD0}	Output Delay to 0			500	ns	
t_{HZ}(3)	Output Delay to High-Z			100	ns	
t_{EW}	Program/Erase Pulse Width			10	ms	
t_{CSMIN}	Minimum CS Low Time	250			ns	
t_{SKHI}	Minimum SK High Time	100			ns	
t_{SKLOW}	Minimum SK Low time	660			ns	
t_{SV}	Output Delay to Status Valid			500	ns	C_L = 100pF
SK_{MAX}	Maximum Clock Frequency	DC		1	MHz	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.

DEVICE OPERATION

The CAT93C46B/CAT93C46BI is a 1024 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C46B/CAT93C46BI can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Seven 9 bit instructions (10 bit instruction in 128 by 8 organization) control the reading, writing and erase operations of the device. The CAT93C46B/CAT93C46BI operates on a single 5V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the CAT93C46B/CAT93C46BI is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 6 bit address (7 bit address when organized as 128 x 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 x 8).

Figure 1. Sychronous Data Timing (5)

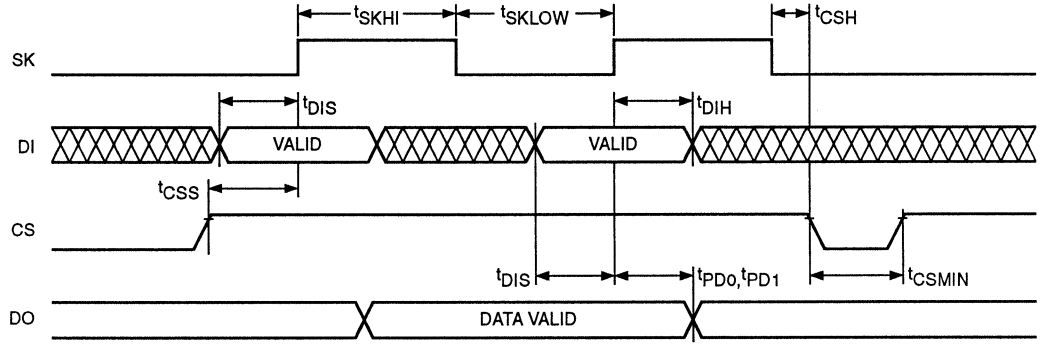

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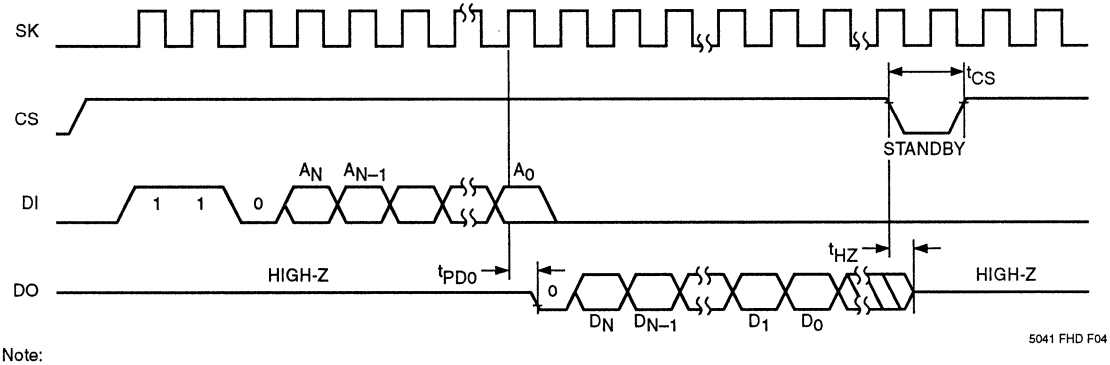
Figure 2. Read Instruction Timing (5)



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Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

At power-down, when V_{CC} falls below a threshold of approximately 3.5V, the data protection circuitry inhibits the erase and write instructions and a write disable (EWDS) is executed internally.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C46B/CAT93C46BI will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Write

After receiving a WRITE command, address and the data, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46B/CAT93C46BI can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent.

Erase

Upon receiving an ERASE command and address, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of the memory location specified in the instruction. The clocking of the SK pin is not neces-

3

Figure 3. Write Instruction Timing (5)

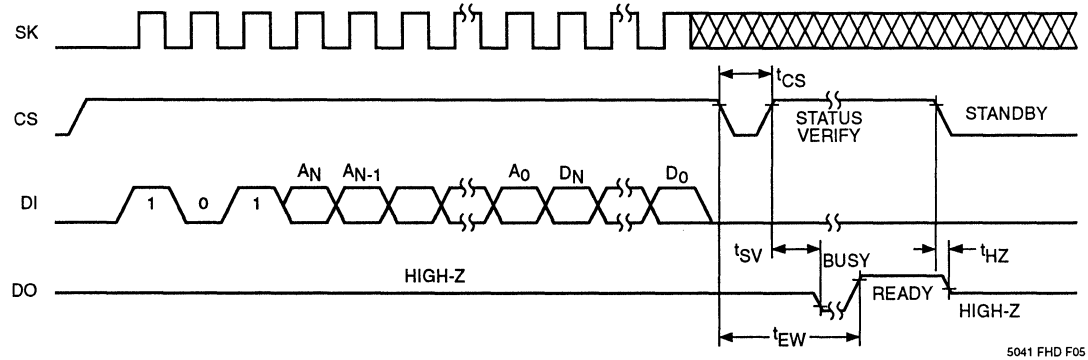
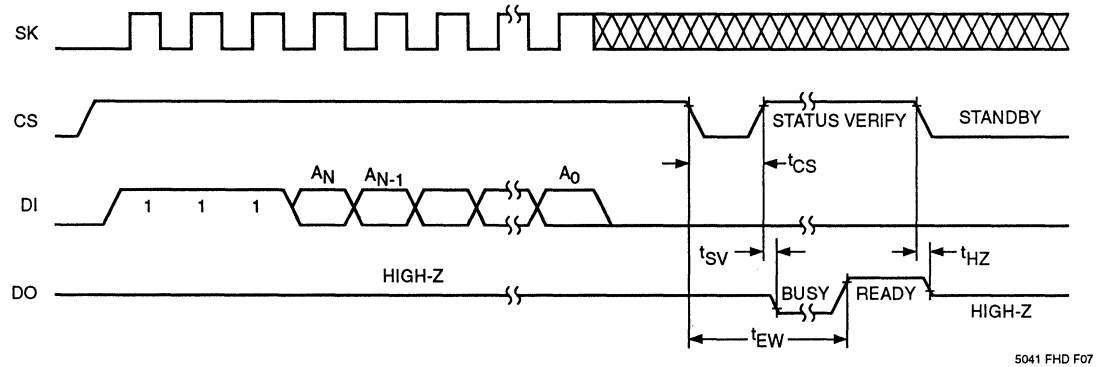


Figure 4. Erase Instruction Timing (5)



Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

sary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46B/CAT93C46BI can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

Erase/Write Enable and Disable

The CAT93C46B/CAT93C46BI powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46B/CAT93C46BI write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46B/CAT93C46BI can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Figure 5. EWEN/EWDS Instruction Timing (5)

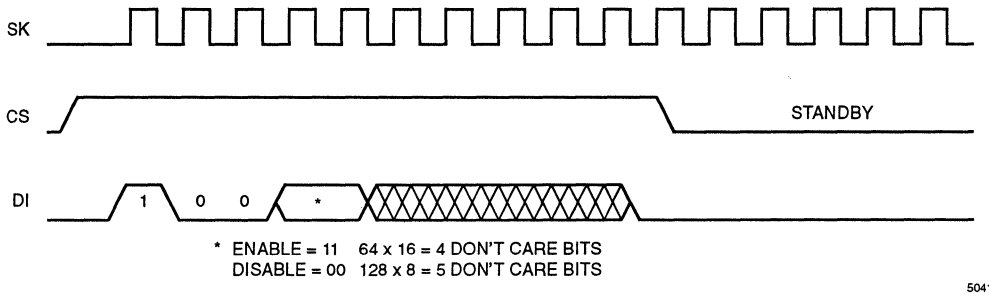
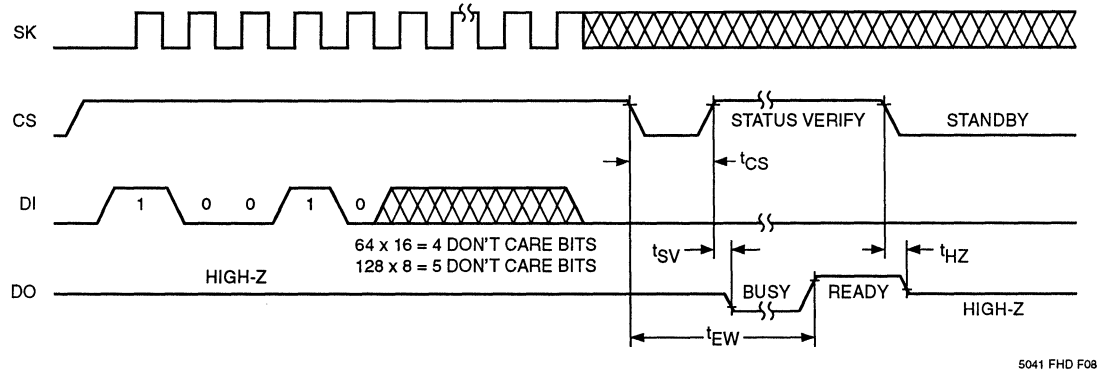


Figure 6. ERAL Instruction Timing (5)

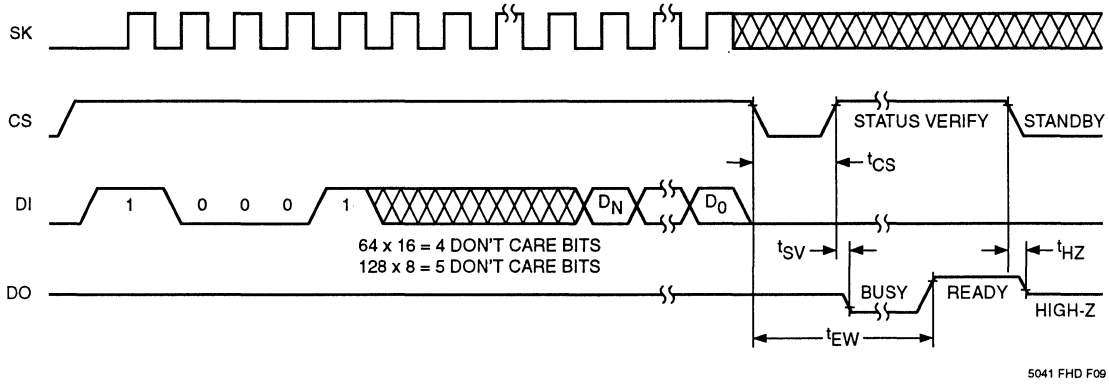


Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

Write All

Upon receiving a WRAL command and data, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46B/CAT93C46BI can be determined by selecting the device and polling the DO pin. It IS necessary for all memory locations to be cleared before the WRAL command is executed.

Figure 7. WRAL Instruction Timing (5)



Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

CAT33C101/CAT33C101I

1K-Bit SERIAL E²PROM

FEATURES

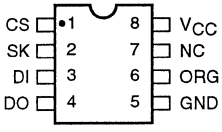
- Low Power CMOS Technology
- Single 3V Supply
- 64 x 16 or 128 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

DESCRIPTION

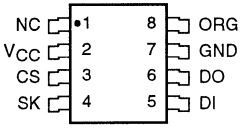
The CAT33C101 and CAT33C101I are 1K bit Serial E²PROM memory devices which can be configured as either 64 registers by 16 bits (ORG pin at V_{CC}) or 128 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT33C101/CAT33C101I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION

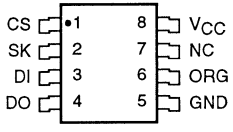
DIP Package



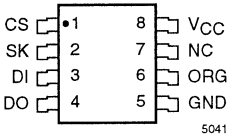
SO Package J



SO Package S



SO Package K



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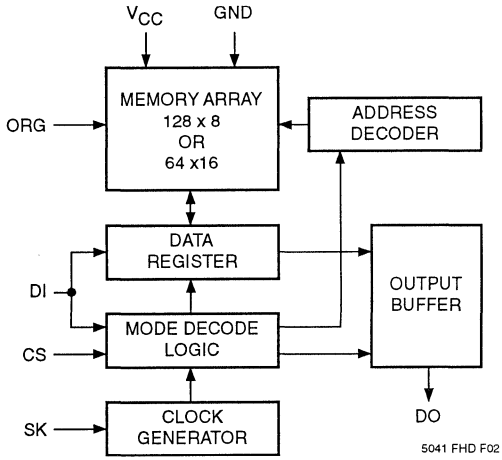
PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+3V Power Supply
GND	Ground
NC	No Connection
ORG	Memory Organization

Note: When the ORG pin is connected to V_{CC}, the 64 x 16 organization is selected. When it is connected to ground, the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64 x 16 organization.

BLOCK DIAGRAM



5041 FHD F02

TD 5041

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground[1] .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current[2] .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}[3]	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}[3]	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}[3]	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}[3][4]	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT33C101 T_A= 0°C to +70°C, V_{CC} = +3V±10%, unless otherwise specified.
CAT33C101I T_A= –40°C to +85°C, V_{CC} = +3V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	Power Supply Current (Operating)			2	mA	DI = 0.0V, SK = 3.3V V_{CC} = 3.3V, CS = 3.3V, Output Open
I_{CC2}	Power Supply Current (Standby)			50	µA	V_{CC} = 3.3V, CS = 0V DI = 0V SK = 0V
I_{LI}	Input Leakage Current			2	µA	V_{IN} = 0V to 3.3V
I_{LO}	Output Leakage Current (Including ORG Pin)			10	µA	V_{OUT} = 0V to 3.3V, CS = 0V
V_{IH}	High Level Input Voltage	V_{CC} – 0.3		V_{CC} + 1	V	
V_{IL}	Low Level Input Voltage	–0.1		0.3	V	
V_{OH}	High Level Output Voltage	V_{CC} – 0.3			V	I_{OH} = –10µs
V_{OL}	Low Level Output Voltage			0.3	V	I_{OL} = 10µs

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1 0	A6–A0	A5–A0			Read Address AN–A0
ERASE	1	1 1	A6–A0	A5–A0			Clear Address AN–A0
WRITE	1	0 1	A6–A0	A5–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	0 0	11XXXXX	11XXXX			Write Enable
EWDS	1	0 0	00XXXXX	00XXXX			Write Disable
ERAL	1	0 0	10XXXXX	10XXXX			Clear All Addresses
WRAL	1	0 0	01XXXXX	01XXXX	D7–D0	D15–D0	Write All Addresses

3

A.C. CHARACTERISTICS

CAT33C101 T_A= 0°C to +70°C, V_{CC} = +3V±10%, unless otherwise specified.
CAT33C101I T_A= –40°C to +85°C, V_{CC} = +3V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	200			ns	
t_{CSH}	CS Hold Time	0			ns	
t_{DIS}	DI Setup Time	400			ns	C_L = 100pF
t_{DIH}	DI Hold Time	400			ns	V_{OL} = 0.8V, V_{OH} = 2.0V
t_{PD1}	Output Delay to 1			2	µs	V_{IL} = 0.45V, V_{IH} = 2.4V
t_{PD0}	Output Delay to 0			2	µs	
t_{HZ}(3)	Output Delay to High-Z			400	ns	
t_{EW}	Program/Erase Pulse Width			20	ms	
t_{CSMIN}	Minimum CS Low Time	1			µs	
t_{SKHI}	Minimum SK High Time	1			µs	
t_{SKLOW}	Minimum SK Low time	1			µs	
t_{SV}	Output Delay to Status Valid			1	µs	C_L = 100pF
SK_{MAX}	Maximum Clock Frequency	DC		250	kHz	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.

DEVICE OPERATION

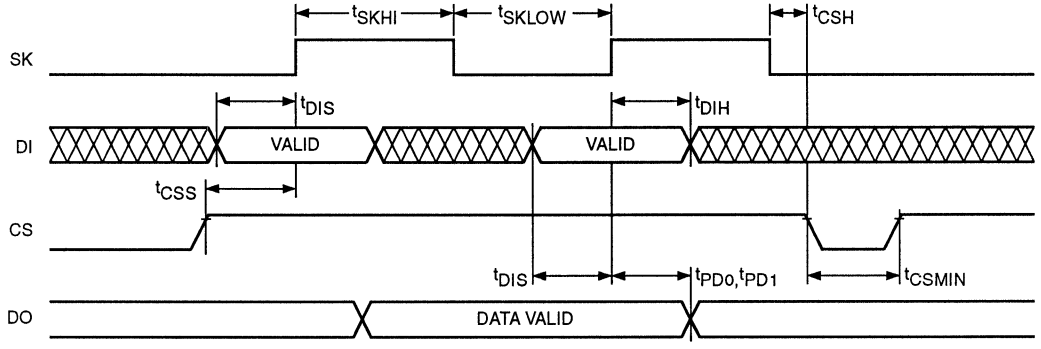
The CAT33C101/CAT33C101I is a 1024 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT33C101/CAT33C101I can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Seven 9 bit instructions (10 bit instruction in 128 by 8 organization) control the reading, writing and erase operations of the device. The CAT33C101/CAT33C101I operates on a single 3V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

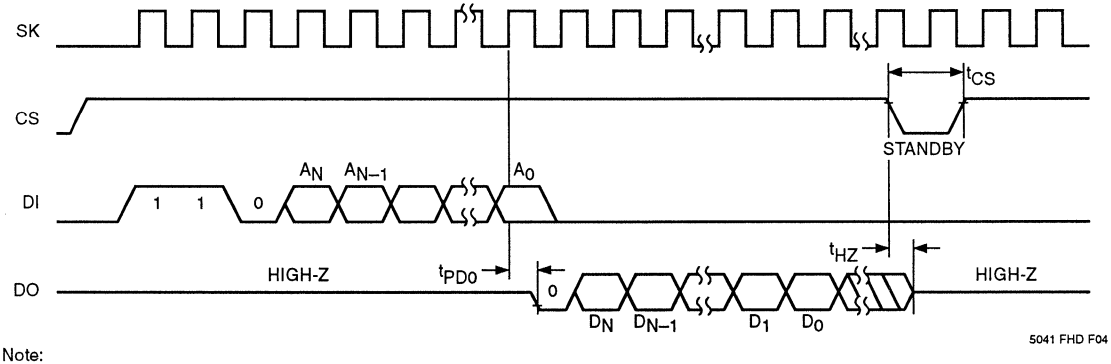
The format for all instructions sent to the CAT33C101/CAT33C101I is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 6 bit address (7 bit address when organized as 128 x 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 x 8).

Figure 1. Sychronous Data Timing (5)



5041 FHD F03

Figure 2. Read Instruction Timing (5)



5041 FHD F04

Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

At power-down, when V_{CC} falls below a threshold of approximately 2.4V, the data protection circuitry inhibits the erase and write instructions and a write disable (EWDS) is executed internally.

NOTE: This device will accept a start bit that is generated when both SK and DI are high with respect to a low to high transition of CS.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT33C101/CAT33C101I will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Write

After receiving a WRITE command, address and the data, the CS (chip select) pin must be deselected for a minimum of 1µs (t_{CSMIN}). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C101/CAT33C101I can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent.

Erase

Upon receiving an ERASE command and address, the CS (chip select) pin must be deselected for a minimum of 1µs (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C101/CAT33C101I

Figure 3. Write Instruction Timing (5)

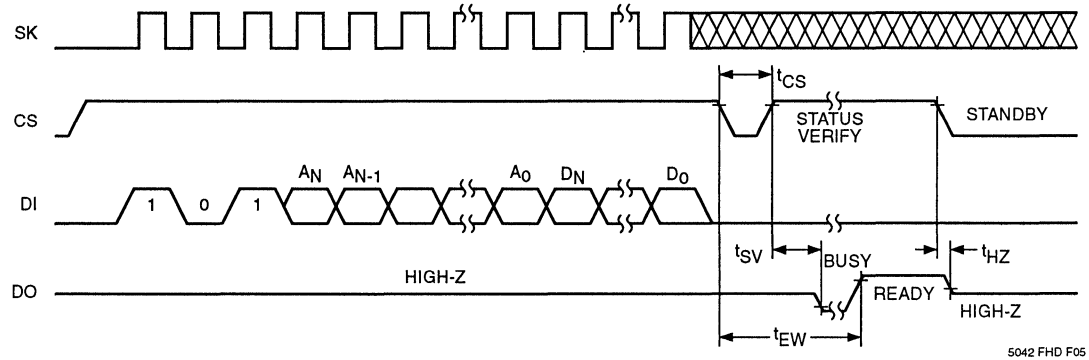
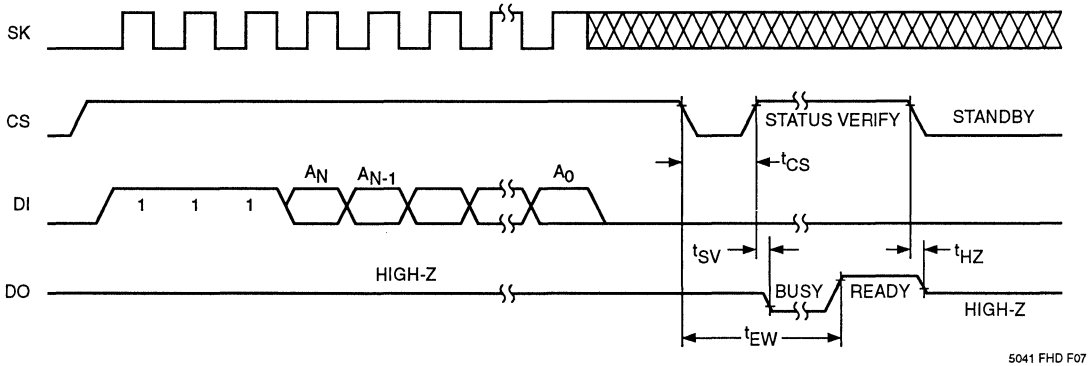


Figure 4. Erase Instruction Timing (5)



Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

Erase/Write Enable and Disable

The CAT33C101/CAT33C101I powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT33C101/CAT33C101I write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (chip select) pin must be deselected for a minimum of 1µs (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C101/CAT33C101I can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Write All

Upon receiving a WRAL command and data, the CS (chip select) pin must be deselected for a minimum of 1µs (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C101/CAT33C101I can be determined by selecting the device and polling the DO pin. It IS necessary for all memory locations to be cleared before the WRAL command is executed.

Figure 5. EWEN/EWDS Instruction Timing (5)

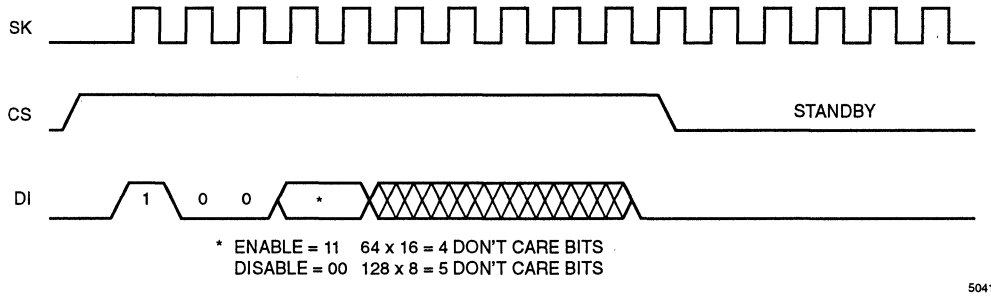
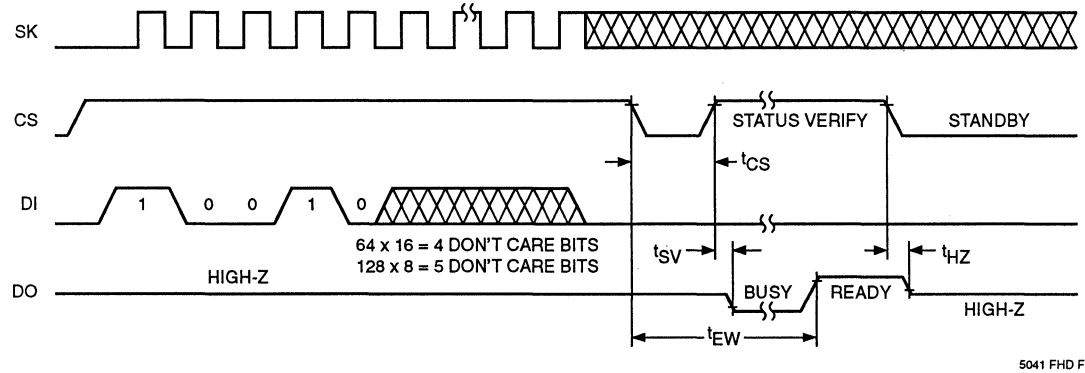


Figure 6. ERAL Instruction Timing (5)

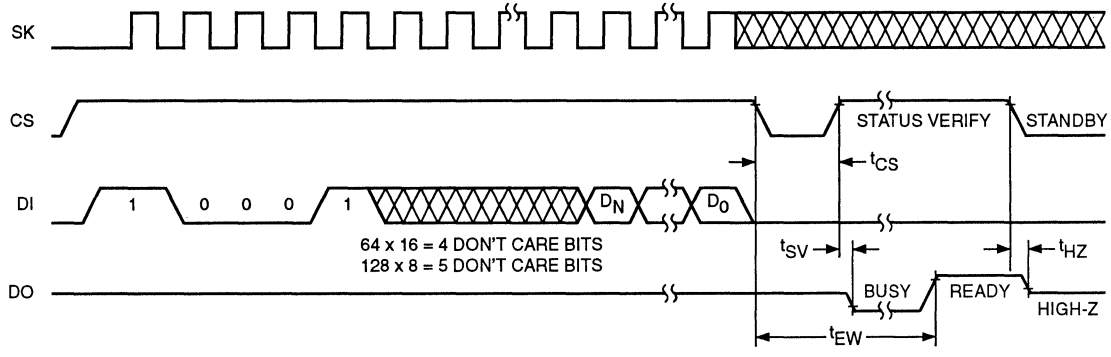


Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

Start Bit Timing

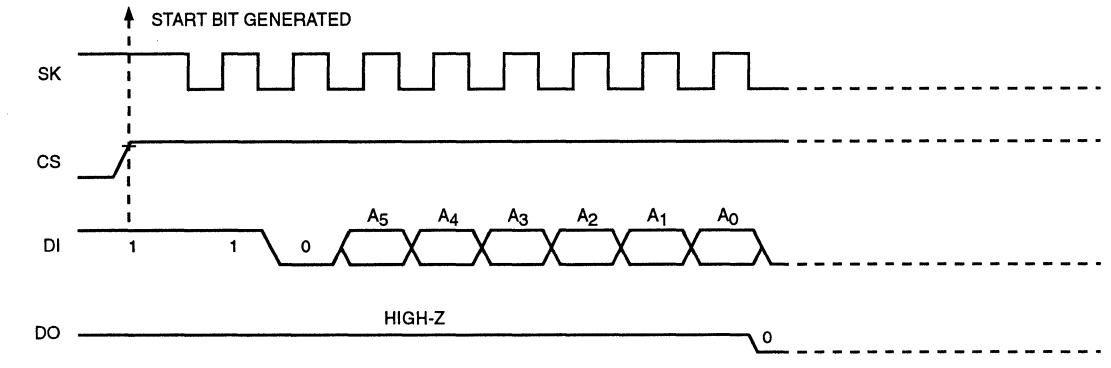
The CAT33C101/CAT33C101I features an alternate start bit timing where the device will accept a start bit that is generated when both SK and DI are high with respect to a low to high transition of CS (see Figure 8). This allows the user to send instructions from microprocessors that transmit and receive data using a sequence of 8 clock cycles only. Once this start bit is generated all subsequent data is clocked into the device on the positive clock edge of SK.

Figure 7. WRAL Instruction Timing (5)



5041 FHD F09

Figure 8. Alternate Start Bit Timing Example: Read Instruction (x 16) (5)



5041 FHD F10

Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

CAT32C101

1K-Bit SERIAL E²PROM

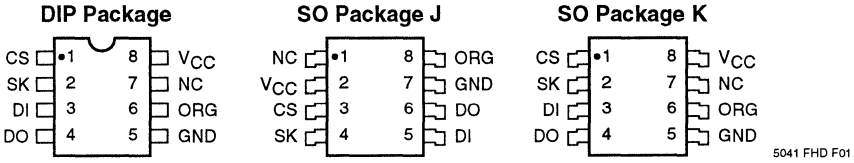
FEATURES

- Low Power CMOS Technology
- 2.2 to 3.5V Operation
- 64 x 16 or 128 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- 1.9V Read Operation
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

DESCRIPTION

The CAT32C101 is a 1K bit Serial E²PROM memory device which can be configured as either 64 registers by 16 bits (ORG pin at V_{CC}) or 128 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT32C101 is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION

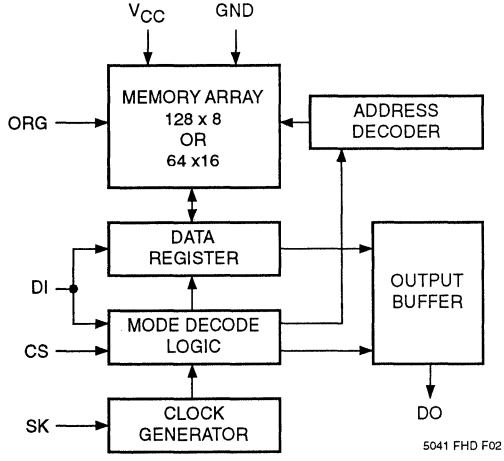


PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+2.2V to +3.5V Power Supply
GND	Ground
NC	No Connection
ORG	Memory Organization

Note: When the ORG pin is connected to V_{CC}, the 64 x 16 organization is selected. When it is connected to ground, the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64 x 16 organization.

BLOCK DIAGRAM



TD 5043

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT32C101 T_A= 0°C to +70°C, V_{CC} = +2.2V to +3.5V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	Power Supply Current (Operating)			2	mA	DI = 0.0V, SK = 3.5V V_{CC} = 3.5V, CS = 3.5V, Output Open
I_{CC2}	Power Supply Current (Standby)			2	µA	V_{CC} = 3.5V, CS = 0V DI = 0V SK = 0V ORG = 3.5V
I_{LI}	Input Leakage Current			2	µA	V_{IN} = 0V to 3.5V
I_{LO}	Output Leakage Current (Including ORG Pin)			10	µA	V_{OUT} = 0V to 3.5V, CS = 0V
V_{IH}	High Level Input Voltage	V_{CC} – 0.3		V_{CC} + 1	V	
V_{IL}	Low Level Input Voltage	–0.1		0.3	V	
V_{OH}	High Level Output Voltage	V_{CC} – 0.3			V	I_{OH} = –10µA
V_{OL}	Low Level Output Voltage			0.3	V	I_{OL} = 10µA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1 0	A6–A0	A5–A0			Read Address AN–A0
ERASE	1	1 1	A6–A0	A5–A0			Clear Address AN–A0
WRITE	1	0 1	A6–A0	A5–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	0 0	11XXXXX	11XXXX			Write Enable
EWDS	1	0 0	00XXXXX	00XXXX			Write Disable
ERAL	1	0 0	10XXXXX	10XXXX			Clear All Addresses
WRAL	1	0 0	01XXXXX	01XXXX	D7–D0	D15–D0	Write All Addresses

3

A.C. CHARACTERISTICS

CAT32C101 T_A= 0°C to +70°C, V_{CC} = +2.2V to +3.5V , unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	200			ns	
t_{CSH}	CS Hold Time	0			ns	C_L = 100pF
t_{DIS}	DI Setup Time	400			ns	V_{OL} = 0.3V
t_{DIH}	DI Hold Time	400			ns	$V_{OH} = V_{CC} - 0.3$
t_{PD1}	Output Delay to 1			2	µs	V_{IL} = 0.3V
t_{PD0}	Output Delay to 0			2	µs	$V_{IH} = V_{CC} - 0.3$
t_{HZ}(3)	Output Delay to High-Z			400	ns	
t_{EW}	Program/Erase Pulse Width			20	ms	
t_{CSMIN}	Minimum CS Low Time	1			µs	
t_{SKHI}	Minimum SK High Time	1			µs	
t_{SKLOW}	Minimum SK Low time	1			µs	
t_{SV}	Output Delay to Status Valid			1	µs	C_L = 100pF
SK_{MAX}	Maximum Clock Frequency	DC		250	kHz	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.

DEVICE OPERATION

The CAT32C101 is a 1024 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT32C101 can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Seven 9 bit instructions (10 bit instruction in 128 by 8 organization) control the reading, writing and erase operations of the device. The CAT32C101 operates on a single 2.2–3.5V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the CAT32C101 is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 6 bit address (7 bit address when organized as 128 x 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 x 8).

Figure 1. Sychronous Data Timing (5)

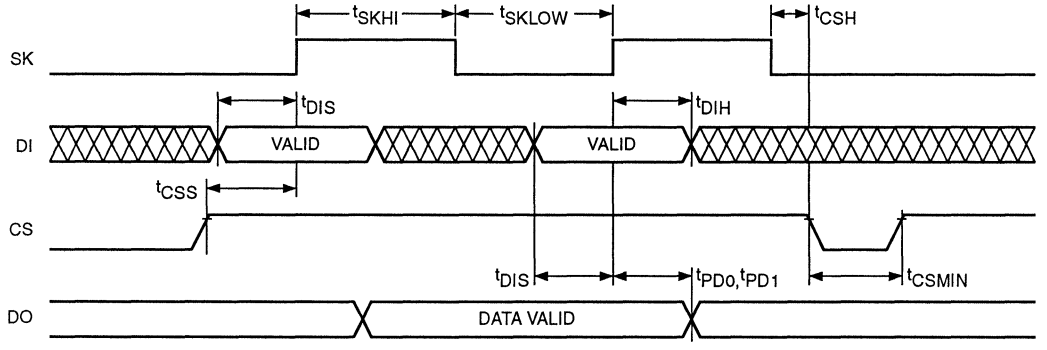


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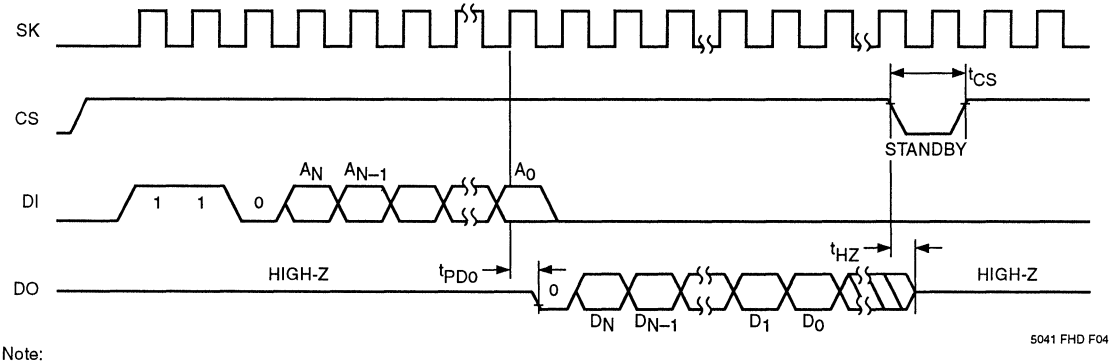
Figure 2. Read Instruction Timing (5)



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Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

At power-down, when V_{CC} falls below a threshold of approximately 1.7V, the data protection circuitry inhibits the erase and write instructions and a write disable (EWDS) is executed internally.

NOTE: This device will accept a start bit that is generated when both SK and DI are high with respect to a low to high transition of CS.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT32C101 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Write

After receiving a WRITE command, address and the data, the CS (chip select) pin must be deselected for a minimum of 1µs (t_{CSMIN}). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT32C101 can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent.

Erase

Upon receiving an ERASE command and address, the CS (chip select) pin must be deselected for a minimum of 1µs (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT32C101 can be determined by selecting the device and polling the DO pin.

3

Figure 3. Write Instruction Timing (5)

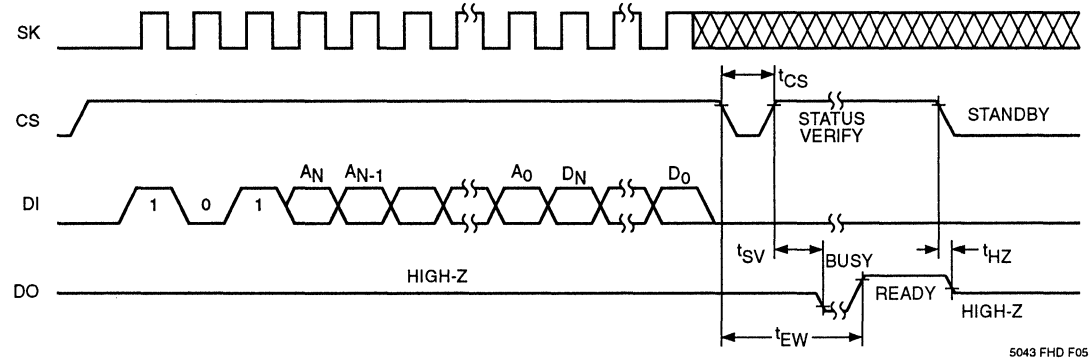
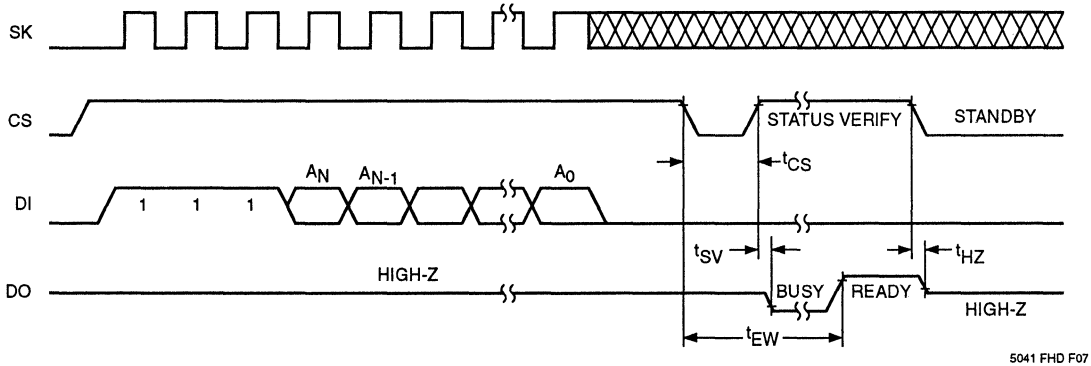


Figure 4. Erase Instruction Timing (5)



Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

Once cleared, the content of a cleared location returns to a logical "1" state.

Erase/Write Enable and Disable

The CAT32C101 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT32C101 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (chip select) pin must be deselected for a minimum of 1μs (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT32C101 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Write All

Upon receiving a WRAL command and data, the CS (chip select) pin must be deselected for a minimum of 1μs (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT32C101 can be determined by selecting the device and polling the DO pin. It IS necessary for all memory locations to be cleared before the WRAL command is executed.

Figure 5. EWEN/EWDS Instruction Timing (5)

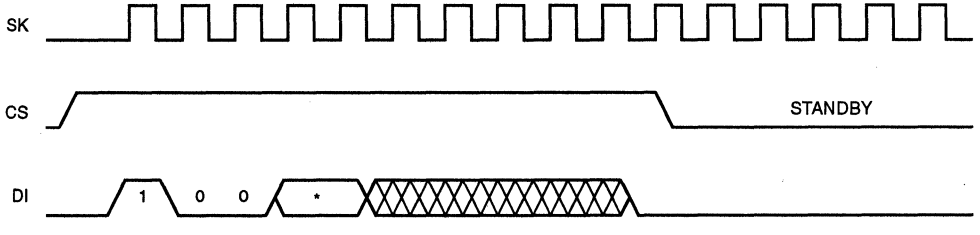
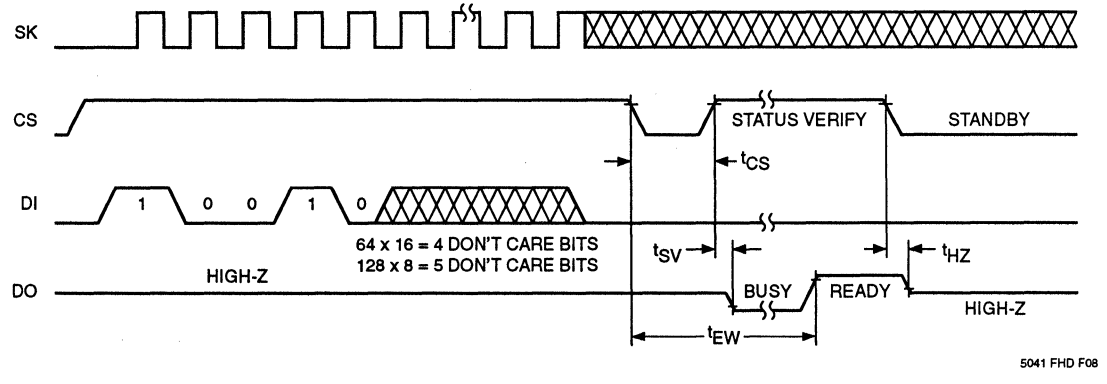


Figure 6. ERAL Instruction Timing (5)



Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

Start Bit Timing

The CAT32C101 features an alternate start bit timing where the device will accept a start bit that is generated when both SK and DI are high with respect to a low to high transition of CS (see Figure 8). This allows the user to send instructions from microprocessors that transmit and receive data using a sequence of 8 clock cycles only. Once this start bit is generated all subsequent data is clocked into the device on the positive clock edge of SK.

Figure 7. WRAL Instruction Timing (5)

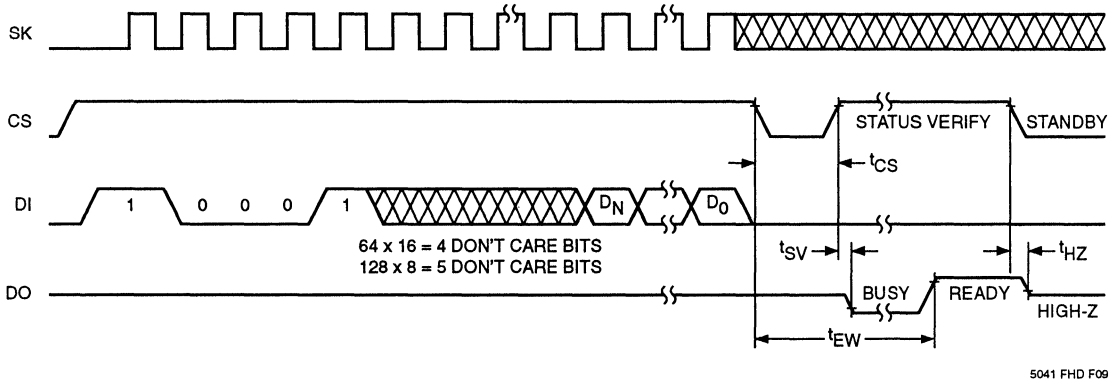


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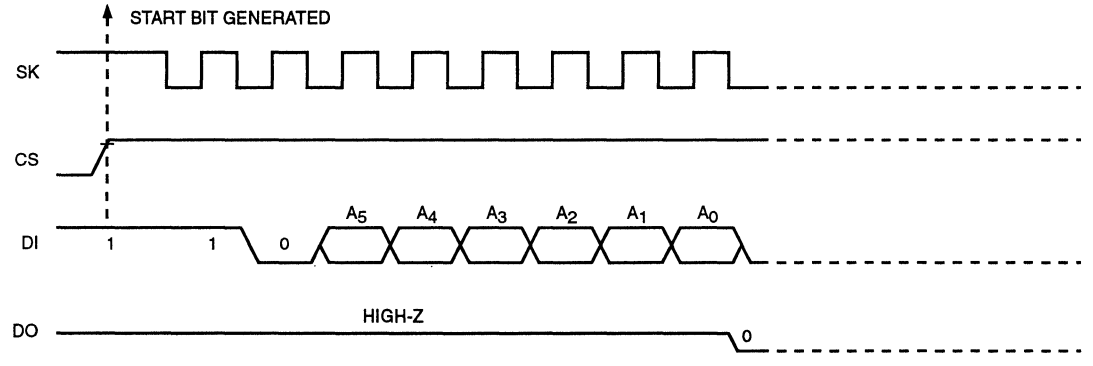
Figure 8. Alternate Start Bit Timing Example: Read Instruction (x 16) (5)



5041 FHD F10

Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

CAT93C56/CAT93C56I

2K-Bit SERIAL E²PROM

FEATURES

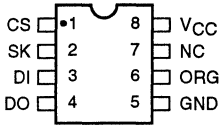
- High Speed Operation: 1MHz
- Low Power CMOS Technology
- Single 5V Supply
- 128 x 16 or 256 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

DESCRIPTION

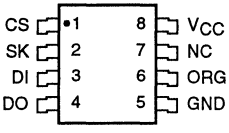
The CAT93C56 and CAT93C56I are 2K bit Serial E²PROM memory devices which can be configured as either 128 registers by 16 bits (ORG pin at V_{CC}) or 256 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C56/CAT93C56I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION

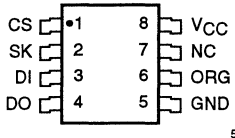
DIP Package



SO Package S



SO Package K



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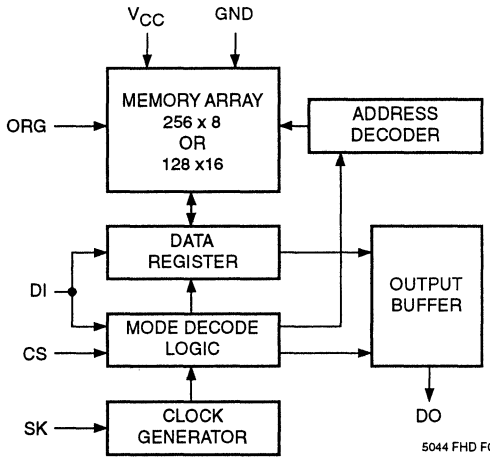
PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+5V Power Supply
GND	Ground
NC	No Connection
ORG	Memory Organization

Note: When the ORG pin is connected to V_{CC}, the 128 x 16 organization is selected. When it is connected to ground, the 256 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 128 x 16 organization.

BLOCK DIAGRAM



5044 FHD F02

TD 5044

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT93C56 T_A= 0°C to +70°C, V_{CC} = +5V±10%, unless otherwise specified.
CAT93C56I T_A= –40°C to +85°C, V_{CC} = +5V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	Power Supply Current (Operating)			3	mA	DI = 0.0V, SK = 5.0V V_{CC} = 5.0V, CS = 5.0V, Output Open
I_{CC2}	Power Supply Current (Standby)			100	µA	V_{CC} = 5.5V, CS = 0V DI = 0V SK = 0V
I_{LI}	Input Leakage Current			2	µA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current (Including ORG Pin)			10	µA	V_{OUT} = 0V to 5.5V, CS = 0V
V_{IH}	High Level Input Voltage	2.0		V_{CC} + 1	V	
V_{IL}	Low Level Input Voltage	–0.1		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1mA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			256 x 8	128 x 16	256 x 8	128 x 16	
READ(5)	1	1 0	A8–A0	A7–A0			Read Address AN–A0
ERASE(5)	1	1 1	A8–A0	A7–A0			Clear Address AN–A0
WRITE(5)	1	0 1	A8–A0	A7–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	0 0	11XXXXXXX	11XXXXXX			Write Enable
EWDS	1	0 0	00XXXXXXX	00XXXXXX			Write Disable
ERAL	1	0 0	10XXXXXXX	10XXXXXX			Clear All Addresses
WRAL	1	0 0	01XXXXXXX	01XXXXXX	D7–D0	D15–D0	Write All Addresses

3

A.C. CHARACTERISTICS

CAT93C56 T_A= 0°C to +70°C, V_{CC} = +5V±10%, unless otherwise specified.
CAT93C56I T_A= –40°C to +85°C, V_{CC} = +5V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	50			ns	
t_{CSH}	CS Hold Time	0			ns	
t_{DIS}	DI Setup Time	100			ns	C_L = 100pF
t_{DIH}	DI Hold Time	100			ns	V_{OL} = 0.8V, V_{OH} = 2.0V
t_{PD1}	Output Delay to 1			500	ns	V_{IL} = 0.45V, V_{IH} = 2.4V
t_{PD0}	Output Delay to 0			500	ns	
t_{HZ}(3)	Output Delay to High-Z			100	ns	
t_{EW}	Program/Erase Pulse Width			10	ms	
t_{CSMIN}	Minimum CS Low Time	250			ns	
t_{SKHI}	Minimum SK High Time	100			ns	
t_{SKLOW}	Minimum SK Low time	660			ns	
t_{SV}	Output Delay to Status Valid			500	ns	C_L = 100pF
SK_{MAX}	Maximum Clock Frequency	DC		1	MHz	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(5) Address bit A8 for 256 x 8 ORG and A7 for 128 x 16 ORG are "Don't Care" bits, but must be kept at either a "1" or "0" for READ, WRITE and ERASE commands.

DEVICE OPERATION

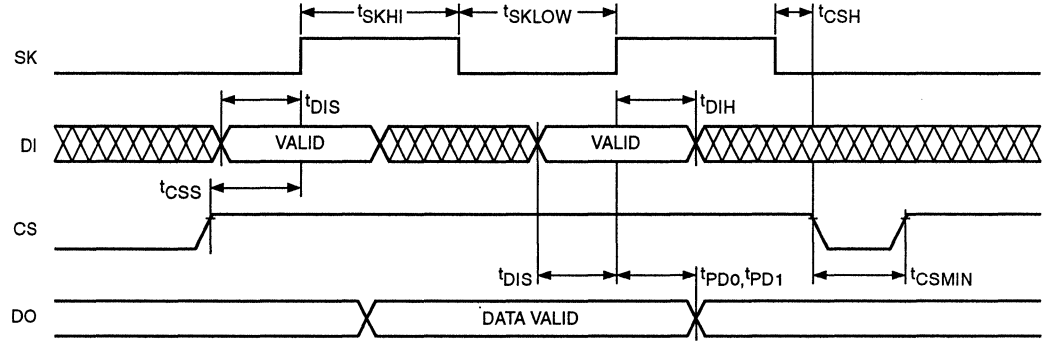
The CAT93C56/CAT93C56I is a 2048 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C56/CAT93C56I can be organized as either 128 registers by 16 bits, or as 256 registers by 8 bits. Seven 11 bit instructions (12 bit instruction in 256 by 8 organization) control the reading, writing and erase operations of the device. The CAT93C56/CAT93C56I operates on a single 5V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

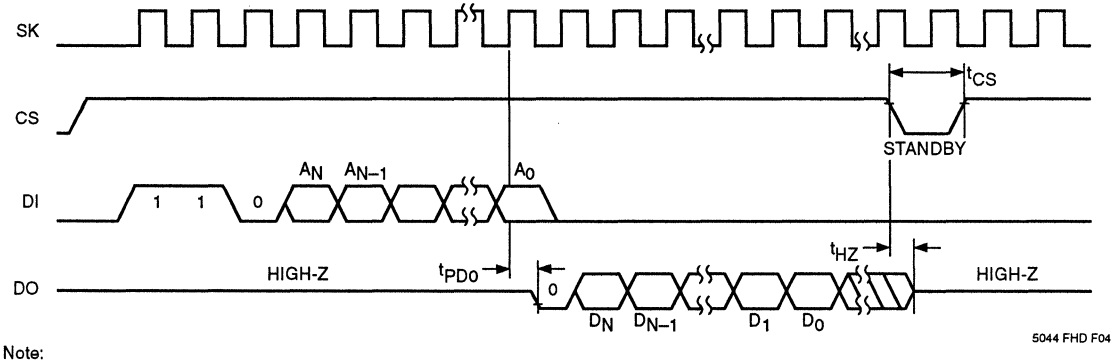
The format for all instructions sent to the CAT93C56/CAT93C56I is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 8 bit address (9 bit address when organized as 256 x 8), and for write operations a 16 bit data field (8 bit data field when organized as 256 x 8).

Figure 1. Sychronous Data Timing (6)



5044 FHD F03

Figure 2. Read Instruction Timing (6)



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Note:

(6) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A8 and DN = D7. When x16 organization is selected, AN = A7 and DN = D15.

At power-down, when V_{CC} falls below a threshold of approximately 3.5V, the data protection circuitry inhibits the erase and write instructions and a write disable (EWDS) is executed internally.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C56/CAT93C56I will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}). The most significant bit of the address is a "Don't Care" bit, but it must be kept at either a "1" or a "0" for READ, WRITE and ERASE commands.

Write

After receiving a WRITE command, address and the data, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C56/CAT93C56I can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent. The most significant bit of the address is a "Don't Care" bit, but it must be kept at either a "1" or a "0" for READ, WRITE and ERASE commands.

Erase

Upon receiving an ERASE command and address, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of the memory location specified in the instruction. The clocking of the SK pin is not neces-

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Figure 3. Write Instruction Timing (6)

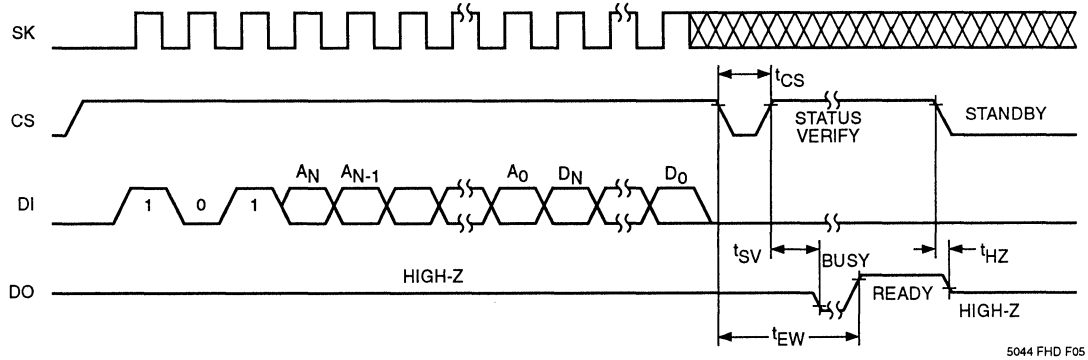
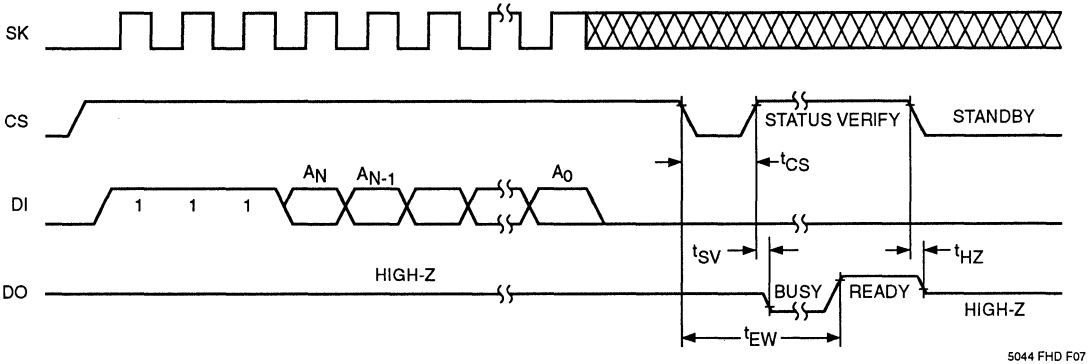


Figure 4. Erase Instruction Timing (6)



Note:
(6) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A8 and DN = D7. When x16 organization is selected, AN = A7 and DN = D15.

sary after the device has entered the self clocking mode. The ready/busy status of the CAT93C56/CAT93C56I can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state. The most significant bit of the address is a "Don't Care" bit, but it must be kept at either a "1" or a "0" for READ, WRITE and ERASE commands.

Erase/Write Enable and Disable

The CAT93C56/CAT93C56I powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C56/CAT93C56I write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C56/CAT93C56I can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Figure 5. EWEN/EWDS Instruction Timing (6)

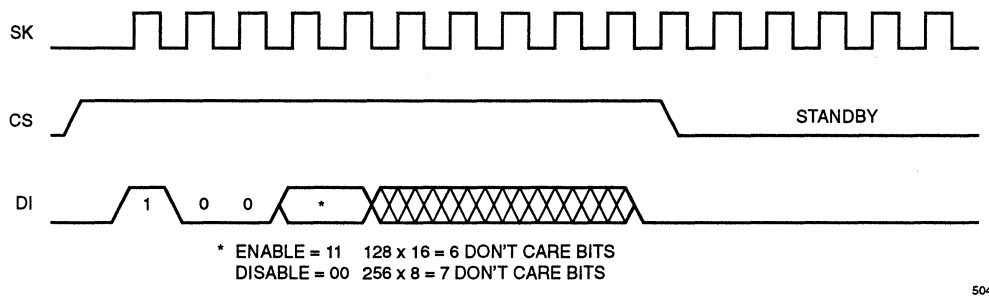
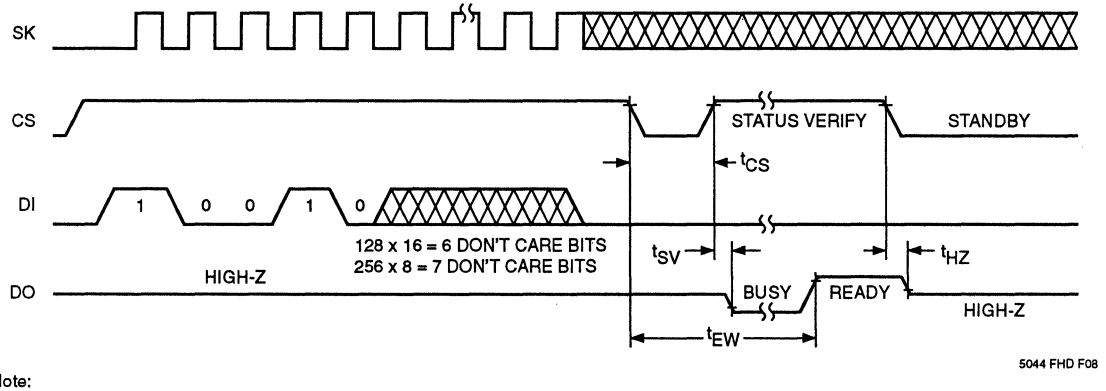


Figure 6. ERAL Instruction Timing (6)

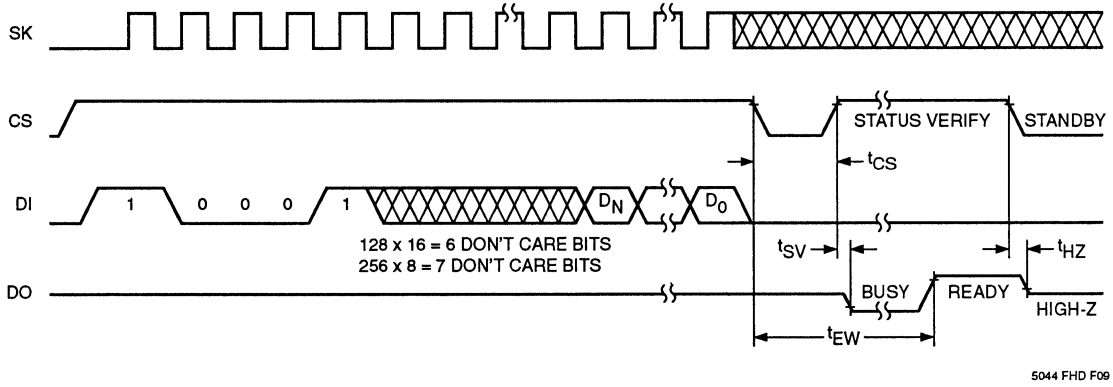


Note:
(6) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A8 and DN = D7. When x16 organization is selected, AN = A7 and DN = D15.

Write All

Upon receiving a WRAL command and data, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C56/CAT93C56I can be determined by selecting the device and polling the DO pin. It IS NOT necessary for all memory locations to be cleared before the WRAL command is executed.

Figure 7. WRAL Instruction Timing (6)



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Note:
(6) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A8 and DN = D7. When x16 organization is selected, AN = A7 and DN = D15.

CAT93LC56/CAT93LC56I

2K-Bit SERIAL E²PROM

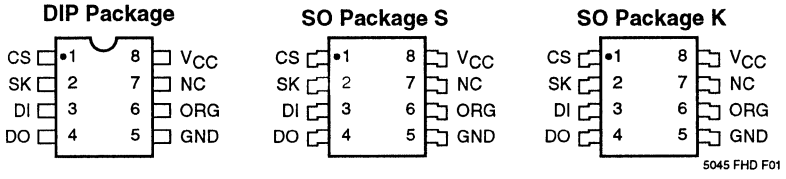
FEATURES

- Low Power CMOS Technology
- Single 3V Supply
- 128 x 16 or 256 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

DESCRIPTION

The CAT93LC56 and CAT93LC56I are 2K bit Serial E²PROM memory devices which can be configured as either 128 registers by 16 bits (ORG pin at V_{CC}) or 256 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93LC56/CAT93LC56I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION

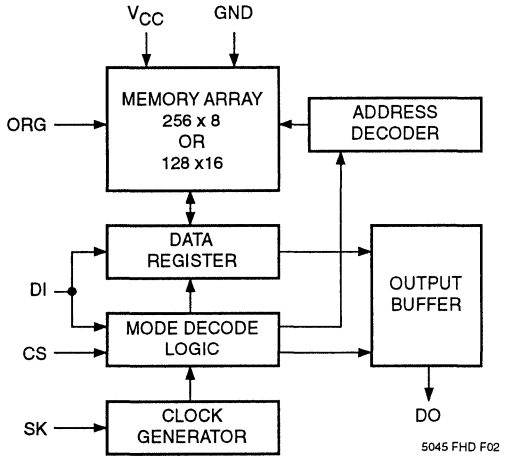


PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+3V Power Supply
GND	Ground
NC	No Connection
ORG	Memory Organization

Note: When the ORG pin is connected to V_{CC}, the 128 x 16 organization is selected. When it is connected to ground, the 256 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 128 x 16 organization.

BLOCK DIAGRAM



TD 5045

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT93LC56 T_A= 0°C to +70°C, V_{CC} = +3V±10%, unless otherwise specified.
CAT93LC56I T_A= –40°C to +85°C, V_{CC} = +3V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	Power Supply Current (Operating)			2	mA	DI = 0.0V, SK = 3.0V V_{CC} = 3.0V, CS = 3.0V, Output Open
I_{CC2}	Power Supply Current (Standby)			50	µA	V_{CC} = 3.3V, CS = 0V DI = 0V SK = 0V
I_{LI}	Input Leakage Current			2	µA	V_{IN} = 0V to 3.3V
I_{LO}	Output Leakage Current (Including ORG Pin)			10	µA	V_{OUT} = 0V to 3.3V, CS = 0V
V_{IH}	High Level Input Voltage	V_{CC} – 0.3		V_{CC} + 1	V	
V_{IL}	Low Level Input Voltage	–0.1		0.3	V	
V_{OH}	High Level Output Voltage	V_{CC} – 0.3			V	I_{OH} = –10µA
V_{OL}	Low Level Output Voltage			0.3	V	I_{OL} = 10µA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			256 x 8	128 x 16	256 x 8	128 x 16	
READ(5)	1	1 0	A8–A0	A7–A0			Read Address AN–A0
ERASE(5)	1	1 1	A8–A0	A7–A0			Clear Address AN–A0
WRITE(5)	1	0 1	A8–A0	A7–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	0 0	11XXXXXXX	11XXXXXX			Write Enable
EWDS	1	0 0	00XXXXXXX	00XXXXXX			Write Disable
ERAL	1	0 0	10XXXXXXX	10XXXXXX			Clear All Addresses
WRAL(6)	1	0 0	01XXXXXXX	01XXXXXX	D7–D0	D15–D0	Write All Addresses

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A.C. CHARACTERISTICS

CAT93LC56 T_A= 0°C to +70°C, V_{CC} = +3V±10%, unless otherwise specified.
CAT93LC56I T_A= –40°C to +85°C, V_{CC} = +3V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	200			ns	
t_{CSH}	CS Hold Time	0			ns	C_L = 100pF
t_{DIS}	DI Setup Time	400			ns	V_{OL} = 0.3V
t_{DIH}	DI Hold Time	400			ns	V_{OH} = V_{CC} –0.3
t_{PD1}	Output Delay to 1			2	µs	V_{IL} = 0.3V
t_{PD0}	Output Delay to 0			2	µs	V_{IH} = V_{CC} –0.3
t_{HZ}(3)	Output Delay to High-Z			400	ns	
t_{EW}	Program/Erase Pulse Width			20	ms	
t_{CSMIN}	Minimum CS Low Time	1			µs	
t_{SKHI}	Minimum SK High Time	1			µs	
t_{SKLOW}	Minimum SK Low time	1			µs	
t_{SV}	Output Delay to Status Valid			1	µs	C_L = 100pF
SK_{MAX}	Maximum Clock Frequency	DC		250	kHz	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(5) Address bit A8 for 256 x 8 ORG and A7 for 128 x 16 ORG are "Don't Care" bits, but must be kept at either a "1" or "0" for READ, WRITE and ERASE commands.
(6) The WRAL command is for test mode only and is not guaranteed over operating conditions.

DEVICE OPERATION

The CAT93LC56/CAT93LC56I is a 2048 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93LC56/CAT93LC56I can be organized as either 128 registers by 16 bits, or as 256 registers by 8 bits. Seven 11 bit instructions (12 bit instruction in 256 by 8 organization) control the reading, writing and erase operations of the device. The CAT93LC56/CAT93LC56I operates on a single 3V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the CAT93LC56/CAT93LC56I is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 8 bit address (9 bit address when organized as 256 x 8), and for write operations a 16 bit data field (8 bit data field when organized as 256 x 8).

Figure 1. Sychronous Data Timing (7)

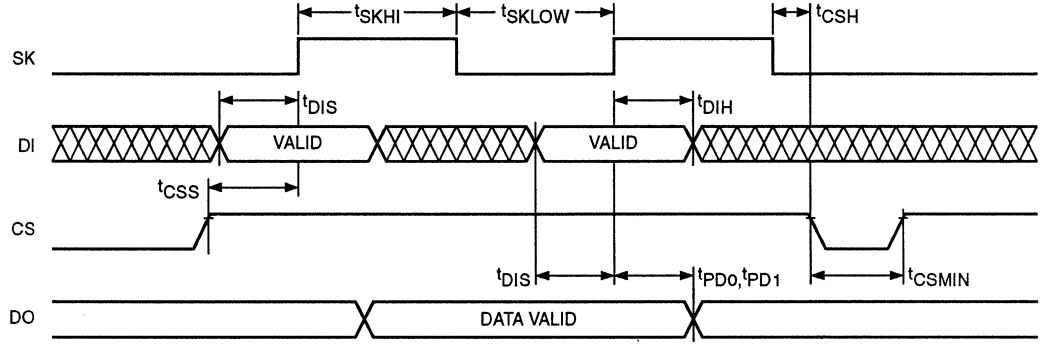

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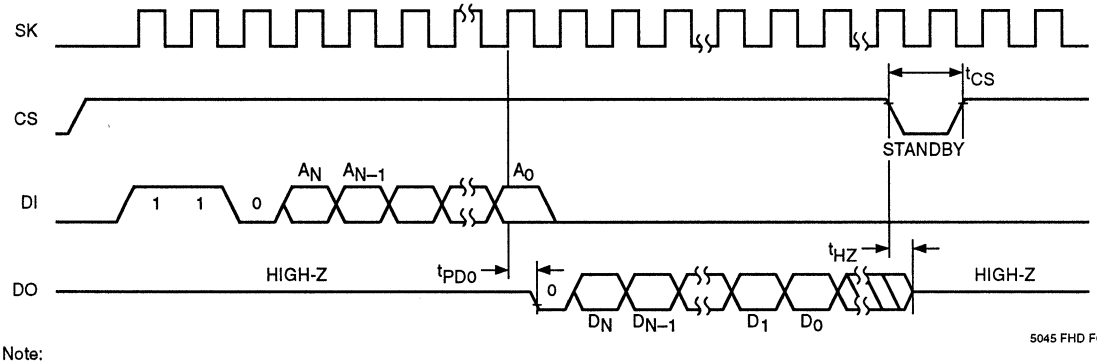
Figure 2. Read Instruction Timing (7)



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Note:
(7) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A8 and DN = D7. When x16 organization is selected, AN = A7 and DN = D15.

At power-down, when V_{CC} falls below a threshold of approximately 2.4V, the data protection circuitry inhibits the erase and write instructions and a write disable (EWDS) is executed internally.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93LC56/ CAT93LC56I will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}). The most significant bit of the address is a "Don't Care" bit, but it must be kept at either a "1" or a "0" for READ, WRITE and ERASE commands.

Write

After receiving a WRITE command, address and the data, the CS (chip select) pin must be deselected for a minimum of 1µs (t_{CSMIN}). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93LC56/CAT93LC56I can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent. The most significant bit of the address is a "Don't Care" bit, but it must be kept at either a "1" or a "0" for READ, WRITE and ERASE commands.

Erase

Upon receiving an ERASE command and address, the CS (chip select) pin must be deselected for a minimum of 1µs (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of the memory location specified in the instruction. The clocking of the SK pin is not neces-

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Figure 3. Write Instruction Timing (7)

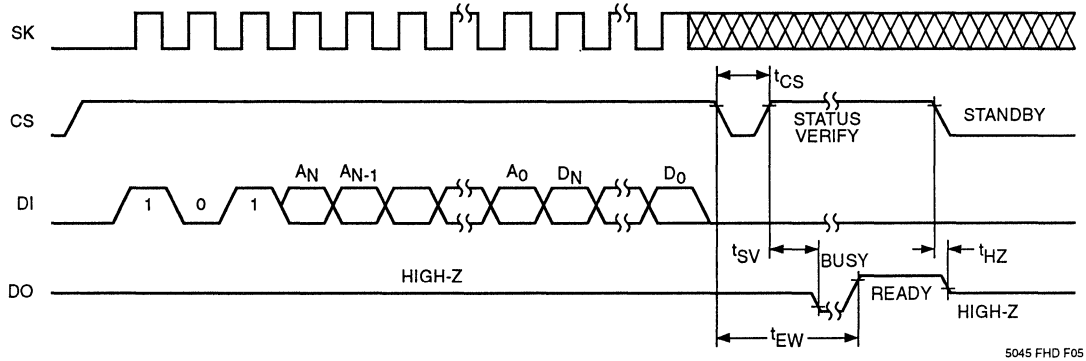
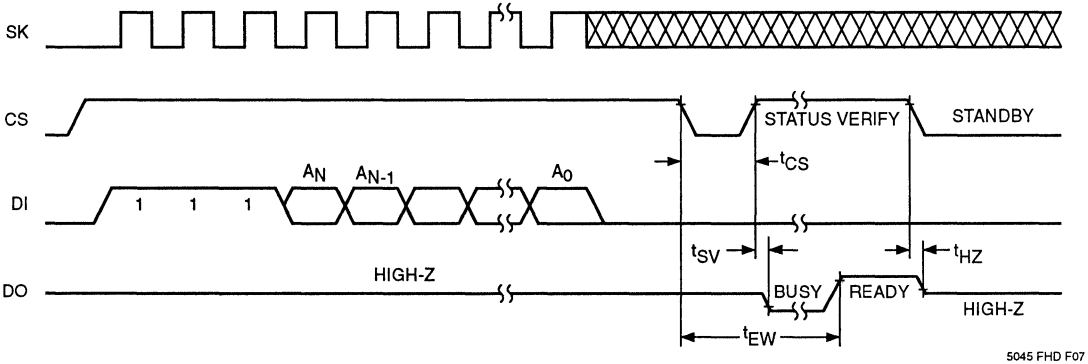


Figure 4. Erase Instruction Timing (7)



Note:

(7) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A8 and DN = D7. When x16 organization is selected, AN = A7 and DN = D15.

sary after the device has entered the self clocking mode. The ready/busy status of the CAT93LC56/CAT93LC56I can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state. The most significant bit of the address is a "Don't Care" bit, but it must be kept at either a "1" or a "0" for READ, WRITE and ERASE commands.

Erase/Write Enable and Disable

The CAT93LC56/CAT93LC56I powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93LC56/CAT93LC56I write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (chip select) pin must be deselected for a minimum of 1µs (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93LC56/CAT93LC56I can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Figure 5. EWEN/EWDS Instruction Timing (7)

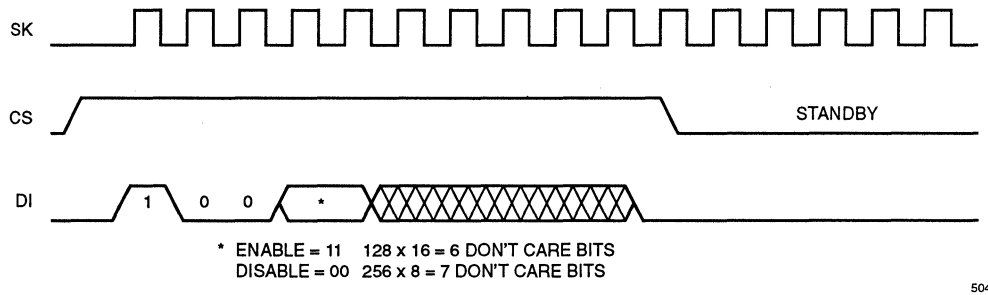
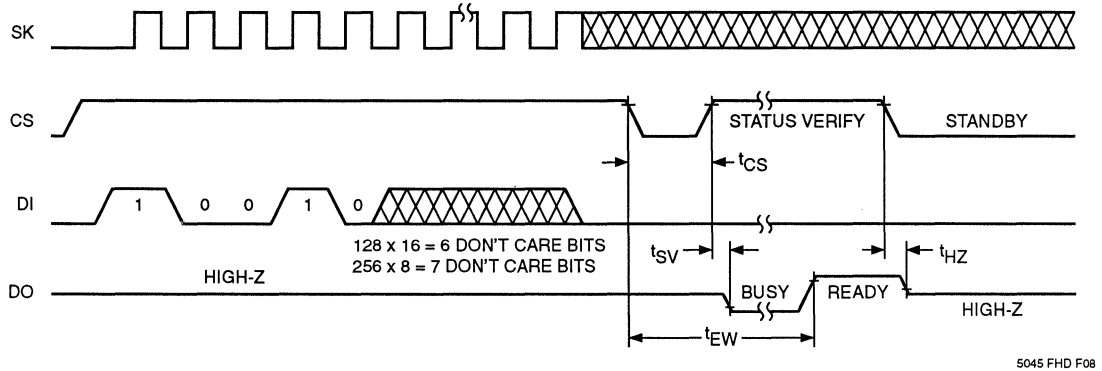


Figure 6. ERAL Instruction Timing (7)

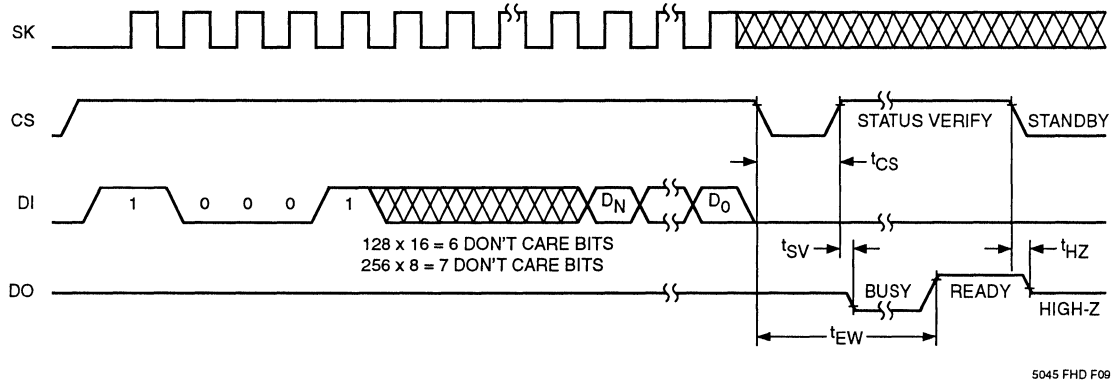


Note:
(7) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A8 and DN = D7. When x16 organization is selected, AN = A7 and DN = D15.

Write All

Upon receiving a WRAL command and data, the CS (chip select) pin must be deselected for a minimum of 1µs (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93LC56/CAT93LC56I can be determined by selecting the device and polling the DO pin. It IS NOT necessary for all memory locations to be cleared before the WRAL command is executed.

Figure 7. WRAL Instruction Timing (7)



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Note:
(7) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A8 and DN = D7. When x16 organization is selected, AN = A7 and DN = D15.

CAT35C102/CAT35C102I

2K-Bit SERIAL E²PROM

FEATURES

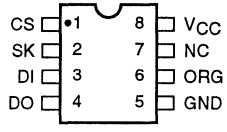
- High Speed Operation: 1MHz
- Low Power CMOS Technology
- Single 5V Supply
- 128 x 16 or 256 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

DESCRIPTION

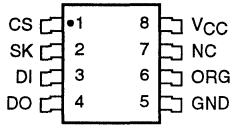
The CAT35C102 and CAT35C102I are 2K bit Serial E²PROM memory devices which can be configured as either 128 registers by 16 bits (ORG pin at V_{CC}) or 256 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C102/CAT35C102I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION

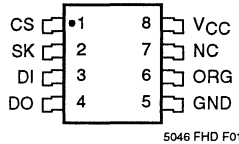
DIP Package



SO Package S



SO Package K



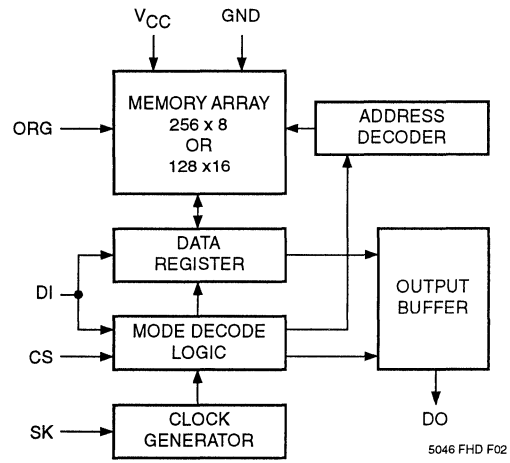
5046 FHD F01

PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+5V Power Supply
GND	Ground
NC	No Connection
ORG	Memory Organization

Note: When the ORG pin is connected to V_{CC}, the 128 x 16 organization is selected. When it is connected to ground, the 256 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 128 x 16 organization.

BLOCK DIAGRAM



5046 FHD F02

TD 5046

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT35C102 T_A= 0°C to +70°C, V_{CC} = +5V±10%, unless otherwise specified.
CAT35C102I T_A= –40°C to +85°C, V_{CC} = +5V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	Power Supply Current (Operating)			3	mA	DI = 0.0V, SK = 5.0V V_{CC} = 5.0V, CS = 5.0V, Output Open
I_{CC2}	Power Supply Current (Standby)			100	µA	V_{CC} = 5.5V, CS = 0V DI = 0V SK = 0V
I_{LI}	Input Leakage Current			2	µA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current (Including ORG Pin)			10	µA	V_{OUT} = 0V to 5.5V, CS = 0V
V_{IH}	High Level Input Voltage	2.0		V_{CC} + 1	V	
V_{IL}	Low Level Input Voltage	–0.1		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1mA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			256 x 8	128 x 16	256 x 8	128 x 16	
READ	1	1 0	A7–A0	A6–A0			Read Address AN–A0
ERASE	1	1 1	A7–A0	A6–A0			Clear Address AN–A0
WRITE	1	0 1	A7–A0	A6–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	0 0	11XXXXXX	11XXXXX			Write Enable
EWDS	1	0 0	00XXXXXX	00XXXXX			Write Disable
ERAL	1	0 0	10XXXXXX	10XXXXX			Clear All Addresses
WRAL	1	0 0	01XXXXXX	01XXXXX	D7–D0	D15–D0	Write All Addresses

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A.C. CHARACTERISTICS

CAT35C102 T_A= 0°C to +70°C, V_{CC} = +5V±10%, unless otherwise specified.
CAT35C102I T_A= –40°C to +85°C, V_{CC} = +5V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	50			ns	
t_{CSH}	CS Hold Time	0			ns	
t_{DIS}	DI Setup Time	100			ns	C_L = 100pF
t_{DIH}	DI Hold Time	100			ns	V_{OL} = 0.8V, V_{OH} = 2.0V
t_{PD1}	Output Delay to 1			500	ns	V_{IL} = 0.45V, V_{IH} = 2.4V
t_{PD0}	Output Delay to 0			500	ns	
t_{HZ}(3)	Output Delay to High-Z			100	ns	
t_{EW}	Program/Erase Pulse Width			10	ms	
t_{CSMIN}	Minimum CS Low Time	250			ns	
t_{SKHI}	Minimum SK High Time	250			ns	
t_{SKLOW}	Minimum SK Low Time	250			ns	
t_{SV}	Output Delay to Status Valid			500	ns	C_L = 100pF
SK_{MAX}	Maximum Clock Frequency	DC		1	MHz	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.

DEVICE OPERATION

The CAT35C102/CAT35C102I is a 2048 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT35C102/CAT35C102I can be organized as either 128 registers by 16 bits, or as 256 registers by 8 bits. Seven 10 bit instructions (11 bit instruction in 256 by 8 organization) control the reading, writing and erase operations of the device. The CAT35C102/CAT35C102I operates on a single 5V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the CAT35C102/CAT35C102I is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 7 bit address (8 bit address when organized as 256 x 8), and for write operations a 16 bit data field (8 bit data field when organized as 256 x 8).

Figure 1. Sychronous Data Timing (5)

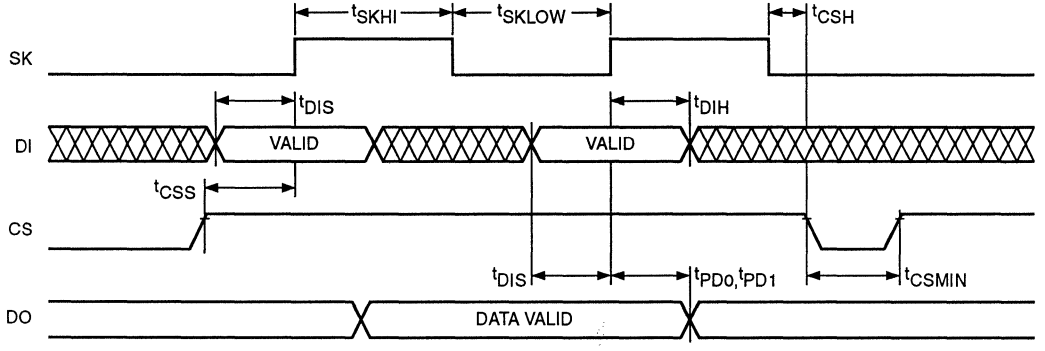

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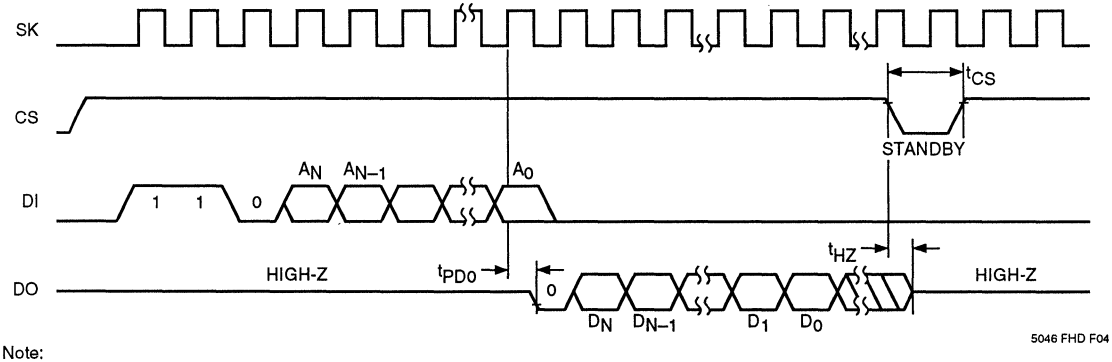
Figure 2. Read Instruction Timing (5)



5046 FHD F04

Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A7 and DN = D7. When x16 organization is selected, AN = A6 and DN = D15.

At power-down, when V_{CC} falls below a threshold of approximately 3.5V, the data protection circuitry inhibits the erase and write instructions and a write disable (EWDS) is executed internally.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT35C102/CAT35C102I will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Write

After receiving a WRITE command, address and the data, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C102/CAT35C102I can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent.

Erase

Upon receiving an ERASE command and address, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of the memory location specified in the instruction. The clocking of the SK pin is not neces-

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Figure 3. Write Instruction Timing (5)

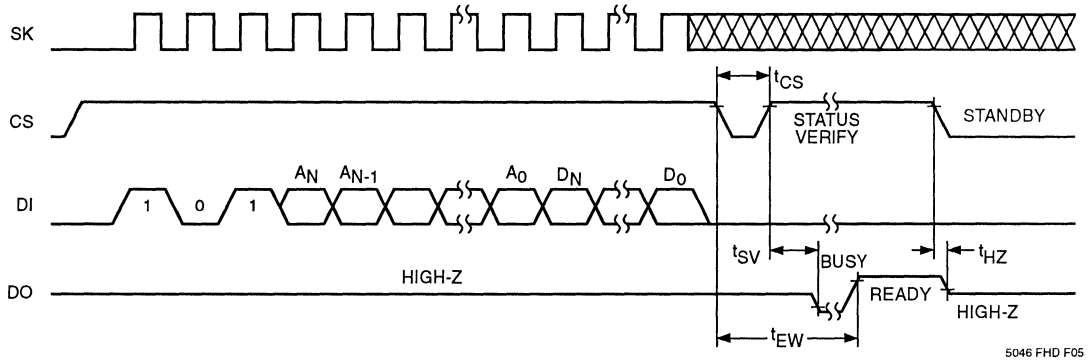
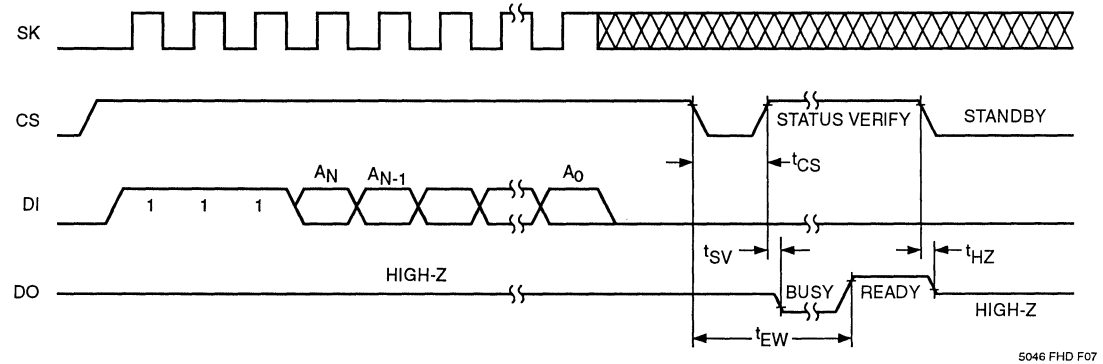


Figure 4. Erase Instruction Timing (5)



Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A7 and DN = D7. When x16 organization is selected, AN = A6 and DN = D15.

sary after the device has entered the self clocking mode. The ready/busy status of the CAT35C102/CAT35C102I can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

Erase/Write Enable and Disable

The CAT35C102/CAT35C102I powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT35C102/CAT35C102I write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C102/CAT35C102I can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Figure 5. EWEN/EWDS Instruction Timing (5)

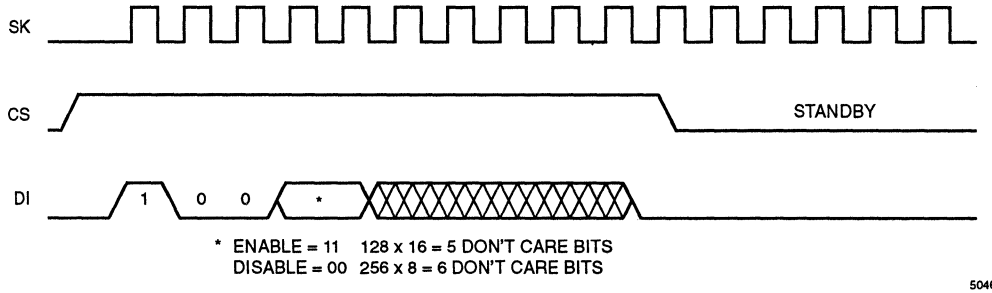
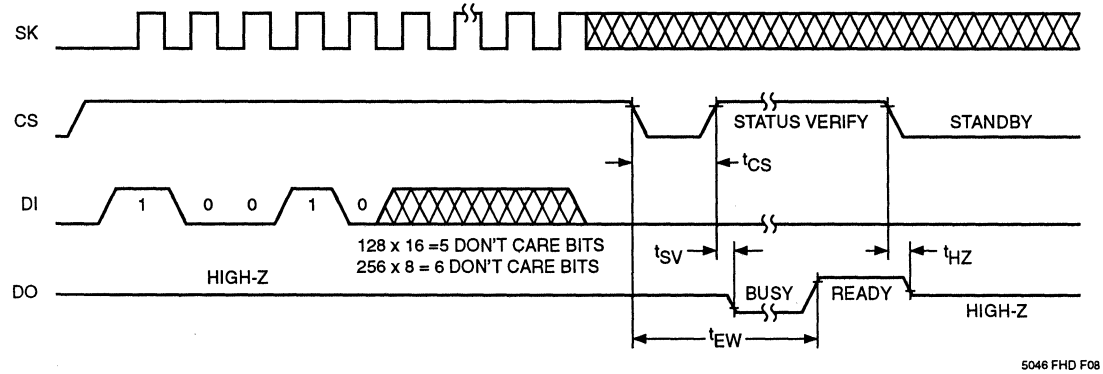


Figure 6. ERAL Instruction Timing (5)

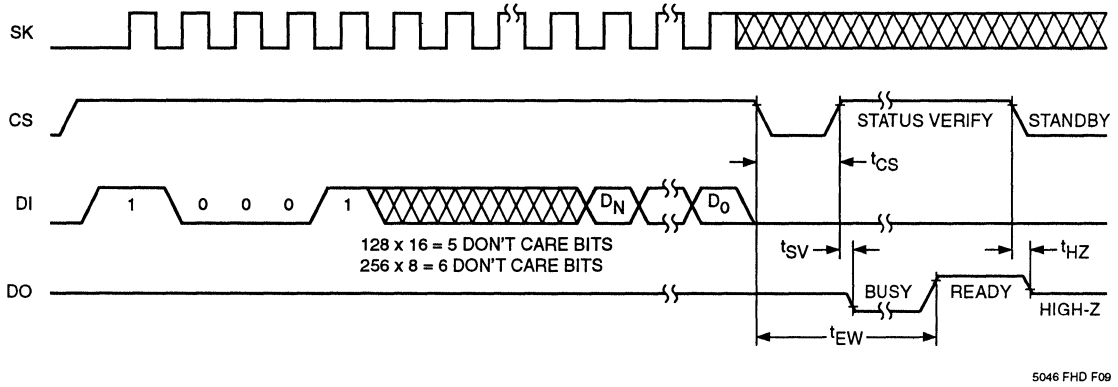


Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A7 and DN = D7. When x16 organization is selected, AN = A6 and DN = D15.

Write All

Upon receiving a WRAL command and data, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C102/CAT35C102I can be determined by selecting the device and polling the DO pin. It IS necessary for all memory locations to be cleared before the WRAL command is executed.

Figure 7. WRAL Instruction Timing (5)



Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A7 and DN = D7. When x16 organization is selected, AN = A6 and DN = D15.

CAT33C104/CAT33C104I

4K-Bit SERIAL E²PROM

FEATURES

- Low Power CMOS Technology
- Single 3V Supply
- 256 x 16 or 512 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

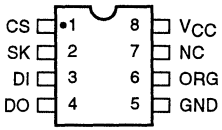
DESCRIPTION

The CAT33C104 and CAT33C104I are 4K bit Serial E²PROM memory devices which can be configured as either 256 registers by 16 bits (ORG pin at V_{CC}) or 512 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin.

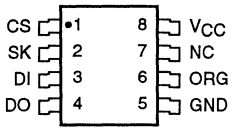
The CAT33C104/CAT33C104I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION

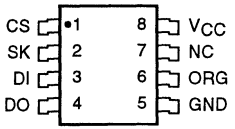
DIP Package



SO Package S



SO Package K



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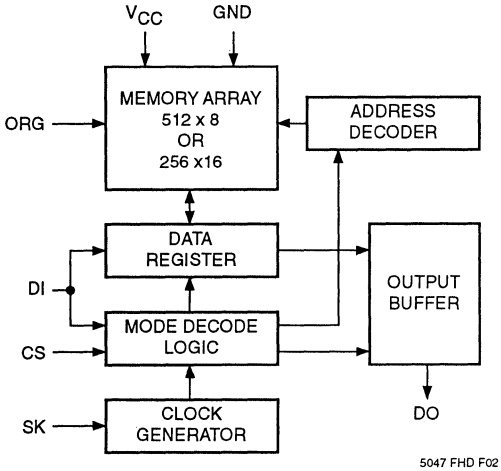
PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+3V Power Supply
GND	Ground
NC	No Connection
ORG	Memory Organization

Note: When the ORG pin is connected to V_{CC}, the 256 x 16 organization is selected. When it is connected to ground, the 512 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 256 x 16 organization.

BLOCK DIAGRAM



5047 FHD F02

TD 5047

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground[1] .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current[2] .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}[3]	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}[3]	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}[3]	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}[3][4]	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT33C104 T_A= 0°C to +70°C, V_{CC} = +3V±10%, unless otherwise specified.
CAT33C104I T_A= –40°C to +85°C, V_{CC} = +3V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	Power Supply Current (Operating)			2	mA	DI = 0.0V, SK = 3.0V V_{CC} = 3.0V, CS = 3.0V, Output Open
I_{CC2}	Power Supply Current (Standby)			50	µA	V_{CC} = 3.3V, CS = 0V DI = 0V SK = 0V
I_{LI}	Input Leakage Current			2	µA	V_{IN} = 0V to 3.3V
I_{LO}	Output Leakage Current (Including ORG Pin)			10	µA	V_{OUT} = 0V to 3.3V, CS = 0V
V_{IH}	High Level Input Voltage	V_{CC} – 0.3		V_{CC} + 1	V	
V_{IL}	Low Level Input Voltage	–0.1		0.3	V	
V_{OH}	High Level Output Voltage	V_{CC} – 0.3			V	I_{OH} = –10µA
V_{OL}	Low Level Output Voltage			0.3	V	I_{OL} = 10µA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			512 x 8	256 x 16	512 x 8	256 x 16	
READ	1	1 0	A8–A0	A7–A0			Read Address AN–A0
ERASE	1	1 1	A8–A0	A7–A0			Clear Address AN–A0
WRITE	1	0 1	A8–A0	A7–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	0 0	11XXXXXXX	11XXXXXX			Write Enable
EWDS	1	0 0	00XXXXXXX	00XXXXXX			Write Disable
ERAL	1	0 0	10XXXXXXX	10XXXXXX			Clear All Addresses
WRAL(5)	1	0 0	01XXXXXXX	01XXXXXX	D7–D0	D15–D0	Write All Addresses

3

A.C. CHARACTERISTICS

CAT33C104 T_A= 0°C to +70°C, V_{CC} = +3V±10%, unless otherwise specified.
CAT33C104I T_A= –40°C to +85°C, V_{CC} = +3V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	200			ns	
t_{CSH}	CS Hold Time	0			ns	C_L = 100pF
t_{DIS}	DI Setup Time	400			ns	V_{OL} = 0.3V
t_{DIH}	DI Hold Time	400			ns	V_{OH} = V_{CC} – 0.3
t_{PD1}	Output Delay to 1			2	µs	V_{IL} = 0.3V
t_{PD0}	Output Delay to 0			2	µs	V_{IH} = V_{CC} – 0.3
t_{HZ}(3)	Output Delay to High-Z			400	ns	
t_{EW}	Program/Erase Pulse Width			20	ms	
t_{CSMIN}	Minimum CS Low Time	1			µs	
t_{SKHI}	Minimum SK High Time	1			µs	
t_{SKLOW}	Minimum SK Low time	1			µs	
t_{SV}	Output Delay to Status Valid			1	µs	C_L = 100pF
SK_{MAX}	Maximum Clock Frequency	DC		250	kHz	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(5) The WRAL command is for test mode only and is not guaranteed over operating conditions.

DEVICE OPERATION

The CAT33C104/CAT33C104I is a 4096 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT33C104/CAT33C104I can be organized as either 256 registers by 16 bits, or as 512 registers by 8 bits. Seven 11 bit instructions (12 bit instruction in 512 by 8 organization) control the reading, writing and erase operations of the device. The CAT33C104/CAT33C104I operates on a single 3V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the CAT33C104/CAT33C104I is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 8 bit address (9 bit address when organized as 512 x 8), and for write operations a 16 bit data field (8 bit data field when organized as 512 x 8).

Figure 1. Sychronous Data Timing (6)

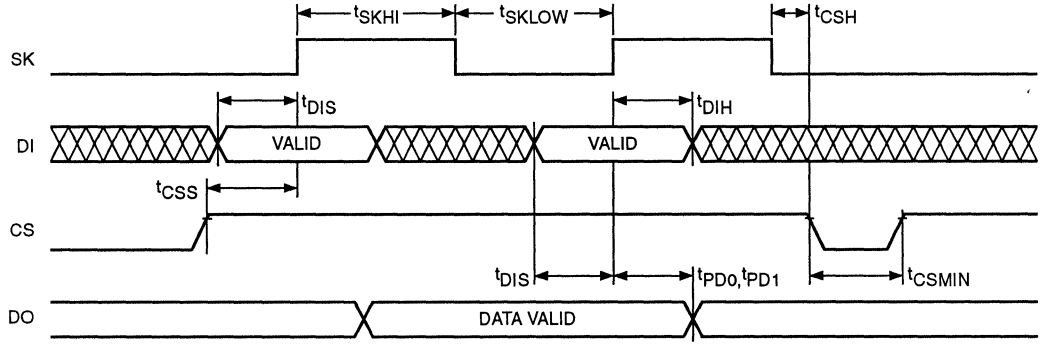


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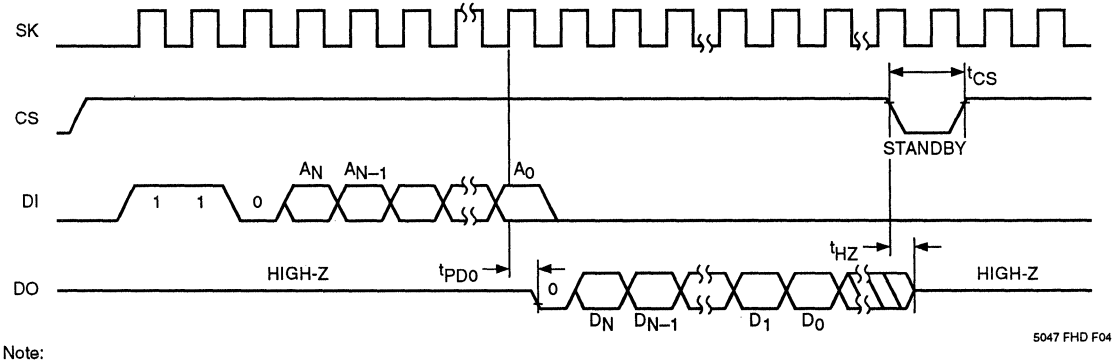
Figure 2. Read Instruction Timing (6)



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Note:
(6) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A8 and DN = D7. When x16 organization is selected, AN = A7 and DN = D15.

At power-down, when V_{CC} falls below a threshold of approximately 2.4V, the data protection circuitry inhibits the erase and write instructions and a write disable (EWDS) is executed internally.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT33C104/CAT33C104I will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Write

After receiving a WRITE command, address and the data, the CS (chip select) pin must be deselected for a minimum of 1µs (t_{CSMIN}). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C104/CAT33C104I can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent.

Erase

Upon receiving an ERASE command and address, the CS (chip select) pin must be deselected for a minimum of 1µs (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of the memory location specified in the instruction. The clocking of the SK pin is not neces-

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Figure 3. Write Instruction Timing (6)

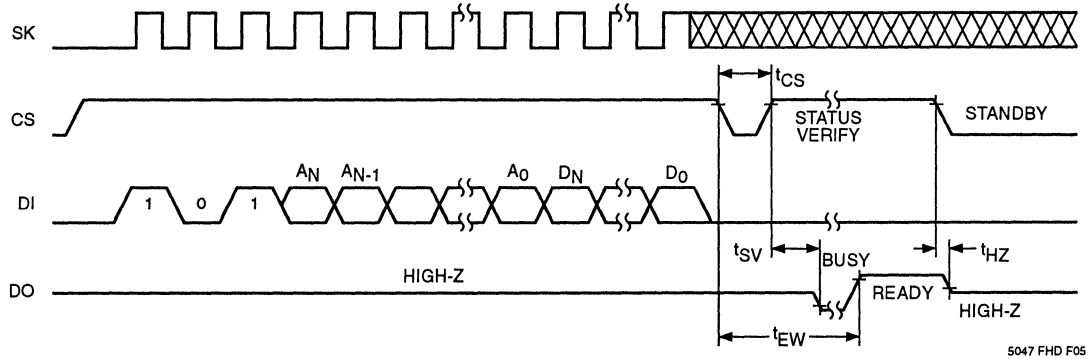
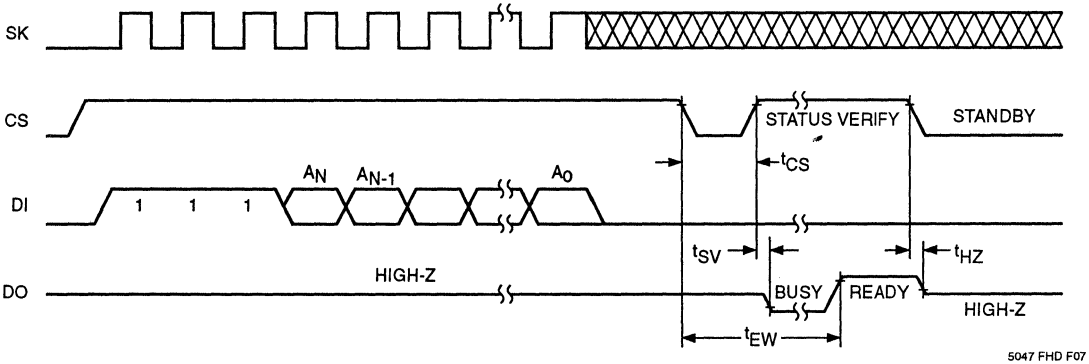


Figure 4. Erase Instruction Timing (6)



Note:
(6) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A8 and DN = D7. When x16 organization is selected, AN = A7 and DN = D15.

sary after the device has entered the self clocking mode. The ready/busy status of the CAT33C104/CAT33C104I can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

Erase/Write Enable and Disable

The CAT33C104/CAT33C104I powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT33C104/CAT33C104I write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (chip select) pin must be deselected for a minimum of 1µs (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C104/CAT33C104I can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Figure 5. EWEN/EWDS Instruction Timing (6)

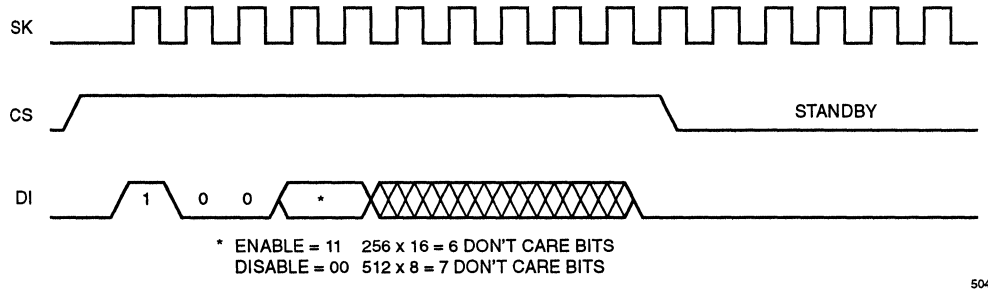
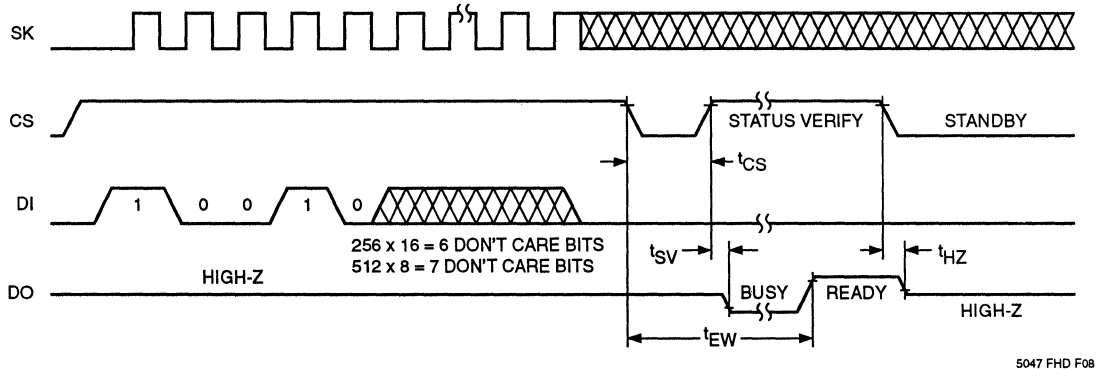


Figure 6. ERAL Instruction Timing (6)



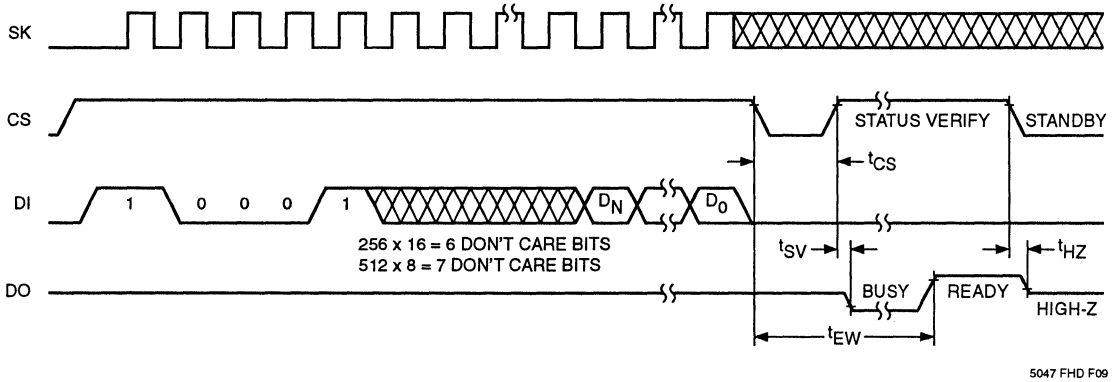
Note:
(6) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A8 and DN = D7. When x16 organization is selected, AN = A7 and DN = D15.

Write All

Upon receiving a WRAL command and data, the CS (chip select) pin must be deselected for a minimum of 1µs (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device.

The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C104/CAT33C104I can be determined by selecting the device and polling the DO pin. It IS NOT necessary for all memory locations to be cleared before the WRAL command is executed.

Figure 7. WRAL Instruction Timing (6)



Note:
(6) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A8 and DN = D7. When x16 organization is selected, AN = A7 and DN = D15.

CAT35C104/CAT35C104I

4K-Bit SERIAL E²PROM

FEATURES

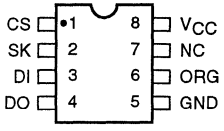
- High Speed Operation: 1MHz
- Low Power CMOS Technology
- Single 5V Supply
- 256 x 16 or 512 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

DESCRIPTION

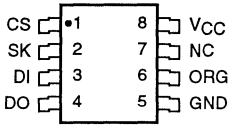
The CAT35C104 and CAT35C104I are 4K bit Serial E²PROM memory devices which can be configured as either 256 registers by 16 bits (ORG pin at V_{CC}) or 512 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C104/CAT35C104I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION

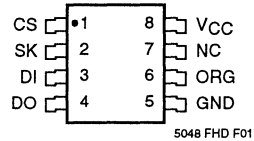
DIP Package



SO Package S



SO Package K



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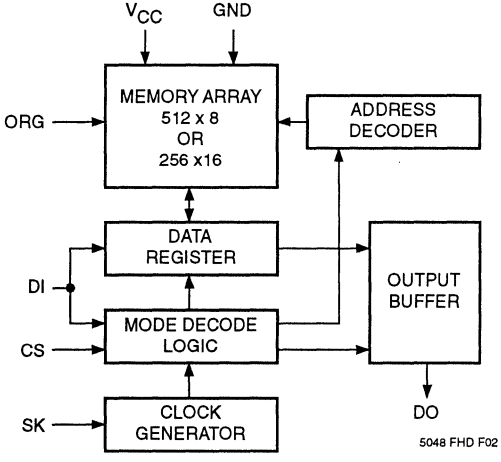
PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+5V Power Supply
GND	Ground
NC	No Connection
ORG	Memory Organization

Note: When the ORG pin is connected to V_{CC}, the 256 x 16 organization is selected. When it is connected to ground, the 512 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 256 x 16 organization.

BLOCK DIAGRAM



5048 FHD F02

TD 5048

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT35C104 T_A= 0°C to +70°C, V_{CC} = +5V±10%, unless otherwise specified.
CAT35C104I T_A= –40°C to +85°C, V_{CC} = +5V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	Power Supply Current (Operating)			3	mA	DI = 0.0V, SK = 5.0V V_{CC} = 5.0V, CS = 5.0V, Output Open
I_{CC2}	Power Supply Current (Standby)			100	µA	V_{CC} = 5.5V, CS = 0V DI = 0V SK = 0V
I_{LI}	Input Leakage Current			2	µA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current (Including ORG Pin)			10	µA	V_{OUT} = 0V to 5.5V, CS = 0V
V_{IH}	High Level Input Voltage	2.0		V_{CC} + 1	V	
V_{IL}	Low Level Input Voltage	–0.1		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1mA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			512 x 8	256 x 16	512 x 8	256 x 16	
READ	1	1 0	A8–A0	A7–A0			Read Address AN–A0
ERASE	1	1 1	A8–A0	A7–A0			Clear Address AN–A0
WRITE	1	0 1	A8–A0	A7–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	0 0	11XXXXXXX	11XXXXXX			Write Enable
EWDS	1	0 0	00XXXXXXX	00XXXXXX			Write Disable
ERAL	1	0 0	10XXXXXXX	10XXXXXX			Clear All Addresses
WRAL	1	0 0	01XXXXXXX	01XXXXXX	D7–D0	D15–D0	Write All Addresses

3

A.C. CHARACTERISTICS

CAT35C104 T_A= 0°C to +70°C, V_{CC} = +5V±10%, unless otherwise specified.
CAT35C104I T_A= –40°C to +85°C, V_{CC} = +5V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	50			ns	
t_{CSH}	CS Hold Time	0			ns	
t_{DIS}	DI Setup Time	100			ns	C_L = 100pF
t_{DIH}	DI Hold Time	100			ns	V_{OL} = 0.8V, V_{OH} = 2.0V
t_{PD1}	Output Delay to 1			500	ns	V_{IL} = 0.45V, V_{IH} = 2.4V
t_{PD0}	Output Delay to 0			500	ns	
t_{HZ}(3)	Output Delay to High-Z			100	ns	
t_{EW}	Program/Erase Pulse Width			10	ms	
t_{CSMIN}	Minimum CS Low Time	250			ns	
t_{SKHI}	Minimum SK High Time	250			ns	
t_{SKLOW}	Minimum SK Low time	250			ns	
t_{SV}	Output Delay to Status Valid			500	ns	C_L = 100pF
SK_{MAX}	Maximum Clock Frequency	DC		1	MHz	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.

DEVICE OPERATION

The CAT35C104/CAT35C104I is a 4096 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT35C104/CAT35C104I can be organized as either 256 registers by 16 bits, or as 512 registers by 8 bits. Seven 11 bit instructions (12 bit instruction in 512 by 8 organization) control the reading, writing and erase operations of the device. The CAT35C104/CAT35C104I operates on a single 5V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the CAT35C104/CAT35C104I is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 8 bit address (9 bit address when organized as 512 x 8), and for write operations a 16 bit data field (8 bit data field when organized as 512 x 8).

Figure 1. Sychronous Data Timing (5)

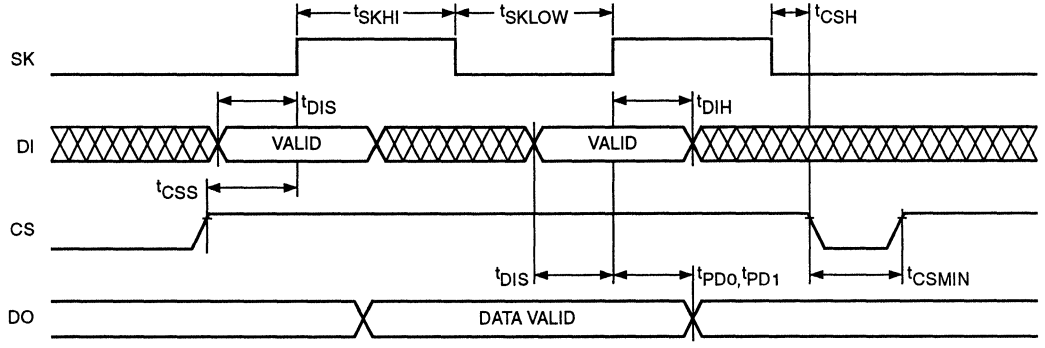


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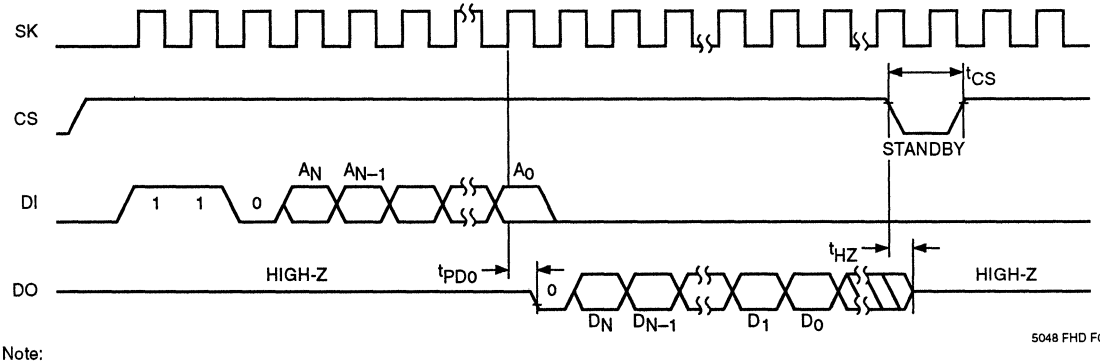
Figure 2. Read Instruction Timing (5)



5048 FHD F04

Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A8 and DN = D7. When x16 organization is selected, AN = A7 and DN = D15.

At power-down, when V_{CC} falls below a threshold of approximately 3.5V, the data protection circuitry inhibits the erase and write instructions and a write disable (EWDS) is executed internally.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT35C104/CAT35C104I will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Write

After receiving a WRITE command, address and the data, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C104/CAT35C104I can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent.

Erase

Upon receiving an ERASE command and address, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of the memory location specified in the instruction. The clocking of the SK pin is not neces-

3

Figure 3. Write Instruction Timing (5)

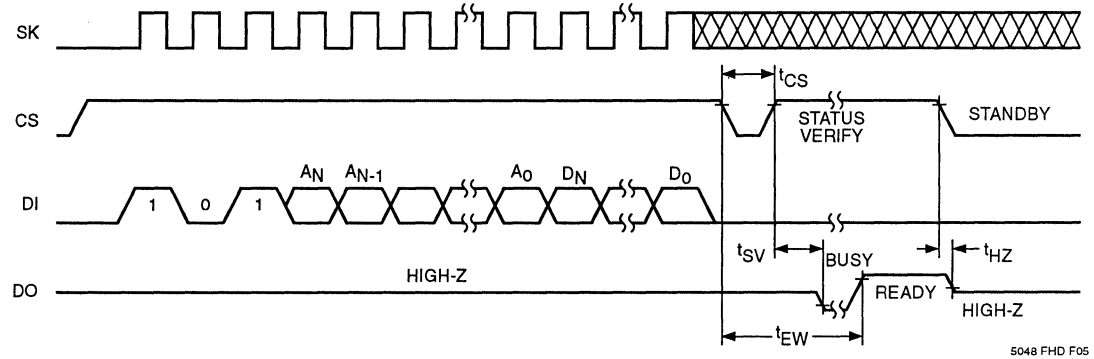
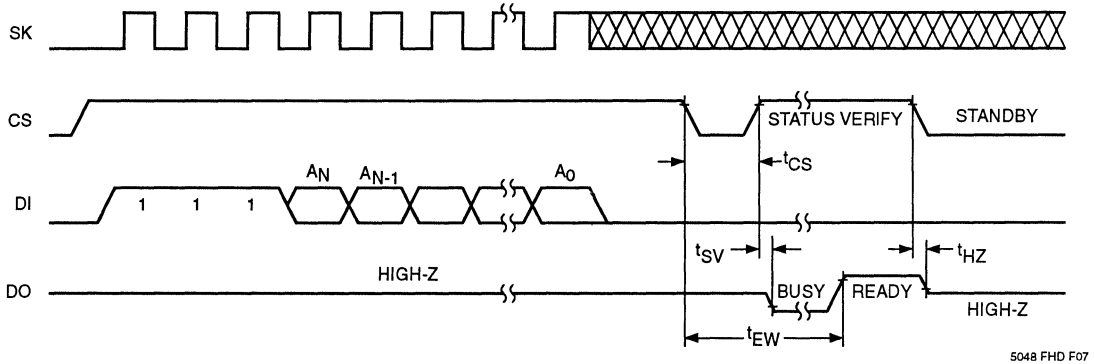


Figure 4. Erase Instruction Timing (5)



Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A8 and DN = D7. When x16 organization is selected, AN = A7 and DN = D15.

sary after the device has entered the self clocking mode. The ready/busy status of the CAT35C104/CAT35C104I can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

Erase/Write Enable and Disable

The CAT35C104/CAT35C104I powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT35C104/CAT35C104I write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C104/CAT35C104I can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Figure 5. EWEN/EWDS Instruction Timing (5)

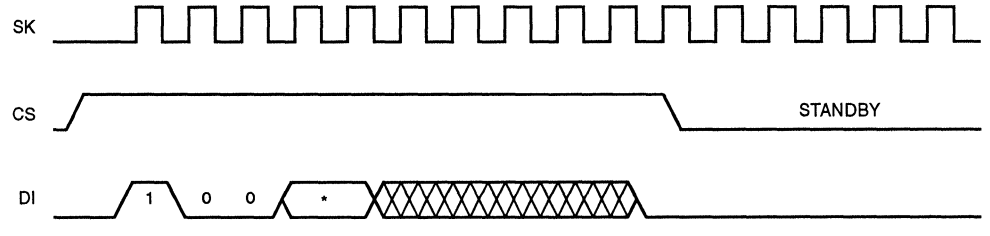


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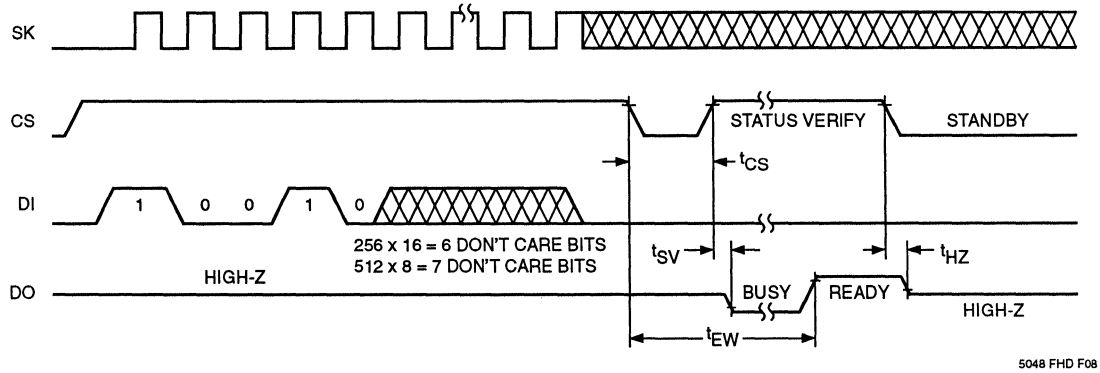
Figure 6. ERAL Instruction Timing (5)



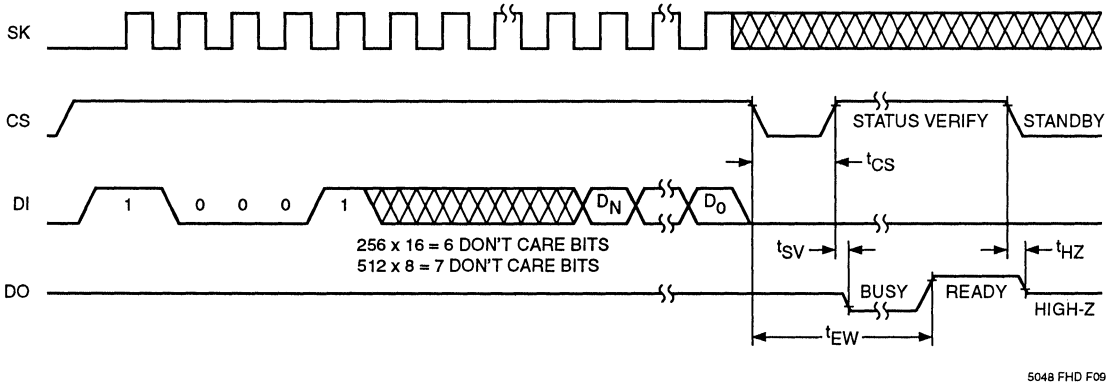
5048 FHD F08

Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A8 and DN = D7. When x16 organization is selected, AN = A7 and DN = D15.

Write All

Upon receiving a WRAL command and data, the CS (chip select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C104/CAT35C104I can be determined by selecting the device and polling the DO pin. It IS NOT necessary for all memory locations to be cleared before the WRAL command is executed.

Figure 7. WRAL Instruction Timing (5)



Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A8 and DN = D7. When x16 organization is selected, AN = A7 and DN = D15.

CAT33C108/CAT33C108I

8K-Bit SERIAL E²PROM

FEATURES

- High Speed Operation: 1MHz
- Low Power CMOS Technology
- Single 3V Supply
- 512 x 16 or 1024 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- Sequential Read
- Program Enable (PE) Pin
- Fast Nonvolatile Write Cycle: 5ms Max
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

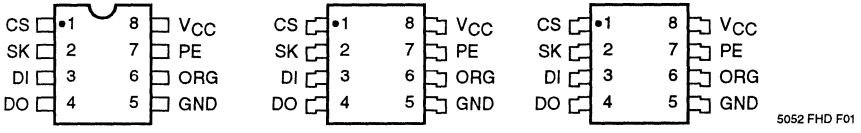
DESCRIPTION

The CAT33C108 and CAT33C108I are 8K bit Serial E²PROM memory devices which can be configured as either 512 registers by 16 bits (ORG pin at V_{CC}) or 1024 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin.

The CAT33C108/CAT33C108I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION

DIP Package / SO Package S / SO Package K



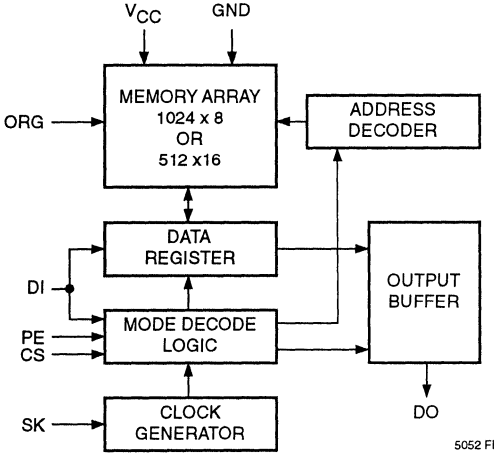
5052 FHD F01

PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+3V Power Supply
GND	Ground
PE	Program Enable
ORG	Memory Organization

Note: When the ORG pin is connected to V_{CC}, the 512 x 16 organization is selected. When it is connected to ground, the 1024 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 512 x 16 organization.

BLOCK DIAGRAM



5052 FHD F02

TD 5052

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT33C108 T_A= 0°C to +70°C, V_{CC} = +3V±10%, unless otherwise specified.
CAT33C108I T_A= –40°C to +85°C, V_{CC} = +3V±10%, unless otherwise specified.

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
I_{CC1}	Power Supply Current (Operating)	Comm.			2	mA	DI = 0.0V, SK = 3.0V V_{CC} = 3.0V, CS = 3.0V, Output Open
		Ind.			3	mA	
I_{CC2}	Power Supply Current (Standby)				10	µA	V_{CC} = 3.3V, CS = 0V DI = 0V SK = 0V
I_{LI}(5)	Input Leakage Current				1	µA	V_{IN} = 0V to 3.3V
I_{LO}(5)	Output Leakage Current (Including ORG Pin)				1	µA	V_{OUT} = 0V to 3.3V, CS = 0V
V_{IH}	High Level Input Voltage		V_{CC} – 0.3		V_{CC} +1	V	
V_{IL}	Low Level Input Voltage		–0.1		0.3	V	
V_{OH}	High Level Output Voltage		V_{CC} – 0.3			V	I_{OH} = –10µA
V_{OL}	Low Level Output Voltage				0.3	V	I_{OL} = 10µA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) PE and ORG pin leakage current (I_{LI} and I_{LO}) = 15 µA max. (at V_{IL}), 10 µA otherwise.

INSTRUCTION SET(6)

Instruction	Start Bit	Opcode	Address		Data		PE	Comments
			1024 x 8	512 x 16	1024 x 8	512 x 16		
READ	1	1 0	XA9–A0	XA8–A0			X	Start Address AN–A0
ERASE	1	1 1	XA9–A0	XA8–A0			1	Clear Address AN–A0
WRITE	1	0 1	XA9–A0	XA8–A0	D7–D0	D15–D0	1	Write Address AN–A0
EWEN	1	0 0	11XXXXXXXXX	11XXXXXXXX			X	Write Enable
EWDS	1	0 0	00XXXXXXXXX	00XXXXXXXX			X	Write Disable
ERAL	1	0 0	10XXXXXXXXX	10XXXXXXXX			1	Clear All Addresses
WRAL	1	0 0	01XXXXXXXXX	01XXXXXXXX	D7–D0	D15–D0	1	Write All Addresses

3

A.C. CHARACTERISTICS

CAT33C108 T_A= 0°C to +70°C, V_{CC} = +3V±10%, unless otherwise specified.
CAT33C108I T_A= –40°C to +85°C, V_{CC} = +3V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	250			ns	
t_{CSH}	CS Hold Time	0			ns	
t_{DIS}	DI Setup Time	250			ns	C_L = 100pF
t_{DIH}	DI Hold Time	250			ns	V_{OL} = 0.3V, V_{OH} = V_{CC} – 0.3
t_{PD1}	Output Delay to 1			500	ns	V_{IL} = 0.3V, V_{IH} = V_{CC} – 0.3
t_{PD0}	Output Delay to 0			500	ns	
t_{HZ}(3)	Output Delay to High-Z			500	ns	
t_{EW}(7)	Program/Erase Pulse Width			5	ms	
t_{CSMIN}	Minimum CS Low Time	500			ns	
t_{SKHI}	Minimum SK High Time	500			ns	
t_{SKLOW}	Minimum SK Low time	500			ns	
t_{SV}	Output Delay to Status Valid			500	ns	C_L = 100pF
SK_{MAX}	Maximum Clock Frequency	DC		1	MHz	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(6) X indicates a "Don't Care" input (either 0 or 1).
(7) ERAL and WRAL instructions = 10 ms max.

DEVICE OPERATION

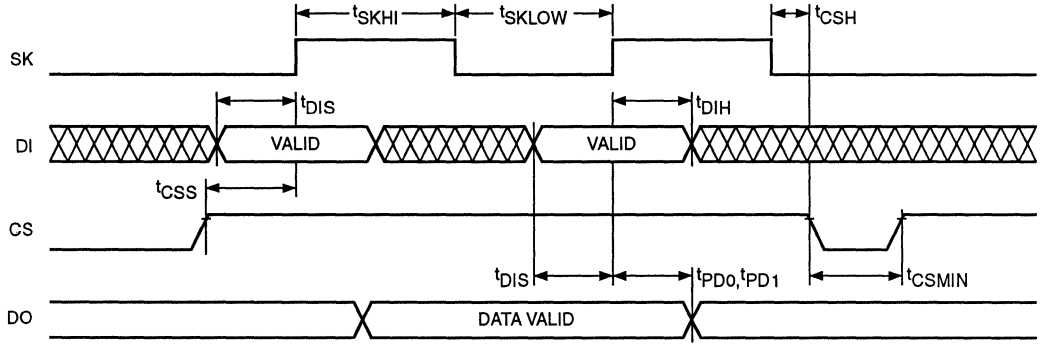
The CAT33C108/CAT33C108I is a 8192 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT33C108/CAT33C108I can be organized as either 512 registers by 16 bits, or as 1024 registers by 8 bits. Seven 13 bit instructions (14 bit instruction in 1024 by 8 organization) control the reading, writing and erase operations of the device. The CAT33C108/CAT33C108I operates on a single 3V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

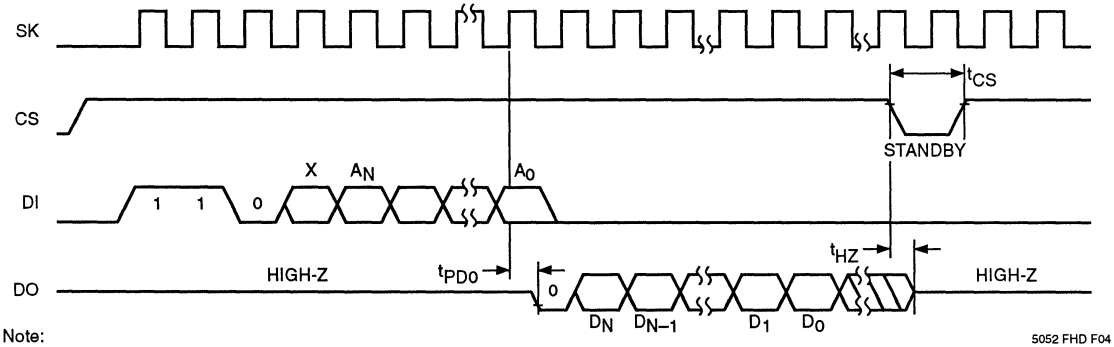
The format for all instructions sent to the CAT33C108/CAT33C108I is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 9 bit address (10 bit address when organized as 1024 x 8), and for write operations a 16 bit data field (8 bit data field when organized as 1024 x 8). All program/erase cycles are enabled only when pin 7 (PE) is held high.

Figure 1. Sychronous Data Timing (8)



5052 FHD F03

Figure 2. Read Instruction Timing (8)(9)



5052 FHD F04

Note:
(8) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A9 and DN = D7. When x16 organization is selected, AN = A8 and DN = D15.
(9) PE = "Don't Care".

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT33C108/CAT33C108I will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}). The data output is sequential with the data from address N followed by the data from address N+1. The data output continues to the highest address and will wrap around to the first address if the clock continues to run. Bringing CS low at any time will stop the data output. The dummy bit is suppressed in the sequential read mode (except for the very first address) and a continuous stream of data results.

Write

After receiving a WRITE command, address and the data, the CS (chip select) pin must be deselected for a minimum of 500ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C108/CAT33C108I can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent. The Write instruction requires that PE = 1.

3

Figure 3. Write Instruction Timing (8)

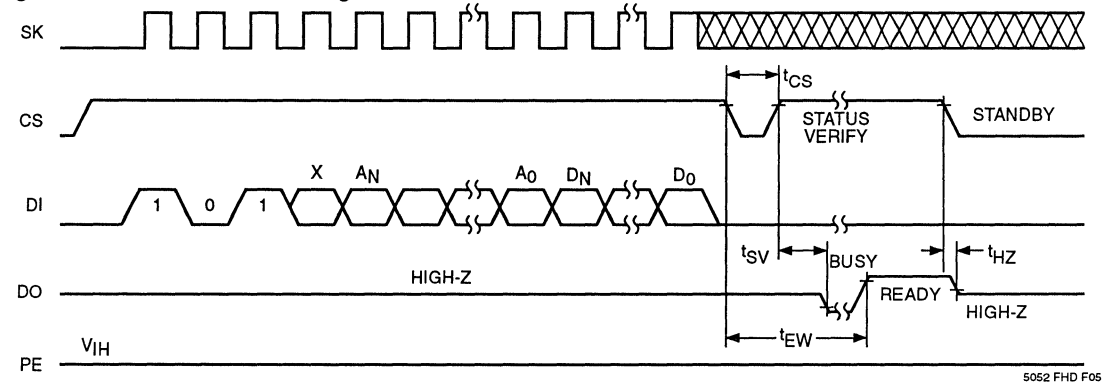
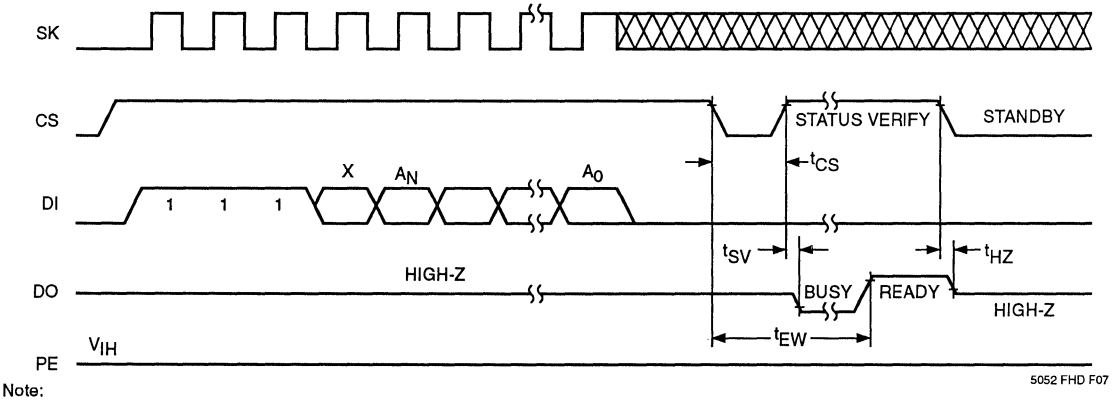


Figure 4. Erase Instruction Timing (8)



Note:
(8) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A9 and DN = D7. When x16 organization is selected, AN = A8 and DN = D15.

Erase

Upon receiving an ERASE command and address, the CS (chip select) pin must be deselected for a minimum of 500ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C108/CAT33C108I can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state. The Erase instruction requires that PE = 1.

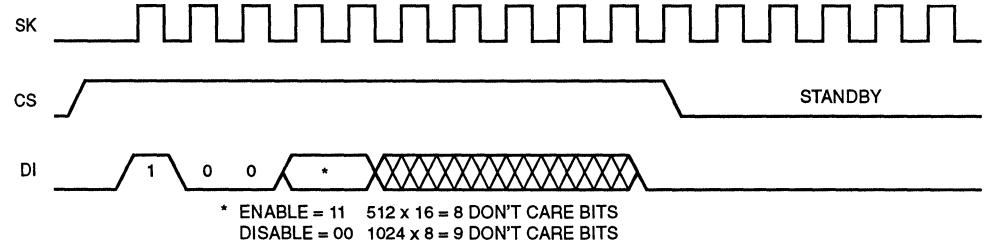
Erase/Write Enable and Disable

The CAT33C108/CAT33C108I powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT33C108/CAT33C108I write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

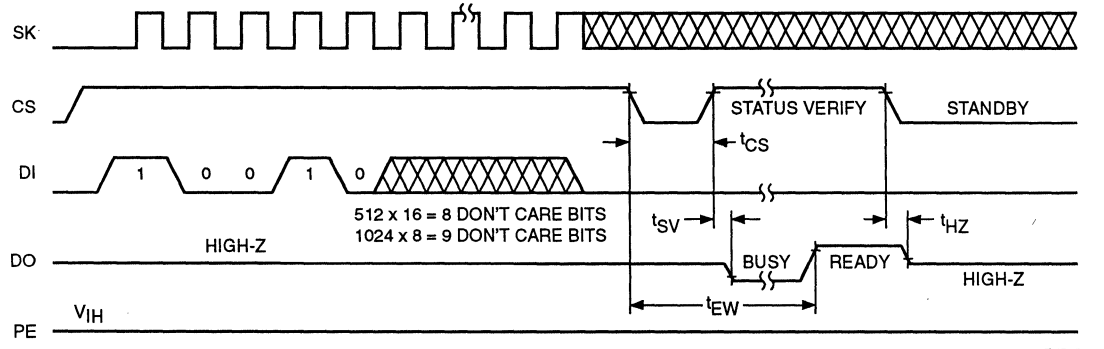
Upon receiving an ERAL command, the CS (chip select) pin must be deselected for a minimum of 500ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C108/CAT33C108I can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state. The Erase All instruction requires that PE = 1.

Figure 5. EWEN/EWDS Instruction Timing (8)(9)



5052 FHD F06

Figure 6. ERAL Instruction Timing (8)



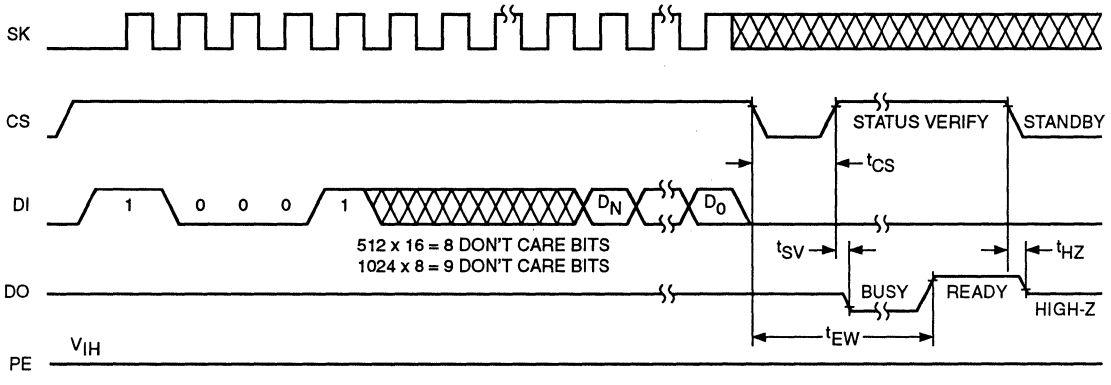
5052 FHD F08

Note:
(8) The ORG pin is used to configure the device for x8 or x16 operation.
(9) PE = "Don't Care".

Write All

Upon receiving a WRAL command and data, the CS (chip select) pin must be deselected for a minimum of 500ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C108/CAT33C108I can be determined by selecting the device and polling the DO pin. It IS NOT necessary for all memory locations to be cleared before the WRAL command is executed. The Write All instruction requires that PE = 1.

Figure 7. WRAL Instruction Timing (8)



5052 FHD F09

Note:
(8) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, DN = D7. When x16 organization is selected, DN = D15.

CAT35C108/CAT35C108I

8K-Bit SERIAL E²PROM

FEATURES

- High Speed Operation: 3MHz
- Low Power CMOS Technology
- Single 5V Supply
- 512 x 16 or 1024 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- Sequential Read
- Program Enable (PE) Pin
- Fast Nonvolatile Write Cycle: 5ms Max
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

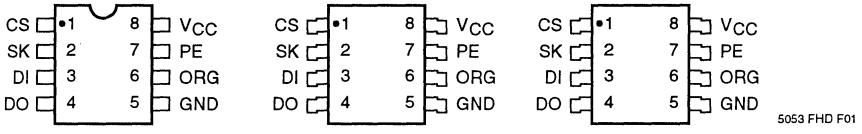
DESCRIPTION

The CAT35C108 and CAT35C108I are 8K bit Serial E²PROM memory devices which can be configured as either 512 registers by 16 bits (ORG pin at V_{CC}) or 1024 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin.

The CAT35C108/CAT35C108I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION

DIP Package / **SO Package S** / **SO Package K**

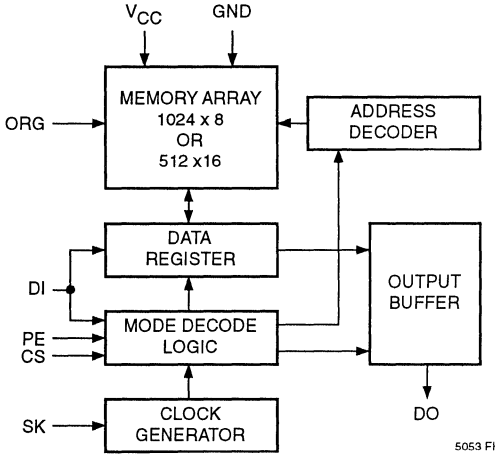


PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+5V Power Supply
GND	Ground
PE	Program Enable
ORG	Memory Organization

Note: When the ORG pin is connected to V_{CC}, the 512 x 16 organization is selected. When it is connected to ground, the 1024 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 512 x 16 organization.

BLOCK DIAGRAM



TD 5053

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT35C108 T_A= 0°C to +70°C, V_{CC} = +5V±10%, unless otherwise specified.
CAT35C108I T_A= –40°C to +85°C, V_{CC} = +5V±10%, unless otherwise specified.

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
I_{CC1}	Power Supply Current (Operating)	Comm.			3	mA	DI = 0.0V, SK = 5.0V V_{CC} = 5.0V, CS = 5.0V, Output Open
		Ind.			4	mA	
I_{CC2}	Power Supply Current (Standby)				10	µA	V_{CC} = 5.5V, CS = 0V DI = 0V SK = 0V
I_{LI}(5)	Input Leakage Current				1	µA	V_{IN} = 0V to 5.5V
I_{LO}(5)	Output Leakage Current				1	µA	V_{OUT} = 0V to 5.5V, CS = 0V
V_{IH}	High Level Input Voltage		2.0		V_{CC} + 1	V	
V_{IL}	Low Level Input Voltage		–0.1		0.8	V	
V_{OH}	High Level Output Voltage		2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage				0.4	V	I_{OL} = 2.1mA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) PE and ORG pin leakage current (I_{LI} and I_{LO}) = 15 µA max. (at V_{IL}), 10 µA otherwise.

INSTRUCTION SET(6)

Instruction	Start Bit	Opcode	Address		Data		PE	Comments
			1024 x 8	512 x 16	1024 x 8	512 x 16		
READ	1	1 0	XA9–A0	XA8–A0			X	Start Address AN–A0
ERASE	1	1 1	XA9–A0	XA8–A0			1	Clear Address AN–A0
WRITE	1	0 1	XA9–A0	XA8–A0	D7–D0	D15–D0	1	Write Address AN–A0
EWEN	1	0 0	11XXXXXXXXX	11XXXXXXXX			X	Write Enable
EWDS	1	0 0	00XXXXXXXXX	00XXXXXXXX			X	Write Disable
ERAL	1	0 0	10XXXXXXXXX	10XXXXXXXX			1	Clear All Addresses
WRAL	1	0 0	01XXXXXXXXX	01XXXXXXXX	D7–D0	D15–D0	1	Write All Addresses

3

A.C. CHARACTERISTICS

CAT35C108 T_A= 0°C to +70°C, V_{CC} = +5V±10%, unless otherwise specified.
CAT35C108I T_A= –40°C to +85°C, V_{CC} = +5V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	50			ns	
t_{CSH}	CS Hold Time	0			ns	
t_{DIS}	DI Setup Time	50			ns	C_L = 100pF
t_{DIH}	DI Hold Time	50			ns	V_{OL} = 0.3V, V_{OH} = V_{CC} – 0.3
t_{PD1}	Output Delay to 1			100	ns	V_{IL} = 0.3V, V_{IH} = V_{CC} – 0.3
t_{PD0}	Output Delay to 0			100	ns	
t_{HZ}(3)	Output Delay to High-Z			100	ns	
t_{EW}(7)	Program/Erase Pulse Width			5	ms	
t_{CSMIN}	Minimum CS Low Time	100			ns	
t_{SKHI}	Minimum SK High Time	100			ns	
t_{SKLOW}	Minimum SK Low time	100			ns	
t_{SV}	Output Delay to Status Valid			100	ns	C_L = 100pF
SK_{MAX}	Maximum Clock Frequency	DC		3	MHz	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(6) X indicates a "Don't Care" input (either 0 or 1).
(7) ERAL and WRAL instructions = 10 ms max.

DEVICE OPERATION

The CAT35C108/CAT35C108I is a 8192 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT35C108/CAT35C108I can be organized as either 512 registers by 16 bits, or as 1024 registers by 8 bits. Seven 13 bit instructions (14 bit instruction in 1024 by 8 organization) control the reading, writing and erase operations of the device. The CAT35C108/CAT35C108I operates on a single 5V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the CAT35C108/CAT35C108I is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 9 bit address (10 bit address when organized as 1024 x 8), and for write operations a 16 bit data field (8 bit data field when organized as 1024 x 8). All program/erase cycles are enabled only when pin 7 (PE) is held high.

Figure 1. Sychronous Data Timing (8)

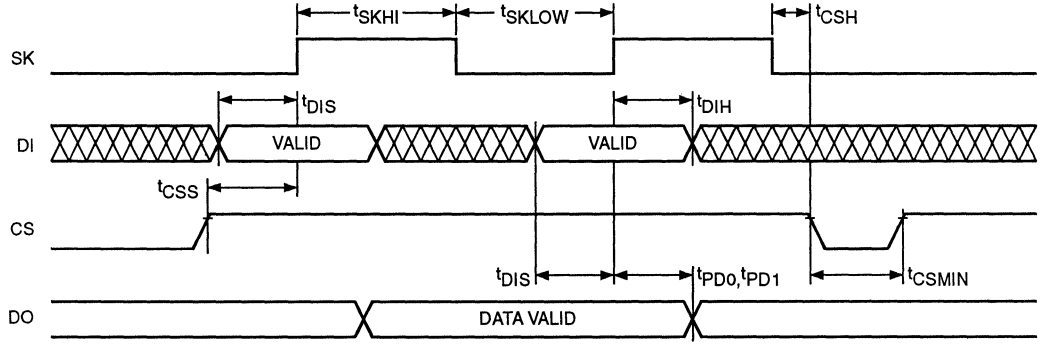
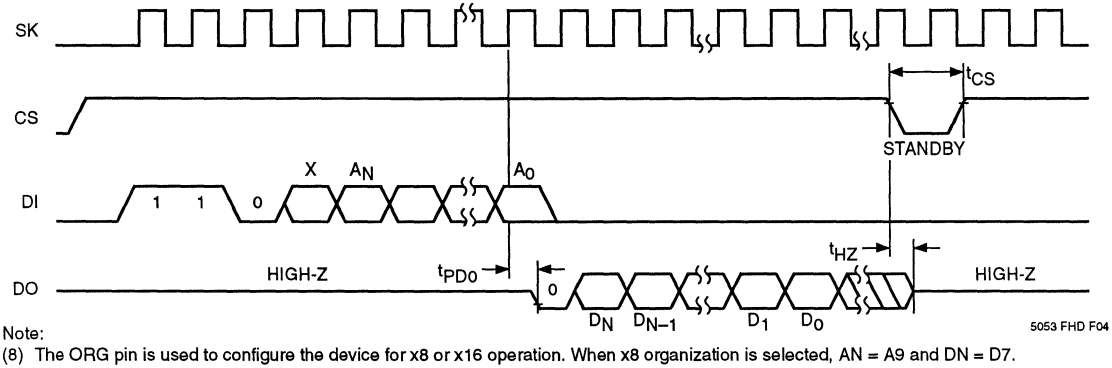


Figure 2. Read Instruction Timing (8)(9)



Note:
(8) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A9 and DN = D7. When x16 organization is selected, AN = A8 and DN = D15.
(9) PE = "Don't Care".

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT35C108/CAT35C108I will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}). The data output is sequential with the data from address N followed by the data from address N+1. The data output continues to the highest address and will wrap around to the first address if the clock continues to run. Bringing CS low at any time will stop the data output . The dummy bit is suppressed in the sequential read mode (except for the very first address) and a continuous stream of data results.

Write

After receiving a WRITE command, address and the data, the CS (chip select) pin must be deselected for a minimum of 100ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C108/CAT35C108I can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent. The Write instruction requires that PE = 1.

Figure 3. Write Instruction Timing (8)

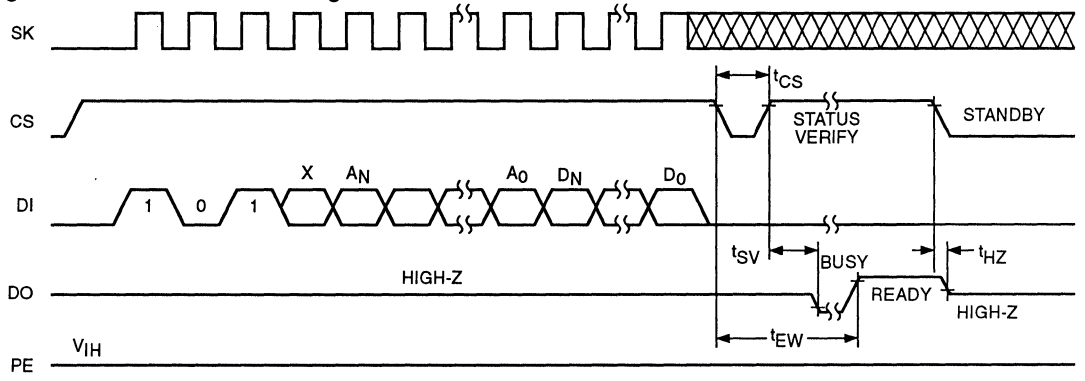
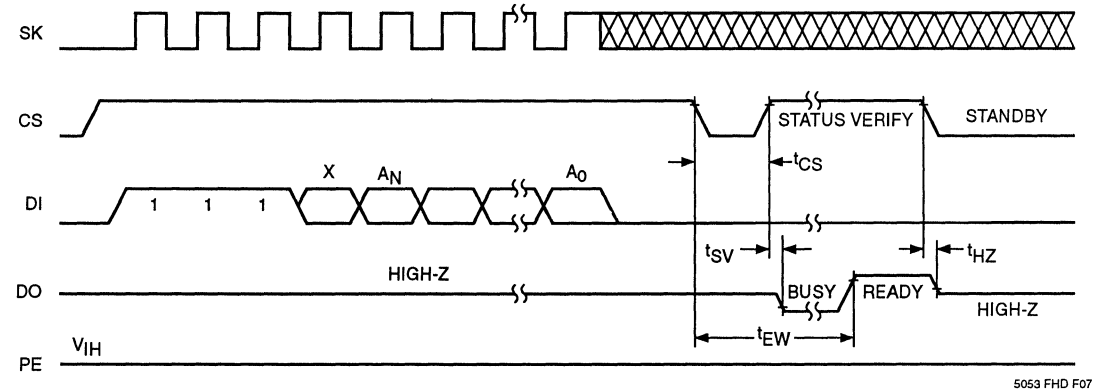


Figure 4. Erase Instruction Timing (8)



Note:
(8) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A9 and DN = D7. When x16 organization is selected, AN = A8 and DN = D15.

Erase

Upon receiving an ERASE command and address, the CS (chip select) pin must be deselected for a minimum of 100ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C108/CAT35C108I can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state. The Erase instruction requires that PE = 1.

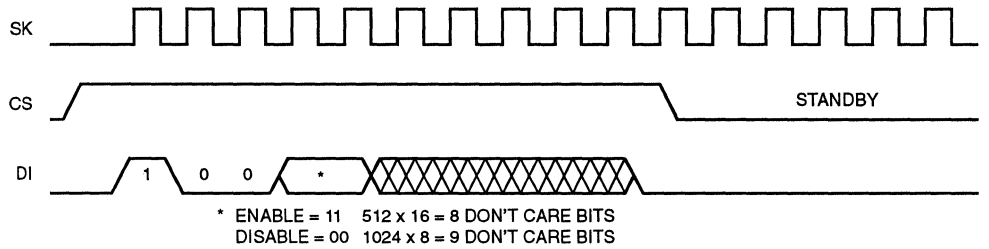
Erase/Write Enable and Disable

The CAT35C108/CAT35C108I powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT35C108/CAT35C108I write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

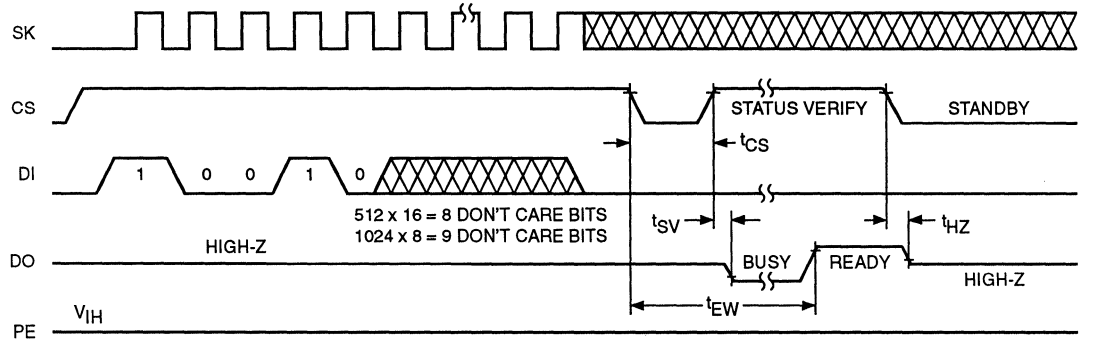
Upon receiving an ERAL command, the CS (chip select) pin must be deselected for a minimum of 100ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C108/CAT35C108I can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state. The Erase All instruction requires that PE = 1.

Figure 5. EWEN/EWDS Instruction Timing (8)(9)



5052 FHD F06

Figure 6. ERAL Instruction Timing (8)



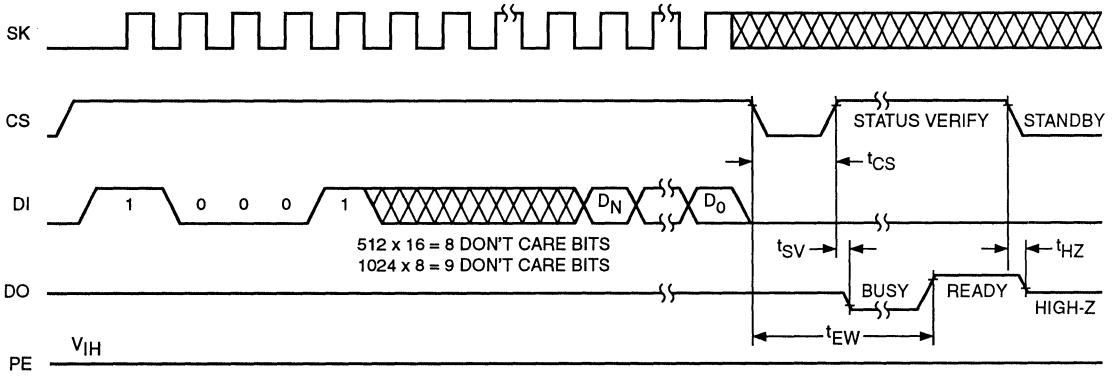
5052 FHD F08

Note:
(8) The ORG pin is used to configure the device for x8 or x16 operation.
(9) PE = "Don't Care".

Write All

Upon receiving a WRAL command and data, the CS (chip select) pin must be deselected for a minimum of 100ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C108/CAT35C108I can be determined by selecting the device and polling the DO pin. It IS NOT necessary for all memory locations to be cleared before the WRAL command is executed. The Write All instruction requires that PE = 1.

Figure 7. WRAL Instruction Timing (8)



5053 FHD F09

Note:
(8) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, DN = D7. When x16 organization is selected, DN = D15.

CAT33C116/CAT33C116I

16K-Bit SERIAL E²PROM

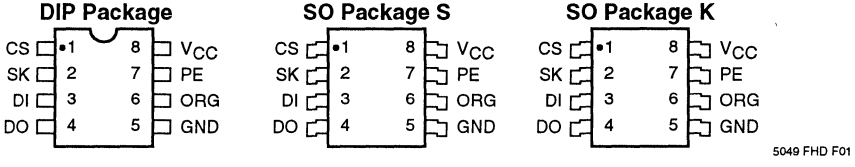
FEATURES

- High Speed Operation: 1MHz
- Low Power CMOS Technology
- Single 3V Supply
- 1024 x 16 or 2048 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- Sequential Read
- Program Enable (PE) Pin
- Fast Nonvolatile Write Cycle: 5ms Max
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

DESCRIPTION

The CAT33C116 and CAT33C116I are 16K bit Serial E²PROM memory devices which can be configured as either 1024 registers by 16 bits (ORG pin at V_{CC}) or 2048 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT33C116/CAT33C116I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION



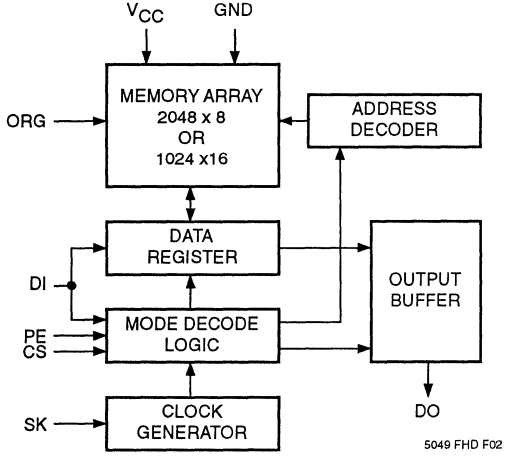
5049 FHD F01

PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+5V Power Supply
GND	Ground
PE	Program Enable
ORG	Memory Organization

Note: When the ORG pin is connected to V_{CC}, the 1024 x 16 organization is selected. When it is connected to ground, the 2048 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 1024 x 16 organization.

BLOCK DIAGRAM



5049 FHD F02

TD 5049

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT33C116 T_A= 0°C to +70°C, V_{CC} = +3V±10%, unless otherwise specified.
CAT33C116I T_A= –40°C to +85°C, V_{CC} = +3V±10%, unless otherwise specified.

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
I_{CC1}	Power Supply Current (Operating)	Comm.			2	mA	DI = 0.0V, SK = 3.0V V_{CC} = 3.0V, CS = 3.0V, Output Open
		Ind.			3	mA	
I_{CC2}	Power Supply Current (Standby)				10	µA	V_{CC} = 3.3V, CS = 0V DI = 0V SK = 0V
I_{LI}(5)	Input Leakage Current				1	µA	V_{IN} = 0V to 3.3V
I_{LO}(5)	Output Leakage Current				1	µA	V_{OUT} = 0V to 3.3V, CS = 0V
V_{IH}	High Level Input Voltage		V_{CC} – 0.3		V_{CC} + 1	V	
V_{IL}	Low Level Input Voltage		–0.1		0.3	V	
V_{OH}	High Level Output Voltage		V_{CC} – 0.3			V	I_{OH} = –10µA
V_{OL}	Low Level Output Voltage				0.3	V	I_{OL} = 10µA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) PE and ORG pin leakage current (I_{LI} and I_{LO}) = 10 µA max.

INSTRUCTION SET (6)

Inst.	Start Bit	Opcode	Address		Data		PE	Comments
			2048 x 8	1024 x 16	2048 x 8	1024 x 16		
READ	1	1 0	A10–A0	A9–A0			X	Start Address AN–A0
ERASE	1	1 1	A10–A0	A9–A0			1	Clear Address AN–A0
WRITE	1	0 1	A10–A0	A9–A0	D7–D0	D15–D0	1	Write Address AN–A0
EWEN	1	0 0	11XXXXXXXXX	11XXXXXXXX			X	Write Enable
EWDS	1	0 0	00XXXXXXXXX	00XXXXXXXX			X	Write Disable
ERAL	1	0 0	10XXXXXXXXX	10XXXXXXXX			1	Clear All Addresses
WRAL	1	0 0	01XXXXXXXXX	01XXXXXXXX	D7–D0	D15–D0	1	Write All Addresses

3

A.C. CHARACTERISTICS

CAT33C116 T_A= 0°C to +70°C, V_{CC} = +3V±10%, unless otherwise specified.
CAT33C116I T_A= –40°C to +85°C, V_{CC} = +3V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	250			ns	
t_{CSH}	CS Hold Time	0			ns	C_L=100pF
t_{DIS}	DI Setup Time	250			ns	V_{OL} = 0.3V,
t_{DIH}	DI Hold Time	250			ns	V_{OH} = V_{CC} – 0.3
t_{PD1}	Output Delay to 1			500	ns	V_{IL} = 0.3V,
t_{PD0}	Output Delay to 0			500	ns	V_{IH} = V_{CC} – 0.3
t_{HZ}(3)	Output Delay to High-Z			500	ns	
t_{EW}(7)	Program/Erase Pulse Width			5	ms	
t_{CSMIN}	Minimum CS Low Time	500			ns	
t_{SKHI}	Minimum SK High Time	500			ns	
t_{SKLOW}	Minimum SK Low time	500			ns	
t_{SV}	Output Delay to Status Valid			500	ns	C_L = 100pF
SK_{MAX}	Maximum Clock Frequency	DC		1	MHz	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(6) X indicates a "Don't Care" input (either 0 or 1).
(7) ERAL and WRAL instructions = 10 ms max.

DEVICE OPERATION

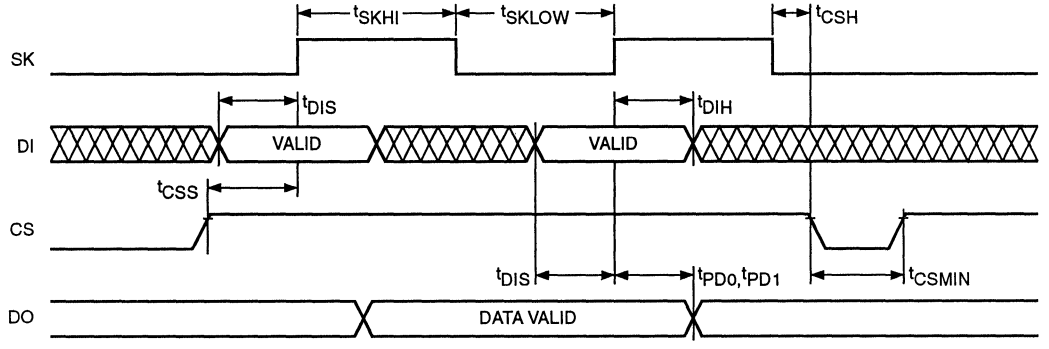
The CAT33C116/CAT33C116I is a 16,384 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT33C116/CAT33C116I can be organized as either 1024 registers by 16 bits, or as 2048 registers by 8 bits. Seven 13 bit instructions (14 bit instruction in 2048 by 8 organization) control the reading, writing and erase operations of the device. The CAT33C116/CAT33C116I operates on a single 3V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

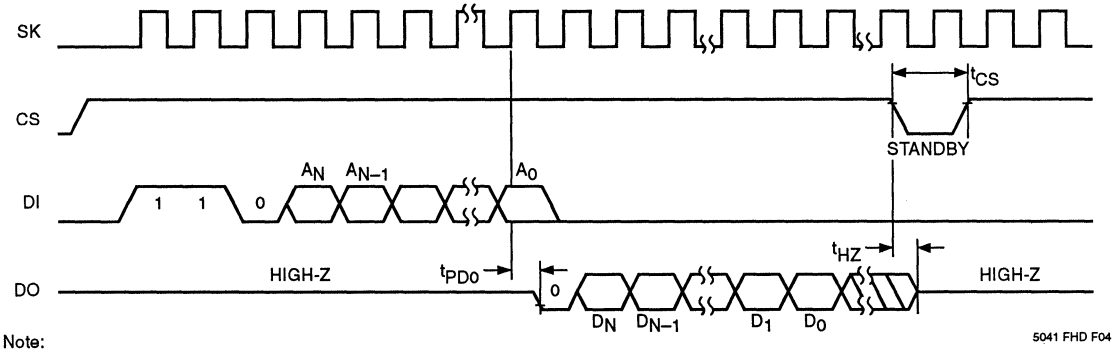
The format for all instructions sent to the CAT33C116/CAT33C116I is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 10 bit address (11 bit address when organized as 2048 x 8), and for write operations a 16 bit data field

Figure 1. Sychronous Data Timing (8)



5041 FHD F03

Figure 2. Read Instruction Timing (8) (9)



5041 FHD F04

Note:

(8) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A10 and DN = D7. When x16 organization is selected, AN = A9 and DN = D15.

(9) PE = "Don't Care".

(8 bit data field when organized as 2048 x 8). All program/erase cycles are enabled only when pin 7 (PE) is held high.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT33C116/CAT33C116I will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}). The data output is sequential with the data from address N followed by the data from address N+1. The data output continues to the highest address and will wrap around to the first address if the clock continues to run. Bringing CS low at any time will stop the data output. The dummy bit is suppressed in the sequential read mode (except for the very first address) and a continuous stream of data results.

Write

After receiving a WRITE command, address and the data, the CS (chip select) pin must be deselected for a minimum of 500ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C116/CAT33C116I can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent. The Write instruction requires that PE = 1.

3

Figure 3. Write Instruction Timing (8)

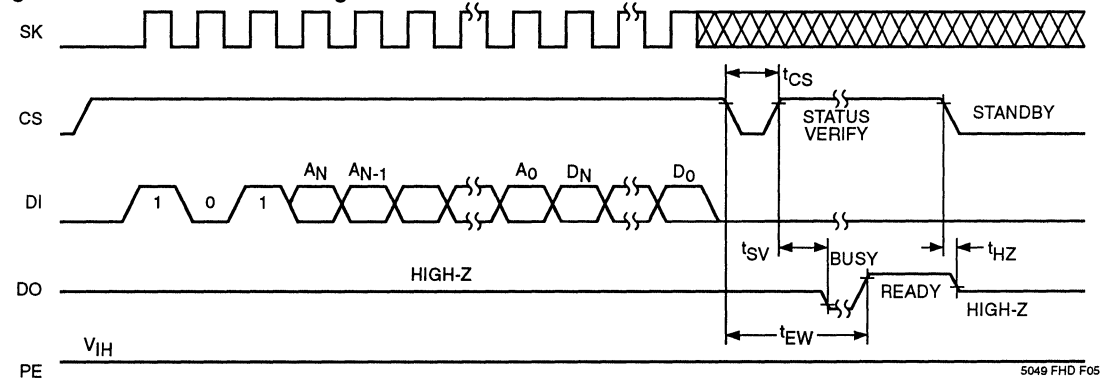
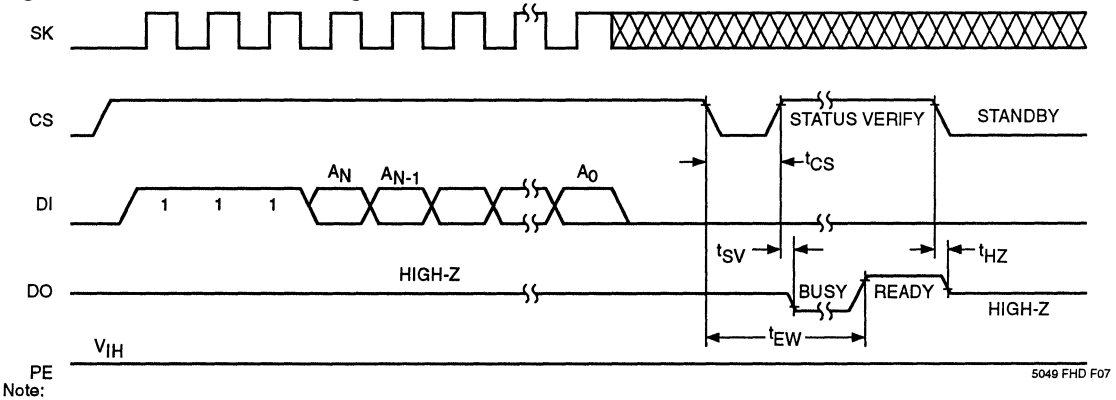


Figure 4. Erase Instruction Timing (8)



Note:
(8) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A10 and DN = D7. When x16 organization is selected, AN = A9 and DN = D15.

Erase

Upon receiving an ERASE command and address, the CS (chip select) pin must be deselected for a minimum of 500ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C116/CAT33C116I can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state. The Erase instruction requires that PE = 1.

Erase/Write Enable and Disable

The CAT33C116/CAT33C116I powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT33C116/CAT33C116I write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (chip select) pin must be deselected for a minimum of 500ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C116/CAT33C116I can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state. The Erase All instruction requires that PE = 1.

Figure 5. EWEN/EWDS Instruction Timing (8) (9)

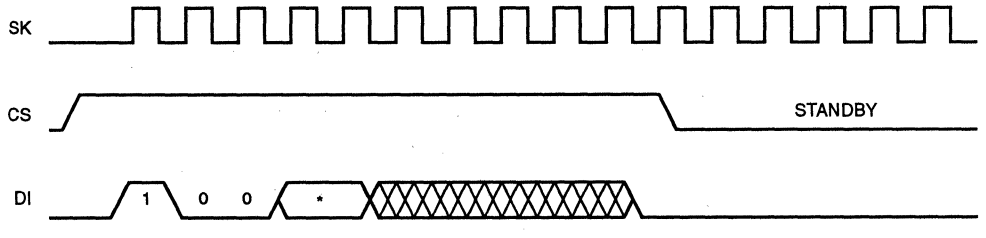
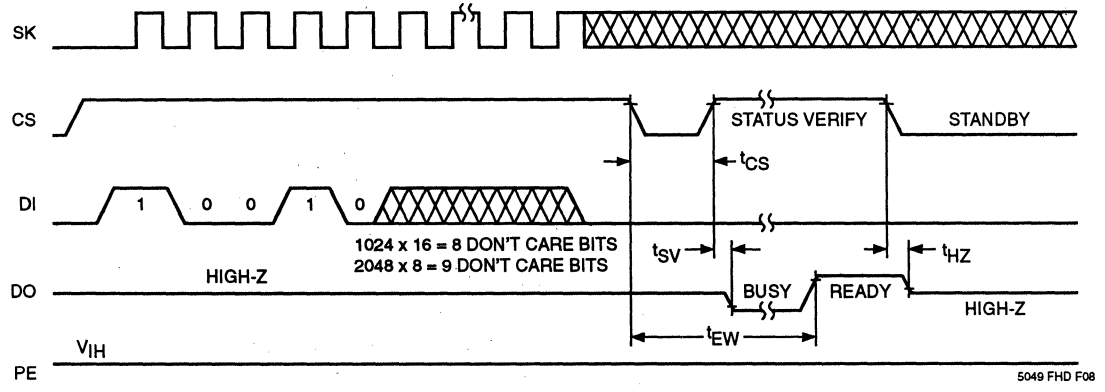


Figure 6. ERAL Instruction Timing (8)

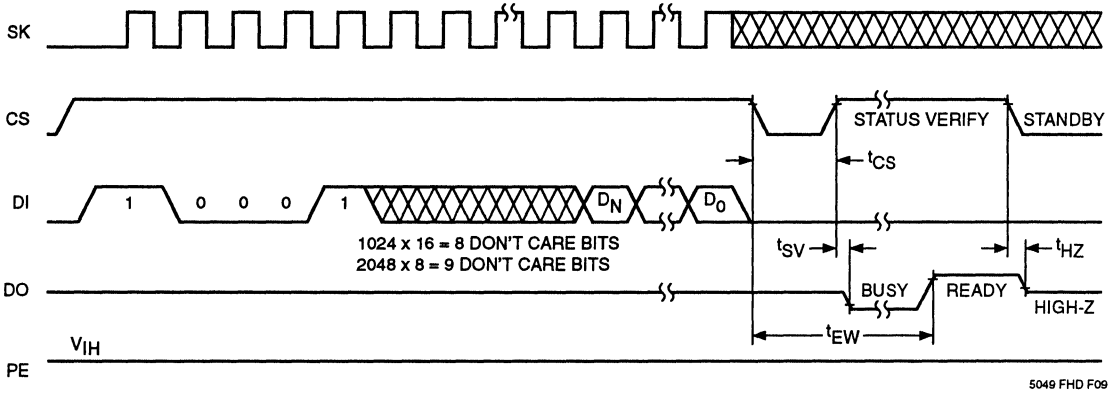


Note:
(8) The ORG pin is used to configure the device for x8 or x16 operation.
(9) PE = "Don't Care".

Write All

Upon receiving a WRAL command and data, the CS (chip select) pin must be deselected for a minimum of 500ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C116/CAT33C116I can be determined by selecting the device and polling the DO pin. It IS NOT necessary for all memory locations to be cleared before the WRAL command is executed. The Write All instruction requires that PE = 1.

Figure 7. WRAL Instruction Timing (8)



Note:
(8) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, DN = D7. When x16 organization is selected, DN = D15.

CAT35C116/CAT35C116I

16K-Bit SERIAL E²PROM

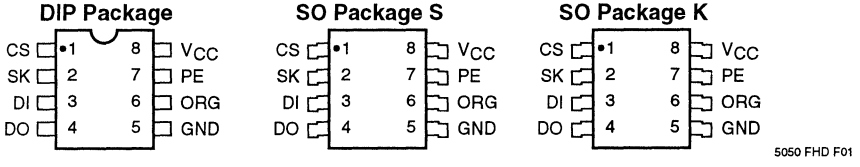
FEATURES

- High Speed Operation: 3MHz
- Low Power CMOS Technology
- Single 5V Supply
- 1024 x 16 or 2048 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- Sequential Read
- Program Enable (PE) Pin
- Fast Nonvolatile Write Cycle: 5ms Max
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

DESCRIPTION

The CAT35C116 and CAT35C116I are 16K bit Serial E²PROM memory devices which can be configured as either 1024 registers by 16 bits (ORG pin at V_{CC}) or 2048 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C116/CAT35C116I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION

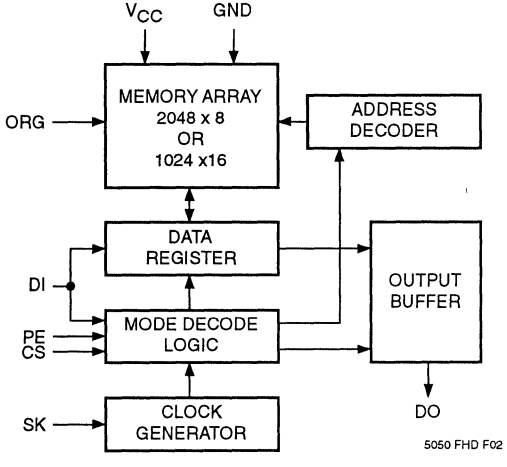


PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+5V Power Supply
GND	Ground
PE	Program Enable
ORG	Memory Organization

Note: When the ORG pin is connected to V_{CC}, the 1024 x 16 organization is selected. When it is connected to ground, the 2048 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 1024 x 16 organization.

BLOCK DIAGRAM



TD 5050

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT35C116 T_A= 0°C to +70°C, V_{CC} = +5V±10%, unless otherwise specified.
CAT35C116I T_A= –40°C to +85°C, V_{CC} = +5V±10%, unless otherwise specified.

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
I_{CC1}	Power Supply Current (Operating)	Comm.			3	mA	DI = 0.0V, SK = 5.0V V_{CC} = 5.0V, CS = 5.0V, Output Open
		Ind.			4	mA	
I_{CC2}	Power Supply Current (Standby)				10	µA	V_{CC} = 5.5V, CS = 0V DI = 0V SK = 0V
I_{LI}(5)	Input Leakage Current				1	µA	V_{IN} = 0V to 5.5V
I_{LO}(5)	Output Leakage Current				1	µA	V_{OUT} = 0V to 5.5V, CS = 0V
V_{IH}	High Level Input Voltage		2.0		V_{CC} + 1	V	
V_{IL}	Low Level Input Voltage		–0.1		0.8	V	
V_{OH}	High Level Output Voltage		2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage				0.4	V	I_{OL} = 2.1mA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) PE and ORG pin leakage current (I_{LI} and I_{LO}) = 15 µA max. (at V_{IL}), 10 µA otherwise.

INSTRUCTION SET (6)

Inst.	Start Bit	Opcode	Address		Data		PE	Comments
			2048 x 8	1024 x 16	2048 x 8	1024 x 16		
READ	1	1 0	A10–A0	A9–A0			X	Start Address AN–A0
ERASE	1	1 1	A10–A0	A9–A0			1	Clear Address AN–A0
WRITE	1	0 1	A10–A0	A9–A0	D7–D0	D15–D0	1	Write Address AN–A0
EWEN	1	0 0	11XXXXXXXXX	11XXXXXXXX			X	Write Enable
EWDS	1	0 0	00XXXXXXXXX	00XXXXXXXX			X	Write Disable
ERAL	1	0 0	10XXXXXXXXX	10XXXXXXXX			1	Clear All Addresses
WRAL	1	0 0	01XXXXXXXXX	01XXXXXXXX	D7–D0	D15–D0	1	Write All Addresses

3

A.C. CHARACTERISTICS

CAT35C116 T_A= 0°C to +70°C, V_{CC} = +5V±10%, unless otherwise specified.
CAT35C116I T_A= –40°C to +85°C, V_{CC} = +5V±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	50			ns	
t_{CSH}	CS Hold Time	0			ns	
t_{DIS}	DI Setup Time	50			ns	C_L=100pF
t_{DIH}	DI Hold Time	50			ns	V_{OL} = 0.8V, V_{OH} = 2.0V
t_{PD1}	Output Delay to 1			100	ns	V_{IL} = 0.45V, V_{IH} = 2.4V
t_{PD0}	Output Delay to 0			100	ns	
t_{HZ}(3)	Output Delay to High-Z			100	ns	
t_{EW}(7)	Program/Erase Pulse Width			5	ms	
t_{CSMIN}	Minimum CS Low Time	100			ns	
t_{SKHI}	Minimum SK High Time	100			ns	
t_{SKLOW}	Minimum SK Low time	100			ns	
t_{SV}	Output Delay to Status Valid			100	ns	C_L = 100pF
SK_{MAX}	Maximum Clock Frequency	DC		3	MHz	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(6) X indicates a "Don't Care" input (either 0 or 1).
(7) ERAL and WRAL instructions = 10 ms max.

DEVICE OPERATION

The CAT35C116/CAT35C116I is a 16,384 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT35C116/CAT35C116I can be organized as either 1024 registers by 16 bits, or as 2048 registers by 8 bits. Seven 13 bit instructions (14 bit instruction in 2048 by 8 organization) control the reading, writing and erase operations of the device. The CAT35C116/CAT35C116I operates on a single 5V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the CAT35C116/CAT35C116I is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 10 bit address (11 bit address when organized as 2048 x 8), and for write operations a 16 bit data field

Figure 1. Sychronous Data Timing (8)

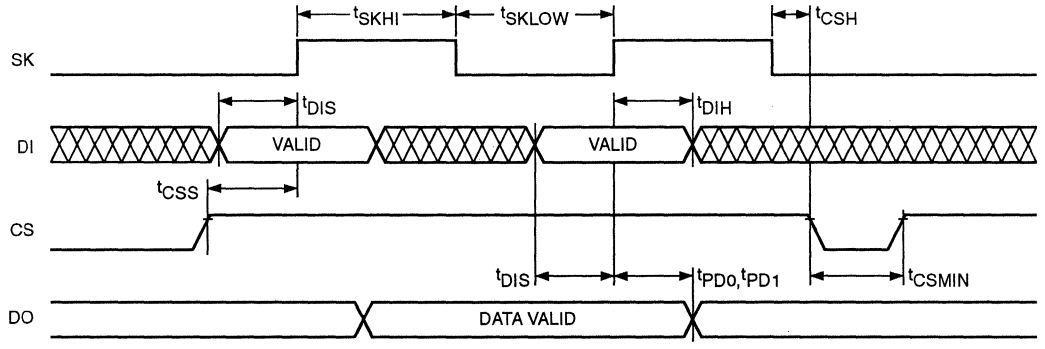


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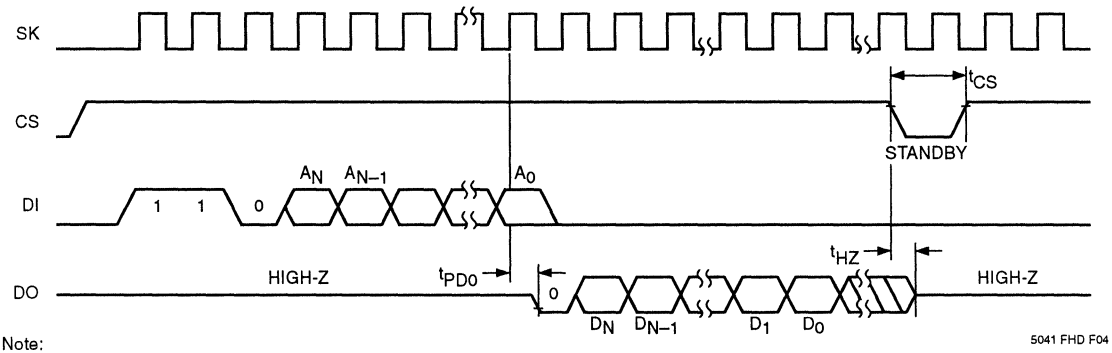
Figure 2. Read Instruction Timing (8) (9)



5041 FHD F04

Note:

(8) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A10 and DN = D7. When x16 organization is selected, AN = A9 and DN = D15.

(9) PE = "Don't Care".

(8 bit data field when organized as 2048 x 8). All program/erase cycles are enabled only when pin 7 (PE) is held high.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT35C116/CAT35C116I will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}). The data output is sequential with the data from address N followed by the data from address N+1. The data output continues to the highest address and will wrap around to the first address if the clock continues to run. Bringing CS low at any time will stop the data output. The dummy bit is suppressed in the sequential read mode (except for the very first address) and a continuous stream of data results.

Write

After receiving a WRITE command, address and the data, the CS (chip select) pin must be deselected for a minimum of 100ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C116/CAT35C116I can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent. The Write instruction requires that PE = 1.

3

Figure 3. Write Instruction Timing (8)

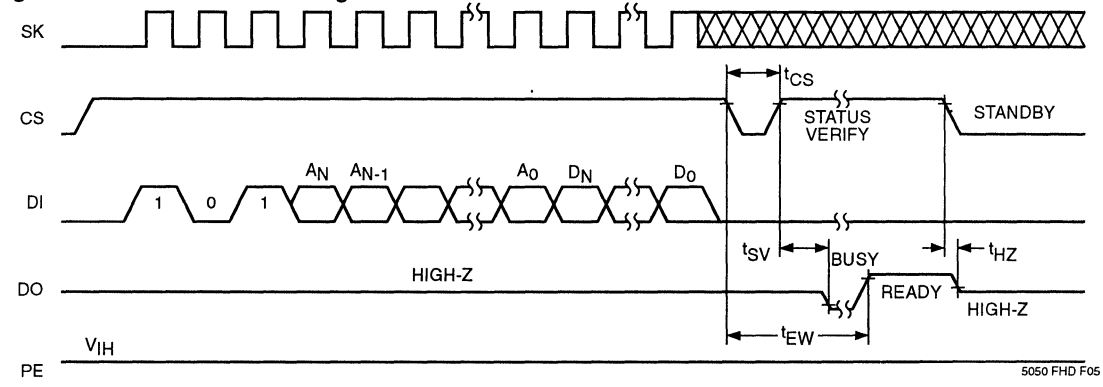
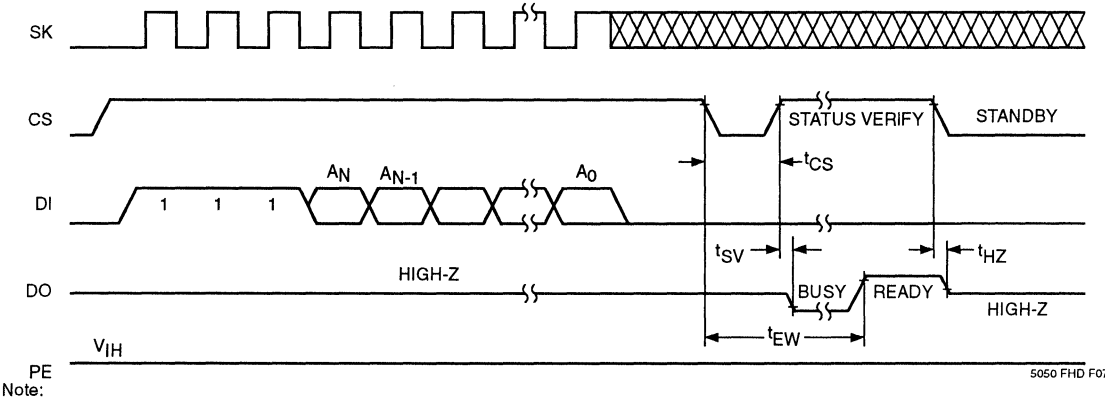


Figure 4. Erase Instruction Timing (8)



Note:
(8) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A10 and DN = D7. When x16 organization is selected, AN = A9 and DN = D15.

Erase

Upon receiving an ERASE command and address, the CS (chip select) pin must be deselected for a minimum of 100ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C116/CAT35C116I can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state. The Erase instruction requires that PE = 1.

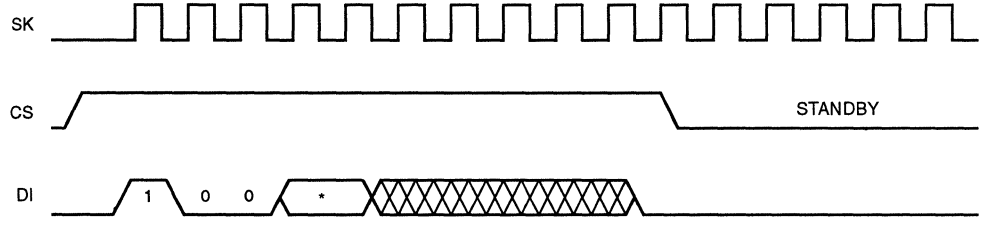
Erase/Write Enable and Disable

The CAT35C116/CAT35C116I powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT35C116/CAT35C116I write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (chip select) pin must be deselected for a minimum of 100ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C116/CAT35C116I can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state. The Erase All instruction requires that PE = 1.

Figure 5. EWEN/EWDS Instruction Timing (8) (9)



* ENABLE = 11 1024 x 16 = 8 DON'T CARE BITS
DISABLE = 00 2048 x 8 = 9 DON'T CARE BITS

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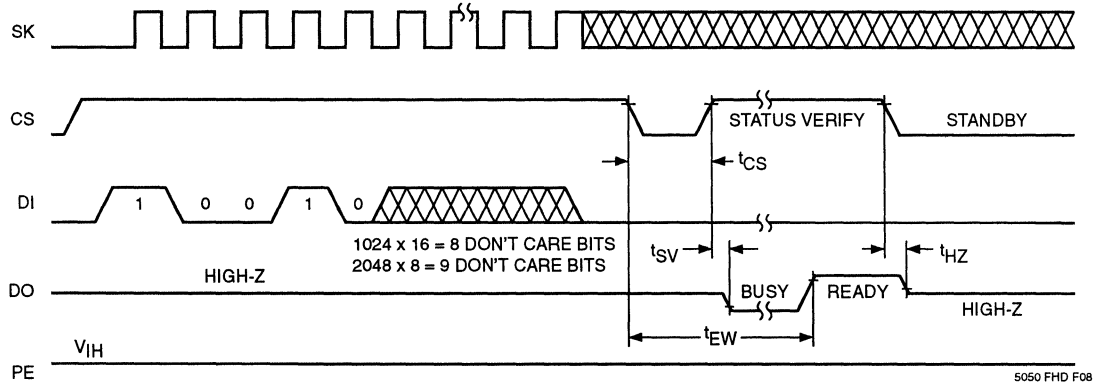
Figure 6. ERAL Instruction Timing (8)



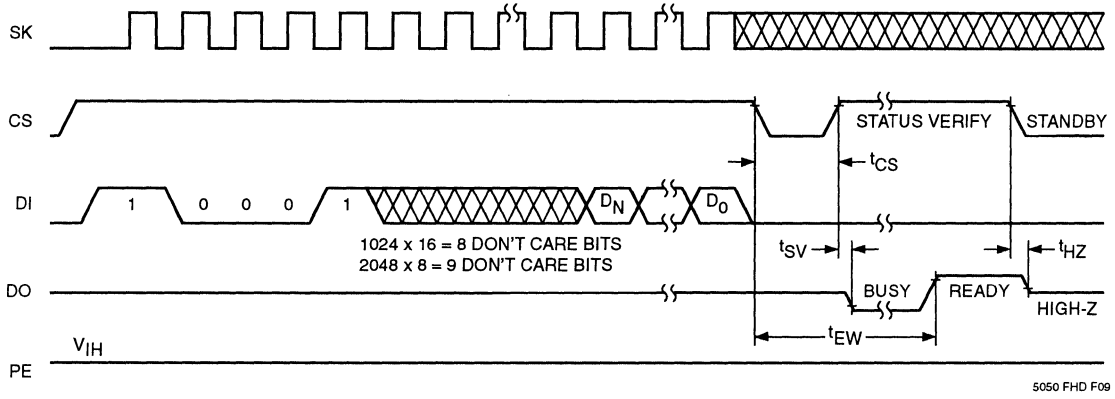
5050 FHD F08

Note:
(8) The ORG pin is used to configure the device for x8 or x16 operation.
(9) PE = "Don't Care".

Write All

Upon receiving a WRAL command and data, the CS (chip select) pin must be deselected for a minimum of 100ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C116/CAT35C116I can be determined by selecting the device and polling the DO pin. It IS NOT necessary for all memory locations to be cleared before the WRAL command is executed. The Write All instruction requires that PE = 1.

Figure 7. WRAL Instruction Timing (8)



Note:
(8) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, DN = D7. When x16 organization is selected, DN = D15.

CATALYST SEMICONDUCTOR

Product Information 1

2-Wire Bus Serial E^2PROMs 2

3-Wire Bus Serial E^2PROMs 3

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SECTION 4 SPI BUS SERIAL E^2PROMS

CAT64LC10/CAT64LC10I ..... 64 x 16 ..... 1K-Bit 4-1

CAT64LC20/CAT64LC20I ..... 128 x 16 ..... 2K-Bit 4-11

CAT64LC40/CAT64LC40I ..... 256 x 16 ..... 4K-Bit 4-21

CAT64LC10/CAT64LC10I

1K-Bit SERIAL E²PROM

FEATURES

- SPI Bus Compatible
- Low Power CMOS Technology
- 2.5V to 5.5V Operation
- Self-Timed Write Cycle with Auto-Clear
- Hardware Reset Pin
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- RDY/$\overline{\text{BUSY}}$ Pin for End-of-Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- ZERO Power™ (CAT64LC10Z) Version Available
- Optional High Endurance Device Available

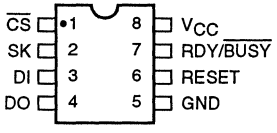
4

DESCRIPTION

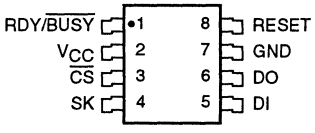
The CAT64LC10 and CAT64LC10I are 1K bit Serial E²PROM memory devices which are configured as 64 registers by 16 bits. Each register can be written (or read) serially by using the DI (or DO) pin. The CAT64LC10/CAT64LC10I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION

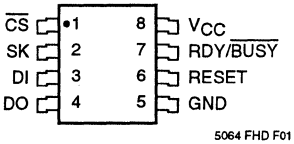
DIP Package



SO Package J



SO Package S

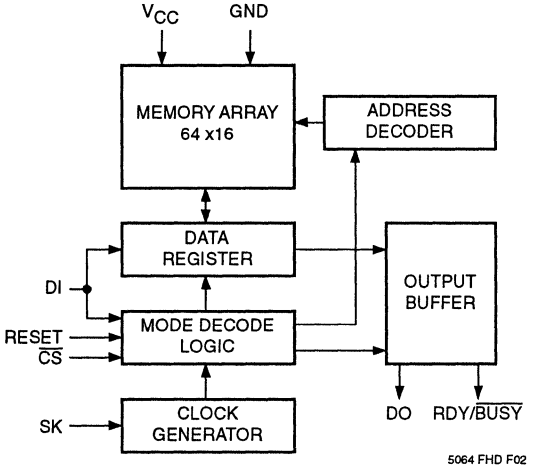


5064 FHD F01

PIN FUNCTIONS

Pin Name	Function
$\overline{CS}$	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+2.5V to +5.5V Power Supply
GND	Ground
RESET	Reset
RDY/$\overline{BUSY}$	Ready/$\overline{BUSY}$ Status

BLOCK DIAGRAM



5064 FHD F02

TD 5064

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE (T_A = 25°C, f= 1.0 MHz, V_{CC} = 5.5V)

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (DO, RDY/$\overline{BUSY}$)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance ($\overline{CS}$, SK, DI, RESET)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

CAT64LC10 T_A= 0°C to +70°C, V_{CC} = +2.5V to +5.5V, unless otherwise specified.
CAT64LC10I T_A= –40°C to +85°C, V_{CC} = +2.5V to +5.5V, unless otherwise specified.

Sym.	Parameter		Limits Min.	Typ.	Max.	Units	Test Conditions
I_{CC}	Operating Current	2.5V			0.4	mA	f_{SK} = 250 kHz
	EWEN, EWDS, READ	5.5V			1.0		f_{SK} = 1 MHz
I_{CCP}	Program Current	2.5V			2.0	mA	
		5.5V			3.0		
I_{SB}	Standby Current	Standard			3.0	µA	V_{IN} = GND or V_{CC}
I_{SBZ}(5)		ZERO Pwr™			0		$\overline{CS}$ = V_{CC}
I_{LI}	Input Leakage Current				2.0	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current				10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Low Level Input Voltage, DI		–0.1		V_{CC} x 0.3	V	
V_{IH}	High Level Input Voltage, DI		V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{IL}	Low Level Input Voltage, $\overline{CS}$, SK, RESET		–0.1		V_{CC} x 0.2	V	
V_{IH}	High Level Input Voltage, $\overline{CS}$, SK, RESET		V_{CC} x 0.8		V_{CC} + 0.5	V	
V_{OH}	High Level Output Voltage	2.5V	V_{CC} – 0.3			V	I_{OH} = –10µA
		4.5V	V_{CC} – 0.3				I_{OH} = –10µA
			2.4				I_{OH} = –400µA
V_{OL}	Low Level Output Voltage	2.5V			0.4	V	I_{OL} = 10µA
		4.5V					I_{OL} = 2.1mA

Note:
(5) Standby Current (I_{SBZ}) = 0µA (<900nA)

A.C. OPERATING CHARACTERISTICS

CAT64LC10 T_A= 0°C to +70°C, V_{CC} = +2.5V to +5.5V, unless otherwise specified.
CAT64LC10I T_A= –40°C to +85°C, V_{CC} = +2.5V to +5.5V, unless otherwise specified.

Symbol	Parameter		Limits Min.	Typ.	Max.	Units
t_{CSS}	$\overline{CS}$ Setup Time		100			ns
t_{CSH}	$\overline{CS}$ Hold Time		100			ns
t_{DIS}	DI Setup Time		200			ns
t_{DIH}	DI Hold Time		200			ns
t_{PD1}	Output Delay to 1				300	ns
t_{PD0}	Output Delay to 0				300	ns
t_{HZ}(6)	Output Delay to High Impendance				500	ns
t_{CSMIN}	Minimum $\overline{CS}$ High Time		250			ns
t_{SKHI}	Minimum SK High Time	2.5V	1000			ns
		4.5V–5.5V	400			
t_{SKLOW}	Minimum SK Low Time	2.5V	1000			ns
		4.5V–5.5V	400			
t_{SV}	Output Delay to Status Valid				500	ns
f_{SK}	Maximum Clock Frequency	2.5V	250			kHz
		4.5V–5.5V	1000			
t_{RESS}	Reset to $\overline{CS}$ Setup Time		0			ns
t_{RESMIN}	Minimum RESET High Time		250			ns
t_{RESH}	RESET to READY Hold Time		0			ns
t_{RC}	Write Recovery		100			ns

POWER-UP TIMING(3)(7)

Symbol	Parameter	Min.	Max.	Units
t_{PUR}	Power-Up to Read Operation		10	µs
t_{PUW}	Power-Up to Program Operation		1	ms

WRITE CYCLE LIMIITS

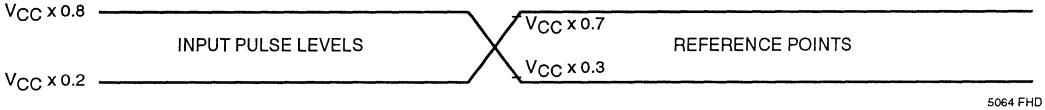
Symbol	Parameter		Min.	Max.	Units
t_{WR}	Program Cycle Time	2.5V		10	ms
		4.5V–5.5V		5	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(6) This parameter is sampled but not 100% tested.
(7) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

INSTRUCTION SET

Instruction	Opcode	Address	Data
Read	10101000	A5 A4 A3 A2 A1 A0 0 0	D15–D0
Write	10100100	A5 A4 A3 A2 A1 A0 0 0	D15–D0
Write Enable	10100011	X X X X X X X X	
Write Disable	10100000	X X X X X X X X	
[Write All Locations](8)	10100001	X X X X X X X X	D15–D0

Figure 1. A.C. Testing Input/Output Waveform (9)(10)(11) (C_L = 100 pF)



5064 FHD F03

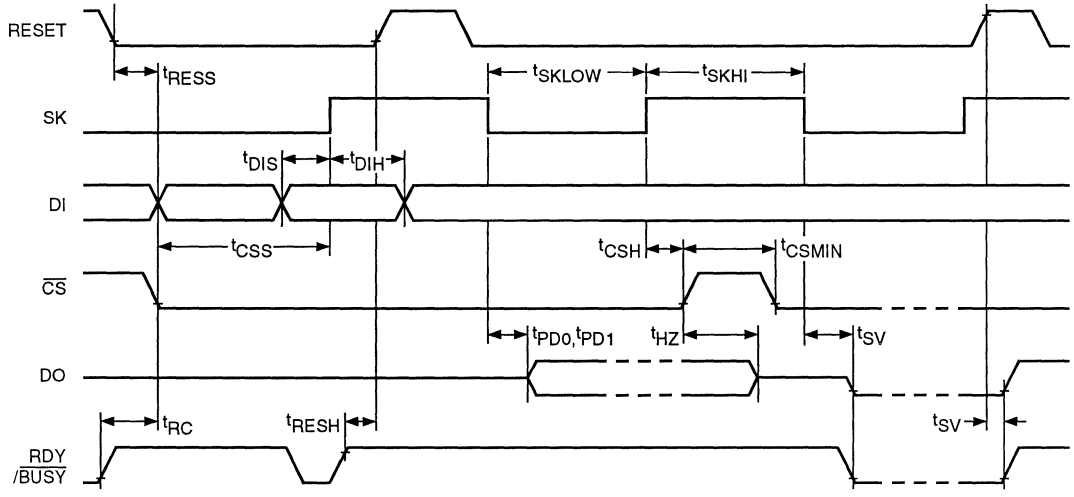
Note:
(8) (Write All Locations) is a test mode operation and is therefore not included in the A.C./D.C. Operations specifications.
(9) Input Rise and Fall Times (10% to 90%) < 10 ns.
(10) Input Pulse Levels = V_{CC} x 0.2 and V_{CC} x 0.8.
(11) Input and Output Timing Reference = V_{CC} x 0.3 and V_{CC} x 0.7.

DEVICE OPERATION

The CAT64LC10/CAT64LC10I is a 1K bit nonvolatile memory intended for use with all standard controllers. The CAT64LC10/CAT64LC10I is organized in a 64 x 16 format. All instructions are based on an 8 bit format. There are four 16 bit instructions: READ, WRITE, EWEN, and EWDS. The CAT64LC10/CAT64LC10I operates on a single power supply ranging from 2.5V to 5.5V and it has an on-chip voltage generator to provide the high voltage needed during a programming operation. Instructions, addresses and data to be written are clocked into the DI pin on the rising edge of the SK clock. The DO pin is normally in a high impedance state except when outputting data in a READ operation or outputting RDY/$\overline{\text{BUSY}}$ status when polled during a WRITE operation.

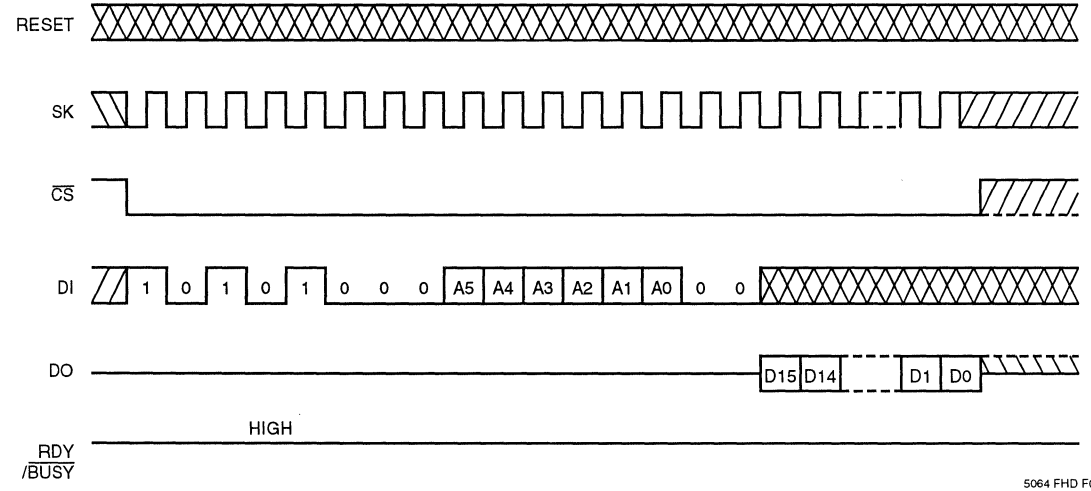
The format for all instructions sent to this device includes a 4 bit start sequence, 1010, a 4 bit op code and an 8 bit address field or dummy bits. For a WRITE operation, a

Figure 2. Sychronous Data Timing



5064 FHD F04

Figure 3. Read Instruction Timing



5064 FHD F05

16 bit data field is also required following the 8 bit address field.

The CAT64LC10/CAT64LC10I requires an active LOW $\overline{CS}$ in order to be selected. Each instruction must be preceded by a HIGH-to-LOW transition of $\overline{CS}$ before the input of the 4 bit start sequence. Prior to the 4 bit start sequence (1010), the device will ignore inputs of all other logical sequence.

Read

Upon receiving a READ command and address (clocked into the DI pin), the DO pin will output data one t_{PD} after the falling edge of the 16th clock (the last bit of the address field). The READ operation is not affected by the RESET input.

Write

After receiving a WRITE op code, address and data, the device goes into the AUTO-Clear cycle and then the

Figure 4. Write Instruction Timing

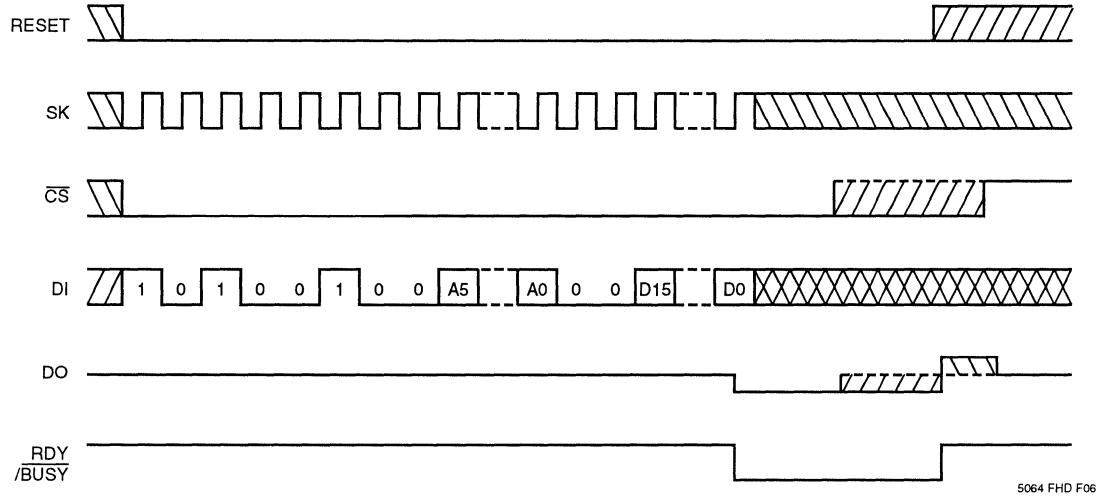
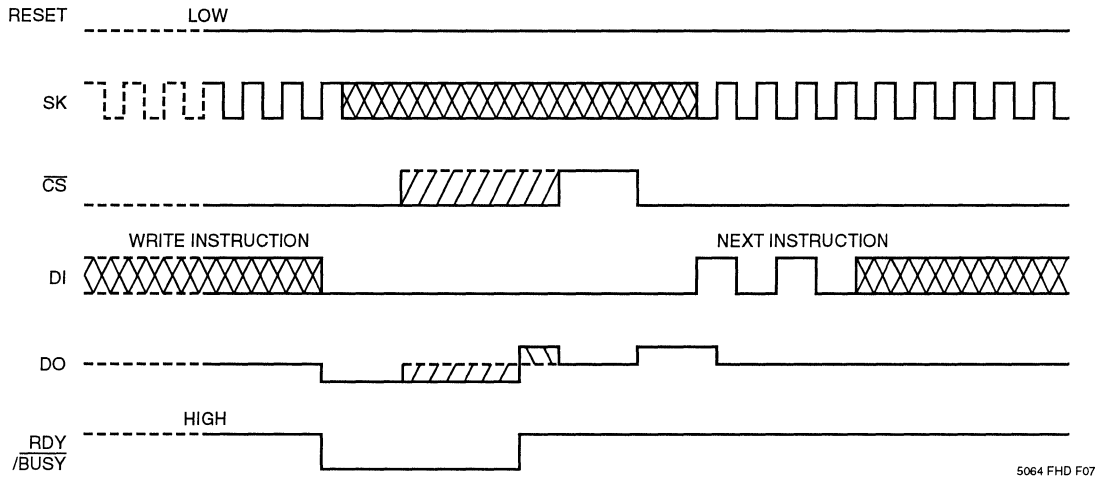


Figure 5. Ready/$\overline{BUSY}$ Status Instruction Timing



WRITE cycle. The RDY/$\overline{\text{BUSY}}$ pin will output the $\overline{\text{BUSY}}$ status (LOW) one t_{SV} after the rising edge of the 32nd clock (the last data bit) and will stay LOW until the write cycle is complete. Then it will output a logical "1" until the next WRITE cycle. The RDY/$\overline{\text{BUSY}}$ output is not affected by the input of $\overline{\text{CS}}$.

An alternative to get RDY/$\overline{\text{BUSY}}$ status is from the DO pin. During a write cycle, asserting a LOW input to the $\overline{\text{CS}}$ pin will cause the DO pin to output the RDY/$\overline{\text{BUSY}}$ status. Bringing $\overline{\text{CS}}$ HIGH will bring the DO pin back to a high impedance state again. After the device has completed a WRITE cycle, the DO pin will output a logical "1" when the device is deselected. The rising edge of the first "1" input on the DI pin will reset DO back to the high impedance state again.

The WRITE operation can be halted anywhere in the operation by the RESET input. If a RESET pulse occurs during a WRITE operation, the device will abort the operation and output a READY status.

NOTE: Data may be corrupted if a RESET occurs while the device is BUSY. If the reset occurs before the BUSY period, no writing will be initiated. However, if RESET occurs after the BUSY period, new data will have been written over the old data.

Figure 6. RESET During $\overline{\text{BUSY}}$ Instruction Timing

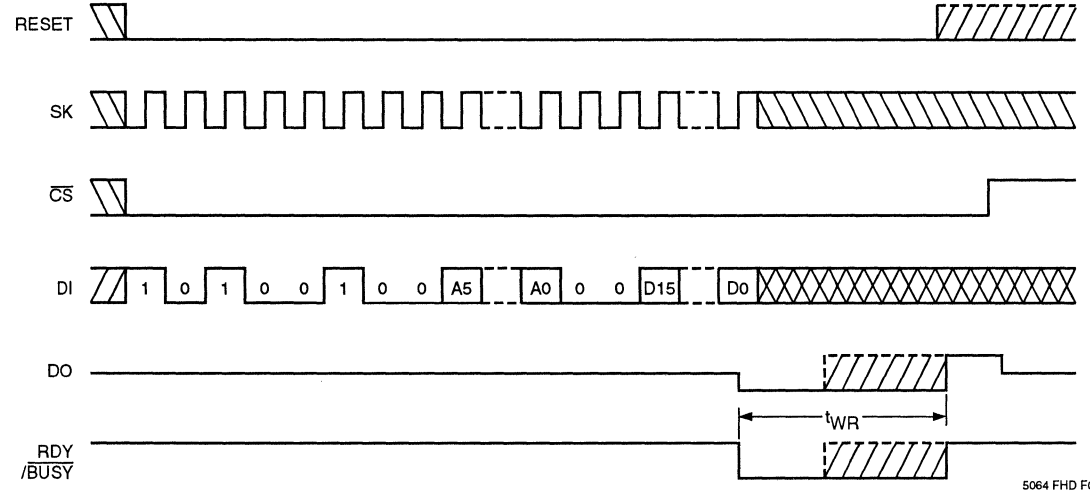
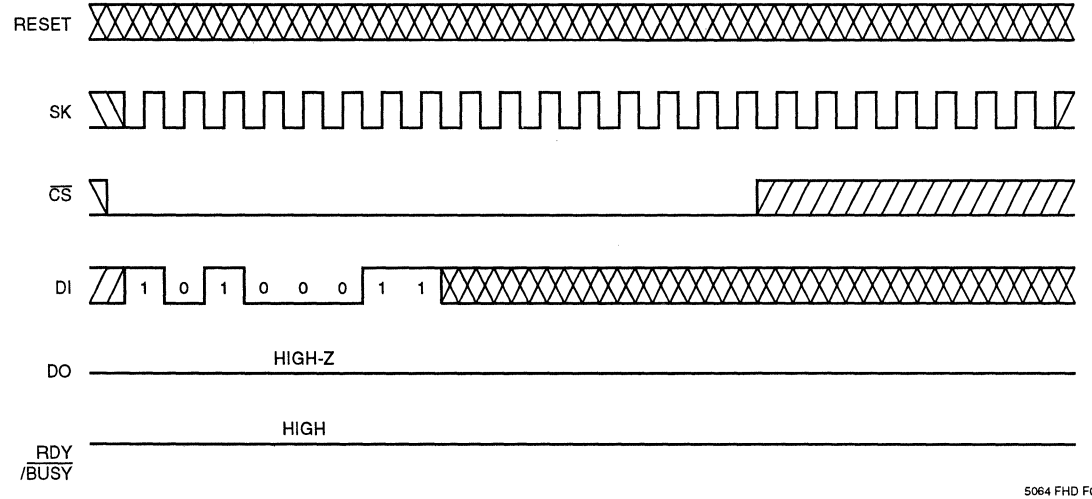


Figure 7. EWEN Instruction Timing



RESET

The RESET pin, when set to HIGH, will reset or abort a WRITE operation. When RESET is set to HIGH while the WRITE instruction is being entered, the device will not execute the WRITE instruction and will keep DO in High-Z condition.

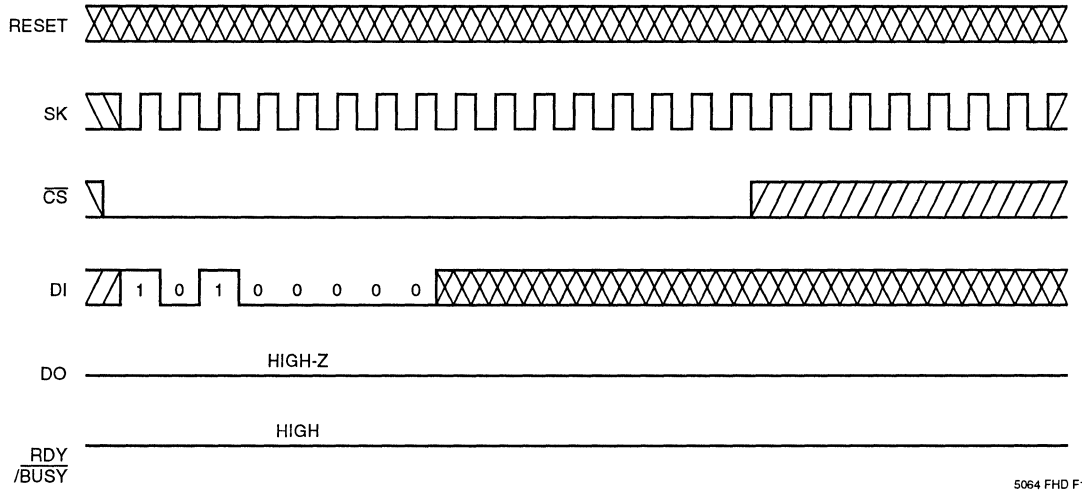
When RESET is set to HIGH, while the device is in a clear/write cycle, the device will abort the operation and will display READY status on the RDY/$\overline{\text{BUSY}}$ pin and on the DO pin if $\overline{\text{CS}}$ is low.

The RESET input affects only the WRITE and WRITE ALL operations. It does not reset any other operations such as READ, EWEN and EWDS.

ERASE/WRITE ENABLE and DISABLE

The CAT64LC10/CAT64LC10I powers up in the erase/write disabled state. After power-up or while the device is in an erase/write disabled state, any write operation must be preceded by an execution of the EWEN instruction. Once enabled, the device will stay enabled until an EWDS has been executed or a power-down has occured. The EWDS is used to prevent any inadvertent over-writing of the data. The EWEN and EWDS instructions have no affect on the READ operation and are not affected by the RESET input.

Figure 8. EWDS Instruction Timing



5064 FHD F10

CAT64LC20/CAT64LC20I

2K-Bit SERIAL E²PROM

FEATURES

- SPI Bus Compatible
- Low Power CMOS Technology
- 2.5V to 5.5V Operation
- Self-Timed Write Cycle with Auto-Clear
- Hardware Reset Pin
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- RDY/$\overline{\text{BUSY}}$ Pin for End-of-Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- ZERO Power™ (CAT64LC20Z) Version Available
- Optional High Endurance Device Available

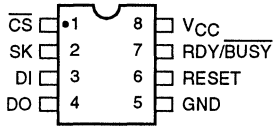
4

DESCRIPTION

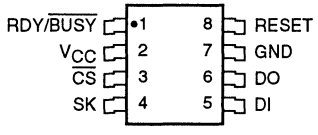
The CAT64LC20 and CAT64LC20I are 2K bit Serial E²PROM memory devices which are configured as 128 registers by 16 bits. Each register can be written (or read) serially by using the DI (or DO) pin. The CAT64LC20/CAT64LC20I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION

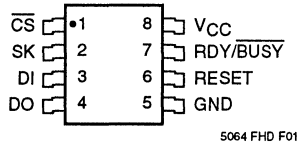
DIP Package



SO Package J



SO Package S

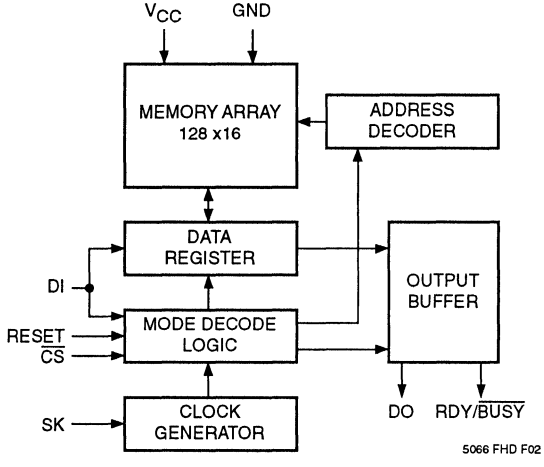


5064 FHD F01

PIN FUNCTIONS

Pin Name	Function
$\overline{CS}$	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+2.5V to +5.5V Power Supply
GND	Ground
RESET	Reset
RDY/$\overline{BUSY}$	Ready/$\overline{BUSY}$ Status

BLOCK DIAGRAM



5066 FHD F02

TD 5066

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE (T_A = 25°C, f= 1.0 MHz, V_{CC} = 5.5V)

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (DO, RDY/$\overline{BUSY}$)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance ($\overline{CS}$, SK, DI, RESET)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

CAT64LC20 T_A= 0°C to +70°C, V_{CC} = +2.5V to +5.5V, unless otherwise specified.
CAT64LC20I T_A= –40°C to +85°C, V_{CC} = +2.5V to +5.5V, unless otherwise specified.

Sym.	Parameter		Limits Min.	Typ.	Max.	Units	Test Conditions
I_{CC}	Operating Current	2.5V			0.4	mA	f_{SK} = 250 kHz
	EWEN, EWDS, READ	5.5V			1.0		f_{SK} = 1 MHz
I_{CCP}	Program Current	2.5V			2.0	mA	
		5.5V			3.0		
I_{SB}	Standby Current	Standard			3.0	µA	V_{IN} = GND or V_{CC}
I_{SBZ}(5)		ZERO Pwr™			0		$\overline{CS}$ = V_{CC}
I_{LI}	Input Leakage Current				2.0	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current				10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Low Level Input Voltage, DI		–0.1		V_{CC} x 0.3	V	
V_{IH}	High Level Input Voltage, DI		V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{IL}	Low Level Input Voltage, $\overline{CS}$, SK, RESET		–0.1		V_{CC} x 0.2	V	
V_{IH}	High Level Input Voltage, $\overline{CS}$, SK, RESET		V_{CC} x 0.8		V_{CC} + 0.5	V	
V_{OH}	High Level Output Voltage	2.5V	V_{CC} – 0.3			V	I_{OH} = –10µA
		4.5V	V_{CC} – 0.3				I_{OH} = –10µA
			2.4				I_{OH} = –400µA
V_{OL}	Low Level Output Voltage	2.5V			0.4	V	I_{OL} = 10µA
		4.5V					I_{OL} = 2.1mA

Note:
(5) Standby Current (I_{SBZ}) = 0µA (<900nA)

A.C. OPERATING CHARACTERISTICS

CAT64LC20 T_A= 0°C to +70°C, V_{CC} = +2.5V to +5.5V, unless otherwise specified.
CAT64LC20I T_A= –40°C to +85°C, V_{CC} = +2.5V to +5.5V, unless otherwise specified.

Symbol	Parameter		Limits			Units
			Min.	Typ.	Max.	
t_{CSS}	$\overline{CS}$ Setup Time		100			ns
t_{CSH}	$\overline{CS}$ Hold Time		100			ns
t_{DIS}	DI Setup Time		200			ns
t_{DIH}	DI Hold Time		200			ns
t_{PD1}	Output Delay to 1				300	ns
t_{PD0}	Output Delay to 0				300	ns
t_{HZ}(6)	Output Delay to High Impendance				500	ns
t_{CSMIN}	Minimum $\overline{CS}$ High Time		250			ns
t_{SKHI}	Minimum SK High Time	2.5V	1000			ns
		4.5V–5.5V	400			
t_{SKLOW}	Minimum SK Low Time	2.5V	1000			ns
		4.5V–5.5V	400			
t_{SV}	Output Delay to Status Valid				500	ns
f_{SK}	Maximum Clock Frequency	2.5V	250			kHz
		4.5V–5.5V	1000			
t_{RESS}	Reset to $\overline{CS}$ Setup Time		0			ns
t_{RESMIN}	Minimum RESET High Time		250			ns
t_{RESH}	RESET to READY Hold Time		0			ns
t_{RC}	Write Recovery		100			ns

POWER-UP TIMING(3)(7)

Symbol	Parameter	Min.	Max.	Units
t_{PUR}	Power-Up to Read Operation		10	µs
t_{PUW}	Power-Up to Program Operation		1	ms

WRITE CYCLE LIMIITS

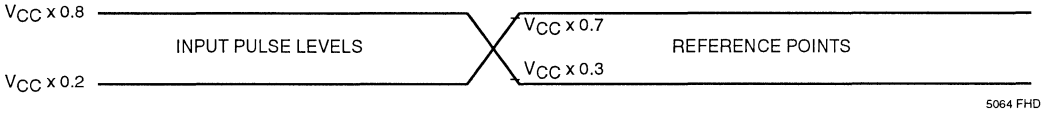
Symbol	Parameter		Min.	Max.	Units
t_{WR}	Program Cycle Time	2.5V		10	ms
		4.5V–5.5V		5	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(6) This parameter is sampled but not 100% tested.
(7) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

INSTRUCTION SET

Instruction	Opcode	Address	Data
Read	10101000	A6 A5 A4 A3 A2 A1 A0 0	D15–D0
Write	10100100	A6 A5 A4 A3 A2 A1 A0 0	D15–D0
Write Enable	10100011	X X X X X X X X	
Write Disable	10100000	X X X X X X X X	
[Write All Locations][8]	10100001	X X X X X X X X	D15–D0

Figure 1. A.C. Testing Input/Output Waveform [9][10][11] (C_L = 100 pF)



4

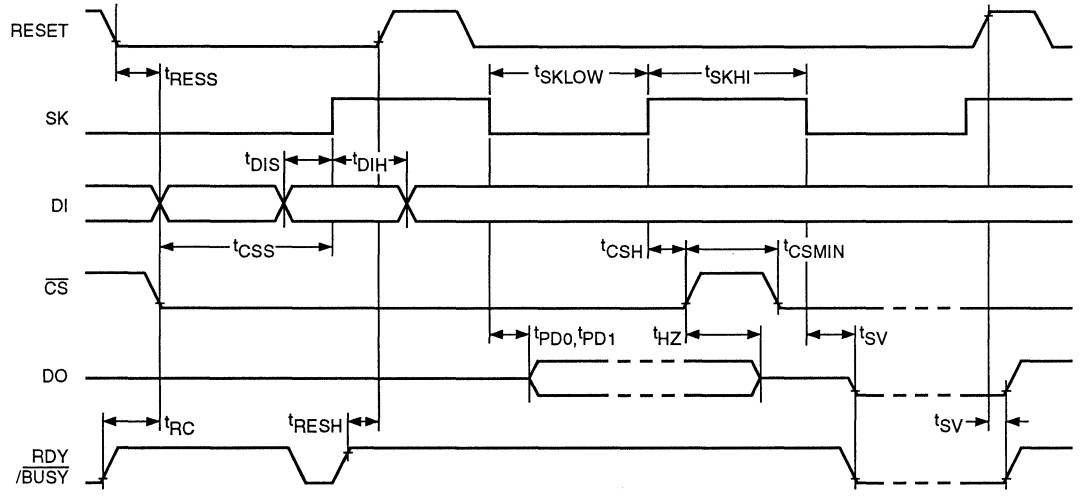
Note:
(8) (Write All Locations) is a test mode operation and is therefore not included in the A.C./D.C. Operations specifications.
(9) Input Rise and Fall Times (10% to 90%) < 10 ns.
(10) Input Pulse Levels = V_{CC} x 0.2 and V_{CC} x 0.8.
(11) Input and Output Timing Reference = V_{CC} x 0.3 and V_{CC} x 0.7.

DEVICE OPERATION

The CAT64LC20/CAT64LC20I is a 2K bit nonvolatile memory intended for use with all standard controllers. The CAT64LC20/CAT64LC20I is organized in a 128 x 16 format. All instructions are based on an 8 bit format. There are four 16 bit instructions: READ, WRITE, EWEN, and EWDS. The CAT64LC20/CAT64LC20I operates on a single power supply ranging from 2.5V to 5.5V and it has an on-chip voltage generator to provide the high voltage needed during a programming operation. Instructions, addresses and data to be written are clocked into the DI pin on the rising edge of the SK clock. The DO pin is normally in a high impedance state except when outputting data in a READ operation or outputting RDY/$\overline{\text{BUSY}}$ status when polled during a WRITE operation.

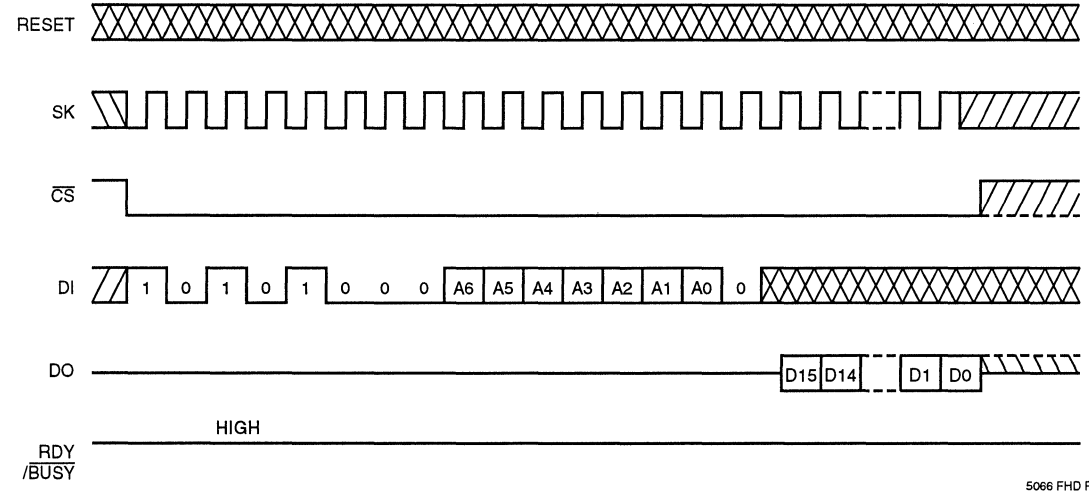
The format for all instructions sent to this device includes a 4 bit start sequence, 1010, a 4 bit op code and an 8 bit address field or dummy bits. For a WRITE operation, a

Figure 2. Sychronous Data Timing



5064 FHD F04

Figure 3. Read Instruction Timing



5066 FHD F05

16 bit data field is also required following the 8 bit address field.

The CAT64LC20/CAT64LC20I requires an active LOW $\overline{CS}$ in order to be selected. Each instruction must be preceded by a HIGH-to-LOW transition of $\overline{CS}$ before the input of the 4 bit start sequence. Prior to the 4 bit start sequence (1010), the device will ignore inputs of all other logical sequence.

Read

Upon receiving a READ command and address (clocked into the DI pin), the DO pin will output data one t_{PD} after the falling edge of the 16th clock (the last bit of the address field). The READ operation is not affected by the RESET input.

Write

After receiving a WRITE op code, address and data, the device goes into the AUTO-Clear cycle and then the

Figure 4. Write Instruction Timing

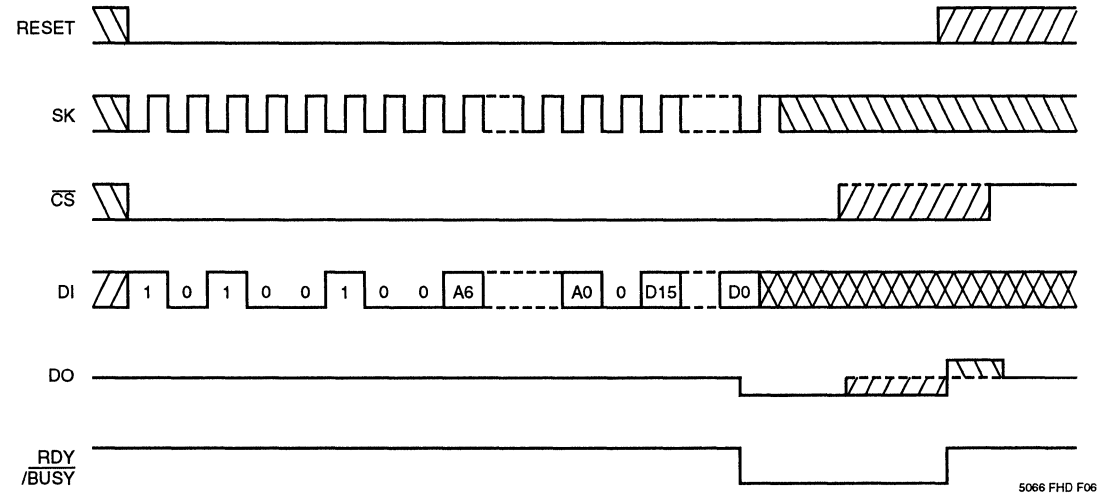
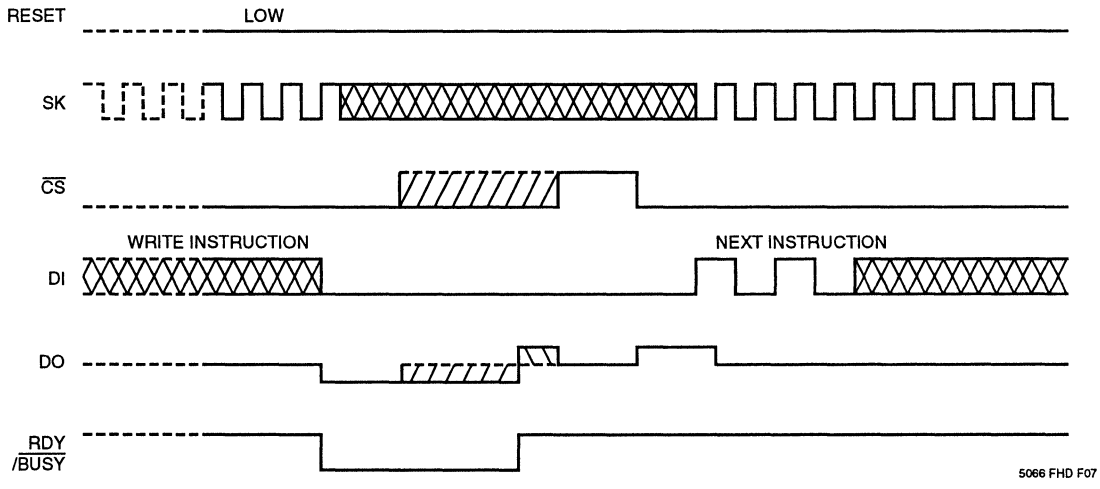


Figure 5. Ready/$\overline{BUSY}$ Status Instruction Timing



WRITE cycle. The RDY/$\overline{BUSY}$ pin will output the $\overline{BUSY}$ status (LOW) one t_{SV} after the rising edge of the 32nd clock (the last data bit) and will stay LOW until the write cycle is complete. Then it will output a logical "1" until the next WRITE cycle. The RDY/$\overline{BUSY}$ output is not affected by the input of $\overline{CS}$.

An alternative to get RDY/$\overline{BUSY}$ status is from the DO pin. During a write cycle, asserting a LOW input to the $\overline{CS}$ pin will cause the DO pin to output the RDY/$\overline{BUSY}$ status. Bringing $\overline{CS}$ HIGH will bring the DO pin back to a high impedance state again. After the device has completed a WRITE cycle, the DO pin will output a logical "1" when the device is deselected. The rising edge of the first "1" input on the DI pin will reset DO back to the high impedance state again.

The WRITE operation can be halted anywhere in the operation by the RESET input. If a RESET pulse occurs during a WRITE operation, the device will abort the operation and output a READY status.

NOTE: Data may be corrupted if a RESET occurs while the device is BUSY. If the reset occurs before the BUSY period, no writing will be initiated. However, if RESET occurs after the BUSY period, new data will have been written over the old data.

Figure 6. RESET During $\overline{BUSY}$ Instruction Timing

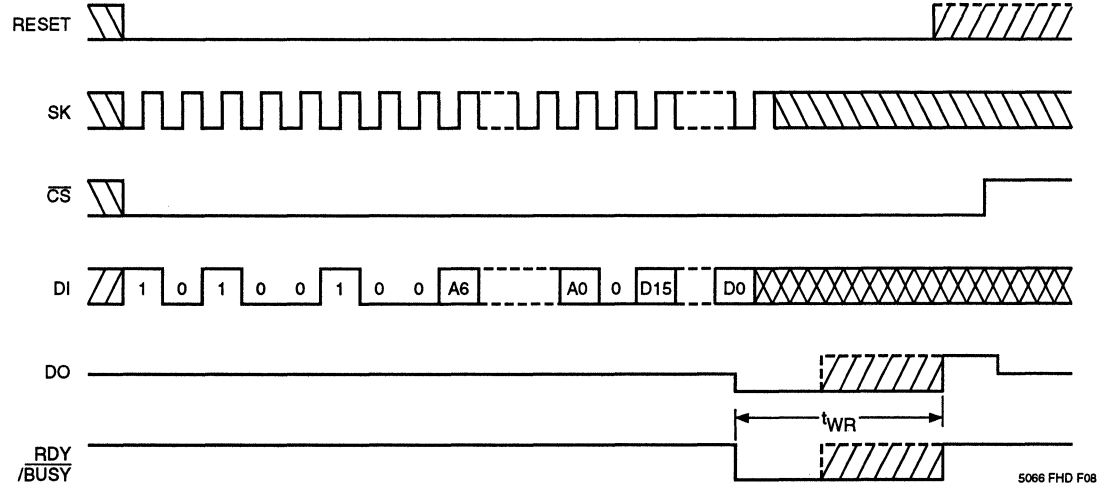
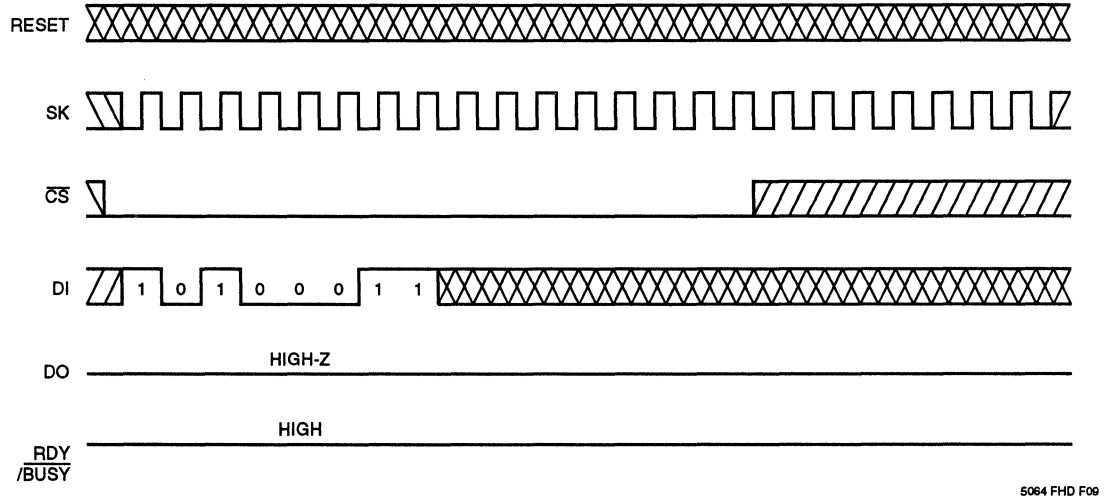


Figure 7. EWEN Instruction Timing



RESET

The RESET pin, when set to HIGH, will reset or abort a WRITE operation. When RESET is set to HIGH while the WRITE instruction is being entered, the device will not execute the WRITE instruction and will keep DO in High-Z condition.

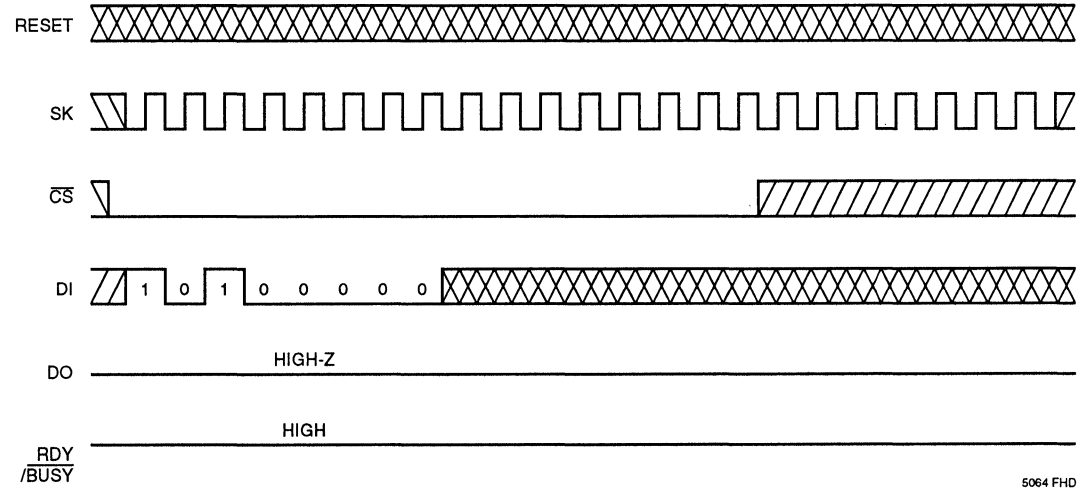
When RESET is set to HIGH, while the device is in a clear/write cycle, the device will abort the operation and will display READY status on the RDY/$\overline{BUSY}$ pin and on the DO pin if $\overline{CS}$ is low.

The RESET input affects only the WRITE and WRITE ALL operations. It does not reset any other operations such as READ, EWEN and EWDS.

ERASE/WRITE ENABLE and DISABLE

The CAT64LC20/CAT64LC20I powers up in the erase/write disabled state. After power-up or while the device is in an erase/write disabled state, any write operation must be preceded by an execution of the EWEN instruction. Once enabled, the device will stay enabled until an EWDS has been executed or a power-down has occured. The EWDS is used to prevent any inadvertent over-writing of the data. The EWEN and EWDS instructions have no affect on the READ operation and are not affected by the RESET input.

Figure 8. EWDS Instruction Timing



CAT64LC40/CAT64LC40I

4K-Bit SERIAL E²PROM

FEATURES

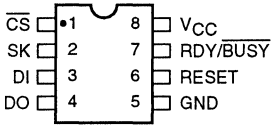
- SPI Bus Compatible
- Low Power CMOS Technology
- 2.5V to 5.5V Operation
- Self-Timed Write Cycle with Auto-Clear
- Hardware Reset Pin
- Hardware and Software Write Protection
- Power-Up Inadvertant Write Protection
- RDY/$\overline{\text{BUSY}}$ Pin for End-of-Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- ZERO Power™ (CAT64LC40Z) Version Available
- Optional High Endurance Device Available

DESCRIPTION

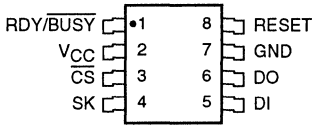
The CAT64LC40 and CAT64LC40I are 4K bit Serial E²PROM memory devices which are configured as 256 registers by 16 bits. Each register can be written (or read) serially by using the DI (or DO) pin. The CAT64LC40/CAT64LC40I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION

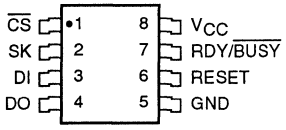
DIP Package



SO Package J



SO Package S



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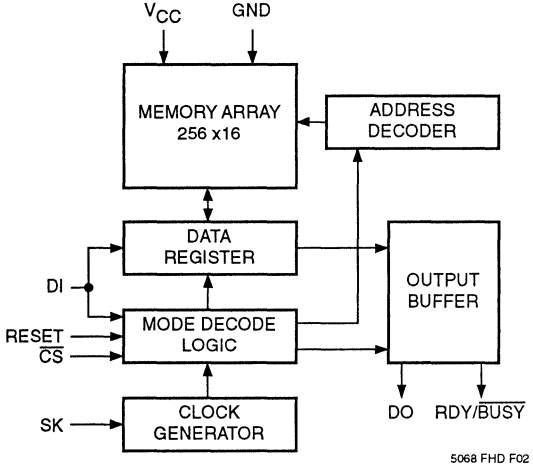
PIN FUNCTIONS

Pin Name	Function
$\overline{\text{CS}}$	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+2.5V to +5.5V Power Supply
GND	Ground
RESET	Reset
RDY/$\overline{\text{BUSY}}$	Ready/$\overline{\text{BUSY}}$ Status

BLOCK DIAGRAM



5068 FHD F02

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE (T_A = 25°C, f= 1.0 MHz, V_{CC} = 5.5V)

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (DO, RDY/$\overline{BUSY}$)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance ($\overline{CS}$, SK, DI, RESET)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

CAT64LC40 T_A= 0°C to +70°C, V_{CC} = +2.5V to +5.5V, unless otherwise specified.
CAT64LC40I T_A= –40°C to +85°C, V_{CC} = +2.5V to +5.5V, unless otherwise specified.

Sym.	Parameter		Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
I_{CC}	Operating Current	2.5V			0.4	mA	f_{SK} = 250 kHz
	EWEN, EWDS, READ	5.5V			1.0		f_{SK} = 1 MHz
I_{CCP}	Program Current	2.5V			2.0	mA	
		5.5V			3.0		
I_{SB}	Standby Current	Standard			3.0	µA	V_{IN} = GND or V_{CC}
I_{SBZ}(5)		ZERO Pwr™			0		$\overline{CS}$ = V_{CC}
I_{LI}	Input Leakage Current				2.0	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current				10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Low Level Input Voltage, DI		–0.1		V_{CC} x 0.3	V	
V_{IH}	High Level Input Voltage, DI		V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{IL}	Low Level Input Voltage, $\overline{CS}$, SK, RESET		–0.1		V_{CC} x 0.2	V	
V_{IH}	High Level Input Voltage, $\overline{CS}$, SK, RESET		V_{CC} x 0.8		V_{CC} + 0.5	V	
V_{OH}	High Level Output Voltage	2.5V	V_{CC} – 0.3			V	I_{OH} = –10µA
		4.5V	V_{CC} – 0.3				I_{OH} = –10µA
			2.4				I_{OH} = –400µA
V_{OL}	Low Level Output Voltage	2.5V			0.4	V	I_{OL} = 10µA
		4.5V					I_{OL} = 2.1mA

Note:
(5) Standby Current (I_{SBZ}) = 0µA (<900nA)

A.C. OPERATING CHARACTERISTICS

CAT64LC40 T_A= 0°C to +70°C, V_{CC} = +2.5V to +5.5V, unless otherwise specified.
CAT64LC40I T_A= –40°C to +85°C, V_{CC} = +2.5V to +5.5V, unless otherwise specified.

Symbol	Parameter		Limits			Units
			Min.	Typ.	Max.	
t_{CSS}	$\overline{CS}$ Setup Time		100			ns
t_{CSH}	$\overline{CS}$ Hold Time		100			ns
t_{DIS}	DI Setup Time		200			ns
t_{DIH}	DI Hold Time		200			ns
t_{PD1}	Output Delay to 1				300	ns
t_{PD0}	Output Delay to 0				300	ns
t_{HZ}(6)	Output Delay to High Impendance				500	ns
t_{CSMIN}	Minimum $\overline{CS}$ High Time		250			ns
t_{SKHI}	Minimum SK High Time	2.5V	1000			ns
		4.5V–5.5V	400			
t_{SKLOW}	Minimum SK Low Time	2.5V	1000			ns
		4.5V–5.5V	400			
t_{SV}	Output Delay to Status Valid				500	ns
f_{SK}	Maximum Clock Frequency	2.5V	250			kHz
		4.5V–5.5V	1000			
t_{RESS}	Reset to $\overline{CS}$ Setup Time		0			ns
t_{RESMIN}	Minimum RESET High Time		250			ns
t_{RESH}	RESET to READY Hold Time		0			ns
t_{RC}	Write Recovery		100			ns

POWER-UP TIMING(3)(7)

Symbol	Parameter	Min.	Max.	Units
t_{PUR}	Power-Up to Read Operation		10	µs
t_{PUW}	Power-Up to Program Operation		1	ms

WRITE CYCLE LIMIITS

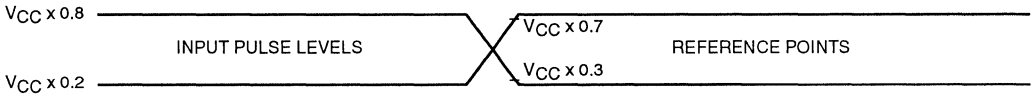
Symbol	Parameter		Min.	Max.	Units
t_{WR}	Program Cycle Time	2.5V		10	ms
		4.5V–5.5V		5	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(6) This parameter is sampled but not 100% tested.
(7) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

INSTRUCTION SET

Instruction	Opcode	Address	Data
Read	10101000	A7 A6 A5 A4 A3 A2 A1 A0	D15–D0
Write	10100100	A7 A6 A5 A4 A3 A2 A1 A0	D15–D0
Write Enable	10100011	X X X X X X X X	
Write Disable	10100000	X X X X X X X X	
[Write All Locations][8]	10100001	X X X X X X X X	D15–D0

Figure 1. A.C. Testing Input/Output Waveform [9][10][11] (C_L = 100 pF)



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Note:
(8) (Write All Locations) is a test mode operation and is therefore not included in the A.C./D.C. Operations specifications.
(9) Input Rise and Fall Times (10% to 90%) < 10 ns.
(10) Input Pulse Levels = V_{CC} x 0.2 and V_{CC} x 0.8.
(11) Input and Output Timing Reference = V_{CC} x 0.3 and V_{CC} x 0.7.

DEVICE OPERATION

The CAT64LC40/CAT64LC40I is a 4K bit nonvolatile memory intended for use with all standard controllers. The CAT64LC40/CAT64LC40I is organized in a 256 x 16 format. All instructions are based on an 8 bit format. There are four 16 bit instructions: READ, WRITE, EWEN, and EWDS. The CAT64LC40/CAT64LC40I operates on a single power supply ranging from 2.5V to 5.5V and it has an on-chip voltage generator to provide the high voltage needed during a programming operation. Instructions, addresses and data to be written are clocked into the DI pin on the rising edge of the SK clock. The DO pin is normally in a high impedance state except when outputting data in a READ operation or outputting RDY/$\overline{\text{BUSY}}$ status when polled during a WRITE operation.

The format for all instructions sent to this device includes a 4 bit start sequence, 1010, a 4 bit op code and an 8 bit address field or dummy bits. For a WRITE operation, a

Figure 2. Sychronous Data Timing

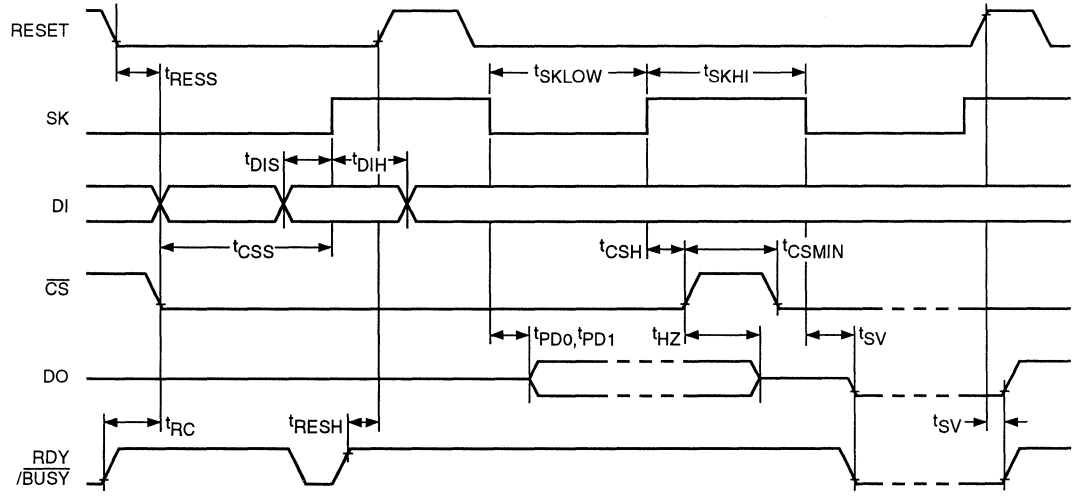

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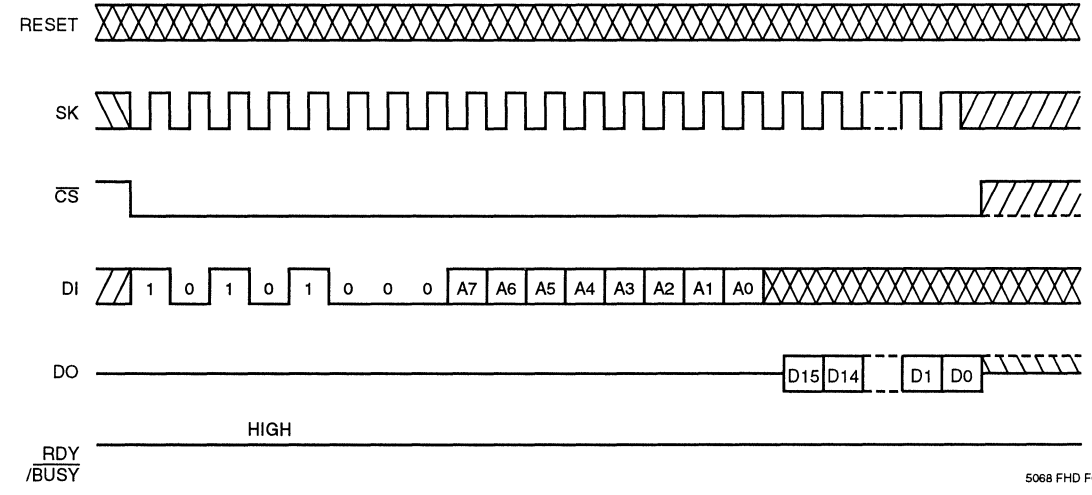
Figure 3. Read Instruction Timing



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16 bit data field is also required following the 8 bit address field.

The CAT64LC40/CAT64LC40I requires an active LOW $\overline{CS}$ in order to be selected. Each instruction must be preceded by a HIGH-to-LOW transition of $\overline{CS}$ before the input of the 4 bit start sequence. Prior to the 4 bit start sequence (1010), the device will ignore inputs of all other logical sequence.

Read

Upon receiving a READ command and address (clocked into the DI pin), the DO pin will output data one t_{PD} after the falling edge of the 16th clock (the last bit of the address field). The READ operation is not affected by the RESET input.

Write

After receiving a WRITE op code, address and data, the device goes into the AUTO-Clear cycle and then the

Figure 4. Write Instruction Timing

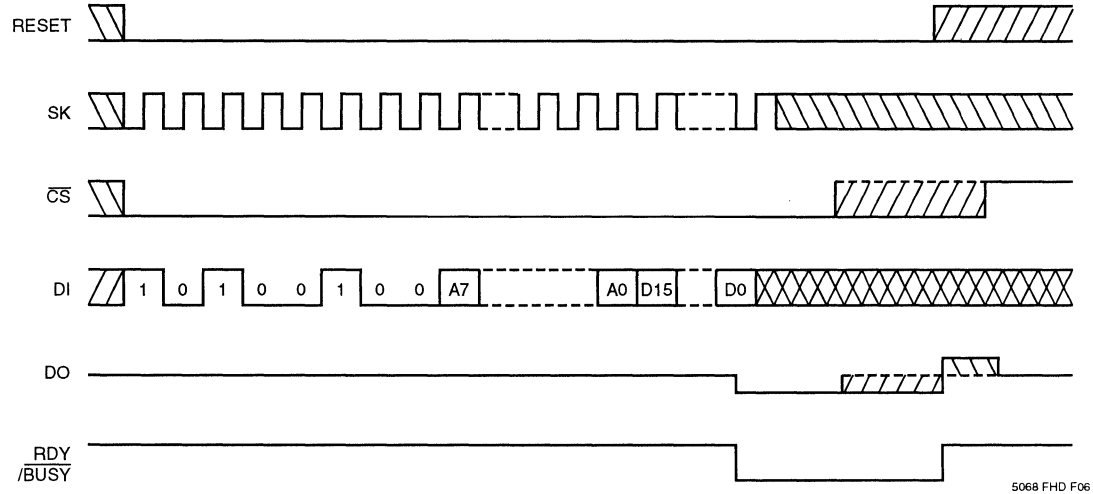
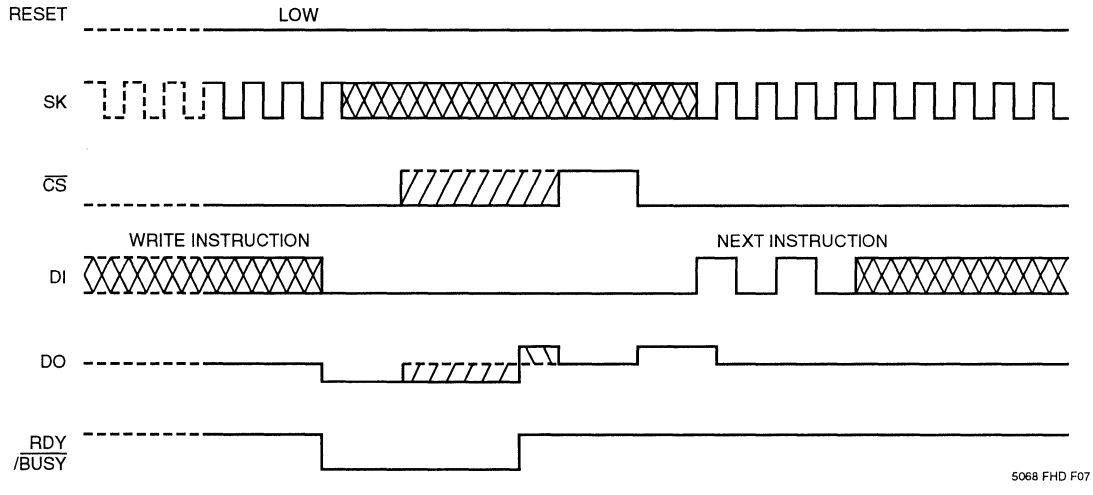


Figure 5. Ready/$\overline{BUSY}$ Status Instruction Timing



WRITE cycle. The RDY/$\overline{\text{BUSY}}$ pin will output the $\overline{\text{BUSY}}$ status (LOW) one t_{SV} after the rising edge of the 32nd clock (the last data bit) and will stay LOW until the write cycle is complete. Then it will output a logical "1" until the next WRITE cycle. The RDY/$\overline{\text{BUSY}}$ output is not affected by the input of $\overline{\text{CS}}$.

An alternative to get RDY/$\overline{\text{BUSY}}$ status is from the DO pin. During a write cycle, asserting a LOW input to the $\overline{\text{CS}}$ pin will cause the DO pin to output the RDY/$\overline{\text{BUSY}}$ status. Bringing $\overline{\text{CS}}$ HIGH will bring the DO pin back to a high impedance state again. After the device has completed a WRITE cycle, the DO pin will output a logical "1" when the device is deselected. The rising edge of the first "1" input on the DI pin will reset DO back to the high impedance state again.

The WRITE operation can be halted anywhere in the operation by the RESET input. If a RESET pulse occurs during a WRITE operation, the device will abort the operation and output a READY status.

NOTE: Data may be corrupted if a RESET occurs while the device is BUSY. If the reset occurs before the BUSY period, no writing will be initiated. However, if RESET occurs after the BUSY period, new data will have been written over the old data.

Figure 6. RESET During $\overline{\text{BUSY}}$ Instruction Timing

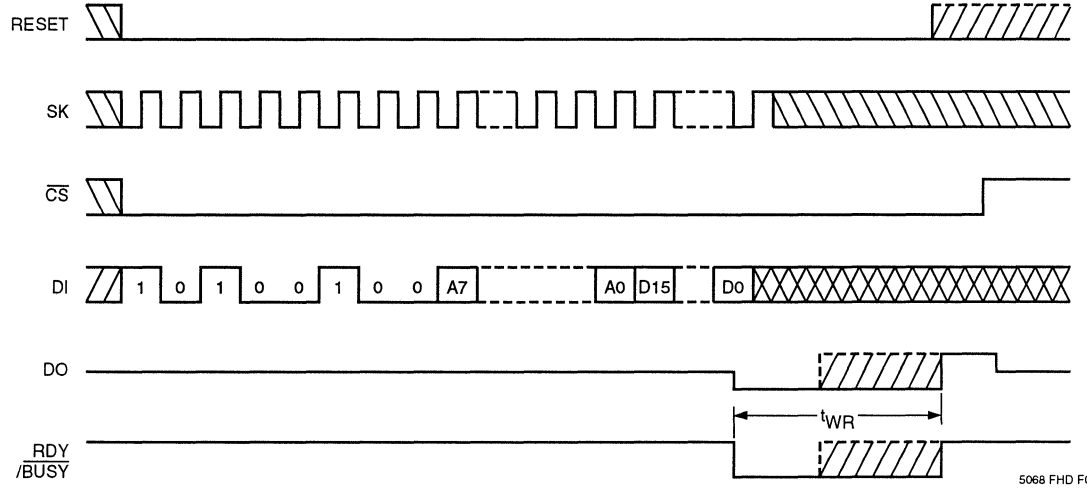
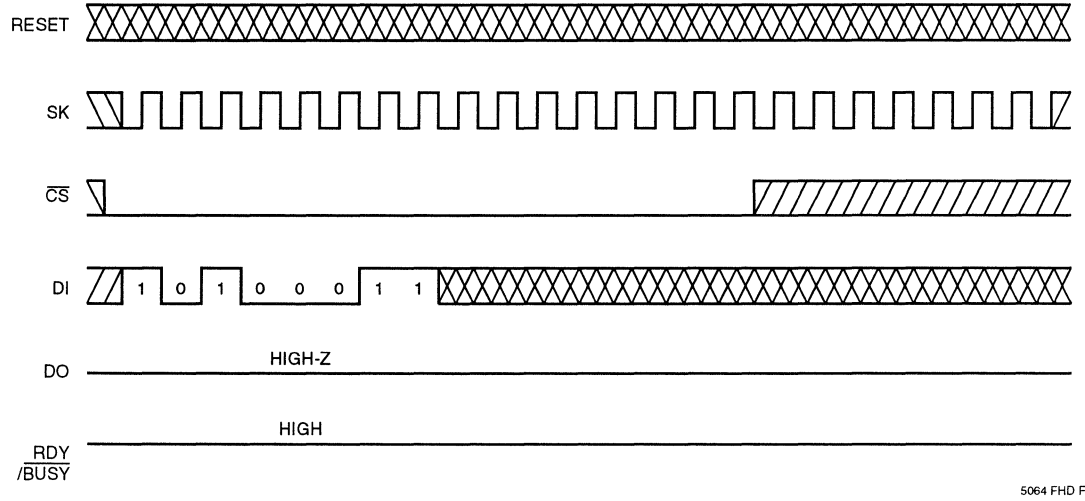


Figure 7. EWEN Instruction Timing



RESET

The RESET pin, when set to HIGH, will reset or abort a WRITE operation. When RESET is set to HIGH while the WRITE instruction is being entered, the device will not execute the WRITE instruction and will keep DO in High-Z condition.

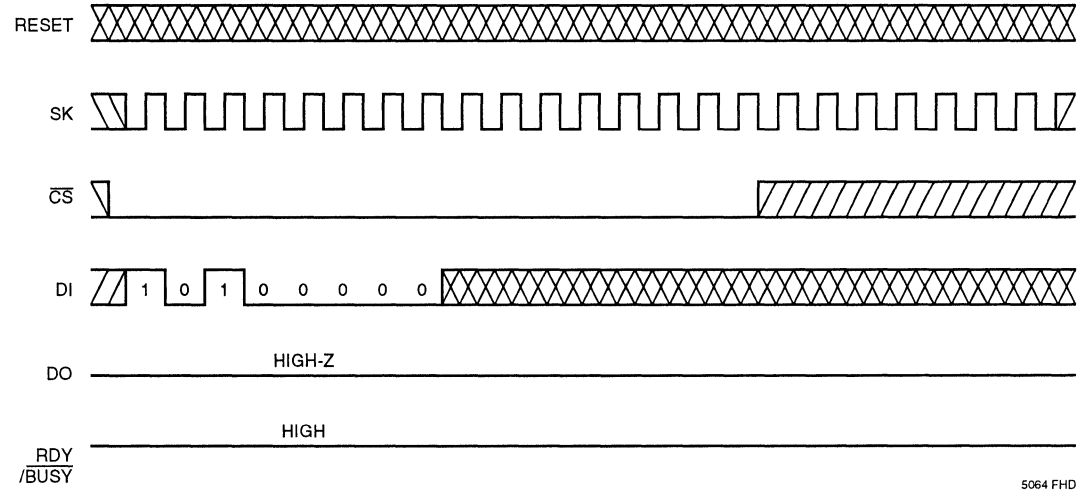
When RESET is set to HIGH, while the device is in a clear/write cycle, the device will abort the operation and will display READY status on the RDY/$\overline{\text{BUSY}}$ pin and on the DO pin if $\overline{\text{CS}}$ is low.

The RESET input affects only the WRITE and WRITE ALL operations. It does not reset any other operations such as READ, EWEN and EWDS.

ERASE/WRITE ENABLE and DISABLE

The CAT64LC40/CAT64LC40I powers up in the erase/write disabled state. After power-up or while the device is in an erase/write disabled state, any write operation must be preceded by an execution of the EWEN instruction. Once enabled, the device will stay enabled until an EWDS has been executed or a power-down has occured. The EWDS is used to prevent any inadvertent over-writing of the data. The EWEN and EWDS instructions have no affect on the READ operation and are not affected by the RESET input.

Figure 8. EWDS Instruction Timing



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CATALYST SEMICONDUCTOR

Product Information 1

2-Wire Bus Serial E^2PROMs 2

3-Wire Bus Serial E^2PROMs 3

SPI Bus Serial E^2PROMs 4

4-Wire Bus Serial E^2PROMs 5

Secure Access Serial E^2PROMs 6

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Contents

SECTION 5 4-WIRE BUS SERIAL E^2PROMS

CAT59C11/CAT59C11I ..... 64 x 16, 128 x 8 ..... 1K-Bit 5-1

CAT35C202/CAT35C202I ..... 128 x 16, 256 x 8 ..... 2K-Bit 5-7

CAT59C11/CAT59C11I

1K-Bit SERIAL E²PROM

FEATURES

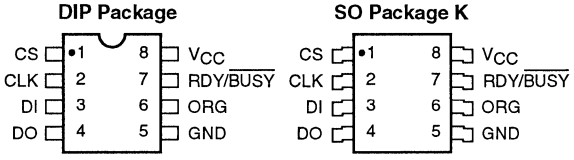
- High Speed Operation: 1MHz
- Low Power CMOS Technology
- Single 5V Supply
- 64 x 16 or 128 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- RDY/$\overline{\text{BUSY}}$ Pin for End-of-Write Detection
- Hardware and Software Write Protection
- Power-Up Inadvertent Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

DESCRIPTION

The CAT59C11 and CAT59C11I are 1K bit Serial E²PROM memory devices which can be configured as either 64 registers by 16 bits (ORG pin at V_{CC}) or 128 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin.

The CAT59C11/CAT59C11I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION



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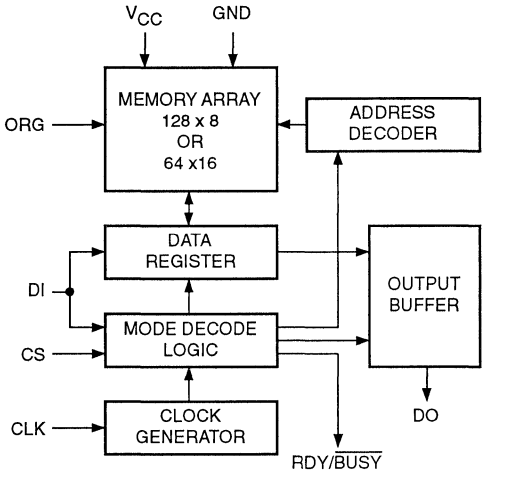
PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
CLK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+5V Power Supply
GND	Ground
RDY/$\overline{\text{BUSY}}$	Ready/Busy Status
ORG	Memory Organization

Note: When the ORG pin is connected to V_{CC}, the 64 x 16 organization is selected. When it is connected to ground, the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64 x 16 organization.

BLOCK DIAGRAM



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TD 5060

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT59C11 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT59C11I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	Power Supply Current (Operating)			5	mA	DI = 0V, CLK = 5.0V V_{CC} = 5.0V, CS = 5.0V Output Open
I_{CC2}	Power Supply Current (Standby)			100	µA	DI = 0V, CLK = 0V V_{CC} = 5.0V, CS = 0V
I_{LI}	Input Leakage Current			2	µA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current (Including ORG Pin)			10	µA	V_{OUT} = 0V to 5.5V, CS = 0
V_{IH}	High Level Input Voltage	2.0		V_{CC} +1	V	
V_{IL}	Low Level Input Voltage	–0.1		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1 mA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1000	A6–A0	A5–A0			Read Address A_N–A_0
WRITE	1	X100	A6–A0	A5–A0	D7–D0	D15–D0	Write Address A_N–A_0
EWEN	1	0011	XXXXXXX	XXXXXX			Write Enable
EWDS	1	0000	XXXXXXX	XXXXXX			Write Disable
ERAL	1	0010	XXXXXXX	XXXXXX			Clear All Addresses
WRAL	1	0001	XXXXXXX	XXXXXX	D7–D0	D15–D0	Write All Addresses

A.C. CHARACTERISTICS

CAT59C11 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT59C11I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	50			ns	
t_{CSH}	CS Hold Time	0			ns	
t_{DIS}	DI Setup Time	100			ns	C_L = 100pF
t_{DIH}	DI Hold Time	100			ns	V_{OL} = 0.8V, V_{OH} = 2.0V
t_{PD1}	Output Delay to 1			500	ns	V_{IL} = 0.45V, V_{IH} = 2.4V
t_{PD0}	Output Delay to 0			500	ns	
t_{HZ}(3)	Output Delay to High-Z			100	ns	C_L = 100pF
t_{EW}	Program/Erase Pulse Width			10	ms	
t_{CKH}	Minimum Clock High Time	100			ns	
t_{CKL}	Minimum Clock Low Time	660			ns	
t_{SV}	RDY/$\overline{\text{BUSY}}$ Delay to Status Valid			500	ns	C_L = 100pF
f_{CLK}	Maximum Clock Frequency	DC		1	MHz	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.

DEVICE OPERATION

The CAT59C11/CAT59C11I is a 1024 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT59C11/CAT59C11I can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Six 11 bit instructions (12 bit instruction in 128x8 organization) control the reading, writing and erase operations of the device. The CAT59C11/CAT59C11I operates on a single 5V supply and will generate on chip, the high voltage required during any write operation. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally in a high impedance state except when reading data from the device. The ready/busy status can be determined after a write operation by polling the RDY/$\overline{\text{BUSY}}$ pin; a low level on this pin indicates that the write operation is not completed, while a high level indicates that the WRITE, ERAL or WRAL operation has been completed and the device is ready for the next instruction.

The format for all instructions sent to the CAT59C11/CAT59C11I is a logical "1" start bit, a 4 bit opcode, a 6 bit address (7 bit address when organized as 128x8), and for write operations a 16 bit data field (8 bit data field when organized as 128x8). At power-down, when V_{CC} falls below a threshold of approximately 3.5V, the data protection circuitry inhibits all erase and write instructions and a write disable (EWDS) is executed internally.

Figure 1. Synchronous Data Timing(5)

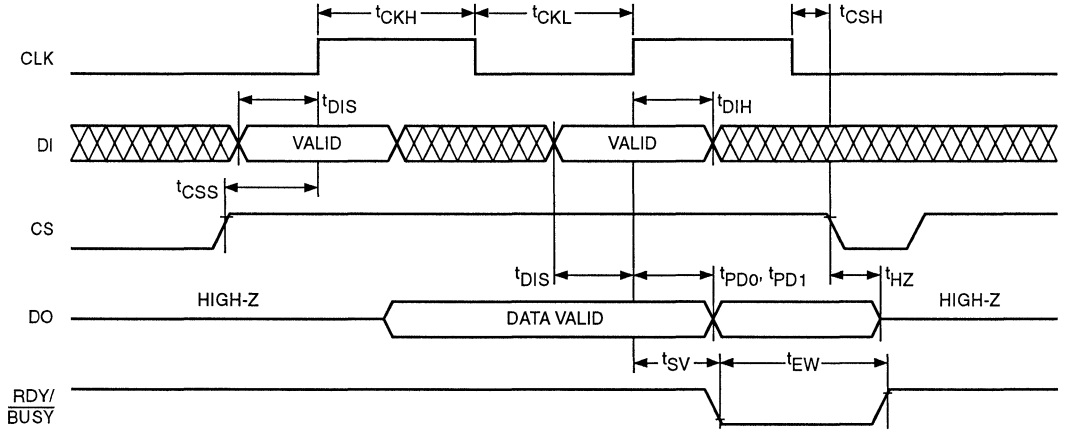

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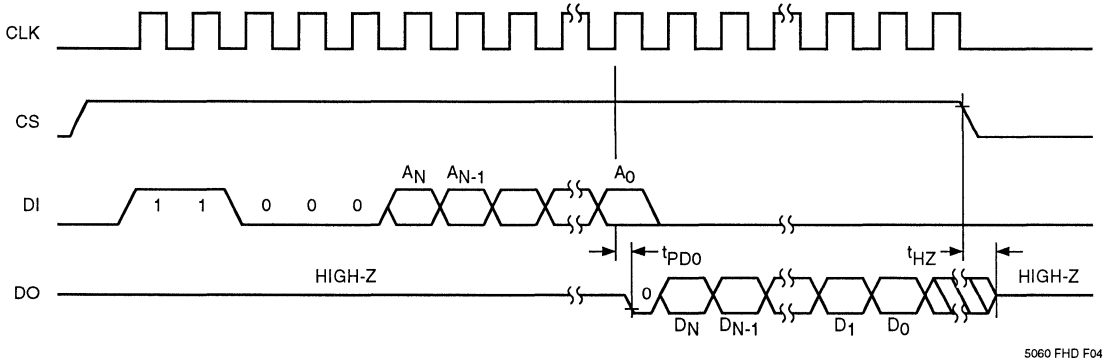
Figure 2. Read Instruction Timing(5)



5060 FHD F04

Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

NOTE: This device will accept a start bit that is generated when both CLK and DI are high with respect to a low to high transition of CS.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT59C11/CAT59C11I will come out of the high impedance state and, after sending an initial dummy zero bit (after a delay of t_{PDO} from the positive edge of the A_0 clock), will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the clock and are stable after the specified time delay (t_{PD0} or t_{PD1}). DO returns to High-Z after a delay of t_{HZ} from the negative going edge of CS.

Erase/Write Enable and Disable

The CAT59C11/CAT59C11I powers up in the write disabled state. Any write after power-up or after a EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWEN instruction is sent. The EWEN instruction can be used to disable all CAT59C11/CAT59C11I write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Write

After receiving a WRITE command, address and data, the RDY/$\overline{BUSY}$ pin goes low (after a delay of t_{SV} from the positive edge of the D_0 clock) indicating the self-clocking program/erase cycle is in progress. The program/erase pulse width (t_{EW}) is timed from the positive clock edge of the last data bit (D_0) and its completion is indicated by the RDY/$\overline{BUSY}$ pin returning to a high level. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent.

5

Figure 3. Write Instruction Timing(5)

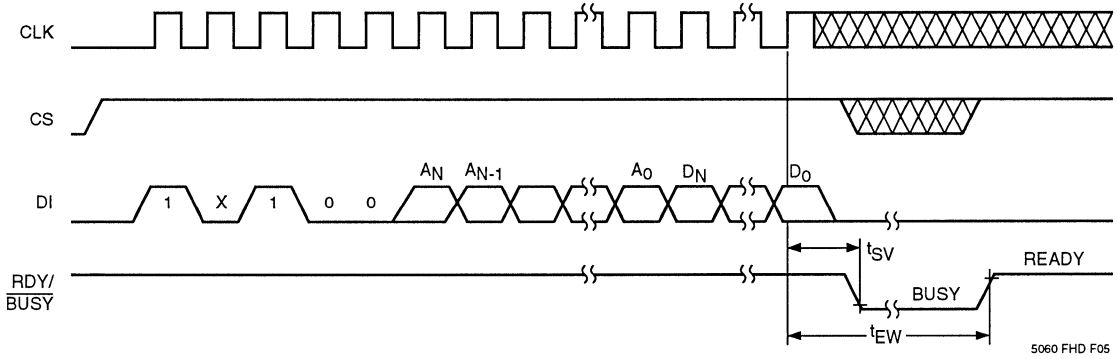
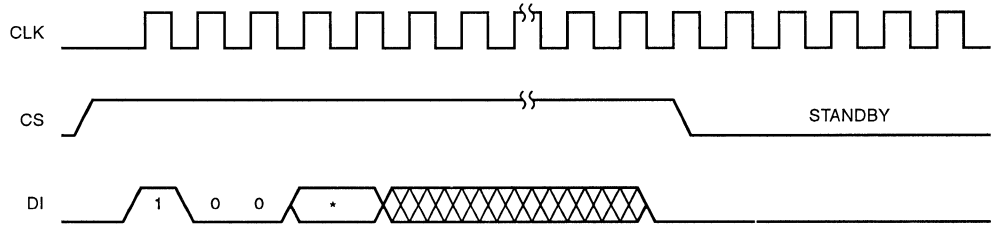


Figure 4. EWEN/EWDS Instruction Timing(5)



* ENABLE = 11 64 x 16 = 6 DON'T CARE BITS
DISABLE = 00 128 x 8 = 7 DON'T CARE BITS

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Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

Erase All

After receiving an ERAL command and address the RDY/$\overline{BUSY}$ pin goes low (after a delay of t_{SV} from the positive edge of the D_0 clock) indicating the self-clocking program/erase cycle is in progress. The program/erase pulse width (t_{EW}) is timed from the positive clock edge of the last don't care bit and its completion is indicated by the RDY/$\overline{BUSY}$ pin returning to a high level. The clocking of the CLK pin is not necessary after the device has entered the self-clocking mode. Once cleared, the contents of all memory bits return to a logical "1" state.

Write All

Upon receiving a WRAL command, address and data, the RDY/$\overline{BUSY}$ pin goes low (after a delay of t_{SV} from the positive edge of the D_0 clock) indicating the self-clocking program/erase cycle is in progress. The program/erase pulse width (t_{EW}) is timed from the positive edge of the last data bit (D_0) and its completion is indicated by the RDY/$\overline{BUSY}$ pin returning to a high level. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. It IS necessary for all memory locations to be cleared before the WRAL command is executed.

Figure 5. ERAL Instruction Timing(5)

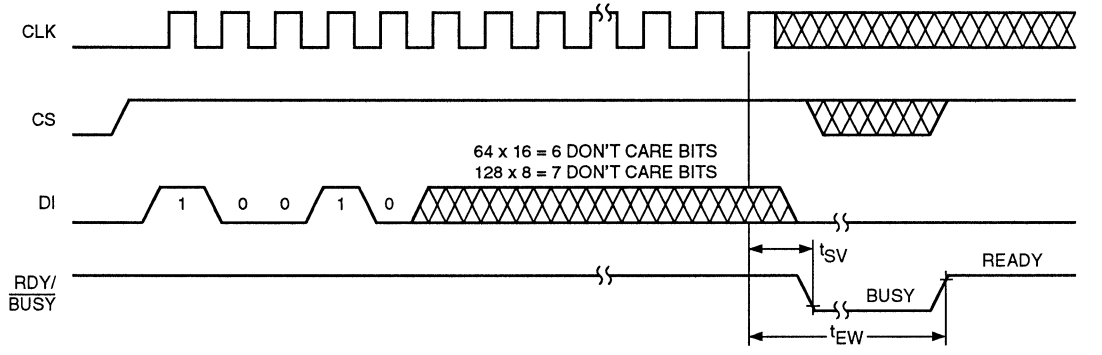
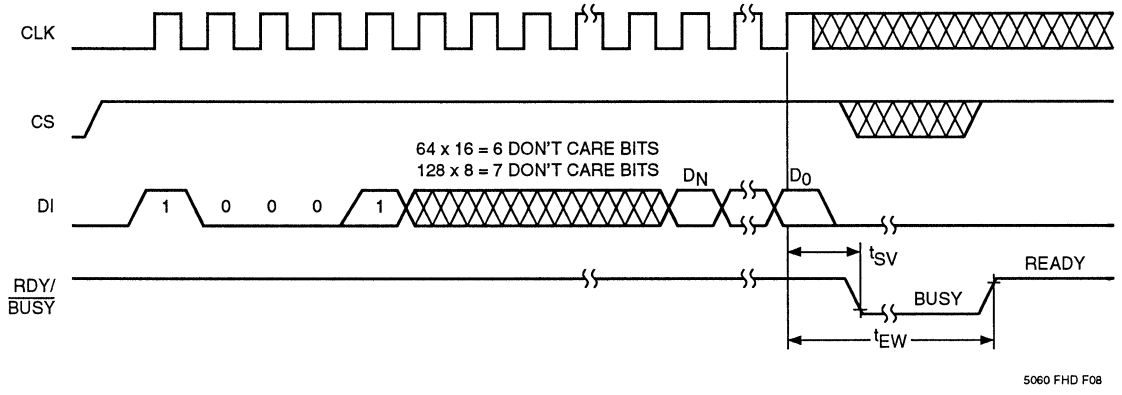


Figure 6. WRAL Instruction Timing(5)



Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A6 and DN = D7. When x16 organization is selected, AN = A5 and DN = D15.

CAT35C202/CAT35C202I

2K-Bit SERIAL E²PROM

FEATURES

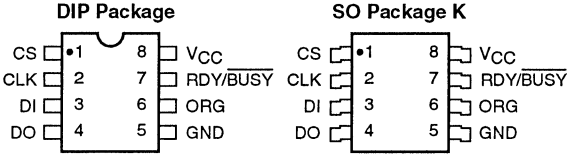
- High Speed Operation: 1MHz
- Low Power CMOS Technology
- Single 5V Supply
- 128 x 16 or 256 x 8 Selectable Serial Memory
- Self-Timed Write Cycle with Auto-Clear
- RDY/$\overline{\text{BUSY}}$ Pin for End-of-Write Detection
- Hardware and Software Write Protection
- Power-Up Inadvertent Write Protection
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

DESCRIPTION

The CAT35C202 and CAT35C202I are 2K bit Serial E²PROM memory devices which can be configured as either 128 registers by 16 bits (ORG pin at V_{CC}) or 256 registers by 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin.

The CAT35C202/CAT35C202I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in 8 pin DIP or SO packages.

PIN CONFIGURATION



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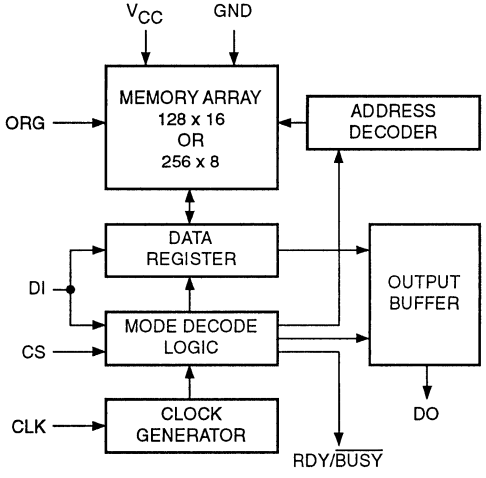
PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
CLK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+5V Power Supply
GND	Ground
RDY/$\overline{\text{BUSY}}$	Ready/Busy Status
ORG	Memory Organization

Note: When the ORG pin is connected to V_{CC}, the 128 x 16 organization is selected. When it is connected to ground, the 256 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 128 x 16 organization.

BLOCK DIAGRAM



5062 FHD F02

TD 5062

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT35C202 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT35C202I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter		Limits Min.	Typ.	Max.	Units	Test Conditions
I_{CC1}	Power Supply Current (Operating)	Comm.			3	mA	DI = 0V, CLK = 5.0V V_{CC} = 5.0V, CS = 5.0V Output Open
		Ind.			4	mA	
I_{CC2}	Power Supply Current (Standby)				100	µA	DI = 0V, CLK = 0V V_{CC} = 5.0V, CS = 0V
I_{LI}	Input Leakage Current				2	µA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current (Including ORG Pin)				10	µA	V_{OUT} = 0V to 5.5V, CS = 0
V_{IH}	High Level Input Voltage		2.0		V_{CC} +1	V	
V_{IL}	Low Level Input Voltage		–0.1		0.8	V	
V_{OH}	High Level Output Voltage		2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage				0.4	V	I_{OL} = 2.1 mA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			256 x 8	128 x 16	256 x 8	128 x 16	
READ	1	1000	A7–A0	A6–A0			Read Address A_N–A_0
WRITE	1	X100	A7–A0	A6–A0	D7–D0	D15–D0	Write Address A_N–A_0
EWEN	1	0011	XXXXXXXX	XXXXXXX			Write Enable
EWDS	1	0000	XXXXXXXX	XXXXXXX			Write Disable
ERAL	1	0010	XXXXXXXX	XXXXXXX			Clear All Addresses
WRAL	1	0001	XXXXXXXX	XXXXXXX	D7–D0	D15–D0	Write All Addresses

A.C. CHARACTERISTICS

CAT35C202 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT35C202I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	50			ns	
t_{CSH}	CS Hold Time	50			ns	
t_{DIS}	DI Setup Time	100			ns	C_L = 100pF
t_{DIH}	DI Hold Time	100			ns	V_{OL} = 0.8V, V_{OH} = 2.0V
t_{PD1}	Output Delay to 1			500	ns	V_{IL} = 0.45V, V_{IH} = 2.4V
t_{PD0}	Output Delay to 0			500	ns	
t_{HZ}(3)	Output Delay to High-Z			100	ns	C_L = 100pF
t_{EW}	Program/Erase Pulse Width			10	ms	
t_{CKH}	Minimum Clock High Time	250			ns	
t_{CKL}	Minimum Clock Low Time	250			ns	
t_{SV}	RDY/$\overline{\text{BUSY}}$ Delay to Status Valid			500	ns	C_L = 100pF
f_{CLK}	Maximum Clock Frequency	DC		1	MHz	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.

DEVICE OPERATION

The CAT35C202/CAT35C202I is a 2048 bit nonvolatile memory intended for use with industry standard microprocessors. The CAT35C202/CAT35C202I can be organized as either 128 registers by 16 bits, or as 256 registers by 8 bits. Six 12 bit instructions (13 bit instruction in 128 x 16 organization) control the reading, writing and erase operations of the device. The CAT35C202/CAT35C202I operates on a single 5V supply and will generate on chip, the high voltage required during any write operation. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally in a high impedance state except when reading data from the device. The ready/busy status can be determined after a write operation by polling the RDY/$\overline{\text{BUSY}}$ pin; a low level on this pin indicates that the write operation is not completed, while a high level indicates that the WRITE, ERAL or WRAL operation has been completed and the device is ready for the next instruction.

The format for all instructions sent to the CAT35C202/CAT35C202I is a logical "1" start bit, a 4 bit opcode, a 7 bit address (8 bit address when organized as 256 x 8), and for write operations a 16 bit data field (8 bit data field when organized as 256 x 8). At power-down, when V_{CC} falls below a threshold of approximately 3.5V, the data protection circuitry inhibits all erase and write instructions and a write disable (EWDS) is executed internally.

Figure 1. Synchronous Data Timing(5)

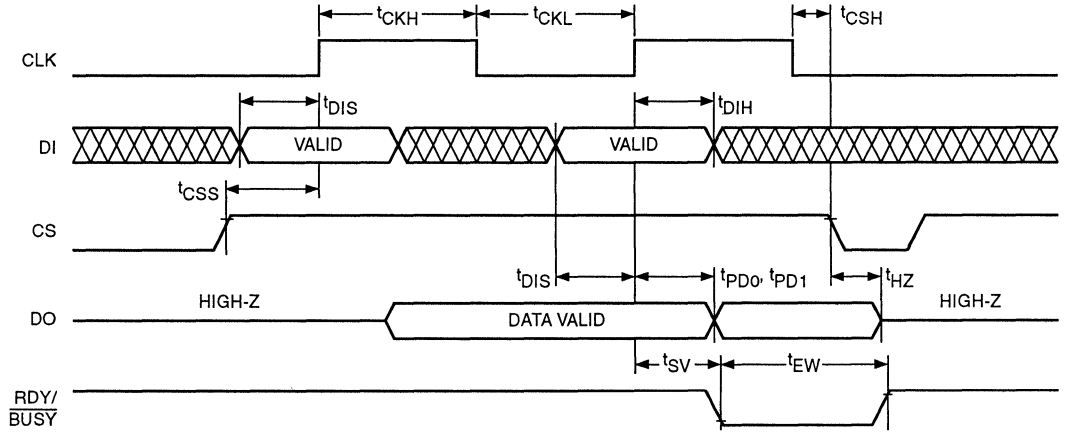


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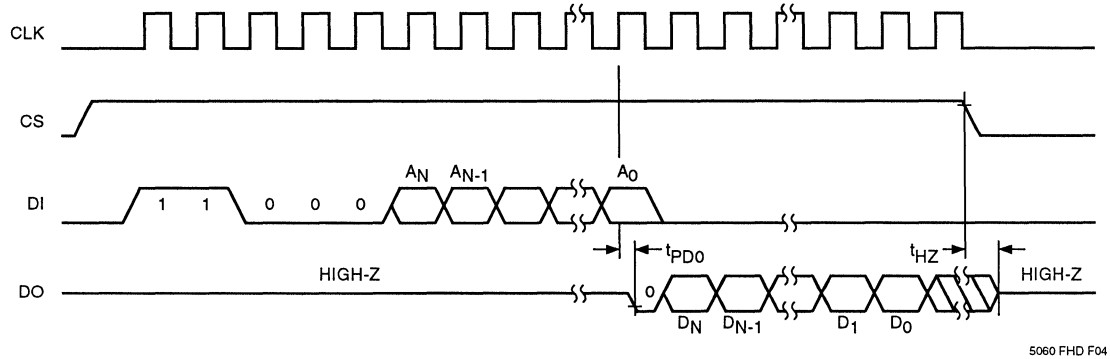
Figure 2. Read Instruction Timing(5)



5060 FHD F04

Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A7 and DN = D7. When x16 organization is selected, AN = A6 and DN = D15.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT35C202/CAT35C202I will come out of the high impedance state and, after sending an initial dummy zero bit (after a delay of t_{PDO} from the positive edge of the A_0 clock), will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the clock and are stable after the specified time delay (t_{PD0} or t_{PD1}). DO returns to High-Z after a delay of t_{HZ} from the negative going edge of CS.

Erase/Write Enable and Disable

The CAT35C202/CAT35C202I powers up in the write disabled state. Any write after power-up or after a EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWEN instruction is sent. The EWEN instruction can be used to disable all CAT35C202/CAT35C202I write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Write

After receiving a WRITE command, address and data, the RDY/$\overline{BUSY}$ pin goes low (after a delay of t_{SV} from the negative edge of the D_0 clock) indicating the self-clocking program/erase cycle is in progress. The program/erase pulse width (t_{EW}) is timed from the negative clock edge of the last data bit (D_0) and its completion is indicated by the RDY/$\overline{BUSY}$ pin returning to a high level. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before the WRITE command is sent.

5

Figure 3. Write Instruction Timing(5)

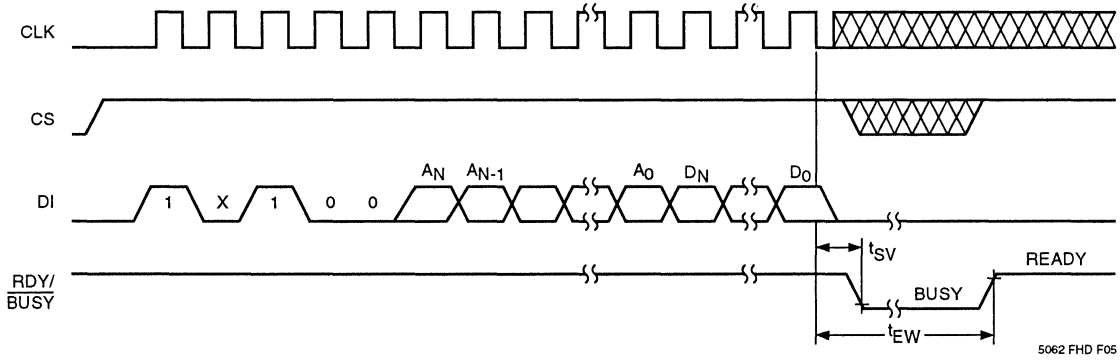
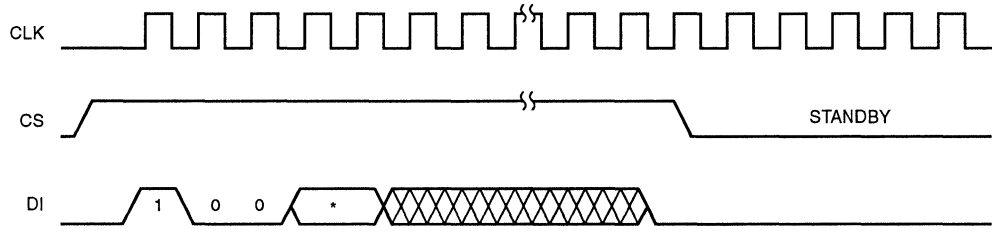


Figure 4. EWEN/EWDS Instruction Timing(5)



Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A7 and DN = D7. When x16 organization is selected, AN = A6 and DN = D15.

Erase All

After receiving an ERAL command and address the RDY/$\overline{BUSY}$ pin goes low (after a delay of t_{SV} from the negative edge of the D_0 clock) indicating the self-clocking program/erase cycle is in progress. The program/erase pulse width (t_{EW}) is timed from the negative clock edge of the last don't care bit and its completion is indicated by the RDY/$\overline{BUSY}$ pin returning to a high level. The clocking of the CLK pin is not necessary after the device has entered the self-clocking mode. Once cleared, the contents of all memory bits return to a logical "1" state.

Write All

Upon receiving a WRAL command, address and data, the RDY/$\overline{BUSY}$ pin goes low (after a delay of t_{SV} from the negative edge of the D_0 clock) indicating the self-clocking program/erase cycle is in progress. The program/erase pulse width (t_{EW}) is timed from the negative edge of the last data bit (D_0) and its completion is indicated by the RDY/$\overline{BUSY}$ pin returning to a high level. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. It IS necessary for all memory locations to be cleared before the WRAL command is executed.

Figure 5. ERAL Instruction Timing(5)

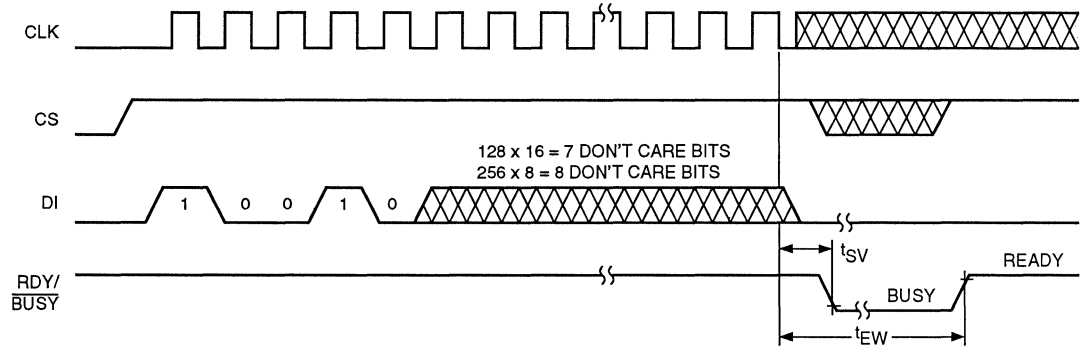


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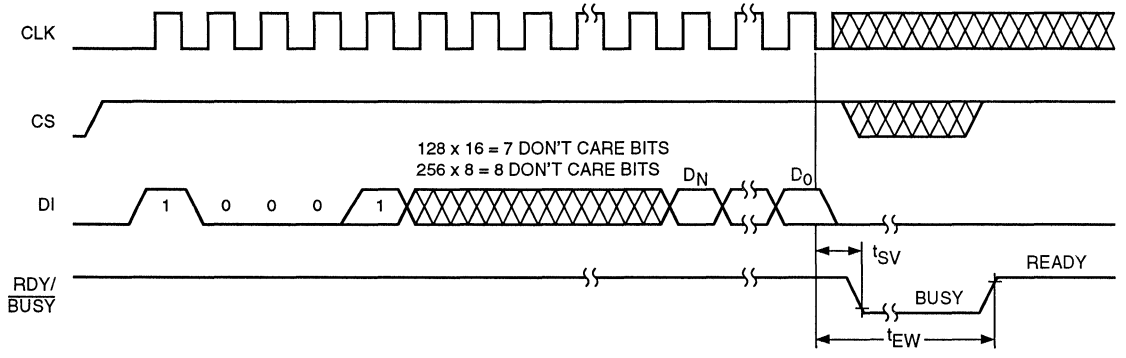
Figure 6. WRAL Instruction Timing(5)



5062 FHD F08

Note:
(5) The ORG pin is used to configure the device for x8 or x16 operation. When x8 organization is selected, AN = A7 and DN = D7. When x16 organization is selected, AN = A6 and DN = D15.

CATALYST SEMICONDUCTOR

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CAT35C704/CAT35C704I ..... 256 x 16, 512 x 8 ..... 4K-Bit 6-15

CAT33C804A-B/CAT33C804A-BI ..... 256 x 16, 512 x 8 ..... 4K-Bit 6-29

CAT35C804A-B/CAT35C804A-BI ..... 256 x 16, 512 x 8 ..... 4K-Bit 6-43

CATALYST SEMICONDUCTOR

CAT33C704/CAT33C704I

4K-Bit SECURE ACCESS SERIAL E²PROM

FEATURES

- Low Power CMOS Technology
- Single 3V Supply
- Password READ/WRITE Protection: 1 to 8 Bytes
- Memory Pointer WRITE Protection
- Sequential READ Operation
- 256 x16 or 512 x 8 Selectable Serial Memory
- High Speed Synchronous Protocol
- Operating Frequency: DC–1MHz
- Low Power Consumption:
  Active: 3mA
  Standby: 250µA
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

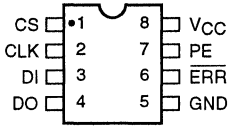
DESCRIPTION

The CAT33C704/CAT33C704I is a 4K bit Serial E²PROM that safeguards stored data from unauthorized access by use of a user selectable (1 to 8 byte) access code and a movable memory pointer. Two operating modes provide unprotected and password-protected operation allowing the user to configure the device as anything from a ROM to a fully protected no-access memory. The CAT33C704/CAT33C704I uses a unique serial-byte synchronous communication protocol and has a Sequential Read feature where data can be sequentially clocked out of the memory array. The device is available in 8 pin DIP or 16 pin SO packages.

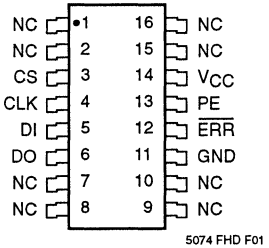
6

PIN CONFIGURATION

DIP Package



SO Package



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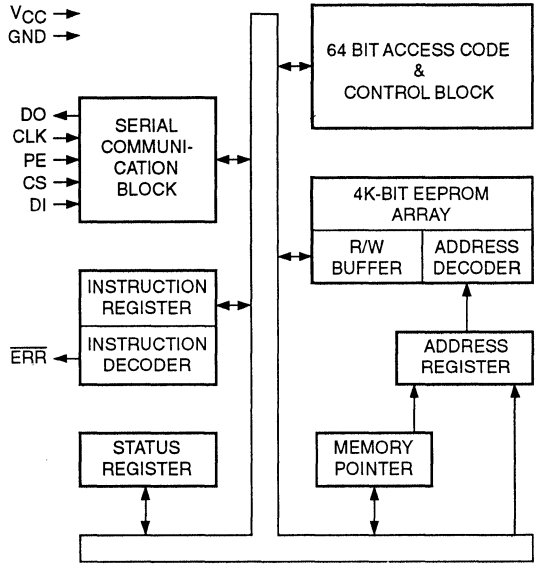
PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
DO(1)	Serial Data Output
CLK	Clock Input
DI(1)	Serial Data Input
PE	Parity Enable
$\overline{ERR}$	Error Indication Pin
VCC	+3V Power Supply
GND	Ground

Note:
(1) DI, DO may be tied together to form a common I/O.

BLOCK DIAGRAM



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TD 5072

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with
Respect to Ground(2) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation
Capability (T_a = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(3) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(4)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(4)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(4)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(4)(5)	Latch-up	100		mA	JEDEC Standard 17

D.C. CHARACTERISTICS

CAT33C704 T_A = 0°C to +70°C, V_{CC} = +3V ±10%,unless otherwise specified.
CAT33C704I T_A = –40°C to +85°C, V_{CC} = +3V ±10%,unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current (Operating)			3	mA	V_{CC} = 3.3V, CS = V_{CC} DO is Unloaded.
I_{SB}	Power Supply Current (Standby)			250	µA	V_{CC} = 3.3V, CS = 0V DI = 0V, CLK = 0V
V_{IL}	Input Low Voltage	–0.1		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –400µA
I_{LI}(6)	Input Leakage Current			2	µA	V_{IN} = 3.3V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 3.3V, CS = 0V

Note:
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) This parameter is tested initially and after a design or process change that affects the parameter.
(5) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(6) PE pin test conditions: $V_{IH} < V_{IN} < V_{IL}$

A.C. CHARACTERISTICS

CAT33C704 T_A = 0°C to +70°C, V_{CC} = +3V ±10%,unless otherwise specified.
CAT33C704I T_A = –40°C to +85°C, V_{CC} = +3V ±10%,unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	150			ns	
t_{CSH}	CS Hold Time	0			ns	C_L = 100pF
t_{DIS}	DI Setup Time	50			ns	V_{IN} = V_{IH} or V_{IL}
t_{DIH}	DI Hold Time	0			ns	V_{OUT} = V_{OH} or V_{OL}
t_{PD}	CLK to DO Delay			150	ns	
t_{HZ}(4) (7)	CLK to DO High-Z Delay			50	ns	
t_{EW}	Program/Erase Pulse Width			12	ms	
t_{CSL}	CS Low Pulse Width	300			ns	
t_{CKH}	CLK High Pulse Width	300			ns	
t_{CKL}	CLK Low Pulse Width	140			ns	
t_{SV}	$\overline{ERR}$ Output Delay			150	ns	C_L = 100pF
t_{VCCS}(4)	V_{CC} to CS Setup Time	5			µs	C_L = 100pF
t_{CSZ}(4)	CS to DO High-Z Delay			50	ns	
t_{CSD}	CS to DO Busy Delay			150	ns	
f_{CLK}	Maximum Clock Frequency	DC		1	MHz	

Note:
(4) This parameter is tested initially and after a design or process change that affects the parameter.
(7) t_{HZ} is measured from the falling edge of the clock to the time when the output is no longer driven.

PASSWORD PROTECTION

The CAT33C704/CAT33C704I is a 4K bit E^2PROM that features a password protection scheme to prevent unauthorized access to the information stored in the device. It contains an access code register which stores one to eight bytes of access code along with the length of that access code. Additionally, a memory pointer register stores the address that partitions the memory into protected and unprotected areas. As shipped from the factory, the device is unprogrammed and unprotected. The length of the access code is equal to zero and the memory pointer register points to location zero. Every byte of the device is fully accessible without an access code. Setting a password and moving the memory pointer register to cover all or part of the memory secures the device. Once secured, the memory is divided into a read/write area and a read-only area with the entry of a valid access code. If no access code is entered, the memory is divided into a read-only area and a non-access area. Figure 2 illlustrates this partitioning of the memory array.

WRITE PROTECTION

Another feature of the CAT33C704/CAT33C704I is WRITE-protection without the use of an access code. If the memory pointer register is set to cover all or part of the memory, without setting the access code register, the device may be divided into an area which allows full access, and an area which allows READ-only access. To write into the READ-only area, the user can override the memory pointer register for every WRITE instruction or he can simply move the address in the memory pointer register to uncover this area, and then write into the memory. This mechanism prevents inadvertent overwriting of important data in the memory without the use

Figure 1. A.C. Timing

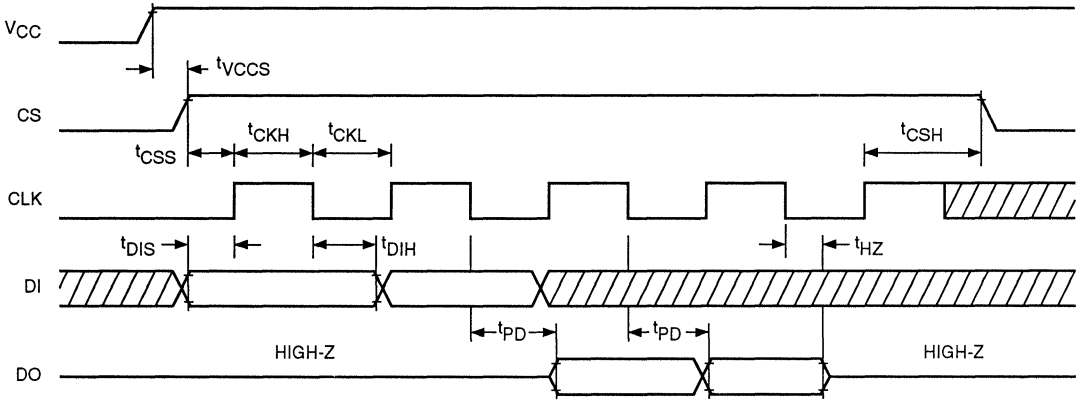

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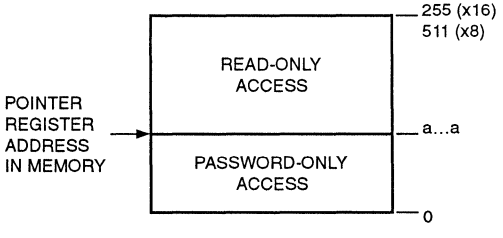
Figure 2. Secure Mode

ACCESS REGISTER: ACCESS CODE (1–8 BYTES)
ACCESS CODE LENGTH: 1 TO 8
MEMORY POINTER: a...a



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of an access code. Figure 3 illustrates this partitioning of the memory array.

READ SEQUENTIAL

To allow for convenient reading of blocks of contiguous data, the device has a READ SEQUENTIAL instruction which accepts a starting address of the block and continuously outputs data of subsequent addresses until the end of memory, or until Chip Select goes LOW.

The CAT33C704/CAT33C704I communicates with external devices via a synchronous serial communication protocol (SECS) that has a maximum transmission rate of 1 MHz. The data transmission may be a continuous stream of data or it can be packed by pulsing Chip Select LOW in between each packet of information. (Except for the SEQUENTIAL READ instruction where Chip Select must be held high).

PIN DESCRIPTIONS

CS

Chip Select is a TTL compatible input which, when set HIGH, allows normal operation of the device. Any time Chip Select is set LOW, it resets the device, terminating all I/O communication, and puts the output in a high impedance state. CS is used to reset the device if an error condition exists or to put the device in a power-down mode to minimize power consumption. It may also be used to frame data transmission in applications where the clock and data input have to be ignored from time to time. Although CS resets the device, it does not change the program/erase or the access-enable status, nor does it terminate a programming cycle once it has started. The program/erase and access-enable operations, once enabled, will remain enabled until specific disabling instructions are sent or until power is removed.

Figure 3. Unprotected Mode(8)

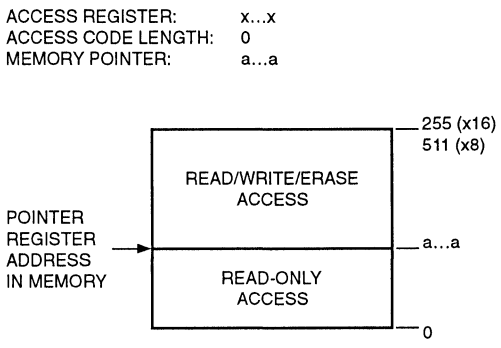

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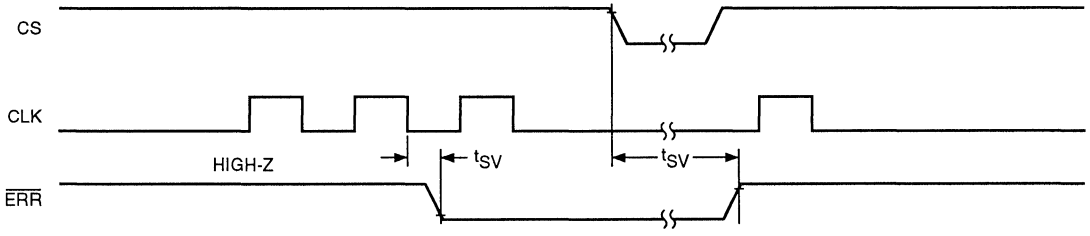
Figure 4. $\overline{ERR}$ Pin Timing



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Note:
(8) x = DON'T CARE; a = ADDRESS BIT.

CLK

The System Clock is a TTL compatible input pin that allows operation of the device over a frequency range of DC to 1 MHz.

DI

The Data Input pin is TTL compatible and accepts data and instructions in a serial format. Each instruction must begin with "1" as a start bit. The device will accept as many bytes as an instruction requires, including both data and address bytes. With the SECS protocol, extra bits will be disregarded if they are "0"s and misinterpreted as the next instruction if they are "1"s. An instruction error will cause the device to abort operation and all I/O communication will be terminated until a reset is received.

DO

The Data Output pin is a tri-state TTL compatible output. It is normally in a high impedance state unless a READ or an ENABLE BUSY instruction is executed. Following the completion of a 16 bit or 8 bit data stream, the output will return to the high impedance state. During a program/erase cycle, if the ENABLE BUSY instruction has been previously executed, the output will stay LOW while the device is BUSY, and it will be set HIGH when the program/erase cycle is completed. DO will stay HIGH until the completion of the next instruction's opcode and, if the next instruction is a READ, DO will output the appropriate data at the end of the instruction. If the ENABLE BUSY instruction has not been previously executed, DO will stay in a high impedance state. DO will

Figure 5. Program/Erase Timing

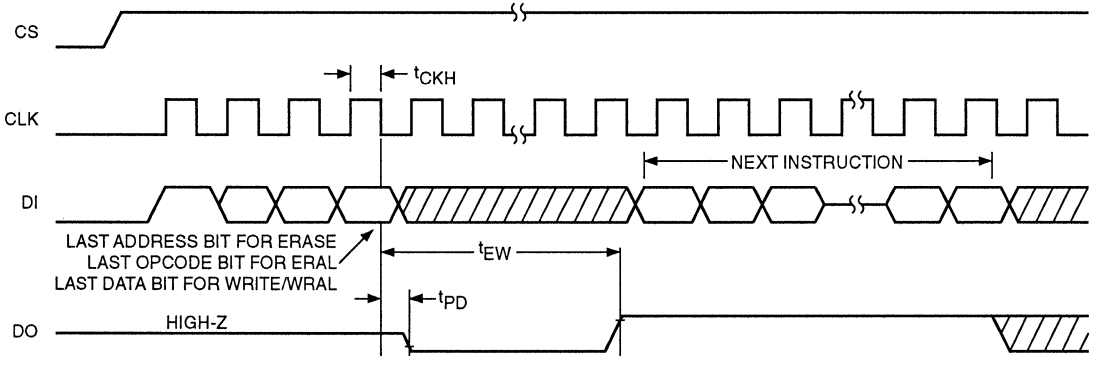

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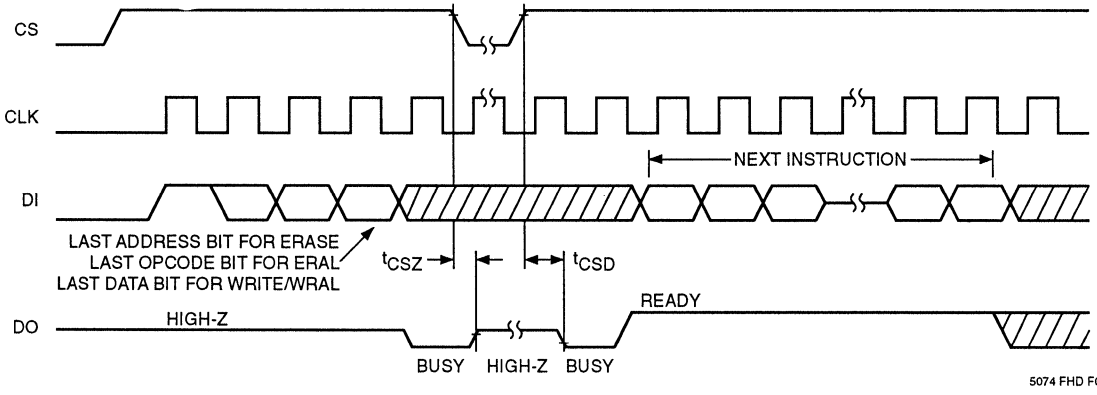
Figure 6. CS to DO Status Timing



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also go to the high impedance state if an error condition is detected. If the ENABLE BUSY instruction has not been executed, to determine whether the device is in a program/erase cycle or in an error condition, a READ STATUS instruction may be entered. When the device is in a program/erase cycle it will output an 8 bit status word. If it does not, it is in an error condition.

PE

The Parity Enable pin is a TTL compatible input. If the PE pin is set HIGH, the device will be configured to communicate using even parity, and if the pin is set LOW, it will use no parity. In this case, instructions or data that include parity bits will not be interpreted correctly. Note: The PE input is internally pulled down to GND (i.e. default = no parity). As with all CMOS devices, CS, CLK and DI inputs must be connected to either HIGH or LOW, and not left floating.

$\overline{ERR}$

The Error indication pin is an open drain output. If either an instruction or parity error exists, the $\overline{ERR}$ pin will output a "0" until the device is reset. This can be done by pulsing CS LOW.

Figure 7. Read Timing

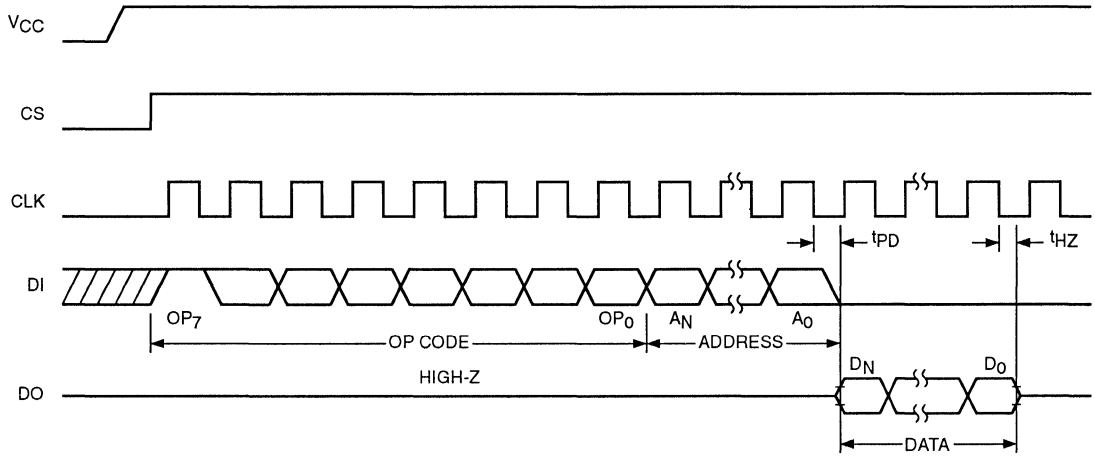

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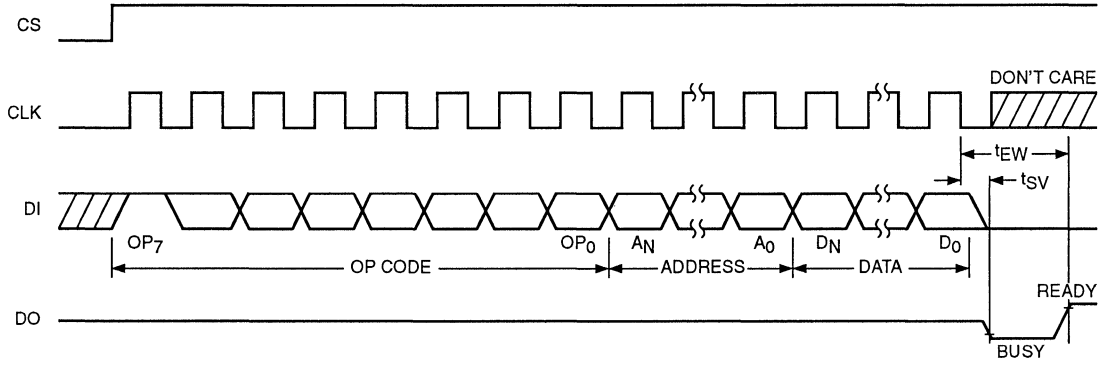
Figure 8. Write Timing



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DEVICE OPERATION

INSTRUCTIONS

The CAT33C704/CAT33C704I instruction set includes 19 instructions.

Six instructions are related to security or write protection:

DISAC	Disable Access
ENAC	Enable Access
MACC	Modify Access Code
OVMPR	Override Memory Pointer Register
RMPR	Read Memory Pointer Register
WMPR	Write Memory Pointer Register

Six instructions are READ/WRITE/ERASE instructions:

ERAL	Clear All Locations
ERASE	Clear Memory Locations
READ	Read Memory
RSEQ	Read Sequentially
WRAL	Write All
WRITE	Write memory

Note: All write instructions will automatically perform a clear before writing data.

Seven instructions are used as control and status functions:

DISBSY	Disable Busy
ENBSY	Enable Busy
EWEN	Program/Erase Enable
EWDS	Program/Erase Disable
NOP	No Operations
ORG	Select Memory Organization
RSR	Read Status Register

UNPROTECTED MODE

As shipped from the factory, the CAT33C704/CAT33C704I is in the unprotected mode. The access code length is set to 0, and the memory pointer is at address 00 hex. While in this mode, any portion of the E^2PROM array can be read or written to without an access code. A portion of the memory may be protected from any write or clear operation by setting the memory pointer to the appropriate address via the WMPR (Write Memory Pointer Register) instruction:

WMPR [address]

Figure 9. EWEN/EWDS Timing

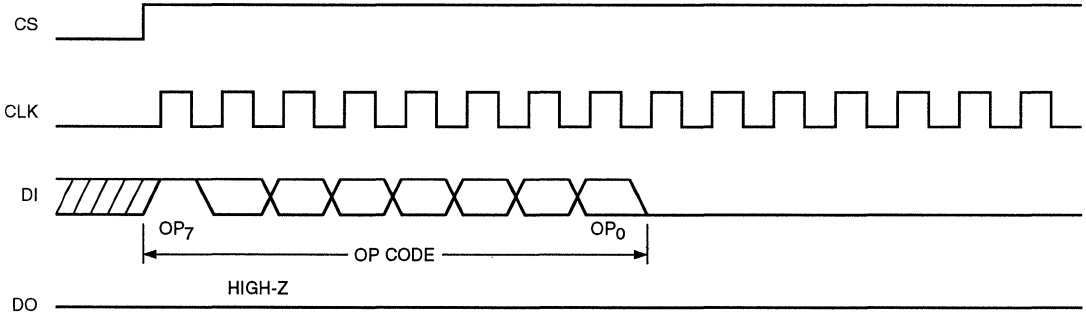
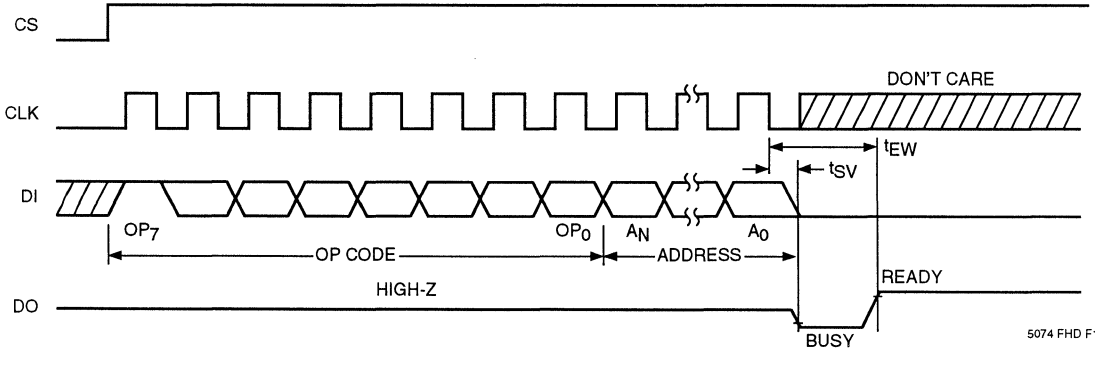


Figure 10. Erase Timing



As shown previously in Figure 3, memory locations below the address set in the memory pointer will be program/erase protected. Thus, unintentional clearing or writing of data in this area will be prevented, while memory locations at or above the protected area still allow full access. This protection does not apply to the ERAL and WRAL commands which are not blocked by the memory pointer.

SECURE MODE

As shown previously in Figure 2, in the secure mode, memory locations at or above the address set in the memory pointer allow READ-only access. Memory locations below that address will require an access code before they can be accessed. The secure mode is activated with an MACC (Modify Access Code) instruction followed by a user access code which can be one to eight bytes in length.

EWEN
MACC [old code][new code][new code]

The EWEN instruction enables the device to perform program/erase operations. The new access code must be entered twice for verification. If the device already has an access code, the old access code must be entered before the new access code can be accepted. The length of the password is incorporated into the MACC portion of the instruction.

Once the secure mode is activated, access to memory locations is under software control. Access (read, write, and clear instructions) to the memory locations below the address in the memory pointer is allowed only if the ENAC (Enable Access) instruction followed by the correct access code has been previously executed.

ENAC [access code]
EWEN
WRITE [address][data]

The ENAC instruction, along with the access code, enables access to the protected area of the device. The EWEN instruction enables execution of the program/erase operations. This portion of the memory is otherwise inaccessible for any operation. Read-only access is allowed without the access code for memory locations at or above the address in the memory pointer.

The access code can be changed by the following instruction:

ENAC [old access code]
EWEN
MACC [old code][new code][new code]

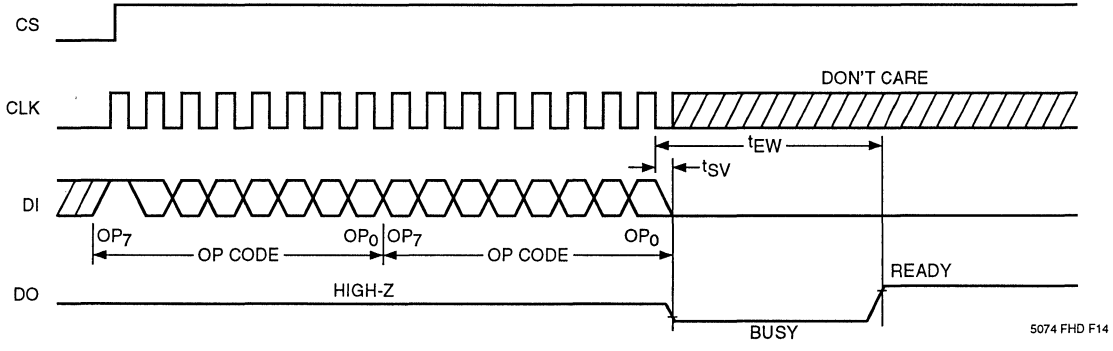
A two-tier protection scheme is implemented to protect data against inadvertent clearing or writing. To write to the memory, an EWEN (Program/Erase Enable) must first be issued. The CAT33C704/CAT33C704I will now allow program/erase operations to be performed only on memory locations at or above the address set in the memory pointer. The remaining portion of the memory is still protected. To override this protection, an OVMPR (Override Memory Pointer Register—see Memory Pointer Register) must be issued for every program/erase instruction which accesses the protected area:

ENAC [access code]
EWEN
OVMPR
WRITE [address][data]

As an alternative to the OVMPR instruction, the WMPR (Write Memory Pointer Register) instruction may be used to move the memory pointer address to uncover the area where writing is to be performed:

ENAC [access code]
EWEN
WMPR [address]
WRITE [address][data]

Figure 11. ERAL Timing



As shipped from the factory, the device is in the unprotected mode. The length of the access code is user selectable from a minimum of one byte to a maximum of eight bytes (> 1.84×10^{19} combinations). Loading a zero-length access code will disable protection.

MEMORY POINTER REGISTER

The memory pointer enables the user to segment the E^2PROM array into two sections. In the unprotected mode, the array can be segmented between read-only and full access, while in the secure mode, the memory may be segmented between read-only access and password-only access. Three instructions are dedicated to the memory pointer operations. The first one is WMPR (Write Memory Pointer Register). This instruction, followed by an address, will load the memory pointer register with a new address. This address will be stored in the E^2PROM and can be modified only by another WMPR instruction. The second instruction is OVMPR (Override Memory Pointer Register) which allows a single program/erase to be performed to memory locations below the address set in the memory pointer. This instruction allows the user to modify data in a segmented array without having to move the memory pointer. Once the operation is complete, the device returns to the protected mode. If the device is in the secure mode both of these instructions require the ENAC instruction and a valid access code prior to their execution. The third instruction is the RMPR (Read Memory Pointer Register) which will place the current contents of the register in the serial output buffer.

SECS PROTOCOL

The CAT33C704/CAT33C704I implements the SECS communication protocol which uses an 8 bit transmission format. As shown in Figures 7–13, all instructions are 8 bits long with the first bit being the start bit and the following 7 bits being the op-code. Data can be one or two bytes long depending on the instruction and the memory array organization. Each address is one or two bytes long depending on the organization of the memory array. In this protocol, the transmission of the MSB is always first and the LSB last. The CS (Chip Select) pin of the CAT33C704/CAT33C704I may be used to frame the data transmission packet or it may be set HIGH for the entire duration of operation. If an error in op-code or parity (if enabled) has been detected, the $\overline{ERR}$ output will be set LOW and the CAT33C704/CAT33C704I will stop receiving and sending data until CS is toggled from HIGH to LOW to HIGH again. Alternatively, an error condition may be detected by interrogating the device for a status word. If an error condition has been detected, the DO (Data Output) pin will not respond. DO may be programmed to become tri-stated or to output a RDY/$\overline{BUSY}$ status flag during program/erase cycles (see ENBSY instruction).

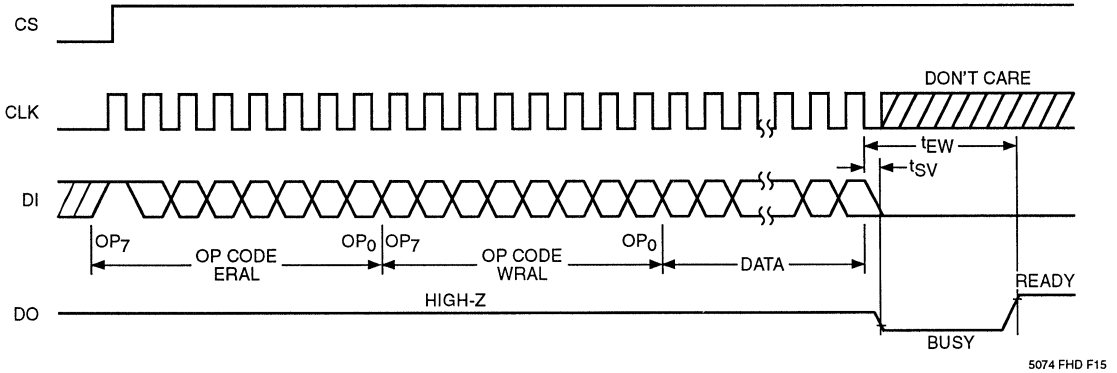
STATUS REGISTER

An eight bit status register is provided to allow the user to determine the status of the CAT33C704/CAT33C704I. The contents of the first three bits of the register are 101 which allows the user to quickly determine the condition of the device. The next three bits indicate the status of the device; they are parity error, instruction error and RDY/$\overline{BUSY}$ status. The last two bits are reserved for future use.

CLEAR ALL AND WRITE ALL

As a precaution, the ERAL instruction has to be entered twice before it is executed. This measure is required as a redundancy check on the incoming instruction for possible transmission errors. The WRAL instruction

Figure 12. WRAL Timing



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requires sending an ERAL first (this sets a flag only) and then the WRAL instruction. The CAT33C704/CAT33C704I will accept the following commands:

ERAL	**ERAL**	An ERAL will be executed
ERAL	**WRAL**	A WRAL will be executed

Both the ERAL and WRAL commands will program/erase the entire array and will not be blocked by the memory pointer.

THE PARITY BIT

The SECS protocol supports an even parity bit if the PE pin of the device is set HIGH, otherwise, there is no parity. If PE is set LOW and the incoming instruction contains a parity bit, it may be interpreted as the start bit of the next instruction. When PE is HIGH, the CAT33C704/CAT33C704I expects a parity bit at the end of every incoming instruction packet. For example, the RSEQ instruction will look like this:

1100 1011
A15...A8
A7...A0 P

The device then outputs data continuously until it reaches the end of the memory. The last byte of data contains 9 bits. The ninth bit is the parity bit calculated over the entire transmitted data packet. The RSEQ instruction may be terminated at any time by bringing CS low; the output will then go to high impedance.

SYSTEM ERRORS

Whenever an error occurs, be it an instruction error (unknown instruction), or parity error (perhaps caused by transmission error), the device will stop its operation. To return to normal operation, the device must be reset by pulsing CS LOW and then set back to HIGH. Resetting the device will not affect the ENAC, EWEN and ENBSY status. The error may be determined by entering the READ STATUS REGISTER (RSR) instruction immediatly following the reset. The status output is an 8 bit word with the first three bits being 101. This three bit pattern indicates that the device is functioning normally. The fourth bit is "1" if a parity error occurred. The fifth bit is a "1" if an instruction error occurred. The sixth bit is a "1" if the device is in a program/erase cycle. The last two bits are reserved for future use.

The reason for the "101" pattern is to distinguish between an error conditon (DO tri-stated) and a device busy status. If an error condition exists, it will not respond to any input instruction from DI. However, if the device is in a program/erase cycle, it responds to the RSR instruction by outputting "101 00100". If RSR is executed at the end of a program/erase cycle, the output will be "101000 00".

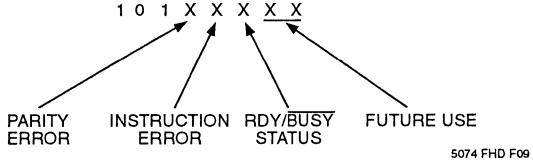
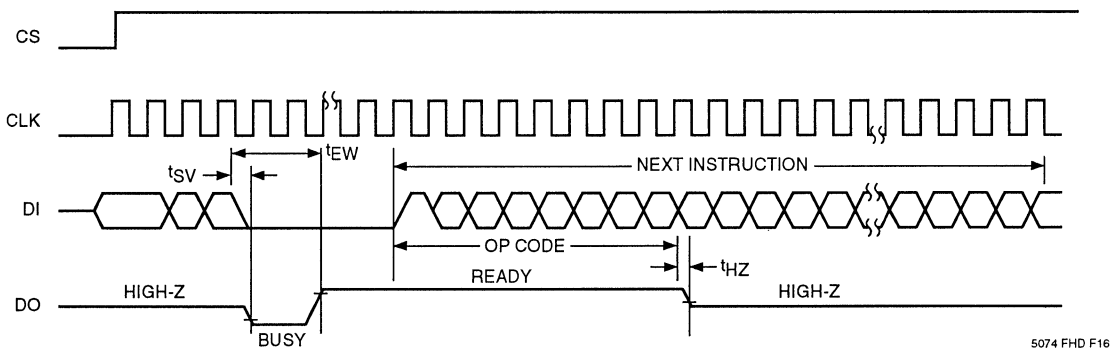


Figure 13. Next Instruction Timing(9)



Note:
(9) DO will be high impedance after the last instruction bit has been clocked in, unless the instruction is RSR or RMPR, in which case, DO will become active.

INSTRUCTION SET

DISAC Disable Access

1000	1000

This instruction will lock the memory from all program/erase operations regardless of the contents of the memory pointer. A write can be accomplished only by first entering the ENAC instruction followed by a valid access code.

ENAC Enable Access

1100	0101	[Access Code]

In the protected mode, this instruction, followed by a valid access code, unlocks the device for read/write/clear access.

WMPR Write Memory Pointer Register

1100	0100	[A15–A8] [A7–A0] *(x8 organization)*
1100	0100	[A7–A0] *(x16 organization)*

The WMPR instruction followed by 8 or 16 bits of address (depending on the organization) will move the pointer to the newly specified address.

MACC Modify Access Code

1101	[Length] [Old code] [New code] [New code]

This instruction requires the user to enter the old access code, if one was set previously, followed by the new access code and a re-entry of the new access code for verification. Within the instruction format, the variable [Length] designates the length of the access code as the following:

[Length] = [0] No access code. Set device to unprotected mode.

[Length] = [1–8] Length of access code is 1 to 8 bytes.

[Length] = [>8] Illegal number of bytes. The CAT33C704/CAT33C704I will ignore the rest of the transmission.

RMPR Read Memory Pointer Register

1100	1010

Output the content of the memory pointer register to the serial output port.

OVMPR Override Memory Pointer Register

1000	0011

Override the memory protection for the next instruction.

READ Read Memory

1100	1001	[A15–A8] [A7–A0] *(x8 organization)*
1100	1001	[A7–A0] *(x16 organization)*

Output the contents of the addressed memory location to the serial port.

WRITE Write Memory

1100	0001	[A15–A8] [A7–A0] [D7–D0] *(x8 organization)*
1100	0001	[A7–A0] [D15–D8] [D7–D0] *(x16 organization)*

Write the 8 bit or 16 bit data to the addressed memory location. After the instruction, address, and data have been entered, the self-timed program/erase cycle will start. The addressed memory location will be erased before data is written. The DO pin may be used to output the RDY/$\overline{\text{BUSY}}$ status by having previously entered the ENBSY instruction. During the program/erase cycle, DO will output a LOW for BUSY during this cycle and a HIGH for READY after the cycle has been completed.

ERASE Clear Memory

1100	0000	[A15–A8] [A7–A0] *(x8 organization)*
1100	0000	[A7–A0] *(x16 organization)*

Erase data in the specified memory location (set memory to "1"). After the instruction and the address have been entered, the self-timed clear cycle will start. The DO pin may be used to output the RDY/$\overline{\text{BUSY}}$ status by having previously entered the ENSBY instruction. During the clear cycle, DO will output a LOW for BUSY during this cycle and a HIGH for ready after the cycle has been completed.

ERAL Clear All

1000	1001
1000	1001

Erase the data of all memory locations (all cells set to "1"). For protection against inadvertent chip clear, the ERAL instruction is required to be entered twice.

WRAL Write All

1000	1001	
1100	0011	[D15–D8] [D7–D0] *(x16 organization)*
1000	1001	
1100	0011	[D7–D0] *(x8 organization)*

Write one or two bytes of data to all memory locations. An ERAL will be automatically performed before the

WRAL is executed. For protection against inadvertent clearing or writing of data, the ERAL instruction is required to be entered preceding the WRAL instruction.

RSEQ Read Sequentially

1100	1011	[A15–A8] [A7–A0] *(x8 organization)*

1100	1011	[A7–A0] *(x16 organization)*

Read memory starting from specified address, sequentially to the highest address or until CS goes LOW. The instruction is terminated when CS goes LOW.

ENBSY Enable Busy

1000	0100

Enable the status indicator on DO during program/erase cycle. DO goes LOW then HIGH once the write cycle is complete. DO will go to HIGH-Z at the end of the next op code transmission.

DISBSY Disable Busy

1000	0101

Disable the status indicator on DO during program/erase cycle.

EWEN Program/Erase Enable

1000	0001

Enable program/erase to be performed on non-protected portion of memory. This instruction must be entered before any program/erase instruction will be carried out. Once entered, it will remain valid until power-down or an EWDS (Program/Erase Disable) is executed.

EWDS Program/Erase Disable

1000	0010

Disable all write and clear functions.

ORG Select Memory Organization

1000	011R	*(where R = 0 or 1)*

Set memory organization to 512 x 8 if R = 0.

Set memory organization to 256 x 16 if R = 1.

RSR Read Status Register

1100	1000

Output the contents of the 8 bit status register. The contents of the first three bits of the register are 101, which allows the user to quickly determine whether the device is listening or is in an error condition. The next three bits indicate parity error, instruction error and RDY/$\overline{\text{BUSY}}$ status. The last two bits are reserved for future use.

NOP No Operation

1000	0000

No Operation.

CAT35C704/CAT35C704I

4K-Bit SECURE ACCESS SERIAL E²PROM

FEATURES

- Low Power CMOS Technology
- Password READ/WRITE Protection: 1 to 8 Bytes
- Memory Pointer WRITE Protection
- Sequential READ Operation
- 256 x16 or 512 x 8 Selectable Serial Memory
- High Speed Synchronous Protocol
- Operating Frequency: DC–3MHz
- Low Power Consumption:
  –Active: 3mA
  –Standby: 250µA
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

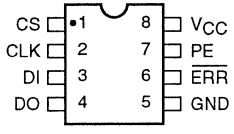
DESCRIPTION

The CAT35C704/CAT35C704I is a 4K bit Serial E²PROM that safeguards stored data from unauthorized access by use of a user selectable (1 to 8 byte) access code and a movable memory pointer. Two operating modes provide unprotected and password-protected operation allowing the user to configure the device as anything from a ROM to a fully protected no-access memory. The CAT35C704/CAT35C704I uses a unique serial-byte synchronous communication protocol and has a Sequential Read feature where data can be sequentially clocked out of the memory array. The device is available in 8 pin DIP or 16 pin SO packages.

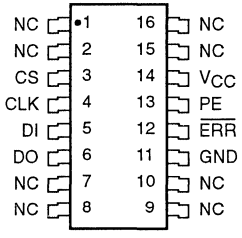
6

PIN CONFIGURATION

DIP Package



SO Package



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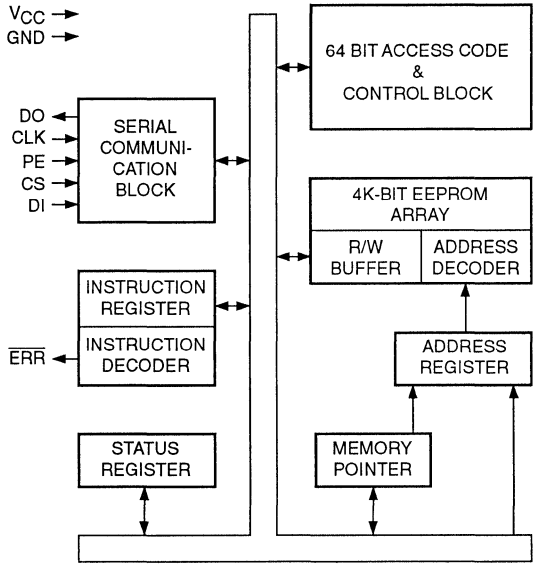
PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
DO(1)	Serial Data Output
CLK	Clock Input
DI(1)	Serial Data Input
PE	Parity Enable
$\overline{ERR}$	Error Indication Pin
VCC	+5V Power Supply
GND	Ground

Note:
(1) DI, DO may be tied together to form a common I/O.

BLOCK DIAGRAM



5074 FHD F02

TD 5074

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with Respect to Ground(2) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (T_a = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(3) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(4)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(4)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(4)	ESD Susceptability	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(4)(5)	Latch-up	100		mA	JEDEC Standard 17

D.C. CHARACTERISTICS

CAT35C704 T_A = 0°C to +70°C, V_{CC} = +5V ±10%,unless otherwise specified.
CAT35C704I T_A = –40°C to +85°C, V_{CC} = +5V ±10%,unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current (Operating)			3	mA	V_{CC} = 5.5V, CS = V_{CC} DO is Unloaded.
I_{SB}	Power Supply Current (Standby)			250	µA	V_{CC} = 5.5V, CS = 0V DI = 0V, CLK = 0V
V_{IL}	Input Low Voltage	–0.1		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –400µA
I_{LI}(6)	Input Leakage Current			2	µA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 5.5V, CS = 0V

Note:
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) This parameter is tested initially and after a design or process change that affects the parameter.
(5) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(6) PE pin test conditions: $V_{IH} < V_{IN} < V_{IL}$

A.C. CHARACTERISTICS

CAT35C704 T_A = 0°C to +70°C, V_{CC} = +5V ±10%,unless otherwise specified.
CAT35C704I T_A = –40°C to +85°C, V_{CC} = +5V ±10%,unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSS}	CS Setup Time	150			ns	
t_{CSH}	CS Hold Time	0			ns	C_L = 100pF
t_{DIS}	DI Setup Time	50			ns	$V_{IN} = V_{IH}$ or V_{IL}
t_{DIH}	DI Hold Time	0			ns	$V_{OUT} = V_{OH}$ or V_{OL}
t_{PD}	CLK to DO Delay			150	ns	
t_{HZ}(4) (7)	CLK to DO High-Z Delay			50	ns	
t_{EW}	Program/Erase Pulse Width			12	ms	
t_{CSL}	CS Low Pulse Width	200			ns	
t_{CKH}	CLK High Pulse Width	165			ns	
t_{CKL}	CLK Low Pulse Width	100			ns	
t_{SV}	$\overline{ERR}$ Output Delay			150	ns	C_L = 100pF
t_{VCCS}(4)	V_{CC} to CS Setup Time	5			µs	C_L = 100pF
t_{CSZ}(4)	CS to DO High-Z Delay			50	ns	
t_{CSD}	CS to DO Busy Delay			150	ns	
f_{CLK}	Maximum Clock Frequency	DC		3	MHz	

Note:
(4) This parameter is tested initially and after a design or process change that affects the parameter.
(7) t_{HZ} is measured from the falling edge of the clock to the time when the output is no longer driven.

6

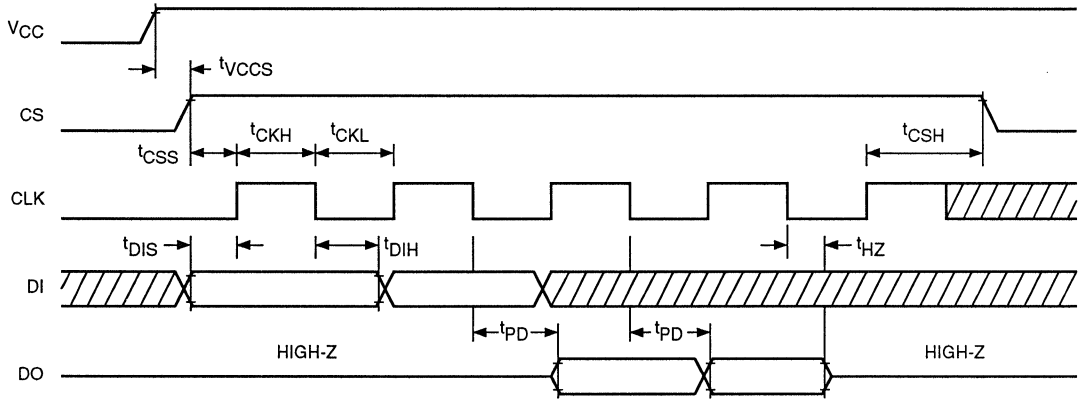
PASSWORD PROTECTION

The CAT35C704/CAT35C704I is a 4K bit E^2PROM that features a password protection scheme to prevent unauthorized access to the information stored in the device. It contains an access code register which stores one to eight bytes of access code along with the length of that access code. Additionally, a memory pointer register stores the address that partitions the memory into protected and unprotected areas. As shipped from the factory, the device is unprogrammed and unprotected. The length of the access code is equal to zero and the memory pointer register points to location zero. Every byte of the device is fully accessible without an access code. Setting a password and moving the memory pointer register to cover all or part of the memory secures the device. Once secured, the memory is divided into a read/write area and a read-only area with the entry of a valid access code. If no access code is entered, the memory is divided into a read-only area and a non-access area. Figure 2 illlustrates this partitioning of the memory array.

WRITE PROTECTION

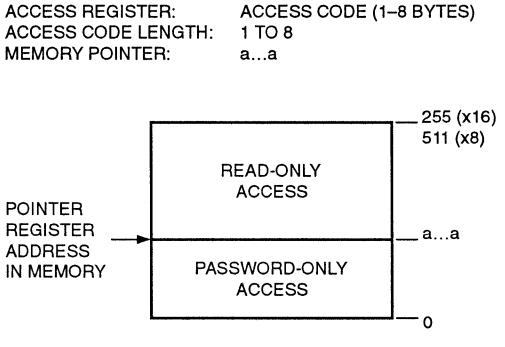
Another feature of the CAT35C704/CAT35C704I is WRITE-protection without the use of an access code. If the memory pointer register is set to cover all or part of the memory, without setting the access code register, the device may be divided into an area which allows full access, and an area which allows READ-only access. To write into the READ-only area, the user can override the memory pointer register for every WRITE instruction or he can simply move the address in the memory pointer register to uncover this area, and then write into the memory. This mechanism prevents inadvertent overwriting of important data in the memory without the use

Figure 1. A.C. Timing



5074 FHD F03

Figure 2. Secure Mode



5074 FHD F04

of an access code. Figure 3 illustrates this partitioning of the memory array.

READ SEQUENTIAL

To allow for convenient reading of blocks of contiguous data, the device has a READ SEQUENTIAL instruction which accepts a starting address of the block and continuously outputs data of subsequent addresses until the end of memory, or until Chip Select goes LOW.

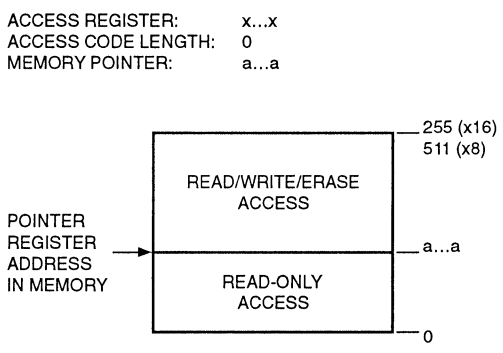
The CAT35C704/CAT35C704I communicates with external devices via a synchronous serial communication protocol (SECS) that has a maximum transmission rate of 3 MHz. The data transmission may be a continuous stream of data or it can be packed by pulsing Chip Select LOW in between each packet of information. (Except for the SEQUENTIAL READ instruction where Chip Select must be held high).

PIN DESCRIPTIONS

CS

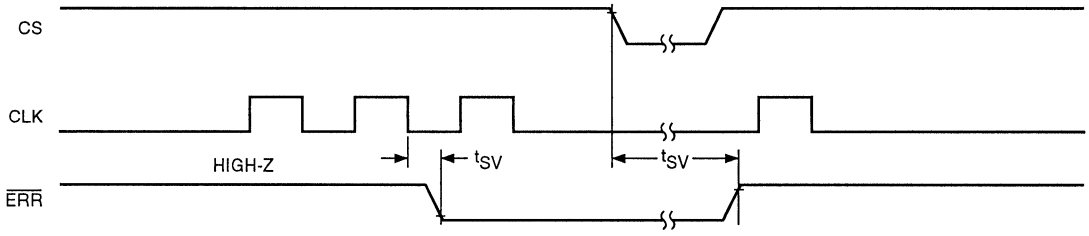
Chip Select is a TTL compatible input which, when set HIGH, allows normal operation of the device. Any time Chip Select is set LOW, it resets the device, terminating all I/O communication, and puts the output in a high impedance state. CS is used to reset the device if an error condition exists or to put the device in a power-down mode to minimize power consumption. It may also be used to frame data transmission in applications where the clock and data input have to be ignored from time to time. Although CS resets the device, it does not change the program/erase or the access-enable status, nor does it terminate a programming cycle once it has started. The program/erase and access-enable operations, once enabled, will remain enabled until specific disabling instructions are sent or until power is removed.

Figure 3. Unprotected Mode(8)



5074 FHD F05

Figure 4. $\overline{ERR}$ Pin Timing



5074 FHD F06

Note:
(8) x = DON'T CARE; a = ADDRESS BIT.

CLK

The System Clock is a TTL compatible input pin that allows operation of the device over a frequency range of DC to 3 MHz.

DI

The Data Input pin is TTL compatible and accepts data and instructions in a serial format. Each instruction must begin with "1" as a start bit. The device will accept as many bytes as an instruction requires, including both data and address bytes. With the SECS protocol, extra bits will be disregarded if they are "0"s and misinterpreted as the next instruction if they are "1"s. An instruction error will cause the device to abort operation and all I/O communication will be terminated until a reset is received.

DO

The Data Output pin is a tri-state TTL compatible output. It is normally in a high impedance state unless a READ or an ENABLE BUSY instruction is executed. Following the completion of a 16 bit or 8 bit data stream, the output will return to the high impedance state. During a program/erase cycle, if the ENABLE BUSY instruction has been previously executed, the output will stay LOW while the device is BUSY, and it will be set HIGH when the program/erase cycle is completed. DO will stay HIGH until the completion of the next instruction's opcode and, if the next instruction is a READ, DO will output the appropriate data at the end of the instruction. If the ENABLE BUSY instruction has not been previously executed, DO will stay in a high impedance state. DO will

Figure 5. Program/Erase Timing

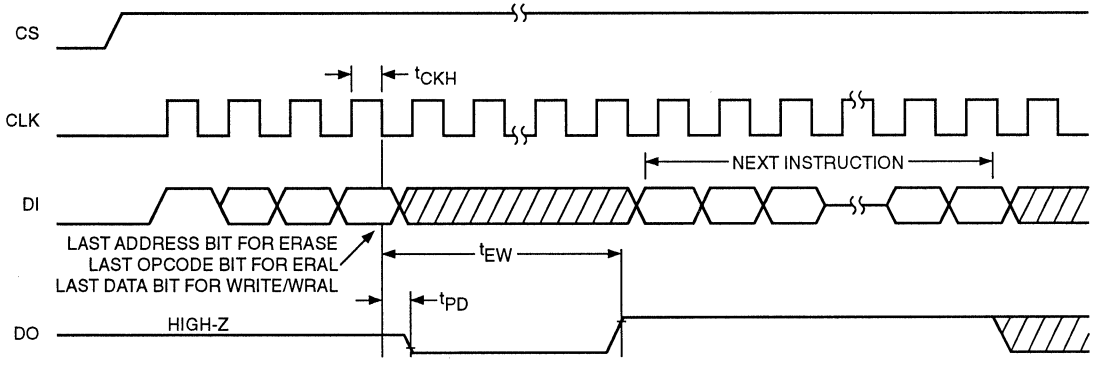
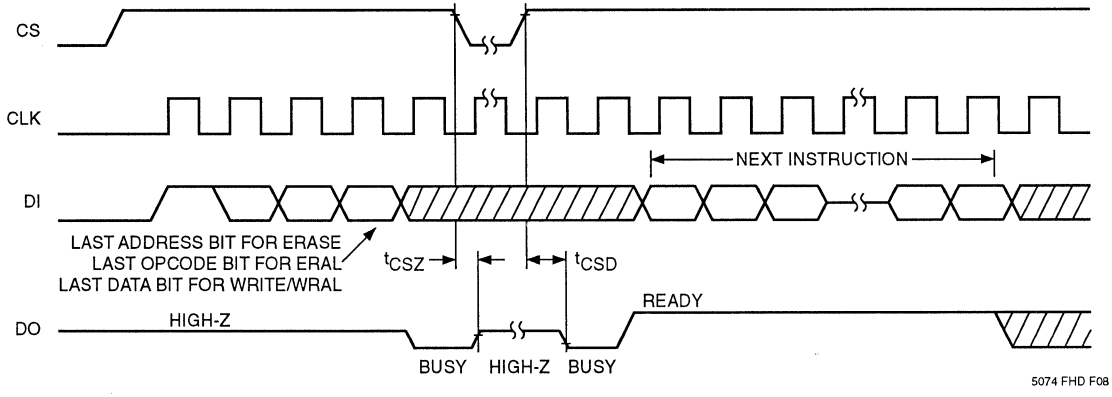


Figure 6. CS to DO Status Timing



also go to the high impedance state if an error condition is detected. If the ENABLE BUSY instruction has not been executed, to determine whether the device is in a program/erase cycle or in an error condition, a READ STATUS instruction may be entered. When the device is in a program/erase cycle it will output an 8 bit status word. If it does not, it is in an error condition.

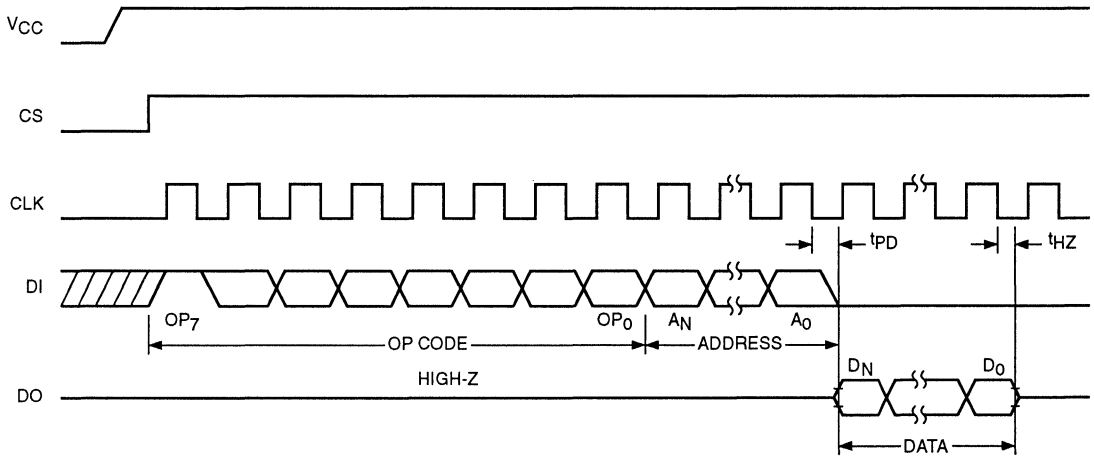
PE

The Parity Enable pin is a TTL compatible input. If the PE pin is set HIGH, the device will be configured to communicate using even parity, and if the pin is set LOW, it will use no parity. In this case, instructions or data that include parity bits will not be interpreted correctly. Note: The PE input is internally pulled down to GND (i.e. default = no parity). As with all CMOS devices, CS, CLK and DI inputs must be connected to either HIGH or LOW, and not left floating.

$\overline{ERR}$

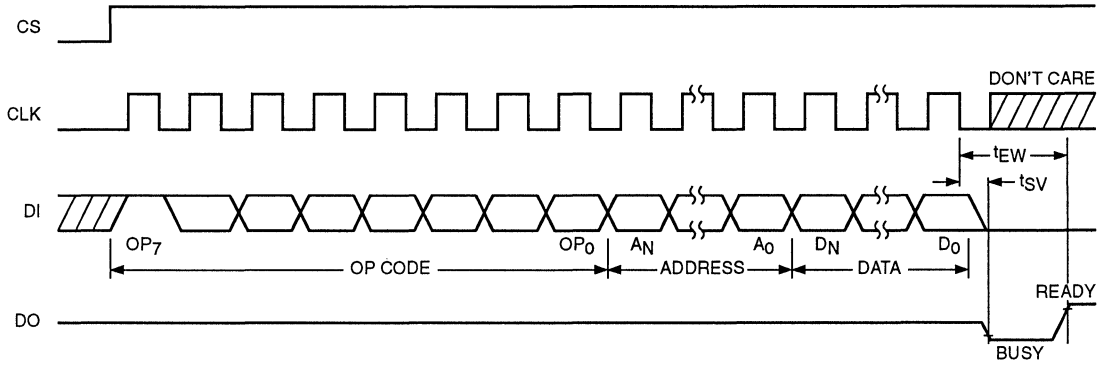
The Error indication pin is an open drain output. If either an instruction or parity error exists, the $\overline{ERR}$ pin will output a "0" until the device is reset. This can be done by pulsing CS LOW.

Figure 7. Read Timing



5074 FHD F10

Figure 8. Write Timing



5074 FHD F11

DEVICE OPERATION

INSTRUCTIONS

The CAT35C704/CAT35C704I instruction set includes 19 instructions.

Six instructions are related to security or write protection:

DISAC	Disable Access
ENAC	Enable Access
MACC	Modify Access Code
OVMPR	Override Memory Pointer Register
RMPR	Read Memory Pointer Register
WMPR	Write Memory Pointer Register

Six instructions are READ/WRITE/ERASE instructions:

ERAL	Clear All Locations
ERASE	Clear Memory Locations
READ	Read Memory
RSEQ	Read Sequentially
WRAL	Write All
WRITE	Write memory

Note: All write instructions will automatically perform a clear before writing data.

Seven instructions are used as control and status functions:

DISBSY	Disable Busy
ENBSY	Enable Busy
EWEN	Program/Erase Enable
EWDS	Program/Erase Disable
NOP	No Operations
ORG	Select Memory Organization
RSR	Read Status Register

UNPROTECTED MODE

As shipped from the factory, the CAT35C704/CAT35C704I is in the unprotected mode. The access code length is set to 0, and the memory pointer is at address 00 hex. While in this mode, any portion of the E^2PROM array can be read or written to without an access code. A portion of the memory may be protected from any write or clear operation by setting the memory pointer to the appropriate address via the WMPR (Write Memory Pointer Register) instruction:

WMPR [address]

Figure 9. EWEN/EWDS Timing

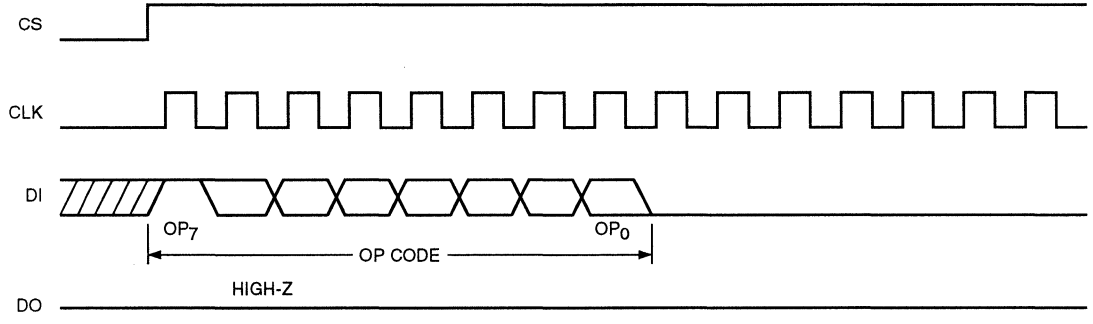
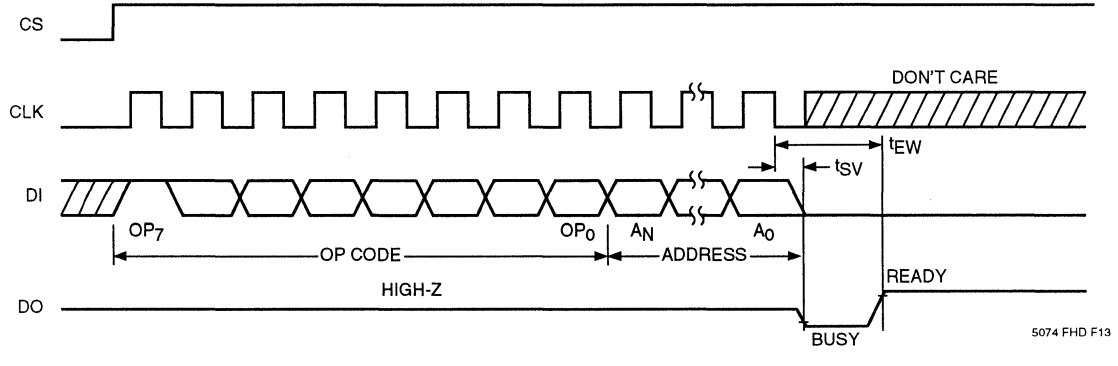


Figure 10. Erase Timing



As shown previously in Figure 3, memory locations below the address set in the memory pointer will be program/erase protected. Thus, unintentional clearing or writing of data in this area will be prevented, while memory locations at or above the protected area still allow full access. This protection does not apply to the ERAL and WRAL commands which are not blocked by the memory pointer.

SECURE MODE

As shown previously in Figure 2, in the secure mode, memory locations at or above the address set in the memory pointer allow READ-only access. Memory locations below that address will require an access code before they can be accessed. The secure mode is activated with an MACC (Modify Access Code) instruction followed by a user access code which can be one to eight bytes in length.

EWEN
MACC [old code][new code][new code]

The EWEN instruction enables the device to perform program/erase operations. The new access code must be entered twice for verification. If the device already has an access code, the old access code must be entered before the new access code can be accepted. The length of the password is incorporated into the MACC portion of the instruction.

Once the secure mode is activated, access to memory locations is under software control. Access (read, write, and clear instructions) to the memory locations below the address in the memory pointer is allowed only if the ENAC (Enable Access) instruction followed by the correct access code has been previously executed.

ENAC [access code]
EWEN
WRITE [address][data]

The ENAC instruction, along with the access code, enables access to the protected area of the device. The EWEN instruction enables execution of the program/erase operations. This portion of the memory is otherwise inaccessible for any operation. Read-only access is allowed without the access code for memory locations at or above the address in the memory pointer.

The access code can be changed by the following instruction:

ENAC [old access code]
EWEN
MACC [old code][new code][new code]

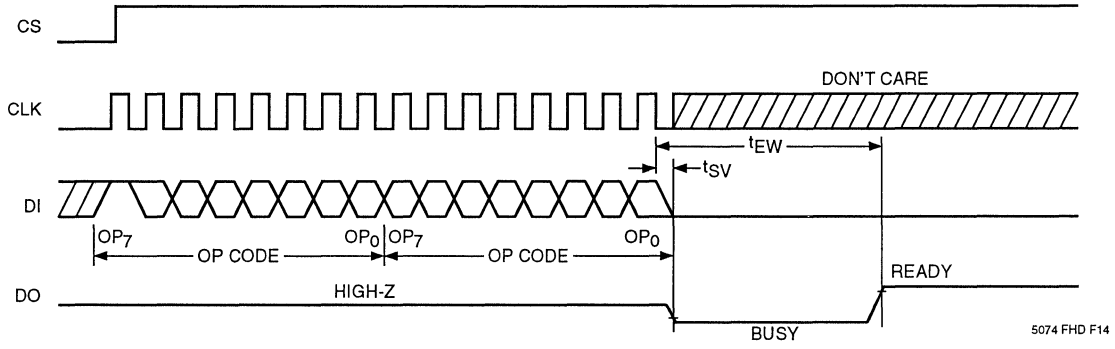
A two-tier protection scheme is implemented to protect data against inadvertent clearing or writing. To write to the memory, an EWEN (Program/Erase Enable) must first be issued. The CAT35C704/CAT35C704I will now allow program/erase operations to be performed only on memory locations at or above the address set in the memory pointer. The remaining portion of the memory is still protected. To override this protection, an OVMPR (Override Memory Pointer Register—see Memory Pointer Register) must be issued for every program/erase instruction which accesses the protected area:

ENAC [access code]
EWEN
OVMPR
WRITE [address][data]

As an alternative to the OVMPR instruction, the WMPR (Write Memory Pointer Register) instruction may be used to move the memory pointer address to uncover the area where writing is to be performed:

ENAC [access code]
EWEN
WMPR [address]
WRITE [address][data]

Figure 11. ERAL Timing



As shipped from the factory, the device is in the unprotected mode. The length of the access code is user selectable from a minimum of one byte to a maximum of eight bytes (> $1.84x10^{19}$ combinations). Loading a zero-length access code will disable protection.

MEMORY POINTER REGISTER

The memory pointer enables the user to segment the E^2PROM array into two sections. In the unprotected mode, the array can be segmented between read-only and full access, while in the secure mode, the memory may be segmented between read-only access and password-only access. Three instructions are dedicated to the memory pointer operations. The first one is WMPR (Write Memory Pointer Register). This instruction, followed by an address, will load the memory pointer register with a new address. This address will be stored in the E^2PROM and can be modified only by another WMPR instruction. The second instruction is OVMPR (Override Memory Pointer Register) which allows a single program/erase to be performed to memory locations below the address set in the memory pointer. This instruction allows the user to modify data in a segmented array without having to move the memory pointer. Once the operation is complete, the device returns to the protected mode. If the device is in the secure mode both of these instructions require the ENAC instruction and a valid access code prior to their execution. The third instruction is the RMPR (Read Memory Pointer Register) which will place the current contents of the register in the serial output buffer.

SECS PROTOCOL

The CAT35C704/CAT35C704I implements the SECS communication protocol which uses an 8 bit transmission format. As shown in Figures 7–13, all instructions are 8 bits long with the first bit being the start bit and the following 7 bits being the op-code. Data can be one or two bytes long depending on the instruction and the memory array organization. Each address is one or two bytes long depending on the organization of the memory array. In this protocol, the transmission of the MSB is always first and the LSB last. The CS (Chip Select) pin of the CAT35C704/CAT35C704I may be used to frame the data transmission packet or it may be set HIGH for the entire duration of operation. If an error in op-code or parity (if enabled) has been detected, the $\overline{ERR}$ output will be set LOW and the CAT35C704/CAT35C704I will stop receiving and sending data until CS is toggled from HIGH to LOW to HIGH again. Alternatively, an error condition may be detected by interrogating the device for a status word. If an error condition has been detected, the DO (Data Output) pin will not respond. DO may be programmed to become tri-stated or to output a RDY/$\overline{BUSY}$ status flag during program/erase cycles (see ENBSY instruction).

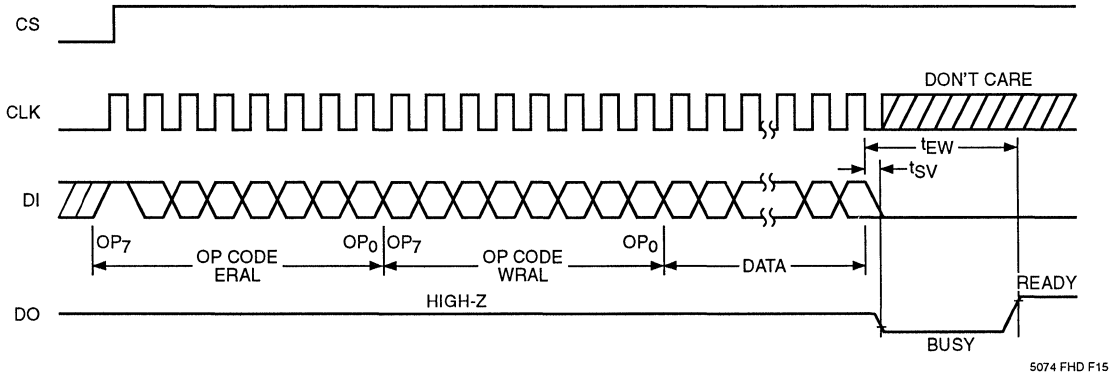
STATUS REGISTER

An eight bit status register is provided to allow the user to determine the status of the CAT35C704/CAT35C704I. The contents of the first three bits of the register are 101 which allows the user to quickly determine the condition of the device. The next three bits indicate the status of the device; they are parity error, instruction error and RDY/$\overline{BUSY}$ status. The last two bits are reserved for future use.

CLEAR ALL AND WRITE ALL

As a precaution, the ERAL instruction has to be entered twice before it is executed. This measure is required as a redundancy check on the incoming instruction for possible transmission errors. The WRAL instruction

Figure 12. WRAL Timing



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requires sending an ERAL first (this sets a flag only) and then the WRAL instruction. The CAT35C704/CAT35C704I will accept the following commands:

ERAL	**ERAL**	An ERAL will be executed
ERAL	**WRAL**	A WRAL will be executed

Both the ERAL and WRAL commands will program/erase the entire array and will not be blocked by the memory pointer.

THE PARITY BIT

The SECS protocol supports an even parity bit if the PE pin of the device is set HIGH, otherwise, there is no parity. If PE is set LOW and the incoming instruction contains a parity bit, it may be interpreted as the start bit of the next instruction. When PE is HIGH, the CAT35C704/CAT35C704I expects a parity bit at the end of every incoming instruction packet. For example, the RSEQ instruction will look like this:

1100 1011
A15...A8
A7...A0 P

The device then outputs data continuously until it reaches the end of the memory. The last byte of data contains 9 bits. The ninth bit is the parity bit calculated over the entire transmitted data packet. The RSEQ instruction may be terminated at any time by bringing CS low; the output will then go to high impedance.

SYSTEM ERRORS

Whenever an error occurs, be it an instruction error (unknown instruction), or parity error (perhaps caused by transmission error), the device will stop its operation. To return to normal operation, the device must be reset by pulsing CS LOW and then set back to HIGH. Resetting the device will not affect the ENAC, EWEN and ENBSY status. The error may be determined by entering the READ STATUS REGISTER (RSR) instruction immediatly following the reset. The status output is an 8 bit word with the first three bits being 101. This three bit pattern indicates that the device is functioning normally. The fourth bit is "1" if a parity error occurred. The fifth bit is a "1" if an instruction error occurred. The sixth bit is a "1" if the device is in a program/erase cycle. The last two bits are reserved for future use.

The reason for the "101" pattern is to distinguish between an error conditon (DO tri-stated) and a device busy status. If an error condition exists, it will not respond to any input instruction from DI. However, if the device is in a program/erase cycle, it responds to the RSR instruction by outputting "101 00100". If RSR is executed at the end of a program/erase cycle, the output will be "101000 00".

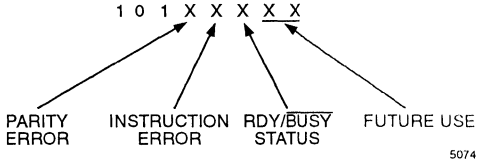
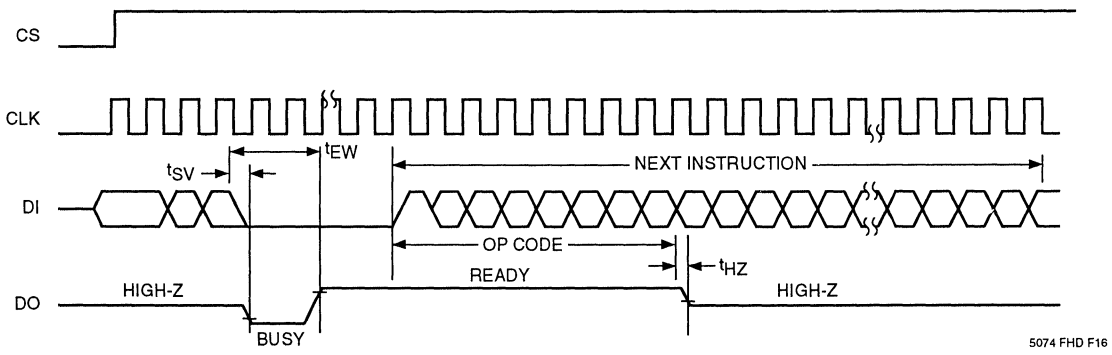


Figure 13. Next Instruction Timing(9)



Note:
(9) DO will be high impedance after the last instruction bit has been clocked in, unless the instruction is RSR or RMPR, in which case, DO will become active.

INSTRUCTION SET

DISAC Disable Access

1000	1000

This instruction will lock the memory from all program/erase operations regardless of the contents of the memory pointer. A write can be accomplished only by first entering the ENAC instruction followed by a valid access code.

ENAC Enable Access

1100	0101	[Access Code]

In the protected mode, this instruction, followed by a valid access code, unlocks the device for read/write/clear access.

WMPR Write Memory Pointer Register

1100	0100	[A15–A8] [A7–A0] *(x8 organization)*
1100	0100	[A7–A0] *(x16 organization)*

The WMPR instruction followed by 8 or 16 bits of address (depending on the organization) will move the pointer to the newly specified address.

MACC Modify Access Code

1101	[Length] [Old code] [New code] [New code]

This instruction requires the user to enter the old access code, if one was set previously, followed by the new access code and a re-entry of the new access code for verification. Within the instruction format, the variable [Length] designates the length of the access code as the following:

[Length] = [0] No access code. Set device to unprotected mode.

[Length] = [1–8] Length of access code is 1 to 8 bytes.

[Length] = [>8] Illegal number of bytes. The CAT35C704/CAT35C704I will ignore the rest of the transmission.

RMPR Read Memory Pointer Register

1100	1010

Output the content of the memory pointer register to the serial output port.

OVMPR Override Memory Pointer Register

1000	0011

Override the memory protection for the next instruction.

READ Read Memory

1100	1001	[A15–A8] [A7–A0] *(x8 organization)*
1100	1001	[A7–A0] *(x16 organization)*

Output the contents of the addressed memory location to the serial port.

WRITE Write Memory

1100	0001	[A15–A8] [A7–A0] [D7–D0] *(x8 organization)*
1100	0001	[A7–A0] [D15–D8] [D7–D0] *(x16 organization)*

Write the 8 bit or 16 bit data to the addressed memory location. After the instruction, address, and data have been entered, the self-timed program/erase cycle will start. The addressed memory location will be erased before data is written. The DO pin may be used to output the RDY/$\overline{\text{BUSY}}$ status by having previously entered the ENBSY instruction. During the program/erase cycle, DO will output a LOW for BUSY during this cycle and a HIGH for READY after the cycle has been completed.

ERASE Clear Memory

1100	0000	[A15–A8] [A7–A0] *(x8 organization)*
1100	0000	[A7–A0] *(x16 organization)*

Erase data in the specified memory location (set memory to "1"). After the instruction and the address have been entered, the self-timed clear cycle will start. The DO pin may be used to output the RDY/$\overline{\text{BUSY}}$ status by having previously entered the ENSBY instruction. During the clear cycle, DO will output a LOW for BUSY during this cycle and a HIGH for ready after the cycle has been completed.

ERAL Clear All

1000	1001
1000	1001

Erase the data of all memory locations (all cells set to "1"). For protection against inadvertent chip clear, the ERAL instruction is required to be entered twice.

WRAL Write All

1000	1001	
1100	0011	[D15–D8] [D7–D0] *(x16 organization)*
1000	1001	
1100	0011	[D7–D0] *(x8 organization)*

Write one or two bytes of data to all memory locations. An ERAL will be automatically performed before the

WRAL is executed. For protection against inadvertent clearing or writing of data, the ERAL instruction is required to be entered preceding the WRAL instruction.

RSEQ Read Sequentially

1100	1011	[A15–A8] [A7–A0] *(x8 organization)*

1100	1011	[A7–A0] *(x16 organization)*

Read memory starting from specified address, sequentially to the highest address or until CS goes LOW. The instruction is terminated when CS goes LOW.

ENBSY Enable Busy

1000	0100

Enable the status indicator on DO during program/erase cycle. DO goes LOW then HIGH once the write cycle is complete. DO will go to HIGH-Z at the end of the next op code transmission.

DISBSY Disable Busy

1000	0101

Disable the status indicator on DO during program/erase cycle.

EWEN Program/Erase Enable

1000	0001

Enable program/erase to be performed on non-protected portion of memory. This instruction must be entered before any program/erase instruction will be carried out. Once entered, it will remain valid until power-down or an EWDS (Program/Erase Disable) is executed.

EWDS Program/Erase Disable

1000	0010

Disable all write and clear functions.

ORG Select Memory Organization

1000	011R	*(where R = 0 or 1)*

Set memory organization to 512 x 8 if R = 0.

Set memory organization to 256 x 16 if R = 1.

RSR Read Status Register

1100	1000

Output the contents of the 8 bit status register. The contents of the first three bits of the register are 101, which allows the user to quickly determine whether the device is listening or is in an error condition. The next three bits indicate parity error, instruction error and RDY/$\overline{\text{BUSY}}$ status. The last two bits are reserved for future use.

NOP No Operation

1000	0000

No Operation.

CATALYST SEMICONDUCTOR

CAT33C804A-B/CAT33C804A-BI

4K-Bit SECURE ACCESS SERIAL E²PROM

FEATURES

- Low Power CMOS Technology
- 3V Operation
- Password READ/WRITE Protection: 1 to 8 Bytes
- Memory Pointer WRITE Protection
- Sequential READ Operation
- 256 x 16 or 512 x 8 Selectable Serial Memory
- UART Compatible Asynchronous Protocol
- 100,000 Program/Erase Cycles
- I/O Speed: 9600 Baud
  –CAT33C804A: 4.9152 MHz Xtal
  –CAT33C804B: 3.579545 MHz Xtal
- Low Power Consumption:
  –Active: 3mA
  –Standby: 250µA
- 100 Year Data Retention
- Optional High Endurance Device Available

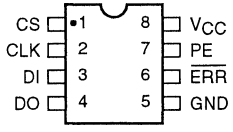
DESCRIPTION

The CAT33C804A-B/CAT33C804A-BI is a 4K bit Serial E²PROM that safeguards stored data from unauthorized access by use of a user selectable (1 to 8 byte) access code and a movable memory pointer. Two operating modes provide unprotected and password-protected operation allowing the user to configure the device as anything from a ROM to a fully protected no-access memory. The CAT33C804A-B/CAT33C804A-BI uses a UART compatible asynchronous protocol and has a Sequential Read feature where data can be sequentially clocked out of the memory array. The device is available in 8 pin DIP or 16 pin SO packages.

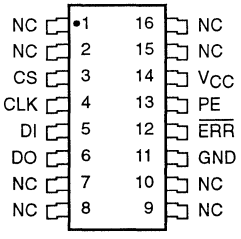
6

PIN CONFIGURATION

DIP Package



SO Package



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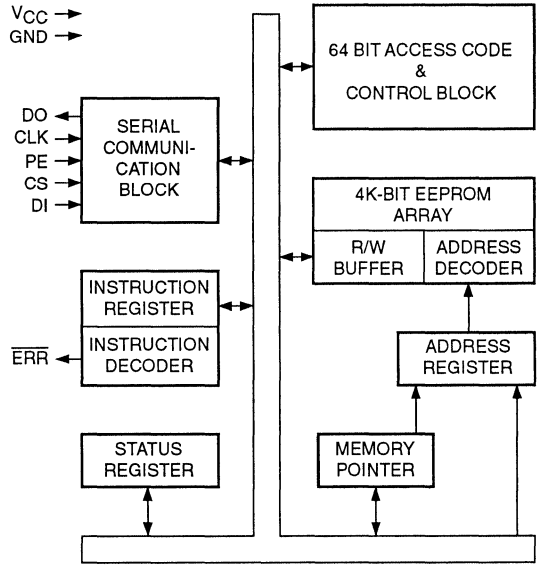
PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
DO(1)	Serial Data Output
CLK	Clock Input
DI(1)	Serial Data Input
PE	Parity Enable
$\overline{ERR}$	Error Indication Pin
VCC	+3V Power Supply
GND	Ground

Note:
(1) DI, DO may be tied together to form a common I/O.

BLOCK DIAGRAM



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TD 5078

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with Respect to Ground(2) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (T_a = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(3) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(4)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(4)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(4)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(4)(5)	Latch-up	100		mA	JEDEC Standard 17

D.C. CHARACTERISTICS

CAT33C804A-B T_A = 0°C to +70°C, V_{CC} = +3V ±10%,unless otherwise specified.
CAT33C804A-BI T_A = –40°C to +85°C, V_{CC} = +3V ±10%,unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current (Operating)			3	mA	V_{CC} = 3.3V, CS = V_{CC} DO is Unloaded.
I_{SB}	Power Supply Current (Standby)			250	µA	V_{CC} = 3.3V, CS = 0V DI = 0V, CLK = 0V
V_{IL}	Input Low Voltage	–0.1		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –400µA
I_{LI}(6)	Input Leakage Current			2	µA	V_{IN} = 3.3V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 3.3V, CS = 0V

Note:
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) This parameter is tested initially and after a design or process change that affects the parameter.
(5) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(6) PE pin test conditions: $V_{IH} < V_{IN} < V_{IL}$

A.C. CHARACTERISTICS

CAT33C804A-B T_A = 0°C to +70°C, V_{CC} = +3V ±10%,unless otherwise specified.
CAT33C804A-BI T_A = –40°C to +85°C, V_{CC} = +3V ±10%,unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSH}	CS Hold Time	0			ns	C_L = 100pF
t_D	CLK to DO Delay		104		µs	$V_{IN} = V_{IH}$ or V_{IL}
t_{PD}	CLK to DO Delay			150	ns	$V_{OUT} = V_{OH}$ or V_{OL}
t_{HZ}(4) (7)	CLK to DO High-Z Delay			50	ns	
t_{EW}	Program/Erase Pulse Width			12	ms	
t_{CSL}	CS Low Pulse Width	100			ns	
t_{SV}	$\overline{ERR}$ Output Delay			150	ns	C_L = 100pF
t_{VCCS}(4)	V_{CC} to CS Setup Time	5			µs	C_L = 100pF
f_{CLK}	Maximum Clock Frequency	DC		A: 4.9152 B: 3.579545	MHz	

Note:
(4) This parameter is tested initially and after a design or process change that affects the parameter.
(7) t_{HZ} is measured from the falling edge of the clock to the time when the output is no longer driven.

6

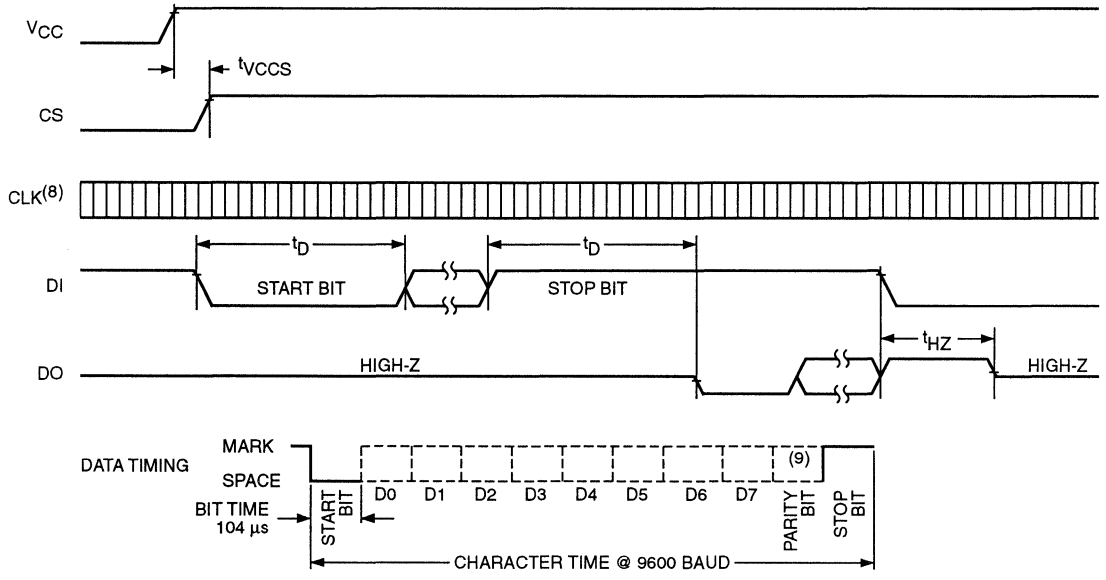
PASSWORD PROTECTION

The CAT33C804A-B/CAT33C804A-BI is a 4K bit E^2PROM that features a password protection scheme to prevent unauthorized access to the information stored in the device. It contains an access code register which stores one to eight bytes of access code along with the length of that access code. Additionally, a memory pointer register stores the address that partitions the memory into protected and unprotected areas. As shipped from the factory, the device is unprogrammed and unprotected. The length of the access code is equal to zero and the memory pointer register points to location zero. Every byte of the device is fully accessible without an access code. Setting a password and moving the memory pointer register to cover all or part of the memory secures the device. Once secured, the memory is divided into a read/write area and a read-only area with the entry of a valid access code. If no access code is entered, the memory is divided into a read-only area and a non-access area. Figure 2 illlustrates this partitioning of the memory array.

WRITE PROTECTION

Another feature of the CAT33C804A-B/CAT33C804A-BI is WRITE-protection without the use of an access code. If the memory pointer register is set to cover all or part of the memory, without setting the access code register, the device may be divided into an area which allows full access, and an area which allows READ-only access. To write into the READ-only area, the user can override the memory pointer register for every WRITE instruction or he can simply move the address in the memory pointer register to uncover this area, and then write into the memory. This mechanism prevents inadvertent overwriting of important data in the memory

Figure 1. A.C. Timing



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Note:
(8) Clock = 4.9152 MHz for the CAT33C804A or 3.579545 MHz for the CAT33C804B.
(9) If PE pin = 1.

without the use of an access code. Figure 3 illustrates this partitioning of the memory array.

READ SEQUENTIAL

To allow for convenient reading of blocks of contiguous data, the device has a READ SEQUENTIAL instruction which accepts a starting address of the block and continuously outputs data of subsequent addresses until the end of memory, or until Chip Select goes LOW.

The CAT33C804A-B/CAT33C804A-BI communicates with external devices via an asynchronous serial communication protocol. The data transmission may be a continuous stream of data or it can be packed by pulsing Chip Select LOW in between each packet of information. (Except for the SEQUENTIAL READ instruction where Chip Select must be held high).

PIN DESCRIPTIONS

CS

Chip Select is a TTL compatible input which, when set HIGH, allows normal operation of the device. Any time Chip Select is set LOW, it resets the device, terminating all I/O communication, and puts the output in a high impedance state. CS is used to reset the device if an error condition exists or to put the device in a power-down mode to minimize power consumption. It may also be used to frame data transmission in applications where the clock and data input have to be ignored from time to time. Although CS resets the device, it does not change the program/erase or the access-enable status, nor does it terminate a programming cycle once it has started. The program/erase and access-enable operations, once enabled, will remain enabled until specific disabling instructions are sent or until power is removed.

Figure 2. Secure Mode

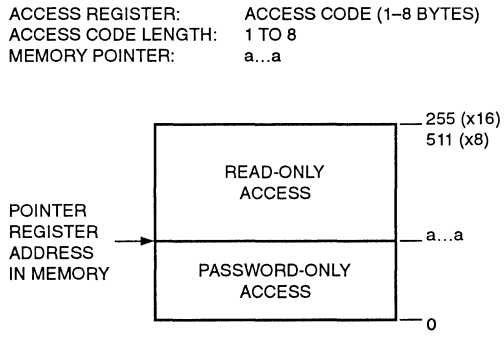

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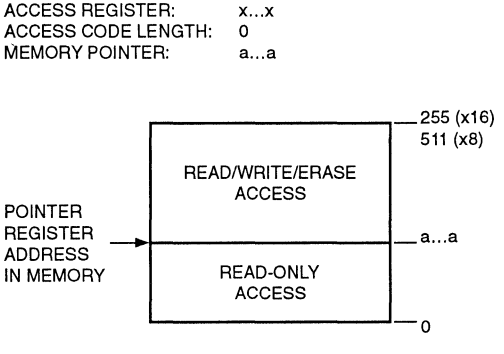
Figure 3. Unprotected Mode(10)



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Note:
(10)x = DON'T CARE; a = ADDRESS BIT.

CLK

The System Clock is a TTL compatible input pin that allows operation of the device at a specified frequency. The CAT33C804A-B/CAT33C804A-BI is designed with an internal divider to produce a 9600 baud output for an input clock frequency of 4.9152 MHz and 3.579545 MHz respectively.

DI

The Data Input pin is TTL compatible and accepts data and instructions in a serial format. Each byte must begin with "0" as a start bit. The device will accept as many bytes as an instruction requires, including both data and address bytes. Extra bits will be disregarded if they are "1"s and extra "0"s will be misinterpreted as the start bit of the next instruction. An instruction error will cause the device to abort operation and all I/O communication will be terminated until a reset is received.

DO

The Data Output pin is a tri-state TTL compatible output. It is normally in a high impedance state unless a READ or an ENABLE BUSY instruction is executed. Following the completion of a 16 bit or 8 bit data stream, the output will return to the high impedance state. During a program/erase cycle, if the ENABLE BUSY instruction has been previously executed, the output will stay LOW while the device is BUSY, and it will be set HIGH when the program/erase cycle is completed. DO will stay HIGH until the completion of the next instruction's opcode and, if the next instruction is a READ, DO will output the appropriate data at the end of the instruction. If the

Figure 4. Program/Erase Timing (x8 Format)

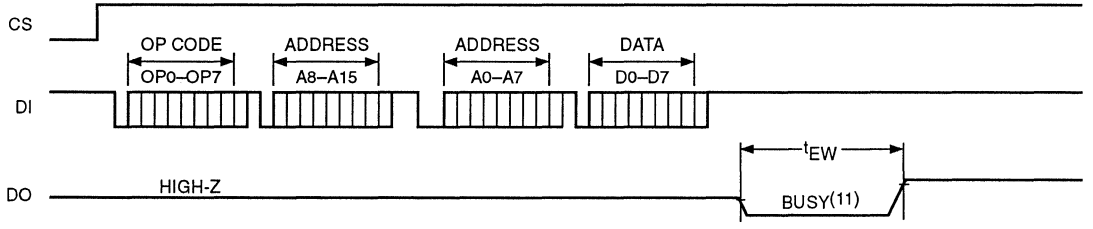

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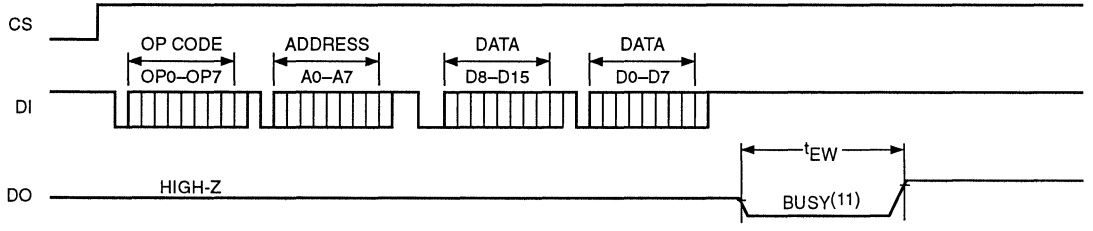
Figure 5. Program/Erase Timing (x16 Format)



5076 FHD F08

Note:
(11) DO becomes low to indicate busy status if ENBSY was previously executed. If ENBSY was not previously executed, DO will be in the High-Z condition.

ENABLE BUSY instruction has not been previously executed, DO will stay in a high impedance state. DO will also go to the high impedance state if an error condition is detected. In the event an ENABLE BUSY instruction has not been sent, a READ STATUS register instruction can be executed. This also tells the user whether the part is in a program/erase cycle or an error condtion. When the device is in a program/erase cycle it will output an 8 bit status word. If it does not, it is in an error condition.

PE

The Parity Enable pin is a TTL compatible input. If the PE pin is set HIGH, the device will be configured to communicate using even parity, and if the pin is set LOW, it will use no parity. In this case, instructions or data that include parity bits will not be interpreted correctly. Note: The PE input is internally pulled down to GND (i.e. default = no parity). As with all CMOS devices, CS, CLK and DI inputs must be connected to either HIGH or LOW, and not left floating.

$\overline{ERR}$

The Error indication pin is an open drain output. If either an instruction or parity error exists, the $\overline{ERR}$ pin will output a "0" until the device is reset. This can be done by pulsing CS LOW.

Figure 6. Read Timing (x8 Format)

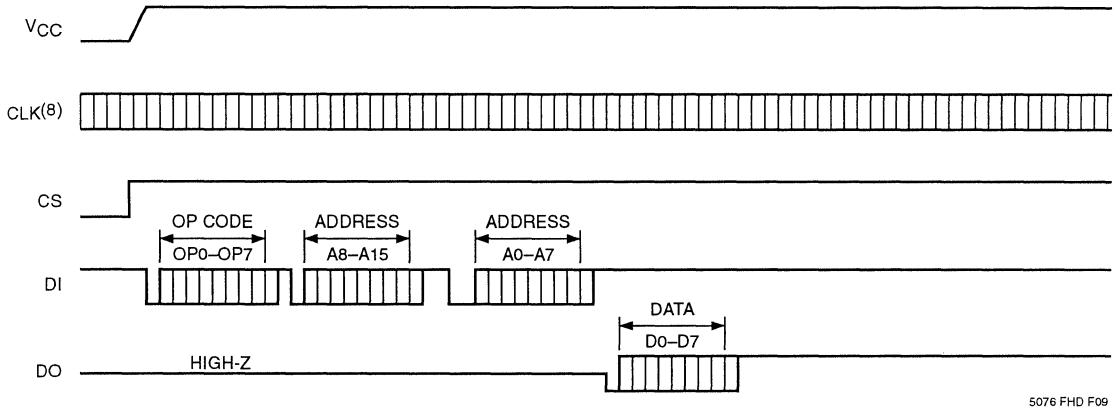
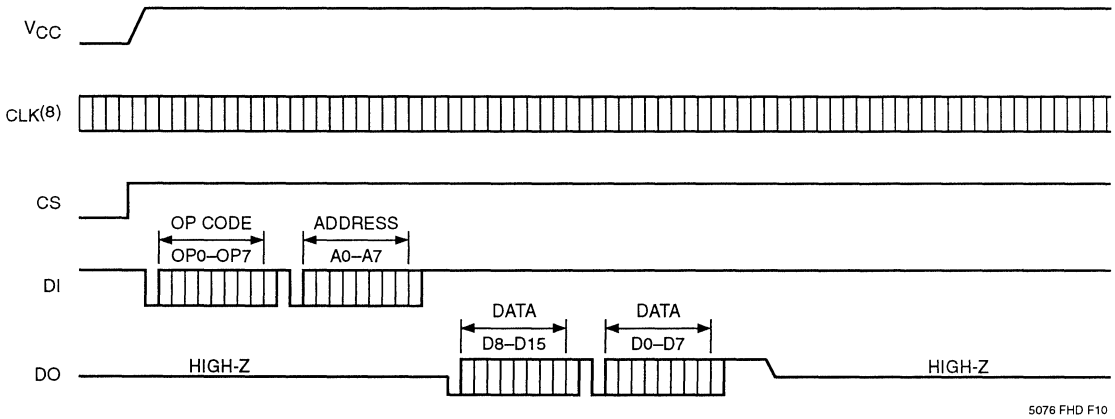


Figure 7. Read Timing (x16 Format)



Note:
(8) Clock = 4.9152 MHz for the CAT33C804A or 3.579545 MHz for the CAT33C804B.

DEVICE OPERATION

INSTRUCTIONS

The CAT33C804A-B/CAT33C804A-BI instruction set includes 19 instructions.

Six instructions are related to security or write protection:

DISAC	Disable Access
ENAC	Enable Access
MACC	Modify Access Code
OVMPR	Override Memory Pointer Register
RMPR	Read Memory Pointer Register
WMPR	Write Memory Pointer Register

Six instructions are READ/WRITE/ERASE instructions:

ERAL	Clear All Locations
ERASE	Clear Memory Locations
READ	Read Memory
RSEQ	Read Sequentially
WRAL	Write All
WRITE	Write memory

Note: All write instructions will automatically perform a clear before writing data.

Seven instructions are used as control and status functions:

DISBSY	Disable Busy
ENBSY	Enable Busy
EWEN	Program/Erase Enable
EWDS	Program/Erase Disable
NOP	No Operation
ORG	Select Memory Organization
RSR	Read Status Register

UNPROTECTED MODE

As shipped from the factory, the CAT33C804A-B/CAT33C804A-BI is in the unprotected mode. The access code length is set to 0, and the memory pointer is at address 00 hex. While in this mode, any portion of the E^2PROM array can be read or written to without an access code. A portion of the memory may be protected from any write or clear operation by setting the memory pointer to the appropriate address via the WMPR (Write Memory Pointer Register) instruction:

WMPR [address]

Figure 8. EWEN/EWDS Timing (x8 Format)

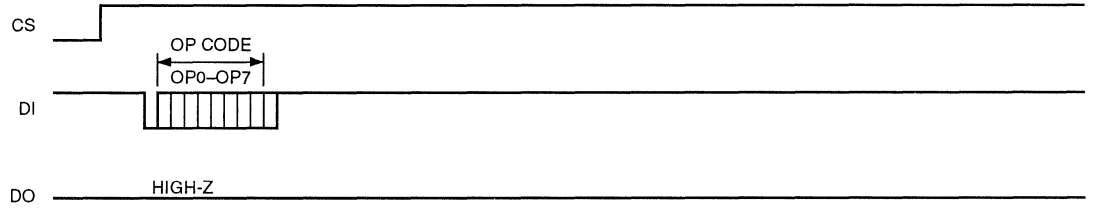


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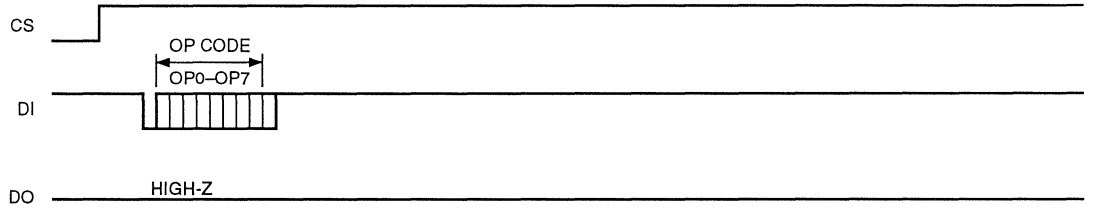
Figure 9. EWEN/EWDS Timing (x16 Format)



5076 FHD F11

As shown previously in Figure 3, memory locations below the address set in the memory pointer will be program/erase protected. Thus, unintentional clearing or writing of data in this area will be prevented, while memory locations at or above the protected area still allow full access. This protection does not apply to the ERAL and WRAL commands which are not blocked by the memory pointer.

SECURE MODE

As shown previously in Figure 2, in the secure mode, memory locations at or above the address set in the memory pointer allow READ-only access. Memory locations below that address will require an access code before they can be accessed. The secure mode is activated with an MACC (Modify Access Code) instruction followed by a user access code which can be one to eight bytes in length.

EWEN
MACC [old code][new code][new code]

The EWEN instruction enables the device to perform program/erase operations. The new access code must be entered twice for verification. If the device already has an access code, the old access code must be entered before the new access code can be accepted. The length of the password is incorporated into the MACC portion of the instruction.

Once the secure mode is activated, access to memory locations is under software control. Access (read, write, and clear instructions) to the memory locations below the address in the memory pointer is allowed only if the ENAC (Enable Access) instruction followed by the correct access code has been previously executed.

ENAC [access code]
EWEN
WRITE [address][data]

The ENAC instruction, along with the access code, enables access to the protected area of the device. The EWEN instruction enables execution of the program/erase operations. This portion of the memory is otherwise inaccessible for any operation. Read-only access is allowed without the access code for memory locations at or above the address in the memory pointer.

The access code can be changed by the following instruction:

ENAC [old access code]
EWEN
MACC [old code][new code][new code]

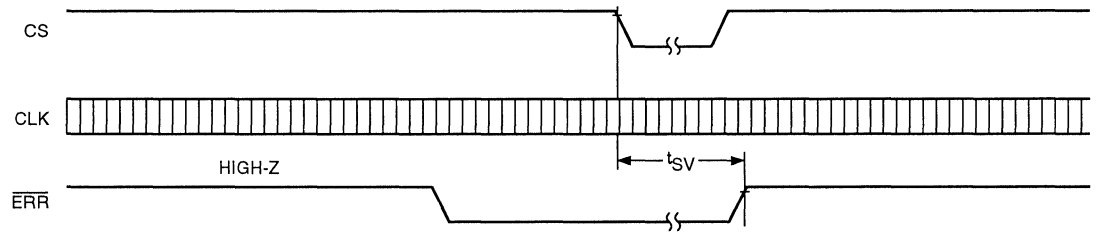
A two-tier protection scheme is implemented to protect data against inadvertent clearing or writing. To write to the memory, an EWEN (Program/Erase Enable) must first be issued. The CAT33C804A-B/CAT33C804A-BI will now allow program/erase operations to be performed only on memory locations at or above the address set in the memory pointer. The remaining portion of the memory is still protected. To override this protection, an OVMPR (Override Memory Pointer Register—see Memory Pointer Register) must be issued for every program/erase instruction which accesses the protected area:

ENAC [access code]
EWEN
OVMPR
WRITE [address][data]

As an alternative to the OVMPR instruction, the WMPR (Write Memory Pointer Register) instruction may be used to move the memory pointer address to uncover the area where writing is to be performed:

ENAC [access code]
EWEN
WMPR [address]
WRITE [address][data]

Figure 10. $\overline{ERR}$ Pin Timing



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As shipped from the factory, the device is in the unprotected mode. The length of the access code is user selectable from a minimum of one byte to a maximum of eight bytes (> $1.84x10^{19}$ combinations). Loading a zero-length access code will disable protection.

MEMORY POINTER REGISTER

The memory pointer enables the user to segment the E^2PROM array into two sections. In the unprotected mode, the array can be segmented between read-only and full access, while in the secure mode, the memory may be segmented between read-only access and password-only access. Three instructions are dedicated to the memory pointer operations. The first one is WMPR (Write Memory Pointer Register). This instruction, followed by an address, will load the memory pointer register with a new address. This address will be stored in the E^2PROM and can be modified only by another WMPR instruction. The second instruction is OVMPR (Override Memory Pointer Register) which allows a single program/erase to be performed to memory locations below the address set in the memory pointer. This instruction allows the user to modify data in a segmented array without having to move the memory pointer. Once the operation is complete, the device returns to the protected mode. If the device is in the secure mode both of these instructions require the ENAC instruction and a valid access code prior to their execution. The third instruction is the RMPR (Read Memory Pointer Register) which will place the current contents of the register in the serial output buffer.

STATUS REGISTER

An eight bit status register is provided to allow the user to determine the status of the CAT33C804A-B/CAT33C804A-BI. The contents of the first three bits of the register are 101 which allows the user to quickly determine the condition of the device. The next three bits indicate the status of the device; they are parity error, instruction error and RDY/$\overline{BUSY}$ status. The last two bits are reserved for future use.

CLEAR ALL AND WRITE ALL

As a precaution, the ERAL instruction has to be entered twice before it is executed. This measure is required as a redundancy check on the incoming instruction for possible transmission errors. The WRAL instruction requires sending an ERAL first (this sets a flag only) and

Figure 11. Erase Timing (x8 Format)

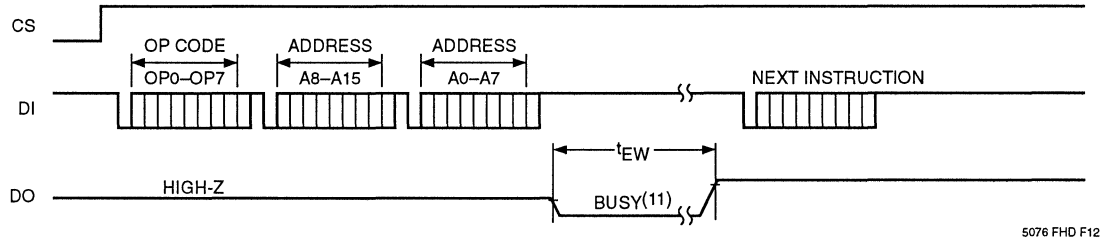
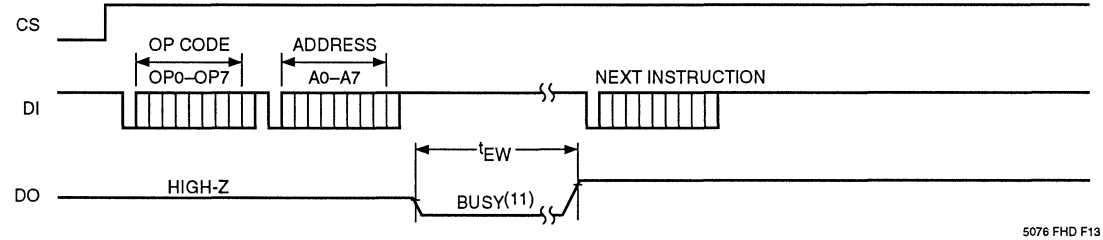


Figure 12. Erase Timing (x16 Format)



Note:
(11) DO becomes low to indicate busy status if ENBSY was previously executed. If ENBSY was not previously executed, DO will be in High-Z condition.

then the WRAL instruction. The CAT33C804A-B/CAT33C804A-BI will accept the following commands:

ERAL	**ERAL**	An ERAL will be executed
ERAL	**WRAL**	A WRAL will be executed

Both the ERAL and WRAL commands will program/erase the entire array and will not be blocked by the memory pointer.

THE PARITY BIT

The UART compatible protocol supports an even parity bit if the PE pin of the device is set HIGH, otherwise, there is no parity. If PE is set LOW and the incoming instruction contains a parity bit, it may be interpreted as the stop bit. When PE is HIGH, the CAT33C804A-B/CAT33C804A-BI expects a parity bit at the end of every byte. For example, the RSEQ instruction will look like this:

0 1100 1011 11
0 A15...A8 P1
0 A7...A0 P1

The device then outputs data continuously until it reaches the end of the memory. Each byte of data contains 9 bits with the ninth bit being the parity bit. The RSEQ instruction may be terminated at any time by bringing CS low; the output will then go to high impedance.

SYSTEM ERRORS

Whenever an error occurs, be it an instruction error (unknown instruction), or parity error (perhaps caused by transmission error), the device will stop its operation. To return to normal operation, the device must be reset by pulsing CS LOW and then set back to HIGH. Resetting the device will not affect the ENAC, EWEN and ENBSY status. The error may be determined by entering the READ STATUS REGISTER (RSR) instruction immediatly following the reset. The status output is an 8 bit word with the first three bits being 101. This three bit pattern indicates that the device is functioning normally. The fourth bit is "1" if a parity error occurred. The fifth bit is a "1" if an instruction error occurred. The sixth bit is a "1" if the device is in a program/erase cycle. The last two bits are reserved for future use.

The reason for the "101" pattern is to distinguish between an error conditon (DO tri-stated) and a device busy status. If an error condition exists, it will not respond to any input instruction from DI. However, if the device is in a program/erase cycle, it responds to the RSR instruction by outputting "101 00100". If RSR is executed at the end of a program/erase cycle, the output will be "101000 00".

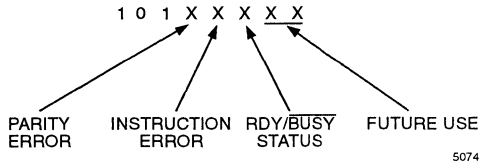


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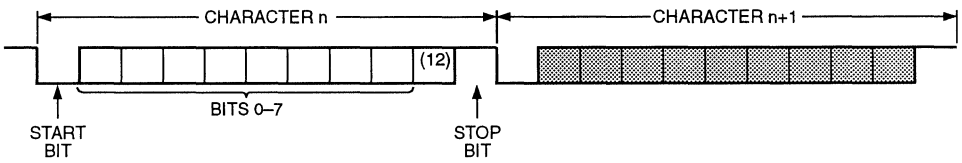
Figure 13. Asynchronous Communication Protocol



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Note:
(12) Parity bit if enabled; skipped if parity disabled.

INSTRUCTION SET

DISAC Disable Access

1000	1000

This instruction will lock the memory from all program/erase operations regardless of the contents of the memory pointer. A write can be accomplished only by first entering the ENAC instruction followed by a valid access code.

ENAC Enable Access

1100	0101	[Access Code]

In the protected mode, this instruction, followed by a valid access code, unlocks the device for read/write/clear access.

WMPR Write Memory Pointer Register

1100	0100	[A15–A8] [A7–A0] *(x8 organization)*
1100	0100	[A7–A0] *(x16 organization)*

The WMPR instruction followed by 8 or 16 bits of address (depending on the organization) will move the pointer to the newly specified address.

MACC Modify Access Code

1101	[Length] [Old code] [New code] [New code] .

This instruction requires the user to enter the old access code, if one was set previously, followed by the new access code and a re-entry of the new access code for verification. Within the instruction format, the variable [Length] designates the length of the access code as the following:

[Length] = [0] No access code. Set device to unprotected mode.

[Length] = [1–8] Length of access code is 1 to 8 bytes.

[Length] = [>8] Illegal number of bytes. The CAT33C804A-B/CAT33C804A-BI will ignore the rest of the transmission.

RMPR Read Memory Pointer Register

1100	1010

Output the content of the memory pointer register to the serial output port.

Figure 14. ERAL Timing (x8 Format)

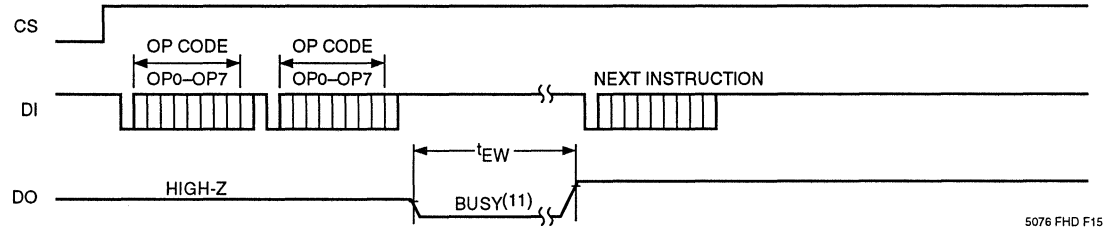
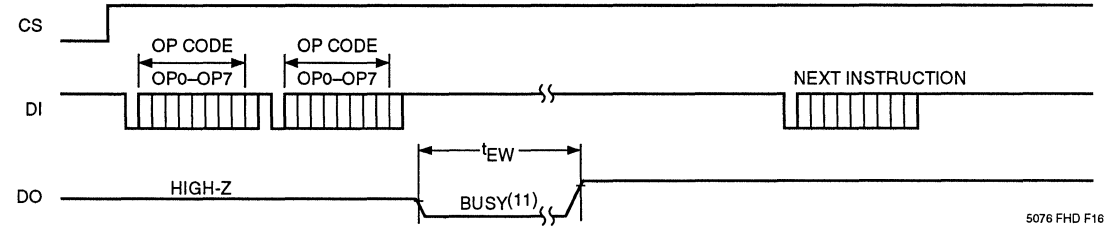


Figure 15. ERAL Timing (x16 Format)



Note:
(11) DO becomes low to indicate busy status if ENBSY was previously executed. If ENBSY was not previously executed, DO will be in the High-Z condition.

OVMPR Override Memory Pointer Register

1000	0011

Override the memory protection for the next instruction.

READ Read Memory

1100	1001	[A15–A8] [A7–A0] *(x8 organization)*
1100	1001	[A7–A0] *(x16 organization)*

Output the contents of the addressed memory location to the serial port.

WRITE Write Memory

1100	0001	[A15–A8] [A7–A0] [D7–D0] *(x8 organization)*
1100	0001	[A7–A0] [D15–D8] [D7–D0] *(x16 organization)*

Write the 8 bit or 16 bit data to the addressed memory location. After the instruction, address, and data have been entered, the self-timed program/erase cycle will start. The addressed memory location will be erased before data is written. The DO pin may be used to output the RDY/$\overline{\text{BUSY}}$ status by having previously entered the ENBSY instruction. During the program/erase cycle, DO will output a LOW for BUSY during this cycle and a HIGH for READY after the cycle has been completed.

ERASE Clear Memory

1100	0000	[A15–A8] [A7–A0] *(x8 organization)*
1100	0000	[A7–A0] *(x16 organization)*

Erase data in the specified memory location (set memory to "1"). After the instruction and the address have been entered, the self-timed clear cycle will start. The DO pin may be used to output the RDY/$\overline{\text{BUSY}}$ status by having previously entered the ENSBY instruction. During the clear cycle, DO will output a LOW for BUSY during this cycle and a HIGH for ready after the cycle has been completed.

ERAL Clear All

1000	1001
1000	1001

Erase the data of all memory locations (all cells set to "1"). For protection against inadvertent chip clear, the ERAL instruction is required to be entered twice.

6

Figure 16. WRAL Timing (x8 Format)

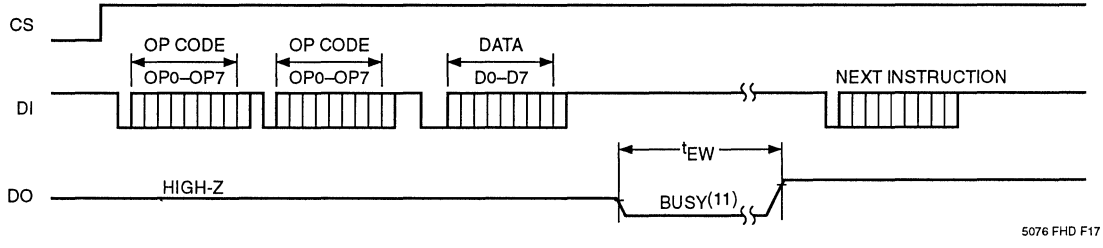
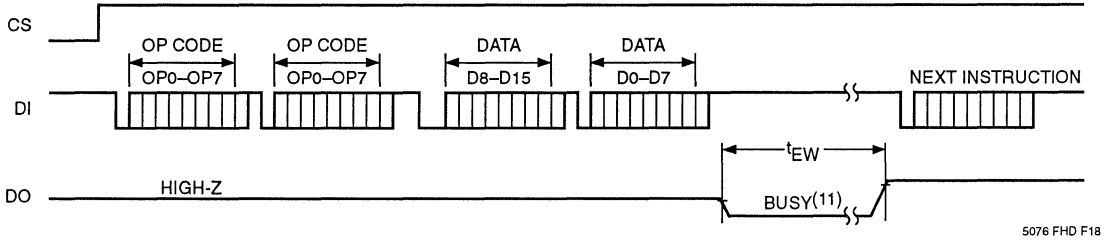


Figure 17. WRAL Timing (x16 Format)



Note:
(11) DO becomes low to indicate busy status if ENBSY was previously executed. If ENBSY was not previously executed, DO will be in the High-Z condition.

WRAL Write All

1000	1001	
1100	0011	[D15–D8] [D7–D0] *(x16 organization)*
1000	1001	
1100	0011	[D7–D0] *(x8 organization)*

Write one or two bytes of data to all memory locations. An ERAL will be automatically performed before the WRAL is executed. For protection against inadvertent clearing or writing of data, the ERAL instruction is required to be entered preceding the WRAL instruction.

RSEQ Read Sequentially

1100	1011	[A15–A8] [A7–A0] *(x8 organization)*
1100	1011	[A7–A0] *(x16 organization)*

Read memory starting from specified address, sequentially to the highest address or until CS goes LOW. The instruction is terminated when CS goes LOW.

ENBSY Enable Busy

1000	0100

Enable the status indicator on DO during program/erase cycle. DO goes LOW then HIGH once the write cycle is complete. DO will go to HIGH-Z at the end of the next op code transmission.

DISBSY Disable Busy

1000	0101

Disable the status indicator on DO during program/erase cycle.

EWEN Program/Erase Enable

1000	0001

Enable program/erase to be performed on non-protected portion of memory. This instruction must be entered before any program/erase instruction will be carried out. Once entered, it will remain valid until power-down or an EWDS (Program/Erase Disable) is executed.

EWDS Program/Erase Disable

1000	0010

Disable all write and clear functions.

ORG Select Memory Organization

1000	011R *(where R = 0 or 1)*

Set memory organization to 512 x 8 if R = 0.

Set memory organization to 256 x 16 if R = 1.

RSR Read Status Register

1100	1000

Output the contents of the 8 bit status register. The contents of the first three bits of the register are 101, which allows the user to quickly determine whether the device is listening or is in an error condition. The next three bits indicate parity error, instruction error and RDY/$\overline{\text{BUSY}}$ status. The last two bits are reserved for future use.

NOP No Operation

1000	0000

No Operation.

CATALYST SEMICONDUCTOR

CAT35C804A-B/CAT35C804A-BI

4K-Bit SECURE ACCESS SERIAL E²PROM

FEATURES

- Low Power CMOS Technology
- Password READ/WRITE Protection: 1 to 8 Bytes
- Memory Pointer WRITE Protection
- Sequential READ Operation
- 256 x16 or 512 x 8 Selectable Serial Memory
- UART Compatible Asynchronous Protocol
- 100,000 Program/Erase Cycles
- I/O Speed: 9600 Baud
  –CAT35C804A: 4.9152 MHz Xtal
  –CAT35C804B: 3.579545 MHz Xtal
- Low Power Consumption:
  –Active: 3mA
  –Standby: 250µA
- 100 Year Data Retention
- Optional High Endurance Device Available

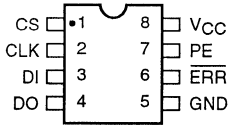
DESCRIPTION

The CAT35C804A-B/CAT35C804A-BI is a 4K bit Serial E²PROM that safeguards stored data from unauthorized access by use of a user selectable (1 to 8 byte) access code and a movable memory pointer. Two operating modes provide unprotected and password-protected operation allowing the user to configure the device as anything from a ROM to a fully protected no-access memory. The CAT35C804A-B/CAT35C804A-BI uses a UART compatible asynchronous protocol and has a Sequential Read feature where data can be sequentially clocked out of the memory array. The device is available in 8 pin DIP or 16 pin SO packages.

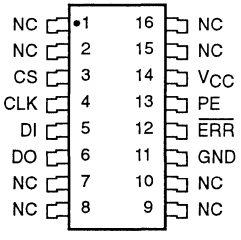
6

PIN CONFIGURATION

DIP Package



SO Package



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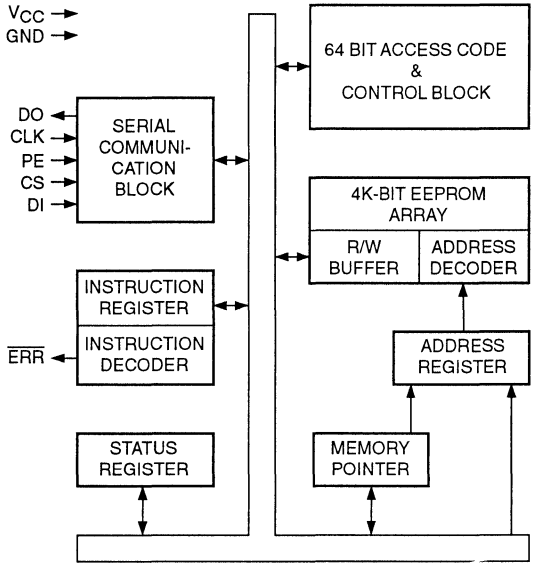
PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
DO(1)	Serial Data Output
CLK	Clock Input
DI(1)	Serial Data Input
PE	Parity Enable
$\overline{ERR}$	Error Indication Pin
VCC	+5V Power Supply
GND	Ground

Note:
(1) DI, DO may be tied together to form a common I/O.

BLOCK DIAGRAM



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TD 5076

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with Respect to Ground(2) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (T_a = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(3) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(4)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(4)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(4)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(4)(5)	Latch-up	100		mA	JEDEC Standard 17

D.C. CHARACTERISTICS

CAT35C804A-B T_A = 0°C to +70°C, V_{CC} = +5V ±10%,unless otherwise specified.
CAT35C804A-BI T_A = –40°C to +85°C, V_{CC} = +5V ±10%,unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current (Operating)			3	mA	V_{CC} = 5.5V, CS = V_{CC} DO is Unloaded.
I_{SB}	Power Supply Current (Standby)			250	µA	V_{CC} = 5.5V, CS = 0V DI = 0V, CLK = 0V
V_{IL}	Input Low Voltage	–0.1		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –400µA
I_{LI}(6)	Input Leakage Current			2	µA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 5.5V, CS = 0V

Note:
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) This parameter is tested initially and after a design or process change that affects the parameter.
(5) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(6) PE pin test conditions: $V_{IH} < V_{IN} < V_{IL}$

A.C. CHARACTERISTICS

CAT35C804A-B T_A = 0°C to +70°C, V_{CC} = +5V ±10%,unless otherwise specified.
CAT35C804A-BI T_A = –40°C to +85°C, V_{CC} = +5V ±10%,unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{CSH}	CS Hold Time	0			ns	C_L = 100pF
t_D	CLK to DO Delay		104		µs	$V_{IN} = V_{IH}$ or V_{IL}
t_{PD}	CLK to DO Delay			150	ns	$V_{OUT} = V_{OH}$ or V_{OL}
t_{HZ}(4) (7)	CLK to DO High-Z Delay			50	ns	
t_{EW}	Program/Erase Pulse Width			12	ms	
t_{CSL}	CS Low Pulse Width	100			ns	
t_{SV}	$\overline{ERR}$ Output Delay			150	ns	C_L = 100pF
t_{VCCS}(4)	V_{CC} to CS Setup Time	5			µs	C_L = 100pF
f_{CLK}	Maximum Clock Frequency	DC		A: 4.9152 B: 3.579545	MHz	

Note:
(4) This parameter is tested initially and after a design or process change that affects the parameter.
(7) t_{HZ} is measured from the falling edge of the clock to the time when the output is no longer driven.

6

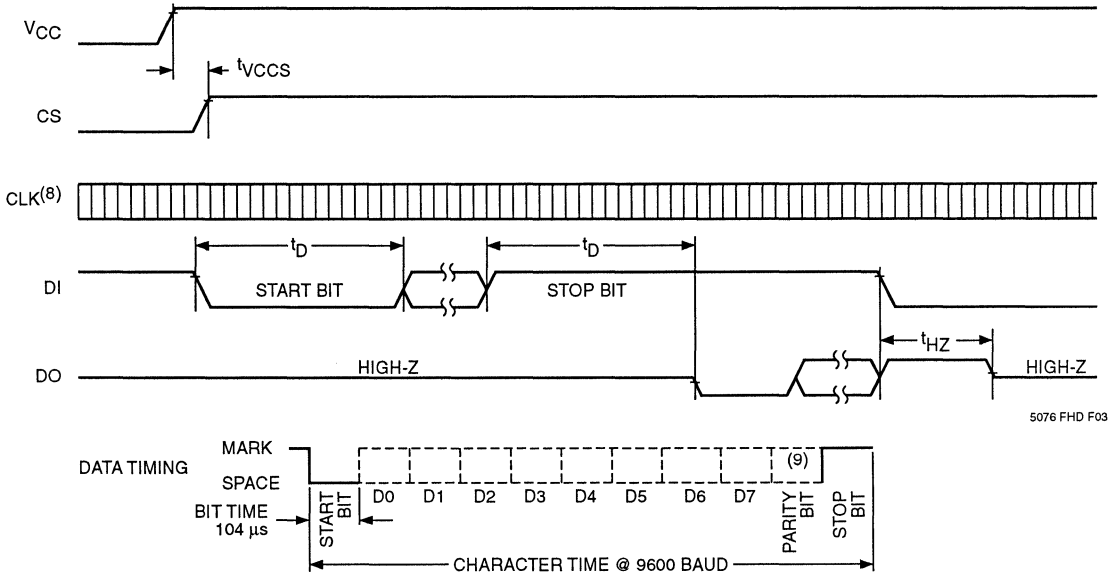
PASSWORD PROTECTION

The CAT35C804A-B/CAT35C804A-BI is a 4K bit E^2PROM that features a password protection scheme to prevent unauthorized access to the information stored in the device. It contains an access code register which stores one to eight bytes of access code along with the length of that access code. Additionally, a memory pointer register stores the address that partitions the memory into protected and unprotected areas. As shipped from the factory, the device is unprogrammed and unprotected. The length of the access code is equal to zero and the memory pointer register points to location zero. Every byte of the device is fully accessible without an access code. Setting a password and moving the memory pointer register to cover all or part of the memory secures the device. Once secured, the memory is divided into a read/write area and a read-only area with the entry of a valid access code. If no access code is entered, the memory is divided into a read-only area and a non-access area. Figure 2 illlustrates this partitioning of the memory array.

WRITE PROTECTION

Another feature of the CAT35C804A-B/CAT35C804A-BI is WRITE-protection without the use of an access code. If the memory pointer register is set to cover all or part of the memory, without setting the access code register, the device may be divided into an area which allows full access, and an area which allows READ-only access. To write into the READ-only area, the user can override the memory pointer register for every WRITE instruction or he can simply move the address in the memory pointer register to uncover this area, and then write into the memory. This mechanism prevents inadvertent overwriting of important data in the memory

Figure 1. A.C. Timing



Note:
(8) Clock = 4.9152 MHz for the CAT35C804A or 3.579545 MHz for the CAT35C804B.
(9) If PE pin = 1.

without the use of an access code. Figure 3 illustrates this partitioning of the memory array.

READ SEQUENTIAL

To allow for convenient reading of blocks of contiguous data, the device has a READ SEQUENTIAL instruction which accepts a starting address of the block and continuously outputs data of subsequent addresses until the end of memory, or until Chip Select goes LOW.

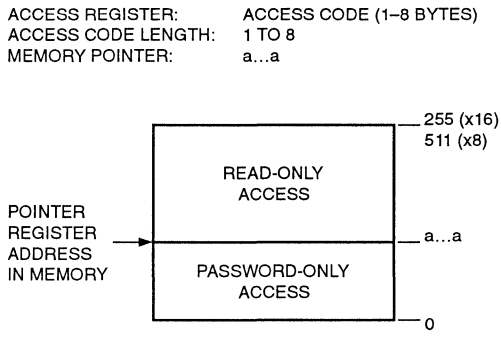
The CAT35C804A-B/CAT35C804A-BI communicates with external devices via an asynchronous serial communication protocol. The data transmission may be a continuous stream of data or it can be packed by pulsing Chip Select LOW in between each packet of information. (Except for the SEQUENTIAL READ instruction where Chip Select must be held high).

PIN DESCRIPTIONS

CS

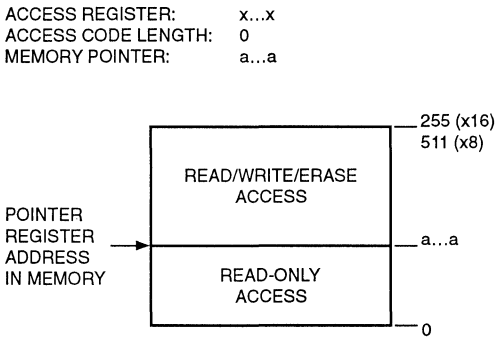
Chip Select is a TTL compatible input which, when set HIGH, allows normal operation of the device. Any time Chip Select is set LOW, it resets the device, terminating all I/O communication, and puts the output in a high impedance state. CS is used to reset the device if an error condition exists or to put the device in a power-down mode to minimize power consumption. It may also be used to frame data transmission in applications where the clock and data input have to be ignored from time to time. Although CS resets the device, it does not change the program/erase or the access-enable status, nor does it terminate a programming cycle once it has started. The program/erase and access-enable operations, once enabled, will remain enabled until specific disabling instructions are sent or until power is removed.

Figure 2. Secure Mode



5074 FHD F04

Figure 3. Unprotected Mode(10)



5074 FHD F05

Note:
(10) x = DON'T CARE; a = ADDRESS BIT.

CLK

The System Clock is a TTL compatible input pin that allows operation of the device at a specified frequency. The CAT35C804A-B/CAT35C804A-BI is designed with an internal divider to produce a 9600 baud output for an input clock frequency of 4.9152 MHz and 3.579545 MHz respectively.

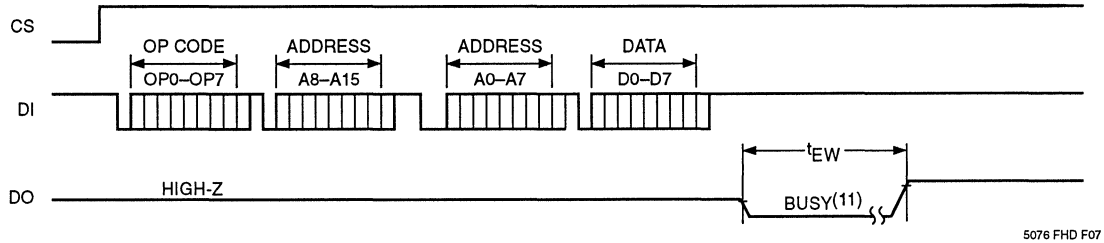
DI

The Data Input pin is TTL compatible and accepts data and instructions in a serial format. Each byte must begin with "0" as a start bit. The device will accept as many bytes as an instruction requires, including both data and address bytes. Extra bits will be disregarded if they are "1"s and extra "0"s will be misinterpreted as the start bit of the next instruction. An instruction error will cause the device to abort operation and all I/O communication will be terminated until a reset is received.

DO

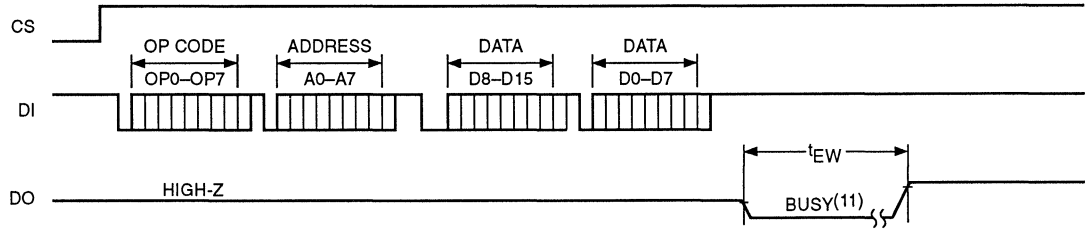
The Data Output pin is a tri-state TTL compatible output. It is normally in a high impedance state unless a READ or an ENABLE BUSY instruction is executed. Following the completion of a 16 bit or 8 bit data stream, the output will return to the high impedance state. During a program/erase cycle, if the ENABLE BUSY instruction has been previously executed, the output will stay LOW while the device is BUSY, and it will be set HIGH when the program/erase cycle is completed. DO will stay HIGH until the completion of the next instruction's opcode and, if the next instruction is a READ, DO will output the appropriate data at the end of the instruction. If the

Figure 4. Program/Erase Timing (x8 Format)



5076 FHD F07

Figure 5. Program/Erase Timing (x16 Format)



5076 FHD F08

Note:
(11) DO becomes low to indicate busy status if ENBSY was previously executed. If ENBSY was not previously executed, DO will be in the High-Z condition.

ENABLE BUSY instruction has not been previously executed, DO will stay in a high impedance state. DO will also go to the high impedance state if an error condition is detected. In the event an ENABLE BUSY instruction has not been sent, a READ STATUS register instruction can be executed. This also tells the user whether the part is in a program/erase cycle or an error condtion. When the device is in a program/erase cycle it will output an 8 bit status word. If it does not, it is in an error condition.

PE

The Parity Enable pin is a TTL compatible input. If the PE pin is set HIGH, the device will be configured to communicate using even parity, and if the pin is set LOW, it will use no parity. In this case, instructions or data that include parity bits will not be interpreted correctly. Note: The PE input is internally pulled down to GND (i.e. default = no parity). As with all CMOS devices, CS, CLK and DI inputs must be connected to either HIGH or LOW, and not left floating.

$\overline{\text{ERR}}$

The Error indication pin is an open drain output. If either an instruction or parity error exists, the $\overline{\text{ERR}}$ pin will output a "0" until the device is reset. This can be done by pulsing CS LOW.

Figure 6. Read Timing (x8 Format)

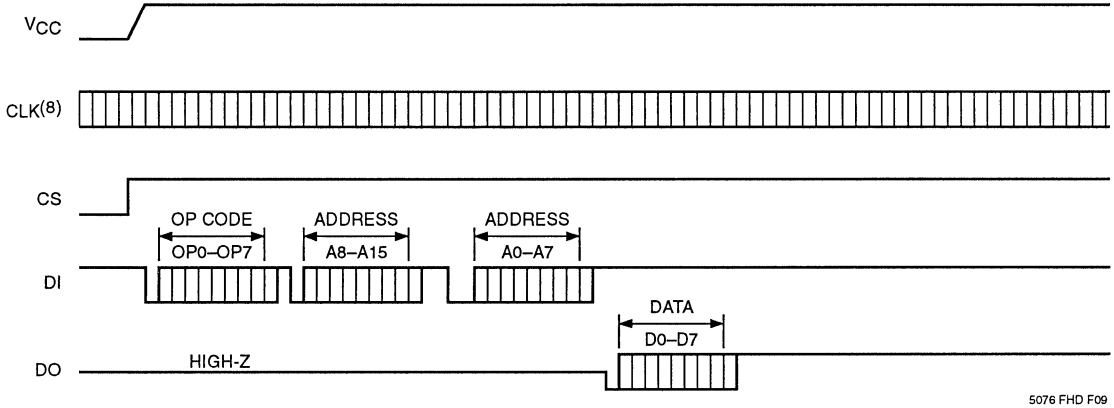
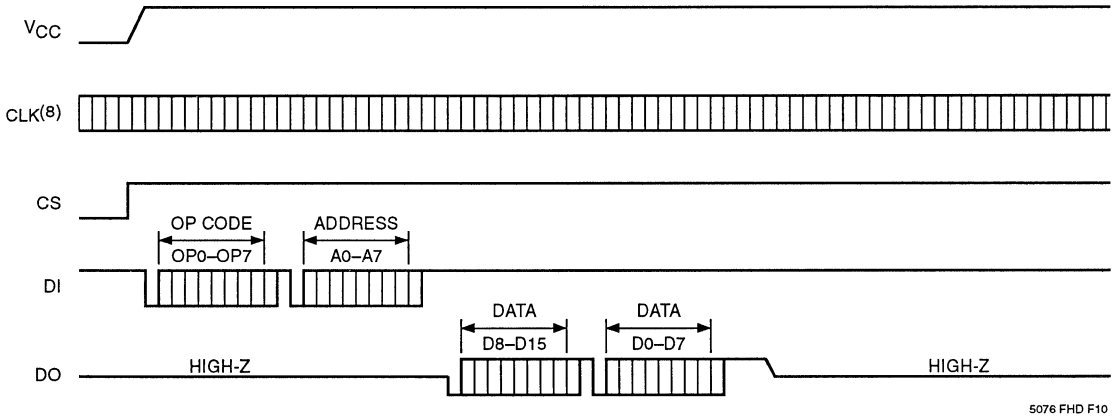


Figure 7. Read Timing (x16 Format)



Note:
(8) Clock = 4.9152 MHz for the CAT35C804A or 3.579545 MHz for the CAT35C804B.

DEVICE OPERATION

INSTRUCTIONS

The CAT35C804A-B/CAT35C804A-BI instruction set includes 19 instructions.

Six instructions are related to security or write protection:

DISAC	Disable Access
ENAC	Enable Access
MACC	Modify Access Code
OVMPR	Override Memory Pointer Register
RMPR	Read Memory Pointer Register
WMPR	Write Memory Pointer Register

Six instructions are READ/WRITE/ERASE instructions:

ERAL	Clear All Locations
ERASE	Clear Memory Locations
READ	Read Memory
RSEQ	Read Sequentially
WRAL	Write All
WRITE	Write memory

Note: All write instructions will automatically perform a clear before writing data.

Seven instructions are used as control and status functions:

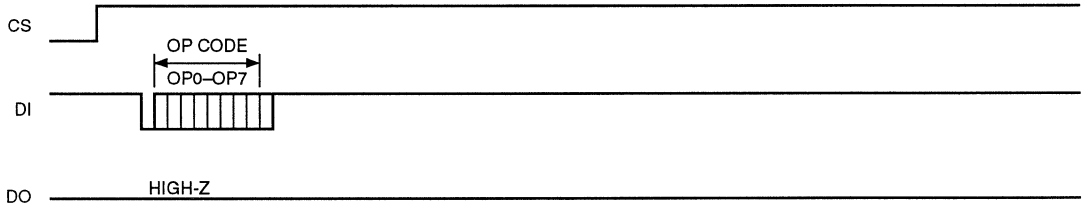
DISBSY	Disable Busy
ENBSY	Enable Busy
EWEN	Program/Erase Enable
EWDS	Program/Erase Disable
NOP	No Operation
ORG	Select Memory Organization
RSR	Read Status Register

UNPROTECTED MODE

As shipped from the factory, the CAT35C804A-B/CAT35C804A-BI is in the unprotected mode. The access code length is set to 0, and the memory pointer is at address 00 hex. While in this mode, any portion of the E^2PROM array can be read or written to without an access code. A portion of the memory may be protected from any write or clear operation by setting the memory pointer to the appropriate address via the WMPR (Write Memory Pointer Register) instruction:

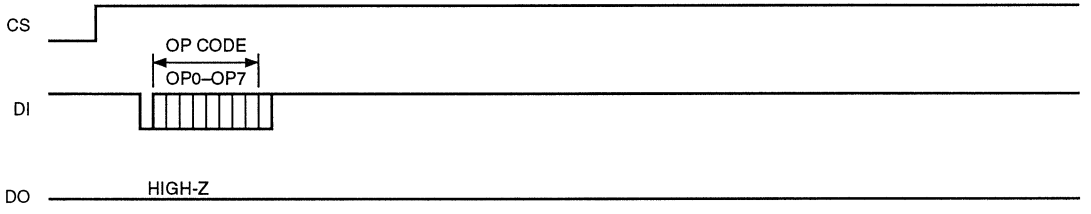
WMPR [address]

Figure 8. EWEN/EWDS Timing (x8 Format)



5076 FHD F11

Figure 9. EWEN/EWDS Timing (x16 Format)



5076 FHD F11

As shown previously in Figure 3, memory locations below the address set in the memory pointer will be program/erase protected. Thus, unintentional clearing or writing of data in this area will be prevented, while memory locations at or above the protected area still allow full access. This protection does not apply to the ERAL and WRAL commands which are not blocked by the memory pointer.

SECURE MODE

As shown previously in Figure 2, in the secure mode, memory locations at or above the address set in the memory pointer allow READ-only access. Memory locations below that address will require an access code before they can be accessed. The secure mode is activated with an MACC (Modify Access Code) instruction followed by a user access code which can be one to eight bytes in length.

EWEN
MACC [old code][new code][new code]

The EWEN instruction enables the device to perform program/erase operations. The new access code must be entered twice for verification. If the device already has an access code, the old access code must be entered before the new access code can be accepted. The length of the password is incorporated into the MACC portion of the instruction.

Once the secure mode is activated, access to memory locations is under software control. Access (read, write, and clear instructions) to the memory locations below the address in the memory pointer is allowed only if the ENAC (Enable Access) instruction followed by the correct access code has been previously executed.

ENAC [access code]
EWEN
WRITE [address][data]

The ENAC instruction, along with the access code, enables access to the protected area of the device. The EWEN instruction enables execution of the program/erase operations. This portion of the memory is otherwise inaccessible for any operation. Read-only access is allowed without the access code for memory locations at or above the address in the memory pointer.

The access code can be changed by the following instruction:

ENAC [old access code]
EWEN
MACC [old code][new code][new code]

A two-tier protection scheme is implemented to protect data against inadvertent clearing or writing. To write to the memory, an EWEN (Program/Erase Enable) must first be issued. The CAT35C804A-B/CAT35C804A-BI will now allow program/erase operations to be performed only on memory locations at or above the address set in the memory pointer. The remaining portion of the memory is still protected. To override this protection, an OVMPR (Override Memory Pointer Register—see Memory Pointer Register) must be issued for every program/erase instruction which accesses the protected area:

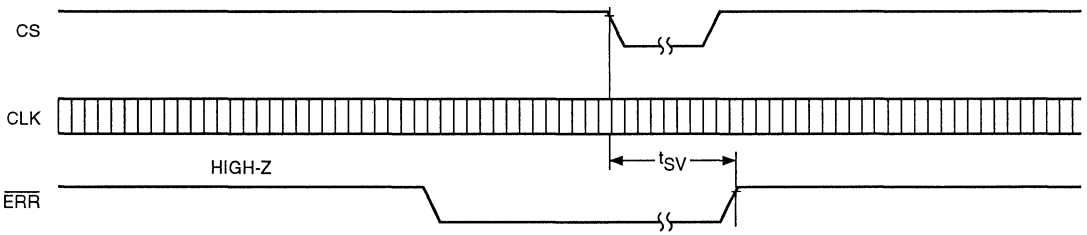
ENAC [access code]
EWEN
OVMPR
WRITE [address][data]

As an alternative to the OVMPR instruction, the WMPR (Write Memory Pointer Register) instruction may be used to move the memory pointer address to uncover the area where writing is to be performed:

ENAC [access code]
EWEN
WMPR [address]
WRITE [address][data]

6

Figure 10. $\overline{ERR}$ Pin Timing



5076 FHD F06

As shipped from the factory, the device is in the unprotected mode. The length of the access code is user selectable from a minimum of one byte to a maximum of eight bytes (> 1.84×10^{19} combinations). Loading a zero-length access code will disable protection.

MEMORY POINTER REGISTER

The memory pointer enables the user to segment the E^2PROM array into two sections. In the unprotected mode, the array can be segmented between read-only and full access, while in the secure mode, the memory may be segmented between read-only access and password-only access. Three instructions are dedicated to the memory pointer operations. The first one is WMPR (Write Memory Pointer Register). This instruction, followed by an address, will load the memory pointer register with a new address. This address will be stored in the E^2PROM and can be modified only by another WMPR instruction. The second instruction is OVMPR (Override Memory Pointer Register) which allows a single program/erase to be performed to memory locations below the address set in the memory pointer. This instruction allows the user to modify data in a segmented array without having to move the memory pointer. Once the operation is complete, the device returns to the protected mode. If the device is in the secure mode both of these instructions require the ENAC instruction and a valid access code prior to their execution. The third instruction is the RMPR (Read Memory Pointer Register) which will place the current contents of the register in the serial output buffer.

STATUS REGISTER

An eight bit status register is provided to allow the user to determine the status of the CAT35C804A-B/CAT35C804A-BI. The contents of the first three bits of the register are 101 which allows the user to quickly determine the condition of the device. The next three bits indicate the status of the device; they are parity error, instruction error and RDY/$\overline{\text{BUSY}}$ status. The last two bits are reserved for future use.

CLEAR ALL AND WRITE ALL

As a precaution, the ERAL instruction has to be entered twice before it is executed. This measure is required as a redundancy check on the incoming instruction for possible transmission errors. The WRAL instruction requires sending an ERAL first (this sets a flag only) and

Figure 11. Erase Timing (x8 Format)

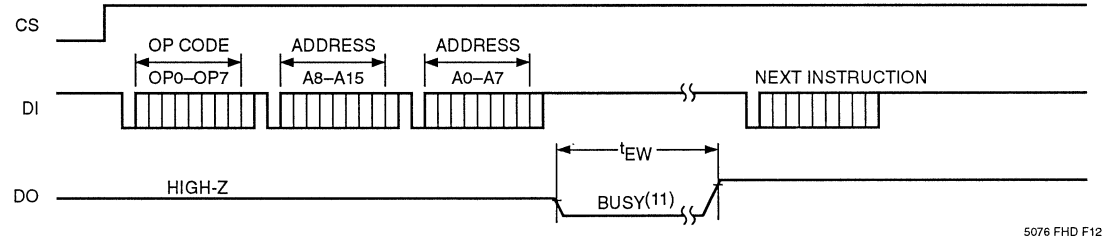
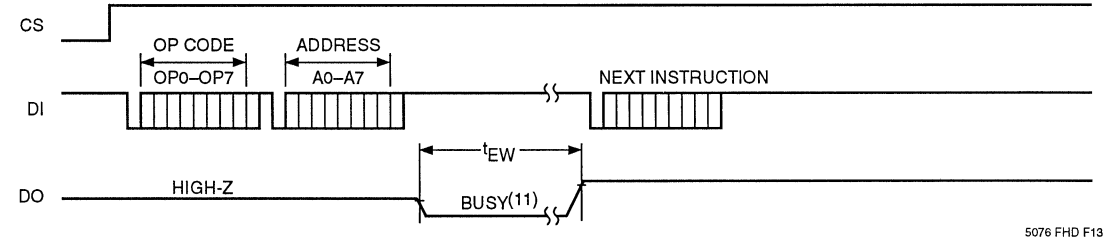


Figure 12. Erase Timing (x16 Format)



Note:
(11) DO becomes low to indicate busy status if ENBSY was previously executed. If ENBSY was not previously executed, DO will be in High-Z condition.

then the WRAL instruction. The CAT35C804A-B/CAT35C804A-BI will accept the following commands:

ERAL	**ERAL**	An ERAL will be executed
ERAL	**WRAL**	A WRAL will be executed

Both the ERAL and WRAL commands will program/erase the entire array and will not be blocked by the memory pointer.

THE PARITY BIT

The UART compatible protocol supports an even parity bit if the PE pin of the device is set HIGH, otherwise, there is no parity. If PE is set LOW and the incoming instruction contains a parity bit, it may be interpreted as the stop bit. When PE is HIGH, the CAT35C804A-B/CAT35C804A-BI expects a parity bit at the end of every byte. For example, the RSEQ instruction will look like this:

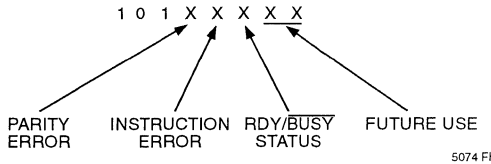
0 1100 1011 11
0 A15...A8 P1
0 A7...A0 P1

The device then outputs data continuously until it reaches the end of the memory. Each byte of data contains 9 bits with the ninth bit being the parity bit. The RSEQ instruction may be terminated at any time by bringing CS low; the output will then go to high impedance.

SYSTEM ERRORS

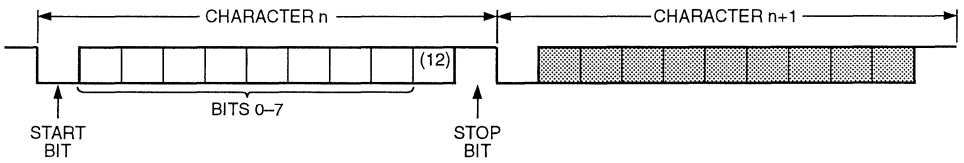
Whenever an error occurs, be it an instruction error (unknown instruction), or parity error (perhaps caused by transmission error), the device will stop its operation. To return to normal operation, the device must be reset by pulsing CS LOW and then set back to HIGH. Resetting the device will not affect the ENAC, EWEN and ENBSY status. The error may be determined by entering the READ STATUS REGISTER (RSR) instruction immediatly following the reset. The status output is an 8 bit word with the first three bits being 101. This three bit pattern indicates that the device is functioning normally. The fourth bit is "1" if a parity error occurred. The fifth bit is a "1" if an instruction error occurred. The sixth bit is a "1" if the device is in a program/erase cycle. The last two bits are reserved for future use.

The reason for the "101" pattern is to distinguish between an error conditon (DO tri-stated) and a device busy status. If an error condition exists, it will not respond to any input instruction from DI. However, if the device is in a program/erase cycle, it responds to the RSR instruction by outputting "101 00100". If RSR is executed at the end of a program/erase cycle, the output will be "101000 00".



5074 FHD F09

Figure 13. Asynchronous Communication Protocol



5076 FHD F14

Note:
(12) Parity bit if enabled; skipped if parity disabled.

INSTRUCTION SET

DISAC Disable Access

1000	1000

This instruction will lock the memory from all program/erase operations regardless of the contents of the memory pointer. A write can be accomplished only by first entering the ENAC instruction followed by a valid access code.

ENAC Enable Access

1100	0101	[Access Code]

In the protected mode, this instruction, followed by a valid access code, unlocks the device for read/write/clear access.

WMPR Write Memory Pointer Register

1100	0100	[A15–A8] [A7–A0] *(x8 organization)*

1100	0100	[A7–A0] *(x16 organization)*

The WMPR instruction followed by 8 or 16 bits of address (depending on the organization) will move the pointer to the newly specified address.

MACC Modify Access Code

1101	[Length] [Old code] [New code] [New code]

This instruction requires the user to enter the old access code, if one was set previously, followed by the new access code and a re-entry of the new access code for verification. Within the instruction format, the variable [Length] designates the length of the access code as the following:

[Length] = [0] No access code. Set device to unprotected mode.

[Length] = [1–8] Length of access code is 1 to 8 bytes.

[Length] = [>8] Illegal number of bytes. The CAT35C804A-B/CAT35C804A-BI will ignore the rest of the transmission.

RMPR Read Memory Pointer Register

1100	1010

Output the content of the memory pointer register to the serial output port.

Figure 14. ERAL Timing (x8 Format)

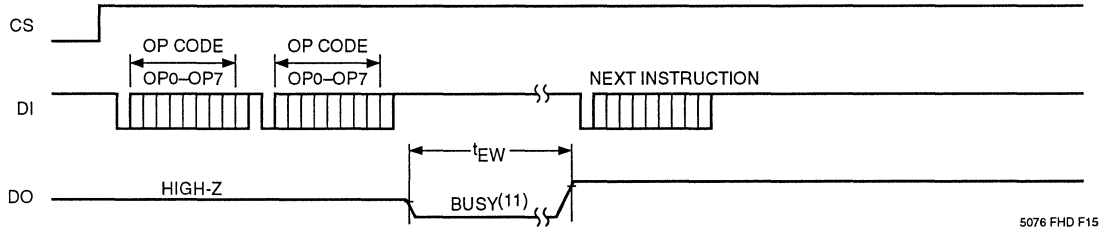
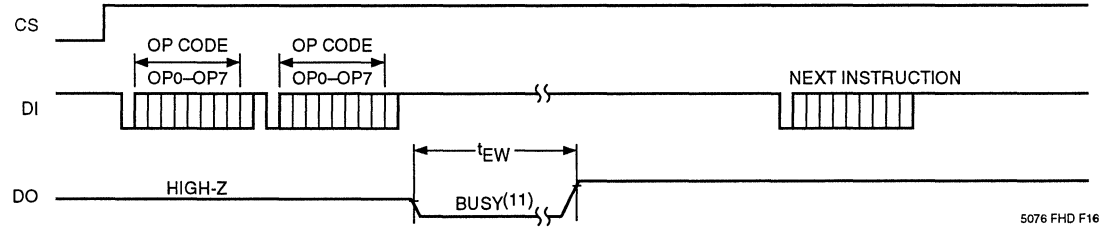


Figure 15. ERAL Timing (x16 Format)



Note:
(11) DO becomes low to indicate busy status if ENBSY was previously executed. If ENBSY was not previously executed, DO will be in the High-Z condition.

OVMPR Override Memory Pointer Register

1000	0011

Override the memory protection for the next instruction.

READ Read Memory

1100	1001	[A15–A8] [A7–A0] *(x8 organization)*
1100	1001	[A7–A0] *(x16 organization)*

Output the contents of the addressed memory location to the serial port.

WRITE Write Memory

1100	0001	[A15–A8] [A7–A0] [D7–D0] *(x8 organization)*
1100	0001	[A7–A0] [D15–D8] [D7–D0] *(x16 organization)*

Write the 8 bit or 16 bit data to the addressed memory location. After the instruction, address, and data have been entered, the self-timed program/erase cycle will start. The addressed memory location will be erased before data is written. The DO pin may be used to output the RDY/$\overline{\text{BUSY}}$ status by having previously entered the ENBSY instruction. During the program/erase cycle, DO will output a LOW for BUSY during this cycle and a HIGH for READY after the cycle has been completed.

ERASE Clear Memory

1100	0000	[A15–A8] [A7–A0] *(x8 organization)*
1100	0000	[A7–A0] *(x16 organization)*

Erase data in the specified memory location (set memory to "1"). After the instruction and the address have been entered, the self-timed clear cycle will start. The DO pin may be used to output the RDY/$\overline{\text{BUSY}}$ status by having previously entered the ENSBY instruction. During the clear cycle, DO will output a LOW for BUSY during this cycle and a HIGH for ready after the cycle has been completed.

ERAL Clear All

1000	1001
1000	1001

Erase the data of all memory locations (all cells set to "1"). For protection against inadvertent chip clear, the ERAL instruction is required to be entered twice.

6

Figure 16. WRAL Timing (x8 Format)

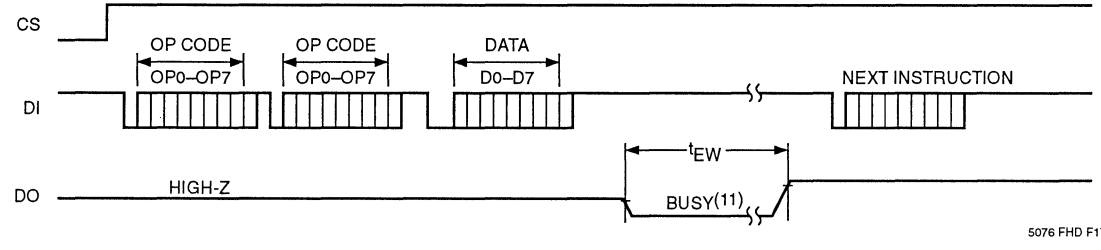
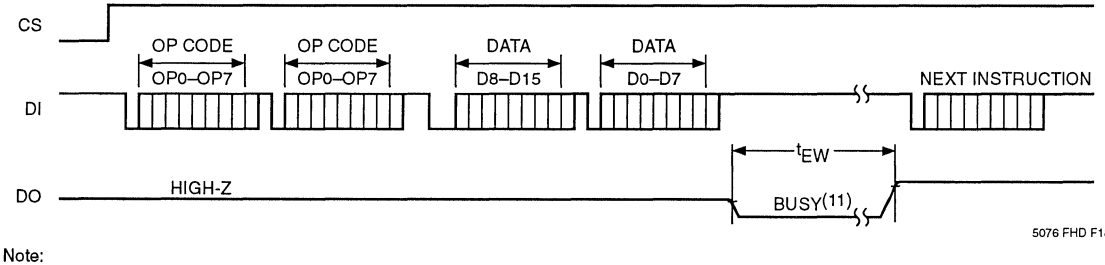


Figure 17. WRAL Timing (x16 Format)



Note:
(11) DO becomes low to indicate busy status if ENBSY was previously executed. If ENBSY was not previously executed, DO will be in the High-Z condition.

WRAL Write All

1000	1001	
1100	0011	[D15–D8] [D7–D0] *(x16 organization)*
1000	1001	
1100	0011	[D7–D0] *(x8 organization)*

Write one or two bytes of data to all memory locations. An ERAL will be automatically performed before the WRAL is executed. For protection against inadvertent clearing or writing of data, the ERAL instruction is required to be entered preceding the WRAL instruction.

RSEQ Read Sequentially

1100	1011	[A15–A8] [A7–A0] *(x8 organization)*
1100	1011	[A7–A0] *(x16 organization)*

Read memory starting from specified address, sequentially to the highest address or until CS goes LOW. The instruction is terminated when CS goes LOW.

ENBSY Enable Busy

1000	0100

Enable the status indicator on DO during program/erase cycle. DO goes LOW then HIGH once the write cycle is complete. DO will go to HIGH-Z at the end of the next op code transmission.

DISBSY Disable Busy

1000	0101

Disable the status indicator on DO during program/erase cycle.

EWEN Program/Erase Enable

1000	0001

Enable program/erase to be performed on non-protected portion of memory. This instruction must be entered before any program/erase instruction will be carried out. Once entered, it will remain valid until power-down or an EWDS (Program/Erase Disable) is executed.

EWDS Program/Erase Disable

1000	0010

Disable all write and clear functions.

ORG Select Memory Organization

1000	011R	*(where R = 0 or 1)*

Set memory organization to 512 x 8 if R = 0.

Set memory organization to 256 x 16 if R = 1.

RSR Read Status Register

1100	1000

Output the contents of the 8 bit status register. The contents of the first three bits of the register are 101, which allows the user to quickly determine whether the device is listening or is in an error condition. The next three bits indicate parity error, instruction error and RDY/$\overline{\text{BUSY}}$ status. The last two bits are reserved for future use.

NOP No Operation

1000	0000

No Operation.

CATALYST SEMICONDUCTOR

Product Information 1

2-Wire Bus Serial E^2PROMs 2

3-Wire Bus Serial E^2PROMs 3

SPI Bus Serial E^2PROMs 4

4-Wire Bus Serial E^2PROMs 5

Secure Access Serial E^2PROMs 6

Parallel E^2PROMs 7

Flash Memories 8

EPROMs 9

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Contents

SECTION 7 PARALLEL E^2PROMS

CAT28C16A/CAT28C16AI	2K x 8	16K-Bit	7-1
CAT28C16V3	2K x 8	16K-Bit	7-9
CAT28C17A/CAT28C17AI	2K x 8	16K-Bit	7-17
CAT28C64A/CAT28C64AI	8K x 8	64K-Bit	7-25
CAT28C65A/CAT28C65AI	8K x 8	64K-Bit	7-33
CAT28C64B/CAT28C64BI	8K x 8	64K-Bit	7-41
CAT28C65B/CAT28C65BI	8K x 8	64K-Bit	7-51
CAT28C256/CAT28C256I	32K x 8	256K-Bit	7-61

CAT28C16A/CAT28C16AI

16K-Bit CMOS E²PROM

FEATURES

- Fast Read Access Times: 200 ns
- Low Power CMOS Dissipation:
  - –Active: 25mA Max.
  - –Standby: 100µA Max.
- Simple Write Operation:
  - –On-Chip Address and Data Latches
  - –Self-Timed Write Cycle with Auto-Clear
- Fast Nonvolatile Write Cycle: 10ms Max
- End of Write Detection: $\overline{\text{DATA}}$ Polling
- Hardware Write Protection
- CMOS and TTL Compatible I/O
- 10,000 Program/Erase Cycles
- 10 Year Data Retention

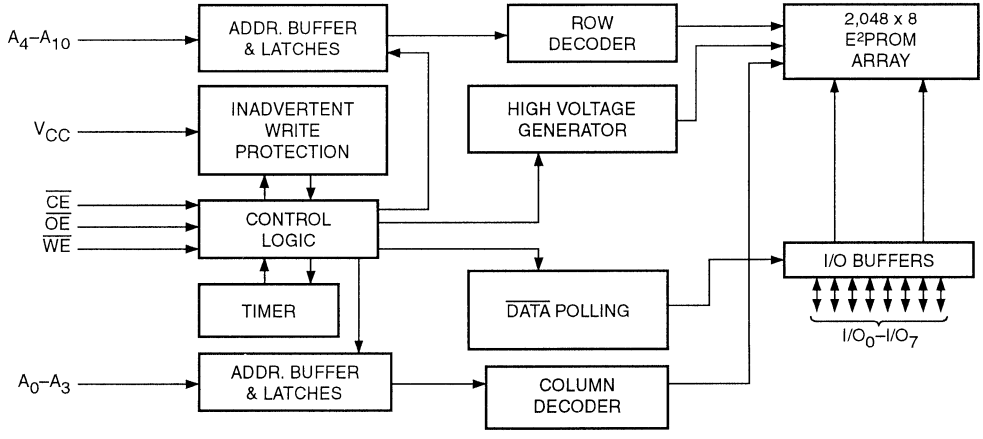
DESCRIPTION

The CAT28C16A/CAT28C16AI is a fast, low power, 5V-only CMOS E²PROM organized as 2K x 8 bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling signals the start and end of the self-timed write cycle. Additionally, the CAT28C16A/CAT28C16AI features hardware write protection.

The CAT28C16A/CAT28C16AI is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 24 pin DIP and SO or 32 pin PLCC packages.

7

BLOCK DIAGRAM

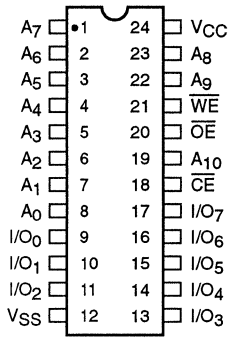


5089 FHD F02

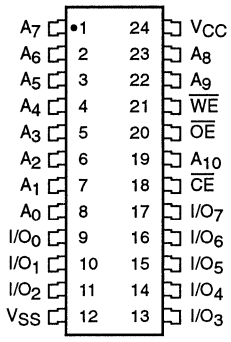
TD 5089

PIN CONFIGURATION

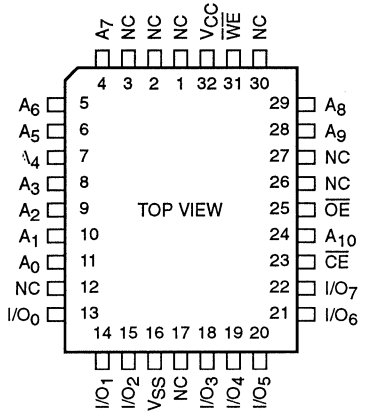
DIP Package



SO Package



PLCC Package



5089 FHD F01

PIN FUNCTIONS

Pin Name	Function
A_0–A_{10}	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	5V Supply
V_{SS}	Ground
NC	No Connect

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with
Respect to Ground(2) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation
Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(3) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(1)	Endurance	10,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(1)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT28C16A T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C16AI T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	V_{CC} Current (Operating, TTL)			35	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 1/t_{RC} min, All I/O's Open
I_{CCC}(5)	V_{CC} Current (Operating, CMOS)			25	mA	$\overline{CE}$ = $\overline{OE}$ = V_{ILC}, f = 1/t_{RC} min, All I/O's Open
I_{SB}	V_{CC} Current (Standby, TTL)			1	mA	$\overline{CE}$ = V_{IH}, All I/O's Open
I_{SBC}(6)	V_{CC} Current (Standby, CMOS)			100	µA	$\overline{CE}$ = V_{IHC}, All I/O's Open
I_{LI}	Input Leakage Current	–10		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	–10		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IH}(6)	High Level Input Voltage	2.0		V_{CC} +0.3	V	
V_{IL}(5)	Low Level Input Voltage	–0.3		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1mA
V_{WI}	Write Inhibit Voltage	3.0			V	

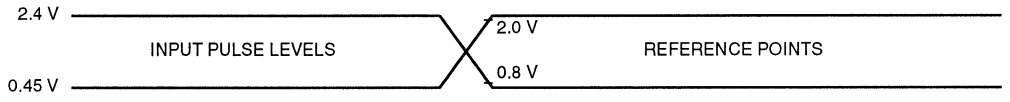
Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} +1V.
(5) V_{ILC} = –0.3V to +0.3V.
(6) V_{IHC} = V_{CC} –0.3V to V_{CC} +0.3V.

A.C. CHARACTERISTICS, Read Cycle

CAT28C16A T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C16AI T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

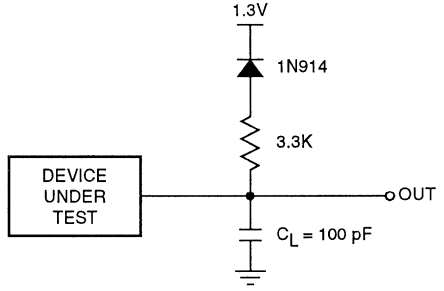
Symbol	Parameter	28C16A-20 28C16AI-20		Units
		Min.	Max.	
t_{RC}	Read Cycle Time	200		ns
t_{CE}	$\overline{CE}$ Access Time		200	ns
t_{AA}	Address Access Time		200	ns
t_{OE}	$\overline{OE}$ Access Time		80	ns
t_{LZ}(1)	$\overline{CE}$ Low to Active Output	0		ns
t_{OLZ}(1)	$\overline{OE}$ Low to Active Output	0		ns
t_{HZ}(1)(7)	$\overline{CE}$ High to High-Z Output		55	ns
t_{OHZ}(1)(7)	$\overline{OE}$ High to High-Z Output		55	ns
t_{OH}(1)	Output Hold from Address Change	0		ns

Figure 1. A.C. Testing Input/Output Waveform(8)



5089 FHD F03

Figure 2. A.C. Testing Load Circuit (example)



C_L INCLUDES JIG CAPACITANCE

5089 FHD F04

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(7) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.
(8) Input rise and fall times (10% and 90%) < 10 ns.

A.C. CHARACTERISTICS, Write Cycle

CAT28C16A T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C16AI T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C16A-20 28C16AI-20		Units
		Min.	Max.	
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}(9)	$\overline{CE}$ Pulse Time	150		ns
t_{OES}	$\overline{OE}$ Setup Time	15		ns
t_{OEH}	$\overline{OE}$ Hold Time	15		ns
t_{WP}(9)	$\overline{WE}$ Pulse Width	150		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{DL}	Data Latch Time	50		ns
t_{INIT}(1)	Write Inhibit Period After Power-up	5	20	ms

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(9) A write pulse of less than 20ns duration will not initiate a write cycle.

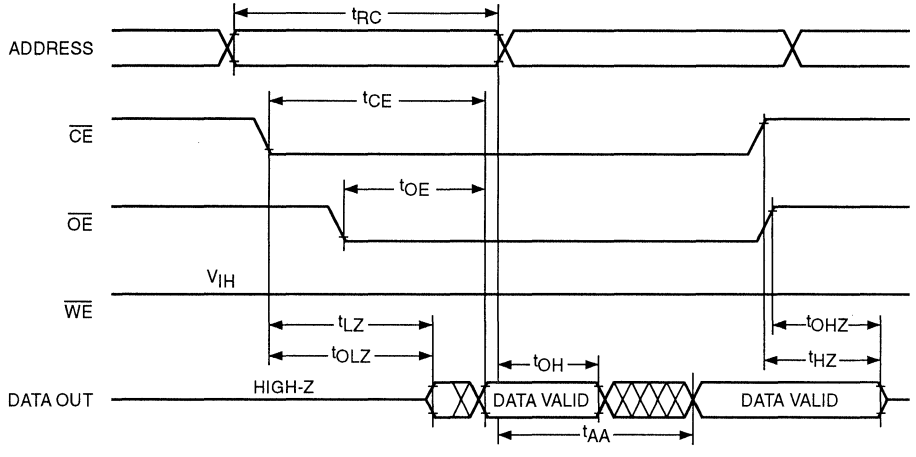
7

DEVICE OPERATION

Read

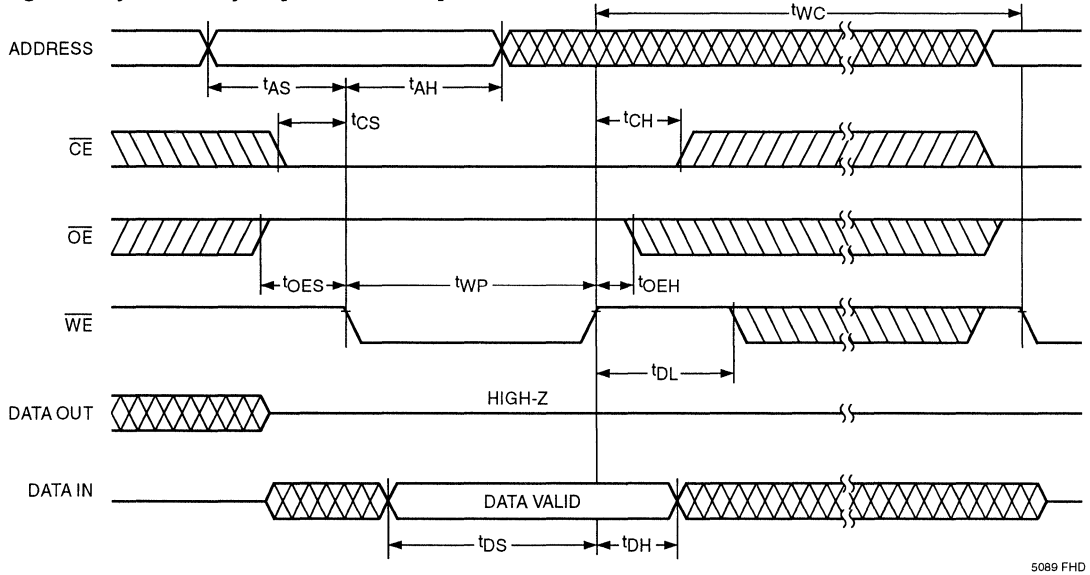
Data stored in the CAT28C16A/CAT28C16AI is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Figure 3. Read Cycle



5089 FHD F05

Figure 4. Byte Write Cycle [$\overline{WE}$ Controlled]



5089 FHD F06

Byte Write

A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 10 ms.

$\overline{DATA}$ Polling

$\overline{DATA}$ polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0–I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle, all I/O's will output true data during a read cycle.

Figure 5. Byte Write Cycle [$\overline{CE}$ Controlled]

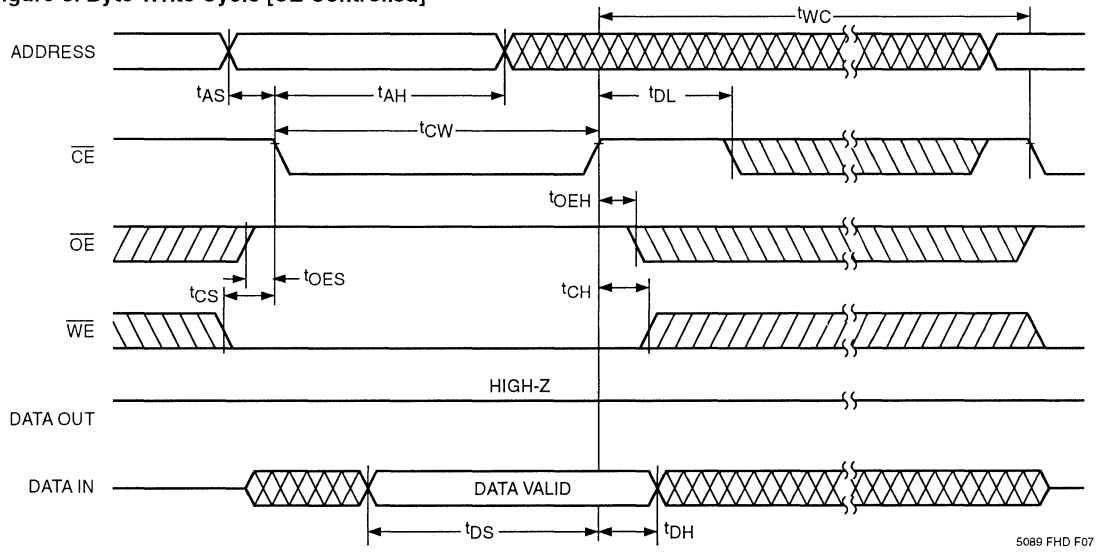
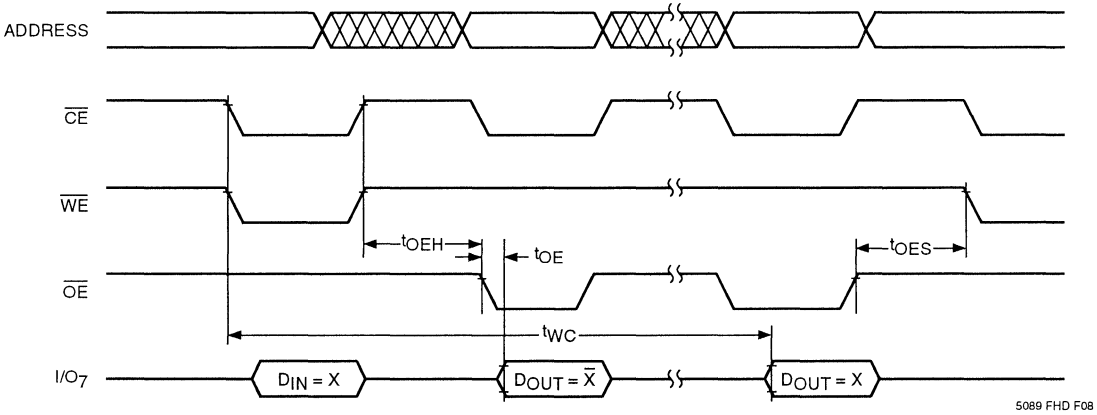


Figure 6. $\overline{DATA}$ Polling



HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28C16A/ CAT28C16AI.

(1) V_{CC} sense provides for write protection when V_{CC} falls below 3.0V min.

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 20 ms delay before a write sequence, after V_{CC} has reached 3.0V min.

(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

CAT28C16V3

16K-Bit CMOS POWER MISER™ E²PROM

FEATURES

- **Fast Read Access Times: 700 ns**
- **Low Power CMOS Dissipation:**
  - **–Active: 10mA Max.**
  - **–Standby: 50μA Max.**
- **Simple Write Operation:**
  - **–On-Chip Address and Data Latches**
  - **–Self-Timed Write Cycle with Auto-Clear**
- **Fast Nonvolatile Write Cycle: 20ms Max**
- **End of Write Detection: $\overline{DATA}$ Polling**
- **Hardware Write Protection**
- **CMOS and TTL Compatible I/O**
- **10,000 Program/Erase Cycles**
- **10 Year Data Retention**

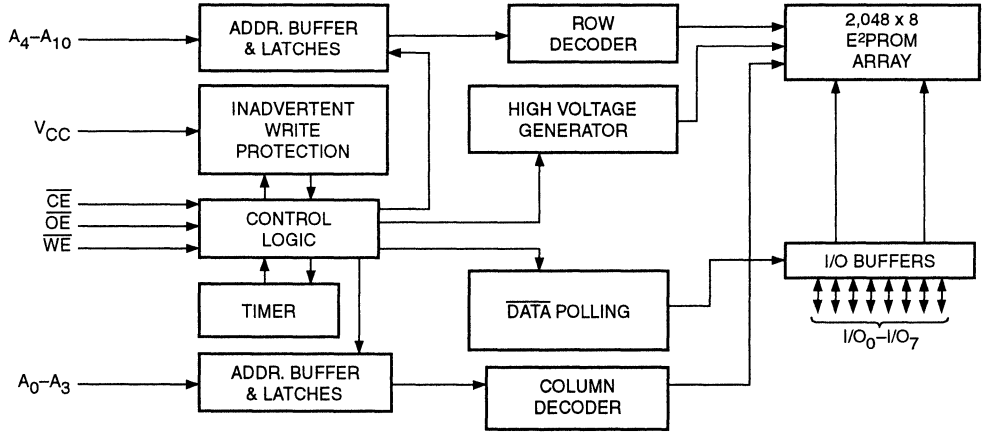
DESCRIPTION

The CAT28C16V3 is a fast, low power, 3V-only CMOS E²PROM organized as 2K x 8 bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{DATA}$ Polling signals the start and end of the self-timed write cycle. Additionally, the CAT28C16V3 features hardware write protection.

The CAT28C16V3 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 24 pin DIP and SO or 32 pin PLCC packages.

7

BLOCK DIAGRAM

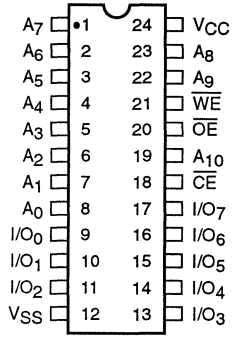


5089 FHD F02

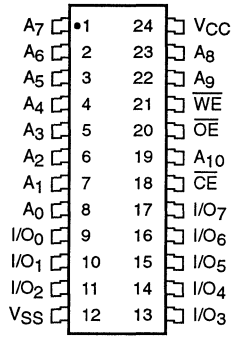
TD 5090

PIN CONFIGURATION

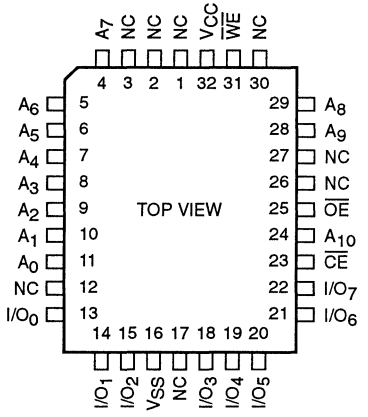
DIP Package



SO Package



PLCC Package



5089 FHD F01

PIN FUNCTIONS

Pin Name	Function
A_0–A_{10}	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	3V Supply
V_{SS}	Ground
NC	No Connect

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with Respect to Ground(2) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(3) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(1)	Endurance	10,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(1)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT28C16V3 T_A = 0°C to +70°C, V_{CC} = 3V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CCC}(5)	V_{CC} Current (Operating, CMOS)			10	mA	$\overline{CE}$ = $\overline{OE}$ = V_{ILC}, f = 1/t_{RC} min, All I/O's Open
I_{SBC}(6)	V_{CC} Current (Standby, CMOS)			50	µA	$\overline{CE}$ = V_{IHC}, All I/O's Open
I_{LI}	Input Leakage Current	–10		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	–10		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IH}(6)	High Level Input Voltage	V_{CC} –0.3		V_{CC} +0.3	V	
V_{IL}(5)	Low Level Input Voltage	–0.3		0.3	V	
V_{OH}	High Level Output Voltage	V_{CC} –0.3			V	I_{OH} = –10µA
V_{OL}	Low Level Output Voltage			0.3	V	I_{OL} = 10mA
V_{WI}	Write Inhibit Voltage	2.0			V	

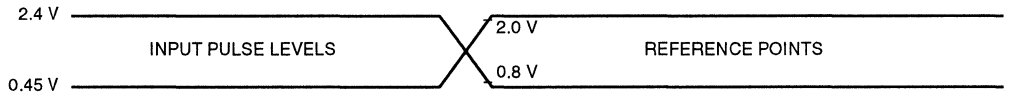
Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} +1V.
(5) V_{ILC} = –0.3V to +0.3V.
(6) V_{IHC} = V_{CC} –0.3V to V_{CC} +0.3V.

A.C. CHARACTERISTICS, Read Cycle

CAT28C16V3 T_A = 0°C to +70°C, V_{CC} = 3V ±10%, unless otherwise specified.

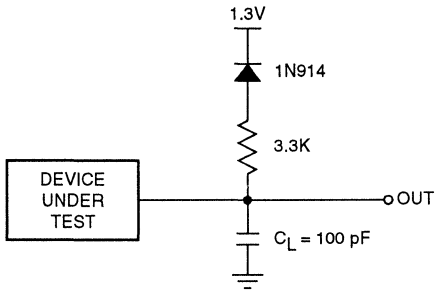
Symbol	Parameter	28C16V3-20		Units
		Min.	Max.	
t_{RC}	Read Cycle Time	700		ns
t_{CE}	$\overline{CE}$ Access Time		700	ns
t_{AA}	Address Access Time		700	ns
t_{OE}	$\overline{OE}$ Access Time		450	ns
t_{LZ}(1)	$\overline{CE}$ Low to Active Output	10		ns
t_{OLZ}(1)	$\overline{OE}$ Low to Active Output	10		ns
t_{HZ}(1)(7)	$\overline{CE}$ High to High-Z Output		80	ns
t_{OHZ}(1)(7)	$\overline{OE}$ High to High-Z Output		80	ns
t_{OH}(1)	Output Hold from Address Change	100		ns

Figure 1. A.C. Testing Input/Output Waveform(8)



5089 FHD F03

Figure 2. A.C. Testing Load Circuit (example)



C_L INCLUDES JIG CAPACITANCE

5089 FHD F04

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(7) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.
(8) Input rise and fall times (10% and 90%) < 10 ns.

A.C. CHARACTERISTICS, Write Cycle

CAT28C16V3 T_A = 0°C to +70°C, V_{CC} = 3V ±10%, unless otherwise specified.

Symbol	Parameter	28C16V3-20		Units
		Min.	Max.	
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	150		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}(9)	$\overline{CE}$ Pulse Time	200		ns
t_{OES}	$\overline{OE}$ Setup Time	20		ns
t_{OEH}	$\overline{OE}$ Hold Time	20		ns
t_{WP}(9)	$\overline{WE}$ Pulse Width	200		ns
t_{DS}	Data Setup Time	100		ns
t_{DH}	Data Hold Time	20		ns
t_{DL}	Data Latch Time	100		ns
t_{INIT}(1)	Write Inhibit Period After Power-up	10	30	ms

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(9) A write pulse of less than 20ns duration will not initiate a write cycle.

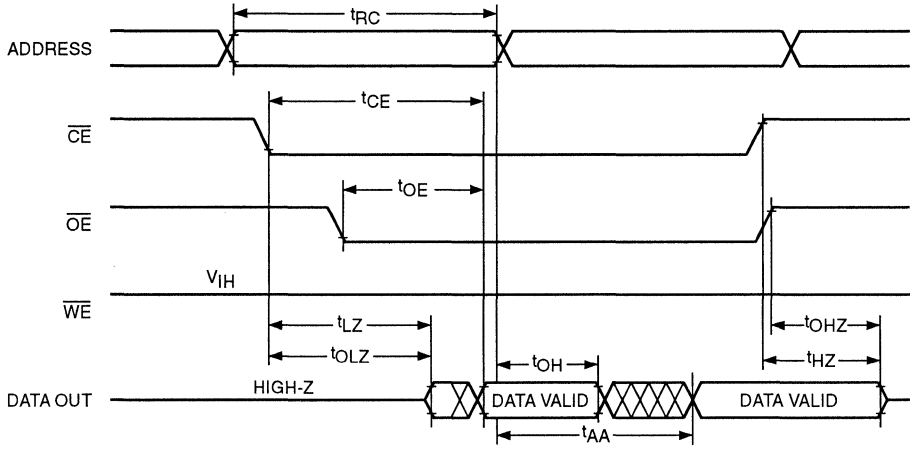
7

DEVICE OPERATION

Read

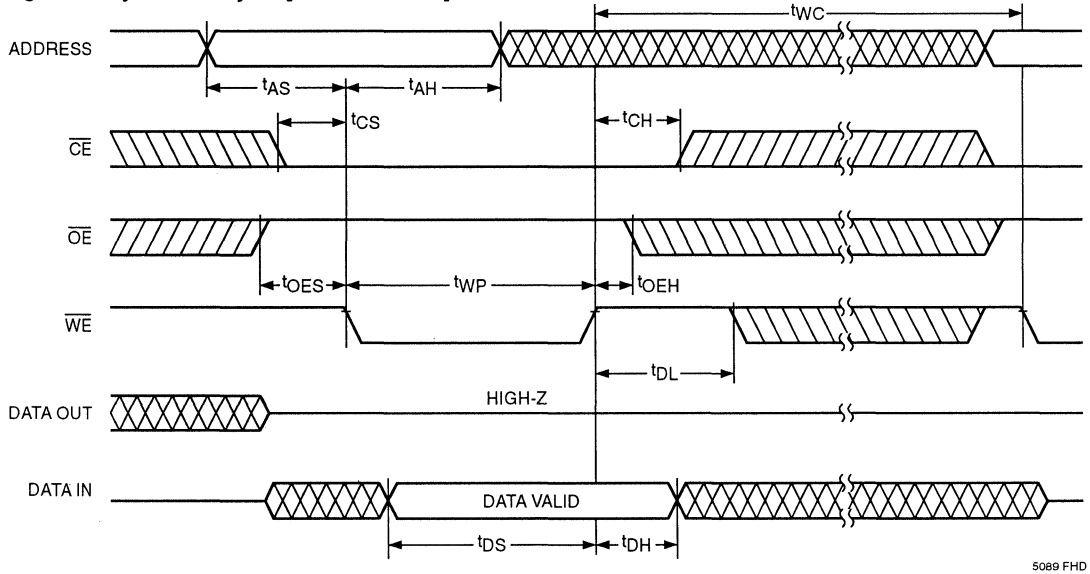
Data stored in the CAT28C16V3 is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Figure 3. Read Cycle



5089 FHD F05

Figure 4. Byte Write Cycle [$\overline{WE}$ Controlled]



5089 FHD F06

Byte Write

A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 20 ms.

$\overline{DATA}$ Polling

$\overline{DATA}$ polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0–I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle, all I/O's will output true data during a read cycle.

Figure 5. Byte Write Cycle [$\overline{CE}$ Controlled]

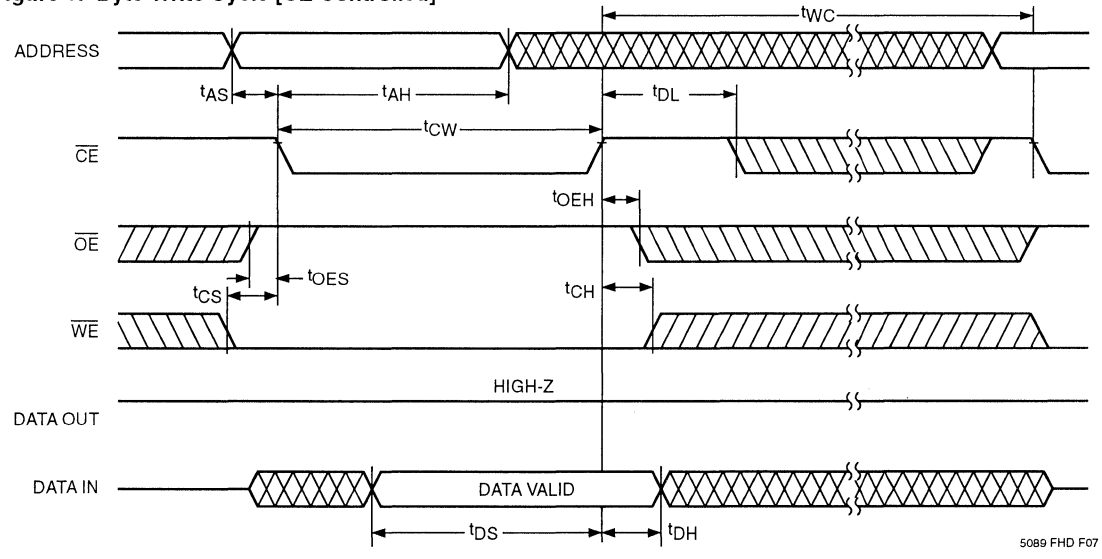
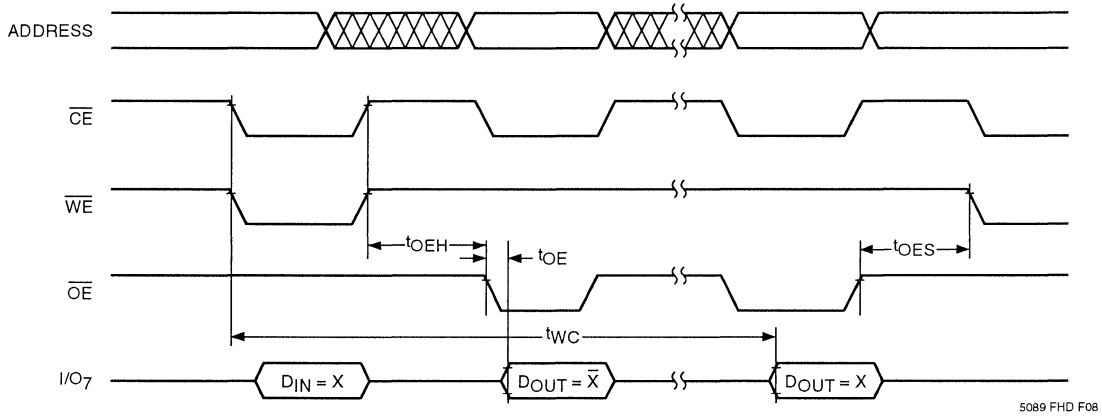


Figure 6. $\overline{DATA}$ Polling



HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28C16V3.

(1) V_{CC} sense provides for write protection when V_{CC} falls below 2.0V min.

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 10 to 30 ms delay before a write sequence, after V_{CC} has reached 2.0V min.

(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

CAT28C17A/CAT28C17AI

16K-Bit CMOS E²PROM

FEATURES

- **Fast Read Access Times: 200 ns**
- **Low Power CMOS Dissipation:**
  - **–Active: 25mA Max.**
  - **–Standby: 100μA Max.**
- **Simple Write Operation:**
  - **–On-Chip Address and Data Latches**
  - **–Self-Timed Write Cycle with Auto-Clear**
- **Fast Nonvolatile Write Cycle: 10ms Max**
- **End of Write Detection:**
  - **–$\overline{\text{DATA}}$ Polling**
  - **–RDY/$\overline{\text{BUSY}}$ Pin**
- **Hardware Write Protection**
- **CMOS and TTL Compatible I/O**
- **10,000 Program/Erase Cycles**
- **10 Year Data Retention**

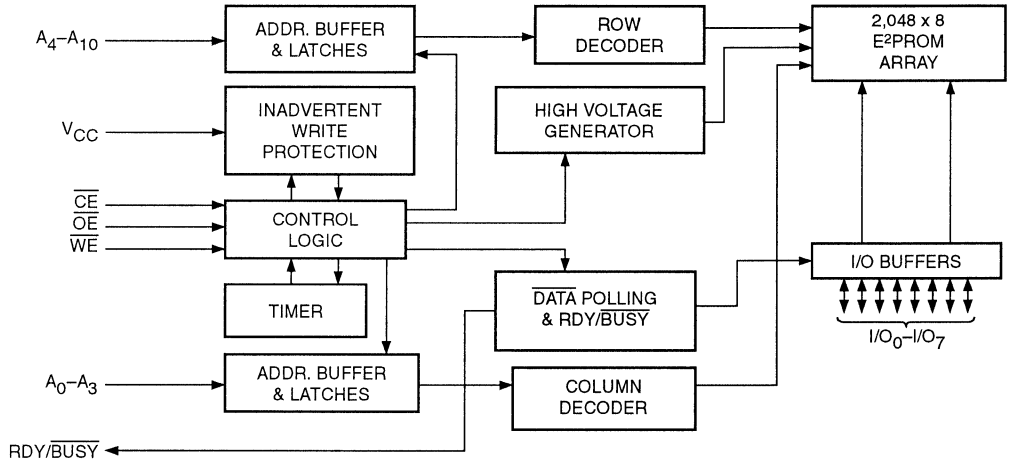
DESCRIPTION

The CAT28C17A/CAT28C17AI is a fast, low power, 5V-only CMOS E²PROM organized as 2K x 8 bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling and a RDY/$\overline{\text{BUSY}}$ pin signal the start and end of the self-timed write cycle. Additionally, the CAT28C17A/CAT28C17AI features hardware write protection.

The CAT28C17A/CAT28C17AI is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 28 pin DIP and SO or 32 pin PLCC packages.

7

BLOCK DIAGRAM

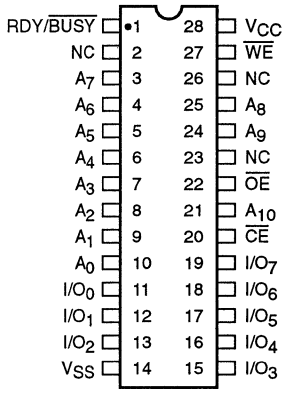


5091 FHD F02

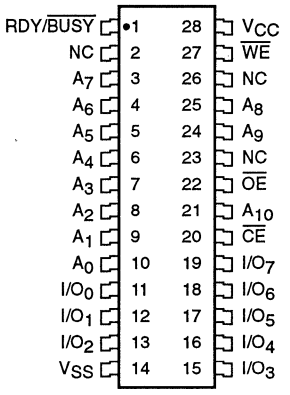
TD 5091

PIN CONFIGURATION

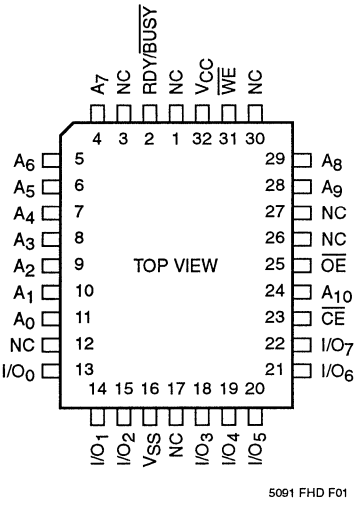
DIP Package



SO Package



PLCC Package



5091 FHD F01

PIN FUNCTIONS

Pin Name	Function
A_0–A_{10}	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
RDY/$\overline{BUSY}$	Ready/$\overline{BUSY}$ Status
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	5V Supply
V_{SS}	Ground
NC	No Connect

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −55°C to +125°C

Storage Temperature ..... −65°C to +150°C

Voltage on Any Pin with
Respect to Ground(2) ..... −2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... −2.0V to +7.0V

Package Power Dissipation
Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(3) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(1)	Endurance	10,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(1)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT28C17A T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C17AI T_A = −40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	V_{CC} Current (Operating, TTL)			35	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 1/t_{RC} min, All I/O's Open
I_{CCC}(5)	V_{CC} Current (Operating, CMOS)			25	mA	$\overline{CE}$ = $\overline{OE}$ = V_{ILC}, f = 1/t_{RC} min, All I/O's Open
I_{SB}	V_{CC} Current (Standby, TTL)			1	mA	$\overline{CE}$ = V_{IH}, All I/O's Open
I_{SBC}(6)	V_{CC} Current (Standby, CMOS)			100	µA	$\overline{CE}$ = V_{IHC}, All I/O's Open
I_{LI}	Input Leakage Current	−10		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	−10		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IH}(6)	High Level Input Voltage	2.0		V_{CC} +0.3	V	
V_{IL}(5)	Low Level Input Voltage	−0.3		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = −400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1mA
V_{WI}	Write Inhibit Voltage	3.0			V	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from −1V to V_{CC} +1V.
(5) V_{ILC} = −0.3V to +0.3V.
(6) V_{IHC} = V_{CC} −0.3V to V_{CC} +0.3V.

A.C. CHARACTERISTICS, Read Cycle

CAT28C17A T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C17AI T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C17A-20 28C17AI-20		Units
		Min.	Max.	
t_{RC}	Read Cycle Time	200		ns
t_{CE}	$\overline{CE}$ Access Time		200	ns
t_{AA}	Address Access Time		200	ns
t_{OE}	$\overline{OE}$ Access Time		80	ns
t_{LZ}(1)	$\overline{CE}$ Low to Active Output	0		ns
t_{OLZ}(1)	$\overline{OE}$ Low to Active Output	0		ns
t_{HZ}(1)(7)	$\overline{CE}$ High to High-Z Output		55	ns
t_{OHZ}(1)(7)	$\overline{OE}$ High to High-Z Output		55	ns
t_{OH}(1)	Output Hold from Address Change	0		ns

Figure 1. A.C. Testing Input/Output Waveform(8)

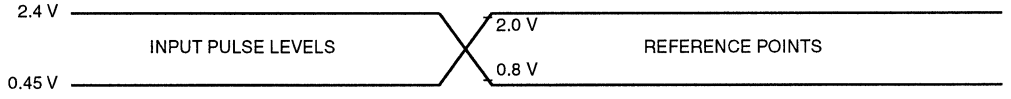


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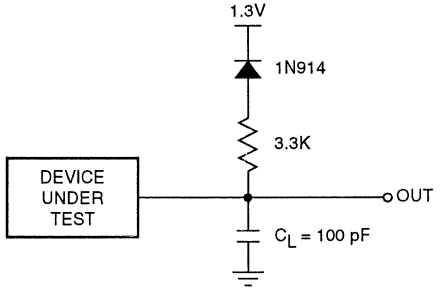
Figure 2. A.C. Testing Load Circuit (example)



C_L INCLUDES JIG CAPACITANCE

5089 FHD F04

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(7) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.
(8) Input rise and fall times (10% and 90%) < 10 ns.

A.C. CHARACTERISTICS, Write Cycle

CAT28C17A T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C17AI T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C17A-20 28C17AI-20		Units
		Min.	Max.	
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}(9)	$\overline{CE}$ Pulse Time	150		ns
t_{OES}	$\overline{OE}$ Setup Time	15		ns
t_{OEH}	$\overline{OE}$ Hold Time	15		ns
t_{WP}(9)	$\overline{WE}$ Pulse Width	150		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{DL}	Data Latch Time	50		ns
t_{INIT}(1)	Write Inhibit Period After Power-up	5	20	ms
t_{DB}	Time to Device Busy		80	ns

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(9) A write pulse of less than 20ns duration will not initiate a write cycle.

DEVICE OPERATION

Read

Data stored in the CAT28C17A/CAT28C17AI is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Ready/$\overline{BUSY}$ (RDY/$\overline{BUSY}$)

The RDY/$\overline{BUSY}$ pin is an open drain output which indicates device status during programming. It is pulled low during the write cycle and released at the end of programming. Several devices may be OR-tied to the same RDY/$\overline{BUSY}$ line.

Figure 3. Read Cycle

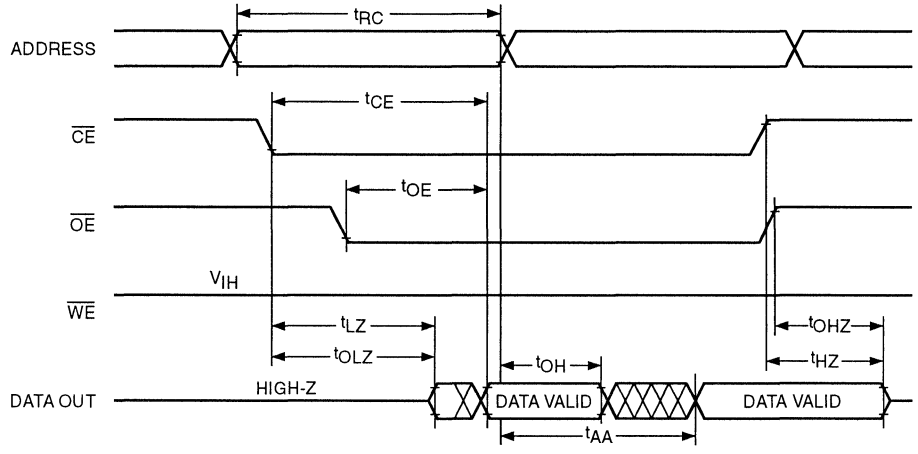
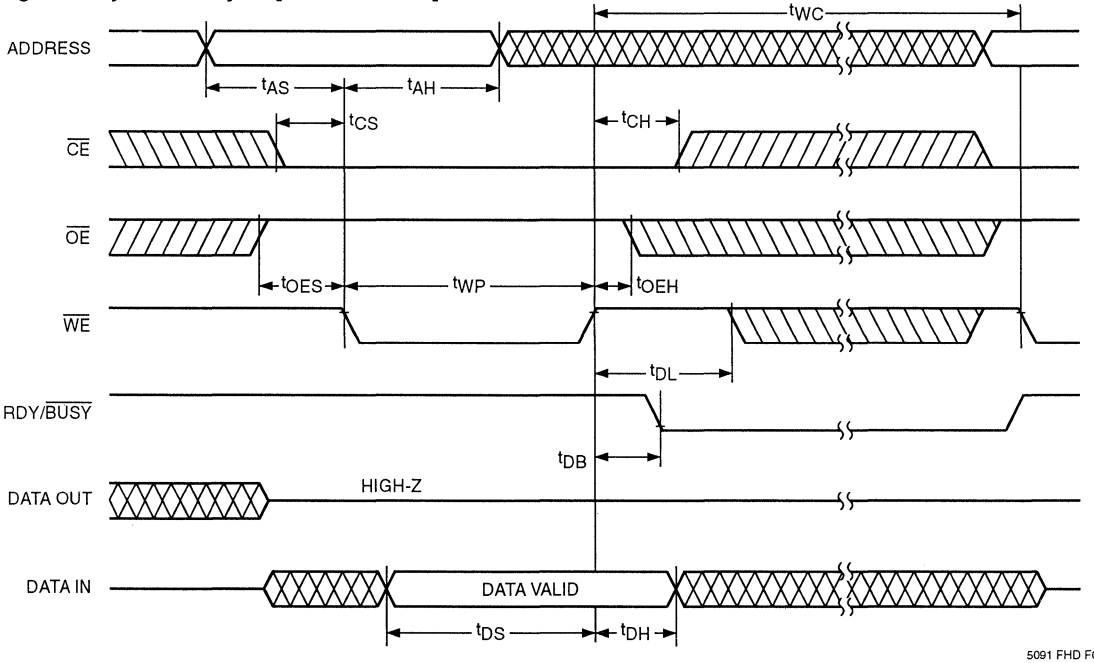


Figure 4. Byte Write Cycle [$\overline{WE}$ Controlled]



Byte Write

A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 10 ms.

$\overline{DATA}$ Polling

$\overline{DATA}$ polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0–I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle, all I/O's will output true data during a read cycle.

Figure 5. Byte Write Cycle [$\overline{CE}$ Controlled]

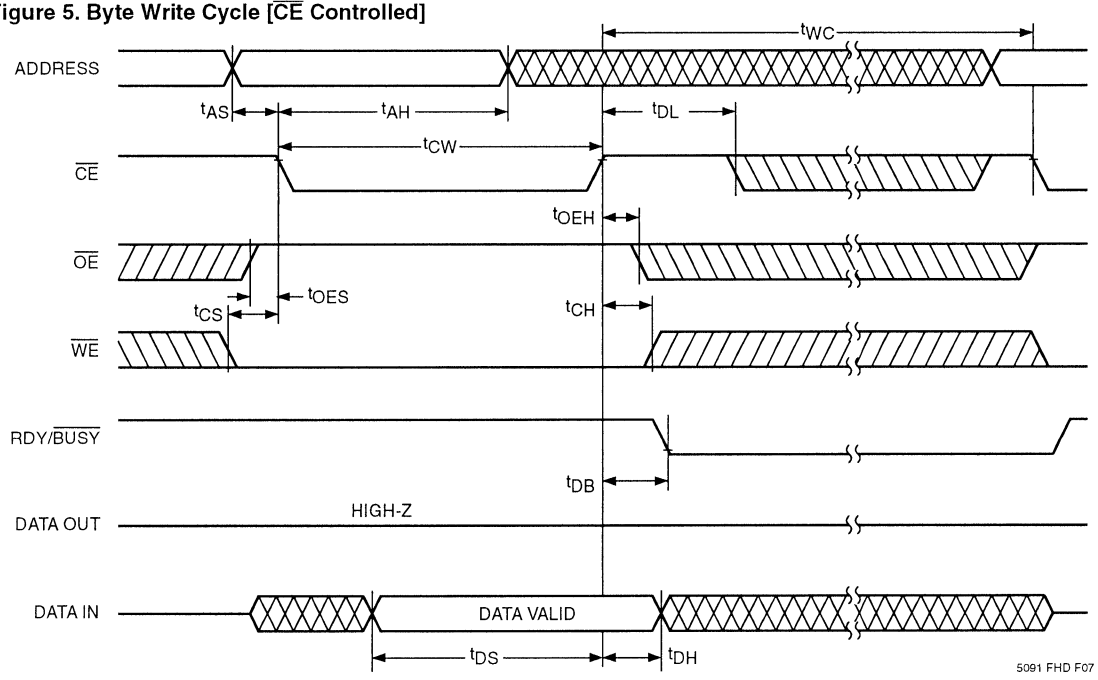
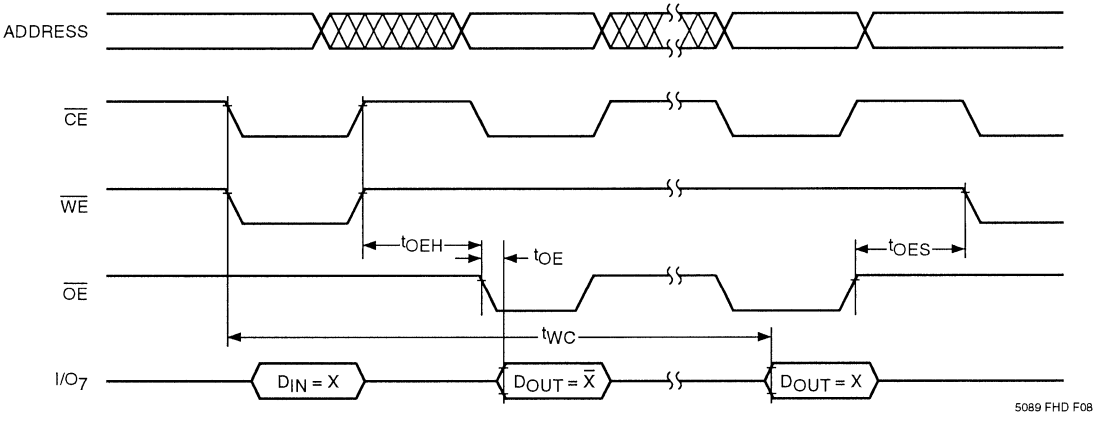


Figure 6. $\overline{DATA}$ Polling



HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28C17A/ CAT28C17AI.

(1) V_{CC} sense provides for write protection when V_{CC} falls below 3.0V min.

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 20 ms delay before a write sequence, after V_{CC} has reached 3.0V min.

(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

CAT28C64A/CAT28C64AI

64K-Bit CMOS E²PROM

FEATURES

- Fast Read Access Times: 150/200/250ns
- Low Power CMOS Dissipation:
  - –Active: 30mA Max.
  - –Standby: 100µA Max.
- Simple Write Operation:
  - –On-Chip Address and Data Latches
  - –Self-Timed Write Cycle with Auto-Clear
- Fast Nonvolatile Write Cycle:
  - –10ms Max (5ms available)
- CMOS and TTL Compatible I/O
- Automatic Page Write Operation:
  - –1 to 32 Bytes in 10ms
  - –Page Load Timer
- End of Write Detection: $\overline{\text{DATA}}$ Polling
- Hardware Write Protection
- 10,000 Program/Erase Cycles
- 10 Year Data Retention

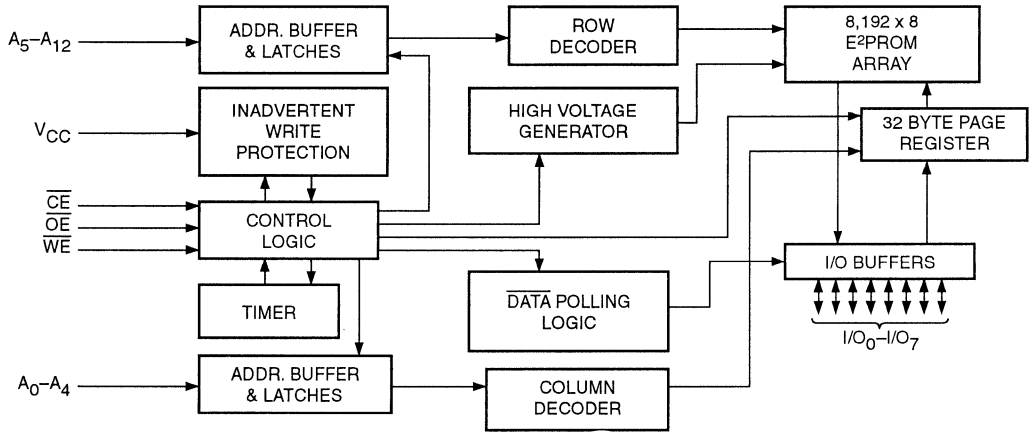
DESCRIPTION

The CAT28C64A/CAT28C64AI is a fast, low power, 5V-only CMOS E²PROM organized as 8K x 8 bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling signals the start and end of the self-timed write cycle. Additionally, the CAT28C64A/CAT28C64AI features hardware write protection.

The CAT28C64A/CAT28C64AI is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 28 pin DIP and SO or 32 pin PLCC packages.

7

BLOCK DIAGRAM

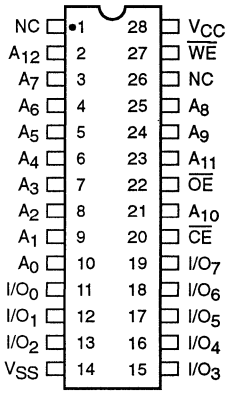


5092 FHD F02

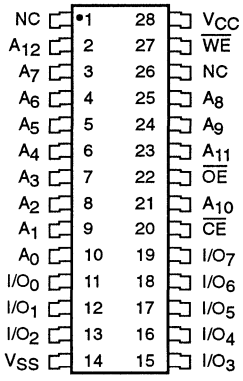
TD 5092

PIN CONFIGURATION

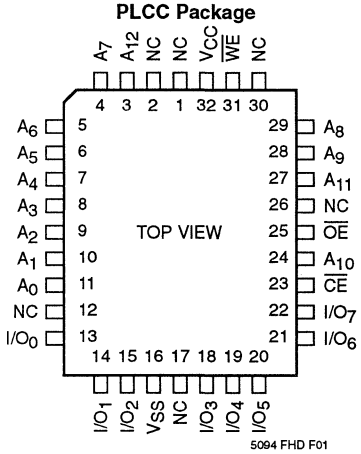
DIP Package



SO Package



PLCC Package



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PIN FUNCTIONS

Pin Name	Function
A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	5V Supply
V_{SS}	Ground
NC	No Connect

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE $T_A = 25°C$, f = 1.0 MHz, $V_{CC} = 5V$

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O} = 0V$
C_{IN}(1)	Input Capacitance	6	pF	$V_{IN} = 0V$

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with
Respect to Ground(2) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation
Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(3) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(1)	Endurance	10,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(1)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT28C64A T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C64AI T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	V_{CC} Current (Operating, TTL)			40	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 1/t_{RC} min, All I/O's Open
I_{CCC}(5)	V_{CC} Current (Operating, CMOS)			30	mA	$\overline{CE}$ = $\overline{OE}$ = V_{ILC}, f = 1/t_{RC} min, All I/O's Open
I_{SB}	V_{CC} Current (Standby, TTL)			1	mA	$\overline{CE}$ = V_{IH}, All I/O's Open
I_{SBC}(6)	V_{CC} Current (Standby, CMOS)			100	µA	$\overline{CE}$ = V_{IHC}, All I/O's Open
I_{LI}	Input Leakage Current	–1		1	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	–10		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IH}(6)	High Level Input Voltage	2.0		V_{CC} +0.3	V	
V_{IL}(5)	Low Level Input Voltage	–0.3		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1mA
V_{WI}	Write Inhibit Voltage	3.0			V	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} +1V.
(5) V_{ILC} = –0.3V to +0.3V.
(6) V_{IHC} = V_{CC} –0.3V to V_{CC} +0.3V.

A.C. CHARACTERISTICS, Read Cycle

CAT28C64A T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C64AI T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C64A-15 28C64AI-15		28C64A-20 28C64AI-20		28C64A-25 28C64AI-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	150		200		250		ns
t_{CE}	$\overline{CE}$ Access Time		150		200		250	ns
t_{AA}	Address Access Time		150		200		250	ns
t_{OE}	$\overline{OE}$ Access Time		70		90		90	ns
t_{LZ}(1)	$\overline{CE}$ Low to Active Output	10		10		10		ns
t_{OLZ}(1)	$\overline{OE}$ Low to Active Output	10		10		10		ns
t_{HZ}(1)(7)	$\overline{CE}$ High to High-Z Output		70		90		90	ns
t_{OHZ}(1)(7)	$\overline{OE}$ High to High-Z Output		70		90		90	ns
t_{OH}(1)	Output Hold from Address Change	20		20		20		ns

Figure 1. A.C. Testing Input/Output Waveform(8)

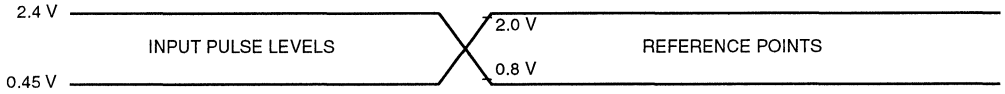

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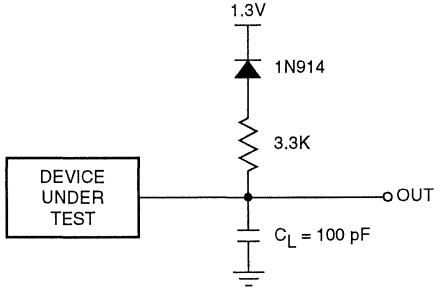
Figure 2. A.C. Testing Load Circuit (example)



C_L INCLUDES JIG CAPACITANCE

5096 FHD F04

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(7) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.
(8) Input rise and fall times (10% and 90%) < 10 ns.

A.C. CHARACTERISTICS, Write Cycle

CAT28C64A T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C64AI T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C64A-15 28C64AI-15		28C64A-20 28C64AI-20		28C64A-25 28C64AI-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		10		10		10	ms
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	100		120		100		ns
t_{CS}	Write Setup Time	0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		ns
t_{CW}(9)	$\overline{CE}$ Pulse Time	150		150		150		ns
t_{OES}	$\overline{OE}$ Setup Time	10		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		10		ns
t_{WP}(9)	$\overline{WE}$ Pulse Width	150		150		150		ns
t_{DS}	Data Setup Time	70		70		70		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{INIT}(1)	Write Inhibit Period After Power-up	5	20	5	20	5	20	ms
t_{BLC}(1)(10)	Byte Load Cycle Time	10	100	10	100	10	100	µs

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(9) A write pulse of less than 20ns duration will not initiate a write cycle.
(10) A timer of duration t_{BLC} max. begins with every LOW to HIGH transition of $\overline{WE}$. If allowed to time out, a page or byte write will begin; however a transition from HIGH to LOW within t_{BLC} max. stops the timer.

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DEVICE OPERATION

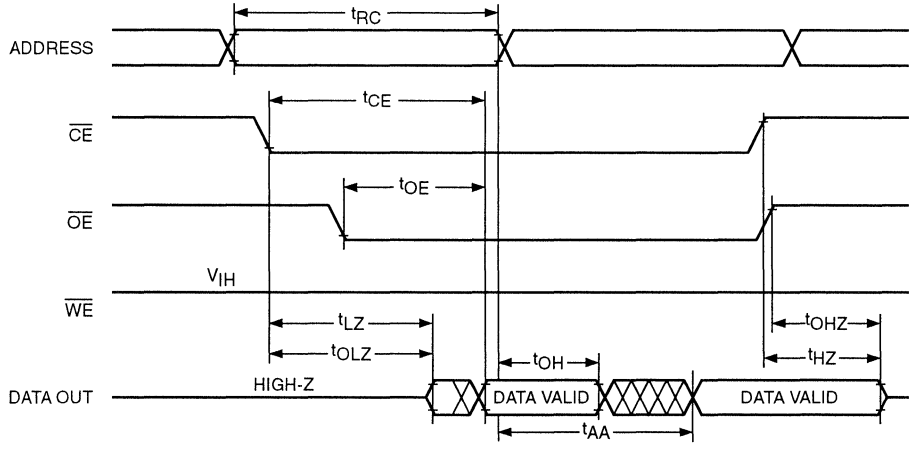
Read

Data stored in the CAT28C64A/CAT28C64AI is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Byte Write

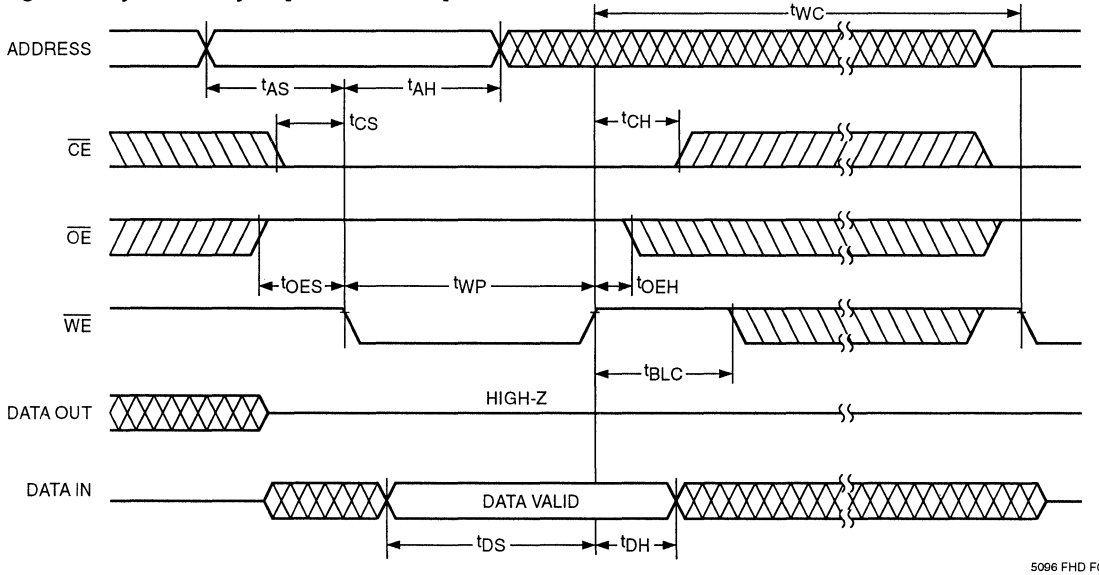
A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 10 ms.

Figure 3. Read Cycle



5096 FHD F05

Figure 4. Byte Write Cycle [$\overline{WE}$ Controlled]



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Page Write

The page write mode of the CAT28C64A/CAT28C64AI (essentially an extended BYTE WRITE mode) allows from 1 to 32 bytes of data to be programmed within a single E^2PROM write cycle. This effectively reduces the byte-write time by a factor of 32.

Following an initial WRITE operation ($\overline{WE}$ pulsed low, for t_{WP}, and then high) the page write mode can begin by issuing sequential $\overline{WE}$ pulses, which load the address and data bytes into a 32 byte temporary buffer. The page address where data is to be written, specified by bits A_5 to A_{12}, is latched on the last falling edge of $\overline{WE}$. Each byte within the page is defined by address bits A_0 to A_4 (which can be loaded in any order) during the first and subsequent write cycles. Each successive byte load cycle must begin within $t_{BLC\ MIN}$ of the rising edge of the preceding $\overline{WE}$ pulse. There is no page write window limitation as long as $\overline{WE}$ is pulsed low within $t_{BLC\ MIN}$.

Upon completion of the page write sequence, $\overline{WE}$ must stay high a minimum of $t_{BLC\ MAX}$ for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

Figure 5. Byte Write Cycle [$\overline{CE}$ Controlled]

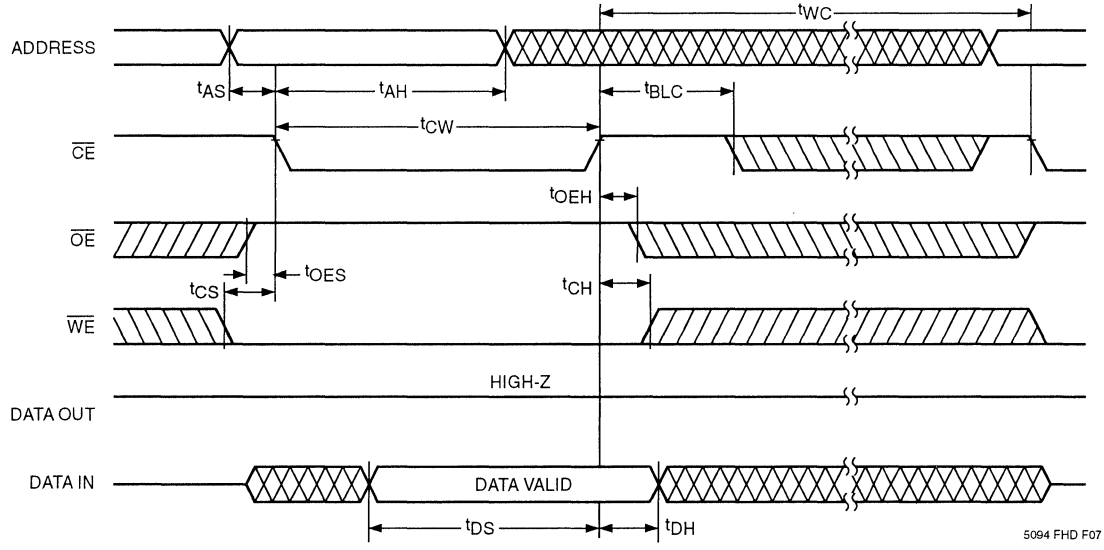
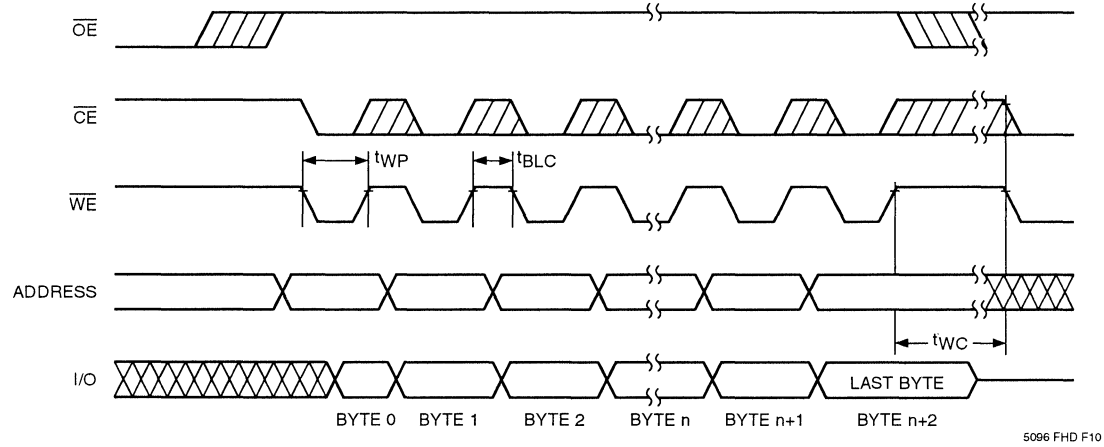


Figure 6. Page Mode Write Cycle



$\overline{\text{DATA}}$ Polling

$\overline{\text{DATA}}$ polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0–I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle, all I/O's will output true data during a read cycle.

HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28C64A/ CAT28C64AI.

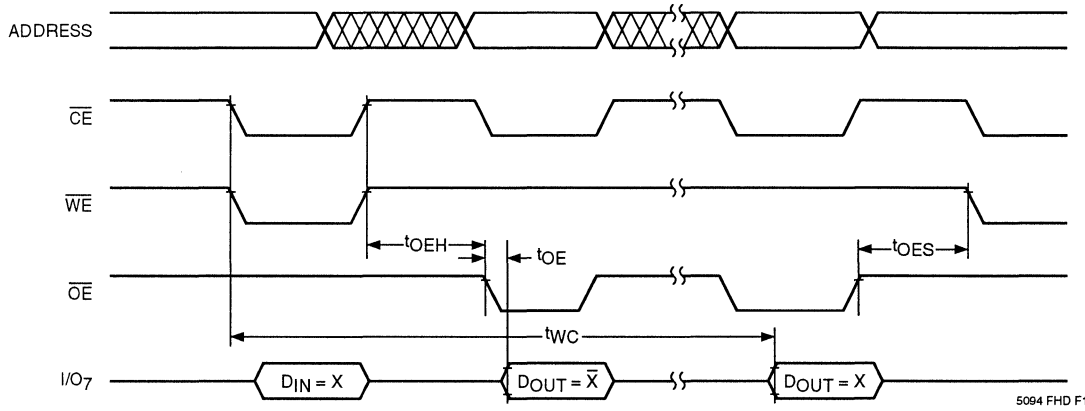
(1) V_{CC} sense provides for write protection when V_{CC} falls below 3.0V min.

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 20 ms delay before a write sequence, after V_{CC} has reached 3.0V min.

(3) Write inhibit is activated by holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not result in a write cycle.

Figure 7. $\overline{\text{DATA}}$ Polling



CAT28C65A/CAT28C65AI

64K-Bit CMOS E²PROM

FEATURES

- Fast Read Access Times: 150/200/250ns
- Low Power CMOS Dissipation:
  - –Active: 30mA Max.
  - –Standby: 100μA Max.
- Simple Write Operation:
  - –On-Chip Address and Data Latches
  - –Self-Timed Write Cycle with Auto-Clear
- Fast Nonvolatile Write Cycle:
  - –10ms Max (5ms available)
- CMOS and TTL Compatible I/O
- Automatic Page Write Operation:
  - –1 to 32 Bytes in 10ms
  - –Page Load Timer
- End of Write Detection:
  - –$\overline{\text{DATA}}$ Polling
  - –RDY/$\overline{\text{BUSY}}$ Pin
- Hardware Write Protection
- 10,000 Program/Erase Cycles
- 10 Year Data Retention

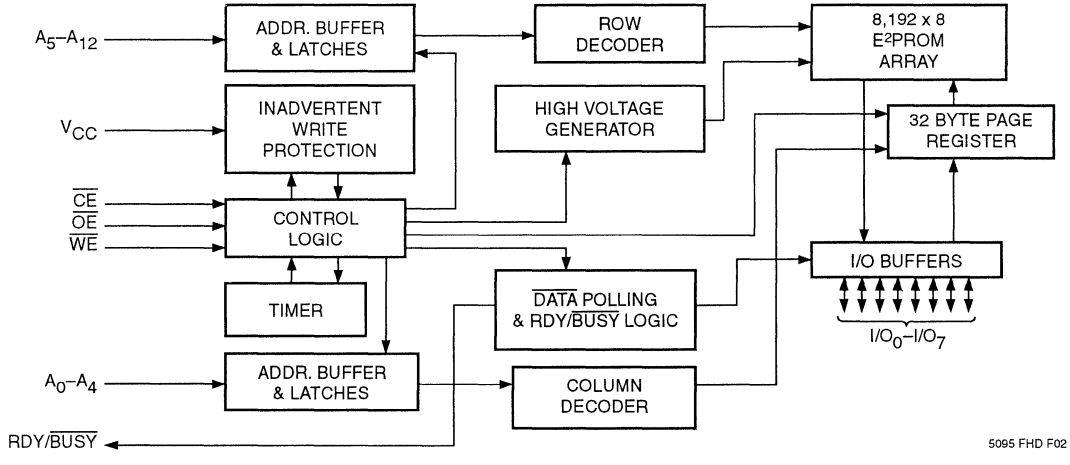
DESCRIPTION

The CAT28C65A/CAT28C65AI is a fast, low power, 5V-only CMOS E²PROM organized as 8K x 8 bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling and a RDY/$\overline{\text{BUSY}}$ pin signal the start and end of the self-timed write cycle. Additionally, the CAT28C65A/CAT28C65AI features hardware write protection.

The CAT28C65A/CAT28C65AI is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 28 pin DIP and SO or 32 pin PLCC packages.

7

BLOCK DIAGRAM

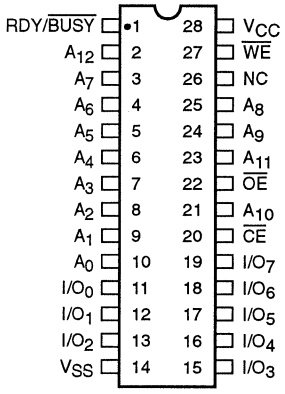


5095 FHD F02

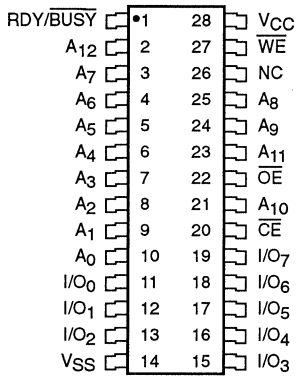
TD 5095

PIN CONFIGURATION

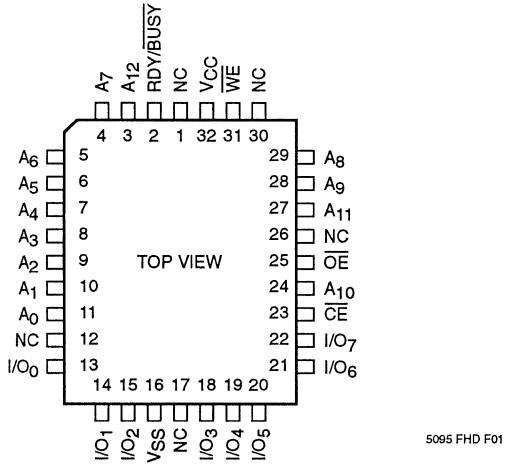
DIP Package



SO Package



PLCC Package



5095 FHD F01

PIN FUNCTIONS

Pin Name	Function
A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
RDY/$\overline{BUSY}$	Ready/$\overline{BUSY}$ Status
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	5V Supply
V_{SS}	Ground
NC	No Connect

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

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Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with
Respect to Ground(2) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation
Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(3) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

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T_{DR}(1)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(4)	Latch-Up	100		mA	JEDEC Standard 17

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CAT28C65AI T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

		Limits				
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{CC}	V_{CC} Current (Operating, TTL)			40	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 1/t_{RC} min, All I/O's Open
I_{CCC}(5)	V_{CC} Current (Operating, CMOS)			30	mA	$\overline{CE}$ = $\overline{OE}$ = V_{ILC}, f = 1/t_{RC} min, All I/O's Open
I_{SB}	V_{CC} Current (Standby, TTL)			1	mA	$\overline{CE}$ = V_{IH}, All I/O's Open
I_{SBC}(6)	V_{CC} Current (Standby, CMOS)			100	µA	$\overline{CE}$ = V_{IHC}, All I/O's Open
I_{LI}	Input Leakage Current	–1		1	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	–10		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IH}(6)	High Level Input Voltage	2.0		V_{CC} +0.3	V	
V_{IL}(5)	Low Level Input Voltage	–0.3		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1mA
V_{WI}	Write Inhibit Voltage	3.0			V	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} +1V.
(5) V_{ILC} = –0.3V to +0.3V.
(6) V_{IHC} = V_{CC} –0.3V to V_{CC} +0.3V.

A.C. CHARACTERISTICS, Read Cycle

CAT28C65A T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C65AI T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C65A-15 28C65AI-15		28C65A-20 28C65AI-20		28C65A-25 28C65AI-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	150		200		250		ns
t_{CE}	$\overline{CE}$ Access Time		150		200		250	ns
t_{AA}	Address Access Time		150		200		250	ns
t_{OE}	$\overline{OE}$ Access Time		70		90		90	ns
t_{LZ}(1)	$\overline{CE}$ Low to Active Output	10		10		10		ns
t_{OLZ}(1)	$\overline{OE}$ Low to Active Output	10		10		10		ns
t_{HZ}(1)(7)	$\overline{CE}$ High to High-Z Output		70		90		90	ns
t_{OHZ}(1)(7)	$\overline{OE}$ High to High-Z Output		70		90		90	ns
t_{OH}(1)	Output Hold from Address Change	20		20		20		ns

Figure 1. A.C. Testing Input/Output Waveform(8)

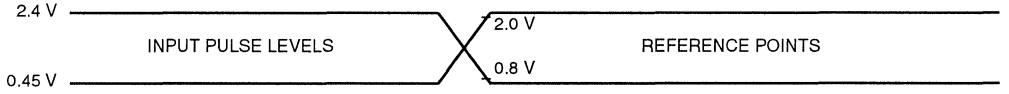

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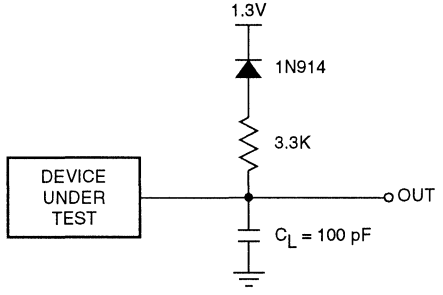
Figure 2. A.C. Testing Load Circuit (example)



C_L INCLUDES JIG CAPACITANCE

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Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(7) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.
(8) Input rise and fall times (10% and 90%) < 10 ns.

A.C. CHARACTERISTICS, Write Cycle

CAT28C65A T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C65AI T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

		28C65A-15 28C65AI-15		28C65A-20 28C65AI-20		28C65A-25 28C65AI-25		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{WC}	Write Cycle Time		10		10		10	ms
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	100		120		100		ns
t_{CS}	Write Setup Time	0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		ns
t_{CW}(9)	$\overline{CE}$ Pulse Time	150		150		150		ns
t_{OES}	$\overline{OE}$ Setup Time	10		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		10		ns
t_{WP}(9)	$\overline{WE}$ Pulse Width	150		150		150		ns
t_{DS}	Data Setup Time	70		70		70		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{INIT}(1)	Write Inhibit Period After Power-up	5	20	5	20	5	20	ms
t_{BLC}(1)(10)	Byte Load Cycle Time	10	100	10	100	10	100	µs
t_{DB}	Time to Device Busy		120		120		120	ns

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(9) A write pulse of less than 20ns duration will not initiate a write cycle.
(10) A timer of duration t_{BLC} max. begins with every LOW to HIGH transition of $\overline{WE}$. If allowed to time out, a page or byte write will begin; however a transition from HIGH to LOW within t_{BLC} max. stops the timer.

DEVICE OPERATION

Read

Data stored in the CAT28C65A/CAT28C65AI is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Byte Write

A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the

Figure 3. Read Cycle

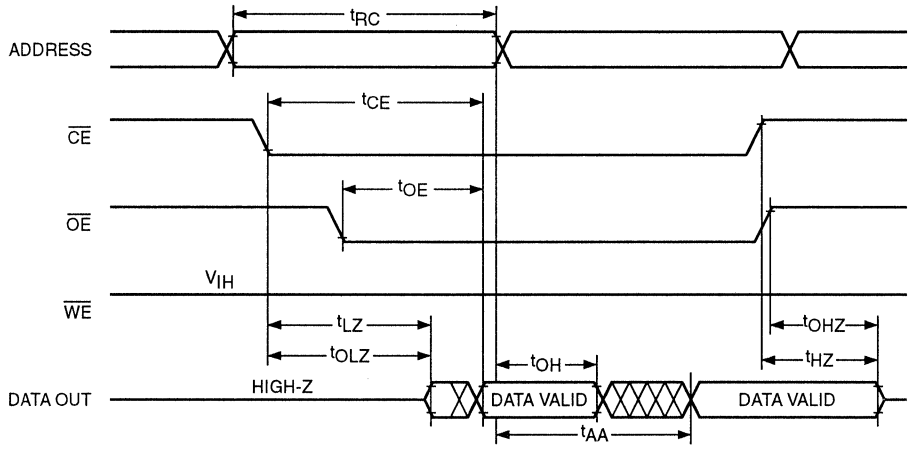

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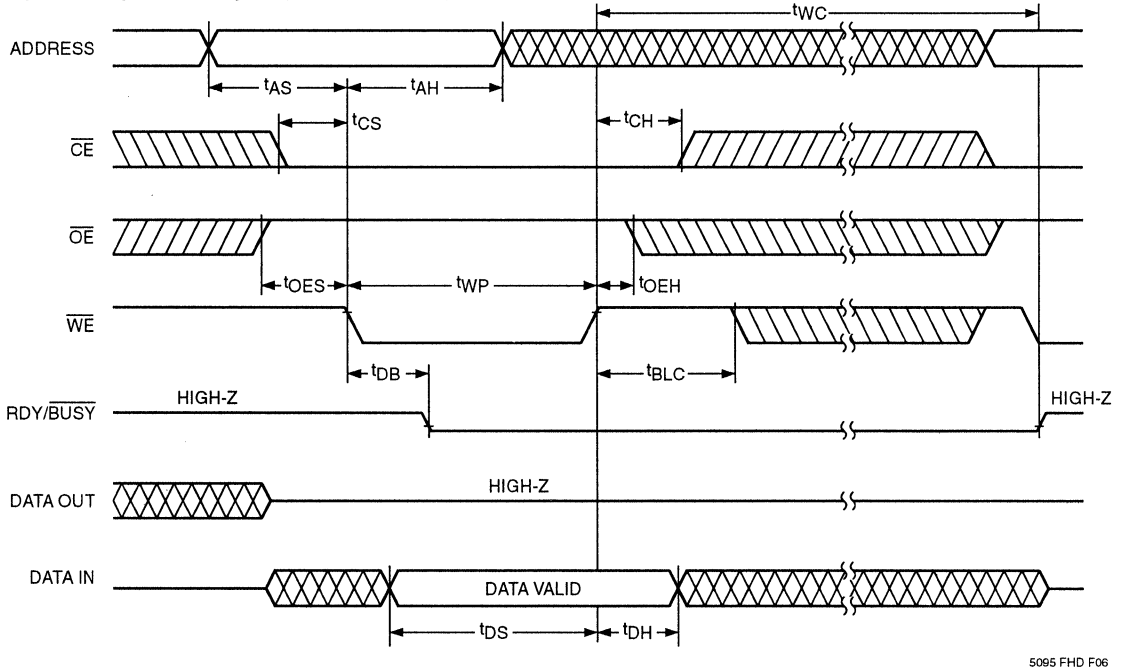
Figure 4. Byte Write Cycle [$\overline{WE}$ Controlled]



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falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 10 ms.

Page Write

The page write mode of the CAT28C65A/CAT28C65AI (essentially an extended BYTE WRITE mode) allows from 1 to 32 bytes of data to be programmed within a single E^2PROM write cycle. This effectively reduces the byte-write time by a factor of 32.

Following an initial WRITE operation ($\overline{WE}$ pulsed low, for t_{WP}, and then high) the page write mode can begin by issuing sequential $\overline{WE}$ pulses, which load the address and data bytes into a 32 byte temporary buffer. The page address where data is to be written, specified by bits A_5 to A_{12}, is latched on the last falling edge of $\overline{WE}$. Each byte within the page is defined by address bits A_0 to A_4

Figure 5. Byte Write Cycle [$\overline{CE}$ Controlled]

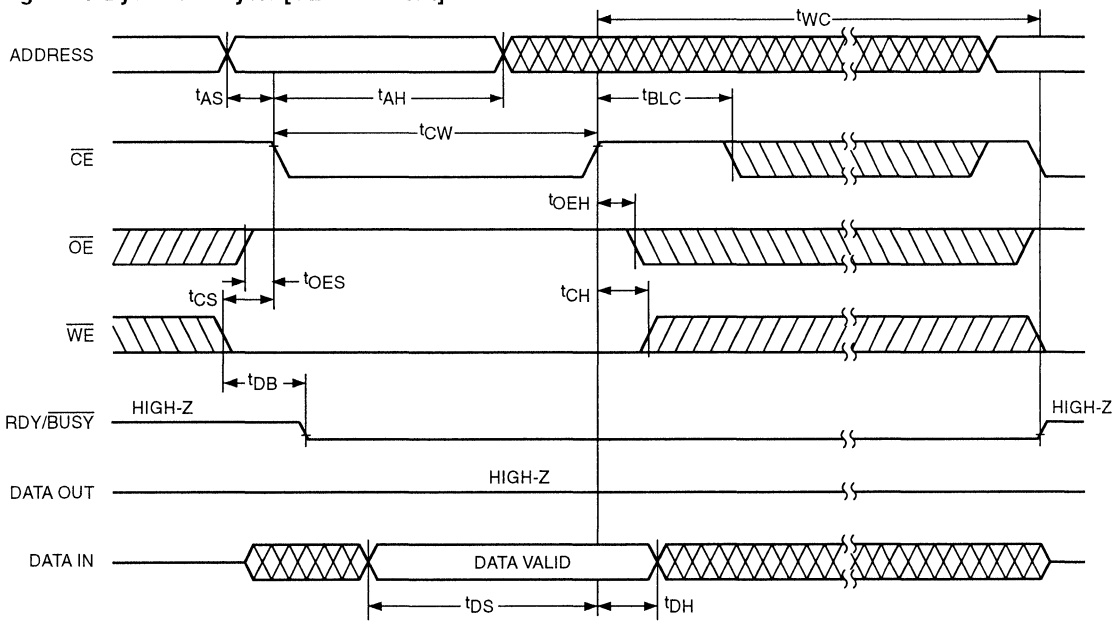
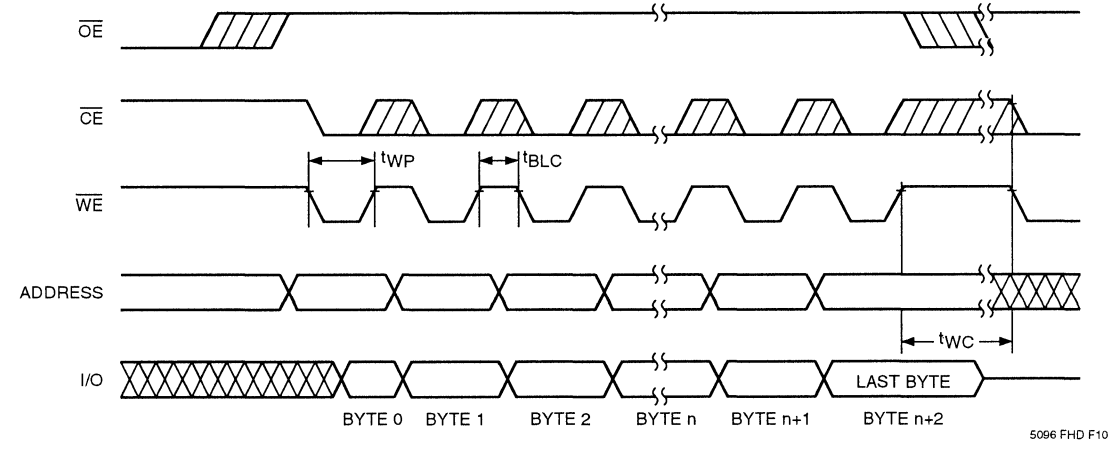


Figure 6. Page Mode Write Cycle



(which can be loaded in any order) during the first and subsequent write cycles. Each successive byte load cycle must begin within $t_{BLC\ MIN}$ of the rising edge of the preceding $\overline{WE}$ pulse. There is no page write window limitation as long as $\overline{WE}$ is pulsed low within $t_{BLC\ MIN}$.

Upon completion of the page write sequence, $\overline{WE}$ must stay high a minimum of $t_{BLC\ MAX}$ for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

$\overline{DATA}$ Polling

$\overline{DATA}$ polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0–I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle, all I/O's will output true data during a read cycle.

Ready/$\overline{BUSY}$ (RDY/$\overline{BUSY}$)

The RDY/$\overline{BUSY}$ pin is an open drain output which indicates device status during programming. It is pulled low during the write cycle and released at the end of programming. Several devices may be OR-tied to the same RDY/$\overline{BUSY}$ line.

HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28C65A/CAT28C65AI.

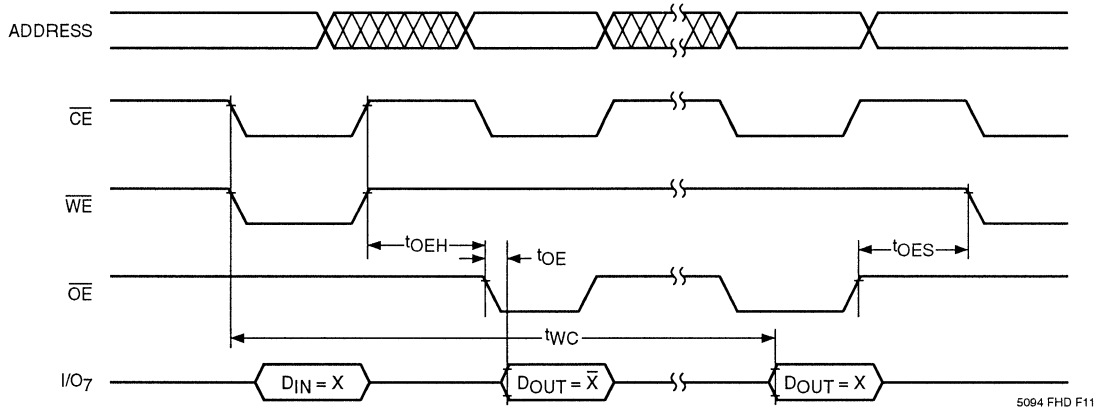
(1) V_{CC} sense provides for write protection when V_{CC} falls below 3.0V min.

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 20 ms delay before a write sequence, after V_{CC} has reached 3.0V min.

(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

Figure 7. $\overline{DATA}$ Polling



CAT28C64B/CAT28C64BI

64K-Bit CMOS E²PROM

FEATURES

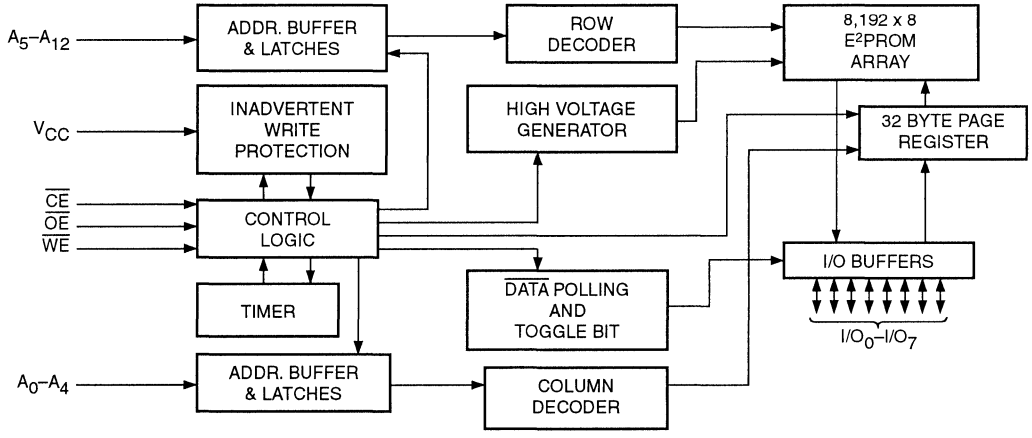
- **Fast Read Access Times:**
  –120/150/200ns (Commercial)
  –150/200ns (Industrial)
- **Low Power CMOS Dissipation:**
  –Active: 25mA Max.
  –Standby: 100μA Max.
- **Simple Write Operation:**
  –On-Chip Address and Data Latches
  –Self-Timed Write Cycle with Auto-Clear
- **Fast Nonvolatile Write Cycle:**
  –5ms Max (3ms available)
- **CMOS and TTL Compatible I/O**
- **Automatic Page Write Operation:**
  –1 to 32 Bytes in 5ms
  –Page Load Timer
- **End of Write Detection:**
  –Toggle Bit
  –$\overline{\text{DATA}}$ Polling
- **Hardware and Software Write Protection**
- **10,000 Program/Erase Cycles**
- **100 Year Data Retention**
- **Optional High Endurance Device Available**

DESCRIPTION

The CAT28C64B/CAT28C64BI is a fast, low power, 5V-only CMOS E²PROM organized as 8K x 8 bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling and Toggle status bits signal the start and end of the self-timed write cycle. Additionally, the CAT28C64B/CAT28C64BI features hardware and software write protection.

The CAT28C64B/CAT28C64BI is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 100 years. The device is available in JEDEC approved 28 pin DIP and SO or 32 pin PLCC and TSOP packages.

BLOCK DIAGRAM



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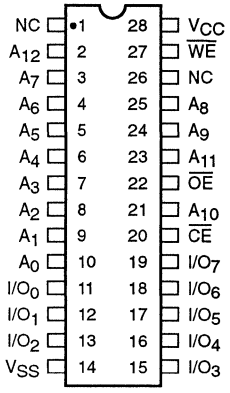
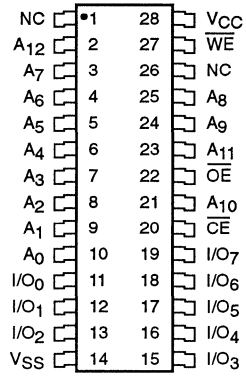
TD 5094

PIN CONFIGURATION

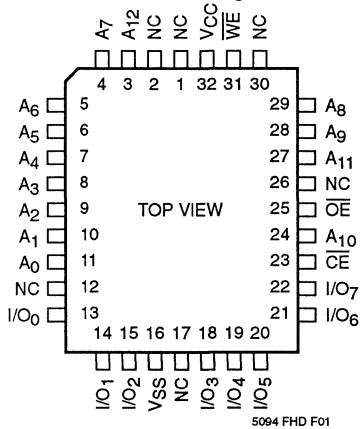
DIP Package



SO Package



PLCC Package



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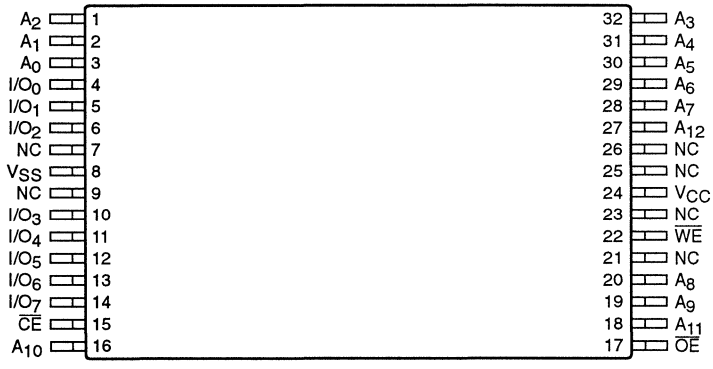
TSOP Package



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PIN FUNCTIONS

Pin Name	Function
A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	5V Supply
V_{SS}	Ground
NC	No Connect

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with
Respect to Ground[2] .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation
Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current[3] ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}[1]	Endurance	10,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}[1]	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}[1]	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}[1][4]	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT28C64B T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C64BI T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

		Limits				
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{CC}	V_{CC} Current (Operating, TTL)			30	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 1/t_{RC} min, All I/O's Open
I_{CCC}[5]	V_{CC} Current (Operating, CMOS)			25	mA	$\overline{CE}$ = $\overline{OE}$ = V_{ILC}, f = 1/t_{RC} min, All I/O's Open
I_{SB}	V_{CC} Current (Standby, TTL)			1	mA	$\overline{CE}$ = V_{IH}, All I/O's Open
I_{SBC}[6]	V_{CC} Current (Standby, CMOS)			100	µA	$\overline{CE}$ = V_{IHC}, All I/O's Open
I_{LI}	Input Leakage Current	–1		1	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	–10		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IH}[6]	High Level Input Voltage	2.0		V_{CC} +0.3	V	
V_{IL}[5]	Low Level Input Voltage	–0.3		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1mA
V_{WI}	Write Inhibit Voltage	3.5			V	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} +1V.
(5) V_{ILC} = –0.3V to +0.3V.
(6) V_{IHC} = V_{CC} –0.3V to V_{CC} +0.3V.

A.C. CHARACTERISTICS, Read Cycle

CAT28C64B T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C64BI T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C64B-12		28C64B-15 28C64BI-15		28C64B-20 28C64BI-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	120		150		200		ns
t_{CE}	$\overline{CE}$ Access Time		120		150		200	ns
t_{AA}	Address Access Time		120		150		200	ns
t_{OE}	$\overline{OE}$ Access Time		60		70		80	ns
t_{LZ}(1)	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ}(1)	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ}(1)(7)	$\overline{CE}$ High to High-Z Output		50		50		55	ns
t_{OHZ}(1)(7)	$\overline{OE}$ High to High-Z Output		50		50		55	ns
t_{OH}(1)	Output Hold from Address Change	0		0		0		ns

Figure 1. A.C. Testing Input/Output Waveform(8)

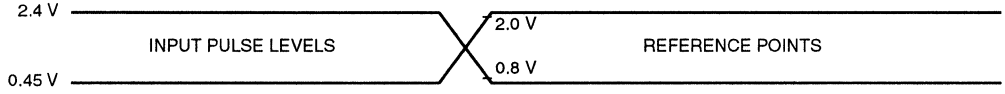

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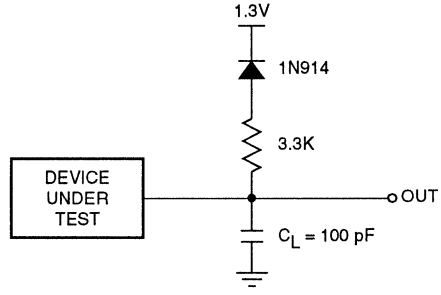
Figure 2. A.C. Testing Load Circuit (example)



C_L INCLUDES JIG CAPACITANCE

5096 FHD F04

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(7) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.
(8) Input rise and fall times (10% and 90%) < 10 ns.

A.C. CHARACTERISTICS, Write Cycle

CAT28C64B T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C64BI T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C64B-12		28C64B-15 28C64BI-15		28C64B-20 28C64BI-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		5		5		5	ms
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	100		100		120		ns
t_{CS}	Write Setup Time	0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		ns
t_{CW}(9)	$\overline{CE}$ Pulse Time	150		150		150		ns
t_{OES}	$\overline{OE}$ Setup Time	10		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		10		ns
t_{WP}(9)	$\overline{WE}$ Pulse Width	150		150		150		ns
t_{DS}	Data Setup Time	70		70		70		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{INIT}(1)	Write Inhibit Period After Power-up	5	10	5	10	5	10	ms
t_{BLC}(1)(10)	Byte Load Cycle Time	.05	100	.05	100	.05	100	µs

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(9) A write pulse of less than 20ns duration will not initiate a write cycle.
(10) A timer of duration t_{BLC} max. begins with every LOW to HIGH transition of $\overline{WE}$. If allowed to time out, a page or byte write will begin; however a transition from HIGH to LOW within t_{BLC} max. stops the timer.

DEVICE OPERATION

Read

Data stored in the CAT28C64B/CAT28C64BI is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Byte Write

A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 5 ms.

Figure 3. Read Cycle

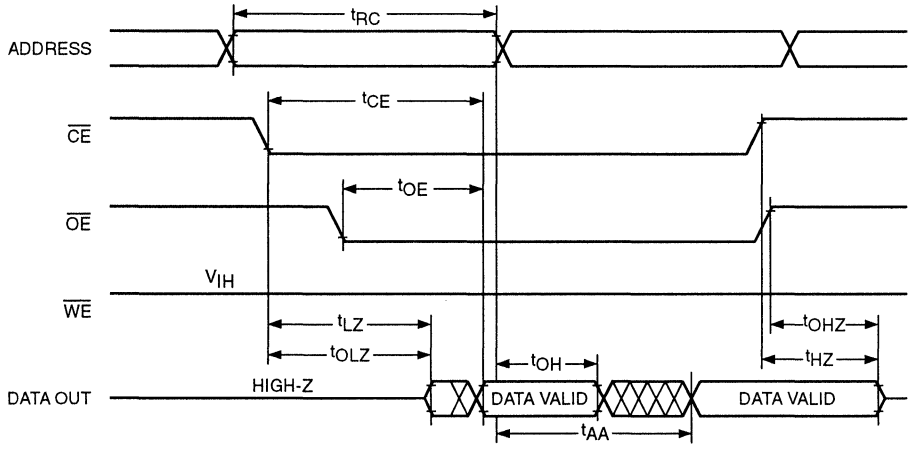


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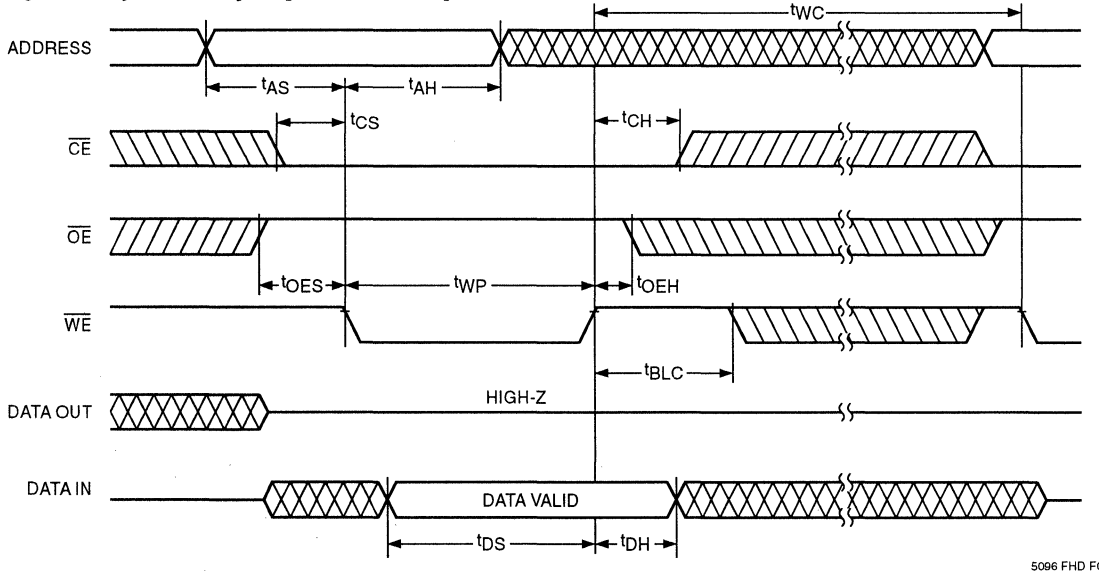
Figure 4. Byte Write Cycle [$\overline{WE}$ Controlled]



5096 FHD F06

Page Write

The page write mode of the CAT28C64B/CAT28C64BI (essentially an extended BYTE WRITE mode) allows from 1 to 32 bytes of data to be programmed within a single E^2PROM write cycle. This effectively reduces the byte-write time by a factor of 32.

Following an initial WRITE operation ($\overline{WE}$ pulsed low, for t_{WP}, and then high) the page write mode can begin by issuing sequential $\overline{WE}$ pulses, which load the address and data bytes into a 32 byte temporary buffer. The page address where data is to be written, specified by bits A_5 to A_{12}, is latched on the last falling edge of $\overline{WE}$. Each byte within the page is defined by address bits A_0 to A_4 (which can be loaded in any order) during the first and subsequent write cycles. Each successive byte load cycle must begin within $t_{BLC\ MAX}$ of the rising edge of the preceding $\overline{WE}$ pulse. There is no page write window limitation as long as $\overline{WE}$ is pulsed low within $t_{BLC\ MAX}$.

Upon completion of the page write sequence, $\overline{WE}$ must stay high a minimum of $t_{BLC\ MAX}$ for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

Figure 5. Byte Write Cycle [$\overline{CE}$ Controlled]

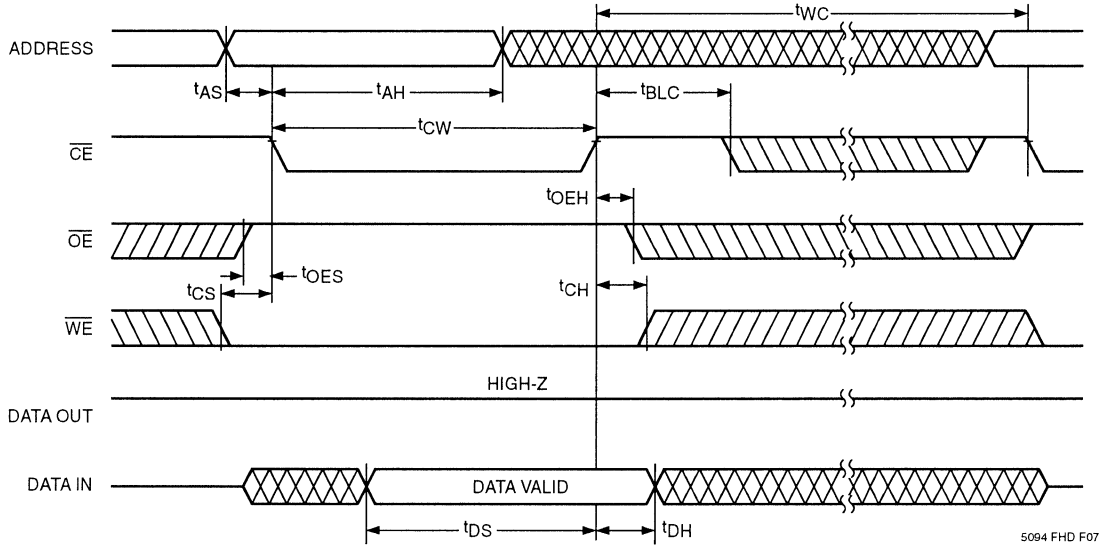
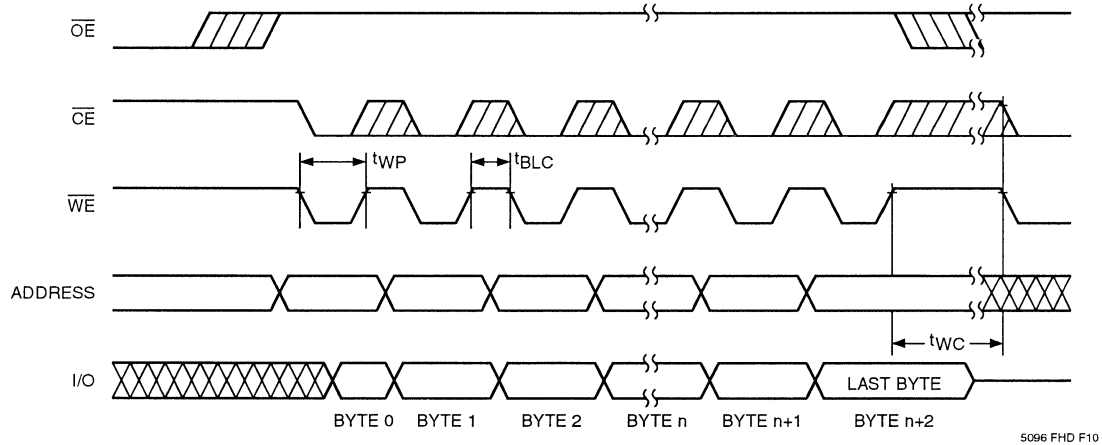


Figure 6. Page Mode Write Cycle



$\overline{\text{DATA}}$ Polling

$\overline{\text{DATA}}$ polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0–I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle, all I/O's will output true data during a read cycle.

Toggle Bit

In addition to the $\overline{\text{DATA}}$ Polling feature of the CAT28C64B/CAT28C64BI, the device offers an additional method for determining the completion of a write cycle. While a write cycle is in progress, reading data from the device will result in I/O_6 toggling between one and zero. However, once the write is complete, I/O_6 stops toggling and valid data can be read from the device.

Figure 7. $\overline{\text{DATA}}$ Polling

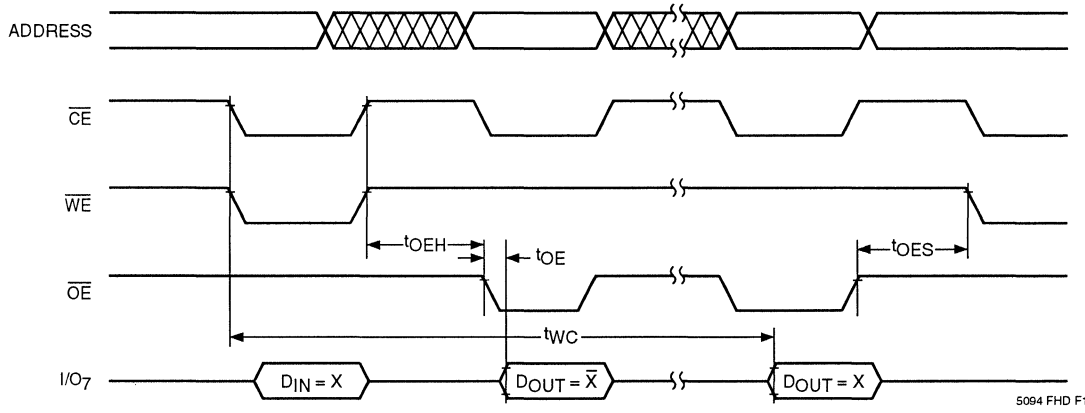
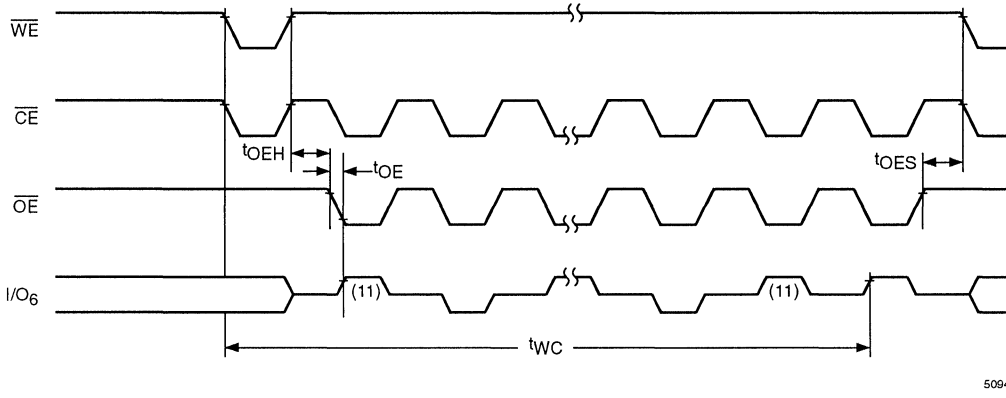


Figure 8. Toggle Bit



Note:
(11) Beginning and ending state of I/O_6 is indeterminate.

HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28C64B/ CAT28C64BI.

(1) V_{CC} sense provides for write protection when V_{CC} falls below 3.5V min.

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 10 ms delay before a write sequence, after V_{CC} has reached 3.5V min.

(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

SOFTWARE DATA PROTECTION

The CAT28C64B/CAT28C64BI features a software controlled data protection scheme which, once enabled, requires a data algorithm to be issued to the device before a write can be performed. The device is shipped from Catalyst with the software protection NOT ENABLED (the CAT28C64B/CAT28C64BI is in the standard operating mode).

Figure 9. Write Sequence for Activating Software Data Protection

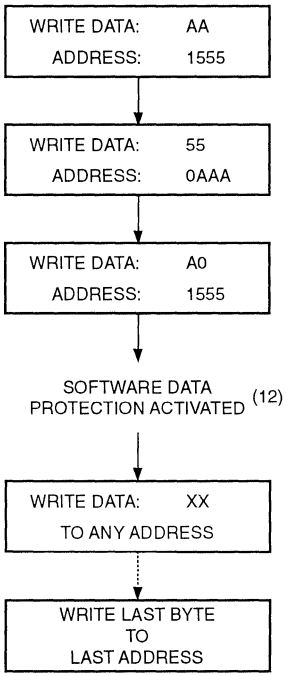


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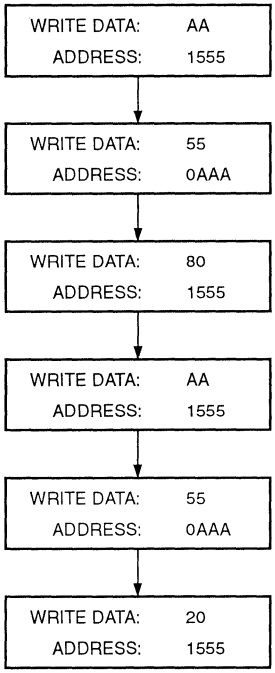
Figure 10. Write Sequence for Deactivating Software Data Protection



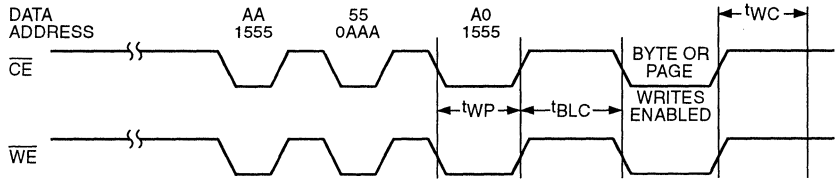
5094 FHD F09

Note:
(12) Write protection is activated at this point whether or not any more writes are completed. Writing to addresses must occur within t_{BLC} Max., after SDP activation.

To activate the software data protection, the device must be sent three write commands to specific addresses with specific data (Figure 9). This sequence of commands (along with subsequent writes) must adhere to the page write timing specifications (Figure 11). Once this is done, all subsequent byte or page writes to the device must be preceded by this same set of write commands. The data protection mechanism is activated until a deactivate sequence is issued regardless of power on/off transitions. This gives the user added inadvertent write protection on power-up in addition to the hardware protection provided.

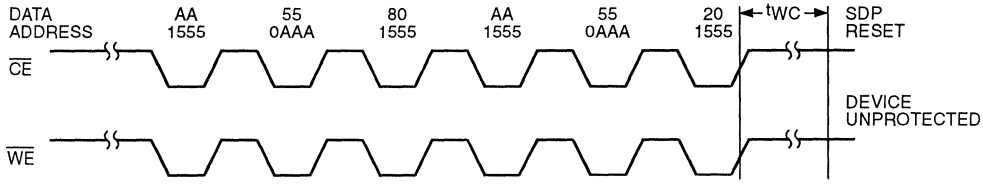
To allow the user the ability to program the device with an E^2PROM programmer (or for testing purposes) there is a software command sequence for deactivating the data protection. The six step algorithm (Figure 10) will reset the internal protection circuitry, and the device will return to standard operating mode (Figure 12 provides reset timing). After the sixth byte of this reset sequence has been issued, standard byte or page writing can commence.

Figure 11. Software Data Protection Timing



5094 FHD F13

Figure 12. Resetting Software Data Protection Timing



5094 FHD F14

CAT28C65B/CAT28C65BI

64K-Bit CMOS E²PROM

FEATURES

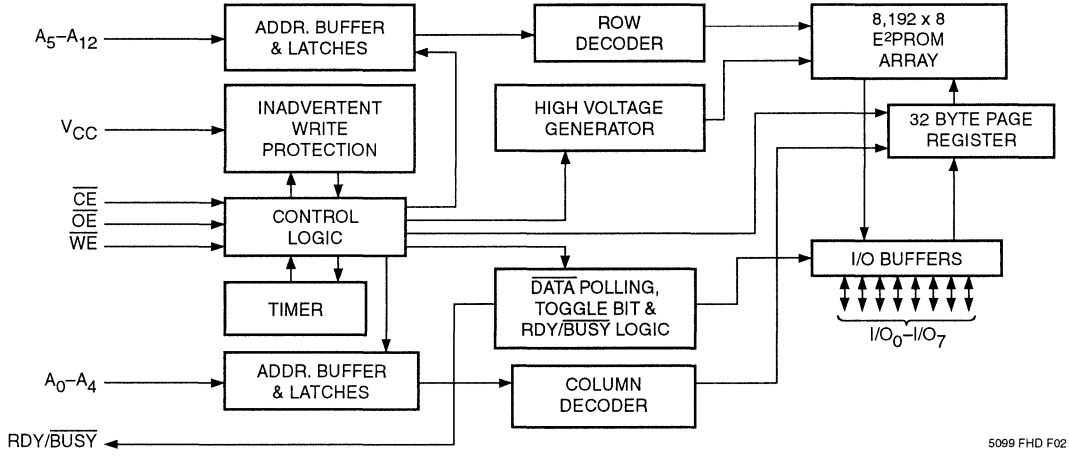
- **Fast Read Access Times:**
  - **–120/150/200ns (Commercial)**
  - **–150/200ns (Industrial)**
- **Low Power CMOS Dissipation:**
  - **–Active: 25mA Max.**
  - **–Standby: 100µA Max.**
- **Simple Write Operation:**
  - **–On-Chip Address and Data Latches**
  - **–Self-Timed Write Cycle with Auto-Clear**
- **Fast Nonvolatile Write Cycle:**
  - **–5ms Max (3ms available)**
- **CMOS and TTL Compatible I/O**
- **Automatic Page Write Operation:**
  - **–1 to 32 Bytes in 5ms**
  - **–Page Load Timer**
- **End of Write Detection:**
  - **–Toggle Bit**
  - **–$\overline{\text{DATA}}$ Polling**
  - **–RDY/$\overline{\text{BUSY}}$**
- **Hardware and Software Write Protection**
- **10,000 Program/Erase Cycles**
- **100 Year Data Retention**
- **Optional High Endurance Device Available**

DESCRIPTION

The CAT28C65B/CAT28C65BI is a fast, low power, 5V-only CMOS E²PROM organized as 8K x 8 bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling, a RDY/$\overline{\text{BUSY}}$ pin and Toggle status bits signal the start and end of the self-timed write cycle. Additionally, the CAT28C65B/CAT28C65BI features hardware and software write protection.

The CAT28C65B/CAT28C65BI is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 100 years. The device is available in JEDEC approved 28 pin DIP and SO or 32 pin PLCC and TSOP packages.

BLOCK DIAGRAM

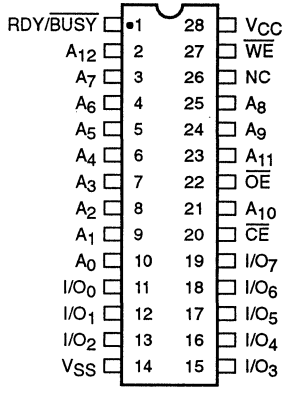


5099 FHD F02

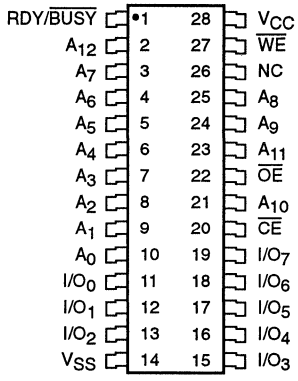
TD 5099

PIN CONFIGURATION

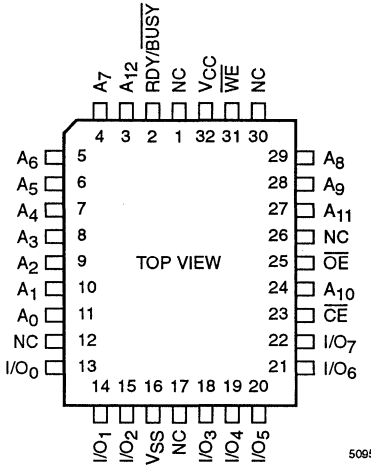
DIP Package



SO Package

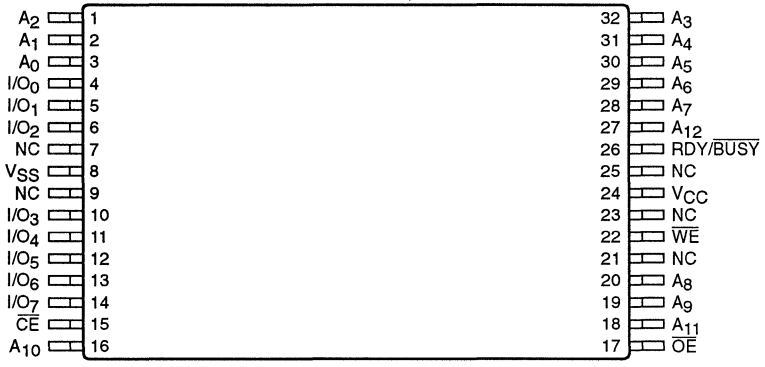


PLCC Package



5095 FHD F01

TSOP Package



5099 FHD F15

PIN FUNCTIONS

Pin Name	Function
A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
RDY/$\overline{BUSY}$	Ready/$\overline{BUSY}$ Status
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	5V Supply
V_{SS}	Ground
NC	No Connect

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with
Respect to Ground(2) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation
Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(3) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(1)	Endurance	10,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(1)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT28C65B T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C65BI T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

		Limits				
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{CC}	V_{CC} Current (Operating, TTL)			30	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 1/t_{RC} min, All I/O's Open
I_{CCC}(5)	V_{CC} Current (Operating, CMOS)			25	mA	$\overline{CE}$ = $\overline{OE}$ = V_{ILC}, f = 1/t_{RC} min, All I/O's Open
I_{SB}	V_{CC} Current (Standby, TTL)			1	mA	$\overline{CE}$ = V_{IH}, All I/O's Open
I_{SBC}(6)	V_{CC} Current (Standby, CMOS)			100	µA	$\overline{CE}$ = V_{IHC}, All I/O's Open
I_{LI}	Input Leakage Current	–1		1	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	–10		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IH}(6)	High Level Input Voltage	2.0		V_{CC} +0.3	V	
V_{IL}(5)	Low Level Input Voltage	–0.3		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1mA
V_{WI}	Write Inhibit Voltage	3.5			V	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} +1V.
(5) V_{ILC} = –0.3V to +0.3V.
(6) V_{IHC} = V_{CC} –0.3V to V_{CC} +0.3V.

A.C. CHARACTERISTICS, Read Cycle

CAT28C65B T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C65BI T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C65B-12		28C65B-15 28C65BI-15		28C65B-20 28C65BI-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	120		150		200		ns
t_{CE}	$\overline{CE}$ Access Time		120		150		200	ns
t_{AA}	Address Access Time		120		150		200	ns
t_{OE}	$\overline{OE}$ Access Time		60		70		80	ns
t_{LZ}(1)	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ}(1)	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ}(1)(7)	$\overline{CE}$ High to High-Z Output		50		50		55	ns
t_{OHZ}(1)(7)	$\overline{OE}$ High to High-Z Output		50		50		55	ns
t_{OH}(1)	Output Hold from Address Change	0		0		0		ns

Figure 1. A.C. Testing Input/Output Waveform(8)

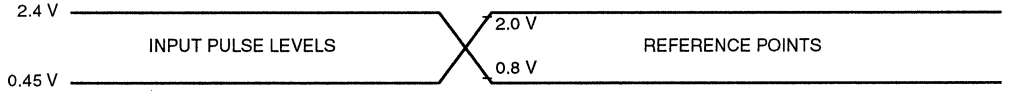


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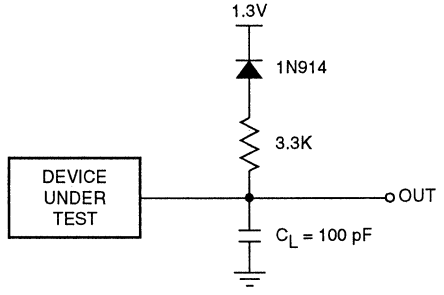
Figure 2. A.C. Testing Load Circuit (example)



C_L INCLUDES JIG CAPACITANCE

5096 FHD F04

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(7) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.
(8) Input rise and fall times (10% and 90%) < 10 ns.

A.C. CHARACTERISTICS, Write Cycle

CAT28C65B T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C65BI T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

		28C65B-12		28C65B-15 28C65BI-15		28C65B-20 28C65BI-20		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{WC}	Write Cycle Time		5		5		5	ms
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	100		100		120		ns
t_{CS}	Write Setup Time	0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		ns
t_{CW}(9)	$\overline{CE}$ Pulse Time	150		150		150		ns
t_{OES}	$\overline{OE}$ Setup Time	10		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		10		ns
t_{WP}(9)	$\overline{WE}$ Pulse Width	150		150		150		ns
t_{RB}	$\overline{WE}$ Low to RDY/$\overline{BUSY}$ Low		120		120		120	ns
t_{DS}	Data Setup Time	70		70		70		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{INIT}(1)	Write Inhibit Period After Power-up	5	10	5	10	5	10	ms
t_{BLC}(1)(10)	Byte Load Cycle Time	.05	100	.05	100	.05	100	µs

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(9) A write pulse of less than 20ns duration will not initiate a write cycle.
(10) A timer of duration t_{BLC} max. begins with every LOW to HIGH transition of $\overline{WE}$. If allowed to time out, a page or byte write will begin; however a transition from HIGH to LOW within t_{BLC} max. stops the timer.

DEVICE OPERATION

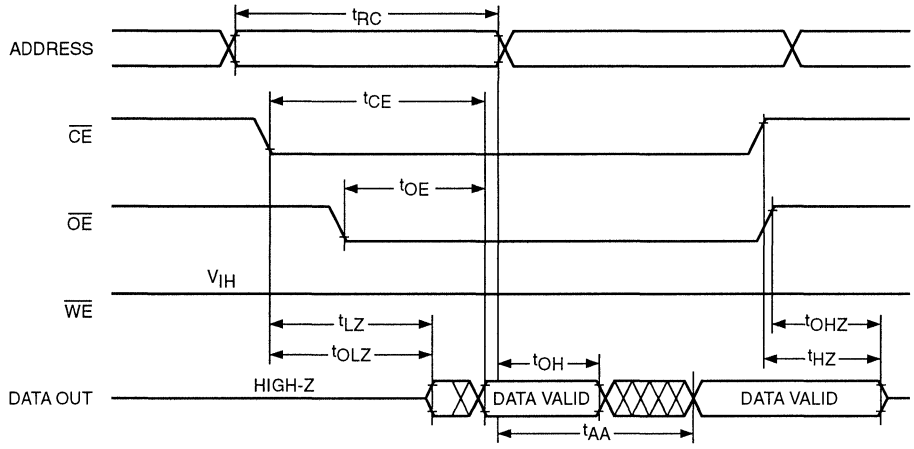
Read

Data stored in the CAT28C65B/CAT28C65BI is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Byte Write

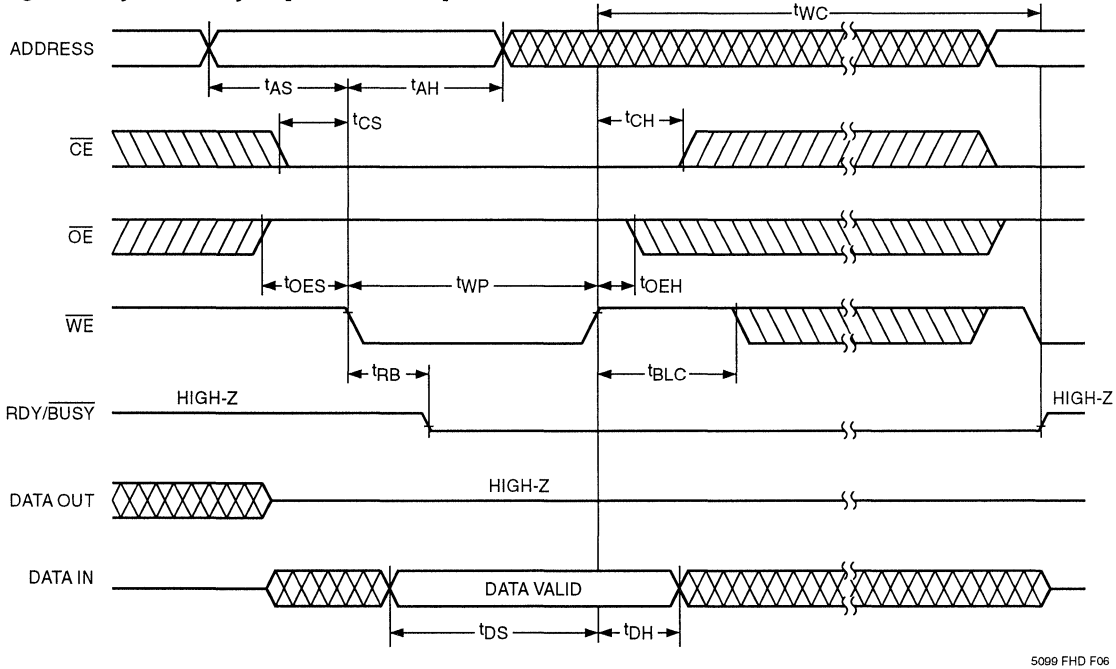
A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the

Figure 3. Read Cycle



5096 FHD F05

Figure 4. Byte Write Cycle [$\overline{WE}$ Controlled]



5099 FHD F06

falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 5 ms.

Page Write

The page write mode of the CAT28C65B/CAT28C65BI (essentially an extended BYTE WRITE mode) allows from 1 to 32 bytes of data to be programmed within a single E^2PROM write cycle. This effectively reduces the byte-write time by a factor of 32.

Following an initial WRITE operation ($\overline{WE}$ pulsed low, for t_{WP}, and then high) the page write mode can begin by issuing sequential $\overline{WE}$ pulses, which load the address and data bytes into a 32 byte temporary buffer. The page address where data is to be written, specified by bits A_5 to A_{12}, is latched on the last falling edge of $\overline{WE}$. Each byte within the page is defined by address bits A_0 to A_4

Figure 5. Byte Write Cycle [$\overline{CE}$ Controlled]

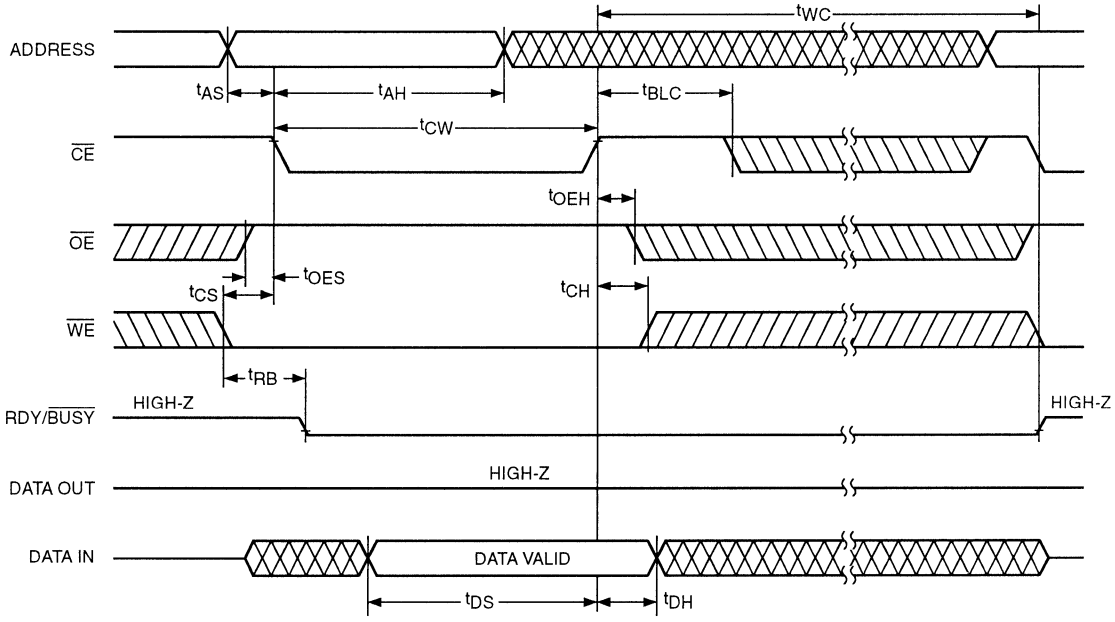
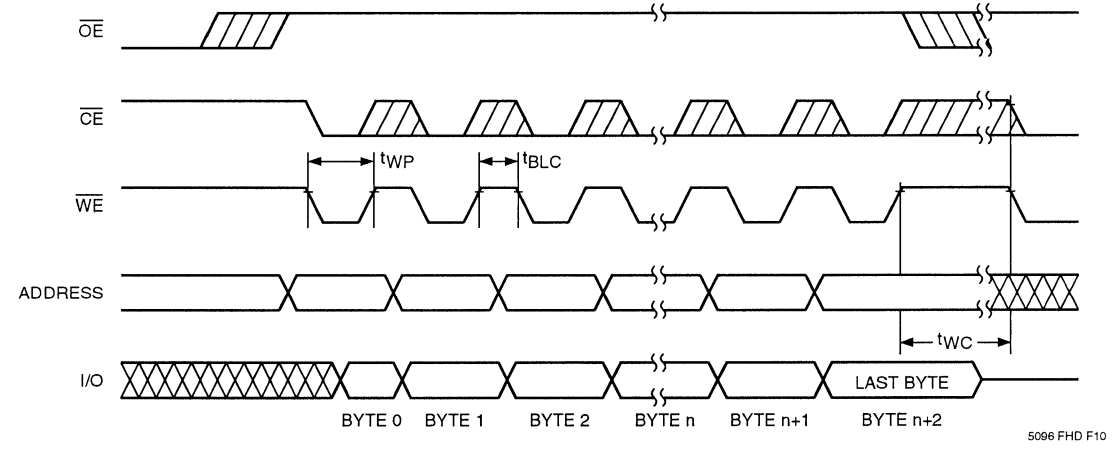


Figure 6. Page Mode Write Cycle



(which can be loaded in any order) during the first and subsequent write cycles. Each successive byte load cycle must begin within $t_{BLC\ MAX}$ of the rising edge of the preceding $\overline{WE}$ pulse. There is no page write window limitation as long as $\overline{WE}$ is pulsed low within $t_{BLC\ MAX}$.

Upon completion of the page write sequence, $\overline{WE}$ must stay high a minimum of $t_{BLC\ MAX}$ for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

$\overline{DATA}$ Polling

$\overline{DATA}$ polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0–I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle, all I/O's will output true data during a read cycle.

Toggle Bit

In addition to the $\overline{DATA}$ Polling feature of the CAT28C65B/CAT28C65BI, the device offers an additional method for determining the completion of a write cycle. While a write cycle is in progress, reading data from the device will result in I/O_6 toggling between one and zero. However, once the write is complete, I/O_6 stops toggling and valid data can be read from the device.

Ready/$\overline{BUSY}$ (RDY/$\overline{BUSY}$)

The RDY/$\overline{BUSY}$ pin is an open drain output which indicates device status during programming. It is pulled low during the write cycle and released at the end of programming. Several devices may be OR-tied to the same RDY/$\overline{BUSY}$ line.

Figure 7. $\overline{DATA}$ Polling

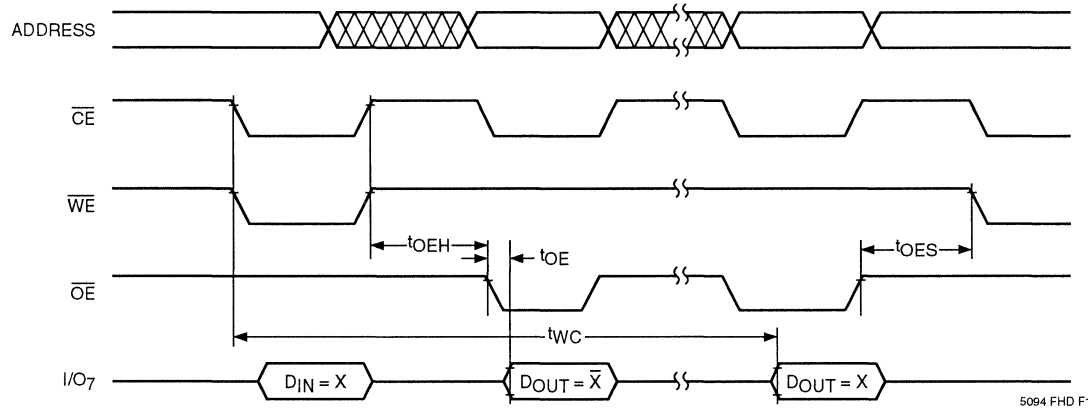
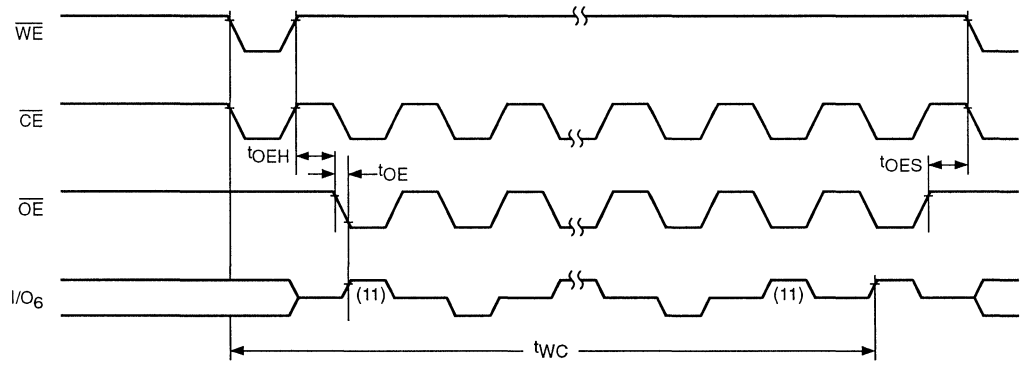


Figure 8. Toggle Bit



Note:
(11) Beginning and ending state of I/O_6 is indeterminate.

HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28C65B/ CAT28C65BI.

(1) V_{CC} sense provides for write protection when V_{CC} falls below 3.5V min.

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 10 ms delay before a write sequence, after V_{CC} has reached 3.5V min.

(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

SOFTWARE DATA PROTECTION

The CAT28C65B/CAT28C65BI features a software controlled data protection scheme which, once enabled, requires a data algorithm to be issued to the device before a write can be performed. The device is shipped from Catalyst with the software protection NOT ENABLED (the CAT28C65B/CAT28C65BI is in the standard operating mode).

Figure 9. Write Sequence for Activating Software Data Protection

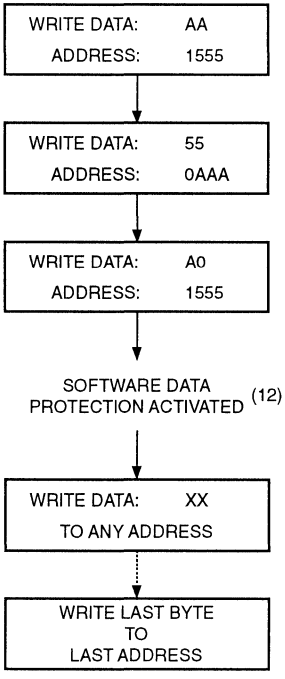


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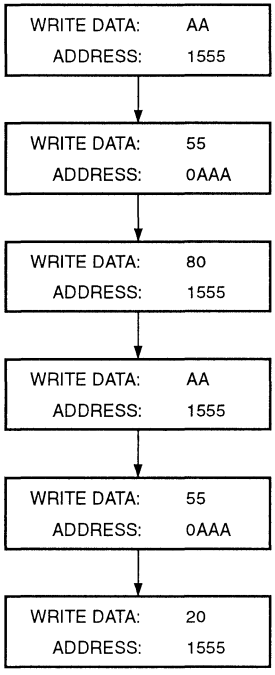
Figure 10. Write Sequence for Deactivating Software Data Protection



5094 FHD F09

Note:
(12) Write protection is activated at this point whether or not any more writes are completed. Writing to addresses must occur within t_{BLC} Max., after SDP activation.

To activate the software data protection, the device must be sent three write commands to specific addresses with specific data (Figure 9). This sequence of commands (along with subsequent writes) must adhere to the page write timing specifications (Figure 11). Once this is done, all subsequent byte or page writes to the device must be preceded by this same set of write commands. The data protection mechanism is activated until a deactivate sequence is issued regardless of power on/off transitions. This gives the user added inadvertent write protection on power-up in addition to the hardware protection provided.

To allow the user the ability to program the device with an E^2PROM programmer (or for testing purposes) there is a software command sequence for deactivating the data protection. The six step algorithm (Figure 10) will reset the internal protection circuitry, and the device will return to standard operating mode (Figure 12 provides reset timing). After the sixth byte of this reset sequence has been issued, standard byte or page writing can commence.

Figure 11. Software Data Protection Timing

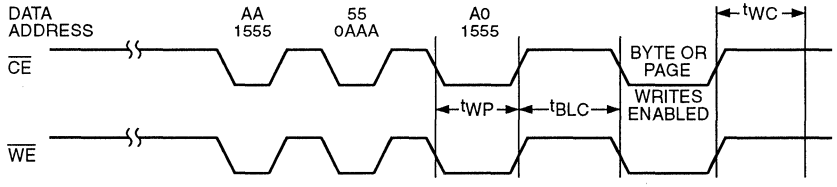


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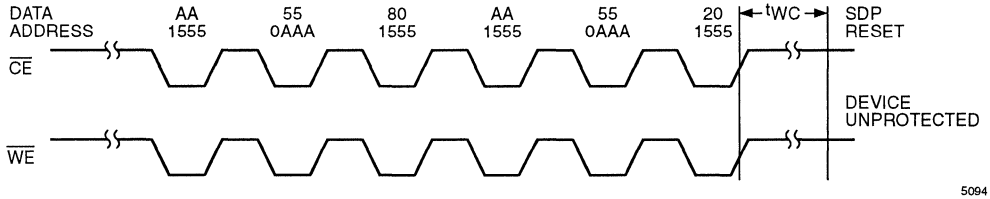
Figure 12. Resetting Software Data Protection Timing



5094 FHD F14

CAT28C256/CAT28C256I

256K-Bit CMOS E²PROM

FEATURES

- Fast Read Access Times: 200/250/300 ns
- Low Power CMOS Dissipation:
  - –Active: 30mA Max.
  - –Standby: 150µA Max.
- Simple Write Operation:
  - –On-Chip Address and Data Latches
  - –Self-Timed Write Cycle with Auto-Clear
- Fast Nonvolatile Write Cycle:
  - –10ms Max (5ms available)
- CMOS and TTL Compatible I/O
- Automatic Page Write Operation:
  - –1 to 64 Bytes in 10ms
  - –Page Load Timer
- End of Write Detection:
  - –Toggle Bit
  - –$\overline{\text{DATA}}$ Polling
- Hardware and Software Write Protection
- 10,000 Program/Erase Cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

DESCRIPTION

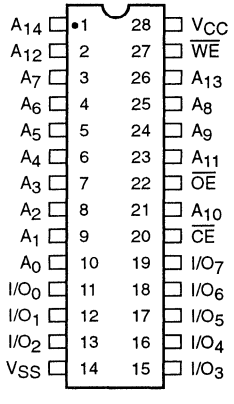
The CAT28C256/CAT28C256I is a fast, low power, 5V-only CMOS E²PROM organized as 32K x 8 bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling and Toggle status bits signal the start and end of the self-timed write cycle. Additionally, the CAT28C256/CAT28C256I features hardware and software write protection as well as an internal Error Correction Code (ECC) for extremely high reliability.

The CAT28C256/CAT28C256I is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 100 years. The device is available in JEDEC approved 28 pin DIP or 32 pin PLCC packages.

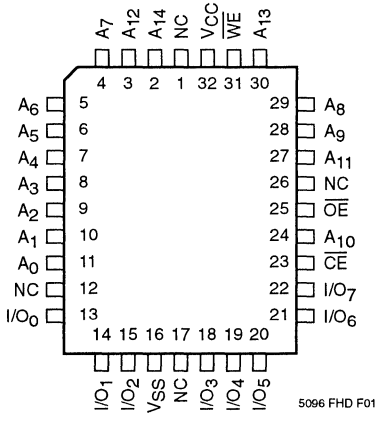
7

PIN CONFIGURATION

DIP Package



PLCC Package



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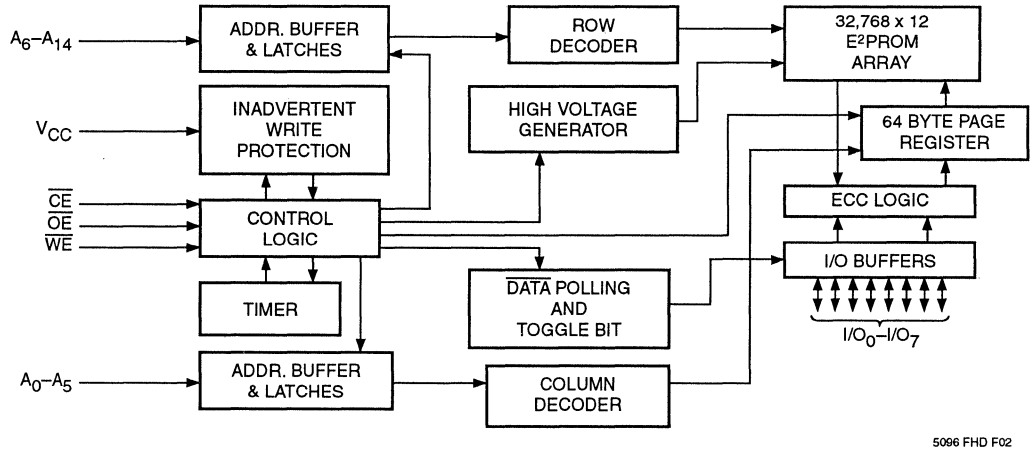
PIN FUNCTIONS

Pin Name	Function
A_0–A_{14}	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	5V Supply
V_{SS}	Ground
NC	No Connect

TD 5096

BLOCK DIAGRAM



MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte Write ($\overline{WE}$ Controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte Write ($\overline{CE}$ Controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with
Respect to Ground(2) .....–2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground .....–2.0V to +7.0V

Package Power Dissipation
Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(3) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(1)	Endurance	10,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(1)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(4)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT28C256 T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C256I T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

		Limits				
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{CC}	V_{CC} Current (Operating, TTL)			30	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 1/t_{RC} min, All I/O's Open
I_{CCC}(5)	V_{CC} Current (Operating, CMOS)			25	mA	$\overline{CE}$ = $\overline{OE}$ = V_{ILC}, f = 1/t_{RC} min, All I/O's Open
I_{SB}	V_{CC} Current (Standby, TTL)			1	mA	$\overline{CE}$ = V_{IH}, All I/O's Open
I_{SBC}(6)	V_{CC} Current (Standby, CMOS)			150	µA	$\overline{CE}$ = V_{IHC}, All I/O's Open
I_{LI}	Input Leakage Current	–1		1	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	–10		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IH}(6)	High Level Input Voltage	2.0		V_{CC} +0.3	V	
V_{IL}(5)	Low Level Input Voltage	–0.3		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –400µA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 2.1mA
V_{WI}	Write Inhibit Voltage	3.5			V	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} +1V.
(5) V_{ILC} = –0.3V to +0.3V.
(6) V_{IHC} = V_{CC} –0.3V to V_{CC} +0.3V.

A.C. CHARACTERISTICS, Read Cycle

CAT28C256 T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C256I T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C256-20 28C256I-20		28C256-25 28C256I-25		28C256-30 28C256I-30		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		300		ns
t_{CE}	$\overline{CE}$ Access Time		200		250		300	ns
t_{AA}	Address Access Time		200		250		300	ns
t_{OE}	$\overline{OE}$ Access Time		80		100		110	ns
t_{LZ}(1)	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ}(1)	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ}(1)(7)	$\overline{CE}$ High to High-Z Output		50		50		55	ns
t_{OHZ}(1)(7)	$\overline{OE}$ High to High-Z Output		50		50		55	ns
t_{OH}(1)	Output Hold from Address Change	0		0		0		ns

Figure 1. A.C. Testing Input/Output Waveform(8)

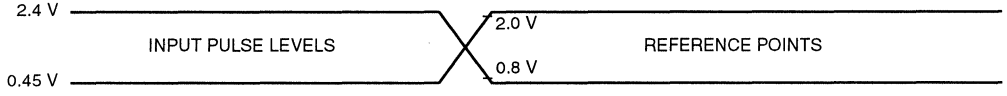


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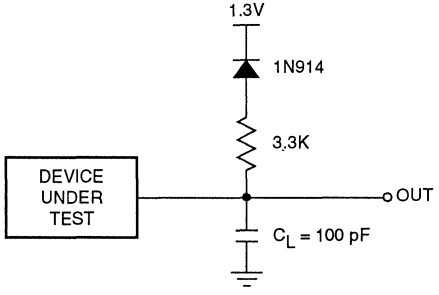
Figure 2. A.C. Testing Load Circuit (example)



C_L INCLUDES JIG CAPACITANCE

5096 FHD F04

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(7) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.
(8) Input rise and fall times (10% and 90%) < 10 ns.

A.C. CHARACTERISTICS, Write Cycle

CAT28C256 T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
CAT28C256I T_A = –40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	28C256-20 28C256I-20		28C256-25 28C256I-25		28C256-30 28C256I-30		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		10		10		10	ms
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	100		100		120		ns
t_{CS}	Write Setup Time	0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		ns
t_{CW}(9)	$\overline{CE}$ Pulse Time	100		100		120		ns
t_{OES}	$\overline{OE}$ Setup Time	10		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		10		ns
t_{WP}(9)	$\overline{WE}$ Pulse Width	100		100		120		ns
t_{DS}	Data Setup Time	50		50		50		ns
t_{DH}	Data Hold Time	10		10		20		ns
t_{INIT}(1)	Write Inhibit Period After Power-up	5	10	5	10	5	10	ms
t_{BLC}(1)(10)	Byte Load Cycle Time	.1	100	.1	100	.1	100	µs

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(9) A write pulse of less than 20ns duration will not initiate a write cycle.
(10) A timer of duration t_{BLC} max. begins with every LOW to HIGH transition of $\overline{WE}$. If allowed to time out, a page or byte write will begin; however a transition from HIGH to LOW within t_{BLC} max. stops the timer.

7

DEVICE OPERATION

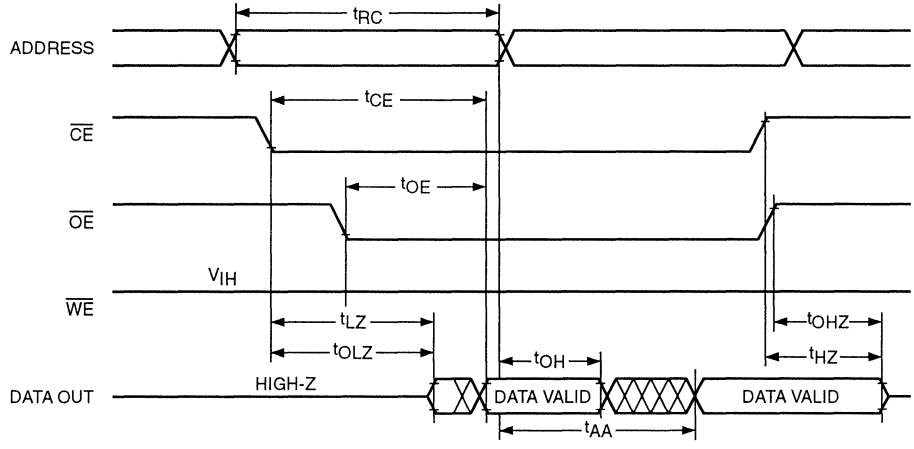
Read

Data stored in the CAT28C256/CAT28C256I is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Byte Write

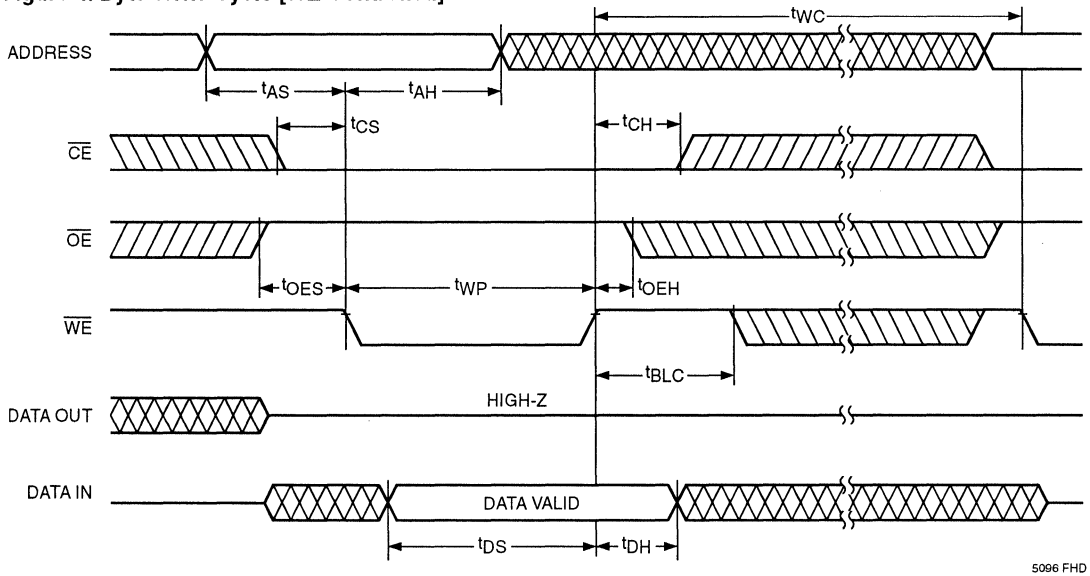
A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 10 ms.

Figure 3. Read Cycle



5096 FHD F05

Figure 4. Byte Write Cycle [$\overline{WE}$ Controlled]



5096 FHD F06

Page Write

The page write mode of the CAT28C256/CAT28C256I (essentially an extended BYTE WRITE mode) allows from 1 to 64 bytes of data to be programmed within a single E^2PROM write cycle. This effectively reduces the byte-write time by a factor of 64.

Following an initial WRITE operation ($\overline{WE}$ pulsed low, for t_{WP}, and then high) the page write mode can begin by issuing sequential $\overline{WE}$ pulses, which load the address and data bytes into a 64 byte temporary buffer. The page address where data is to be written, specified by bits A_6 to A_{14}, is latched on the last falling edge of $\overline{WE}$. Each byte within the page is defined by address bits A_0 to A_5 (which can be loaded in any order) during the first and subsequent write cycles. Each successive byte load cycle must begin within $t_{BLC\ MAX}$ of the rising edge of the preceding $\overline{WE}$ pulse. There is no page write window limitation as long as $\overline{WE}$ is pulsed low within $t_{BLC\ MAX}$.

Upon completion of the page write sequence, $\overline{WE}$ must stay high a minimum of $t_{BLC\ MAX}$ for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

Figure 5. Byte Write Cycle [$\overline{CE}$ Controlled]

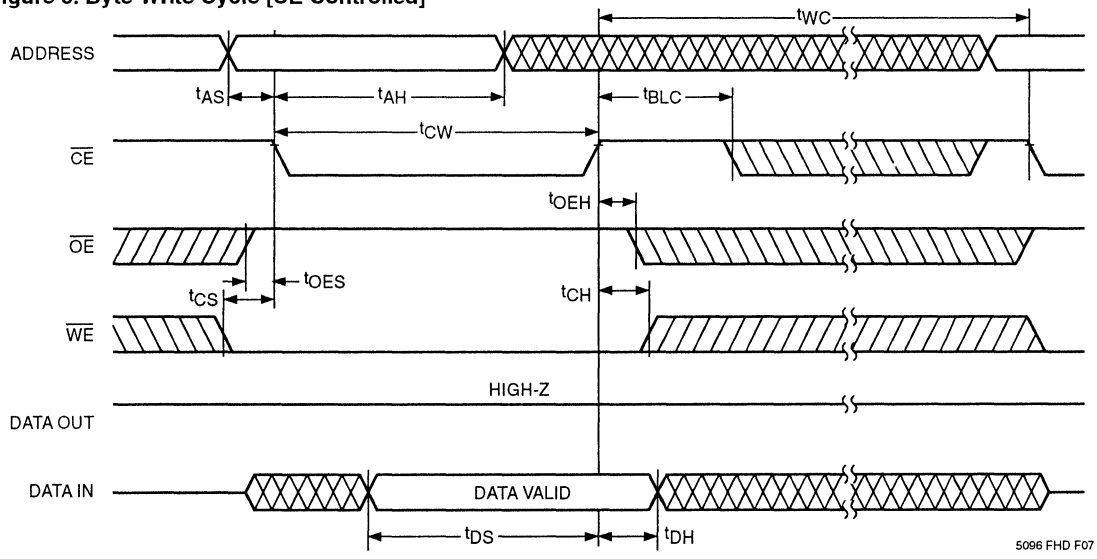
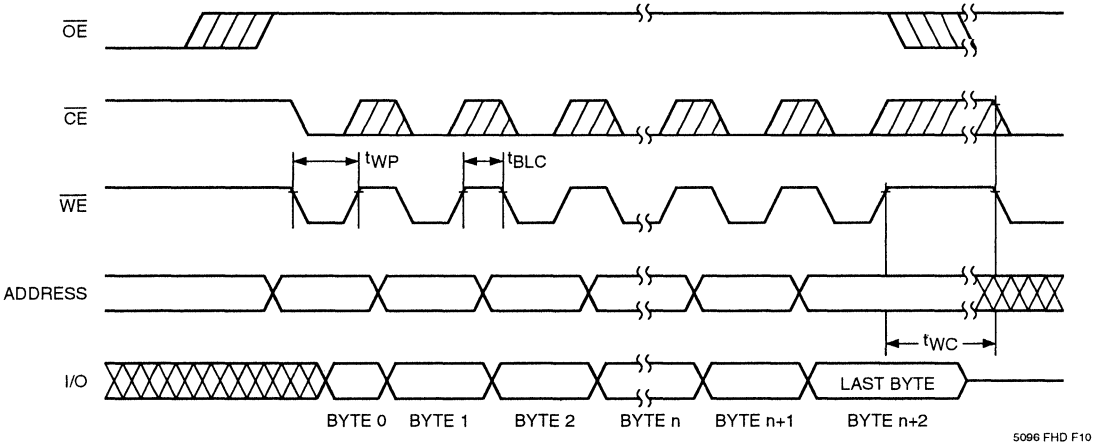


Figure 6. Page Mode Write Cycle



$\overline{\text{DATA}}$ Polling

$\overline{\text{DATA}}$ polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0–I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle, all I/O's will output true data during a read cycle.

Toggle Bit

In addition to the $\overline{\text{DATA}}$ Polling feature of the CAT28C256/ CAT28C256I, the device offers an additional method for determining the completion of a write cycle. While a write cycle is in progress, reading data from the device will result in I/O_6 toggling between one and zero. However, once the write is complete, I/O_6 stops toggling and valid data can be read from the device.

Figure 7. $\overline{\text{DATA}}$ Polling

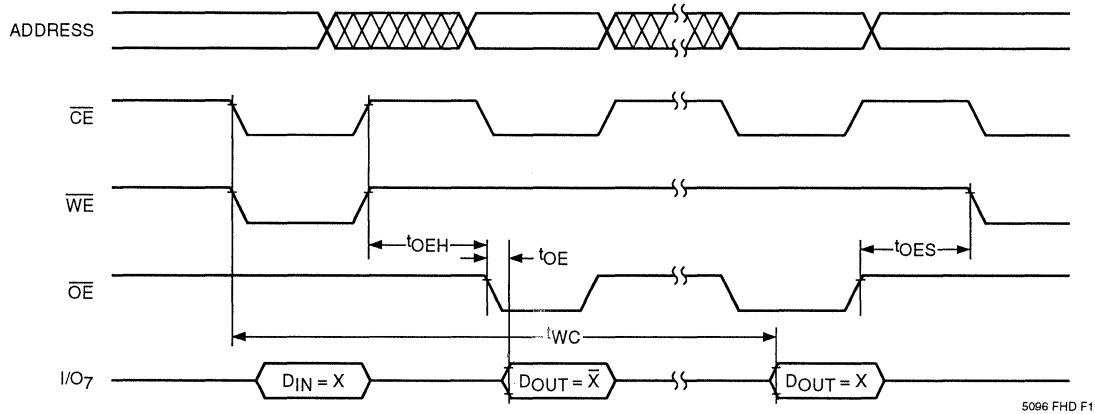
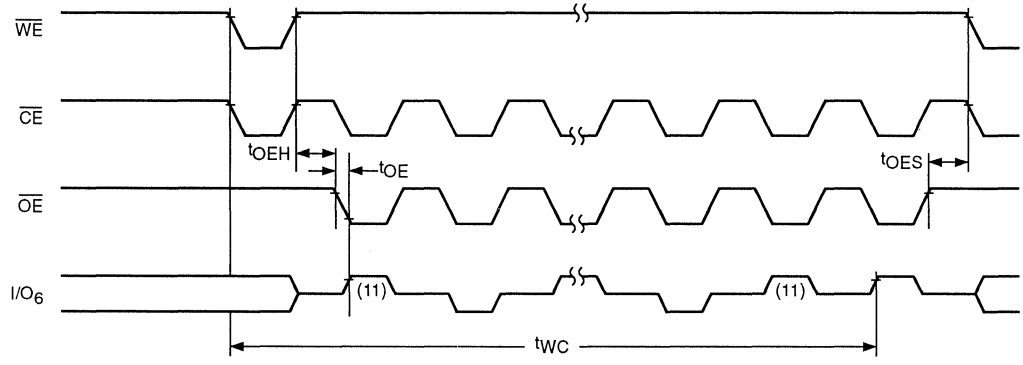


Figure 8. Toggle Bit



Note:
(11) Beginning and ending state of I/O_6 is indeterminate.

HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28C256/ CAT28C256I.

(1) V_{CC} sense provides for write protection when V_{CC} falls below 3.5V min.

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 10 ms delay before a write sequence, after V_{CC} has reached 3.5V min.

(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

SOFTWARE DATA PROTECTION

The CAT28C256/CAT28C256I features a software controlled data protection scheme which, once enabled, requires a data algorithm to be issued to the device before a write can be performed. The device is shipped from Catalyst with the software protection NOT ENABLED (the CAT28C256/CAT28C256I is in the standard operating mode).

Figure 9. Write Sequence for Activating Software Data Protection

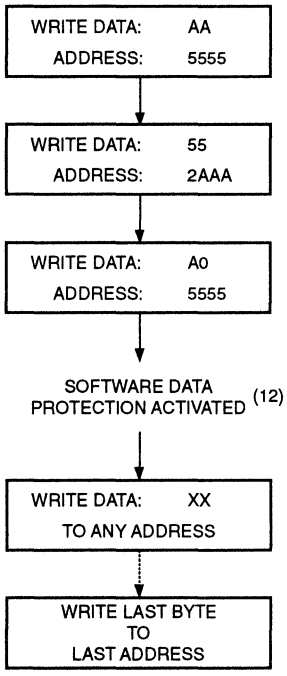


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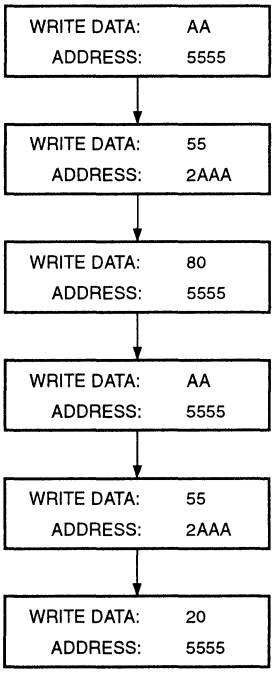
Figure 10. Write Sequence for Deactivating Software Data Protection



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Note:
(12) Write protection is activated at this point whether or not any more writes are completed. Writing to addresses must occur within t_{BLC} Max., after SDP activation.

To activate the software data protection, the device must be sent three write commands to specific addresses with specific data (Figure 9). This sequence of commands (along with subsequent writes) must adhere to the page write timing specifications (Figure 11). Once this is done, all subsequent byte or page writes to the device must be preceded by this same set of write commands. The data protection mechanism is activated until a deactivate sequence is issued regardless of power on/off transitions. This gives the user added inadvertent write protection on power-up in addition to the hardware protection provided.

To allow the user the ability to program the device with an E^2PROM programmer (or for testing purposes) there is a software command sequence for deactivating the data protection. The six step algorithm (Figure 10) will reset the internal protection circuitry, and the device will return to standard operating mode (Figure 12 provides reset timing). After the sixth byte of this reset sequence has been issued, standard byte or page writing can commence.

Figure 11. Software Data Protection Timing

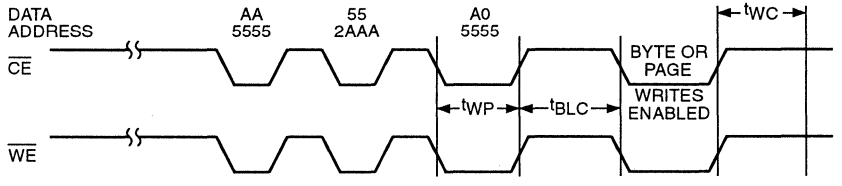

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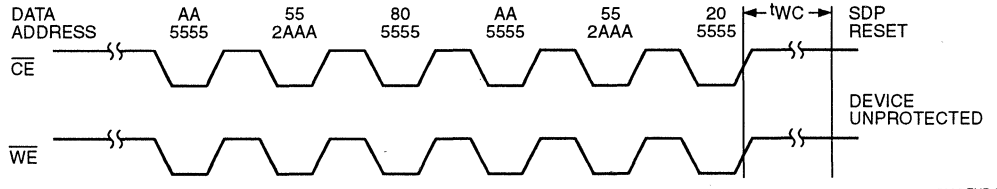
Figure 12. Resetting Software Data Protection Timing



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CATALYST SEMICONDUCTOR

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2-Wire Bus Serial E^2PROMs 2

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CAT28F512/CAT28F512I ..... 64K x 8 ..... 512K-Bit 8-1

CAT28F512V5/CAT28F512V5I ..... 64K x 8 ..... 512K-Bit 8-19

CAT28F010/CAT28F010I ..... 128K x 8 ..... 1M-Bit 8-37

CAT28F010V5/CAT28F010V5I ..... 128K x 8 ..... 1M-Bit 8-55

CAT28F020/CAT28F020I ..... 256K x 8 ..... 2M-Bit 8-73

CATALYST SEMICONDUCTOR

CAT28F512/CAT28F512I

512K-Bit CMOS FLASH MEMORY

FEATURES

- Fast Read Access Time: 120/150/200 ns
- Low Power CMOS Dissipation:
  - –Active: 30 mA max (CMOS/TTL levels)
  - –Standby: 1 mA max (TTL levels)
  - –Standby: 100 μA max (CMOS levels)
- High Speed Programming:
  - –10 μS per byte
  - –1 Sec Typ Chip Program
- 12.0V ± 5% Programming and Erase Voltage
- Stop Timer for Program/Erase
- On-chip Address and Data Latches
- JEDEC Standard Pinouts:
  - –32 pin DIP
  - –32 pin PLCC
  - –32 pin TSOP (8 x 14; 8 x 20)
- 10,000 Program/Erase Cycles
- 10 Year Data Retention
- Electronic Signature

DESCRIPTION

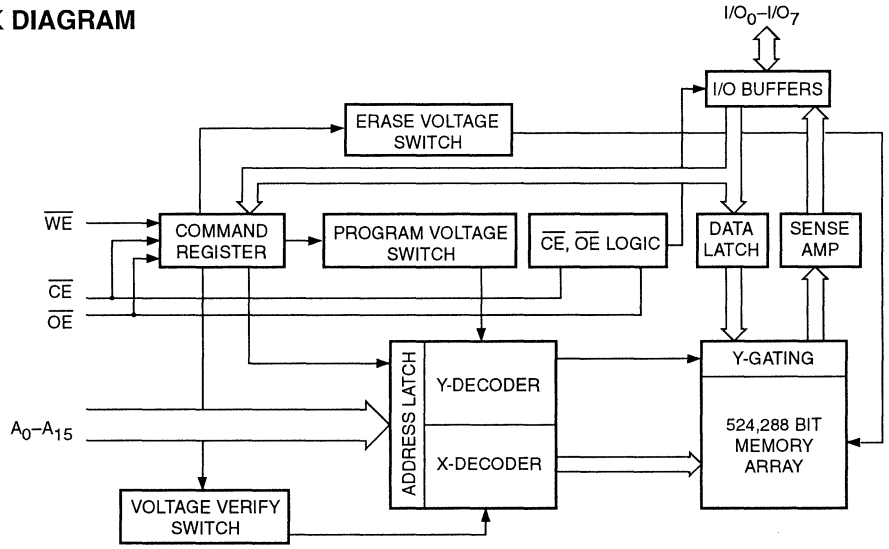
The CAT28F512/CAT28F512I is a high speed 64K x 8 bit electrically erasable and reprogrammable Flash memory ideally suited for applications requiring in-system or after-sale code updates. Electrical erasure of the full memory contents is achieved typically within 1 second.

It is pin and Read timing compatible with standard EPROM and E²PROM devices. Programming and Erase are performed through an operation and verify algorithm. The instructions are input via the I/O bus, using a two write cycle scheme. Address and Data are latched to free the I/O bus and address bus during the write operation.

The CAT28F512/CAT28F512I is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 32 pin plastic DIP, 32 pin PLCC or 32 pin TSOP packages.

8

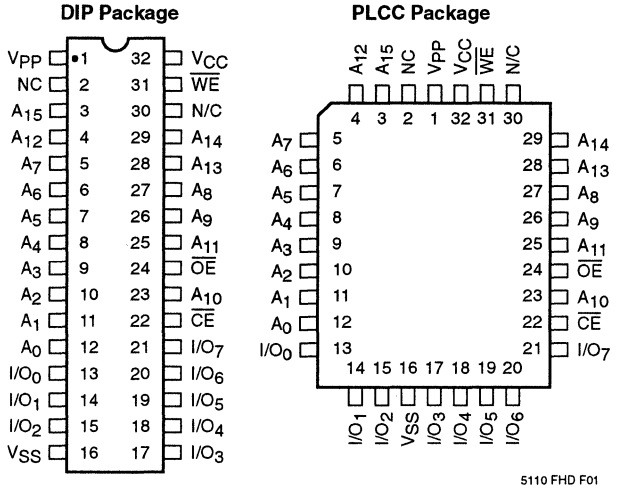
BLOCK DIAGRAM



5110 FHD F02

TD 5110

PIN CONFIGURATION

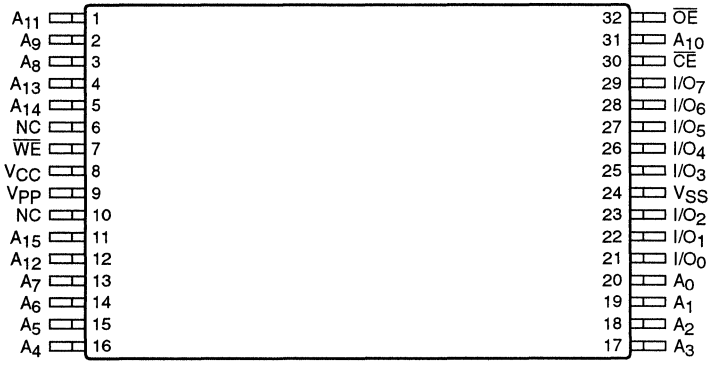


5110 FHD F01

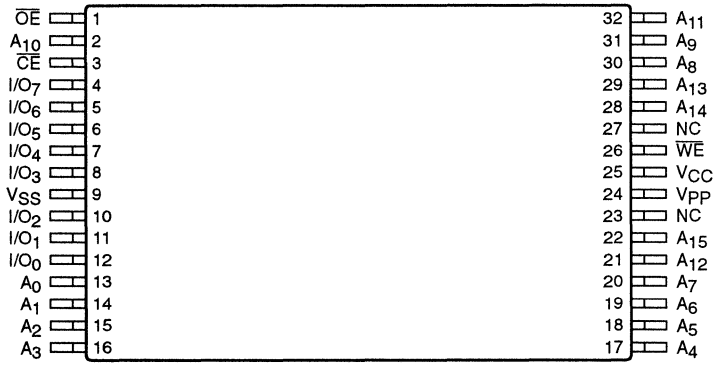
PIN FUNCTIONS

Pin Name	Type	Function
A_0–A_{15}	Input	Address Inputs for memory addressing
I/O_0–I/O_7	I/O	Data Input/Output
$\overline{CE}$	Input	Chip Enable
$\overline{OE}$	Input	Output Enable
$\overline{WE}$	Input	Write Enable
V_{CC}		Voltage Supply
V_{SS}		Ground
V_{PP}		Program/Erase Voltage Supply

TSOP Package (Standard Pinout)



TSOP Package (Reverse Pinout)



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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +95°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V

Voltage on Pin A_9 with Respect to Ground(1) ..... –2.0V to +13.5V

V_{PP} with Respect to Ground during Program/Erase(1) ..... –2.0V to +14.0V

V_{CC} with Respect to Ground(1) ..... –2.0V to +7.0V

Package Power Dissipation Capability (T_A = 25°C) ..... 1.0 W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(3)	Endurance	1K, 10K		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Limits		Units	Conditions
		Min	Max.		
C_{IN}(3)	Input Pin Capacitance		6	pF	V_{IN} = 0V
C_{OUT}(3)	Output Pin Capacitance		10	pF	V_{OUT} = 0V
C_{VPP}(3)	V_{PP} Supply Capacitance		25	pF	V_{PP} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

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D.C. OPERATING CHARACTERISTICS

CAT28F512 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT28F512I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{LI}	Input Leakage Current		±1.0	µA	V_{IN} = V_{CC} or V_{SS} V_{CC} = 5.5V, $\overline{OE}$ = V_{IH}
I_{LO}	Output Leakage Current		±10	µA	V_{OUT} = V_{CC} or V_{SS}, V_{CC} = 5.5V, $\overline{OE}$ = V_{IH}
I_{SB1}	V_{CC} Standby Current CMOS		100	µA	$\overline{CE}$ = V_{CC} ±0.5V, V_{CC} = 5.5V
I_{SB2}	V_{CC} Standby Current TTL		1.0	mA	$\overline{CE}$ = V_{IH}, V_{CC} = 5.5V
I_{CC1}	V_{CC} Active Read Current		30	mA	V_{CC} = 5.5V, $\overline{CE}$ = V_{IL}, I_{OUT} = 0mA, f = 6 MHz
I_{CC2}(3)	V_{CC} Programming Current		15	mA	V_{CC} = 5.5V, Programming in Progress
I_{CC3}(3)	V_{CC} Erase Current		15	mA	V_{CC} = 5.5V, Erasure in Progress
I_{CC4}(3)	V_{CC} Prog./Erase Verify Current		15	mA	V_{PP} = V_{PPH}, Program or Erase Verify in Progress
I_{PPS}	V_{PP} Standby Current		±10	µA	V_{PP} = V_{PPL}
I_{PP1}	V_{PP} Read Current		200	µA	V_{PP} = V_{PPH}
I_{PP2}(3)	V_{PP} Programming Current		30	mA	V_{PP} = V_{PPH}, Programming in Progress
I_{PP3}(3)	V_{PP} Erase Current		30	mA	V_{CC} = 5.5V, Erasure in Progress
I_{PP4}(3)	V_{PP} Prog./Erase Verify Current		5.0	mA	V_{PP} = V_{PPH}, Program or Erase Verify in Progress
V_{IL}	Input Low Level TTL	–0.5	0.8	V	
V_{ILC}	Input Low Level CMOS	–0.5	0.8	V	
V_{OL}	Output Low Level		0.45	V	I_{OL} = 5.8mA, V_{CC} = 4.5V
V_{IH}	Input High Level TTL	2.0	V_{CC}+0.5	V	
V_{IHC}	Input High Level CMOS	0.7 V_{CC}	V_{CC}+0.5	V	
V_{OH}	Output High Level TTL	2.4		V	I_{OH} = –2.5mA, V_{CC} = 4.5V
V_{OH1}	Output High Level CMOS	0.85 V_{CC}		V	I_{OH} = –2.5mA, V_{CC} = 4.5V
V_{OH2}	Output High Level CMOS	V_{CC}–0.4		V	I_{OH} = –400µA, V_{CC} = 4.5V
V_{ID}	A_9 Signature Voltage	11.4	13.0	V	A_9 = V_{ID}
I_{ID}	A_9 Signature Current		200	µA	A_9 = V_{ID}
V_{LO}	V_{CC} Erase/Prog. Lockout Voltage	2.5		V	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.

SUPPLY CHARACTERISTICS

Symbol	Parameter	Limits		Unit
		Min	Max.	
V_{CC}	V_{CC} Supply Voltage	4.5	5.5	V
V_{PPL}	V_{PP} During Read Operations	0	6.5	V
V_{PPH}	V_{PP} During Read/Erase/Program	11.4	12.6	V

A.C. CHARACTERISTICS, Read Operation

CAT28F512 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT28F512I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	28F512-12 28F512I-12		28F512-15 28F512I-15		28F512-20 28F512I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	120		150		200		ns
t_{CE}	$\overline{CE}$ Access Time		120		150		200	ns
t_{ACC}	Address Access Time		120		150		200	ns
t_{OE}	$\overline{OE}$ Access Time		50		55		60	ns
t_{OH}	Output Hold from Address $\overline{OE}$/$\overline{CE}$ Change	0		0		0		ns
t_{OLZ}(3)(9)	$\overline{OE}$ to Output in Low-Z	0		0		0		ns
t_{LZ}(3)(9)	$\overline{CE}$ to Output in Low-Z	0		0		0		ns
t_{DF}(3)(5)	$\overline{OE}$ High to Output High-Z		30		35		40	ns
t_{EHQZ}(3)(5)	$\overline{CE}$ High to Output High-Z		55		55		55	ns
t_{WHGL}(3)	Write Recovery Time Before Read	6		6		6		µs

Figure 1. A.C. Testing Input/Output Waveform(6)(7)(8)

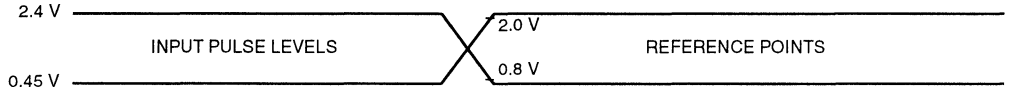

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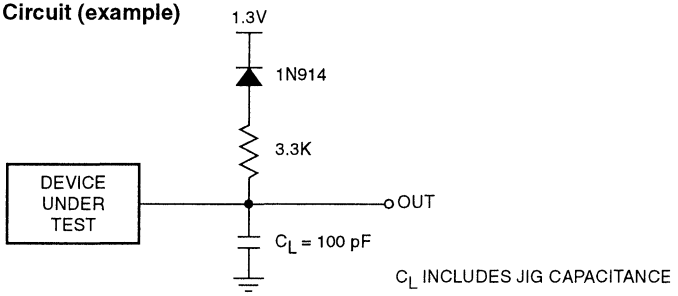
Figure 2. A.C. Testing Load Circuit (example)



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Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(5) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
(6) Input Rise and Fall Times (10% to 90%) < 10 ns.
(7) Input Pulse Levels = 0.45V and 2.4V.
(8) Input and Output Timing Reference = 0.8V and 2.0V.
(9) Low-Z is defined as the state where the external data may be driven by the output buffer but may not be valid.

8

A.C. CHARACTERISTICS, Program/Erase Operation

CAT28F512 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT28F512I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	28F512-12 28F512I-12		28F512-15 28F512I-15		28F512-20 28F512I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	120		150		200		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	60		60		75		ns
t_{DS}	Data Setup Time	50		50		50		ns
t_{DH}	Data Hold Time	10		10		10		ns
t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{WP}	$\overline{WE}$ Pulse Width	60		60		60		ns
t_{WPH}	$\overline{WE}$ High Pulse Width	20		20		20		ns
t_{WPWH1}(11)	Program Pulse Width	10		10		10		µs
t_{WPWH2}(11)	Erase Pulse Width	9.5		9.5		9.5		ms
t_{WPGL}	Write Recovery Time Before Read	6		6		6		µs
t_{GHWL}	Read Recovery Time Before Write	0		0		0		µs
t_{VPEL}	V_{PP} Setup Time to $\overline{CE}$	100		100		100		ns

ERASE AND PROGRAMMING PERFORMANCE(10)

Parameter	28F512-12 28F512I-12			28F512-15 28F512I-15			28F512-20 28F512I-20			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Erase Time(12)(14)		1.0	10		1.0	10		1.0	30	sec
Chip Program Time(12)(13)		1	12.5		1	12.5		1	12.5	sec

Note:
(10) Please refer to Supply characteristics for the value of V_{PPH} and V_{PPL}. The V_{PP} supply can be either hardwired or switched. If V_{PP} is switched, V_{PPL} can be ground, less than V_{CC} + 2.0V or a no connect with a resistor tied to ground.
(11) Program and Erase operations are controlled by internal stop timers.
(12) 'Typicals' are not guaranteed, but based on characterization data. Data taken at 25°C, 12.0V V_{PP}.
(13) Minimum byte programming time (excluding system overhead) is 16 µs (10 µs program + 6 µs write recovery), while maximum is 400 µs/byte (16 µs x 25 loops). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
(14) Excludes 00H Programming prior to Erasure.

FUNCTION TABLE(15)

Mode	Pins					Notes
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	I/O	
Read	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	D_{OUT}	
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	High-Z	
Standby	V_{IH}	X	X	V_{PPL}	High-Z	
Signature (MFG)	V_{IL}	V_{IL}	V_{IH}	X	31H	$A_0 = V_{IL}$, $A_9 = 12V$
Signature (Device)	V_{IL}	V_{IL}	V_{IH}	X	B8H	$A_0 = V_{IL}$, $A_9 = 12V$
Program/Erase	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	D_{IN}	See Command Table
Write Cycle	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	D_{IN}	During Write Cycle
Read Cycle	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	D_{OUT}	During Write Cycle

WRITE COMMAND TABLE

Commands are written into the command register in one or two write cycles. The command register can be altered only when V_{PP} is high and the instruction byte is latched on the rising edge of $\overline{WE}$. Write cycles also internally latch addresses and data required for programming and erase operations.

Mode	Pins						
	First Bus Cycle			Second Bus Cycle			
	Operation	Address	D_{IN}	Operation	Address	D_{IN}	D_{OUT}
Set Read	Write	X	00H	Read	Any		D_{OUT}
Read Sig. (MFG)	Write	X	90H	Read	00		31H
Read Sig. (Device)	Write	X	90H	Read	01		B8H
Erase	Write	X	20H	Write	X	20H	
Erase Verify	Write	X	A0H	Read	X		D_{OUT}
Program	Write	X	40H	Write	A_{IN}	D_{IN}	
Program Verify	Write	X	C0H	Read	X		D_{OUT}
Reset	Write	X	FFH	Write	X	FFH	

Note:
(15) Logic Levels: X = Logic 'Do not care' (V_{IH}, V_{IL}, V_{PPL}, V_{PPH})

8

READ OPERATIONS

Read Mode

A Read operation is performed with both $\overline{CE}$ and $\overline{OE}$ low and with $\overline{WE}$ high. V_{PP} can be either high or low, however, if V_{PP} is high, the Set READ command has to be sent before reading data (see Write Operations). The data retrieved from the I/O pins reflects the contents of the memory location corresponding to the state of the 16 address pins. The respective timing waveforms for the read operation are shown in Figure 3. Refer to the AC Read characteristics for specific timing parameters.

Signature Mode

The signature mode allows the user to identify the IC manufacturer and the type of device while the device resides in the target system. This mode can be activated in either of two ways; through the conventional method of applying a high voltage (12V) to address pin A_9 or by sending an instruction to the command register (see Write Operations).

The conventional mode is entered as a regular READ mode by driving the $\overline{CE}$ and $\overline{OE}$ pins low (with $\overline{WE}$ high) and applying the required high voltage on address pin A_9 while all other address lines are held at V_{IL}.

A Read cycle from address 0000H retrieves the binary code for the IC manufacturer on outputs I/O_0 to I/O_7:

CATALYST Code = 00110001 (31H)

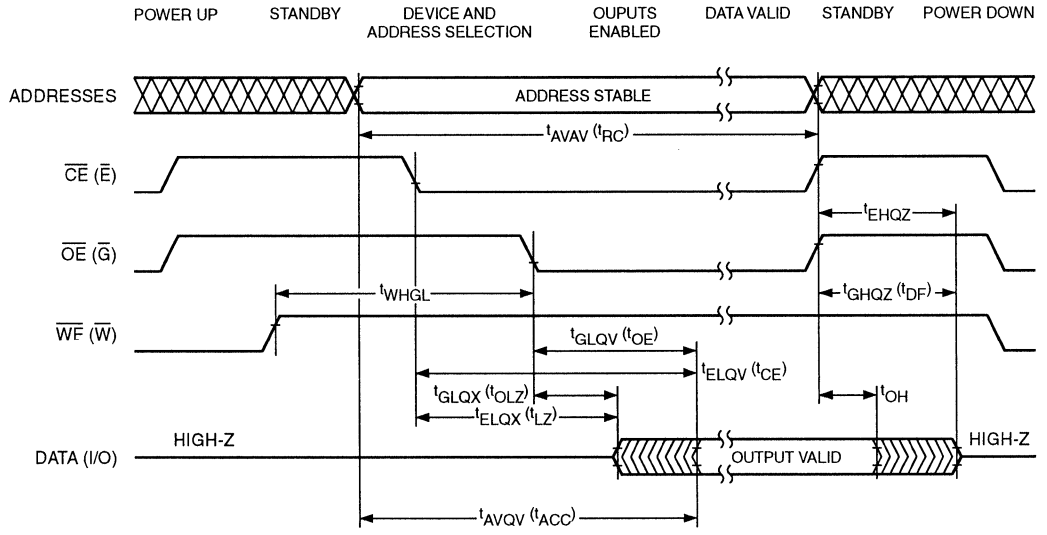
A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F512/28F512I Code = 1011 1000 (B8H)

Standby Mode

With $\overline{CE}$ at a logic-high level, the CAT28F512, CAT28F512I is placed in a standby mode where most of the device circuitry is disabled, thereby substantially reducing power consumption. The outputs are placed in a high-impedance state.

Figure 3. A.C. Timing for Read Operation



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WRITE OPERATIONS

The following operations are initiated by observing the sequence specified in the Write Command Table.

Read Mode

The device can be put into a standard READ mode by initiating a write cycle with 00H on the data bus. The subsequent read cycles will be performed similar to a standard EPROM or E²PROM Read.

Signature Mode

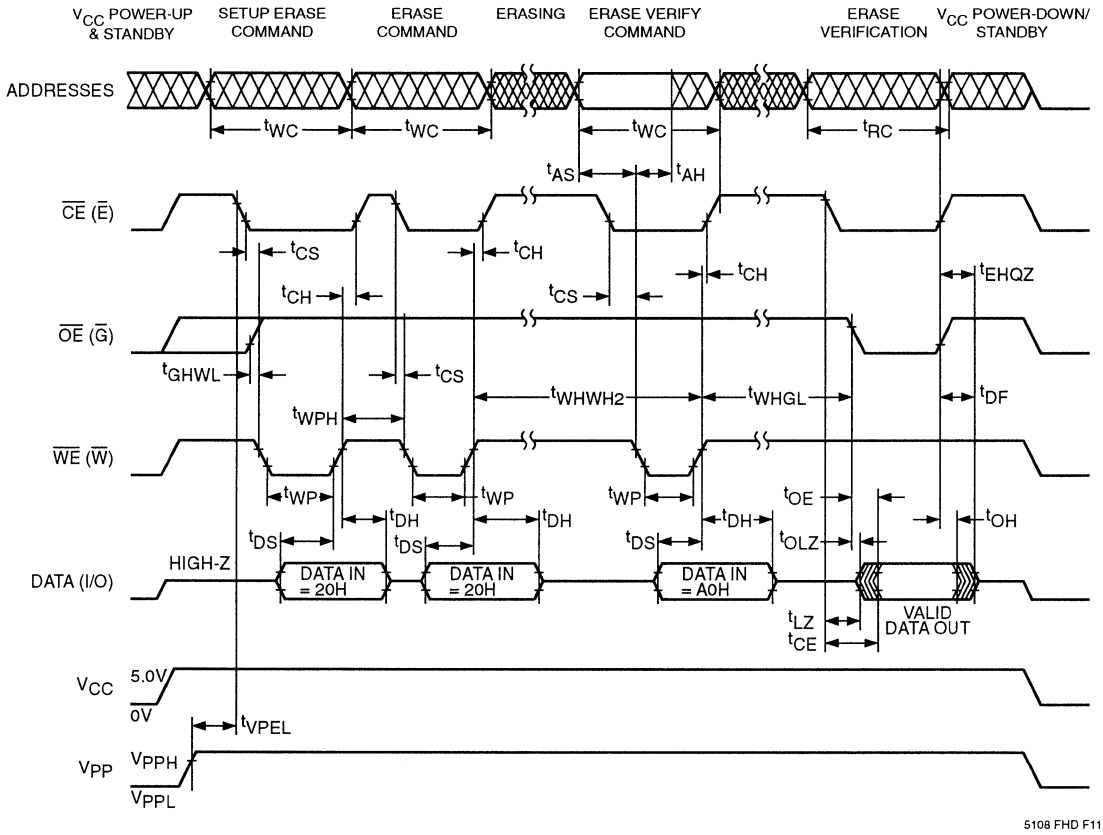
An alternative method for reading device signature (see Read Operations Signature Mode), is initiated by writing the code 90H into the command register while keeping V_{PP} high. A read cycle from address 0000H with $\overline{CE}$ and $\overline{OE}$ low (and $\overline{WE}$ high) will output the device signature.

CATALYST Code = 00110001 (31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F512/28F512I Code = 1011 1000 (B8H)

Figure 4. A.C. Timing for Erase Operation



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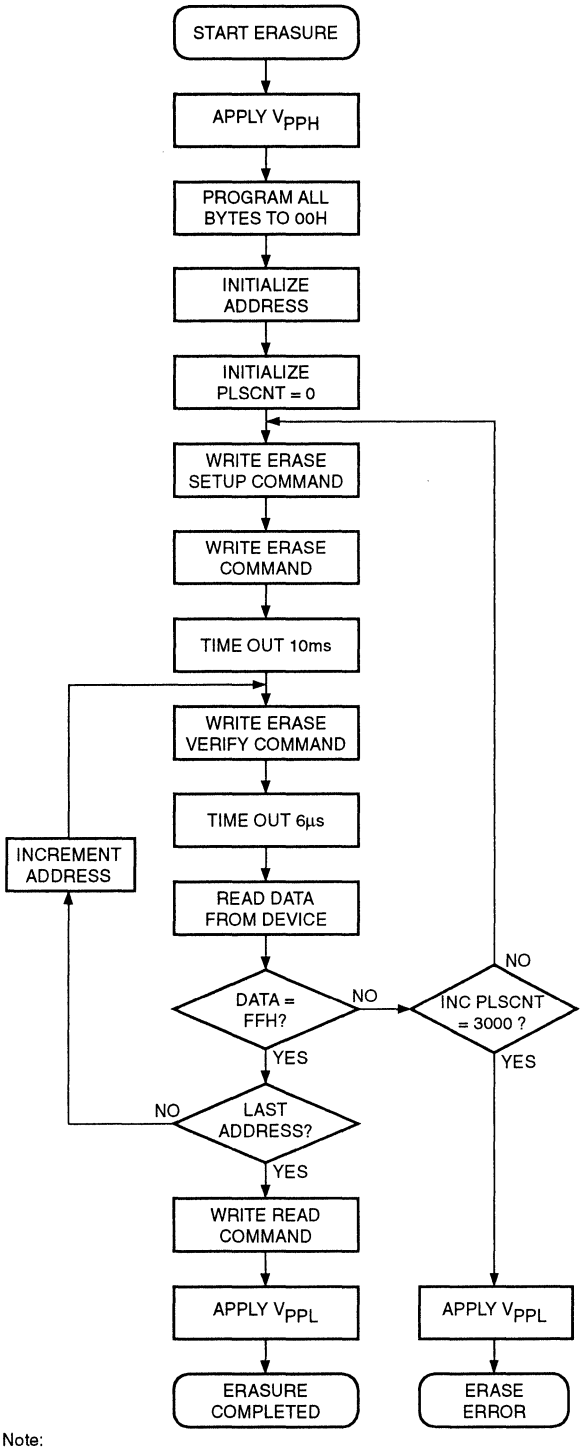
Erase Mode

During the first Write cycle, the command 20H is written into the command register. In order to commence the erase operation, the identical command of 20H has to be written again into the register. This two-step process ensures against accidental erasure of the memory contents. The final erase cycle will be stopped at the rising edge of $\overline{WE}$, at which time the Erase Verify command (A0H) is sent to the command register. During this cycle, the address to be verified is sent to the address bus and latched when $\overline{WE}$ goes high. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum erase timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

TIMING PARAMETER SYMBOLS

Standard	JEDEC	Standard	JEDEC
t_{AS}	t_{AVWL}	t_{LZ}	t_{ELQX}
t_{AH}	t_{WLAX}	t_{OE}	t_{GLQV}
t_{CE}	t_{ELQV}	t_{OLZ}	t_{GLQX}
t_{CH}	t_{WHEH}	t_{RC}	t_{AVAV}
t_{CS}	t_{ELWL}	t_{WC}	t_{AVAV}
t_{DF}	t_{GHQZ}	t_{WP}	t_{WLWH}
t_{DH}	t_{WHDX}	t_{WPH}	t_{WHWL}
t_{DS}	t_{DVWH}		

Figure 5. Chip Erase Algorithm(16)



BUS OPERATION	COMMAND	COMMENTS
		V_{PP} RAMPS TO V_{PPH} (OR V_{PP} HARDWIRED)
STANDBY		ALL BYTES SHALL BE PROGRAMMED TO 00 BEFORE AN ERASE OPERATION
		INITIALIZE ADDRESS
		PLSCNT = PULSE COUNT
WRITE	ERASE	ACTUAL ERASE NEEDS 10ms PULSE, DATA = 20H
WRITE	ERASE	DATA = 20H
		WAIT
WRITE	ERASE VERIFY	ADDRESS = BYTE TO VERIFY DATA = 20H; STOPS ERASE OPERATION
		WAIT
READ		READ BYTE TO VERIFY ERASURE
STANDBY		COMPARE OUTPUT TO FF INCREMENT PULSE COUNT
WRITE	READ	DATA = 00H RESETS THE REGISTER FOR READ OPERATION
STANDBY		V_{PP} RAMPS TO V_{PPL} (OR V_{PP} HARDWIRED)

5108 FHD F10

Note:
(16) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

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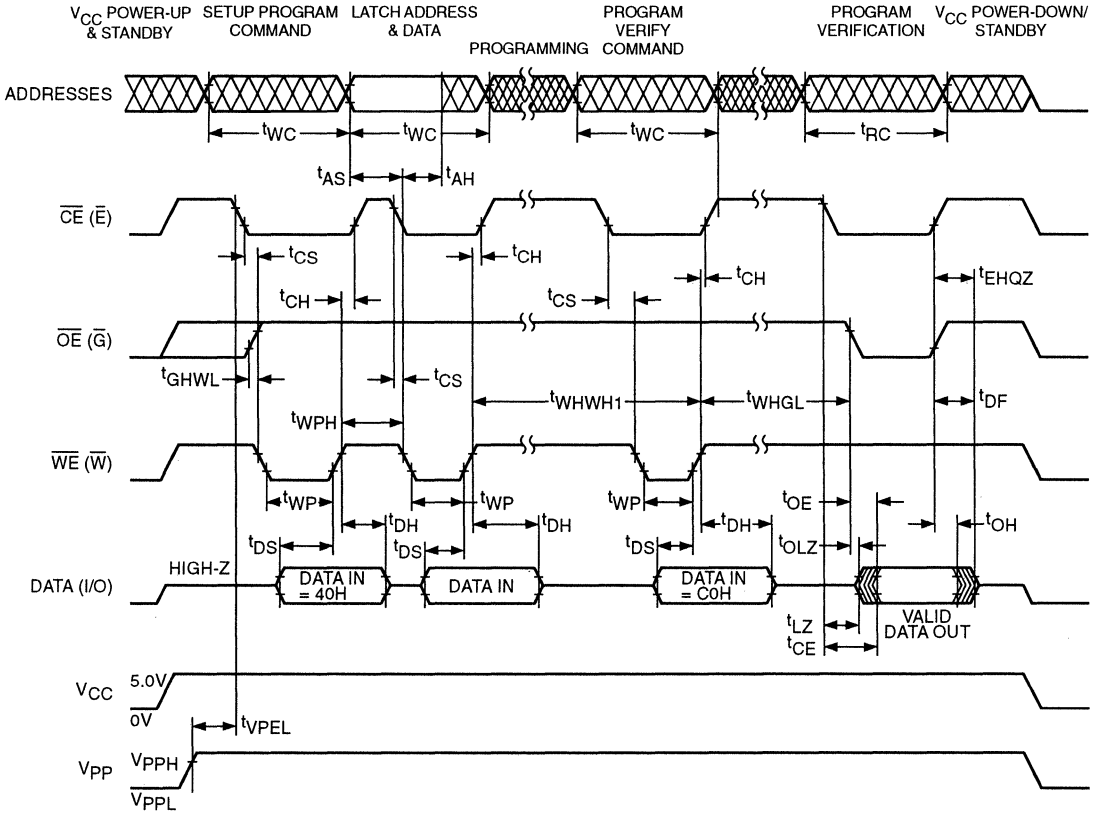
Erase-Verify Mode

The Erase-verify operation is performed on every byte after each erase pulse to verify that the bits have been erased.

Programming Mode

The programming operation is initiated using the programming algorithm of Figure 7. During the first write cycle, the command 40H is written into the command register. During the second write cycle, the address of the memory location to be programmed is latched on the falling edge of $\overline{WE}$, while the data is latched on the rising edge of $\overline{WE}$. The program operation terminates with the next rising edge of $\overline{WE}$. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum program timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Figure 6. A.C. Timing for Programming Operation



5108 FHD F07

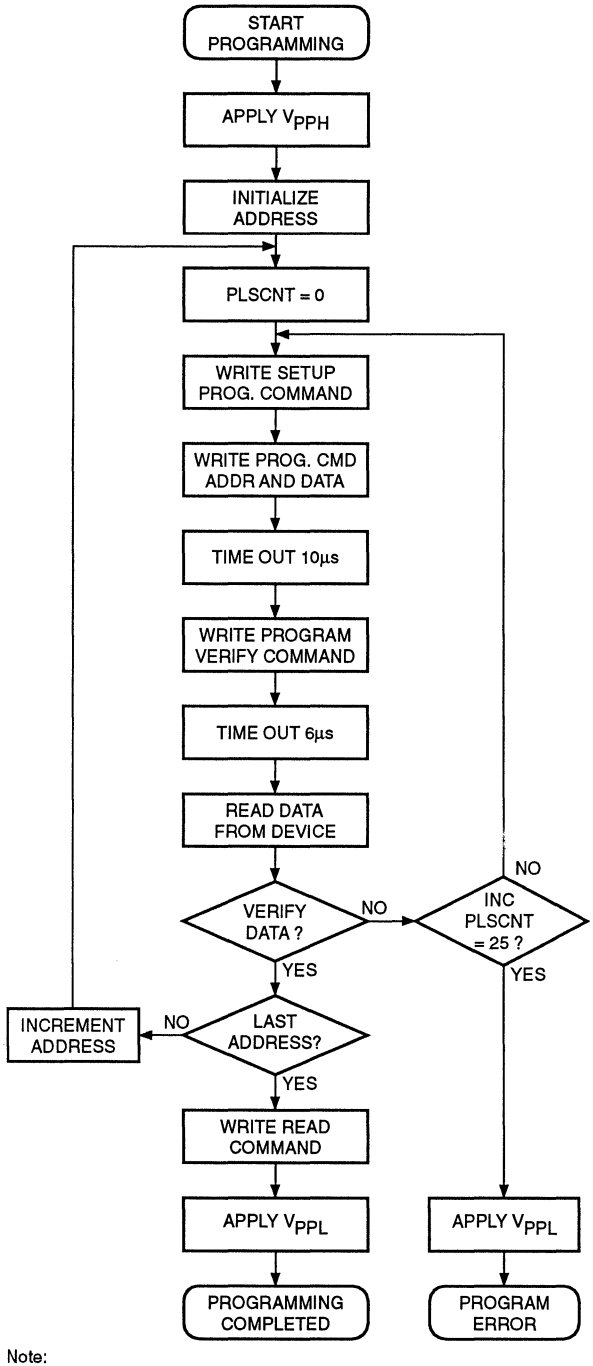
Program-Verify Mode

A Program-verify cycle is performed to ensure that all bits have been correctly programmed following each byte programming operation. The specific address is already latched from the write cycle just completed, and stays latched until the verify is completed. The Program-verify operation is initiated by writing C0H into the command register. An internal reference generates the necessary high voltages so that the user does not need to modify V_{CC}. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

TIMING PARAMETER SYMBOLS

Standard	JEDEC	Standard	JEDEC
t_{AS}	t_{AVWL}	t_{LZ}	t_{ELQX}
t_{AH}	t_{WLAX}	t_{OE}	t_{GLQV}
t_{CE}	t_{ELQV}	t_{OLZ}	t_{GLQX}
t_{CH}	t_{WHEH}	t_{RC}	t_{AVAV}
t_{CS}	t_{ELWL}	t_{WC}	t_{AVAV}
t_{DF}	t_{GHQZ}	t_{WP}	t_{WLWH}
t_{DH}	t_{WHDX}	t_{WPH}	t_{WHWL}
t_{DS}	t_{DVWH}		

Figure 7. Programming Algorithm(16)



BUS OPERATION	COMMAND	COMMENTS
STANDBY		V_{PP} RAMPS TO V_{PPH} (OR V_{PP} HARDWIRED)
		INITIALIZE ADDRESS
		INITIALIZE PULSE COUNT PLSCNT = PULSE COUNT
1ST WRITE CYCLE	WRITE SETUP	DATA = 40H
2ND WRITE CYCLE	PROGRAM	VALID ADDRESS AND DATA
		WAIT
1ST WRITE CYCLE	PROGRAM VERIFY	DATA = C0H
		WAIT
READ		READ BYTE TO VERIFY PROGRAMMING
STANDBY		COMPARE DATA OUTPUT TO DATA EXPECTED
1ST WRITE CYCLE	READ	DATA = 00H SETS THE REGISTER FOR READ OPERATION
STANDBY		V_{PP} RAMPS TO V_{PPL} (OR V_{PP} HARDWIRED)

Note:
(16) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

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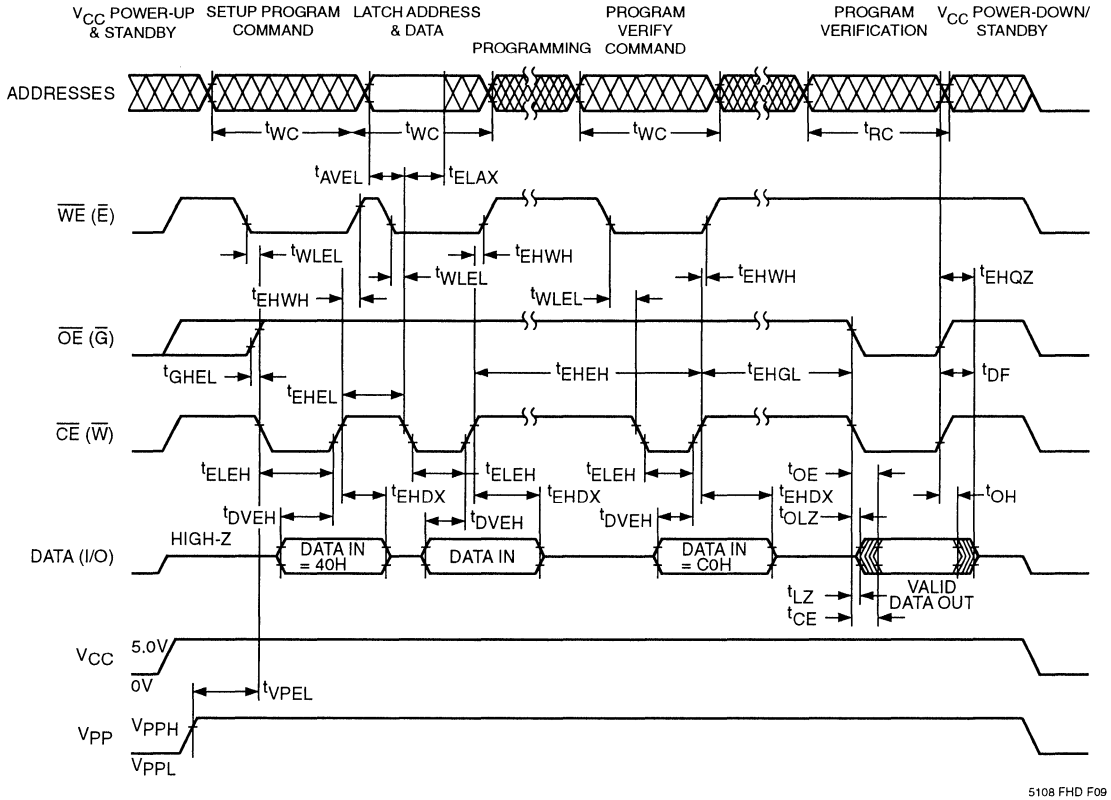
Abort/Reset

An Abort/Reset command is available to allow the user to safely abort an erase or program sequence. Two consecutive program cycles with FFH on the data bus will abort an erase or a program operation. The abort/reset operation can interrupt at any time in a program or erase operation and the device is reset to the Read Mode.

Figure 8. Alternate A.C. Timing for Program Operation



POWER UP/DOWN PROTECTION

The CAT28F512/CAT28F512I offers protection against inadvertent programming during V_{PP} and V_{CC} power transitions. When powering up the device there is no power-on sequencing necessary. In other words, V_{PP} and V_{CC} may power up in any order. Additionally V_{PP} may be hardwired to V_{PPH} independent of the state of V_{CC} and any power up/down cycling. The internal command register of the CAT28F512/CAT28F512I is reset to the Read Mode on power up.

POWER SUPPLY DECOUPLING

To reduce the effect of transient power supply voltage spikes, it is good practice to use a 0.1µF ceramic capacitor between V_{CC} and V_{SS} and V_{PP} and V_{SS}. These high-frequency capacitors should be placed as close as possible to the device for optimum decoupling.

TIMING PARAMETER SYMBOLS

Standard	JEDEC
t_{WC}	t_{AVAV}
t_{OLZ}	t_{GLQX}
t_{LZ}	t_{ELQX}
t_{CE}	t_{ELQV}
t_{DE}	t_{ELQV}
t_{DF}	t_{GHQZ}

ALTERNATE $\overline{CE}$-CONTROLLED WRITES

Symbol	Parameter	28F512-12 28F512I-12		28F512-15 28F512I-15		28F512-20 28F512I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	Write Cycle Time	120		150		200		ns
t_{AVEL}	Address Setup Time	0		0		0		ns
t_{ELAX}	Address Hold Time	80		80		95		ns
t_{DVEH}	Data Setup Time	50		50		50		ns
t_{EHDX}	Data Hold Time	10		10		10		ns
t_{EHGL}	Write Recovery Time Before Read	6		6		6		µs
t_{GHEL}	Read Recovery Time Before Write	0		0		0		µs
t_{WLEL}	$\overline{WE}$ Setup Time Before $\overline{CE}$	0		0		0		ns
t_{EHWH}	Write Enable Hold Time	0		0		0		ns
t_{ELEH}	Write Pulse Width	70		70		80		ns
t_{EHEL}	Write Pulse Width High	20		20		20		ns
t_{VPEL}	V_{PP} Setup Time to $\overline{CE}$ Low	1.0		1.0		1.0		µs

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CAT28F512V5/CAT28F512V5I

512K-Bit CMOS FLASH MEMORY

FEATURES

- Fast Read Access Time: 120/150/200 ns
- Low Power CMOS Dissipation:
  - –Active: 120 mA max (CMOS/TTL levels)
  - –Standby: 1 mA max (TTL levels)
  - –Standby: 100 μA max (CMOS levels)
- High Speed Programming:
  - –10 μS per byte
  - –2 Sec Typ Chip Program
- 5V ± 10% Programming and Erase Voltage
- Stop Timer for Program/Erase
- On-Chip Address and Data Latches
- JEDEC Standard Pinouts:
  - –32 pin DIP
  - –32 pin PLCC
  - –32 pin TSOP (8 x 14; 8 x 20)
- 10,000 Program/Erase Cycles
- 10 Year Data Retention
- Electronic Signature

DESCRIPTION

The CAT28F512V5/CAT28F512V5I is a high speed 64K x 8 bit electrically erasable and reprogrammable Flash memory ideally suited for applications requiring in-system or after-sale code updates. A single 5 volt supply handles all electrical chip erasure and programming. The memory is divided into 32 sectors of 2K bytes each.

The CAT28F512V5/CAT28F512V5I features Random Access Sector Erase by which the user can selectively erase any one of the 32 2K byte sectors. This enhances system performance since the need to erase the entire memory array is eliminated.

It is pin and Read timing compatible with standard EPROM and E²PROM devices. Programming and Erase are performed through an operation and verify algorithm. The instructions are input via the I/O bus, using a two write cycle scheme. Address and Data are latched to free the I/O bus and address bus during the write operation.

The CAT28F512V5/CAT28F512V5I is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 32 pin plastic DIP, 32 pin PLCC or 32 pin TSOP packages.

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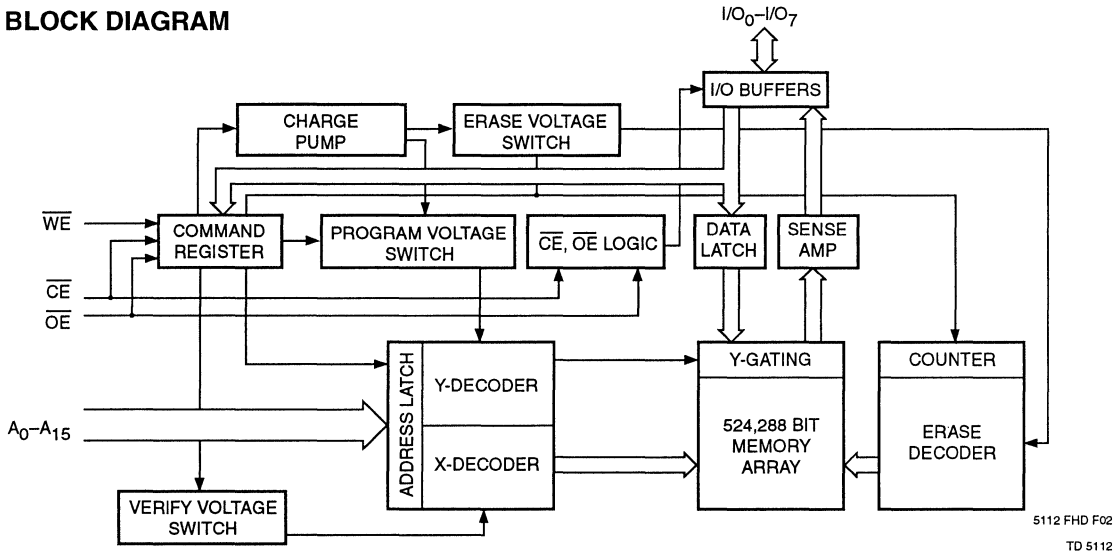
BLOCK DIAGRAM

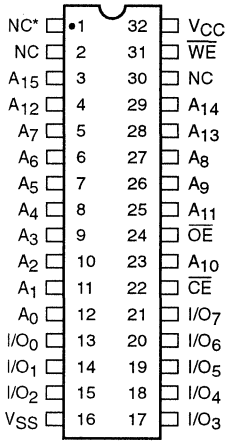


5112 FHD F02

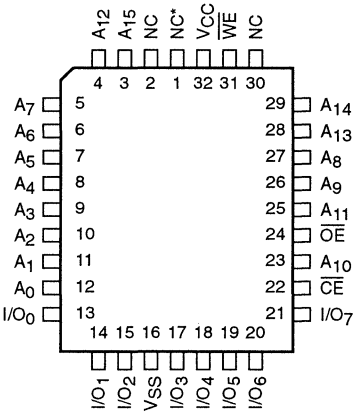
TD 5112

PIN CONFIGURATION

DIP Package



PLCC Package

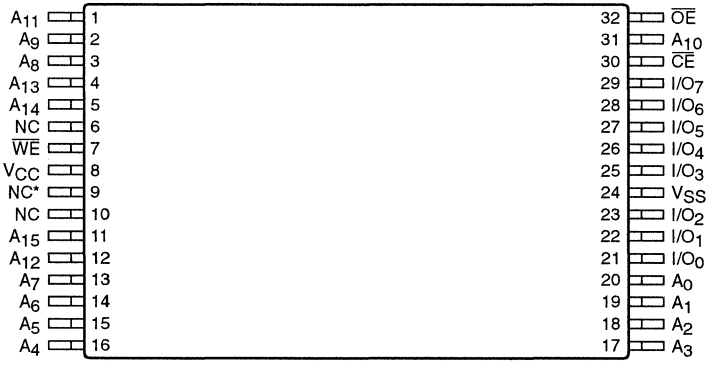


5112 FHD F01

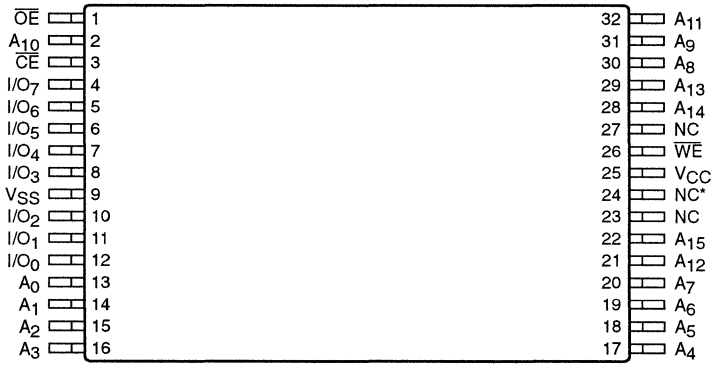
PIN FUNCTIONS

Pin Name	Type	Function
A_0–A_{15}	Input	Address Inputs for memory addressing
I/O_0–I/O_7	I/O	Data Input/Output
$\overline{CE}$	Input	Chip Enable
$\overline{OE}$	Input	Output Enable
$\overline{WE}$	Input	Write Enable
V_{CC}		Voltage Supply
V_{SS}		Ground
NC		No Connect
NC*		Internal connection should be connected to either V_{CC} or V_{SS}

TSOP Package (Standard Pinout)



TSOP Package (Reverse Pinout)



5112 FHD F14

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +95°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V

Voltage on Pin A_9 with Respect to Ground(1) ..... –2.0V to +13.5V

V_{CC} with Respect to Ground(1) ..... –2.0V to +7.0V

Package Power Dissipation Capability (T_A = 25°C) ..... 1.0 W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(3)	Endurance	1K, 10K		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Limits		Units	Conditions
		Min	Max.		
C_{IN}(3)	Input Pin Capacitance		6	pF	V_{IN} = 0V
C_{OUT}(3)	Output Pin Capacitance		10	pF	V_{OUT} = 0V

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Note:
1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
2) Output shorted for no more than one second. No more than one output shorted at a time.
3) This parameter is tested initially and after a design or process change that affects the parameter.
4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

CAT28F512V5 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT28F512V5I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{LI}	Input Leakage Current		±1.0	µA	$V_{IN} = V_{CC}$ or V_{SS} V_{CC} = 5.5V, $\overline{OE} = V_{IH}$
I_{LO}	Output Leakage Current		±10	µA	$V_{OUT} = V_{CC}$ or V_{SS}, V_{CC} = 5.5V, $\overline{OE} = V_{IH}$
I_{SB1}	V_{CC} Standby Current CMOS		100	µA	$\overline{CE} = V_{CC}$ ±0.5V, V_{CC} = 5.5V
I_{SB2}	V_{CC} Standby Current TTL		1.0	mA	$\overline{CE} = V_{IH}$, V_{CC} = 5.5V
I_{CC1}	V_{CC} Active Read/Verify Current		30	mA	V_{CC} = 5.5V, $\overline{CE} = V_{IL}$, I_{OUT} = 0mA, f = 6 MHz
I_{CC2}(3)	V_{CC} Programming Current		120	mA	V_{CC} = 5.5V, Programming in Progress
I_{CC3}(3)	V_{CC} Erase Current		30	mA	V_{CC} = 5.5V, Erasure in Progress
V_{IL}	Input Low Level TTL	–0.5	0.8	V	
V_{ILC}	Input Low Level CMOS	–0.5	0.8	V	
V_{OL}	Output Low Level		0.45	V	I_{OL} = 5.8mA, V_{CC} = 4.5V
V_{IH}	Input High Level TTL	2.0	V_{CC}+0.5	V	
V_{IHC}	Input High Level CMOS	0.7 V_{CC}	V_{CC}+0.5	V	
V_{OH}	Output High Level TTL	2.4		V	I_{OH} = –2.5mA, V_{CC} = 4.5V
V_{OH1}	Output High Level CMOS	0.85 V_{CC}		V	I_{OH} = –2.5mA, V_{CC} = 4.5V
V_{OH2}	Output High Level CMOS	V_{CC}–0.4		V	I_{OH} = –400µA, V_{CC} = 4.5V
V_{ID}	A_9 Signature Voltage	11.4	13.0	V	$A_9 = V_{ID}$
I_{ID}	A_9 Signature Current		200	µA	$A_9 = V_{ID}$
V_{LO}	V_{CC} Erase/Prog. Lockout Voltage	2.5		V	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.

A.C. CHARACTERISTICS, Read Operation

CAT28F512V5 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT28F512V5I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	28F512V5-12 28F512V5I-12		28F512V5-15 28F512V5I-15		28F512V5-20 28F512V5I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	120		150		200		ns
t_{CE}	$\overline{CE}$ Access Time		120		150		200	ns
t_{ACC}	Address Access Time		120		150		200	ns
t_{OE}	$\overline{OE}$ Access Time		50		55		60	ns
t_{OH}	Output Hold from Address $\overline{OE}$/$\overline{CE}$ Change	0		0		0		ns
t_{OLZ}(3)(9)	$\overline{OE}$ to Output in Low-Z	0		0		0		ns
t_{LZ}(3)(9)	$\overline{CE}$ to Output in Low-Z	0		0		0		ns
t_{DF}(3)(5)	$\overline{OE}$ High to Output High-Z		30		35		40	ns
t_{EHQZ}(3)(5)	$\overline{CE}$ High to Output High-Z		55		55		55	ns
t_{WHGL}(3)	Write Recovery Time Before Read	6		6		6		µs

Figure 1. A.C. Testing Input/Output Waveform(6)(7)(8)

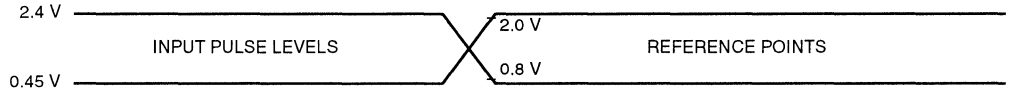
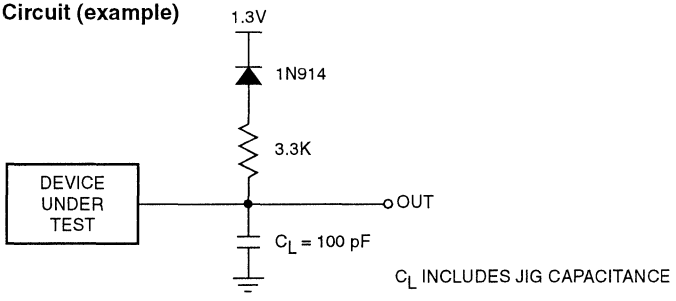


Figure 2. A.C. Testing Load Circuit (example)



Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(5) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
(6) Input Rise and Fall Times (10% to 90%) < 10 ns.
(7) Input Pulse Levels = 0.45V and 2.4V.
(8) Input and Output Timing Reference = 0.8V and 2.0V.
(9) Low-Z is defined as the state where the external data may be driven by the output buffer but may not be valid.

A.C. CHARACTERISTICS, Program/Erase Operation

CAT28F512V5 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT28F512V5I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	28F512V5-12 28F512V5I-12		28F512V5-15 28F512V5I-15		28F512V5-20 28F512V5I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	120		150		200		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	60		60		75		ns
t_{DS}	Data Setup Time	50		50		50		ns
t_{DH}	Data Hold Time	10		10		10		ns
t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{WP}	$\overline{WE}$ Pulse Width	60		60		60		ns
t_{WPH}	$\overline{WE}$ High Pulse Width	20		20		20		ns
t_{WPWH1}(11)	Program Pulse Width	10		10		10		µs
t_{WPWH2}(11)	Erase Pulse Width	9.5		9.5		9.5		ms
t_{WPGL}	Write Recovery Time Before Read	6		6		6		µs
t_{GHWL}	Read Recovery Time Before Write	0		0		0		µs

ERASE AND PROGRAMMING PERFORMANCE

Parameter	28F512V5-12 28F512V5I-12			28F512V5-15 28F512V5I-15			28F512V5-20 28F512V5I-20			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Erase Time(11)(13)		10	320		10	320		15	320	sec
Chip Program Time(11)(12)		2	10		2	10		2	10	sec
Sector Erase Time(11)(13)		0.3	10		0.3	10		0.5	10	sec

Note:
(10) Program and Erase operations are controlled by internal stop timers.
(11) 'Typicals' are not guaranteed, but based on characterization data. Data taken at 25°C.
(12) Minimum byte programming time (excluding system overhead) is 16 µs (10 µs program + 6 µs write recovery), while maximum is 400 µs/byte (16 µs x 25 loops). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
(13) Excludes 00H Programming prior to Erasure.

UNCTION TABLE(14)

Mode	Pins				Notes
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	
ReadV_{IL}	V_{IL}	V_{IH}	D_{OUT}		
Output Disable	V_{IL}	V_{IH}	V_{IH}	High-Z	
Standby	V_{IH}	X	X	High-Z	
Signature (MFG)	V_{IL}	V_{IL}	V_{IH}	31H	$A_0 = V_{IL}$, $A_9 = 12V$
Signature (Device)	V_{IL}	V_{IL}	V_{IH}	B8H	$A_0 = V_{IL}$, $A_9 = 12V$
Program/Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	See Command Table
Write Cycle	V_{IL}	V_{IH}	V_{IL}	D_{IN}	During Write Cycle
Read Cycle	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	During Write Cycle

VRITE COMMAND TABLE

Mode	Pins						
	First Bus Cycle			Second Bus Cycle			
	Operation	Address	D_{IN}	Operation	Address	D_{IN}	D_{OUT}
Set Read	Write	X	00H	Read	Any		D_{OUT}
Read Sig. (MFG)	Write	X	90H	Read	00		31H
Read Sig. (Device)	Write	X	90H	Read	01		B8H
Random Sector Erase	Write	X	60H	Write	Sector Addr	60H	
Sequential Sector Erase	Write	X	20H	Write	X	20H	
Erase Verify	Write	X	A0H	Read	X		D_{OUT}
Program	Write	X	40H	Write	A_{IN}	D_{IN}	
Program Verify	Write	X	C0H	Read	X		D_{OUT}
Reset	Write	X	FFH	Write	X	FFH	

lote:
14) Logic Levels: X = Logic 'Do not care' (V_{IH}, V_{IL})

READ OPERATIONS

Read Mode

A Read operation is performed with both $\overline{CE}$ and $\overline{OE}$ low and with $\overline{WE}$ high. V_{PP} can be either high or low, however, if V_{PP} is high, the Set READ command has to be sent before reading data (see Write Operations). The data retrieved from the I/O pins reflects the contents of the memory location corresponding to the state of the 16 address pins. The respective timing waveforms for the read operation are shown in Figure 3. Refer to the AC Read characteristics for specific timing parameters.

Signature Mode

The signature mode allows the user to identify the IC manufacturer and the type of device while the device resides in the target system. This mode can be activated in either of two ways; through the conventional method of applying a high voltage (12V) to address pin A_9 or by sending an instruction to the command register (see Write Operations).

The conventional mode is entered as a regular READ mode by driving the $\overline{CE}$ and $\overline{OE}$ pins low (with $\overline{WE}$ high) and applying the required high voltage on address pin A_9 while all other address lines are held at V_{IL}.

A Read cycle from address 0000H retrieves the binary code for the IC manufacturer on outputs I/O_0 to I/O_7:

CATALYST Code = 00110001 (31H)

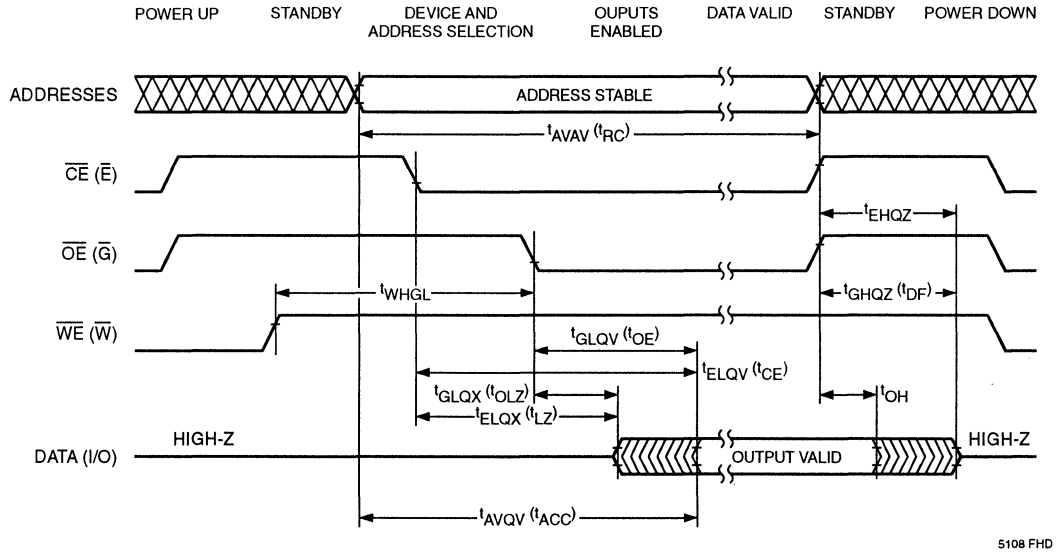
A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F512V5/28F512V5I Code = 1011 1000 (B8H)

Standby Mode

With $\overline{CE}$ at a logic-high level, the CAT28F512V5/ CAT28F512V5I is placed in a standby mode where most of the device circuitry is disabled, thereby substantially reducing power consumption. The outputs are placed in a high-impedance state.

Figure 3. A.C. Timing for Read Operation



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'RITE OPERATIONS

'he following operations are initiated by observing the equence specified in the Write Command Table.

tead Mode

'he device can be put into a standard READ mode by iitiating a write cycle with 00H on the data bus. The ubsequent read cycles will be performed similar to a tandard EPROM or E^2PROM Read.

Signature Mode

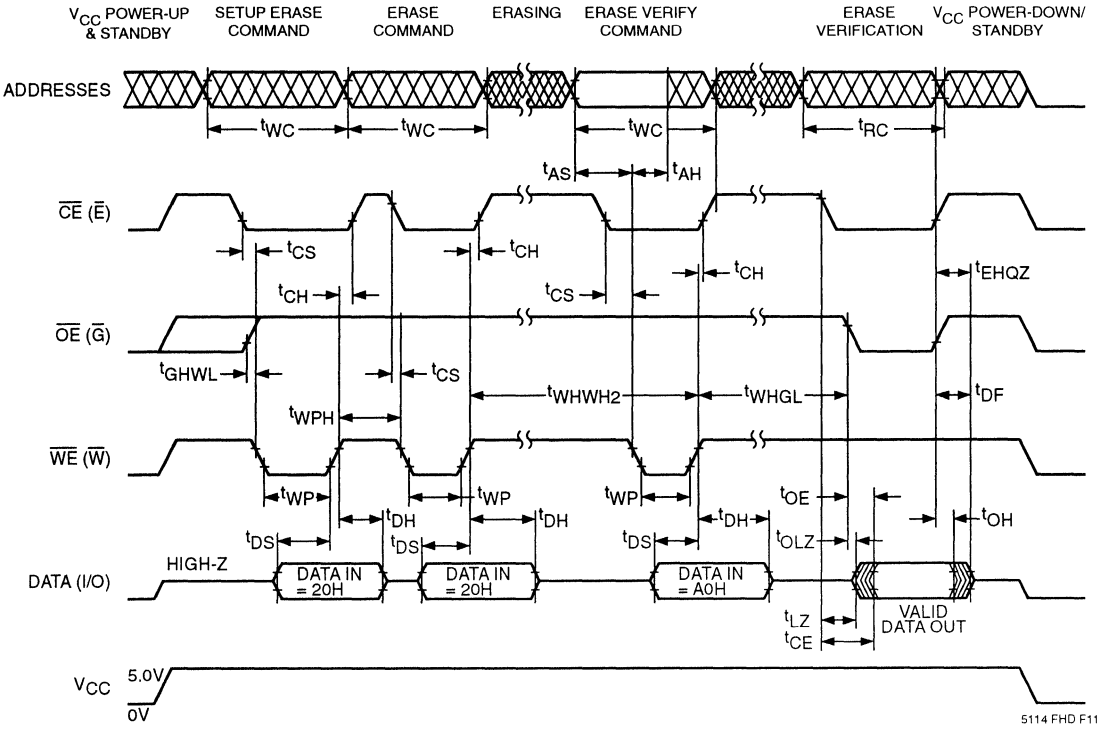
An alternative method for reading device signature (see Read Operations Signature Mode), is initiated by writing the code 90H into the command register while keeping V_{PP} high. A read cycle from address 0000H with $\overline{CE}$ and $\overline{OE}$ low (and $\overline{WE}$ high) will output the device signature.

CATALYST Code = 00110001 (31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F512V5/28F512V5I Code = 1011 1000 (B8H)

'igure 4. A.C. Timing for Erase Operation



Erase Modes

The CAT28F512V5/CAT28F512V5I is organized as 32 sectors of 2K bytes each. The user can erase the entire memory contents (chip erase using Sequential Sector erase) by following the erase algorithm shown in Figure 6. Alternatively, the user can randomly erase any one of the 32 sectors using the Random Access Sector erase algorithm shown in Figure 5. The erase process is accomplished by first programming all bytes to "00" and then erasing all bytes to the "FF" state. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum erase timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

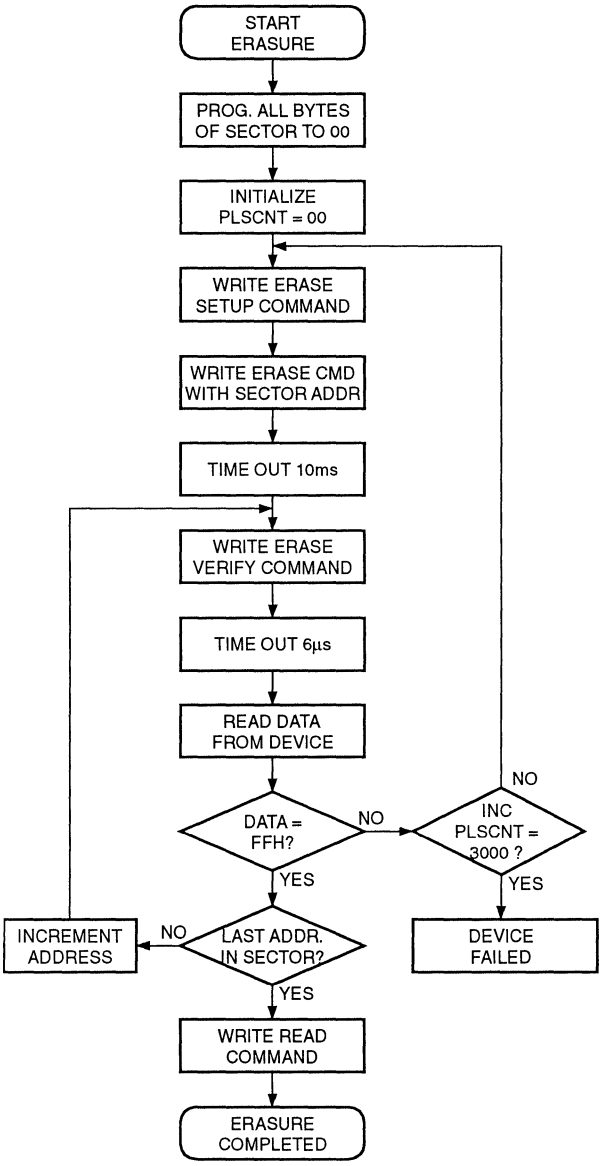
Random Access Sector Erase

The CAT28F512V5/CAT28F512V5I features a random access sector erase where an individual sector (2K bytes) can be erased independent of the other sectors (see Figure 5). To erase a sector, a write command with data 60H is first sent to the device (it is assumed that all locations within the sector have first been written to 00H). A second write command (with data = 60H) along with the beginning address of the sector to be erased is sent next (address bits A11–A15 define the sector). Finally, after sending an erase-verify command, the device will erase the specified 2K byte sector. The Random Access Sector Erase feature minimizes the chance of inadvertently erasing data from sectors that contain boot code or critical data.

TIMING PARAMETER SYMBOLS

Standard	JEDEC	Standard	JEDEC
t_{AS}	t_{AVWL}	t_{LZ}	t_{ELQX}
t_{AH}	t_{WLAX}	t_{OE}	t_{GLQV}
t_{CE}	t_{ELQV}	t_{OLZ}	t_{GLQX}
t_{CH}	t_{WHEH}	t_{RC}	t_{AVAV}
t_{CS}	t_{ELWL}	t_{WC}	t_{AVAV}
t_{DF}	t_{GHQZ}	t_{WP}	t_{WLWH}
t_{DH}	t_{WHDX}	t_{WPH}	t_{WHWL}
t_{DS}	t_{DVWH}		

Figure 5. Random Access Sector Erase Algorithm(15)



BUS OPERATION	COMMAND	COMMENTS
		ALL BYTES WITHIN SECTOR SHOULD BE PROGRAMMED TO 00 BEFORE AN ERASE OPERATION
		PLSCNT = PULSE COUNT
WRITE	ERASE	ACTUAL ERASE NEEDS 10ms PULSE, DATA = 60H
WRITE	ERASE	DATA = 60H ADDRESS = SECTOR ADDR
		WAIT
WRITE	ERASE VERIFY	ADDR = BYTE TO VERIFY DATA = A0H
		WAIT
READ		READ BYTE TO VERIFY ERASURE
STANDBY		COMPARE OUTPUT TO FF INC PULSE COUNT
WRITE	READ	DATA = 00H, RESETS REGISTERS FOR READ OPERATION
STANDBY		

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Note:
(15) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

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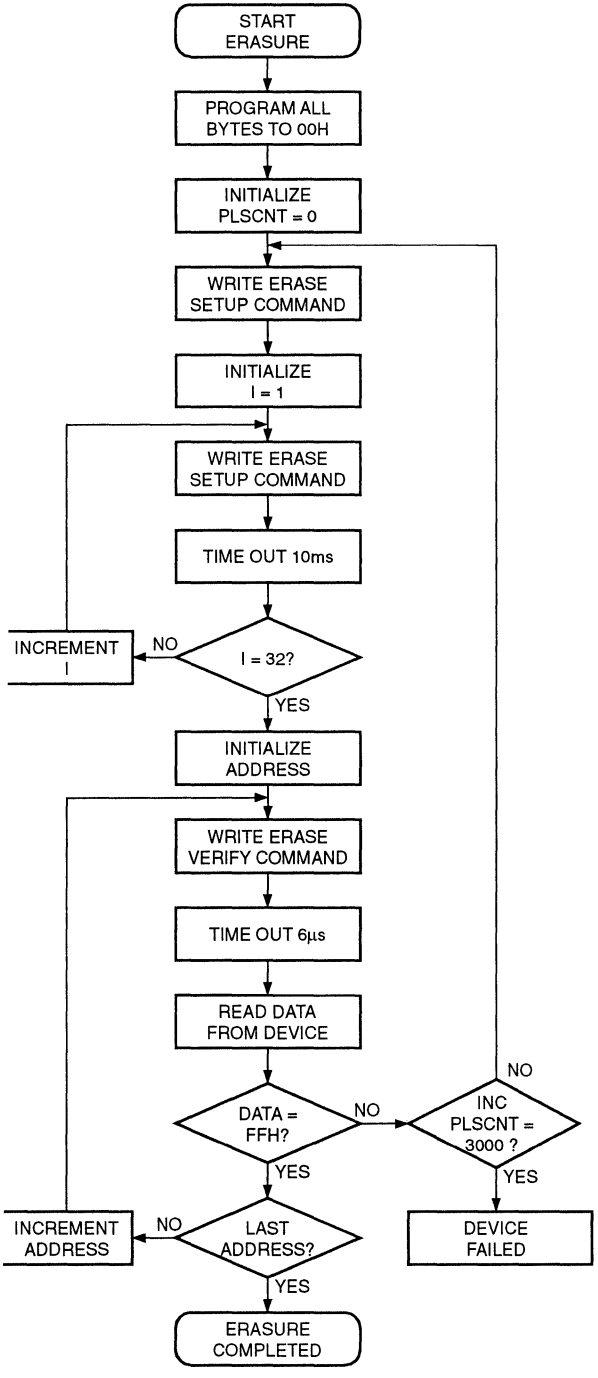
Sequential Sector Erase

During the first Write operation, the command 20H is written into the command register. In order to commence the erase operation, the identical command of 20H has to be written again into the register. This two step process ensures against accidental erasure of the memory contents. The erase cycle is repeated 32 times to erase each of the 32 internal memory blocks sequen tially. The final erase operation will be stopped at th rising edge of $\overline{WE}$, at which time the Erase Verif command (A0H) is sent to the command register. Durin this time, the address to be verified is sent to the addres bus and latched when $\overline{WE}$ goes high.

igure 6. Chip Erase Algorithm (using Sequential Sector Erase)(15)



BUS OPERATION	COMMAND	COMMENTS
		ALL BYTES SHALL BE PROGRAMMED TO 00 BEFORE AN ERASE OPERATION
		PLSCNT = PULSE COUNT
WRITE	ERASE	ACTUAL ERASE NEEDS 10ms PULSE, DATA = 20H
		I = SECTOR INCREMENT COUNTER
WRITE	ERASE	DATA = 20H
		WAIT
		32 ERASE COMMANDS ARE NECESSARY TO ERASE ALL SECTORS
WRITE	ERASE VERIFY	ADDR = BYTE TO VERIFY DATA = A0H
		WAIT
READ		READ BYTE TO VERIFY ERASURE
STANDBY		COMPARE OUTPUT TO FF INCR PULSE COUNT

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Note:
(15) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

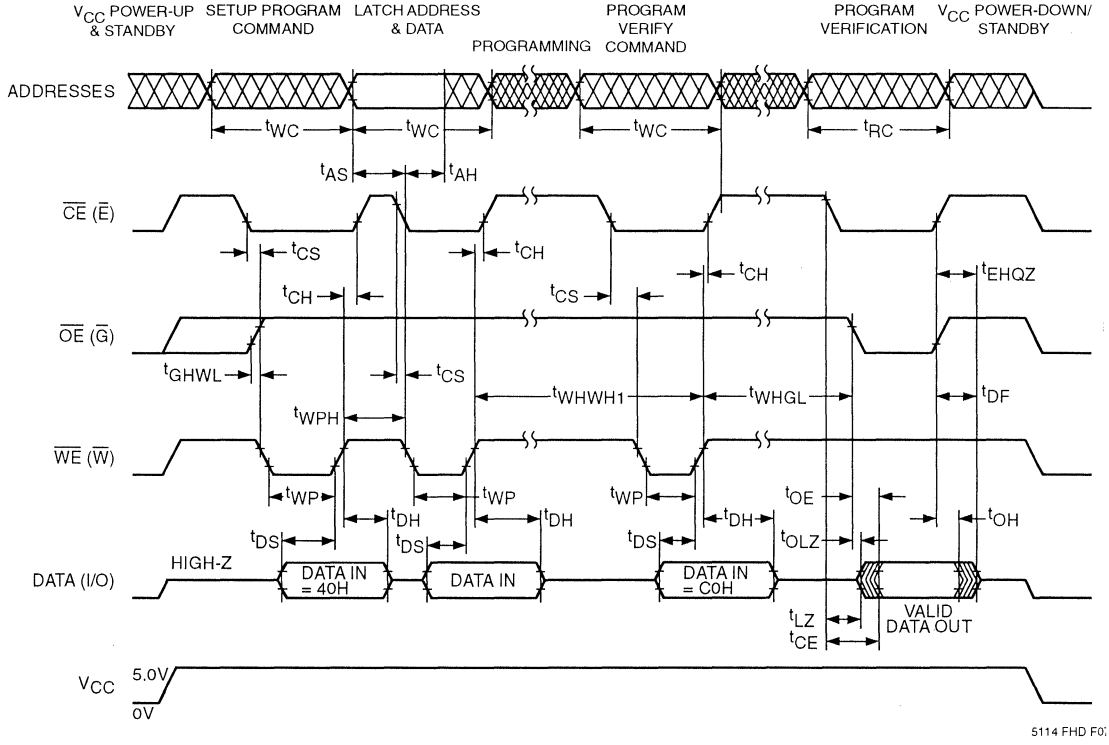
ERASE-VERIFY MODE

The Erase-verify operation is performed on every byte after each erase pulse to verify that the bits have been erased.

Programming Mode

The programming operation is initiated using the programming algorithm of Figure 7. During the first write cycle, the command 40H is written into the command register. During the second write cycle, the address c the memory location to be programmed is latched on th falling edge of $\overline{WE}$, while the data is latched on the risin edge of $\overline{WE}$. The program operation terminates with th next rising edge of $\overline{WE}$. An integrated stop timer allow for automatic timing control over this operation, eliminat ing the need for a maximum program timing specifica tion. Refer to AC Characteristics (Program/Erase) fo specific timing parameters.

Figure 7. A.C. Timing for Programming Operation



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'rogram-Verify Mode

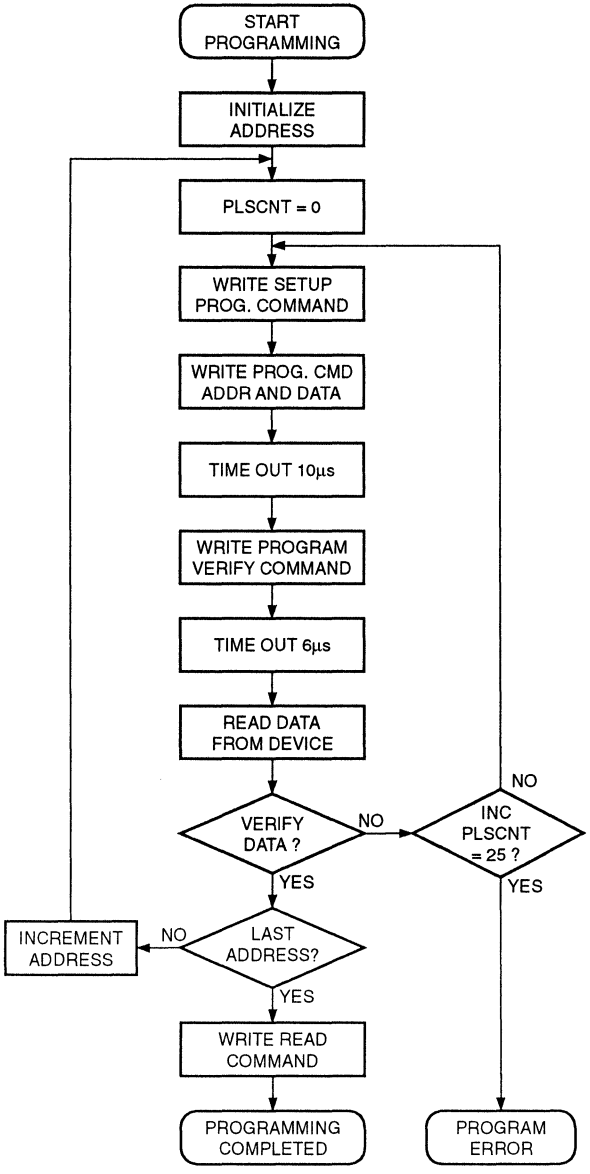
, Program-verify cycle is performed to ensure that all its have been correctly programmed following each yte programming operation. The specific address is lready latched from the write cycle just completed, and tays latched until the verify is completed. The Program-verify operation is initiated by writing C0H into the command register. An internal reference generates the necessary high voltages so that the user does not need to modify V_{CC}. Refer to AC Characteristics (Program/ Erase) for specific timing parameters.

'IMING PARAMETER SYMBOLS

Standard	JEDEC	Standard	JEDEC
t_{AS}	t_{AVWL}	t_{LZ}	t_{ELQX}
t_{AH}	t_{WLAX}	t_{OE}	t_{GLQV}
t_{CE}	t_{ELQV}	t_{OLZ}	t_{GLQX}
t_{CH}	t_{WHEH}	t_{RC}	t_{AVAV}
t_{CS}	t_{ELWL}	t_{WC}	t_{AVAV}
t_{DF}	t_{GHQZ}	t_{WP}	t_{WLWH}
t_{DH}	t_{WHDX}	t_{WPH}	t_{WHWL}
t_{DS}	t_{DVWH}		

8

Figure 8. Programming Algorithm(15)



BUS OPERATION	COMMAND	COMMENTS
		INITIALIZE ADDRESS
		INITIALIZE PULSE COUNT PLSCNT = PULSE COUNT
1ST WRITE CYCLE	WRITE SETUP	DATA = 40H
2ND WRITE CYCLE	PROGRAM	VALID ADDRESS AND DATA
		WAIT
1ST WRITE CYCLE	PROGRAM VERIFY	DATA = C0H
		WAIT
READ		READ BYTE TO VERIFY PROGRAMMING
STANDBY		COMPARE DATA OUTPUT TO DATA EXPECTED
1ST WRITE CYCLE	READ	DATA = 00H SETS THE REGISTER FOR READ OPERATION

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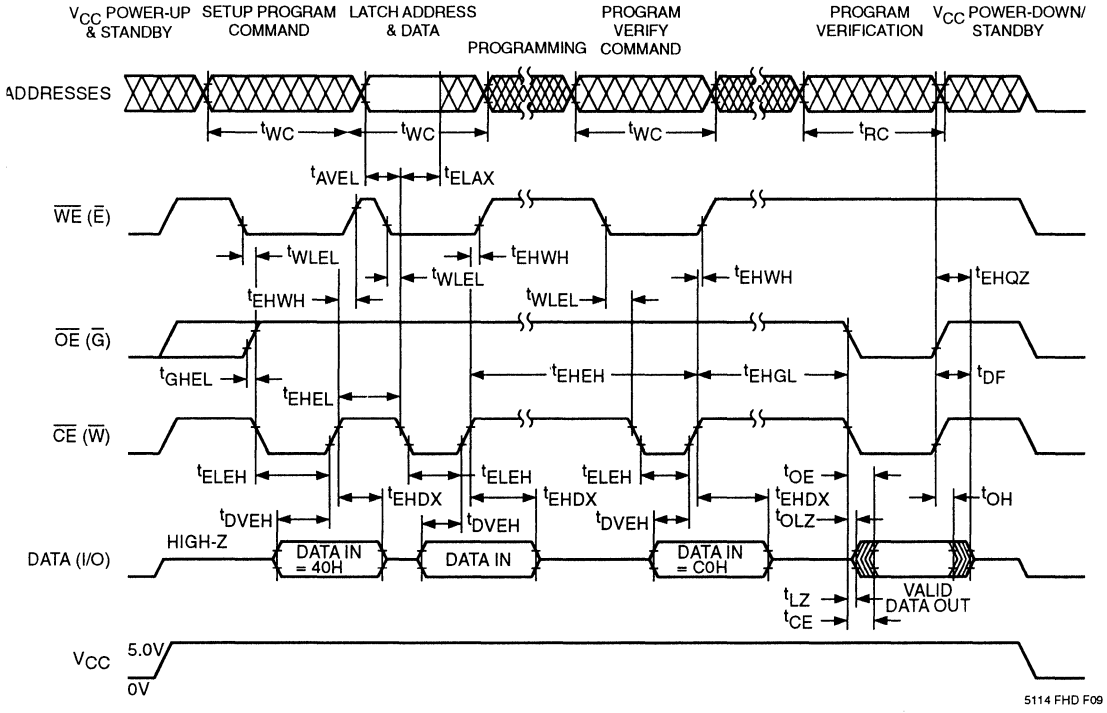
Note:
(15) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

Abort/Reset

An Abort/Reset command is available to allow the user to safely abort an erase or program sequence. Two consecutive program operations with FFH on the data bus will abort an erase or a program operation. The Abort/Reset operation also resets the sector pointer in the sequential sector erase mode. The Abort/Reset operation can interrupt at any time in a program or erase operation, and the device is reset to the Read mode. If an Abort/Reset command is sent prior to completion of an erase or program sequence, a partial erase or program may occur. If a program operation is aborted by the Reset command, the byte in progress can later be programmed. If an erase operation is aborted by the reset command, the erase operation can be continued after the abort.

Figure 9. Alternate A.C. Timing for Program Operation



POWER SUPPLY DECOUPLING

To reduce the effect of transient power supply voltage spikes, it is good practice to use a 0.1µF ceramic capacitor between V_{CC} and V_{SS}. These high-frequency capacitors should be placed as close as possible to the device for optimum decoupling.

It is recommended after a power up to issue an Abor Reset command when operating in particularly nois environments. No power supply sequencing is required

TIMING PARAMETER SYMBOLS

Standard	JEDEC
t_{WC}	t_{AVAV}
t_{OLZ}	t_{GLQX}
t_{LZ}	t_{ELQX}
t_{CE}	t_{ELQV}
t_{DE}	t_{ELQV}
t_{DF}	t_{GHQZ}

ALTERNATE $\overline{CE}$-CONTROLLED WRITES

Symbol	Parameter	28F512V5-12 28F512V5I-12		28F512V5-15 28F512V5I-15		28F512V5-20 28F512V5I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	Write Cycle Time	120		150		200		ns
t_{AVEL}	Address Setup Time	0		0		0		ns
t_{ELAX}	Address Hold Time	80		80		95		ns
t_{DVEH}	Data Setup Time	50		50		50		ns
t_{EHDX}	Data Hold Time	10		10		10		ns
t_{EHGL}	Write Recovery Time Before Read	6		6		6		µs
t_{GHEL}	Read Recovery Time Before Write	0		0		0		µs
t_{WLEL}	$\overline{WE}$ Setup Time Before $\overline{CE}$	0		0		0		ns
t_{EHWH}	Write Enable Hold Time	0		0		0		ns
t_{ELEH}	Write Pulse Width	70		70		80		ns
t_{EHEL}	Write Pulse Width High	20		20		20		ns

CATALYST SEMICONDUCTOR

CAT28F010/CAT28F010I

Megabit CMOS FLASH MEMORY

FEATURES

- Fast Read Access Time: 120/150/200 ns
- Low Power CMOS Dissipation:
  - –Active: 30 mA max (CMOS/TTL levels)
  - –Standby: 1 mA max (TTL levels)
  - –Standby: 100 µA max (CMOS levels)
- High Speed Programming:
  - –10 µS per byte
  - –2 Sec Typ Chip Program
- 12.0V ± 5% Programming and Erase Voltage
- Stop Timer for Program/Erase
- On-Chip Address and Data Latches
- JEDEC Standard Pinouts:
  - –32 pin DIP
  - –32 pin PLCC
  - –32 pin TSOP (8 x 14; 8 x 20)
- 10,000 Program/Erase Cycles
- 10 Year Data Retention
- Electronic Signature

DESCRIPTION

The CAT28F010/CAT28F010I is a high speed 128K x 8 bit electrically erasable and reprogrammable Flash memory ideally suited for applications requiring in-system or after-sale code updates. Electrical erasure of the full memory contents is achieved typically within 1 second.

It is pin and Read timing compatible with standard EPROM and E²PROM devices. Programming and Erase are performed through an operation and verify algorithm. The instructions are input via the I/O bus, using a two write cycle scheme. Address and Data are latched to free the I/O bus and address bus during the write operation.

The CAT28F010/CAT28F010I is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 32 pin plastic DIP, 32 pin PLCC or 32 pin TSOP packages.

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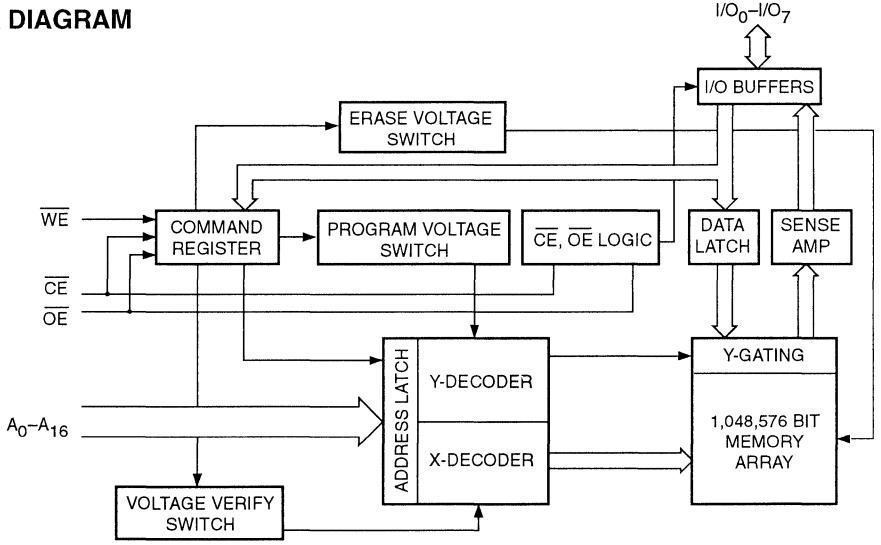
BLOCK DIAGRAM



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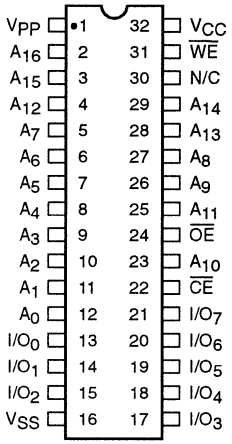
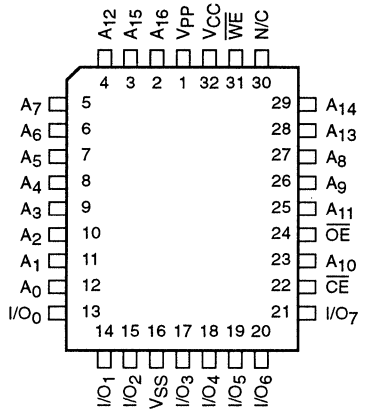
TD 5108

PIN CONFIGURATION

DIP Package



PLCC Package



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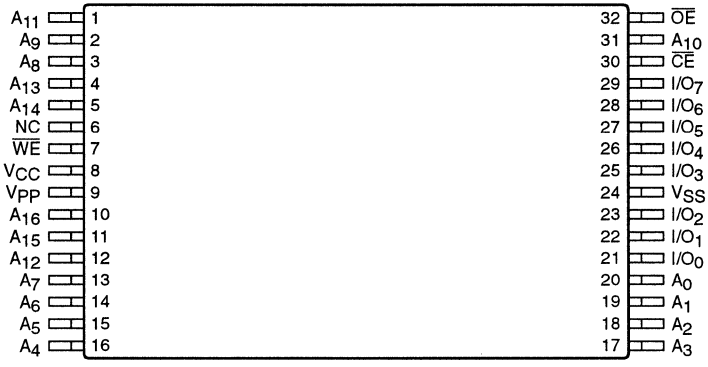
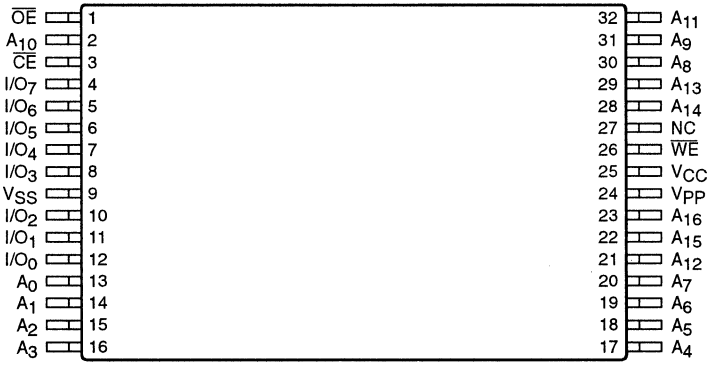
PIN FUNCTIONS

Pin Name	Type	Function
A_0–A_{16}	Input	Address Inputs for memory addressing
I/O_0–I/O_7	I/O	Data Input/Output
$\overline{CE}$	Input	Chip Enable
$\overline{OE}$	Input	Output Enable
$\overline{WE}$	Input	Write Enable
V_{CC}		Voltage Supply
V_{SS}		Ground
V_{PP}		Program/Erase Voltage Supply

TSOP Package (Standard Pinout)



TSOP Package (Reverse Pinout)



5108 FHD F

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +95°C
Storage Temperature ..... –65°C to +150°C
Voltage on Any Pin with
Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V
Voltage on Pin A_9 with
Respect to Ground(1) ..... –2.0V to +13.5V
V_{PP} with Respect to Ground
during Program/Erase(1) ..... –2.0V to +14.0V
V_{CC} with Respect to Ground(1) ..... –2.0V to +7.0V
Package Power Dissipation
Capability (T_A = 25°C) ..... 1.0 W
Lead Soldering Temperature (10 secs) ..... 300°C
Output Short Circuit Current(2) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(3)	Endurance	1K, 10K		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Limits		Units	Conditions
		Min	Max.		
C_{IN}(3)	Input Pin Capacitance		6	pF	V_{IN} = 0V
C_{OUT}(3)	Output Pin Capacitance		10	pF	V_{OUT} = 0V
C_{VPP}(3)	V_{PP} Supply Capacitance		25	pF	V_{PP} = 0V

Note:
1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
2) Output shorted for no more than one second. No more than one output shorted at a time.
3) This parameter is tested initially and after a design or process change that affects the parameter.
4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

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D.C. OPERATING CHARACTERISTICS

CAT28F010 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT28F010I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{LI}	Input Leakage Current		±1.0	µA	$V_{IN} = V_{CC}$ or V_{SS} V_{CC} = 5.5V, $\overline{OE} = V_{IH}$
I_{LO}	Output Leakage Current		±10	µA	$V_{OUT} = V_{CC}$ or V_{SS}, V_{CC} = 5.5V, $\overline{OE} = V_{IH}$
I_{SB1}	V_{CC} Standby Current CMOS		100	µA	$\overline{CE} = V_{CC}$ ±0.5V, V_{CC} = 5.5V
I_{SB2}	V_{CC} Standby Current TTL		1.0	mA	$\overline{CE} = V_{IH}$, V_{CC} = 5.5V
I_{CC1}	V_{CC} Active Read Current		30	mA	V_{CC} = 5.5V, $\overline{CE} = V_{IL}$, I_{OUT} = 0mA, f = 6 MHz
I_{CC2}(3)	V_{CC} Programming Current		15	mA	V_{CC} = 5.5V, Programming in Progress
I_{CC3}(3)	V_{CC} Erase Current		15	mA	V_{CC} = 5.5V, Erasure in Progress
I_{CC4}(3)	V_{CC} Prog./Erase Verify Current		15	mA	$V_{PP} = V_{PPH}$, Program or Erase Verify in Progress
I_{PPS}	V_{PP} Standby Current		±10	µA	$V_{PP} = V_{PPL}$
I_{PP1}	V_{PP} Read Current		200	µA	$V_{PP} = V_{PPH}$
I_{PP2}(3)	V_{PP} Programming Current		30	mA	$V_{PP} = V_{PPH}$, Programming in Progress
I_{PP3}(3)	V_{PP} Erase Current		30	mA	V_{CC} = 5.5V, Erasure in Progress
I_{PP4}(3)	V_{PP} Prog./Erase Verify Current		5.0	mA	$V_{PP} = V_{PPH}$, Program or Erase Verify in Progress
V_{IL}	Input Low Level TTL	–0.5	0.8	V	
V_{ILC}	Input Low Level CMOS	–0.5	0.8	V	
V_{OL}	Output Low Level		0.45	V	I_{OL} = 5.8mA, V_{CC} = 4.5V
V_{IH}	Input High Level TTL	2.0	V_{CC}+0.5	V	
V_{IHC}	Input High Level CMOS	0.7 V_{CC}	V_{CC}+0.5	V	
V_{OH}	Output High Level TTL	2.4		V	I_{OH} = –2.5mA, V_{CC} = 4.5V
V_{OH1}	Output High Level CMOS	0.85 V_{CC}		V	I_{OH} = –2.5mA, V_{CC} = 4.5V
V_{OH2}	Output High Level CMOS	V_{CC}–0.4		V	I_{OH} = –400µA, V_{CC} = 4.5V
V_{ID}	A_9 Signature Voltage	11.4	13.0	V	$A_9 = V_{ID}$
I_{ID}	A_9 Signature Current		200	µA	$A_9 = V_{ID}$
V_{LO}	V_{CC} Erase/Prog. Lockout Voltage	2.5		V	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.

SUPPLY CHARACTERISTICS

Symbol	Parameter	Limits		Unit
		Min	Max.	
V_{CC}	V_{CC} Supply Voltage	4.5	5.5	V
V_{PPL}	V_{PP} During Read Operations	0	6.5	V
V_{PPH}	V_{PP} During Read/Erase/Program	11.4	12.6	V

A.C. CHARACTERISTICS, Read Operation

CAT28F010 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT28F010I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	28F010-12 28F010I-12		28F010-15 28F010I-15		28F010-20 28F010I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	120		150		200		ns
t_{CE}	$\overline{CE}$ Access Time		120		150		200	ns
t_{ACC}	Address Access Time		120		150		200	ns
t_{OE}	$\overline{OE}$ Access Time		50		55		60	ns
t_{OH}	Output Hold from Address $\overline{OE}$/$\overline{CE}$ Change	0		0		0		ns
t_{OLZ}[3][9]	$\overline{OE}$ to Output in Low-Z	0		0		0		ns
t_{LZ}[3][9]	$\overline{CE}$ to Output in Low-Z	0		0		0		ns
t_{DF}[3][5]	$\overline{OE}$ High to Output High-Z		30		35		40	ns
t_{EHQZ}[3][5]	$\overline{CE}$ High to Output High-Z		55		55		55	ns
t_{WHGL}[3]	Write Recovery Time Before Read	6		6		6		µs

Figure 1. A.C. Testing Input/Output Waveform[6][7][8]

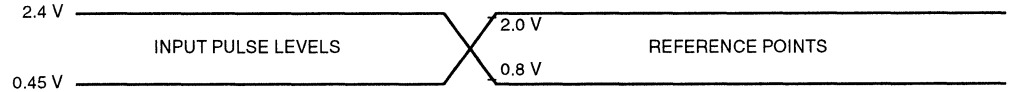
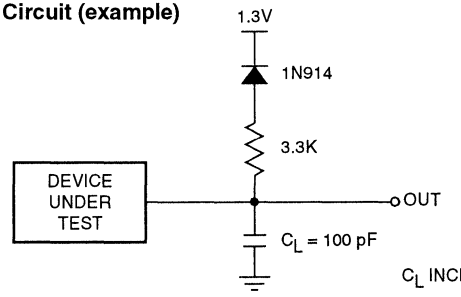


Figure 2. A.C. Testing Load Circuit (example)



Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(5) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
(6) Input Rise and Fall Times (10% to 90%) < 10 ns.
(7) Input Pulse Levels = 0.45V and 2.4V.
(8) Input and Output Timing Reference = 0.8V and 2.0V.
(9) Low-Z is defined as the state where the external data may be driven by the output buffer but may not be valid.

A.C. CHARACTERISTICS, Program/Erase Operation

CAT28F010 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT28F010I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	28F010-12 28F010I-12		28F010-15 28F010I-15		28F010-20 28F010I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	120		150		200		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	60		60		75		ns
t_{DS}	Data Setup Time	50		50		50		ns
t_{DH}	Data Hold Time	10		10		10		ns
t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{WP}	$\overline{WE}$ Pulse Width	60		60		60		ns
t_{WPH}	$\overline{WE}$ High Pulse Width	20		20		20		ns
t_{WPWH1}(11)	Program Pulse Width	10		10		10		µs
t_{WPWH2}(11)	Erase Pulse Width	9.5		9.5		9.5		ms
t_{WPGL}	Write Recovery Time Before Read	6		6		6		µs
t_{GHWL}	Read Recovery Time Before Write	0		0		0		µs
t_{VPEL}	V_{PP} Setup Time to $\overline{CE}$	100		100		100		ns

ERASE AND PROGRAMMING PERFORMANCE(10)

Parameter	28F010-12 28F010I-12			28F010-15 28F010I-15			28F010-20 28F010I-20			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Erase Time(12)(14)		1.0	10		1.0	10		1.0	30	sec
Chip Program Time(12)(13)		2	12.5		2	12.5		2	12.5	sec

Note:
(10) Please refer to Supply characteristics for the value of V_{PPH} and V_{PPL}. The V_{PP} supply can be either hardwired or switched. If V_{PP} is switchec V_{PPL} can be ground, less than V_{CC} + 2.0V or a no connect with a resistor tied to ground.
(11) Program and Erase operations are controlled by internal stop timers.
(12) 'Typicals' are not guaranteed, but based on characterization data. Data taken at 25°C, 12.0V V_{PP}.
(13) Minimum byte programming time (excluding system overhead) is 16 µs (10 µs program + 6 µs write recovery), while maximum is 400 µs/byte (16 µs x 25 loops). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
(14) Excludes 00H Programming prior to Erasure.

FUNCTION TABLE(15)

Mode	Pins					Notes
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	I/O	
Read	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	D_{OUT}	
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	High-Z	
Standby	V_{IH}	X	X	V_{PPL}	High-Z	
Signature (MFG)	V_{IL}	V_{IL}	V_{IH}	X	31H	$A_0 = V_{IL}$, $A_9 = 12V$
Signature (Device)	V_{IL}	V_{IL}	V_{IH}	X	B4H	$A_0 = V_{IL}$, $A_9 = 12V$
Program/Erase	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	D_{IN}	See Command Table
Write Cycle	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	D_{IN}	During Write Cycle
Read Cycle	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	D_{OUT}	During Write Cycle

WRITE COMMAND TABLE

Commands are written into the command register in one or two write cycles. The command register can be altered only when V_{PP} is high and the instruction byte is latched on the rising edge of $\overline{WE}$. Write cycles also internally latch addresses and data required for programming and erase operations.

Mode	Pins						
	First Bus Cycle			Second Bus Cycle			
	Operation	Address	D_{IN}	Operation	Address	D_{IN}	D_{OUT}
Set Read	Write	X	00H	Read	Any		D_{OUT}
Read Sig. (MFG)	Write	X	90H	Read	00		31H
Read Sig. (Device)	Write	X	90H	Read	01		B4H
Erase	Write	X	20H	Write	X	20H	
Erase Verify	Write	X	A0H	Read	X		D_{OUT}
Program	Write	X	40H	Write	A_{IN}	D_{IN}	
Program Verify	Write	X	C0H	Read	X		D_{OUT}
Reset	Write	X	FFH	Write	X	FFH	

Note:
(15) Logic Levels: X = Logic 'Do not care' (V_{IH}, V_{IL}, V_{PPL}, V_{PPH})

READ OPERATIONS

Read Mode

A Read operation is performed with both $\overline{CE}$ and $\overline{OE}$ low and with $\overline{WE}$ high. V_{PP} can be either high or low, however, if V_{PP} is high, the Set READ command has to be sent before reading data (see Write Operations). The data retrieved from the I/O pins reflects the contents of the memory location corresponding to the state of the 17 address pins. The respective timing waveforms for the read operation are shown in Figure 3. Refer to the AC Read characteristics for specific timing parameters.

Signature Mode

The signature mode allows the user to identify the IC manufacturer and the type of device while the device resides in the target system. This mode can be activated in either of two ways; through the conventional method of applying a high voltage (12V) to address pin A_9 or by sending an instruction to the command register (see Write Operations).

The conventional mode is entered as a regular READ mode by driving the $\overline{CE}$ and $\overline{OE}$ pins low (with $\overline{WE}$ high), and applying the required high voltage on address pin A_9 while all other address lines are held at V_{IL}.

A Read cycle from address 0000H retrieves the binary code for the IC manufacturer on outputs I/O_0 to I/O_7:

CATALYST Code = 00110001 (31H)

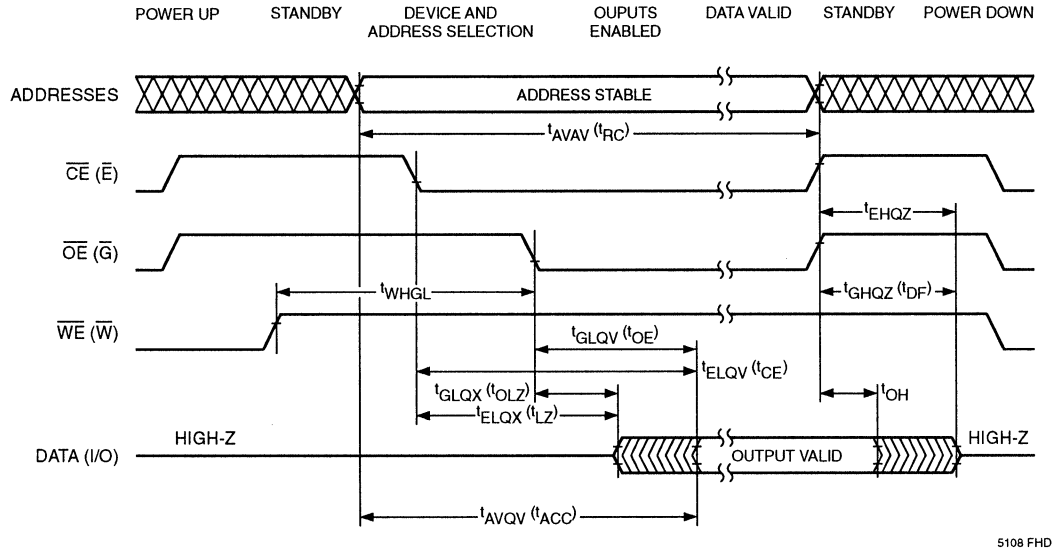
A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F010/28F010I Code = 1011 0100 (B4H)

Standby Mode

With $\overline{CE}$ at a logic-high level, the CAT28F010/ CAT28F010I is placed in a standby mode where most of the device circuitry is disabled, thereby substantially reducing power consumption. The outputs are placed in a high-impedance state.

Figure 3. A.C. Timing for Read Operation



WRITE OPERATIONS

The following operations are initiated by observing the sequence specified in the Write Command Table.

Read Mode

The device can be put into a standard READ mode by initiating a write cycle with 00H on the data bus. The subsequent read cycles will be performed similar to a standard EPROM or E^2PROM Read.

Signature Mode

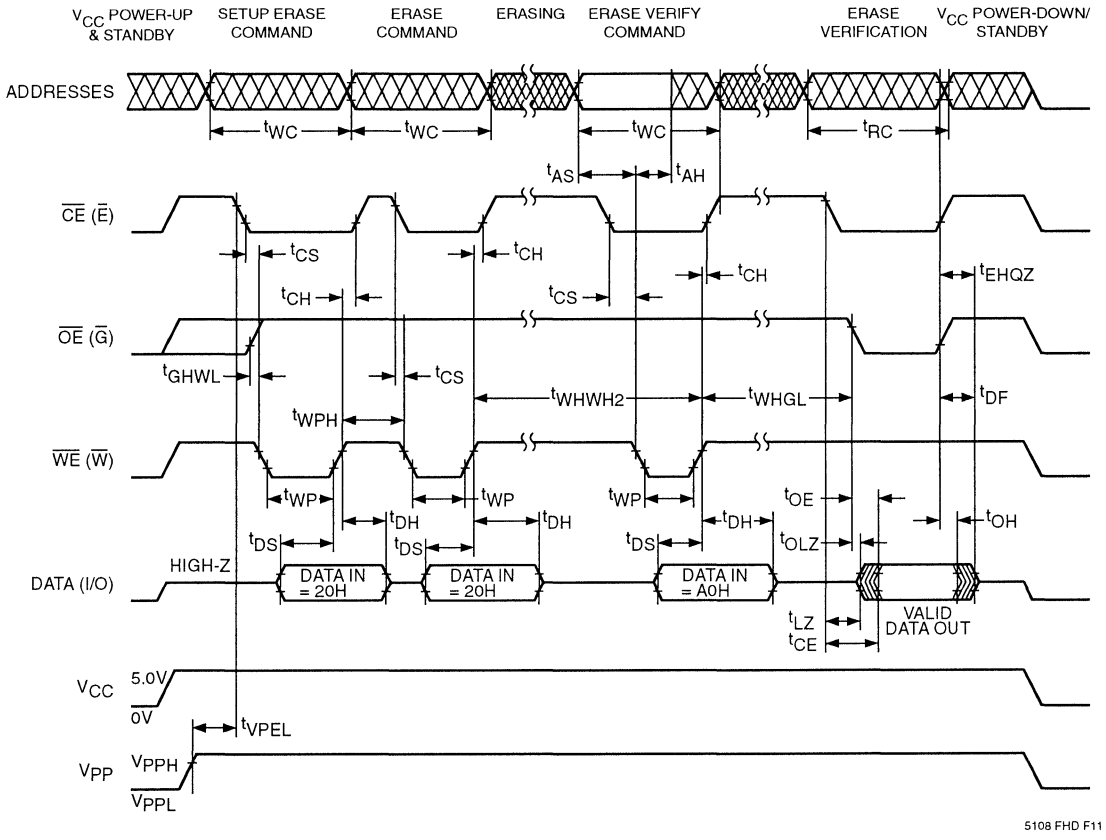
An alternative method for reading device signature (see Read Operations Signature Mode), is initiated by writing the code 90H into the command register while keeping V_{PP} high. A read cycle from address 0000H with $\overline{CE}$ and $\overline{OE}$ low (and $\overline{WE}$ high) will output the device signature.

CATALYST Code = 00110001 (31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F010/28F010I Code = 1011 0100 (B4H)

Figure 4. A.C. Timing for Erase Operation



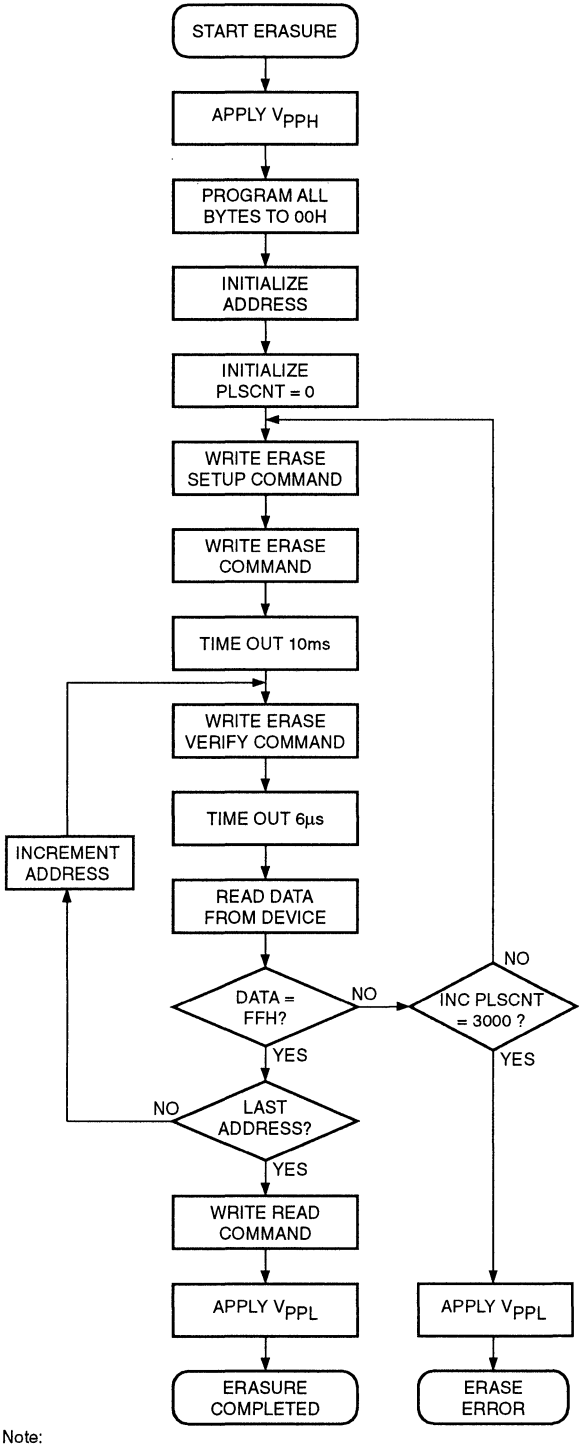
Erase Mode

During the first Write cycle, the command 20H is written into the command register. In order to commence the erase operation, the identical command of 20H has to be written again into the register. This two-step process ensures against accidental erasure of the memory contents. The final erase cycle will be stopped at the rising edge of $\overline{WE}$, at which time the Erase Verify command (A0H) is sent to the command register. During this cycle, the address to be verified is sent to the address bus and latched when $\overline{WE}$ goes high. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum erase timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

TIMING PARAMETER SYMBOLS

Standard	JEDEC	Standard	JEDEC
t_{AS}	t_{AVWL}	t_{LZ}	t_{ELQX}
t_{AH}	t_{WLAX}	t_{OE}	t_{GLQV}
t_{CE}	t_{ELQV}	t_{OLZ}	t_{GLQX}
t_{CH}	t_{WHEH}	t_{RC}	t_{AVAV}
t_{CS}	t_{ELWL}	t_{WC}	t_{AVAV}
t_{DF}	t_{GHQZ}	t_{WP}	t_{WLWH}
t_{DH}	t_{WHDX}	t_{WPH}	t_{WHWL}
t_{DS}	t_{DVWH}		

Figure 5. Chip Erase Algorithm(16)



BUS OPERATION	COMMAND	COMMENTS
		V_{PP} RAMPS TO V_{PPH} (OR V_{PP} HARDWIRED)
STANDBY		ALL BYTES SHALL BE PROGRAMMED TO 00 BEFORE AN ERASE OPERATION
		INITIALIZE ADDRESS
		PLSCNT = PULSE COUNT
WRITE	ERASE	ACTUAL ERASE NEEDS 10ms PULSE, DATA = 20H
WRITE	ERASE	DATA = 20H
		WAIT
WRITE	ERASE VERIFY	ADDRESS = BYTE TO VERIFY DATA = 20H; STOPS ERASE OPERATION
		WAIT
READ		READ BYTE TO VERIFY ERASURE
STANDBY		COMPARE OUTPUT TO FF INCREMENT PULSE COUNT
WRITE	READ	DATA = 00H RESETS THE REGISTER FOR READ OPERATION
STANDBY		V_{PP} RAMPS TO V_{PPL} (OR V_{PP} HARDWIRED)

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Note:
(16) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

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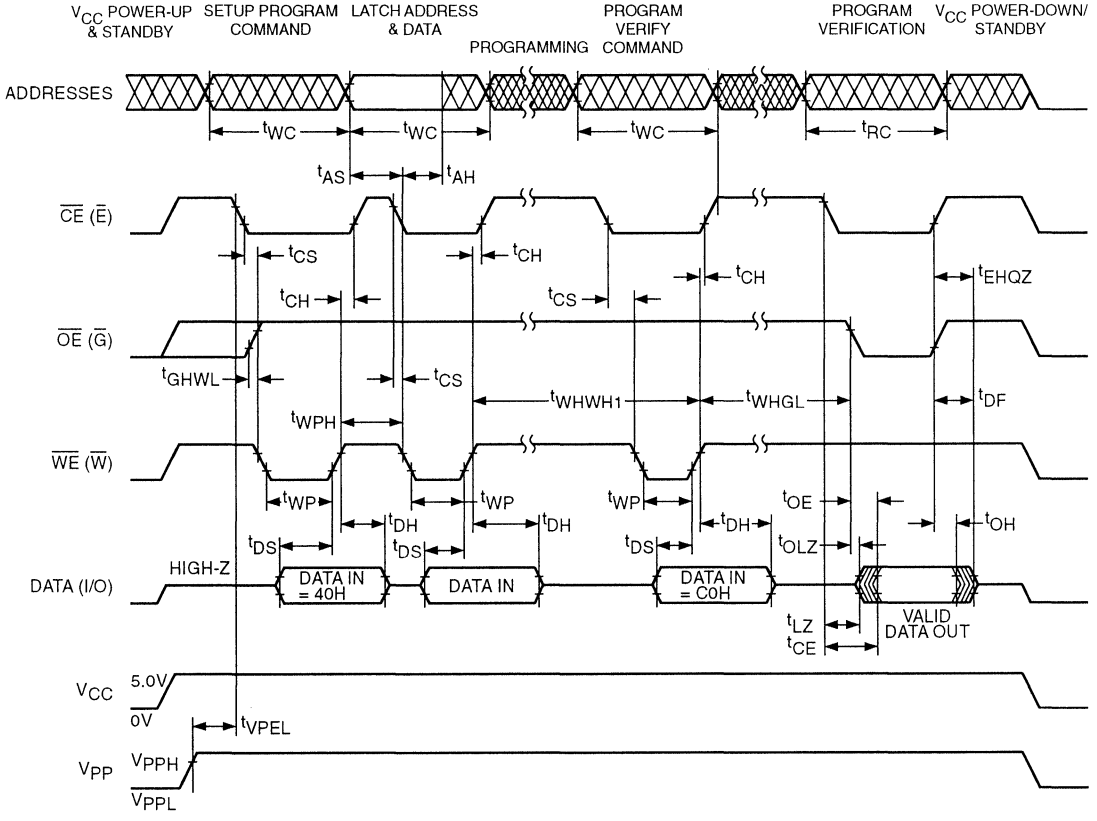
Erase-Verify Mode

The Erase-verify operation is performed on every byte after each erase pulse to verify that the bits have been erased.

Programming Mode

The programming operation is initiated using the programming algorithm of Figure 7. During the first write cycle, the command 40H is written into the command register. During the second write cycle, the address of tne memory location to be programmed is latched on the falling edge of $\overline{WE}$, while the data is latched on the rising edge of $\overline{WE}$. The program operation terminates with the next rising edge of $\overline{WE}$. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum program timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Figure 6. A.C. Timing for Programming Operation



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Program-Verify Mode

A Program-verify cycle is performed to ensure that all bits have been correctly programmed following each byte programming operation. The specific address is already latched from the write cycle just completed, and stays latched until the verify is completed. The Program-verify operation is initiated by writing C0H into the command register. An internal reference generates the necessary high voltages so that the user does not need to modify V_{CC}. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

TIMING PARAMETER SYMBOLS

Standard	JEDEC	Standard	JEDEC
t_{AS}	t_{AVWL}	t_{LZ}	t_{ELQX}
t_{AH}	t_{WLAX}	t_{OE}	t_{GLQV}
t_{CE}	t_{ELQV}	t_{OLZ}	t_{GLQX}
t_{CH}	t_{WHEH}	t_{RC}	t_{AVAV}
t_{CS}	t_{ELWL}	t_{WC}	t_{AVAV}
t_{DF}	t_{GHQZ}	t_{WP}	t_{WLWH}
t_{DH}	t_{WHDX}	t_{WPH}	t_{WHWL}
t_{DS}	t_{DVWH}		

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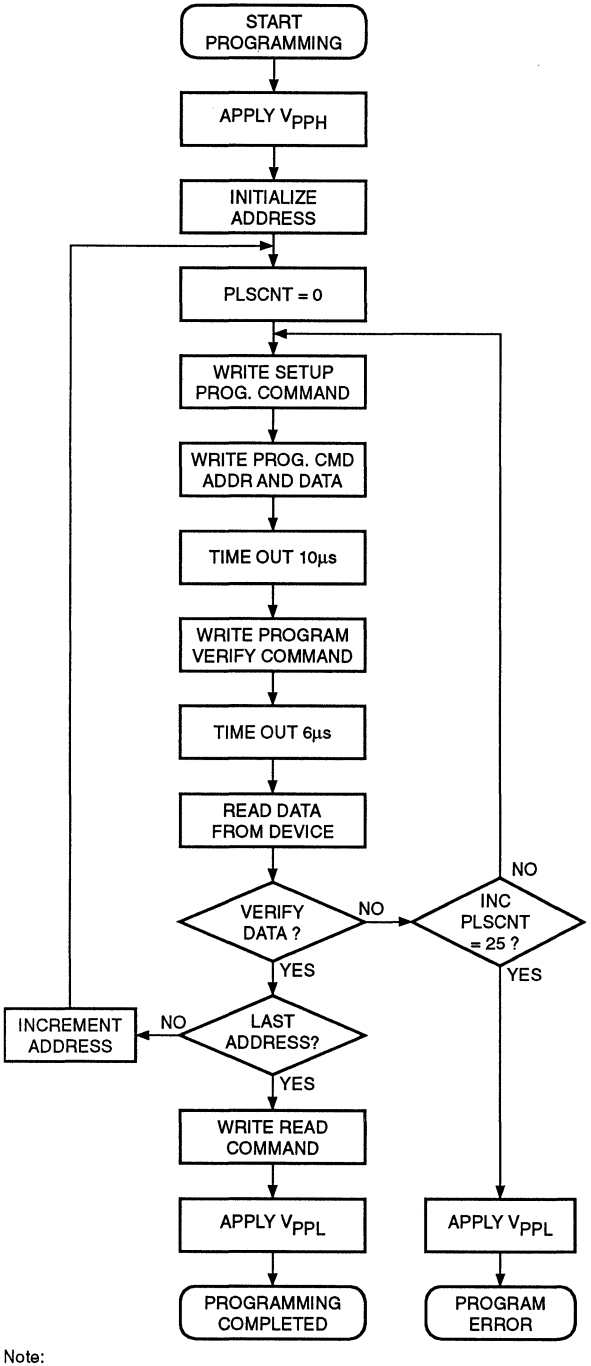
Figure 7. Programming Algorithm(16)



BUS OPERATION	COMMAND	COMMENTS
STANDBY		V_{PP} RAMPS TO V_{PPH} (OR V_{PP} HARDWIRED)
		INITIALIZE ADDRESS
		INITIALIZE PULSE COUNT PLSCNT = PULSE COUNT
1ST WRITE CYCLE	WRITE SETUP	DATA = 40H
2ND WRITE CYCLE	PROGRAM	VALID ADDRESS AND DATA
		WAIT
1ST WRITE CYCLE	PROGRAM VERIFY	DATA = C0H
		WAIT
READ		READ BYTE TO VERIFY PROGRAMMING
STANDBY		COMPARE DATA OUTPUT TO DATA EXPECTED
1ST WRITE CYCLE	READ	DATA = 00H SETS THE REGISTER FOR READ OPERATION
STANDBY		V_{PP} RAMPS TO V_{PPL} (OR V_{PP} HARDWIRED)

Note:
(16) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

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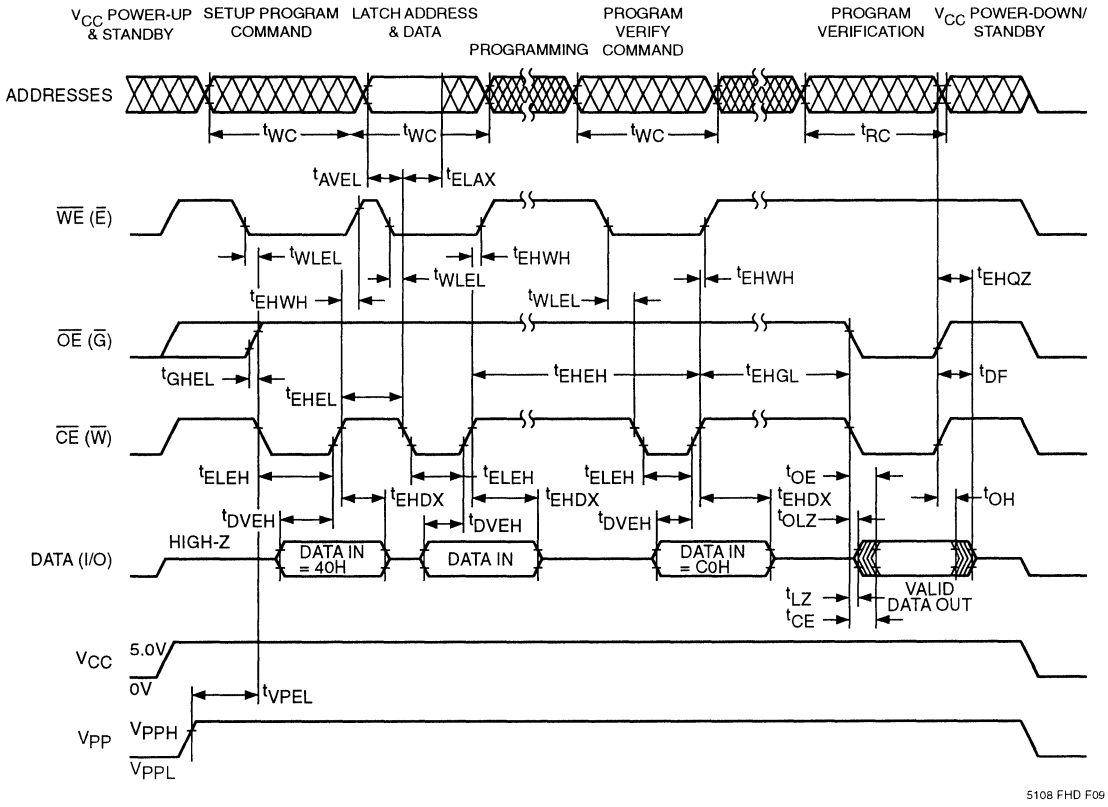
Abort/Reset

An Abort/Reset command is available to allow the user to safely abort an erase or program sequence. Two consecutive program cycles with FFH on the data bus will abort an erase or a program operation. The abort/reset operation can interrupt at any time in a program or erase operation and the device is reset to the Read Mode.

Figure 8. Alternate A.C. Timing for Program Operation



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POWER UP/DOWN PROTECTION

The CAT28F010/CAT28F010I offers protection against inadvertent programming during V_{PP} and V_{CC} power transitions. When powering up the device there is no power-on sequencing necessary. In other words, V_{PP} and V_{CC} may power up in any order. Additionally V_{PP} may be hardwired to V_{PPH} independent of the state of V_{CC} and any power up/down cycling. The internal command register of the CAT28F010/CAT28F010I is reset to the Read Mode on power up.

POWER SUPPLY DECOUPLING

To reduce the effect of transient power supply voltage spikes, it is good practice to use a 0.1μF ceramic capacitor between V_{CC} and V_{SS} and V_{PP} and V_{SS}. These high-frequency capacitors should be placed as close as possible to the device for optimum decoupling.

TIMING PARAMETER SYMBOLS

Standard	JEDEC
t_{WC}	t_{AVAV}
t_{OLZ}	t_{GLQX}
t_{LZ}	t_{ELQX}
t_{CE}	t_{ELQV}
t_{DE}	t_{ELQV}
t_{DF}	t_{GHQZ}

ALTERNATE $\overline{CE}$-CONTROLLED WRITES

Symbol	Parameter	28F010-12 28F010I-12		28F010-15 28F010I-15		28F010-20 28F010I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	Write Cycle Time	120		150		200		ns
t_{AVEL}	Address Setup Time	0		0		0		ns
t_{ELAX}	Address Hold Time	80		80		95		ns
t_{DVEH}	Data Setup Time	50		50		50		ns
t_{EHDX}	Data Hold Time	10		10		10		ns
t_{EHGL}	Write Recovery Time Before Read	6		6		6		µs
t_{GHEL}	Read Recovery Time Before Write	0		0		0		µs
t_{WLEL}	$\overline{WE}$ Setup Time Before $\overline{CE}$	0		0		0		ns
t_{EHWH}	Write Enable Hold Time	0		0		0		ns
t_{ELEH}	Write Pulse Width	70		70		80		ns
t_{EHEL}	Write Pulse Width High	20		20		20		ns
t_{VPEL}	V_{PP} Setup Time to $\overline{CE}$ Low	1.0		1.0		1.0		µs

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CAT28F010V5/CAT28F010V5I

1 Megabit CMOS FLASH MEMORY

FEATURES

- Fast Read Access Time: 120/150/200 ns
- Low Power CMOS Dissipation:
  - –Active: 120 mA max (CMOS/TTL levels)
  - –Standby: 1 mA max (TTL levels)
  - –Standby: 100 µA max (CMOS levels)
- High Speed Programming:
  - –10 µS per byte
  - –2 Sec Typ Chip Program
- 5V ± 10% Programming and Erase Voltage
- Stop Timer for Program/Erase
- On-Chip Address and Data Latches
- JEDEC Standard Pinouts:
  - –32 pin DIP
  - –32 pin PLCC
  - –32 pin TSOP (8 x 14; 8 x 20)
- 10,000 Program/Erase Cycles
- 10 Year Data Retention
- Electronic Signature

DESCRIPTION

The CAT28F010V5/CAT28F010V5I is a high speed 128K x 8 bit electrically erasable and reprogrammable Flash memory ideally suited for applications requiring in-system or after-sale code updates. A single 5 volt supply handles all electrical chip erasure and programming. The memory is divided into 64 sectors of 2K bytes each.

The CAT28F010V5/CAT28F010V5I features Random Access Sector Erase by which the user can selectively erase any one of the 64 2K byte sectors. This enhances system performance since the need to erase the entire memory array is eliminated.

It is pin and Read timing compatible with standard EPROM and E²PROM devices. Programming and Erase are performed through an operation and verify algorithm. The instructions are input via the I/O bus, using a two write cycle scheme. Address and Data are latched to free the I/O bus and address bus during the write operation.

The CAT28F010V5/CAT28F010V5I is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 32 pin plastic DIP, 32 pin PLCC or 32 pin TSOP packages.

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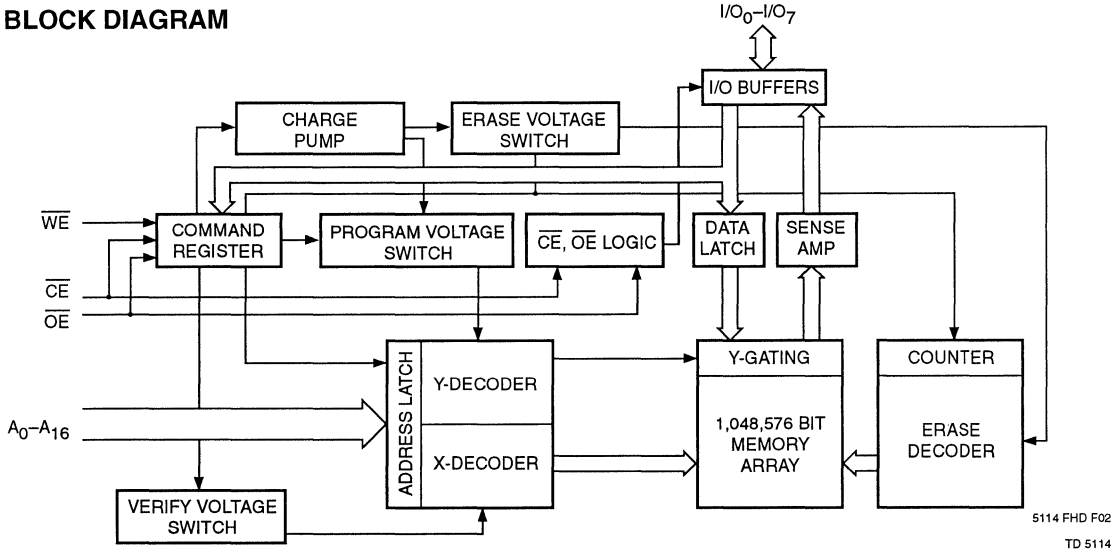
BLOCK DIAGRAM



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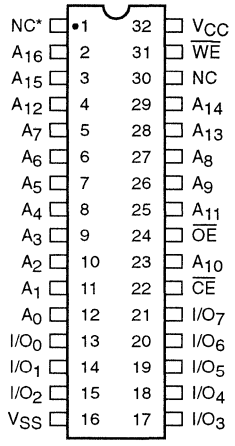
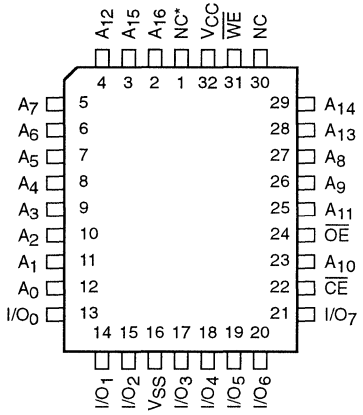
PIN CONFIGURATION

DIP Package



PLCC Package



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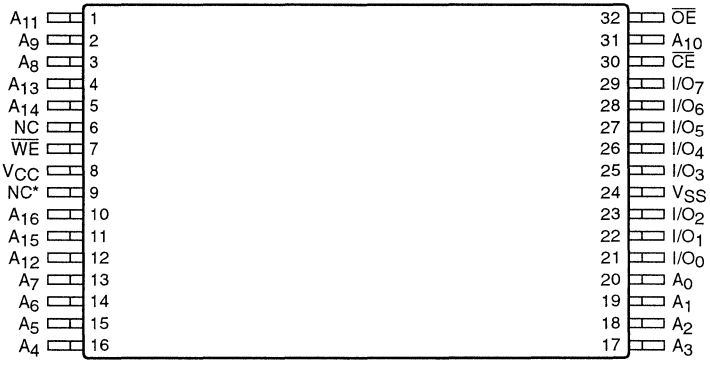
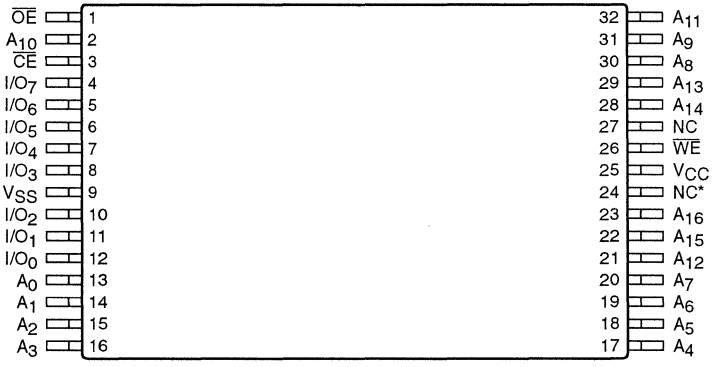
PIN FUNCTIONS

Pin Name	Type	Function
A_0–A_{16}	Input	Address Inputs for memory addressing
I/O_0–I/O_7	I/O	Data Input/Output
$\overline{CE}$	Input	Chip Enable
$\overline{OE}$	Input	Output Enable
$\overline{WE}$	Input	Write Enable
V_{CC}		Voltage Supply
V_{SS}		Ground
NC		No Connect
NC*		Internal connection should be connected to either V_{CC} or V_{SS}

TSOP Package (Standard Pinout)



TSOP Package (Reverse Pinout)



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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +95°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) .....–2.0V to +V_{CC} + 2.0V

Voltage on Pin A_9 with Respect to Ground(1) .....–2.0V to +13.5V

V_{CC} with Respect to Ground(1) .....–2.0V to +7.0V

Package Power Dissipation Capability (T_A = 25°C) ..... 1.0 W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(3)	Endurance	1K, 10K		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Limits		Units	Conditions
		Min	Max.		
C_{IN}(3)	Input Pin Capacitance		6	pF	V_{IN} = 0V
C_{OUT}(3)	Output Pin Capacitance		10	pF	V_{OUT} = 0V

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Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

CAT28F010V5 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT28F010V5I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{LI}	Input Leakage Current		±1.0	µA	$V_{IN} = V_{CC}$ or V_{SS} V_{CC} = 5.5V, $\overline{OE} = V_{IH}$
I_{LO}	Output Leakage Current		±10	µA	$V_{OUT} = V_{CC}$ or V_{SS}, V_{CC} = 5.5V, $\overline{OE} = V_{IH}$
I_{SB1}	V_{CC} Standby Current CMOS		100	µA	$\overline{CE} = V_{CC}$ ±0.5V, V_{CC} = 5.5V
I_{SB2}	V_{CC} Standby Current TTL		1.0	mA	$\overline{CE} = V_{IH}$, V_{CC} = 5.5V
I_{CC1}	V_{CC} Active Read/Verify Current		30	mA	V_{CC} = 5.5V, $\overline{CE} = V_{IL}$, I_{OUT} = 0mA, f = 6 MHz
I_{CC2}(3)	V_{CC} Programming Current		120	mA	V_{CC} = 5.5V, Programming in Progress
I_{CC3}(3)	V_{CC} Erase Current		30	mA	V_{CC} = 5.5V, Erasure in Progress
V_{IL}	Input Low Level TTL	–0.5	0.8	V	
V_{ILC}	Input Low Level CMOS	–0.5	0.8	V	
V_{OL}	Output Low Level		0.45	V	I_{OL} = 5.8mA, V_{CC} = 4.5V
V_{IH}	Input High Level TTL	2.0	V_{CC}+0.5	V	
V_{IHC}	Input High Level CMOS	0.7 V_{CC}	V_{CC}+0.5	V	
V_{OH}	Output High Level TTL	2.4		V	I_{OH} = –2.5mA, V_{CC} = 4.5V
V_{OH1}	Output High Level CMOS	0.85 V_{CC}		V	I_{OH} = –2.5mA, V_{CC} = 4.5V
V_{OH2}	Output High Level CMOS	V_{CC}–0.4		V	I_{OH} = –400µA, V_{CC} = 4.5V
V_{ID}	A_9 Signature Voltage	11.4	13.0	V	$A_9 = V_{ID}$
I_{ID}	A_9 Signature Current		200	µA	$A_9 = V_{ID}$
V_{LO}	V_{CC} Erase/Prog. Lockout Voltage	2.5		V	

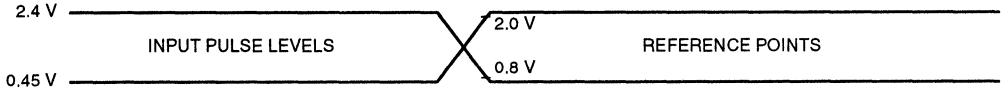
Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.

\.C. CHARACTERISTICS, Read Operation

:AT28F010V5 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
:AT28F010V5I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	28F010V5-12 28F010V5I-12		28F010V5-15 28F010V5I-15		28F010V5-20 28F010V5I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	120		150		200		ns
t_{CE}	$\overline{CE}$ Access Time		120		150		200	ns
t_{ACC}	Address Access Time		120		150		200	ns
t_{OE}	$\overline{OE}$ Access Time		50		55		60	ns
t_{OH}	Output Hold from Address $\overline{OE}$/$\overline{CE}$ Change	0		0		0		ns
t_{OLZ}[3][9]	$\overline{OE}$ to Output in Low-Z	0		0		0		ns
t_{LZ}[3][9]	$\overline{CE}$ to Output in Low-Z	0		0		0		ns
t_{DF}[3][5]	$\overline{OE}$ High to Output High-Z		30		35		40	ns
t_{EHQZ}[3][5]	$\overline{CE}$ High to Output High-Z		55		55		55	ns
t_{WHGL}[3]	Write Recovery Time Before Read	6		6		6		µs

'igure 1. A.C. Testing Input/Output Waveform[6][7][8]



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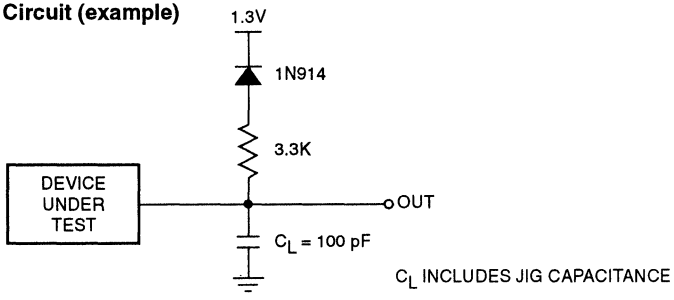
'igure 2. A.C. Testing Load Circuit (example)



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Note:
3) This parameter is tested initially and after a design or process change that affects the parameter.
5) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
6) Input Rise and Fall Times (10% to 90%) < 10 ns.
7) Input Pulse Levels = 0.45V and 2.4V.
8) Input and Output Timing Reference = 0.8V and 2.0V.
9) Low-Z is defined as the state where the external data may be driven by the output buffer but may not be valid.

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A.C. CHARACTERISTICS, Program/Erase Operation

CAT28F010V5 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT28F010V5I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	28F010V5-12 28F010V5I-12		28F010V5-15 28F010V5I-15		28F010V5-20 28F010V5I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	120		150		200		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	60		60		75		ns
t_{DS}	Data Setup Time	50		50		50		ns
t_{DH}	Data Hold Time	10		10		10		ns
t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{WP}	$\overline{WE}$ Pulse Width	60		60		60		ns
t_{WPH}	$\overline{WE}$ High Pulse Width	20		20		20		ns
t_{WPWH1}(11)	Program Pulse Width	10		10		10		µs
t_{WPWH2}(11)	Erase Pulse Width	9.5		9.5		9.5		ms
t_{WPGL}	Write Recovery Time Before Read	6		6		6		µs
t_{GHWL}	Read Recovery Time Before Write	0		0		0		µs

ERASE AND PROGRAMMING PERFORMANCE

Parameter	28F010V5-12 28F010V5I-12			28F010V5-15 28F010V5I-15			28F010V5-20 28F010V5I-20			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Erase Time(11)(13)		10	320		10	320		15	320	sec
Chip Program Time(11)(12)		2	10		2	10		2	10	sec
Sector Erase Time(11)(13)		0.3	10		0.3	10		0.5	30	sec

Note:
(10) Program and Erase operations are controlled by internal stop timers.
(11) 'Typicals' are not guaranteed, but based on characterization data. Data taken at 25°C.
(12) Minimum byte programming time (excluding system overhead) is 16 µs (10 µs program + 6 µs write recovery), while maximum is 400 µs/byte (16 µs x 25 loops). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
(13) Excludes 00H Programming prior to Erasure.

'UNCTION TABLE(14)

Mode	Pins				Notes
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	
ReadV_{IL}	V_{IL}	V_{IH}	D_{OUT}		
Output Disable	V_{IL}	V_{IH}	V_{IH}	High-Z	
Standby	V_{IH}	X	X	High-Z	
Signature (MFG)	V_{IL}	V_{IL}	V_{IH}	31H	$A_0 = V_{IL}$, $A_9 = 12V$
Signature (Device)	V_{IL}	V_{IL}	V_{IH}	B5H	$A_0 = V_{IL}$, $A_9 = 12V$
Program/Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	See Command Table
Write Cycle	V_{IL}	V_{IH}	V_{IL}	D_{IN}	During Write Cycle
Read Cycle	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	During Write Cycle

'RITE COMMAND TABLE

Mode	Pins						
	First Bus Cycle			Second Bus Cycle			
	Operation	Address	D_{IN}	Operation	Address	D_{IN}	D_{OUT}
Set Read	Write	X	00H	Read	Any		D_{OUT}
Read Sig. (MFG)	Write	X	90H	Read	00		31H
Read Sig. (Device)	Write	X	90H	Read	01		B5H
Random Sector Erase	Write	X	60H	Write	Sector Addr	60H	
Sequential Sector Erase	Write	X	20H	Write	X	20H	
Erase Verify	Write	X	A0H	Read	X		D_{OUT}
Program	Write	X	40H	Write	A_{IN}	D_{IN}	
Program Verify	Write	X	C0H	Read	X		D_{OUT}
Reset	Write	X	FFH	Write	X	FFH	

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lote:
14) Logic Levels: X = Logic 'Do not care' (V_{IH}, V_{IL})

READ OPERATIONS

Read Mode

A Read operation is performed with both $\overline{CE}$ and $\overline{OE}$ low and with $\overline{WE}$ high. V_{PP} can be either high or low, however, if V_{PP} is high, the Set READ command has to be sent before reading data (see Write Operations). The data retrieved from the I/O pins reflects the contents of the memory location corresponding to the state of the 17 address pins. The respective timing waveforms for the read operation are shown in Figure 3. Refer to the AC Read characteristics for specific timing parameters.

Signature Mode

The signature mode allows the user to identify the IC manufacturer and the type of device while the device resides in the target system. This mode can be activated in either of two ways; through the conventional method of applying a high voltage (12V) to address pin A_9 or by sending an instruction to the command register (see Write Operations).

The conventional mode is entered as a regular READ mode by driving the $\overline{CE}$ and $\overline{OE}$ pins low (with $\overline{WE}$ high) and applying the required high voltage on address pin A9 while all other address lines are held at V_{IL}.

A Read cycle from address 0000H retrieves the binary code for the IC manufacturer on outputs I/O_0 to I/O_7:

CATALYST Code = 00110001 (31H)

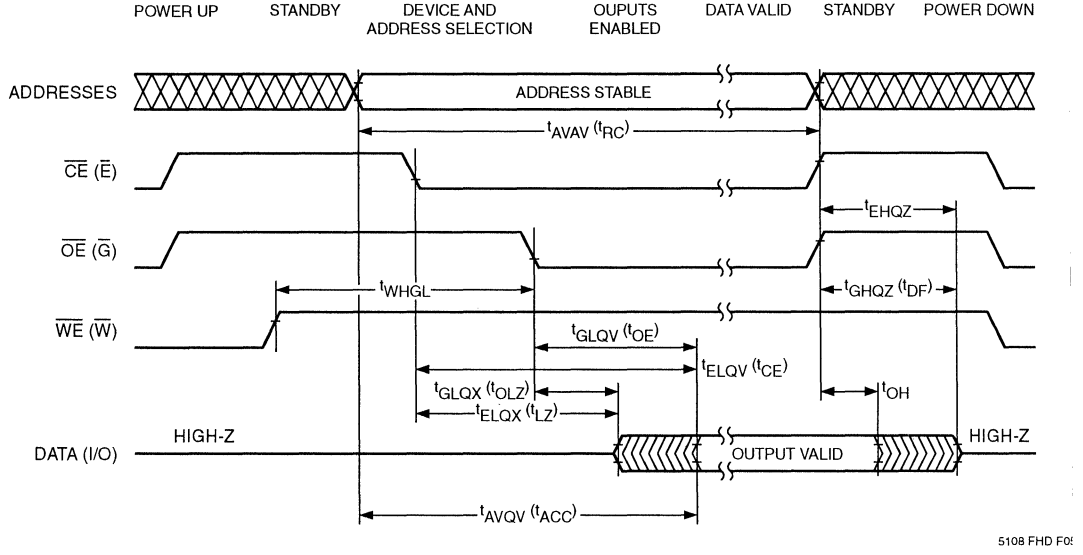
A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F010V5/28F010V5I Code = 1011 0101 (B5H)

Standby Mode

With $\overline{CE}$ at a logic-high level, the CAT28F010V5 CAT28F010V5I is placed in a standby mode where most of the device circuitry is disabled, thereby substantially reducing power consumption. The outputs are placed in a high-impedance state.

Figure 3. A.C. Timing for Read Operation



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WRITE OPERATIONS

The following operations are initiated by observing the sequence specified in the Write Command Table.

Read Mode

The device can be put into a standard READ mode by initiating a write cycle with 00H on the data bus. The subsequent read cycles will be performed similar to a standard EPROM or E^2PROM Read.

Signature Mode

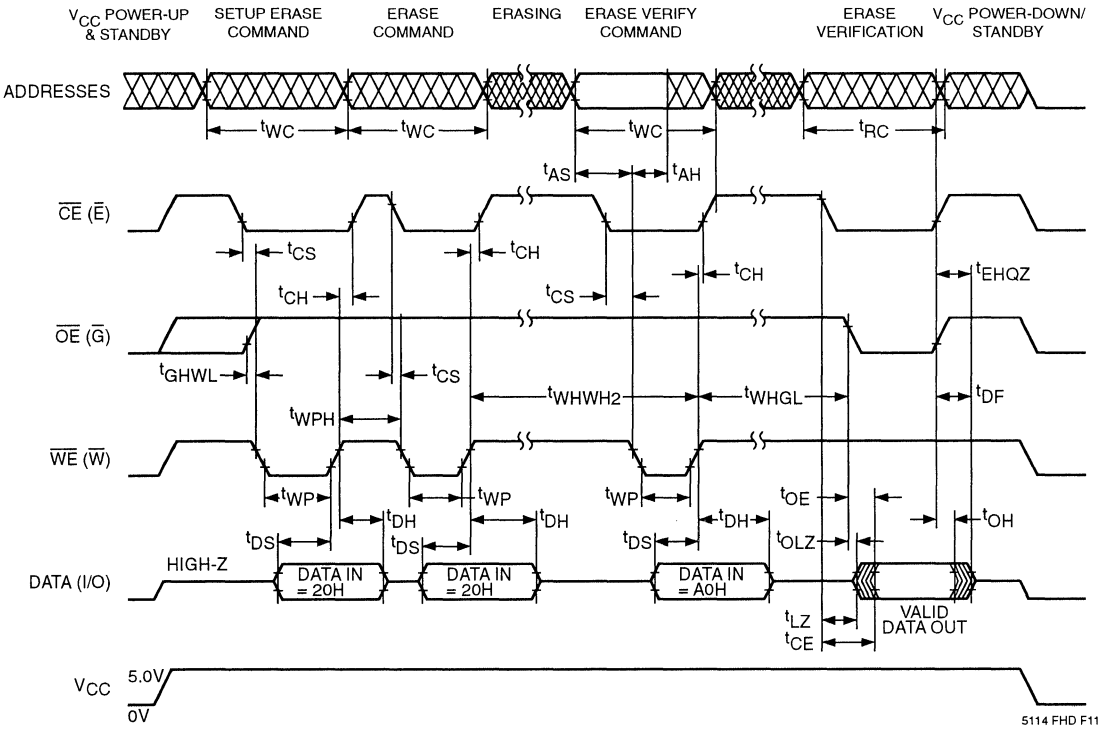
An alternative method for reading device signature (see Read Operations Signature Mode), is initiated by writing the code 90H into the command register while keeping V_{PP} high. A read cycle from address 0000H with $\overline{CE}$ and $\overline{OE}$ low (and $\overline{WE}$ high) will output the device signature.

CATALYST Code = 00110001 (31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F010V5/28F010V5I Code = 1011 0101 (B5H)

Figure 4. A.C. Timing for Erase Operation



Erase Modes

The CAT28F010V5/CAT28F010V5I is organized as 64 sectors of 2K bytes each. The user can erase the entire memory contents (chip erase using Sequential Sector erase) by following the erase algorithm shown in Figure 6. Alternatively, the user can randomly erase any one of the 64 sectors using the Random Access Sector erase algorithm shown in Figure 5. The erase process is accomplished by first programming all bytes to "00" and then erasing all bytes to the "FF" state. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum erase timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

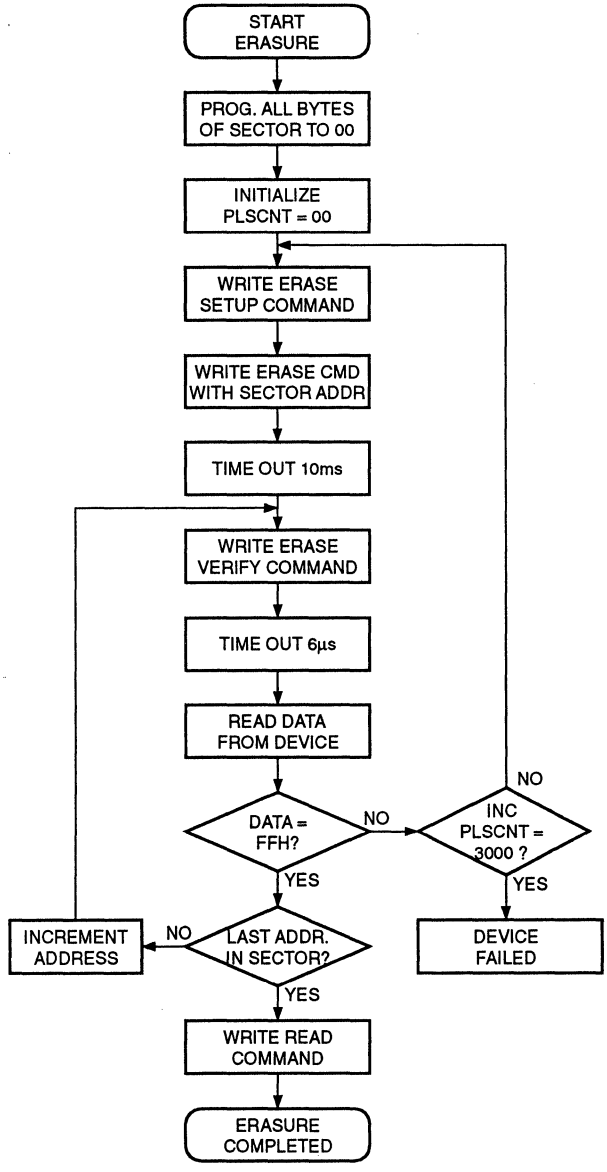
Random Access Sector Erase

The CAT28F010V5/CAT28F010V5I features a random access sector erase where an individual sector (2K bytes) can be erased independent of the other sectors (see Figure 5). To erase a sector, a write command with data 60H is first sent to the device (it is assumed that all locations within the sector have first been written to 00H). A second write command (with data = 60H) along with the beginning address of the sector to be erased is sent next (address bits A11–A16 define the sector). Finally, after sending an erase-verify command, the device will erase the specified 2K sector. The Random Access Sector Erase feature minimizes the chance of inadvertently erasing data from sectors that contain boot code or critical data.

TIMING PARAMETER SYMBOLS

Standard	JEDEC	Standard	JEDEC
t_{AS}	t_{AVWL}	t_{LZ}	t_{ELQX}
t_{AH}	t_{WLAX}	t_{OE}	t_{GLQV}
t_{CE}	t_{ELQV}	t_{OLZ}	t_{GLQX}
t_{CH}	t_{WHEH}	t_{RC}	t_{AVAV}
t_{CS}	t_{ELWL}	t_{WC}	t_{AVAV}
t_{DF}	t_{GHQZ}	t_{WP}	t_{WLWH}
t_{DH}	t_{WHDX}	t_{WPH}	t_{WHWL}
t_{DS}	t_{DVWH}		

Figure 5. Random Access Sector Erase Algorithm(15)



BUS OPERATION	COMMAND	COMMENTS
		ALL BYTES WITHIN SECTOR SHOULD BE PROGRAMMED TO 00 BEFORE AN ERASE OPERATION
		PLSCNT = PULSE COUNT
WRITE	ERASE	ACTUAL ERASE NEEDS 10ms PULSE, DATA = 60H
WRITE	ERASE	DATA = 60H ADDRESS = SECTOR ADDR
		WAIT
WRITE	ERASE VERIFY	ADDR = BYTE TO VERIFY DATA = A0H
		WAIT
READ		READ BYTE TO VERIFY ERASURE
STANDBY		COMPARE OUTPUT TO FF INC PULSE COUNT
WRITE	READ	DATA = 00H, RESETS REGISTERS FOR READ OPERATION
STANDBY		

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Note:
(15) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

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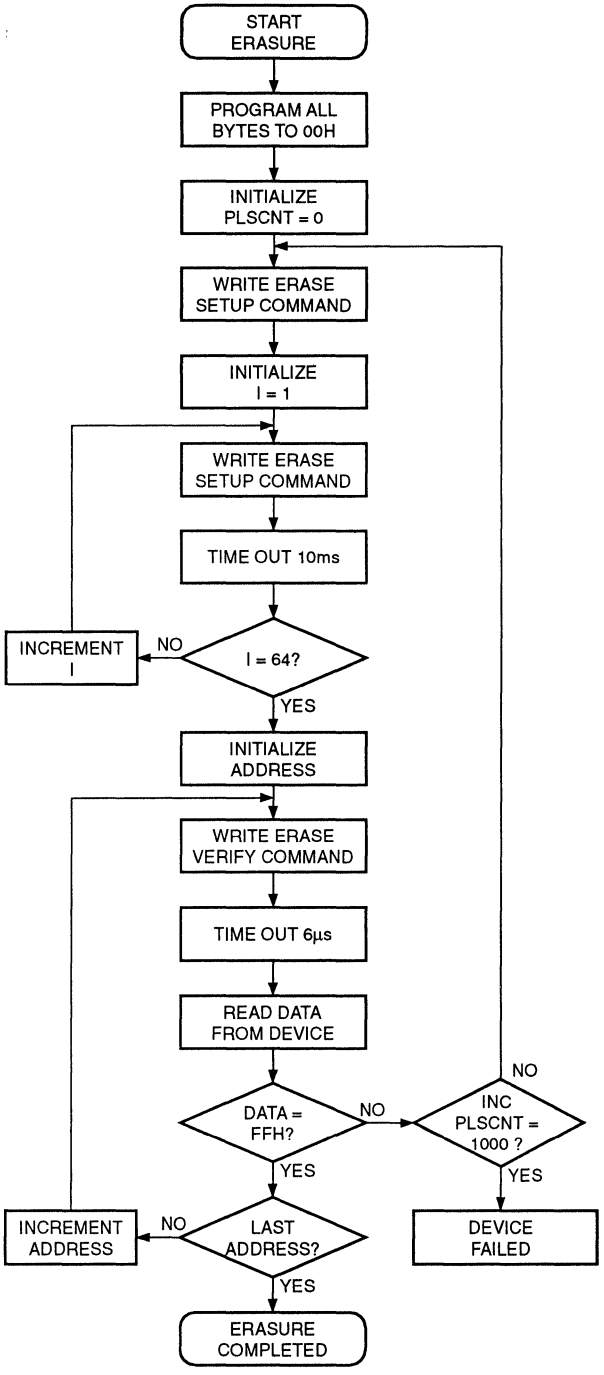
Sequential Sector Erase

During the first Write operation, the command 20H is written into the command register. In order to commence the erase operation, the identical command of 20H has to be written again into the register. This two step process ensures against accidental erasure of the memory contents. The erase cycle is repeated 64 times to erase each of the 64 internal memory blocks sequentially. The final erase operation will be stopped at the rising edge of $\overline{WE}$, at which time the Erase Verify command (A0H) is sent to the command register. During this time, the address to be verified is sent to the address bus and latched when $\overline{WE}$ goes high.

Figure 6. Chip Erase Algorithm (using Sequential Sector Erase)(15)



BUS OPERATION	COMMAND	COMMENTS
		ALL BYTES SHALL BE PROGRAMMED TO 00 BEFORE AN ERASE OPERATION
		PLSCNT = PULSE COUNT
WRITE	ERASE	ACTUAL ERASE NEEDS 10ms PULSE, DATA = 20H
		I = SECTOR INCREMENT COUNTER
WRITE	ERASE	DATA = 20H
		WAIT
		64 ERASE COMMANDS ARE NECESSARY TO ERASE ALL SECTORS
WRITE	ERASE VERIFY	ADDR = BYTE TO VERIFY DATA = A0H
		WAIT
READ		READ BYTE TO VERIFY ERASURE
STANDBY		COMPARE OUTPUT TO FF INCR PULSE COUNT

5114 FHD F08

Note:
(15) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

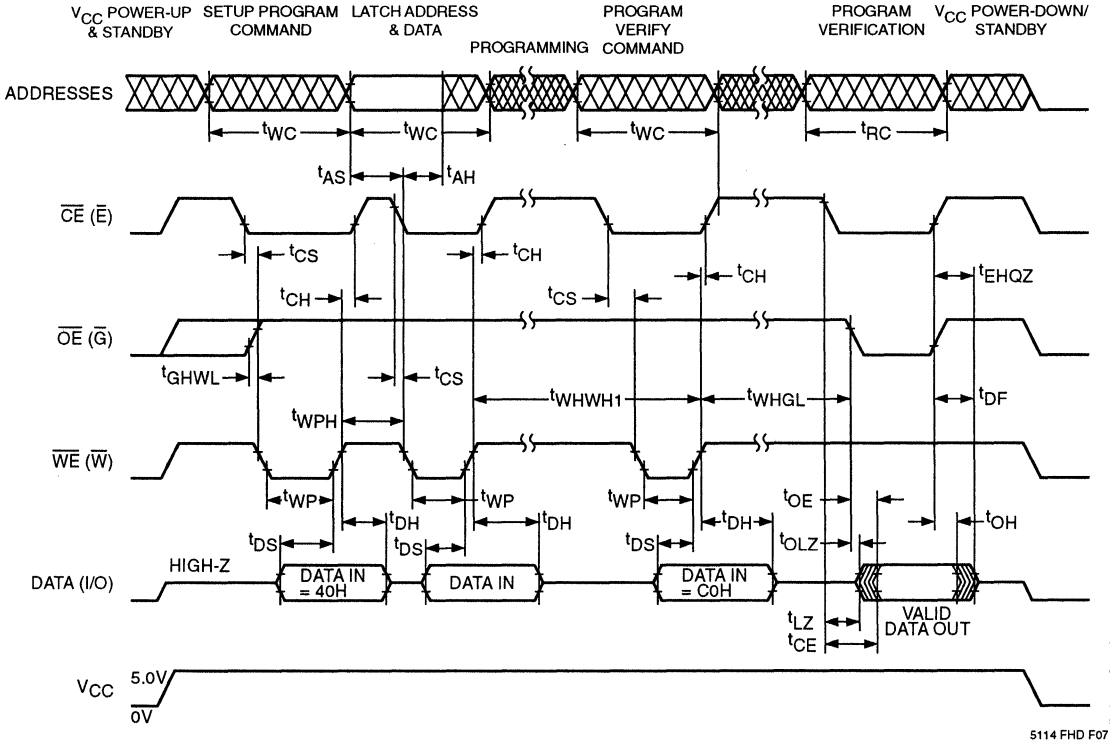
ERASE-VERIFY MODE

The Erase-verify operation is performed on every byte after each erase pulse to verify that the bits have been erased.

Programming Mode

The programming operation is initiated using the programming algorithm of Figure 7. During the first write cycle, the command 40H is written into the command register. During the second write cycle, the address of the memory location to be programmed is latched on the falling edge of $\overline{WE}$, while the data is latched on the rising edge of $\overline{WE}$. The program operation terminates with the next rising edge of $\overline{WE}$. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum program timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Figure 7. A.C. Timing for Programming Operation



Program-Verify Mode

A Program-verify cycle is performed to ensure that all bits have been correctly programmed following each byte programming operation. The specific address is already latched from the write cycle just completed, and stays latched until the verify is completed. The Program-verify operation is initiated by writing C0H into the command register. An internal reference generates the necessary high voltages so that the user does not need to modify V_{CC}. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

TIMING PARAMETER SYMBOLS

Standard	JEDEC	Standard	JEDEC
t_{AS}	t_{AVWL}	t_{LZ}	t_{ELQX}
t_{AH}	t_{WLAX}	t_{OE}	t_{GLQV}
t_{CE}	t_{ELQV}	t_{OLZ}	t_{GLQX}
t_{CH}	t_{WHEH}	t_{RC}	t_{AVAV}
t_{CS}	t_{ELWL}	t_{WC}	t_{AVAV}
t_{DF}	t_{GHQZ}	t_{WP}	t_{WLWH}
t_{DH}	t_{WHDX}	t_{WPH}	t_{WHWL}
t_{DS}	t_{DVWH}		

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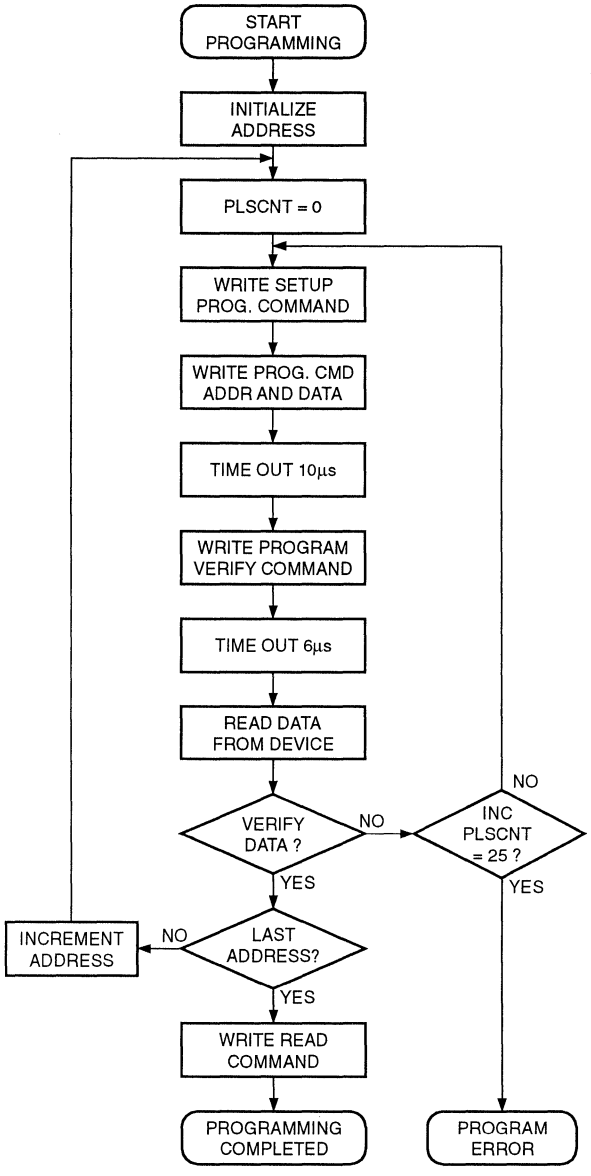
Figure 8. Programming Algorithm(15)



BUS OPERATION	COMMAND	COMMENTS
		INITIALIZE ADDRESS
		INITIALIZE PULSE COUNT PLSCNT = PULSE COUNT
1ST WRITE CYCLE	WRITE SETUP	DATA = 40H
2ND WRITE CYCLE	PROGRAM	VALID ADDRESS AND DATA
		WAIT
1ST WRITE CYCLE	PROGRAM VERIFY	DATA = C0H
		WAIT
READ		READ BYTE TO VERIFY PROGRAMMING
STANDBY		COMPARE DATA OUTPUT TO DATA EXPECTED
1ST WRITE CYCLE	READ	DATA = 00H SETS THE REGISTER FOR READ OPERATION

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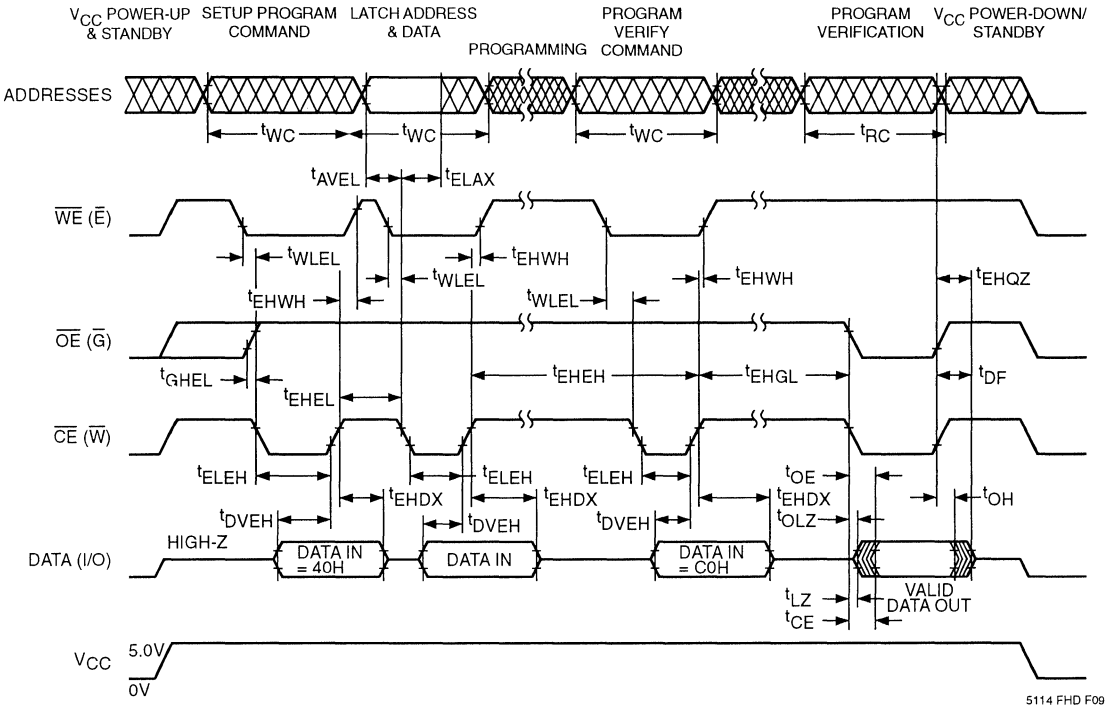
Note:
(15) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

Abort/Reset

An Abort/Reset command is available to allow the user to safely abort an erase or program sequence. Two consecutive program operations with FFH on the data bus will abort an erase or a program operation. The Abort/Reset operation also resets the sector pointer in the sequential sector erase mode. The Abort/Reset operation can interrupt at any time in a program or erase operation, and the device is reset to the Read mode. If an Abort/Reset command is sent prior to completion of an erase or program sequence, a partial erase or program may occur. If a program operation is aborted by the Reset command, the byte in progress can later be programmed. If an erase operation is aborted by the reset command, the erase operation can be continued after the abort.

Figure 9. Alternate A.C. Timing for Program Operation



POWER SUPPLY DECOUPLING

To reduce the effect of transient power supply voltage spikes, it is good practice to use a 0.1µF ceramic capacitor between V_{CC} and V_{SS}. These high-frequency capacitors should be placed as close as possible to the device for optimum decoupling.

It is recommended after a power up to issue an Abort Reset command when operating in particularly noisy environments. No power supply sequencing is required.

TIMING PARAMETER SYMBOLS

Standard	JEDEC
t_{WC}	t_{AVAV}
t_{OLZ}	t_{GLQX}
t_{LZ}	t_{ELQX}
t_{CE}	t_{ELQV}
t_{DE}	t_{ELQV}
t_{DF}	t_{GHQZ}

ALTERNATE $\overline{CE}$-CONTROLLED WRITES

Symbol	Parameter	28F010V5-12 28F010V5I-12		28F010V5-15 28F010V5I-15		28F010V5-20 28F010V5I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	Write Cycle Time	120		150		200		ns
t_{AVEL}	Address Setup Time	0		0		0		ns
t_{ELAX}	Address Hold Time	80		80		95		ns
t_{DVEH}	Data Setup Time	50		50		50		ns
t_{EHDX}	Data Hold Time	10		10		10		ns
t_{EHGL}	Write Recovery Time Before Read	6		6		6		µs
t_{GHEL}	Read Recovery Time Before Write	0		0		0		µs
t_{WLEL}	$\overline{WE}$ Setup Time Before $\overline{CE}$	0		0		0		ns
t_{EHWH}	Write Enable Hold Time	0		0		0		ns
t_{ELEH}	Write Pulse Width	70		70		80		ns
t_{EHEL}	Write Pulse Width High	20		20		20		ns

CATALYST SEMICONDUCTOR

CAT28F020/CAT28F020I

2 Megabit CMOS FLASH MEMORY

FEATURES

- Fast Read Access Time: 120/150/200 ns
- Low Power CMOS Dissipation:
  - –Active: 30 mA max (CMOS/TTL levels)
  - –Standby: 1 mA max (TTL levels)
  - –Standby: 100 μA max (CMOS levels)
- High Speed Programming:
  - –10 μS per byte
  - –4 Sec Typ Chip Program
- 12.0V ± 5% Programming and Erase Voltage
- Stop Timer for Program/Erase
- On-Chip Address and Data Latches
- JEDEC Standard Pinouts:
  - –32 pin DIP
  - –32 pin PLCC
  - –32 pin TSOP (8 x 14; 8 x 20)
- 10,000 Program/Erase Cycles
- 10 Year Data Retention
- Electronic Signature

DESCRIPTION

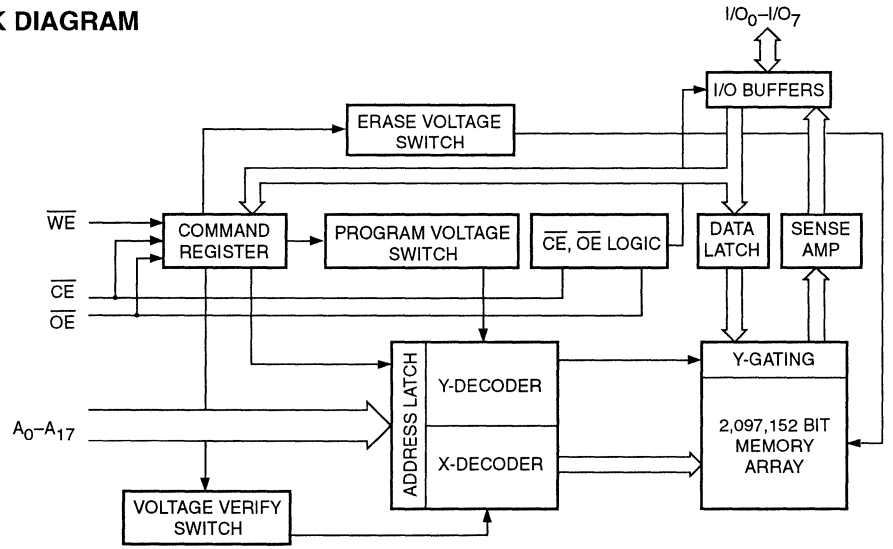
The CAT28F020/CAT28F020I is a high speed 256K x 8 bit electrically erasable and reprogrammable Flash memory ideally suited for applications requiring in-system or after-sale code updates. Electrical erasure of the full memory contents is achieved typically within 1 second.

It is pin and Read timing compatible with standard EPROM and E²PROM devices. Programming and Erase are performed through an operation and verify algorithm. The instructions are input via the I/O bus, using a two write cycle scheme. Address and Data are latched to free the I/O bus and address bus during the write operation.

The CAT28F020/CAT28F020I is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 32 pin plastic DIP, 32 pin PLCC or 32 pin TSOP packages.

8

BLOCK DIAGRAM

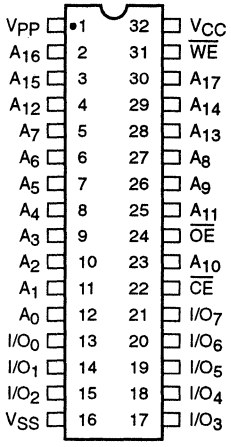


5115 FHD F02

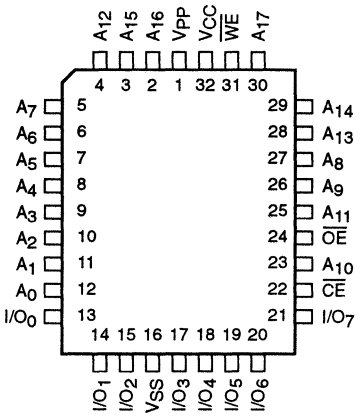
TD 5115

PIN CONFIGURATION

DIP Package



PLCC Package

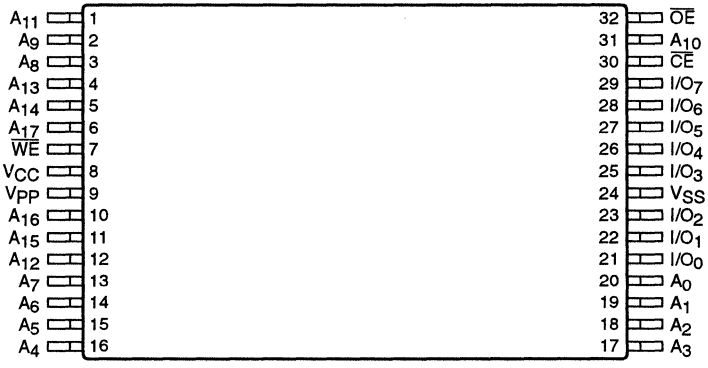


5115 FHD F01

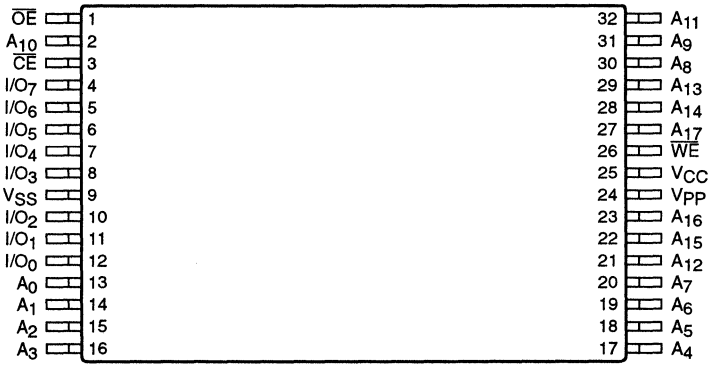
PIN FUNCTIONS

Pin Name	Type	Function
A_0–A_{17}	Input	Address Inputs for memory addressing
I/O_0–I/O_7	I/O	Data Input/Output
$\overline{CE}$	Input	Chip Enable
$\overline{OE}$	Input	Output Enable
$\overline{WE}$	Input	Write Enable
V_{CC}		Voltage Supply
V_{SS}		Ground
V_{PP}		Program/Erase Voltage Supply

TSOP Package (Standard Pinout)



TSOP Package (Reverse Pinout)



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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +95°C

Storage Temperature .....–65°C to +150°C

Voltage on Any Pin with
Respect to Ground(1) .....–2.0V to +V_{CC} + 2.0V

Voltage on Pin A_9 with
Respect to Ground(1) .....–2.0V to +13.5V

V_{PP} with Respect to Ground
during Program/Erase(1) .....–2.0V to +14.0V

V_{CC} with Respect to Ground(1) .....–2.0V to +7.0V

Package Power Dissipation
Capability (T_A = 25°C) ..... 1.0 W

Lead Soldering Temperature (10 secs) .....300°C

Output Short Circuit Current(2) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(3)	Endurance	1K, 10K		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Limits		Units	Conditions
		Min	Max.		
C_{IN}(3)	Input Pin Capacitance		6	pF	V_{IN} = 0V
C_{OUT}(3)	Output Pin Capacitance		10	pF	V_{OUT} = 0V
C_{VPP}(3)	V_{PP} Supply Capacitance		25	pF	V_{PP} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

D.C. OPERATING CHARACTERISTICS

CAT28F020 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT28F020I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{LI}	Input Leakage Current		±1.0	µA	$V_{IN} = V_{CC}$ or V_{SS} V_{CC} = 5.5V, $\overline{OE} = V_{IH}$
I_{LO}	Output Leakage Current		±10	µA	$V_{OUT} = V_{CC}$ or V_{SS}, V_{CC} = 5.5V, $\overline{OE} = V_{IH}$
I_{SB1}	V_{CC} Standby Current CMOS		100	µA	$\overline{CE} = V_{CC}$ ±0.5V, V_{CC} = 5.5V
I_{SB2}	V_{CC} Standby Current TTL		1.0	mA	$\overline{CE} = V_{IH}$, V_{CC} = 5.5V
I_{CC1}	V_{CC} Active Read Current		30	mA	V_{CC} = 5.5V, $\overline{CE} = V_{IL}$, I_{OUT} = 0mA, f = 6 MHz
I_{CC2}(3)	V_{CC} Programming Current		15	mA	V_{CC} = 5.5V, Programming in Progress
I_{CC3}(3)	V_{CC} Erase Current		15	mA	V_{CC} = 5.5V, Erasure in Progress
I_{CC4}(3)	V_{CC} Prog./Erase Verify Current		15	mA	$V_{PP} = V_{PPH}$, Program or Erase Verify in Progress
I_{PPS}	V_{PP} Standby Current		±10	µA	$V_{PP} = V_{PPL}$
I_{PP1}	V_{PP} Read Current		200	µA	$V_{PP} = V_{PPH}$
I_{PP2}(3)	V_{PP} Programming Current		30	mA	$V_{PP} = V_{PPH}$, Programming in Progress
I_{PP3}(3)	V_{PP} Erase Current		30	mA	V_{CC} = 5.5V, Erasure in Progress
I_{PP4}(3)	V_{PP} Prog./Erase Verify Current		5.0	mA	$V_{PP} = V_{PPH}$, Program or Erase Verify in Progress
V_{IL}	Input Low Level TTL	–0.5	0.8	V	
V_{ILC}	Input Low Level CMOS	–0.5	0.8	V	
V_{OL}	Output Low Level		0.45	V	I_{OL} = 5.8mA, V_{CC} = 4.5V
V_{IH}	Input High Level TTL	2.0	V_{CC}+0.5	V	
V_{IHC}	Input High Level CMOS	0.7 V_{CC}	V_{CC}+0.5	V	
V_{OH}	Output High Level TTL	2.4		V	I_{OH} = –2.5mA, V_{CC} = 4.5V
V_{OH1}	Output High Level CMOS	0.85 V_{CC}		V	I_{OH} = –2.5mA, V_{CC} = 4.5V
V_{OH2}	Output High Level CMOS	V_{CC}–0.4		V	I_{OH} = –400µA, V_{CC} = 4.5V
V_{ID}	A_9 Signature Voltage	11.4	13.0	V	$A_9 = V_{ID}$
I_{ID}	A_9 Signature Current		200	µA	$A_9 = V_{ID}$
V_{LO}	V_{CC} Erase/Prog. Lockout Voltage	2.5		V	

Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.

SUPPLY CHARACTERISTICS

Symbol	Parameter	Limits		Unit
		Min	Max.	
V_{CC}	V_{CC} Supply Voltage	4.5	5.5	V
V_{PPL}	V_{PP} During Read Operations	0	6.5	V
V_{PPH}	V_{PP} During Read/Erase/Program	11.4	12.6	V

A.C. CHARACTERISTICS, Read Operation

CAT28F020 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT28F020I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	28F020-12 28F020I-12		28F020-15 28F020I-15		28F020-20 28F020I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	120		150		200		ns
t_{CE}	$\overline{CE}$ Access Time		120		150		200	ns
t_{ACC}	Address Access Time		120		150		200	ns
t_{OE}	$\overline{OE}$ Access Time		50		55		60	ns
t_{OH}	Output Hold from Address $\overline{OE}$/$\overline{CE}$ Change	0		0		0		ns
t_{OLZ}[3][9]	$\overline{OE}$ to Output in Low-Z	0		0		0		ns
t_{LZ}[3][9]	$\overline{CE}$ to Output in Low-Z	0		0		0		ns
t_{DF}[3][5]	$\overline{OE}$ High to Output High-Z		30		35		40	ns
t_{EHQZ}[3][5]	$\overline{CE}$ High to Output High-Z		55		55		55	ns
t_{WHGL}[3]	Write Recovery Time Before Read	6		6		6		µs

Figure 1. A.C. Testing Input/Output Waveform[6][7][8]

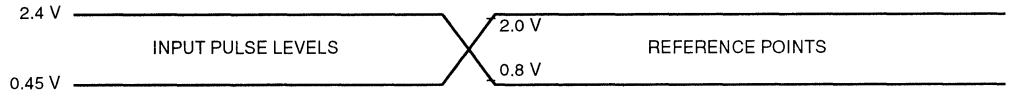

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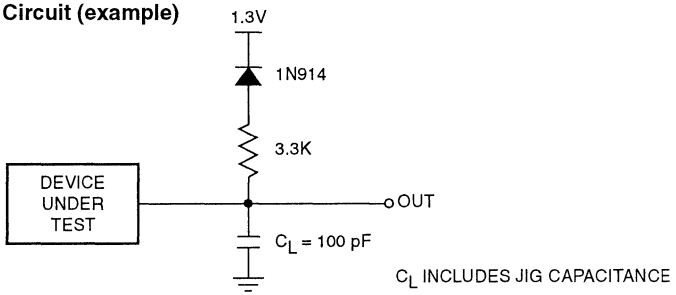
Figure 2. A.C. Testing Load Circuit (example)



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Note:
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(5) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
(6) Input Rise and Fall Times (10% to 90%) < 10 ns.
(7) Input Pulse Levels = 0.45V and 2.4V.
(8) Input and Output Timing Reference = 0.8V and 2.0V.
(9) Low-Z is defined as the state where the external data may be driven by the output buffer but may not be valid.

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A.C. CHARACTERISTICS, Program/Erase Operation

CAT28F020 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT28F020I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	28F020-12 28F020I-12		28F020-15 28F020I-15		28F020-20 28F020I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	120		150		200		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	60		60		75		ns
t_{DS}	Data Setup Time	50		50		50		ns
t_{DH}	Data Hold Time	10		10		10		ns
t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{WP}	$\overline{WE}$ Pulse Width	60		60		60		ns
t_{WPH}	$\overline{WE}$ High Pulse Width	20		20		20		ns
t_{WPWH1}(11)	Program Pulse Width	10		10		10		µs
t_{WPWH2}(11)	Erase Pulse Width	9.5		9.5		9.5		ms
t_{WPGL}	Write Recovery Time Before Read	6		6		6		µs
t_{GHWL}	Read Recovery Time Before Write	0		0		0		µs
t_{VPEL}	V_{PP} Setup Time to $\overline{CE}$	100		100		100		ns

ERASE AND PROGRAMMING PERFORMANCE(10)

Parameter	28F020-12 28F020I-12			28F020-15 28F020I-15			28F020-20 28F020I-20			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Erase Time(12)(14)		1.0	10		1.0	10		1.0	30	sec
Chip Program Time(12)(13)		4	25		4	25		4	25	sec

Note:
(10) Please refer to Supply characteristics for the value of V_{PPH} and V_{PPL}. The V_{PP} supply can be either hardwired or switched. If V_{PP} is switched, V_{PPL} can be ground, less than V_{CC} + 2.0V or a no connect with a resistor tied to ground.
(11) Program and Erase operations are controlled by internal stop timers.
(12) 'Typicals' are not guaranteed, but based on characterization data. Data taken at 25°C, 12.0V V_{PP}.
(13) Minimum byte programming time (excluding system overhead) is 16 µs (10 µs program + 6 µs write recovery), while maximum is 400 µs/byte (16 µs x 25 loops). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
(14) Excludes 00H Programming prior to Erasure.

FUNCTION TABLE(15)

Mode	Pins					Notes
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	I/O	
Read	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	D_{OUT}	
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	High-Z	
Standby	V_{IH}	X	X	V_{PPL}	High-Z	
Signature (MFG)	V_{IL}	V_{IL}	V_{IH}	X	31H	$A_0 = V_{IL}$, $A_9 = 12V$
Signature (Device)	V_{IL}	V_{IL}	V_{IH}	X	BDH	$A_0 = V_{IL}$, $A_9 = 12V$
Program/Erase	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	D_{IN}	See Command Table
Write Cycle	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	D_{IN}	During Write Cycle
Read Cycle	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	D_{OUT}	During Write Cycle

WRITE COMMAND TABLE

Commands are written into the command register in one or two write cycles. The command register can be altered only when V_{PP} is high and the instruction byte is latched on the rising edge of $\overline{WE}$. Write cycles also internally latch addresses and data required for programming and erase operations.

Mode	Pins						
	First Bus Cycle			Second Bus Cycle			
	Operation	Address	D_{IN}	Operation	Address	D_{IN}	D_{OUT}
Set Read	Write	X	00H	Read	Any		D_{OUT}
Read Sig. (MFG)	Write	X	90H	Read	00		31H
Read Sig. (Device)	Write	X	90H	Read	01		BDH
Erase	Write	X	20H	Write	X	20H	
Erase Verify	Write	X	A0H	Read	X		D_{OUT}
Program	Write	X	40H	Write	A_{IN}	D_{IN}	
Program Verify	Write	X	C0H	Read	X		D_{OUT}
Reset	Write	X	FFH	Write	X	FFH	

Note:
(15) Logic Levels: X = Logic 'Do not care' (V_{IH}, V_{IL}, V_{PPL}, V_{PPH})

8

READ OPERATIONS

Read Mode

A Read operation is performed with both $\overline{CE}$ and $\overline{OE}$ low and with $\overline{WE}$ high. V_{PP} can be either high or low, however, if V_{PP} is high, the Set READ command has to be sent before reading data (see Write Operations). The data retrieved from the I/O pins reflects the contents of the memory location corresponding to the state of the 18 address pins. The respective timing waveforms for the read operation are shown in Figure 3. Refer to the AC Read characteristics for specific timing parameters.

Signature Mode

The signature mode allows the user to identify the IC manufacturer and the type of device while the device resides in the target system. This mode can be activated in either of two ways; through the conventional method of applying a high voltage (12V) to address pin A_9 or by sending an instruction to the command register (see Write Operations).

The conventional mode is entered as a regular READ mode by driving the $\overline{CE}$ and $\overline{OE}$ pins low (with $\overline{WE}$ high) and applying the required high voltage on address pin A_9 while all other address lines are held at V_{IL}.

A Read cycle from address 0000H retrieves the binary code for the IC manufacturer on outputs I/O_0 to I/O_7:

CATALYST Code = 00110001 (31H)

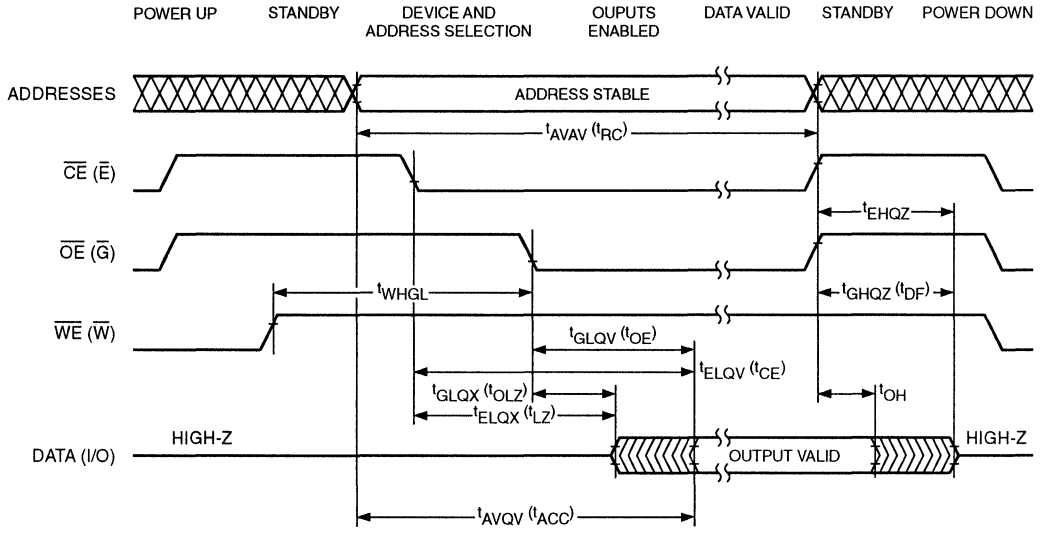
A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F020/28F020I Code = 1011 1101 (BDH)

Standby Mode

With $\overline{CE}$ at a logic-high level, the CAT28F020/ CAT28F020I is placed in a standby mode where most of the device circuitry is disabled, thereby substantially reducing power consumption. The outputs are placed in a high-impedance state.

Figure 3. A.C. Timing for Read Operation



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WRITE OPERATIONS

The following operations are initiated by observing the sequence specified in the Write Command Table.

Read Mode

The device can be put into a standard READ mode by initiating a write cycle with 00H on the data bus. The subsequent read cycles will be performed similar to a standard EPROM or E^2PROM Read.

Signature Mode

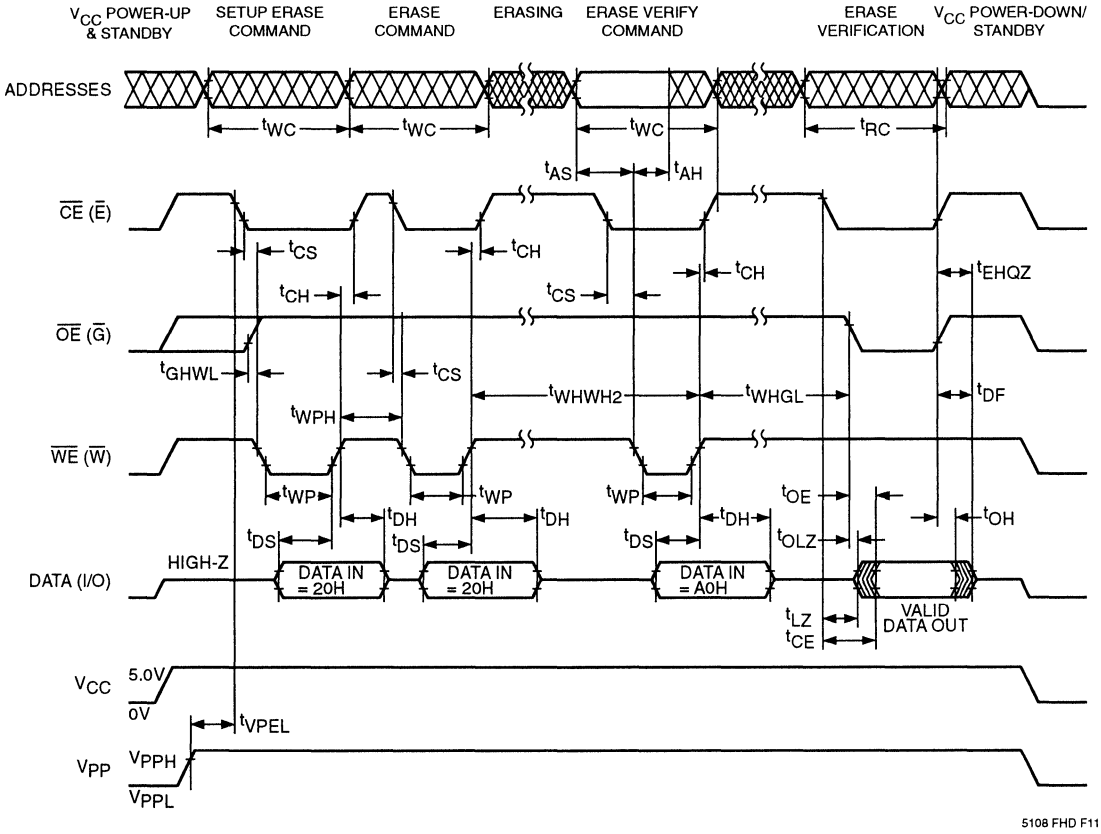
An alternative method for reading device signature (see Read Operations Signature Mode), is initiated by writing the code 90H into the command register while keeping V_{PP} high. A read cycle from address 0000H with $\overline{CE}$ and $\overline{OE}$ low (and $\overline{WE}$ high) will output the device signature.

CATALYST Code = 00110001 (31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F020/28F020I Code = 1011 1101 (BDH)

Figure 4. A.C. Timing for Erase Operation



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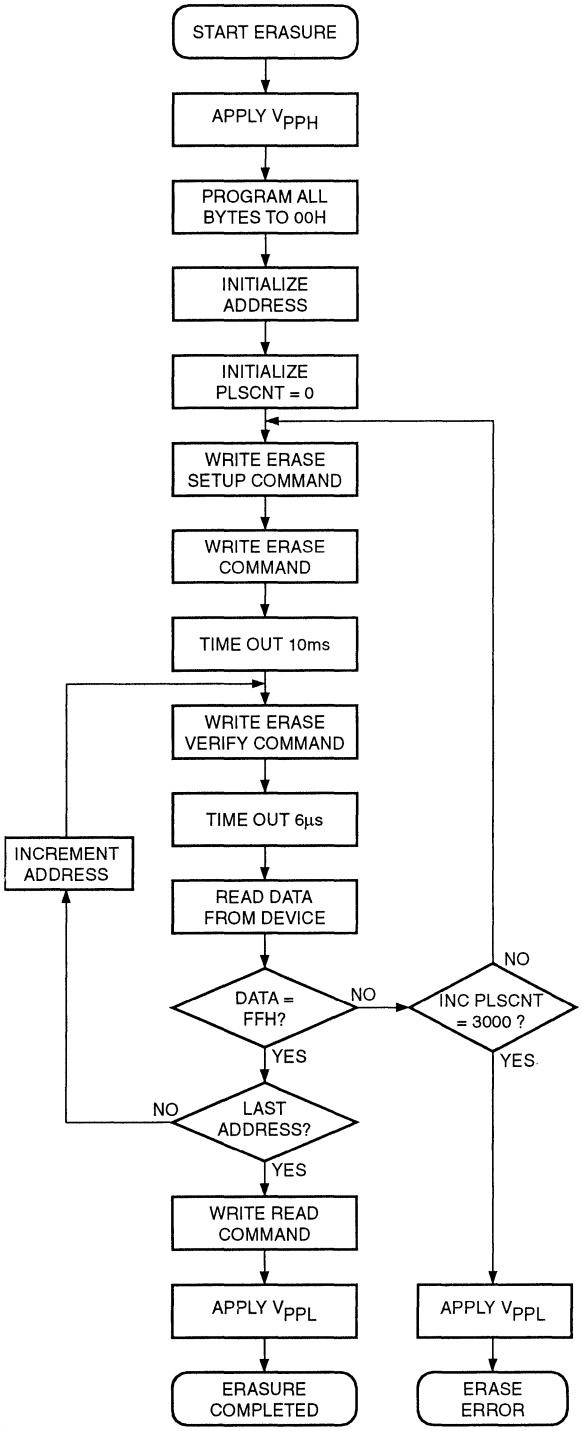
Erase Mode

During the first Write cycle, the command 20H is written into the command register. In order to commence the erase operation, the identical command of 20H has to be written again into the register. This two-step process ensures against accidental erasure of the memory contents. The final erase cycle will be stopped at the rising edge of $\overline{WE}$, at which time the Erase Verify command (A0H) is sent to the command register. During this cycle the address to be verified is sent to the address bus and latched when $\overline{WE}$ goes high. An integrated stop time allows for automatic timing control over this operation eliminating the need for a maximum erase timing specification. Refer to AC Characteristics (Program/Erase for specific timing parameters.

TIMING PARAMETER SYMBOLS

Standard	JEDEC	Standard	JEDEC
t_{AS}	t_{AVWL}	t_{LZ}	t_{ELQX}
t_{AH}	t_{WLAX}	t_{OE}	t_{GLQV}
t_{CE}	t_{ELQV}	t_{OLZ}	t_{GLQX}
t_{CH}	t_{WHEH}	t_{RC}	t_{AVAV}
t_{CS}	t_{ELWL}	t_{WC}	t_{AVAV}
t_{DF}	t_{GHQZ}	t_{WP}	t_{WLWH}
t_{DH}	t_{WHDX}	t_{WPH}	t_{WHWL}
t_{DS}	t_{DVWH}		

Figure 5. Chip Erase Algorithm(16)



BUS OPERATION	COMMAND	COMMENTS
		V_{PP} RAMPS TO V_{PPH} (OR V_{PP} HARDWIRED)
STANDBY		ALL BYTES SHALL BE PROGRAMMED TO 00 BEFORE AN ERASE OPERATION
		INITIALIZE ADDRESS
		PLSCNT = PULSE COUNT
WRITE	ERASE	ACTUAL ERASE NEEDS 10ms PULSE, DATA = 20H
WRITE	ERASE	DATA = 20H
		WAIT
WRITE	ERASE VERIFY	ADDRESS = BYTE TO VERIFY DATA = 20H; STOPS ERASE OPERATION
		WAIT
READ		READ BYTE TO VERIFY ERASURE
STANDBY		COMPARE OUTPUT TO FF INCREMENT PULSE COUNT
WRITE	READ	DATA = 00H RESETS THE REGISTER FOR READ OPERATION
STANDBY		V_{PP} RAMPS TO V_{PPL} (OR V_{PP} HARDWIRED)

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Note:
(16) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

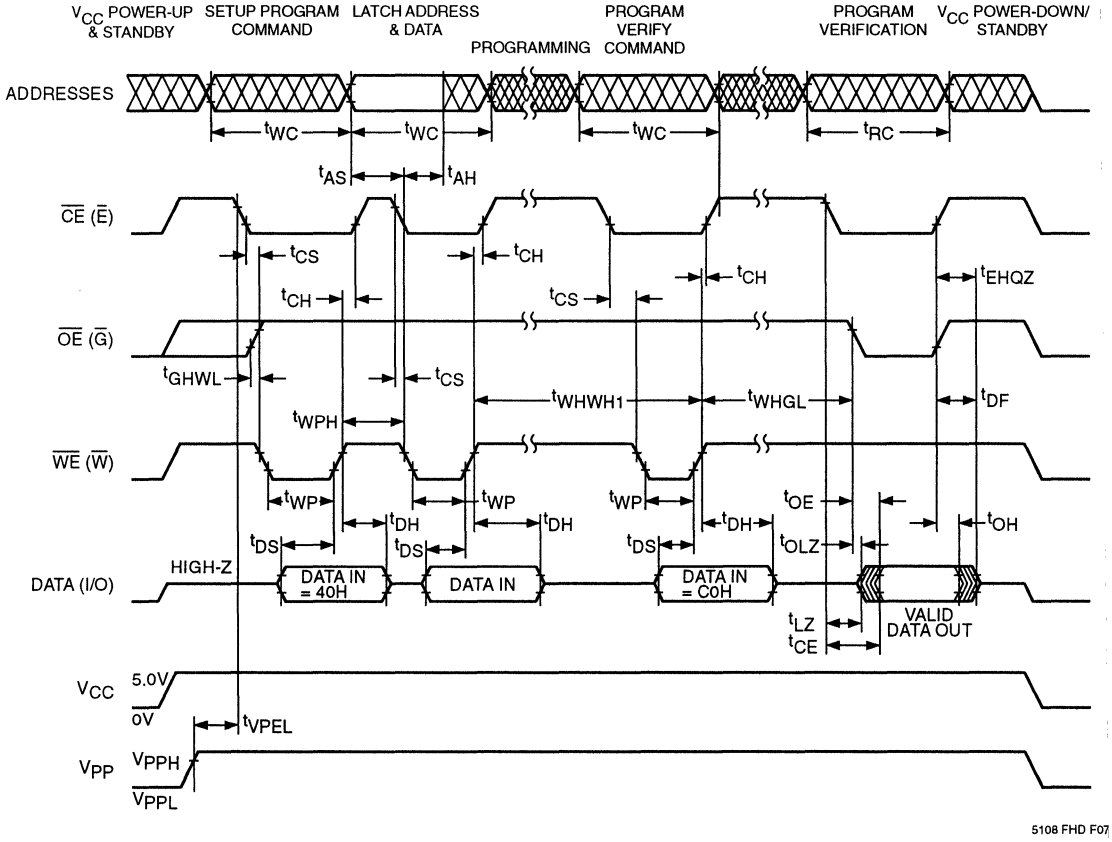
Erase-Verify Mode

The Erase-verify operation is performed on every byte after each erase pulse to verify that the bits have been erased.

Programming Mode

The programming operation is initiated using the programming algorithm of Figure 7. During the first write cycle, the command 40H is written into the command register. During the second write cycle, the address c the memory location to be programmed is latched on th falling edge of $\overline{WE}$, while the data is latched on the risin edge of $\overline{WE}$. The program operation terminates with th next rising edge of $\overline{WE}$. An integrated stop timer allow for automatic timing control over this operation, eliminat ing the need for a maximum program timing specifica tion. Refer to AC Characteristics (Program/Erase) fo specific timing parameters.

Figure 6. A.C. Timing for Programming Operation



Program-Verify Mode

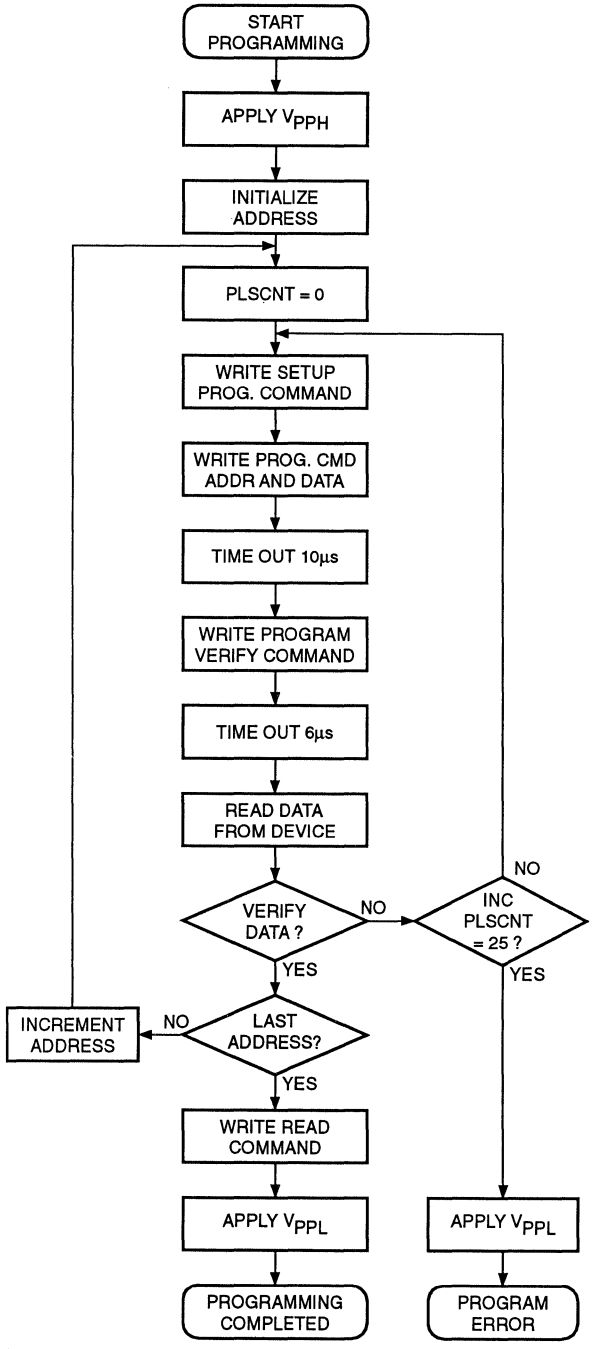
A Program-verify cycle is performed to ensure that all bits have been correctly programmed following each byte programming operation. The specific address is already latched from the write cycle just completed, and stays latched until the verify is completed. The Program-verify operation is initiated by writing C0H into the command register. An internal reference generates the necessary high voltages so that the user does not need to modify V_{CC}. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

TIMING PARAMETER SYMBOLS

Standard	JEDEC	Standard	JEDEC
t_{AS}	t_{AVWL}	t_{LZ}	t_{ELQX}
t_{AH}	t_{WLAX}	t_{OE}	t_{GLQV}
t_{CE}	t_{ELQV}	t_{OLZ}	t_{GLQX}
t_{CH}	t_{WHEH}	t_{RC}	t_{AVAV}
t_{CS}	t_{ELWL}	t_{WC}	t_{AVAV}
t_{DF}	t_{GHQZ}	t_{WP}	t_{WLWH}
t_{DH}	t_{WHDX}	t_{WPH}	t_{WHWL}
t_{DS}	t_{DVWH}		

8

Figure 7. Programming Algorithm(16)



BUS OPERATION	COMMAND	COMMENTS
STANDBY		V_{PP} RAMPS TO V_{PPH} (OR V_{PP} HARDWIRED)
		INITIALIZE ADDRESS
		INITIALIZE PULSE COUNT PLSCNT = PULSE COUNT
1ST WRITE CYCLE	WRITE SETUP	DATA = 40H
2ND WRITE CYCLE	PROGRAM	VALID ADDRESS AND DATA
		WAIT
1ST WRITE CYCLE	PROGRAM VERIFY	DATA = C0H
		WAIT
READ		READ BYTE TO VERIFY PROGRAMMING
STANDBY		COMPARE DATA OUTPUT TO DATA EXPECTED
1ST WRITE CYCLE	READ	DATA = 00H SETS THE REGISTER FOR READ OPERATION
STANDBY		V_{PP} RAMPS TO V_{PPL} (OR V_{PP} HARDWIRED)

Note:
(16) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

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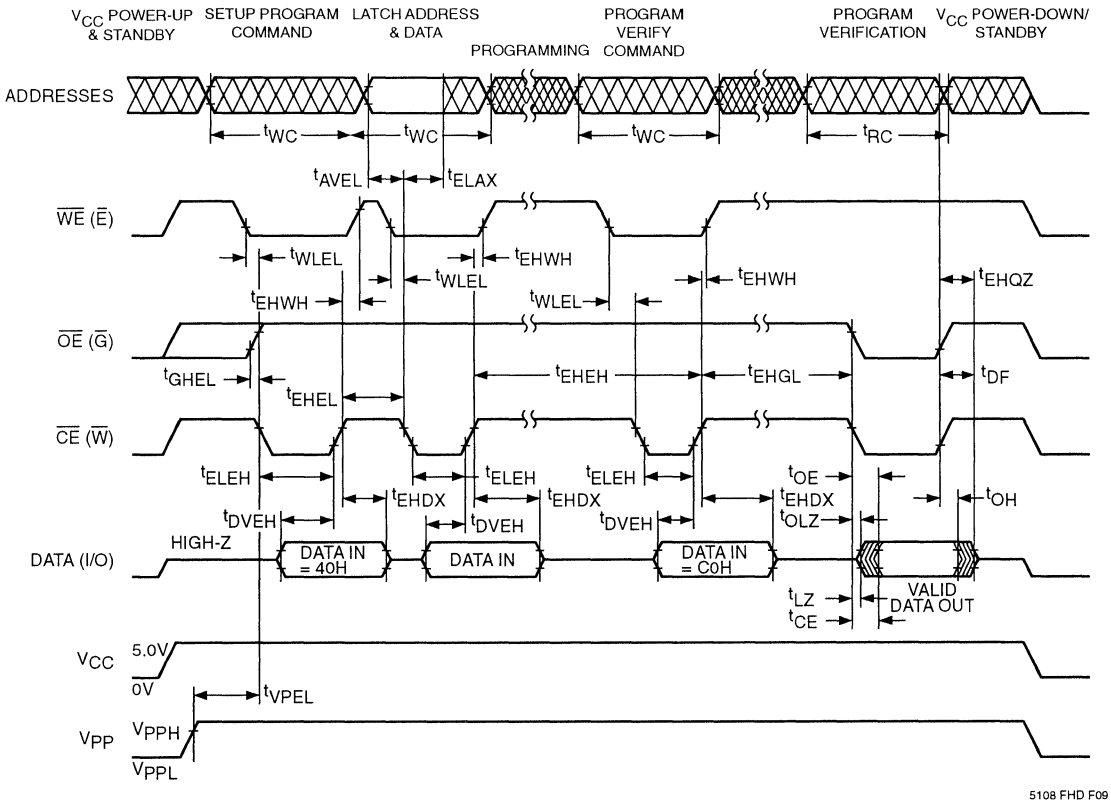
Abort/Reset

An Abort/Reset command is available to allow the user to safely abort an erase or program sequence. Two consecutive program cycles with FFH on the data bus will abort an erase or a program operation. The abort/reset operation can interrupt at any time in a program or erase operation and the device is reset to the Read Mode.

Figure 8. Alternate A.C. Timing for Program Operation



POWER UP/DOWN PROTECTION

The CAT28F020/CAT28F020I offers protection against inadvertent programming during V_{PP} and V_{CC} power transitions. When powering up the device there is no power-on sequencing necessary. In other words, V_{PP} and V_{CC} may power up in any order. Additionally V_{PP} may be hardwired to V_{PPH} independent of the state of V_{CC} and any power up/down cycling. The internal command register of the CAT28F020/CAT28F020I is reset to the Read Mode on power up.

POWER SUPPLY DECOUPLING

To reduce the effect of transient power supply voltage spikes, it is good practice to use a 0.1µF ceramic capacitor between V_{CC} and V_{SS} and V_{PP} and V_{SS}. These high-frequency capacitors should be placed as close as possible to the device for optimum decoupling.

TIMING PARAMETER SYMBOLS

Standard	JEDEC
t_{WC}	t_{AVAV}
t_{OLZ}	t_{GLQX}
t_{LZ}	t_{ELQX}
t_{CE}	t_{ELQV}
t_{DE}	t_{ELQV}
t_{DF}	t_{GHQZ}

ALTERNATE $\overline{CE}$-CONTROLLED WRITES

Symbol	Parameter	28F020-12 28F020I-12		28F020-15 28F020I-15		28F020-20 28F020I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	Write Cycle Time	120		150		200		ns
t_{AVEL}	Address Setup Time	0		0		0		ns
t_{ELAX}	Address Hold Time	80		80		95		ns
t_{DVEH}	Data Setup Time	50		50		50		ns
t_{EHDX}	Data Hold Time	10		10		10		ns
t_{EHGL}	Write Recovery Time Before Read	6		6		6		µs
t_{GHEL}	Read Recovery Time Before Write	0		0		0		µs
t_{WLEL}	$\overline{WE}$ Setup Time Before $\overline{CE}$	0		0		0		ns
t_{EHWH}	Write Enable Hold Time	0		0		0		ns
t_{ELEH}	Write Pulse Width	70		70		80		ns
t_{EHEL}	Write Pulse Width High	20		20		20		ns
t_{VPEL}	V_{PP} Setup Time to $\overline{CE}$ Low	1.0		1.0		1.0		µs

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CATALYST SEMICONDUCTOR

Product Information 1

2-Wire Bus Serial E^2PROMs 2

3-Wire Bus Serial E^2PROMs 3

SPI Bus Serial E^2PROMs 4

4-Wire Bus Serial E^2PROMs 5

Secure Access Serial E^2PROMs 6

Parallel E^2PROMs 7

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SECTION 9 EPROMS

CAT27HC256L/CAT27HC256LI ..... 32K x 8 ..... 256K-Bit 9-1

CAT27C210/CAT27C210I ..... 64K x 16 ..... 1M-Bit 9-13

CAT27HC256L/CAT27HC256LI

256K-Bit HIGH SPEED CMOS EPROM

FEATURES

- Fast Read Access Times:
  - –55/70/90/120ns (Commercial)
  - –70/90/120ns (Industrial)
- Single 5V Supply—Read Mode
- Low Power CMOS Dissipation:
  - –Active: 50 mA (Commercial)
    60 mA (Industrial)
  - –Standby: 100 μA
- High Speed Programming: 100 μs/byte
- CMOS and TTL Compatible I/O
- 12.5V Programming Level
- JEDEC Standard Pinouts:
  - –28 pin DIP and CERDIP
  - –32 pin LCC
  - –32 pin PLCC
- Electronic Signature

DESCRIPTION

The CAT27HC256L/CAT27HC256LI is a high speed low power 32K x 8 bits UV erasable and electronically reprogrammable EPROM ideally suited for high speed applications. Any byte can be accessed in less than 55ns making this device compatible with high performance microprocessor systems by eliminating the need for speed-robbing wait states.

The Quick-Pulse[1] programming algorithm reduces the time required to program the chip and ensures more reliable programming. The CAT27HC256L/CAT27HC256LI is used in applications where fast turnaround and pattern experimentation are important requirements.

The CAT27HC256L/CAT27HC256LI is manufactured using Catalyst's advanced CMOS floating gate technology. The device is available in JEDEC approved 28 pin DIP and CERDIP, 32 pin LCC and 32 pin PLCC packages. The transparent lid on the 28 pin CERDIP and 32 pin LCC allows the user the option of UV erasing the bit pattern in the device, thus allowing a new pattern to be written in.

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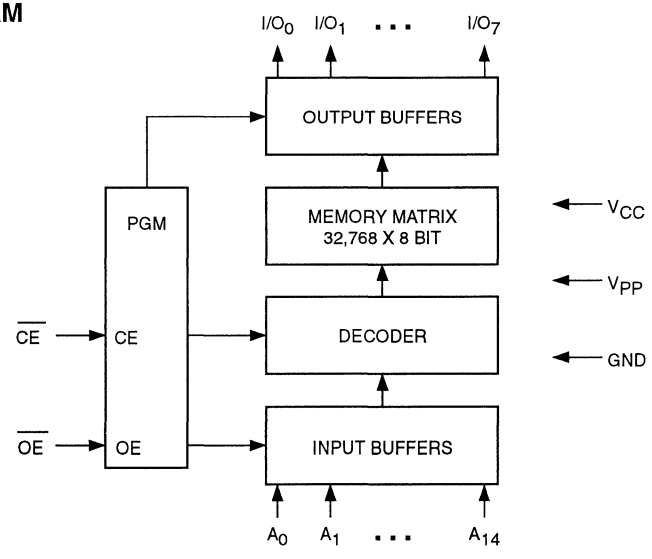
BLOCK DIAGRAM



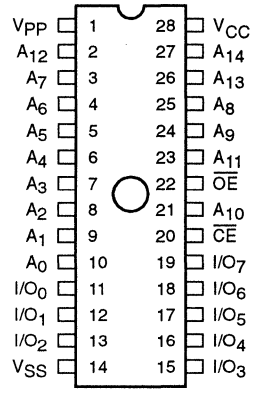
5129 FHD F08

Note:
(1) Quick-Pulse is a trademark of Intel Corporation.

TD 5129

PIN CONFIGURATION

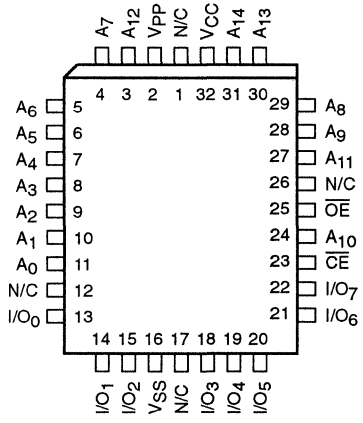
DIP and CERDIP Package



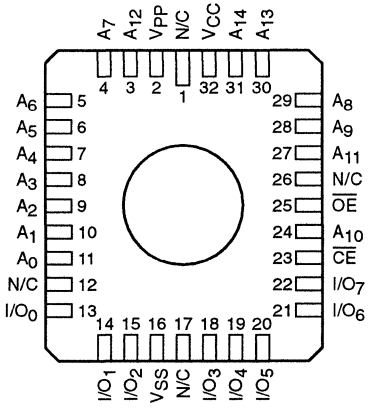
PIN FUNCTIONS

A_0–A_{14}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
I/O_0–I/O_7	Data Inputs/Outputs
NC	No Connect
V_{PP}	Program Supply Voltage
V_{CC}	5V Supply

PLCC Package



LCC Package



5129 FHD F01

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(3) ..... –2.0V to V_{CC} +2.0V

Voltage on Pin A_9 with Respect to Ground(3) ..... –2.0V to +13.5V

V_{PP} with Respect to Ground during Program/Erase ..... –2.0V to +14.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (T_A = 25°C) ..... 1.0 W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short-Circuit Current(4) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
V_{ZAP}(2)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(2)(5)	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V
C_{OUT}(2)	Output Pin Capacitance	10	pF	V_{OUT} = 0V
CV_{PP}(2)	V_{PP} Supply Capacitance	25	pF	V_{PP} = 0V

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Note:
(2) This parameter is tested initially and after a design or process change.
(3) The minimum DC input voltage is –0.5. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20 ns.
(4) Output shorted for no more than one second. No more than one output shorted at a time.
(5) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} + 1V.

D.C. OPERATING CHARACTERISTICS, Read Operation

CAT27HC256L T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT27HC256LI T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter		Limits Min.	Typ.	Max.	Units	Test Conditions
I_{CC}[6]	V_{CC} Operating Current (TTL)	Com.			50	mA	$\overline{CE}$ = V_{IL}, f = 5MHz All I/O's Open
		Ind.			60		
I_{CCC}[6]	V_{CC} Operating Current (CMOS)	Com.			50	mA	$\overline{CE}$ = V_{ILC}, f = 5MHz All I/O's Open
		Ind.			60		
I_{SB1}	V_{CC} Standby Current (TTL)	Com.			2	mA	$\overline{CE}$ = V_{IL}
		Ind.			3		
I_{SB2}	V_{CC} Standby Current (CMOS)	Com.			100	µA	$\overline{CE}$ = V_{IL}
		Ind.			100		
I_{LI}	Input Leakage Current				10	µA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current				10	µA	V_{OUT} = 5.5V
I_{PP1}	V_{PP} Leakage Current				10	µA	V_{PP} = 5.5V
V_{IH}	Input High Level TTL		2.0		V_{CC} +0.5	V	
V_{IL}	Input Low Level TTL		–0.5		0.8	V	
V_{OH}	Output Voltage High Level		2.4			V	I_{OH} = –1.0 mA
V_{OL}	Output Voltage Low Level				0.40	V	I_{OL} = 4.0 mA
V_{ILC}	Input Low Level CMOS		–0.5		0.30	V	
V_{IHC}	Input High Level CMOS		V_{CC} – 0.5		V_{CC} +0.5	V	

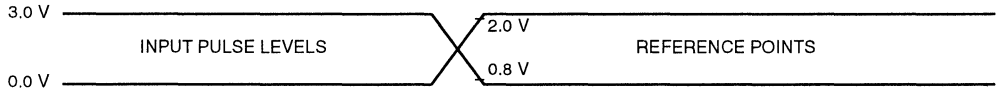
Note:
(6) The maximum current value is with outputs I/O_0 to I/O_7 unloaded.

A.C. CHARACTERISTICS, Read Operation

CAT27HC256L T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT27HC256LI T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

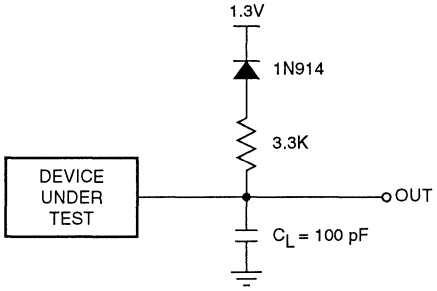
Symbol	Parameter	27HC256L-55[7]		27HC256L-70 27HC256LI-70		27HC256L-90 27HC256LI-90		27HC256L-12 27HC256LI-12		Unit
		Min	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address Access Time		55		70		90		120	ns
t_{CE}	$\overline{CE}$ to Output Delay		55		70		90		120	ns
t_{OE}	$\overline{OE}$ to Output Delay		30		35		40		50	ns
t_{OH}[2][8]	Output Hold A, $\overline{OE}$, $\overline{CE}$	0		0		0		0		ns
t_{DF}[2][8]	$\overline{OE}$ High to High-Z Output	0	30	0	35	0	40	0	50	ns

Figure 1. A.C. Testing Input/Output Waveform[9]



5129 FHD F02

Figure 2. A.C. Testing Load Circuit (example)



C_L INCLUDES JIG CAPACITANCE

5129 FHD F03

Note:
(2) This parameter is tested initially and after a design or process change.
(7) V_{CC} = 5V ±5% for CAT27HC256L-55.
(8) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
(9) Input rise and fall times (10% to 90%) <10ns.

D.C. CHARACTERISTICS, Programming Operation

CAT27HC256L T_A = 25°C ±5°C
CAT27HC256LI T_A = 25°C ±5°C

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
V_{CC}(11)	Supply Voltage (Quick Pulse Algorithm)	6.0	6.25	6.5	V	
	Supply Voltage (Intelligent Algorithm)	5.75	6.0	6.25	V	
V_{PP}(10)(11)	Programming Voltage (Quick Pulse Algorithm)	12.5	12.75	13.0	V	
	Programming Voltage (Intelligent Algorithm)	12.0	12.5	13.0	V	
I_{CCP}(6)	V_{CC} Supply Current Program and Verify			80	mA	$\overline{CE}$ = V_{IL}
I_{PP}(6)	V_{PP} Supply Current Program Operation			40	mA	$\overline{CE}$ = V_{IL}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 5.25V
V_{IL}	Input Low-Level TTL	–0.50		0.80	V	
V_{ILC}	Input Low-Level CMOS	–0.50		0.30	V	
V_{IH}	Input High-Level TTL	2.0		V_{CC} + 0.5	V	
V_{IHC}	Input High-Level CMOS	V_{CC} – 0.50		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Verify)			0.40	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage (Verify)	2.4			V	I_{OH} = 1.0 mA
V_H(6)(10)	A_9 Signature Mode Voltage	11.5		12.5	V	

Note:
(6) The maximum current value is with outputs I/O_0 to I/O_7 unloaded.
(10) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
(11) When programming, a 0.1 µF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.

A.C. CHARACTERISTICS, Programming Operation

CAT27HC256L T_A = 25°C ±5°C
CAT27HC256LI T_A = 25°C ±5°C

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
t_{AS}	Address Setup Time	2			µs	
t_{OES}	$\overline{OE}$ Setup Time	2			µs	
t_{DS}	Data Setup Time	2			µs	
t_{AH}	Address Hold Time	0			µs	
t_{DH}	Data Hold Time	2			µs	
t_{VPS}(10)	V_{PP} Setup Time	2			µs	
t_{VCS}(10)	V_{CC} Setup Time	2			µs	
t_{PW}	$\overline{CE}$ Program Pulse Width (Quick Pulse Algorithm)	95	100	105	µs	
t_{PW}	$\overline{CE}$ Program Pulse Width (Intelligent Algorithm)	0.95	1.0	1.05	ms	
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width (Intelligent Algorithm)	2.85		78.5	ms	
t_{DFP}(2)(8)	$\overline{OE}$ High to Output High-Z	0		130	ns	
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

Note:
2) This parameter is tested initially and after a design or process change.
8) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
10) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

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FUNCTION TABLE

Mode	Pins					
	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	A_0 (10)	A_9 (24)	I/O
Read	V_{IL}	V_{IL}	V_{CC}	X	X	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{CC}	X	X	High-Z
Standby	V_{IH}	X	V_{CC}	X	X	High-Z
Program	V_{IL}	V_{IH}	V_{PP}	X	X	D_{IN}
Program Verify	V_{IH}	V_{IL}	V_{PP}	X	X	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	X	X	High-Z
Signature MFG.	V_{IL}	V_{IL}	V_{CC}	V_{IL}	V_H	31H
Signature Device	V_{IL}	V_{IL}	V_{CC}	V_{IH}	V_H	40H

NOTES ON THE FUNCTION TABLE

Logic Levels: V_{IH} = TTL Logic 1 level
V_{IL} = TTL Logic 0 level
X = Logic "Do not care," V_{IH} or V_{IL}

Supply Voltage: V_{PP} = Programming/High-Voltage
V_{CC} = Read/Low-Voltage
V_H = 12.0V ±0.5V

Read: Read Mode: The content of the addressed memory byte is placed on the I/O pins I/O_0 to I/O_7.

Output Disable: Device is selected (active mode), programming is disabled and I/O_0 to I/O_7 output buffers are tristated (PMOS and NMOS drivers turned-off).

Standby: Device is deselected, low power dissipation.

Program: Byte Programming Mode: Logic zeros in the bit pattern driving the I/O_0 to I/O_7 data input buffers are written into the respective memory cells of the addressed byte.

Program Verify: Following a programming cycle, to verify the cell contents of the memory byte being programmed (not recommended as a normal read operation).

Program Inhibit: $\overline{CE}$ set to logic one and $\overline{OE}$ set to logic one prevents programming and deselects the device.

Signature MFG: Signature mode with all other addresses at V_{IL}, code of IC manufacturer (Catalyst) output on I/O pins I/O_0 to I/O_7.

Signature Device: Signature mode with all other addresses at V_{IL}, code of IC type output on I/O pins I/O_0 to I/O_7.

DEVICE OPERATION

Read Operation and Standby Modes

Memory access for reading an address location is controlled by $\overline{CE}$ and $\overline{OE}$. Chip enable $\overline{CE}$ is used independently of all other input signals as the primary device selection. In the logic zero state (TTL level V_{IL}), $\overline{CE}$ powers up all inputs and enables internal circuitry. In the logic one state (CMOS level V_{IHC}) $\overline{CE}$ places the device in standby mode, all DC paths to ground are shut-off, and the power dissipation is reduced to a minimum. A logic one on Output Enable $\overline{OE}$ disables the output buffers and places the output pads in a high impedance state. Assuming that the address lines A_0 to A_{14} have been stable for a time equal to $t_{ACC} - t_{OE}$, the output data is available after a delay of t_{OE} from the falling edge of $\overline{OE}$.

Signature Mode

The Signature Mode allows one to identify the IC manufacturer and the device type. This mode is entered as a regular Read Mode by driving the $\overline{CE}$ and $\overline{OE}$ inputs low, and additionally driving the A_9 pin to high-voltage (V_H) with all other address lines at V_{IL}.

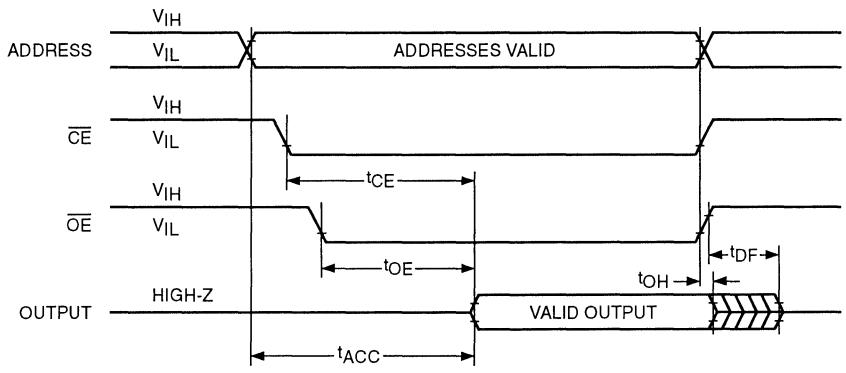
Driving A_0 to V_{IL} with all other addresses at V_{IL}, gives the the binary code of the IC manufacturer on outputs I/O_0 to I/O_7.

CATALYST Code:
0 0 1 1 0 0 0 1 (31H)

Driving A_0 to V_{IH} with all other addresses at V_{IL}, gives the the binary code of the device type on outputs I/O_0 to I/O_7.

27HC256L/27HC256LI Code:
0 1 0 0 0 0 0 0 (40H)

Figure 3. Read Operation Timing



5129 FHD F04

Programming Mode

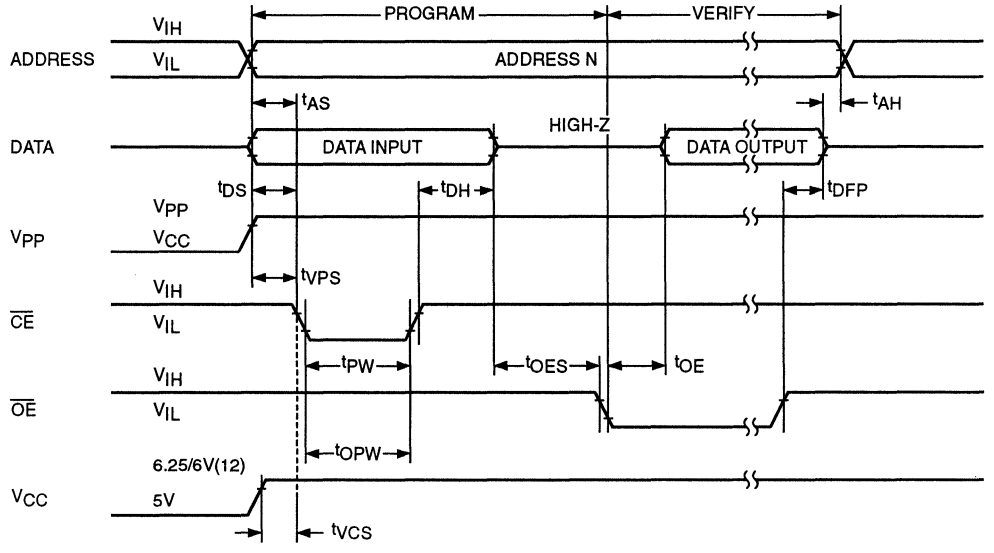
After a proper erase operation, all bits of the EPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. The programming mode is entered by raising $\overline{CE}$ and $\overline{OE}$ to a high level and bringing the low voltage supply pin (V_{CC}), followed by the high voltage supply pin (V_{PP}), to their respective programming levels.

After the address inputs A_0 to A_{14} and data inputs I/O_0 to I/O_7 are stabilized, $\overline{CE}$ is switched from the logic one to logic zero state to perform the programming. The particular memory cells of the addressed byte, corresponding to the 0's of the input data bits, are then programmed.

A Program Verify cycle is performed after each byte is programmed to ensure that the zero bits have been correctly written. The byte verification cycle is initiated by keeping $\overline{CE}$ at V_{IH} and switching $\overline{OE}$ from V_{IH} to V_{IL} while all other pin voltages remain unchanged. In most cases a single 100µs programming cycle is sufficient to set a memory cell in the logic zero state. The Quick Pulse algorithm is recommended as the preferred device programming operation. The CAT27HC256L/ CAT27HC256LI is also compatible with Intelligent Programming(13).

The flow charts for both the algorithms are given in Figures 5 and 6.

Figure 4. Programming Operation Timing



5129 FHD F05

Note:
(12) V_{CC} = 6.25V ±0.25V for Quick Pulse algorithm; 6.0V ±0.25V for Intelligent Programming algorithm.
(13) Intelligent is a trademark of Intel Corporation.

U.V. ERASURE OPERATION FOR CERDIP EPROMS

Direct exposure to fluorescent lamps such as those used in room light fixtures, can erase the CAT27HC256L/CAT27HC256LI EPROM in less than three years. When exposed to direct sun light the EPROM can be erased in less than a week.

The recommended erasure procedure is to expose the CAT27HC256L/CAT27HC256LI EPROM to a standard ultraviolet light with a wavelength of 2537 Angstroms. The integrated dose for proper erasure is 15 Wsec/cm^2.

The erasure time with this dosage is approximately 15 to 60 minutes using an ultraviolet lamp with a 1200 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes.

The maximum integrated dose a CAT27HC256L/CAT27HC256LI EPROM can be exposed to is 7258 Wsec/cm^2 (one week at 1200 uW/cm^2). Exposure of the device to higher U.V. doses may cause permanent damage and loss of functionality.

Figure 5. Quick Pulse Algorithm

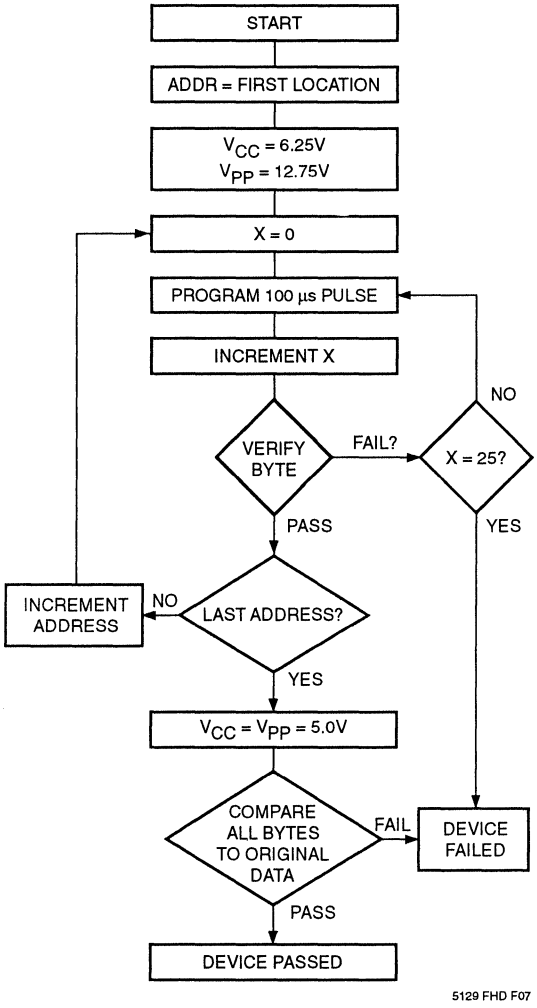
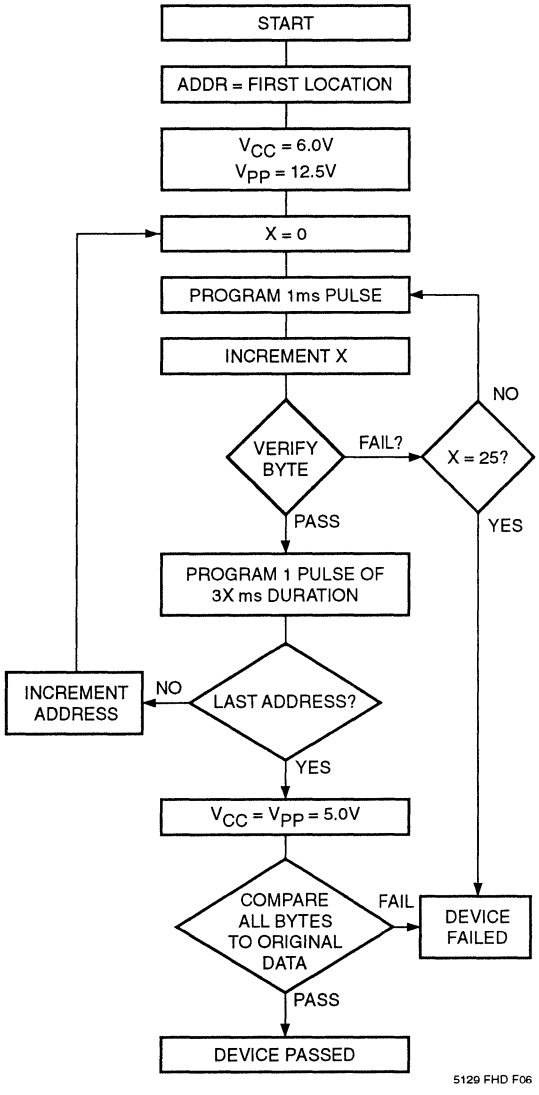


Figure 6. Intelligent Programming Algorithm



9

CAT27C210/CAT27C210I

1 Megabit HIGH SPEED CMOS EPROM

FEATURES

- Fast Read Access Times:
  - –150/170/200/250ns (Commercial)
  - –170/200/250ns (Industrial)
- Single 5V Supply—Read Mode
- Low Power CMOS Dissipation:
  - –Active: 50 mA (Commercial)
    60 mA (Industrial)
  - –Standby: 100 μA
- High Speed Programming: 100 μs/word
- CMOS and TTL Compatible I/O
- 12.5V Programming Level
- JEDEC Standard Pinouts:
  - –40 pin DIP and CERDIP
  - –44 pin PLCC
- Electronic Signature

DESCRIPTION

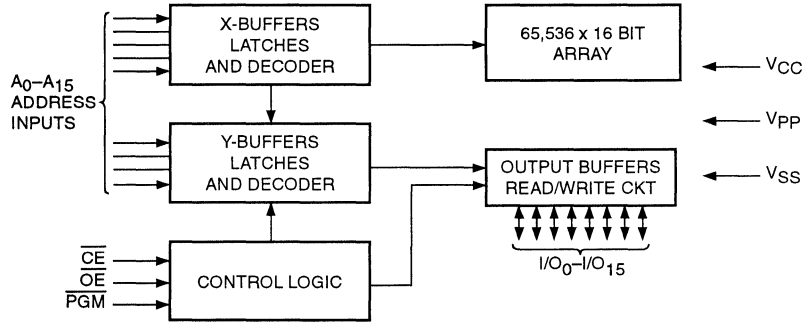
The CAT27C210/CAT27C210I is a high speed low power 64K x 16 bits UV erasable and electronically reprogrammable EPROM ideally suited for high speed applications. Any word can be accessed in less than 150ns making this device compatible with high performance microprocessor systems by eliminating the need for speed-robbing wait states.

The Quick-Pulse(1) programming algorithm reduces the time required to program the chip and ensures more reliable programming. The CAT27C210/CAT27C210I is used in applications where fast turnaround and pattern experimentation are important requirements.

The CAT27C210/CAT27C210I is manufactured using Catalyst's advanced CMOS floating gate technology. The device is available in JEDEC approved 40 pin DIP and CERDIP and 44 pin PLCC packages. The transparent lid on the 40 pin CERDIP allows the user the option of UV erasing the bit pattern in the device, thus allowing a new pattern to be written in.

9

BLOCK DIAGRAM



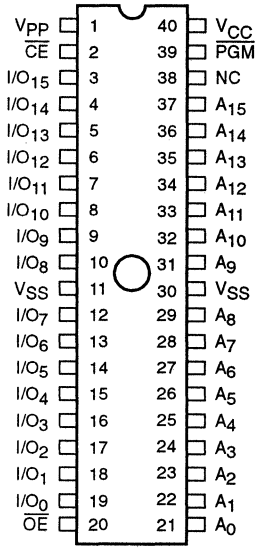
5131 FHD F08

Note:
(1) Quick-Pulse is a trademark of Intel Corporation.

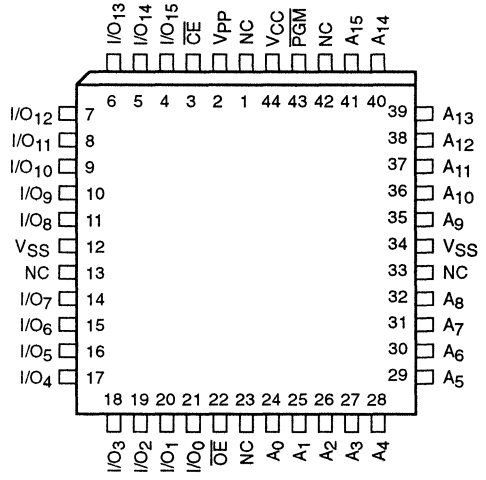
TD 5131

PIN CONFIGURATION

DIP and CERDIP Package



PLCC Package



5131 FHD F01

PIN FUNCTIONS

A_0–A_{15}	Addresses
I/O_0–I/O_{15}	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Write Enable
NC	No Connect
V_{PP}	Program Supply Voltage
V_{CC}	5V Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(3) ..... –2.0V to V_{CC} +2.0V

Voltage on Pin A_9 with Respect to Ground(3) ..... –2.0V to +13.5V

V_{PP} with Respect to Ground during Program/Erase ..... –2.0V to +14.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (T_A = 25°C) ..... 1.0 W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short-Circuit Current(4) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
V_{ZAP}(2)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(2)(5)	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V
C_{OUT}(2)	Output Pin Capacitance	10	pF	V_{OUT} = 0V
CV_{PP}(2)	V_{PP} Supply Capacitance	25	pF	V_{PP} = 0V

Note:
(2) This parameter is tested initially and after a design or process change.
(3) The minimum DC input voltage is –0.5. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20 ns.
(4) Output shorted for no more than one second. No more than one output shorted at a time.
(5) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} + 1V.

9

D.C. OPERATING CHARACTERISTICS, Read Operation

CAT27C210 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT27C210I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter		Limits Min.	Typ.	Max.	Units	Test Conditions
I_{CC}[6]	V_{CC} Operating Current (TTL)	Com.			60	mA	$\overline{CE}$ = V_{IL}, f = 5MHz All I/O's Open
		Ind.			70		
I_{CCC}[6]	V_{CC} Operating Current (CMOS)	Com.			50	mA	$\overline{CE}$ = V_{ILC}, f = 5MHz All I/O's Open
		Ind.			60		
I_{SB1}	V_{CC} Standby Current (TTL)	Com.			1	mA	$\overline{CE}$ = V_{IL}
		Ind.			1		
I_{SB2}	V_{CC} Standby Current (CMOS)	Com.			100	µA	$\overline{CE}$ = V_{IL}
		Ind.			100		
I_{LI}	Input Leakage Current				1	µA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current				1	µA	V_{OUT} = 5.5V
I_{PP1}	V_{PP} Leakage Current				1	µA	V_{PP} = 5.5V
V_{IH}	Input High Level TTL		2.0		V_{CC} +0.5	V	
V_{IL}	Input Low Level TTL		–0.5		0.8	V	
V_{OH}	Output Voltage High Level		2.4			V	I_{OH} = –1.0 mA
V_{OL}	Output Voltage Low Level				0.40	V	I_{OL} = 4.0 mA
V_{ILC}	Input Low Level CMOS		–0.5		0.30	V	
V_{IHC}	Input High Level CMOS		V_{CC} – 0.5		V_{CC} +0.5	V	

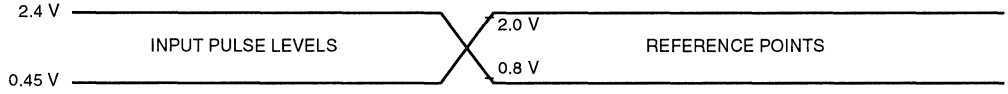
Note:
(6) The maximum current value is with outputs I/O_0 to I/O_{15} unloaded.

A.C. CHARACTERISTICS, Read Operation

CAT27C210 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT27C210I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

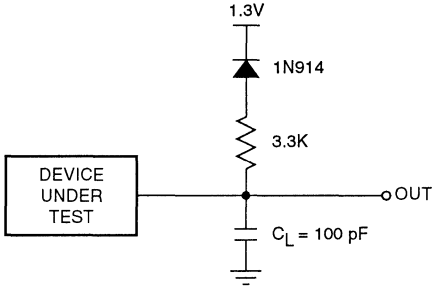
Symbol	Parameter	27C210-15		27C210-17 27C210I-17		27C210-20 27C210I-20		27C210-25 27C210I-25		Unit
		Min	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address Access Time		150		170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay		150		170		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay		60		70		80		100	ns
t_{OH}(2)(7)	Output Hold A, $\overline{OE}$, $\overline{CE}$	0		0		0		0		ns
t_{DF}(2)(7)	$\overline{OE}$ High to High-Z Output	0	35	0	40	0	50	0	60	ns

Figure 1. A.C. Testing Input/Output Waveform(8)



5131 FHD F02

Figure 2. A.C. Testing Load Circuit (example)



C_L INCLUDES JIG CAPACITANCE

5129 FHD F03

Note:
2) This parameter is tested initially and after a design or process change.
7) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
8) Input rise and fall times (10% to 90%) <10ns.

D.C. CHARACTERISTICS, Programming Operation

CAT27C210 T_A = 25°C ±5°C
CAT27C210I T_A = 25°C ±5°C

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
V_{CC}(10)	Supply Voltage (Quick Pulse Algorithm)	6.0	6.25	6.5	V	
	Supply Voltage (Intelligent Algorithm)	5.75	6.0	6.25	V	
V_{PP}(9)(10)	Programming Voltage (Quick Pulse Algorithm)	12.5	12.75	13.0	V	
	Programming Voltage (Intelligent Algorithm)	12.0	12.5	13.0	V	
I_{CCP}(6)	V_{CC} Supply Current Program and Verify			45	mA	$\overline{CE} = V_{IL}$
I_{PP}(6)	V_{PP} Supply Current Program Operation			40	mA	$\overline{CE} = V_{IL}$
I_{LI}	Input Leakage Current			10	µA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 5.25V
V_{IL}	Input Low-Level TTL	–0.50		0.80	V	
V_{ILC}	Input Low-Level CMOS	–0.50		0.30	V	
V_{IH}	Input High-Level TTL	2.0		V_{CC} + 0.5	V	
V_{IHC}	Input High-Level CMOS	V_{CC} – 0.50		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Verify)			0.40	V	I_{OL} = 2.4 mA
V_{OH}	Output High Voltage (Verify)	2.4			V	I_{OH} = –400 µA
V_H(6)(9)	A_9 Signature Mode Voltage	11.5		12.5	V	

Note:
(6) The maximum current value is with outputs I/O_0 to I/O_{15} unloaded.
(9) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
(10) When programming, a 0.1 µF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.

ι.C. CHARACTERISTICS, Programming Operation

:AT27C210 T_A = 25°C ±5°C
:AT27C210I T_A = 25°C ±5°C

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
t_{AS}	Address Setup Time	2			µs	
t_{OES}	$\overline{OE}$ Setup Time	2			µs	
t_{DS}	Data Setup Time	2			µs	
t_{AH}	Address Hold Time	0			µs	
t_{DH}	Data Hold Time	2			µs	
t_{VPS}(9)	V_{PP} Setup Time	2			µs	
t_{VCS}(9)	V_{CC} Setup Time	2			µs	
t_{PW}	$\overline{CE}$ Program Pulse Width (Quick Pulse Algorithm)	95	100	105	µs	
t_{PW}	$\overline{CE}$ Program Pulse Width (Intelligent Algorithm)	0.95	1.0	1.05	ms	
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width (Intelligent Algorithm)	2.85		78.5	ms	
t_{DFP}(2)(7)	$\overline{OE}$ High to Output High-Z	0		130	ns	
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

lote:
2) This parameter is tested initially and after a design or process change.
7) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
9) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

9

FUNCTION TABLE

Mode	Pins						
	$\overline{CE}$	$\overline{OE}$	V_{PP}	$\overline{PGM}$	A_0	A_9	I/O
Read	V_{IL}	V_{IL}	V_{CC}	X	X	X	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{CC}	X	X	X	High-Z
Standby	V_{IH}	X	V_{CC}	X	X	X	High-Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{IL}	X	X	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{PP}	V_{IH}	X	X	D_{OUT}
Program Inhibit	V_{IH}	X	V_{PP}	X	X	X	High-Z
Signature MFG.	V_{IL}	V_{IL}	V_{CC}	X	V_{IL}	V_H	0031H
Signature Device	V_{IL}	V_{IL}	V_{CC}	X	V_{IH}	V_H	0007H

NOTES ON THE FUNCTION TABLE

Logic Levels: V_{IH} = TTL Logic 1 level
V_{IL} = TTL Logic 0 level
X = Logic "Do not care," V_{IH} or V_{IL}

Supply Voltage: V_{PP} = Programming/High-Voltage
V_{CC} = Read/Low-Voltage
V_H = 12.0V ±0.5V

Read: Read Mode: The content of the addressed memory word is placed on the I/O pins I/O_0 to I/O_{15}.

Output Disable: Device is selected (active mode), programming is disabled and I/O_0 to I/O_{15} output buffers are tristated (PMOS and NMOS drivers turned-off).

Standby: Device is deselected, low power dissipation.

Program: Word Programming Mode: Logic zeros in the bit pattern driving the I/O_0 to I/O_{15} data input buffers are written into the respective memory cells of the addressed word.

Program Verify: Following a programming cycle, to verify the cell contents of the memory word being programmed (not recommended as a normal read operation).

Program Inhibit: $\overline{CE}$ set to logic one prevents programming and deselects the device.

Signature MFG: Signature mode with all other addresses at V_{IL}, code of IC manufacturer (Catalyst) output on I/O pins I/O_0 to I/O_{15}.

Signature Device: Signature mode with all other addresses at V_{IL}, code of IC type output on I/O pins I/O_0 to I/O_{15}

EVICE OPERATION

ead Operation and Standby Modes

emory access for reading an address location is con-
olled by $\overline{CE}$ and $\overline{OE}$. Chip enable $\overline{CE}$ is used indepen-
ently of all other input signals as the primary device
election. In the logic zero state (TTL level V_{IL}), $\overline{CE}$
owers up all inputs and enables internal circuitry. In the
gic one state (CMOS level V_{IHC}) $\overline{CE}$ places the device
standby mode, all DC paths to ground are shut-off,
nd the power dissipation is reduced to a minimum. A
gic one on Output Enable $\overline{OE}$ disables the output
uffers and places the output pads in a high impedance
ate. Assuming that the address lines A_0 to A_{15} have
een stable for a time equal to $t_{ACC} - t_{OE}$, the output data
available after a delay of t_{OE} from the falling edge of
$\overline{E}$.

Signature Mode

The Signature Mode allows one to identify the IC manufacturer and the device type. This mode is entered as a regular Read Mode by driving the $\overline{CE}$ and $\overline{OE}$ inputs low, and additionally driving the A_9 pin to high-voltage (V_H) with all other address lines at V_{IL}.

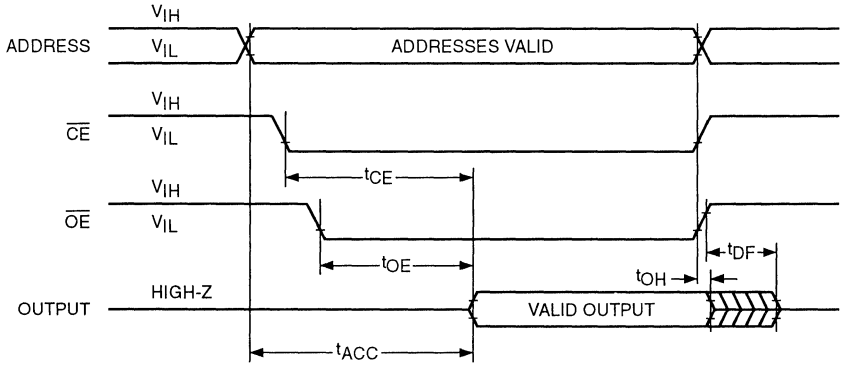
Driving A_0 to V_{IL} with all other addresses at V_{IL}, gives the the binary code of the IC manufacturer on outputs I/O_0 to I/O_{15}.

CATALYST Code:
0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 1 (0031H)

Driving A_0 to V_{IH} with all other addresses at V_{IL}, gives the the binary code of the device type on outputs I/O_0 to I/O_{15}.

27C210/27C210I Code:
0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 (0007H)

igure 3. Read Operation Timing



5129 FHD F04

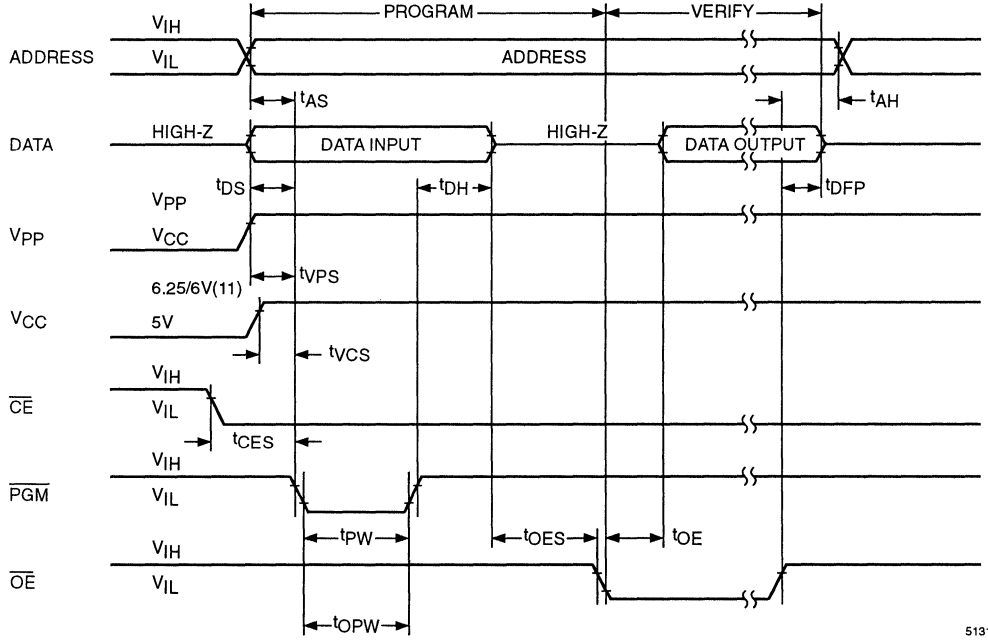
9

Programming Mode

As shipped, all the bits of the CAT27C210/CAT27C210I are in the logic "1" state. The device is programmed by selectively writing logic "0"s into the desired bit locations. To enter the programming mode, V_{CC} and V_{PP} must be adjusted to their programming levels, $\overline{CE}$ pulled to V_{IL}, and a program write pulse applied to the $\overline{PGM}$ pin. After the program write pulse, the programmed data may the be verified by enabling the outputs ($\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IL} and $\overline{PGM}$ = V_{IH}), then comparing the written data to th read data. This device is compatible with Intelligent™ (12 and the Quick-Pulse Programming™ algorithms.

The flow charts for both the algorithms are given i Figures 5 and 6.

Figure 4. Programming Operation Timing



Note:
(11) V_{CC} = 6.25V ±0.25V for Quick Pulse algorithm; 6.0V ±0.25V for Intelligent Programming algorithm.
(12) Intelligent is a trademark of Intel Corporation.

).V. ERASURE OPERATION FOR :ERDIP EPROMS

)irect exposure to fluorescent lamps such as those sed in room light fixtures, can erase the CAT27C210/ :AT27C210I EPROM in less than three years. When xposed to direct sun light the EPROM can be erased in ess than a week.

'he recommended erasure procedure is to expose the :AT27C210/CAT27C210I EPROM to a standard ultra- iolet light with a wavelength of 2537 Angstroms. The ntegrated dose for proper erasure is 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 60 minutes using an ultraviolet lamp with a 1200 µW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes.

The maximum integrated dose a CAT27C210/ CAT27C210I EPROM can be exposed to is 7258 Wsec/ cm^2 (one week at 1200 uW/cm^2). Exposure of the device to higher U.V. doses may cause permanent damage and loss of functionality.

'igure 5. Quick Pulse Algorithm

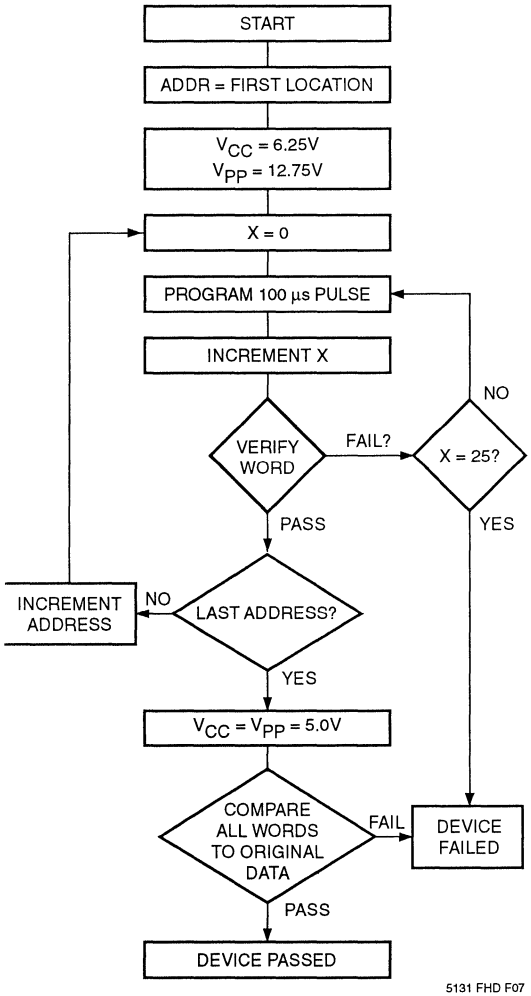
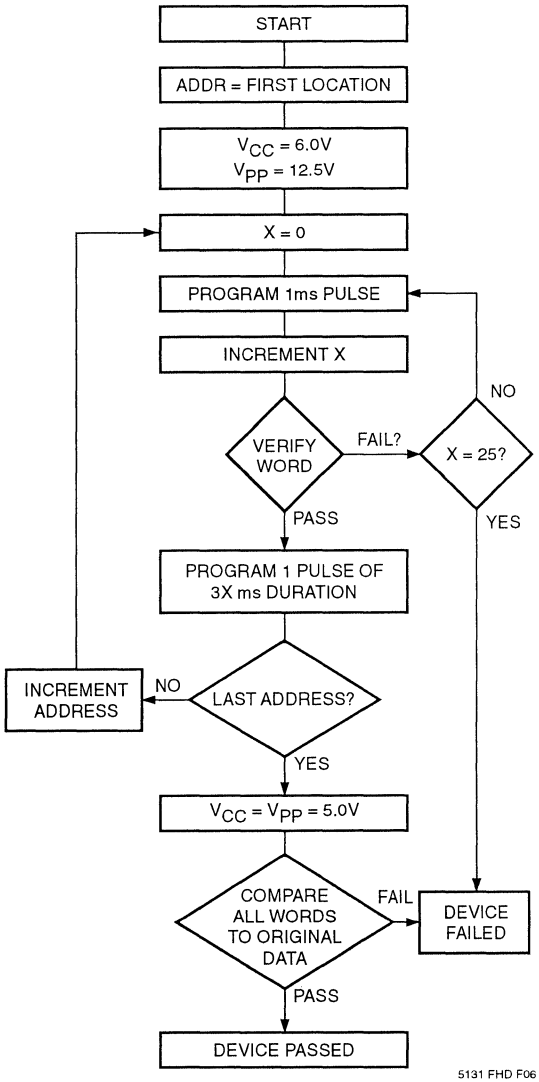


Figure 6. Intelligent Programming Algorithm



9

CATALYST SEMICONDUCTOR

Product Information 1

2-Wire Bus Serial E^2PROMs 2

3-Wire Bus Serial E^2PROMs 3

SPI Bus Serial E^2PROMs 4

4-Wire Bus Serial E^2PROMs 5

Secure Access Serial E^2PROMs 6

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SECTION 10 NVRAMS

CAT22C10/CAT22C10I ..... 64 x 4 ..... 256-Bit 10-1

CAT22C12/CAT22C12I ..... 256 x 4 ..... 1K-Bit 10-9

CAT24C44/CAT24C44I ..... 16 x 16 ..... 256-Bit 10-17

CAT22C10/CAT22C10I

56-Bit NONVOLATILE CMOS STATIC RAM

FEATURES

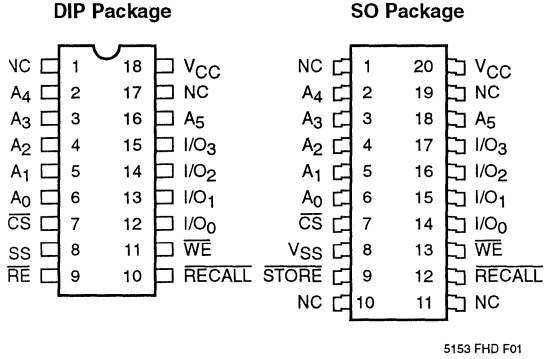
- Low Power CMOS Technology
- Single 5V Supply
- Fast RAM Access Times:
  - –200ns
  - –300ns
- Infinite E²PROM to RAM Recall
- CMOS and TTL Compatible I/O
- Power Up/Down Protection
- Low CMOS Power Consumption:
  - –Active: 40mA Max.
  - –Standby: 30µA Max.
- JEDEC Standard Pinouts:
  - –18 pin DIP
  - –20 pin SO
- 10,000 Program/Erase Cycles (E²PROM)
- 10 Year Data Retention

DESCRIPTION

The CAT22C10/CAT22C10I NVRAM is a 256 bit nonvolatile memory organized as 64 words x 4 bits. The high speed static RAM array is bit for bit backed up by a nonvolatile E²PROM array which allows for easy transfer of data from RAM array to E²PROM (STORE) and from E²PROM to RAM (RECALL). STORE operations are completed in 10ms max. and RECALL operations typically within 1.5µs. The CAT22C10/CAT22C10I features unlimited RAM write operations either through external RAM writes or internal recalls from E²PROM. Internal false store protection circuitry prohibits STORE operations when V_{CC} is less than 3.5V typ.

The CAT22C10/CAT22C10I is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles (E²PROM) and has a data retention of 10 years. The device is available in JEDEC approved 18 pin plastic DIP and 20 pin SO packages.

PIN CONFIGURATION



PIN FUNCTIONS

Pin Name	Function
A_0–A_5	Address
I/O_0–I/O_3	Data In/Out
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{RECALL}$	Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

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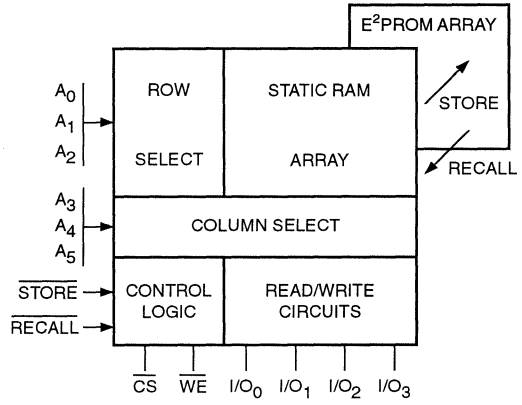
TD 5153

BLOCK DIAGRAM



5153 FHD F

MODE SELECTION(1)(2)(3)

Mode	Input				I/O
	$\overline{CS}$	$\overline{WE}$	$\overline{RECALL}$	$\overline{STORE}$	
Standby	H	X	H	H	Output High-Z
RAM Read	L	H	H	H	Output Data
RAM Write	L	L	H	H	Input Data
(E^2PROM→RAM)	X	H	L	H	Output High-Z RECALL
(E^2PROM→RAM)	H	X	L	H	Output High-Z RECALL
(RAM→E^2PROM)	X	H	H	L	Output High-Z STORE
(RAM→E^2PROM)	H	X	H	L	Output High-Z STORE

POWER-UP TIMING(4)

Symbol	Parameter	Min.	Max.	Units
VCCSR	V_{CC} Slew Rate	.5	.005	V/ms

Note:
(1) $\overline{RECALL}$ signal has priority over $\overline{STORE}$ signal when both are applied at the same time.
(2) $\overline{STORE}$ is inhibited when $\overline{RECALL}$ is active.
(3) The store operation is inhibited when V_{CC} is below ≈ 3.5V.
(4) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

emperature Under Bias ..... –55°C to +125°C

torage Temperature ..... –65°C to +150°C

oltage on Any Pin with
Respect to Ground(5) ..... -2.0 to +VCC +2.0V

cc with Respect to Ground ..... -2.0V to +7.0V

ackage Power Dissipation
Capability (Ta = 25°C) 1.0W

ead Soldering Temperature (10 secs) ..... 300°C

utput Short Circuit Current(6) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

ELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(4)	Endurance	10,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(4)	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(4)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(4)(7)	Latch-Up	100		mA	JEDEC Standard 17

.C. OPERATING CHARACTERISTICS

AT22C10 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
AT22C10I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.	Max.		
I_{CC}	Current Consumption (Operating)			40	mA	All Inputs = 5.5V T_A = 0°C All I/O's Open
I_{SB}	Current Consumption (Standby)			30	µA	$\overline{CS}$ = V_{CC} All I/O's Open
I_{LI}	Input Current			10	µA	0 ≤ V_{IN} ≤ 5.5V
I_{LO}	Output Leakage Current			10	µA	0 ≤ V_{OUT} ≤ 5.5V
V_{IH}	High Level Input Voltage	2.0		V_{CC}	V	
V_{IL}	Low Level Input Voltage	0.0		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –2mA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 4.2mA
V_{DH}	RAM Data Holding Voltage	1.5		5.5	V	V_{CC}

APACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Unit	Conditions
$C_{I/O}$(4)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance	6	pF	V_{IN} = 0V

lote:
4) This parameter is tested initially and after a design or process change that affects the parameter.
5) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
6) Output shorted for no more than one second. No more than one output shorted at a time.
7) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V_{CC} +1V.

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A.C. CHARACTERISTICS, Write Cycle

CAT22C10 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT22C10I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	22C10-20 22C10I-20		22C10-30 22C10I-30		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	200		300		ns	
t_{CW}	$\overline{CS}$ Write Pulse Width	150		150		ns	
t_{AS}	Address Setup Time	50		50		ns	C_L = 100pF
t_{WP}	Write Pulse Width	150		150		ns	+1TTL gate
t_{WR}	Write Recovery Time	25		25		ns	V_{OH} = 2.2V
t_{DW}	Data Valid Time	100		100		ns	V_{OL} = 0.65V
t_{DH}	Data Hold Time	0		0		ns	V_{IH} = 2.2V
t_{WZ}(4)	Output Disable Time		100		100	ns	V_{IL} = 0.65V
t_{OW}	Output Enable Time	0		0		ns	

A.C. CHARACTERISTICS, Read Cycle

CAT22C10 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT22C10I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	22C10-20 22C10I-20		22C10-30 22C10I-30		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	200		300		ns	C_L = 100pF
t_{AA}	Address Access Time		200		300	ns	+1TTL gate
t_{CO}	$\overline{CS}$ Access Time		200		300	ns	V_{OH} = 2.2V
t_{OH}	Output Data Hold Time	0		0		ns	V_{OL} = 0.65V
t_{LZ}(4)	$\overline{CS}$ Enable Time	0		0		ns	V_{IH} = 2.2V
t_{HZ}(4)	$\overline{CS}$ Disable Time		100		100	ns	V_{IL} = 0.65V

Note:
(4) This parameter is tested initially and after a design or process change that affects the parameter.

A.C. CHARACTERISTICS, Store Cycle

CAT22C10 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT22C10I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
t_{STC}	Store Time		10	ms	C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V
t_{STP}	Store Pulse Width	200		ns	
t_{STZ}[4]	Store Disable Time		100	ns	
t_{OST}[4]	Store Enable Time	0		ns	

A.C. CHARACTERISTICS, Recall Cycle

CAT22C10 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT22C10I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
t_{RCC}	Recall Cycle Time	1400		ns	C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V
t_{RCP}	Recall Pulse Width	300		ns	
t_{RCZ}	Recall Disable Time		100	ns	
t_{ORC}	Recall Enable Time	0		ns	
t_{ARC}	Recall Data Access Time		1100	ns	

Note:
(4) This parameter is tested initially and after a design or process change that affects the parameter.

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DEVICE OPERATION

The configuration of the CAT22C10/CAT22C10I allows a common address bus to be directly connected to the address inputs. Additionally, the Input/Output (I/O) pins can be directly connected to a common I/O bus if the bus has less than 1 TTL load and 100pF capacitance. If not, the I/O path should be buffered.

When the chip select ($\overline{CS}$) pin goes low, the device is activated. When $\overline{CS}$ is forced high, the device goes into the standby mode and consumes very little current. With the nonvolatile functions inhibited, the device operates like a Static RAM. The Write Enable ($\overline{WE}$) pin selects a write operation when $\overline{WE}$ is low and a read operation when $\overline{WE}$ is high. In either of these modes, an array byte (4 bits) can be addressed uniquely by using the address lines (A_0–A_5), and that byte will be read or written to through the Input/Output pins (I/O_0–I/O_3).

The nonvolatile functions are inhibited by holding the $\overline{STORE}$ input and the $\overline{RECALL}$ input high. When the $\overline{RECALL}$ input is taken low, it initiates a recall operation which transfers the contents of the entire E^2PROM array into the Static RAM. When the $\overline{STORE}$ input is taken low, it initiates a store operation which transfers the entire Static RAM array contents into the E^2PROM array.

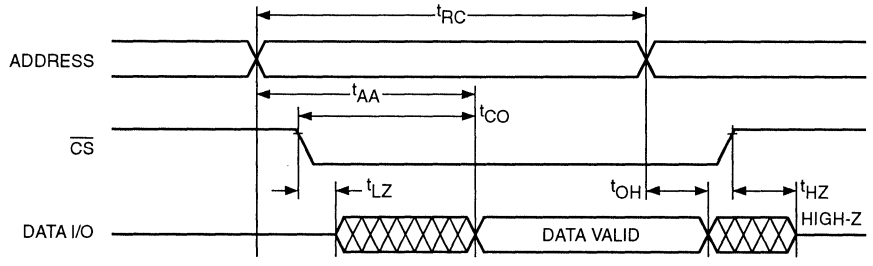
Standby Mode

The chip select ($\overline{CS}$) input controls all of the functions of the CAT22C10/CAT22C10I. When a high level is supplied to the $\overline{CS}$ pin, the device goes into the standby mode where the outputs are put into a high impendance state and the power consumption is drastically reduced. With I_{SB} less than 100µA in standby mode, the designer has the flexibility to use this part in battery operated systems.

Read

When the chip is enabled ($\overline{CS}$ = low), the nonvolatile functions are inhibited ($\overline{STORE}$ = high and $\overline{RECALL}$ = high). With the Write Enable ($\overline{WE}$) pin held high, the data in the Static RAM array may be accessed by selecting an address with input pins A_0–A_5. This will occur when the outputs are connected to a bus which is loaded by no more than 100pF and 1 TTL gate. If the loading is greater than this, some additional buffering circuitry is recommended.

Figure 1. Read Cycle Timing



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Write

With the chip enabled and the nonvolatile functions inhibited, the Write Enable ($\overline{WE}$) pin will select the write mode when driven to a low level. In this mode, the address must be supplied for the byte being written. After the set-up time (t_{AS}), the input data must be supplied to pins I/O_0–I/O_3. When these conditions, including the write pulse width time (t_{WP}) are met, the data will be written to the specified location in the static RAM. A write function may also be initiated from the standby mode by driving $\overline{WE}$ low, inhibiting the nonvolatile functions, supplying valid addresses, and then taking $\overline{CS}$ low and supplying input data.

Figure 2. Write Cycle Timing

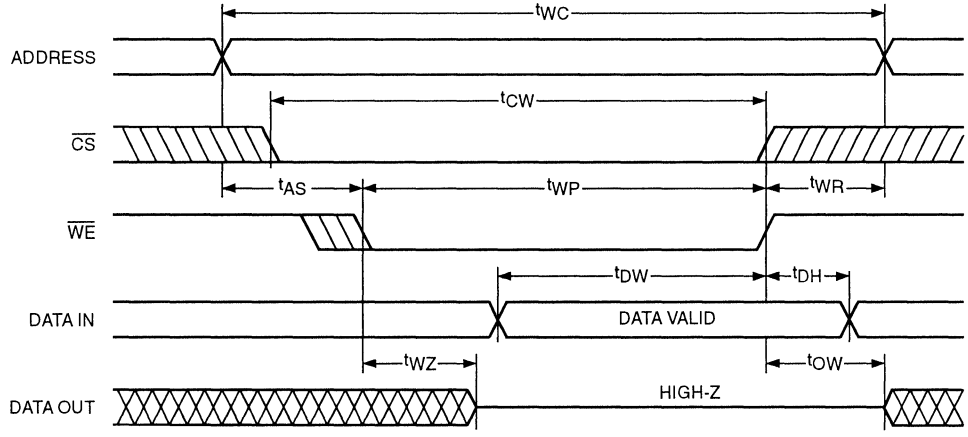

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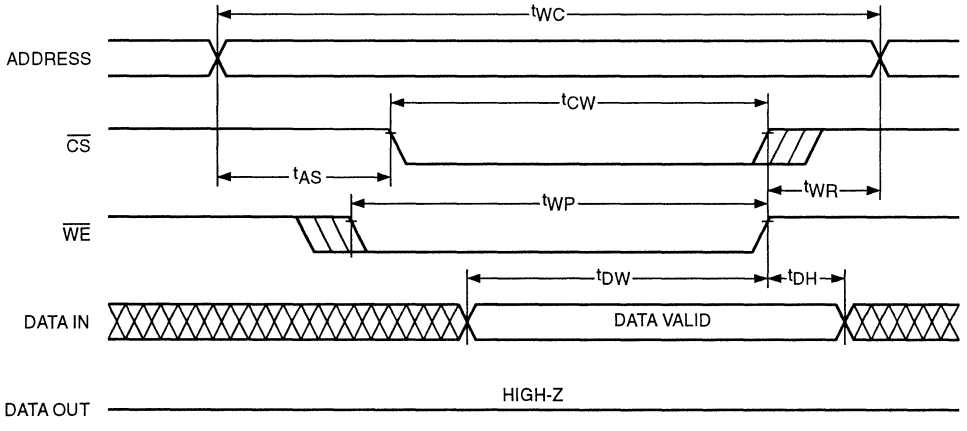
Figure 3. Early Write Cycle Timing



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Recall

At anytime, except during a store operation, taking the $\overline{\text{RECALL}}$ pin low will initiate a recall operation. This is independent of the state of $\overline{\text{CS}}$, $\overline{\text{WE}}$, or A_0–A_5. After the $\overline{\text{RECALL}}$ pin has been held low for the duration of the Recall Pulse Width (t_{RCP}), the recall will continue independent of any other inputs. During the recall, the entire contents of the E²PROM array is transferred to the Static RAM array. The first byte of data may be externally accessed after the recalled data access time from end of recall (t_{ARC}) is met. After this, any other byte may be accessed by using the normal read mode.

If the $\overline{\text{RECALL}}$ pin is held low for the entire Recall Cycle time (t_{RCC}), the contents of the Static RAM may be immediately accessed by using the normal read mode. A recall operation can be performed an unlimited number of times without affecting the integrity of the data.

The outputs I/O_0–I/O_3 will go into the high impedance state as long as the $\overline{\text{RECALL}}$ signal is held low.

Store

At any time, except during a recall operation, taking the $\overline{\text{STORE}}$ pin low will initiate a store operation. This takes place independent of the state of $\overline{\text{CS}}$, $\overline{\text{WE}}$ or A_0–A_5. Th $\overline{\text{STORE}}$ pin must be held low for the duration of the Stor Pulse Width (t_{STP}) to ensure that a store operation i initiated. Once initiated, the $\overline{\text{STORE}}$ pin becomes "Don't Care", and the store operation will complete it transfer of the entire contents of the Static RAM arra into the E²PROM array within the Store Cycle tim (t_{STC}). If a store operation is initiated during a write cycle the contents of the addressed Static RAM byte and it corresponding byte in the E²PROM array will be un known.

During the store operation, the outputs are in a hig impedance state. A minimum of 10,000 store operation can be performed reliably and the data written into th E²PROM array has a minimum data retention time of 1 years.

DATA PROTECTION DURING POWER-UP AND POWER-DOWN

The CAT22C10/CAT22C10I has on-chip circuitry whic will prevent a store operation from occurring when V_C falls below 3.5V typ. This function eliminates the poten tial hazard of spurious signals initiating a store operatio when the system power is below 3.5V typ.

Figure 4. Recall Cycle Timing

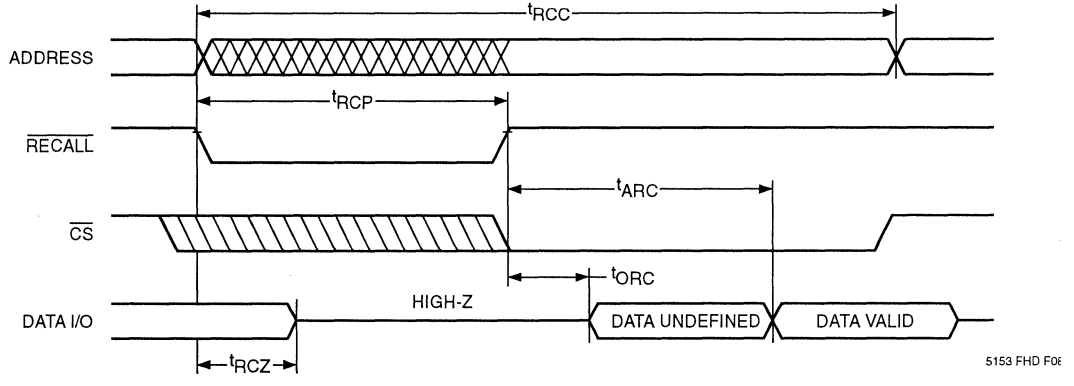
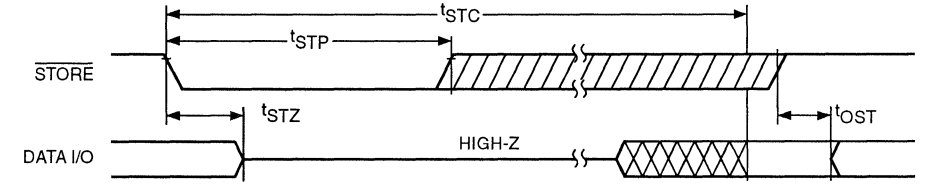


Figure 5. Store Cycle Timing



CAT22C12/CAT22C12I

1K-Bit NONVOLATILE CMOS STATIC RAM

FEATURES

- Low Power CMOS Technology
- Single 5V Supply
- Fast RAM Access Times:
  - –200ns
  - –300ns
- Infinite E²PROM to RAM Recall
- CMOS and TTL Compatible I/O
- Power Up/Down Protection
- Low CMOS Power Consumption:
  - –Active: 50mA Max.
  - –Standby: 30µA Max.
- JEDEC Standard Pinouts:
  - –18 pin DIP
- 10,000 Program/Erase Cycles (E²PROM)
- 10 Year Data Retention

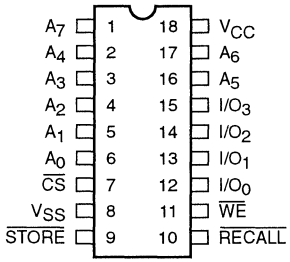
DESCRIPTION

The CAT22C12/CAT22C12I NVRAM is a 1K bit nonvolatile memory organized as 256 words x 4 bits. The high speed static RAM array is bit for bit backed up by a nonvolatile E²PROM array which allows for easy transfer of data from RAM array to E²PROM (STORE) and from E²PROM to RAM (RECALL). STORE operations are completed in 10ms max. and RECALL operations typically within 1.5µs. The CAT22C12/CAT22C12I features unlimited RAM write operations either through external RAM writes or internal recalls from E²PROM. Internal false store protection circuitry prohibits STORE operations when V_{CC} is less than 3.5V typ.

The CAT22C12/CAT22C12I is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles (E²PROM) and has a data retention of 10 years. The device is available in a JEDEC approved 18 pin plastic DIP package.

PIN CONFIGURATION

DIP Package



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PIN FUNCTIONS

Pin Name	Function
A_0–A_7	Address
I/O_0–I/O_3	Data In/Out
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{RECALL}$	Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground

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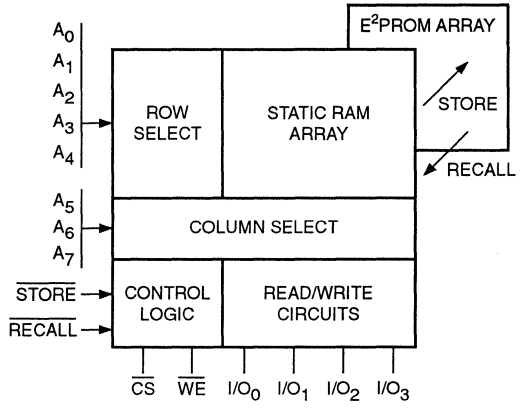
BLOCK DIAGRAM



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MODE SELECTION(1)(2)(3)

Mode	Input				I/O
	$\overline{CS}$	$\overline{WE}$	$\overline{RECALL}$	$\overline{STORE}$	
Standby	H	X	H	H	Output High-Z
RAM Read	L	H	H	H	Output Data
RAM Write	L	L	H	H	Input Data
(E^2PROM→RAM)	X	H	L	H	Output High-Z RECALL
(E^2PROM→RAM)	H	X	L	H	Output High-Z RECALL
(RAM→E^2PROM)	X	H	H	L	Output High-Z STORE
(RAM→E^2PROM)	H	X	H	L	Output High-Z STORE

POWER-UP TIMING(4)

Symbol	Parameter	Min.	Max.	Units
VCCSR	V_{CC} Slew Rate	.5	.005	V/ms

Note:
(1) $\overline{RECALL}$ signal has priority over $\overline{STORE}$ signal when both are applied at the same time.
(2) $\overline{STORE}$ is inhibited when $\overline{RECALL}$ is active.
(3) The store operation is inhibited when V_{CC} is below ≈ 3.5V.
(4) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–55°C to +125°C
Storage Temperature .....–65°C to +150°C
Voltage on Any Pin with
Respect to Ground(5) .....-2.0 to +VCC +2.0V
V_{CC} with Respect to Ground .....-2.0V to +7.0V
Package Power Dissipation
Capability (Ta = 25°C) 1.0W
Lead Soldering Temperature (10 secs) .....300°C
Output Short Circuit Current(6) .....100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(4)	Endurance	10,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(4)	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(4)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(4)(7)	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT22C12 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT22C12I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.	Max.		
I_{CC}	Current Consumption (Operating)			50	mA	All Inputs = 5.5V T_A = 0°C All I/O's Open
I_{SB}	Current Consumption (Standby)			30	µA	$\overline{CS}$ = V_{CC} All I/O's Open
I_{LI}	Input Current			2	µA	$0 \le V_{IN} \le 5.5V$
I_{LO}	Output Leakage Current			10	µA	$0 \le V_{OUT} \le 5.5V$
V_{IH}	High Level Input Voltage	2.0		V_{CC}	V	
V_{IL}	Low Level Input Voltage	0.0		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –2mA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 4.2mA
V_{DH}	RAM Data Holding Voltage	1.5		5.5	V	V_{CC}

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Unit	Conditions
$C_{I/O}$(4)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance	6	pF	V_{IN} = 0V

Note:
(4) This parameter is tested initially and after a design or process change that affects the parameter.
(5) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(6) Output shorted for no more than one second. No more than one output shorted at a time.
(7) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V_{CC} +1V.

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A.C. CHARACTERISTICS, Write Cycle

CAT22C12 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT22C12I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	22C12-20 22C12I-20		22C12-30 22C12I-30		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	200		300		ns	
t_{CW}	$\overline{CS}$ Write Pulse Width	150		150		ns	
t_{AS}	Address Setup Time	50		50		ns	C_L = 100pF
t_{WP}	Write Pulse Width	150		150		ns	+1TTL gate
t_{WR}	Write Recovery Time	25		25		ns	V_{OH} = 2.2V
t_{DW}	Data Valid Time	100		100		ns	V_{OL} = 0.65V
t_{DH}	Data Hold Time	0		0		ns	V_{IH} = 2.2V
t_{WZ}(4)	Output Disable Time		100		100	ns	V_{IL} = 0.65V
t_{OW}	Output Enable Time	0		0		ns	

A.C. CHARACTERISTICS, Read Cycle

CAT22C12 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT22C12I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	22C12-20 22C12I-20		22C12-30 22C12I-30		Unit	Conditions
		Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	200		300		ns	C_L = 100pF
t_{AA}	Address Access Time		200		300	ns	+1TTL gate
t_{CO}	$\overline{CS}$ Access Time		200		300	ns	V_{OH} = 2.2V
t_{OH}	Output Data Hold Time	0		0		ns	V_{OL} = 0.65V
t_{LZ}(4)	$\overline{CS}$ Enable Time	0		0		ns	V_{IH} = 2.2V
t_{HZ}(4)	$\overline{CS}$ Disable Time		100		100	ns	V_{IL} = 0.65V

Note:
(4) This parameter is tested initially and after a design or process change that affects the parameter.

A.C. CHARACTERISTICS, Store Cycle

CAT22C12 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT22C12I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
t_{STC}	Store Time		10	ms	
t_{STP}	Store Pulse Width	200		ns	C_L = 100pF + 1TTL gate
t_{STZ}(4)	Store Disable Time		100	ns	V_{OH} = 2.2V, V_{OL} = 0.65V
t_{OST}(4)	Store Enable Time	0		ns	V_{IH} = 2.2V, V_{IL} = 0.65V

A.C. CHARACTERISTICS, Recall Cycle

CAT22C12 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
CAT22C12I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
t_{RCC}	Recall Cycle Time	1400		ns	
t_{RCP}	Recall Pulse Width	300		ns	C_L = 100pF + 1TTL gate
t_{RCZ}	Recall Disable Time		100	ns	V_{OH} = 2.2V, V_{OL} = 0.65V
t_{ORC}	Recall Enable Time	0		ns	V_{IH} = 2.2V, V_{IL} = 0.65V
t_{ARC}	Recall Data Access Time		1100	ns	

Note:
(4) This parameter is tested initially and after a design or process change that affects the parameter.

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DEVICE OPERATION

The configuration of the CAT22C12/CAT22C12I allows a common address bus to be directly connected to the address inputs. Additionally, the Input/Output (I/O) pins can be directly connected to a common I/O bus if the bus has less than 1 TTL load and 100pF capacitance. If not, the I/O path should be buffered.

When the chip select ($\overline{CS}$) pin goes low, the device is activated. When $\overline{CS}$ is forced high, the device goes into the standby mode and consumes very little current. With the nonvolatile functions inhibited, the device operates like a Static RAM. The Write Enable ($\overline{WE}$) pin selects a write operation when $\overline{WE}$ is low and a read operation when $\overline{WE}$ is high. In either of these modes, an array byte (4 bits) can be addressed uniquely by using the address lines (A_0–A_7), and that byte will be read or written to through the Input/Output pins (I/O_0–I/O_3).

The nonvolatile functions are inhibited by holding the $\overline{STORE}$ input and the $\overline{RECALL}$ input high. When the $\overline{RECALL}$ input is taken low, it initiates a recall operation which transfers the contents of the entire E^2PROM array into the Static RAM. When the $\overline{STORE}$ input is taken low, it initiates a store operation which transfers the entir Static RAM array contents into the E^2PROM array.

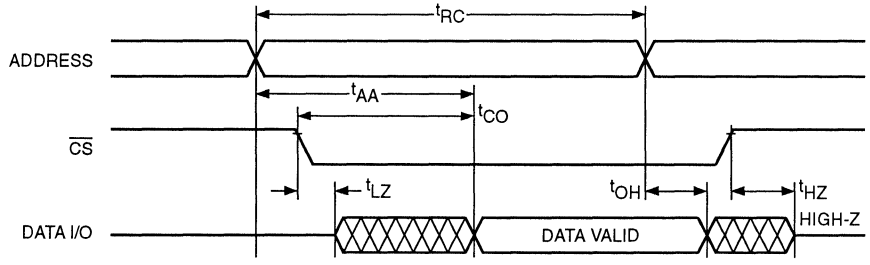
Standby Mode

The chip select ($\overline{CS}$) input controls all of the functions c the CAT22C12/CAT22C12I. When a high level is sup plied to the $\overline{CS}$ pin, the device goes into the standb mode where the outputs are put into a high impendanc state and the power consumption is drastically reducec With I_{SB} less than 100µA in standby mode, the designe has the flexibility to use this part in battery operate systems.

Read

When the chip is enabled ($\overline{CS}$ = low), the nonvolatil functions are inhibited ($\overline{STORE}$ = high and $\overline{RECALL}$ high). With the Write Enable ($\overline{WE}$) pin held high, the dat in the Static RAM array may be accessed by selecting a address with input pins A_0–A_7. This will occur when th outputs are connected to a bus which is loaded by n more than 100pF and 1 TTL gate. If the loading is greate than this, some additional buffering circuitry is recom mended.

Figure 1. Read Cycle Timing



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Write

With the chip enabled and the nonvolatile functions inhibited, the Write Enable ($\overline{WE}$) pin will select the write mode when driven to a low level. In this mode, the address must be supplied for the byte being written. After the set-up time (t_{AS}), the input data must be supplied to pins I/O_0–I/O_3. When these conditions, including the write pulse width time (t_{WP}) are met, the data will be written to the specified location in the static RAM. A write function may also be initiated from the standby mode by driving $\overline{WE}$ low, inhibiting the nonvolatile functions, supplying valid addresses, and then taking $\overline{CS}$ low and supplying input data.

Figure 2. Write Cycle Timing

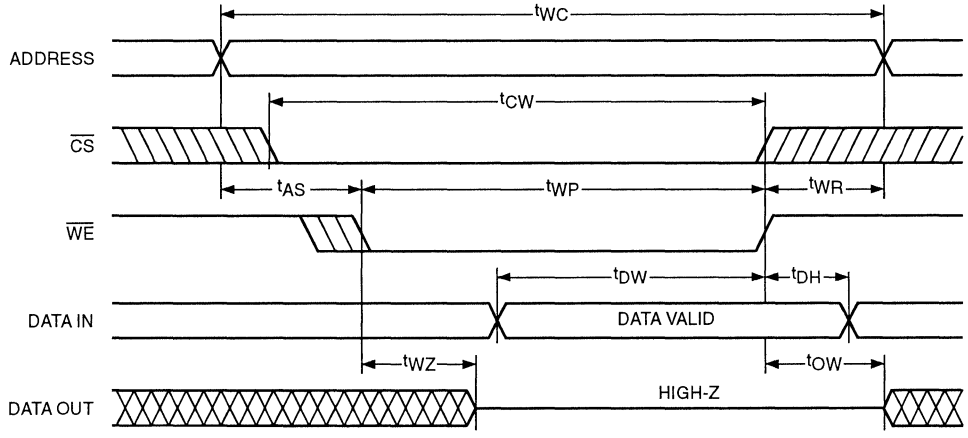

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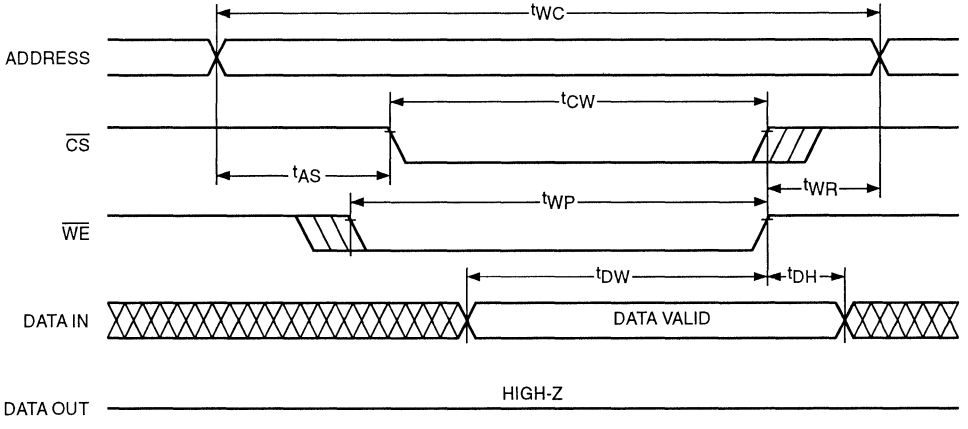
Figure 3. Early Write Cycle Timing



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Recall

At anytime, except during a store operation, taking the $\overline{\text{RECALL}}$ pin low will initiate a recall operation. This is independent of the state of $\overline{\text{CS}}$, $\overline{\text{WE}}$, or A_0–A_7. After the $\overline{\text{RECALL}}$ pin has been held low for the duration of the Recall Pulse Width (t_{RCP}), the recall will continue independent of any other inputs. During the recall, the entire contents of the E²PROM array is transferred to the Static RAM array. The first byte of data may be externally accessed after the recalled data access time from end of recall (t_{ARC}) is met. After this, any other byte may be accessed by using the normal read mode.

If the $\overline{\text{RECALL}}$ pin is held low for the entire Recall Cycle time (t_{RCC}), the contents of the Static RAM may be immediately accessed by using the normal read mode. A recall operation can be performed an unlimited number of times without affecting the integrity of the data.

The outputs I/O_0–I/O_3 will go into the high impedance state as long as the $\overline{\text{RECALL}}$ signal is held low.

Store

At any time, except during a recall operation, taking the $\overline{\text{STORE}}$ pin low will initiate a store operation. This takes place independent of the state of $\overline{\text{CS}}$, $\overline{\text{WE}}$ or A_0–A_7. Th $\overline{\text{STORE}}$ pin must be held low for the duration of the Sto Pulse Width (t_{STP}) to ensure that a store operation initiated. Once initiated, the $\overline{\text{STORE}}$ pin becomes "Don't Care", and the store operation will complete i transfer of the entire contents of the Static RAM arra into the E²PROM array within the Store Cycle tim (t_{STC}). If a store operation is initiated during a write cycl the contents of the addressed Static RAM byte and i corresponding byte in the E²PROM array will be u known.

During the store operation, the outputs are in a hig impedance state. A minimum of 10,000 store operatior can be performed reliably and the data written into th E²PROM array has a minimum data retention time of 1 years.

DATA PROTECTION DURING POWER-UP AND POWER-DOWN

The CAT22C12/CAT22C12I has on-chip circuitry whic will prevent a store operation from occurring when V_C falls below 3.5V typ. This function eliminates the poter tial hazard of spurious signals initiating a store operatio when the system power is below 3.5V typ.

Figure 4. Recall Cycle Timing

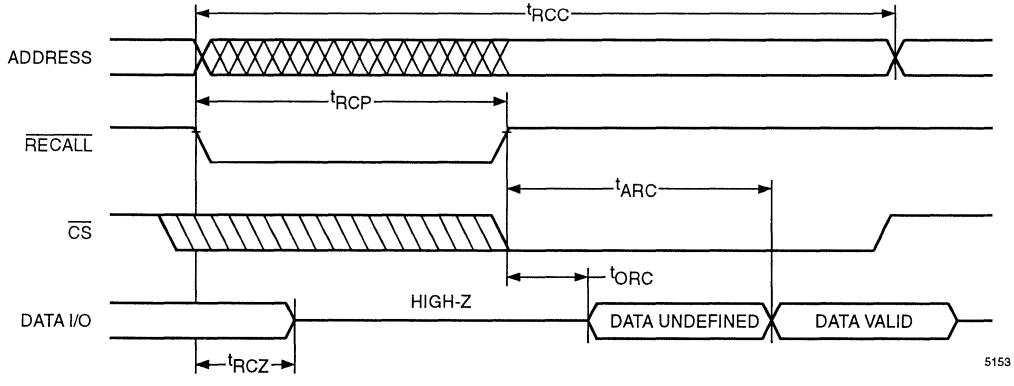

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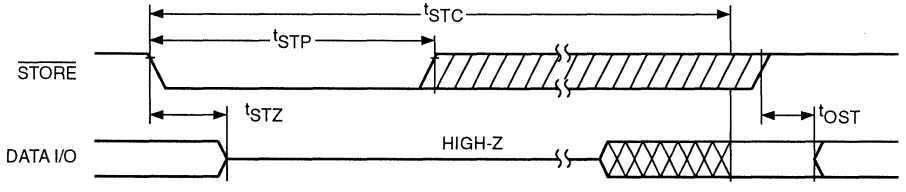
Figure 5. Store Cycle Timing



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CAT24C44/CAT24C44I

256-Bit SERIAL NONVOLATILE CMOS STATIC RAM

FEATURES

- Low Power CMOS Technology
- Single 5V Supply
- Infinite E²PROM to RAM Recall
- CMOS and TTL Compatible I/O
- Low CMOS Power Consumption:
  –Active: 20mA Max.
  –Standby: 30µA Max.
- Power Up/Down Protection
- JEDEC Standard Pinouts:
  –8 pin DIP
  –8 pin SO
- 10,000 Program/Erase Cycles (E²PROM)
- 10 Year Data Retention

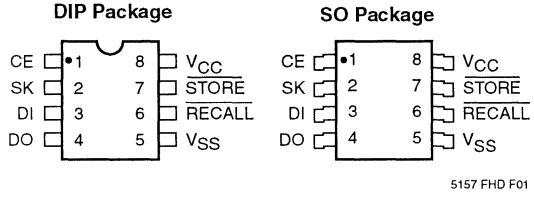
DESCRIPTION

The CAT24C44/CAT24C44I Serial NVRAM is a 256 bit nonvolatile memory organized as 16 words x 16 bits. The high speed static RAM array is bit for bit backed up by a nonvolatile E²PROM array which allows for easy transfer of data from RAM array to E²PROM (STORE) and from E²PROM to RAM (RECALL). STORE operations are completed in 10ms max. and RECALL operations typically within 1.5µs. The CAT24C44/CAT24C44I features unlimited RAM write operations either through external RAM writes or internal recalls from E²PROM.

Internal false store protection circuitry prohibits STORE operations when V_{CC} is less than 3.5V (typical) ensuring E²PROM data integrity.

The CAT24C44/CAT24C44I is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles (E²PROM) and has a data retention of 10 years. The device is available in JEDEC approved 8 pin plastic DIP and SO packages.

PIN CONFIGURATION



PIN FUNCTIONS

Pin Name	Function
SK	Serial Clock
DI	Serial Input
DO	Serial Data Output
CE	Chip Enable
$\overline{\text{RECALL}}$	Recall
$\overline{\text{STORE}}$	Store
V_{CC}	+5V
V_{SS}	Ground

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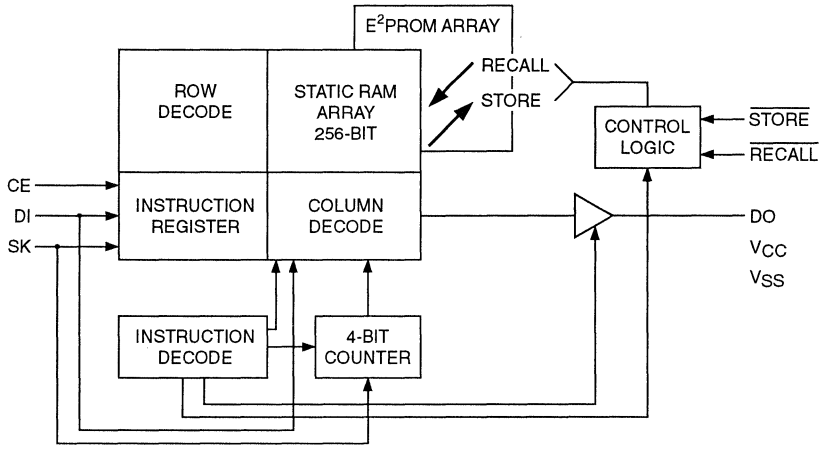
BLOCK DIAGRAM



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MODE SELECTION[1][2]

Mode	$\overline{STORE}$	$\overline{RECALL}$	Software Instruction	Write Enable Latch	Previous Recal Latch
Hardware Recall[3]	1	0	NOP	X	X
Software Recall	1	1	RCL	X	X
Hardware Store[3]	0	1	NOP	SET	TRUE
Software Store	1	1	STO	SET	TRUE

X = Don't Care

POWER-UP TIMING[4]

Symbol	Parameter	Min.	Max.	Units
VCCSR	V_{CC} Slew Rate	.5	.005	V/ms

Note:
(1) The store operation has priority over all the other operations.
(2) The store operation is inhibited when V_{CC} is below ≈ 3.5V.
(3) NOP designates that the device is not currently executing an instruction.
(4) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C
Storage Temperature ..... –65°C to +150°C
Voltage on Any Pin with
Respect to Ground[5] ..... –2.0 to +VCC +2.0V
V_{CC} with Respect to Ground ..... –2.0V to +7.0V
Package Power Dissipation
Capability (Ta = 25°C) 1.0W
Lead Soldering Temperature (10 secs) ..... 300°C
Output Short Circuit Current[6] ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}[4]	Endurance	10,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}[4]	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}[4]	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}[4][7]	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

CAT24C44 T_A = 0°C to +70°C, +5V ±10%, unless otherwise specified.
CAT24C44I T_A = –40°C to +85°C, +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.	Max.		
I_{CCO}	Current Consumption (Operating)			20	mA	Inputs = 5.5V, T_A = 0°C All Outputs Unloaded
I_{SB}	Current Consumption (Standby)			30	µA	Inputs = V_{CC} or V_{SS}
I_{SL}	Sleep Current			30	µA	CE = V_{SS}
I_{LI}	Input Current			2	µA	$0 \le V_{IN} \le 5.5V$
I_{LO}	Output Leakage Current			10	µA	$0 \le V_{OUT} \le 5.5V$
V_{IH}	High Level Input Voltage	2.0		V_{CC}	V	
V_{IL}	Low Level Input Voltage	0.0		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –2mA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 4.2mA
V_{DH}	RAM Data Holding Voltage	1.5		5.5	V	V_{CC}

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Unit	Conditions
$C_{I/O}$[4]	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}[4]	Input Capacitance	6	pF	V_{IN} = 0V

Note:
4) This parameter is tested initially and after a design or process change that affects the parameter.
5) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
6) Output shorted for no more than one second. No more than one output shorted at a time.
7) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

A.C. CHARACTERISTICS

CAT24C44 T_A = 0°C to +70°C, +5V ±10%, unless otherwise specified.
CAT24C44I T_A = –40°C to +85°C, +5V ±10%, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
F_{SK}	SK Frequency	DC	1.0	MHz	
t_{SKH}	SK Positive Pulse Width	400		ns	
t_{SKL}	SK Negative Pulse Width	400		ns	C_L = 100pF + 1TTL gate
t_{DS}	Data Setup Time	400		ns	V_{OH} = 2.2V, V_{OL} = 0.65V
t_{DH}	Data Hold Time	80		ns	V_{IH} = 2.2V, V_{IL} = 0.65V
t_{PD}	SK Data Valid Time		375	ns	Input rise and fall times = 10ns
t_Z	CE Disable Time		1.0	µs	
t_{CES}	CE Enable Setup Time	800		ns	
t_{CEH}	CE Enable Hold Time	400		ns	
t_{CDS}	CE De-Select Time	800		ns	

A.C. CHARACTERISTICS, Store Cycle

CAT24C44 T_A = 0°C to +70°C, +5V ±10%, unless otherwise specified.
CAT24C44I T_A = –40°C to +85°C, +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
t_{ST}	Store Time		10	ms	C_L = 100pF + 1TTL gate
t_{STP}	Store Pulse Width	200		ns	V_{OH} = 2.2V, V_{OL} = 0.65V
t_{STZ}	Store Disable Time		100	ns	V_{IH} = 2.2V, V_{IL} = 0.65V

A.C. CHARACTERISTICS, Recall Cycle

CAT24C44 T_A = 0°C to +70°C, +5V ±10%, unless otherwise specified.
CAT24C44I T_A = –40°C to +85°C, +5V ±10%, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
t_{RCC}	Recall Cycle Time	2500		ns	
t_{RCP}	Recall Pulse Width	500		ns	C_L = 100pF + 1TTL gate
t_{RCZ}	Recall Disable Time		500	ns	V_{OH} = 2.2V, V_{OL} = 0.65V
t_{ORC}	Recall Enable Time	10		ns	V_{IH} = 2.2V, V_{IL} = 0.65V
t_{ARC}	Recall Data Access Time		1500	ns	

INSTRUCTION SET

Instruction	Format			Operation
	Start Bit	Address	OP Code	
WRDS	1	XXXX	0 0 0	Reset Write Enable Latch (Disables, Writes and Stores)
STO	1	XXXX	0 0 1	Store RAM Data in E^2PROM
SLEEP	1	XXXX	0 1 0	Enter SLEEP Mode
WRITE	1	AAAA	0 1 1	Write Data into RAM Address AAAA
WREN	1	XXXX	1 0 0	Set Write Enable Latch (Enables, Writes and Stores)
RCL	1	XXXX	1 0 1	Recall E^2PROM Data into RAM
READ	1	AAAA	1 1 X	Read Data From RAM Address AAAA

X = Don't care
A = Address bit

DEVICE OPERATION

The CAT24C44/CAT24C44I is intended for use with standard microprocessors. The CAT24C44/CAT24C44I is organized as 16 registers by 16 bits. Seven 8 bit instructions control the device's operating modes, the RAM reading and writing, and the E^2PROM storing and recalling. It is also possible to control the E^2PROM store and recall functions in hardware with the $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$ pins. The CAT24C44/CAT24C44I operates on a single 5V supply and will generate, on chip, the high voltage required during a RAM to E^2PROM storing operation.

Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin remains in a high impedance state except when outputting data from the device. The CE (Chip Enable) pin must remain high during the entire data transfer.

The format for all instructions sent to the CAT24C44/CAT24C44I is a logical '1' start bit, 4 address bits (data read or write operations) or 4 "Don't Care" bits (device mode operations), and a 3 bit op code (see Instruction Set). For data write operations, the 8 bit instruction is followed by 16 bits of data. For data read instructions, DO will come out of the high impedance state and enable 16 bits of data to be clocked from the device. The 8th bit of the read instruction is a "Don't Care" bit. This is to eliminate any bus contention that would occur in applications where the DI and DO pins are tied together to from a common DI/DO line. A word of caution whil clocking data to and from the device: If the CE pin prematurely deselected while shifting in an instructio that instruction will not be executed, and the shift regist internal to the CAT24C44/CAT24C44I will be cleared. there are more than or less than 16 clocks during memory data transfer, an improper data transfer w result. The SK clock is completely static allowing th user to stop the clock and restart it to resume shifting data.

Read

Upon receiving a start bit, 4 address bits, and the 3 b read command (clocked into the DI pin), the DO pin the CAT24C44/CAT24C44I will come out of the hig impedance state and the 16 bits of data, located at th address specified in the instructions, will be clocked ou of the device. When clocking data from the device, th first bit clocked out (DO) is timed from the falling edge the 8th clock, all succeeding bits (D1–D15) are time from the rising edge of the clock (Figure 1).

Write

After receiving a start bit, 4 address bits, and the 3 b WRITE command, the 16 bit word is clocked into th device for storage into the RAM memory location spec fied. The CE pin must remain high during the entire writ operation.

Figure 1. RAM Read Cycle Timing

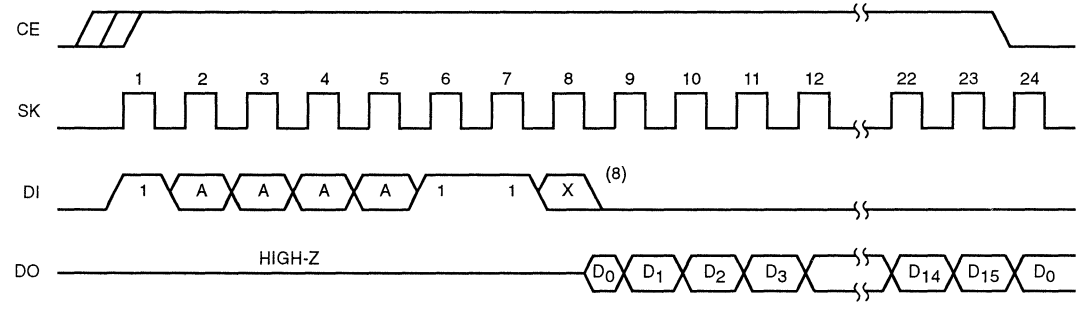

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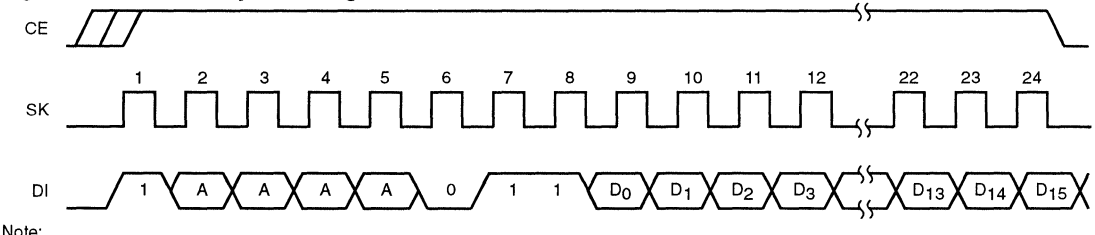
Figure 2. RAM Write Cycle Timing



Note:
(8) Bit 8 of READ instruction is "Don't Care".

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WREN/WRDS

The CAT24C44/CAT24C44I powers up in the program disable state (the "write enable latch" is reset). Any programming after power-up or after a WRDS (RAM write/E²PROM store disable) instruction must first be preceded by the WREN (RAM write/E²PROM store enable) instruction. Once writing/storing is enabled, it will remain enabled until power to the device is removed, the WRDS instruction is sent, or an E²PROM store has been executed (STO/STORE). The WRDS (write/store disable) can be used to disable all CAT24C44/CAT24C44I programming functions, and will prevent any accidental writing to the RAM, or storing to the E²PROM. Data can be read normally from the CAT24C44/CAT24C44I regardless of the "write enable latch" status.

Sleep

The sleep mode places the CAT24C44/CAT24C44I into a lower quiescent power mode. Internal RAM power is turned off, and any data that is written into the RAM area is lost. However, data from the last RAM to E²PROM store operation is retained in the E²PROM memory. The CAT24C44/CAT24C44I will exit the sleep mode, and restore the RAM memory area by issuing either a hardware or software recall command.

Figure 3. Read Cycle Timing

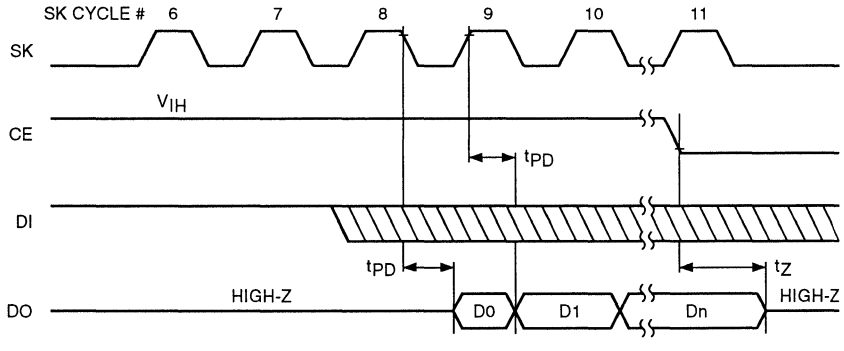

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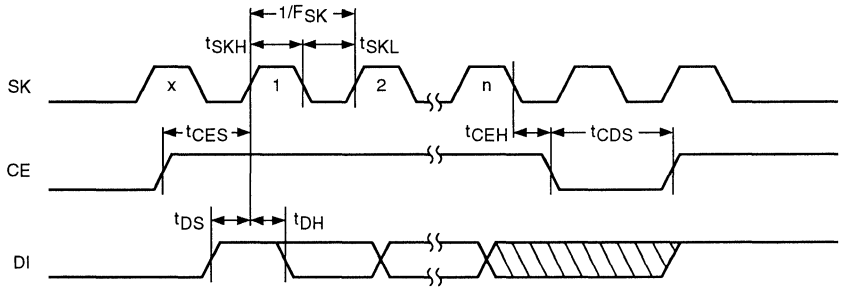
Figure 4. Write Cycle Timing



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RCL/$\overline{\text{RECALL}}$

Data is transferred from the E^2PROM data memory to RAM by either sending the RCL instruction or by pulling the $\overline{\text{RECALL}}$ input pin low. A recall operation must be performed before the E^2PROM store, or RAM write operations can be executed. Either a hardware or software recall operation will set the "previous recall" latch internal to the CAT24C44/CAT24C44I.

STO/$\overline{\text{STORE}}$

Data in the RAM memory area is stored in the E^2PROM memory either by sending the STO instruction or by pulling the $\overline{\text{STORE}}$ input pin low. As security against any inadvertent store operations, the following conditions must each be met before data can be transferred into nonvolatile storage:

- The "previous recall" latch must be set (either a software or hardware recall operation).
- The "write enable" latch must be set (WREN instruction issued).
- STO instruction issued or $\overline{\text{STORE}}$ input low.

During the store operation, all other CAT24C44 CAT24C44I functions are inhibited. Upon completion the store operation, the "write enable" latch is reset. The device also provides false store protection whenever V_{CC} falls below a 3.5V level. If V_{CC} falls below this level the store operation is disabled and the "write enable" latch is reset.

Figure 5. Recall Cycle Timing

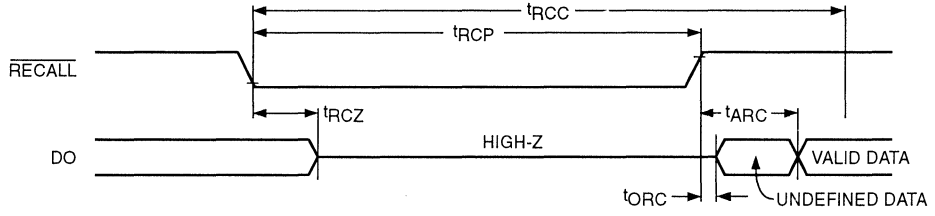

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Figure 6. Hardware Store Cycle Timing

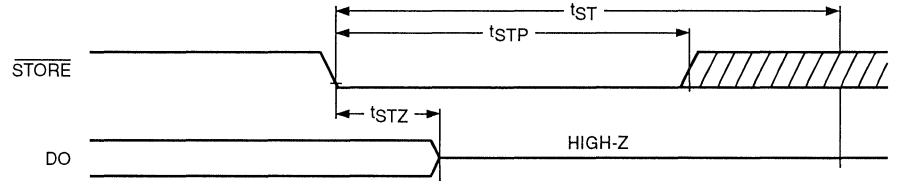

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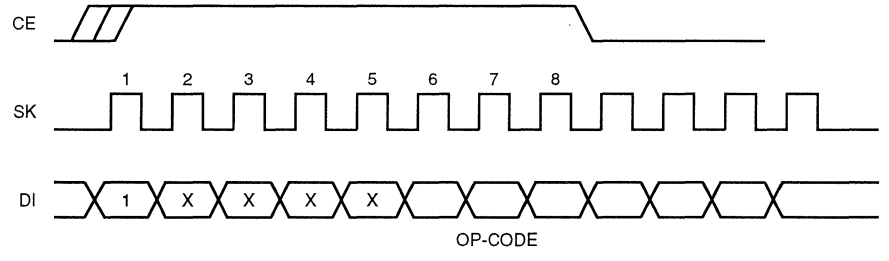
Figure 7. Non-Data Operations



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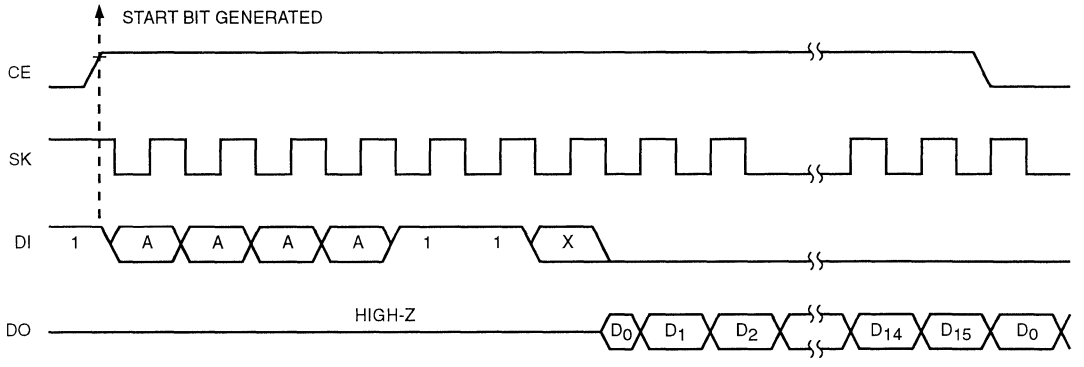
Start Bit Timing

The CAT24C44/CAT24C44I features an alternate start bit timing where the device will accept a start bit that is generated when both SK and DI are high with respect to a low to high transition of CE (see Figure 8). Once this start bit is generated all subsequent data is clocked into the device on the positive clock edge of SK.

Figure 8. Alternate Start Bit Timing Example: Read Instruction



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CATALYST SEMICONDUCTOR

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2-Wire Bus Serial E^2PROMs 2

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CAT104/105

2 Bit, 25MHz D/A Converter

EATURES

- 40 ns maximum settling time (1/2 LSB)
- 25 MHz update rate
- 1/2 LSB Integral Non-Linearity
- 1/2 LSB Differential Non-Linearity
- 25 ppm/°C internal voltage reference
- Low Power BiCMOS construction
- Single Supply operation (+5 V)

PPLICATIONS

- Arbitrary Waveform Generators
- Direct Digital Synthesis (DDS)
- High Resolution A/D Converters
- Automatic Test Equipment
- High Definition Video

ESCRIPTION

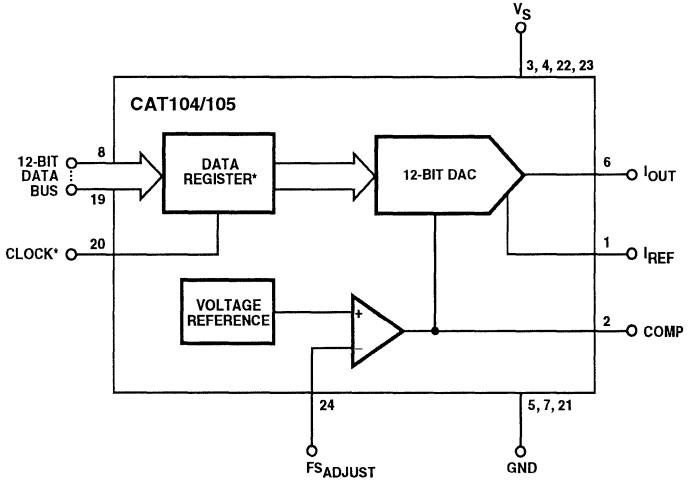
The CAT104 and CAT105 are monolithic 12 bit current utput D/A converters designed for precision high speed data conversion applications. Powered from a single +5 Volt supply the CAT104 and CAT105 will source 40 mA of current into a 25 Ohm load at clock speeds of 25 MHz while maintaining 1/2 LSB accuracy. Settling time is 40 ns to .012% of Full Scale.

Fabricated in a 2.0 micron BiCMOS process, the CAT104 and CAT105 incorporate on-chip EEPROM driven trim circuitry for factory correction of all silicon and package induced errors. Gain error is adjusted to below <0.2 % and linearity to .012 %. Monotocity is guaranteed over the full operating temperature range. The CAT104 and CAT105 include an on-chip voltage reference which is EEPROM trimmed to achieve a typical drift with temperature of 25 ppm/°C.

Data interface is via a 12 bit parallel bus and directly accesses the D/A in the CAT104, while the CAT105 provides a clocked data input register.

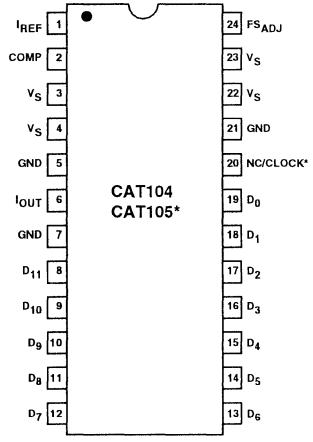
The CAT104 and CAT105 are pin compatible with Brooktree's Bt 104 & Bt 105 while offering improved performance. Both are specified for operation over the 0°C to +70°C Commercial temperature range and are packaged in Ceramic DIPs.

UNCTIONAL DIAGRAM



*CAT105 ONLY

PIN CONFIGURATION



TD 5168

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V_S to GND ..... –0.5V to +7V

Inputs
- D_0-D_{11} to GND ..... –0.5V to V_S +0.5V
- FS_{ADJUST} to GND ..... –0.5V to V_S +0.5V
- COMP to GND ..... –0.5V to V_S +0.5V
- CLOCK to GND ..... –0.5V to V_S +0.5V
- I_{REF} ..... ±10 mA

Outputs
- Analog Output Current (I_{OUT}) ..... 50 mA
- Analog Output Voltage (I_{OUT}) ..... V_S^- 7V to V_S^+ 0.5V
- Analog Output Short Circuit Duration ..... Infinite

Operating Ambient Temperature
- Commercial ('C' suffix) ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Lead Soldering (10 sec max) ..... +300°C

ORDERING INFORMATION

Device	Package	Temp	INL
CAT104AC	24 pin Ceramic DIP	C	1/2 LSB
CAT105AC	24 pin Ceramic DIP	C	1/2 LSB
CAT104BC	24 pin Ceramic DIP	C	1 LSB
CAT105BC	24 pin Ceramic DIP	C	1 LSB
CAT104BCI	24 pin Ceramic DIP	I	1 LSB
CAT105BCI	24 pin Ceramic DIP	I	1 LSB

Temperature: C = 0°C to +70°C
I = -40°C to +85°C

Stresses above those listed under Absolute Maximum Ratings ma cause permanent damage to the device. Absolute Maximum Rating are limited values applied individually while other parameters ar within specified operating conditions, and functional operation at an of these conditions if NOT implied. Device performance and reliabilit may be impaired by exposure to absolute rating conditions for extende periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Method
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(2)	Latch-Up	100		mA	JEDEC Standard 17

NOTES: 1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_S + 1V.

DC ELECTRICAL CHARACTERISTICS: V_S = +5V ±0.25V; T_A = Specified Operating Range; I_{OUT} (FS) = 40mA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Resolution			12	—	—	Bits
Accuracy						
INL	Integral Linearity Error	CAT104A/105A	—	—	±1/2	LSB
		CAT104B/105B	—	—	±1	LSB
DNL	Differential Linearity Error		—	—	±1/2	LSB
	Zero Offset Error		—	—	1.0	µA
	Gain Error	Internal Reference	—	±0.15	±0.3	%FS
		External Reference	—	—	±1.0	%FS
	Monotocity		Guaranteed			
Coding						
	I_{OUT}	D_0-D_{11} = 0	0	—	—	
	I_{OUT}	D_0-D_{11} = 1	—	—	Full Scale	
Data Inputs						
V_{IH}	High Level Input Voltage		2	—	—	V
V_{IL}	Low Level Input Voltage		—	—	0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4V	—	—	1.0	µA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V	—	—	–1.0	µA
Analog Output						
I_{OUT}	Output Current		10	—	40	mA
V_{OUT}	Output Compliance		–1.0	—	+1.0	V
R_{OUT}	Output Impedance		—	1	—	MΩ
Reference						
$I_{REF\ (Pin\ 1)}$	Operating Voltage Range		–0.3	0.68	1.0	V
V_{REF}	Internal Reference Voltage		0.67	0.68	0.69	V
TC_{VREF}	Temperature Coefficient		—	±25	—	ppm/°C

C **ELECTRICAL CHARACTERISTICS** (Cont.): V_S = +5V ±0.25V; T_A = Spec. Operating Range; I_{OUT} (FS) = 40mA

ymbol	Parameter	Conditions	Min	Typ	Max	Units
wer Supply						
$'_S$	Supply Voltage Range		4.5	5	6	V
S	Supply Current	25 MHz, I_{OUT} = 40 mA	—	60	75	mA
'SRR	Power Supply Rejection Ratio	COMP = 0.01 µF, f = 1 kHz	—	0.02	0.5	%/%ΔV_S

C **ELECTRICAL CHARACTERISTICS:** V_S = 5V ±0.25V; R_L = 25Ω; I_{OUT} (FS) = 40 mA.
Logic inputs: 0V-3V; t_r and t_f< 3 ns. T_A = Spec. Operating Range

ymbol	Parameter	Conditions	Min	Typ	Max	Units
ata Inputs						
MAX	Register Clock Rate		—	—	25	MHz
CC	Clock Cycle Time		40	—	—	ns
PWH	Clock Pulse Width High Time		10	—	—	ns
PWL	Clock Pulse Width Low Time		10	—	—	ns
DS	Data Setup Time		10	—	—	ns
DH	Data Hold Time		2	—	—	ns
	Pipeline Delay	CAT105 Only	1	1	1	Clock
nalog Output						
OD	Output Delay		—	25	—	ns
R	Output Rise Time		—	8	—	ns
F	Output Fall Time		—	8	—	ns
OS[1]	Output Settling Time	To 0.012% of FS	—	30	40	ns
		To 0.025% of FS	—	20	40	ns
		To 0.10% of FS	—	15	—	ns
	Clock and Data Feedthrough[1]		—	- 40	—	dB
	Glitch Impulse[1]		—	100	—	pV-sec
	Differential Gain Error		—	1.5	—	%FS
	Differential Phase Error		—	1.5	—	Degrees
in Capacitance						
C_{IN}	Input Capacitance, D_0-D_{11}, CLK	V_{IN} = 2.4V, f = 1 MHz	—	10	—	pF
C_{OUT}	Output Capacitance, Pin 6	I_{OUT} = 0 mA, f= 1 MHz	—	25	—	pF

OTES: 1. Clock and Data feedthrough is function of the magnitude of overshoot and undershoot on the digital inputs. While testing, the digital inputs have a 1k ohm resistor connected to the regular PCB ground plane and are driven by 74 HC logic. Clock and data feedthrough are excluded from the settling time, where as they are included in glitch impulse. (Test bandwidth = 50 MHz.)

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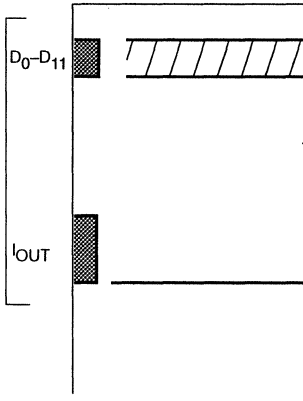
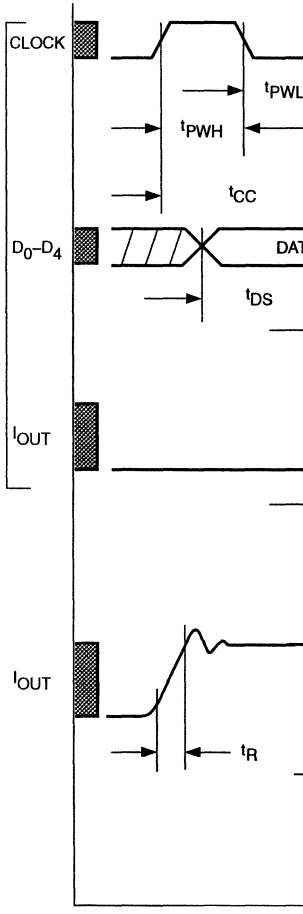
AC TIMING DIAGRAM

CAT104



PARAMETER NAME	MEASURED FROM	MEASURED TO	MIN MAX
t_{OD}	FROM:	Data Valid	Max
	TO:	50% of FS output	
t_{OS}	FROM:	50% of FS output	Max
	TO:	Output within allowed error band (1/2 LSB or 1 LSB)	

CAT105



PARAMETER NAME	MEASURED FROM	MEASURED TO	MIN MAX
t_{PWL}	FROM:	50% point of falling edge	Min
	TO:	50% point of rising edge	
t_{PWH}	FROM:	50% point of rising edge	Min
	TO:	50% point of falling edge	
t_{CC}	FROM:	50% point of rising edge	Min
	TO:	50% point of next rising edge	
t_{DS}	FROM:	Data valid	Min
	TO:	50% point of clock's next rising edge	
t_{DH}	FROM:	End of t_{DS} period	Min
	TO:	data invalid	
t_{OD}	FROM:	50% point of clock's rising edge	Max
	TO:	50% of FS output	
t_{OS}	FROM:	50% of FS output	Max
	TO:	Output within allowed error band (1/2 LSB or 1 LSB)	
t_R	FROM:	10% point of FS output	Max
	TO:	90% point of FS output	
t_F	FROM:	90% point of FS output	Max
	TO:	10% point of FS output	

NS

n No.	Name	Function
	I_{REF}	Reference Current Output. The DAC's full scale output current is set by I_{REF}, which is normaly connected to FS_{ADJUST} and a resistor, R_{SET}. The full scale output current is then determined by the value of R_{SET}.
	COMP	Compensation pin. This pin must be connected to the V_S pin through a ceramic capacitor. This capacitor provides power supply noise rejection and reduces the random noise of the internal bandgap reference. The capacitor can be between 0.01 µF and 0.1 µF, with 0.01µF being the recommended value. When an external reference voltage is used COMP is used in conjunction with FS_{ADJUST} to set I_{REF}.
4, 22, 23	V_S	The positive supply voltage, nominally +5V.
7,21	GND	Ground return for all signals (digital and analog) and V_S.
	I_{OUT}	Analog Current Output. This high impedance current source is capable of sourcing up to 40 mA of current.
9	D_0-D_{11}	TTL compatible Data Inputs. Pin D_0 is the least significant data bit. For CAT105, the inputs are latched on the rising edge of clock. All unused inputs must be tied to V_S or GND.
	Clock or N/C	Clock Input for CAT105. The rising edge of Clock latches the D_0-D_{11} inputs. Ideally, this pin should be driven by a dedicated TTL/CMOS buffer. This pin is not used on CAT104 and may be left floating without affecting performance.
	FS_{ADJUST}	Full Scale Adjust Control. When the internal reference voltage is used, the full scale output current is controlled by the resistor R_{SET}, connected between this input pin and GND. When an external voltage reference is used, FS_{ADJUST} is tied to V_S.

ERMS AND DEFINITIONS

ifferential Non-Linearity (DNL): The maximum deviaon from an ideal LSB step, between any two adjacent output vels. A DNL error more negative than -1LSB implies nononotonic output performance.

ıll Scale Output Current: The output current at I_{out} sulting from all 1's at the data inputs.

ain Error: The variation in the slope (gain) of the transfer nction of a converter with respect to an established ideal ınsfer function. This error is expressed in % of FS (Full Scale) LSB, when all bits are on, and may be eliminated by justing the reference current applied to the device.

litch Impulse Area: The analog output transient occurring tween two adjacent codes as a result of unequal turn-on and rn-off times for the internal current sources. Glitch impulse calculated as the area of the largest excursion, about the final lue, and is specified as the net area of the glitch in nV-sec or A-sec.

ıtegral Non-Linearity (INL): The maximum deviation beveen the actual output level and a best straight line fit. This cludes gain and offset errors.

Least-Significant Bit (LSB): The ideal output increment between two adjacent codes. Also, the data bit with the smallest effect on the output level.

Monotonicity: Implies that for an increase in digital code value that the output will either increase or remain unchanged. In mathematical terms the output is a single valued function of the input code, and the derivative of the output transfer function must not change signs.

Most-Significant Bit (MSB):The data bit with the largest effect on the output level. The MSB, for a linear DAC output, ideally equals the combined output weight of all other data bits, plus 1 LSB.

Offset Error: The deviation of the analog output from the ideal (0V or 0mA) when the inputs are set to all 0s is called unipolar offset error.

Output Compliance Range: The output voltage range over which a stated linearity specification is maintained. Integral linearity errors tend to be exaggerated with increasing output voltage levels.

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CURRENT vs VOLTAGE OUTPUT

The CAT104/105 has been carefully designed to work equally well in both current and voltage output applications, a claim not all DACs can make. When using other DACs, designers may be forced to use additional circuitry or be obliged to accept reduced performance when voltage output is required.

High speed DACs give their best performance in current output mode. This is because in current output operation the DAC's output is tied to a summing junction, such as the negative input of an op amp, and feedback around the op amp holds the junction voltage constant (usually 0 volts). Since no voltage change occurs at the DAC's output the DAC is uneffected by load resistance, R_L , or any other impedances internal or external to the DAC.

When generating a voltage output, however, R_L can have a significant effect on the DAC's performance. The problem is caused by the DAC's own output impedance. As shown in Fig1 a DAC's output can be modeled as a current source in parallel with an internal resistance. When an external load is connected to I_{OUT}, it is in parallel with the internal resistance and the actual load seen by the DAC is the combination of their values. In developing an output voltage, I_{OUT} is split between internal and external loads, producing an apparent error in V_{OUT}. The degree of error is determined by the ratio of R_L to the internal shunt resistance. For ideal current sources the shunt resistance is infinite, but in typical high speed DACs it ranges from 200 to 20,000 Ω. This will produce a significant loading effect, even with the 50 Ω or 25 Ω loads commonly used in high speed systems.

To combat this problem, Catalyst has taken special care to create a true current source output structure for the CAT104/105. The CAT104/105's 1 MΩ output impedance frees designers from concerns about voltage induced errors and voltage outputs can be had with no penalty in performance.

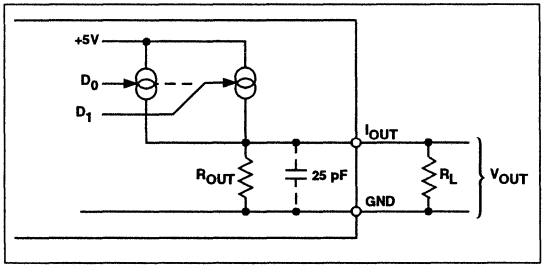

Figure 1. DAC Output Equivalent Circuit

OUTPUT VOLTAGE COMPLIANCE

The maximum voltage that may be realized at the DAC's output, while maintaining rated accuracy and performance, is 1.0 volts. Care should be taken when selecting R_L and I_{OUT} that the resulting Full Scale voltage does not exceed this value. Also, when operating into a summing junction (current mode), be sure the DC voltage of the summing node is below 1.0 volts.

BUFFERED VOLTAGE OUTPUTS

For applications requiring output voltages greater than 1 volts a buffering amplifier will be required. Figure 2 illustrat a typical buffered output application.

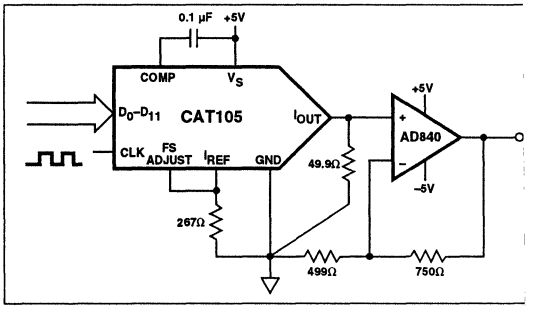

Figure 2. Buffer Voltage Output 0 to +2.5V

FULL SCALE ADJUST

The CAT104/105's output can be adjusted for any desired lev between 0 - 1.0V or 0 - 40 mA via the FS_{ADJUST} pin. Referri to Figure 3, I_{REF}, which sets the DAC's Full Scale output curren is controlled by op amp A1. The control loop is configured so th A1 will maintain a constant 0.68 volts at the FS_{ADJUST} pin. I_{REF} has a maximum compliance voltage of 1.0 volts, it is best use R_{TRIM} as a variable resistor in series with R_{SET} and tie FS_{ADJUS} directly to I_{REF}. This avoids the possibility of the voltage acro the combination of R_{TRIM} and R_{SET} exceeding I_{REF}'s complian range.

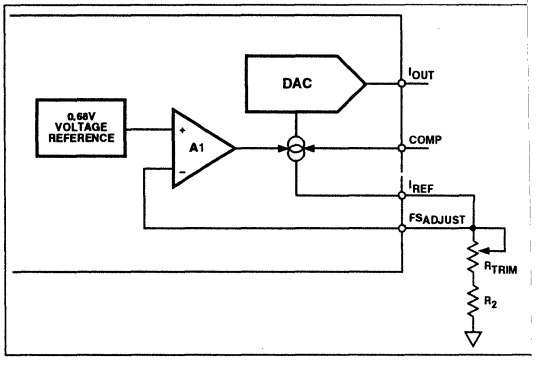

Figure 3. FS_{ADJUST} Equivalent Circuit

;ING THE INTERNAL VOLTAGE REFERENCE

)recision voltage reference is provided by the CAT104/105 allow for easy adjustment and control of I_{REF}, which sets the AC full scale output current, I_{OUT}. The relationship be-een I_{OUT} and I_{REF} is:

$$I_{OUT} = 7.892 * I_{REF}$$

:ET is then calculated from the equation:

$$R_{SET} = \frac{7.892 * V_{REF}}{I_{OUT}}$$

here $V_{REF} = 0.68$ V.

The internal reference is factory trimmed to compensate for variations in the transfer ratio of I_{REF} to I_{OUT}, making the full scale output voltage accurate to within 0.3% for the transfer function:

$$V_{OUT} = 5.367 * \frac{R_L}{R_{SET}}$$

Full scale output voltage variation from device to device will be ±0.3% when there is perfect tracking between the load and reference current resistors. For optimum performance, R_{SET} and R_L should be a trimmed resistor network with ratio tracking better than ±0.1% and temperature coefficient tracking better than 5 ppm/°C.

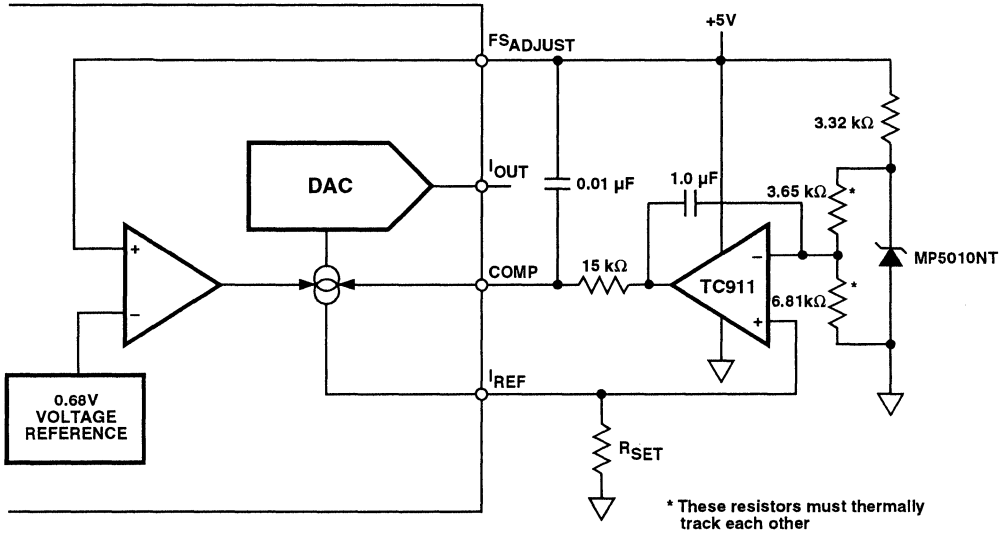

Figure 4a. External Voltage Reference, Single Supply

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USING AN EXTERNAL VOLTAGE REFERENCE

The precision voltage reference contained in the CAT104 and CAT105 is factory trimmed by EEPROM circuitry to guarantee a maximum temperature drift of 10 ppm/ °C. For most applications this is more than adequate, however, there may arise occasions when system requirements dictate that an external reference be used. In such cases the on-chip reference can be disabled and control of I_{REF} can be taken off chip.

When using an external reference, the control amplifier's offset and offset drift can not be ignored. The D/A's output stability is dependent upon not only the reference but the control circuitry around it. For this reason it is recommended that the control amplifier be of the ultra low offset variety, typically < 25μV with a drift of less than 0.1 μV/°C.

Figure 4a shows an example of the CAT104/105 being used with an external reference in a single supply application. In this circuit, a low drift 1.2 V bandgap reference has been chosen and its voltage divided to 0.8 V by a pair of resistors. This is done to insure that I_{REF} does not exceed its voltage compliance range. The op amp, a low drift chopper stabilized type, replaces the internal control amplifier, which has been deactivated by tying FS_{ADJUST} to the positive supply rail. Control of I_{REF} is effected through the COMP pin which adds an inversion to the control loop (I_{REF} current increases as V_{COMP} -> 0 V).

A simpler circuit can be used to incorporate an external volta reference if a negative supply voltage is available, as shown Figure 4b. Here, a precision - 10V reference and R_{SET} co bine with the CAT104/105's internal reference and amplifi to set and control I_{REF}. V_{REF} becomes the sum of the intern and external references, and R_{SET} is calculated from t equation

$$R_{SET} = 7.892 * \frac{V_{REF} + 0.68}{I_{OUT}}$$

Since V_{REF} is now the sum of the two references, a large valu voltage is chosen for the external reference so that its chara teristics will be dominant. Any noise or drift exhibited by t internal reference is now reduced in its effect by the ratio of t two reference voltages.

The internal reference is not precisely 0.68 V, as stated in t equation above, because it is factory adjusted to compensate f variations in the current transfer ratio of I_{OUT} to I_{REF}. T compensate for this, the external voltage reference can b offest by a corresponding amount using the Fine Adjustme feature. For references without this adjustment feature, R_{SE} can be trimmed instead.

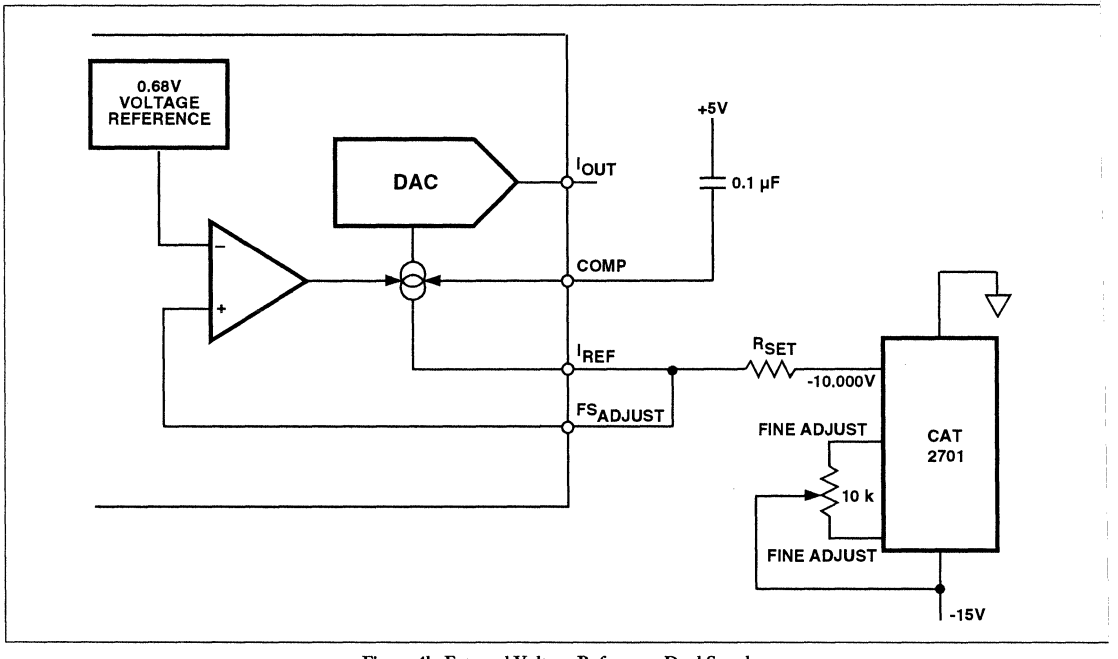
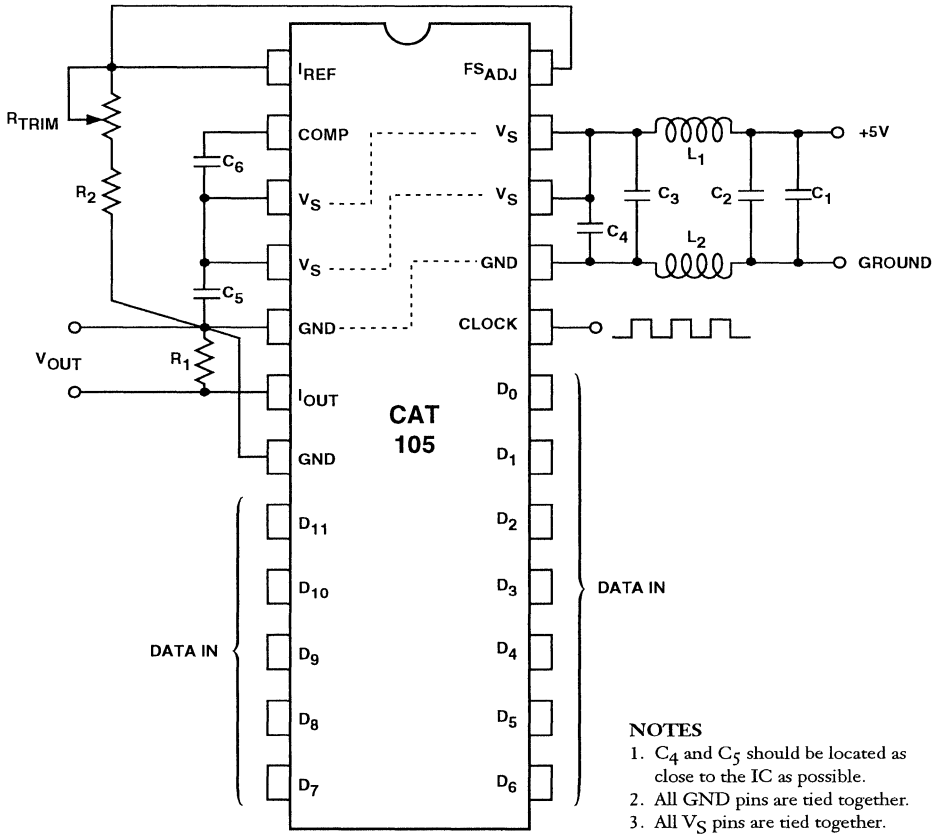


Figure 4b. External Voltage Reference, Dual Supply

UPPLY DECOUPLING

is essential to decouple the power and ground supply lines om the system's main power bus. This prevents glitches and ›ise spikes generated elsewhere in the system from getting ıto the DAC and showing up on its output.

Decoupling is best achieved through a filter network placed in series with the DAC's power supply lines. The filter is comprised of two inductors, one in each supply line, combined with several bypass capacitors. An example of this is shown in Figure 5.



NOTES
1. C_4 and C_5 should be located as close to the IC as possible.
2. All GND pins are tied together.
3. All V_S pins are tied together.

COMPONENT	DESCRIPTION	SUPPLIER	PART NUMBER
C_6	0.1 µF Ceramic Capacitor	Erie	RPE112Z5U104M50V
C_2	0.01 µF Ceramic Capacitor	Erie	RPE110Z5U103M50V
C_4, C_5	0.01 µF Ceramic Chip Capacitor	Johanson Dielectrics	X7R500S41W103KP
C_1, C_3	22 µF Tantalum Capacitor	Mallory	CSR13G226KM
R_1	24.9Ω 1% Metal Film Resistor	Dale	CMF-55C
L_1, L_2	Ferrite Bead	Fair-Rite	2743001111
R_2	121Ω 1% Metal Film Resistor	Dale	CMF-55C
R_{TRIM}	50Ω Cermet Trim Pot	Bourns	3386W

Figure 5. Typical Application: Unbuffered Voltage Output, 0 - 1V

SUPPLY CURRENT

The maximum supply current drawn by the CAT104/105 can be calculated from the equation:

I_S = Full Scale Output Current (in mA) +
1.2mA per MHz of operating speed.

P.C. BOARD LAYOUT

Combining high speed with high precision presents a formidable challenge to system designers. Proper RF techniques must be used in board design, device selection, supply bypassing, grounding and measurement if optimum performance is to be realized.

BYPASS CAPACITORS

The most important external components associated with any high-speed design are the power supply bypass capacitors. Selection and placement of these capacitors is critical, and to a large extent, dependent upon the specifics of the system's configuration. The key consideration in selection of bypass capacitors is minimization of series resistance and inductance. Many capacitors will begin to look inductive at 20 MHz and above. Ceramic and metal film capacitors generally feature lower series inductance than the tantalum or electrolytic types.

Bypass capacitors should be installed on the printed circuit board as close to the IC as is physically possible, and with the shortest possible leads in order to minimize series lead inductance. Chip capacitors are optimal in this respect and thus highly recommended.

CRITICAL CONNECTIONS

In using the CAT104/105 it is of the utmost importance to b
sure *all* V_S and GND pins are connected to to their respectiv
supplies. Failure to do so will result in improper DAC opera
tion, and may result in damage to the IC.

HIGH-SPEED INTERCONNECT

It is essential that care be taken in the signal and power groun
circuits to avoid inducing extraneous voltage drops in the signa
ground paths. All connections should be short and direct an
as physically close to the package as possible. Any conductio
path shared by external components should be minimized
When runs exceed an inch or so in length, some type termina
tion resistor may be required. This is true of both the analo
and digital sections. For digital signals the termination resisto
will be dependent upon the logic family used.

Ground planes should be connected at or near the DAC. Car
should be taken to insure that the ground plane is uninterrupte
over crucial signal paths. On the digital side, this includes th
DAC output signal as well as the supply feeders. The use o
wide runs or planes in the routing of power lines is alsc
recommended. This serves the dual function of providing a lov
series impedance power supply to the part as well as providin
some "free" capacitive decoupling to the appropriate grounc
plane.

For maximum AC performance, the DAC should be mountec
directly to the circuit board; sockets should not be used as the
increase lead inductance and capacitance. Any additional leac
inductance or capacitance at the supply pins can seriously
undermine dynamic performance. Even Teflon or "pin" sock-
ets can create unwanted results, so soldering directly to the
circuit board is highly recommended.

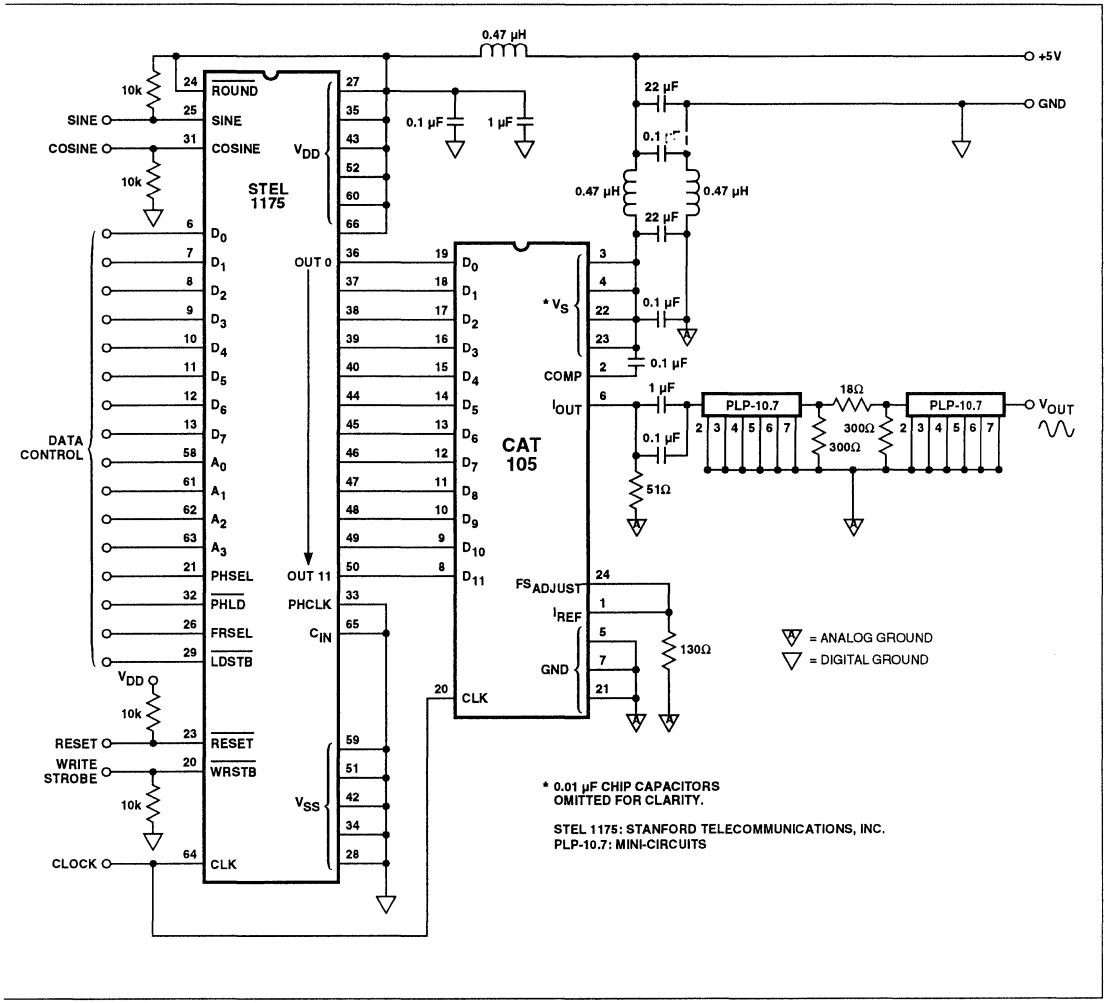


Figure 6. Direct Digital Synthesis (DDS) Using the CAT105

CAT504

Quad DACpot

FEATURES

- Output settings retained without power
- Output range includes both supply rails
- 4 independently addressable outputs
- 1 LSB Accuracy
- Serial uP interface
- Single supply operation: 3 - 5 Volts
- Setting read-back without effecting outputs

APPLICATIONS

- Automated product calibration.
- Remote control adjustment of equipment
- Offset, gain and zero adjustments in Self-Calibrating and Adaptive Control systems.
- Tamper-proof calibrations.

DESCRIPTION

The CAT504 is a quad 8 Bit Memory DAC designed as an electronic replacement for mechanical potentiometers and trim pots. Intended for final calibration of products such as recorders, fax machines and cellular telephones on automated high volume production lines, it is also well suited for systems capable of self calibration, and applications where equipment which is either difficult to access or in a hazardous environment, requires periodic adjustment.

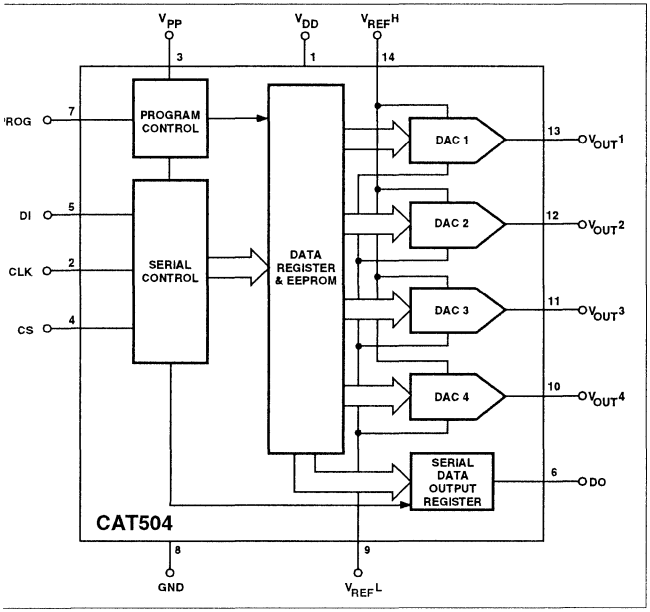
The 4 independently programmable DAC's have an output range which includes both supply rails. Output settings, stored in non-volatile EEPROM memory, are not lost when the device is powered down and are automatically reinstated when power is returned. Each output can be dithered to test new output values without effecting the stored settings and stored settings can be read back without disturbing the DAC's output.

Control of the CAT504 is accomplished with a simple 3 wire serial interface. A Chip Select pin allows several CAT504s to share a common serial interface and communication back to the host controller is via a single serial data line thanks to the CAT504's Tri-Stated Data Output pin.

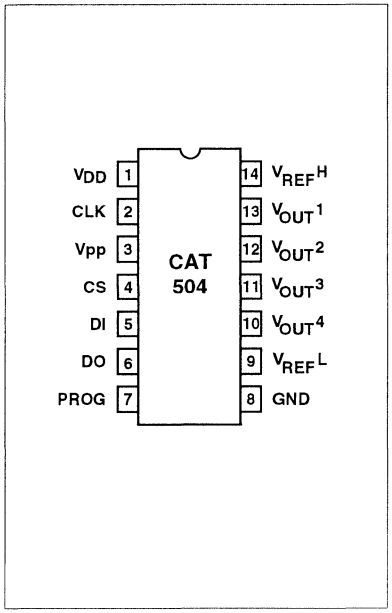
The CAT504 operates from a single 3 - 5 volt power supply drawing just a few milliwatts of power. When storing data in EEPROM memory an additional 20 volt low current supply is required.

The CAT504 is available in the 0 to 70° C Commercial and -40° C to +85° C Industrial operating temperature ranges and offered in both plastic DIP and Surface mount packages.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



TD 5169

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V_{DD} to GND ..... –0.5V to +7V
- V_{PP} to GND ..... –0.5V to +22V

Inputs
- CLK to GND ..... –0.5V to V_{DD} +0.5V
- CS to GND ..... –0.5V to V_{DD} +0.5V
- DI to GND ..... –0.5V to V_{DD} +0.5V
- PROG to GND ..... –0.5V to V_{DD} +0.5V
- $V_{REF}H$ to GND ..... –0.5V to V_{DD} +0.5V
- $V_{REF}L$ to GND ..... –0.5V to V_{DD} +0.5V

Outputs
- D_0 to GND ..... –0.5V to V_{DD} +0.5V
- V_{OUT} 1– 4 to GND ..... –0.5V to V_{DD} +0.5V

Operating Ambient Temperature
- Commercial ('C' suffix) ..... 0°C to +70°C
- Industrial ('I' suffix) ..... – 40°C to +85°C

Junction Temperature ..... +150°C

Storage Temperature ..... –65°C to +150°C

Lead Soldering (10 sec max) ..... +300°C

ORDERING INFORMATION

Device	Package	Temp	INL
CAT504P	14 pin Plastic DIP	C	1 LSB
CAT504PI	14 pin Plastic DIP	I	1 LSB
CAT504J	14 pin SOIC	C	1 LSB
CAT504JI	14 pin SOIC	I	1 LSB

Temperature: C = 0°C to +70°C
I = – 40°C to +85°C

Stresses above those listed under Absolute Maximum Ratings m cause permanent damage to the device. Absolute Maximum Ratin are limited values applied individually while other parameters a within specified operating conditions, and functional operation at a of these conditions is NOT implied. Device performance and reliabil may be impaired by exposure to absolute rating conditions for extend periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Method
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(2)	Latch-Up	100		mA	JEDEC Standard 17

NOTES: 1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{DD} + 1V.

DC ELECTRICAL CHARACTERISTICS:

V_{DD} = +3V to +5V ±10%, $V_{REF}H = V_{DD}$, T_A = 25°C, $V_{REF}L$ = 0V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Resolution		8	—	—	Bits
Accuracy						
INL	Integral Linearity Error	I_{LOAD} = 250 nA, T_R = C	—	—	±1	LSB
		T_R = I	—	—	±1	LSB
		I_{LOAD} = 1 µA, T_R = C	—	—	±2	LSB
		T_R = I	—	—	±2	LSB
DNL	Differential Linearity Error	I_{LOAD} = 250 nA, T_R = C	—	—	±0.5	LSB
		T_R = I	—	—	±0.5	LSB
		I_{LOAD} = 1 µA, T_R = C	—	—	±1.5	LSB
		T_R = I	—	—	±1.5	LSB
Logic Inputs						
I_{IH}	Input Leakage Current	$V_{IN} = V_{DD}$	—	—	10	µA
I_{IL}	Input Leakage Current	V_{IN} = 0V	—	—	–10	µA
V_{IH}	High Level Input Voltage		2	—	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	—	0.8	V
References						
V_{RH}	$V_{REF}H$ Input Voltage Range		2.7	—	V_{DD}	V
V_{RL}	$V_{REF}L$ Input Voltage Range		GND	—	V_{DD} -2.7	V
Z_{IN}	$V_{REF}H$–$V_{REF}L$ Resistance		—	7k	—	Ω
Logic Outputs						
V_{OH}	High Level Output Voltage	I_{OH} = – 40 µA	V_{DD} –0.3	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 1 mA, V_{DD} = +5V	—	—	0.4	V
		I_{OL} = 0.4 mA, V_{DD} = +3V	—	—	0.4	V

C ELECTRICAL CHARACTERISTICS (Cont.): V_{DD} = +3V to +5V ±10%, T_A = 25°C, $V_{REF}H$ = +V_{DD}, $V_{REF}L$ = 0V.

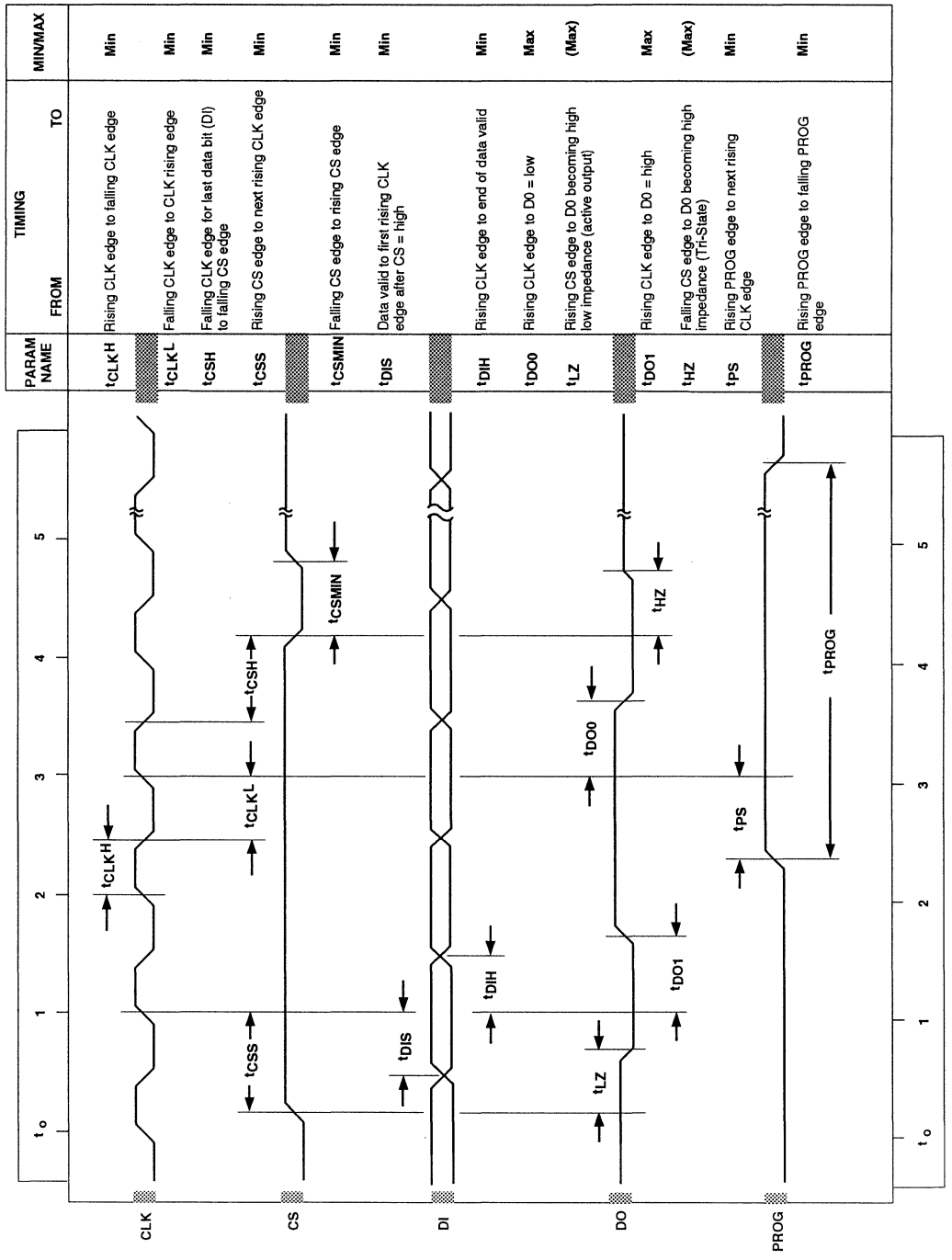
Symbol	Parameter	Conditions	Min	Typ	Max	Units
nalog Output						
FSO	Full-Scale Output Voltage	$V_R = V_{REF}H–V_{REF}L$	0.99 V_R	0.995 V_R	—	V
ZSO	Zero-Scale Output Voltage	$V_R = V_{REF}H–V_{REF}L$	—	0.005 V_R	0.10 V_R	V
IL	DAC Output Load Current		—	—	1	µA
ROUT	DAC Output Impedance	V_{DD} = +5V	—	—	20k	Ω
		V_{DD} = +3V	—	—	40k	Ω
PSSR	Power Supply Rejection	I_{LOAD} = 250 nA	—	—	1	LSB / V
emperature						
TCO	V_{OUT} Temperature Coefficient	$V_{REF}H$ = +5V, $V_{REF}L$ = 0V V_{DD} = +5V, I_{LOAD} = 250nA	—	—	200	µV/ °C
TCREF	Temperature Coefficient of V_{REF} Resistance	$V_{REF}H$ to $V_{REF}L$	—	700	—	ppm / °C
ower Supply						
IDD	Supply Current	Excludes V_{REF}	—	—	50	µA
IPP	Programming Current	V_{PP} = +19V	—	200	500	µA
VDD	Operating Voltage Range		2.7	—	5.5	V
VPP	Programing Voltage Range		18.0	19.0	20.0	V

C ELECTRICAL CHARACTERISTICS: V_{DD} = +3V to +5V ±10%, T_A = 25°C, $V_{REF}H$ = +V_{DD}, $V_{REF}L$ = 0V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
igital						
CSMIN	Minimum CS Low Time		150	—	—	ns
CSS	CS Setup Time		100	—	—	ns
CSH	CS Hold Time		0	—	—	ns
DIS	DI Setup Time	C_L = 100 pF,	50	—	—	ns
DIH	DI Hold Time	see note 1	50	—	—	ns
DO1	Output Delay to 1		—	—	150	ns
DO0	Output Delay to 0		—	—	150	ns
HZ	Output Delay to High-Z		—	400	—	ns
LZ	Output Delay to Low-Z		—	400	—	ns
PROG	Erase/Write Pulse Width		3	5	—	ms
PS	PROG Setup Time		150	—	—	ns
CLKH	Minimum CLK High Time		500	—	—	ns
CLKL	Minimum CLK Low Time		300	—	—	ns
C	Clock Frequency		DC	—	1	MHz
nalog						
DS	DAC Settling Time to 1/2 LSB	C_{LOAD} = 10 pF, V_{DD} = +5V	—	3	10	µs
		C_{LOAD} = 10 pF, V_{DD} = +3V	—	6	10	µs
CIN	Input Capacitance	V_{IN} = 0V, f = 1 MHz, (2)	—	8	—	pF
COUT	Output Capacitance	V_{OUT} = 0V, f = 1 MHz, (2)	—	6	—	pF

OTES: 1. All timing measurements are defined at the point of signal crossing V_{DD} / 2.
2. These parameters are periodically sampled and are not 100% tested.

A. C. TIMING DIAGRAM



IN DESCRIPTION

'in	Name	Function
	V_{DD}	Power supply positive.
	CLK	Clock input pin.Clock input pin.
	V_{PP}	EEPROM Programming Voltage
	CS	Chip Select
	DI	Serial data input pin.
	DO	Serial data output pin.
	PROG	EEPROM Programming Enable Input
	GND	Power supply ground.
	$V_{REF}L$	Minimum DAC output voltage.
0	$V_{OUT}4$	DAC output channel 4.
1	$V_{OUT}3$	DAC output channel 3.
2	$V_{OUT}2$	DAC output channel 2.
3	$V_{OUT}1$	DAC output channel 1.
4	$V_{REF}H$	Maximum DAC output voltage.

'EVICE OPERATION

'he CAT504 is a quad 8 bit Digital to Analog Converter)AC) whose outputs can be programmed to any one of 256 ıdividual voltage steps. Once programmed, these output :ttings are retained in non-volatile EEPROM memory and ill not be lost when power is removed from the chip. Upon ɔwer up the DACs return to the settings stored in EEPROM ıemory. Each DAC can be written to and read from ıdependently without effecting the output voltage during the :ad or write cycle. Each output can also be temporarily ljusted without changing the stored output setting, which is seful for testing new output settings before storing them in ıemory.

)IGITAL INTERFACE

'he CAT504 employs a standard 3 wire serial control interface ɔnsisting of Clock (CLK), Chip Select (CS) and Data In (DI) ıputs. For all operations, address and data are shifted in LSB rst. In addition, all digital data must be preceded by a logic "1" s a start bit. The DAC address and data are clocked into the)I pin on the clock's rising edge. When sending multiple locks of information a minimum of two clock cycles is required etween the last block sent and the next start bit.

Multiple devices may share a common input data line by electively activating the CS control of the desired IC. Data)utputs (DO) can also share a common line because the DO in is Tri-Stated and returns to a high impedance when not in se.

DAC addressing is as follows:

DAC OUTPUT	A0	A1
$V_{OUT}1$	0	0
$V_{OUT}2$	1	0
$V_{OUT}3$	0	1
$V_{OUT}4$	1	1

CHIP SELECT

Chip Select (CS) enables and disables the CAT504's read and write operations. When CS is high data may be read to or from the chip, and the Data Output (DO) pin is active. Data loaded into the DAC control registers will remain in effect until CS goes low. Bringing CS to a logic low returns all DAC outputs to the settings stored in EEPROM memory and switches DO to its high impedance Tri-State mode.

Because CS functions like a reset the CS pin has been equipped with a 30 ns to 90 ns filter circuit to prevent noise spikes from causing unwanted resets and the loss of volatile data.

CLOCK

The CAT504's clock controls both data flow in and out of the IC and EEPROM memory cell programming. Serial data is shifted into the DI pin and out of the DO pin on the clock's rising edge. While it is not necessary for the clock to be running between data transfers, the clock must be operating in order to write to EEPROM memory, even though the data being saved may already be resident in the DAC control register.

No clock is necessary upon system power-up. The CAT504's internal power-on reset circuitry loads data from EEPROM to the DACs without using the external clock.

As data transfers are edge triggered clean clock transitions are necessary to avoid falsely clocking data into the control registers. Standard CMOS and TTL logic families work well in this regard and it is recommended that any mechanical switches used for breadboarding or device evaluation purposes be debounced by a flip-flop or other suitable debouncing circuit.

V_{REF}

V_{REF}, the voltage applied between pins $V_{REF}H$ & $V_{REF}L$, sets the DAC's Zero to Full Scale output range where $V_{REF}L$ = Zero and $V_{REF}H$ = Full Scale. V_{REF} can span the full power supply range or just a fraction of it. In typical applications $V_{REF}H$ & $V_{REF}L$ are connected across the power supply rails. When using less than the full supply voltage $V_{REF}H$ is restricted to voltages between V_{DD} and $V_{DD}/2$ and $V_{REF}L$ to voltages between GND and $V_{DD}/2$.

VPP

When saving data to non-volatile EEPROM memory an external voltage of 18 - 20 volts must be applied to the VPP pin. This voltage need only be present during the programming cycle and may be removed or turned off the remainder of the time. While it is not necessary to remove or power down VPP between programming cycles, some power sensitive applications may choose to do so. In such cases, the VPP supply must be given sufficient time to come up and stabilize before issuing the PROG command.

DATA OUTPUT

Data is output serially by the CAT504, LSB first, via the Data Out (DO) pin following the reception of a start bit and two address bits by the Data Input (DI). DO becomes active whenever CS goes high and resumes its high impedance Tri-State mode when CS returns low. Tri-Stating the DO pin allows several 504s to share a single serial data line and simplifies interfacing multiple 504s to a microprocessor.

WRITING TO MEMORY

Programming the CAT504's EEPROM memory is accomplished through the application of an externally generated programming voltage, VPP, and the control signals: Chip Select (CS) and Program (PROG). With CS high, a start bit followed by a two bit DAC address and eight data bits are clocked into the DAC control register via the DI pin. Data enters on the clock's rising edge. The DAC output changes to its new setting on the clock cycle following D7, the last data bit.

Programming is achieved by bringing PROG high for minimum of 3 ms while supplying 18 to 20 volts to the Vpp pi PROG must be brought high sometime after the start bit a at least 150 ns prior to the rising edge of the clock cyc immediately following the D7 bit. Two clock cycles after t D7 bit the DAC control register will be ready to receive t next set of address and data bits. The clock must be ke running throughout the programming cycle. Internal contr circuitry takes care of ramping the programming voltage f data transfer to the EEPROM cells. The CAT504's EEPRO memory cells will endure over 100,000 write cycles and w retain data for a minimum of 20 years without being refreshe

READING DATA

Each time data is transferred into a DAC control regist currently held data is shifted out via the DI pin, thus in eve data transaction a read cycle occurs. Note, however, that t reading process is destructive. Data must be removed from t register in order to be read. Figure 2 depicts a Read Only cyc in which no change occurs in the DAC's output. This featu allows µPs to poll DACs for their current setting witho disturbing the output voltage but it assumes that the settir being read is also stored in EEPROM so that it can be restor at the end of the read cycle. In Figure 2 CS returns low befo the 13th clock cycle completes. In doing so the EEPROM setting is reloaded into the DAC control register. Since th value is the same as that which had been there previously n change in the DAC's output is noticed. Had the value held the control register been different from that stored in EEPRO then *a change would occur* at the read cycle's conclusion.

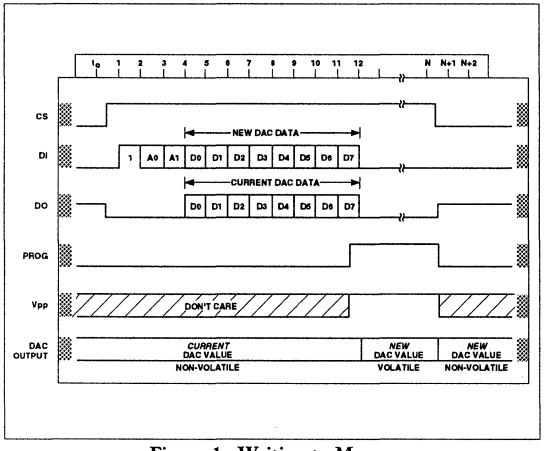


Figure 1. Writing to Memory

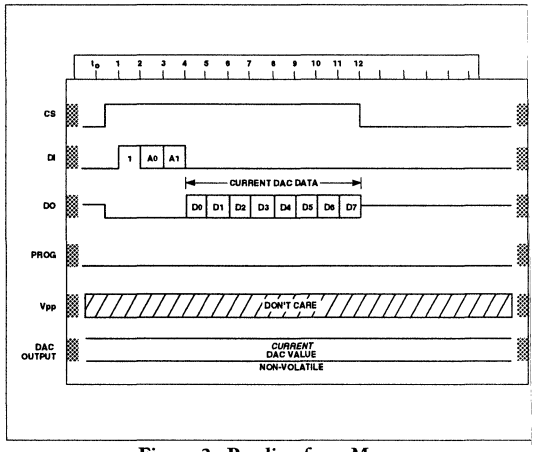


Figure 2. Reading from Memory

'EMPORARILY CHANGE OUTPUT

'he CAT504 allows temporary changes in DAC's output to e made without disturbing the settings retained in EEPROM ıemory. This feature is particularly useful when testing for a ew output setting and allows for user adjustment of preset or efault values without losing the original factory settings.

igure 3 shows the control and data signals needed to effect a :mporary output change. DAC settings may be changed as ıany times as required and can be made to any of the four)ACs in any order or sequence. The temporary setting(s) :main in effect long as CS remains high. When CS returns)w all four DACs will return to the output values stored in .EPROM memory.

Vhen it is desired to save a new setting acquired using this :ature, the new value must be reloaded into the DAC control :gister prior to programming. This is because the CAT504's ıternal control circuitry discards the new data from the rogramming register two clock cycles after receiving it (after :ception is complete) if no PROG signal is received.

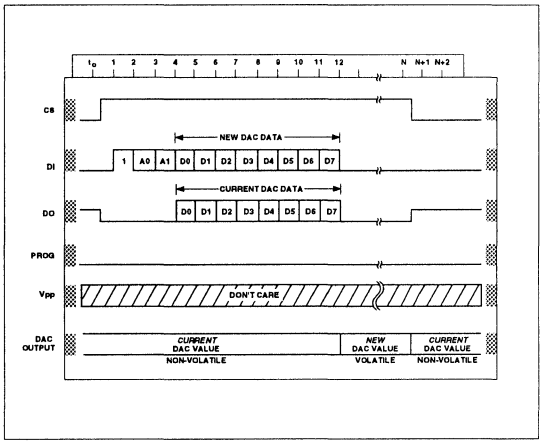
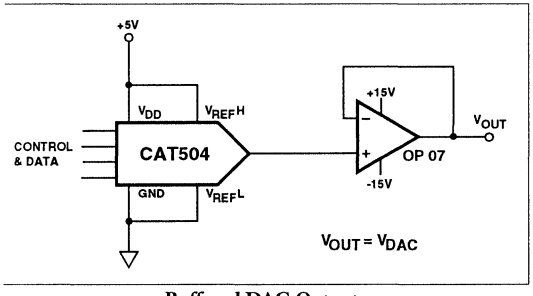
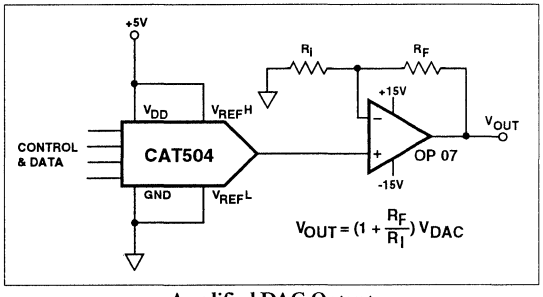


Figure 3. Temporary Change in Output

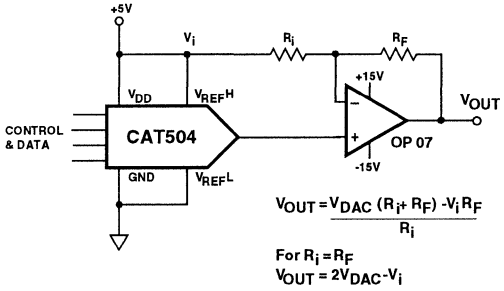
.PPLICATION CIRCUITS



Buffered DAC Output



Amplified DAC Output



DAC INPUT MSB	DAC INPUT LSB	DAC OUTPUT $V_{DAC} = \frac{CODE}{255} (V_{FS} - V_{ZERO}) + V_{ZERO}$ $V_{FS} = 0.99\ V_{REF}$ $V_{ZERO} = 0.01\ V_{REF}$	ANALOG OUTPUT $V_{REF} = 5V$ $R_I = R_F$
1111	1111	$\frac{255}{255}(.98\ V_{REF}) + .01\ V_{REF} = .990\ V_{REF}$	$V_{OUT} = +4.90V$
1000	0000	$\frac{128}{255}(.98\ V_{REF}) + .01\ V_{REF} = .502\ V_{REF}$	$V_{OUT} = +0.02V$
0111	1111	$\frac{127}{255}(.98\ V_{REF}) + .01\ V_{REF} = .498\ V_{REF}$	$V_{OUT} = -0.02V$
0000	0001	$\frac{1}{255}(.98\ V_{REF}) + .01\ V_{REF} = .014\ V_{REF}$	$V_{OUT} = -4.86V$
0000	0000	$\frac{0}{255}(.98\ V_{REF}) + .01\ V_{REF} = .010\ V_{REF}$	$V_{OUT} = -4.90V$

Bipolar DAC Output

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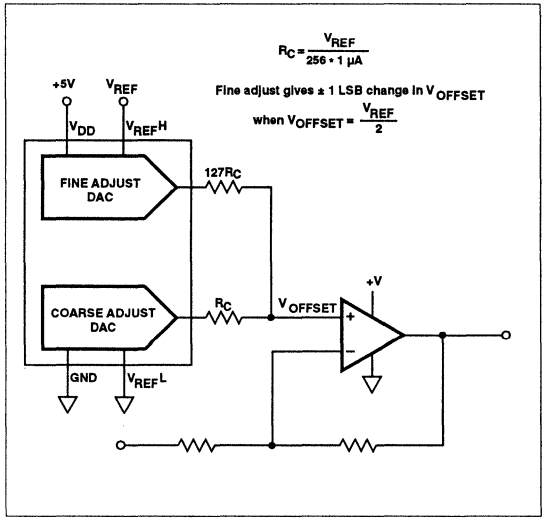
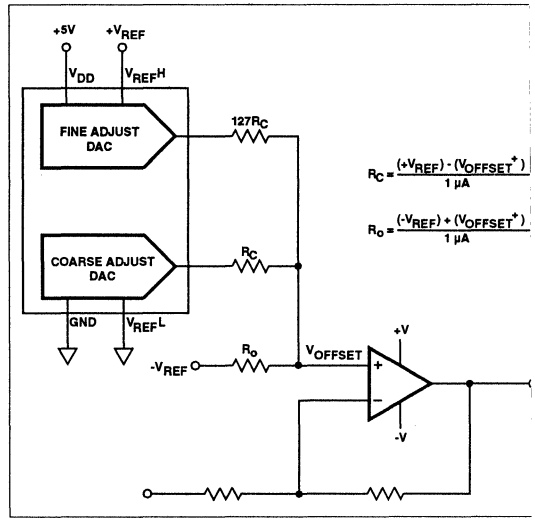
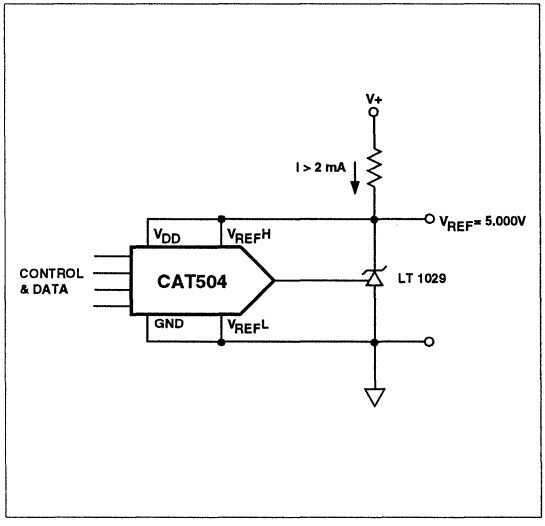
APPLICATION CIRCUITS (Cont.)



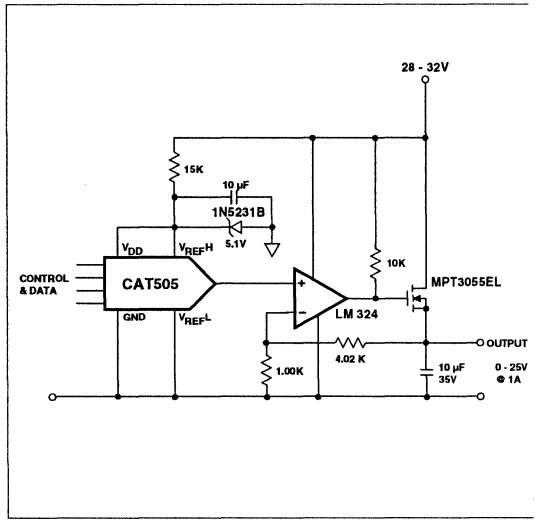
Coarse-Fine Offset Control by Averaging DAC Outputs for Single Power Supply Systems



Coarse-Fine Offset Control by Averaging DAC Outputs for Dual Power Supply Systems

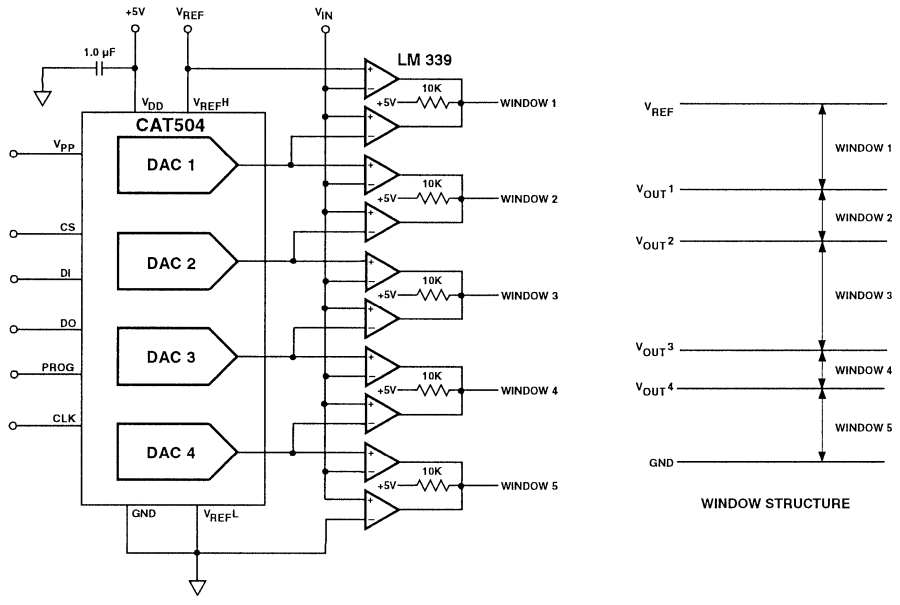


Digitally Trimmed Voltage Reference

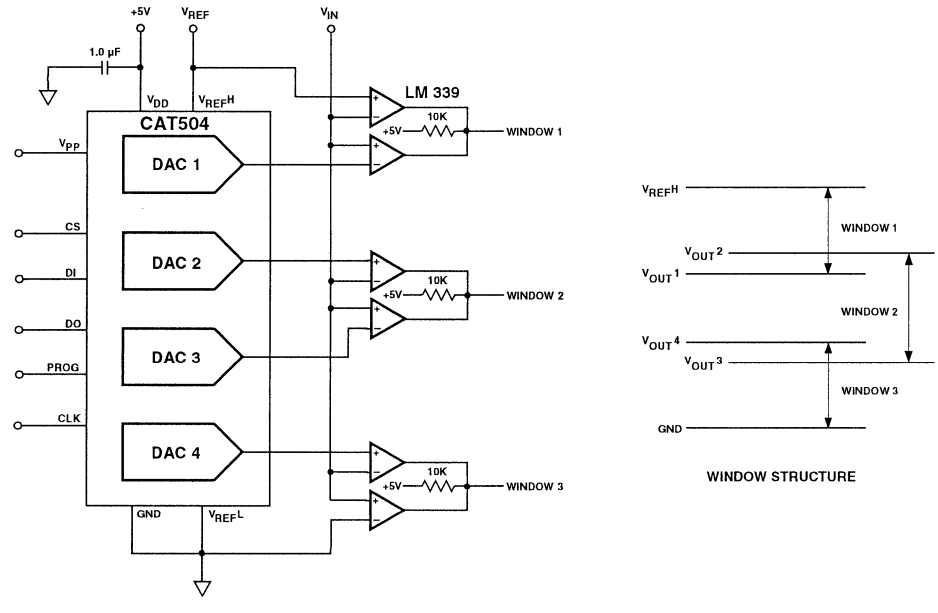


Digitally Controlled Voltage Reference

APPLICATION CIRCUITS (Cont.)

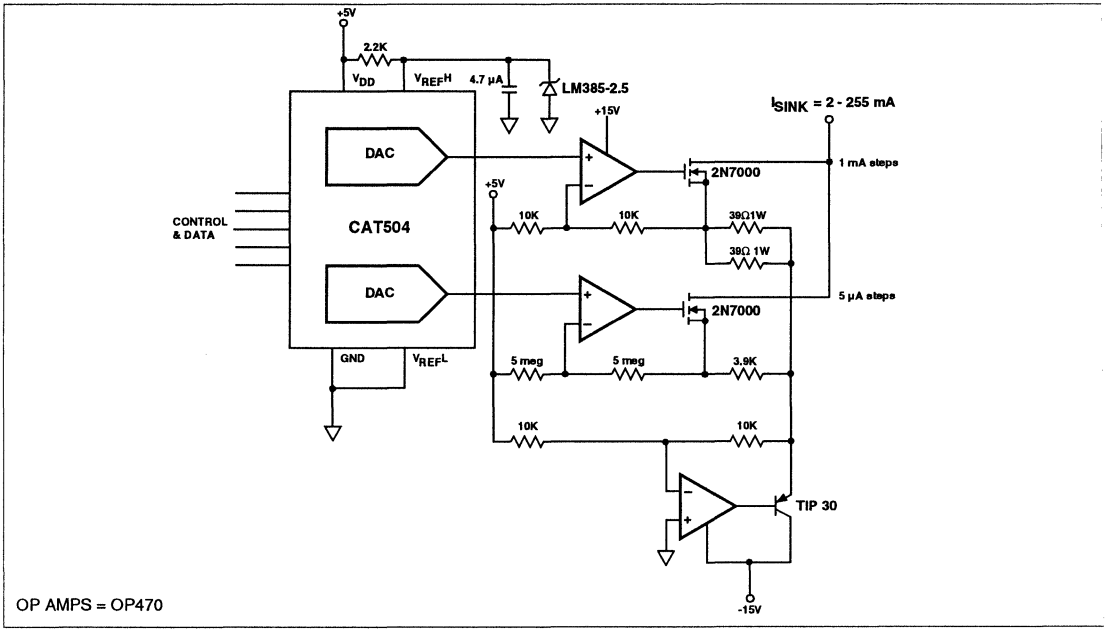


Staircase Window Comparator

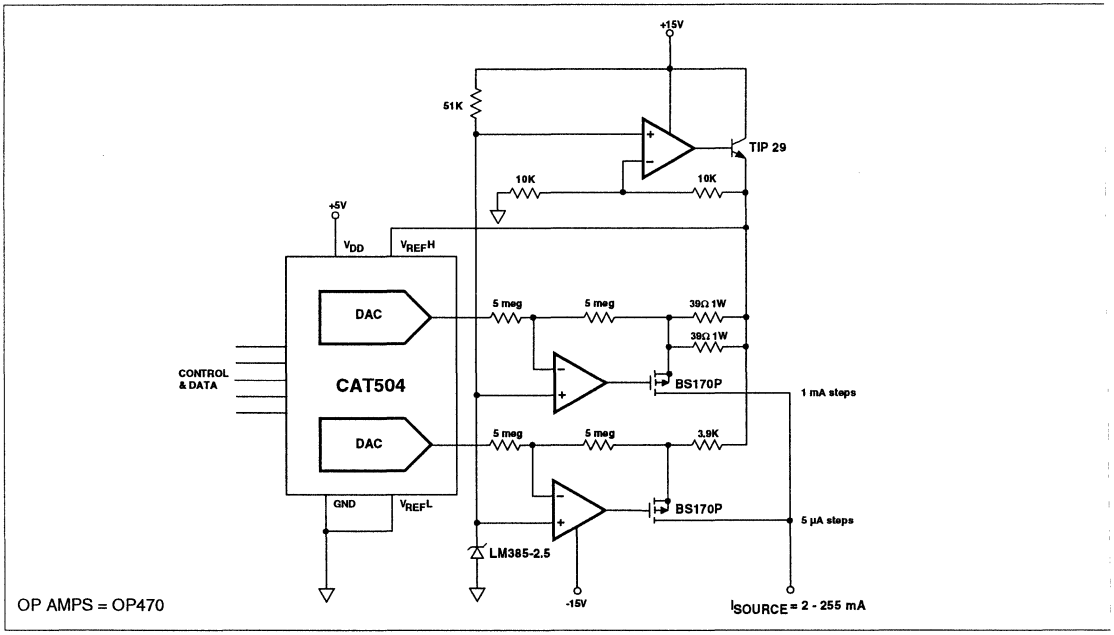


Overlapping Window Comparator

APPLICATION CIRCUITS (Cont.)

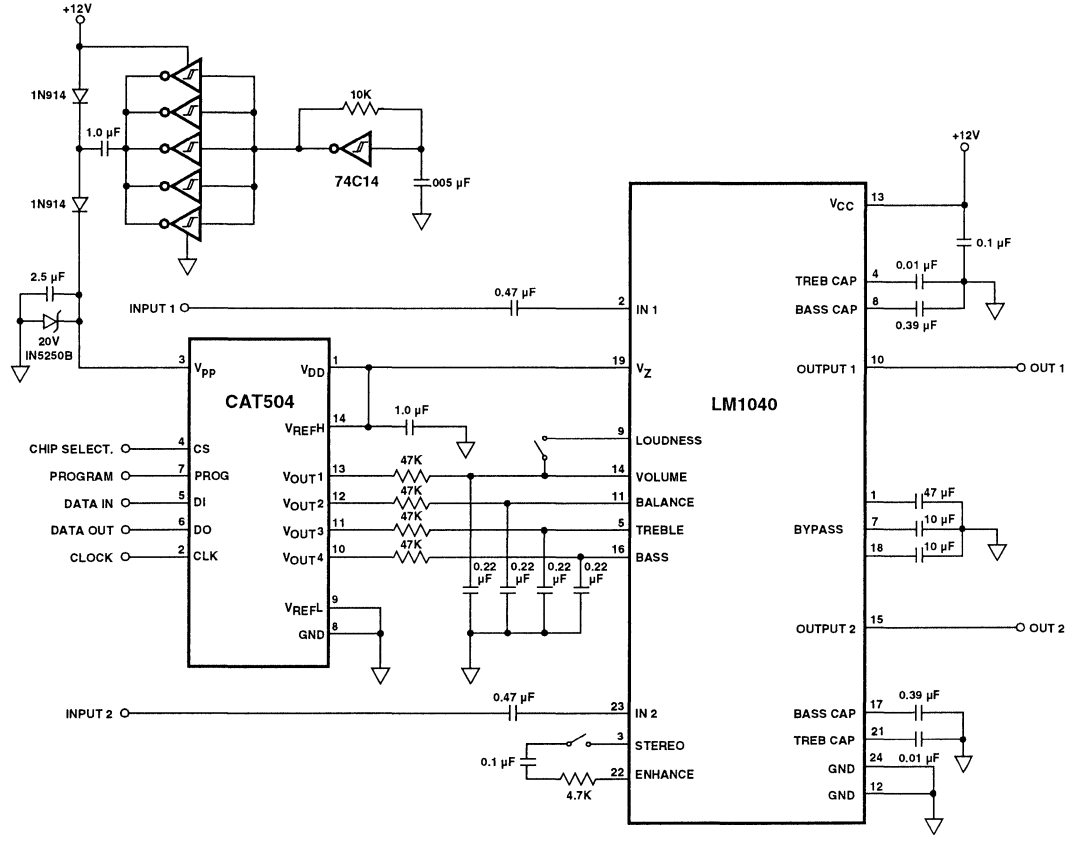


Current Sink with 4 Decades of Resolution



Current Source with 4 Decades of Resolution

APPLICATION CIRCUITS (Cont.)



Digital Stereo Control

CAT505

Quad DACpot

FEATURES

- Output settings retained without power
- Independent Reference Inputs
- Output range includes both supply rails
- Programming voltage generated on-chip
- 4 independently addressable outputs
- Serial µP interface
- Single supply operation: 3 - 5 Volts

APPLICATIONS

- Automated product calibration.
- Remote control adjustment of equipment
- Offset, gain and zero adjustments in Self-Calibrating and Adaptive Control systems.
- Tamper-proof calibrations.

DESCRIPTION

The CAT505 is a quad 8 Bit Memory DAC designed as an electronic replacement for mechanical potentiometers and trim pots. Intended for final calibration of products such as camcorders, fax machines and cellular telephones on automated high volume production lines and systems capable of self calibration, it is also well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous environment.

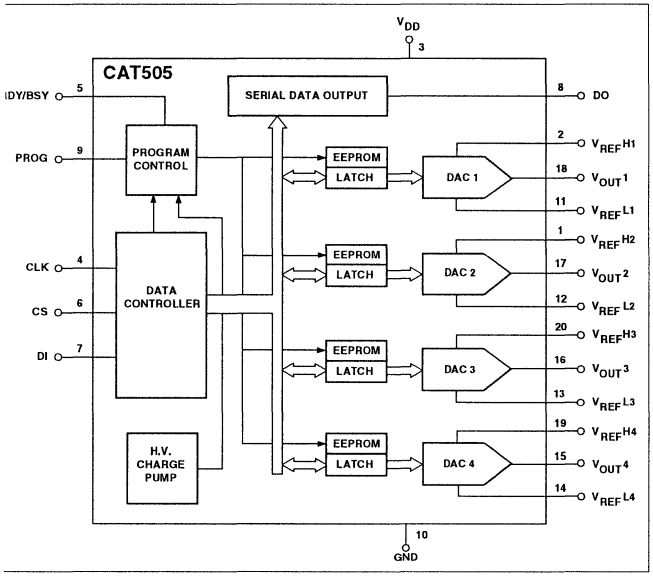
The CAT505 offers 4 independently programmable DACs each having its own reference inputs and each capable of rail to rail output swing. Output settings, stored non-volatile EEPROM memory, are not lost when the device is powered down and are automatically reinstated when power is returned. Each output can be dithered to test new output values without effecting the stored settings and stored settings can be read back without disturbing the DAC's output.

Control of the CAT505 is accomplished with a simple 3 wire serial interface. A Chip Select pin allows several CAT505s to share a common serial interface and communications back to the host controller is via a single serial data line thanks to the CAT505's Tri-Stated Data Output pin. A Rdy/Bsy output working in concert with an internal low voltage detector signals proper operation of EEPROM Erase/Write cycle.

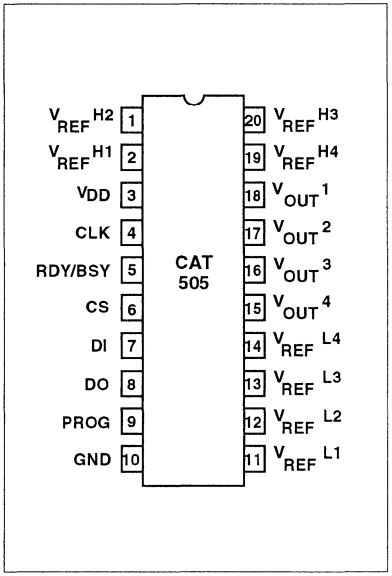
The CAT505 operates from a single 3 - 5 volt power supply. The high voltage required for EEPROM Erase/Write operations is generated on-chip.

The CAT505 is available in the 0 to 70° C Commercial and -40° C to + 85° C Industrial operating temperature ranges and offered in both plastic DIP and Surface mount packages.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



TD 5170

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V_{DD} to GND ..... –0.5V to +7V
- V_{PP} to GND ..... –0.5V to +22V

Inputs
- CLK to GND ..... –0.5V to V_{DD} +0.5V
- CS to GND ..... –0.5V to V_{DD} +0.5V
- DI to GND ..... –0.5V to V_{DD} +0.5V
- RDY/BSY to GND ..... –0.5V to V_{DD} +0.5V
- PROG to GND ..... –0.5V to V_{DD} +0.5V
- $V_{REF}H$ to GND ..... –0.5V to V_{DD} +0.5V
- $V_{REF}L$ to GND ..... –0.5V to V_{DD} +0.5V

Outputs
- D_0 to GND ..... –0.5V to V_{DD} +0.5V
- V_{OUT} 1– 4 to GND ..... –0.5V to V_{DD} +0.5V

Operating Ambient Temperature
- Commercial ('C' suffix) ..... 0°C to +70°C
- Industrial ('I' suffix) ..... – 40°C to +85°C

Junction Temperature ..... +150°C

ORDERING INFORMATION

Device	Package	Temp	INL
CAT505P	20 pin Plastic DIP	C	1 LSB
CAT505PI	20 pin Plastic DIP	I	1 LSB
CAT505J	20 pin SOIC	C	1 LSB
CAT505JI	20 pin SOIC	I	1 LSB

Temperature: C = 0°C to +70°C
I = – 40°C to +85°C

Storage Temperature ..... –65°C to +150°
Lead Soldering (10 sec max) ..... +300°

Stresses above those listed under Absolute Maximum Ratings m cause permanent damage to the device. Absolute Maximum Ratin are limited values applied individually while other parameters a within specified operating conditions, and functional operation at a of these conditions is NOT implied. Device performance and reliabil may be impaired by exposure to absolute rating conditions for extend periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Method
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(2)	Latch-Up	100		mA	JEDEC Standard 17

NOTES: 1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{DD} + 1V.

DC ELECTRICAL CHARACTERISTICS:

V_{DD} = +3V to +5V ±10%, T_A = 25°C
$V_{REF}H$ = V_{DD}, $V_{REF}L$ = 0V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Resolution		8	—	—	Bits
Accuracy						
INL	Integral Linearity Error	I_{LOAD} = 250 nA, T_R = C	—	0.6	± 1	LSB
		T_R = I	—	0.6	± 1	LSB
		I_{LOAD} = 1 µA, T_R = C	—	1.2	—	LSB
		T_R = I	—	1.2	—	LSB
DNL	Differential Linearity Error	I_{LOAD} = 250 nA, T_R = C	—	0.25	± 0.5	LSB
		T_R = I	—	0.25	± 0.5	LSB
		I_{LOAD} = 1 µA, T_R = C	—	0.5	—	LSB
		T_R = I	—	0.5	—	LSB
Logic Inputs						
I_{IH}	Input Leakage Current	V_{IN} = V_{DD}	—	—	10	µA
I_{IL}	Input Leakage Current	V_{IN} = 0V	—	—	–10	µA
V_{IH}	High Level Input Voltage		2	—	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	—	0.8	V
References						
V_{RH}	$V_{REF}H$ Input Voltage Range		2.7	—	V_{DD}	V
V_{RL}	$V_{REF}L$ Input Voltage Range		GND	—	V_{DD} -2.7	V
Z_{IN}	$V_{REF}H$–$V_{REF}L$ Resistance		—	28K	—	Ω
ΔV_{IN} / R_{IN}	Input Resistance Match		—	± 0.5	± 1	%
Logic Outputs						
V_{OH}	High Level Output Voltage	I_{OH} = – 40 µA	V_{DD} –0.3	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 1 mA, V_{DD} = +5V	—	—	0.4	V
		I_{OL} = 0.4 mA, V_{DD} = +3V	—	—	0.4	V

C ELECTRICAL CHARACTERISTICS (Cont.): V_{DD} = +3V to +5V ±10%, T_A = 25°C
$V_{REF}H = V_{DD}$, $V_{REF}L$ = 0V

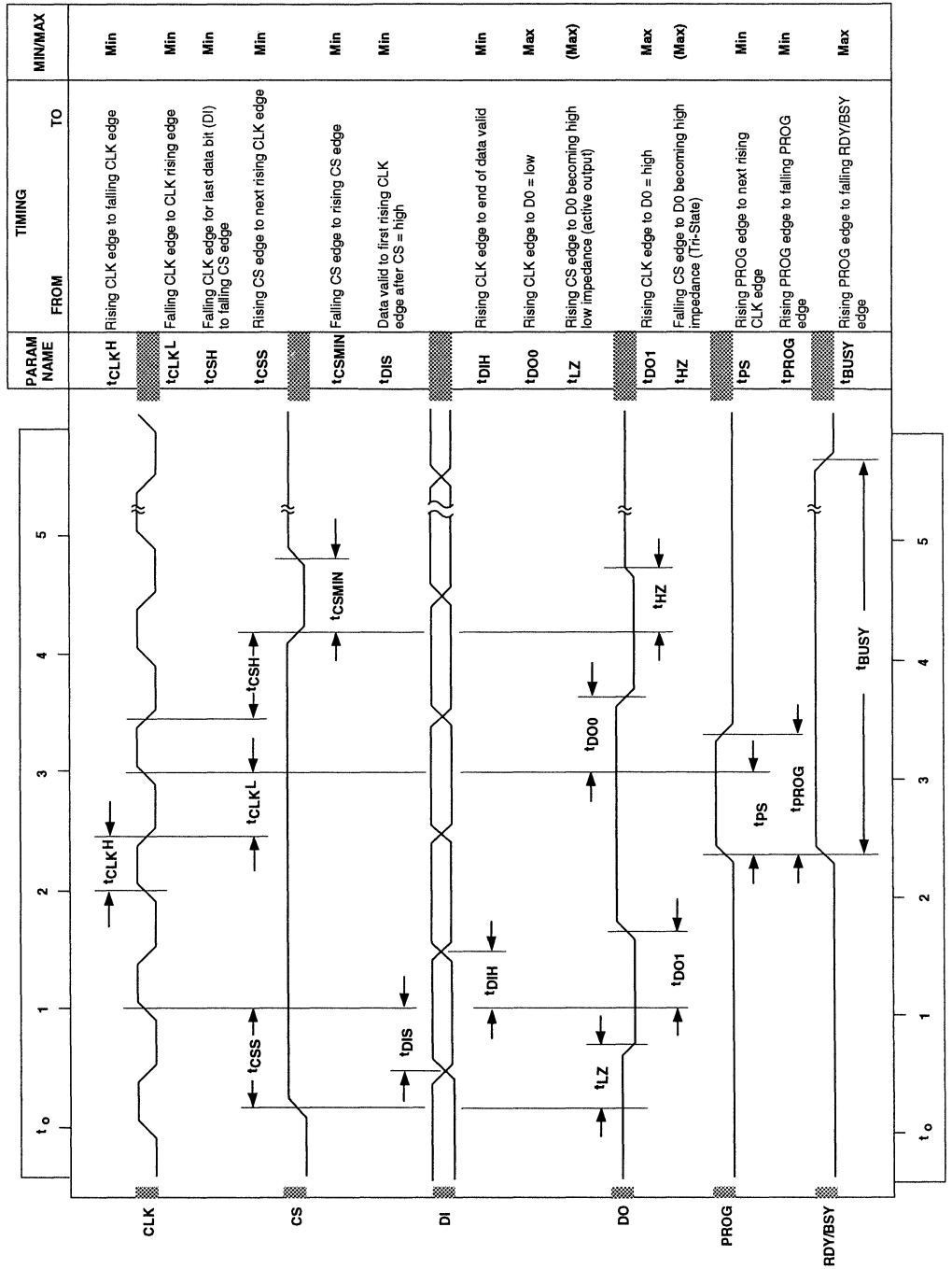
Symbol	Parameter	Conditions	Min	Typ	Max	Units
alog Output						
SO	Full-Scale Output Voltage	$V_R = V_{REF}H - V_{REF}L$	0.99 V_R	0.995 V_R	—	V
SO	Zero-Scale Output Voltage	$V_R = V_{REF}H - V_{REF}L$	—	0.005 V_R	0.10 V_R	V
	DAC Output Load Current		—	—	1	µA
OUT	DAC Output Impedance	$V_{DD} = V_{REF}H$ = +5V	—	—	25K	Ω
		$V_{DD} = V_{REF}H$ = +3V	—	—	40K	Ω
SR	Power Supply Rejection	I_{LOAD} = 1 µA	—	—	1	LSB / V
mperature						
CO	V_{OUT} Temperature Coefficient	V_{DD} = +5V, I_{LOAD} = 250nA $V_{REF}H$= +5V, $V_{REF}L$ = 0V	—	—	200	µV/ °C
CREF	Temperature Coefficient of V_{REF} Resistance	$V_{REF}H$ to $V_{REF}L$	—	700	—	ppm / °C
wer Supply						
DD	Supply Current (Excludes V_{REF})	Normal Operating	—	18	50	µA
		Programming, V_{DD} = 5V	—	1200	2000	µA
		V_{DD} = 3V	—	600	1200	µA
		CS = 0	—	300	250	µA
DD	Operating Voltage Range		2.7	—	5.5	V

C ELECTRICAL CHARACTERISTICS: V_{DD} = +3V to +5V ±10%, T_A = 25°C
$V_{REF}H = V_{DD}$, $V_{REF}L$ = 0V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
igital						
CSMIN	Minimum CS Low Time		150	—	—	ns
CSS	CS Setup Time		100	—	—	ns
CSH	CS Hold Time		0	—	—	ns
DIS	DI Setup Time	C_L = 100 pF,	50	—	—	ns
DIH	DI Hold Time	see note 1	50	—	—	ns
DO1	Output Delay to 1		—	—	150	ns
DO0	Output Delay to 0		—	—	150	ns
HZ	Output Delay to High-Z		—	400	—	ns
LZ	Output Delay to Low-Z		—	400	—	ns
BUSY	Erase/Write Cycle Time		—	3.3	5	ms
PS	PROG Setup Time		150	—	—	ns
PROG	Minimum Pulse Width		500	—	—	ns
CLKH	Minimum CLK High Time		500	—	—	ns
CLKL	Minimum CLK Low Time		300	—	—	ns
C	Clock Frequency		DC	—	1	MHz
nalog						
DS	DAC Settling Time to 1 LSB	C_{LOAD} = 10 pF, V_{DD} = +5V	—	3	10	µs
		C_{LOAD} = 10 pF, V_{DD} = +3V	—	6	10	µs
in Capacitance						
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1 MHz, (2)	—	8	—	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1 MHz, (2)	—	6	—	pF

OTES: 1. All timing measurements are defined at the point of signal crossing V_{DD} / 2.
2. These parameters are periodically sampled and are not 100% tested.

A. C. TIMING DIAGRAM



IN DESCRIPTION

'in	Name	Function
	$V_{REF}H2$	Maximum DAC 2 output voltage
	$V_{REF}H1$	Maximum DAC 1 output voltage
	V_{DD}	Power supply positive
	CLK	Clock input pin
	RDY/BSY	Ready / Busy output
	CS	Chip select
	DI	Serial data input pin
	DO	Serial data output pin
	PROG	EEPROM Programming Enable Input
0	GND	Power supply ground
1	$V_{REF}L1$	Minimum DAC 1 output voltage
2	$V_{REF}L2$	Minimum DAC 2 output voltage
3	$V_{REF}L3$	Minimum DAC 3 output voltage
4	$V_{REF}L4$	Minimum DAC 4 output voltage
5	$V_{OUT}4$	DAC 4 output
6	$V_{OUT}3$	DAC 3 output
7	$V_{OUT}2$	DAC 2 output
8	$V_{OUT}1$	DAC 1 output
9	$V_{REF}H4$	Maximum DAC 4 output voltage
10	$V_{REF}H3$	Maximum DAC 3 output voltage

)EVICE OPERATION

'he CAT505 is a quad 8 bit Digital to Analog Converter)AC) whose outputs can be programmed to any one of 256 ıdividual voltage steps. Once programmed, these output ettings are retained in non-volatile EEPROM memory and 'ill not be lost when power is removed from the chip. Upon ower up the DACs return to the settings stored in EEPROM ıemory. Each DAC can be written to and read from ıdependently without effecting the output voltage during the ead or write cycle. Each output can also be adjusted without ltering the stored output setting, which is useful for testing .ew output settings before storing them in memory.

)IGITAL INTERFACE

'he CAT505 employs a standard 3 wire serial control interface onsisting of Clock (CLK), Chip Select (CS) and Data In (DI) nputs. For all operations, address and data are shifted in LSB irst. In addition, all digital data must be preceded by a logic "1" s a start bit. The DAC address and data are clocked into the)I pin on the clock's rising edge. When sending multiple)locks of information a minimum of two clock cycles is re- ıuired between the last block sent and the next start bit.

Multiple devices may share a common input data line by ;electively activating the CS control of the desired IC. Data)utputs (DO) can also share a common line because the DO)in is Tri-Stated and returns to a high impedance when not in ıse.

DAC addressing is as follows:

DAC OUTPUT	A0	A1
$V_{OUT}1$	0	0
$V_{OUT}2$	1	0
$V_{OUT}3$	0	1
$V_{OUT}4$	1	1

CHIP SELECT

Chip Select (CS) enables and disables the CAT505's read and write operations. When CS is high data may be read to or from the chip, and the Data Output (DO) pin is active. Data loaded into the DAC control registers will remain in effect until CS goes low. Bringing CS to a logic low returns all DAC outputs to the settings stored in EEPROM memory and switches DO to its high impedance Tri-State mode.

Because CS functions like a reset the CS pin has been desensitized with a 30 ns to 90 ns filter circuit to prevent noise spikes from causing unwanted resets and the loss of volatile data.

CLOCK

The CAT505's clock controls both data flow in and out of the IC and EEPROM memory cell programming. Serial data is shifted into the DI pin and out of the DO pin on the clock's rising edge. While it is not necessary for the clock to be running between data transfers, the clock must be operating in order to write to EEPROM memory, even though the data being saved may already be resident in the DAC control register.

No clock is necessary upon system power-up. The CAT505's internal power-on reset circuitry loads data from EEPROM to the DACs without using the external clock.

As data transfers are edge triggered clean clock transitions are necessary to avoid falsely clocking data into the control registers. Standard CMOS and TTL logic families work well in this regard and it is recommended that any mechanical switches used for breadboarding or device evaluation purposes be debounced by a flip-flop or other suitable debouncing circuit.

V_{REF}

V_{REF}, the voltage applied between pins $V_{REF}H$ &$V_{REF}L$, sets the DAC's Zero to Full Scale output range where $V_{REF}L$ = Zero and $V_{REF}H$ = Full Scale. V_{REF} can span the full power supply range or just a fraction of it. In typical applications $V_{REF}H$ &$V_{REF}L$ are connected across the power supply rails. When using less than the full supply voltage be mindfull of the limits placed on $V_{REF}H$ and $V_{REF}L$ as specified in the **References** section of **DC Electrical Characteristics.**

READY/BUSY

When saving data to non-volatile EEPROM memory, the Ready/Busy ouput (RDY/BSY) signals the start and duration of the EEPROM erase/write cycle. Upon receiving a command to store data (PROG goes high) RDY/BSY goes low and remains low until the programming cycle is complete. During this time the CAT505 will ignore any data appearing at DI and no data will be output on DO.

RDY/BSY is internally ANDed with a low voltage detector circuit monitoring V_{DD}. If V_{DD} is below the minimum value required for EEPROM programming, RDY/BSY will remain high following the program command indicating a failure to record the desired data in non-volatile memory.

DATA OUTPUT

Data is output serially by the CAT505, LSB first, via the Data Out (DO) pin following the reception of a start bit and two address bits by the Data Input (DI). DO becomes active whenever CS goes high and resumes its high impedance Tri-State mode when CS returns low. Tri-Stating the DO pin allows several 505s to share a single serial data line and simplifies interfacing multiple 505s to a microprocessor.

WRITING TO MEMORY

Programming the CAT505's EEPROM memory is accomplished through the control signals: Chip Select (CS) and Program (PROG). With CS high, a start bit followed by a two bit DAC address and eight data bits are clocked into the DAC control register via the DI pin. Data enters on the clock's rising edge. The DAC output changes to its new setting on the clock cycle following D7, the last data bit.

Programming is accomplished by bringing PROG hig sometime after the start bit and at least 150 ns prior to the risin edge of the clock cycle immediately following the D7 bit. Tw clock cycles after the D7 bit the DAC control register will b ready to receive the next set of address and data bits. The cloc must be kept running throughout the programming cycl Internal control circuitry takes care of generating and rampin up the programming voltage for data transfer to the EEPRO cells. The CAT505's EEPROM memory cells will endure ov 100,000 write cycles and will retain data for a minimum of 2 years without being refreshed.

READING DATA

Each time data is transferred into a DAC control registe currently held data is shifted out via the DI pin, thus in ever data transaction a read cycle occurs. Note, however, that th reading process is destructive. Data must be removed from th register in order to be read. Figure 2 depicts a Read Only cycl in which no change occurs in the DAC's output. This featur allows µPs to poll DACs for their current setting withou disturbing the output voltage but it assumes that the settin being read is also stored in EEPROM so that it can be restore at the end of the read cycle. In Figure 2 CS returns low befor the 13th clock cycle completes. In doing so the EEPROM' setting is reloaded into the DAC control register. Since thi value is the same as that which had been there previously n change in the DAC's output is noticed. Had the value held i the control register been different from that stored in EEPRO then *a change would occur* at the read cycle's conclusion.

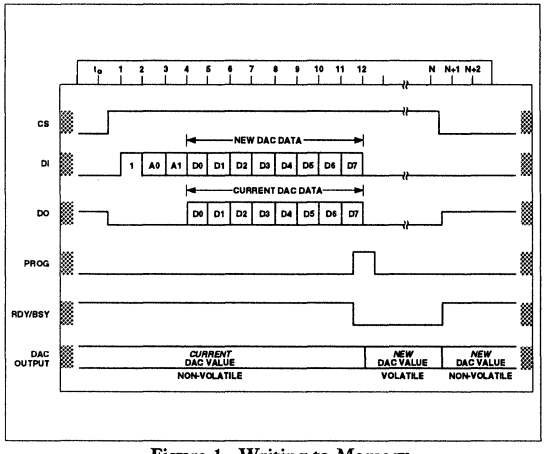


Figure 1. Writing to Memory

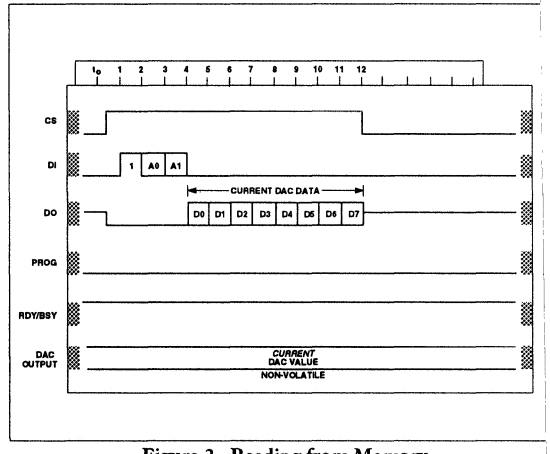


Figure 2. Reading from Memory

EMPORARILY CHANGE OUTPUT

he CAT505 allows temporary changes in DAC's output to made without disturbing the settings retained in EEPROM emory. This feature is particularly useful when testing for a ew output setting and allows for user adjustment of preset or efault values without losing the original factory settings.

igure 3 shows the control and data signals needed to effect a mporary output change. DAC settings may be changed as any times as required and can be made to any of the four ACs in any order or sequence. The temporary setting(s) main in effect long as CS remains high. When CS returns w all four DACs will return to the output values stored in EPROM memory.

hen it is desired to save a new setting acquired using this ature, the new value must be reloaded into the DAC control gister prior to programming. This is because the CAT505's ternal control circuitry discards from the programming gister the new data two clock cycles after receiving it if no ROG signal is received.

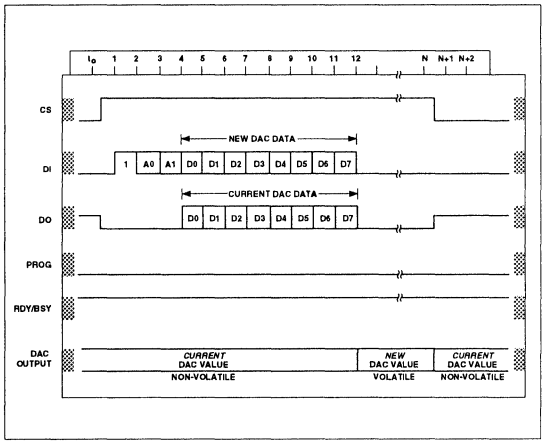
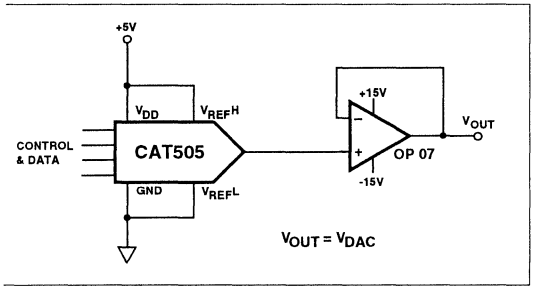
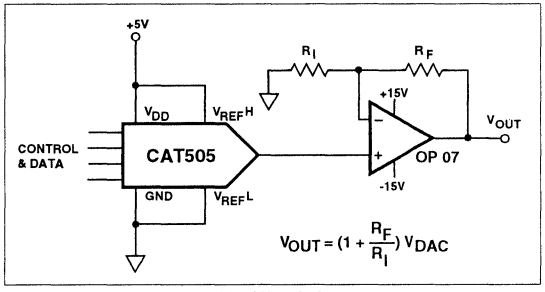


Figure 3. Temporary Change in Output

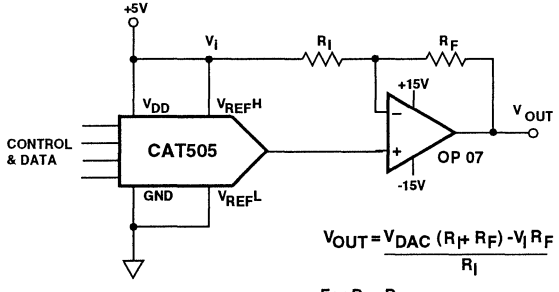
PPLICATION CIRCUITS



Buffered DAC Output



Amplified DAC Output

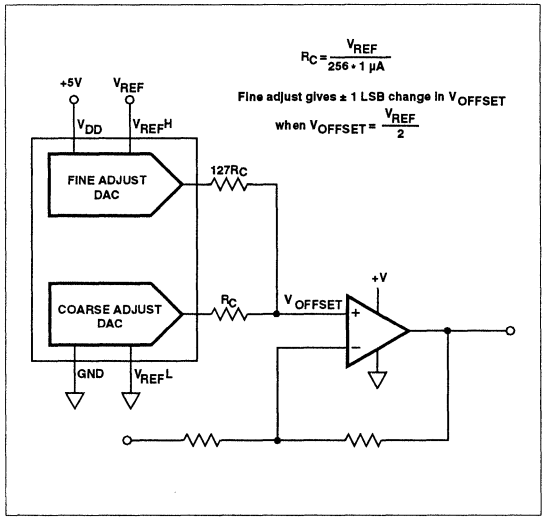


DAC INPUT		DAC OUTPUT	ANALOG OUTPUT
		$V_{DAC} = \frac{CODE}{255} (V_{FS} - V_{ZERO}) + V_{ZERO}$	
		$V_{FS} = 0.99\ V_{REF}$	$V_{REF} = 5V$
MSB	LSB	$V_{ZERO} = 0.01\ V_{REF}$	$R_I = R_F$
1111	1111	$\frac{255}{255} (.98\ V_{REF}) + .01\ V_{REF} = .990\ V_{REF}$	$V_{OUT} = +4.90V$
1000	0000	$\frac{128}{255} (.98\ V_{REF}) + .01\ V_{REF} = .502\ V_{REF}$	$V_{OUT} = +0.02V$
0111	1111	$\frac{127}{255} (.98\ V_{REF}) + .01\ V_{REF} = .498\ V_{REF}$	$V_{OUT} = -0.02V$
0000	0001	$\frac{1}{255} (.98\ V_{REF}) + .01\ V_{REF} = .014\ V_{REF}$	$V_{OUT} = -4.86V$
0000	0000	$\frac{0}{255} (.98\ V_{REF}) + .01\ V_{REF} = .010\ V_{REF}$	$V_{OUT} = -4.90V$

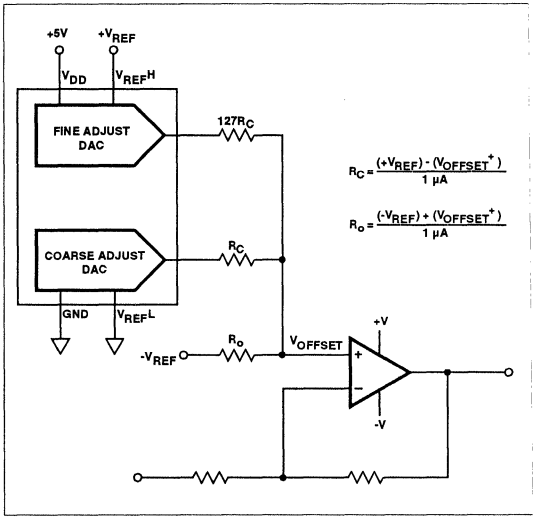
Bipolar DAC Output

11

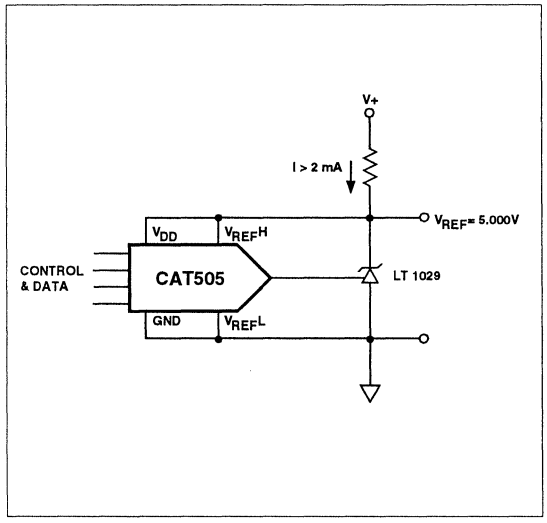
APPLICATION CIRCUITS (Cont.)



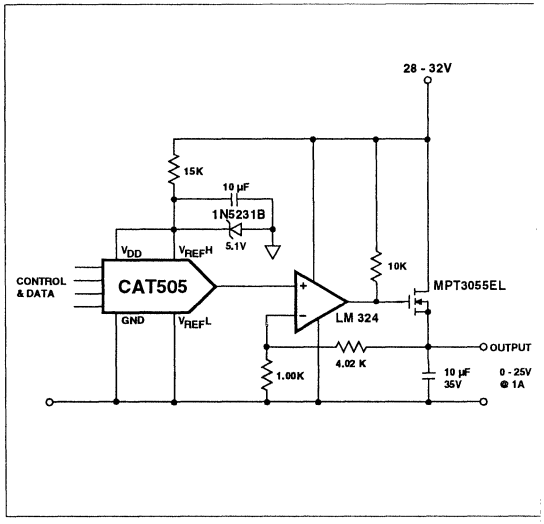
Coarse-Fine Offset Control by Averaging DAC Outputs for Single Power Supply Systems



Coarse-Fine Offset Control by Averaging DAC Outputs for Dual Power Supply Systems

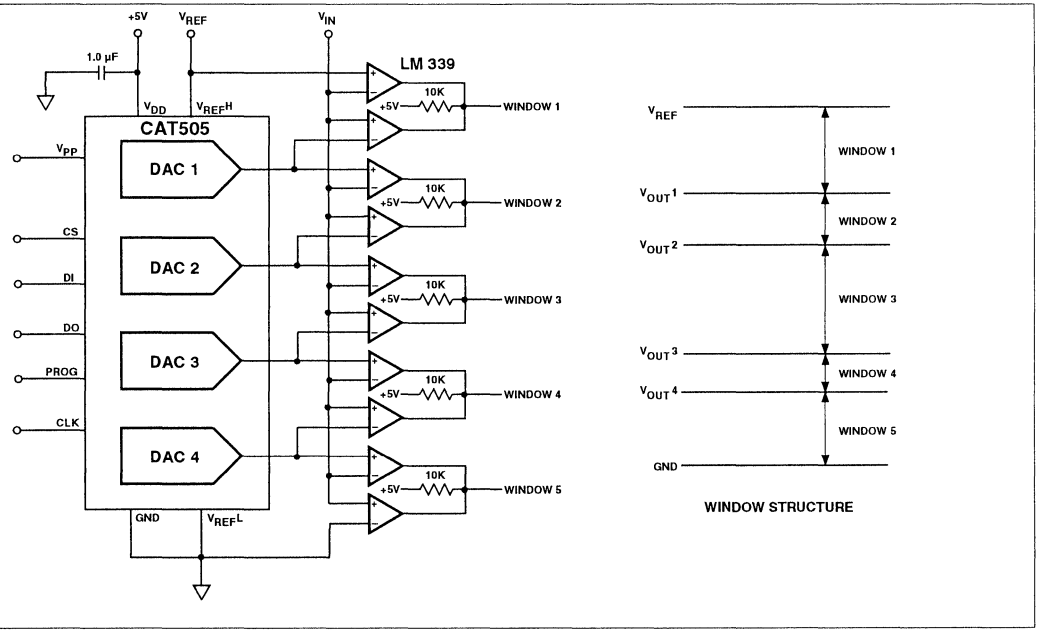


Digitally Trimmed Voltage Reference

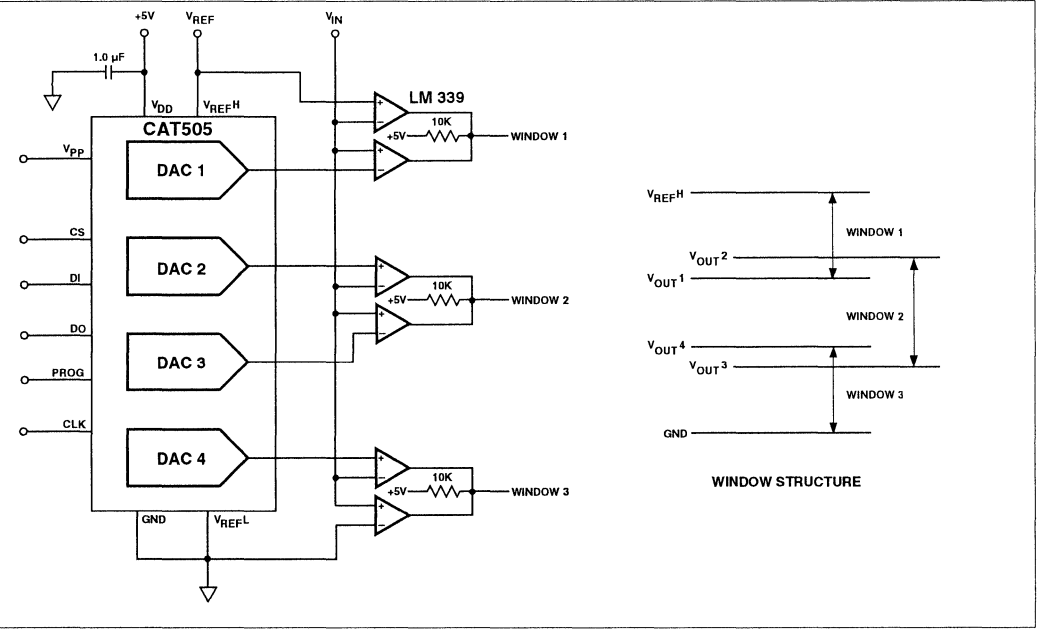


Digitally Controlled Voltage Reference

?PLICATION CIRCUITS (Cont.)



Staircase Window Comparator



Overlapping Window Comparator

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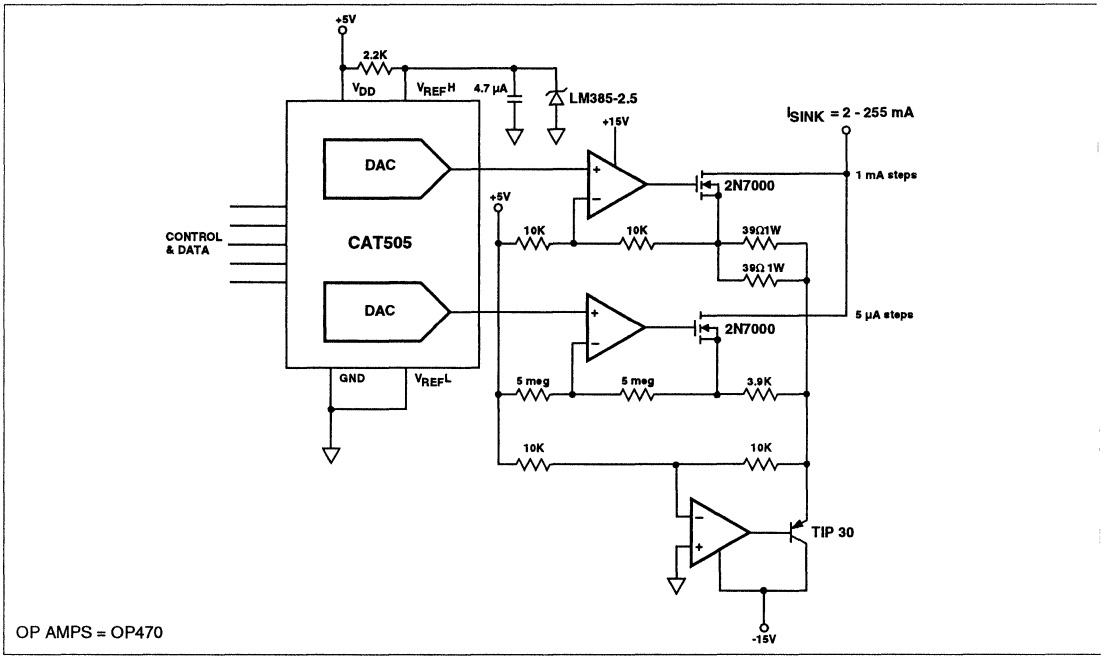
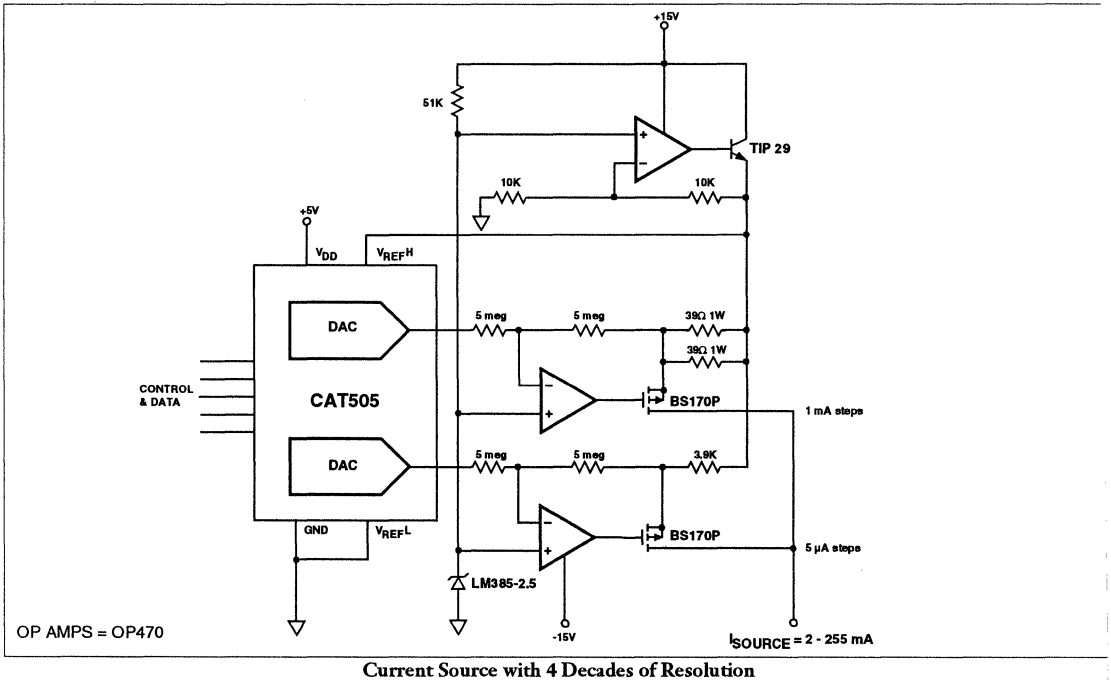
APPLICATION CIRCUITS (Cont.)



Current Sink with 4 Decades of Resolution



Current Source with 4 Decades of Resolution

RELIMINARY

CAT506

Bit, 40MHz D/A Converter

ATURES

25 ns maximum settling time (1/2 LSB)
40 MHz update rate
1/2 LSB Integral Non-Linearity
1/2 LSB Differential Non-Linearity
25 ppm/°C internal voltage reference
Low Power BiCMOS construction
Single Supply operation (+5 V)

PLICATIONS

Arbitrary Waveform Generators
Direct Digital Synthesis (DDS)
High Resolution A/D Converters
Automatic Test Equipment
High Definition Video

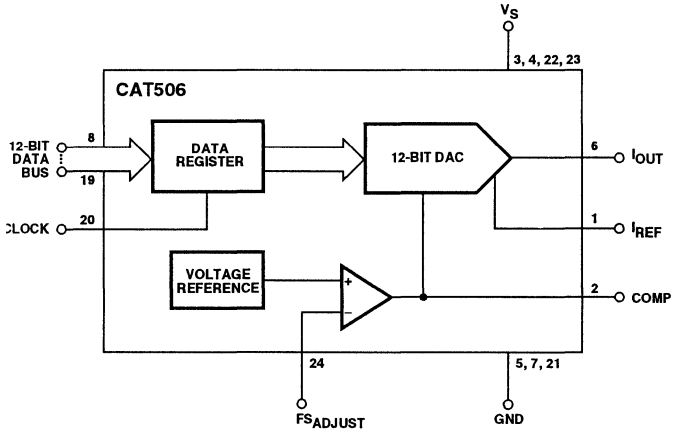
DESCRIPTION

The CAT506 is a monolithic 12 bit current output D/A converter designed for precision high speed data conversion applications. Powered from a single +5 Volt supply the CAT506 will source 40 mA of current into a 25 Ohm load at clock speeds of 40 MHz while maintaining 1/2 LSB accuracy. Settling time is 25 ns to .012% of Full Scale.

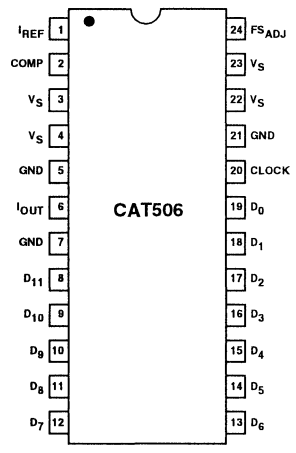
Fabricated in a 2.0 micron BiCMOS process, the CAT506 incorporate on-chip EEPROM driven trim circuitry for factory correction of all silicon and package induced errors. Gain error is adjusted to below <0.2 % and linearity to .012 %. Monotocity is guaranteed over the full operating temperature range. The CAT506 includes an on-chip voltage reference which is EEPROM trimmed to achieve a typical drift with temperature of 25 ppm/°C.

The CAT506 is pin compatible with Brooktree's Bt 105 while offering significantly improved performance. Packaged in Ceramic DIPs the CAT506 is specified for operation over the 0°C to +70°C Commercial temperature range.

JNCTIONAL DIAGRAM



PIN CONFIGURATION



TD 5171

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V_S to GND ..... –0.5V to +7V

Inputs
- D_0-D_{11} to GND ..... –0.5V to V_S +0.5V
- FS_{ADJUST} to GND ..... –0.5V to V_S +0.5V
- COMP to GND ..... –0.5V to V_S +0.5V
- CLOCK to GND ..... –0.5V to V_S +0.5V
- I_{REF} ..... ±10 mA

Outputs
- Analog Output Current (I_{OUT}) ..... 50 mA
- Analog Output Voltage (I_{OUT}) ..... V_S^- 7V to V_S^+ 0.5V
- Analog Output Short Circuit Duration ..... Infinite

Operating Ambient Temperature
- Commercial ('C' suffix) ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Lead Soldering (10 sec max) ..... +300°C

ORDERING INFORMATION

Device	Package	Temp	INL
CAT506AC	24 pin Ceramic DIP	C	1/2 LS
CAT506BC	24 pin Ceramic DIP	C	1 LSE

Temperature: C = 0°C to +70°C

Stresses above those listed under Absolute Maximum Ratings m cause permanent damage to the device. Absolute Maximum Ratir are limited values applied individually while other parameters within specified operating conditions, and functional operation at a of these conditions if NOT implied. Device performance and reliabil may be impaired by exposure to absolute rating conditions for extenc periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Method
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(2)	Latch-Up	100		mA	JEDEC Standard 17

NOTES: 1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_S + 1V.

DC ELECTRICAL CHARACTERISTICS: V_S = +5V ±0.25V; T_A = 0°C to +70°C; I_{OUT} (FS) = 40mA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Resolution			12	—	—	Bits
Accuracy						
INL	Integral Linearity Error	CAT506A	—	—	±1/2	LSB
		CAT506B	—	—	±1	LSB
DNL	Differential Linearity Error		—	—	±1/2	LSB
	Zero Offset Error		—	—	1.0	µA
	Gain Error	Internal Reference	—	±0.15	±0.3	%FS
		External Reference	—	—	±1.0	%FS
	Monotocity		Guaranteed			
Coding						
	I_{OUT}	D_0-D_{11} = 0	0	—	—	
	I_{OUT}	D_0-D_{11} = 1	—	—	Full Scale	
Data Inputs						
V_{IH}	High Level Input Voltage		2	—	—	V
V_{IL}	Low Level Input Voltage		—	—	0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4V	—	—	1.0	µA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V	—	—	–1.0	µA
Analog Output						
I_{OUT}	Output Current		10	—	40	mA
V_{OUT}	Output Compliance		–1.0	—	+1.0	V
R_{OUT}	Output Impedance		—	1	—	MΩ
TC_{GAIN}	Gain Temperature Coefficient		—	—	30	ppm/°C
Reference						
I_{REF} (Pin 1)	Operating Voltage Range		–0.3	0.68	1.0	V
V_{REF}	Internal Reference Voltage		0.67	0.68	0.69	V
TC_{VREF}	Temperature Coefficient		—	+25	—	ppm/°C

C ELECTRICAL CHARACTERISTICS (Cont.): V_S = +5V ±0.25V; T_A = 0°C to +70°C; I_{OUT} (FS) = 40mA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ower Supply						
V_S	Supply Voltage Range		4.5	5	6	V
I_S	Supply Current	40 MHz, I_{OUT} = 40 mA	—	60	75	mA
PSRR	Power Supply Rejection Ratio	COMP = 0.01 µF, f = 1 kHz	—	0.02	0.5	%/%ΔV_S

C ELECTRICAL CHARACTERISTICS: V_S = 5V ±0.25V; R_L = 25Ω; I_{OUT} (FS) = 40 mA.
Logic inputs: 0V-3V; t_r and t_f < 3 ns; T_A = 0°C to +70°C.

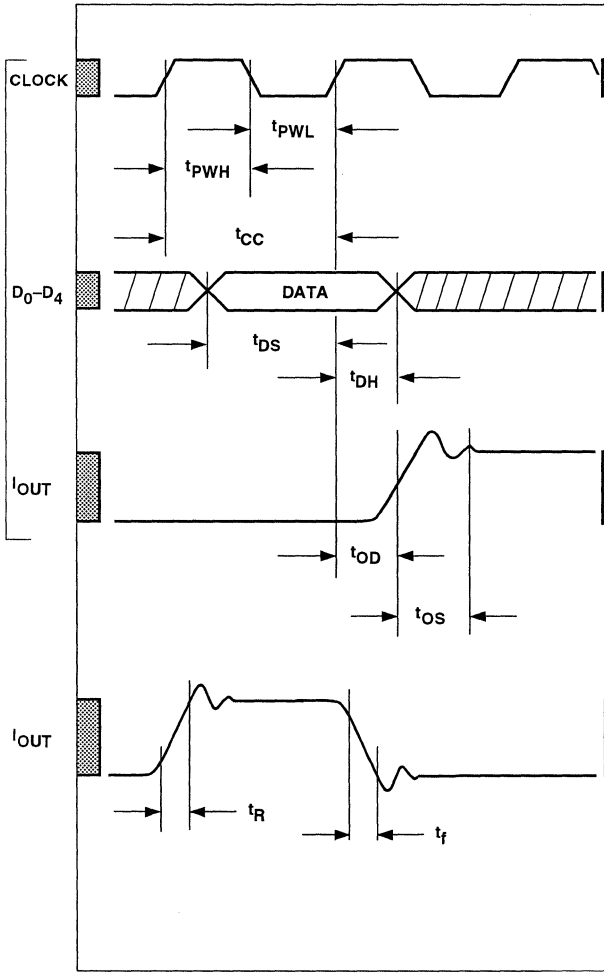
Symbol	Parameter	Conditions	Min	Typ	Max	Units
ata Inputs						
f_{MAX}	Register Clock Rate		—	—	40	MHz
t_{CC}	Clock Cycle Time		25	—	—	ns
t_{PWH}	Clock Pulse Width High Time		10	—	—	ns
t_{PWL}	Clock Pulse Width Low Time		10	—	—	ns
t_{DS}	Data Setup Time		10	—	—	ns
t_{DH}	Data Hold Time		2	—	—	ns
	Pipeline Delay	CAT506 Only	1	1	1	Clock
nalog Output						
t_{OD}	Output Delay		—	18	—	ns
t_R	Output Rise Time		—	5	—	ns
t_F	Output Fall Time		—	5	—	ns
t_{OS}(1)	Output Settling Time	To 0.012% of FS	—	22	35	ns
		To 0.025% of FS	—	20	30	ns
		To 0.10% of FS	—	12	25	ns
	Clock and Data Feedthrough(1)		—	- 40	—	dB
	Glitch Impulse(1)		—	100	—	pV-sec
	Differential Gain Error		—	1.5	—	%FS
	Differential Phase Error		—	1.5	—	Degrees
SINAD	f_{CLK} = 20 MHz f_{OUT} = 500 KHz		—	59	—	dB
	f_{OUT} = 1 MHz		—	58	—	dB
	f_{CLK} = 5 MHz f_{OUT} = 500 KHz		—	65	—	dB
	f_{OUT} = 1 MHz		—	64	—	dB
in Capacitance						
C_{IN}	Input Capacitance, D_0-D_{11}, CLK	V_{IN} = 2.4V, f = 1 MHz	—	10	—	pF
C_{OUT}	Output Capacitance, Pin 6	I_{OUT} = 0 mA, f= 1 MHz	—	25	—	pF

OTES: 1. Clock and Data feedthrough is function of the magnitude of overshoot and undershoot on the digital inputs. While testing, the digital inputs have a 1k ohm resistor connected to the regular PCB ground plane and are driven by 74 HC logic. Clock and data feedthrough are excluded from the settling time, where as they are included in glitch impulse. (Test bandwidth = 100 MHz.)

11

AC TIMING DIAGRAM

CAT506



PARAMETER NAME	MEASURED FROM	MEASURED TO	MIN MAX
t_{PWL}	FROM:	50% point of falling edge	Min
	TO:	50% point of rising edge	
t_{PWH}	FROM:	50% point of rising edge	Min
	TO:	50% point of falling edge	
t_{CC}	FROM:	50% point of rising edge	Min
	TO:	50% point of next rising edge	
t_{DS}	FROM:	Data valid	Min
	TO:	50% point of clock's next rising edge	
t_{DH}	FROM:	End of t_{DS} period	Min
	TO:	data invalid	
t_{OD}	FROM:	50% point of clock's rising edge	Max
	TO:	50% of FS output	
t_{OS}	FROM:	50% of FS output	Max
	TO:	Output within allowed error band (1/2 LSB or 1 LSB)	
t_R	FROM:	10% point of FS output	Max
	TO:	90% point of FS output	
t_F	FROM:	90% point of FS output	Max
	TO:	10% point of FS output	

NS

n No.	Name	Function
	I_{REF}	Reference Current Output. The DAC's full scale output current is set by I_{REF}, which is normaly connected to FS_{ADJUST} and a resistor, R_{SET}. The full scale output current is then determined by the value of R_{SET}.
	COMP	Compensation pin. This pin must be connected to the V_S pin through a ceramic capacitor. This capacitor provides power supply noise rejection and reduces the random noise of the internal bandgap reference. The capacitor can be between 0.01 µF and 0.1 µF, with 0.01µF being the recommended value. When an external reference voltage is used COMP is used in conjunction with FS_{ADJUST} to set I_{REF}.
4, 22, 23	V_S	The positive supply voltage, nominally +5V.
7,21	GND	Ground return for all signals (digital and analog) and V_S.
	I_{OUT}	Analog Current Output. This high impedance current source is capable of sourcing up to 40 mA of current.
19	D_0-D_{11}	TTL compatible Data Inputs. Pin D_0 is the least significant data bit. For CAT506, the inputs are latched on the rising edge of clock. All unused inputs must be tied to V_S or GND.
	Clock	Clock Input for CAT506. The rising edge of Clock latches the D_0-D_{11} inputs. Ideally, this pin should be driven by a dedicated TTL/CMOS buffer.
	FS_{ADJUST}	Full Scale Adjust Control. When the internal reference voltage is used, the full scale output current is controlled by the resistor R_{SET}, connected between this input pin and GND. When an external voltage reference is used, FS_{ADJUST} is tied to V_S.

ERMS AND DEFINITIONS

ifferential Non-Linearity (DNL): The maximum deviaon from an ideal LSB step, between any two adjacent output vels. A DNL error more negative than -1LSB implies nononotonic output performance.

ıll Scale Output Current: The output current at I_{out} sulting from all 1's at the data inputs.

ain Error: The variation in the slope (gain) of the transfer nction of a converter with respect to an established ideal ansfer function. This error is expressed in % of FS (Full Scale) · LSB, when all bits are on, and may be eliminated by ljusting the reference current applied to the device.

litch Impulse Area: The analog output transient occurring :tween two adjacent codes as a result of unequal turn-on and ırn-off times for the internal current sources. Glitch impulse calculated as the area of the largest excursion, about the final ılue, and is specified as the net area of the glitch in nV-sec or A-sec.

ıtegral Non-Linearity (INL): The maximum deviation beveen the actual output level and a best straight line fit. This ccludes gain and offset errors.

Least-Significant Bit (LSB): The ideal output increment between two adjacent codes. Also, the data bit with the smallest effect on the output level.

Monotonicity: Implies that for an increase in digital code value that the output will either increase or remain unchanged. In mathematical terms the output is a single valued function of the input code, and the derivative of the output transfer function must not change signs.

Most-Significant Bit (MSB):The data bit with the largest effect on the output level. The MSB, for a linear DAC output, ideally equals the combined output weight of all other data bits, plus 1 LSB.

Offset Error: The deviation of the analog output from the ideal (0V or 0mA) when the inputs are set to all 0s is called unipolar offset error.

Output Compliance Range: The output voltage range over which a stated linearity specification is maintained. Integral linearity errors tend to be exaggerated with increasing output voltage levels.

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CURRENT vs VOLTAGE OUTPUT

The CAT506 has been carefully designed to work equally well in both current and voltage output applications, a claim not all DACs can make. When using other DACs, designers may be forced to use additional circuitry or be obliged to accept reduced performance when voltage output is required.

High speed DACs give their best performance in current output mode. This is because in current output operation the DAC's output is tied to a summing junction, such as the negative input of an op amp, and feedback around the op amp holds the junction voltage constant (usually 0 volts). Since no voltage change occurs at the DAC's output the DAC is uneffected by load resistance, R_L , or any other impedances internal or external to the DAC.

When generating a voltage output, however, R_L can have a significant effect on the DAC's performance. The problem is caused by the DAC's own output impedance. As shown in Fig1 a DAC's output can be modeled as a current source in parallel with an internal resistance. When an external load is connected to I_{OUT}, it is in parallel with the internal resistance and the actual load seen by the DAC is the combination of their values. In developing an output voltage, I_{OUT} is split between internal and external loads, producing an apparent error in V_{OUT} . The degree of error is determined by the ratio of R_L to the internal shunt resistance. For ideal current sources the shunt resistance is infinite, but in typical high speed DACs it ranges from 200 to 20,000 Ω. This will produce a significant loading effect, even with the 50 Ω or 25 Ω loads commonly used in high speed systems.

To combat this problem, Catalyst has taken special care to create a true current source output structure for the CAT506. The 1 MΩ output impedance of the CAT506 frees designers from concerns about voltage induced errors and voltage outputs can be had with no penalty in performance.

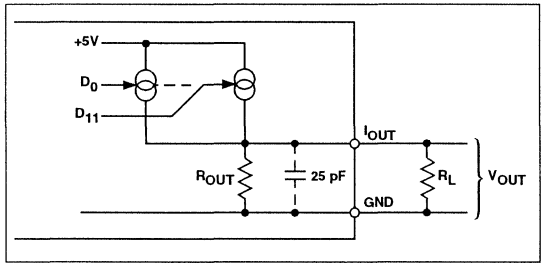

Figure 1. DAC Output Equivalent Circuit

OUTPUT VOLTAGE COMPLIANCE

The maximum voltage that may be realized at the DAC's output, while maintaining rated accuracy and performance, is 1.0 volts. Care should be taken when selecting R_L and I_{OUT} that the resulting Full Scale voltage does not exceed this value. Also, when operating into a summing junction (current mode), be sure the DC voltage of the summing node is below 1.0 volts.

BUFFERED VOLTAGE OUTPUTS

For applications requiring output voltages greater than 1 volts a buffering amplifier will be required. Figure 2 illustrat a typical buffered output application.

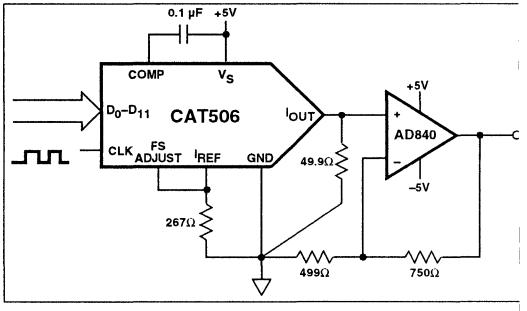

Figure 2. Buffer Voltage Output 0 to +2.5V

FULL SCALE ADJUST

The CAT506 output can be adjusted for any desired le between 0 - 1.0V or 0 - 40 mA via the FS_{ADJUST} pin. Referri to Figure 3, I_{REF}, which sets the DAC's Full Scale output curre is controlled by op amp A1. The control loop is configured so th A1 will maintain a constant 0.68 volts at the FS_{ADJUST} pin. I_{REF} has a maximum compliance voltage of 1.0 volts, it is best use R_{TRIM} as a variable resistor in series with R_{SET} and tie FS_{ADJU} directly to I_{REF}. This avoids the possibility of the voltage acr the combination of R_{TRIM} and R_{SET} exceeding I_{REF}'s complian range.

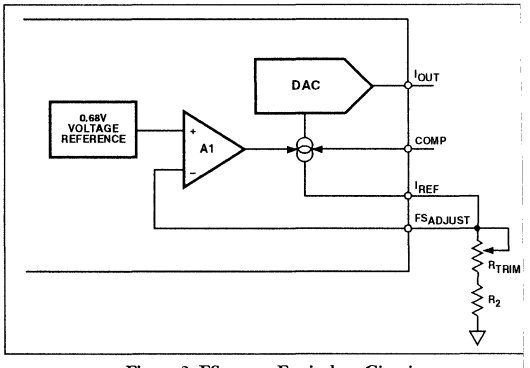

Figure 3. FS_{ADJUST} Equivalent Circuit

)SING THE INTERNAL VOLTAGE REFERENCE

. precision voltage reference is provided by the CAT506 to llow for easy adjustment and control of I_{REF}, which sets the)AC full scale output current, I_{OUT}. The relationship be- ween I_{OUT} and I_{REF} is:

$$I_{OUT} = 7.892 * I_{REF}$$

'SET is then calculated from the equation:

$$R_{SET} = \frac{7.892 * V_{REF}}{I_{OUT}}$$

Vhere V_{REF} = 0.68 V.

The internal reference is factory trimmed to compensate for variations in the transfer ratio of I_{REF} to I_{OUT}, making the full scale output voltage accurate to within 0.3% for the transfer function:

$$V_{OUT} = 5.367 * \frac{R_L}{R_{SET}}$$

Full scale output voltage variation from device to device will be ±0.3% when there is perfect tracking between the load and reference current resistors. For optimum performance, R_{SET} and R_L should be a trimmed resistor network with ratio tracking better than ±0.1% and temperature coefficient tracking better than 5 ppm/°C.

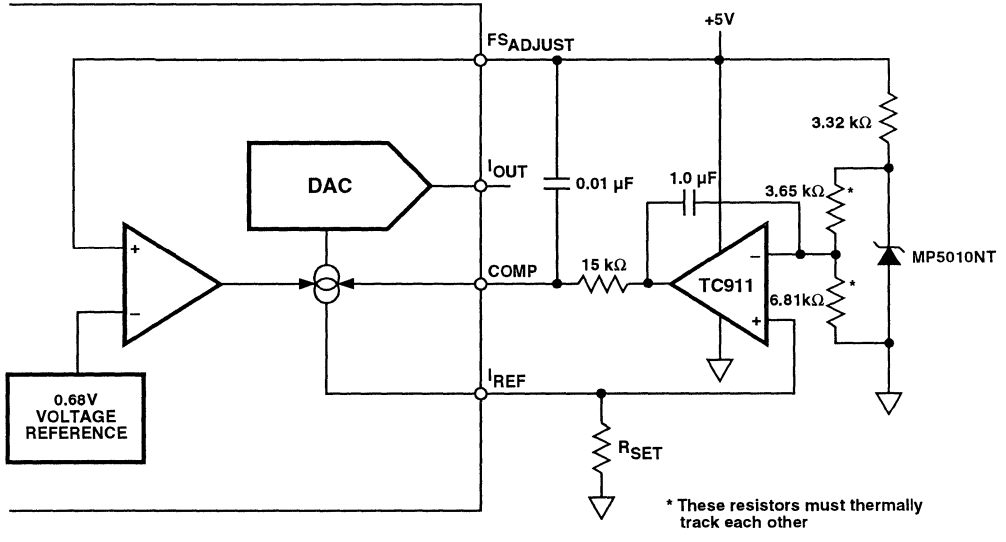

Figure 4a. External Voltage Reference, Single Supply

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USING AN EXTERNAL VOLTAGE REFERENCE

The precision voltage reference contained in the CAT506 is factory trimmed by EEPROM circuitry to guarantee a maximum temperature drift of 10 ppm/ °C. For most applications this is more than adequate, however, there may arise occasions when system requirements dictate that an external reference be used. In such cases the on-chip reference can be disabled and control of I_{REF} can be taken off chip.

When using an external reference, the control amplifier's offset and offset drift can not be ignored. The D/A's output stability is dependent upon not only the reference but the control circuitry around it. For this reason it is recommended that the control amplifier be of the ultra low offset variety, typically < 25µV with a drift of less than 0.1 µV/°C.

Figure 4a shows an example of the CAT506 being used with an external reference in a single supply application. In this circuit, a low drift 1.2 V bandgap reference has been chosen and its voltage divided to 0.8 V by a pair of resistors. This is done to insure that I_{REF} does not exceed its voltage compliance range. The op amp, a low drift chopper stabilized type, replaces the internal control amplifier, which has been de-activated by tying FS_{ADJUST} to the positive supply rail. Control of I_{REF} is effected through the COMP pin which adds an inversion to the control loop (I_{REF} current increases as V_{COMP} -> 0 V).

A simpler circuit can be used to incorporate an external voltag reference if a negative supply voltage is available, as shown i Figure 4b. Here, a precision - 10V reference and R_{SET} com bine with the CAT506's internal reference and amplifier to se and control I_{REF}. V_{REF} becomes the sum of the internal an external references, and R_{SET} is calculated from the equatio

$$R_{SET} = 7.892 * \frac{V_{REF} + 0.68}{I_{OUT}}$$

Since V_{REF} is now the sum of the two references, a large valu voltage is chosen for the external reference so that its charac teristics will be dominant. Any noise or drift exhibited by th internal reference is now reduced in its effect by the ratio of th two reference voltages.

The internal reference is not precisely 0.68 V, as stated in th equation above, because it is factory adjusted to compensate fo variations in the current transfer ratio of I_{OUT} to I_{REF}. T compensate for this, the external voltage reference can b offest by a corresponding amount using the Fine Adjustmen feature. For references without this adjustment feature, R_{SE} can be trimmed instead.

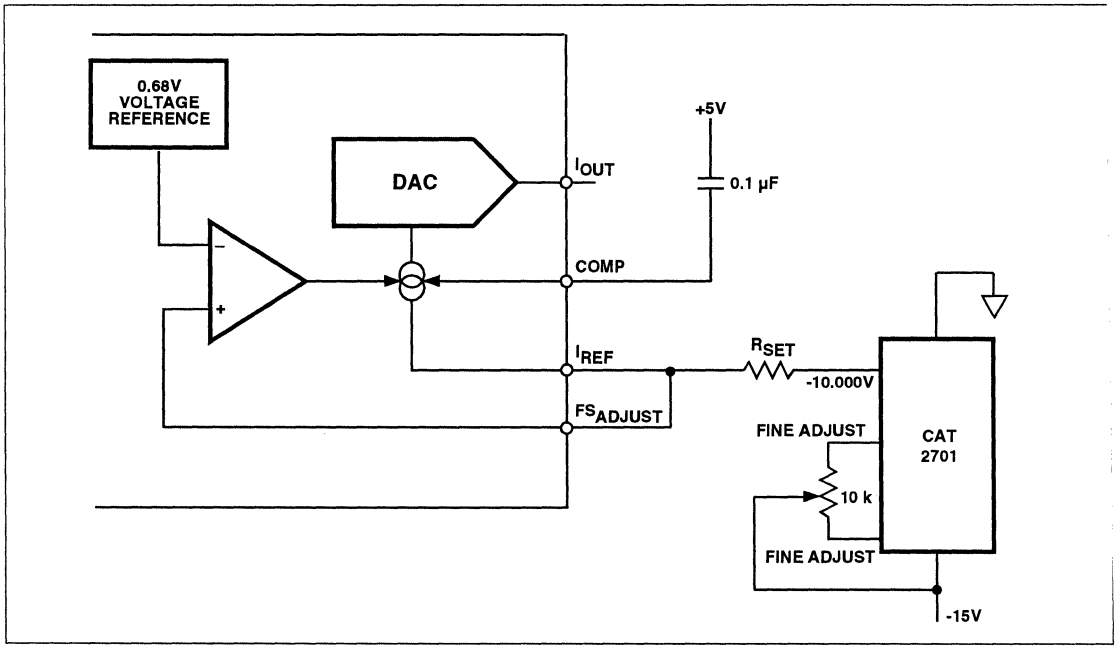
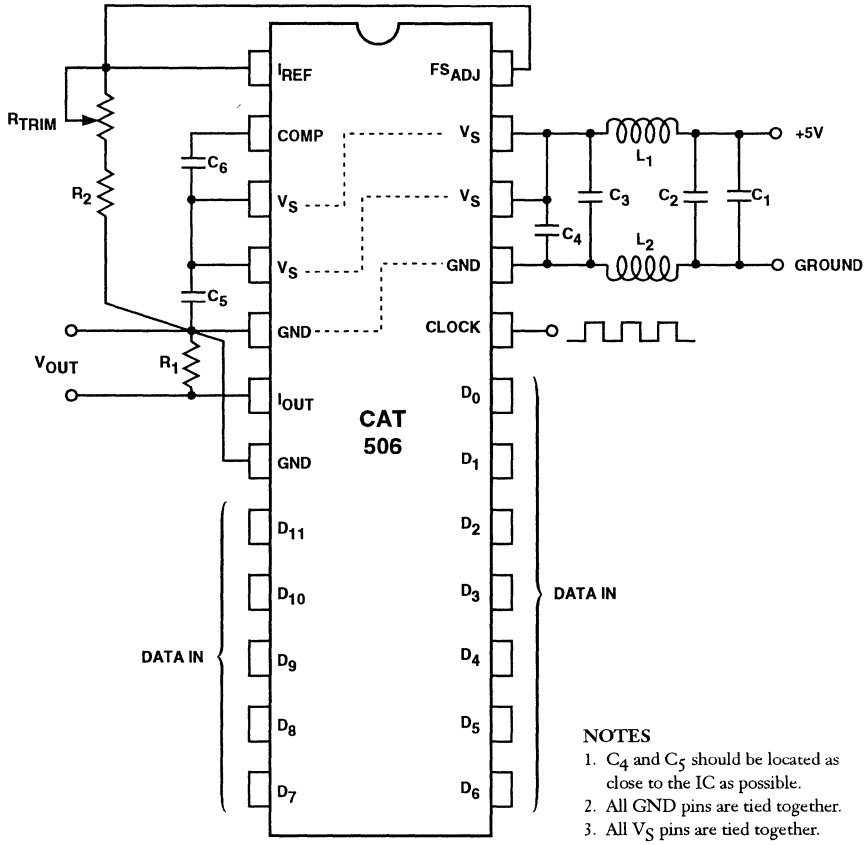


Figure 4b. External Voltage Reference, Dual Supply

SUPPLY DECOUPLING

t is essential to decouple the power and ground supply lines rom the system's main power bus. This prevents glitches and oise spikes generated elsewhere in the system from getting ıto the DAC and showing up on its output.

Decoupling is best achieved through a filter network placed in series with the DAC's power supply lines. The filter is comprised of two inductors, one in each supply line , combined with several bypass capacitors. An example of this is shown in Figure 5.



NOTES
1. C_4 and C_5 should be located as close to the IC as possible.
2. All GND pins are tied together.
3. All V_S pins are tied together.

COMPONENT	DESCRIPTION	SUPPLIER	PART NUMBER
C_6	0.1 µF Ceramic Capacitor	Erie	RPE112Z5U104M50V
C_2	0.01 µF Ceramic Capacitor	Erie	RPE110Z5U103M50V
C_4, C_5	0.01 µF Ceramic Chip Capacitor	Johanson Dielectrics	X7R500S41W103KP
C_1, C_3	22 µF Tantalum Capacitor	Mallory	CSR13G226KM
R_1	24.9Ω 1% Metal Film Resistor	Dale	CMF-55C
L_1, L_2	Ferrite Bead	Fair-Rite	2743001111
R_2	121Ω 1% Metal Film Resistor	Dale	CMF-55C
R_{TRIM}	50Ω Cermet Trim Pot	Bourns	3386W

Figure 5. Typical Application: Unbuffered Voltage Output, 0 - 1V

SUPPLY CURRENT

The maximum supply current drawn by the CAT506 can be calculated from the equation:

I_S = Full Scale Output Current (in mA) +
1.2mA per MHz of operating speed.

P.C. BOARD LAYOUT

Combining high speed with high precision presents a formidable challenge to system designers. Proper RF techniques must be used in board design, device selection, supply bypassing, grounding and measurement if optimum performance is to be realized.

BYPASS CAPACITORS

The most important external components associated with any high-speed design are the power supply bypass capacitors. Selection and placement of these capacitors is critical, and to a large extent, dependent upon the specifics of the system's configuration. The key consideration in selection of bypass capacitors is minimization of series resistance and inductance. Many capacitors will begin to look inductive at 20 MHz and above. Ceramic and metal film capacitors generally feature lower series inductance than the tantalum or electrolytic types.

Bypass capacitors should be installed on the printed circuit board as close to the IC as is physically possible, and with the shortest possible leads in order to minimize series lead inductance. Chip capacitors are optimal in this respect and thus highly recommended.

CRITICAL CONNECTIONS

In using the CAT506 it is of the utmost importance to be sur *all* V_S and GND pins are connected to to their respectiv supplies. Failure to do so will result in improper DAC opera tion, and may result in damage to the IC.

HIGH-SPEED INTERCONNECT

It is essential that care be taken in the signal and power groun circuits to avoid inducing extraneous voltage drops in the signa ground paths. All connections should be short and direct an as physically close to the package as possible. Any conductio path shared by external components should be minimizec When runs exceed an inch or so in length, some type termina tion resistor may be required. This is true of both the analo and digital sections. For digital signals the termination resistc will be dependent upon the logic family used.

Ground planes should be connected at or near the DAC. Car should be taken to insure that the ground plane is uninterrupte over crucial signal paths. On the digital side, this includes th DAC output signal as well as the supply feeders. The use c wide runs or planes in the routing of power lines is als recommended. This serves the dual function of providing a lo series impedance power supply to the part as well as providin some "free" capacitive decoupling to the appropriate groun plane.

For maximum AC performance, the DAC should be mounte directly to the circuit board; sockets should not be used as the increase lead inductance and capacitance. Any additional lea inductance or capacitance at the supply pins can seriousl undermine dynamic performance. Even Teflon or "pin" sock ets can create unwanted results, so soldering directly to th circuit board is highly recommended.

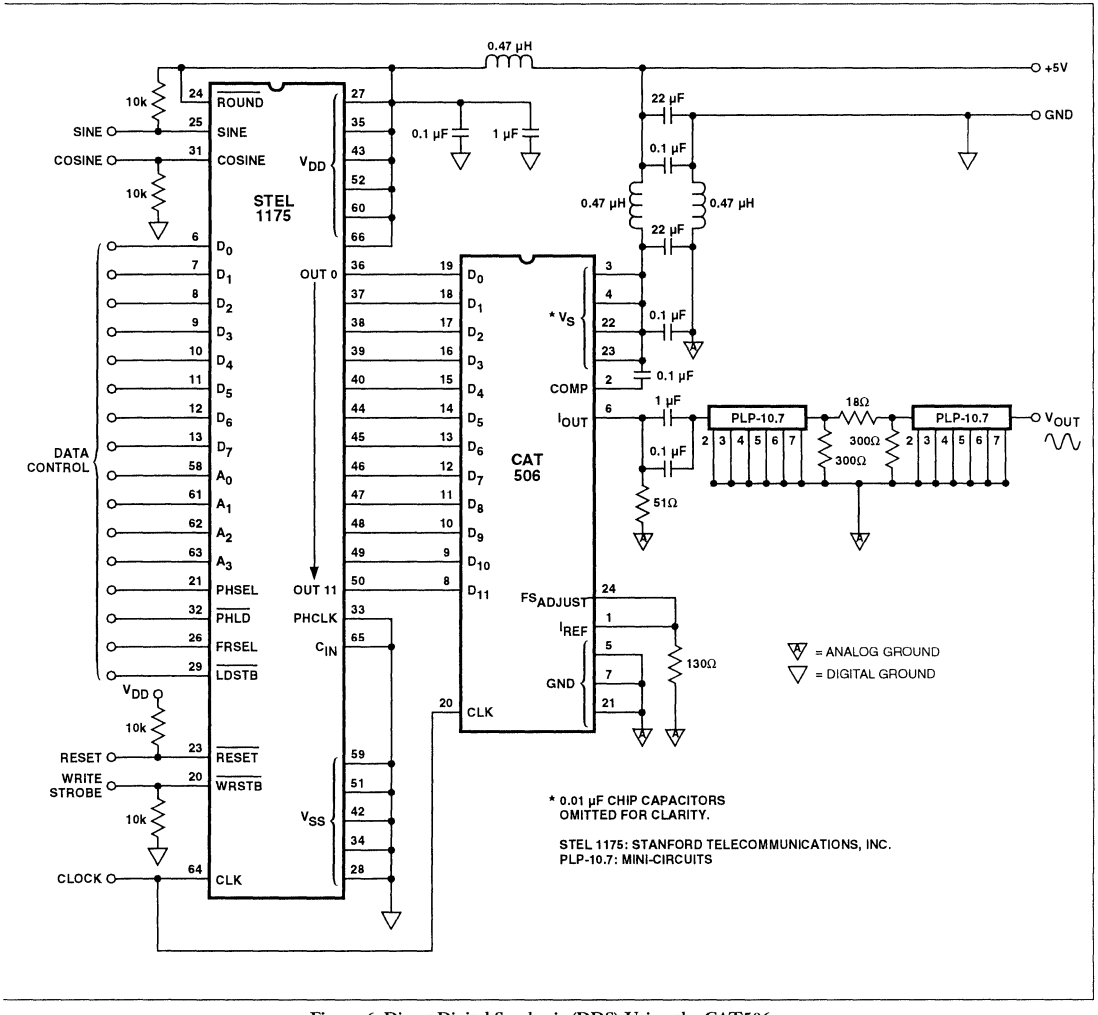


Figure 6. Direct Digital Synthesis (DDS) Using the CAT506

RELIMINARY

:AT507

5V Precision Reference

:ATURES

+5.000V Output ± 0.3%
Output Adjustment Range of > ± 3%
Excellent Temperature Stability < 3 ppm/°C
Output Sinks and Sources > 10 mA

PPLICATIONS

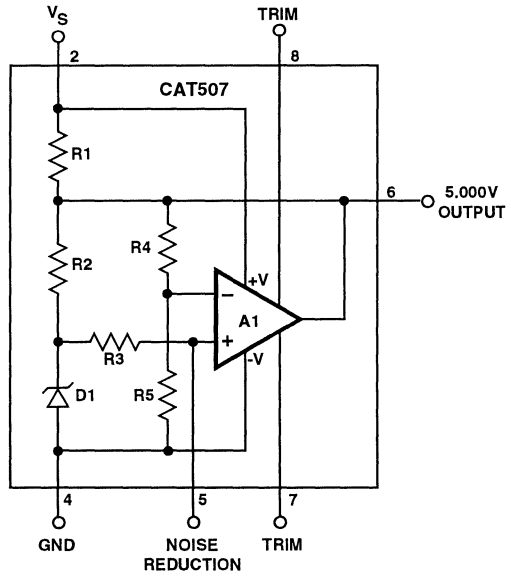
A/D and D/A Converters
V/F Converters
Bridge Excitation
General Purpose System Reference

DESCRIPTION

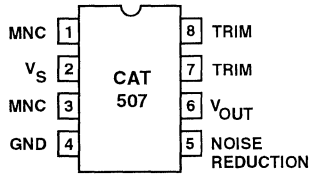
The CAT507 is a precision +5V reference based upon a buried zener diode which eliminates the noise and stability problems associated with surface devices. The output is pretrimmed using Catalyst's on-chip EEPROM driven trim circuitry to ± 0.3% accuracy with a temperature drift of less than 3 ppm/°C. Even greater accuracy may be had through the use of the trim pins provided on the CAT507. Trim allows for an output adjustment of ± 6% without exacting the usual penalty in temperature stability. For noise sensitive applications the CAT507 offers a Noise Reduction pin which further reduces the noise generated by the buried zener. These features combined with the CAT507's ability to source and sink more than 10 mA of current make it an excellent choice as a system reference in a broad range of applications.

The CAT507 is offered in both plastic and ceramic DIPs for operation over the Commercial 0 to +70 °C and the Industrial -40°C to +85°C temperature ranges.

UNCTIONAL DIAGRAM



PIN CONFIGURATION



MNC = MAKE NO CONNECTION
WITH EXTERNAL CIRCUITRY

TD 5172

11

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V_S to GND ..... –0.5V to 18V

Inputs
- Trim ..... –0.5V to V_S +0.5V
- Noise Reduction ..... –0.5V to V_S +0.5V

Output
- V_{OUT} ..... –0.5V to V_S +0.5V
- I_{OUT} 25mA

Output Short Circuit Duration ..... Infinite
Operating Ambient Temperature
- Industrial ('I' Suffix) ..... -40°C to +85°C
- Commercial ('C' Suffix) ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C
Lead Soldering (10 sec max) ..... +300°C

ORDERING INFORMATION

Device	Package	Temp	Outpu
CAT507_P	8 pin Plastic DIP	C	5.000V
CAT507_PI	8 pin Plastic DIP	I	5.000V
CAT507_DI	8 pin CerDIP	I	5.000V

Temperature: C = 0°C to +70°C
I = -40°C to +85°C

Stresses above those listed under Absolute Maximum Ratings m cause permanent damage to the device. Absolute Maximum Ratin are limited values applied individually while other parameters a within specified operating conditions, and functional operation at a of these conditions is NOT implied. Device performance and reliabil may be impaired by exposure to absolute rating conditions for extend periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Method
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(2)	Latch-Up	100		mA	JEDEC Standard 17

NOTES: 1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_S + 1V.

DC ELECTRICAL CHARACTERISTICS: V_S = +15V; T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT}	Output Voltage	I_{LOAD} = 0, "A" Suffix	4.985	5.000	5.015	V
		"B" Suffix	4.975	5.000	5.025	V
ΔV_O	Output Voltage Adjustment Range	R_{TRIM} = 10kΩ	±3	±6	—	%
TCV_O	Output Voltage Temp Coefficient	"A" Suffix	—	—	±3	ppm/°C
		"B" Suffix	—	—	±10	ppm/°C
	Change in V_O Temp Coefficient with Output Adjustment	R_{TRIM} = 10k	—	—	±0.5	ppm/°C
I_O	Output Current	I_{SOURCE}	10	15	—	mA
		I_{SINK}	10	15	—	mA
I_{SC}	Output Short Circuit Current		—	—	20	mA
R_O	Output Resistance		—	—	0.05	Ω
	Line Regulation	V_S= 13 to 16.5 V	—	—	0.005	%/V
	Load Regulation	I_{LOAD}= 0 - 10 mA	—	0.0005	0.001	%/mA
Power Supply						
V_S	Supply Voltage Range		13	15	16.5	V
I_S	Supply Current	I_L = 0	—	4	6	mA

AC ELECTRICAL CHARACTERISTICS: V_S = +15V; T_A = 25°C

e_n	Noise	0.1 to 10 Hz, C_{NR} = 0	—	50	—	µVp-p
		C_{NR} = 10µF	—	15	—	µVp-p
t_{ON}	Turn-On Settling Time		—	5	—	µS

RELIMINARY

CAT508

5V Precision Reference

EATURES

-5.000V Output ± 0.3%
Output Adjustment Range of > ± 3%
Excellent Temperature Stability < 3 ppm/°C
Output Sinks and Sources > 10 mA

PPLICATIONS

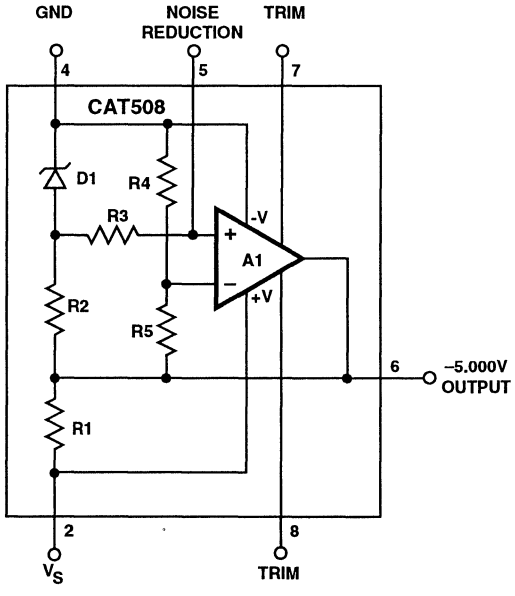
A/D and D/A Converters
V/F Converters
Bridge Excitation
General Purpose System Reference

DESCRIPTION

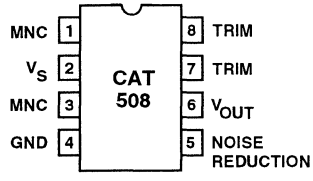
The CAT508 is a precision -5V reference based upon a buried zener diode which eliminates the noise and stability problems associated with surface devices. The output is pretrimmed using Optimium's on-chip EEPROM driven trim circuitry to ±0.3% accuracy with a temperature drift of less than 3 ppm/°C. Even greater accuracy may be had through the use of the trim pins provided on the CAT508. Trim allows for an output adjustment of ± 6% without exacting the usual penalty in temperature stability. For noise sensitive applications the CAT508 offers a Noise Reduction pin which further reduces the noise generated by the buried zener.These features combined with the CAT508's ability to source and sink more than 10 mA of current make it an excellent choice as a system reference in a broad range of applications.

The CAT508 is offered in both plastic and ceramic DIPs for operation over the Commercial 0 to +70°C and the Industrial -40°C to +85°C temperature ranges.

UNCTIONAL DIAGRAM



PIN CONFIGURATION



MNC = MAKE NO CONNECTION WITH EXTERNAL CIRCUITRY

TD 5173

11

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V_S to GND ..... +0.5V to -18V

Inputs
- Trim ..... +0.5V to V_S -0.5V
- Noise Reduction ..... +0.5V to V_S -0.5V

Output
- V_{OUT} ..... +0.5V to V_S -0.5V
- I_{OUT} 25mA

Output Short Circuit Duration ..... Indefinite

Operating Ambient Temperature
- Industrial ('I' Suffix) ..... -40°C to +85°C
- Commercial ('C' Suffix) ..... 0°C to +70°C

Storage Temperature ..... -65°C to +150°C

Lead Soldering (10 sec max) ..... +300°C

ORDERING INFORMATION

Device	Package	Temp	Outpu
CAT508_P	8 pin Plastic DIP	C	-5.000
CAT508_PI	8 pin Plastic DIP	I	-5.000
CAT508_DI	8 pin CerDIP	I	-5.000

Temperature: C = 0°C to +70°C
I = -40°C to + 85°C

Stresses above those listed under Absolute Maximum Ratings m cause permanent damage to the device. Absolute Maximum Ratir are limited values applied individually while other parameters a within specified operating conditions, and functional operation at a of these conditions is NOT implied. Device performance and reliabil may be impaired by exposure to absolute rating conditions for extend periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Method
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(2)	Latch-Up	100		mA	JEDEC Standard 17

NOTES: 1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100mA on address and data pins from -1V to V_S + 1V.

DC ELECTRICAL CHARACTERISTICS: V_S = -15V; T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT}	Output Voltage	I_{LOAD} = 0 "A" Suffix	-4.985	-5.000	-5.015	V
		"B" Suffix	-4.975	-5.000	-5.025	V
ΔV_O	Output Voltage Adjustment Range	R_{TRIM} = 10kΩ	± 3	± 6	—	%
TCV_O	Output Voltage Temp Coefficient	"A" Suffix	—	—	± 3	ppm/°C
		"B" Suffix	—	—	± 10	ppm/°C
	Change in V_O Temp Coefficient with Output Adjustment	R_{TRIM} = 10k	—	—	± 0.5	ppm/°C
I_O	Output Current	I_{SOURCE}	10	15	—	mA
		I_{SINK}	10	15	—	mA
I_{SC}	Output Short Circuit Current		—	—	20	mA
R_O	Output Resistance		—	—	0.05	Ω
	Line Regulation	V_S= 13 to 16.5 V	—	—	0.005	%/V
	Load Regulation	I_{LOAD}= 0 - 10 mA	—	0.0005	0.001	%/mA
Power Supply						
V_S	Supply Voltage Range		-13	-15	-16.5	V
I_S	Supply Current	I_L = 0	—	4	6	mA

AC ELECTRICAL CHARACTERISTICS: V_S = -15V; T_A = 25°C

e_n	Noise	0.1 to 10 Hz, C_{NR} = 0	—	50	—	µVp-p
		C_{NR} = 0µF	—	15	—	µVp-p
t_{ON}	Turn-On Settling Time		—	5	—	µS

'RELIMINARY

CAT2700/2701

:10V Precision References

'EATURES

- High Accuracy: 10.000 Volt ± 2.5 mV
- Low Drift: 3 ppm/°C Drift
- 10 mA Output Drive capability
- Short Circuit Protected Output

.PPLICATIONS

- A/D and D/A Converters
- Instrumentation Reference
- Calibration Standards
- V/F Converters

)ESCRIPTION

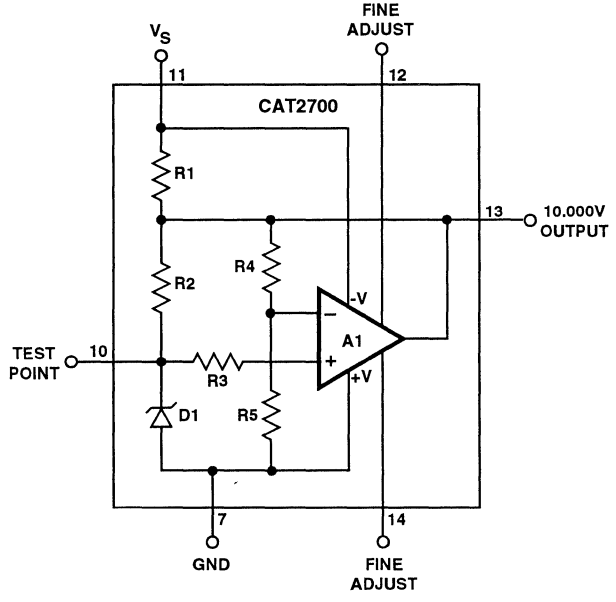
'he CAT2700 & 2701 are precision 10.000 volt references)roviding high accuracy and excellent temperature stability. 'abricated in Catalyst's 2.0µ BiCMOS process, these references)enefit from Catalyst's unique on-chip EEPROM trim circuitry and are factory adjusted for an output voltage error of < ± 2.5 mV and temperature coefficients as low as 3 ppm/°C.

The CAT2700 is a +10V reference is designed for use with high accuracy A/D and D/A converters of 10 and 12 bit resolution. The CAT2701 is a -10V reference designed for similar applications requiring a negative voltage input. For ease of use with Bipolar converters both references source and sink 10 mA of current which makes them an excellent choice for general purpose system references as well.

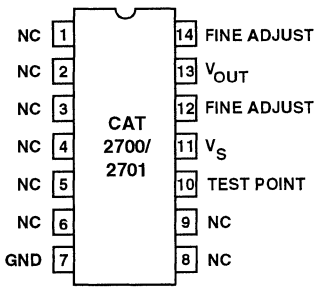
The CAT2700 and the CAT2701 are offered in plastic and ceramic DIPs with operation specified over the Commercial 0 to +70°C and the Industrial -40°C to +85°C temperature ranges.

The CAT2700 and CAT2701 are second source equivalents to Analog Device's AD 2700 and AD 2701.

'UNCTIONAL DIAGRAM



PIN CONFIGURATION



TD 5174

11

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- 2700 V_S to GND ..... –0.5V to +18V
- 2701 V_S to GND ..... +0.5V to -18V

Inputs
- 2700 Fine Adjust to GND ..... –0.5V to V_S +0.5V
- 2700 Test Point to GND ..... –0.5V to V_S +0.5V
- 2701 Fine Adjust to GND ..... +0.5V to V_S -0.5V
- 2701 Test Point to GND ..... +0.5V to V_S -0.5V

Outputs
- 2700 V_{OUT} ..... –0.5V to V_S +0.5V
- 2701 V_{OUT} ..... +0.5V to V_S -0.5V
- 2700 I_{OUT} to GND ..... ±25mA
- 2701 I_{OUT} to GND ..... ±25mA

Output Short Circuit Duration ..... Infinite

Operating Ambient Temperature
- Industrial ('I' Suffix) ..... -40°C to +85°C
- Commercial ('C' Suffix) ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Lead Soldering (10 sec max) ..... +300°C

ORDERING INFORMATION

Device	Package	Temp	Output
CAT2700_P	14 pin Plastic DIP	C	10.000V
CAT2700_PI	14 pin Plastic DIP	I	10.000V
CAT2700_DI	14 pin CerDIP	I	10.000V
CAT2701_P	14 pin Plastic DIP	C	-10.000V
CAT2701_PI	14 pin Plastic DIP	I	-10.000V
CAT2701_DI	14 pin CerDIP	I	-10.000V

Temperature: C = 0°C to +70°C
I = –40°C to +85°C

Stresses above those listed under Absolute Maximum Ratings ma cause permanent damage to the device. Absolute Maximum Ratin are limited values applied individually while other parameters ar within specified operating conditions, and functional operation at an of these conditions is NOT implied. Device performance and reliabilit may be impaired by exposure to absolute rating conditions for extende periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Method
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(2)	Latch-Up	100		mA	JEDEC Standard 17

NOTES: 1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_S + 1V.

DC ELECTRICAL CHARACTERISTICS: V_S = ±15V; T_A = -40°C to +85°C; R_L= 2kΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT}	Output Voltage	CAT2700	—	10.000	—	V
		CAT2701	—	-10.000	—	V
	Output Voltage Error	"A" Suffix	± .0025	—	± .0025	V
		"B" Suffix	± .005	—	± .005	V
ΔV_O	Output Voltage Adjustment Range	R_{ADJ} = 10kΩ	± 20	—	—	mV
TCV_O	Output Voltage Temp Coefficient	"A" Suffix	—	—	± 3	ppm/°C
		"B" Suffix	—	—	± 10	ppm/°C
	Change in V_O Temp Coefficient with Output Adjustment	R_{ADJ} = 10kΩ	—	± 4	—	µV/°C per mV of Adjustment
I_O	Output Current		—	—	± 10	mA
R_O	Output Resistance		—	—	0.05	Ω
	Line Regulation		—	—	300	µV/V
	Load Regulation	V_S= 13 to 16.5 V	—	—	50	µV/mA
	Long Term Stability		—	100	—	ppm/1000 hrs
Power Supply						
V_S	Supply Voltage Range	CAT2700	13	15	16.5	V
		CAT2701	-13	-15	-16.5	V
I_S	Supply Current		—	± 4	± 14	mA

AC ELECTRICAL CHARACTERISTICS: V_S = ±15V; T_A = -40°C to +85°C; R_L= 2kΩ

e_n	Noise	0.1 to 10 Hz	—	50	—	µVp-p

CATALYST SEMICONDUCTOR

Product Information 1

2-Wire Bus Serial E^2PROMs 2

3-Wire Bus Serial E^2PROMs 3

SPI Bus Serial E^2PROMs 4

4-Wire Bus Serial E^2PROMs 5

Secure Access Serial E^2PROMs 6

Parallel E^2PROMs 7

Flash Memories 8

EPROMs 9

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Quality and Reliability 13

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Using Catalyst's Serial E²PROMs in Shared Input/Output Configuration

Jim Bajwa

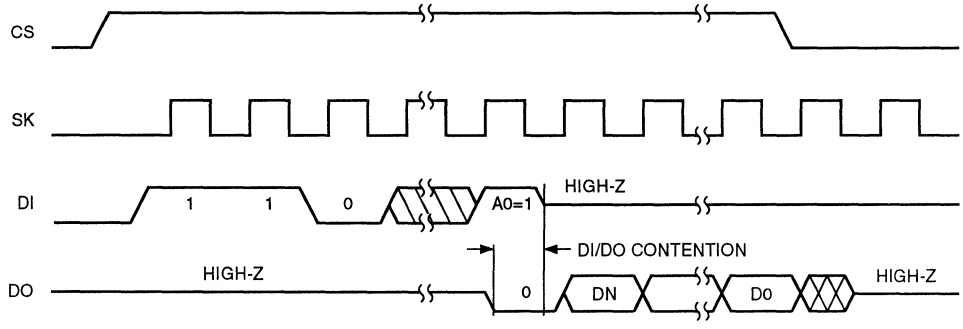
Catalyst Semiconductor's family of serial E²PROMs utilizes 4 signals for the communication interface; Chip Select (CS) for device selection, Serial Clock (SK or CLK) for synchronizing serial data to and from the device, Data Input (DI) to input serial data to the device and Data Output (DO) to output serial data from the device. This interface can be reduced to 3 signals by sharing DI and DO as a common input/output signal. However, the following precautions should be taken to prevent problems due to DI/DO contention:

READ instruction in shared DI/DO configuration:
(applies to 93C46, 59C11, 35C102, 35C202, 35C104, 35C108 and 35C116)

DO remains in high impedance while most of the READ instruction (i.e. start bit, opcode and address) is being input and offers no contention to the DI driver on a shared DI/DO signal (Figure 1a). However, typically 50ns after the rising edge of the serial clock shifts in the least significant bit of the address stream (A0), DO outputs the dummy '0' bit to flag the beginning of the output data stream. If A0 is a '1' and the DI driver has not been disabled by the time the '0' dummy bit becomes valid, a low impedance path between the system power supply and ground is created through the DI driver pullup and DO pulldown device (Figure 1b).

Unless this condition causes excessive noise on the system power supply (which may in turn cause noisy or

Figure 1a. DI/DO Contention Timing During Read Cycle



5192 FHD F01

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spurious signals to the device), the READ instruction will continue and complete normally since A0 is already shifted into the device.

To minimize potential problems during this low impedance condition, a current limiting resistor should be placed between the DI driver and the DO pin when using the shared DI/DO signal (Figure 2).

Alternatively, an open drain (or open collector) DI driver with pullup resistor could be used (Figure 2).

In either case, the clocking rate should be slow enough to ensure that the resistor can charge or discharge the shared DI/DO bus capacitance before the appropriate clock edge. For example, if the resistor used is 10KΩ, and the bus capacitance is 100pF, then a safe clock rate is calculated to be:

Clock Period (T) = 2 x 3RC
= 2 x 3 x 10kΩ x 100pF
= 6μsec

Frequency (f) = 1 / T
= 167KHz

2) Programming Instructions in shared DI/D configuration:
(93C46, 35C102, 35C104, 35C108 and 35C116 on

All devices in the Catalyst serial E²PROM family featu self-timed programming cycles. A programming stat signal indicates whether the self-timed programmi cycle is still in progress or has been completed. A status signal indicates that the device is still progra ming, while a '1' status signal indicates that the progra ming cycle has been completed and the device is rea to receive the next instruction. This feature will allow user to minimize the programming time (t_{EW}).

The 59C11 and 35C202 devices have a separate read busy signal pin (RDY/$\overline{BUSY}$) to output the programmi status signal. The DO signal stays in high impedan throughout the programming cycle and therefore will r

Figure 1b. Current Path

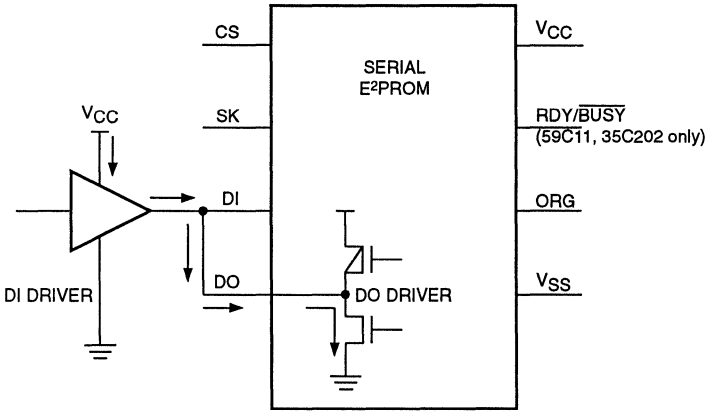
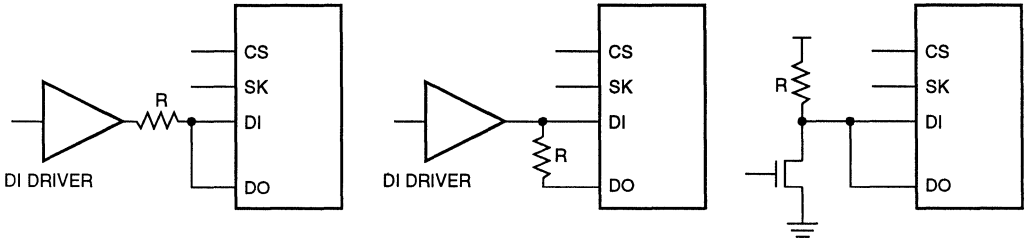


Figure 2. Possible Configurations to Minimize Problems Due to READ Contention



erfere with the DI signal in a shared DI/DO configura-
n.

the 93C46, 35C102, 35C104, 35C108, and 35C116
rial E²PROMs, the programming status signal can be
ad on the DO pin by bringing CS high after initiating a
ogramming cycle. In a 4-signal interface, after a pro-
amming cycle is complete, the status signal is reset to
gh impedance by the start bit of the next instruction
igure 3).

a shared DI/DO configuration, the '1' status signal on
O can be clocked into the device as a start bit and reset
e status signal before it can be read. This can interfere
th the DI signal for the next instruction cycle. The following steps are recommended to avoid these conditions for a 3-signal interface (Figure 4):

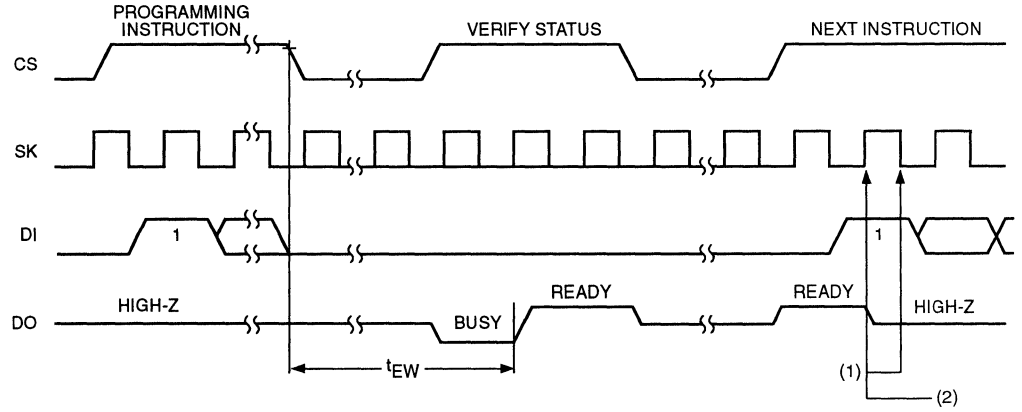
1) The clock (SK) should be stopped after shifting in the programming instruction. This prevents the '1' ready status from resetting the status signal before it can be read.

2) After reading the '1' ready status, at least one clock pulse should be input to the device while the DI/DO signal is '1' in order to reset the status signal.

3) CS should then be brought low to reset the instruction logic.

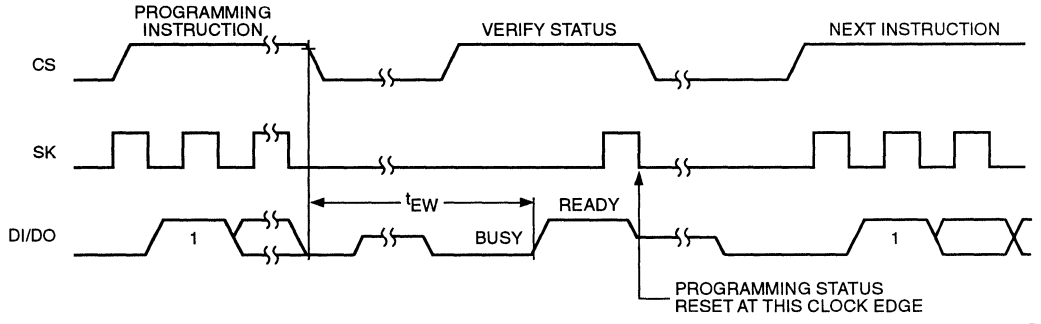
The next instruction can now be executed without any contention from the DO signal.

gure 3. Programming Instruction and Status Reset with 4-Signal Interface



5192 FHD F04

igure 4. Programming Instruction and Status Reset with 3-Signal Interface



5192 FHD F05

lotes:
1) Programming status reset on falling clock edge (93C46).
2) Programming status reset on rising clock edge (35C102, 35C104, 35C108, 35C116).

12

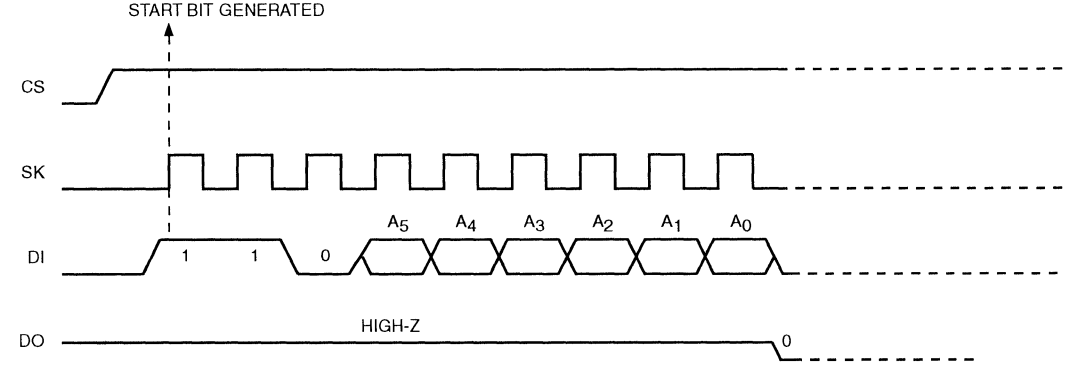
The CAT93C46 Start-Bit Timing

an Apple

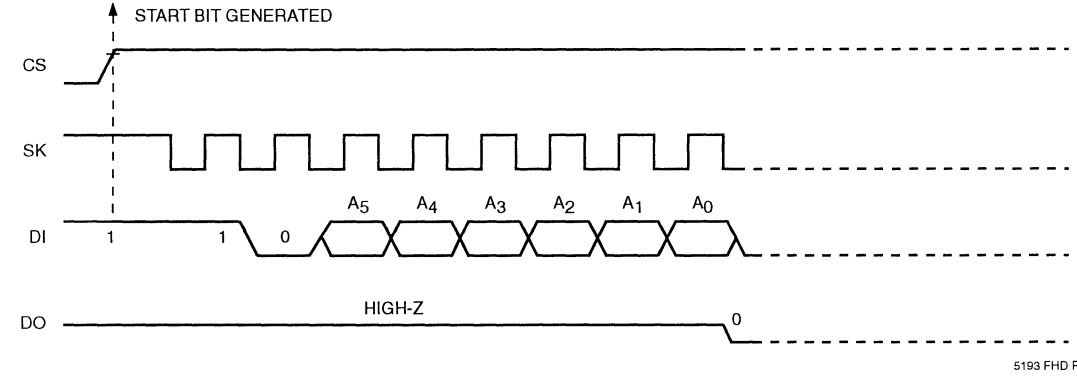
atalyst's CAT93C46 Serial 1k bit E²PROM can be sed in two different start-bit modes of operation. All atalyst serial E²PROMs require a start bit before any nstructions will be accepted. This is accomplished imply by clocking a '1' (high level on DI pin) into the evice while CS is high. Once this is done the device equires that all opcodes, address and data be clocked n on the positive edge of the serial clock (Figure 1).

he CAT93C46 serial E²PROM, however, has been esigned to accept either an edge-triggered start bit (as escribed above) or a level-triggered start bit. A level-iggered start bit is a start condition that is recognized by he device when both SK and DI are high level when CS ansitions from low to high (Figure 2). The advantage with this start bit mode is that the device needs only 8 clock pulses for the remaining opcode and address bits (in x16 configuration), making it compatible with many microprocessors that transfer data in 8 bit clock bursts such as the serial peripheral interface (SPI) bus. The SPI bus does data transfers using a sequence of 8 clock cycles only. Without this level-triggered start condition, another 8 clocks would be necessary to clock in only 1 start bit. The CAT93C46 Read operation requires 9 clock bits consisting of 1 start bit, a 2 bit opcode and 6 bits of address in x16 mode. Once the device accepts this level-triggered start bit all other opcode, address and data bits are clocked in on the positive edge of the serial clock. This mode allows the user to save valuable microprocessor time by optimizing clock cycle routines.

igure 1. Read Timing: Edge Triggered Start Bit



igure 2. Read Timing: Level Triggered Start Bit



12

^{2}C Interface to 8051 Microcontroller

ian Apple

ıtroduction to I^{2}C

he I^{2}C (Inter-Integrated Circuit) bus is a 2-wire serial us which provides a small networking system for cir-uits sharing a common bus. The devices on the bus can ary from microcontrollers to LCD drivers to E^{2}PROMs.

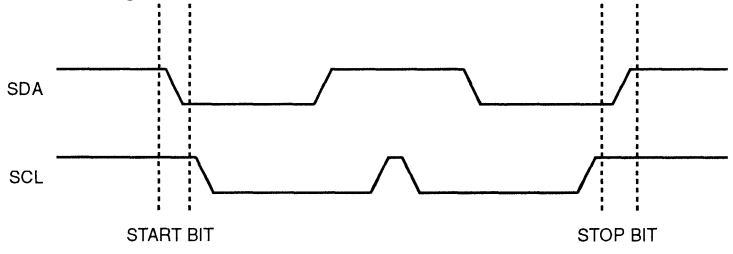
wo bi-directional lines, a serial data (SDA) and a serial lock (SCL) line, transmit data between the devices onnected to the bus. Each device has a unique ddress to differentiate it from the other devices on the us, and each is configured either as a master or a slave hen performing data transfers (see Table 1). A master s the device which initiates a data transfer and gener-tes the clock signals necessary for the transfer. Any evice that is addressed is considered a slave. The I^{2}C bus is a multi-master bus, which means that more than one device that is capable of controlling the bus can be connected to it.

Each transmission on the bus begins with the Master sending a Start condition and ends with a Stop condition (see Figure 1). The Master then sends the address of the particular slave device it is requesting. The first four bits of this slave address are fixed as 1010. The next three bits specify a combination of the device address bit(s) and which 2K array of the memory is being addressed (see Figure 2). The last bit of the slave address specifies whether a read or write operation is to be performed. When this bit is a "1", a read operation is performed, and when it is a "0", a write operation is performed.

able 1. Definition of I^{2}C Bus Terminology

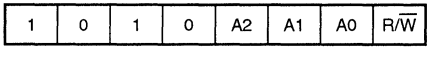
Term	Description
Transmitter	The device which sends the data to the bus.
Receiver	The device which receives the data from the bus.
Master	The device which initiates a transfer, generates clock signals and terminates a transfer.
Slave	The device addressed by a master.
Multi-Master	More than one master can attempt to control the bus at the same time without corrupting the message.
Arbitration	Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so, and the message is not corrupted.
Synchronization	Procedure to synchronize the clock signals of two or more devices.

igure 1. START/STOP Timing



5194 FHD F01

Figure 2. Slave Address Bits



5194 FHD F07

TD 5194

After the Master sends a Start condition, the slave (E²PROM) monitors the bus and responds with an acknowledge when its address matches the transmitted slave address (see Figure 3). The device then performs a read or write operation depending on the state of the R/$\overline{W}$ bit.

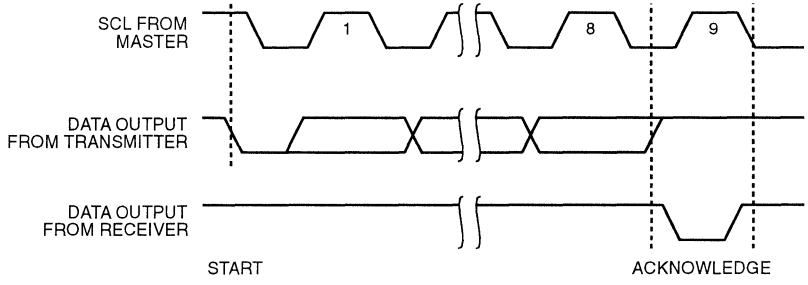
CAT24CXX Interface to 8051 Microcontroller

Catalyst's I²C family of devices interfaces directly with industry standard microcontrollers such as the Intel MCS-51 family. This family includes 8031/8051 and 8032/8052 (ROMless/ROM) family types.

Catalyst I²C E²PROMs are 2-wire interface, nonvolatile memories ranging from 2K bits (CAT24C02) to 16K bits (CAT24C16) in density. They adhere to the I²C protocol which uses 2 lines, a data (SDA) and serial clock (SCL line for all transmissions, as described above.

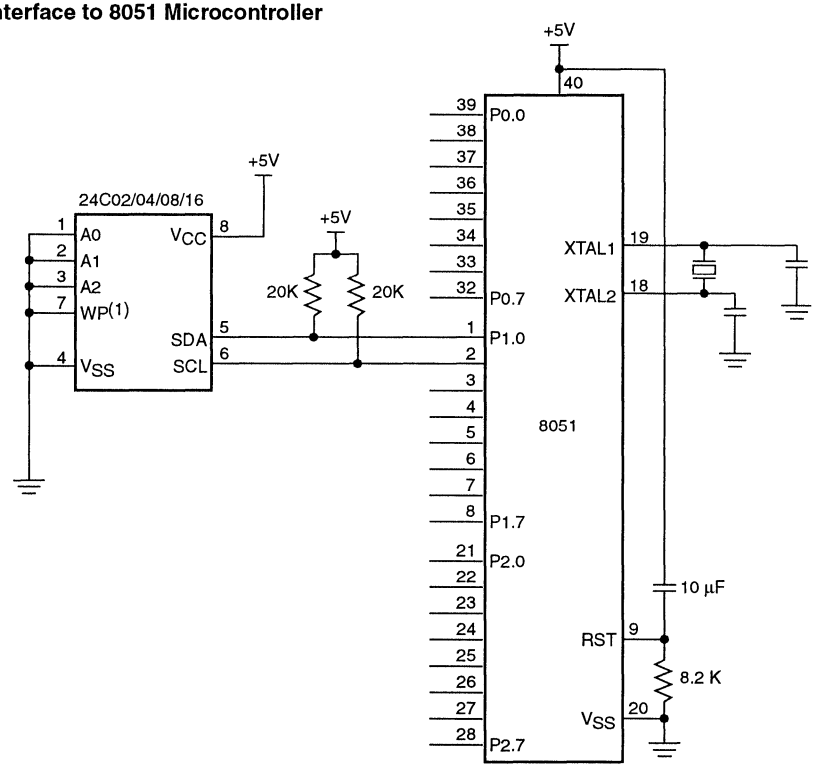
The CAT24C02 E²PROM has an 8 byte page writ buffer and a write protect pin for inadvertent write protec tion. The CAT24C04, CAT24C08 and CAT24C16 de vices have 16 byte page write buffers. Up to eigh CAT24C02 devices, four CAT24C04 devices, tw CAT24C08 devices and one CAT24C16 device may b connected to an I²C bus and addressed independentl Unique addressing is accomplished through hard-wirin address pins A0, A1 and A2 on each device. An exampl program follows that demonstrates simple byte writ and byte read routines as well as page mode an sequential read routines using an 8051 microcontrolle Figure 4 shows a simple hardware interface.

Figure 3. ACKNOWLEDGE Timing



5194 FHD F0

igure 4. I²C Interface to 8051 Microcontroller



lote:
1) WP Pin for CAT24C02; Test Pin for CAT24C04, CAT24C08, CAT24C16

12

```
<< ASM51 >> CROSS ASSEMBLER VER.2.5M    ASSEMBLE LIST DATE:          PAGE:   1

 LOC. OBJECT           LINE    STATEMENT                        I2C_8051.ASM

                        1    ;*********************************************************************
                        2    ; THE FOLLOWING CODE SHOWS AN INTERFACE BETWEEN AN 8051 MICROCONTROLLE
                        3    ; AND CATALYST'S I2C FAMILY OF EEPROMS.
                        4    ;
                        5    ; IT DEMONSTRATES A BYTE WRITE/BYTE READ ROUTINE AND A PAGE MODE
                        6    ; WRITE/SEQUENTIAL READ ROUTINE.  IT USES TWO LINES FROM PORT 1
                        7    ; (P1.0 AND P1.1) OF THE 8051 TO COMMUNICATE WITH THE CAT24CXX.
                        8    ;
                        9    ; THIS PROGRAM WILL WORK WITH THE CAT24C02/04/08/16 DEVICES. NOTE:
                       10    ; THE 24C02 HAS AN 8 BYTE PAGE BUFFER ALL OTHERS ARE 16 BYTES.
                       11    ;*********************************************************************
                       12
   0090                13    SCL          BIT    P1.0                ;SCL BIT IS PORT 1, BIT 0
   0091                14    SDA          BIT    P1.1                ;SDA BIT IS PORT 1, BIT 1
   0005                15    SLV_ADDR     EQU    0101B               ;FIXED SLAVE ADDRESS BITS
   REG                 16    DATAOUT      EQU    R5                  ;DATA READ FROM DEVICE
   0085                17    ACK_READ     EQU    10000101B           ;READ FOR ACK POLLING
                       18
—                      19                 DSEG
0030                   20                 ORG    0030H
                       21
0030                   22    PAGE_DATA:   DS     1
0031                   23    BLK_ADDR:    DS     1
0032                   24    BYTE_ADDR:   DS     1
0033                   25    BYTE_DATA:   DS     1
                       26
0040                   27                 ORG    40H
0040                   28    STACK:       DS     31
                       29
—                      30                 CSEG
0040                   31                 ORG    0040H
0040 02 01 00          32                 LJMP   BEGIN
                       33
0100                   34                 ORG    0100H
0100 75 81 40          35    BEGIN:       MOV    SP,#STACK           ;INITIALIZE STACK POINTER
                       36
0103 75 31 00          37                 MOV    BLK_ADDR,#000B      ;INITIALIZE 2K BLOCK
0106 75 33 55          38                 MOV    BYTE_DATA,#55H      ;BYTE DATA
0109 75 32 00          39                 MOV    BYTE_ADDR,#00H      ;BYTE ADDRESS
010C 75 30 AA          40                 MOV    PAGE_DATA,#0AAH     ;PAGE DATA
                       41
010F 31 45 [0145]      42                 ACALL  PAGE_WR             ;CALL PAGE WRITE ROUTINE
0111 51 1D [021D]      43                 ACALL  SEQ_RD              ;CALL SEQ. READ ROUTINE
0113 31 1A [011A]      44                 ACALL  BYTE_WR             ;CALL BYTE WRITE ROUTINE
0115 31 D6 [01D6]      45                 ACALL  SELECT_RD           ;CALL BYTE READ ROUTINE
0117 02 01 17          46    DONE:        LJMP   DONE                ;LOOP UNTIL RESET OCCURS
                       47
                       48    ;*****************************************
                       49
                       50    ;************** BYTE WRITE *****************
                       51
011A 31 95 [0195]      52    BYTE_WR:     ACALL  START_BIT           ;SEND START BIT
011C 74 05             53                 MOV    A,#SLV_ADDR         ;FIRST 4 SLAVE ADDRESS
011E 7F 04             54                 MOV    R7,#4H              ;BITS
0120 31 89 [0189]      55                 ACALL  SHFTO
0122 E5 31             56                 MOV    A,BLK_ADDR          ;2K BLOCK ADDRESS
0124 7F 03             57                 MOV    R7,#3H
0126 31 89 [0189]      58                 ACALL  SHFTO
```

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< ASM51 >> CROSS ASSEMBLER VER.2.5M    ASSEMBLE LIST DATE:          PAGE:   2

LOC. OBJECT           LINE    STATEMENT                        I2C_8051.ASM

0128 74 00             59              MOV     A,#00H                  ;R/W BIT SET TO 0 FOR
012A 7F 01             60              MOV     R7,#1H                  ;WRITE
012C 31 89 [0189]      61              ACALL   SHFTO
012E 31 AA [01AA]      62              ACALL   SLAVE_ACK
                       63
0130 E5 32             64              MOV     A,BYTE_ADDR             ;BYTE ADDRESS
0132 7F 08             65              MOV     R7,#8H
0134 31 89 [0189]      66              ACALL   SHFTO
0136 31 AA [01AA]      67              ACALL   SLAVE_ACK
0138 E5 33             68              MOV     A,BYTE_DATA             ;BYTE DATA
013A 7F 08             69              MOV     R7,#8H
013C 31 89 [0189]      70              ACALL   SHFTO
013E 31 AA [01AA]      71              ACALL   SLAVE_ACK
0140 31 A1 [01A1]      72              ACALL   STOP_BIT                ;STOP BIT
0142 31 74 [0174]      73              ACALL   ACK_POL                 ;CALL ACK POLLING, WAIT
0144 22                74              RET                             ;FOR END OF WRITE CYCLE
                       75    ;****************************************
                       76
                       77    ;************** PAGE WRITE *****************
                       78
0145 31 95 [0195]      79    PAGE_WR:  ACALL   START_BIT               ;SEND START BIT
0147 74 05             80              MOV     A,#SLV_ADDR             ;FIRST 4 SLAVE ADDRESS
0149 7F 04             81              MOV     R7,#4H                  ;BITS
014B 31 89 [0189]      82              ACALL   SHFTO
014D E5 31             83              MOV     A,BLK_ADDR              ;2K BLOCK ADDRESS
014F 7F 03             84              MOV     R7,#3H
0151 31 89 [0189]      85              ACALL   SHFTO
0153 74 00             86              MOV     A,#00H                  ;R/W BIT SET TO 0 FOR
0155 7F 01             87              MOV     R7,#1H                  ;WRITE
0157 31 89 [0189]      88              ACALL   SHFTO
0159 31 AA [01AA]      89              ACALL   SLAVE_ACK
015B E5 32             90              MOV     A,BYTE_ADDR             ;BYTE ADDRESS
015D 7F 08             91              MOV     R7,#8H
015F 31 89 [0189]      92              ACALL   SHFTO
0161 31 AA [01AA]      93              ACALL   SLAVE_ACK
0163 7C 0F             94              MOV     R4,#0FH
                       95    NEXT_DATA:                              ;WRITE 16 BYTES TO
0165 E5 30             96              MOV     A,PAGE_DATA             ;EEPROM
0167 7F 08             97              MOV     R7,#8H
0169 31 89 [0189]      98              ACALL   SHFTO
016B 31 AA [01AA]      99              ACALL   SLAVE_ACK
016D DC F6 [0165]     100              DJNZ    R4,NEXT_DATA
016F 31 A1 [01A1]     101              ACALL   STOP_BIT
0171 31 74 [0174]     102              ACALL   ACK_POL                 ;CALL ACK POLLING,WAIT
0173 22               103              RET                             ;FOR END OF WRITE CYCLE
                      104    ;****************************************
                      105
                      106    ;************** ACK_POL ********************
                      107
0174 7B 40            108    ACK_POL:  MOV     R3,#40H                 ;# OF TIMES TO POLL
0176 DB 02 [017A]     109    ACK_LOOP: DJNZ    R3,DONE_YET             ;DEVICE
0178 80 0C [0186]     110              SJMP    DN_ACKPOL
017A 31 95 [0195]     111    DONE_YET: ACALL   START_BIT               ;SEND START BIT
017C 74 85            112              MOV     A,#ACK_READ             ;SEND READ
017E 7F 08            113              MOV     R7,#8H
0180 31 89 [0189]     114              ACALL   SHFTO
0182 31 AA [01AA]     115              ACALL   SLAVE_ACK               ;SEND ACKNOWLEDGE
0184 40 F0 [0176]     116              JC      ACK_LOOP                ;LOOP IF NO ACK RCVD,
```

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<< ASM51 >> CROSS ASSEMBLER VER.2.5M    ASSEMBLE LIST DATE:          PAGE:   3

 LOC. OBJECT           LINE    STATEMENT                        I2C_8051.ASM

                       117                                                  ;JUMP IF ACK RCVD
 0186 31 A1 [01A1]     118    DN_ACKPOL:  ACALL  STOP_BIT                   ;SEND STOP BEFORE RETURN
 0188 22               119                RET
                       120    ;*****************************************
                       121
                       122    ;************** SHFTO **********************
                       123
 0189 C2 90            124    SHFTO:      CLR    SCL
 018B C2 90            125    NXTSHF:     CLR    SCL
 018D 13               126                RRC    A                          ;ROTATE DATA INTO CARRY
 018E 92 91            127                MOV    SDA,C                      ;SEND CARRY TO SDA
 0190 D2 90            128                SETB   SCL
 0192 DF F7 [018B]     129                DJNZ   R7,NXTSHF
 0194 22               130                RET
                       131    ;*****************************************
                       132
                       133    ;************** START BIT ******************
                       134
 0195 D2 90            135    START_BIT:  SETB   SCL                        ;START BIT
 0197 00               136                NOP
 0198 D2 91            137                SETB   SDA
 019A 00               138                NOP
 019B C2 91            139                CLR    SDA
 019D 00               140                NOP
 019E C2 90            141                CLR    SCL
 01A0 22               142                RET
                       143    ;*****************************************
                       144
                       145    ;************** STOP BIT ******************
                       146
 01A1 C2 91            147    STOP_BIT:   CLR    SDA                        ;STOP BIT
 01A3 00               148                NOP
 01A4 D2 90            149                SETB   SCL
 01A6 00               150                NOP
 01A7 D2 91            151                SETB   SDA
 01A9 22               152                RET
                       153    ;*****************************************
                       154
                       155    ;************** SLAVE ACKNOWLEDGE **********
                       156
 01AA 00               157    SLAVE_ACK:  NOP
 01AB 00               158                NOP
 01AC C2 90            159                CLR    SCL                        ;SLAVE ACKNOWLEDGE BIT
 01AE 00               160                NOP
 01AF D2 91            161                SETB   SDA
 01B1 00               162                NOP
 01B2 00               163                NOP
 01B3 D2 90            164                SETB   SCL
 01B5 00               165                NOP
 01B6 00               166                NOP
 01B7 00               167                NOP
 01B8 A2 91            168                MOV    C,SDA                      ;READ STATE OF SDA,
 01BA C2 90            169                CLR    SCL                        ;SAVE TO CARRY
 01BC 22               170                RET
```

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: ASM51 >> CROSS ASSEMBLER VER.2.5M    ASSEMBLE LIST DATE:          PAGE:   4

,OC. OBJECT            LINE    STATEMENT                        I2C_8051.ASM

                       171     ;*****************************************
                       172
                       173     ;************** MASTER ACKNOWLEDGE *********
                       174
                       175     MSTR_ACK:
)1BD C2 90             176                 CLR     SCL                     ;MASTER ACKNOWLEDGE BIT
)1BF 00                177                 NOP
)1C0 C2 91             178                 CLR     SDA
)1C2 00                179                 NOP
)1C3 00                180                 NOP
)1C4 D2 90             181                 SETB    SCL
)1C6 00                182                 NOP
)1C7 C2 90             183                 CLR     SCL
)1C9 00                184                 NOP
)1CA D2 91             185                 SETB    SDA
)1CC 22                186                 RET
                       187     ;*****************************************
                       188
                       189     ;************** NO ACKNOWLEDGE *************
                       190
)1CD D2 91             191     NO_ACK:     SETB    SDA                     ;NO ACKNOWLEDGE
)1CF 00                192                 NOP
)1D0 D2 90             193                 SETB    SCL
)1D2 00                194                 NOP
)1D3 C2 90             195                 CLR     SCL
)1D5 22                196                 RET
                       197     ;*****************************************
                       198
                       199     ;************** SELECTIVE READ *************
                       200
                       201     SELECT_RD:
01D6 31 95 [0195]      202                 ACALL   START_BIT               ;START BIT
                       203
01D8 74 05             204                 MOV     A,#SLV_ADDR             ;DUMMY WRITE TO FIRST
01DA 7F 04             205                 MOV     R7,#4H                  ;2K BLOCK
01DC 31 89 [0189]      206                 ACALL   SHFTO
01DE E5 31             207                 MOV     A,BLK_ADDR              ;2K BLOCK ADDRESS
01E0 7F 03             208                 MOV     R7,#3H
01E2 31 89 [0189]      209                 ACALL   SHFTO
01E4 74 00             210                 MOV     A,#00H                  ;R/W BIT SET TO 0
01E6 7F 01             211                 MOV     R7,#1H                  ;FOR WRITE
01E8 31 89 [0189]      212                 ACALL   SHFTO
01EA 31 AA [01AA]      213                 ACALL   SLAVE_ACK               ;SEND ACKNOWLEDG
                       214
01EC E5 32             215                 MOV     A,BYTE_ADDR             ;ADDRESS TO READ
01EE 7F 08             216                 MOV     R7,#8H
01F0 31 89 [0189]      217                 ACALL   SHFTO
01F2 31 AA [01AA]      218                 ACALL   SLAVE_ACK
                       219
01F4 31 95 [0195]      220                 ACALL   START_BIT               ;NEW START BIT
                       221
01F6 74 05             222                 MOV     A,#SLV_ADDR
01F8 7F 04             223                 MOV     R7,#4H
<< ASM51 >> CROSS ASSEMBLER VER.2.5M    ASSEMBLE LIST DATE:          PAGE:   5
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LOC. OBJECT           LINE    STATEMENT                    I2C_8051.ASM

01FA 31 89 [0189]      224              ACALL  SHFTO
01FC E5 31             225              MOV    A,BLK_ADDR            ;2K BLOCK TO READ
01FE 7F 03             226              MOV    R7,#3H
0200 31 89 [0189]      227              ACALL  SHFTO
0202 74 01             228              MOV    A,#1H                 ;R/W BIT SET TO 1
0204 7F 01             229              MOV    R7,#1H                ;FOR READ
0206 31 89 [0189]      230              ACALL  SHFTO
0208 31 AA [01AA]      231              ACALL  SLAVE_ACK
                       232
020A 7F 08             233              MOV    R7,#8H
020C D2 90             234    CLOCK8:   SETB   SCL                   ;CLOCK IN DATA
020E 00                235              NOP
020F A2 91             236              MOV    C,SDA
0211 C2 90             237              CLR    SCL
0213 ED                238              MOV    A,DATAOUT
0214 33                239              RLC    A                     ;ROTATE NEXT BIT
0215 FD                240              MOV    DATAOUT,A             ;SAVE ROTATED DATA
0216 DF F4 [020C]      241              DJNZ   R7,CLOCK8             ;READ 8 BITS OF DATA
0218 31 CD [01CD]      242              ACALL  NO_ACK
021A 31 A1 [01A1]      243              ACALL  STOP_BIT
021C 22                244              RET
                       245    ;*****************************************
                       246
                       247    ;************** SEQUENTIAL READ ************
                       248
                       249    SEQ_RD:
021D 31 95 [0195]      250              ACALL  START_BIT              ;START BIT
                       251
021F 74 05             252              MOV    A,#SLV_ADDR           ;DUMMY WRITE TO FIRST
0221 7F 04             253              MOV    R7,#4H                ;2K BLOCK
0223 31 89 [0189]      254              ACALL  SHFTO
0225 E5 31             255              MOV    A,BLK_ADDR            ;2K BLOCK ADDRESS
0227 7F 03             256              MOV    R7,#3H
0229 31 89 [0189]      257              ACALL  SHFTO
022B 74 00             258              MOV    A,#00H                ;R/W BIT SET TO 0
022D 7F 01             259              MOV    R7,#1H                ;FOR WRITE
022F 31 89 [0189]      260              ACALL  SHFTO
0231 31 AA [01AA]      261              ACALL  SLAVE_ACK
                       262
0233 E5 32             263              MOV    A,BYTE_ADDR           ;ADDRESS TO READ
0235 7F 08             264              MOV    R7,#8H
0237 31 89 [0189]      265              ACALL  SHFTO
0239 31 AA [01AA]      266              ACALL  SLAVE_ACK
                       267
023B 31 95 [0195]      268              ACALL  START_BIT              ;NEW START BIT
                       269
023D 74 05             270              MOV    A,#SLV_ADDR
023F 7F 04             271              MOV    R7,#4H
0241 31 89 [0189]      272              ACALL  SHFTO
0243 E5 31             273              MOV    A,BLK_ADDR            ;2K BLOCK TO READ
0245 7F 03             274              MOV    R7,#3H
0247 31 89 [0189]      275              ACALL  SHFTO
0249 74 01             276              MOV    A,#1H                 ;R/W BIT SET TO 1
024B 7F 01             277              MOV    R7,#1H                ;FOR READ
024D 31 89 [0189]      278              ACALL  SHFTO
024F 31 AA [01AA]      279              ACALL  SLAVE_ACK
                       280
<< ASM51 >> CROSS ASSEMBLER VER.2.5M    ASSEMBLE LIST DATE:          PAGE:   6
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LOC. OBJECT           LINE    STATEMENT                    I2C_8051.ASM

0251 7E 0F            281             MOV    R6,#0FH
0253 7F 08            282     NXT_BYTE:  MOV    R7,#8H
0255 D2 90            283     ONE_BYTE:  SETB   SCL                  ;READ 16 BYTES OF DATA
0257 00               284             NOP
0258 C2 90            285             CLR    SCL
025A 00               286             NOP
025B DF F8 [0255]     287             DJNZ   R7,ONE_BYTE
025D 31 BD [01BD]     288             ACALL  MSTR_ACK              ;ACKNOWLEDGE
025F DE F2 [0253]     289             DJNZ   R6,NXT_BYTE
                      290
0261 7F 08            291             MOV    R7,#8H
0263 D2 90            292     LST_BYTE:  SETB   SCL
0265 00               293             NOP                          ;READ LAST BYTE
0266 C2 90            294             CLR    SCL
0268 00               295             NOP
0269 DF F8 [0263]     296             DJNZ   R7,LST_BYTE
026B 31 CD [01CD]     297             ACALL  NO_ACK                ;NO ACKNOWLEDGE
026D 31 A1 [01A1]     298             ACALL  STOP_BIT              ;STOP BIT
026F 22               299             RET
                      300     ;*****************************************
                      301     END



SSEMBLY END , ERRORS:0
AST CODE ADDRESS:026F
```

:AT64LC10: A User-Friendly Serial E²PROM

avid Wong

ITRODUCTION

ıe CAT64LC10, a 1K bit serial E²PROM device, has a ɔnfiguration of 64 registers by 16 bits(1). Pin configuraɔns are provided in Figure 1. The features that separate ıis particular device from 2-Wire, 3-Wire and 4-Wire atalyst serial E²PROMs include:

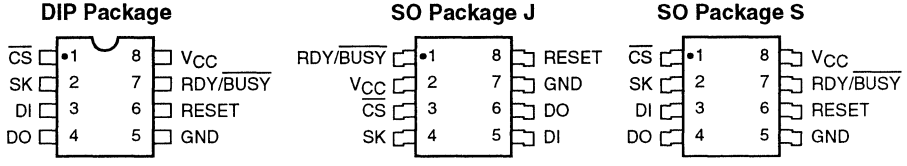
RESET pin which can inhibit any write/erase operation from being executed. It can also abort a write/erase operation that is in progress. This feature adds data protection from inadvertent write in addition to the erase/write enable (EWEN) instruction.

Instructions and data are latched into the input of the device at the rising-edge of the SK clock. Data output from the device is clocked out at the falling-edge of the SK clock. This is useful for interfacing to the SPI bus of Motorola microprocessors.

$\overline{CS}$ (Chip select) must be low to select the device. This is also useful for interfacing to the SPI bus of Motorola microprocessors.

- Two methods for displaying Ready/$\overline{BUSY}$ status:
  1. RDY/$\overline{BUSY}$ pin which normally outputs a logic low when the device is in a programming cycle.
  2. Enable $\overline{CS}$ which will cause DO to output a logic low while the device is programming. As soon as the programming cycle is completed, the DO pin will output a logic high if $\overline{CS}$ is enabled. This "READY" status will be available from the DO pin any time $\overline{CS}$ is enabled. To reset the "READY" status on the DO pin, simply enable $\overline{CS}$, and then enter a logic high on the DI pin. The first rising edge of the SK clock after DI has become "high" will cause the DO pin to return to high impedance.
- Every instruction is a multiple of 16 bits (8 bits of opcode and an 8 bit address or 8 dummy bits). READ or WRITE instructions require an additional 16 bits of data.
- Every instruction begins with a start sequence of "1010". Prior 4 bit sequences other than "1010" will be ignored. For example, starting sequences such as "1000", "1100", "1001" or "1111", etc. will be ignored.

igure 1. Pin Configurations for CAT64LCXX Devices



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Note:
1) Catalyst SPI bus serial E²PROMs are available in densities of 1K, 2K and 4K bits. See Section 4 of this data book.

WHY IS THE CAT64LC10 USER-FRIENDLY?

- Can be configured in a Microwire 3-wire bus structure by simply connecting the DI and DO pins together (see Figure 2). The Ready/$\overline{\text{BUSY}}$ status is obtained from the DO pin.
- Can be configured in a 4-wire bus structure (see Figure 3). In this instance, the Ready/$\overline{\text{BUSY}}$ status is available directly from the RDY/$\overline{\text{BUSY}}$ pin.
- Shifts data in and out at opposite edges of the clock, which makes it easy to interface to microcontrollers by using the system clock instead of having to internally generate a separate clock for serial data transfer. This feature saves code spac and effort in terms of software development.
- Protocol is compatible with SPI interface.
- Pin-controlled data protection.

HOW IS THE CAT64LC10 COMPATIBLE WITH THE SPI BUS?

- The CAT64LC10 accepts a logic low on $\overline{\text{CS}}$ to be selected. Input of instructions and data are clocke in from the DI pin at the rising edge of the clock. When outputting data, the device will shift out dat at the falling edge of the clock (see Figure 4). This interface complies with Motorola's SPI interface.

Figure 2. CAT64LC10 in a 3-Wire Bus Structure

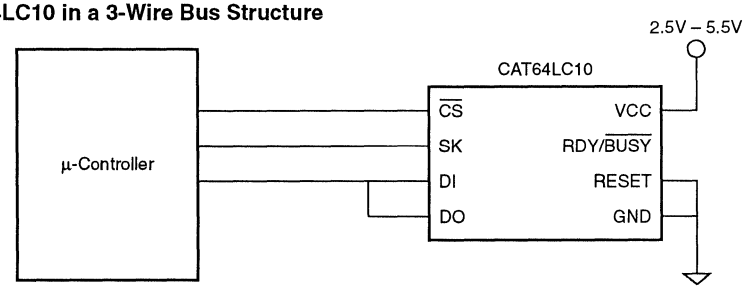

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Figure 3. CAT64LC10 in a 4-Wire Bus Structure

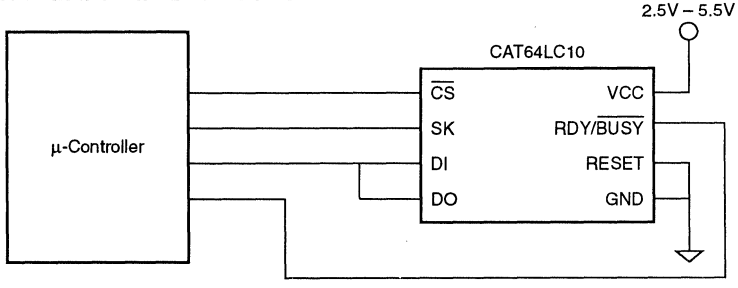

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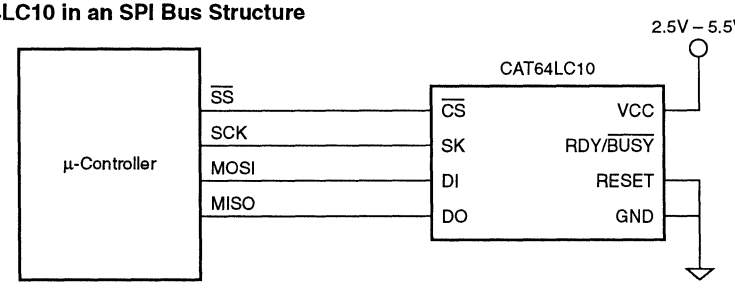
Figure 4. CAT64LC10 in an SPI Bus Structure



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ATA PROTECTION

Software Protection: EWEN/EWDS instructions are erase/write enabling and disabling instructions which can protect the device from inadvertently writing over the data.

Pin Controlled Protection: By setting the RESET pin high, write instructions cannot be executed. The device will ignore the input of a WRITE or WRAL instruction if the RESET pin is held high anywhere during the input of instructions or addresses for more than one clock. However, if the RESET pin is held high after the input of the last address bit for more than one clock, the device will abort the WRITE or WRAL instruction and output a READY status.

CAUTION: Interrupting a programming cycle which is in progress can have unpredictable results in terms of data integrity and is therefore not recommended.

How to Use Catalyst Secure Access Serial E²PROMs

pplications Staff

NTRODUCTION

his application note is intended to be a tutorial on the se of CAT35C704/CAT35C804A-B Secure Access erial E²PROMs. Device operation and typical applica- ons for the device are shown as well as examples for ach of the instructions available. Also included is formation on an evaluation board with software that onnects to a PC and allows the user to quickly and asily evaluate and test the device(s).

EVICE OPERATION

he CAT35C704/CAT35C804A-B is a 4K bit Secure ccess Serial E²PROM that can be used in applications at require nonvolatile memory storage and a need to rotect the contents of that memory from unauthorized ccess. Two basic modes of operation are available, rotected and unprotected. In the unprotected mode, ith the memory pointer set to "0", the device operates e a standard E²PROM, allowing full read/write access the entire array.

sing the memory pointer the user can determine how uch memory needs protection. With the WMPR com- and, a pointer value can be set to split the memory rray into two blocks. Addresses above the pointer value offer full Read/Write access; addresses below and including the pointer are Read only (see Figure 1).

In the protected mode, up to 8 bytes of password security are available. Once the password has been set and a disable access (DISAC) command (or power down) has been executed, the device becomes inaccessible with only the portion of the array not protected by memory pointer readable (see Figure 2). Upon power up, the correct password must be sent to the device before any writing or moving of the memory pointer can be done. This scheme lends itself to applications where users are allowed to view only those portions of memory that is intended for them to see. For example, an application where data is uncovered in the array (by moving the memory pointer) to make available to the user certain features/options that they require, as in the cable TV industry (see Figure 3).

Among the 19 instructions available with the CAT35C704/CAT35C804A-B is a Read Status Register (RSR) instruction, which lets a system interrogate the device and determine its working status. The 8 bit status register displays information regarding parity errors, instruction errors and RDY/$\overline{\text{BUSY}}$ status. An organization instruction (ORG) is also available for organizing the memory into either 512x8 or 256x16 configurations depending on the application.

igure 1. Access Control Using No Access Code

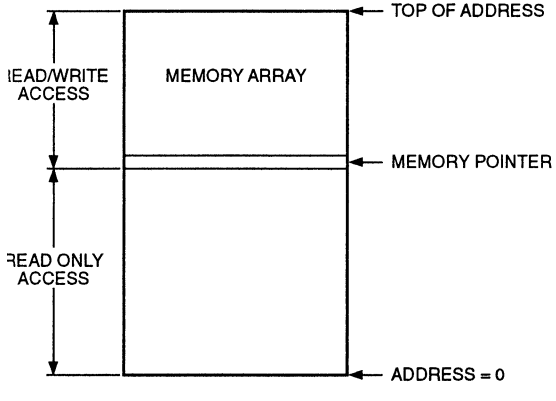

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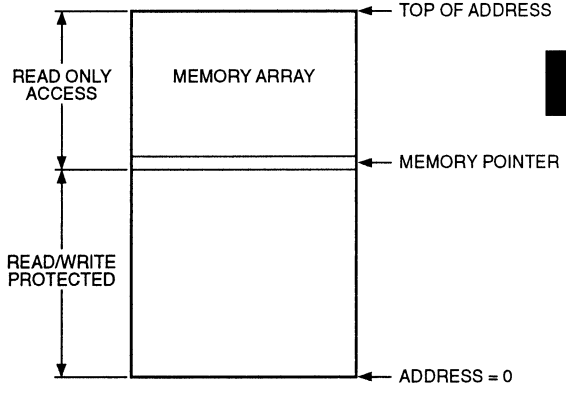
Figure 2. Access Control Using Access Code



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In addition, to allow for reading multiple words from the memory and minimize the overhead of repeated Read instructions, a Read Sequential (RSEQ) instruction allows you to specify a starting location and then continuously shift out data to the end of the array.

The security code is entered/modified by sending the Modify Access Code (MACC) instruction followed by the length of the access code (1 to 8 bytes), the old access code (if needed), and then the new access code twice (for verification). Once power has been removed (or the DISAC instruction sent), the Enable Access (ENAC) instruction, followed by the correct access code, must b sent to the device or the memory array's protecte portion cannot be accessed, and the memory conten above the pointer remain Read only.

A simple interface is shown in Figure 4 where th CAT35C704 is used in an electronic key applicatio The device interfaces directly to a microprocessor and used as the security portion of a door lock mechanisr The lock is only activated when the key's (hotel key, c key, etc.) access code matches the one stored in th CAT35C704.

Figure 3. Using CAT35C704/CAT35C804A-B for Protected Features

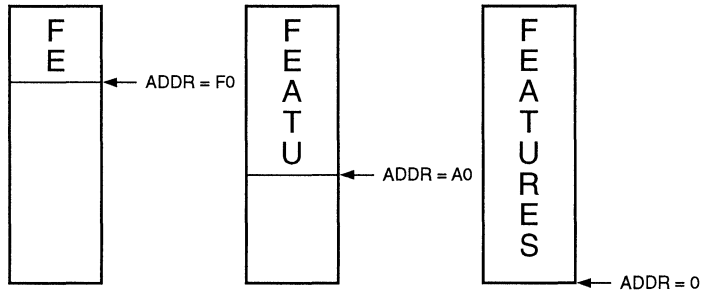

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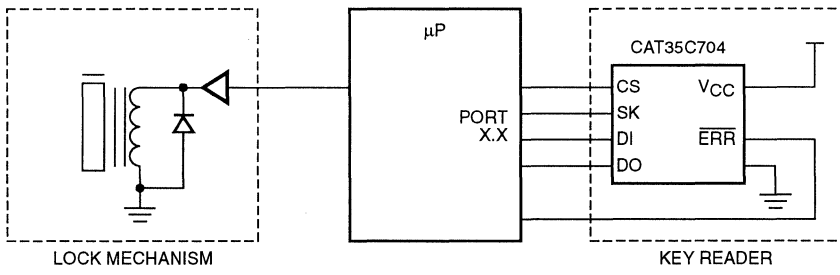
Figure 4. CAT35C704 in an Electronic Key



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ıSTRUCTION SET

ıe following section describes the 19 instructions avail-ɔle for the device and examples of each.

ECURITY OR WRITE PROTECT ıSTRUCTIONS

MACC–Modify Access Code

ıis instruction allows the user to issue a new password ı the device or modify an existing one. The password issued in the following manner:

101 [Length of new pswrd] [old pswrd] [new pswrd] [new pswrd]

ɔr example, to issue the device a password for the first ıe, send the following:

1101	3	AA 55 D2	AA 55 D2
ıstruction Code	*Length*	*3-Byte Pswrd*	*Repeat 3-Byte Pswrd*

he device now has a 3 byte password of AA 55 D2. To ıange this password to a 5 byte password, send the ɔllowing:

1101	5	AA 55 D2	01 02 03 04 05	01 02 03 04 05
ıstruction Code	*Length of New Pswrd*	*Old Pswrd*	*New Pswrd*	*Repeat New Pswrd*

he device now has a 5 byte password equal to 01 02 03 4 05. This password can be modified in the same ıanner to any length password you choose, up to 8 ytes.

inally, to modify the password back to a 0 length (no assword), send the device the following instruction:

1101	0	01 02 03 04 05
ıstruction Code	*Length of New Pswrd*	*Old Pswrd*

he device is now in the unprotected mode.

. **ENAC/DISAC**—Enable/Disable Access

hese two instructions permit the user to turn on or off ıe password protection to the device. To disable any ccess to the device, send the following instruction:

1000 | 1000
Instruction Code

The device will give no indication that it has been disabled other than you now cannot Read or Write to the array.

To enable the device operation, send the following instruction:

1100 | 0101 [Access Code]

For example, to enable access to a device that has an 8 byte password stored in the access code register, send the following:

1100 | 0101	01 02 03 04 AA BB CC DD
Instruction Code	*8-Byte Pswrd*

Again, the device gives no indication that you have entered the correct password, however you now have full Read/Write capabilities.

3. **WMPR**—Write Memory Pointer Register

The Write Memory Pointer Register instruction allows you to modify the contents of the memory pointer register. The value of the register determines what portion of the memory array is protected from byte-writes during unprotected operation and what portion you are allowed to read during protected operation.

For example, if there is no password protection and the memory pointer is set to 00AA, then no byte-writes from address 0000 to address 00AA are allowed (unless the OVMPR instruction has been entered previously). In the protected mode, with the memory pointer set to the same value (00AA), a Read Sequential (RSEQ) instruction from address 0000 will not allow the user to read any of the array. The RSEQ instruction must begin at 00AA and will then allow read access from 00AA to the end of the array. Note: The memory pointer contents will not block Erase All or Write All operations.

To change the contents of the register, send the following:

1100 | 0100 [A15–A8] [A7–A0] *x8*
[A7–A0] *x16*

This instruction is operational only after an ENAC instruction (if a password has been set) and an EWEN (see EWEN section) instruction have been sent to the device. Once this is done, you can modify the register contents to the desired value. For example, to change the contents from 0000 to 0123, send the following:

1100 | 0100	0123
Instruction Code	*New Memory Pointer Value*

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The memory pointer register now has a value of 0123 (x8).

4. **RMPR**—Read Memory Pointer Register

The Write Memory Pointer Register instruction allows you to read the location in memory where the memory pointer resides. This tells you which portions of the memory are divided between read only and full read/write access. To read the value of the register, send the following:

1100 | 1010
Instruction Code

The device will then return the hex value of the memory pointer location.

5. OVMPR—Override Memory Pointer Register

This instruction allows the user to write data to a protected area of memory on a one time basis, without having to uncover that area with the memory pointer. For example, to write data to an area protected by the memory pointer the OVMPR instruction would be issued, followed immediately by a write instruction. After the write has been completed, the area of memory is again protected.

1000 | 0011
Instruction Code

READ/WRITE/ERASE INSTRUCTIONS

1. **READ**—Read Memory

This instruction outputs the data from memory at the specified location.

1100 | 0101	[A15–A8] [A7–A0] *x8* [A7–A0] *x16*
Instruction Code	*Address*

For example, to Read the contents of address 1AH, send the following:

1100 | 1001	00011010

The device then outputs data located at this address on the DO pin.

2. **WRITE**—Write Memory

The Write instruction writes an 8 or 16 bit data word into a specified address of memory. Once the instruction, address, and data have been entered, the self-timed program/erase cycle will start. The addressed memory location is erased before data is written. For example, write the data 5A2D Hex to address C8, send the following:

1100 | 0001	11001000	0101101000101101
Instruction Code	*Address (x16)*	*Data (x16)*

After the specified Program/Erase pulse width, the data 5A2D is written to address C8 Hex.

3. **ERASE**—Clear Memory

The Erase instruction clears the specified memory location by setting all cells to a logic "1". Once the instruction and address have been entered, the self-timed erase cycle will start. For example, to erase the data located at address 1234 Hex, send the following:

1100 | 0000	0001001000110100
Instruction Code	*Address (x8)*

After the specified Erase pulse width, the contents of address 1234 Hex will be FF Hex.

4. **ERAL**—Erase All

The Erase All instruction clears the data from all locations in the memory. To erase the entire device, send the following:

1000 | 1001	1000 | 1001
Instruction Code	*Instruction Code*

The code is required to be sent twice (to protect against inadvertent chip clear) and, once sent, clears all locations to the FF Hex state.

5. **WRAL**—Write All

The Write All instruction is used to write the same data byte to all locations in the memory. For example, to write the data AA Hex to all locations, send the following:

1000 | 1001	1100 | 0011	10101010
Instruction Code	*Instruction Code*	*Data (x8)*

After the specified Program/Erase pulse width, all locations in the device will now have AA Hex written to them.

6. **RSEQ**—Read Sequential

The Read Sequential instruction allows the user to sequentially clock out data starting at a specified address continuing until the end of memory or Chip Select is brought low. For example, to read memory starting at

ıdress 4D Hex continuing to the end of the array, send e following:

100 | 1011	01001101
nstruction Code	*Address (x16)*

ıe device will now clock out (SK pin must be clocked by ;er) the contents of memory starting at address 4D and ɔntinuing to the end of memory.

TATUS AND CONTROL INSTRUCTIONS

EWEN—Erase/Write Enable

his instruction is required to be entered before any ·ogram/erase instruction will be carried out. Once it is ıtered, it remains valid until a power down or a EWDS ;truction is sent. To enable the device for writing/ ·asing, send the following:

000 | 0001
Instruction Code

he device is now ready to be erased or written to.

. **EWDS**—Erase/Write Disable

his instruction disables all writing or erasing of the evice. Once sent, the device must be sent an EWEN ıstruction before any erase/write instruction will be erformed. To disable erase/write instructions, send the ɔllowing:

0000 | 0010
Instruction Code

he device is now protected from any erase or write ıstructions.

. **ORG**—Select Memory Organization

his instruction allows the user to select a x16 or x8 ıemory organization. For example, to configure the evice with a word length of 8 bits, send the following:

1000 | 0110
Instruction Code

o configure the device with a word length of 16 bits, end the following:

1000 | 0111
Instruction Code

4. **RSR**—Read Status Register

The Read Status Register instruction allows the user to determine the state of the device. To determine if the device is in an error condition, send the following:

1100 | 1000
Instruction Code

The device then responds with an 8 bit status word that gives the following information:

10100000 - the device is operating normally
10110000 - the device has a parity error
10101000 - the device has an instruction error
10100100 - the device is in the program/erase cycle

5. **DISBSY**—Disable Busy

The Disable Busy instruction disables the RDY/$\overline{\text{BUSY}}$ status on the DO (data out) pin. To disable the RDY/$\overline{\text{BUSY}}$ function, send the following:

1000 | 0101
Instruction Code

The RDY/$\overline{\text{BUSY}}$ status is now no longer available on the DO pin.

6. **ENBSY**—Enable Busy

The Enable Busy instruction enables the RDY/$\overline{\text{BUSY}}$ status on the DO pin. To enable this status, send the following:

1000 | 0100
Instruction Code

The RDY/$\overline{\text{BUSY}}$ status is now enabled on the DO pin. This allows the user to tell if the device is in the program/erase cycle (DO low) or has completed it (DO high).

7. **NOP**—No Operation

The NOP instruction leaves the device in an idle mode; no operation is executed.

SECURE ACCESS SERIAL E²PROM

EVALUATION KIT

- Single Board Evaluation Kit for Secure Access Serial E²PROMs
- Interfaces to IBM/Compatible PC via Serial Communication Port or Parallel Printer Port
- Supports Both Synchronous and Asynchronous Communications
- Ideal as Application Design Tool
- Comprehensive Users Manual
- PC Communications Program and Power Supply Included

OVERVIEW

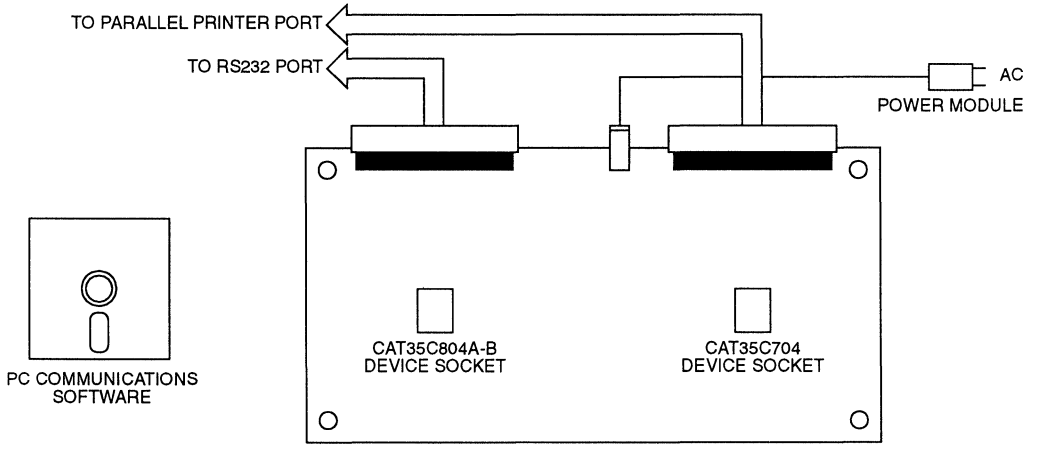
The Catalyst Secure Access Serial E²PROM Evaluation Kit is a simple, low cost solution to programming CAT35C704/CAT35C804A-B serial E²PROMs. The complete package consists of a 4" x 7" hardware board partitioned into two halves for either CAT35C704 or CAT35C804A-B programming. Each half contains an 8 pin device socket, I/O connector, and all necessary interface chips and switches to completely evaluate the CAT35C704 synchronous device or the CAT35C804A-B UART compatible asynchronous device. A wall mount power supply is provided for board operation. MS/DOS compatible software is included for easy device instruction execution.

The kit enables you to use your IBM/Compatible PC a a local evaluation station for device testing and applic tion design.

To test the CAT35C704, connect a standard print cable (50 pin Centronix) to the "704" half of the evalu tion board, insert a device in the test socket and run th evaluation software provided. Similarly, for th CAT35C804A-B, connect a standard RS232 cable the "804" half of the evaluation board, insert a devic and run the appropriate "804" software.

The evaluation package allows the user a faster ar easier path to high security applications.

Figure 5. Secure Access Serial E²PROM Evaluation Board



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VALUATION BOARD INSTRUCTION SET:

he evaluation kit comes with communication software iat allows you to exercise all 19 instructions for Catalyst ecure Access Serial E²PROMs. The first six are ɜlated to security or write protection:

ISAC: The Disable Access instruction locks the memory om all write/erase operations and once enabled, a rite can only be accomplished by first sending the NAC (and access code) instruction.

NAC: The Enable Access instruction followed by a alid access code unlocks the device for READ/WRITE/ RASE operations.

VMPR: The Write Memory Pointer Register command ollowed by address) will move the memory pointer to ıe newly specified address.

IACC: The Modify Access Code instruction allows the ser to change the access code formerly entered or nter one for the first time. The new access code must e entered twice for security measures.

)VMPR: Override Memory Pointer Register allows the ıser to bypass the memory protection for one instruction ınly, following its use, after which the memory is again ıotected from write/erase operations.

ɪMPR: The Read Memory Pointer Register command ıllows the user to interrogate the contents of the memory ıointer register.

he next six instructions are used for READ/WRITE/ ERASE operations:

ERAL: The Erase All command lets you erase the ontents of the entire memory.

ERASE: The Erase command allows you to erase only ı specified address of the memory.

ɪEAD: This instruction will output the contents of the ıddressed memory location to the serial port.

RSEQ: Read Sequential allows you to read the memory from the specified address to the end of memory. It terminates upon reaching the end of memory or when CS goes low.

WRAL: The Write All instruction writes one (or two) bytes of data to all memory locations. An erase all is automatically performed before the WRAL is executed.

WRITE: This command writes the 8 bit or 16 bit data to the addressed memory location. The location being written to is automatically erased before being written to.

Seven instructions are used as control and status functions:

DISBSY: Disables the status indicator on DO during a write/erase cycle.

ENBSY: Enables the status indicator on DO during write/erase cycle. The data out pin goes LOW then HIGH once the write cycle is completed and will go to High-Z at the end of the next op-code transmission.

EWEN: This command enables an erase or write to be performed on non-protected portions of the memory, and must be entered prior to any erase/write operations.

EWDS: This instruction disables all erase and write functions.

ORG: This organization command configures the memory as either a 256x16 or 512x8 array.

RSR: This command outputs the contents of the 8 bit status register and allows the user to quickly determine the working status of a device. RDY/$\overline{\text{BUSY}}$, instruction error and parity error status is displayed.

NOP: No operation is performed.

Catalyst Parallel E²PROMs Feature Software Data Protection

Dan Apple

A common concern among E²PROM users is data integrity during power on/off transitions and system glitches that may cause inadvertent writes to the memory array. Hardware data protection schemes have been around for some time to reduce this problem. They include:

- V_{CC} lockout voltage below which writes are inhibited.
- Power on delay mechanism where writing is inhibited a fixed time after V_{CC} is stable.
- Write inhibits by holding $\overline{CE}$, $\overline{OE}$ or $\overline{WE}$ high.
- Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs are ignored.

Despite these hardware protection features, additional protection is being required by industry users. Catalyst has added Software Data Protection (SDP) to its 64K bit and 256K bit E²PROMs. The CAT28C64B and CAT28C256 parallel E²PROMs feature software controlled data protection that once enabled, requires a set write sequence to be sent to the device prior to any writes being performed. Figures 1 and 2 provide the software sequence required to activate Software Data Protection for both devices:

Figure 1. CAT28C64B Write Sequence for Activating Software Data Protection

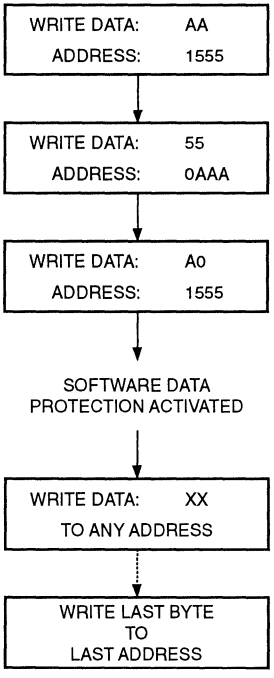

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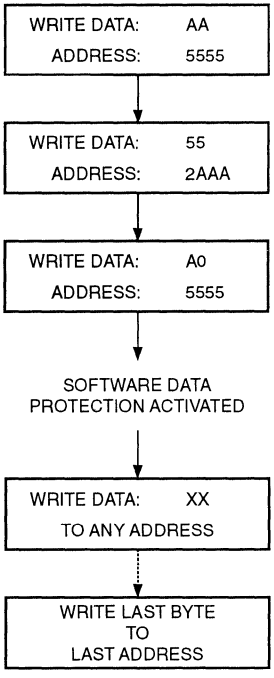
Figure 2. CAT28C256 Write Sequence for Activating Software Data Protection



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Once Software Data Protection has been activated, it remains activated through any power on/off transitions and, prior to any writing, the user must send the device this same algorithm. The addresses used are located on different page boundaries so that the data bytes used in the SDP algorithm are not actually written to the device.

In the event the user wishes to deactivate the SD feature a six step algorithm is provided. Figures 3 an 4 provide this algorithm for both devices.

Once issued the device returns to a normal operatin condition and data already written to the device remain unchanged.

Figure 3. CAT28C64B Write Sequence for Deactivating Software Data Protection

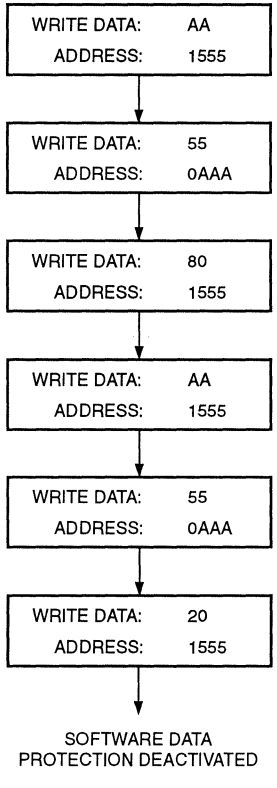

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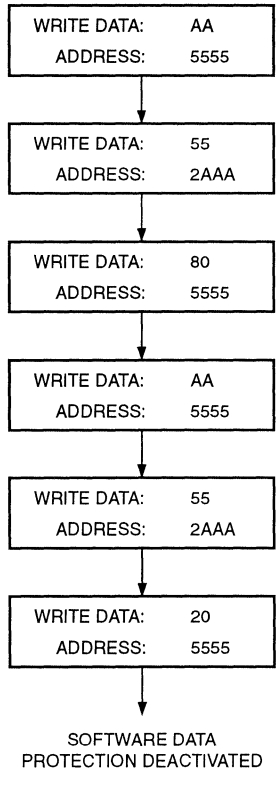
Figure 4. CAT28C256 Write Sequence for Deactivating Software Data Protection



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Advantages of 5V Flash Memories

Ian Apple

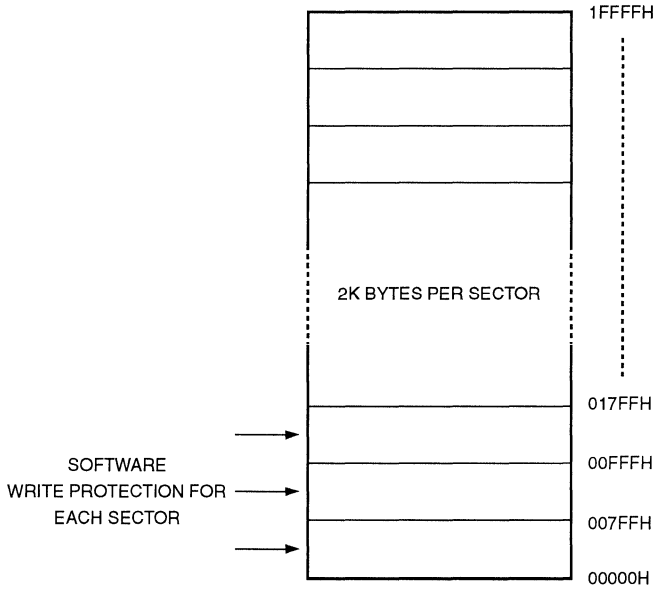
INTRODUCTION

Flash memories continue to fill the void between conventional one transistor cell EPROMs and byte-alterable two transistor cell E²PROMs. Since these nonvolatile memories have the same JEDEC pinouts as EPROMs, the devices are socket compatible in most systems and require only simple software modifications. Programming of a Flash memory is done with the same hot-electron injection technique used on EPROMs, whereas cell erasure is accomplished via the E²PROM Fowler-Norheim tunneling phenomenon. Thus, by combining these two technologies, Flash memories are able to provide the user competitive EPROM pricing capability along with the in-system reprogrammability that E²PROMs offer.

FEATURES

The CAT28F512V5 and CAT28F010V5 offer features that nonvolatile memory users have been requesting for some time. The feature most attractive to users with small, portable, power-conscious systems is the 5V operating supply. With an on-board charge pump to boost the voltage to the required level for erasing and programming, the user does not need an external 12V supply required on other Flash memories. Since the standard 5 to 12V converter chip (and associated components) is not required, overall system cost is reduced. Additionally, the memory is divided into 32 2K-byte sectors (64 for the 1Megabit), and each sector can be randomly accessed for program/erase operations (see Figure 1).

Figure 1. CAT28F010V5 Sector Erase Architecture



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With this flexible sector erase architecture, the user has the option of individual sector, multiple sector or bulk program/erase capability. Boot code can be stored in selected sectors to ensure system re-boot code does not get erased; a problem faced by 12V bulk-erase Flash users. Additionally, the CAT28F010V5 offers software controlled sector protection. This feature allows sector protection by write protecting individual or multiple sectors. Each sector has a nonvolatile bit that can be set via a software command, allowing the specified sector(s) to become read-only.

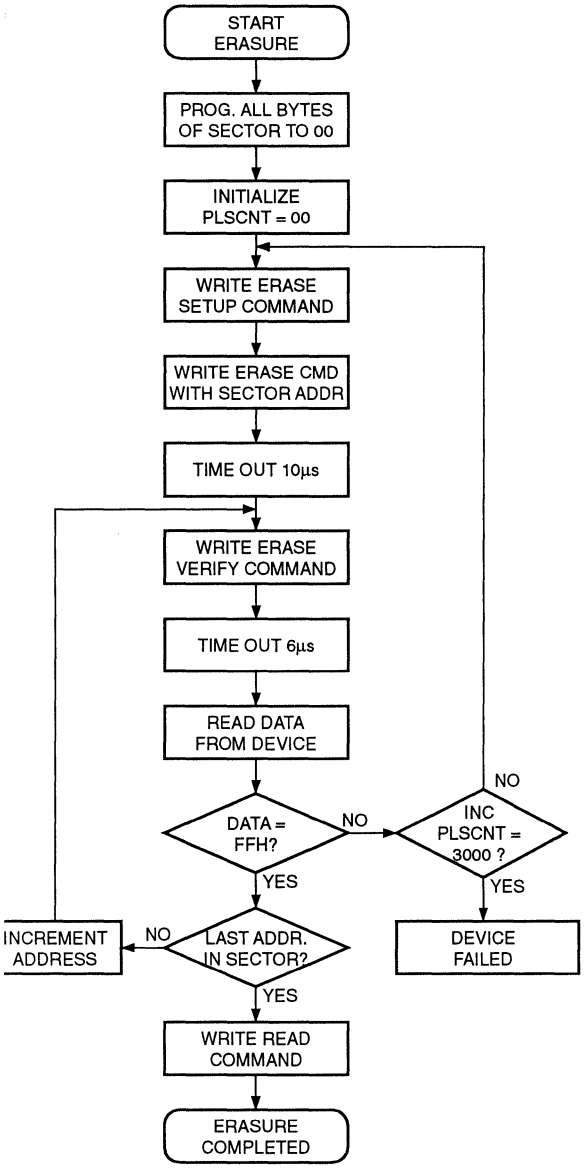
The evolving portable computing market, currently divided between the notebook/pen-based machines and the handheld/palmtop computers, is an ideal match for Flash memories. The need for low-power lightweight systems allows Flash memories to be used as a hard disk replacement. The density, quality, reliability, compactness(1) and low power dissipation are the attractiv features for computer manufacturers. Flash memorie do not have the power requirements of hard disk drive and the instant-on read capabilities are useful for storin application programs.

Some of the applications that Flash memories are ta geting include: applications requiring selective repr gramming, BIOS code storage, embedded control, lase printers, medical equipment, PCMCIA memory card control applications in disk drives, electronic engine communications and networking.

Minor software algorithm changes are required whe replacing 12V bulk erase Flash devices with 5V sect erase Flash memories. Figure 2 details the Sector Eras Algorithm used on the CAT28F512V5 device.

Note:
(1) All Catalyst Flash memories are offered in TSOP packaging.

igure 2. Random Access Sector Erase Algorithm



BUS OPERATION	COMMAND	COMMENTS
		ALL BYTES WITHIN SECTOR SHOULD BE PROGRAMMED TO 00 BEFORE AN ERASE OPERATION
		PLSCNT = PULSE COUNT
WRITE	ERASE	ACTUAL ERASE NEEDS 10ms PULSE, DATA = 60H
WRITE	ERASE	DATA = 60H ADDRESS = SECTOR ADDR
		WAIT
WRITE	ERASE VERIFY	ADDR = BYTE TO VERIFY DATA = A0H
		WAIT
READ		READ BYTE TO VERIFY ERASURE
STANDBY		COMPARE OUTPUT TO FF INC PULSE COUNT
WRITE	READ	DATA = 00H, RESETS REGISTERS FOR READ OPERATION
STANDBY		

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CATALYST SEMICONDUCTOR

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Catalyst Quality and Reliability

INTRODUCTION

The Catalyst corporate mission statement is:

-Use state of the art nonvolatile memory technology to produce innovative leading edge products and obtain a leadership position in all reprogrammable product markets.

-Adopt a global manufacturing strategy by using strategic partners to produce cost-effective, high quality products.

-Provide excellent service to customers worldwide and enter into mutually beneficial, long term partnership agreements.

The Catalyst Quality and Reliability Policy Manual (available on request) contains the methods and philosophies to implement the corporate mission. Catalyst is utilizing a quality system in accordance with the requirements of ISO-9001 "Quality Systems — Model for Quality Assurance in Design/Development, Production, Installation, and Servicing" and the criteria of MIL-M-38510, appendix A "Product Assurance Program".

MANUFACTURING TECHNOLOGY

Catalyst fabricates all memory devices using a CMOS process. The fundamental storage element in all Catalyst reprogrammable nonvolatile memories is a floating gate memory transistor. Details of various memory cells operation are included in the Catalyst Quality and Reliability Application Notes in this section.

All wafer fabrication and package assembly processes have flow charts and baselines as controlled documents. Basic descriptions of all Catalyst device construction are available on request. Detailed descriptions are proprietary; however, a nondisclosure agreement may be used, if required.

QUALIFICATION METHODOLOGIES

Catalyst qualifies reprogrammable nonvolatile memories in accordance with the guidelines of the IEEE Standard Definitions and Characterization of Floating Gate Semiconductor Arrays (IEEE Std 1005–1991, available from IEEE), MIL-STD-883, and JEDEC Standard 22 (JESD-22).

Devices are qualified by Design/Process and Package families. This reduces the overall cost of qualification, while providing assurance that each combination of design, process, and package meets minimum reliability requirements.

A Design/Process family consists of those devices using similar logic, layout, and design rules using the same wafer fabrication process and location.

A Package family consists of those devices using the same assembly package configuration, materials, and location.

Once a representative device is qualified, other members of the Design/Process families are qualified in that package family. Thus, each possible combination of design, process, and package does not require stressing, in order to have each combination fully qualified or requalified after changes. Reference Catalyst specifications (available on request) for Qualification Requirements and Critical Process Change Notification.

For example: If a serial E^2PROM, built on a 1.5 µ process is qualified in a SOIC package; then, other serial E^2PROMs (using the similar logic, layout, and design rules) built on the same 1.5µ process, are also qualified in the same SOIC package.

Catalyst provides Reliability Summaries (upon request) for all devices. Reliability Summaries contain three sections: Design/Process Family, Package Family, and Device Specific.

The Design/Process Family data summary includes the following sections: Reliability Stress, Stress Conditions, Device Hours, # Failures, Failure Rate at 90% C.I. (i.e., at the stress temperature in %/1000 hours) and a Cause category for any failures. The Summary includes: the Device Hours (at the deaccelerated temperature of 55°C), the Apparent Activation Energy and the failure rate at 90% C.I. in FITs (or FICs for endurance). The "Endurance Cycles to Time Conversion Nomograph" is included for the demonstrated endurance failure rate. This format is used for reporting Life Test, Data Retention and Endurance.

The Package Family data summary includes the following sections: Reliability Stress, Stress Conditions, # Lots, Failures/Timepoint. This format is used for reporting: Solder Heat Resistance, including subsequent

Life Test and Data Retention, HAST, Pressure Pot, Biased 85/85, Temperature Cycles, Thermal Shock, Marking Permanency, Lead Fatigue and Physical Dimensions.

The Device Specific data summary includes the following sections: Reliability Stress, Stress Conditions, # Lots, Failures/Timepoint. The data reported includes: Machine Model and Human Body Model ESD results and latch-up data.

ENDURANCE AND DATA RETENTION GUARANTEE

Endurance

Endurance is the measure of the ability of a reprogrammable nonvolatile memory device to meet its data sheet specifications as a function of accumulated program/erase cycles. A device program/erase cycle is the act of changing data from original (e.g., erased) to opposite (e.g., programmed) back to original for all bits of the memory array.

Catalyst provides an endurance lot acceptance guarantee of a 1% AOQL (LTPD 5/1) for the number of program/erase cycles per byte as specified by the applicable data sheet. The endurance is independent of the program or erase method, e.g., byte, page, sector, block, chip. Endurance is verified by the customer with the Endurance, Data Retention and Steady State Life Test Methodology.

Data Retention

Data Retention is the measure of the integrity of the stored data as a function of time. Data retention is the time from data storage to the time at which a repeatable data error is detected.

Catalyst provides a data retention lot acceptance guarantee of a 1% AOQL (LTPD 5/1) for the number of years per device as specified by the applicable data sheet. This applies across the operating temperature range and after the specified minimum number of endurance cycles. Data retention is verified by the customer with the Endurance, Data Retention and Steady State Life Test Methodology.

ENDURANCE, DATA RETENTION, AND STEADY STATE LIFE TEST METHODOLOGY

An endurance test, reference Method 1033 of MIL-STD 883, shall be added before performing the steady stat life test and extended data retention test. Cycling may b chip, sector, block, byte or page on finished devices. Th following conditions shall be met:

(1) All bytes shall be cycled for a minimum of th specified number of cycles at equipment room ambien

(2) Perform parametric, functional and timing tests a room temperature, after cycling. Devices having bits nc in the proper state after functional testing shall constitut a device failure. Separate the devices into two groups fc extended data retention and steady state life test, the write applicable data patterns.

(3) Perform the extended data retention, consisting of high temperature unbiased storage for 1000 hours min mum at 150°C minimum. The storage time may b accelerated by using a higher temperature according t the Arrhenius relationship and an apparent activatio energy of .6eV. The maximum storage temperature i an Nitrogen environment shall not exceed 175°C fc hermetic or 160°C for plastic devices. All devices sha be programmed with a charge on all memory cells i each device, such that a loss of charge can be detecte (e.g., worst case pattern).

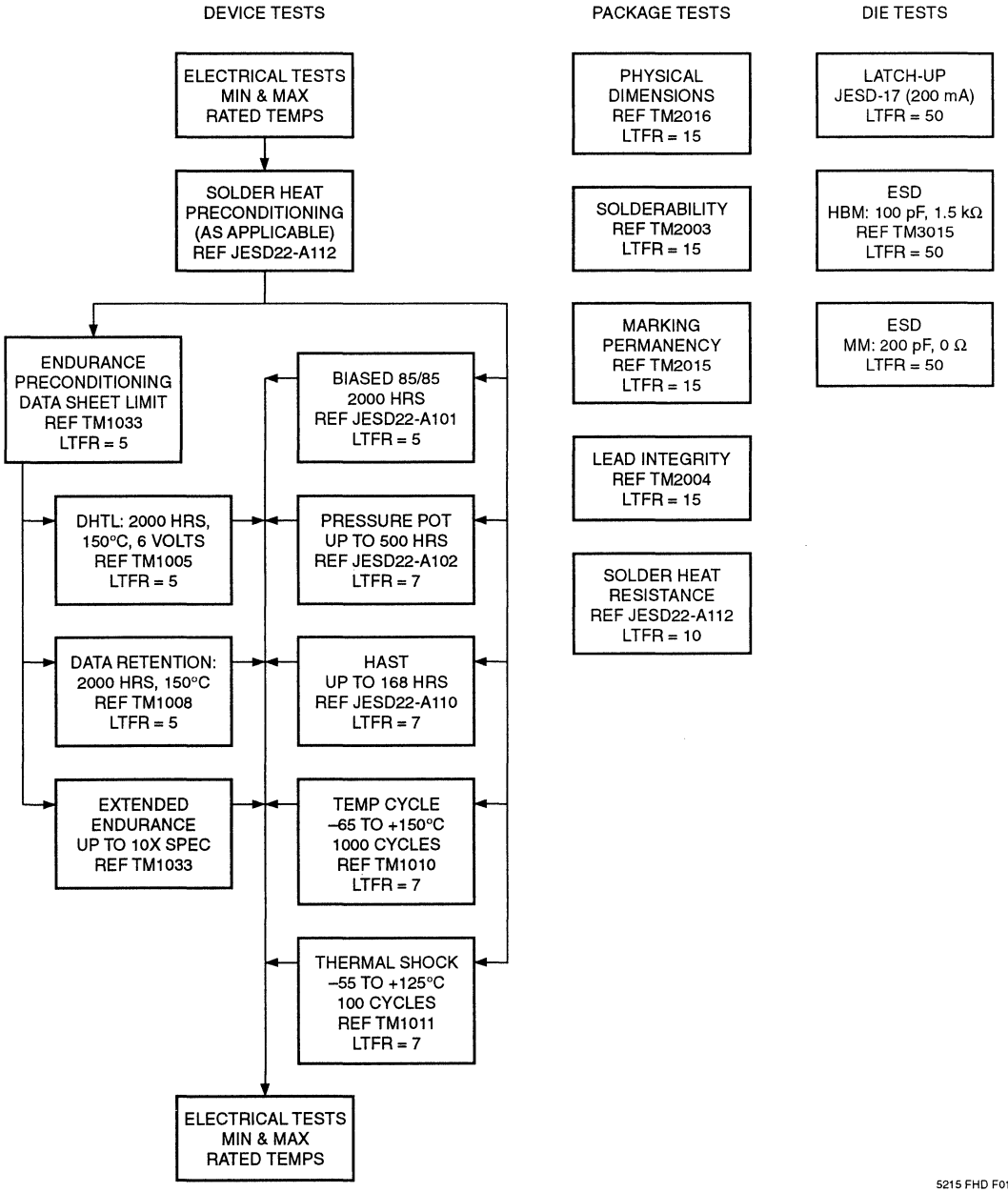
(4) Read the data retention pattern and perform para metric functional and timing tests at room temperature after cycling and bake. Devices having bits not in th proper state after functional testing shall constitute a device failure.

(5) Perform steady state life, reference method 100 condition D of MIL-STD-883, for 1000 hours at 125°C i an Nitrogen environment. The steady state life time ma be accelerated by using an Arrhenius relationship an apparent activation energy of .4 eV. The maximun operating junction temperature shall not exceed 175°C All devices shall be written with a checkerboard o equivalent topological alternating bit pattern.

(6) Read the steady state life pattern and perform para metric, functional, and timing tests at room temperature after cycling and steady state life. Devices having bit not in the proper state after functional testing shal constitute a device failure.

(7) The endurance, data retention, and steady state life tests shall individually pass a sample plan to an LTPD o 5/1 (sample size = 77, accept = 1), equivalent to ar AOQL = 1%.

igure 1. Qualification Requirements (Commercial Plastic Package)



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Note:
1) LTFR = Lot Tolerant Failure Rate or LTPD, sample sizes per MIL-M-38510, appendix B.
2) TMxxxx refers to Test Methods per MIL-STD-883.
3) JESD22 refers to the test methods per JEDEC Standard 22.

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Table 1. General Requirements

Stress Codes	Names of Stress Methods	Standard Conditions
DHTL	Dynamic High Temperature Operating Life	2000 hours @ 150°C
DRSL	Data Retention Storage Life	2000 hours @ 150°C
ENDR	Endurance	10X Data Sheet @ 25°C
THBS	Temperature Humidity Bias Stress	2000 hours 85°C/85%RH
PPOT	Pressure Pot	500 hours @ 121°C
HAST	Highly Accelerated Stress Test	168 hours @ 140°C
TMCL	Temperature Cycling (air-to-air)	1000 cycles –65°C/150°C
TMSK	Thermal Shock (liquid-to-liquid)	100 cycles –55°C/125°C

RELIABILITY STRESS METHODS

DHTL—Dynamic High Temperature Operating Life

Description: This stress accurately replicates the users operating conditions for a device. All inputs are toggled in the read mode and outputs are loaded with an appropriate worst case load. This stress maximizes the number of nodes subjected to changing electric fields in order to optimize detection of latent failures caused by such problems as oxide faults, pinholes, or leaky junctions.

Minimum Duration: 2000 hours at an ambient temperature of 150°C. Catalyst CMOS devices have a small junction temperature rise in this stress, thus there is no concern for elevated temperatures creating packaging or silicon problems.

DRSL—Data Retention Storage Life

Description: This stress exposes the parts to unbiased storage at an elevated temperature, normally 150°C for plastic packages and 250°C for hermetic packages. These are the highest practical temperatures the applicable package can sustain to accelerate the loss of charge off the floating gate.

Temperature: For plastic packages, 165°C is at the maximum safe storage temperature, because the glass transition temperature of most epoxies is below 165°C. Above 165°C, the mechanical and chemical stability of the plastic is uncertain, thus prolonged exposure can create failure mechanisms that would otherwise not be observed. For solder seal hermetic packages, 260°C is the maximum temperature before damaging the solder seal. For glass frit seal hermetic packages, 300°C is the maximum prolonged storage temperature before introducing unpredictable effects in the silicon.

Minimum duration: 2000 hours at 150°C.

ENDR—Endurance

Description: This stress replicates the user's writin conditions for the device. All bits are erased and prc grammed. The stress detects failures due to oxid rupture or charge trapping of the tunnel dielectric c failures in peripheral oxides.

Minimum Duration: The data sheet specified number c cycles must be performed before DHTL or DRSL. Ex tended endurance will be to at least 10 times the spec fied number of cycles.

THBS—Temperature Humidity Bias Stressing

Description: This accelerated temperature and humidit bias stress is performed at 85°C and 85% Relativ Humidity, reference JESD-22, Test Method A102. I general, the worst-case bias condition is the one tha minimizes the device power dissipation and maximize the applied voltage. Higher power dissipations tend t lower the humidity level at the chip surface and lesse the corrosion susceptibility.

Minimum Duration: 2000 hours. As HAST become more widely accepted, it may supplement or replac THBS stressing.

PPOT—Pressure Pot

Description: This stress exposes the devices to satu rated steam at an elevated temperature and pressure The standard condition is 15 PSIG, at a temperature o 121°C, reference JESD-22, Test Method A102. The plastic encapsulant is not a permanent moisture barrie and will eventually saturate with moisture. Since the chip is not biased, the chip temperature and relative humidity will be the same as the autoclave once equilibrium is reached.

fectivity: The steam environment has an unlimited pply of moisture and ample temperature to catalyze ermally activated events, thus is effective at detecting rrosion problems, contamination-induced leakage oblems, general glassivation stability and integrity, ckage integrity (cracks in the package), and for die acks (the moisture swells the plastic enough to stress e die; also, the moisture causes leakage paths in the ack itself.)

nimum Duration: 336 hours for surface mount packjes and 500 hours for DIL packages.

AST—Highly Accelerated Stress Test

escription: This highly accelerated biased humidity mperature test combines the worst-case characteris-s of 85/85 stressing and the high temperature, high essure characteristics of PPOT testing. The ambient saturated steam. The stress condition is 140°C and 5% RH, reference JESD-22, Test Method A110. HAST often used in process control as a rapid test for oisture reliability assessment. Optimum bias condions are the same as used for 85/85.

emperature: Bond integrity may be compromised for tended HAST stressing at junction temperatures in cess of 150°C.

inimum Duration: 96 hours for surface mount packges and 168 hours for DIL packages.

MCL-Temperature Cycling, Air-to-air

escription: The device is cycled between the specified oper and lower temperature without power in an air or trogen environment. Normal temperature extremes e –65°C and +150°C with a minimum 10 minute dwell nd 5 minute transition, per MIL-STD-883, Method 1010, ondition C. This is a good test to measure the overall ackage to die mechanical compatibility.

linimum Duration: 1000 cycles.

MSK-Thermal Shock, Liquid-to-liquid

escription: Heating and cooling are done by immersing ne units in a hot and cold inert liquid. Normal temperaure extremes are –55°C to +125 with a minimum 5 inute dwell and less than a 10 second transition per IIL-STD-883, Method 1011, Condition C.

emperature: Heat transfer by conduction is much faster nan by convection, thus causing rapid temperature hanges in the part. This rapid changing in temperature reates temperature gradients across the part, which vill produce additional mechanical stress compared vith temperature cycling. This additional stress will ccelerate mechanisms such as bond cratering and wire reep.

Minimum Stress Duration: 100 cycles.

Solderability Testing

Description: This method, per MIL-STD-883, Method 2003, is designed to determine the solderability of the device leads using a standardized soldering procedure after a specified pre-conditioning (steam aging). Rejection criteria are based on physical appearance of the finished leads (porosity, pinholes, non-wetting, dewetting, foreign material, etc.)

Lead Integrity

Description: This method tests the leads of a device by bending them in a prescribed manner and rejecting the device if the specified stress results in a broken or loosened lead, or damage to the device hermeticity, per MIL-STD-883, Method 2004.

Latch-up

Description: CMOS devices contain parasitic PNPN structures which may act as SCR's, given the appropriate triggering event. The triggering event may be Gamma radiation or a voltage spike on the power bus or an input pin. Under normal operating conditions, these PNPN structures are reverse biased and quiescent. The latch-up may result in a temporary malfunction or permanent damage. Reference JESD-17 Latch-up in CMOS Integrated Circuits and Catalyst Specification #22009.

ESD Testing

ESD Specs: Catalyst ESD test standards are presented in Specification #22010. This specification includes the human body model based on MIL-STD-883, Method 3015, Electrostatic Discharge Sensitivity Classification; and the machine model.

The human body model uses a 100 pf capacitor with a 1.5 KΩ series resistor. The machine model uses a 200 pf capacitor with no resistor.

Surface Mount Package Solder Heat Preconditioning

Industry Standards: Reference JESD-22, Test Method A112 proposal.

The samples from each pin count of each applicable package family shall be subjected to the following stressing sequences:

Note: Packages containing larger die-attach pads are expected to exhibit less durability when subjected to these same sequences of environmental exposures. Therefore, within a package/pin-count family, only the largest die-pad dimensions need be tested to establish the durability of that package family.

Example: 28 pin SOIC having three different die-attach pad dimensions. Only the largest die size need to be tested to ensure the integrity of the 28 pin SOIC family.

Saturated samples: Samples which have been saturated to a given level of humidity shall be subjected to the sequence listed below. Successful completion of these sequences represents the minimum durability requirement for packages, which can be shipped without special dry-packing precautions.

Sample 1

125°C bake for 24 hours to dry the package
168 hour 85/85 no bias to saturate the package
2 60 second passes through vapor phase furnace at 217°C
Samples to DHTL, DRSL, and 85/85

Sample 2

125°C bake for 24 hours to dry the package
168 hour 85/85 no bias to saturate the package
2 60 second passes through infrared furnace at 240°C
Samples to DHTL, DRSL, and 85/85
Electrical test

Acceptable Performance: There should be NO failures from package degradation, cracks or internal corrosion.

Crack and Damage Inspection: Acoustical microscop and cross sections may be used to analyze samples f evidence of damage.

After electrical test and visual inspection, the sampl shall be exposed to DHTL, DRSL, and THBS for minimum of 1000 hours.

Acceptable performance: Devices in each stress sha meet the applicable sample plan.

Sequence for HUMIDITY-PRECONDITIONE SAMPLES (moisture content = 0.4% to 0.6%)

50 samples
Precondition this sample as follows:
Weigh a sample of 10 devices (record weight)
Bake in dry storage @ 150°C for 48 hours
Weigh the sample of 10 devices again (record weigh
Subject the sample to 85/85 (no bias) for 168 hour
Weigh a sample of 10 devices (record weight)

Acceptable Performance: There should be NO failure from package degradation, cracks or internal corrosio

Crack and Damage Inspection: Additional sequence and inspection techniques: Multiple exposures to vapo phase and infrared reflow profiles may be conducte Acoustical microscopy and cross sections may be use to analyze samples for evidence of damage.

ELIABILITY STRESS RESULTS

erial, by Design/Process Family

able 2. Serial E²PROM Reliability Data Summary (Process/Design 1.5µm CMOS)

Reliability Stress	Stress Conditions	# Lots	Device Hours	# Failures	Apparent Activation Energy	Failure Rate @ 90% C.I.	Cause
Dynamic High Temp. Operating Life (DHTL)	@ 125°C & 5.0V @ 150°C & 6.0V	7 3	430,000 198,000	0 0		0.52%/1000 Hrs 1.15%/1000 Hrs	
Summary	@ 55°C		9.90e+06		0.4 eV	234 FITs(4)	
Data Retention Storage Life (DRSL)	@ 150°C Post 100K Cycles	123	6,104,000	10		.255%/1000 Hrs	8 Oxide Rupture 2 Margin Fail
Summary	@ 55°C		7.20e+08		0.6 eV	22 FITs	
Endurance in Program/Erase Cycles (ENDR)	@ Ambient + 48 Hrs Bake @ End Point	123	9.66e+08	6		.0011%/1000 Cyc.	5 Oxide Rupture 1 Margin Fail
Summary	@ 55°C		6.30e+08		0.12 eV	17 FICs	

able 3. Serial E²PROM Reliability Data Summary (Process/Design 2.0 µm CMOS)

Reliability Stress	Stress Conditions	# Lots	Device Hours	# Failures	Apparent Activation Energy	Failure Rate @ 90% C.I.	Cause
Dynamic High Temp. Operating Life (DHTL)	@ 125°C & 5.0V	25	1,478,000	2		0.36%/1000 Hrs	Latent Oxide Defect
Summary	@ 55°C		1.78e+07		0.4 eV	296 FITs(4)	
Data Retention Storage Life (DRSL)	@ 150°C Post 100k Cycles	104	5,000,000	3		.135%/1000 Hrs	1 Oxide Rupture 2 Margin Fail
Summary	@ 55°C		5.90e+08		0.6 eV	11 FITs	
Endurance in Program/Erase Cycles (ENDR)	@ Ambient + 48 Hrs Bake @ End Point	98	8.34e+08	3		.0007%/1000cyc.	3 Oxide Rupture
Summary	@ 55°C		5.40e+08		0.12 eV	12 FICs	

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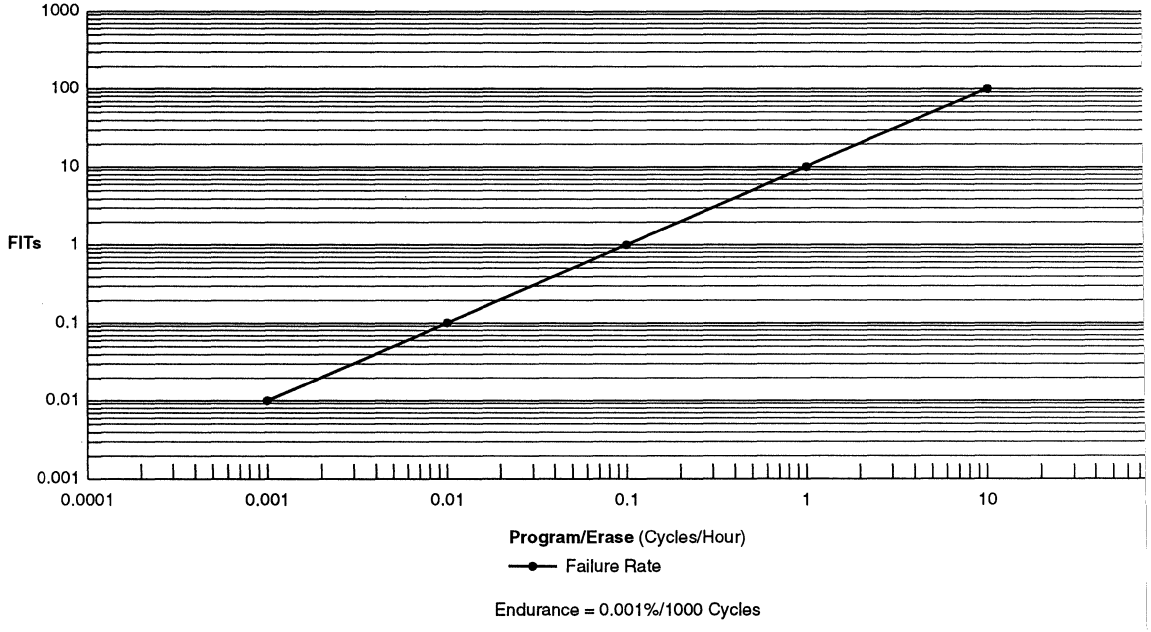
lote:
4) Failure rates are lower bounded by sample size.

Figure 2. Endurance Cycles to Time Conversion Nomograph



Parallel, by Design/Process Family

Table 4. Parallel E^2PROM Reliability Data Summary (Process/Design: 1.2 µm CMOS)

Reliability Stress	Stress Conditions	Device Hours	# Failures	Apparent Energy	Failure Rate @ 90% C.I.	Cause
Dynamic High Temp. Operating Life	@ 150°C & 6.0V 10K P/E Cycles	714,000	0		0.013%/1000hrs	
Summary	@ 55°C	1.71e+07		0.4 eV	134 FITs(4)	
Data Retention Storage Life	@ 150°C Post 10K P/E Cycles	712,000	0		0.003%/1000hrs	
Summary	@ 55°C	8.38e+07		0.6 eV	27 FITs(4)	
Endurance (Program/Erase Cycles)	@ Ambient + 168 Hrs. Bake @ End Point	4.67e+07	0		.002%/1000cyc	
Summary	@ 55°C	1.20e+08		0.12 eV	19 FICs(4)	

Note:
(4) Failure rates are lower bounded by sample size.

ach Plastic Package Family

able 5. 8 Pin Plastic SOK (EIAJ Small Outline 207 Mil)

Reliability Stress	Stress Conditions	# Lots	Failures/Timepoint			
			168hrs	500hrs	1000hrs	
Dynamic High Temperature Operating Life (DHTL)	T_A = 150°C,100K P/E V_{CC} = 6.0 V Dynamic Read	3	0/190	0/190	0/190	
	VP:215°C,60 Sec, 3x	1	0/20	0/20	0/20	
	IR:245°C,10 Sec, 3x	1	0/20	0/20	0/20	
	883/1005					
			168hrs	500hrs	1000hrs	
Data Retention Storage Life (DRSL)	T_A = 150°C Post 100K P/E Cycle Unbiased Storage 883/1008	6	0/300	0/300	0/300	
			168hrs	500hrs	1000hrs	
Temperature Humidity Bias Stressing (THBS)	T_A =85°C, R.H.=85% JEDEC22-A110/Cond.D	6	0/237	0/237	0/237	
			150CY	500CY	1000CY	
Temperature Cycles (TMCL)	–65°C to +150°C 30 Min. Per Cycle 883/1010/Cond. C	6	0/203	0/203	0/203	
			96hrs	168hrs	220hrs	332hrs
Pressure (PPOT)	T_A= 121°C P_A= 30psia R.H.= 100% JEDEC22-A102-B	6	0/204	0/204	0/204	0/204
Solderability	8 Hrs Steam Age 883/2003	6	0/30			
			3 Cyc			
Lead Fatigue	90 Deg. Bend, 250gm 3 Leads Per Device 883/2004 B2	6	0/30			
			3 Rubs			
Solvent Resistance	883/2015	6	0/30			
			15 Cyc			
Thermal Shock (Tmsk)	–55°C To +125°C 10 Min. Per Cycle	6	0/204			
			Length	Width	Thick	
Physical Dimensions		50	.2070 In	.2065 In	.0730 In	
	6 Hrs Bake @150°C		Visual	Elect.		
Solder Heat Resistance	85°C/85%Rh, 24hrs 350°C/3 Sec.Sol.Heat	1	0/34	0/34		

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Table 6. 8 Pin Plastic SOJ (JEDEC Small Outline)

Reliability Stress	Stress Conditions	# Lots	Failures/Timepoint			
			168hrs	500hrs	1000hrs	
Dynamic High Temperature Operating Life (DHTL)	T_A = 150°C,100K P/E V_{CC} = 6.0 V Dynamic Read	2	0/154	0/154	0/154	
	VP:215°C,60 Sec, 3x	2	0/60	0/60	1/60	
	IR:245°C,10 Sec, 3x	2	0/60	0/60	0/60	
	883/1005					
			168hrs	500hrs	1000hrs	
Data Retention Storage Life (DRSL)	T_A = 150°C Post 100k P/E Cycle Unbiased Storage 883/1008	4	0/200	0/200	0/200	
			24hrs	50hrs	100hrs	
Humidity/Temperature With Bias (HAST)	T_A =140°C, R.H.=85% JEDEC22-A110/Cond.D	4	0/136	0/136	0/136	
			150CY	500CY	1000CY	
Temperature Cycles (TMCL)	–65°C To +150°C 30 Min. Per Cycle 883/1010/Cond. C	4	0/136	0/136	0/136	
			96hrs	168hrs	220hrs	332hrs
Pressure Pot (PPOT)	T_A = 121°C P_A = 30psi R.H.= 100% JEDEC22-A102-B	4	0/136	0/136	0/136	0/136
Solderability	4 Hrs Steam Age Method 2003	4	0/20			
			3 Cyc.			
Lead Fatigue	90 Deg. Bend, 250gm 3 Leads Per Device 883/2004 B2	4	0/20			
			3 Rubs			
Solvent Resistance	883/2015	4	0/20			
			15 Cyc			
Thermal Shock (TMSK)	–55°C to +125°C 10 Min. Per Cycle	4	0/136			
			Length	Width	Thick	
Physical Dimensions		2	.196in	.152in	.058in	
	6 Hrs Bake @150°C		Visual	Elect.		
Solder Heat Resistance	85°C/85%Rh, 24hrs 350°C/3 Sec.Sol.Heat	1	0/33	0/33		

ıble 7. 8 Pin Plastic Dip 300 Mil

Reliability Stress	Stress Conditions	# Lots	Failures/Timepoint			
Dynamic High Temperature Operating Life (DHTL)	100k P/E Cycles T_A = 150°C,V_{CC}=6.0V Or T_A = 125°C,V_{CC}=5.0V Dynamic Read 883/1005	12	168hrs 0/1362	500hrs 0/1362	1000hrs 0/1362	
Data Retention Storage Life (DRSL)	T_A = 150°C Post 100k P/E Cycle Unbiased Storage 883/1008	12	168hrs 0/600	500hrs 0/600	1000hrs 0/600	
Humidity/Temperature With Bias (HAST)	T_A =140°C, R.H.=85% JEDEC22-A110/Cond.D	12	24hrs 0/340	50hrs 0/340		
Temperature Cycles (TMCL)	–65°C to +150°C 30 Min. Per Cycle 883/1010/Cond. C	12	150CY 0/340	500CY 0/340	1000CY 0/340	
Pressure Pot (Ppot)	T_A= 121°C PA= 30 psi R.H.= 100% JEDEC22-A102-B	12	96hrs 0/340	168hrs 0/340	220hrs 0/340	332hrs 0/340
Solderability	4 Hrs Steam Age Method 2003	12	0/60			
Lead Fatigue	90 Deg. Bend, 250gm 3 Leads Per Device 883/2004 B2	12	3 Cyc. 0/60			
Solvent Resistance	883/Method 2015	7	3 Rubs 0/35			
Thermal Shock (TMSK)	–55°C to +125°C 10 Min. Per Cycle	7	15 Cyc 0/238			
Resistance To Solder Heat	260°C/ 10 Sec	1	0/239			
Physical Dimensions		1	Length .367in	Width .251in	Thick .128in	

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Table 8. 28 Pin Plastic DIP

Reliability Stress	Stress Conditions	# Lots	Failures/Timepoint			
Dynamic High Temperature Operating Life (DHTL)	T_A = 150°C, 10K P/E V_{CC} = 6.0 V Dynamic Read VP:215°C,60 Sec, 3x IR:245°C, 10 Sec,3x 883/1005	3	168hrs	500hrs	1000hrs	2000hrs
			0/202	0/202	0/202	0/202
Data Retention Storage Life (DRSL)	T_A = 150°C Post 10K P/E Cycles Unbiased Storage 883/1008	3	168hrs	500hrs	1000hrs	2000hrs
			0/160	0/160	0/160	0/160
Humidity / Temperture With Bias (HAST)	T_A=140°C, R.H.=85% JEDEC22-A110/Cond.D	3	24hrs	50hrs	100hrs	
			0/96	0/96	0/96	
Temperature Cycles (TMCL)	–65°C to +150°C 30 Min. Per Cycle 883/1010/Cond. C	2	150CY	500CY	1000CY	
			0/30	0/30	0/30	
Pressure Pot (PPOT)	T_a = 121°C P_a = 30psi R.H. = 100% JEDEC22-A102-B	1	96hrs	168hrs	220hrs	332hrs
			0/34	0/34	0/34	0/34
Solderability	4 Hrs Steam Age Method 2003	4	0/20			
Lead Fatigue	90 Deg.Bend,250gm 3 Leads Per Device 883/2004 B2	4	3 Cyc.			
			0/20			
Solvent Resistance	883/2015	4	3 Rubs			
			0/20			
Thermal Shock (TMSK)	–55°C to +125°C 10 Min. Per Cycle	1	15 Cyc.			
			0/32			
Physical Dimensions	28 Pin PDIP	1	Length	Width	Thick	
			1.48 in	0.54 in	0.15 in	
Solder Heat Resistance	6 Hrs Bake @ 150°C 85°C/85%RH,24hrs 350°C/3 Sec.Sol.Heat	1	Visual	Elect		
			0/22	0/22		

able 9. 32 Pin PLCC

Reliability Stress	Stress Conditions	# Lots	Failures/Timepoint			
Dynamic High Temperature Operating Life (DHTL)	T_A = 150°C, 10K P/E V_{CC} = 6.0 V Dynamic Read VP:215°C,60 Sec, 3x IR:245°C, 10 Sec, 3x 883/1005	2	168hrs	500hrs	1000hrs	2000hrs
			0/155	0/155	0/155	0/155
Data Retention Storage Life (DRSL)	T_A = 150°C Post 10K P/E Cycles Unbiased Storage 883/1008	3	168hrs	500hrs	1000hrs	2000hrs
			0/196	0/196	0/196	0/196
Humidity / Temperture With Bias (HAST)	T_A=140°C, R.H.=85% JEDEC22-A110/Cond.D	1	24hrs	50hrs	100hrs	
			0/32	0/32	0/32	
Temperature Cycles (TMCL)	–65°C to +150°C 30 Min. Per Cycle 883/1010/Cond. C	1	150CY	500CY	1000CY	
			0/32	0/32	0/32	
Pressure Pot (PPOT)	T_A = 121°C P_A = 30psi R.H. = 100% JEDEC22-A102-B	2	96hrs	168hrs	220hrs	332hrs
			0/86	0/86	0/86	0/86
Solderability	4 Hrs Steam Age Method 2003	1	0/5			
Lead Fatigue	90 Deg.Bend,250gm 3 Leads Per Device 883/2004 B2	1	3 Cyc			
			0/5			
Solvent Resistance	883/2015	1	3 Rubs			
			0/5			
Thermal Shock (TMSK)	–55°C to +125°C 10 Min. Per Cycle	1	15 Cyc			
			0/32			
Physical Dimensions	32 Pin PLCC	1	Length	Width	Thick	
			0.59 in	0.49 in	0.12 in	
Solder Heat Resistance	6 Hrs Bake @ 150°C 85°C/85%RH,24hrs 350°C/3 Sec.Sol.Heat	1	Visual	Elect		
			0/32	0/32		

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Warranty Procedure

PURPOSE

To define procedures to implement Catalyst lot acceptance guarantee criteria (applicable at customer's incoming inspection) and product warranty. To define the product warranties, lot acceptance guarantees, warranty periods and Catalyst's limitation of obligation under those guarantees and warranties for all Catalyst integrated circuits and die.

SCOPE

This procedure applies to all Catalyst manufactured devices and die.

REFERENCE DOCUMENTS AND STANDARDS

Catalyst Standard Terms & Conditions of Sale.

Catalyst Returned Material Authorization Procedure.

Applicable Catalyst Data Sheets.

Applicable Customer Specifications, Contracts or Purchase Orders as accepted by a duly authorized Catalyst Representative.

DEFINITIONS AND TERMS

AOQ (Average Outgoing Quality)—The mean proportion non-conforming, often expressed in PPM, shipped by the manufacturer. JEDEC Standard No. 16 describes how to assess AOQ in PPM for microcircuits.

AOQL (Average Outgoing Quality Limit)—The maximum average proportion non-conforming shipped using a given sampling system.

LTPD (Lot Tolerant Percent Defective)—Where the consumer's risk, i.e., probability of having a bad lot accepted equals 10%. Often used as a single sampling procedure for isolated lots or reliability stress evaluation.

EQUIPMENT AND MATERIALS

Not applicable.

CALIBRATION

Not applicable.

RECORDS AND FORMS

Catalyst Return Material Authorization (RMA) Form. Catalyst Customer Failure Analysis Request (CFAR) Form.

WARRANTY PROVISIONS/SEMICONDUCTOR DEVICES

Warranty

Catalyst warrants that standard integrated circuits delivered pursuant to this procedure shall, at the time of shipment, and for a period of one year thereafter, be free from defects in material(s) and shall conform to Catalyst specifications or such specifications agreed upon by Catalyst in writing. Under this warranty, Catalyst obligations, with respect to losses, and at Catalyst's option, shall be limited to; either replacement (by delivery F.O.B., Santa Clara, CA.) or refund of the purchase price of the non-conforming product. This warranty is subject to the following conditions and procedures:

Customer Complaint. In the event a customer believes that product purchased from Catalyst is not in conformance with the Catalyst warranty for that product, the customer should notify Catalyst and, upon request from Catalyst, return a sample of the allegedly non-conforming devices. Following receipt of the sample of allegedly non-conforming devices, Catalyst will issue a CFAR number. Thereafter, failure analysis will be performed to determine whether the device is nonconforming to the applicable Catalyst specification and, if so, whether the non-conformance is covered by Catalyst warranty or whether the warranty is not applicable for some reason (e.g., the non-conformance resulted from misuse, neglect, improper installation, repair, alteration, accident or improper product handling, the warranty period has expired, the product was not purchased from Catalyst, etc.).

Warranty Determination. Final determination of warranty coverage of all returns shall be by Catalyst Semiconductor, Santa Clara, CA. Issuance of a CFAR number does not imply acceptance of any warranty obligation with respect to the returned material by Catalyst. An RMA number will be issued when Catalyst agrees that

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Note:
1) This Warranty Procedure is Catalyst Specification #31000.

material, other than the CFAR sample, should be returned. Issuance of an RMA number also does not imply acceptance of any warranty obligation, but an RMA number may be issued by Catalyst for any reason deemed by Catalyst to be appropriate.

Responsibility. Catalyst's Sales/Marketing department shall notify the customer if a warranty claim is not accepted. Should the customer return product without an authorized RMA number, the product will be returned to the customer, freight collect, or if such request is not forthcoming when requested by Catalyst, then Catalyst shall be entitled to scrap the product at Catalyst without liability to the customer.

The customer will be responsible for payment of product purchase price, and returned freight and handling costs.

If the warranty claim is accepted, after verifying non-conformance, Catalyst will replace product or refund cost, within 90 days. Warranty replacement or refund will be based on final product count at Catalyst.

Disclaimer

This express warranty shall extend only to the customer and not the customer's end user; and is in lieu of all other warranties, express or implied, including the implied warranties being specifically disclaimed by Catalyst. In no event shall Catalyst's liability for any breach or alleged breach of an order by either party exceed the total extended price or prices shown on the goods in question; Catalyst shall not be liable for any special, incidental or consequential damages resulting from such breach or alleged breach. Furthermore, Catalyst shall, in no event, be obligated for any cost incidental to the replacement of non-conforming products.

Commercial Incoming Inspection

Incoming inspection, if any, must be completed by th customer within the warranty period. Product not r jected as a result of incoming inspection and notic thereof given to Catalyst on or before the expiration the warranty period shall be conclusively deemed a cepted. If the customers's incoming inspection is base on lot acceptance sampling, then the following establis the agreed upon sample plan levels. Any lot failing meet the sample plan is eligible for return to Catalys provided an RMA is obtained.

Data Sheets/Control Specifications

Catalyst data sheets are controlled specifications app cable to product at the time of shipment. Catalyst r serves the right to revise published data sheets and/ make changes in the product. Catalyst assumes r responsibility for the use of any circuits described published data sheets, and conveys no license und any patent. Applications for any integrated circuits co tained in publications are for illustration purposes onl and Catalyst makes no representation or warranty th such applications will be suitable for the use specifie

Third Party Warranty Restrictions

Unless previously reviewed and accepted in writing by duly authorized Catalyst representative, environment screening or testing, or failure analysis of products b the customer or a third party laboratory voids the wa ranty of those devices.

Unsalable or Untestable Product

Returned product received in an unsalable or untestab condition, or such condition that verification of the re ported discrepancy is impractical or impossible, voic the warranty.

Table 1. Lot Acceptance Guarantee Criteria for Commercial Standard Integrated Circuits

Condition	Reference	Sample Plan
Timing, parametric and functional functional electrical, cumulative across temperature	Data Sheet	1% AOQL
Mechanical/Visual	Ext. Vis. Spec	1% AOQL
Endurance/Data Retention	Coml End/DR Spec	1% AOQL
One-time Programmability	Data Sheet	2.5% AOQL

ritical Components/Life Support Systems

atalyst products are not authorized for use as critical omponents in Life Support Devices or Systems. If any uch use is intended then provision must be made in a eparate agreement, signed by the President and Vice resident of Quality & Reliability of Catalyst, which will rovide for special terms and provisions relating to sting required because of the nature of such use.

critical component is defined as any component whose ilure to perform an intended function, could possibly ad to loss of life or bodily harm.

ife Support Systems that may include critical compoents, are defined as, but not necessarily limited to:

(1) Surgical implants in a human body,

(2) Equipment used to sustain human life, or

(3) Equipment used to monitor and/or measure human body conditions.

lilitary Incoming Inspection

ncoming inspection, if any, must be completed by the ustomer within the warranty period. Product not rected as a result of incoming inspection and notice ereof given to Catalyst on or before the expiration of e warranty period shall be conclusively deemed accepted. If the customers's incoming inspection is based n lot acceptance sampling, then the following establish e agreed upon sample plan levels. Any lot failing to eet the sample plan is eligible for return to Catalyst, rovided an RMA is obtained.

lanufactured Devices

lilitary devices are manufactured in accordance with e applicable detail specification, (i.e., Catalyst compli- nt device specification for MIL-STD-883 compliant levices, or the Standardized Military Drawing) as acnowledged and accepted by Catalyst in the customer's urchase order.

DIE WARRANTY POLICY

Warranty Limitations

The warranty on die is limited to 90 days from the date of shipment.

Die lots will, at incoming inspection, meet the visual requirements of Catalyst Second Optical Inspection Criteria of MIL-STD-883, Method 2010 Condition B, to a 1% AOQL sample plan.

Die lots not rejected as a result of incoming inspection and notice thereof given to Catalyst on or before the expiration of the warranty period shall be conclusively deemed accepted. Any lot failing to meet the sample plan is eligible for return to Catalyst, provided an RMA is obtained.

The warranty on die is not applicable to die that receive any additional electrical, mechanical or environmental testing, processing or other handling by the customer or a third party.

Catalyst does not grant reliability approval on die because of additional assembly and test processing required when die are integrated into the customer's product where testing and assembly is performed by, or contracted out by the customer, unless it is expressly defined in a customer specification, and accepted in writing by a duly authorized Catalyst representative.

NON-STANDARD PRODUCT

Development

Any product designated for "developmental" or "experimental use" is sold "as is" with no warranty whatsoever except the warranty of title; the implied warranties of fitness for a particular purpose and merchantability are expressly disclaimed. The customer shall indemnify Catalyst from any claim that the product infringes upon in any United States patent, copyright or mask work right.

able 2. Lot Acceptance Criteria for Military Microcircuits

Condition	Reference	Sample Plan
Group A Electrical	Applicable Detail Specification	LTPD 2/0
Mechanical/Visual	MIL-STD-883, Method 2009	1% AOQL
Hermeticity	MIL-STD-883, Method 1014	1% AOQL
Endurance/Data Retention	Applicable Detail Specification	LTPD 5/1 (1% AOQL)

Development product shall be marked with the standard Catalyst marking plus block letters ES instead of the date code.

Pre-Production

Pre-production product is lot guaranteed per paragraph Commercial Incoming Inspection to electrical parameters of the preliminary data sheet or errata sheet specifications only. Reliability testing is in progress, but no reliability approvals are offered to the customer.

Pre-production product shall be marked with the standard Catalyst marking and an MS instead of the date code.

Custom Products

Custom products are manufactured to meet non-standard requirements as specified in a customer's specification,which is accepted in writing by Catalyst.

Any lot failing the specified sample plan and/or failing a customer's screen to a specified test criteria, an agreed to in writing by a duly authorized Catalyst representative is eligible for return to Catalyst in accordance with return provisions.

WARRANTY POLICY FOR DISTRIBUTORS

Products shipped by distributors are subject to a one year warranty by Catalyst from the date of first shipment from the distributor. This warranty by Catalyst expires if the distributor does not ship product within two years from data of shipment from Catalyst.

Distributor returns will be honored only if an RMA form or RMA number is issued by a duly authorized Catalyst representative within the applicable warranty period.

Where distributors remark product, the Catalyst symbol and date code shall not be altered. A record of any remarking operation must accompany material returned to enable traceability to the original shipment.

All distributor returns for stock rotation, obsolete product or other policy reasons must be received with an RMA form or RMA number issued by the responsible Catalyst sales representative.

Distributors must return devices, in accordance with the Return Provisions within 30 days of the issuance of an RMA form or RMA number, otherwise returned devices will not be honored for credit or replacement.

RETURN PROVISIONS

Condition of Received Returned Materials

Returned material must be packed in a manner t prevent damage to the device(s) (electrical or mechar cal) under normal commercial carrier handling conc tions. Products received in a damaged condition due t improper packing for shipment by the customer are th customer's responsibility.

All products, manufactured by Catalyst, must be r turned in containers that prevent static damage. Failur to provide static handling protection, or material four damaged as the result of user negligence, are th responsibility of the customer.

Rework Costs

In the event the customer unilaterally elects to rewo material which fails customer incoming inspection, th cost and liability of such rework shall be the sole respor sibility of the customer. Rework of material by th customer shall nullify the Catalyst warranty.

When a customer requests authorization and rein bursement for rework costs, prior written approval sha be obtained from Catalyst Marketing and the Q & R Vic President before the customer rework commences.

RETURNS METHODOLOGY:

Refer to Catalyst's Returned Material Authorizatio (RMA) Procedure for instructions on completion of th Returned Material Authorization Form and instructior on material return.

DISQUALIFICATION OF CATALYST PRODUCT BY PURCHASER

In the event that the customer determines incomin Catalyst product to be unacceptable and establishe that the product is disqualified, the responsible salespe son must communicate specifically if the return is fc nonconformance to agreed specifications or being re turned for other reasons.

Other reasons for disqualification may include:

(A) Unapproved vendor.

(B) Disqualification for repeated delinquencies by Catalyst.

(C) Non-performance in the customer's system, although the product meets Catalyst's electrica specifications.

If the customer purchases products for production pric to completion of his own qualification tests, such proc ucts cannot be classified as "disqualified".

Reliability Considerations for E²PROMs

When acquiring a microcircuit, many considerations above and beyond the purchase price are important. Among these are quality, reliability, delivery, service and product assurance. The lowest cost of ownership for the user is a result of the proper balance and specification of the above considerations. E²PROMs contain reliability considerations that can significantly affect the cost of ownership if the E²PROM is incorrectly used in the application.

For E²PROMs, whether serial, parallel, flash or other, reliability is the summation of the factors of operating life (read), data retention and endurance.

E²PROM Device Failure Rate

$F.R._{DEVICE} = F.R._{READ} + F.R._{ENDURANCE} + F.R._{RETENTION}$

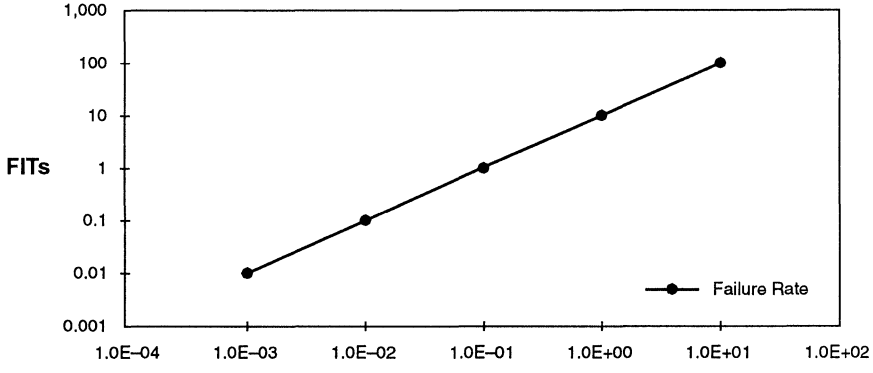
F.R. = FAILURE RATE

Read, Endurance, and Retention mechanisms are thermally accelerated; therefore, failure rates must be stated with temperature, confidence interval, and apparent activation energy.

Endurance is the most important because the endurance reliability is a direct function of the application, i.e., the number of times the device is rewritten during system operation. In other words, the total system life can be compromised by the endurance capability of the E²PROM. (Figure 1). For applications not requiring many rewrites or that must have byte clear, e.g., program storage, flash E²PROMs provide the best combination of cost and reliability. For applications requiring many rewrites, e.g., data storage or configuration, parallel E²PROMs provide the best combination. For applications requiring direct access to the controller, e.g., traceability, and lowest cost per device, serial E²PROMs are appropriate. Quality, delivery, service and product assurance are identical for all Catalyst E²PROMs.

Endurance is defined as: "The measure of the ability of a nonvolatile memory device to meet its data sheet specifications as a function of accumulated nonvolatile data changes," per IEEE "Standard Definitions and Characterization of Floating Gate Semiconductor Arrays." The data sheet specifications include write functionality, data retention and read access time. For a Catalyst E²PROM, a nonvolatile data change is the completion of a program/erase cycle for each byte, i.e., transferring charge to and from the floating gate in the memory storage transistor.

Figure 1. Endurance Cycles to Time Conversion Nomograph



Endurance = .001%/1000 cycles

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Endurance has two primary failure mechanisms (Figure 2) which can result in any of three failure modes, i.e., data retention degradation, access time degradation or loss of write functionality. The charge is transferred on and off the floating gate through an oxide, resulting in the failure mechanisms of oxide damage and charge trapping. These mechanisms are caused by the cumulative effects of passing a current through a nominal insulator and placing a high electric field across an oxide. Thicker oxides have a greater likelihood of measurable charge trapping. Thinner oxides require greater care in processing to reduce initial oxide defects, which cause yield loss. Endurance cycling over the lifetime of the system will cause random oxide damage and charge trapping at some constant low level. Design and processing must be such to minimize initial defects and reduce generated defects to the lowest possible level.

When a high number of endurance cycles before the onset of wearout is desired, error correction is suitable for oxide damage induced failures. Catalyst uses a byte error correction method to achieve extended endurance for high density parallel E²PROMs, e.g., the CAT28C256. Error correction is unnecessary for flash E²PROMs, which have a lower total number of endurance cycles specification or serial E²PROMs of low density. Err correction is not practical for charge trapping induc failures. A low failure rate during the useful life region achieved by proper design, processing, and screenin

Endurance follows the "bathtub" curve, with a knov infant mortality region, a useful life region, and a predic able wearout region. Endurance cycling has historica been the preferred method for screening and for perioc qualification testing. Cycling can be performed in re time and is the actual operating mode of the device.

Although intrinsic data retention is essentially infinit the extrinsic data retention is a function of enduranc The endurance failure rate contains the extrinsic da retention failure rate induced by endurance. The intrins data retention failure fate is reported independent endurance.

Test Method 1033 of MIL-STD-883 (Figure 3) describe the procedures to be used when performing enduranc cycling for screening or endurance performance veri cation. Various means exist to eliminate infant mortalit which will be a function of product design and th dominant failure mechanism of the process. For e ample, floating gate devices usually contain an infa

Figure 2. Endurance Failure Definition

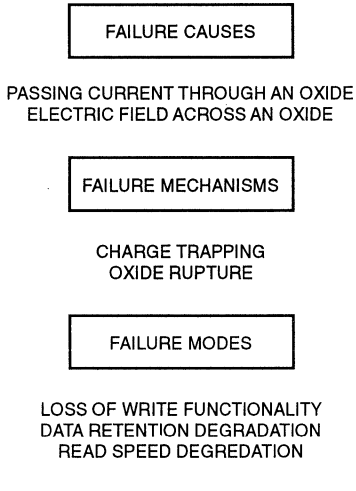

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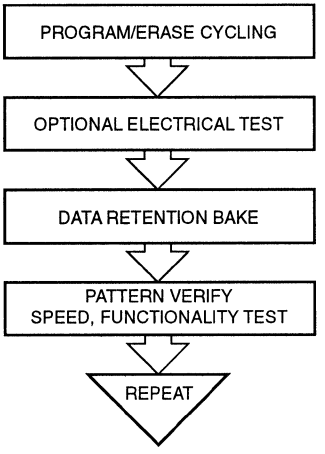
Figure 3. Endurance Testing Procedure MIL-STD-883, Method 1033



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ıortality data retention unbiased bake screen. Normal ɜliability monitoring on E²PROMs verifies operating life, ata retention and endurance.

andom defects, occurring naturally in the wafer fabri- ation process, will cause infant mortality endurance or ata retention failures. In neither case is there an explicit ɜlationship that correlates infant mortality with device erformance in the useful life or wearout regions. To nprove yields, redundant memory in the device is used) repair initial or infant mortality failures in large or ɔmplex memory arrays. Due to the localized nature of ıe random defects that cause initial or infant mortality ıilures, the reliability of repaired and non-repaired de- ices is equivalent.

The endurance failure rate of the E²PROMs in a system will increase in importance as a function of the number of times the system rewrites the E²PROM during system life. System reliability is a function of the failure rate in the specified useful life region of the device, not when the onset of wearout occurs. Given the operating life failure rate of an MOS memory is in the order of 100 FITs (.01%/ 1000 hours), the endurance failure rate contribution should be an order of magnitude or more lower, (Figure 1). Catalyst serial, parallel and flash E²PROMs will meet system reliability requirements by providing the lowest endurance and total device failure rate for the specified system lifetime. The greater system reliability lowers the cost of ownership of a Catalyst E²PROM.

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E²PROM Reliability: On-Chip Error Code Correction for E²PROMs

INTRODUCTION

E²PROMs are reprogrammable nonvolatile rewritable semiconductor memories suitable for applications requiring in system periodic writing of new data. A write cycle requires standard TTL (transistor-transistor logic) levels available from the system 5 volt power supply. E²PROMs have electrical timing and parametric characteristics similar to other CMOS memories.

In addition to the read failure rate, the reliability of the E²PROM is a function of the data retention and endurance failure rates. The read failure rate is less than the read failure rate of comparable density volatile memories and intrinsic data retention is essentially infinite, i.e., hundreds to thousands of years. Endurance is the failure rate component that varies across technology and manufacturer.

Endurance, defined as the number of program/erase cycles before failure of any data sheet parameter, is limited by the mechanisms which transfer charge within the device. For a given design and technology, the E²PROM will have a predictable endurance failure rate and a finite limit to the useful life region (i.e., measurable onset of wearout). Thus, the reliability of the system is a function of the endurance capability of the E²PROM.

In order to enhance endurance for high reliability applications, E²PROM on-chip ECC (Error Code Correction) can be used. The benefits and constraints of the ECC method used for the CAT28C256 will be discussed.

FAILURE MECHANISMS

Various works have demonstrated that intrinsic E²PROM memory transistor endurance is limited by the build-up of negative charge in the tunnel dielectric and the time to breakdown of the tunnel dielectric. The initial fabricated level of defects, the tunnel dielectric composition and structure, and memory circuit design will affect the generation rate of failing memory transistors during clear/write cycling. The endurance of the floating gate memory transistor follows the classic bathtub curve, with infant mortality, useful life, and wearout regions. The ability of ECC to improve endurance can be predicted during the useful life region when the memory transistor failure rate is constant.

The charge trapping and/or oxide damage mechanisms will eventually cause loss of functionality of the memory transistor, degradation in read access time, or extrinsic data retention degradation. These effects will occur randomly during the useful life of the E²PROM, prior to the onset of wearout. The failures (i.e., bit errors) are correctable by ECC. ECC will also correct normal MOS failures that affect the memory transistor.

Peripheral failures caused by endurance cycling are not correctable by on-chip ECC. Examples include failure in the charge pump, an address decoder, or output buffer. Test method 1033 of MIL-STD-883 provides the framework for establishing and verifying the endurance characteristics of E²PROMs, with or without ECC.

ERROR CORRECTION CODES

ECC is implemented using an element of length n consisting of k data bits and p check bits. When the element is accessed during a read cycle, the data and check bits are compared through an algorithm (ECC tree) to determine if an error exists and then to correct the error. Catalyst uses a modified Hamming code scheme to correct a single memory transistor error per byte.

The CAT28C256 memory element is a byte which consists of n = 12 bits, with k = 8 data bits and p = 4 check bits. During a read access all 12 bits are sensed and latched. The latched data is decoded to correct any single-bit error to provide to the 8 bit output byte. Similar circuitry is used to generate the check bits during write. The 8 bits of data in the input byte are latched and the 4 check bits are generated. The total of 12 bits per byte are loaded into registers for transfer to the memory transistors during the write cycle.

ECC MODEL

The ECC model calculates the probability of a device exhibiting no errors after some number of endurance caused memory transistor errors. Although, there may be some initial errors after manufacturing screening, these are usually replaced with redundancy; thus, at the beginning of the user's system life the device has no memory transistor errors. The purpose of ECC is to improve reliability, not manufacturing yield.

The device contains a number of ECC elements as a function of the device density, organization, and ECC scheme. All single bit errors within each memory element (byte) are correctable, regardless if the error occurs in the data or the check bits. An element with 2 or more errors is not correctable. If a memory element should have 2 or more memory transistor errors, the byte could read up to 8 bit errors. This requires that any *system* error detection and/or correction scheme not use the E²PROM byte as the basic element for ECC.

Given that:

B = number of bytes (ECC elements) in a device
n = number of bits in an ECC element (data + check)
c = number of endurance (program/erase) cycles
τ = constant memory transistor failure rate

The device hazard rate in %/1000 cycles is approximated by:

$$h(c) = n \times (n-1) \times B \times c \times \tau^2$$

The cumulative per cent failed is approximated by:

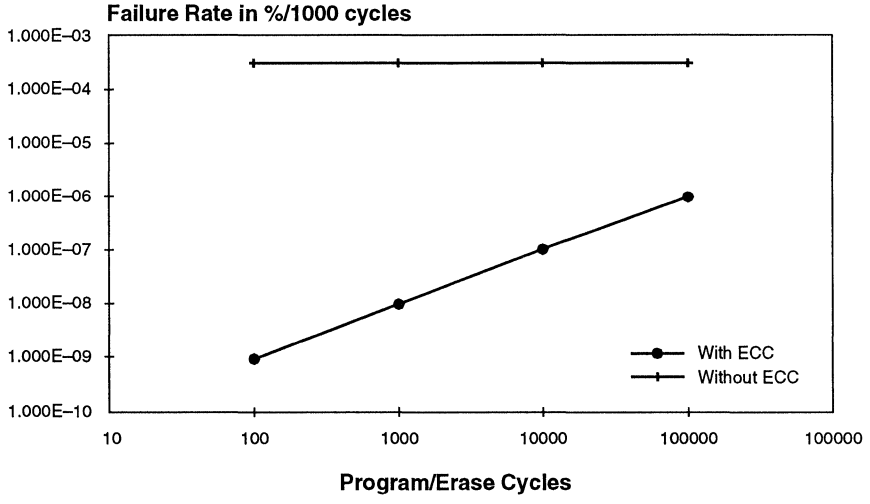
$$H(c) = (1/2) \times n \times (n-1) \times B \times (\tau \times c)^2$$

For Catalyst, the appropriate values are:

B = 32K = 32 x 1024 = 32768
n = 12
$\tau \approx 1.4 \times 10^{-7}$ %/1000 cycles

Figures 1 and 2 show the predicted memory array failure rates and cumulative per cent failures for a CAT28C256 E²PROM with and without ECC, as a function of program/erase cycles. The historical Catalyst memory transistor failure rate is lower than what has been reported by others, thus a Catalyst device with or without ECC has superior endurance reliability.

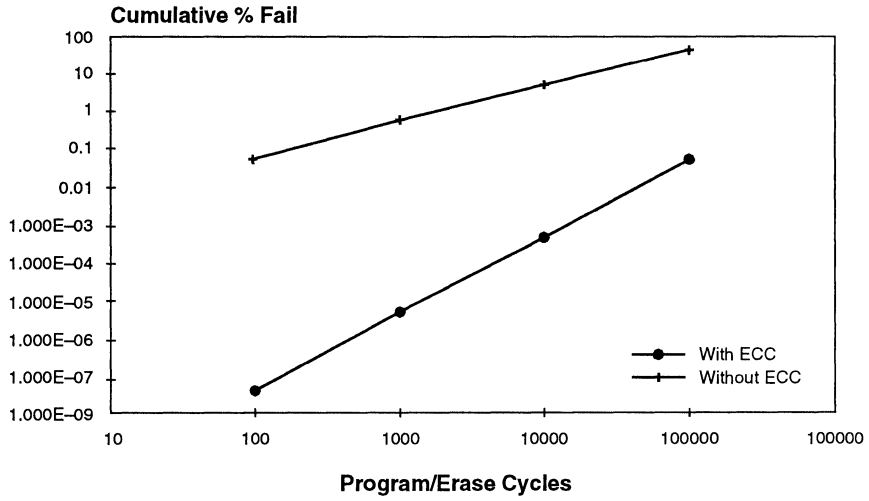
Figure 1. Predicted CAT28C256 Endurance Rate With and Without ECC



Constant transistor failure rate of 1.4E–7 %/1000 cycles

5207 FHD F

igure 2. Predicted CAT28C256 Cumulative Endurance With and Without ECC



Constant transistor failure rate of 1.4E–7 %/1000 cycles

5207 FHD F02

13

Procurement Considerations for Reprogrammable Nonvolatile Microcircuit Memories

OVERVIEW

When procuring a microcircuit, many considerations are important. These may be divided into two categories: administrative and technical. Administrative issues, such as price, delivery, service and product assurance are not topics for discussion herein. Technical issues, such as performance, quality, and reliability will be addressed.

The performance of a microcircuit is evaluated on parameters specified in a data sheet. Quality is a measure of conformance to specification, typically expressed in PPM (Parts Per Million) nonconforming. Quality levels, as maximum PPM lot acceptance guarantees, are usually provided in manufacturers' warranty policies. Reliability is an expectation of quality over time, typically expressed as a failure rate in %/1000 hours or FITs (Failures In Time), or as an MTBF (Mean Time Between Failure). Reliability expectations are usually provided in manufacturers' reliability reports for device or process families.

Reprogrammable nonvolatile semiconductor memories have performance values, data sheets, and quality levels similar to other microcircuits. Reliability expectations are complicated by considerations of endurance and data retention, which have failure mode characteristics not applicable to other microcircuits. Thus, nonvolatile memories have additional procurement considerations that will affect manufacturing methods, data sheet specifications, quality levels and reliability.

The following sections discuss the elements necessary for a complete data sheet, critical parameters for evaluating the quality of a device and a reliability evaluation methodology.

COMMERCIAL SPECIFICATION PRACTICES

DATA SHEETS

Microcircuit electrical performance is specified by a data sheet. Data sheets may be very simple expressions of "nominal" performance levels or extensive listing of minimum and/or maximum performance levels under all allowed conditions. The magnitude of testing by the manufacturer usually correlates with the stringency of the specification. The most thorough and detailed device specifications are military (MIL-M-38510) slash sheets.

The device data sheet contains a description of how the device performs its intended function, e.g., how to write and to read from a memory; and a list of parameters with performance limits and conditions that define and specify how each function is implemented. Testing is utilized to validate the circuit performs as specified. Data sheet limits and values are based on considerations of device performance, system requirements and test capability. The ability to test parameter performance is critical in understanding various data sheet limits and values.

Device performance will predictably change as a function of environmental parameters. For example, with MOS devices, speed will be slower at high temperatures and power supply current will be higher at low temperatures. Therefore, the environment is specified. Device testing is performed at worst case conditions by the manufacturer to assure the user of device conformance to the data sheet under all allowable conditions. The power supply level directly affects the performance to the device; a lower value is worst case for most parameters because of the poorer conductivity of the MOS transistor. This is most evident for access times, which are generally slower at low V_{CC}.

Temperature is typically specified as: commercial 0 to 70 °C; industrial –40 to +85 °C; or military –55 to +125 °C, reflecting the severity of the expected application. Commercial and industrial temperatures are ambient temperatures; therefore, the junction temperature of an operating device will be higher than the ambient and the device must be tested at other than the specified limits. The test temperature can be calculated as a function of the specified temperature, the device power dissipation at the temperature limit, and the thermal resistance of the package. Military temperatures are case temperatures; therefore, the junction temperature will be the same as the case test temperature, e.g., the test temperature and the specified case temperature are the same, excluding guardbands. Ambient humidity is a test concern because at low temperatures condensation can freeze up in the equipment or cause leakage paths.

MOS devices are typically specified with ± 10% power supplies; however, both extremes need not be tested for all parameters. A worst case power supply condition, based on characterization, can be stipulated for most parameters. That is the only condition that should be tested in production.

MOS nonvolatile memory test parameters fall into three categories: AC or timing, DC or parametric, and functional. AC parameters are the maximum or minimum timing conditions needed for the device to function, e.g., address set-up times, data hold times; as well as the minimum/maximum responses from the device, e.g., access times. DC parameters are the static levels on each pin in the various operational modes, e.g., power supply current, input levels, output leakage. Functional includes those timing and static conditions, i.e., AC and DC parameters, necessary for the device to function in a given mode, e.g., read or write. The conditions, under which each parameter is specified, are usually included in the data sheet and should reflect how the device is tested.

Conventions for measuring parameters should be clearly stated, as device performance can change significantly for apparently minor differences in measuring methods. The most critical reference points are for AC or timing measurements. Timing limits are minimum and/or maximum timing values for each parameter. Input requirements for the device are specified from the external system point of view, i.e., what the system must provide to the device. Responses from the device are specified from the device point of view, i.e., what the device provides to the system. Timing edge reference points are required to differentiate between the input pulse levels or output levels and their respective (as recognized by the device) valid reference points. Edge reference points must be specified relative to where the device recognizes a valid signal level. Actual test specification edge reference points will generally indicate those points that the tester recognizes as the beginning of a transition for timing measurement, not where the device recognizes a valid signal. The difference provides a built-in guardband between test conditions and actual performance requirements. The levels specified for DC or static performance may not be the same levels specified for AC or timing performance.

Integral to the testing of an integrated circuit is the test philosophy utilized to determine which parameters are tested and in what manner. Included in the philosophy will be guardbanding methodologies, interface hardware design rules, test routine algorithms and characterization requirements.

Guardbanding is the off-setting of a parameter, condition, or attribute acceptance level from the specified value. This is done to account for variability in equipme and device performance or to make test programs mo efficient and effective. Machine guardbands, impl mented in the forcing, measured or external condition are required to account for the accuracy and precisi capabilities of testers, interface hardware and handle Device guardbands are implemented where device pe formance greatly exceeds the parameter limit; thus, early warning of a change in performance is availabl Test program guardbands are implemented to speed device testing, where worst case conditions can applied based on predictable device behavior, e.g., f pattern sensitivities.

Parameter conformance to specification can be me sured in a variety of ways. In variate testing, which usually only used for characterization, the actual val of the parameter is determined. For DC parameters, th is relatively simple because the measurement is effe tively the output of a voltmeter or ammeter. For A parameters, this can be very complex, depending on t timing signal measured, because a narrow strobe mu be continuously repositioned until the desired transiti is detected or the reference edge must be continuous repositioned until the desired output is obtained. Varia testing, whether on an automated tester or a ben setup, is used primarily to validate the design a performance models for initial device release or aft design changes.

Attribute testing is the comparison of a measured p rameter under given conditions to a specified limit. T tested parameter then either passes or fails—go/no g Some parameters are directly compared with the lim while others must be "tested by inference" or "tested b the application of specified signals and condition Tested by inference is the validation of the performan of a parameter by the measurement of the corre performance of a correlated parameter or functio *Tested by inference* also applies when testing a wor case condition; therefore, all other conditions need n be tested. *Tested by the application of specified signa and conditions* is the applying of input parameters their specified minimum or maximum and measuring t correct performance of a dependent parameter or fun tion. Parameters that are outputs from the device a compared with standards or measured. Inputs to t device are tested by inference or application of specifi signals and conditions.

Data sheets usually reference mechanical specific tions for the packages containing the microcircuits. Mo packages conform with either JEDEC Publication 95 MIL-STD-1835. Otherwise, the manufacturer shou have a similar specification providing all dimension and material requirements. Visual and mechanical pe formance criteria per applicable specification are usual

spected for by the manufacturer before shipment of e devices. Dimensions, such as package thickness id lead spacing, may be critical for automatic insertion quipment operation. Composition, such as lead finish, ay be critical for solderabilty. Explicit methodology for alidating mechanical and visual performance is coned in MIL-STD-883, which is generally used as the aseline for all mechanical or visual inspection criteria.

ELIABILITY PARAMETERS

eliability evaluation may be divided into two catego-es: mechanical and electrical. Nonvolatile semicon-uctor memories are assembled in packages using milar materials and processes as other microcircuits; ius, the mechanical reliability is the same. Mechanical eliability evaluations typically use JEDEC Standard 22 r MIL-STD-883 for test methods.

lectrical reliability for nonvolatile semiconductor memoes is different from reliability for other microcircuits ecause reprogrammable nonvolatile memory reliability the summation of the factors of operating life (read), ata retention and endurance.

$$F.R._{device} = F.R._{read} + F.R._{endurance} + F.R._{data\ retention}$$

F.R. = Failure Rate

he read, endurance and data retention failure rates are ermally accelerated; therefore, must be given stating e temperature, confidence interval and apparent actiation energy or alternative deacceleration technique.

ndurance is the most important because the endurnce reliability is a direct function of the application, i.e., he number of times the device is rewritten during ystem operation. In other words, the total system life an be compromised by the endurance capability of the E^2PROM. Floating gate devices have a known endurnce wearout mechanism, which is not a factor in normal peration, but can affect system performance if the pecified number of endurance cycles is greatly exceeded.

Endurance is defined as: "The measure of the ability of a nonvolatile memory device to meet its data sheet specifications as a function of accumulated nonvolatile data changes", per IEEE STD-1005-1991 "Standard Definitions and Characterization of Floating Gate Semiconductor Arrays". The data sheet specifications include write functionality, data retention, and read access time. Typically, a nonvolatile data change is the completion of a program/erase cycle for each byte, i.e., transferring charge to and from the storage node in the memory transistor.

Endurance has two primary failure mechanisms, charge trapping or oxide damage, which can result in any of three failure modes, data retention degradation, access time degradation, or loss of write functionality. The charge is transferred to and from the storage node through an oxide, resulting in the failure mechanisms of oxide damage and charge trapping. These are caused by the cumulative effects of passing a current through a nominal insulator and placing a high electric field across an oxide. Thicker oxides have a greater likelihood of measurable charge trapping. Thinner oxides require greater care in processing to reduce initial oxide defects, which cause yield loss. Endurance cycling over the lifetime of the system will cause random oxide damage and charge trapping at some constant low level. Design and processing by the manufacturer must be such to minimize initial defects and reduce generated defects to the lowest possible level. Stressing and testing must be performed to separate devices with various levels of endurance performance.

When a high number of endurance cycles or a very low endurance cycle failure rate is desired, error correction is suitable for oxide damage induced failures. Bit or byte error correction methods are used to extend the endurance of devices whose dominant failure mode is oxide damage in the storage node. Error correction is not practical for uniform charge trapping induced failures. However, a low failure rate during the stipulated useful life region may be achieved by proper design, processing and screening.

Endurance follows the "bathtub" curve, with an infant mortality region governed by defects, a useful life region governed by the intrinsic integrity of the design and process, and a predictable wearout region governed by the cumulative effects of transferring charge through an oxide. Infant mortality is eliminated by the manufacturer during screening and testing. The useful life region failure rate level is assessed by way of product monitors. The onset of wearout is determined by extended endurance cycling, including stressing devices past the initial failure. Endurance cycling as a periodic qualification test has historically been considered the preferred means of verifying capability because cycling can be performed in real time and is the actual operating mode of the device.

Data retention has infant mortality, which must be screened in the manufacturing flow. There is a useful life region that is governed by the intrinsic integrity of the design and process. Wearout does not occur (in the sense that permanent, nonreversable degradation is present) because the storage node may be refreshed. Intrinsic data retention, the time the storage node is capable of retaining charge independent of the application, may vary by device design and process technology, but is essentially very long compared with real world operating conditions. The extrinsic data retention is a

function of endurance. Endurance failure rate expectations should contain the extrinsic data retention failure rate induced by endurance. The intrinsic data retention failure rate should be considered independent of endurance.

Test Method 1033 of MIL-STD-883 describes the procedures to be used when performing endurance cycling for screening or endurance performance verification. Various means exist to eliminate infant mortality, which will be a function of product design and the dominant failure mechanism of the process. For example, some devices use endurance cycling and others use a margin test to screen out infant mortality. Most device manufacturing flows contain an infant mortality data retention unbiased bake screen. Military requirements contain a periodic Quality Conformance Inspection (QCI) which must be performed on JAN, SMD, or 883 compliant E^2PROMs to verify operating life, data retention and endurance. A similar requirement could be added for other reprogrammable nonvolatile devices.

Random defects, occurring naturally in the wafer fabrication process, will cause infant mortality endurance or data retention failures. In neither case is there an explicit relationship that correlates infant mortality with device performance in the useful life or wearout regions. To improve yields, manufacturers may include redundant memory in the device, used to repair initial or infant mortality failures. For large and complex memory arrays, e.g., RAMs, EPROMs, or E^2PROMs, few devices are shipped that do not include some level of redundancy repair. Due to the localized nature of the random defects that cause initial or infant mortality failures, the reliability of repaired and non-repaired devices is equivalent.

The endurance failure rate of the reprogrammable nonvolatile memories in a system will increase in importance as a function of the number of times the system rewrites the memory during system life. System reliability is a function of the failure rate in the specified useful life region of the device, not when the onset of wearout occurs. Given the operating life failure rate of an MOS memory is in the order of 100 FITs (.01%/1000 hours), the endurance and intrinsic data retention failure rate contributions should be an order of magnitude or more lower.

WARRANTY POLICIES

All microcircuit manufacturers provide warranty policies. These documents are typically broken into three categories: the warranty, the guarantee and the applicable conditions.

The warranty typically states that any nonconforming device may be returned to the manufacturer for credit or replacement. Conformance is to the data sheet or othe applicable specification and is usually for a term of on year from date of shipment.

The guaranty is for lot acceptance and typically state that any lot that fails the lot acceptance sampling pla per the applicable specification may be returned to th manufacturer for credit or replacement, within one yea from shipment.

The warranty policy will define those conditions unde which devices may be returned, including administrativ and technical requirements. Administrative requirement define the logistics and methodology of documentin and returning the affected devices, e.g., so that cred may be applied to the correct order. Technical require ments include: defining the condition of returned de vices, e.g., must be testable, and the amount of correla tion needed to validate nonconformance.

Lot acceptance guaranties, specified per the applicabl lot acceptance sampling plan, will define guarantee quality levels. Typically the quality level applies to a data sheet electrical parameters and the applicabl mechanical/visual requirements but does not apply t reliability expectations. Parameters such as data reten tion and endurance, which although reliability expecta tions, can be treated as quality parameters; thus, ofte have a quality level or lot acceptance guaranty.

Quality levels, measured in PPM nonconforming, are estimates of the AOQ (Average Outgoing Quality) of the manufacturers' production line, post all screening, test ing and sampling. JEDEC Standard 16 defines how t assess AOQ in PPM for microcircuit manufacturing Transformation of AQL (Acceptable Quality Level) o LTPD (Lot Tolerant Percent Defective) sampling plans and lot guaranty levels to AOQ values are treated in standard texts on acceptance sampling.

The warranty policy should contain a definition and statement of guaranty for endurance and data retention. An example:

Endurance is the measure of the ability of a reprogrammable nonvolatile memory device to meet its data sheet specifications as a function of accumulated program/erase cycles. A program/erase cycle is the act of changing data from original (e.g., erased) to opposite (e.g., programmed) back to original for all bits of the memory array.

The memory shall be capable of the specified number of program/erase cycles per specified memory element, e.g., byte sector, page, independent of the programming or erase method, e.g., byte, page, sector, chip.

Data retention is the measure of the integrity of the stored data as a function of time. Data retention time is

e time from data storage to the time at which a peatable data error is detected.

ıe device shall be capable of the specified number of ars of data retention. This applies across the operat- g temperature range and after the specified minimum ımber of endurance cycles.

ıe memory has a lot acceptance guaranty of a 1% DQL (LTPD 5/1) for the specified number of endurance cles and data retention years, as verified by the ecified test methodology (see the Verification section Qualification Testing).

RITICAL DEVICE PARAMETERS

LECTRICAL

ll electrical parameters are important for the correct nctioning of the device in the application; however, a w tend to be more visible because they are the ırameters that most often appear to fail.

ritical DC parameters are input/output leakage and ɔwer supply currents. High input/output leakage levels, pically caused by ESD (Electro-Static Discharge) or OS (Electrical Over-Stress) will cause non-functional- / by address lines, control pins or outputs being unable) go to correct levels. High power supply currents, either ctive or standby, typically caused by EOS, may over- ıad supply lines and damage other components.

ritical AC parameters are access timing values and ıput/output level conditions. Access times are sensitive) data and address patterns; if the device is inad- quately tested by the manufacturers, i.e., not using /orst case data and address patterns, the device may ccasionally read incorrectly in the application. Input/ utput level test conditions differ widely from device to evice and manufacturer to manufacturer. Timing val- es are extremely sensitive to the applied input/output evels; thus, devices with supposedly the same timing alue may function differently in the application because f different levels used during manufacturer's testing.

ıll parameters should be controlled by the manufacturer's ıternal documentation for how they are tested. Some ıarameters, e.g., capacitance, are only tested initially ınd after a design change that affects capacitance. Dthers should indicate if tested by inference or ıpplication of specified signals and conditions. The ıddress and data patterns used for verifying write and ead functionality as well as appropriate machine, est or device guardbands should be included in the documentation.

MECHANICAL/VISUAL

Critical mechanical parameters are: the package dimensions of thickness and lead spacing, which can affect how devices interact with automatic insertion equipment or the dimensions of the application; and solderability, which affects the mechanical, thermal and electrical connection of the device to the application.

Critical visual parameters are the marking of the device and the marking permanency. These are important to clearly and permanently identify the device, e.g., part number, date code, orientation.

RELIABILITY

Critical reliability parameters include endurance, data retention and package integrity. Endurance will be application dependent, i.e., how often the device is rewritten, will affect the overall failure rate. Data retention will be application sensitive, i.e., the intrinsic data retention failure rate of some devices or technologies may preclude some applications. Package integrity is not unique to nonvolatile memories but is also application sensitive, i.e., concerns with hermeticity especially for glass sealed packages and concerns with cumulative exposure to temperature and humidity for plastic packages.

Although not exactly reliability concerns, two other issues may be of concern when using nonvolatile memories: radiation tolerance and declassification ability. Radiation tolerance is a measure of how much radiation a device may receive and continue functioning. In some cases for similar technologies, radiation tolerance correlates with reliability performance, but is not always a means for comparing different nonvolatile technologies for reliability. Declassification ability is a measure of the difficulty or possibility of recovering information supposedly removed from the device.

MANUFACTURER'S SCREENING

ELECTRICAL

Manufacturing of microcircuits consists of three major steps: fabrication, assembly and test. Fabrication consists of various physical, chemical, photolithographic and inspection operations to form die on the microcircuit wafer. Assembly consists of placing microcircuit die in a package for connection to other elements. Test consists of identifying the conformance level of each microcircuit.

Normal microcircuit manufacturing practices include one or more 100% electrical tests, e.g., each device is tested for DC, AC and functional parameters, separating devices by performance level. For complex microcircuits such as nonvolatile memories, electrical testing before assembly is done at room temperature and electrical testing post assembly is at high and/or cold temperature. Military devices require testing at high, low, and room temperatures. MOS devices are worst case at higher

temperatures; thus, commercial devices may have a single insertion at high temperature and be guardbanded for parameters that are adversely affected by lower temperatures.

Complex devices are tested using automated testers (ATE—Automated Test Equipment) and test handlers with suitable interface hardware. The ATE is controlled by software, called a test program, which contains the various algorithms for testing a device. These will include the forced and measured values, guardbands, data and address patterns in a sequence sufficient to exercise all functions at applicable data sheet limits. In addition, manufacturer's test programs typically include special modes that allow operation of the device in a non-data sheet specified manner to improve test effectiveness or efficiency, e.g., apply an accelerating stress or reduce test time. Handlers will control the ambient temperature for test and segregate devices to various bins by test results.

Users should verify the manufacturer has fully documented the test program, interface hardware, the accuracy and precision of the test setup and the operating procedures for performing test.

RELIABILITY

Although microcircuits are designed for reliability, variability in the manufacturing processes could cause sooner than expected degradation of performance. This infant mortality is usually the result of random defects in manufacturing material or processes and may be detected by accelerated stresses.

Nonvolatile memories have two reliability parameters, endurance and data retention, which require evaluation and possible additional screening to remove infant mortalities. Screening of other reliability parameters should be consistent with that of other microcircuits fabricated with similar processes and assembled in similar packages. Test methods should reference MIL-STD-883 for hermetic devices or JEDEC Standards for plastic devices.

The manufacturer's test flow should include screens for endurance and data retention. Endurance screening is typically performing some number of endurance (program/erase) cycles or other oxide stress to accelerate defects in the charge transmission oxide. This is usually followed by a data retention stress, e.g., a high temperature unbiased bake, for a data retention screen. The manufacturer should be able to provide a methodology and data to support whatever endurance and data retention screens are used. Test Method 1033 of MIL-STD-883 provides a format for defining the requirements for an endurance and data retention screen.

QUALIFICATION TESTING

CHARACTERIZATION

Upon identification of a potential device for an applica tion, the adequacy of the device for the application mu be verified. Given the application constraints are know this usually consists of characterizing the electrical ar reliability performance of the proposed device. Befor embarking on the very expensive effort of device cha acterization, several other activities should be performe

The manufacturer should be audited by the user users' representative, e.g., DESC or the NSI (Nation Supervising Inspectorate for the ISO-9000 series Qua ity Systems), for general capability to manufacture cor sistently a device that conforms to applicable specifica tions. This will include system capability as well a specific technical abilities. Then the manufacturer shoul provide information to the user, detailing the manufac turing technology and device performance specifica tions and reliability expectations.

Once satisfied that the manufacturer and device compl with the application requirements, the user should ob tain some devices for validation of promised results User testing should verify performance to the data shee or other applicable specification and should be used t establish correlation between the manufacturer's in spection and the user's application. Critical electrica and mechanical/visual parameters should require extr attention to assure consistency in measurement.

Reliability parameters should receive characterization in particular endurance and data retention. Program erase cycling and data retention bake should continu until the onset of endurance wearout, i.e., where th endurance failure rate increases with additional cycles Verification of the intrinsic data retention failure rat should establish, using standard deacceleration tech niques, that the MTBF of the nonvolatile memory i greater than the application's required storage time Other reliability parameters, such as life test, may us data provided by the manufacturer.

A typical endurance and data retention characterizatio test would consist of choosing two samples; then: sub ject the first sample to the number of endurance cycles at the temperature used in the application followed by a data retention bake that correlates to the storage time required of the application. Subject the second sample to increasing numbers of program/erase cycles, inter leaved periodically with short data retention bakes until the majority of devices have failed two or more bits. Analysis of this data in conjunction with the manufactur ers supplied data should validate the feasibility of the proposed device in the application.

ERIFICATION

ter characterization verifies the microcircuit is capable meeting the application requirements, some ongoing sting will be required to assure production deliveries ntinue to conform to specification. Commonly used ethods include: source inspection, incoming inspec-n, regular audits and periodic monitors.

ource inspection requires the user or designate to tness critical manufacturing or quality assurance op-ations to verify shipped product conforms to the appli-ble specification. Incoming inspection accomplishes similar purpose by having the user inspect production aterial upon receipt.

egular audits are the occasional assessment of the anufacturer by the user to assure that manufacturing ethods, systems, procedures and specifications are eing adhered to in the ongoing production of the rchased microcircuits. Periodic monitors are the sub-cting of a sample to an incoming test or a characteriza-n evaluation.

coming inspection is probably the least productive of e various verification methodologies and certainly the ost expensive. Regular audits, combined with periodic onitors is probably the most effective but requires a illed and trained audit and evaluation team to imple-ent. Source inspection is the simplest and probably ast expensive means to verify product conformance to ecification. The means that are most appropriate to tuation depend on the relationship of manufacturer nd user, the capabilities of both parties, and any other verriding considerations, e.g., government require-ents. In all cases, regular communication between anufacturer and user is vital to assure ongoing perfor-ance improvement.

eliability parameters should be monitored by the anufacturer's reliability reports. In addition, endur-nce, data retention, and steady state life performance an be periodically validated by the following methodol-gy:

n endurance test, reference Method 1033 of MIL-STD-83, shall be added before performing the steady state fe test and extended data retention test. Cycling may be hip, sector, block, byte or page on finished devices. The llowing conditions shall be met:

. All bytes shall be cycled for a minimum of the specified number of cycles at equipment room ambient.

2. Perform parametric, functional and timing tests at room temperature, after cycling. Devices having bits not in the proper state after functional testing shall constitute a device failure. Separate the devices into two groups for extended data retention and steady state life test, then write correct data patterns.
3. Perform the extended data retention, consisting of a high temperature unbiased storage for 1000 hours minimum at +150°C minimum. The storage time may be accelerated by using a higher temperature according to the Arrhenius relationship and an apparent activation energy of .6eV. The maximum storage temperature in a Nitrogen environment shall not exceed +175°C for hermetic or +160°C for plastic devices. All devices shall be programmed with a charge on all memory cells in each device, such that a loss of charge can be detected e.g., worst case pattern.
4. Read the data retention pattern and perform parametric, functional and timing tests at room temperature, after cycling and bake. Devices having bits not in the proper state after functional testing shall constitute a device failure.
5. Perform steady state life, reference method 1005 condition D of MIL-STD-883, for 1000 hours at +125°C in a Nitrogen environment. The steady state life time may be accelerated by using an Arrhenius relationship and apparent activation energy of .4 eV. The maximum operating junction temperature shall not exceed +175°C. All devices shall be written with a checkerboard or equivalent topological alternating bit pattern.
6. Read the steady state life pattern and perform parametric, functional and timing tests at room temperature, after cycling and steady state life. Devices having bits not in the proper state after functional testing shall constitute a device failure.
7. The endurance, data retention and steady state life tests shall individually pass a sample plan to an LTPD of 5/1 (sample size = 77, accept = 1), equivalent to an AOQL = 1%.

SUMMARY

Reprogrammable nonvolatile memories should be procured with the same care as other microcircuits. The additional application dependent reliability parameters of endurance and data retention require careful consideration of device design, manufacturing methodology, reliability criteria and documented performance.

ull-Featured E²PROM Cell Operation

ıe Catalyst full-featured E²PROM memory cell, used r both serial and parallel devices, consists of an MOS ıating gate memory transistor, a select transistor and ıpport circuitry (Figure 1). The memory cell defines a gic state, either a "1" or a "0," by storing negative or ısitive charge on the floating polysilicon gate of Q1. ıe status of the gate is sensed during the read operaın.

harge is transferred to and from the floating gate ırough the thin tunnel dielectric by Fowler-Nordheim ınneling; i.e., the quantum-mechanical transmission of ı electron through the oxide bandgap. Tunneling ocırs when a high voltage, generated within the die, is aced across the tunnel dielectric region of the memory ansistor.

or a logic "1," electrons are stored on the floating gate, sing the conditions defined for "program" (Table 1). Q1 as the high voltage placed on the top polysilicon gate, a the sense line through Q4 and Q5. The source and rain are grounded, through array Vss, Q2 and Q3 espectively. Fowler-Nordheim tunneling, generated by ıe high field from the top gate to the drain, will transfer lectrons to the floating gate. The net negative charge ill raise the Q1 threshold to a value greater than the eference voltage.

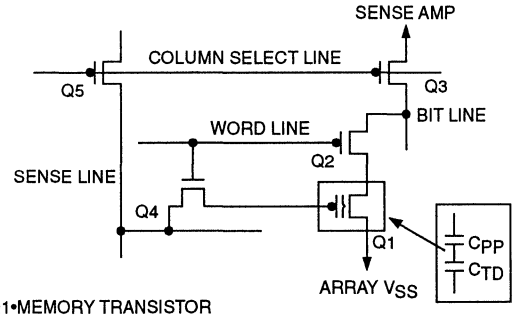
For a logic "0," holes (absence of negative charge) are stored on the floating gate, using the conditions defined for "erase" (see attached table). Q1 has a high voltage place on the drain, via the bit line through Q2 and Q3. The top gate is grounded through Q4 and Q5, and the source is floating. Fowler-Nordheim tunneling transfers electrons off the floating gate. The net positive charge will lower the Q1 threshold to a value less than the reference voltage.

During the read operation, the reference voltage is applied to the top gate of Q1 via the sense line. For Q1 thresholds greater {less} than the reference voltage, the selected Q1 will {will not} conduct. The cell current on the bit line is detected by the sense amplifier and the resulting output is a logic "1" {"0"}.

Q2 isolates unselected memory transistors on the same bit line, eliminating program and read disturb. Q4 isolates unselected bytes on the same sense line, eliminating DC program, DC erase and read disturbs.

Support circuitry is used to input and output data to and from the memory in various modes, e.g., serial, parallel, page. Error correction can be implemented using multiple cells and an ECC algorithm.

igure 1. Generic Full-Featured E²PROM lemory Cell



Q1•MEMORY TRANSISTOR
Q2•ROW SELECT TRANSISTOR
Q3•COLUMN SELECT TRANSISTOR
Q4•BYTE SELECT TRANSISTOR
Q5•SENSE SELECT TRANSISTOR

Table 1. Full-Featured E²PROM Memory Cell

	PROGRAM	ERASE	READ
Bit Line	0	20 V	1.5 V
Column Select	0	0	5V
Word Line	20 +Vt V	20 +Vt V	5 V
Sense Line	20 V	0	2 V
Array VSS	Ground	Floating	Ground

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lash Memory Cell Operation

ıe patented Catalyst flash memory cell consists of an OS Floating Gate memory transistor and support cuitry (Figure 1). The memory cell defines a logic ate, either a "1" or a "0," by storing two different levels negative charge on the floating polysilicon gate of Q1. ıe status of the gate is sensed during the read operaon.

ıarge is transferred to the floating gate through the ıte oxide by channel hot electron injection. Charge is ansferred from the floating gate by Fowler-Nordheim nneling; i.e., the quantum-mechanical transmission of ı electron through the oxide bandgap. Both transmison mechanisms require the application of a high voltge, which may be supplied externally or generated ithin the die.

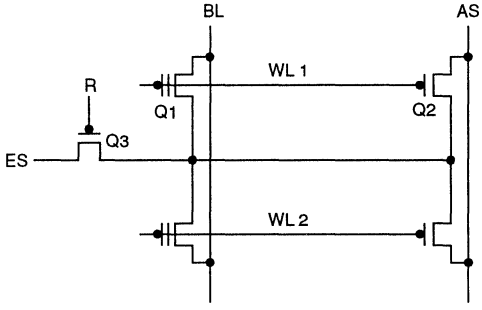
or a logic "0," electrons are stored on the floating gate, sing the conditions defined for "program" (Table 1). Q1 as the high voltage placed on the top polysilicon gate, a the word line, and the drain, via the bit line. Q1's ource is connected to array source, which is at ground, ırough Q2. Channel hot electrons, generated by the ource-drain potential, are swept to the floating gate by ıe top gate to substrate field. The excess negative charge will raise the Q1 threshold to a value greater than the reference voltage.

For a logic "1," a reduced quantity of electrons is stored on the floating gate, using the conditions defined for "erase" (see attached table). Q1 has a high voltage placed on the source, via the erase source through Q3. The top gate is grounded, via the word line, and the drain is floating. Fowler-Nordheim tunneling transfers electrons off the floating gate. The Q1 threshold is lowered to a value less than the reference voltage.

During the read operation, the reference voltage is applied to the top gate of Q1, via the word line. For Q1 thresholds greater {less} than the reference voltage, the selected Q1 will {will not} conduct. The cell current on the bit line is detected by the sense amplifier and the resulting output is a logic "0" {"1"}.

Q2 isolates unselected memory transistors on the same bit line, eliminating program disturb. Q2 also isolates every 16 memory transistors along the word line, preventing DC program and DC erase disturbs. Q3 isolates each sector for erasure, preventing overerase of unselected sectors.

igure 1. Generic Flash Memory Cell



ı1 • MEMORY TRANSISTOR
ı2 • PASS GATE (EACH 16 COLUMNS)
ı3 • SECTOR SELECT (EACH 16 ROWS)
EVERY 16 ROWS • 2K BYTES • 1 SECTOR

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Table 1. FLASH Memory Cell

	PROGRAM	ERASE	READ
BL (Bit Line)	≈7 V	Floating	≈1 V
WL (Word Line)	V_{pp}	0	V_{CC}
AS (Array Source)	0	0	0
ES (Erase Source)	0	V_{pp}+	0
R (Sector Select)	OFF (0)	V_{pp}+Vt	OFF (0)

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'ailure Rate Prediction

:egrated circuits have no moving parts, yet like all ıctional devices have a possibility of failure. Although ə future of an individual device cannot be predicted, ə lifetime of a population of devices will have predict- ıle behavior. The expected lifetime will be a function of ə design, manufacturing, screening and testing history the population.

ıilure rate predictions are used to estimate the longev- ' of applications using the devices. Reliability is often ɜscribed as device performance over time; thus, the ɜhavior of populations of devices is mathematically ɜscribed using probability models. Probability density nctions and cumulative distribution functions are used r predictions of failure. Some commonly used terms ıd definitions are:

. Mortality Function (Probability Density Function f Time-to-Failure); f(t):

he rate at which devices are failing referenced to the riginal population. f(t)dt is the probability the device will ıil in the interval "t" to "t + dt."

. Cumulative Mortality Function (Cumulative Distri- ution Function of Time-to-Failure), F(t):

ə] the integral of f(t).
ɔ] the probability that a device will have failed by time "t";
ɔ] the fraction of units that have failed by time "t."

. Cumulative Reliability Function; R(t) = 1 – F(t):

ə] the probability that a device will function at time "t";
b] the fraction of units that have survived to time "t."

. Hazard Rate (Instantaneous Failure Rate); h(t):

The rate at which devices are failing referenced to the ;urvivors.

ı(t) = f(t) / R(t).

ɜ. Cumulative Hazard Function; H(t):

The integral of h(t).

ɜ. FIT:

Failure In Time: the number of failures per 10^9 hours. Typically used to express the failure rate.

7. %/1000 hours:

An alternative expression of the failure rate.

Many population failure distributions have been utilized; e.g., the normal, lognormal, weibull, exponential extreme value. The exponential (similar to the weibull with $\beta = 1$) is often used for modeling because of its ease of use and applicability. The exponential is appropriate for failures caused by random latent defects or a component of many constituents.

The failure rate of devices is expected to vary over the lifetime of the population. This behavior is modeled by the classic "bathtub curve"; which includes an infant mortality region, an intrinsic or useful life region and a wearout region.

Infant mortalities are a result of latent defects or poor manufacturing practices, which result in early failures and a sharply declining failure rate. The device manufacturer should eliminate this region by design or screens, i.e., accelerated stresses that are part of the manufacturing flow.

The wearout region is caused by an accumulation of stress during the operation of the device, resulting in an increasing failure rate. This region is eliminated by the user choosing a device of sufficient reliability for the application.

The useful life region is a function of the intrinsic capability of the device including the design, construction materials, manufacturing, and screening flow. This region is characterized by a relatively constant failure rate; thus, the exponential is an appropriate distribution: $f(t) = \tau e^{(-\tau t)}$ and $h(t) = \tau$; where τ is the constant hazard rate.

The reliability performance of a microcircuit population is evaluated by stressing a sample. The stress is performed at conditions which should accelerate the failure rate during the stress, relative to normal operating conditions. Because a sample is used, the estimate (τ) of the population hazard rate (τ) is derived by statistics. The χ^2 (chi-squared) distribution is used to determine the τ confidence interval.

$$\tau = x / \{2 \times \Sigma ntA\}$$

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where χ is the tabular value of the χ^2 for the desired confidence (α), with 2r + 2 degrees of freedom (r = the number of failures in the sample).

n = the number of devices on stress.
t = the duration of the stress for each passing device.
A = the acceleration factor.

The failure mechanisms that contribute to the failure rate vary with temperature. The mortality function is the probability distribution that represents the aggregate of these mechanisms; thus, the mortality rate will vary with temperature. Analogous to modeling the rate of a chemical reaction, the Arrhenius equation is used to model the shift in the mortality distribution. The apparent activation energy, associated with various failure mechanisms, quantifies the temperature dependence of the distribution's shift.

The acceleration factor, A, is calculated by the Arrhenius equation and the apparent activation energy:

$A = \exp\{[Ea/k][(1/Tn) - (1/Tj)]\}$ where,

Ea = the apparent activation energy.

k = Boltzman's constant (8.62×10^5)

Tn = normalized junction temperature °K.

Tj = stress junction temperature in °K.

Models for infant mortality and wearout have been derived, but are not pertinent to useful life failure rate prediction.

EXAMPLE

A sample of 77 devices is submitted to dynamic burn at an ambient oven temperature of 150°C for 20 hours, with 1 failure at 1000 hours. What is the 9(confidence interval estimation of the failure rate at 55 ambient operating.

$\tau 150 = X / \{2 \times \Sigma nt\}$

where X = 7.779 for $\propto$ = .90 and degrees of freedom = 4 [(2 x1) + 2]

$\Sigma nt = (76 \times 2000) + (1 \times 1000) = 153{,}000$

thus

$\tau 150 = 7.779 / (2 \times 153{,}000) = 25{,}422$ FITs

$\tau 55 = \tau 150 / A$

Notes: The typical Ea for an MOS device in dynam burn-in is .4. Ambient temperatures were given and tl equation requires junction temperatures. For this d and package, assume the junction temperature rise 5°C; therefore,

$A = \exp\{[.4/8.62 \times 10^5] \times \{[1/(55+273+5)] - [1/(150+273+5)]\}\}$

$= 22$

$\tau 55 = 25{,}422 / 22 = 1156$ FITs

The estimation of a failure rate based on a single sma sample is limited by the statistics of the sample size. I order to have true representations of the populatic failure rate, data must be combined from several sample Therefore, typical failure rates are given for devic families or technologies, not individual device types.

;ingle Transistor 5V Flash Technology, vith Sector Erase

1.0µm Flash technology has been developed, for full evice operation with one external 5V power supply. he single transistor Flash cell has been used to obtain high density with the smallest possible die size, which inimizes cost.

he use of a 5V power supply enlarges the range of pplications and reduces cost, by eliminating the need or an additional power supply.

he use of sector erase is particularly suited to applicaons where a boot program must remain unchanged hile the program memory or remaining data is updated.)ne chip providing both functions will reduce the numer of chips on the board. Otherwise, a standard design ould use an E^2PROM or battery backed-up RAM, for updatable memory, and a PROM or EPROM to store the boot program.

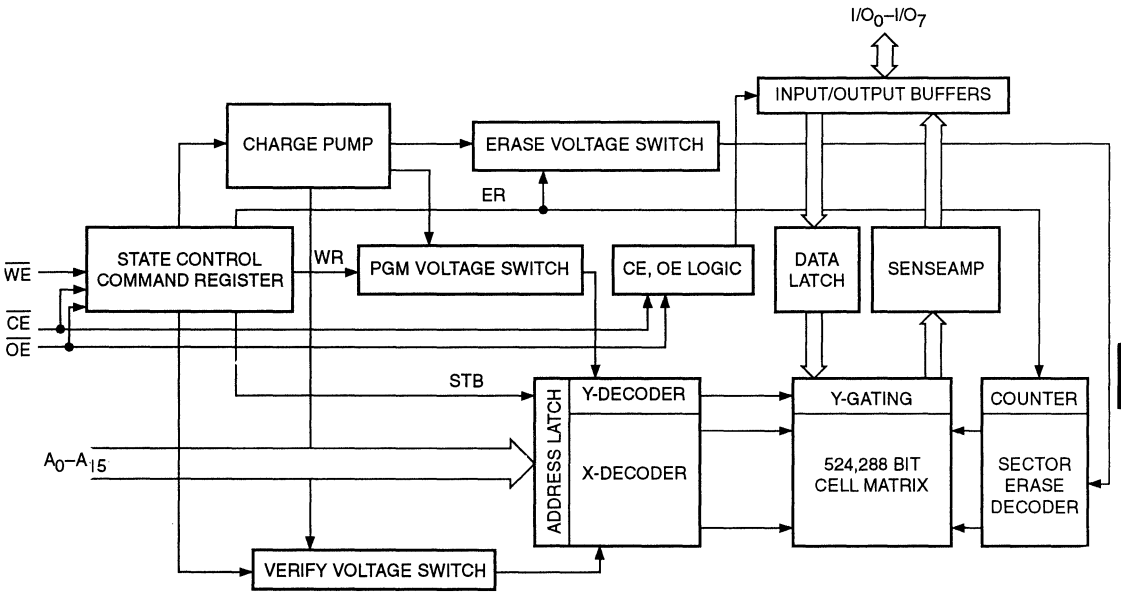
The advantages of one 5V power supply, one chip for boot and updatable memory, and device price will significantly reduce the cost of an application.

The 5V functionality is achieved by means of 2 charge pumps:

a. one providing 10 mA at 7V during programming and 5 mA at 13V during erase,

b. one providing 100 µA at 13V, during programming to pump up the Word Lines and during erase to control the sector decoder.

igure 1. Block Diagram



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The design of a 5V to 13V converter with high output current implies not only a careful sizing of the capacitors and diode mounted transistors, but requires noise reduction features, such as separate ground lines, stepped clocks and pump output regulation (Figure 1, Block diagram).

The array consists of 8 blocks, one for each I/O pin. To ground the cell source during read and program, pass gates are regularly distributed along each word line. To bring the cell source to a high voltage during erase, each source is tied, through an erase decoder, to the erase voltage internal supply. The sector size is 2K bytes, consisting of 16 rows in each block.

The addition in the array of the pass gates and erase gates allows the erase of single sectors. These gates decrease the leakage on each bit line, since only 16 cells on one bit line have their source grounded at one time. This provides extra protection against the risk of "over-erase," e. g., disturb of the accessed cell by unselected depleted cells (Figure 2, array structure).

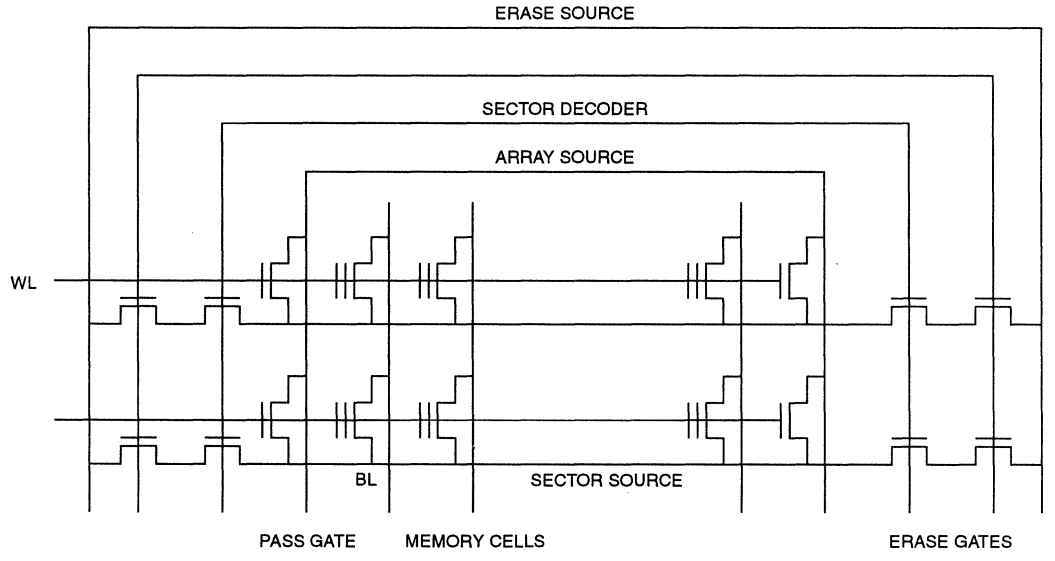
The sectors can either be erased one by one at random, or sequentially. One by one, an erase pulse is sent selectively to the chosen sector. The sector data is th verified and other erase pulses are sent, if necessar Sequentially, each erase pulse increments the sect pointer, so that all sectors erase within the same su routine. A reset command initializes the sector pointe The sequential erase is faster for a program memo update, with boot sectors unchanged. The random se tor erase is faster for a data memory update, with oth data sectors unchanged.

Preliminary reliability evaluations verify the usual floa ing gate data retention of greater than 100 years. Endu ance is specified at 1% AOQL for 1000 cycles, which more than adequate for program memory and mar data memory applications. The technology is intrins cally capable of high endurance; however, the potenti additional screening requirements are not compatib with making a low cost device.

The circuitry and technology have been developed for high density, reliable, cost effective 5V only Flas memory.

A 512K bit, CAT28F512V5, has been designed with thi technology, and is now in pre-production. A 1 Megabi CAT28F010V5, is in development.

Figure 2. Array Structure



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ble 1. Device Characteristics (Typical)

cess Time	120 ns
C Standby	10 µA
C Read (8.3 MHz)	30 mA
C Program	50 mA
C Erase	20 mA
ogram Time	10 µs/byte
ase Time	100 ms/sector

Table 2. Process Characteristics

Erase Mechanism	Tunneling
Program Mechanism	Hot Electron Injection
Tunnel Oxide	11 nm
Gate Oxide	25 nm
Polysilicon Layers	2
Metal Layer	1
Metal Thickness	1.0 µm
Metal Width	1.4 µm
Metal Spacing	1.2 µm
Cell Size	16.8 μm^2

eatures and Performance of Reprogrammable lonvolatile Floating Gate Memories

ITRODUCTION

ver the past 15 years, various floating gate devices ave been increasingly used for reprogrammable non- latile memory (NVM) applications. The UV-EPROM, eveloped as an engineering prototype tool, gradually placed the original IC memory for program storage, e ROM. The UV-EPROM technology evolved into the ^{2}PROM technology, and the two have recently merged create the flash E^{2}PROM and EPROM technology.

ne floating gate MOS transistor allows the use of a ultitude of design approaches to satisfy user needs. ne major device categories are NVRAM, serial ^{2}PROM, parallel E^{2}PROM, flash, UV-EPROM and the TP-EPROM. This paper will compare the features and erformance of these categories.

PPLICATIONS

omparisons must start with the application perspec- ve. Reprogrammable nonvolatile memories are re- uired where information may be changed during opera- on and must be retained during power-off. The two ajor types of information are data and program, each pe contains several classifications.

ata memory includes information from recorders or ensors that is required for historical purposes or to aintain continuity of operation after power loss.

rogram memory can be classified as configuration, aceability, boot program or main program. Configura- on contains look-up tables or other settings to control ne features and set-up of different equipment and rmats within the system. Traceability includes calibra- on and maintenance settings and history, as well as elf-test vectors. The boot program is the series of structions necessary to start the system. The main rogram is the algorithm or operating system, containing ne instructions to operate the system.

Within each classification of memory, the actual applica- ion requirements may vary. Intrinsically, floating gate memories have different performance characteristics and limitations. These must be carefully matched with the application. Some of the most important system considerations are: how many times must the memory be reprogrammed, what is required to change the memory, what voltages must the system supply, how much memory is required and how much does the memory function cost?

These system considerations can be directly compared with NVM features and performance. How many times the memory must be reprogrammed is related to device endurance, i.e., the minimum number of program/erase cycles at a given failure rate (or cumulative percent fail). What is required to change the memory relates ease of erasing and reprogramming the device, i.e., the level, timing, and sequence of waveforms. What voltages the system must supply for device operation relates to tradeoffs in cost and performance issues of the circuit board.

How much memory is required varies by memory classification and available device density. How much the memory function costs depends on what categories and densities of memory and support devices are required.

DEVICE FEATURES AND PERFORMANCE

Important device parameters include speed, write method, power supply requirements, endurance, data retention, density, package pin count and types of usable packages. Speed involves both read and write time impact on system performance. The erasing and programming method, e.g., pulse or algorithmic, affects the total time to change the system memory. Some devices require the system to be interactive with the device during writing, while other devices allow alternate system operations to be performed in parallel.

The endurance capability, typically the number of program/erase cycles to meet a 1% AOQL guarantee, is normally much greater than the system update frequency requirement. Data retention of floating gate

devices is essentially infinite compared to alternates such as batteries or SNOS. The power supply voltage and power dissipation relate to circuit board design and the types of other components required, e.g., a 3 volt device may be more suitable for portable applications.

The number of transistors per memory cell relates directly to density and die size, thus cost. The die function and size also determine what package types and pin counts are suitable.

CONCLUSION

Selection of a device for an NVM application is a comp cated task. A number of floating gate reprogrammat nonvolatile memory devices exist, with a wide variety features and performance, which further complicat the selection. This paper has summarized the status existing devices, comparing critical features and perf mance to simplify the choice of the most appropria device for a given application.

Table 1. Application Comparisons

	Application	Update Frequency	Ease of Write	Density Range	Cost/ Bit	Cost/ Device
NVRAM	Data	Store or Power Down	Very Easy	256 bit to 1K	High	High
Serial	Configuration	Power Down	Easy	256 bit to 16K	Medium	Low
Parallel	Data, Boot Program, Main Program, Configuration, Traceability	1–5/day 1–2/year 1–2/year Power Down 2–6/year	Easy	4K to 1M	Medium	High
Flash	Main Program, Boot Program, Data	1–2/year 1-2/year 1–4/month	Moderate	64K to 2M	Low	Medium
UV-EPROM Window	Main Program, Boot Program	1–3/decade 1–3/decade	Difficult	256K to 4M	Low	Medium
EPROM OTP	Main Program, Boot Program	N/A N/A	N/A	256K to 4M	Low	Low

Table 2. Performance Comparisons

	Read Speed	NV Write Speed	NV Write Method	Endurance	Power Supply Required	Typical Power Dissipation
NVRAM	200ns to 100 KHz	10ms /device	Store Device	10,000	5V	100mw to 200mw
Serial	250 KHz to 2 MHz	5–10ms /address	Pulse: Address	10,000 100,000	2, 3, 5V	15mw
Parallel	35ns to 250ns	1–10ms /byte,page	Pulse: Byte, Page	10,000 100,000	3, 5V	100mw to 500mw
Flash	150ns to 250ns	10–100 µs /byte	Algorithmic Chip, Sector	1,000 10,000	5V or 5V & 12V	150mw to 500mw
UV-EPROM Window	55ns to 250ns	10–100 µs /byte	Algorithmic Chip	100	5V & 12V	150mw to 500 mw
EPROM OTP	55ns to 250ns	10–100 µs /byte	Algorithmic Chip	N/A	5V & 12V	150mw to 500mw

able 3. Technology Comparisons

	Endurance	Data Retention	Density Range	Transistors Per Cell	Package & Pins	Package Types[1]
NVRAM	10,000	>100 years	256 bit to 1K	9–13	8–18	SMT,TH,MOD
Serial	10,000 100,000	>100 years	256 bit to 16K	2	8–14	SMT,TH,MOD
Parallel	10,000 100,000	>100 years	4K to 1M	2–6	24–44	SMT,TH,MOD
Flash	1,000 10,000	>100 years	64K to 2M	1	28–44	SMT,TH,MOD
UV-EPROM Window	100	>100 years	256K to 4M	1	28–44	TH
EPROM OTP	N/A	>100 years	256K to 4M	1	28–44	SMT,TH

otes
SMT = Surface Mount Technology, TH = Through Hole, MOD = Module or Hybrid

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CATALYST SEMICONDUCTOR

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3-Wire Bus Serial E^2PROMs 3

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SECTION 14 DIE PRODUCTS

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Catalyst Die Products

INTRODUCTION TO UNENCAPSULATED DIE

This document provides the user with guidelines for processes, testing, and application issues associated with purchasing unencapsulated E^2PROM die or wafers. Product electrical specifications, functional descriptions, and bonding diagrams are not included. This information is available in the appropriate sections of the Catalyst Data Book or directly from Catalyst.

The guide provides recommendations for die attach and wire bonding methods. Typicals for die thickness, top passivation composition and thickness, and metalization composition and thickness are included. The Catalyst production flow is outlined herein showing the steps taken for each die or wafer shipment. In addition, application information covering some common issues encountered when using E^2PROM die is provided.

Properly packaged die and wafers will perform according to the parametric, AC, and DC parameters listed in the device data sheet. Procedures to demonstrate conformance to these specifications should be established contractually with Catalyst on an individual basis.

STANDARD DIE SALES GUIDELINES

Reliability Expectations:

1. Endurance/Data Retention: 5% AOQL.
2. Life Test: Same as packaged units; see reliability reports.

Guarantees:

1. 1% AOQL for Visual per MIL-STD-883, Method 2010, Condition B for plated and inspected die.
2. Packing/Shipping per "Packaging" Section, in accordance with Catayst shipping specification 17001.

Correlated Yields:

1. Expect initial yields while doing correlation to be:
   A. ≈70% for high density devices (≥ 64K bits).
   B. ≈90% for low density devices (≤ 16K bits).
2. After correlation, yields should be:
   A. ≈90% for high density devices (≥ 64K bits).
   B. ≈95% for low density devices (≤ 16K bits).

Test Modes:

Catalyst uses control fuses for various built-in test modes and other functions within some devices. Exposure to UV light or misapplications of high voltages can erase or reprogram the fuses, causing loss of functionality. Control fuses are used for redundancy repair to improve manufacturing yield and chip functions to reduce test time. Catalyst strongly recommends the use of control fuses.

STANDARD DIE PACKAGING

All die shipped by Catalyst will be packaged per the following:

1. The die will be placed in a "waffle pack" with a cavity of proper size to restrain the die without causing damage and without allowing the die to change orientation.
2. A lint-free paper insert is placed over the "waffle pack". The waffle pack lid is placed on top and then secured with plastic locking clips.
3. A set of waffle packs (as required) are stacked.
4. A label with lot number, quantity, part number, and packing date is placed on the waffle pack.
5. Die do not require cleaning prior to assembly.

STANDARD WAFER PACKAGING

All wafers shipped by Catalyst will be packaged per the following:

1. Wafers will be separated by lint-free paper.
2. Wafers will be packed in an appropriately sized shipping container to minimize movement.
3. A label with lot number, quantity, part number, and packing date is placed on the shipping container.

GENERAL DIE or WAFER SPECIFICATIONS

1. Thickness: 430 to 510 μm (17 to 20 mils).

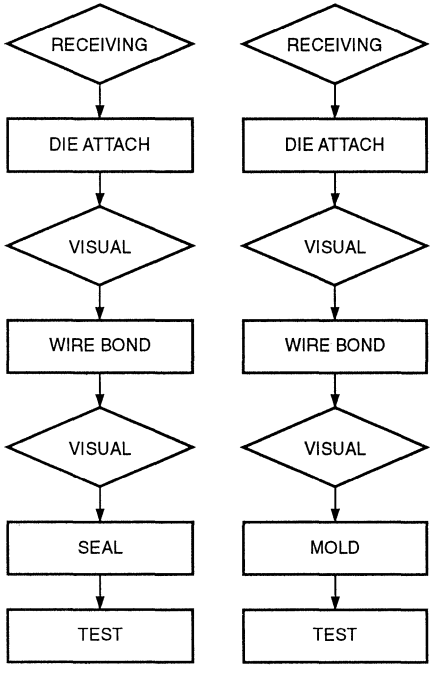
   Other thicknesses down to 280 μm (11 mils) can be accomplished. Please contact Catalyst for this price adder.

2. X-Y Dimensions: Per each device (contact Catalyst). Wafer diameter: 125 or 150 mm (5 or 6 inches).

3. Top Glassivation: Varies according to device ar manufacturing location. Typically 1 μm of SiO (oxynitride).

4. Metalization: Varies according to device and mani facturing location. Typically 1 μm of Al/Si (99/1) Al/Si/Cu (98.5/1/.5).

SUGGESTED ASSEMBLY FLOW AND CONDITIONS



CONDITIONS

DOCUMENTATION CHECK. OPTIONAL

VISUAL - 1% AOQL
MECHANICAL/FUNCTIONAL - 2.5% AOQL

HERMETIC: SILVER-GLASS WITH VENDOR RECOMMENDED CURE PROFILE.
PLASTIC: EPOXY WITH VENDOR RECOMMENDED CURE PROFILE.

MIL-STD-883, METHOD 2010, CONDITION B

HERMETIC: 99%/1% AL/SI 1.25 MIL WIRE ULTRASONIC WEDGE BOND.
PLASTIC: GOLD 1.3 MIL WIRE, 200°C THERMASONIC BALL BOND.

MIL-STD-883, METHOD 2010, CONDITION B

HERMETIC: GLASS FRIT, PEAK TEMP < 430°C SOLDER SEAL, PEAK TEMP < 370°C
PLASTIC: LOW STRESS MOISTURE RESISTANT MOLDING COMPOUND.

TIMING, PARAMETRIC, FUNCTIONAL

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Note:
(1) Final electrical screen and test yield will vary with device type data sheet performance limits (i.e. access time, temperature range, V_{CC} range and use of redundancy).
(2) For some devices, test yields may be improved by the use of redundancy repair. Information on how to use redundancy repair is available from Catalyst.

\PPLICATION INFORMATION

'ower Up and Power Down Consideration:

;atalyst E²PROMs contain circuitry to minimize false /rite during power up or power down. This circuitry ırevents writing under the following conditions:

. V_{CC} is less than V_{WI}.

:. A write pulse of less than 20ns duration.

;atalyst recommends the following power up/power lown sequence, applicable.

'ower Up Sequence:

. All addresses and data lines to 0V.

:. Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) to 0V.

3. Write Enable ($\overline{WE}$) to 3V or TTL high.

4. V_{CC} to Supply Value.

5. Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) to high.

'ower Down Sequence:

. All addresses and data lines to 0V.

:. Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) to 0V.

3. Write Enable ($\overline{WE}$) to 3V or TTL high.

4. V_{CC} to 0V.

5. Wait longer than 10 ms.

6. Write Enable ($\overline{WE}$) to 0V.

;ome devices provide a Software Data Protect (SDP) eature. When activated, this feature disables write)perations through software, by accessing an internal :ontrol register. Software control of write operations can educe the possibility of inadvertent writes resulting from)ower up, power down, or momentary power distur-)ances. Consult the Catalyst Data Book for the availabil- ty and specifics on the use of this feature.

Signal Lines Above V_{CC}

Some devices incorporate built-in test modes to aid in testing or modify device functions. These test modes are accessed by taking one or more device pins above the maximum recommended input level to enable the mode, then operating other pins as necessary. Although unlikely, a noise "spike" of sufficient duration and amplitude can enable a test mode. If this occurs, device operation may be changed. The device may be reset by turning power off; however, in some cases a change to device functionality occurs. Consult Catalyst for recommended preventative measures and recovery procedures.

Substrate Grounding

Some devices require a substrate ground connection for proper operation. If the die attach pad is not grounded or has a high resistance path to ground, the device timing or functionality performance may be affected. Other devices are designed using a back-bias generator; thus, requiring isolation of the die attach pad. Consult Catalyst for the recommended die attach and pad design per device.

Effects of UV Light or X Rays

E²PROM cells as control fuses are used to select or modify various internal device functions. If die are exposed to UV (ultra- violet) light or X-Rays of sufficient intensity and duration, these cells could be erased. This erasure is the same mechanism as used by UV EPROMs and is non-destructive, but could cause a change in functionality of the device. Consult Catalyst for recommended preventative measures and recovery techniques.

Built-in Test Modes

Contact Catalyst for additional information of how to utilize the built-in test modes previously mentioned.

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Sidebraze 15-53

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Sales Offices 15-61

Ordering Information

SERIAL E²PROMs

-Wire Bus Structure (Data Book Section 2)

Device Order Number	Org.	Package J	J14	S	K	P	Special Features	Temp Range	Clock Freq.	# of Pins	Tape & Reel	Rail Qty.
CAT24C02P	256 x 8					x		†	100kHz	8		50
CAT24C02PI	256 x 8					x		I	100kHz	8		50
CAT24C02J	256 x 8	x						†	100kHz	8		100
CAT24C02J-TE7	256 x 8	x						†	100kHz	8	TE7	500
CAT24C02J-TE13	256 x 8	x						†	100kHz	8	TE13	2000
CAT24C02JI	256 x 8	x						I	100kHz	8		100
CAT24C02JI-TE7	256 x 8	x						I	100kHz	8	TE7	500
CAT24C02JI-TE13	256 x 8	x						I	100kHz	8	TE13	2000
CAT24C02J14	256 x 8		x					†	100kHz	14		56
CAT24C02J14-TE7	256 x 8		x					†	100kHz	14	TE7	500
CAT24C02J14-TE13	256 x 8		x					†	100kHz	14	TE13	2000
CAT24C02J14I	256 x 8		x					I	100kHz	14		56
CAT24C02J14I-TE7	256 x 8		x					I	100kHz	14	TE7	500
CAT24C02J14I-TE13	256 x 8		x					I	100kHz	14	TE13	2000
CAT24C02ZP	256 x 8					x	Z	†	100kHz	8		50
CAT24C02ZPI	256 x 8					x	Z	I	100kHz	8		50
CAT24C02ZJ	256 x 8	x					Z	†	100kHz	8		100
CAT24C02ZJ-TE7	256 x 8	x					Z	†	100kHz	8	TE7	500
CAT24C02ZJ-TE13	256 x 8	x					Z	†	100kHz	8	TE13	2000
CAT24C02ZJI	256 x 8	x					Z	I	100kHz	8		100
CAT24C02ZJI-TE7	256 x 8	x					Z	I	100kHz	8	TE7	500
CAT24C02ZJI-TE13	256 x 8	x					Z	I	100kHz	8	TE13	2000
CAT24C02ZJ14	256 x 8		x				Z	†	100kHz	14		56
CAT24C02ZJ14-TE7	256 x 8		x				Z	†	100kHz	14	TE7	500
CAT24C02ZJ14-TE13	256 x 8		x				Z	†	100kHz	14	TE13	2000
CAT24C02ZJ14I	256 x 8		x				Z	I	100kHz	14		56
CAT24C02ZJ14I-TE7	256 x 8		x				Z	I	100kHz	14	TE7	500
CAT24C02ZJ14I-TE13	256 x 8		x				Z	I	100kHz	14	TE13	2000

Note:
1) Contact factory for High Endurance device availability.

Key:

†	=	Blank = Commercial = 0°C to +70°C
I	=	Industrial = –40°C to +85°C
A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
Z	=	Zero Power™
J	=	S.O. (JEDEC)
J14	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
P	=	Plastic DIP
S	=	S.O. Non-Rotated (JEDEC)
TE7	=	Tape Embossed 7" Reel, Min. Order 500 Pcs/Reel
TE13	=	Tape Embossed 13" Reel, Min. Order 2000 Pcs/Reel

SERIAL E²PROMs

2-Wire Bus Structure (Data Book Section 2)

Device Order Number	Org.	Package					Special Features	Temp Range	Clock Freq.	# of Pins	Tape & Reel	Rail Qty.
		J	J14	S	K	P						
CAT24LC02P	256 x 8					x	L	†	100kHz	8		50
CAT24LC02PI	256 x 8					x	L	I	100kHz	8		50
CAT24LC02J	256 x 8	x					L	†	100kHz	8		100
CAT24LC02J-TE7	256 x 8	x					L	†	100kHz	8	TE7	500
CAT24LC02J-TE13	256 x 8	x					L	†	100kHz	8	TE13	2000
CAT24LC02JI	256 x 8	x					L	I	100kHz	8		100
CAT24LC02JI-TE7	256 x 8	x					L	I	100kHz	8	TE7	500
CAT24LC02JI-TE13	256 x 8	x					L	I	100kHz	8	TE13	2000
CAT24LC02J14	256 x 8		x				L	†	100kHz	14		56
CAT24LC02J14-TE7	256 x 8		x				L	†	100kHz	14	TE7	500
CAT24LC02J14-TE13	256 x 8		x				L	†	100kHz	14	TE13	2000
CAT24LC02J14I	256 x 8		x				L	I	100kHz	14		56
CAT24LC02J14I-TE7	256 x 8		x				L	I	100kHz	14	TE7	500
CAT24LC02J14I-TE13	256 x 8		x				L	I	100kHz	14	TE13	2000
CAT24LC02ZP	256 x 8					x	L,Z	†	100kHz	8		50
CAT24LC02ZPI	256 x 8					x	L,Z	I	100kHz	8		50
CAT24LC02ZJ	256 x 8	x					L,Z	†	100kHz	8		100
CAT24LC02ZJ-TE7	256 x 8	x					L,Z	†	100kHz	8	TE7	500
CAT24LC02ZJ-TE13	256 x 8	x					L,Z	†	100kHz	8	TE13	2000
CAT24LC02ZJI	256 x 8	x					L,Z	I	100kHz	8		100
CAT24LC02ZJI-TE7	256 x 8	x					L,Z	I	100kHz	8	TE7	500
CAT24LC02ZJI-TE13	256 x 8	x					L,Z	I	100kHz	8	TE13	2000
CAT24LC02ZJ14	256 x 8		x				L,Z	†	100kHz	14		56
CAT24LC02ZJ14-TE7	256 x 8		x				L,Z	†	100kHz	14	TE7	500
CAT24LC02ZJ14-TE13	256 x 8		x				L,Z	†	100kHz	14	TE13	2000
CAT24LC02ZJ14I	256 x 8		x				L,Z	I	100kHz	14		56
CAT24LC02ZJ14I-TE7	256 x 8		x				L,Z	I	100kHz	14	TE7	500
CAT24LC02ZJ14I-TE13	256 x 8		x				L,Z	I	100kHz	14	TE13	2000
CAT24C02AP	256 x 8					x	A	†	100kHz	8		50
CAT24C02API	256 x 8					x	A	I	100kHz	8		50
CAT24C02AJ	256 x 8	x					A	†	100kHz	8		100
CAT24C02AJ-TE7	256 x 8	x					A	†	100kHz	8	TE7	500
CAT24C02AJ-TE13	256 x 8	x					A	†	100kHz	8	TE13	2000
CAT24C02AJI	256 x 8	x					A	I	100kHz	8		100
CAT24C02AJI-TE7	256 x 8	x					A	I	100kHz	8	TE7	500
CAT24C02AJI-TE13	256 x 8	x					A	I	100kHz	8	TE13	2000
CAT24C02AJ14	256 x 8		x				A	†	100kHz	14		56
CAT24C02AJ14-TE7	256 x 8		x				A	†	100kHz	14	TE7	500
CAT24C02AJ14-TE13	256 x 8		x				A	†	100kHz	14	TE13	2000
CAT24C02AJ14I	256 x 8		x				A	I	100kHz	14		56
CAT24C02AJ14I-TE7	256 x 8		x				A	I	100kHz	14	TE7	500
CAT24C02AJ14I-TE13	256 x 8		x				A	I	100kHz	14	TE13	2000

Note:
(1) Contact factory for High Endurance device availability.

Key:

†	=	Blank = Commercial = 0°C to +70°C
I	=	Industrial = –40°C to +85°C
A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
Z	=	Zero Power™
J	=	S.O. (JEDEC)
J14	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
P	=	Plastic DIP
S	=	S.O. Non-Rotated (JEDEC)
TE7	=	Tape Embossed 7" Reel, Min. Order 500 Pcs/Reel
TE13	=	Tape Embossed 13" Reel, Min. Order 2000 Pcs/Reel

ERIAL E²PROMs

Wire Bus Structure (Data Book Section 2)

Device Order Number	Org.	Package J	J14	S	K	P	Special Features	Temp Range	Clock Freq.	# of Pins	Tape & Reel	Rail Qty.
CAT24C02AZP	256 x 8					x	A,Z	†	100kHz	8		50
CAT24C02AZPI	256 x 8					x	A,Z	I	100kHz	8		50
CAT24C02AZJ	256 x 8	x					A,Z	†	100kHz	8		100
CAT24C02AZJ-TE7	256 x 8	x					A,Z	†	100kHz	8	TE7	500
CAT24C02AZJ-TE13	256 x 8	x					A,Z	†	100kHz	8	TE13	2000
CAT24C02AZJI	256 x 8	x					A,Z	I	100kHz	8		100
CAT24C02AZJI-TE7	256 x 8	x					A,Z	I	100kHz	8	TE7	500
CAT24C02AZJI-TE13	256 x 8	x					A,Z	I	100kHz	8	TE13	2000
CAT24C02AZJ14	256 x 8		x				A,Z	†	100kHz	14		56
CAT24C02AZJ14-TE7	256 x 8		x				A,Z	†	100kHz	14	TE7	500
CAT24C02AZJ14-TE13	256 x 8		x				A,Z	†	100kHz	14	TE13	2000
CAT24C02AZJ14I	256 x 8		x				A,Z	I	100kHz	14		56
CAT24C02AZJ14I-TE7	256 x 8		x				A,Z	I	100kHz	14	TE7	500
CAT24C02AZJ14I-TE13	256 x 8		x				A,Z	I	100kHz	14	TE13	2000
CAT24LC02AP	256 x 8					x	L,A	†	100kHz	8		50
CAT24LC02API	256 x 8					x	L,A	I	100kHz	8		50
CAT24LC02AJ	256 x 8	x					L,A	†	100kHz	8		100
CAT24LC02AJ-TE7	256 x 8	x					L,A	†	100kHz	8	TE7	500
CAT24LC02AJ-TE13	256 x 8	x					L,A	†	100kHz	8	TE13	2000
CAT24LC02AJI	256 x 8	x					L,A	I	100kHz	8		100
CAT24LC02AJI-TE7	256 x 8	x					L,A	I	100kHz	8	TE7	500
CAT24LC02AJI-TE13	256 x 8	x					L,A	I	100kHz	8	TE13	2000
CAT24LC02AJ14	256 x 8		x				L,A	†	100kHz	14		56
CAT24LC02AJ14-TE7	256 x 8		x				L,A	†	100kHz	14	TE7	500
CAT24LC02AJ14-TE13	256 x 8		x				L,A	†	100kHz	14	TE13	2000
CAT24LC02AJ14I	256 x 8		x				L,A	I	100kHz	14		56
CAT24LC02AJ14I-TE7	256 x 8		x				L,A	I	100kHz	14	TE7	500
CAT24LC02AJ14I-TE13	256 x 8		x				L,A	I	100kHz	14	TE13	2000
CAT24LC02AZP	256 x 8					x	L,A,Z	†	100kHz	8		50
CAT24LC02AZPI	256 x 8					x	L,A,Z	I	100kHz	8		50
CAT24LC02AZJ	256 x 8	x					L,A,Z	†	100kHz	8		100
CAT24LC02AZJ-TE7	256 x 8	x					L,A,Z	†	100kHz	8	TE7	500
CAT24LC02AZJ-TE13	256 x 8	x					L,A,Z	†	100kHz	8	TE13	2000
CAT24LC02AZJI	256 x 8	x					L,A,Z	I	100kHz	8		100
CAT24LC02AZJI-TE7	256 x 8	x					L,A,Z	I	100kHz	8	TE7	500
CAT24LC02AZJI-TE13	256 x 8	x					L,A,Z	I	100kHz	8	TE13	2000
CAT24LC02AZJ14	256 x 8		x				L,A,Z	†	100kHz	14		56
CAT24LC02AZJ14-TE7	256 x 8		x				L,A,Z	†	100kHz	14	TE7	500
CAT24LC02AZJ14-TE13	256 x 8		x				L,A,Z	†	100kHz	14	TE13	2000
CAT24LC02AZJ14I	256 x 8		x				L,A,Z	I	100kHz	14		56
CAT24LC02AZJ14I-TE7	256 x 8		x				L,A,Z	I	100kHz	14	TE7	500
CAT24LC02AZJ14I-TE13	256 x 8		x				L,A,Z	I	100kHz	14	TE13	2000

Note:
1) Contact factory for High Endurance device availability.

Key:

†	=	Blank = Commercial = 0°C to +70°C
I	=	Industrial = –40°C to +85°C
A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
Z	=	Zero Power™
J	=	S.O. (JEDEC)
J14	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
P	=	Plastic DIP
S	=	S.O. Non-Rotated (JEDEC)
TE7	=	Tape Embossed 7" Reel, Min. Order 500 Pcs/Reel
TE13	=	Tape Embossed 13" Reel, Min. Order 2000 Pcs/Reel

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SERIAL E²PROMs

2-Wire Bus Structure (Data Book Section 2)

Device Order Number	Org.	Package J	J14	S	K	P	Special Features	Temp Range	Clock Freq.	# of Pins	Tape & Reel	Rail Qty.
CAT24C04P	512 x 8					x		†	100kHz	8		50
CAT24C04PI	512 x 8					x		I	100kHz	8		50
CAT24C04J	512 x 8	x						†	100kHz	8		100
CAT24C04J-TE7	512 x 8	x						†	100kHz	8	TE7	500
CAT24C04J-TE13	512 x 8	x						†	100kHz	8	TE13	2000
CAT24C04JI	512 x 8	x						I	100kHz	8		100
CAT24C04JI-TE7	512 x 8	x						I	100kHz	8	TE7	500
CAT24C04JI-TE13	512 x 8	x						I	100kHz	8	TE13	2000
CAT24C04J14	512 x 8		x					†	100kHz	14		56
CAT24C04J14-TE7	512 x 8		x					†	100kHz	14	TE7	500
CAT24C04J14-TE13	512 x 8		x					†	100kHz	14	TE13	2000
CAT24C04J14I	512 x 8		x					I	100kHz	14		56
CAT24C04J14I-TE7	512 x 8		x					I	100kHz	14	TE7	500
CAT24C04J14I-TE13	512 x 8		x					I	100kHz	14	TE13	2000
CAT24C04ZP	512 x 8					x	Z	†	100kHz	8		50
CAT24C04ZPI	512 x 8					x	Z	I	100kHz	8		50
CAT24C04ZJ	512 x 8	x					Z	†	100kHz	8		100
CAT24C04ZJ-TE7	512 x 8	x					Z	†	100kHz	8	TE7	500
CAT24C04ZJ-TE13	512 x 8	x					Z	†	100kHz	8	TE13	2000
CAT24C04ZJI	512 x 8	x					Z	I	100kHz	8		100
CAT24C04ZJI-TE7	512 x 8	x					Z	I	100kHz	8	TE7	500
CAT24C04ZJI-TE13	512 x 8	x					Z	I	100kHz	8	TE13	2000
CAT24C04ZJ14	512 x 8		x				Z	†	100kHz	14		56
CAT24C04ZJ14-TE7	512 x 8		x				Z	†	100kHz	14	TE7	500
CAT24C04ZJ14-TE13	512 x 8		x				Z	†	100kHz	14	TE13	2000
CAT24C04ZJ14I	512 x 8		x				Z	I	100kHz	14		56
CAT24C04ZJ14I-TE7	512 x 8		x				Z	I	100kHz	14	TE7	500
CAT24C04ZJ14I-TE13	512 x 8		x				Z	I	100kHz	14	TE13	2000
CAT24LC04P	512 x 8					x	L	†	100kHz	8		50
CAT24LC04PI	512 x 8					x	L	I	100kHz	8		50
CAT24LC04J	512 x 8	x					L	†	100kHz	8		100
CAT24LC04J-TE7	512 x 8	x					L	†	100kHz	8	TE7	500
CAT24LC04J-TE13	512 x 8	x					L	†	100kHz	8	TE13	2000
CAT24LC04JI	512 x 8	x					L	I	100kHz	8		100
CAT24LC04JI-TE7	512 x 8	x					L	I	100kHz	8	TE7	500
CAT24LC04JI-TE13	512 x 8	x					L	I	100kHz	8	TE13	2000
CAT24LC04J14	512 x 8		x				L	†	100kHz	14		56
CAT24LC04J14-TE7	512 x 8		x				L	†	100kHz	14	TE7	500
CAT24LC04J14-TE13	512 x 8		x				L	†	100kHz	14	TE13	2000
CAT24LC04J14I	512 x 8		x				L	I	100kHz	14		56
CAT24LC04J14I-TE7	512 x 8		x				L	I	100kHz	14	TE7	500
CAT24LC04J14I-TE13	512 x 8		x				L	I	100kHz	14	TE13	2000

Note:
(1) Contact factory for High Endurance device availability.

Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C
A = Advanced Device or Special Assembly
B = Advanced Device
L = Low Voltage
Z = Zero Power™
J = S.O. (JEDEC)
J14 = S.O. (JEDEC)
K = S.O. (EIAJ)
P = Plastic DIP
S = S.O. Non-Rotated (JEDEC)
TE7 = Tape Embossed 7" Reel, Min. Order 500 Pcs/Reel
TE13 = Tape Embossed 13" Reel, Min. Order 2000 Pcs/Reel

ERIAL E²PROMs

Wire Bus Structure (Data Book Section 2)

Device Order Number	Org.	Package J	J14	S	K	P	Special Features	Temp Range	Clock Freq.	# of Pins	Tape & Reel	Rail Qty.
CAT24LC04ZP	512 x 8					x	L,Z	†	100kHz	8		50
CAT24LC04ZPI	512 x 8					x	L,Z	I	100kHz	8		50
CAT24LC04ZJ	512 x 8	x					L,Z	†	100kHz	8		100
CAT24LC04ZJ-TE7	512 x 8	x					L,Z	†	100kHz	8	TE7	500
CAT24LC04ZJ-TE13	512 x 8	x					L,Z	†	100kHz	8	TE13	2000
CAT24LC04ZJI	512 x 8	x					L,Z	I	100kHz	8		100
CAT24LC04ZJI-TE7	512 x 8	x					L,Z	I	100kHz	8	TE7	500
CAT24LC04ZJI-TE13	512 x 8	x					L,Z	I	100kHz	8	TE13	2000
CAT24LC04ZJ14	512 x 8		x				L,Z	†	100kHz	14		56
CAT24LC04ZJ14-TE7	512 x 8		x				L,Z	†	100kHz	14	TE7	500
CAT24LC04ZJ14-TE13	512 x 8		x				L,Z	†	100kHz	14	TE13	2000
CAT24LC04ZJ14I	512 x 8		x				L,Z	I	100kHz	14		56
CAT24LC04ZJ14I-TE7	512 x 8		x				L,Z	I	100kHz	14	TE7	500
CAT24LC04ZJ14I-TE13	512 x 8		x				L,Z	I	100kHz	14	TE13	2000
CAT24C08P	1024 x 8					x		†	100kHz	8		50
CAT24C08PI	1024 x 8					x		I	100kHz	8		50
CAT24C08J	1024 x 8	x						†	100kHz	8		100
CAT24C08J-TE7	1024 x 8	x						†	100kHz	8	TE7	500
CAT24C08J-TE13	1024 x 8	x						†	100kHz	8	TE13	2000
CAT24C08JI	1024 x 8	x						I	100kHz	8		100
CAT24C08JI-TE7	1024 x 8	x						I	100kHz	8	TE7	500
CAT24C08JI-TE13	1024 x 8	x						I	100kHz	8	TE13	2000
CAT24C08J14	1024 x 8		x					†	100kHz	14		56
CAT24C08J14-TE7	1024 x 8		x					†	100kHz	14	TE7	500
CAT24C08J14-TE13	1024 x 8		x					†	100kHz	14	TE13	2000
CAT24C08J14I	1024 x 8		x					I	100kHz	14		56
CAT24C08J14I-TE7	1024 x 8		x					I	100kHz	14	TE7	500
CAT24C08J14I-TE13	1024 x 8		x					I	100kHz	14	TE13	2000
CAT24C08ZP	1024 x 8					x	Z	†	100kHz	8		50
CAT24C08ZPI	1024 x 8					x	Z	I	100kHz	8		50
CAT24C08ZJ	1024 x 8	x					Z	†	100kHz	8		100
CAT24C08ZJ-TE7	1024 x 8	x					Z	†	100kHz	8	TE7	500
CAT24C08ZJ-TE13	1024 x 8	x					Z	†	100kHz	8	TE13	2000
CAT24C08ZJI	1024 x 8	x					Z	I	100kHz	8		100
CAT24C08ZJI-TE7	1024 x 8	x					Z	I	100kHz	8	TE7	500
CAT24C08ZJI-TE13	1024 x 8	x					Z	I	100kHz	8	TE13	2000
CAT24C08ZJ14	1024 x 8		x				Z	†	100kHz	14		56
CAT24C08ZJ14-TE7	1024 x 8		x				Z	†	100kHz	14	TE7	500
CAT24C08ZJ14-TE13	1024 x 8		x				Z	†	100kHz	14	TE13	2000
CAT24C08ZJ14I	1024 x 8		x				Z	I	100kHz	14		56
CAT24C08ZJ14I-TE7	1024 x 8		x				Z	I	100kHz	14	TE7	500
CAT24C08ZJ14I-TE13	1024 x 8		x				Z	I	100kHz	14	TE13	2000

Note:
(1) Contact factory for High Endurance device availability.

Key:

†	=	Blank = Commercial = 0°C to +70°C
I	=	Industrial = –40°C to +85°C
A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
Z	=	Zero Power™
J	=	S.O. (JEDEC)
J14	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
P	=	Plastic DIP
S	=	S.O. Non-Rotated (JEDEC)
TE7	=	Tape Embossed 7" Reel, Min. Order 500 Pcs/Reel
TE13	=	Tape Embossed 13" Reel, Min. Order 2000 Pcs/Reel

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SERIAL E²PROMs

2-Wire Bus Structure (Data Book Section 2)

Device Order Number	Org.	Package					Special Features	Temp Range	Clock Freq.	# of Pins	Tape & Reel	Rail Qty.
		J	J14	S	K	P						
CAT24LC08P	1024 x 8					x	L	†	100kHz	8		50
CAT24LC08PI	1024 x 8					x	L	I	100kHz	8		50
CAT24LC08J	1024 x 8	x					L	†	100kHz	8		100
CAT24LC08J-TE7	1024 x 8	x					L	†	100kHz	8	TE7	500
CAT24LC08J-TE13	1024 x 8	x					L	†	100kHz	8	TE13	2000
CAT24LC08JI	1024 x 8	x					L	I	100kHz	8		100
CAT24LC08JI-TE7	1024 x 8	x					L	I	100kHz	8	TE7	500
CAT24LC08JI-TE13	1024 x 8	x					L	I	100kHz	8	TE13	2000
CAT24LC08J14	1024 x 8		x				L	†	100kHz	14		56
CAT24LC08J14-TE7	1024 x 8		x				L	†	100kHz	14	TE7	500
CAT24LC08J14-TE13	1024 x 8		x				L	†	100kHz	14	TE13	2000
CAT24LC08J14I	1024 x 8		x				L	I	100kHz	14		56
CAT24LC08J14I-TE7	1024 x 8		x				L	I	100kHz	14	TE7	500
CAT24LC08J14I-TE13	1024 x 8		x				L	I	100kHz	14	TE13	2000
CAT24LC08ZP	1024 x 8					x	L,Z	†	100kHz	8		50
CAT24LC08ZPI	1024 x 8					x	L,Z	I	100kHz	8		50
CAT24LC08ZJ	1024 x 8	x					L,Z	†	100kHz	8		100
CAT24LC08ZJ-TE7	1024 x 8	x					L,Z	†	100kHz	8	TE7	500
CAT24LC08ZJ-TE13	1024 x 8	x					L,Z	†	100kHz	8	TE13	2000
CAT24LC08ZJI	1024 x 8	x					L,Z	I	100kHz	8		100
CAT24LC08ZJI-TE7	1024 x 8	x					L,Z	I	100kHz	8	TE7	500
CAT24LC08ZJI-TE13	1024 x 8	x					L,Z	I	100kHz	8	TE13	2000
CAT24LC08ZJ14	1024 x 8		x				L,Z	†	100kHz	14		56
CAT24LC08ZJ14-TE7	1024 x 8		x				L,Z	†	100kHz	14	TE7	500
CAT24LC08ZJ14-TE13	1024 x 8		x				L,Z	†	100kHz	14	TE13	2000
CAT24LC08ZJ14I	1024 x 8		x				L,Z	I	100kHz	14		56
CAT24LC08ZJ14I-TE7	1024 x 8		x				L,Z	I	100kHz	14	TE7	500
CAT24LC08ZJ14I-TE13	1024 x 8		x				L,Z	I	100kHz	14	TE13	2000
CAT24C16P	2048 x 8					x		†	100kHz	8		50
CAT24C16PI	2048 x 8					x		I	100kHz	8		50
CAT24C16J	2048 x 8	x						†	100kHz	8		100
CAT24C16J-TE7	2048 x 8	x						†	100kHz	8	TE7	500
CAT24C16J-TE13	2048 x 8	x						†	100kHz	8	TE13	2000
CAT24C16JI	2048 x 8	x						I	100kHz	8		100
CAT24C16JI-TE7	2048 x 8	x						I	100kHz	8	TE7	500
CAT24C16JI-TE13	2048 x 8	x						I	100kHz	8	TE13	2000
CAT24C16J14	2048 x 8		x					†	100kHz	14		56
CAT24C16J14-TE7	2048 x 8		x					†	100kHz	14	TE7	500
CAT24C16J14-TE13	2048 x 8		x					†	100kHz	14	TE13	2000
CAT24C16J14I	2048 x 8		x					I	100kHz	14		56
CAT24C16J14I-TE7	2048 x 8		x					I	100kHz	14	TE7	500
CAT24C16J14I-TE13	2048 x 8		x					I	100kHz	14	TE13	2000

Note:
(1) Contact factory for High Endurance device availability.

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†	=	Blank = Commercial = 0°C to +70°C
I	=	Industrial = –40°C to +85°C
A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
Z	=	Zero Power™
J	=	S.O. (JEDEC)
J14	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
P	=	Plastic DIP
S	=	S.O. Non-Rotated (JEDEC)
TE7	=	Tape Embossed 7" Reel, Min. Order 500 Pcs/Reel
TE13	=	Tape Embossed 13" Reel, Min. Order 2000 Pcs/Reel

ERIAL E²PROMs

Wire Bus Structure (Data Book Section 2)

Device Order Number	Org.	Package J	J14	S	K	P	Special Features	Temp Range	Clock Freq.	# of Pins	Tape & Reel	Rail Qty.
CAT24C16ZP	2048 x 8					x	Z	†	100kHz	8		50
CAT24C16ZPI	2048 x 8					x	Z	I	100kHz	8		50
CAT24C16ZJ	2048 x 8	x					Z	†	100kHz	8		100
CAT24C16ZJ-TE7	2048 x 8	x					Z	†	100kHz	8	TE7	500
CAT24C16ZJ-TE13	2048 x 8	x					Z	†	100kHz	8	TE13	2000
CAT24C16ZJI	2048 x 8	x					Z	I	100kHz	8		100
CAT24C16ZJI-TE7	2048 x 8	x					Z	I	100kHz	8	TE7	500
CAT24C16ZJI-TE13	2048 x 8	x					Z	I	100kHz	8	TE13	2000
CAT24C16ZJ14	2048 x 8		x				Z	†	100kHz	14		56
CAT24C16ZJ14-TE7	2048 x 8		x				Z	†	100kHz	14	TE7	500
CAT24C16ZJ14-TE13	2048 x 8		x				Z	†	100kHz	14	TE13	2000
CAT24C16ZJ14I	2048 x 8		x				Z	I	100kHz	14		56
CAT24C16ZJ14I-TE7	2048 x 8		x				Z	I	100kHz	14	TE7	500
CAT24C16ZJ14I-TE13	2048 x 8		x				Z	I	100kHz	14	TE13	2000
CAT24LC16P	2048 x 8					x	L	†	100kHz	8		50
CAT24LC16PI	2048 x 8					x	L	I	100kHz	8		50
CAT24LC16J	2048 x 8	x					L	†	100kHz	8		100
CAT24LC16J-TE7	2048 x 8	x					L	†	100kHz	8	TE7	500
CAT24LC16J-TE13	2048 x 8	x					L	†	100kHz	8	TE13	2000
CAT24LC16JI	2048 x 8	x					L	I	100kHz	8		100
CAT24LC16JI-TE7	2048 x 8	x					L	I	100kHz	8	TE7	500
CAT24LC16JI-TE13	2048 x 8	x					L	I	100kHz	8	TE13	2000
CAT24LC16J14	2048 x 8		x				L	†	100kHz	14		56
CAT24LC16J14-TE7	2048 x 8		x				L	†	100kHz	14	TE7	500
CAT24LC16J14-TE13	2048 x 8		x				L	†	100kHz	14	TE13	2000
CAT24LC16J14I	2048 x 8		x				L	I	100kHz	14		56
CAT24LC16J14I-TE7	2048 x 8		x				L	I	100kHz	14	TE7	500
CAT24LC16J14I-TE13	2048 x 8		x				L	I	100kHz	14	TE13	2000
CAT24LC16ZP	2048 x 8					x	L,Z	†	100kHz	8		50
CAT24LC16ZPI	2048 x 8					x	L,Z	I	100kHz	8		50
CAT24LC16ZJ	2048 x 8	x					L,Z	†	100kHz	8		100
CAT24LC16ZJ-TE7	2048 x 8	x					L,Z	†	100kHz	8	TE7	500
CAT24LC16ZJ-TE13	2048 x 8	x					L,Z	†	100kHz	8	TE13	2000
CAT24LC16ZJI	2048 x 8	x					L,Z	I	100kHz	8		100
CAT24LC16ZJI-TE7	2048 x 8	x					L,Z	I	100kHz	8	TE7	500
CAT24LC16ZJI-TE13	2048 x 8	x					L,Z	I	100kHz	8	TE13	2000
CAT24LC16ZJ14	2048 x 8		x				L,Z	†	100kHz	14		56
CAT24LC16ZJ14-TE7	2048 x 8		x				L,Z	†	100kHz	14	TE7	500
CAT24LC16ZJ14-TE13	2048 x 8		x				L,Z	†	100kHz	14	TE13	2000
CAT24LC16ZJ14I	2048 x 8		x				L,Z	I	100kHz	14		56
CAT24LC16ZJ14I-TE7	2048 x 8		x				L,Z	I	100kHz	14	TE7	500
CAT24LC16ZJ14I-TE13	2048 x 8		x				L,Z	I	100kHz	14	TE13	2000

lote:
l) Contact factory for High Endurance device availability.

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Z	=	Zero Power™
J	=	S.O. (JEDEC)
J14	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
P	=	Plastic DIP
S	=	S.O. Non-Rotated (JEDEC)
TE7	=	Tape Embossed 7" Reel, Min. Order 500 Pcs/Reel
TE13	=	Tape Embossed 13" Reel, Min. Order 2000 Pcs/Reel

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SERIAL E²PROMs

3-Wire Bus Structure (Data Book Section 3)

Device Order Number	Organization	Package					Special Features	Temp Range	Clock Freq.	# of Pins	Tape & Reel	Rail Qty.
		J	J14	S	K	P						
CAT93C46P	128 x 8/64 x 16					x		†	1 MHz	8		50
CAT93C46PI	128 x 8/64 x 16					x		I	1 MHz	8		50
CAT93C46K	128 x 8/64 x 16				x			†	1 MHz	8		94
CAT93C46K-TE7	128 x 8/64 x 16				x			†	1 MHz	8	TE7	500
CAT93C46K-TE13	128 x 8/64 x 16				x			†	1 MHz	8	TE13	2000
CAT93C46KI	128 x 8/64 x 16				x			I	1 MHz	8		94
CAT93C46KI-TE7	128 x 8/64 x 16				x			I	1 MHz	8	TE7	500
CAT93C46KI-TE13	128 x 8/64 x 16				x			I	1 MHz	8	TE13	2000
CAT93C46J	128 x 8/64 x 16	x						†	1 MHz	8		100
CAT93C46J-TE7	128 x 8/64 x 16	x						†	1 MHz	8	TE7	500
CAT93C46J-TE13	128 x 8/64 x 16	x						†	1 MHz	8	TE13	2000
CAT93C46JI	128 x 8/64 x 16	x						I	1 MHz	8		100
CAT93C46JI-TE7	128 x 8/64 x 16	x						I	1 MHz	8	TE7	500
CAT93C46JI-TE13	128 x 8/64 x 16	x						I	1 MHz	8	TE13	2000
CAT93C46S	128 x 8/64 x 16			x				†	1 MHz	8		100
CAT93C46S-TE7	128 x 8/64 x 16			x				†	1 MHz	8	TE7	500
CAT93C46S-TE13	128 x 8/64 x 16			x				†	1 MHz	8	TE13	2000
CAT93C46SI	128 x 8/64 x 16			x				I	1 MHz	8		100
CAT93C46SI-TE7	128 x 8/64 x 16			x				I	1 MHz	8	TE7	500
CAT93C46SI-TE13	128 x 8/64 x 16			x				I	1 MHz	8	TE13	2000
CAT93C46AP	64 x 16					x	A	†	1 MHz	8		50
CAT93C46API	64 x 16					x	A	I	1 MHz	8		50
CAT93C46AK	64 x 16				x		A	†	1 MHz	8		94
CAT93C46AK-TE7	64 x 16				x		A	†	1 MHz	8	TE7	500
CAT93C46AK-TE13	64 x 16				x		A	†	1 MHz	8	TE13	2000
CAT93C46AKI	64 x 16				x		A	I	1 MHz	8		94
CAT93C46AKI-TE7	64 x 16				x		A	I	1 MHz	8	TE7	500
CAT93C46AKI-TE13	64 x 16				x		A	I	1 MHz	8	TE13	2000
CAT93C46AJ	64 x 16	x					A	†	1 MHz	8		100
CAT93C46AJ-TE7	64 x 16	x					A	†	1 MHz	8	TE7	500
CAT93C46AJ-TE13	64 x 16	x					A	†	1 MHz	8	TE13	2000
CAT93C46AJI	64 x 16	x					A	I	1 MHz	8		100
CAT93C46AJI-TE7	64 x 16	x					A	I	1 MHz	8	TE7	500
CAT93C46AJI-TE13	64 x 16	x					A	I	1 MHz	8	TE13	2000
CAT93C46AS	64 x 16			x			A	†	1 MHz	8		100
CAT93C46AS-TE7	64 x 16			x			A	†	1 MHz	8	TE7	500
CAT93C46AS-TE13	64 x 16			x			A	†	1 MHz	8	TE13	2000
CAT93C46ASI	64 x 16			x			A	I	1 MHz	8		100
CAT93C46ASI-TE7	64 x 16			x			A	I	1 MHz	8	TE7	500
CAT93C46ASI-TE13	64 x 16			x			A	I	1 MHz	8	TE13	2000

Note:
(1) Contact factory for High Endurance device availability.

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A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
Z	=	Zero Power™
J	=	S.O. (JEDEC)
J14	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
P	=	Plastic DIP
S	=	S.O. Non-Rotated (JEDEC)
TE7	=	Tape Embossed 7" Reel, Min. Order 500 Pcs/Reel
TE13	=	Tape Embossed 13" Reel, Min. Order 2000 Pcs/Reel

:RIAL E²PROMs

Vire Bus Structure (Data Book Section 3)

Device Order Number	Organization	Package J	J14	S	K	P	Special Features	Temp Range	Clock Freq.	# of Pins	Tape & Reel	Rail Qty.
AT93C46BP	128 x 8/64 x 16					x	B	†	1 MHz	8		50
AT93C46BPI	128 x 8/64 x 16					x	B	I	1 MHz	8		50
AT93C46BK	128 x 8/64 x 16				x		B	†	1 MHz	8		94
AT93C46BK-TE7	128 x 8/64 x 16				x		B	†	1 MHz	8	TE7	500
AT93C46BK-TE13	128 x 8/64 x 16				x		B	†	1 MHz	8	TE13	2000
AT93C46BKI	128 x 8/64 x 16				x		B	I	1 MHz	8		94
AT93C46BKI-TE7	128 x 8/64 x 16				x		B	I	1 MHz	8	TE7	500
AT93C46BKI-TE13	128 x 8/64 x 16				x		B	I	1 MHz	8	TE13	2000
:AT93C46BJ	128 x 8/64 x 16	x					B	†	1 MHz	8		100
:AT93C46BJ-TE7	128 x 8/64 x 16	x					B	†	1 MHz	8	TE7	500
:AT93C46BJ-TE13	128 x 8/64 x 16	x					B	†	1 MHz	8	TE13	2000
:AT93C46BJI	128 x 8/64 x 16	x					B	I	1 MHz	8		100
:AT93C46BJI-TE7	128 x 8/64 x 16	x					B	I	1 MHz	8	TE7	500
:AT93C46BJI-TE13	128 x 8/64 x 16	x					B	I	1 MHz	8	TE13	2000
:AT93C46BS	128 x 8/64 x 16			x			B	†	1 MHz	8		100
:AT93C46BS-TE7	128 x 8/64 x 16			x			B	†	1 MHz	8	TE7	500
:AT93C46BS-TE13	128 x 8/64 x 16			x			B	†	1 MHz	8	TE13	2000
:AT93C46BSI	128 x 8/64 x 16			x			B	I	1 MHz	8		100
:AT93C46BSI-TE7	128 x 8/64 x 16			x			B	I	1 MHz	8	TE7	500
:AT93C46BSI-TE13	128 x 8/64 x 16			x			B	I	1 MHz	8	TE13	2000
:AT33C101P	128 x 8/64 x 16					x		†	250 kHz	8		50
:AT33C101PI	128 x 8/64 x 16					x		I	250 kHz	8		50
:AT33C101K	128 x 8/64 x 16				x			†	250 kHz	8		94
:AT33C101K-TE7	128 x 8/64 x 16				x			†	250 kHz	8	TE7	500
:AT33C101K-TE13	128 x 8/64 x 16				x			†	250 kHz	8	TE13	2000
:AT33C101KI	128 x 8/64 x 16				x			I	250 kHz	8		94
:AT33C101KI-TE7	128 x 8/64 x 16				x			I	250 kHz	8	TE7	500
:AT33C101KI-TE13	128 x 8/64 x 16				x			I	250 kHz	8	TE13	2000
:AT33C101J	128 x 8/64 x 16	x						†	250 kHz	8		100
:AT33C101J-TE7	128 x 8/64 x 16	x						†	250 kHz	8	TE7	500
:AT33C101J-TE13	128 x 8/64 x 16	x						†	250 kHz	8	TE13	2000
:AT33C101JI	128 x 8/64 x 16	x						I	250 kHz	8		100
:AT33C101JI-TE7	128 x 8/64 x 16	x						I	250 kHz	8	TE7	500
:AT33C101JI-TE13	128 x 8/64 x 16	x						I	250 kHz	8	TE13	2000
:AT33C101S	128 x 8/64 x 16			x				†	250 kHz	8		100
:AT33C101S-TE7	128 x 8/64 x 16			x				†	250 kHz	8	TE7	500
:AT33C101S-TE13	128 x 8/64 x 16			x				†	250 kHz	8	TE13	2000
:AT33C101SI	128 x 8/64 x 16			x				I	250 kHz	8		100
:AT33C101SI-TE7	128 x 8/64 x 16			x				I	250 kHz	8	TE7	500
:AT33C101SI-TE13	128 x 8/64 x 16			x				I	250 kHz	8	TE13	2000

ote:
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A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
Z	=	Zero Power™
J	=	S.O. (JEDEC)
J14	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
P	=	Plastic DIP
S	=	S.O. Non-Rotated (JEDEC)
TE7	=	Tape Embossed 7" Reel, Min. Order 500 Pcs/Reel
TE13	=	Tape Embossed 13" Reel, Min. Order 2000 Pcs/Reel

SERIAL E²PROMs

3-Wire Bus Structure (Data Book Section 3)

Device Order Number	Organization	Package					Special Features	Temp Range	Clock Freq.	# of Pins	Tape & Reel	Rai Qty
		J	J14	S	K	P						
CAT32C101P	128 x 8/64 x 16					x		†	250 kHz	8		50
CAT32C101K	128 x 8/64 x 16				x			†	250 kHz	8		94
CAT32C101K-TE7	128 x 8/64 x 16				x			†	250 kHz	8	TE7	500
CAT32C101K-TE13	128 x 8/64 x 16				x			†	250 kHz	8	TE13	200
CAT32C101J	128 x 8/64 x 16	x						†	250 kHz	8		100
CAT32C101J-TE7	128 x 8/64 x 16	x						†	250 kHz	8	TE7	500
CAT32C101J-TE13	128 x 8/64 x 16	x						†	250 kHz	8	TE13	200
CAT93C56P	256 x 8/128 x 16					x		†	1 MHz	8		50
CAT93C56PI	256 x 8/128 x 16					x		I	1 MHz	8		50
CAT93C56K	256 x 8/128 x 16				x			†	1 MHz	8		94
CAT93C56K-TE7	256 x 8/128 x 16				x			†	1 MHz	8	TE7	500
CAT93C56K-TE13	256 x 8/128 x 16				x			†	1 MHz	8	TE13	200
CAT93C56KI	256 x 8/128 x 16				x			I	1 MHz	8		94
CAT93C56KI-TE7	256 x 8/128 x 16				x			I	1 MHz	8	TE7	500
CAT93C56KI-TE13	256 x 8/128 x 16				x			I	1 MHz	8	TE13	200
CAT93C56S	256 x 8/128 x 16			x				†	1 MHz	8		100
CAT93C56S-TE7	256 x 8/128 x 16			x				†	1 MHz	8	TE7	500
CAT93C56S-TE13	256 x 8/128 x 16			x				†	1 MHz	8	TE13	200
CAT93C56SI	256 x 8/128 x 16			x				I	1 MHz	8		100
CAT93C56SI-TE7	256 x 8/128 x 16			x				I	1 MHz	8	TE7	500
CAT93C56SI-TE13	256 x 8/128 x 16			x				I	1 MHz	8	TE13	200
CAT93LC56P	256 x 8/128 x 16					x	L	†	250 kHz	8		50
CAT93LC56PI	256 x 8/128 x 16					x	L	I	250 kHz	8		50
CAT93LC56K	256 x 8/128 x 16				x		L	†	250 kHz	8		94
CAT93LC56K-TE7	256 x 8/128 x 16				x		L	†	250 kHz	8	TE7	500
CAT93LC56K-TE13	256 x 8/128 x 16				x		L	†	250 kHz	8	TE13	2000
CAT93LC56KI	256 x 8/128 x 16				x		L	I	250 kHz	8		94
CAT93LC56KI-TE7	256 x 8/128 x 16				x		L	I	250 kHz	8	TE7	500
CAT93LC56KI-TE13	256 x 8/128 x 16				x		L	I	250 kHz	8	TE13	2000
CAT93LC56S	256 x 8/128 x 16			x			L	†	250 kHz	8		100
CAT93LC56S-TE7	256 x 8/128 x 16			x			L	†	250 kHz	8	TE7	500
CAT93LC56S-TE13	256 x 8/128 x 16			x			L	†	250 kHz	8	TE13	2000
CAT93LC56SI	256 x 8/128 x 16			x			L	I	250 kHz	8		100
CAT93LC56SI-TE7	256 x 8/128 x 16			x			L	I	250 kHz	8	TE7	500
CAT93LC56SI-TE13	256 x 8/128 x 16			x			L	I	250 kHz	8	TE13	2000

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(1) Contact factory for High Endurance device availability.

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L	=	Low Voltage
Z	=	Zero Power™
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J14	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
P	=	Plastic DIP
S	=	S.O. Non-Rotated (JEDEC)
TE7	=	Tape Embossed 7" Reel, Min. Order 500 Pcs/Reel
TE13	=	Tape Embossed 13" Reel, Min. Order 2000 Pcs/Reel

ERIAL E²PROMs

Wire Bus Structure (Data Book Section 3)

Device Order Number	Organization	Package J	J14	S	K	P	Special Features	Temp Range	Clock Freq.	# of Pins	Tape & Reel	Rail Qty.
CAT35C102P	256 x 8/128 x 16					x		†	1 MHz	8		50
CAT35C102PI	256 x 8/128 x 16					x		I	1 MHz	8		50
CAT35C102K	256 x 8/128 x 16				x			†	1 MHz	8		94
CAT35C102K-TE7	256 x 8/128 x 16				x			†	1 MHz	8	TE7	500
CAT35C102K-TE13	256 x 8/128 x 16				x			†	1 MHz	8	TE13	2000
CAT35C102KI	256 x 8/128 x 16				x			I	1 MHz	8		94
CAT35C102KI-TE7	256 x 8/128 x 16				x			I	1 MHz	8	TE7	500
CAT35C102KI-TE13	256 x 8/128 x 16				x			I	1 MHz	8	TE13	2000
CAT35C102S	256 x 8/128 x 16			x				†	1 MHz	8		100
CAT35C102S-TE7	256 x 8/128 x 16			x				†	1 MHz	8	TE7	500
CAT35C102S-TE13	256 x 8/128 x 16			x				†	1 MHz	8	TE13	2000
CAT35C102SI	256 x 8/128 x 16			x				I	1 MHz	8		100
CAT35C102SI-TE7	256 x 8/128 x 16			x				I	1 MHz	8	TE7	500
CAT35C102SI-TE13	256 x 8/128 x 16			x				I	1 MHz	8	TE13	2000
CAT33C104P	512 x 8/256 x 16					x		†	250 kHz	8		50
CAT33C104PI	512 x 8/256 x 16					x		I	250 kHz	8		50
CAT33C104K	512 x 8/256 x 16				x			†	250 kHz	8		94
CAT33C104K-TE7	512 x 8/256 x 16				x			†	250 kHz	8	TE7	500
CAT33C104K-TE13	512 x 8/256 x 16				x			†	250 kHz	8	TE13	2000
CAT33C104KI	512 x 8/256 x 16				x			I	250 kHz	8		94
CAT33C104KI-TE7	512 x 8/256 x 16				x			I	250 kHz	8	TE7	500
CAT33C104KI-TE13	512 x 8/256 x 16				x			I	250 kHz	8	TE13	2000
CAT33C104S	512 x 8/256 x 16			x				†	250 kHz	8		100
CAT33C104S-TE7	512 x 8/256 x 16			x				†	250 kHz	8	TE7	500
CAT33C104S-TE13	512 x 8/256 x 16			x				†	250 kHz	8	TE13	2000
CAT33C104SI	512 x 8/256 x 16			x				I	250 kHz	8		100
CAT33C104SI-TE7	512 x 8/256 x 16			x				I	250 kHz	8	TE7	500
CAT33C104SI-TE13	512 x 8/256 x 16			x				I	250 kHz	8	TE13	2000
CAT35C104P	512 x 8/256 x 16					x		†	1 MHz	8		50
CAT35C104PI	512 x 8/256 x 16					x		I	1 MHz	8		50
CAT35C104K	512 x 8/256 x 16				x			†	1 MHz	8		94
CAT35C104K-TE7	512 x 8/256 x 16				x			†	1 MHz	8	TE7	500
CAT35C104K-TE13	512 x 8/256 x 16				x			†	1 MHz	8	TE13	2000
CAT35C104KI	512 x 8/256 x 16				x			I	1 MHz	8		94
CAT35C104KI-TE7	512 x 8/256 x 16				x			I	1 MHz	8	TE7	500
CAT35C104KI-TE13	512 x 8/256 x 16				x			I	1 MHz	8	TE13	2000
CAT35C104S	512 x 8/256 x 16			x				†	1 MHz	8		100
CAT35C104S-TE7	512 x 8/256 x 16			x				†	1 MHz	8	TE7	500
CAT35C104S-TE13	512 x 8/256 x 16			x				†	1 MHz	8	TE13	2000
CAT35C104SI	512 x 8/256 x 16			x				I	1 MHz	8		100
CAT35C104SI-TE7	512 x 8/256 x 16			x				I	1 MHz	8	TE7	500
CAT35C104SI-TE13	512 x 8/256 x 16			x				I	1 MHz	8	TE13	2000

lote:
1) Contact factory for High Endurance device availability.

Key:

†	=	Blank = Commercial = 0°C to +70°C
I	=	Industrial = –40°C to +85°C
A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
Z	=	Zero Power™
J	=	S.O. (JEDEC)
J14	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
P	=	Plastic DIP
S	=	S.O. Non-Rotated (JEDEC)
TE7	=	Tape Embossed 7" Reel, Min. Order 500 Pcs/Reel
TE13	=	Tape Embossed 13" Reel, Min. Order 2000 Pcs/Reel

SERIAL E²PROMs

3-Wire Bus Structure (Data Book Section 3)

Device Order Number	Organization	Package					Special Features	Temp Range	Clock Freq.	# of Pins	Tape & Reel	Rail Qty.
		J	J14	S	K	P						
CAT33C108P	1024 x 8/512 x 16					x		†	1 MHz	8		50
CAT33C108PI	1024 x 8/512 x 16					x		I	1 MHz	8		50
CAT33C108K	1024 x 8/512 x 16				x			†	1 MHz	8		94
CAT33C108K-TE7	1024 x 8/512 x 16				x			†	1 MHz	8	TE7	500
CAT33C108K-TE13	1024 x 8/512 x 16				x			†	1 MHz	8	TE13	2000
CAT33C108KI	1024 x 8/512 x 16				x			I	1 MHz	8		94
CAT33C108KI-TE7	1024 x 8/512 x 16				x			I	1 MHz	8	TE7	500
CAT33C108KI-TE13	1024 x 8/512 x 16				x			I	1 MHz	8	TE13	2000
CAT33C108S	1024 x 8/512 x 16			x				†	1 MHz	8		100
CAT33C108S-TE7	1024 x 8/512 x 16			x				†	1 MHz	8	TE7	500
CAT33C108S-TE13	1024 x 8/512 x 16			x				†	1 MHz	8	TE13	2000
CAT33C108SI	1024 x 8/512 x 16			x				I	1 MHz	8		100
CAT33C108SI-TE7	1024 x 8/512 x 16			x				I	1 MHz	8	TE7	500
CAT33C108SI-TE13	1024 x 8/512 x 16			x				I	1 MHz	8	TE13	2000
CAT35C108P	1024 x 8/512 x 16					x		†	3 MHz	8		50
CAT35C108PI	1024 x 8/512 x 16					x		I	3 MHz	8		50
CAT35C108K	1024 x 8/512 x 16				x			†	3 MHz	8		94
CAT35C108K-TE7	1024 x 8/512 x 16				x			†	3 MHz	8	TE7	500
CAT35C108K-TE13	1024 x 8/512 x 16				x			†	3 MHz	8	TE13	2000
CAT35C108KI	1024 x 8/512 x 16				x			I	3 MHz	8		94
CAT35C108KI-TE7	1024 x 8/512 x 16				x			I	3 MHz	8	TE7	500
CAT35C108KI-TE13	1024 x 8/512 x 16				x			I	3 MHz	8	TE13	2000
CAT35C108S	1024 x 8/512 x 16			x				†	3 MHz	8		100
CAT35C108S-TE7	1024 x 8/512 x 16			x				†	3 MHz	8	TE7	500
CAT35C108S-TE13	1024 x 8/512 x 16			x				†	3 MHz	8	TE13	2000
CAT35C108SI	1024 x 8/512 x 16			x				I	3 MHz	8		100
CAT35C108SI-TE7	1024 x 8/512 x 16			x				I	3 MHz	8	TE7	500
CAT35C108SI-TE13	1024 x 8/512 x 16			x				I	3 MHz	8	TE13	2000
CAT33C116P	2048 x 8/1024 x 16					x		†	1 MHz	8		50
CAT33C116PI	2048 x 8/1024 x 16					x		I	1 MHz	8		50
CAT33C116K	2048 x 8/1024 x 16				x			†	1 MHz	8		94
CAT33C116K-TE7	2048 x 8/1024 x 16				x			†	1 MHz	8	TE7	500
CAT33C116K-TE13	2048 x 8/1024 x 16				x			†	1 MHz	8	TE13	2000
CAT33C116KI	2048 x 8/1024 x 16				x			I	1 MHz	8		94
CAT33C116KI-TE7	2048 x 8/1024 x 16				x			I	1 MHz	8	TE7	500
CAT33C116KI-TE13	2048 x 8/1024 x 16				x			I	1 MHz	8	TE13	2000
CAT33C116S	2048 x 8/1024 x 16			x				†	1 MHz	8		100
CAT33C116S-TE7	2048 x 8/1024 x 16			x				†	1 MHz	8	TE7	500
CAT33C116S-TE13	2048 x 8/1024 x 16			x				†	1 MHz	8	TE13	2000
CAT33C116SI	2048 x 8/1024 x 16			x				I	1 MHz	8		100
CAT33C116SI-TE7	2048 x 8/1024 x 16			x				I	1 MHz	8	TE7	500
CAT33C116SI-TE13	2048 x 8/1024 x 16			x				I	1 MHz	8	TE13	2000

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A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
Z	=	Zero Power™
J	=	S.O. (JEDEC)
J14	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
P	=	Plastic DIP
S	=	S.O. Non-Rotated (JEDEC)
TE7	=	Tape Embossed 7" Reel, Min. Order 500 Pcs/Reel
TE13	=	Tape Embossed 13" Reel, Min. Order 2000 Pcs/Reel

ERIAL E²PROMs

Wire Bus Structure (Data Book Section 3)

Device Order Number	Organization	Package					Special Features	Temp Range	Clock Freq.	# of Pins	Tape & Reel	Rail Qty.
		J	J14	S	K	P						
CAT35C116P	2048 x 8/1024 x 16					x		†	3 MHz	8		50
CAT35C116PI	2048 x 8/1024 x 16					x		I	3 MHz	8		50
CAT35C116K	2048 x 8/1024 x 16				x			†	3 MHz	8		94
CAT35C116K-TE7	2048 x 8/1024 x 16				x			†	3 MHz	8	TE7	500
CAT35C116K-TE13	2048 x 8/1024 x 16				x			†	3 MHz	8	TE13	2000
CAT35C116KI	2048 x 8/1024 x 16				x			I	3 MHz	8		94
CAT35C116KI-TE7	2048 x 8/1024 x 16				x			I	3 MHz	8	TE7	500
CAT35C116KI-TE13	2048 x 8/1024 x 16				x			I	3 MHz	8	TE13	2000
CAT35C116S	2048 x 8/1024 x 16			x				†	3 MHz	8		100
CAT35C116S-TE7	2048 x 8/1024 x 16			x				†	3 MHz	8	TE7	500
CAT35C116S-TE13	2048 x 8/1024 x 16			x				†	3 MHz	8	TE13	2000
CAT35C116SI	2048 x 8/1024 x 16			x				I	3 MHz	8		100
CAT35C116SI-TE7	2048 x 8/1024 x 16			x				I	3 MHz	8	TE7	500
CAT35C116SI-TE13	2048 x 8/1024 x 16			x				I	3 MHz	8	TE13	2000

ote:
) Contact factory for High Endurance device availability.

Key:

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I	=	Industrial = –40°C to +85°C
A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
Z	=	Zero Power™
J	=	S.O. (JEDEC)
J14	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
P	=	Plastic DIP
S	=	S.O. Non-Rotated (JEDEC)
TE7	=	Tape Embossed 7" Reel, Min. Order 500 Pcs/Reel
TE13	=	Tape Embossed 13" Reel, Min. Order 2000 Pcs/Reel

SERIAL E²PROMs

SPI Bus Structure (Data Book Section 4)

Device Order Number	Organization	Package					Special Features	Temp Range	Clock Freq.	# of Pins	Tape & Reel	Rail Qty.
		J	J14	S	K	P						
CAT64LC10P	64 x 16					x	L	†	1 MHz	8		50
CAT64LC10PI	64 x 16					x	L	I	1 MHz	8		50
CAT64LC10J	64 x 16	x					L	†	1 MHz	8		100
CAT64LC10J-TE7	64 x 16	x					L	†	1 MHz	8	TE7	500
CAT64LC10J-TE13	64 x 16	x					L	†	1 MHz	8	TE13	2000
CAT64LC10JI	64 x 16	x					L	I	1 MHz	8		100
CAT64LC10JI-TE7	64 x 16	x					L	I	1 MHz	8	TE7	500
CAT64LC10JI-TE13	64 x 16	x					L	I	1 MHz	8	TE13	2000
CAT64LC10S	64 x 16			x			L	†	1 MHz	8		100
CAT64LC10S-TE7	64 x 16			x			L	†	1 MHz	8	TE7	500
CAT64LC10S-TE13	64 x 16			x			L	†	1 MHz	8	TE13	2000
CAT64LC10SI	64 x 16			x			L	I	1 MHz	8		100
CAT64LC10SI-TE7	64 x 16			x			L	I	1 MHz	8	TE7	500
CAT64LC10SI-TE13	64 x 16			x			L	I	1 MHz	8	TE13	2000
CAT64LC10ZP	64 x 16					x	L, Z	†	1 MHz	8		50
CAT64LC10ZPI	64 x 16					x	L, Z	I	1 MHz	8		50
CAT64LC10ZJ	64 x 16	x					L, Z	†	1 MHz	8		100
CAT64LC10ZJ-TE7	64 x 16	x					L, Z	†	1 MHz	8	TE7	500
CAT64LC10ZJ-TE13	64 x 16	x					L, Z	†	1 MHz	8	TE13	2000
CAT64LC10ZJI	64 x 16	x					L, Z	I	1 MHz	8		100
CAT64LC10ZJI-TE7	64 x 16	x					L, Z	I	1 MHz	8	TE7	500
CAT64LC10ZJI-TE13	64 x 16	x					L, Z	I	1 MHz	8	TE13	2000
CAT64LC10ZS	64 x 16			x			L, Z	†	1 MHz	8		100
CAT64LC10ZS-TE7	64 x 16			x			L, Z	†	1 MHz	8	TE7	500
CAT64LC10ZS-TE13	64 x 16			x			L, Z	†	1 MHz	8	TE13	2000
CAT64LC10ZSI	64 x 16			x			L, Z	I	1 MHz	8		100
CAT64LC10ZSI-TE7	64 x 16			x			L, Z	I	1 MHz	8	TE7	500
CAT64LC10ZSI-TE13	64 x 16			x			L, Z	I	1 MHz	8	TE13	2000
CAT64LC20P	128 x 16					x	L	†	1 MHz	8		50
CAT64LC20PI	128 x 16					x	L	I	1 MHz	8		50
CAT64LC20J	128 x 16	x					L	†	1 MHz	8		100
CAT64LC20J-TE7	128 x 16	x					L	†	1 MHz	8	TE7	500
CAT64LC20J-TE13	128 x 16	x					L	†	1 MHz	8	TE13	2000
CAT64LC20JI	128 x 16	x					L	I	1 MHz	8		100
CAT64LC20JI-TE7	128 x 16	x					L	I	1 MHz	8	TE7	500
CAT64LC20JI-TE13	128 x 16	x					L	I	1 MHz	8	TE13	2000
CAT64LC20S	128 x 16			x			L	†	1 MHz	8		100
CAT64LC20S-TE7	128 x 16			x			L	†	1 MHz	8	TE7	500
CAT64LC20S-TE13	128 x 16			x			L	†	1 MHz	8	TE13	2000
CAT64LC20SI	128 x 16			x			L	I	1 MHz	8		100
CAT64LC20SI-TE7	128 x 16			x			L	I	1 MHz	8	TE7	500
CAT64LC20SI-TE13	128 x 16			x			L	I	1 MHz	8	TE13	2000

Note:
(1) Contact factory for High Endurance device availability.

Key:

†	=	Blank = Commercial = 0°C to +70°C
I	=	Industrial = –40°C to +85°C
A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
Z	=	Zero Power™
J	=	S.O. (JEDEC)
J14	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
P	=	Plastic DIP
S	=	S.O. Non-Rotated (JEDEC)
TE7	=	Tape Embossed 7" Reel, Min. Order 500 Pcs/Reel
TE13	=	Tape Embossed 13" Reel, Min. Order 2000 Pcs/Reel

ERIAL E²PROMs

²I Bus Structure (Data Book Section 4)

Device Order Number	Organization	Package J	J14	S	K	P	Special Features	Temp Range	Clock Freq.	# of Pins	Tape & Reel	Rail Qty.
CAT64LC20ZP	128 x 16					x	L, Z	†	1 MHz	8		50
CAT64LC20ZPI	128 x 16					x	L, Z	I	1 MHz	8		50
CAT64LC20ZJ	128 x 16	x					L, Z	†	1 MHz	8		100
CAT64LC20ZJ-TE7	128 x 16	x					L, Z	†	1 MHz	8	TE7	500
CAT64LC20ZJ-TE13	128 x 16	x					L, Z	†	1 MHz	8	TE13	2000
CAT64LC20ZJI	128 x 16	x					L, Z	I	1 MHz	8		100
CAT64LC20ZJI-TE7	128 x 16	x					L, Z	I	1 MHz	8	TE7	500
CAT64LC20ZJI-TE13	128 x 16	x					L, Z	I	1 MHz	8	TE13	2000
CAT64LC20ZS	128 x 16			x			L, Z	†	1 MHz	8		100
CAT64LC20ZS-TE7	128 x 16			x			L, Z	†	1 MHz	8	TE7	500
CAT64LC20ZS-TE13	128 x 16			x			L, Z	†	1 MHz	8	TE13	2000
CAT64LC20ZSI	128 x 16			x			L, Z	I	1 MHz	8		100
CAT64LC20ZSI-TE7	128 x 16			x			L, Z	I	1 MHz	8	TE7	500
CAT64LC20ZSI-TE13	128 x 16			x			L, Z	I	1 MHz	8	TE13	2000
CAT64LC40P	256 x 16					x	L	†	1 MHz	8		50
CAT64LC40PI	256 x 16					x	L	I	1 MHz	8		50
CAT64LC40J	256 x 16	x					L	†	1 MHz	8		100
CAT64LC40J-TE7	256 x 16	x					L	†	1 MHz	8	TE7	500
CAT64LC40J-TE13	256 x 16	x					L	†	1 MHz	8	TE13	2000
CAT64LC40JI	256 x 16	x					L	I	1 MHz	8		100
CAT64LC40JI-TE7	256 x 16	x					L	I	1 MHz	8	TE7	500
CAT64LC40JI-TE13	256 x 16	x					L	I	1 MHz	8	TE13	2000
CAT64LC40S	256 x 16			x			L	†	1 MHz	8		100
CAT64LC40S-TE7	256 x 16			x			L	†	1 MHz	8	TE7	500
CAT64LC40S-TE13	256 x 16			x			L	†	1 MHz	8	TE13	2000
CAT64LC40SI	256 x 16			x			L	I	1 MHz	8		100
CAT64LC40SI-TE7	256 x 16			x			L	I	1 MHz	8	TE7	500
CAT64LC40SI-TE13	256 x 16			x			L	I	1 MHz	8	TE13	2000
CAT64LC40ZP	256 x 16					x	L, Z	†	1 MHz	8		50
CAT64LC40ZPI	256 x 16					x	L, Z	I	1 MHz	8		50
CAT64LC40ZJ	256 x 16	x					L, Z	†	1 MHz	8		100
CAT64LC40ZJ-TE7	256 x 16	x					L, Z	†	1 MHz	8	TE7	500
CAT64LC40ZJ-TE13	256 x 16	x					L, Z	†	1 MHz	8	TE13	2000
CAT64LC40ZJI	256 x 16	x					L, Z	I	1 MHz	8		100
CAT64LC40ZJI-TE7	256 x 16	x					L, Z	I	1 MHz	8	TE7	500
CAT64LC40ZJI-TE13	256 x 16	x					L, Z	I	1 MHz	8	TE13	2000
CAT64LC40ZS	256 x 16			x			L, Z	†	1 MHz	8		100
CAT64LC40ZS-TE7	256 x 16			x			L, Z	†	1 MHz	8	TE7	500
CAT64LC40ZS-TE13	256 x 16			x			L, Z	†	1 MHz	8	TE13	2000
CAT64LC40ZSI	256 x 16			x			L, Z	I	1 MHz	8		100
CAT64LC40ZSI-TE7	256 x 16			x			L, Z	I	1 MHz	8	TE7	500
CAT64LC40ZSI-TE13	256 x 16			x			L, Z	I	1 MHz	8	TE13	2000

Note:
(1) Contact factory for High Endurance device availability.

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A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
Z	=	Zero Power™
J	=	S.O. (JEDEC)
J14	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
P	=	Plastic DIP
S	=	S.O. Non-Rotated (JEDEC)
TE7	=	Tape Embossed 7" Reel, Min. Order 500 Pcs/Reel
TE13	=	Tape Embossed 13" Reel, Min. Order 2000 Pcs/Reel

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SERIAL E²PROMs

4-Wire Bus Structure (Data Book Section 5)

Device Order Number	Organization	Package					Special Features	Temp Range	Clock Freq.	# of Pins	Tape & Reel	Rail Qty.
		J	J14	S	K	P						
CAT59C11P	128 x 8/64 x 16					x		†	1 MHz	8		50
CAT59C11PI	128 x 8/64 x 16					x		I	1 MHz	8		50
CAT59C11K	128 x 8/64 x 16				x			†	1 MHz	8		94
CAT59C11K-TE7	128 x 8/64 x 16				x			†	1 MHz	8	TE7	500
CAT59C11K-TE13	128 x 8/64 x 16				x			†	1 MHz	8	TE13	2000
CAT59C11KI	128 x 8/64 x 16				x			I	1 MHz	8		94
CAT59C11KI-TE7	128 x 8/64 x 16				x			I	1 MHz	8	TE7	500
CAT59C11KI-TE13	128 x 8/64 x 16				x			I	1 MHz	8	TE13	2000
CAT35C202P	128 x 8/64 x 16					x		†	1 MHz	8		50
CAT35C202PI	128 x 8/64 x 16					x		I	1 MHz	8		50
CAT35C202K	128 x 8/64 x 16				x			†	1 MHz	8		94
CAT35C202K-TE7	128 x 8/64 x 16				x			†	1 MHz	8	TE7	500
CAT35C202K-TE13	128 x 8/64 x 16				x			†	1 MHz	8	TE13	2000
CAT35C202KI	128 x 8/64 x 16				x			I	1 MHz	8		94
CAT35C202KI-TE7	128 x 8/64 x 16				x			I	1 MHz	8	TE7	500
CAT35C202KI-TE13	128 x 8/64 x 16				x			I	1 MHz	8	TE13	2000

Note:
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A	=	Advanced Device or Special Assembly
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L	=	Low Voltage
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J14	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
P	=	Plastic DIP
S	=	S.O. Non-Rotated (JEDEC)
TE7	=	Tape Embossed 7" Reel, Min. Order 500 Pcs/Reel
TE13	=	Tape Embossed 13" Reel, Min. Order 2000 Pcs/Reel

ECURE ACCESS SERIAL E²PROMs (Data Book Section 6)

Device Order Number	Organization	Package					Special Features	Temp Range	Clock Freq.	# of Pins	Tape & Reel	Rail Qty.
		J	J14	S	K	P						
CAT33C704P	512 x 8/256 x 16					x		†	1 MHz	8		50
CAT33C704PI	512 x 8/256 x 16					x		I	1 MHz	8		50
CAT33C704J	512 x 8/256 x 16	x						†	1 MHz	16		47
CAT33C704J-TE7	512 x 8/256 x 16	x						†	1 MHz	16	TE7	250
CAT33C704J-TE13	512 x 8/256 x 16	x						†	1 MHz	16	TE13	1000
CAT33C704JI	512 x 8/256 x 16	x						I	1 MHz	16		47
CAT33C704JI-TE7	512 x 8/256 x 16	x						I	1 MHz	16	TE7	250
CAT33C704JI-TE13	512 x 8/256 x 16	x						I	1 MHz	16	TE13	1000
CAT35C704P	512 x 8/256 x 16					x		†	3 MHz	8		50
CAT35C704PI	512 x 8/256 x 16					x		I	3 MHz	8		50
CAT35C704J	512 x 8/256 x 16	x						†	3 MHz	16		47
CAT35C704J-TE7	512 x 8/256 x 16	x						†	3 MHz	16	TE7	250
CAT35C704J-TE13	512 x 8/256 x 16	x						†	3 MHz	16	TE13	1000
CAT35C704JI	512 x 8/256 x 16	x						I	3 MHz	16		47
CAT35C704JI-TE7	512 x 8/256 x 16	x						I	3 MHz	16	TE7	250
CAT35C704JI-TE13	512 x 8/256 x 16	x						I	3 MHz	16	TE13	1000
CAT33C804AP	512 x 8/256 x 16					x	A	†	5 MHz	8		50
CAT33C804API	512 x 8/256 x 16					x	A	I	5 MHz	8		50
CAT33C804AJ	512 x 8/256 x 16	x					A	†	5 MHz	16		47
CAT33C804AJ-TE7	512 x 8/256 x 16	x					A	†	5 MHz	16	TE7	250
CAT33C804AJ-TE13	512 x 8/256 x 16	x					A	†	5 MHz	16	TE13	1000
CAT33C804AJI	512 x 8/256 x 16	x					A	I	5 MHz	16		47
CAT33C804AJI-TE7	512 x 8/256 x 16	x					A	I	5 MHz	16	TE7	250
CAT33C804AJI-TE13	512 x 8/256 x 16	x					A	I	5 MHz	16	TE13	1000
CAT33C804BP	512 x 8/256 x 16					x	B	†	5 MHz	8		50
CAT33C804BPI	512 x 8/256 x 16					x	B	I	5 MHz	8		50
CAT33C804BJ	512 x 8/256 x 16	x					B	†	5 MHz	16		47
CAT33C804BJ-TE7	512 x 8/256 x 16	x					B	†	5 MHz	16	TE7	250
CAT33C804BJ-TE13	512 x 8/256 x 16	x					B	†	5 MHz	16	TE13	1000
CAT33C804BJI	512 x 8/256 x 16	x					B	I	5 MHz	16		47
CAT33C804BJI-TE7	512 x 8/256 x 16	x					B	I	5 MHz	16	TE7	250
CAT33C804BJI-TE13	512 x 8/256 x 16	x					B	I	5 MHz	16	TE13	1000

ote:
) Contact factory for High Endurance device availability.

Key:

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I	=	Industrial = –40°C to +85°C
A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
Z	=	Zero Power™
J	=	S.O. (JEDEC)
J14	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
P	=	Plastic DIP
S	=	S.O. Non-Rotated (JEDEC)
TE7	=	Tape Embossed 7" Reel, Min. Order 500 Pcs/Reel
TE13	=	Tape Embossed 13" Reel, Min. Order 2000 Pcs/Reel

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SECURE ACCESS SERIAL E²PROMs (Data Book Section 6)

Device Order Number	Organization	Package					Special Features	Temp Range	Clock Freq.	# of Pins	Tape & Reel	Rail Qty.
		J	J14	S	K	P						
CAT35C804AP	512 x 8/256 x 16					x	A	†	5 MHz	8		50
CAT35C804API	512 x 8/256 x 16					x	A	I	5 MHz	8		50
CAT35C804AJ	512 x 8/256 x 16	x					A	†	5 MHz	16		47
CAT35C804AJ-TE7	512 x 8/256 x 16	x					A	†	5 MHz	16	TE7	250
CAT35C804AJ-TE13	512 x 8/256 x 16	x					A	†	5 MHz	16	TE13	1000
CAT35C804AJI	512 x 8/256 x 16	x					A	I	5 MHz	16		47
CAT35C804AJI-TE7	512 x 8/256 x 16	x					A	I	5 MHz	16	TE7	250
CAT35C804AJI-TE13	512 x 8/256 x 16	x					A	I	5 MHz	16	TE13	1000
CAT35C804BP	512 x 8/256 x 16					x	B	†	5 MHz	8		50
CAT35C804BPI	512 x 8/256 x 16					x	B	I	5 MHz	8		50
CAT35C804BJ	512 x 8/256 x 16	x					B	†	5 MHz	16		47
CAT35C804BJ-TE7	512 x 8/256 x 16	x					B	†	5 MHz	16	TE7	250
CAT35C804BJ-TE13	512 x 8/256 x 16	x					B	†	5 MHz	16	TE13	1000
CAT35C804BJI	512 x 8/256 x 16	x					B	I	5 MHz	16		47
CAT35C804BJI-TE7	512 x 8/256 x 16	x					B	I	5 MHz	16	TE7	250
CAT35C804BJI-TE13	512 x 8/256 x 16	x					B	I	5 MHz	16	TE13	1000

Note:
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L	=	Low Voltage
Z	=	Zero Power™
J	=	S.O. (JEDEC)
J14	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
P	=	Plastic DIP
S	=	S.O. Non-Rotated (JEDEC)
TE7	=	Tape Embossed 7" Reel, Min. Order 500 Pcs/Reel
TE13	=	Tape Embossed 13" Reel, Min. Order 2000 Pcs/Ree

ARALLEL E²PROMs (Data Book Section 7)

Device Order Number	Organization	Package C	D	E	J	K	N	P	T	Special Features	Temp Range	Access Time (ns)	# of Pins	Rail Qty
CAT28C16AP-20	2K x 8							x			†	200	24	16
CAT28C16API-20	2K x 8							x			I	200	24	16
CAT28C16AK-20	2K x 8					x					†	200	24	30
CAT28C16AKI-20	2K x 8					x					I	200	24	30
CAT28C16AJ-20	2K x 8				x						†	200	24	30
CAT28C16AJI-20	2K x 8				x						I	200	24	30
CAT28C16AN-20	2K x 8						x				†	200	32	32
CAT28C16ANI-20	2K x 8						x				I	200	32	32
CAT28C17AP-20	2K x 8							x			†	200	28	14
CAT28C17API-20	2K x 8							x			I	200	28	14
CAT28C17AK-20	2K x 8					x					†	200	28	27
CAT28C17AKI-20	2K x 8					x					I	200	28	27
CAT28C17AJ-20	2K x 8				x						†	200	28	27
CAT28C17AJI-20	2K x 8				x						I	200	28	27
CAT28C17AN-20	2K x 8						x				†	200	32	32
CAT28C17ANI-20	2K x 8						x				I	200	32	32
CAT28C16V3P-70	2K x 8							x		V	†	700	24	16
CAT28C16V3K-70	2K x 8					x				V	†	700	24	30
CAT28C16V3N-70	2K x 8						x			V	†	700	32	32
CAT28C64AP-15	8K x 8							x			†	150	28	14
CAT28C64AP-20	8K x 8							x			†	200	28	14
CAT28C64AP-25	8K x 8							x			†	250	28	14
CAT28C64API-15	8K x 8							x			I	150	28	14
CAT28C64API-20	8K x 8							x			I	200	28	14
CAT28C64API-25	8K x 8							x			I	250	28	14
CAT28C64AN-15	8K x 8						x				†	150	32	32
CAT28C64AN-20	8K x 8						x				†	200	32	32
CAT28C64AN-25	8K x 8						x				†	250	32	32
CAT28C64ANI-15	8K x 8						x				I	150	32	32
CAT28C64ANI-20	8K x 8						x				I	200	32	32
CAT28C64ANI-25	8K x 8						x				I	250	32	32
CAT28C64AJ-15	8K x 8				x						†	150	28	27
CAT28C64AJ-20	8K x 8				x						†	200	28	27
CAT28C64AJ-25	8K x 8				x						†	250	28	27
CAT28C64AJI-15	8K x 8				x						I	150	28	27
CAT28C64AJI-20	8K x 8				x						I	200	28	27
CAT28C64AJI-25	8K x 8				x						I	250	28	27
CAT28C64AK-15	8K x 8					x					†	150	28	27
CAT28C64AK-20	8K x 8					x					†	200	28	27
CAT28C64AK-25	8K x 8					x					†	250	28	27
CAT28C64AKI-15	8K x 8					x					I	150	28	27
CAT28C64AKI-20	8K x 8					x					I	200	28	27
CAT28C64AKI-25	8K x 8					x					I	250	28	27

ote:
) Contact factory for High Endurance device availability.

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I	=	Industrial = –40°C to +85°C
A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
V	=	Special Voltage
C	=	Sidebraze
D	=	CERDIP
E	=	LCC
J	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
N	=	PLCC
P	=	Plastic DIP
T	=	TSOP

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PARALLEL E²PROMs (Data Book Section 7)

Device Order Number	Organization	Package								Special Features	Temp Range	Access Time (ns)	# of Pins	Rail Qty
		C	D	E	J	K	N	P	T					
CAT28C65AP-15	8K x 8							x			†	150	28	14
CAT28C65AP-20	8K x 8							x			†	200	28	14
CAT28C65AP-25	8K x 8							x			†	250	28	14
CAT28C65API-15	8K x 8							x			I	150	28	14
CAT28C65API-20	8K x 8							x			I	200	28	14
CAT28C65API-25	8K x 8							x			I	250	28	14
CAT28C65AN-15	8K x 8						x				†	150	32	32
CAT28C65AN-20	8K x 8						x				†	200	32	32
CAT28C65AN-25	8K x 8						x				†	250	32	32
CAT28C65ANI-15	8K x 8						x				I	150	32	32
CAT28C65ANI-20	8K x 8						x				I	200	32	32
CAT28C65ANI-25	8K x 8						x				I	250	32	32
CAT28C65AJ-15	8K x 8				x						†	150	28	27
CAT28C65AJ-20	8K x 8				x						†	200	28	27
CAT28C65AJ-25	8K x 8				x						†	250	28	27
CAT28C65AJI-15	8K x 8				x						I	150	28	27
CAT28C65AJI-20	8K x 8				x						I	200	28	27
CAT28C65AJI-25	8K x 8				x						I	250	28	27
CAT28C65AK-15	8K x 8					x					†	150	28	27
CAT28C65AK-20	8K x 8					x					†	200	28	27
CAT28C65AK-25	8K x 8					x					†	250	28	27
CAT28C65AKI-15	8K x 8					x					I	150	28	27
CAT28C65AKI-20	8K x 8					x					I	200	28	27
CAT28C65AKI-25	8K x 8					x					I	250	28	27

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D	= CERDIP
E	= LCC
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K	= S.O. (EIAJ)
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ARALLEL E²PROMs (Data Book Section 7)

Device Order Number	Organization	Package								Special Features	Temp Range	Access Time (ns)	# of Pins	Rail Qty
		C	D	E	J	K	N	P	T					
CAT28C64BP-12	8K x 8							x		B	†	120	28	14
CAT28C64BP-15	8K x 8							x		B	†	150	28	14
CAT28C64BP-20	8K x 8							x		B	†	200	28	14
CAT28C64BPI-15	8K x 8							x		B	I	150	28	14
CAT28C64BPI-20	8K x 8							x		B	I	200	28	14
CAT28C64BN-12	8K x 8						x			B	†	120	32	32
CAT28C64BN-15	8K x 8						x			B	†	150	32	32
CAT28C64BN-20	8K x 8						x			B	†	200	32	32
CAT28C64BNI-15	8K x 8						x			B	I	150	32	32
CAT28C64BNI-20	8K x 8						x			B	I	200	28	32
CAT28C64BJ-12	8K x 8				x					B	†	120	28	27
CAT28C64BJ-15	8K x 8				x					B	†	150	28	27
CAT28C64BJ-20	8K x 8				x					B	†	200	28	27
CAT28C64BJI-15	8K x 8				x					B	I	150	28	27
CAT28C64BJI-20	8K x 8				x					B	I	200	28	27
CAT28C64BT-12	8K x 8								x	B	†	120	32	15
CAT28C64BT-15	8K x 8								x	B	†	150	32	15
CAT28C64BT-20	8K x 8								x	B	†	200	32	15
CAT28C64BTI-15	8K x 8								x	B	I	150	32	15
CAT28C64BTI-20	8K x 8								x	B	I	200	32	15
CAT28C64BK-12	8K x 8					x				B	†	120	28	27
CAT28C64BK-15	8K x 8					x				B	†	150	28	27
CAT28C64BK-20	8K x 8					x				B	†	200	28	27
CAT28C64BKI-15	8K x 8					x				B	I	150	28	27
CAT28C64BKI-20	8K x 8					x				B	I	200	28	27

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C	=	Sidebraze
D	=	CERDIP
E	=	LCC
J	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
N	=	PLCC
P	=	Plastic DIP
T	=	TSOP

PARALLEL E²PROMs (Data Book Section 7)

Device Order Number	Organization	Package								Special Features	Temp Range	Access Time (ns)	# of Pins	Rail Qty
		C	D	E	J	K	N	P	T					
CAT28C65BP-12	8K x 8							x		B	†	120	28	14
CAT28C65BP-15	8K x 8							x		B	†	150	28	14
CAT28C65BP-20	8K x 8							x		B	†	200	28	14
CAT28C65BPI-15	8K x 8							x		B	I	150	28	14
CAT28C65BPI-20	8K x 8							x		B	I	200	28	14
CAT28C65BN-12	8K x 8						x			B	†	120	32	32
CAT28C65BN-15	8K x 8						x			B	†	150	32	32
CAT28C65BN-20	8K x 8						x			B	†	200	32	32
CAT28C65BNI-15	8K x 8						x			B	I	150	32	32
CAT28C65BNI-20	8K x 8						x			B	I	200	28	32
CAT28C65BJ-12	8K x 8				x					B	†	120	28	27
CAT28C65BJ-15	8K x 8				x					B	†	150	28	27
CAT28C65BJ-20	8K x 8				x					B	†	200	28	27
CAT28C65BJI-15	8K x 8				x					B	I	150	28	27
CAT28C65BJI-20	8K x 8				x					B	I	200	28	27
CAT28C65BT-12	8K x 8								x	B	†	120	32	15
CAT28C65BT-15	8K x 8								x	B	†	150	32	15
CAT28C65BT-20	8K x 8								x	B	†	200	32	15
CAT28C65BTI-15	8K x 8								x	B	I	150	32	15
CAT28C65BTI-20	8K x 8								x	B	I	200	32	15
CAT28C65BK-12	8K x 8					x				B	†	120	28	27
CAT28C65BK-15	8K x 8					x				B	†	150	28	27
CAT28C65BK-20	8K x 8					x				B	†	200	28	27
CAT28C65BKI-15	8K x 8					x				B	I	150	28	27
CAT28C65BKI-20	8K x 8					x				B	I	200	28	27
CAT28C256P-20	32K x 8							x			†	200	28	14
CAT28C256P-25	32K x 8							x			†	250	28	14
CAT28C256P-30	32K x 8							x			†	300	28	14
CAT28C256PI-20	32K x 8							x			I	200	28	14
CAT28C256PI-25	32K x 8							x			I	250	28	14
CAT28C256PI-30	32K x 8							x			I	300	28	14
CAT28C256N-20	32K x 8						x				†	200	32	32
CAT28C256N-25	32K x 8						x				†	250	32	32
CAT28C256N-30	32K x 8						x				†	300	32	32
CAT28C256NI-20	32K x 8						x				I	200	32	32
CAT28C256NI-25	32K x 8						x				I	250	32	32
CAT28C256NI-30	32K x 8						x				I	300	32	32

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C	=	Sidebraze
D	=	CERDIP
E	=	LCC
J	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
N	=	PLCC
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_ASH MEMORIES (Data Book Section 8)

Device Order Number	Organization	Package								Special Features	Temp Range	Access Time (ns)	# of Pins	Rail Qty
		C	D	E	J	K	N	P	T					
:AT28F512P-12	64K x 8							x			†	120	32	12
:AT28F512P-15	64K x 8							x			†	150	32	12
:AT28F512P-20	64K x 8							x			†	200	32	12
:AT28F512PI-12	64K x 8							x			I	120	32	12
:AT28F512PI-15	64K x 8							x			I	150	32	12
:AT28F512PI-20	64K x 8							x			I	200	32	12
:AT28F512N-12	64K x 8						x				†	120	32	32
:AT28F512N-15	64K x 8						x				†	150	32	32
:AT28F512N-20	64K x 8						x				†	200	32	32
:AT28F512NI-12	64K x 8						x				I	120	32	32
:AT28F512NI-15	64K x 8						x				I	150	32	32
:AT28F512NI-20	64K x 8						x				I	200	32	32
:AT28F512T-12	64K x 8								x		†	120	32	15
:AT28F512T-15	64K x 8								x		†	150	32	15
:AT28F512T-20	64K x 8								x		†	200	32	15
:AT28F512TI-12	64K x 8								x		I	120	32	15
:AT28F512TI-15	64K x 8								x		I	150	32	15
:AT28F512TI-20	64K x 8								x		I	200	32	15
:AT28F512V5P-12	64K x 8							x		V	†	120	32	12
:AT28F512V5P-15	64K x 8							x		V	†	150	32	12
:AT28F512V5P-20	64K x 8							x		V	†	200	32	12
:AT28F512V5PI-12	64K x 8							x		V	I	120	32	12
:AT28F512V5PI-15	64K x 8							x		V	I	150	32	12
:AT28F512V5PI-20	64K x 8							x		V	I	200	32	12
:AT28F512V5N-12	64K x 8						x			V	†	120	32	32
:AT28F512V5N-15	64K x 8						x			V	†	150	32	32
:AT28F512V5N-20	64K x 8						x			V	†	200	32	32
:AT28F512V5NI-12	64K x 8						x			V	I	120	32	32
:AT28F512V5NI-15	64K x 8						x			V	I	150	32	32
:AT28F512V5NI-20	64K x 8						x			V	I	200	32	32
:AT28F512V5T-12	64K x 8								x	V	†	120	32	15
:AT28F512V5T-15	64K x 8								x	V	†	150	32	15
:AT28F512V5T-20	64K x 8								x	V	†	200	32	15
:AT28F512V5TI-12	64K x 8								x	V	I	120	32	15
:AT28F512V5TI-15	64K x 8								x	V	I	150	32	15
:AT28F512V5TI-20	64K x 8								x	V	I	200	32	15

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B	=	Advanced Device
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V	=	Special Voltage
C	=	Sidebraze
D	=	CERDIP
E	=	LCC
J	=	S.O. (JEDEC)
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N	=	PLCC
P	=	Plastic DIP
T	=	TSOP

FLASH MEMORIES (Data Book Section 8)

Device Order Number	Organization	Package								Special Features	Temp Range	Access Time (ns)	# of Pins	Rail Qty
		C	D	E	J	K	N	P	T					
CAT28F010P-12	128K x 8							x			†	120	32	12
CAT28F010P-15	128K x 8							x			†	150	32	12
CAT28F010P-20	128K x 8							x			†	200	32	12
CAT28F010PI-12	128K x 8							x			I	120	32	12
CAT28F010PI-15	128K x 8							x			I	150	32	12
CAT28F010PI-20	128K x 8							x			I	200	32	12
CAT28F010N-12	128K x 8						x				†	120	32	32
CAT28F010N-15	128K x 8						x				†	150	32	32
CAT28F010N-20	128K x 8						x				†	200	32	32
CAT28F010NI-12	128K x 8						x				I	120	32	32
CAT28F010NI-15	128K x 8						x				I	150	32	32
CAT28F010NI-20	128K x 8						x				I	200	32	32
CAT28F010T-12	128K x 8								x		†	120	32	15
CAT28F010T-15	128K x 8								x		†	150	32	15
CAT28F010T-20	128K x 8								x		†	200	32	15
CAT28F010TI-12	128K x 8								x		I	120	32	15
CAT28F010TI-15	128K x 8								x		I	150	32	15
CAT28F010TI-20	128K x 8								x		I	200	32	15
CAT28F010V5P-12	128K x 8							x		V	†	120	32	12
CAT28F010V5P-15	128K x 8							x		V	†	150	32	12
CAT28F010V5P-20	128K x 8							x		V	†	200	32	12
CAT28F010V5PI-12	128K x 8							x		V	I	120	32	12
CAT28F010V5PI-15	128K x 8							x		V	I	150	32	12
CAT28F010V5PI-20	128K x 8							x		V	I	200	32	12
CAT28F010V5N-12	128K x 8						x			V	†	120	32	32
CAT28F010V5N-15	128K x 8						x			V	†	150	32	32
CAT28F010V5N-20	128K x 8						x			V	†	200	32	32
CAT28F010V5NI-12	128K x 8						x			V	I	120	32	32
CAT28F010V5NI-15	128K x 8						x			V	I	150	32	32
CAT28F010V5NI-20	128K x 8						x			V	I	200	32	32
CAT28F010V5T-12	128K x 8								x	V	†	120	32	15
CAT28F010V5T-15	128K x 8								x	V	†	150	32	15
CAT28F010V5T-20	128K x 8								x	V	†	200	32	15
CAT28F010V5TI-12	128K x 8								x	V	I	120	32	15
CAT28F010V5TI-15	128K x 8								x	V	I	150	32	15
CAT28F010V5TI-20	128K x 8								x	V	I	200	32	15

Note:
(1) Contact factory for High Endurance device availability.

Key:

†	=	Blank = Commercial = 0°C to +70°C
I	=	Industrial = –40°C to +85°C
A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
V	=	Special Voltage
C	=	Sidebraze
D	=	CERDIP
E	=	LCC
J	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
N	=	PLCC
P	=	Plastic DIP
T	=	TSOP

FLASH MEMORIES (Data Book Section 8)

Device Order Number	Organization	Package								Special Features	Temp Range	Access Time (ns)	# of Pins	Rail Qty
		C	D	E	J	K	N	P	T					
CAT28F020P-12	256K x 8							x			†	120	32	12
CAT28F020P-15	256K x 8							x			†	150	32	12
CAT28F020P-20	256K x 8							x			†	200	32	12
CAT28F020PI-12	256K x 8							x			I	120	32	12
CAT28F020PI-15	256K x 8							x			I	150	32	12
CAT28F020PI-20	256K x 8							x			I	200	32	12
CAT28F020N-12	256K x 8						x				†	120	32	32
CAT28F020N-15	256K x 8						x				†	150	32	32
CAT28F020N-20	256K x 8						x				†	200	32	32
CAT28F020NI-12	256K x 8						x				I	120	32	32
CAT28F020NI-15	256K x 8						x				I	150	32	32
CAT28F020NI-20	256K x 8						x				I	200	32	32
CAT28F020T-12	256K x 8								x		†	120	32	15
CAT28F020T-15	256K x 8								x		†	150	32	15
CAT28F020T-20	256K x 8								x		†	200	32	15
CAT28F020TI-12	256K x 8								x		I	120	32	15
CAT28F020TI-15	256K x 8								x		I	150	32	15
CAT28F020TI-20	256K x 8								x		I	200	32	15

Note:
1) Contact factory for High Endurance device availability.

Key:

†	=	Blank = Commercial = 0°C to +70°C
I	=	Industrial = –40°C to +85°C
A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
V	=	Special Voltage
C	=	Sidebraze
D	=	CERDIP
E	=	LCC
J	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
N	=	PLCC
P	=	Plastic DIP
T	=	TSOP

EPROMs (Data Book Section 9)

Device Order Number	Organization	Package							Special Features	Temp Range	Access Time (ns)	# of Pins	Rail Qty
		C	D	E	J	K	N	P	T					
CAT27HC256LP-55/5	32K x 8							x			†	55	28	14
CAT27HC256LP-70	32K x 8							x			†	70	28	14
CAT27HC256LP-90	32K x 8							x			†	90	28	14
CAT27HC256LP-12	32K x 8							x			†	120	28	14
CAT27HC256LPI-70	32K x 8							x			I	70	28	14
CAT27HC256LPI-90	32K x 8							x			I	90	28	14
CAT27HC256LPI-12	32K x 8							x			I	120	28	14
CAT27HC256LD-55/5	32K x 8		x								†	55	28	14
CAT27HC256LD-70	32K x 8		x								†	70	28	14
CAT27HC256LD-90	32K x 8		x								†	90	28	14
CAT27HC256LD-12	32K x 8		x								†	120	28	14
CAT27HC256LDI-70	32K x 8		x								I	70	28	14
CAT27HC256LDI-90	32K x 8		x								I	90	28	14
CAT27HC256LDI-12	32K x 8		x								I	120	28	14
CAT27HC256LN-55/5	32K x 8						x				†	55	32	32
CAT27HC256LN-70	32K x 8						x				†	70	32	32
CAT27HC256LN-90	32K x 8						x				†	90	32	32
CAT27HC256LN-12	32K x 8						x				†	120	32	32
CAT27HC256LNI-70	32K x 8						x				I	70	32	32
CAT27HC256LNI-90	32K x 8						x				I	90	32	32
CAT27HC256LNI-12	32K x 8						x				I	120	32	32
CAT27HC256LE-55/5	32K x 8			x							†	55	32	34
CAT27HC256LE-70	32K x 8			x							†	70	32	34
CAT27HC256LE-90	32K x 8			x							†	90	32	34
CAT27HC256LE-12	32K x 8			x							†	120	32	34
CAT27HC256LEI-70	32K x 8			x							I	70	32	34
CAT27HC256LEI-90	32K x 8			x							I	90	32	34
CAT27HC256LEI-12	32K x 8			x							I	120	32	34

Note:
(1) Contact factory for High Endurance device availability.
(2) V_{CC} = 5V±5% for CAT27HC256L-55.

Key:

†	=	Blank = Commercial = 0°C to +70°C
I	=	Industrial = –40°C to +85°C
A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
V	=	Special Voltage
C	=	Sidebraze
D	=	CERDIP
E	=	LCC
J	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
N	=	PLCC
P	=	Plastic DIP
T	=	TSOP

PROMs (Data Book Section 9)

Device Order Number	Organization	Package								Special Features	Temp Range	Access Time (ns)	# of Pins	Rail Qty
		C	D	E	J	K	N	P	T					
CAT27C210P-15	64K x 16							x			†	150	40	9
CAT27C210P-17	64K x 16							x			†	170	40	9
CAT27C210P-20	64K x 16							x			†	200	40	9
CAT27C210P-25	64K x 16							x			†	250	40	9
CAT27C210PI-17	64K x 16							x			I	170	40	9
CAT27C210PI-20	64K x 16							x			I	200	40	9
CAT27C210PI-25	64K x 16							x			I	250	40	9
CAT27C210D-15	64K x 16		x								†	150	40	9
CAT27C210D-17	64K x 16		x								†	170	40	9
CAT27C210D-20	64K x 16		x								†	200	40	9
CAT27C210D-25	64K x 16		x								†	250	40	9
CAT27C210DI-17	64K x 16		x								I	170	40	9
CAT27C210DI-20	64K x 16		x								I	200	40	9
CAT27C210DI-25	64K x 16		x								I	250	40	9
CAT27C210N-15	64K x 16						x				†	150	44	28
CAT27C210N-17	64K x 16						x				†	170	44	28
CAT27C210N-20	64K x 16						x				†	200	44	28
CAT27C210N-25	64K x 16						x				†	250	44	28
CAT27C210NI-17	64K x 16						x				I	170	44	28
CAT27C210NI-20	64K x 16						x				I	200	44	28
CAT27C210NI-25	64K x 16						x				I	250	44	28

ote:
) Contact factory for High Endurance device availability.

Key:

†	=	Blank = Commercial = 0°C to +70°C
I	=	Industrial = –40°C to +85°C
A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
V	=	Special Voltage
C	=	Sidebraze
D	=	CERDIP
E	=	LCC
J	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
N	=	PLCC
P	=	Plastic DIP
T	=	TSOP

NVRAMs (Data Book Section 10)

Device Order Number	Organization	Package C	D	E	J	K	N	P	T	Special Features	Temp Range	Access Time (ns)	# of Pins	Rail Qty
CAT22C10P-20	64 x 4							x			†	200	18	22
CAT22C10P-30	64 x 4							x			†	300	18	22
CAT22C10PI-20	64 x 4							x			I	200	18	22
CAT22C10PI-30	64 x 4							x			I	300	18	22
CAT22C10J-20	64 x 4				x						†	200	20	47
CAT22C10J-30	64 x 4				x						†	300	20	47
CAT22C10JI-20	64 x 4				x						I	200	20	47
CAT22C10JI-30	64 x 4				x						I	300	20	47
CAT22C12P-20	256 x 4							x			†	200	18	22
CAT22C12P-30	256 x 4							x			†	300	18	22
CAT22C12PI-20	256 x 4							x			I	200	18	22
CAT22C12PI-30	256 x 4							x			I	300	18	22
CAT22C44P	16 x 16							x			†		8	50
CAT22C44PI	16 x 16							x			I		8	50
CAT22C44J	16 x 16				x						†		8	100
CAT22C44JI	16 x 16				x						I		8	100

Note:
(1) Contact factory for High Endurance device availability.

Key:

†	=	Blank = Commercial = 0°C to +70°C
I	=	Industrial = –40°C to +85°C
A	=	Advanced Device or Special Assembly
B	=	Advanced Device
L	=	Low Voltage
V	=	Special Voltage
C	=	Sidebraze
D	=	CERDIP
E	=	LCC
J	=	S.O. (JEDEC)
K	=	S.O. (EIAJ)
N	=	PLCC
P	=	Plastic DIP
T	=	TSOP

ACs—High Speed

Device Order Number	Resolution (bits)	Accuracy (LSB)	Settling Time (ns)	Special Feature	Package C	Package D	Package J	Package P	Temp Range	# of Pins	DACs/ Pkg	Rail Qty
CAT104AC	12	1/2	40	A	x				†	24	1	16
CAT104BC	12	1	40	B	x				†	24	1	16
CAT104BCI	12	1	40	B	x				I	24	1	16
CAT105AC	12	1/2	40	A	x				†	24	1	16
CAT105BC	12	1	40	B	x				†	24	1	16
CAT105BCI	12	1	40	B	x				I	24	1	16
CAT506AC	12	1/2	25	A	x				†	24	1	16
CAT506BC	12	1	25	B	x				†	24	1	16
CAT506BCI	12	1	25	B	x				I	24	1	16

Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C
A = 1/2 LSB
B = 1 LSB
C = Sidebraze
D = CERDIP
J = S.O. (JEDEC)
P = Plastic DIP

ACs—Low Speed DACpot

Device Order Number	Resolution (bits)	Accuracy (LSB)	Settling Time (µs)	V_{PP}	Package C	Package D	Package J	Package P	Temp Range	# of Pins	DACs/ Pkg	Tape & Reel	Rail Qty
CAT504P	8	1	10	Ext.				x	†	14	4		25
CAT504PI	8	1	10	Ext.				x	I	14	4		25
CAT504J	8	1	10	Ext.			x		†	14	4	TE7	94
CAT504JI	8	1	10	Ext.			x		I	14	4	TE13	94
CAT505P	8	1	10	Int.				x	†	20	4		18
CAT505PI	8	1	10	Int.				x	I	20	4		18
CAT505J	8	1	10	Int.			x		†	20	4	TE7	47
CAT505JI	8	1	10	Int.			x		I	20	4	TE13	47

Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C
C = Sidebraze
D = CERDIP
J = S.O. (JEDEC)
P = Plastic DIP

VOLTAGE REFERENCES

Device Order Number	Output Voltage	Accuracy (%)	Drift (ppm)	Output Adj. (%)	Special Feature	Package C	Package D	Package J	Package P	Temp Range	# of Pins	Rail Qty
CAT507AP	5.000	0.300	3	3.0	A				x	†	8	50
CAT507API	5.000	0.300	3	3.0	A				x	I	8	50
CAT507ADI	5.000	0.300	3	3.0	A		x			I	8	50
CAT507BP	5.000	0.500	10	3.0	B				x	†	8	50
CAT507BPI	5.000	0.500	10	3.0	B				x	I	8	50
CAT507BDI	5.000	0.500	10	3.0	B		x			I	8	50
CAT508AP	–5.000	0.300	3	3.0	A				x	†	8	50
CAT508API	–5.000	0.300	3	3.0	A				x	I	8	50
CAT508ADI	–5.000	0.300	3	3.0	A		x			I	8	50
CAT508BP	–5.000	0.500	10	3.0	B				x	†	8	50
CAT508BPI	–5.000	0.500	10	3.0	B				x	I	8	50
CAT508BDI	–5.000	0.500	10	3.0	B		x			I	8	50

Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C
A = 0.300% Accuracy
B = 0.500% Accuracy
C = Sidebraze
D = CERDIP
J = S.O. (JEDEC)
P = Plastic DIP

VOLTAGE REFERENCES

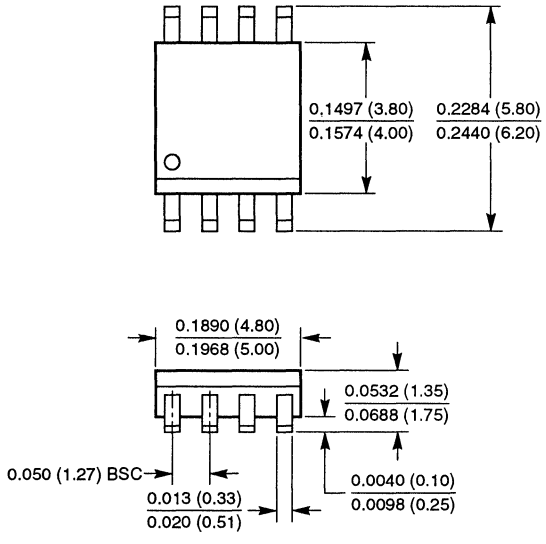
Device Order Number	Output Voltage	Accuracy (%)	Drift (ppm)	Output Adj. (%)	Special Feature	Package C	Package D	Package J	Package P	Temp Range	# of Pins	Rail Qty
CAT2700AP	10.000	0.025	3	0.2	A				x	†	14	25
CAT2700API	10.000	0.025	3	0.2	A				x	I	14	25
CAT2700ADI	10.000	0.025	3	0.2	A		x			I	14	25
CAT2700BP	10.000	0.050	10	0.2	B				x	†	14	25
CAT2700BPI	10.000	0.050	10	0.2	B				x	I	14	25
CAT2700BDI	10.000	0.050	10	0.2	B		x			I	14	25
CAT2701AP	–10.000	0.025	3	0.2	A				x	†	14	25
CAT2701API	–10.000	0.025	3	0.2	A				x	I	14	25
CAT2701ADI	–10.000	0.025	3	0.2	A		x			I	14	25
CAT2701BP	–10.000	0.050	10	0.2	B				x	†	14	25
CAT2701BPI	–10.000	0.050	10	0.2	B				x	I	14	25
CAT2701BDI	–10.000	0.050	10	0.2	B		x			I	14	25

Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = –40°C to +85°C
A = 0.025% Accuracy
B = 0.050% Accuracy
C = Sidebraze
D = CERDIP
J = S.O. (JEDEC)
P = Plastic DIP

ackaging Information

.EAD 150 MIL WIDE SOIC (S)



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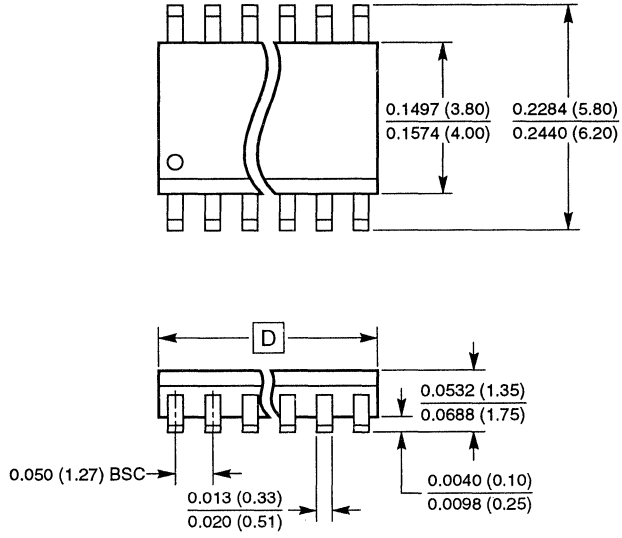
tes:
Complies with JEDEC publication 95 MS-012 dimensions; however, some dimensions may be more stringent.
All linear dimensions are in inches and parenthetically in millimeters.

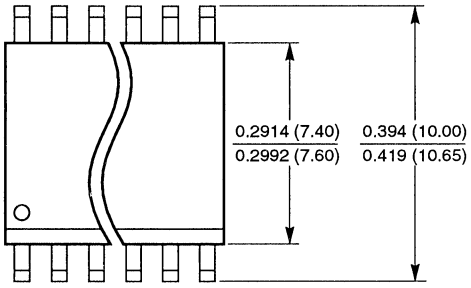
8, 14 AND16-LEAD 150 MIL WIDE SOIC (J)

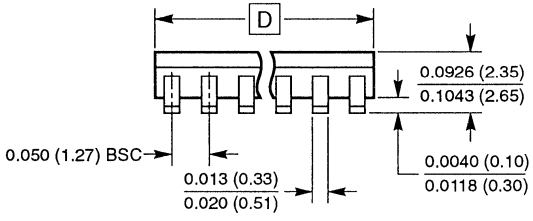


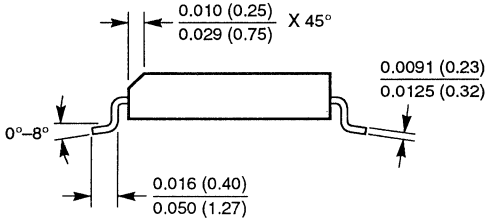
Dimension D		
Pkg	**Min**	**Max**
8L	0.1890(4.80)	0.1968(5.00)
14L	0.3367(8.55)	0.3444(8.75)
16L	0.3859(9.80)	0.3937(10.00)

Notes:
1. Complies with JEDEC publication 95 MS-012 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

–28-LEAD 300 MIL WIDE SOIC (J)







Dimension D		
Pkg	**Min**	**Max**
16L	0.3977 (10.10)	0.4133 (10.50)
18L	0.4469 (11.35)	0.4625 (11.75)
20L	0.4961 (12.60)	0.5118 (13.00)
24L	0.5985 (15.20)	0.6141 (15.60)
28L	0.6969 (17.70)	0.7125 (18.10)

ɔtes:
Complies with JEDEC publication 95 MS-013 dimensions; however, some dimensions may be more stringent.
All linear dimensions are in inches and parenthetically in millimeters.

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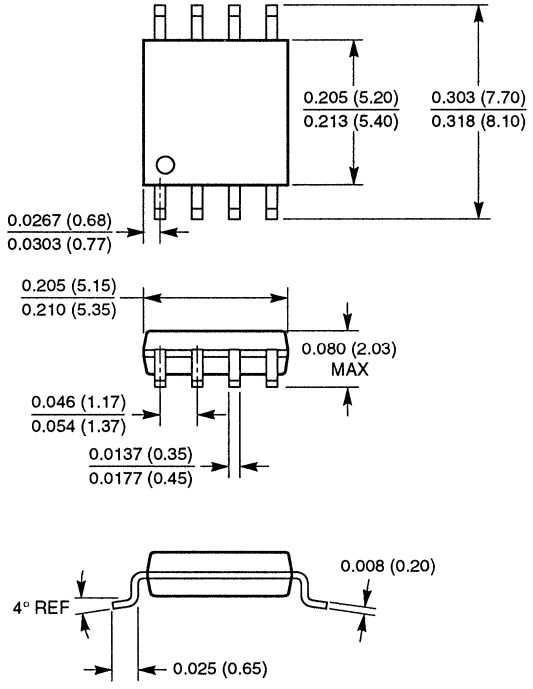
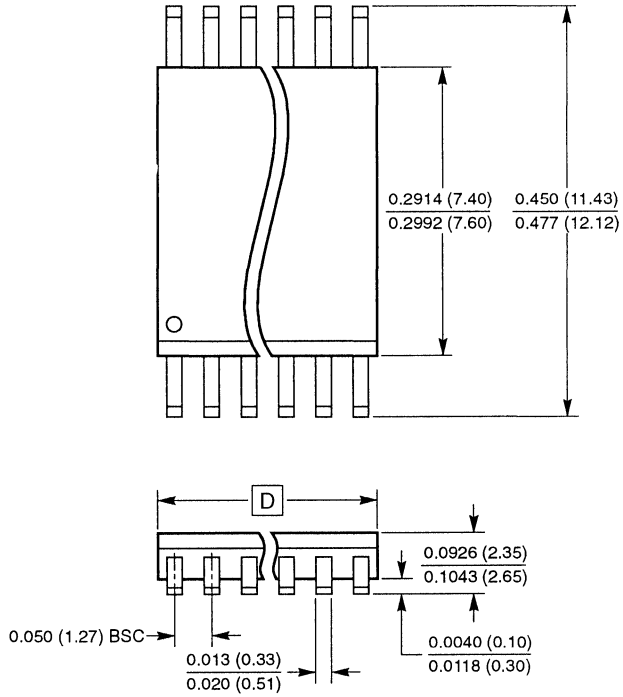
8-LEAD 210 MIL WIDE SOIC (K)



Note:
1. All linear dimensions are in inches and parenthetically in millimeters.

–28-LEAD 300 MIL WIDE EXTENDED FOOTPRINT SOIC (K)



Dimension D		
Pkg	**Min**	**Max**
24L	0.5985 (15.20)	0.6141 (15.60)
28L	0.6969 (17.70)	0.7125 (18.10)

ote:
All linear dimensions are in inches and parenthetically in millimeters.

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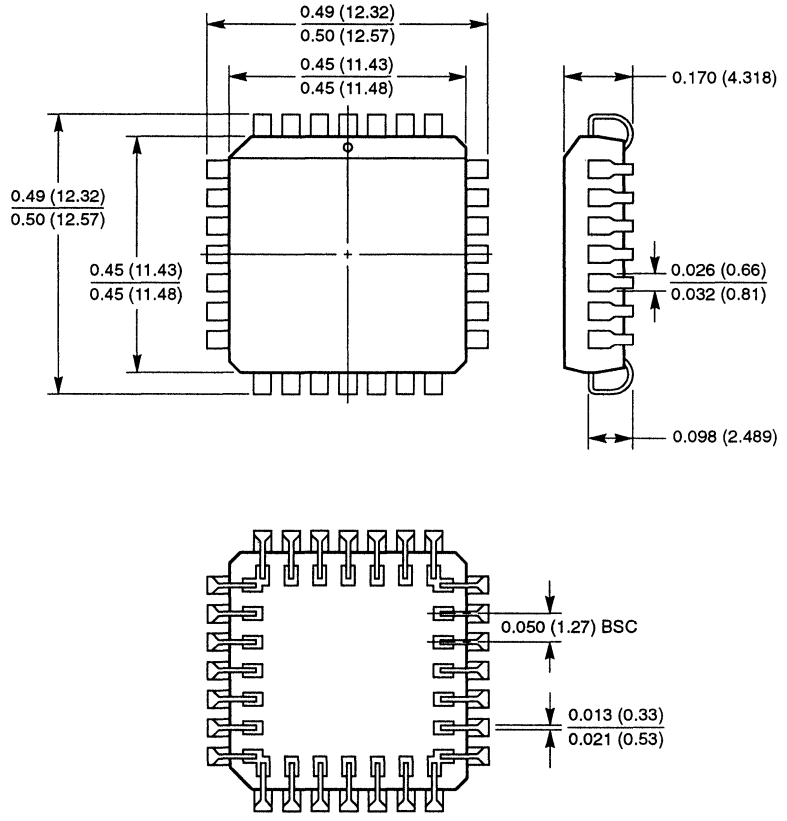
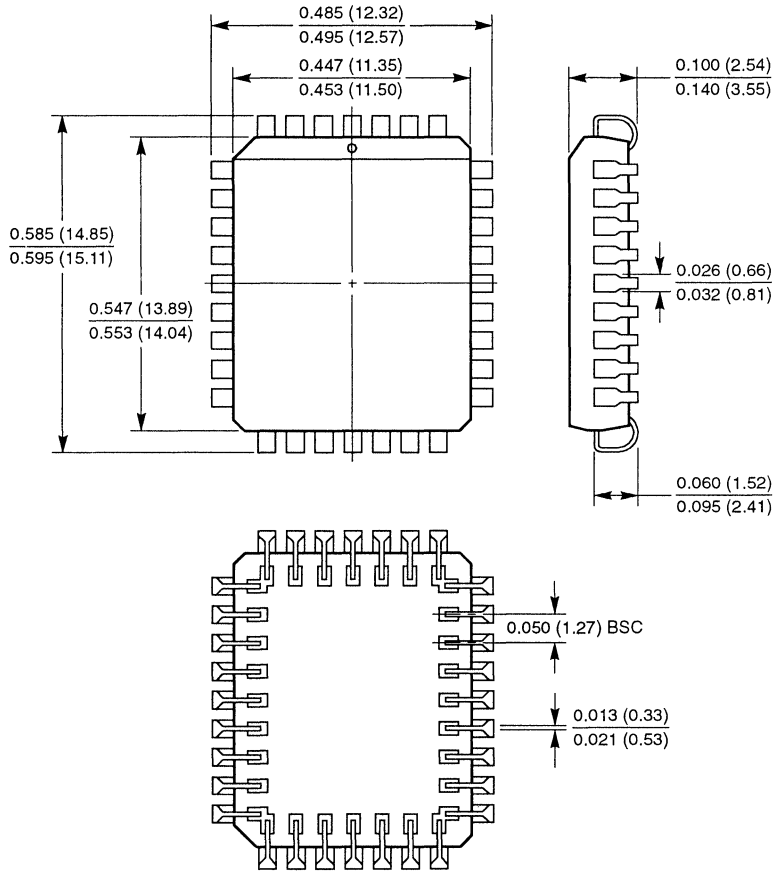
28-LEAD PLASTIC LEADED CHIP CARRIER (N)



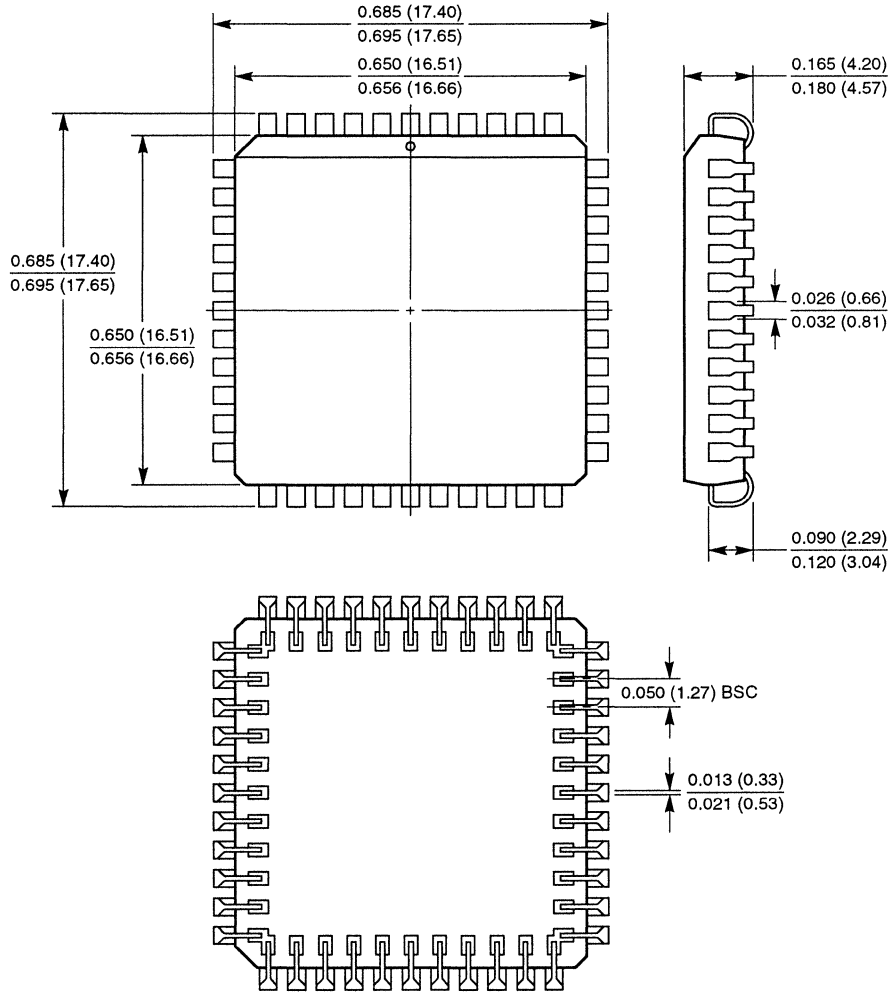
Notes:
1. Complies with JEDEC Publication 95 MO-052 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

-LEAD PLASTIC LEADED CHIP CARRIER (N)



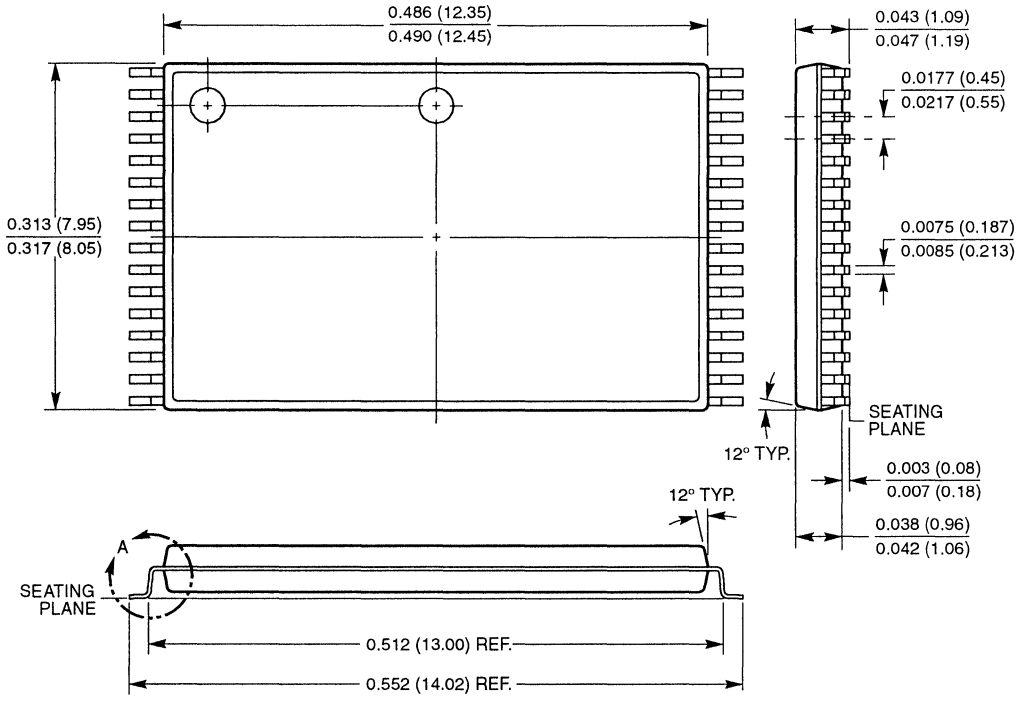
otes:
. Complies with JEDEC Publication 95 MO-052 dimensions; however, some dimensions may be more stringent.
. All linear dimensions are in inches and parenthetically in millimeters.

44-LEAD PLASTIC LEADED CHIP CARRIER (N)

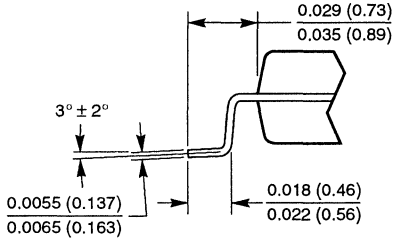


Notes:
1. Complies with JEDEC Publication 95 MO-047 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

-LEAD 8MM X 14MM TSOP (T)



DETAIL "A"



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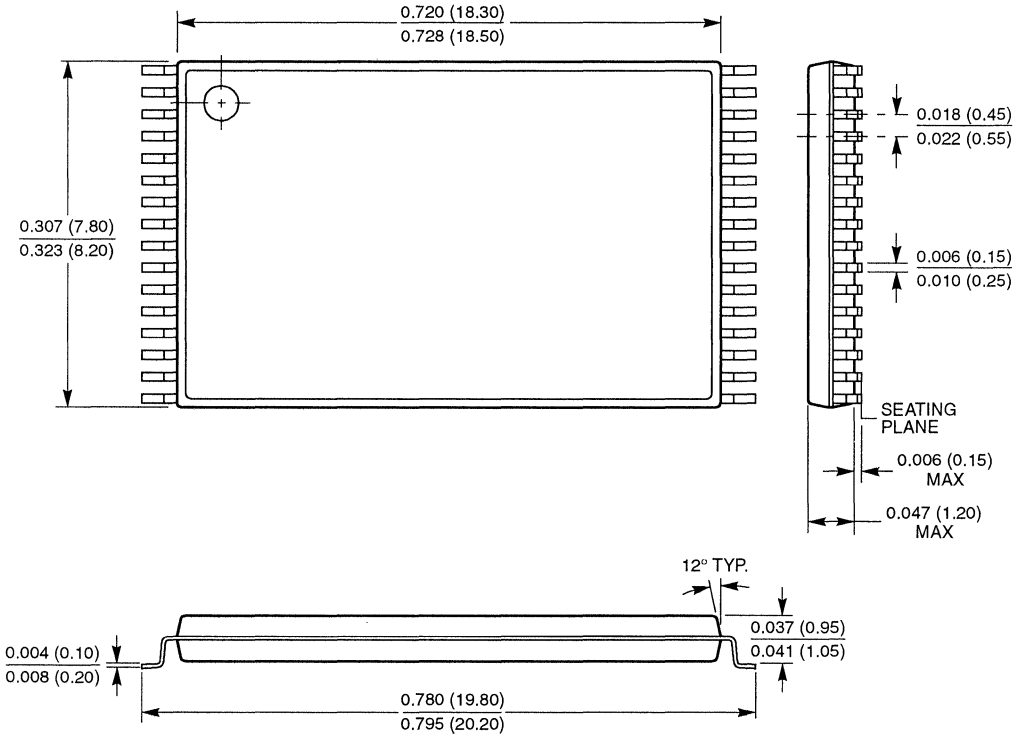
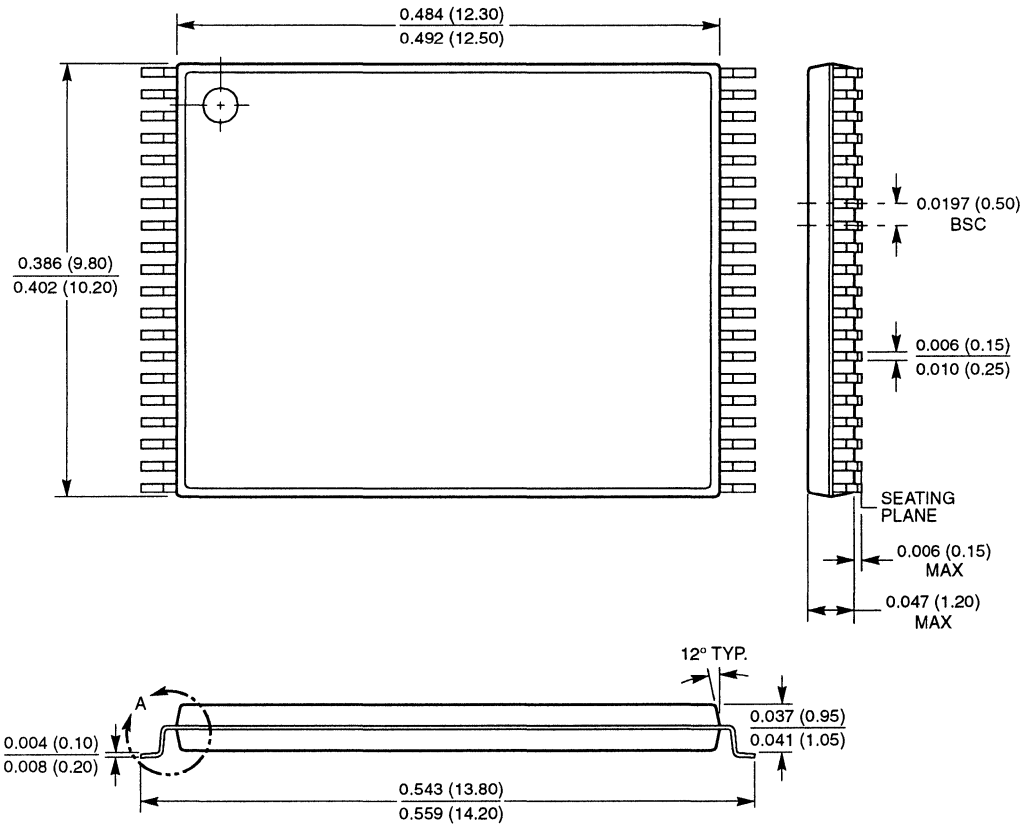
ote:
. All linear dimensions are in inches and parenthetically in millimeters.

32-LEAD 8MM X 20MM TSOP (T)

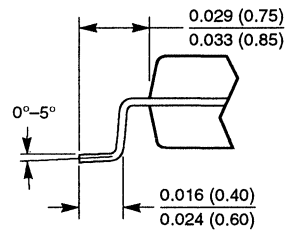


Note:
1. All linear dimensions are in inches and parenthetically in millimeters.

LEAD 10MM X 14MM TSOP (T)



DETAIL "A"



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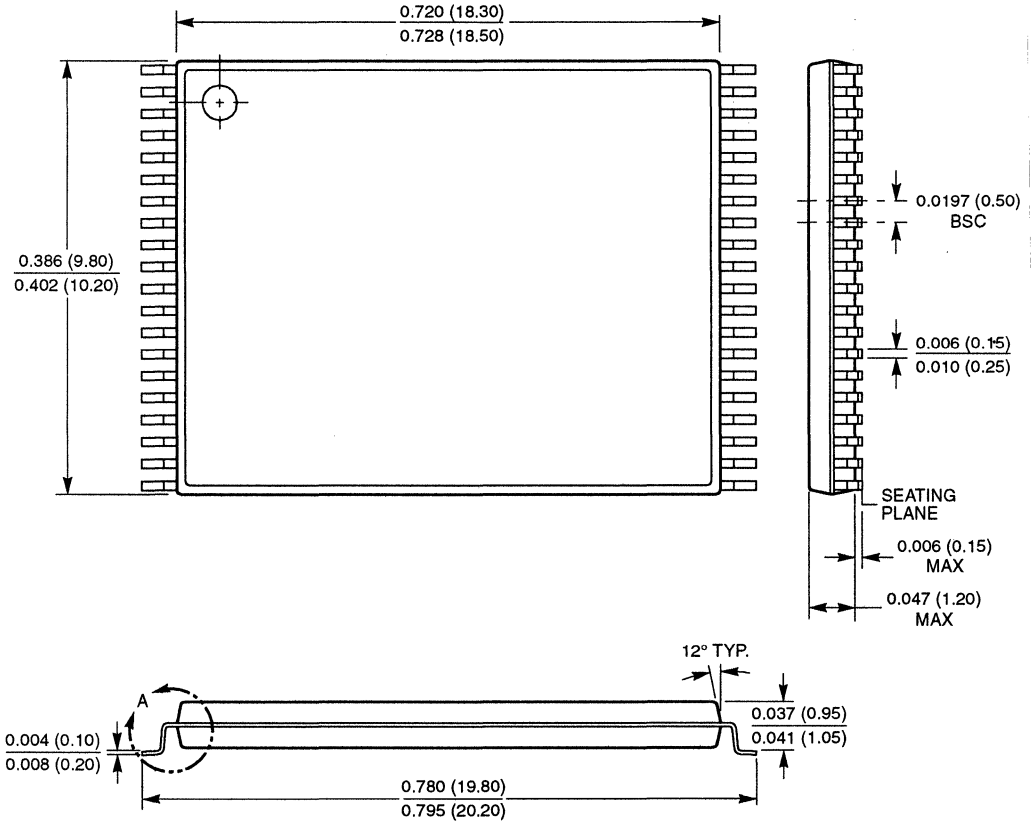
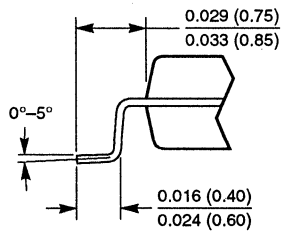
ote:
All linear dimensions are in inches and parenthetically in millimeters.

40-LEAD 10MM X 20MM TSOP (T)

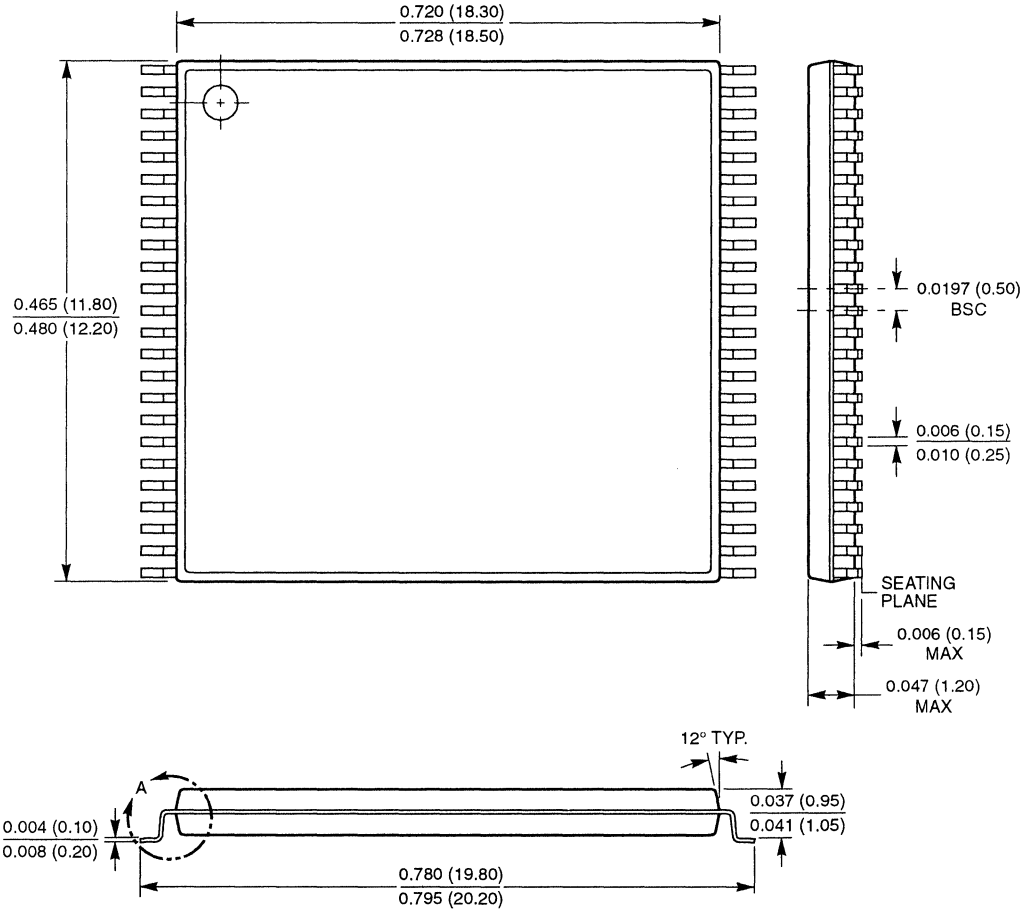


DETAIL "A"

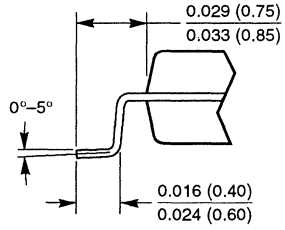


Note:
1. All linear dimensions are in inches and parenthetically in millimeters.

·LEAD 12MM X 20MM TSOP (T)



DETAIL "A"



ote:
All linear dimensions are in inches and parenthetically in millimeters.

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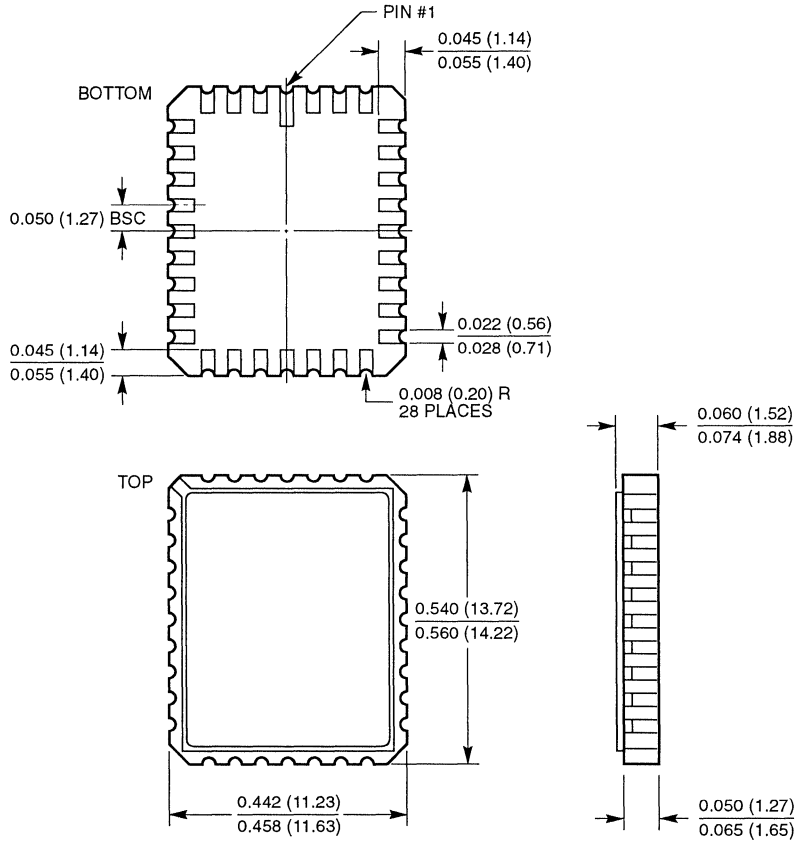
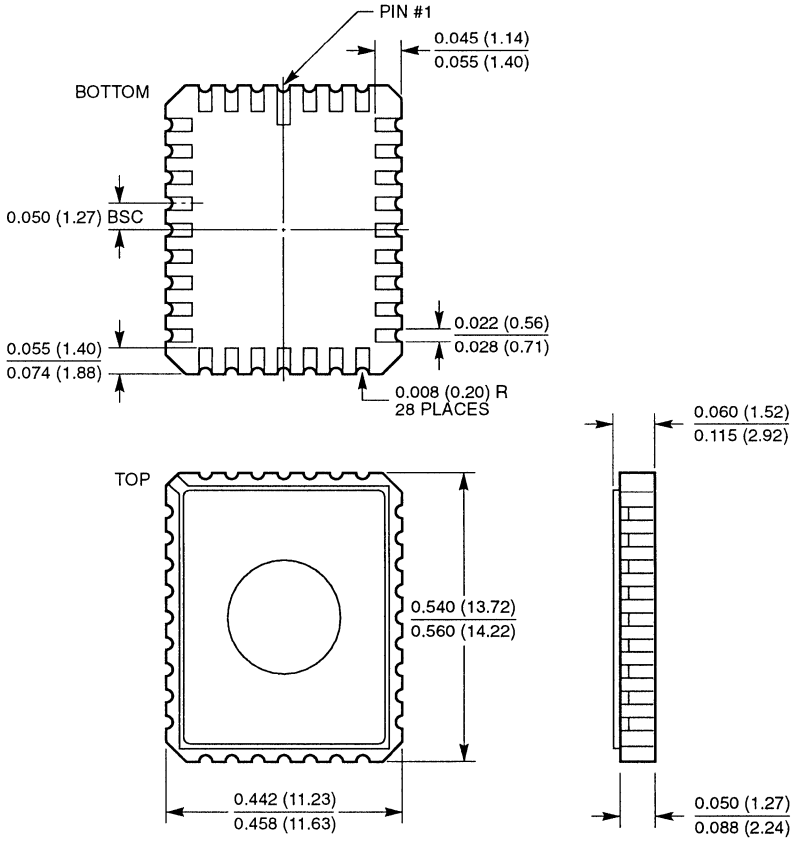
32-TERMINAL LEADLESS CHIP CARRIER - LCC (E)



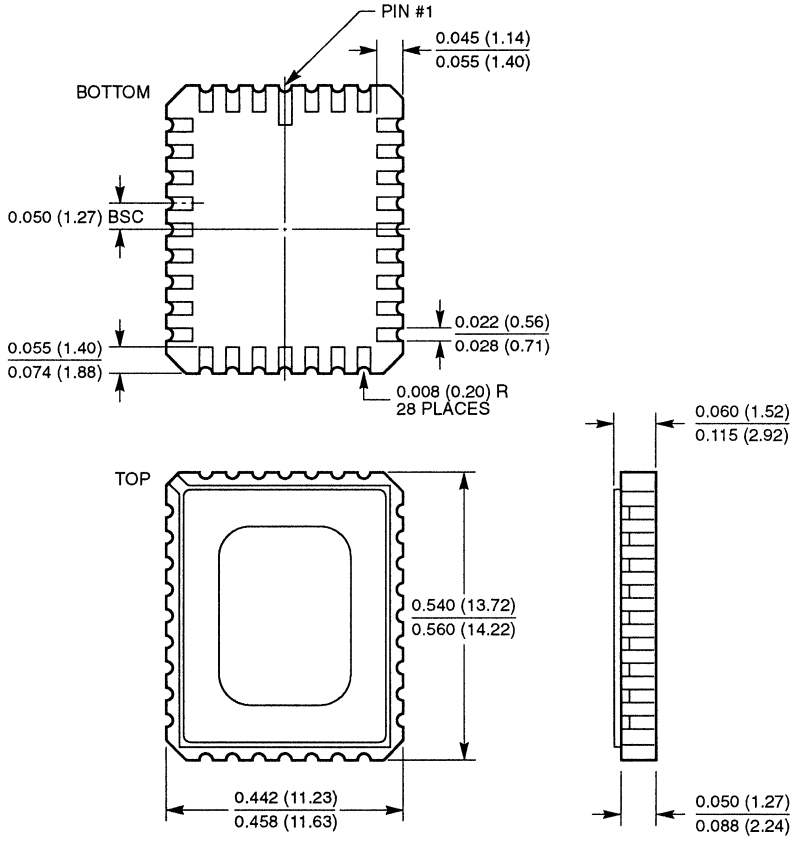
Notes:
1. Complies with MIL-STD-1835 C-12A dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

-TERMINAL LEADLESS WINDOWED CERAMIC LCC (E)



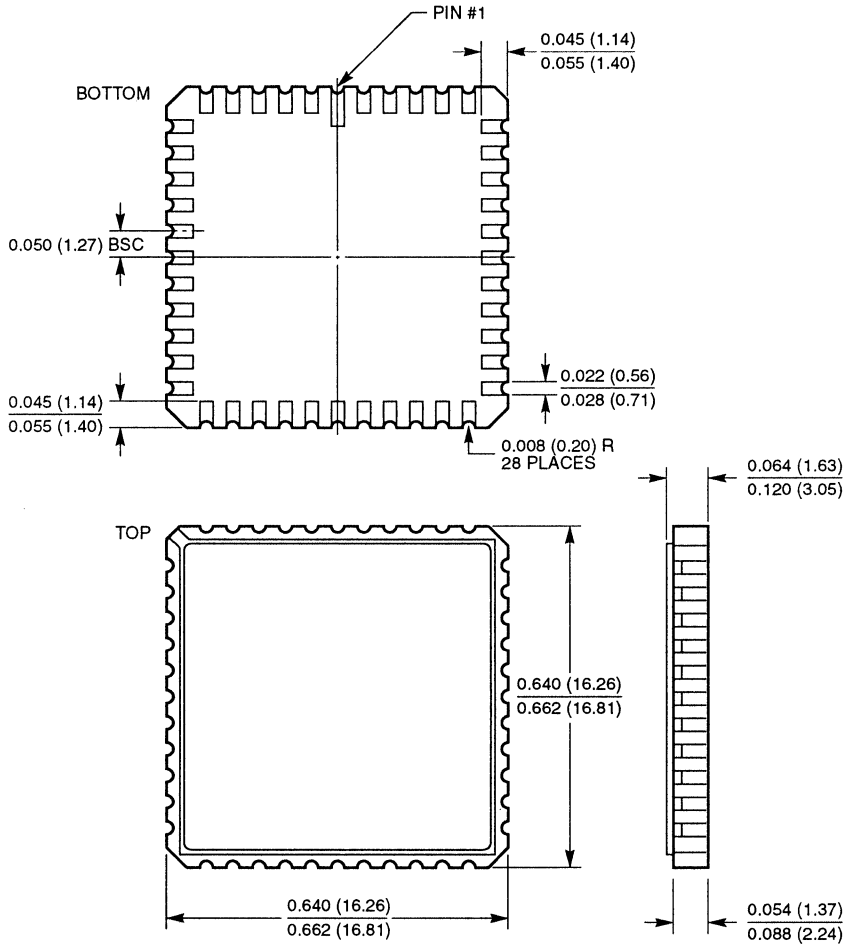
ote:
. All linear dimensions are in inches and parenthetically in millimeters.

32-TERMINAL LEADLESS LARGE WINDOWED CERAMIC LCC (E)



Note:
1. All linear dimensions are in inches and parenthetically in millimeters.

-TERMINAL LEADLESS CHIP CARRIER - LCC (E)



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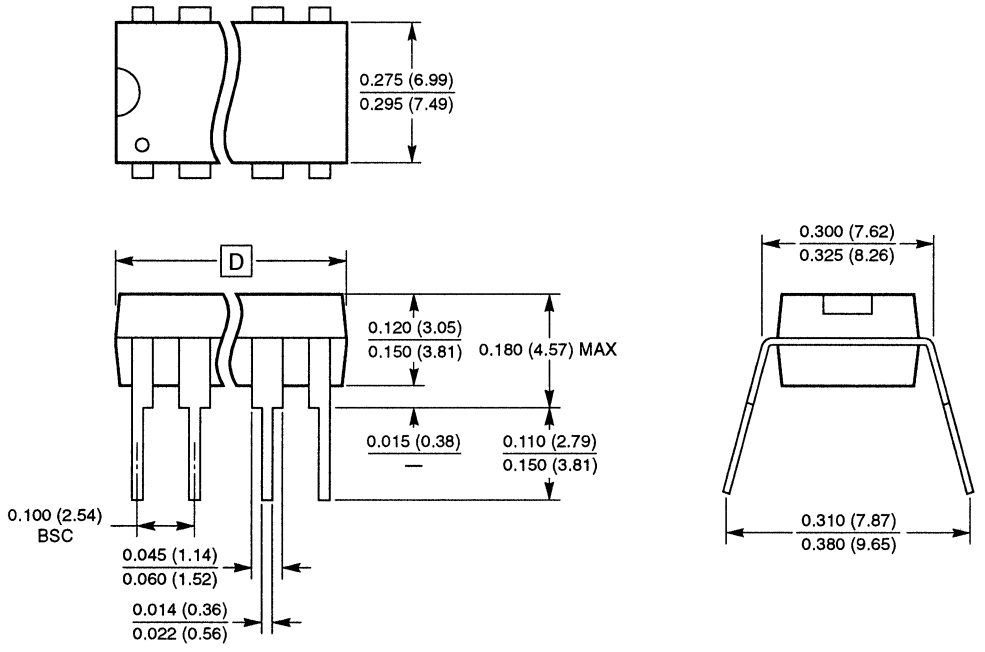
otes:
. Complies with MIL-STD-1835 C-5 dimensions; however, some dimensions may be more stringent.
. All linear dimensions are in inches and parenthetically in millimeters.

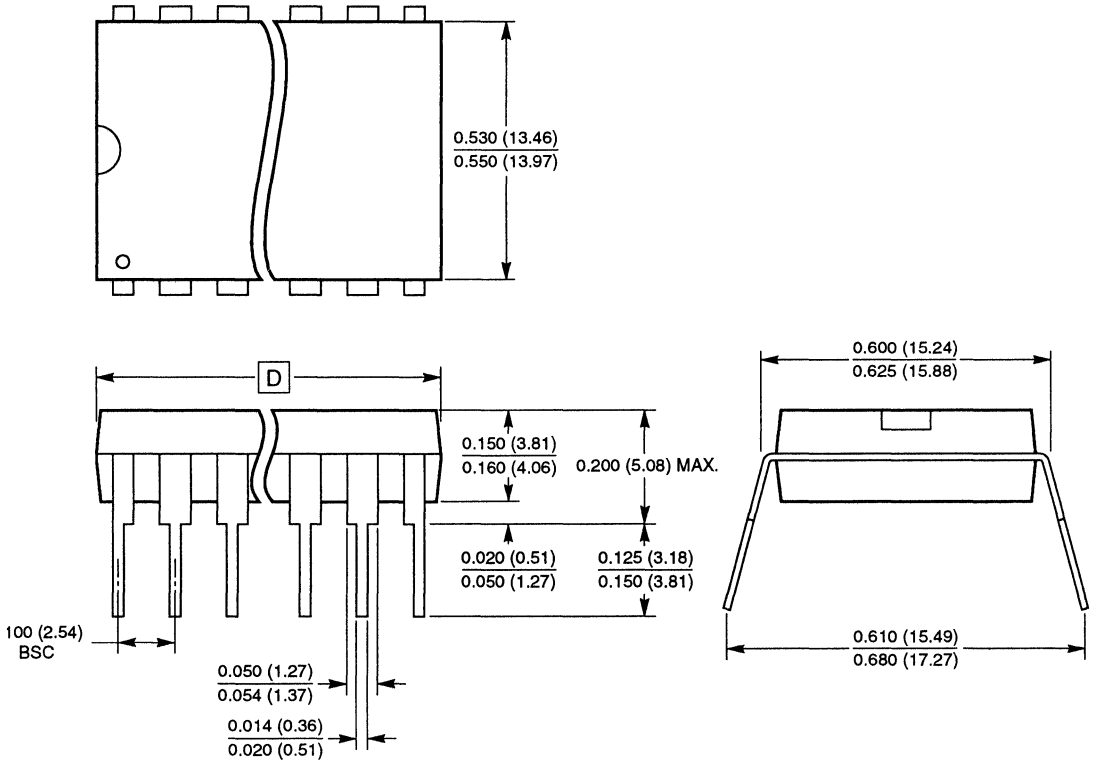
8–32-LEAD 300 MIL WIDE PLASTIC DIP (P)



Dimension D		
Pkg	**Min**	**Max**
8L	0.355 (9.02)	0.375 (9.53)
14L	0.645 (16.38)	0.685 (17.40)
16L	0.745 (21.45)	0.785 (19.94)
18L	0.845 (21.46)	0.885 (22.48)
20L	0.945 (24.00)	0.985 (25.02)
22L	1.045 (26.54)	1.085 (27.56)
24L	1.145 (29.08)	1.185 (30.01)
28L	1.345 (34.16)	1.385 (35.18)
32L	1.545 (39.75)	1.585 (40.26)

Notes:
1. Complies with JEDEC Publication 95 MO-95 dimensions; however, some of the dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

–40-LEAD 600 MIL WIDE PLASTIC DIP (P)



Dimension D		
Pkg	**Min**	**Max**
24L	1.240 (31.50)	1.270 (32.25)
28L	1.420 (36.06)	1.470 (37.33)
32L	1.640 (41.65)	1.670 (42.41)
40L	2.040 (51.81)	2.070 (52.57)

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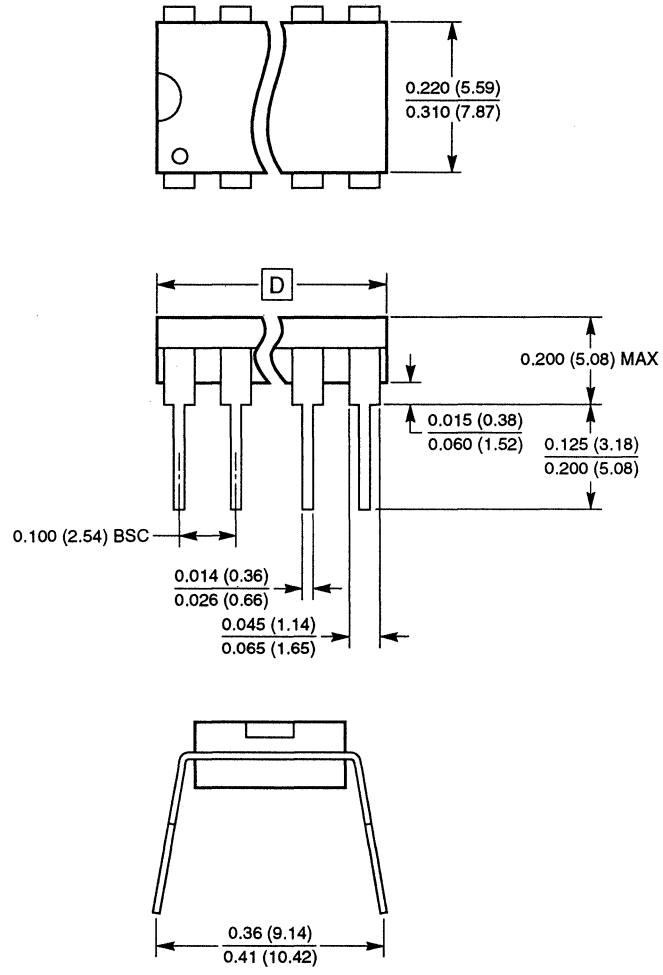
otes:
Complies with JEDEC Publication 95 MO-015 dimensions; however, some dimensions may be more stringent.
All linear dimensions are in inches and parenthetically in millimeters.

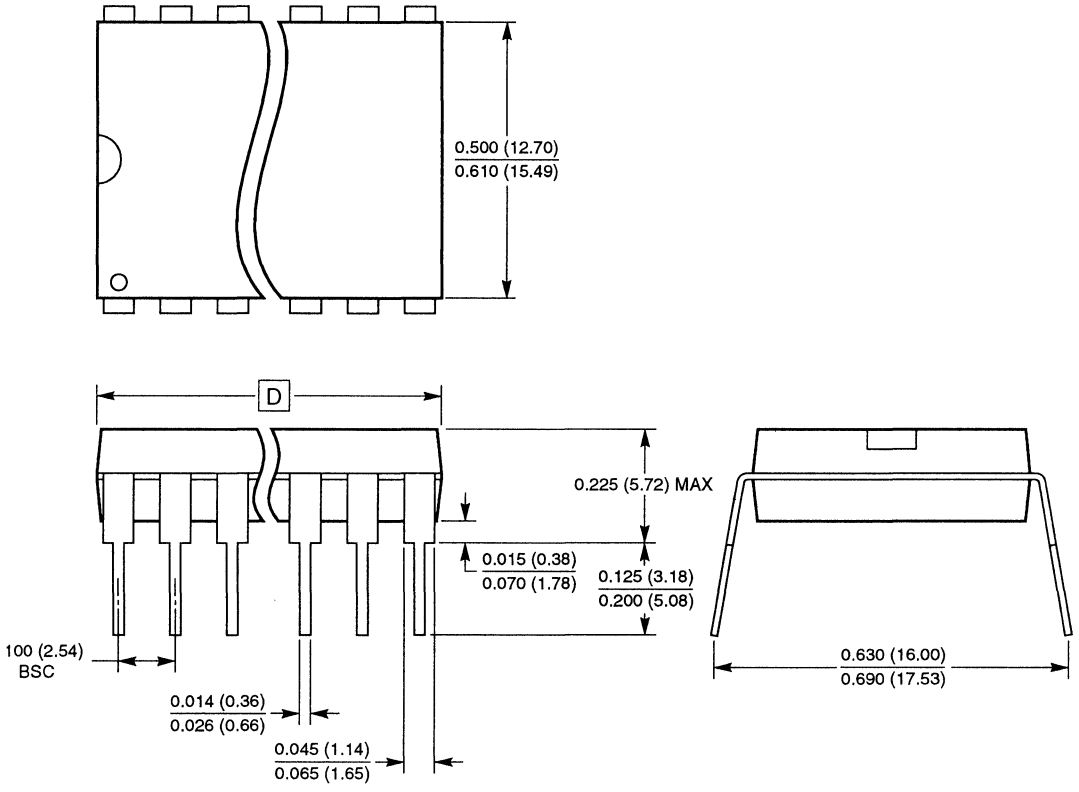
8 AND 14-LEAD 300 MIL WIDE CERDIP (D)



Dimension D		
Pkg	**Min**	**Max**
8L		0.405(10.28)
14L		0.785(19.93)

Notes:
1. Complies with MIL-STD-1835 (D-4, D-1) Configuration A dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

–40-LEAD 600 MIL WIDE CERDIP (D)

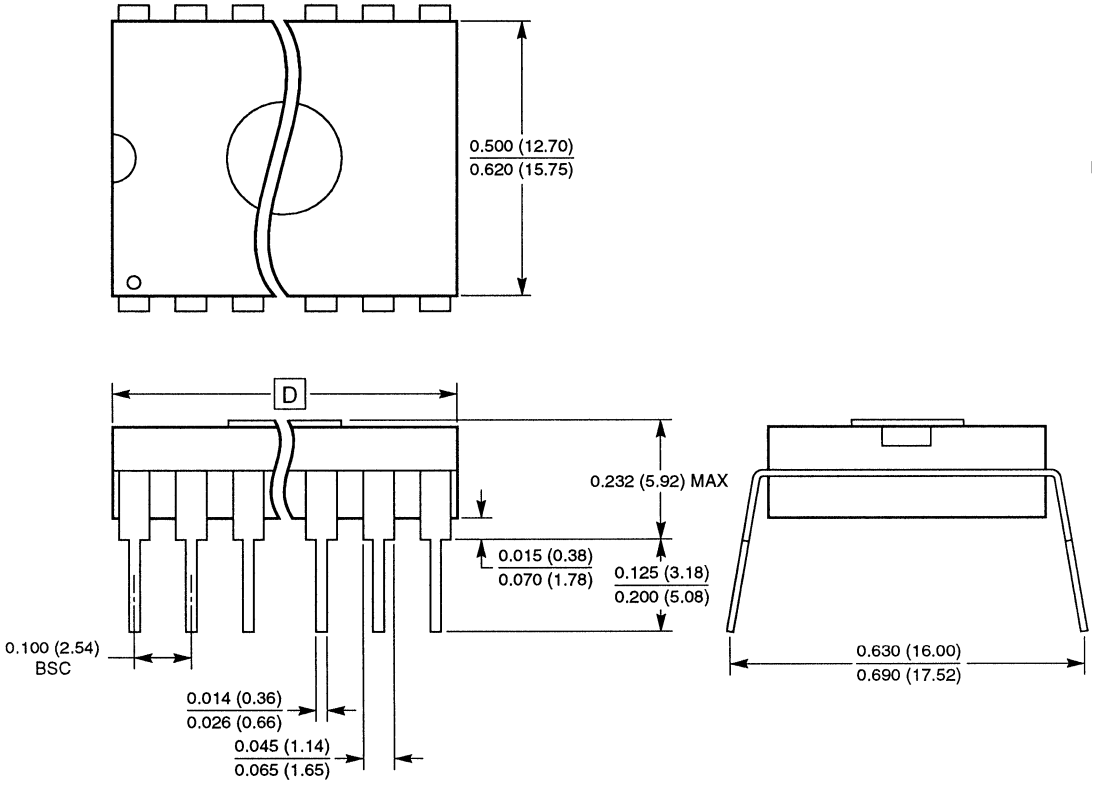


Dimension D		
Pkg	**Min**	**Max**
24L	1.235 (31.36)	1.285 (32.63)
28L	1.440 (36.57)	1.485 (37.71)
32L	1.635 (41.52)	1.685 (42.79)
40L	2.035 (51.68)	2.085 (52.95)

15

ote:
Complies with MIL-STD-1835 (D-3, D-10, N/A, D-5) Configuration A dimensions; however, some dimensions may be more stringent.
All linear dimensions are in inches and parenthetically in millimeters.

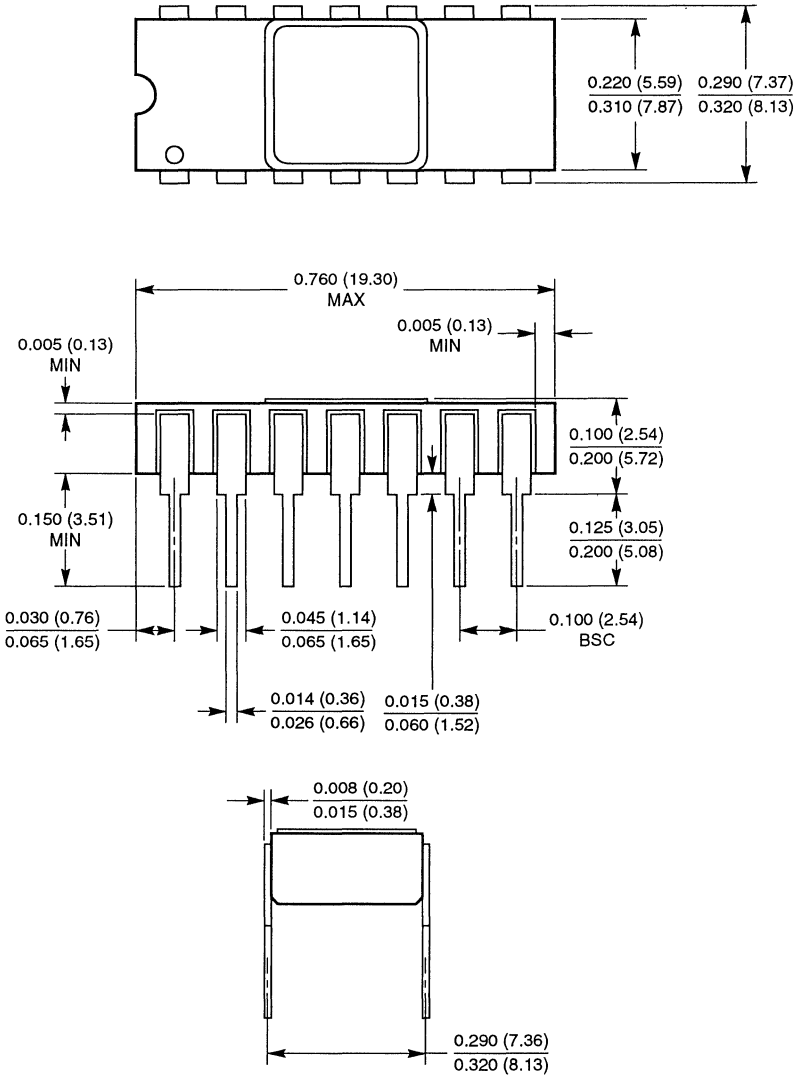
28–40-LEAD 600 MIL WIDE WINDOWED CERDIP (D)



Dimension D		
Pkg	**Min**	**Max**
28L	1.440 (36.57)	1.485 (37.71)
32L	1.635 (41.52)	1.685 (42.79)
40L	2.035 (51.68)	2.085 (52.95)

Notes:
1. Complies with MIL-STD-1835 (D-10, N/A , D-5) Configuration A dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

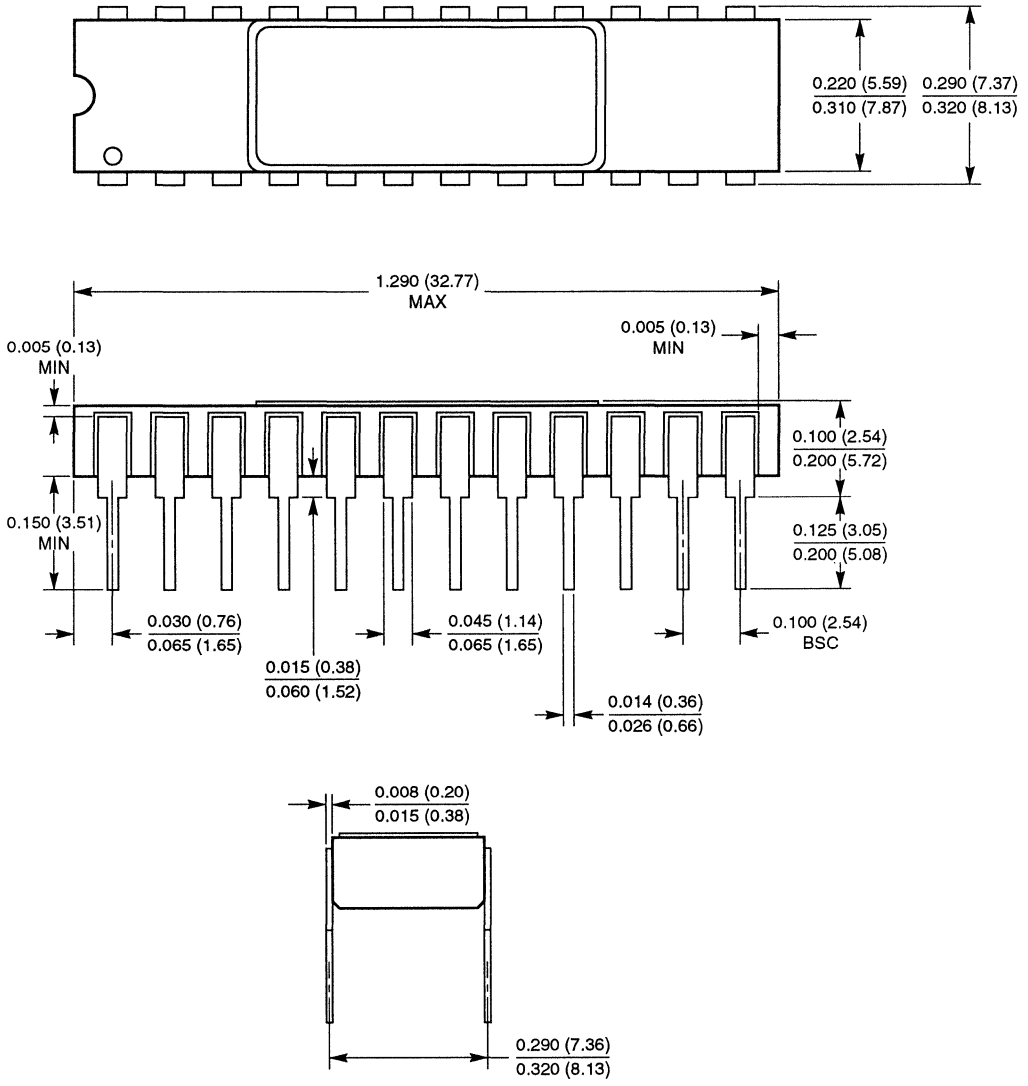
-LEAD 300 MIL WIDE SIDEBRAZE (C)



15

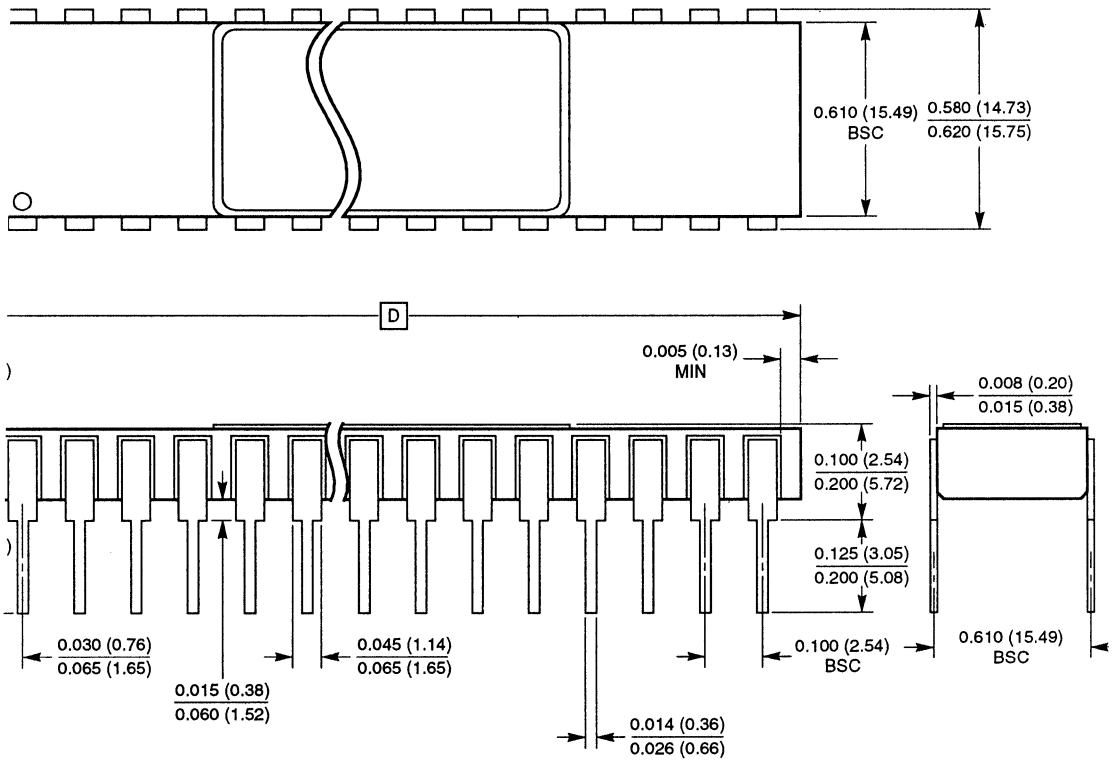
otes:
Complies with MIL-STD-1835 D-1, Configuration C dimensions; however, some dimensions may be more stringent.
All linear dimensions are in inches and parenthetically in millimeters.

24-LEAD 300 MIL WIDE SIDEBRAZE (C)



Notes:
1. Complies with MIL-STD-1835 D9, Configuration C dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

–48-LEAD 600 MIL WIDE SIDEBRAZE (C)



Dimension D		
Pkg	**Min**	**Max**
28	1.390(35.30)	1.430(36.32)
32	1.590(40.38)	1.630(41.40)
40	1.990(50.54)	2.030(51.56)
44	2.190(55.62)	2.230(56.64)
48	2.390(60.70)	2.430(61.72)

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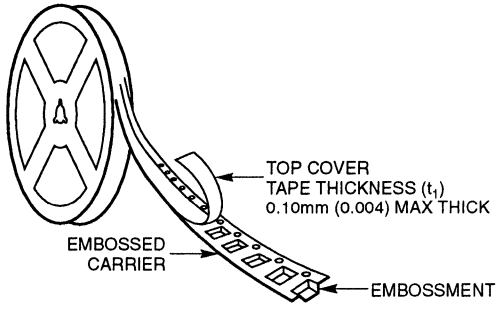
otes:
. Complies with MIL-STD-1835 (D-10, N/A, D-5, N/A, D-14) Configuration C dimensions; however, some dimensions may be more stringent.
. All linear dimensions are in inches and parenthetically in millimeters.

TAPE AND REEL

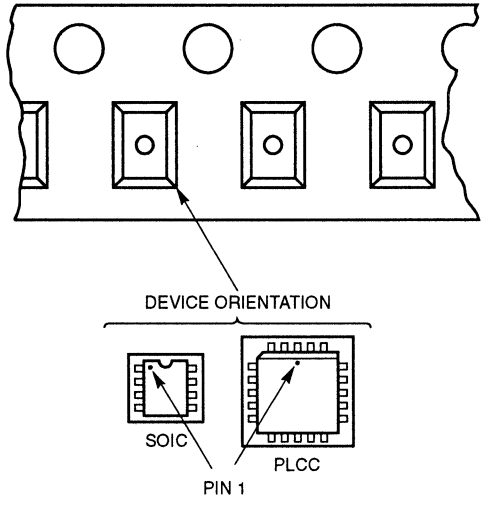
Catalyst surface mount devices, which are normally shipped in antistatic plastic tubes, are also available mounted on embossed tape for customers using automatic placement systems. The tape is wound on 178mm (7 inch) or 330mm (13 inch) reels and individually packaged for shipment.

The following tables and diagrams provide general t and reel specification data and indicate the tape sizes various package types. Further tape and reel specifi tions can be found in the Electronic Industries Associat (EIA) standard 481.

Direction of Feed



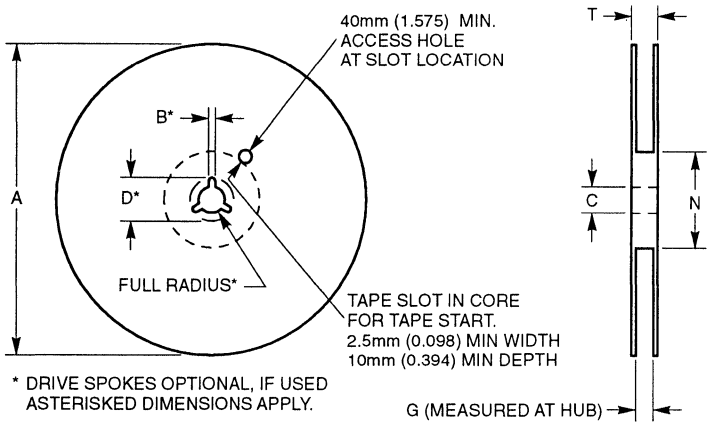
Device Orientation



Note:
(1) Metric dimensions will govern; English measurements rounded, for reference only and in parentheses.

ΛPE AND REEL

ːel Dimensions[1]



Tape Size	A				B	C	D*	N	G	T
	Max.	Qty/Reel	Max.	Qty/Reel	Min.		Min.	Min.		Max.
12mm	178 (7.00)	500	330 (13.00)	2000	1.5 (0.059)	12.80 (0.504) / 13.20 (0.520)	20.2 (0.795)	50 (1.969)	12.4 (0.488) / 14.4 (0.558)	18.4 (0.724)
16mm	178 (7.00)	500		2000					16.4 (0.646) / 18.4 (0.724)	22.4 (0.882)
24mm	N/A			500					24.4 (0.961) / 26.4 (1.039)	30.4 (1.197)

ɔmponent/Tape Size Cross-Reference

Component	Package Type	Tape Size (W)	Part Pitch (P)
8-Lead SOIC	J, S	12mm	8mm
8-Lead SOIC	K	16mm	12mm
14-Lead SOIC	J14	16mm	8mm
16-Lead SOIC	J	16mm	12mm
20-Lead SOIC	J	24mm	12mm
24-Lead SOIC	J, K	24mm	12mm
28-Lead SOIC	J, K	24mm	16mm
32-Lead PLCC	N	24mm	16mm

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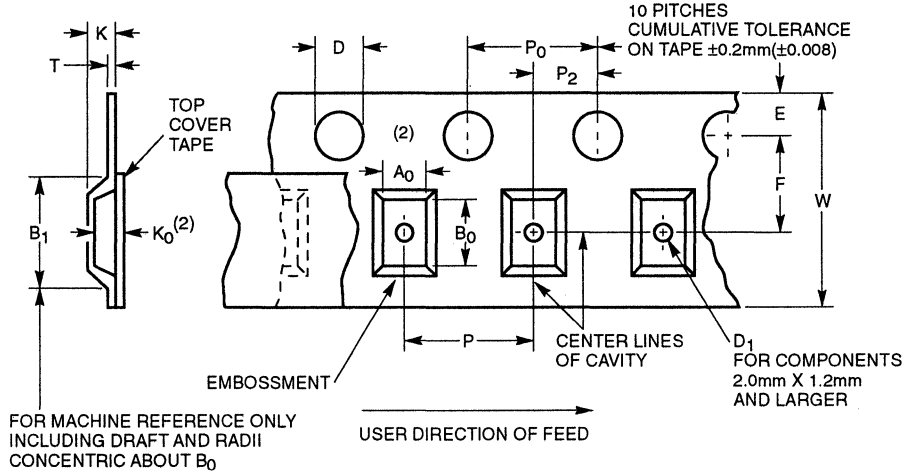
ote:
) Metric dimensions will govern; English measurements rounded, for reference only and in parentheses.

TAPE AND REEL

Embossed Carrier Dimensions (12, 16, 24mm Tape Only)



Embossed Tape—Constant Dimensions(1)

Tape Size	D	E	P_0	T Max.	D_1 Min.	A_0 B_0 K_0(2)
12, 16, 24mm	1.5 (0.059) 1.6 (0.063)	1.65 (0.065) 1.85 (0.073)	3.9 (0.153) 4.1 (0.161)	0.400 (0.016)	1.5 (0.059)	

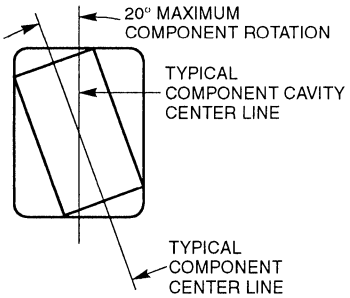
Embossed Tape—Variable Dimensions(1)

Tape Size	B_1 Max.	F	K Max.	P_2	R Min.	W	P
12mm	8.2 (0.323)	5.45 (0.215) 5.55 (0.219)	4.5 (0.177)	1.95 (0.077) 2.05 (0.081)	30 (1.181)	11.7 (0.460) 12.3 (0.484)	7.9 (0.275) 8.1 (0.355)
16mm	12.1 (0.476)	7.4 (0.291) 7.6 (0.299)	6.5 (0.256)	1.9 (0.075) 2.1 (0.083)	40 (1.575)	15.7 (0.618) 16.3 (0.642)	11.9 (0.468) 12.1 (0.476)
24mm	20.1 (0.791)	11.4 (0.449) 11.6 (0.457)			50 (1.969)	23.7 (0.933) 24.3 (0.957)	11.9 (0.468) 12.1 (0.476) 15.9 (0.623) 16.1 (0.634)

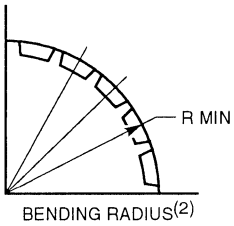
Note:
(1) Metric dimensions will govern; English measurements rounded, for reference only and in parentheses.
(2) A_0 B_0 K_0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) min. to 0.65 (0.026) max. for 12mm tape, 0.05 (0.002) min. to 0.90 (0.035) max. for 16mm tape, and 0.05 (0.002) min. to 1.00 (0.039) max. for 24mm tape and larger. The component cannot rotate more than 20° within the determined cavity, see Component Rotation.

ΛPE AND REEL

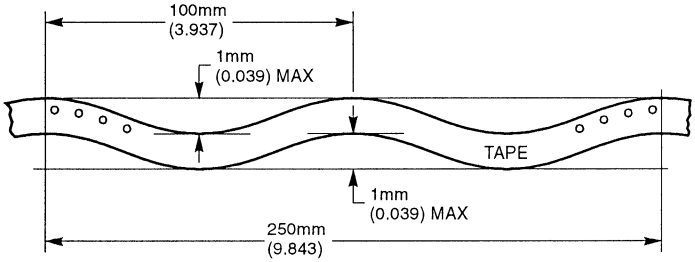
›mponent Rotation



Bending Radius



ıpe Camber (Top View)



ALLOWABLE CAMBER TO BE 1mm/100mm NONACCUMULATIVE OVER 250mm

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ɔte:
) Metric dimensions will govern; English measurements rounded, for reference only and in parentheses.
:) Tape and components shall pass around radius "R" without damage.

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