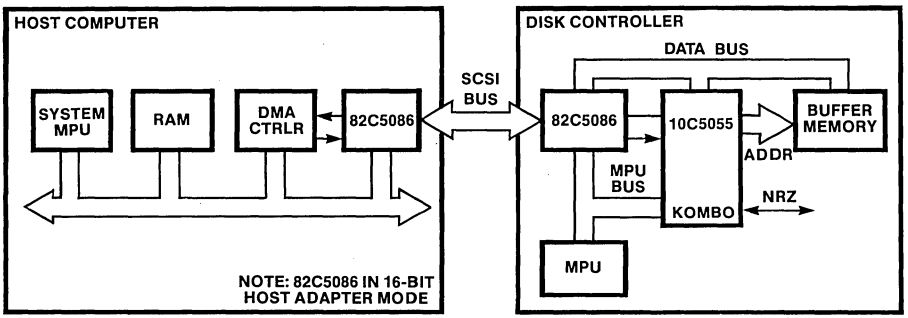
82C5086B SYNCHRONOUS/ASYNCHRONOUS SCSI PROTOCOL CONTROLLER

- 5.3 Megabyte Data Transfer Rate
- Support for Wide SCSI Bus
- Internal State Machine
- 64-Byte FIFO—Offset of 63
- 16-Bit Host Interface
- Queue for Four SCSI Command Sequences
- Pipelined Commands Plus Control Queuing
- Powerful Command Set: One Command Performs Any One of a Variety of Initiator or Target Sequences
- Multiported Bus Structure
- Pipelining for Up to Four Commands
- 6 Separate On-Chip 32-Byte Scripts for SCSI Command and/or Message Queuing
- Synchronous Transfer Mode Provides:
  - — Sustained Data Transfer Rates of 5.3 Megabytes/Second
  - — Programmable Offset to 63 (64-Byte FIFO)
- Asynchronous Data Transfer Rates up to 4 Megabytes/Second
- Single-Ended Drivers and Receivers
- Support for Differential Drivers and Receivers
- Support for Wide SCSI Bus (Multiples of 8 Bit)
- Connects to Non-Multiplexed and Multiplex Address/Data Microprocessor Bus
- Clock Rate Up to 32MHz
- Pin-Compatible with 10C5080 Asynchronous SCSI Controller
- 68-Pin and 84-Pin Plastic Leadless Chip Carrier, 80-Pin Flat Pack
- Low Power, Advanced 1.5 μ CMOS Technology



Typical System Configuration Using the 82C5086

The 82C5086 provides an interface between a host or peripheral device, and the SCSI (Small Computer System Interface) bus.

An impressive combination of hardware and firmware features makes this a powerful chip, with an unbeatable data transfer rate of 5.3 MBytes/sec. in synchronous mode, at a clock rate of 32MHz (transfer rate in asynchronous mode is 4MBytes/sec.). The chip is built using proven CMOS low-power technology.

Hardware Features

The 82C5086 can support both a single-ended and differential 8-bit SCSI interface. It can be used to implement SCSI host adapters and for providing a SCSI port on the motherboard. It provides a 16-bit gateway for SCSI devices such as printers and disk drives to access host memory. The 16-bit bus maximizes the data transfer rate, passing two bytes per cycle. The chip also has a separate memory data bus, which contributes to its high-speed performance. Data does not have to wait for control signals to clear from the bus.

Hardware on the 82C5086 performs command, status, message and data transfers, increasing the bandwidth of the SCSI bus, and leaving the on-board microprocessor (state machine) free to handle task scheduling and resource allocations. The wide SCSI bus (greater than 8 bits) is supported by the 80-pin flat-pack version of the chip by cascading devices.

The 82C5086 has two segments of memory. The 64-Byte FIFO is the largest available in the industry. It smooths out data transfers and increases system performance. The second segment, the MCS (Message Command Script), consists of 6 individual 32-Byte segments. The memory is a useful tool for firmware engineers, who can package blocks of commands, store them in the MCS, and access them as a sequence. There are two MCS address pointers, so that the MPU (Microprocessing Unit) can be processing on one segment, while the internal State Machine is accessing another 32-Byte segment.

The 82C5086 can interface to both multiplexed and non-multiplexed microprocessor buses, making it compatible with a variety of microprocessor product lines. Use of differential receivers and drivers enables the 82C5086 to support operation over cables up to 25 meters long.

Firmware Features

The large instruction set gives more control to the programmer, and enables higher system performance. Command queuing, with pipelining, permits up to four SCSI commands to be set up for the SCSI bus, and allows the 82C5086 to sequence through several SCSI bus phases without microprocessor intervention. As each command is executed, an interrupt may be generated for the host, providing tight status control. Using the 32-Byte scripts, programmers can tailor their own applications.

The register set is organized to give maximum programming flexibility. Registers record all commands executed, and keep records of previous executions. This makes it easy to monitor command flow, and facilitates error recovery.

The 82C5086 is a cost-effective design solution. It is available in a number of package options, and can be purchased with or without firmware, or standalone.

I/O Specifications:

8-bit address/data bus

8-bit memory data bus

8-bit SCSI bus

16-bit host adapter bus

I/O Ports:

4-bit ID

Operation:

Synchronous

Asynchronous

Operating Modes:

Target

Initiator

16-bit host adapter

Master/slave

The 82C5086 controller is available in three packages:

68-pin PLCC version:

Connects only to multiplexed address/data bus (Z8, 80188, 8085/8051). Compatible with the 82C5080

80-pin Flat Pack:

Supports wide SCSI buses and differential interfaces

Connects multiplexed address/data bus

Connects directly to non-multiplexed microprocessor bus

84-pin PLCC version:

Connects directly to AT bus (data bus drivers required)

Timing:

32MHz clock rate

5.3 Mbytes/sec. transfer rate in synchronous mode

4 Mbytes/sec. transfer rate in asynchronous mode

MPU strobe cycle times—100ns read/write

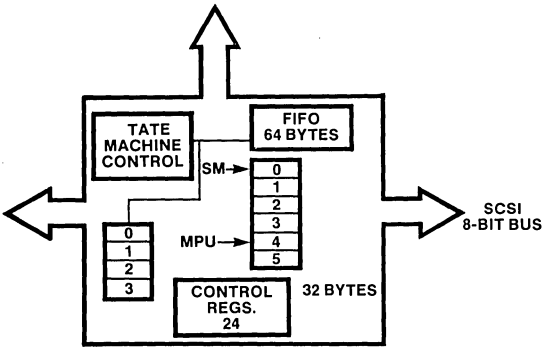
Command overhead—25 microseconds

Register Set:

24 registers

Command Set:

46 commands



82C5086 Block Diagram

Chips and Technologies, Inc.
3050 Zanker Road, San Jose, CA 95134 408-434-0600 telex 272929 CHIPS UR