82C575
COMMUNICATION MICROCHANNEL™ INTERFACE CHIP

- **Compatible with IBM Microchannel™ specifications**
- **Provides highly integrated Microchannel™ compatible interface solution for most communication adapter applications**
- **Suitable for most 8 bit slave IO peripheral applications**
- **Unique and flexible Card ID assignment**
- **Supports POS registers**
- **Four POS register bit outputs for system configuration**
- **Resource relocation capability to avoid address conflict**
- **Dual resource relocators to support multiple peripherals per card**
- **Sophisticated Card Channel Ready signal generator**
- **On chip system wait state generator**
- **Low power CMOS technology**
- **68 pins PLCC package**

The 82C575 is a highly integrated Microchannel™ compatible interface chip for use in personal computer applications compatible with the IBM PS/2 standard. It supports the Microchannel™ compatible interface to most of the 8 bit IO slave devices. The adapter IO address can be programed during the setup procedure, this resource relocation capability avoids adapter address conflicts. The interrupt level can also be selected via software. The on-chip wait state generator allows the user to optimize the system bus timing to his/her specific needs. A unique Card ID generator does not require any external components.

All these features greatly simplify the design of a circuit to interface to the Microchannel™ compatible bus.

The 82C575 supports application markets such as intelligent Modems, SDLC/BISYNC/UART adapter card applications, instrumentation, etc. The dual resource relocater provides the capability to support multiple peripheral system with a maximum of 32 IO address space.

The 82C575 is fabricated using advanced CMOS technology and is packaged in a 68 pin PLCC.

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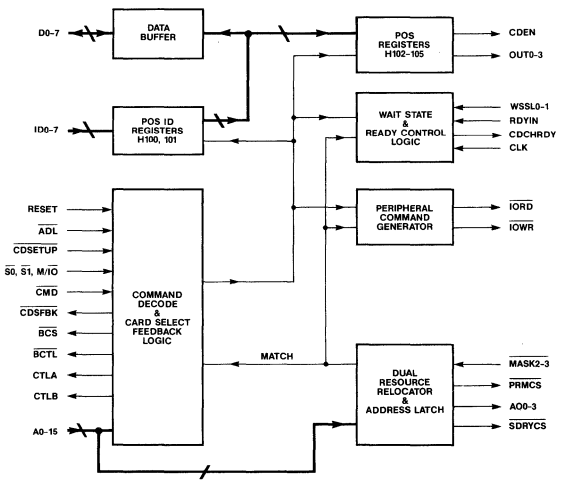
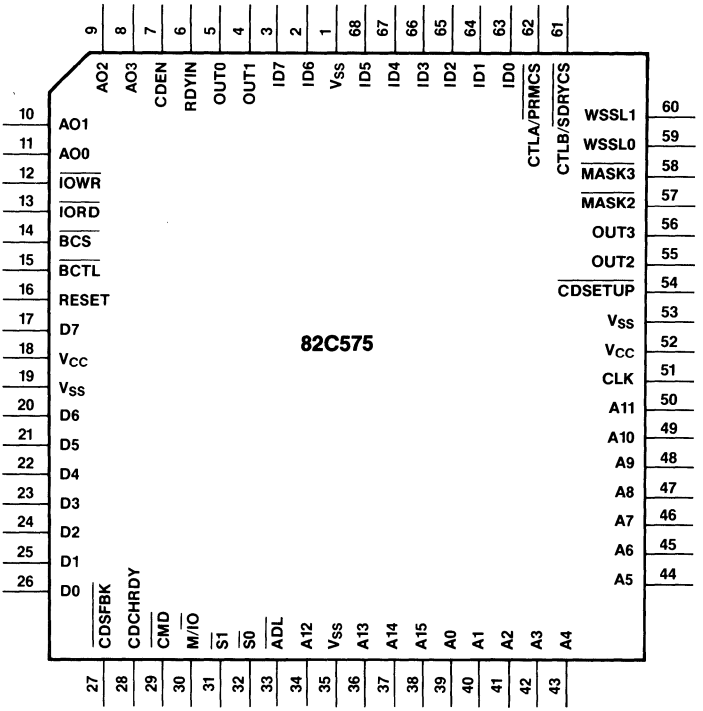


Figure 1. 82C575 Functional Block Diagram


82C575
1 VSS
2 ID6
3 ID7
4 OUT1
5 OUT0
6 RDYIN
7 CDEN
8 AO3
9 AO2
10 AO1
11 AO0
12 IOWR
13 IORD
14 BCS
15 BCTL
16 RESET
17 D7
18 VCC
19 VSS
20 D6
21 D5
22 D4
23 D3
24 D2
25 D1
26 D0
27 CDSFBK
28 CDCHRDY
29 CMD
30 M/IO
31 S1
32 S0
33 ADL
34 A12
35 VSS
36 A13
37 A14
38 A15
39 A0
40 A1
41 A2
42 A3
43 A4
44 A5
45 A6
46 A7
47 A8
48 A9
49 A10
50 A11
51 CLK
52 VCC
53 VSS
54 CDSETUP
55 OUT2
56 OUT3
57 MASK2
58 MASK3
59 WSSL0
60 WSSL1
61 CTLB/SDRYCS
62 CTLA/PRMCS
63 ID0
64 ID1
65 ID2
66 ID3
67 ID4
68 ID5

82C575 Pin Description

Pin No.	Pin Type	Symbol	Description
63-68 2-3	I I	ID0-5 ID6-7	Adapter Identification bits 0 to 7 for both low byte (Register 100) and high byte (Register 101). ID0 is the least significant bit (LSB) and ID7 is the most significant bit (MSB). The individual multiplexed ID bit can be tied to V_{CC}, V_{SS}, CTLA or CTLB according to the following table: V_{CC}: IF both high and low byte bits are "1". V_{SS}: If both high and low byte bits are "0". CTLA: If high byte bit is "0" and low byte bit is "1". CTLB: If high byte bit is "1" and low byte bit is "0". The values of these pins are returned by executing a READ ID command during the adapter setup operation. The input buffers have internal pullup resistors. They can be left floating instead of being tied to V_{CC}.
5-4 55-56	O O	OUT0-1 OUT2-3	Outputs from POS register 102 bits 1 to 4. They can be used as the general purpose control signals for the system configuration, such as interrupt level selection.
6	I	RDYIN	Active high Ready Input from a slow IO device. For external asynchronous extended channel cycle operation, CDCHRDY goes inactive at the begining of the cycle and stays inactive until a low to high transition is detected on RDYIN pin.
7	O	CDEN	Active high Card Enable. It is the output of POS register 102 bit 0.
8-11	O	AO3-0	Latched Address Output 3 to 0. These bits are latched by ADL and are used by the peripheral device to address the 82C575 internal registers.
12	O	$\overline{\text{IOWR}}$	Active low IO write strobe. It is the decoded command from CPU to load the information into the the registers of the externally addressed IO slave device. It goes active only when the IO address matches the primary or secondary resource relocater address.
13	O	$\overline{\text{IORD}}$	Active low IO read strobe. It is the decoded command from CPU to read the device registers. It goes active only when the IO address matches the primary or secondary resource relocater address.
14	O	$\overline{\text{BCS}}$	Active low 74LS245 buffer chip enable. It goes active if the internal POS registers or external IO device is addressed. (Either read or write operation.)
15	O	$\overline{\text{BCTL}}$	Active low external 74LS245 buffer transfer direction control signal. It becomes active during an IO READ operation if the POS registers or external IO device is addressed.

82C575 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
16	I	RESET	Active high hardware reset signal to initialize the chip. It should stay high for a minimum period of 500 ns.
17 20-26	B B	D7 D6-0	System data bits 7 to 0. These bits are used to transfer the data to and from the CPU data bus during the configuration cycle. They are 3-state bidirectional lines.
27	O	$\overline{\text{CDSFBK}}$	Active low Card Select Feedback. This signal goes active when an IO slave peripheral is addressed by the host. It stays inactive during a setup cycle.
28	O	CDCHRDY	Card Channel Ready. This signal is used by an external slow peripheral device to extend the channel cycle. During the setup operation, CDCHRDY always stays active and bus cycle is not extended. The maximum time CDCHRDY can stay inactive is 3 μs.
29	I	$\overline{\text{CMD}}$	Active low Command signal to define when data is valid on the data bus. It is used to generate the IO/memory read and write commands and is also used to latch the status signals.
30	I	M/$\overline{\text{IO}}$	Memory/Input Output. If M/$\overline{\text{IO}}$ is high, it indicates a memory cycle. If it is low, it indicates an IO cycle.
31 32	I I	$\overline{\text{S1}}$ $\overline{\text{S0}}$	Status bits 1 and 0. These signals indicate the start and the type of channel cycle. It is used with M/$\overline{\text{IO}}$ to generate the memory or IO read and write commands.
33	I	$\overline{\text{ADL}}$	Active low Address Decode Latch. It is used to latch the A0-3 address lines.
34 36-38 39-50	I I I	A12 A13-15 A0-11	System Address bits 15 to 0. These bits are used for the address decoding of the external IO device. They are also used to address the POS registers.
51	I	CLK	14.3 MHz System Clock. It is used to generate a system wait state.

M/$\overline{\text{IO}}$	$\overline{\text{S0}}$	$\overline{\text{S1}}$	Function
0	0	0	Reserved
0	0	1	IO Write
0	1	0	IO Read
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Memory Write
1	1	0	Memory Read
1	1	1	Reserved

82C575 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
54	I	CDSETUP	Active low Card Setup enable signal. During configuration and error recovery procedures, CDSETUP becomes active along with IO Read/Write commands to access the POS registers.
57 58	I I	MASK2 MASK3	Active low mask bits for the comparators of both primary and secondary relocaters. When a mask bit is low, the comparison of the corresponding address input (A2-3) with the relocater address bits 2 to 3 is bypassed. The input buffers have internal pull up resistors. They can be left floating for a "1" value.
59 60	I I	WSSL0 WSSL1	Wait State Selection signals. They are used to control the system wait state.

WSSL1	WSSL0	Function
0	0	Synchronous Extented bus cycle
0	1	Synchronous Wait State 1
1	0	Synchronous Wait State 2
1	1	External asynchronous Extented bus cycle

Synchronous Extended bus cycle is used for 120 ns (Max) read access time peripheral. Synchronous Wait State 1 is for the 250 ns (Max) Read delay time device and Synchronous Wait State 2 for the 460 ns (Max) read delay time peripheral. The External asynchronous Extended bus cycle is used to extend the system bus cycle by using the external RDYIN control signal.

62 61	O O	CTLA/PRMCS CTLB/SDRYCS	In set-up cycle, they are Control Output signals for the adapter identification bits. CTLA goes active high while reading the low byte ID (Register 100). CTLB becomes active while reading the high byte ID (Register 101). In normal operation cycle, those two pins are Peripheral Chip Select signals. PRMCS goes active low when the IO address matches the primary resource relocater address. SDRYCS goes active low when IO address matches the secondary resource relocater.
18,52	I	V_{CC}	5V Power Supply.
1,19, 35,53	I	V_{SS}	Power Supply Ground.

Note: I = Input
O = Output
B = Bidirectional

82C575 Functional Description

The 82C575 block diagram is illustrated in Fig 1. The chip consists of the following functional blocks:

- POS Registers
- Peripheral Commands and Card Select Feedback Generator
- Dual Resource Relocator Logic
- Wait state and Card Channel Ready Signal Generator

POS Registers

A total of 6 POS registers are supported by 82C575. These registers can be accessed only during configuration cycle by activating CDSETUP, M/IO to low. The description of each register are as follows:

1. 100H: Low Byte ID Register.

Bit	7	6	5	4	3	2	1	0
	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

This register is a read only register. The reading of this register returns the contents of pins ID7-ID0.

2. 101H: High Byte ID Register.

Bit	7	6	5	4	3	2	1	0
	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8

This register is a read only register. The reading of this register returns the contents of pins ID7-ID0.

The ID7 to 0 are the multiplexed pins for both low and high ID bytes. Each individual bit can be tied to V_{CC}, V_{SS}, CTLA or CTLB depending on the bit value in the high and low byte register as described in the pin description. For example if 100 low byte ID is "00110110" and 101 high byte ID is "01011010" starting with MSB, ID7 should be tied to V_{SS}, ID6 to CTLB, ID5 to CTLA, ID4 to V_{CC}, ID3 to CTLB, ID2 to CTLA, ID1 to V_{CC} and ID0 to V_{SS}.

3. 102H: Control Register.

Bit	7	6	5	4	3	2	1	0
	SADR15	SADR14	SRDYEN	OUT3	OUT2	OUT1	OUT0	CDEN

Bits 1 to 4 are brought out to OUT0-3 pins. They can be used for system configuration.

Bits 5, 6 and 7 are used with registers 0103H, 0104H and 0105H and are described below.

Register 102H is readable and writable. All the bits are reset to "0" by RESET signal.

4. 103H: Low Byte Primary Card Address and Secondary Card Address Register.

Bit	7	6	5	4	3	2	1	0
	PADR7	PADR6	PADR5	PADR4	PADR3	PADR2	SADR8	SADR3

5. 104H: High Byte Primary Card Address Register.

Bit	7	6	5	4	3	2	1	0
	PADR15	PADR14	PADR13	PADR12	PADR11	PADR10	PADR9	PADR8

6. 105H: Secondary Card Address Register.

Bit	7	6	5	4	3	2	1	0
	X	X	SADR13	SADR12	SADR7	SADR6	SADR5	SADR4

The Card Address registers are read/write registers. They are used for resource relocation to avoid adapter conflicts. In case of the same adapter address, the host can reassign the board address. There are two sets of adapter address: Primary and Secondary. For Primary relocator, address bits 15 to 2 are programmable. For Secondary relocater, only bits 15 to 12, bit 8, bits 7 to 3 are programmable. SRDYEN (0102H bit 5) is used to enable the secondary address relocation feature: a zero enables the secondary address relocation registers. Bits 6 and 7 of 0105H are not used and will be read as one's. **The unprogrammed bits in the Secondary relocater (SADR11-9, SADR2) are the same value as the Primary address register bits.**

To generate IO read/write commands for the peripheral, or to activate the CDSFBK, or inactivate the CDCHRDY signals, the address from host A15 to A4 have to match the Primary or the Secondary address register bits. A3 or A2 may bypass the comparison if the individual mask bit is activated by forcing MASK3-2 pins to VSS. A1 to A0 will always bypass the

comparison. The PRMCS signal goes active low if the IO address matches the Primary address register. It can be used as the chip enable signal for the primary peripheral. The SDRYCS signal goes active low when IO address matches the secondary address register and SRDYEN = 0, and can be used as the chip enable for a secondary peripheral. **In case only the primary peripheral is used in a system, disable secondary address relocation (SRDYEN = 1).**

Peripheral Commands and Card Select Feedback Generator

The peripheral read/write command is generated by decoding the IO or memory address, M/IO, S0, S1, status and gating with CMD signal.

To generate IO read/write commands, the address from host needs to match the dual relocator card address as programmed in the POS registers.(A2-A3 comparison can be bypassed by activating MASK3 to MASK2 individually.)

The Card Select Feedback (CDSFBK) is used to inform the host that the adapter is selected. It stays inactive during a setup cycle. It is generated by decoding the IO address space and S0, S1 status. It should go active within 50 ns after Address and M/IO become valid and within 25 ns from the time status becomes active.

Dual Resource Relocator Logic

Two sets of the resource relocator address registers are supported in this chip. The operation of this block is described in the POS Registers section.

Wait State and Card Channel Ready Generator

The basic channel cycle time in an IBM PS/2 compatible system is 200 ns. It can be extended by using CDCHRDY signal. There are four ways to extend the cycle: Synchronous, Synchronous wait state 1, Synchronous wait state 2 and External Asynchronous.

During a setup cycle, the 82C575 requires no wait states for read/write operations from the host CPU, CDCHRDY is always active and no cycle extension is required. In normal IO operation, the bus cycle is always extended either synchronously or asynchronously.

When the peripheral is addressed, CDCHRDY will go low within 55 ns from the time M/IO and Address become valid (25 ns from the time status S0, S1 become valid) and then returns high within 25 ns after CMD becomes active. The bus cycle is extended from 200 ns to 300 ns, this is called a synchronous extention. This mode is for a peripheral that has a read access delay time of less than 120 ns.

For Synchronous wait state 1 operation, CDCHRDY will go low and stay low for 210 ns to 290 ns from the time CMD goes active. This mode is for a peripheral that has a maximum read access time of 250 ns.

For Synchronous wait state 2 operation, CDCHRDY will go low and stay low for 420 ns to 500 ns after CMD goes active. This can fit the application with the peripheral having read access delay time less than 460 ns.

For External Asynchronous operation, CDCHRDY will go inactive just like synchronous IO access but it will stay low until a low to high transition on pin RDYIN is detected. This mode is for the extremely slow peripheral access.

Application

Figure 2 show an application diagram for 8 bit IO slave peripherals. The Card ID is selected by tying ID0-7 to V_{CC}, V_{SS}, CTLA or CTLB according the table described in the pin description section. This provides a very flexible method for ID selection. Two resource relocaters are supported which make the multiple peripherals per card applications feasible. Address bits 0 to 3 are latched by the 82C575 for these peripherals. The 82C575 also provides the 74LS245 buffer chip select and direction control signals. The OUT0-3 and CDEN can be used for the system configuration such as interrupt level selection. Due to the high integration of the chip, only a few external components are required to implement a low cost, low parts count solution for Microchannel compatible adapter boards.

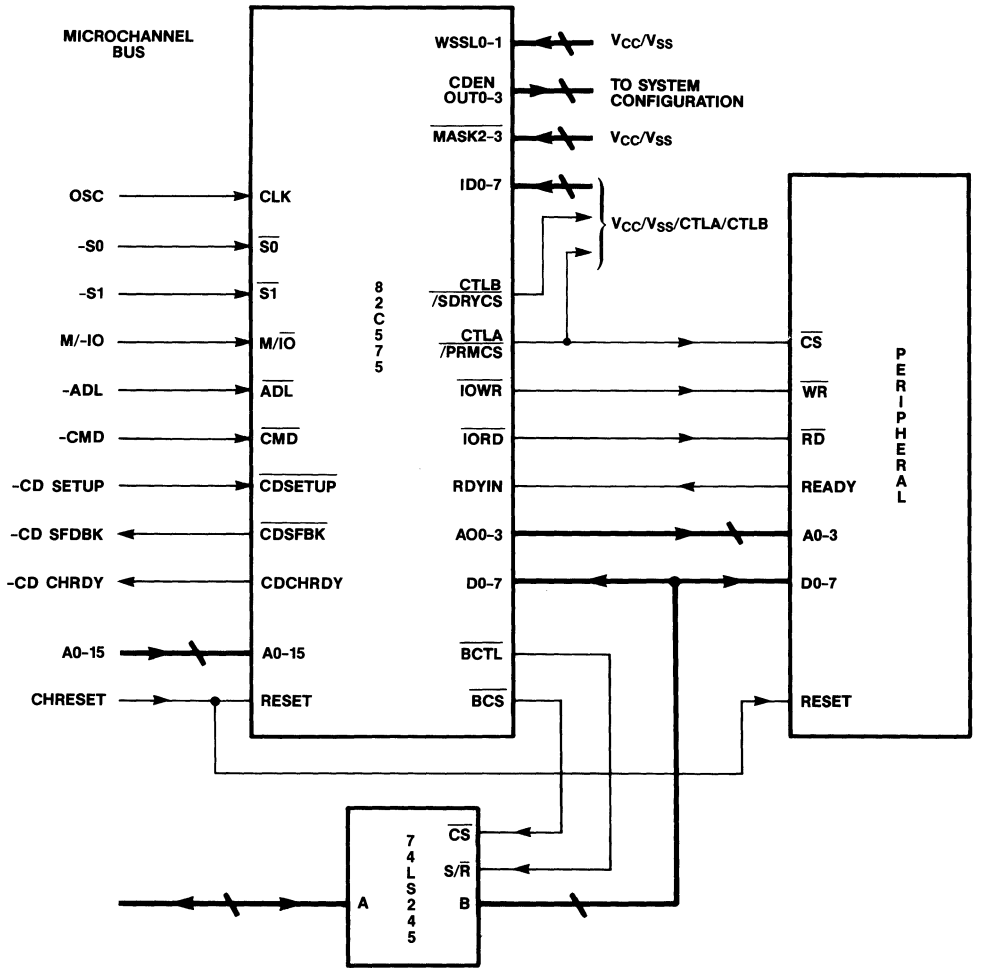


Figure 2. 82C575 Application Diagram for 8-Bit I/O Slave Peripheral

82C575 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}		7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operation Temperature	T_{op}	-25	85	°C
Storage Temperature	T_{stg}	-40	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operation Conditions.

82C575 Operation Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C

82C575 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Power Supply Current	I_{CC}		30	mA
Input Low Voltage	V_{IL}	-0.5	0.8	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V
Output Low Voltage (Note 1)	V_{OL}		0.4	V
Output High Voltage (Note 1)	V_{OH}	2.4		V
Input Leakage Current For V_{IN} = 0 to V_{CC} Pins ID0-7, MASK2-3	I_{IL1}	-100	100	μA
Input Leakage Current For all other input pins	I_{IL2}	-10	10	μA
Output Tri-State Leakage Current for V_O = 0 to V_{CC}	I_{OL}	-10	10	μA

Note 1: I_{OL} = 6 mA, I_{OH} = -2 mA for pins CDCHRDY , $\overline{CDSFBK}$. I_{OL} = 2.4 mA, I_{OH} = -400 μA for all other pins.

Capacitance (T_A = 25°C , V_{CC} = 0)

Parameter	Symbol	Min.	Max.	Units
Input Capacitance For F_C = 1 MHz	C_{IN}		10	pF
Output Capacitance	C_{OUT}		20	pF
I/O Capacitance	$C_{I/O}$		20	pF

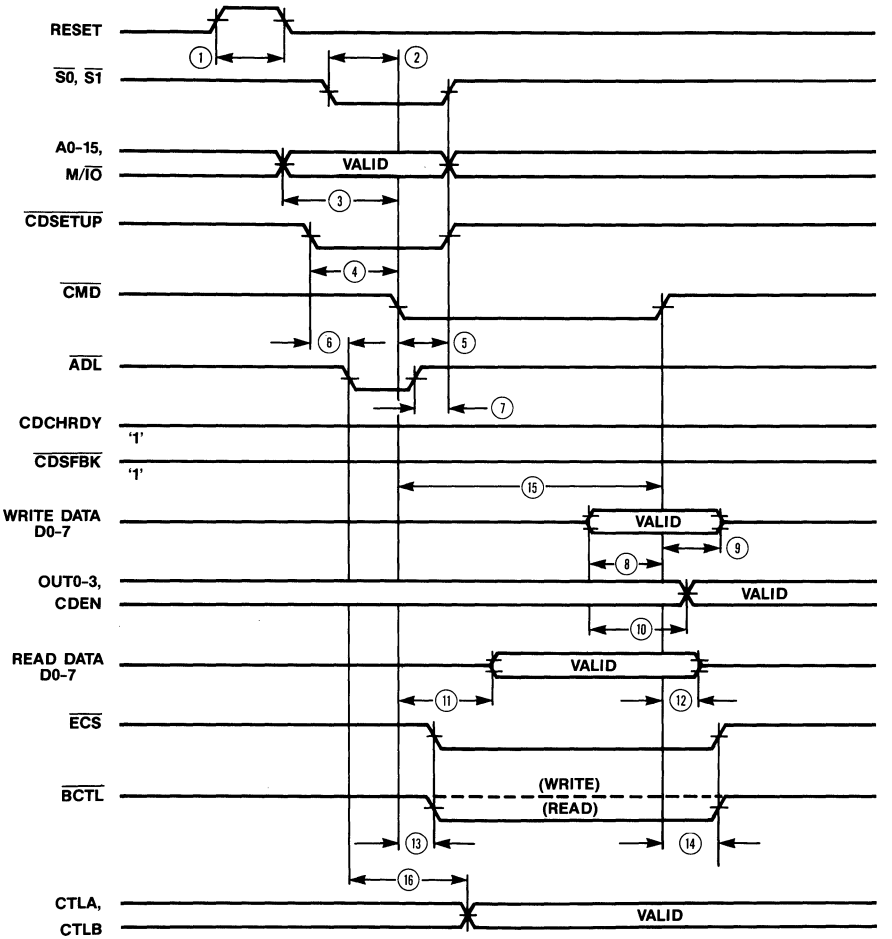
82C575 AC Characteristics
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5% , C_L = 60 pF for all the output pins)

Sym	Parameter	Min	Max	Units
t1	RESET Active Pulse Width	500		ns
t2	$\overline{S0}$, $\overline{S1}$ Set-up to $\overline{CMD}$ Active	50		ns
t3	A0-15, M/$\overline{IO}$ Set-up to $\overline{CMD}$ Active	80		ns
t4	$\overline{CDSETUP}$ Set-up to $\overline{CMD}$ Active	50		ns
t5	$\overline{S0}$, $\overline{S1}$, A0-15, M/$\overline{IO}$, $\overline{CDSETUP}$ Hold time from $\overline{CMD}$ Active	25		ns
t6	$\overline{CDSETUP}$ Setup time from $\overline{ADL}$ Active	15		ns
t7	$\overline{CDSETUP}$ Hold time from $\overline{ADL}$ Inactive	25		ns
t8	Write Data Set-up to $\overline{CMD}$ Inactive	30		ns
t9	Write Data Hold time from $\overline{CMD}$ Inactive	15		ns
t10	OUT0-3, CDEN Delay time from Data Valid		50	ns
t11	Read Data Delay from $\overline{CMD}$ Active		40	ns
t12	Read Data Hold time from $\overline{CMD}$ Inactive	5		ns
t13	$\overline{BCS}$, $\overline{BCTL}$ Assert Delay from $\overline{CMD}$ Active		40	ns
t14	$\overline{BCS}$, $\overline{BCTL}$ Deassert Delay from $\overline{CMD}$ Inactive	5	40	ns
t15	$\overline{CMD}$ Active Pulse Width in SETUP Cycle	90		ns
t16	CTLA, $\overline{CTLB}$ Assert and Deassert delay time from $\overline{ADL}$ Active	0	35	ns
t21	$\overline{ADL}$ Active to $\overline{CMD}$ Active	40		ns
t22	AO0-3 Delay from $\overline{ADL}$ Active	0	25	ns
t23	$\overline{CDSFBK}$ Active Delay from Address, M/$\overline{IO}$, Valid		55	ns
t24	$\overline{CDSFBK}$ Active Delay from Status Active		25	ns
t25	CDCHRDY Inactive Delay from Status Active		25	ns

82C575 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, C_L = 60 pF for all the output pins)

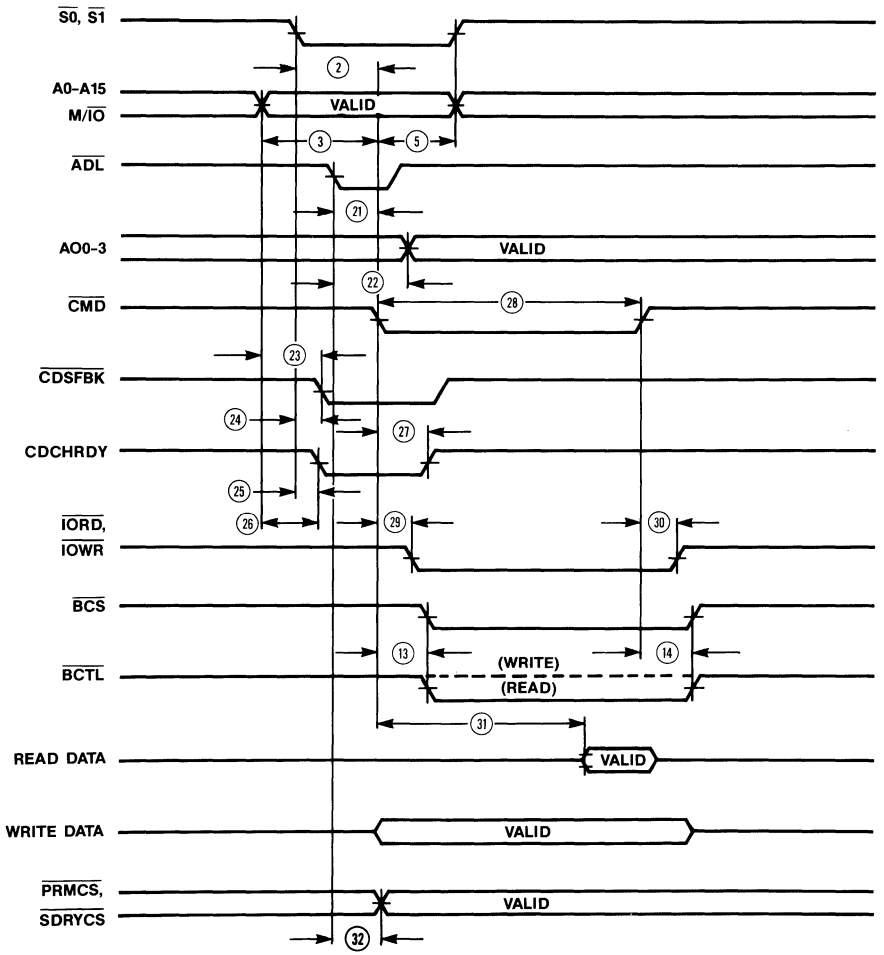
Sym	Parameter	Min	Max	Units
t26	CDCHRDY Inactive Delay from Address, M/$\overline{IO}$, Valid		55	ns
t27	CDCHRDY Release Delay from $\overline{CMD}$ Active in Synchronous Extended Cycle		25	ns
t28	$\overline{CMD}$ Active Pulse Width in both Sync and External Asyn Extended Cycles	190		ns
t29	$\overline{IORD}$, $\overline{IOWR}$ Active Delay from $\overline{CMD}$ Active		25	ns
t30	$\overline{IORD}$, $\overline{IOWR}$ Inactive Delay from $\overline{CMD}$ Inactive		25	ns
t31	READ DATA Valid from $\overline{CMD}$ Active in Sync Extended Cycle		140	ns
t32	$\overline{PRMCS}$, $\overline{SDRYCS}$ Assert and Deassert delay time from $\overline{ADL}$ Active		25	ns
t33	CLK High time	20		ns
t34	CLK Low time	20		ns
t35	CLK Cycle time	69	71	ns
t36	READ DATA Valid from CDCHRDY Active in External Async Extended, Synch Wait State 1 and Sync Wait State 2 bus cycle		40	ns
t37	CDCHRDY Release delay time from $\overline{IORD}$, $\overline{IOWR}$ going Active:			
	For Synchronous Wait State 1	210	290	ns
	For Synchronous Wait State 2	420	500	ns
t38	CDCHRDY Release delay time from RDYIN Active in External Async Extended cycle		40	ns

82C575 Timing Diagrams



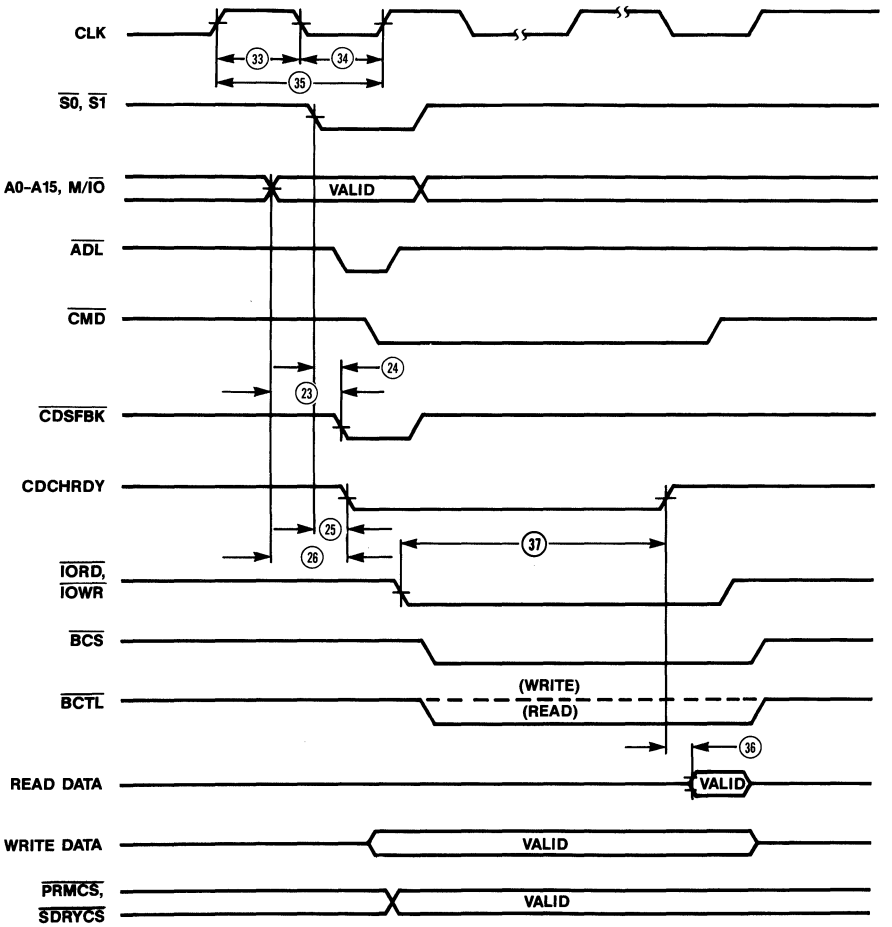
POS Register Setup Cycle Timing

82C575 Timing Diagrams (Continued)



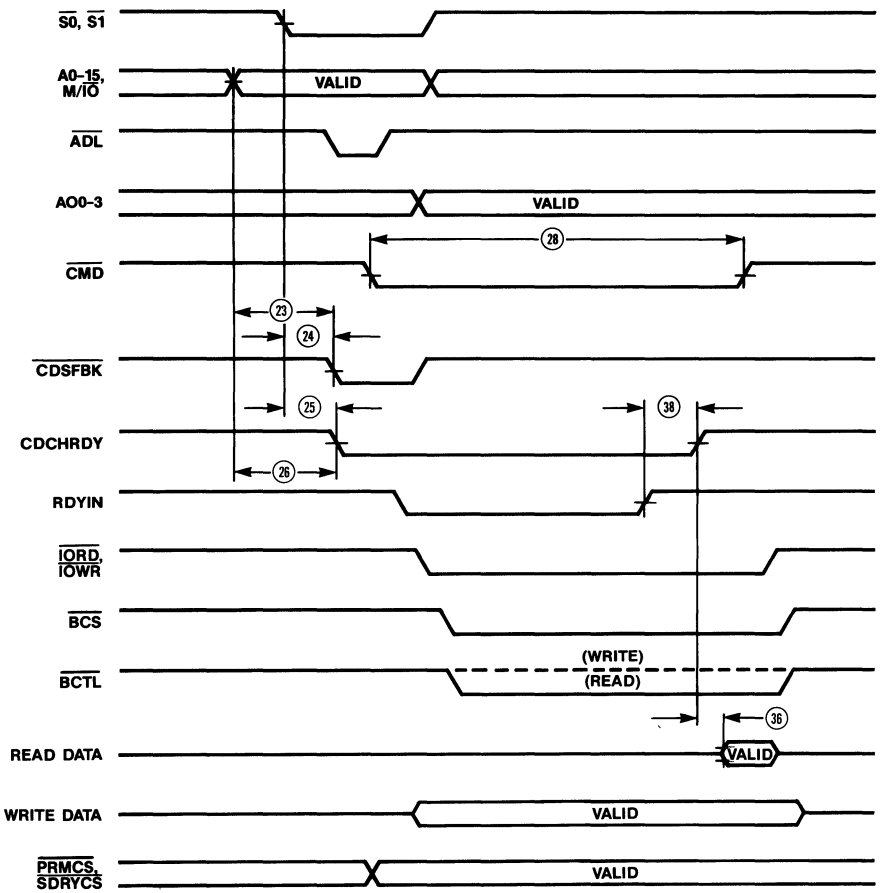
Synchronous Extended Cycle Timing

82C575 Timing Diagrams (Continued)



Synchronous Wait State 1 & Wait State 2 Cycle Timing

82C575 Timing Diagrams (Continued)



External Asynchronous Extended Cycle Timing

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