PS/2™ Technology

Total Integration: From Silicon Through Software

CHIPS

adaptec, inc.

Backgrounder

PS/2-COMPATIBLE PRODUCTS FROM CHIPS & TECHNOLOGIES AND ADAPTEC

Overview

Just as the IBM PC forever changed the personal computer market when it appeared in 1981, the IBM Personal System/2™ (Models 50, 60 and 80) will have a major impact on future product directions. Unlike IBM's first microcomputer family, however, the PS/2 was designed as a "clone-killer", thereby making the development of compatible systems a costly, complex, lengthy task.

However, the announcement of a tightly integrated solution for PS/2-compatible products from Chips & Technologies and Adaptec will allow personal computer manufacturers to quickly bring to market powerful PS/2 "desktop mainframes" with the highest level of performance found in any personal computers available today.

The essential logic and graphics circuits being introduced by Chips & Technologies work in tandem with Adaptec's advanced new I/O controller boards and SCSI host adapter, as well as with a special ROM-BIOS interface from Phoenix Technologies. This solution offers 100 percent compatibility with the Models 50, 60 and 80 PS/2s, Microsoft's DOS OS/2™ operating systems, the XENIX System V operating system from the Santa Cruz Operation.

This system solution provides the OEM with everything needed to develop high-performance PS/2-compatible computers, with the first such systems expected to appear by spring or summer. As the technology leaders in their respective markets, Adaptec and Chips & Technologies have utilized their innovative skills to create products that are compatible with -- and offer higher performance than -- IBM's PS/2 and its Micro Channel bus.

PS/2: The Future Standard

Reactions to the April 2, 1987 announcement by IBM of its new Personal System/2 family were strong. A few of those OEMs wedded to the PC family predicted -- at least publicly -- that this new generation of the IBM personal computers would never catch on. Many other companies in the personal computer marketplace viewed the introduction as evidence of a fundamental shift toward higher performance, with the PS/2 opening up demand for powerful, 16- and 32-bit small systems.

Analysts say IBM is staking the future of its personal computer business on the PS/2, having moved its production from the older PC machines to the new family. The company reports

good PS/2 sales, which contributed to a strong financial performance by the end of 1987 for its personal computer division.

Importance of SAA

The success of the PS/2 is important to IBM. One reason is because the PS/2 is a vehicle by which the company can begin to overcome a long-term problem: the incompatibility of its various systems, large and small. If the PS/2 and its Systems Application Architecture (SAA), an applications programming environment, become industry standards, a strong link will have been created between IBM's personal computers and larger systems, many of which use SAA. IBM probably hopes this will increase sales of its minicomputers and mainframes among users who desire communication and shared applications among all their systems. The computer giant is promoting SAA among software and hardware developers industry wide.

IBM's commitment to the PS/2 and the company's undeniable marketing clout have convinced most industry experts that the new personal computer family will become a standard.

PCs/ Yesterday and Today

Before the PS/2, it was less arduous for personal computer and peripheral manufacturers to make and market IBM PC compatibles, thanks to the well-documented, open architecture of these older systems and their use of off-the-shelf components. Many companies chose to compete with the IBM machines based on cost, with their compatible products undercutting the original. Adaptec and Chips & Technologies improved upon the original, offering PC-compatible makers products with high-performance features. These superior machines found an eager market.

IBM has made development much more difficult with its PS/2 family. The complex, VLSI logic chips that surround the Intel 80286 and 80386 microprocessors at the heart of the machines are proprietary, as is the Micro Channel bus architecture and many other crucial system components, none of which have been documented. The company has also created a unique, sophisticated I/O subsystem allowing fast transfer rates, multi-tasking and other features.

Despite the technical obstacles presented by IBM, most top system and component manufacturers are either considering or have already undertaken development projects for PS/2 compatible products.

Performance Increases

An examination of the evolution of personal computers reveals that ongoing performance improvements are a key to understanding the industry: from the first IBM PC to the more powerful PC-XT and AT, then the DOS-based "bridge" PS/2s (Model 25, 30) and the Models 50, 60 and 80 PS/2s with their Micro Channel.

Technology moves forward, not backward. A major factor fueling this evolution is the performance breakthroughs in IBM-compatible products from companies like Adaptec and Chips & Technologies that spur on IBM itself to improve its product line. For example, some of the most advanced PS/2 features like 1:1 interleave and ESDI 10 MHz drive support have been available in Adaptec controllers for years, although not for PC products until more recently.

At the same time, Chips & Technologies consistently offered leading-edge products. For example, the company pioneered PC-AT chip sets that allow the creation of 16-MHz '286 and 20-MHz '386 machines.

Development is Tough

The mission of emulating a desktop mainframe like the PS/2 demands much of a components manufacturer, who must design "new" products that are still fully compatible with the Micro Channel and OS/2. Mainframe-level design experience is necessary to accomplish this challenging development task, as well as the ability to comprehend the subtle, complicated relationships between the system components. These are not common skills.

It's clear what the OEM marketplace will want for a version of the PS/2: 100 percent compatibility with the original, complete integration of all components and performance features superior to those provided by IBM. In the scramble that will undoubtedly ensue as companies try to bring PS/2 compatibles to market in 1988 and 1989, these preferences will become increasingly evident.

The Companies

Market Leaders

Chips & Technologies and Adaptec have been at the forefront in their respective markets since their foundings. Using its superior integration skills, Chips & Technologies has captured 80% of the market for logic chip sets for IBM AT compatibles, doing in five chips what IBM accomplished with 63.

For the much more complex PS/2, Chips & Technologies has at least halved the component count compared to the original. For example, the company's Model 50 chip set has reduced the 119-chip IBM solution to just 68 devices. Other chip sets in the product family increase integration even more. But Chips' new products go beyond reducing component count. The company has built upon its experience in improving the PC AT architecture, offering OEMs PS/2 products that can decouple the processor speed from the I/O bus for overall system compatibility.

Adaptec, the performance leader in the PC-compatible controller business, also has a history of pioneering technological achievement. The company was the first to introduce 2,7 RLL

controllers for XT and AT systems, which increase capacity and transfer speed by 50 percent. Other firsts include non-interleaved ESDI controllers and high-performance, multitasking SCSI host adapters. The company's new PS/2 controllers provide the fastest direct memory access (DMA) transfer rate available today and include the industry's fastest synchronous SCSI host adapter. These new controllers are also the only PS/2-compatible products that offer multitasking.

With their products so often appearing concurrently within AT-compatible systems, these two firms have a close working relationship that began when they started cross-testing their AT products for compatibility. The backgrounds of the Adaptec and Chips and Technologies development staffs are similar: VLSI and system-level experience as well as a total of more than 200 man-years of mainframe engineering design expertise.

Integration is the Key

Besides their superior performance, the PS/2 products now being introduced by Adaptec and Chips & Technologies have been tightly integrated on all levels to ensure complete compatibility and maximum system operation. Behind this philosophy is the knowledge that system manufacturers can't afford any product delays while mismatched or non-optimized components are re-engineered.

This integrated approach extends to software support. These new products have been tested for total compatibility with Microsoft's MS-DOS and OS/2, including special features like Presentation Manager. In planning their products, Adaptec and Chips & Technologies investigated OS/2 in order to find ways of enhancing its performance.

Enthusiastic support of this system solution is being offered by The Santa Cruz Operation (SCO) and Phoenix Technologies. The Adaptec and Chips PS/2 products are fully compatible with SCO's industry-standard XENIX System V operating system and with a new Phoenix ROM-BIOS for the PS/2. Phoenix dominates the market for compatible BIOS interfaces for the PC family and shows evidence of doing the same with the new IBM family. The company developed a special implementation of its ROM-BIOS that supports the enhanced functionality and performance of Chips & Technologies' new product offering.

Customer Commitment

In aligning to produce truly integrated PS/2 products, Adaptec and Chips & Technologies have cooperated on both the development and service ends. The physical proximity of the two Silicon Valley companies has facilitated these efforts. Joint development consultations and extensive cross-compatibility testing of the various components were the first examples of this alliance.

Customer support begins during initial development. Chips & Technologies design services operation will help OEMs quickly create high-performance, compatible product families using Chips' system logic and graphics, along with Adaptec's innovative controllers and host adapters. This support is also available out in the field, with the two firms having cross-trained their respective sales organizations so that system manufacturers are told how to get the full benefit of these integrated products.

Patents and Copyrights

IBM has put together a variety of patents and copyrights to protect its new PS/2 Micro Channel products. However, the company's long-term practice has been to issue utility patent licenses. The licensees don't copy IBM's hardware, but rather create their own, different version.

While IBM is moving slowly in granting these utility patents, the company is encouraging software vendors and manufacturers of add-in boards to create PS/2 products. This strategy is obviously designed to promote the spread of its new product family, a goal that seems assured in any case.

Introducing the First Choice in PS/2 Technology

Total Integration: From Silicon Through Software

IBM's New PS/2 Rules

- Mainframe performance
- Mainframe compatibility strategy
  - Custom silicon
  - Proprietary software
  - Undocumented system architecture
- Mainframe family approach

Significance of the PS/2 Environment

- Compatibility is much tougher
- Compatibility requires significant investment
- Strong performance emphasis
- Closer hardware/software coupling
- More products, more often

Competing in the PS/2 Environment Requires

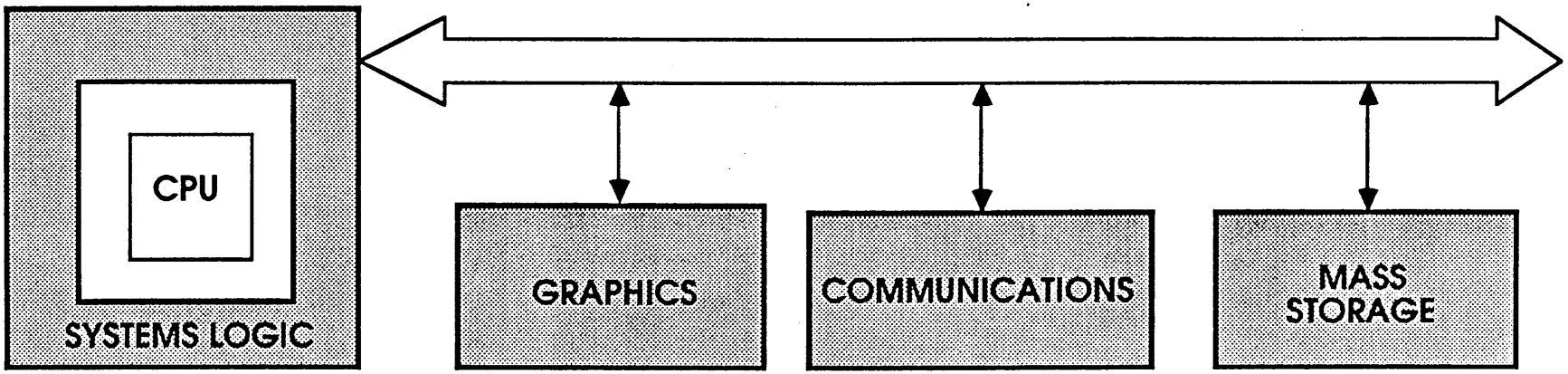
- Complete system understanding
- Mainframe performance capabilities
- Architectural and silicon integration
- Integrated hardware/software solutions
- Easy product migration and extension

Announcing PS/2 Solutions from CHIPS & Adaptec

CHIPS

Chips & Technologies

Complete CHIPSet Solutions for Microcomputers



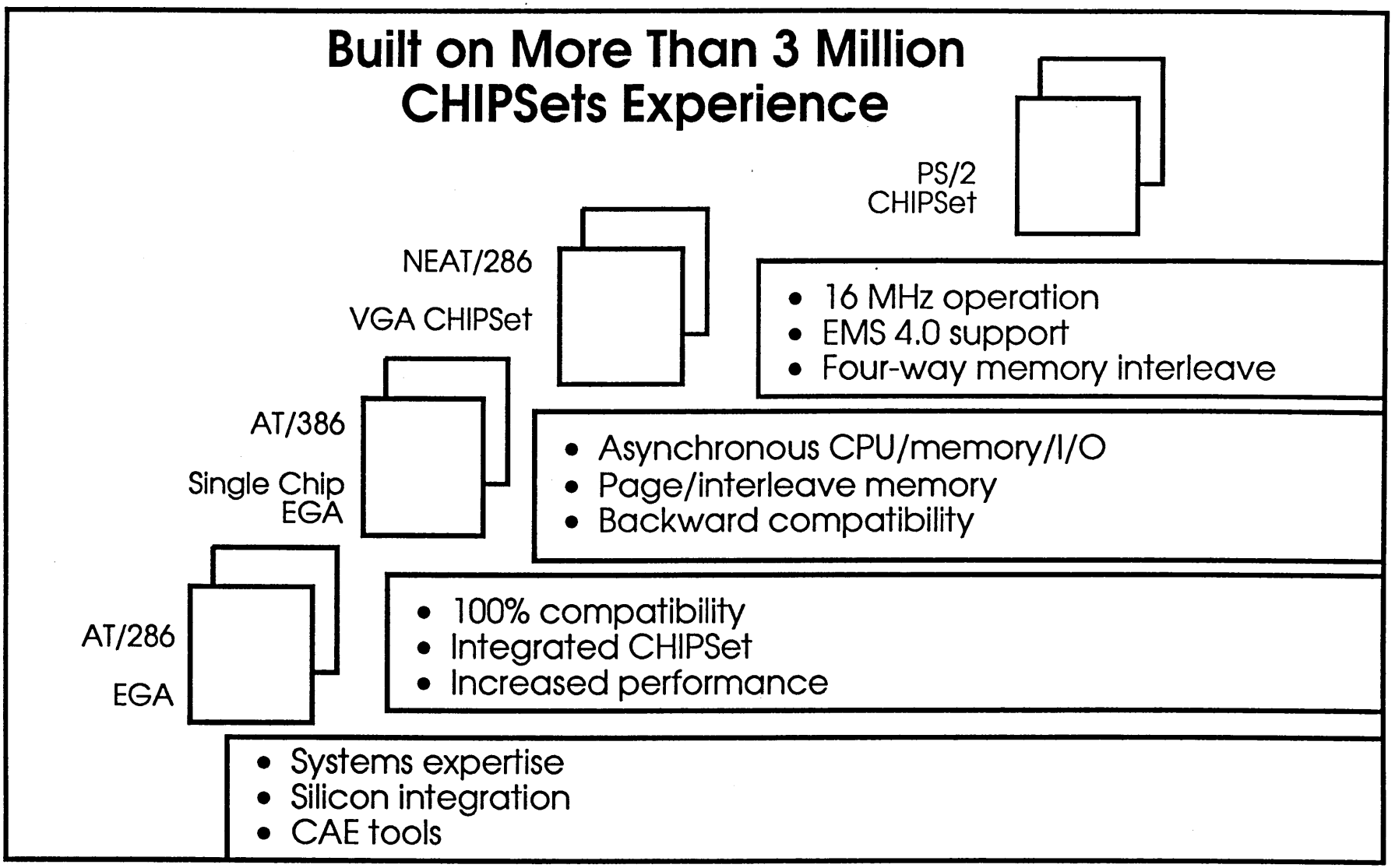
CPU CONTROL
MEMORY CONTROL
SYSTEM PERIPHERALS
I/O AND DMA CONTROL
KEYBOARD INTERFACE

EGA
VGA
LCD CGA

3270 COMM
SERIAL I/O PORTS

FLOPPY DISK
INTERFACE

Built on More Than 3 Million CHIPSets Experience

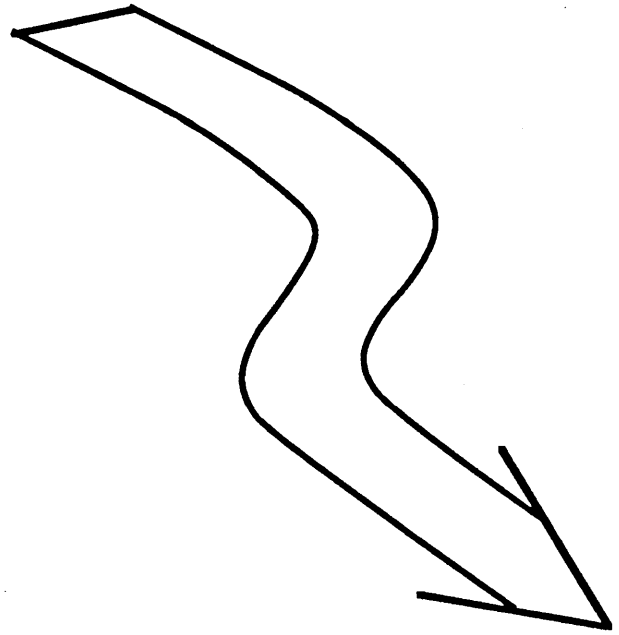


CHIPSet Summary

	PC AT Compatibles	PS/2 Compatibles
High-End	AT/386 CHIPSet 16/20 MHz	CHIPS/280 16/20 MHz
Mid-Range	NEAT/286 CHIPSet 12/16/20 MHz	CHIPS/250 12/16/20 MHz
Low-End	82C100 SXT 8/10 MHz XT	82C100 SXT 8/10 MHz Mod 30
Graphics	CS8241 EGA 82C245 VGA	CHIPS/451 VGA PLUS CHIPS/452 SUPER VGA

CHIPS' Strategy for PS/2

- Provide complete CHIPSet solutions
  - Compatibility



PLUS

- Performance
- Integration
- Functionality

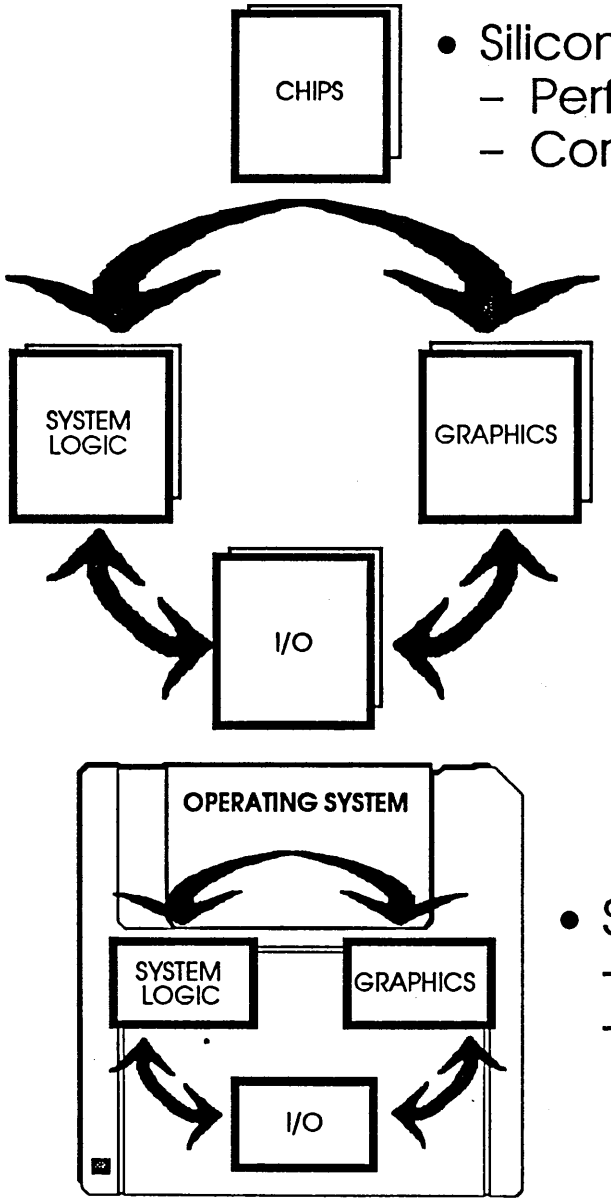
CHIPS' Compatibility

- Logic extraction, gate-level
- Implement "undocumented" functions
- Full compliance with Micro Channel timing specs
- Complete system analysis
- Operating system testing with
  - OS/2
  - DOS
  - XENIX

CHIPS' "Plus" Strategy

Integration, Integration, Integration

CHIPS' "Plus" Strategy



- Silicon **integration**
  - Performance
  - Compatibility

- Functional **integration**
  - Tightly coupled functions

- System **integration**
  - Operating system specific
  - Compatibility

Introducing
CHIPS' PS/2 Family

Function	Models 50/60	Model 80
System Logic	CS8225	CS8238
Graphics	82C451/2	82C451/2
COMM/FD I/O	82C607	82C607
Micro Channel Adapter Interface	82C6XX	82C6XX
	CHIPS/250	**CHIPS/280**

CHIPS/250

for IBM PS/2 Model 50/60

Compatible Systems

The Challenge of Designing a PS/2 Compatible

Goal

Compete effectively vs IBM's PS/2 family

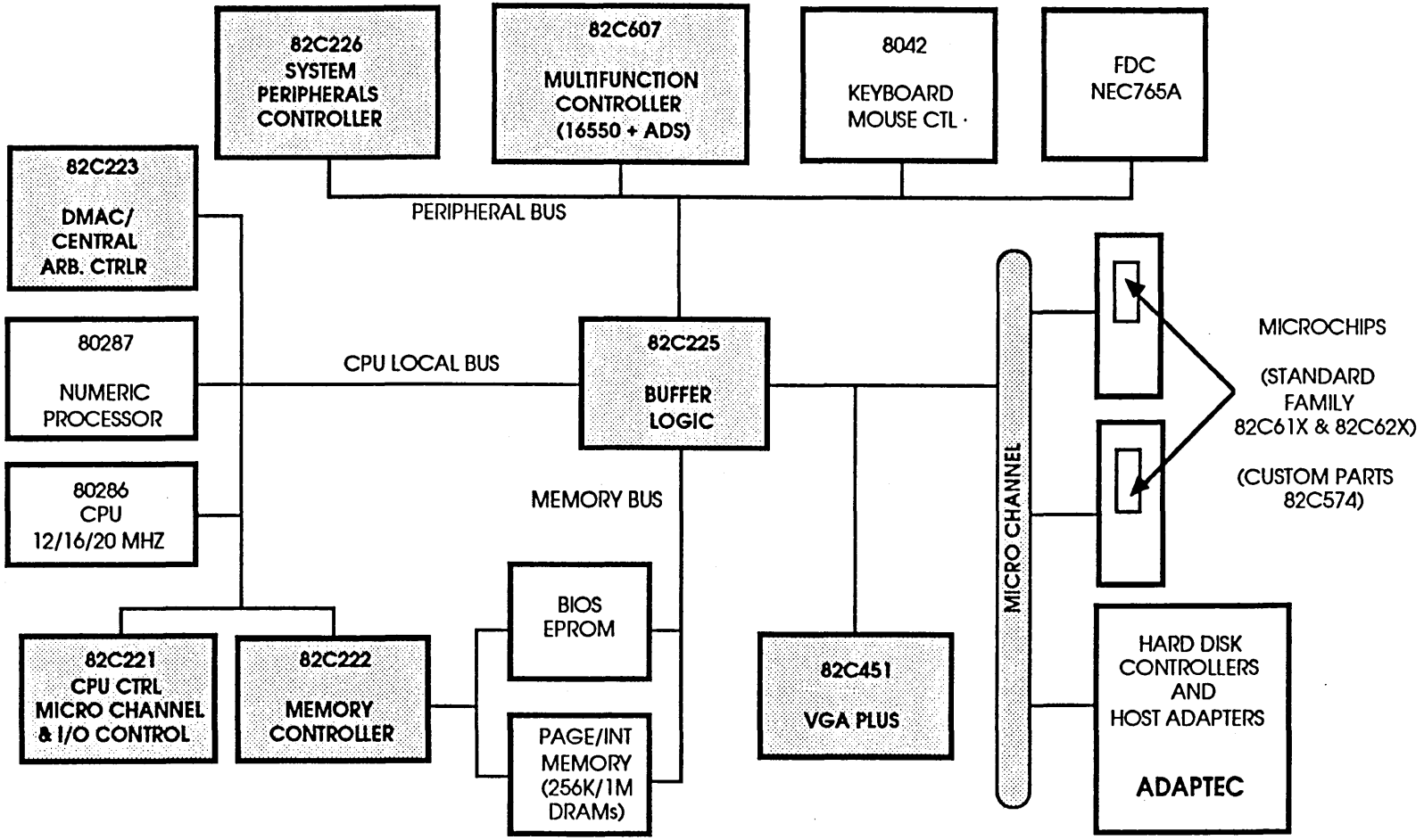
How?

- Uncompromising hardware/software *compatibility, plus*
- Exceed IBM's *integration* level in all areas
  - Systems logic, graphics, mass storage
- Clearly *superior performance* to IBM's PS/2
- *Graphic superiority*
- *Lower system cost*
- *Product differentiation*

Meeting the Challenge: Uncompromising Compatibility

- **Complete logic extraction** of all VLSI devices, PALs, system boards and IBM Micro Channel adapters
- OS/2 optimization similar to IBM PS/2
  - Fast CPU reset and Fast Gate A20
- CHIPS/2XX system will **boot up** in IBM compatible mode
  - Chips enhancements invisible
- Compatible with all IBM **hidden registers and functional modes** of IBM VLSI devices
- CHIPS compatibility will demonstrate operation with **IBM's BIOS, OS/2 Extended Edition and Presentation Manager, XENIX**

Meeting the Challenge: System Integration



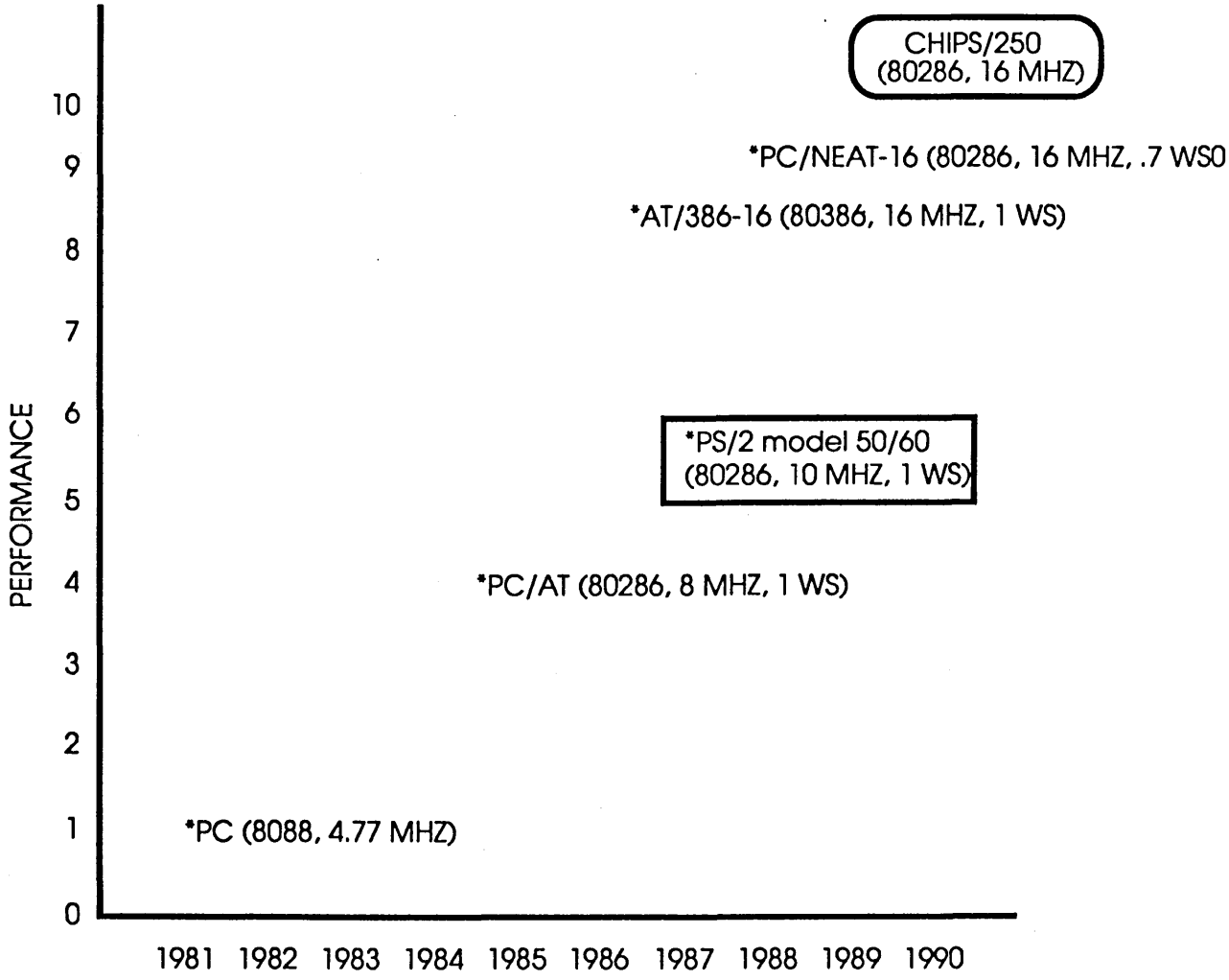
Meeting the Challenge: Performance Superiority

- CHIPS/250 targeted at **12, 16, and 20 MHz** vs 10 MHz IBM Models 50/60
  - Maximize CPU/memory performance
  - Run DMAC asynchronously at 10 MHz for all CPU clock speeds, while IBM's runs at 1X or 1/2X CPU clock speed

- CHIPS/250 is tightly coupled with VGA
  - ***Fast* VGA cycle** cuts I/O and memory cycles by 50%

- CHIPS/250 brings **matched memory** implementation to Models 50/60
  - 50% faster Micro Channel memory cycle

Meeting the Challenge: Performance Superiority



PS/2 systems solutions — CHIPS/250

Meeting the Challenge: Efficient Memory Design

- CHIPS/250 supports 2 memory architectures
  - Conventional and Paged Interleave

- CHIPS/250 conventional RAM architecture can implement 12 MHz 0 WS vs IBM's 10 MHz 1 WS Models 50/60

CPU Speed	Wait States	RAM Speed
10 MHz	0	100 NS
12 MHz	0	80 NS
12 MHz	1	120 NS

- CHIPS/250 Paged Interleave RAM architecture provides substantial cost savings with performance improvements

CPU Speed	Wait States	RAM Speed
10 MHz	0.7 - 0.5	200 NS
12 MHz	0.7 - 0.5	150NS
16 MHz	0.7 - 0.5	120NS

Meeting the Challenge: Efficient Memory Design

- 82C222 advanced memory controller achieves lower wait states with the slowest, most inexpensive DRAMs
  - Refined over **three generations** (AT/386, NEAT and CHIPS/250)
  - **Two-way/four-way paged interleave** memory
  - **Bad block remapping** for four 16 KB blocks
  - Paging with **one, two, three and four banks** for complete memory configuration flexibility
  - **Page hit space** ranging from 1 KB in a 512 KB system up to 8 KB in an 8 MB system – CACHE? 68030

- The full range of LIM EMS 4.0 implementations for DOS and windows applications
  - On-chip EMS support with four mapping registers
  - Up to four external **EMS mapper chips** for full implementation: eight sets of 64 mapping registers

Meeting the Challenge: Lower System Cost

- CHIPS/250 reduces component count

IBM Model 50	CHIPS/250 Compatible
119 plus DRAMs	68 plus DRAMs

- CHIPS/250 reduces DRAM memory speeds, lowering system memory cost (without a performance hit)

IBM Model 50	CHIPS/250 Compatible
120 ns @ 10 MHz	200 ns @ 10 MHz
N/A	150 ns @ 12 MHz
N/A	120 ns @ 16 MHz

- CHIPS/250 uses low-cost PLCC and PFP packaging, versus expensive ceramic PGAs from IBM

Meeting the Challenge: Differentiated Product

- **Matched memory** connector provides the OEM flexibility in memory design
- **External EMS mapper** control allows enhancement to support more sophisticated EMS implementations
- Four **user-programmable decodes** enable the OEM to add your own value added without using up expensive real estate
- Extensive list of **software configurable** features
- **Customizable CHIPS/250 macro cell** enables the OEM to implement his own value added

The Impact of CHIPS/250 on the 80286 Market

- CHIPS/250 will enable OEMs to offer clearly faster, less expensive, better Models 50/60

- CHIPS/250 extends IBM's PS/2 architecture in a compatible fashion:
  - Matched memory on Micro Channel
  - Fast VGA cycles
  - Asynchronous DMA
  - Paged interleave memory controller
  - Integrated EMS mapping
  - Enhanced VGA

- The strategy that let OEMs take over the PC-AT market is now available for Micro Channel technology

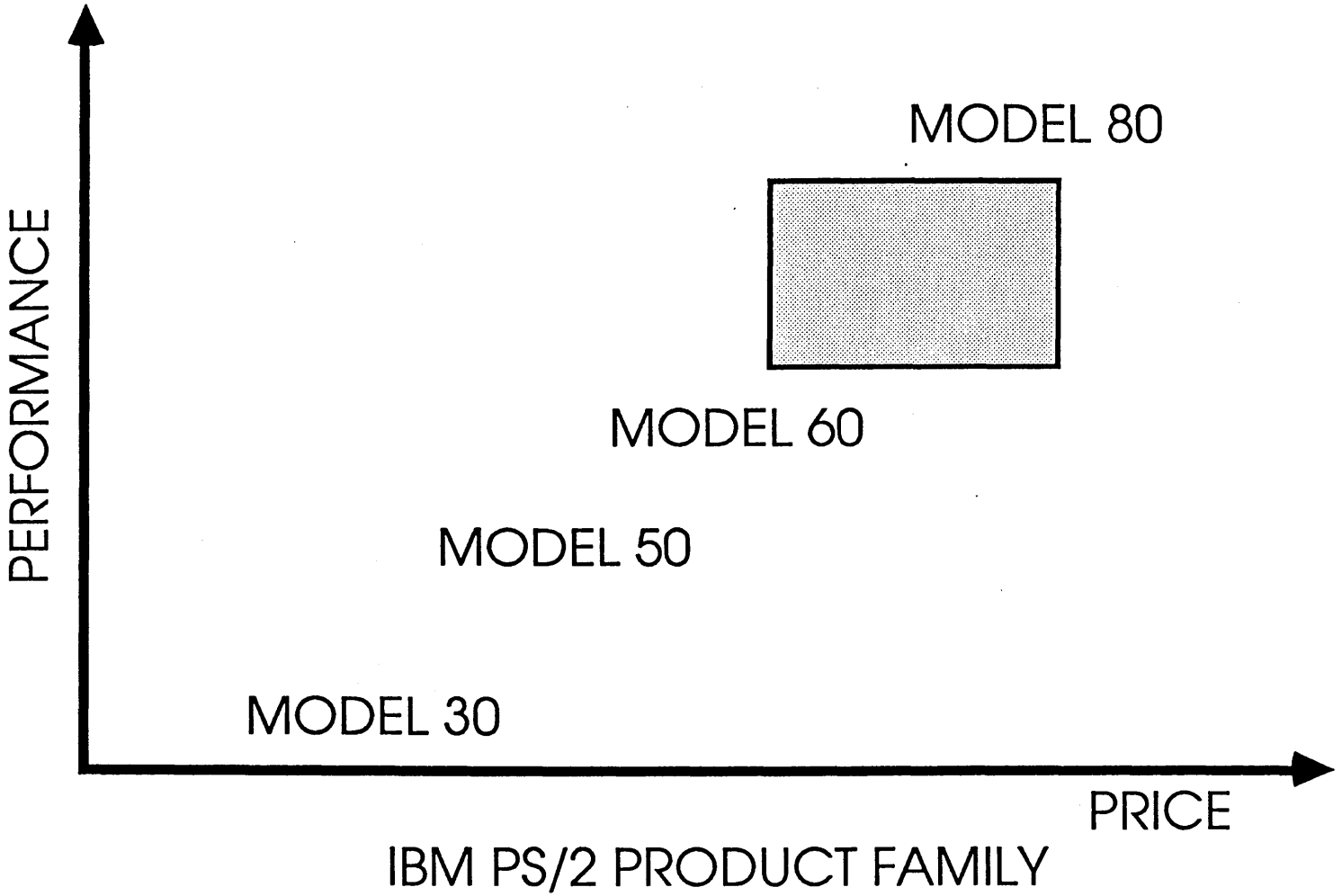
INTRODUCING:

CHIPS/280

The High-Performance IBM PS/2 Model 80 Compatible CHIPSet

- New generation of high-performance 32-bit computers
- Architected for compatibility, performance, enhanced functionality and cost-effectiveness

Meeting the Challenge:
CHIPS/280 Creates New Market Segment



PS/2 32-Bit Market Consists of Two Distinct Market Segments

Low-Cost Market	High-End Market
80386-16, 20	80386-20, 25
Page/Interleaved Memory System	Cache-Based Memory System
20-40 MB Hard Disk	40 MB Hard Disk and Above
Desktop Model	Floor Standing/Tower Model
CHIPS/280 for 16, 20 MHz	CHIPS/281 for 20, 25 MHz

The **two separate and distinct markets**
can best be served by
two separate and distinct CHIPSets and **two separate and distinct machines**

The Challenge of Designing a PS/2 Model 80 Compatible Machine

Goal

Compete effectively vs IBM's PS/2 Model 80

How?

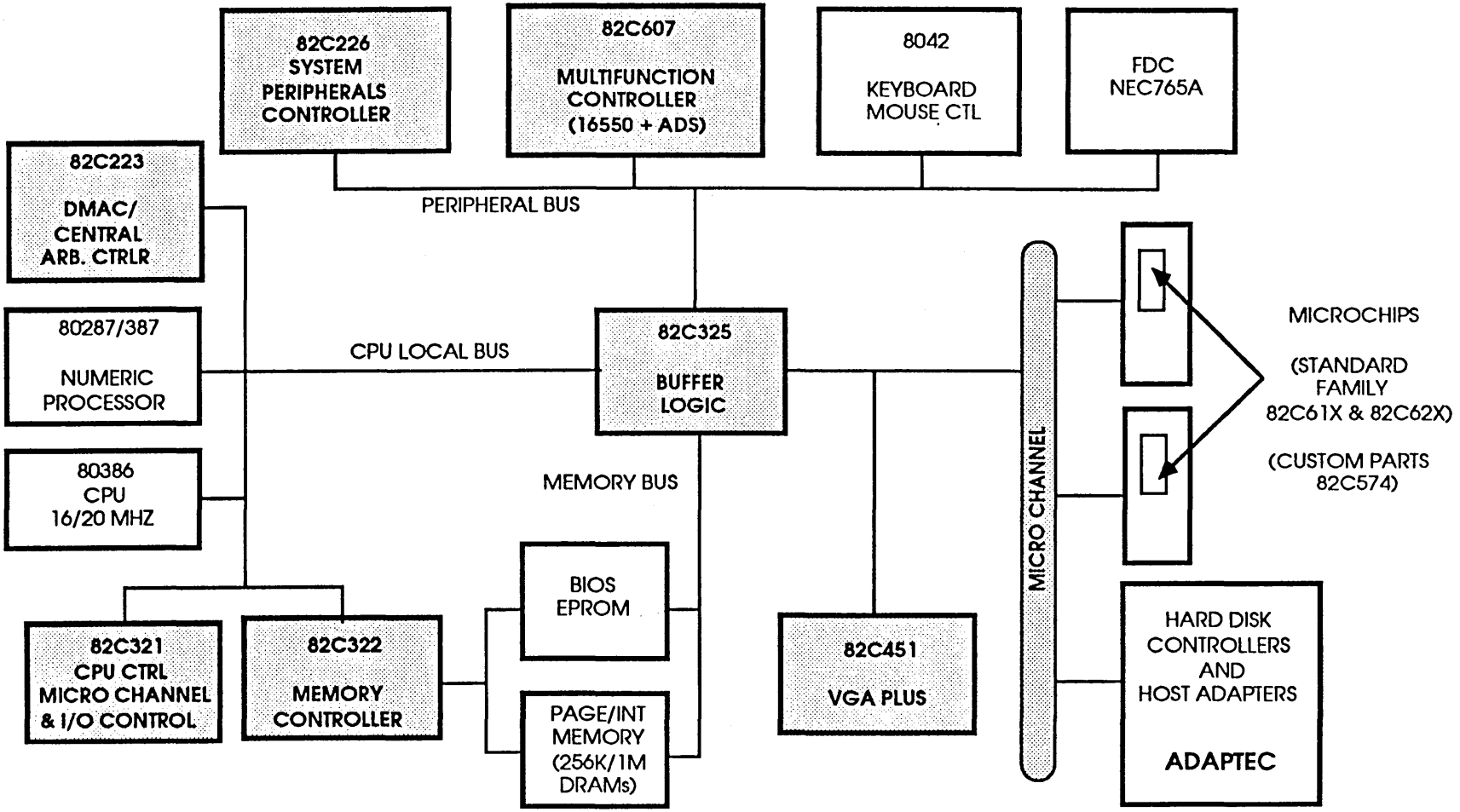
- Uncompromising hardware/software **COMPATIBILITY**
- Highest level of component and system **INTEGRATION**
- **LOWER** system cost
- Clearly **SUPERIOR PERFORMANCE** to IBM's PS/2
- **GRAPHICS SUPERIORITY**

Create a new market segment by serving a wide gap in IBM's PS/2 product line

Meeting the Challenge: Uncompromising Compatibility

- **Complete logic extraction** of all VLSI devices, PALs, system boards and IBM Micro Channel adapters
- CHIPS will demonstrate operation with **IBM's BIOS, OS/2 Extended Edition and Presentation Manager, XENIX**
- CHIPS/2XX system will **boot up** in IBM compatible mode
  - CHIPS enhancements invisible
- Compatible with all IBM **hidden registers and functional modes** of IBM VLSI devices
- CHIPS/280 includes **undocumented** IBM PS/2 Model 80 **address recovery logic**
- **OS/2 optimization** similar to IBM PS/2
  - Fast CPU reset and Fast Gate A20

The Compatible Model 80 With CHIPS/280



Meeting the Challenge: Highest-Level of Integration

- CHIPS/280 has the **highest** level of integration
  - IBM Model 50: 119 ICs plus DRAMs
  - IBM Model 80: 179 ICs plus DRAMs
  - CHIPS/280 compatible: **66 ICs** plus DRAMs

- **Super integration**
  - **1/3** the components of an IBM Model 80
  - Approximately **1/2** the components of an IBM Model 50

- CHIPS/280 enables OEMs to build PS/2 Model 80 compatible **desktop machines**
  - **Fits** into a Model 50 chassis

Meeting the Challenge: Lower System Cost

- Drastically reduces component count and real estate requirements
- Reduces DRAM speeds while increasing performance

IBM Model 80	CHIPS/280 Compatible
80 ns @ 16 MHz	100 ns @ 16 MHz
1 Wait State	0.5 - 0.7 Wait States

- Low cost PLCC and PFP packaging, versus expensive ceramic PGAs from IBM

CHIPS' *FAST* Micro Channel Matched Memory Cycle

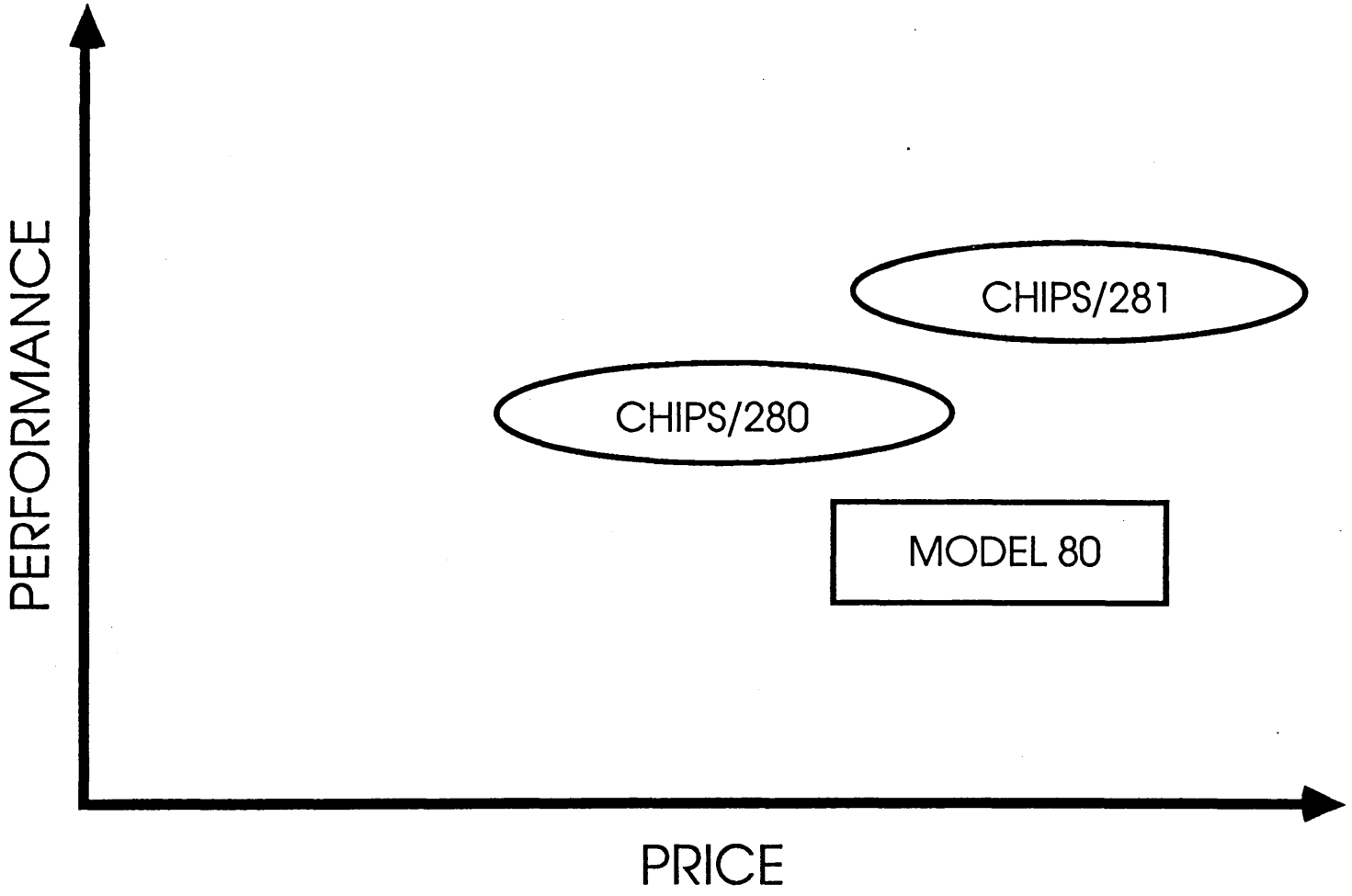
	IBM Model 80	CHIPS/280
At 20 MHz		
Regular MC Memory Cycle	200 ns (2 WS)	200 ns (2 WS)
MC Matched Memory Cycle	200 ns (2 WS)	200 ns (2 WS)
CHIPS Fast MC Matched Memory Cycle	**None**	**150 ns (1 WS)**
At 25 MHz		
Regular MC Memory Cycle	N/A	200 ns (3 WS)
MC Matched Memory Cycle	N/A	200 ns (3 WS)
CHIPS Fast MC Matched Memory Cycle	**N/A**	**160 ns (2 WS)** -CACHE

Meeting the Challenge: Performance Superiority

Architectural improvements over IBM Model 80

- **Fast Micro Channel matched memory cycle**
  - Up to 33% faster access to memory on the Micro Channel
- **CHIPS/280 is tightly coupled with VGA**
  - Fast VGA cycle cuts I/O and memory cycles by 50%
- **Enhanced memory controller**
  - Improvements of 8 - 10% in performance
- 16 MHz systems
  - IBM DMA runs at **8 MHz**
  - CHIPS/280 DMA runs at **10 MHz**

Meeting the Challenge: Performance Superiority



Impact of CHIPS/280 On The 80386 PC Market

- CHIPS/280
  - Uncompromising compatibility
  - Highest level of integration
  - Lower system cost
  - Superior performance
- Enable OEMs to offer clearly faster, less expensive, more functional Model 80 compatibles
- Creates new market segment by filling gap in IBM's PS/2 product line

CHIPS/450 Graphics Product Line

82C451 VGA Controller

82C452 Super VGA Controller

A new generation of power VGA graphics

tailored to PS/2 and Presentation Manager environments

PS/2 Graphics Enhancements

Increased color and resolution

- 640 x 480 x 16 colors
- 320 x 200 x 256 colors

- Implications
  - Incremental changes to EGA

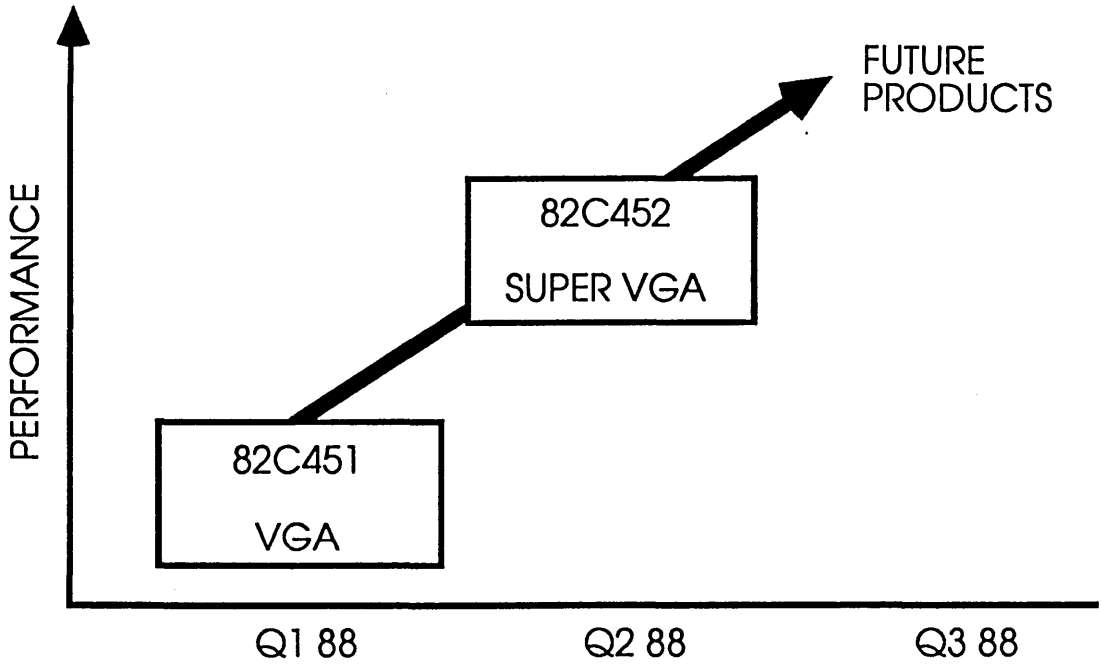
The most significant enhancement:
A standard graphics user interface — the OS/2 Presentation Manager

- Implications
  - A new generation of software
  - Graphics performance and throughput are now a significant performance challenge

The Challenge and Opportunity in VGA Graphics for the PS/2

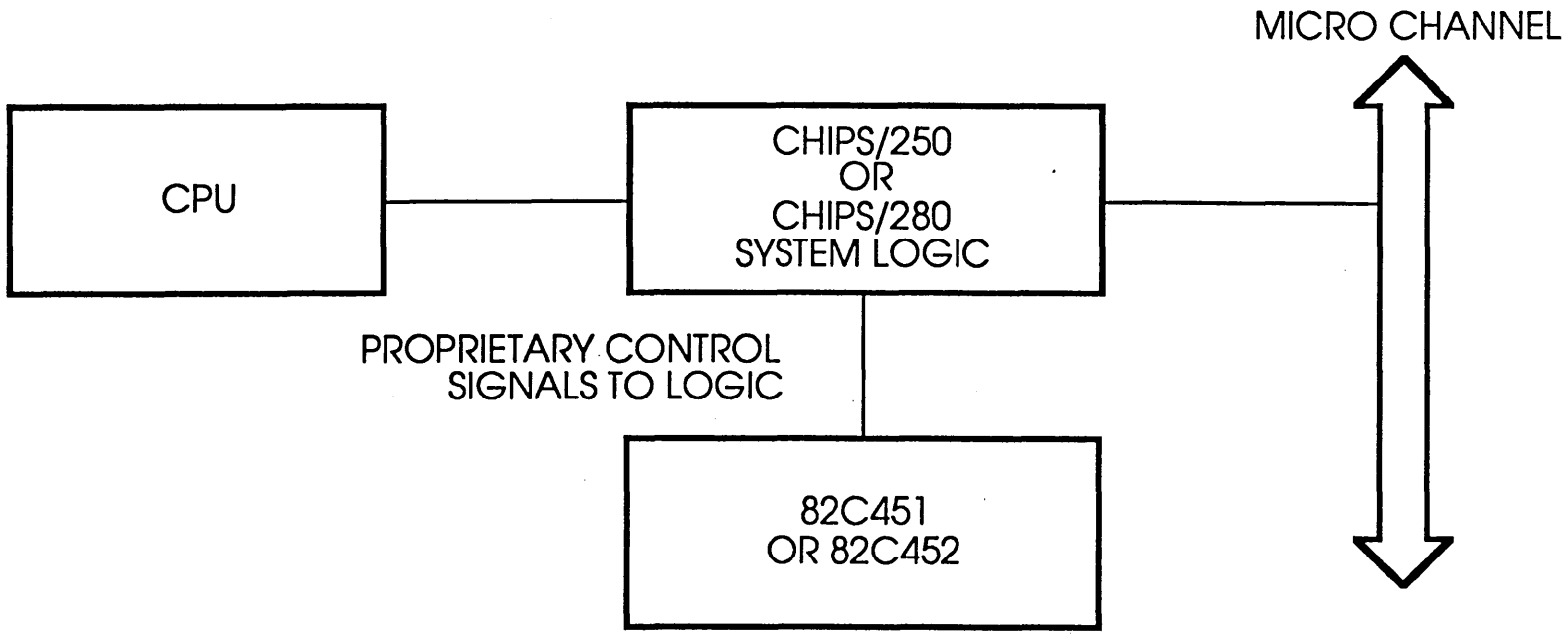
- Provide performance improvements over IBM VGA for standard business users
- Be prepared for Presentation Manager availability

Meeting the Challenge:
The CHIPS/450 Graphics Product Family



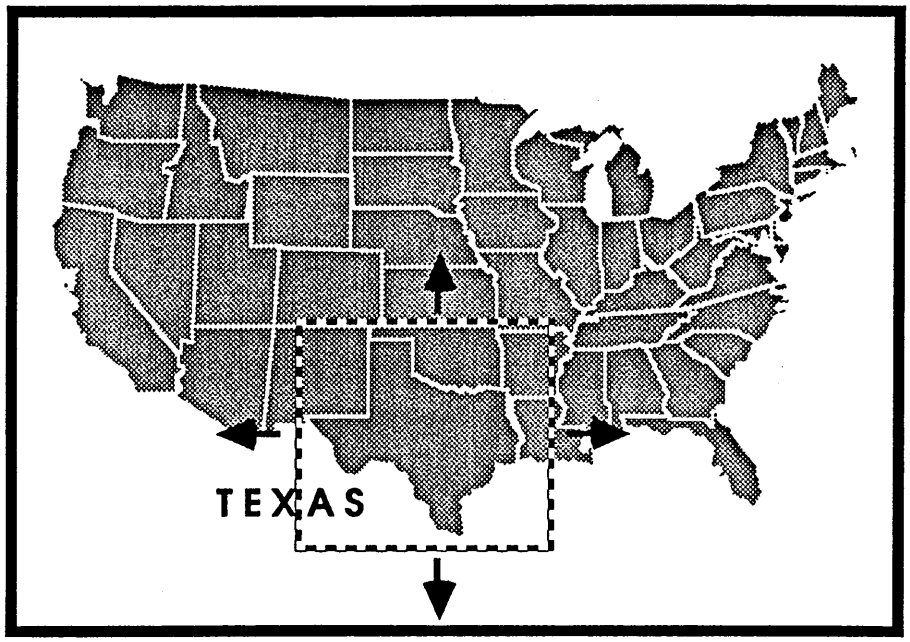
- Pin-compatible upgrade path to high-performance graphics for OS/2 Presentation Manager
- Maximizes windowing performance in both standard and high-resolution modes

System-Engineered for Optimum Performance

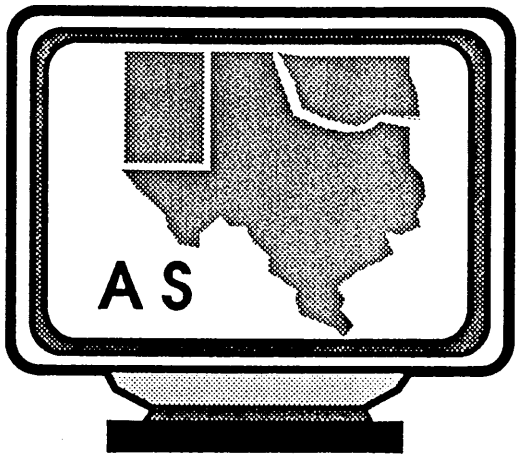


- High-performance proprietary interface to CHIPS/250 and CHIPS/280 system logic . . . CHIPS fast VGA cycle
  - Up to 50% performance improvement
- 16-bit CPU interface
  - Up to 100% performance improvement

100% VGA Compatibility



VIDEO BIT MAP

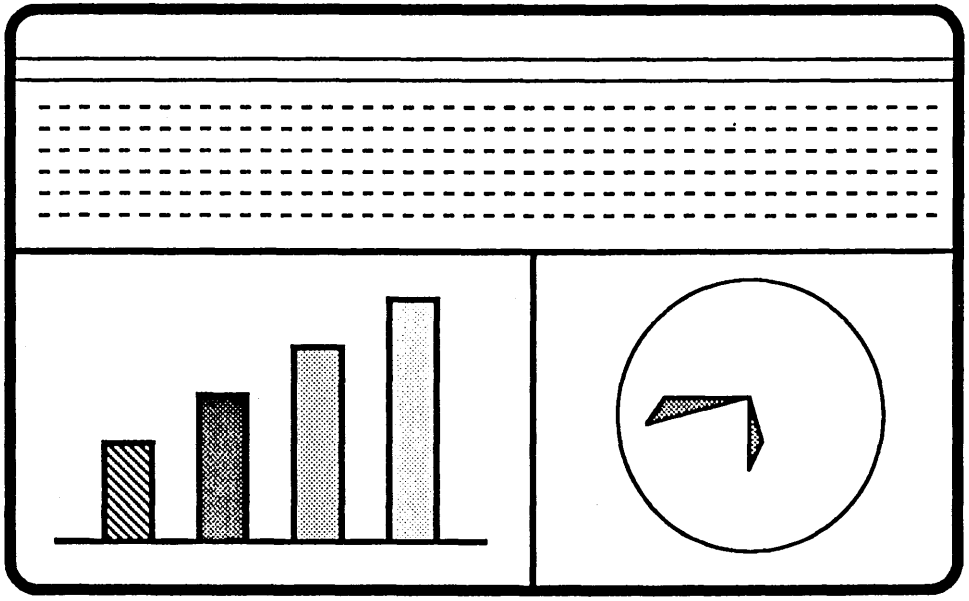


- Undocumented features in IBM's VGA provide added options going beyond today's VGA features
  - Up to 1K x 1K resolution
  - Panning in a 1K x 1K video bit map in both standard and high-resolution modes

82C451 VGA Controller

- All standard VGA modes with CHIPS enhanced functions
  - High-performance proprietary I/F
  - 16-bit interface
- Enhanced hardware backward compatibility to EGA, CGA, Hercules, MDA
- 1024 x 768 monochrome

82C452 Super VGA: The Graphics Advantage for the Next Generation of OS/2 Software



Added features enhancing Presentation Manager performance:

- Graphics cursor with transparency
  - Cursor movement consumes 30% of software overhead in windowing environments
  - Reduces software overhead for cursor movement by over 95%
- New write mode for fast graphics text (patent pending)

82C452 Super VGA

- Intelligent arbitration to improve CPU bandwidth
- Page mode memory operation to maximize memory bandwidth
- A superset of VGA graphics modes
  - 640 x 480 x 256 colors
  - 960 x 720 x 16 colors
  - 1280 x 960 monochrome
  - Supports up to 1 MByte of display memory

82C452 Performance Improvement Over IBM VGA

- High-performance proprietary interface
  - Up to 50%
- 16-bit data path
  - Up to 100%
- Intelligent CPU arbitration
  - Up to 100%
- Page-mode memory cycles
  - Up to 100%

Key Advantages to OEMs

- Highest performance in CHIPS/250, CHIPS/280 systems
- Pin-compatible upgrade path
  - Fast time to market with performance enhancements
  - Leverage development investment in design time and software
- Configurable bus architecture: PC/PC-AT and PS/2
  - Single chip supports both environments

Key Advantages to OEMs

- True 100% compatibility
  - Added feature benefits
  - Eliminates risk of future incompatibility with currently undocumented modes

- Presentation Manager functions
  - High-performance graphics for standard business applications
  - Allows OEMs to be well positioned for Presentation Manager

CHIPS' "Plus" Scoreboard

- Performance
  - 2X faster than IBM Model 50
  - 50% higher Micro Channel memory bandwidth
  - 50% faster VGA memory & I/O cycles
- Integration
  - 66 versus 179 for the Model 80
  - 68 versus 119 for the Model 50
- Functionality
  - Asynchronous CPU/memory/DMA
  - Four-way interleaved memory
  - VGA with graphics cursor
  - Integrated EMS 4.0

Meeting Accelerated Product Cycles

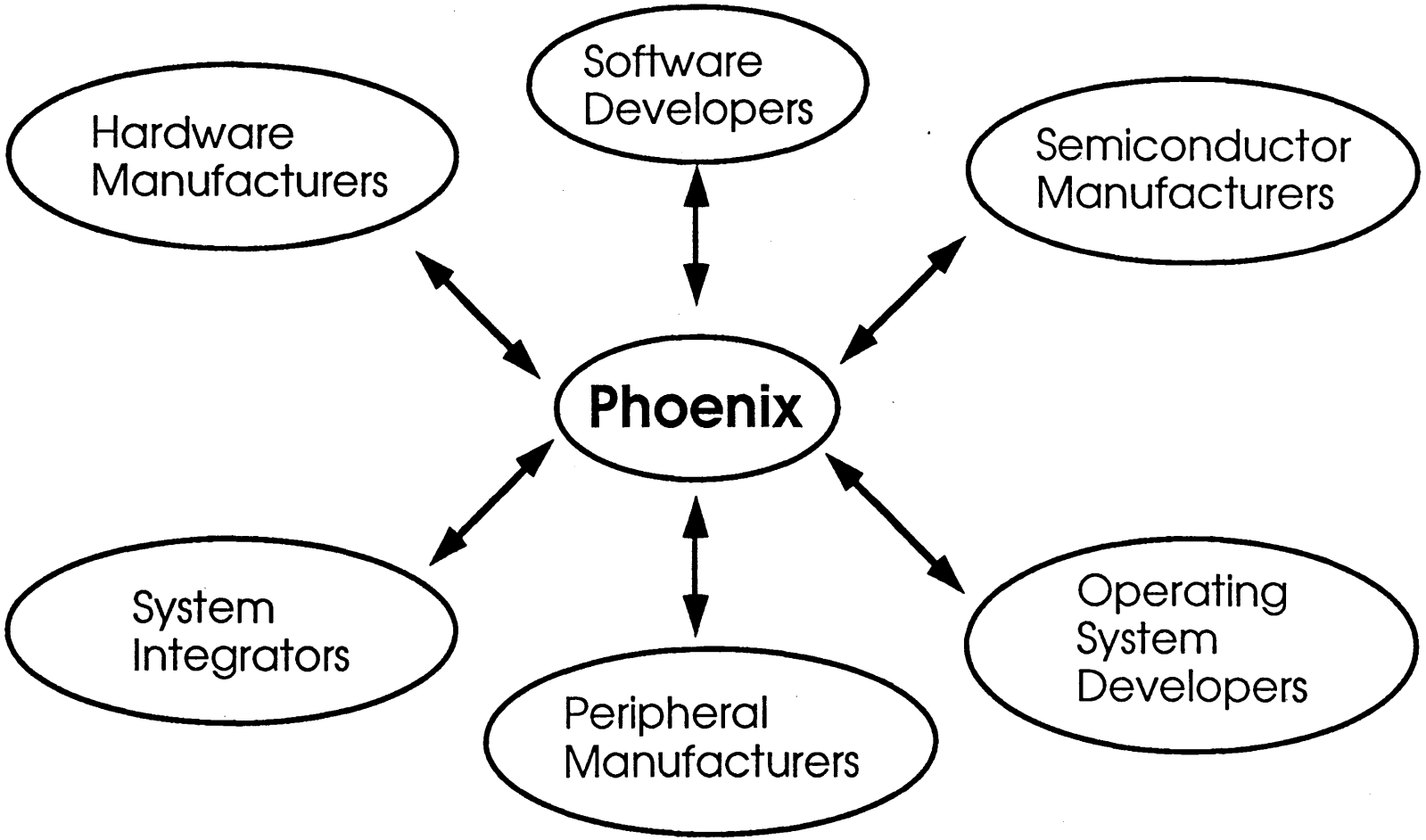
- Evaluation kits
  - Development board
  - System schematics
  - Phoenix BIOS
- Turnkey system design services
  - Standard manufacturing packages
  - Customer-specific designs

CHIPS/2 Product Family

	Model 50/60	Model 80
CHIPSets	CHIPS/250 CHIPS/451 2/88	CHIPS/280 CHIPS/452 4/88
Development Kits	DK250 DK451 3/88	DK280 DK452 5/88
Design Services	BD250 BD451 SYS250 4/88	BD280 BD452 SYS280 6/88

Phoenix Technologies

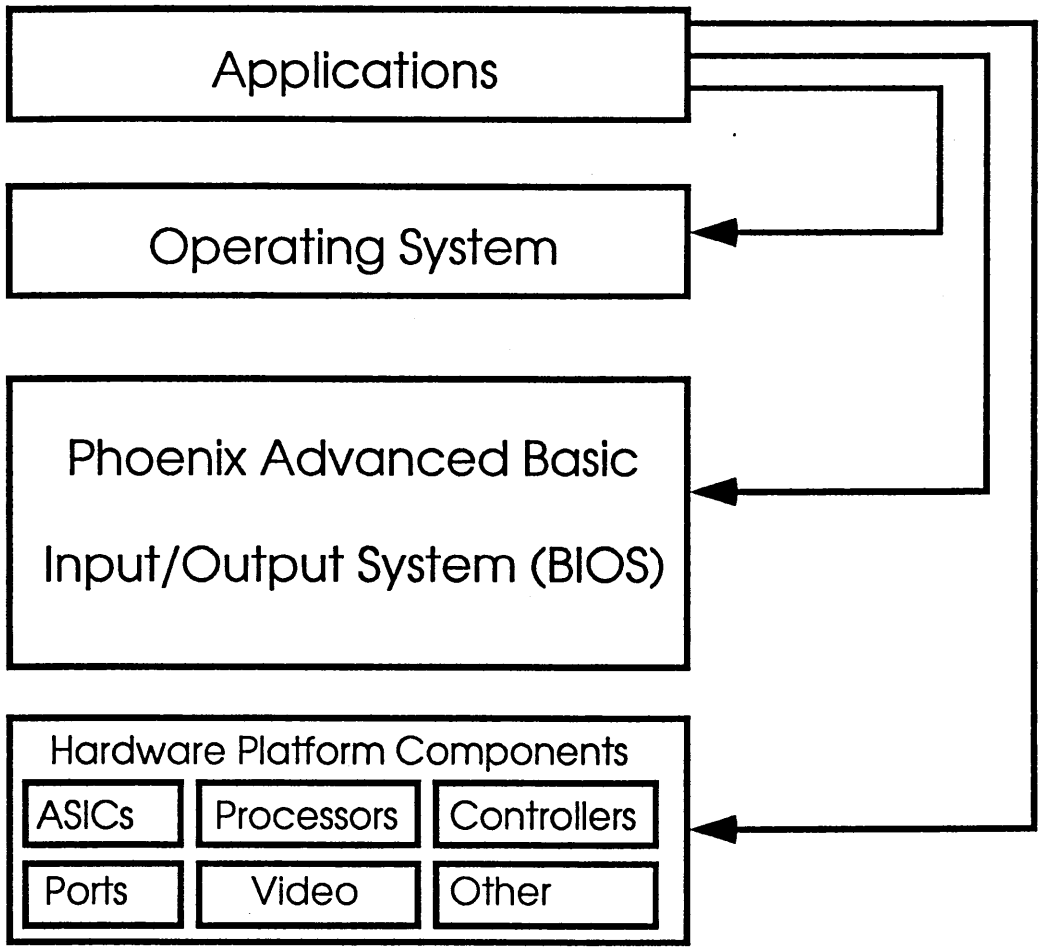
Phoenix Position In The Industry



The Compatibility Challenge

- Market requires compatibility
- Market demands value-added features

The Compatibility Issues



PS/2 Compatible Software

- Must run ALL old applications
- Must run ALL new applications
- Must facilitate DOS 3.x and OS/2
- Must facilitate hardware advances in design and configurations

Phoenix BIOS Support For CHIPS/2 Customers

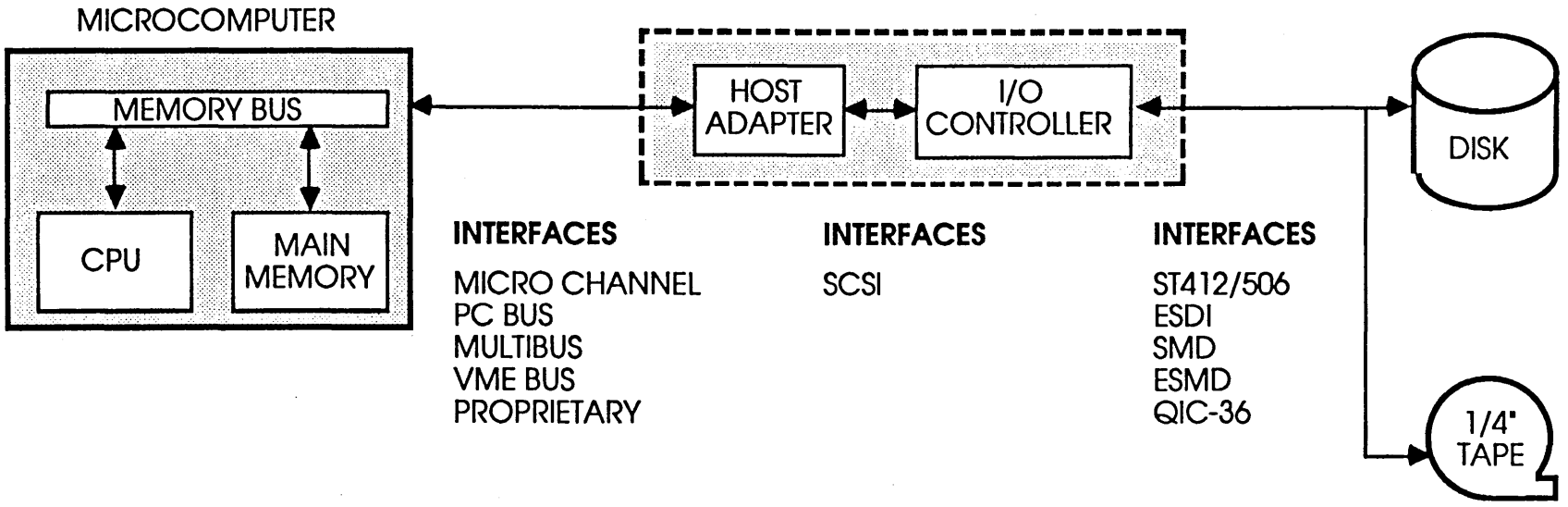
- Phoenix BIOS supports CHIPS/2 system configuration options
  - Memory architecture
  - Graphics options
- Phoenix BIOS supports Micro Channel architecture in CHIPS/2 extended modes
  - BIOS selectable use of fast VGA cycle
  - BIOS selectable DMA cycle period

Phoenix BIOS Products, Implementation Services and Design Centers Ensure

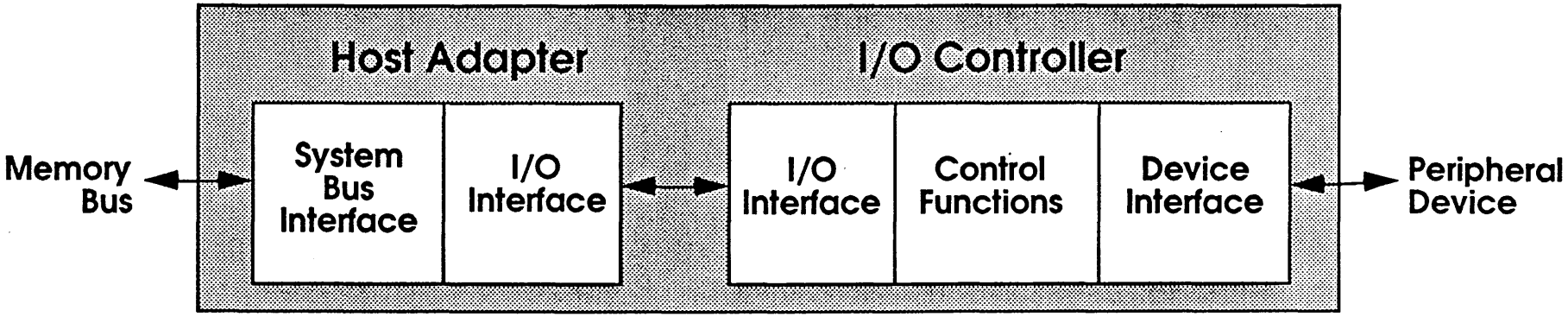
- Utilization of unique hardware advances
- Attainment of OEM product goals
- Full application and operating system testing
- Users are satisfied

adaptec, inc.

Adaptec Business



Adaptec Software



SOFTWARE

- Caching
- SCSI
- Direct Memory Access
- Multitasking

SOFTWARE

- SCSI
- Memory Bus Interface
- Data Buffer
- Data Sequencing
- Non-Interleave
- Multitasking
- Record Locking (Multiuser)
- Concurrent I/O
- Disk Interface
- Defect Management
- Tape Interface

Adaptec Business Strategy

- **Strategy**
  - Sell mainframe I/O solutions to the high-performance segment of high-volume microcomputer markets

- **Technological Innovation**
  - 1979 Adaptec founders create SCSI
  - 1984 First multitasking disk controller and host adapter
  - 1986 First Run-Length Limited controller for PCs
  - 1986 First SCSI development system
  - 1987 First multitasking IBM PC AT to SCSI host adapter
  - 1987 First 1:1 interleaved 286/386 controllers

How IBM Changed the Rules

for Personal Computer I/O

IBM Offers Mainframe Performance on PS/2

- Multitasking
- Micro Channel
- Faster bus transfer rates
- 1:1 interleaving
- High-performance drives: ESDI

System Manufacturers Face Complex Compatibility Issues

- Proprietary hardware and software
- Undocumented system architecture
  - Schematics
  - BIOS

Competitive Challenges

- Compatibility
- Product differentiation
  - Higher performance alternatives
  - Configuration options
  - Peripheral connectivity

Adaptec Strategy for PS/2

COMPATIBILITY

"PLUS"

Adaptec Delivers Compatibility

- Total compliance with IBM's PS/2 Micro Channel architecture
- Port and BIOS compatibility with IBM PS/2 Models 50/60/80
- Based on Adaptec's chips used in IBM PS/2 controller
- Designed and tested to work with IBM's and CHIPS' PS/2 Micro Channel core logic
- And with all PS/2 operating systems
  - MS-DOS
  - OS/2
  - XENIX
  - UNIX

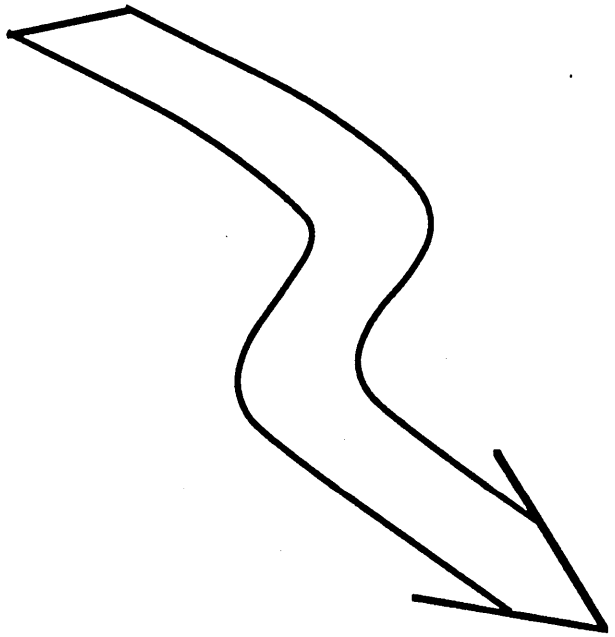
Adaptec Supplies the "Plus"

Product differentiation based on:

- Performance options
  - Data rates up to three times faster
  - Faster access drives
  - Multitasking alternatives
- Capacity alternatives
  - Drive sizes up to 768 MB
  - Support for MFM, RLL, ESDI and SCSI drives
- Peripheral connectivity via SCSI
  - As many as 56 devices

Without sacrificing compatibility with IBM offerings

COMPATIBILITY
"PLUS"



ADAPTEC'S PS/2
COMPATIBLE
FAMILY

Adaptec's PS/2-Compatible Family of Controller Boards and Host Adapters

IBM PS/2 Offerings	Adaptec's PS/2-Compatible Products	Availability
Models 25/30	• ACB-2072 ST412/506 RLL Hard Disk Controller • AHA-1020 PS/2 Models 25/30 to SCSI Host Adapter • Embedded Chip Set Solutions	In Production
Models 50/60	• ACB-2610 Micro Channel to ST412/506 MFM Hard Disk Controller • ACB-2670 Micro Channel to ST412/506 RLL Hard Disk Controller	**New Announcements**
Models 60/80	• ACB-26M20 Micro Channel to ESDI Multitasking Controller • AHA-1640 High-Performance Micro Channel to SCSI Host Adapter	

ACB-2610

Description: Micro Channel to ST412/506 MFM Hard Disk Controller

Function: To provide high-performance and configuration options to system manufacturers building PS/2 Models 50/60 compatibles

Availability: 1Q88

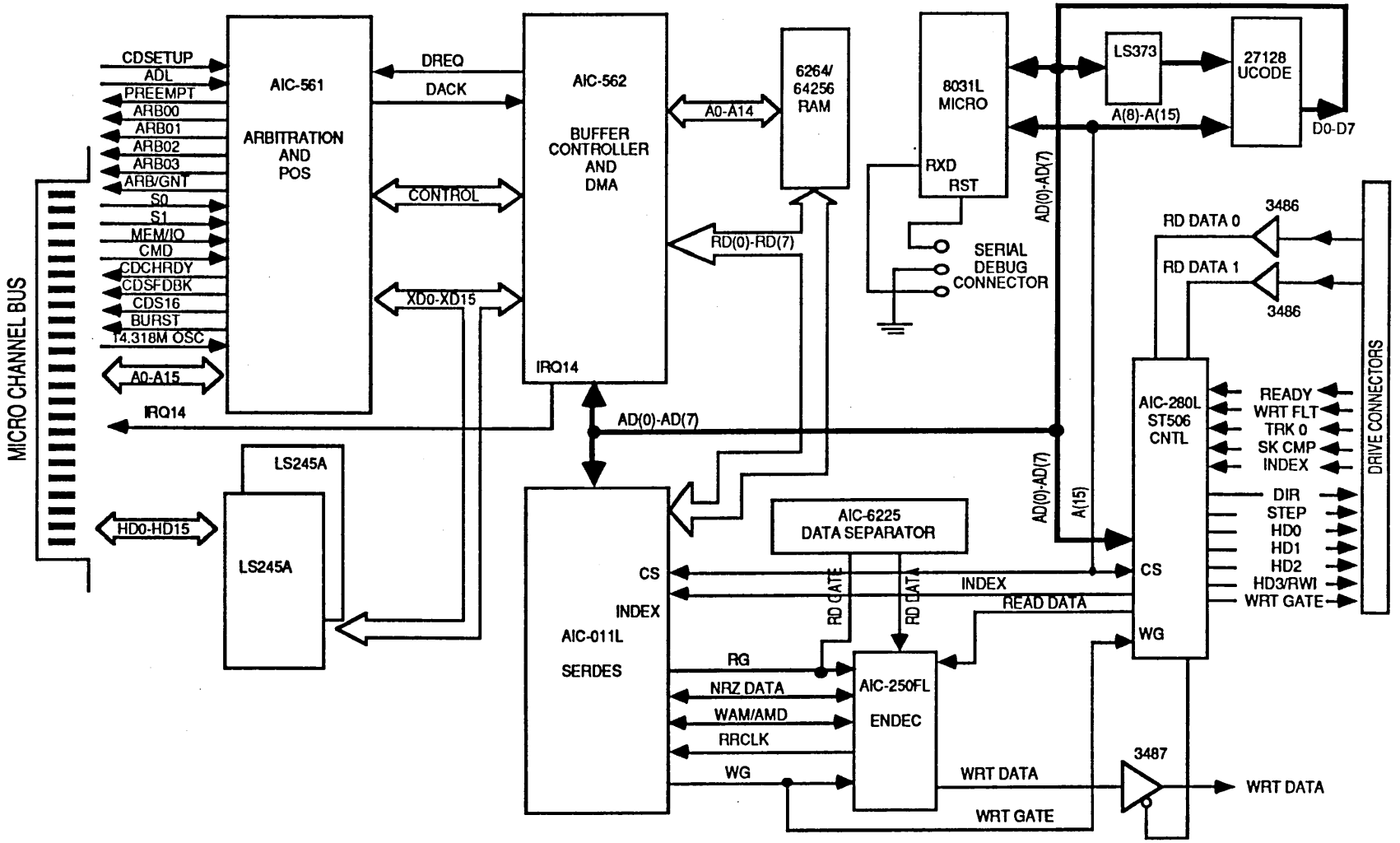
ACB-2610 Micro Channel to ST412/506 MFM Disk Controller

FEATURE	BENEFIT
• 100% IBM PS/2 port compatible	• Software compatible with IBM Models 50/60
• 1:1 interleave	• Highest performance available from an MFM I/O subsystem
• Supports 2 drives, 4096 cylinders, 16 heads	• Works with wide variety of drives • Offers several price/performance options
• Burst mode DMA up to 10 MB/sec	• Fastest DMA transfer capability • Easy upgrade path
• 48-bit ECC polynomial	• Increased data integrity and reliability
• Bipolar monolithic data separator AIC-6225	• Improved window margin yielding increased drive reliability

ACB-2610 Micro Channel to ST412/506 Disk Controller

FEATURE	BENEFIT
• Optional 8K, 32K, or 64K data buffer	• Configuration flexibility
• Read-ahead cache	• Reduced disk latency
• Surface mount technology	• Increased reliability • Smaller form factors
• Programmable option select	• Easy to configure in software
• Thoroughly tested with CHIPS and IBM systems	• High confidence in system compatibility • Shorter time to market
• On-board advanced diagnostics	• Simplifies debugging
• Limited lifetime warranty	• High confidence in product support over long term

ACB-2610 Micro Channel to ST412/506 MFM Disk Controller



ACB-2670

Description: Micro Channel to ST412/506 RLL Hard Disk Controller

Function: To greatly expand drive capacity and performance alternatives available to system manufacturers building Models 50/60 compatibles, while maintaining total compliance with IBM's Micro Channel architecture

Availability: 2Q88

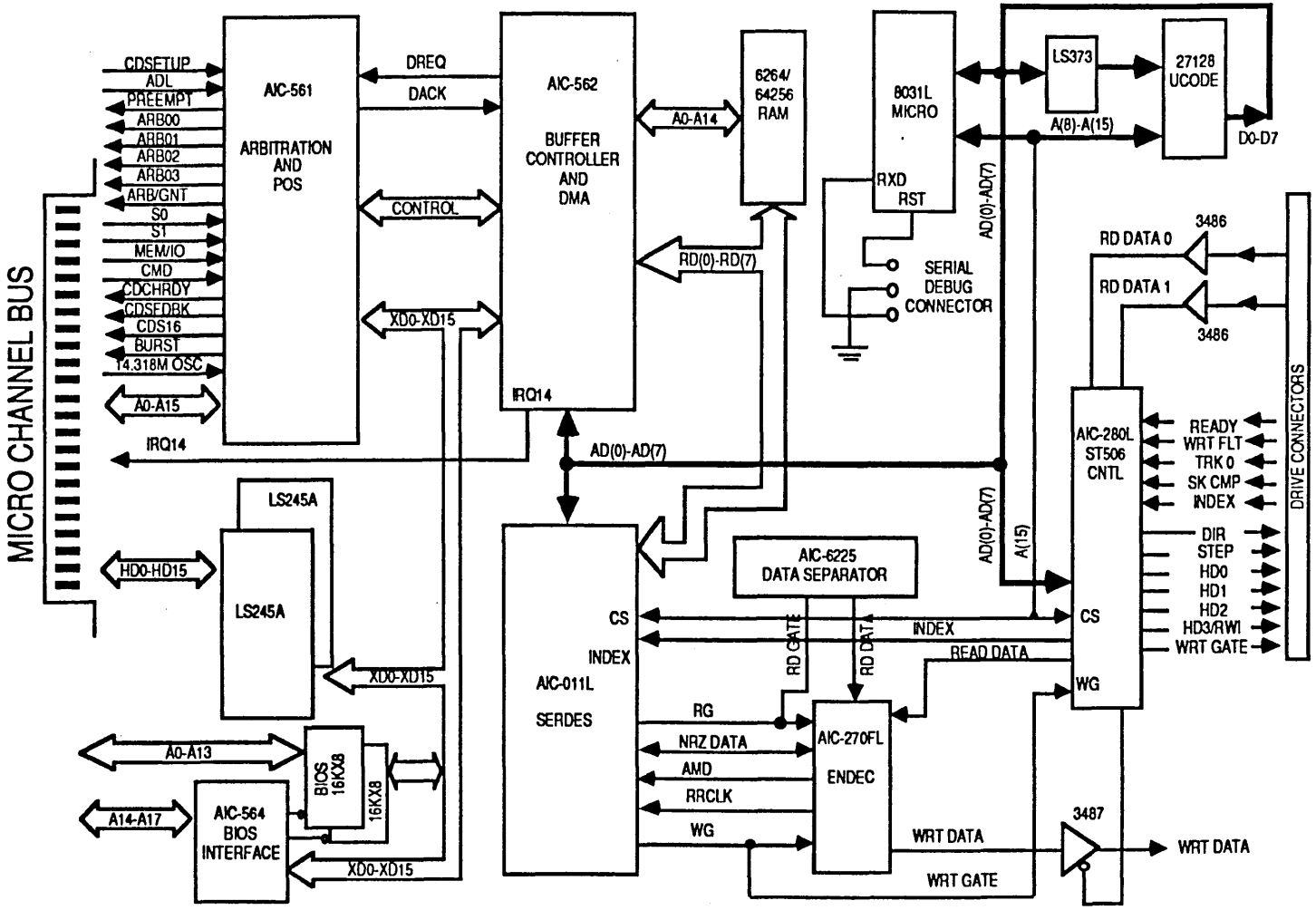
ACB-2670 Micro Channel to RLL Disk Controller

FEATURE	BENEFIT
• 100% IBM PS/2 Micro Channel port and BIOS compatible	• 100% software compatible with IBM PS/2 Models 50/60
• 1:1 interleave, 7.5 Mb/sec drive transfer rate	• 50% more capacity, 50% faster vs MFM • Lowest cost/MB solution
• Supports 2 drives, 4096 cylinders, 16 heads, 26 sectors/track RLL	• Works with wide variety of drives • Offers several price/performance options
• Slave burst DMA up to 10 MB/sec	• Fastest DMA transfer capability • Easy upgrade path
• Optional 8K, 32K, or 64K data buffer	• Configuration flexibility
• Read-ahead cache	• Reduced disk latency
• 48-bit ECC polynomial	• Increased data integrity and reliability

ACB-2670 Micro Channel to RLL Disk Controller

FEATURE	BENEFIT
• Bipolar monolithic data separator AIC-6225	• Improved window margin yielding increased drive reliability
• Surface mount technology	• Increased reliability • Smaller form factors
• Programmable option select	• Easy to configure in software
• Thoroughly tested with CHIPS and IBM systems	• High confidence in system capability • Shorter time to market
• Optional on-board compatible BIOS	• Supports 26 sectors per track • Autoconfiguration
• On-board advanced diagnostics	• Faster debugging
• Limited lifetime warranty	• High confidence in product support over long term

ACB-2670 Micro Channel to ST412/506 2,7 RLL Disk Controller



Configuration Comparison: IBM PS/2 Model 50

	IBM PS/2 Model 50	Adaptec ACB-2610	Adaptec ACB-2670
Encoding Scheme	MFM	MFM	RLL
Number of Drives	1	2	2
Total Capacity	20 MB	Up to 160 MB per drive	Up to 285 MB per drive
Access Time	80 ms	≥ 28 ms	≥ 28 ms
Bus Data Rate	3.3 MB/sec	10 MB/sec	10 MB/sec
Drive Data Rate	5.0 Mb/sec	5.0 Mb/sec	7.5 Mb/sec
Interleave	1:1	1:1	1:1

ACB-26M20

Description: Micro Channel to ESDI Multitasking Hard Disk Controller

Function: To offer the highest performance disk controller options available to system manufacturers, building Models 60/80 compatibles, while maintaining total compliance with IBM's Micro Channel architecture

Availability: 3Q88

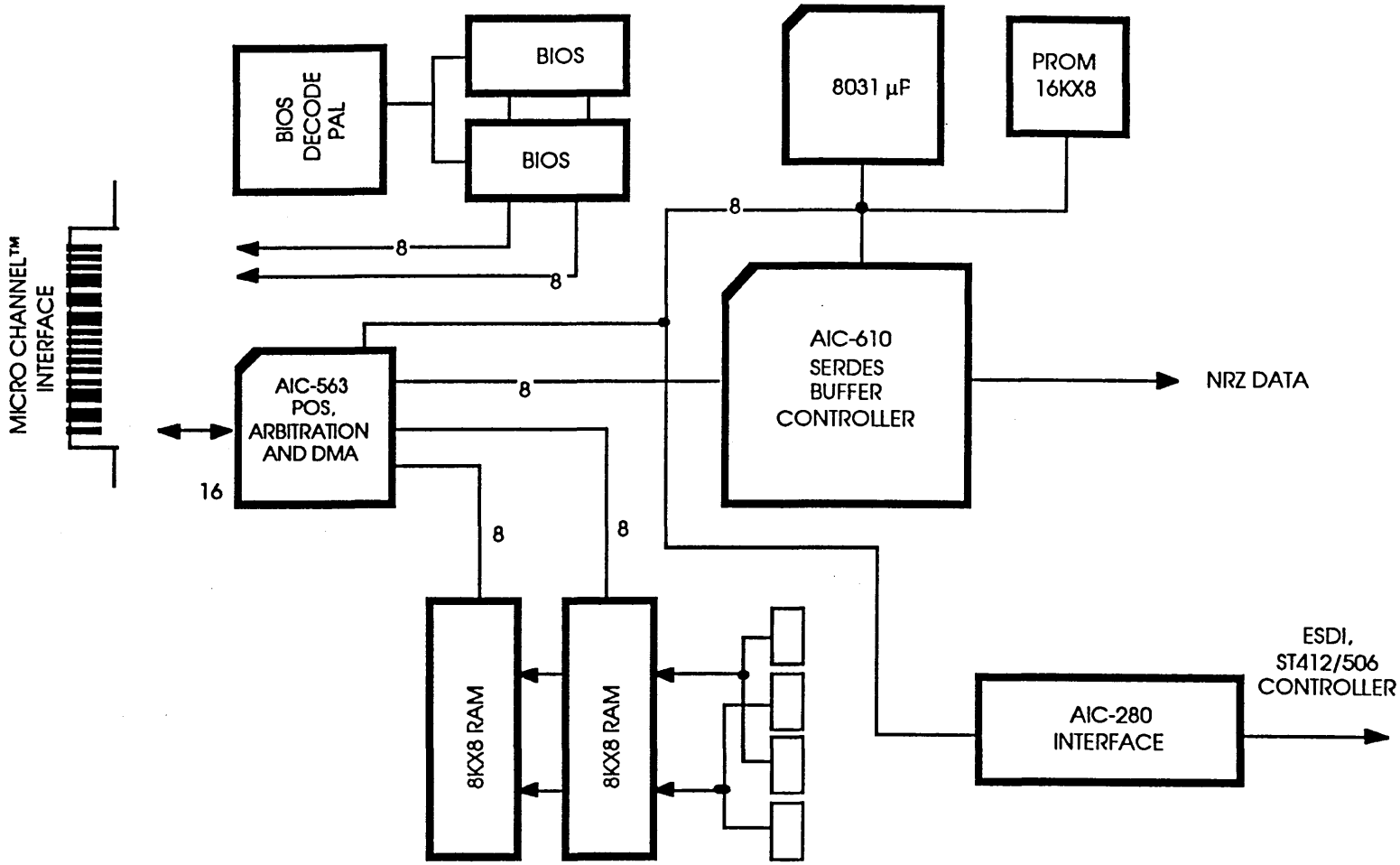
ACB-26M20 Micro Channel to ESDI Multitasking Disk Controller

FEATURE	BENEFIT
• 100% IBM PS/2 Micro Channel port and BIOS compatible	• 100% software compatible with IBM PS/2 Model 80
• Multitasking/multithreading	• Able to execute 3 simultaneous tasks
• 1:1 interleave, 15 Mb/sec drive transfer rate 52 SEC/TRACK	• Provides access to largest and highest-performance ESDI
• Supports 2 drives, 4096 cylinders, 16 heads, 52 sectors/track	• Works with wide variety of drives • Offers price/performance options
• Slave burst DMA up to 10 MB/sec	• Three times faster than IBM • 50% faster than competitive products
• Optional 16K, 32K, or 64K data buffer	• Configuration flexibility
• Read-ahead cache	• Reduced disk latency

ACB-26M20 Micro Channel to ESDI Multitasking Disk Controller

FEATURE	BENEFIT
• On-board 16-bit compatible BIOS	• Reduces execution overhead
• 48-bit ECC polynomial	• Increased data integrity and reliability
• On-board advanced diagnostics	• Faster debugging
• Programmable option select	• Easy to configure in software
• Surface mount technology	• Increased reliability • Smaller form factors
• Thoroughly tested with CHIPS and IBM systems	• High confidence in system compatibility • Shorter time to market
• Limited lifetime warranty	• High confidence in the product support over the long term

ACB-26M20 ESDI Disk Controller Block Diagram



Configuration Comparison: IBM PS/2 Model 80

Encoding Scheme	IBM PS/2 Model 80	Adaptec ACB-26M20
Interleave	1:1	1:1
Number of Drives	2	2
Total Capacity	70-314 MB per drive	Up to 780 MB per drive
Access Time	30 ms	10-25 ms
Bus Data Rate	3.3 MB/sec	10 MB/sec
Drive Data Rate	10 Mb/sec	15 Mb/sec

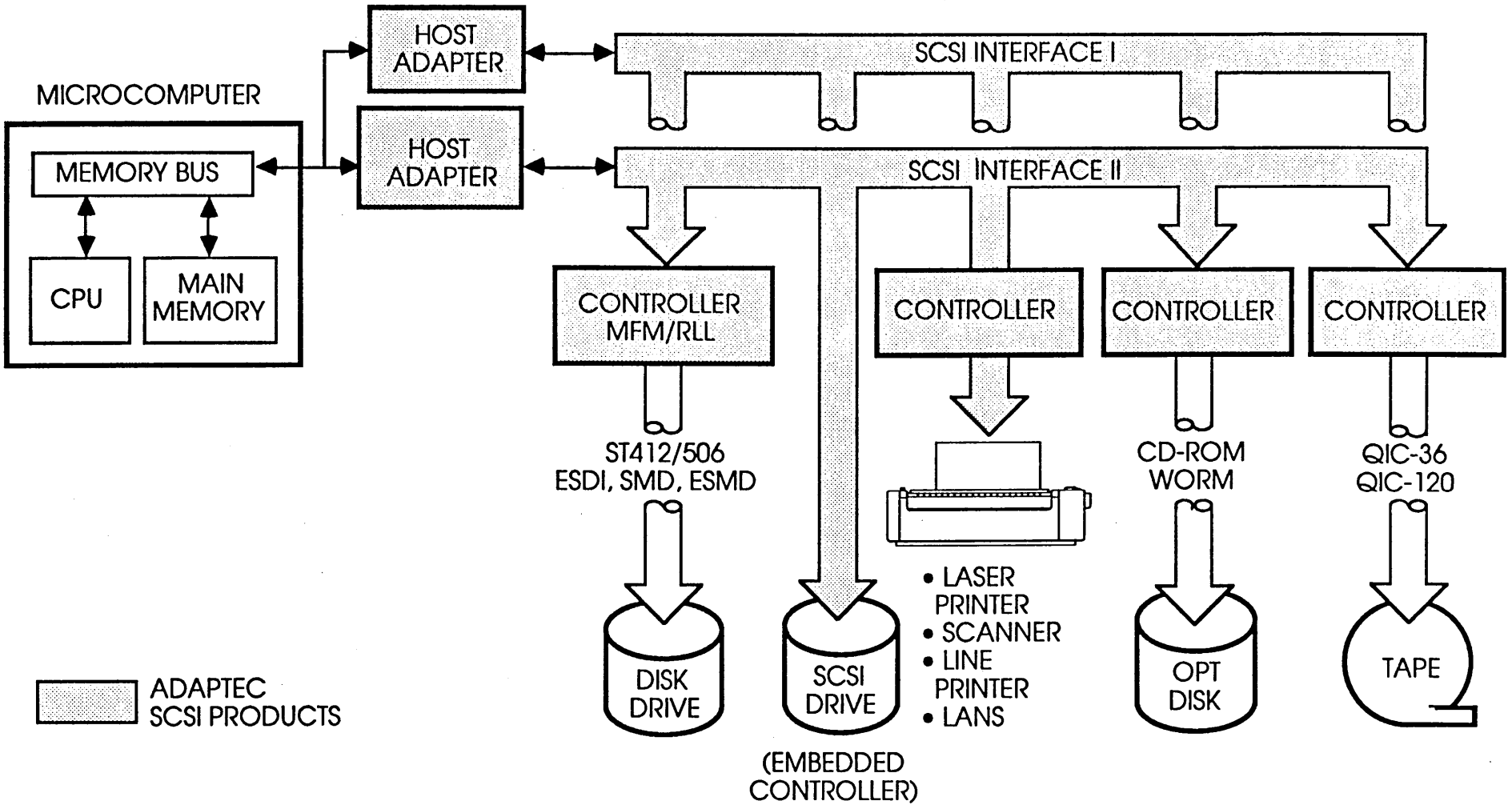
AHA-1640

Description: High-Performance Micro Channel to SCSI Host Adapter

Function: To provide SCSI multitasking performance plus multiple peripheral and host connectivity for PS/2 Models 60/80 compatibles

Availability: 3Q88

Adaptec SCSI Business



Customer Base

SCSI Development System

- Altos
- Apple
- Apollo
- Archive
- AT&T Bell Labs
- Bell Northern Rsrch
- Boeing
- CDC
- Cipher Data
- Compugraphics
- Conner Peripherals
- Convergent
- DEC
- Eastman Kodak
- Epson
- Fujitsu
- General Electric
- Hewlett-Packard
- Hitachi
- IBM
- Intel
- Intergraph
- Matsushita Electric
- Maxtor
- Micropolis
- Miniscribe
- Nat'l Bur. of Stds.
- NEC
- Nixdorf
- Priam
- Prime
- Quantum
- Rodime
- Rolm
- Seagate
- Sun Microsystems
- Tandem
- Tektronix
- Toshiba
- Unisys
- Wang
- Wangtek

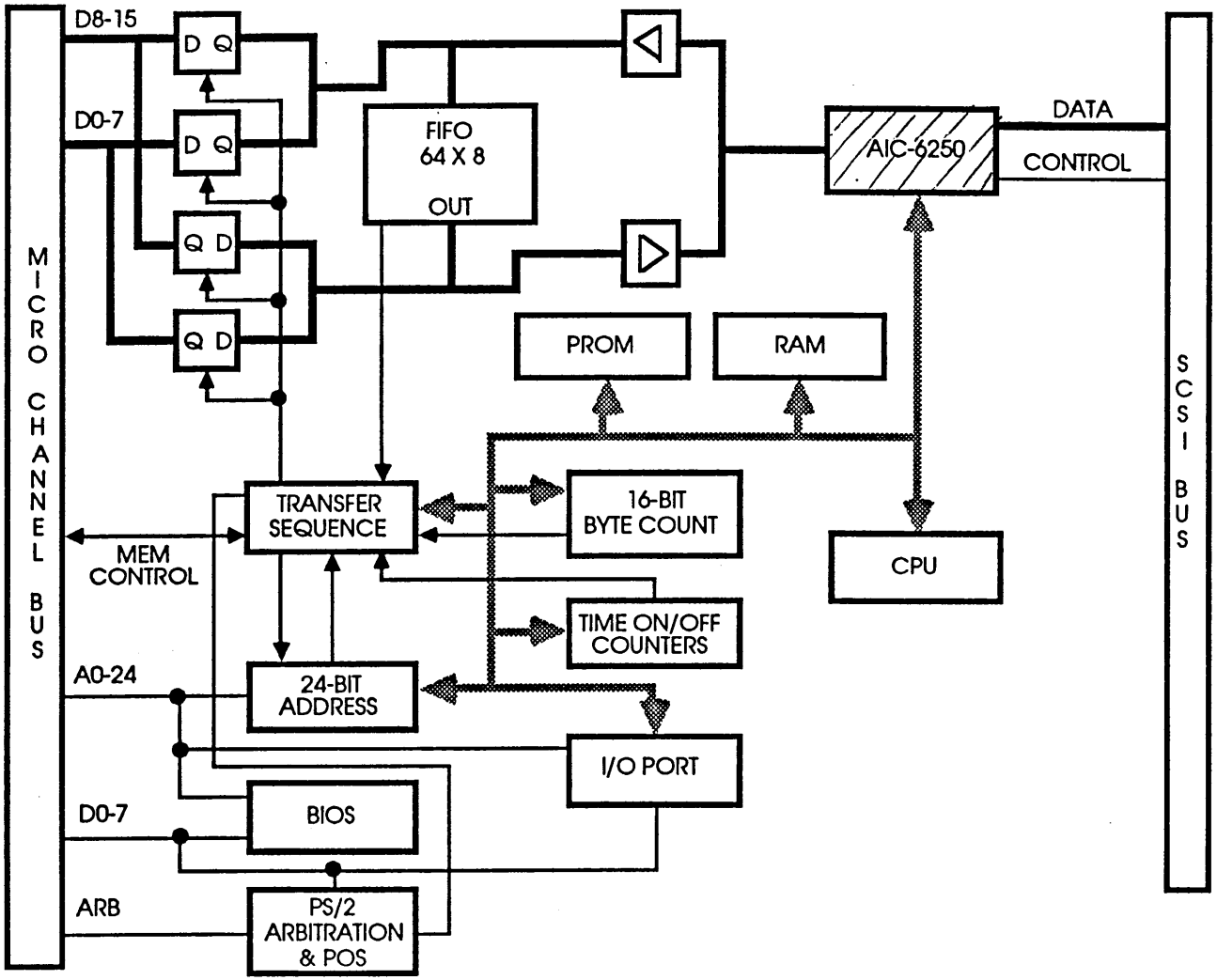
AHA-1640 Micro Channel to SCSI Host Adapter

FEATURE	BENEFIT
• Target mode capability	• Implements a high bandwidth local net
• Special high-performance functions, including zero latency read and queuing	• Faster response time and higher throughput
• Software compatible with AHA-1540	• Transferability of most software
• Drivers available for large variety of operating systems	• Allows installation into MS-DOS, OS/2, XENIX, and other operating environments
• Programmable option select	• AHA-1640 is self-installing
• Thoroughly tested with CHIPS and IBM systems	• Reliable and error-free operation

AHA-1640 Micro Channel to SCSI Host Adapter

FEATURE	BENEFIT
• Fully-implemented Micro Channel	• Compatible with PS/2 Models 50/60/80
• Bus master capability	• Transfers data at full bandwidth of bus
• Full multitasking capability	• Takes full advantage of multitasking capabilities of OS/2 and XENIX
• Supports conformance level 2 SCSI, CCS, and SCSI-2	• One bus supports many types of devices, including optical disk, high-performance magnetic disk, tape, and paper I/O
• Asynchronous transfer to >2 MBytes	• Supports fast low-cost devices
• Synchronous transfer to 5 MBytes	• Supports very high performance and high bandwidth of newest devices

AHA-1640 PS/2 to SCSI Host Adapter



Configuration Comparison: IBM PS/2 Model 80 With and Wthout SCSI Support

	IBM PS/2 Model 80	Adaptec AHA-1640
SCSI Attachment	Not available	Full synchronous, multitasking, SCSI support
Number of Disk Drives Supported	2 70-314 MB/drive	Up to 56 drives; full range of capacity and performance alternatives
Tape Support	Optional tape controller required	Fully supported by SCSI
Other Peripherals	Printers	Optical disk, printers, scanners, LANs, etc.
Multitasking Support	Up to 3 simultaneous tasks	Up to 255 simultaneous tasks
I/O Bus Bandwidth	Not applicable	5 MB/sec
Host Bus Bandwidth	3.3 MB/sec	8 MB/sec

Adaptec Products for High-Performance Personal Computers

	Product	Availability
AT	ACB-2320 ESDI PC/AT Hard Disk Controller	Now
AT	ACB-2322 ESDI PC/AT Hard Disk and Floppy Controller	Now
AT	ACB-2370 RLL PC/AT Hard Disk Controller	Now
AT	ACB-2372 RLL PC/AT Hard Disk and Floppy Controller	Now
AT	AHA-1540 PC/AT to SCSI Host Adapter	Now
PS/2	ACB-2072 RLL Models 25/30 Hard Disk Controller	Now
PS/2	AHA-1020 PS/2 Models 25/30 to SCSI Host Adapter	Now
PS/2	ACB-2610 MFM Models 50/60 Hard Disk Controller	1Q 88
PS/2	ACB-2670 RLL Models 50/60 Hard Disk Controller	2Q 88
PS/2	ACB-26M20 ESDI Models 60/80 Multitasking Hard Disk Controller	3Q 88
PS/2	AHA-1640 Micro Channel to SCSI Host Adapter	3Q 88

Software Support for PS/2-Compatible Products

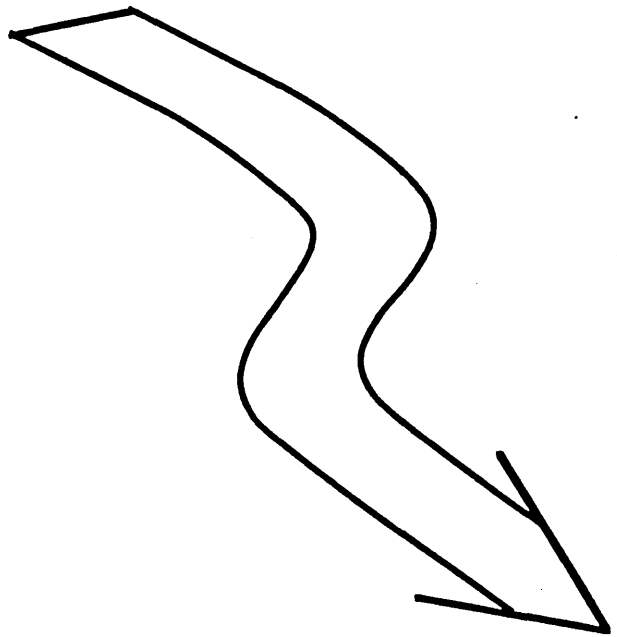
- **DOS**
  - Controllers fully functional with DOS 3.3 and greater
  - Drivers available for host adapters
- **OS/2**
  - Controllers compatible with OS/2
  - Drivers available for host adapters
- **SCO (Santa Cruz Operations) XENIX System V**
  - Standard product fully supports controllers and host adapters
- **UNIX**
  - Drivers available for controllers and host adapters
- **Novell Netware V 2.1**
  - Installable device drivers available for all products from Adaptec
- **BIOS**
  - ACB-2610 is 100% compatible with IBM BIOS
  - ACB-2670 available with optional BIOS for > 17 sectors/track
  - ACB-26M20: BIOS on board

Second Generation Features

- Controllers
  - Bus master
  - Embedded SCSI port
  - Disk mirroring
  - Faster bus transfer rates
- Host Adapters
  - Caching
  - Faster bus transfer rates

Adaptec Meets the PS/2 Challenge

- Total focus on I/O
- Mainframe expertise
- High-performance PC/AT solutions
- Adaptec chips in IBM PS/2



- 100% PS/2 compatibility

—plus—

- Higher performance
- Capacity alternatives
- Peripheral connectivity

SCO

THE SANTA CRUZ OPERATION

SCO XENIX System V Operating System

- Over 5,000 SCO XENIX systems already shipped for PS/2 Models 50/60/80
- Binary compatibility with over 250,000 installed XENIX systems
- Runs DOS programs as a task with SCO VP/ix: co-developed with Phoenix
- Supports CHIPS and Adaptec components
- Custom code for CHIPS, Adaptec, and OEM "Compatibility Plus" features
- Supports IBM and popular third-party peripherals

SCO XENIX System V Operating System

- SCO XENIX System V for the Personal System/2 and compatibles
- UNIX 5.3 licensed operating system
- Multiuser, multitasking
- Protected 286 mode and demand paged 32-bit virtual memory 386 mode
- Domestic and international versions
- Complete SCO solution including graphics, connectivity and applications

Complete System V Operating System Solution

- SCO XENIX System V Operating System
  - Supports as many users as hardware configuration allows
- SCO XENIX System V Development System
  - Complete with Microsoft C and SCO CGI Graphics Development System
- SCO XENIX System V Text Processing System
  - Text analysis and formatting and intelligent on-line manuals
- SCO XENIX Documenters WorkBench System
  - Advanced typesetting supports many lasers printers

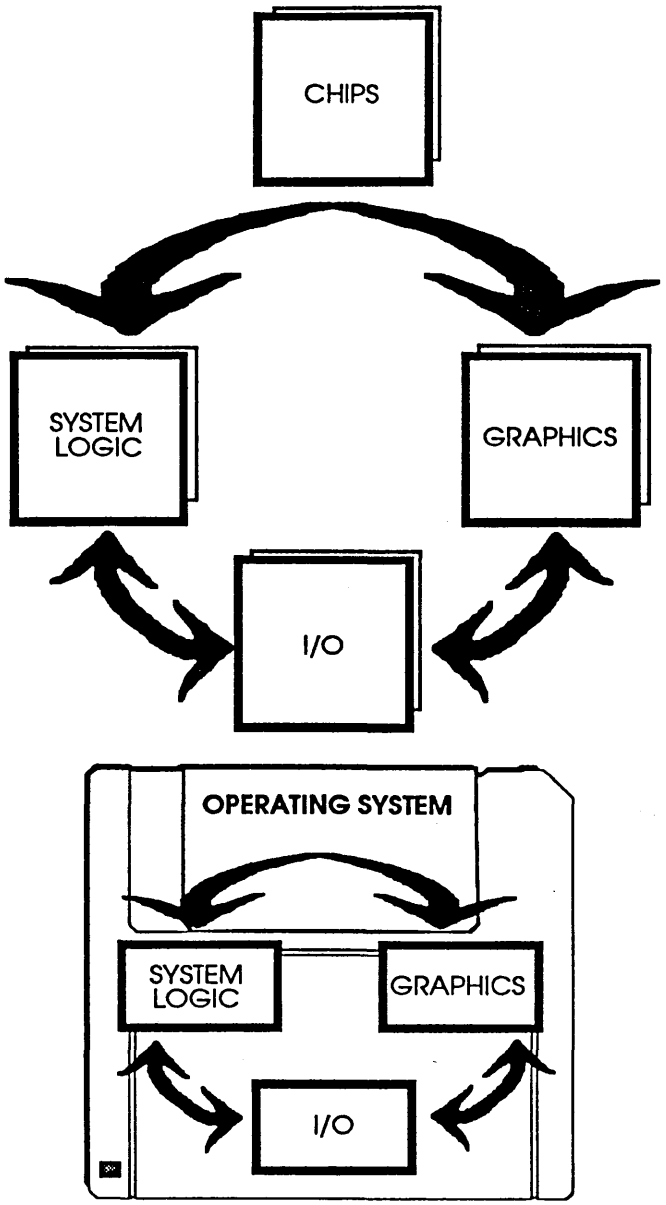
Systems Applications for PS/2's

- SCO VP/ix
  - Run DOS applications transparently under SCO XENIX 386
- SCO MultiView
  - Multitasking windows on console or terminals
- SCO XENIX-Net
  - PC-networks compatible XENIX/XENIX, XENIX/DOS connectivity
- SCO SNA-3270
  - Mainframe communications

SCO Solution

SCO Applications Family

- SCO Professional
  - 1-2-3 workalike
- SCO Foxbase and Foxbase+
  - Dbase II & III workalikes
- SCO Lyrix
  - Advanced word processing
- SCO Masterplan
  - Project planning
- SCO Statistician
  - Advanced statistics
- SCO ImageBuilder
  - Business and presentation graphics



The First Choice In PS/2 Solutions

CHIPS and Adaptec

Compatibility

PLUS

Higher Performance

Integrated Software

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Netware is a registered trademark of Novell, Inc.

VME is a trademark of Motorola

1-2-3 is a registered trademark of Lotus Development Corp.

dBase II & III are trademarks of Ashton-Tate

SCO is a trademark of The Santa Cruz Operation

82C221, 82C222, 82C223, 82C225, 82C226, 82C607, 82C451
CHIPS/250: Complete IBM® PS/2™ MODEL 50/60 Compatible CHIPSet™

- 100% IBM PS/2 Model 50/60 Compatible Chipset
- Supports 10, 12, 16 and 20 MHz 80286 based Systems
- Complete IBM PS/2 Model 50 Compatible Mother Board requires 68 components plus memory
- Available as CMOS PLCC and PFP Components

SYSTEM LOGIC CS8225 CHIPSET

- Asynchronous CPU, DMA and Micro Channel™ Operation
- Advanced Page/Interleave Memory Controller with Integrated Bad Block Remapping Capability, Shadow RAM and LIM EMS 4.0 Support
- Slow DRAMs at high CPU clock speeds, without Wait State penalty - 0.5 to 0.7 wait states with:
  150ns DRAMs @ 12.5 MHz
  120ns DRAMs @ 16 MHz
  80ns DRAMs @ 20 MHz
- Integrated Lotus-Intel-Microsoft Expanded Memory Specification (LIM OMS 4.0) Memory Controller expandable to full LIM EMS 4.0 specification with 8 register sets of 64 mapping registers
- High performance, proprietary Matched Memory interface for Micro Channel Memory Adapters

GRAPHICS

- Enhanced Gate-level Compatible VGA
- High performance, proprietary FAST VGA interface to CPU controller

PERIPHERAL SUPPORT

- Integrated Analog Data Separator and 16550 compatible serial port

CHIPS/250 is a 7-chip, Enhanced CMOS implementation of most of the system logic necessary to implement IBM PS/2 Model 50/60 compatible personal computers. CHIPS/250 will enable OEMs to offer PCs that are more functional, more integrated and clearly higher in performance than IBM's Model 50 and Model 60.

CHIPS/250 includes the CS8225 System Logic CHIPSet, the 82C607 Multi-Function Controller with an Analog FDC Data Separator and 16550 compatible serial port, and the Enhanced Gate-Level Compatible 82C451 VGA chip. With these 7 VLSI devices, it requires only 61 additional components plus memory to implement superior PCs to IBM's models.

System Logic CS8225 CHIPSet

The CS8225 System Logic CHIPSet consists of the 82C221 CPU and Micro Channel Controller, the 82C222 Page/Interleave and EMS Memory Controller, the 82C223 DMA Controller, the 82C225 Data/Address Bus Buffer and the 82C226 System Peripherals Controller. Each of these 5 components is available in 84-pin PLCC and 100-pin PFP.

The 82C221 CPU and Micro Channel Controller manages the system timing for the asynchronous CPU, DMA and Micro Channel cycles. It supports CPU clock speeds from 10, 12, 16 to 20 MHz. It supports all Micro Channel cycles, along with Matched Memory and Fast VGA cycles. It includes state machines for command and control logic signal generation, DMA and refresh logic control.

The 82C222 Page/Interleave and EMS Memory Controller provides an interleaved memory subsystem design with page mode operation. It supports 4 memory banks, with memory configurations from 640KB to 8MB. While operating under DOS, memory above 1MB can be treated as EMS memory, improving significantly the value of the large memory organizations of the OS/2 era. The on-chip EMS logic provides 4 mapping registers, however, with external EMS mappers, the full

LIM EMS 4.0 specification with 8 sets of 64 mapping registers can be implemented.

The 82C223 DMA Controller provides 8 DMA channels for slave devices and the Central Arbitration Control Point (CACP) for the entire system. Each DMA Channel has 24-bit address capability and can perform 8-bit or 16-bit transfers. It also supports Virtual DMA so that DMA Channels 0 and 4 can be used to service multiple DMA slaves by multiplexing the DMA Channels between the arbitration levels assigned to those slaves. It supports Multiple Bus Masters via the CACP arbitrator and control signals which enable Bus Masters to monitor the readiness and data size of other adapters and system board components. The Bus Arbitration logic includes protection mechanisms against error conditions, like burst-mode devices not relinquishing the bus within the specified time.

The 82C225 Data Bus Buffer provides high speed bus switching support to enable the use of low speed DRAMs at high clock speeds.

The 82C226 System Peripherals Controller integrates PS/2 compatible peripherals in one compact package, with an optimized bus interface to the Peripheral Bus. It includes two 8259 compatible interrupt controllers, one 8254 compatible timer, one 146818 compatible real-time clock, 114 bytes of CMOS battery back-up RAM and one PS/2 compatible Bi-directional Parallel Port.

Graphics

The 82C451 Gate Level compatible VGA provides 100% VGA compatible graphics with backwards compatibility to EGA, CGA, MDA and Hercules. In VGA Graphics modes, it provides resolutions from 320 × 200 with 256 colors to 640 × 480 with 16 colors. In VGA text mode, it supports fonts up to 9 × 32. It supports all standard monitors—IBM PS/2 analog, Multi-frequency, EGA, CGA and Monochrome. The 82C451 boosts graphics performance with a tightly coupled high performance interface to the CPU and a 16-bit memory interface. The 82C451 is packaged in a 144 pin PFP package.

Peripheral Support

The 82C607 Multi-Function Controller integrates additional PS/2 compatible peripherals in one compact package. It includes one 16550 Compatible UART, an Analog Data Separator, POS registers and Glue Logic for a NEC 765A Floppy Disk Controller. The 82C607 is available in a 68 pin PLCC package.

Additional components that complement CHIPS/250 are the MicroCHIPS for Micro Channel Adapters and EMS Mapper Chips. The 82C610 and 82C611 MicroCHIPs can be used for I/O intensive Micro Channel Adapters, while the 82C612 is applicable to Adapters that require Slave DMA support.

CHIPS

Chips and Technologies, Incorporated

3050 Zanker Road, San Jose, CA 95134 408-434-0600 Telex 272929 CHIP UR

82C321, 82C322, 82C223, 82C325, 82C226, 82C607, 82C451
CHIPS/280: Complete IBM® PS/2™ Model 80 Compatible CHIPSet™

- 100% IBM PS/2 Model 80 Compatible Chipset
- Supports 16, 20 and 25 MHz 80386 based Systems
- Complete IBM PS/2 Model 80 Compatible Mother Board requires only 66 components plus memory
- Available as CMOS PFP Components

SYSTEM LOGIC CS8238 CHIPSet

- Asynchronous CPU, DMA and Micro Channel™ Operation
- Advanced Page/Interleave Memory Controller with Integrated Bad Block Remapping Capability, Shadow RAM and LIM EMS 4.0 Support
- Supports static column DRAMs
- Slow DRAMs at high CPU clock speeds, without Wait State penalty: 0.5 to 0.7 wait states with:

  100ns DRAMs @ 16 MHz
  80ns static column DRAMs @ 20 MHz

- Integrated Lotus-Intel-Microsoft Expanded Memory Specification (LIM EMS 4.0) Memory Controller expandable to full LIM EMS 4.0 specification with 8 register sets of 64 mapping registers
- High performance Matched Memory interface for Micro Channel Memory Adapters at 16 MHz, 20 MHz and 25 MHz
- Supports a CHIPS FAST Micro Channel Matched Memory Cycle which can increase access to memory on the Micro Channel by up to 33%.
- PS/2 Model 80 Compatible Address Recovery Logic
- User Programmable I/O Decodes
- OS/2 Optimizations

GRAPHICS

- Enhanced Gate-level Compatible VGA
- High performance, FAST VGA interface to CPU controller

PERIPHERAL SUPPORT

- Integrated Analog Data Separator and 16550 compatible serial port

CHIPS/280 is a 7-chip, Enhanced CMOS implementation of most of the system logic necessary to implement IBM PS/2 Model 80 compatible personal computers. CHIPS/280 enables OEMs to offer PCs that are more functional, more integrated and higher in performance than IBM's Model 80.

CHIPS/280 includes the CS8238 System Logic CHIPSet, the 82C607 Multi-Function Controller with an Analog FDC Data Separator and 16550 compatible serial port, and the Enhanced Gate-Level Compatible 82C451 VGA chip. With these 7 VLSI devices, it requires only 59 additional components plus memory to implement superior PCs to IBM's models.

System Logic CS8238 CHIPSet

The CS8238 System Logic CHIPSet consists of the 82C321 CPU and Micro Channel Controller, the 82C322 Page/Interleave and EMS

Memory Controller, the 82C223 DMA Controller, the 82C325 Data/Buffer Controller and the 82C226 System Peripherals Controller. The 82C321 is available in a 100 pin PFP, the 82C322 and the 82C325 are available in a 144 pin PFP, and the 82C223 and 82C226 are available in both a 84 pin PLCC and 100 pin PFP packages.

The 82C321 CPU and Micro Channel Controller manages the system timing for the asynchronous 80386 CPU, DMA and Micro Channel cycles. It supports CPU clock speeds from 16, 20, to 25 MHz. It supports all Micro Channel cycles, along with Matched Memory and Fast VGA cycles at 16, 20 and 25 MHz. It includes state machines for command and control logic signal generation, DMA and refresh logic control. It also supports a CHIPS FAST Micro Channel Matched Memory Cycle which can increase access to memory on the Micro Channel by up to 33%.

The 82C322 Page/Interleave and EMS Memory Controller provides an interleaved memory subsystem design with page mode operation. It supports 4 memory banks, with memory configurations from 1MB to 16MB. While operation under DOS, memory above 1MB can be treated as EMS memory, improving significantly the value of the large memory organizations of the OS/2 era. The on-chip EMS logic provides 4 mapping registers, however, with external EMS mappers, the full LIM EMS 4.0 specification with 8 sets of 64 mapping registers can be implemented. It supports static column DRAMs and shadow RAM BIOS. It contains on board I/O decode logic and IBM PS/2 Model 80 compatible Address Recovery Logic.

The 82C223 DMA Controller provides 8 DMA channels for slave devices and the Central Arbitration Control Point (CACP) for the entire system. Each DMA Channel has 24-bit address capability and can perform 8-bit or 16-bit transfers. It also supports Virtual DMA so that DMA Channels 0 and 4 can be used to service multiple DMA slaves by multiplexing the DMA Channels between the arbitration levels assigned to those slaves. It supports Multiple Bus Masters via the CACP arbitrator and control signals which enable Bus Masters to monitor the readiness and data size of other adapters and system board components. The Bus Arbitration logic includes protection mechanisms against error conditions, like burst-mode devices not relinquishing the bus within the specified time.

The 82C325 Data Buffer/Controller provides high speed bus sizing and conversion to enable the use of low speed DRAMs at high clock speeds. It contains system POS registers, and NMI as well as DRAM parity generation and detection logic. User programmable I/O ports, 82C607 Decode Signals, and 82C451 VGA Setup and Enable Signals are also contained in the 82C325.

The 82C226 System Peripherals Controller integrates PS/2 compatible peripherals in one compact package, with an optimized bus interface to the Peripheral Bus. It includes two 8259 compatible interrupt controllers, one 8254 compatible timer, one 146818 compatible real-time clock, 114 bytes of CMOS battery back-up SRAM and one PS/2 compatible Bi-directional Parallel Port.

Graphics

The 82C451 Gate Level compatible VGA provides 100% VGA compatible graphics with backwards compatibility to EGA, CGA, MDA and Hercules. In VGA Graphics modes, it provides resolutions from 320 × 200 with 256 colors to 640 × 480 with 16 colors. In VGA text mode, it supports fonts up to 9 × 32. It supports all standard monitors—IBM PS/2 analog, Multi-frequency, EGA, CGA and Monochrome. The 82C451 boosts graphics performance with a tightly coupled high performance interface to the CPU and a 16-bit memory interface. The 82C451 is packaged in a 144 pin PFP package.

Peripheral Support

The 82C607 Multi-Function Controller integrates additional PS/2 compatible peripherals in one compact package. It includes one 16550 Compatible UART, an Analog Data Separator, POS registers and Glue Logic for a NEC 765A Floppy Disk Controller. The 82C607 is available in a 68 pin PLCC package.

Additional components that complement CHIPS/280 are the MicroCHIPS for Micro Channel Adapters and EMS Mapper Chips. The 82C610 and 82C611 MicroCHIPs can be used for I/O intensive Micro Channel Adapters, while the 82C612 is applicable to Adapters that require Slave DMA support.

CHIPS

Chips and Technologies, Incorporated

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82C100, 82C101
IBM™ PS/2 Model 30 and Super XT™ Compatible Chips

- **100% PC/XT compatible**
- **Build IBM PS/2™ Model 30 with XT software compatibility**
- **Bus Interface compatible with 8086, 80C86, V30 8088, 80C88, V20**
- **Includes all PC/XT functional units compatible with:**

  8284, 8288, 8237, 8259, 8253, 8255, DRAM control, SRAM control, Keyboard control, Parity Generation and Configuration registers
- **Key superset features: EMS control, dual clock, and power management**
- **Complete system requires 12 ICs plus memory**
- **10 MHz Zero wait state operation**
- **Applicable for high performance Desktop PCs, Laptop PCs and CMOS Industrial Control Applications**
- **Single chip implementations available in 100-pin flat pack and 84-pin PLCC packages**

The 82C100 and the 82C101 are single chip implementations of most of the system logic necessary to implement a super XT compatible system with PS/2 Model 30 functionality using either an 8086 or 8088 microprocessor. The 82C100 can be used with 8 or 16-bit microprocessors, while the 82C101 is tailored to operate with 8-bit microprocessors. The 82C100 includes features which will enable the PC manufacturer to design a Super PS/2 Model 30/XT compatible system with the *highest performance* at 10 MHz zero wait state system with an 8086, the *highest functionality* with dual clock and 2.5 MB DRAM (with integrated Extended Memory System control logic), the *lowest power* implementation by utlizing the on-chip power management features and the *highest integration* with the lowest component count SMT design.

The 82C100 or 82C101 can be combined with CHIPS' 82C606 CHIPSpak, 82C441/442 VGA Graphics Controller and 82C764A Analog Data Separator, to provide a high performance, high integration PS/2 Model 30 type system.

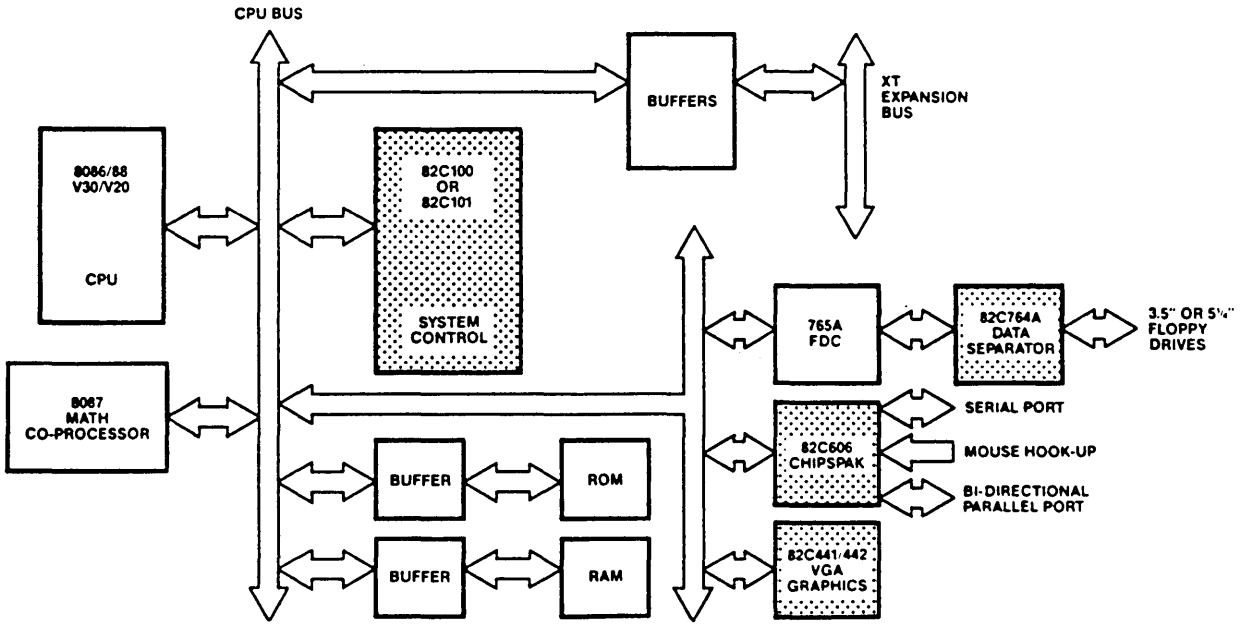

Figure 1. Super XT Model 30 Compatible System

The 82C100/82C101 support most of the peripheral functions on the PS/2 Model 30 planar board: 8284 compatible clock generator with the option of 2 independent oscillators, 8288 compatible bus controller, 8237 compatible DMA controller, 8259 compatible interrupt controller, 8253 compatible timer/counter, 8255 compatible peripheral I/O port, XT Keyboard interface, Parity Generation and Checking for DRAM memory and memory controller for DRAM and SRAM memory sub-systems.

The 82C100/82C101 enables the uses to add PS/2 Model 30 superset functionality on the planar board: dual clock with synchronized switching between the two clocks, built-in Lotus-Intel-Microsoft™ (LIM) EMS support for up to 2.5 Megabytes of DRAM and power management features for SLEEP mode as well as SUSPEND/RESUME operations. The SLEEP and SUSPEND/RESUME features help in preserving the battery life in laptop portable applications.

The 82C100/82C101 support a very flexible memory architecture. For systems with DRAMs, the DRAM controller supports 64K, 256K and 1M DRAMS. These DRAMs can be organized in four banks of up to a maximum of 2.5 MB on the planar board. The 2.5 MB memory can be implemented with 2 banks of 1M × 1 DRAMs, partitioned logicaly as 640KB of real memory and 1.875MB of EMS memory. For systems which require low operating power and minimum standby power dissipation, the chips provide the decode logic which in conjunction with external decoders allows selection of up to 640KB of static RAM. This option is useful in laptop portable application.

The 82C100 is packaged in 100-pin plastic flatpack, and the 82C101 is packaged in 84-pin PLCC.

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3050 Zanker Road, San Jose, CA 95134 408-434-0600 Telex 272929 CHIP UR

82C451 CHIPS Integrated VGA

- **Fully IBM™ VGA Compatible at hardware, register and BIOS level.**
- **Dual Bus Architecture. Integrated interface to PC-Bus and Microchannel (CHIPS/250 and CHIPS/280).**
- **Single Chip Solution.**
- **Proprietary High Speed Interface to CHIPS/250 and CHIPS/280 Systems.**
- **Supports 8 and 16 bit CPU interface for memory and I/O cycles.**
- **Supports external palette DAC of up to 16 million colors.**
- **Resolutions up to 640*480 in 16 colors, 960*720 in 4 colors and 1280*960 monochrome.**
- **Enhanced backward compatibility with EGA, CGA, Hercules™, MDA without using NMI.**
- **Processor Latches and Attribute Flip Flop are readable.**
- **Pinout Compatible with 82C452. Same design can use both parts.**

CPU Interface

82C451 has a strap option to select a PC-Bus Interface or a Microchannel Interface. All control signals for both the interfaces are integrated into the single chip.

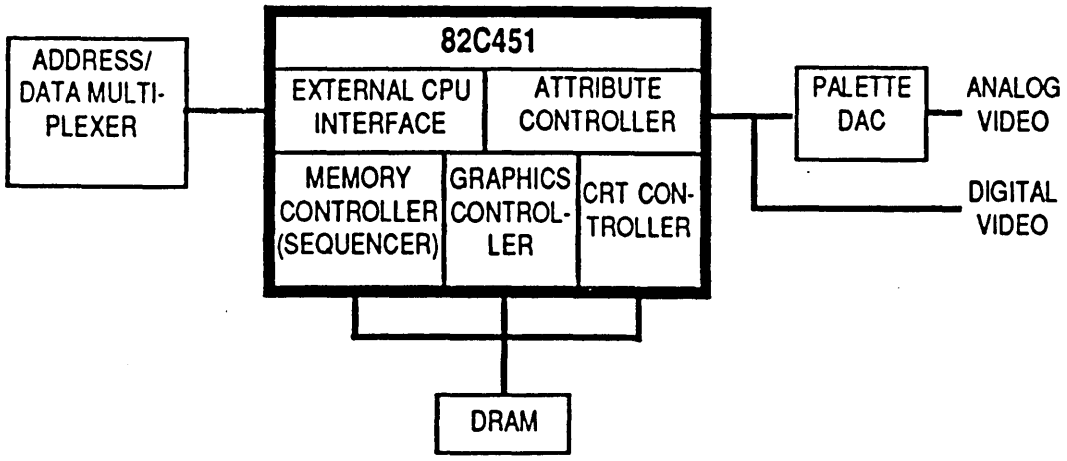
82C451 supports both a 8 bit and 16 bit CPU interface. The 16 bit interface can be independently enabled/disabled for memory and I/O cycles. On reset, the chip is configured for 8 bit accesses for memory and I/O cycles. 16 bit interface for I/O cycles is restricted to index/data pair of registers. This includes the Sequencer (3C4h), Graphics Controller (3CEh), CRT Controller (3B4h/3D4h) and the Attribute Controller (3C0h). All other I/O addresses (color palette, Misc Output and Status) are always treated as 8 bit ports.

If the 16 bit interface is chosen, then depending on the state of A0 and $\overline{BHE}$, either a 8 bit or 16 bit cycle will actually be executed. This ensures compatibility with old software.

All I/O cycles are completed without wait states. For memory cycles, the cycles are extended with wait states.

BIOS ROM Interface

In the PC-BUS Interface, the 82C451 supports an external BIOS ROM. The ROM address is decoded and the $\overline{ROMCS}$ pin is asserted to enable ROM data on the CPU bus. In the Microchannel Interface, the system BIOS includes the video BIOS.



82C451 System Diagram

Display Modes and Resolution

82C451 supports a superset of all VGA display modes. It supports resolutions upto 640*480 in 16 colors, 960*720 in 4 colors and 1280*960 in monochrome.

Memory Interface

The entire display memory (256 Kbytes) is always available to the CPU in regular 4 plane mode, chained 2 plane mode and in super chained 1 plane mode.

The display memory control signals are derived from the dot clock. The MCLK is used for internal sequencing of 16 bit memory cycles. MCLK should be 25-40 MHz.

Extended Registers

All functionality of the extended registers in 82C451 are disabled on reset. Before the extended registers can be written into, they must be enabled by two sets of control bits (disabled on reset). The Processor Latches in the Graphics Controller and the Attribute Flipflop are readable in the extended register space. **No new bits are defined or any of the unused bits used in the regular VGA registers.**

External Palette Interface

82C451 supports programming of an external palette DAC by decoding the CPU addresses and generating the $\overline{RD}$ and $\overline{WR}$ signals to the external palette. 82C451 decodes I/O addresses 3C6-3C9h as valid external palette addresses.

High Speed CPU Interface

82C451 supports a high speed interface to CHIPS/250 and CHIPS/280 systems. There are special interface pins on the CHIPS/250, CHIPS/280 and 82C451. Using these special interface pins, CPU accesses to the 82C451 can be executed faster than CPU accesses to other peripheral devices.

The 82C451 is packaged in a 144 pin plastic flat pack (PFP).

CHIPS

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82C452 CHIPS Super VGA

- **Fully IBM™ VGA Compatible at hardware, register and BIOS level.**
- **Dual Bus Architecture. Integrated interface to PC-Bus and Microchannel (CHIPS/250 and CHIPS/280).**
- **Single Chip Solution.**
- **Proprietary High Speed Interface to CHIPS/250 and CHIPS/280 Systems.**
- **Supports 8 and 16 bit CPU interface.**
- **Graphics Cursor with transparency.**
- **Resolutions up to 640*480 in 256 colors, 960*720 in 16 colors and 1280*960 in 4 colors**
- **Enhanced backward compatibility with EGA, CGA, Hercules™, MDA without using NMI.**
- **Intelligent memory cycle arbitration to maximize CPU bandwidth.**
- **Pinout compatible with 82C451. Same board design can use both parts.**
- **New Patented Write Mode to speed up graphics text.**

CPU Interface

82C452 has a strap option to select the PC-Bus Interface or the Microchannel Interface. All control signals for both the interfaces are integrated on the single chip.

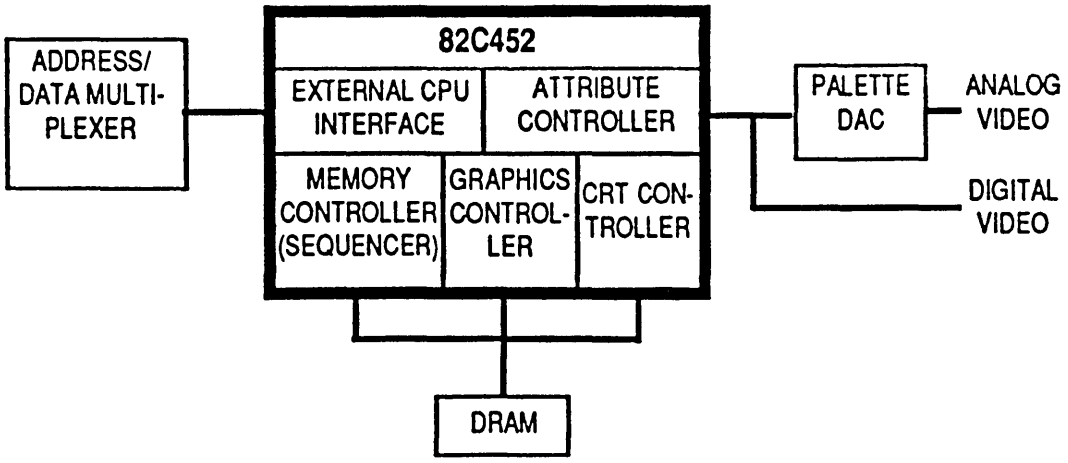
82C452 supports both 8 and 16 bit CPU interface. The 16 bit interface can be independently enabled/disabled for memory and I/O cycles. On reset, the chip is configured for 8 bit cycles. The 16 bit interface for I/O cycles is restricted to the index/data pair of registers. This includes the Sequencer, Graphics Controller, CRT Controller and the Attribute Controller. All other registers are always treated as 8 bit ports.

If the 16 bit interface is selected, then software can still execute 8 bit cycles. This ensures compatibility with old software.

All I/O cycles are completed without wait states. Memory cycles are arbitrated using an intelligent algorithm and is completed in the fastest possible time.

BIOS ROM Interface

In the PC-BUS Interface, the 82C452 supports an external BIOS ROM. The ROM address is decoded and the $\overline{\text{ROMCS}}$ pin is asserted to enable ROM data to the CPU.



82C452 System Diagram

Display Memory Interface

The 82C452 supports a high speed page mode DRAM interface. This along with the 16 bit data path and intelligent CPU arbitration, can improve CPU performance by upto 8 times.

The 82C452 supports 256 KB, 512 KB and 1 MB of display memory as follows:

8 devices 64k*4	256KB
16 devices 64k*4	512KB
8 devices 256k*4	1MB

The entire display memory (256 Kbytes, 512 Kbytes or 1 Mbyte) is always available to the CPU in regular 4 plane mode, chained 2 plane mode and in super chained 1 plane mode.

The display memory control signals are derived from an independent clock (MCLK). For 120ns DRAMs, the MCLK frequency should be in the range of 30-33 MHz. This can support a 50 MHz (4 bits/pixel) video data stream. With 100ns DRAMs, the MCLK frequency can be upto 35-36 MHz. At this frequency, the average number of wait states for the CPU is reduced resulting in higher performance.

Display Modes and Resolution

82C452 supports a superset of all VGA display modes. The maximum display bandwidth is 200 Mbits/s — 25 MHz at 8 bit/pixel or 50 MHz at 4 bit/pixel. This translates to resolutions up to 640*480 in 256 colors (packed pixel mode), up to 960*720 in 16 colors (both planar and packed pixel mode) and up to 1280*960 in 4 colors (both planar and packed pixel mode).

Extended Registers

All functionality of the extended registers in 82C452 are disabled on reset. Before the extended registers can be written into, they must be enabled by two sets of control bits (disabled on reset). The Processor Latches in the Graphics Controller and the Attribute Flipflop are readable in the extended register space. **No new bits are defined or any of the unused bits in the regular VGA registers are used.**

Graphics Cursor

82C452 supports a 32 pixel wide and 512 pixel high hardware graphics cursor. The graphics cursor supports transparency and can be any arbitrary shape within the outline box. The hardware cursor is based on the definition of the graphics pointer in Microsoft Windows™. Use of the hardware cursor frees the CPU of the responsibility of managing the pointer in any graphics environment like Windows™ or Presentation Manager, leading to improved performance of the application programs.

External Palette Interface

The 82C452 supports programming an external palette DAC by decoding the CPU addresses and generating the READ and WRITE signals for the external palette.

The 82C452 is packaged in a 144 pin plastic flat pack (PFP).

CHIPS

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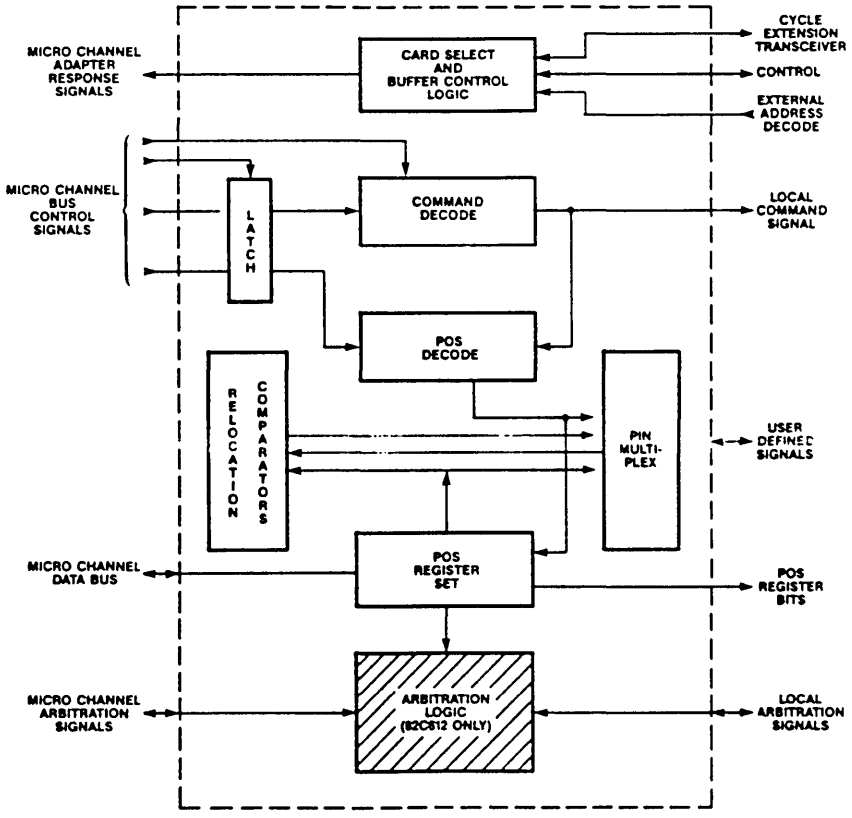
82C611, 82C612
MicroCHIPS™: Micro Channel™ Interface Parts

- **Implements 100% IBM® PS/2™ Compatible Micro Channel Adapters**
- **82C611 Supports Multi-function, I/O and Memory Adapters.**
- **82C612 Supports Controller-type Adapters Including All DMA Slave Arbitration Functions.**
- **Programmable Option Select (POS) Support Including:**
  - **Adapter ID Support**
  - **Flexible I/O and Memory Relocation Support**
  - **POS Port Decode Logic and Handshaking**
- **Full Micro Channel Interface Including:**
  - **Command and Status Decoding**
  - **Response Signal Generation**
  - **Full DMA Slave Arbitration and Handshake (82C612 only)**
- **Meets all IBM specified Timing and Drive Specifications.**
- **Simplifies migration of XT/AT adapter designs to the Micro Channel.**
- **Available as 68-pin PLCC or 80-pin PFP components.**

Description

The MicroCHIPS (Micro Channel Interface Parts) family of components integrates most of the interface logic required on an adapter card for the Micro Channel—IBM's new high speed bus for its latest generation of PCs. MicroCHIPS provide many benefits to designers of add-in adapters for the Micro Channel: Space savings because of the single-chip VLSI approach, cost savings because of the integration of many components into one, and time savings because of the ease of design.



Simplified Block Diagram of the 82C611/612

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DK8250 Model 50/60 Development Kit

- **80286 CPU running at 10, 12, 16, or 20 MHz.**
- **Socket for 80287.**
- **Up to 2 MB on the System Board using 256K DRAMs or 8 MB using 1 MB DRAMs.**
- **Sockets for four 256K EPROMS for the BIOS.**
- **Support for Advanced Memory Control with Page Interleaved memory, LIM EMS 4.0, and Shadow RAM.**
- **One serial port and one parallel port, each with a 25 pin connector.**
- **VGA controller with 256KB of video memory and a 15 pin video connector.**
- **Integrated floppy disk controller with connector.**
- **Integrated Keyboard and Mouse ports controller with PS/2 style connectors.**
- **Eight 16 bit Micro Channel connectors with 5 as standard 16 bit connectors, one with the Micro Channel Video Extension, and 2 with the Matched Memory Extension.**

The DK8250 development kit includes a complete package for a designer implementing a board product around the CHIPS/250 PS/2 Model 50 CHIPset. Included in this kit are product documentation, sample schematics, and the DB8250 evaluation board.

The DB8250 evaluation board implements a fully compatible PS/2 Model 60 style system on an 16" (41 cm) × 11" (28 cm) circuit board. The physical form factor of the board itself is compatible with IBM's Model 60 for use in system check-out.

This board is expressly designed to help the system designer to speed up the evaluation process and reduce the development time for products using the CHIPS/250 CHIPset. This board provides extra room for implementing patch circuitry and oscilloscope probe points for use as a design aid during prototype debugging.

This board makes use of the following Chips and Technologies chips from the CHIPS/250 CHIPset:

82C221 — CPU Controller
82C222 — Advanced Memory Controller
82C223 — DMA Controller
82C225 — Address/Data Buffer
82C226 — System Peripheral Chip
82C607 — Multifunction Controller
82C451 — Super VGA Controller

CHIPS

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DK8251 82C451 Super VGA Development Kit

- **256 KB of video memory.**
- **Support for either an 8 or 16 bit interface.**
- **Two video output connectors including a 9 pin digital output and a 15 pin analog output.**
- **Support for over 16 miliion colors using a triple 8-bit video DAC.**
- **PS/2 compatible video feature connector.**

The DK8251 development kit includes a complete package for a designer implementing a board product around the 82C451 VGA chip. Included in this kit are product documentation, sample schematics, and the DB8251 evaluation board.

The DB8251 evaluation board implements a fully IBM VGA compatible board at the hardware, register, and BIOS level. The board is the same size as a standard PC-XT plug in card and it interfaces to either the PC-AT or PC-XT busses.

This board is expressly designed to help the system designer to speed up the evaluation process and reduce the development time for products using the 82C451 VGA chip. This board provides extra room for implementing patch circuitry and oscilloscope probe points for use as a design aid during prototype debugging.

CHIPS

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TMP9251 82C451 Super VGA Turnkey Manufacturing Package

- **256 KB of video memory.**
- **Support of 8 and 16 bit CPU interface for memory and I/O cycles.**
- **Video output using a 15 pin analog connector.**
- **Support for over 16 million colors using a triple 8-bit video DAC.**
- **PS/2 compatible video feature connector.**

The TMP9251 supplies a complete manufacturing package for those who want to quickly produce an IBM VGA compatible board using the 82C451 VGA chip. This package includes a schematic, film, bill of materials, FCC test data, and a working prototype of the BD9251 VGA board.

The BD9251 VGA board implements a fully IBM VGA compatible board at the hardware, register, and BIOS level using the 82C451 single chip VGA controller. The board is two-thirds the size of a standard PC-XT plug-in card and it interfaces to the PC-XT or PC-AT bus.

The board uses surface mount technology in order to minimize production cost and to maximize the space efficiency of the design. Special attention is used to minimize the production cost of the design and includes such items as minimization of the number of layers in the board, using physical design rules which are compatible with automatic insertion, and usage of as much VLSI as practical to minimize assembly cost. Great care is taken in the layout and the design to minimize potential EMI problems on the board.

CHIPS

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TMP9250 Model 50 Turnkey Manufacturing Package

- **80286 CPU running at 10, 12, 16, or 20 MHz.**
- **Socket for 80287.**
- **Up to 2 MB on the System Board using 256K DRAMs or 8 MB using 1 MB DRAMs.**
- **Support for Advanced Memory Control with Page Interleaved memory, LIM EMS 4.0, and Shadow RAM.**
- **One serial port and one parallel port, each with a 25 pin connector.**
- **VGA controller with 256KB of video memory and a 15 pin video connector.**
- **Integrated floppy disk controller with connector.**
- **Integrated Keyboard and Mouse ports controller with PS/2 style connectors.**
- **Four 16 bit Micro Channel connectors with two as standard 16 bit connectors, one with the Micro Channel Video Extension, and one with the Matched Memory Extension.**

The TMP9250 supplies a complete manufacturing package for those who want to quickly produce an IBM PS/2 Model 50 compatible board using the CHIPS/250 CHIPset. This package includes a schematic, film, bill of materials, FCC test data, and a working prototype of the BD9250 Model 50 evaluation board.

The BD9250 evaluation board implements a PS/2 Model 50 style system on an 13" (33 cm) × 11" (28 cm) circuit board. Because of the use of a faster microprocessor and improved architecture in the memory and video interface areas, this board provides significantly higher performance than the comparable IBM product while still maintaining full compatibility. The physical form factor of the board itself is compatible with IBM's Model 50 for use in producing systems which are compatible with IBM in both fit and function.

The board is optimized to be highly manufacturable in order to achieve the minimum costs. This includes such items as minimization of the number of layers in the board, using physical design rules which are compatible with automatic insertion, and usage of as much VLSI as practical to minimize assembly cost. Also, great care is taken in the layout and design to minimize potential EMI problems on the board.

This board makes use of the following Chips and Technologies chips from the CHIPS/250 CHIPset:

82C221 — CPU Controller
82C222 — Advanced Memory Controller
82C223 — DMA Controller
82C225 — Address/Data Buffer
82C226 — System Peripheral Chip
82C607 — Multifunction Controller
82C451 — Super VGA Controller

CHIPS

Chips and Technologies, Incorporated

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IBM PS/2 Micro Channel Model 50/60 Compatible ST412/506 MFM Disk Controller

ACB-2610: Micro Channel™ ST412/506 MFM Disk Controller

Adaptec's ACB-2610 is a highly integrated ST412/506 MFM Winchester disk controller designed for the IBM Personal System/2™ Micro Channel™ architecture in system Models 50, 60, 80 and compatibles. Features such as 1:1 sector interleaving and host DMA transfers of 10 MBytes/second are only a few advantages of Adaptec's ACB-2610, as a result of incorporating Adaptec's pioneering VLSI technologies.

IBM PS/2 COMPATIBLE

ACB-2610 is fully port and BIOS compatible with IBM's Personal System 2 Models 50, 60 and 80. In addition, the ACB-2610 has been thoroughly tested with CHIPS/250, PS/2 Model 50 compatible system logic. That means your software will run with no modifications. The ACB-2610 has been successfully tested with MS-DOS® 3.3, OS/2™, XENIX® and UNIX® operating systems. Compatible manufacturers can take full advantage of software developed for IBM PS/2 systems.

ADVANCED VLSI TECHNOLOGY

The AIC-561 and AIC-562 are the latest additions to Adaptec's family of high-performance VLSI controller interface circuits. The AIC-581 implements all the logic necessary to comply with the programmable option select feature and arbitration protocols of the Micro Channel. The AIC-582 integrates the buffer controller and DMA logic enabling the ACB-2610 to achieve DMA transfer rates far superior to the standard IBM disk controller.

PROVEN ARCHITECTURE

At the heart of the ACB-2610 is the Adaptec AIC-011, programmable media sequencer, the next generation of the device used in IBM's PS/2 Model 80 ESDI disk controller. The AIC-011 architecture serves as the heart of all of Adaptec's high performance disk controllers. This device along with Adaptec's AIC-6225 high precision bipolar monolithic data separator give the ACB-2610 the highest reliability and data integrity available.

And to demonstrate Adaptec's commitment to Quality Excellence, we're extending Adaptec's **Limited Lifetime Warranty** to the ACB-2610.

HIGH PERFORMANCE

The ACB-2610 is the highest performance Micro Channel ST412/506 MFM disk controller available. With a disk data rate of 5 Mbits/second and full track buffering, and read-ahead cache, the ACB-2610 maintains 1:1 sector interleaving, while bursting data across the Micro Channel at DMA speeds up to 10 Mbytes/second. We've optimized the ACB-2610 for minimum use of your system's I/O bandwidth. That will leave more time for other I/O intensive operations to occur almost simultaneously, ideal for multitasking, multiuser and multiprocessor applications.

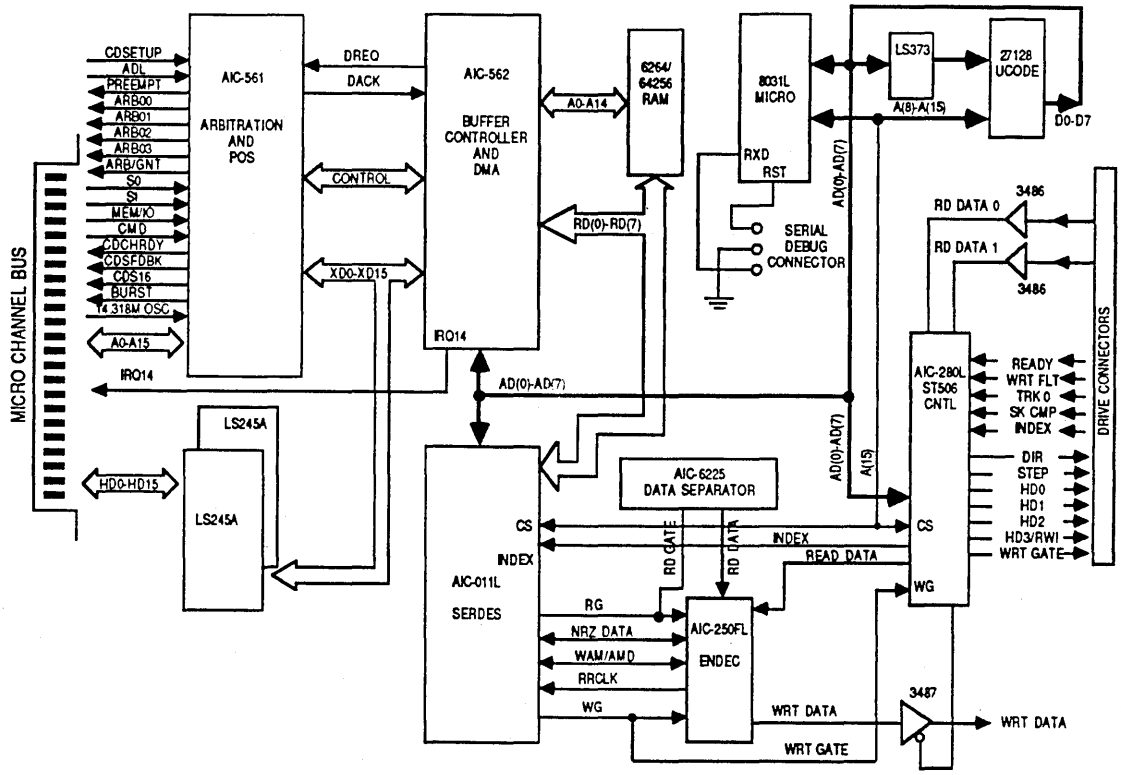
GREATER FLEXIBILITY

The ACB-2610 gives manufacturers the flexibility to configure systems with a wide variety of disk sizes and performance characteristics. The ACB-2610 fits in the PS/2 Models 50, 60 and 80, making it an ideal choice for compatible manufacturers that want to develop a broad price/performance range of systems. And for those developers requiring operating system support, Adaptec is providing I/O drivers for the most popular software, such as OS/2, XENIX, UNIX and Novell Netware™.

ADVANCE INFORMATION

adaptec, inc. • 580 cottonwood drive • milpitas, ca 95035 • (408) 432-8600

ACB-2610 Block Diagram



FEATURES

- 100% IBM Micro Channel Port and BIOS Compatible
- 1:1 Sector Interleaving
- Supports Two ST412/506 Disk Drives, 4096 Cylinders, 16 Heads
- MFM, 5 Mbits/Sec Drive Data Rate
- Burst DMA Up To 10 MBytes/Sec Or Programmed I/O Host Transfers
- Optional 8K, 32K, Or 64K Buffer
- Read-Ahead Cache
- High Precision Bipolar Monolithic Data Separator
- Surface Mount Construction
- 48-bit ECC Polynomial
- Onboard Advanced Diagnostic Port

ENIVRONMENTAL LIMITS

- Operating
  Temperature: 0°C (32°F) To 55°C (131°F)
  Humidity: 10% To 95% Noncondensing
  MTFB: 20,000 POH at 55C
- Storage
  Temperature: -40°C (-40°F) To 75°C (167°F)
  Humidity: 10% To 95% Noncondensing

PHYSICAL SPECIFICATIONS

The ACB-2610 is designed for an expansion slot of the IBM Personal System/2 Models 50, 60 or 80.

- Length: 11.5 Inches
- Height: 3.5 Inches
- Width: 0.6 Inch

IBM PS/2 Micro Channel Model 50/60 Compatible ST412/506 2,7 RLL Disk Controller

ACB-2670: Micro Channel™ ST412/506 2,7 RLL Disk Controller

Adaptec's ACB-2670 is a highly integrated ST412/506 RLL Winchester disk controller designed for the IBM Personal System/2™ Micro Channel architecture in system models 50, 60, 80 and compatibles. Features such as 1:1 sector interleaving and host DMA transfers of 10 MBytes/second are only a few advantages of Adaptec's ACB-2670, a result of incorporating Adaptec's pioneering VLSI technologies

PROVEN ARCHITECTURE

At the heart of the ACB-2670 is the Adaptec AIC-011, programmable media sequencer, the next generation of the device used in IBM's PS/2 Model 80 ESDI disk controller. The AIC-011 architecture serves as the heart of all of Adaptec's high-performance disk controllers. This device, along with Adaptec's AIC-6225 high-precision bipolar monolithic data separator, give the ACB-2670 the highest RLL reliability and data integrity available.

And to demonstrate Adaptec's commitment to Quality Excellence, we're extending Adaptec's **Limited Lifetime Warranty** to the ACB-2670.

IBM PS/2 COMPATIBLE

ACB-2670 is fully port and register compatible with IBM's Personal System/2 Models 50, 60 and 80. In addition, the ACB-2670 has been thoroughly tested with CHIPS/250, PS/2 Model 50 compatible system logic. The ACB-2670 has been successfully tested with MS-DOS® 3.3, IBM OS/2®, XENIX® and UNIX® operating systems. Compatible manufacturers can take full advantage of software developed for IBM PS/2 systems. And for those developers requiring operating system support, Adaptec is providing I/O drivers for the most popular software, such as OS/2, XENIX, UNIX and Novell Netware™.

HIGH PERFORMANCE

The ACB-2670 is the highest performance Micro Channel ST412/506 RLL disk controller available. With a disk data rate of 7.5 Mbits/second, full track buffering and read-ahead cache, the ACB-2670 maintains 1:1 sector interleaving, while bursting data across the Micro Channel at DMA speeds up to 10 Mbytes/second. We've optimized the ACB-2670 for minimum use of your system's I/O bandwidth. That will leave more time for other I/O intensive operations to occur almost simultaneously, ideal for multitasking, multi-user and multiprocessor applications.

For customers requiriing BIOS compatibility with 26 sectors/track RLL, Adaptec provides a version of the ACB-2670 with a compatible BIOS.

ADVANCED VLSI TECHNOLOGY

The AIC-561 and AIC-562 are the latest additions to Adaptec's family of high performance VLSI controller interface circuits. The AIC-561 implements all the logic necessary to comply with the programmable option select feature and arbitration protocols of the Micro Channel. The AIC-562 integrates the buffer controller and DMA logic enabling the ACB-2670 to achieve DMA transfer rates far superior to the standard IBM disk controller.

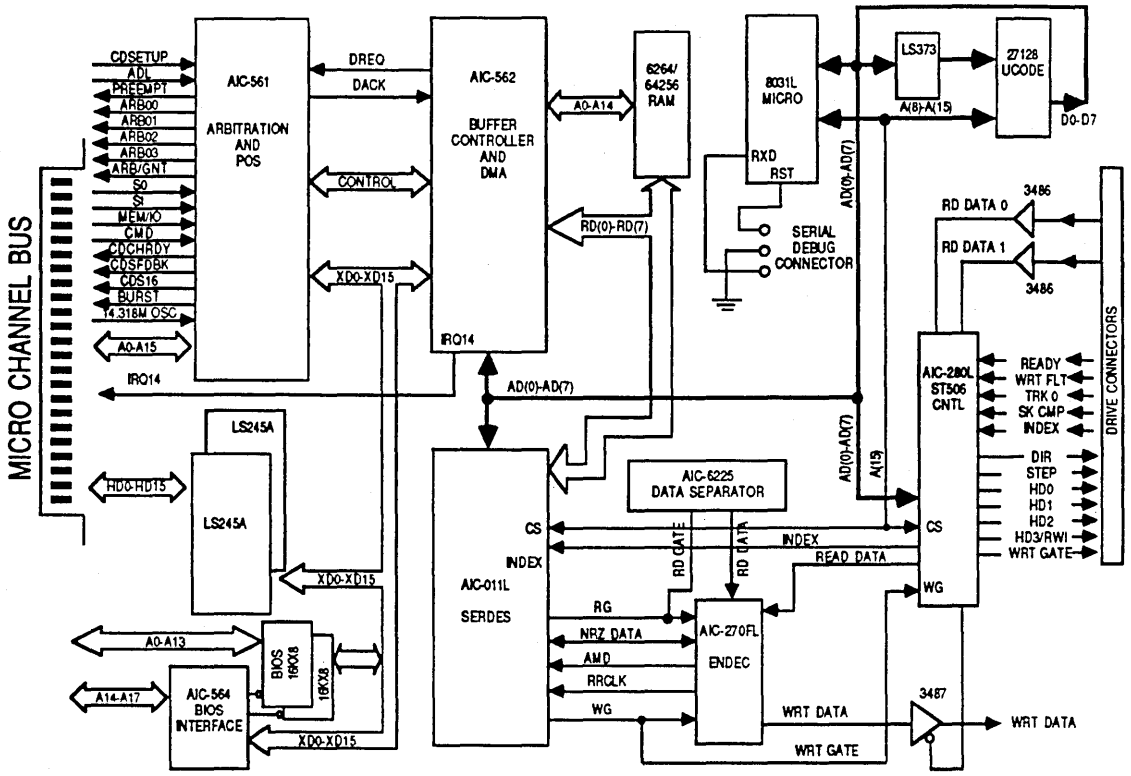
50% MORE CAPACITY

With the ACB-2610 's 2,7 RLL data encoding technology, you get an additional 50% more capacity and throughput with RLL qualified disk drives. And you get confidence in reliability because our encoding scheme is licensed from IBM.

ADVANCE INFORMATION

adaptec, inc. • 580 cottonwood drive • milpitas, ca 95035 • (408) 432-8600

ACB-2670 Block Diagram



FEATURES

- 100% IBM Micro Channel Port And Register Compatible
- Optional Onboard BIOS
- 1:1 Sector Interleaving
- Autoconfiguration
- Supports Two ST412/506 Disk Drives, 4096 Cylinders, 16 Heads
- 2,7 RLL, 7.5 Mbit/Sec Drive Data Rate
- Burst DMA Up To 10 MBytes/Sec Or Programmed I/O Host Transfers
- Optional 8K, 32K, Or 64K Buffer
- Read-Ahead Cache
- High Precision Bipolar Monolithic Data Separator
- Surface Mount Construction
- 48-bit ECC Polynomial
- Onboard Advanced Diagnostic Port

ENIVRONMENTAL LIMITS

- Operating
  Temperature: 0°C (32°F) To 55°C (131°F)
  Humidity: 10% To 95% Noncondensing
  MTBF: 20,000 POH at 55C
- Storage
  Temperature: -40°C (-40°F) To 75°C (167°F)
  Humidity: 10% To 95% Noncondensing

PHYSICAL SPECIFICATIONS

The ACB-2670 is designed for an expansion slot of the IBM Personal System 2 Models 50, 60 or 80.

- Length: 11.5 Inches
- Height: 3.5 Inches
- Width: 0.6 Inch

IBM PS/2 Micro Channel Model 80 Compatible Multitasking ESDI Disk Controller

ACB-26M20: Micro Channel™ Model 80 Compatible Multitasking ESDI Disk Controller

Adaptec's ACB-26M20 is a highly integrated ESDI Winchester disk controller designed for the IBM Personal System/2™ Model 80 Micro Channel and compatibles. Features such as multitasking, 1:1 sector interleaving and host DMA transfers of 10 MBytes/second are only a few advantages of Adaptec's ACB-26M20, a result of incorporating Adatec's pioneering VLSI technologies.

IBM PS/2 COMPATIBLE

ACB-26M20 is fully port and BIOS compatible with IBM's Personal System/2 Models 50, 60 and 80. In addition, the ACB-26M20 has been thoroughly tested with CHIPS/250, PS/2 Model 80 compatible system logic. That means your software will run with no modifications. The ACB-26M20 has been successfully tested with MS-DOS® 3.3, OS/2™, XENIX® and UNIX® operating systems. Compatible manufacturers can take full advantage of software developed for IBM PS/2 systems. And for those developers requiring operating system support, Adaptec is providing I/O drivers for the most popular sofware, such as OS/2, XENIX, UNIX and Novell Netware™.

ADVANCED VLSI TECHNOLOGY

The AIC-583 is the latest addition to Adaptec's family of high performance VLSI controller interface circuits. The AIC-583 integrates the programmable option select feature, arbitration protocols and DMA logic of the Model 80 Micro Channel, enabling the ACB-26M20 to achieve DMA transfer rates far superior to the standard IBM disk controller.

PROVEN ARCHITECTURE

At the heart of the ACB-26M20 is the Adaptec AIC-011, programmable media sequencer, the next generation of the device used in IBM's PS/2 Model 80 ESDI disk controller. The AIC-011 architecture serves as the heart of all of Adaptec's high-performance disk controllers.

And to demonstrate Adaptec's commitment to Quality Excellence, we're extending Adaptec's **Limited Lifetime Warranty** to the ACB-26M20.

HIGH PERFORMANCE

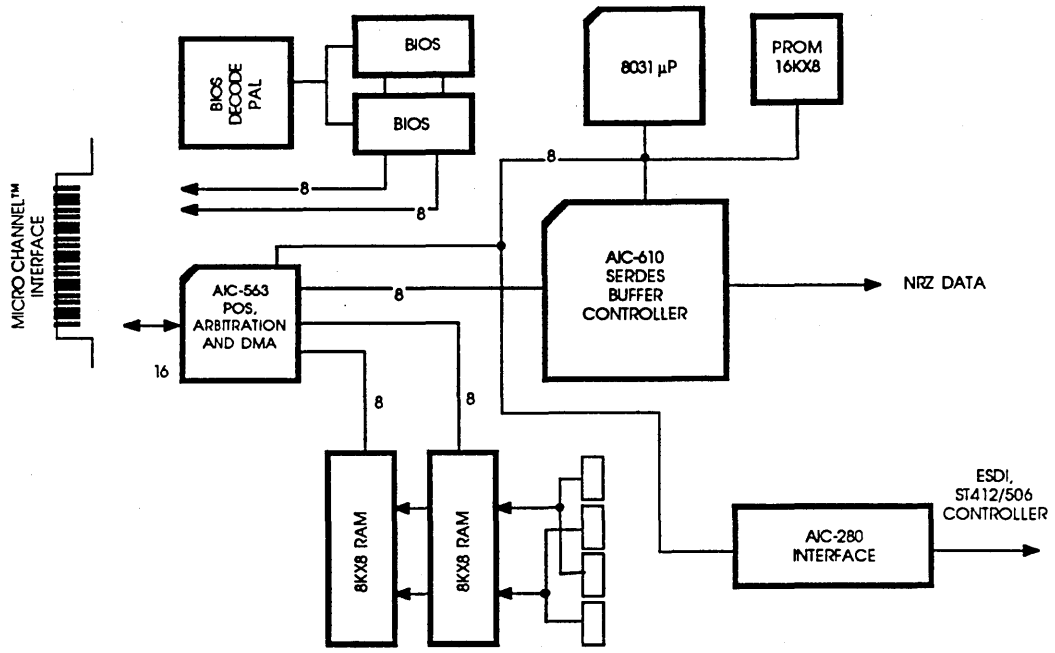
The ACB-26M20 is the highest performance Micro Channel ESDI disk controller available. With a disk data rate of 15 Mbits/second, the ACB-26M20 maintains 1:1 sector interleaving, while bursting data across the Micro Channel at DMA speeds up to 10 Mbytes/second. We've optimized the ACB-26M20 for minimum use of your system's I/O bandwidth. That will leave more time for other I/O intensive operations to occur almost simultaneously, ideal for multitasking, multi-user and multiprocessor applications.

As the recognized industry leader in high-performance multitasking I/O, once again Adaptec has provided its customers with mainframe technology on a PC. The ACB-26M20 is Multitasking. In fact, as many as three tasks may be executed simultaneously. With two ESDI drives attached, users may configure the highest performance workstations and file servers available.

ADVANCE INFORMATION

adaptec, inc. • 580 cottonwood drive • milpitas, ca 95035 • (408) 432-8600

ACB-26M20 Block Diagram



FEATURES

- 100% IBM Micro Channel Port And BIOS Compatible
- Multitasking (Up To 3 Threads)
- Relative Byte Addressing Support
- 1:1 Sector Interleaving
- Supports Two ST412/506 Disk Drives, 4096 Cylinders, 16 Heads
- ESDI, 15 Mbit/Sec Drive Data Rate
- Autoconfiguration
- Burst DMA up to 10 MBytes/Sec or Programmed I/O Host Transfers
- Surface Mount Construction
- 48-bit ECC Polynomial
- Onboard Advanced Diagnostic Port
- Optional 8K, 32K, or 64K Buffer
- Read Ahead Cache

ENIVRONMENTAL LIMITS

- Operating
  Temperature: 0°C (32°F) To 55°C (131°F)
  Humidity: 10% To 95% Noncondensing
  MTBF: 20,000 POH at 55C
- Storage
  Temperature: -40°C (-40°F) To 75°C (167°F)
  Humidity: 10% To 95% Noncondensing

PHYSICAL SPECIFICATIONS

The ACB-26M20 is designed for an expansion slot of the IBM Personal System/2 Models 50, 60 or 80.

- Length: 11.5 Inches
- Height: 3.5 Inches
- Width: 0.6 Inch

PS/2 -To-SCSI Intelligent Host Adapter

AHA-1640: PS/2™-To-SCSI Intelligent Host Adapter

Adaptec's AHA-1640 SCSI Host Adapter meets the I/O performance requirements of the powerful multitasking Micro Channel™-based systems. The extremely high data transfer rate and intelligence of the AHA-1640 provide maximum performance access to a wide variety of SCSI devices in both single- and multitasking environments.

The AHA-1640 offers Micro Channel bus performance up to 8 Mbytes/second, double the usual transfer rate. Bus master control of the Micro Channel reduces the memory contention on the system bus by half. Across the SCSI bus, the AHA-1640 offers the maximum synchronous transfer rate of two Mbytes/second. The high bus bandwidth, low memory interference and powerful multitasking capability make the AHA-1640 Host Adapter ideal for Micro Channel-based computers using powerful 286 and 386 processors in XENIX®, UNIX® and OS/2® environments.

ENHANCE PS/2 PERFORMANCE

Adaptec allows Micro Channel manufacturers to increase system performance by greatly enhancing bus transfer rates and decreasing memory contention.

By implementing Bus Master direct memory access (DMA), the AHA-1640 supports an 8-Mbyte/second bus transfer rate with none of the wasted cycles associated with Slave DMA.

MAXIMIZE HOST PERFORMANCE

A very high-speed microprocessor provides the intelligence that brings the full power and flexibility of SCSI to the host, while minimizing host processing cycles. All SCSI protocol management, all multitasking management, all memory address management, and all error monitoring and recovery functions are performed by the AHA-1640, freeing the host CPU for processing data, rather than monitoring I/O operations.

MAXIMIZE MULTITASKING PERFORMANCE

Adaptec's mailbox architecture provides a simple interface for multitasking operating systems. Up to 255 simultaneous tasks can be activated, optimizing performance for individual systems.

The AHA-1640 supports synchronous and asynchronous peripherals concurrently. It automatically adjusts the data transfer mode without software intervention, allowing easy upgrade to future SCSI devices.

Features such as disconnect/reconnect, command linking, zero latency and queuing are used to full advantage in multitasking systems.

The AHA-1640 is software compatible with previous Adaptec host adapters, particularly the AHA-1540.

VERSATILITY AND FLEXIBILITY

The AHA-1640 emulates a standard disk controller providing easy integration to MS-DOS and OS/2 systems. The AHA-1640 is also supported under the SCO XENIX™ System V™ operating system.

The Host Adapter has been designed to support all CCS Rev 4B SCSI disk drives, allowing ease of integration and a simple upgrade path to SCSI-2 devices.

Using the simple mailbox interface, drivers can be programmed to connect any variety of SCSI devices, including magnetic and optical disks, tapes, printers, scanners and others. In addition, the AHA-1640 can operate simultaneously as a Processor Type SCSI target, allowing the implementation of a powerful Local Computer Network for task-sharing and non-stop computing using multiple Micro Channel systems.

ADVANCE INFORMATION

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SCSI BUS SIGNALS	
DB(0)-DB(7)	DATA BUS
DB(P)	DATA PARITY
I/O	(INPUT/OUTPUT) DATA DIRECTION
C/D	(COMMAND/DATA) DATA TYPE
REQ	(REQUEST) DATA OR COMMAND TRANSFER REQUEST
ACK	(ACKNOWLEDGE) DATA OR COMMAND TRANSFER ACKNOWLEDGE
BSY	(BUSY) BUS BUSY
MSG	(MESSAGE) CONTROLLER/HOST ADAPTER COMMUNICATION
RST	(RESET) RESET ALL CONTROLLERS/ HOST ADAPTERS
SEL	(SELECT) SELECTS OR RESELECTS SCSI DEVICE
ATN	(ATTENTION) MESSAGE REQUEST

HOST ADAPTER COMMANDS	
00	NO OPERATION
01	MAILBOX INITIALIZATION
02	START SCSI COMMAND
03	START BIOS COMMAND
04	ADAPTER INQUIRY
05	ENABLE MAILBOX OUT INTERRUPT
06	SET SELECTION TIMEOUT
07	SET BUS ON TIME
08	SET BUS OFF TIME
09	SET TRANSFER SPEED
OA	RETURN INSTALLED DEVICES
OB	RETURN CONFIGURATION DATA
OC	ENABLE TARGET MODE
1C	WRITE ADAPTER FIFO BUFFER
1D	READ ADAPTER FIFO BUFFER
1F	ECHO COMMAND DATA

FEATURES

- Fast Data Transfer Rates
  - 8.0 Mbytes/Sec On The Micro Channel
  - 2.0 Mbytes/Sec Asynchronous SCSI Data Rate
  - 5.0 Mbytes/Sec Synchronous SCSI Data Rate
- High Performance By Offloading The Host CPU
  - Proprietary Protocol Chip Handles SCSI Protocol
  - Bus Master DMA Implementation
  - Task Scheduling And Message-Based Communication
  - Communication With The Host and SCSI Devices Through Mailbox Architecture
  - 16/8-Bit Host Bus Data Transfer
  - Very Fast Processor Reduces Overhead
- High Performance Through Advanced SCSI Implementation
  - Supports Both Synchronous And Asynchronous Devices Concurrently
  - Fully Multitasking/Multithreading
  - Programmable Number Of Mailboxes Up To A Maximum Of 255
  - Supports Advanced SCSI Features Such As Zero Latency Operation And Linked Commands
  - Supports Processor-Type Target Mode
- Get To Market Fast
  - XENIX/UNIX Drivers Available
  - DOS Driver And BIOS Are Available
  - Controller And Device Independence
  - Full SCSI Compatibility
  - Internal And External SCSI Connectors
  - Standard Micro Channel Host Bus Interface

ENIVRONMENTAL LIMITS

- Operating
  Temperature: 0°C (32°F) To 55°C (131°F)
  Humidity: 10% To 95% Noncondensing
- Storage
  Temperature: -40°C (-40°F) To 75°C (167°F)
  Humidity: 10% To 95% Noncondensing

POWER REQUIREMENTS

- +5 VDC @ 1.6 Amp
  Termination Power Provided

PHYSICAL SPECIFICATIONS

- Length: 12.75 Inches
- Height: 3.5 Inches
- Width: 0.826 Inch
- Weight (Shipping): One Pound

PS/2 Models 25 & 30 And PC/XT & PC/AT SCSI Host Adapters

AHA-1020: PS/2 Models 25 & 30 and PC/XT® & PC/AT®-To-SCSI Host Adapter

Adaptec's AHA-1020 SCSI Host Adapter provides an interface between the IBM PS/2 Models 25 & 30 plus the IBM PC/XT & PC/AT to the industry-standard SCSI interface. This allows for the economical connection of multiple device independent peripherals. Utilizing only one short slot in the host, the Adaptec AHA-1020 features SCSI performance at a minimal cost.

IBM COMPATIBLE

The AHA-1020 plugs into a PS/2 Model 25 and 30 system PC/XT, or PC/AT 8-bit expansion slot. It is command and bus interface compatible. In the PC/XT or PC/AT it can co-reside or replace the existing PC controller board.

LOW COST SCSI SOLUTION

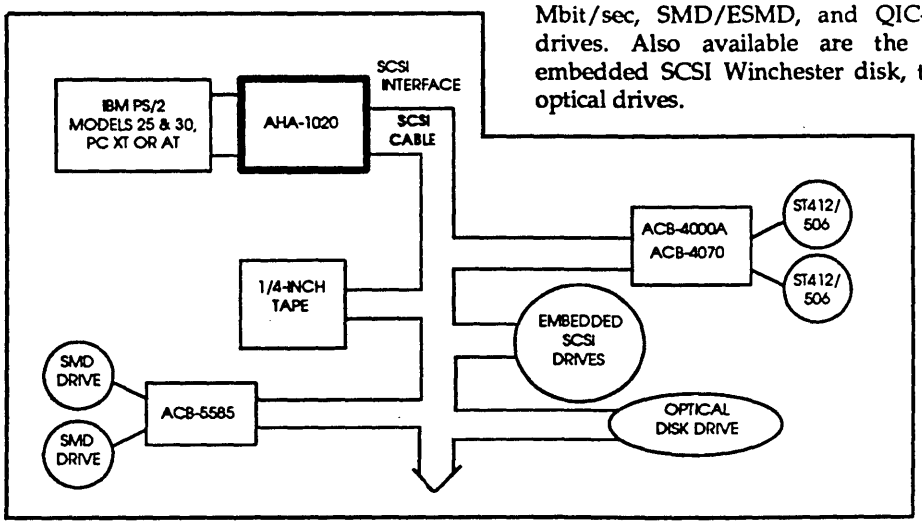
Our new Host Adapter brings a low-cost, high-performance SCSI solution to the IBM PS/2 Models 25 and 30, PC/XT, and PC/AT. The Host Adapter provides the high level of performance needed to optimize the advanced features offered by SCSI devices.

HIGH PERFORMANCE

The AHA-1020 Host Adapter supports an array of additional features available only on Adaptec's high-performance host adapters and controller boards. These features include autoconfiguration, sector level defect handling and a preprogrammed BIOS – all designed to increase system performance and efficiency as well as simplify design-in.

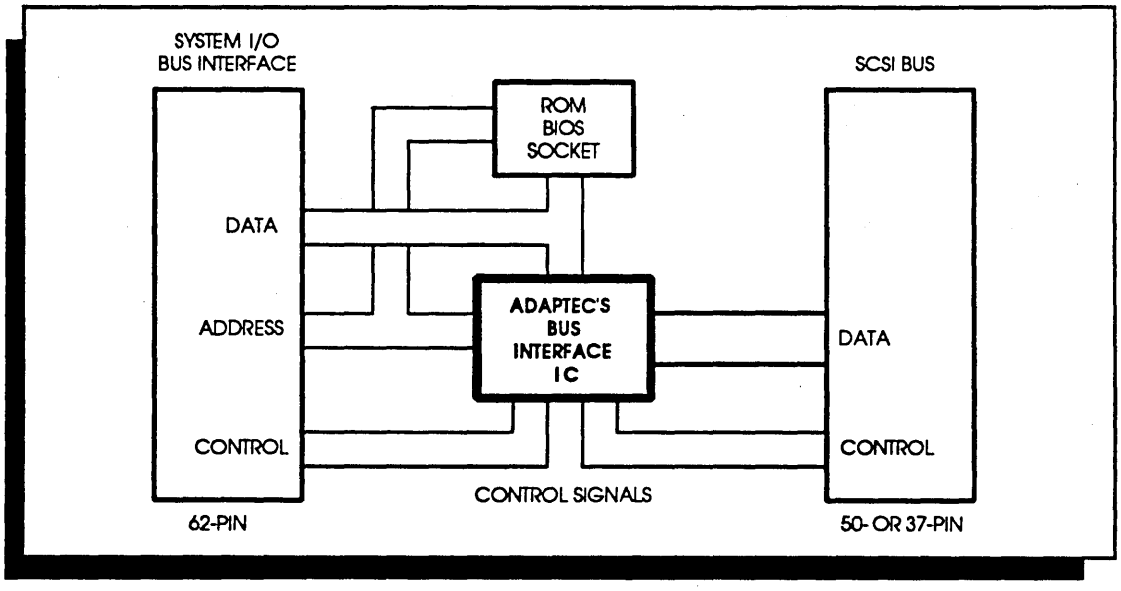
GREATER FLEXIBILITY

By providing SCSI to the PS/2 Models 25 and 30, PC/XT and PC/AT, a variety of peripherals become available through the use of Adaptec's full line of SCSI disk and tape controllers that support ST412/506 in MFM and RLL formats, ESDI 10 and 15 Mbit/sec, SMD/ESMD, and QIC-36 tape drives. Also available are the popular embedded SCSI Winchester disk, tape and optical drives.



Typical SCSI Configuration

ADVANCE INFORMATION



Functional Block Diagram

FEATURES

- High Performance Through Advanced SCSI Implementation
  - Fast DMA 300KB/Sec Transfer
  - Multiprocessing: Up To Seven SCSI Devices
  - 8-Bit Host Data Transfer
- Various SCSI Device Support
  - Adaptec's SCSI Controller Line:
    ACB-4000A MFM ST412/506
    ACB-4070 RLL ST412/506
    ACB-4525 ESDI
    ACB-5580 SMD/ACB-5585 ESMD
  - Embedded SCSI Winchester Disk & Tape
  - Optical Disk Drives
  - Other SCSI Device Interfaces
- Complete PS/2 Models 25 & 30 and IBM PC/XT & PC/AT Compatibility
  - Command Compatible, Accepts IBM BIOS Command Set
- Autoconfigure
  - User-Specified Drive Characteristics
  - Drive Characteristics Loadable From A Batch File
- Adaptec Defect Handling
  - Allows User The Option To Enter Manufacturer's Defect List
- Low Cost & Reliable
  - Two-layer Printed Circuit Card
  - Highly Integrated Componen•
- Half-Slot Size
  - Saves Valuable PC Space
- Internal And External SCSI Connectivity Options
  - Comes Standard With Internal SCSI Connectivity
  - Optional External Connector For Adding SCSI Subsystems

ENVIRONMENTAL LIMITS

- Operating
  Temperature: 0°C (32°F) To 55°C (131°F)
  Humidity: 10% To 95% Noncondensing
- Storage
  Temperature: -40°C (-40°F) To 75°C (167°F)
  Humidity: 10% To 95% Noncondensing

POWER REQUIREMENTS

- +5 VDC @ 0.5 Amp Typical

PHYSICAL SPECIFICATIONS

- Length: 5.50 Inches
- Height: 4.40 Inches
- Width: .75 Inch
- Weight (Shipping): One Pound

SCO

THE SANTA CRUZ OPERATION

SCO XENIX System V Operating System

- Over 5,000 SCO XENIX systems already shipped for PS/2 Models 50/60/80
- Binary compatibility with over 250,000 installed XENIX systems
- Runs DOS programs as a task with SCO VP/ix: co-developed with Phoenix
- Supports CHIPS and Adaptec components
- Custom code for CHIPS, Adaptec, and OEM 'Compatibility Plus' features
- Supports IBM and popular third-party peripherals

SCO XENIX System V Operating System

- SCO XENIX System V for the Personal System/2 and compatibles
- UNIX 5.3 licensed operating system
- Multiuser, multitasking
- Protected 286 mode and demand paged 32-bit virtual memory 386 mode
- Domestic and international versions
- Complete SCO solution including graphics, connectivity and applications

Complete System V Operating System Solution

- SCO XENIX System V Operating System
  - Supports as many users as hardware configuration allows
- SCO XENIX System V Development System
  - Complete with Microsoft C and SCO CGI Graphics Development System
- SCO XENIX System V Text Processing System
  - Text analysis and formatting and intelligent on-line manuals
- SCO XENIX Documenters WorkBench System
  - Advanced typesetting supports many lasers printers

Systems Applications for PS/2's

- SCO VP/ix
  - Run DOS applications transparently under SCO XENIX 386
- SCO MultiView
  - Multitasking windows on console or terminals
- SCO XENIX-Net
  - PC-networks compatible XENIX/XENIX, XENIX/DOS connectivity
- SCO SNA-3270
  - Mainframe communications

SCO Solution

SCO Applications Family

- SCO Professional
  - 1-2-3 workalike
- SCO Foxbase and Foxbase+
  - Dbase II & III workalikes
- SCO Lyrix
  - Advanced word processing
- SCO Masterplan
  - Project planning
- SCO Statistician
  - Advanced statistics
- SCO ImageBuilder
  - Business and presentation graphics

PRESS RELEASE

FOR IMMEDIATE RELEASE

CONTACT:

Zee Zaballos
The Santa Cruz Operation, Inc.
408 425-7222

SCO SHIPS FIRST MULTI-USER OPERATING SYSTEM FOR IBM PS/2

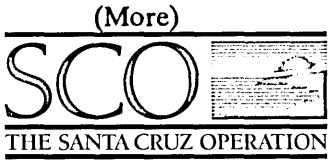
SANTA CRUZ, CA (October 15, 1987) –Responding to heavy demand for a multiuser, multi-tasking operating system for the new IBM Personal System/2™ series of microcomputers, The Santa Cruz Operation, Inc. (SCO) has started shipping versions of its industry-standard SCO XENIX® System V for the PS/2™.

The release of SCO XENIX 286 for the 80286-based PS/2 Models 50 and 60, and SCO XENIX 386 for the 80386-based PS/2 Model 80, represents the first commercial shipment of an operating system designed specificially for the PS/2.

SCO XENIX 286 and SCO XENIX 386 are, respectively, the only operating systems yet available for the IBM PS/2 series to take full advantage of the Intel 80286 and 80386 microprocessors, providing true multiuser and multi-tasking capabilities and using full memory protection. In particular, SCO XENIX 386 runs in native 32-bit, demand-paging virtual memory mode on 80386-based machines such as the PS/2 Model 80.

SCO XENIX System V for the PS/2 series is 100 percent binary compatible with other versions of SCO XENIX System V. 286-based XENIX applications running under SCO XENIX 286 and SCO XENIX 386 on industry-standard machines will run unchanged, without requiring recompilation, on PS/2 Models 50, 60, or 80. Native 386-mode 32-bit programs running on SCO XENIX 386 for industry-standard 386-based computers will run unchanged, without requiring recompilation, on the PS/2 Model 80.

(More)



"Complete compatibility with other versions of XENIX meets our customers' need for easy integration of their new PS/2 systems with other, industry-standard 286- and 386-based XENIX PCs they already have in place," said Doug Michels, vice president of SCO. "Our insistence on making the extra effort to ensure compatibility reflects SCO's commitment to providing the broadest multiuser and multi-tasking capability available from any systems software company."

XENIX System V is a commercially enhanced, unlimited-user- licensed, SVID-conforming version of AT&T's multiuser, multi-tasking UNIX System V Operating System. SCO XENIX System V was cooperatively developed specifically for the microcomputer environment by Microsoft and SCO, who have had an ongoing XENIX technology exchange, development, and marketing agreement since 1982. SCO is Microsoft's exclusive "second source" for packaged XENIX product through OEM, VAR, and other reseller channels. SCO XENIX for the PS/2 was developed primarily by the engineering group at SCO's european office in London.

The Santa Cruz Operation, Inc. is a privately owned, self-funded company recognized internationally as a developer and supplier of premier XENIX and UNIX multiuser business software solutions, training, and support services. Founded in 1979, SCO fields a staff of over five hundred between its Santa Cruz, California, Washington D.C., and London offices, including the largest XENIX technical team in the world.

# # #

(More)

PRICING SCHEDULE

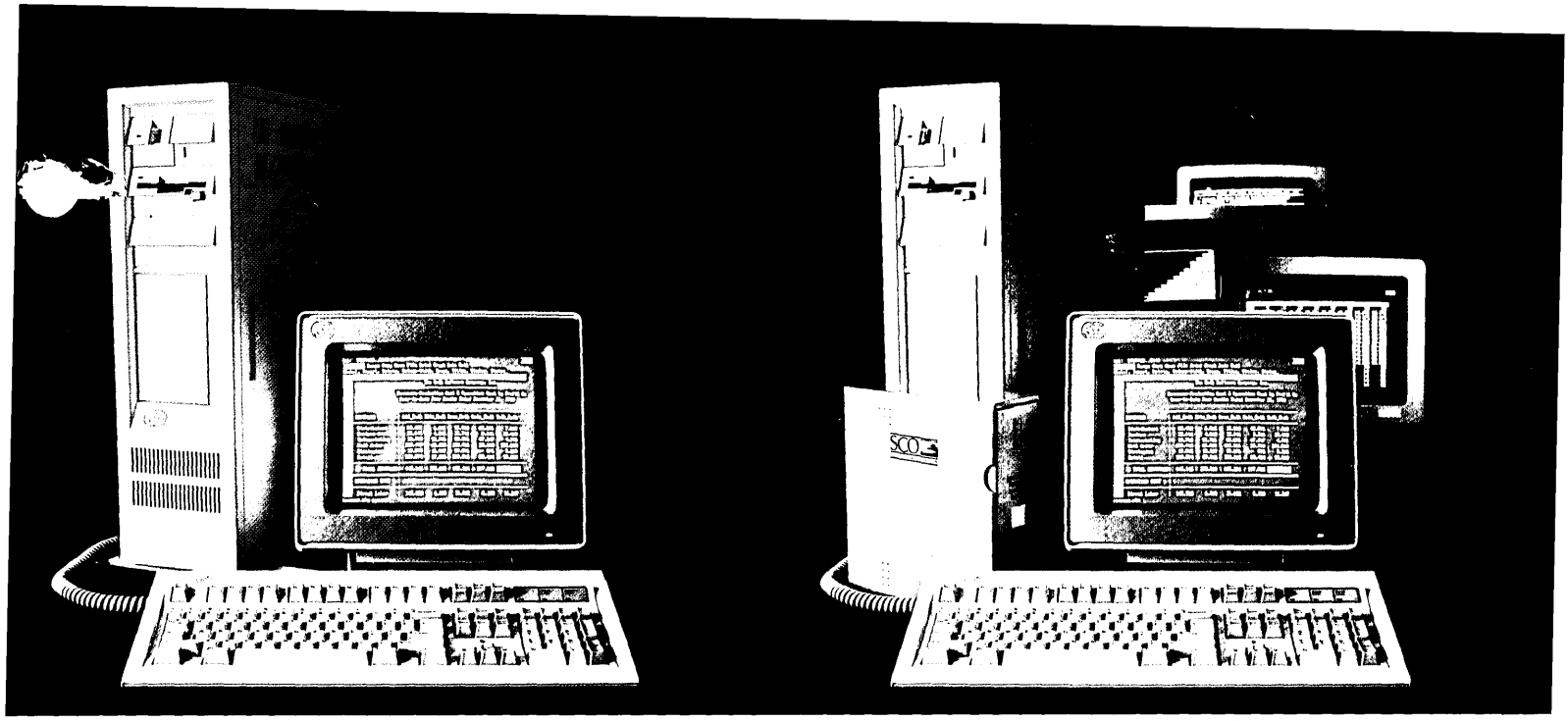
SCO XENIX 286 System V for IBM Personal System/2 Models 50 and 60

Operating System:	$ 695.00
Development System:	$ 695.00
Text Processing System:	$ 195.00
Complete System:	$1495.00

SCO XENIX 386 System V for IBM Personal System/2 Model 80

Operating System:	$ 795.00
Development System:	$ 795.00
Text Processing System:	$ 195.00
Complete System:	$1695.00

All Prices are U.S. Suggested List Prices



DOS system running Lotus 1-2-3

SCO XENIX system running SCO Professional

THIS IS AN IBM PS/2 MODEL 80 RUNNING DOS

Under DOS, this PS/2™ is a powerful 80386-based single-tasking, single-user computer that can run thousands of DOS applications. In 16-bit, 8086 mode.

One at a time.

When OS/2™ becomes available, the PS/2 can become a multitasking, single-user computer running in 16-bit, 286 mode that can utilize DOS applications under OS/2.

One at a time.

With DOS or OS/2, the PS/2 will support one user.

	1 user (DOS)	1 user (OS/2)
Cost per system**:	$12,389	$12,594
Cost per user:	**$12,389**	**$12,594**

THIS IS AN IBM PS/2 MODEL 80 RUNNING SCO XENIX

Under SCO XENIX,® this PS/2 becomes a powerful 80386-based multitasking, multiuser computer that can run thousands of XENIX applications. In full-tilt, 32-bit, 386 mode.

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With SCO XENIX, the PS/2 will support one user. Or 9 users. Or even 33 users.

And it can do all that today because you can get SCO XENIX for the PS/2—*now!*

	1 user	9 users	33 users
Cost per system**:	$14,559	$19,726	$40,402
Cost per user:	**$14,559**	**$2,192**	**$1,224**

SCO XENIX System V and the SCO XENIX family of software solutions are available for all industry-standard 8086-, 80286-, and 80386-based computers, and the IBM® Personal System/2™ Models 50, 60, and 80.

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*SCO VP/ix available as separate product.

**Cost comparisons are based on most recently published U.S. domestic suggested list prices. Cost model: Base machine: IBM PS/2 Model 80, 70Mb disk, 1Mb RAM, IBM 8512 color monitor, 1Mb additional IBM RAM, IBM ProPrinter XL,® 1-user DOS system: Base machine, plus DOS 3.3, WordPerfect 4.2, Lotus® 1-2-3,® dBASE III PLUS® 1-user OS/2 system: 1-user DOS system; substitute OS/2 for DOS. 1-user SCO XENIX system: Base machine, plus SCO XENIX 386 for PS/2, SCO VP/ix, SCO Lyrix® (word processing), SCO FoxBASE+™ (dBASE III PLUS workalike), SCO Professional™ (1-2-3 workalike). 9-user SCO XENIX system: 1-user SCO XENIX system, plus intelligent 8-user multiport card, 8 IBM 3151 ASCII terminals. 33-user SCO XENIX system: 9-user SCO XENIX System, plus 3 more intelligent 8-user multiport cards, 24 more IBM 3151 ASCII terminals, 4 Mb additional RAM, additional 70Mb disk.