CIRRUS LOGIC

PRELIMINARY DATA SHEET

July, 1989

FEATURES

- Direct interface to dual-line, dual panel LCDs
- Full backwards compatibility at the hardware level
- 256 color modes mapped to 32 gray shades on LCD
- Text & graphics scaling to fit LCD resolution
- Programmable for 8 or 16 bit PC bus interface
- Hardware graphics pointer and caret
- Fully compatible with GD510A/520A VGA chipset
- Software selectable support for LCD, Plasma, EL and digital/analog CRT displays
- Intelligent 8/16 bit Video Memory read/write interface from the microprocessor
- Can work with multi-frequency synthesizer IC
- 32 bit non-multiplexed Video Memory interface
- Supports eight 64kx4 or eight 256kx4 DRAMs, or four 128Kx8 pseudo-static RAMs.
- Support for system power down modes
- 16 ICs including RAM for motherboard VGA
- Can share video memory & RAMDAC with graphics coprocessor (eg 34010)
- Advanced low power CMOS technology

CL – GD 610/620

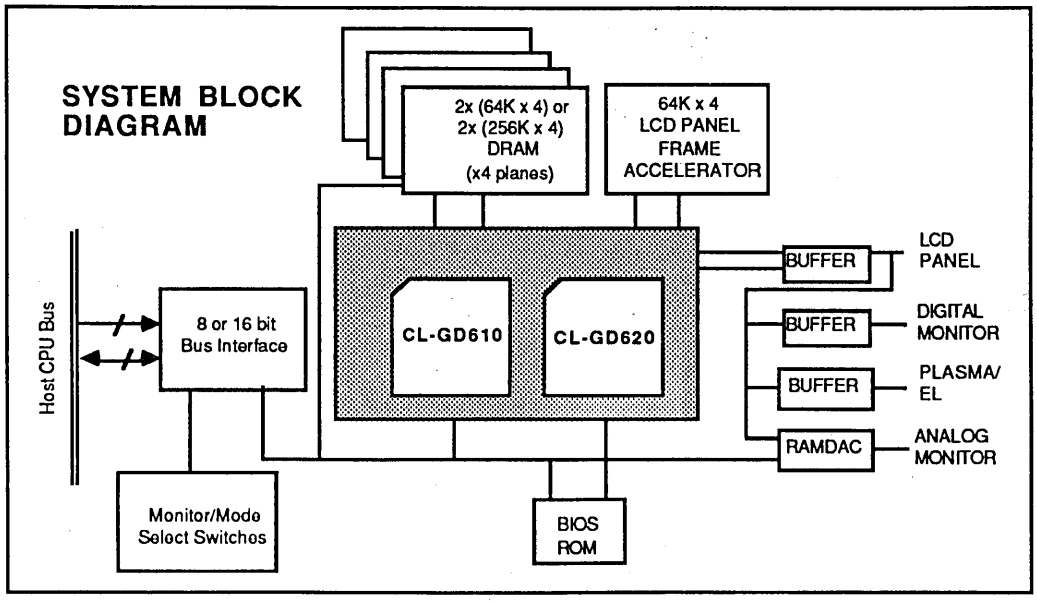
Flat Panel/CRT Enhanced VGA Controller

OVERVIEW

The CL-GD610 Graphics/Attributes chip and the CL-GD620 Sequencer/CRT Controller chip are enhanced versions of the CL-GD510A/520A VGA chipsets and continue to be hardware compatible with the IBM® VGA, EGA, CGA, and MDA standards, as well as with the Hercules® HGC at all levels-register, data path and BIOS. In addition, these chips may be used with a variety of flat panel displays as well as all popular CRT displays (CD, MD, ECD, PS/2, Variable frequency).

Monochrome LCD panels are driven by duty cycle modulation techniques to yield 16 gray scales with no screen flickering or stability problems. In addition, CIRRUS LOGIC's AutoMap™ technique automatically maps 256 colors into as many as 32 shades of gray for CRT quality gray scale emulation. Foreground/background color attributes are remapped automatically for maximum contrast. Expanded Text and Graphics modes provide larger character fonts and the ability to fill a panel (via ratiometrically determined scanline replication) even with low-resolution video modes. If expanded modes are not desired, automatic screen centering is performed. Panning/data compression allows viewing of 720 column modes on 640 column panels.

(cont'd on next page)



314610-001

OVERVIEW (cont'd)

Operating at dot clock rates up to 33 MHz, the CL-GD610/620 chip set supports high resolution graphics and alphanumeric display modes for both monochrome and color, and for high resolution variable frequency and PS/2 monitors. Refresh rates from 60Hz up to 160Hz are available.

CIRRUS LOGIC's proprietary technology provides greater contrast, reduced flicker, and lower power dissipation with dual-line, dual-panel 400 or 480 scanline LCD panels.

Video outputs to CRT displays are provided in 4 bits per pixel (all resolutions) and 8 bits per pixel (256 color modes). Using analog video output and an external palette, selection may be made from 256K colors.

Video outputs to flat panel displays are provided in dual-panel format (4 bits each to upper and lower panels). LCD panels may be directly driven.

Plasma panels may be driven by the CRT video signals. AutoMap™ (256 color to 32 gray scale mapping) will work with gas plasma panels that can support 16 gray shades.

The intelligent 8/16 bit Video Memory Interface detects memory map configurations that place adjacent bytes in adjacent memory locations and automatically configures the chipset as a 16 bit peripheral. 16 bit operation may also be configured by program control.

The CL-GD610/620 implements all control and data registers in the current graphics standards, including those of the 6845 CRT Controller. Flexible register write protect control and the ability to save/restore all registers are both key elements enabling the chipset to be used in a variety of operating system and application environments.

The sequencer design provides more video memory cycles for the CPU during the normal video refresh/display cycle. During display-blanked intervals, ALL memory cycles can be allocated to process CPU memory requests.

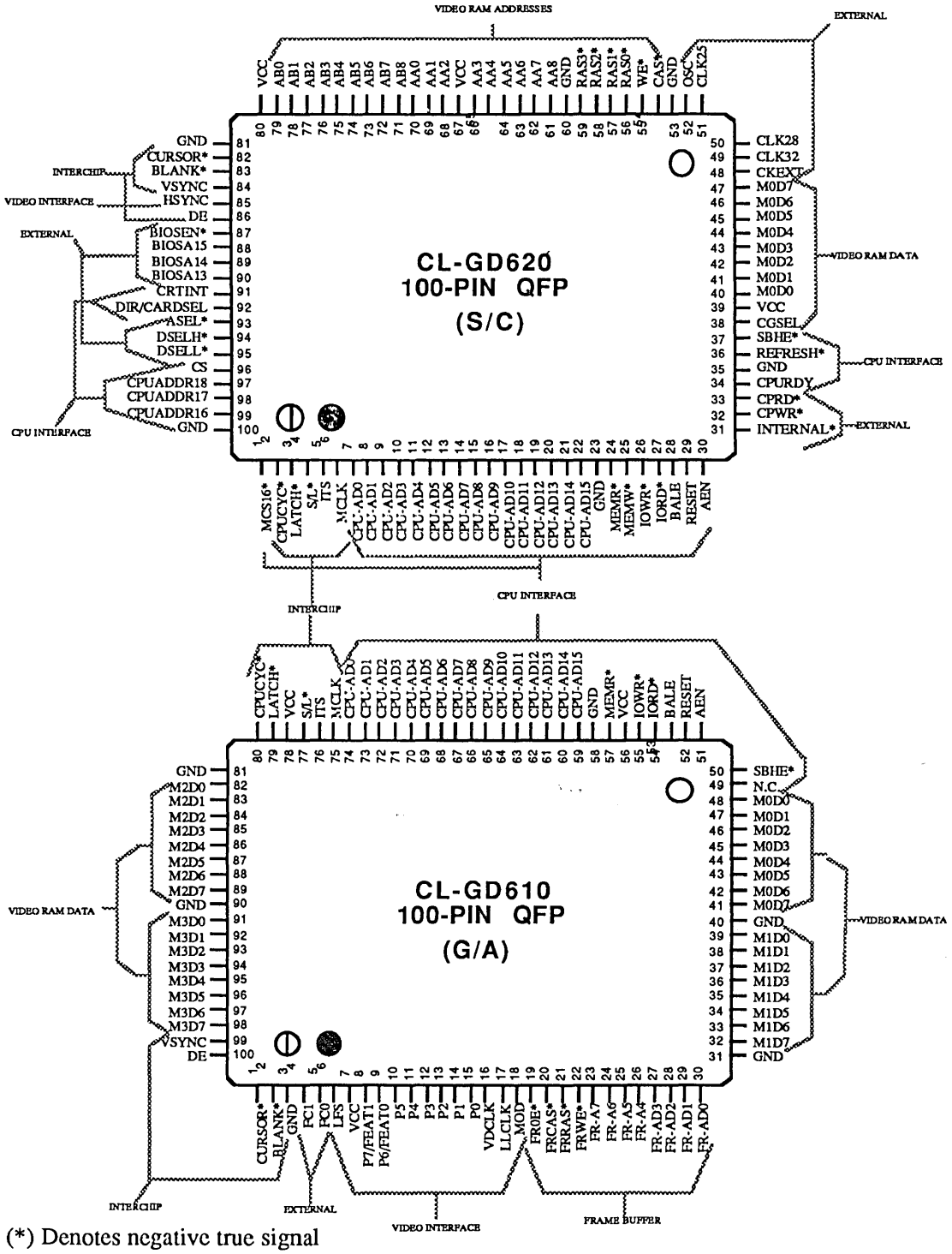
The hardware supports a mouse/graphics cursor, and a blinking insertion point text cursor. Additional text cursor controls include blink disable and replace/invert mode control. The hardware supports simultaneous and independent smooth scrolling of two separate text screens.

The CL-GD610/620 is designed for minimum external circuitry support and is ideal for integrated systems. For example, only 18 chips are necessary for a low-cost controller that can drive both a 640x480 LCD panel as well as a PS/2 monitor. No PALs are required with this dual 100-pin QFP chipset.

Table of Contents

1 PIN INFORMATION

1.1 Pin Diagram



(*) Denotes negative true signal

1.2 Pin Assignment Table

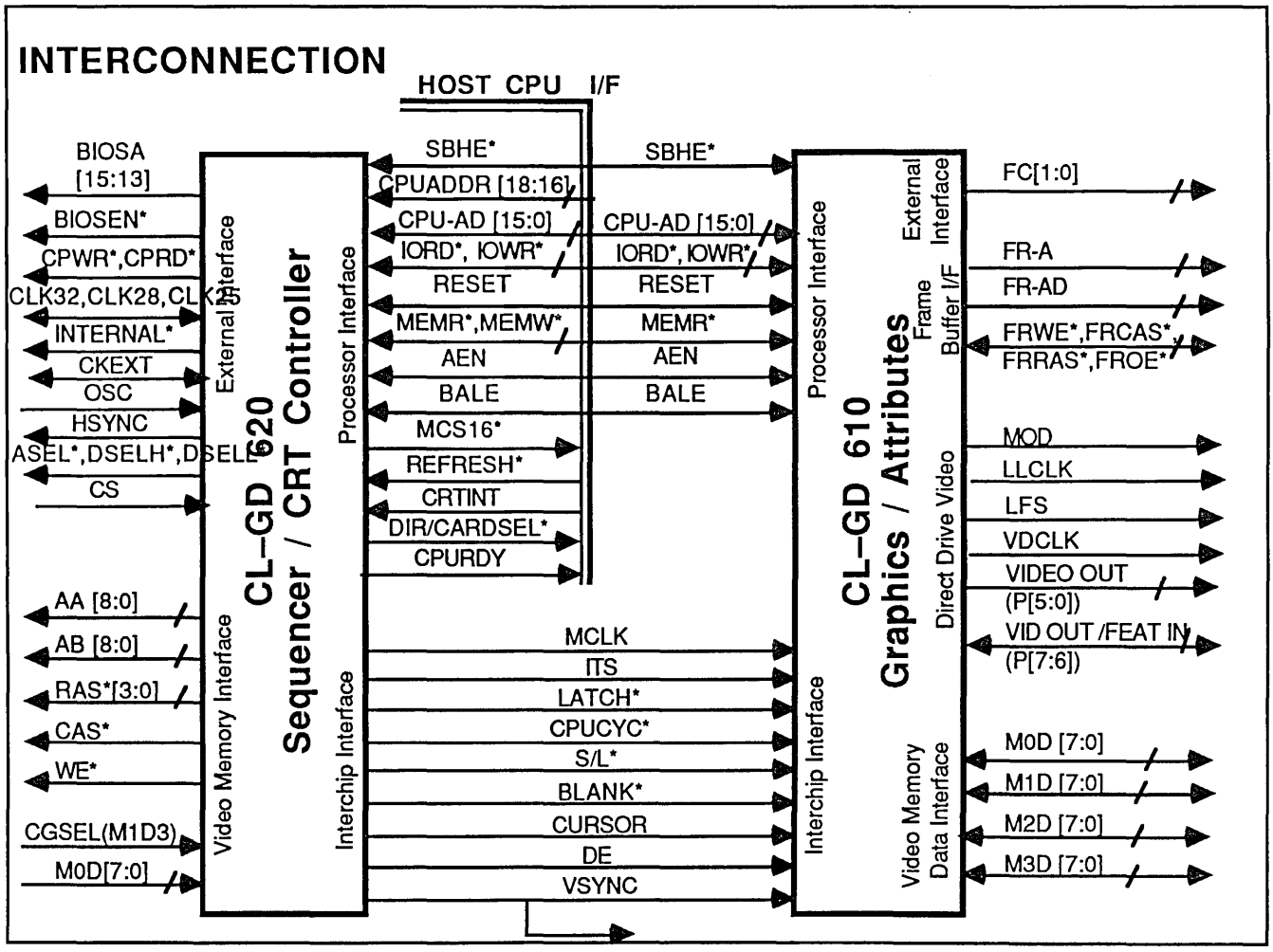
NAME	GD610 PIN NO.	GD620 PIN NO.	TYPE	FUNCTION
PROCESSOR INTERFACE				
SBHE*	50	37	I-T	Bus High Enable from host CPU
AEN	51	30	I-T	DMA vs non-DMA bus cycles)
RESET	52	29	I-T	System Reset
BALE	53	28	I-T	Buffered address latch enable from host CPU
IORD*,IOWR*	54,55	27,26	I-T	I/O R/W Strobes
MEMR*,MEMW*	57	24,25	I-T	CPU read/write of video memory
CPU-AD [15:0]	59-74	7-22	I/O-T	Multiplexed CPU Address/Data/Switch bus
CPUADDR [18:16]		97-99	I-T	Upper 3 address bits from host CPU
CS		96	I-T	Memory decode of LA[23:19]
DIR / CARDSEL*		92	O-T	Bidirectional CPU data bus transceiver control
CRTINT		91	OD	Display retrace interrupt
REFRESH*		36	I-T	System refresh of bus attached RAM
CPURDY		34	OD	Data available signal for wait-state logic
MCS16*		1	OD	16 bit peripheral access acknowledge
VIDEO MEMORY DATA INTERFACE				
M0D[7:0]	41-48	47-40	I/O-T	Byte wide bidirectional data bus to Plane 0
M1D[7:0]	32-39		I/O-T	Byte wide bidirectional data bus to Plane 1
M2D[7:0]	82-89		I/O-T	Byte wide bidirectional data bus to Plane 2
M3D[7:0]	91-98		I/O-T	Byte wide bidirectional data bus to Plane 3
CGSEL (Attr bit 3, M1D3)		38	I-T	Selects alpha map
VIDEO MEMORY ADDRESS INTERFACE				
CAS*		54	O-T	Column address strobe to all planes
WE*		55	O-T	Video memory write enable
RAS[3:0]*		56-59	O-T	Row address strobe to planes 3-0
AA[8:0]		61-66, 68-70	O-T	Address bus to byte planes 0 and 1
AB[8:0]		71-79	O-T	Address bus to byte planes 2 and 3
EXTERNAL INTERFACE				
INTERNAL*		31	O-T	Selects internal vs. external video drivers.
CPWR*, CPRD*		32,33	O-T	Color Palette write/read
CKEXT		48	I/O-T	Input from ext clock (feat conn) or output to LCD panel
CLK32, CLK28, CLK25		49-51	I/O-T	Programmable pins, either clock select or clock inputs
OSC		52	I-T	Oscillator input, MUST be connected to a clock
BIOSEN*		87	O-T	BIOS ROM output enable select
BIOSA [15:13]		88-90	O-T	BIOS page select (for 27C512 devices)
ASEL*, DSELH*, DSELL*		93-95	O-T	Address and data select (low and high byte) enables
FC [1:0]	4,5		O-T	Programmable, normally drive feature connector
GD610 / 620 INTERCONNECT				
CURSOR*	1	82	GD620 to GD610-C	Cursor valid signal
BLANK*	2	83	GD620 to GD610-C	Video blanking signal
MCLK	75	6	GD620 to GD610-C	Master clock
ITS	76	5	GD620 to GD610-C	Interchip timing strobe
S/L*	77	4	GD620 to GD610-C	Syncs loading shift registers with CRTC char clock
LATCH*	79	3	GD620 to GD610-C	Latches video RAM data on CPU or CRT reads
CPUCYC*	80	2	GD620 to GD610-C	Indicates CPU read/write cycle to display memory
VSYNC	99	84	GD620 to GD610-C	Vertical Sync signal
DE	100	86	GD620 to GD610-C	Display enable

VIDEO INTERFACE				Analog	ECD	CD	MD	LCD
LFS	6	O-C	LCD Frame Start					
P7/FEAT1	8	I/O-C	Pixel Data MSB / Feature Bit 1	P7				UD3
P6/FEAT0	9	I/O-C	Pixel Data 6 / Feature Bit 0	P6				UD2
P5/SR	10	O-C	Pixel Data 5 / Secondary Red	P5	SR			UD1
P4/SG/I	11	O-C	Pixel Data 4 / Second. Gr. / Intens	P4	SG	I	I	UD0
P3/SB/V	12	O-C	Pixel Data 3 / Second.Blue / Video	P3	SB		V	LD3
P2/R	13	O-C	Pixel Data 2 / Primary Red	P2	R	R		LD2
P1/G	14	O-C	Pixel Data 1 / Primary Green	P1	G	G		LD1
P0/B	15	O-C	Pixel Data LSB / Primary Blue	P0	B	B		LD0

1.2 Pin Assignment Table (cont'd)

NAME	PIN NO.	GD610 PIN NO.	GD620 TYPE	FUNCTION
VDCLK	16		O-C	Video Data Clock
LLCLK	17		O-C	LCD Line clock
MOD	18		O-C	LCD Modulation output
HSYNC		70	O-T	Horizontal Sync output
BUFFER MEMORY ADDRESS INTERFACE				
FROE*	19		O-T	Buffer Output Enable
FRCAS*	20		O-T	Buffer CAS*
FRRAS*	21		O-T	Buffer RAS*
FRWE*	22		O-T	Buffer Write Enable
FR-A[7:4]	23-26		O-T	Upper 4 bits of Buffer address
FR-AD[3:0]	27-30		I/O-T	Multiplexed Buffer Address/Data

Note: Under the TYPE column, T-> TTL pad, C-> CMOS pad



2 DETAILED SIGNAL DESCRIPTION

2.1 Processor Interface

NAME	GD610	GD620	DESCRIPTION
SBHE*	INPUT	INPUT	Host CPU System Byte High Enable. This signal is sampled only if the 16-bit mode is enabled (3C5 index C7:0), otherwise 8-bit bus operations are assumed. 16-bit mode is only for video memory access. I/O port accesses are always 8-bit.
CPUADDR [18:16]		INPUT	The GD620 uses 3 upper address bits from the host CPU along with CPU-AD and CS for all decoding.
CPU-AD[15:0]	I/O	I/O	Bi-directional multiplexed address/data bus between the CPU and the chip set for video RAM addresses, I/O and switch data .
CS		INPUT	Memory Input, decoded from LA[23:19} for low 1Mbyte operation.
CPURDY		OUTPUT	This signal is inactive (tri-state) when no video memory request is pending. The request may be either MEMR* or MEMW*. At the beginning of a host CPU access to video memory, CPURDY drops low, putting the host CPU in a wait-state. This condition is held until the video memory sequencer fits the memory request into the next available "slot". At completion of the sequencers' host CPU memory cycle, CPURDY is driven high until MEMR* and MEMW* go inactive and then returns to the tri-state condition.
CRTINT		OUTPUT	This signal is enabled by clearing Bit 5 of the Vertical Retrace End Register and cleared by resetting Bit 4 of the Vertical Retrace End Register. When enabled, the CRTINT pin will go high at the start of the vertical retrace interval and remain high until cleared by a write of "0"to Bit 4 of the Vertical Retrace End Register (CR11). CRTINT is enabled by: •Clearing bit 5 of CR11 • Setting bit 4 of CR11 If bit 4 is not reset to a "1" after clearing the initial CRTINT , interrupts will cease. The CR11 of the GD620 is also readable. This feature simplifies greatly the task of ORing in the proper value for the remaining bits of the CR11 register (this is not the case for an IBM-EGA or VGA controller). This Display Retrace Interrupt may be programmed for the AT Bus, or a direct interrupt controller interface.
DIR/CARDSEL*		OUTPUT	Controls the direction of the data flow on the bi-directional CPUDATA bus. Driven low when the CPU is performing an I/O or memory read cycle. This signal can also be used for PC XT slot-8 control.

(*) Denotes negative true signal.

2.1 Processor Interface (cont'd)

NAME	GD610	GD620	DESCRIPTION
IORD*,IOWR*	INPUT	INPUT	When low, these signals indicate that an IORD* or IOWR*cycle is taking place. The GD610/620 will respond only if CS is also active and the proper I/O port addresses have been decoded internally, and if not in the sleep mode.
RESET	INPUT	INPUT	This input is normally connected to the system reset bus signal and is used as a hardware reset of the GD610/620 chips. The GD620 may be partially reset via software by clearing SR0-bit 0 or 1. The falling edge of RESET* latches the data bus into switch registers to control S/W selectable functions. Two pins, CPU-AD15,14 control H/W options at this time.
REFRESH*		INPUT	Indicates host system refresh of bus attached main memory and tells GD620 to ignore memory addresses on the bus.
AEN		INPUT	Host CPU bus signal that distinguishes between DMA and non-DMA bus cycles. The signal is high for a DMA cycle.
BALE		INPUT	Host CPU bus buffered address latch enable signal. High indicates a valid memory address.
MCS16*		OUTPUT	This output is an acknowledge for 16-bit wide accesses and is generated by the GD620 only if the 16-bit peripheral mode is enabled and a valid memory address range has been decoded. It may be generated by a full internal decode (LA16:23, SA15:14), a partial internal decode (without SA15) or with external decoding for fastest response time.
MEMR*/W*	INPUT	INPUT	Video memory read and write strobes. These inputs are driven INPUT low on all CPU memory read/write accesses. Video memory will be accessed if the GD610/620 chipset internal address decoders determine that the partial decode of the MSB addresses of the CPU address bus lies in the AxxxxH or BxxxxH range. The GD610 chip is not connected to MEMW* signal. It decodes this operation if a valid CPU cycle is in progress, (CPUCYC*=0) and a read is not occurring (MEMR*=1).

(*) Denotes negative true signal.

2.2 Video Memory Interface

NAME	GD610	GD620	DESCRIPTION
AA [8:0]		OUTPUT	Multiplexed video memory address bus A. This bus contains the row/column address information required by the DRAMS in the video memory for memory planes 0 and 1. The GD610/620 chipset may be programmed to support 64Kx4 or 256Kx4 DRAMs (256KB or 1MB total video memory). This bus carries different addresses than AB in text modes.
AB [8:0]		OUTPUT	Multiplexed video memory address bus B. This bus contains the row/column address information required by the DRAMS in the video memory for memory planes 2 and 3. The GD610/620 chipset may be programmed to support 64Kx4 or 256Kx4 DRAMs (256KB or 1MB total video memory). This bus carries different addresses than AA in text modes.
CAS*		OUTPUT	Video memory DRAM column address strobe. A low going edge on this signal latches the column address (contained on the AA and AB address busses) into video memory.
CGSEL		INPUT	Enabled by the sequencer character map select register, this bit (normally connected to M1D3 of the attribute memory plane in text mode) can be used to access 1 of 16 secondary character sets (instead of the normal intensity function), to give a total of 512 active display characters from a total of 4096.
M3D [7:0]	I/O		This bi-directional video memory data bus is controlled by the GD610 for read/write operations into video memory Plane 3 which stores graphic data for color plane #3, and eight extra alternate fonts in text modes.
M2D [7:0]	I/O		This bi-directional video memory data bus is controlled by the GD610 for read/write operations into video memory Plane 2 which stores graphic data for color plane #2 or character generator font tables in the text modes.
M1D [7:0]	I/O		Bi-directional video memory data bus controlled by GD610 for read/write operations into video memory Plane 1 which stores graphic data for color plane #1 or attribute codes in text modes.
M0D [7:0]	I/O	INPUT	This bi-directional video memory data bus is controlled by the GD610 for read/write operations into video memory Plane 0 which stores graphic data for color plane #0 or attribute codes in the text modes. The GD620 uses these character codes in text mode to produce the proper address on the memory AB bus to access the character generator fonts.
RAS [3:0]*		OUTPUT	Video memory DRAM row address strobes. A low going edge on these signals latch the row address (contained on the AA and AB address busses) into the video memory DRAMs.
WE*		OUTPUT	When low, this signal enables a video memory write to the bank selected by the appropriate RAS* signal(s). The actual write occurs on the falling edge of CAS*.

(*) Denotes negative true signal.

2.3 Video Interface

The PIXEL DATA bits drive the analog or digital inputs of color or monochrome displays. When driving dual-line LCD panels, P4-P7 drive the upper panel data inputs, and P0-P3 drive the lower panel data inputs. P0-P7 pins are described more fully in the following table:

NAME	DESCR.	Analog RAM DAC Interface	ECD 64-Color Digital	CD 16-Color Digital	MD Mono-chrome	LCD	GD610
P7 / FEAT1	Tertiary Red Feature Bit 1†	P7	0	0	0	UD3	OUTPUT INPUT
P6 / FEAT0	Tertiary Green Feature Bit 0†	P6	0	0	0	UD2	OUTPUT INPUT
P5 / SR	Secondary Red	P5	SR	I	Note	UD1	OUTPUT
P4 / SG / I	Secondary Green/ Intensity	P4	SG	I	Note	UD0	OUTPUT
P3 / SB / V	Secondary Blue/ Video	P3	SB	I	Note	LD3	OUTPUT
P2 / R	Primary Red	P2	R	R	Note	LD2	OUTPUT
P1 / G	Primary Green	P1	G	G	Note	LD1	OUTPUT
P0 / B	Primary Blue	P0	B	B	Note	LD0	OUTPUT

† FEAT1 and FEAT0 (Feature Bits 1 and 0) are programmable as inputs to the FC Register (Feature Control), and can be read at port address 3CA.

Note:
In Monochrome modes, video outputs are driven from GD610 Palette Registers 0, 7, 8, 15 as follows:

Intensity	Video	Palette Register Selected	Mode
0	0	0	Mono Text or HGC Graphics
0	1	7	Mono Text or HGC Graphics
1	0	8	Mono Text Only
1	1	15	Mono Text Only

Intensity = Text mode attribute byte bit 3
Video = Normal output to the monochrome display

NAME	GD610	GD620	DESCRIPTION
MOD	OUTPUT		Used to prevent DC polarization of LCD. MOD changes polarity at least once per frame period. Some panels generate randomized alternating signals derived from LLCLK to perform this function, and may not need this signal. Its pulse width is programmable. The period is twice the number of line clocks written to register 3C5:D9

2.3 Video Interface (cont'd)

NAME	GD610	GD620	DESCRIPTION
LLCLK	OUTPUT		The LCD line clock is used to latch column segment data into the horizontal shift registers. 4 bits of data for the upper panel, and 4 bits of data for the lower panel are simultaneously latched by this signal, for two corresponding scanlines.
VDCLK	OUTPUT		The Video clock is used to clock data through the horizontal shift registers. This signal should be used for all video timing purposes. It is used as a shift clock in LCD mode, and a pixel clock in CRT modes.
LFS	OUTPUT		LCD Frame Start pulse that indicates the start of a new frame, resetting horizontal and vertical logic to the first nibble of the first (of top and bottom panel) scanline.
HSYNC		OUTPUT	Horizontal Sync. The active polarity of this signal can be selected by bit 6 of the miscellaneous output register (I/O address 3C2hex) or bit 6 of the timing control register (extension address 85H).
VSYNC	INPUT	OUTPUT	Vertical Sync. The active polarity of this signal can be selected by bit 7 of the miscellaneous output register (I/O address 3C2H) or bit 7 of the timing control register (extension address 85H).

2.4 External Interface

NAME	GD610	GD620	DESCRIPTION
BIOSA[15:13]		OUTPUT	These 3 pins select one of the five 8kbyte pages mapped into the lower 8kbyte of the 32kbyte BIOS address space, allowing a 64kbyte ROM to be used in this 32kbyte space.
OSC		INPUT	Oscillator input which MUST be connected to a clock, typically the 14.318 MHz clock from the system bus.
CLK32,CLK28,CLK25		I/O	These pins are configured as inputs or outputs based on the state of CPU-AD14 latched from the bus on the falling edge of RESET*. They may be driven from crystal oscillators to provide 32.514, 28.332, and 25.172 MHz inputs to the GD620's internal mux (a 16.257 MHz clock, when required, is internally generated). When configured as outputs, they provide select signals to an external PLL-based multi-frequency synthesizer circuit.
CKEXT		I/O	External clock input, typically from the feature connector, or used for LCD clock requirements.
CPWR*,CPRD*			OUTPUT Color Palette write/read strobes. These pins are active when valid I/O reads or writes to port addresses xC6-xC9H are decoded.

2.4 External Interface (cont'd)

NAME	GD610	GD620	DESCRIPTION
FC[1:0]	OUTPUT		General-purpose programmable output pins, normally used to drive the feature connector. Can be used to enable/disable battery-save modes for low-power laptop PC applications. These bits may be write-protected with WRC bit 6.
INTERNAL*		OUTPUT	Programmable output pin,normally driving tri-state control pins of video drivers for internal or external (feature connector) video operation in CRT mode. This disables external driver in LCD mode. MISC reg bit 4 controls this pin.
BIOSEN*		OUTPUT	This signal is typically connected to a ROM BIOS's OE* input. It enables the BIOS ROM's outputs if a memory address in the C0000H-CFFFFH range has been decoded and ROM control register bit 7 is cleared. This pin will not activate if the BIOS resides on the 'CPU' side of the address/data muxes as indicated by a low state of CPU-AD15 latched from the bus during the falling edge of RESET.
ASEL*,DSELH*,DSELL*		OUTPUT	Address and data select (high and low byte) enables.

2.5 CL-GD610 / 620 Interconnect Signals

NAME	GD610	GD620	DESCRIPTION
BLANK* /DE	INPUT	OUTPUT	CRT Video Blanking signal and Display Enable signal. These signals function as follows:

LCD BLANK*	CRT BLANK*	CRT/LCD DE	FUNCTION
dont care	0	–	OFF (Screen is black)
dont care	1	0	Border display
dont care	1	1	Active Screen

CPUCYC*	INPUT	OUTPUT	Active low during an actual CPU Video RAM read or write cycles. This signal brackets the LATCH* signal during a read operation. The GD610 also uses this signal to differentiate between CPU and CRT write cycles.
CURSOR*	INPUT	OUTPUT	Active during valid cursor position.
ITS	INPUT	OUTPUT	Interchip Timing Strobe. This signal is in a critical timing path. Loading on this pin and the S/L* pin must be the same.
MCLK	INPUT	OUTPUT	Derived from the currently selected clock, this is the master clock used to produce all of the signals in the GD610/GD620.
LATCH*	INPUT	OUTPUT	Latches data to and from the video RAM in the GD610.
S/L*	INPUT	OUTPUT	Shift / Load. Synchronizes the loading of the shift registers in the GD610. This signal is in a critical timing path. Loading on this pin and the ITS pin must be the same.
VSYNC	INPUT	OUTPUT	See description under video interface.

2.6 LCD Display Frame Buffer Interface Signals

NAME	GD610	GD620	DESCRIPTION
FR-A[7:4]	OUTPUT		Upper four bits of frame buffer address
FR-AD[3:0]	I/O		Multiplexed frame buffer address/data
FRWE*	OUTPUT		Buffer write enable
FROE*	OUTPUT		Buffer output enable
FRCAS*	OUTPUT		Buffer CAS*
FRRAS*	OUTPUT		Buffer RAS*

(*) Denotes negative true signal.

3 FUNCTIONAL DESCRIPTION

3.1 Functional Operation

The CIRRUS LOGIC GD610 Graphics/ Attributes chip and CIRRUS LOGIC GD620 Sequencer/CRT Controller chip are tightly coupled and interface with the host processor, video memory, the display device and other external I/O.

The host interface may be 8 or 16 bits wide, under program control. Register LCDCNTL3 is provided to switch bus sizes.
Video memory may be 256Kbytes or 1Mbyte of DRAM.

The display device is typically a 640 by 400/480 line LCD (or other flat panel type) but all standard TTL and analog CRT monitors are supported as well.

The four major operations supported by the CL-GD610/620 are:

- Host access to CL-GD610/620 registers
- Host access to video memory
- Memory refresh
- Display access to video memory

Host Access to Registers

The host (typically an 8088/80286/80386 processor in an IBM PC/XT/AT bus compatible environment) can access CL-GD610/620 registers by setting up 24 bit addresses and generating IOR* / IOW* / MEMR* / MEMW* signals to read or write 8-bit or 16-bit data.

DRAM and screen refresh activities occur concurrently and independently (unless display parameters are being changed by the host CPU's actions on CL-GD610/620 registers).

The registers that may be accessed by the host are listed in sections 4 and 5. They include the registers of the IBM VGA, EGA, CGA, MDA, and Hercules HGC, including those of the 6845 CRT controller. Non-VGA registers have also been made host-readable and writable in order to allow BIOS and driver software to determine the state of the graphics adapter. The state may thus be readily switched and restored in multi-tasking and windowing environments. These so-called extension registers provide the numerous enhancements to the basic VGA function listed in the features/benefits section.

Host access to video memory is channelled via the CL-GD610/620. The host must set up the proper address/data/timing parameters in CL-GD610/620 registers, then handshake with the CL-GD610/620 in order to connect the host data bus to one of the 4 video memory byte plane buses. For example, consider VGA/EGA operation:

Byte planes 0 and 1 share address bus A; planes 2 and 3 share the address bus B. The GD620 Sequencer/CRT Controller chip takes 17-bit addresses from the host, and transforms them according to the selected addressing mode and address space mappings, finally issuing multiplexed addresses to the different planes via the A and B address buses. The CAS* signal, four RAS* signals, and WE* are also generated.

Note that the GD620 Sequencer/CRT Controller chip also contains an intelligent address sequencer that allocates video memory cycles not only to the host, as just described, but also to the DRAM refresh controller and the display CRT controller.

Memory Refresh

Memory bandwidth is allocated to each process according to the actual realtime needs of the process, ensuring efficient use of the available bandwidth. In the case of a CRT display device, the display is blanked during horizontal and vertical retrace intervals, freeing up memory bandwidth for host access and/or memory refresh.

The CL-GD610/620, unlike early VGA implementations that gave the host only 14% of memory cycles, can give the host from 25-50% access to video memory (1 out of 2 memory cycles), largely due to the sequencing strategy.

Display Access to Video Memory

The GD620 Sequencer/CRT Controller chip works very closely with the GD610 Graphics/Attributes chip in all video modes, as the GD610 actually contains the video memory data interface as well as the video outputs to the display device. Thus the

display data is latched in the GD610 after the GD620 determines where it is. Note that due to the 32-bit memory data interface, character data and attribute data can be pipelined. The GD610 contains the video shift registers to interface to the display device. The GD620 works with the GD610 in order to fetch scan line data from the font bitmaps, separately controlling the A and B address buses.

Foreground and background attributes are specified for each character in alphanumeric mode. Cursors and borders are also controlled by the GD610 in alpha modes.

In bit-mapped graphics (All Points Addressable) modes, pixel data is latched into the GD610 Graphics/Attributes chip, transferred to shift registers, and shifted out upon translation through the color palette registers, which are also contained in the GD610.

The GD620 Sequencer/CRT Controller chip supplies a clock (ITS) to the GD610 Graphics/Attributes chip, as well as display memory read strobe (LATCH*), CPU read/write cycle (CPUCYC*), and shift register load (S/L*).

The GD620 Sequencer/CRT Controller chip keeps track of the active and unused areas of the screen and cursor positions and consequently supplies screen control signals (VSYNC, BLANK, Display Enable DE, and CURSOR) to the GD610 Graphics/ Attributes chip.

When the GD610/620 are interfaced to an LCD display, an additional 64Kx4 DRAM is needed. This device is used by the chipset to accelerate panel refresh without using high-frequency clocks, thus reducing power, and, allowing vertical refresh rates from 60Hz to 160Hz for improved contrast and freedom from flicker.

3.2 CRT Display Compatibility Modes

The CL-GD610/620 includes all registers and data paths required for VGA/EGA, CGA, MDA, and HGC controllers. VGA enhancements to baseline EGA functionality include 320x200 eight-bit/pixel mode and support for an external color palette, 16 (double IBM's capability) simultaneously loadable text fonts, write mode 3, and readable registers.
These devices provide support for new extended resolution display modes with CRT displays.

Extended graphics resolutions beyond the 640x480 IBM VGA standard are available using either multiple frequency monitors such as the NEC MultiSync™ or Sony MultiScan™ \ or single frequency PS/2 monitors such as the IBM 8514. These include a 720 x 540 mode which has a 4:3 aspect ratio (square pixels on typical monitors). This mode is supported on both PS/2 monitors as well as multi-frequency displays. In addition there is an 800 x 600 mode which has a 4:3 aspect ratio (the same as 640 x 480 and 720 x 540). This mode requires a multi-frequency display. There are also high resolution text modes from 100 columns by 30 rows up to 132 columns by 60 rows.

Additional 256 color modes (besides IBM mode 13) are available in the chipset and the Cirrus Logic BIOS supports these as well.

The chip set also supports an extended mode 13 where 4 (256Kb RAM) or 16 (1Mb RAM) pages of 64K blocks of memory can be switched and displayed instead of the IBM VGA's single page. This will allow for animation using 256 displayable colors without requiring a large amount of data to be manipulated (64K maximum size per image).

3.3 Flat Panel Display Compatibility Modes

The GD610/620 chip set will directly drive all of the popular dual panel/dual scan flat panels from manufacturers such as Sharp, Hitachi, Sanyo, Epson, Kyocera, Optrex, Toshiba etc

Proprietary techniques minimize flicker, noise and pattern motion while enhancing contrast within the gray scales being used.

Gray-scaling is accomplished by modulating the ON to OFF time of individual pixels in the panel and allowing the eye to integrate the superposed pixels to 16 perceptible gray scales. Flicker is eliminated by proprietary techniques involving distribution of time between ON and OFF pixels during frame modulation.

The GD610/620 provides various mechanisms in order to allow the full spectrum of PC applications, written for various TTL and analog monitors, and various video modes, to run on standard 640x400 and 640x480 flat panels.
These mechanisms include color emulation, attribute remapping, resolution mapping, etc

In addition, summing circuitry allows rapid generation of IBM-compatible gray-scale equivalents of color images. Up to 32 gray scales are available using algorithms similar to those used with IBM PS/2-monochrome CRT monitors, enhanced with Cirrus Logic-proprietary 2-dimensional stippling logic. This allows running all applications generating monochrome, 4, 16, or 256 color images with a monochrome flat panel display. CIRRUS LOGIC's AutoMap™ logic is capable of mapping 256 colors to a stunning monochrome image appearing in 32 gray scales. The hardware-based algorithm maintains independence of the particular palette map being used by calculating and storing (in real time) 5 bit gray scale values in an internal palette RAM that reflects all writes to the external RAMDAC. RAMDAC data may be stored as desired by the application in orderly sequences or in random sequences without affecting the consistently realistic renditions of color images.

In color text modes, foreground and background attributes can be automatically remapped to black and white for maximum contrast. Positive or negative raster may be selected under program control to match the visual qualities of the display and/or needs of the application. Bold characters are generated by using built-in intensified text fonts when the attribute calls for intensification.

The video resolutions that an application has selected are remapped to a flat panel according to whether compatibility mode, compression mode or expanded mode was selected.

In compatible text mode, the image is centered on the display with no change in the number of scanlines (200 line modes are double scanned to 400, however). 9 dot character fonts are replaced by 8 dot character fonts (HGC and VGA text) in order to fit within 640 columns. If alternate fonts from plane 3 are used, 9-dot fonts are no longer available.

In compatible graphics mode, the image is centered on the screen, with no change to the number of pixels displayed (except for double scanning 200 line CGA graphics modes). HGC images are 720x348, so panning with a 640 pixel wide window may be performed to view the entire image.

Compression mode allows the 720 horizontal pixels of an HGC generated image to be displayed on a 640 pixel-wide display. Under program control, the 8th and 9th bit of each 9-bit word may be AND'ed or suppressed to generate the compressed bit. This compression provides very little degradation to text, and panning is always available if compressed graphics do not look satisfactory.

Expansion mode lets the display be filled in a symmetric and ratiometrically determined fashion and is available for both text and graphics video modes. In text modes, 9-dot characters are replaced by 8-dot characters, and character cell heights are expanded (from 8, 14, or 16 scanlines) to 19 scanlines. Thus 25 text-lines become 475 scanlines filling most of a 480 scanline panel. The filling algorithm was designed for a symmetric, pleasing expansion of the text, and automatically extends pixels used in character-based graphics applications to the cell boundaries.

Laptop PCs have stringent power dissipation limits. The GD610/620 chip set supports these objectives by being fabricated in low-power CMOS, and by having the ability to drop down to a low-power mode. In this low-power mode, the clock to the GD610 is stopped, and the clock to the RAMDAC is stopped. Low-power static or pseudo-static RAM may also be used in the system.

The FC bits may be used to control power to devices such as the RAMDAC, LCD back-panel, and other H/W.

Low total system component count also contributes to minimizing power consumption. This low chip count is achieved by eliminating most glue logic. For example, an add-in card with an 8-bit host interface can be designed with 16 ICs or less; one with a 16-bit I/F would need no more than 21 ICs.

3.4 Supported Screen Formats

PS/2 (Single Frequency Analog Display, IBM 85xx series-compatible)

Mode No.	No. of Colors	Char. x Row	Char. Cell	Video Mode	Display Mode	Screen Format	Buffer Start	CRT H/V Sync.	Dot Clock
0	4/256K	40x25	8x8	CGA	Text	320x200	B8000	31.5KHz/70Hz	25.172MHz
0*	16/256K	40x25	8x14	EGA	Text	320x350	B8000	31.5KHz/70Hz	25.172MHz
0/1+	16/256K	40x25	9x16	VGA	Text	360x400	B8000	31.5KHz/70Hz	28.332MHz
1	4/256K	40x25	8x8	CGA	Text	320x200	B8000	31.5KHz/70Hz	25.172MHz
1*	16/256K	40x25	8x14	EGA	Text	320x350	B8000	31.5KHz/70Hz	25.172MHz
2	4/256K	80x25	8x8	CGA	Text	640x200	B8000	31.5KHz/70Hz	25.172MHz
2*	16/256K	80x25	8x14	EGA	Text	640x350	B8000	31.5KHz/70Hz	25.172MHz
2/3+	16/256K	80x25	9x16	VGA	Text	720x400	B8000	31.5KHZ/70Hz	28.332MHZ
3	4/256K	80x25	8x8	CGA	Text	640x200	B8000	31.5KHz/70Hz	25.172MHz
3*	16/256K	80x25	8x14	EGA	Text	640x350	B8000	31.5KHz/70Hz	25.172MHz
4	4/256K			CGA	Graphics	320x200	B8000	31.5Khz/70Hz	12.586MHz
5	4/256K			CGA	Graphics	320x200	B8000	31.5KHz/70Hz	12.586MHz
6	2/256K			CGA	Graphics	640x200	B8000	31.5KHz/70Hz	25.172MHz
7	4	80x25	9x14	HGC/MDA	Text	720x350	B0000	31.5KHz/70Hz	28.332MHz
7+	4	80x25	9x16	VGA	Text	720x400	B0000	31.5KHz/70Hz	28.332MHz
HGC	2			HGC	Graphics	720x348	A0000	31.5KHz/70Hz	28.332MHz
D	16/256K			EGA	Graphics	320x200	A0000	31.5KHz/70Hz	12.586MHz
E	16/256K			EGA	Graphics	640x200	A0000	31.6KHz/70Hz	25.172MHz
F*	4			EGA	Graphics	640x350	A0000	31.5KHz/70Hz	25.172MHz
10*	16x256K			EGA	Graphics	640x350	A0000	31.5KHz/70Hz	25.172MHz
11	2/256K			VGA	Graphics	640x480	A0000	31.5KHz/60Hz	25.172MHz
12	16/256K			VGA	Graphics	640x480	A0000	31.5KHz/60Hz	25.172MHz
13	256/256K			VGA	Graphics	320x200	A0000	31.5KHz/70Hz	25.172MHz
40	16/256K	100x30	8x13	Extended	Text	800x390	B8000	31.5KHz/70Hz	32.514MHz
41	16/256K	100x50	8x8	Extended	Text	800x400	B8000	31.5KHz/70Hz	32.514MHz
42	16/256K	100x60	8x8	Extended	Text	800x536	B8000	31.5KHz/56.2Hz	32.514MHz
53	16/256K	80x60	8x8	Extended	Text	640x480	B8000	31.5KHz/70Hz	32.514MHz
63	16/256K			Extended	Graphics	720x540	A0000	31.6KHz/56.5Hz	32.514MHz
70	256/256K			VGA	Graphics	360x480	A0000	31.5KHz/70Hz	28.332MHz

Note: Modes 40-52 and 63-64 require at least a 32.514 MHz dot clock and 100ns DRAM or faster. In monochrome modes, 4 colors is defined as Black, White, "Blinking" White, and "Intensified " White.
Note that "*" and "+" are part of the IBM mode names.

IBM Enhanced Color Display (Model 5154) or Compatible

Mode No.	No. of Colors	Char. x Row	Char. Cell	Video Mode	Display Mode	Screen Format	Buffer Start	CRT H/V Sync.	Dot Clock
0	4	40x25	8x8	CGA	Text	320x200	B8000	15.75KHz/60Hz	14.318MHz
0*	16/64	40x25	8x14	EGA	Text	320x350	B8000	21.85KHz/60Hz	16.257MHz
1	4	40x25	8x8	CGA	Text	320x200	B8000	15.75KHz/60Hz	14.318MHz
1*	16/64	40x25	8x14	EGA	Text	320x350	B8000	21.85KHz/60Hz	16.257MHz
2	4	80x25	8x8	CGA	Text	640x200	B8000	15.75KHz/60Hz	14.318MHz
2*	16/64	80x25	8x14	EGA	Text	640x350	B8000	21.85KHz/60Hz	16.257MHz
3	4	80x25	8x8	CGA	Text	640x200	B8000	15.75KHz/60Hz	14.318MHz
3*	16/64	80x25	8x14	EGA	Text	640x350	B8000	21.85KHz/60Hz	16.257MHz
4	4			CGA	Graphics	320x200	B8000	15.75KHz/60Hz	14.318MHz
5	4			CGA	Graphics	320x200	B8000	15.75KHz/60Hz	14.318MHz
6	2			CGA	Graphics	640x200	B8000	15.75KHz/60Hz	14.318MHz
10*	16/64			EGA	Graphics	640x350	A0000	21.85KHz/60Hz	16.257MHz
D	16/64			EGA	Graphics	320x200	A0000	21.85KHz/60Hz	16.257MHz
E	16/64			EGA	Graphics	640x200	A0000	21.85KHz/60Hz	16.257MHz
F*	4			EGA	Graphics	640x350	A0000	21.85KHz/60Hz	16.257MHz

3.4 Supported Screen Formats (cont'd)

IBM Color Display (Model 5153) or Compatible

Mode No.	No. of Colors	Char. x Row	Char. Cell	Video Mode	Display Mode	Screen Format	Buffer Start	CRT H/V Sync.	Dot Clock
0	4	40x25	8x8	CGA	Text	320x200	B8000	15.75KHz/60Hz	14.318MHz
1	4	40x25	8x8	CGA	Text	320x200	B8000	15.75KHz/60Hz	14.318MHz
2	4	80x25	8x8	CGA	Text	640x200	B8000	15.75KHz/60Hz	14.318MHz
3	4	80x25	8x8	CGA	Text	640x200	B8000	15.75KHz/60Hz	14.318MHz
4	4			CGA	Graphics	320x200	B8000	15.75KHz/60Hz	14.318MHz
5	4			CGA	Graphics	320x200	B8000	15.75KHz/60Hz	14.318MHz
6	2			CGA	Graphics	640x200	B8000	15.75KHz/60Hz	14.318MHz
D	16/64			EGA	Graphics	320x200	A0000	15.75KHz/60KHz	14.318MHz
E	16/64			EGA	Graphics	640x200	A0000	15.75KHz/60Hz	14.318MHz

Note: In monochrome modes, 4 colors is defined as Black, White, "Blinking" White, and "Intensified" White.

IBM Monochrome Display (Model 5151) or Compatible

Mode No.	No. of Colors	Char. x Row	Char. Cell	Video Mode	Display Mode	Screen Format	Buffer Start	CRT H/V Sync.	Dot Clock
7	4	80x25	9x14	HGC/MDA	Text	720x350	B0000	18.4KHz/50Hz	16.257MHz
F*	4			EGA	Graphics	640x350	A0000	18.4KHz/50Hz	16.257MHz
HGC	2			HGC	Graphics	720x348	B0000	18.4KHz/50Hz	16.257MHz

Note: In monochrome modes,4 colors means Black, White, "Blinking" White, and "Intensified" White.

Multi-Frequency Display (NEC Multisync™, SonyMultiscan™, or compatible)

Mode No.	No. of Colors	Char. x Row	Char. Cell	Video Mode	Display Mode	Screen Format	Buffer Start	CRT H/V Sync.†	Dot Clock†
0	4/256K	40x25	8x8	CGA	Text	320x200	B8000	–	–
0*	16/256K	40x25	8x14	EGA	Text	320x350	B8000	–	–
0/1+	16/256K	40x25	9x16	VGA	Text	360x400	B8000	–	–
1	4/256K	40x25	8x8	CGA	Text	320x200	B8000	–	–
1*	16/256K	40x25	8x14	EGA	Text	320x350	B8000	–	–
2	4/256K	80x25	8x8	CGA	Text	640x200	B8000	-	–
2*	16/256K	80x25	8x14	EGA	Text	640x350	B8000	-	–
2/3+	16/256K	80x25	9x16	VGA	Text	720x400	B8000	–	–
3	4/256K	80x25	8x8	CGA	Text	640x200	B8000	–	–
3*	16/256K	80x25	8x14	EGA	Text	640x350	B8000	–	–
4	4/256K			CGA	Graphics	320x200	B8000	–	–
5	4/256K			CGA	Graphics	320x200	B8000	–	–
6	2/256K			CGA	Graphics	640x200	B8000	–	–
7	4	80x25	9x14	HGC/MDA	Text	720x350	B0000	–	–
7+	4	80x25	9x16	VGA	Text	720x400	B0000	–	–
HGC	2			HGC	Graphics	720x348	A0000	–	–
D	16/256K			EGA	Graphics	320x200	A0000	–	–
E	16/256K			EGA	Graphics	640x200	A0000	–	–
F*	4			EGA	Graphics	640x350	A0000	–	–
10*	16/256K			EGA	Graphics	640x350	A0000	–	–
11	2/256K			VGA	Graphics	640x480	A0000	–	–
12	16/256K			VGA	Graphics	640x480	A0000	–	–
13	256/256K			VGA	Graphics	320x200	A0000	–	–
40	16/256K	100x30	9x13	Extended	Text	900x390	B8000	–	–
41	16/256K	100x50	8x8	Extended	Text	800x400	B8000	–	–
42	16/256K	100x60	8x8	Extended	Text	800x480	B8000	–	–
43	16/256K	100x75	8x8	Extended	Text	800x600	B8000	–	–
50	16/256K	132x30	8x13	Extended	Text	1056x390	B8000	–	–
51	16/256K	132x50	8x8	Extended	Text	1056x400	B8000	–	–
52	16/256K	132x60	8x8	Extended	Text	1056x480	B8000	–	–
53	16/256K	80x60	8x8	Extended	Text	640x480	B8000	–	–
63	16/256K			Extended	Graphics	720x540	A0000	–	–
64	16/256K			Extended	Graphics	800x600	A0000	–	–
70	256/256K			VGA	Graphics	360x480	A0000	-	-

Note: Modes 40h-52h and 63h-64h require at least a 32.514 MHz dot clock and 100ns DRAM or faster. In monochrome modes, 4 colors is defined as Black, White, "Blinking" White, and "Intensified " White.
Note that "*" and "+" are part of the IBM mode names.
† These values will vary depending upon which monitor and which monitor parameters are used in the BIOS.

3.5 LCD/CRT Screen Format Comparison Table

			Compatible mode				Expansion/ Compression Mode	
Mode	CRT Color	Type	Color Emulation	Video Clock	Display Area	Cell Size	Display Area	Cell Size
0,1	16/256K	40x25 CGA text	Color Attr. emul	14.17	640x400	16x16	640x475	16x19
2,3	16/256K	80x25 CGA text	ColorAttr. emul	28.33	640x400	8x16	640x475	8x19
0*,1*	16/256K	40x25 EGA text	Color Attr. emul	14.17	640x350	16x14	640x475	16x19
2*,3*	16/256K	80x25 EGA text	Color Attr. emul	28.33	640x350	8x14	640x475	8x19
0+,1+	16/256K	40x25 VGA text	Color Attr. emul	14.17	640x400	16x16	640x475	16x19
2+,3+	16/256K	80x25 VGA text	Color Attr. emul	28.33	640x400	8x16	640x475	8x19
4,5	4/256K	320x200 CGA gr	4 Gray Scl-ACB	14.17	640x400	2x2	640x475	2x2
6	2/256K	640x200 CGA gr	2 Gray Scl-ACB	28.33	640x400	1x2	640x475	1x2
7	Mono	80x25 MGA text	Mono Attr. emul	28.33	640x350	8x14	640x475	8x19
7+	Mono	80x25 VGA text	Mono Attr. emul	28.33	640x400	8x16	640x475	8x19
D	16/256K	320x200 EGA gr	16 Gray Scales	14.17	640x400	2x2	640x475	2x2
E	16/256K	640x200 EGA gr	16 Gray Scales	28.33	640x400	1x2	640x475	1x2
F*	Mono	640x350 EGA gr	On,Off,Bl,Halftn	28.33	640x350	1x1	640x475	1x1
10*	16/256K	640x350 EGA gr	16 Gray Scales	28.33	640x350	1x1	640x475	1x1
11	2/256K	640x480 VGA gr	2 Gray Scl-ACB	28.33	640x480	1x1	640x480	1x1
12	16/256K	640x480 VGA gr	16 Gray Scales	28.33	640x480	1x1	640x480	1x1
13	256/256K	320x200 VGA gr	32 Gray Scales	14.17	640x400	2x2	640x475	2x2
-	Mono	720x348 HGC gr	Image comp/pan	28.33	640x350	1x1	640x475	1x1

Note1: ACB: - Automatic Contrast Balancing

Note2: Color Attribute Emulation: -when foreground and background colors are different, they are mapped to high contrast gray scales.
-when foreground and background colors are the same, then different gray scales are selected to enhance contrast.

Mono Attribute Emulation: -straightforward mapping of monochrome attributes to gray scales similar to CRT case

4 VGA, EGA, CGA, AND HGC REGISTER PORT MEMORY MAP

Address	VGA/EGA Port	CGA Port	HGC Port
2B0 / 3B0	CRTC Index (R/W) (EGA Only)		6845 Index (R/W)
2B1 / 3B1	CRTC Data (R/W) (EGA Only)		6845 Data (R/W)
2B2 / 3B2	CRTC Index (R/W) (EGA Only)		6845 Index (R/W)
2B3 / 3B3	CRTC Data (R/W) (EGA Only)		6845 Data (R/W)
2B4 / 3B4	CRTC Index (R/W) (EGA Only)		6845 Index (R/W)
2B5 / 3B5	CRTC Data (R/W)		6845 Data (R/W)
2B6 / 3B6	CRTC Index (R/W) (EGA Only)		6845 Index (R/W)
2B7 / 3B7	CRTC Data (R/W) (EGA Only)		6845 Data (R/W)
2B8 / 3B8			Mode Control (R/W)
2B9 / 3B9			Set Light Pen Flip Flop (W)
2BA / 3BA	Feature Control(W), Display Status(R)		Display Status (R)
2BB / 3BB	Clear Light Pen Flip Flop (W)		Clear Light Pen Flip Flop (W)
2BC / 3BC	Set Light Pen Flip Flop (W)		
2BD / 3BD			
2BE / 3BE			
2BF / 3BF			Configuration (R/W)
2C0 / 3C0	Attribute Controller Index/Data (R/W)		
2C1 / 3C1	Attribute Controller Index/Data (R/W)		
2C2 / 3C2	Misc Output (W), Feature (R)		
2C3 / 3C3	Misc Output (W), Feature (R)		
2C4 / 3C4	Sequencer/Extensions Index (R/W)		
2C5 / 3C5	Sequencer/Extensions Data (R/W)		
2C6 / 3C6	Palette Pixel Mask (R/W)		
2C7 / 3C7	Palette Address Register R Mode (R/W)		
2C8 / 3C8	Palette Address Register W Mode (R/W)		
2C9 / 3C9	Palette Data (R/W)		
2CA / 3CA	G. Pos. 2 (W) (EGA Only)		
2CB / 3CB	(Reserved)		
2CC / 3CC	G. Pos. 1(W)(EGA Only) Misc Output (R)		
2CD / 3CD	(Reserved)		
2CE / 3CE	Graphics Controller Index (R/W)		
2CF / 3CF	Graphics Controller Data (R/W)		
2D0 / 3D0	CRTC Index (R/W) (EGA Only)	6845 Index (R/W)	
2D1 / 3D1	CRTC Data (R/W) (EGA Only)	6845 Data (R/W)	
2D2 / 3D2	CRTC Index (R/W) (EGA Only)	6845 Index (R/W)	
2D3 / 3D3	CRTC Data (R/W) (EGA Only)	6845 Data (R/W)	
2D4 / 3D4	CRTC Index (R/W) (EGA Only)	6845 Index (R/W)	
2D5 / 3D5	CRTC Data (R/W)	6845 Data (R/W)	
2D6 / 3D6	CRTC Index (R/W) (EGA Only)	6845 Index (R/W)	
2D7 / 3D7	CRTC Data (R/W) (EGA Only)	6845 Data (R/W)	
2D8 / 3D8		Mode Control (R/W)	
2D9 / 3D9		Color Select (R/W)	
2DA / 3DA	Feature Control(W), Display Status(R)	Display Status (R)	
2DB / 3DB	Clear Light Pen Flip Flop (W)	Clear Light Pen Flip Flop (W)	
2DC / 3DC	Set Light Pen Flip Flop (W)	Set Light Pen Flip Flop (W)	
2DD / 3DD			
2DE / 3DE			
2DF / 3DF			

5 CGA, MDA, AND HGC REGISTERS

5.1 Color Graphics Adapter (CGA) Compatible Registers

ABBREV	CGA REGISTER NAME	BITS	REG TYPE	READ/ WRITE	REG/ INDEX	PORT ADDRESS
MODE	Mode Control	7	GD610/GD620‡	R/W	--	3D8
COLOR	Color Select	6	GD610	R/W	--	3D9
STAT	Display Status	7	GD610/GD620‡	R	--	3DA
CLPEN	Clear Light Pen Flip Flop	0	GD620	W	--	3DB
SLPEN	Set Light Pen Flip Flop	0	GD620	W	--	3DC
CRX	6845 Index	5	GD620	R/W	--	3D4 (3D0,3D2,3D6)†
R0	Horizontal Total	8	GD620	R/W	00	3D5 (3D1,3D3,3D7)†
R1	Horizontal Displayed	8	GD620	R/W	01	3D5 (3D1,3D3,3D7)†
R2	Horizontal Sync Position	8	GD620	R/W	02	3D5 (3D1,3D3,3D7)†
R3	Sync Width	4+4††	GD620	R/W	03	3D5 (3D1,3D3,3D7)†
R4	Vertical Total	7	GD620	R/W	04	3D5 (3D1,3D3,3D7)†
R5	Vertical Total Adjust	5	GD620	R/W	05	3D5 (3D1,3D3,3D7)†
R6	Vertical Displayed	7	GD620	R/W	06	3D5 (3D1,3D3,3D7)†
R7	Vertical Sync Position	7	GD620	R/W	07	3D5 (3D1,3D3,3D7)†
R8	Interlace Mode	2	GD620	R/W	08	3D5 (3D1,3D3,3D7)†
R9	Character Cell Height	5	GD620	R/W	09	3D5 (3D1,3D3,3D7)†
RA	Cursor Start	5+2††	GD620	R/W	0A	3D5 (3D1,3D3,3D7)†
RB	Cursor End	5	GD620	R/W	0B	3D5 (3D1,3D3,3D7)†
CRC	Start Address High	8	GD620	R/W	0C	3D5 (3D1,3D3,3D7)†
CRD	Start Address Low	8	GD620	R/W	0D	3D5 (3D1,3D3,3D7)†
CRE	Cursor Address High	8	GD620	R/W	0E	3D5 (3D1,3D3,3D7)†
CRF	Cursor Address Low	8	GD620	R/W	0F	3D5 (3D1,3D3,3D7)†
LPENH	Light Pen High	8	GD620	R	10	3D5 (3D1,3D3,3D7)†
LPENL	Light Pen Low	8	GD620	R	11	3D5 (3D1,3D3,3D7)†

5.2 Monochrome Display Adapter (MDA) and Hercules Graphics Adapter (HGC) Compatible Registers

ABBREV	MDA/HGC REGISTER NAME	BITS	REG TYPE	READ/ WRITE	REG/ INDEX	PORT ADDRESS
MODE	Mode Control	7	GD610/GD620‡	R/W	--	3B8
STAT	Display Status	7	GD610/GD620‡	R	--	3BA
CONFIG	Configuration	2	GD610/GD620‡	R/W	--	3BF
CLPEN	Clear Light Pen Flip Flop	0	GD620	W	--	3BB
SLPEN	Set Light Pen Flip Flop	0	GD620	W	--	3B9
CRX	6845 Index	5	GD620	R/W	--	3B4 (3B0,3B2,3B6)†
R0	Horizontal Total	8	GD620	R/W	00	3B5 (3B1,3B3,3B7)†
R1	Horizontal Displayed	8	GD620	R/W	01	3B5 (3B1,3B3,3B7)†
R2	Horizontal Sync Position	8	GD620	R/W	02	3B5 (3B1,3B3,3B7)†
R3	Sync Width	4+4††	GD620	R/W	03	3B5 (3B1,3B3,3B7)†
R4	Vertical Total	7	GD620	R/W	04	3B5 (3B1,3B3,3B7)†
R5	Vertical Total Adjust	5	GD620	R/W	05	3B5 (3B1,3B3,3B7)†
R6	Vertical Displayed	7	GD620	R/W	06	3B5 (3B1,3B3,3B7)†
R7	Vertical Sync Position	7	GD620	R/W	07	3B5 (3B1,3B3,3B7)†
R8	Interlace Mode	2	GD620	R/W	08	3B5 (3B1,3B3,3B7)†
R9	Character Cell Height	5	GD620	R/W	09	3B5 (3B1,3B3,3B7)†
RA	Cursor Start	5+2††	GD620	R/W	0A	3B5 (3B1,3B3,3B7)†
RB	Cursor End	5	GD620	R/W	0B	3B5 (3B1,3B3,3B7)†
CRC	Start Address High	8	GD620	R/W	0C	3B5 (3B1,3B3,3B7)†
CRD	Start Address Low	8	GD620	R/W	0D	3B5 (3B1,3B3,3B7)†
CRE	Cursor Address High	8	GD620	R/W	0E	3B5 (3B1,3B3,3B7)†
CRF	Cursor Address Low	8	GD620	R/W	0F	3B5 (3B1,3B3,3B7)†
LPENH	Light Pen High	8	GD620	R	10	3B5 (3B1,3B3,3B7)†
LPENL	Light Pen Low	8	GD620	R	11	3B5 (3B1,3B3,3B7)

‡ Physical readback chip is underlined for split/duplicated registers
† Valid alternate register addresses are presented in parenthesis
†† Split-field registers are denoted by 'X+Y'

6 VGA / EGA REGISTERS

6.1 Video Graphics Array/Enhanced Graphics Adapter Compatible Register Table

ABBREV	EGA REGISTER NAME	BITS	REG TYPE	R/W	REG/NDX	MONO PORT	COLOR PORT
MISC	Miscellaneous Output	8	GD610/GD620‡	W	--	3C2	3C2
FEAT	Input Status 0 (Feature Read)	4	GD610/GD620‡	R	--	3C2	3C2
STAT	Input Status 1 (Display Status)	7	GD610/GD620‡	R	--	3BA	3DA
FC	Feature Control	3	GD610	W	--	3BA	3DA
GPOS1/MISC	Graphics 1 Pos (W), Misc (R)	2,8	GD610, GD610/GD620‡	R/W	--	3CC	3CC
GPOS2/FC	Graphics 2 Pos (W), FeatCtrl (R)	2,3	GD610,GD610	R/W	--	3CA	3CA
GRX	Graphics Controller Index	4	GD610	R/W	--	3CE	3CE
GR0	Set/Reset	4	GD610	R/W	00	3CF	3CF
GR1	Enable Set/Reset	4	GD610	R/W	01	3CF	3CF
GR2	Color Compare	4	GD610	R/W	02	3CF	3CF
GR3	Data Rotate	5	GD610	R/W	03	3CF	3CF
GR4	Read Map Select	3	GD610	R/W	04	3CF	3CF
GR5	Mode	7	GD610	R/W	05	3CF	3CF
GR6	Miscellaneous	4	GD620	R/W	06	3CF	3CF
GR7	Color Don't Care	4	GD610	R/W	07	3CF	3CF
GR8	Bit Mask	8	GD610	R/W	08	3CF	3CF
ARX	Attribute Controller Index	6	GD610/GD620‡	R/W	--	3C0	3C0
AR0-F	Color Palette Regs 0-15	8	GD610	R/W	00-0F	3C0	3C0
AR10	Mode Control	7	GD610	R/W	10	3C0	3C0
AR11	Overscan Color	8	GD610	R/W	11	3C0	3C0
AR12	Color Plane Enable	6	GD610	R/W	12	3C0	3C0
AR13	Horizontal Pixel Panning	4	GD610	R/W	13	3C0	3C0
AR14	Color Select	4	GD610	R/W	14	3C0	3C0
CLPEN	Clear Light Pen Flip Flop	0	GD620	W	--	3BB	3DB
SLPEN	Set Light Pen Flip Flop	0	GD620	W	--	3BC / 3B9	3DC
SERX	Sequencer / Extension Reg. Index	7	GD620	R/W	--	3C4	3C4
SR0	Reset	2	GD620	R/W	00	3C5	3C5
SR1	Clocking Mode	6	GD620	R/W	01	3C5	3C5
SR2	Plane Mask	4	GD620	R/W	02	3C5	3C5
SR3	Character Map Select	6	GD620	R/W	03	3C5	3C5
SR4	Memory Mode	3	GD6610/20	R/W	04	3C5	3C5
SR6	Extensions Control (see Ext. Table)	1	GD610/GD620‡	R/W	06	3C5	3C5
SR7	Reset H. Character Counter	1	GD620	W	07	3C5	3C5
CRX	CRTC Index	6/5	GD620	R/W	--	3B4	3D4
CR0	Horizontal Total	8	GD620	R/W	00	3B5	3D5
CR1	Horizontal Display End	8	GD620	R/W	01	3B5	3D5
CR2	Horizontal Blanking Start	8	GD620	R/W	02	3B5	3D5
CR3	Horizontal Blanking End	5+2+1††	GD620	R/W	03	3B5	3D5
CR4	Horizontal Retrace Start	8	GD620	R/W	04	3B5	3D5
CR5	Horizontal Retrace End	5+2+1††	GD620	R/W	05	3B5	3D5
CR6	Vertical Total	8	GD620	R/W	06	3B5	3D5
CR7	Overflow	8	GD620	R/W	07	3B5	3D5
CR8	Screen A Preset Row Scan	7	GD620	R/W	08	3B5	3D5
CR9	Character Cell Height	5+1+1+1	GD620	R/W	09	3B5	3D5
CRA	Cursor Start	6	GD620	R/W	0A	3B5	3D5
CRB	Cursor End	5+2††	GD620	R/W	0B	3B5	3D5
CRC	Screen A Start Address High	8	GD620	R/W	0C	3B5	3D5
CRD	Screen A Start Address Low	8	GD620	R/W	0D	3B5	3D5
CRE	Cursor Location High	8	GD620	R/W	0E	3B5	3D5
CRF	Cursor Location Low	8	GD620	R/W	0F	3B5	3D5
LPENH	Light Pen High	8	GD620	R	10	3B5	3D5
LPENL	Light Pen Low	8	GD620	R	11	3B5	3D5
CR10	Vertical Retrace Start	8	GD620	W	10	3B5	3D5
CR11	Vertical Retrace End	4+2+1+1††	GD620	W	11	3B5	3D5
CR12	Vertical Display End	8	GD620	R/W	12	3B5	3D5
CR13	Offset	8	GD620	R/W	13	3B5	3D5
CR14	Underline Location	5+2††	GD620	R/W	14	3B5	3D5
CR15	Vertical Blanking Start	8	GD620	R/W	15	3B5	3D5
CR16	Vertical Blanking End	8	GD620	R/W	16	3B5	3D5
CR17	CRT Mode Control	7	GD620	R/W	17	3B5	3D5
CR18	Line Compare	8	GD620	R/W	18	3B5	3D5
CR22	Readback CRT Latches	8	GD610	R	22	3B5	3D5
CR24	Attribute Index Toggle	7	GD610	R	24	3B5	3D5
CR26MSB	CRTC scrA str addr MSB	2	GD620	R/W	26	3B5	3D5
CR27MSB	CRTC cursor addr MSB	2	GD620	R/W	27	3B5	3D5
CR30-CR3F	Frame Blank	1	GD620	W	3X	3B5	3D5

‡ Physical readback chip is underlined for split/duplicated registers
†† Split-field registers are denoted by 'X+Y' or "X+Y+Z" or 'X+Y+Z+M.'

6.2 Extension Register Table (GD510A/520A compatible)

ABBREV	EXTENSION REGISTER	BITS	REG TYPE	READ/WRITE	REG/INDEX	PORT ADDR
SERX	Sequencer Extensions Register Index	7	GD610/GD620‡	R/W	–	3C4
SR6	Extension Control	1	GD610/GD620‡	R/W	06	3C5
CR7F	Identification	8	GD620	R	7F	3B5/3D5
MC1	Misc. Control 1	8	GD620	R/W	80	3C5
GPOS1	Graphics 1 Position	2	GD610	R/W	81	3C5
GPOS2	Graphics 2 Position	2	GD610	R/W	82	3C5
ARX	Attribute Controller Index	7	GD610	R/W	83	3C5
WRC	Write Control	8	GD610/GD620‡	R/W	84	3C5
TC	Timing Control	7	GD620	R/W	85	3C5
BWC	Bandwidth Control	6	GD620	R/W	86	3C5
MC2	Misc. Control 2	8	GD620	R/W	87	3C5
HSS	H. Sync Skew	4	GD620	R/W	88	3C5
FONTC	CGA, HGC Font Control	4	GD620	R/W	89	3C5
	-reserved-	0	–	–	8A	3C5
SBPR	Screen B Preset Row Scan	5	GD620	R/W	8B	3C5
SBSH	Screen B Start Address High	8	GD620	R/W	8C	3C5
SBSL	Screen B Start Address Low	8	GD620	R/W	8D	3C5
GAVER	GD610 Version Code	8	GD610	R	8E	3C5
SCVER	GD620 Version Code	8	GD620	R	8F	3C5
CR10	Vertical Retrace Start	8	GD620	R/W	90	3C5
CR11	Vertical Retrace End	8	GD620	R/W	91	3C5
LPENH	Light Pen High	8	GD620	R/W	92	3C5
LPENL	Light Pen Low	8	GD620	R/W	93	3C5
PPAH	Pointer Pattern Address High	8	GD620	R/W	94	3C5
CADJ	Cursor Height Adjust	5	GD620	R/W	95	3C5
CW	Caret Width	8	GD610	R/W	96	3C5
CH	Caret Height	8	GD610	R/W	97	3C5
CXH	Caret Horizontal Position High	3	GD610	R/W	98	3C5
CXL	Caret Horizontal Position Low	8	GD610	R/W	99	3C5
CYH	Caret Vertical Position High	2	GD610	R/W	9A	3C5
CYL	Caret Vertical Position Low	8	GD610	R/W	9B	3C5
PXH	Pointer Horizontal Position High	3	GD610	R/W	9C	3C5
PXL	Pointer Horizontal Position Low	8	GD610	R/W	9D	3C5
PYH	Pointer Vertical Position High	2	GD620	R/W	9E	3C5
PYL	Pointer Vertical Position Low	8	GD620	R/W	9F	3C5
GRL0	Graphics Ctrlr Memory Latch 0	8	GD610	R/W	A0	3C5
GRL1	Graphics Ctrlr Memory Latch 1	8	GD610	R/W	A1	3C5
GRL2	Graphics Ctrlr Memory Latch 2	8	GD610	R/W	A2	3C5
GRL3	Graphics Ctrlr Memory Latch 3	8	GD610	R/W	A3	3C5
CLK	Clock Select	6	GD610	R/W	A4	3C5
CURS	Cursor Attributes	8	GD610/GD620‡	R/W	A5	3C5
ISS	Internal Switch Source	8	GGD610	R/W	A6	3C5
NMI1	NMI Mask 1	8	GD610	R/W	A8	3C5
NMI2	NMI Mask 2	8	GD610	R/W	A9	3C5
	-reserved-	0	–	–	AA	3C5
SWITCH	State Switch Control	8	GD610/GD620‡	R/W	A7	3C5
CACHE	NMI Data Cache‡‡	4x24	GD610	R	AE	3C5
NSTAT1	NMI Status 1	8	GD610	R	AB	3C5
NSTAT2	NMI Status 2	8	GD610	R	AC	3C5
256 CPC	256 Color Page Control	4	GD620	R/W	AD	3C5
STATE	Active Adapter State	7	GD610/GD620‡	R/W	AF	3C5
SCR0-F	Scratch Register 0-F	8	GD610	R/W	B0-BF	3C5

‡ Physical readback chip is underlined for split/duplicated registers
‡‡ NMI Data Cache consists of four 24-bit words.

6.3 Added Extension Register Table (New to GD610/620)

ABBREV	EXTENSION REGISTER	BITS	REG TYPE	READ/WRITE	REG/INDEX	PORT ADDR
-	Graphics Cursor Address	2	GD620	-	-	-
CR26MSB	CRTC scrA strt addr highest	2	GD620	R/W	26	3?5
CR27MSB	CRTC Cursor addr highest	2	GD620	R/W	27	3?5
LCDCNTL1	LCD Control register 1	8	GD610/620	R/W	8A	3C5
CPURAR	CPU Read Access Register	8	GD620	R/W	C0	3C5
CPUWAR	CPU Write Access Register	8	GD620	R/W	C1	3C5
LCDCNTL2	LCD Control register 2	8	GD620	R/W	C2	3C5
SWITCHH	Switch Setting Register High	8	GD620	R	C4	3C5
SWITCHL	Switch Setting Register Low	8	GD620	R	C5	3C5
SBSHH	Screen B strt addr highest	2	GD620	R/W	C6	3C5
LCDCNTL3	LCD Control register 3	3	GD610/620	R/W	C7	3C5
COLOFF	Column Offset	8+1	GD610	R/W	D0-D4	3C5
PNLHDIS	Panel Horizontal Displayed	8+1	GD610	R/W	D1-D4	3C5
ROWOFF	Row Offset	8+1	GD610	R/W	D2-D4	3C5
PRSEGTOT	Panel Row Segment Total	8+1	GD610	R/W	D3-D4	3C5
PNLCNTL1	Panel Control 1	8	GD610	R/W	D4	3C5
PNLCNTL2	Panel Control 2	8	GD610	R/W	D5	3C5
FONTC	Plane 3 Alt font enable	1	GD610/620	R/W	89	3C5
GROFFSET	Gray-scale Offset	4	GD610	R/W	D6	3C5
MOD	Modulation/AC inversion	8	GD610	R/W	D9	3C5
FRMCOLOR	Frame Color	4	GD610	R/W	DA	3C5
PNLCNTL3	Panel Control 3(reserved)	8	GD610	R/W	DB	3C5

7 ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Ambient Temperature Under Bias. .....0° C to 70° C
Storage Temperature. .....-65° C to 150° C
Voltage On Any Pin With Respect To Ground.....GND-0.5 to VCC+0.5 Volts
Operating Power Dissipation (Per Chip).....0.300 Watt
Standby Power Dissipation (Per Chip).. .....0.035 Watt
Power Supply Voltage. .....7 Volts
Injection Current (Latch-up). .....25 mA

Note: Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

7.2 CL–GD610 / 620 D.C. Characteristics

(VCC=5V±5%, TA=0° to 70° C, unless otherwise specified)

	SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
	VCC	Power Supply Voltage	4.75	5.25	V	Normal Operations
	VIL	Input Low Voltage	-0.5	0.8	V	
	VIH	Input High Voltage	2.0	VCC + 0.5	V	
	VOL	Output Low Voltage		0.4	V	IOL = 2mA†
GD610	VOH	Output High Voltage	2.4		V	IOH = 400µA
	ICC	Operating Supply Current		40	mA	@ 33MHz, 5V nominal
	ICCpd	Powerdown mode current			mA	@ 33MHz, 5V nominal
	IL	Input Leakage	-10	10	µA	0 < VIN < VCC
	CIN	Input Capacitance		10	pF	
	COUT	Output Capacitance		10	pF	
	VCC	Power Supply Voltage	4.75	5.25	V	Normal Operations
	VIL	Input Low Voltage	-0.5	0.8	V	
	VIH	Input High Voltage	2.0	VCC + 0.5	V	
	VOL	Output Low Voltage		0.4	V	IOL = 2mA††
GD620	VOH	Output High Voltage	2.4		V	IOH = 400µA
	ICC	Operating Supply Current		40	mA	@ 33MHz, 5V nominal
	ICCpd	Powerdown mode current			mA	@ 33MHz, 5V nominal
	IL	Input Leakage	-10	10	µA	0 < VIN < VCC
	CIN	Input Capacitance		10	pF	
	COUT	Output Capacitance		10	pF	

†**NOTE:** IOL max for GD610 = 12mA for NMI* (IOCHCK*) @ .4 Vol
= 16mA for NMI* (IOCHCK*) @ .5 Vol

††**NOTE:** IOL max for GD620 = 12mA for CPURDY, CRTINT
= 8mA for DIR / CRDSEL*, WE*, CAS*

7.3 A.C. Characteristics / Timing Information

The following timing information assumes that all outputs will drive one Schottky TTL load in parallel with 50 pF and all inputs are at TTL level. The MIN and MAX timings are those conforming to the operating ranges of a power supply voltage of 5V ± 5% and an ambient temperature of 0° C to 70° C.

Index of Timing Information

DRAM Memory Performance Table

DRAM ACCESS TIME (ns)	DOT CLOCK FREQ. (MHz)	MEMORY BANDWIDTH CPU:CRT CYCLE INTERLEAVE
80	25	
100	20	1:1, 1:2
120	16	
150	13	
80	33	
100	30	3:2‡
120	25	
150	20	
80	FcMax†	
100	33	1:4 8 dot character clock
120	25	
150	20	
80	FcMax†	
100	FcMax†	1:7 8 dot character clock
120	30	1:4 9 dot character clock
150	26	

† FcMax = Maximum CLKIN frequency = 1/Tc = 33MHz

‡ Used when Dot Clock = Clock in/2

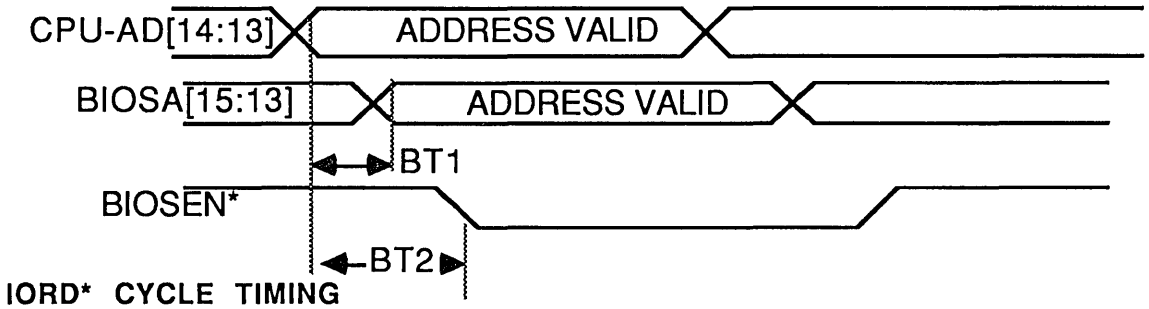
Note: 1 character clock is 8 dot clocks in graphics modes and either 8 or 9 dot clocks in text modes, depending upon the character width used.

BIOS Interface, I/O Port, and RAMDAC Timing Table

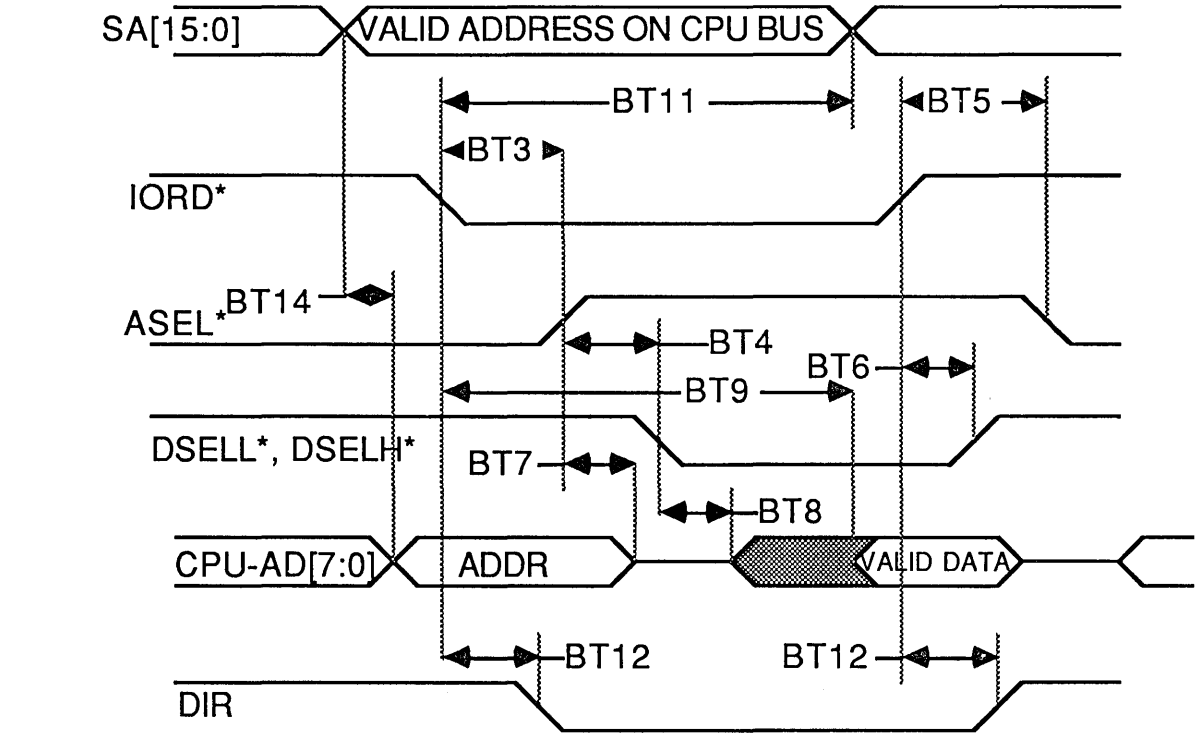
SYMBOL	PARAMETER	MIN	MAX	UNITS
BT1	CPU Address to BIOS Address valid Delay		40	ns
BT2	Address to BIOSEN* Delay		40	ns
BT3	ASEL* delay after command active delay		40	ns
BT4	DSELL/H* low from ASEL* high delay		18	ns
BT5	ASEL* delay after command inactive delay		40	ns
BT6	DSEL* high after command inactive delay		32	ns
BT7	Allowable Address hold time after ASEL* inactive		20	ns
BT8	Allowable Data drive delay from DSELL/H* active		20	ns
BT9	IORD* access time	100		ns
BT10	Min inter-command delay for IORD*	80		ns
BT11	Bus address hold time from IORD* low	BT3+BT7		ns
BT12	DIR low delay from IORD* command		36	ns
BT13	CPRD*/CPWR* delay from command		30	ns
BT14	Bus Address to CPU-AD[7:0] delay		40	ns
BT15	Command delay after IOWR* inactive	120		ns
BT16	Data setup time to IOWR* trailing edge	60		ns
BT17	IOWR* to I/O Port output delay (FC[0,1], INTERNAL*, CLKxx)		80	ns
BT18	RESET pulse width	500		ns
BT19	Select lines inactive after RESET active		100	ns
BT20	Select lines inactive hold time after RESET low	30	100	ns
BT21	CPU-AD bus High-Z setup time to RESET low	400		ns

NOTE: BT2 depends on ROM access time from enable and bidirectional buffer prop delay time
BT4, BT7, BT8, BT9 depend on external components selected. Max delays shown here for reference only
'Command' implies IOWR*/IORD* or MEMR*/MEMW*; I/O command means IOWR*/IORD*

BIOS ADDRESSING TIMING

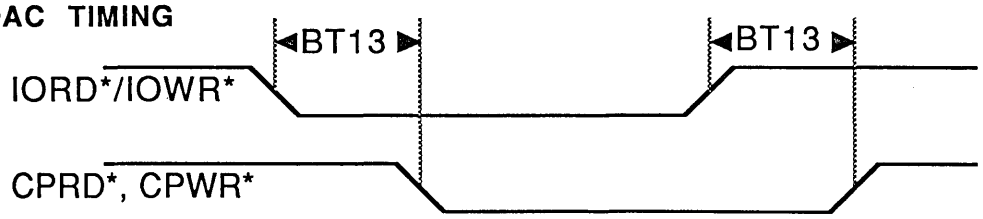


IORD* CYCLE TIMING

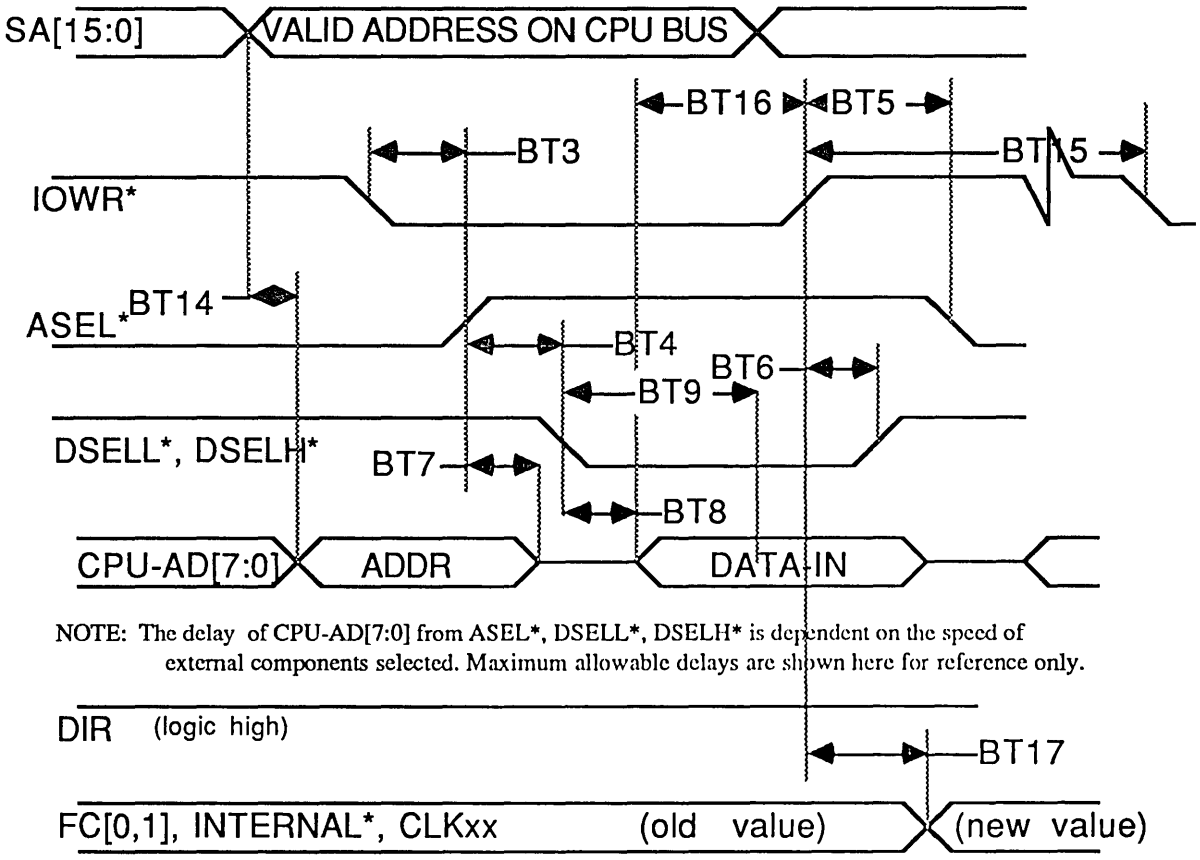


NOTE: The delay of CPU-AD[7:0] from ASEL*, DSELL*, DSELH* is dependent on the speed of external components selected. Maximum allowable delays are shown here for reference only.

RAMDAC TIMING

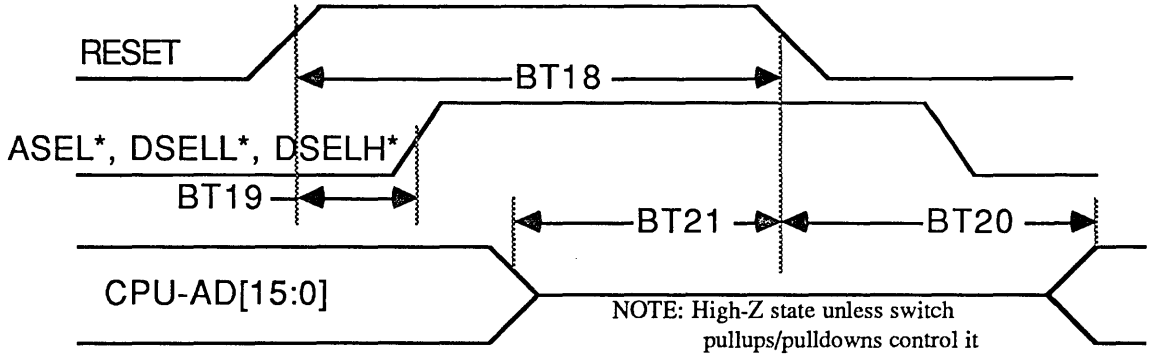


IOWR* CYCLE TIMING



NOTE: The delay of CPU-AD[7:0] from ASEL*, DSELL*, DSELH* is dependent on the speed of external components selected. Maximum allowable delays are shown here for reference only.

I/O BUS TIMING AT RESET



NOTE: High-Z state unless switch pullups/pulldowns control it

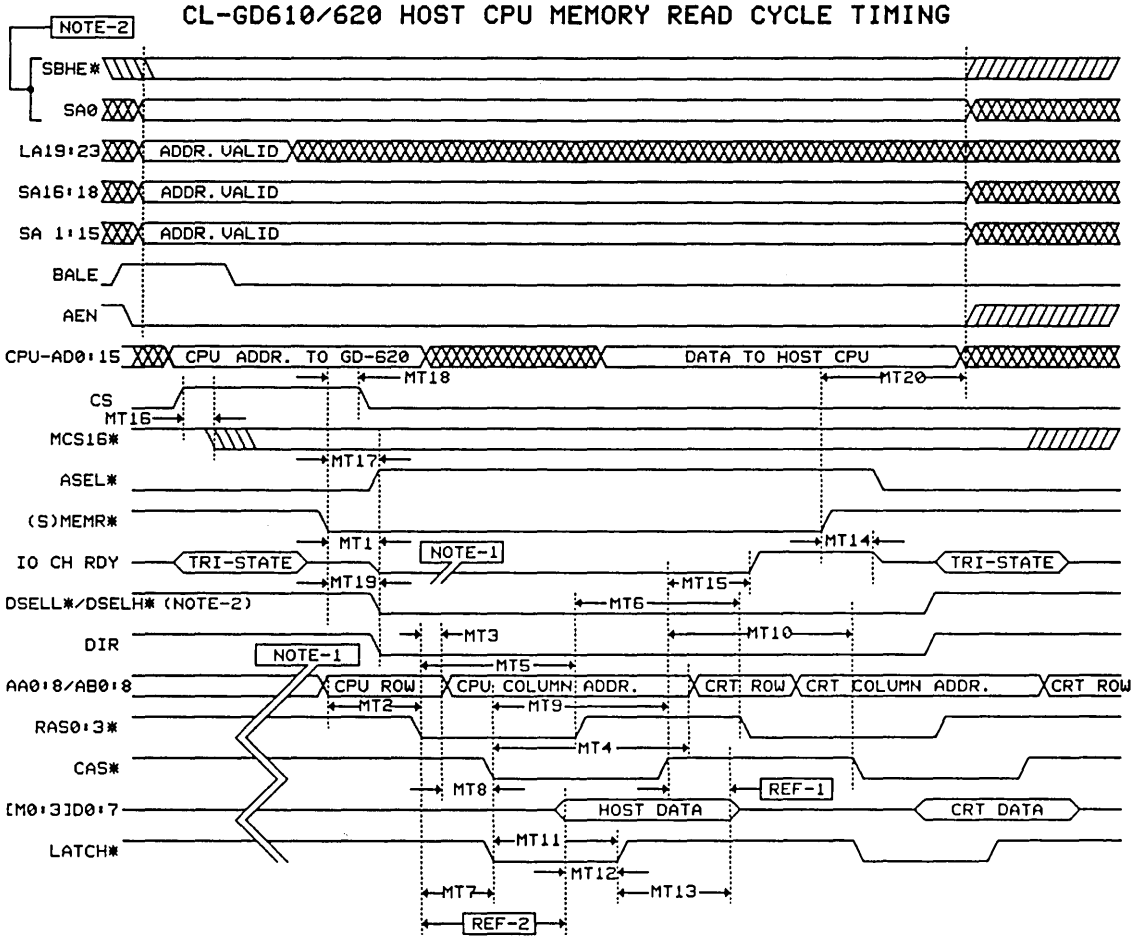
DRAM Read Timing Table

SYMBOL	PARAMETER	X:Y - Z † 1:4 - 9	1:4 - 8	1:7 - 8	3:2 - 8	1:2 - 6	1:1 - 8	1:1 - 9	ns
Tc	CLKIN Cycle Time (100 ns DRAM)	25	30	25	30	50	50	50	Typ
MT1	CPURDY Low from MEMR*	15	15	15	15	15	15	15	Typ
MT2	Row Address Setup Time	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	Typ
MT3	Row Address Hold Time	0.5 Tc	0.5 Tc	0.5 Tc	0.5 Tc	15	15	15	Typ
MT4	Column Address Hold Time	4 Tc	3 Tc	4 Tc	3 Tc	1.5 Tc	1.5 Tc	1.5 Tc	Typ
MT5	RAS* Low Time	4 Tc	3 Tc	4 Tc	3 Tc	2 Tc	2 Tc	2 Tc	Typ
MT6	RAS* Precharge	3 Tc	3 Tc	3 Tc	3 Tc	2 Tc	2 Tc	2 Tc	Typ
MT7	RAS* to CAS* Delay	1 Tc	1 Tc	1 Tc	1 Tc	0.5 Tc	0.5 Tc	0.5 Tc	Typ
MT8	Column Address Setup Time	5	5	5	5	5	5	5	Typ
MT9	CAS* Low Time	5 Tc	4 Tc	5 Tc	4 Tc	2.5 Tc	2.5 Tc	2.5 Tc	Typ
MT10	CAS* Precharge	2 Tc	2 Tc	2 Tc	2 Tc	1.5 Tc	1.5 Tc	1.5 Tc	Typ
MT11	Data Sample From CAS* (T34-0.5Tc)	4.5 Tc	3.5 Tc	4.5 Tc	3.5 Tc	2 Tc	2 Tc	2Tc	Typ
MT12	Valid Data Setup Time (to LATCH*)	0	0	0	0	0	0	0	Typ
MT13	Valid Data Hold Time (to LATCH*)	40	40	40	40	40	40	40	Typ
MT14	MEMR* Inactive to CPURDY* Tristate	15	15	15	15	15	15	15	Typ
MT15	CPU Read Cycle End to CPURDY* Inactive	1 Tc	1 Tc	1 Tc	1 Tc	1 Tc	1 Tc	1 Tc	Typ
MT16	CS valid to MCS16* active	20	20	20	20	20	20	20	Typ
MT17	MEMR* active to ASEL* disable	40/20	40/20	40/20	40/20	40/20	40/20	40/20	Max/Typ
MT18	CS hold time after command	45	45	45	45	45	45	45	Min
MT19	MEMR* active to DSEL* active delay	58/30	58/30	58/30	58/30	58/30	58/30	58/30	Max/Typ
MT20	MEMR* to CPU read data hold time	32/16	32/16	32/16	32/16	32/16	32/16	32/16	Max/Typ

† X:Y - Z (X = CPU Cycles, Y = CRT Cycles, Z = Dots / Character)

NOTE: All times are in nanoseconds (ns) unless otherwise noted; 50 pf Load capacitance is assumed.; Use parameter MT20 with I/O port parameters BT5, BT6
GD610 latches the video memory data on the rising edge of LATCH*. That is when the data is actually sampled (See MT11, MT12 and MT13).
'command' implies IORD*/IOWR* or MEMR*/MEMWR*; I/O command implies IORD* or IOWR*

CL-GD610/620 HOST CPU MEMORY READ CYCLE TIMING



NOTE-1	A CPU READ CYCLE WILL GO IN A WAIT STATE IF A CRT CYCLE IS IN PROGRESS. THE INTERLEAVE WILL DETERMINE THE WAIT LENGTH.
REF-1	DRAM O/P TURN-OFF DELAY
T_{OFF}	TYP =20/30 NS FOR 100/120 NS DRAM DEVICE.
REF-2	DRAM RAS* ACCESS TIME.
T_{RAS}	TYP =100/120 NS FOR 100/120 NS DRAM DEVICE.

NOTE-2	8/16-BIT BUS CYCLE CONTROL			
SBHE*	A0	DSELL*	DSELH*	OPERATION
0	0	0	0	16-BIT WRD
0	1	1	0	ODD BYTE
1	0	0	1	EVEN BYTE
1	1	X	X	RESERVED

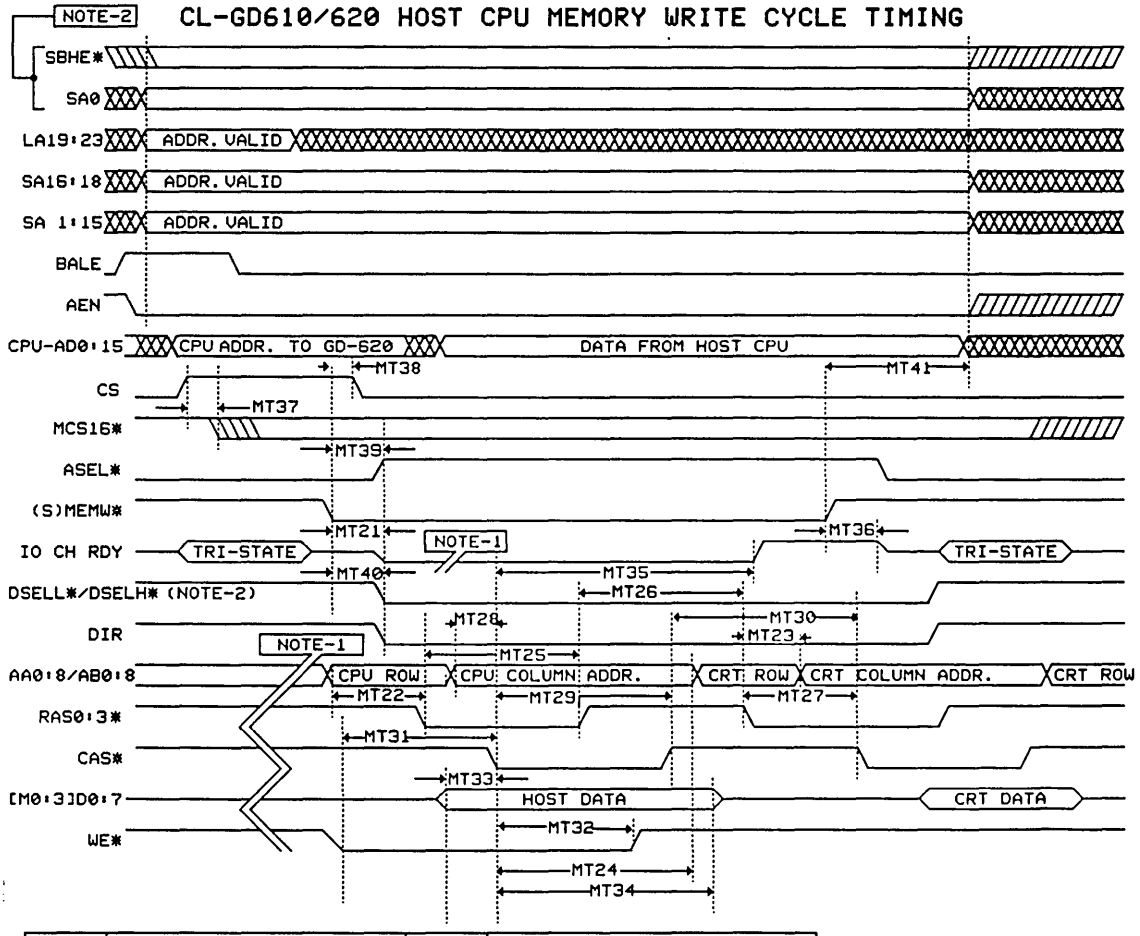
DRAM Write Timing Table

SYMBOL	PARAMETER	X:Y - Z † 1:4 - 9	1:4 - 8	1:7 - 8	3:2 - 8	1:2 - 6	1:1 - 8	1:1 - 9	ns
Tc	MCLK Cycle Time	25	30	25	30	50	50	50	Typ
MT21	CPURDY Low from MEMW*	15	15	15	15	15	15	15	Typ
MT22	Row Address Setup Time	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	Typ
MT23	Row Address Hold Time	0.5 Tc	0.5 Tc	0.5 Tc	0.5 Tc	15	15	15	Typ
MT24	Column Address Hold Time	4 Tc	3 Tc	4 Tc	3 Tc	1.5 Tc	1.5 Tc	1.5 Tc	Typ
MT25	RAS* Low Time	4 Tc	3 Tc	4 Tc	3 Tc	2 Tc	2 Tc	2 Tc	Typ
MT26	RAS* Precharge	3 Tc	3 Tc	3 Tc	3 Tc	2 Tc	2 Tc	2 Tc	Typ
MT27	RAS* to CAS* Delay	1 Tc	1 Tc	1 Tc	1 Tc	0.5 Tc	0.5 Tc	0.5 Tc	Typ
MT28	Address Setup to CAS*	5	5	5	5	5	5	5	Typ
MT29	CAS* Low Time	5 Tc	4 Tc	5 Tc	4 Tc	2.5 Tc	2.5 Tc	2.5 Tc	Typ
MT30	CAS* Precharge	2 Tc	2 Tc	2 Tc	2 Tc	1.5 Tc	1.5 Tc	1.5 Tc	Typ
MT31	WE* Setup to CAS*	1.5 Tc	1.5 Tc	1.5 Tc	1.5 Tc	1 Tc	1 Tc	1 Tc	Typ
MT32	WE* Hold from CAS* (=T47)	5 Tc	4 Tc	5 Tc	4 Tc	2.5 Tc	2.5 Tc	2.5 Tc	Typ
MT33	Data Setup to CAS*	5	5	5	5	10	10	10	Typ
MT34	Data Hold from CAS* (=T47)	5Tc	4Tc	5 Tc	4Tc	2.5 Tc	2.5 Tc	2.5	Typ
MT35	CPU Write Cycle End (=CAS* Low) to CPURDY* Inactive	2 Tc	2 Tc	2 Tc	2 Tc	2 Tc	2 Tc	2 Tc	Typ
MT36	MEMW* Inactive to CPURDY* Tristate	15	15	15	15	15	15	15	Typ
MT37	CS active to MCS16* active delay	20	20	20	20	20	20	20	Typ
MT38	CS Hold time after command	45	45	45	45	45	45	45	Max
MT39	MEMW* active to ASEL* inactive delay	40/20	40/20	40/20	40/20	40/20	40/20	40/20	Max/Typ
MT40	MEMW* active to DSELL*, DSELH* delay	58/30	58/30	58/30	58/30	58/30	58/30	58/30	Max/Typ
MT41	MEMW* to CPU write data hold time	32/16	32/16	32/16	32/16	32/16	32/16	32/16	Max/Typ

† X:Y - Z (X = CPU Cycles, Y = CRT Cycles, Z = Dots / Character)

NOTE: All times are in nanoseconds (ns) unless otherwise noted; Use parameter MT41 with I/O Port parameters BT5, BT6

CL-GD610/620 HOST CPU MEMORY WRITE CYCLE TIMING



NOTE-1	A CPU WRITE CYCLE WILL GO IN A WAIT STATE IF A CRT CYCLE IS IN PROGRESS. THE INTERLEAVE WILL DETERMINE THE WAIT LENGTH.

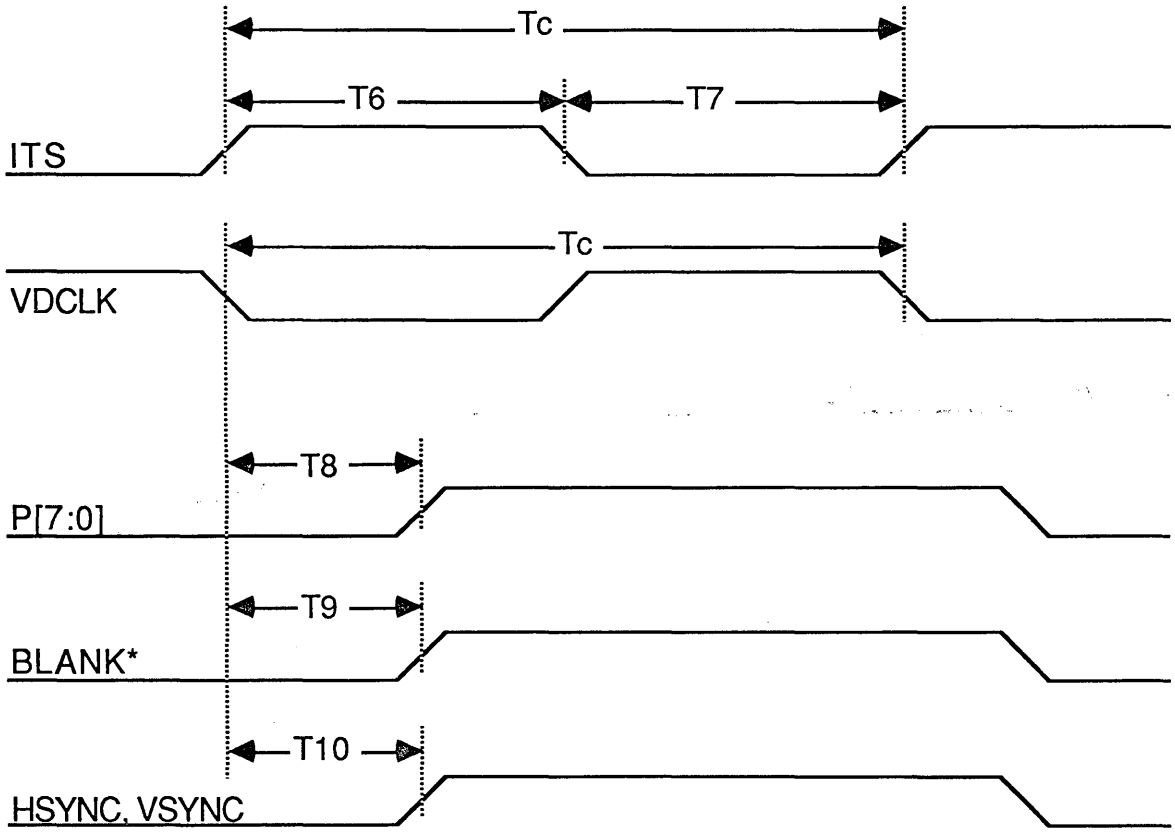
NOTE-2	8/16-BIT BUS CYCLE CONTROL				
SBHE*	A0	DSELL*	DSELH*	OPERATION
0	0	0	0	16-BIT WRD
0	1	1	0	ODD BYTE
1	0	0	1	EVEN BYTE
1	1	X	X	RESERVED

CRT Display Interface Video Timing Table

SYMBOL	PARAMETER	MIN	MAX	UNITS
Tc	ITS/VDCLK Cycle	30		ns
CT1	VDCLK High (measured @ 2.0v)	[Tc/2]-5%	[Tc/2]+5%	
CT2	VDCLK Low (measured @ 0.4v)	[Tc/2]-5%	[Tc/2]+5%	
CT3	P[7:0] Delay		15	ns
CT4	BLANK* Delay		15	ns
CT5	VSYNC, HSYNC Delay		15	ns

NOTE: ITS/VDCLK will have the same frequency as the clock selected for the current video mode. For example, when using the 610/620 internal clock mux, this could be CLK25, CLK28, CLK32, CKEXT, or OSC.

CRT Video Timing:

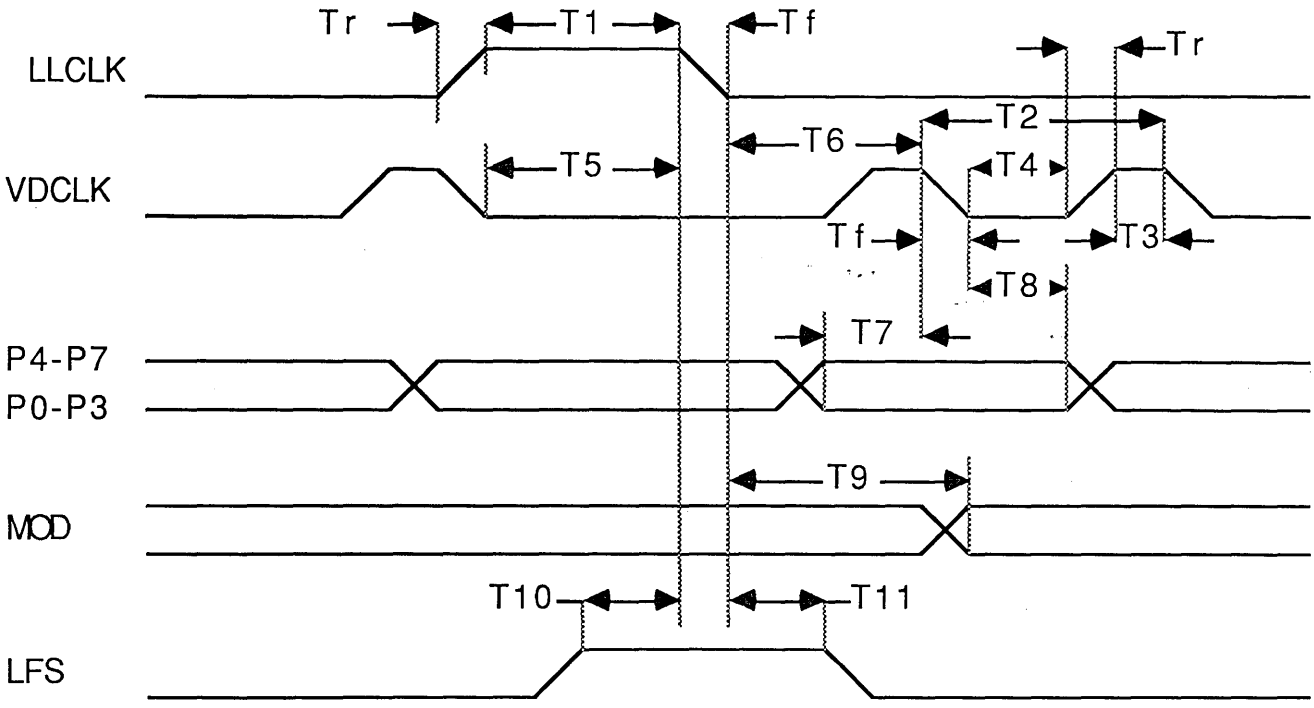


LCD Panel Interface Video Timing Table

SYMBOL	PARAMETER	MIN	MAX	UNITS
LT1	LLCLK pulse width	4Tc		ns
LT2	VDCLK cycle time	4Tc		ns
LT3	VDCLK H level width	2Tc		ns
LT4	VDCLK L level width	2Tc		ns
LT5	Clock setup time	4Tc+20		ns
LT6	Clock hold time	4Tc-20		ns
Tr,Tf	Clock rise, fall time		4	ns
LT7	Data setup time	0.5Tc		ns
LT8	Data hold time		0.5Tc	ns
LT9	MOD delay time		30	ns
LT10	LFS setup time	4Tc+15		ns
LT11	LFS hold time	4Tc-15		ns
Tc	MCLK cycle time	41.7	62.5	ns

NOTE: MCLK is 24MHz max with 5% max skew, and 16MHz min with 5% max skew

LCD Video Timing:

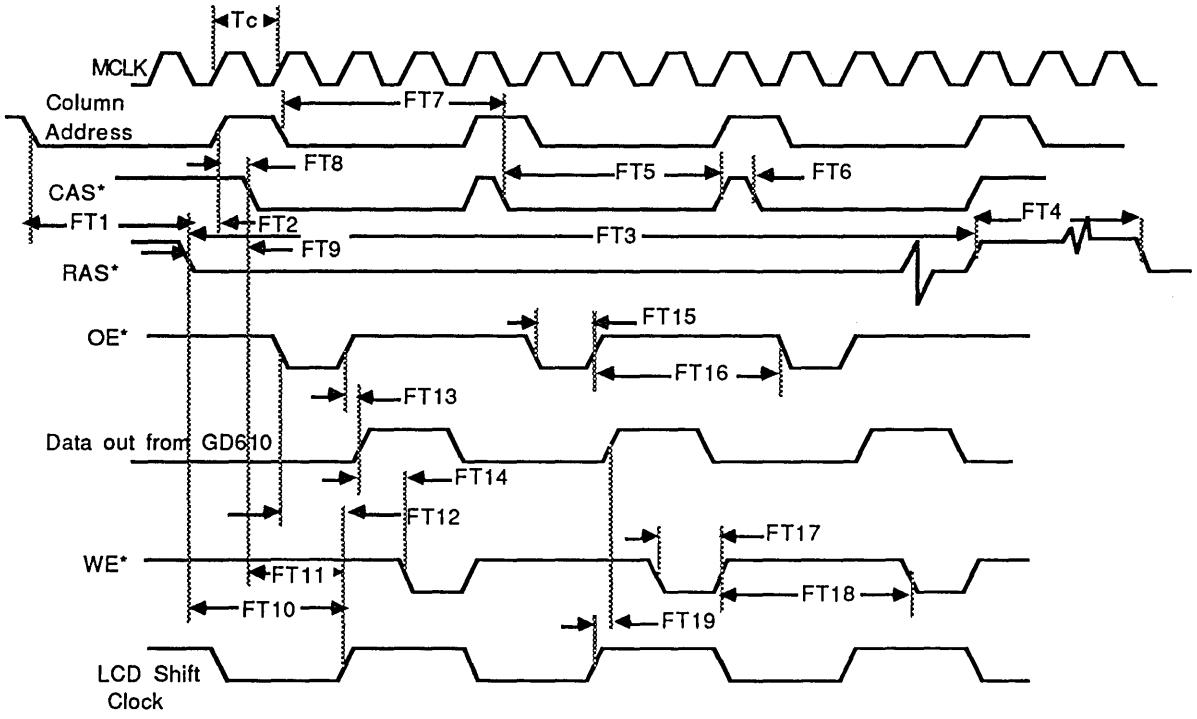


Frame Accelerator DRAM timing Table

SYMBOL	PARAMETER	MIN	MAX	UNITS
FTc	MCLK cycle (in LCD mode)	41.7	62.5	ns
FT1	Row address setup time	2 Tc		ns
FT2	Row address hold time	0.5 Tc		ns
FT3	FRRAS* L time	641 Tc		ns
FT4	FRRAS* H time	12 Tc		ns
FT5	FRCAS* L time	3.5 Tc		ns
FT6	FRCAS* H time	0.5 Tc		ns
FT7	Column address setup time to FRCAS*	0.5 Tc		ns
FT8	Column address hold time to FRCAS*	0.5 Tc		ns
FT9	FRCAS* L delay from FRRAS* L	Tc		ns
FT10	FRRAS* access time	2.5 Tc		ns
FT11	FRCAS* access time	1.5 Tc		ns
FT12	FROE* access time	Tc		ns
FT13	Data out delay from FROE*	0.5 Tc + 10		ns
FT14	Write data setup time to FRWE*	0.5 Tc - 10		ns
FT15	FROE* active pulse width	Tc		ns
FT16	FROE* inactive	1.5 Tc		ns
FT17	FRWE* active pulse width	Tc		ns
FT18	FRWE* inactive	3 Tc		ns
FT19	Data hold after LCD shift clock (VDCLK) rising edge	0.5 Tc - 10		ns
FT20	FRCAS* setup to FRRAS* during refresh	4 Tc		ns
FT21	FRRAS* L during refresh	4 Tc		ns
FT22	FRCAS* hold time after FRRAS* L during refresh	4 Tc		ns

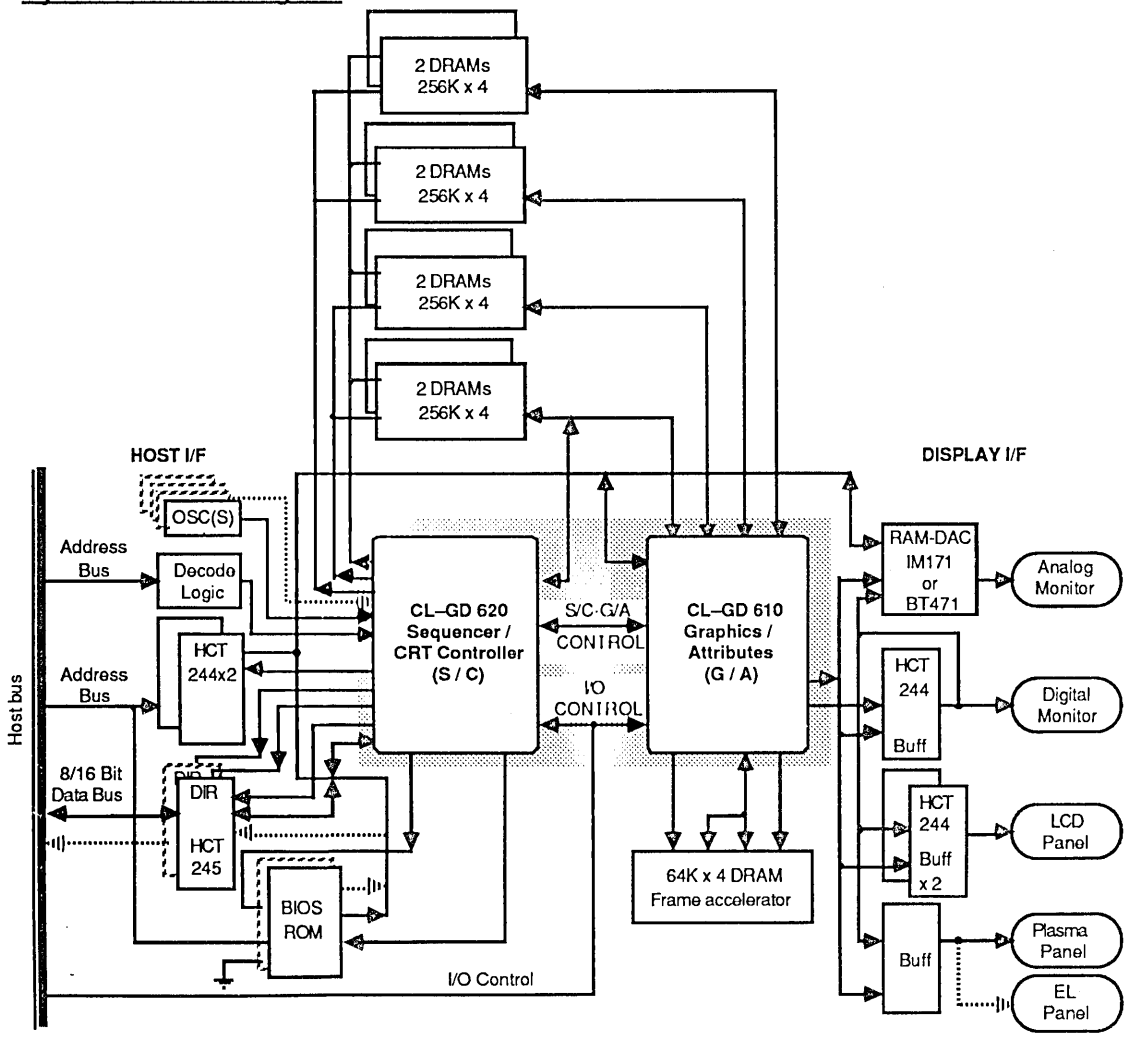
NOTE: The Frame accelerator DRAM uses page mode read-modify-write cycles and CAS before RAS refresh; The DRAM must support page mode access, and must be able to work with a maximum RAS* low time of 40 microseconds (worst-case is for a 16MHz MCLK) as FRRAS* will be low during an entire LCD line display time

Frame Accelerator Read-Modify-Write Cycle Timing:



8 TYPICAL APPLICATION

8.1 System Block Diagram



8.2 Parts List

Core Logic		16 b Interface	Display RAM
• 1	CL–GD610 Graphics / Attributes chip		• 8 256Kx4 DRAMs or
• 1	CL–GD620 Sequencer / CRT Controller chip		• 8 64Kx4 DRAMs or
• 1	BIOS (64 KB 27C512 ROM) or	• 2 27C256 ROMs	• 4 128Kx8 Pseudo
• 1	HCT245 Octal Data Bus transceiver or	• 2 HCT245	static RAMs
• 2	HCT244 Octal Address Bus buffer		
• 1	HCT244 Octal Pixel Output Bus buffer		

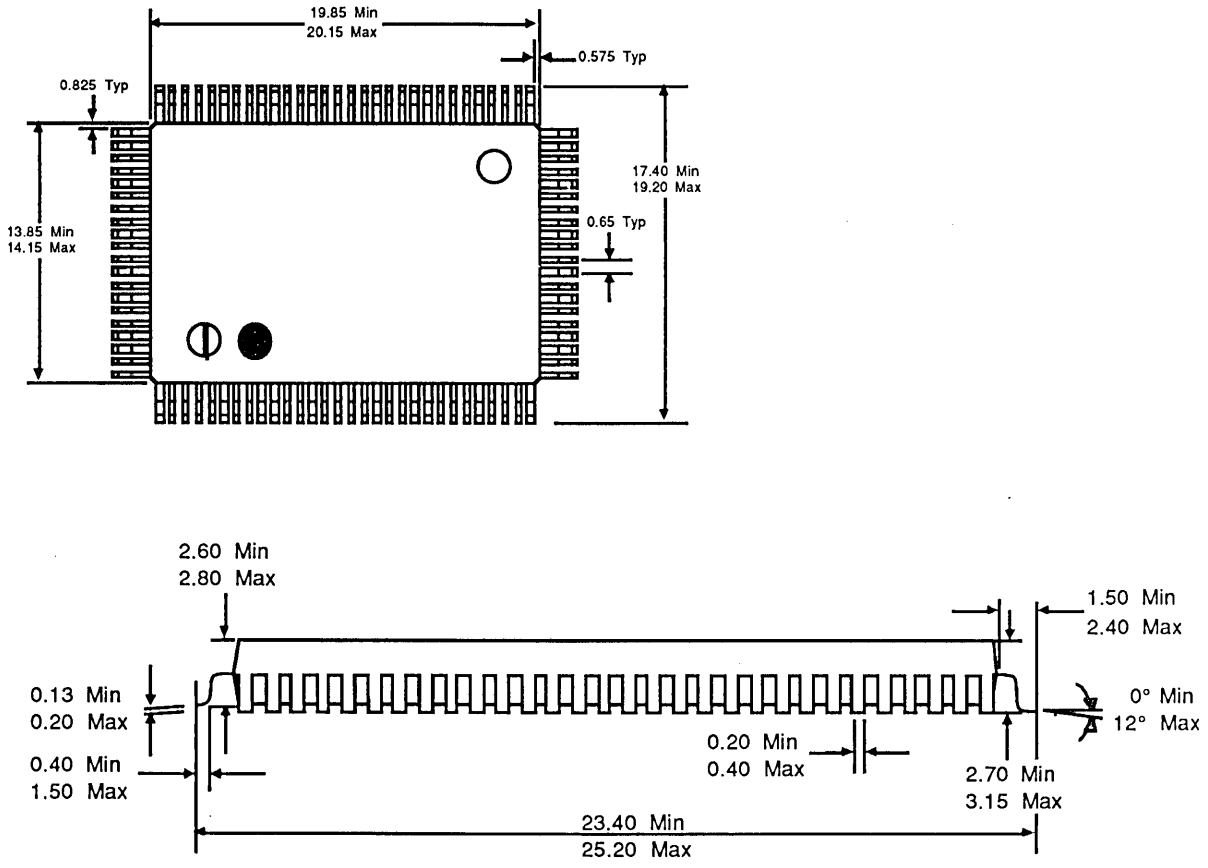
7 Core ICs for 8b I/F; 9 Core ICs for 16b I/F; 4 RAM chips for 512Kbytes or 8 RAM chips for 256Kbytes/1 Mbyte

Optional Logic

- 1/2 HCT244 Octal Pixel Output Bus buffer for LCD panel interface
- 1 Refresh accelerator (one 64Kx4 DRAM) for LCD panel interface
- 1 IMSG171 or BT471 RAMDAC or equivalent (for VGA only)
- 1 MSI device for Plasma or Electroluminescent panel interface
- 1 PLL IC to replace up to 5 crystal oscillators
- 2 Latches to demux addresses for PSRAM or SRAM from RAS,CAS
- 2 MSI devices to control latches for PSRAM/SRAM applications

9 PACKAGE INFORMATION

9.1 100-Pin QFP



Note: All dimensions are in millimeters and are nominal unless otherwise stated.

SALES DIRECTORY

Corporate Sales Offices

NORTHERN CALIFORNIA
1463 Centre Pointe Drive
Milpitas, CA 95035
Phone: (408) 945 - 8300
Telex: 171918
FAX: (408) 263 - 5682

SOUTHERN CALIFORNIA
23046 Avenida de la Carlota
Suite 600
Laguna Hills, CA 92653
Phone: (714) 472 - 3939
FAX: (714) 472 - 4804

NORTH CENTRAL AREA
5174 Pillar Creek Ave. S.E.
Kentwood, MI 49508
Phone: (616) 698 - 0475
FAX: (616) 698 - 0554

SOUTH CENTRAL AREA
17304 N. Preston Rd., Suite 800
Dallas, TX 75252
Phone: (214) 733 - 6929
FAX: (214) 733 - 6809

NORTH EASTERN AREA
210 Carnegie Center, Ste 101
Princeton, NJ 08540
Phone: (609) 520 - 9696
FAX: (609) 520 - 8731

2 Elm Square
Suite 16
Andover, MA 01810
PH: (508) 474-9300
FX: (508) 470-0499

SOUTH EASTERN AREA
3401 N. Federal Hwy, Suite 219
Boca Raton, FL 33431
Phone: (407) 750 - 4101
FAX: (407) 750 - 7237

JAPAN
1-8-16, 203, Higashi Rinkan
Sagamihara City, Kanagawa
228 JAPAN
Phone: 81 (42) 749 - 5814
FAX: 81 (42) 749 - 5814

TAIWAN
Rm 1123
No. 602 Ming Chuen E. Road
Taipei
TAIWAN, R. O. C.
Phone: (886) 2 - 718 - 4533
FAX: (886) 2 - 718 - 4526

Domestic Sales Representatives

ALABAMA

REP, INC.
11535 Gilleland Rd.
P.O. BOX 4889
Huntsville, AL 35815-0889
Phone: (205) 881-9270
FAX: (205) 882-6692

ATLANTA

REP , INC.
1944 Northlake Parkway #1
Tucker, GA 30084
Phone: (404) 938-4358
FAX: (404) 938-0194

CALIFORNIA

BESTRONICS
9683 Tierra Grande, Ste 102
San Diego, CA 92126
Phone: (619) 693 - 1111
FAX: (619) 693 - 1963

DYNAREP, Inc.
Plaza Del Lago
17220 Newhope St. Ste 211
Fountain Valley, CA 92708
Phone: (714) 545 - 3255
FAX: (714) 545 - 3717

DYNAREP, Inc.
14451 Los Angeles Ave.
Suite 301V
Simi Valley, CA 93065
Phone: (805) 527 - 0072
FAX: (805) 527 - 0433

PHASE II
2700 Augustine Dr.
Suite 239
Santa Clara, CA 95054
Phone: (408) 980-0414
FAX: (408) 980-8932

CONNECTICUT

TECHNOLOGY SALES, INC.
237 Hall Avenue
Wallingford, CT 06492
Phone: (203) 269 - 8853
FAX: (203) 269 - 2099

MASSACHUSETTS

TECHNOLOGY SALES, INC.
332 Second Avenue
Waltham, MA 02154
Phone: (617) 890 - 5700
FAX: (617) 890 - 3913

MINNESOTA

MEL FOSTER TECHNICAL SALES
P.O. Box 35216
7611 Washington Ave. So.
Edina, MN 55435
Phone: (612) 941 - 9790
FAX: (612) 944 - 0634

NEW YORK

TECHNOLOGY SALES, INC.
1777-40 Veterans Memorial Hwy
Central Islip, NY 11722
Phone: (516) 232 - 2870
FAX: (516) 232 - 2874

TECHNOLOGY SALES, INC.
470 Perinton Hills Office Park
Fairport, NY 14450
Phone: (716) 223 - 7500
FAX: (716) 223 - 5526

TECHNOLOGY SALES, INC.
145 Oakwood Lane
Ithaca, NY 14850
Phone: (607) 273 - 1188
FAX: (607) 273 - 2939

NORTH CAROLINA

REP, INC.
2500 Gateway Centre Blvd.
Suite #400
Morrisville, NC 27560
Phone: (919) 469-9997
FAX: (919) 481-3897

REP, INC.
Independence Office Park
6407 Idlewild
Suite #425
Charlotte, NC 28212
Phone: (704) 563-5554
FAX: (704) 535-7507

PENNSYLVANIA

TECHNOLOGY SALES, INC.
2300 Computer Ave. Ste J52
Willow Grove, PA 19090
Phone: (215) 784 - 0170
FAX: (215) 784 - 9201

PUERTO RICO

TECHNOLOGY SALES, INC.
Box 121
San German, PR 00753
Phone: (809) 892 - 4745
FAX: (809) 892 - 1128

TENNESSEE

REP, INC.
113 South Branner St.
P.O. Box 728
Jefferson City, TN 37760
Phone: (615) 475-4105
FAX: (615) 475-6340

Canadian Sales Representatives

HAR-TECH ELECTRONICS
5000 Dufferin Street Suite 216
Downsview, Ontario
CANADA M3H 5T5
Phone: (416) 665-7773
FAX: (416) 665-7290

HAR-TECH ELECTRONICS
39 Robertson Road, Suite 233
Nepean, Ontario
CANADA K2H 8R2
Phone: (613) 726-9410
FAX: (613) 726-8834

HAR-TECH ELECTRONICS
6600 Trans-Canada Highway
Suite 460
Pointe Claire, Quebec
CANADA H9R 4S2
Phone: (514) 694-6110
FAX: (514) 694-8501

International Sales Representatives

WEST GERMANY

SCANTEC GMBH
Behringstr. 10
8033 Planegg
FED. REPUBLIC OF GERMANY
Phone: (49) 89 - 859 - 8021
FAX: (49) 89 - 857-6574

HONG KONG

LESTINA INTERNATIONAL
Room 405, Park Tower,
15 Austin Road, Tsimshatsui
HONG KONG
Phone: (852) 3 - 7351736
FAX: (852) 3 - 7305260

JAPAN

DIA SEMICON SYSTEMS
Wacore 64, 1-37-8 Sangenjaya
Setagaya-Ku Tokyo
154 JAPAN
Phone: 81 (3) 487 - 0386
FAX: 81 (3) 487 - 8088

MARUBUN CORPORATION
8-1, Nihombashi Odemma-Cho
Chuo-Ku Tokyo
103 JAPAN
Phone: 81 (3) 639 - 9844
Telex: 252-2957
FAX: 81 (3) 661 - 7433

KOREA

CROWN CORPORATION
4F Moolim Building
993-57 Daelim-dong
Youngdeungpo-ku, Seoul
REPUBLIC OF KOREA
Phone: (82) 2 - 845 - 7289
FAX: (82) 2 - 845 - 7416

SINGAPORE

SCAN ELECTRONICS
50, Kallang Bahru #04-01/03
Kallang Basin Industrial Estate
SINGAPORE 1233
Phone: (65) 294 - 2112
Telex: RS 24983 S TECH
FAX: (65) 2961685

UNITED KINGDOM

AMEGA ELECTRONICS, LTD.
Armstrong Road, Daneshill East
Basingstoke, Hampshire
RG24 OPF ENGLAND
Phone: 0256 843166
Telex: 858297
FAX: 0256 842956

ABOUT CIRRUS LOGIC

CIRRUS LOGIC makes proprietary VLSI circuits for peripheral controller applications. Current product lines include: data communications circuits, disk drive controllers, and graphics and display controllers.

A family of products is offered in each line. Each product provides a VLSI solution to a current system design requirement. You will find CIRRUS LOGIC to be different from other semiconductor companies in the way we respond to your needs, with VLSI products that are specific to your applications.

The CIRRUS LOGIC formula combines state-of-the-art IC design automation technology with an understanding of system requirements that is uncommon in the semiconductor industry. The result is better VLSI products, with richer features, brought to market in a time frame that allows you to lead your field. Our products help you compete.

Our internally developed, proprietary S/LA™ IC design automation technology is unique in the industry.† It gives us unparalleled capability in bringing highly complex, high performance logic circuits to market in less than half the time of other semiconductor companies. But design technology is only half of the story. It is our knowledge of system requirements, and our commitment to meeting the needs of the system design engineer that makes CIRRUS LOGIC a different kind of semiconductor company. CIRRUS LOGIC offers system level solutions in silicon.

So look at our products. Talk to our systems and applications specialists. Consider the system-specific solutions that we offer, and consider how your products can benefit from the capabilities of a new kind of semiconductor company ... CIRRUS LOGIC.

† U.S. Patent No. 4,293,783

CIRRUS LOGIC, Inc. 1463 Centre Pointe Drive, Milpitas, CA 95035 PHONE 408.945.8300 FAX 263.5682 TLX 171918

1.0 Introduction

1.1 Scope of Document

This manual provides technical coverage of the CL-GD610/620 Flat panel/CRT Enhanced VGA controller chip set. Topics include the modes of operation of the Enhanced VGA controller, the major components and registers, the BIOS functions, and programming information including examples. In addition, detailed information is presented on each of the Enhanced VGA controller registers.

The following definitions are used throughout this manual:

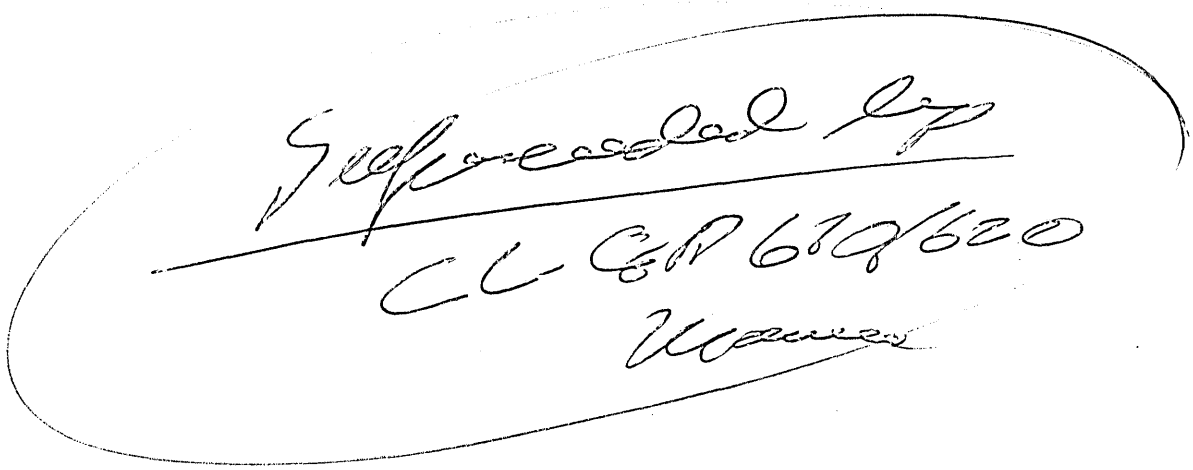
VGA	Industry Standard Video Graphics Array
EGA	Industry Standard Enhanced Graphics Adapter.
CGA	Industry Standard Color Graphics Adapter.
MDA	Industry Standard Monochrome Display Adapter.
HGC	Hercules™ Graphics Controller.
ECD	Industry Standard Enhanced Color Display.
CD	Industry Standard Color Display.
MD	Industry Standard Monochrome Display.
PS/2 Display	Industry Standard 31.5 kHz Monochrome or Color Display
MFD	Multiple-Frequency Color Display (MultiSync™, MultiScan™, etc.)
LCD	Liquid Crystal Display (typically 640x400/480 dual panel, dual line)

1.2 Chip Revisions Covered

This manual documents the following chip revisions:

1.3 Intended Audience

This manual is directed toward the technically sophisticated audience. It assumes the reader is familiar with assembly language programming on the 80286/80386 or similar microprocessor, and understands the fundamentals of video display terminology.



(This page intentionally left blank.)

3.0 Register Definition Summary

This chapter presents summary information on the registers of the 610/620 chip-set. The register name is shown first (full name and an abbreviation), along with the port address and index if applicable. Below that is a figure illustrating the register configuration and a discussion of the register contents.

Note that the GD610 has been abbreviated to G/A for Graphics/Attribute controller, and the GD620 has been abbreviated to S/C for Sequencer/CRT Controller.

Note: In all register descriptions in this document, unused bits return 0 when read.

3.1 610/620 I/O Port Summary Table

Port Addr	VGA/EGA Port	CGA Port	HGC Port
2B0/3B0	CRTC Index (RW)		6845 Index (RW)
2B1/3B1	CRTC Data (RW)		6845 Data (RW)
2B2/3B2	CRTC Index (RW)		6845 Index (RW)
2B3/3B3	CRTC Data (RW)		6845 Data (RW)
2B4/3B4	CRTC Index (RW)		6845 Index (RW)
2B5/3B5	CRTC Data (RW)		6845 Data (RW)
2B6/3B6	CRTC Index (RW)		6845 Index (RW)
2B7/3B7	CRTC Data (RW)		6845 Data (RW)
2B8/3B8			Mode Control (RW)
2B9/3B9			Set Light Pen Flip Flop (W)
2BA/3BA	Feature Control(W), Display Status(R)		Display Stams (R)
2BB/3BB	Clear Light Pen Flip Flop (W)		Clear Light Pen Flip Flop (W)
2BC/3BC	Set Light Pen Flip Flop (W)		
2BD/3BD			
2BE/3BE			
2BF/3BF			Configuration (RW)
2C0/3C0	Attribute Controller Index/Data (W), Index (R)		
2C1/3C1	Attribute Controller Index/Data (W), Data (R)		
2C2/3C2	Misc Output (W), Feature (R)		
2C3/3C3	Misc Output (W), Feature (R)		
2C4/3C4	Sequencer/Extensions Index (RW)		
2C5/3C5	Sequencer/Extensions Data (RW)		
2C6/3C6	Palette Pixel Mask (R/W)		
2C7/3C7	Palette Addr Reg R Mode (W), DAC State (R)		
2C8/3C8	Palette Address Register W Mode (RW)		
2C9/3C9	Palette Data (RW)		
2CA/3CA	Graphics 2 Position (W), Feature Control (R)		
2CB/3CB	(Reserved)		
2CC/3CC	Graphics 1 Position (W), Misc Output (R)		
2CD/3CD	(Reserved)		
2CE/3CE	Graphics Controller Index (RW)		
2CF/3CF	Graphics Controller Data (RW)		
2D0/3D0	CRTC Index (RW)	6845 Index (RW)	
2D1/3D1	CRTC Data (RW)	6845 Data (RW)	
2D2/3D2	CRTC Index (RW)	6845 Index (RW)	
2D3/3D3	CRTC Data (RW)	6845 Data (RW)	
2D4/3D4	CRTC Index (RW)	6845 Index (RW)	
2D5/3D5	CRTC Data (RW)	6845 Data (RW)	
2D6/3D6	CRTC Index (RW)	6845 Index (RW)	
2D7/3D7	CRTC Data (RW)	6845 Data (RW)	
2D8/3D8		Mode Control (RW)	
2D9/3D9		Color Select (RW)	
2DA/3DA	Feature Control(W), Display Status(R)	Display Status (R)	
2DB/3DB	Clear Light Pen Flip Flop (W)	Clear Light Pen Flip Flop (W)	
2DC/3DC	Set Light Pen Flip Flop (W)	Set Light Pen Flip Flop (W)	
2DD/3DD			
2DE/3DE			
2DF/3DF			

3.2 Color Graphics Adapter (CGA) Compatible Registers Table

Abbrev	CGA Register Name	Bits	Reg Type	Read/ Write	Reg/ Index	Port Address
MODE	Mode Control	7	G/A/S/C	R/W	--	3D8
COLOR	Color Select	6	G/A	R/W	--	3D9
STAT	Display Status	7	G/A/S/C	R	--	3DA
CLPEN	Clear Light Pen Flip Flop	0	S/C	W	--	3DB
SLPEN	Set Light Pen Flip Flop	0	S/C	W	--	3DC
CRX	6845 Index	5	S/C	R/W	--	3D4 (3D0,3D2,3D6)
R0	Horizontal Total	8	S/C	R/W	00	3D5 (3D1,3D3,3D7)
R1	Horizontal Displayed	8	S/C	R/W	01	3D5 (3D1,3D3,3D7)
R2	Horizontal Sync Position	8	S/C	R/W	02	3D5 (3D1,3D3,3D7)
R3	Sync Width	4+4	S/C	R/W	03	3D5 (3D1,3D3,3D7)
R4	Vertical Total	7	S/C	R/W	04	3D5 (3D1,3D3,3D7)
R5	Vertical Total Adjust	5	S/C	R/W	05	3D5 (3D1,3D3,3D7)
R6	Vertical Displayed	7	S/C	R/W	06	3D5 (3D1,3D3,3D7)
R7	Vertical Sync Position	7	S/C	R/W	07	3D5 (3D1,3D3,3D7)
R8	Interlace Mode	2	S/C	R/W	08	3D5 (3D1,3D3,3D7)
R9	Character Cell Height	5	S/C	R/W	09	3D5 (3D1,3D3,3D7)
RA	Cursor Start	5+2	S/C/G/A	R/W	0A	3D5 (3D1,3D3,3D7)
RB	Cursor End	5	S/C	R/W	0B	3D5 (3D1,3D3,3D7)
CRC/SAH	Start Address High	8	S/C	R/W	0C	3D5 (3D1,3D3,3D7)
CRD/SAL	Start Address Low	8	S/C	R/W	0D	3D5 (3D1,3D3,3D7)
CRE/CAH	Cursor Address High	8	S/C	R/W	0E	3D5 (3D1,3D3,3D7)
CRF/CAL	Cursor Address Low	8	S/C	R/W	0F	3D5 (3D1,3D3,3D7)
LPENH	Light Pen High	8	S/C	R/W	10	3D5 (3D1,3D3,3D7)
LPENL	Light Pen Low	8	S/C	R/W	11	3D5 (3D1,3D3,3D7)

3.3 Monochrome Graphics Adapter (MGA) Compatible Registers Table

Abbrev	MGA Register Name	Bits	Reg Type	Read/ Write	Reg/ Index	Port Address
MODE	Mode Control	7	G/A/S/C	R/W	--	3B8
STAT	Display Status	7	G/A/S/C	R	--	3BA
CONFIG	Configuration	2	G/A/S/C	R/W	--	3BF
CLPEN	Clear Light Pen Flip Flop	0	S/C	W	--	3BB
SLPEN	Set Light Pen Flip Flop	0	S/C	W	--	3B9
CRX	6845 Index	5	S/C	R/W	--	3B4 (3B0,3B2,3B6)
R0	Horizontal Total	8	S/C	R/W	00	3B5 (3B1,3B3,3B7)
R1	Horizontal Displayed	8	S/C	R/W	01	3B5 (3B1,3B3,3B7)
R2	Horizontal Sync Position	8	S/C	R/W	02	3B5 (3B1,3B3,3B7)
R3	Sync Width	4+4	S/C	R/W	03	3B5 (3B1,3B3,3B7)
R4	Vertical Total	7	S/C	R/W	04	3B5 (3B1,3B3,3B7)
R5	Vertical Total Adjust	5	S/C	R/W	05	3B5 (3B1,3B3,3B7)
R6	Vertical Displayed	7	S/C	R/W	06	3B5 (3B1,3B3,3B7)
R7	Vertical Sync Position	7	S/C	R/W	07	3B5 (3B1,3B3,3B7)
R8	Interlace Mode	2	S/C	R/W	08	3B5 (3B1,3B3,3B7)
R9	Character Cell Height	5	S/C	R/W	09	3B5 (3B1,3B3,3B7)
RA	Cursor Start	5+2	S/C/G/A	R/W	0A	3B5 (3B1,3B3,3B7)
RB	Cursor End	5	S/C	R/W	0B	3B5 (3B1,3B3,3B7)
CRC/SAH	Start Address High	8	S/C	R/W	0C	3B5 (3B1,3B3,3B7)
CRD/SAL	Start Address Low	8	S/C	R/W	0D	3B5 (3B1,3B3,3B7)
CRE/CAH	Cursor Address High	8	S/C	R/W	0E	3B5 (3B1,3B3,3B7)
CRF/CAL	Cursor Address Low	8	S/C	R/W	0F	3B5 (3B1,3B3,3B7)
LPENH	Light Pen High	8	S/C	R/W	10	3B5 (3B1,3B3,3B7)
LPENL	Light Pen Low	8	S/C	R/W	11	3B5 (3B1,3B3,3B7)

3.4 VGA/EGA Compatible Registers Table

Abbrev	EGA Register Name	Bits	Reg Type	Read/ Write	Reg/ Index	Mono Port	Color Port
MISC	Miscellaneous Output	8	G/A/S/C	W	--	3C2 (3C3)	3C2 (3C3
FC	Feature Control	3	G/A	W	--	3BA	3DA
FEAT	Feature Read (Input Status 0)	4	G/A/S/C	R	--	3C2 (3C3)	3C2 (3C3)
STAT	Display Status (Input Status 1)	7	G/A/S/C	R	--	3BA	3DA
CLPEN	Clear Light Pen Flip Flop	0	S/C	W	--	3BB	3DB
SLPEN	Set Light Pen Flip Flop	0	S/C	W	--	3BC/3B9	3DC
SRX(SQEX)	Sequencer/Extensions Index	7	G/A S/C	R/W	--	3C4	3C4
SR0	Reset	2	S/C	R/W	00	3C5	3C5
SR1	Clocking Mode	4	S/C	R/W	01	3C5	3C5
SR2	Plane Mask	4	S/C	R/W	02	3C5	3C5
SR3	Character Map Select	6	S/C	R/W	03	3C5	3C5
SR4	Memory Mode	4	S/C	R/W	04	3C5	3C5
SR6	Extensions Control	1	G/A/S/C	R/W	06	3C5	3C5
CRX	CRTC Index	5	S/C	R/W	--	3B4 (0,2,6)	3D4 (0,2,6)
CR0	Horizontal Total	8	S/C	R/W	00	3B5 (1,3,7)	3D5 (1,3,7)
CR1	Horizontal Display End	8	S/C	R/W	01	3B5 (1,3,7)	3D5 (1,3,7)
CR2	Horizontal Blanking Start	8	S/C	R/W	02	3B5 (1,3,7)	3D5 (1,3,7)
CR3	Horizontal Blanking End	5+2+1	S/C	R/W	03	3B5 (1,3,7)	3D5 (1,3,7)
CR4	Horizontal Retrace Start	8	S/C	R/W	04	3B5 (1,3,7)	3D5 (1,3,7)
CR5	Horizontal Retrace End	5+2+1	S/C	R/W	05	3B5 (1,3,7)	3D5 (1,3,7)
CR6	Vertical Total	8	S/C	R/W	06	3B5 (1,3,7)	3D5 (1,3,7)
CR7	Overflow	8	S/C	R/W	07	3B5 (1,3,7)	3D5 (1,3,7)
CR8	Screen A Preset Row Scan	7	S/C	R/W	08	3B5 (1,3,7)	3D5 (1,3,7)
CR9	Character Cell Height	5+1+1+1	S/C	R/W	09	3B5 (1,3,7)	3D5 (1,3,7)
CRA	Cursor Start	5+1	S/C	R/W	0A	3B5 (1,3,7)	3D5 (1,3,7)
CRB	Cursor End	5+2	S/C	R/W	0B	3B5 (1,3,7)	3D5 (1,3,7)
CRC	Screen A Start Address High	8	S/C	R/W	0C	3B5 (1,3,7)	3D5 (1,3,7)
CRD	Screen A Start Address Low	8	S/C	R/W	0D	3B5 (1,3,7)	3D5 (1,3,7)
CRE	Cursor Location High	8	S/C	R/W	0E	3B5 (1,3,7)	3D5 (1,3,7)
CRF	Cursor Location Low	8	S/C	R/W	0F	3B5 (1,3,7)	3D5 (1,3,7)
LPENH	Light Pen High	8	S/C	R	10	3B5 (1,3,7)	3D5 (1,3,7)
LPENL	Light Pen Low	8	S/C	R	11	3B5 (1,3,7)	3D5 (1,3,7)
CR10	Vertical Retrace Start	8	S/C	W	10	3B5 (1,3,7)	3D5 (1,3,7)
CR11	Vertical Retrace End	4+3+1	S/C	W	11	3B5 (1,3,7)	3D5 (1,3,7)
CR12	Vertical Display End	8	S/C	R/W	12	3B5 (1,3,7)	3D5 (1,3,7)
CR13	Offset	8	S/C	R/W	13	3B5 (1,3,7)	3D5 (1,3,7)
CR14	Underline Row Scan	5+1+1	S/C	R/W	14	3B5 (1,3,7)	3D5 (1,3,7)
CR15	Vertical Blanking Start	8	S/C	R/W	15	3B5 (1,3,7)	3D5 (1,3,7)
CR16	Vertical Blanking End	8	S/C	R/W	16	3B5 (1,3,7)	3D5 (1,3,7)
CR17	CRT Mode Control	8	S/C	R/W	17	3B5 (1,3,7)	3D5 (1,3,7)
CR18	Line Compare	8	S/C	R/W	18	3B5 (1,3,7)	3D5 (1,3,7)
CR22	Readback CRT Latches	8	G/A	R	22	3B5	3D5
CR24	Attribute Index Toggle	7	G/A	R	24	3B5	3D5
CR26MSB	CRTC screen A start addr MSB	2	S/C	R/W	26	3B5	3D5
CR27MSB	CRTC cursor start addr MSB	2	S/C	R/W	27	3B5	3D5
CR30-CR3F	Frame Blank	1	S/C	W	3X	3B5	3D5
CR7F	610/620 Identification	8	S/C	R	7F	3B5 (1,3,7)	3D5 (1,3,7)
GPOS1	Graphics 1 Pos(W), Misc (R)	2,8	G/A,G/A/S/C	R/W	--	3CC	3CC
GPOS2	Graphics 2 Pos (W), FeatCtrl (R)	2,3	G/A,G/A	R/W	--	3CA	3CA
GRX	Graphics Controller Index	4	G/A	R/W	--	3CE	3CE
GR0	Set/Reset	4	G/A	R/W	00	3CF	3CF
GR1	Enable Set/Reset	4	G/A	R/W	01	3CF	3CF
GR2	Color Compare	4	G/A	R/W	02	3CF	3CF

GR3	Data Rotate	5	G/A	R/W	03	3CF	3CF
GR4	Read Map Select	3	G/A	R/W	04	3CF	3CF
GR5	Mode	7	G/A	R/W	05	3CF	3CF
GR6	Miscellaneous	4	S/C	R/W	06	3CF	3CF
GR7	Color Don't Care	4	G/A	R/W	07	3CF	3CF
Abbrev	EGA Register Name	Bits	Reg Type	Read/ Write	Reg/ Index	Mono Port	Color Port
GR8	Bit Mask	8	G/A	R/W	08	3CF	3CF
ARX	Attribute Controller Index	6	G/A/S/C	R/W	--	3C0 (3C1)	3C0 (3C1)
AR0-F	Color Palette Regs 0-15	8	G/A	R/W	00-0F	3C0 (3C1)	3C0 (3C1)
AR10	Mode Control	5	G/A/S/C	R/W	10	3C0 (3C1)	3C0 (3C1)
AR11	Overscan Color	8	G/A	R/W	11	3C0 (3C1)	3C0 (3C1)
AR12	Color Plane Enable	6	G/A	R/W	12	3C0 (3C1)	3C0 (3C1)
AR13	Horizontal Pixel Panning	4	G/A	R/W	13	3C0 (3C1)	3C0 (3C1)
AR14	Color Select	4	G/A	R/W	14	3CO (3C1)	3CO (3C1)

3.5 610/620 Extension Registers (Compatible with GD510A/520A) Table

Abbreviations		Eagle VGA Register Name	Bits	Reg Type	Read. Write	Index	Port	Reset
ER0	TEST	Hardware Test	8	/S/C	RW	80	3C5	00000000
ER1	GPOS1	*Graphics 1 Position	2	G/A	R/W	81	3C5	xxxxxx00
ER2	GPOS2	*Graphics 2 Position	2	G/A	R/W	82	3C5	xxxxxx01
ER3	ARX	*Attribute Controller Index	7	G/A	R/W	83	3C5	–
ER0	WRC	Write Control	8	G/A/S/C	R/W	84	3C5	00000000
ER5	TC	Timing Control	8	S/C	R/W	85	3C5	00000x0x
ER6	BWC	Bandwidth Control	6	S/C	R/W	86	3C5	xxx10000
ER7	ROMC	ROM Control	8	S/C	R/W	87	3C5	00000000
ER8	HSYNC Skew		4	S/C	88	3C5	---	
ER9	FONTC	CMGA Font Control	6	S/C	R/W	89	3C5	---
ERA		reserved-	0	--	--	8A	3C5	---
ERB	SBPR	Screen B Preset Row Scan	5	S/C	R/W	8B	3C5	xxx00000
ERC	SBSH	Screen B Start Address High	8	S/C	R/W	8C	3C5	00000000
ERD	SBSL	Screen B Start Address Low	8	S/C	R/W	8D	3C5	00000000
ERE	GAREV	G/A Revision Code	8	G/A	R	8E	3C5	11101010
ERF	SCREV	S/C Revision Code	8	S/C	R	8F	3C5	11101010
ER10	CR10	*Vertical Retrace Start	8	S/C	R/W	90	3C5	---
ER11	CR11	*Vertical Retrace End	7	S/C	R/W	91	3C5	---
ER12	LPENH	*Light Pen High	8	S/C	R/W	92	3C5	---
ER13	LPENL	*Light Pen Low	8	S/C	R/W	93	3C5	---
ER14	PPA	Pointer Pattern Address	8	S/C	R/W	94	3C5	11111111
ER15	CADJ	Cursor Height Adjust	5	S/C	R/W	95	3C5	---
ER16	CW	Caret Width	8	G/A	R/W	96	3C5	---
ER17	CH	Caret Height	8	G/A	R/W	97	3C5	---
ER18	CXH	Caret Horizontal Position High	3	G/A	R/W	98	3C5	---
ER19	CXL	Caret Horizontal Position Low	8	G/A	R/W	99	3C5	---
ER1A	CYH	Caret Vertical Position High	2	G/A	R/W	9A	3C5	---
ER1B	CYL	Caret Vertical Position Low	8	G/A	R/W	9B	3C5	---
ER1C	PXH	Pointer Horizontal Position High	3	G/A	R/W	9C	3C5	---
ER1D	PXL	Pointer Horizontal Position Low	8	G/A	R/W	9D	3C5	---
ER1E	PYH	Pointer Vertical Position High	2	S/C	R/W	9E	3C5	---
ER1F	PYL	Pointer Vertical Position Low	8	S/C	R/W	9F	3C5	---
ER20	GRL0	Graphics Ctrlr Memory Latch 0	8	G/A	R/W	A0	3C5	---
ER21	GRL1	Graphics Ctrlr Memory Latch 1	8	G/A	R/W	A1	3C5	---
ER22	GRL2	Graphics Ctrlr Memory Latch 2	8	G/A	R/W	A2	3C5	---
ER23	GRL3	Graphics Ctrlr Memory Latch 3	8	G/A	R/W	A3	3C5	---
ER24	CLK	Clock Select	3	G/A	R/W	A4	3C5	xxx0mn00
ER25	CURS	Cursor Attributes	8	G/A/S/C	R/W	A5	3C5	00000000
ER26		-reserved-	0	--	--	A6	3C5	---
ER27	SWITCH	State Switch Control	8	G/A/S/C	R/W	A7	3C5	00000000
ER28	NMI1	NMI Mask 1	8	G/A	R/W	A8	3C5	00000000
ER29	NMI2	NMI Mask 2	8	G/A	R/W	A9	3C5	00000000
ER2A		reserved-	0	--	--	AA	3C5	---
ER2B	NSTAT1	NMI Status 1	8	G/A	R	AB	3C5	00000000
ER2C	NSTAT2	NMI Status 2	8	G/A	R	AC	3C5	00000000
ER2D		reserved-	4	S/C	--	AD	3C5	---
ER2E	CACHE	NMI Data Cache	4x24	G/A	R	AE	3C5	---
ER2F	STATE	Active Adapter State	5	G/A/S/C	R/W	AF	3C5	0x00xx00
ER30-3F	SCR0-F	Scratch Register 0-F	8	G/A	R/W	B0-BF	3C5	---
		reserved	0	---	---	C0-FF	3C5	---

* Duplicated VGA/EGA registers also accessible as extension registers for state save/restore.

1.0 Introduction

1.1 Scope of Document

This manual provides technical coverage of the CL-GD610/620 Flat panel/CRT Enhanced VGA controller chip set. Topics include the modes of operation of the Enhanced VGA controller, the major components and registers, the BIOS functions, and programming information including examples. In addition, detailed information is presented on each of the Enhanced VGA controller registers.

The following definitions are used throughout this manual:

VGA	Industry Standard Video Graphics Array
EGA	Industry Standard Enhanced Graphics Adapter.
CGA	Industry Standard Color Graphics Adapter.
MDA	Industry Standard Monochrome Display Adapter.
HGC	Hercules™ Graphics Controller.
ECD	Industry Standard Enhanced Color Display.
CD	Industry Standard Color Display.
MD	Industry Standard Monochrome Display.
PS/2 Display	Industry Standard 31.5 kHz Monochrome or Color Display
MFD	Multiple-Frequency Color Display (MultiSync™, MultiScan™, etc.)
LCD	Liquid Crystal Display (typically 640x400/480 dual panel, dual line)

1.2 Chip Revisions Covered

This manual documents the following chip revisions:

1.3 Intended Audience

This manual is directed toward the technically sophisticated audience. It assumes the reader is familiar with assembly language programming on the 80286/80386 or similar microprocessor, and understands the fundamentals of video display terminology.

4.0 CMGA Registers

The 610/620 provides additional registers, referred to as the CMGA registers, for direct hardware emulation of the CGA (Color Graphics Adapter) and MGA (Monochrome Graphics Adapter). (The MGA is also known in the industry as the Hercules Graphics Controller or HGC). These registers are accessible only while in CGA or MGA/HGC emulation mode. The registers required include some additional 'external' registers plus the 'timing registers' subset (R0-RB) of the 6845. 6845 registers RX (Index), RC-D (Screen Start Address), RE-F (Cursor Location), and R10-11 (Light Pen Address) are the same as their CRTC counterparts so are not duplicated. CRTC registers CRX, CRC-CRF, LPENH, and LPENL are used for both EGA and CMGA modes.

The additional CMGA registers are summarized in the table below:

Abbrev	Register Name	Port	Index	Access	Mode	Type
MODE	Mode Control	3?8	--	R/W	All	CMGA External
COLOR	Color Select	3D9	--	R/W	All	CGA External
CONFIG	Configuration	3BF	--	R/W	All	MGA External
R0	6845 Horizontal Total	3?5	00	R/W	Not EGA	Monitor Timing
R1	6845 Horizontal Displayed	3?5	01	R/W	Not EGA	Display Timing
R2	6845 Horizontal Sync Position	3?5	02	R/W	Not EGA	Monitor Timing
R3	6845 Sync Width	3?5	03	R/W	Not EGA	Monitor Timing
R4	6845 Vertical Total	3?5	04	R/W	Not EGA	Monitor Timing
R5	6845 Vertical Total Adjust	3?5	05	R/W	Not EGA	Monitor Timing
R6	6845 Vertical Displayed	3?5	06	R/W	Not EGA	Display Timing
R7	6845 Vertical Sync Position	3?5	07	R/W	Not EGA	Monitor Timing
R8	6845 Interlace Mode	3?5	08	R/W	Not EGA	Monitor Timing
R9	6845 Character Cell Height	3?5	09	R/W	Not EGA	Display Timing
RA	6845 Cursor Start Row	3?5	0A	R/W	Not EGA	Display Timing
RB	6845 Cursor End Row	3?5	0B	R/W	Not EGA	Display Timing

'?' in the above port addresses are 'B' in monochrome mode and 'D' in color mode.

The 6845 timing registers (R0-RB) are not accessible in VGA mode, instead the CRTC timing registers CR0-CRB are accessible at the indicated port address and index in that mode. R0-RB are accessible while in CGA, MGA, or EGATXT mode (see active state register ER2F).

The 6845 timing registers are grouped into 'Monitor Timing Registers' and 'Display Timing Registers'. These groups may be separately write protected by bits 4 and 5 of the Write Control Register at extensions index 84. The other CMGA-specific registers may be write-protected by bits 6 and 7.

See External Registers section for CMGA STAT Register definition (same as VGA Status Register 1).

See CRTC Registers section for 6845 Index Register definition (same as CRTC Index Register).

See CRTC Registers section for 6845 Registers RC-R11 (same as CRTC Registers CRC-CR11).

4.1 CMGA Mode Register: MODE

I/O Port Address: 3?8

Protection Bits: WRC[7]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Page (MGA only)	R/W	Reset or write to port w/ CONFIG D1=0 or non-MGA	0
6	-unused-			
5	Blink Enable	R/W	Reset	0
4	High-Res Graphics (CGA only)	R/W		0
3	Video Enable	R/W	Reset	0
2	Monochrome (CGA only)	R/W		0
1	Graphics	R/W	Reset or CONFIG D0=0	0
0 (lsb)	High-Res Text (CGA only)	R/W		0

Bit Descriptions

Bit 7 Page (MGA only)

State 1 = Page 1 (display memory at B8000-BFFFF)

State 0 = Page 0 (display memory at B0000-B7FFF)

Bit 6 unused

Bit 5 Text Blink Enable

State 1 = Enable text character blink for characters with blink attributes set (attribute msb = 1)

Bit 4 Hi-Res Graphics (CGA only)

State 1 = 640x200 2-color mode

State 0 = all other modes (must be 0 in text mode in an IBM CGA; don't care in text mode in the 610/620)

Bit 3 Video Enable

State 1 = Display Video Enabled (use to turn off video while changing 6845 parameters to prevent screen glitches)

State 0 = Display Blank (if extensions TC register bit-5 is set in CGA Text mode, display remains enabled)

Bit 2 Monochrome (CGA only)

State 1 = Monochrome

State 0 = Color

Bit 1 Graphics Mode

State 0 = Text mode: character width = 8 (CGA) or 9 (MGA)

State 1 = Graphics mode

When in text mode, certain attribute patterns are detected by hardware:

b000i000	= No display (black)	
b000i001	= Underline	MGA only (line 13)
b000i111	= Normal Video	
b111i000	= Reverse Video	
b111i111	= No display (white)	CGA only
bBBBifff	= Normal character	CGA only

Where:

BBB	= background
fff	= foreground

b = blinking

i = intensified

All other attribute values are ignored in CMGA modes. EGA modes interpret attribute bits 0-3 as foreground (character) color and bits 4-7 as background color. EGA modes use CR17 to determine where underlining appears.

Bit 0 High-Res Text (CGA only)

State 1 = 80x25

State 0 = 40x25 (divide character clock by 2)

if bit-4 = 1, this bit is a don't care (normal clock rate)

Note: This register is effective only in MGA and CGA modes (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

4.2 CMGA Color Register: COLOR

I/O Port Address: 3D9

Protection Bits: WRC[7]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	Color Set Number	R/W		
4	Intensity	R/W		
3	Color Bit-3 (Intensity)	R/W		
2	Color Bit-2 (Red)	R/W		
1	Color Bit-1 (Green)	R/W		
0 (lsb)	Color Bit-0 (Blue)	R/W		

This register is provided for CGA compatibility.

Bit Descriptions

Bit 7 unused

Bit 6 unused

Bit 5 CGA Palette Number: This bit determines which of two available CGA palettes are used according to the following table (where 'color number' is the 2-bit pixel value in 320x200 CGA graphics mode):

Pixel Value	Color No.	CGA Palette 0	CGA Palette 1
0 0	Color 0	Determined by bits 0-3	Determined by bits 0-3
0 1	Color 1	Green	Cyan
1 0	Color 2	Red	Magenta
1 1	Color 3	Brown	White

This bit is defined for CGA 320x200 graphics mode only and is a don't care otherwise.

Bit 4 Intensity

In text mode, this bit enables intensified background colors.

In graphics 320x200 mode, this bit enables intensified colors 0-3.

In graphics 640x200 mode, this bit is a don't care.

Bit 3-0 Color

In text mode, these bits determine the border color.

In 320x200 4-color mode, they determine the background color (color 0).

In 640x200 2-color mode, they determine the foreground color (the color when the pixel value is 1). The background color is black (pixel value = 0).

Note: This register is effective only in CGA mode (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register). In EGA mode, the Attribute Controller controls the video data path; in CGA mode, special CGA hardware (which includes this register) controls the video data path; in MGA mode, special MGA hardware controls the video data path.

4.3 CMGA Configuration Register: CONFIG

I/O Port Address: 3BF

Protection Bits: WRC[7]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	-unused-			
3	-unused-			
2	-unused-			
1	Page 1 Enable	R/W	Reset	0
0 (lsb)	Graphics Mode Enable	R/W	Reset	0

This register is provided for MGA compatibility.

Bit Descriptions

Bit 7 unused

Bit 6 unused

Bit 5 unused

Bit 4 unused

Bit 3 unused

Bit 2 unused

Bit 1 Page 1 Enable

State 1 = Pages 0 & 1 enabled ('Full' mode 64K wrap)

State 0 = Page 0 enabled only ('Half' mode 32K wrap) ('Diag' mode)

Writes to MODE register will cause bit 7 to capture 0 if this bit is 0 (for MDA compatibility).

Bit 0 Graphics Mode Enable

State 1 = Graphics Mode (720 x 348)

State 0 = Text Mode (4K wrap) ('Diag' mode)

This bit forces MODE register (port 3B8) bit-1 to zero (graphics mode bit) if this bit is 0 (for MDA compatibility) and if in MGA mode.

Note: If both bits are off (the default state on reset), the MGA is in "DIAG" mode and accesses to display memory by the CPU wraparound every 4K within the 32K space from B0000-B7FFF (MDA compatibility mode).

4.4 6845 Horizontal Total Register: R0

I/O Port Address: 3?5
Index: 00
Protection Bits: WRC[4]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Horizontal Displayed Bit-7	R/W		
6	Horizontal Displayed Bit-6	R/W		
5	Horizontal Displayed Bit-5	R/W		
4	Horizontal Displayed Bit-4	R/W		
3	Horizontal Displayed Bit-3	R/W		
2	Horizontal Displayed Bit-2	R/W		
1	Horizontal Displayed Bit-1	R/W		
0 (lsb)	Horizontal Displayed Bit-0	R/W		

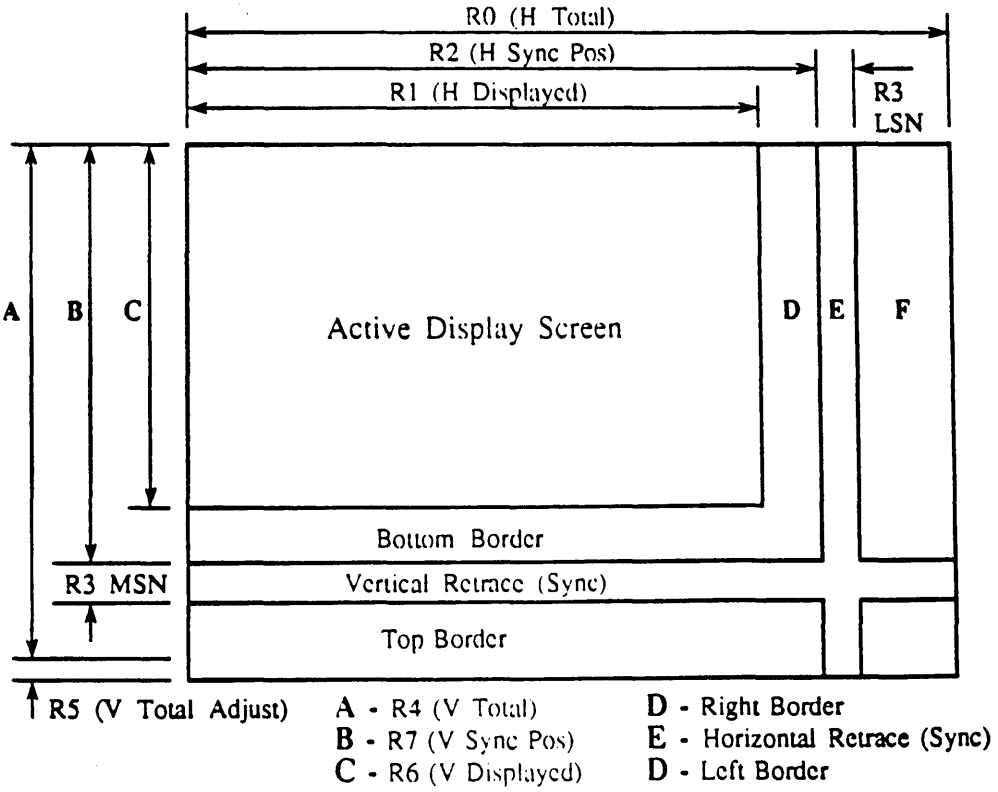
The Horizontal Total register defines the total number of characters in a horizontal scan line, including the retrace time. The character clock input to the device is counted by a character counter. The value of the character counter is compared with the value in this register to provide the horizontal timing. All horizontal and vertical timing is based upon the contents of this register.

The value in the register = Total Number of Characters - 1 (value must be > 0).

In Interlace Mode (see register R8), some 6845 chips require that this register be programmed to an odd number (i.e., an even number of character times). The 610/620 allows even or odd values in interlace mode, but requires odd values in scan doubling mode.

Note: This register is effective only in MGA and CGA modes (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

Figure 4-1: 6845 Timing Registers



4.5 6845 Horizontal Displayed Register: R1

I/O Port Address: 3?5

Index: 01

Protection Bits: WRC[5]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Horizontal Displayed Bit-7	R/W		
6	Horizontal Displayed Bit-6	R/W		
5	Horizontal Displayed Bit-5	R/W		
4	Horizontal Displayed Bit-4	R/W		
3	Horizontal Displayed Bit-3	R/W		
2	Horizontal Displayed Bit-2	R/W		
1	Horizontal Displayed Bit-1	R/W		
0 (lsb)	Horizontal Displayed Bit-0	R/W		

The Horizontal Displayed register defines the total number of displayed characters in a horizontal line.

The value in the register = Total Number of Characters Displayed (value must be R0)

Refer to Figure 4-1 (see register R0) for a summary of 6845 timing registers.

Note: This register is effective only in MGA and CGA modes (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

4.6 6845 Horizontal Sync Position Register: R2

I/O Port Address: 3?5

Index: 02

Protection Bits: WRC[4]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Horizontal Sync Position Bit-7	R/W		
6	Horizontal Sync Position Bit-6	R/W		
5	Horizontal Sync Position Bit-5	R/W		
4	Horizontal Sync Position Bit-4	R/W		
3	Horizontal Sync Position Bit-3	R/W		
2	Horizontal Sync Position Bit-2	R/W		
1	Horizontal Sync Position Bit-1	R/W		
0 (lsb)	Horizontal Sync Position Bit-0	R/W		

The contents of this register define the start position of the horizontal sync pulse in terms of horizontal character clocks assuming character positions are numbered starting with 0 as the first displayed character at the left side of the screen. The register value must be less than or equal to the value in R0.

Refer to Figure 4-1 (see register R0) for a summary of 6845 timing registers.

Note: This register is effective only in MGA and CGA modes (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

4.7 6845 Sync Width Register: R3

I/O Port Address: 3?5
Index: 03
Protection Bits: WRC[4]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Vertical Sync Width Bit-3	R/W		
6	Vertical Sync Width Bit-2	R/W		
5	Vertical Sync Width Bit-1	R/W		
4	Vertical Sync Width Bit-0	R/W		
3	Horizontal Sync Width Bit-3	R/W		
2	Horizontal Sync Width Bit-2	R/W		
1	Horizontal Sync Width Bit-1	R/W		
0 (lsb)	Horizontal Sync Width Bit-0	R/W		

The contents of bits 0-3 of this register define the width of the horizontal sync pulse. The value is defined in terms of the number of horizontal character clocks.

The contents of bits 4-7 of this register define the width of the vertical sync pulse in terms of raster scan lines. A value of 1-15 in these bits indicates a vertical sync pulse width of 1-15 raster scan lines. For compatibility with some 6845 chips which do not implement these bits, a value of 0 indicates a vertical sync pulse width of 16 scan lines. For scan-doubling mode (see the Timing Control register at extensions index 85), a given value in this field will produce a vertical sync pulse with twice the normal number of raster scan lines.

Refer to Figure 4-1 (see register R0) for a summary of 6845 timing registers.

Note: This register is effective only in MGA and CGA modes (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

4.8 6845 Vertical Total Register: R4

I/O Port Address: 3?5
Index: 03
Protection Bits: WRC[4]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	Vertical Total Bit-6	R/W		
5	Vertical Total Bit-5	R/W		
4	Vertical Total Bit-4	R/W		
3	Vertical Total Bit-3	R/W		
2	Vertical Total Bit-2	R/W		
1	Vertical Total Bit-1	R/W		
0 (lsb)	Vertical Total Bit-0	R/W		

This register, along with the Vertical Total Adjust register (R5), the Character Cell Height register (R9), and the scan doubling bit, determines the total number of scan lines per frame. The value programmed into this register is defined in terms of character rows, but varies according to the current interlace mode (see register R8):

Normal/Interlace Modes: Rows - 1
Interlace Sync & Video Mode: (Rows/2) - 1

The value in this register is not affected by scan-doubling mode (see the Timing Control register at extensions index 85.

Refer to Figure 4-1 (see register R0) for a summary of 6845 timing registers.

Note: This register is effective only in MGA and CGA modes (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

4.9 6845 Vertical Total Adjust Register: R5

I/O Port Address: 3?5
Index: 05
Protection Bits: WRC[4]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	Vertical Total Adjust Bit-4	R/W		
3	Vertical Total Adjust Bit-3	R/W		
2	Vertical Total Adjust Bit-2	R/W		
1	Vertical Total Adjust Bit-1	R/W		
0 (lsb)	Vertical Total Adjust Bit-0	R/W		

This register, along with the Vertical Total register (R4) determines the vertical scan frequency (typically either 50 or 60 Hz). It is programmed with the number of scan lines required to get exactly the rate desired. This is derived by calculating the total number of scan lines required per field and dividing by the number of scan lines per character cell. The integer part of the result is programmed into R4 and the fractional part into R5.

The value programmed into this register is the same independent of the current interlace mode (see register R8). Scan doubling mode doubles the number of added scan lines per field.

Refer to Figure 4-1 (see register R0) for a summary of 6845 timing registers.

Note: This register is effective only in MGA and CGA modes (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

4.10 6845 Vertical Displayed Register: R6

I/O Port Address: 3?5
Index: 06
Protection Bits: WRC[5]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-	-		
6	Vertical Displayed Bit-6	R/W		
5	Vertical Displayed Bit-5	R/W		
4	Vertical Displayed Bit-4	R/W		
3	Vertical Displayed Bit-3	R/W		
2	Vertical Displayed Bit-2	R/W		
1	Vertical Displayed Bit-1	R/W		
0 (lsb)	Vertical Displayed Bit-0	R/W		

The Vertical Displayed register specifies the number of displayed character rows on the CRT screen. The value in this register should be less than or equal to the contents of R4 (Vertical Total) plus one.

The value programmed into this register varies according to the current interlace mode (see register R8):

Normal/Interlace Modes: Rows
Interlace Sync & Video Mode: Rows/2

The value in this register is not affected by scan-doubling mode.

Refer to Figure 4-1 (see register R0) for a summary of 6845 timing registers.

Note: This register is effective only in MGA and CGA modes (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

4.11 6845 Vertical Sync Position Register: R7

I/O Port Address: 3?5
Index: 07
Protection Bits: WRC[4]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	Vertical Sync Position Bit-6	R/W		
5	Vertical Sync Position Bit-5	R/W		
4	Vertical Sync Position Bit-4	R/W		
3	Vertical Sync Position Bit-3	R/W		
2	Vertical Sync Position Bit-2	R/W		
1	Vertical Sync Position Bit-1	R/W		
0 (lsb)	Vertical Sync Position Bit-0	R/W		

This register controls the position of vertical sync and is programmed in character rows assuming the character rows are numbered starting from 0 as the first row of characters at the top of the screen. When the programmed value of this register is increased, the display position of the CRT screen is shifted up. When the programmed value is decreased, the display position is shifted down. Any number less than or equal to the vertical total (R4) and greater than or equal to the vertical displayed (R6) may be used.

The value programmed into this register varies according to the current interlace mode (see register R8):

Normal/Interlace Modes: Row Position
Interlace Sync & Video Mode: Row Position/2

The value in this register is not affected by scan-doubling mode (see the Timing Control register at extensions index 5, port 3C9)..

Refer to Figure 4-1 (see register R0) for a summary of 6845 timing registers.

Note: This register is effective only in MGA and CGA modes (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

4.12 6845 Interlace Mode Register: R8

I/O Port Address: 3?5

Index: 08

Protection Bits: WRC[4]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	-unused-			
3	-unused-			
2	-unused-			
1	Interlace Mode Bit-1	R/W		
0 (lsb)	Interlace Mode Bit-0	R/W		

This register specifies the interlace mode according to the following table:

Bit-1	Bit-0	Interlace Mode
0	0	Normal Sync (Non-Interlace)
0	1	Interlace Sync Mode
1	0	Normal Sync (Non-Interlace)
1	1	Interlace Sync and Video Mode

Normal Sync

Only one field is available. Each scan line is refreshed at the vertical frequency.

Interlace Sync

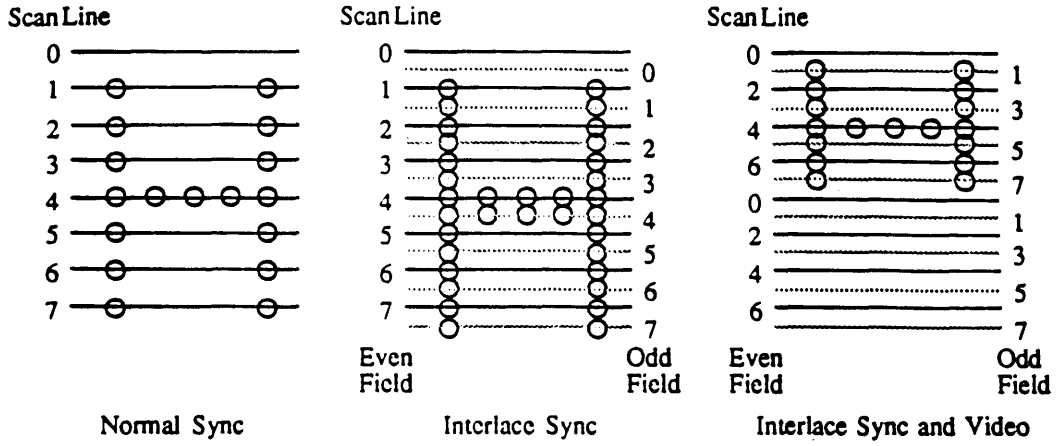
The same information is painted in both fields. This is a useful mode for filling in a character to enhance readability. In this mode, some 6845 chips require the horizontal total register (R0) to be odd (i.e., an even number of character times). This is not a restriction in the 610/620.

Interlace Sync & Video

Alternating lines are displayed in the even field and the odd field. This effectively doubles the given bandwidth of the CRT Monitor. In this mode, some 6845 chips require the cursor start and end registers (RA and RB) to both be even or both be odd, depending on which field the cursor is to be displayed in. This is not a restriction in the 610/620. A full block cursor will be displayed in both odd and even fields when the cursor end register (RB) is programmed to a value greater than that in the character cell height register (R9).

In CGA mode, registers R4, R6, and R7 must be programmed to half the actual number required (the even numbered scan lines are displayed in the even field and the odd numbered scan lines are displayed in the odd field).

Figure 4-2: 6845 Interlace Mode Summary



In the even field of both interlace modes, the VSYNC position is delayed by half a scan line (plus half a character if R0 contains an even value) to shift the display so that the lines of the odd field are displayed between the lines of the even field. Also, an extra scan line is added to the end of the blanking time in the even field if the number of scan lines (determined by R4 (vertical total) and R9 (scan lines per row)) is even, so that the period between VSYNC pulses will be constant. Therefore, the number of scan lines per frame (2 fields) is odd.

Use of the interlace modes is only practical if the monitor used has a long persistance phosphor. Otherwise a perceptible flicker will be present on the display. This flicker effect is due to the doubling of the refresh time for all scan lines since each field is displayed alternately. Each scan line is therefore effectively refreshed at 25 or 30 Hz instead of 50 or 60 Hz, which is slow enough that the off time between scans can be detected. The CRT phosphor must be persistant enough to eliminate this off time in order to eliminate flicker. Some typical CRT phosphors and characteristics are shown in the table below:

Type	Color	Persistance	Decay to 10% Brightness	Burn Resistance	Interlace
Operation P4	(W) White	Medium	60 microseconds	Moderate	Not suitable
P31 (GH)	Green	Short	38 microseconds	Good	Not suitable
P39 (GR)	Yellowish Green	Long	150 milliseconds	Poor	OK

Note that P39 is not suitable for data displays in which the format is fixed for long periods of time.

Interlace and Scan Line Doubling:

Scan line doubling mode converts the interlace modes to non-interlace modes in which all the scan lines from the even and odd fields are displayed on every field. This still doubles the number of scan lines per field, but leaves the same number of lines per frame as non-scan-line-doubling mode, except that the extra scan line per frame (which otherwise exists when the number of scan lines is even in interlace modes) is not added.

Note: This register is effective only in MGA and CGA modes (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

4.13 6845 Character Cell Height Register: R9

I/O Port Address: 3?5

Index: 09

Protection Bits: WRC[5]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	Character Cell Height Bit-4	R/W		
3	Character Cell Height Bit-3	R/W		
2	Character Cell Height Bit-2	R/W		
1	Character Cell Height Bit-1	R/W		
0 (lsb)	Character Cell Height Bit-0	R/W		

This register specifies the number of scan lines per character row per the following table:

No Scan Line Doubling	Fields/ Frame	Scan Lines/Row In Each Field	Scan Lines/Row Displayed per Frame	Data Lines/Row Displayed per Frame
Non-Interlace	2	R9 + 1	R9 + 1	R9 + 1
Interlace	2	R9 + 1	2(R9 + 1)	R9 + 1
Sync & Video	2	(R9 + 1)/2	R9 + 1	R9 + 1
Scan Line Doubling				
Non-Interlace	2	2(R9 + 1)	2(R9 + 1)	R9 + 1
Interlace	2	2(R9 + 1)	2(R9 + 1)	R9 + 1
Sync & Video	2	R9 + 1	R9 + 1	R9 + 1

Some 6845 chips, including the Motorola MC6845 used in the IBM CGA, restrict the value in R9 to be an odd number in interlace sync and video mode (i.e., an even number of scan lines). In the 610/620 chip set, this restriction does not apply.

For scan-doubling mode (see the Timing Control register at extensions index 85), a given value in this register will produce twice the normal number of raster scan lines.

Note: This register is effective only in MGA and CGA modes (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

4.14 6845 Cursor Start Register: RA

I/O Port Address: 3?5

Index: 0A

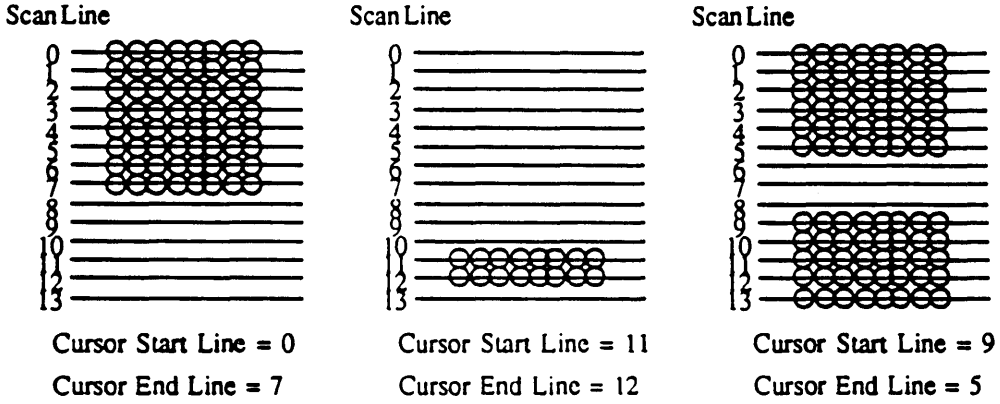
Protection Bits: WRC[5]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	Cursor Display Mode Bit-1	R/W		
5	Cursor Display Mode Bit-0	R/W		
4	Cursor Start Bit-4	R/W		
3	Cursor Start Bit-3	R/W		
2	Cursor Start Bit-2	R/W		
1	Cursor Start Bit-1	R/W		
0 (lsb)	Cursor Start Bit-0	R/W		

Bit Descriptions

Bits 0-4 of this register specify the scan line of a character row where the cursor is to begin assuming the lines of the character rows are numbered 0-31:

Figure 4-3: 6845 Cursor Programming Examples



Bits 5-6 of this register determine the cursor display mode according to the following table:

Bit-6	Bit-5	Cursor Mode (6845 Chip Spec)	Actual Cursor Mode in CGA and MGA	610/620 Cursor
0	0	**No Cursor Blink**	Cursor Blink (1/16 of the field rate)	Fast Blink
0	1	**No Cursor Display**	No Cursor Display	No Cursor Display
1	0	**Fast Blink** (1/16 of the field rate)	No Cursor Display	No Cursor Display
1	1	**Slow Blink** (1/32 of the field rate)	Blink at intermittant rate	Slow Blink

The reason that the 6845 cursor display mode and the actual cursor display mode are different is that there is external circuitry on the CGA and MGA that blinks the cursor at 1/16 of the current field rate (exactly out of phase with the 6845 blink mechanism). Therefore, the 6845 cursor display mode must be set to 'no blink' or 'no cursor' and there is normally no way to turn off cursor blink in the CGA and MGA. The 610/620 provides control over the external blink mechanism, however, to allow the full 6845 blink control capability to be used (see extension register ER25, Cursor Attributes Register). The 610/620 emulates the actual CGA and MGA cursor blink operation exactly except for the intermittent blink (slow blink occurs instead).

Note that displaying a blinking cursor over a blinking character can result in apparently erratic blink operation.

Note: This register is only effective in MGA and CGA modes and in a special Autoswitch mode called 'EGA Text' mode (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register). See also the description of 610/620 extension register ER15 (Cursor Height Adjust Register) for special interpretation of this register by hardware in 'EGA Text' Autoswitch mode.

Note: Bits 6:5 are implemented in the 610 (write only) for functional operation and are effective only in CMGA and NOT in 'EGA TEXT'.

4.15 6845 Cursor End Register: RB

I/O Port Address: 3?5
Index: 0B
Protection Bits: WRC[5]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	Cursor End Bit-4	R/W		
3	Cursor End Bit-3	R/W		
2	Cursor End Bit-2	R/W		
1	Cursor End Bit-1	R/W		
0 (lsb)	Cursor End Bit-0	R/W		

The Cursor End register specifies the scan line of the character row where the cursor is to end assuming the lines of the character rows are numbered 0-31. Refer to Figure 4-3 for cursor size programming examples (see register RA).

The Cursor Start and End registers allow a cursor up to 32 scan lines high to be placed on any scan line of the character block. The values in the Start and End registers define the height of the cursor.

In Interlace Sync & Video mode for some 6845 chips, the cursor start and end registers must both be even or both be odd, depending on which field the cursor is to be displayed in. In the 610/620, this is not a restriction.

A full block cursor will be displayed in both odd and even fields when the cursor end register is programmed to a value greater than that in the character cell height register (R9).

For scan-doubling mode (see the Timing Control register at extensions index 85), the values in the cursor start and end registers are interpreted as 'logical' scan lines, where there are two physical scan lines for every one logical scan line. Or, looking at it another way, the register values are interpreted as twice the value programmed with the actual character cell height also being twice the normal number of scan lines. The cursor height will always be an even number of scan lines in scan doubling mode.

Note: This register is only effective in MGA and CGA modes and in a special Autoswitch mode called 'EGA Text' mode (see the description of 610/620 'Active Adapter State' Register at extensions index AF). See also the description of 610/620 Cursor Adjust Register (extensions index 95) for special interpretation of this register by hardware in 'EGA Text' Autoswitch mode.

5.0 VGA/EGA External Registers

The external registers are those not contained in the other major functional blocks (Sequencer, Attributes Controller, Graphics Controller, and CRT Controller). These registers are called external due to being external to the LSI chips that implement these functions in the IBM VGA/EGA.

Abbrev	Register Name	Port Addresses
MISC	Misc Output Register	3C2 (W), 3CC (R)
FC	Feature Control Register	3?A (W), 3CA (R)
FEAT	Input Status Register 0 (Feature Read)	3C2 (R)
STAT	Input Status Register 1 (Display Status)	3?A (R)
CLPEN	Clear light pen flip flop	3?B (W)
SLPEN	Set light pen flip flop	3B9/3BC/3DC(W)

Note: '?' in the above port address is 'B' in monochrome mode and 'D' in color mode

Light Pen

The actual data value written to the 'Set/Clear Light Pen Flip Flop' ports is ignored. Any write to these ports sets or clears the Light Pen Flip Flop. The Light Pen Flip Flop is also set by an active-low pulse on the light pen connector strobe input. If the Light Pen Flip Flop is clear, setting it by either method also causes the CRT Controller Light Pen Registers (LPENH and LPENL) to be loaded from the current memory address. The current state of the Light Pen Flip Flop may be read as bit-1 of Input Status Register 1 (Display Status).

Write Control (WRC) register bit-6 (extensions register ER4) is used to write-protect these two ports. If the bit is set, writes to the SLPEN and CLPEN ports are ignored.

5.1 Miscellaneous Output Register: (MISC)

I/O Port Address: 3C2 (W)

Index: I/O Port 3CC(R)

Protection Bits: Write Protected by WRC[3,0]

Bit #	Description	Write Protect	3C2 Access	3CC Access	Reset By	Reset State
7 (msb)	Vertical Retrace Polarity	WRC[0]	W	R	Hard Reset	0
6	Horizontal Retrace Polarity	WRC[0]	W	R	Hard Reset	0
5	Page Select	WRC[3]	W	R	Hard Reset	0
4	Disable External Video Drivers	WRC[3]	W	R	Hard Reset	1
3	Clock Select Bit-1	WRC[0]	W	R	Hard Reset	0
2	Clock Select Bit-0	WRC[0]	W	R	Hard Reset	0
1	Enable RAM	WRC[3]	W	R	Hard Reset	0
0 (lsb)	CRTC I/O Address	WRC[3]	W	R	Hard Reset	0

This register is normally write-only at I/O port 3C2 in the standard EGA. Reading I/O port 3C2 returns the contents of the Feature Read Register (FEAT) (also called Input Status 0). For state save/restore and VGA compatibility, the 610/620 allows this register to also be read at I/O port 3CC.

Bit Descriptions

Bit 7 Vertical Retrace Polarity

State 0 = active high (positive)

State 1 = active low (negative)

Bit 6 Horizontal Retrace Polarity

State 0 = active high (positive)

State 1 = active low (negative)

Note: Bits 7 and 6 affect retrace polarity in EGA mode only (see the extensions TC register for polarity control in CMGA modes)

Bit 5 Page Bit for Odd/Even

This bit acts as the lsb of the display memory address when in the 'Odd/Even' modes (SR4 bit-2 = 1).

State 0 = selects odd memory locations

State 1 = selects even locations. This bit is set for modes 0, 1, 2, 3, and 7.

Bit 4 Disable External Video Drivers

State 0 = activates

and

State 1 = de-activates the LS244 video driver chip located on the board external to the 610/620 chip set.

The LS244 chip normally drives the 9-pin video output connector when no feature cards are installed. Disabling the external video driver chip allows the feature connecter to drive the video output connector pins instead. This bit appears as the 'INTERNAL*' pin of the 610 'G/A' chip.

Bit 3-2 Clock Select

These bits select the clock source and dipswitch section as follows:

D3	D2	Switch	Clock Source
0	0	4	Selects 14.318 MHz clock from the system bus
0	1	3	Selects 16.257 MHz clock from an on-board oscillator
1	0	2	Selects 25.172 MHz clock from an on-board oscillator or an external clock source from the feature connector (jumper selectable)
1	1	1	Selects 32.514 MHz clock
			Selects 40.000 MHz clock

This field has been extended to a 3-bit field in the Clock Select (CLK) register (extension register ER24) by duplicating these 2 bits at that register and adding a new msb. This field should not be changed except during synchronous reset (SRO bit-1 = 0).

Bit 1 Enable RAM

State 0 = the RAM is disabled from access by the processor.

State 1 = the RAM will respond at addresses set by the value programmed into the Control Data Select of the Graphics Controller.

Bit 0 CRTC I/O Address

This bit selects I/O addresses for monochrome or color mode.

State 0 = sets the CRTC to 3BxH and the Input Status Register 1 to 3BAH (monochrome mode).

State 1 = sets the CRTC to 3DxH and the Input Status Register 1 to 3DAH (color mode).

5.2 Feature Control Register: FC

I/O Port Address: 3?A(W)

Index: I/O Port 3CA (R)

Protection Bits: Write Protected by WRC[3]

Bit #	Description	3?A Access	3CA Access	Reset By	Reset State
7 (msb)	8-bit Video Out	W	R		
6	-unused-				
5	-unused-				
4	-unused-				
3	-reserved - (CRTC Interlace)	(W)	(R)		
2	-unused-				
1	Feature Ctrl Bit 1 (Feature Connector Pin 20)	W	R		
0 (lsb)	Feature Ctrl Bit 0 (Feature Connector Pin 21)	W	R		

This register is normally write-only at I/O port 3?A in the standard EGA. Reading I/O port 3?A returns the contents of the Display Status Register (STAT) (also called Input Status 1). For state save/restore and VGA compatibility, the 610/620 allows this register to also be read at I/O port 3CA.

Bit Descriptions

Bit 7 8-bit Video

State 1 = video output bits 6 and 7 are enable. Video output bits 6 and 7 use the same pins as Feature Code input bits 0 and 1 (see bits 5 and 6 of the Feature Read registeer). Therefore, when this bit is 1, the feature connector feature code inputs become extra video output bits instead, which appear on the feature connector.

State 0 = the feature code inputs perform their normal function.

Bit 6 Unused

Bit 5 Unused

Bit 4 Unused

Bit-3 Reserved - this bit is reserved for control of CRTC interlace

Bit-2 Unused

Bit 1-0 These bits convey information to the feature connector. The output of these bits goes to the feature connector as signals FC0 (pin 21) and FC1 (pin 20). These bits are for general-purpose use. A typical application is for LCD back-panel power control in a laptop computer.

5.3 Input Status Register 0 (Feature Read): FEAT

I/O Port Address: 3C2

Bit #	Description	Chip	Access	Reset By	Reset State
7 (msb)	CRT Interrupt	S/C	R		
6	Feature Code Bit-1 (Feature Conn Pin 17)	G/A	R		
5	Feature Code Bit-0 (Feature Conn Pin 19)	G/A	R		
4	Switch Sense	G/A	R		
3	-unused-	G/A	R		
2	-unused-	G/A	R		
1	-unused-	G/A	R		
0 (lsb)	-unused-	G/A	R		

Bit Descriptions

Bit 7 CRT Interrupt

State 0 = indicates no IRQ2 interrupt is pending.

State 1 = indicates an IRQ2 interrupt is active.

CRTC register 11 (CR11) bit-5 enables CRT interrupts to occur at the leading edge of vertical sync if it is set to 0.

Note: A CRT Interrupt does not properly indicate that the CRT Controller is requesting service of a frame interrupt. IBM's implementation has this signal connected directly to the IRQ2 Bus. If other boards use IRQ2, this bit may be a "1" even if a CRT interrupt is not pending. For compatibility, the 610/620 duplicates this behavior.

Bit 6-5 Feature Code

These bits are input from the feature connector as signals FEAT0 (pin 19) and FEAT1 (pin 17). If Feature Control (FC) register bit-7 is set to 1, these bits indicate the state of video output bits 6 and 7 (FEATO and FEAT1 input pins become VIDEO7 and VIDEO6 output pins instead.)

Bit 4 Switch Sense

This bit reads the configuration DIP switches, positions 1-4 or 1-8. The contents of the CLKSEL field determine which switch is currently selected. This bit reads 0 if the selected switch is closed and 1 if it is open. Since the CLKSEL field also selects the current clock, the switch states are generally only read by power-up initialization code. The switch configuration for switches 1-4 may be subsequently determined by reading bits 0-3 of byte 40:88h in system RAM.

CLKSEL = 0	Switch 4	(IBM EGA standard)
CLKSEL = 1	Switch 3	(IBM EGA standard)
CLKSEL = 2	Switch 2	(IBM EGA standard)
CLKSEL = 3	Switch 1	(IBM EGA standard)
CLKSEL = 4	Switch 5	(Cirrus Logic Extension)
CLKSEL = 5	Switch 6	(Cirrus Logic Extension)
CLKSEL = 6	Switch 7	(Cirrus Logic Extension)
CLKSEL = 7	Switch 8	(Cirrus Logic Extension)

The CLKSEL field is a 2-bit field in Miscellaneous Output Register bits D2-D3. This allows switches 1-4 to be selected for read at this register. The CLKSEL field is extended to a 3-bit field in bits D2-D4 of the Clock Select (CLK) Register (see extensions register ER24) by duplicating bits D2-D3 of the MISC register and adding a new msb. The extension CLKSEL msb is cleared by writing to the standard 2-bit CLKSEL field in the MISC output register at the 3C2 I/O port.

5.4 Input Status Register 1 (Display Status): STAT

I/O Port Address:3?A

Bit #	Description	Chip	Access	Reset By	Reset State
7 (msb)	Not Vertical Retrace (MGA compatible)	G/A	R		
6	-unused-	G/A	-		
5	Diagnostic Use Bit-1 (EGA compatible)	G/A	R		
4	Diagnostic Use Bit-0 (EGA compatible)	G/A	R		
3	Vertical Retrace (CGA,EGA)/Real-time Pixel Data (MGA)	G/A	R		
2	Light Pen Switch	S/C	R		
1	Light Pen Flip Flop	S/C	R	Reset	0
0 (lsb)	Display Enabled	G/A	R		

Bit Descriptions

Bit 7 Not Vertical Retrace

State 0 indicates that vertical retrace is in progress.

Bit 6 Unused

Bit 5-4 Diagnostic Usage

These bits are connected to 2 of the 8 outputs of the Attribute Controller. The selection of one of the 4 pairs is controlled by bits 5-4 of the Color Plane Register. Note that the arrangement below matches the Chips and Technologies implementation of these bits, not IBM's which has 01 and 10 reversed (IBM's EGA Technical Reference Manual matches the table but their hardware doesn't).

Color Plane Register		Input Status Register 1 (Display Status)	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	Video 2 - Red	Video 0 - Blue
0	1	Video 3 - Secondary Blue (B')	Video 1 - Green
1	0	Video 5 - Secondary Red (R')	Video 4 - Secondary Green (G')
1	1	Video 7 - Test	Video 6 - Test

Bit 3 CGA/EGA: Vertical Retrace: 1 = indicates that vertical retrace is in progress.

MGA: Video Data: Real-time video pixel data (secondary blue/video)

Bit 2 Light Pen Switch

State 0 = indicates that the light pen switch is closed (on).

State 1 = indicates that the light pen switch is open (off).

Bit 1 Light Pen Flip Flop:

State 0 = indicates that a light pen trigger pulse has not been received.

State 1 = indicates that a pulse has been received (and that LPENH/LPENL contain a valid address value). Receiving a light pen trigger pulse may be simulated under software control by writing to the SLPEN and CLPEN I/O ports (3B9 & 3BB for the MGA, 3DC & 3DB for the CGA, and 3?C & 3?B for the EGA) to set and clear this flip flop respectively.

The change of this bit from 0 to 1 loads the light pen address registers LPENH and LPENL from the current video memory address. This is independent of whether the bit is set by software or hardware.

Bit 0 Display Enable

State 0 = indicates display of video data is enabled

State 1 = indicates that a vertical or horizontal retrace interval is in progress

This bit is the inverse of the DE (Display Enable) pin of the chip set.

6.0 VGA/EGA Sequencer Registers

The Sequencer generates memory timing for the display RAMs and the character clock for controlling display memory refresh reads.

Abbrev	Register Name	Port Address	Index	Access
SRX/SQEX	Sequencer/Extensions Index Register	3C4		R/W
SR0	Reset	3C5	00	R/W
SR1	Clocking Mode	3C5	01	R/W
SR2	Plane Mask	3C5	02	R/W
SR3	Character Map Select	3C5	03	R/W
SR4	Memory Mode	3C5	04	R/W
SR6/EXTC	Extensions Control	3C5	06	R/W

Note: The above registers are effective only in EGA/VGA mode (refer to extension register ER2F). In CGA and MGA modes, the sequencer is forced into a preselected mode of operation, independent of the values in the above listed registers. The sequencer registers may be accessed while in non-EGA/VGA modes of operation, however the values don't have any effect on sequencer operation until the 610/620 VGA is returned to EGA/VGA mode.

Note: Sequencer registers 0-4 are write-protected by bit 3 of the extensions Write Control register (ER4).

Sequencer Operation

The sequencer generates all display memory timing including RAS and CAS to the display memory chips. It also refreshes display memory. During each horizontal scan, display memory accesses alternate between CRT accesses and CPU accesses in a ratio controlled by the current bandwidth setting (see Bandwidth Control Register at extensions index 86). When display enable ends at the end of each horizontal scan line (after the proper number of displayed characters have been read), CRT accesses are not required until the start of the next scan line, so the cycles are free for other use. The first five are used by the sequencer to generate refresh accesses to display memory; the next two are used if required to read graphics pointer pattern information; the remaining cycles are available for access by the CPU. The total number of cycles (character clocks) available during each horizontal blanking interval (CR0-CR1+1 in CRTC modes and R0-R1+1 in 6845 modes) typically ranges from 13 (EGA 350-line mode) to 34 (CGA text mode). If the number of cycles drops below 7, the graphics pointer may not be used; if it drops below 5, display memory may not be adequately refreshed. This is typically no problem for CRT monitors built using current technology.

6.1 Sequencer/Extensions Index Register: SQEX/SRX

I/O Port Address: 3C4

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Sequencer/Extensions Index Bit-7 (msb)	R/W		
6	-unused-			
5	Extensions Index Bit-5	R/W		
4	Extensions Index Bit-4	R/W		
3	Extensions Index Bit-3	R/W		
2	Sequencer/Extensions Index Bit-2	R/W		
1	Sequencer/Extensions Index Bit-1	R/W		
0 (lsb)	Sequencer/Extensions Index Bit-0 (lsb)	R/W		

The Sequencer/Extensions Index Register points to the Sequencer registers and to the 610/620 Extensions registers. The three least significant bits determine the Sequencer register which will be pointed to in the next register read/write operation. The five least significant bits determine the Extension register which will be pointed to in the next register read/write operation.

If the msb of the Index register is set to 0, or access to the extension registers is disabled, the Sequencer registers will be accessed per the three lsbs of the index. If the index register msb is set to 1 and write access to the extension registers is enabled, the 610/620 extension registers will be accessed per the 5 lsbs of the index.

In other words, if extensions access is disabled, the original sequencer registers SR0-4 plus the new SR6 may be accessed anywhere in the range of indices from 00 to FF (0 same as 8, 10, 18, etc.). If extensions are enabled, sequencer registers SR0-4 and SR6 are accessed in 8-register blocks from 00 to 7F only and the new extension registers are accessed at 80-FF (C0-FF are reserved for future use and currently repeat registers 80-BF).

6.2 Sequencer Reset Register: SRO

I/O Port Address: 3C5
Index: 00
Protection Bits: Write Protected by WRC[3]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	-unused-			
3	-unused-			
2	-unused-			
1	Synchronous Reset*	R/W		
0 (lsb)	Asynchronous Reset*	R/W		

Bit Descriptions

Bit 1 Synchronous Reset*

Setting this bit to 0 causes the sequencer to clear synchronously and halt (disabling display memory RAM refresh and display refresh). Setting this bit to 1 causes the sequencer to run unless D0 (asynchronous reset) is cleared to 0. Both reset register bits must be "1" to allow the sequencer to operate. In order to preserve display memory contents, this bit should be left set to 0 only for short periods of time (a few tens of microseconds at most). The following registers should not be changed unless this bit is 0:

Clocking Mode Register (SR1) bits 0 and 3
Misc Output Register bits 2-3
Extensions CLK Register bits 2-4
Extensions BWC (Bandwidth Control) Register bits 0-2
Extensions TC (Timing Control) Register bits 0-1

Setting this bit to 0 also causes various 610/620 extension registers to be reset to their power-on state: TC bit-1 (character width extension), BWC bits 0-2, SBPR, SBSH, SBSL, CURS, CR9[7] (scan doubling enable) and CR14[6] (doubleword). The clearing of these bits occurs at the transition of the synchronous reset bit from 1 to 0.

Bit 0 Unused in the 610/620 chip set

CR17	**[7]**	(0)	Enable H/V Retrace	TEST	[0-4]	(00)	Chip Test
CR11	**[5]**	(0)	Disable Vertical Intrpt	WRC	[0-7]	(00)	Write Protect
CR11	**[4]**	(0)	Don't Clear Vert Intrpt	TC	[1]	(0)	Character Width Extension
SR6	**[0]**	(0)	Extensions Enable	BWC	[0-2]	(0)	Bandwidth Control
SR3	**[0-5]**	(00)	Character Map Select	ROMC	[7]	(0)	ROM Disable
STAT	**[1]**	(0)	Light Pen Flip Flop	SBPR	[0-4]	(00)	Screen B Preset Rowscan
MISC	**[4]**	(1)	Disa Ext Video Drivers	SBSH	[0-7]	(00)	Screen B Start High
CONFIG	**[0]**	(0)	MGA Graphics Enable	SBSL	[0-7]	(00)	Screen B Start Low
CONFIG	**[1]**	(0)	MGA Page 1 Enable	PPA	[0-7]	(FF)	Pointer Pattern Addr
MODE	**[7]**	(0)	MGA Page Bit	CURS	[0-7]	(00)	Cursor Attributes
MODE	**[5]**	(0)	CMGA Blink Enable	SWITCH	[0-7]	(00)	State Switch Control
MODE	**[3]**	(0)	CMGA Video Enable	NMI1	[0-7]	(00)	NMI Control 1
MODE	**[1]**	(0)	CMGA Graphics Mode	NMI2	[0-7]	(00)	NMI Control 2
GPOSO	**[0-1]**	(0)	Graphics Position 0	NSTAT1	[0-7]	(00)	NMI Status 1
GPOS1	**[0-1]**	(1)	Graphics Position 1	NSTAT2	[0-7]	(00)	NMI Status 2
CLK	**[2-4,7]**	(10)	Clock Control	STATE	[0-7]	(04)	State Control

6.3 Sequencer Clocking Mode Register: SR1

I/O Port Address: 3C5

Index: 01

Protection Bits: Write Protected by WRC[3]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	-unused-			
3	Dot Clock (1 = divide master clock by 2)	R/W		
2	Shift Load	R/W		
1	Bandwidth (0 = 1:4, 1 = 3:2 interleave)	R/W		
0 (lsb)	8/9 Dot Clocks (0 = 9 dots, 1 = 8 dots)	R/W in S/C W only in G/A		

Bit Descriptions

Bit 3 Dot Clock

State 0 = selects the Sequencer master clock input to be output on the Dot Clock output pin.

State 1 = causes the master clock to be divided by 2 to generate the dot clock. As the dot clock is the primary clock used by the system, all other timings will be stretched as they are derived from the dot clock. Dot clock divided by 2 is used for 320 x 200 modes (except 256-color mode).

Bit 2 Shift Load

State 0 = causes the display serializers in the Graphics Controller to be reloaded every character clock.

State 1 = causes the display serializers in the Graphics Controller to be reloaded every other character clock. This mode is useful when 16 bits are fetched every memory cycle and chained together in the shift registers. This bit is typically only set for monochrome graphics modes.

Bit 1 Bandwidth

State 0 = 1:4 interleave

State 1 = 3:2 interleave

This bit selects the ratio of display memory accesses allowed by the CPU relative to accesses by EGA/VGA hardware to refresh the CRT display. Higher resolution modes must fetch more data from memory in a given period of time to refresh the CRT display, so allow the CPU to access display memory less often. The bandwidth bit is therefore provided to allow selection of the best possible performance for the current mode of operation. The only allowable selections in the IBM EGA and VGA are via this bit: a setting of 0 indicates that a memory access by the CPU may occur only once for every 4 CRT accesses (referred to as 1:4 interleave) and a setting of 1 indicates that CPU memory accesses may occur 3 times for every 2 CRT accesses (3:2 interleave). Note: 3:2 interleave does not currently support 9 dots per character.

In addition, the bandwidth control mechanisms have been extended in the 610/620 via a new 3-bit field in the BWC register (Bandwidth Control) at extensions index 86. The new field allows a wider selection of bandwidth settings than are available in the standard EGA to accommodate new high resolution modes. If the bandwidth control field of the BWC register is set to 0, the bandwidth control bit in the Sequencer Clocking Mode register works as described to select between

1:4 and 3:2 interleave. If the bandwidth control field is non-zero, it selects additional bandwidth control settings.

Refer to the BWC register (extensions index 86) for additional detail.

Bit 0 8/9 Dot Clocks

State 0 = causes the Sequencer to generate character clocks which are 9 dots wide.

State 1 = causes the sequencer to generate character clocks which are 8 dots wide. The IBM modes that use 9-dot wide character clocks are monochrome text mode (720 x 350 resolution), and the new VGA 400-line text modes (9x16 font, 40x25 and 80x25 text modes). All other standard modes use 8 dot wide character clocks.

For compatibility, this bit is implemented the same as the standard EGA and VGA, but has been extended to a 3-bit field in extension register TC (Timing Control) at index 5 by duplicating this bit in that register and adding two initially 0 msbs. This allows more character width selections including 6 bits for implementing 132-column text modes. If this register is written, the added extension register bits are reset. If the extension register is written, this bit is changed according to the lsb of the value written into the field.

Refer to the description of the TC register at extensions index 85 for additional information.

6.4 Sequencer Plane Mask (Map Mask) Register: SR2

I/O Port: 3C5

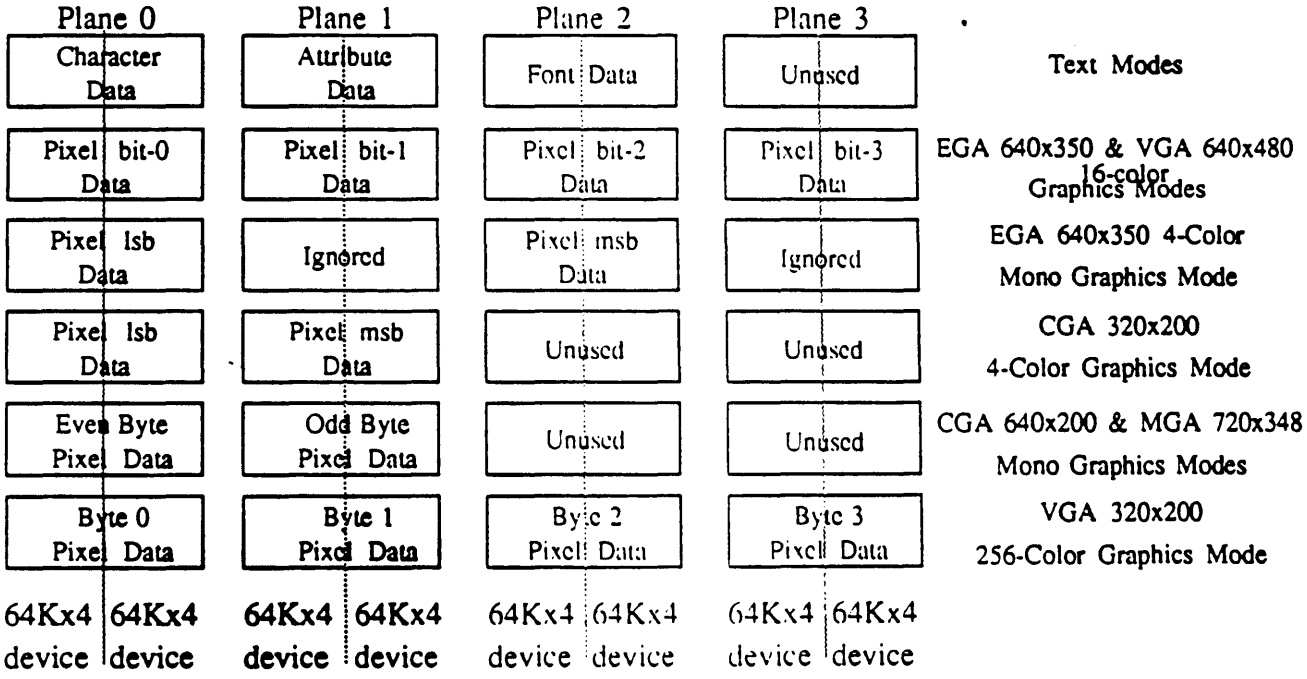
Index: 02

Protection Bits: Write Protected by WRC[3]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Reserved for future use			
6	Reserved for future use			
5	Reserved for future use			
4	Reserved for future use			
3	Enable Plane 3	R/W		
2	Enable Plane 2	R/W		
1	Enable Plane 1	R/W		
0 (lsb)	Enable Plane 0	R/W		

A "1" in any of the bits 0 through 3 enables the CPU to write to the corresponding memory planes 0 through 3. When this register is loaded with 0Fh, the CPU can do a 32-bit write operation in one memory cycle.

Figure 6-1: Display Memory Plane Mapping



In EGA 4-bit per pixel graphics modes, planes 0-3 each contain 1 bit of the pixel value (this register is set to x'F). In text modes, this register should be set to 3 (the CPU needs to access planes 0 and 1; the font information is retrieved directly by hardware independent of the contents of this register).

When odd/even modes are selected (by clearing bit 2 of the Memory Mode register) planes 0/1 and planes 2/3 should have the same plane mask value.

The effective value in this register is 3 (planes 0 and 1 enabled) in CGA and MGA text and graphics modes. The actual contents of this register are unchanged; a constant value is effectively substituted for this register in CMGA modes of operation.

6.5 Sequencer Character Map Select Register: SR3

I/O Port: 3C5

Index: 03

Protection Bits: Write Protected by WRC[3]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	Secondary Character Map Select bit-0 (lsb)	R/W	Reset	0
4	Primary Character Map Select bit-0 (lsb)	RW	Reset	0
3	Secondary Character Map Select bit-2 (msb)	R/W	Reset	0
2	Secondary Character Map Select bit-1	R/W	Reset	0
1	Primary Character Map Select bit-2 (msb)	R/W	Reset	0
0 (lsb)	Primary Character Map Select bit-1	R/W	Reset	0

Bit Descriptions

Bit 3,2,5 Secondary Character Map Select

These bits select the bank used to generate alpha characters when attribute bit-3 is "1" according to the following table:

D3	D2	D5	Font#	Table Location
0	0	0	0	1st 8K of Plane 2
0	0	1	1	2nd 8K of Plane 2
0	1	0	2	3rd 8K of Plane 2
0	1	1	3	4th 8K of Plane 2
1	0	0	4	5th 8K of Plane 2
1	0	1	5	6th 8K of Plane 2
1	1	0	6	7th 8K of Plane 2
1	1	1	7	8th 8K of Plane 2

Bit 1,0,4 Primary Character Font Select

These bits select the plane used to generate alpha characters when attribute bit-3 is "0" according to the following table:

D1	D0	D4	Font#	Table Location
0	0	0	0	1st 8K of Plane 2
0	0	1	1	2nd 8K of Plane 2
0	1	0	2	3rd 8K of Plane 2
0	1	1	3	4th 8K of Plane 2
1	0	0	4	5th 8K of Plane 2
1	0	1	5	6th 8K of Plane 2
1	1	0	6	7th 8K of Plane 2
1	1	1	7	8th 8K of Plane 2

In alphanumeric modes, bit-3 of the attribute byte normally turns the foreground intensity on or off. This bit may be redefined to be a switch between character sets. This function is enabled when there is a difference between the values of Primary and Secondary Character Map Select bits. Whenever the two values are the same, the character select function is disabled.

The format of Plane 2 font address bits 15-0 is: F2 F1 F0 C7 C6 C5 C4 C3 C2 C1 C0 R4 R3 R2 R1 R0 where F2-0 is the font # (D3/2/5 or D1/0/4), C7-0 is the character code, and R4-0 is the character row adddress. In the EGA, F0 (D4 and D5) is not implemented and is effectively always 0, limiting selection to only 4 of the 8 potential font storage areas of

plane 2 (the even numbered fonts in the tables above).

This register (along with the character attribute value) determines where font information is located for EGA and VGA text modes. For CGA or MGA text modes, which normally expect font information to be contained in ROM, the FONTC register (Font Control) at extensions index 89 determines where the font information is located.

6.6 Sequencer Memory Mode Register: SR4

I/O Port: 3C5

Index: 04

Protection Bits: Write Protected by WRC[3]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	-unused-			
3	Chain4	R/W in S/C W only in G/A		
2	Odd/Even* (0=Text/CGA, 1=MGA/EGA graphics)	R/W		
1	Extended Memory (0=64KB RAM, 1=256KB RAM)	R/W		
0 (lsb)	Text Mode (0=Graphics, 1=Text)	R/W		

Bit Descriptions

Bit 7-4 unused

Bit 3 Chain4 (double odd/even)

This bit is provided for compatibility with the VGA and should always be set to 0 by EGA programs.

When this bit is 1, A0 provides plane select bit-0 and A1 provides plane select bit-1. This is like odd/even mode, except that A1 is used as well as A0. This bit takes priority over bit-2 (odd/even); when this bit is set to 1, bit-2 has no effect.

There is no separate bit in the Graphics Controller to select double odd/even mode as is the case with the odd/even bit; this bit is used for both.

The Graphics Controller Read Map register is ignored when this bit is 1. This bit controls plane selection for both reads and writes.

Bit 2 Odd/Even*

Setting this bit to 0 will put the sequencer into the odd/even mode.

"0" directs even CPU addresses to access planes 0 and 2 while odd CPU addresses access planes 1 and 3. "1" causes CPU addresses to sequentially access data within a bit plane. The planes are accessed according to the value in the Sequencer Plane Mask Register (SR2).

This bit should be set to 0 for text modes. This bit should also be set to 0 when emulating CGA graphics mode with EGA hardware.

The function of this bit should track the function of bit-4 of the Graphics Controller Mode Register (GR5 Odd/Even bit). Note: the binary values will be opposite.

Bit 1 Extended Memory

256KB display memory is standard on the 610/620 board, so this bit is usually set to 1. This bit may, however, be set to 0 to allow emulation of IBM EGA modes which assume a display memory size of 64KB.

Bit 0 Text Mode

State 0 = indicates that graphics mode is active.

State 1 = indicates that text (alphanumeric) mode is active. This bit enables the Character Map Select Register (SR3).

6.7 Extensions Control Register: (EXTC) SR6

I/O Port: 3C5

Index: 06

Bit#	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	-unused-			
3	-unused-			
2	-unused-			
1	-unused-			
0 (lsb)	Extensions Access Enable	R from GA	Reset	0

Access to the extended registers of the 610/620 chip set (registers pointed to by Sequencer indices 80-BF) is enabled and disabled by issuing write operations to port address 3C5 with an index of 6 stored in the Sequencer/Extensions Index Register. Access is enabled by writing hex 0CAH; access is disabled by writing 0ACH. Reading from 3C5 with an index of 6 stored in the index register returns the state of the access enable flag in the lsb (0=disabled, 1=enabled).

Access to the extension registers is disabled on reset. The capability to disable access to the extension registers is provided to allow the on-board BIOS to initialize the chip set to a particular mode of operation (especially one of the backwards-compatibility modes), with assurance that extension register contents won't be clobbered inadvertently by older non-610/620-aware user programs.

7.0 VGA/EGA CRT Controller Registers

The CRT Controller provides synchronization signals for the display monitor. The registers are shown in the table below:

Abbrev	Register Name	Standard Port	Extension Port	Mode	Type	Wr Protect
CRX	CRTC Index Register	3?4 I=00 (R/W)		All		
CR0	Horizontal Total	3?5 I=00 (R/W)		EGA	Monitor Tim	WRC[0]
CR1	Horizontal Display End	3?5 I=01 (R/W)		EGA	Display Tim	WRC[1]
CR2	Horizontal Blanking Start	3?5 I=02 (R/W)		EGA	Monitor Tim	WRC[0]
CR3	Horizontal Blanking End	3?5 I=03 (R/W)		EGA	Monitor Tim	WRC[0]
CR4	Horizontal Retrace Start	3?5 I=04 (R/W)		EGA	Monitor Tim	WRC[0]
CR5	Horizontal Retrace End	3?5 I=05 (R/W)		EGA	Monitor Tim	WRC[0]
CR6	Vertical Total	3?5 I=06 (R/W)		EGA	Monitor Tim	WRC[0]
CR7	Overflow	3?5 I=07 (R/W)		EGA	Disp/Mon Tim	WRC[1:0]
CR8	Screen A Preset Row Scan	3?5 I=08 (R/W)		EGA	Display Tim	WRC[1]
CR9	Character Cell Height	3?5 I=09 (R/W)		EGA	Display Tim	WRC[1]
CRA	Cursor Start	3?5 I=0A (R/W)		EGA	Display Tim	WRC[1]
CRB	Cursor End	3?5 I=0B (R/W)		EGA	Display Tim	WRC[1]
CRC	Screen A Start Address High	3?5 I=0C (R/W)		All		WRC[2]
CRD	Screen A Start Address Low	3?5 I=0D (R/W)		All		WRC[2]
CRE	Cursor Location High	3?5 I=0E (R/W)		All		WRC[2]
CRF	Cursor Location Low	3?5 I=0F (R/W)		All		WRC[2]
LPENH	Light Pen High	3?5 I=10 (R)	3C5 I=12 (R/W)	All		n/a
LPENL	Light Pen Low	3?5 I=11 (R)	3C5 I=13 (R/W)	All		n/a
CR10	Vertical Retrace Start	3?5 I=10 (W)	3C5 I=10 (R/W)	EGA	Monitor Tim	WRC[0]
CR11	Vertical Retrace End	3?5 I=11 (W)	3C5 I=11 (R/W)	EGA	Monitor Tim	WRC[0]
CR12	Vertical Display End	3?5 I=12 (R/W)		EGA	Display Tim	WRC[1]
CR13	Offset	3?5 I=13 (R/W)		EGA	Display Tim	WRC[1]
CR14	Underline Location	3?5 I=14 (R/W)		EGA	Display Tim	WRC[1]
CR15	Vertical Blanking Start	3?5 I=15 (R/W)		EGA	Monitor Tim	WRC[0]
CR16	Vertical Blanking End	3?5 I=16 (R/W)		EGA	Monitor Tim	WRC[0]
CR17	CRT Mode Control	3?5 I=17 (R/W)		EGA	Monitor Tim	WRC[0]
CR18	Line Compare	3?5 I=18 (R/W)		EGA	Display Tim	WRC[1]
CR1F	610/620 Identification	3?5 I=1F (R)		VGAI		n/a

Note: '?' in the above port address is 'B' in monochrome mode and 'D' in color mode.

Note: CR0-CRB and CR10-CR18 are referred to collectively as the 'CRTC Timing Registers' and are active in EGA/VGA mode to control CRT timing. In CMGA modes, these registers are disabled and CRT timing is controlled by the '6845 Timing Registers' (R0-RB). CRX, CRC-CRF, LPENH, and LPENL are common to both EGA/VGA and CMGA modes. As shown in the table above, the timing registers are further categorized as 'Monitor Timing' or 'Display Timing'; these two groups of registers can be write protected separately (refer to the description of the Write Control register at extension index 4 for further information).

Note: All CRTC registers except CRC-CRF (R/W) and LPENH/LPENL (R/O) are write-only in the standard IBM EGA. In addition, CRTC registers CR10-CR11 and LPENH/LPENL are at conflicting locations in the standard EGA, so cannot be made R/W at port 3?5 such as was done in the 610/620 VGA chip set for all other CRTC registers. The 610/620 VGA, therefore, allows CR10-CR11 and LPENH/LPENL to be R/W accessed at extension register index locations in addition to their normal access as part of the CRTC register group. This capability is provided for state save and restore. The IBM VGA does not support light pens.

7.1 CRTC Index Register: CRX

I/O Port Address: 3?4

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	CRTC Index Bit-4	R/W		
3	CRTC Index Bit-3	R/W		
2	CRTC Index Bit-2	R/W		
1	CRTC Index Bit-1	R/W		
0 (lsb)	CRTC Index Bit-0	R/W		

The CRTC Index register points to the internal registers of the CRT Controller. The five least significant bits determine which register will be pointed to in the next register read/write operation to I/O port 3B5/3D5.

Since only 5 bits of index register are currently implemented, CRTC registers 0-1F may also be addressed using index ranges 20-3F, 40-5F, 60-7F, 80-9F, A0-BF, C0-DF, and E0-FF. This, however, is not recommended, as higher index ranges are resrved for future use and this may not be true in fuure chip revisions.

The same index register is used for access to both CRTC registers (VGA/EGA mode) and 6845 registers (CMGA modes).

7.2 CRTC Horizontal Total Register: CR0

I/O Port Address: 3?5

Index: 0C

Protecti` ,its: WRC[0]

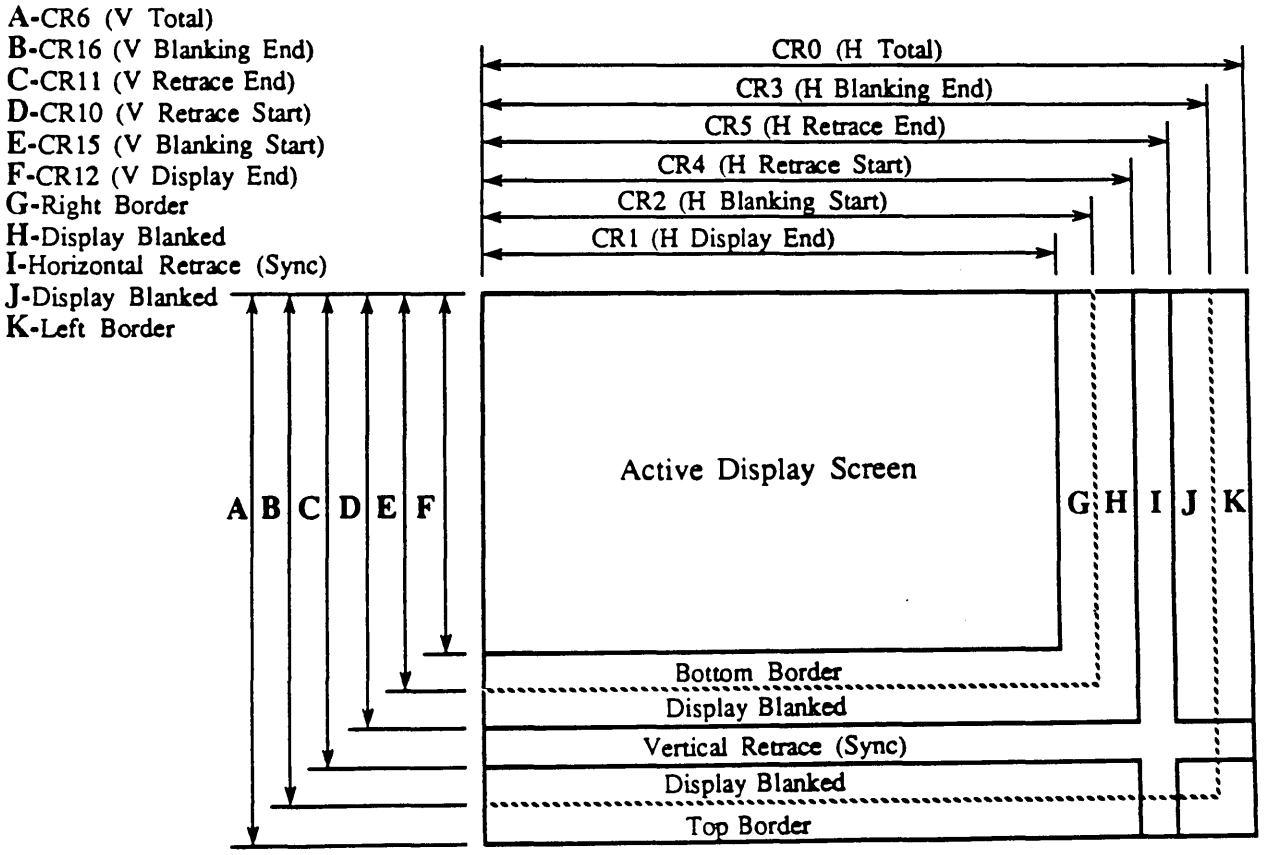
Bit #	Description	Access	Reset By	Reset State
7 (msb)	Horizontal Total Bit-7	R/W		
6	Horizontal Total Bit-6	R/W		
5	Horizontal Total Bit-5	R/W		
4	Horizontal Total Bit-4	R/W		
3	Horizontal Total Bit-3	R/W		
2	Horizontal Total Bit-2	R/W		
1	Horizontal Total Bit-1	R/W		
0 (lsb)	Horizontal Total Bit-0	R/W		

The Horizontal Total register defines the total number of characters in a horizontal scan line, including the retrace time. Together with the value in the Retrace Timing registers CR4 and CR5, the period of the retrace output signal is determined by the value in this register. The character clock input to the device is counted by a character counter. The value of the character counter is compared with the value in this register to provide the horizontal timing. All horizontal and vertical timings are based upon the contents of this register.

The value in the register = Total Number of Characters - 2.

Note: This register is effective only in EGA/VGA mode (see the description of 610/620 VGA extension register ER2F, the 'Active Adapter State' Register).

Figure 7-1: CRTC Timing Registers



7.3 CRTC Horizontal Display End Register: CR1

I/O Port Address: 3?5

Index: 01

Protection Bits: WRC[1]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Horizontal Display End Bit-7	R/W		
6	Horizontal Display End Bit-6	R/W		
5	Horizontal Display End Bit-5	R/W		
4	Horizontal Display End Bit-4	R/W		
3	Horizontal Display End Bit-3	R/W		
2	Horizontal Display End Bit-2	R/W		
1	Horizontal Display End Bit-1	R/W		
0 (lsb)	Horizontal Display End Bit-0	R/W		

The Horizontal Display Enable End register defines the total number of displayed characters in a horizontal line.

The value in the register = Total Number of Characters - 1.

Refer to Figure 6-1 (see register CR0) for a summary of CRTC timing registers.

Note: This register is effective only in EGA/VGA mode (see the description of 610/620 VGA extension register ER2F, the 'Active Adapter State' Register).

7.4 CRTC Horizontal Blanking Start Register: CR2

I/O Port Address: 3?5

Index: 02

Protection Bits: WRC[0]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Horizontal Blanking Start Bit-7	R/W		
6	Horizontal Blanking Start Bit-6	R/W		
5	Horizontal Blanking Start Bit-5	R/W		
4	Horizontal Blanking Start Bit-4	R/W		
3	Horizontal Blanking Start Bit-3	R/W		
2	Horizontal Blanking Start Bit-2	R/W		
1	Horizontal Blanking Start Bit-1	R/W		
0 (lsb)	Horizontal Blanking Start Bit-0	R/W		

The contents of this register define the time when the horizontal blanking will start. The register is defined in terms of the number of horizontal character clocks assuming character positions are numbered 0-n where position 0 is the first displayed character position at the left side of the screen. The horizontal blanking signal becomes active when the horizontal character count is equal to the contents of this register.

The underline scan line decode output is multiplexed on the cursor output during the blanking period. The underline signal is valid for one character count beyond the end of the blanking signal.

Refer to Figure 6-1 (see register CR0) for a summary of CRTC timing registers.

Note: This register is effective only in EGA/VGA mode (see the description of 610/620 VGA extension register ER2F, the 'Active Adapter State' Register).

7.5 CRTC Horizontal Blanking End Register: CR3

I/O Port Address: 3?5
Index: 03
Protection Bits: WRC[0]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	LIGHTPEN compatibility readback	R/W		
6	Display Enable Skew Control	R/W		
5	Display Enable Skew Control	R/W		
4	Horizontal Blanking End Bit-4	R/W		
3	Horizontal Blanking End Bit-3	R/W		
2	Horizontal Blanking End Bit-2	R/W		
1	Horizontal Blanking End Bit-1	R/W		
0 (lsb)	Horizontal Blanking End Bit-0	R/W		

The contents of this register define the time when the horizontal blanking will end. The register is defined in terms of the number of horizontal character clocks assuming character positions are numbered 0-n where position 0 is the first displayed character position at the left side of the screen.

The underline scan line decode output is multiplexed on the cursor output during the blanking period. The underline signal is valid for one character count beyond the end of the blanking signal.

Bit Descriptions

Bit 6-5 Display Enable Skew Control

Prior to displaying data on the screen, the CRT controller has to access the display buffer to obtain a character to be displayed, access the attribute code, access the character generator font, and finally read the Pixel Panning register in the Attribute Controller. Each of these accesses require the display enable signal to be skewed by one character clock to allow for synchronization with the horizontal and vertical retrace pulses. The display enable skew bits in this register allow for this skew. The skew can be programmed from 0-3 character clocks as follows:

D6	D5	Skew in character clocks	
0	0	0	
0	1	1	<= typical setting
1	0	2	
1	1	3	

Bit 4-0 End Horizontal Blanking

The horizontal blanking signal width is determined as follows:

Value in Start Blanking Register (R2) + Width of Blanking Signal W = 5-bit value to be programmed into the End Horizontal Blanking register.

The least five significant bits of the horizontal character counter are compared with the contents of this register. When a match occurs, the horizontal blanking pulse becomes inactive. Note that the five bits of this register limit the length of the blanking pulse to 31 character clocks. Note also that if the blanking interval extends beyond the end of the line, erratic behavior will result since the horizontal character counter gets cleared after the number of character times programmed in the horizontal total register.

Refer to Figure 6-1 (see register CR0) for a summary of CRTC timing registers.

Note: This register is effective only in EGA/VGA mode (see the description of 610/620 VGA extension register ER2F, the 'Active Adapter State' Register).

7.6 CRTC Horizontal Retrace Start Register: CR4

I/O Port Address: 3?5

Index: 04

Protection Bits: WRC[0]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Horizontal Retrace Start Bit-7	R/W		
6	Horizontal Retrace Start Bit-6	R/W		
5	Horizontal Retrace Start Bit-5	R/W		
4	Horizontal Retrace Start Bit-4	R/W		
3	Horizontal Retrace Start Bit-3	R/W		
2	Horizontal Retrace Start Bit-2	R/W		
1	Horizontal Retrace Start Bit-1	R/W		
0 (lsb)	Horizontal Retrace Start Bit-0	R/W		

This register defines the character position at which the Horizontal Retrace Pulse becomes active assuming character positions are numbered 0-n where position 0 is the first displayed character position at the left side of the screen. This register centers the monitor screen horizontally. The value in the register is the character count at which the Horizontal Retrace Pulse becomes active.

Refer to Figure 6-1 (see register CR0) for a summary of CRTC timing registers.

Note: This register is effective only in EGA/VGA mode (see the description of 610/620 VGA extension register ER2F, the 'Active Adapter State' Register).

7.7 CRTC Horizontal Retrace End Register: CR5

I/O Port Address: 3?5

Index: 05

Protection Bits: WRC[0]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Horizontal Retrace End Bit-7	R/W		
6	Horizontal Retrace End Bit-6	R/W		
5	Horizontal Retrace End Bit-5	R/W		
4	Horizontal Retrace End Bit-4	R/W		
3	Horizontal Retrace End Bit-3	R/W		
2	Horizontal Retrace End Bit-2	R/W		
1	Horizontal Retrace End Bit-1	R/W		
0 (lsb)	Horizontal Retrace End Bit-0	R/W		

This register defines the character position at which the Horizontal Retrace Pulse becomes inactive assuming character positions are numbered 0-n where position 0 is the first displayed character position at the left side of the screen.

Bit Descriptions

Bit 7 Start Odd Memory Address: This bit determines the CRT memory address after a horizontal retrace. 0 selects an even address, and 1 selects an odd address. In most cases this bit should be set to 0. This bit is useful in applications where horizontal pixel panning is required.

Bit 6-5 Horizontal Retrace Delay: The skew of the horizontal retrace signal is controlled by these bits. In some modes, it is necessary to provide a horizontal retrace signal that takes up the entire blanking period. The horizontal retrace signal also triggers some internal timings on the falling edge of the signal. To ensure that the signals are latched properly, the retrace signal is started before the end of the display enable signal. It is then skewed several character clock times to provide the proper screen centering.

D6	D5	Skew in character clocks
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4-0 End Horizontal Retrace: The horizontal retrace signal becomes inactive after the character count becomes equal to the count in these bits. The width of the retrace signal is determined as follows:

Value in Retrace Start Register (CR4) + Width of Retrace Signal W = 5-bit value to be programmed into the Horizontal Retrace End register.

The five lsbs of the horizontal character counter are compared to the contents of this register. When a match occurs, the horizontal retrace pulse becomes inactive. Note that the five bits of this register limit the length of the retrace signal to 31 character clocks. Note also that if the retrace interval extends beyond the end of the line, erratic behavior will result since the horizontal character counter gets cleared after the number of character times programmed in the horizontal total register.

Refer to Figure 6-1 (see register CR0) for a summary of CRTC timing registers.

Note: This register is effective only in EGA/VGA mode (see the description of 610/620 VGA extension register ER2F, the 'Active Adapter State' Register).

7.8 CRTC Vertical Total Register: CR6

I/O Port Address: 3?5

Index: 06

Protection Bits: WRC[0]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Vertical Total Bit-7	R/W		
6	Vertical Total Bit-6	R/W		
5	Vertical Total Bit-5	R/W		
4	Vertical Total Bit-4	R/W		
3	Vertical Total Bit-3	R/W		
2	Vertical Total Bit-2	R/W		
1	Vertical Total Bit-1	R/W		
0 (lsb)	Vertical Total Bit-0	R/W		

The Vertical Total register defines the number of horizontal raster scans on the CRT screen, including the vertical retrace. The Vertical Total register contains the low order 8 bits of a 9-bit register. The ninth bit is located in the CRT Controller Overflow register (CR7 bit-0).

Refer to Figure 6-1 (see register CR0) for a summary of CRTC timing registers.

Note: This register is effective only in EGA/VGA mode (see the description of 610/620 VGA extension register ER2F, the 'Active Adapter State' Register).

7.9 CRTC Overflow Register: CR7

I/O Port Address: 3?5

Index: 07

Protection Bits: WRC[1:0]

Bit #	Description	Protected By	Access	Reset By	Reset State
7 (msb)	-unused-				
6	-unused-				
5	-unused-				
4	Bit-8 of Line Compare Reg (CR18)	WRC[1]	R/W		
3	Bit-8 of Vertical Blanking Start Reg (CR15)	WRC[0]	R/W		
2	Bit-8 of Vertical Retrace Reg (CR10)	WRC[0]	R/W		
1	Bit-8 of Vertical Display End Reg (CR12)	WRC[1]	R/W		
0 (lsb)	Bit-8 of Vertical Total Reg (CR6)	WRC[0]	R/W		

The CRT Controller Overflow register is used in conjunction with other control registers and contains the ninth bit (D8) of these registers.

The bits of this register are write protected by ones in bits 0 and 1 of the Extensions Write Control (WRC) Register (extensions index 84).

Note: This register is effective only in EGA/VGA mode (see the description of 610/620 VGA extension register ER2F, the 'Active Adapter State' Register).

7.10 CRTC Screen A Preset Row Scan Register: CR8

I/O Port Address: 3?5

Index: 08

Protection Bits: WRC[1]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	Screen A Preset Row Scan Bit-4	R/W		
3	Screen A Preset Row Scan Bit-3	R/W		
2	Screen A Preset Row Scan Bit-2	R/W		
1	Screen A Preset Row Scan Bit-1	R/W		
0 (lsb)	Screen A Preset Row Scan Bit-0	R/W		

This register specifies the starting row scan count of the character cell after a vertical retrace (assuming the scan lines of a character row are numbered starting with 0). This is the start of the top half of the screen (referred to as 'Screen A') if split screen mode is in effect. Each horizontal retrace increments the horizontal row scan counter. The horizontal row scan counter is cleared at maximum row scan count, which is programmed through register CR9. In text and certain graphics modes, this register can be used for soft scrolling by setting the register value between 0 and the value in CR9. For example, by setting the Preset Row Scan to 1 instead of 0, the next frame will start at scan line 1 of the character cell, which will give the effect of shifting vertically by 1 row, or vertical scrolling. This register should be changed only during vertical retrace.

Refer also to the descriptions of the 'Line Compare' register (CR18) and the 'Screen B' extension registers for more information on how to implement split-screen mode.

Note: This register is effective only in EGA/VGA mode (see the description of 610/620 VGA extension register ER2F, the 'Active Adapter State' Register).

7.11 CRTC Character Cell Height Register: CR9

I/O Port Address: 3?5

Index: 09

Protection Bits: WRC[1]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Scan Double	R/W	Reset or Sync Reset	0
6	-unused-			
5	-unused-			
4	Character Cell Height Bit-4	R/W		
3	Character Cell Height Bit-3	R/W		
2	Character Cell Height Bit-2	R/W		
1	Character Cell Height Bit-1	R/W		
0 (lsb)	Character Cell Height Bit-0	R/W		

This register specifies the number of scan lines per character row minus one.

The msb also enables CRTC scan doubling. When the msb is 0, scan lines are generated for the monitor as in the normal EGA and VGA. When the msb is 1, every scan line in the normal display is displayed twice in succession. The scan doubling bit in this register only effects the CRTC (not the 6845), so only effects the display in EGA/VGA mode. It has no effect in CGA and MGA modes.

Note: This register is effective only in EGA/VGA mode (see the description of 610/620 VGA extension register ER2F, the 'Active Adapter State' Register).

7.12 CRTC Cursor Start Register: CRA

I/O Port Address: 3?5

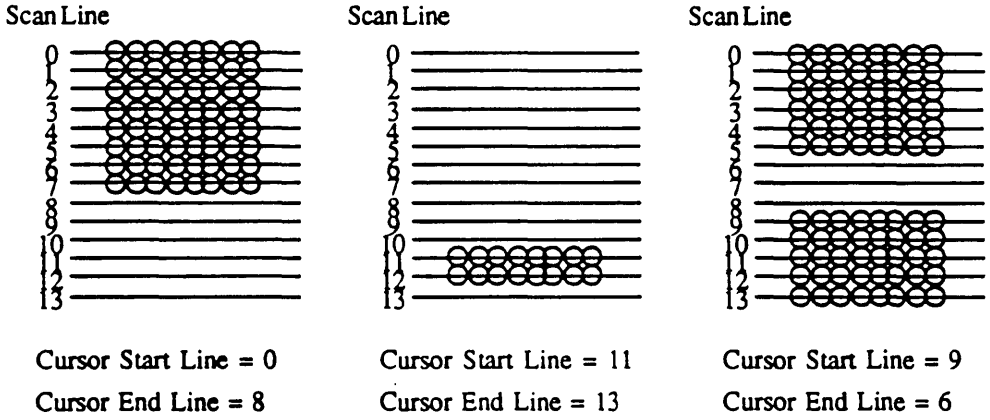
Index: 0A

Protection Bits: WRC[1]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	Cursor Start Bit-4	R/W		
3	Cursor Start Bit-3	R/W		
2	Cursor Start Bit-2	R/W		
1	Cursor Start Bit-1	R/W		
0 (lsb)	Cursor Start Bit-0	R/W		

This register specifies the scan line of the character row where the cursor is to begin assuming the scan lines of a character row are numbered starting with 0. Some examples are shown in the figure below:

Figure 7-2: CRTC Cursor Programming Examples



Note that if the cursor start register value is greater than the cursor end register value, the cursor wraps around, resulting in a two-part cursor. Note also that the end register value must be one greater than that required for 6845 cursor programming.

If the cursor start value is the same as the cursor end value, a 1 line cursor will result. In the IBM EGA, only the 4 lsbs are compared, so that a one-line cursor will result if the start and end registers are identical or different by exactly 16. The 4-bit comparison is not duplicated by the 610/620; the 610/620 produces a one-line cursor only for the expected cases of the start and end registers being different by either 0 or 1.

Note: This register is effective only in EGA/VGA mode (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

7.13 CRTC Cursor End Register: CRB

I/O Port Address: 3?5
Index: 0B
Protection Bits: WRC[1]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused- (IBM EGA/VGA: Cursor Skew Control Bit-1)			
5	-unused- (IBM EGA/VGA: Cursor Skew Control Bit-0)			
4	Cursor End Bit-4	R/W		
3	Cursor End Bit-3	R/W		
2	Cursor End Bit-2	R/W		
1	Cursor End Bit-1	R/W		
0 (lsb)	Cursor End Bit-0	R/W		

The Cursor End register specifies the scan line plus one of the character row where the cursor is to end assuming the scan lines of the character row are numbered starting with 0 (note that this is one greater than that required in the 6845). Refer to the definition of the CRTC cursor start register (CRA) on the previous page for CRTC cursor programming examples.

This register also controls the cursor skew as described below:

Bit Descriptions

Bit 6-5 These two bits are unused in the 610/620 VGA. For reference, in the IBM EGA and VGA, these two bits control the cursor skew as follows:

D6	D5	Skew	Comment
0	0	Zero character skew	
0	1	Zero character skew	
1	0	One character skew	IBM EGA Cursor 2 characters wide in column 1
1	1	Two character skew	IBM EGA Cursor 3 characters wide in column 1

Programming this field with 0 or 1 in the IBM EGA and VGA will result in the cursor being located over the character pointed at by the cursor location registers CRE and CRF. This is the desired result. Programming this field, however, with a non-zero value in the IBM EGA, will result in the cursor being located 1 or 2 characters to the right of that position in most cases, but results in a cursor that is more than one character wide when in column 1. This is usually non-interesting and is not emulated in the 610/620.

Bit 4-0 These bits define the scan line of the character cell where the cursor is to end plus 1. The 'plus 1' part of the definition limits the maximum cursor height to 31 lines instead of the expected 32. An end value greater than the height of the character cell results in a full block cursor the same height as the character cell. An end value less than the start value results in a wrap-around cursor as shown in the figure above.

If the start and end registers have the same value, a 1-line cursor results. However, in the IBM EGA, the comparison is performed with a 4-bit comparator, instead of the expected 5-bit comparator. This, therefore, results in a 1-line cursor also when the cursor start and end registers are different by exactly 16. This behavior of the cursor logic is not emulated by the 610/620; programming the cursor start and end registers to values 16 apart will result in a 16-line cursor.

Note: This register is effective only in EGA/VGA mode (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

7.14 CRTC Screen A Start Address Register High: CRC

I/O Port Address: 3?5

Index: 0C

Protection Bits: WRC[2]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Screen A Start Address Bit-15	R/W		
6	Screen A Start Address Bit-14	R/W		
5	Screen A Start Address Bit-13	R/W		
4	Screen A Start Address Bit-12	R/W		
3	Screen A Start Address Bit-11	R/W		
2	Screen A Start Address Bit-10	R/W		
1	Screen A Start Address Bit-9	R/W		
0 (lsb)	Screen A Start Address Bit-8	R/W		

The Screen A Start Address register is a 16-bit value which specifies first display memory address after a vertical retrace at which the display on the screen begins on each screen refresh. This register contains 8 high order bits of the address, while the Screen A Start Address Low register (CRD) specifies the 8 low-order bits.

The reason that the name of this register is qualified with 'Screen A' is that under some circumstances, two logical screens may be present (split-screen mode). In this case, this register specifies the start address of the first of the two (the top one). The start address of screen B (the bottom one) is specified by a pair of extension registers (ERC and ERD also called SBSH and SBSL). The bottom screen's start scan line on the screen is determined by the line compare register (CR18). Refer to the description of the line compare register for a diagram of split-screen mode.

Note that there is no split screen capability in CMGA modes since there is no line compare register in the 6845.

This register is used for both CMGA and EGA/VGA modes.

Note: This register is also part of the mechanism used to identify the 610/620 chip. Any value written to this register can be read back exclusive-or'd with 'EA' hex (binary '11101010') at CRTC index 1F.

7.15 CRTC Screen A Start Address Register Low: CRD

I/O Port Address: 3?5

Index: 0D

Protection Bits: WRC[2]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Screen A Start Address Bit-7	R/W		
6	Screen A Start Address Bit-6	R/W		
5	Screen A Start Address Bit-5	R/W		
4	Screen A Start Address Bit-4	R/W		
3	Screen A Start Address Bit-3	R/W		
2	Screen A Start Address Bit-2	R/W		
1	Screen A Start Address Bit-1	R/W		
0 (lsb)	Screen A Start Address Bit-0	R/W		

The Screen A Start Address register is a 16-bit value which specifies the first display memory address after a vertical retrace at which the display on the screen begins on each screen refresh. This register contains the 8 low order bits of the address, while the Screen A Start Address High register (CRC) specifies the 8 high-order bits.

This register is used for both EGA/VGA and CMGA modes.

7.16 CRTC Cursor Location Register High: CRE

I/O Port Address: 3?5

Index: 0E

Protection Bits: WRC[2]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Cursor Location Bit-15	R/W		
6	Cursor Location Bit-14	R/W		
5	Cursor Location Bit-13	R/W		
4	Cursor Location Bit-12	R/W		
3	Cursor Location Bit-11	R/W		
2	Cursor Location Bit-10	R/W		
1	Cursor Location Bit-9	R/W		
0 (lsb)	Cursor Location Bit-8	R/W		

The Cursor Location register contains a 16-bit value which specifies the offset of the cursor location from the start of physical display memory in character positions. This register contains the 8 high order bits of the value, while the Cursor Location Low register (CRF) specifies the 8 low-order bits.

When the screen start address registers (CRC and CRD) contain 0, programming the cursor location registers (this register and CRF) to 0 positions the cursor over the upper left character of the screen (row 1, column 1); programming them to 1 positions the cursor over the character in the next column to the right (row 1 column 2), etc. If the screen start registers are changed, the cursor will remain pointed at the same character (i.e., the cursor will effectively move the same number of characters as the displayed screen contents to remain pointed at the same displayed character). The value in the cursor location registers is relative to the start of physical display memory, not to the start of the screen.

Since information is stored in display memory as character/attribute pairs, the address of the character under the cursor will be exactly two times the value in the cursor location registers (plus the base address of the screen).

This register is used for both EGA/VGA and CMGA modes.

7.17 CRTC Cursor Location Register Low: CRF

I/O Port Address: 3?5

Index: 0F

Protection Bits: WRC[2]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Cursor Location Bit-7	R/W		
6	Cursor Location Bit-6	R/W		
5	Cursor Location Bit-5	R/W		
4	Cursor Location Bit-4	R/W		
3	Cursor Location Bit-3	R/W		
2	Cursor Location Bit-2	R/W		
1	Cursor Location Bit-1	R/W		
0 (lsb)	Cursor Location Bit-0	R/W		

The Cursor Location register contains a 16-bit value which specifies the offset of the cursor location from the start of physical display memory in character positions. This register contains the 8 low order bits of the value, while the Cursor Location High register (CRE) specifies the 8 high-order bits.

When the screen start address registers (CRC and CRD) contain 0, programming the cursor location registers (this register and CRE) to 0 positions the cursor over the upper left character of the screen (row 1, column 1); programming them to 1 positions the cursor over the character in the next column to the right (row 1 column 2), etc. If the screen start registers are changed, the cursor will remain pointed at the same character (i.e., the cursor will effectively move the same number of characters as the displayed screen contents to remain pointed at the same displayed character). The value in the cursor location registers is relative to the start of physical display memory, not to the start of the screen.

Since information is stored in display memory as character/attribute pairs, the address of the character under the cursor will be exactly two times the value in the cursor location registers (plus the base address of the screen).

This register is used in both CMGA and EGA/VGA modes.

7.18 CRTC Light Pen Register High: LPENH

I/O Port Address: 3?5 Index 10

Index: I/O Port 3C5 Index 92

Bit #	Description	3?5 Access	3C5 Access	Reset By	Reset State
7 (msb)	Light Pen Address Bit-15	R	R/W		
6	Light Pen Address Bit-14	R	R/W		
5	Light Pen Address Bit-13	R	R/W		
4	Light Pen Address Bit-12	R	R/W		
3	Light Pen Address Bit-11	R	R/W		
2	Light Pen Address Bit-10	R	R/W		
1	Light Pen Address Bit-9	R	R/W		
0 (lsb)	Light Pen Address Bit-8	R	R/W		

The Light Pen High register contains the 8 high-order bits of the memory address at the time the light pen flip flop is set. The low order 8 bits are stored in the Light Pen Low register (LPENL at CRTC index 11). The LPENH and LPENL registers are normally read-only at CRTC index 10 and 11. However, the 610/620 also allows these registers to be accessed R/W at extension index 92 and 93 for state save and restore.

Refer to SLPEN and CLPEN for further information on loading the LPENH and LPENL registers.

This register is used in both CMGA and EGA/VGA modes (the two msbs are always loaded with 0 when the 6845 is active since the 6845 memory address register is only 14 bits wide).

7.19 CRTC Light Pen Register Low: LPENL

I/O Port Address: 3?5 Index 11

Index: I/O Port 3C5 Index 93

Bit #	Description	3?5 Access	3C5 Access	Reset By	Reset State
7 (msb)	Light Pen Address Bit-7	R	R/W		
6	Light Pen Address Bit-6	R	R/W		
5	Light Pen Address Bit-5	R	R/W		
4	Light Pen Address Bit-4	R	R/W		
3	Light Pen Address Bit-3	R	R/W		
2	Light Pen Address Bit-2	R	R/W		
1	Light Pen Address Bit-1	R	R/W		
0 (lsb)	Light Pen Address Bit-0	R	R/W		

The Light Pen Low register contains the 8 low-order bits of the memory address at the time the light pen flip flop is set. The high order 8 bits are stored in the Light Pen High register (LPENH at CRTC index 10). The LPENH and LPENL registers are normally read-only at CRTC index 10 and 11. However, the 610/620 also allows these registers to be accessed R/W at extension index 92 and 93 for state save and restore.

Refer to SLPEN and CLPEN for further information on loading the LPENH and LPENL registers.

This register is used in both CMGA and EGA/VGA modes.

7.20 CRTC Vertical Retrace Start Register: CR10

I/O Port Address: 3?5 Index 10

Index: I/O Port 3C5 Index 90

Protection Bits: WRC[0]

Bit #	Description	3?5 Access	3C5 Access	Reset By	Reset State
7 (msb)	Vertical Retrace Start Bit-7	W	R/W		
6	Vertical Retrace Start Bit-6	W	R/W		
5	Vertical Retrace Start Bit-5	W	R/W		
4	Vertical Retrace Start Bit-4	W	R/W		
3	Vertical Retrace Start Bit-3	W	R/W		
2	Vertical Retrace Start Bit-2	W	R/W		
1	Vertical Retrace Start Bit-1	W	R/W		
0 (lsb)	Vertical Retrace Start Bit-0	W	R/W		

The Vertical Retrace Start register is a 9-bit address which defines the position of the vertical retrace start signal in terms of horizontal scan lines assuming the scan lines are numbered starting from 0 at the top of the screen. The low order 8 bits are programmed through this register, while the high order ninth bit is programmed through the CRTC Overflow register (CR7 bit-2).

This register is normally accessed at CRTC index 10 as a write-only register (read-back at this index returns the Light Pen High Address Register). The 610/620 also allows read/write access at extensions index 90 for state save and restore.

Refer to Figure 7-1 (see register CR0) for a summary of CRTC timing registers.

Note: This register is effective only in EGA/VGA mode (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

7.21 CRTC Vertical Retrace End Register: CR11

I/O Port Address: 3?5 Index 11

Index: I/O Port 3C5 Index 91

Protection Bits: WRC[0]

Bit #	Description	3?5 Access	3C5 Access	Reset By	Reset State
7 (msb)	0=Normal, 1=Test	W	R/W		
6	0=Normal, 1=Test	W	R/W		
5	0=Enable Vertical Interrupt	W	R/W	Reset	1
4	0=Clear Vertical Interrupt	W	R/W	Reset	0
3	Vertical Retrace End Bit-3	W	R/W		
2	Vertical Retrace End Bit-2	W	R/W		
1	Vertical Retrace End Bit-1	W	R/W		
0 (lsb)	Vertical Retrace End Bit-0	W	R/W		

This register is normally accessed at CRTC index 11 as a write-only register (read-back at this index returns the Light Pen Low Address Register). The 610/620 also allows read/write access at extensions index 91 for state save and restore.

Bit Descriptions

Bit 7 Test

For normal operation this bit must be set to "0". This bit is ignored by the 610/620.

Bit 6 Test

For normal operation this bit must be set to "0".Setting this bit to 1 causes line counter bits 7-8 to be forced to 1's ('6845-compatibility' mode). This capability is never used.

Bit 5 A "0" will enable the vertical interrupt of the CRT Controller. (See Input Status Register 0 bit-7 at port address 3C2).

Bit 4 Clear Vertical Interrupt

This bit clears the vertical interrupt generated on the CRTINT output of the CRT controller. A "0" will clear the interrupt.

Bit 3-0 Vertical Retrace End

These 4 bits specify the horizontal scan line count at which the vertical retrace output pulse becomes inactive assuming the scan lines are numbered starting from 0 at the top of the screen. The four bits are compared with the four least significant bits of the vertical scan line counter. When the four counter bits are equal to the contents in this register, the vertical retrace is terminated. The Width W of the vertical retrace pulse can be determined from the following algorithm:

Value of Start Vertical Retrace register (CR10) + W = 4-bit value to be programmed into the Vertical Retrace End register.

Note that the four least significant bits of the algorithm result are to be programmed into this register. Thus the maximum retrace pulse width can only be 15 scan lines. Note also that if the blanking interval extends beyond the end of the screen, erratic behavior will result since the vertical scan line counter gets cleared after the number of scan lines programmed in the vertical total register.

Refer to Figure 7-1 (see register CR0) for a summary of CRTC timing registers.

Note: This register is effective only in EGA/VGA mode (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

7.22 CRTC Vertical Display End Register: CR12

I/O Port Address: 3?5

Index: 12

Protection Bits: WRC[1]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Vertical Display End Bit-7	R/W		
6	Vertical Display End Bit-6	R/W		
5	Vertical Display End Bit-5	R/W		
4	Vertical Display End Bit-4	R/W		
3	Vertical Display End Bit-3	R/W		
2	Vertical Display End Bit-2	R/W		
1	Vertical Display End Bit-1	R/W		
0 (lsb)	Vertical Display End Bit-0	R/W		

The Vertical Display Enable End register defines 8 bits of the 9-bit address which specifies the scan line position where the display on the screen ends assuming the scan lines are numbered starting from 0 at the top of the screen. The ninth bit is located in the CRTC Overflow register (CR7 bit-1).

Refer to Figure 7-1 (see register CR0) for a summary of CRTC timing registers.

Note: This register is effective only in EGA/VGA mode (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

7.23 CRTC Offset Register: CR13

I/O Port Address: 3?5

Index: 13

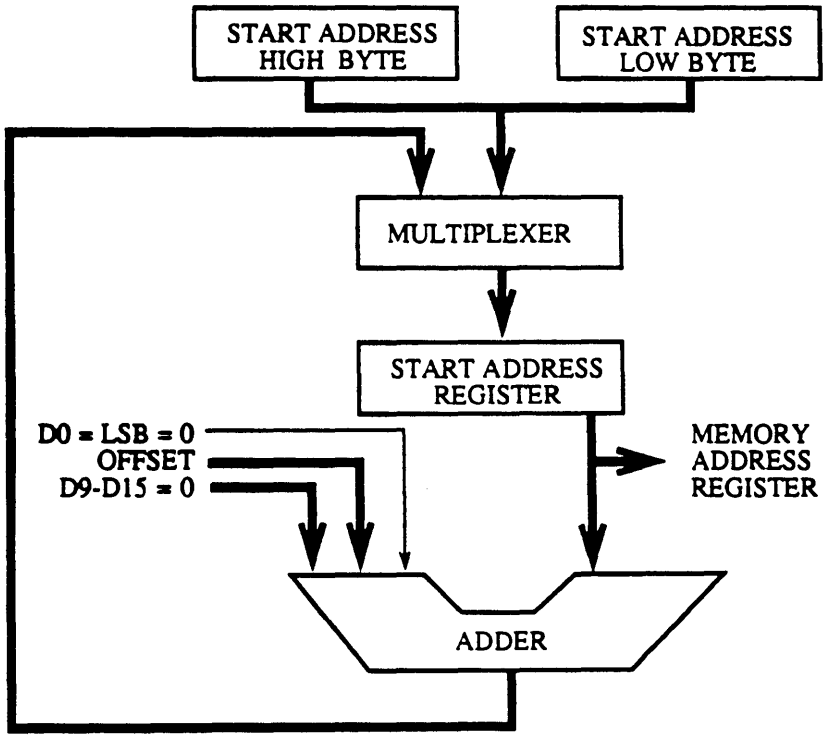
Protection Bits: WRC[1]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Logical Screen Line Width Bit-7	R/W		
6	Logical Screen Line Width Bit-6	R/W		
5	Logical Screen Line Width Bit-5	R/W		
4	Logical Screen Line Width Bit-4	R/W		
3	Logical Screen Line Width Bit-3	R/W		
2	Logical Screen Line Width Bit-2	R/W		
1	Logical Screen Line Width Bit-1	R/W		
0 (lsb)	Logical Screen Line Width Bit-0	R/W		

The Offset register contents define the logical line width of the screen. The starting address of the next character row is determined by the value in the Offset register.

The following figure is a functional diagram of how the Offset register is used. The register start address is sent to the memory address counter. When the memory address counter counts bytes, the next line address is the current line start address + 2 times the Offset register contents. This is shown in the figure by the fact that the adder has one of the input port's least significant bits forced to a "0". When the memory address counter is counting words, the next line address is the current line start address + 4 times the Offset register contents. The byte or word mode for the memory address counter is selected by the Mode Control register (CR17), bit 6. The Start Address High and Low bytes in the figure correspond to the first address after a vertical retrace at which the display on the screen begins.

Figure 7-3: CRTC Offset Register Operation



Note: This register is effective only in EGA mode (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

7.24 CRTC Underline Row Scan Register: CR14

I/O Port Address: 3?5

Index: 14

Protection Bits: WRC[1]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	Double Word Mode	R/W		
5	Count by 4	?		
4	Underline Row Scan Bit-4	R/W		
3	Underline Row Scan Bit-3	R/W		
2	Underline Row Scan Bit-2	R/W		
1	Underline Row Scan Bit-1	R/W		
0 (lsb)	Underline Row Scan Bit-0	R/W		

This register specifies the horizontal row scan of the character cell at which the underline will occur assuming the scan lines of the character cell are numbered from the top starting at 0.

Underlining occurs in text (alphanumeric) mode only when an attribute value of binary 'b000i001' is detected (where b indicates blink and i indicates intensified).

Underlining is normally only enabled while in monochrome modes (EGA mode 7 and Hercules/MGA text modes for example) by setting this register to 13 (the last scan line of the 8x14 character cell). For color modes, this register is normally programmed to a value larger than the size of the character cell to effectively disable underlining. This is due to bits 0-2 and 4-6 of the attribute value being used for foreground and background colors respectively in color modes (activating underlining when the character attributes are set to foreground color 1 and background color 0 is usually not desirable).

In hardware MGA mode in the 610/620, the underline row is fixed at line 13 as there is no equivalent register in the 6845 for specifying the underline row.

Note: This register is effective only in EGA/VGA mode (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

7.25 CRTC Vertical Blanking Start Register: CR15

I/O Port Address: 3?5

Index: 15

Protection Bits: WRC[0]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Vertical Blanking Start Bit-7	R/W		
6	Vertical Blanking Start Bit-6	R/W		
5	Vertical Blanking Start Bit-5	R/W		
4	Vertical Blanking Start Bit-4	R/W		
3	Vertical Blanking Start Bit-3	R/W		
2	Vertical Blanking Start Bit-2	R/W		
1	Vertical Blanking Start Bit-1	R/W		
0 (lsb)	Vertical Blanking Start Bit-0	R/W		

This register contains the low order 8 bits of the horizontal scan line count at which the vertical blanking pulse becomes active assuming the scan lines are numbered starting from 0 at the top of the screen. The ninth bit is located in the CRTC Overflow register (CR7 bit-3).

Refer to Figure 7-1 (see register CR0) for a summary of CRTC timing registers.

Note: This register is effective only in EGA mode (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

7.26 CRTC Cursor Vertical Blanking End Register: CR16

I/O Port Address: 3?5

Index: 16

Protection Bits: WRC[0]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	Vertical Blanking End Bit-4	R/W		
3	Vertical Blanking End Bit-3	R/W		
2	Vertical Blanking End Bit-2	R/W		
1	Vertical Blanking End Bit-1	R/W		
0 (lsb)	Vertical Blanking End Bit-0	R/W		

This register specifies the horizontal scan line count at which the vertical blanking pulse becomes inactive assuming the scan lines are numbered starting from 0 at the top of the screen. The vertical blanking width (W) is determined from the following algorithm:

Value of Start Vertical Blanking register (CR15) + W = 5-bit value to be programmed into the Vertical Blanking End register.

The five least significant bits of the result are programmed into this register. When the five least significant bits of the vertical scan line counter are equal to the value in this register, vertical blanking is terminated. Note that the maximum width of the vertical blanking is limited to 31 scan lines. Note also that if the blanking interval extends beyond the end of the screen, erratic behavior will result since the vertical scan line counter gets cleared after the number of line times programmed in the vertical total register.

Refer to Figure 7-1 (see register CR0) for a summary of CRTC timing registers.

Note: This register is effective only in EGA mode (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

7.27 CRTC Mode Register: CR17

I/O Port Address: 3?5

Index: 17

Protection Bits: WRC[0]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	H/V Retrace Enable	R/W	Reset	0
6	Byte Mode (1), Word Mode (0)	R/W		
5	Address Wrap	R/W		
4	-unused- (IBM EGA: CRTC Output Driver Control)	R/W		
3	Count by Two	R/W		
2	Multiply Vertical by 2 (CR6,10,12,15,18)	R/W		
1	Select Row Scan Counter	R/W		
0 (lsb)	Compatibility Mode Support	R/W		

The Mode Control register is a multi-function register with each bit defining a different option. The following is a description of these bits:

Bit Descriptions

Bit 7 Hardware Reset

State 1 enables vertical and horizontal retrace.

State 0 disables vertical and horizontal retrace.

Bit 6 Byte Mode

State 1 selects byte mode.

State 0 selects word mode. Word mode causes the memory address counter bits to shift down one bit, and the most significant bit of the counter appears on the least significant bit of the memory address output.

Internal Memory Address Counter/Output Multiplexer Relationship

CRTC Out Pin	Byte Address Mode	Word Address Mode
MA0	MA0	MA13 or MA15
MA1	MA1	MA0
MA2	MA2	MA1
.		.
.		.
.		.
MA14	MA14	MA13
MA15	MA15	MA14

Bit 5 Address Wrap

This bit selects the correct memory address counter bit to be output on MA0 in word mode. MA13 is selected if this bit is 0 and MA15 is selected if this bit is 1. When byte mode is selected through D6 of this register, MA0 counter output appears on the MA0 output pin. This bit is set to 0 in the IBM EGA when less than 64K of memory is configured and to 1 if 256K of memory is configured. 610/620 based systems typically come standard with at least 256K of memory configured, so this bit is normally always set to 1.

Bit 4 Unused (this bit must be 0 in the IBM EGA/VGA to enable the CRTC output drivers)

Bit 3 Count by Two

This bit defines whether the contents of the Offset register (CR13) are a word or a double word value. When D3 = "0", the memory address counter is clocked by

the character clock input. When D3 = "1", the memory address is clocked by the character clock input divided by 2. This bit also creates either a byte or word refresh address for the display memory.

Bit 2 Horizontal Retrace Select

This bit controls the vertical resolution capability of the CRT Controller. The vertical counter has a maximum resolution of 512 scan lines as defined by the Vertical Total register. If the vertical retrace counter is clocked with the horizontal retrace clock divided by 2, the vertical resolution is doubled to 1024 horizontal scan lines. D2 = "0" selects the horizontal retrace clock, and D2 = "1" selects the horizontal retrace clock divided by 2.

If this bit is set, the following vertical registers must be programmed to half their normal value to result in the same number of scan lines:

CR6 Vertical Total

CR10 Vertical Retrace Start

CR12 Vertical Display End

CR15 Vertical Blanking Start

CR18 Line Compare

Note that these are the same registers that have overflow bits in the CRTC Overflow register CR7.

Bit 1 Select Row Scan Counter

This bit allows compatibility with the Hercules graphics card and with any other 400 line graphics system. If D1 = "0" the row scan counter bit 1 is substituted for memory address bit 14 during active display time. If D1 = "1" no such substitution takes place.

Bit 0 Compatibility Mode Support

This bit allows compatibility with the IBM Color Graphics Adapter. When D0 = "0" the row scan address bit 0 is substituted for memory address bit 13 during active display time. When D0 = "1" no such substitution takes place.

Note: This register is effective only in EGA mode (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

7.28 CRTC Line Compare Register: CR18

I/O Port Address: 3?5

Index: 18

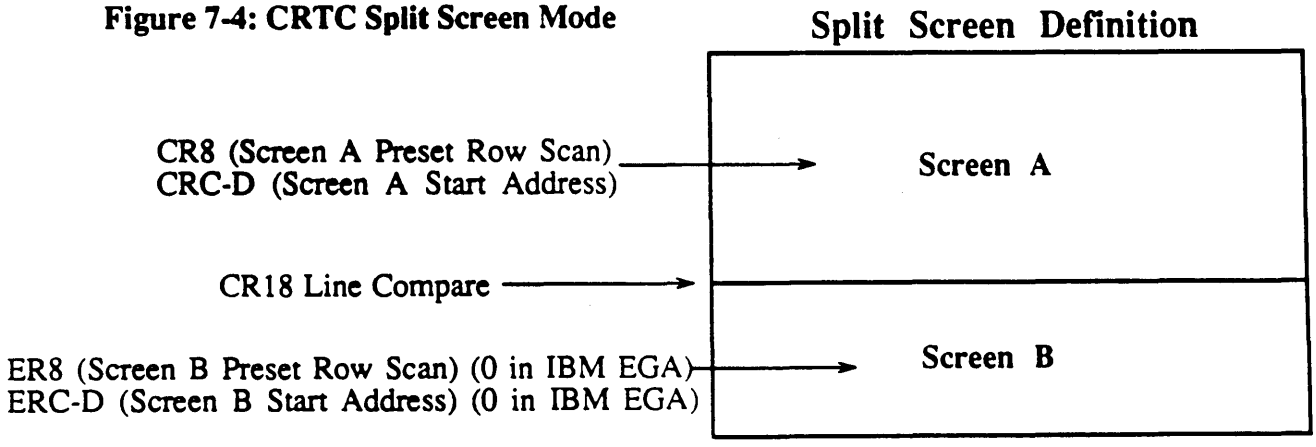
Protection Bits: WRC[1]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	610/620 ID: CRTC Reg C Bit-7 xor 1	R/W		
6	610/620 ID: CRTC Reg C Bit-6 xor 1	R/W		
5	610/620 ID: CRTC Reg C Bit-5 xor 1	R/W		
4	610/620 ID: CRTC Reg C Bit-4 xor 0	R/W		
3	610/620 ID: CRTC Reg C Bit-3 xor 1	R/W		
2	610/620 ID: CRTC Reg C Bit-2 xor 0	R/W		
1	610/620 ID: CRTC Reg C Bit-1 xor 1	R/W		
0 (lsb)	610/620 ID: CRTC Reg C Bit-0	R/W		

The Line Compare register is used to implement the split screen function. It is a 9-bit register where the 8 lsbs are in this register and the msb is in the CRTC Overflow register CR7 bit-4. When the horizontal scan line counter value is equal to the contents of the Line Compare register, the memory address generator is loaded with the contents of the Screen B Start Address Register. In addition, the character row scan count is loaded with the contents of the Screen B Preset Row Scan register. The Screen B registers are not present in the IBM EGA (0 is loaded instead). For compatibility, the Screen B registers are cleared on power-up.

The screen area above where the Line Compare register points is called Screen A and the screen area below that point is called Screen B (see figure below). In standard EGA mode, the Screen B register contents are 0. This allows Screen A to be smooth scrolled, but not Screen B. The 610/620 provides loadable Screen B extension registers which allows Screen B to also be smooth scrolled independently of Screen A. Each scroll window has a starting address for text data in memory and each has a start scan row for the first line of character cells in that window (smooth scrolling requires that the first scan row for the character cells of the first row of the window be nonzero). The Line Compare register determines the point where Screen A ends and Screen B begins. It is typically set to a value of FF (along with a 1 in bit-4 of CRTC Overflow Register CR7) to disable the split-screen feature (no comparison ever occurs so Screen B never starts and the contents of the Screen B extension registers are don't care).

Figure 7-4: CRTC Split Screen Mode



Note: This register is effective only in EGA mode (see the description of 610/620 extension register ER2F, the 'Active Adapter State' Register).

7.29 CRTC 610/620 Identification Register: ID/CR1F

I/O Port Address: 3?5

Index: 1F

Bit #	Description	Access	Reset By	Reset State
7 (msb)	610/620 ID: CRTC Reg C Bit-7 xor 1	R		
6	610/620 ID: CRTC Reg C Bit-6 xor 1	R		
5	610/620 ID: CRTC Reg C Bit-5 xor 1	R		
4	610/620 ID: CRTC Reg C Bit-4 xor 0	R		
3	610/620 ID: CRTC Reg C Bit-3 xor 1	R		
2	610/620 ID: CRTC Reg C Bit-2 xor 0	R		
1	610/620 ID: CRTC Reg C Bit-1 xor 1	R		
0 (lsb)	610/620 ID: CRTC Reg C Bit-0 xor 0	R		

This read-only register may be used to determine whether the graphics adapter is a 510A/520A or 610/620 chip set. The value read back from this register is the current value in CRTC register C (Screen A Start Address High) exclusive-or'd with hex 'EA'. For example, if CRC contains 0, this register will read back hex 'EA'; if CRC contains hex 'FF', this register will read back hex '15'; and so forth. It is unlikely that any graphics adapter other than the **Cirrus Logic** 510A/520A or 610/620 does this in exactly this manner.

Writes to this register are ignored.

(This page intentionally left blank.)

8.0 VGA/EGA Graphics Controller Registers

The Graphics Controller directs data from the display memory to the Attribute Controller and the CPU. The Graphics Controller registers are listed in the following table:

Abbrev	Register Name	Write Port	Read Port	Type
GPOS1	Graphics Controller Position Register 1	3CC	3C5 Index 01	
GPOS2	Graphics Controller Position Register 2	3CA	3C5 Index 02	
GRX	Graphics Controller Index Register	3CE	Same as write	
GRO	Set/Reset Register	3CF Index 00	Same as write	Planar
GR1	Enable Set/Reset Register	3CF Index 01	Same as write	Planar
GR2	Color Compare Register	3CF Index 02	Same as write	Planar
GR3	Data Rotate Register	3CF Index 03	Same as write	
GR4	Read Map Select Register	3CF Index 04	Same as write	
GR5	Mode Register	3CF Index 05	Same as write	
GR6	Miscellaneous Register	3CF Index 06	Same as write	
GR7	Color Don't Care Register	3CF Index 07	Same as write	Planar
GR8	Bit Mask Register	3CF Index 08	Same as write	

Note: These registers are only effective in VGA/EGA mode. In CGA and MGA modes, the data path is fixed in hardware for compatibility with those modes.

Note: The registers labeled above as 'planar' have 1 bit for each of the 4 display memory planes. The definition of these registers is effected by the contents of GPOS1 and GPOS2. The definitions in this document assume that GPOS1 and GPOS2 are programmed to their normal values of 0 and 1 respectively. Refer to the definitions of GPOS1 and GPOS2 for a description of what happens if they aren't.

Note: The Graphics Controller Position registers and Graphics Controller registers 0-8 are write protected by the extensions Write Control (WRC) register (extension register ER4).

8.1 Graphics Controller Position Register 1: GPOS1

I/O Port Address: 3CC (W)
Index: I/O Port 3C5 Index 01 (R)
Protection Bits: WRC[3]

Bit #	Description	3CC Access	3C5 Index 01 Access	Reset By	Reset State
7 (msb)	-unused-				
6	-unused-				
5	-unused-				
4	-unused-				
3	-unused-				
2	-unused-				
1	Graphics Position 1 Bit-1	W	R	Reset	0
0 (lsb)	Graphics Position 1 Bit-0	W	R	Reset	0

Graphics Controller 1 controls planes 0 and 1. This register is programmed to select which bits of the data bus Graphics Controller 1 will respond to for plane-oriented data operations:

GPOS1 Value	Bit-Group Selected for Plane 0/1 Operations
0	0-1 <== Typical value for GPOS1
1	2-3
2	4-5
3	6-7

In other words, if GPOS1 were set to 2, for example, Graphics Controller 1 would respond to bits 4 and 5 for I/O write operations to the 'planar' registers and also for graphics data read/write operations to display memory planes 0 and 1.

This register is normally programmed to 0 to select bits 0 and 1 of the 'planar' Graphics Controller Registers GR0, GR1, GR2, and GR7) for operations involving display memory planes 0 and 1. Graphics Controller registers GR3-GR5 and GR8 are 'non-planar' and are not effected by the contents of the position registers. GPOS1 and GPOS2 should not normally be set to the same value.

Plane assignments are fixed for I/O read operations of the planar registers. Plane-0 control bits always read back on bit-0 and plane-1 control bits always read back on bit-1, independent of the value of this register. No special considerations are required for state save, however, for state restore the following sequence must be followed:

1) Set GPOS1 and GPOS2 to their default values of 0 and 1, respectively
2) Restore registers GR0-8 from saved values
3) Restore registers GPOS1 and GPOS2 from saved values

The Graphics Controller Position registers are not implemented in the IBM VGA (Graphics Controller registers in the IBM VGA are fixed in positions corresponding to values of 0 and 1 programmed into the Graphics Controller Position registers. The 610/620 implements the Position registers for EGA/VGA compatibility.

8.2 Graphics Controller Position Register 2: GPOS2

I/O Port Address: 3CA

Index: I/O Port 3C5 Index 02 (R)

Protection Bits: WRC[3]

Bit #	Description	3CC Access	3C5 Index 01 Access	Reset By	Reset State
7 (msb)	-unused-				
6	-unused-				
5	-unused-				
4	-unused-				
3	-unused-				
2	-unused-				
1	Graphics Position 2 Bit-1	W	R	Reset	0
0 (lsb)	Graphics Position 2 Bit-0	W	R	Reset	1

Graphics Controller 2 controls planes 2 and 3. This register is programmed to select which bits of the data bus Graphics Controller 2 will respond to for plane-oriented data operations:

GPOS2 Value	Bit-Group Selected for Plane 2/3 Operations
0	0-1
1	2-3 <== Typical value for GPOS2
2	4-5
3	6-7

In other words, if GPOS2 were set to 2, for example, Graphics Controller 2 would respond to bits 4 and 5 for I/O write operations to the 'planar' registers and also for graphics data read/write operations to display memory planes 2 and 3.

This register is normally programmed to 1 to select bits 2 and 3 of the 'planar' Graphics Controller Registers GR0, GR1, GR2, and GR7) for operations involving display memory planes 2 and 3. Graphics Controller registers GR3-GR5 and GR8 are 'non-planar' and are not effected by the contents of the position registers. GPOS1 and GPOS2 should not normally be set to the same value.

Plane assignments are fixed for I/O read operations of the planar registers. Plane-2 control bits always read back on bit-2 and plane-3 control bits always read back on bit-3, independent of the value of this register. No special considerations are required for state save, however, for state restore the following sequence must be followed:

1) Set GPOS1 and GPOS2 to their default values of 0 and 1, respectively

2) Restore registers GR0-8 from saved values

3) Restore registers GPOS1 and GPOS2 from saved values

The Graphics Controller Position registers are not implemented in the IBM VGA (Graphics Controller registers in the IBM VGA are fixed in positions corresponding to values of 0 and 1 programmed into the Graphics Controller Position registers. The 610/620 implements the Position registers for EGA/VGA compatibility.

8.3 Graphics Controller Index Register: GRX

I/O Port Address: 3CE

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	-unused-			
3	Graphics Controller Index Bit-3	R/W		
2	Graphics Controller Index Bit-2	R/W		
1	Graphics Controller Index Bit-1	R/W		
0 (lsb)	Graphics Controller Index Bit-0	R/W		

The Graphics Controller Index Register points to other internal registers of the Graphics Controller. The four least significant bits determine the register which will be pointed to in the next Graphics Controller register read/write operation.

8.4 Graphics Controller Set/Reset Register: GR0

I/O Port Address: 3CF
Index: 00
Protection Bits: WRC[3]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	(see GPOS1/GPOS2 register description)	(W)		
6	(see GPOS1/GPOS2 register description)	(W)		
5	(see GPOS1/GPOS2 register description)	(W)		
4	(see GPOS1/GPOS2 register description)	(W)		
3	Set/Reset Plane 3	R/W		
2	Set/Reset Plane 2	R/W		
1	Set/Reset Plane 1	R/W		
0 (lsb)	Set/Reset Plane 0	R/W		

The bits in this register define the value written to the corresponding memory planes when the processor does a memory write with Write Mode 0 selected and the Set/Reset mode enabled with the Enable Set/Reset Register. Note that this can be done on an individual memory plane with separate OUT commands to the Enable Set/Reset Register.

For example, if the Set/Reset register contents are 1101, then a write to display memory will result in the following:

	D7	D6	D5	D4	D3	D2	D1	D0
Plane 3	1	1	1	1	1	1	1	1
Plane 2	1	1	1	1	1	1	1	1
Plane 1	0	0	0	0	0	0	0	0
Plane 0	1	1	1	1	1	1	1	1

This assumes the Enable Set/Reset register (GR1) contents are 1111, all planes are enabled (Sequencer SR2 = 1111) and all bits are unmasked (GR8 = FFh).

Note: The above definition assumes GPOS1 and GPOS2 are set to 0 and 1 respectively. If not, the above definition of which bits correspond to which planes will be different (refer to the GPOS1 or GPOS2 register descriptions for further details). At any one time, 4 of the 8 bits of this register will be writable; which 4 is determined by the values in the position registers. The 4 bits of this register are always readable on bits 0-3.

8.5 Graphics Controller Enable Set/Reset Register: GR1

I/O Port Address: 3CF
Index: 01
Protection Bits: WRC[3]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	(see GPOS1/GPOS2 register description)	(W)		
6	(see GPOS1/GPOS2 register description)	(W)		
5	(see GPOS1/GPOS2 register description)	(W)		
4	(see GPOS1/GPOS2 register description)	(W)		
3	Enable Set/Reset Plane 3	R/W		
2	Enable Set/Reset Plane 2	R/W		
1	Enable Set/Reset Plane 1	R/W		
0 (lsb)	Enable Set/Reset Plane 0	R/W		

The bits in this register enable the Set/Reset function in conjunction with the Set/Reset Register. If the mode register is programmed to write mode 0, the contents of the Set/Reset register are written to the respective display memory planes. If the write mode is 0 and Set/Reset is not enabled on a plane, the plane is written with the data from the CPU data bus.

For example, if the Set/Reset register (R0) contents are 0100, the contents of the Enable Set/Reset register (R1) are 0101 (enable Set/Reset on planes 0 and 2) and a write of 11001101 is done to display memory, it will result in the following:

	D7	D6	D5	D4	D3	D2	D1	D0
Plane 3	1	1	0	0	1	1	0	1
Plane 2	1	1	1	1	1	1	1	1
Plane 1	1	1	0	0	1	1	0	1
Plane 0	0	0	0	0	0	0	0	0

This assumes write mode 0, all planes are enabled (Sequencer SR2 = 1111) and all bits are unmasked (GR8 = FFh).

Note: The above definition assumes GPOS1 and GPOS2 are set to 0 and 1 respectively. If not, the above definition of which bits correspond to which planes will be different (refer to the GPOS1 or GPOS2 register descriptions for further details). At any one time, 4 of the 8 bits of this register will be writable; which 4 is determined by the values in the position registers. The 4 bits of this register are always readable on bits 0-3.

8.6 Graphics Controller Color Compare Register: GR2

I/O Port Address: 3CF
Index: 02
Protection Bits: WRC[3]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	(see GPOS1/GPOS2 register description)	(W)		
6	(see GPOS1/GPOS2 register description)	(W)		
5	(see GPOS1/GPOS2 register description)	(W)		
4	(see GPOS1/GPOS2 register description)	(W		
3	Color Compare Plane 3	R/W		
2	Color Compare Plane 2	R/W		
1	Color Compare Plane 1	R/W		
0 (lsb)	Color Compare Plane 0	R/W		

If the Mode Register has Read mode set, the data read from display memory planes 0 to 3 is compared to the bits D0 to D3 in the Color Compare Register. A match will cause a 1 to be output on the corresponding data bus bit.

For example, if the contents of the Color Compare register are 0011 (to compare planes 0 and 1) and the contents of the plane are as follows:

	D7	D6	D5	D4	D3	D2	D1	D0
Plane 3	0	0	0	0	0	0	0	0
Plane 2	1	1	1	1	1	1	1	0
Plane 1	0	0	0	0	0	0	0	1
Plane 0	1	1	1	1	1	1	1	1

The data bus will contain the following:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1

This assumes the Color Don't Care register (GR7) = 1111.

Note: The above definition assumes GPOS1 and GPOS2 are set to 0 and 1 respectively. If not, the above definition of which bits correspond to which planes will be different (refer to the GPOS1 or GPOS2 register descriptions for further details). At any one time, 4 of the 8 bits of this register will be writable; which 4 is determined by the values in the position registers. The 4 bits of this register are always readable on bits 0-3.

NOTE: An IBM VGA compatible read @ 3?5 index 22 will override ReadMode setting.

8.7 Graphics Controller Data Rotate Register: GR3

I/O Port Address: 3CF
Index: 03
Protection Bits: WRC[3]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	Function Select Bit-1	R/W		
3	Function Select Bit-0	R/W		
2	Rotate Count Bit-2	R/W		
1	Rotate Count Bit-1	R/W		
0 (lsb)	Rotate Count Bit-0	R/W		

This register performs a rotate function on the data written by the CPU. If the Mode Register is programmed for write mode 0, the value in the Rotate Count field represents the number of bits the CPU data will be rotated during CPU write cycles. The shift is a right shift circular.

The Function Select Bits (D3 and D4) allow data in the CPU latches to be logically operated on by the data written into the memory. The bits operate as shown:

D4	D3	Operation
0	0	No change
0	1	Logical 'AND' between Data and latched data
1	0	Logical 'OR' between Data and latched data
1	1	Logical 'XOR' between Data and latched data

Data may be any of the options available with the Write Mode Register. Data cannot be the CPU latched data. For example, if the contents of the Data Rotate register (D2-D0) are 011 and a program is writing CAh to display memory:

PC Data = 1 1 0 0 1 0 1 0 = CAh
the Result Stored is = 0 1 0 1 1 0 0 1 = 59h (the result is shifted 3 bits to the right, circularly)

If the contents of Data Rotate register bits 3 and 4 are binary 11 (the XOR function) and the Graphics CPU latches have been loaded (by a read of display memory) data will appear as follows:

	D7	D6	D5	D4	D3	D2	D1	D0
Plane 3 Latch	1	0	0	1	0	1	1	1
Plane 2 Latch	0	1	1	1	1	0	0	1
Plane 1 Latch	1	1	0	1	0	1	0	1
Plane 0 Latch	1	0	1	1	0	0	0	0

With a write from the PC with data 00111100, an XOR function will be performed on the PC data and the CPU latch, with a result in display memory as follows:

	D7	D6	D5	D4	D3	D2	D1	D0
Plane 3	1	0	1	0	1	0	1	1
Plane 2	0	1	0	0	0	1	0	1
Plane 1	1	1	1	0	1	0	0	1
Plane 0	1	0	0	0	1	1	0	0

This assumes write mode 1, all planes enabled (Sequencer SR2 = 1111) and all bits unmasked (GR8 = FF).

8.8 Graphics Controller Read Map Select Register: GR4

I/O Port Address: 3CF
Index: 04
Protection Bits: WRC[3]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	-unused-			
3	-unused-			
2	Map Select Bit-2	R/W		
1	Map Select Bit-1	R/W		
0 (lsb)	Map Select Bit-0	R/W		

The three least significant bits of this register designate the memory plane from which the CPU reads the data. This register does not effect the read operation performed through the Color Compare register. The four memory planes are selected as follows:

D2	D1	D0	Plane Selected
0	0	0	Plane 0
0	0	1	Plane 1
0	1	0	Plane 2
0	1	1	Plane 3
1	x	x	none

8.9 Graphics Controller Mode Register: GR5

I/O Port Address: 3CF
Index: 05
Protection Bits: WRC[3]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	Shift 256	R/W		
5	Shift Register	R/W		
4	Odd/Even	R/W		
3	Read Mode	R/W		
2	Test Condition	R/W		
1	Write Mode Bit-1	R/W		
0 (lsb)	Write Mode Bit-0	R/W		

Bit Descriptions

Bit 6 Shift 256

This bit is implemented for VGA compatibility and is set to 0 in all EGA-compatible modes. When this bit is 1, the video shift register is set up for 256-color mode. If this bit is set, bit-5 is ignored.

Bit 5 Shift Register

The data bits in the memory planes 0-3 are represented as M0D0-M0D7, M1D0-M1D7, M2D0-M2D7, and M3D0-M3D7 respectively. When this bit is 1, the data in the four serial shift registers will be formatted as follows:

MSB							LSB	Output to:
M1D0	M1D2	M1D4	M1D6	M0D0	M0D2	M0D4	M0D6	ATR0
M1D1	M1D3	M1D5	M1D7	M0D1	M0D3	M0D5	M0D7	ATR1
M3D0	M3D2	M3D4	M3D6	M2D0	M2D2	M2D4	M2D6	ATR2
M3D1	M3D3	M3D5	M3D7	M2D1	M2D3	M2D5	M2D7	ATR3

The least significant bit is shifted out first.

When this bit is 0, M0D7-M0D0, M1D7-M1D0, M2D7-M2D0, and M3D7-M3D0 are shifted out with bit D7 going out first in all cases. The outputs are ATR0-ATR3 respectively for the M0-M3 planes, and are internally connected to the Attribute Controller inputs in the 610 G/A chip.

The first two shift registers correspond to Graphics Controller 1, while the remaining two correspond to Graphics Controller 2.

Bit 4 Odd/Even

Setting this bit to 1 will put the Graphics Controller in the Odd/Even addressing mode. This option is used to emulate the CGA. The function of this bit should track the function of bit-2 of the Sequencer Memory Mode register (note: the binary values will be opposite).

Bit 3 Read Mode

When this bit equals 0 the CPU reads the data from the display memory planes. The plane is selected through the Read Map Select register. When this bit is 1 the CPU reads the result of the logical comparison between the data from the four display memory planes and the contents of the Color Compare register.

Bit 2 Test Condition

This bit is ignored by the 610/620. Setting this bit to 1 in the IBM EGA will tri-state various Graphics Controller outputs for testing the chip.

Bit 1-0 Write Mode

Mode 0:

Each of the four display memory planes is written with the CPU data rotated by the number of counts in the Rotate register. This is always true except when the Set/Reset register is enabled for any of the four planes. In this case the corresponding plane is written with the data stored in the Set/Reset register.

Mode 1:

Each of the four display memory planes is written with the data in the CPU latches. These latches are loaded during a previous CPU read operation. Bit mask values are overridden in this mode. The effect is the same as if the bit mask register is programmed to all zeroes.

Mode 2:

Memory planes 0-3 are filled with the value of data bits 0-3, respectively. For example, memory plane 0 is filled with the value of data bit D0, memory plane 1 is filled with the value of data bus bit D1, etc.

Note that this assumes GPOS1 and GPOS2 are set to 0 and 1 respectively. If not, the mapping between planes and bits will be different.

Mode 3:

This mode is implemented for VGA compatibility and is undefined in the EGA. In this mode, the CPU data is rotated, ANDed with the Bit Mask register, and the result fed into the bit mask in place of the Bit Mask register. In addition, Set/Reset is enabled for all planes in this mode.

8.10 Graphics Controller Miscellaneous Register: GR6

I/O Port Address: 3CF
Index: 06
Protection Bits: WRC[3]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	-unused-			
3	Memory Map Bit-1	R/W		
2	Memory Map Bit-0	R/W		
1	Chain Odd Maps to Even	R/W		
0 (lsb)	Graphics Mode	R/W		

Bit Descriptions

Bit 3-2 Memory Map - These bits control the mapping of the address memory buffers into the CPU address space.

Memory Map 0: A000h for 128K
Memory Map 1: A000h for 64K
Memory Map 2: B000h for 32K
Memory Map 3: B800h for 32K

Bit 1 Chain Odd Maps to Even

When this bit is 1, CPU address bit A0 is replaced by a higher order address bit. The contents of A0 determine which memory plane is selected. A "0" will select planes 0 and 2; a "1" will select planes 1 and 3.

Bit 0 Graphics Mode

When this bit is 1, graphics mode is selected. This will disable the character generator latches.

In the IBM EGA, there are two physical Graphics Controller chips (called 1 and 2). In that hardware, bits 0 and 1 of this register are physically connected to pins of Graphics Controller chip 1 and bits 2 and 3 are physically connected to pins of Graphics Controller chip 2. Therefore, if the Position registers (ports 3CC and 3CA) are not loaded with their normal values, the contents of this register have to be modified to match. For example, if GPOS1 is loaded with 2 and GPOS2 with 3, bits 6-7 of this register are interpreted as Memory Map bits and bits 4-5 of this register are interpreted as Graphics Mode and Chain Odd Maps to Even. In other words, in the IBM EGA, GR6 is 'planar' like the other obvious planar registers GR0-2 and 7.

In the 610/620 chip set, this register is actually located in the S/C (Sequencer/CRTC) chip as part of the address control logic, and is actually not part of the Graphics Controller logic. It is, therefore, non-planar in function. In the IBM VGA, the position registers were not implemented at all, so all IBM VGA registers are non-planar.

In the 610/620 chip set, EGA/VGA graphics mode is determined solely by AR10 [0]

8.11 Graphics Controller Color Don't Care Register: GR7

I/O Port Address: 3CF
Index: 07
Protection Bits: WRC[3]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	(see GPOS1/GPOS2 register description)	(W)		
6	(see GPOS1/GPOS2 register description)	(W)		
5	(see GPOS1/GPOS2 register description)	(W)		
4	(see GPOS1/GPOS2 register description)	(W)		
3	Color Plane 3 = Don't Care	R/W		
2	Color Plane 2 = Don't Care	R/W		
1	Color Plane 1 = Don't Care	R/W		
0 (lsb)	Color Plane 0 = Don't Care	R/W		

Bit Descriptions

Bit 3 0 indicates that color plane 3 is a "don't care" when the Color Compare register test is performed.

Bit 2 0 indicates that color plane 2 is a "don't care" when the Color Compare register test is performed.

Bit 1 0 indicates that color plane 1 is a "don't care" when the Color Compare register test is performed.

Bit 0 0 indicates that color plane 0 is a "don't care" when the Color Compare register test is performed.

For example, if the contents of the Color Compare register (GR2) are 0011 (to compare planes 0 and 1) and the contents of the Color Don't Care register (GR7) are 1011 (ignore plane 2)

	D7	D6	D5	D4	D3	D2	D1	D0
Plane 0	1	1	1	1	1	1	1	1
Plane 1	0	1	0	0	1	1	0	1
Plane 2	1	1	0	1	0	1	1	0
Plane 3	0	0	0	1	1	1	0	0

The data bus will contain the following:

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	1

Note: The above definition assumes GPOS1 and GPOS2 are set to 0 and 1 respectively. If not, the above definition of which bits correspond to which planes will be different (refer to the GPOS1 or GPOS2 register descriptions for further details). At any one time, 4 of the 8 bits of this register will be writable; which 4 is determined by the values in the position registers. The 4 bits of this register are always readable on bits 0-3.

8.12 Graphics Controller Bit Mask Register: GR8

I/O Port Address: 3CF
Index: 08
Protection Bits: WRC[3]

Bit #	Description	Access	Reset By	Reset State
7	Write Enable Data Bit-7	R/W		
6	Write Enable Data Bit-6	R/W		
5	Write Enable Data Bit-5	R/W		
4	Write Enable Data Bit-4	R/W		
3	Write Enable Data Bit-3	R/W		
2	Write Enable Data Bit-2	R/W		
1	Write Enable Data Bit-1	R/W		
0	Write Enable Data Bit-0	R/W		

Any bit programmed to 0 in this register will cause the corresponding bit in each of the four memory planes to be immune to change. The data written into memory in this case will be the data which was read in the previous cycle, and was stored in an internal latch on the Graphics Controller.

Any bit programmed to 1 will allow unrestricted manipulation of the data in the corresponding bit in each of the four memory planes.

The bit mask is applicable to any data written by the CPU, including rotate, logical functions (AND, OR, XOR), Set/Reset and No Change. The data to be preserved using the bit mask must be latched internally by reading the location. The bit mask applies to all the four planes simultaneously.

For example, if the contents of the Bit Mask register are 01101001 and the data latches have been loaded as follows:

	D7	D6	D5	D4	D3	D2	D1	D0
Plane 0 Latch	1	0	1	0	1	0	1	0
Plane 1 Latch	1	1	0	0	1	1	0	1
Plane 2 Latch	0	0	1	0	1	0	1	1
Plane 3 Latch	0	1	0	1	0	0	1	0

With a write from the PC with data 01100110, will result in display memory as follows:

	D7	D6	D5	D4	D3	D2	D1	D0	
Plane 3	0	1	1	1	0	0	1	0	
Plane 2	0	1	1	0	0	0	1	0	
Plane 1	1	1	1	0	0	1	0	0	
Plane 0	1	1	1	0	0	0	1	0	
Effect	L	B	B	L	B	L	L	B	(L=Latched data, B=Bus Data)

This assumes all planes are enabled (Sequencer SR2 = 1111).

9.0 VGA/EGA Attribute Controller Registers

The Attribute Controller registers are summarized in the following table:

Abbrev	Register Name	Port Address	Port Address
ARX	Attribute Controller Index Register	3C0 (R/W)	3C5 index 83 (R/W)
ARO-F	Palette Registers	3CO index 00-0F (W)	3C1 index 00-0F (R)
AR10	Mode Control	3CO index 10 (W)	3C1 index 10 (R)
AR11	Overscan Color	3CO index 11 (W)	3C1 index 11 (R)
AR12	Color Plane Enable	3CO index 12 (W)	3C1 index 12 (R)
AR13	Horizontal Pixel Panning	3CO index 13 (W)	3C1 index 13 (R)
AR14	Color Select	3C0 index 14 (W)	3C1 index 14 (R)

Note: The above registers are effective only in EGA and VGA modes. In CGA and MGA modes the palette is bypassed in hardware.

Note: The Attribute Controller Index register (ARX) is readable at extensions index 83 for state save and restore. An extra bit is available (the data/index pointer) when reads are performed at the extension port. This bit is not available when ARX is read at the 3C0 port. Writes to ARX at the 3C0 port toggle the data/index pointer; writes to ARX at 3C0 and read/write accesses at the extension port do not.

Note: Attribute Controller Registers AR0-AR13 and bit-5 of index register ARX are write protected by bit-3 of the Write Control (WRC) register (see extension register ER4).

9.1 Attribute Controller Index Register: ARX

I/O Port Address: 3C0

Index: I/O Port 3C5 Index 83

Protection Bits: Bit-5 Write Protected by WRC[3]

Bit #	Description	Access at 3C0	Access at 3C5	Reset By	Reset State
7 (msb)	Index (0) / Data (1)	R/O (0)	R/W		
6	-unused-				
5	Palette Address Source	R/W	R/W		
4	Attribute Controller Index Bit-4	R/W	R/W		
3	Attribute Controller Index Bit-3	R/W	R/W		
2	Attribute Controller Index Bit-2	R/W	R/W		
1	Attribute Controller Index Bit-1	R/W	R/W		
0 (lsb)	Attribute Controller Index Bit-0	R/W	R/W		

The Attribute Index Register points to the other internal registers of the Attribute Controller. The five least significant bits (D0-D4) determine which data register is accessed on subsequent data port I/O operations. The index register is accessed at the same I/O port address as the data registers in the standard EGA/VGA; write accesses to 3C0/1 are therefore directed to index and data on alternate accesses. The 3C0 I/O port index/data pointer may be initialized for access of the index register by reading Status Register 1 (I/O port 3BA/3DA).

Attribute Controller operations are further complicated in the standard EGA/VGA by having only write access to both index and data. There is no provision in the standard EGA/VGA for determining the current state of the Attribute Controller registers or the flip flop which determines whether index or data registers are to be accessed next at port 3C0. To minimize these problems, the 610/620 Attribute Controller implements two extensions to the basic functionality of the standard EGA/VGA:

1) The Attribute Controller index may be read at 3C0; the data registers may be read at 3C1.

2) An alternate port (extensions index 83 of port 3C4/3C5) is provided to read or write the flip flop state which determines index or data access at 3C0. For convenience, the remainder of the Attribute Controller Index register bits may also be read or written at the extension port.

Bit Descriptions

Bit 7 This bit indicates whether the Attribute Controller is ready to accept an access to its index register (0) or its data registers (1) for read or write accesses to I/O port 3C0. If the read of this register is performed at 610/620 extensions index 83 (I/O port 3C4/3C5), this bit will return a value of 0 or 1. For compatibility with the standard EGA and VGA, this bit always reads 0 if the read is performed at 3C0. This bit is cleared (to set the Attribute Controller for index accesses at port 3C0) by reading I/O port 3BA or 3DA (EGA/VGA Status Register 1). This bit is toggled by writes to I/O port 3C0 (and not by reads).

Bit 6 This bit is unused.

Bit 5 Video Enable - When this bit is set to 0, the screen displays the color indicated by overscan register AR11 (normally black); when set to 1, normal video display is enabled. In the standard EGA/VGA, this bit also selects the address source for the palette registers (0 = CPU and 1 = Video), which requires that CPU writes to the palette registers only take place when this bit is 0 (or else the data will be written to random palette register locations as determined by the video data

stream at the time of the write). In the 610/620, the palette is dual ported and may be accessed at any time, independent of the state of this bit.

Bit 4-0 These bits form a 5-bit field for storing an index to the data registers in the Attribute Controller.

9.2 Attribute Controller Palette Registers: AR0-F

I/O Port Address: 3C0
Index: 00-0F
Protection Bits: WRC[3]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Reserved for future use	R/W		
6	Reserved for future use	R/W		
5	Secondary Red Video	R/W		
4	Secondary Green Video/Intensity	R/W		
3	Secondary Blue/Mono Video	R/W		
2	Red Video	R/W		
1	Green Video	R/W		
0 (lsb)	Blue Video	R/W		

These sixteen 8-bit registers are pointed to when the contents of the Index register are 00h through 0Fh.

These registers allow a dynamic mapping between the text attribute or graphic color input and the display color on the CRT screen. The six bits, D0 through D5, are output as B, G, R, BS/V, GS/I and RS respectively. A logic 1 in a bit position selects the corresponding color for that bit while a 0 deselects it. The maximum number of possible displayable colors is 64 for monitors with 6 color inputs. Monitors with 3 color inputs allow a maximum of 8 displayable colors, while color monitors which also have an intensity input allow a maximum of 16 displayable colors.

The upper two bits, D6 and D7, are implemented in the palette as read/write bits, but currently do not affect the video output. These bits are reserved for future use.

In the IBM EGA/VGA, the color palette registers should be modified only during retrace intervals to avoid disturbing the displayed image. In the 610/620, the color palette registers may be modified at any time due to the dual ported nature of the palette. (See also the note on the previous page under the 'Palette Address Source' bit of the Attribute Controller Index register regarding this same subject).

9.3 Attribute Controller Mode Control Register: AR10

I/O Port Address: 3C0

Index: 10

Protection Bits: WRC[3]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Video source?			
6	Pixel doubling			
5	Pixel pan compatibility			
4	-unused-			
3	Blink Enable	R/W		
2	Line Graphics Enable	R/W		
1	Monochrome Graphics Attributes Enable	R/W		
0 (lsb)	Graphics Mode	R/W		

Bit Descriptions

Bit7 Video Source 4/5

Bit 6 Pixel Width

This bit is used for VGA compatibility and must be programmed to 0 in all EGA/VGA-compatible modes. If set to 1, the video shift register is clocked at half speed for implementation of 256-color mode. In addition, the internal attribute controller color palette is bypassed (the 8 video bits are passed directly to the external palette). In the 610/620, this bit is not implemented; its function is enabled by GR6 bit-6 (shift-256). Both bits are typically set in 256-color mode, even though this bit is ignored.

Bit 5 Pixel pan compatibility

Bit 4 -unused-

Bit 3 Blink Enable

Setting this bit to 1 enables character blink at a rate determined by the current vertical retrace frequency divided by 32 (16 frames in one state and 16 frames in the other state). This is approximately 1/4 of a second each at 60 Hz and about 1/3 of a second at 50Hz. This is the same rate as the cursor 'slow' blink.

Blinking is implemented by toggling data at the msb of the palette address input. This toggles the palette between registers 0-7 and 8-F. The action of this bit is effected by bit-1 of this register (Monochrome Attributes). Refer to the table on the following page for additional details.

This bit is effective in both text and graphics modes.

Bit 2 Line Graphics Enable

Setting this bit enables the special line graphics character codes by forcing the ninth dot of a line graphics character to be identical to the eighth dot of the character. The line graphics character codes are C0h through DFh.

For 9-bit wide character modes, the left-most 8 bits are determined by data from the font tables; a ninth bit is added on the right of the character cell. Clearing this bit makes the ninth dot the same as the background. For fonts which do not use the line graphics codes from C0h to DFh, this bit should be set to "0". If character widths of 8 dots or less are selected, this bit is a don't care.

This bit is effective in text mode only; it is ignored in graphics mode.

Bit 1 Monochrome Attributes

This bit is programmed to 1 for monochrome '4-color' modes to control the way blinking is handled (see bit-3 of this register). The meaning of the pixel patterns

in graphics '4-color' mode (mode 'F') are black (00), white (01), blinking (10), and intensified white (11). These patterns map to palette entries 0, 1, 4, and 5 if plane 3 is off and 8, 9, C, and D if plane 3 is on (2 bits per pixel get mapped to planes 0 and 2 with planes 1 and 3 = 0). The '10' pattern is caused to blink by placing different contents in the two palette entries corresponding to pixel pattern '10' (entries 4 and C).

This bit works in both graphics mode only.

Bit 0 Graphics Mode

State 1 selects graphics mode.

State 0 selects text mode.

Summary of Operation of AR10 (in graphics mode, planes 0-2 select palette inputs A0-2)

Bit 3	Bit-2	Bit-1	Bit-0	Mode	Description
0	x	x	1	Graphics	Plane 3 selects palette A3
1	x	0	1	Graphics	If plane 3 data =0 then palette input A3=1
					If plane 3 data =1 then palette input A3 is blinked
1	x	1	1	Graphics	Palette input A3 is blinked (toggled on/off at the blink rate)
BL	LG	x	0	Text	If BL=0, characters don't blink (attribute bit-7 controls BG intensity)
					If BL=1, characters link if attribute bit-7 =1 (BG is non-intensified)
					Character blink toggles the character between foreground color (attribute bits 4-6).

9.4 Attribute Controller Overscan Color Register: AR11

I/O Port Address: 3C0

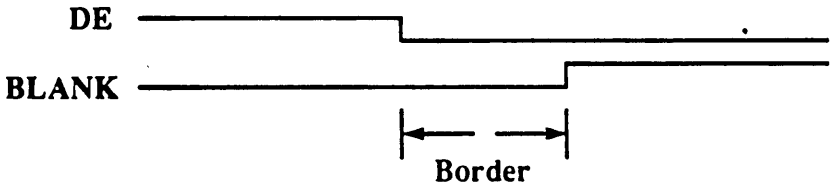
Index: 11

Protection Bits: WRC[3]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Reserved for future use	R/W		
6	Reserved for future use	R/W		
5	Selects Secondary Red Border Color	R/W		
4	Selects Intensified or Secondary Green Border Color	R/W		
3	Selects Secondary Blue Border Color	R/W		
2	Selects Red Border Color	R/W		
1	Selects Green Border Color	R/W		
0 (lsb)	Selects Blue Border Color	R/W		

This register defines the overscan or border color displayed on the CRT screen. "1" bits selects the corresponding color (0 in all bits selects black). The border color is displayed when both BLANK and DE (Display Enable) signals are inactive.

The upper two bits, D6 and D7, are implemented as read/write bits, but currently do not affect the video output. These bits are reserved for future use.



Note: The Enhanced Color Display (ECD) does not support "Border Colors" in 350 line mode. The overscan register should be programmed to 0 in these modes.

9.5 Attribute Controller Color Plane Enable Register: AR12

I/O Port Address: 3C0

Index: 12

Protection Bits: WRC[3]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	Video Status Mux Bit-1	R/W		
4	Video Status Mux Bit-0/Cursor Blink Disable/ Video Output Disable	R/W		
3	Enable Color Plane 3	R/W		
2	Enable Color Plane 2	R/W		
1	Enable Color Plane 1	R/W		
0 (lsb)	Enable Color Plane 0	R/W		

Bit Descriptions

Bit 5-4 Display Status MUX

Bits D4 and D5 select two of the six color outputs to the CRT screen, which are 2 outputs of the 4 status bits. The output color combinations are:

Color Plane Enable Register		Display Status Register (Port 3?A)	
D5	D4	Bit 5	Bit 4
0	0	Video 2 - Red	Video 0 - Blue
0	1	Video 3 - Secondary Blue	Video 1 - Green
1	0	Video 5 - Secondary Red	Video 4 - Secondary Green
1	1	Video 7 - Test	Video 6 - Test

This capability can be used to run diagnostics on the color subsystem card.

Setting bit-4 will also tri-state the video outputs R, G, B, RS, GS/I, and BS/V; and disable the cursor blink counter. Bit-4 must be clear for the cursor blink counter to function.

Bit 3-0 Enable Color Plane

Setting any bit in this group to "1" enables the respective display memory color plane 0-3. A zero in any bit forces the corresponding display memory color plane bit to 0 at the address input of the color palette.

9.6 Attribute Controller Horizontal Pixel Planning Register: AR13

I/O Port Address: 3C0

Index: 13

Protection Bits: WRC[3]

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	-unused-			
3	Horizontal Pixel Panning Shift Count Bit-3	R/W		
2	Horizontal Pixel Panning Shift Count Bit-2	R/W		
1	Horizontal Pixel Panning Shift Count Bit-1	R/W		
0 (lsb)	Horizontal Pixel Panning Shift Count Bit-0	R/W		

Bits D0-D3 of this register select the number of picture elements (pixels) to shift the display data horizontally to the left. Pixel panning is available in both alphanumeric and graphics modes. The start address register specifies the byte of the upper left corner of the screen display, and pixel panning makes it possible to move it in portions of a byte, pixel by pixel.

The amount of shift varies with the character width according to the following table:

Count	9-bit Characters	8-bit Characters	6-bit Characters
0	1 bit left	no shift	2 bits right
1	2 bits left	1 bit left	1 bit right
2	3 bits left	2 bits left	no shift
3	4 bits left	3 bits left	1 bit left
4	5 bits left	4 bits left	2 bits left
5	6 bits left	5 bits left	3 bits left
6	7 bits left	6 bits left	4 bits left
7	8 bits left	7 bits left	5 bits left
8-F	no shift	1 bit right	3 bits right

The Horizontal Pixel Panning register should be changed only during vertical retrace intervals to prevent distorting the display images.

The Offset Register (CR13) should be set to at least one more than normal when characters are not aligned with the character cell, since there is a partial character displayed on the left and the right (for 81 characters total, for example, in 80 column text mode).

(This page intentionally left blank.)

Gopal

10.0 610/620 Extension Registers

610/620 Extension Register Summary

The extension registers provide additional functions to the 610/620 beyond the standard EGA and VGA.

Abbreviations		Register Name	Port	Index	Access
ERX		Extensions Index Register	3C4	--	R/W
ER80	TEST	Extensions Hardware Test	3C5	80	R/W
ER81	GPOS1	* Graphics 1 Position	3C5	81	R/W
ER82	GPOS2	* Graphics 2 Position	3C5	82	R/W
ER83	ARX	* Attribute Controller Index	3C5	83	R/W
ER84	WRC	Write Control	3C5	84	R/W
ER85	TC	Timing Control	3C5	85	R/W
ER86	BWC	Bandwidth Control	3C5	86	R/W
ER87	ROMC	ROM Control	3C5	87	R/W
ER88	SBPR	Screen B Preset Row Scan	3C5	88	R/W
ER89	FONTC	Font Control	3C5	89	R/W
ER8A	LCDCNTLI	LCD Control 1	3C5	8A	R/W
ER8B	SBPR	Screen B Preset Row Scan	3C5	8B	R/W
ER8C	SBSH	Screen B Start Address High	3C5	8C	R/W
ER8D	SBSL	Screen B Start Address Low	3C5	8D	R/W
ER8E	GAREV	G/A Chip Revision Level	3C5	8E	R
ER8F	SCREV	S/C Chip Revision Level	3C5	8F	R
ER90	CR10	* Vertical Retrace Start	3C5	90	R/W
ER91	CR11	* Vertical Retrace End	3C5	91	R/W
ER92	LPENH	* Light Pen High	3C5	92	R/W
ER93	LPENL	* Light Pen Low	3C5	93	R/W
ER94	PPA	Pointer Pattern Address	3C5	94	R/W
ER95	CADJ	Cursor Height Adjust	3C5	95	R/W
ER96	CW	Caret Width	3C5	96	R/W
ER97	CH	Caret Height	3C5	97	R/W
ER98	CXH	Caret Horizontal Position High	3C5	98	R/W
ER99	CXL	Caret Horizontal Position Low	3C5	99	R/W
ER9A	CYH	Caret Vertical Position High	3C5	9A	R/W
ER9B	CYL	Caret Vertical Position Low	3C5	9B	R/W
ER9C	PXH	Pointer Horizontal Position High	3C5	9C	R/W
ER9D	PXL	Pointer Horizontal Position Low	3C5	9D	R/W
ER9E	PYH	Pointer Vertical Position High	3C5	9E	R/W
ER9F	PYL	Pointer Vertical Position Low	3C5	9F	R/W
ERA0	GRL0	GC Memory Latch 0	3C5	A0	R/W
ERA1	GRL1	GC Memory Latch 1	3C5	A1	R/W
ERA2	GRL2	GC Memory Latch 2	3C5	A2	R/W
ERA3	GRL3	GC Memory Latch 3	3C5	A3	R/W
ERA4	CLK	Clock Select	3C5	A4	R/W
ERA5	CURS	Cursor Attributes	3C5	A5	R/W
ERA6		-reserved-	3C5	A6	
ERA7	SWITCH	Mode Switch Control	3C5	A7	R/W
ERA8	NMI1	NMI Mask 1	3C5	A8	R/W
ERA9	NMI2	NMI Mask 2	3C5	A9	R/W
ERAA		-reserved-	3C5	AA	
ERAB	NSTAT1	NMI Status 1	3C5	AB	R
ERAC	NSTAT2	NMI Status 2	3C5	AC	R

ERAD		-reserved-	3C5	AD	
ERAE	CACHE	NMI Data Cache	3C5	AE	R
ERAF	STATE	Active Adapter State	3C5	AF	R/W
ERB0-BF	SCR0-F	Scratch Registers 0-F	3C5	B0-BF	R/W
ERC0	CPURAR	CPU Read Access Range	3C5	C0	R/W
ERC1	CPUWAR	CPU Write Access Range	3C5	C1	R/W
ERC2	LCDCNTLII	LCD Control 2	3C5	C2	R/W
ERC3		-reserved-	3C5	C3	
ERC4	SWRH	Switch Register - High	3C5	C4	R
ERC5	SWRL	Switch Register - Low	3C5	C5	R
ERC6	SBSAM	Screen B Start Addr (msb)	3C5	C6	R/W
ERC7	LCDCNTLIII	LCD Control 3	3C5	C7	R/W
ERC8-CF		-reserved-	3C5	C8-CF	
ERD0	COLOFF	Column Offset Register	3C5	D0	R/W
ERD1	PHDIS	Panel Horizontal Displayed	3C5	D1	R/W
ERD2	ROWOFF	Row Offset Register	3C5	D2	R/W
ERD3	PRST	Panel Row Segment Total	3C5	D3	R/W
ERD4	PNLCTLI	Panel Control 1	3C5	D4	R/W
ERD5	PNLCTLII	Panel Control 2	3C5	D5	R/W
ERD6	GROFF	Gray Scale Offset	3C5	D6	R/W
ERD7-D8		-reserved-	3C5	D7-D8	
ERD9	MOD	Modulation Register	3C5	D9	R/W
ERDA	FRCLR	Frame Color	3C5	DA	R/W
ERDB	PNLCTLIII	Panel Control 3	3C5	DB	R/W
ERDC-DF		-reserved-	3C5	DC-DF	

*Duplicated VGA/EGA registers also read/write accessible as extension registers for state save/restore.

Summary of Bits in 610/620 Not Present in 510/520

		#-Bit	Reset State	Ext Reg Location
Screen A Start Address	S/C	2	0	3?5 I=26 [1:0]
Text Cursor Address	S/C	2	0	3?5 I=27 [1:0]
Plane-3 Font Enable	S/C G/A	1	0	3C5 I=89 [6]
LCDCNTL I:				
Power Save Enable	S/C G/A	1	0	3C5 I=8A [7]
Force 8-dot text	S/C	1	0	3C5 I=8A [6]
Divide Ext Clk by 2	S/C	1	0	3C5 I=8A [4]
Use Ext Clk Mux	S/C	1	0	3C5 I=8A [3]
ROM Page Bits	S/C	3	0,1,1	3C5 I=8A [2:0]
CPU Read Addr. range	S/C	8	0	3C5 I=C0
CPU Write Addr. range	S/C	8	0	3C5 I=C1
LCDCNTL II:				
256K Bytes Vmem addr	S/C	1	0	3C5 I=C2 [7]
CPU Addr Shift Left	S/C	2	0	3C5 I=C2 [6,5]
400/480 line cntl	S/C	1	0	3C5 I=C2 [4]
Display type select	S/C G/A	2	0,0	3C5 I=C2 [3:2]
Enable Expanded Graphic	S/C	1	0	3C5 I=C2 [1]
Protect CRTC Vert. Dis.	S/C	1	0	3C5 I=C2 [0]
Switch Register (hi)	S/C	8	0	3C5 I=C4 [7:0]
Switch Register (low)	S/C	8	0	3C5 I=C5 [7:0]
Screen B Start Address (msb)	S/C	2	0	3C5 I=C6 [1:0]
LCDCNTL III:				
Div Mclk by 2	S/C	1	x	3C5 I=C7 [4]
Force 16 bit	S/C	1	x	3C5 I=C7 [3]
Shadow Vertical Total	S/C	1	0	3C5 I=C7 [2]
All A&B Addr 16-bits	S/C	1	0	3C5 I=C7 [1]
Enable 16 bit Interface	S/C G/A	1	0	3C5 I=C7 [0]
Column Offset	G/A	9		3C5 I=D0 [7:0] & I=D4 [4]
Panel Horz. Displayed	G/A	9		3C5 I=D1 [7:0] & I=D4 [5]
Row Offset	G/A	9		3C5 I=D2 [7:0] & I=D4 [6]
Panel Row Seg Total	G/A	9		3C5 I=D3 [7:0] & I=D4 [7]
PNLCNTLI:				
Panel Row Seg Total (8)	G/A	1	x	3C5 I=D4 [7]
Row Offset (8)	G/A	1	x	3C5 I=D4 [6]
Panel Horz. Displayed (8)	G/A	1	x	3C5 I=D4 [5]
Column Offset (8)	G/A	1	x	3C5 I=D4 [4]
Auto Center Enable	G/A	1	x	3C5 I=D4 [3]
Extra-llclk-en	G/A	1	x	3C5 I=D4 [2]
Fr-A8-en	G/A	1	x	3C5 I=D4 [1]
rtrc-llclk-en	G/A	1	x	3C5 I=D4 [0]

		#-Bit	Reset State	Ext Reg Location
PNLCNTLII:				
LCD Palette enable	G/A	1	0	3C5 I=D5 [7]
Reverse Video bit	G/A	1	0	3C5 I=D5 [6]
Attribute Emulation	G/A	1	0	3C5 I=D5 [5]
Force 16 bit	G/A	1	0	3C5 I=D5 [4]
-unused-	G/A	1	0	3C5 I=D5 [3]
Color Palette protect	G/A	1	0	3C5 I=D5 [2]
MGA Reduction	G/A	2	0	3C5 I=D5 [1,0]
Gray-Scale Offset	G/A	4	1101	3C5 I=D6 [3:0]
Vert-Stipple-en	G/A	1	0	3C5 I=D6 [7]
Modulation	G/A	8-bit	0	3C5 I=D9 [7:0]
Frame Color	G/A	4-Bit	x	3C5 I=DA [3:0]
PNLCNTLIII:				
CGA color emulation	G/A	1	0	3C5 I=DB [7]
MCLK invert	G/A	1	0	3C5 I=DB [6]
Video Tristate	G/A	1	0	3C5 I=DB [5]
				3C5 I=DC [0] (reserved)
				3C5 I=DE [7:0] (reserved)
				3C5 I=DF [3:0] (reserved)

Note: Reserved registers do not exist in Stingray. Bits common to S/C & G/A are read-back by S/c.

10.1 Extensions Hardware Test Register: TEST

I/O Port Address: 3C5
Index: 80

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Tristate Video Controls			
6	-unused-	R/W	-	-
5	-reserved-			
4	All-to-CPU Enable	R/W	Reset	0
3	RAMDAC State	R/W	Reset	0
2	All-to-CPU Horizontal Disable	R/W	Reset	0
1	CLKIN Filter Disable	R/W	Reset	0
0 (lsb)	S/C Chip Test	R/W	Reset	0

Bit Descriptions

Bit 7 This bit tristates the S/C controls to support 34010 interface.

Bit 6 reserved

Bit 5 reserved

Bit 4 All-to-CPU Enable

When this bit is clear, 'all-to-CPU' capability is disabled and the currently selected bandwidth determines CPU access at all times, not just when video is enabled. When this bit is 1, the CPU gets all memory access cycles when video is disabled (blanked).

Bit3 RAMDAC State

This bit is used to indicate which RAMDAC port was written to last (0 indicates 3C7 and 1 indicates 3C8). This is used for state save and restore. This bit essentially emulates the function of the 3C7 readback of the VGA.

Bit 2 All-to-CPU Horizontal Disable

This is the same as bit-3 of Rev D, but inverted so that the default is enabled rather than disabled.

Bit 1 CLKIN Filter Disable

This bit disables the filter on the CLKIN input that eliminates clock spikes potentially generated when the clock multiplexer is switched from one clock oscillator to another. This should not be necessary, but is provided just in case.

Bit 0 S/C Chip Test

When this bit is set, registers in the S/C chip (which normally read back from the G/A chip) read back from the S/C chip. Software should never set this bit when both chips are installed in a board. This bit is for standalone chip test only.

10.2 Graphics Controller Position Register 1: GPOS1

I/O Port Address: 3C5

Index: 81

Bit #	Description	3CC Access	3C5 Index 01 Access	Reset By	Reset State
7 (msb)	-unused-				
6	-unused-				
5	-unused-				
4	-unused-				
3	-unused-				
2	-unused-				
1	Graphics Position 1 Bit-1	W	R	Reset	0
0 (lsb)	Graphics Position 1 Bit-0	W	R	Reset	0

Graphics Controller 1 controls planes 0 and 1. This register is programmed to select which bits of the data bus Graphics Controller 1 will respond to for plane-oriented data operations:

GPOS1 Value	Bit-Group Selected for Plane 0/1 Operations
0	0-1 <== Typical value for GPOS1
1	2-3
2	4-5
3	6-7

In other words, if GPOS1 were set to 2, for example, Graphics Controller 1 would respond to bits 4 and 5 for I/O write operations to the 'planar' registers and also for graphics data read/write operations to display memory planes 0 and 1.

This register is normally programmed to 0 to select bits 0 and 1 of the 'planar' Graphics Controller Registers GR0, GR1, GR2, and GR7) for operations involving display memory planes 0 and 1. Graphics Controller registers GR3-GR5 and GR8 are 'non-planar' and are not effected by the contents of the position registers. The 'non-planar' registers are duplicated in each Graphics Controller chip in the IBM EGA; the Veg VGA has all Graphics Controller sections implemented in one chip so only implements one set of non-planar registers which control all sections.

GPOS1 and GPOS2 should not normally be set to the same value.

Plane assignments are fixed for I/O read operations of the planar registers. Plane-0 control bits always read back on bit-0 and plane-1 control bits always read back on bit-1, independent of the value of this register. No special considerations are required for state save, however, for state restore the following sequence must be followed:

1) Set GPOS1 and GPOS2 to their default values of 0 and 1, respectively

2) Restore registers GR0-8 from saved values

3) Restore registers GPOS1 and GPOS2 from saved values

The Graphics Controller Position registers are not implemented in the IBM VGA (Graphics Controller registers in the IBM VGA are fixed in positions corresponding to values of 0 and 1 programmed into the Graphics Controller Position registers. The Eagle VGA implements the Position registers for EGA compatibility.

10.3 Graphics Controller Position Register 2: GPOS2

I/O Port Address: 3C5

Index: 82

Bit #	Description	3CC Access	3C5 Index 01 Access	Reset By	Reset State
7 (msb)	-unused-				
6	-unused-				
5	-unused-				
4	-unused-				
3	-unused-				
2	-unused-				
1	Graphics Position 2 Bit-1	W	R	Reset	0
0 (lsb)	Graphics Position 2 Bit-0	W	R	Reset	1

Graphics Controller 2 controls planes 2 and 3. This register is programmed to select which bits of the data bus Graphics Controller 2 will respond to for plane-oriented data operations:

GPOS2 Value	Bit-Group Selected for Plane 2/3 Operations
0	0-1
1	2-3 <== Typical value for GPOS2
2	4-5
3	6-7

In other words, if GPOS2 were set to 2, for example, Graphics Controller 2 would respond to bits 4 and 5 for I/O write operations to the 'planar' registers and also for graphics data read/write operations to display memory planes 2 and 3.

This register is normally programmed to 1 to select bits 2 and 3 of the 'planar' Graphics Controller Registers GR0, GR1, GR2, and GR7) for operations involving display memory planes 2 and 3. Graphics Controller registers GR3-GR5 and GR8 are 'non-planar' and are not effected by the contents of the position registers. The 'non-planar' registers are duplicated in each Graphics Controller chip in the IBM EGA; the Eagle VGA has all Graphics Controller sections implemented in one chip so only implements one set of non-planar registers which control all sections.

GPOS1 and GPOS2 should not normally be set to the same value.

Plane assignments are fixed for I/O read operations of the planar registers. Plane-2 control bits always read back on bit-2 and plane-3 control bits always read back on bit-3, independent of the value of this register. No special considerations are required for state save, however, for state restore the following sequence must be followed:

1) Set GPOS1 and GPOS2 to their default values of 0 and 1, respectively

2) Restore registers GR0-8 from saved values

3) Restore registers GPOS1 and GPOS2 from saved values

The Graphics Controller Position registers are not implemented in the IBM VGA (Graphics Controller registers in the IBM VGA are fixed in positions corresponding to values of 0 and 1 programmed into the Graphics Controller Position registers. The Eagle VGA implements the Position registers for EGA compatibility.

10.4 Attribute Controller Index: ARX

I/O Port Address: 3C5

Index: 83

Bit #	Description	Access at 3C0	Access at 3C5	Reset By	Reset State
7 (msb)	Index (0) / Data (1)	R/O (0)	R/W		
6	-unused-				
5	Palette Address Source	R/W	R/W		
4	Attribute Controller Index Bit-4	R/W	R/W		
3	Attribute Controller Index Bit-3	R/W	R/W		
2	Attribute Controller Index Bit-2	R/W	R/W		
1	Attribute Controller Index Bit-1	R/W	R/W		
0 (lsb)	Attribute Controller Index Bit-0	R/W	R/W		

The Attribute Index Register points to the other internal registers of the Attribute Controller. The five least significant bits (D0-D4) determine which data register is accessed on subsequent data port I/O operations. The index register is accessed at the same I/O port address as the data registers in the standard EGA/VGA; accesses to 3C0 are therefore directed to index and data on alternate accesses. The 3C0 I/O port index/data pointer may be initialized for access of the index register by reading Status Register 1 (I/O port 3BA/3DA).

Attribute Controller operations are further complicated in the standard EGA by having only write access to both index and data. There is no provision in the standard EGA for determining the current state of the Attribute Controller registers or the flip flop which determines whether index or data registers are to be accessed next at port 3C0. To minimize these problems, the Eagle VGA Attribute Controller implements two extensions to the basic functionality of the standard EGA:

1) The Attribute Controller index may be read at 3C0; the data registers may be read at 3C1.
2) An alternate port (extensions index 83 of port 3C4/3C5) is provided to read or write the flip flop state which determines index or data access at 3C0. For convenience, the remainder of the Attribute Controller Index register bits may also be read or written at the extension port.

Bit Descriptions

Bit 7 This bit indicates whether the Attribute Controller is ready to accept an access to its index register (0) or its data registers (1) for read or write accesses to I/O port 3C0. If the read of this register is performed at Eagle VGA extensions index 83 (I/O port 3C4/3C5), this bit will return a value of 0 or 1. For compatibility with the standard EGA and VGA, this bit always reads 0 if the read is performed at 3C0. This bit is cleared (to set the Attribute Controller for index accesses at port 3C0) by reading I/O port 3BA or 3DA (EGA/VGA Status Register 1). This bit is toggled by writes to I/O port 3C0 (and not by reads).

Bit 6 This bit is unused.

Bit 5 Video Enable - When this bit is set to 0, the screen displays the color indicated by overscan register AR11 (normally black); when set to 1, normal video display is enabled. In the standard EGA/VGA, this bit also selects the address source for the palette registers (0 = CPU and 1 = Video), which requires that CPU writes to the palette registers only take place when this bit is 0 (or else the data will be written to random palette register locations as determined by the video data stream at the time of the write). In the Eagle VGA, the palette is dual ported and

may be accessed at any time, independent of the state of this bit.

Bit 4-0 These bits form a 5-bit field for storing an index to the data registers in the Attribute Controller.

10.5 Extensions Write Control Register: WRC

I/O Port Address: 3C5
Index: 84

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Disable Write of Non-6845 CMGA Registers	R/W	Reset	0
6	Disable Write of Non-CRTC/6845 Regs common to VGA/CMGA	R/W	Reset	0
5	Disable Write of 6845 Display Timing Registers	R/W	Reset	0
4	Disable Write of 6845 Monitor Timing Registers	R/W	Reset	0
3	Disable Write of Non-CRTC EGA/VGA Registers	R/W	Reset	0
2	Disable Write of common CRTC/6845 Registers (CRC-CRF)	R/W	Reset	0
1	Disable Write of CRTC Display Timing Resgisters	R/W	Reset	0
0 (lsb)	Disable Write of CRTC Monitor Timing and MISC Registers	R/W	Reset	0

The most significant nibble of this register is for CMGA register write control. The least significant nibble is for EGA/VGA register write control.

Bit Descriptions

Bit 7 State 1 = Disable write of CGA and MGA registers other than the 6845 registers:
Mode, Config, Color

Bit 6 State 1 = Disable write of non-6845/CRTC registers common to the EGA/VGA & CMGA:
CLPEN, SLPEN
Disable write to FC[1,0] register bits

Bit 5 State 1 = Disable write of 6845 Display Timing registers:
R1 - Horizontal Displayed
R6 - Vertical Displayed
R9 - Character Cell Height
RA - Cursor Start
RB - Cursor End

Bit 4 State 1 = Disable write of 6845 Monitor Timing registers:
R0 - Horizontal Total
R2 - Horizontal Sync Position
R3 - Horizontal/Vertical Sync Width
R4 - Vertical Total
R5 - Vertical Total Adjust
R7 - Vertical Sync PositionR8 - Interlace Mode

Bit 3 State 1 = Disable write of non-CRTC EGA/VGA registers:
Graphics Controller Registers: GPOS1-2, GR0-8
Sequencer Registers: SR0-4
Attribute Controller Registers: AR0-13, ARX bit-5
External Registers: Feature Control, Misc bits 0-1 and 4-5

Bit 2 State 1 = Disable write of registers common to the CRTC and 6845:
CRC-CRF

Bit 1 State 1 = Disable write of CRTC Display Timing registers:
CR1 - Horizontal Display End
CR7 - Overflow (bits 1 and 4)

CR13 - Offset
CR8 - Screen A Preset Row Scan
CR14 - Underline Location
CR9 - Character Cell Height
CR12 - Vertical Display End
CR18 - Line Compare
CRA - Cursor Start
CRB - Cursor End

Bit 0 State 1 = Disable write of CRTC Monitor Timing registers and MISC output register clock bits:

CR0 - Horizontal Total
CR2 - Horizontal Blank Start
CR3 - Horizontal Blank End
CR4 - Horizontal Retrace Start
CR5 - Horizontal Retrace End
CR6 - Vertical Total
CR7 - Overflow (bits 0, 2, and 3)
CR10 - Vertical Retrace Start
CR11 - Vertical Retrace End
CR15 - Vertical Blank Start
CR16 - Vertical Blank End
CR17 - Mode
MISC - Misc Register (bits 2-3 and 6-7)

'Display Timing' registers are defined as those in which the value determines how the image is displayed and viewed by the user of the system. Display timing register values must be known by the current applications program to determine how to store data to make the displayed image appear correctly. These registers may need to be changed during execution of a user program (especially to switch between text and graphics modes). These registers determine the displayed horizontal resolution (in character times) and displayed vertical resolution (in 'logical' scan lines). They also determine the size and shape of the cursor and underline placement.

'Monitor Timing' registers are defined as those in which the value determines the timing of the horizontal and vertical retrace and blanking signals (pulse width, placement, and frequency). These registers must be set to match the current monitor and determine, among other things, the number of raster scan lines on the monitor.

The timing registers are write protected in separate display and monitor timing groups so that the monitor timing register group may be set with values for a fixed frequency monitor such as a 400-line monitor, then write protected. The scan-line doubling control may then be enabled to allow the 610/620 to automatically switch into scan-line doubled 6845 mode to run CGA programs on 400-line monitors.

Note that the extensions active state register (ER2F) also controls write enable of the CRTC and 6845 timing registers. Write of CRTC/6845 registers may be disabled by 1-bits in the Write Control (WRC) register (to override write-enable by ER2F); zeros in the WRC register only allow CRTC/6845 writes to occur if writes would otherwise be enabled.

10.6 Extensions Timing Control Register: TC

I/O Port Address: 3C5
Index: 85

Bit #	Description	Access	Reset By	Reset State
7 (msb)	CMGA VRTC Polarity Reversal	R/W		
6	CMGA HRTC Polarity Reversal	R/W		
5	Allow Video Disable in CGA Text MODE	R/W		
4	6845 Scan Double	R/W		
3	Analog Monitor	R/W		
2	Reserved (should be set to 0)	R/W		
1	Character Width Bit-1	R/W	Reset or Sync Reset or SR1 write	0
0 (lsb)	Character Width Bit-0	R/W		

Bit Descriptions

Bit 7 State 1 = Reverse normal Vertical Retrace polarity in CMGA mode.

Bit 6 State 1 = Reverse normal Horizontal Retrace polarity in CMGA mode.

When bits 6 and 7 of this register are 0, retrace polarities are as follows:

	CGA	MGA	EGA 350-line Mode (for reference only)
Vertical:	high	low	low (MISC bit-7 = 0)
Horizontal:	high	high	high (MISC bit-6 = 1)

Bit 5 Allow Video Disable in CGA Text Mode

If this bit is set, CMGA Mode register (port 3?8) bit-3 (Video Enable) works as described in that register description. If this bit is clear, Mode register bit-3 is ignored in CGA Text mode (video is forced on in this mode).

In the IBM CGA, display memory accesses can only be performed during vertical retrace; otherwise 'snow' will be displayed on the screen. In addition, scrolling the screen in text mode requires movement of a large amount of characters and would take too long if restricted to vertical retrace. Therefore, system BIOS turns display memory off temporarily during scrolling. This, however, produces an annoying 'flashing' effect during scrolling. This bit is provided to eliminate the flashing, but still allow the hardware to be put into a totally CGA-compatible mode if desired.

Bit 4 6845 Scan Line Doubling

If this bit is set, every, scan line is displayed twice in succession. All vertical reister values (R3 bits 4-7 and R4-R7) are interpreted as twice the programmed value. This results in twice the normal number of scan lines being produced if the vertical registers are programmed to their standard values, but the same amount of actual information is displayed. This allows older 200-line CGA modes to be displayed on newer 400-line monitors with bettter readability while maintaining software compatibility. Typically, a double-frequency clock is also programmed when this mode is selected, in order to maintain the same vertical frequency (see bit-3).

Bit 3 This bit is unused in chip rev DAnalog Monitor - If this bit is clear, the memory interleave for CGA and MGA modes is forced to 1:1 or 2:1, which are adequate forclock frequencies up to 16 MHz (the typical clock value programmed for these modes). If this bit is set, the interleave is forced to 1:4 or 3:2, to allow higher clock frequencies to be programmed. This bit is typically set along with bit-4 above (scan doubling) and a clock setting of 28 MHz.

In chip rev A, setting this bit also forces the vertical sync width to 1 (6845 R3 bits 4-7) and forces the horizontal sync position to one less than the value programmed into 6845 R2. In addition, the memory interleave in chip revision A is no longer forced; it is programmable via new bits in the BWC register (extensions index 86).

Bit 2-0 These bits select the character cell width per the following table:

Bit-2	Bit-1	Bit-0	Character Cell Width
0	0	0	9 dots - set by hardware for MGA text mode
0	0	1	8 dots - set by hardware for CGA & MGA graphics mode
0	1	0	6 dots - limited to 16 MHz max
0	1	1	Reserved for future use
1	x	x	Reserved for future use

For 9-dot mode, use the following bandwidth settings:

3:2 for 7 MHz and monochrome 1-bit/pixel graphics mode

1:1 for 16 MHz

1:4 for > 16 MHz

Note that bit-0 is the same as Sequencer Register 1 bit-0 (which selects between 8 and 9 bits per character) and will continue to perform that function in SR1 if bits 1-2 of this register are 0 (the default state). Changing bit-0 of this register will also change SR1 bit-0 and vice versa (they are the same physical bit internally). This bit was duplicated here for programmer convenience, since its function was expanded into a field that would not fit in the standard register.

Bit 1 is cleared automatically by the hardware if Sequencer register SR1 is written. Bit-2 is currently ignored, but should be written to 0 by the user for compatibility with future chip versions.

10.7 Extensions Bandwidth Control Register: BWC

I/O Port Address: 3C5
Index: 86

Bit #	Description	Access	Reset By	Reset State
7 (msb)	(reserved)			
6	(reserved)			
5	CMGA Bandwidth Bit-1 (not in rev D,E)	R/W	Reset or Sync Reset	0
4	CMGA Bandwidth Bit-0 (not in rev D,E)	R/W	Reset or Sync Reset	0
3	(reserved)			
2	EGA/VGA Bandwidth Bit-2	R/W	Reset or Sync Reset	0
1	EGA/VGA Bandwidth Bit-1	R/W	Reset or Sync Reset	0
0 (lsb)	EGA/VGA Bandwidth Bit-0	R/W	Reset or Sync Reset	0

Bit Descriptions

Bit 7-4 This field selects the memory bandwidth in CMGA states according to the following table (assuming 120ns rams):

xx00 1:4 CPU to CRT interleave (28 MHz 8-dot, 40 MHz 9-dot)

xx01 1:1 CPU to CRT interleave (20 MHz 8/9-dot)

xx10 (reserved)

xx11 1:7 CPU to CRT interleave (33 MH 8-DOT, 9-DOT FORCES 1:4)

The interleave is automatically forced to 1:4 if 9-dot characters and 1:7 interleave are both slected. The interleave is automatically forced to 3:2 for CLKIN/2 mode ('low-res' or '40-column').

Bit 3-0 This field selects the memory bandwidth in EGA/VGA amd TXT states according to the following table (assuming 120ns RAMs):

x000 Interleave selected by SR1 bit-1: 0 = 1:4, 1 = 3:2

x001 1:1 CPU to CRT interleave (20 MHz 8/9-dot)

x010 1:2 CPU to CRT interleave (20 MHz 6-dot)

x011 1:7 CPU to CRT interleave (33 MHz 8-dot)

x100 1:4 CPU to CRT interleave (28 MHz, 32 MHz 8/9-dot)

x101 3:2 CPU to CRT interleave (28 MHz CLKIN/2 modes)

x110 Reserved for future use

x111 Reserved for future use

The above interleave notation is interpreted as follows: 1:4 interleave indicates that one CPU cycle is allocated for every four CRT cycles (1-out-of-5 allocation of memory cycles to procesor read/write operations)

Note also that when video memory is not otherwise occupied in refreshing the screen or fetching graphics cursor data, that ALL memory cycles are available for CPU access (in effect, 1:0 interleave). This occurs during horizontal and vertical retrace and any time that video is disabled (e.g., Attribute Controller Index Register Bit-5 = 0), except for video memory refresh cycles (which occur for 5 cycles at the start of horizontal retrace) and pointer mask read cycles (which occur for 2 cycles following the refresh cycles if the pointer is enabled).

It is the responsibility of the programmer to set these bits correctly according to the dot clock frequency selected, the number of pixels per character clock, and whether the input clock is being divided by 2. Incorrect settings will result in erratic operation of display memory read/write operations and/or displayed data. Contact **Cirrus Logic** for more specific information on the correct settings of these bits for particular sets of timing parameters.

10.8 Extensions ROM Control Register: ROMC

I/O Port Address: 3C5

Index: 87

Bit #	Description	Access	Reset By	Reset State
7 (msb)	ROM Disable	R/W	Reset	0
6	-unused-			
5	-unused-			
4	-unused-			
3	-unused-			
2	-unused-			
1	-unused-			
0 (lsb)	-unused-			

Bit Descriptions

Bit 7 ROM Disable

When this bit is set to 1, the 610/620 board will ignore BIOS read operations. When this bit is set to 0, the 610/620 board will respond to BIOS read operations with data from the BIOS ROM.

Bit 6-0 Unused

10.9 Extensions Screen B Preset Row Scan Register: SBPR

I/O Port Address: 3C5

Index: 88

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-		Reset	
6	-unused-			
5	-unused-			
4	Screen B Preset Row Scan Bit-4	R.W	Reset or SRO-D1=0 (Sync Reset)	0
3	Screen B Preset Row Scan Bit-3	R/W	Reset or SRO-D1=0 (Sync Reset)	0
2	Screen B Preset Row Scan Bit-2	R/W	Reset or SRO-D1=0 (Sync Reset)	0
1	Screen B Preset Row Scan Bit-1	R/W	Reset or SRO-D1=0 (Sync Reset)	0
0 (lsb)	Screen B Preset Row Scan Bit-0	R/W	Reset or SRO-D1=0 (Sync Reset)	0

This register contains the Preset Row Scan value for the start of screen B. This register is used to load the character scan row counter when the line compare register compares with the current horizontal scan (see CRTC register CR18). This register allows split-screen smooth scrolling to be performed on the lower screen of the split screen (screen B). Refer to the Screen A Preset Row Scan Register (CR8) for further information on split-screen smooth scrolling.

10.10 Extensions Font Control Register: FONTC

I/O Port Address: 3C5

Index: 89

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-		Reset	
6	Plane 3 Font Enable	R/W	Reset	0
5	PS2 CGA Vsync Width Ctl	R/W		
4	PS2 CGA Hsync Width Ctl	R/W		
3	CMGA Font Position	R/W		
2	CMGA Font Pointer Bit-2	R/W		
1	CMGA Font Pointer Bit-1	R.W		
0 (lsb)	CMGA Font Pointer Bit-0	R/W		

Font information is normally located in non-software-accessable ROMs in the real CGA and MGA. The 610/620 has RAM-based font tables, so requires a place to put font information which doesn't conflict with the EGA/vVGA fonts. This is especially important for automatically switching into CGA or MGA mode from EGA/VGA mode where either an 8-high or 14-high font may be available already (or may not). This register therefore controls where the font information is located and how it is arranged. The programmer has the option of locating the CMGA font information in the unused upper scan lines of the EGA/VGA font tables (where is will get saved and restored automatically by existing software) or in locations normally inaccessable by the standard EGA or VGA. In either case, font information is located in plane 2 for all modes.

Bit Descriptions

Bit 6 Plane 3 Font Enable

Only bit 6 of this register exists in G/A. Setting this bit selects the font from plane3 instead of plane2. This bit has power up reset state of "0" in G/A. This bit exists in S/C for the readback convenience and does not have reset state.

Bit 5-4 PS2 CGA Vsync/Hsync Width Control

In CGA HSYNC and VSYNC have a standard width (i.e., the width cannot be programmed). This width fits TTL monitors for which CGA was originally conceived. In order to allow CGA programs to run on new monitors, like the fixed frequency monitors, the H/VSYNC pulse width has to be programmed to fit the monitor specification.

When bits 4 and/or 5 are high, the circuit which normally restricts H/VSYNC width to a standard value in CGA is bypassed and the width becomes programmable. The programmability is restricted to 6 bits (see 6845 Register R3 description).

Bit 3 CMGA Font Position

Setting this bit to 0 causes font information to be fetched from increasing addresses beginning at byte 0 of the indicated character area in the font table while in CGA or MGA emulation mode (i.e., in the same manner as for EGA/VGA font information). Setting this bit to 1 causes font information to be fetched from decreasing addresses beginning at byte 31 of the indicated character area in the font table.

Typically, when the EGA is in 25-line mode, a 14-line font is loaded into the font tables. In this mode, the 610/620 also loads an 8-line font in reverse order into the upper end of each character area. So to set up for automatic switching into CGA mode, this bit is set to 1 and to set up for automatic switching into MGA mode, this bit is set to 0.

When the EGA is in 43-line mode, an 8-line font is loaded into the font tables. In this mode, the 610/620 also loads a 14-line font in reverse order into the upper end of each character area. So to set up for automatic switching into CGA mode, this bit is set to 0. To set up for automatic switching into MGA mode, this bit is set to 1.

Bit 2-0 CMGA font pointer

These bits determine where the font information is located when in CGA or MGA modes. The value in this field indicates one of eight 8KB blocks in plane 2. Note that values of 0, 2, 4, and 6 indicate existing fonts 0, 1, 2, and 3 respectively. Odd values indicate the other four 8KB blocks which are not currently used for font information in the standard EGA but are used in the VGA.

The 8K byte blocks are arranged as 256 consecutive groups of 32 bytes each (8 bits per character times 32 scan lines each).

Font selection in EGA/VGA modes is controlled by the character attribute value and Sequencer Register 3 (Character Map Select).

10.11 Extensions LCD Control Register: LCDCNTLI

I/O Port Address: 3C5

Index: 8A

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Enable Power Save	R/W	Reset	0
6	Force 8-dots text mode	R/W	Reset	0
5	Unused	R/W	Reset	0
4	Divide external clock by 2 for LCD	R/W	Reset	0
3	Use Multiple Frequency Crystal	R/W	Reset	0
2	ROM Page bit-2	R/W	Reset	0
1	ROM Page bit-1	R/W	Reset	1
0 (lsb)	ROM Page bit-0	R/W	Reset	1

Bit Descriptions

Bit 7 In Power Save mode, the data paths for video signal processing will be disabled, and the video memory will only be accessed for refreshing. (Setting this bit cuts off the clock to "GRAYSCALE" and "HALF-FRAME-BUFFER". This bit has no effect on SumtoGray palette. S/C cuts off the "ITS*" clock when this bit is set, thus turning off most of the data path in G/A.)

Bit 6 VGA and MGA text modes are normally 9 dot modes. This bit will force VGA and MGA text modes to run with 8 dots per character. This bit will take effect in CRTC modes as well as in LCD modes.

Bit 5 Unused.

Bit 4 When this bit is set to 1, the external clock selected is divided by 2 before being used as the internal primary clock signal. Note that the sequencer registers may be programmed to further divide this primary clock signal by 2 in 40 column modes.

Bit 3 When this bit is set to 1, some clock input pins are used as outputs to drive an external multiple frequency crystal. When this bit is set to 0, multiple external clock sources can be used.

Bit 2-0 This 3-bit field is always substituted for the most significant three bits of a 16 bit BIOS ROM address when system bus address during a BIOS READ points to the highest 8K of the 32K BIOS segment. This allows access to 4 additional 8K pages in the BIOS. To access the highest 8K of the 32K BIOS segment at C:0000, this field must be programmed to 011, its reset state.

10.12 Screen B Preset Row Scan: SBPR

I/O Port Address: 3C5

Index: 8B

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-		Reset	
6	-unused-			
5	-unused-			
4	Screen B Preset Row Scan Bit-4	R.W	Reset or SRO-D1=0 (Sync Reset)	0
3	Screen B Preset Row Scan Bit-3	R/W	Reset or SRO-D1=0 (Sync Reset)	0
2	Screen B Preset Row Scan Bit-2	R/W	Reset or SRO-D1=0 (Sync Reset)	0
1	Screen B Preset Row Scan Bit-1	R/W	Reset or SRO-D1=0 (Sync Reset)	0
0 (lsb)	Screen B Preset Row Scan Bit-0	R/W	Reset or SRO-D1=0 (Sync Reset)	0

This register contains the Preset Row Scan value for the start of screen B. This register is used to load the character scan row counter when the line compare register compares with the current horizontal scan (see CRTC register CR18). This register allows split-screen smooth scrolling to be performed on the lower screen of the split screen (screen B). Refer to the Screen A Preset Row Scan Register (CR8) for further information on split-screen smooth scrolling.

10.13 Extensions Screen B Start Address High Register: SBSH

I/O Port Address: 3C5

Index: 8C

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Screen B Start Address Bit-15	R/W	Reset or SRO-D1=0 (Sync Reset)	0
6	Screen B Start Address Bit-14	R/W	Reset or SRO-D1=0 (Sync Reset)	0
5	Screen B Start Address Bit-13	R/W	Reset or SRO-D1=0 (Sync Reset)	0
4	Screen B Start Address Bit-12	R/W	Reset or SRO-D1=0 (Sync Reset)	0
3	Screen B Start Address Bit-11	R/W	Reset or SRO-D1=0 (Sync Reset)	0
2	Screen B Start Address Bit-10	R/W	Reset or SRO-D1=0 (Sync Reset)	0
1	Screen B Start Address Bit-9	R/W	Reset or SRO-D1=0 (Sync Reset)	0
0 (lsb)	Screen B Start Address Bit-8	R/W	Reset or SRO-D1=0 (Sync Reset)	0

This register contains the upper 8 bits of the start address for screen B (the lower of the two screens in split-screen mode). This address is relative to the start of video memory. Refer to the descriptions of CRTC registers CR8, CRC, CRD, CR18 and extension registers ER8 and ERD for more information on split-screen mode.

10.14 Extensions Screen B Start Address Low Register: SBSL

I/O Port Address: 3C5

Index: 8D

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Screen B Start Address Bit-7	R/W	Reset or SRO-D1=0 (Sync Reset)	0
6	Screen B Start Address Bit-6	R/W	Reset or SRO-D1=0 (Sync Reset)	0
5	Screen B Start Address Bit-5	R/W	Reset or SRO-D1=0 (Sync Reset)	0
4	Screen B Start Address Bit-4	R/W	Reset or SRO-D1=0 (Sync Reset)	0
3	Screen B Start Address Bit-3	R/W	Reset or SRO-D1=0 (Sync Reset)	0
2	Screen B Start Address Bit-2	R/W	Reset or SRO-D1=0 (Sync Reset)	0
1	Screen B Start Address Bit-1	R/W	Reset or SRO-D1=0 (Sync Reset)	0
0 (lsb)	Screen B Start Address Bit-0	R/W	Reset or SRO-D1=0 (Sync Reset)	0

This register contains the lower 8 bits of the start address for screen B (the lower of the two screens in split-screen mode). This address is relative to the start of video memory. Refer to the descriptions of CRTC registers CR8, CRC, CRD, CR18 and extension registers ER8 and ERD for more information on split-screen mode.

10.15 Extensions G/A Chip Revision Register: GAREV

I/O Port Address: 3C5

Index: 8E

Bit #	Description	Access	Reset By	Reset State
7 (msb)	G/A Chip Revision Bit-7	R		
6	G/A Chip Revision Bit-6	R		
5	G/A Chip Revision Bit-5	R		
4	G/A Chip Revision Bit-4	R		
3	G/A Chip Revision Bit-3	R		
2	G/A Chip Revision Bit-2	R		
1	G/A Chip Revision Bit-1	R		
0 (lsb)	G/A Chip Revision Bit-0	R		

The G/A chip revision is determined by reading back this register.

The value returned will be fixed for each revision of the chip.

The value returned is 0AFh for chip revision 'A'.

10.16 Extensions S/C Chip Revision Register: SCREV

I/O Port Address: 3C5

Index: 8F

Bit #	Description	Access	Reset By	Reset State
7 (msb)	S/C Chip Revision Bit-7	R	-	-
6	S/C Chip Revision Bit-6	R	-	-
5	S/C Chip Revision Bit-5	R	-	-
4	S/C Chip Revision Bit-4	R	-	-
3	S/C Chip Revision Bit-3	R	-	-
2	S/C Chip Revision Bit-2	R	-	-
1	S/C Chip Revision Bit-1	R	-	-
0 (lsb)	S/C Chip Revision Bit-0	R	-	-

The S/C chip revision is determined by reading back this register.

The value returned will be fixed for each revision of the chip.

The value returned is 0AFh for chip revision 'A'.

10.17 Vertical Retrace Start: CR10

I/O Port Address: 3C5

Index: 90

Bit #	Description	3?5 Access	3C5 Access	Reset By	Reset State
7 (msb)	Vertical Retrace Start Bit-7	W	R/W		
6	Vertical Retrace Start Bit-6	W	R/W		
5	Vertical Retrace Start Bit-5	W	R/W		
4	Vertical Retrace Start Bit-4	W	R/W		
3	Vertical Retrace Start Bit-3	W	R/W		
2	Vertical Retrace Start Bit-2	W	R/W		
1	Vertical Retrace Start Bit-1	W	R/W		
0 (lsb)	Vertical Retrace Start Bit-0	W	R/W		

The Vertical Retrace Start register is a 9-bit address which defines the position of the vertical retrace start signal in terms of horizontal scan lines assuming the scan lines are numbered starting from 0 at the top of the screen. The low order 8 bits are programmed through this register, while the high order ninth bit is programmed through the CRTC Overflow register (CR7 bit-2).

This register is normally accessed at CRTC index 10 as a write-only register (read-back at this index returns the Light Pen High Address Register). The Eagle VGA also allows read/write access at extensions index 90 for state save and restore.

Refer to Figure 7-1 (see register CR0) for a summary of CRTC timing registers.

Note: This register is effective only in EGA/VGA mode (see the description of Eagle VGA extension register ER2F, the 'Active Adapter State' Register).

10.18 Vertical Retrace End: CR11

I/O Port Address: 3C5

Index: 91

Bit #	Description	3?5 Access	3C5 Access	Reset By	Reset State
7 (msb)	0=Normal, 1=Test	W	R/W		
6	0=Normal, 1=Test	W	R/W		
5	0=Enable Vertical Interrupt	W	R/W	Reset	1
4	0=Clear Vertical Interrupt	W	R/W	Reset	0
3	Vertical Retrace End Bit-3	W	R/W		
2	Vertical Retrace End Bit-2	W	R/W		
1	Vertical Retrace End Bit-1	W	R/W		
0 (lsb)	Vertical Retrace End Bit-0	W	R/W		

This register is normally accessed at CRTC index 11 as a write-only register (read-back at this index returns the Light Pen Low Address Register). The EEGA/VGA also allows read/write access at extensions index 91 for state save and restore.

Bit Descriptions

Bit 7 Test

For normal operation this bit must be set to "0". This bit is ignored by the Eagle VGA.

Bit 6 Test

For normal operation this bit must be set to "0".Setting this bit to 1 causes line counter bits 7-8 to be forced to 1's ('6845-compatibility' mode). This capability is never used.

Bit 5 A "0" will enable the vertical interrupt of the CRT Controller. (See Input Status Register 0 bit-7 at port address 3C2).

Bit 4 Clear Vertical Interrupt

This bit clears the vertical interrupt generated on the CRTINT output of the CRT controller. A "0" will clear the interrupt.

Bit 3-0 Vertical Retrace End

These 4 bits specify the horizontal scan line count at which the vertical retrace output pulse becomes inactive assuming the scan lines are numbered starting from 0 at the top of the screen. The four bits are compared with the four least significant bits of the vertical scan line counter. When the four counter bits are equal to the contents in this register, the vertical retrace is terminated. The Width W of the vertical retrace pulse can be determined from the following algorithm:

Value of Start Vertical Retrace register (CR10) + W = 4-bit value to be programmed into the Vertical Retrace End register.

Note that the four least significant bits of the algorithm result are to be programmed into this register. Thus the maximum retrace pulse width can only be 15 scan lines. Note also that if the blanking interval extends beyond the end of the screen, erratic behavior will result since the vertical scan line counter gets cleared after the number of scan lines programmed in the vertical total register.

Refer to Figure 7-1 (see register CR0) for a summary of CRTC timing registers.

Note: This register is effective only in EGA/VGA mode (see the description of Eagle VGA extension register ER2F, the 'Active Adapter State' Register).

10.19 Light Pen High: LPENH

I/O Port Address: 3C5

Index: 92

Bit #	Description	3?5 Access	3C5 Access	Reset By	Reset State
7 (msb)	Light Pen Address Bit-15	R	R/W		
6	Light Pen Address Bit-14	R	R/W		
5	Light Pen Address Bit-13	R	R/W		
4	Light Pen Address Bit-12	R	R/W		
3	Light Pen Address Bit-11	R	R/W		
2	Light Pen Address Bit-10	R	R/W		
1	Light Pen Address Bit-9	R	R/W		
0 (lsb)	Light Pen Address Bit-8	R	R/W		

The Light Pen High register contains the 8 high-order bits of the memory address at the time the light pen flip flop is set. The low order 8 bits are stored in the Light Pen Low register (LPENL at CRTC index 11). The LPENH and LPENL registers are normally read-only at CRTC index 10 and 11. However, the Eagle VGA also allows these registers to be accessed R/W at extension index 92 and 93 for state save and restore.

Refer to SLPEN and CLPEN for further information on loading the LPENH and LPENL registers.

This register is used in both CMGA and EGA/VGA modes (the two msbs are always loaded with 0 when the 6845 is active since the 6845 memory address register is only 14 bits wide).

10.20 Light Pen Low: LPENL

I/O Port Address: 3C5

Index: 93

Bit #	Description	3?5 Access	3C5 Access	Reset By	Reset State
7 (msb)	Light Pen Address Bit-7	R	R/W		
6	Light Pen Address Bit-6	R	R/W		
5	Light Pen Address Bit-5	R	R/W		
4	Light Pen Address Bit-4	R	R/W		
3	Light Pen Address Bit-3	R	R/W		
2	Light Pen Address Bit-2	R	R/W		
1	Light Pen Address Bit-1	R	R/W		
0 (lsb)	Light Pen Address Bit-0	R	R/W		

The Light Pen Low register contains the 8 low-order bits of the memory address at the time the light pen flip flop is set. The high order 8 bits are stored in the Light Pen High register (LPENH at CRTC index 10). The LPENH and LPENL registers are normally read-only at CRTC index 10 and 11. However, the Eagle VGA also allows these registers to be accessed R/W at extension index 92 and 93 for state save and restore.

Refer to SLPEN and CLPEN for further information on loading the LPENH and LPENL registers.

This register is used in both CMGA and EGA/VGA modes.

10.21 Extensions Pointer Pattern Address Register: PPA

I/O Port Address: 3C5
Index: 94

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Pointer Pattern Address Bit-13	R/W	Reset	1
6	Pointer Pattern Address Bit-12	R/W	Reset	1
5	Pointer Pattern Address Bit-11	R/W	Reset	1
4	Pointer Pattern Address Bit-10	R/W	Reset	1
3	Pointer Pattern Address Bit-9	R/W	Reset	1
2	Pointer Pattern Address Bit-8	R/W	Reset	1
1	Pointer Pattern Address Bit-7	R/W	Reset	1
0 (lsb)	Pointer Pattern Address Bit-6	R/W	Reset	1

This register contains the msbs of the address of the graphics pointer pattern in display memory. The format of the address into the 64Kx32 display memory are shown below:

Bit	Description
15	1
14	1
13	PPAH bit-7
12	PPAH bit-6
11	PPAH bit-5
10	PPAH bit-4
9	PPAH bit-3
8	PPAH bit-2
7	PPAH bit-1
6	PPAH bit-0
5	Mask (0 = 'and' mask, 1 = 'or' mask)
4	Pattern line # bit 4 (msb)
3	Pattern line # bit 3
2	Pattern line # bit 2
1	Pattern line # bit 1
0	Pattern line # bit 0 (lsb)

This allows the user to place the pattern on any 256-byte boundary in display memory. The pattern takes up 256 bytes and defaults to the last 256 bytes of display memory. The pattern consists of a 128-byte screen mask (which is ANDed with display memory at the current pointer location) followed by a 128-byte pointer mask (which is XORed with the result of the previous AND operation). This produces the resulting video data for the 32x32-pixel area covered by the graphics pointer.

The patterns consist of 32 consecutive 32-bit values which represent the 32 successive lines of the pointer pattern. These 32-bit patterns are stored in display memory across all 4 planes so that they can be fetched from display memory with two memory read operations (one for the screen mask and one for the pointer mask) during the horizontal retrace interval prior to the scan line on which they are required. Plane-0 bit-7 is shifted out first; plane-3 bit-0 is shifted out last.

Correspondence between the above display memory address and the location of the pattern in the system memory space is determined by the state of the graphics controller registers, but typically places the pointer pattern from 0AFF00H to 0AFFFFH (assuming the PPA register is set to 0FFH).

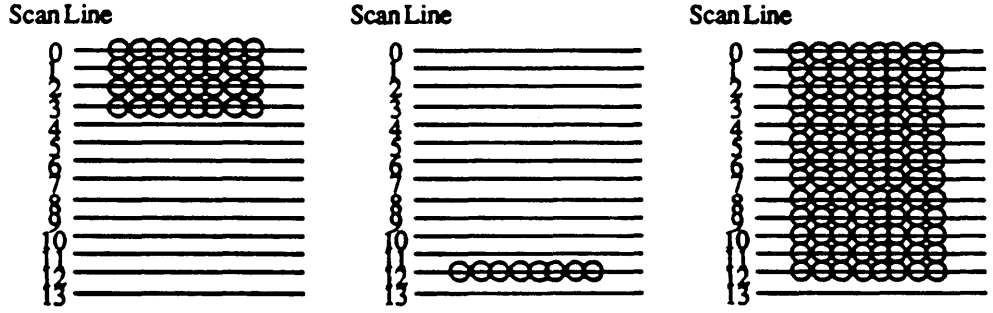
10.22 Extensions Cursor Height Adjust Register: CADJ

I/O Port Address: 3C5
Index: 95

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	Pointer Pattern Address Bit-10	R/W	-	-
3	Pointer Pattern Address Bit-9	R/W	-	-
2	Pointer Pattern Address Bit-8	R/W	-	-
1	Pointer Pattern Address Bit-7	R/W	-	-
0 (lsb)	Pointer Pattern Address Bit-6	R/W	-	-

This register contains a value used to adjust the 6845 cursor size (RA and RB) during 'Enhanced Text' mode (see 'STATE' register ER2F). This mode is actually a CGA text emulation mode in which the 610/620 uses the CRTC (i.e., EGA/VGA) to produce enhanced (8x14 or better) text instead of using the 6845 registers which would normally produce 8x8 text. In this mode, the 610/620 does, however, use the 6845 cursor start and end registers to control the size of the cursor by modifying their values with the contents of this register. This is done by adding the contents of this register to the contents of the cursor start and end registers if the value of those registers are greater than or equal to 4. The value in this register depends on the EGA/VGA font size, but is typically set to 5 for an 8x14 font and 7 for an 8x16 font.

Figure 10-1: Cursor Adjust Programming Examples



Note: The value written to this register doesn't take effect to modify the cursor shape until the CRTC Cursor Start or Cursor End registers are written to.

10.23 Extensions Caret Width Register: CW

I/O Port Address: 3C5

Index: 96

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Caret Width Bit-7	R/W	-	-
6	Caret Width Bit-6	R/W	-	-
5	Caret Width Bit-5	R/W	-	-
4	Caret Width Bit-4	R/W	-	-
3	Caret Width Bit-3	R/W	-	-
2	Caret Width Bit-2	R/W	-	-
1	Caret Width Bit-1	R/W	-	-
0 (lsb)	Caret Width Bit-0	R/W	-	-

This register contains the width in pixels of the caret (graphics text insertion point indicator). It is an 8-bit register which allows the caret to be up to 255 pixels wide. A value of 0 causes the caret to be turned off, as does a zero in bit-4 of the Cursor Attributes register (ER25).

10.24 Extensions Caret Height Register: CH

I/O Port Address: 3C5

Index: 97

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Caret Height Bit-7	R/W	-	-
6	Caret Height Bit-6	R/W	-	-
5	Caret Height Bit-5	R/W	-	-
4	Caret Height Bit-4	R/W	-	-
3	Caret Height Bit-3	R/W	-	-
2	Caret Height Bit-2	R/W	-	-
1	Caret Height Bit-1	R/W	-	-
0 (lsb)	Caret Height Bit-0	R/W	-	-

This register contains the height in pixels of the caret (graphics text insertion point indicator). It is an 8-bit register which allows the caret to be up to 255 pixels tall. A value of 0 causes the caret to be turned off, as does a zero in bit-4 of the Cursor Attributes register (ER25).

10.25 Extensions Caret Horizontal Position High Register: CXH

I/O Port Address: 3C5
Index: 98

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	-unused-			
3	-unused-			
2	Caret Horizontal Position Bit-10	R/W	-	-
1	Caret Horizontal Position Bit-9	R/W	-	-
0 (lsb)	Caret Horizontal Position Bit-8	R/W	-	-

This register contains the upper 3 bits of the Caret Horizontal Position in pixels from the left edge of the display screen. The lower 8 bits are contained in the CXL register.

Note: The value programmed into the Caret Horizontal Position is off by 1 or by 2 depending on the currently programmed character width: for 8-bit characters, add 1 to the actual position prior to programming the Caret Horizontal Position regisrers; for 9-bit characters, add 2 to the actual position.

For example, a value of 1 in horizontal position bits 0-10 would position the left-most pixel of the caret over the left-most pixel of the display screen if the display is programmed for 8-bit characters. A value of 2 in horizontal position bits 0-10 would produce the same result for 9-bit characters.

10.26 Extensions Caret Horizontal Position Low Register: CXL

I/O Port Address: 3C5

Index: 99

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Caret Horizontal Position Bit-7	R/W	-	-
6	Caret Horizontal Position Bit-6	R/W	-	-
5	Caret Horizontal Position Bit-5	R/W	-	-
4	Caret Horizontal Position Bit-4	R/W	-	-
3	Caret Horizontal Position Bit-3	R/W	-	-
2	Caret Horizontal Position Bit-2	R/W	-	-
1	Caret Horizontal Position Bit-1	R/W	-	-
0 (lsb)	Caret Horizontal Position Bit-0	R/W	-	-

This register contains the lower 8 bits of the Caret Horizontal Position in pixels from the left edge of the display screen. The upper 3 bits are contained in the CXH register.

Note: The value programmed into the Caret Horizontal Position is off by 1 or by 2 depending on the currently programmed character wideth: for 8-bit characters, add 1 to the actual position prior to programming the Caret Horizontal Position registers; for 9-bit characters, add 2 to the actual position.

For example, a value of 1 in horizontal position bits 0-10 would position the left-most pixel of the caret over the left-most pixel of the display screen if the display is programmed for 8-bit characters. A value of 2 in horizontal position bits 0-10 would produce the same result for 9-bit characters.

10.27 Extensions Caret Vertical Position High Register: CYH

I/O Port Address: 3C5
Index: 9A

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	-unused-			
3	-unused-			
2	-unused-			
1	Caret Vertical Position Bit-9	R/W	-	-
0 (lsb)	Caret Vertical Position Bit-8	R/W	-	-

This register contains the upper 2 bits of the Caret Vertical Position in scan lines from the upper edge of the display screen. A value of 0 in vertical position bits 0-9 would position the upper-most pixel of the caret over the upper-most pixel of the display screen.

10.28 Extensions Caret Vertical Position Low Register: CYL

I/O Port Address: 3C5

Index: 9B

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Caret Vertical Position Bit-7	R/W	-	-
6	Caret Vertical Position Bit-6	R/W	-	-
5	Caret Vertical Position Bit-5	R/W	-	-
4	Caret Vertical Position Bit-4	R/W	-	-
3	Caret Vertical Position Bit-3	R/W	-	-
2	Caret Vertical Position Bit-2	R/W	-	-
1	Caret Vertical Position Bit-1	R/W	-	-
0 (lsb)	Caret Vertical Position Bit-0	R/W	-	-

This register contains the lower 8 bits of the Caret Vertical Position in scan lines from the upper edge of the display screen. A value of 0 in vertical position bits 0-9 would position the upper-most pixel of the caret over the upper-most pixel of the display screen.

10.29 Extensions Pointer Horizontal Position High Register: PXH

I/O Port Address: 3C5
Index: 9C

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	-unused-			
3	-unused-			
2	Pointer Horizontal Position Bit-10	R/W	-	-
1	Pointer Horizontal Position Bit-9	R/W	-	-
0 (lsb)	Pointer Horizontal Position Bit-8	R/W	-	-

This register contains the upper 3 bits of the pointer horizontal position in pixels from the left edge of the display screen. A value of 0 in horizontal position bits 0-10 would position the left-most pixel of the pointer pattern over the left-most pixel of the display screen.

Note: GA-A will only update the counter with the value from this register at vertical retrace time.

10.30 Extensions Pointer Vertical Position Low Register: PXL

I/O Port Address: 3C5

Index: 9D

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Pointer Horizontal Position Bit-7	R/W	-	-
6	Pointer Horizontal Position Bit-6	R/W	-	-
5	Pointer Horizontal Position Bit-5	R/W	-	-
4	Pointer Horizontal Position Bit-4	R/W	-	-
3	Pointer Horizontal Position Bit-3	R/W	-	-
2	Pointer Horizontal Position Bit-2	R/W	-	-
1	Pointer Horizontal Position Bit-1	R/W	-	-
0 (lsb)	Pointer Horizontal Position Bit-0	R/W	-	-

This register contains the lower 8 bits of the pointer horizontal position in pixels from the left edge of the display screen. A value of 0 in horizontal position bits 0-10 would position the left-most pixel of the pointer pattern over the left-most pixel of the display screen.

See Note Page 10-28 for "PXH" register.

10.31 Extensions Pointer Vertical Position High Register: PYH

I/O Port Address: 3C5
Index: 9E

Bit #	Description	Access	Reset By	Reset State
7 (msb)	-unused-			
6	-unused-			
5	-unused-			
4	-unused-			
3	-unused-			
2	-unused-			
1	Pointer Vertical Position Bit-9	R/W	-	-
0 (lsb)	Pointer Vertical Position Bit-8	R/W	-	-

This register contains the upper 2 bits of the pointer vertical position in scan lines from the upper edge of the display screen. A value of 0 in vertical position bits 0-9 would position the upper-most pixel of the pointer pattern over the upper-most pixel of the display screen.

10.32 Extensions Pointer Vertical Position Low Register: PYL

I/O Port Address: 3C5

Index: 9F

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Pointer Vertical Position Bit-7	R/W	-	-
6	Pointer Vertical Position Bit-6	R/W	-	-
5	Pointer Vertical Position Bit-5	R/W	-	-
4	Pointer Vertical Position Bit-4	R/W	-	-
3	Pointer Vertical Position Bit-3	R/W	-	-
2	Pointer Vertical Position Bit-2	R/W	-	-
1	Pointer Vertical Position Bit-1	R/W	-	-
0 (lsb)	Pointer Vertical Position Bit-0	R/W	-	-

This register contains the lower 8 bits of the pointer vertical position in scan lines from the upper edge of the display screen. A value of 0 in vertical position bits 0-9 would position the upper-most pixel of the pointer pattern over the upper-most pixel of the display screen.

10.33 Extensions Graphics Controller Memory Latch 0: GRL0

I/O Port Address: 3C5

Index: A0

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Graphics Controller Memory Latch 0 Bit-7	R/W	-	-
6	Graphics Controller Memory Latch 0 Bit-6	R/W	-	-
5	Graphics Controller Memory Latch 0 Bit-5	R/W	-	-
4	Graphics Controller Memory Latch 0 Bit-4	R/W	-	-
3	Graphics Controller Memory Latch 0 Bit-3	R/W	-	-
2	Graphics Controller Memory Latch 0 Bit-2	R/W	-	-
1	Graphics Controller Memory Latch 0 Bit-1	R/W	-	-
0 (lsb)	Graphics Controller Memory Latch 0 Bit-0	R/W	-	-

This register is actually the memory data latch which gets loaded from plane 0 data whenever video memory is read by the CPU. This register exists in a standard EGA and VGA, it just can't be accessed directly as it can in the 610/620.

Note: This latch may also be read @ 3?5.22 for IBM VGA® compatibility.

10.34 Extensions Graphics Controller Memory Latch 1: GRL1

I/O Port Address: 3C5

Index: A1

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Graphics Controller Memory Latch 1 Bit-7	R/W	-	-
6	Graphics Controller Memory Latch 1 Bit-6	R/W	-	-
5	Graphics Controller Memory Latch 1 Bit-5	R/W	-	-
4	Graphics Controller Memory Latch 1 Bit-4	R/W	-	-
3	Graphics Controller Memory Latch 1 Bit-3	R/W	-	-
2	Graphics Controller Memory Latch 1 Bit-2	R/W	-	-
1	Graphics Controller Memory Latch 1 Bit-1	R/W	-	-
0 (lsb)	Graphics Controller Memory Latch 1 Bit-0	R/W	-	-

This register is actually the memory data latch which gets loaded from plane 1 data whenever video memory is read by the CPU. This register exists in a standard EGA and VGA, it just can't be accessed directly as it can in the 610/620.

Note: This latch may also be read @ 3?5.22 for IBM VGA® compatibility.

10.35 Extensions Graphics Controller Memory Latch 2: GRL2

I/O Port Address: 3C5

Index: A2

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Graphics Controller Memory Latch 2 Bit-7	R/W	-	-
6	Graphics Controller Memory Latch 2 Bit-6	R/W	-	-
5	Graphics Controller Memory Latch 2 Bit-5	R/W	-	-
4	Graphics Controller Memory Latch 2 Bit-4	R/W	-	-
3	Graphics Controller Memory Latch 2 Bit-3	R/W	-	-
2	Graphics Controller Memory Latch 2 Bit-2	R/W	-	-
1	Graphics Controller Memory Latch 2 Bit-1	R/W	-	-
0 (lsb)	Graphics Controller Memory Latch 2 Bit-0	R/W	-	-

This register is actually the memory data latch which gets loaded from plane 2 data whenever video memory is read by the CPU. This register exists in a standard EGA and VGA, it just can't be accessed directly as it can in the 610/620.

10.36 Extensions Graphics Controller Memory Latch 3: GRL3

I/O Port Address: 3C5

Index: A3

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Graphics Controller Memory Latch 3 Bit-7	R/W	-	-
6	Graphics Controller Memory Latch 3 Bit-6	R/W	-	-
5	Graphics Controller Memory Latch 3 Bit-5	R/W	-	-
4	Graphics Controller Memory Latch 3 Bit-4	R/W	-	-
3	Graphics Controller Memory Latch 3 Bit-3	R/W	-	-
2	Graphics Controller Memory Latch 3 Bit-2	R/W	-	-
1	Graphics Controller Memory Latch 3 Bit-1	R/W	-	-
0 (lsb)	Graphics Controller Memory Latch 3 Bit-0	R/W	-	-

This register is actually the memory data latch which gets loaded from plane 3 data whenever video memory is read by the CPU. This register exists in a standard EGA and VGA, it just can't be accessed directly as it can in the 610/620.

Note: This latch may also be read @ 3?5.22 for IBM VGA® compatibility.

10.37 Extensions Clock Select Register: CLK

I/O Port Address: 3C5

Index: A4

Bit #	Description	Access	Reset By	Reset State
7 (msb)	CMGA Clock Select Bit-2 (A)/CMGA CLK Override (D,E)	R/W	Reset	0
6	CMGA Clock Select Bit-1 (A)	R/W (A)	Reset	0
5	CMGA Clock Select BIt-0 (A)	R/W (A)	Reset	0
4	EGA/VGA Clock Select Bit-2	R/W	Reset	0 (D,E), 1 (A)
3	EGA/VGA Clock Select Bit-1 (same as MISC Reg Bit-3)	R/W		
2	EGA/VGA Clock Select Bit-1 (same as MISC Reg Bit-2)	R/W		
1	-unused-			
0 (lsb)	-unused-			

Bit Descriptions

Bit 7 (Rev D,E) CMGA Clock Override

When this bit is 0, clocks are set to fixed values in CMGA modes (14 MHz in CGA mode and 16 MHz in MGA mode). When this bit is set to 1, the clock in CMGA modes is selected by bits 2-4 of this register.

Bit 7-5 (Rev A) CMGA Clock Select

This 3-bit field selects clocks for CMGA modes; bits 2-4 select clocks and switches for EGA/VGA modes.

Bit 4 When this bit is set to 0, Clock Select 1 and 0 are used to select clock and switch sources as defined in the EGA. When this bit is set to 1, four additional clock and switch sources can be selected (typically, the additional clock sources are set up for VGA compatibility).

Bit 3-2 These are the same bits as bits 3-2 of the EGA/VGA Miscellaneous Output Register.

This register may be used to select 1 of 8 clock sources. If only 4 clock sources are required, the two bits in the Misc Output Register (bits 2 and 3) may be used to select the clock source, since bits 2 and 3 of this register are the same as Misc Output Register bits 2 and 3. If external clock sources are connected as shown in the table below, and bit-4 of this register is set to 0, EGA-standard clock sources may be selected using the MISC Output register; if bit-4 of this register is set to 1, VGA-standard clock sources may be selected:

Bit-4	Bit-3	Bit-2	Switch	Clock Source	Comment
0	0	0	Sw4	14.318MHz (from the PC Bus)	EGA Standard
0	0	1	Sw3	16.257 MHz	EGA Standard
0	1	0	Sw 2	25.172 MHz/Feature Connector	Eagle Deluxe 24 MHz
0	1	1	Sw 1	32.514.MHz	610/620 Extension
1	0	0	Sw 5	25.172 MHz	VGA Standard
1	0	1	Sw 6	28.332 MHz	VGA Standard
1	1	0	Sw 7	20.000 MHz	610/620 Extension
1	1	1	Sw 8	40.000 MHz	610/620 Extension

As shown in the table, these same three CLKSEL bits may also be used to select 1 of 4 or 1 of 8 switches (EGA standard is 4 switches; the 610/620 provides for 4 more if desired).

These switches are typically read at power up by the BIOS by setting the CLKSEL bits to successive values and reading the switches from Input Status Register 0 bit-4 one at a time (swtiches read as 0 if closed). These switches are used to inform the BIOS of the type of monitor attached and the initial mode of operation. The 610/620 PCB is designed to allow the analog monitor type code bits to be read back in place of the switches (in Feature Read Register bit-4) when the digital video outputs are enabled (Misc Output Register bit-4 = 0). If connected in this manner, the switches are readable only when digital video is disabled (Misc Output Register bit-4 = 1).

10.38 Extensions Cursor Attributes Register: CURS

I/O Port Address: 3C5

Index: A5

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Pointer Enable	R/W	Reset	0
6	Caret Enable	R/W	Reset	0
5	Caret Color (0=Black=0000, 1=White=1111)	R/W	Reset	0
4	Caret Mode (0=Replace, 1=Invert)	R/W	Reset	0
3	Cursor Mode (0=Replace, 1=Invert)	R/W	Reset	0
2	Blink Rate (0=Fast, 1=Slow)	R/W	Reset	0
1	Caret Blink Disable	R/W	Reset	0
0 (lsb)	Cursor Blink Disable	R/W	Reset	0

This register controls the appearance of the text cursor, graphics caret, and mouse pointer Note that this register is also reset by synchronous reset in chip rev D.

Bit Descriptions

Bit 7 Pointer Enable

Setting this bit to 1 enables the pointer logic to display the 32x32-pixel hardware mouse pointer on the screen at a location determined by the Pointer Horizontal and Vertical Position Registers (PXH/PXL and PYH/PYL). Setting this bit to 0 (the default state) disables this feature. The screen mask pattern for the pointer is fetched from display memory at absolute location Ann00 or Bnn00 for 128 bytes where nn is the contents of the Pointer Position Address Register (PPA at extensions index 94). The screen mask is ANDed with video memory data at the output of the color palette. The pointer mask pattern for the pointer is fetched from display memory at absolute location Ann80 for 128 bytes. The pointer mask is XORed with the results of the previous screen mask AND operation to produce the final video output. This results in the following truth table for the mask data:

ScreenMask	PointerMask	Resulting Screen Pixel
0	0	Black
0	1	White
1	0	Same as original pixel (pointer transparent)
1	1	Inverse of original pixel

The pointer is available in EGA/VGA (CRTC) modes only. The pointer is not available in CMGA (6845) modes.

Bit 6 Caret Enable

Setting this bit to 1 enables the caret logic to display an insertion point indicator.

The graphics caret size (up to 255x255 pixels) is controlled by the Caret Height and Width Registers (CH and CW). The location is controlled by the Caret Horizontal and Vertical Position Registers (CXH/CXL and CYH/CYL). The caret may be enabled in either graphics or text modes.

The text cursor size (up to 32 scan rows) is controlled by the 6845/CRTC Cursor Start and End Row Registers (RA/CRA and RB/CRB). The location is controlled by the Cursor Position Register (CRE and CRF). The text cursor is only enabled in text mode.

The caret is available in EGA/VGA (CRTC) modes only. The caret is not available in CMGA (6845) modes. The caret is inserted into the video data stream prior to the attribute controller color palette so that the caret color is modified by the palette. The caret position is adjusted by smooth scrolling and by horizontal pixel

panning.

Bit 5 Caret Color

State 0 = Black caret (for use on white background) (Black = color 0000)

State 1 = White caret (for use on black background) (White = color 1111)

Bit 4 Caret Mode

State 0 shows screen under caret in fixed-color when caret is on (color set by bit-5)

State 1 shows screen under caret in reverse video when caret is on (XOR with bit-5)

Bit 3 Cursor Mode

State 0 overwrites screen under cursor with foreground color when cursor is on

State 1 shows character under cursor in reverse video when cursor is on

Bit 2 Blink Rate

State 0 = Fast blink - caret/cursor blinks at 1/16 of the current field rate (Vrtc ÷ 16)

State 1 = Slow blink - caret/cursor blinks at 1/32 of the current field rate (Vrtc ÷ 32)

This bit is used to control the cursor/caret blink rate in EGA modes and the cursor blink only in CMGA modes (the caret is not available in CMGA modes).

In the IBM EGA and VGA, the cursor blink rate is fixed at the 'Fast Blink' rate. Character blink, if used, occurs at the 'Slow Blink' rate.

Fast Blink: 1/16 of the field rate means off for 8 vertical retrace times (approximately 1/8 second at 60Hz and 1/6 second at 50Hz) and on for 8 vertical retrace times. This is approximately 4 Hz at 60 Hz vertical frequency and 3 Hz at 50 Hz vertical.

Slow Blink: 1/32 of the field rate means off for 16 vertical retrace times and on for 16. This is approximately 2 Hz at 60 Hz vertical frequency and 1.5 Hz at 50 Hz vertical.

Bit 1 Caret blink disable

State 1 = Disable caret blink

State 0 = Enable caret blink

Bit 0 Cursor blink disable

State 1 = Disable cursor blink

State 0 = Enable cursor blink

In EGA/VGA modes, this bit is used to enable/disable cursor blink. If enabled, bit-2 of this register determines the blink rate.

In CMGA modes, this register has no effect on cursor operation. Bits 5 and 6 of the 6845 Cursor Start Register (RA) determine whether cursor blink is enabled or disabled and, if enabled, the blink rate:

6845 Register A bits 6-5	Cursor Function
0 0	Cursor Fast Blink
0 1	No Cursor
1 0	No Cursor
1 1	Cursor Slow Blink

10.39 Reserved

I/O Port Address: 3C5
Index: A6

10.40 Extensions Mode Switch Control Register: SWITCH

I/O Port Address: 3C5

Index: A7

Bit #	Description	Access	Reset By	Reset State
7 (msb)	CRTC Timing Check (Sanity Bit)	R/W	Reset	0
6	Enable S3toS2 Smartswitch B	R/W	Reset	0
5	Enable S3toS2 Smartswitch A	R/W	Reset	0
4	Enable Enhanced Text Smartswitch	R/W	Reset	0
3	Enable MGA Smartswitch	R/W	Reset	0
2	Enable CGA Smartswitch	R/W	Reset	0
1	Enable EGA/VGA Smartswitch B	R/W	Reset	0
0 (lsb)	Enable EGA/VGA Smartswitch A	R/W	Reset	0

These bits are programmed to control state transitions in the Smartswitch state machine. Specific state transitions can be enabled or disabled by setting and resetting these bits.

Bit Descriptions

Bit 7 CRTC Sanity Bit

This bit is cleared by software after CRTC timing registers are loaded with a complete set of values. This bit is cleared by hardware if any of the CRTC timing registers 0-9 are changed. This bit is used to detect whether a CGA or MGA applications program has messed up the CRTC timing registers (presumably thinking it was changing 6845 registers at the same locations) and is used to prevent automatic switching from CGA or MGA mode back into EGA/VGA mode or Enhanced Text (TXT) mode. If the application program behaves 'correctly', it will turn off video via the mode port before changing any of the 6845 registers. In this case, the automatic switching mechanism will switch on the mode port hit thus write protecting the CRTC registers and allowing a Smartswitch return to EGA/VGA mode. This bit is used to catch the case where the program doesn't behave correctly and just starts programming the 6845 registers with no warning. By detecting this case, the program will just stay in CGA/MGA mode until software intervention (BIOS set mode) rather than attempting to go back to EGA/VGA mode with an illEGA/VGA1 set of timing values in the CRTC (and possibly damaging a CRT monitor by giving it incorrect timing signals.)

Bit 6 Enable TXT to CGA Smartswitch B

Enable automatic switching from Enhanced Text mode to CGA mode on detection of a write to 6845 registers 0-9.

Bit 5 Enable TXT to CGA Smartswitch A

Enable automatic switching from Enhanced Text mode to CGA mode on detection of a write to the CGA mode register with anything other than '80-column text mode' (binary 'xxx01x01').

Bit 4 Enable Enhanced Text Smartswitch

Enable automatic switching from CGA mode to Enhanced Text mode on detection of a write to the CGA mode register in color mode (i.e., at 3D8) with '80-column text mode' (binary 'xxx01x01') and the 6845 Character Cell Height register contains a 7 (cell height = 8). Enhanced Text mode allows more readable EGA/VGA-type enhanced text to be displayed in place of CGA text.

Bit 3 Enable MGA Smartswitch

Enable automatic switching from EGA/VGA mode to MGA mode on detection of a write to the MGA mode port in mono mode (i.e.., AT 3B8).

Bit 2 Enable CGA Smartswitch

Enable automatic switching from EGA/VGA mode to CGA mode on detection of a write to the CGA mode register in color mode (port 3D8) with anything other than '80-column text mode' (binary 'xxx01x01') or detection of a write to the CGA color register in color mode (port 3D9).

Bit 1 Enable EGA/VGA Smartswitch B

Enable automatic switching to EGA/VGA mode from any other mode on detection of a write to any EGA/VGA-specific register (port 3Cx).

Bit 0 Enable EGA/VGA Smartswitch A

Enable automatic switching to EGA/VGA mode from any other mode on detection of a sequencer synchronous reset (writing 0 to bit-1 of SR0).

SMARTSWITCH STATE TRANSITION EQUATIONS - REV E & A

Cond 1 =

CGA-Auto • MM* • WE/CGA-Mode/ • ((DB[7:0]≠xxx01x01)+(6845-MaxScan≠7)) • DB[3]=1
;Write to CGA Mode (3D8) +

CGA-Auto • MM* • WE/CGA-Mode/ • CGA-Mode[1] = 1
;Only if in graphics mode
;Write to CGA Color (3D9)

Cond 2 =

EEGATXT • CRTC-Sane • WE/CGA-Mode/ • (DB[7:0] = xxx01x01) • (6845-MaxScan = 7)
;Write to CGA Mode (3D8)

Cond 3 =

TXTtoCGAA• WE/CGA-Mode/ • ((DB[7:0] ≠ xxx01x01)+(6845-MaxScan ≠ 7))
;Write to CGA Mode (3D8) +

TXTtoCGAA WE/addr =xD1 + xD# + xD5 + xD7/ • (6845-Index = 0-9)
;Write to 6845 R0-9 (3D1)

Cond 4 =

EEGATXT • CRTC-Sane • WE/CGA-Mode/
;Write to CGA Mode (3D8)

• CGA-Auto • MM* • (((DB[7:0] = xxx01x01) • (6845-MaxScan = 7) + (DB[3] = 0))
;Video-on/80col or video-off

Cond 5 =

MGA-Auto • MM • WE/MGA-Mode/
;Write to MGA Mode (3B8)

Cond 6 =

EGA-AutoA • WE/addr=xCx/
;Write to any EGA reg(3Cx)

Cond 7 =

Cond6 • CRTC-Sane

where:

6845-MaxScan = 6845 Register R9 (Character Cell Height Register: a value of 7 indicates a cell height of 8)

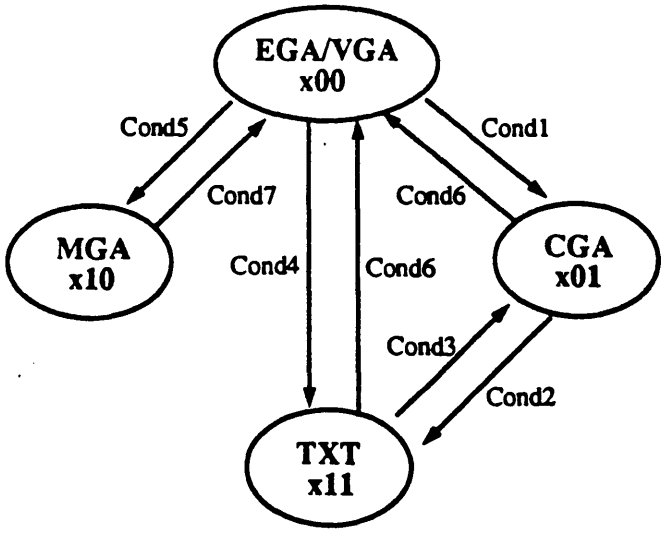
Data pattern xxx01x01 written to the CMGA mode register indicates video on and 80-column text

CRTC-Sane = 1 indicates that the CRTC contains valid parameters for display of 80-column EGA enhanced text

CRTC-Sane is set by software and cleared by hardware on any write to CRTC aregisters 0-9 in EGA mode

Mode register bit-3 is the video enable bit (equations are written to transition to TXT if Mode write with video off)

Figure 10-2: Smartswitch State Transitions



Note: Smartswitch transitions do not effect the EGA/VGA control bit (state bit-2).

10.41 Extensions NMI Mask Register 1: NMI1

I/O Port Address: 3C5

Index: A8

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Mono mode port accessed in color mode Mask	R/W	Reset	0
6	Color mode port accessed in mono mode Mask	R/W	Reset	0
5	-unused-	R/W	Reset	0
4	Port Register 3D9 Update Mask (CGA Color)	R/W	Reset	0
3	Port Register 3D8 Update Mask (CGA Mode)	R/W	Reset	0
2	Port Register 3BF Update Mask (MGA Config)	R/W	Reset	0
1	Port Register 3B9 Update Mask (MGA Set Light Pen FF)	R/W	Reset	0
0 (lsb)	Port Register 3B8 Update Mask (MGA Mode)	R/W	Reset	0

Each bit enables (when set to 1) or disables (when set to 0) the generation of NMI interrupts when the corresponding register(s) is written. When the NMI type is disabled by setting the corresponding mask bit to 0, occurrences of events of that type are not recorded in the status registers.

Bit Descriptions

Bit 7 Mono Port Accessed in Color Mode

This bit controls whether an NMI is generated on writes to 3Bx when in color mode (color mode ports are at 3Dx).

Bit 6 Color Port Accessed in Mono Mode

This bit controls whether an NMI is generated on writes to 3Dx when in mono mode (mono mode ports are at 3Bx).

Bit 5 This bit is implemented as a read/write bit but is not currently connected to anything.

Bit 4 Port 3D9 Update Mask

This bit controls whether an NMI is generated on writes to the CGA Color register.

Bit 3 Port 3D8 Update Mask

This bit controls whether an NMI is generated on writes to the CGA Mode register.

Bit 2 Port 3BF Update Mask

This bit controls whether an NMI is generated on writes to the MGA Configuration register.

Bit 1 Port 3B9 Update Mask

This bit controls whether an NMI is generated on writes to the MGA Set Light Pen Flip Flop port.

Bit 0 Port 3B8 Update Mask

This bit controls whether an NMI is generated on writes to the MGA Mode register.

10.42 Extensions NMI Mask Register 2: NMI2

I/O Port Address: 3C5

Index: A9

Bit #	Description	Access	Reset By	Reset State
7 (msb)	CRTC Data Registers 10-18 Update Mask	R/W	Reset	0
6	CRTC/6845 Data Registers C-F Update Mask	R/W	Reset	0
5	CRTC/6845 Data Registers 0-B Update Mask	R/W	Reset	0
4	Feature Control Register Update Mask	R/W	Reset	0
3	Misc Output Register Update Mask	R/W	Reset	0
2	Attribute Controller Data Registers Update Mask	R/W	Reset	0
1	Graphics Controller Data Registers Update Mask	R/W	Reset	0
0 (lsb)	Sequencer Data Registers Update Mask	R/W	Reset	0

Each bit enables (when set to 1) or disables (when set to 0) the generation of NMI interrupts when the corresponding register(s) is updated. When the NMI type is disabled by setting the corresponding mask bit to 0, occurrences of events of that type are not recorded in the status registers.

NMIs are never produced on writes to index register.

Bit Descriptions

Bit 7 CRTC Data Registers 10-18 Update Mask

This bit controls whether an NMI is generated on writes to CRTC registers CR10-CR18. These registers are unique to the CRTC.

Bit 6 CRTC/6845 Data Registers C-F Update Mask

This bit controls whether an NMI is generated on writes to CRTC registers C-F. The registers at this index range are common to the 6845 and CRTC and work the same way for both.

Bit 5 CRTC/6845 Date Registers 0-B Update Mask

This bit controls whether an NMI is generated on writes to 6845/CRTC registers 0-B. The 6845 and CRTC both have registers at this index range, but the register sets have different functions.

Bit 4 Feature Control Register Update Mask

This bit controls whether an NMI is generated on writes to the EGA/VGA Feature Control register (port 3BA in mono mode or 3DA in color mode).

Bit 3 Misc Output Register Update Mask

This bit controls whether an NMI is generated on writes to the EGA/VGA Misc Output register (port 3C2 or 3C3).

Bit 2 Attribute Controller Data Registers Update Mask

This bit controls whether an NMI is generated on writes to the EGA/VGA Attribute Controller data registers (port 3C0).

Bit 1 Graphics Controller Data Registers Update Mask

This bit controls whether an NMI is generated on writes to the EGA/VGA Graphics Controller position or data registers (ports 3CA, 3CC, and 3CF).

Bit 0 Sequencer Data Registers Update Mask

This bit controls whether an NMI is generated on writes to the EGA/VGA Sequencer Registers (port 3C5).

10.43 Reserved

I/O Port Address: 3C5
Index: AA

10.44 Extensions NMI Status Register 1: NSTAT1

I/O Port Address: 3C5

Index: AB

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Mono mode port accessed in color mode	R/	Reset	0
6	Color mode port accessed in mono mode	R/	Reset	0
5	State Change	R/	Reset	0
4	Port Register 3D9 Updated (CGA Color)	R/	Reset	0
3	Port Register 3D8 Updated (CGA Mode)	R/	Reset	0
2	Port Register 3BF Updated (MGA Config)	R/	Reset	0
1	Port Register 3B9 Updated (MGA Set Light Pen FF)	R/	Reset	0
0 (lsb)	Port Register 3B8 Updated (MGA Mode)	R/	Reset	0

A bit in this register is set to 1 when the corresponding register(s) is updated and the corresponding mask bit is 1. Creating the condition which sets one of the bits in this register will also generate an NMI interrupt if so enabled by the corresponding mask bit in the NMI Mask 1 Register.

This register is read-only. A read operation on this register resets every bit to 0.

10.45 Extensions NMI Status Register 2: NSTAT2

I/O Port Address: 3C5

Index: AC

Bit #	Description	Access	Reset By	Reset State
7 (msb)	CRTC Data Registers 10-18 Updated	R/	Reset	0
6	CRTC/6845 Data Registers C-F Updated	R/	Reset	0
5	CRTC/6845 Data Registers 0-B Updated	R	Reset	0
4	Feature Control Register Updated	R	Reset	0
3	Misc Output Register Updated	R	Reset	0
2	Attribute Controller Data Registers Updated	R	Reset	0
1	Graphics Controller Data Registers Updated	R	Reset	0
0 (lsb)	Sequencer Data Registers Updated	R	Reset	0

A bit in this register is set to 1 when the corresponding register(s) is updated and the corresponding mask bit is 1. Creating the condition which sets one of the bits in this register will also generate an NMI interrupt if so enabled by the corresponding mask bit in the NMI Mask 1 Register.

This register is read-only. A read operation on this register resets every bit to 0.

10.46 Reserved

I/O Port Address: 3C5
Index: AD

10.47 Extensions NMI Data Cache: CACHE

I/O Port Address: 3C5

Index: AE

Bit #	First Read	Second Read	Third Read	Access	Reset By	Reset State
7 (msb)	Data[7]	Write	Cache Empty	R		
6	Data[6]	Addr[7:4] = D	Cache Overrun	R		
5	Data[5]	Addr[7:4] = C	Index[5]	R		
4	Data[4]	Addr[7:4] = B	Index[4]	R		
3	Data[3]	Addr[3]	Index[3]	R		
2	Data[2]	Addr[2]	Index[2]	R		
1	Data[1]	Addr[1]	Index[1]	R		
0 (lsb)	Data[0]	Addr[0]	Index[0]	R		

The NMI data cache is used to capture data from NMI-producing I/O write cycles (I/O write cycles which NMI Mask registers 1 and 2 have been set up to detect). Each such event to occur causes the corresponding bit in NMI Status Register 1 or 2 to be set and in addiition causes 3 bytes of information about the event to be saved in the cache. the first such event to occur following the setup of the NMI subsystem will cause the NMI line to be asserted; however, the CPU may not recognize the NMI until several such events have occurred. Therefore, the cache contains 4 sets of 3 save registers. Readback of the save registers occurs in sequence, with the first set of 3 bytes out of the cache corresponding to the first event to occur. The 3 bytes of information for each event are read in the order shown. The last byte of the 3 contains a bit which indicates if any more data remains in the cache. The cache contains data if and only if NSTAT1 or NSTAT2 are non-zero. If the cache is full (4 sets of save data values stored) and another NMI events occurs, an over-run bit is set and the data from that event is not saved (the cache contents are preserved.)

Bit Descriptions (First Sequential Read)

Bit 7-0 Data [7:0]

This is the data value written by the system CPU during the NMI event

Bit Descriptions (Second Sequential Read)

Bit 7 Write

This bit will be set if the I/O operation attempted was a write operation. This bit will currently always be set as all currently defined NMI conditions are I/O writes.

Bit 6 Decoded A[7:4]

This bit will be set if the second nibble of the I/O address is hex 'D'

Bit 5 Decoded A[7:4]

This bit will be set if the second nibble of the I/O address is hex 'C'

Bit 4 Decoded A[7:4]

This bit will be set if the second nibble of the I/O address is hex 'B'

Bit 3-0 Address [3:0]

This is the lower nibble of the I/O address during the NMI event

Bit Descriptions (Third Sequential Read)

Bit 7 Cache Empty

This bit will be set on the last value read out of the cache

Bit 6 Cache Overrun

This bit will be set if the cache is already full when an NMI event occurs

Bit 5-0 NMI Index

These bits hold a copy of the index register value in effect when an NMI event occurred, (i.e., if the write was to an odd address for which there is an index register at the next lower even address, this field will save the value in that index register). If not, the value save in this field should be ignored.

10.48 Extensions Active Adapter State Register: STATE

I/O Port Address: 3C5

Index: AF

Bit #	Description	Access	Reset By	Reset State
7 (msb)	State Change Occurred	R/W	Reset and read of this register	0
6	Previous Adapter State Bit-2	R/W(Rev A)	Reset	0 -1 (Rev A)
5	Previous Adapter State Bit-1	R/W	Reset	0
4	Previous Adapter State Bit-0	R/W	Reset	0
3	-unused-			
2	Current Adapter State Bit-2	R/W(Rev A)	Reset	0 (D-E), 1 (A)
1	Current Adapter State Bit-1	R/W	Reset	0
0 (lsb)	Current Adapter State Bit-0	R/W	Reset	0

Bit Descriptions

Bit 7 State Change Occurred

If this bit is set, a state change has automatically occurred; also, an NMI condition. The other bits in this register indicate the type of change. Reading this register clears this bit.

Bit 6-4 Previous State

If bit-7 of this register is set, these bits indicate the state of the adapter (according to the state table below) prior to the immediately preceding state change. These bits get copied from bits 2-0 immediately preceding every state change. If bit-7 is 0, the state of these bits is unknown.

Bit 3 Unused

Bit 2-0 Current State

These bits always indicate the current adapter state (mode) according to the table below, independent of whether a state change has occurred.

State	Mode Name	Video Timing Control	Cursor Control	3?5 I/O Write	3?5 I/O Read
x01	CGA	6845	6845	6845	6845
x10	MGA	6845	6845	6845	6845
000	EGA	CRTC (EGA Mode)	CRTC (EGA)	6845 & CRTC	CRTC
100	VGA	CRTC (VGA Mode)	CRTC (VGA)	6845 & CRTC	CRTC
011	EGA Enhanced Text	CRTC (EGA Mode)	6845	6845	6845
111	VGA Enhanced Text	CRTC (VGA Mode)	6845	6845	6845

The registers that control video timing in the 6845 are R0-R9. The registers that control video timing in the CRTC are CR0-CR9 and CR10-CR18. The cursor control registers are RA & RB in the 6845 and CRA & CRB in the CRTC.

In order to perform state save operations from EGA or VGA mode without effecting monitor timing, the current adapter state should be temporarily set to state 'x11' (TXT mode) to read 6845 registers R0-RB in place of CRTC registers CR0-CRB at I/O port 3?5 (index = 00-0B).

Note that in enhanced text mode, the video timing is controlled by the CRTC except that the cursor size is controlled by the 6845 cursor size registers (modified per the Cursor Adjust Register at extensions index 95). Enhanced text mode is for programs that are written to produce CGA text. The 610/620 automatically substitutes high-resolution text by using this mode resulting in much more readable text.

The msb of the status number is the EGA/VGA control bit. If 0, the CRTC is EGA-com-

patible; if 1, the VGA extensions of the CRTC are enabled to control CRTC activity. The VGA extension bits may be read and written in EGA mode, but will have no effect until the VGA control bit in this register is set. In revision D and E chips, the EGA/VGA CRTC control bit is always 0; in rev A chips it is implemented and defaults to 1 on reset. The EGA/VGA control bit is not considered part of the state number for Smartswitch transitions; transitions occur only between the 4 basic states: CGA, MGA, EGA/VGA, and TXT.

10.49 Extensions Scratch Registers 0-F: SCR0-F

I/O Port Address: 3C5

Index: B0-BF

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Scratch Register Bit-7	R/W	-	-
6	Scratch Register Bit-6	R/W	-	-
5	Scratch Register Bit-5	R/W	-	-
4	Scratch Register Bit-4	R/W	-	-
3	Scratch Register Bit-3	R/W	-	-
2	Scratch Register Bit-2	R/W	-	-
1	Scratch Register Bit-1	R/W	-	-
0 (lsb)	Scratch Register Bit-0	R/W	-	-

These sixteen 8-bit read/write registers are provided for software (BIOS, etc.) to store whatever is needed. None of the bits are connected to direct hardware functions. None are reset on power-up or reset.

All of these registers are reserved for use by the 610/620 BIOS and associated Cirrus Logic utility programs. None of these registers are available for use by user programs.

10.50 Extensions CPU Read Access Register: CPURAR

I/O Port Address: 3C5

Index: C0

Bit #	Description	Access	Reset By	Reset State
7 (msb)	CPU Read Access Address Bit 7	R/W	Reset	0
6	CPU Read Access Address Bit 6	R/W	Reset	0
5	CPU Read Access Address Bit 5	R/W	Reset	0
4	CPU Read Access Address Bit 4	R/W	Reset	0
3	CPU Read Access Address Bit 3	R/W	Reset	0
2	CPU Read Access Address Bit 2	R/W	Reset	0
1	CPU Read Access Address Bit 1	R/W	Reset	0
0 (lsb)	CPU Read Access Address Bit 0	R/W	Reset	0

This register contains an 8-bit index to be added to bits 16 through 12 of the CPU address during a video memory read operation. This indexing operation allows accesses to 4K byte segments in the video memory. The 8 bit result is used as the most significant bits of a 20 bit video memory address. Depending on the actual size of the video memory installed, some of these bits may be ignored.

Every read address is indexed. This register must be programmed to all 0's for CPU read addresses to be passed unmodified to the video memory.

10.51 Extensions CPU Write Access Register: CPUWAR

I/O Port Address: 3C5

Index: C1

Bit #	Description	Access	Reset By	Reset State
7 (msb)	CPU Write Access Address Bit 7	R/W	Reset	0
6	CPU Write Access Address Bit 6	R/W	Reset	0
5	CPU Write Access Address Bit 5	R/W	Reset	0
4	CPU Write Access Address Bit 4	R/W	Reset	0
3	CPU Write Access Address Bit 3	R/W	Reset	0
2	CPU Write Access Address Bit 2	R/W	Reset	0
1	CPU Write Access Address Bit 1	R/W	Reset	0
0 (lsb)	CPU Write Access Address Bit 0	R/W	Reset	0

This register contains an 8-bit index to be added to bits 16 through 12 of the CPU address during a video memory write operation. This indexing operation allows accesses to 4K byte segments in the video memory. The 8 bit result is used as the most significant bits of a 20 bit video memory address. Depending on the actual size of the video memory installed, some of these bits may be ignored.

Address indexing is always in effect. This register must be programmed to all 0's to pass the system addresses unmodified to the video memory.

10.52 Extensions LCD Control Register: LCDCNTLII

I/O Port Address: 3C5

Index: C2

Bit #	Description	Access	Reset By	Reset State
7 (msb)	256K Bytes Video Memory Addressing	R/W	Reset	0
6	CPU Address Shift Left, Bit-1	R/W	Reset	0
5	CPU Address Shift Left, Bit-0	R/W	Reset	0
4	400/480* Lines LCD Panel	R/W	Reset	0
3	Display Type Select, Bit-1	R/W	Reset	0
2	Display Type Select, Bit-0	R/W	Reset	0
1	Enable LCD expanded graphics mode	R/W	Reset	0
0 (lsb)	Protect CRTC Vertical Display Parameters	R/W	Reset	0

Bit Descriptions

Bit 7 This bit is set to 1 when there are 256K bytes of video memory per plane. In this video memory addressing scheme, the Screen A Starting Address, Screen B Starting address, and the cursor address can all be programmed as 18-bit values. When this bit is set to 0, the address pin assigned to the 9th RAS address bit and the 9th CAS address bit is held low. To support 256K bytes of video memory, the refresh counter is also extended to 9 bits, and the memory address counter is extended to 18 bits.

Bit 6-5 After indexing, the CPU address is shifted to the left under control of this field. This shift control is always in effect. So it must be set to 0 if no address shifting is desired.

Bit 4 This bit is set to 0 for 480 line LCD panels, and set to 1 for 400 line LCD panels.

Bit 3-2 This field specifies the type of display driven by Stingray:

00 : CRT (power up state)

01: LCD

10, 11: reserved

Bit 1 When this bit is set to 1, a predetermined set of scan lines will be replicated in LCD graphics modes.

Bit 0 When this bit is set to 1, the Max Scan Line field in CR09, the Vertical Displayed parameter in CR12 and CR07 are write protected. This mechanism is used to support expanded LCD text modes using 19 line character fonts.

10.53 Reserved

I/O Port Address: 3C5
Index: C3

10.54 Extensions Switch Setting Register: SWRH

I/O Port Address: 3C5

Index: C4

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Switch Setting Bit 15	R	Reset	Pin CPU-AD15
6	Switch Setting Bit 14	R	Reset	Pin CPU-AD14
5	Switch Setting Bit 13	R	Reset	Pin CPU-AD13
4	Switch Setting Bit 12	R	Reset	Pin CPU-AD12
3	Switch Setting Bit 11	R	Reset	Pin CPU-AD11
2	Switch Setting Bit 10	R	Reset	Pin CPU-AD10
1	Switch Setting Bit 9	R	Reset	Pin CPU-AD9
0 (lsb)	Switch Setting Bit 8	R	Reset	Pin CPU-AD8

This register is initialized at power up to store switch settings. The setting of most of these switches is interpreted by the BIOS which then configures Stingray accordingly. There is only 1 switch bit, bit 15, which controls the Stingray hardware directly.

Bit Descriptions

Bit 15 When this switch is set, Stingray will not respond to any BIOS read operation on power up. When BIOS operations are disabled by this switch setting, it CANNOT be reactivated by any other programmable control mechanism.

10.55 Extensions Switch Setting Register: SWRL

I/O Port Address: 3C5

Index: C5

Bit #	Description	Access	Reset By	Reset State
7 (msb)	Switch Setting Bit 7	R	Reset	Pin CPU-AD7
6	Switch Setting Bit 6	R	Reset	Pin CPU-AD6
5	Switch Setting Bit 5	R	Reset	Pin CPU-AD5
4	Switch Setting Bit 4	R	Reset	Pin CPU-AD4
3	Switch Setting Bit 3	R	Reset	Pin CPU-AD3
2	Switch Setting Bit 2	R	Reset	Pin CPU-AD2
1	Switch Setting Bit 1	R	Reset	Pin CPU-AD1
0 (lsb)	Switch Setting Bit 0	R	Reset	Pin CPU-AD0

This register is initialized at power up to store switch settings. The setting of most of these switches is interpreted by the BIOS which then configures Stingray accordingly. There is only 1 switch bit, bit 15, which controls the Stingray hardware directly.

10.56 Extensions Screen B Start Address Highest Register: SBSAM

I/O Port Address: 3C5

Index: C6

Bit #	Description	Access	Reset By	Reset State
7 -2	-unused-			
1	Screen B Start Address Bit-17	R/W	Reset	0
0	Screen B Start Address Bit-16	R/W	Reset	0

Bit Descriptions

Bit 7-2 Unused

Bit 1-0 This 2 bit field constitutes the two most significant bits in an 18-bit Screen B starting address for use with a 256K bytes video memory.

10.57 Extensions LCD Control Register: LCDCNTLIII

I/O Port Address: 3C5

Index: C7

Bit #	Description	Access	Reset By	Reset State
7 -5	unused			
4	Div Mclk by 2	R/W	-	-
3	Force 16 bit	R/W	-	-
2	Shadow Vertical Total	R/W	Reset	0
1	All A and B Addresses for 16 bits	R/W	Reset	0
0 (lsb)	Enable 16 bits interface	R/W	Reset	0

Bit Descriptions

Bit 7-5 Unused

Bit 4 Setting this bit divides Mclk by 2.

Bit 3 When this bit is set to 1, it forces 16 bit write/read of video memory, independent of any mode.

Bit 2 When this bit is set to 1, the CRTC vertical total parameter stored in CR06 and CR07 is protected from modification, for use in LCD frame rate control. A shadow register is activated so that new vertical total parameters can be written and read back, but these new parameter values will have no effect in LCD screen control. When this bit is 0, values written into CR06, and bits 8 and 9 for the CRTC vertical total parameter in CR07 will control the display frame rate.

Bit 1 When this bit is set to 1, the entire video memory address range from A:0000 to B:FFFF is accepted as the valid address range in accepting 16 bit memory operations. When this bit is 0, only addresses in the valid address subrange in effect will be accepted for 16 bit memory operations.

Bit 0 When this bit is set to 0, all system bus operations to the video memory are handled as 8 bit operations. When this bit is set to 1, all system bus operations to the video memory are handled as 16 bit operations in all planar modes.

10.58 Reserved

I/O Port Address: 3C5
Index: C8-CF

10.59 Column Offset: COLOFF

I/O Port Address: 3C5
Index: D0 (and D4[4])

Bit #	Description	Access	Reset By	Reset State
7 (msb)		R/W	-	-
6		R/W	-	-
5		R/W	-	-
4		R/W	-	-
3		R/W	-	-
2		R/W	-	-
1		R/W	-	-
0 (lsb)		R/W	-	-

Bit Descriptions

The main purpose for this register is to provide the panning function (left 640 or right 640 pixels) for MGA reduction mode. A value of zero (0) (and a "0" for bit-8 at ext reg index location D4[6]) will cause the data being sent to the display to start with the first (left-most) pixel of the display to start at the first displayable location (0). This value is used for MGA reduction to display the left-most 640/720 pixels. In non-MGA modes this value should be set to 0 for normal operation. Setting a non-zero value will cause the display to start at the programmed location, thus, for displaying the right-most 640/720 pixels in MGA mode, a value of 80 decimal (50Hex) should be programmed.

10.60 Panel Horizontal Displayed: PHDIS

I/O Port Address: 3C5

Index: D1 (and D4[5])

Bit #	Description	Access	Reset By	Reset State
7 (msb)		R/W	-	-
6		R/W	-	-
5		R/W	-	-
4		R/W	-	-
3		R/W	-	-
2		R/W	-	-
1		R/W	-	-
0 (lsb)		R/W	-	-

Bit Descriptions

This 9-bit register (see D4[5] for the 8th-msb) determines how many nibbles (4-bit groups) wide the panel is. For 640 column panels this register should be programmed to 640/4 -1 = 159 decimal (9FH). Panels up to 2048 bits wide can be accommodated.

10.61 Row Offset: ROWOFF

I/O Port Address: 3C5

Index: D2 (and D4[6])

Bit #	Description	Access	Reset By	Reset State
7 (msb)		R/W	-	-
6		R/W	-	-
5		R/W	-	-
4		R/W	-	-
3		R/W	-	-
2		R/W	-	-
1		R/W	-	-
0 (lsb)		R/W	-	-

Bit Descriptions

If the Auto-Center-Enable bit is "off" (disable auto-center), the value in this register determines where the displayable image will appear on the panel.

If Automatic centering is required, the value stored in this register is given by the following equation and example:

Auto-Center = enabled:

ROWOFF = LCDVTOTAL(C6) - PANEL VERTICAL SIZE

= 506 - 480 = 26

If manual centering is required, the value stored in this register is given by the following equation and example:

Auto-Center = disabled:

ROWOFF = LCDVTOTAL(C6) - PANEL ROW SEGMENT TOTAL

= 506 - 239 = 267

All of the non-displayed lines (i.e., 80 blank lines in a 640x400 mode on a 640 x 480 panel) will appear at the bottom of the screen.

10.62 Panel Row Segment Total: PRST

I/O Port Address: 3C5

Index: D3 (and D4[7])

Bit #	Description	Access	Reset By	Reset State
7 (msb)		R/W	-	-
6		R/W	-	-
5		R/W	-	-
4		R/W	-	-
3		R/W	-	-
2		R/W	-	-
1		R/W	-	-
0 (lsb)		R/W	-	-

Bit Descriptions

For dual-drive double panel LCDs, the value programmed into this register is half the panel vertical size (i.e., 239 for a 480 line panel). The maximum panel size which can be accommodated is then 2 times the value loaded in this register (and bit 8 located in D4[7]) or 512 x 2 = 1024.

10.63 Panel Control 1: PNLCTLI

I/O Port Address: 3C5

Index: D4

Bit #	Description	Access	Reset By	Reset State
7	Bit-8(msb) Panel Row Seg Total	R/W	-	-
6	Bit-8(msb) Row Offset	R/W	-	-
5	Bit-8(msb) Panel Horz. Displayed	R/W	-	-
4	Bit-8(msb) Column Offset	R/W	-	-
3	Auto Center Enable	R/W	-	-
2	Extra-llclk-en	R/W	-	-
1	Fr-A8-en	R/W	-	-
0 (lsb)	rtrc-llclk-en	R/W	-	-

Bit Descriptions

Bit 7-4 These are the over-flow (8th) bits from previously defined registers.

Bit 3 When in compatible modes of operation (non-expanded graphics or text modes) which do not completely fill the panel (i.e., a 400-line text mode on a 480 line panel), the non-displayed lines will be equally divided on the top of the screen and the bottom of the screen.

See also Panel Row Segment Total register description.

Bit 2 When this bit is set, it generates an extra Llclk pulse for lower panel. This is useful for panels requiring an extra Llclk pulse for lower panel.

Bit 1 When this bit is set to 1, the 8th address bit for frame buffer is put out on NMI* pin.

(Note: NMI* is an open collector pin.)

Bit 0 When this bit is set to 1, llclk (line CLK) is generated during vertical retrace time.

10.64 Panel Control 2: PNLCTLII

I/O Port Address: 3C5

Index: D5

Bit #	Description	Access	Reset By	Reset State
7 (msb)	LCD RAMDAC Enable	R/W	Reset	0
6	Reverse Video bit	R/W	Reset	0
5	Attribute Emulation	R/W	Reset	0
4	Force 16 bit	R/W	Reset	0
3	~~unused~~ Reverse grayscale	R/W	Reset	0
2	Color Palette protect	R/W	Reset	0
1	MGA Reduction (msb)	R/W	Reset	0
0 (lsb)	MGA Reduction (lsb)	R/W	Reset	0

Bit Descriptions

Bit 7 Setting this bit with LCD panels enables the internal gray-scale generation circuit to receive its input data from the 256x4 internal palette which keeps track of the CRT RAMDAC contents, applies the sum-to-gray conversion and stores the result in 256-4-bit locations. Setting this bit in non-LCD modes can also be useful if sum-to-gray is desired (i.e., Plasma Panels which can accept 4-bits/pixel and produce gray-scales). Clearing this bit bypasses the LCD palette.

Bit 6 Setting this bit reverses the screen image when in LCD and Text mode.

Bit 5 Setting this bit maps colors in text-modes to shades of gray which produce the highest contrast image.

Clearing this bit allows colors to be freely mapped to shades of gray under control of the attribute palette and LCD Palette RAM.

Bit 4 Setting this bit forces 16 bit memory operation. Note: This does not depend on any modes. The user should know what he/she is doing.

Bit 3 ~~unused~~ Setting this bit will cause panels ~~to~~ ~~work~~ that reverse the video pixel data. ~~work~~ This bit will be present in Rev BC and later.

Bit 2 Setting this bit protects the attribute palette.

Bit 1-0 Displays 720 pixel Hercules Graphics images on a 640 pixel display as follows:

1	0	Description
0	X	Display left 640 or right 640 pixels of 720 depending on the value stored in the Column Offset Register.
1	0	Skip every 9th pixel
1	1	"or" every 8th and 9th pixel

10.65 Gray Scale Offset: GROFF

I/O Port Address: 3C5

Index: D6

Bit #	Description	Access	Reset By	Reset State
7	Vert Stipple enable	R/W	Reset	0
6	Reserved	-	-	-
5	Reserved	-	-	-
4	Reserved	-	-	-
3 (msb)	Groff3	R/W	Reset	1
2	Groff2	R/W	Reset	1
1	Groff1	R/W	Reset	0
0 (lsb)	Groff0	R/W	Reset	1

Bit Description

Bit 7 When this bit is set, stippling occurs vertically.

Bit 6-4 Reserved

Bit 3-0 The 4-bit value stored in this register is used to offset the starting gray-scale wave position of the current line with respect to the previous displayed line. This value is not used on the first displayed line. The current Gray-scale algorithm uses value 13 which is the reset state of this register.

10.66 Reserved

I/O Port Address: 3C5
Index: D7-D8

10.67 Modulation (AC Inversion): MOD

I/O Port Address: 3C5

Index: D9

Bit #	Description	Access	Reset By	Reset State
7 (msb)		R/W	Reset	0
6		R/W	Reset	0
5		R/W	Reset	0
4		R/W	Reset	0
3		R/W	Reset	0
2		R/W	Reset	0
1		R/W	Reset	0
0 (lsb)		R/W	Reset	0

Bit Descriptions

LCD panels must have a modulation signal (sometimes referred to as AC inversion) to:

- invert the LCD drive voltages in order to prevent any net DC voltage from appearing on the LCD fluid which can cause chemical breakdown of the LCD material and destroy the panel.
- Reduce LCD crosstalk

Some panels have this function built into the panel. The contents of this register determines the width of 1/2 of the square-wave output of an 8-bit counter which is clocked by LCD Line clock. Normally, some number which does not divide evenly into the panel size is used (i.e., 13 or 17).

0C PHEONIX
20 CIRRUS

10.68 Frame Color: FRCLR

I/O Port Address: 3C5

Index: DA

Bit #	Description	Access	Reset By	Reset State
7	Reserved	R/W	-	-
6	Reserved	R/W	-	-
5	Reserved	R/W	-	-
4	Reserved	R/W	-	-
3 (msb)	FRCLR3	R/W	-	-
2	FRCLR2	R/W	-	-
1	FRCLR1	R/W	-	-
0 (lsb)	FRCLR0	R/W	-	-

Bit Descriptions

Bit 3-0 These bits control the gray-shade of the non-displayed portion of the screen. Up to 16-shades can be selected to provide as close a match as possible between the LCD non-display area and the color of the Display's cosmetic Bezel. (0=darkest shade, F=brightest shade regardless of the state of the Reverse Video bit.)

10.69 Panel Control 3: PNLCTLIII:

I/O Port Address: 3C5

Index: DB

Bit #	Description	Access	Reset By	Reset State
7 (msb)	CGA palette select	R/W	Reset	0
6	MCLK invert	R/W	Reset	0
5	Video Tristate	R/W	Reset	0
4	Reserved	-	-	-
3	Reserved	-	-	-
2	Reserved	-	-	-
1	Reserved	-	-	-
0 (lsb)	Reserved	-	-	-

Bit Descriptions

Bit 7 Setting this bit to a "1" forces CGA color mapping and bypasses internal palette in "LCD" modes. Setting this bit to "0" forces the video through internal palette in LCD modes and uses the CGA hardware as in EAGLE G/A.

Bit 6 Setting this bit inverts the MCLK used in G/A. This bit is provided in case we have ITS and MCLK skews.

Bit 5 Setting this bit to "1" tristates video (P0, P1, P2, P3, P4, P5, P6/FEAT0, P7/FEAT1) & VDCLK pins.

10.70 Reserved

I/O Port Address: 3C5
Index: DC-DF

10.71 CRTC Screen A Start Address Register Highest: CR26

I/O Port Address: 3?5

Index: 26

Bit #	Description	Access	Reset By	Reset State
7 -2	-unused-			
1	Screen A Start Address Bit-17	R/W	Reset	0
0	Screen A Start Address Bit-16	R/W	Reset	0

Bit Descriptions

Bit 7-2 Unused

Bit 1-0 This 2 bit field constitutes the two most significant bits in an 18-bit Screen A starting address for use with a 256K bytes video memory.

10.72 CRTC Cursor Location Register Highest: CR27

I/O Port Address: 3?5

Index: 27

Bit #	Description	Access	Reset By	Reset State
7 -2	-unused-			
1	Cursor Location Bit-17	R/W	Reset	0
0	Cursor Location Bit-16	R/W	Reset	0

Bit Descriptions

Bit 7-2 Unused

Bit 1-0 This 2 bit field constitutes the two most significant bits in an 18-bit cursor location address for use with a 256K bytes video memory.

10.65 Gray Scale Offset: GROFF

I/O Port Address: 3C5

Index: D6

Bit #	Description	Access	Reset By	Reset State
7	Vert Stipple enable	R/W	Reset	0
6	Reserved	-	-	-
5	Reserved	-	-	-
4	Reserved	-	-	-
3 (msb)	Groff3	R/W	Reset	1
2	Groff2	R/W	Reset	1
1	Groff1	R/W	Reset	0
0 (lsb)	Groff0	R/W	Reset	1

Bit Description

Bit 7 When this bit is set, stippling occurs vertically.

Bit 6-4 Reserved

Bit 3-0 The 4-bit value stored in this register is used to offset the starting gray-scale wave position of the current line with respect to the previous displayed line. This value is not used on the first displayed line. The current Gray-scale algorithm uses value 13 which is the reset state of this register.

10.66 Reserved

I/O Port Address: 3C5
Index: D7-D8

10.67 Modulation (AC Inversion): MOD

I/O Port Address: 3C5
Index: D9

Bit #	Description	Access	Reset By	Reset State
7 (msb)		R/W	Reset	0
6		R/W	Reset	0
5		R/W	Reset	0
4		R/W	Reset	0
3		R/W	Reset	0
2		R/W	Reset	0
1		R/W	Reset	0
0 (lsb)		R/W	Reset	0

Bit Descriptions

LCD panels must have a modulation signal (sometimes referred to as AC inversion) to:

- invert the LCD drive voltages in order to prevent any net DC voltage from appearing on the LCD fluid which can cause chemical breakdown of the LCD material and destroy the panel.
- Reduce LCD crosstalk

Some panels have this function built into the panel. The contents of this register determines the width of 1/2 of the square-wave output of an 8-bit counter which is clocked by LCD Line clock. Normally, some number which does not divide evenly into the panel size is used (i.e., 13 or 17).

10.68 Frame Color: FRCLR

I/O Port Address: 3C5

Index: DA

Bit #	Description	Access	Reset By	Reset State
7	Reserved	R/W	-	-
6	Reserved	R/W	-	-
5	Reserved	R/W	-	-
4	Reserved	R/W	-	-
3 (msb)	FRCLR3	R/W	-	-
2	FRCLR2	R/W	-	-
1	FRCLR1	R/W	-	-
0 (lsb)	FRCLR0	R/W	-	-

Bit Descriptions

Bit 3-0 These bits control the gray-shade of the non-displayed portion of the screen. Up to 16-shades can be selected to provide as close a match as possible between the LCD non-display area and the color of the Display's cosmetic Bezel. (0=darkest shade, F=brightest shade regardless of the state of the Reverse Video bit.)

10.69 Panel Control 3: PNLCTLIII:

I/O Port Address: 3C5

Index: DB

Bit #	Description	Access	Reset By	Reset State
7 (msb)	CGA palette select	R/W	Reset	0
6	MCLK invert	R/W	Reset	0
5	Video Tristate	R/W	Reset	0
4	Reserved	-	-	-
3	Reserved	-	-	-
2	Reserved	-	-	-
1	Reserved	-	-	-
0 (lsb)	Reserved	-	-	-

Bit Descriptions

Bit 7 Setting this bit to a "1" forces CGA color mapping and bypasses internal palette in "LCD" modes. Setting this bit to "0" forces the video through internal palette in LCD modes and uses the CGA hardware as in EAGLE G/A.

Bit 6 Setting this bit inverts the MCLK used in G/A. This bit is provided in case we have ITS and MCLK skews.

Bit 5 Setting this bit to "1" tristates video (P0, P1, P2, P3, P4, P5, P6/FEAT0, P7/FEAT1) & VDCLK pins.

10.70 Reserved

I/O Port Address: 3C5

Index: DC-DF

10.71 CRTC Screen A Start Address Register Highest: CR26

I/O Port Address: 3?5

Index: 26

Bit #	Description	Access	Reset By	Reset State
7 -2	-unused-			
1	Screen A Start Address Bit-17	R/W	Reset	0
0	Screen A Start Address Bit-16	R/W	Reset	0

Bit Descriptions

Bit 7-2 Unused

Bit 1-0 This 2 bit field constitutes the two most significant bits in an 18-bit Screen A starting address for use with a 256K bytes video memory.

10.72 CRTC Cursor Location Register Highest: CR27

I/O Port Address: 3?5

Index: 27

Bit #	Description	Access	Reset By	Reset State
7 -2	-unused-			
1	Cursor Location Bit-17	R/W	Reset	0
0	Cursor Location Bit-16	R/W	Reset	0

Bit Descriptions

Bit 7-2 Unused

Bit 1-0 This 2 bit field constitutes the two most significant bits in an 18-bit cursor location address for use with a 256K bytes video memory.

External Functional Specification
PHOENIX VGA BIOS IMPLEMENTATION

FOR Cirrus Logic CL-GD610/620

Version 1.0
September 19, 1989

Copyright

Disclaimers

Phoenix Technologies Ltd. makes no representations or warranties with respect to the design and documentation herein described and especially disclaims any implied warranties of merchantability or fitness for any particular purpose. Further, Phoenix Technologies Ltd. reserves the right to revise this design and associated documentation and to make changes from time to time in the content without obligation of Phoenix Technologies Ltd. to notify any person of such revisions or changes.

Print Date: September 19, 1989

Preface

The Phoenix Extensible Video BIOS functions and external interface for VGA are described in this document. This BIOS is 100% IBM compatibile, easily extensible and faster and more reliable than the previous implementation. This implementation:

- Is designed with future enhancements in mind.
- Is not intricately tied to a specific environment or input/output situation.
- Allows enhancements without danger of affecting compatability.
- Allows modification for chipset changes/enhancements without affecting general utility.

The purpose of this document is to describe the functions and external interface provided by the Phoenix implementation of the VGA BIOS for the Cirrus Logic CL-GD610/620 chip set. Following is a brief outline of the material covered in this document.

- **Chapter 1 Overview** - A high level overview of the design and functions of the VGA BIOS.
- **Chapter 2 Compatibility** - An overview of the Interrupt 10H and hardware registers compatibility.
- **Chapter 3 Cirrus Logic CL-GD610/620 Implementation** - A description of the Cirrus Logic CL-GD610/620 VGA BIOS implementation extensions and features.
- **Appendix A VGA Analysis and Verification** - A discussion of the general approach for Engineering Verification, and a brief description of GSCRIPT script files to be used in testing.

Related Documentation

- Cirrus Logic Video Subsystem External Software Specification, Cirrus Logic, Inc., 1989
- Preliminary Data Sheet, CL-GD 610/620, Cirrus Logic, Inc., April 1989
- GD610/620 Hardware Technical Reference Manual, Cirrus Logic, Inc., July 1989
- IBM Personal System/2 Technical Reference for Model 50/60 or Model 80.
- Programmer's Guide to the EGA and VGA Cards, Richard F. Ferraro, Addison-Wesley Publishing Company, 1988
- Programmer's Guide to PC & PS/2 Video Systems, Richard Wilton, Microsoft Press, 1987
- Guide to Features, Advanced Video BIOS, VGA Compatible, Phoenix Technologies, 1988
- FOCUS User's Guide, Phoenix Technologies, 1989

(This page intentionally left almost blank)

TABLE OF CONTENTS

Chapter 1 Overview

Chapter 2 Compatibility

Chapter 3 Cirrus Logic CL-GD610/620 Implementation

LIST OF FIGURES

(This page intentionally left almost blank)

CHAPTER 1
OVERVIEW

1.1 Compatibility

The Phoenix Extensible VGA BIOS is 100% IBM compatible at the hardware register and interrupt 10H levels.

1.2 Design Overview

1.2.1 Table Driven Code Structure

The Phoenix Extensible VGA BIOS (PEVB) is implemented using a table driven software structure. This approach provides for a clean design as well as straight forward modification for enhancements.

1.2.1.1 Easily Extensible

The Extensible VGA is designed to facilitate modification to meet new VGA chipset demands. By removing mode parameters such as number of rows, columns, scan lines, and page length from inline sections of code and placing them in globally known tables, the profile of any particular mode of operation can be clearly seen. VGA extensions are added by filling in these well defined structures and providing access to the extensions through call tables. This design allows customized options to be implemented with a much shorter development time, especially where extensions are defined across a wide range of monitors and emulation states.

1.2.1.2 Emulation of Other Video Subsystems

For chipsets that provide backwards emulation (i.e. EGA, CGA, MGA) the design incorporates two special structures: one that branches the emulation state, and one that branches the monitor type. Both structures help clarify the parametric differences between a VGA state driving an ECD display and a VGA state driving an PS/2 display. These structures give the software a standard access mechanism to state display specific HW register values and emulation compatible function blocking. The state structures provide function blocking of nonemulation state compatible function calls. This type of organization significantly reduces the amount of engineering effort necessary to support new modes.

1.2.1.3 Designed in Performance

In order to provide table driven code that is performance oriented, time critical mode parameters are contained in primary structures indexed by mode number and Segment 040h VGA input parameters. These primary structures provide fast address translation of cursor offsets to Regen buffer cells, general alpha/grafix information, column count, page size, flags, and other frequently used mode specific data. Infrequently used data (such as GRAFIX CTRL values) are branched from the primary structures through a series of linked lists.

(This page intentionally left almost blank)

CHAPTER 2
COMPATIBILITY

2.1 Interrupt 10H Interface

The Phoenix Extensible VGA BIOS is fully compatible with the Interrupt 10H external interface as defined by IBM® for the VGA. Figure 2-1 lists the Int 10H functions and subfunctions. On call, the function is specified in AH.

2.1.1 Video Modes

One of the functions provided by the Video BIOS external interface is video mode selection. Not all video modes are available to all video subsystems. Since the VGA implementation of the video BIOS includes emulation of subsystems other than VGA, Figure 2-3 is provided to show the different video modes supported by various video subsystems.

2.2 Hardware Registers

In addition to Interrupt 10H compatibility, the Phoenix Extensible VGA BIOS is completely register level compatible with the IBM VGA BIOS. Figure 2-2 provides an overview of the VGA hardware registers.

2.3 Emulation of Other Adapter Types

Compatibility with other adapter types is also provided. Certain hardware vendors provide true hardware compatibility of other adapter types as part of the adapter. In these cases, the Phoenix Extensible VGA exploits this feature. When compatibility is not provided in the hardware, emulation of other adapter types may be accomplished through software.

AH Value (hex)	Function Description
00	Set Video Mode
01	Set Cursor Size
02	Set Cursor Position
03	Get Cursor Position
04	Read Light Pen Position (not supported in BIOS for VGA implementations)
05	Select New Video Page
06	Scroll Active Page Up
07	Scroll Active Page Down
08	Read Character and Attribute at Cursor
09	Write Character and Attribute at Cursor
0A	Write Character at Cursor
0B	Set CGA Color Palette BH = 00 sets border or background color = 01 selects 4 color palette for mode 4 or 5 (320x200)
0C	Write Pixel to Screen
0D	Read Pixel
0E	Write Character in TTY Mode
0F	Get Current Video State
10	Set Palette Registers AL = 00 set specified palette register = 01 specify overscan (border) color = 02 set all palette registers and overscan = 03 set background intensity or blink bit = 07 read specified palette register = 08 read overscan register = 09 read all palette registers and overscan = 10 set specified DAC color register = 12 set block of DAC color registers = 13 set Attribute Controller Color Select State = 15 read specified DAC color register = 17 read block of DAC color registers = 18 set DAC Mask register = 19 read DAC Mask register = 1A read Attribute Controller Color Select Register = 1B grey scaling on block of DAC Color Registers

Figure 2-1 . Compatible Interrupt 10H Functions (1 of 2)

AH Value (hex)	Function Description
11	Character Generator AL = 00 load user text font = 01 load ROM monochrome 8x14 text font = 02 load ROM 8x8 text font = 03 select displayed character definition tables = 04 load ROM 8x16 text font = 10 load user text font and program CRTC = 11 load ROM monochrome 8x14 text font and program CRTC = 12 load ROM 8x8 text font and program CRTC = 14 load ROM 8x16 text font and program CRTC = 20 load pointer to 8x8 user graphics font = 21 load user graphics font = 22 load ROM 8x14 graphics font = 23 load ROM 8x8 graphics font = 24 load ROM 8x16 graphics font = 30 get current character generater information
12	Alternate Select BL = 10 return EGA video configuration information = 20 select alternate print screen routine = 30 select scan lines for text modes = 31 select default palette loading during set mode = 32 CPU video buffer access = 33 grey scale summing = 34 cursor emulation = 35 PS/2 video display switch = 36 video refresh on/off
13	Display String AL = 00 BL contains attribute for string, cursor position unchanged = 01 BL contains attribute for string, cursor position updated = 02 String contains attribute bytes, cursor position unchanged (text modes only) = 03 String contains attribute bytes, cursor position updated (text modes only)
1A	Get/Set Video Display Combination Codes AL = 00 get display combination code = 01 set display combination code
1B	Get Functionality/State Information
1C	Save/Restore Video State AL = 00 return buffer size for requested state(s). = 01 save requested state(s) to buffer = 02 restore requested state(s) from buffer

Figure 2-1 . Compatible Interrupt 10H Functions (2 of 2)

Register Group	Register Name	Read Port	Write Port	Index
General Registers (GENR)	Miscellaneous Output	03CCh	03C2h	-
	Input Status 0	03C2h	-	-
	Input Status 1	03?Ah	-	-
	Feature Control	03CAh	03?Ah	-
	VGA Enable	03C3h	03C3h	-
	DAC State	03C7h	-	-
CRT Controller Registers (CRTC)	CRT Controller Address	03?4h	03?4h	-
	Horizontal Total	03?5h	03?5h	00
	Horizontal Display Enable End	03?5h	03?5h	01
	Start Horizontal Blanking	03?5h	03?5h	02
	End Horizontal Blanking	03?5h	03?5h	03
	Start Horizontal Retrace Pulse	03?5h	03?5h	04
	End Horizontal Retrace	03?5h	03?5h	05
	Vertical Total	03?5h	03?5h	06
	CRT Controller Overflow	03?5h	03?5h	07
	Preset Row Scan	03?5h	03?5h	08
	Maximum Scan Line	03?5h	03?5h	09
	Cursor Start	03?5h	03?5h	0A
	Cursor End	03?5h	03?5h	0B
	Start Address High	03?5h	03?5h	0C
	Start Address Low	03?5h	03?5h	0D
	Cursor Location High	03?5h	03?5h	0E
	Cursor Location Low	03?5h	03?5h	0F
	Vertical Retrace Start	03?5h	03?5h	10
	Vertical Retrace End	03?5h	03?5h	11
	Vertical Display Enable End	03?5h	03?5h	12
	Offset	03?5h	03?5h	13
	Underline Location	03?5h	03?5h	14
	Start Vertical Blank	03?5h	03?5h	15
	End Vertical Blank	03?5h	03?5h	16
	CRTC Mode Control	03?5h	03?5h	17
	Line Compare	03?5h	03?5h	18
	Read CRT Latches	03?5h	03?5h	22
	Attrib Toggle State	03?5h	03?5h	24

? = B in Monochrome Emulation Modes ? = D in Color Emulation Modes

NOTE: ? in address depends on Bit 0 of Miscellaneous Output register

Figure 2-2 . VGA Register Overview (1 of 2)

Register Group	Register Name	Read Port	Write Port	Index
Graphics Controller Registers (GRFX)	Graphics Address	03CEh	03CEh	-
	Set/Reset	03CFh	03CFh	00
	Enable Set/Reset	03CFh	03CFh	01
	Color Compare	03CFh	03CFh	02
	Data Rotate	03CFh	03CFh	03
	Read Map Select	03CFh	03CFh	04
	Graphics Mode Register	03CFh	03CFh	05
	Miscellaneous	03CFh	03CFh	06
	Color Don't Care	03CFh	03CFh	07
	Bit Mask	03CFh	03CFh	08
Sequencer Registers (SEQ)	Sequencer Address	03C4h	03C4h	-
	Reset	03C5h	03C5h	00
	Clocking Mode	03C5h	03C5h	01
	Map Mask	03C5h	03C5h	02
	Character Map Select	03C5h	03C5h	03
	Memory Mode	03C5h	03C5h	04
Attribute Controller Registers (ATTRIB)	Attribute Address	03C0h	03C0h	-
	Palette Registers	03C1h	03C0h	00-0F
	Attribute Mode Control	03C1h	03C0h	10
	Overscan Color	03C1h	03C0h	11
	Color Plane Enable	03C1h	03C0h	12
	Horizontal PEL Panning	03C1h	03C0h	13
	Color Select	03C1h	03C0h	14
Digital to Analog Converter (DAC)	PEL Address (Write Mode)	03C8h	03C8h	-
	PEL Address (Read Mode)	-	03C7h	-
	DAC State	03C7h	-	-
	PEL Data	03C9h	03C9h	-
	PEL Mask	03C6h	03C6h	-

Figure 2-2 . VGA Register Overview (2 of 2)

MODE (hex)	RESOLUTION	COLORS	TYPE	SEGMENT	MDA	CGA	EGA	VGA	COMMENTS
00	40x25 chars (320x200 pixels)	16	A	B800		X	X	X	Modes 0 & 1 are the same.
00*	40x25 chars (320x350 pixels)	16	A	B800			X	X	VGA vertical pixel resolution
00+	40x25 chars (360x400 pixels)	16	A	B800				X	selected using INT 10H func 12H.
01	40x25 chars (320x200 pixels)	16	A	B800		X	X	X	VGA vertical pixel resolution
01*	40x25 chars (320x350 pixels)	16	A	B800			X	X	selected using INT 10H func 12H.
01+	40x25 chars (360x400 pixels)	16	A	B800				X	
02	80x25 chars (640x200 pixels)	16	A	B800		X	X	X	Modes 2 & 3 are the same.
02*	80x25 chars (640x350 pixels)	16	A	B800			X	X	VGA vertical pixel resolution
02+	80x25 chars (720x400 pixels)	16	A	B800				X	selected using INT 10H func 12H.
03	80x25 chars (640x200 pixels)	16	A	B800		X	X	X	VGA vertical pixel resolution
03*	80x25 chars (640x350 pixels)	16	A	B800			X	X	selected using INT 10H func 12H.
03+	80x25 chars (720x400 pixels)	16	A	B800				X	
04	320x200 pixels	4	G	B800		X	X	X	Modes 4 & 5 are the same for VGA and EGA.
05	320x200 pixels	4	G	B800		X	X	X	CGA 4 color palette contains black, cyan, red and white.
06	640x200 pixels	2	G	B800		X	X	X	
07	80x25 chars (720x350 pixels)	2	A	B000	X		X	X	VGA vertical pixel resolution
07+	80x25 chars (720x400 pixels)	2	A	B000				X	selected using INT 10H func 12H.
0D	320x200 pixels	16	G	A000			X	X	
0E	640x200 pixels	16	G	A000			X	X	
0F*	640x350 pixels	2	G	A000			X	X	
10*	640x350 pixels	16	G	A000			X	X	
11	640x480 pixels	2	G	A000				X	
12	640x480 pixels	16	G	A000				X	
13	320x200 pixels	256	G	A000				X	

A = Alphanumeric G = Graphics

* modes are the EGA default
+ modes are the VGA default

NOTE: Modes 08-0A are reserved for PCjr only, Modes 0B and 0C are used by EGA video BIOS.

Figure 2-3 . Standard BIOS Video Modes

CHAPTER 3
CIRRUS LOGIC CL-GD610/620 IMPLEMENTATION

This implementation of the VGA BIOS is written for the Cirrus Logic CL-GD610/620 chip set. The features provided by this chip set are as follow:

- Fully VGA Compatible at the hardware level, including register and data path.
- Full backwards compatibility with EGA, CGA, MDA and MGA (Hercules) at the hardware level, including register and data path.
- No extended feature control registers or bits are placed in the I/O address spaces used by any IBM graphics controller or the Hercules controller.
- Hardware support for I/O address 3C3 (motherboard) sleep mechanism
- Flat Panel Mode
  - 16 shades of grey for color emulation (32 shades of grey by stippling)
  - Automatic foreground/background color attribute remapping
  - AutoMap® automatically maps 256 colors into 16 shades of grey
  - Expanded text mode provides more readable characters using 8x19 character fonts
    NOTE: The 8x19 font is used with extended modes (0^, 1^, 2^, 3^ and 7^ 640x475). Refer to Figure 3-2 for a description.
  - Expanded graphics modes allow 200, 348 and 350 scanline resolutions (CGA, MGA and EGA) to fill either 400 or 480 line panels (software selectable) via hardware scanline replication (ratiometrically determined).
  - Hercules 720 pixel Graphics support on a 640 pixel display via user choice of screen pan or data compression.
  - Automatic centering of screen when expanded mode is not selected (Compatibility Mode)
  - Refresh rate up to 110Hz to provide greater contrast and reduce flicker
  - Software selectable Positive Raster (reverse video)
  - Support for 400 or 480 scan line panels
  - Support for dual line flat panels
- Supports CD, MD, ECD, PS/2, Variable Frequency Monitors
  IMPLEMENTATION NOTE: Digital monitor support is not implemented for the general release of the Phoenix Video BIOS for the Cirrus Logic CL-GD610/620 chip set; however, the mechanism is present to allow full support to be added later.
- Extended features of Cirrus Logic CL-GD610/620
  - Graphics cursor
  - Insertion caret
  - Hardware switching between graphics controller types
  - Flexible register write protect control

3.1 Configuration

The initial configuration data must be available to the VGA BIOS. Two Cirrus Logic Extension registers, Switch Register - High and Switch Register - Low, Index 0C4H and 0C5H respectively, contain hardwired configuration data. In the case of an adapter card VGA BIOS, portions of this data are defined with hardware DIP switches (Refer to 3.1.2 Adapter: DIP Switches). In the case of a planar VGA BIOS, the registers contain predetermined default data unless there are hardware DIP switches present. These registers contain the following:

bits 0-2 Monitor Sense Lines

bits 3-4 Monitor Type
- 0 = Monochrome Display
- 1 = Color Display
- 2 = Enhanced Color Display
- 3 = Color or Monochrome PS/2 (or compatible) Display

bits 5-7 Panel Type
(dual panel/dual screen - 2 drivers)
- 0 = Balance line clock and dot clock/2 (Sharp LCD Display)
  - 241 scan lines upper panel
  - 241 scan lines lower panel
- 1 = Free running line clock and dot clock/2
  - 241 scan lines upper panel
  - 248 scan lines lower panel
- 2 = Constrained line clock and dot clock/2
  - 240 scan lines upper panel
  - 241 scan lines lower panel

bits 8-10 State Control
- 0 = Reserved
- 1 = CGA Locked State
- 2 = MGA Locked State
- 3 = EGA Locked State
- 4 = VGA Locked State
- 5 = VGA Protected State

bits 11-13 Reserved = 0

bit 14 Clock Mux, Internal/External
- 0 = External
- 1 = Internal

bit 15 BIOS Location
- 0 = C000H (Video Controller side)
- 1 = E000H (CPU side)

3.1.1 Planar: CMOS Soft Switches

In addition to the default configuration data available in the Cirrus Logic Extension registers, the planar implementation of the VGA BIOS reads the switch information by making an Interrupt 15 call to the system BIOS.

IMPLEMENTATION NOTE: The Interrupt 15 interface is not implemented for the general release of the Phoenix Video BIOS for the Cirrus Logic CL-GD610/620 chip set.

The system BIOS returns the information by reading from CMOS RAM. Refer to 3.6 Interrupt 15H

Support and 3.7 Get Configuration or User Options for details on the Interrupt 15H calls.

NOTE: If Interrupt 15H is not supported in the system BIOS, the alternative is to use hardware switches to provide configuration information.

3.1.1.1 Setup

The Phoenix Setup program allows a user to configure their system. This configuration data is stored in CMOS RAM and may be retrieved using Interrupt 15H as described in 3.7 Get Configuration or User Options.

3.1.2 Adapter: DIP Switches

Since it is not possible to use Setup with a VGA adapter card, DIP switches are used as shown in Figure 3-1.

NOTE: Switch values not shown in the figure have no meaning for the particular option being described.

The switch information is contained in two Cirrus Logic Extension registers (Switch Register - High, Switch Register - Low Index 0C4H and 0C5H respectively). These registers are read only and therefore always contain the initial configuration data.

3.1.2.1 Read DIP Switches

Eight bits of configuration and option data are latched when reset is applied to the chips. These bits are latched and available to the BIOS.

Three bits of monitor identification are latched when reset is applied to the video system. These bits are latched and available to the BIOS to determine the presence and type of monitor attached.

sw8	sw7	sw6	sw5	sw4	sw3	sw2	sw1	Option Description
						0	0	Monochrome Display
						0	1	Color Display
						1	0	Enhanced Color Display
						1	1	Color or Monochrome PS/2 (or compatible) Display
			x 0 0 0	x 0 0 1	x 0 1 0			These bits are used to identify the panel display type. These panels are dual panel/dual screen with two drivers. Balance line clock and dot clock/2 (Sharp LCD Display). 241 scan lines upper panel, 241 scan lines lower panel. Free running line clock and dot clock/2. 241 scan lines upper panel, 248 scan lines lower panel. Constrained line clock and dot clock/2. 240 scan lines upper panel, 241 scan lines lower panel.
0	0	0						Reserved
0	0	1						CGA Locked State
0	1	0						MGA Locked State
0	1	1						EGA Locked State
1	0	0						VGA Locked State
1	0	1						VGA Protected State

sw1 - sw2 represent the Monitor type
sw3 - sw5 represent the panel type
sw6 - sw8 represent the State of the VGA adapter

Figure 3-1 . VGA Flat Panel Adapter DIP Switch Settings

3.2 Extension Features

The Cirrus Logic CL-GD610/620 implementation of the Phoenix Extensible Video BIOS includes support for twelve additional video modes. Extension features include inquiry functions and miscellaneous options (i.e. set video state, fast mode, protect mode, etc). To support these features, extensions to Interrupt 10H function 12H have been added in the form of Cirrus Logic specific subfunctions.

The FOCUS utilities provide users with control of certain features provided by the video BIOS.

3.3 Flexible Online Configuration Utility System (FOCUS)

The Flexible Online Configuration Utility System (FOCUS) consists of two Terminate and Stay Resident (TSR) utilities provided with the flat panel Video BIOS. FOCUS gives the user both command line and hot key access to functions and menus which provide video BIOS controlled features.

> **NOTE:** These Utilities are provided to Cirrus Logic as a sales tool to be used for demonstration purposes only and may not be resold by Cirrus Logic to any third party.

Refer to the FOCUS User's Guide for detailed information on using these utilities.

3.3.1 Phoenix Video Control Console

The Phoenix Video Control Console portion of FOCUS provides both command line and state/mode sensitive versions of the configuration menu. The command line version of the menu provides all of the configuration options described below. A state/mode sensitive menu is produced when the menu system is entered using the hot key. There are eleven variations of the hot key menu. Which variation is presented depends on the current display type, video state and mode. The hot key menu types are:

- CRT - Graphics Modes (all states)
- CRT - Text Modes (all states)
- LCD - VGA Text Modes
- LCD - VGA Graphics Modes 4, 5 and 6
- LCD - VGA Graphics Modes 0D-12
- LCD - VGA 256 Color Graphics Mode 13
- LCD - VGA 256 Color Graphics Mode 70
- LCD - MGA (Hercules) Text Modes
- LCD - MGA (Hercules) Graphics Modes
- LCD - EGA and CGA Text Modes
- LCD - EGA and CGA Graphics Modes

Following is a brief description of all of the FOCUS menu options. Included in the description is a list of when the option is available to the user:

OPTION NAME	DESCRIPTION
Display Type	Controls which display is active, CRT or Flat Panel (LCD). Available in all Menus.
Video State	Controls the state the video subsystem runs in: MGA, CGA, EGA or VGA. Available in all Menus.

Horiz Compensation Specifies how to display a 720 dot image on a 640 dot panel.
Available in the full configuration menu, both LCD MGA menus and the LCD VGA 256 Color Graphics Mode 70 menu.

Vertical Position Specifies how to vertically position an image that does not fill the flat panel screen.
Available in the full configuration menu, the LCD VGA menus with the exception of the Mode 70 menu, both LCD MGA menus and both LCD EGA/CGA menus.

Expanded Text Uses a font with a larger character box (8x19) to allow the text to completely fill a 480 line flat panel.
Available in the full configuration menu and LCD VGA text modes menu.

Expanded Graphics Vertically expands the graphics image to to fill as much of a 480 line flat panel as possible.
Available in the full configuration menu, all three LCD VGA graphics modes menus, LCD MGA graphics modes menus and LCD EGA/CGA graphics modes menus.

32 Grey Shades Controls mapping color into 32 shades of grey, which is the default in Mode 13.
Available in the full configuration menu and both LCD VGA 256 Color Graphics mode menus.

Maximum Contrast Selects the highest level of contrast possible on the flat panel.
Available in the full configuration menu, CRT Text modes menu and all LCD text modes menus (VGA, MGA and EGA/CGA).

Intensity w/ Fonts Allows the differentiation of intensified characters while maximum contrast is in effect.
Available in the full configuration menu, CRT Text modes menu and LCD VGA text modes menu.

Text Reverse Video Specifies if text modes are displayed in reverse video or not.
Available in the full configuration menu, CRT text modes menu and all LCD text modes menus (VGA, MGA and EGA/CGA).

Grfx Reverse Video Specifies if graphics modes are displayed in reverse video or not.
Available in the full configuration menu, CRT graphics modes menu and all LCD graphics modes menus (three for VGA, one for MGA and one for EGA/CGA).

Fast Mode Specifies if fast mode is enabled or not. When fast mode is enabled the CL-GD620 can be programmed to provide more CPU access to video memory.
Available in all Menus.

3.3.2 Power User

The Power User (PWRUSER) utility provides a means to map BIOS functions to hot key combinations. A script file defines the individual keys associated with each function that is to be available via the hot key interface. These keys are used in combination with the Power User hot key to perform the specific

function. The script provided with PWRUSER defines keys for Universal Horizontal Compensation and Vertical Position.

3.4 Video Modes

The VGA BIOS implementation for Cirrus Logic CL-GD610/620 supports twelve video modes not included in standard VGA and new variations for modes 0-3 and 7. These modes are described in Figure 3-2. Refer to Figure 2-3 for a description of the standard modes.

> **NOTE:** The new expanded modes (^) are only available to a flat panel display. The Cirrus Logic extended modes which use more than 480 scan lines are not available to a flat panel display.

Mode (hex)	Resolution	Cols.	Rows	Colors	Type	Segment	Comments
0^	320x475 pixels	40	25	16	A	B800	Used with 480 line flat panels. Modes 0^ and 1^ are the same.
1^	320x475 pixels	40	25	16	A	B800	Used with 480 line flat panels.
2^	640x475 pixels	80	25	16	A	B800	Used with 480 line flat panels. Modes 2^ and 3^ are the same.
3^	640x475 pixels	80	25	16	A	B800	Used with 480 line flat panels. Power on default mode for VGA.
7^	640x475 pixels	80	25	2	A	B000	Used with 480 line flat panels.
40	900x390 pixels	100	30	16	A	B800	Character box of 9x13.*
41	800x400 pixels	100	50	16	A	B800	Character box of 8x8.
42	800x480 pixels	100	60	16	A	B800	Character box of 8x8.
43	800x600 pixels	100	75	16	A	B800	Character box of 8x8. Multi Frequency monitor required (i.e. NEC Multisync, SonyMultiscan, or compatible.)
50	1056x390 pixels	132	30	16	A	B800	Character box of 8x13.* Multi Frequency monitor required (i.e. NEC Multisync, SonyMultiscan, or compatible.)
51	1056x400 pixels	132	50	16	A	B800	Character box of 8x8. Multi Frequency monitor required (i.e. NEC Multisync, SonyMultiscan, or compatible.)
52	1056x480 pixels	132	60	16	A	B800	Character box of 8x8. Multi Frequency monitor required (i.e. NEC Multisync, SonyMultiscan, or compatible.)
53	640x480 pixels	80	60	16	A	B800	Character box of 8x8.
62	640x450 pixels	80	28	16	G	A000	Character box of 8x16.
63	720x540 pixels	90	33	16	G	A000	Character box of 8x16.
64	800x600 pixels	100	37	16	G	A000	Character box of 8x16. Multi Frequency monitor required (i.e. NEC Multisync, SonyMultiscan, or compatible.)
70	360x480 pixels	45	30	256	G	A000	Character box of 8x16.

^ New panel modes beyond + and *. ^ modes use a character box of 8x19.
A = Alphanumeric G = Graphics
* The characters appear on screen as ?x13, however they are actually ?x14 fonts with one line thrown away.

Figure 3-2 . BIOS Video Modes for CL-GD610/620

3.5 Extended Function Calls

The PEVB implementation for the Cirrus Logic CL-GD610/620 includes extended support for Interrupt 10H. Interrupt 10H Function 00H is extended to recognize the Cirrus Logic extended modes. Twenty two extended subfunctions have been defined for Interrupt 10H Function 12H. Refer to 3.8 Set Video Mode, page 22 and 3.9 Alternate Select, page 25 for details.

3.6 Interrupt 15H Support

Interrupt 15H is used to retrieve configuration and user option information stored in CMOS RAM.

> **IMPLEMENTATION NOTE:** The Interrupt 15 interface is not implemented for the general release of the Phoenix Video BIOS for the Cirrus Logic CL-GD610/620 chip set.

If the system BIOS supports the Interrupt 15H calls documented on the following pages, the Phoenix VGA BIOS could use them to obtain configuration information at POST time. The configuration data is defined using the Setup program.

> **NOTE:** If Interrupt 15H is not supported in the system BIOS, the alternative is to use hardware switches to provide configuration information.

3.7 Get Configuration or User Options

This is a system BIOS call and must be implemented if there are no hardware switches for the VGA BIOS to read on the mother board.

> NOTE: Adapter card implementations of the Phoenix VGA BIOS will use hardware switches to obtain configuration information.

The Cassette Interface interrupt (Int 15H) is used to obtain the configuration byte or the user options word stored in CMOS RAM.

> IMPLEMENTATION NOTE: The planar BIOS must support subfunction AL=8E unless Interrupt 15 returns a known value for unsupported calls which cannot be mistaken as a configuration byte value.

The AH value is 44H, the AL value is shown below:

AL Value (hex)	Function Description
8E	Get Configuration Byte
8F	Get User Option Word

3.7.1 Get Configuration Byte

Returns the Configuration Byte stored in CMOS RAM.

ON CALL:

Proc Regs: AH = 44
AL = 8E Return Configuration Byte

ON RETURN:

Proc Regs: DL = Configuration Byte
bits 0-3 Monitor Type
0 = Monochrome Display
1 = Color Display
2 = Enhanced Color Display
3 = Digital Multi Frequency Display (Not implemented)
8 = PS/2 or Compatible Display
9 = Analog Multi Frequency Display
bits 4-7 Flat Panel Type
0 = Balance line clock and dot clock/2 (Sharp LCD Display)
241 scan lines upper panel
241 scan lines lower panel
1 = Free running line clock and dot clock/2
241 scan lines upper panel
248 scan lines lower panel
2 = Constrained line clock and dot clock/2
240 scan lines upper panel
241 scan lines lower panel

REMARKS: The monitor type definitions available here are more extensive than those available through DIP switches on an adapter or in the Cirrus Logic Extension Switch Registers.

3.7.2 Get User Options Words

Returns the User Options Configuration words stored in CMOS RAM.

ON CALL:

Proc Regs: AH = 44
AL = 8F Return User Options Words

ON RETURN:

Proc Regs: AH = 0 for success
BX = Second User Option Word
DX = First User Option Word

First User Option configuration word:

bits 0-1 Vertical Position (LCD)
- 0 = Automatic Centering
- 1 = Display at Top of Panel
- 2 = Display at Bottom of Panel

bits 2-3 Universal Horizontal Compensation (LCD)
- 0 = Display left most 640 dots
- 1 = Display right most 640 dots (of 720 dots)
- 2 = Skip every 9th dot
- 3 = 'OR' each 8th dot with 9th dot and drop 9th

bit 4 Graphics Mode Reverse Video (LCD)
- 0 = Reverse Video Enabled
- 1 = Reverse Video Disabled

bits 5-7 State Control
- 0 = Reserved
- 1 = CGA Locked State
- 2 = MGA Locked State
- 3 = EGA Locked State
- 4 = VGA Locked State

bit 8 CRT Operation
- 0 = Flat Panel is Display
- 1 = CRT is Display

bit 9 Expanded Graphics Mode (LCD)
- 0 = Expanded mode enabled
- 1 = Normal VGA size displays

bit 10 Force 8 bit Operation
- 0 = Run as 16 bit device if possible
- 1 = Force 8 bit opertion

bit 11 Text Mode Reverse Video (LCD)
- 0 = Reverse Video Enabled
- 1 = Reverse Video Disabled.

bit 12 Text Mode Maximum Contrast (LCD)
- 0 = Maximum Contrast Enabled
- 1 = Maximum Contrast Disabled

bit 13 Text Mode Intensity with Fonts (LCD)
- 0 = Intensity with Fonts Enabled
- 1 = Intensity with Fonts Disabled

bit 14 Fast Mode
- 0 = Safe Mode
- 1 = Fast Mode

bit 15 Protect Mode
- 0 = Monitor timing not protected
- 1 = Monitor timing protected

Second User Option configuration word:

bits 0-1 Reserved = 0

bits 2-3 Mode Sensitive Horizontal Compensation (LCD)
- 0 = Display left most 640 dots
- 1 = Display right most 640 dots
- 2 = Skip every 9th dot
- 3 = 'OR' each 8th dot with 9th dot and drop 9th

bit 4 Graphics Mode Reverse Video (CRT)
- 0 = Reverse Video Enabled
- 1 = Reverse Video Disabled

bits 5-9 Reserved = 0

bit 10 256x4 Memory Check
- 0 = No (memory is not 256x4)
- 1 = Yes (memory is 256x4)

bit 11 Text Mode Reverse Video (CRT)
- 0 = Reverse Video Enabled
- 1 = Reverse Video Disabled

bit 12 Text Mode Maximum Contrast (CRT)
- 0 = Maximum Contrast Enabled
- 1 = Maximum Contrast Disabled

bit 13 Text Mode Intensity with Fonts (CRT)
- 0 = Intensity with Fonts Enabled
- 1 = Intensity with Fonts Disabled

bit 14 Expanded Text Mode (LCD)
- 0 = Expanded Font (19 high)
- 1 = Normal Size Font (16 high)

bit 15 32 Grey Shades (LCD)
- 0 = 32 Grey Shades Enabled
- 1 = 32 Grey Shades Disabled

REMARKS: The user options words available here are the same as those available through Int 10H function 12H subfunction 84H.

3.8 Set Video Mode

Puts the video subsystem into the specified video mode.

All of the video modes are not supported for all emulation states. The following list is meant to provide a brief overview of modes available and is not detailed. Some of the modes listed may include +, * or ^ modes also. Refer to Figures 2-3 and 3-2 for details on the modes supported by the Phoenix BIOS implementation for Cirrus Logic CL-GD610/620 chip set.

ON CALL:

Proc Regs: AH = 00
AL = video mode number:

00	40 x 25 16 color alphanumeric
01	40 x 25 16 color alphanumeric
02	80 x 25 16 color alphanumeric
03	80 x 25 16 color alphanumeric
04	320 x 200 4 color graphics
05	320 x 200 4 color graphics
06	640 x 200 2 color graphics
07	80 x 25 monochrome alphanumeric
08	Reserved (PCjr)
09	Reserved (PCjr)
0A	Reserved (PCjr)
0B	Reserved
0C	Reserved
0D	320 x 200 16 color graphics
0E	640 x 200 16 color graphics
0F	640 x 350 monochrome graphics
10	640 x 350 16 color graphics
11	640 x 480 2 color graphics
12	640 x 480 16 color graphics
13	320 x 200 256 color graphics
40	900 x 390 16 color alphanumeric
41	800 x 400 16 color alphanumeric
42	800 x 480 16 color alphanumeric
43	800 x 600 16 color alphanumeric
50	1056 x 390 16 color alphanumeric
51	1056 x 400 16 color alphanumeric
52	1056 x 480 16 color alphanumeric
53	640 x 480 16 color alphanumeric
62	640 x 450 16 color graphics
63	720 x 540 16 color graphics
64	800 x 600 16 color graphics
70	360 x 480 256 color graphics

NOTE: If bit 7 in AL is set to 1, the video buffer is not cleared.

VGA Regs: None

Cirrus Regs: Scratch Registers 0-3 (SCR0-3) Index B0-B3
These scratch registers hold the User Options Configuration Words

Seg 40H: All information about monitor types and scan lines.

Also uses pointer to primary save pointer table to get information about primary and secondary alpha numeric text overrides.

ON RETURN:

Proc Regs: None

VGA Regs: All of the VGA Hardware registers are modified by this function.

Cirrus Regs:

Write Control Register (WRC) Index 084H bits 0 and 4
Bandwidth Control Register (BWC) Index 86H bits 0-2 and 4
LCD Control Register (LCDCNTLI) Index 8AH bit 6
Clock Select Register (CLK) Index 0A4H bit 4
Cursor Attribute Register (CURS) Index 0A5H
Column Offset Register (COLOFF) Index 0D0H)
Row Offset Register (ROWOFF) Index 0D2H
Panel Control 1 (PNLCTLI) Index 0D4H bits 4 and 6
Panel Control 2 (PNLCTLII) Index 0D5H bits 0-3 and 6
Scratch Register (SCR1) Index 0B0H bit 7

Seg 40H:

[49]	CRT_MODE
[4A]	CRT_COLS
[4C]	CRT_PLEN
[4E]	CRT_POFF
[50]	CURSPOS0
[52]	CURSPOS1
[54]	CURSPOS2
[56]	CURSPOS3
[58]	CURSPOS4
[5A]	CURSPOS5
[5C]	CURSPOS6
[5E]	CURSPOS7
[60]	CURSMODE
[62]	ACTIVPAG
[63]	ADDRCRTC
[65]	MDCTLVAL
[66]	CLRSLVAL
[84]	ROWSMNS1
[85]	BYTESCHR
[87]	GENINFO1
[88]	GENINFO2
[89]	GENINFO3

REMARKS: When a request for a legal mode is given, the BIOS clears the screen and positions the

cursor in the top left hand corner. The screen is not cleared if bit 7 is set in AL.

NOTE: When an undefined mode is requested the BIOS returns without doing anything. The system remains in the mode it was in before the request was issued.

Invalid modes are modes that are defined but are not permitted for the current monitor or state. When an invalid mode is requested, IBM forces mode 0 if a color monitor is attached, mode 7 if a monochrome monitor is attached.

3.9 Alternate Select

In addition to the basic VGA functions provided by this call, the Cirrus Logic CL-GD610/620 implementation provides the following:

BL Value (hex)	Function Description
80	Get VGA Type
81	Get BIOS Version
84	Get User Options Configuration Words
85	Get Installed Memory
86	Set Video State
87	Enable/Disable Fast Mode
88	Enable/Disable Protect Mode
89	Enable/Disable Text Reverse Video
8A*	Set Frame Color
8B	Enable/Disable Text Mode Intensity with Fonts
8C	Enable/Disable Maximum Contrast or Auto Grey Scale Mapping
8D	Enable/Disable ATTRIB Palette Lock
8E*	Grey Scale Lookup Bypass
8F*	Enable/Disable Expanded Graphics Mode
90*	Vertical Position
91*	Horizontal Compensation
92	Set Display Type
93	Set 8 bit Operation
94*	Power Conserve Mode
95*	Enable/Disable Expanded Text
96*	Enable/Disable 32 Grey Shades
97	Enable/Disable Graphics Reverse Video

* Only has an effect when the LCD is the active display

These functions are fully described on the following pages.

3.9.1 Get VGA Type

Returns the type of Cirrus Logic VGA controller.

ON CALL:

Proc Regs: AH = 12
BL = 80

Cirrus Regs: None

ON RETURN:

Proc Regs: AL = Controller Type
00 Extended alternate select not supported
01 Eagle I
02 Eagle II
03 Stingray
AH = Capabilities Mask
All bits reserved = 0

Cirrus Regs: None

REMARKS: Provides a mechanism for software to determine the type of VGA controller and its corresponding hardware capabilities.

NOTE: The Phoenix BIOS recognizes the Cirrus Logic CL-GD610/620 chip set and always returns 03 (Stingray).

3.9.2 Get BIOS Version

Returns BIOS version number.

ON CALL:

Proc Regs: AH = 12
BL = 81

Cirrus Regs: None

ON RETURN:

Proc Regs: AH = Major BIOS version number
AL = minor BIOS version number

Cirrus Regs: None

REMARKS: The version number is hard coded in ROM.

The version number is of the form *MM.mm* where:
MM The Major BIOS version number
mm The minor BIOS version number

3.9.3 Get User Options

Returns the user options configuration words.

ON CALL:

Proc Regs: AH = 12
BL = 84

Cirrus Regs: The user options configuration words are held in four Cirrus Extension Scratch registers:
Index 0B0H = Upper byte (bits 15-8) of First User Options Word
Index 0B1H = Lower byte (bits 7-0) of First User Options Word
Index 0B2H = Upper byte (bits 15-8) of Second User Options Word
Index 0B3H = Lower byte (bits 7-0) of Second User Options Word

ON RETURN:

Proc Regs: AX = First User Options Word
BX = Second User Options Word

First User Options configuration word:

bits 0-1 Vertical Position (LCD)
- 0 = Automatic Centering
- 1 = Display at Top of Panel
- 2 = Display at Bottom of Panel

bits 2-3 Universal Horizontal Compensation (LCD)
- 0 = Display left most 640 dots
- 1 = Display right most 640 dots
- 2 = Skip every 9th dot
- 3 = 'OR' each 8th dot with 9th dot and drop 9th

bit 4 Graphics Mode Reverse Video (LCD)
- 0 = Reverse Video Enabled
- 1 = Reverse Video Disabled

bits 5-7 State Control
- 0 = Reserved
- 1 = CGA Locked State
- 2 = MGA Locked State
- 3 = EGA Locked State
- 4 = VGA Locked State

bit 8 CRT Operation
- 0 = Flat Panel is Display
- 1 = CRT is Display

bit 9 Expanded Graphics Mode (LCD)
- 0 = Expanded mode enabled
- 1 = Normal VGA size displays

bit 10 Force 8 bit Operation
- 0 = Run as 16 bit device if possible
- 1 = Force 8 bit opertion

bit 11 Text Mode Reverse Video (LCD)
0 = Reverse Video Enabled
1 = Reverse Video Disabled
bit 12 Text Mode Maximum Contrast (LCD)
0 = Maximum Contrast Enabled
1 = Maximum Contrast Disabled
bit 13 Intensity with Fonts (LCD)
0 = Intensity with Fonts Enabled
1 = Intensity with Fonts Disabled
bit 14 Fast Mode
0 = Safe Mode
1 = Fast Mode
bit 15 Protect Mode
0 = Monitor timing not protected
1 = Monitor timing protected

Second User Options configuration word:
bits 0-1 Reserved = 0
bits 2-3 Mode Sensitive Horizontal Compensation (LCD)
0 = Display left most 640 dots
1 = Display right most 640 dots
2 = Skip every 9th dot
3 = 'OR' each 8th dot with 9th dot and drop 9th
bit 4 Graphics Mode Reverse Video (CRT)
0 = Reverse Video Enabled
1 = Reverse Video Disabled
bits 5-9 Reserved = 0
bit 10 256x4 Memory Check
0 = No (memory is not 256x4)
1 = Yes (memory is 256x4)
bit 11 Text Mode Reverse Video (CRT)
0 = Reverse Video Enabled
1 = Reverse Video Disabled
bit 12 Text Mode Maximum Contrast (CRT)
0 = Maximum Contrast Enabled
1 = Maximum Contrast Disabled
bit 13 Text Mode Intensity with Fonts (CRT)
0 = Intensity with Fonts Enabled
1 = Intensity with Fonts Disabled
bit 14 Expanded Text Mode (LCD)
0 = Expanded Font (19 high)
1 = Normal Size Font (16 high)
bit 15 32 Grey Shades (LCD)
0 = 32 Grey Shades Enabled
1 = 32 Grey Shades Disabled

Cirrus Regs: None

REMARKS: Refer to the corresponding BIOS call for details on each of the areas for which information is returned.

3.9.4 Get Installed Memory

Returns the amount of video memory.

ON CALL:

Proc Regs: AH = 12
BL = 85

Cirrus Regs: Scratch Register Index 0B2H bit 2
At initialization, a memory test is done to determine if one meg of video memory is available. If it is, bit 2 of scratch register 0B2H (bit 10 of Second User Options word) is set to 1. This bit is then referenced to check if one meg of video memory is available. If not, memory available is read from segment 40 data.

Seg 40H: GENINFO1 [0040:0087] bits 6-5 (read if less than one meg video memory available)

ON RETURN:

Proc Regs: AX = Amount of video memory in 64k units.

Cirrus Regs: None

REMARKS: None

3.9.5 Set Video State

Controls the state the video subsystem runs in.

ON CALL:

Proc Regs: AH = 12
BL = 86
AL = video state
00 Reserved
01 CGA Locked
02 MGA Locked
03 EGA Locked
04 VGA Locked

Cirrus Regs: Scratch Register Index 0B1H bits 5-7
These bits are bits 5-7 First User Options word - State Control

ON RETURN:

Proc Regs: None

Cirrus Regs: Timing Control Register (TC) Index 085H bits 4, 6 and 7,
Bit 4 - 6845 scan line doubling
Bit 6 - CMGA HRTC Polarity Reversal
Bit 7 - CMGA VRTC Polarity Reversal
Active Adapter State Register (STATE) Index 0AFH
Contains current state info and maintains a record of the previous state.
Scratch Register Index 0B1H bits 5-7
These bits are bits 5-7 First User Options word - State Control
This call updates all of the registers updated by a setmode (Int 10, AH=00) call.
Refer to 3.8 Set Video Mode, page 22 for details.

VGA Regs: Since this call performs a set mode, all of the VGA hardware registers may be modified by this function.

REMARKS: The specified state takes effect immediately and remains in effect until the next set state function call or the next cold boot. When the state is changed the mode is set to the power on default mode for the specified state and monitor(s) combination as follows:

STATE	MONITOR(S)	DEFAULT
VGA	LCD and Color CRT	LCD-Mode 3^, Color CRT-Mode 3+
	LCD and Mono CRT	LCD-Mode 7^, Mono CRT-Mode 7+
	LCD alone	Mode 3^
EGA	LCD and Color CRT	Both - Mode 3*
	LCD and Mono CRT	Both - Mode 7
	LCD alone	Mode 3*
CGA	LCD and Color CRT	Both - Mode 3
	LCD and Mono CRT	Both - Mode 7
	LCD alone	Mode 3
MGA	LCD and Color CRT	Both - Mode 7
	LCD and Mono CRT	Both - Mode 7
	LCD alone	Mode 7

SYSTEM DEFAULT: To whatever state is specified by the hardware switches.

3.9.6 Fast Mode

Enables/Disables fast mode.

ON CALL:

Proc Regs: AH = 12
BL = 87
AL = enable/disable
00 safe mode (disable fast mode)
01 enable fast mode

Cirrus Regs: Scratch Register Index 0B0H bit 6
Bit 6 is bit 14 First User Options word - Fast Mode

Seg 40H: [4A] CRT_COLS Number of character columns displayed (40 or 80)

ON RETURN:

Proc Regs: None

Cirrus Regs: Bandwidth Control Register (BWC) Index 86H
Selects memory bandwidth. The content of this register only has meaning if Miscellaneous Control Register 1 (MC1) Index 080H bit 4 is set to zero (0).
Scratch Register Index 0B0H bit 6
Bit 6 is bit 14 First User Options word - Fast Mode

REMARKS: Allows the CL-GD620 to be programmed to provide more CPU access to video memory. Takes effect immediately. The CPU access is determined by the CPU to CRT interleave ratio. In 40 column modes this ratio is 3:2 and cannot be changed. In all other display modes the safe mode ratio is 1:4 and can be changed to 1:1 for fast mode.

SYSTEM DEFAULT: Safe Mode

3.9.7 Protect Mode

Enables/Disables protect mode.

ON CALL:

Proc Regs: AH = 12
BL = 88
AL = enable/disable
00 disable protect mode
01 enable protect mode

Cirrus Regs: Scratch Register Index 0B0H bit 7
Bit 7 is bit 15 First User Options word - Protect Mode

ON RETURN:

Proc Regs: None

Cirrus Regs: Write Control Register (WRC) Index 084H bits 4 and 0
Bit 4 enables/disables write of 6845 Monitor Timing registers.
Bit 0 enables/disables CRTC Monitor Timing registers and MISC Output Register clock bits.
Scratch Register Index 0B0H bit 7
Bit 7 is bit 15 First User Options word - Protect Mode

REMARKS: When protect mode is enabled, the registers that control monitor timing are write protected. Takes effect immediately.

NOTE: Protect mode remains in effect until the next set mode call or when the system is booted.

SYSTEM DEFAULT: Disabled

3.9.8 Text Reverse Video

Enable/disable text mode reverse video.

NOTE: This Video BIOS function only has effect in text modes.

ON CALL:

Proc Regs: AH = 12
BL = 89
AL = enable/disable
00 enable text reverse video for LCD
01 disable text reverse video for LCD
02 enable text reverse video for CRT
03 disable text reverse video for CRT

Cirrus Regs: Scratch Register Index 0B0H bit 3
Bit 3 is bit 11 First User Options word - LCD Text Mode Reverse Video
Scratch Register Index 0B2H bit 3
Bit 3 is bit 11 Second User Options word - CRT Text Mode Reverse Video

ON RETURN:

Proc Regs: None

Cirrus Regs: Cursor Attributes (CURS) Index 0A5H
At initialization, the Caret Width (CW) and Caret Height (CH) registers Indices 096H and 097H respectively, are both initialized to 1. This permits the Cursor Attributes register to be used to enable/disable reverse video on the CRT.
Scratch Register Index 0B0H bit 3
Bit 3 is bit 11 First User Options word - LCD Text Mode Reverse Video
Scratch Register Index 0B2H bit 3
Bit 3 is bit 11 Second User Options word - CRT Text Mode Reverse Video
Panel Control 2 (PNLCTLII) Index 0D5H bit 6
Enables/disables text reverse video for the LCD

REMARKS: Determines if text modes are displayed in reverse video or not. If a request for reverse video is issued and the current mode is a text mode, reverse video takes effect immediately. If the current mode is a graphics mode, reverse video takes effect when the mode is changed to a text mode.

NOTE: In LCD modes, if a frame color was explicitly set using the Set Frame Color function (Int 10, AH=12, BL=8A), changing from or to reverse video will cause the frame color to be 'reversed' also.

SYSTEM DEFAULT: LCD - Enabled
CRT - Disabled

3.9.9 Set Frame Color

Controls the grey shade of the panel in the portions of the panel not occupied by the current video mode.

NOTE: This Video BIOS function only has effect in LCD modes.

ON CALL:

Proc Regs: AH = 12
BL = 8A
AL = Grey shade for frame color (0 to 15)

Cirrus Regs: None

ON RETURN:

Proc Regs: None

Cirrus Regs: Frame Color (FRCLR) Index 0DAH

REMARKS: Validates grey shade (AL) value and determines the grey shade for screen areas not occupied by the current video mode (i.e. above or below the display, depending upon expanded mode and centering). Setting the frame color explicitly overrides the default frame color. The frame color set by this call remains in effect until the next set frame color call or the next set mode call. Takes effect immediately.

SYSTEM DEFAULT: LCD - Black (00)

NOTE: Since the system defaults to reverse video, the default frame color of black shows up as white in reverse video.

3.9.10 Intensity with Fonts

Enable/disable text mode intensity with fonts.

NOTE: This Video BIOS function only has effect in text modes.

ON CALL:

Proc Regs: AH = 12
BL = 8B
AL = enable/disable
00 Enable intensity with fonts for LCD
01 Disable intensity with fonts for LCD
02 Enable intensity with fonts for CRT
03 Disable intensity with fonts for CRT

Cirrus Regs: Scratch Register Index 0B0H bits 4 and 0
Bit 4 is bit 13 First User Options word - Intensity with Fonts LCD
Bit 0 is bit 8 First User Options word - CRT Operation
Scratch Register Index 0B2H bit 4
Bit 4 is bit 13 First User Options word - Intensity with Fonts CRT

VGA Regs: Character Map Select (SEQ Index 03)

ON RETURN:

Proc Regs: None

Cirrus Regs: Scratch Register Index 0B0H bit 4
Bit 4 is bit 13 First User Options word - Intensity with Fonts LCD
Scratch Register Index 0B2H bit 4
Bit 4 is bit 13 First User Options word - Intensity with Fonts CRT

VGA Regs: Character Map Select (SEQ Index 03)

REMARKS: Controls visible font differentiation for intensified text mode attributes. When 'Intensity with Fonts' is in effect, a 'thin' font is used as the default font and the normal default font is used as a 'bold' font. The intensity bit triggers the use of the bold font. Takes effect immediately.

NOTE: On CRT monitors the 'bold' font characters will also be intensified since the intensity bit is on.

If a request for 'Intensity with Fonts' is issued and the current mode is a text mode, use of the thin and normal fonts takes effect immediately. If the current mode is a graphics mode, the request takes effect when the mode is changed to a text mode.

SYSTEM DEFAULT: LCD - Enabled
CRT - Disabled

3.9.11 Max Contrast or Auto Grey Scale Mapping

Enables maximum text mode attribute contrast in flat panel or monochrome CRT modes.

NOTE: This Video BIOS function only has effect in text modes on either the flat panel or in monochrome CRT modes.

ON CALL:

Proc Regs: AH = 12
BL = 8C
AL = enable/disable
00 Enable maximum contrast mode for LCD
01 Enable automatic grey scale mapping for LCD
02 Enable maximum contrast mode for CRT
03 Disable maximum contrast mode for CRT

Cirrus Regs: Scratch Register Index 0B0H bits 0 and 4
Bit 0 is bit 8 First User Options word - CRT Operation
Bit 4 is bit 12 First User Options word - Text Mode Maximum Contrast (LCD)
Scratch Register Index 0B2H bit 4
Bit 4 is bit 12 Second User Options word - Text Mode Maximum Contrast (CRT)

ON RETURN:

Proc Regs: None

Cirrus Regs: Scratch Register Index 0B0H bit 4
Bit 4 is bit 12 First User Options word - Text Mode Maximum Contrast (LCD)
Scratch Register Index 0B2H bit 4
Bit 4 is bit 12 Second User Options word - Text Mode Maximum Contrast (CRT)
Panel Control 2 (PNLCTLII) Index 0D5H bit 5
Bit 5 enables/disables maximum contrast color mapping.

REMARKS: This creates the highest level of contrast possible by mapping colors in text modes to shades of grey. Operates by selecting the grey shade based on the comparison of the foreground and background attribute values. When foreground is equal to background, the grey shade is that value. When foreground is greater than background, the foreground is white and the background is black and vice versa. The flat panel internal palette and the attribute controller palette registers are bypassed.

CAUTION: If the display is a color CRT in a color mode, this call produces strange looking output.

If a request for 'Maximum Contrast' is issued and the current mode is a text mode, maximum contrast takes effect immediately. If the current mode is a graphics mode, the request takes effect when the mode is changed to a text mode.

If the LCD is the current display, automatic grey scale mapping is used when maximum contrast is disabled.

SYSTEM DEFAULT: LCD - Enabled
CRT - Disabled

3.9.12 ATTRIB Palette Lock

Enable/disable write protect of the Attribute Controller Palette Registers (Indices 00-FF).

ON CALL:

Proc Regs: AH = 12
BL = 8D
AL = enable/disable
00 enable write protect of palette registers (lock)
01 disable write protect of palette registers (unlock)

Cirrus Regs: None

ON RETURN:

Proc Regs: None

Cirrus Regs: Panel Control 2 (PNLCTLII) Index 0D5H bit 2
Bit 2 enables/disables attribute palette protection.

REMARKS: While the palette registers are locked, all BIOS function calls to load the palette, except set mode (AH=00), have no effect. When the palette registers are locked, a set mode call clears the lock and loads the palette registers as expected. This function takes effect immediately.

NOTE: Maximum Contrast (AH=12, BL=8C) supercedes this function since it causes the internal palette to be bypassed.

SYSTEM DEFAULT: Disabled

3.9.13 Grey Scale Lookup Bypass

Part of the grey scale management. A lookup table maps the CRT DAC values to shades of grey for the flat panel.

NOTE: This Video BIOS function only has effect in LCD text modes.

ON CALL:

Proc Regs: AH = 12
BL = 8E
AL = enable/disable
00 use the flat panel grey scale look up table.
01 bypass the flat panel grey scale look up table.

Cirrus Regs: None

ON RETURN:

Proc Regs: None

Cirrus Regs: Panel Control 2 (PNLCTLII) Index 0D5H bit 7

REMARKS: Attribute Controller output goes directly to the flat panel display while the flat panel grey scale mapping is bypassed. Takes effect immediately.

NOTE: Maximum Contrast (AH=12, BL=8C) supercedes this function since it causes the internal palette to be bypassed.

SYSTEM DEFAULT: Use flat panel grey scale lookup table

3.9.14 Expanded Graphics Mode

Enable/disable expanded mode for graphics modes.

NOTE: This Video BIOS function only has effect in LCD modes.

ON CALL:

Proc Regs: AH = 12
BL = 8F
AL = enable/disable
00 enable expanded graphics mode
01 disable expanded graphics mode

Cirrus Regs: Scratch Register Index 0B0H bits 0 and 1
Bit 0 is bit 8 First User Options word - CRT Operation
Bit 1 is bit 9 First User Options word - Expanded Graphics Mode (LCD)
Scratch Register Index 0B1H bits 0-1
These bits are bits 0-1 First User Options word - Vertical Position (LCD)

ON RETURN:

Proc Regs: None

Cirrus Regs: Scratch Register Index 0B0H bit 1
Bit 1 is bit 9 First User Options word - Expanded Graphics Mode (LCD)
LCD Control 2 (LCDCNTLII) Index 0C2H bit 1
Enables/disables scan line replication in flat panel graphics modes.
Row Offset (ROWOFF) Index 0D2H
If auto centering is off, this register determines where the image appears on the panel (top or bottom).
Panel Control 1 (PNLCTLI) Index 0D4H bits 6 and 3
Bit 6 is the overflow (9th) bit for ROWOFF
Bit 3 enables/disables flat panel centering for nonexpanded modes.

REMARKS: Controls the vertical expansion of the display in graphics modes to fill as much of the flat panel as possible. Takes effect immediately.

NOTE: This is not the same as using the expanded text font to fill the LCD screen in text modes.

SYSTEM DEFAULT: Disabled

3.9.15 Vertical Position

Used to control the vertical position of an image that does not fill the flat panel.

NOTE: This Video BIOS function only has effect in LCD modes.

ON CALL:

Proc Regs: AH = 12
BL = 90
AL = 00 enable automatic centering
01 display at top of panel
02 display at bottom of panel

Cirrus Regs: Scratch Register Index 0B0H bits 0 and 1
Bit 0 is bit 8 First User Options word - CRT Operation
Bit 1 is bit 9 First User Options word - Expanded Graphics Mode (LCD)
Scratch Register Index 0B1H bits 0-1
These bits are bits 0-1 First User Options word - Vertical Position (LCD)

ON RETURN:

Proc Regs: None

Cirrus Regs: Scratch Register Index 0B1H bits 0-1
These bits are bits 0-1 First User Options word - Vertical Position (LCD)
Row Offset (ROWOFF) Index 0D2H
If auto centering is off, this register determines where the image appears on the panel (top or bottom).
Panel Control 1 (PNLCTLI) Index 0D4H bits 6 and 3
Bit 6 is the overflow (9th) bit for ROWOFF
Bit 3 enables/disables flat panel centering for nonexpanded modes.

REMARKS: Controls the vertical position of the display image on the panel for video modes that have fewer scan lines than the panel size. Takes effect immediately.

SYSTEM DEFAULT: Automatic Centering

3.9.16 Horizontal Compensation

Used to control the horizontal position or width of an image. Specifies how 720 dot modes are displayed on the 640 dot panel.

NOTE: This Video BIOS function only has effect in LCD modes. The 'mode sensitive' options for this function have effect in Cirrus Extended mode 70 (a VGA mode) and MGA (Hercules) mode only.

The 'universal' options for this function have effect for all modes and all states.

ON CALL:

Proc Regs: AH = 12
BL = 91
AL = 00 display left 640 pixels (universal)
01 display right 640 pixels (universal)
02 skip every 9th pixel (universal)
03 'OR' every 8th and 9th pixel (universal)
04 display left 640 pixels (mode sensitive)
05 display right 640 pixels (mode sensitive)
06 skip every 9th pixel (mode sensitive)
07 'OR' every 8th and 9th pixel (mode sensitive)

Cirrus Regs: Scratch Register Index 0B1H bits 2-3
These bits are bits 2-3 First User Options word - Universal Horizontal Compensation
Scratch Register Index 0B3H bits 2-3
These bits are bits 2-3 Second User Options word - Mode Sensitive Horizontal Compensation

ON RETURN:

Proc Regs: None

Cirrus Regs: LCD Control Register (LCDCNTL,I) Index 8AH bit 6
Forces VGA and MGA text modes to run with 8 dots per character. Good for both CRT and flat panel modes.
Scratch Register Index 0B1H bits 2-3
These bits are bits 2-3 First User Options word - Universal Horizontal Compensation
Scratch Register Index 0B3H bits 2-3
These bits are bits 2-3 Second User Options word - Mode Sensitive Horizontal Compensation
Column Offset Register (COLOFF) Index 0D0H bits 7-0
Used to select whether to display left most or right most 640 pixels.
Panel Control 1 (PNLCTLI) Index 0D4H bit 4
The overflow (9th) bit for COLOFF
Panel Control 2 (PNLCTLII) Index 0D5H bits 1-0
Selects how to display 720 pixel images on a 640 pixel display; left or right 640

pixels, skip every 9th pixel, OR every 8th and 9th pixel. Uses COLOFF reg to determine left or right 640 display.

REMARKS: Although this call is designed for 720 dot modes, the universal options work in any mode. If the image is greater than 720 dots wide, the 'display right 640 option' displays a 640 dot wide portion of the image beginning with dot 81. Takes effect immediately.

NOTE: The Mode Sensitive options are only available if the current state of the Universal Horizontal Compensation is 'display left most 640 dots'. If Universal Horizontal Compensation is set to anything else, the Mode Sensitive options have no effect.

SYSTEM DEFAULT: Left 640 Pixels

3.9.17 Set Display Type

Specifies whether the flat panel or the CRT is the active display.

NOTE: This Video BIOS function only works in VGA mode.

ON CALL:

Proc Regs: AH = 12
BL = 92
AL = 00 enable Flat Panel for display
01 enable CRT for display

Cirrus Regs: Scratch Register Index 0B0H bits 0 and 3-5
Bit 0 is bit 8 First User Options word - CRT Operation
Bit 3 is bit 11 First User Options word - Text Mode Reverse Video (LCD)
Bit 4 is bit 12 First User Options word - Text Mode Maximum Contrast (LCD)
Bit 5 is bit 13 First User Options word - Intensity with Fonts (LCD)
Scratch Register Index 0B1H bits 0-7
Bits 5-7 are bits 5-7 First User Options word - State Control
Bit 4 is bit 4 First User Options word - Graphics Mode Reverse Video (LCD)
Bits 2-3 are bits 2-3 First User Options word - Universal Horizontal Compensation (LCD)
Bits 0-1 are bits 0-1 First User Options word - Vertical Position (LCD)
Scratch Register Index 0B2H bits 3-5
Bit 3 is bit 11 Second User Options word - Text Mode Reverse Video (LCD)
Bit 4 is bit 12 Second User Options word - Text Mode Maximum Contrast (LCD)
Bit 5 is bit 13 Second User Options word - Intensity with Fonts (LCD)
Scratch Register Index 0B3H bits 2-3
Bits 2-3 are bits 2-3 Second User Options word - Mode Sensitive Horizontal Compensation (LCD)

Seg 40H:

[49]	CRT_MODE	Video mode setting
[63]	ADDRCRTC	6845 compatible I/O port address for current mode.
[85]	BYTESCHR	Height of character matrix
[87]	GENINF01	Informational byte
[89]	GENINFO3	Informational byte

ON RETURN:

Proc Regs: None

Cirrus Regs: Clock Select (CLK) Index 0A4H bits 5-7
Selects clocks for MGA modes
LCD Control 2 (LCDCNTLII) Index 0C2H bits 3-2
Specifies CRT or LCD for type of display.
Column Offset Register (COLOFF) Index 0D0H bits 7-0
Used to select whether to display left most or right most 640 pixels.
Row Offset (ROWOFF) Index 0D2H
Used to determine the vertical position of a displayable image (top, bottom or

center)
Panel Control 1 (PNLCTLI) Index 0D4H bit 6
Bit 6 is the overflow (9th) bit for ROWOFF
Panel Control 2 (PNLCTLII) Index 0D5H bits 2 and 7
Bit 2 protects the attribute palette
Bit 7 enables the internal grey scale generation circuit to receive input data from the 256x4 internal palette which keeps track of the CRT RAMDAC contents, applies the sum to grey conversion and stores the result in 256 4 bit locations.
This call updates all of the registers updated by a setmode (Int 10, AH=00) call. Refer to 3.8 Set Video Mode, page 22 for details.

VGA Regs: Feature Control Register (GENR) bits 0-1

NOTE: These bits are not used for standard VGA and are specified as reserved by IBM, Cirrus Logic uses them as described below:

bit 1	bit 0	Description
0	0	Flat Panel Standby mode
0	1	Flat Panel Active
1	0	CRT Active
1	1	Undefined

Since this call performs a set mode, all of the VGA hardware registers may be modified by this function.

Seg 40H:

[50+(ACTIVPAG*2)]	CURSPOSn	Used to decide where to put character and whether or not to wrap the cursor position.
[87]	GENINFO1	Informational byte

REMARKS: Takes effect immediately when in VGA state (not at all in any other state). The BIOS attempts to preserve the screen image exactly as it appears when the display is switched. The CRT will be driven as a color monitor if it is PS/2 compatible and was not connected at the time the system was powered up. There is no other error checking on this function..

SYSTEM DEFAULT: Flat Panel (LCD)

3.9.18 Set 8 bit Operation

Used to force the system to run as an 8 bit device.

ON CALL:

Proc Regs: AH = 12
BL = 93
AL = 00 allow system to run as 16 bit device
01 force system to run as 8 bit device

Cirrus Regs: Scratch Register Index 0B0H bits 2
Bit 2 is bit 10 First User Options word - Force 8 bit Operation

ON RETURN:

Proc Regs: None

Cirrus Regs: Scratch Register Index 0B0H bits 2
Bit 2 is bit 10 First User Options word - Force 8 bit Operation
LCD Control 3 (LCDCNTLIII) Index 0C7H bit 0
Selects 8 or 16 bit bus operation.

REMARKS: Used to force 8 bit operation in an environment where 16 bit operation is possible. Takes effect immediately.

SYSTEM DEFAULT: Allow system to run as 16 bit device

3.9.19 Power Conserve Mode

Enable/disable power conserve mode.

NOTE: External hardware is required to actually perform a power shutdown.

ON CALL:

Proc Regs: AH = 12
BL = 94
AL = 00 normal operation
01 power conserve mode

Cirrus Regs: Scratch Register Index 0B0H bit 0
This bit is bit 8 First User Options word - CRT Operation

Seg 40H: [63] ADDRCRTC 6845 compatible I/O port address for current mode.

ON RETURN:

Proc Regs: None

Cirrus Regs: LCD Control Register (LCDCNTLI) Index 8AH bit 7
Enable/disable power save mode.

VGA Regs: Feature Control Register (GENR) bits 0-1

NOTE: These bits are not used for standard VGA and are specified as reserved by IBM, Cirrus Logic uses them as described below. While the system is in power conserve mode, these bits are write protected.

bit 1	bit 0	Description
0	0	Display in Standby mode
0	1	Flat Panel Active
1	0	CRT Active
1	1	Undefined

REMARKS: Useful in power management. When the system is in power conserve mode, the screen is blanked, the flat panel backlight is turned off, video DRAM refresh is reduced, RAS and CAS are reduced, and the ITS clock to the CL-GD610 is turned off. Writes to the video buffer work normally while in power conserve mode. When normal operation is resumed, the video system is restored to the state it was in before power conserve mode was entered. This includes restoring the screen image. Takes effect immediately.

NOTE: It is the responsibility of the software that placed the system in power conserve mode turn it back on when needed.

SYSTEM DEFAULT: Normal Operation

3.9.20 Expanded Text Mode

Enable/disable expanded text for text modes.

NOTE: This Video BIOS function only has effect in LCD text modes.

ON CALL:

Proc Regs: AH = 12
BL = 95
AL = 00 enable expanded text mode
01 disable expanded text mode

Cirrus Regs: Scratch Register Index 0B0H bit 0
This bit is bit 8 First User Options word - CRT Operation
Scratch Register Index 0B2H bit 6
This bit is bit 14 Second User Options word - Expanded Text Mode (LCD)

Seg 40H: [85] BYTESCHR Height of character matrix
[89] GENINFO3 Information byte bits 7 and 4
These bits are used to determine the number of scan lines in the current mode.

ON RETURN:

Proc Regs: None

Cirrus Regs: Scratch Register Index 0B2H bit 6
This bit is bit 14 Second User Options word - Expanded Text Mode (LCD)
LCD Control 2 (LCDCNTLII) Index 0C2H bit 0
Supports expanded LCD text modes using 19 line character fonts.
This call updates all of the registers updated by a setmode (Int 10, AH=00) call. Refer to 3.8 Set Video Mode, page 22 for details.

VGA Regs: Since this call performs a set mode, all of the VGA hardware registers may be modified by this function.

REMARKS: Uses font with an 8x19 character box to allow the text to completely fill a 480 line flat panel.

NOTE: The expanded font is only used in VGA 400 line text modes using a 16 high (or greater) font on an LCD. In all other cases, the normal font size is used even if this option is enabled.

Takes effect immediately.

NOTE: This is not the same as using the expanded graphics mode used to fill the screen in graphics modes.

SYSTEM DEFAULT: Enabled

3.9.21 32 Grey Shades

Enables/Disables stipple (32 grey shades).

NOTE: This Video BIOS function only has effect on the LCD in VGA graphics mode 13 and Cirrus Extended mode 70.

ON CALL:

Proc Regs: AH = 12
BL = 96
AL = enable/disable
00 enable 32 grey shades
01 disable 32 grey shades

Cirrus Regs: Scratch Register Index 0B2H bit 7
This bit is bit 15 Second User Options word - 32 Grey Shades (LCD)

ON RETURN:

Proc Regs: None

Cirrus Regs: Scratch Register Index 0B2H bit 7
This bit is bit 15 Second User Options word - 32 Grey Shades (LCD)
Grey Scale Offset Register (GROFF) Index 0D6H bit 7
Bit 7 enables/disables stippling

REMARKS: 256 color modes are displayed on a monochrome flat panel display in 32 (instead of 16) shades of grey when stippling is enabled. Each pixel is represented by two bits and one bit gets a different color value than the other bit when stippling is enabled.

SYSTEM DEFAULT: Enabled

3.9.22 Graphics Reverse Video

Enable/disable graphics mode reverse video.

NOTE: This Video BIOS function only has effect in graphics modes.

ON CALL:

Proc Regs: AH = 12
BL = 97
AL = enable/disable
00 enable graphics reverse video for LCD
01 disable graphics reverse video for LCD
02 enable graphics reverse video for CRT
03 disable graphics reverse video for CRT

Cirrus Regs: Scratch Register Index 0B0H bit 0
This bit is bit 8 First User Options word - CRT Operation
Scratch Register Index 0B1H bit 4
This bit is bit 4 First User Options word - Graphics Mode Reverse Video (LCD)
Scratch Register Index 0B3H bit 4
This bit is bit 4 First User Options word - Graphics Mode Reverse Video (CRT)

ON RETURN:

Proc Regs: None

Cirrus Regs: Cursor Attributes (CURS) Index 0A5H
At initialization, the Caret Width (CW) and Caret Height (CH) registers Indices 096H and 097H respectively, are both initialized to 1. This permits the Cursor Attributes register to be used to enable/disable reverse video on the CRT.
Scratch Register Index 0B1H bit 4
This bit is bit 4 First User Options word - Graphics Mode Reverse Video (LCD)
Scratch Register Index 0B3H bit 4
This bit is bit 4 First User Options word - Graphics Mode Reverse Video (CRT)
Panel Control 2 (PNLCTLII) Index 0D5H bit 3
Enables/disables graphics reverse video.

REMARKS: Determines if graphics modes are displayed in reverse video or not. If a request for reverse video is issued and the current mode is a graphics mode, reverse video takes effect immediately. If the current mode is a text mode, reverse video takes effect when the mode is changed to a graphics mode.

NOTE: In LCD modes, if a frame color was explicitly set using the Set Frame Color function (Int 10, AH=12, BL=8A), changing from or to reverse video will cause the frame color to be 'reversed' also.

SYSTEM DEFAULT: LCD - Enabled
CRT - Disabled

Appendix A VGA Analysis and Verification

(This page intentionally left almost blank)

APPENDIX A
VGA ANALYSIS AND VERIFICATION

The following sections describe the proposed verification plan for the Extensible VGA. The verification is done using the GSCRIPT utility developed by Phoenix. GSCRIPT is a tool for modifying and/or watching the environment before and after an interrupt call.

A.1 Theory

For the purpose of this discussion PC BIOS interrupt services are treated as black boxes - although the data environment can be observed before and after an interrupt call, the internal workings of the BIOS as it services the interrupt cannot be watched.

For the purpose of verifying compatibility these black boxes are examined as follows:

Data in the environment are set up and a BIOS interrupt is invoked, affecting the data environent of the caller. The data environment input to the interrupt can be any/all of the following data elements:

Processor Registers	AX,BX,...,BP
Mother Board Memory	-Segment 40h
	-Save Tables
	-User Defined Tables
	-etc.
Adapter Registers	
Adapter Memory	

After a BIOS interrupt call is complete any part of the data environment might be changed, depending on the service invoked.

Interrrupt compatibility between two systems exists if for every possible input condition they both produce the exactly same output condition.

Interrupt compatibility between two systems is verified by making calls to both BIOSes with exactly the same input data (registers, memory. etc.) and then verifying that both produce exactly the same effect for a set of input conditions. This set of input conditions should cover a large number of BIOS calls which are within the defined bounds of legal requests as well as a fair number of calls which are outside the defined boundaries of normal operation. In this manner is is possible to verify that a given BIOS is compatible with another not ony under normal operating conditions, but also under undefined conditions.

Once a set of test cases which encompass the full range of input conditions is established, verification of functional compatibility can begin At this point verifying compatibility between two BIOSes becomes a simple three step process:

1. Run the test cases on one BIOS and collect the results.
2. Run the test cases on the other BIOS and collect the results.
3. Compare the results.

If the comparision finds no functional differences, then the two BIOSes are compatible.

A.2 Operation

Testing for complete compatibility involves running a large number of tests on both BIOSes under consideration and then comparing the results for functional differences. In the interest of conserving person hours the test process is automated as much as possible. This process of running tests and comparing results requires two tools - a program to run the tests and a program to compare the results. As of this writing we have the program to run the tests, GSCRIPT.

The program GSCRIPT takes three command line arguments - an initialization file, an script file, and a name for the output file. The initialization file contains information about which data elements are looked at during test execution and whether to report the value of any given data element after every BIOS call or only if it has changed. The script file contains information about actually running the test - what values to put in which data elements, and which interrupt calls to make when. It is also possible in the script file to instruct GSCRIPT about which data elements to report on. The output file name is simply the desired name for the file where GSCRIPT dumps its results.

When testing for compatibility it is important to use a robust set of test cases which encompass the full range of input conditions. This set of test cases is bound to be large and, unless it is dealt with in a systematic and organized fashion, completely unmanagible.

Critical to managibility is the concept of input data hierarchy. For any given BIOS call there are one or more input data elements which have an effect on the output data. Of these input data, some have a greater effect than others, and are therefore higher on the input data hierarchy. For example, in the video BIOS world there is a variable in memory at location 40:49 - Current Mode Number - which has an effect on the functionality of every video BIOS call. This scope of effect puts 40:49 at the top of the input data hierarchy. As an example of lesser effect there is in the video BIOS world a bit in memory, bit 0 at 40:87, which indicates whether or not cursor emulation is enabled. This bit contributes to the calcuation of the start and ending lines of the alphanumeric cursor. Not very many functions care about the state of this bit. Bit 0 of 40:87 is close to the bottom of the input data hierarchy.

This concept of hierarchy of input data effect is instrumental in any discussion of how to create a managible input data set.

First, the ideal approach. For any given BIOS call there are a finite number, X, of input data which have an effect on the output data. Ideally X-1 of the input data is kept constant while changing a single input datum between BIOS calls. After making BIOS calls with all of the values in the range of the single changing datum, one of the other data may be changed which were previously held constant. At this point we can begin again to cycle through all of the values in the range of the single changing datum. In order to keep things simple it is best to change those input data at the top of the hierarchy as seldom as possible.

As an example, let's consider a test for write character at cursor. This function allows one to specify at which video page to write a character. Depending upon the current mode it is possible to write to any one of as many as eight pages. For the sake of discussion we will consider this function to have three input data - video mode number, video page number, and cursor location. In this example mode number is highest in the hierarchy and cursor location is lowest. Accordingly, the mode number and page number would be set to the first values in their test range and then left constant while changing the cursor position, the lowest in the hierarchy, between BIOS calls. This would continue until all of the values in the test range of cursor position were exausted. At this point the page number would be changed, the next lowest in the hierarchy, to the next value in its test range and cycle once again through all the values for cursor position.

This cycling of values continues until BIOS calls for all possible combinations of values in the test ranges of page number and cursor position have been made. Once all of those combinations are tested, the video mode number can be changed, highest in the hierarchy, using the set mode function and start cycling cursor position and page number all over again.

The main point of all this cycling through values is NEVER change more than one input variable at a time, ALWAYS be consistant about how you change groups of interdependant input variables, and BE CERTAIN to change the highest item in the hierarchy at LEAST OFTEN. The benefit to organizing tests in this fashion is that test files are easier to create and manage, and the result files are easier to interpret.

Placing all test cases for verifying complete compatibility in a single script file is not a viable option because it would take too long to run and would not allow one to test an individual aspect of one function by itself. The alternative to one huge script file is a number of smaller script files. The main problem with having more than one script file is keeping them organized in a managable fashion.

The first level of organization should be by function. As an example, in the VGA video BIOS world the functions one can request are numbered 0 through 1Ch. A person creating test scripts should create a directory for each function to be tested and place each function's scripts in it's directory.

Just as it is not practical to create one huge script for a given BIOS it is not practical to create one big script for a given function. It is easier to break the testing into a number of levels and create a test script for each level. In testing for compatibility there are three levels of testing:

1. Desired results (e.g. was the character really written) - This level of testing should test normal operating conditions.
2. Undefined side-effects - This level of testing should test operation under undefined/non-standard/out of bounds conditions.
3. Side effects - are any occuring? This level should examine the entire environment for side-effects/changes.

Level 1 testing involves looking at the place in the data environment where the BIOS function is expected to do its main work before and after the BIOS call to verify that the work got done.

Level 2 testing involves making BIOS calls with input parameters that are probably not what the BIOS designers had in mind when they put it together.

Level 3 testing involves making complete dumps of the entire data environment before and after BIOS calls to keep track of side effects. The functionality tested by level three scripts is the same as that tested by level one scripts. The only difference between level one scripts and level three scripts is that level one scripts report changes in the entire data environment while level three scripts report the contents of the entire data environment, regardless of changes.

In all cases it is important to compare the results from our BIOS with the results from IBM's to make sure our's is compatible.

A.3 Interrupt 10H

Each Interrupt will be verified using one or more GSCRIPT script files.

A.3.1 Set Video Mode - Int 10H, AH=00

S0000A0.in This script requests a set mode for all legal modes. To get monochrome modes it is necessary to change DEVFLAG 40:10 bits 4-5 to indicate a mono display is installed. Because the purpose of function zero is to set up the data environment, the entire data environment is dumped before and after calls to set mode.

S0000B0.in Try to set undefined/illegal modes. Try to set color modes when DEVFLAG says a mono display is installed and vice versa. Also call setmode with all the various override character sets, number of lines etc. set to a number of combinations.

S0000C0.in Due to the nature of this function and S0000A0.in, this script may not be needed. Look into it.

A.3.2 Set Cursor Size - Int 10H, AH=01

S0100A0.in This script tests set cursor size in all text modes. Cursor size is set to underbar, overbar, halfblock and fullblock in both emulation and non-emulation modes. Emulation mode is on when 40:87[0] = 0.

S0100B0.in This script tests out of bounds and undefined conditions such as setting cursor size while in a graphics mode, using values appropriate for non-emulation while cursor emulation is on etc.

S0100C0.in This file should be like S0100A0.in, but with all the data environment being examined for side effects.

A.3.3 Set Cursor Position - Int 10H, AH=02

S0200A0.in This script tests set cursor location in all modes. Processor and CRTC registers and segment 40h are checked for differences. Test cases include setting cursor location to all four corners of the screen. These test cases are tried on all valid pages.

S0200B0.in This script tests set cursor location in all modes. Processor and CRTC registers and segment 40h are checked for differences. Cases tested include setting cursor of a non-current page, setting current page's cursor to point to another page, setting current page's cursor to point to a nonexistant page by specifying bad page in BH and by specifying out of bounds location in DX.

S0200C0.in This file is like S0200A0.in, but with all the data environment being examined for side effects.

A.3.4 Get Cursor Status - Int 10H, AH=03

S0300A0.in This function is tested by first using GSCRIPT to set segment 40h (40:50-5E) and then calling int 10 function 03 to retrieve the values put there. All pages in all modes are tested. Testing always reads the current page's cursor location. Processor and CRTC registers as well as segment 40h are checked for differences.

S0300B0.in This function is tested by first using GSCRIPT to set the variable CURPOS in segment

40h (40:50-5E) and then calling int 10 function 03 to retrieve the values put there. All pages in all modes are tested. This script concentrates on non-current and invalid pages. Processor and CRTC registers as well as segment 40h are checked for differences.

S0300C0.in This file should be like S0300A0.in, but with all the data environment being examined for side effects.

A.3.5 Read Light Pen Position - Int 10H AH=04

This function is not supported on the VGA adapter.

A.3.6 Select New Video Page - Int 10H, AH=05

S0500A0.in For this function there is a different cursor position for each page to see how CRTC registers are set. Test cases include all valid pages and modes. Processor and CRTC registers as well as segment 40h are examined for differences.

S0500B0.in For this function there is a different cursor position for each page to see how CRTC registers are set. This script tests for dependencies on CRT_COLS (40:4a) and CRT_PLEN (40:4c) by dividing the values held there by two and calling function 05. Processor and CRTC registers as well as segment 40h are examined for differences.

S0500C0.in This file should be like S0500A0.in, but with all the data environment being examined for side effects.

A.3.7 Scroll Active Page Up - Int 10H, AH=06

S0600A0.in This function is tested by writing a pattern to the regen buffer with GSCRIPT's FILL command, invoking the service and then using the DUMP command to verify that the pattern was shifted appropriately. All pages in all modes should be tested. at least six different kinds of boxes should be scrolled - full screen, each of the four corners and a box in the middle of the screen. Each box should get scrolled three different ways - by one line, by zero lines (scroll clear), and by as many lines as the box is big (should be the same as scroll clear) In addition to DUMPing the regen buffer to see if the scroll happened, we should check processor and CRTC registers and segment 40h for changes.

S0600B0.in In this script we use the regen buffer FILL and DUMP commands from the script above but the actual scroll requests are invalid - top of box is lower on screen than bottom, left side of box is farther right than right side, etc. In addition to DUMPing the regen buffer to see if the scroll happened, we check processor and CRTC registers and segment 40h for changes.

S0600C0.in This script tests for CRT_COLS (40:4A) dependencies by dividing the value found there by 2. One or two pages in each mode are tested in the manner used by S0600A0.IN. Processor and VGA registers are checked for changes.

S0600D0.in This script tests for CRT_PLEN (40:4C) dependencies by dividing the value found there by 2. One or two pages in each mode are tested in the manner used by S0600A0.IN. Processor and VGA registers are checked for changes.

S0600E0.in This script tests for CRT_POFF (40:4E) dependencies by dividing the value found there by 2. One or two pages in each mode are tested in the manner used by S0600A0.IN. Processor and VGA registers are checked for changes.

S0600F0.in This script tests for BYTESCHR (40:85) dependencies by dividing the value found there by 2. One or two pages in each mode are tested in the manner used by S0600A0.IN. Processor and VGA registers are checked for changes.

S0600G0.in This file should be like S0600A0.in, but with all the data environment being examined for side effects.

A.3.8 Scroll Active Page Down - Int 10H, AH=07

S0700A0.in This function is tested by writing a pattern to the regen buffer with GSCRIPT's FILL command, invoking the service and then using the DUMP command to verify that the pattern was shifted appropriately. All pages in all modes should be tested. at least six different kinds of boxes should be scrolled - full screen, each of the four corners and a box in the middle of the screen. Each box should get scrolled three different ways - by one line, by zero lines (scroll clear), and by as many lines as the box is big (should be the same as scroll clear) In addition to DUMPing the regen buffer to see if the scroll happened, we should check processor and CRTC registers and segment 40h for changes.

S0700B0.in In this script we the regen buffer FILL and DUMP commands from the script above but the actual scroll requests are invalid - top of box is lower on screen than bottom, left side of box is farther right than right side, etc. In addition to DUMPing the regen buffer to see if the scroll happened, we check processor and CRTC registers and segment 40h for changes.

S0700C0.in This script tests for CRT_COLS (40:4A) dependencies by dividing the value found there by 2. One or two pages in each mode are tested in the manner used by S0700A0.IN. Processor and VGA registers are checked for changes.

S0700D0.in This script tests for CRT_PLEN (40:4C) dependencies by dividing the value found there by 2. One or two pages in each mode are tested in the manner used by S0700A0.IN. Processor and VGA registers are checked for changes.

S0700E0.in This script tests for CRT_POFF (40:4E) dependencies by dividing the value found there by 2. One or two pages in each mode are tested in the manner used by S0700A0.IN. Processor and VGA registers are checked for changes.

S0700F0.in This script tests for BYTESCHR (40:85) dependencies by dividing the value found there by 2. One or two pages in each mode are tested in the manner used by S0700A0.IN. Processor and VGA registers are checked for changes.

S0700G0.in This file should be like S0700A0.in, but with all the data environment being examined for side effects.

A.3.9 Read Character and Attribute at Cursor - Int 10H, AH=08

S0800A0.in The script for this function uses FILL to load characters into the regen buffer before reading them back. That is not feasable for graphics modes in which case function 9 is used. The script puts a different character at all four corners of every page and then reads it back using function 08h for all modes. This script tests every page while it is not the active page. Instead of using function 02h to set the cursor between calls to function 08h, the cursor position variable is changed at 40:50-5E.

S0800B0.in The script for this function should use FILL to load characters into the regen buffer before reading them back. That may not be feasable for graphics modes but it should definitely be done for the text modes. The script should put a different character at all four corners and the middle of every page and then read it back using function 08h for all modes. In this script test every page while it is not the active page. Instead of using function 02h to set the cursor between calls to function 08h, it changes the cursor position variable at 40:50-5E.

S0800C0.in This script tests for CRT_COLS(40:4a) dependencies.

S0800D0.in This script tests for CRT_PLEN(40:4c) dependencies.

S0800E0.in This script tests for BYTESCHR(40:85) dependencies.

S0800F0.in This file should be like S0800A0.in, but with all the data environment being examined for side effects.

A.3.10 Write Character and Attribute at Cursor - Int 10H, AH=09

S0900A0.in Test all legal pages in all modes, always writing to the current page. Write three characters to all four corners of screen. Use ICE probe and SEEREGEN macro to verify write. Write to current page with CX set so that the characters write past the end of line/end of screen. Make special note of what happens in this case - it is a big compatibility issue. Write different attributes. Check processor and CRTC registers as well as segment 40h variables for differences.

S0900B0.in Test for DEVFLAG (40:10) dependencies by setting bits 4 and 5 to each of the four possible values and calling function 9.

S0900C0.in Test for CRT_COLS (40:4A) dependencies by dividing contents of 40:4A by 2 and calling function 9.

S0900D0.in Test for CRT_PLEN (40:4C) dependencies by dividing contents of 40:4C by 2 and calling function 9.

S0900E0.in Test all pages in all modes, writing to non-current pages by calling function with BH <> ACTIVPAGE Write to invalid pages. Write a character to all four corners of screen. Use ICE probe SEEREGEN macro to verify write. Write different attributes. Check processor and CRTC registers as well as segment 40h variables for differences.

S0900f0.in This file is like S0900A0.in, but with all the data environment being examined for side effects.

A.3.11 Write Character at Cursor - Int 10H, AH=0A

S0A00A0.in Test all legal pages in all modes, always writing to the current page. Write three characters to all four corners of screen. Use ICE probe and SEEREGEN macro to verify write. Write to current page with CX set so that the characters write past the end of line/end of screen. Make special note of what happens in this case - it is a big compatibility issue. Write different attributes. Check processor and CRTC registers as well as segment 40h variables for differences.

S0A00B0.in Test for DEVFLAG (40:10) dependencies by setting bits 4 and 5 to each of the four possible values and calling function 9.

S0A00C0.in Test for CRT_COLS (40:4A) dependencies by dividing contents of 40:4A by 2 and calling function 9.

S0A00D0.in Test for CRT_PLEN (40:4C) dependencies by dividing contents of 40:4C by 2 and calling function 9.

S0A00E0.in Test all pages in all modes, writing to non-current pages by calling function with BH <> ACTIVPAGE Write to invalid pages. Write a character to all four corners of screen. Use ICE probe SEEREGEN macro to verify write. Write different attributes. Check processor and CRTC registers as well as segment 40h variables for differences.

S0A00f0.in This file should be like S0900A0.in, but with all the data environment being examined for side effects.

A.3.12 Set CGA Color Palette - Int 10H, AH=0B

S0B00A0.in Test sub-function 0 (BH = 0) in all graphics modes. Test with all legal values in BL (0-31). Check processor, attribute controller and CRTC registers as well as segment 40h variables for differences. In CGA hardware emulation modes check the CGA COLOR register at port 3D9h for changes. Test sub-function 1 (BH = 1) in all graphics modes. Test with all legal values in BL (0,1). Check processor, attribute controller and CRTC registers as well as segment 40h variables for differences. In CGA hardware emulation modes check the CGA COLOR register at port 3D9h for changes.

S0B00B0.in Test both sub-functions in all modes including text. In graphics modes concentrate on out of bounds values for register BL. Check processor, attribute controller and CRTC registers as well as segment 40h variables for differences. In CGA hardware emulation modes check the CGA COLOR register at port 3D9h for changes.

S0B00C0.in This file should be like S0B00A0.in, but with all the data environment being examined for side effects.

A.3.13 Write Pixel to Screen - Int 10H, AH=0C

S0C00A0.in Test all legal pages in all modes, always writing to the current page. Write a dot to all four corners of screen. Use Ice probe and SEEREGEN macro to verify write. Try all legal color values. Check processor and CRTC registers as well as segment 40h variables for differences.

S0C00B0.in Test all pages in all modes, writing to non-current pages by calling function with CX and/or DX = a value past the bounds of the current page. Write to invalid pages. Write a dot to all four corners of screen. Use Ice probe and SEEREGEN macro to verify write. Test color values. Check processor and CRTC registers as well as segment 40h variables for differences.

S0C00C0.in This file should be like S0A00A0.in, but with all the data environment being examined for side effects.

A.3.14 Read Pixel - Int 10H, AH=0D

S0D00A0.in The script for this function should use FILL to load dots into the regen buffer before reading them back. The script should put a different dot at all four corners of every page and then read it back using function 0Dh for all modes. In this script test every page while it is the active page.

S0D00B0.in The script for this function should use FILL to load dots into the regen buffer before reading them back. The script should put a different dot at all four corners and the middle of every page and then read it back using function 0Dh for all modes. In this script test every page while it is not the active page with a number not equal to the current page in BX and/or DX & CX pointing off the end of the page.

S0D00C0.in This file should be like S0D00A0.in, but with all the data environment being examined for side effects.

A.3.15 Write Character in TTY Mode - Int 10H, AH=0E

S0E00A0.in Test all legal pages in all modes, always writing to the current page. Write a character to all four corners of screen. Use ICE probe and SEEREGEN macro to verify write. Write to current page with CX set so that the characters write past the end of line/end of screen. Make special note of what happens in this case - it is a big compatibility issue. Write control characters BS,BELL,CR,LF. Check processor and CRTC registers as well as segment 40h variables for differences.

S0E00B0.in Test for DEVFLAG (40:10) dependencies by setting bits 4 and 5 to each of the four possible values and calling function 9.

S0E00C0.in Test for CRT_COLS (40:4A) dependencies by dividing contents of 40:4A by 2 and calling function 9.

S0E00D0.in Test for CRT_PLEN (40:4C) dependencies by dividing contents of 40:4C by 2 and calling function 9.

S0E00E0.in Test all pages in all modes, writing to non-current pages by calling function with CURPOSn past end of page. Write a character to all four corners of screen. Use ICE probe SEEREGEN macro to verify write. Write different attributes. Check processor and CRTC registers as well as segment 40h variables for differences.

S0E00f0.in This file should be like S0900A0.in, but with all the data environment being examined for side effects.

S0E00C0.in

A.3.16 Get Current Video State - Int 10H, AH=0F

S0F00A0.in This file would best be written as a part of S0500A0.in, making a call to function 0Fh after every call to function 05h.

S0F00B0.in This file would best be written as a part of S0500B0.in, making a call to function 0Fh after every call to function 05h.

S0F00C0.in

A.3.17 Set Palette Registers - Int 10H, AH=10

S1000A0.in This script uses four files for the attribute controller and four files for the DAC. These files are loaded into memory using the BUFF command so that the update palette registers and update block of DAC registers subfunctions have tables to get values from when updating those registers. The files contain tables which will set all the registers involved to 00h,55h, AAh, and FFh. The basic idea of this script is to set every register to 00h, 55h, AAh, and FFh using every subfunction that can be used to set them. After the registers are set to a given value by a given subfunction, they are read back using all of the appropriate subfunctions. After every call the attribute controller,DAC, parameter save area and user palette profile are checked for changes. The processor registers and segment 40h variables are also checked for changes.

S1000B0.in
S1000C0.in

A.3.18 Character Generator - Int 10H, AH=11

S1100A0.in This scripts uses three files with font definitions in them-one each for 8X8, 8X14 and 8X16 character sets. For each text mode the number of lines is set to each possible value and the appropriate sized font loaded. All the RAM banks (0-7) are loaded using the subfunctions to load a user defined font, load a ROM font, and load a ROM font and program the CRTC. Only the currently active bank is loaded when subfunctions 10h,11h,12h, and 14h are used. All 8 RAM banks are selected as active. One at a time, of course. In each graphics mode, all reasonable combinations of font size and rows per screen are loaded. After each load font subfunction call is made, a call to get current font info (AX=1130h) is made. After each call the processor registers, CRTC, sequencer, segment 40h variables and interrupt vectors 1fh and 43h are checked for changes.

S1100B0.in This scripts uses three files with font definitions in them one each for 8X8, 8X14 and 8X16 character sets. In text modes graphics fonts are loaded and in graphics modes text fonts are loaded. In text modes the subfunctions to load a font and reprogram the CRTC are called to load a font into a non-active bank. In graphics modes, unreasonable combinations of font size and rows per screen are used. (E.G. load an 8X16 font and say # rows = 43.) After each load font subfunction call is made, a call to get current font info (AX=1130h) is made. After each call the processor registers, CRTC, sequencer, segment 40h variables and interrupt vectors 1fh and 43h are checked for changes.

S1100C0.in

A.3.19 Alternate Select - Int 10H, AH=12

S1200A0.in In this script, all of function 12h's subfunctions are tested, except those which support display switching. PS/2 display switching support (subfunction 35h) is tested as part of the scripts to test function 1Ah. All others subfunctions are tested in this script. Testing consists of calling each subfunction with all defined values of input parameters while checking segment 40h variables and VGA registers for change. When testing subfunction 32h, CPU access to RAM, the Video System Enable register at port 3C3h is checked for changes.

S1200B0.in This script tests all of the subfunctions tested by S1200A0.in, but with undefined input values. This script's main purpose is to examine bounds checking functionality.

S1200C0.in

A.3.20 Display String - Int 10H, AH=13

S1300A0.in Have two character strings - one with embedded attributes and one without. Use these two strings to test all four sub-functions. Both strings should include the control characters CR, LF, BS and BELL. Write to all valid pages in all modes. Always write to current page. Check processor and CRTC registers as well as segment 40h variables for differences.

S1300B0.in Have two character strings - one with embedded attributes and one without. Use these two strings to test all four sub-functions. Both strings should include the control characters CR, LF, BS and BELL. Write to all pages in all modes. Write to some invalid pages. Try writting to non-current pages. Write past end of line and end of screen. Check processor and CRTC registers as well as segment 40h variables for differences.

S1300C0.in

A.3.21 Get/Set Video Display Combination Codes - Int 10H, AH=1A

S1A00A0.in This script is best run with more than one video display adapter installed. This test should be run with all possible display combinations installed: Query what is the current display combination, swap active and inactive displays, and query again. repeat the test to return to original configuration. This script also tests function 12h subfunction 35h.

S1A00B0.in This script is best run with more than one video display adapter installed. This test should be run with all possible display combinations installed. Query what is the current display combination, and try to make an uninstalled adaper active. Try for all uninstalled combinations. This script also tests function 12h subfunction 35h.

S1A00C0.in This file should be like S1A00A0.in, but with all the data environment being examined for side effects.

A.3.22 Get Functionality/State Information - Int 10H, AH=1B

S1B00A0.in Perform these tests for all modes. Allocate a 64 byte buffer pointed to by ES:DI and call function 1Bh, then DUMP the buffer.

S1B00B0.in Make this script like S1B00A0.in, but put a non-zero value in BX.

S1B00C0.in This file should be like S1B00A0.in, but with all the data environment being examined for side effects.

A.3.23 Save/Restore Video State

S1C00A0.in Perform these tests for all modes. For each type of save request buffer size, allocate a buffer and then save the state, change the data environment coresponding to the type of save performed, and restore the state. Look at the contents of the buffer after the save. Compare data environment before save and after restore for differences.

S1C00B0.in Perform save/restore where save is of one type and restore is of another.

S1C00C0.in This file should be like S1C00A0.in, but with all the data environment being examined for side effects.

A.4 Application Verification

Application Verification includes, but is not limited to, the following:

- PC Tech Journal System Benchmarks V1.0, Ziff Communications Co., 1988
- PC Magazine Laboratory Benchmark Series Release 5.0, Ziff-Davis Corp., 1989
- Power Meter V1.5, The Database Group Inc., 1988
- Microsoft Flight Simulator V3.0, Microsoft Corp.
- Splash, Spinmaker Software Corp., 1988
- Tetris, NEXA Corp.
- Microsoft Windows, Microsoft Corp., 1987
- VGAHDS - PS/2 Video Graphics Array Hardware Test V1.0, Paradise Systems Inc (Western Digital Corp.), 1987
- Fantasy Land, IBM Corp., 1984
- PC Paint V2.0
- Norton Utilities SI V4.5, Peter Norton, 1987
- QA Plus V3.11, Diagsoft

INDEX