

**CMOS  
BiCMOS**

# **CMOS BiCMOS DATA BOOK**



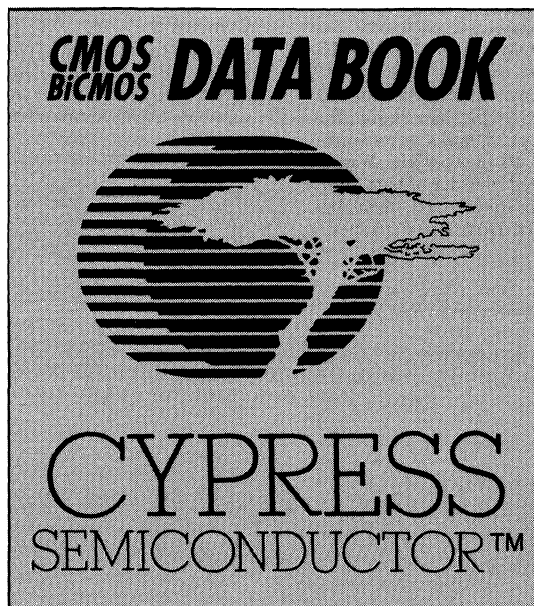
**CYPRESS  
SEMICONDUCTOR**

**TTL ECL**

**SRAMS  
PROMS  
EPLD  
LOGIC  
RISC**

**CYPRESS  
SEMICONDUCTOR**





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## How To Use This Book

This book has been organized by product type, beginning with Product Information. The products then follow, beginning with SRAMs, then PROMs, EPLDs, LOGIC (FIFO products are included in this section), RISC, Modules, and ECL. A section containing military information is next, followed by the BridgeMOS™ product family, the Cypress programming board, QuickPro, and Cypress' programmable logic design tool, the PLD ToolKit. Within each section, data sheets are arranged in order of part number. Quality and Reliability aspects follow next, then Application Briefs, and finally Thermal Data and Packages.

A Numeric Device Index is included after the Table of Contents that identifies products by numeric order, rather than by device type. To further help you in identifying parts, a Product Line Cross Reference is in the Product Information section. It can be used to find the Cypress part number that is comparable to another manufacturer's part number.

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## Cypress Semiconductor Background

Cypress Semiconductor was founded in April 1983 with the stated goal of serving the high performance semiconductor market. This market is served by producing the highest performance integrated circuits using state-of-the-art processes and circuit design. Cypress is a complete semiconductor manufacturer, performing its own process development, circuit design, wafer fabrication, assembly, and test. The company went public in May 1986 and was listed on the New York Stock Exchange in October 1988.

The initial semiconductor process, a CMOS process employing 1.2 micron geometries, was introduced in March 1984. This process is used in the manufacturing of Static RAMs and Logic circuits. In the third quarter of 1984, a 1.2 micron CMOS EPROM process was introduced for the production of programmable products. At the time of introduction, these processes were the most advanced production processes in the industry. Following the 1.2 micron processes, a 0.8 micron CMOS SRAM process was implemented in the first quarter of 1986, and a 0.8 micron EPROM process in the third quarter of 1987.

In keeping with the strategy of serving the high performance markets with state-of-the-art integrated circuits, Cypress will introduce two new processes in 1989. These will be a bipolar submicron process, targeted for ECL circuits, and a BiCMOS process to be used for most types of TTL and ECL circuits.

The circuit design technology used by Cypress is also state-of-the-art. This design technology, along with advanced process technology, allows Cypress to introduce the fastest, highest performance circuits in the industry. Cypress' products fall into seven families: high speed Static RAMs, PROMS, Erasable Programmable Logic Devices, Logic, RISC microprocessors, ECL, and module products. Members of the Static RAM family include devices in densities of 64 bits to 256K bits, and performance from 7 ns to 35 ns. The various organizations, 16 x 4, 256 x 4 through 256K x 1, 32K x 8, and 64K x 4, provide optimal solutions for applications such as large mainframes, high-speed controllers, communications, and graphics display.

Cypress' programmable products consist of high speed CMOS PROMs and Erasable Programmable Logic Devices (EPLDs), both employing an EPROM programming element. Like the high speed Static RAM family, these products are the natural choice to replace older devices because they provide superior performance at one half of the power consumption. PROM densities range from 4K to 256K bits in byte wide organization. EPLD products range from 20-pins to 68-pins with performance as fast as 12 ns. To support new programmable products, Cypress introduced the QuickPro™ programming system (CY3000) for PLDs and PROMs, and the PLD ToolKit for PLDs. QuickPro is a development tool which includes a single, IBM PC® compatible add-on board, and a software utility program. The PLD ToolKit is a software design tool that assembles and simulates logic functions, generates JEDEC files, and reverse assembles to create source files. Both QuickPro and

the PLD ToolKit software are updated via floppy disk, thereby allowing quick support of all Cypress programmable products.

Logic products include circuits such as 4-bit and 16-bit slices, 16 x 16 multipliers, and 16-bit microprogrammable ALUs, as well as a family of FIFOs that range from 64 x 4 to 2048 x 9. FIFOs provide the interface between digital information paths of widely varying speeds. This allows the information source to operate at its own intrinsic speed while the results may be processed or distributed at a speed commensurate with need.

Until 1988, all Cypress products were TTL I/O compatible. In 1989, Cypress will introduce ECL products having access times (propagation delays) of less than 3 ns in either of the popular I/O configurations, 100K or 10K/10KH. ECL RAMs include 256 x 4 and 1K x 4 RAM families with balanced read/write cycles. The ECL PLDs are combinatorial 16P8 and 16P4 devices that can be programmed on QuickPro and other commercially available programming tools. Both the RAMs and PLDs are offered in low power versions, reducing operating power by 30 to 40 percent, while achieving 5 ns access time (RAM) and 6 ns t<sub>pp</sub> (PLD).

The module family consists of both standard and custom modules incorporating circuits from the other six product families. This capability provides a fast, low risk solution for designs requiring the ultimate in system performance and density. Several module configurations are available depending on height and board real estate constraints. Modules include Single-In-Line, Dual-In-Line, Dual Single-In-Line, Vertical Dual-In-Line, Quad-In-Line, and (Staggered) Zig-Zag-In-Line packages.

Cypress' CY7C600 family of RISC microprocessor products provides state-of-the-art high performance computing for applications ranging from UNIX-based business computers and workstations to embedded controls. Based on the SPARC™ RISC architecture, the family provides a complete solution with Integer Unit (IU), Floating-Point Unit (FPU), Cache Control and Memory Management Unit (CMU) and Cache RAMs (CRAMs). The family is functionally partitioned to provide a range of features, performance, and price to suit each type of application.

Situated in California's Silicon Valley (San Jose) and Round Rock (Austin), Texas, Cypress houses R&D, design, wafer fabrication, assembly, and administration. The facilities are designed to the most demanding technical and environmental specifications in the industry. At the Texas facility, the entire wafer fabrication area is specified to be a Class 1 environment. This means that the ambient air has less than 1 particle of greater than 0.2 microns in diameter per cubic foot of air. Other environmental considerations are carefully insured: temperature is controlled to a ±0.2 degree Fahrenheit tolerance; filtered air is completely exchanged more than 10 times each minute throughout the fab; and critical equipment is situated on isolated slabs to minimize vibration.

## Cypress Semiconductor Background (Continued)

Attention to assembly is equally as critical. Cypress assembles and tests 55 packages in the United States at its San Jose, California, plant. Assembly is completed in a clean room until the silicon die is sealed in a package. Lead frames are handled in carriers or cassettes through the entire operation. Automated robots remove and replace parts into cassettes. Using sophisticated automated equipment, parts are assembled and tested in less than five days. The Cypress assembly line is the most flexible, automated line in the United States.

The Cypress motto has always been "only the best—the best facilities, the best equipment, the best employees . . . all striving to make the best CMOS, BiCMOS and bipolar products."

## Cypress Process Technology

In the last decade, there has been a tremendous need for high performance semiconductor products manufactured with a balance of SPEED, RELIABILITY, and POWER. Cypress Semiconductor has overcome the classically held perceptions that CMOS is a moderate performance technology.

Cypress initially introduced a 1.2 micron "N" well technology with double layer poly, and a single layer metal. The process employs lightly doped extensions of the heavily doped source and drain regions for both "N" and "P" channel transistors for significant improvement in gate delays. Further improvements in performance, through the use of substrate bias techniques, have added the benefit of eliminating the input and output latchup characteristics associated with the older CMOS technologies.

Cypress pushed process development to new limits in the area of PROMs (Programmable Read Only Memory) and EPLDs (Eraseable Programmable Logic Devices). Both PROMs and EPLDs have existed since the early 1970s in a bipolar process which employed various fuse technologies and was the only viable high speed non-volatile process available. Cypress PROMs and EPLDs use EPROM technology, which has also been in use in MOS (Metal Oxide Silicon) also since the early 1970s. EPROM technology has traditionally emphasized density advantages, while forsaking performance. Through improved technology, Cypress has produced the first high performance CMOS PROMs and EPLDs, replacing their bipolar counterparts.

To maintain our leadership position in CMOS Technology, Cypress has introduced a sub-micron technology into production. This process reduces the drawn channel length from the current 1.2 microns to 0.8 microns. This sub-micron breakthrough makes Cypress' CMOS one of the most advanced production processes in the world.

To further enhance the technology from the reliability direction, improvements have been incorporated in the process and design, minimizing electrostatic discharge and input signal clipping problems.

Finally, although not a requirement in the high performance arena, CMOS technology substantially reduces the

power consumption for any device. This improves reliability by allowing the device to operate at a lower die temperature. Now higher levels of integration are possible without trading performance for power. For instance, devices may now be delivered in plastic packages, without any impact on reliability.

While addressing the performance issues of CMOS technology, Cypress has not ignored the quality and reliability aspects of technology development. Rather, the traditional failure mechanisms of electrostatic discharge (ESD) and latchup have been addressed and solved through process and design technology innovation.

ESD-induced failure has been a generic problem for many high performance MOS and bipolar products. Although in its earliest years MOS technology experienced oxide reliability failures, this problem has largely been eliminated through improved oxide growth techniques and a better understanding of the ESD problem. The effort to adequately protect against ESD failures is perturbed by circuit delays associated with ESD protection circuits. Focusing on these constraints, Cypress has developed ESD protection circuitry specific to 1.2 and 0.8 micron CMOS process technology. Cypress products are designed to withstand voltage and energy levels in excess of 2001 volts and 0.4 milli-joules, more than twice the energy level specified by MIL STD 883C.

Latchup, a traditional problem with CMOS technologies, has been eliminated through the use of substrate bias generation techniques, the elimination of the "P" MOS pull-ups in the output drivers, the use of guarding structures, and care in the physical layout of the products.

Cypress has also developed additional process innovations and enhancements: the use of multi-layer metal interconnections, advanced metal deposition techniques, silicides, exclusive use of plasma for etching and ashing process steps, and 100% stepper technology with the world's most advanced equipment.

A wholly owned subsidiary of Cypress, Aspen Semiconductor, has developed both advanced Bipolar and BiCMOS technologies augmenting the capabilities of the Cypress CMOS processes. Both the new Bipolar and BiCMOS technologies are based on the Cypress 0.8 micron CMOS process for enhanced manufacturability. Like CMOS, these processes are scalable to take advantage of finer line lithography. Where speed is critical, Cypress BiCMOS allows increased transistor performance. It also allows reduced power in the non-speed critical sections of the design to optimize the speed/power balance. The Bipolar and BiCMOS processes make possible memories and logic operating up to 400 MHz. The drive to maintain process technology leadership has not stopped with the 0.8 micron devices. Cypress is developing fine line geometries beyond this to insure technology leadership in the next decade.

Cypress technologies have been carefully designed, creating products that are "only the best" in high speed, excellent reliability, and low power.

|       | Size | Organization                            | Pins | Part Number      | Speed (ns)                           | I <sub>CC</sub> /I <sub>SB</sub> /I <sub>CCDR</sub><br>(mA @ ns) | Packages   |
|-------|------|---|------|------------------|--------------------------------------|--|------------|
| SRAMS | 64   | 16 x 4—Inverting                        | 16   | CY7C189          | t <sub>AA</sub> = 15, 25             | 55 @ 25  | D, L, P    |
|       | 64   | 16 x 4—Non-Inverting                    | 16   | CY7C190          | t <sub>AA</sub> = 15, 25             | 55 @ 25  | D, L, P    |
|       | 64   | 16 x 4—Inverting                        | 16   | CY74S189         | t <sub>AA</sub> = 35                 | 90 @ 35  | D, P       |
|       | 64   | 16 x 4—Inverting                        | 16   | CY27S03A         | t <sub>AA</sub> = 25, 35             | 90 @ 25  | D, L, P    |
|       | 64   | 16 x 4—Non-Inverting                    | 16   | CY27S07A         | t <sub>AA</sub> = 25, 35             | 90 @ 25  | D, L, P    |
|       | 64   | 16 x 4—Inv. Low Power                   | 16   | CY27LS03M        | t <sub>AA</sub> = 65                 | 38 @ 65  | D, L       |
|       | 1K   | 256 x 4                                 | 22   | CY7C122          | t <sub>AA</sub> = 15, 25, 35         | 60 @ 25  | D, L, P, S |
|       | 1K   | 256 x 4                                 | 24S  | CY7C123          | t <sub>AA</sub> = 7, 9, 12           | 120 @ 7  | D, L, P, V |
|       | 1K   | 256 x 4                                 | 22   | CY9122/91L22     | t <sub>AA</sub> = 25, 35, 45         | 120 @ 25   | D, P       |
|       | 1K   | 256 x 4                                 | 22   | CY93422A/93L422A | t <sub>AA</sub> = 35, 45, 60         | 80 @ 45  | D, P, L    |
|       | 4K   | 4096 x 1—CS Power Down                  | 18   | CY7C147          | t <sub>AA</sub> = 25, 35, 45         | 80/10 @ 35   | D, L, P, S |
|       | 4K   | 4096 x 1—CS Power Down                  | 18   | CY2147/21L47     | t <sub>AA</sub> = 35, 45, 55         | 125/25 @ 35  | D, P       |
|       | 4K   | 1024 x 4—CS Power Down                  | 18   | CY7C148          | t <sub>AA</sub> = 25, 35, 45         | 80/10 @ 35   | D, L, P, S |
|       | 4K   | 1024 x 4—CS Power Down                  | 18   | CY2148/21L48     | t <sub>AA</sub> = 35, 45, 55         | 120/20 @ 35  | D, P, S    |
|       | 4K   | 1024 x 4                                | 18   | CY7C149          | t <sub>AA</sub> = 25, 35, 45         | 80 @ 35  | D, L, P, S |
|       | 4K   | 1024 x 4                                | 18   | CY2149/21L49     | t <sub>AA</sub> = 35, 45, 55         | 120 @ 35   | D, P       |
|       | 4K   | 1024 x 4—Separate I/O, Reset            | 24S  | CY7C150          | t <sub>AA</sub> = 12, 15, 25, 35     | 90 @ 12  | D, L, P, S |
|       | 8K   | 1024 x 8—Dual Port                      | 48   | CY7C130          | t <sub>AA</sub> = 25, 35, 45, 55     | 170 @ 25   | D, L, P    |
|       | 8K   | 1024 x 8—Dual Port (Slave)              | 48   | CY7C140          | t <sub>AA</sub> = 25, 35, 45, 55     | 170 @ 25   | D, L, P    |
|       | 8K   | 1024 x 8—Dual Port                      | 52   | CY7C131          | t <sub>AA</sub> = 25, 35, 45, 55     | 170 @ 25   | L, J       |
|       | 8K   | 1024 x 8—Dual Port                      | 52   | CY7C141          | t <sub>AA</sub> = 25, 35, 45, 55     | 170 @ 25   | L, J       |
|       | 16K  | 2048 x 8—CS Power Down                  | 24S  | CY7C128          | t <sub>AA</sub> = 35, 45, 55         | 90/20 @ 55   | D, L, P, V |
|       | 16K  | 2048 x 8—CS Power Down                  | 24   | CY7C128A         | t <sub>AA</sub> = 20, 25, 35, 45, 55 | 90/20 @ 55   | D, L, P, V |
|       | 16K  | 2048 x 8—CS Power Down                  | 24   | CY6116           | t <sub>AA</sub> = 35, 45, 55         | 120/20 @ 45  | D, L       |
|       | 16K  | 2048 x 8—CS Power Down                  | 24   | CY6116A          | t <sub>AA</sub> = 20, 25, 35, 45, 55 | 80/20 @ 55   | D, L       |
|       | 16K  | 2048 x 8—CS Power Down                  | 32S  | CY6117           | t <sub>AA</sub> = 35, 45, 55         | 130/20 @ 55  | L          |
|       | 16K  | 2048 x 8—CS Power Down                  | 32S  | CY6117A          | t <sub>AA</sub> = 20, 25, 35, 45, 55 | 100/20 @ 55  | L          |
|       | 16K  | 16384 x 1—CS Power Down                 | 20   | CY7C167          | t <sub>AA</sub> = 25, 35, 45         | 50/15 @ 25   | D, L, P, V |
|       | 16K  | 16384 x 1—CS Power Down                 | 20   | CY7C167A         | t <sub>AA</sub> = 20, 25, 35, 45     | 50/15 @ 45   | D, L, P, V |
|       | 16K  | 4096 x 4—CS Power Down                  | 20   | CY7C168          | t <sub>AA</sub> = 25, 35, 45         | 90/15 @ 25   | D, L, P, V |
|       | 16K  | 4096 x 4—CS Power Down                  | 20   | CY7C168A         | t <sub>AA</sub> = 20, 25, 35, 45     | 70/15 @ 45   | D, L, P, V |
|       | 16K  | 4096 x 4                                | 20   | CY7C169          | t <sub>AA</sub> = 25, 35, 40         | 90 @ 25  | D, L, P, V |
|       | 16K  | 4096 x 4                                | 20   | CY7C169A         | t <sub>AA</sub> = 20, 25, 35, 40     | 70 @ 45  | D, L, P, V |
|       | 16K  | 4096 x 4—Output Enable                  | 22S  | CY7C170          | t <sub>AA</sub> = 25, 35, 45         | 90 @ 45  | D, L, P, V |
|       | 16K  | 4096 x 4—Output Enable                  | 20   | CY7C170A         | t <sub>AA</sub> = 20, 25, 35, 45     | 90 @ 45  | D, L, P, V |
|       | 16K  | 4096 x 4—Separate I/O                   | 24S  | CY7C171          | t <sub>AA</sub> = 20, 25, 35, 45     | 90/15 @ 25   | D, L, P, V |
|       | 16K  | 4096 x 4—Separate I/O                   | 24S  | CY7C171A         | t <sub>AA</sub> = 20, 25, 35, 45     | 90 @ 45  | D, L, P, V |
|       | 16K  | 4096 x 4—Separate I/O                   | 24S  | CY7C172          | t <sub>AA</sub> = 20, 25, 35, 45     | 90/15 @ 25   | D, L, P, V |
|       | 16K  | 4096 x 4—Separate I/O                   | 24S  | CY7C172A         | t <sub>AA</sub> = 20, 25, 35, 45     | 90 @ 45  | D, L, P, V |
|       | 16K  | 2048 x 8—Dual Port                      | 48   | CY7C132          | t <sub>AA</sub> = 25, 35, 45, 55     | 170 @ 25   | D, L, P    |
|       | 16K  | 2048 x 8—Dual Port (Slave)              | 48   | CY7C142          | t <sub>AA</sub> = 25, 35, 45, 55     | 170 @ 25   | D, L, P    |
|       | 64K  | 2048 x 8                                | 52   | CY7C136          | t <sub>AA</sub> = 25, 35, 45, 55     | 170 @ 25   | L, J       |
|       | 64K  | 2048 x 8                                | 52   | CY7C146          | t <sub>AA</sub> = 25, 35, 45, 55     | 170 @ 25   | L, J       |
|       | 64K  | 8192 x 8                                | 28   | CY7C185-12       | t <sub>AA</sub> = 12, 15             | 115/50 @ 15  | D, L, P, V |
|       | 64K  | 8192 x 8                                | 28   | CY7C186-12       | t <sub>AA</sub> = 12, 15             | 115/50 @ 15  | D, L, P, V |
|       | 64K  | 8192 x 8—CS Power Down                  | 28S  | CY7C185-20       | t <sub>AA</sub> = 20, 25, 35, 45     | 100/20 @ 25  | D, L, P, V |
|       | 64K  | 8192 x 8—CS Power Down                  | 28   | CY7C186-20       | t <sub>AA</sub> = 20, 25, 35, 45     | 100/20 @ 25  | D, P       |
|       | 64K  | 16384 x 4                               | 22   | CY7C164-10       | t <sub>AA</sub> = 10, 12, 15         | 115/50 @ 15  | D, L, P, V |
|       | 64K  | 16384 x 4—CS Power Down                 | 22S  | CY7C164-20       | t <sub>AA</sub> = 20, 25, 35, 45     | 70/20 @ 25   | D, L, P, V |
|       | 64K  | 16384 x 4                               | 24   | CY7C166-10       | t <sub>AA</sub> = 10, 12, 15         | 115/50 @ 15  | D, L, P, V |
|       | 64K  | 16384 x 4—Output Enable                 | 24S  | CY7C166-20       | t <sub>AA</sub> = 20, 25, 35, 45     | 70/20 @ 25   | D, L, P, V |
|       | 64K  | 16384 x 4                               | 28   | CY7C161-10       | t <sub>AA</sub> = 10, 12, 15         | 115/50 @ 15  | D, L, P, V |
|       | 64K  | 16384 x 4                               | 28   | CY7C162-10       | t <sub>AA</sub> = 10, 12, 15         | 115/50 @ 15  | D, L, P, V |
|       | 64K  | 16384 x 4—Separate I/O                  | 28S  | CY7C161-20       | t <sub>AA</sub> = 20, 25, 35, 45     | 70/20 @ 25   | D, L, P, V |
|       | 64K  | 16384 x 4—Separate I/O                  | 28S  | CY7C162-20       | t <sub>AA</sub> = 20, 25, 35, 45     | 70/20 @ 25   | D, L, P, V |
|       | 64K  | 65536 x 1—CS Power Down                 | 22S  | CY7C187          | t <sub>AA</sub> = 20, 25, 35, 45     | 70/20 @ 25   | D, L, P, V |
|       | 128K | 8192 x 16—Addresses Latched except A-12 | 52   | CY7C183          | t <sub>AA</sub> = 25, 35, 45         | 220 @ 25   | D, J, L    |
|       | 128K | 8192 x 16—Addresses Latched             | 52   | CY7C184          | t <sub>AA</sub> = 25, 35, 45         | 220 @ 25   | D, J, L    |
|       | 256K | 16384 x 16                              | 52   | CY7C157          | t <sub>AA</sub> = 20, 24             | TBD  | J, L       |
|       | 256K | 32768 x 8—CS Power Down                 | 28   | CY7C198          | t <sub>AA</sub> = 35, 45, 55         | 110/20 @ 35  | D, P       |
|       | 256K | 32768 x 8—CS Power Down                 | 28S  | CY7C199          | t <sub>AA</sub> = 35, 45, 55         | 110/20 @ 35  | D, L, P, V |
|       | 256K | 65536 x 4—CS Power Down                 | 24S  | CY7C194          | t <sub>AA</sub> = 25, 35, 45         | 80/20 @ 25   | D, L, P, V |
|       | 256K | 65536 x 4—CS Power Down With OE         | 28S  | CY7C196          | t <sub>AA</sub> = 25, 35, 45         | 80/20 @ 25   | D, L, P, V |
|       | 256K | 65536 x 4—Separate I/O                  | 28S  | CY7C191          | t <sub>AA</sub> = 25, 35, 45         | 80/20 @ 25   | D, L, P, V |
|       | 256K | 65536 x 4—Separate I/O                  | 28S  | CY7C192          | t <sub>AA</sub> = 25, 35, 45         | 80/20 @ 25   | D, L, P, V |
|       | 256K | 262144 x 1—CS Power Down                | 24S  | CY7C197          | t <sub>AA</sub> = 25, 35, 45         | 70/20 @ 25   | D, L, P, V |

**Notes:**

The above specifications are for the commercial temperature range of 0°C to 70°C.

Military temperature range (-55°C to +125°C) product processed to MIL-STD-883 Revision C is also available. Speed and power selections may vary from those above.

Commercial grade product is available in plastic, CERDIP, or LCC. Military grade product is available in CERDIP or LCC. PLCC, SOJ, and SOIC packages are available on some products.

All power supplies are V<sub>CC</sub> = 5V ± 10%.

22S stands for 22-pin 300 mil. 24S stands for 24-pin 300 mil. 28S stands for 28-pin 300 mil.

F, K and T packages are special order only.

**Package Code:**

B = PLASTIC PIN GRID

ARRAY

D = CERDIP

F = FLATPAK

G = PIN GRID ARRAY

H = WINDOWED

HERMETIC LCC

J = PLCC

K = CERPAK

L = LCC

P = PLASTIC

Q = WINDOWED LCC

R = WINDOWED PGA

S = SOIC

T = WINDOWED CERPAK

V = SOJ

W = WINDOWED CERDIP

X = DICE

HD = HERMETIC DIP

HV = HERMETIC VERTICAL

DIP

PF = PLASTIC FLAT SIP

PS = PLASTIC SIP

PZ = PLASTIC ZIP



# Product Selection Guide (Continued)

|              | Size                    | Organization                    | Pins    | Part Number                  | Speed (ns)   | I <sub>CC</sub> /I <sub>SB</sub> /I <sub>CCDR</sub><br>(mA @ ns) | Packages         |
|--------------|-------------------------|---------------------------------|---------|------------------------------|--|--|------------------|
| <b>PROMs</b> | 4K                      | 512 x 8—Registered              | 24S     | CY7C225                      | t <sub>SA</sub> /CO = 25/12, 30/15                                       | 90   | D, L, P          |
|              | 8K                      | 1024 x 8—Registered             | 24S     | CY7C235                      | t <sub>SA</sub> /CO = 25/12, 30/15                                       | 90   | D, L, P          |
|              | 8K                      | 1024 x 8                        | 24S     | CY7C281                      | t <sub>AA</sub> = 30, 45   | 90   | D, L, P          |
|              | 8K                      | 1024 x 8                        | 24      | CY7C282                      | t <sub>AA</sub> = 30, 45   | 90   | D, L, P          |
|              | 16K                     | 2048 x 8—Registered             | 24S     | CY7C245/L                    | t <sub>SA</sub> /CO = 25/12, 35/15                                       | 100, 60  | D, L, P, Q, W, S |
|              | 16K                     | 2048 x 8—Registered             | 24S     | CY7C245A/L                   | t <sub>SA</sub> /CO = 18/12  | 60 @ 35  | D, L, P, Q, W, S |
|              | 16K                     | 2048 x 8                        | 24S     | CY7C291/L                    | t <sub>AA</sub> = 35, 50   | 90, 60   | D, L, P, Q, W, S |
|              | 16K                     | 2048 x 8                        | 24S     | CY7C291A/L                   | t <sub>AA</sub> = 25, 30, 35, 50   | 60 @ 35  | D, L, P, Q, W, S |
|              | 16K                     | 2048 x 8                        | 24      | CY7C292/L                    | t <sub>AA</sub> = 35, 50   | 90, 60   | D, P             |
|              | 16K                     | 2048 x 8—CS Power Down          | 24S     | CY7C293A/L                   | t <sub>AA</sub> = 25, 30, 35, 50   | 60/15 @ 35   | D, L, P, Q, W, S |
|              | 64K                     | 8192 x 8—CS Power Down          | 24S     | CY7C261                      | t <sub>AA</sub> = 35, 40, 45, 55   | 100/30   | D, L, P, Q, W, S |
|              | 64K                     | 8192 x 8                        | 24S     | CY7C263                      | t <sub>AA</sub> = 35, 40, 45, 55   | 100  | D, L, P, Q, W, S |
|              | 64K                     | 8192 x 8                        | 24      | CY7C264                      | t <sub>AA</sub> = 35, 40, 45, 55   | 100  | D, P             |
|              | 64K                     | 8192 x 8—Registered             | 28S     | CY7C265                      | t <sub>SA</sub> /CO = 40/20  | 80   | D, L, P, Q, W, S |
|              | 64K                     | 8192 x 8                        | 28      | CY7C266                      | t <sub>AA</sub> = 55   | 80/15  | D, L, P, Q, W    |
|              | 64K                     | 8192 x 8—Registered, Diagnostic | 28S     | CY7C269                      | t <sub>SA</sub> /CO = 40/20, 50/25                                       | 100  | D, L, P, Q, W, S |
|              | 64K                     | 8192 x 8—Registered, Diagnostic | 32      | CY7C268                      | t <sub>SA</sub> /CO = 40/20, 50/25                                       | 100  | D, L, Q, W       |
|              | 128K                    | 16384 x 8—CS Power Down         | 28S     | CY7C251                      | t <sub>AA</sub> = 45, 55, 65   | 100/30   | D, L, P, Q, W, S |
|              | 128K                    | 16384 x 8                       | 28      | CY7C254                      | t <sub>AA</sub> = 45, 55, 65   | 100  | D, P             |
|              | 256K                    | 32768 x 8—CS Power Down         | 28S     | CY7C271                      | t <sub>AA</sub> = 45, 55, 65   | 100/30   | D, L, P, Q, W, S |
| 256K         | 32768 x 8               | 28                              | CY7C274 | t <sub>AA</sub> = 45         | 120/30   | D, L, P, Q, W  |                  |
| 256K         | 32768 x 8—Registered    | 28S                             | CY7C277 | t <sub>SA</sub> /CO = 40/20  | 120/30   | D, L, P, Q, W  |                  |
| 256K         | 32768 x 8—Address Latch | 28S                             | CY7C279 | t <sub>AA</sub> = 45         | 120  | D, L, P, Q, W  |                  |
| 512K         | 65536 x 8—FCA           | 28S                             | CY7C285 | t <sub>AA</sub> /CAA = 65/30 | 180  | D, L, P, Q, W  |                  |
| 512K         | 65536 x 8—CE Power Down | 28                              | CY7C286 | t <sub>AA</sub> = 65         | 120/40   | D, L, P, Q, W  |                  |
| 512K         | 65536 x 8—Registered    | 28S                             | CY7C287 | t <sub>SA</sub> /CO = 55/20  | 180  | D, L, P, Q, W  |                  |
| 512K         | 65536 x 8—FCA           | 32S                             | CY7C289 | t <sub>AA</sub> /CA = 75/30  | 180  | D, L, P, Q, W  |                  |
| <b>PLDs</b>  | PALC20                  | 16L8                            | 20      | PALC16L8/L                   | t <sub>PD</sub> = 20   | 70, 45   | D, L, P, Q, V, W |
|              | PALC20                  | 16R8                            | 20      | PALC16R8/L                   | t <sub>S</sub> /CO = 15/12   | 70, 45   | D, L, P, Q, V, W |
|              | PALC20                  | 16R6                            | 20      | PALC16R6/L                   | t <sub>PD</sub> /S/CO = 20/20/15   | 70, 45   | D, L, P, Q, V, W |
|              | PALC20                  | 16R4                            | 20      | PALC16R4/L                   | t <sub>PD</sub> /S/CO = 20/20/15   | 70, 45   | D, L, P, Q, V, W |
|              | PLDC20                  | 18G8—Generic                    | 20      | PLDC18G8                     | t <sub>PD</sub> /S/CO = 12/12/10   | 90   | D, L, P, Q, V, W |
|              | PLDC24                  | 22V10—Macro Cell                | 24S     | PALC22V10/L                  | t <sub>PD</sub> /S/CO = 25/15/15   | 90, 55   | D, L, P, Q, W, J |
|              | PLDC24                  | 22V10—Macro Cell                | 24S     | PALC22V10B                   | t <sub>PD</sub> /S/CO = 15/10/10   | 90   | D, L, P, Q, W, J |
|              | PLDC24                  | 20G10—Generic                   | 24S     | PLDC20G10                    | t <sub>PD</sub> /S/CO = 25/15/15   | 55   | D, L, P, Q, W, J |
|              | PLDC24                  | 20G10—Generic                   | 24S     | PLDC20G10B                   | t <sub>PD</sub> /S/CO = 15/12/10   | 70   | D, L, P, Q, W, J |
|              | PLDC24                  | 20RA10—Asynchronous             | 24S     | PLDC20RA10                   | t <sub>PD</sub> /S/CO = 20/10/20   | 80   | D, L, P, Q, W, J |
|              | PLDC28                  | 7C330—State Machine             | 28S     | CY7C330                      | f <sub>MAX</sub> , t <sub>IS</sub> , t <sub>CO</sub> = 66 MHz/3 ns/12 ns | 130  | D, L, P, Q, W, J |
|              | PLDC28                  | 7C331—Asynchronous              | 28S     | CY7C331                      | t <sub>PD</sub> /S/CO = 20/12/20   | 120  | D, L, P, Q, W, J |
|              | PLDC28                  | 7C332—Combinatorial             | 28S     | CY7C332                      | t <sub>PD</sub> = 20 ns  | 120  | D, L, P, Q, W, J |
|              | PLDC28                  | 7C361—State Machine             | 28S     | CY7C361                      | f <sub>MAX</sub> /t <sub>S</sub> /t <sub>CO</sub> = 125 MHz/2 ns/12 ns   | 140  | D, L, P, Q, W, J |
|              | MAXC28                  | 7C344-32—Macro Cell             | 28S     | CY7C344                      | t <sub>PD</sub> /S/CO = TBD  | I <sub>CC</sub> = TBD  | D, L, P, Q, W, J |
|              | MAXC40                  | 7C343-64—Macro Cell             | 40/44   | CY7C343                      | t <sub>PD</sub> /S/CO = TBD  | I <sub>CC</sub> = TBD  | D, L, P, W, J, H |
|              | MAXC40                  | 7C345-128—Macro Cell            | 40/44   | CY7C345                      | t <sub>PD</sub> /S/CO = TBD  | I <sub>CC</sub> = TBD  | D, L, P, W, J, H |
|              | MAXC68                  | 7C342-128—Macro Cell            | 68      | CY7C342                      | t <sub>PD</sub> /S/CO = TBD  | I <sub>CC</sub> = TBD  | L, J, G, H, R    |
| <b>FIFOs</b> | 256                     | 64 x 4—Cascadeable              | 16      | CY3341                       | 1.2, 2 MHz   | 45   | D, P             |
|              | 256                     | 64 x 4—Cascadeable              | 16      | CY7C401                      | 5, 10, 15, 25 MHz  | 75   | D, L, P, V       |
|              | 256                     | 64 x 4—Cascadeable/OE           | 16      | CY7C403                      | 10, 15, 25 MHz   | 75   | D, L, P, V       |
|              | 320                     | 64 x 5—Cascadeable              | 18      | CY7C402                      | 5, 10, 15, 25 MHz  | 75   | D, L, P, V       |
|              | 320                     | 64 x 5—Cascadeable/OE           | 18      | CY7C404                      | 10, 15, 25 MHz   | 75   | D, L, P, V       |
|              | 512                     | 64 x 8—Cascadeable/OE           | 28S     | CY7C408A                     | 15, 25, 35 MHz   | 120  | D, L, P, V       |
|              | 576                     | 64 x 9—Cascadeable              | 28S     | CY7C409A                     | 15, 25, 35 MHz   | 120  | D, L, P, V       |
|              | 4608                    | 512 x 9—Cascadeable             | 28      | CY7C420                      | 30, 40, 65 ns  | 100  | D, P             |
|              | 4608                    | 512 x 9—Cascadeable             | 28S     | CY7C421                      | 30, 40, 65 ns  | 100  | D, J, L, P, V    |
|              | 9216                    | 1024 x 9—Cascadeable            | 28      | CY7C424                      | 30, 40, 65 ns  | 100  | D, P             |
|              | 9216                    | 1024 x 9—Cascadeable            | 28S     | CY7C425                      | 30, 40, 65 ns  | 100  | D, J, L, P       |
|              | 18432                   | 2048 x 9—Cascadeable            | 28      | CY7C428                      | 30, 40, 65 ns  | 100  | D, P             |
|              | 18432                   | 2048 x 9—Cascadeable            | 28S     | CY7C429                      | 30, 40, 65 ns  | 100  | D, J, L, P, V    |

**Notes:**

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Commercial grade product is available in plastic, CERDIP, or LCC. Military grade product is available in CERDIP or LCC. PLCC, SOJ, and SOIC packages are available on some products.

All power supplies are V<sub>CC</sub> = 5V ± 10%.

22S stands for 22-pin 300 mil. 24S stands for 24-pin 300 mil. 28S stands for 28-pin 300 mil.

F, K and T packages are special order only.

**Package Code:**

- B = PLASTIC PIN GRID ARRAY
- D = CERDIP
- F = FLATPAK
- G = PIN GRID ARRAY
- H = WINDOWED HERMETIC LCC
- J = PLCC
- K = CERPAK
- L = LCC
- P = PLASTIC
- Q = WINDOWED LCC

- R = WINDOWED PGA
- S = SOIC
- T = WINDOWED CERPAK
- V = SOJ
- W = WINDOWED CERDIP
- X = DICE
- HD = HERMETIC DIP
- HV = HERMETIC VERTICAL DIP
- PF = PLASTIC FLAT SIP
- PS = PLASTIC SIP
- PZ = PLASTIC ZIP

| Size             |  | Organization                                    | Pins    | Part Number                       | Speed (ns)                             | I <sub>CC</sub> /I <sub>SB</sub> /I <sub>CCDR</sub><br>(mA @ ns) | Packages      |
|------------------|--|---|---------|-----------------------------------|--|--|---------------|
| <b>LOGIC</b>     |  | 2901—4 Bit Slice                                | 40      | CY7C901                           | t <sub>CLK</sub> = 23, 31              | 70   | D, L, P, J    |
|                  |  | 2901—4 Bit Slice                                | 40      | CY2901                            | C                                      | 140  | D, P          |
|                  |  | 4 x 2901—16 Bit Slice                           | 64      | CY7C9101                          | t <sub>CLK</sub> = 30, 40              | 60   | D, L, P, J    |
|                  |  | 29116—16 Bit Controller                         | 52      | CY7C9115                          | t <sub>CLK</sub> = 35, 45, 53, 79, 100 | 145  | J             |
|                  |  | 29116—16 Bit Controller                         | 52      | CY7C9116                          | t <sub>CLK</sub> = 35, 45, 53, 79, 100 | 145  | D, L, G, J    |
|                  |  | 29117—16 Bit Controller                         | 68      | CY7C9117                          | t <sub>CLK</sub> = 35, 45, 53, 79, 100 | 145  | L, G, J       |
|                  |  | 2909—Sequencer                                  | 28      | CY7C909                           | t <sub>CLK</sub> = 30, 40              | 55   | D, L, P, J    |
|                  |  | 2911—Sequencer                                  | 20      | CY7C911                           | t <sub>CLK</sub> = 30, 40              | 55   | D, L, P, J    |
|                  |  | 2909—Sequencer                                  | 28      | CY2909                            | A                                      | 70   | D, P          |
|                  |  | 2911—Sequencer                                  | 20      | CY2911                            | A                                      | 70   | D, P          |
|                  |  | 2910—Controller (17 Word Stack)                 | 40      | CY7C910                           | t <sub>CLK</sub> = 40, 50, 93          | 100  | D, L, P, J    |
|                  |  | 2910—Controller (9 Word Stack)                  | 40      | CY2910                            | A                                      | 170  | D, L, P, J    |
|                  |  | 16 x 16—Multiplier                              | 64      | CY7C516                           | t <sub>MC</sub> = 38, 45, 55, 75       | 100 @ 10 MHz   | D, L, P, G, J |
|                  |  | 16 x 16—Multiplier                              | 64      | CY7C517                           | t <sub>MC</sub> = 38, 45, 55, 75       | 100 @ 10 MHz   | D, L, P, G, J |
|                  |  | 16 x 16—Multiplier/Accumulator                  | 64      | CY7C510                           | t <sub>MC</sub> = 45, 55, 65, 75       | 100 @ 10 MHz   | D, L, P, G, J |
| <b>RISC</b>      | IU   | SPARC 32 Bit Integer Unit                       | 208     | CY7C601                           | t <sub>CYC</sub> = 40, 33, 25 MHz      | 650  | G, B          |
|                  | FPC  | Floating-Point Controller                       | 281     | CY7C608                           | t <sub>CYC</sub> = 33, 25 MHz          | 600  | G             |
|                  | FPP  | Floating-Point Processor                        | 208     | CY7C609                           | t <sub>CYC</sub> = 33, 25 MHz          | 600  | G             |
|                  | FPU  | Floating-Point Unit<br>(Controller & Processor) | 299/144 | CY7C602                           | t <sub>CYC</sub> = 40, 33, 25 MHz      | 650  | G, K          |
|                  | CMU  | Cache Controlled Memory<br>Management Unit      | 207/196 | CY7C604                           | t <sub>CYC</sub> = 40, 33, 25 MHz      | 650  | G, K          |
| CMU-MP           | Cache Controller and Multiprocessing<br>Memory Management Unit | 207/196   | CY7C605 | t <sub>CYC</sub> = 40, 33, 25 MHz | 650                                    | G, K   |               |
| <b>Modules</b>   | 32K  | 1K x 32—SRAM                                    | 56      | CYM1804                           | t <sub>AA</sub> = 15, 17               | 720 @ 15   | PZ            |
|                  | 256K   | 16K x 16—SRAM (JEDEC)                           | 40      | CYM1610                           | t <sub>AA</sub> = 25, 35, 45, 50       | 330 @ 25   | HD            |
|                  | 256K   | 16K x 16—SRAM                                   | 36      | CYM1611                           | t <sub>AA</sub> = 25, 30, 35, 45       | 330 @ 25   | HV            |
|                  | 512K   | 16K x 32—SRAM                                   | 64      | CYM1821                           | t <sub>AA</sub> = 25, 35, 45           | 720 @ 25   | PZ            |
|                  | 512K   | 16K x 32—SRAM Separate I/O                      | 88      | CYM1822                           | t <sub>AA</sub> = 25, 30, 35, 45       | 720 @ 25   | HV            |
|                  | 1M   | 128K x 8—SRAM (JEDEC)                           | 32      | CYM1420                           | t <sub>AA</sub> = 45, 55               | 210 @ 45   | HD            |
|                  | 1M   | 128K x 8—SRAM (JEDEC)                           | 32      | CYM1421                           | t <sub>AA</sub> = 70, 85               | 120 @ 70   | HD            |
|                  | 1M   | 128K x 8—SRAM                                   | 30      | CYM1422                           | t <sub>AA</sub> = 35, 45, 55           | 220 @ 35   | PF, PS        |
|                  | 1M   | 64K x 16—SRAM (JEDEC)                           | 40      | CYM1620                           | t <sub>AA</sub> = 45, 55               | 340 @ 45   | HD            |
|                  | 1M   | 64K x 16—SRAM                                   | 40      | CYM1621                           | t <sub>AA</sub> = 25, 30, 35, 45       | 1250 @ 25  | HD            |
|                  | 1M   | 64K x 16—SRAM                                   | 40      | CYM1622                           | t <sub>AA</sub> = 35, 45, 55           | 400 @ 35   | HV            |
|                  | 1M   | 64K x 16—SRAM (JEDEC)                           | 40      | CYM1623                           | t <sub>AA</sub> = 70, 85, 100          | 240 @ 70   | HD            |
|                  | 1M   | 64K x 16—SRAM                                   | 40      | CYM1626                           | t <sub>AA</sub> = 30, 35, 45           | 340 @ 30   | PF, PS        |
|                  | 2M   | 64K x 32—SRAM                                   | 60      | CYM1830                           | t <sub>AA</sub> = 35, 45, 55           | 550 @ 45   | HD            |
|                  | 2M   | 64K x 32—SRAM                                   | 64      | CYM1831                           | t <sub>AA</sub> = 30, 35, 45           | 670 @ 30   | PZ            |
|                  | 2M   | 64K x 32—SRAM                                   | 64      | CYM1832                           | t <sub>AA</sub> = 35, 45, 55           | 980 @ 35   | PZ            |
|                  | 4M   | 512K x 8—SRAM                                   | 36      | CYM1460                           | t <sub>AA</sub> = 45, 55, 70           | 450 @ 45   | PF, PS        |
|                  | 4M   | 512K x 8—SRAM                                   | 36      | CYM1461                           | t <sub>AA</sub> = 70, 85, 100          | 120 @ 70   | PF, PS        |
|                  | 4M   | 256K x 16—SRAM                                  | 48      | CYM1641                           | t <sub>AA</sub> = 35, 45, 55           | 1760 @ 35  | HD            |
| <b>ECL SRAMs</b> | 1K   | 256K x 4—10K/10 KH                              | 24      | CY10E422                          | t <sub>AA</sub> = 3, 5                 | 205  | D, L          |
|                  | 1K   | 256K x 4—10K/10 KH                              | 24      | CY10E422L                         | t <sub>AA</sub> = 5, 7                 | 150  | D, L          |
|                  | 1K   | 256K x 4—100K                                   | 24      | CY100E422                         | t <sub>AA</sub> = 3, 5                 | 200  | D, L          |
|                  | 1K   | 256K x 4—100K                                   | 24      | CY100E422L                        | t <sub>AA</sub> = 5, 7                 | 150  | D, L          |
|                  | 4K   | 1024K x 4—10K/10 KH                             | 24      | CY10E474                          | t <sub>AA</sub> = 3, 5                 | 275  | D, L          |
|                  | 4K   | 1024K x 4—10K/10 KH                             | 24      | CY10E474L                         | t <sub>AA</sub> = 5, 7                 | 190  | D, L          |
|                  | 4K   | 1024K x 4—100K                                  | 24      | CY100E474                         | t <sub>AA</sub> = 3, 5                 | 275  | D, L          |
|                  | 4K   | 1024K x 4—100K                                  | 24      | CY100E474L                        | t <sub>AA</sub> = 5, 7                 | 190  | D, L          |
| <b>ECL PLDs</b>  | 32 x 64  | 16P8—10 KH                                      | 24      | CY10E301                          | t <sub>AA</sub> = 3, 4                 | 240  | D, L          |
|                  | 32 x 64  | 16P8—10 KH                                      | 24      | CY10E301L                         | t <sub>AA</sub> = 6                    | 150  | D, P, L, J    |
|                  | 32 x 64  | 16P8—100K                                       | 24      | CY100E301                         | t <sub>AA</sub> = 3, 4                 | 240  | D, L          |
|                  | 32 x 64  | 16P8—100K                                       | 24      | CY100E301L                        | t <sub>AA</sub> = 6                    | 150  | D, P, L, J    |
|                  | 32 x 32  | 16P4—10 KH                                      | 24      | CY10E302                          | t <sub>AA</sub> = 2, 5, 4              | 220  | D, L          |
|                  | 32 x 32  | 16P4—10 KH                                      | 24      | CY10E302L                         | t <sub>AA</sub> = 6                    | 150  | D, P, L, J    |
|                  | 32 x 32  | 16P4—100K                                       | 24      | CY100E302                         | t <sub>AA</sub> = 2, 5, 4              | 220  | D, L          |
|                  | 32 x 32  | 16P4—100K                                       | 24      | CY100E302L                        | t <sub>AA</sub> = 6                    | 150  | D, P, L, J    |

**Notes:**

The above specifications are for the commercial temperature range of 0°C to 70°C.

Military temperature range (–55°C to +125°C) product processed to MIL-STD-883 Revision C is also available. Speed and power selections may vary from those above.

Commercial grade product is available in plastic, CERDIP, or LCC. Military grade product is available in CERDIP or LCC. PLCC, SOJ, and SOIC packages are available on some products.

All power supplies are V<sub>CC</sub> = 5V ± 10%.

22S stands for 22-pin 300 mil. 24S stands for 24-pin 300 mil. 28S stands for 28-pin 300 mil.

F, K and T packages are special order only.

**Package Code:**

B = PLASTIC PIN GRID  
ARRAY  
D = CERDIP  
F = FLATPAK  
G = PIN GRID ARRAY  
H = WINDOWED  
HERMETIC LCC  
J = PLCC  
K = CERPAK  
L = LCC  
P = PLASTIC  
Q = WINDOWED LCC

R = WINDOWED PGA  
S = SOIC  
T = WINDOWED CERPAK  
V = SOJ  
W = WINDOWED CERDIP  
X = DICE  
HD = HERMETIC DIP  
HV = HERMETIC VERTICAL  
DIP  
PF = PLASTIC FLAT SIP  
PS = PLASTIC SIP  
PZ = PLASTIC ZIP

## Ordering Information

Specific ordering codes are indicated in the detailed data sheets. In general, the codes for all products (except modules) follow the format below:

| PAL & PLD |         |          |                               |
|-----------|---------|----------|-------------------------------|
| PREFIX    | DEVICE  | SUFFIX   | FAMILY                        |
| PAL C     | 16R8    | -25 P C  | PAL 20                        |
| PAL C     | 16R8    | L-35 P C | LOW POWER PAL 20              |
| PAL C     | 22V10   | -25 W C  | PAL 24 VARIABLE PRODUCT TERMS |
| PLD C     | 20G10   | -25 W C  | GENERIC PLD 24                |
| CY        | 7C330   | -33 P C  | PLD SYNCHRONOUS STATE MACHINE |
| CY        | 10E302  | -2.5 D C | 10K ECL PLD                   |
| CY        | 100E302 | -2.5 D C | 100K ECL PLD                  |

| RAM, PROM, FIFO, $\mu$ P, ECL |         |           |               |
|-------------------------------|---------|-----------|---------------|
| PREFIX                        | DEVICE  | SUFFIX    | FAMILY        |
| CY                            | 7C128   | -45 D M B | SRAM          |
| CY                            | 7C245   | L-35 P C  | PROM          |
| CY                            | 7C404   | -25 D M B | FIFO          |
| CY                            | 7C901   | -23 P C   | $\mu$ P       |
| CY                            | 10E415  | -3 D C    | 10K ECL SRAM  |
| CY                            | 100E415 | -3 F C    | 100K ECL SRAM |

PROCESSING  
 B = HI REL MIL STD 883 C  
 FOR MILITARY PRODUCT  
 = LEVEL 2 PROCESSING FOR COMMERCIAL PRODUCT

TEMPERATURE RANGE  
 C = COMMERCIAL (0°C TO 70°C)  
 M = MILITARY (-55°C TO +125°C)

PACKAGE  
 D = CERDIP  
 F = FLATPAK  
 G = PIN GRID ARRAY (PGA)  
 J = PLCC  
 K = CERPAK (GLASS SEALED FLAT PACKAGE)  
 L = LEADLESS CHIP CARRIER  
 P = PLASTIC  
 Q = WINDOWED LEADLESS CHIP CARRIER  
 S = SOIC (GULL WING)  
 T = WINDOWED CERPAK  
 V = SOIC (J LEAD)  
 W = WINDOWED CERDIP  
 X = DICE (WAFFLE PACK)

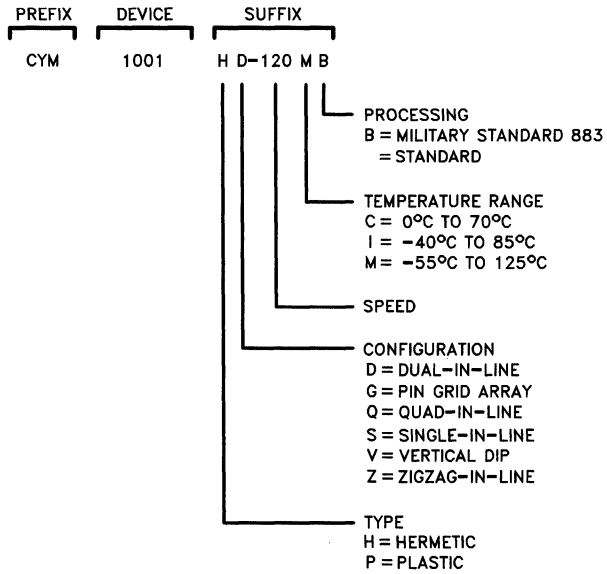
SPEED (ns or MHz)  
 L = LOW POWER OPTION  
 A, B, C = REVISION LEVEL

i.e. CY7C128-35PC, PALC16R8L-25PC

Cypress FSCM # 65786

## Ordering Information (Continued)

The codes for module products follow the format below:



0018-2

Cypress FSCM # 65786





# Product Line Cross Reference

|            |             |             |             |             |              |             |              |
|------------|-------------|-------------|-------------|-------------|--------------|-------------|--------------|
| CYPRESS    | CYPRESS     | CYPRESS     | CYPRESS     | CYPRESS     | CYPRESS      | CYPRESS     | CYPRESS      |
| 2147-35C   | 7C147-35C   | 2911AM      | 7C911-40M   | 7C150-25C   | 7C150-15C    | 7C251-65M   | 7C251-55M    |
| 2147-45C   | 2147-35C    | 3341-2C     | 7C401-5C +  | 7C150-35C   | 7C150-25C    | 7C253-65M   | 7C253-55M    |
| 2147-45C   | 7C147-45C   | 3341-2M     | 7C401-10M   | 7C150-35M   | 7C150-25M    | 7C254-45C   | 7C254-45C    |
| 2147-45M + | 7C147-45M + | 3341C       | 3341-2C     | 7C167-35C   | 7C167-25C    | 7C254-55C   | 7C254-45C    |
| 2147-55C   | 2147-45C    | 3341M       | 3341-2M     | 7C167-45M   | 7C167-35M +  | 7C254-65C   | 7C254-55C    |
| 2147-55M   | 2147-45M    | 54S189M     | 27S03M      | 7C168-35C   | 7C168-25C    | 7C254-65M   | 7C254-55M    |
| 2148-35C   | 21L48-35C   | 6116-35C    | 6116-35C    | 7C168-45M   | 7C168-35M +  | 7C261-35C   | 7C261-35C    |
| 2148-35C   | 7C148-35C   | 6116-45C    | 6116-35C    | 7C169-35C   | 7C169-25C    | 7C261-45C   | 7C261-35C    |
| 2148-35M   | 7C148-35M   | 6116-45M    | 6116-45M    | 7C169-40M   | 7C169-35M +  | 7C261-45M   | 7C261-45M    |
| 2148-45C   | 2148-35C    | 6116-55C    | 6116-45C    | 7C170-35C   | 7C170-25C    | 7C261-55C   | 7C261-45C    |
| 2148-45C   | 21L48-45C   | 6116-55M    | 6116-45M    | 7C170-45C   | 7C170-35C    | 7C261-55M   | 7C261-45M    |
| 2148-45M   | 2148-35M    | 74S189C     | 27S03C      | 7C170-45M   | 7C170-35M    | 7C263-35C   | 7C263-35C    |
| 2148-45M + | 7C148-45M + | 7C122-25C   | 7C122-15C + | 7C171-35C   | 7C171-25C    | 7C263-45C   | 7C263-35C    |
| 2148-55C   | 2148-45C    | 7C122-35C   | 7C122-25C   | 7C171-35M   | 7C171-35M    | 7C263-45M   | 7C263-45M    |
| 2148-55C   | 21L48-55C   | 7C122-35M   | 7C122-25M   | 7C171-45M   | 7C171-35M +  | 7C263-55C   | 7C263-45C    |
| 2148-55M   | 2148-45M    | 7C123-12C   | 7C123-7C    | 7C172-35C   | 7C172-25C    | 7C263-55M   | 7C263-45M    |
| 2149-35C   | 21L49-35C   | 7C128-35C   | 7C128-25C   | 7C172-45M   | 7C172-35M +  | 7C264-35C   | 7C264-35C    |
| 2149-35C   | 7C149-35C   | 7C128-35M   | 7C128-35M   | 7C186L-45M  | 7C186-45M    | 7C264-45C   | 7C264-35C    |
| 2149-35M   | 7C149-35M   | 7C128-45C   | 7C128-35C   | 7C189-25C   | 7C189-15C +  | 7C264-45M   | 7C264-45M    |
| 2149-45C   | 21L49-45C   | 7C128-45M   | 7C128-35M + | 7C190-25C   | 7C190-15C +  | 7C264-55C   | 7C264-45C    |
| 2149-45M   | 2149-35M    | 7C128-55C   | 7C128-45C + | 7C191-45M   | 7C191-35M    | 7C264-55M   | 7C264-45M    |
| 2149-45M   | 7C149-45M   | 7C128-55M   | 7C128-45M + | 7C192-45M   | 7C192-35M    | 7C268-50C   | 7C268-40C +  |
| 2149-55C   | 2149-45C    | 7C130-45C   | 7C130-35C   | 7C194-35C   | 7C194-25C    | 7C268-60C   | 7C268-50C    |
| 2149-55C   | 21L49-55C   | 7C130-45M   | 7C130-45M   | 7C194-45C   | 7C194-35C +  | 7C268-60M   | 7C268-50M +  |
| 2149-55M   | 2149-45M    | 7C130-55C   | 7C130-45C   | 7C194-45M   | 7C194-35M    | 7C269-50C   | 7C269-40C +  |
| 21L48-35C  | 7C148-35C   | 7C130-55M   | 7C130-45M   | 7C196-35C   | 7C196-25C    | 7C269-60C   | 7C269-50C    |
| 21L48-45C  | 21L48-35C   | 7C131-45C   | 7C131-35C   | 7C196-35M   | 7C196-35M    | 7C269-60M   | 7C269-50M +  |
| 21L48-45C  | 7C148-45C   | 7C131-45M   | 7C131-45M   | 7C196-45C   | 7C196-35C +  | 7C281-30C   | 7C281-30C    |
| 21L48-55C  | 21L48-45C   | 7C131-55C   | 7C131-45C   | 7C197-35C   | 7C197-25C    | 7C282-45C   | 7C282-30C +  |
| 21L49-35C  | 7C149-25C   | 7C131-55M   | 7C131-45M   | 7C197-45C   | 7C197-35C +  | 7C282-45M   | 7C282-45M    |
| 21L49-45C  | 21L49-35C   | 7C132-35C   | 7C132-35C   | 7C197-45M   | 7C197-35M    | 7C291-35C   | 7C291-25C +  |
| 21L49-45C  | 7C149-45C   | 7C132-45C   | 7C132-35C   | 7C198-45C   | 7C198-35C    | 7C291-35M   | 7C291-35M    |
| 21L49-55C  | 21L49-45C   | 7C132-55C   | 7C132-45C   | 7C198-55C   | 7C198-45C +  | 7C291-50C   | 7C291-35C    |
| 27S03AC    | 7C189-25C   | 7C132-55M   | 7C132-45M   | 7C198-55M   | 7C198-45M    | 7C291-50M   | 7C291-35M    |
| 27S03AM    | 7C189-25M   | 7C136-35C   | 7C136-35C   | 7C199-45C   | 7C199-35C    | 7C291A-35C  | 7C291AL-35C  |
| 27S03C     | 27S03AC     | 7C136-45C   | 7C136-35C   | 7C199-55C   | 7C199-45C +  | 7C291A-35M  | 7C291A-30M   |
| 27S03C     | 74S189C     | 7C136-55C   | 7C136-45C   | 7C199-55M   | 7C199-45M    | 7C291A-50C  | 7C291AL-50C  |
| 27S03M     | 27S03AM     | 7C136-55M   | 7C136-45M   | 7C225-30C   | 7C225-25C    | 7C291A-50M  | 7C291A-35M   |
| 27S03M     | 54S189M     | 7C140-35C   | 7C140-25C   | 7C225-30M   | 7C225-25M    | 7C291AL-35C | 7C291A-25C + |
| 27S07AC    | 7C190-25C   | 7C140-45C   | 7C140-35C   | 7C225-40C   | 7C225-30C    | 7C291AL-50C | 7C291AL-35C  |
| 27S07AM    | 7C190-25M   | 7C140-55C   | 7C140-45C   | 7C225-40M   | 7C225-35M    | 7C291L-35C  | 7C291-35C +  |
| 27S07C     | 27S07AC     | 7C141-35C   | 7C141-25C   | 7C235-40C   | 7C235-30C    | 7C291L-50C  | 7C291L-35C   |
| 27S07M     | 27S07AM     | 7C141-45C   | 7C141-35C   | 7C245-35C   | 7C245-25C    | 7C292-35C   | 7C292-25C +  |
| 27S07M     | 7C190-25M   | 7C141-55C   | 7C141-45C   | 7C245-45C   | 7C245-35C    | 7C292-50C   | 7C292-35C    |
| 2901CC     | 7C901-31C   | 7C147-35C   | 7C147-25C + | 7C245-45M   | 7C245-35M    | 7C292L-35C  | 7C292-35C +  |
| 2901CM     | 7C901-32M   | 7C147-35M + | 7C147-35M + | 7C245A-25C  | 7C245A-18C   | 7C292L-50C  | 7C292L-35C   |
| 2909AC     | 7C909-40C   | 7C147-45C   | 7C147-35C   | 7C245A-35C  | 7C245AL-35C  | 7C293A-35C  | 7C293AL-35C  |
| 2909AM     | 7C909-40M   | 7C148-25C   | 7C148-25C   | 7C245A-35M  | 7C245A-25M   | 7C293A-35M  | 7C293A-30M   |
| 2910AC     | 7C910-50C   | 7C148-35C   | 7C148-25C + | 7C245AL-35C | 7C245A-25C + | 7C293A-50C  | 7C293AL-50C  |
| 2910AM     | 7C910-51M   | 7C148-45C   | 7C148-35C   | 7C245L-35C  | 7C245-35C +  | 7C293A-50M  | 7C293A-35M   |
| 2910C      | 2910AC      | 7C149-35C   | 7C149-25C + | 7C245L-45C  | 7C245L-35C   | 7C293AL-35C | 7C293A-20C + |
| 2910M      | 2910AM      | 7C149-45C   | 7C149-35C   | 7C251-55C   | 7C251-45C    | 7C293AL-50C | 7C293AL-35C  |
| 2911AC     | 7C911-40C   | 7C149-45M   | 7C149-35M   | 7C251-65C   | 7C251-55C    | 7C401-10C   | 7C401-15C    |

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I<sub>CC</sub> and 5 mA on I<sub>SB</sub> ;

+ = meets all performance specs but may not meet I<sub>CC</sub> or I<sub>SB</sub> ;

\* = meets all performance specs except 2V data retention—may not meet I<sub>CC</sub> or I<sub>SB</sub> ;

- = functionally equivalent

# Product Line Cross Reference (Continued)

| CYPRESS   | CYPRESS   | CYPRESS       | CYPRESS       | CYPRESS        | CYPRESS        | AMD         | CYPRESS      |
|-----------|-----------|---------------|---------------|----------------|----------------|-------------|--------------|
| 7C401-10M | 7C401-15M | 7C517-45C     | 7C517-38C     | PALC16R8-35C   | PALC16R8-25C   | 2168-45M    | 7C168-45M    |
| 7C401-5C  | 7C401-10C | 7C517-55C     | 7C517-45C     | PALC16R8-40M   | PALC16R8-30M   | 2168-55C    | 7C168-45C    |
| 7C402-10C | 7C402-15C | 7C517-55M     | 7C517-42M     | PALC16R8L-35C  | PALC16R8L-25C  | 2168-55M    | 7C168-45M    |
| 7C402-10M | 7C402-15M | 7C517-75C     | 7C517-55C     | PALC22V10-35C  | PALC22V10-25C  | 2168-70C    | 7C168-45C    |
| 7C402-5C  | 7C402-10C | 7C517-75M     | 7C517-55M     | PALC22V10-40M  | PALC22V10-30M  | 2168-70M    | 7C168-45M    |
| 7C403-10C | 7C403-15C | 7C901-31C     | 7C901-23C +   | PALC22V10L-25C | PALC22V10-25C  | 2169-40C    | 7C169-40C    |
| 7C403-10M | 7C403-15M | 7C901-32M     | 7C901-27M     | PALC22V10L-35C | PALC22V10L-25C | 2169-50C    | 7C169-40C    |
| 7C403-15C | 7C403-25C | 7C909-40C     | 7C909-30C     | PLDC20G10-35C  | PLDC20G10-25C  | 2169-50M    | 7C169-40M    |
| 7C403-15M | 7C403-25M | 7C909-40M     | 7C909-30M     | PLDC20G10-40M  | PLDC20G10-30M  | 2169-70C    | 7C169-40C    |
| 7C404-10C | 7C404-15C | 7C910-50C     | 7C910-40C     |                |                | 2169-70M    | 7C169-40M    |
| 7C404-10M | 7C404-15M | 7C910-51M     | 7C910-46M     | <b>AMD</b>     | <b>CYPRESS</b> | 21L47-45C   | 7C147-45C    |
| 7C404-15C | 7C404-25C | 7C910-93C     | 7C910-50C     | PREFIX:Am      | PREFIX:CY      | 21L47-55C   | 7C147-45C    |
| 7C404-15M | 7C404-25M | 7C910-99M     | 7C910-51M     | PREFIX:SN      | PREFIX:CY      | 21L47-70C   | 7C147-45C    |
| 7C408-15C | 7C408-25C | 7C9101-40C    | 7C9101-30C    | SUFFIX:B       | SUFFIX:B       | 21L48-45C   | 21L48-45C    |
| 7C408-15M | 7C408-25M | 7C9101-45M    | 7C9101-35M    | SUFFIX:D       | SUFFIX:D       | 21L48-55C   | 21L48-55C    |
| 7C408-25C | 7C408-35C | 7C911-40C     | 7C911-30C     | SUFFIX:F       | SUFFIX:F       | 21L48-70C   | 21L48-55C    |
| 7C409-15C | 7C409-25C | 7C911-40M     | 7C911-30M     | SUFFIX:L       | SUFFIX:L       | 21L49-45C   | 21L49-45C    |
| 7C409-15M | 7C409-25M | 9122-25C      | 7C122-15C     | SUFFIX:P       | SUFFIX:P       | 21L49-55C   | 21L49-55C    |
| 7C409-25C | 7C409-35C | 9122-25C      | 91L22-25C     | 2130-100C      | 7C130-55C      | 21L49-70C   | 21L49-55C    |
| 7C420-40C | 7C420-30C | 9122-35C      | 9122-25C      | 2130-120C      | 7C130-55C      | 27C191-25C  | 7C292A-25C   |
| 7C420-40M | 7C420-30M | 9122-35C      | 91L22-35C     | 2130-70C       | 7C130-55C      | 27C191-35C  | 7C291A-25C + |
| 7C420-65C | 7C420-40C | 9122-45C      | 93L422C       | 2147-35C       | 2147-35C       | 27C191-35C  | 7C291A-35C   |
| 7C420-65M | 7C420-40M | 91L22-25C     | 7C122-25C     | 2147-45C       | 2147-45C       | 27C191-35C  | 7C292A-35C   |
| 7C421-40C | 7C421-30C | 91L22-35C     | 7C122-35C     | 2147-45M       | 2147-45M       | 27C191-35C  | 7C292AL-35C  |
| 7C421-40M | 7C421-30M | 91L22-45C     | 93L422AC      | 2147-55C       | 2147-55C       | 27C191-35M  | 7C292A-30M   |
| 7C421-65C | 7C421-40C | 93422AC       | 7C122-35C     | 2147-55M       | 2147-55M       | 27C191-45M  | 7C291A-45M   |
| 7C421-65M | 7C421-40M | 93422AC       | 9122-35C      | 2147-70C       | 2147-55C       | 27C291-25C  | 7C291A-25C   |
| 7C424-40C | 7C424-30C | 93422AM       | 7C122-35M     | 2147-70M       | 2147-55M       | 27C291-35C  | 7C291AL-35C  |
| 7C424-40M | 7C424-30M | 93422C        | 93L422AC      | 2148-35C       | 2148-35C       | 27C291-45M  | 7C291A-35M   |
| 7C424-65C | 7C424-40C | 93422M        | 93422AM       | 2148-35M       | 2148-35M       | 27C291A-30M | 7C291A-30M   |
| 7C424-65M | 7C424-40M | 93422M        | 93L422AM      | 2148-45C       | 2148-45C       | 27L803C     | 27L803C      |
| 7C425-40C | 7C425-30C | 93L422AC      | 7C122-35C     | 2148-45M       | 2148-45M       | 27L803M     | 27L803M +    |
| 7C425-40M | 7C425-30M | 93L422AC      | 91L22-45C     | 2148-55C       | 2148-55C       | 27L807C     | 27S07C +     |
| 7C425-65C | 7C425-40C | 93L422AM      | 7C122-35M     | 2148-55M       | 2148-55M       | 27L8191C    | 7C292-35C    |
| 7C425-65M | 7C425-40M | 93L422C       | 93L422AC      | 2148-70C       | 2148-55C       | 27L8291C    | 7C291-35C    |
| 7C428-40C | 7C428-30C | 93L422M       | 93L422AM      | 2148-70M       | 2148-55M       | 27L8291M    | 7C291-35M    |
| 7C428-40M | 7C428-30M | PALC16L8-25C  | PALC16L8L-25C | 2149-35C       | 2149-35C       | 27PS181AC   | 7C282-45C    |
| 7C428-65C | 7C428-40C | PALC16L8-30M  | PALC16L8-20M  | 2149-45C       | 2149-45C       | 27PS181AM   | 7C282-45M +  |
| 7C428-65M | 7C428-40M | PALC16L8-35C  | PALC16L8-25C  | 2149-45M       | 2149-45M       | 27PS181C    | 7C282-45C    |
| 7C429-40C | 7C429-30C | PALC16L8-40M  | PALC16L8-30M  | 2149-55C       | 2149-55C       | 27PS181M    | 7C282-45M +  |
| 7C429-40M | 7C429-30M | PALC16L8L-35C | PALC16L8L-25C | 2149-55M       | 2149-55M       | 27PS191AC   | 7C292-50C    |
| 7C429-65C | 7C429-40C | PALC16R4-25C  | PALC16R4L-25C | 2149-70C       | 2149-55C       | 27PS191AM   | 7C292-50M +  |
| 7C429-65M | 7C429-40M | PALC16R4-30M  | PALC16R4-20M  | 2149-70M       | 2149-55M       | 27PS191C    | 7C292-50C    |
| 7C510-55C | 7C510-45C | PALC16R4-35C  | PALC16R4-25C  | 2167-35C       | 7C167-35C      | 27PS191M    | 7C292-50M +  |
| 7C510-65C | 7C510-55C | PALC16R4-40M  | PALC16R4-30M  | 2167-35M       | 7C167-35M      | 27PS281AC   | 7C281-45C    |
| 7C510-65M | 7C510-55M | PALC16R4L-35C | PALC16R4L-25C | 2167-45C       | 7C167-45C      | 27PS281AM   | 7C281-45M +  |
| 7C510-75C | 7C510-65C | PALC16R6-25C  | PALC16R6L-25C | 2167-45M       | 7C167-45M      | 27PS281C    | 7C281-45C    |
| 7C510-75M | 7C510-65M | PALC16R6-30M  | PALC16R6-20M  | 2167-55C       | 7C167-45C      | 27PS281M    | 7C281-45M +  |
| 7C516-45C | 7C516-38C | PALC16R6-35C  | PALC16R6-25C  | 2167-55M       | 7C167-45M      | 27PS291AC   | 7C291-50C    |
| 7C516-55C | 7C516-45C | PALC16R6-40M  | PALC16R6-30M  | 2167-70C       | 7C167-45C      | 27PS291AM   | 7C291-50M +  |
| 7C516-55M | 7C516-42M | PALC16R6L-35C | PALC16R6L-25C | 2167-70M       | 7C167-45M      | 27PS291C    | 7C291-50C    |
| 7C516-75C | 7C516-55C | PALC16R8-25C  | PALC16R8L-25C | 2168-35C       | 7C168-35C      | 27PS291M    | 7C291-50M +  |
| 7C516-75M | 7C516-55M | PALC16R8-30M  | PALC16R8-20M  | 2168-45C       | 7C168-45C      | 27S03AC     | 27S03AC      |

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- = functionally equivalent



# Product Line Cross Reference (Continued)

| AMD        | CYPRESS      | AMD      | CYPRESS     | AMD        | CYPRESS     | AMD         | CYPRESS       |
|------------|--------------|----------|-------------|------------|-------------|-------------|---------------|
| 27S03AM    | 27S03AM      | 2901BC   | 2901CC      | 29L510M    | 7C510-75M   | 99C165-55C  | 7C166-45C +   |
| 27S03C     | 27S03C       | 2901BM   | 2901CM      | 29L516C    | 7C516-75C   | 99C165-55M  | 7C166-45M +   |
| 27S03M     | 27S03M       | 2901CC   | 2901CC      | 29L516M    | 7C516-75M   | 99C165-70C  | 7C166-45C +   |
| 27S07AC    | 27S07AC      | 2901CM   | 2901CM      | 29L517C    | 7C517-75C   | 99C165-70M  | 7C166-45M +   |
| 27S07AM    | 27S07AM      | 2909AC   | 2909AC      | 29L517M    | 7C517-75M   | 99C641-25C  | 7C187-25C     |
| 27S07C     | 27S07C       | 2909AM   | 2909AM      | 3341C      | 3341C       | 99C641-35C  | 7C187-35C     |
| 27S07M     | 27S07M       | 2909C    | 2909AC      | 3341M      | 3341M       | 99C641-45C  | 7C187-45C     |
| 27S181AC   | 7C282-30C    | 2909M    | 2909M       | 54S189M    | 54S189M     | 99C641-45M  | 7C187-45M     |
| 27S181AM   | 7C282-45M    | 2910-1C  | 2910C       | 74S189C    | 74S189C     | 99C641-55C  | 7C187-45C     |
| 27S181C    | 7C282-45C    | 2910-1M  | 2910M       | 9122-25C   | 9122-25C    | 99C641-55M  | 7C187-45M     |
| 27S181M    | 7C282-45M    | 2910AC   | 2910AC      | 9122-35C   | 9122-35C    | 99C641-70C  | 7C187-45C     |
| 27S191AC   | 7C292-35C    | 2910AM   | 2910AM      | 9122-35M   | 7C122-35M   | 99C641-70M  | 7C187-45M     |
| 27S191AM   | 7C292-50M    | 2910C    | 2910C       | 9128-100C  | 6116-55C    | 99C68-35C   | 7C168-35C     |
| 27S191C    | 7C292-50C    | 2910M    | 2910M       | 9128-120M  | 6116-55M    | 99C68-45C   | 7C168-45C*    |
| 27S191M    | 7C292-50M    | 29116AC  | 7C9116AC    | 9128-150C  | 6116-55C    | 99C68-45M   | 7C168-45M*    |
| 27S191SAC  | 7C292A-20C   | 29116AM  | 7C9116AM    | 9128-150M  | 6116-55M    | 99C68-55C   | 7C168-45C*    |
| 27S25AC    | 7C225-30C    | 29116C   | 7C9116AC    | 9128-200C  | 6116-55C    | 99C68-55M   | 7C168-45M*    |
| 27S25AM    | 7C225-35M    | 29116M   | 7C9116AM    | 9128-200M  | 6116-55M    | 99C68-70C   | 7C168-45C*    |
| 27S25C     | 7C225-40C    | 29117C   | 7C9117AC    | 9128-70C   | 6116-55C    | 99C68-70M   | 7C168-45M*    |
| 27S25M     | 7C225-40M    | 29117M   | 7C9117AM    | 9128-90M   | 6116-55M    | 99C88H-35C  | 7C186-35C     |
| 27S25SAC   | 7C225-25C    | 2911AC   | 2911AC      | 9150-20C   | 7C150-15C   | 99C88H-45C  | 7C186-45C     |
| 27S25SAM   | 7C225-35M    | 2911AM   | 2911AM      | 9150-25C   | 7C150-25C   | 99C88H-45M  | 7C186-45M     |
| 27S281AC   | 7C281-30C    | 2911C    | 2911AC      | 9150-25M   | 7C150-25M   | 99C88H-55C  | 7C186-55C     |
| 27S281AM   | 7C281-45M    | 2911M    | 2911M       | 9150-35C   | 7C150-35C   | 99C88H-55M  | 7C186-55M     |
| 27S281C    | 7C281-45C    | 29510C   | 7C510-75C   | 9150-35M   | 7C150-35M   | 99C88H-70C  | 7C186-55C     |
| 27S281M    | 7C281-45M    | 29510M   | 7C510-75M   | 9150-45C   | 7C150-35C   | 99C88H-70M  | 7C186-55M     |
| 27S291AC   | 7C291-35C    | 29516AM  | 7C516-55M   | 9150-45M   | 7C150-35M   | 99CL68-35C  | 7C168-35C     |
| 27S291AM   | 7C291-50M    | 29516C   | 7C516-55C   | 91L22-35C  | 91L22-35C   | 99CL68-45C  | 7C168-45C*    |
| 27S291C    | 7C291-50C    | 29516M   | 7C516-55M   | 91L22-35M  | 7C122-35M   | 99CL68-45M  | 7C168-45M*    |
| 27S291M    | 7C291-50M    | 29517AC  | 7C517-38C   | 91L22-45C  | 91L22-45C   | 99CL68-55C  | 7C168-45C*    |
| 27S291SAC  | 7C291A-25C   | 29517C   | 7C517-55C   | 91L22-45M  | 7C122-35M   | 99CL68-55M  | 7C168-45M*    |
| 27S291SAM  | 7C291A-30M   | 29517M   | 7C517-55M   | 91L22-60C  | 7C122-35C + | 99CL68-70C  | 7C168-45C*    |
| 27S35AC    | 7C235-30C    | 29701C   | 27S07C      | 91L50-25C  | 7C150-25C   | 99CL68-70M  | 7C168-45M*    |
| 27S35AM    | 7C235-40M    | 29701M   | 27S07M      | 91L50-35C  | 7C150-35C   | PAL16L8A-4C | PALC16L8L-35C |
| 27S35C     | 7C235-40C    | 29703C   | 27S03C      | 91L50-45C  | 7C150-35C   | PAL16L8A-4M | PALC16L8L-40M |
| 27S35M     | 7C235-40M    | 29703M   | 27S03M      | 93422AC    | 93422AC     | PAL16L8AC   | PALC16L8L-25C |
| 27S45AC    | 7C245-35C    | 29C01-1C | 7C901-23C + | 93422AM    | 93422AM     | PAL16L8ALC  | PALC16L8L-25C |
| 27S45AM    | 7C245-45M    | 29C01BA  | 7C901-32M   | 93422C     | 93422C      | PAL16L8ALM  | PALC16L8L-30M |
| 27S45C     | 7C245-45C    | 29C01BC  | 7C901-31C   | 93422M     | 93422M      | PAL16L8AM   | PALC16L8L-30M |
| 27S45M     | 7C245-45M    | 29C01C   | 7C901-31C   | 93L422AC   | 93L422AC    | PAL16L8BM   | PALC16L8L-20M |
| 27S45SAC   | 7C245-25C    | 29C01CC  | 7C901-31C   | 93L422AM   | 93L422AM    | PAL16L8C    | PALC16L8L-35C |
| 27S45SAM   | 7C245A-25M - | 29C10-1C | 7C910-40C   | 93L422C    | 93L422C     | PAL16L8LC   | PALC16L8L-35C |
| 27S49A-45C | 7C264-45C    | 29C101C  | 7C9101-40C  | 93L422M    | 93L422M     | PAL16L8LM   | PALC16L8L-40M |
| 27S49AC    | 7C264-45C    | 29C101M  | 7C9101-35M  | 99C164-35C | 7C164-35C + | PAL16L8M    | PALC16L8L-40M |
| 27S49AM    | 7C264-55M    | 29C10ABA | 7C910-51M   | 99C164-45C | 7C164-45C + | PAL16L8QC   | PALC16L8L-35C |
| 27S49C     | 7C264-55C    | 29C10AC  | 7C910-50C   | 99C164-45M | 7C164-45M + | PAL16L8QM   | PALC16L8L-40M |
| 27S49M     | 7C264-55M    | 29C10AC  | 7C910-93C   | 99C164-55C | 7C164-45C + | PAL16R4A-4C | PALC16R4L-35C |
| 27S51C     | 7C254-55C    | 29C116C  | 7C9116AC    | 99C164-55M | 7C164-45M + | PAL16R4A-4M | PALC16R4-40M  |
| 27S51M     | 7C254-65M    | 29C116M  | 7C9116AM    | 99C164-70C | 7C164-45C + | PAL16R4ALC  | PALC16R4-25C  |
| 2841AC     | 3341C        | 29C117C  | 7C9117AC    | 99C164-70M | 7C164-45M   | PAL16R4ALM  | PALC16R4-30M  |
| 2841AM     | 3341M        | 29L116AC | 7C9116AC    | 99C165-35C | 7C166-35C + | PAL16R4AM   | PALC16R4-30M  |
| 2841C      | 3341C        | 29L116AM | 7C9116AM    | 99C165-45C | 7C166-45C + | PAL16R4BM   | PALC16R4-20M  |
| 2841M      | 3341M        | 29L510C  | 7C510-75C   | 99C165-45M | 7C166-45M + | PAL16R4C    | PALC16R4-35C  |

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\* = meets all performance specs except 2V data retention—may not meet I<sub>CC</sub> or I<sub>SB</sub> ;

- = functionally equivalent

| AMD               | CYPRESS        | DENSEPAK         | CYPRESS        | FAIRCHILD   | CYPRESS        | FAIRCHILD      | CYPRESS        |
|-------------------|----------------|------------------|----------------|-------------|----------------|----------------|----------------|
| PAL16R4LC         | PALC16R4-35C   | 1027-25C         | 1621HD-25C     | 100E422-5   | 100E422-5C     | 93L422AC       | 93L422AC       |
| PAL16R4LM         | PALC16R4-40M   | 1027-25C         | 1621HD-25C     | 100E422-5   | 100E422-5C     | 93L422AM       | 93L422AM       |
| PAL16R4M          | PALC16R4-40M   | 1027-35C         | 1621HD-30C     | 100E422-7   | 100E422-7C     | 93L422C        | 93L422C        |
| PAL16R4QC         | PALC16R4L-35C  | 1027-35C         | 1621HD-35C     | 100E422-7   | 10E422-7C      | 93L422M        | 93L422M        |
| PAL16R4QM         | PALC16R4-40M   | 1027-45C         | 1621HD-45C     | 100E474-7   | 100E474-7C     | 93Z451AC       | 7C282-30C      |
| PAL16R6A-4C       | PALC16R6L-35C  | 1027-55C         | 1621HD-55C     | 100E474-7   | 10E474-7C      | 93Z451AM       | 7C282-45M      |
| PAL16R6A-4M       | PALC16R6-40M   | 16X17-25C        | 1611HV-25C     | 1600C45     | 7C187-45C      | 93Z451C        | 7C282-30C      |
| PAL16R6AC         | PALC16R6-25C   | 16X17-25C        | 1611HV-25C     | 1600C55     | 7C187-45C      | 93Z451M        | 7C282-45M      |
| PAL16R6ALC        | PALC16R6-25C   | 16X17-35C        | 1611HV-35C     | 1600C70     | 7C187-45C      | 93Z511C        | 7C292-35C      |
| PAL16R6ALM        | PALC16R6-30M   | 16X17-35C        | 1611HV-35C     | 1600M55     | 7C187-45M      | 93Z511M        | 7C292-50M      |
| PAL16R6AM         | PALC16R6-30M   | 16X17-45C        | 1611HV-45C     | 1600M70     | 7C187-45M      | 93Z565AC       | 7C264-45C      |
| PAL16R6BM         | PALC16R6-20M   | 16X17-45C        | 1611HV-45C     | 1601C55     | 7C187-45C      | 93Z565AM       | 7C264-55M      |
| PAL16R6C          | PALC16R6-35C   | 16X17-55C        | 1611HV-55C     | 1620C35     | 7C164-35C +    | 93Z565C        | 7C264-55C      |
| PAL16R6LC         | PALC16R6-35C   | 41288-100C       | 1421HD-85C     | 1620M35     | 7C164-35M      | 93Z565M        | 7C264-55M      |
| PAL16R6LM         | PALC16R6-40M   | 41288-100C       | 1421HD-100C    | 1620M45     | 7C164-45M      | 93Z611C        | 7C292-25C      |
| PAL16R6M          | PALC16R6-40M   | 41288-70C        | 1421HD-70C     | 1621C25     | 7C164-25C +    | 93Z611M        | 7C291A-30M     |
| PAL16R6QC         | PALC16R6L-35C  | 41288-85C        | 1421HD-85C     | 1622C25     | 7C166-25C +    | 93Z665C        | 7C264-35C      |
| PAL16R6QM         | PALC16R6-40M   | 41288-85C        | 1421HD-85C     | 1622C35     | 7C166-35C +    | 93Z665M        | 7C264-45M      |
| PAL16R8A-4C       | PALC16R8L-35   | 6432-45C         | 1830HD-45C     | 1622M35     | 7C166-35M      | 93Z667C        | 7C263-35C      |
| PAL16R8A-4M       | PALC16R8-40M   | 6432-55C         | 1830HD-55C     | 1622M45     | 7C166-45M      | 93Z667M        | 7C261-45M      |
| PAL16R8AC         | PALC16R8-25C   | 6432-55C         | 1830HD-55C     | 16L8A       | PALC16L8-20M   |                |                |
| PAL16R8ALC        | PALC16R8-25C   | 8M624-100C       | 1623HD-85C     | 16L8A       | PALC16L8-25C   | <b>FUJITSU</b> | <b>CYPRESS</b> |
| PAL16R8ALM        | PALC16R8-30M   | 8M624-85C        | 1623HD-100C    | 16P8A       | PALC16L8-20M   | PREFIX:MB      | PREFIX:CY      |
| PAL16R8AM         | PALC16R8-30M   | 8M656-35C        | 1610HD-35C     | 16P8A       | PALC16L8-25C - | PREFIX:MBM     | PREFIX:CY      |
| PAL16R8BM         | PALC16R8-20M   | 8M656-70C        | 1610HD-70C     | 16R4A       | PALC16R4-20M   | SUFFIX:F       | SUFFIX:F       |
| PAL16R8C          | PALC16R8-35C   |                  |                | 16R4A       | PALC16R4-25C   | SUFFIX:M       | SUFFIX:P       |
| PAL16R8LC         | PALC16R8-35C   | <b>EDI</b>       | <b>CYPRESS</b> | 16R6A       | PALC16R6-20M   | SUFFIX:Z       | SUFFIX:D       |
| PAL16R8LM         | PALC16R8-40M   | PREFIX:ED        | PREFIX:CYM     | 16R6A       | PALC16R6-25C   | 100422A-5C     | 100E422-5C     |
| PAL16R8M          | PALC16R8-40M   | 816H16C-25       | 1611HV-25C     | 16R8A       | PALC16R8-20M   | 100422A-7C     | 100E422-7C     |
| PAL16R8QC         | PALC16R8L-35   | 816H16C-35       | 1611HV-35C     | 16R8A       | PALC16R8-25C   | 100422AC       | 100E422-7C     |
| PAL16R8QM         | PALC16R8-40M   | 816H16C-45       | 1611HV-45C     | 16RP4A      | PALC16R4-20M   | 100474A-3C     | 100E474-3C     |
| PAL22V10AC        | PALC22V10-25C  | 8M8128C-100      | 1421HD-85C     | 16RP4A      | PALC16R4-25C   | 100474A-5C     | 100E474-5C     |
| PAL22V10AM        | PALC22V10-30M  | 8M8128C-70       | 1421HD-70C     | 16RP6A      | PALC16R6-20M   | 100474A-7C     | 100E474-7C     |
| PAL22V10C         | PALC22V10-35C  | H816H16C-25CC-   | 1611HV-25C     | 16RP6A      | PALC16R6-25C   | 100474AC       | 100E474-7C     |
| PAL22V10M         | PALC22V10-40M  | H816H16C-35CC-   | 1611HV-35C     | 16RP8A      | PALC16R8-20M   | 10422A-5C      | 10E422-5C      |
|                   |                | H816H16C-45CC-   | 1611HV-45C     | 16RP8A      | PALC16R8-25C   | 10422A-7C      | 10E422-7C      |
|                   |                | H816H16C-55CC-   | 1611HV-45C     | 3341AC      | 3341C          | 10422AC        | 10E422-7C      |
| <b>ANALOG DEV</b> | <b>CYPRESS</b> | 18M1664C100CC    | 1623HD-100C    | 3341C       | 3341C          | 10474A-3C      | 10E474-3C      |
| PREFIX:ADSP       | PREFIX:CY      | 18M1664C60CC     | 1623HD-55C     | 54F189      | 7C189-25M -    | 10474A-5C      | 10E474-5C      |
| SUFFIX:883B       | SUFFIX:B       | 18M1664C70CC     | 1623HD-70C     | 54F219      | 7C190-25M -    | 10474A-7C      | 10E474-7C      |
| SUFFIX:D          | SUFFIX:D       | 18M1664C85CC     | 1623HD-85C     | 54F413      | 7C401-15M      | 10474AC        | 10E474-7C      |
| SUFFIX:E          | SUFFIX:L       |                  |                |             |                |                |                |
| SUFFIX:F          | SUFFIX:F       | 18M8128C60CC     | 1420HD-55C     | 54S189M     | 54S189M        | 2147H-35       | 2147-35C       |
| SUFFIX:G          | SUFFIX:G       | 18M8128C70CC     | 1421HD-70C     | 74AC1010-40 | 7C510-45C      | 2147H-45       | 2147-45C       |
| 1010A             | 7C510-65C +    | 18M8128C80CC     | 1421HD-70C     | 74F189      | 7C189-25C -    | 2147H-55       | 2147-55C       |
| 1010J             | 7C510-75C +    | 18M8128C90CC     | 1421HD-85C     | 74F219      | 7C190-25C -    | 2147H-70       | 2147-55C       |
| 1010K             | 7C510-75C +    |                  |                | 74F413      | 7C401-15C      | 2148-55L       | 21L48-55C      |
| 1010S             | 7C510-75M +    | <b>FAIRCHILD</b> | <b>CYPRESS</b> | 74LS189     | 27LS03C        | 2148-70L       | 21L48-55C      |
|                   |                | PREFIX:F         | PREFIX:CY      |             |                |                |                |
| 1010T             | 7C510-75M +    | SUFFIX:D         | SUFFIX:D       | 74S189      | 74S189C        | 2149-45        | 2149-45C       |
| 7C901-27M         | 7C901-32M      | SUFFIX:F         | SUFFIX:F       | 93422AC     | 93422AC        | 2149-55L       | 21L49-55C      |
| 7C901-32M         | 2901CM         | SUFFIX:L         | SUFFIX:L       | 93422AM     | 93422AM        | 2149-70L       | 21L49-55C      |
|                   |                | SUFFIX:P         | SUFFIX:P       | 93422C      | 93422C         | 7132E          | 7C282-45C      |
| <b>DENSEPAK</b>   | <b>CYPRESS</b> | SUFFIX:QB        | SUFFIX:B       | 93422M      | 93422M         | 7132E-SK       | 7C281-45C      |
| PREFIX:DPS        | PREFIX:CYM     |                  |                | 93475C      | 2149-45C       | 7132E-W        | 7C282-45M      |

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- = functionally equivalent



# Product Line Cross Reference (Continued)

| FUJITSU   | CYPRESS     | HARRIS     | CYPRESS       | HITACHI    | CYPRESS     | HITACHI   | CYPRESS     |
|-----------|-------------|------------|---------------|------------|-------------|-----------|-------------|
| 7132H     | 7C282-45C   | PREFIX:HM  | PREFIX:CY     | PREFIX:HM  | PREFIX:CY   | 6168HL-55 | 7C168-45C*  |
| 7132H-SK  | 7C281-45C   | PREFIX:HPL | PREFIX:CY     | PREFIX:HN  | PREFIX:CY   | 6168HL-70 | 7C168-45C*  |
| 7132Y     | 7C282-30C   | SUFFIX:8   | SUFFIX:B      | SUFFIX:CG  | SUFFIX:L    | 6264-10   | 7C186-55C + |
| 7132Y-SK  | 7C281-30C   | PREFIX:1   | SUFFIX:D      | SUFFIX:G   | SUFFIX:D    | 6264-12   | 7C186-55C + |
| 7138E     | 7C292-50C   | PREFIX:9   | SUFFIX:F      | SUFFIX:P   | SUFFIX:P    | 6264-15   | 7C186-55C + |
| 7138E-SK  | 7C291-50C   | PREFIX:4   | SUFFIX:L      | 100422C    | 100E422-7C  | 6267-35   | 7C167-35C + |
| 7138E-W   | 7C292-50M   | PREFIX:3   | SUFFIX:P      | 100474-10C | 100E474-7C  | 6267-45   | 7C167-45C   |
| 7138H     | 7C292-35C   | 16LC8-5    | PALC16L8L-35C | 100474-8C  | 100E474-7C  | 6268-25   | 7C168-25C   |
| 7138H-SK  | 7C291-35C   | 16LC8-8    | PALC16L8-40M  | 100474C    | 100E474-7C  | 6268-35   | 7C168-35C   |
| 7138Y     | 7C292-35C   | 16LC8-9    | PALC16L8-40M  | 10422C     | 10E422-7C   | 6287-45   | 7C187-45C   |
| 7138Y-SK  | 7C291-35C   | 16RC4-5    | PALC16R4L-35C | 10474-10C  | 100E474-7C  | 6287-55   | 7C187-45C   |
| 7144E     | 7C264-55C   | 16RC4-8    | PALC16R4-40M  | 10474-8C   | 10E474-7C   | 6287-70   | 7C187-45C   |
| 7144E-W   | 7C264-55M   | 16RC4-9    | PALC16R4-40M  | 10474C     | 100E474-7C  | 6288-35   | 7C164-35C   |
| 7144H     | 7C264-55C   | 16RC6-5    | PALC16R6L-35C | 25089      | 7C282-45C   | 6288-45   | 7C164-45C   |
| 7144Y     | 7C264-45C   | 16RC6-8    | PALC16R6-40M  | 25089S     | 7C282-45C   | 6288-55   | 7C164-45C   |
| 7226RA-20 | 7C225-30C   | 16RC6-9    | PALC16R6-40M  | 25169S     | 7C292-30C   | 6716      | 7C128-25C   |
| 7226RA-25 | 7C225-30C   | 16RC8-5    | PALC16R8L-35C | 4847       | 2147-55C    | 6787-30   | 7C187-25C   |
| 7232RA-20 | 7C235-30C   | 16RC8-8    | PALC16R8-40M  | 4847-2     | 2147-45C    | 6788-25   | 7C164-25C   |
| 7232RA-25 | 7C235-30C   | 16RC8-9    | PALC16R8-40M  | 4847-3     | 2147-55C    | 6788-30   | 7C164-25C   |
| 7238RA-20 | 7C245-25C   | 6-76161-2  | 7C291-50M     | 6116ALS-12 | 6116-55C*   |           |             |
| 7238RA-25 | 7C245-35C   | 6-76161-5  | 7C291-50C     | 6116ALS-15 | 6116-55C*   |           |             |
| 8128-10   | 7C128-55C   | 6-76161A-2 | 7C291-50M     | 6116ALS-20 | 6116-55C*   |           |             |
| 8128-15   | 7C128-55C   | 6-76161A-5 | 7C291-50C     | 6116AS-12  | 6116-55C +  |           |             |
| 8167-70W  | 7C167-45M   | 6-76161B-5 | 7C291-35C     | 6116AS-15  | 6116-55C +  | SUFFIX:P  | SUFFIX:P    |
| 8167A-55  | 7C167-45C   | 6-7681-5   | 7C281-45C     | 6116AS-20  | 6116-55C +  | SUFFIX:S  | SUFFIX:D    |
| 8167A-70  | 7C167-45C   | 6-7681A-5  | 7C281-45C     | 6147       | 7C147-45C*  | SUFFIX:W  | SUFFIX:L    |
| 8168-55   | 7C168-45C   | 65162-5    | 6116-55C*     | 6147-3     | 7C147-45C*  | 1203-25   | 7C147-25C + |
| 8168-70   | 7C168-45C   | 65162-8    | 6116-55M*     | 6147H-35   | 7C147-35C + | 1203-35   | 7C147-35C + |
| 8168-70W  | 7C168-45M   | 65162-9    | 6116-55M*     | 6147H-45   | 7C147-45C + | 1203-45   | 7C147-45C + |
| 8171-55   | 7C187-45    | 65162B-5   | 6116-55C*     | 6147H-55   | 7C147-45C + | 1203M-35  | 7C147-35M + |
| 8171-70   | 7C187-45C   | 65162B-8   | 6116-55M*     | 6147HL-35  | 7C147-35C*  | 1203M-45  | 7C147-45M + |
| 81C67-35  | 7C167-35C   | 65162B-9   | 6116-55M*     | 6147HL-45  | 7C147-45C*  | 1223-25   | 7C148-25C   |
| 81C67-45  | 7C167-45C   | 65162C-8   | 6116-55M*     | 6147HL-55  | 7C147-55C*  | 1223-35   | 7C148-35C   |
| 81C67-55W | 7C167-45M   | 65162C-9   | 6116-55M*     | 6148       | 7C148-45C   | 1223-45   | 7C148-45C   |
| 81C68-45  | 7C168-45C   | 65162S-5   | 6116-55C*     | 6148H-35   | 21L48-35C   | 1223M-35  | 7C148-25M + |
| 81C68-55W | 7C168-45M + | 65162S-9   | 6116-55M*     | 6148H-45   | 7C148-45C + | 1223M-45  | 7C148-45M + |
| 81C71-45  | 7C187-45C   | 65262-8    | 7C167-45M*    | 6148H-55   | 7C148-45C + | 1400-35   | 7C167-35C   |
| 81C71-55  | 7C187-45C   | 65262-9    | 7C167-45M*    | 6148HL-35  | 21L48-35C*  | 1400-45   | 7C167-45C   |
| 81C74-25  | 7C164-25C   | 65262B-8   | 7C167-45M*    | 6148HL-45  | 7C148-45C*  | 1400-55   | 7C167-45C   |
| 81C74-35  | 7C164-35C + | 65262B-9   | 7C167-45M*    | 6148HL-55  | 7C148-45C*  | 1400M-45  | 7C167-45M   |
| 81C74-45  | 7C164-45C   | 65262C-9   | 7C167-45M*    | 6148L      | 7C148-45C*  | 1400M-55  | 7C167-45M   |
| 81C75-25  | 7C166-25C   | 65262S-9   | 7C167-45M*    | 6167-6     | 7C167-45C + | 1400M-70  | 7C167-45M   |
| 81C75-35  | 7C166-35C   | 76161-2    | 7C292-50M     | 6167-8     | 7C167-45C + | 1403-25   | 7C167-25C   |
| 81C78-45  | 7C186-45C   | 76161A-2   | 7C292-50M     | 6167H-55   | 7C167-45C   | 1403-35   | 7C167-35C + |
| 81C78-55  | 7C186-55C   | 76161A-5   | 7C292-50C     | 6167H-70   | 7C167-45C   | 1403-45   | 7C167-45C + |
| 81C81-45  | 7C197-45C   | 76161B-5   | 7C292-35C     | 6167HL-55  | 7C167-45C*  | 1403-55   | 7C167-45C + |
| 81C81-55  | 7C197-45C   | 76641-2    | 7C264-55M     | 6167HL-70  | 7C167-45C*  | 1403LM-35 | 7C167-35M*  |
| 81C84-45  | 7C194-45C   | 76641-5    | 7C264-55C     | 6167L-6    | 7C167-45C*  | 1403M-35  | 7C167-35M + |
| 81C84-55  | 7C194-45C   | 76641A-5   | 7C264-45C     | 6167L-8    | 7C167-45C*  | 1403M-45  | 7C167-45M + |
| 81C86-55  | 7C192-45C + | 7681-2     | 7C282-45M     | 6168H-45   | 7C168-45C + | 1403M-55  | 7C167-45M + |
| 81C86-70  | 7C192-45C + | 7681-5     | 7C282-45C     | 6168H-55   | 7C168-45C + | 1403M-70  | 7C167-45M + |
| 8464L-100 | 7C185-55C + | 7681A-5    | 7C282-45C     | 6168H-70   | 7C168-45C + | 1420-45   | 7C168-35C   |
| 8464L-70  | 7C185-45C + |            |               | 6168HL-45  | 7C168-45C*  | 1420-55   | 7C168-45C   |

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I<sub>CC</sub> and 5 mA on I<sub>SB</sub> ;

+ = meets all performance specs but may not meet I<sub>CC</sub> or I<sub>SB</sub> ;

\* = meets all performance specs except 2V data retention—may not meet I<sub>CC</sub> or I<sub>SB</sub> ;

- = functionally equivalent

| INMOS     | CYPRESS     | INMOS       | CYPRESS        | IDT         | CYPRESS     | IDT       | CYPRESS     |
|-----------|-------------|-------------|----------------|-------------|-------------|-----------|-------------|
| 1420M-55  | 7C168-45M + | 1800-45     | 7C197-45C      | 6116LA70TB  | 7C128-55M*  | 6167SA25  | 7C167-25C + |
| 1420M-70  | 7C168-45M   | 1800M-35    | 7C197-35M      | 6116LA90    | 6116-55C*   | 6167SA35  | 7C167-35C + |
| 1421C-40  | 7C169-40C   | 1800M-45    | 7C197-45M      | 6116LA90B   | 6116-55M*   | 6167SA35B | 7C167-35M + |
| 1423-25   | 7C168-25C + | 1820-25     | 7C194-25C      | 6116LA90T   | 7C128-55C*  | 6167SA45  | 7C167-45C + |
| 1423-35   | 7C168-35C + | 1820-35     | 7C194-35C      | 6116LA90TB  | 7C128-55M*  | 6167SA45B | 7C167-45M + |
| 1423-40   | 7C168-45C + | 1820-45     | 7C194-45C      | 6116S120B   | 6116-55M +  | 6167SA55  | 7C167-45C + |
| 1423M-35  | 7C168-35M*  |             |                | 6116S150B   | 6116-55M +  | 6167SA55B | 7C167-45M + |
| 1423M-45  | 7C168-45M*  |             |                | 6116S55     | 6116-55C +  | 6167SA70B | 7C167-45M + |
| 1423M-55  | 7C168-45M*  | <b>IDT</b>  | <b>CYPRESS</b> | 6116S55B    | 6116-55M +  | 6168L100B | 7C168-45M*  |
| 1433-30   | 7C128-25C + | PREFIX:IDT  | PREFIX:CY      | 6116S70     | 6116-55C +  | 6168L45   | 7C168-45C*  |
| 1433-35   | 7C128-35C + | PREFIX:IDT  | PREFIX:CYM     | 6116S70B    | 6116-55M +  | 6168L55   | 7C168-45C*  |
|           |             | SUFFIX:B    | SUFFIX:B       |             |             |           |             |
|           |             | SUFFIX:D    | SUFFIX:D       | 6116S90     | 6116-55C +  | 6168L55B  | 7C168-45M*  |
| 1433-45   | 7C128-45C + | SUFFIX:F    | SUFFIX:F       | 6116S90B    | 6116-55M +  | 6168L70   | 7C168-45C*  |
| 1433-55   | 7C128-55C + | SUFFIX:L    | SUFFIX:L       | 6116SA120B  | 6116-55M +  | 6168L70B  | 7C168-45M*  |
| 1433M-35  | 7C128-35M + | SUFFIX:P    | SUFFIX:P       | 6116SA120TB | 7C128-55M + | 6168L85   | 7C168-45C*  |
| 1433M-45  | 7C128-45M + | 39C01CB     | 7C901-32M +    | 6116SA35    | 6116-35C +  | 6168L85B  | 7C168-45M*  |
| 1433M-55  | 7C128-55M + | 39C01CC     | 2901CC +       | 6116SA35B   | 6116-45M +  | 6168LA25  | 7C168-25C*  |
| 1600-35   | 7C187-35C   |             |                |             |             |           |             |
|           |             | 39C01CM     | 2901CM +       | 6116SA35T   | 7C128-35C + | 6168LA35  | 7C168-35C*  |
| 1600-45   | 7C187-45C   | 39C01DB     | 7C901-27M +    | 6116SA35TB  | 7C128-35M + | 6168LA35B | 7C168-35M*  |
| 1600-55   | 7C187-45C   | 39C01DC     | 7C901-23C +    | 6116SA45    | 6116-45C +  | 6168LA45  | 7C168-45C*  |
| 1600M-45  | 7C187-45M + | 39C09A      | 7C909-40C +    | 6116SA45B   | 6116-45M +  | 6168LA45B | 7C168-45M*  |
| 1600M-55  | 7C187-45M + | 39C09AB     | 7C909-40M +    | 6116SA45T   | 7C128-45C + | 6168LA55  | 7C168-45C*  |
| 1600M-70  | 7C187-45M + | 39C10B      | 7C910-50C -    | 6116SA45TB  | 7C128-45M + | 6168LA55B | 7C168-45M*  |
|           |             |             |                |             |             |           |             |
| 1601LM-45 | 7C187-45M + | 39C10BB     | 7C910-51M      | 6116SA55    | 6116-55C +  | 6168LA70B | 7C168-45M*  |
| 1601LM-55 | 7C187-45M + | 39C11A      | 7C911-40C +    | 6116SA55B   | 6116-55M +  | 6168S100B | 7C168-45M + |
| 1601LM-70 | 7C187-45M + | 39C11AB     | 7C911-40M +    | 6116SA55T   | 7C128-55C + | 6168S45   | 7C168-45C + |
| 1620-35   | 7C164-35C   | 49C401      | 7C9101-40C -   | 6116SA55TB  | 7C128-55M + | 6168S55   | 7C168-45C + |
| 1620-45   | 7C164-45C + | 49C401      | 7C9101-45M -   | 6116SA70    | 6116-55C +  | 6168S55B  | 7C168-45M + |
| 1620-55   | 7C164-45C + | 6116L120B   | 6116-55M*      | 6116SA70B   | 6116-55M +  | 6168S70   | 7C168-45C   |
|           |             |             |                |             |             |           |             |
| 1620-70   | 7C164-45C + | 6116L150B   | 6116-55M*      | 6116SA70T   | 7C128-55C + | 6168S70B  | 7C168-45M   |
| 1620M-45  | 7C164-45M   | 6116L55     | 6116-55C*      | 6116SA70TB  | 7C128-55M + | 6168S85   | 7C168-45C   |
| 1620M-55  | 7C164-45M   | 6116L55B    | 6116-55M*      | 6116SA90    | 6116-55C +  | 6168S85B  | 7C168-45M   |
| 1620M-70  | 7C164-45M   | 6116L70     | 6116-55C*      | 6116SA90B   | 6116-55M +  | 6168SA25  | 7C168-25C + |
| 1624-35   | 7C166-35C + | 6116L70B    | 6116-55M*      | 6116SA90T   | 7C128-55C + | 6168SA35  | 7C168-35C + |
| 1624-45   | 7C166-45C + | 6116L90     | 6116-55C*      | 6116SA90TB  | 7C128-55M + | 6168SA35B | 7C168-35M + |
|           |             |             |                |             |             |           |             |
| 1624-55   | 7C166-45C + | 6116L90B    | 6116-55M*      | 6167L100B   | 7C167-45M*  | 6168SA45  | 7C168-45C + |
| 1624-70   | 7C166-45C + | 6116LA120B  | 6116-55M*      | 6167L55B    | 7C167-45M*  | 6168SA45B | 7C168-45M + |
| 1624M-45  | 7C166-45M   | 6116LA120TB | 7C128-55M*     | 6167L70B    | 7C167-45M*  | 6168SA55  | 7C168-45C + |
| 1624M-55  | 7C166-45M   | 6116LA35    | 6116-35C*      | 6167L85B    | 7C167-45M*  | 6168SA55B | 7C168-45M + |
| 1624M-70  | 7C166-45M   | 6116LA35B   | 6116-45M*      | 6167LA25    | 7C167-25C*  | 6168SA70B | 7C168-45M + |
| 1625-25   | 7C164-25C   | 6116LA35T   | 7C128-35C*     | 6167LA35    | 7C167-35C*  | 7130L100  | 7C130-55C*  |
|           |             |             |                |             |             |           |             |
| 1625-35   | 7C164-35C   | 6116LA35TB  | 7C128-35M*     | 6167LA35B   | 7C167-35M*  | 7130L100B | 7C130-55M   |
| 1625M-35  | 7C164-45M   | 6116LA45    | 6116-45C*      | 6167LA45    | 7C167-45C*  | 7130L120B | 7C130-55M   |
| 1625M-45  | 7C164-45M   | 6116LA45B   | 6116-45M*      | 6167LA45B   | 7C167-45M*  | 7130L55   | 7C130-55C*  |
| 1630-45   | 7C186-45C + | 6116LA45T   | 7C128-45C*     | 6167LA55    | 7C167-45C*  | 7130L70   | 7C130-55C*  |
| 1630-55   | 7C186-55C + | 6116LA45TB  | 7C128-45M*     | 6167LA55B   | 7C167-45M*  | 7130L90   | 7C130-55C*  |
| 1630-70   | 7C186-55C + | 6116LA55    | 6116-55C*      | 6167LA70B   | 7C167-45M*  | 7130S100  | 7C130-55C   |
|           |             |             |                |             |             |           |             |
| 1630LM-70 | 7C186-55M   | 6116LA55B   | 6116-55M*      | 6167S100B   | 7C167-45M   | 7130S100B | 7C130-55M   |
| 1630M-45  | 7C186-45M   | 6116LA55T   | 7C128-55C*     | 6167S45     | 7C167-45C   | 7130S120B | 7C130-55M   |
| 1630M-55  | 7C186-55M + | 6116LA55TB  | 7C128-55M*     | 6167S55     | 7C167-45C   | 7130S55   | 7C130-55C   |
| 1630M-70  | 7C186-55M   | 6116LA70    | 6116-55C*      | 6167S55B    | 7C167-45M   | 7130S70   | 7C130-55C   |
| 1800-30   | 7C197-25C   | 6116LA70B   | 6116-55M*      | 6167S70B    | 7C167-45M   | 7130S90   | 7C130-55C   |
| 1800-35   | 7C197-35C   | 6116LA70T   | 7C128-55C*     | 6167S85B    | 7C167-45M   | 7132L100  | 7C132-55C*  |

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+ = meets all performance specs but may not meet I<sub>CC</sub> or I<sub>SB</sub>;

\* = meets all performance specs except 2V data retention—may not meet I<sub>CC</sub> or I<sub>SB</sub>;

- = functionally equivalent

| IDT        | CYPRESS     | IDT        | CYPRESS     | IDT         | CYPRESS     | IDT         | CYPRESS     |
|------------|-------------|------------|-------------|-------------|-------------|-------------|-------------|
| 7132L100B  | 7C132-55M*  | 71682L100B | 7C172-45M*  | 71981S55B   | 7C161-45M   | 7202SA-120B | 7C424-65M   |
| 7132L120B  | 7C132-55M*  | 71682LA45  | 7C172-45C*  | 71981S70    | 7C161-45C   | 7202SA-35   | 7C424-30C   |
| 7132L55    | 7C132-55C*  | 71682L55   | 7C172-45C*  | 71981S70B   | 7C161-45M   | 7202SA-40B  | 7C424-40M   |
| 7132L70    | 7C132-55C*  | 71682L55B  | 7C172-45M*  | 71981S85B   | 7C161-45M   | 7202SA-50   | 7C424-40C   |
| 7132L70B   | 7C132-55M*  | 71682L70   | 7C172-45C*  | 71982S35    | 7C162-35C   | 7202SA-50B  | 7C424-40M   |
| 7132L90    | 7C132-55C*  | 71682L70B  | 7C172-45M*  | 71982S35B   | 7C162-35M   | 7202SA-65   | 7C424-65C   |
| 7132L90B   | 7C132-55M*  | 71682LA85B | 7C172-45M*  | 71982S45    | 7C162-45C   | 7202SA-65B  | 7C424-65M   |
| 7132S100   | 7C132-55C + | 71682LA25  | 7C172-25C*  | 71982S45B   | 7C162-45M   | 7202SA-80   | 7C424-65C   |
| 7132S100B  | 7C132-55M + | 71682LA35  | 7C172-35C*  | 71982S55    | 7C162-45C   | 7202SA-80B  | 7C424-65M   |
| 7132S120B  | 7C132-55M + | 71682LA35B | 7C172-35M*  | 71982S55B   | 7C162-45M   | 7210-120B   | 7C510-75M + |
| 7132S55    | 7C132-55C + | 71682LA45  | 7C172-45C*  | 71982S70    | 7C162-45C   | 7210-200B   | 7C510-75M + |
| 7132S70    | 7C132-55C + | 71682LA45B | 7C172-45M*  | 71982S70B   | 7C162-45M   | 7210-55B    | 7C510-55M   |
| 7132S70B   | 7C132-55M + | 71682LA55  | 7C172-45C*  | 71982S85B   | 7C162-45M   | 7210-65B    | 7C510-65M   |
| 7132S90    | 7C132-55C + | 71682LA55B | 7C172-45M*  | 7198S35     | 7C166-35C   | 7210-75B    | 7C510-75M   |
| 7132S90B   | 7C132-55M + | 71682S100B | 7C172-45M + | 7198S35B    | 7C166-35M   | 7210-85B    | 7C510-75M   |
| 7164S35    | 7C186-35C   | 71682S45   | 7C172-45C + | 7198S45     | 7C166-45C   | 7210L-45    | 7C510-45C + |
| 7164S45    | 7C186-45C   | 71682S55   | 7C172-45C + | 7198S45B    | 7C166-45M   | 7210L100    | 7C510-75C + |
| 7164S45B   | 7C186-45M   | 71682S55B  | 7C172-45M + | 7198S55     | 7C166-45C   | 7210L165    | 7C510-75C + |
| 7164S55    | 7C186-55C   | 71682S70   | 7C172-45C + | 7198S55B    | 7C166-45M   | 7210L55     | 7C510-55C + |
| 7164S55B   | 7C186-55M   | 71682S70B  | 7C172-45M + | 7198S70     | 7C166-45C   | 7210L65     | 7C510-65C + |
| 7164S70    | 7C186-55C   | 71682S85B  | 7C172-45M + | 7198S70B    | 7C166-45M   | 7210L75     | 7C510-75C + |
| 7164S70B   | 7C186-55M   | 71682SA25  | 7C172-25C + | 7198S85B    | 7C166-45M   | 7216L120B   | 7C516-75M + |
| 7164S85B   | 7C186-55M   | 71682SA35  | 7C172-35C + | 7201LA-120  | 7C420-65C + | 7216L140    | 7C516-75C + |
| 71681L100B | 7C171-45M*  | 71682SA35B | 7C172-35M + | 7198S85     | 7C166-45C   | 7216L185B   | 7C516-75M + |
| 71681L45   | 7C171-45C*  | 71682SA45  | 7C172-45C + | 7198S85B    | 7C166-45M   | 7216L55     | 7C516-55C + |
| 71681L55   | 7C171-45C*  | 71682SA45B | 7C172-45M + | 7198S70     | 7C166-45C   | 7216L55B    | 7C516-55M   |
| 71681L55B  | 7C171-45M*  | 71682SA55  | 7C172-45C + | 7198S70B    | 7C166-45M   | 7216L65     | 7C516-65C + |
| 71681L70   | 7C171-45C*  | 71682SA55B | 7C172-45M + | 7198S85B    | 7C166-45M   | 7216L65B    | 7C516-65M   |
| 71681L70B  | 7C171-45M*  | 7187S30    | 7C187-25C   | 7201LA-120  | 7C420-65C + | 7216L75     | 7C516-75C + |
| 71681L85B  | 7C171-45M*  | 7187S35    | 7C187-35C   | 7201LA-65B  | 7C420-65M + | 7216L75B    | 7C516-75M   |
| 71681LA25  | 7C171-25C*  | 7187S35B   | 7C187-35M   | 7201LA-80   | 7C420-65C + | 7216L90     | 7C516-75C + |
| 71681LA35  | 7C171-35C*  | 7187S45    | 7C187-45C   | 7201LA-80B  | 7C420-65M + | 7216L90B    | 7C516-75M + |
| 71681LA35B | 7C171-35M*  | 7187S45B   | 7C187-45M   | 7201SA-120  | 7C420-65C   | 7217L120B   | 7C517-75M + |
| 71681LA45  | 7C171-45C*  | 7187S55    | 7C187-45C   | 7201SA-120B | 7C420-65M   | 7217L140    | 7C517-75C + |
| 71681LA45B | 7C171-45M*  | 7187S55B   | 7C187-45M   | 7201SA-35   | 7C420-30C   | 7217L185B   | 7C517-75M + |
| 71681LA55  | 7C171-45C*  | 7187S70    | 7C187-45C   | 7201SA-40B  | 7C420-40M   | 7217L45     | 7C517-45C + |
| 71681LA55B | 7C171-45M*  | 7187S70B   | 7C187-45M   | 7201SA-50   | 7C420-40C   | 7217L55     | 7C517-55C + |
| 71681LA70B | 7C171-45C*  | 7187S85    | 7C187-45C   | 7201SA-50B  | 7C420-40M   | 7217L55B    | 7C517-55M   |
| 71681S100B | 7C171-45M + | 7187S85B   | 7C187-45M   | 7201SA-65   | 7C420-65C   | 7217L65     | 7C517-65C + |
| 71681S45   | 7C171-45C + | 7188S30    | 7C164-25C   | 7201SA-65B  | 7C420-65M   | 7217L65B    | 7C517-65M   |
| 71681S55   | 7C171-45C + | 7188S35    | 7C164-35C   | 7201SA-80   | 7C420-65C   | 7217L75     | 7C517-75C + |
| 71681S55B  | 7C171-45M + | 7188S45    | 7C164-45C   | 7201SA-80B  | 7C420-65M   | 7217L75B    | 7C517-75M   |
| 71681S70   | 7C171-45C + | 7188S45B   | 7C164-45M   | 7202LA-120  | 7C424-65C + | 7217L90     | 7C517-75C + |
| 71681S70B  | 7C171-45M + | 7188S55    | 7C164-45C   | 7202LA-120B | 7C424-65M + | 7217L90B    | 7C517-75M + |
| 71681S85B  | 7C171-45M + | 7188S55B   | 7C164-45M   | 7202LA-35   | 7C424-30C + | 7M4016S35C  | 1641HD-35C  |
| 71681SA25  | 7C171-25C + | 7188S70    | 7C164-45C   | 7202LA-40B  | 7C424-40M + | 7M4016S45C  | 1641HD-45C  |
| 71681SA35  | 7C171-35C + | 7188S70B   | 7C164-45M   | 7202LA-50   | 7C424-40C + | 7M4016S55C  | 1641HD-55C  |
| 71681SA35B | 7C171-35M + | 7188S85B   | 7C164-45M   | 7202LA-50B  | 7C424-40M + | 7M4017S40C  | 1830HD-35C  |
| 71681SA45  | 7C171-45C + | 71981S35   | 7C161-35C   | 7202LA-65   | 7C424-65C + | 7M4017S45C  | 1830HD-45C  |
| 71681SA45B | 7C171-45M + | 71981S35B  | 7C161-35M   | 7202LA-65B  | 7C424-65M + | 7M4017S50C  | 1830HD-45C  |
| 71681SA55  | 7C171-45C + | 71981S45   | 7C161-45C   | 7202LA-80   | 7C424-65C + | 7M4017S50CB | 1830HD-45MB |
| 71681SA55B | 7C171-45M + | 71981S45B  | 7C161-45M   | 7202LA-80B  | 7C424-65M + | 7M4017S55C  | 1830HD-55C  |
| 71681SA70B | 7C171-45M + | 71981S55   | 7C161-45C   | 7202SA-120  | 7C424-65C   | 7M4017S60C  | 1830HD-55C  |

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I<sub>CC</sub> and 5 mA on I<sub>SB</sub> ;

+ = meets all performance specs but may not meet I<sub>CC</sub> or I<sub>SB</sub> ;

\* = meets all performance specs except 2V data retention—may not meet I<sub>CC</sub> or I<sub>SB</sub> ;

- = functionally equivalent

| IDT          | CYPRESS     | IDT            | CYPRESS        | LATTICE  | CYPRESS       | LATTICE    | CYPRESS     |
|--------------|-------------|----------------|----------------|----------|---------------|------------|-------------|
| 7M4017S60CB  | 1830HD-55MB | 8MP624S40S     | 1626PS-35C     | 16K4-25  | 7C168-25C     | 64E4-45    | 7C166-45C   |
| 7M4017S70C   | 1830HD-55C  | 8MP624S45S     | 1626PS-45C     | 16K4-35  | 7C168-35C     | 64E4-55    | 7C166-45C   |
| 7M4017S70CB  | 1830HD-55MB | 8MP624S50S     | 1626PS-45C     | 16K4-35M | 7C168-35M     | 64K1-35    | 7C187-35C   |
| 7M624S30C    | 1621HD-30C  | 8MP624S60S     | 1626PS-45C     | 16K4-45  | 7C168-45C     | 64K1-45    | 7C187-45C   |
| 7M624S35C    | 1621HD-35C  | 8MP824S40S     | 1422PS-35C     | 16K4-45M | 7C168-45M     | 64K1-45M   | 7C187-45M   |
| 7M624S35CB   | 1621HD-35MB | 8MP824S45S     | 1422PS-45C     | 16K8-35  | 7C128-35C +   | 64K1-55    | 7C187-45C   |
| 7M624S45C    | 1621HD-45C  | 8MP824S50S     | 1422PS-45C     | 16K8-55  | 7C128-45C +   | 64K1-55M   | 7C187-45M   |
| 7M624S45CB   | 1621HD-45MB | 8MP824S60S     | 1422PS-55C     | 16V8-25  | PALC16L8-25C  | 64K4-35    | 7C164-35C   |
| 7M624S55C    | 1621HD-45C  | 8MP824S70S     | 1422PS-55C     | 16V8-25  | PALC16R4-25C  | 64K4-45    | 7C164-45C   |
| 7M624S55CB   | 1621HD-45MB |                |                | 16V8-25  | PALC16R6-25C  | 64K4-45M   | 7C164-45M   |
| 7M624S65C    | 1621HD-45C  |                |                | 16V8-25  | PALC16R8-25C  | 64K4-55    | 7C164-45C   |
| 7M624S65CB   | 1621HD-45MB | <b>INTEL</b>   | <b>CYPRESS</b> |          |               |            |             |
| 7MC400S25CV  | 1611HV-25C  | PREFIX:D       | SUFFIX:D       | 16V8-25L | PALC16L8-25C  | 64K4-55M   | 7C164-45M   |
| 7MC400S30CV  | 1611HV-30C  | PREFIX:L       | SUFFIX:L       | 16V8-25L | PALC16R4-25C  | 64K8-35    | 7C186-35C   |
| 7MC400S35CV  | 1611HV-35C  | PREFIX:P       | SUFFIX:P       | 16V8-25L | PALC16R6-25C  | 64K8-45    | 7C186-45C   |
| 7MC400S45CV  | 1611HV-45C  | SUFFIX:/B      | SUFFIX:B       | 16V8-25L | PALC16R8-25C  | 64K8-45    | 7C264-45C   |
| 7MC400S55CV  | 1611HV-45C  | 2147H          | 2147-55C       | 16V8-25Q | PALC16L8L-25C | 64K8-45M   | 7C186-45M   |
|              |             | 2147H-1        | 2147-35C       | 16V8-25Q | PALC16R4L-25  | 64K8-55    | 7C186-55C   |
| 7MC4032S25CV | 1822HV-25C  | 2147H-2        | 2147-45C       | 16V8-25Q | PALC16R6L-25  | 64K8-55    | 7C264-55C   |
| 7MC4032S30CV | 1822HV-30C  | 2147H-3        | 2147-55C       | 16V8-25Q | PALC16R8L-25  | 64K8-55M   | 7C186-45M   |
| 7MC4032S40CV | 1822HV-35C  | 2147HL         | 7C147-45C      | 16V8-30  | PALC16L8-30M  | 64K8-70    | 7C264-55C   |
| 7MC4032S50CV | 1822HV-45C  | 2148H          | 2148-55C       | 16V8-30  | PALC16R4-30M  | L1010-45   | 7C510-45C + |
| 7MP400L100S  | 1461PS-100C | 2148H-2        | 2148-45C       | 16V8-30  | PALC16R6-30M  | L1010-65   | 7C510-65C + |
| 7MP400L85S   | 1461PS-85C  | 2148H-3        | 2148-55C       | 16V8-30  | PALC16R8-30M  | L1010-65B  | 7C510-65M + |
| 7MP400S45S   | 1460PS-45C  | 2148HL         | 21L48-55C      | 16V8-30L | PALC16L8-30M  | L1010-90   | 7C510-75C + |
| 7MP400S55S   | 1460PS-55C  | 2148HL-3       | 21L48-55C      | 16V8-30L | PALC16R4-30M  | L1010-90B  | 7C510-75M + |
| 7MP400S70S   | 1460PS-70C  | 2149H          | 2149-55C       | 16V8-30L | PALC16R6-30M  |            |             |
| 8M624S45C    | 1620HD-45C  | 2149H-1        | 2149-35C       | 16V8-30L | PALC16R8-30M  |            |             |
| 8M624S50C    | 1620HD-45C  | 2149H-2        | 2149-45C       | 16V8-30Q | PALC16L8-30M  |            |             |
| 8M624S50CB   | 1620HD-45MB | 2149H-3        | 2149-55C       | 16V8-30Q | PALC16R4-30M  |            |             |
| 8M624S60C    | 1620HD-55C  | 2149HL         | 21L49-55C      | 16V8-30Q | PALC16R6-30M  | 5C1601-25C | 7C167A-25C  |
| 8M624S60CB   | 1620HD-55MB | 51C66-25       | 7C167-25C -    | 16V8-30Q | PALC16R8-30M  | 5C1601-25M | 7C167A-25M  |
| 8M624S70C    | 1620HD-55C  | 51C66-30       | 7C167-25C -    | 16V8-35  | PALC16L8-35C  | 5C1601-35C | 7C167A-35C  |
| 8M624S70CB   | 1620HD-55MB | 51C66-35       | 7C167-25C -    | 16V8-35  | PALC16R4-35C  | 5C1601-35M | 7C167A-35M  |
| 8M656S40C    | 1610HD-35C  | 51C66-35L      | 7C167-25C -    | 16V8-35  | PALC16R6-35C  | 5C1601-45C | 7C167A-45C  |
| 8M656S50C    | 1610HD-50C  | 51C67-30       | 7C167-25C +    | 16V8-35  | PALC16R8-35C  | 5C1601-45M | 7C167A-45M  |
| 8M656S60CB   | 1610HD-50MB | 51C67-35       | 7C167-35C +    | 16V8-35L | PALC16L8-35C  | 5C1604-20C | 7C168A-20C  |
| 8M656S70C    | 1610HD-50C  | 51C67-35L      | 7C167-35C +    | 16V8-35L | PALC16R4-35C  | 5C1604-25C | 7C168A-25C  |
| 8M656S70CB   | 1610HD-50MB | 51C68-30       | 7C168-25C +    | 16V8-35L | PALC16R6-35C  | 5C1604-25M | 7C168A-25M  |
| 8M824L100C   | 1421HD-85C  | 51C68-35       | 7C168-35C +    | 16V8-35L | PALC16R8-35C  | 5C1604-35C | 7C168A-35C  |
| 8M824L100N   | 1421HD-85C  | M2147H-3       | 7C169-40M      | 16V8-35Q | PALC16L8L-35C | 5C1604-35M | 7C168A-35M  |
| 8M824L85C    | 1421HD-85C  | M2148H         | 2148-55M       | 16V8-35Q | PALC16R4L-35C | 5C1604-45C | 7C168A-45C  |
| 8M824L85N    | 1421HD-85C  | M2149H         | 2149-55M       | 16V8-35Q | PALC16R6L-35C | 5C1604-45M | 7C168A-45M  |
| 8M824S45C    | 1420HD-45C  | M2149H-2       | 2149-45M       | 16V8-35Q | PALC16R8L-35C | 5C1605-20C | 7C170A-20C  |
| 8M824S45N    | 1420HD-45C  | M2149H-3       | 2149-55M       | 20V8-25  | PLDC20G10-25C | 5C1605-25C | 7C170A-25C  |
| 8M824S50C    | 1420HD-45C  |                |                | 20V8-25L | PLDC20G10-25C | 5C1605-25M | 7C170A-25M  |
| 8M824S50CB   | 1420HD-45MB |                |                | 20V8-25Q | PLDC20G10-25C | 5C1605-35C | 7C170A-35C  |
| 8M824S50N    | 1420HD-45C  |                |                | 20V8-35  | PLDC20G10-30M | 5C1605-35M | 7C170A-35M  |
| 8M824S60C    | 1420HD-55C  | <b>LATTICE</b> | <b>CYPRESS</b> |          |               |            |             |
| 8M824S60CB   | 1420HD-55MB | PREFIX:EE      | PREFIX:CY      | 20V8-35  | PLDC20G10-30M | 5C1605-45C | 7C170A-45C  |
| 8M824S60N    | 1420HD-55C  | PREFIX:GAL     | PREFIX:CY      | 20V8-35L | PLDC20G10-35C | 5C1605-45M | 7C170A-45M  |
| 8M824S70C    | 1421HD-70C  | PREFIX:SR      | PREFIX:CY      | 20V8-35L | PLDC20G10-35C | 5C1606-20C | 7C171A-20C  |
| 8M824S70CB   | 1421HD-70C  | SUFFIX:B       | SUFFIX:B       | 20V8-35L | PLDC20G10-35C | 5C1606-25C | 7C171A-25C  |
| 8M824S70C    | 1421HD-70C  | SUFFIX:D       | SUFFIX:D       | 20V8-35Q | PLDC20G10-30M | 5C1606-25M | 7C171A-25M  |
| 8M824S70CB   | 1420HD-55MB | SUFFIX:L       | SUFFIX:L       | 20V8-35Q | PLDC20G10-35C | 5C1606-25M | 7C171A-25M  |
| 8M824S70N    | 1421HD-70C  | SUFFIX:P       | SUFFIX:P       | 64E4-35  | 7C166-35C     | 5C1606-35C | 7C171A-35C  |

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+ = meets all performance specs but may not meet I<sub>CC</sub> or I<sub>SB</sub>;

\* = meets all performance specs except 2V data retention—may not meet I<sub>CC</sub> or I<sub>SB</sub>;

- = functionally equivalent



# Product Line Cross Reference (Continued)

| MICRON     | CYPRESS    | MICRON            | CYPRESS        | MMI        | CYPRESS   | MMI         | CYPRESS       |
|------------|------------|-------------------|----------------|------------|-----------|-------------|---------------|
| 5C1606-35M | 7C171A-35M | 5C6407-25C        | 7C162-25C      | 5381-2     | 7C282-45M | C57401      | 7C401-10M     |
| 5C1606-45C | 7C171A-45C | 5C6407-25M        | 7C162-25M      | 5381S-1    | 7C281-45M | C57401A     | 7C401-10M     |
| 5C1606-45M | 7C171A-45M | 5C6407-35C        | 7C162-35C      | 5381S-2    | 7C281-45M | C57402      | 7C402-10M     |
| 5C1607-20C | 7C172A-20C | 5C6407-35M        | 7C162-35M      | 53RA1681AS | 7C245-35M | C57402A     | 7C402-10M     |
| 5C1607-25C | 7C172A-25C | 5C6407-45C        | 7C162-45C      | 53RA1681S  | 7C245-45M | C67401A     | 7C401-15C     |
| 5C1607-25M | 7C172A-25M | 5C6407-45M        | 7C162-45M      | 53RA481AS  | 7C225-35M | C67401B     | 7C403-25C     |
| 5C1607-35C | 7C172A-35C | 5C6408-20C        | 7C185-20C      | 53RA481S   | 7C225-40M | C67402      | 7C402-10C     |
| 5C1607-35M | 7C172A-35M | 5C6408-25C        | 7C185-25C      | 53RS1681AS | 7C245-35M | C67402A     | 7C402-15C     |
| 5C1607-45C | 7C172A-45C | 5C6408-25M        | 7C185-25M      | 53RS1681S  | 7C245-45M | C67402B     | 7C404-25C     |
| 5C1607-45M | 7C172A-45M | 5C6408-35C        | 7C185-35C      | 53RS881AS  | 7C235-40M | C67L401     | 7C401-5C      |
| 5C1608-20C | 7C128A-20C | 5C6408-35M        | 7C185-35M      | 53RS881S   | 7C235-40M | C67L401D    | 7C401-15C     |
| 5C1608-25C | 7C128A-25C | 5C6408-45C        | 7C185-45C      | 53S1681    | 7C292-50M | C67L402D    | 7C402-15C     |
| 5C1608-25M | 7C128A-25M | 5C6408-45M        | 7C185-45M      | 53S1681AS  | 7C291-35M | PAL12110C   | PLDC20G10-35C |
| 5C1608-35C | 7C128A-35C | 5C6408-55C        | 7C128-55C      | 53S1681S   | 7C291-50M | PAL12110M   | PLDC20G10-40M |
| 5C1608-35M | 7C128A-35M | 5C6408-55M        | 7C185-55M      | 53S881     | 7C282-45M | PAL14L8C    | PLDC20G10-35C |
| 5C1608-45C | 7C128A-45C |                   |                | 53S881A    | 7C282-45M | PAL14L8M    | PLDC20G10-40M |
| 5C1608-45M | 7C128A-45M |                   |                | 53S881AS   | 7C281-45M | PAL16L6C    | PLDC20G10-35C |
|            |            | <b>MITSUBISHI</b> | <b>CYPRESS</b> |            |           |             |               |
| 5C1608-55C | 7C128A-55C | PREFIX:M5M        | PREFIX:CY      | 53S881S    | 7C281-45M | PAL16L6M    | PLDC20G10-40M |
| 5C1608-55M | 7C128A-55M | SUFFIX:AP         | SUFFIX:L       | 57401      | 7C401-10M | PAL16L8A-2C | PALC16L8-35C  |
| 5C2561-25C | 7C197-25C  | SUFFIX:FP         | SUFFIX:F       | 57401A     | 7C401-10M | PAL16L8A-2M | PALC16L8-40M  |
| 5C2561-35C | 7C197-35C  | SUFFIX:K          | SUFFIX:D       | 57402      | 7C402-10M | PAL16L8A-4C | PALC16L8L-35C |
| 5C2561-35M | 7C197-35M  | SUFFIX:P          | SUFFIX:P       | 57402A     | 7C402-10M | PAL16L8A-4M | PALC16L8-40M  |
| 5C2561-45C | 7C197-45C  | 21C67P-35         | 7C167-35C      | 6381-1     | 7C282-45C | PAL16L8AC   | PALC16L8-25C  |
| 5C2561-45M | 7C197-45M  | 21C67P-45         | 7C167-45C      | 6381-2     | 7C282-45C | PAL16L8AM   | PALC16L8-30M  |
| 5C6401-20C | 7C187-20C  | 21C67P-55         | 7C167-45C      | 6381S-1    | 7C281-45C | PAL16L8B-2C | PALC16L8-25C  |
| 5C6401-25C | 7C187-25C  | 21C68P-35         | 7C168-35C      | 6381S-2    | 7C281-45C | PAL16L8B-2M | PALC16L8-30M  |
| 5C6401-25M | 7C187-25M  | 21C68P-45         | 7C168-45C      | 63RA1681AS | 7C245-35C | PAL16L8B-4C | PALC16L8L-35C |
| 5C6401-35C | 7C187-35C  | 21C68P-55         | 7C168-45C      | 63RA1681S  | 7C245-35C | PAL16L8B-4M | PALC16L8-40M  |
| 5C6401-35M | 7C187-35M  | 5165L-100         | 7C186-55C+     | 63RA481AS  | 7C225-25C | PAL16L8BM   | PALC16L8-20M  |
| 5C6401-45C | 7C187-45C  | 5165L-120         | 7C186-55C+     | 63RA481S   | 7C225-30C | PAL16L8C    | PALC16L8-35C  |
| 5C6401-45M | 7C187-45M  | 5165L-70          | 7C186-55C+     | 63RS1681AS | 7C245-35C | PAL16L8D-4C | PALC16L8L-25C |
| 5C6404-20C | 7C164-20C  | 5165P-100         | 7C186-55C+     | 63RS1681S  | 7C245-35C | PAL16L8D-4M | PALC16L8-30M  |
| 5C6404-25C | 7C164-25C  | 5165P-120         | 7C186-55C+     | 63RS881AS  | 7C235-30C | PAL16L8M    | PALC16L8-40M  |
| 5C6404-25M | 7C164-25M  | 5165P-70          | 7C186-55C+     | 63RS881S   | 7C235-30C | PAL16R4A-2C | PALC16R4-35C  |
| 5C6404-35C | 7C164-35C  | 5178P-45          | 7C186-45C+     | 63S1681    | 7C292-50C | PAL16R4A-2M | PALC16R4-40M  |
| 5C6404-35M | 7C164-35M  | 5178P-55          | 7C186-55C+     | 63S1681A   | 7C292-35C | PAL16R4A-4C | PALC16R4L-35C |
| 5C6404-45C | 7C164-45C  | 5187P-25          | 7C187-25C      | 63S1681AS  | 7C291-35C | PAL16R4A-4M | PALC16R4-40M  |
| 5C6404-45M | 7C164-45M  | 5187P-35          | 7C187-35C      | 63S1681S   | 7C291-50C | PAL16R4AC   | PALC16R4-25C  |
| 5C6405-20C | 7C166-20C  | 5187P-45          | 7C187-45C      | 63S881     | 7C281-45C | PAL16R4AM   | PALC16R4-30M  |
| 5C6405-25C | 7C166-25C  | 5187P-55          | 7C187-45C      | 63S881S    | 7C281-45C | PAL16R4B-2C | PALC16R4-25C  |
| 5C6405-25M | 7C166-25M  | 5188P-25          | 7C164-25C      | 63S881A    | 7C281-30C | PAL16R4B-2M | PALC16R4-30M  |
| 5C6405-35C | 7C166-35C  | 5188P-35          | 7C164-35C      | 63S881A    | 7C282-30C | PAL16R4B-4C | PALC16R4L-35C |
| 5C6405-35M | 7C166-35M  | 5188P-45          | 7C164-45C      | 67401      | 7C401-10C | PAL16R4B-4M | PALC16R4-40M  |
| 5C6405-45C | 7C166-45C  | 5188P-55          | 7C164-45C      | 67401A     | 7C401-15C | PAL16R4BM   | PALC16R4-20M  |
| 5C6405-45M | 7C166-45M  |                   |                | 67401B     | 7C403-25C | PAL16R4C    | PALC16R4-35C  |
| 5C6406-20C | 7C161-20C  |                   |                | 67401D     | 7C403-25C | PAL16R4D-4C | PALC16R4L-25C |
| 5C6406-25C | 7C161-25C  | <b>MMI</b>        | <b>CYPRESS</b> | 67402      | 7C402-10C | PAL16R4M    | PALC16R4-40M  |
|            |            | SUFFIX:883B       | SUFFIX:B       |            |           |             |               |
| 5C6406-25M | 7C161-25M  | SUFFIX:F          | SUFFIX:F       | 67402A     | 7C402-15C | PAL16R6A-2C | PALC16R6-35C  |
| 5C6406-35C | 7C161-35C  | SUFFIX:J          | SUFFIX:D       | 67402B     | 7C402-25C | PAL16R6A-2M | PALC16R6-40M  |
| 5C6406-35M | 7C161-35M  | SUFFIX:L          | SUFFIX:L       | 67402D     | 7C404-25C | PAL16R6A-4C | PALC16R6L-35C |
| 5C6406-45C | 7C161-45C  | SUFFIX:N          | SUFFIX:P       | 67411      | 7C403-25C | PAL16R6A-4M | PALC16R6-40M  |
| 5C6406-45M | 7C161-45M  | SUFFIX:SHRP       | SUFFIX:B       | 67412      | 7C402-25C | PAL16R6AC   | PALC16R6-25C  |
| 5C6407-20C | 7C162-20C  | 5381-1            | 7C282-45M      | 67L402     | 7C402-10C | PAL16R6AM   | PALC16R6-30M  |

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I<sub>CC</sub> and 5 mA on I<sub>SB</sub> ;

+ = meets all performance specs but may not meet I<sub>CC</sub> or I<sub>SB</sub> ;

\* = meets all performance specs except 2V data retention—may not meet I<sub>CC</sub> or I<sub>SB</sub> ;

- = functionally equivalent

| MMI         | CYPRESS       | MMI             | CYPRESS        | MOTOROLA | CYPRESS    | NATIONAL    | CYPRESS       |
|-------------|---------------|-----------------|----------------|----------|------------|-------------|---------------|
| PAL16R6B-2C | PALC16R6-25C  | PAL20R8M        | PLDC20G10-40M  | 2018-45  | 7C128-45C  | PREFIX:NMC  | PREFIX:CY     |
| PAL16R6B-2M | PALC16R6-30M  | PALC22V10/A     | PALC22V10-35C  | 2167H-35 | 7C167-35C  | SUFFIX:J    | SUFFIX:D      |
| PAL16R6B-4C | PALC16R6L-35C | PLE10P8C        | 7C281-30C      | 2167H-45 | 7C167-45C  | SUFFIX:N    | SUFFIX:P      |
| PAL16R6B-4M | PALC16R6-40M  | PLE10P8C        | 7C282-30C      | 2167H-55 | 7C167-45C  | 100422-10C  | 100E422-7C    |
| PAL16R6BM   | PALC16R6-20M  | PLE10P8M        | 7C281-45M      | 6147-55  | 7C147-45C* | 100422-5C   | 100E422-5C    |
| PAL16R6C    | PALC16R6-35C  | PLE10P8M        | 7C282-45M      | 6147-70  | 7C147-45C* | 100422A-7C  | 100E422-7C    |
| PAL16R6D-4C | PALC16R6L-25C | PLE10R8C        | 7C235-30C-     | 6164-45  | 7C186-45C  | 100422AC    | 100E422-7C    |
| PAL16R6M    | PALC16R6-40M  | PLE10R8M        | 7C235-40M-     | 6164-55  | 7C186-55C  | 100474A-10C | 100E474-7C    |
| PAL16R8A-2C | PALC16R8-35C  | PLE11P8C        | 7C291-35C      | 6164-70  | 7C186-55C  | 100474A-8C  | 100E474-7C    |
| PAL16R8A-2M | PALC16R8-40M  | PLE11P8M        | 7C291-35M      | 6168-35  | 7C168-35C+ | 10422-10C   | 10E422-7C     |
| PAL16R8A-4C | PALC16R8L-35C | PLE11RA8C       | 7C245-35C-     | 6168-45  | 7C168-45C+ | 10422-5C    | 10E422-5C     |
| PAL16R8A-4M | PALC16R8-40M  | PLE11RA8M       | 7C245-35M-     | 6168-55  | 7C168-45C+ | 10422A-7C   | 10E422-7C     |
| PAL16R8AC   | PALC16R8-25C  | PLE11RS8C       | 7C245-35C-     | 6168-70  | 7C168-45C+ | 10422AC     | 10E422-7C     |
| PAL16R8AM   | PALC16R8-30M  | PLE11RS8M       | 7C245-35M-     | 61L47-55 | 7C147-45C* | 10474A-10C  | 10E474-7C     |
| PAL16R8B-2C | PALC16R8-25C  | PLE9R8C         | 7C225-30C      | 61L47-70 | 7C147-45C* | 10474A-8C   | 10E474-7C     |
| PAL16R8B-2M | PALC16R8-30M  | PLE9R8M         | 7C225-35M      | 61L64-45 | 7C186-45C  | 12L10C      | PLDC20G10-35C |
| PAL16R8B-4C | PALC16R8L-35C |                 |                | 61L64-55 | 7C186-55C  | 14L8C       | PLDC20G10-35C |
| PAL16R8B-4M | PALC16R8-40M  | <b>MOSAIC</b>   | <b>CYPRESS</b> | 61L64-70 | 7C186-55C  | 14L8M       | PLDC20G10-40M |
| PAL16R8BM   | PALC16R8-20M  | PREFIX:MS       | PREFIX:CYM     | 6268-25  | 7C168-25C  | 16L6C       | PLDC20G10-35C |
| PAL16R8C    | PALC16R8-35C  | 8128SC-100      | 1420HD-85C     | 6268-35  | 7C168-35C  | 16L6M       | PLDC20G10-40M |
| PAL16R8D-4C | PALC16R8L-25C | 8128SC-100      | 1421HD-85C     | 6269-25  | 7C169-25C  | 18L4C       | PLDC20G10-35C |
| PAL16R8M    | PALC16R8-40M  | 8128SC-45       | 1420HD-45C     | 6269-35  | 7C169-35C  | 18L4M       | PLDC20G10-40M |
| PAL18L4C    | PLDC20G10-35C | 8128SC-55       | 1420HD-55C     | 6270-25  | 7C170-25C  | 20L2M       | PLDC20G10-40M |
| PAL18L4M    | PLDC20G10-40M | 8128SC-70       | 1420HD-70C     | 6270-35  | 7C170-35C  | 2147H       | 2147-55C      |
| PAL20L10AC  | PLDC20G10-35C | 8128SC-70       | 1421HD-70C     | 6270-45  | 7C170-45C  | 2147H       | 2147-55M      |
| PAL20L10AM  | PLDC20G10-30M |                 |                | 6287-25  | 7C187-25C  | 2147H-1     | 2147-35C      |
| PAL20L10C   | PLDC20G10-35C | <b>MOSTEK</b>   | <b>CYPRESS</b> | 6287-35  | 7C187-35C  | 2147H-2     | 2147-45C      |
| PAL20L10M   | PLDC20G10-40M | PREFIX:ET       | PREFIX:CY      | 6287-45  | 7C187-45C  | 2147H-3     | 2147-55C      |
| PAL20L2C    | PLDC20G10-35C | PREFIX:MK       | PREFIX:CY      | 6288-25C | 7C164-25C  | 2147H-3     | 2147-55M      |
| PAL20L2M    | PLDC20G10-40M | PREFIX:TS       | PREFIX:CY      | 6288-35C | 7C164-35C  | 2147H-3L    | 7C147-45C     |
| PAL20L8A-2C | PLDC20G10-35C | SUFFIX:N        | SUFFIX:P       | 6288-35M | 7C164-35M  | 2148H       | 2148-55C      |
| PAL20L8A-2M | PLDC20G10-40M | SUFFIX:P        | SUFFIX:D       | 6288-45M | 7C164-45M  | 2148H-2     | 2148-45C      |
| PAL20L8AC   | PLDC20G10-25C | 41H67-25        | 7C167-25C+     | 6290-25C | 7C166-25C  | 2148H-3     | 2148-55C      |
| PAL20L8AM   | PLDC20G10-30M | 41H67-35        | 7C167-35+      | 6290-35C | 7C166-35C  | 2148H-3L    | 21L48-55C     |
| PAL20L8C    | PLDC20G10-35C | 41H68-25        | 7C168-25C+     | 6290-35M | 7C166-35M  | 2148HL      | 21L48-55C     |
| PAL20L8M    | PLDC20G10-40M | 41H68-35        | 7C168-35C+     | 6290-45C | 7C166-45C  | 2901A-1C    | 7C901-31C     |
| PAL20R4A-2C | PLDC20G10-35C | 41H69-25        | 7C169-25       | 6290-45M | 7C166-45M  | 2901A-1M    | 7C901-32M     |
| PAL20R4A-2M | PLDC20G10-40M | 41H69-35        | 7C169-35C      | 62L87-25 | 7C187-25C  | 2901A-2C    | 7C901-31C     |
| PAL20R4AC   | PLDC20G10-25C | 41L67-25        | 7C167-25C-     | 62L87-35 | 7C187-35C+ | 2901A-2M    | 7C901-32M     |
| PAL20R4AM   | PLDC20G10-30M | 41L67-35        | 7C167-35-      | 7681     | 7C282-45C  | 2901AC      | 7C901-31C     |
| PAL20R4C    | PLDC20G10-35C | 41L67-45        | 7C167-35-      | 7681A    | 7C282-45C  | 2901AM      | 7C901-32M     |
| PAL20R4M    | PLDC20G10-40M |                 |                | 93422    | 93422C     | 2909AC      | 2909AC        |
| PAL20R6A-2C | PLDC20G10-35C | <b>MOTOROLA</b> | <b>CYPRESS</b> | 93422    | 93422M     | 2909AM      | 2909M         |
| PAL20R6A-2M | PLDC20G10-40M | PREFIX:MCM      | PREFIX:CY      | 93422A   | 93422AC    | 2911AC      | 2911AC        |
| PAL20R6AC   | PLDC20G10-25C | SUFFIX:P        | SUFFIX:P       | 93422A   | 93422AM    | 2911AM      | 2911M         |
| PAL20R6AM   | PLDC20G10-30M | SUFFIX:S        | SUFFIX:D       | 93L422   | 93L422C    | 54S189      | 54S189M       |
| PAL20R6C    | PLDC20G10-35C | SUFFIX:Z        | SUFFIX:L       | 93L422   | 93L422M    | 54S189A     | 7C189-25M     |
| PAL20R6M    | PLDC20G10-40M |                 |                | 93L422A  | 93L422AC   | 74S189      | 74S189C       |
| PAL20R8A-2C | PLDC20G10-35C | 10422-10C       | 10E422-7C      | 93L422A  | 93L422AM   | 74S189A     | 27S03AC       |
| PAL20R8A-2M | PLDC20G10-40M | 1423-45         | 7C168-45C+     |          |            | 75S07       | 7C190-25M     |
| PAL20R8AC   | PLDC20G10-25C | 2016H-45        | 6116-45C       |          |            | 75S07A      | 27S07AM       |
| PAL20R8AM   | PLDC20G10-30M | 2016H-55        | 6116-55C       |          |            | 77S181      | 7C282-45M     |
| PAL20R8C    | PLDC20G10-35C | 2016H-70        | 6116-55C       |          |            | 77S181      | 7C282-45M     |
|             |               | 2018-35         | 7C128-35C      |          |            |             |               |

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 + = meets all performance specs but may not meet I<sub>CC</sub> or I<sub>SB</sub> ;  
 \* = meets all performance specs except 2V data retention—may not meet I<sub>CC</sub> or I<sub>SB</sub> ;  
 - = functionally equivalent

| NATIONAL       | CYPRESS      | NATIONAL    | CYPRESS       | NATIONAL    | CYPRESS       | NEC      | CYPRESS     |
|----------------|--------------|-------------|---------------|-------------|---------------|----------|-------------|
| 77S181A        | 7C282-45M    | PAL16L8A2M  | PALC16L8-40M  | PAL20L8M    | PLDC20G10-40M | 429-1    | 7C292-50C   |
| 77S191         | 7C292-50M    | PAL16L8AC   | PALC16L8-25C  | PAL20R4AC   | PLDC20G10-25C | 429-2    | 7C292-50C   |
| 77S191A        | 7C292-50M    | PAL16L8AM   | PALC16L8-30M  | PAL20R4AM   | PLDC20G10-30M | 429-3    | 7C292-35C   |
| 77S191B        | 7C292-50M    | PAL16L8B2C  | PALC16L8-25C  | PAL20R4BC   | PLDC20G10-25C | 4311-45  | 7C167-45C   |
| 77S281         | 7C281-45M    | PAL16L8B2M  | PALC16L8-30M  | PAL20R4BM   | PLDC20G10-30M | 4311-55  | 7C167-45C   |
| 77S281A        | 7C281-45M    | PAL16L8B4C  | PALC16L8L-35C | PAL20R4C    | PLDC20G10-35C | 4361-40  | 7C187-35C   |
| 77S291         | 7C291-50M    | PAL16L8B4M  | PALC16L8-40M  | PAL20R4M    | PLDC20G10-40M | 4361-45  | 7C187-45C   |
| 77S291A        | 7C291-50M    | PAL16L8BM   | PALC16L8-20M  | PAL20R6AC   | PLDC20G10-25C | 4361-55  | 7C187-45C   |
| 77S291B        | 7C291-50M    | PAL16L8C    | PALC16L8-35C  | PAL20R6AM   | PLDC20G10-30M | 4361-70  | 7C187-45C   |
| 77S401         | 7C401-10M    | PAL16L8M    | PALC16L8-40M  | PAL20R6BC   | PLDC20G10-25C | 4362-45  | 7C164-45C   |
| 77S401A        | 7C401-10M    | PAL16R4A2C  | PALC16R4-35C  | PAL20R6BM   | PLDC20G10-30M | 4362-55  | 7C164-45C   |
| 77S402         | 7C402-10M    | PAL16R4A2M  | PALC16R4-40M  | PAL20R6C    | PLDC20G10-35C | 4362-70  | 7C164-45C   |
| 77S402A        | 7C402-10M    | PAL16R4AC   | PALC16R4-25C  | PAL20R6M    | PLDC20G10-40M | 4363-45  | 7C166-45C   |
| 77SR181        | 7C235-40M    | PAL16R4AM   | PALC16R4-30M  | PAL20R8AC   | PLDC20G10-25C | 4363-55  | 7C166-45C   |
| 77SR25         | 7C225-40M    | PAL16R4B2C  | PALC16R4-25C  | PAL20R8AM   | PLDC20G10-30M | 4363-70  | 7C166-45C   |
| 77SR25B        | 7C225-40M    | PAL16R4B2M  | PALC16R4-30M  | PAL20R8BC   | PLDC20G10-25C |          |             |
| 77SR476        | 7C225-40M    | PAL16R4B4C  | PALC16R4L-35C | PAL20R8BM   | PLDC20G10-30M |          |             |
| 77SR476B       | 7C225-40M    | PAL16R4B4M  | PALC16R4-40M  | PAL20R8C    | PLDC20G10-35C |          |             |
| 85S07          | 27S07C       | PAL16R4BM   | PALC16R4-20M  | PAL20R8M    | PLDC20G10-40M |          |             |
| 85S07A         | 27S07AC      | PAL16R4C    | PALC16R4-35C  |             |               |          |             |
| 85S07A         | 7C128-45C +  | PAL16R4M    | PALC16R4-40M  |             |               |          |             |
| 87LS181        | 7C282-45C    | PAL16R6A2C  | PALC16R6-25C  | NEC         | CYPRESS       | PREFIX:R | PREFIX:CY   |
| 87S181         | 7C282-45C    | PAL16R6A2M  | PALC16R6-40M  | PREFIX:nPD  | PREFIX:CY     | SUFFIX:B | SUFFIX:B    |
|                |              |             |               | SUFFIX:C    | SUFFIX:P      | SUFFIX:D | SUFFIX:D    |
|                |              |             |               |             |               | SUFFIX:F | SUFFIX:F    |
|                |              |             |               |             |               | SUFFIX:L | SUFFIX:L    |
|                |              |             |               |             |               | SUFFIX:S | SUFFIX:S    |
| 87S191         | 7C292-50C    | PAL16R6AC   | PALC16R6-25C  | SUFFIX:D    | SUFFIX:D      | 29631AC  | 7C282-45C   |
| 87S191A        | 7C292-35C    | PAL16R6AM   | PALC16R6-30M  | SUFFIX:K    | SUFFIX:L      | 29631AM  | 7C282-45M   |
| 87S191B        | 7C292-35C    | PAL16R6B2C  | PALC16R6-25C  | SUFFIX:L    | SUFFIX:F      | 29631ASC | 7C281-45C   |
| 87S281         | 7C281-45C    | PAL16R6B2M  | PALC16R6-30M  | 100422-10C  | 100E422-7C    | 29631ASM | 7C281-45M   |
| 87S281A        | 7C281-45C    | PAL16R6B4C  | PALC16R6L-35C | 100422-5C   | 100E422-5C    | 29631C   | 7C282-45C   |
| 87S291         | 7C291-50C    | PAL16R6B4M  | PALC16R6-40M  | 100422-7C   | 100E422-7C    | 29631M   | 7C282-45M   |
| 87S291A        | 7C291-35C    | PAL16R6BM   | PALC16R6-20M  | 100474-10C  | 100E474-7C    | 29631SC  | 7C281-45C   |
| 87S291B        | 7C291-35C    | PAL16R6C    | PALC16R6-35C  | 100474-3C   | 100E474-3C    | 29631SM  | 7C281-45M   |
| 87S401         | 7C401-10C    | PAL16R6M    | PALC16R6-40M  | 100474-4.5C | 100E474-3C    | 29633AC  | 7C282-45C + |
| 87S401A        | 7C401-15C    | PAL16R8A2C  | PALC16R8-35C  | 100474-6C   | 100E474-5C    | 29633AM  | 7C282-45M + |
| 87S402         | 7C402-10C    | PAL16R8A2M  | PALC16R8-40M  | 100474-8C   | 100E474-7C    | 29633ASC | 7C281-45C + |
| 87S402A        | 7C402-15C    | PAL16R8AC   | PALC16R8-25C  | 10422-10C   | 10E422-7C     | 29633ASM | 7C281-45M + |
| 87SR181        | 7C235-30C    | PAL16R8AM   | PALC16R8-30M  | 10422-5C    | 10E422-5C     | 29633C   | 7C282-45C + |
| 87SR25         | 7C225-40C    | PAL16R8B2C  | PALC16R8-25C  | 10422-7C    | 10E422-7C     | 29633M   | 7C282-45M + |
| 87SR25B        | 7C225-30C    | PAL16R8B2M  | PALC16R8-30M  | 10474-10C   | 10E474-7C     | 29633SC  | 7C281-45C + |
| 87SR476        | 7C225-40C    | PAL16R8B4C  | PALC16R8L-35C | 10474-3C    | 10E474-3C     | 29633SM  | 7C281-45M + |
| 87SR476B       | 7C225-30C    | PAL16R8B4M  | PALC16R8-40M  | 10474-4.5C  | 10E474-3C     | 29681AC  | 7C292-50C   |
| PAL10016P4-2.5 | 100E302-2.5C | PAL16R8BM   | PALC16R8-20M  | 10474-6C    | 10E474-5C     | 29681AM  | 7C292-50M   |
| PAL10016P4-4C  | 100E302-4C   | PAL16R8C    | PALC16R8-35C  | 10474-8C    | 10E474-7C     | 29681ASC | 7C291-50C   |
| PAL10016P4-6C  | 100E302-6C   | PAL16R8M    | PALC16R8-40M  | 2147-2      | 2147-55C      | 29681ASM | 7C291-50M   |
| PAL10016P8-3C  | 100E301-3C   | PAL20L10B2C | PLDC20G10-25C | 2147-3      | 2147-55C      | 29681C   | 7C292-50C   |
| PAL10016P8-4C  | 100E301-4C   | PAL20L10B2M | PLDC20G10-30M | 2147A-25    | 7C147-25C     | 29681M   | 7C292-50M   |
| PAL10016P8-6C  | 100E301-6C   | PAL20L10C   | PLDC20G10-35C | 2147A-35    | 2147-35C      | 29681SC  | 7C291-50C   |
| PAL1016P4-2.5C | 10E302-2.5C  | PAL20L10M   | PLDC20G10-40M | 2147A-45    | 2147-45C      | 29681SM  | 7C291-50M   |
| PAL1016P4-4C   | 10E302-4C    | PAL20L2C    | PLDC20G10-35C | 2149        | 2149-55C      | 29683AC  | 7C292-50C + |
| PAL1016P4-6C   | 10E302-6C    | PAL20L8AC   | PLDC20G10-25C | 2149-1      | 2149-45C      | 29683AM  | 7C292-50M + |
| PAL1016P8-3C   | 10E301-3C    | PAL20L8AM   | PLDC20G10-30M | 2149-2      | 2149-35C      | 29683ASC | 7C291-50C + |
| PAL1016P8-4C   | 10E301-4C    | PAL20L8BC   | PLDC20G10-25C | 2167-2      | 7C167-45C     | 29683ASM | 7C291-50M + |
| PAL1016P8-6C   | 10E301-6C    | PAL20L8BM   | PLDC20G10-30M | 2167-3      | 7C167-45C     | 29683C   | 7C292-50C + |
| PAL16L8A2C     | PALC16L8-35C | PAL20L8C    | PLDC20G10-35C | 429         | 7C292-50C     | 29683M   | 7C292-50M + |

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 + = meets all performance specs but may not meet I<sub>CC</sub> or I<sub>SB</sub> ;  
 \* = meets all performance specs except 2V data retention—may not meet I<sub>CC</sub> or I<sub>SB</sub> ;  
 - = functionally equivalent

| <b>RAYTHEON</b>  | <b>CYPRESS</b> | <b>TI</b>    | <b>CYPRESS</b> | <b>TI</b>    | <b>CYPRESS</b> | <b>TOSHIBA</b> | <b>CYPRESS</b> |
|------------------|----------------|--------------|----------------|--------------|----------------|----------------|----------------|
| 29683SC          | 7C291-50C +    | PREFIX:TBP   | PREFIX:CY      | HCT9510E     | 7C510-75C +    | PREFIX:P       | SUFFIX:P       |
| 29683SM          | 7C291-50M +    | PREFIX:TIB   | PREFIX:CY      | HCT9510E-10  | 7C510-75C +    | PREFIX:TMM     | PREFIX:CY      |
| 29VP864DB        | 7C264-55M      | SUFFIX:F     | SUFFIX:F       | HCT9510M     | 7C510-75M +    | SUFFIX:D       | SUFFIX:D       |
| 29VP864SB        | 7C263-55M      | SUFFIX:J     | SUFFIX:L       | PAL16L8-20M  | PALC16L8-20M   | 2015A-10       | 7C128-55C +    |
| 29VS864SB        | 7C261-55M      | SUFFIX:N     | SUFFIX:D       | PAL16L8-25C  | PALC16L8-25C   | 2015A-12       | 7C128-55C +    |
| 39VP864D         | 7C264-55C      | 10016P8-3C   | 100E301-3C     | PAL16L8-30M  | PALC16L8-30M   | 2015A-15       | 7C128-55C +    |
| 39VP864S         | 7C263-55C      | 10016P8-4C   | 100E301-4C     | PAL16L8A-2C  | PALC16L8-35C   | 2015A-90       | 7C128-55C +    |
| 39VS864S         | 7C261-55C      | 10016P8-6C   | 100E301-6C     | PAL16L8A-2M  | PALC16L8-40M   | 2018-25        | 7C128-25C      |
|                  |                | 10H16P8-3C   | 10E301-3C      | PAL16L8AC    | PALC16L8-25C   | 2018-35        | 7C128-35C      |
|                  |                | 10H16P8-4C   | 10E301-4C      | PAL16L8AM    | PALC16L8-30M   | 2018-45        | 7C128-45C      |
|                  |                | 10H16P8-6C   | 10E301-6C      | PAL16R4-20M  | PALC16R4-20M   | 2018-55        | 7C128-55C +    |
| <b>SIGNETICS</b> | <b>CYPRESS</b> |              |                |              |                |                |                |
| PREFIX:N         | PREFIX:CY      |              |                |              |                |                |                |
| PREFIX:S         | PREFIX:CY      | 22V10AC      | PALC22V10-25C  | PAL16R4-25C  | PALC16R4-25C   | 2068-25        | 7C168-25C      |
| SUFFIX:883B      | SUFFIX:B       | 22V10AM      | PALC22V10-30M  | PAL16R4-30M  | PALC16R4-30M   | 2068-35        | 7C168-35C      |
| SUFFIX:F         | SUFFIX:D       | 27C291-3     | 7C291L-35C +   | PAL16R4A-2C  | PALC16R4-25C   | 2068-45        | 7C168-45C      |
| SUFFIX:G         | SUFFIX:L       | 27C291-30    | 7C291L-35C +   | PAL16R4A-2M  | PALC16R4-40M   | 2068-55        | 7C168-45C      |
| SUFFIX:N         | SUFFIX:P       | 27C291-5     | 7C291L-50C +   | PAL16R4AC    | PALC16R4-25C   | 2069-35        | 7C169-35C      |
| SUFFIX:R         | SUFFIX:F       | 27C291-50    | 7C291L-50C +   | PAL16R4AM    | PALC16R4-30M   | 2078-35        | 7C170-35C      |
| 100422BC         | 100E422-7C     | 27C292-3     | 7C292L-35C +   | PAL16R6-20M  | PALC16R6-20M   | 2078-45        | 7C170-45C      |
| 100422CC         | 100E422-7C     | 27C292-35    | 7C292L-35C +   | PAL16R6-25C  | PALC16R6-25C   | 2078-55        | 7C170-45C      |
| 100474AC         | 100E474-7C     | 27C292-5     | 7C292L-50C +   | PAL16R6-30M  | PALC16R6-30M   | 2088-35        | 7C186-35C      |
| 10422BC          | 10E422-7C      | 27C292-50    | 7C292L-50C +   | PAL16R6A-2C  | PALC16R6-25C   | 2088-45        | 7C186-45C      |
| 10422CC          | 10E422-7C      | 28L166W      | 7C292-50C      | PAL16R6A-2M  | PALC16R6-40M   | 2088-55        | 7C186-55C      |
| 10474AC          | 10E474-7C      | 28L86AMW     | 7C282-45M      | PAL16R6AC    | PALC16R6-25C   | 315            | 2147-55C       |
| N74S189          | 74S189C        | 28L86AW      | 7C282-45C      | PAL16R6AM    | PALC16R6-30M   | 315-1          | 2147-55C       |
| N82HS641         | 7C264-55C      | 28S166W      | 7C292-50C      | PAL16R8-20M  | PALC16R8-20M   | 55416-35       | 7C164-35C      |
| N82HS641A        | 7C264-45C      | 28S86AMW     | 7C282-45M      | PAL16R8-25C  | PALC16R8-25C   | 55416-45       | 7C164-45C      |
| N82HS641B        | 7C264-35C      | 28S86AW      | 7C282-45C      | PAL16R8-30M  | PALC16R8-30M   | 55417-25       | 7C166-25C      |
| N82LS181         | 7C282-45C      | 38L165-35C   | 7C291-35C      | PAL16R8A-2C  | PALC16R8-25C   | 55417-35       | 7C166-35C      |
| N82S181          | 7C282-45C      | 38L165-45C   | 7C291-35C      | PAL16R8A-2M  | PALC16R8-40M   | 55417-45       | 7C166-45C      |
| N82S181A         | 7C282-45C      | 38L166-35    | 7C292-35C      | PAL16R8AC    | PALC16R8-25C   | 5561-45        | 7C187-45C +    |
| N82S181B         | 7C282-45C      | 38L166-45    | 7C292-35C      | PAL16R8AM    | PALC16R8-30M   | 5561-55        | 7C187-45C +    |
| N82S191A-3       | 7C291-50C      | 38L85-45C    | 7C281-45C      | PAL20L10A-2C | PLDC20G10-25C  | 5561-70        | 7C187-45C +    |
| N82S191A-6       | 7C292-50C      | 38R165-18C   | 7C245-25C      | PAL20L10A-2M | PLDC20G10-30M  | 5562-35        | 7C187-35C      |
| N82S191B-3       | 7C291-35C      | 38R165-25C   | 7C245-35C      | PAL20L10AC   | PLDC20G10-35C  | 5562-45        | 7C187-45C      |
| N82S191B-6       | 7C292-35C      | 38R85-15C    | 7C235-30C      | PAL20L10AM   | PLDC20G10-30M  | 5562-55        | 7C187-45C      |
| N82S191-3        | 7C291-50C      | 38S165-25C   | 7C291A-25C     | PAL20L8A-2C  | PLDC20G10-25C  |                |                |
| N82S191-6        | 7C292-50C      | 38S165-35C   | 7C291-35C      | PAL20L8A-2M  | PLDC20G10-30M  |                |                |
| S54S189          | 54S189M        | 38S85-30C    | 7C281-30C      | PAL20L8AC    | PLDC20G10-25C  |                |                |
| S82HS641         | 7C264-55M      | 54HC189      | 7C189-25M      | PAL20L8AM    | PLDC20G10-30M  |                |                |
| S82LS181         | 7C282-45M      | 54HCT189     | 7C189-25M      | PAL20R4A-2C  | PLDC20G10-25C  |                |                |
| S82S181          | 7C282-45M      | 54LS189A     | 27LS03M        | PAL20R4A-2M  | PLDC20G10-30M  |                |                |
| S82S181A         | 7C282-45M      | 54LS219A     | 7C190-25M +    | PAL20R4AC    | PLDC20G10-25C  |                |                |
| S82S191A-3       | 7C291-50M      | 54S189A      | 54S189M        | PAL20R4AM    | PLDC20G10-30M  |                |                |
| S82S191A-6       | 7C292-50M      | 7489         | 7C189-25C      | PAL20R6A-2C  | PLDC20G10-25C  |                |                |
| S82S191B-3       | 7C291-50M      | 74ACT29116   | 7C9116AC       | PAL20R6A-2M  | PLDC20G10-30M  |                |                |
| S82S191B-6       | 7C292-50M      | 74ACT29116-1 | 7C9116AC       | PAL20R6AC    | PLDC20G10-25C  |                |                |
| S82S191-3        | 7C291-50M      | 74HC189      | 7C189-25C      | PAL20R6AM    | PLDC20G10-30M  |                |                |
| S82S191-6        | 7C292-50M      | 74HC219      | 7C190-25C      | PAL20R8A-2C  | PLDC20G10-25C  |                |                |
|                  |                | 74HCT189     | 7C189-25C      | PAL20R8A-2M  | PLDC20G10-30M  |                |                |
|                  |                | 74LS189A     | 27LS03C        | PAL20R8AC    | PLDC20G10-25C  |                |                |
|                  |                | 74LS219A     | 27S07C +       | PAL20R8AM    | PLDC20G10-30M  |                |                |
|                  |                | 74S189A      | 74S189C        |              |                |                |                |
|                  |                | 74S189B      | 7C189-25C      |              |                |                |                |
| <b>TI</b>        | <b>CYPRESS</b> |              |                |              |                |                |                |
| PREFIX:JBP       | PREFIX:CY      |              |                |              |                |                |                |
| PREFIX:PAL       | SUFFIX:P       |              |                |              |                |                |                |
| PREFIX:SN        | PREFIX:CY      |              |                |              |                |                |                |
|                  |                |              |                |              |                | <b>TRW</b>     | <b>CYPRESS</b> |
|                  |                |              |                |              |                | MPY016HA       | 7C516-75M      |
|                  |                |              |                |              |                | MPY016HC       | 7C516-75C      |
|                  |                |              |                |              |                | MPY016KA       | 7C516-75M      |
|                  |                |              |                |              |                | MPY016KC       | 7C516-75C      |
|                  |                |              |                |              |                | TDC1010A       | 7C510-75M      |
|                  |                |              |                |              |                | TDC1010C       | 7C510-75C      |
|                  |                |              |                |              |                | TMC2010A       | 7C510-75M +    |
|                  |                |              |                |              |                | TMC2010C       | 7C510-75C +    |
|                  |                |              |                |              |                | TMC2110A       | 7C510-75M      |
|                  |                |              |                |              |                | TMC2110C       | 7C510-75C      |
|                  |                |              |                |              |                | TMC216HA       | 7C516-75M      |
|                  |                |              |                |              |                | TMC216HC       | 7C516-75C +    |
|                  |                |              |                |              |                | <b>VTI</b>     | <b>CYPRESS</b> |
|                  |                |              |                |              |                | 20C18-25       | 7C128-25C +    |
|                  |                |              |                |              |                | 20C18-35       | 7C128-35C +    |

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\* = meets all performance specs except 2V data retention—may not meet I<sub>CC</sub> or I<sub>SB</sub>;

- = functionally equivalent



# Product Line Cross Reference (Continued)

| VTI         | CYPRESS        | WSI           | CYPRESS        | WEITEK | CYPRESS     |
|-------------|----------------|---------------|----------------|--------|-------------|
| 20C19-25    | 7C128-25C      | 57C191-55     | 7C292-50C      | 2517C  | 7C517-75C   |
| 20C19-35    | 7C128-35C      | 57C191-55M    | 7C292-50M      | 2517M  | 7C517-75M + |
| 20C68-25    | 7C168-25C +    | 57C191-70     | 7C292-50C      |        |             |
| 20C68-35    | 7C168-35C +    | 57C191-70M    | 7C292-50M      |        |             |
| 20C69-25    | 7C169-25C      | 57C291-40     | 7C291-35C      |        |             |
| 20C69-35    | 7C169-35C      | 57C291-55     | 7C291-50C      |        |             |
| 20C69-45    | 7C169-45C      | 57C291-55M    | 7C291-50M      |        |             |
| 20C78-25    | 7C170-25C +    | 57C291-70     | 7C291-50C      |        |             |
| 20C78-35    | 7C170-35C +    | 57C291-70M    | 7C291-50M      |        |             |
| 20C78-45    | 7C170-45C +    | 57C49-55      | 7C264-55C +    |        |             |
| 20C79-25    | 7C170-25C      | 57C49-55M     | 7C264-55M      |        |             |
| 20C79-35    | 7C170-35C      | 57C49-70      | 7C264-55C +    |        |             |
| 20C79-45    | 7C170-45C      | 57C49-70M     | 7C264-55M      |        |             |
| 20C98-35    | 7C185-35C +    | 57C49-90      | 7C264-55C +    |        |             |
| 20C98-45    | 7C185-45C +    | 57C49-90M     | 7C264-55M      |        |             |
| 20C99-35    | 7C185-35C      | 59016C        | 7C9101-40C     |        |             |
| 20C99-45    | 7C185-45C      | 59016C        | 7C9101-45M     |        |             |
| 2130-10C    | 7C130-55C      | 5901C         | 2901CC +       |        |             |
| 2130-12C    | 7C130-55C      | 5901M         | 2901CM +       |        |             |
| 2130-15C    | 7C130-55C      | 5910AC        | 7C910-40C      |        |             |
| 7132-55     | 7C132-55C      | 5910AM        | 7C910-46M      |        |             |
| 7132-70     | 7C132-55C      | 59516         | 7C516-45C      |        |             |
| 7132A-35    | 7C132-35C      | 59517         | 7C517-45C      |        |             |
| 7132A-45    | 7C132-45C      |               |                |        |             |
| 7142-55     | 7C142-55C      | <b>WEITEK</b> | <b>CYPRESS</b> |        |             |
| 7142-70     | 7C142-55C      | 1010AC        | 7C510-75C      |        |             |
| 7142A-35    | 7C142-35C      | 1010AM        | 7C510-75M      |        |             |
| 7142A-45    | 7C142-45C      | 1010BC        | 7C510-75C      |        |             |
| 7C122-15    | 7C122-15C      | 1010BM        | 7C510-75M      |        |             |
| 7C122-25    | 7C122-25C      | 1010C         | 7C510-75C      |        |             |
| 7C122-35    | 7C122-35C      | 1010M         | 7C510-75M      |        |             |
| VL2010-65   | 7C510-65C      | 1516AC        | 7C516-75C      |        |             |
| VL2010-70   | 7C510-65C      | 1516AM        | 7C516-75M      |        |             |
| VL2010-90   | 7C510-75C      | 1516BC        | 7C516-55C      |        |             |
| VT64KS4-35  | 7C164-35C      | 1516BM        | 7C516-75M      |        |             |
| VT64KS4-45  | 7C164-45C      | 1516C         | 7C516-75C      |        |             |
| VT64KS4-55  | 7C164-45C      | 1516M         | 7C516-75M      |        |             |
| VT65KS4-35  | 7C166-35C      | 2010AC        | 7C510-55C      |        |             |
| VT65KS4-45  | 7C166-45C      | 2010AM        | 7C510-75M      |        |             |
| VT65KS4-55  | 7C166-45C      | 2010BC        | 7C510-45C      |        |             |
|             |                | 2010BM        | 7C510-55M      |        |             |
| <b>WSI</b>  | <b>CYPRESS</b> | 2010C         | 7C510-75C      |        |             |
| PREFIX:WS   | PREFIX:CY      | 2010DC        | 7C510-55C      |        |             |
| SUFFIX:C    | PREFIX:CY      | 2010DM        | 7C510-75M      |        |             |
| SUFFIX:D    | PREFIX:CY      | 2010M         | 7C510-75M +    |        |             |
| SUFFIX:M    | SUFFIX:P       | 2516AC        | 7C516-55C      |        |             |
| SUFFIX:P    | PREFIX:CY      | 2516AM        | 7C516-75M      |        |             |
| 29C01C      | 7C901-31C      | 2516C         | 7C516-75C      |        |             |
| 57C128F-70  | 7C251-55C      | 2516DC        | 7C516-45C      |        |             |
| 57C128F-70M | 7C251-55M +    | 2516DM        | 7C516-55M      |        |             |
| 57C128F-90  | 7C251-55C      | 2516M         | 7C516-75M +    |        |             |
| 57C128F-90M | 7C251-55M +    | 2517AC        | 7C517-55C      |        |             |
| 57C191-40   | 7C292-35C      | 2517AM        | 7C517-75M      |        |             |

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\* = meets all performance specs except 2V data retention—may not meet I<sub>CC</sub> or I<sub>SB</sub> ;

- = functionally equivalent



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| CY7C192       | 65,536 x 4 Static RAM Separate I/O       | 2-222       |
| CY7C194       | 65,536 x 4 Static RAM                    | 2-228       |
| CY7C196       | 65,536 x 4 Static RAM with Output Enable | 2-228       |





# Section Contents (Continued)

## Static RAMs (Random Access Memory) (Continued)

| Device Number | Description                             | Page Number |
|---------------|---|-------------|
| CY7C197       | 262,144 x 1 Static RAM                  | 2-234       |
| CY7C198       | 32,768 x 8 Static RAM                   | 2-240       |
| CY7C199       | 32,768 x 8 Static RAM                   | 2-240       |
| CY74S189      | 16 x 4 Static RAM                       | 2-246       |
| CY27LS03      | 16 x 4 Static RAM                       | 2-246       |
| CY27S03       | 16 x 4 Static RAM                       | 2-246       |
| CY27S07       | 16 x 4 Static RAM                       | 2-246       |
| CY93422A      | 256 x 4 Static RAM Separate I/O         | 2-252       |
| CY93L422A     | 256 x 4 Static RAM Separate I/O         | 2-252       |
| CY93422       | 256 x 4 Static RAM Separate I/O         | 2-252       |
| CY93L422      | 256 x 4 Static RAM Separate I/O         | 2-252       |
| CYM1420       | 128K x 8 Static RAM Module              | 2-259       |
| CYM1421       | 128K x 8 Static RAM Module              | 2-265       |
| CYM1422       | 128K x 8 Static RAM Module              | 2-271       |
| CYM1460       | 512K x 8 Static RAM Module              | 2-277       |
| CYM1461       | 512K x 8 Static RAM Module              | 2-282       |
| CYM1610       | 16K x 16 Static RAM Module              | 2-287       |
| CYM1611       | 16K x 16 Static RAM Module              | 2-293       |
| CYM1620       | 64K x 16 Static RAM Module              | 2-299       |
| CYM1621       | 64K x 16 Static RAM Module              | 2-305       |
| CYM1622       | 64K x 16 Static RAM Module              | 2-311       |
| CYM1623       | 64K x 16 Static RAM Module              | 2-312       |
| CYM1626       | 64K x 16 Static RAM Module              | 2-318       |
| CYM1641       | 256K x 16 Static RAM Module             | 2-324       |
| CYM1804       | 1K x 32 Static RAM Module Separate I/O  | 2-330       |
| CYM1821       | 16K x 32 Static RAM Module              | 2-331       |
| CYM1822       | 16K x 32 Static RAM Module Separate I/O | 2-337       |
| CYM1830       | 64K x 32 Static RAM Module              | 2-343       |
| CYM1831       | 64K x 32 Static RAM Module              | 2-349       |
| CYM1832       | 64K x 32 Static RAM Module              | 2-355       |



**Features**

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed  
— 35 ns
- Low active power  
— 690 mW (commercial)  
— 770 mW (military)
- Low standby power  
— 140 mW
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2000V electrostatic discharge

**Functional Description**

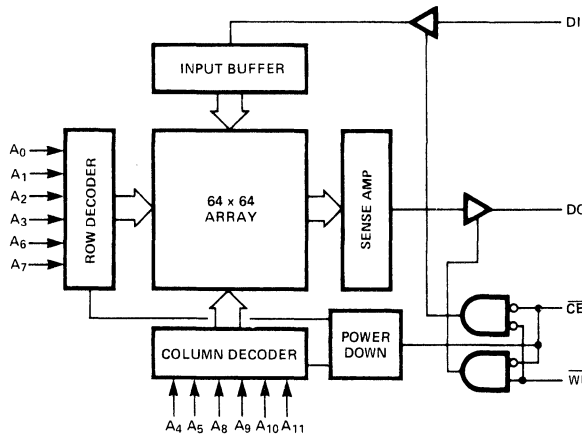
The CY2147 is a high performance CMOS static RAM organized as 4096 x 1 bit. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and three-state drivers. The CY2147 has an automatic power-down feature, reducing the power consumption by 80% when deselected.

Writing to the device is accomplished when the chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the input pin ( $\overline{DI}$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{11}$ ).

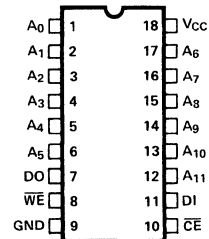
Reading the device is accomplished by taking the chip enable ( $\overline{CE}$ ) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output ( $\overline{DO}$ ) pin.

The output pin stays in high impedance state when chip enable ( $\overline{CE}$ ) is HIGH or write enable ( $\overline{WE}$ ) is LOW.

**Logic Block Diagram**



**Pin Configuration**



0013-2

0013-1

**Selection Guide** (For higher performance and lower power refer to CY7C147 data sheet.)

|                                |            | 2147-35 | 2147-45 | 2147-55 |
|--------------------------------|------------|---------|---------|---------|
| Maximum Access Time (ns)       |            | 35      | 45      | 55      |
| Maximum Operating Current (mA) | Commercial | 125     | 125     | 125     |
|                                | Military   |         | 140     | 140     |
| Maximum Standby Current (mA)   | Commercial | 25      | 25      | 25      |
|                                | Military   |         | 25      | 25      |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|  |                 |
|--|-----------------|
| Storage Temperature .....                                  | -65°C to +150°C |
| Ambient Temperature with Power Applied .....               | -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 18 to Pin 9) ..... | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State .....        | -0.5V to +7.0V  |
| DC Input Voltage .....                                     | -3.0V to +7.0V  |
| Output Current into Outputs (Low) .....                    | 20 mA           |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | > 2001V<br>(Per MIL-STD-883 Method 3015) |
| Latchup Current .....          | > 200 mA                                 |

## Operating Range

| Range       | Ambient Temperature | V <sub>CC</sub> |
|-------------|---------------------|-----------------|
| Commercial  | 0°C to +70°C        | 5V ± 10%        |
| Military[5] | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over Operating Range[4]

| Parameters      | Description   | Test Conditions   | Min.       | Max.            | Units |
|-----------------|---|---|------------|-----------------|-------|
| V <sub>OH</sub> | Output HIGH Voltage                                 | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA         | 2.4        |                 | V     |
| V <sub>OL</sub> | Output LOW Voltage                                  | V <sub>CC</sub> = Min., I <sub>OL</sub> = 12.0 mA         |            | 0.4             | V     |
| V <sub>IH</sub> | Input HIGH Voltage                                  |   | 2.0        | V <sub>CC</sub> | V     |
| V <sub>IL</sub> | Input LOW Voltage                                   |   | -3.0       | 0.8             | V     |
| I <sub>IX</sub> | Input Load Current                                  | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                    | -10        | +10             | μA    |
| I <sub>OZ</sub> | Output Leakage Current                              | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub><br>Output Disabled | -50        | +50             | μA    |
| I <sub>OS</sub> | Output Short Circuit Current <sup>[1]</sup>         | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND            |            | -350            | mA    |
| I <sub>CC</sub> | V <sub>CC</sub> Operating Supply Current            | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA         | Commercial | 125             | mA    |
|                 |   |   | Military   | 140             |       |
| I <sub>SB</sub> | Automatic $\overline{CE}$ [2]<br>Power Down Current | Max. V <sub>CC</sub> ,<br>$\overline{CE} \geq V_{IH}$     | Commercial | 25              | mA    |
|                 |   |   | Military   | 25              |       |

## Capacitance[3]

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 6    |       |

### Notes:

- Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the  $\overline{CE}$  input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- Tested initially and after any design or process changes that may affect these parameters.
- See the last page of this specification for Group A subgroup testing information.
- T<sub>A</sub> is the "instant on" case temperature.

## AC Test Loads and Waveforms

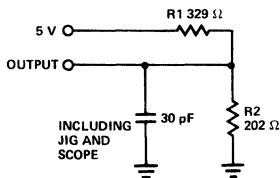


Figure 1a

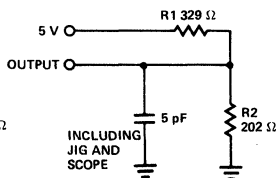


Figure 1b

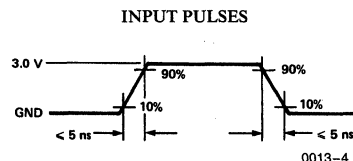
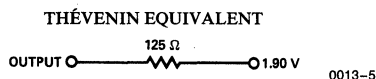


Figure 2

Equivalent to:



Switching Characteristics Over Operating Range<sup>[4, 6]</sup>

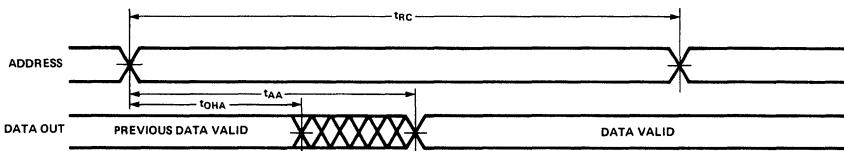
| Parameters                       | Description                         | 2147-35 |      | 2147-45 |      | 2147-55 |      | Units |
|----------------------------------|-------------------------------------|---------|------|---------|------|---------|------|-------|
|                                  |                                     | Min.    | Max. | Min.    | Max. | Min.    | Max. |       |
| <b>READ CYCLE</b>                |                                     |         |      |         |      |         |      |       |
| t <sub>RC</sub>                  | Read Cycle Time                     | 35      |      | 45      |      | 55      |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid               |         | 35   |         | 45   |         | 55   | ns    |
| t <sub>OHA</sub>                 | Data Hold from Address Change       | 5       |      | 5       |      | 5       |      | ns    |
| t <sub>ACE</sub>                 | CE LOW to Data Valid                |         | 35   |         | 45   |         | 55   | ns    |
| t <sub>LZCE</sub>                | CE LOW to Low Z <sup>[8]</sup>      | 5       |      | 5       |      | 5       |      | ns    |
| t <sub>HZCE</sub>                | CE HIGH to High Z <sup>[7, 8]</sup> |         | 30   |         | 30   |         | 30   | ns    |
| t <sub>PU</sub>                  | CE LOW to Power Up                  | 0       |      | 0       |      | 0       |      | ns    |
| t <sub>PD</sub>                  | CE HIGH to Power Down               |         | 20   |         | 20   |         | 20   | ns    |
| <b>WRITE CYCLE<sup>[9]</sup></b> |                                     |         |      |         |      |         |      |       |
| t <sub>WC</sub>                  | Write Cycle Time                    | 35      |      | 45      |      | 55      |      | ns    |
| t <sub>SCE</sub>                 | CE LOW to Write End                 | 35      |      | 45      |      | 45      |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End         | 35      |      | 45      |      | 45      |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End         | 0       |      | 0       |      | 10      |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start       | 0       |      | 0       |      | 0       |      | ns    |
| t <sub>PWE</sub>                 | WE Pulse Width                      | 20      |      | 25      |      | 25      |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End            | 20      |      | 25      |      | 25      |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End            | 10      |      | 10      |      | 10      |      | ns    |
| t <sub>LZWE</sub>                | WE HIGH to Low Z <sup>[8]</sup>     | 0       |      | 0       |      | 0       |      | ns    |
| t <sub>HZWE</sub>                | WE LOW to High Z <sup>[7, 8]</sup>  | 0       | 20   | 0       | 25   | 0       | 25   | ns    |

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZCE</sub> and t<sub>HZWE</sub> are tested with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> for all devices.
- The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- WE is HIGH for read cycle.
- Device is continuously selected, CE = V<sub>IL</sub>.
- Address valid prior to or coincident with CE transition LOW.

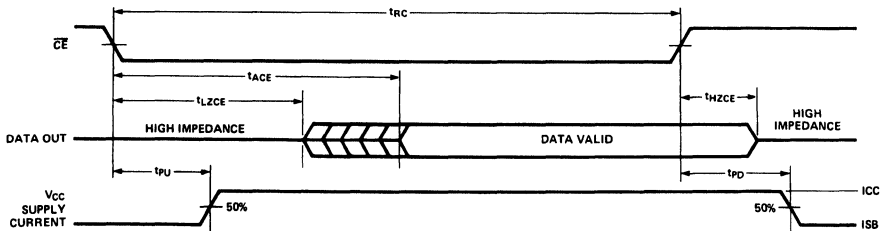
Switching Waveforms

Read Cycle No. 1 (Notes 10, 11)

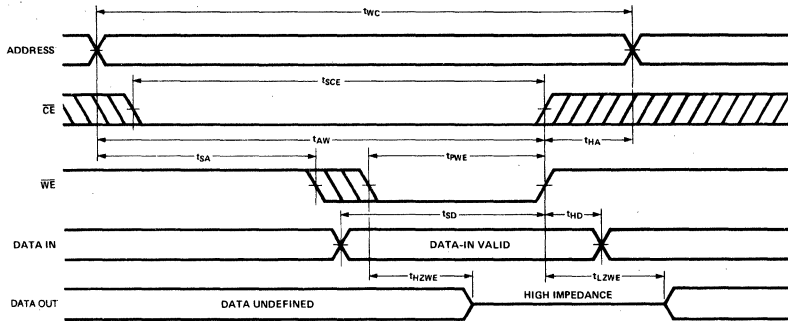


0013-6

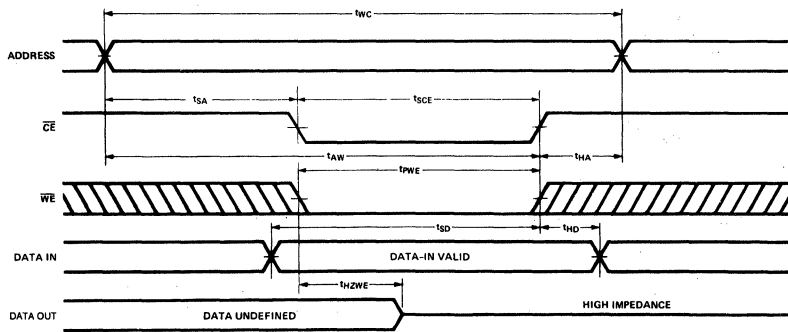
Read Cycle No. 2 (Notes 10, 12)



0013-7

**Switching Waveforms (Continued)**
**Write Cycle No. 1 ( $\overline{WE}$  Controlled) (Note 9)**


0013-8

**Write Cycle No. 2 ( $\overline{CE}$  Controlled) (Note 9)**


0013-9

Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 35         | CY2147-35 PC  | P3           | Commercial      |
|            | CY2147-35 DC  | D4           |                 |
| 45         | CY2147-45 PC  | P3           | Commercial      |
|            | CY2147-45 DC  | D4           |                 |
|            | CY2147-45 DMB | D4           | Military        |
| 55         | CY2147-55 PC  | P3           | Commercial      |
|            | CY2147-55 DC  | D4           |                 |
|            | CY2147-55 DMB | D4           | Military        |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**
**2**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB</sub>      | 1,2,3     |

**Switching Characteristics**

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>ACE</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>SCE</sub>   | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |

Document #: 38-00023-B



### Features

- Automated power-down when deselected (2148)
- CMOS for optimum speed/power
- Low power
  - 660 mW (commercial)
  - 770 mW (military)
- 5 volt power supply  $\pm 10\%$  tolerance both commercial and military
- TTL compatible inputs and outputs

### Functional Description

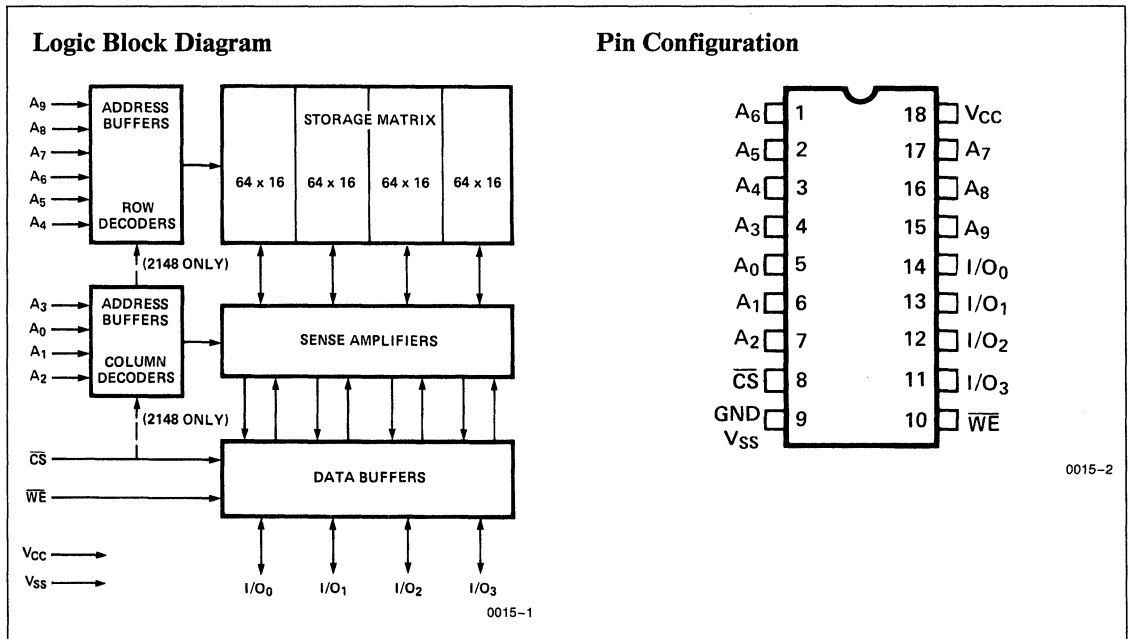
The CY2148 and CY2149 are high performance CMOS static RAMs organized as 1024 x 4 bits. Easy memory expansion is provided by an active LOW chip select ( $\overline{CS}$ ) input, and three-state outputs. The CY2148 and CY2149 are identical except that the CY2148 includes an automatic ( $\overline{CS}$ ) power-down feature. The CY2148 remains in a low power mode as long as the device remains unselected, i.e. ( $\overline{CS}$ ) is HIGH, thus reducing the average power requirements of the device. The chip select ( $\overline{CS}$ ) of the CY2149 does not affect the power dissipation of the device.

An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When the chip

select ( $\overline{CS}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW, data on the four data input/output pins (I/O<sub>0</sub> through I/O<sub>3</sub>) is written into the memory location addressed by the address present on the address pins (A<sub>0</sub> through A<sub>9</sub>).

Reading the device is accomplished by selecting the device, ( $\overline{CS}$ ) active LOW, while ( $\overline{WE}$ ) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins (A<sub>0</sub> through A<sub>9</sub>) is present on the four data input/output pins (I/O<sub>0</sub> through I/O<sub>3</sub>).

The input/output pins (I/O<sub>0</sub> through I/O<sub>3</sub>) remain in a high impedance state unless the chip is selected, and write enable ( $\overline{WE}$ ) is high.



### Selection Guide (For Higher Performance and Lower Power Refer to CY7C148/9 Data Sheet)

|                                |            | 2148/9-35 | 21L48/9-35 | 2148/9-45 | 21L48/9-45 | 2148/9-55 | 21L48/9-55 |
|--------------------------------|------------|-----------|------------|-----------|------------|-----------|------------|
| Maximum Access Time (ns)       |            | 35        | 35         | 45        | 45         | 55        | 55         |
| Maximum Operating Current (mA) | Commercial | 140       | 120        | 140       | 120        | 140       | 120        |
|                                | Military   |           |            | 140       |            | 140       |            |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential (Pin 18 to Pin 9) ..... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

### Operating Range

| Range                    | Ambient Temperature | V <sub>CC</sub> |
|--------------------------|---------------------|-----------------|
| Commercial               | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[11]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[12]</sup>

| Parameters       | Description                                  | Test Conditions   |  | 21L48/9 |      | 2148/9 |      | Units |
|------------------|--|---|--|---------|------|--------|------|-------|
|                  |  |   |  | Min.    | Max. | Min.   | Max. |       |
| I <sub>OH</sub>  | Output HIGH Current                          | V <sub>OH</sub> = 2.4V  | V <sub>CC</sub> = 4.5V   | -4      |      | -4     |      | mA    |
| I <sub>OL</sub>  | Output LOW Current                           | V <sub>OL</sub> = 0.4V  | T <sub>A</sub> = 70°C<br>T <sub>A</sub> = 125°C                                | 8       |      | 8      |      | mA    |
| V <sub>IH</sub>  | Input HIGH Voltage                           |   |  | 2.0     | 6.0  | 2.0    | 6.0  | V     |
| V <sub>IL</sub>  | Input LOW Voltage                            |   |  | -3.0    | 0.8  | -3.0   | 0.8  | V     |
| I <sub>IX</sub>  | Input Load Current                           | V <sub>SS</sub> ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                                      |  | -10     | 10   | -10    | 10   | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                       | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub><br>Output Disabled                               | T <sub>A</sub> = -55°C to +125°C   | -50     | 50   | -50    | 50   | μA    |
| C <sub>I</sub>   | Input Capacitance <sup>[13]</sup>            | Test Frequency = 1.0 MHz<br>T <sub>A</sub> = 25°C, All Pins at 0V, V <sub>CC</sub> = 5V |  |         | 5    |        | 5    | pF    |
| C <sub>I/O</sub> | Input/Output Capacitance <sup>[13]</sup>     |   |  |         | 7    |        | 7    |       |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current     | Max. V <sub>CC</sub> , $\overline{CS} \leq V_{IL}$<br>Output Open                       | T <sub>A</sub> = 0°C to +70°C<br>T <sub>A</sub> = -55°C to +125°C              |         | 120  |        | 140  | mA    |
| I <sub>SB</sub>  | Automatic $\overline{CS}$ Power Down Current | Max. V <sub>CC</sub> ,<br>$\overline{CS} \geq V_{IH}$                                   | 2148 only<br>T <sub>A</sub> = 0°C to +70°C<br>T <sub>A</sub> = -55°C to +125°C |         | 20   |        | 30   | mA    |
| I <sub>PO</sub>  | Peak Power-On Current                        | Max. V <sub>CC</sub> ,<br>$\overline{CS} \geq V_{IH}$ <sup>[3]</sup>                    | 2148 only<br>T <sub>A</sub> = 0°C to +70°C<br>T <sub>A</sub> = -55°C to +125°C |         | 30   |        | 50   | mA    |
| I <sub>OS</sub>  | Output Short Circuit Current                 | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> <sup>[10]</sup>                                  | T <sub>A</sub> = 0°C to +70°C<br>T <sub>A</sub> = -55°C to +125°C              |         | ±275 |        | ±275 | mA    |
|                  |  |   |  |         |      |        | ±350 | mA    |

#### Notes:

- Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance. Output timing reference is 1.5V.
- The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- A pull up resistor to V<sub>CC</sub> on the  $\overline{CS}$  input is required to keep the device deselected during V<sub>CC</sub> power up. Otherwise current will exceed values given (CY2148 only).
- Chip deselected greater than 55 ns prior to selection.
- Chip deselected less than 55 ns prior to selection.
- At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> for all devices. Transition is measured ±500 mV from steady state voltage with specified loading in Figure 1b.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CS} = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{CS}$  transition LOW.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.

### AC Test Loads and Waveforms

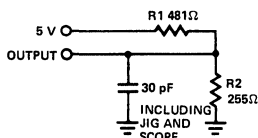


Figure 1a

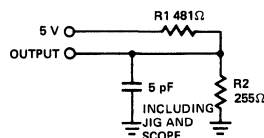


Figure 1b

0015-3

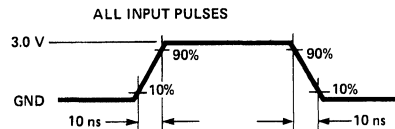
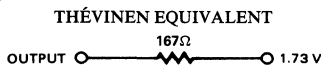


Figure 2

0015-5

Equivalent to:



0015-4

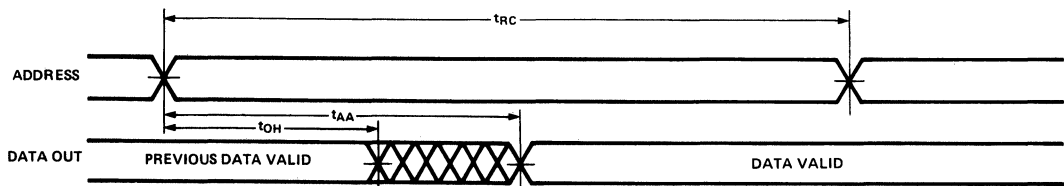


## Switching Characteristics<sup>[12]</sup>

| Parameters                       | Description   | 2148/9-35 |      | 2148/9-45 |      | 2148/9-55 |      | Units |
|----------------------------------|---|-----------|------|-----------|------|-----------|------|-------|
|                                  |   | Min.      | Max. | Min.      | Max. | Min.      | Max. |       |
| <b>READ CYCLE</b>                |   |           |      |           |      |           |      |       |
| t <sub>RC</sub>                  | Address Valid to Address Do Not Care Time (Read Cycle Time) | 35        |      | 45        |      | 55        |      | ns    |
| t <sub>AA</sub>                  | Address Valid to Data Out Valid Delay (Address Access Time) |           | 35   |           | 45   |           | 55   | ns    |
| t <sub>ACS1</sub> <sup>[4]</sup> | Chip Select LOW to Data Out Valid (CY2148 only)             |           | 35   |           | 45   |           | 55   | ns    |
| t <sub>ACS2</sub> <sup>[5]</sup> |   |           | 45   |           | 55   |           | 65   |       |
| t <sub>ACS</sub>                 | Chip Select LOW to Data Out Valid (CY2149 only)             |           | 15   |           | 20   |           | 25   | ns    |
| t <sub>LZ</sub> <sup>[6]</sup>   | Chip Select LOW to Data Out On                              | 2148      | 10   |           | 10   |           | 10   | ns    |
|                                  |   | 2149      | 5    |           | 5    |           | 5    |       |
| t <sub>HZ</sub> <sup>[6]</sup>   | Chip Select HIGH to Data Out Off                            | 0         | 20   | 0         | 20   | 0         | 20   | ns    |
| t <sub>OH</sub>                  | Address Unknown to Data Out Unknown Time                    | 0         |      | 5         |      | 5         |      | ns    |
| t <sub>PD</sub>                  | Chip Select HIGH to Power-Down Delay                        | 2148      |      | 30        |      | 30        |      | ns    |
| t <sub>PU</sub>                  | Chip Select LOW to Power-Up Delay                           | 2148      | 0    |           | 0    |           | 0    | ns    |
| <b>WRITE CYCLE</b>               |   |           |      |           |      |           |      |       |
| t <sub>WC</sub>                  | Address Valid to Address Do Not Care (Write Cycle Time)     | 35        |      | 45        |      | 55        |      | ns    |
| t <sub>WP</sub> <sup>[2]</sup>   | Write Enable LOW to Write Enable HIGH                       | 30        |      | 35        |      | 40        |      | ns    |
| t <sub>WR</sub>                  | Address Hold from Write End                                 | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>WZ</sub> <sup>[6]</sup>   | Write Enable LOW to Output in High Z                        | 0         | 10   | 0         | 15   | 0         | 20   | ns    |
| t <sub>DW</sub>                  | Data in Valid to Write Enable HIGH                          | 20        |      | 20        |      | 20        |      | ns    |
| t <sub>DH</sub>                  | Data Hold Time  | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>AS</sub>                  | Address Valid to Write Enable LOW                           | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>CW</sub> <sup>[2]</sup>   | Chip Select LOW to Write Enable HIGH                        | 30        |      | 40        |      | 50        |      | ns    |
| t <sub>OW</sub> <sup>[6]</sup>   | Write Enable High to Output in Low Z                        | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>AW</sub>                  | Address Valid to End of Write                               | 30        |      | 35        |      | 50        |      | ns    |

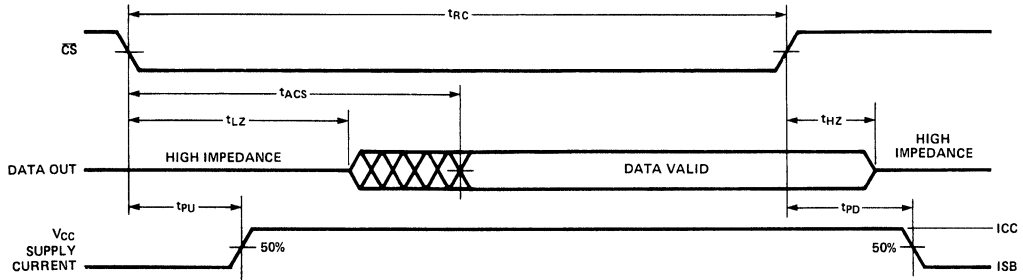
## Switching Waveforms

### Read Cycle No. 1 (Notes 7, 8)



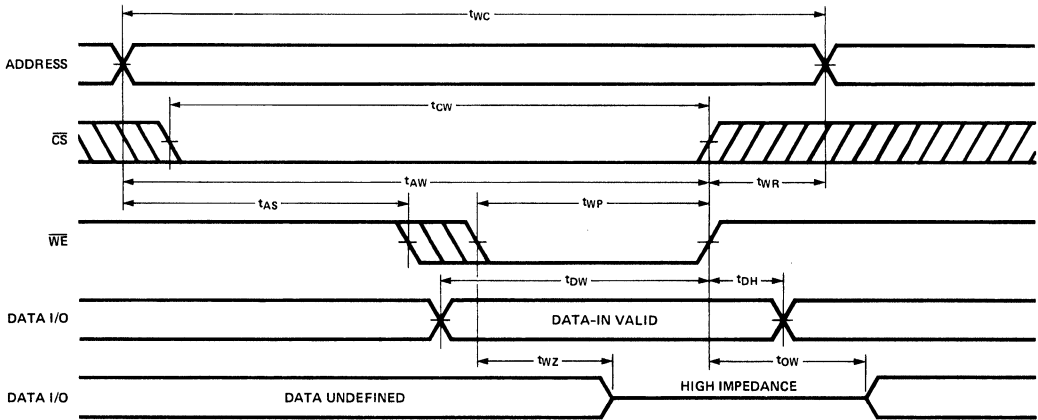
## Switching Waveforms (Continued)

### Read Cycle No. 2 (Notes 7, 9)



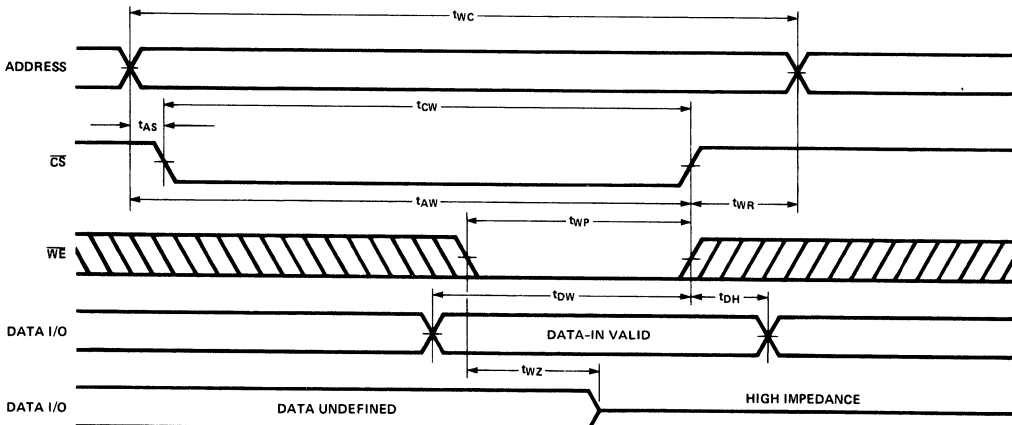
0015-9

### Write Cycle No. 1 ( $\overline{WE}$ Controlled)



0015-8

### Write Cycle No. 2 ( $\overline{CS}$ Controlled)



Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a HIGH impedance state.

0015-7

### Ordering Information

| Speed (ns) | Ordering Code                  | Package Type | Operating Range |
|------------|--------------------------------|--------------|-----------------|
| 35         | CY2148-35 PC<br>CY2149-35 PC   | P3           | Commercial      |
|            | CY2148-35 DC<br>CY2149-35 DC   | D4           |                 |
|            | CY21L48-35 PC<br>CY21L49-35 PC | P3           | Commercial      |
|            | CY21L48-35 DC<br>CY21L49-35 DC | D4           |                 |
| 45         | CY2148-45 PC<br>CY2149-45 PC   | P3           | Commercial      |
|            | CY2148-45 DC<br>CY2149-45 DC   | D4           |                 |
|            | CY2148-45 DMB<br>CY2149-45 DMB | D4           | Military        |
|            | CY21L48-45 PC<br>CY21L49-45 PC | P3           | Commercial      |
|            | CY21L48-45 DC<br>CY21L49-45 DC | D4           |                 |
| 55         | CY2148-55 PC<br>CY2149-55 PC   | P3           | Commercial      |
|            | CY2148-55 DC<br>CY2149-55 DC   | D4           |                 |
|            | CY2148-55 DMB<br>CY2149-55 DMB | D4           | Military        |
|            | CY21L48-55 PC<br>CY21L49-55 PC | P3           | Commercial      |
|            | CY21L48-55 DC<br>CY21L49-55 DC | D4           |                 |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters                     | Subgroups |
|--------------------------------|-----------|
| I <sub>OH</sub>                | 1,2,3     |
| I <sub>OL</sub>                | 1,2,3     |
| V <sub>IH</sub>                | 1,2,3     |
| V <sub>IL Max.</sub>           | 1,2,3     |
| I <sub>IX</sub>                | 1,2,3     |
| I <sub>OZ</sub>                | 1,2,3     |
| I <sub>CC</sub>                | 1,2,3     |
| I <sub>SB</sub> <sup>[1]</sup> | 1,2,3     |

#### Switching Characteristics

| Parameters                       | Subgroups   |
|----------------------------------|-------------|
| <b>READ CYCLE</b>                |             |
| t <sub>RC</sub>                  | 7,8,9,10,11 |
| t <sub>AA</sub>                  | 7,8,9,10,11 |
| t <sub>ACS1</sub> <sup>[1]</sup> | 7,8,9,10,11 |
| t <sub>ACS2</sub> <sup>[1]</sup> | 7,8,9,10,11 |
| t <sub>ACS</sub> <sup>[2]</sup>  | 7,8,9,10,11 |
| t <sub>OH</sub>                  | 7,8,9,10,11 |
| <b>WRITE CYCLE</b>               |             |
| t <sub>WC</sub>                  | 7,8,9,10,11 |
| t <sub>WP</sub>                  | 7,8,9,10,11 |
| t <sub>WR</sub>                  | 7,8,9,10,11 |
| t <sub>DW</sub>                  | 7,8,9,10,11 |
| t <sub>DH</sub>                  | 7,8,9,10,11 |
| t <sub>AS</sub>                  | 7,8,9,10,11 |
| t <sub>AW</sub>                  | 7,8,9,10,11 |

**Notes:**

1. CY2148 only.
2. CY2149 only.

Document #: 38-00024-B



**Features**

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed—35 ns
- Low active power — 660 mW
- Low standby power — 110 mW
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

**Functional Description**

The CY6116 and CY6117 are high performance CMOS static RAMs organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ), and active LOW output enable ( $\overline{OE}$ ) and three-state drivers. The CY6116 and CY6117 have an automatic power-down feature, reducing the power consumption by 83% when deselected.

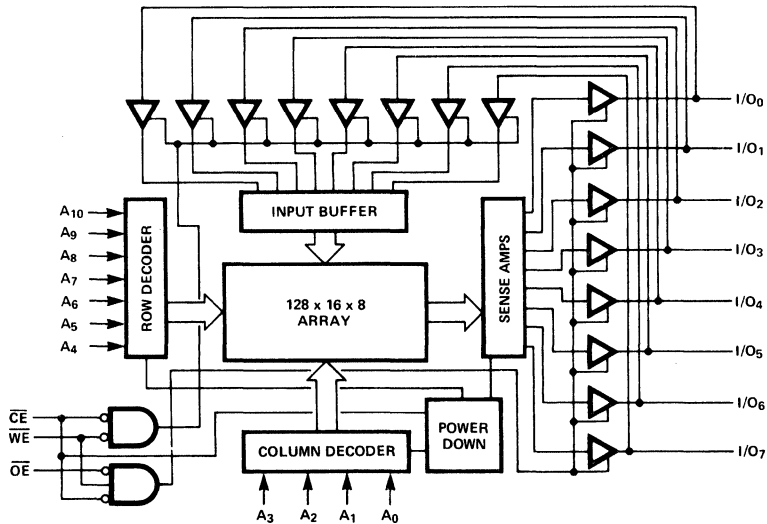
An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When the chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW, data on the eight data input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the memory loca-

tion addressed by the address present on the address pins (A<sub>0</sub> through A<sub>10</sub>). Reading the devices is accomplished by selecting the device and enabling the outputs,  $\overline{CE}$  and  $\overline{OE}$  active LOW, while ( $\overline{WE}$ ) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH.

The CY6116 and CY6117 utilize a die coat to ensure alpha immunity.

**Logic Block Diagram**



0087-1

**Selection Guide**

|                                |            | <b>CY6116-35</b><br><b>CY6117-35</b> | <b>CY6116-45</b><br><b>CY6117-45</b> | <b>CY6116-55</b><br><b>CY6117-55</b> |
|--------------------------------|------------|--------------------------------------|--------------------------------------|--------------------------------------|
| Maximum Access Time (ns)       |            | 35                                   | 45                                   | 55                                   |
| Maximum Operating Current (mA) | Commercial | 120                                  | 120                                  | 120                                  |
|                                | Military   | 130                                  | 130                                  | 130                                  |
| Maximum Standby Current (mA)   | Commercial | 20                                   | 20                                   | 20                                   |
|                                | Military   | 20                                   | 20                                   | 20                                   |

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied ..... -55°C to +125°C
- Supply Voltage to Ground Potential (Pin 24 to Pin 12)..... -0.5V to +7.0V
- DC Voltage Applied to Outputs in High Z State..... -0.5V to +7.0V
- DC Input Voltage ..... -3.0V to +7.0V
- Output Current into Outputs (Low) ..... 20 mA

- Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015)
- Latch-up Current ..... >200 mA

**Operating Range**

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[4]</sup> | -55°C to +125°C     | 5V ± 10%        |

**Electrical Characteristics Over Operating Range<sup>[3]</sup>**

| Parameters      | Description                                  | Test Conditions   | CY6116<br>CY6117 |                 | Units |
|-----------------|--|---|------------------|-----------------|-------|
|                 |  |   | Min.             | Max.            |       |
| V <sub>OH</sub> | Output HIGH Voltage                          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA         | 2.4              |                 | V     |
| V <sub>OL</sub> | Output LOW Voltage                           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA          |                  | 0.4             | V     |
| V <sub>IH</sub> | Input HIGH Voltage                           |   | 2.0              | V <sub>CC</sub> | V     |
| V <sub>IL</sub> | Input LOW Voltage                            |   | -3.0             | 0.8             | V     |
| I <sub>IX</sub> | Input Load Current                           | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                    | -10              | 10              | μA    |
| I <sub>OZ</sub> | Output Leakage Current                       | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub><br>Output Disabled |                  | 10              | μA    |
| I <sub>OS</sub> | Output Short Circuit Current <sup>[1]</sup>  | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND            |                  | -300            | mA    |
| I <sub>CC</sub> | V <sub>CC</sub> Operating Supply Current     | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA         | Commercial       | 120             | mA    |
|                 |  |   | Military         | 130             |       |
| I <sub>SB</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> ,<br>CE ≥ V <sub>IH</sub>            | Commercial       | 20              | mA    |
|                 |  |   | Military         | 20              |       |

**Capacitance<sup>[2]</sup>**

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 7    |       |

**Notes:**

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested initially and after any design or process changes that may affect these parameters.
3. See the last page of this specification for Group A subgroup testing information.
4. T<sub>A</sub> is the “instant on” case temperature.

**AC Test Loads and Waveforms**

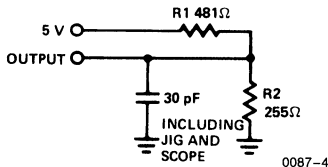


Figure 1a

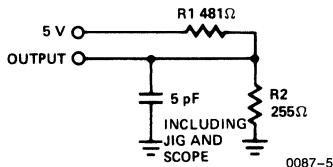


Figure 1b

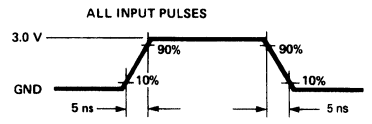
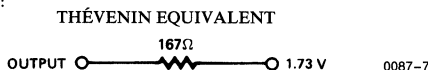


Figure 2

Equivalent to:



**Switching Characteristics Over Operating Range<sup>[4, 6]</sup>**

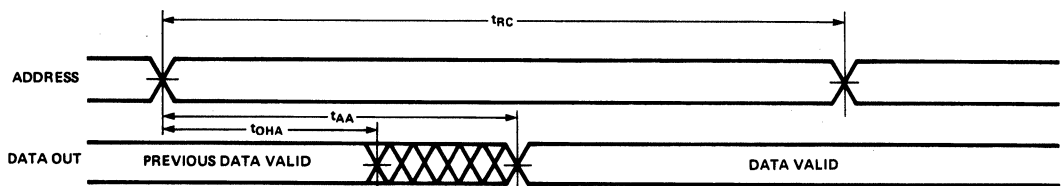
| Parameters                       | Description                                      | CY6116-35<br>CY6117-35 |      | CY6116-45<br>CY6117-45 |      | CY6116-55<br>CY6117-55 |      | Units |
|----------------------------------|--|------------------------|------|------------------------|------|------------------------|------|-------|
|                                  |  | Min.                   | Max. | Min.                   | Max. | Min.                   | Max. |       |
| <b>READ CYCLE</b>                |  |                        |      |                        |      |                        |      |       |
| t <sub>RC</sub>                  | Read Cycle Time                                  | 35                     |      | 45                     |      | 55                     |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid                            |                        | 35   |                        | 45   |                        | 55   | ns    |
| t <sub>OHA</sub>                 | Data Hold from Address Change                    | 5                      |      | 5                      |      | 5                      |      | ns    |
| t <sub>ACE</sub>                 | $\overline{CE}$ LOW to Data Valid                |                        | 35   |                        | 45   |                        | 55   | ns    |
| t <sub>DOE</sub>                 | $\overline{OE}$ LOW to Data Valid                |                        | 15   |                        | 20   |                        | 25   | ns    |
| t <sub>LZOE</sub>                | $\overline{OE}$ LOW to Low Z                     | 0                      |      | 0                      |      | 0                      |      | ns    |
| t <sub>HZOE</sub>                | $\overline{OE}$ HIGH to High Z <sup>[7]</sup>    |                        | 15   |                        | 15   |                        | 20   | ns    |
| t <sub>LZCE</sub>                | $\overline{CE}$ LOW to Low Z <sup>[8]</sup>      | 5                      |      | 5                      |      | 5                      |      | ns    |
| t <sub>HZCE</sub>                | $\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup> |                        | 15   |                        | 20   |                        | 20   | ns    |
| t <sub>PU</sub>                  | $\overline{CE}$ LOW to Power Up                  | 0                      |      | 0                      |      | 0                      |      | ns    |
| t <sub>PD</sub>                  | $\overline{CE}$ HIGH to Power Down               |                        | 20   |                        | 25   |                        | 25   | ns    |
| <b>WRITE CYCLE<sup>[9]</sup></b> |  |                        |      |                        |      |                        |      |       |
| t <sub>WC</sub>                  | Write Cycle Time                                 | 35                     |      | 45                     |      | 55                     |      | ns    |
| t <sub>SCE</sub>                 | $\overline{CE}$ LOW to Write End                 | 30                     |      | 40                     |      | 40                     |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End                      | 30                     |      | 40                     |      | 40                     |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End                      | 0                      |      | 0                      |      | 0                      |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                    | 0                      |      | 0                      |      | 0                      |      | ns    |
| t <sub>PWE</sub>                 | WE Pulse Width                                   | 20                     |      | 20                     |      | 25                     |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End                         | 15                     |      | 20                     |      | 25                     |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End                         | 0                      |      | 0                      |      | 0                      |      | ns    |
| t <sub>HZWE</sub>                | WE LOW to High Z                                 |                        | 15   |                        | 15   |                        | 20   | ns    |
| t <sub>LZWE</sub>                | WE HIGH to Low Z                                 | 0                      |      | 0                      |      | 0                      |      | ns    |

**Notes:**

- Data I/O Pins enter high-impedance state, as shown, when  $\overline{OE}$  is held LOW during write.
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- WE is HIGH for read cycle.
- Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  = V<sub>IL</sub>.
- Address valid prior to or coincident with CE transition LOW.

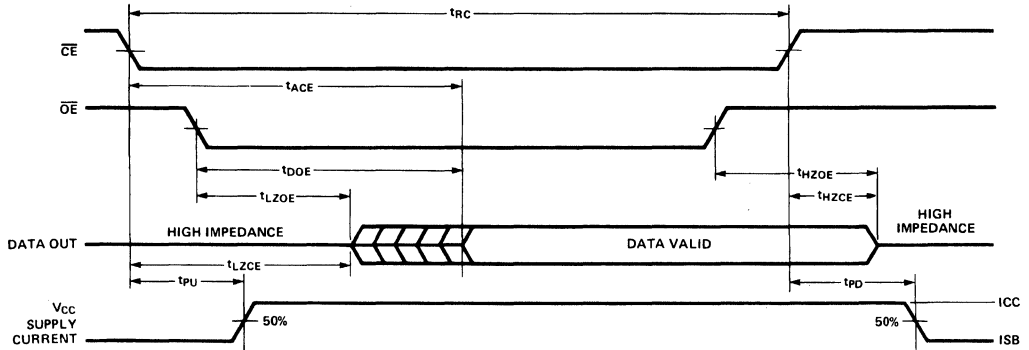
**Switching Waveforms**

**Read Cycle No. 1 (Notes 10, 11)**



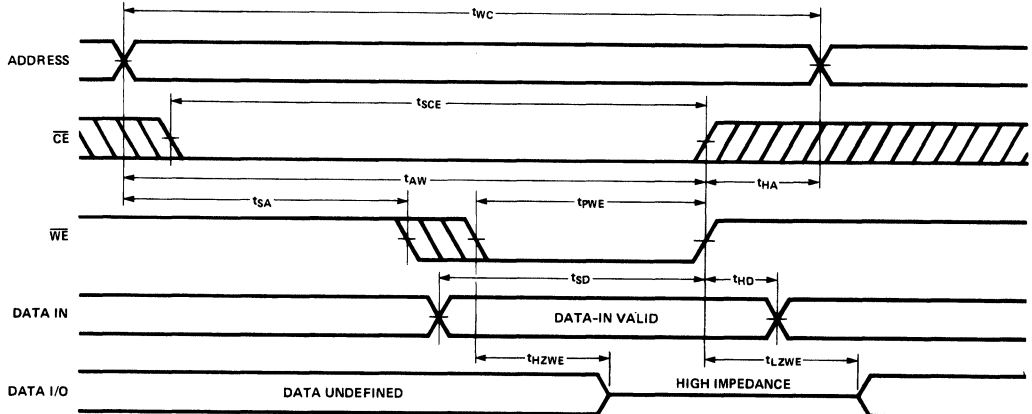
## Switching Waveforms (Continued)

### Read Cycle No. 2 (Notes 10, 12)



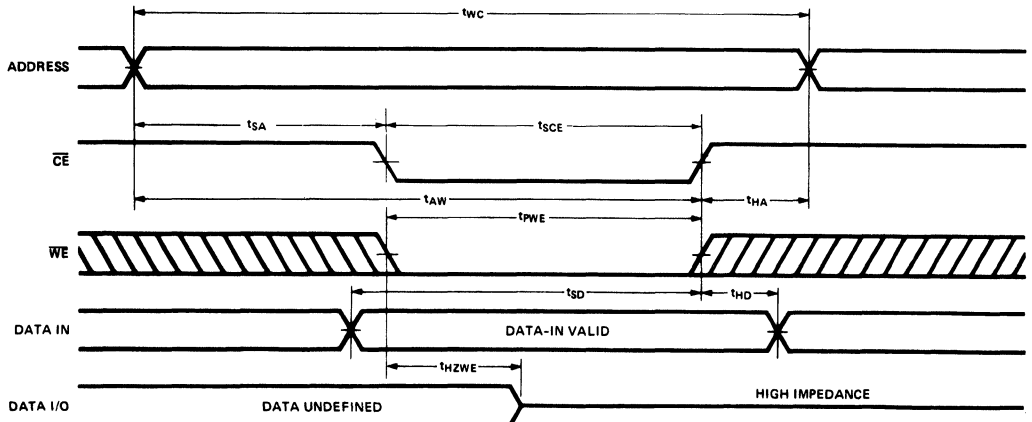
0087-9

### Write Cycle No. 1 ( $\overline{WE}$ Controlled) (Notes 5, 9)



0087-10

### Write Cycle No. 2 ( $\overline{CE}$ Controlled) (Notes 5, 9)

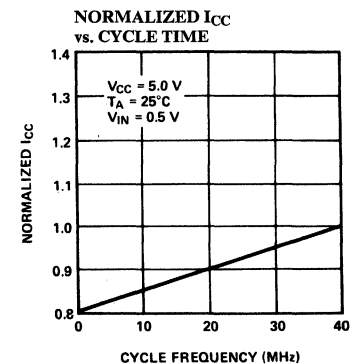
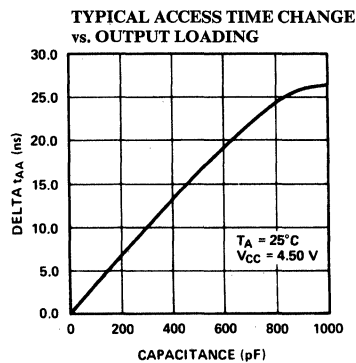
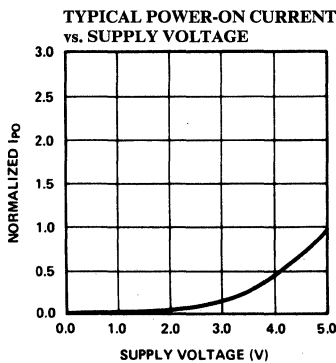
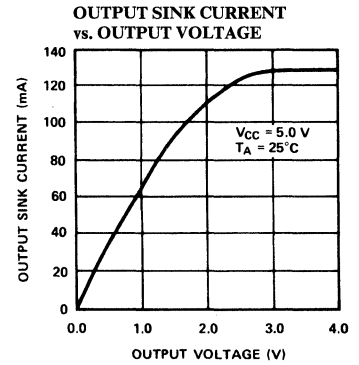
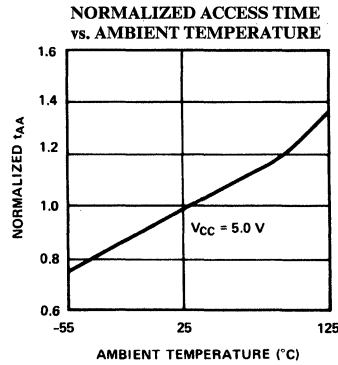
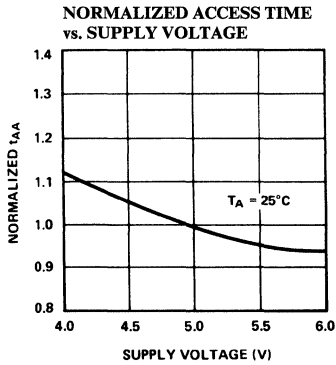
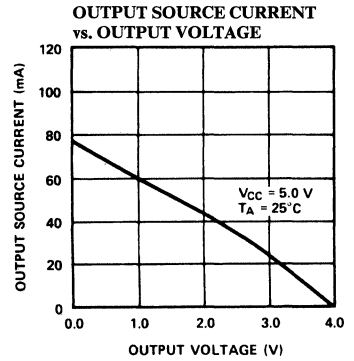
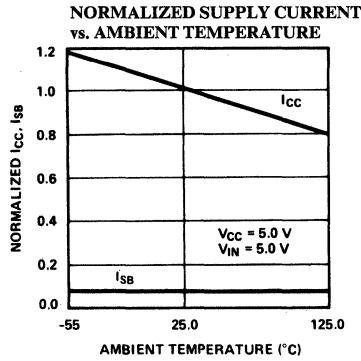
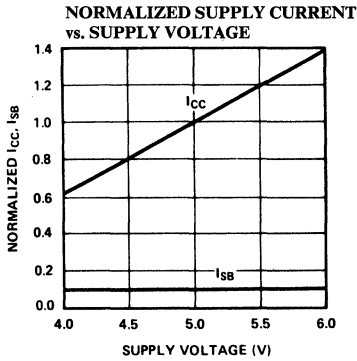


Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

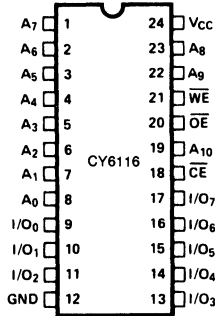
0087-11



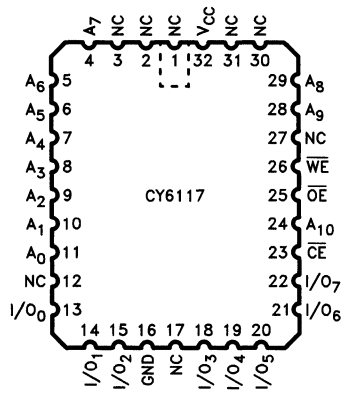
Typical DC and AC Characteristics



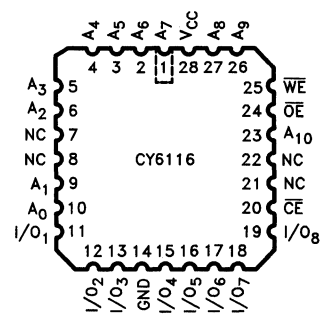
## Pin Configurations



0087-2



0087-14



0087-3

## Ordering Information

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 35         | CY6116-35PC   | P11          | Commercial      |
|            | CY6116-35DC   | D12          |                 |
|            | CY6116-35LC   | L64          |                 |
|            | CY6116-35DMB  | D12          | Military        |
|            | CY6116-35LMB  | L64          |                 |
| 45         | CY6116-45PC   | P11          | Commercial      |
|            | CY6116-45DC   | D12          |                 |
|            | CY6116-45LC   | L64          |                 |
|            | CY6116-45DMB  | D12          | Military        |
|            | CY6116-45LMB  | L64          |                 |
| 55         | CY6116-55PC   | P11          | Commercial      |
|            | CY6116-55DC   | D12          |                 |
|            | CY6116-55LC   | L64          |                 |
|            | CY6116-55DMB  | D12          | Military        |
|            | CY6116-55LMB  | L64          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 35         | CY6117-35LMB  | L55          | Military        |
| 45         | CY6117-45LMB  | L55          | Military        |
| 55         | CY6117-55LMB  | L55          | Military        |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>Ix</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB</sub>      | 1,2,3     |

#### Switching Characteristics

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>ACE</sub>   | 7,8,9,10,11 |
| t <sub>DOE</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>SCE</sub>   | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |

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**Features**

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed—20 ns
- Low active power — 550 mW
- Low standby power — 110 mW
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

**Functional Description**

The CY6116A and CY6117A are high performance CMOS static RAMs organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (CE), and active LOW output enable (OE) and three-state drivers. The CY6116A and CY6117A have an automatic power-down feature, reducing the power consumption by 83% when deselected.

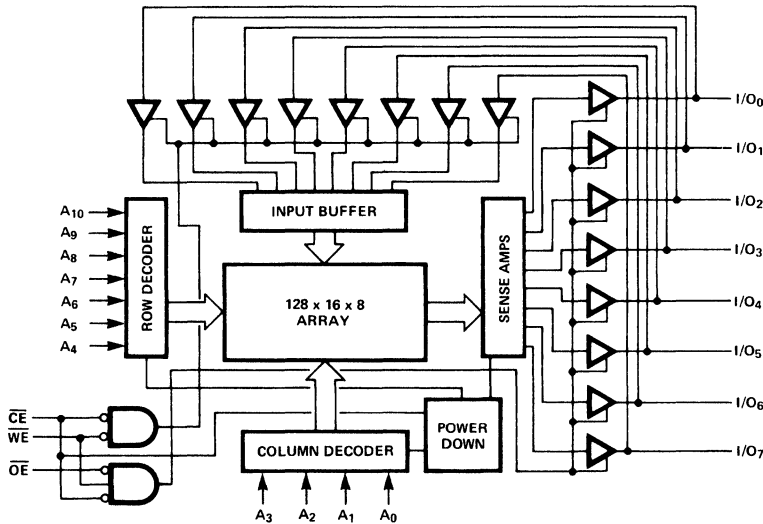
An active LOW write enable signal (WE) controls the writing/reading operation of the memory. When the chip enable (CE) and write enable (WE) inputs are both LOW, data on the eight data input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the memory loca-

tion addressed by the address present on the address pins (A<sub>0</sub> through A<sub>10</sub>). Reading the device is accomplished by selecting the device and enabling the outputs, CE and OE active LOW, while (WE) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable (WE) is HIGH.

The CY6116A and CY6117A utilize a die coat to ensure alpha immunity.

**Logic Block Diagram**



0167-1

**Selection Guide**

|                                |            | CY6116A-20<br>CY6117A-20 | CY6116A-25<br>CY6117A-25 | CY6116A-35<br>CY6117A-35 | CY6116A-45<br>CY6117A-45 | CY6116A-55<br>CY6117A-55 |
|--------------------------------|------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| Maximum Access Time (ns)       |            | 20                       | 25                       | 35                       | 45                       | 55                       |
| Maximum Operating Current (mA) | Commercial | 100                      | 100                      | 100                      | 100                      | 80                       |
|                                | Military   |                          | 125                      | 100                      | 100                      | 100                      |
| Maximum Standby Current (mA)   | Commercial | 40/20                    | 20                       | 20                       | 20                       | 20                       |
|                                | Military   |                          | 40                       | 20                       | 20                       | 20                       |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature                                   | -65°C to +150°C |
| Ambient Temperature with Power Applied                | -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 24 to Pin 12) | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State         | -0.5V to +7.0V  |
| DC Input Voltage                                      | -3.0V to +7.0V  |
| Output Current into Outputs (Low)                     | 20 mA           |

|                          |  |
|--------------------------|--|
| Static Discharge Voltage | > 2001V<br>(Per MIL-STD-883 Method 3015) |
| Latch-up Current         | > 200 mA                                 |

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[4]</sup> | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over Operating Range<sup>[3]</sup>

| Parameters       | Description                                  | Test Conditions  | CY6116A-20<br>CY6117A-20 |                 | CY6116A-25, 35, 45<br>CY6117A-25, 35, 45 |                 | CY6116A-55<br>CY6117A-55 |                 | Units |
|------------------|--|--|--------------------------|-----------------|--|-----------------|--------------------------|-----------------|-------|
|                  |  |  | Min.                     | Max.            | Min.                                     | Max.            | Min.                     | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA  | 2.4                      |                 | 2.4                                      |                 | 2.4                      |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA   |                          | 0.4             |  | 0.4             |                          | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                           |  | 2.2                      | V <sub>CC</sub> | 2.2                                      | V <sub>CC</sub> | 2.2                      | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage <sup>[4A]</sup>            |  | -0.5                     | 0.8             | -0.5                                     | 0.8             | -0.5                     | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current                           | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -10                      | 10              | -10                                      | 10              | -10                      | 10              | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                       | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub><br>Output Disabled  | -10                      | +10             | -10                                      | +10             | -10                      | +10             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>  | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND   |                          | -300            |  | -300            |                          | -300            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current     | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA  | Coml.                    | 100             |  | 100             |                          | 80              | mA    |
|                  |  |  | Mil.                     | 25              |  | 125             |                          | 100             |       |
|                  |  |  |                          | 35, 45          |  | 100             |                          |                 |       |
| I <sub>SB1</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> ,<br>CE <sub>1</sub> ≥ V <sub>IH</sub> ,<br>Min. Duty Cycle = 100%  | Coml.                    | 40              |  | 20              |                          | 20              | mA    |
|                  |  |  | Mil.                     | 25              |  | 40              |                          | 20              |       |
|                  |  |  |                          | 35, 45          |  | 20              |                          |                 |       |
| I <sub>SB2</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> ,<br>CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.3V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V<br>or V <sub>IN</sub> ≤ 0.3V | Coml.                    | 20              |  | 20              |                          | 20              | mA    |
|                  |  |  | Mil.                     |                 |  | 20              |                          | 20              |       |

\*35 ns and 55 ns only

## Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 7    |       |

### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- See the last page of this specification for Group A subgroup testing information.
- T<sub>A</sub> is the "instant on" case temperature.
- V<sub>IL min.</sub> = -3.0V for pulse durations less than 30 ns.

## AC Test Loads and Waveforms

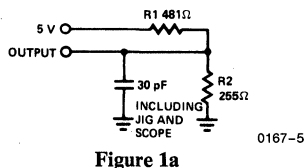


Figure 1a

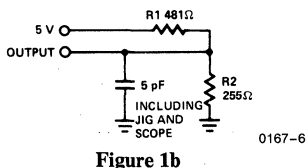


Figure 1b

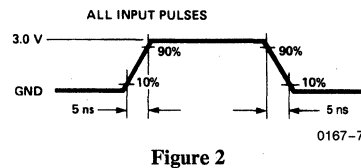
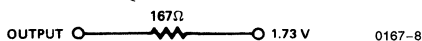


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



### Switching Characteristics Over Operating Range<sup>[4, 6]</sup>

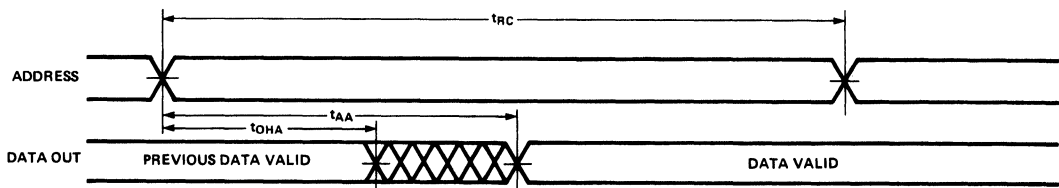
| Parameters                       | Description                                      | CY6116A-20<br>CY6117A-20 |      | CY6116A-25<br>CY6117A-25 |      | CY6116A-35<br>CY6117A-35 |      | CY6116A-45<br>CY6117A-45 |      | CY6116A-55<br>CY6117A-55 |      | Units |
|----------------------------------|--|--------------------------|------|--------------------------|------|--------------------------|------|--------------------------|------|--------------------------|------|-------|
|                                  |  | Min.                     | Max. | Min.                     | Max. | Min.                     | Max. | Min.                     | Max. | Min.                     | Max. |       |
|                                  |  | <b>READ CYCLE</b>        |      |                          |      |                          |      |                          |      |                          |      |       |
| t <sub>RC</sub>                  | Read Cycle Time                                  | 20                       |      | 25                       |      | 35                       |      | 45                       |      | 55                       |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid                            |                          | 20   |                          | 25   |                          | 35   |                          | 45   |                          | 55   | ns    |
| t <sub>OHA</sub>                 | Data Hold from Address Change                    | 5                        |      | 5                        |      | 5                        |      | 5                        |      | 5                        |      | ns    |
| t <sub>ACE</sub>                 | $\overline{CE}$ LOW to Data Valid                |                          | 20   |                          | 25   |                          | 35   |                          | 45   |                          | 55   | ns    |
| t <sub>DOE</sub>                 | $\overline{OE}$ LOW to Data Valid                |                          | 10   |                          | 12   |                          | 15   |                          | 20   |                          | 25   | ns    |
| t <sub>LZOE</sub>                | $\overline{OE}$ LOW to Low Z                     | 3                        |      | 3                        |      | 3                        |      | 3                        |      | 3                        |      | ns    |
| t <sub>HZOE</sub>                | $\overline{OE}$ HIGH to High Z <sup>[7]</sup>    |                          | 8    |                          | 10   |                          | 12   |                          | 15   |                          | 20   | ns    |
| t <sub>LZCE</sub>                | $\overline{CE}$ LOW to Low Z <sup>[8]</sup>      | 5                        |      | 5                        |      | 5                        |      | 5                        |      | 5                        |      | ns    |
| t <sub>HZCE</sub>                | $\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup> |                          | 8    |                          | 10   |                          | 15   |                          | 15   |                          | 20   | ns    |
| t <sub>PU</sub>                  | $\overline{CE}$ LOW to Power Up                  | 0                        |      | 0                        |      | 0                        |      | 0                        |      | 0                        |      | ns    |
| t <sub>PD</sub>                  | $\overline{CE}$ HIGH to Power Down               |                          | 20   |                          | 20   |                          | 20   |                          | 25   |                          | 25   | ns    |
| <b>WRITE CYCLE<sup>[9]</sup></b> |  |                          |      |                          |      |                          |      |                          |      |                          |      |       |
| t <sub>WC</sub>                  | Write Cycle Time                                 | 20                       |      | 20                       |      | 25                       |      | 40                       |      | 50                       |      | ns    |
| t <sub>SCE</sub>                 | $\overline{CE}$ LOW to Write End                 | 15                       |      | 20                       |      | 25                       |      | 30                       |      | 40                       |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End                      | 15                       |      | 20                       |      | 25                       |      | 30                       |      | 40                       |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End                      | 0                        |      | 0                        |      | 0                        |      | 0                        |      | 0                        |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                    | 0                        |      | 0                        |      | 0                        |      | 0                        |      | 0                        |      | ns    |
| t <sub>PWE</sub>                 | WE Pulse Width                                   | 15                       |      | 15                       |      | 20                       |      | 20                       |      | 25                       |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End                         | 10                       |      | 10                       |      | 15                       |      | 15                       |      | 25                       |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End                         | 0                        |      | 0                        |      | 0                        |      | 0                        |      | 0                        |      | ns    |
| t <sub>HZWE</sub>                | $\overline{WE}$ LOW to High Z                    |                          | 7    |                          | 7    |                          | 10   |                          | 15   |                          | 20   | ns    |
| t <sub>LZWE</sub>                | $\overline{WE}$ HIGH to Low Z                    | 5                        |      | 5                        |      | 5                        |      | 5                        |      | 5                        |      | ns    |

**Notes:**

- Data I/O Pins enter high-impedance state, as shown, when  $\overline{OE}$  is held LOW during write.
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  = V<sub>IL</sub>.
- Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

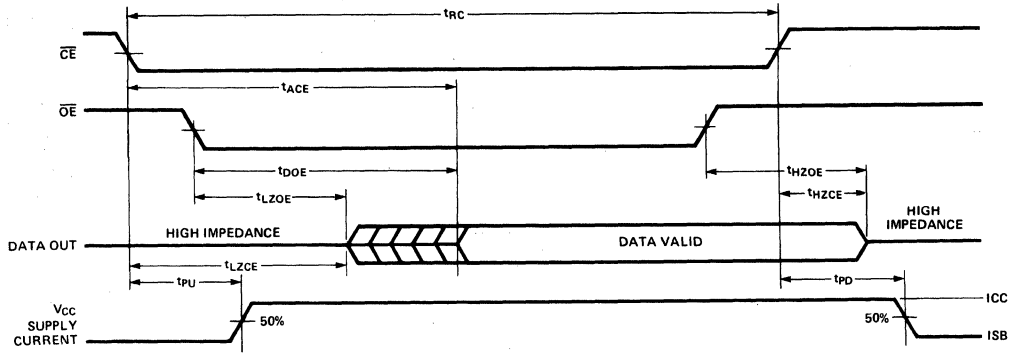
### Switching Waveforms

#### Read Cycle No. 1 (Notes 10, 11)



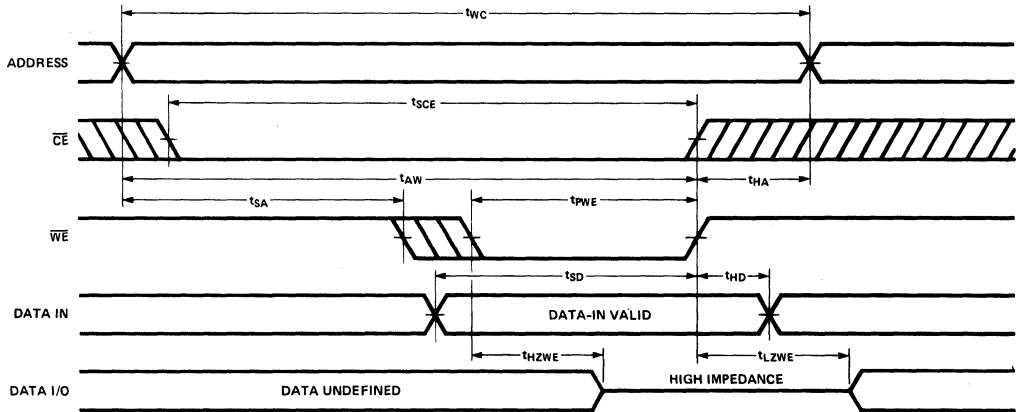
### Switching Waveforms (Continued)

#### Read Cycle No. 2 (Notes 10, 12)



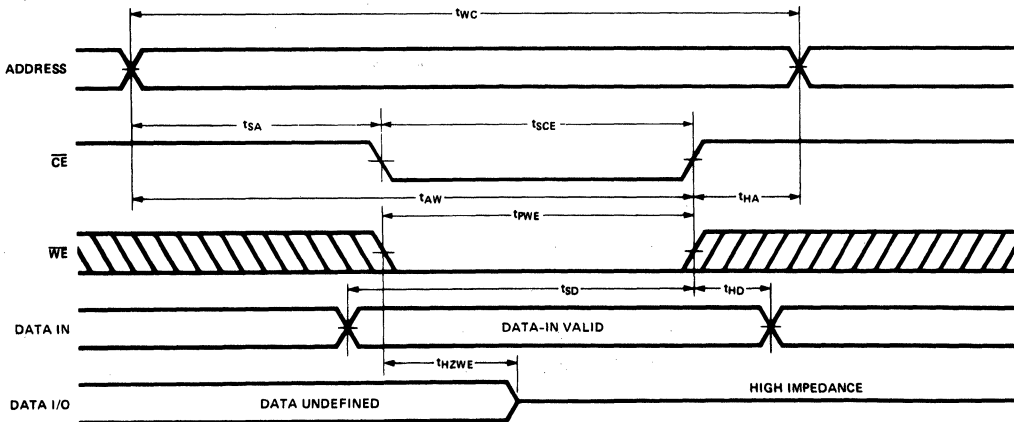
0167-10

#### Write Cycle No. 1 ( $\overline{WE}$ Controlled) (Notes 5, 9)



0167-11

#### Write Cycle No. 2 ( $\overline{CE}$ Controlled) (Notes 5, 9)

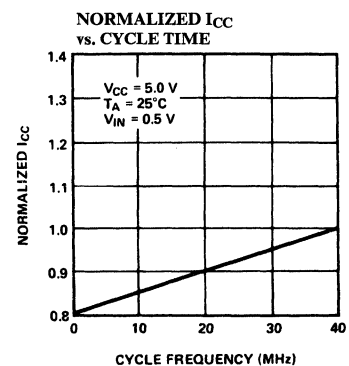
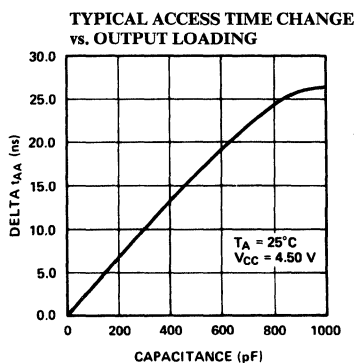
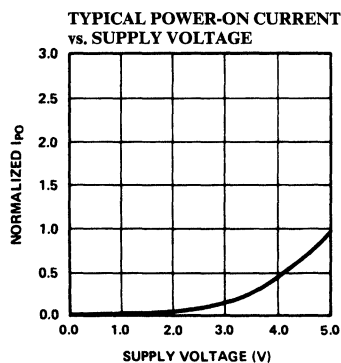
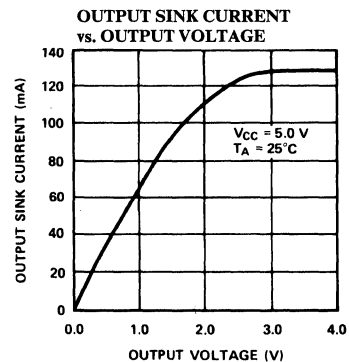
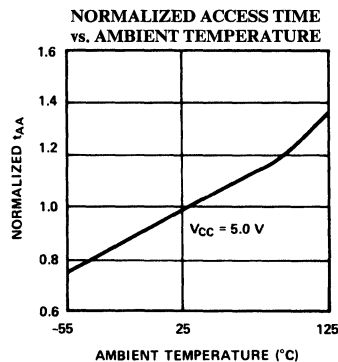
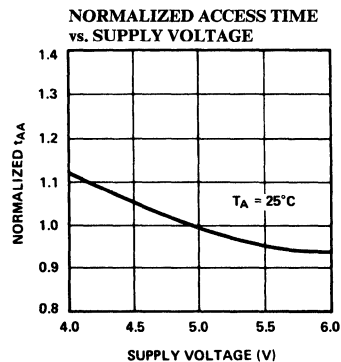
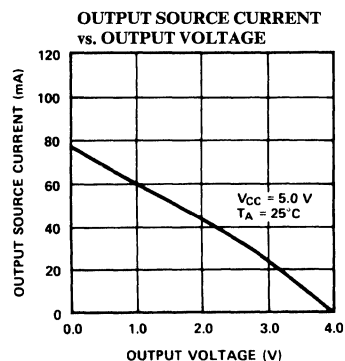
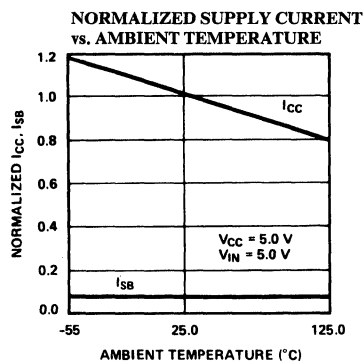
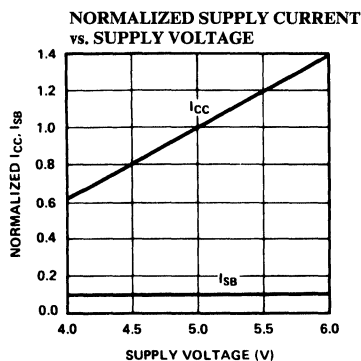


0167-12

Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

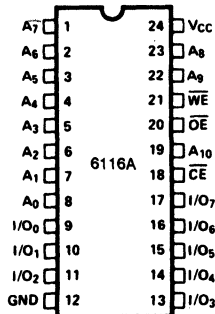
## Typical DC and AC Characteristics

2

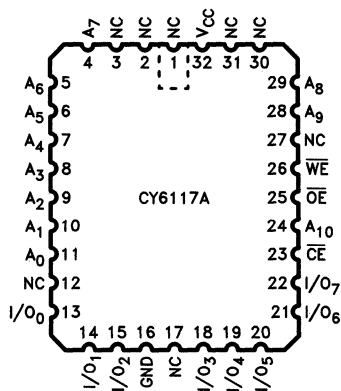




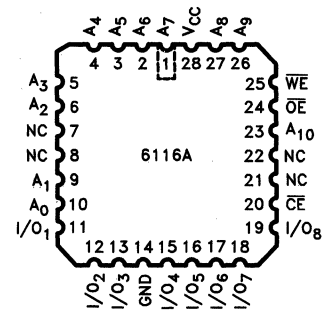
## Pin Configurations



0167-2



0167-3



0167-4

## Ordering Information

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 20         | CY6116A-20PC  | P11          | Commercial      |
|            | CY6116A-20DC  | D12          |                 |
| 25         | CY6116A-25PC  | P11          | Commercial      |
|            | CY6116A-25DC  | D12          |                 |
|            | CY6116A-25LC  | L64          |                 |
|            | CY6116A-25DMB | D12          | Military        |
|            | CY6116A-25LMB | L64          |                 |
| 35         | CY6116A-35PC  | P11          | Commercial      |
|            | CY6116A-35DC  | D12          |                 |
|            | CY6116A-35LC  | L64          |                 |
|            | CY6116A-35DMB | D12          | Military        |
|            | CY6116A-35LMB | L64          |                 |
| 45         | CY6116A-45PC  | P11          | Commercial      |
|            | CY6116A-45DC  | D12          |                 |
|            | CY6116A-45LC  | L64          |                 |
|            | CY6116A-45DMB | D12          | Military        |
|            | CY6116A-45LMB | L64          |                 |
| 55         | CY6116A-55PC  | P11          | Commercial      |
|            | CY6116A-55DC  | D12          |                 |
|            | CY6116A-55LC  | L64          |                 |
|            | CY6116A-55DMB | D12          | Military        |
|            | CY6116A-55LMB | L64          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY6117A-25LMB | L55          | Military        |
| 35         | CY6117A-35LMB | L55          | Military        |
| 45         | CY6117A-45LMB | L55          | Military        |
| 55         | CY6117A-55LMB | L55          | Military        |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters | Subgroups |
|------------|-----------|
| VOH        | 1,2,3     |
| VOL        | 1,2,3     |
| VIH        | 1,2,3     |
| VIL Max.   | 1,2,3     |
| IIX        | 1,2,3     |
| IOZ        | 1,2,3     |
| ICC        | 1,2,3     |
| ISB        | 1,2,3     |

**2**

#### Switching Characteristics

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>ACE</sub>   | 7,8,9,10,11 |
| t <sub>DOE</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>SCE</sub>   | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |

Document #: 38-00105



**Features**

- 256 x 4 static RAM for control store in high speed computers
- CMOS for optimum speed/power
- High speed
  - 15 ns (commercial)
  - 25 ns (military)
- Low power
  - 330 mW (commercial)
  - 495 mW (military)
- Separate inputs and outputs
- 5 volt power supply  $\pm 10\%$  tolerance both commercial and military
- Capable of withstanding greater than 2000V static discharge
- TTL compatible inputs and outputs

**Functional Description**

The CY7C122 is a high performance CMOS static RAM organized as 256 words x 4 bits. Easy memory expansion is provided by an active LOW chip select one ( $\overline{CS}_1$ ) input, an active HIGH chip select two ( $CS_2$ ) input, and three-state outputs.

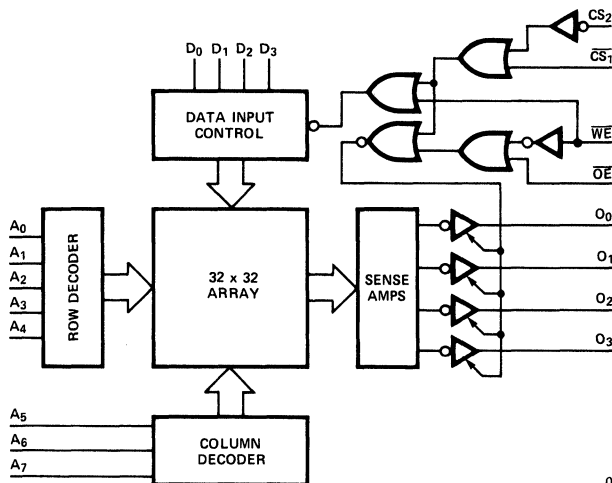
An active LOW write enable input ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When the chip select one ( $\overline{CS}_1$ ) and write enable ( $\overline{WE}$ ) inputs are LOW and the chip select two ( $CS_2$ ) input is HIGH, the information on the four data inputs  $D_0$  to  $D_3$  is written into the addressed memory word and the output circuitry is pre-conditioned so that the correct data is present at the outputs when the write cycle is complete. This preconditioning

operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select one ( $\overline{CS}_1$ ) input LOW, the chip select two input ( $CS_2$ ) and write enable ( $\overline{WE}$ ) inputs HIGH, and the output enable input ( $\overline{OE}$ ) LOW. The information stored in the addressed word is read out on the four non-inverting outputs  $O_0$  to  $O_3$ .

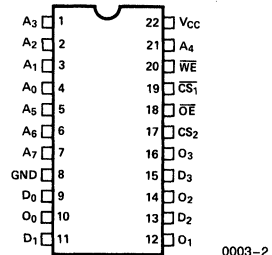
The outputs of the memory go to an active high impedance state whenever chip select one ( $\overline{CS}_1$ ) is HIGH, chip select two ( $CS_2$ ) is LOW, output enable ( $\overline{OE}$ ) is HIGH, or during the writing operation when write enable ( $\overline{WE}$ ) is LOW.

**Logic Block Diagram**

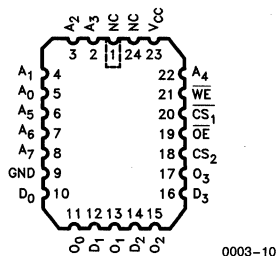


0003-1

**Pin Configurations**



0003-2



0003-10

**Selection Guide**

|                                |            | 7C122-15 | 7C122-25 | 7C122-35 |
|--------------------------------|------------|----------|----------|----------|
| Maximum Access Time (ns)       | Commercial | 15       | 25       | 35       |
|                                | Military   | NA       | 25       | 35       |
| Maximum Operating Current (mA) | Commercial | 90       | 60       | 60       |
|                                | Military   | NA       | 90       | 90       |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature .....                                     | -65°C to +150°C |
| Ambient Temperature with<br>Power Applied .....               | -55°C to +125°C |
| Supply Voltage to Ground Potential<br>(Pin 22 to Pin 8) ..... | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs<br>in High Z State .....        | -0.5V to +7.0V  |
| DC Input Voltage .....  | -3.0V to +7.0V  |
| Output Current, into Outputs (Low) .....                      | 20 mA           |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | > 2001V<br>(per MIL-STD-883 Method 3015) |
| Latchup Current .....          | > 200 mA                                 |

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[5]</sup> | -55°C to +125°C     | 5V ± 10%        |

## Logic Table

| OE | Inputs          |                 |    |   | D <sub>0</sub> -D <sub>3</sub> | Outputs                        | Mode             |
|----|-----------------|-----------------|----|---|--------------------------------|--------------------------------|------------------|
|    | CS <sub>1</sub> | CS <sub>2</sub> | WE |   |                                |                                |                  |
| X  | H               | X               | X  | X | X                              | High Z                         | Not Selected     |
| X  | X               | L               | X  | X | X                              | High Z                         | Not Selected     |
| L  | L               | H               | H  | X | X                              | O <sub>0</sub> -O <sub>3</sub> | Read Stored Data |
| X  | L               | H               | L  | L | L                              | High Z                         | Write "0"        |
| X  | L               | H               | L  | H | H                              | High Z                         | Write "1"        |
| H  | L               | H               | H  | X | X                              | High Z                         | Output Disabled  |

Notes: H = HIGH Voltage    L = LOW Voltage    X = Don't Care  
 High Z = High Impedance

## Electrical Characteristics Over the Operating Range<sup>[4]</sup>

| Parameters      | Description                           | Test Conditions   | 7C122-15   |                 | 7C122-25<br>7C122-35 |                 | Units |
|-----------------|---------------------------------------|---|------------|-----------------|----------------------|-----------------|-------|
|                 |                                       |   | Min.       | Max.            | Min.                 | Max.            |       |
| V <sub>OH</sub> | Output HIGH Voltage                   | V <sub>CC</sub> = Min., I <sub>OH</sub> = -5.2 mA                       | 2.4        |                 | 2.4                  |                 | V     |
| V <sub>OL</sub> | Output LOW Voltage                    | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA                        |            | 0.4             |                      | 0.4             | V     |
| V <sub>IH</sub> | Input HIGH Voltage                    |   | 2.1        | V <sub>CC</sub> | 2.1                  | V <sub>CC</sub> | V     |
| V <sub>IL</sub> | Input LOW Voltage                     |   | -3.0       | 0.8             | -3.0                 | 0.8             | V     |
| I <sub>IX</sub> | Input Load Current                    | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                                  |            | 10              |                      | 10              | μA    |
| V <sub>CD</sub> | Input Diode Clamp Voltage             |   |            | Note 2          |                      | Note 2          | V     |
| I <sub>OZ</sub> | Output Current (High-Z)               | V <sub>OL</sub> ≤ V <sub>OUT</sub> ≤ V <sub>OH</sub><br>Output Disabled | -10        | +10             | -10                  | +10             | μA    |
| I <sub>OS</sub> | Output Short Circuit Current (Note 1) | V <sub>CC</sub> = Max.,<br>V <sub>OUT</sub> = GND                       | Commercial | -70             |                      | -70             | mA    |
|                 |                                       |   | Military   | -80             |                      | -80             | mA    |
| I <sub>CC</sub> | Power Supply Current                  | V <sub>CC</sub> = Max.,<br>I <sub>OUT</sub> = 0 mA                      | Commercial | 90              |                      | 60              | mA    |
|                 |                                       |   | Military   | NA              |                      | 90              | mA    |

## Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 4    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 7    |       |

### Notes:

- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- The CMOS process does not provide a clamp diode. However, the CY7C122 is insensitive to -3V dc input levels and -5V undershoot pulses of less than 10 ns (measured at 50% point).
- Tested initially and after any design or process changes that may affect these parameters.
- See the last page of this specification for Group A subgroup testing information.
- T<sub>A</sub> is the "instant on" case temperature.

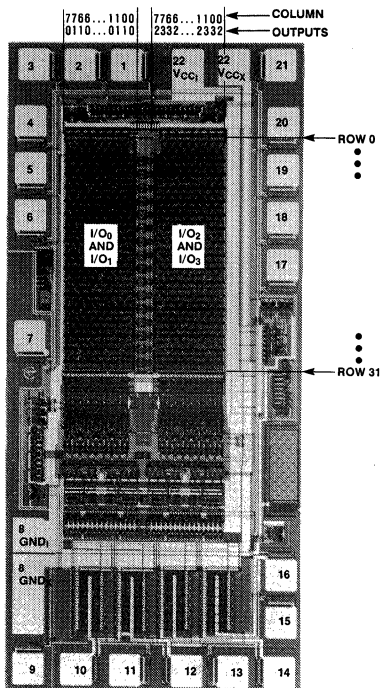
**Switching Characteristics Over the Operating Range<sup>[6, 7]</sup>**

| Parameters         | Description                    | Test Conditions | CY7C122-15 |      | CY7C122-25 |      | CY7C122-35 |      | Units |
|--------------------|--------------------------------|-----------------|------------|------|------------|------|------------|------|-------|
|                    |                                |                 | Min.       | Max. | Min.       | Max. | Min.       | Max. |       |
| <b>READ CYCLE</b>  |                                |                 |            |      |            |      |            |      |       |
| t <sub>RC</sub>    | Read Cycle Time                |                 | 15         |      | 25         |      | 35         |      | ns    |
| t <sub>ACS</sub>   | Chip Select Time               |                 |            | 8    |            | 15   |            | 25   | ns    |
| t <sub>ZRCS</sub>  | Chip Select to High-Z          | Note 8          |            | 12   |            | 20   |            | 30   | ns    |
| t <sub>AOS</sub>   | Output Enable Time             |                 |            | 8    |            | 15   |            | 25   | ns    |
| t <sub>ZROS</sub>  | Output Enable to High-Z        | Note 8          |            | 12   |            | 20   |            | 30   | ns    |
| t <sub>AA</sub>    | Address Access Time            |                 |            | 15   |            | 25   |            | 35   | ns    |
| <b>WRITE CYCLE</b> |                                |                 |            |      |            |      |            |      |       |
| t <sub>WC</sub>    | Write Cycle Time               |                 | 15         |      | 25         |      | 35         |      | ns    |
| t <sub>ZWS</sub>   | Write Disable to High-Z        | Note 8          |            | 12   |            | 20   |            | 30   | ns    |
| t <sub>WR</sub>    | Write Recovery Time            |                 |            | 12   |            | 20   |            | 25   | ns    |
| t <sub>W</sub>     | Write Pulse Width              | Note 6          | 11         |      | 15         |      | 25         |      | ns    |
| t <sub>WSD</sub>   | Data Setup Time Prior to Write |                 | 0          |      | 5          |      | 5          |      | ns    |
| t <sub>WHD</sub>   | Data Hold Time After Write     |                 | 2          |      | 5          |      | 5          |      | ns    |
| t <sub>WSA</sub>   | Address Setup Time             | Note 6          | 0          |      | 5          |      | 10         |      | ns    |
| t <sub>WHA</sub>   | Address Hold Time              |                 | 4          |      | 5          |      | 5          |      | ns    |
| t <sub>WSCS</sub>  | Chip Select Setup Time         |                 | 0          |      | 5          |      | 5          |      | ns    |
| t <sub>WHCS</sub>  | Chip Select Hold Time          |                 | 2          |      | 5          |      | 5          |      | ns    |

**Notes:**

6. t<sub>W</sub> measured at t<sub>WSA</sub> = min.; t<sub>WSA</sub> measured at t<sub>W</sub> = min.  
 7. Test conditions assume signal transition times of 5 ns or less for the -15 product and 10 ns or less for the -25 and -35 product. Timing reference levels of 1.5V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance as in *Figure 1a*.

8. Transition is measured at steady state HIGH level - 500 mV or steady state LOW level + 500 mV on the output from 1.5V level on the input with load shown in *Figure 1b*.

**Bit Map**

**Address Designators**

| Address Name   | Address Function | Pin Number |
|----------------|------------------|------------|
| A <sub>0</sub> | AX0              | 4          |
| A <sub>1</sub> | AX1              | 3          |
| A <sub>2</sub> | AX2              | 2          |
| A <sub>3</sub> | AX3              | 1          |
| A <sub>4</sub> | AX4              | 21         |
| A <sub>5</sub> | AY0              | 5          |
| A <sub>6</sub> | AY1              | 6          |
| A <sub>7</sub> | AY2              | 7          |

## AC Test Loads and Waveforms

### AC Test Loads

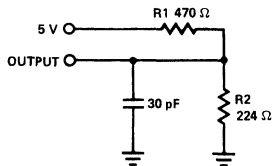


Figure 1a

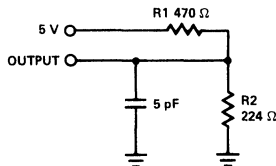


Figure 1b

0003-4

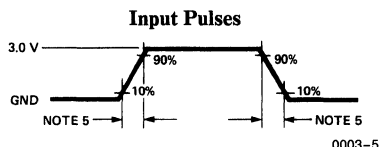


Figure 2

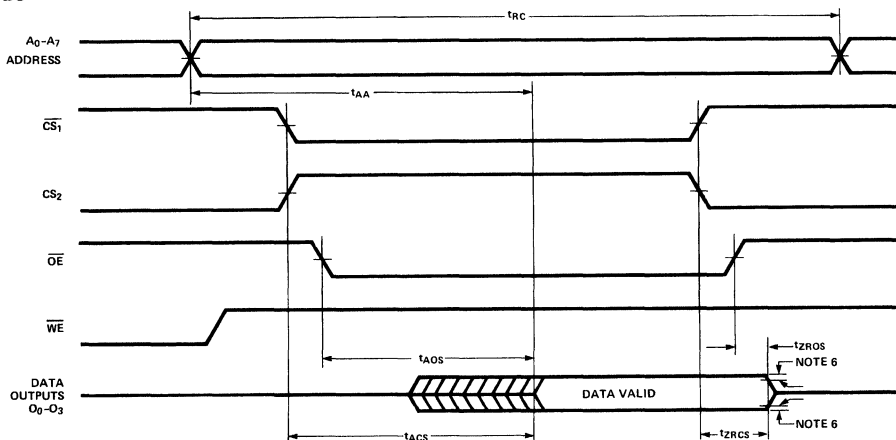
2

Equivalent to: THÉVENIN EQUIVALENT



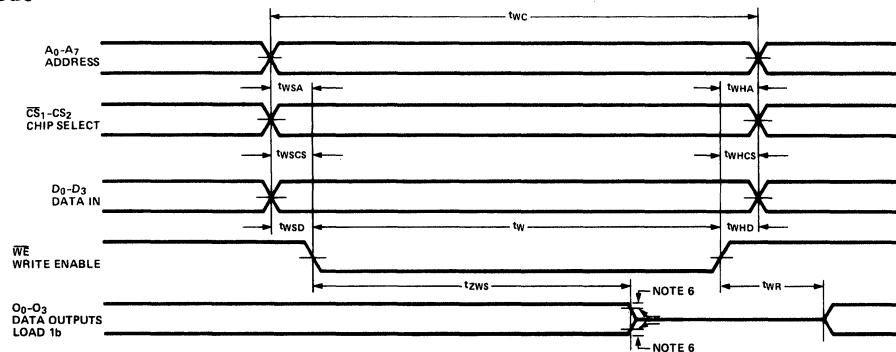
0003-6

## Read Mode



0003-7

## Write Mode

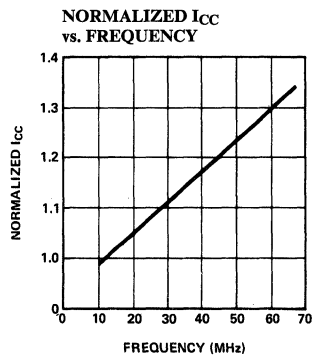
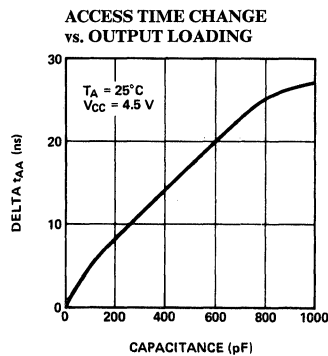
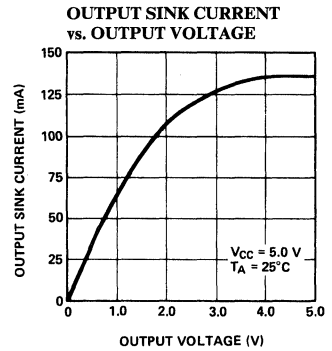
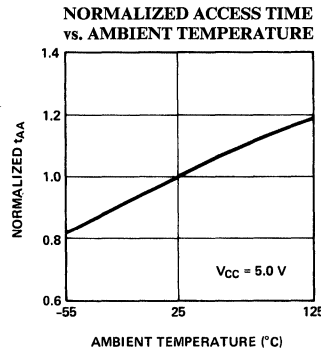
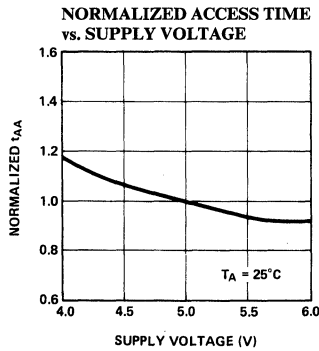
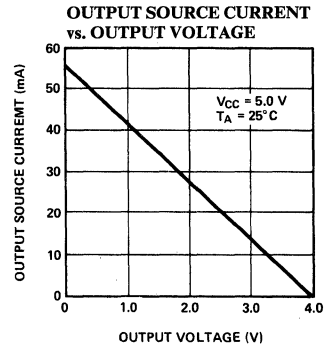
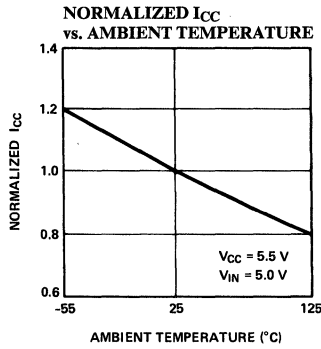
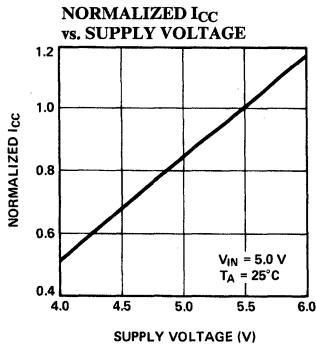


0003-8

(All above measurements referenced to 1.5V unless otherwise stated.)

**Note:**  
Timing diagram represents one solution which results in an optimum cycle time. Timing may be changed in various applications as long as the worst case limits are not violated.

Typical DC and AC Characteristics



**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 15         | CY7C122-15PC  | P7           | Commercial      |
|            | CY7C122-15DC  | D8           | Commercial      |
| 25         | CY7C122-25PC  | P7           | Commercial      |
|            | CY7C122-25DC  | D8           | Commercial      |
|            | CY7C122-25LC  | L53          | Commercial      |
|            | CY7C122-25DMB | D8           | Military        |
| 35         | CY7C122-35PC  | P7           | Commercial      |
|            | CY7C122-35DC  | D8           | Commercial      |
|            | CY7C122-35LC  | L53          | Commercial      |
|            | CY7C122-35DMB | D8           | Military        |
|            | CY7C122-35LMB | L53          | Military        |



**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |

**Switching Characteristics**

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>ACS</sub>   | 7,8,9,10,11 |
| t <sub>AOS</sub>   | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>WR</sub>    | 7,8,9,10,11 |
| t <sub>w</sub>     | 7,8,9,10,11 |
| t <sub>WSD</sub>   | 7,8,9,10,11 |
| t <sub>WHD</sub>   | 7,8,9,10,11 |
| t <sub>WSA</sub>   | 7,8,9,10,11 |
| t <sub>WHA</sub>   | 7,8,9,10,11 |
| t <sub>WSCS</sub>  | 7,8,9,10,11 |
| t <sub>WHCS</sub>  | 7,8,9,10,11 |

Document #: 38-00025-B



**Features**

- 256 x 4 static RAM for control store in high speed computers
- CMOS for optimum speed/power
- High speed
  - 7 ns (commercial)
  - 10 ns (military)
- Low power
  - 660 mW (commercial)
  - 825 mW (military)
- Separate inputs and outputs
- 5 volt power supply  $\pm 10\%$  tolerance both commercial and military
- TTL compatible inputs and outputs
- 24 pin
- 300 MIL package

**Functional Description**

The CY7C123 is a high performance CMOS static RAM organized as 256 words x 4 bits. Easy memory expansion is provided by an active LOW chip select one ( $\overline{CS}_1$ ) input, an active HIGH chip select two ( $CS_2$ ) input, and three-state outputs.

An active LOW write enable input ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When the chip select one ( $\overline{CS}_1$ ) and write enable ( $\overline{WE}$ ) inputs are LOW and the chip select two ( $CS_2$ ) input is HIGH, the information on the four data inputs  $D_0$  to  $D_3$  is written into the addressed memory word and the output circuitry is preconditioned so that the write data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write re-

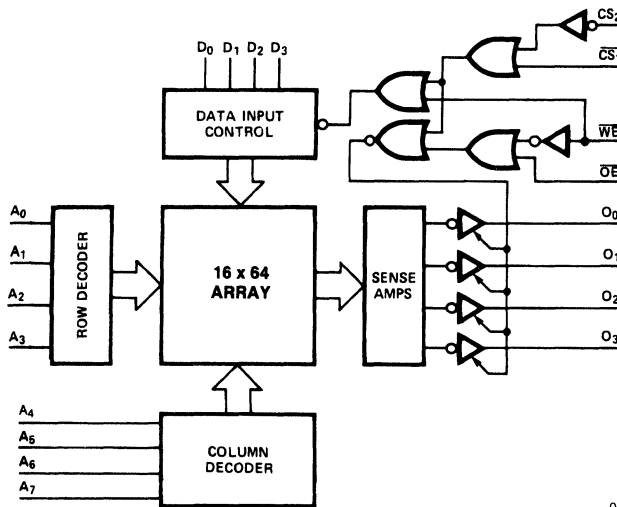
covery times by eliminating the “write recovery glitch.”

Reading is performed with the chip select one ( $\overline{CS}_1$ ) input LOW, the chip select two input ( $CS_2$ ) and write enable ( $\overline{WE}$ ) inputs HIGH, and the output enable input ( $\overline{OE}$ ) LOW. The information stored in the addressed word is read out on the four non-inverting outputs  $O_0$  to  $O_3$ .

The outputs of the memory go to an active high impedance state whenever chip select one ( $\overline{CS}_1$ ) is HIGH, chip select two ( $CS_2$ ) is LOW, output enable ( $\overline{OE}$ ) is HIGH, or during the writing operation when write enable ( $\overline{WE}$ ) is LOW.

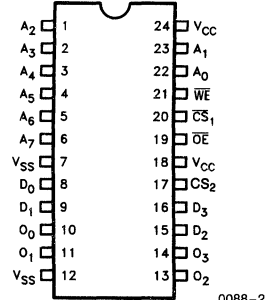
A die coat is used to insure alpha immunity.

**Logic Block Diagram**

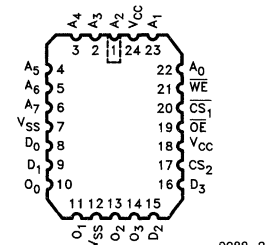


0088-1

**Pin Configurations**



0088-2



0088-3

**Selection Guide**

|                                |            | 7C123-7 | 7C123-9 | 7C123-10 | 7C123-12 | 7C123-15 |
|--------------------------------|------------|---------|---------|----------|----------|----------|
| Maximum Access Time (ns)       | Commercial | 7       | 9       | NA       | 12       | NA       |
|                                | Military   | NA      | NA      | 10       | 12       | 15       |
| Maximum Operating Current (mA) | Commercial | 120     | 120     | NA       | 120      | NA       |
|                                | Military   | NA      | NA      | 150      | 150      | 150      |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
 Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential  
 Pins 24 & 18 to Pins 7 & 12 ..... -0.5V to +7.0V

DC Voltage Applied to Outputs  
 in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Output Current, into Outputs (Low) ..... 20 mA

Latchup Current ..... >200 mA

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[2]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Logic Table

| Inputs |                 |                 |    |                                | Outputs                        | Mode             |
|--------|-----------------|-----------------|----|--------------------------------|--------------------------------|------------------|
| OE     | CS <sub>1</sub> | CS <sub>2</sub> | WE | D <sub>0</sub> -D <sub>3</sub> |                                |                  |
| X      | H               | X               | X  | X                              | High Z                         | Not Selected     |
| X      | X               | L               | X  | X                              | High Z                         | Not Selected     |
| L      | L               | H               | H  | X                              | O <sub>0</sub> -O <sub>3</sub> | Read Stored Data |
| X      | L               | H               | L  | L                              | High Z                         | Write "0"        |
| X      | L               | H               | L  | H                              | High Z                         | Write "1"        |
| H      | L               | H               | H  | X                              | High Z                         | Output Disabled  |

Notes: H = HIGH Voltage    L = LOW Voltage    X = Don't Care  
 High Z = High Impedance

### Electrical Characteristics Over the Operating Range<sup>[3]</sup>

| Parameters      | Description                | Test Conditions   | 7C123-7<br>7C123-9 |                 | 7C123-10<br>7C123-15 |                 | 7C123-12 |                 | Units |
|-----------------|----------------------------|---|--------------------|-----------------|----------------------|-----------------|----------|-----------------|-------|
|                 |                            |   | Min.               | Max.            | Min.                 | Max.            | Min.     | Max.            |       |
| V <sub>OH</sub> | Output HIGH Voltage        | V <sub>CC</sub> = Min., I <sub>OH</sub> = -5.2 mA                       | 2.4                |                 | 2.4                  |                 | 2.4      |                 | V     |
| V <sub>OL</sub> | Output LOW Voltage         | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA                        |                    | 0.4             |                      | 0.4             |          | 0.4             | V     |
| V <sub>IH</sub> | Input HIGH Voltage         |   | 2.2                | V <sub>CC</sub> | 2.2                  | V <sub>CC</sub> | 2.2      | V <sub>CC</sub> | V     |
| V <sub>IL</sub> | Input LOW Voltage          |   | -3.0               | 0.8             | -3.0                 | 0.8             | -3.0     | 0.8             | V     |
| I <sub>IX</sub> | Input Load Current         | V <sub>SS</sub> ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                      | -10                | 10              | -10                  | 10              | -10      | 10              | μA    |
| I <sub>OZ</sub> | Output Current<br>(High-Z) | V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub><br>Output Disabled | -10                | +10             | -10                  | +10             | -10      | +10             | μA    |
| I <sub>CC</sub> | Power Supply<br>Current    | V <sub>CC</sub> = Max.,<br>I <sub>OUT</sub> = 0 mA                      | Commercial         | 120             | NA                   |                 | 120      |                 | mA    |
|                 |                            |   | Military           |                 | NA                   | 150             |          | 150             | mA    |

### Capacitance<sup>[1]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 4    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 7    |       |

#### Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. T<sub>A</sub> is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.

**Switching Characteristics Over the Operating Range<sup>[3]</sup>**

| Parameters         | Description                   | Test Conditions | 7C123-7 |      | 7C123-9 |      | 7C123-10 |      | 7C123-12 |      | 7C123-15 |      | Units |
|--------------------|-------------------------------|-----------------|---------|------|---------|------|----------|------|----------|------|----------|------|-------|
|                    |                               |                 | Min.    | Max. | Min.    | Max. | Min.     | Max. | Min.     | Max. | Min.     | Max. |       |
| <b>READ CYCLE</b>  |                               |                 |         |      |         |      |          |      |          |      |          |      |       |
| t <sub>RC</sub>    | Read Cycle Time               |                 | 7       |      | 9       |      | 10       |      | 12       |      | 15       |      | ns    |
| t <sub>AA</sub>    | Address Access Time           |                 |         | 7    |         | 9    |          | 10   |          | 12   |          | 15   | ns    |
| t <sub>ACS</sub>   | Chip Select Time              |                 |         | 7    |         | 8    |          | 8    |          | 8    |          | 10   | ns    |
| t <sub>DOE</sub>   | Output Enable Time            |                 |         | 7    |         | 8    |          | 8    |          | 8    |          | 10   | ns    |
| t <sub>HZCS</sub>  | Chip Select to Output Hi-Z    | Notes 4, 5      |         | 5    |         | 6    |          | 6    |          | 6.5  |          | 8    | ns    |
| t <sub>HZOE</sub>  | Output Enable to Out Hi-Z     | Note 4          |         | 5    |         | 6    |          | 6    |          | 6.5  |          | 8    | ns    |
| t <sub>LZCS</sub>  | Chip Select to Out Low-Z      | Notes 4, 5      | 2       |      | 2       |      | 2        |      | 2        |      | 2        |      | ns    |
| t <sub>LZOE</sub>  | Output Enable to Out Low-Z    | Note 4          | 2       |      | 2       |      | 2        |      | 2        |      | 2        |      | ns    |
| <b>WRITE CYCLE</b> |                               |                 |         |      |         |      |          |      |          |      |          |      |       |
| t <sub>WC</sub>    | Write Cycle Time              |                 | 7       |      | 9       |      | 10       |      | 12       |      | 15       |      | ns    |
| t <sub>HZWE</sub>  | Write Enable to Hi-Z          |                 |         | 5.5  |         | 6    |          | 6    |          | 7    |          | 8    | ns    |
| t <sub>LZWE</sub>  | Write Enable to Low-Z         |                 | 2       |      | 2       |      | 2        |      | 2        |      | 2        |      | ns    |
| t <sub>PWE</sub>   | Write Pulse Width             |                 | 5       |      | 6.5     |      | 7        |      | 8        |      | 11       |      | ns    |
| t <sub>SD</sub>    | Data Setup to End of Write    |                 | 5       |      | 6       |      | 7        |      | 8        |      | 11       |      | ns    |
| t <sub>HD</sub>    | Data Hold Time After Write    |                 | 1       |      | 1       |      | 1        |      | 1        |      | 1        |      | ns    |
| t <sub>SA</sub>    | Add Setup to Start of Write   |                 | 0.5     |      | 1       |      | 1        |      | 2        |      | 2        |      | ns    |
| t <sub>HA</sub>    | Address Hold Time             |                 | 1.5     |      | 1.5     |      | 2        |      | 2        |      | 2        |      | ns    |
| t <sub>SCS</sub>   | CS Active Low to End of Write |                 | 5       |      | 6.5     |      | 7        |      | 8        |      | 11       |      | ns    |
| t <sub>AW</sub>    | Add Setup to End of Write     |                 | 5.5     |      | 7.5     |      | 8        |      | 10       |      | 13       |      | ns    |

**Notes:**

4. Transition is measured at steady state HIGH level – 500 mV or steady state LOW level + 500 mV on the output from 1.5V level on the input with load shown in *Figure 1b*.

5. At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device.

**2**

## AC Test Loads and Waveforms

### AC Test Loads

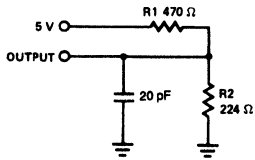


Figure 1a

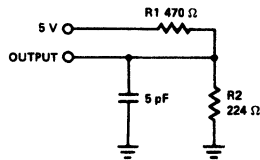


Figure 1b

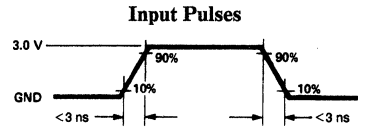


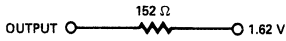
Figure 2

0088-4

0088-5

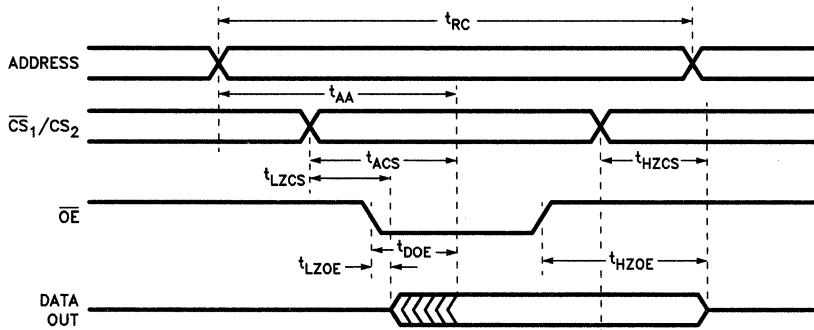
Equivalent to:

THÉVENIN EQUIVALENT



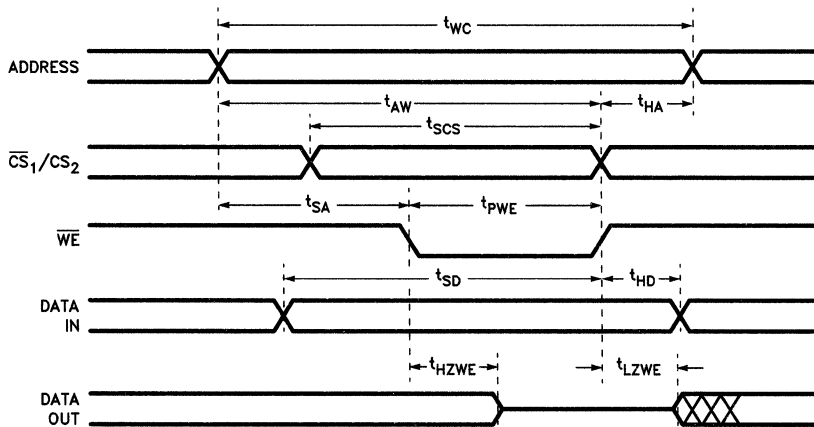
0088-6

## Read Mode



0088-11

## Write Mode



0088-12

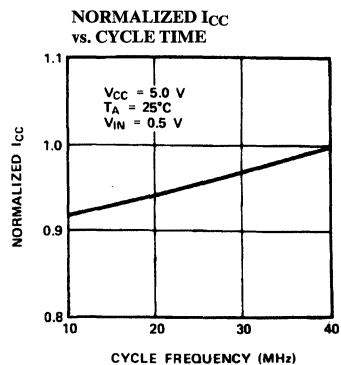
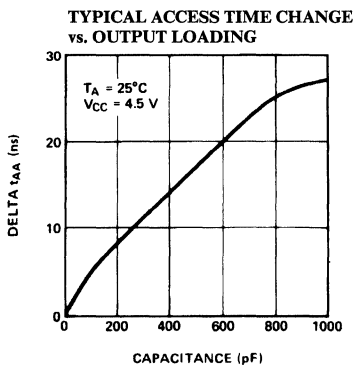
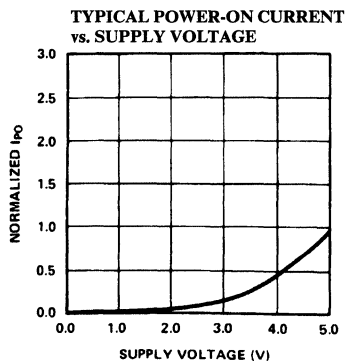
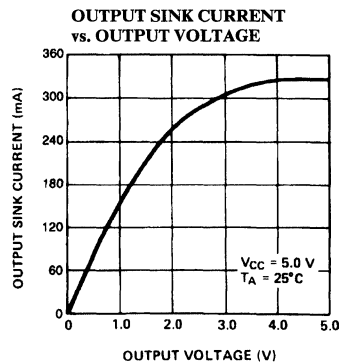
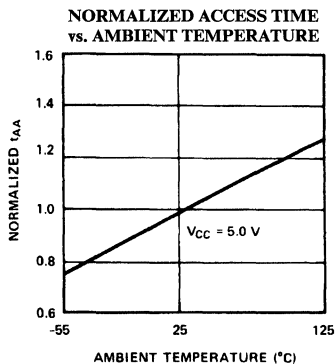
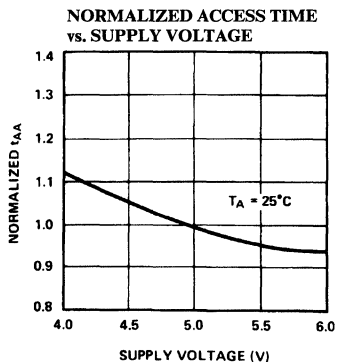
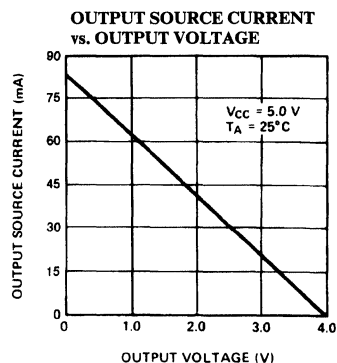
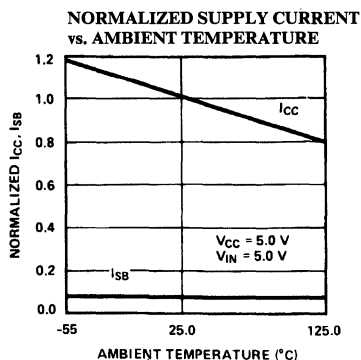
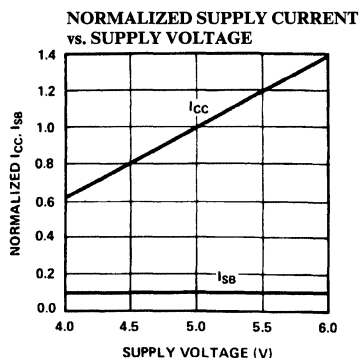
(All above measurements referenced to 1.5V unless otherwise stated.)

### Note:

Timing diagram represents one solution which results in an optimum cycle time. Timing may be changed in various applications as long as the worst case limits are not violated.

Typical DC and AC Characteristics

2



### Ordering Information

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 7          | CY7C123-7PC   | P13A         | Commercial      |
|            | CY7C123-7DC   | D14          |                 |
|            | CY7C123-7LC   | L53          |                 |
| 9          | CY7C123-9PC   | P13A         | Commercial      |
|            | CY7C123-9DC   | D14          |                 |
|            | CY7C123-9LC   | L53          |                 |
| 10         | CY7C123-10DMB | D14          | Military        |
|            | CY7C123-10LMB | L53          |                 |
|            | CY7C123-10KMB | K73          |                 |
| 12         | CY7C123-12PC  | P13A         | Commercial      |
|            | CY7C123-12DC  | D14          |                 |
|            | CY7C123-12LC  | L53          |                 |
|            | CY7C123-12DMB | D14          | Military        |
|            | CY7C123-12LMB | L53          |                 |
|            | CY7C123-12KMB | K73          |                 |
| 15         | CY7C123-15DMB | D14          | Military        |
|            | CY7C123-15LMB | L53          |                 |
|            | CY7C123-15KMB | K73          |                 |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>Ix</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |

2

#### Switching Characteristics

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>ACS</sub>   | 7,8,9,10,11 |
| t <sub>DOE</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SCS</sub>   | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |

Document #: 38-00060-D





**Features**

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed—35 ns
- Low active power
  - 660 mW (commercial)
  - 825 mW (military)
- Low standby power
  - 110 mW
- SOJ package
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

**Functional Description**

The CY7C128 is a high performance CMOS static RAM organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ), and active LOW output enable ( $\overline{OE}$ ) and three-state drivers. The CY7C128 has an automatic power-down feature, reducing the power consumption by 83% when deselected.

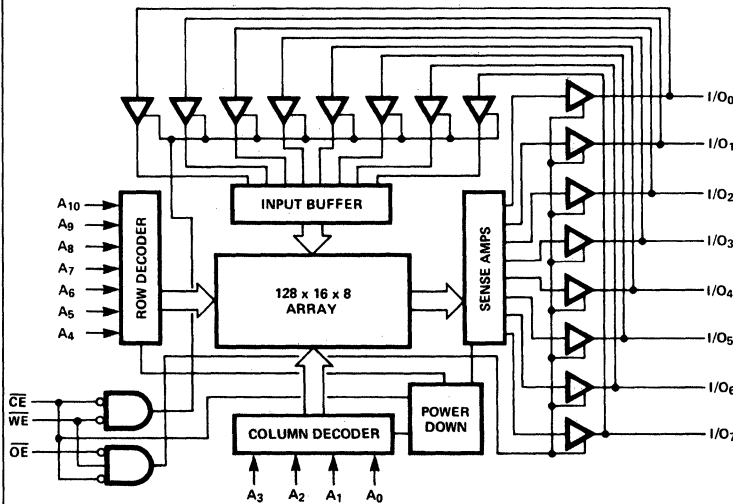
An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When the chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW, data on the eight data input/output pins ( $I/O_0$  through  $I/O_7$ ) is written into the memory loca-

tion addressed by the address present on the address pins ( $A_0$  through  $A_{10}$ ). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{CE}$  and  $\overline{OE}$  active LOW, while ( $\overline{WE}$ ) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

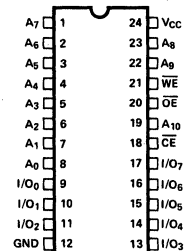
The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH.

The 7C128 utilizes a die coat to ensure alpha immunity.

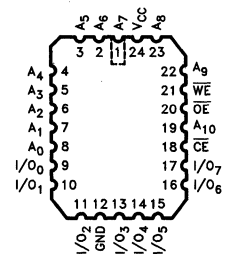
**Logic Block Diagram**



**Pin Configurations**



0036-2



0036-3

**Selection Guide**

|                                |            | 7C128-35 | 7C128-45 | 7C128-55 |
|--------------------------------|------------|----------|----------|----------|
| Maximum Access Time (ns)       |            | 35       | 45       | 55       |
| Maximum Operating Current (mA) | Commercial | 120      | 120      | 90       |
|                                | Military   |          | 130      | 100      |
| Maximum Standby Current (mA)   | Commercial | 20       | 20       | 20       |
|                                | Military   |          | 20       | 20       |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature .....                                   | -65°C to +150°C |
| Ambient Temperature with Power Applied .....                | -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State .....         | -0.5V to +7.0V  |
| DC Input Voltage .....                                      | -3.0V to +7.0V  |
| Output Current into Outputs (Low) .....                     | 20 mA           |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | > 2001V<br>(Per MIL-STD-883 Method 3015) |
| Latch-up Current .....         | > 200 mA                                 |

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[4]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[3]</sup>

| Parameters      | Description                                  | Test Conditions   | 7C128                    |                 | Units |
|-----------------|--|---|--------------------------|-----------------|-------|
|                 |  |   | Min.                     | Max.            |       |
| V <sub>OH</sub> | Output HIGH Voltage                          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA         | 2.4                      |                 | V     |
| V <sub>OL</sub> | Output LOW Voltage                           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA          |                          | 0.4             | V     |
| V <sub>IH</sub> | Input HIGH Voltage                           |   | 2.0                      | V <sub>CC</sub> | V     |
| V <sub>IL</sub> | Input LOW Voltage                            |   | -3.0                     | 0.8             | V     |
| I <sub>Ix</sub> | Input Load Current                           | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                    | -10                      | 10              | μA    |
| I <sub>OZ</sub> | Output Leakage Current                       | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub><br>Output Disabled | -40                      | 40              | μA    |
| I <sub>OS</sub> | Output Short Circuit Current <sup>[1]</sup>  | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND            |                          | -300            | mA    |
| I <sub>CC</sub> | V <sub>CC</sub> Operating Supply Current     | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA         | Commercial -25, -35, -45 | 120             | mA    |
|                 |  |   | Commercial -55           | 90              | mA    |
|                 |  |   | Military -35             | 150             | mA    |
|                 |  |   | Military -45             | 130             | mA    |
|                 |  |   | Military -55             | 100             | mA    |
| I <sub>SB</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> ,<br>CE ≥ V <sub>IH</sub>            | Commercial               | 20              | mA    |
|                 |  |   | Military*                | 20              |       |

\*35 ns and 55 ns only

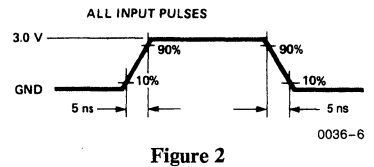
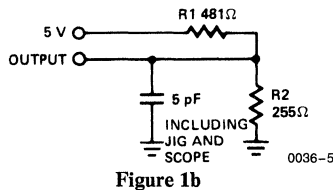
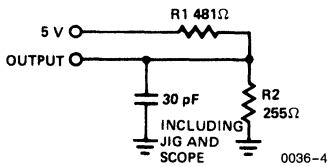
### Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 7    |       |

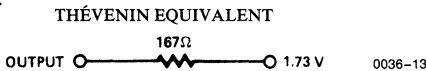
#### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- See the last page of this specification for Group A subgroup testing information.
- T<sub>A</sub> is the "instant on" case temperature.

### AC Test Loads and Waveforms



Equivalent to:

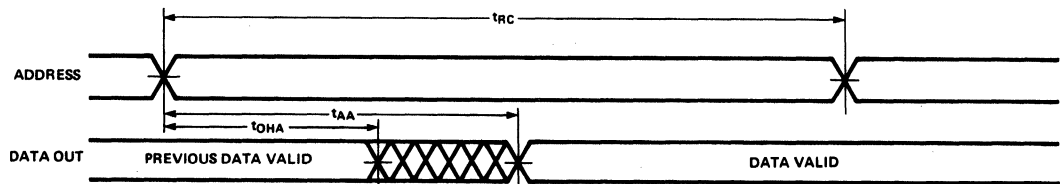


**Switching Characteristics Over Operating Range**<sup>[3, 6]</sup>

| Parameters                        | Description                                      | 7C128-35 |      | 7C128-45 |      | 7C128-55 |      | Units |
|-----------------------------------|--|----------|------|----------|------|----------|------|-------|
|                                   |  | Min.     | Max. | Min.     | Max. | Min.     | Max. |       |
| <b>READ CYCLE</b>                 |  |          |      |          |      |          |      |       |
| t <sub>RC</sub>                   | Read Cycle Time                                  | 35       |      | 45       |      | 55       |      | ns    |
| t <sub>AA</sub>                   | Address to Data Valid                            |          | 35   |          | 45   |          | 55   | ns    |
| t <sub>OHA</sub>                  | Data Hold from Address Change                    | 5        |      | 5        |      | 5        |      | ns    |
| t <sub>ACE</sub>                  | $\overline{CE}$ LOW to Data Valid                |          | 35   |          | 45   |          | 55   | ns    |
| t <sub>DOE</sub>                  | $\overline{OE}$ LOW to Data Valid                |          | 15   |          | 20   |          | 25   | ns    |
| t <sub>LZOE</sub>                 | $\overline{OE}$ LOW to Low Z                     | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>HZOE</sub>                 | $\overline{OE}$ HIGH to High Z <sup>[7]</sup>    |          | 15   |          | 15   |          | 20   | ns    |
| t <sub>LZCE</sub>                 | $\overline{CE}$ LOW to Low Z <sup>[8]</sup>      | 5        |      | 5        |      | 5        |      | ns    |
| t <sub>HZCE</sub>                 | $\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup> |          | 15   |          | 20   |          | 20   | ns    |
| t <sub>PU</sub>                   | $\overline{CE}$ LOW to Power Up                  | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>PD</sub>                   | $\overline{CE}$ HIGH to Power Down               |          | 20   |          | 25   |          | 25   | ns    |
| <b>WRITE CYCLE</b> <sup>[9]</sup> |  |          |      |          |      |          |      |       |
| t <sub>WC</sub>                   | Write Cycle Time                                 | 35       |      | 45       |      | 55       |      | ns    |
| t <sub>SCE</sub>                  | $\overline{CE}$ LOW to Write End                 | 30       |      | 40       |      | 50       |      | ns    |
| t <sub>AW</sub>                   | Address Set-up to Write End                      | 30       |      | 40       |      | 50       |      | ns    |
| t <sub>HA</sub>                   | Address Hold from Write End                      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>SA</sub>                   | Address Set-up to Write Start                    | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>PWE</sub>                  | WE Pulse Width                                   | 20       |      | 20       |      | 25       |      | ns    |
| t <sub>SD</sub>                   | Data Set-up to Write End                         | 15       |      | 20       |      | 25       |      | ns    |
| t <sub>HD</sub>                   | Data Hold from Write End                         | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>HZWE</sub>                 | WE LOW to High Z <sup>[7]</sup>                  |          | 15   |          | 15   |          | 20   | ns    |
| t <sub>LZWE</sub>                 | WE HIGH to Low Z                                 | 0        |      | 0        |      | 0        |      | ns    |

**Notes:**

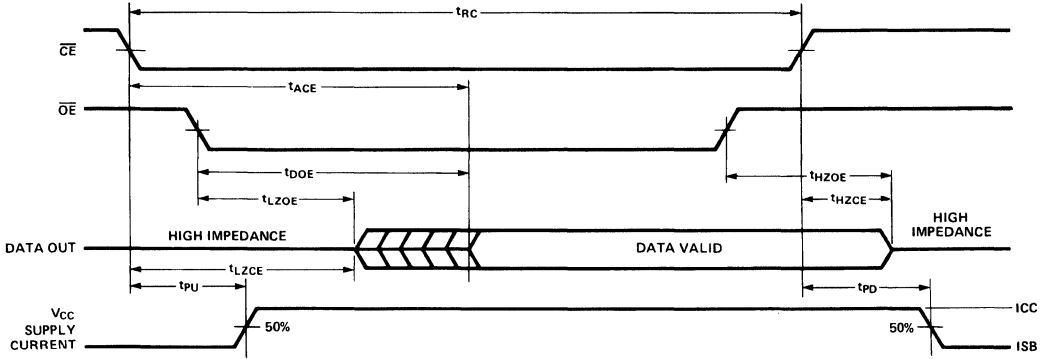
- Data I/O Pins enter high-impedance state, as shown, when  $\overline{OE}$  is held LOW during write.
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- WE is HIGH for read cycle.
- Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  = V<sub>IL</sub>.
- Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms**
**Read Cycle No. 1 (Notes 10, 11)**


Switching Waveforms (Continued)

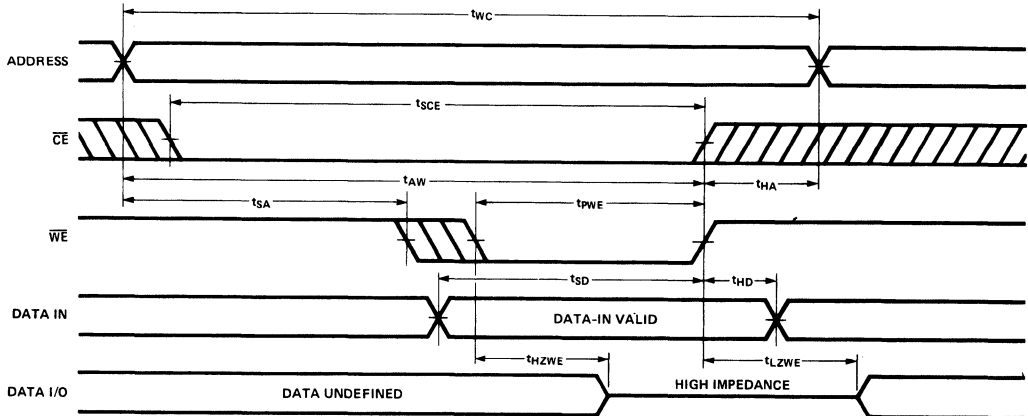
Read Cycle No. 2 (Notes 10, 12)

2



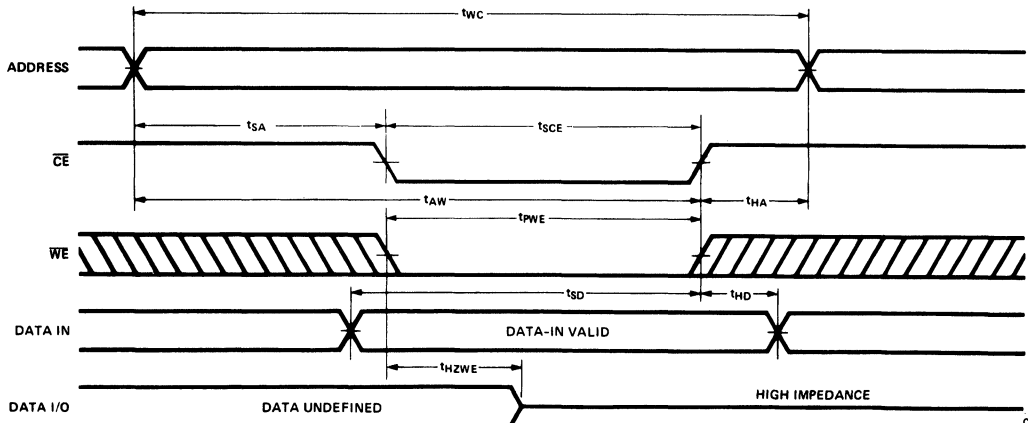
0036-8

Write Cycle No. 1 ( $\overline{WE}$  Controlled) (Notes 5, 9)



0036-9

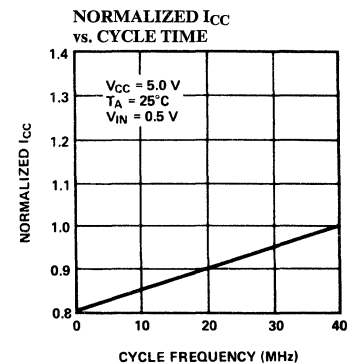
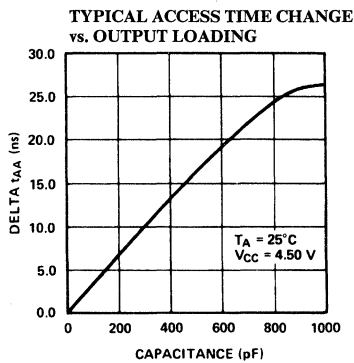
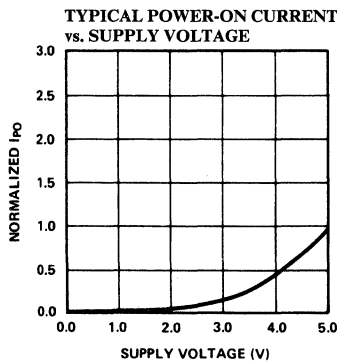
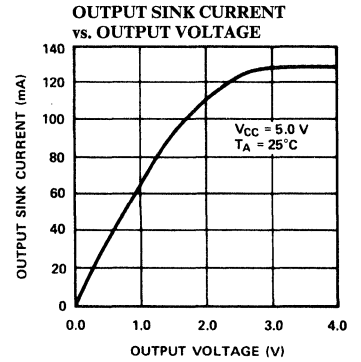
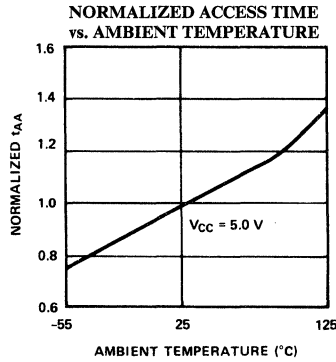
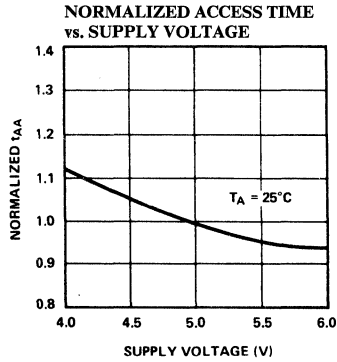
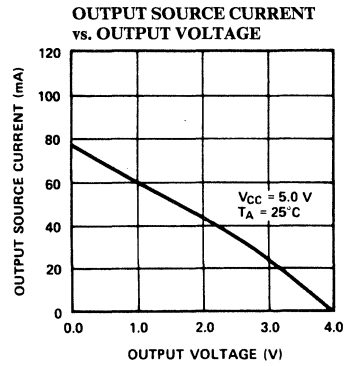
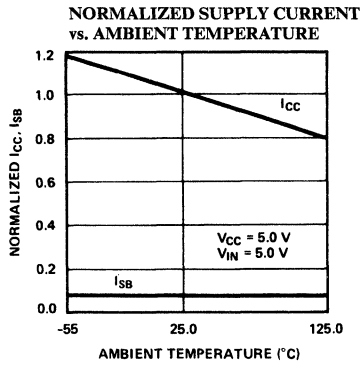
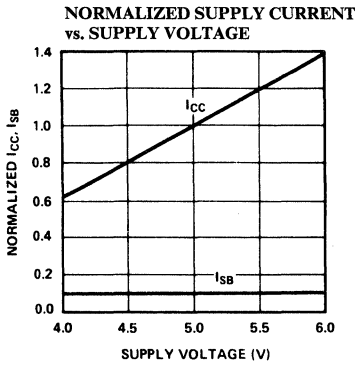
Write Cycle No. 2 ( $\overline{CE}$  Controlled) (Notes 5, 9)



0036-10

Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

Typical DC and AC Characteristics



**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 35         | CY7C128-35PC  | P13          | Commercial      |
|            | CY7C128-35VC  | V13          |                 |
|            | CY7C128-35DC  | D14          |                 |
|            | CY7C128-35LC  | L53          |                 |
|            | CY7C128-35KMB | K73          | Military        |
| 45         | CY7C128-45PC  | P13          | Commercial      |
|            | CY7C128-45VC  | V13          |                 |
|            | CY7C128-45DC  | D14          |                 |
|            | CY7C128-45LC  | L53          |                 |
|            | CY7C128-45DMB | D14          | Military        |
|            | CY7C128-45LMB | L53          |                 |
|            | CY7C128-45KMB | K73          |                 |
| 55         | CY7C128-55PC  | P13          | Commercial      |
|            | CY7C128-55VC  | V13          |                 |
|            | CY7C128-55DC  | D14          |                 |
|            | CY7C128-55LC  | L53          |                 |
|            | CY7C128-55DMB | D14          | Military        |
|            | CY7C128-55LMB | L53          |                 |
|            | CY7C128-55KMB | K73          |                 |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB</sub>      | 1,2,3     |

**Switching Characteristics**

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>ACE</sub>   | 7,8,9,10,11 |
| t <sub>DOE</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>SCE</sub>   | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |

Document #: 38-00026-C



**Features**

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed—20 ns
- Low active power  
— 440 mW (commercial)  
— 550 mW (military)
- Low standby power  
— 110 mW
- SOJ package
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge
- $V_{IH}$  of 2.2V

**Functional Description**

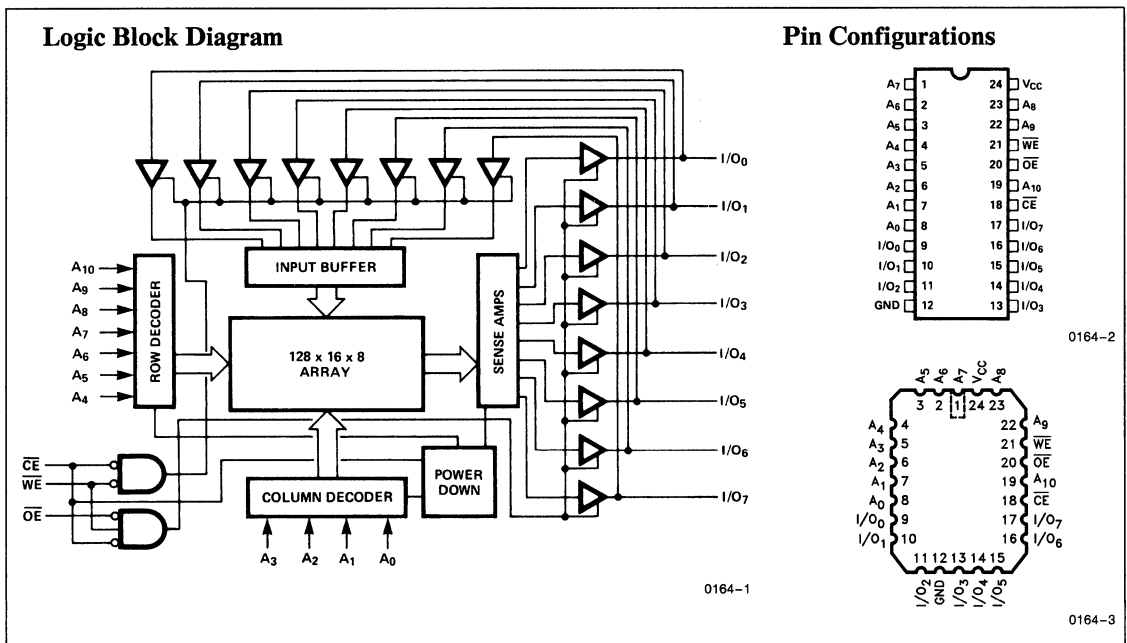
The CY7C128A is a high performance CMOS static RAM organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ), and active LOW output enable ( $\overline{OE}$ ) and three-state drivers. The CY7C128A has an automatic power-down feature, reducing the power consumption by 83% when deselected.

An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When the chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW, data on the eight data input/output pins ( $I/O_0$  through  $I/O_7$ ) is written into the memory loca-

tion addressed by the address present on the address pins ( $A_0$  through  $A_{10}$ ). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{CE}$  and  $\overline{OE}$  active LOW, while ( $\overline{WE}$ ) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH.

The 7C128A utilizes a die coat to ensure alpha immunity.



**Selection Guide**

|                                |            | 7C128A-20 | 7C128A-25 | 7C128A-35 | 7C128A-45 | 7C128A-55 |
|--------------------------------|------------|-----------|-----------|-----------|-----------|-----------|
| Maximum Access Time (ns)       |            | 20        | 25        | 35        | 45        | 55        |
| Maximum Operating Current (mA) | Commercial | 100       | 100       | 100       | 100       | 80        |
|                                | Military   |           | 125       | 100       | 100       | 100       |
| Maximum Standby Current (mA)   | Commercial | 40/20     | 20        | 20        | 20        | 20        |
|                                | Military   |           | 40        | 20        | 20        | 20        |



## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature .....                                   | -65°C to +150°C |
| Ambient Temperature with Power Applied .....                | -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State .....         | -0.5V to +7.0V  |
| DC Input Voltage .....                                      | -3.0V to +7.0V  |
| Output Current into Outputs (Low) .....                     | 20 mA           |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | > 2001V<br>(Per MIL-STD-883 Method 3015) |
| Latch-up Current .....         | > 200 mA                                 |

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ±10%         |
| Military <sup>[4]</sup> | -55°C to +125°C     | 5V ±10%         |

## Electrical Characteristics Over Operating Range<sup>[3]</sup>

| Parameters       | Description                                  | Test Conditions  | 7C128A-20 |                 | 7C128A-25, 35, 45 |                 | 7C128A-55 |                 | Units |
|------------------|--|--|-----------|-----------------|-------------------|-----------------|-----------|-----------------|-------|
|                  |  |  | Min.      | Max.            | Min.              | Max.            | Min.      | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA  | 2.4       |                 | 2.4               |                 | 2.4       |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA   |           | 0.4             |                   | 0.4             |           | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                           |  | 2.2       | V <sub>CC</sub> | 2.2               | V <sub>CC</sub> | 2.2       | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage <sup>[4A]</sup>            |  | -0.5      | 0.8             | -0.5              | 0.8             | -0.5      | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current                           | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -10       | 10              | -10               | 10              | -10       | 10              | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                       | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub><br>Output Disabled  | -10       | +10             | -10               | +10             | -10       | +10             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>  | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND   |           | -300            |                   | -300            |           | -300            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current     | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA  | Coml.     |                 |                   | 100             |           | 80              | mA    |
|                  |  |  | Mil.      | 25              |                   |                 | 125       | 100             |       |
|                  |  |  |           | 35, 45          |                   |                 | 100       |                 |       |
| I <sub>SB1</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> ,<br>CE <sub>1</sub> ≥ V <sub>IH</sub> ,<br>Min. Duty Cycle = 100%  | Coml.     |                 |                   | 40              |           | 20              | mA    |
|                  |  |  | Mil.      | 25              |                   |                 | 40        | 20              |       |
|                  |  |  |           | 35, 45          |                   |                 | 20        |                 |       |
| I <sub>SB2</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> ,<br>CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.3V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V<br>or V <sub>IN</sub> ≤ 0.3V | Coml.     |                 |                   | 20              |           | 20              | mA    |
|                  |  |  | Mil.      |                 |                   |                 | 20        | 20              |       |

\*35 ns and 55 ns only

## Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 7    |       |

### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- See the last page of this specification for Group A subgroup testing information.
- T<sub>A</sub> is the "instant on" case temperature.
- 4A. V<sub>IL</sub> min. = -3.0V for pulse durations less than 30 ns.

## AC Test Loads and Waveforms

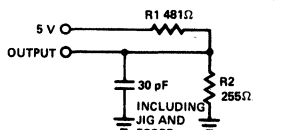


Figure 1a

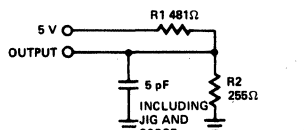


Figure 1b

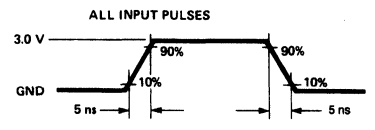
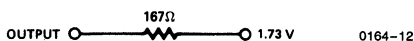


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



## Switching Characteristics Over Operating Range<sup>[3, 6]</sup>

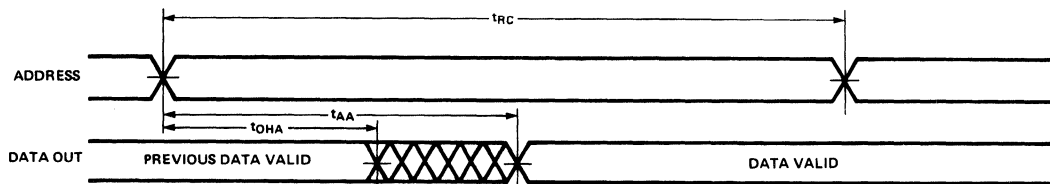
| Parameters                       | Description                                      | 7C128A-20 |      | 7C128A-25 |      | 7C128A-35 |      | 7C128A-45 |      | 7C128A-55 |      | Units |
|----------------------------------|--|-----------|------|-----------|------|-----------|------|-----------|------|-----------|------|-------|
|                                  |  | Min.      | Max. | Min.      | Max. | Min.      | Max. | Min.      | Max. | Min.      | Max. |       |
| <b>READ CYCLE</b>                |  |           |      |           |      |           |      |           |      |           |      |       |
| t <sub>RC</sub>                  | Read Cycle Time                                  | 20        |      | 25        |      | 35        |      | 45        |      | 55        |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid                            |           | 20   |           | 25   |           | 35   |           | 45   |           | 55   | ns    |
| t <sub>OHA</sub>                 | Data Hold from Address Change                    | 5         |      | 5         |      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>ACE</sub>                 | $\overline{CE}$ LOW to Data Valid                |           | 20   |           | 25   |           | 35   |           | 45   |           | 55   | ns    |
| t <sub>DOE</sub>                 | $\overline{OE}$ LOW to Data Valid                |           | 10   |           | 12   |           | 15   |           | 20   |           | 25   | ns    |
| t <sub>LZOE</sub>                | $\overline{OE}$ LOW to Low Z                     | 3         |      | 3         |      | 3         |      | 3         |      | 3         |      | ns    |
| t <sub>HZOE</sub>                | $\overline{OE}$ HIGH to High Z <sup>[7]</sup>    |           | 8    |           | 10   |           | 12   |           | 15   |           | 20   | ns    |
| t <sub>LZCE</sub>                | $\overline{CE}$ LOW to Low Z <sup>[8]</sup>      | 5         |      | 5         |      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>HZCE</sub>                | $\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup> |           | 8    |           | 10   |           | 15   |           | 15   |           | 20   | ns    |
| t <sub>PU</sub>                  | $\overline{CE}$ LOW to Power Up                  | 0         |      | 0         |      | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>PD</sub>                  | $\overline{CE}$ HIGH to Power Down               |           | 20   |           | 20   |           | 20   |           | 25   |           | 25   | ns    |
| <b>WRITE CYCLE<sup>[9]</sup></b> |  |           |      |           |      |           |      |           |      |           |      |       |
| t <sub>WC</sub>                  | Write Cycle Time                                 | 20        |      | 20        |      | 25        |      | 40        |      | 50        |      | ns    |
| t <sub>SCE</sub>                 | $\overline{CE}$ LOW to Write End                 | 15        |      | 20        |      | 25        |      | 30        |      | 40        |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End                      | 15        |      | 20        |      | 25        |      | 30        |      | 40        |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End                      | 0         |      | 0         |      | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                    | 0         |      | 0         |      | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>PWE</sub>                 | WE Pulse Width                                   | 15        |      | 15        |      | 20        |      | 20        |      | 25        |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End                         | 10        |      | 10        |      | 15        |      | 15        |      | 25        |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End                         | 0         |      | 0         |      | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>HZWE</sub>                | $\overline{WE}$ LOW to High Z <sup>[7]</sup>     |           | 7    |           | 7    |           | 10   |           | 15   |           | 20   | ns    |
| t <sub>LZWE</sub>                | $\overline{WE}$ HIGH to Low Z                    | 5         |      | 5         |      | 5         |      | 5         |      | 5         |      | ns    |

**Notes:**

- Data I/O Pins enter high-impedance state, as shown, when  $\overline{OE}$  is held LOW during write.
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  = V<sub>IL</sub>.
- Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

## Switching Waveforms

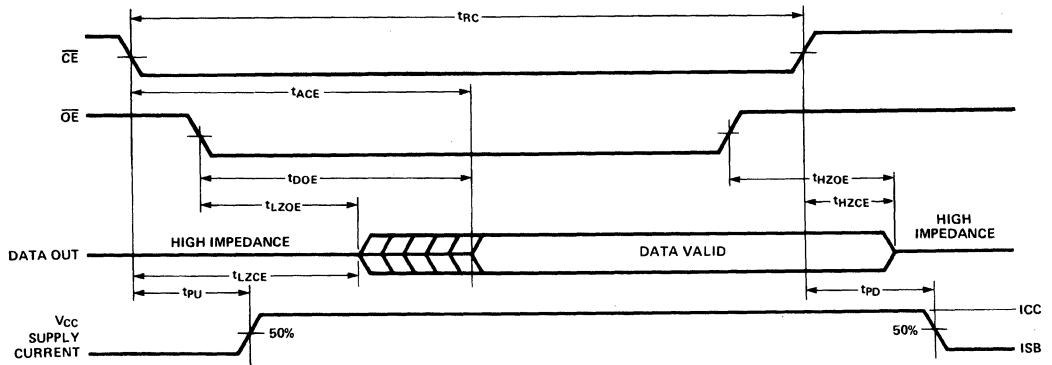
### Read Cycle No. 1 (Notes 10, 11)



0164-7

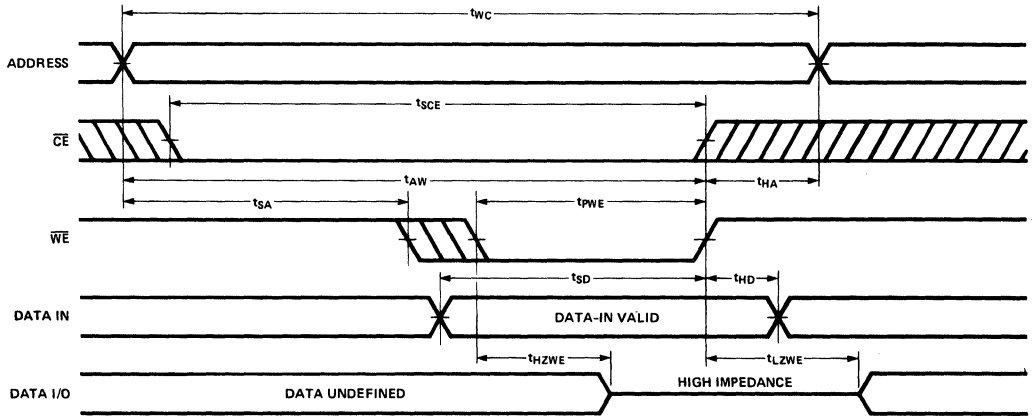
### Switching Waveforms (Continued)

#### Read Cycle No. 2 (Notes 10, 12)



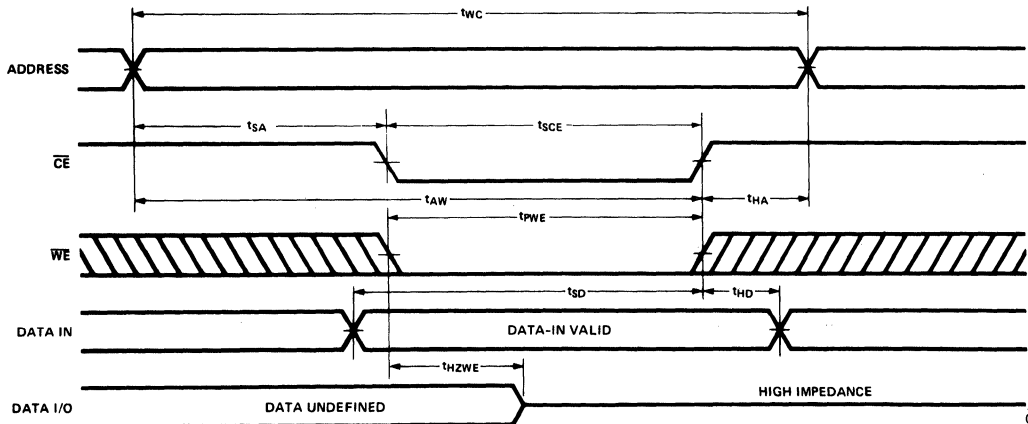
0164-8

#### Write Cycle No. 1 ( $\overline{WE}$ Controlled) (Notes 5, 9)



0164-9

#### Write Cycle No. 2 ( $\overline{CE}$ Controlled) (Notes 5, 9)

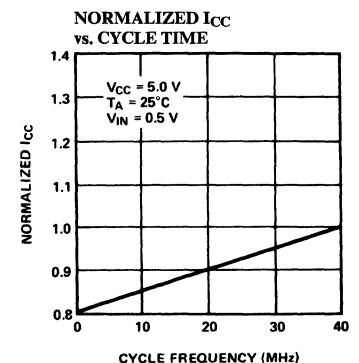
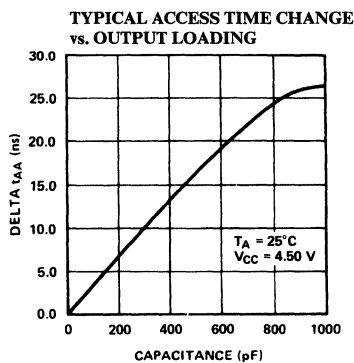
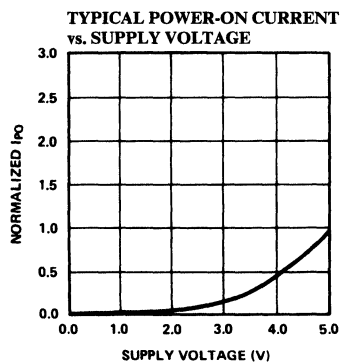
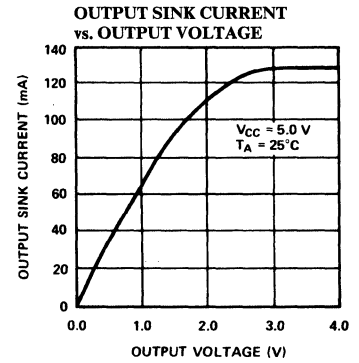
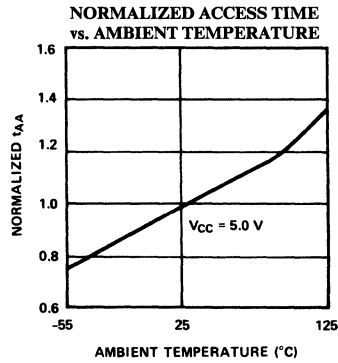
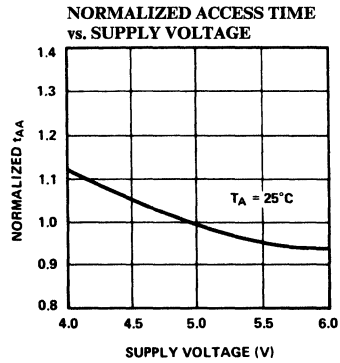
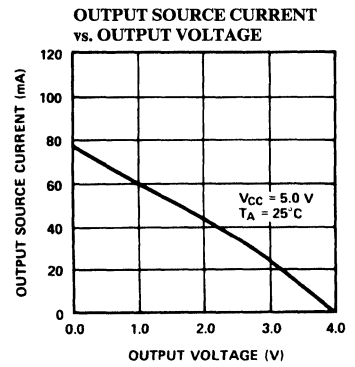
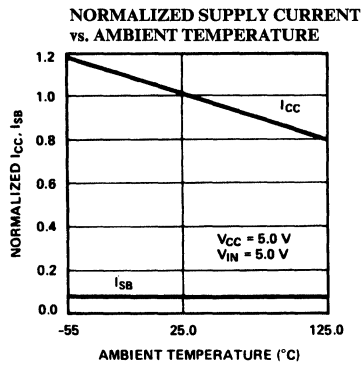
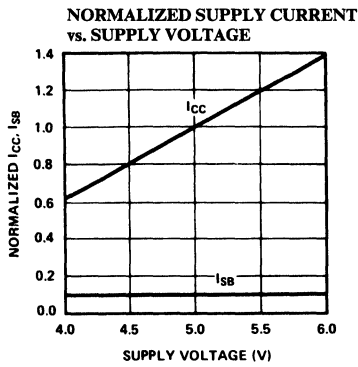


0164-10

Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

Typical DC and AC Characteristics

2



**Ordering Information**

| Speed (ns) | Ordering Code  | Package Type | Operating Range |
|------------|----------------|--------------|-----------------|
| 20         | CY7C128A-20PC  | P13          | Commercial      |
|            | CY7C128A-20VC  | V13          |                 |
|            | CY7C128A-20DC  | D14          |                 |
|            | CY7C128A-20LC  | L53          |                 |
| 25         | CY7C128A-25PC  | P13          | Commercial      |
|            | CY7C128A-25VC  | V13          |                 |
|            | CY7C128A-25DC  | D14          |                 |
|            | CY7C128A-25LC  | L53          |                 |
|            | CY7C128A-25DMB | D14          | Military        |
|            | CY7C128A-25LMB | L53          |                 |
| 35         | CY7C128A-35PC  | P13          | Commercial      |
|            | CY7C128A-35VC  | V13          |                 |
|            | CY7C128A-35DC  | D14          |                 |
|            | CY7C128A-35LC  | L53          |                 |
|            | CY7C128A-35DMB | D14          | Military        |
|            | CY7C128A-35LMB | L53          |                 |
|            | CY7C128A-35KMB | K73          |                 |
|            |                |              |                 |
| 45         | CY7C128A-45PC  | P13          | Commercial      |
|            | CY7C128A-45VC  | V13          |                 |
|            | CY7C128A-45DC  | D14          |                 |
|            | CY7C128A-45LC  | L53          |                 |
|            | CY7C128A-45DMB | D14          | Military        |
|            | CY7C128A-45LMB | L53          |                 |
|            | CY7C128A-45KMB | K73          |                 |
| 55         | CY7C128A-55PC  | P13          | Commercial      |
|            | CY7C128A-55VC  | V13          |                 |
|            | CY7C128A-55DC  | D14          |                 |
|            | CY7C128A-55LC  | L53          |                 |
|            | CY7C128A-55DMB | D14          | Military        |
|            | CY7C128A-55LMB | L53          |                 |
|            | CY7C128A-55KMB | K73          |                 |
|            |                |              |                 |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL</sub> Max. | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB</sub>      | 1,2,3     |

**2**
**Switching Characteristics**

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>ACE</sub>   | 7,8,9,10,11 |
| t <sub>DOE</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>SCE</sub>   | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |

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**Features**

- 0.8 micron CMOS for optimum speed/power
- Automatic power-down
- TTL compatible
- Capable of withstanding greater than 2001V electrostatic discharge
- Fully asynchronous operation
- Master CY7C130/CY7C131 easily expands data bus width to 16 or more bits using SLAVE CY7C140/CY7C141
- **BUSY** output flag on CY7C130/CY7C131; **BUSY** input on CY7C140/CY7C141
- **INT** flag for port to port communication

**Functional Description**

The CY7C130/CY7C140/CY7C131/CY7C141 are high speed CMOS 1K x 8 Dual Port Static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C130/CY7C131 can be utilized as either a stand-alone 8-bit Dual Port Static RAM or as a MASTER Dual Port RAM in conjunction with the CY7C140/CY7C141 SLAVE Dual Port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, Bit-Slice, or multiprocessor designs.

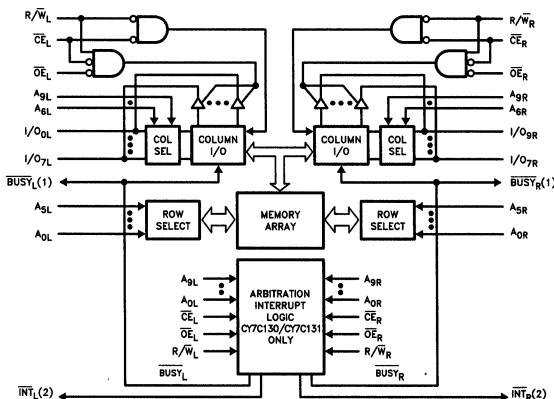
Each port has independent control pins; Chip Enable (CE), Write Enable

(WE), and Output Enable (OE). Two flags are provided on each port, **BUSY** and **INT**. **BUSY** signals that the port is trying to access the same location currently being accessed by the other port. **INT** is an interrupt flag indicating that data has been placed in a unique location by the other port. An automatic power-down feature is controlled independently on each port by the Chip Enable (CE) pin.

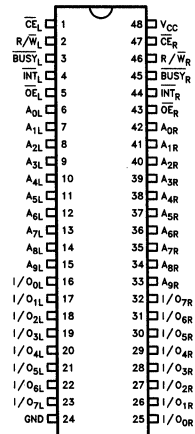
The CY7C130/CY7C140 are available in both 48-pin DIP and 48-pin LCC. The CY7C131/CY7C141 are available in both 52-pin LCC and PLCC.

A die coat is used to insure alpha immunity.

**Logic Block Diagram**



**Pin Configuration**



- Notes:
1. CY7C130/CY7C131 (Master): **BUSY** is open drain output and requires pullup resistor.  
CY7C140/CY7C141 (Slave): **BUSY** is input.
  2. Open drain outputs: pullup resistor required.

0114-1

0114-2

**DIP**  
**Top View**

**Selection Guide**

|                                |            | 7C130-25<br>7C131-25<br>7C140-25<br>7C141-25 | 7C130-35<br>7C131-35<br>7C140-35<br>7C141-35 | 7C130-45<br>7C131-45<br>7C140-45<br>7C141-45 | 7C130-55<br>7C131-55<br>7C140-55<br>7C141-55 |
|--------------------------------|------------|--|--|--|--|
| Maximum Access Time (ns)       |            | 25   | 35   | 45   | 55   |
| Maximum Operating Current (mA) | Commercial | 170  | 120  | 90   | 90   |
|                                | Military   |  | 170  | 120  | 120  |
| Maximum Standby Current (mA)   | Commercial | 65   | 45   | 35   | 35   |
|                                | Military   |  | 65   | 45   | 45   |

Shaded area contains preliminary information.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature .....                                   | -65°C to +150°C |
| Ambient Temperature with Power Applied .....                | -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State .....         | -0.5V to +7.0V  |
| DC Input Voltage .....                                      | -3.5V to +7.0V  |
| Output Current into Outputs (Low) .....                     | 20 mA           |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | > 2001V<br>(Per MIL-STD-883 Method 3015) |
| Latch-up Current .....         | > 200 mA                                 |

## Operating Range

| Range       | Ambient Temperature | V <sub>CC</sub> |
|-------------|---------------------|-----------------|
| Commercial  | 0°C to +70°C        | 5V ± 10%        |
| Military[6] | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over Operating Range[7]

| Parameters       | Description                                    | Test Conditions  | 7C130-25<br>7C131-25<br>7C140-25<br>7C141-25 |                     | 7C130-35<br>7C131-35<br>7C140-35<br>7C141-35      |      | 7C130-45, 55<br>7C131-45, 55<br>7C140-45, 55<br>7C141-45, 55 |      | Units |
|------------------|--|--|--|---------------------|---|------|--|------|-------|
|                  |  |  | Min.   | Max.                | Min.  | Max. | Min.   | Max. |       |
|                  |  |  | V <sub>OH</sub>                              | Output HIGH Voltage | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA | 2.4  |  | 2.4  |       |
| V <sub>OL</sub>  | Output LOW Voltage                             | I <sub>OL</sub> = 4.0 mA   |  | 0.4                 |   | 0.4  |  | 0.4  | V     |
|                  |  | I <sub>OL</sub> = 16.0 mA <sup>[5]</sup>   |  | 0.5                 |   | 0.5  |  | 0.5  |       |
| V <sub>IH</sub>  | Input HIGH Voltage                             |  | 2.2  |                     | 2.2   |      | 2.2  |      | V     |
| V <sub>IL</sub>  | Input LOW Voltage                              |  |  | 0.8                 |   | 0.8  |  | 0.8  | V     |
| I <sub>IX</sub>  | Input Load Current                             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -5   | +5                  | -5  | +5   | -5   | +5   | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                         | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub><br>Output Disabled  | -5   | +5                  | -5  | +5   | -5   | +5   | μA    |
| I <sub>OS</sub>  | Output Short <sup>[3]</sup><br>Circuit Current | V <sub>CC</sub> = Max.,<br>V <sub>OUT</sub> = GND  |  | -350                |   | -350 |  | -350 | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating<br>Supply Current    | CE = V <sub>IL</sub><br>Outputs Open<br>f = f <sub>MAX</sub>   | Commercial                                   | 170                 |   | 120  |  | 90   | mA    |
|                  |  |  | Military                                     |                     |   | 170  |  | 120  |       |
| I <sub>SB1</sub> | Standby Current<br>Both Ports, TTL Inputs      | CE <sub>L</sub> and CE <sub>R</sub> ≥ V <sub>IH</sub><br>f = f <sub>MAX</sub>  | Commercial                                   | 65                  |   | 45   |  | 35   | mA    |
|                  |  |  | Military                                     |                     |   | 65   |  | 45   |       |
| I <sub>SB2</sub> | Standby Current<br>One Port, TTL Inputs        | CE <sub>L</sub> or CE <sub>R</sub> ≥ V <sub>IH</sub><br>Active Port Outputs Open<br>f = f <sub>MAX</sub>   | Commercial                                   | 115                 |   | 90   |  | 75   | mA    |
|                  |  |  | Military                                     |                     |   | 115  |  | 90   |       |
| I <sub>SB3</sub> | Standby Current<br>Both Ports, CMOS Inputs     | Both Ports CE <sub>L</sub> and CE <sub>R</sub><br>≥ V <sub>CC</sub> - 0.2V<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or<br>V <sub>IN</sub> ≤ 0.2V, f = 0   | Commercial                                   | 15                  |   | 15   |  | 15   | mA    |
|                  |  |  | Military                                     |                     |   | 15   |  | 15   |       |
| I <sub>SB4</sub> | Standby Current<br>One Port, CMOS Inputs       | One Port CE <sub>L</sub> or CE <sub>R</sub><br>≥ V <sub>CC</sub> - 0.2V<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V<br>Active Ports Outputs Open<br>f = f <sub>MAX</sub> | Commercial                                   | 105                 |   | 85   |  | 70   | mA    |
|                  |  |  | Military                                     |                     |   | 105  |  | 85   |       |

Shaded area contains preliminary information.

## Capacitance[4]

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 10   | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 10   |       |

### Notes:

- Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- BUSY and INT pins only.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.



## AC Test Loads and Waveforms

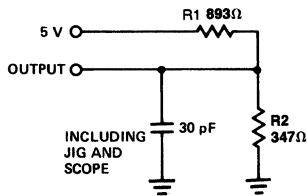


Figure 1

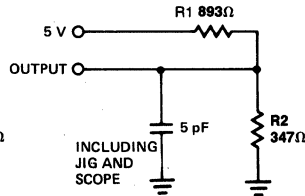


Figure 2

0114-5

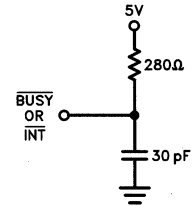


Figure 3. BUSY Output Load  
(CY7C130/CY7C131 Only)

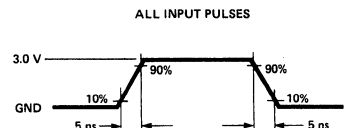
0114-4

Equivalent to:

THÉVENIN EQUIVALENT



0114-7



0114-6

Figure 4

## Switching Characteristics Over Operating Range<sup>[7, 9]</sup>

| Parameters                        | Description  | 7C130-25 |      | 7C130-35 |      | 7C130-45 |      | 7C130-55 |      | Units |  |
|-----------------------------------|--|----------|------|----------|------|----------|------|----------|------|-------|--|
|                                   |  | 7C131-25 |      | 7C131-35 |      | 7C131-45 |      | 7C131-55 |      |       |  |
|                                   |  | 7C140-25 |      | 7C140-35 |      | 7C140-45 |      | 7C140-55 |      |       |  |
|                                   |  | 7C141-25 |      | 7C141-35 |      | 7C141-45 |      | 7C141-55 |      |       |  |
|                                   |  | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.     | Max. |       |  |
| <b>READ CYCLE</b>                 |  |          |      |          |      |          |      |          |      |       |  |
| t <sub>RC</sub>                   | Read Cycle Time                                    | 25       |      | 35       |      | 45       |      | 55       |      | ns    |  |
| t <sub>AA</sub>                   | Address to Data Valid                              |          | 25   |          | 35   |          | 45   |          | 55   | ns    |  |
| t <sub>OHA</sub>                  | Data Hold from Address Change                      | 0        |      | 0        |      | 0        |      | 0        |      | ns    |  |
| t <sub>ACE</sub>                  | $\overline{CE}$ LOW to Data Valid                  |          | 30   |          | 35   |          | 45   |          | 55   | ns    |  |
| t <sub>DOE</sub>                  | $\overline{OE}$ LOW to Data Valid                  |          | 15   |          | 20   |          | 25   |          | 25   | ns    |  |
| t <sub>LZOE</sub>                 | $\overline{OE}$ LOW to Low Z                       | 3        |      | 3        |      | 3        |      | 3        |      | ns    |  |
| t <sub>HZOE</sub>                 | $\overline{OE}$ HIGH to High Z <sup>[10]</sup>     |          | 15   |          | 20   |          | 20   |          | 25   | ns    |  |
| t <sub>LZCE</sub>                 | $\overline{CE}$ LOW to Low Z <sup>[11]</sup>       | 5        |      | 5        |      | 5        |      | 5        |      | ns    |  |
| t <sub>HZCE</sub>                 | $\overline{CE}$ HIGH to High Z <sup>[10, 11]</sup> |          | 15   |          | 20   |          | 20   |          | 25   | ns    |  |
| t <sub>PU</sub>                   | $\overline{CE}$ LOW to Power Up                    | 0        |      | 0        |      | 0        |      | 0        |      | ns    |  |
| t <sub>PD</sub>                   | $\overline{CE}$ HIGH to Power Down                 |          | 25   |          | 35   |          | 35   |          | 35   | ns    |  |
| <b>WRITE CYCLE<sup>[12]</sup></b> |  |          |      |          |      |          |      |          |      |       |  |
| t <sub>WC</sub>                   | Write Cycle Time                                   | 25       |      | 35       |      | 45       |      | 55       |      | ns    |  |
| t <sub>SCE</sub>                  | $\overline{CE}$ LOW to Write End                   | 20       |      | 30       |      | 35       |      | 40       |      | ns    |  |
| t <sub>AW</sub>                   | Address Set-up to Write End                        | 20       |      | 30       |      | 35       |      | 40       |      | ns    |  |
| t <sub>HA</sub>                   | Address Hold from Write End                        | 2        |      | 2        |      | 2        |      | 2        |      | ns    |  |
| t <sub>SA</sub>                   | Address Set-up to Write Start                      | 0        |      | 0        |      | 0        |      | 0        |      | ns    |  |
| t <sub>PWE</sub>                  | $\overline{WE}$ Pulse Width                        | 20       |      | 25       |      | 30       |      | 30       |      | ns    |  |
| t <sub>SD</sub>                   | Data Set-up to Write End                           | 15       |      | 15       |      | 20       |      | 20       |      | ns    |  |
| t <sub>HD</sub>                   | Data Hold from Write End                           | 0        |      | 0        |      | 0        |      | 0        |      | ns    |  |
| t <sub>HZWE</sub>                 | $\overline{WE}$ LOW to High Z                      |          | 15   |          | 20   |          | 20   |          | 25   | ns    |  |
| t <sub>LZWE</sub>                 | $\overline{WE}$ HIGH to Low Z                      | 0        |      | 0        |      | 0        |      | 0        |      | ns    |  |

Shaded area contains preliminary information.

Switching Characteristics Over Operating Range<sup>[7, 9]</sup> (Continued)

| Parameters                   | Description                                     | 7C130-25 |         | 7C130-35 |         | 7C130-45 |         | 7C130-55 |         | Units |  |
|------------------------------|---|----------|---------|----------|---------|----------|---------|----------|---------|-------|--|
|                              |   | 7C131-25 |         | 7C131-35 |         | 7C131-45 |         | 7C131-55 |         |       |  |
|                              |   | 7C140-25 |         | 7C140-35 |         | 7C140-45 |         | 7C140-55 |         |       |  |
|                              |   | 7C141-25 |         | 7C141-35 |         | 7C141-45 |         | 7C141-55 |         |       |  |
|                              |   | Min.     | Max.    | Min.     | Max.    | Min.     | Max.    | Min.     | Max.    |       |  |
| <b>BUSY/INTERRUPT TIMING</b> |   |          |         |          |         |          |         |          |         |       |  |
| tBLA                         | BUSY LOW from Address Match                     |          | 20      |          | 20      |          | 25      |          | 30      | ns    |  |
| tBHA                         | BUSY HIGH from Address Mismatch <sup>[17]</sup> |          | 20      |          | 20      |          | 25      |          | 30      | ns    |  |
| tBLC                         | BUSY LOW from CE LOW                            |          | 20      |          | 20      |          | 25      |          | 30      | ns    |  |
| tBHC                         | BUSY HIGH from CE HIGH <sup>[17]</sup>          |          | 20      |          | 20      |          | 25      |          | 30      | ns    |  |
| tps                          | Port Set Up for Priority                        | 5        |         | 5        |         | 5        |         | 5        |         | ns    |  |
| tWB*                         | WE LOW after BUSY LOW                           | 0        |         | 0        |         | 0        |         | 0        |         | ns    |  |
| tWH                          | WE HIGH after BUSY HIGH                         | 20       |         | 30       |         | 35       |         | 35       |         | ns    |  |
| tBDD                         | BUSY HIGH to Valid Data                         |          | 25      |          | 35      |          | 45      |          | 45      | ns    |  |
| tDDD                         | Write Data Valid to Read Data Valid             |          | Note 16 |          | Note 16 |          | Note 16 |          | Note 16 | ns    |  |
| tWDD                         | Write Pulse to Data Delay                       |          | Note 16 |          | Note 16 |          | Note 16 |          | Note 16 | ns    |  |
| <b>INTERRUPT TIMING</b>      |   |          |         |          |         |          |         |          |         |       |  |
| tWINS                        | WE to INTERRUPT Set Time                        |          | 25      |          | 25      |          | 35      |          | 45      | ns    |  |
| tEINS                        | CE to INTERRUPT Set Time                        |          | 25      |          | 25      |          | 35      |          | 45      | ns    |  |
| tINS                         | Address to INTERRUPT Set Time                   |          | 25      |          | 25      |          | 35      |          | 45      | ns    |  |
| tOINR                        | OE to INTERRUPT Reset Time <sup>[17]</sup>      |          | 25      |          | 25      |          | 35      |          | 45      | ns    |  |
| tEINR                        | CE to INTERRUPT Reset Time <sup>[17]</sup>      |          | 25      |          | 25      |          | 35      |          | 45      | ns    |  |
| tINR                         | Address to INTERRUPT Reset Time <sup>[17]</sup> |          | 25      |          | 25      |          | 35      |          | 45      | ns    |  |

Shaded area contains preliminary information.

\* CY7C140/CY7C141 Only

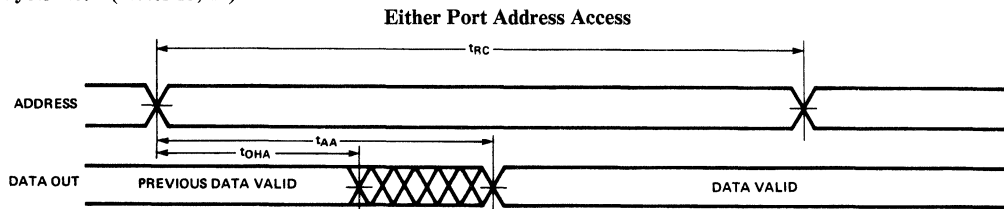
Notes:

- Data I/O pins enter high impedance state, as shown when OE is held LOW during write.
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF in Figure 2. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

- WE is HIGH for read cycle.
- Device is continuously selected OE, CE = V<sub>IL</sub>.
- Address valid prior to or coincident with CE transition LOW.
- A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
  - BUSY on Port B goes HIGH.
  - Port B's address toggled.
  - CE for Port B is toggled.
  - WE for Port B is toggled.
- These parameters are measured from the input signal changing, until the output pin goes to a high impedance state.
- For master/slave combinations t<sub>WC</sub> = t<sub>PWE</sub> + t<sub>BLA</sub>.

Switching Waveforms

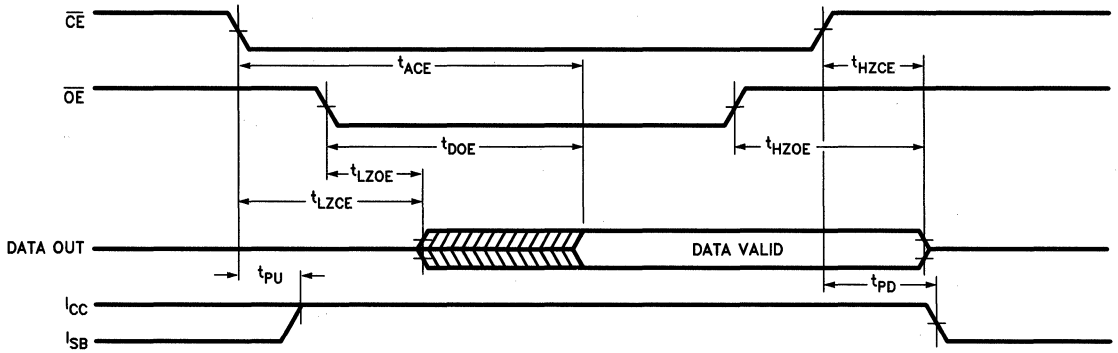
Read Cycle No. 1 (Notes 13, 14)



Switching Waveforms (Continued)

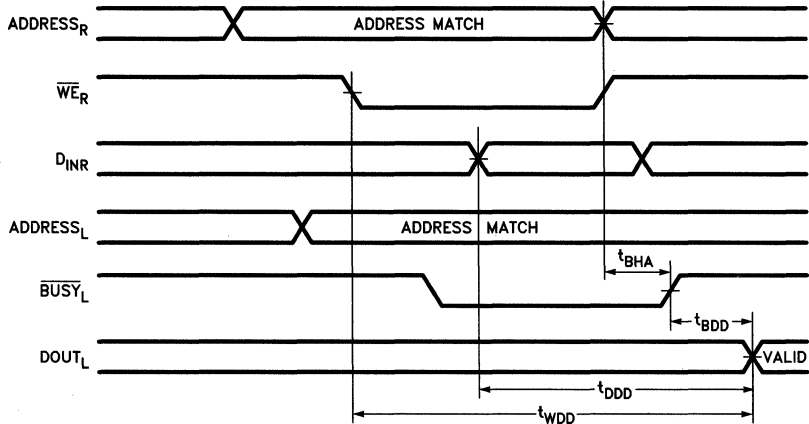
Read Cycle No. 2 (Notes 13, 15)

Either Port  $\overline{CE}/\overline{OE}$  Access



0114-9

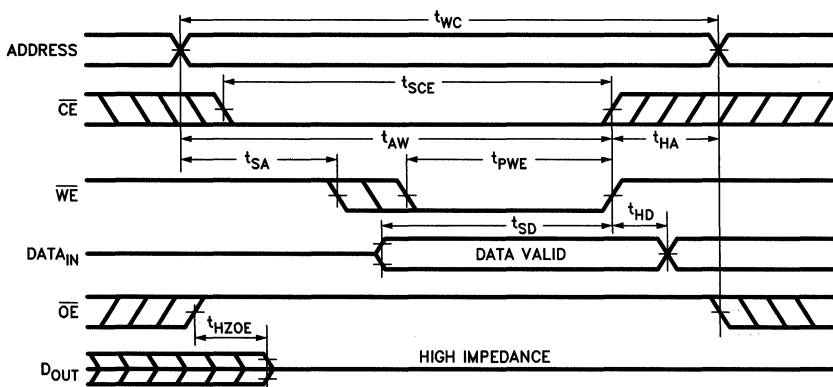
Timing Waveform of Read with  $\overline{BUSY}$  (Note 13)



0114-10

Write Cycle No. 1 (Notes 8, 12)

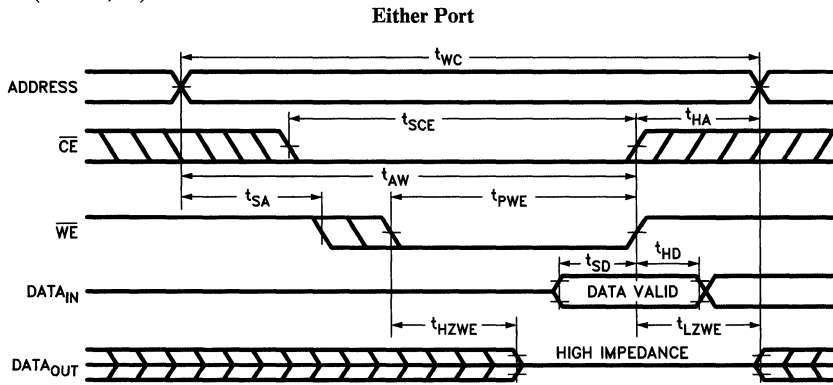
Either Port



0114-12

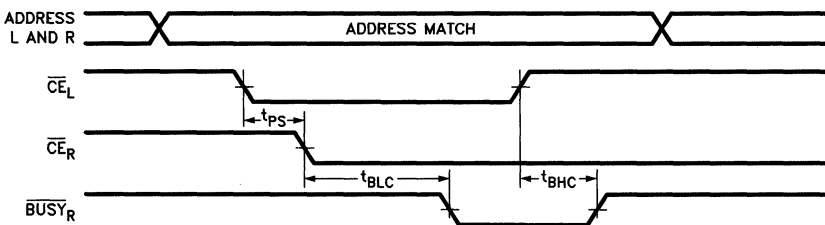
Switching Waveforms (Continued)

Write Cycle No. 2 (Notes 8, 12)

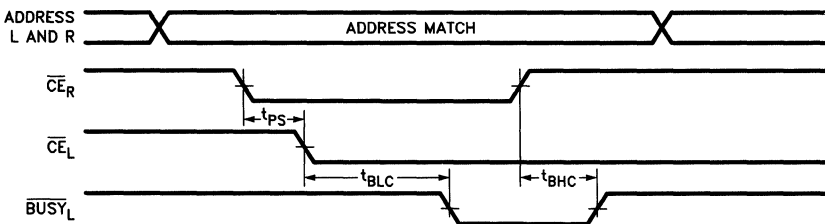


Busy Timing Diagram No. 1 ( $\overline{CE}$  Arbitration)

$\overline{CE}_L$  Valid First:



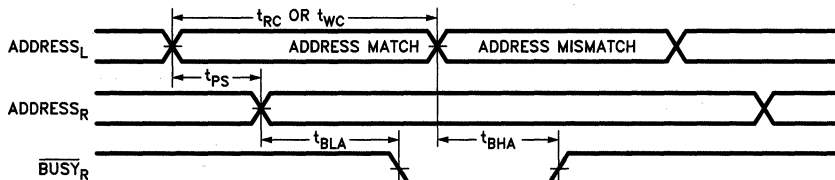
$\overline{CE}_R$  Valid First:



## Switching Waveforms (Continued)

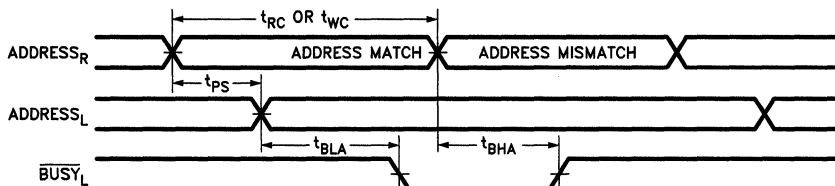
### Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:



0114-16

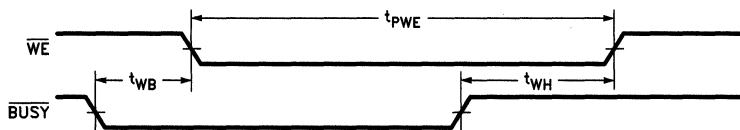
Right Address Valid First:



0114-17

### Busy Timing Diagram No. 3

Write with  $\overline{BUSY}$  (Slave: CY7C140/CY7C141) (Note 19):

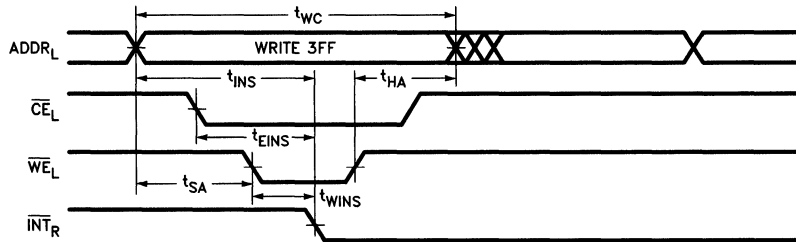


0114-11

## Switching Waveforms (Continued)

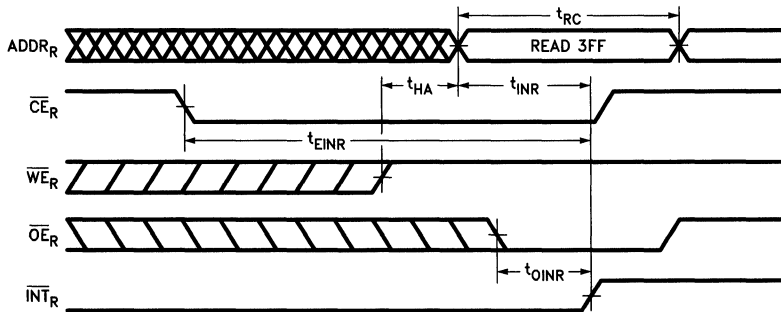
### Interrupt Timing Diagrams

#### Left Side Sets $\overline{INT}_R$ :



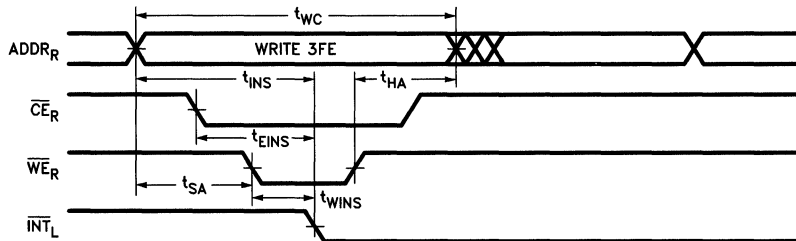
0114-18

#### Right Side Clears $\overline{INT}_R$ :



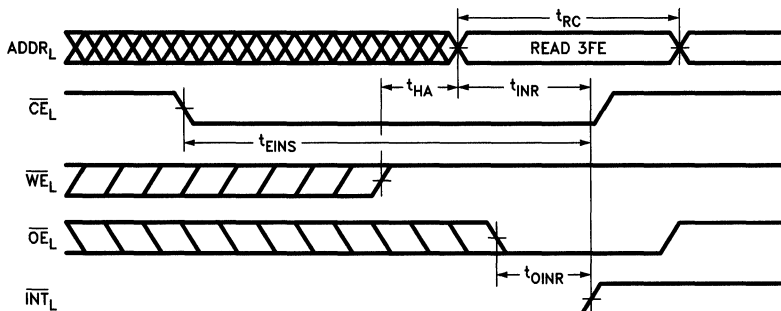
0114-19

#### Right Side Sets $\overline{INT}_L$ :



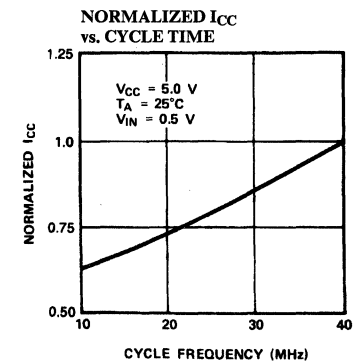
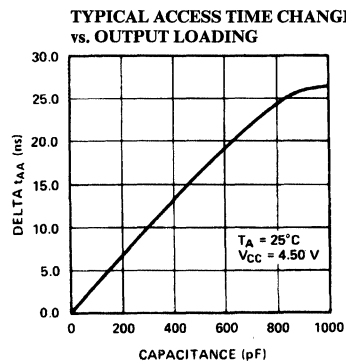
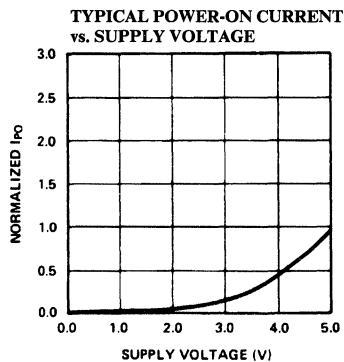
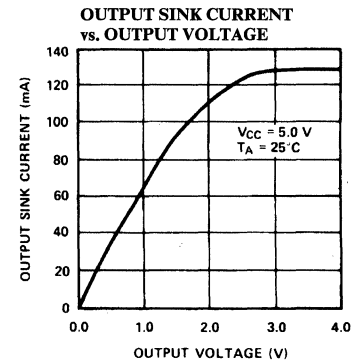
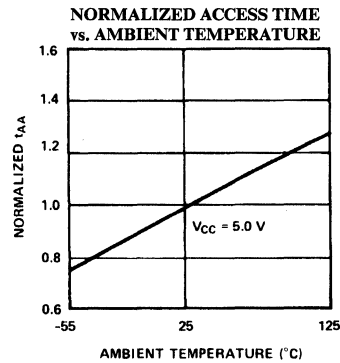
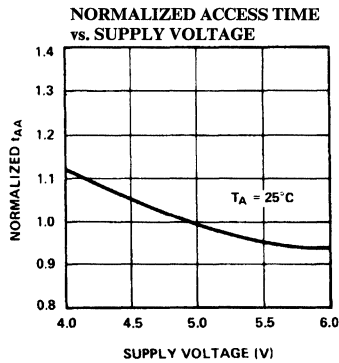
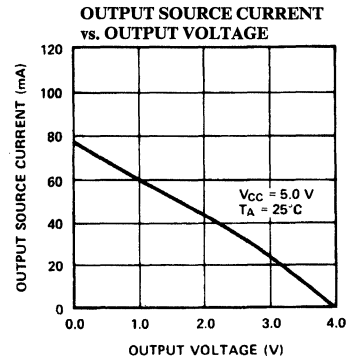
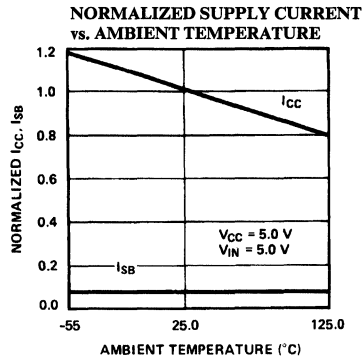
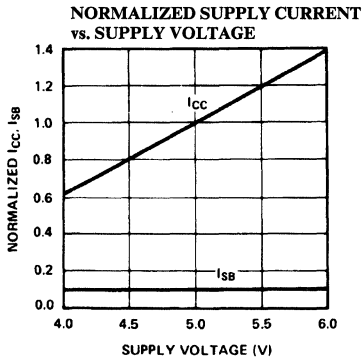
0114-20

#### Left Side Clears $\overline{INT}_L$ :

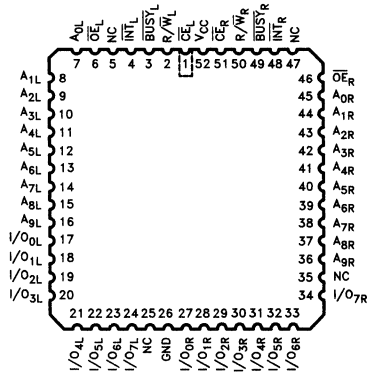


0114-21

## Typical DC and AC Characteristics

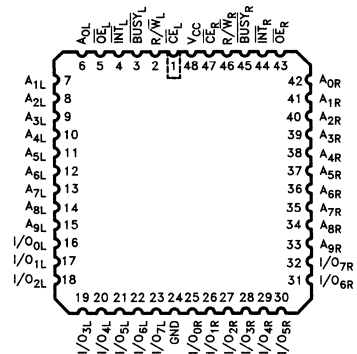


## Pin Configurations



52-Pin LCC/PLCC  
Top View

0114-3



48-Pin LCC  
Top View

0114-22

## Ordering Information

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C130-25PC  | P25          | Commercial      |
|            | CY7C130-25DC  | D26          |                 |
|            | CY7C130-25LC  | L68          |                 |
| 35         | CY7C130-35PC  | P25          | Commercial      |
|            | CY7C130-35DC  | D26          |                 |
|            | CY7C130-35LC  | L68          |                 |
|            | CY7C130-35DMB | D26          | Military        |
|            | CY7C130-35LMB | L68          |                 |
| 45         | CY7C130-45PC  | P25          | Commercial      |
|            | CY7C130-45DC  | D26          |                 |
|            | CY7C130-45LC  | L68          |                 |
|            | CY7C130-45DMB | D26          | Military        |
|            | CY7C130-45LMB | L68          |                 |
| 55         | CY7C130-55PC  | P25          | Commercial      |
|            | CY7C130-55DC  | D26          |                 |
|            | CY7C130-55LC  | L68          |                 |
|            | CY7C130-55DMB | D26          | Military        |
|            | CY7C130-55LMB | L68          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C140-25PC  | P25          | Commercial      |
|            | CY7C140-25DC  | D26          |                 |
|            | CY7C140-25LC  | L68          |                 |
| 35         | CY7C140-35PC  | P25          | Commercial      |
|            | CY7C140-35DC  | D26          |                 |
|            | CY7C140-35LC  | L68          |                 |
|            | CY7C140-35DMB | D26          | Military        |
|            | CY7C140-35LMB | L68          |                 |
| 45         | CY7C140-45PC  | P25          | Commercial      |
|            | CY7C140-45DC  | D26          |                 |
|            | CY7C140-45LC  | L68          |                 |
|            | CY7C140-45DMB | D26          | Military        |
|            | CY7C140-45LMB | L68          |                 |
| 55         | CY7C140-55PC  | P25          | Commercial      |
|            | CY7C140-55DC  | D26          |                 |
|            | CY7C140-55LC  | L68          |                 |
|            | CY7C140-55DMB | D26          | Military        |
|            | CY7C140-55LMB | L68          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C131-25LC  | L69          | Commercial      |
|            | CY7C131-25JC  | J69          |                 |
| 35         | CY7C131-35LC  | L69          | Commercial      |
|            | CY7C131-35JC  | J69          |                 |
|            | CY7C131-35LMB | L69          | Military        |
| 45         | CY7C131-45LC  | L69          | Commercial      |
|            | CY7C131-45JC  | J69          |                 |
|            | CY7C131-45LMB | L69          | Military        |
| 55         | CY7C131-55LC  | L69          | Commercial      |
|            | CY7C131-55JC  | J69          |                 |
|            | CY7C131-55LMB | L69          | Military        |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C141-25LC  | L69          | Commercial      |
|            | CY7C141-25JC  | J69          |                 |
| 35         | CY7C141-35LC  | L69          | Commercial      |
|            | CY7C141-35JC  | J69          |                 |
|            | CY7C141-35LMB | L69          | Military        |
| 45         | CY7C141-45LC  | L69          | Commercial      |
|            | CY7C141-45JC  | J69          |                 |
|            | CY7C141-45LMB | L69          | Military        |
| 55         | CY7C141-55LC  | L69          | Commercial      |
|            | CY7C141-55JC  | J69          |                 |
|            | CY7C141-55LMB | L69          | Military        |

Shaded area contains preliminary information.



**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>OS</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB1</sub>     | 1,2,3     |
| I <sub>SB2</sub>     | 1,2,3     |
| I <sub>SB3</sub>     | 1,2,3     |

| Parameters       | Subgroups |
|------------------|-----------|
| I <sub>SB4</sub> | 1,2,3     |

**Switching Characteristics**

| Parameters                   | Subgroups   |
|------------------------------|-------------|
| <b>READ CYCLE</b>            |             |
| t <sub>AA</sub>              | 7,8,9,10,11 |
| t <sub>OHA</sub>             | 7,8,9,10,11 |
| t <sub>ACE</sub>             | 7,8,9,10,11 |
| t <sub>DOE</sub>             | 7,8,9,10,11 |
| <b>WRITE CYCLE</b>           |             |
| t <sub>SCE</sub>             | 7,8,9,10,11 |
| t <sub>AW</sub>              | 7,8,9,10,11 |
| t <sub>HA</sub>              | 7,8,9,10,11 |
| t <sub>SA</sub>              | 7,8,9,10,11 |
| t <sub>PWE</sub>             | 7,8,9,10,11 |
| t <sub>SD</sub>              | 7,8,9,10,11 |
| t <sub>HD</sub>              | 7,8,9,10,11 |
| <b>BUSY/INTERRUPT TIMING</b> |             |
| t <sub>BLA</sub>             | 7,8,9,10,11 |
| t <sub>BHA</sub>             | 7,8,9,10,11 |
| t <sub>BLC</sub>             | 7,8,9,10,11 |
| t <sub>BHC</sub>             | 7,8,9,10,11 |
| t <sub>PS</sub>              | 7,8,9,10,11 |
| t <sub>WINS</sub>            | 7,8,9,10,11 |
| t <sub>EINS</sub>            | 7,8,9,10,11 |
| t <sub>INS</sub>             | 7,8,9,10,11 |

| Parameters                               | Subgroups   |
|--|-------------|
| <b>BUSY/INTERRUPT TIMING (Continued)</b> |             |
| t <sub>OINR</sub>                        | 7,8,9,10,11 |
| t <sub>EINR</sub>                        | 7,8,9,10,11 |
| t <sub>INR</sub>                         | 7,8,9,10,11 |
| <b>BUSY TIMING</b>                       |             |
| t <sub>WB</sub> <sup>[1]</sup>           | 7,8,9,10,11 |
| t <sub>WH</sub>                          | 7,8,9,10,11 |
| t <sub>BDD</sub>                         | 7,8,9,10,11 |
| t <sub>DDD</sub>                         | 7,8,9,10,11 |
| t <sub>WDD</sub>                         | 7,8,9,10,11 |

**Note:**

1. CY7C140 only.

Document #: 38-00027-D



**Features**

- 0.8 micron CMOS for optimum speed/power
- Automatic power-down
- TTL compatible
- Capable of withstanding greater than 2001V electrostatic discharge
- Fully asynchronous operation
- MASTER CY7C132/CY7C136 easily expands databus width to 16 or more bits using SLAVE CY7C142/CY7C146
- **BUSY** output flag on CY7C132/CY7C136; **BUSY** input on CY7C142/CY7C146
- **INT** flag for port to port communication (LCC/PLCC versions)

**Functional Description**

The CY7C132/CY7C142/CY7C136/CY7C146 are high speed CMOS 2K x 8 Dual Port Static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C132/CY7C136 can be utilized as either a stand-alone 8-Bit Dual Port RAM or as a MASTER Dual Port RAM in conjunction with the CY7C142/CY7C146 SLAVE Dual Port device in systems requiring 16-Bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, bit-slice or multiprocessor designs.

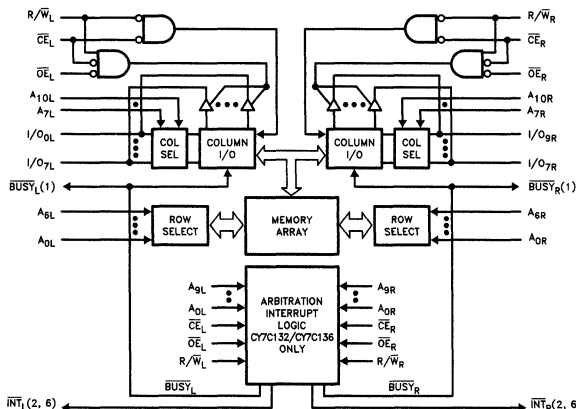
Each port has independent control pins; Chip Enable (CE), Write Enable (WE), and Output Enable (OE). **BUSY**

flags are provided on each port. In addition, an interrupt flag (INT) is provided on each port of the 52-pin LCC or PLCC versions. **BUSY** signals that the port is trying to access the same location currently being accessed by the other port. On the LCC/PLCC versions, **INT** is an interrupt flag indicating that data has been placed in a unique location by the other port.

An automatic power-down feature is controlled independently on each port by the Chip Enable (CE) pin.

The CY7C132/CY7C142 are available in both 48-pin DIP and 48-pin LCC. The CY7C136/CY7C146 are available in both 52-pin LCC and 52-pin PLCC. A die coat is used to insure alpha immunity.

**Logic Block Diagram**

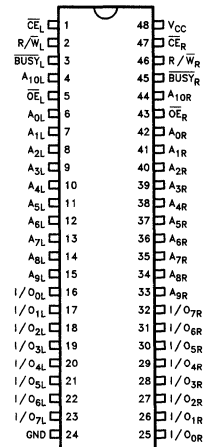


**Notes:**

1. CY7C132/CY7C136 (MASTER): **BUSY** is open drain output and requires pullup resistor. CY7C142/CY7C146 (SLAVE): **BUSY** is input.
2. Open drain outputs: pullup resistor required.

0106-1

**Pin Configuration**



DIP  
Top View

0106-2

**Selection Guide**

|                                |            | 7C132-25<br>7C136-25<br>7C142-25<br>7C146-25 | 7C132-35<br>7C136-35<br>7C142-35<br>7C146-35 | 7C132-45<br>7C136-45<br>7C142-45<br>7C146-45 | 7C132-55<br>7C136-55<br>7C142-55<br>7C146-55 |
|--------------------------------|------------|--|--|--|--|
| Maximum Access Time (ns)       |            | 25   | 35   | 45   | 55   |
| Maximum Operating Current (mA) | Commercial | 170  | 120  | 90   | 90   |
|                                | Military   |  | 170  | 120  | 120  |
| Maximum Standby Current (mA)   | Commercial | 65   | 45   | 35   | 35   |
|                                | Military   |  | 65   | 45   | 45   |

Shaded area contains preliminary information.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature .....                                   | -65°C to +150°C |
| Ambient Temperature with Power Applied .....                | -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State .....         | -0.5V to +7.0V  |
| DC Input Voltage .....                                      | -3.5V to +7.0V  |
| Output Current into Outputs (Low) .....                     | 20 mA           |

|                                |                                       |
|--------------------------------|---------------------------------------|
| Static Discharge Voltage ..... | > 2001V (per MIL-STD-883 Method 3015) |
| Latch-up Current .....         | > 200 mA                              |

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[7]</sup> | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over Operating Range<sup>[8]</sup>

| Parameters       | Description                              | Test Conditions  | 7C132-25<br>7C136-25<br>7C142-25<br>7C146-25 |      | 7C132-35<br>7C136-35<br>7C142-35<br>7C146-35 |      | 7C132-45, 55<br>7C136-45, 55<br>7C142-45, 55<br>7C146-45, 55 |      | Units |    |
|------------------|--|--|--|------|--|------|--|------|-------|----|
|                  |  |  | Min.   | Max. | Min.   | Max. | Min.   | Max. |       |    |
| V <sub>OH</sub>  | Output HIGH Voltage                      | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA  | 2.4  |      | 2.4  |      | 2.4  |      | V     |    |
| V <sub>OL</sub>  | Output LOW Voltage                       | I <sub>OL</sub> = 4.0 mA   |  | 0.4  |  | 0.4  |  | 0.4  | V     |    |
|                  |  | I <sub>OL</sub> = 16.0 mA <sup>[6]</sup>   |  | 0.5  |  | 0.5  |  | 0.5  |       |    |
| V <sub>IH</sub>  | Input HIGH Voltage                       |  | 2.2  |      | 2.2  |      | 2.2  |      | V     |    |
| V <sub>IL</sub>  | Input LOW Voltage                        |  |  | 0.8  |  | 0.8  |  | 0.8  | V     |    |
| I <sub>IX</sub>  | Input Load Current                       | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -5   | +5   | -5   | +5   | -5   | +5   | μA    |    |
| I <sub>OZ</sub>  | Output Leakage Current                   | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub><br>Output Disabled  | -5   | +5   | -5   | +5   | -5   | +5   | μA    |    |
| I <sub>OS</sub>  | Output Short [3] Circuit Current         | V <sub>CC</sub> = Max.,<br>V <sub>OUT</sub> = GND  |  | -350 |  | -350 |  | -350 | mA    |    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current | CE̅ = V <sub>IL</sub><br>Outputs Open<br>f = f <sub>MAX</sub>  | Commercial                                   |      | 170  |      | 120  |      | 90    | mA |
|                  |  |  | Military                                     |      |  |      | 170  |      | 120   |    |
| I <sub>SB1</sub> | Standby Current Both Ports, TTL Inputs   | CE̅ <sub>L</sub> and CE̅ <sub>R</sub> ≥ V <sub>IH</sub><br>f = f <sub>MAX</sub>  | Commercial                                   |      | 65   |      | 45   |      | 35    | mA |
|                  |  |  | Military                                     |      |  |      | 65   |      | 45    |    |
| I <sub>SB2</sub> | Standby Current One Port, TTL Inputs     | CE̅ <sub>L</sub> or CE̅ <sub>R</sub> ≥ V <sub>IH</sub><br>Active Port Outputs Open<br>f = f <sub>MAX</sub>   | Commercial                                   |      | 115  |      | 90   |      | 75    | mA |
|                  |  |  | Military                                     |      |  |      | 115  |      | 90    |    |
| I <sub>SB3</sub> | Standby Current Both Ports, CMOS Inputs  | Both Ports CE̅ <sub>L</sub> and CE̅ <sub>R</sub> ≥ V <sub>CC</sub> - 0.2V<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or<br>V <sub>IN</sub> ≤ 0.2V, f = 0  | Commercial                                   |      | 15   |      | 15   |      | 15    | mA |
|                  |  |  | Military                                     |      |  |      | 15   |      | 15    |    |
| I <sub>SB4</sub> | Standby Current One Port, CMOS Inputs    | One Port CE̅ <sub>L</sub> or CE̅ <sub>R</sub> ≥ V <sub>CC</sub> - 0.2V<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or<br>V <sub>IN</sub> ≤ 0.2V<br>Active Ports Outputs Open<br>f = f <sub>MAX</sub> | Commercial                                   |      | 105  |      | 85   |      | 70    | mA |
|                  |  |  | Military                                     |      |  |      | 105  |      | 85    |    |

Shaded area contains preliminary information.

## Capacitance<sup>[4]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 10   | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 10   |       |

### Notes:

- Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- LCC version only.
- BUSY and INT pins only.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

## AC Test Loads and Waveforms

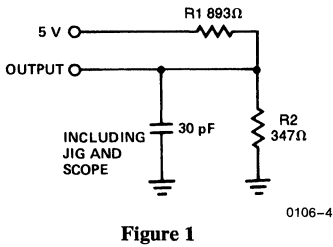


Figure 1

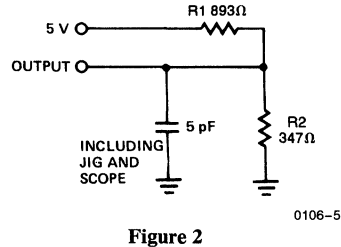


Figure 2

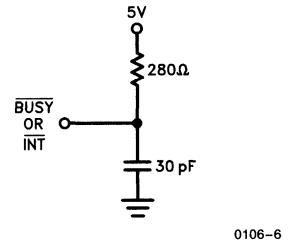
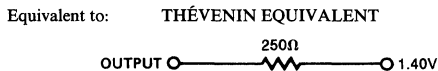


Figure 3.  $\overline{\text{BUSY}}$  OR INT Output Load (CY7C132/CY7C136 Only)



0106-8

ALL INPUT PULSES

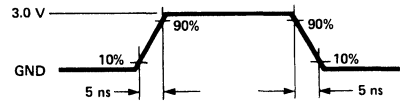


Figure 4

## Switching Characteristics Over Operating Range [8, 10]

| Parameters                        | Description   | 7C132-25<br>7C136-25<br>7C142-25<br>7C146-25 |      | 7C132-35<br>7C136-35<br>7C142-35<br>7C146-35 |      | 7C132-45<br>7C136-45<br>7C142-45<br>7C146-45 |      | 7C132-55<br>7C136-55<br>7C142-55<br>7C146-55 |      | Units |
|-----------------------------------|---|--|------|--|------|--|------|--|------|-------|
|                                   |   | Min.   | Max. | Min.   | Max. | Min.   | Max. | Min.   | Max. |       |
| <b>READ CYCLE</b>                 |   |  |      |  |      |  |      |  |      |       |
| t <sub>RC</sub>                   | Read Cycle Time   | 25   |      | 35   |      | 45   |      | 55   |      | ns    |
| t <sub>AA</sub>                   | Address to Data Valid                                     |  | 25   |  | 35   |  | 45   |  | 55   | ns    |
| t <sub>OHA</sub>                  | Data Hold from Address Change                             | 0  |      | 0  |      | 0  |      | 0  |      | ns    |
| t <sub>ACE</sub>                  | $\overline{\text{CE}}$ LOW to Data Valid                  |  | 30   |  | 35   |  | 45   |  | 55   | ns    |
| t <sub>DOE</sub>                  | $\overline{\text{OE}}$ LOW to Data Valid                  |  | 15   |  | 20   |  | 25   |  | 25   | ns    |
| t <sub>LZOE</sub>                 | $\overline{\text{OE}}$ LOW to Low Z                       | 3  |      | 3  |      | 3  |      | 3  |      | ns    |
| t <sub>HZOE</sub>                 | $\overline{\text{OE}}$ HIGH to High Z <sup>[11]</sup>     |  | 15   |  | 20   |  | 20   |  | 25   | ns    |
| t <sub>LZCE</sub>                 | $\overline{\text{CE}}$ LOW to Low Z <sup>[12]</sup>       | 5  |      | 5  |      | 5  |      | 5  |      | ns    |
| t <sub>HZCE</sub>                 | $\overline{\text{CE}}$ HIGH to High Z <sup>[11, 12]</sup> |  | 15   |  | 20   |  | 20   |  | 25   | ns    |
| t <sub>PU</sub>                   | $\overline{\text{CE}}$ LOW to Power Up                    | 0  |      | 0  |      | 0  |      | 0  |      | ns    |
| t <sub>PD</sub>                   | $\overline{\text{CE}}$ HIGH to Power Down                 |  | 25   |  | 35   |  | 35   |  | 35   | ns    |
| <b>WRITE CYCLE<sup>[13]</sup></b> |   |  |      |  |      |  |      |  |      |       |
| t <sub>WC</sub>                   | Write Cycle Time  | 25   |      | 35   |      | 45   |      | 55   |      | ns    |
| t <sub>SCE</sub>                  | $\overline{\text{CE}}$ LOW to Write End                   | 20   |      | 30   |      | 35   |      | 40   |      | ns    |
| t <sub>AW</sub>                   | Address Set-Up to Write End                               | 20   |      | 30   |      | 35   |      | 40   |      | ns    |
| t <sub>HA</sub>                   | Address Hold from Write End                               | 2  |      | 2  |      | 2  |      | 2  |      | ns    |
| t <sub>SA</sub>                   | Address Set-Up to Write Start                             | 0  |      | 0  |      | 0  |      | 0  |      | ns    |
| t <sub>PWE</sub>                  | $\overline{\text{WE}}$ Pulse Width                        | 20   |      | 25   |      | 30   |      | 30   |      | ns    |
| t <sub>SD</sub>                   | Data Set-Up to Write End                                  | 15   |      | 15   |      | 20   |      | 20   |      | ns    |
| t <sub>HD</sub>                   | Data Hold from Write End                                  | 0  |      | 0  |      | 0  |      | 0  |      | ns    |
| t <sub>HZWE</sub>                 | $\overline{\text{WE}}$ LOW to High Z                      |  | 15   |  | 20   |  | 20   |  | 25   | ns    |
| t <sub>LZWE</sub>                 | $\overline{\text{WE}}$ HIGH to Low Z                      | 0  |      | 0  |      | 0  |      | 0  |      | ns    |

Shaded area contains preliminary information.

Switching Characteristics Over Operating Range [8, 10] (Continued)

| Parameters              | Description                                     | 7C132-25 |         | 7C132-35 |         | 7C132-45 |         | 7C132-55 |         | Units |  |
|-------------------------|---|----------|---------|----------|---------|----------|---------|----------|---------|-------|--|
|                         |   | 7C136-25 |         | 7C136-35 |         | 7C136-45 |         | 7C136-55 |         |       |  |
|                         |   | 7C142-25 |         | 7C142-35 |         | 7C142-45 |         | 7C142-55 |         |       |  |
|                         |   | 7C146-25 |         | 7C146-35 |         | 7C146-45 |         | 7C146-55 |         |       |  |
|                         |   | Min.     | Max.    | Min.     | Max.    | Min.     | Max.    | Min.     | Max.    |       |  |
| <b>BUSY TIMING</b>      |   |          |         |          |         |          |         |          |         |       |  |
| tBLA                    | BUSY LOW from Address Match                     |          | 20      |          | 20      |          | 25      |          | 30      | ns    |  |
| tBHA                    | BUSY HIGH from Address Mismatch <sup>[18]</sup> |          | 20      |          | 20      |          | 25      |          | 30      | ns    |  |
| tBLC                    | BUSY LOW from CE LOW                            |          | 20      |          | 20      |          | 25      |          | 30      | ns    |  |
| tBHC                    | BUSY HIGH from CE HIGH <sup>[18]</sup>          |          | 20      |          | 20      |          | 25      |          | 30      | ns    |  |
| tps                     | Port Set-Up for Priority                        | 5        |         | 5        |         | 5        |         | 5        |         | ns    |  |
| tWB*                    | WE LOW after BUSY LOW                           | 0        |         | 0        |         | 0        |         | 0        |         | ns    |  |
| tWH                     | WE HIGH After BUSY HIGH                         | 20       |         | 30       |         | 35       |         | 35       |         | ns    |  |
| tBDD                    | BUSY HIGH to Valid Data                         |          | 25      |          | 35      |          | 45      |          | 45      | ns    |  |
| tDDD                    | Write Data Valid to Read Data Valid             |          | Note 17 |          | Note 17 |          | Note 17 |          | Note 17 | ns    |  |
| tWDD                    | Write Pulse to Data Delay                       |          | Note 17 |          | Note 17 |          | Note 17 |          | Note 17 | ns    |  |
| <b>INTERRUPT TIMING</b> |   |          |         |          |         |          |         |          |         |       |  |
| tWINS                   | WE to INTERRUPT Set Time                        |          | 25      |          | 25      |          | 35      |          | 45      | ns    |  |
| tEINS                   | CE to INTERRUPT Set Time                        |          | 25      |          | 25      |          | 35      |          | 45      | ns    |  |
| tINS                    | Address to INTERRUPT Set Time                   |          | 25      |          | 25      |          | 35      |          | 45      | ns    |  |
| tOINR                   | OE to INTERRUPT Reset Time <sup>[18]</sup>      |          | 25      |          | 25      |          | 35      |          | 45      | ns    |  |
| tEINR                   | CE to INTERRUPT Reset Time <sup>[18]</sup>      |          | 25      |          | 25      |          | 35      |          | 45      | ns    |  |
| tINR                    | Address to INTERRUPT Reset Time <sup>[18]</sup> |          | 25      |          | 25      |          | 35      |          | 45      | ns    |  |

Shaded area contains preliminary information.

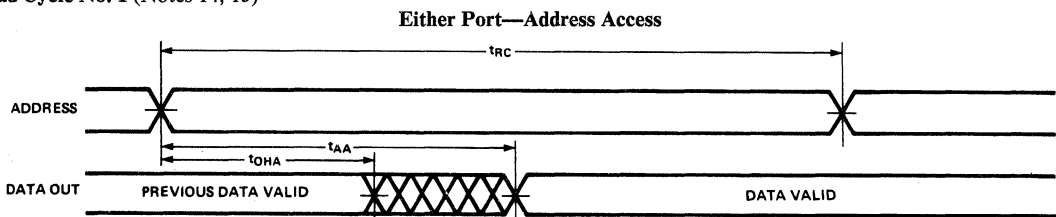
\*CY7C142/CY7C146 Only

Notes:

- Data I/O pins enter high-impedance state, as shown, when OE is held LOW during write.
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 2. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- WE is HIGH for read cycle.
- Device is continuously selected. OE, CE = V<sub>IL</sub>.
- Address valid prior to or coincident with CE transition LOW.
- A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
  - BUSY on Port B goes HIGH.
  - Port B's address toggled.
  - CE for Port B is toggled.
  - WE for Port B is toggled.
- These parameters are measured from the input signal changing, until the output pin goes to a high impedance state.
- For master/slave combinations t<sub>WC</sub> = t<sub>PWE</sub> + t<sub>BLA</sub>.

Switching Waveforms

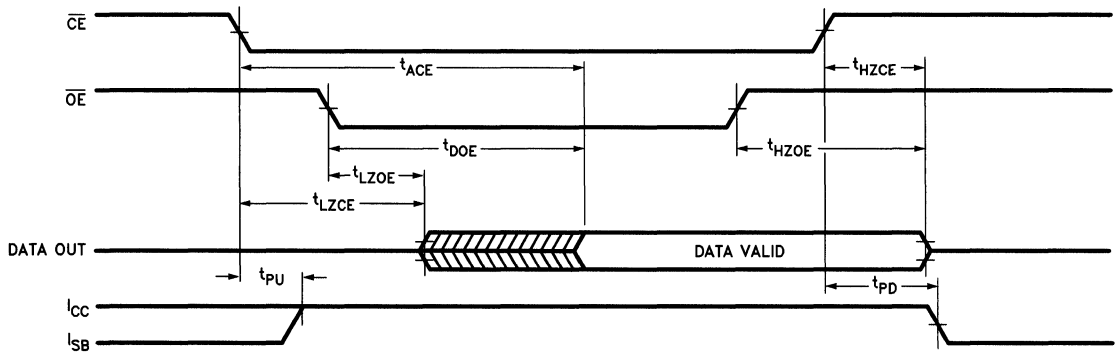
Read Cycle No. 1 (Notes 14, 15)



Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 14, 16)

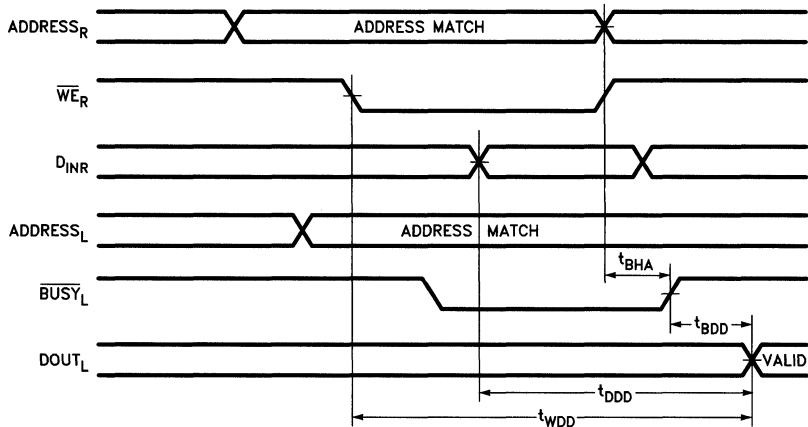
Either Port— $\overline{CE}/\overline{OE}$  Access



0106-10

Read Cycle No. 3 (Note 14)

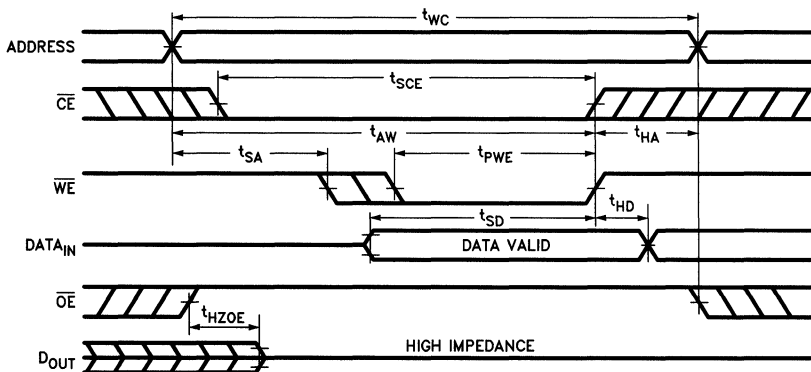
READ with  $\overline{BUSY}$



0106-11

Write Cycle No. 1 (Notes 9, 13)

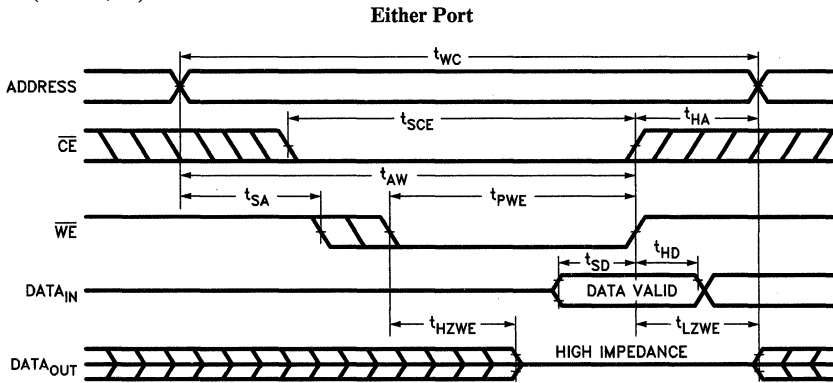
Either Port



0106-13

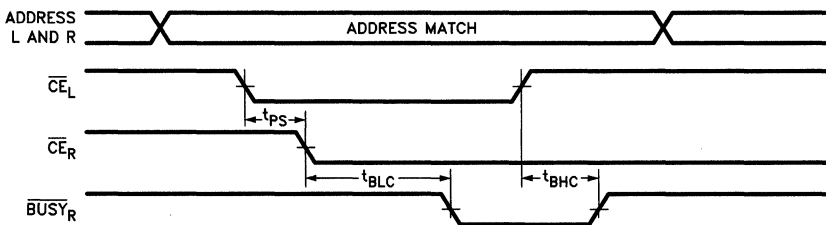
Switching Waveforms (Continued)

Write Cycle No. 2 (Notes 9, 13)

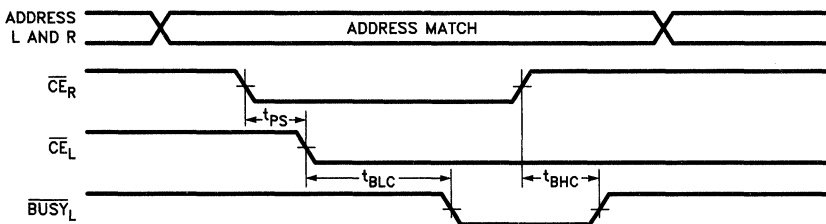


BUSY Timing Diagram No. 1 (CE Arbitration)

$\overline{CE}_L$  Valid First:



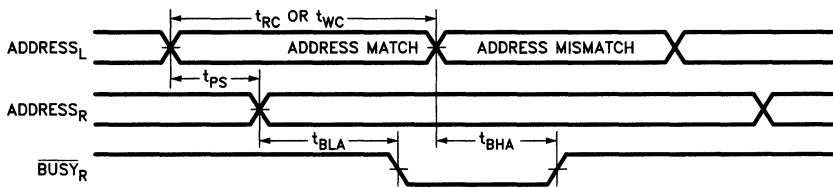
$\overline{CE}_R$  Valid First:



Switching Waveforms (Continued)

BUSY Timing Diagram No. 2 (Address Arbitration)

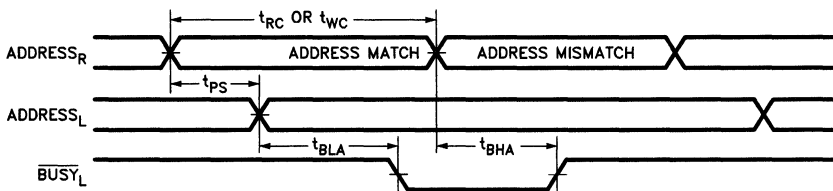
LEFT Address Valid First:



0106-17

BUSY Timing Diagram No. 2

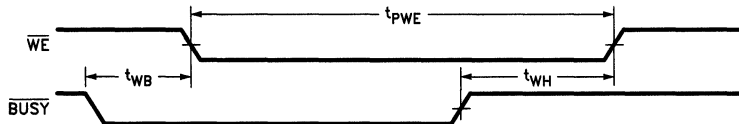
RIGHT Address Valid First:



0106-18

BUSY Timing Diagram No. 3

WRITE with  $\overline{\text{BUSY}}$  (SLAVE: CY7C142/CY7C146) (Note 20):



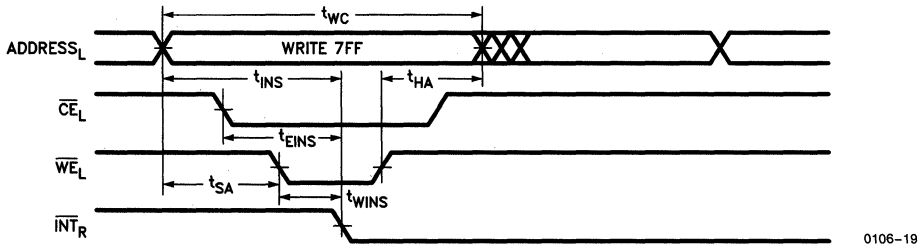
0106-12



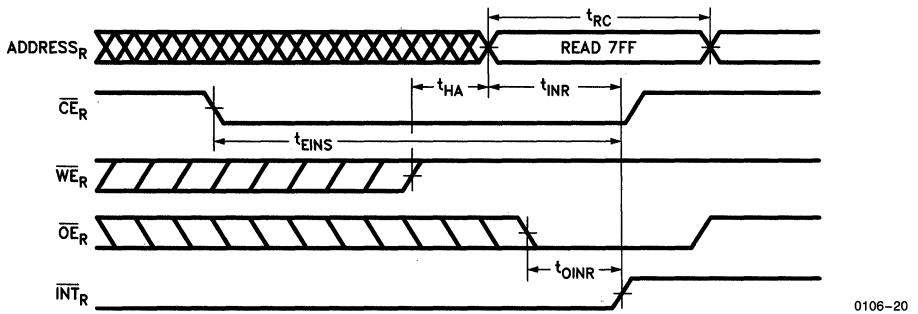
**Switching Waveforms (Continued)**

**Interrupt Timing Diagram (Note 5)**

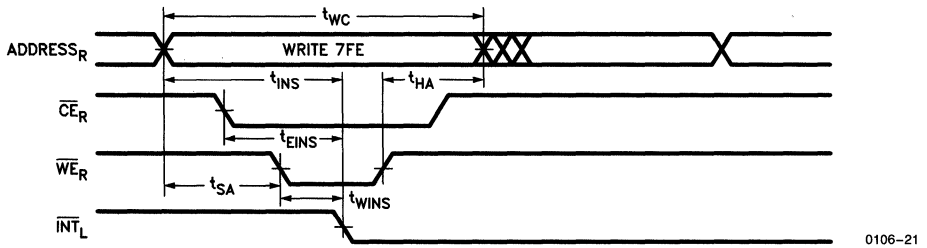
**LEFT Side Sets  $\overline{INT}_R$ :**



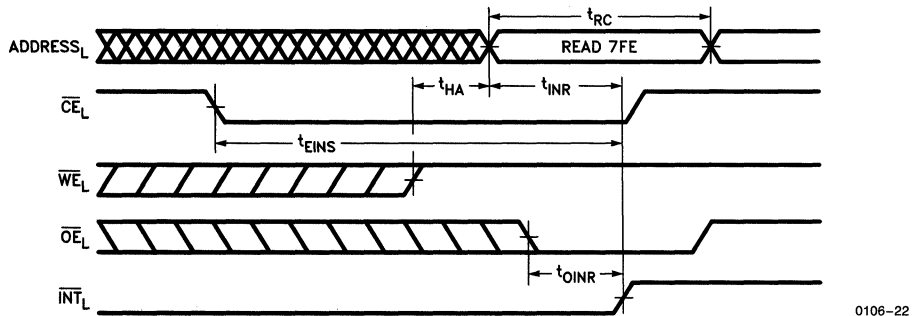
**RIGHT Side Clears  $\overline{INT}_R$ :**



**RIGHT Side Sets  $\overline{INT}_L$ :**

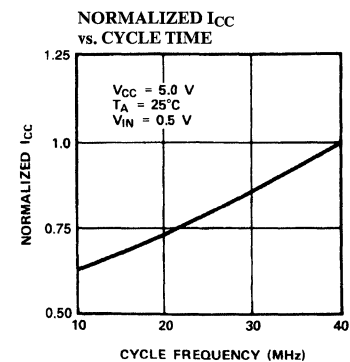
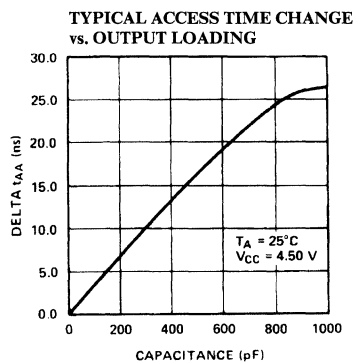
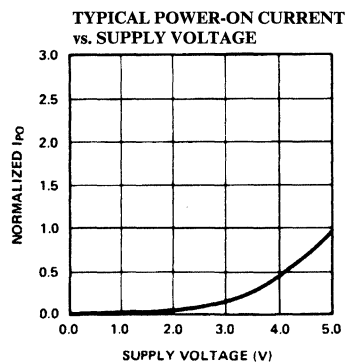
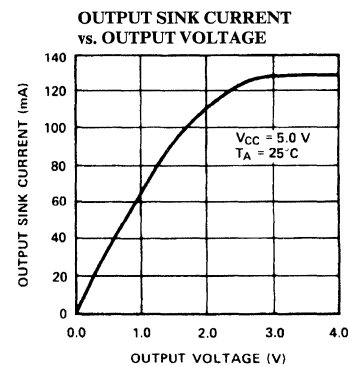
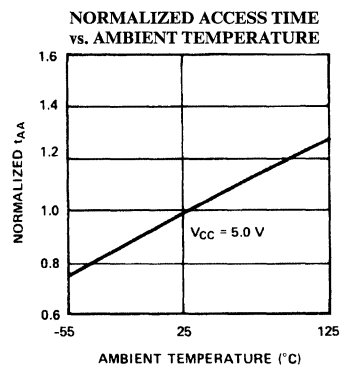
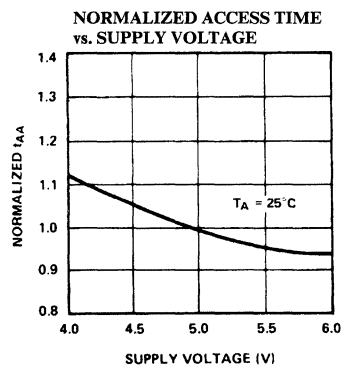
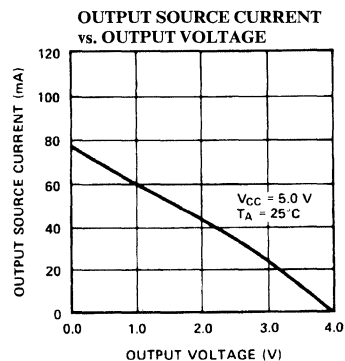
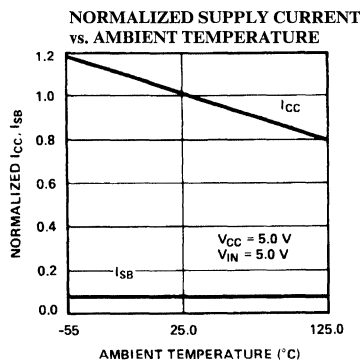
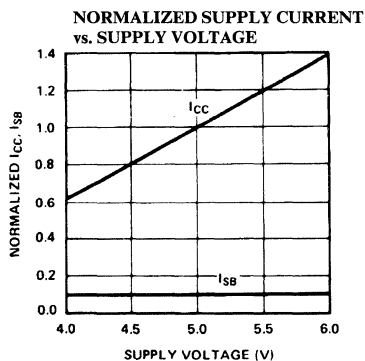


**LEFT Side Clears  $\overline{INT}_L$ :**

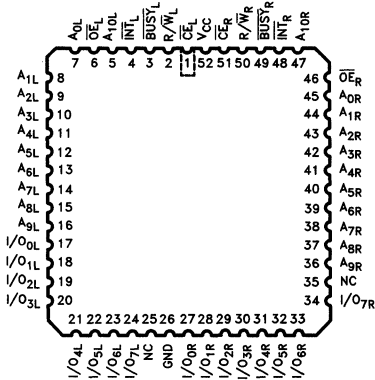


## Typical DC and AC Characteristics

2

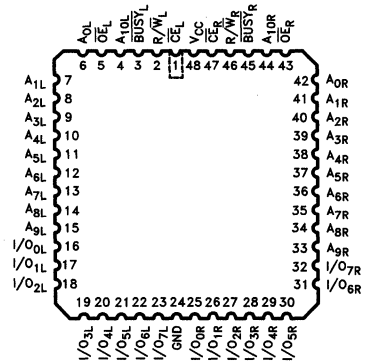


## Pin Configurations



52-Pin LCC/PLCC  
Top View

0106-23



48-Pin LCC  
Top View

0106-24

## Ordering Information

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C132-25PC  | P25          | Commercial      |
|            | CY7C132-25DC  | D26          |                 |
|            | CY7C132-25LC  | L68          |                 |
| 35         | CY7C132-35PC  | P25          | Commercial      |
|            | CY7C132-35DC  | D26          |                 |
|            | CY7C132-35LC  | L68          |                 |
|            | CY7C132-35DMB | D26          | Military        |
|            | CY7C132-35LMB | L68          |                 |
| 45         | CY7C132-45PC  | P25          | Commercial      |
|            | CY7C132-45DC  | D26          |                 |
|            | CY7C132-45LC  | L68          |                 |
|            | CY7C132-45DMB | D26          | Military        |
|            | CY7C132-45LMB | L68          |                 |
| 55         | CY7C132-55PC  | P25          | Commercial      |
|            | CY7C132-55DC  | D26          |                 |
|            | CY7C132-55LC  | L68          |                 |
|            | CY7C132-55DMB | D26          | Military        |
|            | CY7C132-55LMB | L68          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C142-25PC  | P25          | Commercial      |
|            | CY7C142-25DC  | D26          |                 |
|            | CY7C142-25LC  | L68          |                 |
| 35         | CY7C142-35PC  | P25          | Commercial      |
|            | CY7C142-35DC  | D26          |                 |
|            | CY7C142-35LC  | L68          |                 |
|            | CY7C142-35DMB | D26          | Military        |
|            | CY7C142-35LMB | L68          |                 |
| 45         | CY7C142-45PC  | P25          | Commercial      |
|            | CY7C142-45DC  | D26          |                 |
|            | CY7C142-45LC  | L68          |                 |
|            | CY7C142-45DMB | D26          | Military        |
|            | CY7C142-45LMB | L68          |                 |
| 55         | CY7C142-55PC  | P25          | Commercial      |
|            | CY7C142-55DC  | D26          |                 |
|            | CY7C142-55LC  | L68          |                 |
|            | CY7C142-55DMB | D26          | Military        |
|            | CY7C142-55LMB | L68          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C136-25LC  | L69          | Commercial      |
|            | CY7C136-25JC  | J69          |                 |
| 35         | CY7C136-35LC  | L69          | Commercial      |
|            | CY7C136-35JC  | J69          |                 |
|            | CY7C136-35LMB | L69          | Military        |
| 45         | CY7C136-45LC  | L69          | Commercial      |
|            | CY7C136-45JC  | J69          |                 |
|            | CY7C136-45LMB | L69          | Military        |
| 55         | CY7C136-55LC  | L69          | Commercial      |
|            | CY7C136-55JC  | J69          |                 |
|            | CY7C136-55LMB | L69          | Military        |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C146-25LC  | L69          | Commercial      |
|            | CY7C146-25JC  | J69          |                 |
| 35         | CY7C146-35LC  | L69          | Commercial      |
|            | CY7C146-35JC  | J69          |                 |
|            | CY7C146-35LMB | L69          | Military        |
| 45         | CY7C146-45LC  | L69          | Commercial      |
|            | CY7C146-45JC  | J69          |                 |
|            | CY7C146-45LMB | L69          | Military        |
| 55         | CY7C146-55LC  | L69          | Commercial      |
|            | CY7C146-55JC  | J69          |                 |
|            | CY7C146-55LMB | L69          | Military        |

Shaded area contains preliminary information.

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>OS</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB1</sub>     | 1,2,3     |
| I <sub>SB2</sub>     | 1,2,3     |
| I <sub>SB3</sub>     | 1,2,3     |

| Parameters       | Subgroups |
|------------------|-----------|
| I <sub>SB4</sub> | 1,2,3     |

2

#### Switching Characteristics

| Parameters                   | Subgroups   |
|------------------------------|-------------|
| <b>READ CYCLE</b>            |             |
| t <sub>AA</sub>              | 7,8,9,10,11 |
| t <sub>OHA</sub>             | 7,8,9,10,11 |
| t <sub>ACE</sub>             | 7,8,9,10,11 |
| t <sub>DOE</sub>             | 7,8,9,10,11 |
| <b>WRITE CYCLE</b>           |             |
| t <sub>SCE</sub>             | 7,8,9,10,11 |
| t <sub>AW</sub>              | 7,8,9,10,11 |
| t <sub>HA</sub>              | 7,8,9,10,11 |
| t <sub>SA</sub>              | 7,8,9,10,11 |
| t <sub>PWE</sub>             | 7,8,9,10,11 |
| t <sub>SD</sub>              | 7,8,9,10,11 |
| t <sub>HD</sub>              | 7,8,9,10,11 |
| <b>BUSY/INTERRUPT TIMING</b> |             |
| t <sub>BLA</sub>             | 7,8,9,10,11 |
| t <sub>BHA</sub>             | 7,8,9,10,11 |
| t <sub>BLC</sub>             | 7,8,9,10,11 |
| t <sub>BHC</sub>             | 7,8,9,10,11 |
| t <sub>PS</sub>              | 7,8,9,10,11 |
| t <sub>WINS</sub>            | 7,8,9,10,11 |
| t <sub>EINS</sub>            | 7,8,9,10,11 |
| t <sub>INS</sub>             | 7,8,9,10,11 |

| Parameters                               | Subgroups   |
|--|-------------|
| <b>BUSY/INTERRUPT TIMING (Continued)</b> |             |
| t <sub>OINR</sub>                        | 7,8,9,10,11 |
| t <sub>EINR</sub>                        | 7,8,9,10,11 |
| t <sub>INR</sub>                         | 7,8,9,10,11 |
| <b>BUSY TIMING</b>                       |             |
| t <sub>WB</sub> <sup>[1]</sup>           | 7,8,9,10,11 |
| t <sub>WH</sub>                          | 7,8,9,10,11 |
| t <sub>BDD</sub>                         | 7,8,9,10,11 |
| t <sub>DDD</sub>                         | 7,8,9,10,11 |
| t <sub>WDD</sub>                         | 7,8,9,10,11 |

**Note:**

1. CY7C142 only.

Document #: 38-00061-C



**Features**

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed—25 ns
- Low active power  
— 440 mW (commercial)  
— 605 mW (military)
- Low standby power  
— 55 mW
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2000V electrostatic discharge

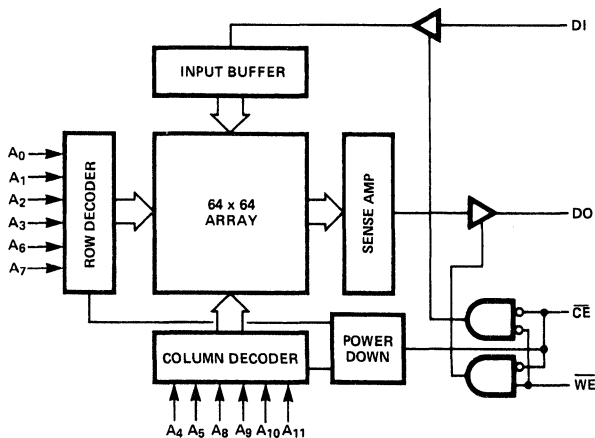
**Functional Description**

The CY7C147 is a high performance CMOS static RAM organized as 4096 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable (CE) and three-state drivers. The CY7C147 has an automatic power-down feature, reducing the power consumption by 80% when deselected. Writing to the device is accomplished when the chip enable (CE) and write enable (WE) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A<sub>0</sub> through A<sub>11</sub>).

Reading the device is accomplished by taking the chip enable (CE) LOW, while write enable (WE) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

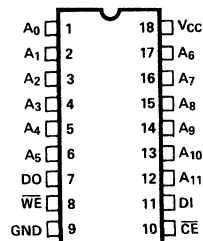
The output pin stays in high impedance state when chip enable (CE) is HIGH or write enable (WE) is LOW.

**Logic Block Diagram**

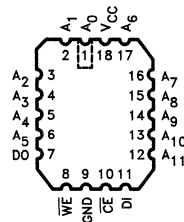


0019-1

**Pin Configurations**



0019-2



0019-3

**Selection Guide**

|                                |            | 7C147-25 | 7C147-35 | 7C147-45 |
|--------------------------------|------------|----------|----------|----------|
| Maximum Access Time (ns)       | Commercial | 25       | 35       | 45       |
|                                | Military   |          | 35       | 45       |
| Maximum Operating Current (mA) | Commercial | 90       | 80       | 80       |
|                                | Military   |          | 110      | 110      |
| Maximum Standby Current (mA)   | Commercial | 15       | 10       | 10       |
|                                | Military   |          | 10       | 10       |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|  |                 |
|--|-----------------|
| Storage Temperature .....                                    | -65°C to +150°C |
| Ambient Temperature with<br>Power Applied .....              | -55°C to +125°C |
| Supply Voltage to Ground Potential<br>(Pin 18 to Pin 9)..... | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs<br>in High Z State.....        | -0.5V to +7.0V  |
| DC Input Voltage .....                                       | -3.0V to +7.0V  |
| Output Current into Outputs (Low) .....                      | 20 mA           |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | > 2001V<br>(Per MIL-STD-883 Method 3015) |
| Latchup Current .....          | > 200 mA                                 |

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[4]</sup>

| Parameters       | Description  | Test Conditions   | 7C147-25   |      | 7C147-35, 45 |      | Units |
|------------------|--|---|------------|------|--------------|------|-------|
|                  |  |   | Min.       | Max. | Min.         | Max. |       |
| V <sub>OH</sub>  | Output HIGH Voltage  | V <sub>CC</sub> = Min. I <sub>OH</sub> = -4.0 mA          | 2.4        |      | 2.4          |      | V     |
| V <sub>OL</sub>  | Output LOW Voltage   | V <sub>CC</sub> = Min. I <sub>OL</sub> = 12.0 mA          |            | 0.4  |              | 0.4  | V     |
| V <sub>IH</sub>  | Input High Voltage   |   | 2.0        | 6.0  | 2.0          | 6.0  | V     |
| V <sub>IL</sub>  | Input Low Voltage  |   | -3.0       | 0.8  | -3.0         | 0.8  | V     |
| I <sub>IX</sub>  | Input Load Current   | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                    | -10        | +10  | -10          | +10  | μA    |
| I <sub>OZ</sub>  | Output Leakage Current   | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub><br>Output Disabled | -50        | +50  | -50          | +50  | μA    |
| I <sub>OS</sub>  | Output Short <sup>[1]</sup><br>Circuit Current                 | V <sub>CC</sub> = Max. V <sub>OUT</sub> = GND             |            | -350 |              | -350 | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating<br>Supply Current                    | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA         | Commercial | 90   | 80           |      | mA    |
|                  |  |   | Military   |      |              | 110  |       |
| I <sub>SB1</sub> | Automatic $\overline{CE}$ <sup>[2]</sup><br>Power Down Current | Max. V <sub>CC</sub> ,<br>$\overline{CE} \geq V_{IH}$     | Commercial | 15   | 10           |      | mA    |
|                  |  |   | Military   |      |              | 10   |       |

### Capacitance<sup>[5]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 6    |       |

#### Notes:

- Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the CE input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.

### AC Test Loads and Waveforms

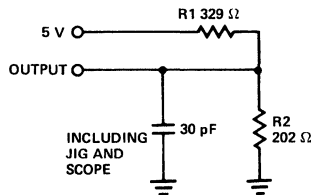


Figure 1a

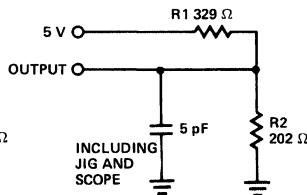


Figure 1b

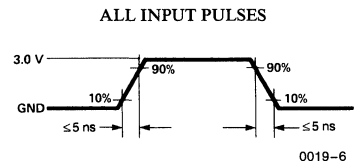
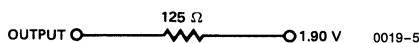


Figure 2

Equivalent to:

THÉVENIN EQUIVALENT

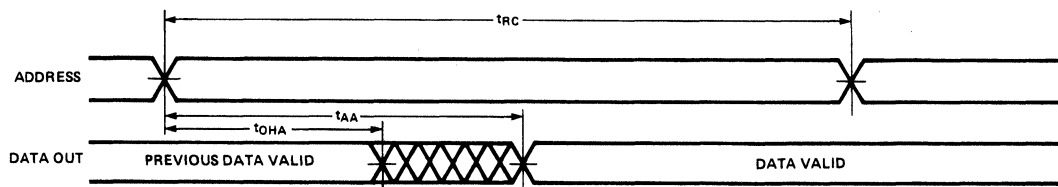


**Switching Characteristics Over Operating Range<sup>[6]</sup>**

| Parameters                       | Description                                      | 7C147-25 |      | 7C147-35 |      | 7C147-45 |      | Units |
|----------------------------------|--|----------|------|----------|------|----------|------|-------|
|                                  |  | Min.     | Max. | Min.     | Max. | Min.     | Max. |       |
| <b>READ CYCLE</b>                |  |          |      |          |      |          |      |       |
| t <sub>RC</sub>                  | Read Cycle Time                                  | 25       |      | 35       |      | 45       |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid                            |          | 25   |          | 35   |          | 45   | ns    |
| t <sub>OHA</sub>                 | Data Hold from Address Change                    | 3        |      | 5        |      | 5        |      | ns    |
| t <sub>ACE</sub>                 | $\overline{CS}$ Low to Data Valid                |          | 25   |          | 35   |          | 45   | ns    |
| t <sub>LZCE</sub>                | $\overline{CE}$ LOW to Low Z <sup>[8]</sup>      | 5        |      | 5        |      | 5        |      | ns    |
| t <sub>HZCE</sub>                | $\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup> |          | 20   |          | 30   |          | 30   | ns    |
| t <sub>PU</sub>                  | $\overline{CE}$ LOW to Power Up                  | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>PD</sub>                  | $\overline{CE}$ HIGH to Power Down               |          | 20   |          | 20   |          | 20   | ns    |
| <b>WRITE CYCLE<sup>[9]</sup></b> |  |          |      |          |      |          |      |       |
| t <sub>WC</sub>                  | Write Cycle Time                                 | 25       |      | 35       |      | 45       |      | ns    |
| t <sub>SCE</sub>                 | $\overline{CE}$ LOW to Write End                 | 25       |      | 35       |      | 45       |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End                      | 25       |      | 35       |      | 45       |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End                      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                    | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>PWE</sub>                 | $\overline{WE}$ Pulse Width                      | 15       |      | 20       |      | 25       |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End                         | 15       |      | 20       |      | 25       |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End                         | 0        |      | 10       |      | 10       |      | ns    |
| t <sub>LZWE</sub>                | $\overline{WE}$ HIGH to Low Z <sup>[8]</sup>     | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>HZWE</sub>                | $\overline{WE}$ LOW to High Z <sup>[7, 8]</sup>  |          | 15   |          | 20   |          | 25   | ns    |

**Notes:**

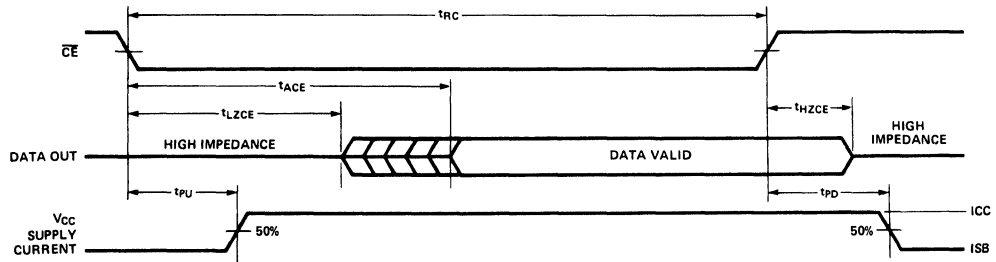
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZCE</sub> and t<sub>HZWE</sub> are tested with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> for all devices.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CE} = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms**
**Read Cycle No. 1 (Notes 10, 11)**


0019-7

Switching Waveforms (Continued)

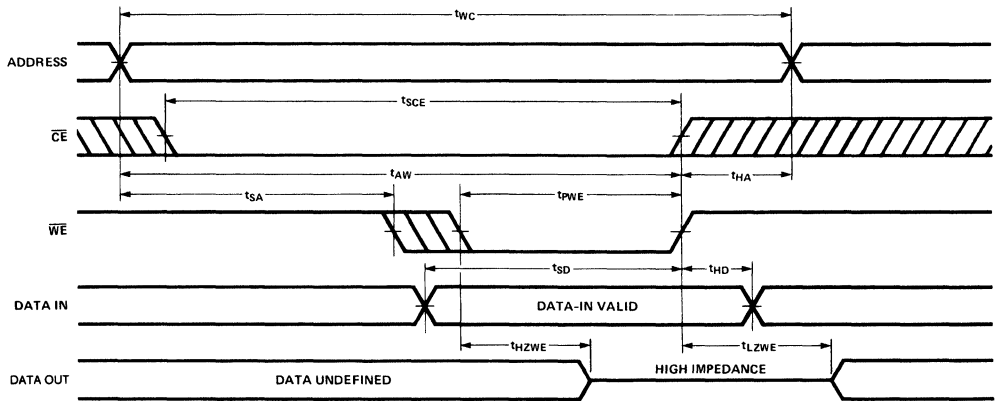
Read Cycle No. 2 (Notes 10, 12)



0019-8

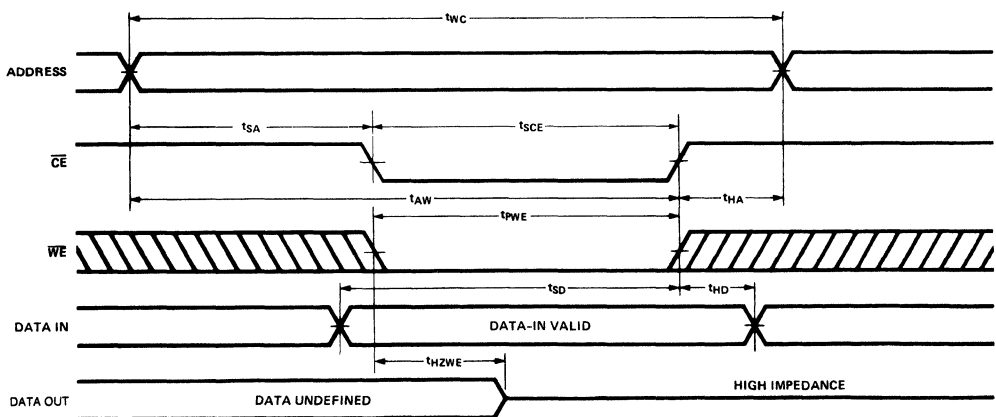
2

Write Cycle No. 1 ( $\overline{WE}$  Controlled) (Note 9)



0019-9

Write Cycle No. 2 ( $\overline{CE}$  Controlled) (Note 9)

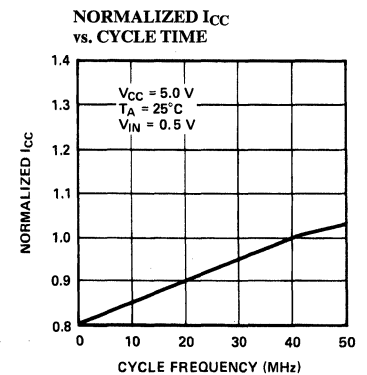
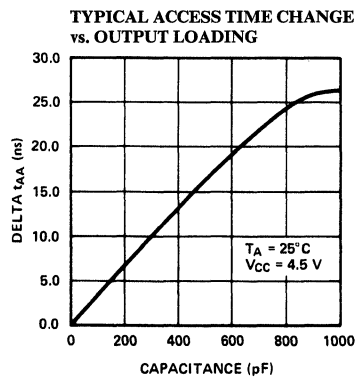
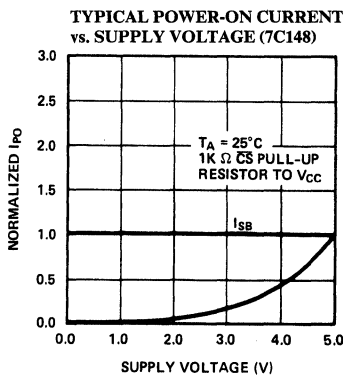
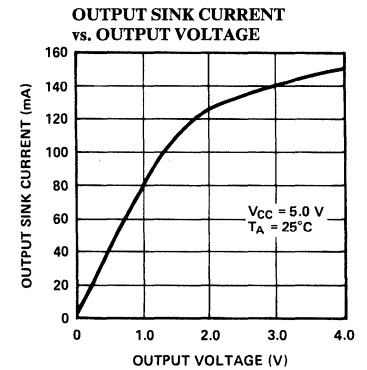
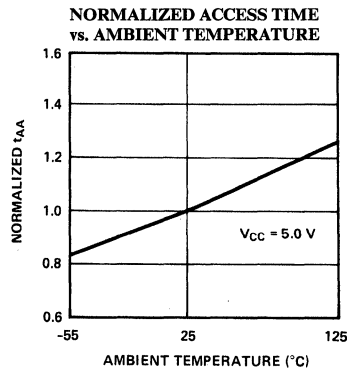
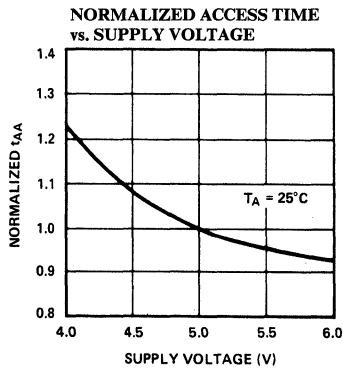
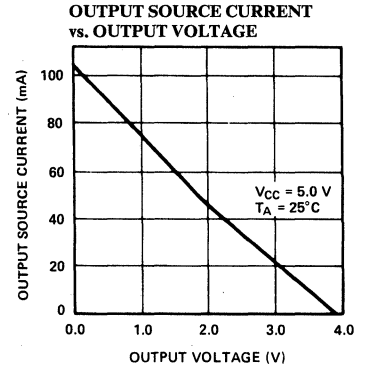
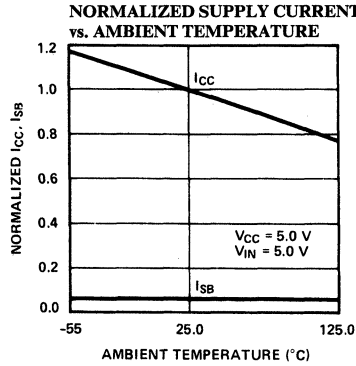
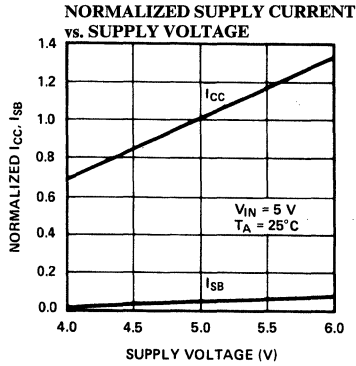


0019-10

Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.



## Typical DC and AC Characteristics



### Ordering Information

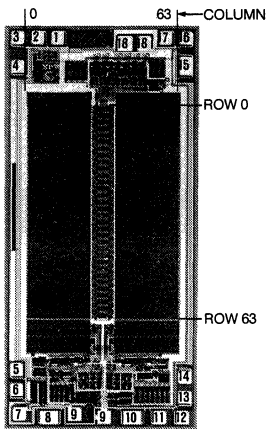
| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C147-25PC  | P3           | Commercial      |
|            | CY7C147-25DC  | D4           | Commercial      |
|            | CY7C147-25LC  | L50          | Commercial      |
| 35         | CY7C147-35PC  | P3           | Commercial      |
|            | CY7C147-35DC  | D4           | Commercial      |
|            | CY7C147-35LC  | L50          | Commercial      |
|            | CY7C147-35DMB | D4           | Military        |
|            | CY7C147-35LMB | L50          | Military        |
| 45         | CY7C147-45PC  | P3           | Commercial      |
|            | CY7C147-45DC  | D4           | Commercial      |
|            | CY7C147-45LC  | L50          | Commercial      |
|            | CY7C147-45DMB | D4           | Military        |
|            | CY7C147-45LMB | L50          | Military        |

### Address Designators

| Address Name    | Address Function | Pin Number |
|-----------------|------------------|------------|
| A <sub>0</sub>  | X <sub>0</sub>   | 1          |
| A <sub>1</sub>  | X <sub>1</sub>   | 2          |
| A <sub>2</sub>  | X <sub>2</sub>   | 3          |
| A <sub>3</sub>  | X <sub>3</sub>   | 4          |
| A <sub>4</sub>  | Y <sub>0</sub>   | 5          |
| A <sub>5</sub>  | Y <sub>1</sub>   | 6          |
| A <sub>6</sub>  | X <sub>4</sub>   | 17         |
| A <sub>7</sub>  | X <sub>5</sub>   | 16         |
| A <sub>8</sub>  | Y <sub>2</sub>   | 15         |
| A <sub>9</sub>  | Y <sub>3</sub>   | 14         |
| A <sub>10</sub> | Y <sub>4</sub>   | 13         |
| A <sub>11</sub> | Y <sub>5</sub>   | 12         |

2

### Bit Map



0019-12

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL</sub> Max. | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB1</sub>     | 1,2,3     |

**Switching Characteristics**

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>ACE</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>SCE</sub>   | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |

Document #: 38-00030-B



**Features**

- Automatic power-down when deselected (7C148)
- CMOS for optimum speed/power
- 25 ns access time
- Low active power
  - 440 mW (commercial)
  - 605 mW (military)
- Low standby power (7C148)
  - 82.5 mW (25 ns version)
  - 55 mW (all others)
- 5 volt power supply  $\pm 10\%$  tolerance both commercial and military
- TTL compatible inputs and outputs

**Functional Description**

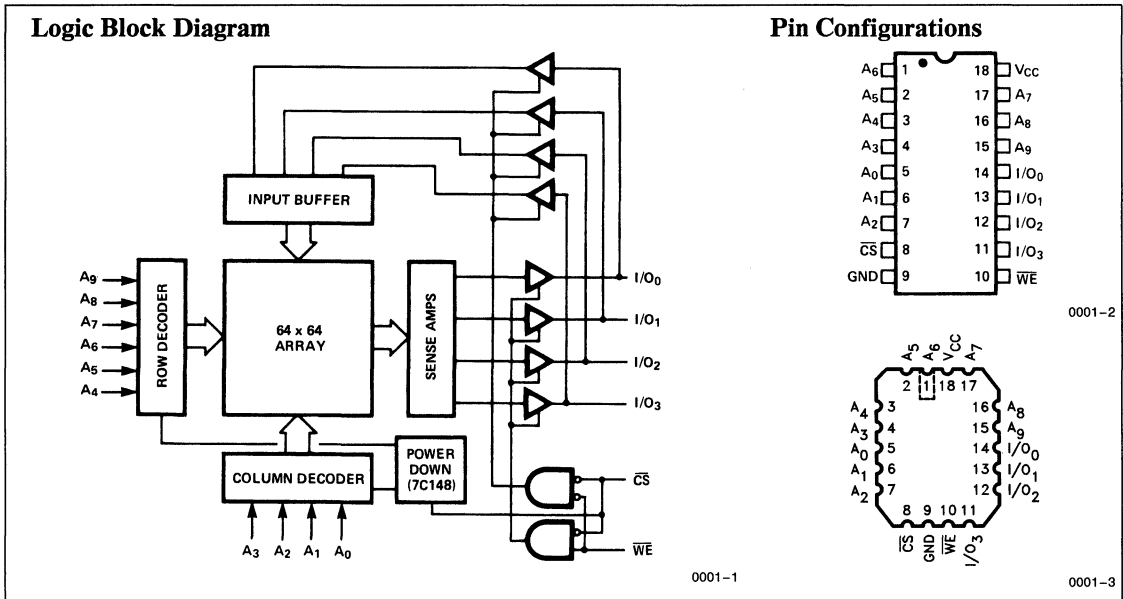
The CY7C148 and CY7C149 are high performance CMOS static RAMs organized as 1024 x 4 bits. Easy memory expansion is provided by an active LOW chip select ( $\overline{CS}$ ) input, and three-state outputs. The CY7C148 and CY7C149 are identical except that the CY7C148 includes an automatic ( $\overline{CS}$ ) power-down feature. The CY7C148 remains in a low power mode as long as the device remains unselected, i.e. ( $\overline{CS}$ ) is HIGH, thus reducing the average power requirements of the device. The chip select ( $\overline{CS}$ ) of the CY7C149 does not affect the power dissipation of the device.

An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When the chip

select ( $\overline{CS}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW, data on the four data input/output pins ( $I/O_0$  through  $I/O_3$ ) is written into the memory location addressed by the address present on the address pins ( $A_0$  through  $A_9$ ).

Reading the device is accomplished by selecting the device, ( $\overline{CS}$ ) active LOW, while ( $\overline{WE}$ ) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins ( $A_0$  through  $A_9$ ) is present on the four data input/output pins ( $I/O_0$  through  $I/O_3$ ).

The input/output pins ( $I/O_0$  through  $I/O_3$ ) remain in a high impedance state unless the chip is selected, and write enable ( $\overline{WE}$ ) is high.



**Selection Guide**

|                                |            | 7C148-25 | 7C148-35 | 7C148-45 | 7C149-25 | 7C149-35 | 7C149-45 |
|--------------------------------|------------|----------|----------|----------|----------|----------|----------|
| Maximum Access Time (ns)       |            | 25       | 35       | 45       | 25       | 35       | 45       |
| Maximum Operating Current (mA) | Commercial | 90       | 80       | 80       | 90       | 80       | 80       |
|                                | Military   |          | 110      | 110      |          | 110      | 110      |
| Maximum Standby Current (mA)   | Commercial | 15       | 10       | 10       |          |          |          |
|                                | Military   |          | 10       | 10       |          |          |          |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|  |                       |
|--|-----------------------|
| Storage Temperature                                  | ..... -65°C to +150°C |
| Ambient Temperature with Power Applied               | ..... -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 18 to Pin 9) | ..... -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State        | ..... -0.5V to +7.0V  |
| DC Input Voltage                                     | ..... -3.0V to +7.0V  |
| Output Current into Outputs (Low)                    | ..... 20 mA           |

|  |                |
|--|----------------|
| Static Discharge Voltage (Per MIL-STD-883 Method 3015) | ..... > 2001V  |
| Latchup Current  | ..... > 200 mA |

## Operating Range

| Range                    | Ambient Temperature | V <sub>CC</sub> |
|--------------------------|---------------------|-----------------|
| Commercial               | 0°C to +70°C        | 5V ±10%         |
| Military <sup>[11]</sup> | -55°C to +125°C     | 5V ±10%         |

## Electrical Characteristics Over Operating Range<sup>[12]</sup>

| Parameters       | Description                                  | Test Conditions   | 7C148/9-25          |      | 7C148/9-35, 45 |      | Units |
|------------------|--|---|---------------------|------|----------------|------|-------|
|                  |  |   | Min.                | Max. | Min.           | Max. |       |
| I <sub>OH</sub>  | Output High Current                          | V <sub>OH</sub> = 2.4V<br>V <sub>CC</sub> = 4.5V  | -4                  |      | -4             |      | mA    |
| I <sub>OL</sub>  | Output Low Current                           | V <sub>OL</sub> = 0.4V  | 8                   |      | 8              |      | mA    |
| V <sub>IH</sub>  | Input High Voltage                           |   | 2.0                 | 6.0  | 2.0            | 6.0  | V     |
| V <sub>IL</sub>  | Input Low Voltage                            |   | -3.0                | 0.8  | -3.0           | 0.8  | V     |
| I <sub>IX</sub>  | Input Load Current                           | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>  | -10                 | 10   | -10            | 10   | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                       | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> Output Disabled                                  | -50                 | 50   | -50            | 50   | μA    |
| C <sub>I</sub>   | Input Capacitance <sup>[13]</sup>            | Test Frequency = 1.0 MHz<br>T <sub>A</sub> = 25°C, All Pins at 0V, V <sub>CC</sub> = 5V |                     | 5    |                | 5    | pF    |
| C <sub>I/O</sub> | Input/Output Capacitance <sup>[13]</sup>     |   |                     | 7    |                | 7    |       |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current     | Max. V <sub>CC</sub> , $\overline{CS} \leq V_{IL}$<br>Output Open                       | Commercial          | 90   | 80             | mA   |       |
|                  |  |   | Military            |      | 110            |      |       |
| I <sub>SB</sub>  | Automatic $\overline{CS}$ Power Down Current | Max. V <sub>CC</sub> ,<br>$\overline{CS} \geq V_{IH}$ only                              | 7C148<br>Commercial | 15   | 10             | mA   |       |
|                  |  |   | 7C148<br>Military   |      | 10             |      |       |
| I <sub>PO</sub>  | Peak Power-On Current                        | Max. V <sub>CC</sub> ,<br>$\overline{CS} \geq V_{IH}$ <sup>[3]</sup> only               | 7C148<br>Commercial | 15   | 10             | mA   |       |
|                  |  |   | 7C148<br>Military   |      | 10             |      |       |
| I <sub>OS</sub>  | Output Short Circuit Current                 | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> <sup>[10]</sup>                                  | Commercial          | ±275 | ±275           | mA   |       |
|                  |  |   | Military            |      | ±350           |      |       |

### Notes:

- Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance. Output timing reference is 1.5V.
- The internal write time of the memory is defined by the overlap of  $\overline{CS}$  low and  $\overline{WE}$  low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- A pull up resistor to V<sub>CC</sub> on the  $\overline{CS}$  input is required to keep the device deselected during V<sub>CC</sub> power up. Otherwise current will exceed values given (CY7C148 only).
- Chip deselected greater than 25 ns prior to selection.
- Chip deselected less than 25 ns prior to selection.
- At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> for all devices. Transition is measured ±500 mV from steady state voltage with specified loading in Figure 1b.
- $\overline{WE}$  is high for read cycle.
- Device is continuously selected,  $\overline{CS} = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{CS}$  transition low.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms

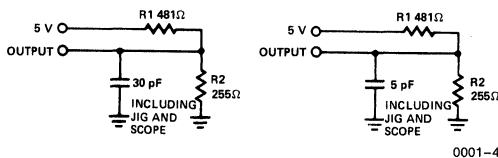


Figure 1a

Figure 1b

Equivalent To:

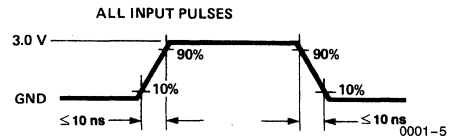
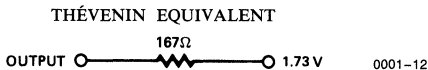


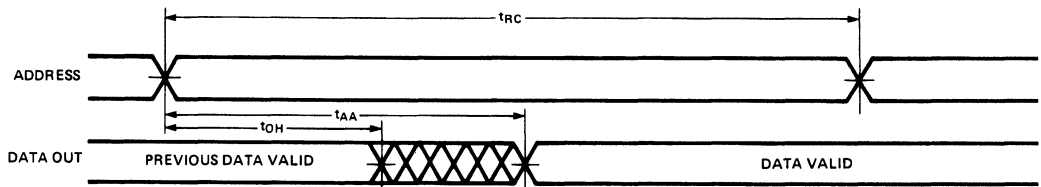
Figure 2

**Switching Characteristics Over Operating Range<sup>[12]</sup>**

| Parameters                             | Description   | 7C148/9-25 |                   | 7C148/9-35 |      | 7C148/9-45 |      | Units |
|--|---|------------|-------------------|------------|------|------------|------|-------|
|  |   | Min.       | Max.              | Min.       | Max. | Min.       | Max. |       |
| <b>READ CYCLE</b>                      |   |            |                   |            |      |            |      |       |
| t <sub>RC</sub>                        | Address Valid to Address Do Not Care Time (Read Cycle Time) | 25         |                   | 35         |      | 45         |      | ns    |
| t <sub>AA</sub>                        | Address Valid to Data Out Valid Delay (Address Access Time) |            | 25                |            | 35   |            | 45   | ns    |
| t <sub>ACS1</sub><br>t <sub>ACS2</sub> | Chip Select Low to Data Out Valid (CY7C148 only)            |            | 25 <sup>[4]</sup> |            | 35   |            | 45   | ns    |
|  |   |            | 30 <sup>[5]</sup> |            | 35   |            | 45   |       |
| t <sub>ACS</sub>                       | Chip Select Low to Data Out Valid (CY7C149 only)            |            | 15                |            | 15   |            | 20   | ns    |
| t <sub>LZ</sub> <sup>[6]</sup>         | Chip Select Low to Data Out On                              | 7C148      | 8                 |            | 10   |            | 10   | ns    |
|  |   | 7C149      | 5                 |            | 5    |            | 5    |       |
| t <sub>HZ</sub> <sup>[6]</sup>         | Chip Select High to Data Out Off                            | 0          | 15                | 0          | 20   | 0          | 20   | ns    |
| t <sub>OH</sub>                        | Address Unknown to Data Out Unknown Time                    | 0          |                   | 0          |      | 5          |      | ns    |
| t <sub>PD</sub>                        | Chip Select High to Power-Down Delay                        | 7C148      |                   | 20         |      | 30         |      | ns    |
| t <sub>PU</sub>                        | Chip Select Low to Power-Up Delay                           | 7C148      | 0                 |            | 0    |            | 0    | ns    |
| <b>WRITE CYCLE</b>                     |   |            |                   |            |      |            |      |       |
| t <sub>WC</sub>                        | Address Valid to Address Do Not Care (Write Cycle Time)     | 25         |                   | 35         |      | 45         |      | ns    |
| t <sub>WP</sub> <sup>[2]</sup>         | Write Enable Low to Write Enable High                       | 20         |                   | 30         |      | 35         |      | ns    |
| t <sub>WR</sub>                        | Address Hold from Write End                                 | 5          |                   | 5          |      | 5          |      | ns    |
| t <sub>WZ</sub> <sup>[6]</sup>         | Write Enable to Output in High Z                            | 0          | 8                 | 0          | 10   | 0          | 15   | ns    |
| t <sub>DW</sub>                        | Data in Valid to Write Enable High                          | 12         |                   | 20         |      | 20         |      | ns    |
| t <sub>DH</sub>                        | Data Hold Time  | 0          |                   | 0          |      | 0          |      | ns    |
| t <sub>AS</sub>                        | Address Valid to Write Enable Low                           | 0          |                   | 0          |      | 0          |      | ns    |
| t <sub>CW</sub> <sup>[2]</sup>         | Chip Select Low to Write Enable High                        | 20         |                   | 30         |      | 40         |      | ns    |
| t <sub>OW</sub> <sup>[6]</sup>         | Write Enable High to Output in Low Z                        | 0          |                   | 0          |      | 0          |      | ns    |
| t <sub>AW</sub>                        | Address Valid to End of Write                               | 20         |                   | 30         |      | 35         |      | ns    |

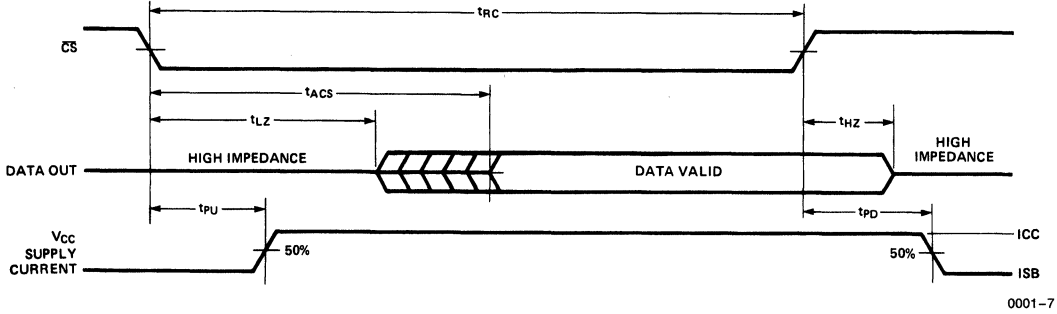
**Switching Waveforms**

Read Cycle No. 1 (Notes 7, 8)

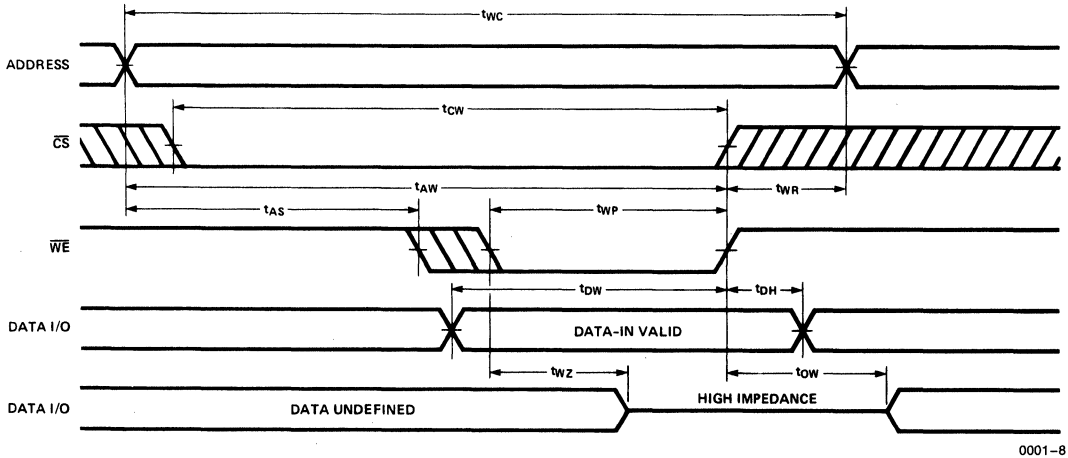


### Switching Waveforms (Continued)

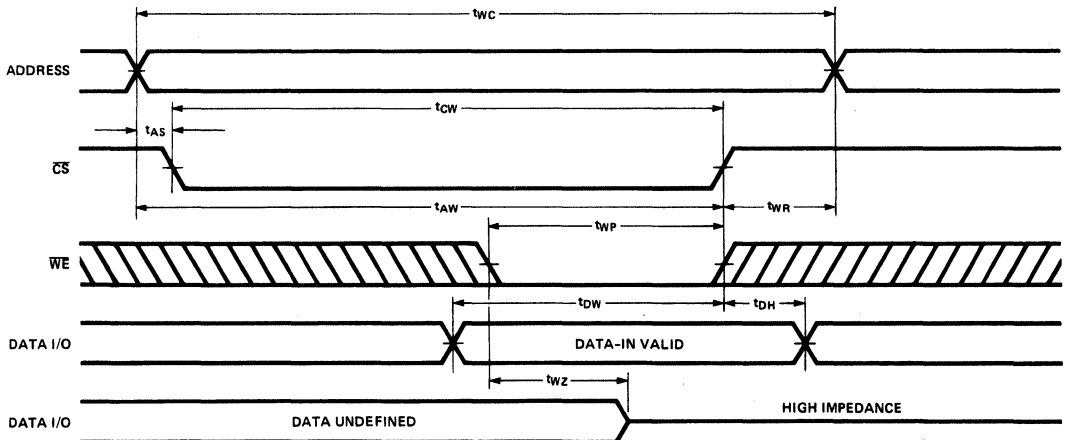
#### Read Cycle No. 2 (Notes 7, 9)



#### Write Cycle No. 1 ( $\overline{WE}$ Controlled)



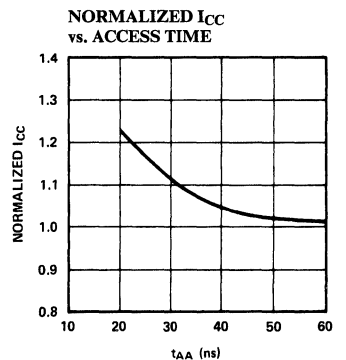
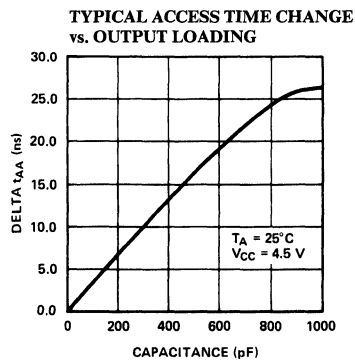
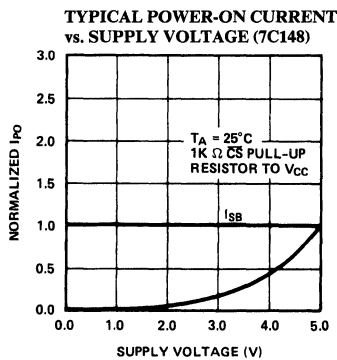
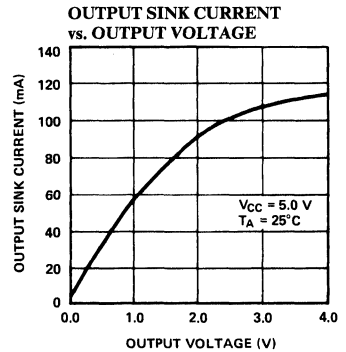
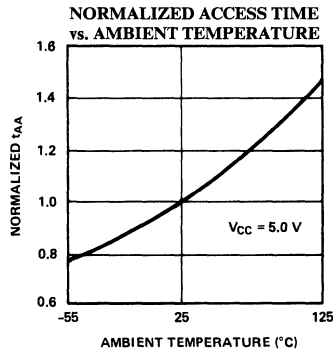
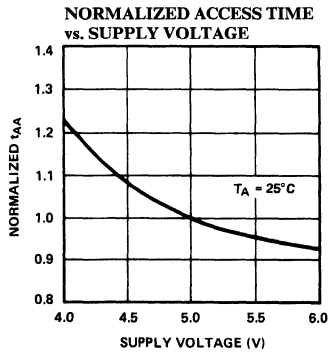
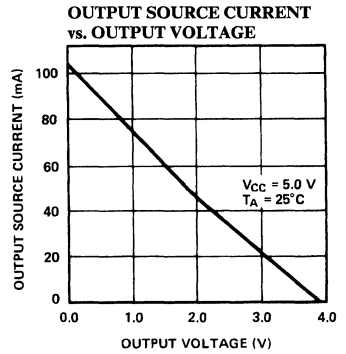
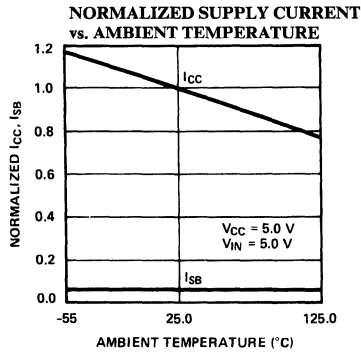
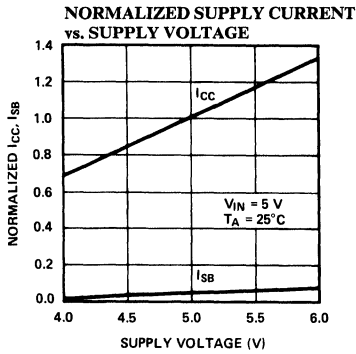
#### Write Cycle No. 2 ( $\overline{CS}$ Controlled)



Note: If  $\overline{CS}$  goes high simultaneously with  $\overline{WE}$  high, the output remains in a high impedance state.

Typical DC and AC Characteristics

2





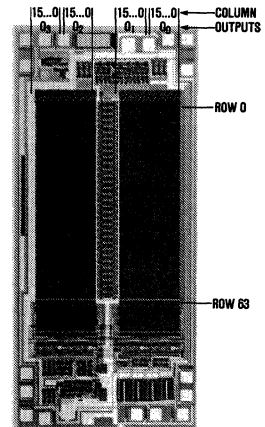
### Ordering Information

| Speed (ns) | Ordering Code                  | Package Type | Operating Range |
|------------|--------------------------------|--------------|-----------------|
| 25         | CY7C148-25PC<br>CY7C149-25PC   | P3           | Commercial      |
|            | CY7C148-25DC<br>CY7C149-25DC   | D4           |                 |
|            | CY7C148-25LC<br>CY7C149-25LC   | L50          |                 |
| 35         | CY7C148-35PC<br>CY7C149-35PC   | P3           | Commercial      |
|            | CY7C148-35DC<br>CY7C149-35DC   | D4           |                 |
|            | CY7C148-35LC<br>CY7C149-35LC   | L50          |                 |
|            | CY7C148-35DMB<br>CY7C149-35DMB | D4           | Military        |
|            | CY7C148-35LMB<br>CY7C149-35LMB | L50          |                 |
| 45         | CY7C148-45PC<br>CY7C149-45PC   | P3           | Commercial      |
|            | CY7C148-45DC<br>CY7C149-45DC   | D4           |                 |
|            | CY7C148-45LC<br>CY7C149-45LC   | L50          |                 |
|            | CY7C148-45DMB<br>CY7C149-45DMB | D4           | Military        |
|            | CY7C148-45LMB<br>CY7C149-45LMB | L50          |                 |

### Address Designators

| Address Name   | Address Function | Pin Number |
|----------------|------------------|------------|
| A <sub>0</sub> | Y <sub>0</sub>   | 5          |
| A <sub>1</sub> | Y <sub>1</sub>   | 6          |
| A <sub>2</sub> | Y <sub>2</sub>   | 7          |
| A <sub>3</sub> | Y <sub>3</sub>   | 4          |
| A <sub>4</sub> | X <sub>0</sub>   | 3          |
| A <sub>5</sub> | X <sub>3</sub>   | 2          |
| A <sub>6</sub> | X <sub>2</sub>   | 1          |
| A <sub>7</sub> | X <sub>5</sub>   | 17         |
| A <sub>8</sub> | X <sub>4</sub>   | 16         |
| A <sub>9</sub> | X <sub>1</sub>   | 15         |

### Bit Map



0001-11

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters                     | Subgroups |
|--------------------------------|-----------|
| I <sub>OH</sub>                | 1,2,3     |
| I <sub>OL</sub>                | 1,2,3     |
| V <sub>IH</sub>                | 1,2,3     |
| V <sub>IL Max.</sub>           | 1,2,3     |
| I <sub>IX</sub>                | 1,2,3     |
| I <sub>OZ</sub>                | 1,2,3     |
| I <sub>CC</sub>                | 1,2,3     |
| I <sub>SB</sub> <sup>[1]</sup> | 1,2,3     |

**2**
**Switching Characteristics**

| Parameters                       | Subgroups   |
|----------------------------------|-------------|
| <b>READ CYCLE</b>                |             |
| t <sub>RC</sub>                  | 7,8,9,10,11 |
| t <sub>AA</sub>                  | 7,8,9,10,11 |
| t <sub>ACS1</sub> <sup>[1]</sup> | 7,8,9,10,11 |
| t <sub>ACS2</sub> <sup>[1]</sup> | 7,8,9,10,11 |
| t <sub>ACS</sub> <sup>[2]</sup>  | 7,8,9,10,11 |
| t <sub>OH</sub>                  | 7,8,9,10,11 |
| <b>WRITE CYCLE</b>               |             |
| t <sub>WC</sub>                  | 7,8,9,10,11 |
| t <sub>WP</sub>                  | 7,8,9,10,11 |
| t <sub>WR</sub>                  | 7,8,9,10,11 |
| t <sub>DW</sub>                  | 7,8,9,10,11 |
| t <sub>DH</sub>                  | 7,8,9,10,11 |
| t <sub>AS</sub>                  | 7,8,9,10,11 |
| t <sub>AW</sub>                  | 7,8,9,10,11 |

**Notes:**

1. 7C148 only.
2. 7C149 only.

Document #: 38-00031-B



**Features**

- Memory reset function
- 1024 x 4 static RAM for control store in high speed computers
- CMOS for optimum speed/power
- High speed
  - 12 ns (commercial)
  - 15 ns (military)
- Low power
  - 495 mW (commercial)
  - 550 mW (military)
- Separate inputs and outputs
- 5 volt power supply  $\pm 10\%$  tolerance both commercial and military
- Capable of withstanding greater than 2001V static discharge
- TTL compatible inputs and outputs

**Functional Description**

The CY7C150 is a high performance CMOS static RAM designed for use in cache memory, high speed graphics, and data acquisition applications. Organized as 1024 words x 4 bits, the entire memory can be reset to zero in two memory cycles.

Separate I/O paths eliminate the need to multiplex data in and data out, providing for simpler board layout and faster system performance. Outputs are tri-stated during write, reset, deselect, or when output enable (OE) is held HIGH, allowing for easy memory expansion.

Reset is initiated by selecting the device (CS = LOW) and pulsing the reset (RS) input LOW. Within two memory cycles all bits are internally cleared to zero. Since chip select must be LOW for the device to be reset, a global reset signal can be employed, with only selected devices being cleared at any given time.

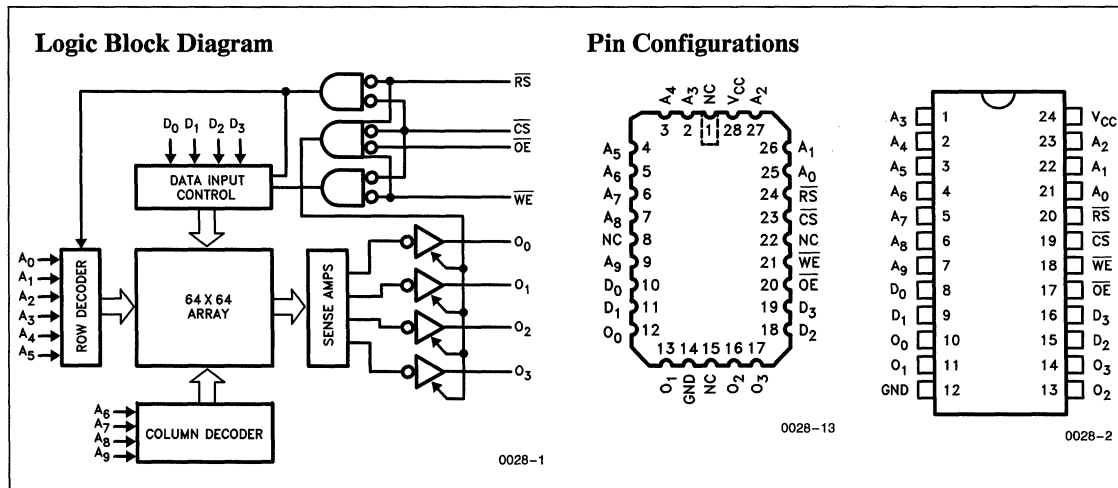
An active LOW write enable input (WE) controls the writing/reading op-

eration of the memory. When the chip select (CS) and write enable (WE) inputs are LOW, the information on the four data inputs D<sub>0</sub> to D<sub>3</sub> is written into the addressed memory location and the output circuitry is preconditioned so that the write data is present at the outputs when the write cycle is completed.

Reading is performed with the chip select (CS) input LOW, and the write enable (WE) input HIGH, and the output enable input (OE) LOW. The information stored in the addressed word is read out on the four non-inverting outputs O<sub>0</sub> to O<sub>3</sub>.

The outputs of the memory go to an active high impedance state whenever chip select (CS) is HIGH, Reset (RS) is LOW, output enable (OE) is HIGH, or during the writing operation when Write Enable (WE) is LOW.

A die coat is used to ensure alpha immunity.



**Selection Guide**

|                                |            | 7C150-12 | 7C150-15 | 7C150-25 | 7C150-35 |
|--------------------------------|------------|----------|----------|----------|----------|
| Maximum Access Time (ns)       | Commercial | 12       | 15       | 25       | 35       |
|                                | Military   |          | 15       | 25       | 35       |
| Maximum Operating Current (mA) | Commercial | 90       | 90       | 90       | 90       |
|                                | Military   |          | 100      | 100      | 100      |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied ..... -55°C to +125°C  
 Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs in High Z State ..... -0.5V to +7.0V  
 DC Input Voltage ..... -3.0V to +7.0V  
 Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... > 2001V (Per MIL-STD-883 Method 3015)  
 Latch-up Current ..... > 200 mA

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[4]</sup>

| Parameters       | Description                              | Test Conditions   | 7C150-12, 15, 25, 35 |                 | Units |
|------------------|--|---|----------------------|-----------------|-------|
|                  |  |   | Min.                 | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                      | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA         | 2.4                  |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                       | V <sub>CC</sub> = Min., I <sub>OL</sub> = 12.0 mA         |                      | 0.4             | V     |
| V <sub>IH</sub>  | Input High Voltage                       |   | 2.0                  | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input Low Voltage                        |   | -3.0                 | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current                       | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                    | -10                  | +10             | μA    |
| I <sub>IOZ</sub> | Output Leakage Current                   | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub><br>Output Disabled | -50                  | +50             | μA    |
| I <sub>OS</sub>  | Output Short <sup>[1]</sup>              | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND            |                      | -300            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA         | Commercial           | 90              | mA    |
|                  |  |   | Military*            | 100             |       |

\*-15, -25 and -35 only

### Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 7    | pF    |

**Notes:**

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

### AC Test Loads and Waveforms

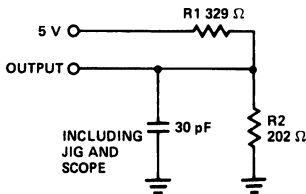


Figure 1a

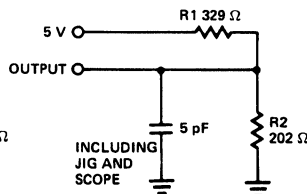


Figure 1b

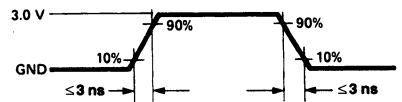
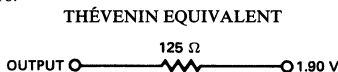


Figure 2. All Input Pulses

Equivalent To:



0028-4

0028-3

0028-5

**Switching Characteristics Over Operating Range<sup>[4, 5]</sup>**

| Parameters                       | Description   | 7C150-12 |      | 7C150-15 |      | 7C150-25 |      | 7C150-35 |      | Units |
|----------------------------------|---|----------|------|----------|------|----------|------|----------|------|-------|
|                                  |   | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.     | Max. |       |
| <b>READ CYCLE</b>                |   |          |      |          |      |          |      |          |      |       |
| t <sub>RC</sub>                  | Read Cycle Time   | 12       |      | 15       |      | 25       |      | 35       |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid                                   |          | 12   |          | 15   |          | 25   |          | 35   | ns    |
| t <sub>OHA</sub>                 | Output Hold from Address Change                         | 2        |      | 2        |      | 2        |      | 2        |      | ns    |
| t <sub>ACS</sub>                 | $\overline{\text{CS}}$ LOW to Data Valid                |          | 10   |          | 12   |          | 15   |          | 20   | ns    |
| t <sub> LZCS</sub>               | $\overline{\text{CS}}$ LOW to Low Z <sup>[7]</sup>      | 0        |      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub> HZCS</sub>               | $\overline{\text{CS}}$ HIGH to High Z <sup>[6, 7]</sup> |          | 8    | 0        | 11   | 0        | 20   | 0        | 25   | ns    |
| t <sub>DOE</sub>                 | $\overline{\text{OE}}$ LOW to Data Valid                |          | 8    |          | 10   |          | 15   |          | 20   | ns    |
| t <sub> LZOE</sub>               | $\overline{\text{OE}}$ LOW to Low Z <sup>[7]</sup>      | 0        |      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub> HZOE</sub>               | $\overline{\text{OE}}$ HIGH to High Z <sup>[6, 7]</sup> | 0        | 8    | 0        | 9    | 0        | 20   | 0        | 25   | ns    |
| <b>WRITE CYCLE<sup>[8]</sup></b> |   |          |      |          |      |          |      |          |      |       |
| t <sub>WC</sub>                  | Write Cycle Time  | 12       |      | 15       |      | 25       |      | 35       |      | ns    |
| t <sub>SCS</sub>                 | $\overline{\text{CS}}$ LOW to Write End                 | 8        |      | 11       |      | 15       |      | 20       |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End                             | 10       |      | 13       |      | 20       |      | 30       |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End                             | 2        |      | 2        |      | 5        |      | 5        |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                           | 2        |      | 2        |      | 5        |      | 5        |      | ns    |
| t <sub>PWE</sub>                 | $\overline{\text{WE}}$ Pulse Width                      | 8        |      | 11       |      | 15       |      | 20       |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End                                | 8        |      | 11       |      | 15       |      | 20       |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End                                | 2        |      | 2        |      | 5        |      | 5        |      | ns    |
| t <sub> LZWE</sub>               | $\overline{\text{WE}}$ HIGH to Low Z <sup>[7]</sup>     | 0        |      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub> HZWE</sub>               | $\overline{\text{WE}}$ LOW to High Z <sup>[6, 7]</sup>  | 0        | 8    | 0        | 12   | 0        | 20   | 0        | 25   | ns    |
| <b>RESET CYCLE</b>               |   |          |      |          |      |          |      |          |      |       |
| t <sub>RRC</sub>                 | Reset Cycle Time  | 24       |      | 30       |      | 50       |      | 70       |      | ns    |
| t <sub>SAR</sub>                 | Address Valid to Beginning of Reset                     | 0        |      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>SWER</sub>                | Write Enable HIGH to Beginning of Reset                 | 0        |      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>SCSR</sub>                | Chip Select LOW to Beginning of Reset                   | 0        |      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>PRS</sub>                 | Reset Pulse Width                                       | 12       |      | 15       |      | 20       |      | 30       |      | ns    |
| t <sub>HCSR</sub>                | Chip Select Hold after End of Reset                     | 0        |      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>HWER</sub>                | Write Enable Hold after End of Reset                    | 12       |      | 15       |      | 30       |      | 40       |      | ns    |
| t <sub>HAR</sub>                 | Address Hold after End of Reset                         | 12       |      | 15       |      | 30       |      | 40       |      | ns    |
| t <sub> LZRS</sub>               | Reset HIGH to Output in Low Z <sup>[7]</sup>            | 0        |      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub> HZRS</sub>               | Reset LOW to Output in High Z <sup>[6, 7]</sup>         | 0        | 8    | 0        | 12   | 0        | 20   | 0        | 25   | ns    |

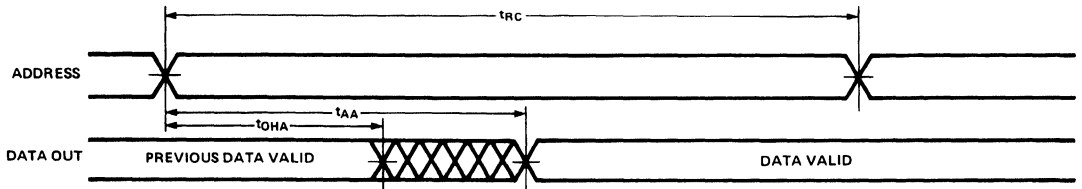
**Notes:**

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZCS</sub>, t<sub>HZOE</sub>, t<sub>HZR</sub> and t<sub>HZWE</sub> are tested with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> for any given device.

- The internal write time of the memory is defined by the overlap of  $\overline{\text{CS}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{\text{WE}}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{\text{CS}}$  and  $\overline{\text{OE}} = V_{\text{IL}}$ .
- Address valid prior to or coincident with  $\overline{\text{CS}}$  transition LOW.

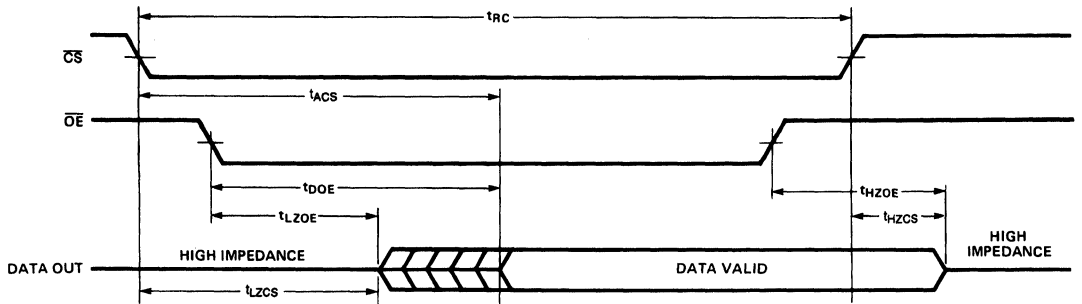
## Switching Waveforms

### Read Cycle No. 1 (Notes 9, 10)



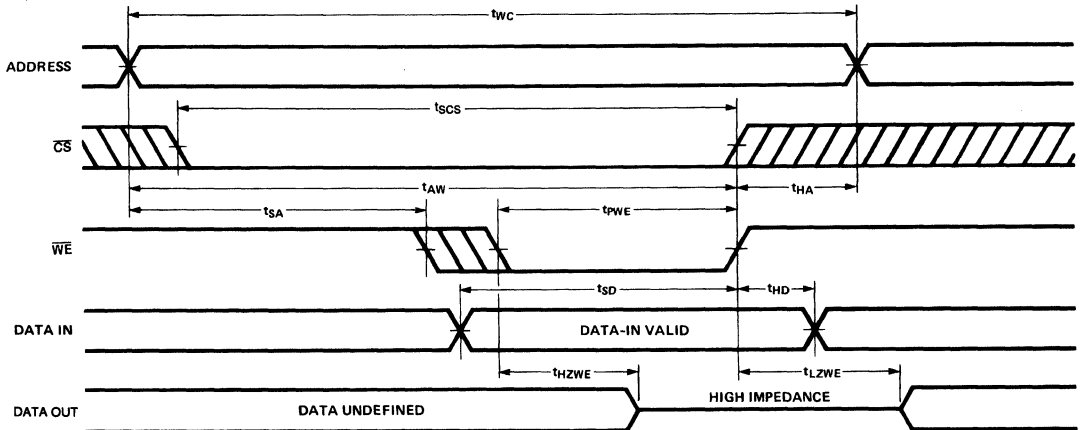
0028-6

### Read Cycle No. 2 (Notes 9, 11)



0028-8

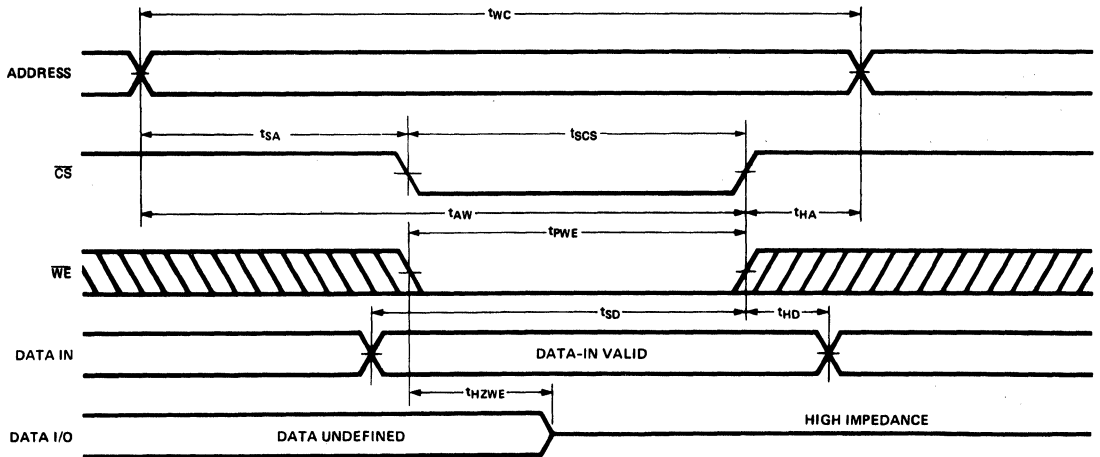
### Write Cycle No. 1 ( $\overline{WE}$ Controlled) (Note 8)



0028-9

### Switching Waveforms (Continued)

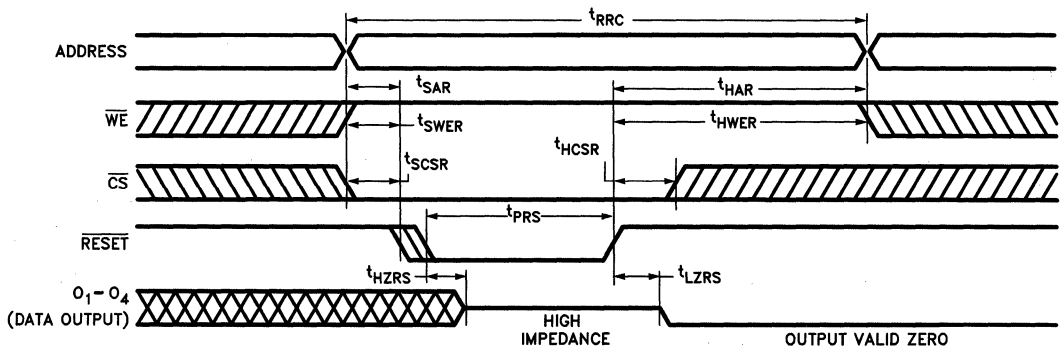
#### Write Cycle No. 2 ( $\overline{CS}$ Controlled) (Note 8)



0028-10

Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

#### Reset Cycle

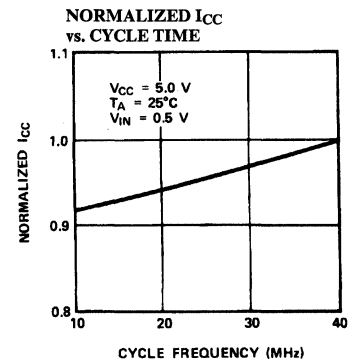
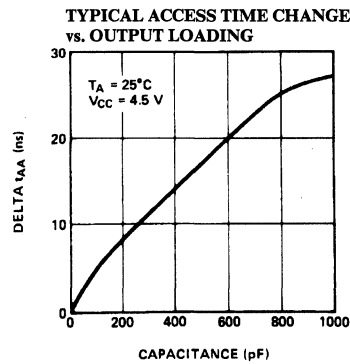
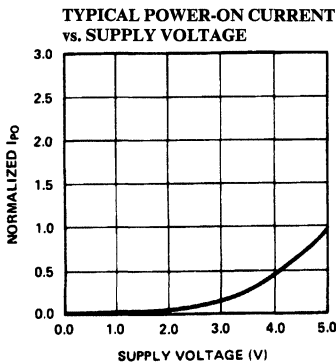
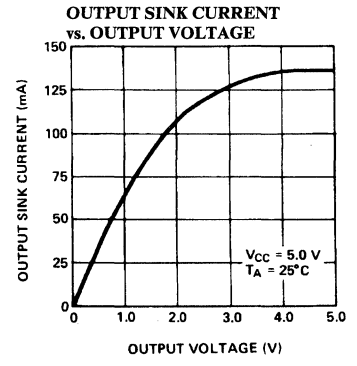
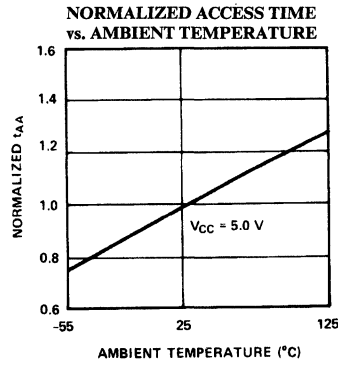
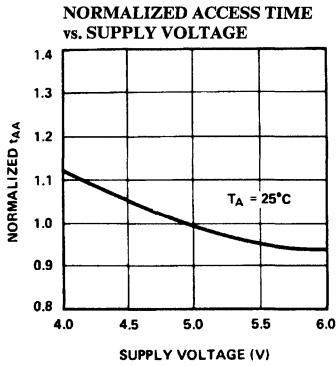
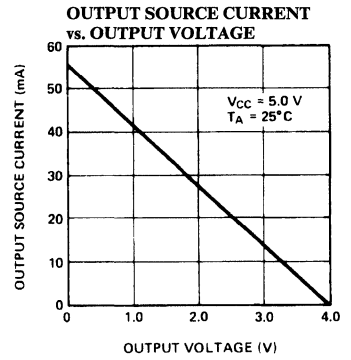
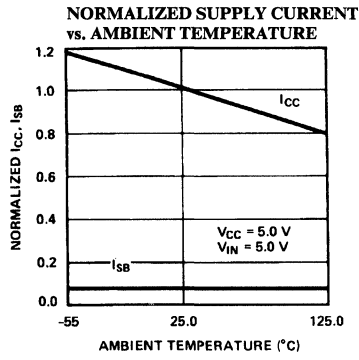
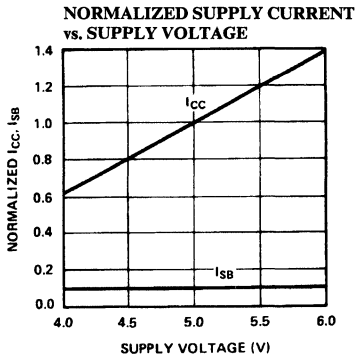


0028-11

Note: Reset cycle is defined by the overlap of  $\overline{RS}$  and  $\overline{CS}$  for the minimum reset pulse width.

Typical DC and AC Characteristics

2





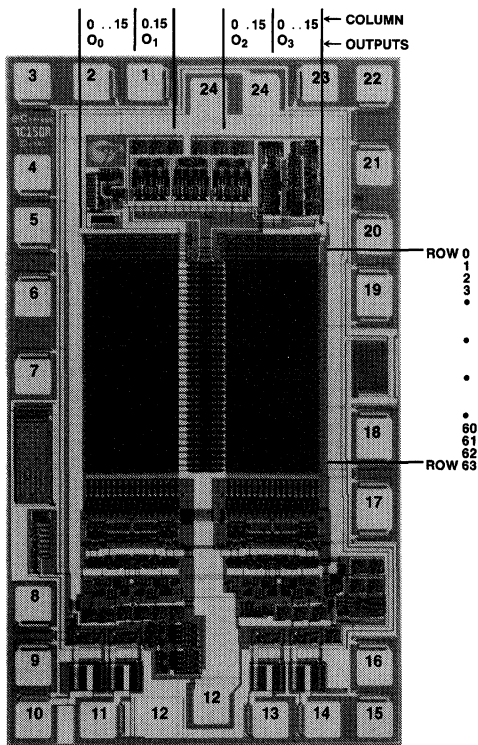
**Truth Table**

| Inputs |    |    |    | Outputs                        | Mode           |
|--------|----|----|----|--------------------------------|----------------|
| CS     | WE | OE | RS |                                |                |
| H      | X  | X  | X  | High Z                         | Not Selected   |
| L      | H  | X  | L  | High Z                         | Reset          |
| L      | L  | X  | H  | High Z                         | Write          |
| L      | H  | L  | H  | O <sub>0</sub> -O <sub>3</sub> | Read           |
| L      | X  | H  | H  | High Z                         | Output Disable |

**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 12         | CY7C150-12PC  | P13A         | Commercial      |
|            | CY7C150-12DC  | D14          |                 |
|            | CY7C150-12LC  | L54          |                 |
|            | CY7C150-12SC  | S13          |                 |
| 15         | CY7C150-15PC  | P13A         | Commercial      |
|            | CY7C150-15DC  | D14          |                 |
|            | CY7C150-15LC  | L54          |                 |
|            | CY7C150-15SC  | S13          |                 |
|            | CY7C150-15DMB | D14          | Military        |
|            | CY7C150-15LMB | L54          |                 |
| 25         | CY7C150-25PC  | P13A         | Commercial      |
|            | CY7C150-25DC  | D14          |                 |
|            | CY7C150-25LC  | L54          |                 |
|            | CY7C150-25SC  | S13          |                 |
|            | CY7C150-25DMB | D14          | Military        |
|            | CY7C150-25LMB | L54          |                 |
| 35         | CY7C150-35PC  | P13A         | Commercial      |
|            | CY7C150-35DC  | D14          |                 |
|            | CY7C150-35LC  | L54          |                 |
|            | CY7C150-35SC  | S13          |                 |
|            | CY7C150-35DMB | D14          | Military        |
|            | CY7C150-35LMB | L54          |                 |

**Bit Map**



**Address Designators**

| Address Name   | Address Function | Pin Number |
|----------------|------------------|------------|
| A <sub>0</sub> | X <sub>0</sub>   | 21         |
| A <sub>1</sub> | X <sub>1</sub>   | 22         |
| A <sub>2</sub> | X <sub>2</sub>   | 23         |
| A <sub>3</sub> | X <sub>3</sub>   | 1          |
| A <sub>4</sub> | X <sub>4</sub>   | 2          |
| A <sub>5</sub> | X <sub>5</sub>   | 3          |
| A <sub>6</sub> | Y <sub>0</sub>   | 4          |
| A <sub>7</sub> | Y <sub>1</sub>   | 5          |
| A <sub>8</sub> | Y <sub>2</sub>   | 6          |
| A <sub>9</sub> | Y <sub>3</sub>   | 7          |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**
**2**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL</sub> Max. | 1,2,3     |
| I <sub>FX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |

**Switching Characteristics**

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>ACS</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>SCS</sub>   | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |
| <b>RESET CYCLE</b> |             |
| t <sub>RRC</sub>   | 7,8,9,10,11 |
| t <sub>SAR</sub>   | 7,8,9,10,11 |
| t <sub>SWER</sub>  | 7,8,9,10,11 |
| t <sub>SCSR</sub>  | 7,8,9,10,11 |
| t <sub>PRS</sub>   | 7,8,9,10,11 |
| t <sub>HCSR</sub>  | 7,8,9,10,11 |
| t <sub>HWER</sub>  | 7,8,9,10,11 |
| t <sub>HAR</sub>   | 7,8,9,10,11 |

Document #: 38-00028-B



### Features

- Address and  $\overline{WE}$  registers
- CMOS for optimum speed/power
- High speed—20 ns
- Data In and Data Out latches
- TTL compatible inputs and outputs
- Self-timed write
- Capable of withstanding greater than 2001V electrostatic discharge
- Common I/O

### Functional Description

The CY7C157 is a high performance CMOS static RAM organized as 16,384 x 16 bits. It is intended specifically for use as a high speed cache memory device with the CY7C600 SPARC™ family of devices. The CY7C157 employs common I/O architecture, and a self timed byte-write mechanism.

Reading the device is accomplished by taking  $\overline{WE}$  HIGH, and  $\overline{OE}$  LOW. On the rising edge of CLOCK, addresses  $A_0$ – $A_{13}$  are loaded into the input registers. A memory access occurs, and data is held after a read cycle beyond the next rising edge of CLOCK in

order to meet the hold time requirements of the microprocessor.

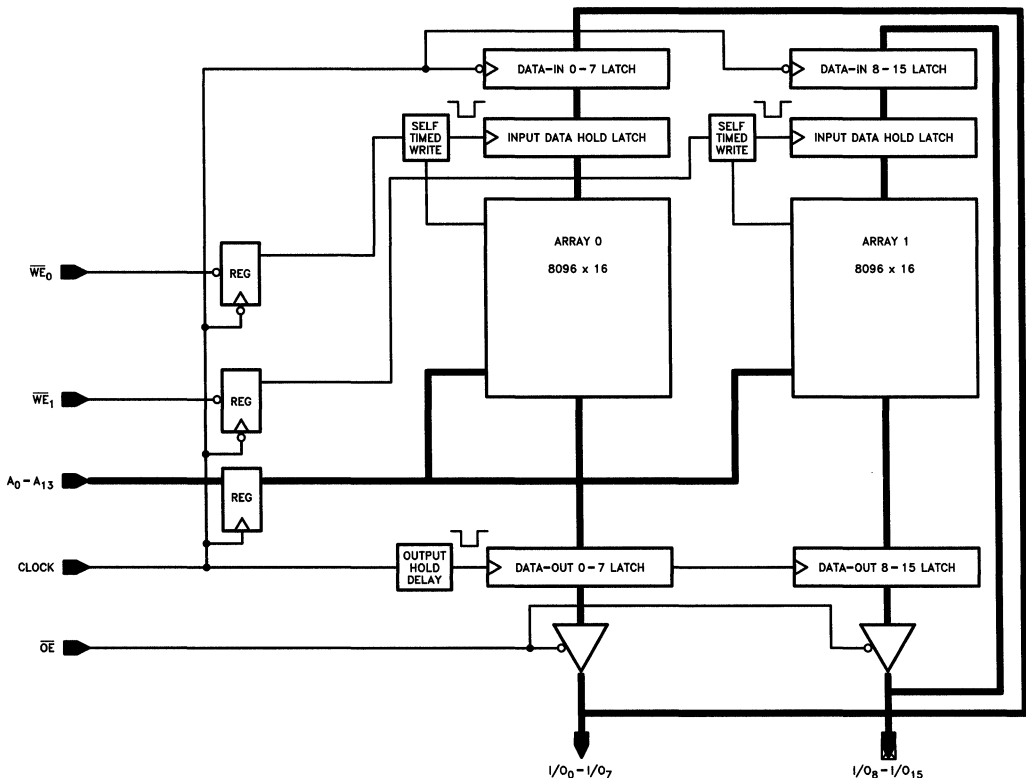
To write the device correctly,  $\overline{OE}$  must be taken HIGH. If the falling edge of CLOCK samples either or both of  $\overline{WE}_0$  or  $\overline{WE}_1$  LOW, a self timed byte write mechanism is triggered. Data is written from the data-in latch into the memory array at the corresponding address.

Note that the  $\overline{OE}$  signal must be HIGH for a proper write as the  $\overline{WE}_0$  and  $\overline{WE}_1$  signals do not tristate the outputs.

A die coat insures alpha immunity.

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### Logic Block Diagram



0153-1

**Selection Guide**

|   |            | 7C157-20 | 7C157-24 | 7C157-33 |
|---|------------|----------|----------|----------|
| Maximum Clock to Output (ns)              | Commercial | 20       | 24       | 33       |
|   | Military   |          | 24       | 33       |
| Maximum Output Enable to Output Time (ns) | Commercial | 8        | 10       | 15       |
|   | Military   |          | 10       | 15       |
| Maximum Current (mA)                      | Commercial | 250      | 250      | 250      |
|   | Military   |          | 300      | 300      |

**2**
**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential .... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Output Current into Outputs (LOW) ..... 50 mA

 Static Discharge Voltage ..... >2001V  
 (Per MIL-STD-883 Method 3015)

Latch-up Current ..... &gt;200 mA

**Operating Range**

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C        | 5V ± 10%        |
| Military   | -55°C to +125°C     | 5V ± 10%        |

**Electrical Characteristics Over Operating Range**

| Parameters      | Description                                 | Test Conditions  | 7C157-20   |                 | 7C157-24 |                 | 7C157-33 |                 | Units |
|-----------------|---|--|------------|-----------------|----------|-----------------|----------|-----------------|-------|
|                 |   |  | Min.       | Max.            | Min.     | Max.            | Min.     | Max.            |       |
| V <sub>OH</sub> | Output HIGH Voltage                         | V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA         | 2.4        |                 | 2.4      |                 | 2.4      |                 | V     |
| V <sub>OL</sub> | Output LOW Voltage                          | V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA          |            | 0.4             |          | 0.4             |          | 0.4             | V     |
| V <sub>IH</sub> | Input HIGH Voltage                          |  | 2.2        | V <sub>CC</sub> | 2.2      | V <sub>CC</sub> | 2.2      | V <sub>CC</sub> | V     |
| V <sub>IL</sub> | Input LOW Voltage                           |  | -3.0       | 0.8             | -3.0     | 0.8             | -3.0     | 0.8             | V     |
| I <sub>IX</sub> | Input Load Current                          | GND < V <sub>I</sub> < V <sub>CC</sub>                   | -10        | +10             | -10      | +10             | -10      | +10             | μA    |
| I <sub>OZ</sub> | Output Leakage Current                      | GND < V <sub>O</sub> < V <sub>CC</sub> , Output Disabled | -50        | +50             | -50      | +50             | -50      | +50             | μA    |
| I <sub>OS</sub> | Output Short Circuit Current <sup>[1]</sup> | V <sub>CC</sub> = Max, V <sub>OUT</sub> = GND            |            | -350            |          | -350            |          | -350            | mA    |
| I <sub>CC</sub> | V <sub>CC</sub> Operating Supply Current    | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA        | Commercial | 250             |          | 250             |          | 250             | mA    |
|                 |   |  | Military   |                 |          | 300             |          | 300             |       |

**Capacitance [2]**

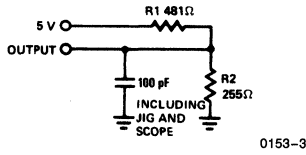
| Parameters       | Description        | Test Conditions   | Max. | Units |
|------------------|--------------------|---|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V <sup>[3]</sup> | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |   | 8    |       |

**Notes:**

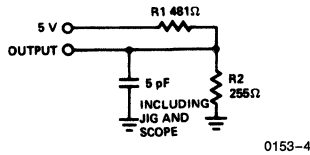
1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

2. Tested initially and after any design or process changes that may affect these parameters.

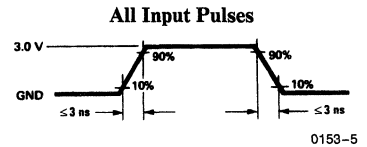
 3. T<sub>A</sub> is the "instant on" case temperature.

**AC Test Loads and Waveforms**

**Figure 1a**

0153-3

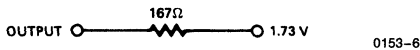

**Figure 1b**

0153-4


**Figure 2**

0153-5

Equivalent to: THÉVENIN EQUIVALENT



0153-6

**Switching Characteristics Over Operating Range [4, 5]**

| Parameters              | Description  | 7C157-20[6] |      | 7C157-24[6] |      | 7C157-33 |      | Units |
|-------------------------|--|-------------|------|-------------|------|----------|------|-------|
|                         |  | Min.        | Max. | Min.        | Max. | Min.     | Max. |       |
| <b>READ CYCLE[7, 8]</b> |  |             |      |             |      |          |      |       |
| t <sub>CHCH</sub>       | Clock Cycle Time                                   |             | 25   |             | 30   |          | 40   | ns    |
| t <sub>CHQV</sub>       | Clock HIGH to Output Valid                         |             | 20   |             | 24   |          | 33   | ns    |
| t <sub>CHQX</sub>       | Output Data Hold                                   | 5           |      | 5           |      | 5        |      | ns    |
| t <sub>GLQV</sub>       | $\overline{\text{OE}}$ LOW to Output Valid         |             | 8    |             | 10   |          | 15   | ns    |
| t <sub>GHQZ</sub>       | $\overline{\text{OE}}$ HIGH to Output Tristate     |             | 8    |             | 10   |          | 15   | ns    |
| t <sub>GHCH</sub>       | $\overline{\text{OE}}$ HIGH to Next Clock HIGH     | 7           |      | 7           |      | 7        |      | ns    |
| t <sub>AVCH</sub>       | Address Setup                                      | 2           |      | 2           |      | 3        |      | ns    |
| t <sub>CHAX</sub>       | Address Hold                                       | 6           |      | 6           |      | 6        |      | ns    |
| <b>WRITE CYCLE[9]</b>   |  |             |      |             |      |          |      |       |
| t <sub>GHQZ</sub>       | $\overline{\text{OE}}$ HIGH to Output Tristate[10] |             | 8    |             | 10   |          | 15   | ns    |
| t <sub>GHCH</sub>       | $\overline{\text{OE}}$ HIGH to Next Clock HIGH     | 7           |      | 7           |      | 7        |      | ns    |
| t <sub>DVCL</sub>       | Data in Setup to Clock                             | 6           |      | 6           |      | 7        |      | ns    |
| t <sub>CLDX</sub>       | Data in Hold from Clock                            | 2           |      | 2           |      | 2        |      | ns    |
| t <sub>WLCL</sub>       | $\overline{\text{WE}}_X$ LOW to Clock LOW[12, 13]  | 4           |      | 4           |      | 6        |      | ns    |
| t <sub>CLWH</sub>       | Clock LOW to $\overline{\text{WE}}_X$ HIGH[12, 13] | 3           |      | 3           |      | 3        |      | ns    |
| t <sub>AVCH</sub>       | Address Setup                                      | 2           |      | 2           |      | 3        |      | ns    |
| t <sub>CHAX</sub>       | Address Hold                                       | 6           |      | 6           |      | 6        |      | ns    |

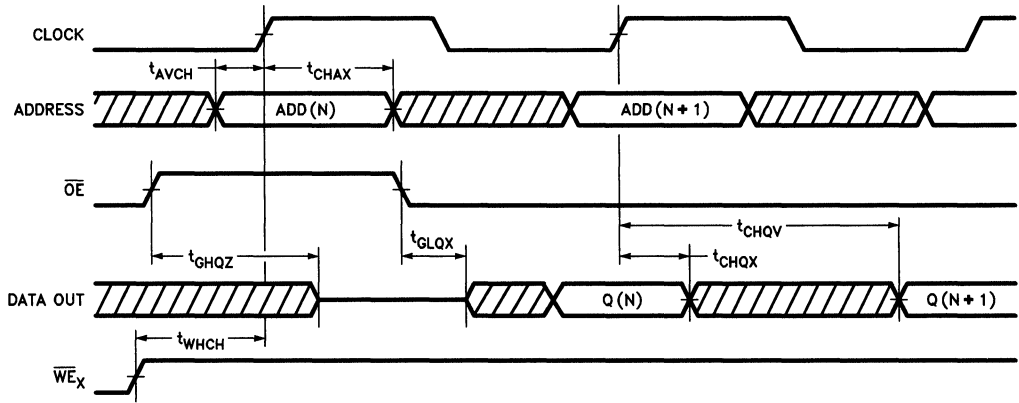
**Notes:**

- See the last page of this specification for Group A subgroup testing information.
- Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 100 pF load capacitance.
- Surface mount package only.
- WE is HIGH for read cycle.
- OE is selected (LOW).
- OE must be high for data-in to propagate to latch.
- t<sub>GHQZ</sub> is specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- Self Timed Write is triggered on falling edge of either  $\overline{\text{WE}}_0$  or  $\overline{\text{WE}}_1$ .
- X = 0 or 1 for low byte and high byte, respectively.
- Self Timed Write is triggered on falling edge of registered  $\overline{\text{WE}}_0$  or  $\overline{\text{WE}}_1$  signals.

## Switching Waveforms

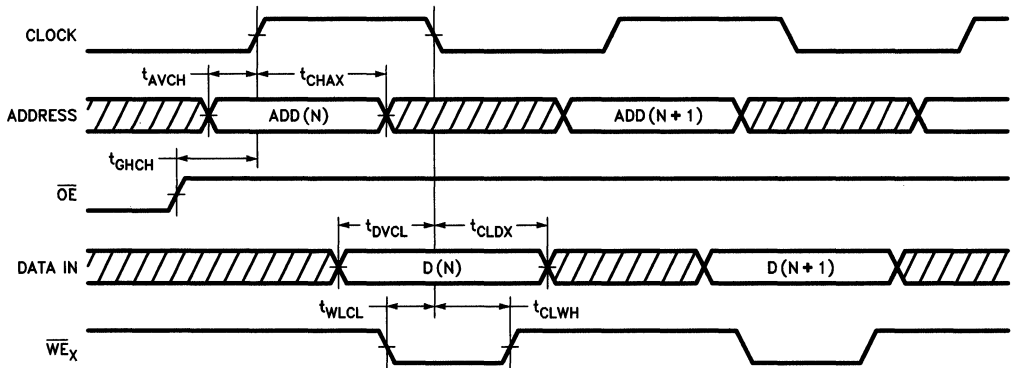
### Read Cycle

2



0153-7

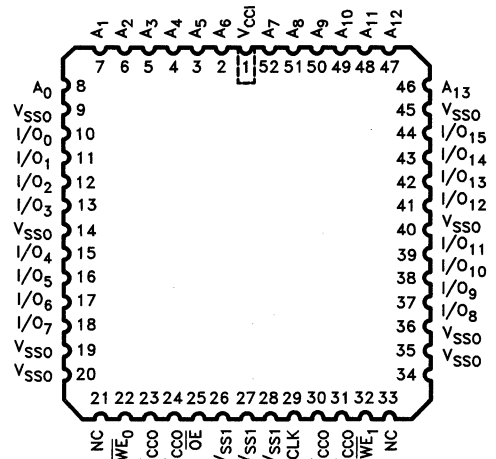
### Write Cycle



0153-8

**Pin Timing Cross Reference**

| Pin Name  | Timing Reference | Description    |
|---|------------------|----------------|
| Clock   | C                | Clock Inputs   |
| A <sub>0</sub> -A <sub>13</sub>                           | A                | Address Inputs |
| I/O <sub>0</sub> -I/O <sub>15</sub> (Input)               | D                | Data Inputs    |
| I/O <sub>0</sub> -I/O <sub>15</sub> (Output)              | Q                | Data Outputs   |
| $\overline{WE}_0$ , $\overline{WE}_1$ , $\overline{WE}_X$ | W                | Write Enable   |
| $\overline{OE}$   | G                | Output Enable  |

**Pin Configuration**

**PLCC  
Top View**

0153-2

**Truth Table**

| Inputs          |                             |                             | Outputs                             |
|-----------------|-----------------------------|-----------------------------|-------------------------------------|
| $\overline{OE}$ | $\overline{WE}_0$ (↓ CLOCK) | $\overline{WE}_1$ (↓ CLOCK) |                                     |
| X               | X                           | X                           | High Z                              |
| H               | H                           | H                           | High Z                              |
| L               | H                           | H                           | I/O <sub>0</sub> -I/O <sub>15</sub> |
| H               | L                           | H                           | I/O <sub>0</sub> -I/O <sub>7</sub>  |
| H               | H                           | L                           | I/O <sub>8</sub> -I/O <sub>15</sub> |
| H               | L                           | L                           | I/O <sub>0</sub> -I/O <sub>15</sub> |

**Notes:**

14. Data In latch is transparent when clock ↑ HIGH.  
 15. Data In latch is closed when clock ↓ LOW.

**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 20         | CY7C157-20LC  | L69          | Commercial      |
|            | CY7C157-20JC  | J69          |                 |
| 24         | CY7C157-24LC  | L69          | Military        |
|            | CY7C157-24JC  | J69          |                 |
|            | CY7C157-24LMB | L69          |                 |
| 33         | CY7C157-33LC  | L69          | Commercial      |
|            | CY7C157-33JC  | J69          |                 |
|            | CY7C157-33LMB | L69          | Military        |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL</sub> Max. | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>OS</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |

**2**
**Switching Characteristics**

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>CHCH</sub>  | 7,8,9,10,11 |
| t <sub>CHQV</sub>  | 7,8,9,10,11 |
| t <sub>GHQZ</sub>  | 7,8,9,10,11 |
| t <sub>CHQX</sub>  | 7,8,9,10,11 |
| t <sub>GHQV</sub>  | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>CHCH</sub>  | 7,8,9,10,11 |
| t <sub>DVCL</sub>  | 7,8,9,10,11 |
| t <sub>AVCH</sub>  | 7,8,9,10,11 |
| t <sub>CHAX</sub>  | 7,8,9,10,11 |
| t <sub>CLDX</sub>  | 7,8,9,10,11 |
| t <sub>DVWL</sub>  | 7,8,9,10,11 |
| t <sub>WLDX</sub>  | 7,8,9,10,11 |

Document #: 38-00098





16,384 x 4 Static RAM  
Separate I/O

Features

- Automatic power-down when deselected
- Transparent Write (7C161)
- CMOS for optimum speed/power
- High speed  
— 10 ns  $t_{AA}$
- Low active power  
— 525 mW at 40 MHz
- Low standby power  
— 150 mW
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C161 and CY7C162 are high performance CMOS static RAMs organized as 16,384 x 4 bits with separate I/O. These RAMs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor. Easy memory expansion is provided by active LOW chip enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ ) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 75% when deselected.

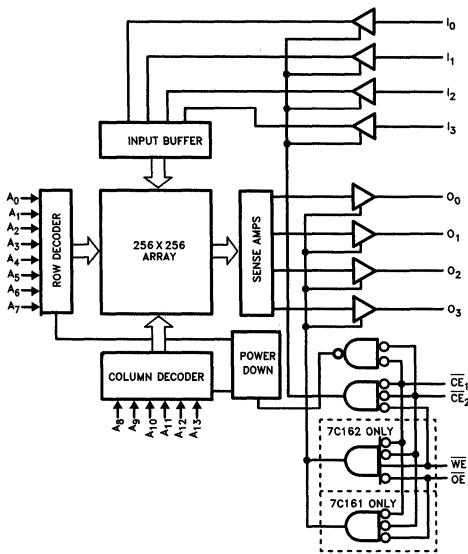
Writing to the device is accomplished when the chip enable ( $\overline{CE}_1$ ,  $\overline{CE}_2$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the four input pins

( $I_0$  through  $I_3$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{13}$ ).

Reading the device is accomplished by taking the chip enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ ) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

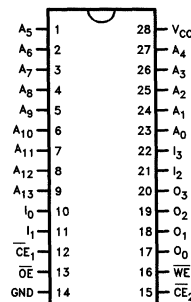
The output pins stay in high impedance state when write enable ( $\overline{WE}$ ) is LOW (7C162 only), or one of the chip enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ ) are HIGH.

Logic Block Diagram

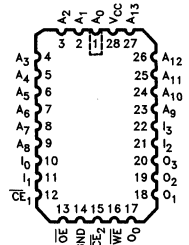


0152-1

Pin Configurations



0152-2



0152-3

Selection Guide

|                                |            | 7C161-10<br>7C162-10 | 7C161-12<br>7C162-12 | 7C161-15<br>7C162-15 |
|--------------------------------|------------|----------------------|----------------------|----------------------|
| Maximum Access Time (ns)       |            | 10                   | 12                   | 15                   |
| Maximum Operating Current (mA) | Commercial | 125                  | 120                  | 115                  |
|                                | Military   |                      | 150                  | 135                  |
| Maximum Standby Current (mA)   | Commercial | 30                   | 30                   | 30                   |
|                                | Military   |                      | 50                   | 50                   |

### Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature                                   | -65°C to +150°C |
| Ambient Temperature with Power Applied                | -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 24 to Pin 12) | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State         | -0.5V to +7.0V  |
| Input Voltage <sup>[14]</sup>                         | -3.0V to +7.0V  |
| Output Current into Outputs (Low)                     | 20 mA           |

Static Discharge Voltage > 2001V  
(Per MIL-STD-883 Method 3015)

Latch-up Current > 200 mA

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[4]</sup>

| Parameters       | Description                                  | Test Conditions  | 7C161-10<br>7C162-10 |                 | 7C161-12<br>7C162-12 |                 | 7C161-15<br>7C162-15 |                 | Units |
|------------------|--|--|----------------------|-----------------|----------------------|-----------------|----------------------|-----------------|-------|
|                  |  |  | Min.                 | Max.            | Min.                 | Max.            | Min.                 | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA                            | 2.4                  |                 | 2.4                  |                 | 2.4                  |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA                             |                      | 0.4             |                      | 0.4             |                      | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                           |  | 2.2                  | V <sub>CC</sub> | 2.2                  | V <sub>CC</sub> | 2.2                  | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage <sup>[14]</sup>            |  | -0.5                 | 0.8             | -0.5                 | 0.8             | -0.5                 | 0.8             | V     |
| I <sub>Ix</sub>  | Input Load Current                           | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                                       | -10                  | +10             | -10                  | +10             | -10                  | +10             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                       | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> ,<br>Output Dsbl'd.                   | -10                  | +10             | -10                  | +10             | -10                  | +10             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>  | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND                               |                      | -350            |                      | -350            |                      | -350            | mA    |
| I <sub>CC1</sub> | Automatic $\overline{CE}$ Power Down Current | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA<br>f = 40 MHz              | Commercial           | 105             |                      | 105             |                      | 105             | mA    |
|                  |  |  | Military             |                 |                      | 130             |                      | 130             |       |
| I <sub>CC2</sub> | V <sub>CC</sub> Operating Supply Current     | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA<br>f = f max.              | Commercial           | 125             |                      | 120             |                      | 115             | mA    |
|                  |  |  | Military             |                 |                      | 150             |                      | 135             |       |
| I <sub>SB</sub>  | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$<br>Min. Duty Cycle = 100% | Commercial           | 30              |                      | 30              |                      | 30              | mA    |
|                  |  |  | Military             |                 |                      | 50              |                      | 50              |       |

### Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions  | Max. <sup>[13]</sup> | Units |
|------------------|--------------------|--|----------------------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 5                    | pF    |
| C <sub>OUT</sub> | Output Capacitance | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 7                    | pF    |

#### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

### AC Test Loads and Waveforms

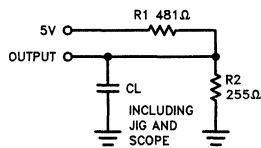


Figure 1a

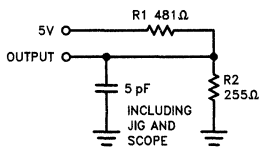


Figure 1b

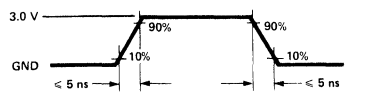
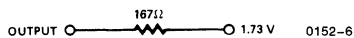


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over Operating Range<sup>[4, 5, 12]</sup>

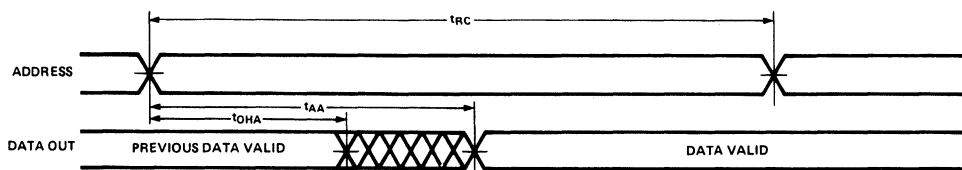
| Parameters                       | Description   | 7C161-10<br>7C162-10 |      | 7C161-12<br>7C162-12 |      | 7C161-15<br>7C162-15 |      | Units |
|----------------------------------|---|----------------------|------|----------------------|------|----------------------|------|-------|
|                                  |   | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. |       |
| <b>READ CYCLE</b>                |   |                      |      |                      |      |                      |      |       |
| t <sub>RC</sub>                  | Read Cycle Time   | 10                   |      | 12                   |      | 15                   |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid                                   |                      | 10   |                      | 12   |                      | 15   | ns    |
| t <sub>OHA</sub>                 | Output Hold from Address Change                         | 2                    |      | 3                    |      | 3                    |      | ns    |
| t <sub>ACE</sub>                 | $\overline{CE}$ LOW to Data Valid                       |                      | 10   |                      | 12   |                      | 15   | ns    |
| t <sub>LZCE</sub>                | $\overline{CE}$ LOW to Low Z <sup>[7]</sup>             | 2                    |      | 3                    |      | 3                    |      | ns    |
| t <sub>HZCE</sub>                | $\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>        |                      | 6    |                      | 8    |                      | 8    | ns    |
| t <sub>DOE</sub>                 | $\overline{OE}$ LOW to Data Valid                       |                      | 8    |                      | 10   |                      | 10   | ns    |
| t <sub>LZOE</sub>                | $\overline{OE}$ LOW to LOW Z                            | 2                    |      | 3                    |      | 2                    |      | ns    |
| t <sub>HZOE</sub>                | $\overline{OE}$ HIGH to HIGH Z                          |                      | 6    |                      | 8    |                      | 8    | ns    |
| t <sub>PU</sub>                  | $\overline{CE}$ LOW to Power Up                         | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>PD</sub>                  | $\overline{CE}$ HIGH to Power Down                      |                      | 10   |                      | 12   |                      | 15   | ns    |
| <b>WRITE CYCLE<sup>[8]</sup></b> |   |                      |      |                      |      |                      |      |       |
| t <sub>WC</sub>                  | Write Cycle Time  | 10                   |      | 12                   |      | 15                   |      | ns    |
| t <sub>SCE</sub>                 | $\overline{CE}$ LOW to Write End                        | 8                    |      | 10                   |      | 12                   |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End                             | 8                    |      | 10                   |      | 12                   |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End                             | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                           | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>PWE</sub>                 | $\overline{WE}$ Pulse Width                             | 8                    |      | 10                   |      | 12                   |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End                                | 8                    |      | 10                   |      | 10                   |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End                                | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>LZWE</sub>                | $\overline{WE}$ HIGH to Low Z <sup>[7]</sup> (7C162)    | 3                    |      | 5                    |      | 5                    |      | ns    |
| t <sub>HZWE</sub>                | $\overline{WE}$ LOW to High Z <sup>[6, 7]</sup> (7C162) |                      | 5    |                      | 7    |                      | 7    | ns    |
| t <sub>AWE</sub>                 | $\overline{WE}$ LOW to Data Valid (7C161)               |                      | 10   |                      | 12   |                      | 15   | ns    |
| t <sub>ADV</sub>                 | Data Valid to Output Valid (7C161)                      |                      | 10   |                      | 12   |                      | 15   | ns    |

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and C<sub>L</sub> = 30 pF load capacitance for 15 ns t<sub>AA</sub> devices and C<sub>L</sub> = 20 pF load capacitance for 10 ns and 12 ns t<sub>AA</sub> devices.
- t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$ ,  $\overline{CE}_2$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CE}_1$ ,  $\overline{CE}_2 = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{CE}_1$ ,  $\overline{CE}_2$  transition LOW.
- Both  $\overline{CE}_1$  and  $\overline{CE}_2$  are represented by  $\overline{CE}$  in the Switching Characteristics and Waveforms.
- For all packages except cerdip (D22) which has maximums of C<sub>JN</sub> = 10 pF, C<sub>OUT</sub> = 12 pF.
- V<sub>IL</sub> (min.) = -3.0V for pulse width < 20 ns.

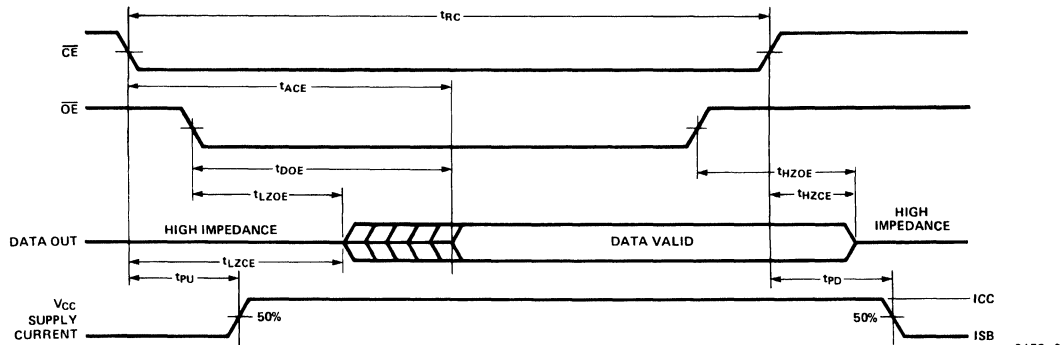
Switching Waveforms<sup>[12]</sup>

Read Cycle No. 1<sup>[9, 10]</sup>



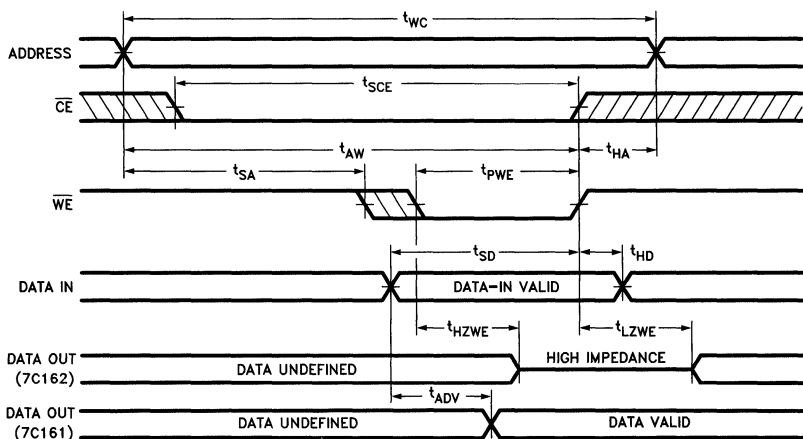
### Switching Waveforms<sup>[12]</sup> (Continued)

#### Read Cycle<sup>[9, 11]</sup>



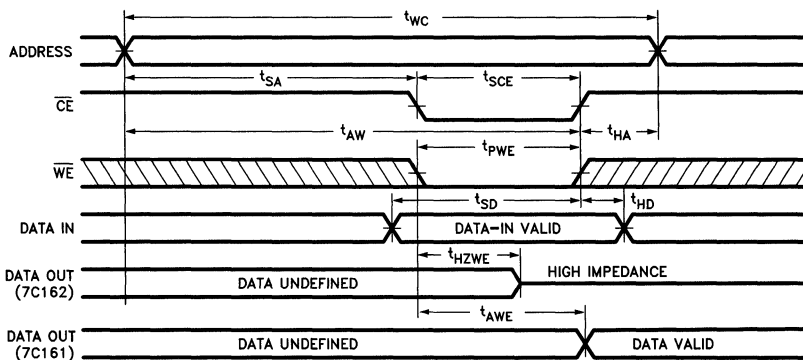
0152-8

#### Write Cycle No. 1 ( $\overline{WE}$ Controlled)<sup>[8]</sup>



0152-9

#### Write Cycle No. 2 ( $\overline{CE}$ Controlled)<sup>[8]</sup>



0152-10

Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state (7C162 only).

**Truth Tables**
**CY7C161**

| CE <sub>1</sub> | CE <sub>2</sub> | WE | OE | Output   | Input   | Mode                |
|-----------------|-----------------|----|----|----------|---------|---------------------|
| H               | X               | X  | X  | High Z   | X       | Deselect Power Down |
| X               | H               | X  | X  | High Z   | X       | Deselect Power Down |
| L               | L               | H  | L  | Data Out | X       | Read                |
| L               | L               | L  | X  | High Z   | Data In | Write               |
| L               | L               | H  | H  | High Z   | X       | Deselect            |

**CY7C162**

| CE <sub>1</sub> | CE <sub>2</sub> | WE | OE | Output   | Input   | Mode                |
|-----------------|-----------------|----|----|----------|---------|---------------------|
| H               | X               | X  | X  | High Z   | X       | Deselect Power Down |
| X               | H               | X  | X  | High Z   | X       | Deselect Power Down |
| L               | L               | H  | L  | Data Out | X       | Read                |
| L               | L               | L  | L  | Data In  | Data In | Write               |
| L               | L               | L  | H  | High Z   | Data In | Write               |
| L               | L               | H  | H  | High Z   | X       | Deselect            |

**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 10         | CY7C161-10VC  | V21          | Commercial      |
|            | CY7C161-10LC  | L54          |                 |
| 12         | CY7C161-12PC  | P21          | Commercial      |
|            | CY7C161-12VC  | V21          |                 |
|            | CY7C161-12DC  | D22          |                 |
|            | CY7C161-12LC  | L54          |                 |
|            | CY7C161-12DMB | D22          | Military        |
|            | CY7C161-12LMB | L54          |                 |
| 15         | CY7C161-15PC  | P21          | Commercial      |
|            | CY7C161-15VC  | V21          |                 |
|            | CY7C161-15DC  | D22          |                 |
|            | CY7C161-15LC  | L54          |                 |
|            | CY7C161-15DMB | D22          | Military        |
|            | CY7C161-15LMB | L54          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 10         | CY7C162-10VC  | V21          | Commercial      |
|            | CY7C162-10LC  | L54          |                 |
| 12         | CY7C162-12PC  | P21          | Commercial      |
|            | CY7C162-12VC  | V21          |                 |
|            | CY7C162-12DC  | D22          |                 |
|            | CY7C162-12LC  | L54          |                 |
|            | CY7C162-12DMB | D22          | Military        |
|            | CY7C162-12LMB | L54          |                 |
| 15         | CY7C162-15PC  | P21          | Commercial      |
|            | CY7C162-15VC  | V21          |                 |
|            | CY7C162-15DC  | D22          |                 |
|            | CY7C162-15LC  | L54          |                 |
|            | CY7C162-15DMB | D22          | Military        |
|            | CY7C162-15LMB | L54          |                 |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB</sub>      | 1,2,3     |

**2**
**Switching Characteristics**

| Parameters           | Subgroups   |
|----------------------|-------------|
| <b>READ CYCLE</b>    |             |
| t <sub>AA</sub>      | 7,8,9,10,11 |
| t <sub>OHA</sub>     | 7,8,9,10,11 |
| t <sub>ACE</sub>     | 7,8,9,10,11 |
| t <sub>DOE</sub>     | 7,8,9,10,11 |
| <b>WRITE CYCLE</b>   |             |
| t <sub>SCE</sub>     | 7,8,9,10,11 |
| t <sub>AW</sub>      | 7,8,9,10,11 |
| t <sub>HA</sub>      | 7,8,9,10,11 |
| t <sub>SA</sub>      | 7,8,9,10,11 |
| t <sub>PWE</sub>     | 7,8,9,10,11 |
| t <sub>SD</sub>      | 7,8,9,10,11 |
| t <sub>HD</sub>      | 7,8,9,10,11 |
| t <sub>AWE</sub> [1] | 7,8,9,10,11 |
| t <sub>ADV</sub> [1] | 7,8,9,10,11 |

**Note:**

1. 7C161 only.

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**Features**

- Automatic power-down when deselected
- Transparent Write (7C161)
- CMOS for optimum speed/power
- High speed  
— 20 ns  $t_{AA}$
- Low active power  
— 275 mW
- Low standby power  
— 110 mW
- TTL compatible inputs and outputs

- Capable of withstanding greater than 2001V electrostatic discharge

**Functional Description**

The CY7C161 and CY7C162 are high performance CMOS static RAMs organized as 16,384 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ ) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 60% when deselected.

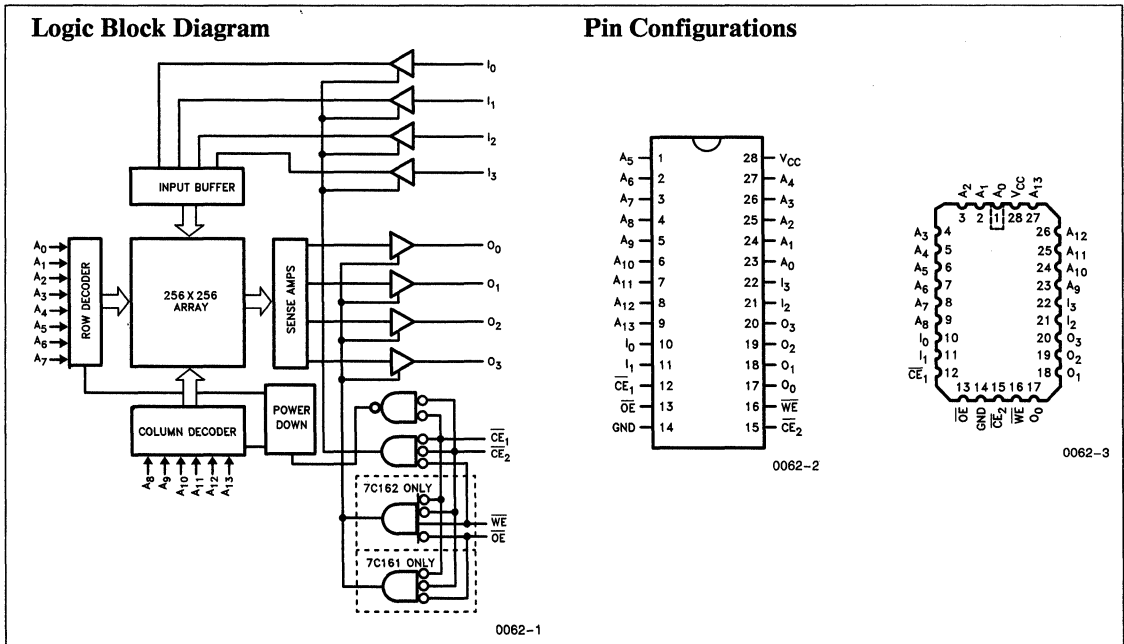
Writing to the device is accomplished when the chip enable ( $\overline{CE}_1$ ,  $\overline{CE}_2$ ) and write enable ( $\overline{WE}$ ) inputs are both

LOW. Data on the four input pins ( $I_0$  through  $I_3$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{13}$ ).

Reading the device is accomplished by taking the chip enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ ) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

The output pins stay in high impedance state when write enable ( $\overline{WE}$ ) is LOW (7C162 only), or one of the chip enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ ) are HIGH.

A die coat is used to insure alpha immunity.



**Selection Guide**

|                                |            | 7C161-20<br>7C162-20 | 7C161-25<br>7C162-25 | 7C161-35<br>7C162-35 | 7C161-45<br>7C162-45 |
|--------------------------------|------------|----------------------|----------------------|----------------------|----------------------|
| Maximum Access Time (ns)       |            | 20                   | 25                   | 35                   | 45                   |
| Maximum Operating Current (mA) | Commercial | 80                   | 70                   | 70                   | 50                   |
|                                | Military   |                      | 80                   | 70                   | 70                   |
| Maximum Standby Current (mA)   | Commercial | 40/20                | 20/20                | 20/20                | 20/20                |
|                                | Military   |                      | 40/20                | 20/20                | 20/20                |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature .....                                   | -65°C to +150°C |
| Ambient Temperature with Power Applied .....                | -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State .....         | -0.5V to +7.0V  |
| DC Input Voltage .....                                      | -3.0V to +7.0V  |
| Output Current into Outputs (Low) .....                     | 20 mA           |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | > 2001V<br>(Per MIL-STD-883 Method 3015) |
| Latch-up Current .....         | > 200 mA                                 |

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[4]</sup>

| Parameters       | Description                                  | Test Conditions   | 7C161-20 |                 | 7C161-25, 35 |                 | 7C161-45 |                 | Units |
|------------------|--|---|----------|-----------------|--------------|-----------------|----------|-----------------|-------|
|                  |  |   | 7C162-20 | 7C162-25, 35    | 7C162-25, 35 | 7C162-45        |          |                 |       |
|                  |  |   | Min.     | Max.            | Min.         | Max.            | Min.     | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA   | 2.4      |                 | 2.4          |                 | 2.4      |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA  |          | 0.4             |              | 0.4             |          | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                           |   | 2.2      | V <sub>CC</sub> | 2.2          | V <sub>CC</sub> | 2.2      | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage <sup>[4A]</sup>            |   | -3.0     | 0.8             | -3.0         | 0.8             | -3.0     | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current                           | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>  | -10      | +10             | -10          | +10             | -10      | +10             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                       | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Dsbl'd.   | -10      | +10             | -10          | +10             | -10      | +10             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>  | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND  |          | -350            |              | -350            |          | -350            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current     | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA   | Coml.    |                 | 80           | 70              | 50       | mA              |       |
|                  |  |   | Mil.     | 25              |              | 80              | 70       |                 |       |
|                  |  |   |          | 35              |              | 70              |          |                 |       |
| I <sub>SB1</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$<br>Min. Duty Cycle = 100%  | Coml.    |                 | 40           | 20              | 20       | mA              |       |
|                  |  |   | Mil.     | 25              |              | 40              | 20       |                 |       |
|                  |  |   |          | 35              |              | 20              |          |                 |       |
| I <sub>SB2</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> ,<br>$\overline{CE} \geq V_{CC} - 0.3V$<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V | Coml.    |                 | 20           | 20              | 20       | mA              |       |
|                  |  |   | Mil.     |                 |              | 20              | 20       |                 |       |

### Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 7    | pF    |

#### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- 4A. V<sub>IL</sub> min. = -3.0V for pulse durations less than 30 ns.

### AC Test Loads and Waveforms

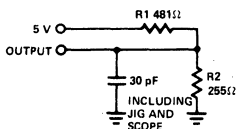


Figure 1a

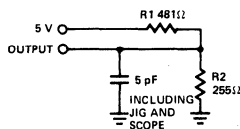


Figure 1b

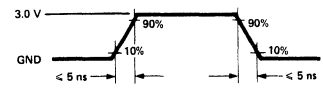


Figure 2

0062-4

0062-6

Equivalent to:

THÉVENIN EQUIVALENT



0062-5



### Switching Characteristics Over Operating Range<sup>[4, 5, 12]</sup>

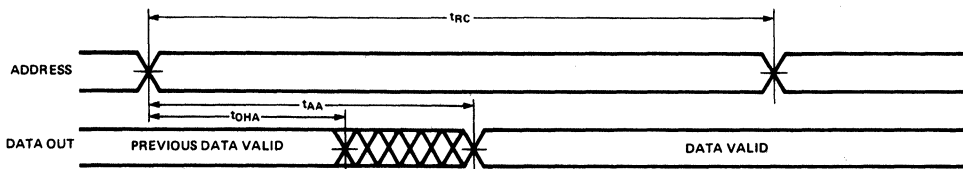
| Parameters                       | Description   | 7C161-20<br>7C162-20 |      | 7C161-25<br>7C162-25 |      | 7C161-35<br>7C162-35 |      | 7C161-45<br>7C162-45 |      | Units |
|----------------------------------|---|----------------------|------|----------------------|------|----------------------|------|----------------------|------|-------|
|                                  |   | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. |       |
| <b>READ CYCLE</b>                |   |                      |      |                      |      |                      |      |                      |      |       |
| t <sub>RC</sub>                  | Read Cycle Time   | 20                   |      | 25                   |      | 35                   |      | 45                   |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid                                   |                      | 20   |                      | 25   |                      | 35   |                      | 45   | ns    |
| t <sub>OHA</sub>                 | Output Hold from Address Change                         | 5                    |      | 5                    |      | 5                    |      | 5                    |      | ns    |
| t <sub>ACE</sub>                 | $\overline{CE}$ LOW to Data Valid                       |                      | 20   |                      | 25   |                      | 35   |                      | 45   | ns    |
| t <sub>LZCE</sub>                | $\overline{CE}$ LOW to Low Z <sup>[7]</sup>             | 5                    |      | 5                    |      | 5                    |      | 5                    |      | ns    |
| t <sub>HZCE</sub>                | $\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>        |                      | 8    |                      | 10   |                      | 15   |                      | 15   | ns    |
| t <sub>DOE</sub>                 | $\overline{OE}$ LOW to Data Valid                       |                      | 10   |                      | 12   |                      | 15   |                      | 20   | ns    |
| t <sub>LZOE</sub>                | $\overline{OE}$ LOW to LOW Z                            | 3                    |      | 3                    |      | 3                    |      | 3                    |      | ns    |
| t <sub>HZOE</sub>                | $\overline{OE}$ HIGH to HIGH Z                          |                      | 8    |                      | 10   |                      | 12   |                      | 15   | ns    |
| t <sub>PU</sub>                  | $\overline{CE}$ LOW to Power Up                         | 0                    |      | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>PD</sub>                  | $\overline{CE}$ HIGH to Power Down                      |                      | 20   |                      | 20   |                      | 20   |                      | 25   | ns    |
| <b>WRITE CYCLE<sup>[8]</sup></b> |   |                      |      |                      |      |                      |      |                      |      |       |
| t <sub>WC</sub>                  | Write Cycle Time  | 20                   |      | 20                   |      | 25                   |      | 40                   |      | ns    |
| t <sub>SCE</sub>                 | $\overline{CE}$ LOW to Write End                        | 15                   |      | 20                   |      | 25                   |      | 30                   |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End                             | 15                   |      | 20                   |      | 25                   |      | 30                   |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End                             | 0                    |      | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                           | 0                    |      | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>PWE</sub>                 | $\overline{WE}$ Pulse Width                             | 15                   |      | 15                   |      | 20                   |      | 20                   |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End                                | 10                   |      | 10                   |      | 15                   |      | 15                   |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End                                | 0                    |      | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>LZWE</sub>                | $\overline{WE}$ HIGH to Low Z <sup>[7]</sup> (7C162)    | 5                    |      | 5                    |      | 5                    |      | 5                    |      | ns    |
| t <sub>HZWE</sub>                | $\overline{WE}$ LOW to High Z <sup>[6, 7]</sup> (7C162) |                      | 7    |                      | 7    |                      | 10   |                      | 15   | ns    |
| t <sub>AWE</sub>                 | $\overline{WE}$ LOW to Data Valid (7C161)               |                      | 20   |                      | 25   |                      | 30   |                      | 35   | ns    |
| t <sub>ADV</sub>                 | Data Valid to Output Valid (7C161)                      |                      | 20   |                      | 20   |                      | 30   |                      | 35   | ns    |

**Notes:**

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$ ,  $\overline{CE}_2$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CE}_1$ ,  $\overline{CE}_2 = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{CE}_1$ ,  $\overline{CE}_2$  transition LOW.
- Both  $\overline{CE}_1$  and  $\overline{CE}_2$  are represented by CE in the Switching Characteristics and Waveforms.

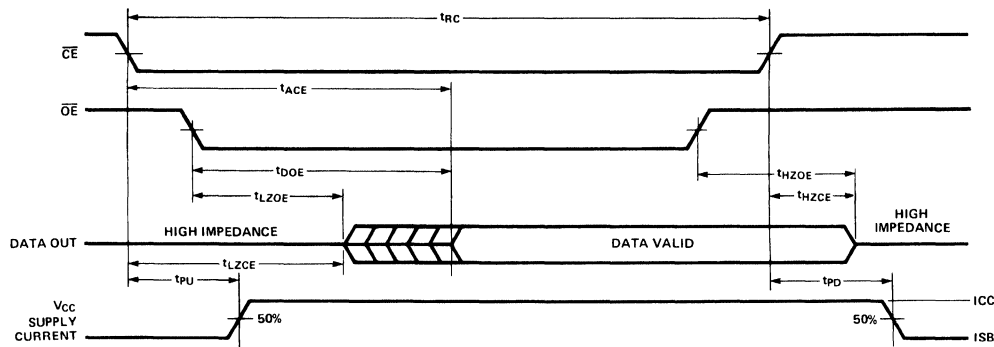
### Switching Waveforms<sup>[12]</sup>

#### Read Cycle No. 1 (Notes 9, 10)

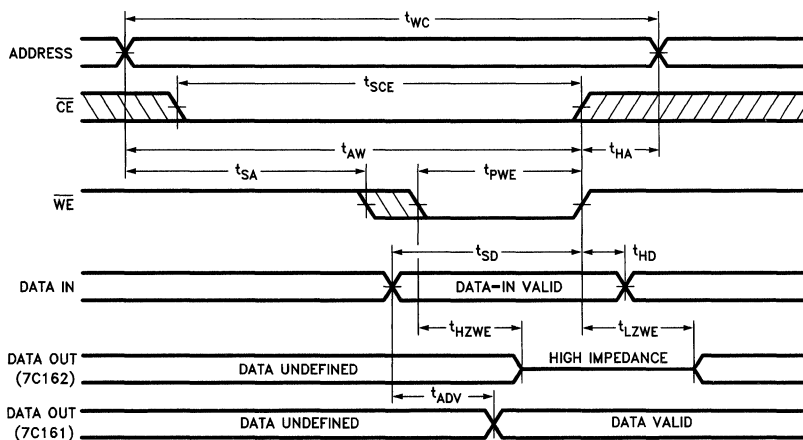


## Switching Waveforms<sup>[12]</sup> (Continued)

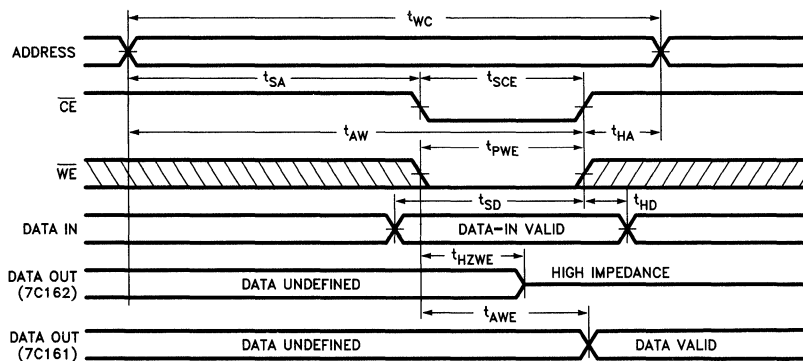
### Read Cycle (Notes 9, 11)



### Write Cycle No. 1 ( $\overline{WE}$ Controlled) (Note 8)



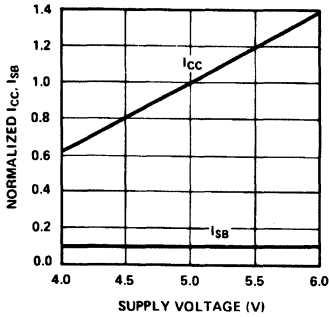
### Write Cycle No. 2 ( $\overline{CE}$ Controlled) (Note 8)



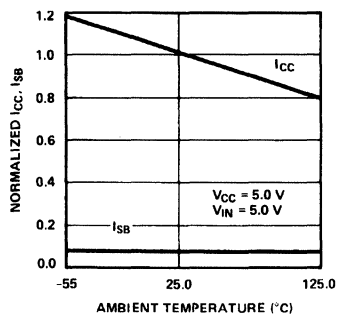
Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state (7C162 only).

Typical DC and AC Characteristics

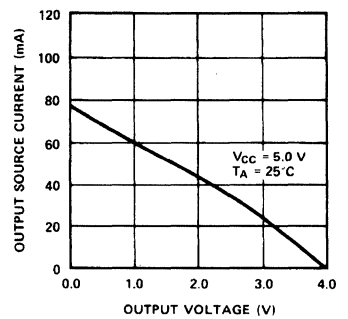
**NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE**



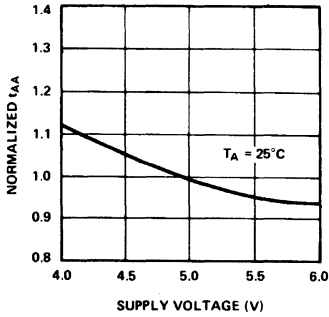
**NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE**



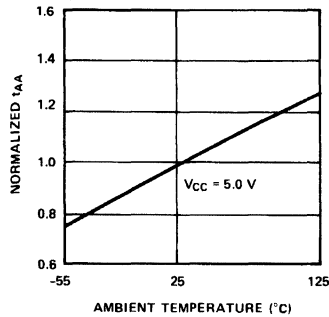
**OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE**



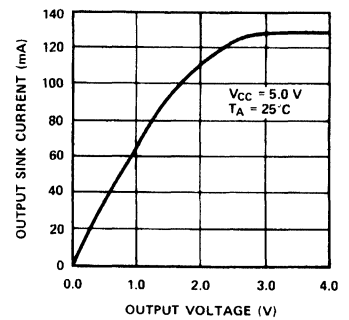
**NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE**



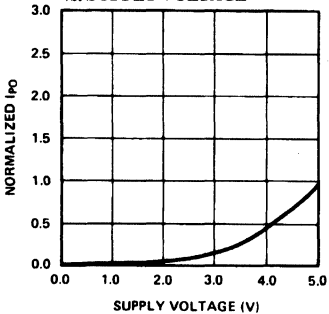
**NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE**



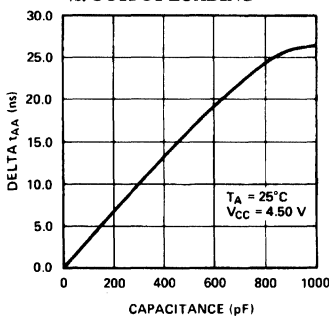
**OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE**



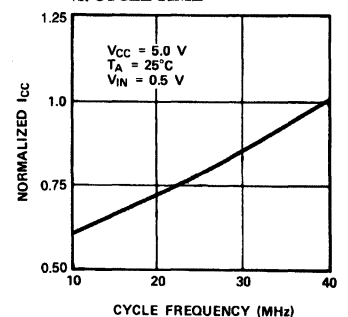
**TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE**



**TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING**



**NORMALIZED ICC vs. CYCLE TIME**

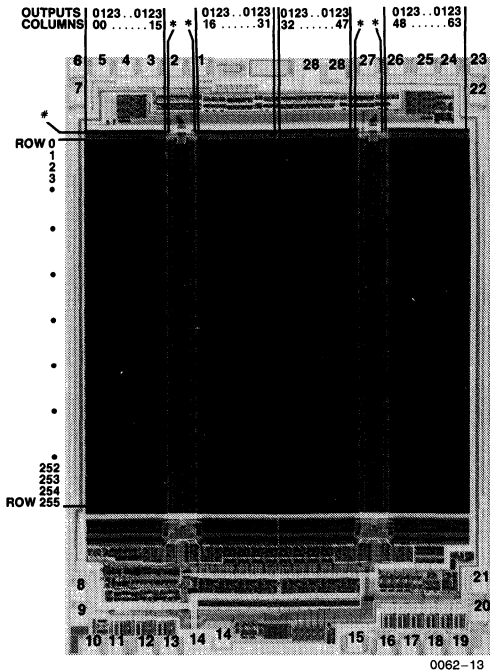


### Ordering Information

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 20         | CY7C161-20PC  | P21          | Commercial      |
|            | CY7C161-20VC  | V21          |                 |
|            | CY7C161-20DC  | D22          |                 |
|            | CY7C161-20LC  | L54          |                 |
| 25         | CY7C161-25PC  | P21          | Commercial      |
|            | CY7C161-25VC  | V21          |                 |
|            | CY7C161-25DC  | D22          |                 |
|            | CY7C161-25LC  | L54          |                 |
|            | CY7C161-25DMB | D22          | Military        |
|            | CY7C161-25LMB | L54          |                 |
| 35         | CY7C161-35PC  | P21          | Commercial      |
|            | CY7C161-35VC  | V21          |                 |
|            | CY7C161-35DC  | D22          |                 |
|            | CY7C161-35LC  | L54          |                 |
|            | CY7C161-35DMB | D22          | Military        |
|            | CY7C161-35LMB | L54          |                 |
| 45         | CY7C161-45PC  | P21          | Commercial      |
|            | CY7C161-45VC  | V21          |                 |
|            | CY7C161-45DC  | D22          |                 |
|            | CY7C161-45LC  | L54          |                 |
|            | CY7C161-45DMB | D22          | Military        |
|            | CY7C161-45LMB | L54          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 20         | CY7C162-20PC  | P21          | Commercial      |
|            | CY7C162-20VC  | V21          |                 |
|            | CY7C162-20DC  | D22          |                 |
|            | CY7C162-20LC  | L54          |                 |
| 25         | CY7C162-25PC  | P21          | Commercial      |
|            | CY7C162-25VC  | V21          |                 |
|            | CY7C162-25DC  | D22          |                 |
|            | CY7C162-25LC  | L54          |                 |
|            | CY7C162-25DMB | D22          | Military        |
|            | CY7C162-25LMB | L54          |                 |
| 35         | CY7C162-35PC  | P21          | Commercial      |
|            | CY7C162-35VC  | V21          |                 |
|            | CY7C162-35DC  | D22          |                 |
|            | CY7C162-35LC  | L54          |                 |
|            | CY7C162-35DMB | D22          | Military        |
|            | CY7C162-35LMB | L54          |                 |
| 45         | CY7C162-45PC  | P21          | Commercial      |
|            | CY7C162-45VC  | V21          |                 |
|            | CY7C162-45DC  | D22          |                 |
|            | CY7C162-45LC  | L54          |                 |
|            | CY7C162-45DMB | D22          | Military        |
|            | CY7C162-45LMB | L54          |                 |
|            | CY7C162-45KMB | K74          |                 |

### Bit Map



### Address Designators

| Address Name | Address Function | Pin Number |
|--------------|------------------|------------|
| A5           | X3               | 1          |
| A6           | X4               | 2          |
| A7           | X5               | 3          |
| A8           | X6               | 4          |
| A9           | X7               | 5          |
| A10          | Y0               | 6          |
| A11          | Y1               | 7          |
| A12          | Y5               | 8          |
| A13          | Y4               | 9          |
| A0           | Y3               | 23         |
| A1           | Y2               | 24         |
| A2           | X0               | 25         |
| A3           | X1               | 26         |
| A4           | X2               | 27         |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>OS</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB1</sub>     | 1,2,3     |
| I <sub>SB2</sub>     | 1,2,3     |

#### Switching Characteristics

| Parameters                      | Subgroups   |
|---------------------------------|-------------|
| <b>READ CYCLE</b>               |             |
| t <sub>RC</sub>                 | 7,8,9,10,11 |
| t <sub>AA</sub>                 | 7,8,9,10,11 |
| t <sub>OHA</sub>                | 7,8,9,10,11 |
| t <sub>ACE</sub>                | 7,8,9,10,11 |
| t <sub>DOE</sub>                | 7,8,9,10,11 |
| <b>WRITE CYCLE</b>              |             |
| t <sub>WC</sub>                 | 7,8,9,10,11 |
| t <sub>SCE</sub>                | 7,8,9,10,11 |
| t <sub>AW</sub>                 | 7,8,9,10,11 |
| t <sub>HA</sub>                 | 7,8,9,10,11 |
| t <sub>SA</sub>                 | 7,8,9,10,11 |
| t <sub>PWE</sub>                | 7,8,9,10,11 |
| t <sub>SD</sub>                 | 7,8,9,10,11 |
| t <sub>HD</sub>                 | 7,8,9,10,11 |
| t <sub>AWE</sub> <sup>[1]</sup> | 7,8,9,10,11 |
| t <sub>ADV</sub> <sup>[1]</sup> | 7,8,9,10,11 |

**Note:**

1. 7C161 only.

Document #: 38-00029-D



**Features**

- Automatic power-down when deselected
- Output Enable ( $\overline{OE}$ ) Feature (7C166)
- CMOS for optimum speed/power
- High speed  
— 10 ns  $t_{AA}$
- Low active power  
— 525 mW at 40 MHz
- Low standby power  
— 150 mW
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

**Functional Description**

The CY7C164 and CY7C166 are high performance CMOS static RAMs organized as 16,384 x 4 bits. These RAMs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and three-state drivers. The CY7C166 has an active low output enable ( $\overline{OE}$ ) feature. Both devices have an automatic power-down feature, reducing the power consumption by 60% when deselected.

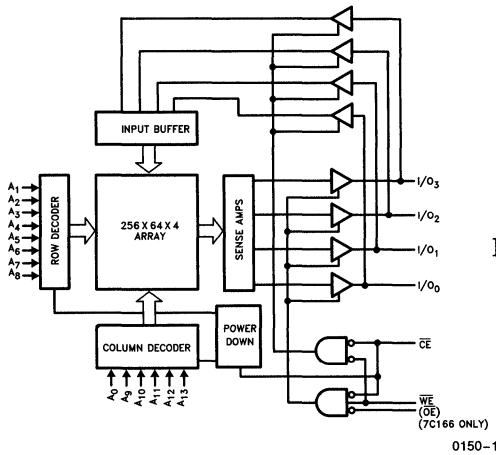
Writing to the device is accomplished when the chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW (and the output enable ( $\overline{OE}$ ) is LOW

for the 7C166). Data on the four input/output pins ( $I/O_0$  through  $I/O_3$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{13}$ ).

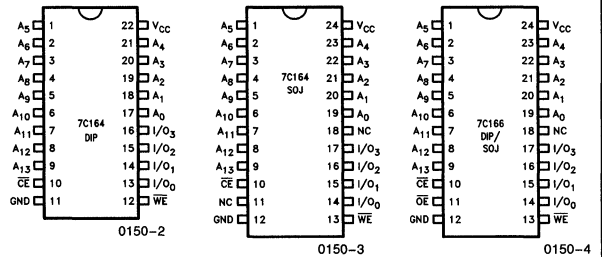
Reading the device is accomplished by taking chip enable ( $\overline{CE}$ ) LOW (and  $\overline{OE}$  LOW for 7C166), while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high impedance state when chip enable ( $\overline{CE}$ ) is HIGH, or write enable ( $\overline{WE}$ ) is LOW (or output enable ( $\overline{OE}$ ) is HIGH for 7C166).

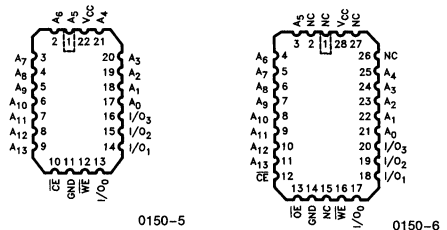
**Logic Block Diagram**



**DIP Pin Configurations**



**LCC Pin Configurations**



**Selection Guide**

|                                | 7C164-10<br>7C166-10 | 7C164-12<br>7C166-12 | 7C164-15<br>7C166-15 |
|--------------------------------|----------------------|----------------------|----------------------|
| Maximum Access Time (ns)       | 10                   | 12                   | 15                   |
| Maximum Operating Current (mA) | Commercial           | 125                  | 115                  |
|                                | Military             |                      | 150                  |
| Maximum Standby Current (mA)   | Commercial           | 30                   | 30                   |
|                                | Military             |                      | 50                   |

### Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied ..... -55°C to +125°C  
 Supply Voltage to Ground Potential .... -0.5V to +7.0V  
 DC Voltage Applied to Outputs  
 in High Z State ..... -0.5V to +7.0V  
 Input Voltage<sup>[14]</sup> ..... -3.0V to +7.0V  
 Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... > 2001V  
 (Per MIL-STD-883 Method 3015)

Latch-up Current ..... > 200 mA

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ±10%         |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ±10%         |

### Electrical Characteristics Over Operating Range<sup>[4]</sup>

| Parameters       | Description  | Test Conditions  | 7C164-10<br>7C166-10 |                 | 7C164-12<br>7C166-12 |                 | 7C164-15<br>7C166-15 |                 | Units |
|------------------|--|--|----------------------|-----------------|----------------------|-----------------|----------------------|-----------------|-------|
|                  |  |  | Min.                 | Max.            | Min.                 | Max.            | Min.                 | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage  | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA                            | 2.4                  |                 | 2.4                  |                 | 2.4                  |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage   | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA                             |                      | 0.4             |                      | 0.4             |                      | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage   |  | 2.2                  | V <sub>CC</sub> | 2.2                  | V <sub>CC</sub> | 2.2                  | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage <sup>[14]</sup>                              |  | -0.5                 | 0.8             | -0.5                 | 0.8             | -0.5                 | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current   | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                                       | -10                  | +10             | -10                  | +10             | -10                  | +10             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current   | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> ,<br>Output Disabled                  | -10                  | +10             | -10                  | +10             | -10                  | +10             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>                    | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND                               |                      | -350            |                      | -350            |                      | -350            | mA    |
| I <sub>CC1</sub> | V <sub>CC</sub> Operating Supply Current                       | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA<br>f = 40 MHz              | Commercial           | 105             |                      | 105             |                      | 105             | mA    |
|                  |  |  | Military             |                 |                      | 130             |                      | 130             |       |
| I <sub>CC2</sub> | V <sub>CC</sub> Operating Supply Current                       | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA<br>f = f max.              | Commercial           | 125             |                      | 120             |                      | 115             | mA    |
|                  |  |  | Military             |                 |                      | 150             |                      | 135             |       |
| I <sub>SB</sub>  | Automatic $\overline{CE}$ <sup>[2]</sup><br>Power Down Current | Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$<br>Min. Duty Cycle = 100% | Commercial           | 30              |                      | 30              |                      | 30              | mA    |
|                  |  |  | Military             |                 |                      | 50              |                      | 50              |       |

### Capacitance<sup>[5]</sup>

| Parameters       | Description        | Test Conditions   | Max. <sup>[15]</sup> | Units |
|------------------|--------------------|---|----------------------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 5                    | pF    |
| C <sub>OUT</sub> | Output Capacitance |   | 7                    |       |

#### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the  $\overline{CE}$  input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.

### AC Test Loads and Waveforms

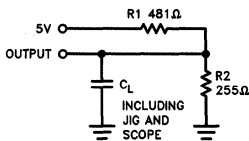


Figure 1a

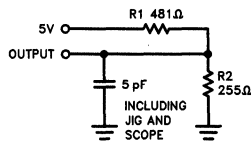


Figure 1b

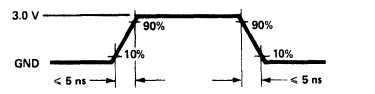
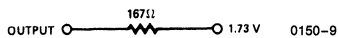


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over Operating Range<sup>[4, 6]</sup>

| Parameters                       | Description                                      | 7C164-10<br>7C166-10 |      | 7C164-12<br>7C166-12 |      | 7C164-15<br>7C166-15 |      | Units |    |
|----------------------------------|--|----------------------|------|----------------------|------|----------------------|------|-------|----|
|                                  |  | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. |       |    |
| <b>READ CYCLE</b>                |  |                      |      |                      |      |                      |      |       |    |
| t <sub>RC</sub>                  | Read Cycle Time                                  | 10                   |      | 12                   |      | 15                   |      | ns    |    |
| t <sub>AA</sub>                  | Address to Data Valid                            |                      | 10   |                      | 12   |                      | 15   | ns    |    |
| t <sub>OHA</sub>                 | Output Hold from Address Change                  | 2                    |      | 3                    |      | 3                    |      | ns    |    |
| t <sub>ACE</sub>                 | $\overline{CE}$ LOW to Data Valid                |                      | 10   |                      | 12   |                      | 15   | ns    |    |
| t <sub>DOE</sub>                 | $\overline{OE}$ LOW to Data Valid                | 7C166                | 8    |                      | 10   |                      | 10   | ns    |    |
| t <sub>LZOE</sub>                | $\overline{OE}$ LOW to LOW Z                     | 7C166                | 2    | 2                    |      | 3                    |      | ns    |    |
| t <sub>HZOE</sub>                | $\overline{OE}$ HIGH to HIGH Z                   | 7C166                | 8    | 9                    |      | 8                    |      | ns    |    |
| t <sub>LZCE</sub>                | $\overline{CE}$ LOW to Low Z <sup>[8]</sup>      |                      | 2    | 3                    |      | 3                    |      | ns    |    |
| t <sub>HZCE</sub>                | $\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup> |                      | 6    | 8                    |      | 8                    |      | ns    |    |
| t <sub>PU</sub>                  | $\overline{CE}$ LOW to Power Up                  |                      | 0    | 0                    |      | 0                    |      | ns    |    |
| t <sub>PD</sub>                  | $\overline{CE}$ HIGH to Power Down               |                      | 10   | 12                   |      | 15                   |      | ns    |    |
| <b>WRITE CYCLE<sup>[9]</sup></b> |  |                      |      |                      |      |                      |      |       |    |
| t <sub>WC</sub>                  | Write Cycle Time                                 | 10                   |      | 12                   |      | 15                   |      | ns    |    |
| t <sub>SCE</sub>                 | $\overline{CE}$ LOW to Write End                 | 8                    |      | 10                   |      | 12                   |      | ns    |    |
| t <sub>AW</sub>                  | Address Set-up to Write End                      | 8                    |      | 10                   |      | 12                   |      | ns    |    |
| t <sub>HA</sub>                  | Address Hold from Write End                      | 0                    |      | 0                    |      | 0                    |      | ns    |    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                    | 0                    |      | 0                    |      | 0                    |      | ns    |    |
| t <sub>PWE</sub>                 | $\overline{WE}$ Pulse Width                      | 8                    |      | 10                   |      | 12                   |      | ns    |    |
| t <sub>SD</sub>                  | Data Set-up to Write End                         | 8                    |      | 10                   |      | 10                   |      | ns    |    |
| t <sub>HD</sub>                  | Data Hold from Write End                         | 0                    |      | 0                    |      | 0                    |      | ns    |    |
| t <sub>LZWE</sub>                | $\overline{WE}$ HIGH to Low Z <sup>[8]</sup>     |                      | 3    | 5                    |      | 5                    |      | ns    |    |
| t <sub>HZWE</sub>                | $\overline{WE}$ LOW to High Z <sup>[7, 8]</sup>  |                      | 0    | 5                    | 0    | 7                    | 0    | 7     | ns |

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and C<sub>L</sub> = 30 pF load capacitance for 15 ns t<sub>AA</sub> devices and C<sub>L</sub> = 20 pF load capacitance for 10 and 12 ns t<sub>AA</sub> devices.
- t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> for any given device. These parameters are guaranteed and not 100% tested.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

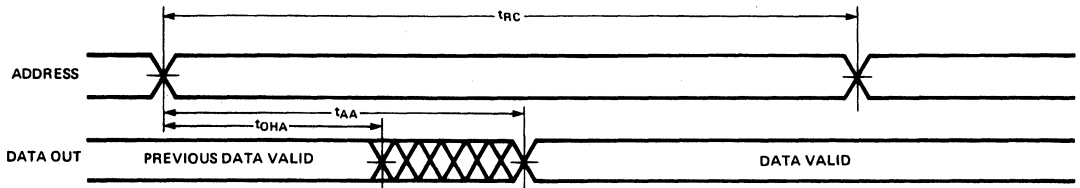
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CE} = V_{IL}$ . (7C166:  $\overline{OE} = V_{IL}$  also.)
- Address valid prior to or coincident with  $\overline{CE}$  transition low.
- 7C166 only: Data I/O will be high impedance if  $\overline{OE} = V_{IH}$ .
- V<sub>IL</sub> (min.) = -3.0V for pulse width < 20 ns.
- For all packages except cerdip (D10, D14) which has maximums of C<sub>IN</sub> = 10 pF, C<sub>OUT</sub> = 12 pF.

2



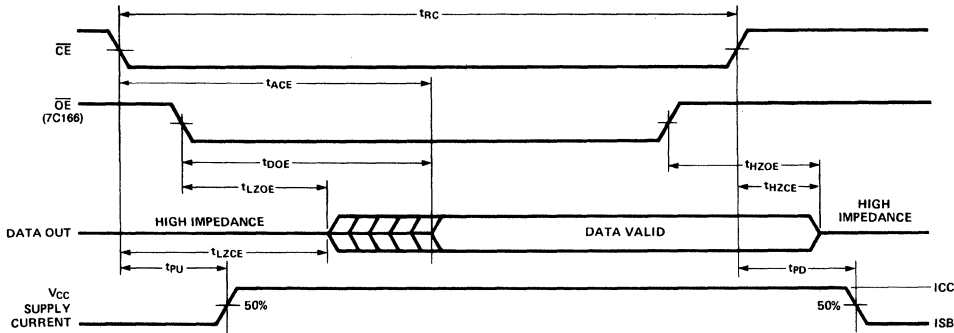
## Switching Waveforms

### Read Cycle No. 1 (Notes 10, 11)



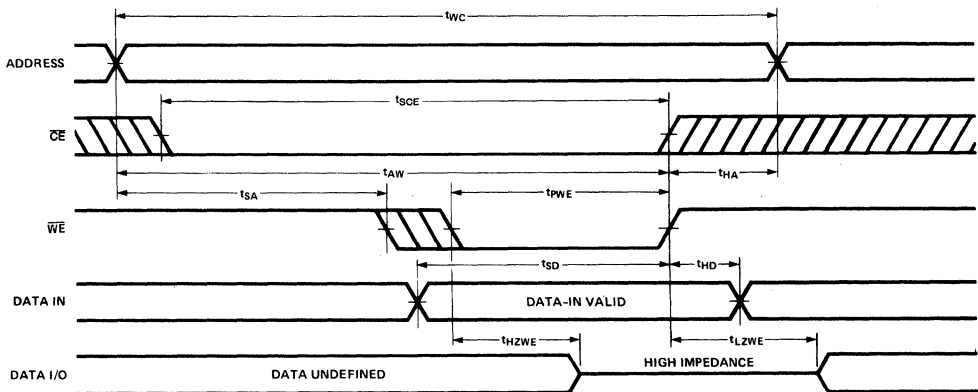
0150-10

### Read Cycle No. 2 (Notes 10, 12)



0150-11

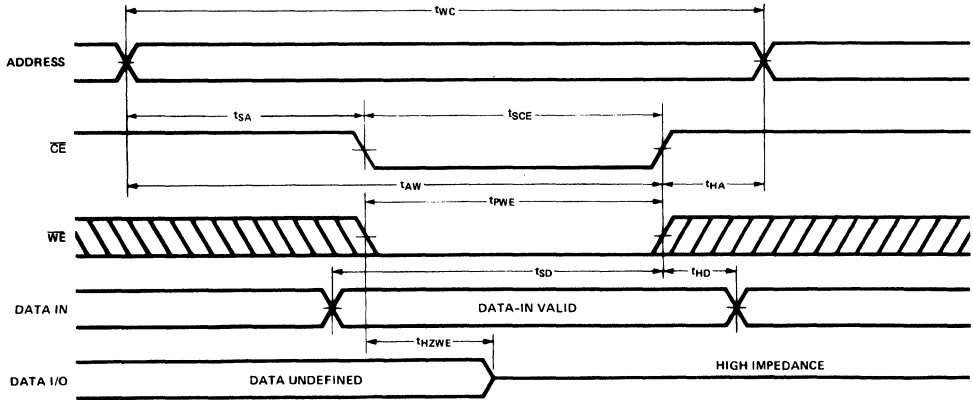
### Write Cycle No. 1 ( $\overline{WE}$ Controlled) (Notes 9, 13)



0150-12

**Switching Waveforms (Continued)**

**Write Cycle No. 2 (CE Controlled) (Notes 9, 13)**



Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

0150-13

**7C164 Truth Table**

| $\overline{CE}$ | $\overline{WE}$ | Input/Outputs | Mode                |
|-----------------|-----------------|---------------|---------------------|
| H               | X               | High Z        | Deselect Power Down |
| L               | H               | Data Out      | Read                |
| L               | L               | Data In       | Write               |

**7C166 Truth Table**

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | Inputs/Outputs | Mode                |
|-----------------|-----------------|-----------------|----------------|---------------------|
| H               | X               | X               | High Z         | Deselect Power Down |
| L               | H               | L               | Data Out       | Read                |
| L               | L               | X               | Data In        | Write               |
| L               | H               | H               | High Z         | Deselect            |

**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 10         | CY7C164-10VC  | V13          | Commercial      |
|            | CY7C164-10LC  | L52          |                 |
| 12         | CY7C164-12PC  | P9           | Commercial      |
|            | CY7C164-12VC  | V13          |                 |
|            | CY7C164-12DC  | D10          |                 |
|            | CY7C164-12LC  | L52          |                 |
|            | CY7C164-12DMB | D10          | Military        |
|            | CY7C164-12LMB | L52          |                 |
|            |               |              |                 |
| 15         | CY7C164-15PC  | P9           | Commercial      |
|            | CY7C164-15VC  | V13          |                 |
|            | CY7C164-15DC  | D10          |                 |
|            | CY7C164-15LC  | L52          |                 |
|            | CY7C164-15DMB | D10          | Military        |
|            | CY7C164-15LMB | L52          |                 |
|            |               |              |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 10         | CY7C166-10VC  | V13          | Commercial      |
|            | CY7C166-10LC  | L54          |                 |
| 12         | CY7C166-12PC  | P13          | Commercial      |
|            | CY7C166-12VC  | V13          |                 |
|            | CY7C166-12DC  | D14          |                 |
|            | CY7C166-12LC  | L54          |                 |
|            | CY7C166-12DMB | D14          | Military        |
|            | CY7C166-12LMB | L54          |                 |
|            |               |              |                 |
| 15         | CY7C166-15PC  | P13          | Commercial      |
|            | CY7C166-15VC  | V13          |                 |
|            | CY7C166-15DC  | D14          |                 |
|            | CY7C166-15LC  | L54          |                 |
|            | CY7C166-15DMB | D14          | Military        |
|            | CY7C166-15LMB | L54          |                 |
|            |               |              |                 |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>Ix</sub>      | 1,2,3     |
| I <sub>Oz</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB</sub>      | 1,2,3     |

**Switching Characteristics**

| Parameters                      | Subgroups   |
|---------------------------------|-------------|
| <b>READ CYCLE</b>               |             |
| t <sub>AA</sub>                 | 7,8,9,10,11 |
| t <sub>OHA</sub>                | 7,8,9,10,11 |
| t <sub>ACE</sub>                | 7,8,9,10,11 |
| t <sub>DOE</sub> <sup>[1]</sup> | 7,8,9,10,11 |
| <b>WRITE CYCLE</b>              |             |
| t <sub>SCE</sub>                | 7,8,9,10,11 |
| t <sub>AW</sub>                 | 7,8,9,10,11 |
| t <sub>HA</sub>                 | 7,8,9,10,11 |
| t <sub>SA</sub>                 | 7,8,9,10,11 |
| t <sub>PWE</sub>                | 7,8,9,10,11 |
| t <sub>SD</sub>                 | 7,8,9,10,11 |
| t <sub>HD</sub>                 | 7,8,9,10,11 |

**Note:**

1. 7C166 only.

Document #: 38-A-00015



**Features**

- Automatic power-down when deselected
- Output Enable ( $\overline{OE}$ ) Feature (7C166)
- CMOS for optimum speed/power
- High speed  
— 20 ns  $t_{AA}$
- Low active power  
— 440 mW
- Low standby power  
— 110 mW
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

**Functional Description**

The CY7C164 and CY7C166 are high performance CMOS static RAMs organized as 16,384 x 4 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and three-state drivers. The CY7C166 has an active low output enable ( $\overline{OE}$ ) feature. Both devices have an automatic power-down feature, reducing the power consumption by 60% when deselected.

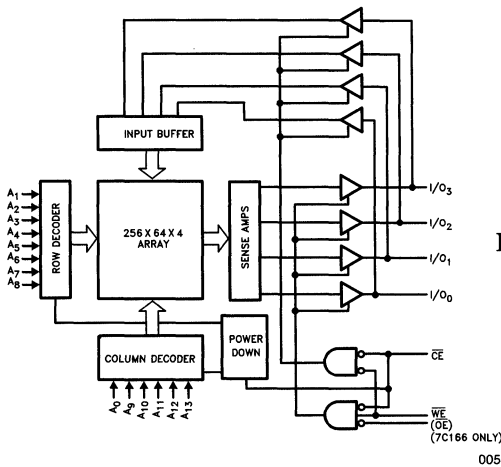
Writing to the device is accomplished when the chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW (and the output enable ( $\overline{OE}$ ) is LOW for the 7C166). Data on the four input/output pins ( $I/O_0$  through  $I/O_3$ )

is written into the memory location specified on the address pins ( $A_0$  through  $A_{13}$ ).

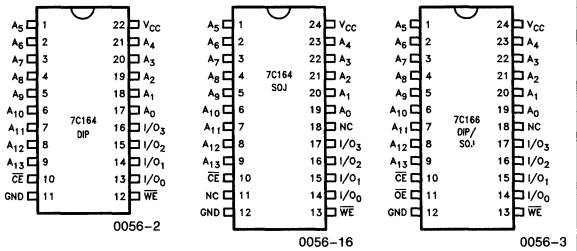
Reading the device is accomplished by taking chip enable ( $\overline{CE}$ ) LOW (and  $\overline{OE}$  LOW for 7C166), while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high impedance state when chip enable ( $\overline{CE}$ ) is HIGH, or write enable ( $\overline{WE}$ ) is LOW (or output enable ( $\overline{OE}$ ) is HIGH for 7C166). A die coat is used to insure alpha immunity.

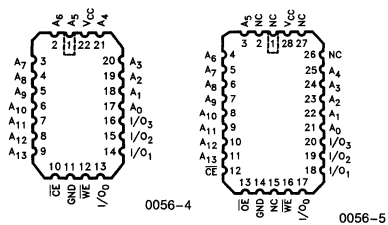
**Logic Block Diagram**



**DIP Pin Configurations**



**LCC Pin Configurations**



**Selection Guide**

|                                | 7C164-20<br>7C166-20 | 7C164-25<br>7C166-25 | 7C164-35<br>7C166-35 | 7C164-45<br>7C166-45 |
|--------------------------------|----------------------|----------------------|----------------------|----------------------|
| Maximum Access Time (ns)       | 20                   | 25                   | 35                   | 45                   |
| Maximum Operating Current (mA) | Commercial           | 80                   | 70                   | 50                   |
|                                | Military             | 80                   | 70                   | 70                   |
| Maximum Standby Current (mA)   | Commercial           | 40/20                | 20/20                | 20/20                |
|                                | Military             | 40/20                | 20/20                | 20/20                |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential .... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... > 2001V  
(Per MIL-STD-883 Method 3015)

Latch-up Current ..... > 200 mA

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[4]</sup>

| Parameters       | Description  | Test Conditions   | 7C164-20<br>7C166-20 |                 | 7C164-25, 35<br>7C166-25, 35 |                 | 7C164-45<br>7C166-45 |                 | Units |
|------------------|--|---|----------------------|-----------------|------------------------------|-----------------|----------------------|-----------------|-------|
|                  |  |   | Min.                 | Max.            | Min.                         | Max.            | Min.                 | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage  | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA   | 2.4                  |                 | 2.4                          |                 | 2.4                  |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage   | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA  |                      | 0.4             |                              | 0.4             |                      | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage   |   | 2.2                  | V <sub>CC</sub> | 2.2                          | V <sub>CC</sub> | 2.2                  | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage <sup>[5A]</sup>                              |   | -3.0                 | 0.8             | -3.0                         | 0.8             | -3.0                 | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current   | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>  | -10                  | +10             | -10                          | +10             | -10                  | +10             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current   | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> ,<br>Output Disabled   | -10                  | +10             | -10                          | +10             | -10                  | +10             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>                    | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND  |                      | -350            |                              | -350            |                      | -350            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current                       | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA   | Coml.                |                 | 80                           | 70              | 50                   | mA              |       |
|                  |  |   | Mil.                 | 25              |                              | 80              | 70                   |                 |       |
| I <sub>SB1</sub> | Automatic $\overline{CE}$ <sup>[2]</sup><br>Power Down Current | Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$<br>Min. Duty Cycle = 100%  |                      | Coml.           |                              | 40              | 20                   | 20              | mA    |
|                  |  |   | Mil.                 | 25              |                              | 40              | 20                   |                 |       |
| I <sub>SB2</sub> | Automatic $\overline{CE}$ <sup>[2]</sup><br>Power Down Current | Max. V <sub>CC</sub> ,<br>$\overline{CE} \geq V_{CC} - 0.3V$<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V |                      | Coml.           |                              | 20              | 20                   | 20              | mA    |
|                  |  |   | Mil.                 |                 |                              | 20              | 20                   |                 |       |

### Capacitance<sup>[5]</sup>

| Parameters       | Description        | Test Conditions   | Max. | Units |
|------------------|--------------------|---|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |   | 7    |       |

#### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the  $\overline{CE}$  input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.
- V<sub>IL</sub> min. = -3.0V for pulse durations less than 30 ns.

### AC Test Loads and Waveforms

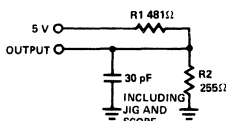


Figure 1a

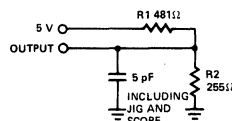


Figure 1b

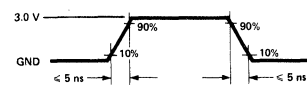
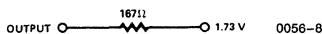


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



0056-8

### Switching Characteristics Over Operating Range<sup>[4, 6]</sup>

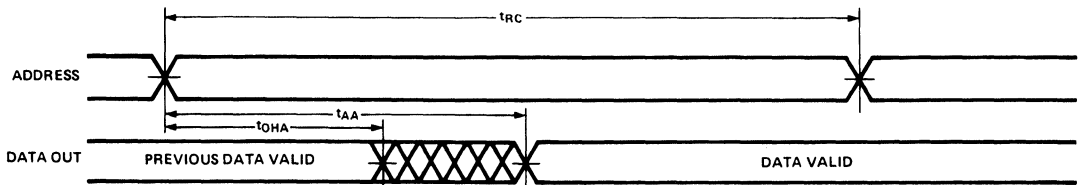
| Parameters                       | Description                                      | 7C164-20<br>7C166-20 |      | 7C164-25<br>7C166-25 |      | 7C164-35<br>7C166-35 |      | 7C164-45<br>7C166-45 |      | Units |    |
|----------------------------------|--|----------------------|------|----------------------|------|----------------------|------|----------------------|------|-------|----|
|                                  |  | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. |       |    |
|                                  |  | <b>READ CYCLE</b>    |      |                      |      |                      |      |                      |      |       |    |
| t <sub>RC</sub>                  | Read Cycle Time                                  | 20                   |      | 25                   |      | 35                   |      | 45                   |      | ns    |    |
| t <sub>AA</sub>                  | Address to Data Valid                            |                      | 20   |                      | 25   |                      | 35   |                      | 45   | ns    |    |
| t <sub>OHA</sub>                 | Output Hold from Address Change                  | 5                    |      | 5                    |      | 5                    |      | 5                    |      | ns    |    |
| t <sub>ACE</sub>                 | $\overline{CE}$ LOW to Data Valid                |                      | 20   |                      | 25   |                      | 35   |                      | 45   | ns    |    |
| t <sub>DOE</sub>                 | $\overline{OE}$ LOW to Data Valid                | 7C166                | 10   |                      | 12   |                      | 15   |                      | 20   | ns    |    |
| t <sub>LZOE</sub>                | $\overline{OE}$ LOW to LOW Z                     | 7C166                | 3    |                      | 3    |                      | 3    |                      | 3    | ns    |    |
| t <sub>HZOE</sub>                | $\overline{OE}$ HIGH to HIGH Z                   | 7C166                |      | 8                    |      | 10                   |      | 12                   |      | 15    | ns |
| t <sub>LZCE</sub>                | $\overline{CE}$ LOW to Low Z <sup>[8]</sup>      |                      | 5    |                      | 5    |                      | 5    |                      | 5    | ns    |    |
| t <sub>HZCE</sub>                | $\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup> |                      |      | 8                    |      | 10                   |      | 15                   |      | 15    | ns |
| t <sub>PU</sub>                  | $\overline{CE}$ LOW to Power Up                  |                      | 0    |                      | 0    |                      | 0    |                      | 0    | ns    |    |
| t <sub>PD</sub>                  | $\overline{CE}$ HIGH to Power Down               |                      | 20   |                      | 20   |                      | 20   |                      | 25   | ns    |    |
| <b>WRITE CYCLE<sup>[9]</sup></b> |  |                      |      |                      |      |                      |      |                      |      |       |    |
| t <sub>WC</sub>                  | Write Cycle Time                                 | 20                   |      | 20                   |      | 25                   |      | 40                   |      | ns    |    |
| t <sub>SCE</sub>                 | $\overline{CE}$ LOW to Write End                 | 15                   |      | 20                   |      | 25                   |      | 30                   |      | ns    |    |
| t <sub>AW</sub>                  | Address Set-up to Write End                      | 15                   |      | 20                   |      | 25                   |      | 30                   |      | ns    |    |
| t <sub>HA</sub>                  | Address Hold from Write End                      | 0                    |      | 0                    |      | 0                    |      | 0                    |      | ns    |    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                    | 0                    |      | 0                    |      | 0                    |      | 0                    |      | ns    |    |
| t <sub>PWE</sub>                 | $\overline{WE}$ Pulse Width                      | 15                   |      | 15                   |      | 20                   |      | 20                   |      | ns    |    |
| t <sub>SD</sub>                  | Data Set-up to Write End                         | 10                   |      | 10                   |      | 15                   |      | 15                   |      | ns    |    |
| t <sub>HD</sub>                  | Data Hold from Write End                         | 0                    |      | 0                    |      | 0                    |      | 0                    |      | ns    |    |
| t <sub>LZWE</sub>                | $\overline{WE}$ HIGH to Low Z <sup>[8]</sup>     | 5                    |      | 5                    |      | 5                    |      | 5                    |      | ns    |    |
| t <sub>HZWE</sub>                | $\overline{WE}$ LOW to High Z <sup>[7, 8]</sup>  |                      | 7    |                      | 7    |                      | 10   |                      | 15   | ns    |    |

**Notes:**

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> for any given device. These parameters are guaranteed and not 100% tested.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CE} = V_{IL}$ . (7C166:  $\overline{OE} = V_{IL}$  also.)
- Address valid prior to or coincident with  $\overline{CE}$  transition low.
- 7C166 only: Data I/O will be high impedance if  $\overline{OE} = V_{IH}$ .

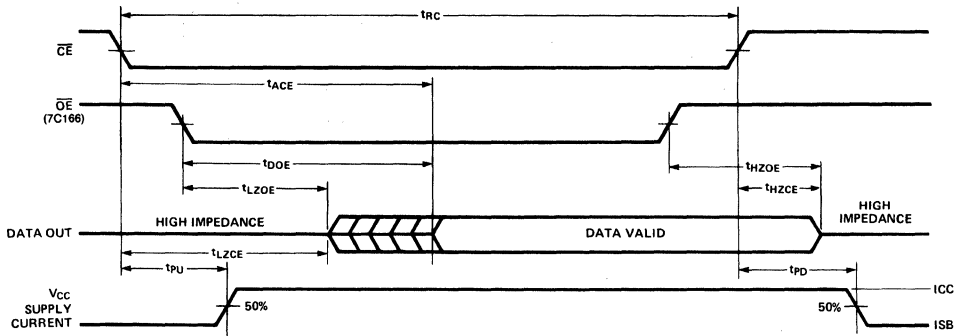
### Switching Waveforms

#### Read Cycle No. 1 (Notes 10, 11)



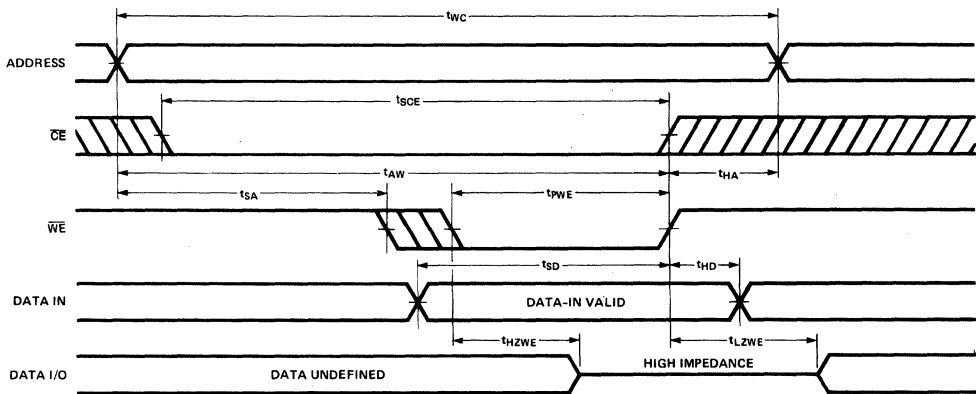
### Switching Waveforms (Continued)

#### Read Cycle No. 2 (Notes 10, 12)



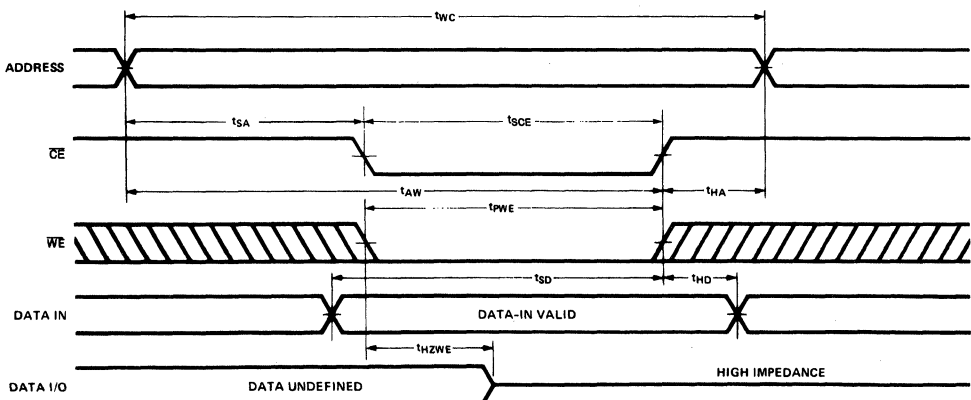
0056-10

#### Write Cycle No. 1 ( $\overline{WE}$ Controlled) (Notes 9, 13)



0056-11

#### Write Cycle No. 2 ( $\overline{CE}$ Controlled) (Notes 9, 13)

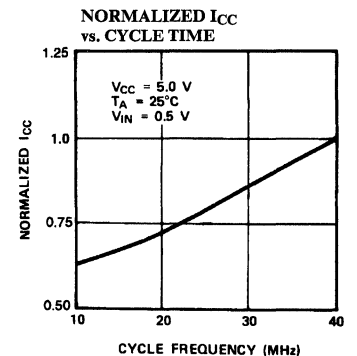
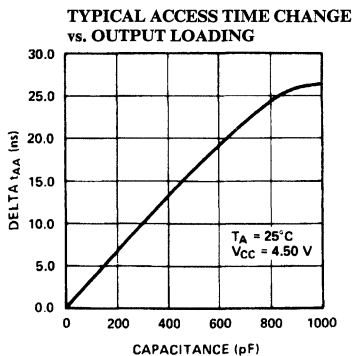
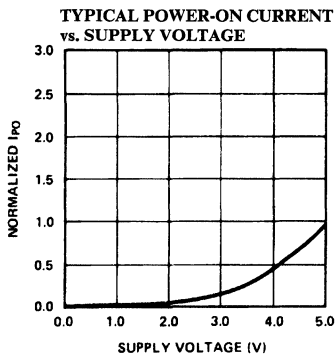
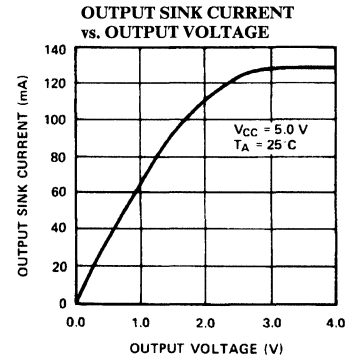
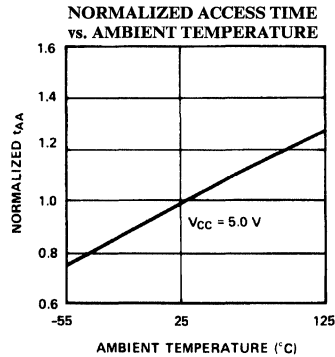
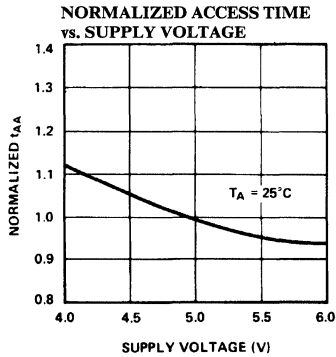
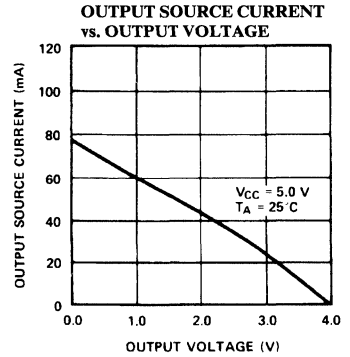
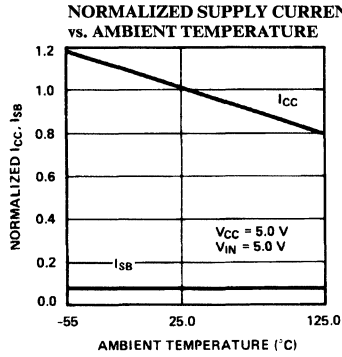
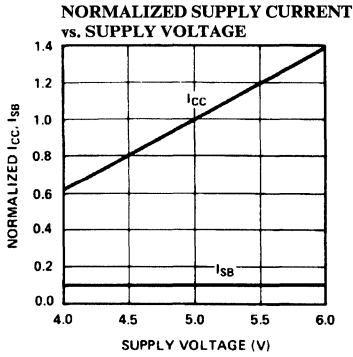


Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

0056-12

Typical DC and AC Characteristics

2





**7C164 Truth Table**

| CE | WE | Input/Outputs | Mode                |
|----|----|---------------|---------------------|
| H  | X  | High Z        | Deselect Power Down |
| L  | H  | Data Out      | Read                |
| L  | L  | Data In       | Write               |

**7C166 Truth Table**

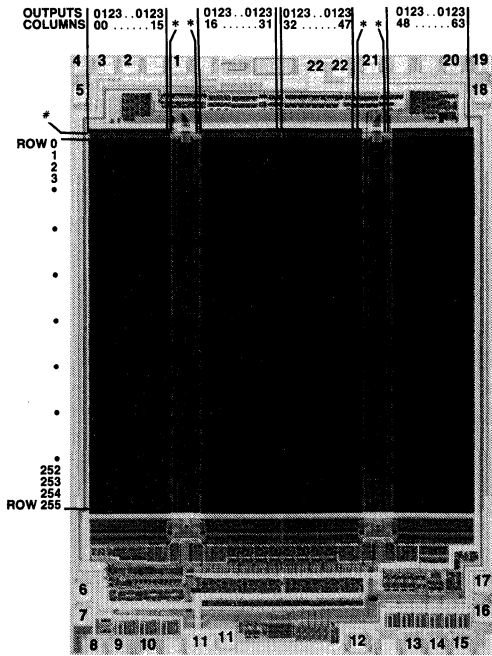
| CE | WE | OE | Inputs/Outputs | Mode                |
|----|----|----|----------------|---------------------|
| H  | X  | X  | High Z         | Deselect Power Down |
| L  | H  | L  | Data Out       | Read                |
| L  | L  | X  | Data In        | Write               |
| L  | H  | H  | High Z         | Deselect            |

**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 20         | CY7C164-20PC  | P9           | Commercial      |
|            | CY7C164-20VC  | V13          |                 |
|            | CY7C164-20DC  | D10          |                 |
|            | CY7C164-20LC  | L52          |                 |
| 25         | CY7C164-25PC  | P9           | Commercial      |
|            | CY7C164-25VC  | V13          |                 |
|            | CY7C164-25DC  | D10          |                 |
|            | CY7C164-25LC  | L52          |                 |
|            | CY7C164-25DMB | D10          | Military        |
|            | CY7C164-25LMB | L52          |                 |
|            | CY7C164-25KMB | K73          |                 |
| 35         | CY7C164-35PC  | P9           | Commercial      |
|            | CY7C164-35VC  | V13          |                 |
|            | CY7C164-35DC  | D10          |                 |
|            | CY7C164-35LC  | L52          |                 |
|            | CY7C164-35DMB | D10          | Military        |
|            | CY7C164-35LMB | L52          |                 |
|            | CY7C164-35KMB | K73          |                 |
| 45         | CY7C164-45PC  | P9           | Commercial      |
|            | CY7C164-45VC  | V13          |                 |
|            | CY7C164-45DC  | D10          |                 |
|            | CY7C164-45LC  | L52          |                 |
|            | CY7C164-45DMB | D10          | Military        |
|            | CY7C164-45LMB | L52          |                 |
|            | CY7C164-45KMB | K73          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 20         | CY7C166-20PC  | P13          | Commercial      |
|            | CY7C166-20VC  | V13          |                 |
|            | CY7C166-20DC  | D14          |                 |
|            | CY7C166-20LC  | L54          |                 |
| 25         | CY7C166-25PC  | P13          | Commercial      |
|            | CY7C166-25VC  | V13          |                 |
|            | CY7C166-25DC  | D14          |                 |
|            | CY7C166-25LC  | L54          |                 |
|            | CY7C166-25DMB | D14          | Military        |
|            | CY7C166-25LMB | L54          |                 |
| 35         | CY7C166-35PC  | P13          | Commercial      |
|            | CY7C166-35VC  | V13          |                 |
|            | CY7C166-35DC  | D14          |                 |
|            | CY7C166-35LC  | L54          |                 |
|            | CY7C166-35DMB | D14          | Military        |
|            | CY7C166-35LMB | L54          |                 |
|            | CY7C166-35KMB | K73          |                 |
| 45         | CY7C166-45PC  | P13          | Commercial      |
|            | CY7C166-45VC  | V13          |                 |
|            | CY7C166-45DC  | D14          |                 |
|            | CY7C166-45LC  | L54          |                 |
|            | CY7C166-45DMB | D14          | Military        |
|            | CY7C166-45LMB | L54          |                 |
|            | CY7C166-45KMB | K73          |                 |

### Bit Map



0056-15

### Address Designators

| Address Name | Address Function | Pin Number |
|--------------|------------------|------------|
| A5           | X3               | 1          |
| A6           | X4               | 2          |
| A7           | X5               | 3          |
| A8           | X6               | 4          |
| A9           | X7               | 5          |
| A10          | Y5               | 6          |
| A11          | Y4               | 7          |
| A12          | Y0               | 8          |
| A13          | Y1               | 9          |
| A0           | Y2               | 17         |
| A1           | Y3               | 18         |
| A2           | X0               | 19         |
| A3           | X1               | 20         |
| A4           | X2               | 21         |

2

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>OS</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| ISB1                 | 1,2,3     |
| ISB2                 | 1,2,3     |

#### Switching Characteristics

| Parameters                      | Subgroups   |
|---------------------------------|-------------|
| <b>READ CYCLE</b>               |             |
| t <sub>RC</sub>                 | 7,8,9,10,11 |
| t <sub>AA</sub>                 | 7,8,9,10,11 |
| t <sub>OHA</sub>                | 7,8,9,10,11 |
| t <sub>ACE</sub>                | 7,8,9,10,11 |
| t <sub>DOE</sub> <sup>[1]</sup> | 7,8,9,10,11 |
| <b>WRITE CYCLE</b>              |             |
| t <sub>WC</sub>                 | 7,8,9,10,11 |
| t <sub>SCE</sub>                | 7,8,9,10,11 |
| t <sub>AW</sub>                 | 7,8,9,10,11 |
| t <sub>HA</sub>                 | 7,8,9,10,11 |
| t <sub>SA</sub>                 | 7,8,9,10,11 |
| t <sub>PWE</sub>                | 7,8,9,10,11 |
| t <sub>SD</sub>                 | 7,8,9,10,11 |
| t <sub>HD</sub>                 | 7,8,9,10,11 |

**Note:**

1. 7C166 only.

Document #: 38-00032-C



**Features**

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed—25 ns
- Low active power — 275 mW
- Low standby power — 83 mW
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

**Functional Description**

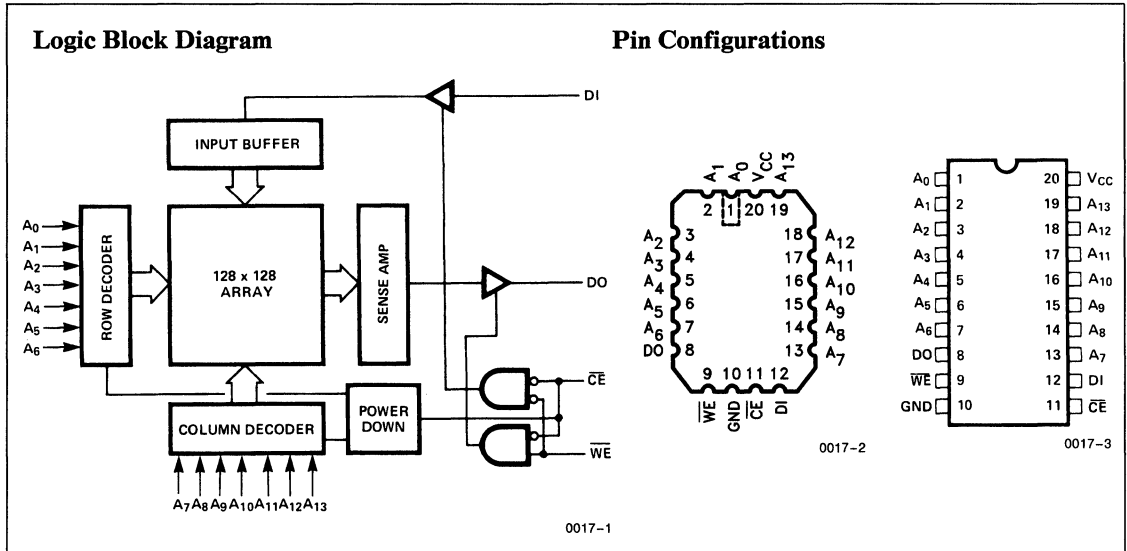
The CY7C167 is a high performance CMOS static RAM organized as 16,384 words x 1 bit. Easy memory expansion is provided by an active LOW chip enable (CE) and three-state drivers. The CY7C167 has an automatic power-down feature, reducing the power consumption by 67% when deselected.

Writing to the device is accomplished when the chip enable (CE) and write enable (WE) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A<sub>0</sub> through A<sub>13</sub>).

Reading the device is accomplished by taking the chip enable (CE) LOW, while write enable (WE) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

The output pin stays in high impedance state when chip enable (CE) is HIGH or write enable (WE) is LOW.

A die coat is used to insure alpha immunity.



**Selection Guide**

|                                |     | 7C167-25   | 7C167-35 | 7C167-45 |
|--------------------------------|-----|------------|----------|----------|
| Maximum Access Time (ns)       |     | 25         | 35       | 45       |
| Maximum Operating Current (mA) | STD | Commercial | 60       | 50       |
|                                |     | Military   | 60       | 50       |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature .....                                   | -65°C to +150°C |
| Ambient Temperature with Power Applied .....                | -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 20 to Pin 10) ..... | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State .....         | -0.5V to +7.0V  |
| DC Input Voltage .....                                      | -3.0V to +7.0V  |
| Output Current into Outputs (Low) .....                     | 20 mA           |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | > 2001V<br>(Per MIL-STD-883 Method 3015) |
| Latch-up Current .....         | > 200 mA                                 |

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[4]</sup>

| Parameters      | Description   | Test Conditions   | 7C167-25   |                 | 7C167-35 |                 | 7C167-45 |                 | Units |
|-----------------|---|---|------------|-----------------|----------|-----------------|----------|-----------------|-------|
|                 |   |   | Min.       | Max.            | Min.     | Max.            | Min.     | Max.            |       |
| V <sub>OH</sub> | Output HIGH Voltage   | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA             | 2.4        |                 | 2.4      |                 | 2.4      |                 | V     |
| V <sub>OL</sub> | Output LOW Voltage  | V <sub>CC</sub> = Min., I <sub>OL</sub> = 12.0 mA, 8.0 mA Mil |            | 0.4             |          | 0.4             |          | 0.4             | V     |
| V <sub>IH</sub> | Input HIGH Voltage  |   | 2.0        | V <sub>CC</sub> | 2.0      | V <sub>CC</sub> | 2.0      | V <sub>CC</sub> | V     |
| V <sub>IL</sub> | Input LOW Voltage   |   | -3.0       | 0.8             | -3.0     | 0.8             | -3.0     | 0.8             | V     |
| I <sub>IX</sub> | Input Load Current  | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                        | -10        | +10             | -10      | +10             | -10      | +10             | μA    |
| I <sub>OZ</sub> | Output Leakage Current                                      | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub><br>Output Disabled     | -50        | +50             | -50      | +50             | -50      | +50             | μA    |
| I <sub>OS</sub> | Output Short <sup>[1]</sup> Circuit Current                 | V <sub>CC</sub> = Max.,<br>V <sub>OUT</sub> = GND             |            | -350            |          | -350            |          | -350            | mA    |
| I <sub>CC</sub> | V <sub>CC</sub> Operating Supply Current                    | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA             | Commercial | 60              | 60       | 50              |          |                 | mA    |
|                 |   |   | Military   |                 | 60       | 50              |          |                 |       |
| I <sub>SB</sub> | Automatic $\overline{CE}$ <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> ,<br>$\overline{CE} \geq V_{IH}$         | Commercial | 20              | 20       | 15              |          |                 | mA    |
|                 |   |   | Military   |                 | 20       | 20              |          |                 |       |

### Capacitance<sup>[5]</sup>

| Parameters       | Description             | Test Conditions  | Max. | Units |
|------------------|-------------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance       | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 4    | pF    |
| C <sub>OUT</sub> | Output Capacitance      |  | 6    |       |
| C <sub>CE</sub>  | Chip Enable Capacitance |  | 5    |       |

#### Notes:

- Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the  $\overline{CE}$  input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.

### AC Test Loads and Waveforms

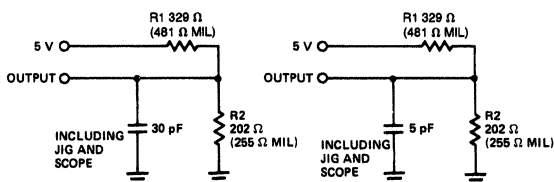


Figure 1a

Figure 1b

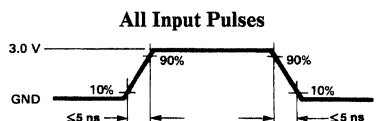
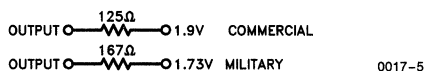


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



0017-5

0017-4

0017-6

**Switching Characteristics Over Operating Range**<sup>[4, 6]</sup>

| Parameters                        | Description                                      | 7C167-25 |      | 7C167-35 |      | 7C167-45 |      | Units |
|-----------------------------------|--|----------|------|----------|------|----------|------|-------|
|                                   |  | Min.     | Max. | Min.     | Max. | Min.     | Max. |       |
| <b>READ CYCLE</b>                 |  |          |      |          |      |          |      |       |
| t <sub>RC</sub>                   | Read Cycle Time (Commercial)                     | 25       |      | 30       |      | 40       |      | ns    |
| t <sub>RC</sub>                   | Read Cycle Time (Military)                       | 25       |      | 35       |      | 40       |      | ns    |
| t <sub>AA</sub>                   | Address to Data Valid (Commercial)               |          | 25   |          | 30   |          | 40   | ns    |
| t <sub>AA</sub>                   | Address to Data Valid (Military)                 |          |      |          | 35   |          | 40   | ns    |
| t <sub>OHA</sub>                  | Data Hold from Address Change                    | 3        |      | 3        |      | 3        |      | ns    |
| t <sub>ACE</sub>                  | $\overline{CE}$ LOW to Data Valid                |          | 25   |          | 35   |          | 45   | ns    |
| t <sub>LZCE</sub>                 | $\overline{CE}$ LOW to Low Z <sup>[8]</sup>      | 5        |      | 5        |      | 5        |      | ns    |
| t <sub>HZCE</sub>                 | $\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup> |          | 15   |          | 20   |          | 25   | ns    |
| t <sub>PU</sub>                   | $\overline{CE}$ LOW to Power Up                  | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>PD</sub>                   | $\overline{CE}$ HIGH to Power Down               |          | 20   |          | 25   |          | 30   | ns    |
| <b>WRITE CYCLE</b> <sup>[9]</sup> |  |          |      |          |      |          |      |       |
| t <sub>WC</sub>                   | Write Cycle Time                                 | 25       |      | 30       |      | 40       |      | ns    |
| t <sub>SCE</sub>                  | $\overline{CE}$ LOW to Write End                 | 25       |      | 30       |      | 40       |      | ns    |
| t <sub>AW</sub>                   | Address Set-up to Write End                      | 25       |      | 30       |      | 40       |      | ns    |
| t <sub>HA</sub>                   | Address Hold from Write End                      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>SA</sub>                   | Address Set-up to Write Start                    | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>PWE</sub>                  | WE Pulse Width                                   | 15       |      | 20       |      | 20       |      | ns    |
| t <sub>SD</sub>                   | Data Set-up to Write End                         | 15       |      | 15       |      | 15       |      | ns    |
| t <sub>HD</sub>                   | Data Hold from Write End                         | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>HZWE</sub>                 | $\overline{WE}$ LOW to High Z <sup>[7, 8]</sup>  |          | 15   |          | 20   |          | 20   | ns    |
| t <sub>LZWE</sub>                 | $\overline{WE}$ HIGH to Low Z <sup>[8]</sup>     | 0        |      | 0        |      | 0        |      | ns    |

**Notes:**

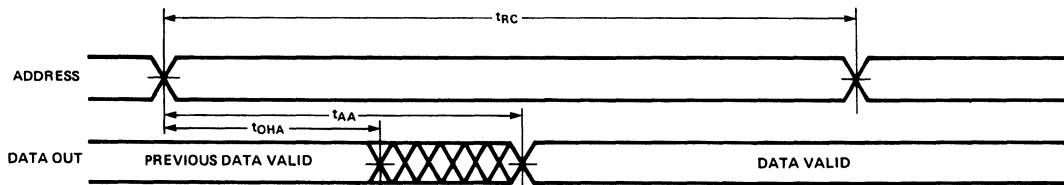
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> for any given device.

- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

10.  $\overline{WE}$  is HIGH for read cycle.

11. Device is continuously selected,  $\overline{CE} = V_{IL}$ .

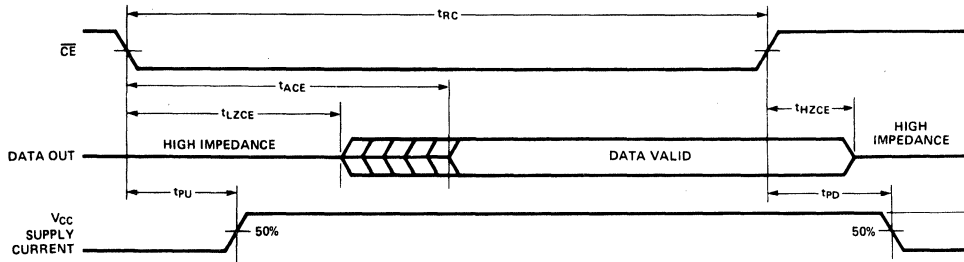
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms**
**Read Cycle No. 1 (Notes 10, 11)**


0017-7

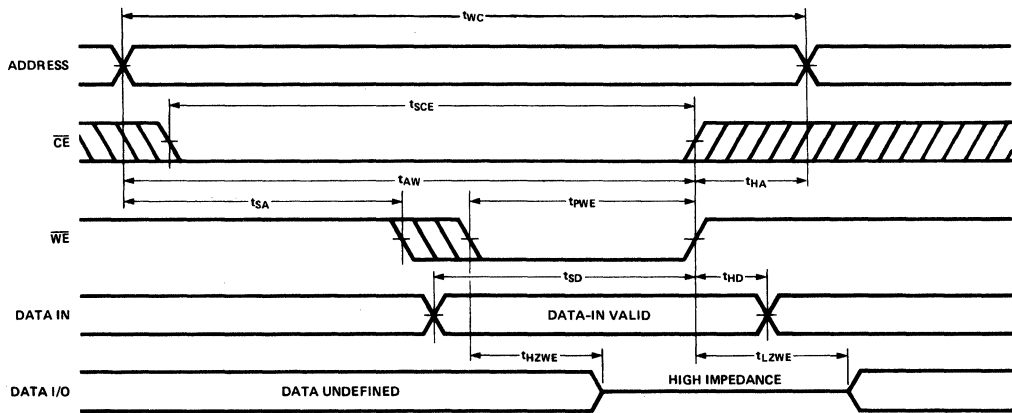
Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 10, 12)



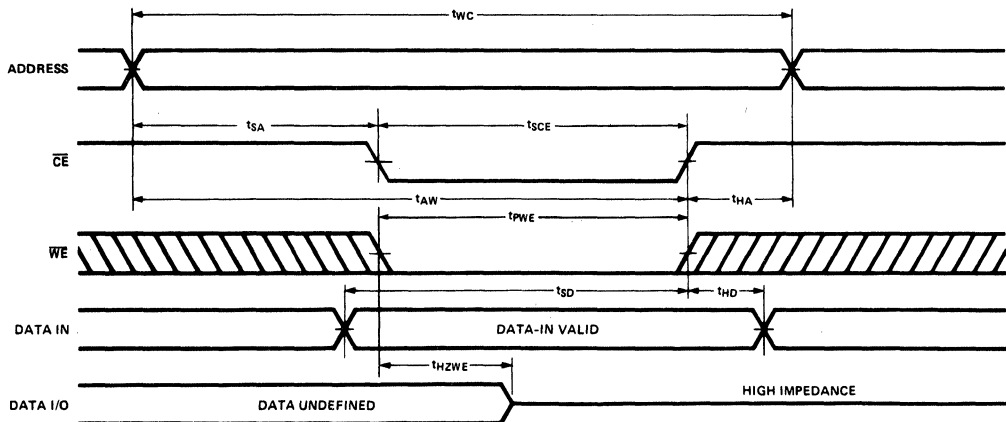
0017-8

Write Cycle No. 1 ( $\overline{WE}$  Controlled) (Note 9)



0017-9

Write Cycle No. 2 ( $\overline{CE}$  Controlled) (Note 9)

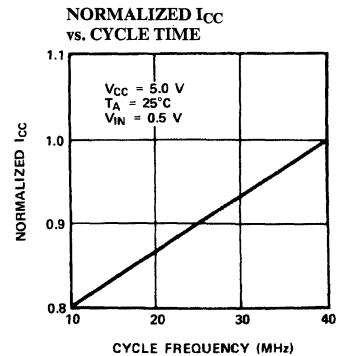
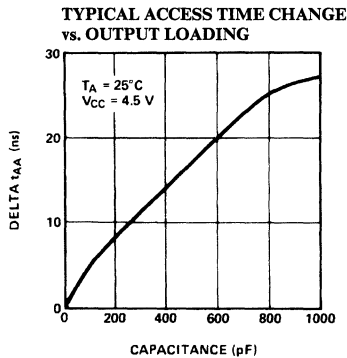
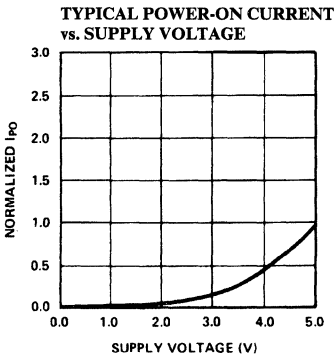
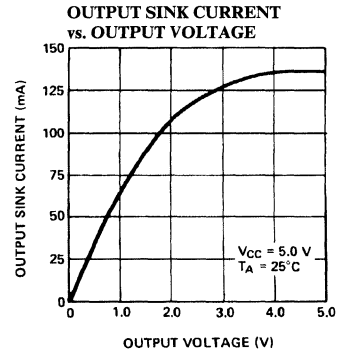
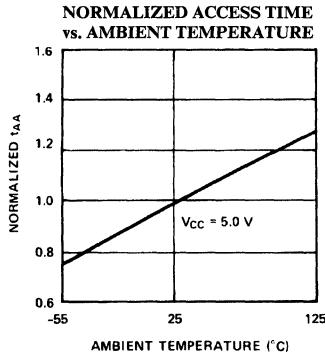
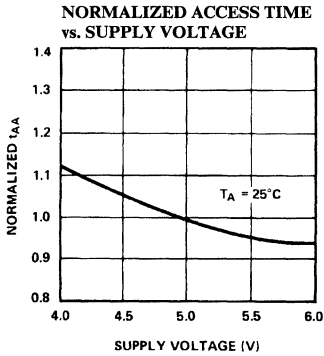
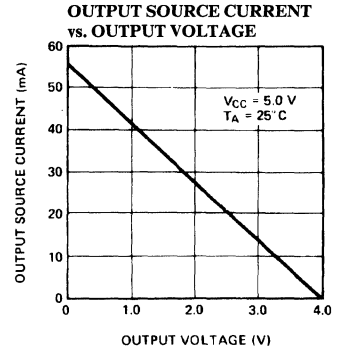
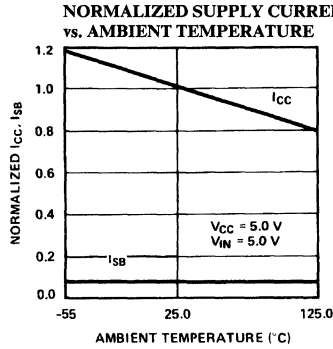
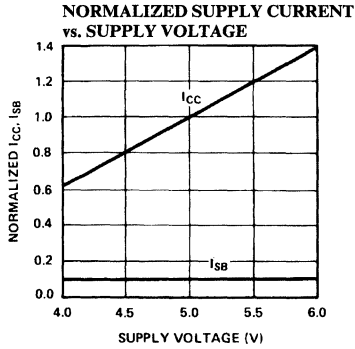


0017-10

Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

Typical DC and AC Characteristics

2





**Ordering Information**

| Speed (ns) | I <sub>CC</sub> mA | Ordering Code | Package Type | Operating Range |
|------------|--------------------|---------------|--------------|-----------------|
| 25         | 60                 | CY7C167-25PC  | P5           | Commercial      |
|            |                    | CY7C167-25DC  | D6           |                 |
|            |                    | CY7C167-25LC  | L51          |                 |
|            |                    | CY7C167-25VC  | V5           |                 |
| 35         | 60                 | CY7C167-35PC  | P5           | Commercial      |
|            |                    | CY7C167-35DC  | D6           |                 |
|            |                    | CY7C167-35LC  | L51          |                 |
|            |                    | CY7C167-35VC  | V5           |                 |
|            |                    | CY7C167-35DMB | D6           | Military        |
|            |                    | CY7C167-35LMB | L51          |                 |
| 45         | 50                 | CY7C167-45PC  | P5           | Commercial      |
|            |                    | CY7C167-45DC  | D6           |                 |
|            |                    | CY7C167-45LC  | L51          |                 |
|            |                    | CY7C167-45VC  | V5           |                 |
|            |                    | CY7C167-45DMB | D6           | Military        |
|            |                    | CY7C167-45LMB | L51          |                 |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

2

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>Ix</sub>      | 1,2,3     |
| I <sub>Oz</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB</sub>      | 1,2,3     |

#### Switching Characteristics

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>ACE</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>SCE</sub>   | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |

Document #: 38-00033-D



### Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed—20 ns
- Low active power — 275 mW
- Low standby power — 83 mW
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge
- $V_{IH}$  of 2.2V

### Functional Description

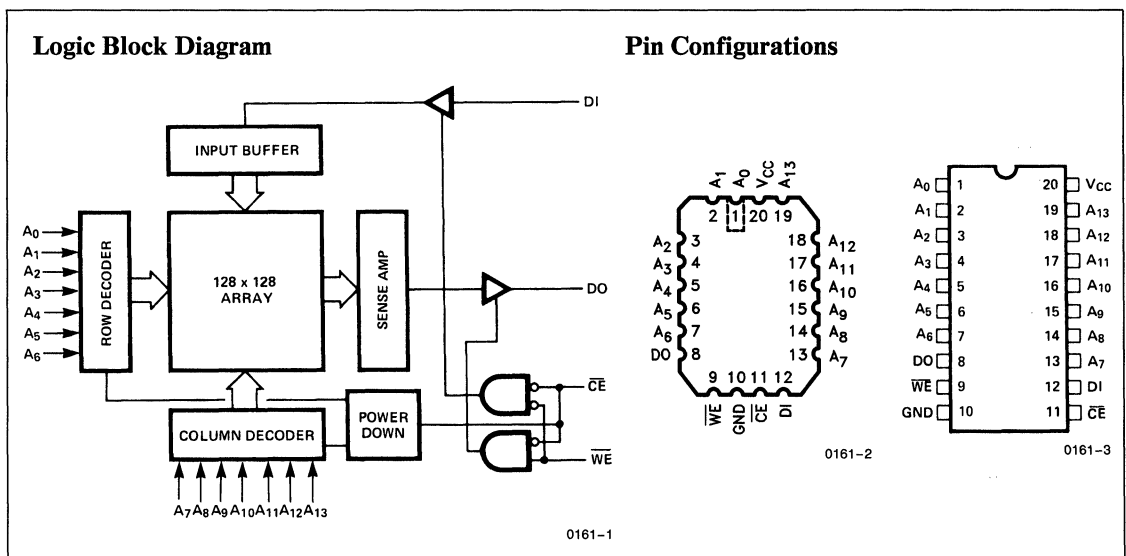
The CY7C167A is a high performance CMOS static RAM organized as 16,384 words x 1 bit. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and three-state drivers. The CY7C167A has an automatic power-down feature, reducing the power consumption by 67% when deselected.

Writing to the device is accomplished when the chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins ( $A_0$  through  $A_{13}$ ).

Reading the device is accomplished by taking the chip enable ( $\overline{CE}$ ) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

The output pin stays in high impedance state when chip enable ( $\overline{CE}$ ) is HIGH or write enable ( $\overline{WE}$ ) is LOW.

A die coat is used to insure alpha immunity.



### Selection Guide

|                                |     | 7C167A-20  | 7C167A-25 | 7C167A-35 | 7C167A-45 |
|--------------------------------|-----|------------|-----------|-----------|-----------|
| Maximum Access Time (ns)       |     | 20         | 25        | 35        | 45        |
| Maximum Operating Current (mA) | STD | Commercial | 60        | 60        | 50        |
|                                |     | Military   | 70        | 60        | 50        |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied ..... -55°C to +125°C  
 Supply Voltage to Ground Potential (Pin 20 to Pin 10) ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs in High Z State ..... -0.5V to +7.0V  
 DC Input Voltage ..... -3.0V to +7.0V  
 Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... > 2001V  
 (Per MIL-STD-883 Method 3015)  
 Latch-up Current ..... > 200 mA

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ±10%         |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ±10%         |

### Electrical Characteristics Over Operating Range<sup>[4]</sup>

| Parameters      | Description  | Test Conditions   | 7C167A-20  |                 | 7C167A-25 |                 | 7C167A-35 |                 | 7C167A-45 |                 | Units |
|-----------------|--|---|------------|-----------------|-----------|-----------------|-----------|-----------------|-----------|-----------------|-------|
|                 |  |   | Min.       | Max.            | Min.      | Max.            | Min.      | Max.            | Min.      | Max.            |       |
| V <sub>OH</sub> | Output HIGH Voltage  | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA             | 2.4        |                 | 2.4       |                 | 2.4       |                 | 2.4       |                 | V     |
| V <sub>OL</sub> | Output LOW Voltage   | V <sub>CC</sub> = Min., I <sub>OL</sub> = 12.0 mA, 8.0 mA Mil |            | 0.4             |           | 0.4             |           | 0.4             |           | 0.4             | V     |
| V <sub>IH</sub> | Input HIGH Voltage   |   | 2.2        | V <sub>CC</sub> | 2.2       | V <sub>CC</sub> | 2.2       | V <sub>CC</sub> | 2.2       | V <sub>CC</sub> | V     |
| V <sub>IL</sub> | Input LOW Voltage <sup>[5A]</sup>                              |   | -0.5       | 0.8             | -0.5      | 0.8             | -0.5      | 0.8             | -0.5      | 0.8             | V     |
| I <sub>IX</sub> | Input Load Current   | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                        | -10        | +10             | -10       | +10             | -10       | +10             | -10       | +10             | μA    |
| I <sub>OZ</sub> | Output Leakage Current   | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub><br>Output Disabled     | -10        | +10             | -10       | +10             | -10       | +10             | -10       | +10             | μA    |
| I <sub>OS</sub> | Output Short <sup>[1]</sup><br>Circuit Current                 | V <sub>CC</sub> = Max.,<br>V <sub>OUT</sub> = GND             |            | -350            |           | -350            |           | -350            |           | -350            | mA    |
| I <sub>CC</sub> | V <sub>CC</sub> Operating<br>Supply Current                    | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA             | Commercial |                 | 60        |                 | 60        |                 | 50        |                 | mA    |
|                 |  |   | Military   |                 | 70        |                 | 60        |                 | 50        |                 |       |
| I <sub>SB</sub> | Automatic $\overline{CE}$ <sup>[2]</sup><br>Power Down Current | Max. V <sub>CC</sub> ,<br>CE ≥ V <sub>IH</sub>                | Commercial |                 | 40        |                 | 20        |                 | 15        |                 | mA    |
|                 |  |   | Military   |                 | 20        |                 | 20        |                 | 20        |                 |       |

### Capacitance<sup>[5]</sup>

| Parameters       | Description             | Test Conditions  | Max. | Units |
|------------------|-------------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance       | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 4    | pF    |
| C <sub>OUT</sub> | Output Capacitance      |  | 6    |       |
| C <sub>CE</sub>  | Chip Enable Capacitance |  | 5    |       |

#### Notes:

- Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the CE input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.
- 5A. V<sub>IL</sub> min. = -3.0V for pulse durations less than 30 ns.

### AC Test Loads and Waveforms

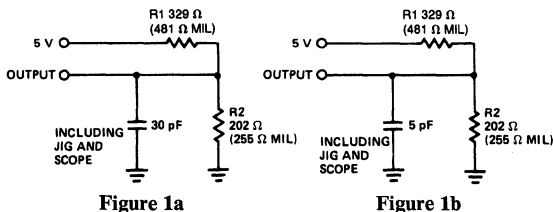
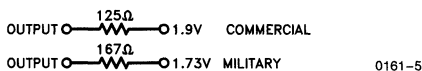


Figure 1a

Figure 1b

Equivalent to: THÉVENIN EQUIVALENT



0161-5

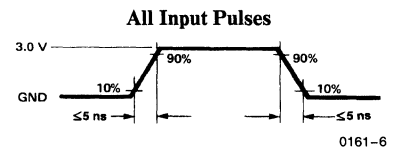


Figure 2

0161-4

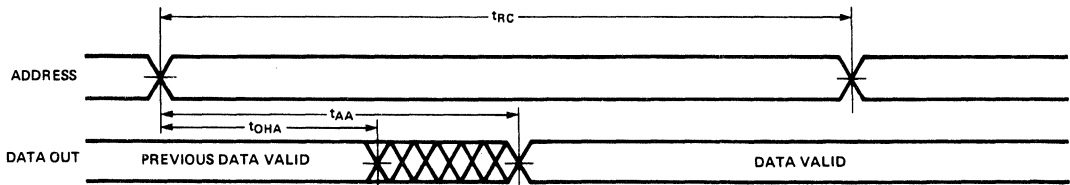
0161-6

**Switching Characteristics Over Operating Range**<sup>[4, 6]</sup>

| Parameters                        | Description                                      | 7C167A-20 |      | 7C167A-25 |      | 7C167A-35 |      | 7C167A-45 |      | Units |
|-----------------------------------|--|-----------|------|-----------|------|-----------|------|-----------|------|-------|
|                                   |  | Min.      | Max. | Min.      | Max. | Min.      | Max. | Min.      | Max. |       |
| <b>READ CYCLE</b>                 |  |           |      |           |      |           |      |           |      |       |
| t <sub>RC</sub>                   | Read Cycle Time (Commercial)                     | 20        |      | 25        |      | 30        |      | 40        |      | ns    |
| t <sub>RC</sub>                   | Read Cycle Time (Military)                       |           |      | 25        |      | 35        |      | 40        |      | ns    |
| t <sub>AA</sub>                   | Address to Data Valid (Commercial)               |           | 20   |           | 25   |           | 30   |           | 40   | ns    |
| t <sub>AA</sub>                   | Address to Data Valid (Military)                 |           |      |           |      |           | 35   |           | 40   | ns    |
| t <sub>OHA</sub>                  | Data Hold from Address Change                    | 5         |      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>ACE</sub>                  | $\overline{CE}$ LOW to Data Valid                |           | 20   |           | 25   |           | 35   |           | 45   | ns    |
| t <sub>LZCE</sub>                 | $\overline{CE}$ LOW to Low Z <sup>[8]</sup>      | 5         |      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>HZCE</sub>                 | $\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup> |           | 8    |           | 10   |           | 15   |           | 15   | ns    |
| t <sub>PU</sub>                   | $\overline{CE}$ LOW to Power Up                  | 0         |      | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>PD</sub>                   | $\overline{CE}$ HIGH to Power Down               |           | 20   |           | 20   |           | 20   |           | 25   | ns    |
| <b>WRITE CYCLE</b> <sup>[9]</sup> |  |           |      |           |      |           |      |           |      |       |
| t <sub>WC</sub>                   | Write Cycle Time                                 | 20        |      | 20        |      | 25        |      | 40        |      | ns    |
| t <sub>SCE</sub>                  | $\overline{CE}$ LOW to Write End                 | 15        |      | 20        |      | 25        |      | 30        |      | ns    |
| t <sub>AW</sub>                   | Address Set-up to Write End                      | 15        |      | 20        |      | 25        |      | 30        |      | ns    |
| t <sub>HA</sub>                   | Address Hold from Write End                      | 0         |      | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>SA</sub>                   | Address Set-up to Write Start                    | 0         |      | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>PWE</sub>                  | WE Pulse Width                                   | 15        |      | 15        |      | 20        |      | 20        |      | ns    |
| t <sub>SD</sub>                   | Data Set-up to Write End                         | 10        |      | 10        |      | 15        |      | 15        |      | ns    |
| t <sub>HD</sub>                   | Data Hold from Write End                         | 0         |      | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>HZWE</sub>                 | WE LOW to High Z <sup>[7, 8]</sup>               |           | 7    |           | 7    |           | 10   |           | 15   | ns    |
| t <sub>LZWE</sub>                 | WE HIGH to Low Z <sup>[8]</sup>                  | 5         |      | 5         |      | 5         |      | 5         |      | ns    |

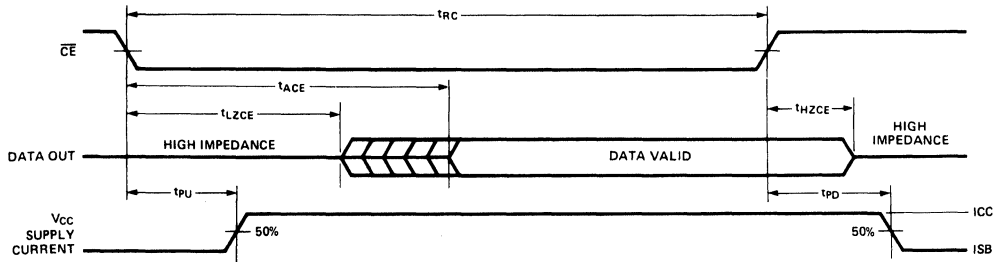
**Notes:**

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CE} = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms**
**Read Cycle No. 1 (Notes 10, 11)**


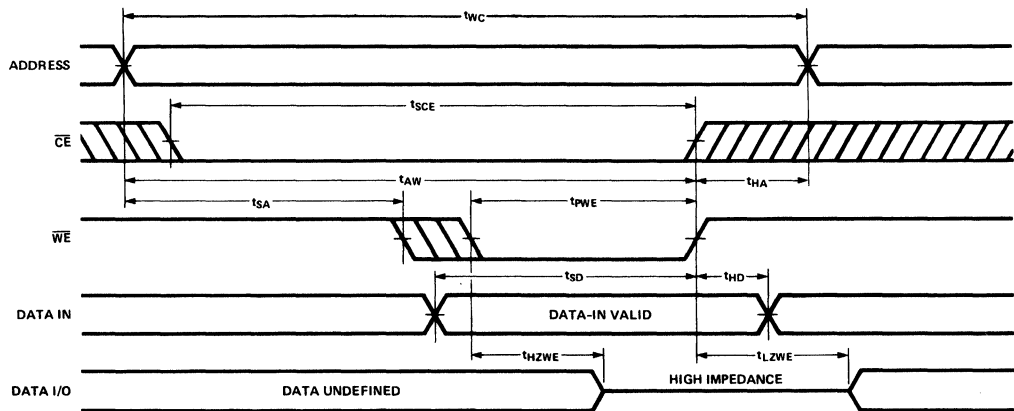
Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 10, 12)



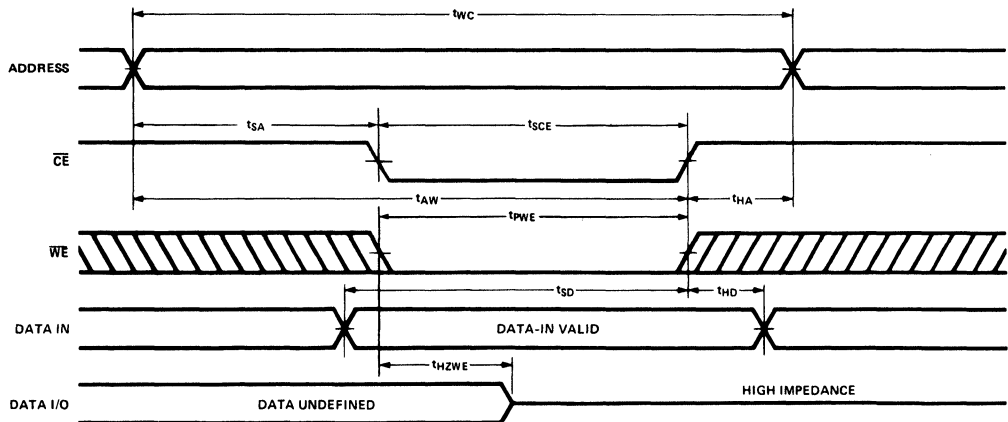
0161-8

Write Cycle No. 1 ( $\overline{WE}$  Controlled) (Note 9)



0161-9

Write Cycle No. 2 ( $\overline{CE}$  Controlled) (Note 9)

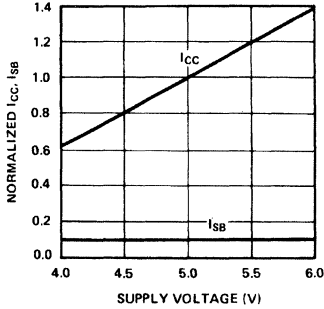


0161-10

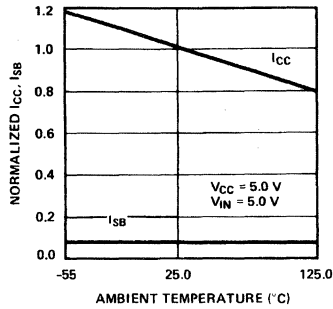
Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

Typical DC and AC Characteristics

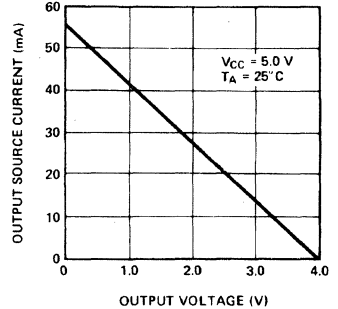
**NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE**



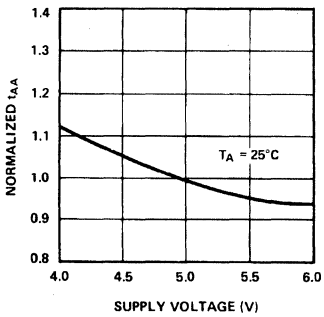
**NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE**



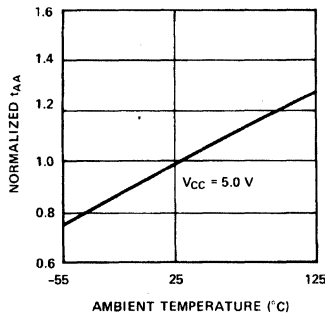
**OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE**



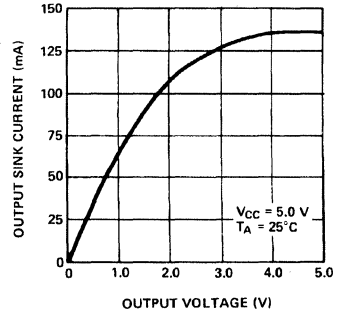
**NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE**



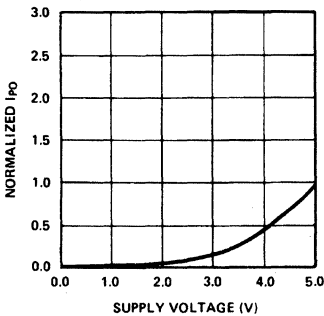
**NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE**



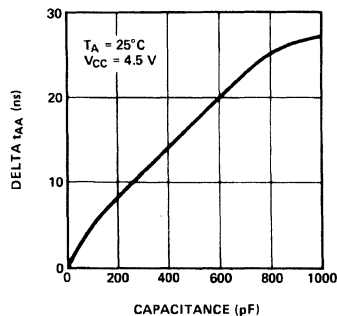
**OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE**



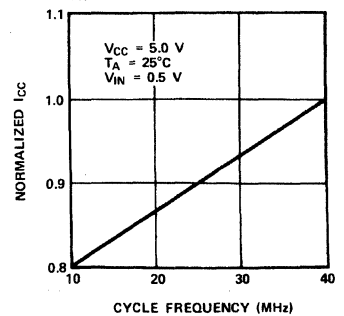
**TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE**



**TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING**



**NORMALIZED I<sub>CC</sub> vs. CYCLE TIME**



**Ordering Information**

| Speed (ns) | ICC mA | Ordering Code  | Package Type | Operating Range |
|------------|--------|----------------|--------------|-----------------|
| 20         | 60     | CY7C167A-20PC  | P5           | Commercial      |
|            |        | CY7C167A-20DC  | D6           |                 |
|            |        | CY7C167A-20VC  | V5           |                 |
| 25         | 60     | CY7C167A-25PC  | P5           | Commercial      |
|            |        | CY7C167A-25DC  | D6           |                 |
|            |        | CY7C167A-25LC  | L51          |                 |
|            |        | CY7C167A-25VC  | V5           |                 |
|            |        | CY7C167A-25DMB | D6           | Military        |
|            |        | CY7C167A-25LMB | L51          |                 |
| 35         | 60     | CY7C167A-35PC  | P5           | Commercial      |
|            |        | CY7C167A-35DC  | D6           |                 |
|            |        | CY7C167A-35LC  | L51          |                 |
|            |        | CY7C167A-35VC  | V5           |                 |
|            |        | CY7C167A-35DMB | D6           | Military        |
|            |        | CY7C167A-35LMB | L51          |                 |
| 45         | 50     | CY7C167A-45PC  | P5           | Commercial      |
|            |        | CY7C167A-45DC  | D6           |                 |
|            |        | CY7C167A-45LC  | L51          |                 |
|            |        | CY7C167A-45VC  | V5           |                 |
|            |        | CY7C167A-45PC  | P5           | Military        |
|            |        | CY7C167A-45DMB | D6           |                 |
|            |        | CY7C167A-45LMB | L51          |                 |



**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL</sub> Max. | 1,2,3     |
| I <sub>Ix</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB</sub>      | 1,2,3     |

**Switching Characteristics**

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>ACE</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>SCE</sub>   | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |

Document #: 38-00093



**Features**

- Automatic power-down when deselected (7C168)
- CMOS for optimum speed/power
- High speed
  - 25 ns  $t_{AA}$
  - 15 ns  $t_{ACE}$  (7C169)
- Low active power
  - 385 mW
- Low standby power (7C168)
  - 83 mW
- TTL compatible inputs and outputs

- Capable of withstanding greater than 2001V electrostatic discharge

**Functional Description**

The CY7C168 and CY7C169 are high performance CMOS static RAMs organized as 4096 x 4 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and three-state drivers. The CY7C168 has an automatic power-down feature, reducing the power consumption by 77% when deselected.

Writing to the device is accomplished when the chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW.

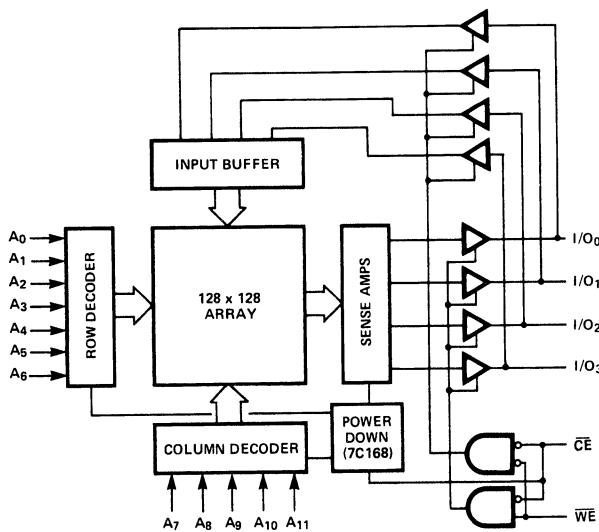
Data on the four input/output pins ( $I/O_0$  through  $I/O_3$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{11}$ ).

Reading the device is accomplished by taking chip enable ( $\overline{CE}$ ) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high impedance state when chip enable ( $\overline{CE}$ ) is HIGH, or write enable ( $\overline{WE}$ ) is LOW.

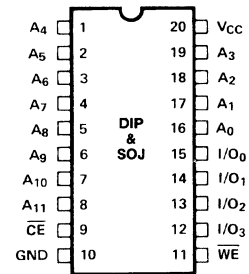
A die coat is used to insure alpha immunity.

**Logic Block Diagram**

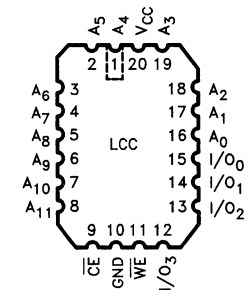


0021-1

**Pin Configurations**



0021-2



0021-3

**Selection Guide**

|                                |     | 7C168-25<br>7C169-25 | 7C168-35<br>7C169-35 | 7C169-40 | 7C168-45 |
|--------------------------------|-----|----------------------|----------------------|----------|----------|
| Maximum Access Time (ns)       |     | 25                   | 35                   | 40       | 45       |
| Maximum Operating Current (mA) | STD | Commercial           | 90                   | 90       | 70       |
|                                |     | Military             |                      | 90       | 70       |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential  
(Pin 20 to Pin 10) ..... -0.5V to +7.0V

DC Voltage Applied to Outputs  
in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... > 2001V  
(Per MIL-STD-883 Method 3015)

Latch-up Current ..... > 200 mA

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[2]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[3]</sup>

| Parameters       | Description                                  | Test Conditions   | 7C168-25<br>7C169-25 |                 | 7C168-35<br>7C169-35 |                 | 7C168-45<br>7C169-40 |                 | Units |
|------------------|--|---|----------------------|-----------------|----------------------|-----------------|----------------------|-----------------|-------|
|                  |  |   | Min.                 | Max.            | Min.                 | Max.            | Min.                 | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA           | 2.4                  |                 | 2.4                  |                 | 2.4                  |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA            |                      | 0.4             |                      | 0.4             |                      | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                           |   | 2.0                  | V <sub>CC</sub> | 2.0                  | V <sub>CC</sub> | 2.0                  | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage                            |   | -3.0                 | 0.8             | -3.0                 | 0.8             | -3.0                 | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current                           | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                      | -10                  | +10             | -10                  | +10             | -10                  | +10             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                       | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> ,<br>Output Disabled | -50                  | +50             | -50                  | +50             | -50                  | +50             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>  | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND              |                      | -350            |                      | -350            |                      | -350            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current     | V <sub>CC</sub> = Max.,<br>I <sub>OUT</sub> = 0 mA          | Commercial           | 90              |                      | 70              |                      | 70              | mA    |
|                  |  |   | Military             |                 |                      | 90              |                      | 70              |       |
| I <sub>SB1</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> ,<br>CE ≥ V <sub>IH</sub>              | Commercial           | 20              |                      | 20              |                      | 15              | mA    |
|                  |  |   | Military             |                 |                      | 20              |                      | 20              |       |
| I <sub>SB2</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> ,<br>CE ≥ V <sub>CC</sub> - 0.3V       | Commercial           | 11              |                      | 11              |                      | 11              | mA    |
|                  |  |   | Military             |                 |                      | 20              |                      | 20              |       |

### Capacitance<sup>[4]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 4    | pF    |
| C <sub>OUT</sub> | Output Capacitance | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 7    | pF    |

#### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.

### AC Test Loads and Waveforms

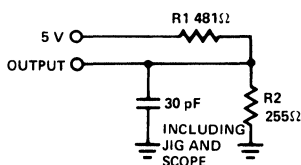


Figure 1a

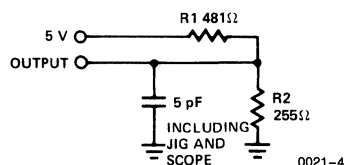


Figure 1b

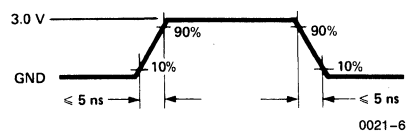


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



### Switching Characteristics Over Operating Range<sup>[3, 5]</sup>

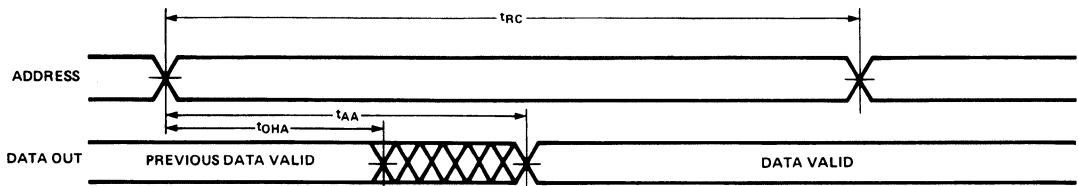
| Parameters                       | Description   | 7C168-25<br>7C169-25 |      | 7C168-35<br>7C169-35 |      | 7C169-40 |      | 7C168-45 |      | Units |
|----------------------------------|---|----------------------|------|----------------------|------|----------|------|----------|------|-------|
|                                  |   | Min.                 | Max. | Min.                 | Max. | Min.     | Max. | Min.     | Max. |       |
| <b>READ CYCLE</b>                |   |                      |      |                      |      |          |      |          |      |       |
| t <sub>RC</sub>                  | Read Cycle Time   | 25                   |      | 35                   |      | 40       |      | 45       |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid                                   |                      | 25   |                      | 35   |          | 40   |          | 45   | ns    |
| t <sub>OHA</sub>                 | Output Hold from Address Change                         | 3                    |      | 3                    |      | 3        |      | 3        |      | ns    |
| t <sub>ACE</sub>                 | $\overline{\text{CE}}$ LOW to Data Valid                | 7C168                | 25   |                      | 35   |          |      |          | 45   | ns    |
|                                  |   | 7C169                | 15   |                      | 25   |          | 25   |          |      | ns    |
| t <sub> LZCE</sub>               | $\overline{\text{CE}}$ LOW to Low Z <sup>[7]</sup>      | 5                    |      | 5                    |      | 5        |      | 5        |      | ns    |
| t <sub> HZCE</sub>               | $\overline{\text{CE}}$ HIGH to High Z <sup>[6, 7]</sup> |                      | 15   |                      | 20   |          | 20   |          | 25   | ns    |
| t <sub>PU</sub>                  | $\overline{\text{CE}}$ LOW to Power Up (7C168)          | 0                    |      | 0                    |      |          |      | 0        |      | ns    |
| t <sub>PD</sub>                  | $\overline{\text{CE}}$ HIGH to Power Down (7C168)       |                      | 25   |                      | 25   |          |      |          | 30   | ns    |
| t <sub>RCS</sub>                 | Read Command Set-up                                     | 0                    |      | 0                    |      | 0        |      | 0        |      | ns    |
| t <sub>RCH</sub>                 | Read Command Hold                                       | 0                    |      | 0                    |      | 0        |      | 0        |      | ns    |
| <b>WRITE CYCLE<sup>[8]</sup></b> |   |                      |      |                      |      |          |      |          |      |       |
| t <sub>WC</sub>                  | Write Cycle Time  | 25                   |      | 35                   |      | 40       |      | 40       |      | ns    |
| t <sub>SCE</sub>                 | $\overline{\text{CE}}$ LOW to Write End                 | 25                   |      | 30                   |      | 30       |      | 35       |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End                             | 20                   |      | 30                   |      | 40       |      | 35       |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End                             | 0                    |      | 0                    |      | 0        |      | 0        |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                           | 0                    |      | 0                    |      | 0        |      | 0        |      | ns    |
| t <sub>PWE</sub>                 | $\overline{\text{WE}}$ Pulse Width                      | 20                   |      | 30                   |      | 35       |      | 35       |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End                                | 10                   |      | 15                   |      | 15       |      | 15       |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End                                | 0                    |      | 0                    |      | 3        |      | 3        |      | ns    |
| t <sub> LZWE</sub>               | $\overline{\text{WE}}$ HIGH to Low Z <sup>[7]</sup>     | 6                    |      | 6                    |      | 6        |      | 6        |      | ns    |
| t <sub> HZWE</sub>               | $\overline{\text{WE}}$ LOW to High Z <sup>[6, 7]</sup>  |                      | 10   |                      | 15   |          | 20   |          | 20   | ns    |

**Notes:**

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZCE</sub> and t<sub>HZWE</sub> are tested with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{\text{WE}}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{\text{CE}} = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{\text{CE}}$  transition LOW.

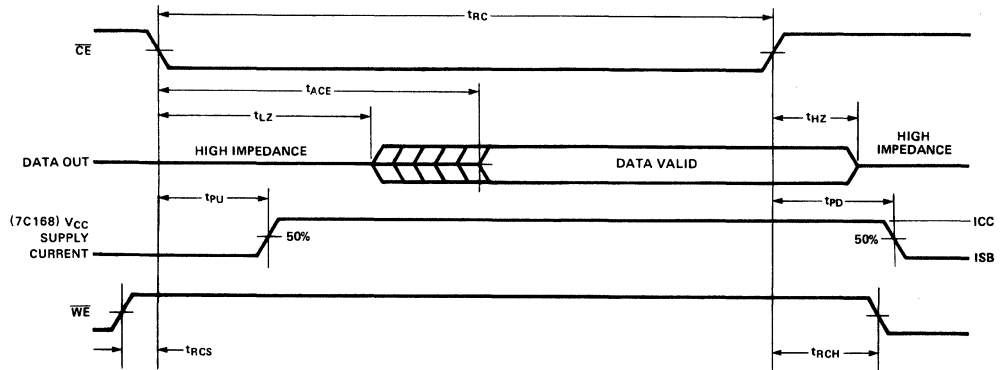
### Switching Waveforms

Read Cycle No. 1 (Notes 9, 10)



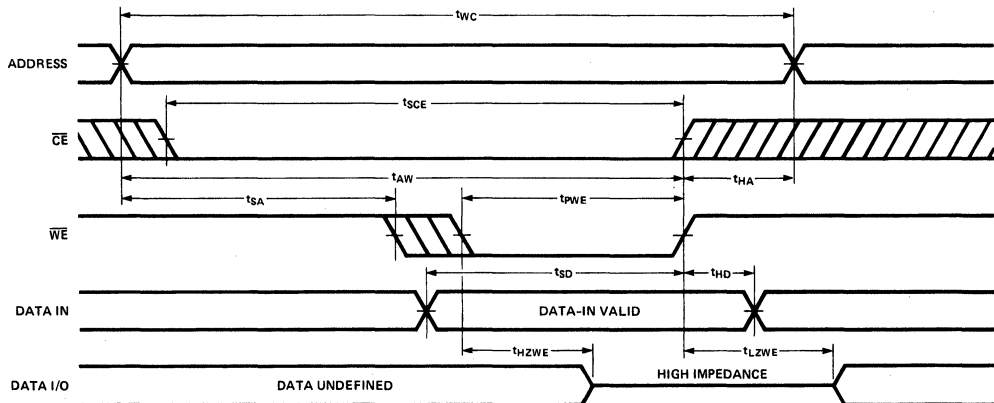
## Switching Waveforms (Continued)

### Read Cycle (Notes 9, 11)



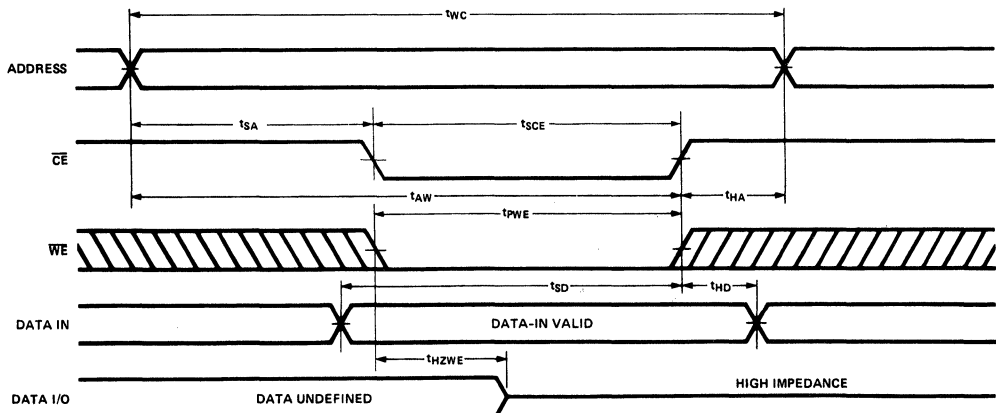
0021-8

### Write Cycle No. 1 (WE Controlled) (Note 8)



0021-9

### Write Cycle No. 2 (CE Controlled) (Note 8)

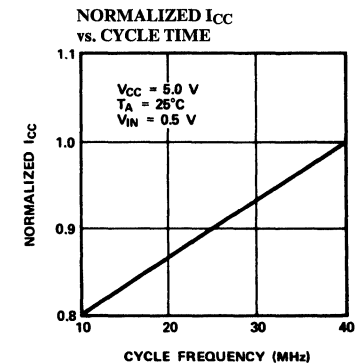
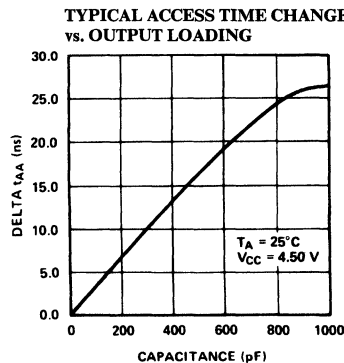
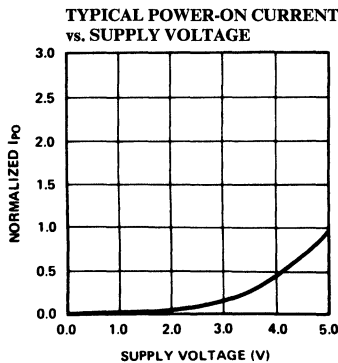
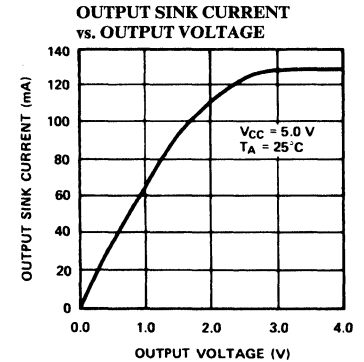
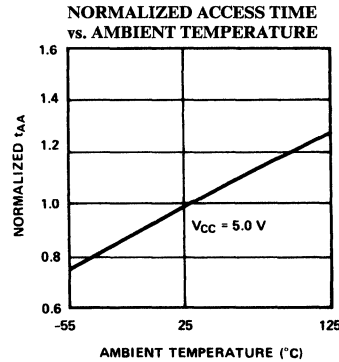
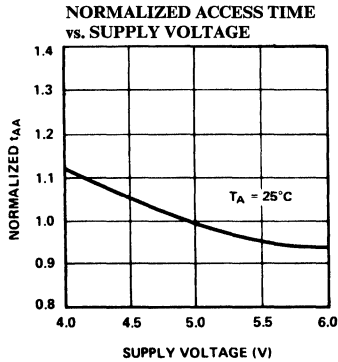
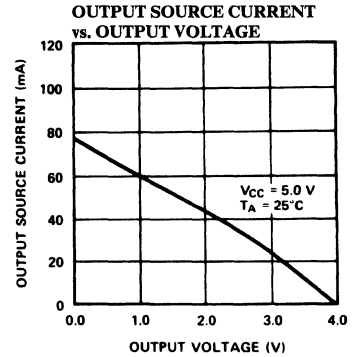
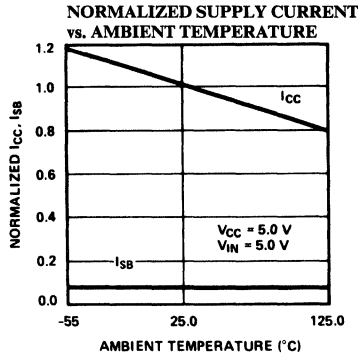
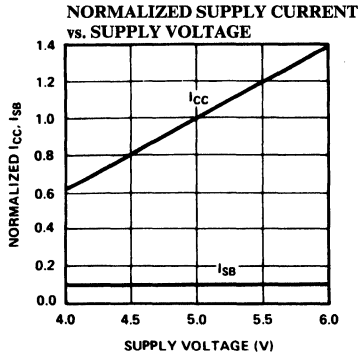


Note: If CE goes HIGH simultaneously with WE HIGH, the output remains in a high impedance state.

0021-10

Typical DC and AC Characteristics

2



**Ordering Information**

| Speed (ns) | ICC mA | Ordering Code | Package Type | Operating Range |
|------------|--------|---------------|--------------|-----------------|
| 25         | 90     | CY7C168-25PC  | P5           | Commercial      |
|            |        | CY7C168-25DC  | D6           |                 |
|            |        | CY7C168-25LC  | L51          |                 |
|            |        | CY7C168-25VC  | V5           |                 |
| 35         | 90     | CY7C168-35PC  | P5           | Commercial      |
|            |        | CY7C168-35DC  | D6           |                 |
|            |        | CY7C168-35LC  | L51          |                 |
|            |        | CY7C168-35VC  | V5           |                 |
|            |        | CY7C168-35DMB | D6           | Military        |
|            |        | CY7C168-35LMB | L51          |                 |
| 45         | 70     | CY7C168-45PC  | P5           | Commercial      |
|            |        | CY7C168-45DC  | D6           |                 |
|            |        | CY7C168-45LC  | L51          |                 |
|            |        | CY7C168-45VC  | V5           |                 |
|            |        | CY7C168-45DMB | D6           | Military        |
|            |        | CY7C168-45LMB | L51          |                 |

| Speed (ns) | ICC mA | Ordering Code | Package Type | Operating Range |
|------------|--------|---------------|--------------|-----------------|
| 25         | 90     | CY7C169-25PC  | P5           | Commercial      |
|            |        | CY7C169-25DC  | D6           |                 |
|            |        | CY7C169-25LC  | L51          |                 |
|            |        | CY7C169-25VC  | V5           |                 |
| 35         | 90     | CY7C169-35PC  | P5           | Commercial      |
|            |        | CY7C169-35DC  | D6           |                 |
|            |        | CY7C169-35LC  | L51          |                 |
|            |        | CY7C169-35VC  | V5           |                 |
|            |        | CY7C169-35DMB | D6           | Military        |
|            |        | CY7C169-35LMB | L51          |                 |
| 40         | 70     | CY7C169-40PC  | P5           | Commercial      |
|            |        | CY7C169-40DC  | D6           |                 |
|            |        | CY7C169-40LC  | L51          |                 |
|            |        | CY7C169-40VC  | V5           |                 |
|            |        | CY7C169-40DMB | D6           | Military        |
|            |        | CY7C169-40LMB | L51          |                 |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters                       | Subgroups |
|----------------------------------|-----------|
| V <sub>OH</sub>                  | 1,2,3     |
| V <sub>OL</sub>                  | 1,2,3     |
| V <sub>IH</sub>                  | 1,2,3     |
| V <sub>IL Max.</sub>             | 1,2,3     |
| I <sub>IX</sub>                  | 1,2,3     |
| I <sub>OZ</sub>                  | 1,2,3     |
| I <sub>CC</sub>                  | 1,2,3     |
| I <sub>SB1</sub> <sup>[12]</sup> | 1,2,3     |
| I <sub>SB2</sub> <sup>[12]</sup> | 1,2,3     |

Note:

12. 7C168 only.

#### Switching Characteristics

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>ACE</sub>   | 7,8,9,10,11 |
| t <sub>RCS</sub>   | 7,8,9,10,11 |
| t <sub>RCH</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>SCE</sub>   | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |

Document #: 38-00034-D





**Features**

- Automatic power-down when deselected (7C168A)
- CMOS for optimum speed/power
- High speed
  - 20 ns  $t_{AA}$
  - 15 ns  $t_{ACE}$  (7C169A)
- Low active power
  - 385 mW
- Low standby power (7C168A)
  - 83 mW
- TTL compatible inputs and outputs
- $V_{IH}$  of 2.2V

- Capable of withstanding greater than 2001V electrostatic discharge

**Functional Description**

The CY7C168A and CY7C169A are high performance CMOS static RAMs organized as 4096 x 4 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and three-state drivers. The CY7C168A has an automatic power-down feature, reducing the power consumption by 77% when deselected.

Writing to the device is accomplished when the chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW.

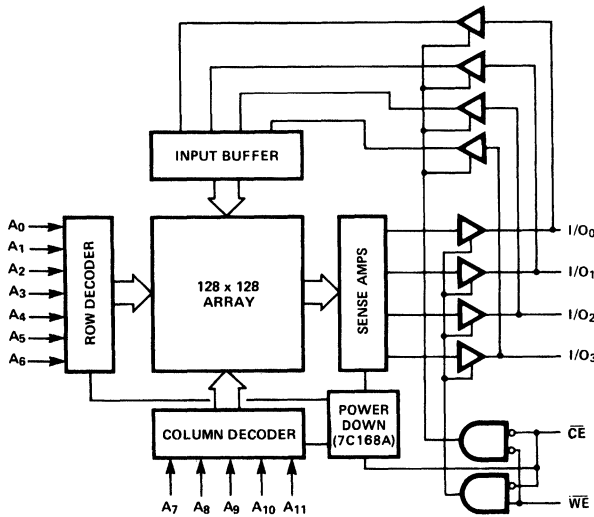
Data on the four input/output pins ( $I/O_0$  through  $I/O_3$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{11}$ ).

Reading the device is accomplished by taking chip enable ( $\overline{CE}$ ) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high impedance state when chip enable ( $\overline{CE}$ ) is HIGH, or write enable ( $\overline{WE}$ ) is LOW.

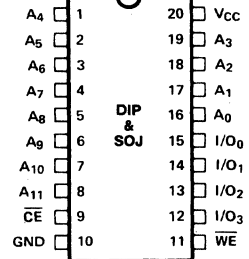
A die coat is used to insure alpha immunity.

**Logic Block Diagram**

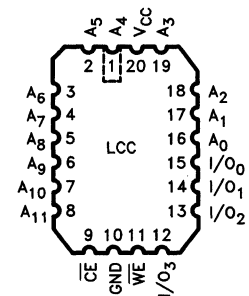


0162-1

**Pin Configurations**



0162-2



0162-3

**Selection Guide**

|                                |          | 7C168A-20<br>7C169A-20 | 7C168A-25<br>7C169A-25 | 7C168A-35<br>7C169A-35 | 7C169A-40 | 7C168A-45 |
|--------------------------------|----------|------------------------|------------------------|------------------------|-----------|-----------|
| Maximum Access Time (ns)       |          | 20                     | 25                     | 35                     | 40        | 45        |
| Maximum Operating Current (mA) | STD      | 90                     | 70                     | 70                     | 50        | 50        |
|                                | Military |                        | 80                     | 70                     | 70        | 70        |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10) ..... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... > 2001V  
(Per MIL-STD-883 Method 3015)

Latch-up Current ..... > 200 mA

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[2]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[3]</sup>

| Parameters       | Description                                  | Test Conditions   | 7C168A-20<br>7C169A-20 |                 | 7C168A-25<br>7C169A-25 |                 | 7C168A-35<br>7C169A-35 |                 | 7C168A-45<br>7C169A-40 |                 | Units |
|------------------|--|---|------------------------|-----------------|------------------------|-----------------|------------------------|-----------------|------------------------|-----------------|-------|
|                  |  |   | Min.                   | Max.            | Min.                   | Max.            | Min.                   | Max.            | Min.                   | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA           | 2.4                    |                 | 2.4                    |                 | 2.4                    |                 | 2.4                    |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA            |                        | 0.4             |                        | 0.4             |                        | 0.4             |                        | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                           |   | 2.2                    | V <sub>CC</sub> | 2.2                    | V <sub>CC</sub> | 2.2                    | V <sub>CC</sub> | 2.2                    | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage <sup>[4A]</sup>            |   | -0.5                   | 0.8             | -0.5                   | 0.8             | -0.5                   | 0.8             | -0.5                   | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current                           | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                      | -10                    | +10             | -10                    | +10             | -10                    | +10             | -10                    | +10             | μA    |
| I <sub>IOZ</sub> | Output Leakage Current                       | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> ,<br>Output Disabled | -10                    | +10             | -10                    | +10             | -10                    | +10             | -10                    | +10             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>  | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND              |                        | -350            |                        | -350            |                        | -350            |                        | -350            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current     | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA           | Commercial             | 90              |                        | 70              |                        | 70              |                        | 70              | mA    |
|                  |  |   | Military               |                 |                        |                 |                        | 80              |                        | 70              |       |
| I <sub>SB1</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> ,<br>CE ≥ V <sub>IH</sub>              | Commercial             | 40              |                        | 20              |                        | 20              |                        | 20              | mA    |
|                  |  |   | Military               |                 |                        |                 |                        | 20              |                        | 20              |       |
| I <sub>SB2</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> ,<br>CE ≥ V <sub>CC</sub> - 0.3V       | Commercial             | 20              |                        | 20              |                        | 20              |                        | 20              | mA    |
|                  |  |   | Military               |                 |                        |                 |                        | 20              |                        | 20              |       |

### Capacitance<sup>[4]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 7    | pF    |

**Notes:**

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.
- V<sub>IL min.</sub> = -3.0V for pulse durations less than 30 ns.

### AC Test Loads and Waveforms

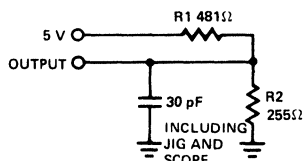


Figure 1a

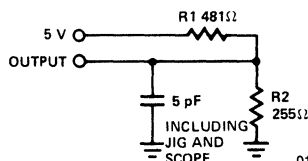


Figure 1b

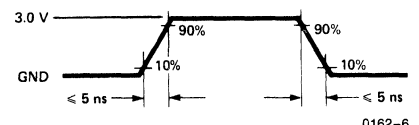


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



**Switching Characteristics Over Operating Range<sup>[3, 5]</sup>**

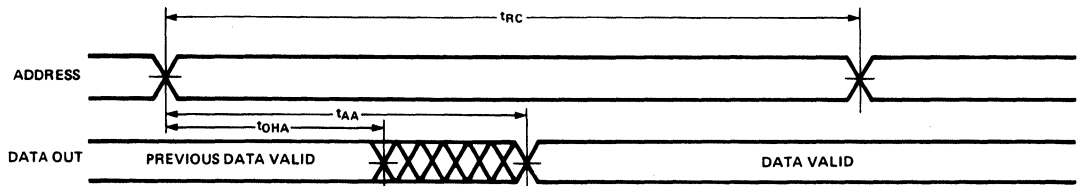
| Parameters                       | Description   | 7C168A-20 |      | 7C168A-25 |      | 7C168A-35 |      | 7C169A-40 |      | 7C168A-45 |      | Units |    |
|----------------------------------|---|-----------|------|-----------|------|-----------|------|-----------|------|-----------|------|-------|----|
|                                  |   | 7C169A-20 |      | 7C169A-25 |      | 7C169A-35 |      |           |      |           |      |       |    |
|                                  |   | Min.      | Max. | Min.      | Max. | Min.      | Max. | Min.      | Max. | Min.      | Max. |       |    |
| <b>READ CYCLE</b>                |   |           |      |           |      |           |      |           |      |           |      |       |    |
| t <sub>RC</sub>                  | Read Cycle Time   | 20        |      | 25        |      | 35        |      | 40        |      | 45        |      | ns    |    |
| t <sub>AA</sub>                  | Address to Data Valid                                   |           | 20   |           | 25   |           | 35   |           | 40   |           | 45   | ns    |    |
| t <sub>OHA</sub>                 | Output Hold from Address Change                         | 5         |      | 5         |      | 5         |      | 5         |      | 5         |      | ns    |    |
| t <sub>ACE</sub>                 | $\overline{\text{CE}}$ LOW to Data Valid                | 7C168A    |      | 20        |      | 25        |      | 35        |      | 40        |      | 45    | ns |
|                                  |   | 7C169A    |      | 12        |      | 15        |      | 25        |      | 25        |      |       | ns |
| t <sub>LZCE</sub>                | $\overline{\text{CE}}$ LOW to Low Z <sup>[7, 12]</sup>  | 5         |      | 5         |      | 5         |      | 5         |      | 5         |      | ns    |    |
| t <sub>HZCE</sub>                | $\overline{\text{CE}}$ HIGH to High Z <sup>[6, 7]</sup> |           | 8    |           | 10   |           | 15   |           | 15   |           | 15   | ns    |    |
| t <sub>PU</sub>                  | $\overline{\text{CE}}$ LOW to Power Up (7C168A)         | 0         |      | 0         |      | 0         |      |           |      | 0         |      | ns    |    |
| t <sub>PD</sub>                  | $\overline{\text{CE}}$ HIGH to Power Down (7C168A)      |           | 20   |           | 20   |           | 20   |           | 20   |           | 25   | ns    |    |
| t <sub>RCS</sub>                 | Read Command Set-up                                     | 0         |      | 0         |      | 0         |      | 0         |      | 0         |      | ns    |    |
| t <sub>RCH</sub>                 | Read Command Hold                                       | 0         |      | 0         |      | 0         |      | 0         |      | 0         |      | ns    |    |
| <b>WRITE CYCLE<sup>[8]</sup></b> |   |           |      |           |      |           |      |           |      |           |      |       |    |
| t <sub>WC</sub>                  | Write Cycle Time  | 20        |      | 20        |      | 25        |      | 35        |      | 40        |      | ns    |    |
| t <sub>SCE</sub>                 | $\overline{\text{CE}}$ LOW to Write End                 | 15        |      | 20        |      | 25        |      | 30        |      | 30        |      | ns    |    |
| t <sub>AW</sub>                  | Address Set-up to Write End                             | 15        |      | 20        |      | 25        |      | 30        |      | 30        |      | ns    |    |
| t <sub>HA</sub>                  | Address Hold from Write End                             | 0         |      | 0         |      | 0         |      | 0         |      | 0         |      | ns    |    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                           | 0         |      | 0         |      | 0         |      | 0         |      | 0         |      | ns    |    |
| t <sub>PWE</sub>                 | $\overline{\text{WE}}$ Pulse Width                      | 15        |      | 15        |      | 20        |      | 20        |      | 20        |      | ns    |    |
| t <sub>SD</sub>                  | Data Set-up to Write End                                | 10        |      | 10        |      | 15        |      | 15        |      | 15        |      | ns    |    |
| t <sub>HD</sub>                  | Data Hold from Write End                                | 0         |      | 0         |      | 0         |      | 0         |      | 0         |      | ns    |    |
| t <sub>LZWE</sub>                | $\overline{\text{WE}}$ HIGH to Low Z <sup>[7]</sup>     | 7         |      | 7         |      | 10        |      | 15        |      | 15        |      | ns    |    |
| t <sub>HZWE</sub>                | $\overline{\text{WE}}$ LOW to High Z <sup>[6, 7]</sup>  |           | 5    |           | 5    |           | 5    |           | 5    |           | 5    | ns    |    |

**Notes:**

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
6. t<sub>HZCE</sub> and t<sub>HZWE</sub> are tested with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
7. At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> for any given device.
8. The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
9.  $\overline{\text{WE}}$  is HIGH for read cycle.
10. Device is continuously selected,  $\overline{\text{CE}} = V_{IL}$ .
11. Address valid prior to or coincident with  $\overline{\text{CE}}$  transition LOW.
12. 3 ns min. for the CY7C169A.

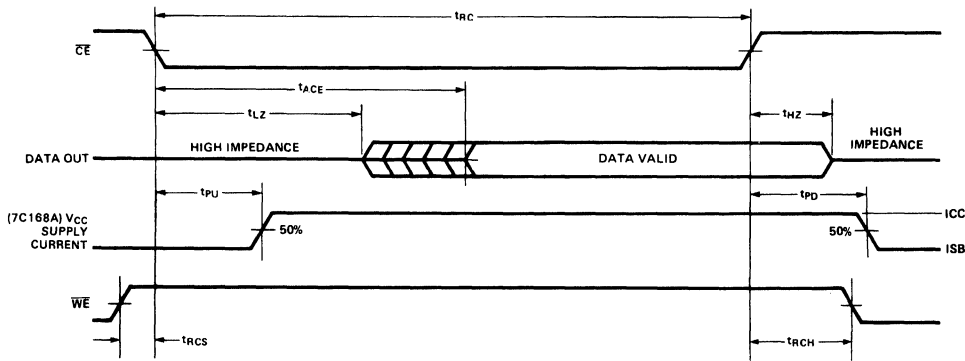
**Switching Waveforms**

**Read Cycle No. 1 (Notes 9, 10)**



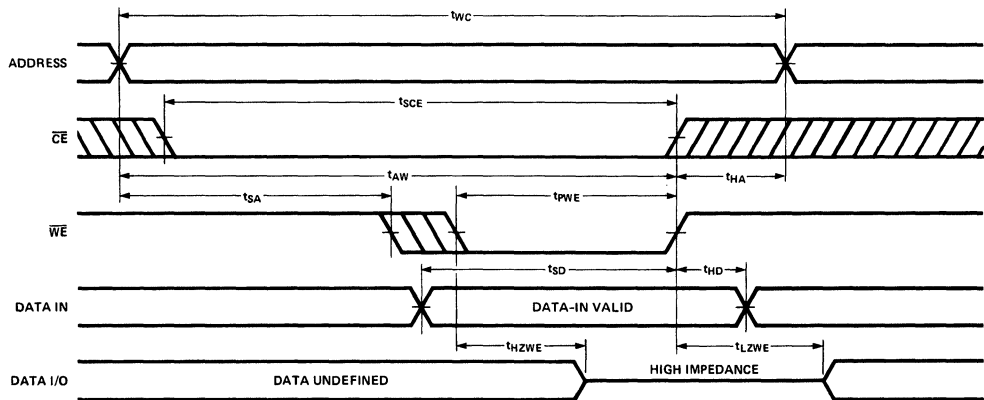
## Switching Waveforms (Continued)

### Read Cycle (Notes 9, 11)



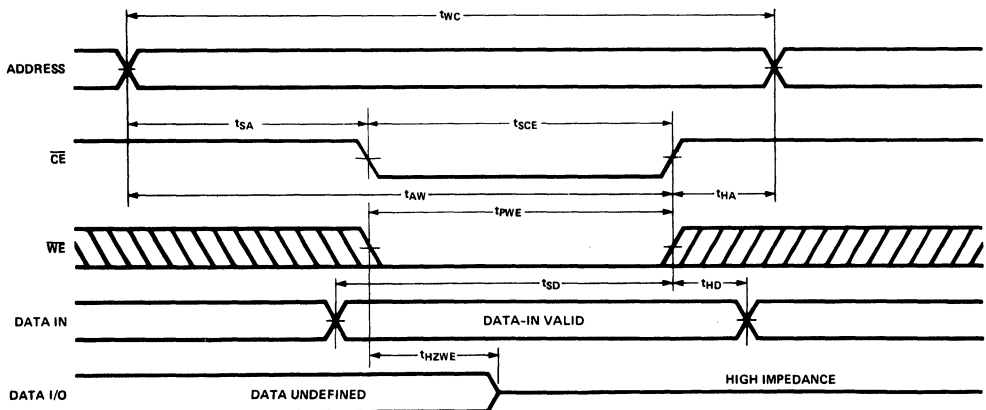
0162-8

### Write Cycle No. 1 ( $\overline{WE}$ Controlled) (Note 8)



0162-9

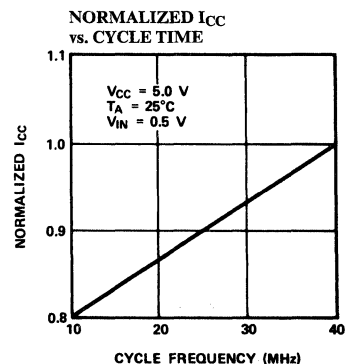
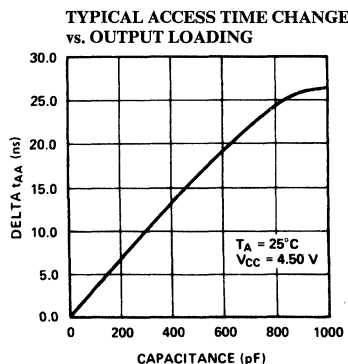
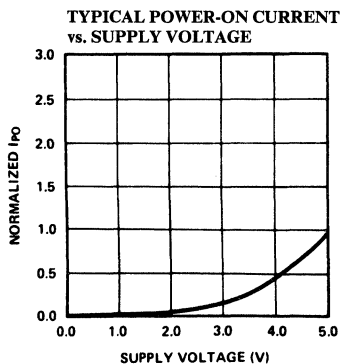
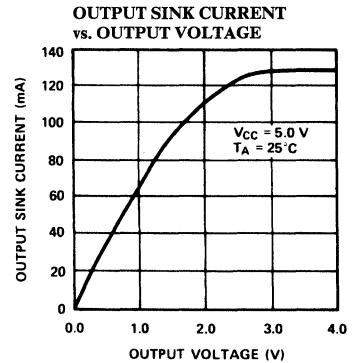
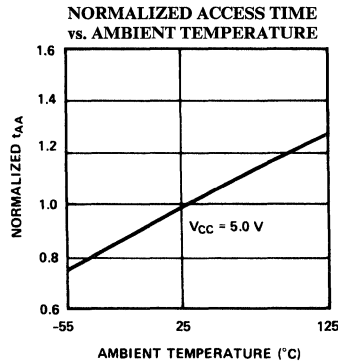
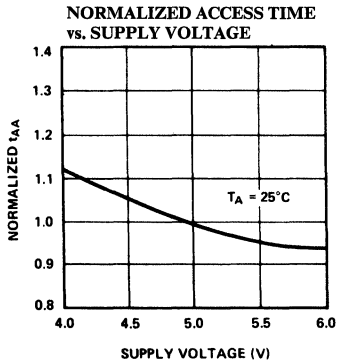
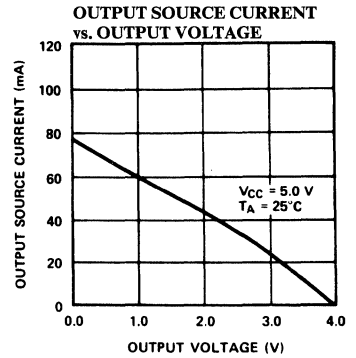
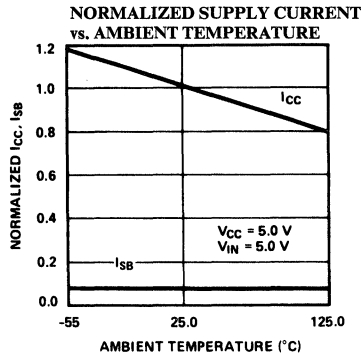
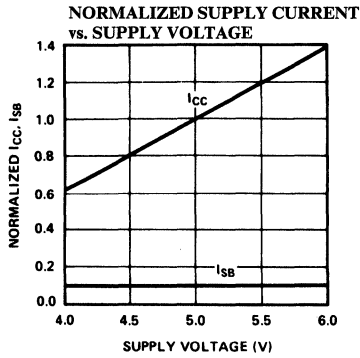
### Write Cycle No. 2 ( $\overline{CE}$ Controlled) (Note 8)



Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

0162-10

Typical DC and AC Characteristics



**Ordering Information**

| Speed (ns) | ICC mA | Ordering Code  | Package Type | Operating Range |
|------------|--------|----------------|--------------|-----------------|
| 20         | 90     | CY7C168A-20PC  | P5           | Commercial      |
|            |        | CY7C168A-20DC  | D6           |                 |
|            |        | CY7C168A-20VC  | V5           |                 |
| 25         | 90     | CY7C168A-25PC  | P5           | Commercial      |
|            |        | CY7C168A-25DC  | D6           |                 |
|            |        | CY7C168A-25LC  | L51          |                 |
|            |        | CY7C168A-25VC  | V5           |                 |
|            |        | CY7C168A-25DMB | D6           | Military        |
|            |        | CY7C168A-25LMB | L51          |                 |
| 35         | 90     | CY7C168A-35PC  | P5           | Commercial      |
|            |        | CY7C168A-35DC  | D6           |                 |
|            |        | CY7C168A-35LC  | L51          |                 |
|            |        | CY7C168A-35VC  | V5           |                 |
|            |        | CY7C168A-35DMB | D6           | Military        |
|            |        | CY7C168A-35LMB | L51          |                 |
| 45         | 70     | CY7C168A-45PC  | P5           | Commercial      |
|            |        | CY7C168A-45DC  | D6           |                 |
|            |        | CY7C168A-45LC  | L51          |                 |
|            |        | CY7C168A-45VC  | V5           |                 |
|            |        | CY7C168A-45DMB | D6           | Military        |
|            |        | CY7C168A-45LMB | L51          |                 |

| Speed (ns) | ICC mA | Ordering Code  | Package Type | Operating Range |
|------------|--------|----------------|--------------|-----------------|
| 20         | 90     | CY7C169A-20PC  | P5           | Commercial      |
|            |        | CY7C169A-20DC  | D6           |                 |
|            |        | CY7C169A-20VC  | V5           |                 |
| 25         | 90     | CY7C169A-25PC  | P5           | Commercial      |
|            |        | CY7C169A-25DC  | D6           |                 |
|            |        | CY7C169A-25LC  | L51          |                 |
|            |        | CY7C169A-25VC  | V5           |                 |
|            |        | CY7C169A-25DMB | D6           | Military        |
|            |        | CY7C169A-25LMB | L51          |                 |
| 35         | 90     | CY7C169A-35PC  | P5           | Commercial      |
|            |        | CY7C169A-35DC  | D6           |                 |
|            |        | CY7C169A-35LC  | L51          |                 |
|            |        | CY7C169A-35VC  | V5           |                 |
|            |        | CY7C169A-35DMB | D6           | Military        |
|            |        | CY7C169A-35LMB | L51          |                 |
| 40         | 70     | CY7C169A-40PC  | P5           | Commercial      |
|            |        | CY7C169A-40DC  | D6           |                 |
|            |        | CY7C169A-40LC  | L51          |                 |
|            |        | CY7C169A-40VC  | V5           |                 |
|            |        | CY7C169A-40DMB | D6           | Military        |
|            |        | CY7C169A-40LMB | L51          |                 |

2

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters                       | Subgroups |
|----------------------------------|-----------|
| V <sub>OH</sub>                  | 1,2,3     |
| V <sub>OL</sub>                  | 1,2,3     |
| V <sub>IH</sub>                  | 1,2,3     |
| V <sub>IL</sub> Max.             | 1,2,3     |
| I <sub>Ix</sub>                  | 1,2,3     |
| I <sub>OZ</sub>                  | 1,2,3     |
| I <sub>CC</sub>                  | 1,2,3     |
| I <sub>SB1</sub> <sup>[12]</sup> | 1,2,3     |
| I <sub>SB2</sub> <sup>[12]</sup> | 1,2,3     |

Note:  
12. 7C168A only.

#### Switching Characteristics

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>ACE</sub>   | 7,8,9,10,11 |
| t <sub>RCS</sub>   | 7,8,9,10,11 |
| t <sub>RCH</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>SCE</sub>   | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |

Document #: 38-00095



**Features**

- CMOS for optimum speed/power
- High speed
  - 25 ns  $t_{AA}$
  - 15 ns  $t_{ACS}$
- Low active power
  - 495 mW (commercial)
  - 660 mW (military)
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge
- Output enable

**Functional Description**

The CY7C170 is a high performance CMOS static RAM organized as 4096 words x 4 bits. Easy memory expansion is provided by an active LOW chip select ( $\overline{CS}$ ), an active LOW output enable ( $\overline{OE}$ ), and three-state drivers.

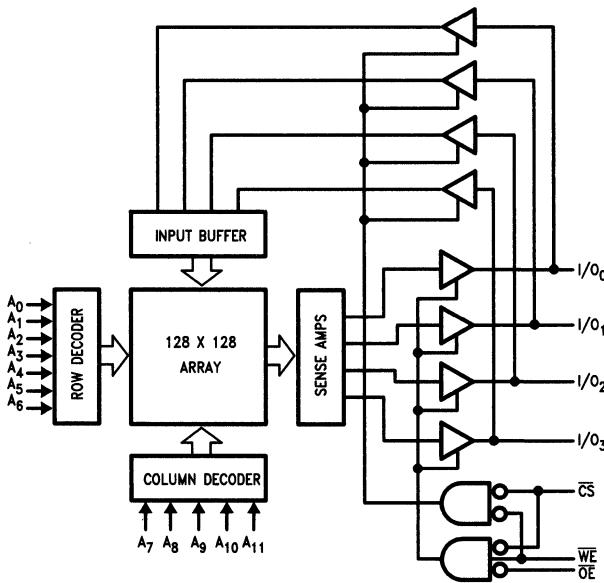
Writing to the device is accomplished when the chip select ( $\overline{CS}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the four input/output pins ( $I/O_0$  through  $I/O_3$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{11}$ ).

Reading the device is accomplished by taking chip select ( $\overline{CS}$ ) and output enable ( $\overline{OE}$ ) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high impedance state when chip select ( $\overline{CS}$ ) or output enable ( $\overline{OE}$ ) is HIGH, or write enable ( $\overline{WE}$ ) is LOW.

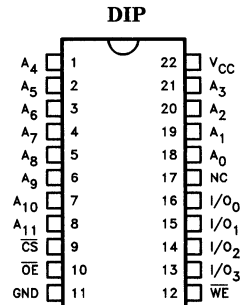
A die coat is used to insure alpha immunity.

**Logic Block Diagram**

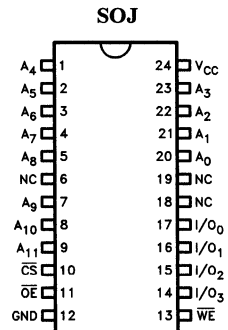


0037-1

**Pin Configurations**



0037-2



0037-12

Figure 1

**Selection Guide**

|                                |            | 7C170-25 | 7C170-35 | 7C170-45 |
|--------------------------------|------------|----------|----------|----------|
| Maximum Access Time (ns)       |            | 25       | 35       | 45       |
| Maximum Operating Current (mA) | Commercial | 90       | 90       | 90       |
|                                | Military   |          | 120      | 120      |



### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential  
(Pin 22 to Pin 11) ..... -0.5V to +7.0V

DC Voltage Applied to Outputs  
in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... > 2001V  
(Per MIL-STD-883 Method 3015)

Latch-up Current ..... > 200 mA

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[4]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[3]</sup>

| Parameters      | Description                                    | Test Conditions   | 7C170      |                 | Units |
|-----------------|--|---|------------|-----------------|-------|
|                 |  |   | Min.       | Max.            |       |
| V <sub>OH</sub> | Output HIGH Voltage                            | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA         | 2.4        |                 | V     |
| V <sub>OL</sub> | Output LOW Voltage                             | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA          |            | 0.4             | V     |
| V <sub>IH</sub> | Input HIGH Voltage                             |   | 2.0        | V <sub>CC</sub> | V     |
| V <sub>IL</sub> | Input LOW Voltage                              |   | -3.0       | 0.8             | V     |
| I <sub>IX</sub> | Input Load Current                             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                    | -10        | +10             | μA    |
| I <sub>OZ</sub> | Output Leakage Current                         | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub><br>Output Disabled | -50        | +50             | μA    |
| I <sub>OS</sub> | Output Short <sup>[1]</sup><br>Circuit Current | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND            |            | -350            | mA    |
| I <sub>CC</sub> | V <sub>CC</sub> Operating<br>Supply Current    | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA         | Commercial | 90              | mA    |
|                 |  |   | Military*  | 120             |       |

\*-25, -35 and -45 only

### Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions                  | Max. | Units |
|------------------|--------------------|----------------------------------|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz | 4    | pF    |
| C <sub>OUT</sub> | Output Capacitance | V <sub>CC</sub> = 5.0V           | 7    |       |

#### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- See the last page of this specification for Group A subgroup testing information.
- T<sub>A</sub> is the "instant on" case temperature.

### AC Test Loads and Waveforms

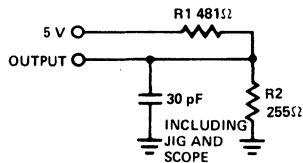


Figure 1a

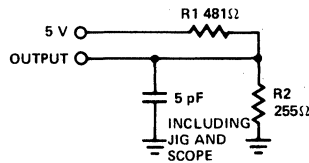


Figure 1b

0037-4

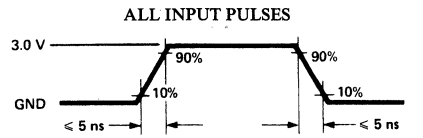
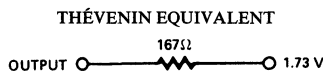


Figure 2

0037-6

Equivalent to:



0037-5

Switching Characteristics Over Operating Range<sup>[3, 5]</sup>

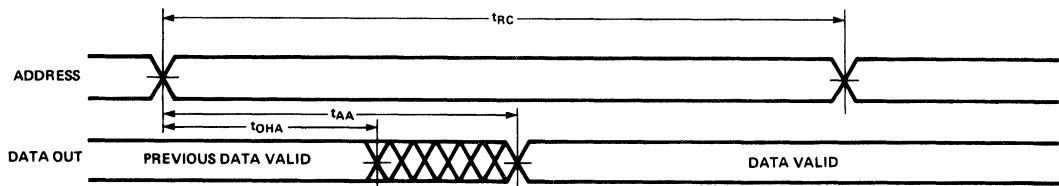
| Parameters                       | Description                         | 7C170-25 |      | 7C170-35 |      | 7C170-45 |      | Units |
|----------------------------------|-------------------------------------|----------|------|----------|------|----------|------|-------|
|                                  |                                     | Min.     | Max. | Min.     | Max. | Min.     | Max. |       |
| <b>READ CYCLE</b>                |                                     |          |      |          |      |          |      |       |
| t <sub>RC</sub>                  | Read Cycle Time                     | 25       |      | 35       |      | 45       |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid               |          | 25   |          | 35   |          | 45   | ns    |
| t <sub>OHA</sub>                 | Data Hold from Address Change       | 3        |      | 3        |      | 3        |      | ns    |
| t <sub>ACS</sub>                 | CS Low to Data Valid                |          | 15   |          | 25   |          | 30   | ns    |
| t <sub>DOE</sub>                 | OE LOW to Data Valid                |          | 15   |          | 15   |          | 20   | ns    |
| t <sub>LZOE</sub>                | OE LOW to Low Z                     | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>HZOE</sub>                | OE HIGH to High Z <sup>[6]</sup>    |          | 15   |          | 15   |          | 15   | ns    |
| t <sub>LZCS</sub>                | CS LOW to Low Z <sup>[7]</sup>      | 3        |      | 5        |      | 5        |      | ns    |
| t <sub>HZCS</sub>                | CE HIGH to High Z <sup>[6, 7]</sup> |          | 15   |          | 20   |          | 25   | ns    |
| <b>WRITE CYCLE<sup>[8]</sup></b> |                                     |          |      |          |      |          |      |       |
| t <sub>WC</sub>                  | Write Cycle Time                    | 25       |      | 35       |      | 40       |      | ns    |
| t <sub>SCS</sub>                 | CS LOW to Write End                 | 25       |      | 35       |      | 35       |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End         | 20       |      | 30       |      | 35       |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End         | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start       | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>PWE</sub>                 | WE Pulse Width                      | 20       |      | 30       |      | 35       |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End            | 10       |      | 15       |      | 15       |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End            | 0        |      | 0        |      | 3        |      | ns    |
| t <sub>HZWE</sub>                | WE LOW to High Z                    |          | 10   |          | 15   |          | 20   | ns    |
| t <sub>LZWE</sub>                | WE HIGH to Low Z                    | 6        |      | 6        |      | 6        |      | ns    |

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCS</sub> and t<sub>HZWE</sub> are tested with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for all devices. These parameters are sampled and not 100% tested.
- The internal write time of the memory is defined by the overlap of CS LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- WE is HIGH for read cycle.
- Device is continuously selected, CS = V<sub>IL</sub> and OE = V<sub>IL</sub>.
- Address valid prior to or coincident with CS transition LOW.
- Data I/O will be high impedance if OE = V<sub>IH</sub>.

Switching Waveforms

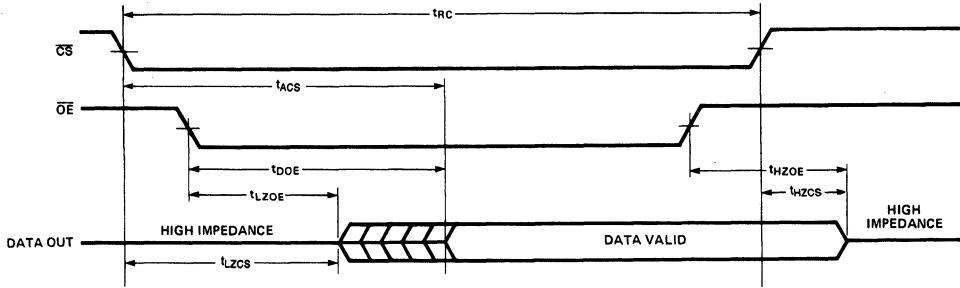
Read Cycle No. 1 (Notes 9, 10)



0037-11

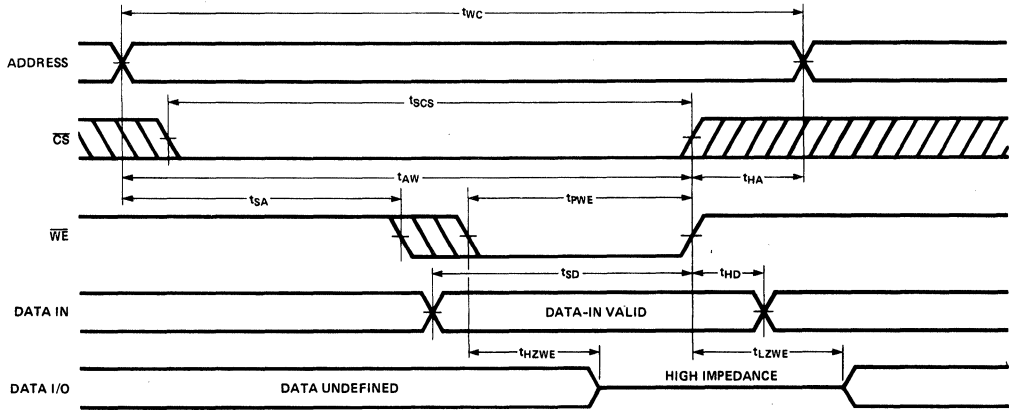
Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 9, 11)



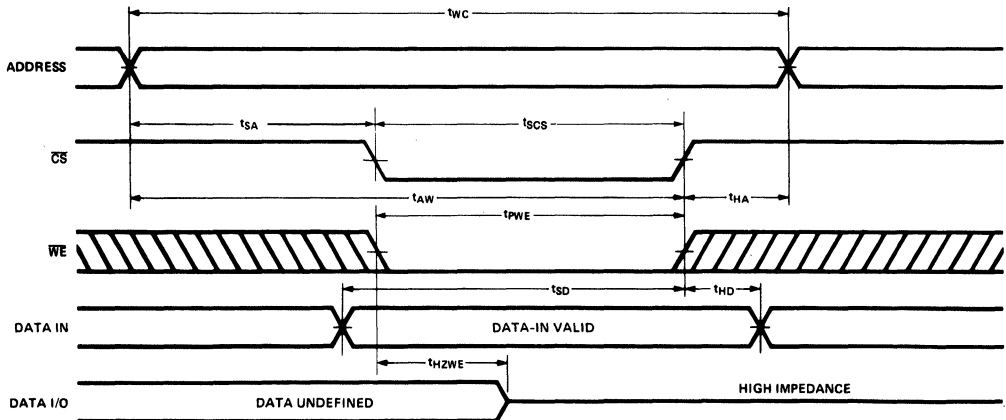
0037-7

Write Cycle No. 1 ( $\overline{WE}$  Controlled) (Notes 8, 12)



0037-8

Write Cycle No. 2 ( $\overline{CS}$  Controlled) (Notes 8, 12)



0037-9

Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C170-25PC  | P9           | Commercial      |
|            | CY7C170-25DC  | D10          |                 |
|            | CY7C170-25VC  | V13          |                 |
| 35         | CY7C170-35PC  | P9           | Commercial      |
|            | CY7C170-35DC  | D10          |                 |
|            | CY7C170-35VC  | V13          |                 |
|            | CY7C170-35DMB | D10          | Military        |
| 45         | CY7C170-45PC  | P9           | Commercial      |
|            | CY7C170-45DC  | D10          |                 |
|            | CY7C170-45VC  | V13          |                 |
|            | CY7C170-45DMB | D10          | Military        |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL</sub> Max. | 1,2,3     |
| I <sub>I</sub> X     | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |

**Switching Characteristics**

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>ACS</sub>   | 7,8,9,10,11 |
| t <sub>DOE</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>SCS</sub>   | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |

Document #: 38-00035-E



**Features**

- CMOS for optimum speed/power
- High speed
  - 20 ns  $t_{AA}$
  - 15 ns  $t_{ACS}$
- Low active power
  - 495 mW (commercial)
  - 660 mW (military)
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge
- Output enable
- $V_{IH}$  of 2.2V

**Functional Description**

The CY7C170A is a high performance CMOS static RAM organized as 4096 words x 4 bits. Easy memory expansion is provided by an active LOW chip select ( $\overline{CS}$ ), an active LOW output enable ( $\overline{OE}$ ), and three-state drivers.

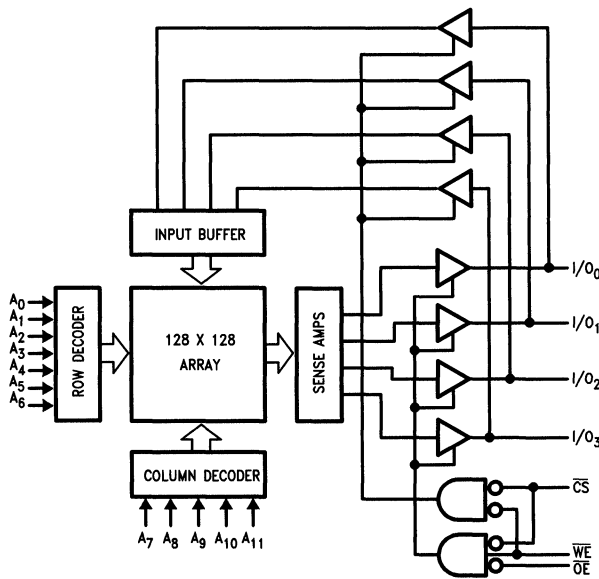
Writing to the device is accomplished when the chip select ( $\overline{CS}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the four input/output pins ( $I/O_0$  through  $I/O_3$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{11}$ ).

Reading the device is accomplished by taking chip select ( $\overline{CS}$ ) and output enable ( $\overline{OE}$ ) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high impedance state when chip select ( $\overline{CS}$ ) or output enable ( $\overline{OE}$ ) is HIGH, or write enable ( $\overline{WE}$ ) is LOW.

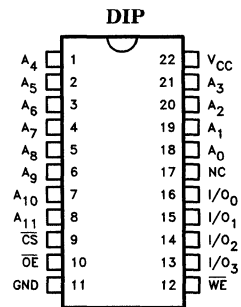
A die coat is used to insure alpha immunity.

**Logic Block Diagram**

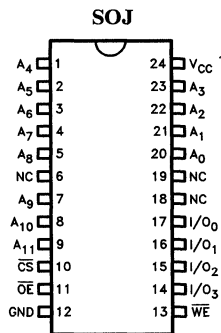


0149-1

**Pin Configurations**



0149-2



0149-3

**Figure 1**

**Selection Guide**

|                                |            | 7C170A-20 | 7C170A-25 | 7C170A-35 | 7C170A-45 |
|--------------------------------|------------|-----------|-----------|-----------|-----------|
| Maximum Access Time (ns)       |            | 20        | 25        | 35        | 45        |
| Maximum Operating Current (mA) | Commercial | 90        | 90        | 90        | 90        |
|                                | Military   |           | 120       | 120       | 120       |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|  |                 |
|--|-----------------|
| Storage Temperature .....                                      | -65°C to +150°C |
| Ambient Temperature with<br>Power Applied .....                | -55°C to +125°C |
| Supply Voltage to Ground Potential<br>(Pin 22 to Pin 11) ..... | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs<br>in High Z State .....         | -0.5V to +7.0V  |
| DC Input Voltage .....   | -3.0V to +7.0V  |
| Output Current into Outputs (Low) .....                        | 20 mA           |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | > 2001V<br>(Per MIL-STD-883 Method 3015) |
| Latch-up Current .....         | > 200 mA                                 |

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ±10%         |
| Military <sup>[4]</sup> | -55°C to +125°C     | 5V ±10%         |

### Electrical Characteristics Over Operating Range<sup>[3]</sup>

| Parameters      | Description                                    | Test Conditions   | 7C170A     |                 | Units |
|-----------------|--|---|------------|-----------------|-------|
|                 |  |   | Min.       | Max.            |       |
| V <sub>OH</sub> | Output HIGH Voltage                            | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA         | 2.4        |                 | V     |
| V <sub>OL</sub> | Output LOW Voltage                             | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA          |            | 0.4             | V     |
| V <sub>IH</sub> | Input HIGH Voltage                             |   | 2.2        | V <sub>CC</sub> | V     |
| V <sub>IL</sub> | Input LOW Voltage                              |   | -3.0       | 0.8             | V     |
| I <sub>IX</sub> | Input Load Current                             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                    | -10        | +10             | μA    |
| I <sub>OZ</sub> | Output Leakage Current                         | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub><br>Output Disabled | -10        | +10             | μA    |
| I <sub>OS</sub> | Output Short <sup>[1]</sup><br>Circuit Current | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND            |            | -350            | mA    |
| I <sub>CC</sub> | V <sub>CC</sub> Operating<br>Supply Current    | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA         | Commercial | 90              | mA    |
|                 |  |   | Military*  | 120             |       |

\*-25, -35 and -45 only

### Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 4    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 7    |       |

#### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- See the last page of this specification for Group A subgroup testing information.
- T<sub>A</sub> is the "instant on" case temperature.

### AC Test Loads and Waveforms

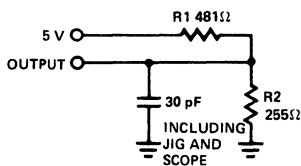


Figure 1a

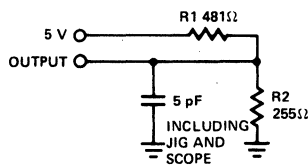


Figure 1b

0149-4

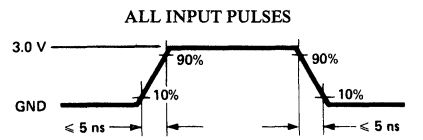
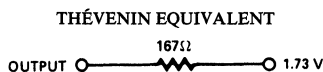


Figure 2

0149-6

Equivalent to:



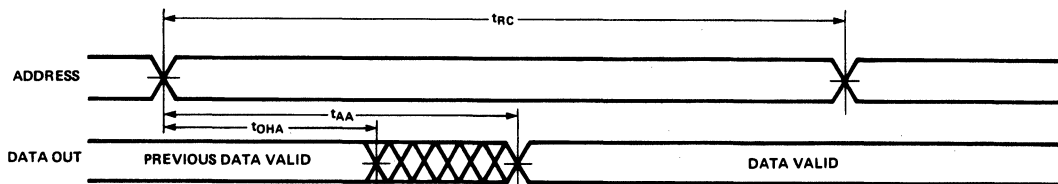
0149-5

**Switching Characteristics Over Operating Range<sup>[3, 5]</sup>**

| Parameters                       | Description                                      | 7C170A-20 |      | 7C170A-25 |      | 7C170A-35 |      | 7C170A-45 |      | Units |
|----------------------------------|--|-----------|------|-----------|------|-----------|------|-----------|------|-------|
|                                  |  | Min.      | Max. | Min.      | Max. | Min.      | Max. | Min.      | Max. |       |
| <b>READ CYCLE</b>                |  |           |      |           |      |           |      |           |      |       |
| t <sub>RC</sub>                  | Read Cycle Time                                  | 20        |      | 25        |      | 35        |      | 45        |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid                            |           | 20   |           | 25   |           | 35   |           | 45   | ns    |
| t <sub>OHA</sub>                 | Data Hold from Address Change                    | 5         |      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>ACS</sub>                 | $\overline{CS}$ Low to Data Valid                |           | 15   |           | 15   |           | 25   |           | 30   | ns    |
| t <sub>DOE</sub>                 | $\overline{OE}$ LOW to Data Valid                |           | 10   |           | 12   |           | 15   |           | 20   | ns    |
| t <sub>LZOE</sub>                | $\overline{OE}$ LOW to Low Z                     | 3         |      | 3         |      | 3         |      | 3         |      | ns    |
| t <sub>HZOE</sub>                | $\overline{OE}$ HIGH to High Z <sup>[6]</sup>    |           | 8    |           | 10   |           | 12   |           | 15   | ns    |
| t <sub>LZCS</sub>                | $\overline{CS}$ LOW to Low Z <sup>[7]</sup>      | 5         |      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>HZCS</sub>                | $\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup> |           | 8    |           | 10   |           | 15   |           | 15   | ns    |
| <b>WRITE CYCLE<sup>[8]</sup></b> |  |           |      |           |      |           |      |           |      |       |
| t <sub>WC</sub>                  | Write Cycle Time                                 | 20        |      | 20        |      | 25        |      | 40        |      | ns    |
| t <sub>SCS</sub>                 | $\overline{CS}$ LOW to Write End                 | 15        |      | 20        |      | 25        |      | 30        |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End                      | 15        |      | 20        |      | 25        |      | 30        |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End                      | 0         |      | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                    | 0         |      | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>PWE</sub>                 | WE Pulse Width                                   | 15        |      | 15        |      | 20        |      | 20        |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End                         | 10        |      | 10        |      | 15        |      | 15        |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End                         | 0         |      | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>HZWE</sub>                | $\overline{WE}$ LOW to High Z                    |           | 7    |           | 7    |           | 10   |           | 15   | ns    |
| t <sub>LZWE</sub>                | $\overline{WE}$ HIGH to Low Z                    | 5         |      | 5         |      | 5         |      | 5         |      | ns    |

**Notes:**

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCS</sub> and t<sub>HZWE</sub> are tested with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for all devices. These parameters are sampled and not 100% tested.
- The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CS} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{CS}$  transition LOW.
- Data I/O will be high impedance if  $\overline{OE} = V_{IH}$ .

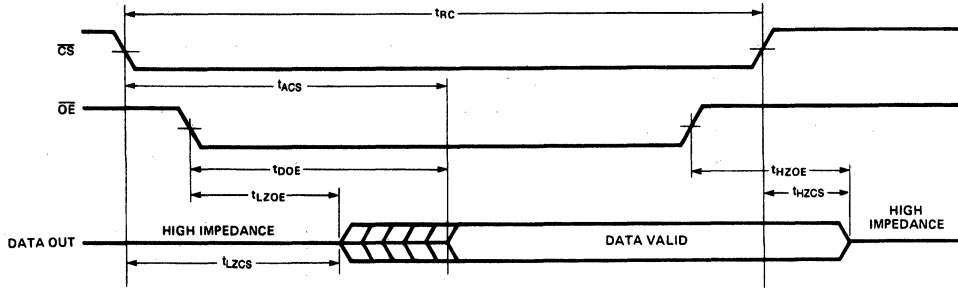
**Switching Waveforms**
**Read Cycle No. 1 (Notes 9, 10)**


0149-7



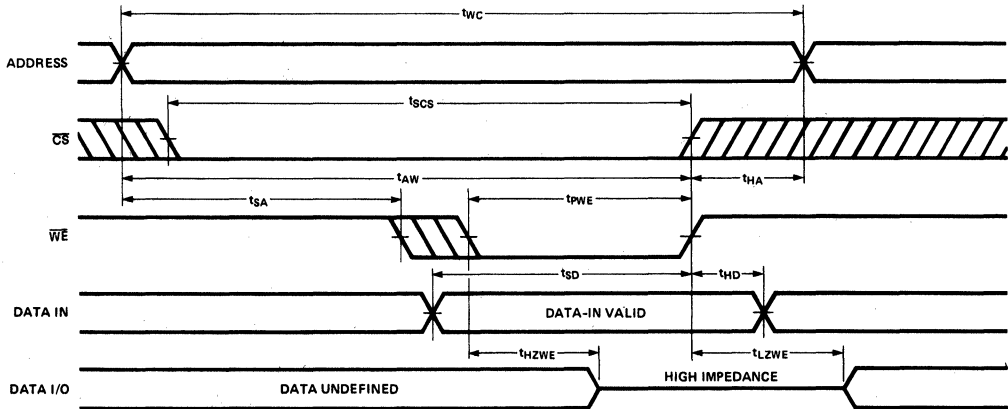
Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 9, 11)



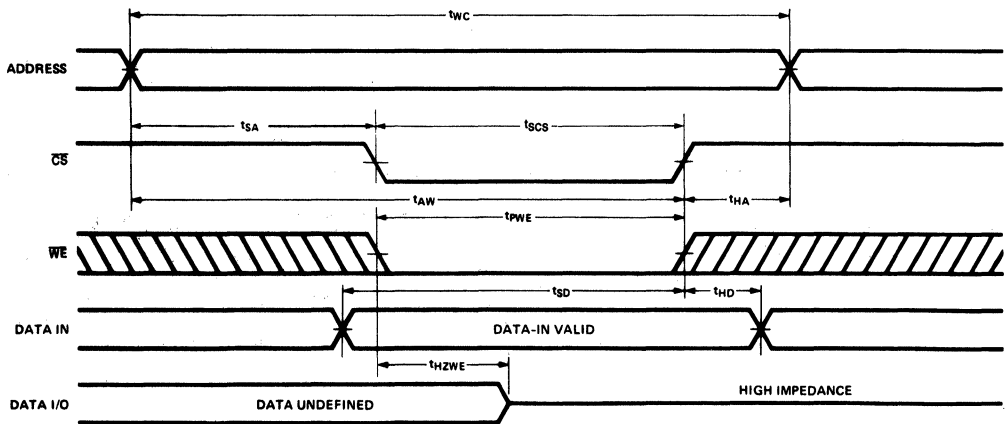
0149-8

Write Cycle No. 1 ( $\overline{WE}$  Controlled) (Notes 8, 12)



0149-9

Write Cycle No. 2 ( $\overline{CS}$  Controlled) (Notes 8, 12)



0149-10

Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

## Ordering Information

| Speed (ns) | Ordering Code  | Package Type | Operating Range |
|------------|----------------|--------------|-----------------|
| 20         | CY7C170A-20PC  | P9           | Commercial      |
|            | CY7C170A-20DC  | D10          |                 |
|            | CY7C170A-20VC  | V13          |                 |
| 25         | CY7C170A-25PC  | P9           | Commercial      |
|            | CY7C170A-25DC  | D10          |                 |
|            | CY7C170A-25VC  | V13          |                 |
|            | CY7C170A-25DMB | D10          | Military        |
| 35         | CY7C170A-35PC  | P9           | Commercial      |
|            | CY7C170A-35DC  | D10          |                 |
|            | CY7C170A-35VC  | V13          |                 |
|            | CY7C170A-35DMB | D10          | Military        |
| 45         | CY7C170A-45PC  | P9           | Commercial      |
|            | CY7C170A-45DC  | D10          |                 |
|            | CY7C170A-45VC  | V13          |                 |
|            | CY7C170A-45DMB | D10          | Military        |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |

**Switching Characteristics**

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>ACS</sub>   | 7,8,9,10,11 |
| t <sub>DOE</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>SCS</sub>   | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |

Document #: 38-00096



**Features**

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed  
— 25 ns  $t_{AA}$
- Transparent Write (7C171)
- Low active power  
— 385 mW
- Low standby power  
— 83 mW
- TTL compatible inputs and outputs

- Capable of withstanding greater than 2001V electrostatic discharge

**Functional Description**

The CY7C171 and CY7C172 are high performance CMOS static RAMs organized as 4096 x 4 bits with separate I/O. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 77% when deselected.

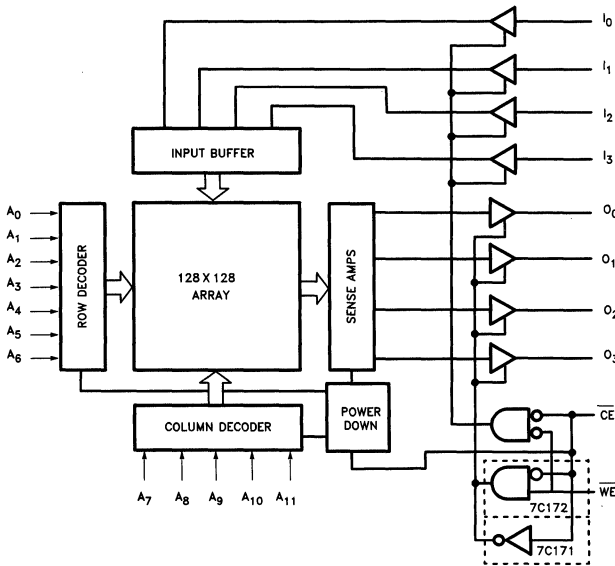
Writing to the device is accomplished when the chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW.

Data on the four input pins ( $I_0$  through  $I_3$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{11}$ ).

Reading the device is accomplished by taking chip enable ( $\overline{CE}$ ) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

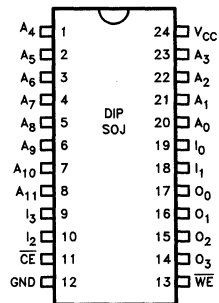
The output pins stay in high impedance state when write enable ( $\overline{WE}$ ) is LOW (7C172 only), or chip enable ( $\overline{CE}$ ) is HIGH. A die coat is used to insure alpha immunity.

**Logic Block Diagram**

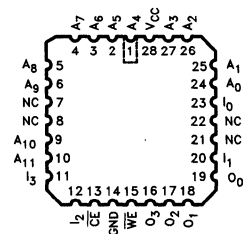


0051-1

**Pin Configurations**



0051-2



0051-3

**Selection Guide**

|                                |     | 7C171-25<br>7C172-25 | 7C171-35<br>7C172-35 | 7C171-45<br>7C172-45 |
|--------------------------------|-----|----------------------|----------------------|----------------------|
| Maximum Access Time (ns)       |     | 25                   | 35                   | 45                   |
| Maximum Operating Current (mA) | STD | Commercial           | 90                   | 70                   |
|                                |     | Military             | 90                   | 70                   |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|  |                 |
|--|-----------------|
| Storage Temperature .....                                  | -65°C to +150°C |
| Ambient Temperature with Power Applied .....               | -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 24 to Pin 12)..... | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State.....         | -0.5V to +7.0V  |
| DC Input Voltage .....                                     | -3.0V to +7.0V  |
| Output Current into Outputs (Low) .....                    | 20 mA           |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | > 2001V<br>(Per MIL-STD-883 Method 3015) |
| Latch-up Current.....          | > 200 mA                                 |

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[2]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[3]</sup>

| Parameters       | Description                                  | Test Conditions   | 7C171-25<br>7C172-25 |      | 7C171-35<br>7C172-35 |      | 7C171-45<br>7C172-45 |      | Units |
|------------------|--|---|----------------------|------|----------------------|------|----------------------|------|-------|
|                  |  |   | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. |       |
| V <sub>OH</sub>  | Output HIGH Voltage                          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA           | 2.4                  |      | 2.4                  |      | 2.4                  |      | V     |
| V <sub>OL</sub>  | Output LOW Voltage                           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA            |                      | 0.4  |                      | 0.4  |                      | 0.4  | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                           |   | 2.2                  |      | 2.2                  |      | 2.2                  |      | V     |
| V <sub>IL</sub>  | Input LOW Voltage                            |   | -3.0                 | 0.8  | -3.0                 | 0.8  | -3.0                 | 0.8  | V     |
| I <sub>IX</sub>  | Input Load Current                           | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                      | -10                  | +10  | -10                  | +10  | -10                  | +10  | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                       | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> ,<br>Output Disabled | -50                  | +50  | -50                  | +50  | -50                  | +50  | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>  | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND              |                      | -350 |                      | -350 |                      | -350 | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current     | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA           | Commercial           | 90   | 90                   | 90   | 70                   | mA   |       |
|                  |  |   | Military             | 90   | 90                   | 90   | 70                   | mA   |       |
| I <sub>SB1</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> ,<br>CE ≥ V <sub>IH</sub>              | Commercial           | 20   | 20                   | 20   | 15                   | mA   |       |
|                  |  |   | Military             | 40   | 40                   | 20   | 20                   | mA   |       |
| I <sub>SB2</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> ,<br>CE ≥ V <sub>CC</sub> - 0.3V       | Commercial           | 15   | 15                   | 15   | 15                   | mA   |       |
|                  |  |   | Military             | 20   | 20                   | 20   | 20                   | mA   |       |

### Capacitance<sup>[4]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 4    | pF    |
| C <sub>OUT</sub> | Output Capacitance | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 7    | pF    |

#### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.

### AC Test Loads and Waveforms

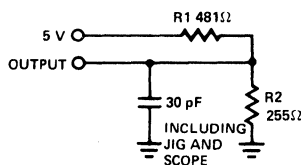


Figure 1a

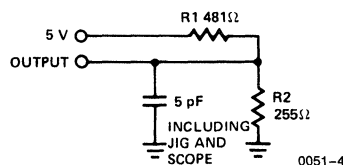


Figure 1b

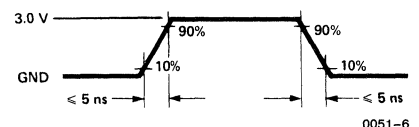
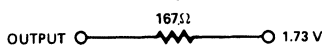


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



0051-5

## Switching Characteristics Over Operating Range<sup>[3, 5]</sup>

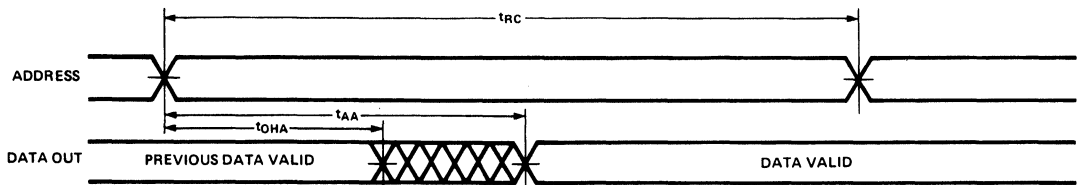
| Parameters                       | Description   | 7C171-25<br>7C172-25 |      | 7C171-35<br>7C172-35 |      | 7C171-45<br>7C172-45 |      | Units |
|----------------------------------|---|----------------------|------|----------------------|------|----------------------|------|-------|
|                                  |   | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. |       |
| <b>READ CYCLE</b>                |   |                      |      |                      |      |                      |      |       |
| t <sub>RC</sub>                  | Read Cycle Time   | 25                   |      | 35                   |      | 45                   |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid                                   |                      | 25   |                      | 35   |                      | 45   | ns    |
| t <sub>OHA</sub>                 | Output Hold from Address Change                         | 3                    |      | 3                    |      | 3                    |      | ns    |
| t <sub>ACE</sub>                 | $\overline{CE}$ LOW to Data Valid                       |                      | 25   |                      | 35   |                      | 45   | ns    |
| t <sub>LZCE</sub>                | $\overline{CE}$ LOW to Low Z <sup>[7]</sup>             | 5                    |      | 5                    |      | 5                    |      | ns    |
| t <sub>HZCE</sub>                | $\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>        |                      | 15   |                      | 20   |                      | 20   | ns    |
| t <sub>PU</sub>                  | $\overline{CE}$ LOW to Power Up                         | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>PD</sub>                  | $\overline{CE}$ HIGH to Power Down                      |                      | 25   |                      | 25   |                      | 30   | ns    |
| t <sub>RCS</sub>                 | Read Command Set-up                                     | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>RCH</sub>                 | Read Command Hold                                       | 0                    |      | 0                    |      | 0                    |      | ns    |
| <b>WRITE CYCLE<sup>[8]</sup></b> |   |                      |      |                      |      |                      |      |       |
| t <sub>WC</sub>                  | Write Cycle Time  | 25                   |      | 35                   |      | 40                   |      | ns    |
| t <sub>SCE</sub>                 | $\overline{CE}$ LOW to Write End                        | 25                   |      | 30                   |      | 35                   |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End                             | 20                   |      | 30                   |      | 35                   |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End                             | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                           | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>PWE</sub>                 | $\overline{WE}$ Pulse Width                             | 20                   |      | 25                   |      | 30                   |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End                                | 10                   |      | 15                   |      | 15                   |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End                                | 0                    |      | 0                    |      | 3                    |      | ns    |
| t <sub>LZWE</sub>                | $\overline{WE}$ HIGH to Low Z <sup>[7]</sup> (7C172)    | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>HZWE</sub>                | $\overline{WE}$ LOW to High Z <sup>[6, 7]</sup> (7C172) |                      | 10   |                      | 15   |                      | 20   | ns    |
| t <sub>AWE</sub>                 | $\overline{WE}$ LOW to Data Valid (7C171)               |                      | 25   |                      | 30   |                      | 35   | ns    |
| t <sub>ADV</sub>                 | Data Valid to Output Valid (7C171)                      |                      | 25   |                      | 30   |                      | 35   | ns    |

### Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/O<sub>H</sub> and 30 pF load capacitance.
- t<sub>HZCE</sub> and t<sub>HZWE</sub> are tested with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CE} = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

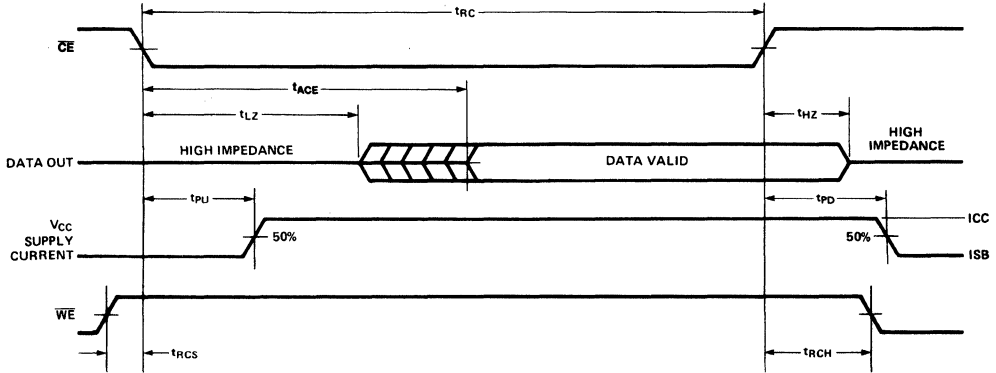
## Switching Waveforms

### Read Cycle No. 1 (Notes 9, 10)



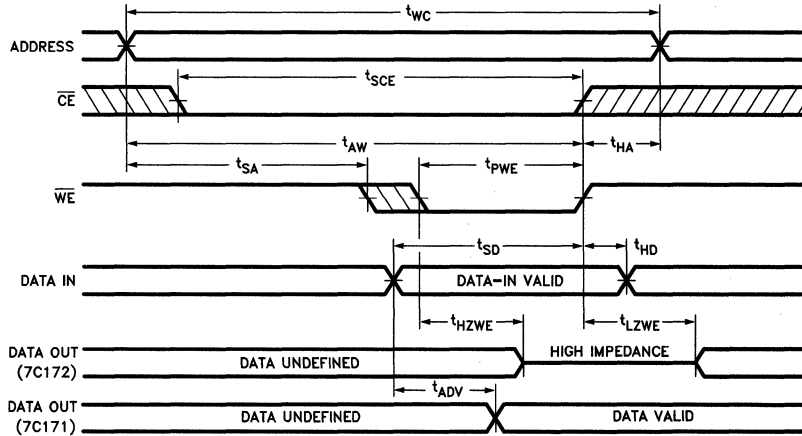
### Switching Waveforms (Continued)

#### Read Cycle (Notes 9, 11)



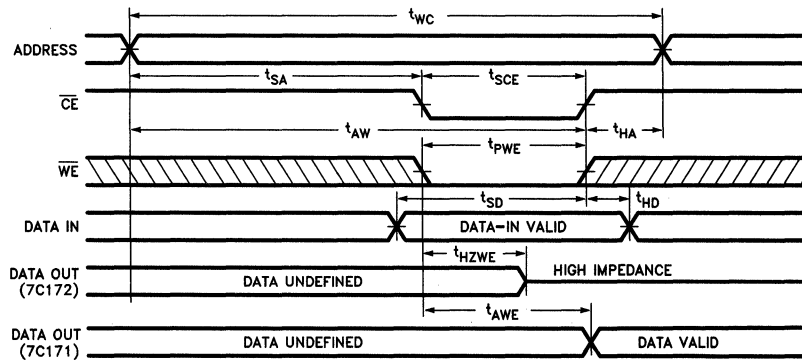
0051-8

#### Write Cycle No. 1 ( $\overline{WE}$ Controlled) (Note 8)



0051-9

#### Write Cycle No. 2 ( $\overline{CE}$ Controlled) (Note 8)

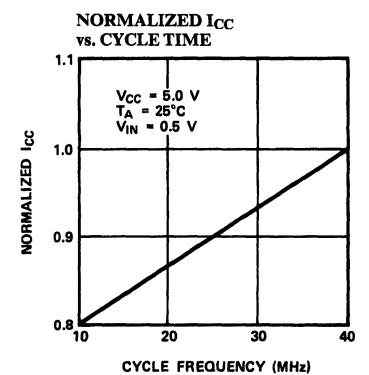
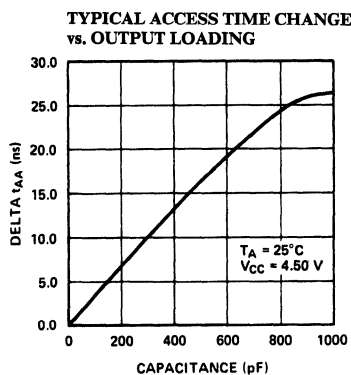
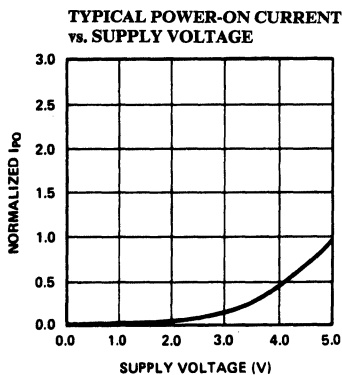
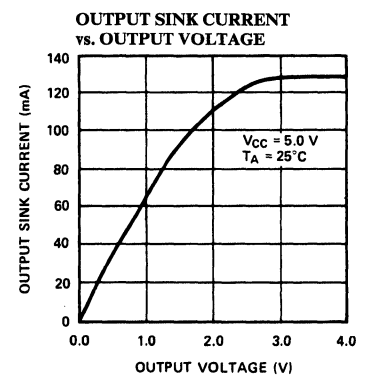
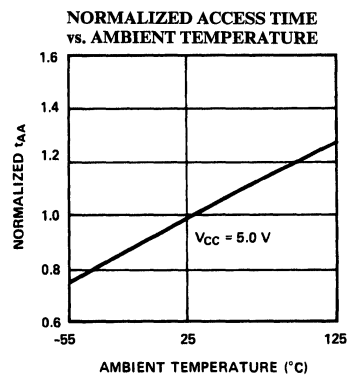
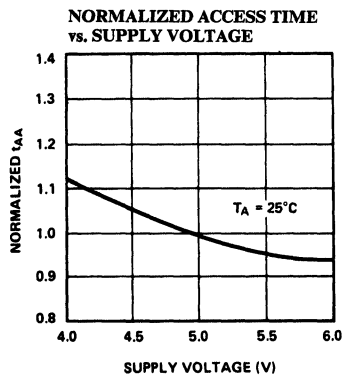
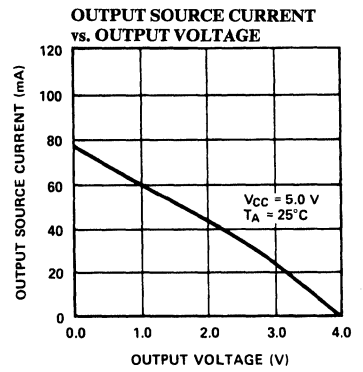
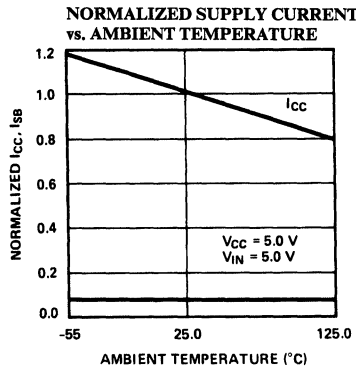
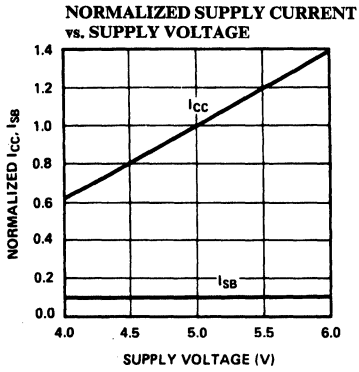


0051-10

Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state (7C172).

Typical DC and AC Characteristics

2





**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C171-25PC  | P13          | Commercial      |
|            | CY7C171-25DC  | D14          |                 |
|            | CY7C171-25LC  | L64          |                 |
|            | CY7C171-25VC  | V13          |                 |
| 35         | CY7C171-35PC  | P13          | Commercial      |
|            | CY7C171-35DC  | D14          |                 |
|            | CY7C171-35LC  | L64          |                 |
|            | CY7C171-35VC  | V13          |                 |
|            | CY7C171-35DMB | D14          | Military        |
|            | CY7C171-35LMB | L64          |                 |
| 45         | CY7C171-45PC  | P13          | Commercial      |
|            | CY7C171-45DC  | D14          |                 |
|            | CY7C171-45LC  | L64          |                 |
|            | CY7C171-45VC  | V13          |                 |
|            | CY7C171-45DMB | D14          | Military        |
|            | CY7C171-45LMB | L64          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C172-25PC  | P13          | Commercial      |
|            | CY7C172-25DC  | D14          |                 |
|            | CY7C172-25LC  | L64          |                 |
|            | CY7C172-25VC  | V13          |                 |
| 35         | CY7C172-35PC  | P13          | Commercial      |
|            | CY7C172-35DC  | D14          |                 |
|            | CY7C172-35LC  | L64          |                 |
|            | CY7C172-35VC  | V13          |                 |
|            | CY7C172-35DMB | D14          | Military        |
|            | CY7C172-35LMB | L64          |                 |
| 45         | CY7C172-45PC  | P13          | Commercial      |
|            | CY7C172-45DC  | D14          |                 |
|            | CY7C172-45LC  | L64          |                 |
|            | CY7C172-45VC  | V13          |                 |
|            | CY7C172-45DMB | D14          | Military        |
|            | CY7C172-45LMB | L64          |                 |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB1</sub>     | 1,2,3     |
| I <sub>SB2</sub>     | 1,2,3     |

**2**
**Switching Characteristics**

| Parameters                       | Subgroups   |
|----------------------------------|-------------|
| <b>READ CYCLE</b>                |             |
| t <sub>RC</sub>                  | 7,8,9,10,11 |
| t <sub>AA</sub>                  | 7,8,9,10,11 |
| t <sub>OHA</sub>                 | 7,8,9,10,11 |
| t <sub>ACE</sub>                 | 7,8,9,10,11 |
| t <sub>RCS</sub>                 | 7,8,9,10,11 |
| t <sub>RCH</sub>                 | 7,8,9,10,11 |
| <b>WRITE CYCLE</b>               |             |
| t <sub>WC</sub>                  | 7,8,9,10,11 |
| t <sub>SCE</sub>                 | 7,8,9,10,11 |
| t <sub>AW</sub>                  | 7,8,9,10,11 |
| t <sub>HA</sub>                  | 7,8,9,10,11 |
| t <sub>SA</sub>                  | 7,8,9,10,11 |
| t <sub>PWE</sub>                 | 7,8,9,10,11 |
| t <sub>SD</sub>                  | 7,8,9,10,11 |
| t <sub>HD</sub>                  | 7,8,9,10,11 |
| t <sub>AWE</sub> <sup>[12]</sup> | 7,8,9,10,11 |
| t <sub>ADV</sub> <sup>[12]</sup> | 7,8,9,10,11 |

**Note:**

12. 7C171 only.

Document #: 38-00036-E



4096 x 4 Static R/W RAM  
Separate I/O

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed  
— 20 ns  $t_{AA}$
- Transparent Write (7C171A)
- Low active power  
— 375 mW
- Low standby power  
— 93 mW
- TTL compatible inputs and outputs

- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C171A and CY7C172A are high performance CMOS static RAMs organized as 4096 x 4 bits with separate I/O. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 77% when deselected.

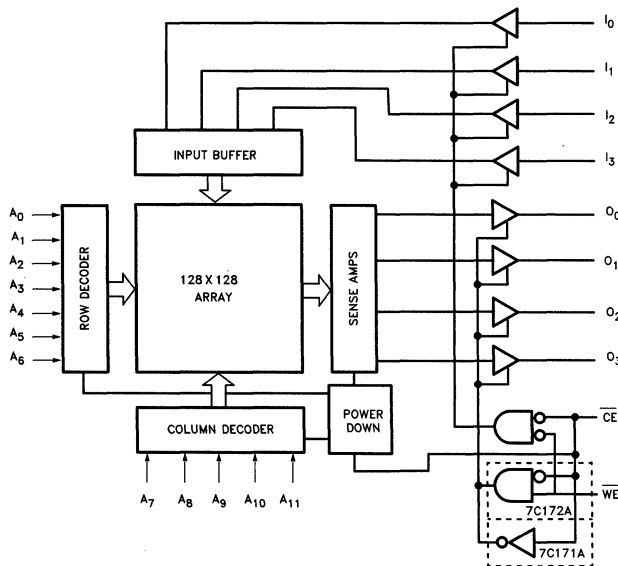
Writing to the device is accomplished when the chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW.

Data on the four input pins ( $I_0$  through  $I_3$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{11}$ ).

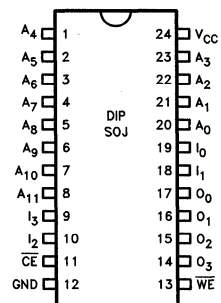
Reading the device is accomplished by taking chip enable ( $\overline{CE}$ ) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

The output pins stay in high impedance state when write enable ( $\overline{WE}$ ) is LOW (7C172A only), or chip enable ( $\overline{CE}$ ) is HIGH. A die coat is used to insure alpha immunity.

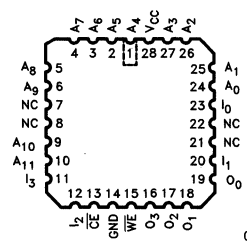
Logic Block Diagram



Pin Configurations



0148-2



0148-3

0148-1

Selection Guide

|                                |          | 7C171A-20<br>7C172A-20 | 7C171A-25<br>7C172A-25 | 7C171A-35<br>7C172A-35 | 7C171A-45<br>7C172A-45 |
|--------------------------------|----------|------------------------|------------------------|------------------------|------------------------|
| Maximum Access Time (ns)       |          | 20                     | 25                     | 35                     | 45                     |
| Maximum Operating Current (mA) | STD      | 80                     | 70                     | 70                     | 50                     |
|                                | Military |                        | 80                     | 70                     | 70                     |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied ..... -55°C to +125°C  
 Supply Voltage to Ground Potential  
 (Pin 24 to Pin 12) ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs  
 in High Z State ..... -0.5V to +7.0V  
 DC Input Voltage ..... -3.0V to +7.0V  
 Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... > 2001V  
 (Per MIL-STD-883 Method 3015)

Latch-up Current ..... > 200 mA

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[2]</sup> | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over Operating Range<sup>[3]</sup>

| Parameters       | Description                                  | Test Conditions   | 7C171A-20 7C172A-20 |      |                     |      |                     |      |      |      | Units |
|------------------|--|---|---------------------|------|---------------------|------|---------------------|------|------|------|-------|
|                  |  |   | 7C171A-25 7C172A-25 |      | 7C171A-35 7C172A-35 |      | 7C171A-45 7C172A-45 |      |      |      |       |
|                  |  |   | Min.                | Max. | Min.                | Max. | Min.                | Max. | Min. | Max. |       |
| V <sub>OH</sub>  | Output HIGH Voltage                          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA   | 2.4                 |      | 2.4                 |      | 2.4                 |      | 2.4  |      | V     |
| V <sub>OL</sub>  | Output LOW Voltage                           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA  |                     | 0.4  |                     | 0.4  |                     | 0.4  |      | 0.4  | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                           |   | 2.2                 |      | 2.2                 |      | 2.2                 |      | 2.2  |      | V     |
| V <sub>IL</sub>  | Input LOW Voltage                            |   | -3.0                | 0.8  | -3.0                | 0.8  | -3.0                | 0.8  | -3.0 | 0.8  | V     |
| I <sub>IX</sub>  | Input Load Current                           | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>  | -10                 | +10  | -10                 | +10  | -10                 | +10  | -10  | +10  | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                       | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> ,<br>Output Disabled   | -10                 | +10  | -10                 | +10  | -10                 | +10  | -10  | +10  | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>  | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND  |                     | -350 |                     | -350 |                     | -350 |      | -350 | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current     | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA   | Commercial          | 80   |                     | 70   |                     | 70   |      | 50   | mA    |
|                  |  |   | Military            |      |                     | 80   |                     | 70   |      | 70   |       |
| I <sub>SB1</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$<br>Min. Duty Cycle = 100%  | Commercial          | 40   |                     | 20   |                     | 20   |      | 20   | mA    |
|                  |  |   | Military            |      |                     | 20   |                     | 20   |      | 20   |       |
| I <sub>SB2</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> ,<br>$\overline{CE} \geq V_{CC} - 0.3V$<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V | Commercial          | 20   |                     | 20   |                     | 20   |      | 20   | mA    |
|                  |  |   | Military            |      |                     | 20   |                     | 20   |      | 20   |       |

## Capacitance<sup>[4]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 7    | pF    |

### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms

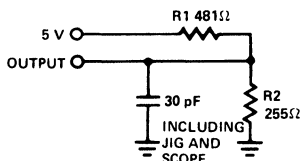


Figure 1a

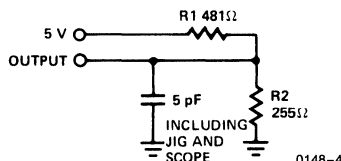


Figure 1b

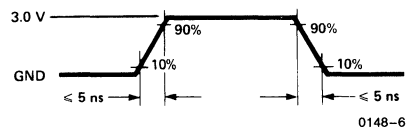


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



0148-5

### Switching Characteristics Over Operating Range<sup>[3, 5]</sup>

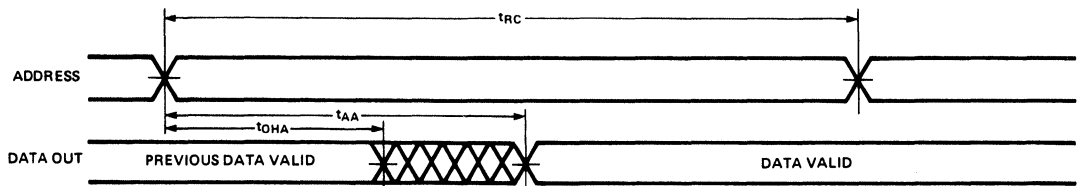
| Parameters                       | Description   | 7C171A-20<br>7C172A-20 |      | 7C171A-25<br>7C172A-25 |      | 7C171A-35<br>7C172A-35 |      | 7C171A-45<br>7C172A-45 |      | Units |
|----------------------------------|---|------------------------|------|------------------------|------|------------------------|------|------------------------|------|-------|
|                                  |   | Min.                   | Max. | Min.                   | Max. | Min.                   | Max. | Min.                   | Max. |       |
| <b>READ CYCLE</b>                |   |                        |      |                        |      |                        |      |                        |      |       |
| t <sub>RC</sub>                  | Read Cycle Time   | 20                     |      | 25                     |      | 35                     |      | 45                     |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid                                   |                        | 20   |                        | 25   |                        | 35   |                        | 45   | ns    |
| t <sub>OHA</sub>                 | Output Hold from Address Change                         | 5                      |      | 5                      |      | 5                      |      | 5                      |      | ns    |
| t <sub>ACE</sub>                 | $\overline{CE}$ LOW to Data Valid                       |                        | 20   |                        | 25   |                        | 35   |                        | 45   | ns    |
| t <sub>LZCE</sub>                | $\overline{CE}$ LOW to Low Z <sup>[7]</sup>             | 5                      |      | 5                      |      | 5                      |      | 5                      |      | ns    |
| t <sub>HZCE</sub>                | $\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>        |                        | 8    |                        | 10   |                        | 15   |                        | 15   | ns    |
| t <sub>PU</sub>                  | $\overline{CE}$ LOW to Power Up                         | 0                      |      | 0                      |      | 0                      |      | 0                      |      | ns    |
| t <sub>PD</sub>                  | $\overline{CE}$ HIGH to Power Down                      |                        | 20   |                        | 20   |                        | 20   |                        | 25   | ns    |
| t <sub>RCS</sub>                 | Read Command Set-up                                     | 0                      |      | 0                      |      | 0                      |      | 0                      |      | ns    |
| t <sub>RCH</sub>                 | Read Command Hold                                       | 0                      |      | 0                      |      | 0                      |      | 0                      |      | ns    |
| <b>WRITE CYCLE<sup>[8]</sup></b> |   |                        |      |                        |      |                        |      |                        |      |       |
| t <sub>WC</sub>                  | Write Cycle Time  | 20                     |      | 20                     |      | 25                     |      | 40                     |      | ns    |
| t <sub>SCE</sub>                 | $\overline{CE}$ LOW to Write End                        | 15                     |      | 20                     |      | 25                     |      | 30                     |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End                             | 15                     |      | 20                     |      | 25                     |      | 30                     |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End                             | 0                      |      | 0                      |      | 0                      |      | 0                      |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                           | 0                      |      | 0                      |      | 0                      |      | 0                      |      | ns    |
| t <sub>PWE</sub>                 | $\overline{WE}$ Pulse Width                             | 15                     |      | 15                     |      | 20                     |      | 20                     |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End                                | 10                     |      | 10                     |      | 15                     |      | 15                     |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End                                | 0                      |      | 0                      |      | 0                      |      | 0                      |      | ns    |
| t <sub>LZWE</sub>                | $\overline{WE}$ HIGH to Low Z <sup>[7]</sup> (7C172)    | 5                      |      | 5                      |      | 5                      |      | 5                      |      | ns    |
| t <sub>HZWE</sub>                | $\overline{WE}$ LOW to High Z <sup>[6, 7]</sup> (7C172) |                        | 7    |                        | 7    |                        | 10   |                        | 15   | ns    |
| t <sub>AWE</sub>                 | $\overline{WE}$ LOW to Data Valid (7C171)               |                        | 20   |                        | 25   |                        | 30   |                        | 35   | ns    |
| t <sub>ADV</sub>                 | Data Valid to Output Valid (7C171)                      |                        | 20   |                        | 25   |                        | 30   |                        | 35   | ns    |

**Notes:**

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZCE</sub> and t<sub>HZWE</sub> are tested with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CE} = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

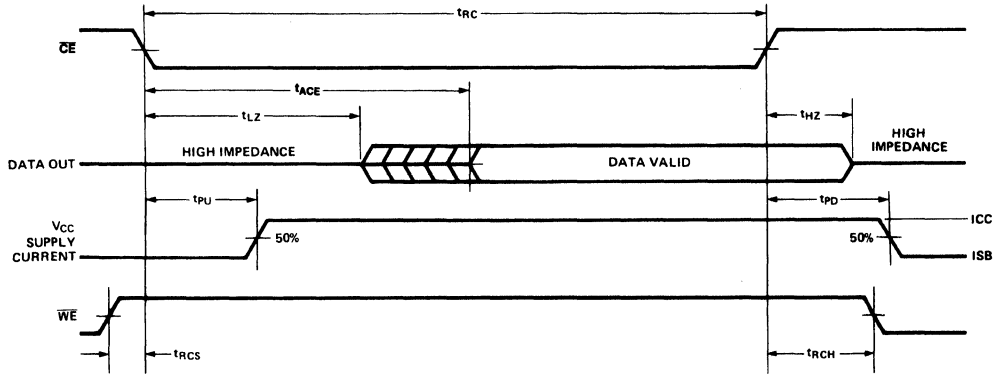
### Switching Waveforms

#### Read Cycle No. 1 (Notes 9, 10)



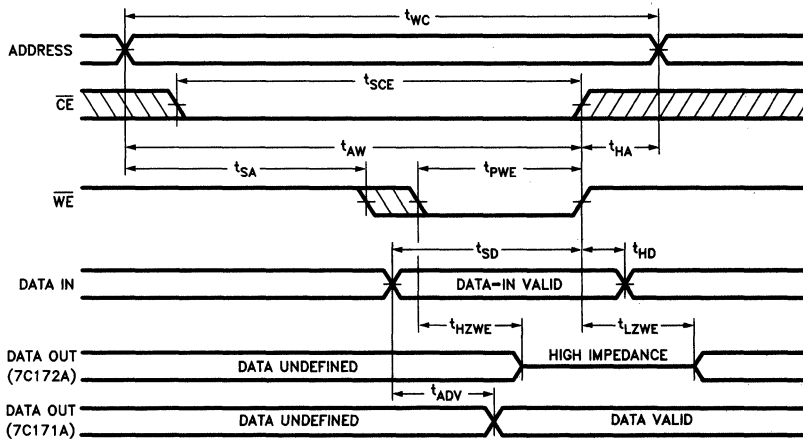
## Switching Waveforms (Continued)

### Read Cycle (Notes 9, 11)



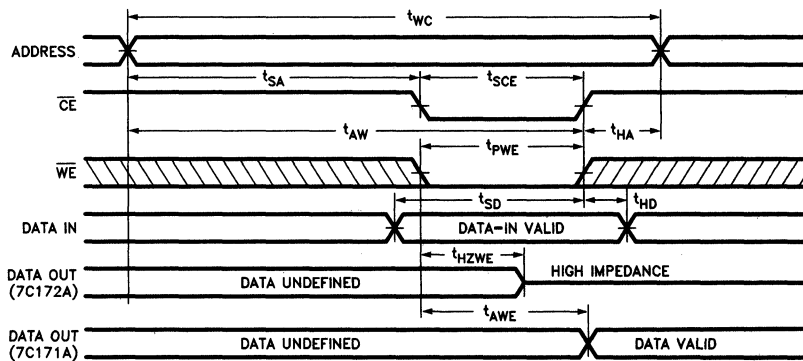
0148-8

### Write Cycle No. 1 ( $\overline{WE}$ Controlled) (Note 8)



0148-9

### Write Cycle No. 2 ( $\overline{CE}$ Controlled) (Note 8)

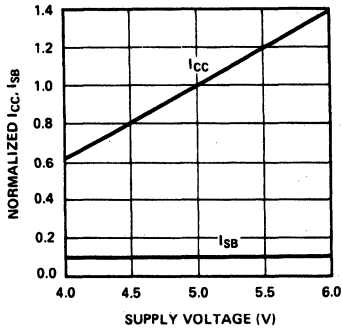


0148-10

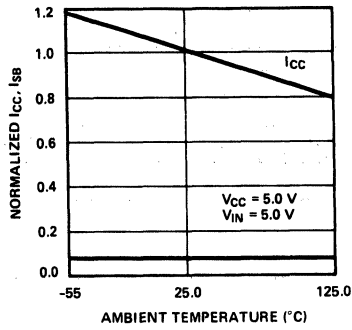
Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state (7C172A).

## Typical DC and AC Characteristics

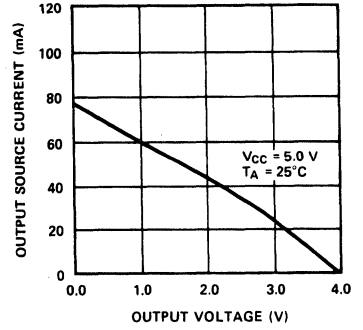
**NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE**



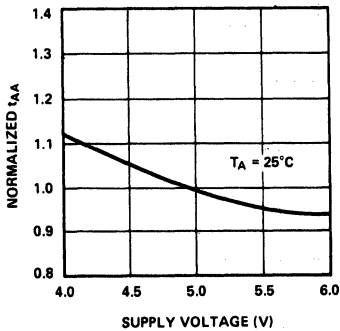
**NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE**



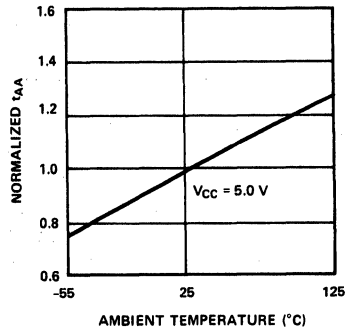
**OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE**



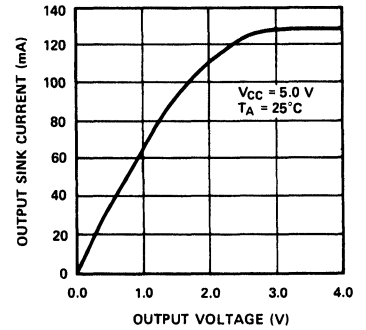
**NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE**



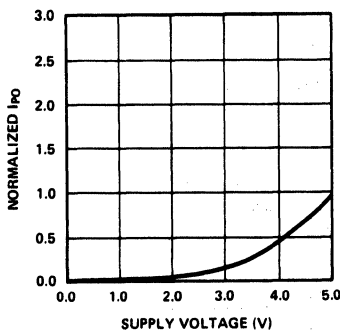
**NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE**



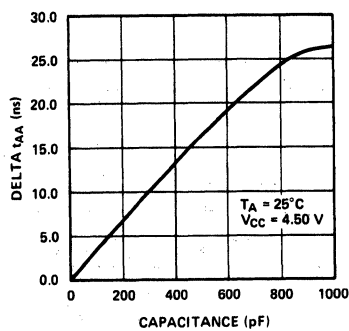
**OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE**



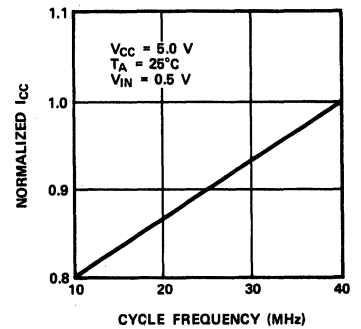
**TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE**



**TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING**



**NORMALIZED  $I_{CC}$  vs. CYCLE TIME**



**Ordering Information**

| Speed (ns) | Ordering Code  | Package Type | Operating Range |
|------------|----------------|--------------|-----------------|
| 20         | CY7C171A-20PC  | P13          | Commercial      |
|            | CY7C171A-20DC  | D14          |                 |
|            | CY7C171A-20LC  | L64          |                 |
|            | CY7C171A-20VC  | V13          |                 |
| 25         | CY7C171A-25PC  | P13          | Commercial      |
|            | CY7C171A-25DC  | D14          |                 |
|            | CY7C171A-25LC  | L64          |                 |
|            | CY7C171A-25VC  | V13          |                 |
|            | CY7C171A-25DMB | D14          | Military        |
|            | CY7C171A-25LMB | L64          |                 |
| 35         | CY7C171A-35PC  | P13          | Commercial      |
|            | CY7C171A-35DC  | D14          |                 |
|            | CY7C171A-35LC  | L64          |                 |
|            | CY7C171A-35VC  | V13          |                 |
|            | CY7C171A-35DMB | D14          | Military        |
|            | CY7C171A-35LMB | L64          |                 |
| 45         | CY7C171A-45PC  | P13          | Commercial      |
|            | CY7C171A-45DC  | D14          |                 |
|            | CY7C171A-45LC  | L64          |                 |
|            | CY7C171A-45VC  | V13          |                 |
|            | CY7C171A-45DMB | D14          | Military        |
|            | CY7C171A-45LMB | L64          |                 |

| Speed (ns) | Ordering Code  | Package Type | Operating Range |
|------------|----------------|--------------|-----------------|
| 20         | CY7C172A-20PC  | P13          | Commercial      |
|            | CY7C172A-20DC  | D14          |                 |
|            | CY7C172A-20LC  | L64          |                 |
|            | CY7C172A-20VC  | V13          |                 |
| 25         | CY7C172A-25PC  | P13          | Commercial      |
|            | CY7C172A-25DC  | D14          |                 |
|            | CY7C172A-25LC  | L64          |                 |
|            | CY7C172A-25VC  | V13          |                 |
|            | CY7C172A-25DMB | D14          | Military        |
|            | CY7C172A-25LMB | L64          |                 |
| 35         | CY7C172A-35PC  | P13          | Commercial      |
|            | CY7C172A-35DC  | D14          |                 |
|            | CY7C172A-35LC  | L64          |                 |
|            | CY7C172A-35VC  | V13          |                 |
|            | CY7C172A-35DMB | D14          | Military        |
|            | CY7C172A-35LMB | L64          |                 |
| 45         | CY7C172A-45PC  | P13          | Commercial      |
|            | CY7C172A-45DC  | D14          |                 |
|            | CY7C172A-45LC  | L64          |                 |
|            | CY7C172A-45VC  | V13          |                 |
|            | CY7C172A-45DMB | D14          | Military        |
|            | CY7C172A-45LMB | L64          |                 |

**2**



## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB1</sub>     | 1,2,3     |
| I <sub>SB2</sub>     | 1,2,3     |

#### Switching Characteristics

| Parameters                       | Subgroups   |
|----------------------------------|-------------|
| <b>READ CYCLE</b>                |             |
| t <sub>RC</sub>                  | 7,8,9,10,11 |
| t <sub>AA</sub>                  | 7,8,9,10,11 |
| t <sub>OHA</sub>                 | 7,8,9,10,11 |
| t <sub>ACE</sub>                 | 7,8,9,10,11 |
| t <sub>RCS</sub>                 | 7,8,9,10,11 |
| t <sub>RCH</sub>                 | 7,8,9,10,11 |
| <b>WRITE CYCLE</b>               |             |
| t <sub>WC</sub>                  | 7,8,9,10,11 |
| t <sub>SCE</sub>                 | 7,8,9,10,11 |
| t <sub>AW</sub>                  | 7,8,9,10,11 |
| t <sub>HA</sub>                  | 7,8,9,10,11 |
| t <sub>SA</sub>                  | 7,8,9,10,11 |
| t <sub>PWE</sub>                 | 7,8,9,10,11 |
| t <sub>SD</sub>                  | 7,8,9,10,11 |
| t <sub>HD</sub>                  | 7,8,9,10,11 |
| t <sub>AWE</sub> <sup>[12]</sup> | 7,8,9,10,11 |
| t <sub>ADV</sub> <sup>[12]</sup> | 7,8,9,10,11 |

Note:

12. 7C171A only.

Document #: 38-00104



**Features**

- Pin programmable into direct mapped or two-way set associative format
- CMOS for optimum speed/power
- High speed—25 ns
- Common I/O
- Internal address latch
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge
- Compatible with Intel 82385 Cache Controller

**Functional Description**

The CY7C183 and CY7C184 are high performance monolithic CMOS static RAMs which contain 128K bits organized into either two, two-way set associative blocks of 4K x 16 RAM, or one directly mapped 8K x 16-bit RAM.

They are designed specifically for use with the Intel 82385 Cache Controller, and their addresses are latched on the falling edge of the Address Latch Enable (ALE) signal. When ALE is HIGH, the latch is transparent. The CY7C183 has all address bits latched by the ALE signal except A<sub>12</sub>, which is unlatched. A<sub>12</sub>, which bypasses the latch, has a faster access time. All address bits are latched by the ALE signal in the CY7C184. The mode pin controls whether they are configured as direct mapped 8K x 16 or two-way set associative 2 x 4K x 16 RAMs. When mode is HIGH, the circuits are placed in the two-way mode. In the two-way mode, the upper address bit, A<sub>12</sub> is a "don't care", and is externally wired to ground. When mode is LOW, the circuits are placed in the direct mode.

Writing is accomplished, in the two-way mode, by taking  $\overline{CE}$  LOW and by inserting the respective  $\overline{CS}_X$  and  $\overline{WE}_X$  signals LOW.  $\overline{CS}_0$  enables bits D<sub>0</sub>–D<sub>7</sub> while  $\overline{CS}_1$  enables bits D<sub>8</sub>–D<sub>15</sub>.  $\overline{WE}_A$

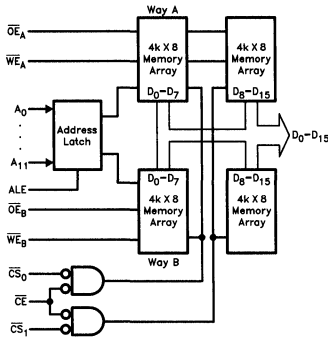
enables cache bank A, and  $\overline{WE}_B$  enables cache bank B to receive whatever data resides on the data bus.  $\overline{OE}_A$  and  $\overline{OE}_B$  similarly enable cache banks A and B, respectively, to drive the data bus.

Writing is accomplished, in the direct mode, by tying  $\overline{WE}_A$  and  $\overline{WE}_B$  together externally, and using A<sub>12</sub> to determine which 4K x 16 memory bank is selected.

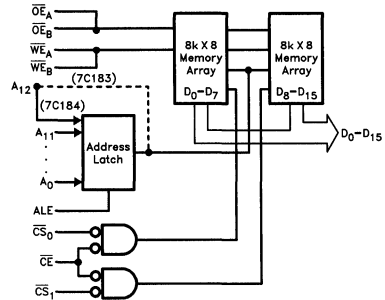
Reading is accomplished, in the two-way mode, by taking  $\overline{CE}$  LOW, inserting the respective  $\overline{OE}_X$  and  $\overline{CS}_X$  signals LOW, and the respective  $\overline{WE}_X$  signal HIGH. The contents of the memory location specified on the address pins will appear on the 16 outputs. Activation of  $\overline{OE}_A$  and  $\overline{OE}_B$  simultaneously will cause both banks to be deselected. Reading is accomplished, in the direct mode, by tying  $\overline{OE}_A$  and  $\overline{OE}_B$  together externally. A<sub>12</sub> will determine which 4K x 16 memory bank is enabled.

**Logic Block Diagrams**

**Two-Way Set Associative (Mode = HIGH)**



**Direct Map (Mode = LOW)**



0145-1

0145-2

**Selection Guide**

|  |            | 7C183-25<br>7C184-25 | 7C183-35<br>7C184-35 | 7C183-45<br>7C184-45 |
|--|------------|----------------------|----------------------|----------------------|
| Maximum Address Access Time (ns)       | Commercial | 25                   | 35                   | 45                   |
|  | Military   |                      | 35                   | 45                   |
| Maximum Output Enable Access Time (ns) | Commercial | 10                   | 14                   | 16                   |
|  | Military   |                      | 14                   | 16                   |
| Maximum Operating Current (mA)         | Commercial | 220                  | 170                  | 140                  |
|  | Military   |                      | 200                  | 160                  |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature .....                           | -65°C to +150°C |
| Ambient Temperature with Power Applied .....        | -55°C to +125°C |
| Supply Voltage to Ground Potential .....            | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State ..... | -0.5V to +7.0V  |
| DC Input Voltage .....                              | -3.0V to +7.0V  |
| Output Current into Outputs (LOW) .....             | 20 mA           |

|                                |   |
|--------------------------------|---|
| Static Discharge Voltage ..... | >2001V<br>(Per MIL-STD-883 Method 3015) |
| Latch-up Current .....         | >200 mA                                 |

### Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C        | 5V ± 10%        |
| Military   | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range

| Parameters      | Description                                 | Test Conditions   | 7C183-25<br>7C184-25 |                 | 7C183-35<br>7C184-35 |                 | 7C183-45<br>7C184-45 |                 | Units |    |
|-----------------|---|---|----------------------|-----------------|----------------------|-----------------|----------------------|-----------------|-------|----|
|                 |   |   | Min.                 | Max.            | Min.                 | Max.            | Min.                 | Max.            |       |    |
| V <sub>OH</sub> | Output HIGH Voltage                         | V <sub>CC</sub> = Min., I <sub>OH</sub> = -1.0 mA   | 2.4                  |                 | 2.4                  |                 | 2.4                  |                 | V     |    |
| V <sub>OL</sub> | Output LOW Voltage                          | V <sub>CC</sub> = Min., I <sub>OL</sub> = 4.0 mA  |                      | 0.4             |                      | 0.4             |                      | 0.4             | V     |    |
| V <sub>IH</sub> | Input HIGH Voltage                          |   | 2.2                  | V <sub>CC</sub> | 2.2                  | V <sub>CC</sub> | 2.2                  | V <sub>CC</sub> | V     |    |
| V <sub>IL</sub> | Input LOW Voltage                           |   | -3.0                 | 0.8             | -3.0                 | 0.8             | -3.0                 | 0.8             | V     |    |
| I <sub>IX</sub> | Input Load Current                          | GND < V <sub>I</sub> < V <sub>CC</sub>  | -10                  | +10             | -10                  | +10             | -10                  | +10             | μA    |    |
| I <sub>OZ</sub> | Output Leakage Current                      | GND < V <sub>O</sub> < V <sub>CC</sub> ,<br>Output Disabled                               | -10                  | +10             | -10                  | +10             | -10                  | +10             | μA    |    |
| I <sub>OS</sub> | Output Short Circuit Current <sup>[1]</sup> | V <sub>CC</sub> = Max.,<br>V <sub>OUT</sub> = GND   |                      | -350            |                      | -350            |                      | -350            | mA    |    |
| I <sub>CC</sub> | V <sub>CC</sub> Operating Supply Current    | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA<br>Duty Cycle = 45%<br>Single Way Write | Commercial           |                 | 220                  |                 | 170                  |                 | 140   | mA |
|                 |   |   | Military             |                 |                      |                 | 200                  |                 | 160   |    |

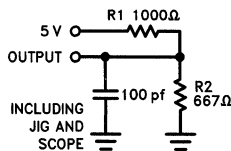
### Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions   | Max. | Units |
|------------------|--------------------|---|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V <sup>[3]</sup> | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |   | 8    |       |

#### Notes:

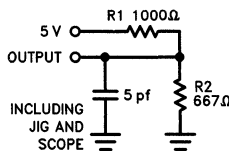
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 100 pF load capacitance.

### AC Test Loads and Waveforms



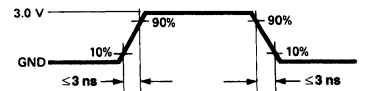
0145-3

Figure 1a



0145-4

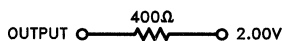
Figure 1b



0145-5

Figure 2. All Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



0145-6

### Switching Characteristics Over Operating Range [4, 5]

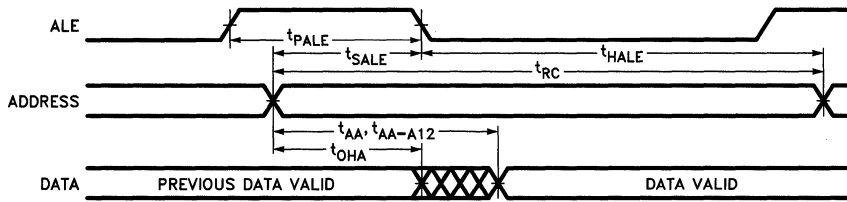
| Parameters                                     | Description                                  | 7C183-25<br>7C184-25 |      | 7C183-35<br>7C184-35 |      | 7C183-45<br>7C184-45 |      | Units |
|--|--|----------------------|------|----------------------|------|----------------------|------|-------|
|  |  | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. |       |
| <b>READ CYCLE</b>                              |  |                      |      |                      |      |                      |      |       |
| t <sub>RC</sub>                                | Read Cycle Time                              | 25                   |      | 35                   |      | 45                   |      | ns    |
| t <sub>AA</sub>                                | Address to Data Valid                        |                      | 25   |                      | 35   |                      | 45   | ns    |
| t <sub>AA A<sub>12</sub></sub> <sup>[12]</sup> | Address to Data Valid A <sub>12</sub>        |                      | 17   |                      | 25   |                      | 35   | ns    |
| t <sub>CE</sub>                                | Chip Enable to Data Valid                    |                      | 12   |                      | 15   |                      | 20   | ns    |
| t <sub>CS</sub>                                | Chip Select to Data Valid                    |                      | 12   |                      | 15   |                      | 20   | ns    |
| t <sub>OE</sub>                                | Output Enable to Data Valid                  |                      | 10   |                      | 14   |                      | 16   | ns    |
| t <sub>OH</sub>                                | Output Hold from Address Change              | 3                    |      | 3                    |      | 3                    |      | ns    |
| t <sub> LZCE</sub>                             | Chip Enable to Low Z <sup>[7]</sup>          | 3                    |      | 3                    |      | 3                    |      | ns    |
| t <sub> LZOE</sub>                             | Output Enable to Low Z <sup>[7, 8]</sup>     | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub> LZCE</sub>                             | Chip Enable to High Z                        |                      | 15   |                      | 25   |                      | 30   | ns    |
| t <sub> LZOE</sub>                             | Output Enable to High Z                      |                      | 9    |                      | 10   |                      | 12   | ns    |
| t <sub>PALE</sub>                              | ALE Pulse Width                              |                      | 8    |                      | 10   |                      | 12   | ns    |
| t <sub>SALE</sub>                              | Address Set-up to ALE Low                    |                      | 4    |                      | 6    |                      | 8    | ns    |
| t <sub>HALE</sub>                              | Address Hold from ALE Low                    |                      | 4    |                      | 4    |                      | 4    | ns    |
| <b>WRITE CYCLE<sup>[8]</sup></b>               |  |                      |      |                      |      |                      |      |       |
| t <sub>WC</sub>                                | Write Cycle Time                             | 25                   |      | 35                   |      | 45                   |      | ns    |
| t <sub>AW</sub>                                | Address Set-up to Write End                  | 20                   |      | 30                   |      | 40                   |      | ns    |
| t <sub>SCE</sub>                               | Chip Enable to Write End                     | 20                   |      | 25                   |      | 30                   |      | ns    |
| t <sub>SCS</sub>                               | Chip Select to Write End                     | 20                   |      | 25                   |      | 30                   |      | ns    |
| t <sub>SD</sub>                                | Data Set-up to Write End                     | 10                   |      | 10                   |      | 10                   |      | ns    |
| t <sub>HD</sub>                                | Data Hold from Write End                     | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>PWE</sub>                               | Write Enable Pulse Width                     | 20                   |      | 25                   |      | 30                   |      | ns    |
| t <sub>SA</sub>                                | Address Set-up to Write Enable               | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>HA</sub>                                | Address Hold from Write Enable               | 2                    |      | 2                    |      | 2                    |      | ns    |
| t <sub> LZWE</sub>                             | Write Enable HIGH to Low Z <sup>[7]</sup>    | 3                    |      | 3                    |      | 3                    |      | ns    |
| t <sub> LZWE</sub>                             | Write Enable LOW to High Z <sup>[7, 8]</sup> |                      | 15   |                      | 15   |                      | 20   | ns    |
| t <sub>PALE</sub>                              | ALE Pulse Width                              |                      | 8    |                      | 10   |                      | 12   | ns    |
| t <sub>SALE</sub>                              | Address / $\overline{CE}$ Set-up to ALE Low  |                      | 4    |                      | 6    |                      | 8    | ns    |
| t <sub>HALE</sub>                              | Address / $\overline{CE}$ Hold from ALE Low  |                      | 4    |                      | 4    |                      | 4    | ns    |

**Notes:**

6. t <sub>LZCE</sub> and t <sub>LZCE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
7. The internal write time of the memory is defined by the overlap of  $\overline{CE}$ ,  $\overline{CS}_X$ , and  $\overline{WE}_X$ . All signals must be LOW to initiate a write and any signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. Both  $\overline{WE}_A$  and  $\overline{WE}_B$  must be HIGH for read cycle.
9. Device is continuously selected,  $\overline{CE}$  and  $\overline{CS}$  are LOW.
10. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
11.  $\overline{OE}$  is selected (LOW).
12. CY7C183 only.

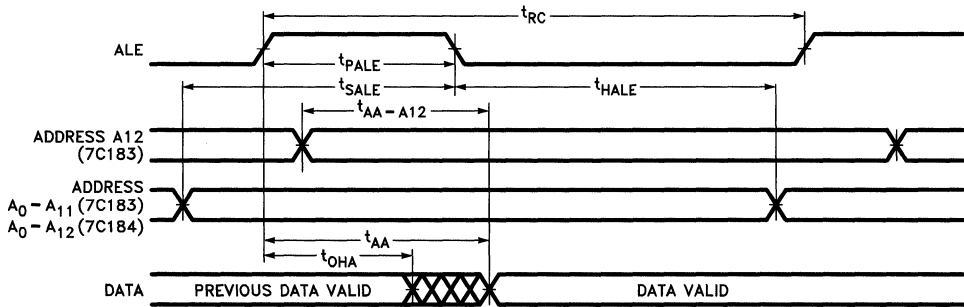
### Switching Waveforms

Read Cycle No. 1 [9, 10, 12]



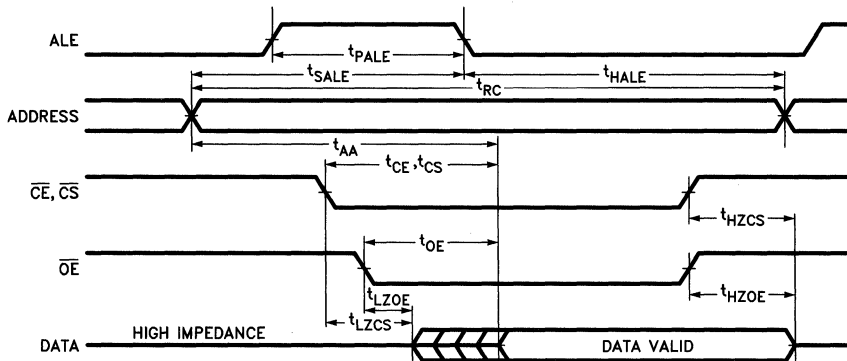
0145-7

Read Cycle No. 2 [9, 10, 12]



0145-8

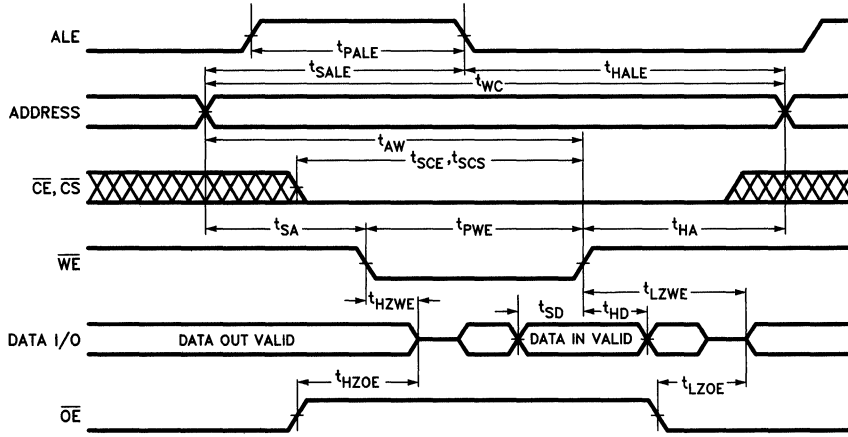
Read Cycle No. 3 [9]



0145-9

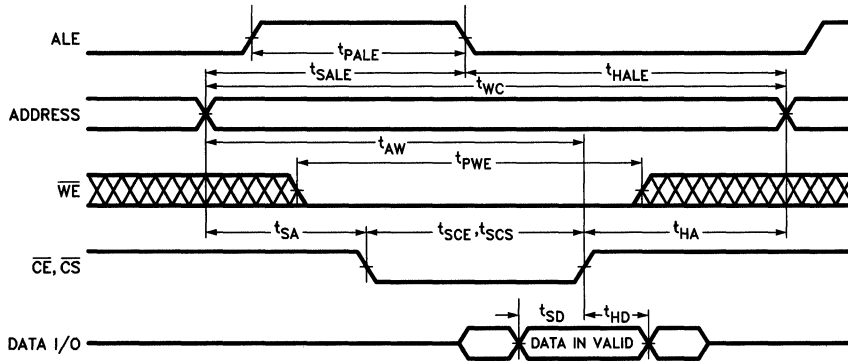
Switching Waveforms (Continued)

Write Cycle No. 1 (WE Controlled)



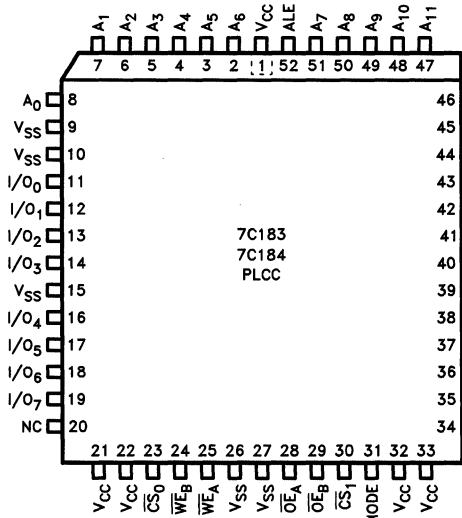
0145-10

Write Cycle No. 1 ( $\overline{CE}$ ,  $\overline{CS}$  Controlled)

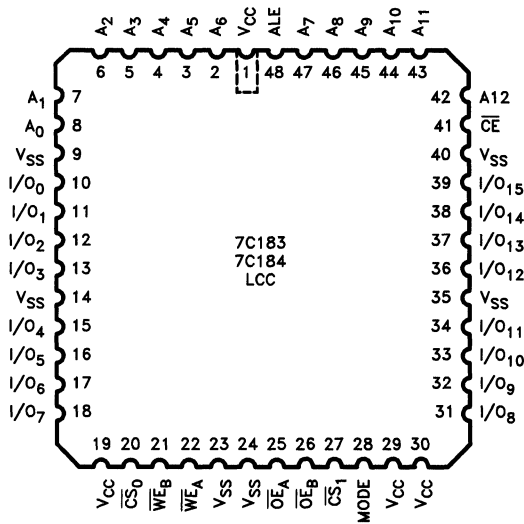


0145-11

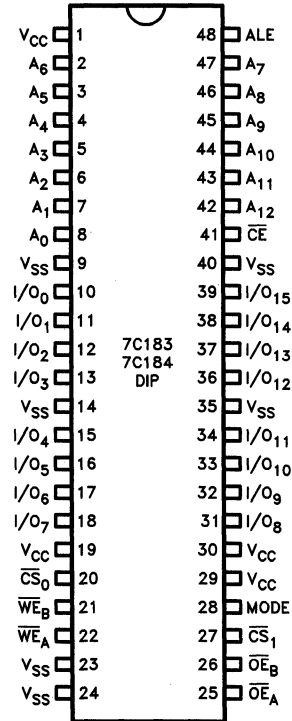
### Pin Configurations



0145-12



0145-14



0145-13

## Truth Tables

### Two-Way Mode (MODE = HIGH)

| CE | CS <sub>0</sub> | CS <sub>1</sub> | OE <sub>A</sub> | OE <sub>B</sub> | WE <sub>A</sub> | WE <sub>B</sub> | Operation   |
|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|---|
| H  | X               | X               | X               | X               | X               | X               | Outputs Hi-Z, Write Disabled                        |
| L  | H               | H               | X               | X               | X               | X               | Outputs Hi-Z, Write Disabled                        |
| X  | X               | X               | H               | H               | X               | X               | Outputs Hi-Z  |
| X  | X               | X               | L               | L               | X               | X               | Outputs Hi-Z  |
| L  | L               | H               | L               | H               | H               | H               | Read I/O <sub>0</sub> -I/O <sub>7</sub> Way A       |
| L  | L               | H               | H               | L               | H               | H               | Read I/O <sub>0</sub> -I/O <sub>7</sub> Way B       |
| L  | H               | L               | L               | H               | H               | H               | Read I/O <sub>8</sub> -I/O <sub>15</sub> Way A      |
| L  | H               | L               | H               | L               | H               | H               | Read I/O <sub>8</sub> -I/O <sub>15</sub> Way B      |
| L  | L               | L               | L               | H               | H               | H               | Read I/O <sub>0</sub> -I/O <sub>15</sub> Way A      |
| L  | L               | L               | H               | L               | H               | H               | Read I/O <sub>0</sub> -I/O <sub>15</sub> Way B      |
| L  | L               | H               | X               | X               | L               | H               | Write I/O <sub>0</sub> -I/O <sub>7</sub> Way A      |
| L  | L               | H               | X               | X               | H               | L               | Write I/O <sub>0</sub> -I/O <sub>7</sub> Way B      |
| L  | H               | L               | X               | X               | L               | H               | Write I/O <sub>8</sub> -I/O <sub>15</sub> Way A     |
| L  | H               | L               | X               | X               | H               | L               | Write I/O <sub>8</sub> -I/O <sub>15</sub> Way B     |
| L  | L               | L               | X               | X               | L               | H               | Write I/O <sub>0</sub> -I/O <sub>15</sub> Way A     |
| L  | L               | L               | X               | X               | H               | L               | Write I/O <sub>0</sub> -I/O <sub>15</sub> Way B     |
| L  | L               | H               | X               | X               | L               | L               | Write I/O <sub>0</sub> -I/O <sub>7</sub> Way A & B  |
| L  | H               | L               | X               | X               | L               | L               | Write I/O <sub>8</sub> -I/O <sub>15</sub> Way A & B |
| L  | L               | L               | X               | X               | L               | L               | Write I/O <sub>0</sub> -I/O <sub>15</sub> Way A & B |

### Direct Mode (MODE = LOW)

| CE | CS <sub>0</sub> | CS <sub>1</sub> | OE <sub>A</sub> | OE <sub>B</sub> | WE <sub>A</sub> | WE <sub>B</sub> | Operation                                 |
|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|---|
| H  | X               | X               | X               | X               | X               | X               | Outputs Hi-Z, Write Disabled              |
| L  | H               | H               | X               | X               | X               | X               | Outputs Hi-Z, Write Disabled              |
| X  | X               | X               | H               | H               | X               | X               | Outputs Hi-Z                              |
| L  | L               | H               | L               | L               | H               | H               | Read I/O <sub>0</sub> -I/O <sub>7</sub>   |
| L  | H               | L               | L               | L               | H               | H               | Read I/O <sub>8</sub> -I/O <sub>15</sub>  |
| L  | L               | L               | L               | L               | H               | H               | Read I/O <sub>0</sub> -I/O <sub>15</sub>  |
| L  | L               | H               | X               | X               | L               | L               | Write I/O <sub>0</sub> -I/O <sub>7</sub>  |
| L  | H               | L               | X               | X               | L               | L               | Write I/O <sub>8</sub> -I/O <sub>15</sub> |
| L  | L               | L               | X               | X               | L               | L               | Write I/O <sub>0</sub> -I/O <sub>15</sub> |

## Ordering Information

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C183-25DC  | D26          | Commercial      |
|            | CY7C183-25JC  | J69          |                 |
| 35         | CY7C183-35DC  | D26          | Military        |
|            | CY7C183-35JC  | J69          |                 |
|            | CY7C183-35DMB | D26          |                 |
|            | CY7C183-35LMB | L68          |                 |
| 45         | CY7C183-45DC  | D26          | Commercial      |
|            | CY7C183-45JC  | J69          |                 |
|            | CY7C183-45DMB | D26          | Military        |
|            | CY7C183-45LMB | L68          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C184-25DC  | D26          | Commercial      |
|            | CY7C184-25JC  | J69          |                 |
| 35         | CY7C184-35DC  | D26          | Military        |
|            | CY7C184-35JC  | J69          |                 |
|            | CY7C184-35DMB | D26          |                 |
|            | CY7C184-35LMB | L68          |                 |
| 45         | CY7C184-45DC  | D26          | Commercial      |
|            | CY7C184-45JC  | J69          |                 |
|            | CY7C184-45DMB | D26          | Military        |
|            | CY7C184-45LMB | L68          |                 |



## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>Ix</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>OS</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |

#### Switching Characteristics

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>ACE</sub>   | 7,8,9,10,11 |
| t <sub>OE</sub>    | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>SCE</sub>   | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |

Document #: 38-00090



**Features**

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed—12 ns
- Low active power — 550 mW at 40 MHz
- Low standby power — 150 mW
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

**Functional Description**

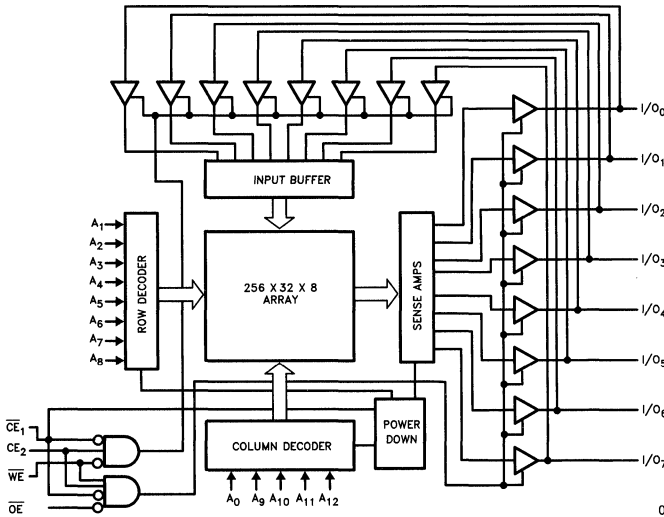
The CY7C185 and CY7C186 are high performance CMOS static RAMs organized as 8192 words by 8 bits. These RAMs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor. Easy memory expansion is provided by an active LOW chip enable (CE<sub>1</sub>), an active HIGH chip enable (CE<sub>2</sub>), and active LOW output enable (OE) and three-state drivers. Both devices have an automatic power-down feature (CE<sub>1</sub>), reducing the power consumption by 75% when deselected. The CY7C185 is in the space saving 300 mil wide DIP package and leadless chip carrier. The CY7C186 is in the standard 600 mil wide package.

An active LOW write enable signal (WE) controls the writing/reading

operation of the memory. When CE<sub>1</sub> and WE inputs are both LOW, data on the eight data input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the memory location addressed by the address present on the address pins (A<sub>0</sub> through A<sub>12</sub>). Reading the device is accomplished by selecting the device and enabling the outputs, CE<sub>1</sub> and OE active LOW, CE<sub>2</sub> active HIGH, while (WE) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

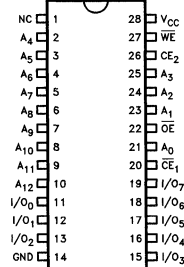
The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable (WE) is HIGH.

**Logic Block Diagram**

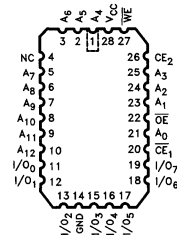


0147-1

**Pin Configurations**



0147-2



0147-3

**Selection Guide**

|                                |            | 7C185-12<br>7C186-12 | 7C185-15<br>7C186-15 |
|--------------------------------|------------|----------------------|----------------------|
| Maximum Access Time (ns)       |            | 12                   | 15                   |
| Maximum Operating Current (mA) | Commercial | 125                  | 120                  |
|                                | Military   | 155                  | 145                  |
| Maximum Standby Current (mA)   | Commercial | 30                   | 30                   |
|                                | Military   | 50                   | 50                   |

### Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

|   |                       |
|---|-----------------------|
| Storage Temperature                                   | ..... -65°C to +150°C |
| Ambient Temperature with Power Applied                | ..... -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 28 to Pin 14) | ..... -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State         | ..... -0.5V to +7.0V  |
| Input Voltage <sup>[14]</sup>                         | ..... -3.0V to +7.0V  |
| Output Current into Outputs (Low)                     | ..... 20 mA           |

|                          |   |
|--------------------------|---|
| Static Discharge Voltage | ..... > 2001V (Per MIL-STD-883 Method 3015) |
| Latch-up Current         | ..... > 200 mA                              |

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ±10%         |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ±10%         |

### Electrical Characteristics Over Operating Range<sup>[4]</sup>

| Parameters       | Description                                    | Test Conditions   | 7C185-12<br>7C186-12 |                 | 7C185-15<br>7C186-15 |                 | Units |
|------------------|--|---|----------------------|-----------------|----------------------|-----------------|-------|
|                  |  |   | Min.                 | Max.            | Min.                 | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                            | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA                                   | 2.4                  |                 | 2.4                  |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                             | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA                                    |                      | 0.4             |                      | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                             |   | 2.2                  | V <sub>CC</sub> | 2.2                  | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage <sup>[14]</sup>              |   | -0.5                 | 0.8             | -0.5                 | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current                             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>  | -10                  | 10              | -10                  | 10              | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                         | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub><br>Output Disabled                           | -10                  | +10             | -10                  | +10             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>    | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND                                      |                      | -300            |                      | -300            | mA    |
| I <sub>CC1</sub> | V <sub>CC</sub> Operations Supply              | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA<br>f = 40 MHz                     | Commercial           | 110             |                      | 110             | mA    |
|                  |  |   | Military             | 135             |                      | 135             |       |
| I <sub>CC2</sub> | V <sub>CC</sub> Operating Supply Current       | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA                                   | Commercial           | 125             |                      | 120             | mA    |
|                  |  |   | Military             | 155             |                      | 145             |       |
| I <sub>SB</sub>  | Automatic $\overline{CE}_1$ Power Down Current | Max. V <sub>CC</sub> ,<br>$\overline{CE}_1 \geq V_{IH}$ ,<br>Min. Duty Cycle = 100% | Commercial           | 30              |                      | 30              | mA    |
|                  |  |   | Military             | 50              |                      | 50              |       |

### Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions  | Max. <sup>[13]</sup> | Units |
|------------------|--------------------|--|----------------------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5                    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 7                    |       |

#### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

### AC Test Loads and Waveforms

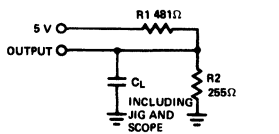


Figure 1a

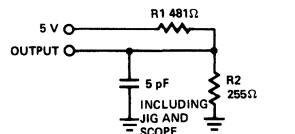


Figure 1b

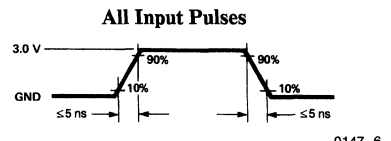


Figure 2

Equivalent to:

THÉVENIN EQUIVALENT



Switching Characteristics Over Operating Range<sup>[4, 5]</sup>

| Parameters                       | Description   | 7C185-12<br>7C186-12 |      | 7C185-15<br>7C186-15 |      | Units |
|----------------------------------|---|----------------------|------|----------------------|------|-------|
|                                  |   | Min.                 | Max. | Min.                 | Max. |       |
| <b>READ CYCLE</b>                |   |                      |      |                      |      |       |
| t <sub>RC</sub>                  | Read Cycle Time   | 12                   |      | 15                   |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid   |                      | 12   |                      | 15   | ns    |
| t <sub>OHA</sub>                 | Data Hold from Address Change   | 3                    |      | 3                    |      | ns    |
| t <sub>ACE<sub>1</sub></sub>     | $\overline{CE}_1$ LOW to Data Valid   |                      | 12   |                      | 15   | ns    |
| t <sub>ACE<sub>2</sub></sub>     | CE <sub>2</sub> HIGH to Data Valid  |                      | 12   |                      | 15   | ns    |
| t <sub>DOE</sub>                 | $\overline{OE}$ LOW to Data Valid   |                      | 10   |                      | 10   | ns    |
| t <sub>LZOE</sub>                | $\overline{OE}$ LOW to Low Z  | 3                    |      | 3                    |      | ns    |
| t <sub>HZOE</sub>                | $\overline{OE}$ HIGH to High Z <sup>[6]</sup>                                       |                      | 8    |                      | 8    | ns    |
| t <sub>LZCE<sub>1</sub></sub>    | $\overline{CE}_1$ LOW to Low Z <sup>[7]</sup>                                       | 3                    |      | 5                    |      | ns    |
| t <sub>LZCE<sub>2</sub></sub>    | CE <sub>2</sub> HIGH to Low Z   | 3                    |      | 3                    |      | ns    |
| t <sub>HZCE</sub>                | $\overline{CE}_1$ HIGH to High Z <sup>[6, 7]</sup><br>CE <sub>2</sub> LOW to High Z |                      | 8    |                      | 8    | ns    |
| t <sub>PU</sub>                  | $\overline{CE}_1$ LOW to Power Up   | 0                    |      | 0                    |      | ns    |
| t <sub>PD</sub>                  | $\overline{CE}_1$ HIGH to Power Down  |                      | 12   |                      | 15   | ns    |
| <b>WRITE CYCLE<sup>[8]</sup></b> |   |                      |      |                      |      |       |
| t <sub>WC</sub>                  | Write Cycle Time  | 12                   |      | 15                   |      | ns    |
| t <sub>SCE<sub>1</sub></sub>     | $\overline{CE}_1$ LOW to Write End  | 10                   |      | 12                   |      | ns    |
| t <sub>SCE<sub>2</sub></sub>     | CE <sub>2</sub> HIGH to Write End   | 10                   |      | 12                   |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End   | 10                   |      | 12                   |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End   | 0                    |      | 0                    |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start   | 0                    |      | 0                    |      | ns    |
| t <sub>PWE</sub>                 | WE Pulse Width  | 10                   |      | 12                   |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End  | 10                   |      | 10                   |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End  | 0                    |      | 0                    |      | ns    |
| t <sub>HZWE</sub>                | $\overline{WE}$ LOW to High Z <sup>[6]</sup>  |                      | 7    |                      | 7    | ns    |
| t <sub>LZWE</sub>                | $\overline{WE}$ HIGH to Low Z   | 5                    |      | 5                    |      | ns    |

Notes:

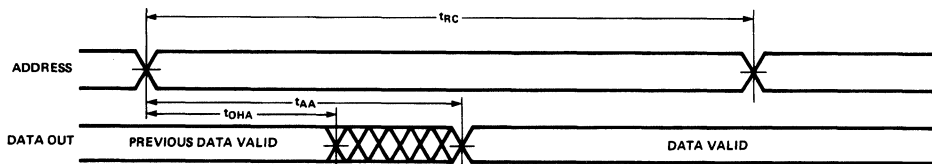
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and C<sub>L</sub> = 30 pF load capacitance for 15 ns t<sub>AA</sub> devices and C<sub>L</sub> = 20 pF load capacitance for 12 ns t<sub>AA</sub> devices.
- t<sub>HZOE</sub>, t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 7b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW, CE<sub>2</sub> HIGH and  $\overline{WE}$  LOW. Both signals must be LOW

to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  = V<sub>IL</sub>. CE<sub>2</sub> = V<sub>IH</sub>.
- Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
- Data I/O is HIGH impedance if  $\overline{OE}$  = V<sub>IH</sub>.
- For all packages except cerdip (D22, D16) which has maximums of C<sub>IN</sub> = 10 pF, C<sub>OUT</sub> = 12 pF.
- V<sub>IL</sub> (min.) = -3.0V for pulse width < 20 ns.

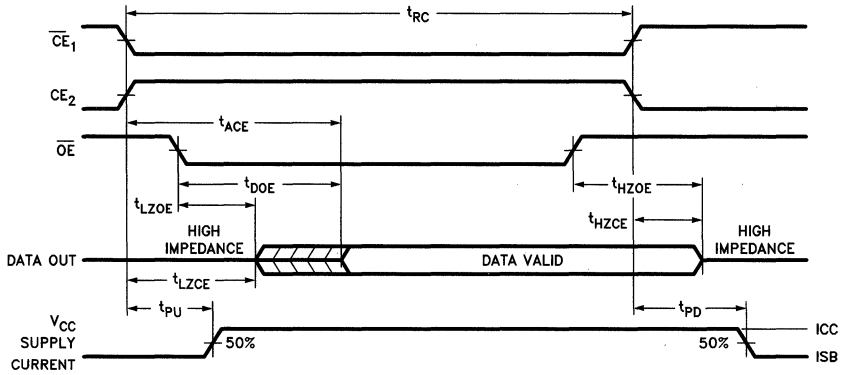
Switching Waveforms

Read Cycle No. 1 (Notes 10, 11)



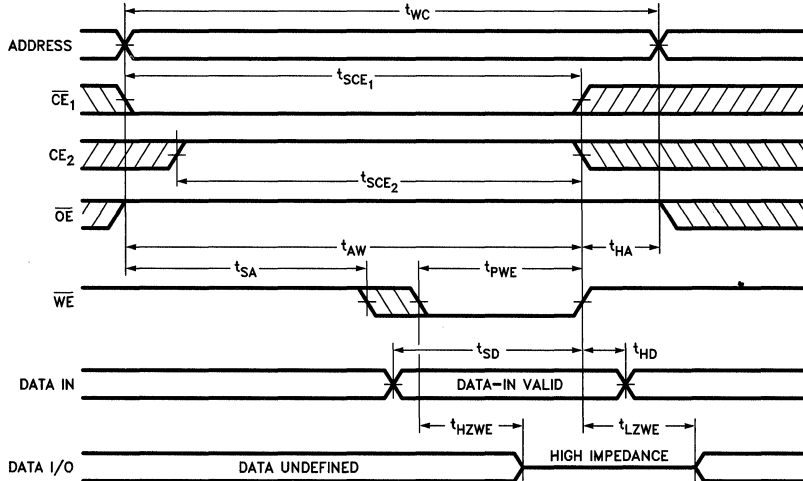
Switching Waveforms (Continued)

Read Cycle No. 2 (Notes 9, 11)



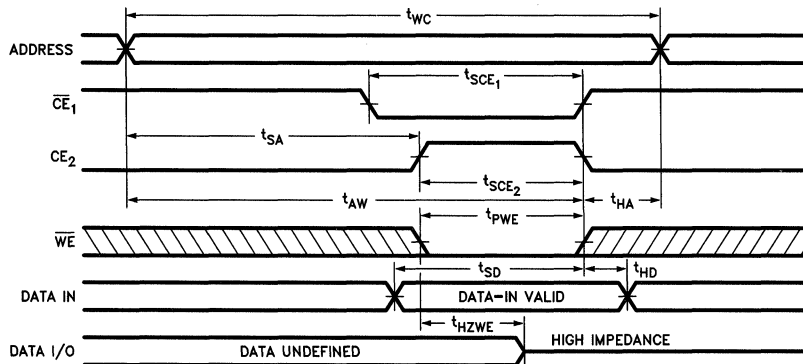
0147-9

Write Cycle No. 1 ( $\overline{WE}$  Controlled) (Notes 8, 12)



0147-10

Write Cycle No. 2 ( $\overline{CE}$  Controlled) (Notes 8, 12)



0147-11

Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

### Truth Table

| $\overline{CE}_1$ | $CE_2$ | $\overline{WE}$ | $\overline{OE}$ | Input/Outputs | Mode                |
|-------------------|--------|-----------------|-----------------|---------------|---------------------|
| H                 | X      | X               | X               | High Z        | Deselect Power Down |
| X                 | L      | X               | X               | High Z        | Deselect            |
| L                 | H      | H               | L               | Data Out      | Read                |
| L                 | H      | L               | X               | Data In       | Write               |
| L                 | H      | H               | H               | High Z        | Deselect            |

### Ordering Information

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 12         | CY7C185-12PC  | P21          | Commercial      |
|            | CY7C185-12VC  | V21          |                 |
|            | CY7C185-12DC  | D22          |                 |
|            | CY7C185-12LC  | L54          |                 |
|            | CY7C185-12DMB | D22          | Military        |
|            | CY7C185-12LMB | L54          |                 |
| 15         | CY7C185-15PC  | P21          | Commercial      |
|            | CY7C185-15VC  | V21          |                 |
|            | CY7C185-15DC  | D22          |                 |
|            | CY7C185-15LC  | L54          |                 |
|            | CY7C185-15DMB | D22          | Military        |
|            | CY7C185-15LMB | L54          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 12         | CY7C186-12PC  | P21          | Commercial      |
|            | CY7C186-12DC  | D22          |                 |
|            | CY7C186-12DMB | D22          | Military        |
| 15         | CY7C186-15PC  | P21          | Commercial      |
|            | CY7C186-15DC  | D22          |                 |
|            | CY7C186-15DMB | D22          | Military        |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>Ix</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB1</sub>     | 1,2,3     |

**Switching Characteristics**

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>ACE1</sub>  | 7,8,9,10,11 |
| t <sub>ACE2</sub>  | 7,8,9,10,11 |
| t <sub>DOE</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>SCE1</sub>  | 7,8,9,10,11 |
| t <sub>SCE2</sub>  | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |

Document #: 38-A-00016



**Features**

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed—20 ns
- Low active power — 550 mW
- Low standby power — 110 mW
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

**Functional Description**

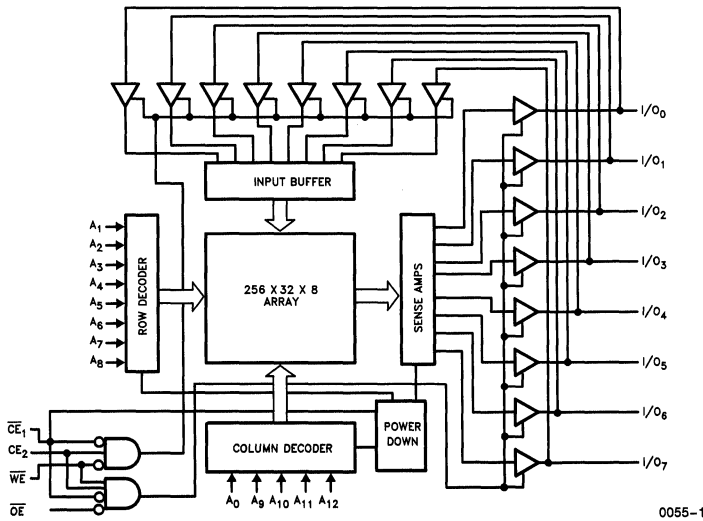
The CY7C185 and CY7C186 are high performance CMOS static RAMs organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}_1$ ), an active HIGH chip enable ( $CE_2$ ), and active LOW output enable ( $\overline{OE}$ ) and three-state drivers. Both devices have an automatic power-down feature ( $\overline{CE}_1$ ), reducing the power consumption by 73% when deselected. The CY7C185 is in the space saving 300 mil wide DIP package and leadless chip carrier. The CY7C186 is in the standard 600 mil wide package.

An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When  $\overline{CE}_1$  and  $\overline{WE}$  inputs are both LOW, data on

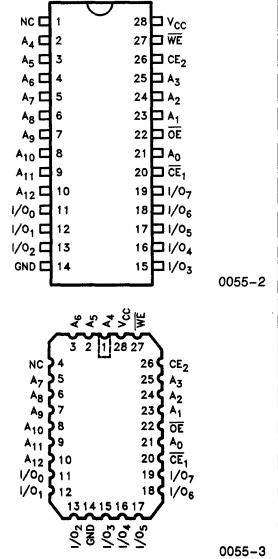
the eight data input/output pins ( $I/O_0$  through  $I/O_7$ ) is written into the memory location addressed by the address present on the address pins ( $A_0$  through  $A_{12}$ ). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{CE}_1$  and  $\overline{OE}$  active LOW,  $CE_2$  active HIGH, while ( $\overline{WE}$ ) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH. A die coat is used to ensure alpha immunity.

**Logic Block Diagram**



**Pin Configurations**



**Selection Guide**

|                                |            | 7C185-20<br>7C186-20 | 7C185-25<br>7C186-25 | 7C185-35<br>7C186-35 | 7C185-45<br>7C186-45 | 7C185-55<br>7C186-55 |
|--------------------------------|------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| Maximum Access Time (ns)       |            | 20                   | 25                   | 35                   | 45                   | 55                   |
| Maximum Operating Current (mA) | Commercial | 125                  | 100                  | 100                  | 100                  | 80                   |
|                                | Military   |                      | 125                  | 100                  | 100                  | 100                  |
| Maximum Standby Current (mA)   | Commercial | 40/20                | 20/20                | 20/20                | 20/20                | 20/20                |
|                                | Military   |                      | 40/20                | 20/20                | 20/20                | 20/20                |



### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                       |
|---|-----------------------|
| Storage Temperature                                   | ..... -65°C to +150°C |
| Ambient Temperature with Power Applied                | ..... -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 28 to Pin 14) | ..... -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State         | ..... -0.5V to +7.0V  |
| DC Input Voltage                                      | ..... -3.0V to +7.0V  |
| Output Current into Outputs (Low)                     | ..... 20 mA           |

|                          |   |
|--------------------------|---|
| Static Discharge Voltage | ..... > 2001V (Per MIL-STD-883 Method 3015) |
| Latch-up Current         | ..... > 200 mA                              |

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ±10%         |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ±10%         |

### Electrical Characteristics Over Operating Range<sup>[4]</sup>

| Parameters       | Description                                    | Test Conditions   | 7C185-20<br>7C186-20 |                 | 7C185-25, 35, 45<br>7C186-25, 35, 45 |                 | 7C185-55<br>7C186-55 |                 | Units |
|------------------|--|---|----------------------|-----------------|--------------------------------------|-----------------|----------------------|-----------------|-------|
|                  |  |   | Min.                 | Max.            | Min.                                 | Max.            | Min.                 | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                            | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA   | 2.4                  |                 | 2.4                                  |                 | 2.4                  |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                             | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA  |                      | 0.4             |                                      | 0.4             |                      | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                             |   | 2.2                  | V <sub>CC</sub> | 2.2                                  | V <sub>CC</sub> | 2.2                  | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage <sup>[4A]</sup>              |   | -3.0                 | 0.8             | -3.0                                 | 0.8             | -3.0                 | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current                             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>  | -10                  | 10              | -10                                  | 10              | -10                  | 10              | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                         | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub><br>Output Disabled   | -10                  | +10             | -10                                  | +10             | -10                  | +10             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>    | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND  |                      | -300            |                                      | -300            |                      | -300            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current       | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA   | Coml.                |                 |                                      | 100             |                      | 80              | mA    |
|                  |  |   | Mil.                 | 25<br>35, 45    |                                      | 125<br>100      |                      | 100             |       |
| I <sub>SB1</sub> | Automatic $\overline{CE}_1$ Power Down Current | Max. V <sub>CC</sub> ,<br>$\overline{CE}_1 \geq V_{IH}$ ,<br>Min. Duty Cycle = 100%   | Coml.                |                 |                                      | 40              |                      | 20              | mA    |
|                  |  |   | Mil.                 | 25<br>35, 45    |                                      | 40<br>20        |                      | 20              |       |
| I <sub>SB2</sub> | Automatic $\overline{CE}_1$ Power Down Current | Max. V <sub>CC</sub> ,<br>$\overline{CE}_1 \geq V_{CC} - 0.3V$ ,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V<br>or V <sub>IN</sub> ≤ 0.3V | Coml.                |                 |                                      | 20              |                      | 20              | mA    |
|                  |  |   | Mil.                 |                 |                                      | 20              |                      | 20              |       |

### Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 7    |       |

#### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- V<sub>IL</sub> min. = -3.0V for pulse durations less than 30 ns.

### AC Test Loads and Waveforms

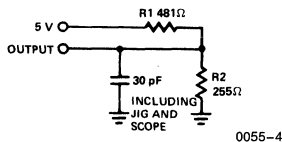


Figure 1a

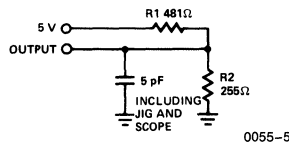


Figure 1b

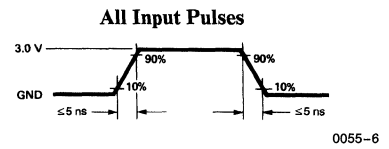
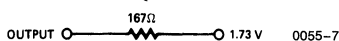


Figure 2

Equivalent to: THÉVENIN EQUIVALENT



## Switching Characteristics Over Operating Range<sup>[4, 5]</sup>

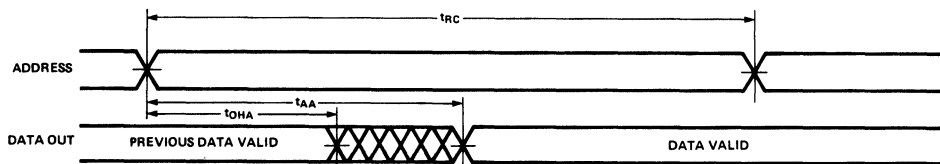
| Parameters                       | Description   | 7C185-20<br>7C186-20 |      | 7C185-25<br>7C186-25 |      | 7C185-35<br>7C186-35 |      | 7C185-45<br>7C186-45 |      | 7C185-55<br>7C186-55 |      | Units |
|----------------------------------|---|----------------------|------|----------------------|------|----------------------|------|----------------------|------|----------------------|------|-------|
|                                  |   | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. |       |
| <b>READ CYCLE</b>                |   |                      |      |                      |      |                      |      |                      |      |                      |      |       |
| t <sub>RC</sub>                  | Read Cycle Time   | 20                   |      | 25                   |      | 35                   |      | 45                   |      | 55                   |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid   |                      | 20   |                      | 25   |                      | 35   |                      | 45   |                      | 55   | ns    |
| t <sub>OHA</sub>                 | Data Hold from Address Change   | 5                    |      | 5                    |      | 5                    |      | 5                    |      | 5                    |      | ns    |
| t <sub>ACE<sub>1</sub></sub>     | $\overline{CE}_1$ LOW to Data Valid   |                      | 20   |                      | 25   |                      | 35   |                      | 45   |                      | 55   | ns    |
| t <sub>ACE<sub>2</sub></sub>     | CE <sub>2</sub> HIGH to Data Valid  |                      | 20   |                      | 25   |                      | 25   |                      | 30   |                      | 40   | ns    |
| t <sub>DOE</sub>                 | $\overline{OE}$ LOW to Data Valid   |                      | 10   |                      | 12   |                      | 15   |                      | 20   |                      | 25   | ns    |
| t <sub>LZOE</sub>                | $\overline{OE}$ LOW to Low Z  | 3                    |      | 3                    |      | 3                    |      | 3                    |      | 3                    |      | ns    |
| t <sub>HZOE</sub>                | $\overline{OE}$ HIGH to High Z <sup>[6]</sup>                                       |                      | 8    |                      | 10   |                      | 12   |                      | 15   |                      | 20   | ns    |
| t <sub>LZCE<sub>1</sub></sub>    | $\overline{CE}_1$ LOW to Low Z <sup>[7]</sup>                                       | 5                    |      | 5                    |      | 5                    |      | 5                    |      | 5                    |      | ns    |
| t <sub>LZCE<sub>2</sub></sub>    | CE <sub>2</sub> HIGH to Low Z   | 3                    |      | 3                    |      | 3                    |      | 3                    |      | 3                    |      | ns    |
| t <sub>HZCE</sub>                | $\overline{CE}_1$ HIGH to High Z <sup>[6, 7]</sup><br>CE <sub>2</sub> LOW to High Z |                      | 8    |                      | 10   |                      | 15   |                      | 15   |                      | 20   | ns    |
| t <sub>PU</sub>                  | $\overline{CE}_1$ LOW to Power Up   | 0                    |      | 0                    |      | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>PD</sub>                  | $\overline{CE}_1$ HIGH to Power Down  |                      | 20   |                      | 20   |                      | 20   |                      | 25   |                      | 25   | ns    |
| <b>WRITE CYCLE<sup>[8]</sup></b> |   |                      |      |                      |      |                      |      |                      |      |                      |      |       |
| t <sub>WC</sub>                  | Write Cycle Time  | 20                   |      | 20                   |      | 25                   |      | 40                   |      | 50                   |      | ns    |
| t <sub>SCE<sub>1</sub></sub>     | $\overline{CE}_1$ LOW to Write End  | 15                   |      | 20                   |      | 25                   |      | 30                   |      | 40                   |      | ns    |
| t <sub>SCE<sub>2</sub></sub>     | CE <sub>2</sub> HIGH to Write End   | 15                   |      | 20                   |      | 20                   |      | 25                   |      | 30                   |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End   | 15                   |      | 20                   |      | 25                   |      | 30                   |      | 40                   |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End   | 0                    |      | 0                    |      | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start   | 0                    |      | 0                    |      | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>PWE</sub>                 | WE Pulse Width  | 15                   |      | 15                   |      | 20                   |      | 20                   |      | 25                   |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End  | 10                   |      | 10                   |      | 15                   |      | 15                   |      | 25                   |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End  | 0                    |      | 0                    |      | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>HZWE</sub>                | WE LOW to High Z <sup>[6]</sup>   |                      | 7    |                      | 7    |                      | 10   |                      | 15   |                      | 20   | ns    |
| t <sub>LZWE</sub>                | WE HIGH to Low Z  | 5                    |      | 5                    |      | 5                    |      | 5                    |      | 5                    |      | ns    |

**Notes:**

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>O1</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW, CE<sub>2</sub> HIGH and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- WE is HIGH for read cycle.
- Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  = V<sub>IL</sub>. CE<sub>2</sub> = V<sub>IH</sub>.
- Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
- Data I/O is HIGH impedance if  $\overline{OE}$  = V<sub>IH</sub>.

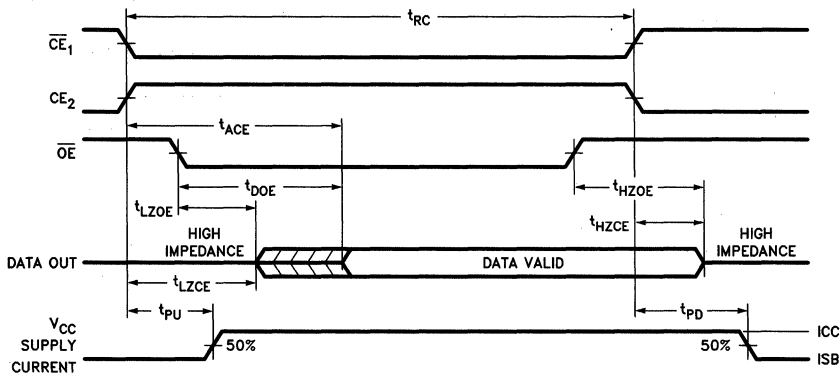
## Switching Waveforms

### Read Cycle No. 1 (Notes 10, 11)



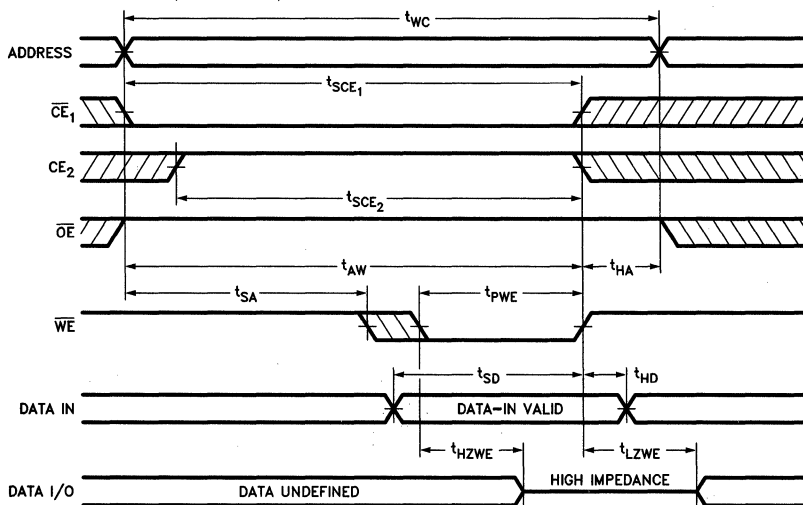
## Switching Waveforms (Continued)

### Read Cycle No. 2 (Notes 9, 11)



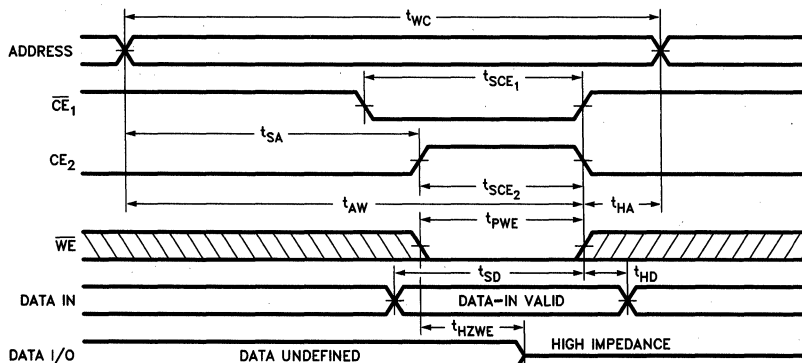
0055-9

### Write Cycle No. 1 ( $\overline{WE}$ Controlled) (Notes 8, 12)



0055-10

### Write Cycle No. 2 ( $\overline{CE}$ Controlled) (Notes 8, 12)

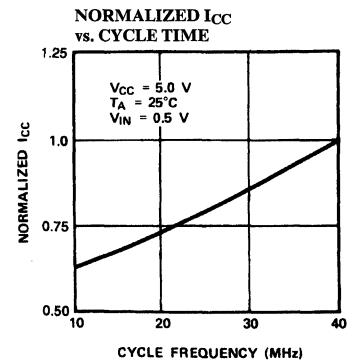
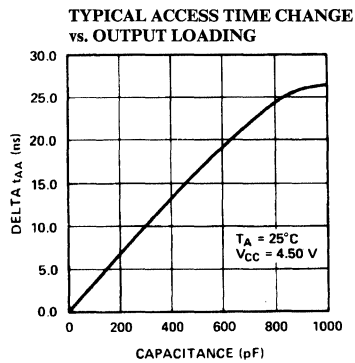
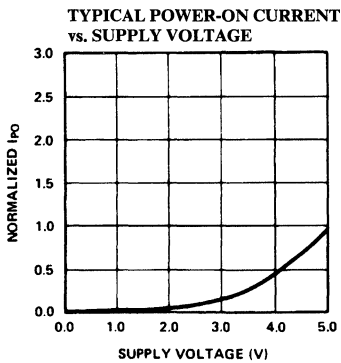
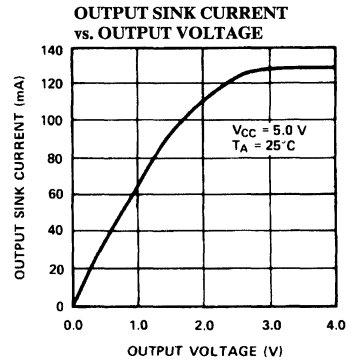
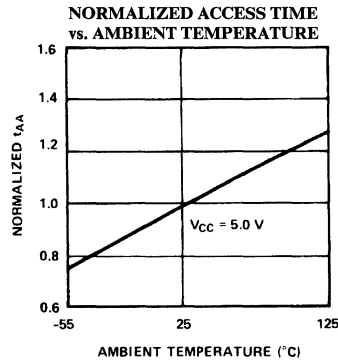
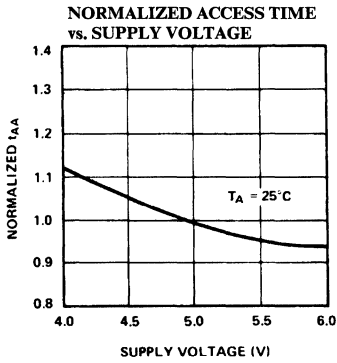
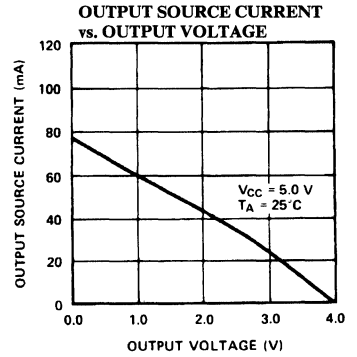
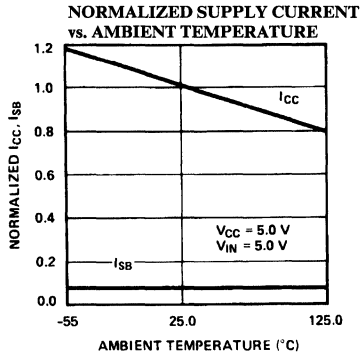
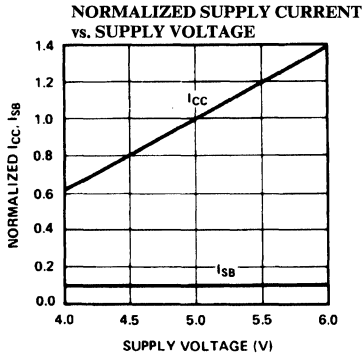


Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

0055-11

Typical DC and AC Characteristics

2



**Truth Table**

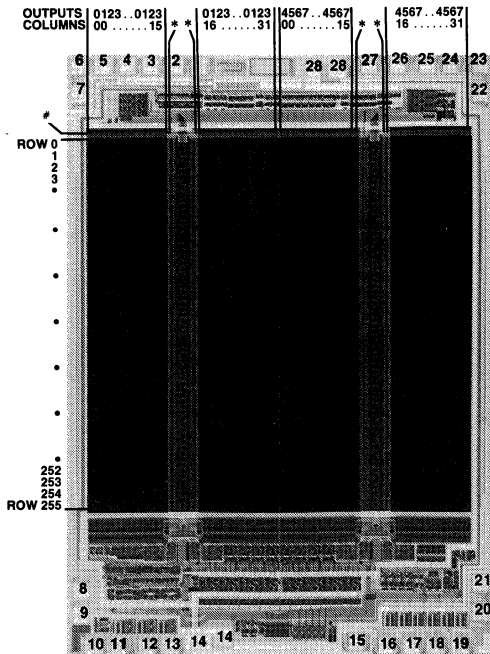
| $\overline{CE}_1$ | $CE_2$ | $\overline{WE}$ | $\overline{OE}$ | Input/Outputs | Mode                |
|-------------------|--------|-----------------|-----------------|---------------|---------------------|
| H                 | X      | X               | X               | High Z        | Deselect Power Down |
| X                 | L      | X               | X               | High Z        | Deselect            |
| L                 | H      | H               | L               | Data Out      | Read                |
| L                 | X      | L               | X               | Data In       | Write               |
| L                 | H      | H               | H               | High Z        | Deselect            |

**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 20         | CY7C185-20PC  | P21          | Commercial      |
|            | CY7C185-20VC  | V21          |                 |
|            | CY7C185-20DC  | D22          |                 |
|            | CY7C186-20LC  | L54          |                 |
| 25         | CY7C185-25PC  | P21          | Commercial      |
|            | CY7C185-25VC  | V21          |                 |
|            | CY7C185-25DC  | D22          |                 |
|            | CY7C185-25LC  | L54          |                 |
|            | CY7C185-25DMB | D22          | Military        |
|            | CY7C185-25LMB | L54          |                 |
|            | CY7C185-25KMB | K74          |                 |
| 35         | CY7C185-35PC  | P21          | Commercial      |
|            | CY7C185-35VC  | V21          |                 |
|            | CY7C185-35DC  | D22          |                 |
|            | CY7C185-35LC  | L54          |                 |
|            | CY7C185-35DMB | D22          | Military        |
|            | CY7C185-35LMB | L54          |                 |
|            | CY7C185-35KMB | K74          |                 |
| 45         | CY7C185-45PC  | P21          | Commercial      |
|            | CY7C185-45VC  | V21          |                 |
|            | CY7C185-45DC  | D22          |                 |
|            | CY7C185-45LC  | L54          |                 |
|            | CY7C185-45DMB | D22          | Military        |
|            | CY7C185-45LMB | L54          |                 |
|            | CY7C185-45KMB | K74          |                 |
| 55         | CY7C185-55PC  | P21          | Commercial      |
|            | CY7C185-55VC  | V21          |                 |
|            | CY7C185-55DC  | D22          |                 |
|            | CY7C185-55LC  | L54          |                 |
|            | CY7C185-55DMB | D22          | Military        |
|            | CY7C185-55LMB | L54          |                 |
|            | CY7C185-55KMB | K74          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 20         | CY7C186-20PC  | P21          | Commercial      |
|            | CY7C186-20DC  | D22          |                 |
| 25         | CY7C186-25PC  | P21          | Commercial      |
|            | CY7C186-25DC  | D22          |                 |
|            | CY7C186-25DMB | D22          | Military        |
| 35         | CY7C186-35PC  | P21          | Commercial      |
|            | CY7C186-35DC  | D22          |                 |
|            | CY7C186-35DMB | D22          | Military        |
| 45         | CY7C186-45PC  | P21          | Commercial      |
|            | CY7C186-45DC  | D22          |                 |
|            | CY7C186-45DMB | D22          | Military        |
| 55         | CY7C186-55PC  | P21          | Commercial      |
|            | CY7C186-55DC  | D22          |                 |
|            | CY7C186-55DMB | D22          | Military        |

## Bit Map



0055-14

## Address Designators

| Address Name | Address Function | Pin Number |
|--------------|------------------|------------|
| A4           | X3               | 2          |
| A5           | X4               | 3          |
| A6           | X5               | 4          |
| A7           | X6               | 5          |
| A8           | X7               | 6          |
| A9           | Y1               | 7          |
| A10          | Y4               | 8          |
| A11          | Y3               | 9          |
| A12          | Y0               | 10         |
| A0           | Y2               | 21         |
| A1           | X0               | 23         |
| A2           | X1               | 24         |
| A3           | X2               | 25         |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL</sub> Max. | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>OS</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB1</sub>     | 1,2,3     |
| I <sub>SB2</sub>     | 1,2,3     |

#### Switching Characteristics

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>ACE1</sub>  | 7,8,9,10,11 |
| t <sub>ACE2</sub>  | 7,8,9,10,11 |
| t <sub>DOE</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>SCE1</sub>  | 7,8,9,10,11 |
| t <sub>SCE2</sub>  | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |

Document #: 38-00037-D



**Features**

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed—20 ns
- Low active power — 440 mW
- Low standby power — 110 mW
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

**Functional Description**

The CY7C187 is a high performance CMOS static RAM organized as 65,536 words x 1 bit. Easy memory expansion is provided by an active LOW chip enable (CE) and three-state drivers. The CY7C187 has an automatic power-down feature, reducing the power consumption by 80% when deselected.

Writing to the device is accomplished when the chip enable (CE) and write enable (WE) inputs are both LOW.

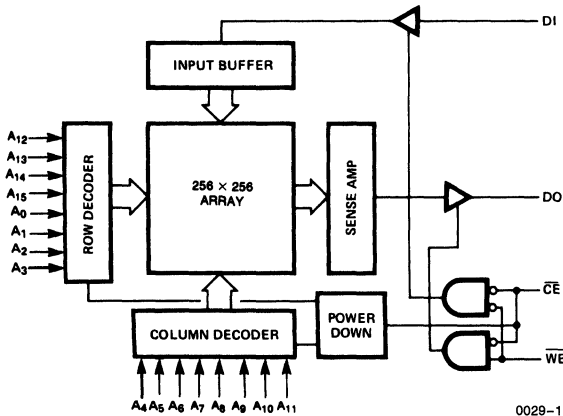
Data on the input pin (DI) is written into the memory location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>).

Reading the device is accomplished by taking the chip enable (CE) LOW, while write enable (WE) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

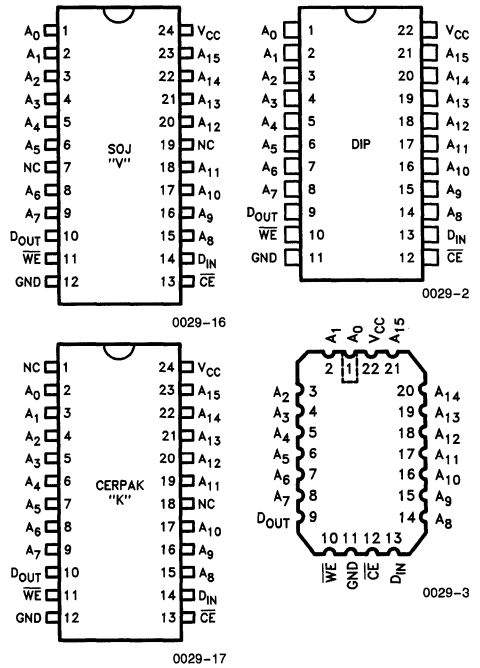
The output pin stays in high impedance state when chip enable (CE) is HIGH or write enable (WE) is LOW.

The 7C187 utilizes a Die Coat to ensure alpha immunity.

**Logic Block Diagram**



**Pin Configurations**



**Selection Guide**

|                                |            | 7C187-20 | 7C187-25 | 7C187-35 | 7C187-45 |
|--------------------------------|------------|----------|----------|----------|----------|
| Maximum Access Time (ns)       |            | 20       | 25       | 35       | 45       |
| Maximum Operating Current (mA) | Commercial | 80       | 70       | 70       | 50       |
|                                | Military   |          | 70       | 70       | 70       |
| Maximum Standby Current (mA)   | Commercial | 40/20    | 20/20    | 20/20    | 20/20    |
|                                | Military   |          | 40/20    | 20/20    | 20/20    |



### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature                                   | -65°C to +150°C |
| Ambient Temperature with Power Applied                | -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 22 to Pin 11) | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State         | -0.5V to +7.0V  |
| DC Input Voltage                                      | -3.0V to +7.0V  |
| Output Current into Outputs (Low)                     | 20 mA           |

|                          |  |
|--------------------------|--|
| Static Discharge Voltage | > 2001V<br>(Per MIL-STD-883 Method 3015) |
| Latch-up Current         | > 200 mA                                 |

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[4]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[5]</sup>

| Parameters       | Description   | Test Conditions  | 7C187-20   |                 | 7C187-25, 35 |                 | 7C187-45 |                 | Units |
|------------------|---|--|------------|-----------------|--------------|-----------------|----------|-----------------|-------|
|                  |   |  | Min.       | Max.            | Min.         | Max.            | Min.     | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage   | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA  | 2.4        |                 | 2.4          |                 | 2.4      |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage  | V <sub>CC</sub> = Min.<br>I <sub>OL</sub> = 8.0 mA Military<br>I <sub>OL</sub> = 12.0 mA Commercial                          |            | 0.4             |              | 0.4             |          | 0.4             | V     |
|                  |   |  |            |                 |              |                 |          |                 |       |
| V <sub>IH</sub>  | Input HIGH Voltage  |  | 2.2        | V <sub>CC</sub> | 2.2          | V <sub>CC</sub> | 2.2      | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage <sup>[5A]</sup>                           |  | -3.0       | 0.8             | -3.0         | 0.8             | -3.0     | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current  | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -10        | +10             | -10          | +10             | -10      | +10             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                                      | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled   | -10        | +10             | -10          | +10             | -10      | +10             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>                 | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND   |            | -350            |              | -350            |          | -350            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current                    | V <sub>CC</sub> = Max.<br>I <sub>O</sub> = 0 mA  | Commercial | 80              |              | 70              |          | 50              | mA    |
|                  |   |  | Military   |                 |              | 70              |          | 70              |       |
| I <sub>SB1</sub> | Automatic $\overline{CE}$ <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> ,<br>CE ≥ V <sub>IH</sub>   | Commercial | 40              |              | 20              |          | 20              | mA    |
|                  |   |  | Military   | 25              |              | 40              |          | 20              |       |
|                  |   |  |            | 35              |              | 20              |          |                 |       |
| I <sub>SB2</sub> | Automatic $\overline{CE}$ <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V | Commercial | 20              |              | 20              |          | 20              | mA    |
|                  |   |  | Military   |                 |              | 20              |          | 20              |       |

### Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 7    |       |

#### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the CE input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- V<sub>IL</sub> min. = -3.0V for pulse durations less than 30 ns.

### AC Test Loads and Waveforms

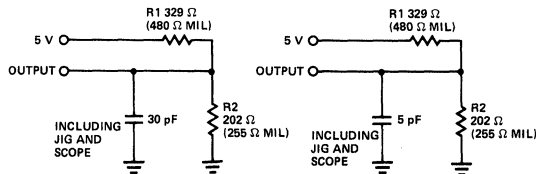


Figure 1a

Figure 1b

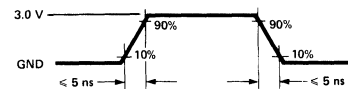
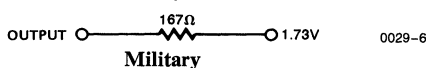


Figure 2

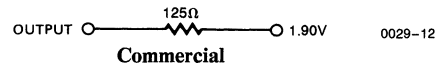
Equivalent to:

THÉVENIN EQUIVALENT



Military

0029-6



Commercial

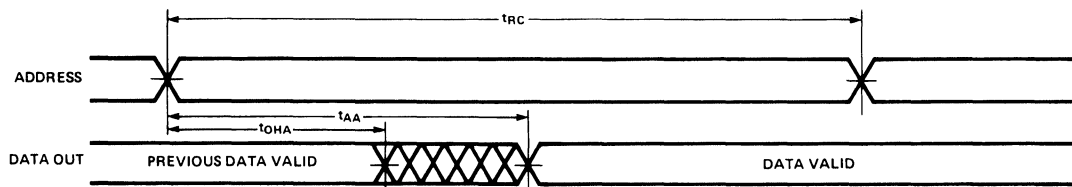
0029-12

**Switching Characteristics Over Operating Range**<sup>[5, 6]</sup>

| Parameters                        | Description                                      | 7C187-20 |      | 7C187-25 |      | 7C187-35 |      | 7C187-45 |      | Units |
|-----------------------------------|--|----------|------|----------|------|----------|------|----------|------|-------|
|                                   |  | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.     | Max. |       |
| <b>READ CYCLE</b>                 |  |          |      |          |      |          |      |          |      |       |
| t <sub>RC</sub>                   | Read Cycle Time                                  | 20       |      | 25       |      | 35       |      | 45       |      | ns    |
| t <sub>AA</sub>                   | Address to Data Valid                            |          | 20   |          | 25   |          | 35   |          | 45   | ns    |
| t <sub>OHA</sub>                  | Output Hold from Address Change                  | 5        |      | 5        |      | 5        |      | 5        |      | ns    |
| t <sub>ACE</sub>                  | $\overline{CE}$ LOW to Data Valid                |          | 20   |          | 25   |          | 35   |          | 45   | ns    |
| t <sub>LZCE</sub>                 | $\overline{CE}$ LOW to Low Z <sup>[8]</sup>      | 5        |      | 5        |      | 5        |      | 5        |      | ns    |
| t <sub>HZCE</sub>                 | $\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup> |          | 8    |          | 10   |          | 15   |          | 15   | ns    |
| t <sub>PU</sub>                   | $\overline{CE}$ LOW to Power Up                  | 0        |      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>PD</sub>                   | $\overline{CE}$ HIGH to Power Down               |          | 20   |          | 20   |          | 20   |          | 25   | ns    |
| <b>WRITE CYCLE</b> <sup>[9]</sup> |  |          |      |          |      |          |      |          |      |       |
| t <sub>WC</sub>                   | Write Cycle Time                                 | 20       |      | 20       |      | 25       |      | 40       |      | ns    |
| t <sub>SCE</sub>                  | $\overline{CE}$ LOW to Write End                 | 15       |      | 20       |      | 25       |      | 30       |      | ns    |
| t <sub>AW</sub>                   | Address Set-up to Write End                      | 15       |      | 20       |      | 25       |      | 30       |      | ns    |
| t <sub>HA</sub>                   | Address Hold from Write End                      | 0        |      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>SA</sub>                   | Address Set-up to Write Start                    | 0        |      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>PWE</sub>                  | $\overline{WE}$ Pulse Width                      | 15       |      | 15       |      | 20       |      | 20       |      | ns    |
| t <sub>SD</sub>                   | Data Set-up to Write End                         | 10       |      | 10       |      | 15       |      | 15       |      | ns    |
| t <sub>HD</sub>                   | Data Hold from Write End                         | 0        |      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>LZWE</sub>                 | $\overline{WE}$ HIGH to Low Z <sup>[8]</sup>     | 5        |      | 5        |      | 5        |      | 5        |      | ns    |
| t <sub>HZWE</sub>                 | $\overline{WE}$ LOW to High Z <sup>[7, 8]</sup>  |          | 7    |          | 7    |          | 10   |          | 15   | ns    |

**Notes:**

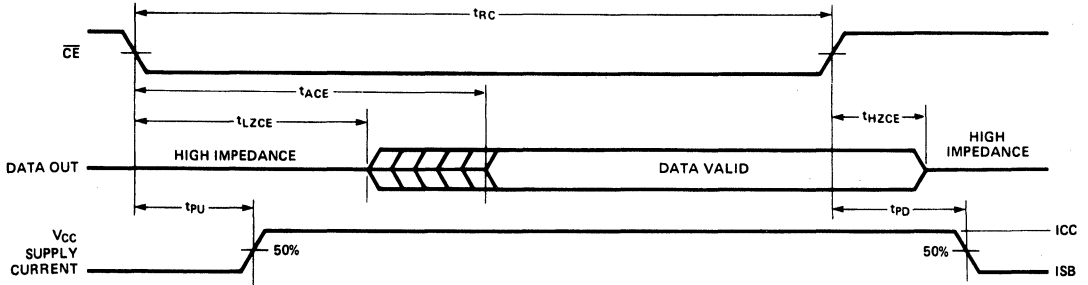
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CE} = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms**
**Read Cycle No. 1**<sup>[10, 11]</sup>


0029-7

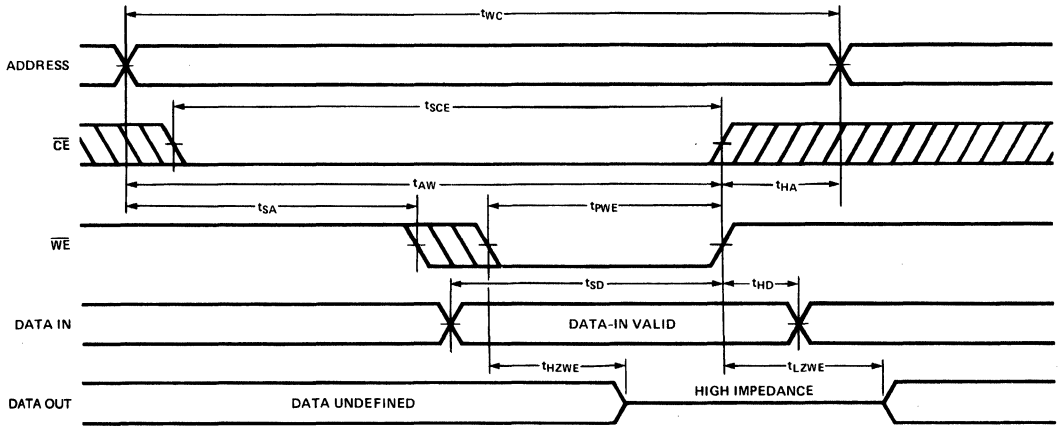
**Switching Waveforms (Continued)**

**Read Cycle No. 2 [10, 12]**



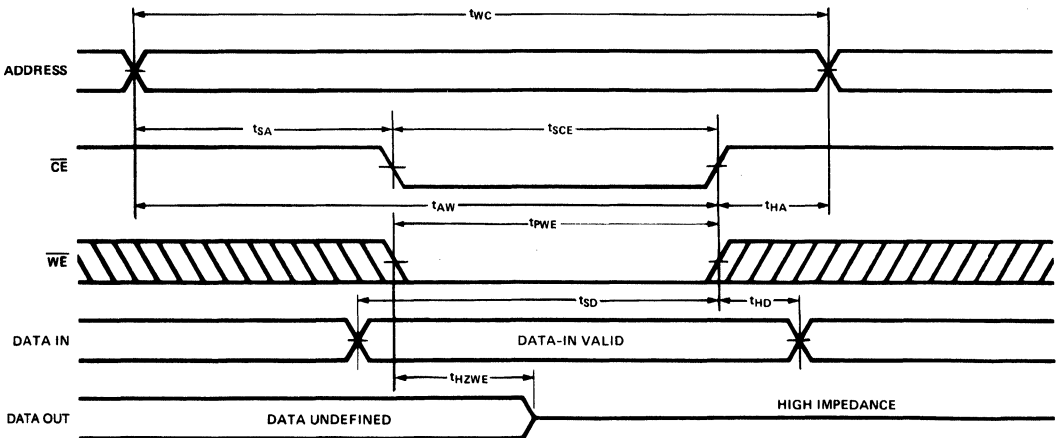
0029-8

**Write Cycle No. 1 ( $\overline{WE}$  Controlled) [9]**



0029-9

**Write Cycle No. 2 ( $\overline{CE}$  Controlled) [9]**

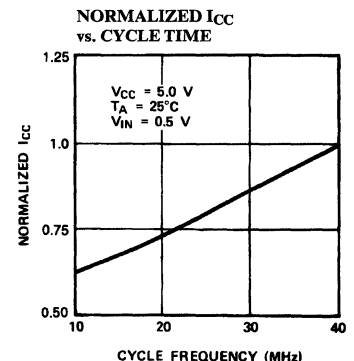
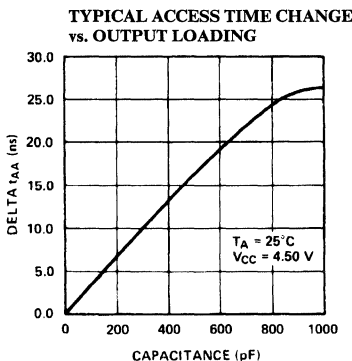
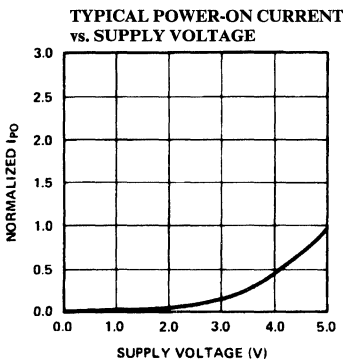
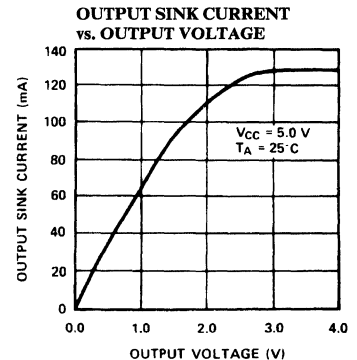
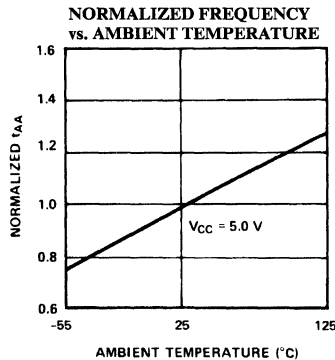
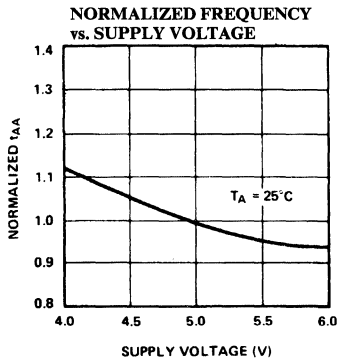
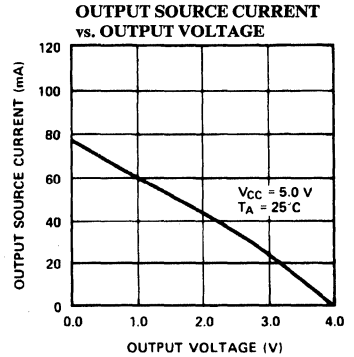
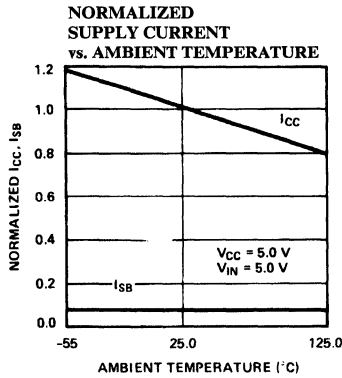
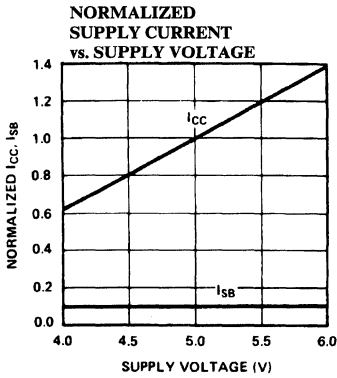


0029-10

Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

Typical DC and AC Characteristics

2



**Truth Table**

| CE | WE | Input/Outputs | Mode                |
|----|----|---------------|---------------------|
| H  | X  | High Z        | Deselect Power Down |
| L  | H  | Data Out      | Read                |
| L  | L  | Data In       | Write               |

**Ordering Information**

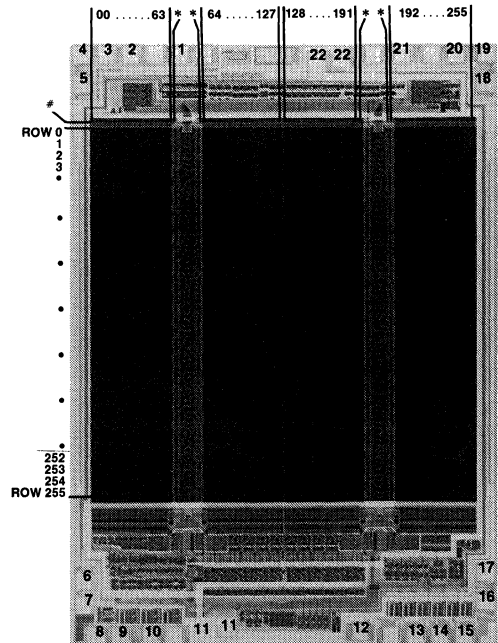
| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 20         | CY7C187-20PC  | P9           | Commercial      |
|            | CY7C187-20VC  | V13          |                 |
|            | CY7C187-20DC  | D10          |                 |
|            | CY7C187-20LC  | L52          |                 |
| 25         | CY7C187-25PC  | P9           | Commercial      |
|            | CY7C187-25VC  | V13          |                 |
|            | CY7C187-25DC  | D10          |                 |
|            | CY7C187-25LC  | L52          |                 |
|            | CY7C187-25DMB | D10          | Military        |
|            | CY7C187-25LMB | L52          |                 |
|            | CY7C187-25KMB | K73          |                 |

| Speed (ns)    | Ordering Code | Package Type | Operating Range |
|---------------|---------------|--------------|-----------------|
| 35            | CY7C187-35PC  | P9           | Commercial      |
|               | CY7C187-35VC  | V13          |                 |
|               | CY7C187-35DC  | D10          |                 |
|               | CY7C187-35LC  | L52          |                 |
|               | CY7C187-35DMB | D10          |                 |
| CY7C187-35LMB | L52           |              |                 |
| CY7C187-35KMB | K73           |              |                 |
| 45            | CY7C187-45PC  | P9           | Commercial      |
|               | CY7C187-45VC  | V13          |                 |
|               | CY7C187-45DC  | D10          |                 |
|               | CY7C187-45LC  | L52          |                 |
|               | CY7C187-45DMB | D10          | Military        |
|               | CY7C187-45LMB | L52          |                 |
|               | CY7C187-45KMB | K73          |                 |

### Address Designators

| Address Name | Address Function | Pin Number |
|--------------|------------------|------------|
| A0           | X3               | 1          |
| A1           | X4               | 2          |
| A2           | X5               | 3          |
| A3           | X6               | 4          |
| A4           | X7               | 5          |
| A5           | Y7               | 6          |
| A6           | Y6               | 7          |
| A7           | Y2               | 8          |
| A8           | Y3               | 14         |
| A9           | Y1               | 15         |
| A10          | Y0               | 16         |
| A11          | Y4               | 17         |
| A12          | Y5               | 18         |
| A13          | X0               | 19         |
| A14          | X1               | 20         |
| A15          | X2               | 21         |

### Bit Map



2

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>OS</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB1</sub>     | 1,2,3     |
| I <sub>SB2</sub>     | 1,2,3     |

**Switching Characteristics**

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>ACE</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>SCE</sub>   | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |

Document #: 38-00038-E



**Features**

- Fully decoded, 16 word x 4-bit high speed CMOS RAMs
- Inverting outputs CY7C189
- Non-inverting outputs CY7C190
- High speed
  - 15 ns and 25 ns commercial
  - 25 ns military
- Low power
  - 303 mW at 25 ns
  - 495 mW at 15 ns
- Power supply 5V ± 10%
- Advanced high speed CMOS processing for optimum speed/power product
- Capable of withstanding greater than 2000V static discharge
- Three-state outputs
- TTL compatible interface levels

**Functional Description**

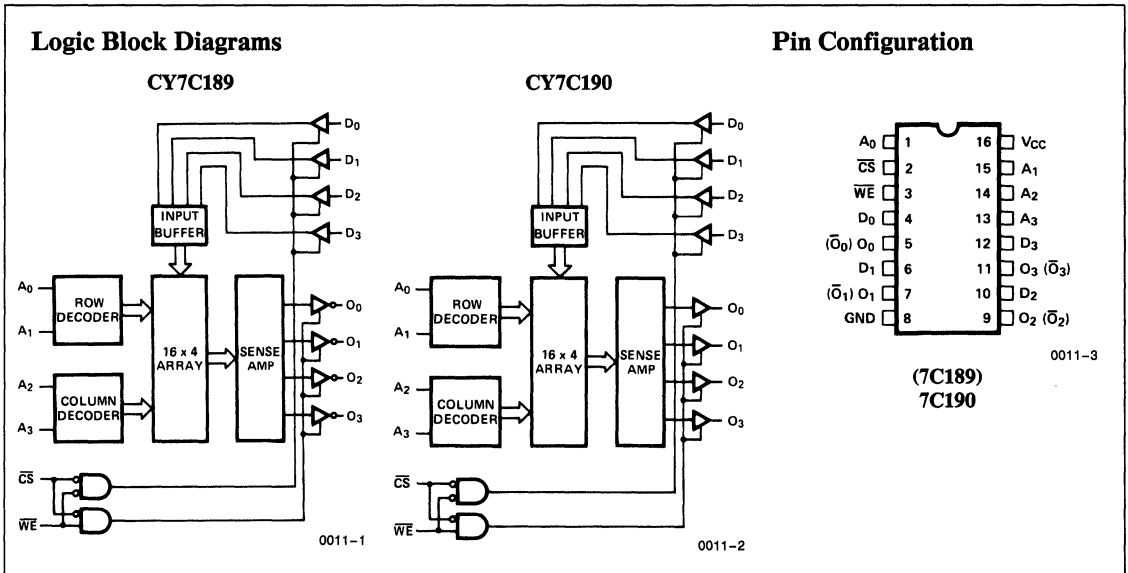
The CY7C189 and CY7C190 are extremely high performance 64-bit static RAMs organized as 16 words x 4-bits. Easy memory expansion is provided by an active LOW chip select (CS) input and three-state outputs. The devices are provided with inverting (CY7C189) and non-inverting (CY7C190) outputs.

An active LOW write enable (WE) signal controls the writing and reading of the memory. When the write enable (WE) and chip select (CS) are both LOW the information on the four data inputs (D<sub>0</sub>–D<sub>3</sub>) is written into the location addressed by the information on the address lines (A<sub>0</sub>–A<sub>3</sub>). The outputs are preconditioned such that the cor-

rect data is present at the data outputs (O<sub>0</sub>–O<sub>3</sub>) when the write cycle is complete. This precondition operation insures minimum write recovery times by eliminating the “write recovery glitch”.

Reading is accomplished with an active LOW on the chip select line (CS) and a HIGH on the write enable (WE) line. The information stored is read out from the addressed location and presented at the outputs in inverted (CY7C189) or non-inverted (CY7C190) format.

During the write operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.



**Selection Guide**

|                                |            | 7C189-15<br>7C190-15 | 7C189-25<br>7C190-25 |
|--------------------------------|------------|----------------------|----------------------|
| Maximum Access Time (ns)       | Commercial | 15                   | 25                   |
|                                | Military   |                      | 25                   |
| Maximum Operating Current (mA) | Commercial | 90                   | 55                   |
|                                | Military   |                      | 70                   |



### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied ..... -55°C to +125°C  
 Supply Voltage to Ground Potential  
 (Pin 16 to Pin 8) ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs  
 in High Z State ..... -0.5V to +7.0V  
 DC Input Voltage ..... -3.0V to +7.0V  
 Output Current, into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V  
 (per MIL-STD-883 Method 3015)

Latchup Current ..... >200 mA

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[4]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over the Operating Range<sup>[5]</sup>

| Parameters      | Description                                 | Test Conditions                                    | 7C189-15<br>7C190-15 |                 | 7C189-25<br>7C190-25 |                 | Units |
|-----------------|---|--|----------------------|-----------------|----------------------|-----------------|-------|
|                 |   |  | Min.                 | Max.            | Min.                 | Max.            |       |
| V <sub>OH</sub> | Output HIGH Voltage                         | V <sub>CC</sub> = Min., I <sub>OH</sub> = -5.2 mA  | 2.4                  |                 | 2.4                  |                 | V     |
| V <sub>OL</sub> | Output LOW Voltage                          | V <sub>CC</sub> = Min., I <sub>OL</sub> = 16.0 mA  |                      | 0.45            |                      | 0.45            | V     |
| V <sub>IH</sub> | Input HIGH Voltage                          |  | 2.0                  | V <sub>CC</sub> | 2.0                  | V <sub>CC</sub> | V     |
| V <sub>IL</sub> | Input LOW Voltage                           |  | -3.0                 | 0.8             | -3.0                 | 0.8             | V     |
| I <sub>IX</sub> | Input Leakage Current                       | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>             | -10                  | +10             | -10                  | +10             | μA    |
| V <sub>CD</sub> | Input Diode Clamp Voltage <sup>[1]</sup>    |  |                      |                 |                      |                 |       |
| I <sub>OZ</sub> | Output Leakage Current                      | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub>             | -40                  | +40             | -40                  | +40             | μA    |
| I <sub>OS</sub> | Output Short Circuit Current <sup>[2]</sup> | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND     |                      | -90             |                      | -90             | mA    |
| I <sub>CC</sub> | Power Supply Current                        | V <sub>CC</sub> = Max.,<br>I <sub>OUT</sub> = 0 mA | Commercial           | 90              |                      | 55              | mA    |
|                 |   |  | Military             |                 |                      | 70              | mA    |

### Capacitance<sup>[6]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 4    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 7    |       |

#### Notes:

- The CMOS process does not provide a clamp diode. However the CY7C189 and CY7C190 are insensitive to -3V dc input levels and -5V undershoot pulses of less than 5 ns (measured at 50% points).
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Output is preconditioned to data in (inverted or non-inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch).
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.

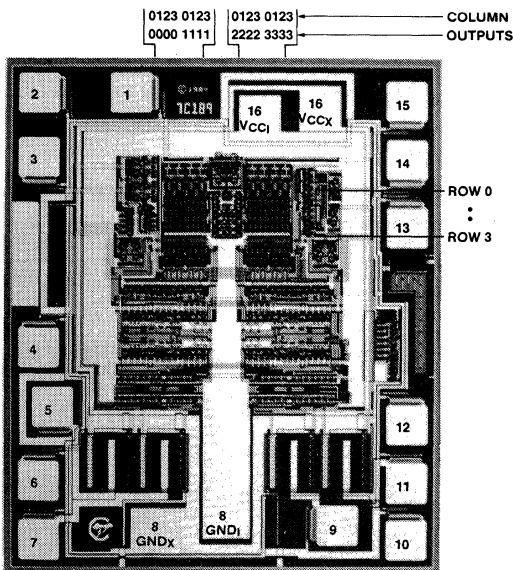
## Switching Characteristics Over the Operating Range<sup>[5, 7]</sup>

| Parameter                           | Description                           | Test Conditions | 7C189-15<br>7C190-15 |      | 7C189-25<br>7C190-25 |      | Units |
|-------------------------------------|---------------------------------------|-----------------|----------------------|------|----------------------|------|-------|
|                                     |                                       |                 | Min.                 | Max. | Min.                 | Max. |       |
| <b>READ CYCLE</b>                   |                                       |                 |                      |      |                      |      |       |
| t <sub>RC</sub>                     | Read Cycle Time                       |                 | 15                   |      | 25                   |      | ns    |
| t <sub>ACS</sub>                    | Chip Select to Output Valid           | Note 10         |                      | 12   |                      | 15   | ns    |
| t <sub>HZCS</sub>                   | Chip Select Inactive to High Z        | Notes 9, 11     |                      | 12   |                      | 15   | ns    |
| t <sub>LZCS</sub>                   | Chip Select Active to Low Z           |                 |                      | 12   |                      | 15   | ns    |
| t <sub>OHA</sub>                    | Output Hold from Address Change       |                 | 5                    |      | 5                    |      | ns    |
| t <sub>AA</sub>                     | Address Access Time                   | Note 10         |                      | 15   |                      | 25   | ns    |
| <b>WRITE CYCLE<sup>[3, 8]</sup></b> |                                       |                 |                      |      |                      |      |       |
| t <sub>WC</sub>                     | Write Cycle Time                      |                 | 15                   |      | 20                   |      | ns    |
| t <sub>HZWE</sub>                   | Write Enable Active to High Z         | Notes 9, 11     |                      | 12   |                      | 20   | ns    |
| t <sub>LZWE</sub>                   | Write Enable Inactive to Low Z        |                 |                      | 12   |                      | 20   | ns    |
| t <sub>AWE</sub>                    | Write Enable Inactive to Output Valid | Note 10         |                      | 12   |                      | 20   | ns    |
| t <sub>PWE</sub>                    | Write Enable Pulse Width              |                 | 15                   |      | 20                   |      | ns    |
| t <sub>SD</sub>                     | Data Setup to Write End               |                 | 15                   |      | 20                   |      | ns    |
| t <sub>HD</sub>                     | Data Hold from Write End              |                 | 0                    |      | 0                    |      | ns    |
| t <sub>SA</sub>                     | Address Setup to Write Start          |                 | 0                    |      | 0                    |      | ns    |
| t <sub>HA</sub>                     | Address Hold from Write End           |                 | 0                    |      | 0                    |      | ns    |

**Notes:**

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- The internal write time of the memory is defined by the overlap of CS LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- Transition is measured at steady state HIGH level - 500 mV or steady state LOW level + 500 mV on the output from 1.5V level on the input.
- t<sub>AA</sub>, t<sub>ACS</sub> and t<sub>AWE</sub> are tested with C<sub>L</sub> = 30 pF as in Figure 1a. Timing is referenced to 1.5V on the inputs and outputs.
- t<sub>HZCS</sub> and t<sub>HZWE</sub> are tested with C<sub>L</sub> = 5 pF as in Figure 1b.

## Bit Map



## Address Designators

| Address Name   | Address Function | Pin Number |
|----------------|------------------|------------|
| A <sub>0</sub> | AX0              | 1          |
| A <sub>1</sub> | AX1              | 15         |
| A <sub>2</sub> | AY0              | 14         |
| A <sub>3</sub> | AY1              | 13         |

### AC Test Loads and Waveforms

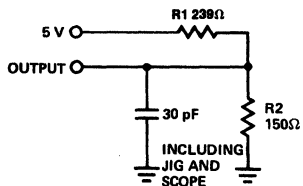


Figure 1a

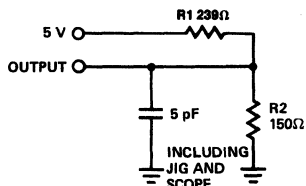
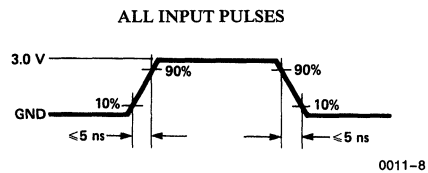


Figure 1b

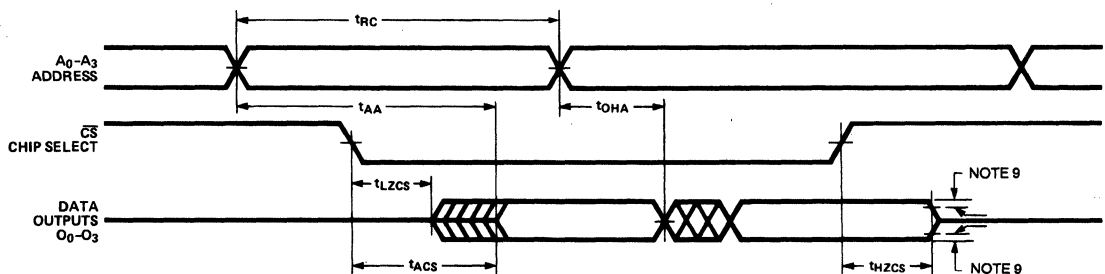


Equivalent to:

THÉVENIN EQUIVALENT

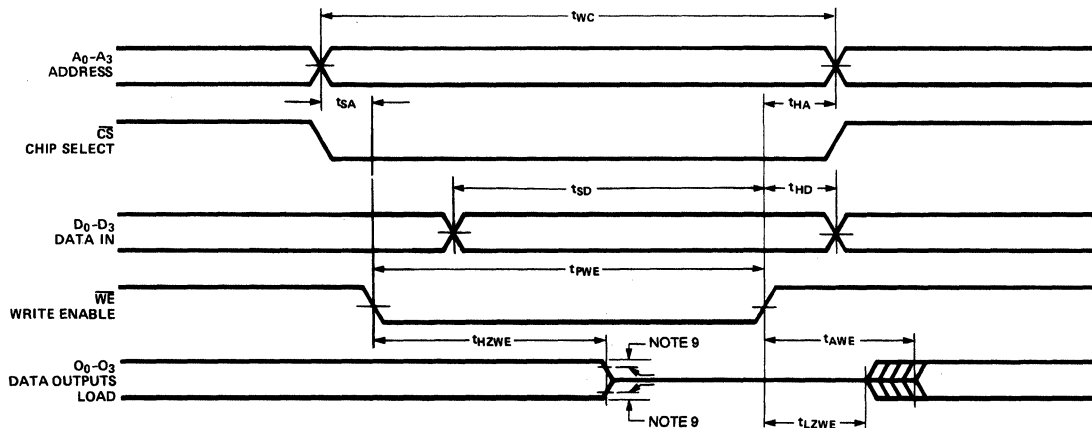


### Read Mode



0011-9

### Write Mode



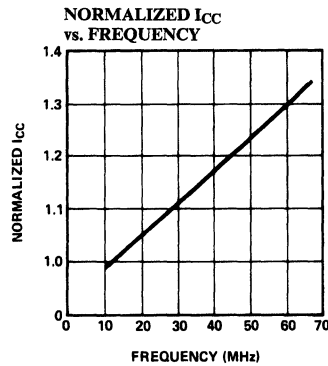
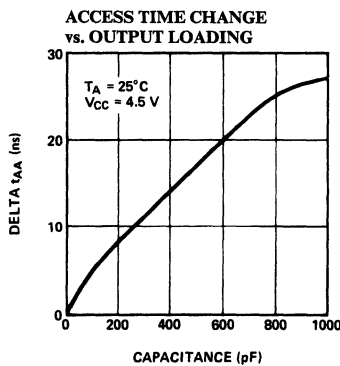
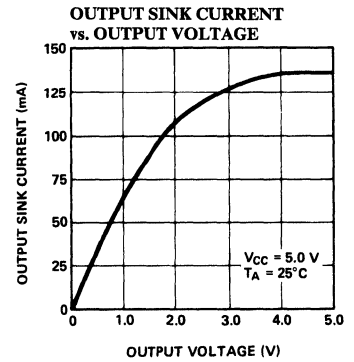
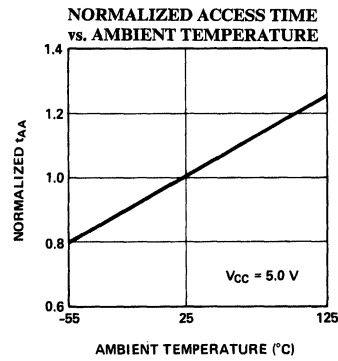
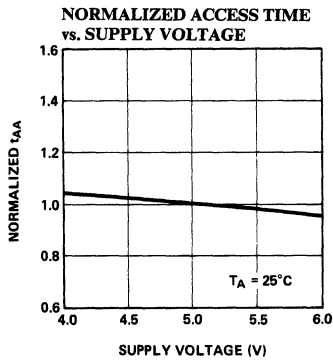
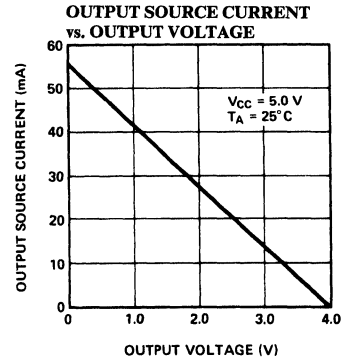
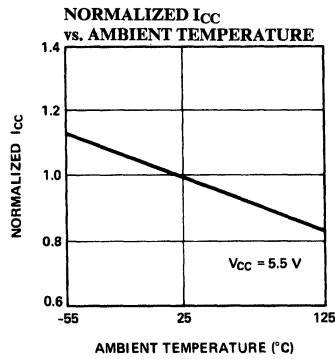
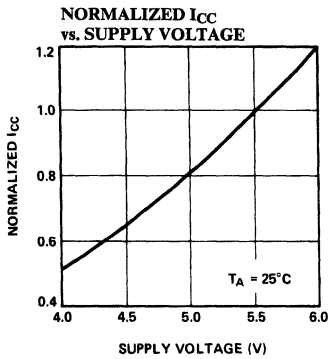
0011-10

(All above measurements referenced to 1.5V.)

**Note:**

Timing diagram represents one solution which results in an optimum cycle time. Timing may be changed in various applications as long as the worst case limits are not violated.

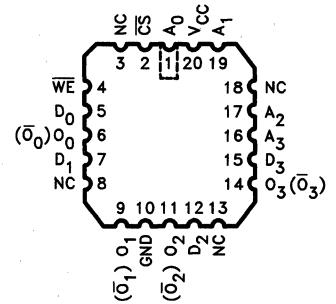
## Typical DC and AC Characteristics



### Ordering Information

| Speed (ns) | Ordering Code                  | Package Type | Operating Range |
|------------|--------------------------------|--------------|-----------------|
| 15         | CY7C189-15PC<br>CY7C190-15PC   | P1           | Commercial      |
|            | CY7C189-15DC<br>CY7C190-15DC   | D2           |                 |
|            | CY7C189-15LC<br>CY7C190-15LC   | L61          |                 |
| 25         | CY7C189-25PC<br>CY7C190-25PC   | P1           | Commercial      |
|            | CY7C189-25DC<br>CY7C190-25DC   | D2           |                 |
|            | CY7C189-25LC<br>CY7C190-25LC   | L61          |                 |
|            | CY7C189-25DMB<br>CY7C190-25DMB | D2           |                 |
|            | CY7C189-25LMB<br>CY7C190-25LMB | L61          | Military        |

### Pin Configuration



(7C189)  
7C190

0011-4

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL</sub> Max. | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |

2

#### Switching Characteristics

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>ACS</sub>   | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>AWE</sub>   | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |

Document #: 38-00039-B



**65,536 x 4 Static R/W RAM**  
**Separate I/O**

**Features**

- Automatic power-down when deselected
- Transparent write (7C191)
- CMOS for optimum speed/power
- High speed  
— 25 ns  $t_{AA}$
- Low active power  
— 385 mW
- Low standby power  
— 110 mW
- TTL compatible inputs and outputs

- Capable of withstanding greater than 2001V electrostatic discharge

**Functional Description**

The CY7C191 and CY7C192 are high performance CMOS static RAMs organized as 65,536 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enable ( $\overline{CE}$ ) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 71% when deselected.

Writing to the device is accomplished when the chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW.

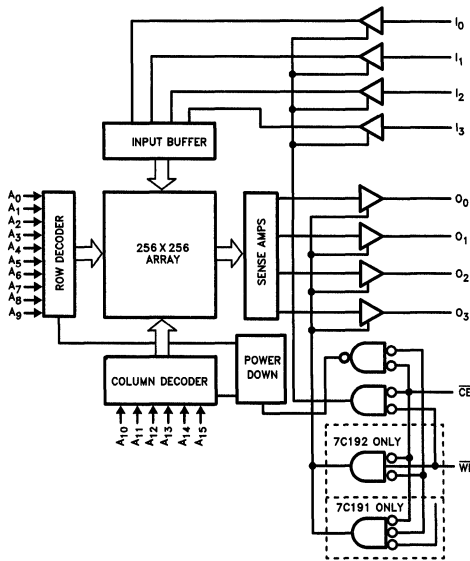
Data on the four input pins ( $I_0$  through  $I_3$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{15}$ ).

Reading the device is accomplished by taking the chip enable ( $\overline{CE}$ ) LOW, while the write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

The output pins stay in high impedance state when write enable ( $\overline{WE}$ ) is LOW (7C192 only), or chip enable ( $\overline{CE}$ ) is HIGH.

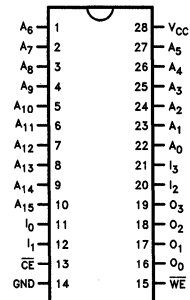
A die coat is used to insure alpha immunity.

**Logic Block Diagram**

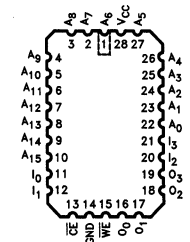


0108-1

**Pin Configurations**



0108-2



0108-10

**Selection Guide**

|                                |            | <b>7C191-25</b><br><b>7C192-25</b> | <b>7C191-35</b><br><b>7C192-35</b> | <b>7C191-45</b><br><b>7C192-45</b> |
|--------------------------------|------------|------------------------------------|------------------------------------|------------------------------------|
| Maximum Access Time (ns)       |            | 25                                 | 35                                 | 45                                 |
| Maximum Operating Current (mA) | Commercial | 80                                 | 80                                 | 70                                 |
|                                | Military   |                                    | 90                                 | 90                                 |
| Maximum Standby Current (mA)   | Commercial | 20                                 | 20                                 | 20                                 |
|                                | Military   |                                    | 20                                 | 20                                 |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V  
(Per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[2]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[3]</sup>

| Parameters       | Description                                  | Test Conditions   | 7C191-25   |                 | 7C191-35 |                 | 7C191-45 |                 | Units |
|------------------|--|---|------------|-----------------|----------|-----------------|----------|-----------------|-------|
|                  |  |   | Min.       | Max.            | Min.     | Max.            | Min.     | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA   | 2.4        |                 | 2.4      |                 | 2.4      |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA  |            | 0.4             |          | 0.4             |          | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                           |   | 2.2        | V <sub>CC</sub> | 2.2      | V <sub>CC</sub> | 2.2      | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage                            |   | -3.0       | 0.8             | -3.0     | 0.8             | -3.0     | 0.8             | V     |
| I <sub>Ix</sub>  | Input Load Current                           | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>  | -10        | +10             | -10      | +10             | -10      | +10             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                       | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled  | -10        | +10             | -10      | +10             | -10      | +10             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>  | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND  |            | -350            |          | -350            |          | -350            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current     | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA   | Commercial | 80              |          | 80              |          | 70              | mA    |
|                  |  |   | Military   |                 |          |                 | 90       | 90              |       |
| I <sub>SB1</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$<br>Min. Duty Cycle = 100%  | Commercial | 20              |          | 20              |          | 20              | mA    |
|                  |  |   | Military   | 20              |          | 20              |          | 20              |       |
| I <sub>SB2</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> ,<br>$\overline{CE} \geq V_{CC} - 0.3V$<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V | Commercial | 20              |          | 20              |          | 20              | mA    |
|                  |  |   | Military   |                 |          | 20              |          | 20              |       |

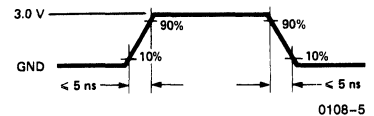
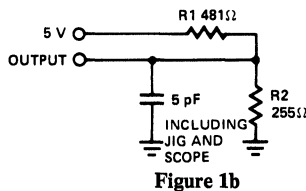
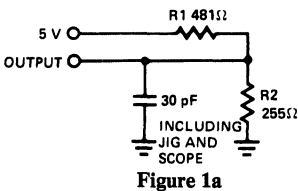
### Capacitance<sup>[4]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 7    | pF    |

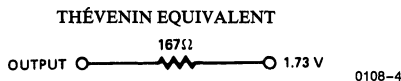
**Notes:**

- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.

### AC Test Loads and Waveforms



Equivalent to:





### Switching Characteristics Over Operating Range<sup>[3, 5]</sup>

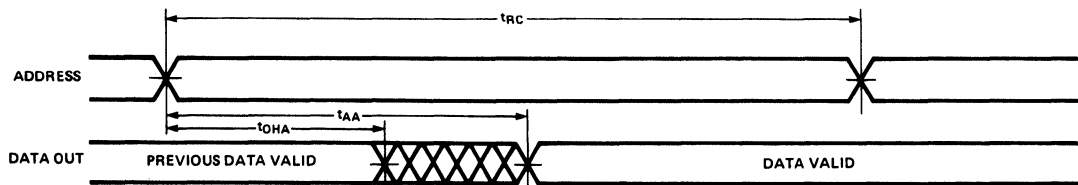
| Parameters                       | Description   | 7C191-25<br>7C192-25 |      | 7C191-35<br>7C192-35 |      | 7C191-45<br>7C192-45 |      | Units |
|----------------------------------|---|----------------------|------|----------------------|------|----------------------|------|-------|
|                                  |   | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. |       |
| <b>READ CYCLE</b>                |   |                      |      |                      |      |                      |      |       |
| t <sub>RC</sub>                  | Read Cycle Time   | 25                   |      | 35                   |      | 45                   |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid                                   |                      | 25   |                      | 35   |                      | 45   | ns    |
| t <sub>OHA</sub>                 | Output Hold from Address Change                         | 3                    |      | 3                    |      | 3                    |      | ns    |
| t <sub>ACE</sub>                 | $\overline{CE}$ LOW to Data Valid                       |                      | 25   |                      | 35   |                      | 45   | ns    |
| t <sub>LZCE</sub>                | $\overline{CE}$ LOW to LOW Z <sup>[7]</sup>             | 3                    |      | 3                    |      | 3                    |      | ns    |
| t <sub>HZCE</sub>                | $\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>        |                      | 10   |                      | 15   |                      | 15   | ns    |
| t <sub>PU</sub>                  | $\overline{CE}$ LOW to Power Up                         | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>PD</sub>                  | $\overline{CE}$ HIGH to Power Down                      |                      | 25   |                      | 35   |                      | 45   | ns    |
| <b>WRITE CYCLE<sup>[8]</sup></b> |   |                      |      |                      |      |                      |      |       |
| t <sub>WC</sub>                  | Write Cycle Time  | 20                   |      | 30                   |      | 40                   |      | ns    |
| t <sub>SCE</sub>                 | $\overline{CE}$ LOW to Write End                        | 20                   |      | 30                   |      | 35                   |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End                             | 20                   |      | 25                   |      | 35                   |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End                             | 2                    |      | 2                    |      | 2                    |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                           | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>PWE</sub>                 | $\overline{WE}$ Pulse Width                             | 20                   |      | 25                   |      | 35                   |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End                                | 10                   |      | 15                   |      | 20                   |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End                                | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>LZWE</sub>                | $\overline{WE}$ HIGH to Low Z <sup>[7]</sup> (7C192)    | 3                    |      | 3                    |      | 3                    |      | ns    |
| t <sub>HZWE</sub>                | $\overline{WE}$ LOW to High Z <sup>[6, 7]</sup> (7C192) |                      | 10   |                      | 10   |                      | 15   | ns    |
| t <sub>AWE</sub>                 | $\overline{WE}$ LOW to Data Valid (7C191)               |                      | 25   |                      | 30   |                      | 35   | ns    |
| t <sub>ADV</sub>                 | Data Valid to Output Valid (7C191)                      |                      | 20   |                      | 30   |                      | 35   | ns    |

**Notes:**

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
6. t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
7. At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> for any given device.
8. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
9.  $\overline{WE}$  is HIGH for read cycle.
10. Device is continuously selected.  $\overline{CE} = V_{IL}$ .
11. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

### Switching Waveforms

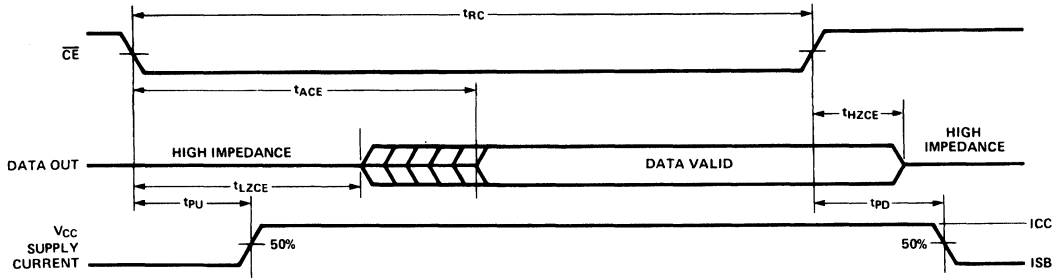
#### Read Cycle No. 1 (Notes 9, 10)



0108-6

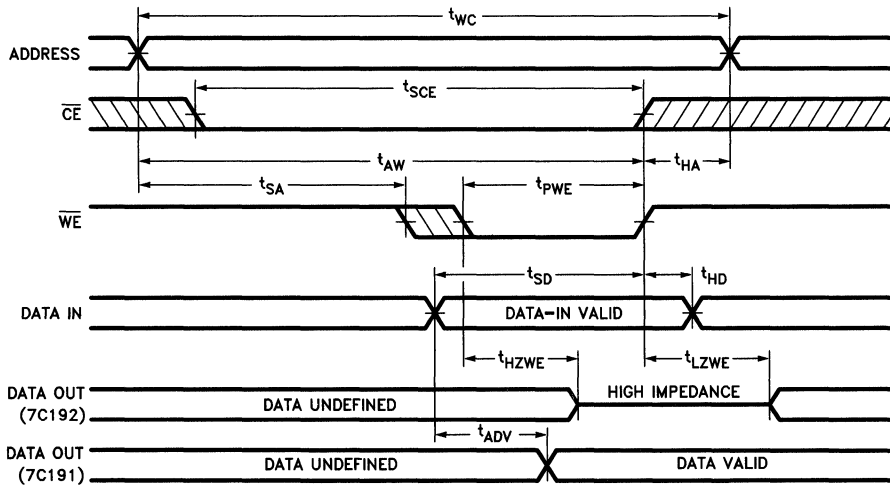
### Switching Waveforms (Continued)

#### Read Cycle (Notes 9, 11)



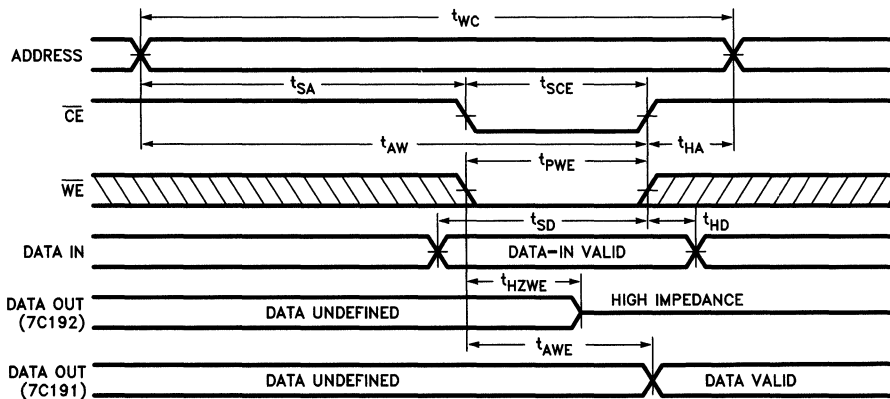
0108-7

#### Write Cycle No. 1 ( $\overline{WE}$ Controlled) (Note 8)



0108-8

#### Write Cycle No. 2 ( $\overline{CE}$ Controlled) (Note 8)



Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state (7C192 only).

0108-9

**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C191-25PC  | P21          | Commercial      |
|            | CY7C191-25VC  | V21          |                 |
|            | CY7C191-25DC  | D22          |                 |
|            | CY7C191-25LC  | L54          |                 |
| 35         | CY7C191-35PC  | P21          | Commercial      |
|            | CY7C191-35VC  | V21          |                 |
|            | CY7C191-35DC  | D22          |                 |
|            | CY7C191-35LC  | L54          |                 |
|            | CY7C191-35DMB | D22          | Military        |
|            | CY7C191-35LMB | L54          |                 |
| 45         | CY7C191-45PC  | P21          | Commercial      |
|            | CY7C191-45VC  | V21          |                 |
|            | CY7C191-45DC  | D22          |                 |
|            | CY7C191-45LC  | L54          |                 |
|            | CY7C191-45DMB | D22          | Military        |
|            | CY7C191-45LMB | L54          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C192-25PC  | P21          | Commercial      |
|            | CY7C192-25VC  | V21          |                 |
|            | CY7C192-25DC  | D22          |                 |
|            | CY7C192-25LC  | L54          |                 |
| 35         | CY7C192-35PC  | P21          | Commercial      |
|            | CY7C192-35VC  | V21          |                 |
|            | CY7C192-35DC  | D22          |                 |
|            | CY7C192-35LC  | L54          |                 |
|            | CY7C192-35DMB | D22          | Military        |
|            | CY7C192-35LMB | L54          |                 |
| 45         | CY7C192-45PC  | P21          | Commercial      |
|            | CY7C192-45VC  | V21          |                 |
|            | CY7C192-45DC  | D22          |                 |
|            | CY7C192-45LC  | L54          |                 |
|            | CY7C192-45DMB | D22          | Military        |
|            | CY7C192-45LMB | L54          |                 |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>Ix</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>OS</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB1</sub>     | 1,2,3     |
| I <sub>SB2</sub>     | 1,2,3     |

2

#### Switching Characteristics

| Parameters                      | Subgroups   |
|---------------------------------|-------------|
| <b>READ CYCLE</b>               |             |
| t <sub>RC</sub>                 | 7,8,9,10,11 |
| t <sub>AA</sub>                 | 7,8,9,10,11 |
| t <sub>OHA</sub>                | 7,8,9,10,11 |
| t <sub>ACE</sub>                | 7,8,9,10,11 |
| <b>WRITE CYCLE</b>              |             |
| t <sub>WC</sub>                 | 7,8,9,10,11 |
| t <sub>SCE</sub>                | 7,8,9,10,11 |
| t <sub>AW</sub>                 | 7,8,9,10,11 |
| t <sub>HA</sub>                 | 7,8,9,10,11 |
| t <sub>SA</sub>                 | 7,8,9,10,11 |
| t <sub>PWE</sub>                | 7,8,9,10,11 |
| t <sub>SD</sub>                 | 7,8,9,10,11 |
| t <sub>HD</sub>                 | 7,8,9,10,11 |
| t <sub>AWE</sub> <sup>[1]</sup> | 7,8,9,10,11 |
| t <sub>ADV</sub> <sup>[1]</sup> | 7,8,9,10,11 |

**Note:**

1. 7C191 only.

Document #: 38-00076-A



**Features**

- Automatic power-down when deselected
- Output Enable ( $\overline{OE}$ ) feature (7C196)
- CMOS for optimum speed/power
- High speed  
— 25 ns  $t_{AA}$
- Low active power  
— 385 mW
- Low standby power  
— 110 mW
- TTL compatible inputs and outputs

- Capable of withstanding greater than 2001V electrostatic discharge

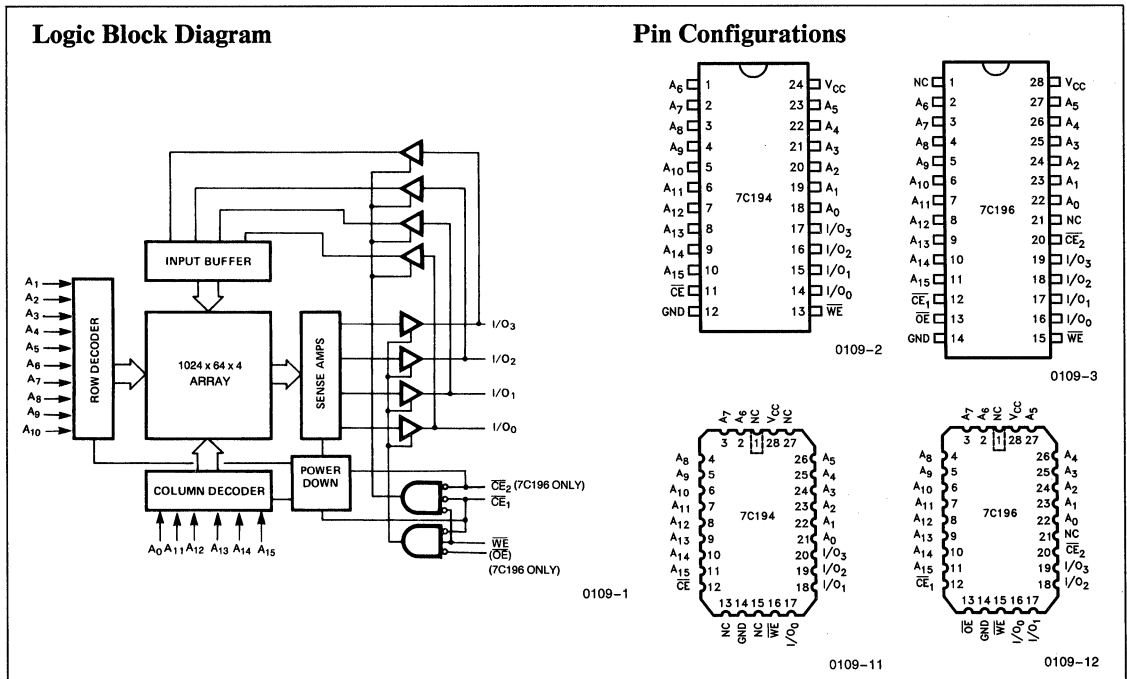
**Functional Description**

The CY7C194 and CY7C196 are high performance CMOS static RAMs organized as 65,536 x 4 bits. Easy memory expansion is provided by active LOW chip enable(s) ( $\overline{CE}$  on the CY7C194,  $\overline{CE}_1$ ,  $\overline{CE}_2$  on the CY7C196) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 71% when deselected.

Writing to the device is accomplished when the chip enable(s) ( $\overline{CE}$  on the

CY7C194,  $\overline{CE}_1$ ,  $\overline{CE}_2$  on the CY7C196) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the four input pins ( $I/O_0$  through  $I/O_3$ ) is written into the memory location, specified on the address pins ( $A_0$  through  $A_{15}$ ).

Reading the device is accomplished by taking the chip enable(s) ( $\overline{CE}$  on the CY7C194,  $\overline{CE}_1$ ,  $\overline{CE}_2$  on the CY7C196) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins. A die coat is used to insure alpha immunity.



**Selection Guide**

|                                |            | 7C194-25<br>7C196-25 | 7C194-35<br>7C196-35 | 7C194-45<br>7C196-45 |
|--------------------------------|------------|----------------------|----------------------|----------------------|
| Maximum Access Time (ns)       |            | 25                   | 35                   | 45                   |
| Maximum Operating Current (mA) | Commercial | 80                   | 80                   | 70                   |
|                                | Military   |                      | 90                   | 90                   |
| Maximum Standby Current (mA)   | Commercial | 20                   | 20                   | 20                   |
|                                | Military   |                      | 20                   | 20                   |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature .....                           | -65°C to +150°C |
| Ambient Temperature with Power Applied .....        | -55°C to +125°C |
| Supply Voltage to Ground Potential ....             | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State ..... | -0.5V to +7.0V  |
| DC Input Voltage .....                              | -3.0V to +7.0V  |
| Output Current into Outputs (Low) .....             | 20 mA           |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | > 2001V<br>(Per MIL-STD-883 Method 3015) |
| Latch-up Current .....         | > 200 mA                                 |

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[4]</sup>

| Parameters       | Description   | Test Conditions  | 7C194-25<br>7C196-25 |                 | 7C194-35<br>7C196-35 |                 | 7C194-45<br>7C196-45 |                 | Units |
|------------------|---|--|----------------------|-----------------|----------------------|-----------------|----------------------|-----------------|-------|
|                  |   |  | Min.                 | Max.            | Min.                 | Max.            | Min.                 | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage   | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA  | 2.4                  |                 | 2.4                  |                 | 2.4                  |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage  | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA   |                      | 0.4             |                      | 0.4             |                      | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage  |  | 2.2                  | V <sub>CC</sub> | 2.2                  | V <sub>CC</sub> | 2.2                  | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage   |  | -3.0                 | 0.8             | -3.0                 | 0.8             | -3.0                 | 0.8             | V     |
| I <sub>Ix</sub>  | Input Load Current  | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -10                  | +10             | -10                  | +10             | -10                  | +10             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                                      | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled   | -10                  | +10             | -10                  | +10             | -10                  | +10             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>                 | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND   |                      | -350            |                      | -350            |                      | -350            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current                    | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA  | Commercial           | 80              |                      | 80              |                      | 70              | mA    |
|                  |   |  | Military             |                 |                      |                 |                      | 90              |       |
| I <sub>SB1</sub> | Automatic $\overline{CE}$ <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$<br>Min. Duty Cycle = 100%   | Commercial           | 20              |                      | 20              |                      | 20              | mA    |
|                  |   |  | Military             |                 |                      |                 |                      | 20              |       |
| I <sub>SB2</sub> | Automatic $\overline{CE}$ <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> ,<br>CE ≥ V <sub>CC</sub> - 0.3V<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V | Commercial           | 20              |                      | 20              |                      | 20              | mA    |
|                  |   |  | Military             |                 |                      |                 |                      | 20              |       |

### Capacitance<sup>[5]</sup>

| Parameters       | Description        | Test Conditions   | Max. | Units |
|------------------|--------------------|---|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |   | 7    |       |

#### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the  $\overline{CE}$  input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.

### AC Test Loads and Waveforms

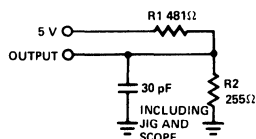


Figure 1a

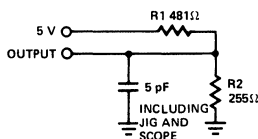


Figure 1b

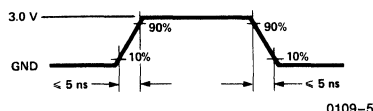
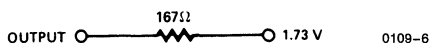


Figure 2

0109-4

0109-5

Equivalent to: THÉVENIN EQUIVALENT



0109-6

### Switching Characteristics Over Operating Range<sup>[4, 6]</sup>

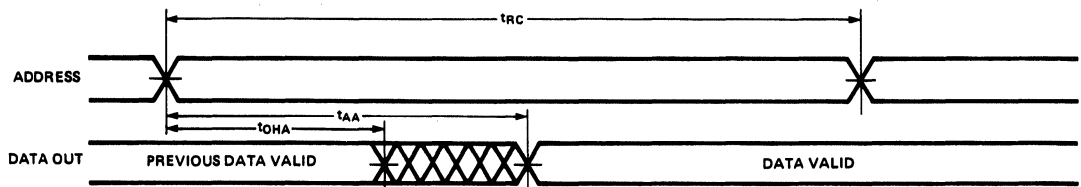
| Parameters                       | Description                                      | 7C194-25<br>7C196-25 |             | 7C194-35<br>7C196-35 |      | 7C194-45<br>7C196-45 |      | Units |    |
|----------------------------------|--|----------------------|-------------|----------------------|------|----------------------|------|-------|----|
|                                  |  | Min.                 | Max.        | Min.                 | Max. | Min.                 | Max. |       |    |
| <b>READ CYCLE</b>                |  |                      |             |                      |      |                      |      |       |    |
| $t_{RC}$                         | Read Cycle Time                                  | 25                   |             | 35                   |      | 45                   |      | ns    |    |
| $t_{AA}$                         | Address to Data Valid                            |                      | 25          |                      | 35   |                      | 45   | ns    |    |
| $t_{OHA}$                        | Output Hold from Address Change                  | 3                    |             | 3                    |      | 3                    |      | ns    |    |
| $t_{ACE_1, ACE_2}$               | $\overline{CE}$ LOW to Data Valid                |                      | 25          |                      | 35   |                      | 45   | ns    |    |
| $t_{DOE}$                        | $\overline{OE}$ LOW to Data Valid                |                      | 7C196<br>15 |                      | 25   |                      | 30   | ns    |    |
| $t_{LZOE}$                       | $\overline{OE}$ LOW to LOW Z                     |                      | 7C196<br>3  |                      | 3    |                      | 3    | ns    |    |
| $t_{HZOE}$                       | $\overline{OE}$ HIGH to HIGH Z                   |                      | 7C196<br>15 |                      | 15   |                      | 15   | ns    |    |
| $t_{LZCE_1, CE_2}$               | $\overline{CE}$ LOW to LOW Z <sup>[8]</sup>      |                      | 3           |                      | 3    |                      | 3    | ns    |    |
| $t_{HZCE_1, CE_2}$               | $\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup> |                      | 10          |                      | 15   |                      | 15   | ns    |    |
| $t_{PU}$                         | $\overline{CE}$ LOW to Power Up                  |                      | 0           |                      | 0    |                      | 0    | ns    |    |
| $t_{PD}$                         | $\overline{CE}$ HIGH to Power Down               |                      | 25          |                      | 35   |                      | 45   | ns    |    |
| <b>WRITE CYCLE<sup>[9]</sup></b> |  |                      |             |                      |      |                      |      |       |    |
| $t_{WC}$                         | Write Cycle Time                                 |                      | 20          |                      | 30   |                      | 40   | ns    |    |
| $t_{SCE}$                        | $\overline{CE}$ LOW to Write End                 |                      | 20          |                      | 30   |                      | 35   | ns    |    |
| $t_{AW}$                         | Address Set-up to Write End                      |                      | 20          |                      | 25   |                      | 35   | ns    |    |
| $t_{HA}$                         | Address Hold from Write End                      |                      | 2           |                      | 2    |                      | 2    | ns    |    |
| $t_{SA}$                         | Address Set-up to Write Start                    |                      | 0           |                      | 0    |                      | 0    | ns    |    |
| $t_{PWE}$                        | $\overline{WE}$ Pulse Width                      |                      | 20          |                      | 25   |                      | 35   | ns    |    |
| $t_{SD}$                         | Data Set-up to Write End                         |                      | 10          |                      | 15   |                      | 20   | ns    |    |
| $t_{HD}$                         | Data Hold from Write End                         |                      | 0           |                      | 0    |                      | 0    | ns    |    |
| $t_{LZWE}$                       | $\overline{WE}$ HIGH to LOW Z <sup>[8]</sup>     |                      | 3           |                      | 3    |                      | 3    | ns    |    |
| $t_{HZWE}$                       | $\overline{WE}$ LOW to HIGH Z <sup>[7, 8]</sup>  |                      | 0           | 10                   | 0    | 10                   | 0    | 15    | ns |

**Notes:**

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
- $t_{HZCE}$  and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in Figure 1b. Transition is measured  $\pm 500$  mV from steady state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $\overline{CE}_2$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CE}_1 = V_{IL}/\overline{CE}_2 = V_{IL}$ . (7C196:  $\overline{OE} = V_{IL}$ ,  $\overline{CE}_2 = V_{IL}$  also.)
- Address valid prior to or coincident with  $\overline{CE}_1$  and  $\overline{CE}_2$  transition LOW.
- 7C196 only: Data I/O will be high impedance if  $\overline{OE} = V_{IH}$ .

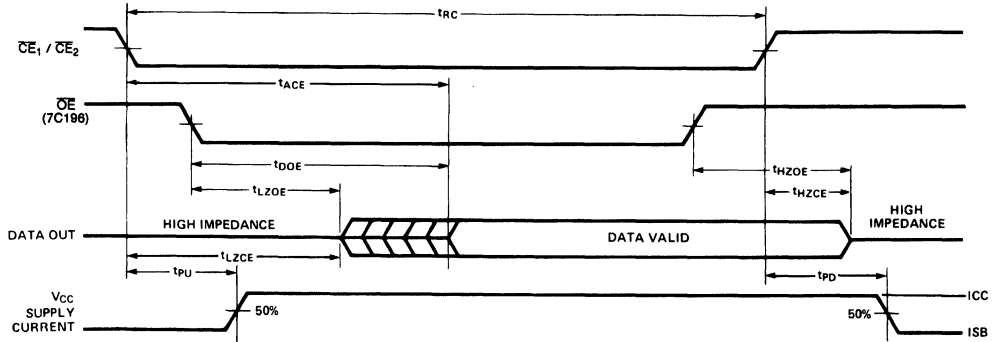
### Switching Waveforms

#### Read Cycle No. 1 (Notes 10, 11)



**Switching Waveforms (Continued)**

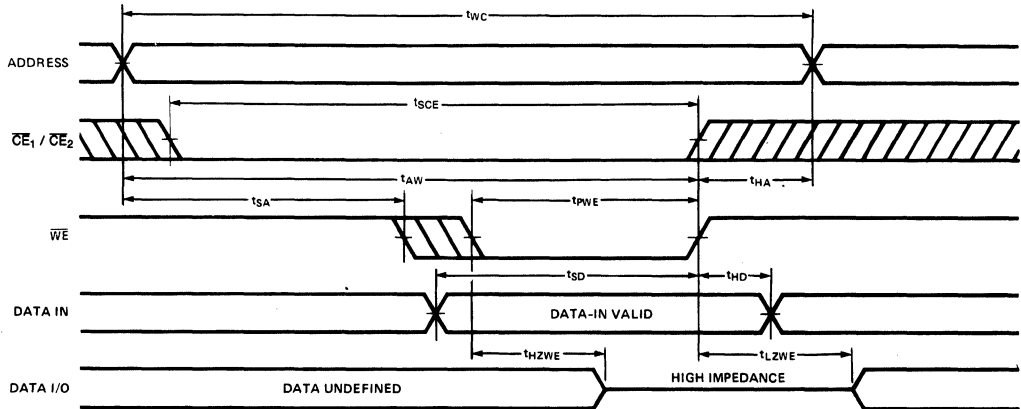
**Read Cycle No. 2 (Notes 10, 12)**



2

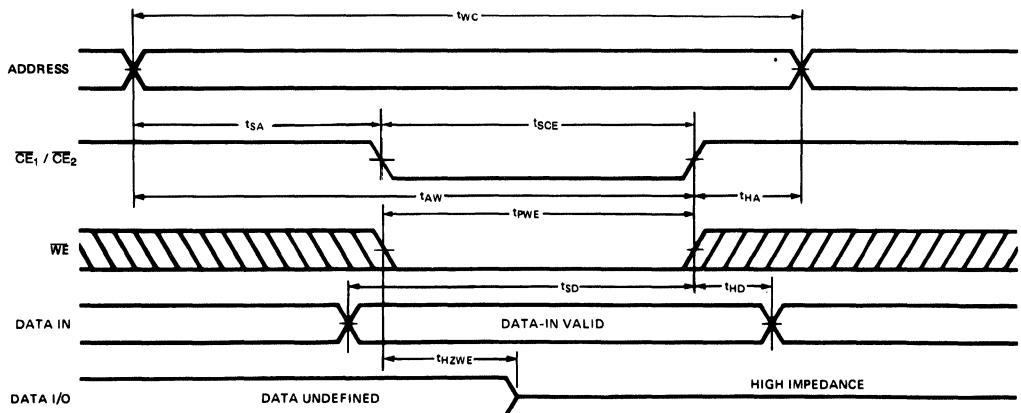
0109-8

**Write Cycle No. 1 (WE Controlled) (Notes 9, 13)**



0109-9

**Write Cycle No. 2 (CE Controlled) (Notes 9, 13)**



Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

0109-10



**7C194 Truth Table**

| CE | WE | Input/Outputs | Mode                |
|----|----|---------------|---------------------|
| H  | X  | High Z        | Deselect/Power Down |
| L  | H  | Data Out      | Read                |
| L  | L  | Data In       | Write               |

**7C196 Truth Table**

| CE <sub>1</sub> | CE <sub>2</sub> | WE | OE | Inputs/Outputs | Mode                |
|-----------------|-----------------|----|----|----------------|---------------------|
| H               | X               | X  | X  | High Z         | Deselect/Power Down |
| X               | H               | X  | X  |                |                     |
| L               | L               | H  | L  | Data Out       | Read                |
| L               | L               | L  | X  | Data In        | Write               |
| L               | L               | H  | H  | High Z         | Deselect            |

**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C194-25PC  | P13          | Commercial      |
|            | CY7C194-25VC  | V13          |                 |
|            | CY7C194-25DC  | D14          |                 |
|            | CY7C194-25LC  | L54          |                 |
| 35         | CY7C194-35PC  | P13          | Commercial      |
|            | CY7C194-35VC  | V13          |                 |
|            | CY7C194-35DC  | D14          |                 |
|            | CY7C194-35LC  | L54          |                 |
|            | CY7C194-35DMB | D14          | Military        |
|            | CY7C194-35LMB | L54          |                 |
| 45         | CY7C194-45PC  | P13          | Commercial      |
|            | CY7C194-45VC  | V13          |                 |
|            | CY7C194-45DC  | D14          |                 |
|            | CY7C194-45LC  | L54          |                 |
|            | CY7C194-45DMB | D14          | Military        |
|            | CY7C194-45LMB | L54          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C196-25PC  | P21          | Commercial      |
|            | CY7C196-25VC  | V21          |                 |
|            | CY7C196-25DC  | D22          |                 |
|            | CY7C196-25LC  | L54          |                 |
| 35         | CY7C196-35PC  | P21          | Commercial      |
|            | CY7C196-35VC  | V21          |                 |
|            | CY7C196-35DC  | D22          |                 |
|            | CY7C196-35LC  | L54          |                 |
|            | CY7C196-35DMB | D22          | Military        |
|            | CY7C196-35LMB | L54          |                 |
| 45         | CY7C196-45PC  | P21          | Commercial      |
|            | CY7C196-45VC  | V21          |                 |
|            | CY7C196-45DC  | D22          |                 |
|            | CY7C196-45LC  | L54          |                 |
|            | CY7C196-45DMB | D22          | Military        |
|            | CY7C196-45LMB | L54          |                 |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL</sub> Max. | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>OS</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB1</sub>     | 1,2,3     |
| I <sub>SB2</sub>     | 1,2,3     |

**2**
**Switching Characteristics**

| Parameters                      | Subgroups   |
|---------------------------------|-------------|
| <b>READ CYCLE</b>               |             |
| t <sub>RC</sub>                 | 7,8,9,10,11 |
| t <sub>AA</sub>                 | 7,8,9,10,11 |
| t <sub>OHA</sub>                | 7,8,9,10,11 |
| t <sub>ACE1, ACE2</sub>         | 7,8,9,10,11 |
| t <sub>DOE</sub> <sup>[1]</sup> | 7,8,9,10,11 |
| <b>WRITE CYCLE</b>              |             |
| t <sub>WC</sub>                 | 7,8,9,10,11 |
| t <sub>SCE</sub>                | 7,8,9,10,11 |
| t <sub>AW</sub>                 | 7,8,9,10,11 |
| t <sub>HA</sub>                 | 7,8,9,10,11 |
| t <sub>SA</sub>                 | 7,8,9,10,11 |
| t <sub>PWE</sub>                | 7,8,9,10,11 |
| t <sub>SD</sub>                 | 7,8,9,10,11 |
| t <sub>HD</sub>                 | 7,8,9,10,11 |
| t <sub>AWE</sub>                | 7,8,9,10,11 |
| t <sub>ADV</sub>                | 7,8,9,10,11 |

**Note:**

1. 7C196 only.

Document #: 38-00081



### Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed—25 ns
- Low active power—330 mW
- Low standby power—110 mW
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

### Functional Description

The CY7C197 is a high performance CMOS static RAM organized as 262,144 words x 1 bit. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and three-state drivers. The CY7C197 has an automatic power-down feature, reducing the power consumption by 67% when deselected.

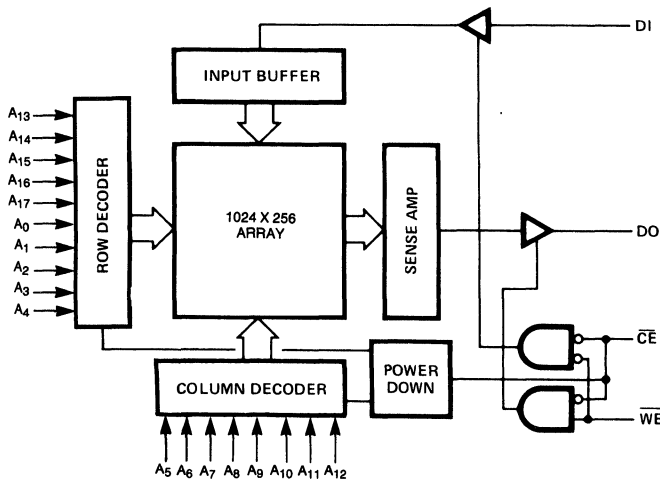
Writing to the device is accomplished when the chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the input pin ( $D_{IN}$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{17}$ ).

Reading the device is accomplished by taking the chip enable ( $\overline{CE}$ ) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output ( $D_{OUT}$ ) pin.

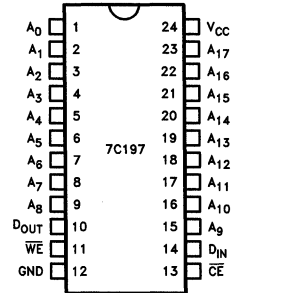
The output pin stays in high impedance state when chip enable ( $\overline{CE}$ ) is HIGH or write enable ( $\overline{WE}$ ) is LOW.

The 7C197 utilizes a Die Coat to ensure alpha immunity.

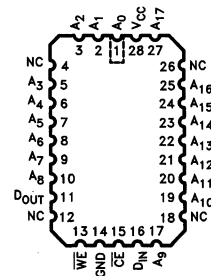
### Logic Block Diagram



### Pin Configurations



0110-2



0110-11

### Selection Guide

|                                |            | 7C197-25 | 7C197-35 | 7C197-45 |
|--------------------------------|------------|----------|----------|----------|
| Maximum Access Time (ns)       | Commercial | 25       | 35       | 45       |
|                                | Military   |          | 35       | 45       |
| Maximum Operating Current (mA) | Commercial | 70       | 70       | 60       |
|                                | Military   |          | 80       | 80       |
| Maximum Standby Current (mA)   | Commercial | 20/20    | 20/20    | 20/20    |
|                                | Military   |          | 20/20    | 20/20    |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature .....                                   | -65°C to +150°C |
| Ambient Temperature with Power Applied .....                | -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State .....         | -0.5V to +7.0V  |
| DC Input Voltage .....                                      | -3.0V to +7.0V  |
| Output Current into Outputs (Low) .....                     | 20 mA           |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | > 2001V<br>(Per MIL-STD-883 Method 3015) |
| Latch-up Current .....         | > 200 mA                                 |

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[4]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[5]</sup>

| Parameters       | Description   | Test Conditions  | 7C197-25   |                 | 7C197-35 |                 | 7C197-45 |                 | Units |
|------------------|---|--|------------|-----------------|----------|-----------------|----------|-----------------|-------|
|                  |   |  | Min.       | Max.            | Min.     | Max.            | Min.     | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage   | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA  | 2.4        |                 | 2.4      |                 | 2.4      |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage  | V <sub>CC</sub> = Min.,<br>I <sub>OL</sub> = 8.0 mA Military<br>I <sub>OL</sub> = 12.0 mA Commercial                         |            | 0.4             |          | 0.4             |          | 0.4             | V     |
|                  |   |  |            |                 |          |                 |          |                 |       |
| V <sub>IH</sub>  | Input HIGH Voltage  |  | 2.2        | V <sub>CC</sub> | 2.2      | V <sub>CC</sub> | 2.2      | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage   |  | -3.0       | 0.8             | -3.0     | 0.8             | -3.0     | 0.8             | V     |
| I <sub>Ix</sub>  | Input Load Current  | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -10        | +10             | -10      | +10             | -10      | +10             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                                      | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled   | -50        | +50             | -50      | +50             | -50      | +50             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>                 | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND   |            | -350            |          | -350            |          | -350            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current                    | V <sub>CC</sub> = Max.,<br>I <sub>OUT</sub> = 0 mA   | Commercial | 70              |          | 70              |          | 60              | mA    |
|                  |   |  | Military   |                 |          | 80              |          | 80              |       |
| I <sub>SB1</sub> | Automatic $\overline{CE}$ <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> ,<br>CE ≥ V <sub>IH</sub>   | Commercial | 20              |          | 20              |          | 20              | mA    |
|                  |   |  | Military   |                 |          | 20              |          | 20              |       |
| I <sub>SB2</sub> | Automatic $\overline{CE}$ <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V | Commercial | 20              |          | 20              |          | 20              | mA    |
|                  |   |  | Military   |                 |          | 20              |          | 20              |       |

### Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 7    |       |

#### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the CE input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

### AC Test Loads and Waveforms

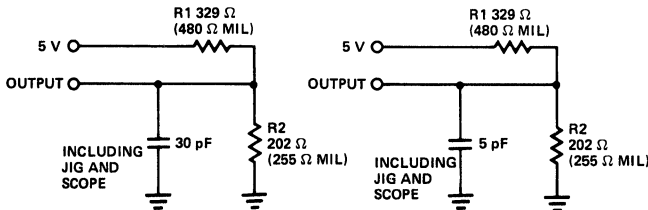


Figure 1a

Figure 1b

0110-3

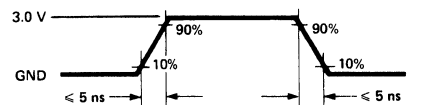
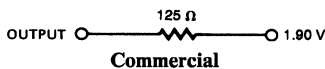


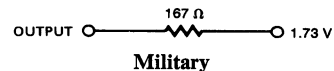
Figure 2

0110-4

Equivalent to: THÉVENIN EQUIVALENT



0110-5



0110-6

### Switching Characteristics Over Operating Range<sup>[5, 6]</sup>

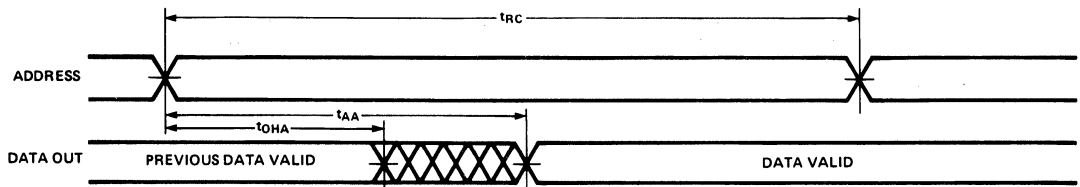
| Parameters                       | Description                                      | 7C197-25 |      | 7C197-35 |      | 7C197-45 |      | Units |
|----------------------------------|--|----------|------|----------|------|----------|------|-------|
|                                  |  | Min.     | Max. | Min.     | Max. | Min.     | Max. |       |
| <b>READ CYCLE</b>                |  |          |      |          |      |          |      |       |
| t <sub>RC</sub>                  | Read Cycle Time                                  | 25       |      | 35       |      | 45       |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid                            |          | 25   |          | 35   |          | 45   | ns    |
| t <sub>OHA</sub>                 | Output Hold from Address Change                  | 3        |      | 3        |      | 3        |      | ns    |
| t <sub>ACE</sub>                 | $\overline{CE}$ LOW to Data Valid                |          | 25   |          | 35   |          | 45   | ns    |
| t <sub>LZCE</sub>                | $\overline{CE}$ LOW to Low Z <sup>[8]</sup>      | 3        |      | 3        |      | 3        |      | ns    |
| t <sub>HZCE</sub>                | $\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup> | 0        | 15   | 0        | 20   | 0        | 20   | ns    |
| t <sub>PU</sub>                  | $\overline{CE}$ LOW to Power Up                  | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>PD</sub>                  | $\overline{CE}$ HIGH to Power Down               |          | 20   |          | 25   |          | 30   | ns    |
| <b>WRITE CYCLE<sup>[9]</sup></b> |  |          |      |          |      |          |      |       |
| t <sub>WC</sub>                  | Write Cycle Time                                 | 25       |      | 35       |      | 45       |      | ns    |
| t <sub>SCE</sub>                 | $\overline{CE}$ LOW to Write End                 | 20       |      | 30       |      | 40       |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End                      | 20       |      | 30       |      | 40       |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End                      | 2        |      | 2        |      | 2        |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                    | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>PWE</sub>                 | $\overline{WE}$ Pulse Width                      | 20       |      | 25       |      | 25       |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End                         | 15       |      | 20       |      | 25       |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End                         | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>LZWE</sub>                | $\overline{WE}$ HIGH to Low Z <sup>[8]</sup>     | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>HZWE</sub>                | $\overline{WE}$ LOW to High Z <sup>[7, 8]</sup>  | 0        | 15   | 0        | 20   | 0        | 20   | ns    |

**Notes:**

6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
7. t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
8. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> for any given device.
9. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
10.  $\overline{WE}$  is HIGH for read cycle.
11. Device is continuously selected,  $\overline{CE} = V_{IL}$ .
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

### Switching Waveforms

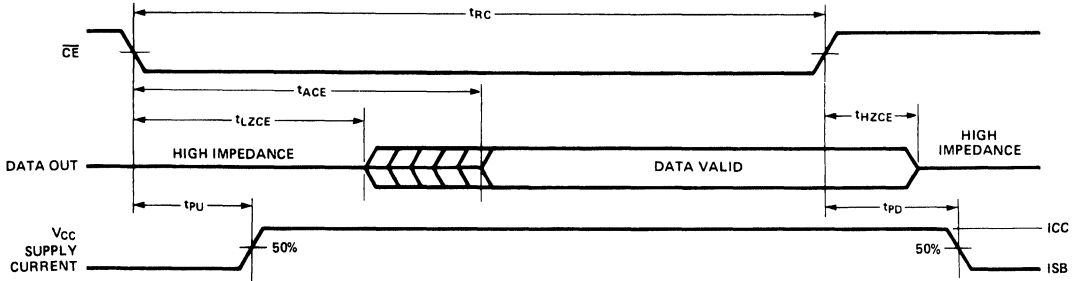
#### Read Cycle No. 1<sup>[10, 11]</sup>



0110-7

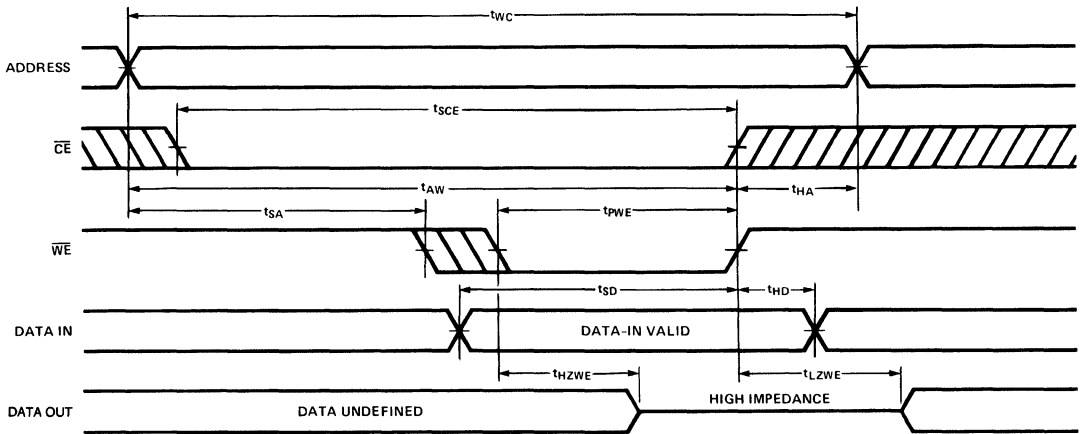
Switching Waveforms (Continued)

Read Cycle No. 2<sup>[11]</sup>



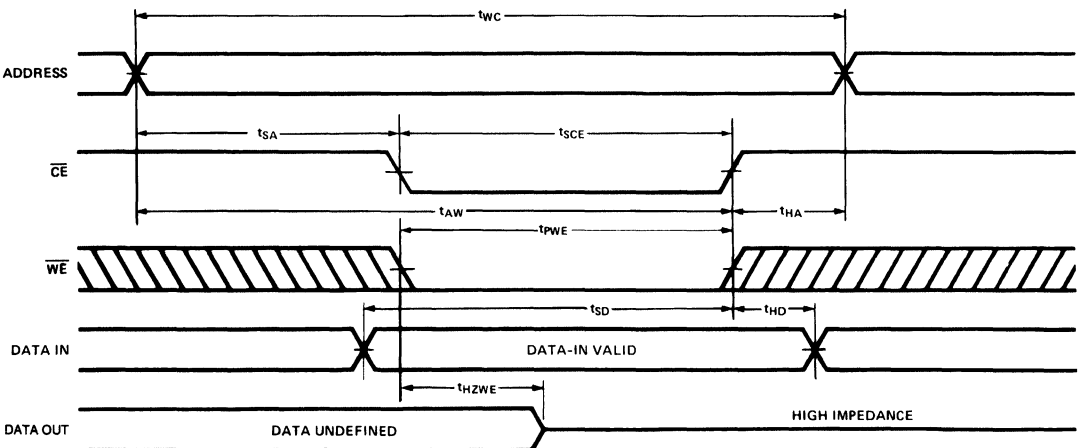
0110-8

Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[10]</sup>



0110-9

Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>[10]</sup>



0110-10

Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

**Truth Table**

| CE | WE | Input/Outputs | Mode                |
|----|----|---------------|---------------------|
| H  | X  | High Z        | Deselect/Power Down |
| L  | H  | Data Out      | Read                |
| L  | L  | Data In       | Write               |

**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 25         | CY7C197-25PC  | P13          | Commercial      |
|            | CY7C197-25VC  | V13          |                 |
|            | CY7C197-25DC  | D14          |                 |
|            | CY7C197-25LC  | L54          |                 |
| 35         | CY7C197-35PC  | P13          | Commercial      |
|            | CY7C197-35VC  | V13          |                 |
|            | CY7C197-35DC  | D14          |                 |
|            | CY7C197-35LC  | L54          |                 |
|            | CY7C197-35DMB | D14          | Military        |
|            | CY7C197-35LMB | L54          |                 |
| 45         | CY7C197-45PC  | P13          | Commercial      |
|            | CY7C197-45VC  | V13          |                 |
|            | CY7C197-45DC  | D14          |                 |
|            | CY7C197-45LC  | L54          |                 |
|            | CY7C197-45DMB | D14          | Military        |
|            | CY7C197-45LMB | L54          |                 |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters | Subgroups |
|------------|-----------|
| VOH        | 1,2,3     |
| VOL        | 1,2,3     |
| VIH        | 1,2,3     |
| VIL Max.   | 1,2,3     |
| IIX        | 1,2,3     |
| IOZ        | 1,2,3     |
| Ios        | 1,2,3     |
| ICC        | 1,2,3     |
| ISB1       | 1,2,3     |
| ISB2       | 1,2,3     |

**2**
**Switching Characteristics**

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| tRC                | 7,8,9,10,11 |
| tAA                | 7,8,9,10,11 |
| tOHA               | 7,8,9,10,11 |
| tACE               | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| tWC                | 7,8,9,10,11 |
| tSCE               | 7,8,9,10,11 |
| tAW                | 7,8,9,10,11 |
| tHA                | 7,8,9,10,11 |
| tSA                | 7,8,9,10,11 |
| tPWE               | 7,8,9,10,11 |
| tSD                | 7,8,9,10,11 |
| tHD                | 7,8,9,10,11 |

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**Features**

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed—35 ns
- Low active power—550 mW
- Low standby power—110 mW
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

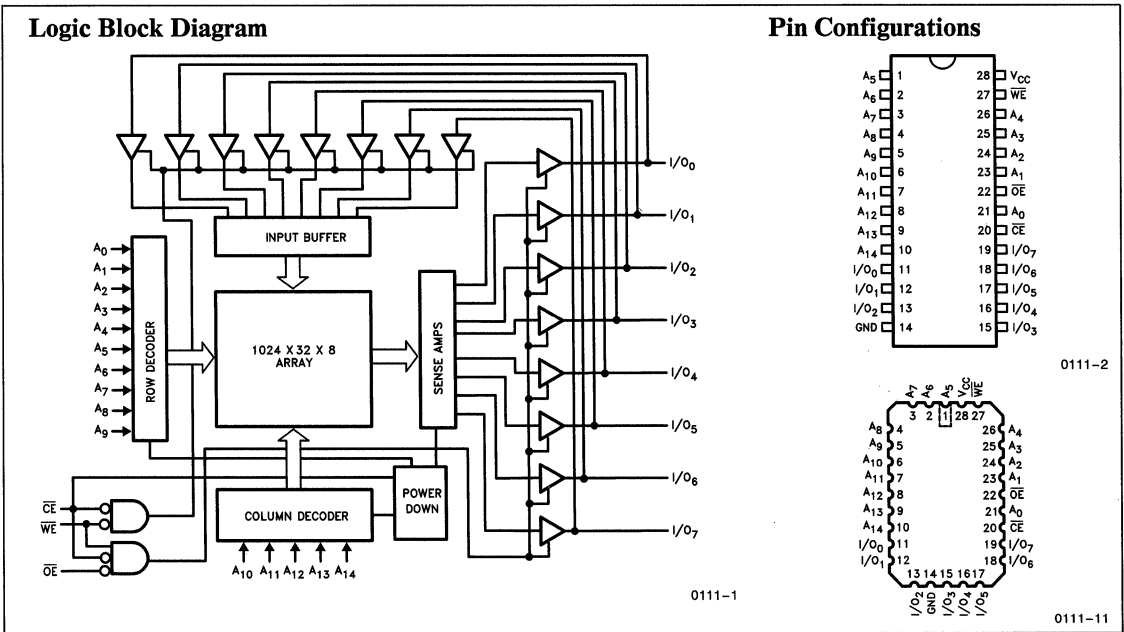
**Functional Description**

The CY7C198 and CY7C199 are high performance CMOS static RAMs organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (CE) and active LOW output enable (OE) and three-state drivers. Both devices have an automatic power-down feature, reducing the power consumption by 80% when deselected. The CY7C199 is in the space saving 300 mil wide DIP package and leadless chip carrier. The CY7C198 is in the standard 600 mil wide package.

An active LOW write enable signal (WE) controls the writing/reading operation of the memory. When CE and WE inputs are both LOW, data on

the eight data input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the memory location addressed by the address present on the address pins (A<sub>0</sub> through A<sub>14</sub>). Reading the device is accomplished by selecting the device and enabling the outputs, CE and OE active LOW, while (WE) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable (WE) is HIGH. A die coat is used to ensure alpha immunity.



**Selection Guide**

|                                |            | <b>7C198-35</b><br><b>7C199-35</b> | <b>7C198-45</b><br><b>7C199-45</b> | <b>7C198-55</b><br><b>7C199-55</b> |
|--------------------------------|------------|------------------------------------|------------------------------------|------------------------------------|
| Maximum Access Time (ns)       |            | 35                                 | 45                                 | 55                                 |
| Maximum Operating Current (mA) | Commercial | 110                                | 110                                | 100                                |
|                                | Military   |                                    | 120                                | 120                                |
| Maximum Standby Current (mA)   | Commercial | 20/20                              | 20/20                              | 20/20                              |
|                                | Military   |                                    | 20/20                              | 20/20                              |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|  |                 |                                |  |
|--|-----------------|--------------------------------|--|
| Storage Temperature .....                                      | -65°C to +150°C | Static Discharge Voltage ..... | > 2001V<br>(Per MIL-STD-883 Method 3015) |
| Ambient Temperature with<br>Power Applied .....                | -55°C to +125°C | Latch-up Current .....         | > 200 mA                                 |
| Supply Voltage to Ground Potential<br>(Pin 28 to Pin 14) ..... | -0.5V to +7.0V  |                                |  |
| DC Voltage Applied to Outputs<br>in High Z State .....         | -0.5V to +7.0V  |                                |  |
| DC Input Voltage .....   | -3.0V to +7.0V  |                                |  |
| Output Current into Outputs (Low) .....                        | 20 mA           |                                |  |

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[4]</sup>

| Parameters       | Description                                  | Test Conditions   | 7C198-35<br>7C199-35 |                 | 7C198-45<br>7C199-45 |                 | 7C198-55<br>7C199-55 |                 | Units |
|------------------|--|---|----------------------|-----------------|----------------------|-----------------|----------------------|-----------------|-------|
|                  |  |   | Min.                 | Max.            | Min.                 | Max.            | Min.                 | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA   | 2.4                  |                 | 2.4                  |                 | 2.4                  |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA  |                      | 0.4             |                      | 0.4             |                      | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                           |   | 2.2                  | V <sub>CC</sub> | 2.2                  | V <sub>CC</sub> | 2.2                  | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage                            |   | -3.0                 | 0.8             | -3.0                 | 0.8             | -3.0                 | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current                           | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>  | -10                  | 10              | -10                  | 10              | -10                  | +10             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                       | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub><br>Output Disabled   | -10                  | +10             | -10                  | +10             | -10                  | +10             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>  | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND  |                      | -300            |                      | -300            |                      | -300            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current     | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA   | Commercial           | 110             |                      | 110             |                      | 100             | mA    |
|                  |  |   | Military             |                 |                      |                 | 120                  | 120             |       |
| I <sub>SB1</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> ,<br>$\overline{CE} \geq V_{IH}$ ,<br>Min. Duty Cycle = 100%   | Commercial           | 20              |                      | 20              |                      | 20              | mA    |
|                  |  |   | Military             |                 |                      |                 | 20                   | 20              |       |
| I <sub>SB2</sub> | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> ,<br>$\overline{CE} \geq V_{CC} - 0.3V$ ,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V | Commercial           | 20              |                      | 20              |                      | 20              | mA    |
|                  |  |   | Military             |                 |                      |                 | 20                   | 20              |       |

### Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 7    |       |

Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

### AC Test Loads and Waveforms

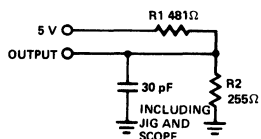


Figure 1a

0111-3

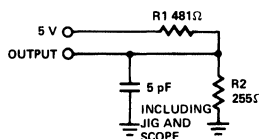


Figure 1b

0111-4

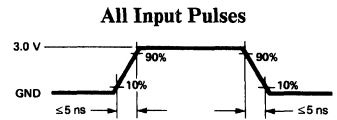
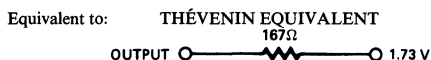


Figure 2

0111-5



0111-6

### Switching Characteristics Over Operating Range<sup>[4, 5]</sup>

| Parameters                       | Description                                      | 7C198-35<br>7C199-35 |      | 7C198-45<br>7C199-45 |      | 7C198-55<br>7C199-55 |      | Units |
|----------------------------------|--|----------------------|------|----------------------|------|----------------------|------|-------|
|                                  |  | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. |       |
| <b>READ CYCLE</b>                |  |                      |      |                      |      |                      |      |       |
| t <sub>RC</sub>                  | Read Cycle Time                                  | 35                   |      | 45                   |      | 55                   |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid                            |                      | 35   |                      | 45   |                      | 55   | ns    |
| t <sub>OHA</sub>                 | Data Hold from Address Change                    | 3                    |      | 3                    |      | 3                    |      | ns    |
| t <sub>ACE</sub>                 | $\overline{CE}$ LOW to Data Valid                |                      | 35   |                      | 45   |                      | 55   | ns    |
| t <sub>DOE</sub>                 | $\overline{OE}$ LOW to Data Valid                |                      | 20   |                      | 20   |                      | 25   | ns    |
| t <sub>LZOE</sub>                | $\overline{OE}$ LOW to Low Z                     | 3                    |      | 3                    |      | 3                    |      | ns    |
| t <sub>HZOE</sub>                | $\overline{OE}$ HIGH to High Z <sup>[6]</sup>    |                      | 20   |                      | 25   |                      | 30   | ns    |
| t <sub>LZCE</sub>                | $\overline{CE}$ LOW to Low Z <sup>[7]</sup>      | 3                    |      | 3                    |      | 3                    |      | ns    |
| t <sub>HZCE</sub>                | $\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup> |                      | 15   |                      | 20   |                      | 20   | ns    |
| t <sub>PU</sub>                  | $\overline{CE}$ LOW to Power Up                  | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>PD</sub>                  | $\overline{CE}$ HIGH to Power Down               |                      | 20   |                      | 25   |                      | 25   | ns    |
| <b>WRITE CYCLE<sup>[8]</sup></b> |  |                      |      |                      |      |                      |      |       |
| t <sub>WC</sub>                  | Write Cycle Time                                 | 35                   |      | 45                   |      | 50                   |      | ns    |
| t <sub>SCE</sub>                 | $\overline{CE}$ LOW to Write End                 | 30                   |      | 40                   |      | 50                   |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End                      | 30                   |      | 40                   |      | 50                   |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End                      | 2                    |      | 2                    |      | 2                    |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                    | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>PWE</sub>                 | WE Pulse Width                                   | 20                   |      | 25                   |      | 30                   |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End                         | 15                   |      | 20                   |      | 25                   |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End                         | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>HZWE</sub>                | $\overline{WE}$ LOW to High Z <sup>[6]</sup>     |                      | 15   |                      | 20   |                      | 25   | ns    |
| t <sub>LZWE</sub>                | $\overline{WE}$ HIGH to Low Z                    | 3                    |      | 3                    |      | 3                    |      | ns    |

**Notes:**

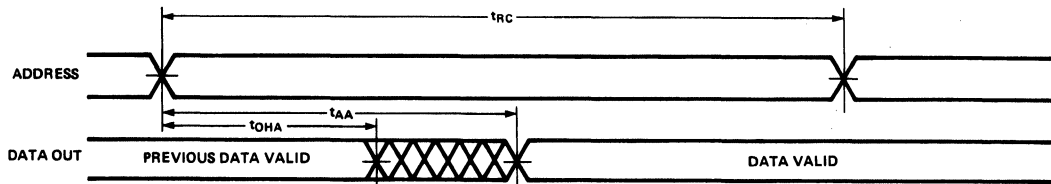
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a

write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  = V<sub>IL</sub>.
- Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
- Data I/O is high impedance if  $\overline{OE}$  = V<sub>IH</sub>.

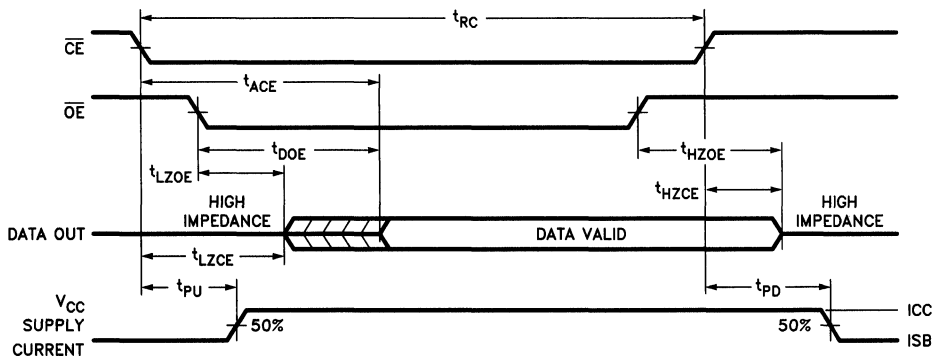
### Switching Waveforms

#### Read Cycle No. 1 (Notes 10, 11)



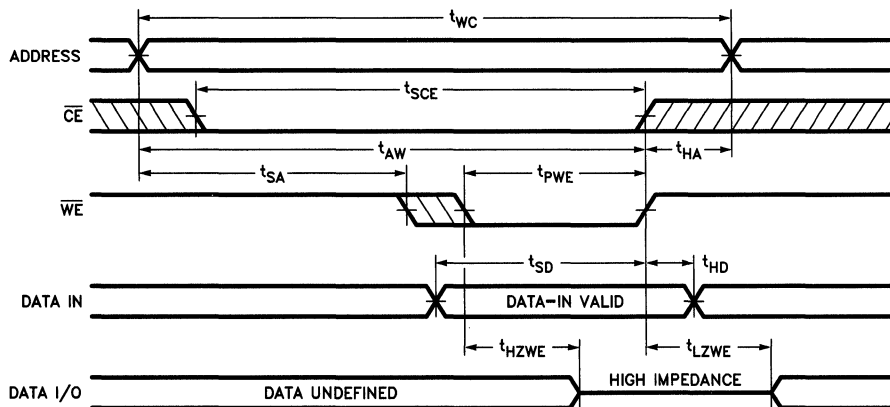
### Switching Waveforms (Continued)

#### Read Cycle No. 2 (Notes 9, 11)



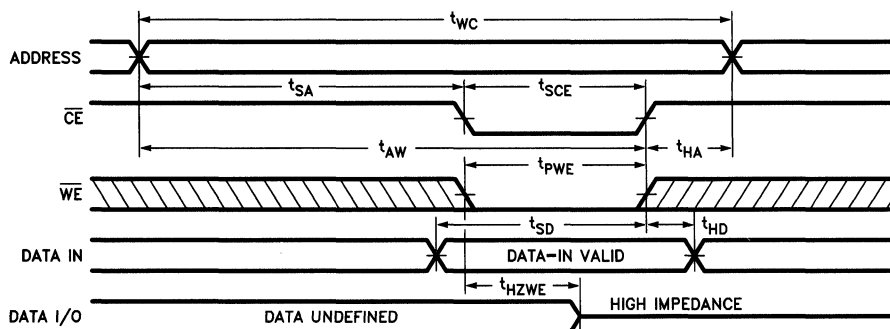
0111-8

#### Write Cycle No. 1 ( $\overline{WE}$ Controlled) (Notes 8, 12)



0111-9

#### Write Cycle No. 2 ( $\overline{CE}$ Controlled) (Notes 8, 12)



0111-10

Note: If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

**Truth Table**

| CE | WE | OE | Input/Outputs | Mode                |
|----|----|----|---------------|---------------------|
| H  | X  | X  | High Z        | Deselect Power Down |
| L  | H  | L  | Data Out      | Read                |
| L  | L  | X  | Data In       | Write               |
| L  | H  | H  | High Z        | Deselect            |

**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 35         | CY7C198-35PC  | P15          | Commercial      |
|            | CY7C198-35DC  | D16          |                 |
| 45         | CY7C198-45PC  | P15          | Commercial      |
|            | CY7C198-45DC  | D16          |                 |
|            | CY7C198-45DMB | D16          | Military        |
| 55         | CY7C198-55PC  | P15          | Commercial      |
|            | CY7C198-55DC  | D16          |                 |
|            | CY7C198-55DMB | D16          | Military        |

| Speed (ns)    | Ordering Code | Package Type | Operating Range |          |
|---------------|---------------|--------------|-----------------|----------|
| 35            | CY7C199-35PC  | P21          | Commercial      |          |
|               | CY7C199-35VC  | V21          |                 |          |
|               | CY7C199-35DC  | D22          |                 |          |
| 45            | CY7C199-35LC  | L54          | Commercial      |          |
|               | CY7C199-45PC  | P21          |                 |          |
|               | CY7C199-45VC  | V21          |                 |          |
|               | CY7C199-45DC  | D22          |                 |          |
|               | CY7C199-45LC  | L54          |                 |          |
|               | CY7C199-45DMB | D22          |                 | Military |
| CY7C199-45LMB | L54           |              |                 |          |
| 55            | CY7C199-55PC  | P21          | Commercial      |          |
|               | CY7C199-55VC  | V21          |                 |          |
|               | CY7C199-55DC  | D22          |                 |          |
|               | CY7C199-55LC  | L54          |                 |          |
|               | CY7C199-55DMB | D22          |                 | Military |
|               | CY7C199-55LMB | L54          |                 |          |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>OS</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB1</sub>     | 1,2,3     |
| I <sub>SB2</sub>     | 1,2,3     |

2

#### Switching Characteristics

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>OHA</sub>   | 7,8,9,10,11 |
| t <sub>ACE</sub>   | 7,8,9,10,11 |
| t <sub>DOE</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>SCE</sub>   | 7,8,9,10,11 |
| t <sub>AW</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |

Document #: 38-00077-A



### Features

- Fully decoded, 16 word x 4-bit high speed CMOS RAMs
- Inverting outputs 27S03, 27LS03, 74S189
- Non-inverting outputs 27S07
- High speed  
— 25 ns
- Low power  
— 210 mW (27LS03)
- Power supply 5V ±10%
- Advanced high speed CMOS processing for optimum speed/power product
- Capable of withstanding greater than 2001V static discharge
- Three-state outputs
- TTL compatible interface levels

### Functional Description

These devices are high performance 64-bit static RAMs organized as 16 words x 4-bits. Easy memory expansion is provided by an active LOW chip select (CS) input and three-state outputs. The devices are provided with inverting and non-inverting outputs.

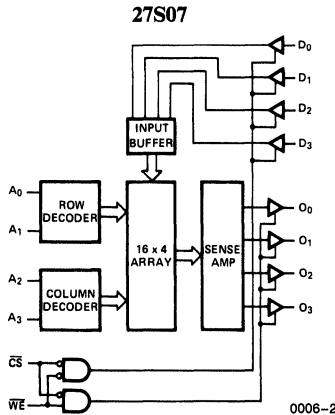
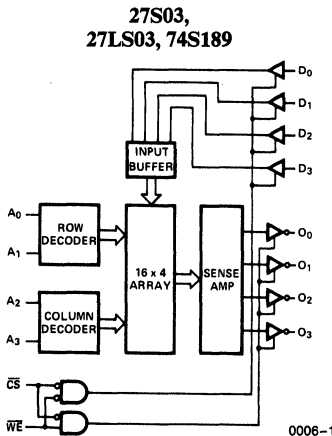
An active LOW write enable (WE) signal controls the writing and reading of the memory. When the write enable (WE) and chip select (CS) are both LOW the information on the four data inputs (D<sub>0</sub>–D<sub>3</sub>) is written into the location addressed by the information on the address lines (A<sub>0</sub>–A<sub>3</sub>). The outputs are preconditioned such that the correct data is present at the data outputs (O<sub>0</sub>–O<sub>3</sub>) when the write cycle is complete. This preconditioning operation

insures minimum write recovery times by eliminating the “write recovery glitch”.

Reading is accomplished with an active LOW on the chip select line (CS) and a HIGH on the write enable (WE) line. The information stored is read out from the addressed location and presented at the outputs in inverted or non-inverted format.

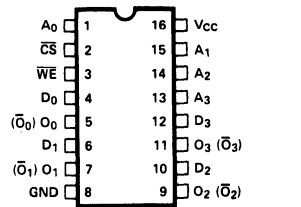
During the write operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

### Logic Block Diagrams

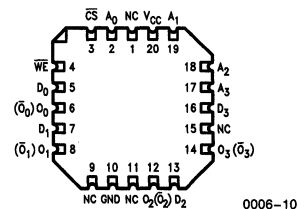


### Pin Configurations

27S07  
(27S03, 27LS03, 74S189)



DIP  
Top View



LCC  
Top View

### Selection Guide (For higher performance and lower power refer to CY7C189/90 data sheet.)

|                                |            | 27S03A<br>27S07A | 27S03, 27S07<br>74S189 | 27LS03 |
|--------------------------------|------------|------------------|------------------------|--------|
| Maximum Access Time (ns)       | Commercial | 25               | 35                     |        |
|                                | Military   | 25               | 35                     | 65     |
| Maximum Operating Current (mA) | Commercial | 90               | 90                     |        |
|                                | Military   | 100              | 100                    | 38     |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature . . . . .  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$   
 Ambient Temperature with  
 Power applied . . . . .  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
 Supply Voltage to Ground Potential  
 (Pin 16 to 8) . . . . .  $-0.5\text{V}$  to  $+7.0\text{V}$   
 DC Voltage Applied to Outputs  
 in High Z State . . . . .  $-0.5\text{V}$  to  $+7.0\text{V}$   
 DC Input Voltage . . . . .  $-3.0\text{V}$  to  $+7.0\text{V}$   
 Output Current, into Outputs (Low) . . . . . 20 mA

Static Discharge Voltage . . . . .  $> 2001\text{ V}$   
 (per MIL-STD-883 Method 3015)  
 Latchup Current . . . . .  $> 200\text{ mA}$

### Operating Range

| Range                   | Ambient Temperature                             | V <sub>CC</sub>      |
|-------------------------|---|----------------------|
| Commercial              | $0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$    | $5\text{V} \pm 10\%$ |
| Military <sup>[3]</sup> | $-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ | $5\text{V} \pm 10\%$ |

### Electrical Characteristics Over the Operating Range<sup>[6]</sup>

| Parameters      | Description                                 | Test Conditions  | 74S189,<br>27S03, 27S07 |                 | 27LS03 |                 | Units         |
|-----------------|---|--|-------------------------|-----------------|--------|-----------------|---------------|
|                 |   |  | Min.                    | Max.            | Min.   | Max.            |               |
| V <sub>OH</sub> | Output HIGH Voltage                         | V <sub>CC</sub> = Min., I <sub>OH</sub> = $-5.2\text{ mA}$ | 2.4                     |                 | 2.4    |                 | V             |
| V <sub>OL</sub> | Output LOW Voltage                          | V <sub>CC</sub> = Min., I <sub>OL</sub> = $16.0\text{ mA}$ |                         | 0.45            |        |                 | V             |
|                 |   | V <sub>CC</sub> = Min., I <sub>OL</sub> = $8.0\text{ mA}$  |                         |                 |        | 0.45            | V             |
| V <sub>IH</sub> | Input HIGH Voltage                          |  | 2.0                     | V <sub>CC</sub> | 2.0    | V <sub>CC</sub> | V             |
| V <sub>IL</sub> | Input LOW Voltage                           |  | $-3.0$                  | 0.8             | $-3.0$ | 0.8             | V             |
| I <sub>IX</sub> | Input Leakage Current                       | $\text{GND} \leq V_I \leq V_{CC}$                          | $-10$                   | $+10$           | $-10$  | $+10$           | $\mu\text{A}$ |
| V <sub>CD</sub> | Input Diode Clamp Voltage <sup>[1]</sup>    |  |                         |                 |        |                 |               |
| I <sub>OZ</sub> | Output Leakage Current                      | $\text{GND} \leq V_O \leq V_{CC}$                          | $-40$                   | $+40$           | $-40$  | $+40$           | $\mu\text{A}$ |
| I <sub>OS</sub> | Output Short Circuit Current <sup>[2]</sup> | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND             |                         | $-90$           |        | $-90$           | mA            |
| I <sub>CC</sub> | Power Supply Current                        | V <sub>CC</sub> = Max.,<br>I <sub>OUT</sub> = 0 mA         | Commercial              |                 | 90     |                 | mA            |
|                 |   | Military   |                         | 100             |        | 38              | mA            |

### Capacitance<sup>[4]</sup>

| Parameters       | Description        | Test Conditions   | Max. | Units |
|------------------|--------------------|---|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = $25^{\circ}\text{C}$ , f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 4    | pF    |
| C <sub>OUT</sub> | Output Capacitance |   | 7    |       |

#### Notes:

- The CMOS process does not provide a clamp diode. However these devices are insensitive to  $-3\text{V}$  dc input levels and  $-5\text{V}$  undershoot pulses of less than 5 ns (measured at 50% points).
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Output is preconditioned to data in (inverted or non-inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.



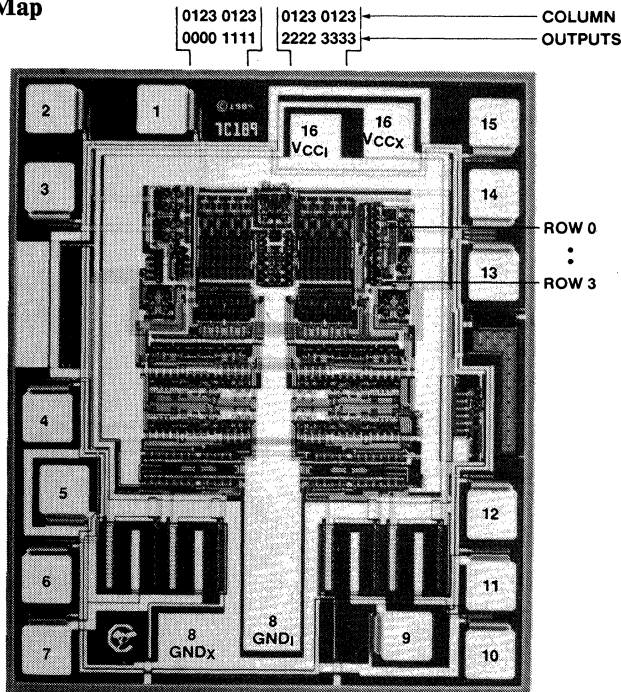
### Switching Characteristics Over the Operating Range<sup>[6, 7]</sup>

| Parameters                             | Description  | 27S03A<br>27S07A |      | 27S03<br>27S07 |      | 74S189 |      | 27LS03 |      | Units |
|--|--|------------------|------|----------------|------|--------|------|--------|------|-------|
|  |  | Min.             | Max. | Min.           | Max. | Min.   | Max. | Min.   | Max. |       |
| <b>READ CYCLE</b>                      |  |                  |      |                |      |        |      |        |      |       |
| t <sub>RC</sub>                        | Read Cycle Time  | 25               |      | 35             |      | 35     |      | 65     |      | ns    |
| t <sub>AA</sub>                        | Address to Data Valid <sup>[10]</sup>                        |                  | 25   |                | 35   |        | 35   |        | 65   | ns    |
| t <sub>ACS</sub>                       | $\overline{\text{CS}}$ Low to Data Valid <sup>[10]</sup>     |                  | 15   |                | 17   |        | 22   |        | 35   | ns    |
| t <sub>HZCS</sub>                      | $\overline{\text{CS}}$ HIGH to High Z <sup>[9, 11, 12]</sup> |                  | 15   |                | 20   |        | 17   |        | 35   | ns    |
| <b>WRITE CYCLE<sup>[3, 7, 8]</sup></b> |  |                  |      |                |      |        |      |        |      |       |
| t <sub>WC</sub>                        | Write Cycle Time   | 25               |      | 35             |      | 35     |      | 65     |      | ns    |
| t <sub>SA</sub>                        | Address Set-up to Write Start                                | 0                |      | 0              |      | 0      |      | 0      |      | ns    |
| t <sub>HA</sub>                        | Address Hold from Write End                                  | 0                |      | 0              |      | 0      |      | 0      |      | ns    |
| t <sub>SCS</sub>                       | $\overline{\text{CS}}$ Set-up to Write Start                 |                  |      |                |      | 0      |      |        |      | ns    |
| t <sub>HCS</sub>                       | $\overline{\text{CS}}$ Hold from Write End                   |                  |      |                |      | 0      |      |        |      | ns    |
| t <sub>SD</sub>                        | Data Set-up to Write End                                     | 20               |      | 25             |      | 20     |      | 55     |      | ns    |
| t <sub>HD</sub>                        | Data Hold from Write End                                     | 0                |      | 0              |      | 0      |      | 0      |      | ns    |
| t <sub>PWE</sub>                       | $\overline{\text{WE}}$ Pulse Width                           | 20               |      | 25             |      | 20     |      | 55     |      | ns    |
| t <sub>HZWE</sub>                      | $\overline{\text{WE}}$ LOW to High Z <sup>[9, 11, 12]</sup>  |                  | 20   |                | 25   |        | 20   |        | 35   | ns    |
| t <sub>AWE</sub>                       | $\overline{\text{WE}}$ HIGH to Output Valid <sup>[10]</sup>  |                  | 20   |                | 35   |        | 30   |        | 35   | ns    |

**Notes:**

7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
8. The internal write time of the memory is defined by the overlap of  $\overline{\text{CS}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. Transition is measured at steady state HIGH level - 500 mV or steady state LOW level + 500 mV on the output from 1.5V level on the input.
10. t<sub>AA</sub>, t<sub>ACS</sub> and t<sub>AWE</sub> are tested with C<sub>L</sub> = 30 pF as in Figure 1a. Timing is referenced to 1.5V on the inputs and outputs.
11. t<sub>HZCS</sub> and t<sub>HZWE</sub> are tested with C<sub>L</sub> = 5 pF as in Figure 1b.
12. At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device.

### Bit Map



### Address Designators

| Address Name   | Address Function | Pin Number |
|----------------|------------------|------------|
| A <sub>0</sub> | AX0              | 1          |
| A <sub>1</sub> | AX1              | 15         |
| A <sub>2</sub> | AY0              | 14         |
| A <sub>3</sub> | AY1              | 13         |

## AC Test Loads and Waveforms

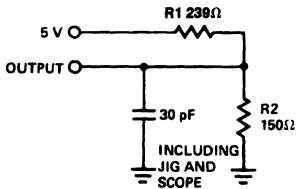


Figure 1a

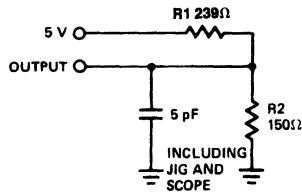
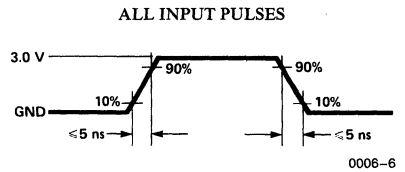
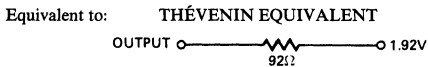


Figure 1b

0006-4

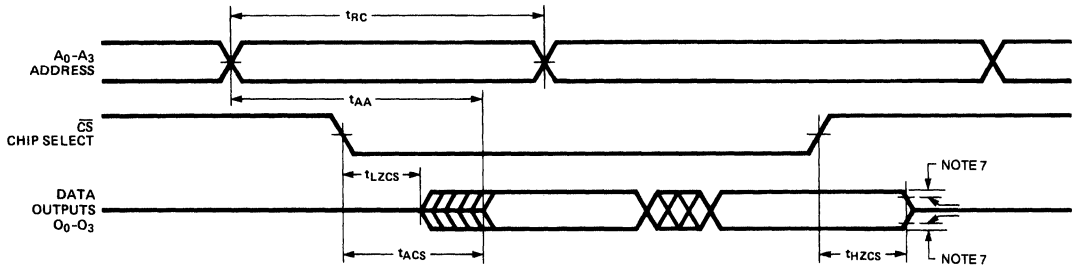


2



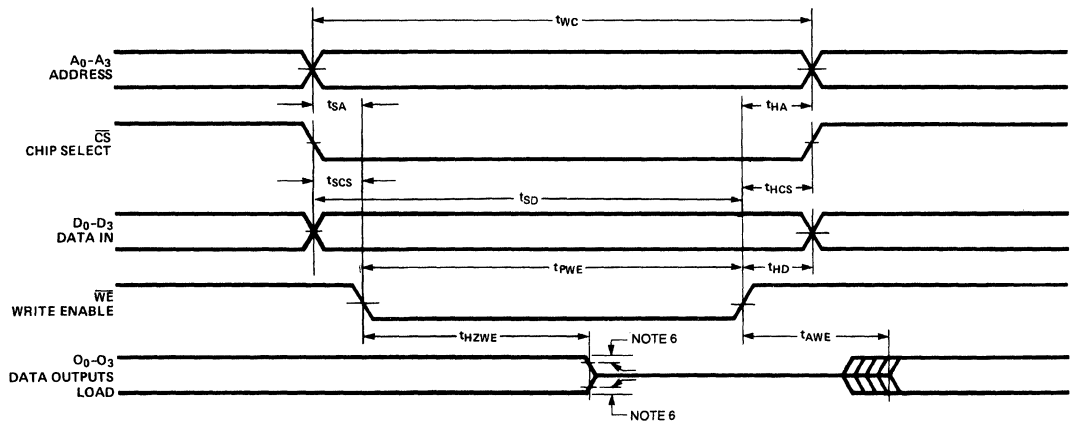
0006-5

## Read Mode



0006-7

## Write Mode



0006-8

(All above measurements referenced to 1.5V)

Note: Timing diagram represents one solution which results in optimum cycle time. Timing may be changed in various applications as long as the worst case limits are not violated.

### Ordering Information

| Speed (ns) | Ordering Code                        | Package Type | Operating Range |
|------------|--------------------------------------|--------------|-----------------|
| 25         | CY27S03APC<br>CY27S07APC             | P1           | Commercial      |
|            | CY27S03ADC<br>CY27S07ADC             | D2           |                 |
|            | CY27S03ALMB<br>CY27S07ALMB           | L61          | Military        |
|            | CY27S03ADMB<br>CY27S07ADMB           | D2           |                 |
| 35         | CY27S03PC<br>CY27S07PC<br>CY74S189PC | P1           | Commercial      |
|            | CY27S03DC<br>CY27S07DC<br>CY74S189DC | D2           |                 |
|            | CY27S03LC<br>CY27S07LC               | L61          |                 |
|            | CY27S03LMB<br>CY27S07LMB             | L61          | Military        |
|            | CY27S03DMB<br>CY27S07DMB             | D2           |                 |
| 65         | CY27LS03LMB                          | L61          | Military        |
|            | CY27LS03DMB                          | D2           |                 |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>Ix</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |

2

#### Switching Characteristics

| Parameters         | Subgroups   |
|--------------------|-------------|
| <b>READ CYCLE</b>  |             |
| t <sub>RC</sub>    | 7,8,9,10,11 |
| t <sub>AA</sub>    | 7,8,9,10,11 |
| t <sub>ACS</sub>   | 7,8,9,10,11 |
| <b>WRITE CYCLE</b> |             |
| t <sub>WC</sub>    | 7,8,9,10,11 |
| t <sub>SA</sub>    | 7,8,9,10,11 |
| t <sub>HA</sub>    | 7,8,9,10,11 |
| t <sub>SCS</sub>   | 7,8,9,10,11 |
| t <sub>HCS</sub>   | 7,8,9,10,11 |
| t <sub>SD</sub>    | 7,8,9,10,11 |
| t <sub>HD</sub>    | 7,8,9,10,11 |
| t <sub>PWE</sub>   | 7,8,9,10,11 |
| t <sub>AWE</sub>   | 7,8,9,10,11 |

Document #: 38-00041-C



### Features

- 256 x 4 static RAM for control stores in high speed computer
- Processed with high speed CMOS for optimum speed/power
- Separate inputs and outputs
- Low power
  - Standard power: 660 mW (commercial) 715 mW (military)
  - Low power: 440 mW (commercial) 495 mW (military)
- 5 volt power supply  $\pm 10\%$  tolerance both commercial and military
- Capable of withstanding greater than 2001V static discharge

### Functional Description

The CY93422 is a high performance CMOS static RAM organized as 256 x 4 bits. Easy memory expansion is provided by an active LOW chip select one ( $\overline{CS}_1$ ) input, an active HIGH chip select two ( $CS_2$ ) input, and three-state outputs.

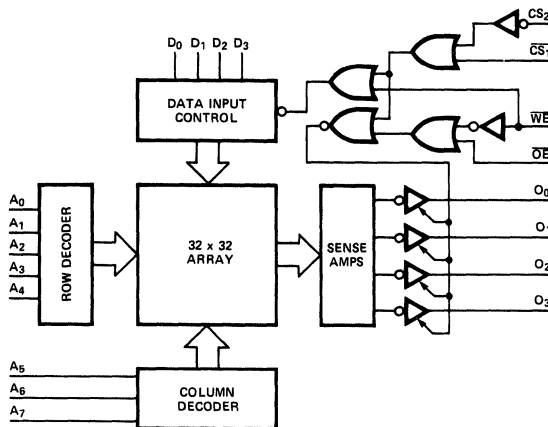
An active LOW write enable input ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When the chip select one ( $\overline{CS}_1$ ) and write enable ( $\overline{WE}$ ) inputs are LOW and the chip select two ( $CS_2$ ) input is HIGH, the information on the four data inputs  $D_0$  to  $D_3$  is written into the addressed memory word and the output circuitry is pre-conditioned so that the correct data is present at the outputs when the write cycle is complete. This preconditioning

operation insures minimum write recovery times by eliminating the "write recovery glitch."

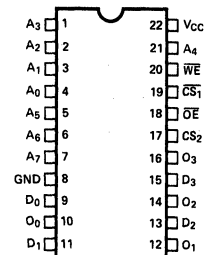
Reading is performed with the chip select one ( $\overline{CS}_1$ ) input LOW, the chip select two input ( $CS_2$ ) and write enable ( $\overline{WE}$ ) inputs HIGH, and the output enable input ( $\overline{OE}$ ) LOW. The information stored in the addressed word is read out on the four non-inverting outputs  $O_0$  to  $O_3$ .

The outputs of the memory go to an active high impedance state whenever chip select one ( $\overline{CS}_1$ ) is HIGH, chip select two ( $CS_2$ ) is LOW, output enable ( $\overline{OE}$ ) is HIGH, or during the writing operation when write enable ( $\overline{WE}$ ) is LOW.

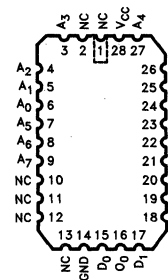
### Logic Block Diagram



### Pin Configurations



0002-2



0002-8

### Selection Guide (For higher performance and lower power refer to CY7C122 data sheet)

|                                |            | 93422A | 93L422A | 93422 | 93L422 |
|--------------------------------|------------|--------|---------|-------|--------|
| Maximum Access Time (ns)       | Commercial | 35     | 45      | 45    | 60     |
|                                | Military   | 45     | 55      | 60    | 75     |
| Maximum Operating Current (mA) | Commercial | 120    | 80      | 120   | 80     |
|                                | Military   | 130    | 90      | 130   | 90     |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|  |                              |
|--|------------------------------|
| Storage Temperature                                    | -65°C to +150°C              |
| Ambient Temperature with Power Applied                 | -55°C to +125°C              |
| Supply Voltage to Ground Potential (Pin 22 to Pin 8)   | -0.5V to +7.0V               |
| DC Voltage Applied to Outputs for High Output State    | -0.5V to V <sub>CC</sub> Max |
| DC Input Voltage                                       | -0.5V to +5.5V               |
| Output Current, into Outputs (Low)                     | 20 mA                        |
| DC Input Current                                       | -30 mA to +5.0 mA            |
| Static Discharge Voltage (per MIL-STD-883 Method 3015) | >2001V                       |
| Latchup Current  | >200 mA                      |

## Operating Range

| Range                   | V <sub>CC</sub> | Ambient Temperature |
|-------------------------|-----------------|---------------------|
| Commercial              | 5V ± 10%        | 0°C to +75°C        |
| Military <sup>[6]</sup> | 5V ± 10%        | -55°C to +125°C     |

## DC Electrical Characteristics Over Operating Range<sup>[5]</sup>

| Parameters       | Description                     | Test Conditions   | 93422<br>93422A           |            | 93L422<br>93L422A |            | Units |    |
|------------------|---------------------------------|---|---------------------------|------------|-------------------|------------|-------|----|
|                  |                                 |   | Min.                      | Max.       | Min.              | Max.       |       |    |
| V <sub>OH</sub>  | Output HIGH Voltage             | V <sub>CC</sub> = Min.,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | I <sub>OH</sub> = -5.2 mA | 2.4        |                   | 2.4        |       | V  |
| V <sub>OL</sub>  | Output LOW Voltage              | V <sub>CC</sub> = Min.,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | I <sub>OL</sub> = 8.0 mA  |            | 0.45              |            | 0.45  | V  |
| V <sub>IH</sub>  | Input HIGH Level <sup>[1]</sup> | Guaranteed Input Logical HIGH Voltage for all Inputs                            |                           | 2.1        |                   | 2.1        |       | V  |
| V <sub>IL</sub>  | Input LOW Level <sup>[1]</sup>  | Guaranteed Input Logical LOW Voltage for all Inputs                             |                           |            | 0.8               |            | 0.8   | V  |
| I <sub>IL</sub>  | Input LOW Current               | V <sub>CC</sub> = Max., V <sub>IN</sub> = 0.40V                                 |                           |            | -300              |            | -300  | μA |
| I <sub>IH</sub>  | Input HIGH Current              | V <sub>CC</sub> = Max., V <sub>IN</sub> = 4.5V                                  |                           |            | 40                |            | 40    | μA |
| I <sub>SC</sub>  | Output Short Circuit Current    | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0V <sup>[2]</sup>                  |                           |            | -90               |            | -90   | mA |
| I <sub>CC</sub>  | Power Supply Current            | All Inputs = GND,<br>V <sub>CC</sub> = Max.                                     | T <sub>A</sub> = 125°C    |            | 110               |            | 70    | mA |
|                  |                                 |   | T <sub>A</sub> = 75°C     |            | 110               |            | 70    |    |
|                  |                                 |   | T <sub>A</sub> = 0°C      |            | 120               |            | 80    |    |
|                  |                                 |   | T <sub>A</sub> = -55°C    |            | 130               |            | 90    |    |
| V <sub>CL</sub>  | Input Clamp Voltage             |   |                           | See Note 4 |                   | See Note 4 |       |    |
| I <sub>CEx</sub> | Output Leakage Current          | V <sub>OUT</sub> = 2.4V   |                           |            | 50                |            | 50    | μA |
|                  |                                 | V <sub>OUT</sub> = 0.5V, V <sub>CC</sub> = Max.                                 |                           | -50        |                   | -50        |       |    |
| C <sub>IN</sub>  | Input Pin Capacitance           | See Note 3  |                           |            | 4                 |            | 4     | pF |
| C <sub>OUT</sub> | Output Pin Capacitance          | See Note 3  |                           |            | 7                 |            | 7     | pF |

### Notes:

- These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
- Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
- Tested initially and after any design or process changes that may affect these parameters.
- The CMOS process does not provide a clamp diode. However, the CY93422 is insensitive to -3V dc input levels and -5V undershoot pulses of less than 10 ns (measured at 50% point).
- See the last page of this specification for Group A subgroup testing information.
- T<sub>A</sub> is the "instant on" case temperature.

## Function Table

| Inputs          |                 |    |    |                | Outputs        | Mode           |
|-----------------|-----------------|----|----|----------------|----------------|----------------|
| CS <sub>2</sub> | CS <sub>1</sub> | WE | OE | D <sub>n</sub> | O <sub>n</sub> |                |
| L               | X               | X  | X  | X              | *HIGH Z        | Not Select     |
| X               | H               | X  | X  | X              | *HIGH Z        | Not Select     |
| H               | L               | H  | H  | X              | *HIGH Z        | Output Disable |
| H               | L               | H  | L  | X              | Selected Data  | Read Data      |
| H               | L               | L  | X  | L              | *HIGH Z        | Write "0"      |
| H               | L               | L  | X  | H              | *HIGH Z        | Write "1"      |

H = High Voltage Level L = Low Voltage Level X = Don't Care  
\*HIGH Z implies outputs are disabled or off. This condition is defined as a high impedance state for the CY93422.

**Commercial Switching Characteristics**  $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0^\circ C$  to  $+75^\circ C$  (Unless Otherwise Noted)

| Parameters  | Description   | 93422A |      | 93L422A |      | 93422 |      | 93L422 |      | Units |
|---|---|--------|------|---------|------|-------|------|--------|------|-------|
|   |   | Min.   | Max. | Min.    | Max. | Min.  | Max. | Min.   | Max. |       |
| t <sub>PLH(A)</sub> <sup>[1]</sup><br>t <sub>PHL(A)</sub> <sup>[1]</sup>  | Delay from Address to Output (Address Access Time) (See Figure 2)                         |        | 35   |         | 45   |       | 45   |        | 60   | ns    |
| t <sub>PZH</sub> ( $\overline{CS}_1$ , CS <sub>2</sub> )<br>t <sub>PZL</sub> (CS <sub>1</sub> , $\overline{CS}_2$ ) | Delay from Chip Select to Active Output and Correct Data (See Figure 2)                   |        | 25   |         | 30   |       | 30   |        | 35   | ns    |
| t <sub>PZH</sub> ( $\overline{WE}$ )<br>t <sub>PZL</sub> ( $\overline{WE}$ )  | Delay from Write Enable to Active Output and Correct Data (Write Recovery) (See Figure 1) |        | 25   |         | 40   |       | 40   |        | 45   | ns    |
| t <sub>PZH</sub> ( $\overline{OE}$ )<br>t <sub>PZL</sub> ( $\overline{OE}$ )  | Delay from Output Enable to Active Output and Correct Data (See Figure 2)                 |        | 25   |         | 30   |       | 30   |        | 35   | ns    |
| t <sub>s</sub> (A)  | Setup Time Address (Prior to Initiation of Write) (See Figure 1)                          | 5      |      | 5       |      | 10    |      | 10     |      | ns    |
| t <sub>h</sub> (A)  | Hold Time Address (After Termination of Write) (See Figure 1)                             | 5      |      | 5       |      | 5     |      | 5      |      | ns    |
| t <sub>s</sub> (DI)   | Setup Time Data Input (Prior to Initiation of Write) (See Figure 1)                       | 5      |      | 5       |      | 5     |      | 5      |      | ns    |
| t <sub>h</sub> (DI)   | Hold Time Data Input (After Termination of Write) (See Figure 1)                          | 5      |      | 5       |      | 5     |      | 5      |      | ns    |
| t <sub>s</sub> ( $\overline{CS}_1$ , CS <sub>2</sub> )  | Setup Time Chip Select (Prior to Initiation of Write) (See Figure 1)                      | 5      |      | 5       |      | 5     |      | 5      |      | ns    |
| t <sub>h</sub> ( $\overline{CS}_1$ , CS <sub>2</sub> )  | Hold Time Chip Select (After Termination of Write) (See Figure 1)                         | 5      |      | 5       |      | 5     |      | 5      |      | ns    |
| t <sub>pw</sub> ( $\overline{WE}$ )   | Minimum Write Enable Pulse Width to Insure Write (See Figure 1)                           | 20     |      | 40      |      | 30    |      | 45     |      | ns    |
| t <sub>PHZ</sub> ( $\overline{CS}_1$ , CS <sub>2</sub> )<br>t <sub>PLZ</sub> (CS <sub>1</sub> , $\overline{CS}_2$ ) | Delay from Chip Select to Inactive Output (HIGH Z) (See Figure 2)                         |        | 30   |         | 40   |       | 30   |        | 45   | ns    |
| t <sub>PHZ</sub> ( $\overline{WE}$ )<br>t <sub>PLZ</sub> ( $\overline{WE}$ )  | Delay from Write Enable to Inactive Output (HIGH Z) (See Figure 1)                        |        | 30   |         | 40   |       | 35   |        | 45   | ns    |
| t <sub>PHZ</sub> ( $\overline{OE}$ )<br>t <sub>PLZ</sub> ( $\overline{OE}$ )  | Delay from Output Enable to Inactive Output (HIGH Z) (See Figure 2)                       |        | 30   |         | 40   |       | 30   |        | 45   | ns    |

**Notes:**

- t<sub>PLH</sub>(A) and t<sub>PHL</sub>(A) are tested with S<sub>1</sub> closed and C<sub>L</sub> = 15 pF with both input and output timing referenced to 1.5V.
- t<sub>PZH</sub>( $\overline{WE}$ ), t<sub>PZH</sub>( $\overline{CS}_1$ , CS<sub>2</sub>) and t<sub>PZH</sub>( $\overline{OE}$ ) are measured with S<sub>1</sub> open, C<sub>L</sub> = 15 pF and with both the input and output timing referenced to 1.5V. t<sub>PZL</sub>( $\overline{WE}$ ), t<sub>PZL</sub>(CS<sub>1</sub>,  $\overline{CS}_2$ ) and t<sub>PZL</sub>( $\overline{OE}$ ) are measured with S<sub>1</sub> closed, C<sub>L</sub> = 15 pF and with both the input and output

timing referenced to 1.5V. t<sub>PHZ</sub>( $\overline{WE}$ ), t<sub>PHZ</sub>( $\overline{CS}_1$ , CS<sub>2</sub>) and t<sub>PHZ</sub>( $\overline{OE}$ ) are measured with S<sub>1</sub> open, C<sub>L</sub> ≤ 5 pF and are measured between the 1.5V level on the input to the V<sub>OH</sub> - 500 mV level on the output. t<sub>PLZ</sub>( $\overline{WE}$ ), t<sub>PLZ</sub>(CS<sub>1</sub>,  $\overline{CS}_2$ ) and t<sub>PLZ</sub>( $\overline{OE}$ ) are measured with S<sub>1</sub> closed and C<sub>L</sub> ≤ 5 pF and are measured between the 1.5V level on the input and the V<sub>OL</sub> + 500 mV level on the output.

**Military Switching Characteristics**  $V_{CC} = 5V \pm 10\%$ ,  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  (Unless Otherwise Noted)<sup>[5]</sup>

| Parameters   | Description   | 93422A |      | 93L422A |      | 93422 |      | 93L422 |      | Units |
|--|---|--------|------|---------|------|-------|------|--------|------|-------|
|  |   | Min.   | Max. | Min.    | Max. | Min.  | Max. | Min.   | Max. |       |
| t <sub>PLH(A)</sub> <sup>[1]</sup><br>t <sub>PHL(A)</sub> <sup>[1]</sup>                     | Delay from Address to Output<br>(Address Access Time) (See Figure 2)                            |        | 45   |         | 55   |       | 60   |        | 75   | ns    |
| t <sub>PZH</sub> ( $\overline{CS}_1, CS_2$ )<br>t <sub>PZL</sub> ( $\overline{CS}_1, CS_2$ ) | Delay from Chip Select to Active<br>Output and Correct Data (See Figure 2)                      |        | 35   |         | 40   |       | 45   |        | 45   | ns    |
| t <sub>PZH</sub> ( $\overline{WE}$ )<br>t <sub>PZL</sub> ( $\overline{WE}$ )                 | Delay from Write Enable to<br>Active Output and Correct Data<br>(Write Recovery) (See Figure 1) |        | 40   |         | 45   |       | 50   |        | 50   | ns    |
| t <sub>PZH</sub> ( $\overline{OE}$ )<br>t <sub>PZL</sub> ( $\overline{OE}$ )                 | Delay from Output Enable to Active<br>Output and Correct Data (See Figure 2)                    |        | 35   |         | 40   |       | 45   |        | 45   | ns    |
| t <sub>s</sub> (A)   | Setup Time Address (Prior to<br>Initiation of Write) (See Figure 1)                             | 5      |      | 10      |      | 10    |      | 10     |      | ns    |
| t <sub>h</sub> (A)   | Hold Time Address (After<br>Termination of Write) (See Figure 1)                                | 5      |      | 5       |      | 5     |      | 10     |      | ns    |
| t <sub>s</sub> (DI)  | Setup Time Data Input (Prior to<br>Initiation of Write) (See Figure 1)                          | 5      |      | 5       |      | 5     |      | 5      |      | ns    |
| t <sub>h</sub> (DI)  | Hold Time Data Input (After<br>Termination of Write) (See Figure 1)                             | 5      |      | 5       |      | 5     |      | 5      |      | ns    |
| t <sub>s</sub> ( $\overline{CS}_1, CS_2$ )   | Setup Time Chip Select (Prior to<br>Initiation of Write) (See Figure 1)                         | 5      |      | 5       |      | 5     |      | 5      |      | ns    |
| t <sub>h</sub> ( $\overline{CS}_1, CS_2$ )   | Hold Time Chip Select (After<br>Termination of Write) (See Figure 1)                            | 5      |      | 5       |      | 5     |      | 10     |      | ns    |
| t <sub>pw</sub> ( $\overline{WE}$ )  | Minimum Write Enable Pulse Width<br>to Insure Write (See Figure 1)                              | 35     |      | 40      |      | 40    |      | 45     |      | ns    |
| t <sub>PHZ</sub> ( $\overline{CS}_1, CS_2$ )<br>t <sub>PLZ</sub> ( $\overline{CS}_1, CS_2$ ) | Delay from Chip Select to Inactive<br>Output (HIGH Z) (See Figure 2)                            |        | 35   |         | 40   |       | 45   |        | 45   | ns    |
| t <sub>PHZ</sub> ( $\overline{WE}$ )<br>t <sub>PLZ</sub> ( $\overline{WE}$ )                 | Delay from Write Enable to Inactive<br>Output (HIGH Z) (See Figure 1)                           |        | 40   |         | 40   |       | 45   |        | 45   | ns    |
| t <sub>PHZ</sub> ( $\overline{OE}$ )<br>t <sub>PLZ</sub> ( $\overline{OE}$ )                 | Delay from Output Enable to Inactive<br>Output (HIGH Z) (See Figure 2)                          |        | 35   |         | 40   |       | 45   |        | 45   | ns    |

**Notes:**

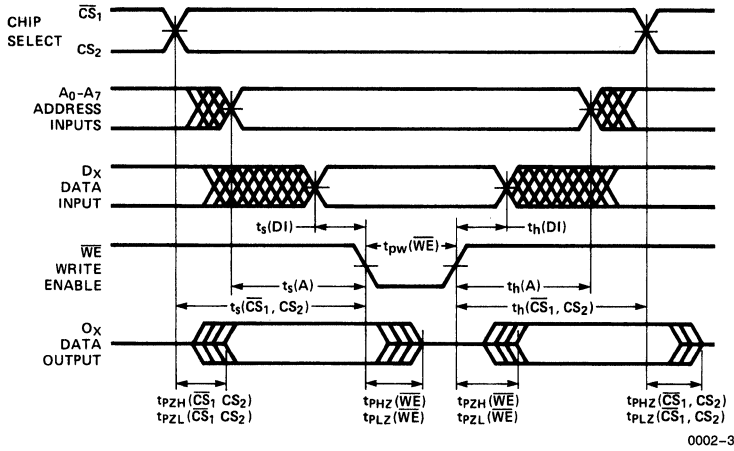
- t<sub>PLH</sub>(A) and t<sub>PHL</sub>(A) are tested with S<sub>1</sub> closed and C<sub>L</sub> = 15 pF with both input and output timing referenced to 1.5V.
- t<sub>PZH</sub>( $\overline{WE}$ ), t<sub>PZH</sub>( $\overline{CS}_1, CS_2$ ) and t<sub>PZH</sub>( $\overline{OE}$ ) are measured with S<sub>1</sub> open, C<sub>L</sub> = 15 pF and with both the input and output timing referenced to 1.5V. t<sub>PZL</sub>( $\overline{WE}$ ), t<sub>PZL</sub>( $\overline{CS}_1, CS_2$ ) and t<sub>PZL</sub>( $\overline{OE}$ ) are measured with S<sub>1</sub> closed, C<sub>L</sub> = 15 pF and with both the input and output

timing referenced to 1.5V. t<sub>PHZ</sub>( $\overline{WE}$ ), t<sub>PHZ</sub>( $\overline{CS}_1, CS_2$ ) and t<sub>PHZ</sub>( $\overline{OE}$ ) are measured with S<sub>1</sub> open, C<sub>L</sub> ≤ 5 pF and are measured between the 1.5V level on the input to the V<sub>OH</sub> - 500 mV level on the output. t<sub>PLZ</sub>( $\overline{WE}$ ), t<sub>PLZ</sub>( $\overline{CS}_1, CS_2$ ) and t<sub>PLZ</sub>( $\overline{OE}$ ) are measured with S<sub>1</sub> closed and C<sub>L</sub> ≤ 5 pF and are measured between the 1.5V level on the input and the V<sub>OL</sub> + 500 mV level on the output.



## Switching Waveforms

### Write Mode (with $\overline{OE} = \text{Low}$ )



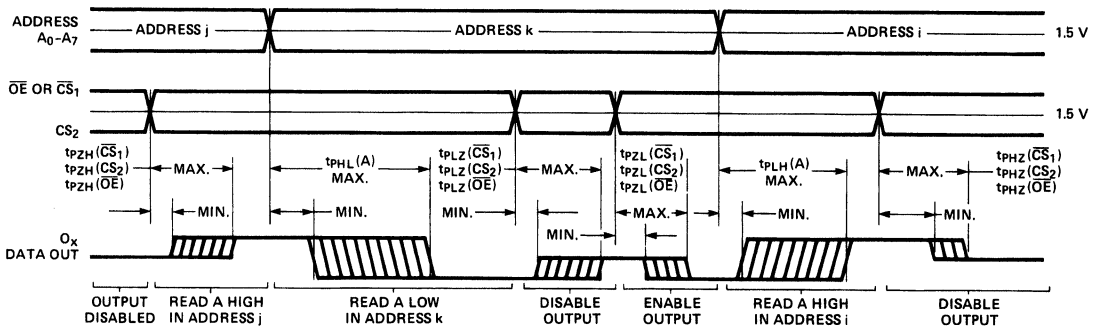
### Key to Timing Diagram

| Waveform | Inputs                           | Outputs                                   |
|----------|----------------------------------|---|
| —        | Must be steady                   | Will be steady                            |
| ▨        | May change from H to L           | Will be changing from H to L              |
| ▩        | May change from L to H           | Will be changing from L to H              |
| ▧        | Don't care; any change permitted | Changing; state unknown                   |
| ▬        | Does not apply                   | Center line is high impedance "off" state |

0002-4

Figure 1

### Read Mode



Switching delays from address input, output enable input and the chip select inputs to the data output. The CY93422 disabled output in the "OFF" condition is represented by a single center line.

Figure 2

### AC Test Load and Waveform

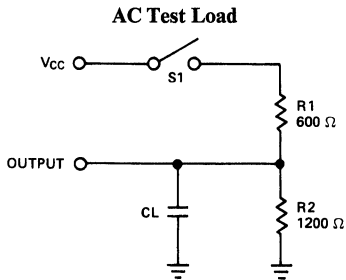


Figure 3

### Input Pulses

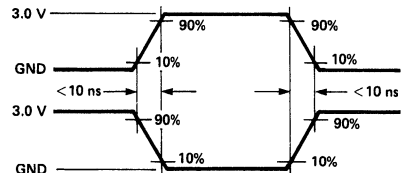


Figure 4

See Notes 1 and 2 of Switching Characteristics

## Ordering Information

| Speed<br>(ns) | Ordering Code                          |   | Package<br>Type | Operating<br>Range |
|---------------|--|---|-----------------|--------------------|
|               | Std. Power                             | Low Power                                 |                 |                    |
| 35            | CY93422APC<br>CY93422ADC<br>CY93422ALC |   | P7<br>D8<br>L54 | Commercial         |
| 45            | CY93422PC<br>CY93422DC<br>CY93422LC    | CY93L422APC<br>CY93L422ADC<br>CY93L422ALC | P7<br>D8<br>L54 | Commercial         |
|               | CY93422ADMB<br>CY93422ALMB             |   | D8<br>L54       | Military           |
| 55            |  | CY93L422ADMB<br>CY93L422ALMB              | D8<br>L54       | Military           |
| 60            | CY93422DMB<br>CY93422LMB               |   | D8<br>L54       | Military           |
|               |  | CY93L422PC<br>CY93L422DC<br>CY93L422LC    | P7<br>D8<br>L54 | Commercial         |
| 75            |  | CY93L422DMB<br>CY93L422LMB                | D8<br>L54       | Military           |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL</sub> Max. | 1,2,3     |
| I <sub>IL</sub>      | 1,2,3     |
| I <sub>IH</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>CEX</sub>     | 1,2,3     |

**Switching Characteristics**

| Parameters                                   | Subgroups   |
|--|-------------|
| t <sub>PLH(A)</sub>                          | 7,8,9,10,11 |
| t <sub>PHL(A)</sub>                          | 7,8,9,10,11 |
| t <sub>PZH</sub> ( $\overline{CS}_1, CS_2$ ) | 7,8,9,10,11 |
| t <sub>PZL</sub> ( $\overline{CS}_1, CS_2$ ) | 7,8,9,10,11 |
| t <sub>PZH</sub> ( $\overline{WE}$ )         | 7,8,9,10,11 |
| t <sub>PZL</sub> ( $\overline{WE}$ )         | 7,8,9,10,11 |
| t <sub>PZH</sub> ( $\overline{OE}$ )         | 7,8,9,10,11 |
| t <sub>PZL</sub> ( $\overline{OE}$ )         | 7,8,9,10,11 |
| t <sub>s</sub> (A)                           | 7,8,9,10,11 |
| t <sub>h</sub> (A)                           | 7,8,9,10,11 |
| t <sub>s</sub> (DI)                          | 7,8,9,10,11 |
| t <sub>h</sub> (DI)                          | 7,8,9,10,11 |
| t <sub>s</sub> ( $\overline{CS}_1, CS_2$ )   | 7,8,9,10,11 |
| t <sub>h</sub> ( $\overline{CS}_1, CS_2$ )   | 7,8,9,10,11 |
| t <sub>pw</sub> ( $\overline{WE}$ )          | 7,8,9,10,11 |

Document #: 38-00022-C



**128K x 8 Static RAM  
Module**

**Features**

- High-density 1 Megabit SRAM Module
- High speed CMOS SRAMs
  - Access time – 45 ns
- 32 pin – 0.6 in. wide DIP package
- JEDEC compatible pin-out
- Low active power – 1.2 W (max)
- Hermetic SMD Technology
- TTL compatible inputs and outputs
- Commercial and Military Temperature Ranges
- 2 V data retention (L version)

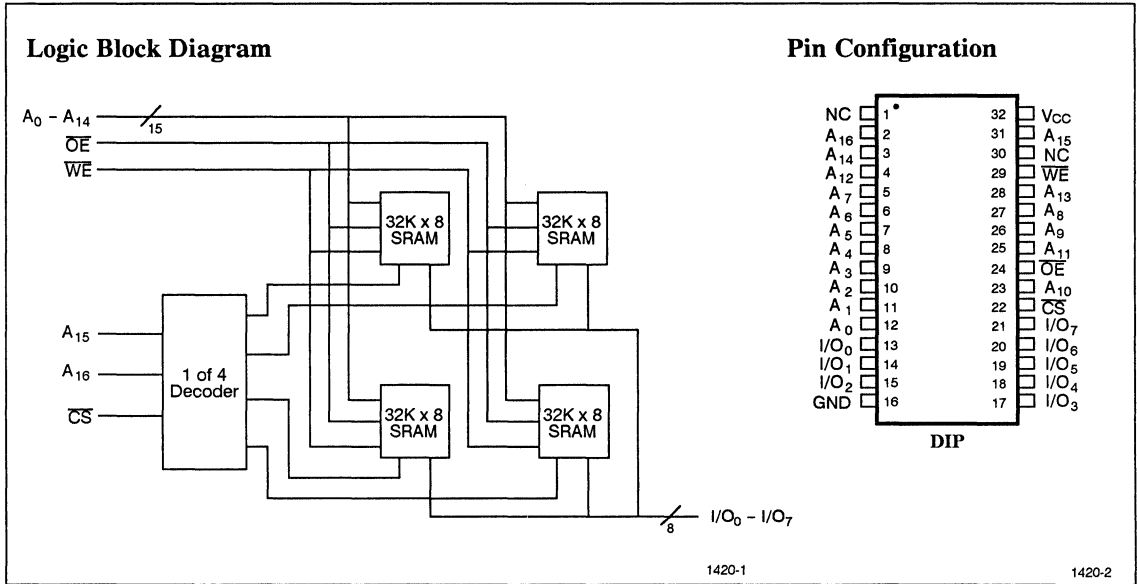
**Functional Description**

The CYM1420 is a very high performance 1 Megabit Static RAM module organized as 128K words by 8 bits. The module is constructed using four 32K x 8 Static RAMs in Leadless Chip Carriers mounted onto a double sided multilayer ceramic substrate. A decoder is used to interpret the higher order addresses  $A_{15}$  and  $A_{16}$  and select one of the four RAMs.

Writing to the memory module is accomplished when the chip select ( $\overline{CS}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the eight input/output pins ( $I/O_0$

through  $I/O_7$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{16}$ ). Reading the device is accomplished by taking chip select ( $\overline{CS}$ ), and output enable ( $\overline{OE}$ ) LOW, while write enable ( $\overline{WE}$ ) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the module is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH.



**Selection Guide**

|                                |            | 1420HD-45 | 1420HD-55 |
|--------------------------------|------------|-----------|-----------|
| Maximum Access time (ns)       |            | 45        | 55        |
| Maximum Operating Current (mA) | Commercial | 210       | 210       |
|                                | Military   | 210       | 210       |
| Maximum Standby Current (mA)   | Commercial | 80        | 80        |
|                                | Military   | 80        | 80        |

## Maximum Ratings

(Above which the useful life may be impaired)

|   |                 |
|---|-----------------|
| Storage Temperature .....                           | -65°C to +150°C |
| Ambient Temperature with Power Applied .....        | -55°C to +125°C |
| Supply Voltage to Ground Potential .....            | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State ..... | -0.5V to +7.0V  |
| DC Input Voltage .....                              | -0.5V to +7.0V  |
| Output Current into Outputs (Low) .....             | 20 mA           |

## Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C        | 5V ± 10%        |
| Military   | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over Operating Range

| Parameters       | Description                                    | Test Conditions  | CYM1420HD |                 | Units |
|------------------|--|--|-----------|-----------------|-------|
|                  |  |  | Min.      | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                            | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA  | 2.4       |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                             | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA   |           | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                             |  | 2.2       | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage                              |  | -0.5      | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current                             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -15       | +15             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                         | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled   | -15       | +15             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>    | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND   |           | -300            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current       | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS = V <sub>IL</sub>  |           | 210             | mA    |
| I <sub>SB1</sub> | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> , CS ≥ V <sub>IH</sub> ,<br>Min. Duty Cycle = 100%  |           | 80              | mA    |
| I <sub>SB2</sub> | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> , CS ≥ V <sub>CC</sub> - 0.3V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V |           | 80              | mA    |

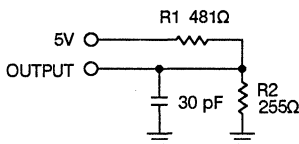
## Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions   | Max. | Units |
|------------------|--------------------|---|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 35   | pF    |
| C <sub>OUT</sub> | Output Capacitance |   | 40   |       |

### Notes:

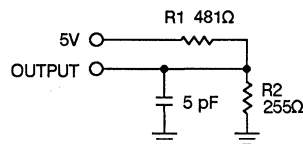
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the CS input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- Tested on a sample basis.

## AC Test Loads and Waveforms



INCLUDING  
JIG AND  
SCOPE

Figure 1a



INCLUDING  
JIG AND  
SCOPE

Figure 1b

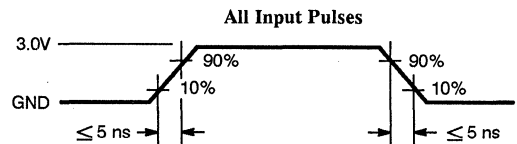
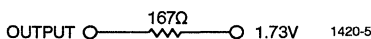


Figure 2

Equivalent to: THEVENIN EQUIVALENT



Switching Characteristics Over Operating Range <sup>[4]</sup>

| Parameters                        | Description                                      | 1420HD-45 |      | 1420HD-55 |      | Unit |
|-----------------------------------|--|-----------|------|-----------|------|------|
|                                   |  | Min.      | Max. | Min.      | Max. |      |
| <b>READ CYCLE</b>                 |  |           |      |           |      |      |
| t <sub>RC</sub>                   | Read Cycle Time                                  | 45        |      | 55        |      | ns   |
| t <sub>AA</sub>                   | Address to Data Valid                            |           | 45   |           | 55   | ns   |
| t <sub>OHA</sub>                  | Data Hold from Address Change                    | 5         |      | 5         |      | ns   |
| t <sub>ACS</sub>                  | $\overline{CS}$ LOW to Data Valid                |           | 45   |           | 55   | ns   |
| t <sub>DOE</sub>                  | $\overline{OE}$ LOW to Data Valid                |           | 25   |           | 30   | ns   |
| t <sub>LZOE</sub>                 | $\overline{OE}$ LOW to LOW Z                     | 5         |      | 5         |      | ns   |
| t <sub>HZOE</sub>                 | $\overline{OE}$ HIGH to HIGH Z                   |           | 20   |           | 25   | ns   |
| t <sub>LZCS</sub>                 | $\overline{CS}$ LOW to Low Z <sup>[6]</sup>      | 5         |      | 5         |      | ns   |
| t <sub>HZCS</sub>                 | $\overline{CS}$ HIGH to High Z <sup>[5, 6]</sup> |           | 20   |           | 25   | ns   |
| t <sub>PU</sub>                   | $\overline{CS}$ LOW to Power Up                  | 0         |      | 0         |      | ns   |
| t <sub>PD</sub>                   | $\overline{CS}$ HIGH to Power Down               |           | 45   |           | 55   | ns   |
| <b>WRITE CYCLE <sup>[7]</sup></b> |  |           |      |           |      |      |
| t <sub>WC</sub>                   | Write Cycle Time                                 | 45        |      | 55        |      | ns   |
| t <sub>SCS</sub>                  | $\overline{CS}$ LOW to Write End                 | 40        |      | 45        |      | ns   |
| t <sub>AW</sub>                   | Address Set-up to Write End                      | 40        |      | 45        |      | ns   |
| t <sub>HA</sub>                   | Address Hold from Write End                      | 5         |      | 5         |      | ns   |
| t <sub>SA</sub>                   | Address Set-up to Write Start                    | 5         |      | 5         |      | ns   |
| t <sub>PWE</sub>                  | $\overline{WE}$ Pulse Width                      | 25        |      | 30        |      | ns   |
| t <sub>SD</sub>                   | Data Set-up to Write End                         | 20        |      | 25        |      | ns   |
| t <sub>HD</sub>                   | Data Hold from Write End                         | 5         |      | 5         |      | ns   |
| t <sub>LZWE</sub>                 | $\overline{WE}$ HIGH to Low Z <sup>[6]</sup>     | 5         |      | 5         |      | ns   |
| t <sub>HZWE</sub>                 | $\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>  | 0         | 15   | 0         | 25   | ns   |

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
5. t<sub>HZCS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device. These parameters are guaranteed and not 100% tested.

7. The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

8.  $\overline{WE}$  is HIGH for read cycle.

9. Device is continuously selected,  $\overline{CS} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .

10. Address valid prior to or coincident with  $\overline{CS}$  transition low.

11. Data I/O will be high impedance if  $\overline{OE} = V_{IH}$ .

### Data Retention Characteristics (L Version Only)

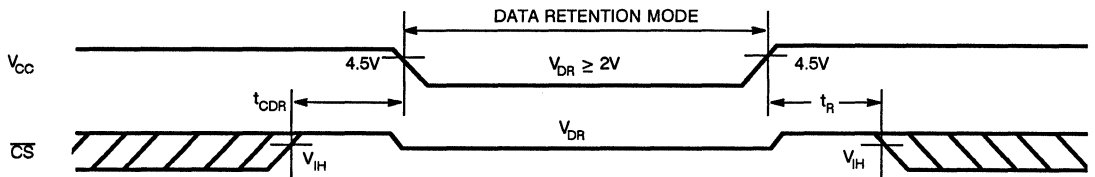
| Parameters       | Description                          | Test Conditions   | CYM1420         |      | Units   |
|------------------|--------------------------------------|---|-----------------|------|---------|
|                  |                                      |   | Min.            | Max. |         |
| $V_{DR}$         | $V_{CC}$ for Retention Data          | $V_{CC} = 2.0V$ ,<br>$\overline{CS} \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$<br>or $V_{IN} \leq 0.2V$ | 2.0             |      | V       |
| $I_{CCDR}$       | Data Retention Current               |   |                 | 16   | mA      |
| $t_{CDR}^{[13]}$ | Chip Deselect to Data Retention Time |   | 0               |      | ns      |
| $t_R^{[13]}$     | Operation Recovery Time              |   | $t_{RC}^{[12]}$ |      | ns      |
| $I_{LI}^{[13]}$  | Input Leakage Current                |   |                 | 8    | $\mu A$ |

**Notes:**

12.  $t_{RC}$  = Read Cycle Time.

13. Guaranteed, not tested.

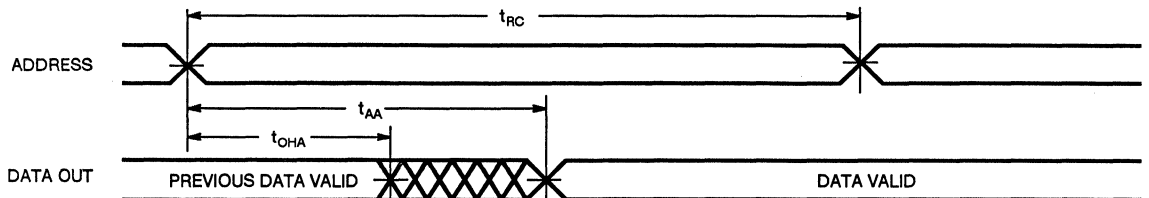
### Data Retention Waveform



1420-6

### Switching Waveforms<sup>[10]</sup>

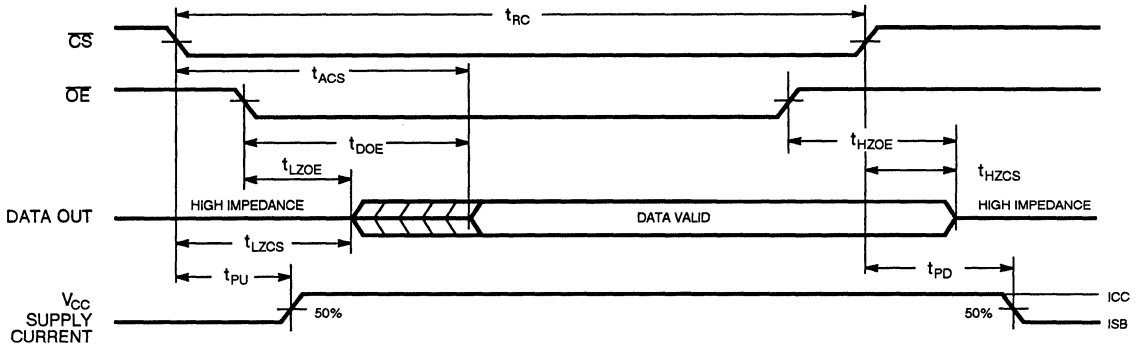
Read Cycle No. 1<sup>[8,9]</sup>



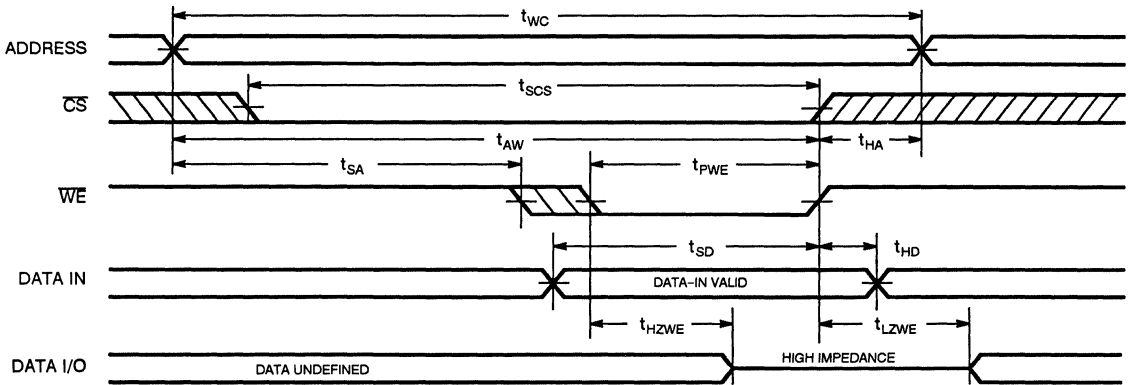
1420-7

### Switching Waveforms (Continued)

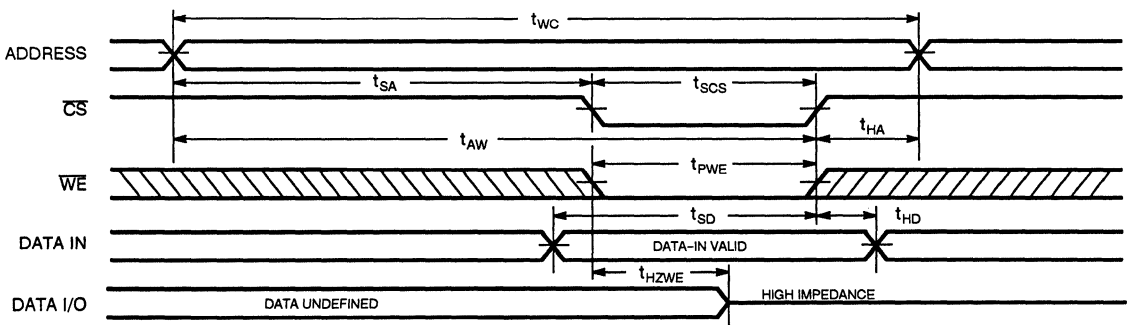
Read Cycle No. 2<sup>[8, 10]</sup>



Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[7, 11]</sup>



Write Cycle No. 2 ( $\overline{CS}$  Controlled)<sup>[7, 11]</sup>



Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.



**Truth Table**

| $\overline{\text{CS}}$ | $\overline{\text{WE}}$ | $\overline{\text{OE}}$ | Input/Outputs | Mode                |
|------------------------|------------------------|------------------------|---------------|---------------------|
| H                      | X                      | X                      | High Z        | Deselect Power Down |
| L                      | H                      | L                      | Data Out      | Read                |
| L                      | L                      | X                      | Data In       | Write               |
| L                      | H                      | H                      | High Z        | Deselect            |

**Ordering Information**

| Speed | Ordering Code   | Package Type | Operating Range |
|-------|-----------------|--------------|-----------------|
| 45    | CYM1420HD-45C   | HD04         | Commercial      |
|       | CYM1420LHD-45C  | HD04         |                 |
|       | CYM1420HD-45MB  | HD04         | Military        |
|       | CYM1420LHD-45MB | HD04         |                 |
| 55    | CYM1420HD-55C   | HD04         | Commercial      |
|       | CYM1420LHD-55C  | HD04         |                 |
|       | CYM1420HD-55MB  | HD04         | Military        |
|       | CYM1420LHD-55MB | HD04         |                 |

Document #: 38-M-00001



**Features**

- High-density 1 Megabit SRAM Module
- High speed CMOS SRAMs  
— Access time – 70 ns
- 32 pin – 0.6 in. wide DIP package
- JEDEC compatible pin-out
- Low active power – 660 mW (max)
- Hermetic SMD Technology
- TTL compatible inputs and outputs
- Commercial and Military Temperature Ranges
- 2 V data retention (L version)

**Functional Description**

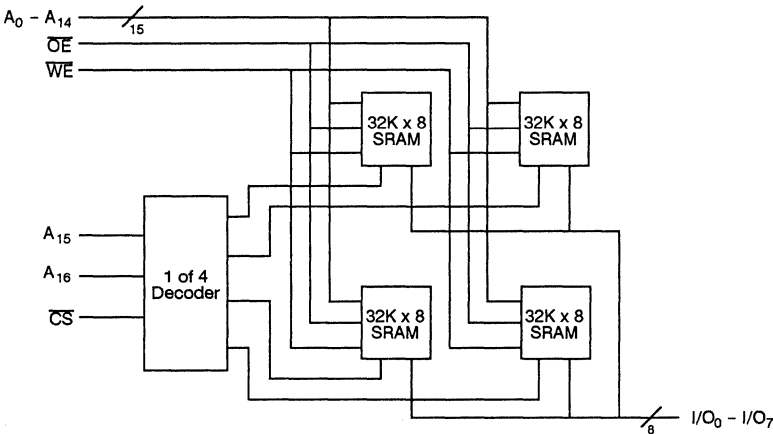
The CYM1421 is a high performance 1 Megabit Static RAM module organized as 128K words by 8 bits. The module is constructed using four 32K x 8 Static RAMs in Leadless Chip Carriers mounted onto a double sided multilayer ceramic substrate. A decoder is used to interpret the higher order addresses  $A_{15}$  and  $A_{16}$  and select one of the four RAMs.

Writing to the memory module is accomplished when the chip select ( $\overline{CS}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the eight input/output pins ( $I/O_0$

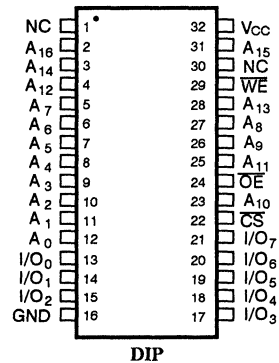
through  $I/O_7$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{16}$ ). Reading the device is accomplished by taking chip select ( $\overline{CS}$ ), and output enable ( $\overline{OE}$ ) LOW, while write enable ( $\overline{WE}$ ) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the module is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH.

**Logic Block Diagram**



**Pin Configuration**



1421-1

1421-2

**Selection Guide**

|                                |            | 1421HD-70 | 1421HD-85 |
|--------------------------------|------------|-----------|-----------|
| Maximum Access time (ns)       |            | 70        | 85        |
| Maximum Operating Current (mA) | Commercial | 120       | 120       |
|                                | Military   | 120       | 120       |
| Maximum Standby Current (mA)   | Commercial | 70        | 70        |
|                                | Military   | 70        | 70        |

### Maximum Ratings

(Above which the useful life may be impaired)

|  |                 |
|--|-----------------|
| Storage Temperature .....                              | -65°C to +150°C |
| Ambient Temperature with<br>Power Applied .....        | -55°C to +125°C |
| Supply Voltage to Ground Potential .....               | -0.3V to +7.0V  |
| DC Voltage Applied to Outputs<br>in High Z State ..... | -0.3V to +7.0V  |
| DC Input Voltage .....                                 | -0.3V to +7.0V  |
| Output Current into Outputs (Low) .....                | 50 mA           |

### Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C        | 5V ± 10%        |
| Military   | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range

| Parameters       | Description                                    | Test Conditions  | CYM1421HD |                 | Units |
|------------------|--|--|-----------|-----------------|-------|
|                  |  |  | Min.      | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                            | V <sub>CC</sub> = Min., I <sub>OH</sub> = -1.0 mA  | 2.4       |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                             | V <sub>CC</sub> = Min., I <sub>OL</sub> = 4.0 mA   |           | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                             |  | 2.2       | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage                              |  | -0.3      | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current                             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -10       | +10             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                         | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled   | -10       | +10             | μA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current       | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS = V <sub>IL</sub>  |           | 120             | mA    |
| I <sub>SB1</sub> | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> , CS ≥ V <sub>IH</sub> ,<br>Min. Duty Cycle = 100%  |           | 70              | mA    |
| I <sub>SB2</sub> | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> , CS ≥ V <sub>CC</sub> - 0.2V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or<br>V <sub>IN</sub> ≤ 0.2V |           | 20              | mA    |

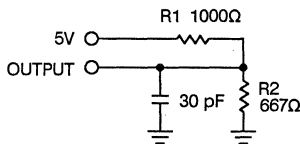
### Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 35   | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 40   |       |

#### Notes:

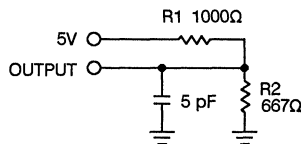
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the CS input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- Tested on a sample basis.

### AC Test Loads and Waveforms



INCLUDING  
JIG AND  
SCOPE

Figure 1a



INCLUDING  
JIG AND  
SCOPE

Figure 1b

1421-3

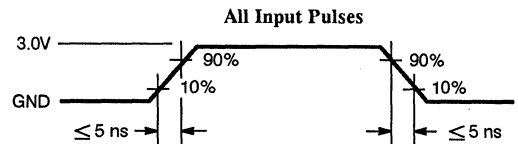
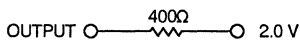


Figure 2

1421-4

Equivalent to: THEVENIN EQUIVALENT



1421-5

Switching Characteristics Over Operating Range <sup>[4]</sup>

| Parameters                        | Description                                      | 1421HD-70 |      | 1421HD-85 |      | Units |
|-----------------------------------|--|-----------|------|-----------|------|-------|
|                                   |  | Min.      | Max. | Min.      | Max. |       |
| <b>READ CYCLE</b>                 |  |           |      |           |      |       |
| t <sub>RC</sub>                   | Read Cycle Time                                  | 70        |      | 85        |      | ns    |
| t <sub>AA</sub>                   | Address to Data Valid                            |           | 70   |           | 85   | ns    |
| t <sub>OHA</sub>                  | Data Hold from Address Change                    | 5         |      | 5         |      | ns    |
| t <sub>ACS</sub>                  | $\overline{CS}$ LOW to Data Valid                |           | 70   |           | 85   | ns    |
| t <sub>DOE</sub>                  | $\overline{OE}$ LOW to Data Valid                |           | 40   |           | 50   | ns    |
| t <sub>LZOE</sub>                 | $\overline{OE}$ LOW to LOW Z                     | 5         |      | 5         |      | ns    |
| t <sub>HZOE</sub>                 | $\overline{OE}$ HIGH to HIGH Z                   |           | 30   |           | 35   | ns    |
| t <sub>LZCS</sub>                 | $\overline{CS}$ LOW to Low Z <sup>[6]</sup>      | 5         |      | 5         |      | ns    |
| t <sub>HZCS</sub>                 | $\overline{CS}$ HIGH to High Z <sup>[5, 6]</sup> |           | 35   |           | 35   | ns    |
| <b>WRITE CYCLE <sup>[7]</sup></b> |  |           |      |           |      |       |
| t <sub>WC</sub>                   | Write Cycle Time                                 | 70        |      | 85        |      | ns    |
| t <sub>SCS</sub>                  | $\overline{CS}$ LOW to Write End                 | 65        |      | 75        |      | ns    |
| t <sub>AW</sub>                   | Address Set-up to Write End                      | 65        |      | 75        |      | ns    |
| t <sub>HA</sub>                   | Address Hold from Write End                      | 10        |      | 15        |      | ns    |
| t <sub>SA</sub>                   | Address Set-up to Write Start                    | 25        |      | 25        |      | ns    |
| t <sub>PWE</sub>                  | $\overline{WE}$ Pulse Width                      | 30        |      | 35        |      | ns    |
| t <sub>SD</sub>                   | Data Set-up to Write End                         | 20        |      | 20        |      | ns    |
| t <sub>HD</sub>                   | Data Hold from Write End                         | 10        |      | 10        |      | ns    |
| t <sub>LZWE</sub>                 | $\overline{WE}$ LOW to Low Z <sup>[6]</sup>      | 5         |      | 5         |      | ns    |
| t <sub>HZWE</sub>                 | $\overline{WE}$ HIGH to High Z <sup>[5, 6]</sup> | 0         | 45   | 0         | 50   | ns    |

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>, I<sub>OH</sub> and 30 pF load capacitance.

5. t<sub>HZCS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ±500 mV from steady state voltage.

6. At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device. These parameters are guaranteed and not 100% tested.

7. The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

8.  $\overline{WE}$  is HIGH for read cycle.

9. Device is continuously selected,  $\overline{CS} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .

10. Address valid prior to or coincident with  $\overline{CS}$  transition low.

11. Data I/O will be high impedance if  $\overline{OE} = V_{IH}$ .

**Data Retention Characteristics (L Version Only)**

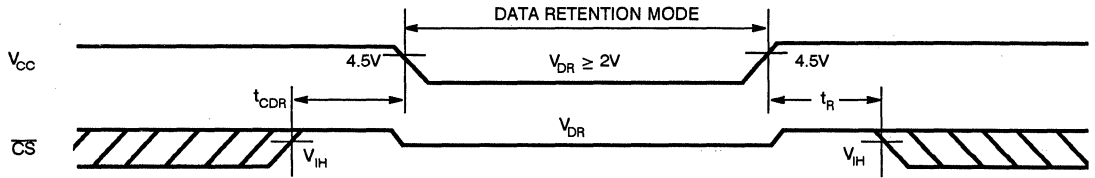
| Parameter        | Description                          | Test Conditions  | CYM1421         |      | Units   |
|------------------|--------------------------------------|--|-----------------|------|---------|
|                  |                                      |  | Min.            | Max. |         |
| $V_{DR}$         | $V_{CC}$ for Retention Data          | $V_{CC} = 2.0V,$<br>$\overline{CS} \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$<br>or $V_{IN} \leq 0.2V$ | 2.0             |      | V       |
| $I_{CCDR}$       | Data Retention Current               |  |                 | 250  | $\mu A$ |
| $t_{CDR}^{[13]}$ | Chip Deselect to Data Retention Time |  | 0               |      | ns      |
| $t_R^{[13]}$     | Operation Recovery Time              |  | $t_{RC}^{[12]}$ |      | ns      |

Notes:

12.  $t_{RC}$  = Read Cycle Time.

13. Guaranteed, not tested.

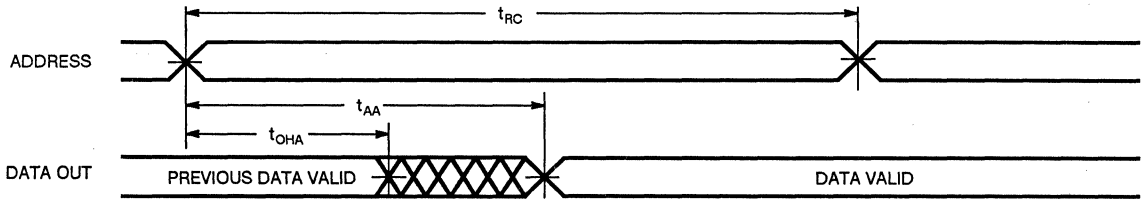
**Data Retention Waveform**



1421-6

**Switching Waveforms<sup>[10]</sup>**

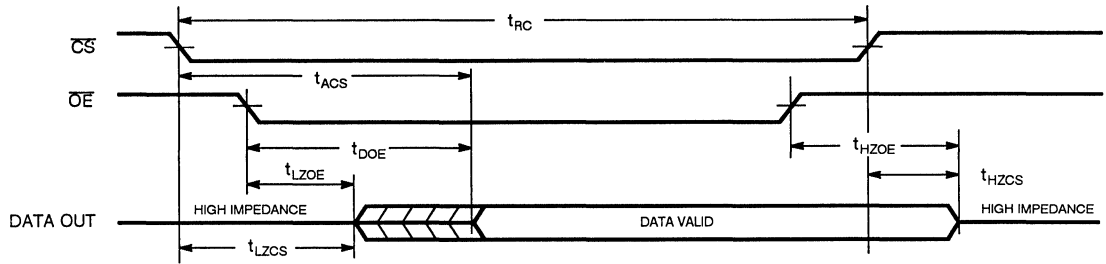
Read Cycle No. 1<sup>[8,9]</sup>



1421-7

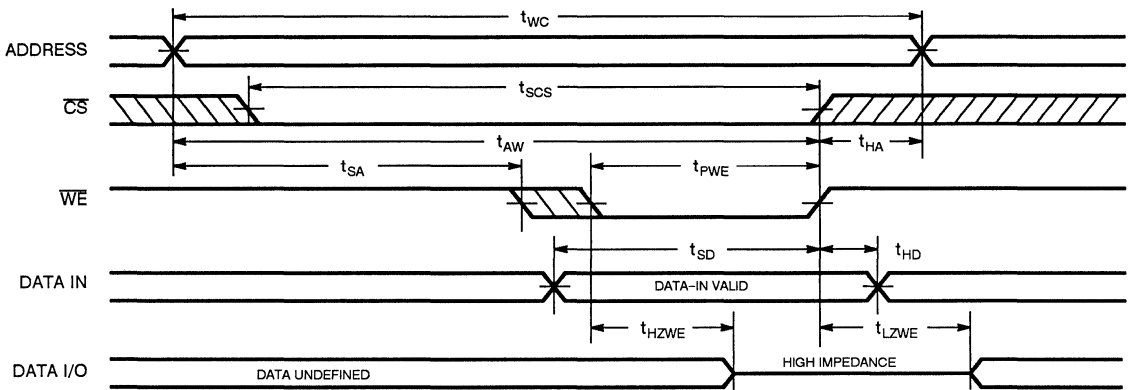
## Switching Waveforms (Continued)

### Read Cycle No. 2<sup>[8, 10]</sup>



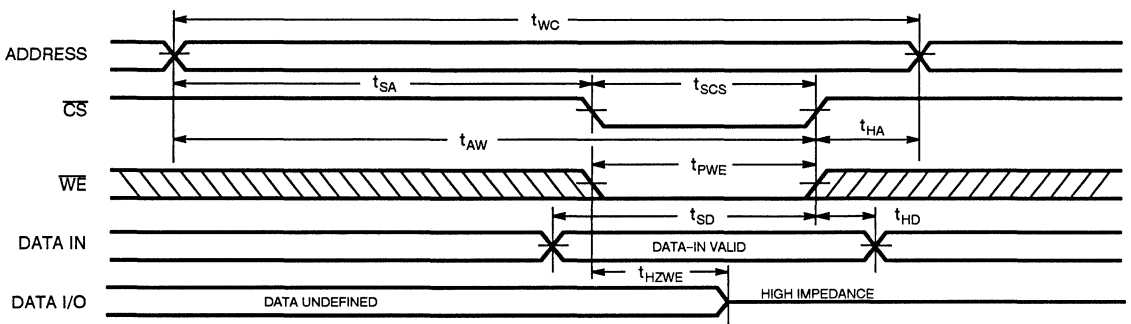
1421-8

### Write Cycle No. 1 ( $\overline{WE}$ Controlled)<sup>[7, 11]</sup>



1421-9

### Write Cycle No. 2 ( $\overline{CS}$ Controlled)<sup>[7, 11]</sup>



1421-10

Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

### Truth Table

| CS | WE | OE | Input/Outputs | Mode                |
|----|----|----|---------------|---------------------|
| H  | X  | X  | High Z        | Deselect Power Down |
| L  | H  | L  | Data Out      | Read                |
| L  | L  | X  | Data In       | Write               |
| L  | H  | H  | High Z        | Deselect            |

### Ordering Information

| Speed | Ordering Code  | Package Type | Operating Range |
|-------|----------------|--------------|-----------------|
| 70    | CYM1421HD-70C  | HD04         | Commercial      |
|       | CYM1421LHD-70C | HD04         |                 |
|       | CYM1421HD-70M  | HD04         | Military        |
|       | CYM1421LHD-70M | HD04         |                 |
| 85    | CYM1421HD-85C  | HD04         | Commercial      |
|       | CYM1421LHD-85C | HD04         |                 |
|       | CYM1421HD-85M  | HD04         | Military        |
|       | CYM1421LHD-85M | HD04         |                 |

Document #: 38-M-00002



# 128K x 8 Static RAM Module

## Features

- High-density 1M bit SRAM Module
- High speed CMOS SRAMs  
— Access time – 30 ns
- Low active power – 1.3 W (max)
- SMD technology
- TTL compatible inputs and outputs
- Low profile  
— Max. height – .50 in.
- Small PCB footprint – 0.8 sq in.
- 2V data retention (L version)

## Functional Description

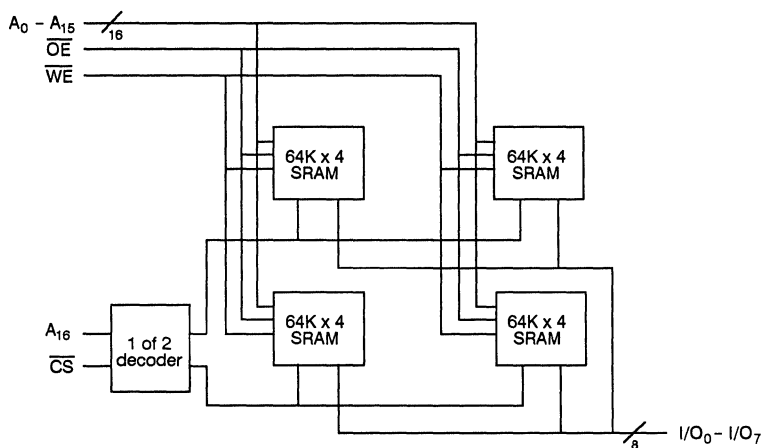
The CYM1422 is a high performance 1 Megabit Static RAM module organized as 128K words by 8 bits. This module is constructed using four 64K x 4 Static RAMs in SOJs mounted onto a single sided multilayer epoxy laminate board with pins. A decoder is used to interpret the higher order address A<sub>16</sub> and select one pair of the four RAMs.

Writing to the memory module is accomplished when the chip select ( $\overline{CS}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the eight input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the memory

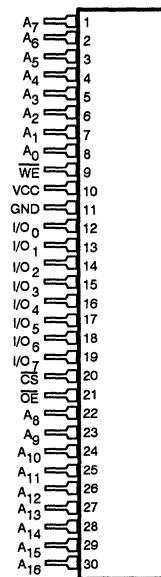
location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>). Reading the device is accomplished by taking chip select ( $\overline{CS}$ ) and output enable ( $\overline{OE}$ ) LOW, while write enable ( $\overline{WE}$ ) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the module is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH.

## Logic Block Diagram



## Pin Configuration



SIP

Component Side

1422-1

1422-2

## Selection Guide

|                                | 1422PS-30 | 1422PS-35 | 1422PS-45 | 1422PS-55 |
|--------------------------------|-----------|-----------|-----------|-----------|
| Maximum Access time (ns)       | 30        | 35        | 45        | 55        |
| Maximum Operating Current (mA) | 230       | 230       | 230       | 230       |
| Maximum Standby Current (mA)   | 80        | 80        | 80        | 80        |



## Maximum Ratings

(Above which the useful life may be impaired)

|   |                 |
|---|-----------------|
| Storage Temperature .....                           | -65°C to +150°C |
| Ambient Temperature with Power Applied .....        | -10°C to +90°C  |
| Supply Voltage to Ground Potential .....            | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State ..... | -0.5V to +7.0V  |
| DC Input Voltage .....                              | -0.5V to +7.0V  |
| Output Current into Outputs (Low) .....             | 20 mA           |

## Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C        | 5V ± 10%        |

## Electrical Characteristics Over Operating Range

| Parameters       | Description                                    | Test Conditions  | CYM1422PS |                 | Units |
|------------------|--|--|-----------|-----------------|-------|
|                  |  |  | Min.      | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                            | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA  | 2.4       |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                             | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA   |           | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                             |  | 2.2       | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage                              |  | -0.5      | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current                             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -15       | +15             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                         | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled   | -15       | +15             | μA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current       | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS ≤ V <sub>IL</sub>  |           | 230             | mA    |
| I <sub>SB1</sub> | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> ; CS ≥ V <sub>IH</sub><br>Min. Duty Cycle = 100%  |           | 80              | mA    |
| I <sub>SB2</sub> | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> ; CS ≥ V <sub>CC</sub> - 0.3V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V |           | 80              | mA    |

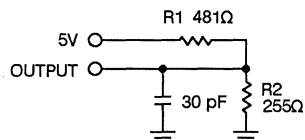
## Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions   | Max. | Units |
|------------------|--------------------|---|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 40   | pF    |
| C <sub>OUT</sub> | Output Capacitance |   | 30   |       |

### Notes:

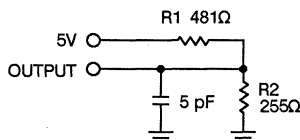
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the CS input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- Tested on a sample basis.

## AC Test Loads and Waveforms



INCLUDING  
JIG AND  
SCOPE

Figure 1a



INCLUDING  
JIG AND  
SCOPE

Figure 1b

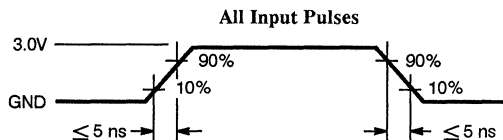
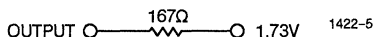


Figure 2

Equivalent to: THEVENIN EQUIVALENT



Switching Characteristics Over Operating Range <sup>[4]</sup>

| Parameters                        | Description   | 1422PS-30 |      | 1422PS-35 |      | 1422PS-45 |      | 1422PS-55 |      | Units |
|-----------------------------------|---|-----------|------|-----------|------|-----------|------|-----------|------|-------|
|                                   |   | Min.      | Max. | Min.      | Max. | Min.      | Max. | Min.      | Max. |       |
| <b>READ CYCLE</b>                 |   |           |      |           |      |           |      |           |      |       |
| t <sub>RC</sub>                   | Read Cycle Time   | 30        |      | 35        |      | 45        |      | 55        |      | ns    |
| t <sub>AA</sub>                   | Address to Data Valid                                   |           | 30   |           | 35   |           | 45   |           | 55   | ns    |
| t <sub>OHA</sub>                  | Data Hold from Address Change                           | 3         |      | 3         |      | 3         |      | 3         |      | ns    |
| t <sub>ACS</sub>                  | $\overline{\text{CS}}$ LOW to Data Valid                |           | 30   |           | 35   |           | 45   |           | 55   | ns    |
| t <sub>DOE</sub>                  | $\overline{\text{OE}}$ LOW to Data Valid                |           | 20   |           | 25   |           | 30   |           | 30   | ns    |
| t <sub>LZOE</sub>                 | $\overline{\text{OE}}$ LOW to LOW Z                     | 3         |      | 3         |      | 3         |      | 3         |      | ns    |
| t <sub>HZOE</sub>                 | $\overline{\text{OE}}$ HIGH to HIGH Z                   |           | 20   |           | 20   |           | 20   |           | 20   | ns    |
| t <sub>LZCS</sub>                 | $\overline{\text{CS}}$ LOW to Low Z <sup>[6]</sup>      | 3         |      | 3         |      | 3         |      | 3         |      | ns    |
| t <sub>HZCS</sub>                 | $\overline{\text{CS}}$ HIGH to High Z <sup>[5, 6]</sup> |           | 15   |           | 20   |           | 20   |           | 20   | ns    |
| t <sub>PU</sub>                   | $\overline{\text{CS}}$ LOW to Power Up                  | 0         |      | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>PD</sub>                   | $\overline{\text{CS}}$ HIGH to Power Down               |           | 30   |           | 35   |           | 45   |           | 55   | ns    |
| <b>WRITE CYCLE <sup>[7]</sup></b> |   |           |      |           |      |           |      |           |      |       |
| t <sub>WC</sub>                   | Write Cycle Time  | 25        |      | 30        |      | 40        |      | 50        |      | ns    |
| t <sub>SCS</sub>                  | $\overline{\text{CS}}$ LOW to Write End                 | 30        |      | 35        |      | 45        |      | 55        |      | ns    |
| t <sub>AW</sub>                   | Address Set-up to Write End                             | 30        |      | 35        |      | 45        |      | 55        |      | ns    |
| t <sub>HA</sub>                   | Address Hold from Write End                             | 4         |      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>SA</sub>                   | Address Set-up to Write Start                           | 5         |      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>PWE</sub>                  | $\overline{\text{WE}}$ Pulse Width                      | 25        |      | 35        |      | 35        |      | 40        |      | ns    |
| t <sub>SD</sub>                   | Data Set-up to Write End                                | 15        |      | 20        |      | 20        |      | 25        |      | ns    |
| t <sub>HD</sub>                   | Data Hold from Write End                                | 5         |      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>LZWE</sub>                 | $\overline{\text{WE}}$ HIGH to Low Z <sup>[6]</sup>     | 3         |      | 3         |      | 3         |      | 3         |      | ns    |
| t <sub>HZWE</sub>                 | $\overline{\text{WE}}$ LOW to High Z <sup>[5, 6]</sup>  | 0         | 15   | 0         | 20   | 0         | 25   | 0         | 30   | ns    |

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZCS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device. These parameters are guaranteed and not 100% tested.
- The internal write time of the memory is defined by the overlap of  $\overline{\text{CS}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{\text{WE}}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{\text{CS}} = V_{IL}$  and  $\overline{\text{OE}} = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{\text{CS}}$  transition low.
- Data I/O will be high impedance if  $\overline{\text{OE}} = V_{IH}$

### Data Retention Characteristics (L Version Only)

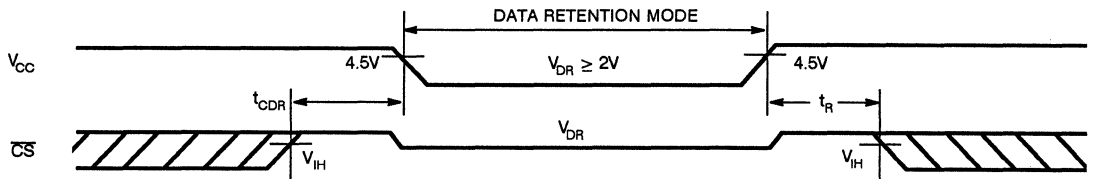
| Parameter        | Description                          | Test Conditions   | CYM1422         |      | Units   |
|------------------|--------------------------------------|---|-----------------|------|---------|
|                  |                                      |   | Min.            | Max. |         |
| $V_{DR}$         | $V_{CC}$ for Retention Data          | $V_{CC} = 2.0V$ ,<br>$\overline{CS} \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$<br>or $V_{IN} \leq 0.2V$ | 2.0             |      | V       |
| $I_{CCDR}$       | Data Retention Current               |   |                 | 16   | mA      |
| $t_{CDR}^{(13)}$ | Chip Deselect to Data Retention Time |   | 0               |      | ns      |
| $t_R^{(13)}$     | Operation Recovery Time              |   | $t_{RC}^{(12)}$ |      | ns      |
| $I_{LI}^{(13)}$  | Input Leakage Current                |   |                 | 16   | $\mu A$ |

**Notes:**

12.  $t_{RC}$  = Read Cycle Time.

13. Guaranteed, not tested.

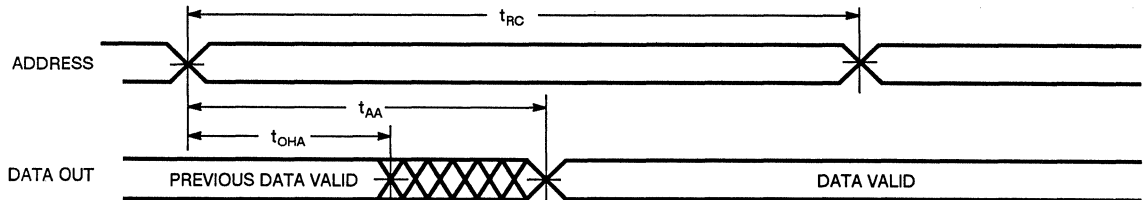
### Data Retention Waveform



1422-6

### Switching Waveforms<sup>(11)</sup>

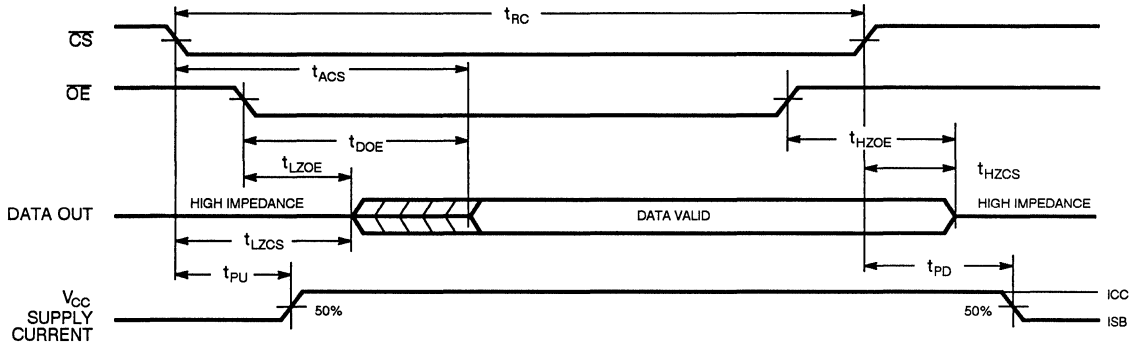
Read Cycle No. 1<sup>(8, 9)</sup>



1422-7

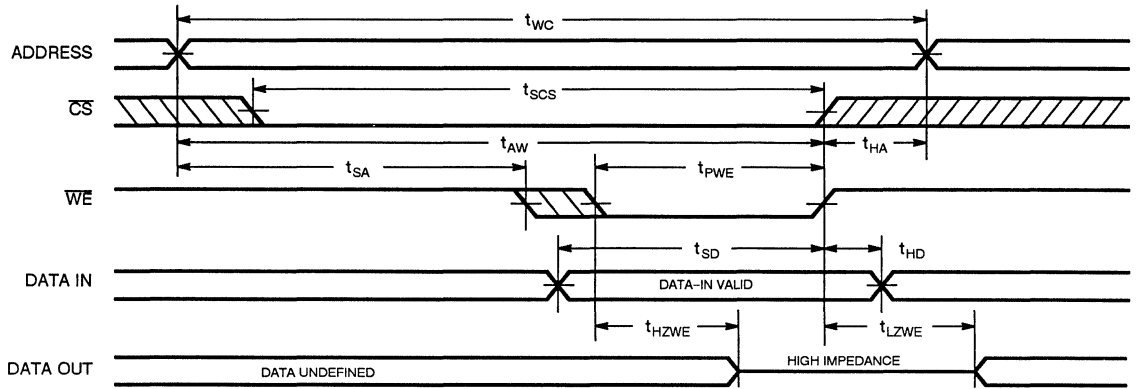
Switching Waveforms (Continued)

Read Cycle No. 2<sup>[8, 10]</sup>



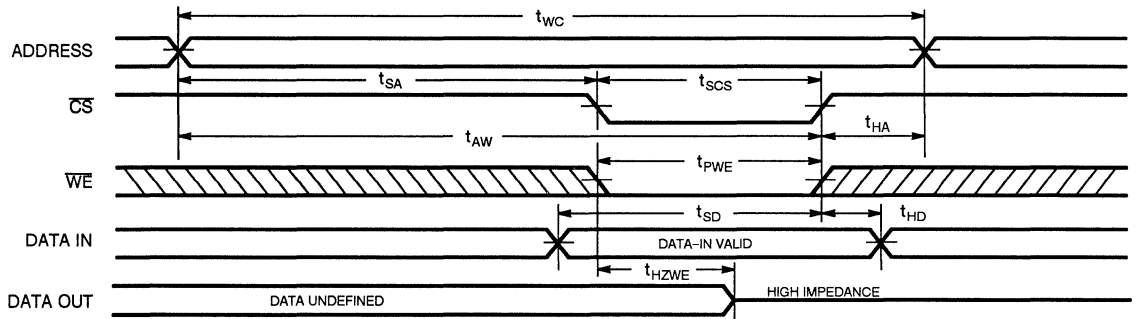
1422-8

Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[7]</sup>



1422-9

Write Cycle No. 2 ( $\overline{CS}$  Controlled)<sup>[7]</sup>



Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

1422-10

### Truth Table

| $\overline{CS}$ | $\overline{WE}$ | $\overline{OE}$ | Input/Outputs | Mode                |
|-----------------|-----------------|-----------------|---------------|---------------------|
| H               | X               | X               | High Z        | Deselect Power Down |
| L               | H               | L               | Data Out      | Read                |
| L               | L               | X               | Data In       | Write               |
| L               | H               | H               | High Z        | Deselect            |

### Ordering Information

| Speed | Ordering Code | Package Type | Operating Range |
|-------|---------------|--------------|-----------------|
| 25    | M1422PS-30C   | PS03         | Commercial      |
|       | M1422LPS-30C  | PS03         |                 |
| 35    | M1422PS-35C   | PS03         |                 |
|       | M1422LPS-35C  | PS03         |                 |
| 45    | M1422PS-45C   | PS03         |                 |
|       | M1422LPS-45C  | PS03         |                 |
| 55    | M1422PS-55C   | PS03         |                 |
|       | M1422LPS-55C  | PS03         |                 |

Document #: 38-M-00003



**512K x 8 Static RAM  
Module**

**Features**

- High-density 4 Megabit SRAM Module
- High speed CMOS SRAMs
  - Access time – 45 ns
- Low active power – 2.5 W (max)
- Double-sided SMD Technology
- TTL compatible inputs and outputs
- Low profile version (PF)
  - Max. height – .315 in.
- Small footprint SIP version (PS)
  - PCB layout area – 1.5 sq in.

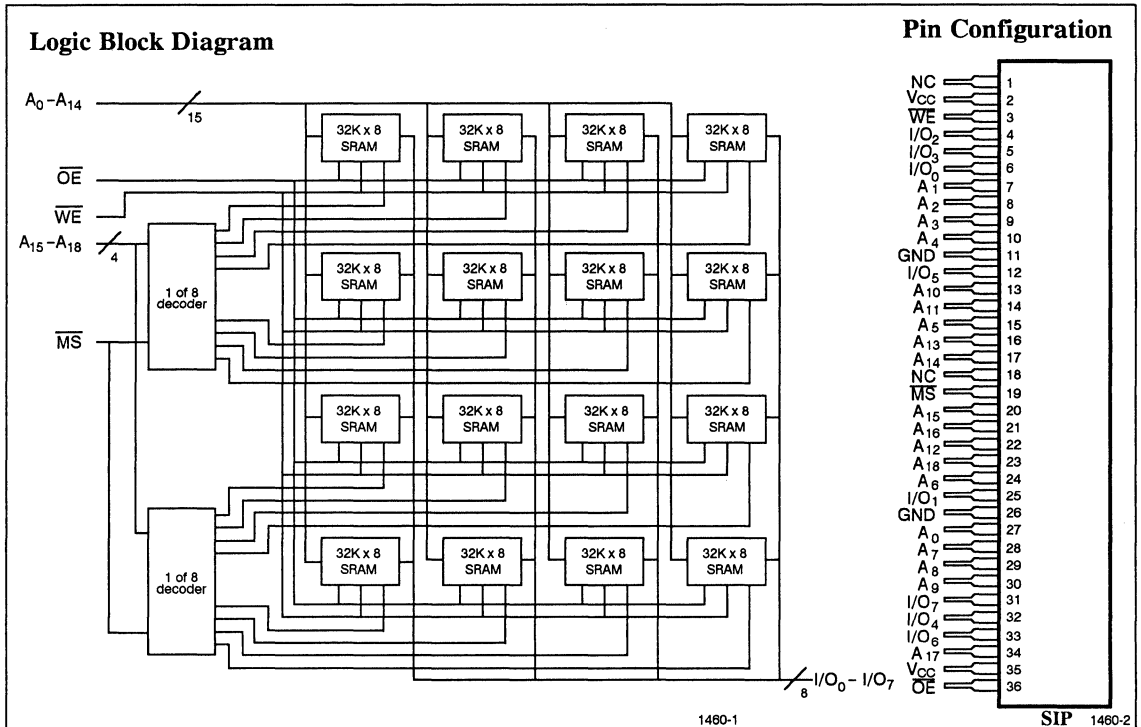
**Functional Description**

The CYM1460 is a high performance 4-Megabit Static RAM module organized as 512K words by 8 bits. This module is constructed from sixteen 32K x 8 SRAMs in plastic surface mount packages on an epoxy laminate board with pins. Two choices of pins are available for vertical (PS) or horizontal (PF) through-hole mounting. On-board decoding selects one of the sixteen SRAMs from the high order address lines keeping the remaining fifteen devices in standby mode for minimum power consumption.

An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of

the memory. When  $\overline{MS}$  and  $\overline{WE}$  inputs are both LOW, data on the eight data input/output pins is written into the memory location specified on the address pins. Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{MS}$  and  $\overline{OE}$  active LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the content of the location addressed by the information on the address pins is present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the module is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH.



**Selection Guide**

|                                | <b>1460PS-45<br/>1460PF-45</b> | <b>1460PS-55<br/>1460PF-55</b> | <b>1460PS-70<br/>1460PF-70</b> |
|--------------------------------|--------------------------------|--------------------------------|--------------------------------|
| Maximum Access time (ns)       | 45                             | 55                             | 70                             |
| Maximum Operating Current (mA) | 450                            | 450                            | 450                            |
| Maximum Standby Current (mA)   | 320                            | 320                            | 320                            |

## Maximum Ratings

(Above which the useful life may be impaired)

|   |                 |
|---|-----------------|
| Storage Temperature .....                           | -65°C to +150°C |
| Ambient Temperature with Power Applied .....        | 0°C to +70°C    |
| Supply Voltage to Ground Potential .....            | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State ..... | -0.5V to +7.0V  |
| DC Input Voltage .....                              | -0.5V to +7.0V  |

Output Current into Outputs (Low) ..... 20 mA

## Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C        | 5V ± 10%        |

## Electrical Characteristics Over Operating Range

| Parameters       | Description                                  | Test Conditions  | CYM1460 |                 | Units |
|------------------|--|--|---------|-----------------|-------|
|                  |  |  | Min.    | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA  | 2.4     |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA   |         | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                           |  | 2.2     | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage                            |  | -0.5    | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current                           | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -20     | +20             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                       | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub><br>Output Disabled  | -20     | +20             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>  | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND   |         | -300            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current     | V <sub>CC</sub> = Max., $\overline{MS} \leq V_{IL}$<br>I <sub>OUT</sub> = 0 mA   |         | 450             | mA    |
| I <sub>SB1</sub> | Automatic $\overline{MS}$ Power Down Current | Max. V <sub>CC</sub> , $\overline{MS} \geq V_{IH}$ ,<br>Min. Duty Cycle = 100%   |         | 320             | mA    |
| I <sub>SB2</sub> | Automatic $\overline{MS}$ Power Down Current | Max. V <sub>CC</sub> , $\overline{MS} \geq V_{CC} - 0.3V$ ,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V |         | 320             | mA    |

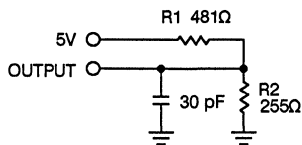
## Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Unit |
|------------------|--------------------|--|------|------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 100  | pF   |
| C <sub>OUT</sub> | Output Capacitance |  | 125  |      |

### Notes:

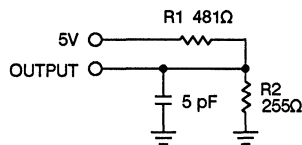
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested on a sample basis.

## AC Test Loads and Waveforms



INCLUDING  
JIG AND  
SCOPE

Figure 1a



INCLUDING  
JIG AND  
SCOPE

Figure 1b

1460-3

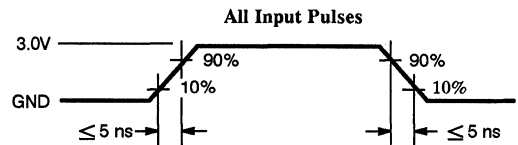
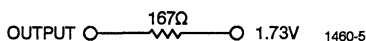


Figure 2

1460-4

Equivalent to: THEVENIN EQUIVALENT



1460-5

Switching Characteristics Over Operating Range <sup>[3]</sup>

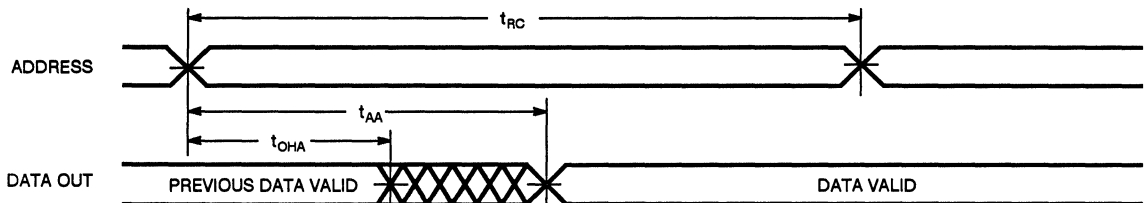
| Parameters                        | Description                                     | 1460PS-45<br>1460PF-45 |      | 1460PS-55<br>1460PF-55 |      | 1460PS-70<br>1460PF-70 |      | Units |
|-----------------------------------|---|------------------------|------|------------------------|------|------------------------|------|-------|
|                                   |   | Min.                   | Max. | Min.                   | Max. | Min.                   | Max. |       |
| <b>READ CYCLE</b>                 |   |                        |      |                        |      |                        |      |       |
| t <sub>RC</sub>                   | Read Cycle Time                                 | 45                     |      | 55                     |      | 70                     |      | ns    |
| t <sub>AA</sub>                   | Address to Data Valid                           |                        | 45   |                        | 55   |                        | 70   | ns    |
| t <sub>OHA</sub>                  | Data Hold from Address Change                   | 5                      |      | 5                      |      | 5                      |      | ns    |
| t <sub>AMS</sub>                  | $\overline{MS}$ LOW to Data Valid               |                        | 45   |                        | 55   |                        | 70   | ns    |
| t <sub>DOE</sub>                  | $\overline{OE}$ LOW to Data Valid               |                        | 20   |                        | 25   |                        | 30   | ns    |
| t <sub>LZOE</sub>                 | $\overline{OE}$ LOW to Low Z                    | 0                      |      | 0                      |      | 0                      |      | ns    |
| t <sub>HZOE</sub>                 | $\overline{OE}$ HIGH to High Z <sup>[4]</sup>   |                        | 25   |                        | 25   |                        | 30   | ns    |
| t <sub>LZMS</sub>                 | $\overline{MS}$ LOW to Low Z <sup>[5]</sup>     | 5                      |      | 5                      |      | 5                      |      | ns    |
| t <sub>HZMS</sub>                 | $\overline{MS}$ HIGH to High Z <sup>[4,5]</sup> |                        | 25   |                        | 30   |                        | 35   | ns    |
| t <sub>PU</sub>                   | $\overline{MS}$ LOW to Power Up                 | 0                      |      | 0                      |      | 0                      |      | ns    |
| t <sub>PD</sub>                   | $\overline{MS}$ HIGH to Power Down              |                        | 45   |                        | 55   |                        | 70   | ns    |
| <b>WRITE CYCLE</b> <sup>[6]</sup> |   |                        |      |                        |      |                        |      |       |
| t <sub>WC</sub>                   | Write Cycle Time                                | 45                     |      | 55                     |      | 70                     |      | ns    |
| t <sub>SMS</sub>                  | $\overline{MS}$ LOW to Write End                | 40                     |      | 50                     |      | 60                     |      | ns    |
| t <sub>AW</sub>                   | Address Set-up to Write End                     | 40                     |      | 50                     |      | 60                     |      | ns    |
| t <sub>HA</sub>                   | Address Hold from Write End                     | 5                      |      | 5                      |      | 5                      |      | ns    |
| t <sub>SA</sub>                   | Address Set-up to Write Start                   | 5                      |      | 5                      |      | 5                      |      | ns    |
| t <sub>PWE</sub>                  | $\overline{WE}$ Pulse Width                     | 35                     |      | 45                     |      | 55                     |      | ns    |
| t <sub>SD</sub>                   | Data Set-up to Write End                        | 20                     |      | 25                     |      | 30                     |      | ns    |
| t <sub>HD</sub>                   | Data Hold from Write End                        | 5                      |      | 5                      |      | 5                      |      | ns    |
| t <sub>HZWE</sub>                 | $\overline{WE}$ LOW to High Z <sup>[4]</sup>    |                        | 15   |                        | 20   |                        | 25   | ns    |
| t <sub>LZWE</sub>                 | $\overline{WE}$ HIGH to Low Z                   | 3                      |      | 5                      |      | 5                      |      | ns    |

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZMS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZMS</sub> is less than t<sub>LZMS</sub> for any given device. These parameters are guaranteed and not 100% tested.
- The internal write time of the memory is defined by the overlap of  $\overline{MS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected.  $\overline{OE}$ ,  $\overline{MS}$  = V<sub>IL</sub>.
- Address valid prior to or coincident with  $\overline{MS}$  transition LOW.
- Data I/O is HIGH impedance if  $\overline{OE}$  = V<sub>IH</sub>.

Switching Waveforms

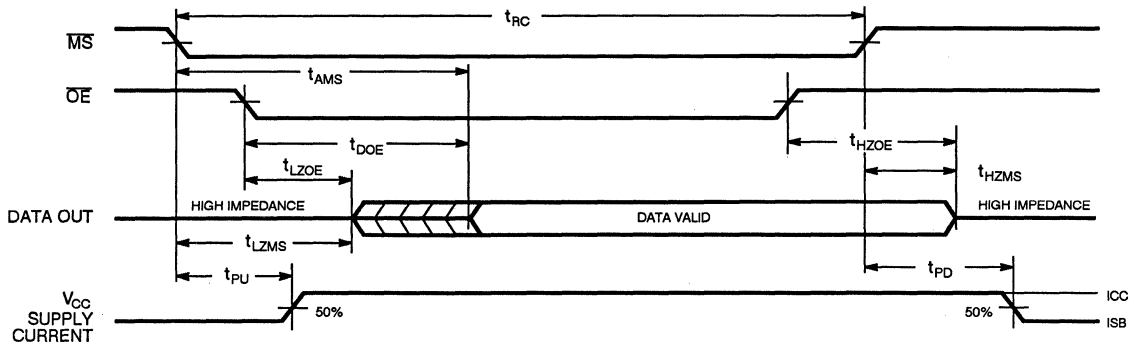
Read Cycle No. 1<sup>[8,9]</sup>





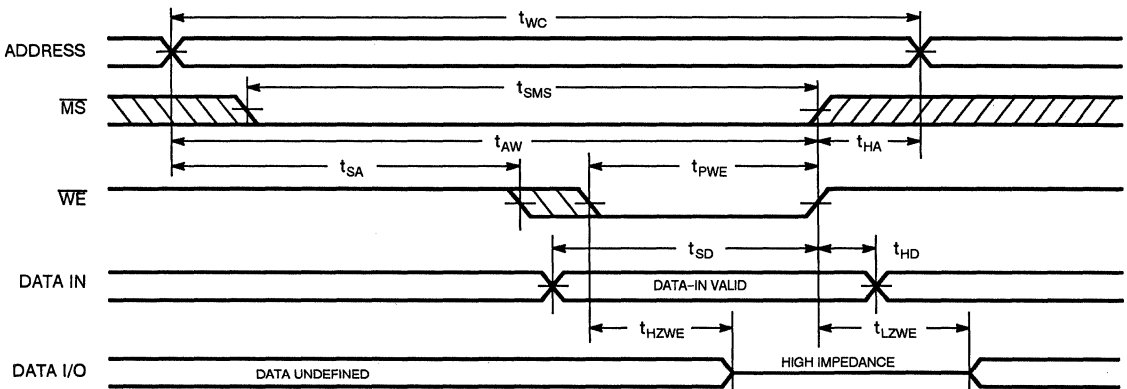
Switching Waveforms (Continued)

Read Cycle No. 2<sup>[7, 9]</sup>



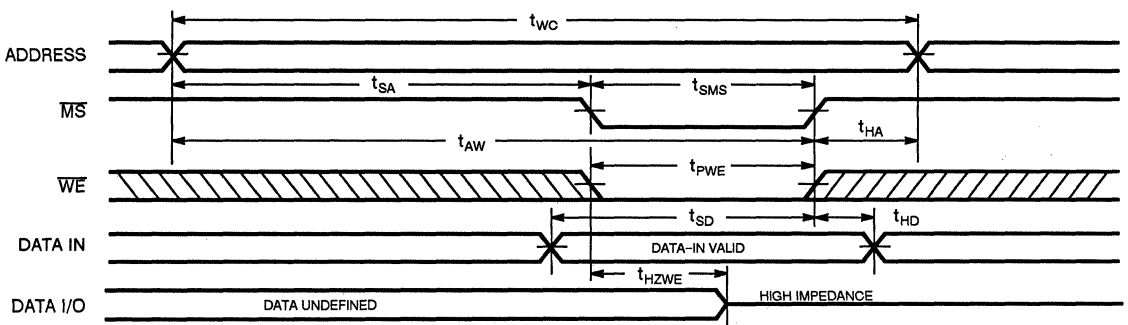
1460-7

Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[6, 10]</sup>



1460-8

Write Cycle No. 2 ( $\overline{MS}$  Controlled)<sup>[6, 10]</sup>



Note: If  $\overline{MS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

1460-9

**Truth Table**

| MS | WE | OE | Input/Outputs | Mode                |
|----|----|----|---------------|---------------------|
| H  | X  | X  | High Z        | Deselect Power Down |
| L  | H  | L  | Data Out      | Read                |
| L  | L  | X  | Data In       | Write               |
| L  | H  | H  | High Z        | Deselect            |

Document #: 38-M-00004

**Ordering Information**

| Speed | Ordering Code                  | Package Type | Operating Range |
|-------|--------------------------------|--------------|-----------------|
| 45    | CYM1460PS-45C<br>CYM1460PF-45C | PS01<br>PF01 | Commercial      |
| 55    | CYM1460PS-55C<br>CYM1460PF-55C | PS01<br>PF01 | Commercial      |
| 70    | CYM1460PS-70C<br>CYM1460PF-70C | PS01<br>PF01 | Commercial      |



# 512K x 8 Static RAM Module

## Features

- High-density 4 Megabit SRAM Module
- High speed CMOS SRAMs
  - Access time - 70 ns
- Low active power - 660 mW (max)
- Double-sided SMD Technology
- TTL compatible inputs and outputs
- Low profile version (PF)
  - Max. height - .315 in.
- Small footprint SIP version (PS)
  - PCB layout area - 1.5 sq in.

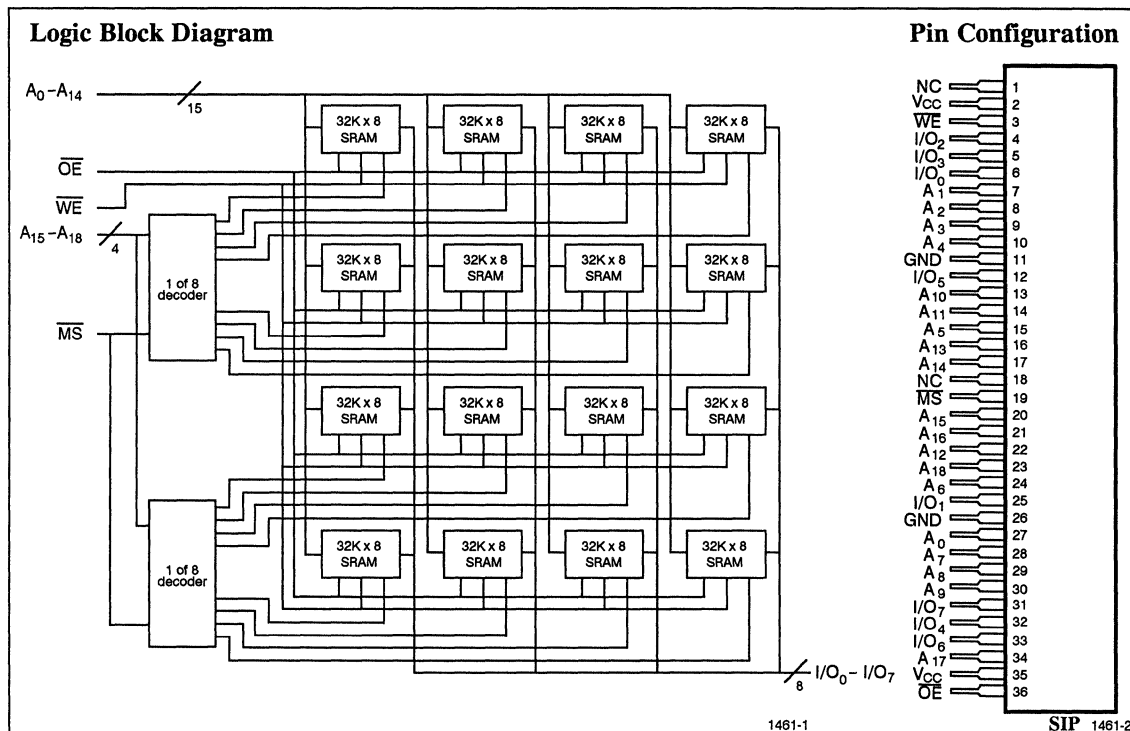
## Functional Description

The CYM1461 is a high performance 4-Megabit Static RAM module organized as 512K words by 8 bits. This module is constructed from sixteen 32K x 8 SRAMs in plastic surface mount packages on an epoxy laminate board with pins. Two choices of pins are available for vertical (PS) or horizontal (PF) through-hole mounting. On-board decoding selects one of the sixteen SRAMs from the high order address lines keeping the remaining fifteen devices in standby mode for minimum power consumption.

An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of

the memory. When  $\overline{MS}$  and  $\overline{WE}$  inputs are both LOW, data on the eight data input/output pins is written into the memory location specified on the address pins. Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{MS}$  and  $\overline{OE}$  active LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the content of the location addressed by the information on the address pins is present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the module is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH.



## Selection Guide

|                                | 1461PS-70<br>1461PF-70 | 1461PS-85<br>1461PF-85 | 1461PS-100<br>1461PF-100 |
|--------------------------------|------------------------|------------------------|--------------------------|
| Maximum Access time (ns)       | 70                     | 85                     | 100                      |
| Maximum Operating Current (mA) | 120                    | 120                    | 120                      |
| Maximum Standby Current (mA)   | 32                     | 32                     | 32                       |

## Maximum Ratings

(Above which the useful life may be impaired)

|   |                 |
|---|-----------------|
| Storage Temperature .....                           | -65°C to +150°C |
| Ambient Temperature with Power Applied .....        | 0°C to +70°C    |
| Supply Voltage to Ground Potential .....            | -0.3V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State ..... | -0.3V to +7.0V  |
| DC Input Voltage .....                              | -0.3V to +7.0V  |
| Output Current into Outputs (Low) .....             | 20 mA           |

## Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C        | 5V ± 10%        |

2

## Electrical Characteristics Over Operating Range

| Parameters       | Description                                  | Test Conditions  | CYM1461 |                       | Units |
|------------------|--|--|---------|-----------------------|-------|
|                  |  |  | Min.    | Max.                  |       |
| V <sub>OH</sub>  | Output HIGH Voltage                          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -1.0 mA  | 2.4     |                       | V     |
| V <sub>OL</sub>  | Output LOW Voltage                           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 2.0 mA   |         | 0.4                   | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                           |  | 2.2     | V <sub>CC</sub> + 0.3 | V     |
| V <sub>IL</sub>  | Input LOW Voltage                            |  | -0.3    | 0.8                   | V     |
| I <sub>IX</sub>  | Input Load Current                           | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -20     | +20                   | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                       | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub><br>Output Disabled  | -20     | +20                   | μA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current     | V <sub>CC</sub> = Max., $\overline{MS} \leq V_{IL}$<br>I <sub>OUT</sub> = 0 mA   |         | 120                   | mA    |
| I <sub>SB1</sub> | Automatic $\overline{MS}$ Power Down Current | Max. V <sub>CC</sub> , $\overline{MS} \geq V_{IH}$ ,<br>Min. Duty Cycle = 100%   |         | 50                    | mA    |
| I <sub>SB2</sub> | Automatic $\overline{MS}$ Power Down Current | Max. V <sub>CC</sub> , $\overline{MS} \geq V_{CC} - 0.3V$ ,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V |         | 32                    | mA    |

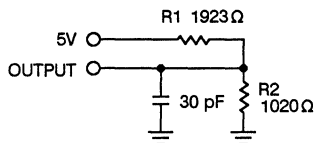
## Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 100  | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 125  |       |

### Notes:

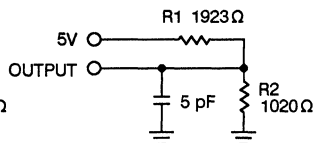
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested on a sample basis.

## AC Test Loads and Waveforms



INCLUDING  
JIG AND  
SCOPE

Figure 1a



INCLUDING  
JIG AND  
SCOPE

Figure 1b

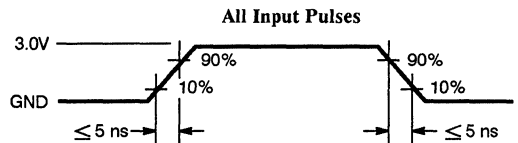
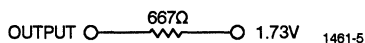


Figure 2

Equivalent to: THEVENIN EQUIVALENT



### Switching Characteristics Over Operating Range <sup>[3]</sup>

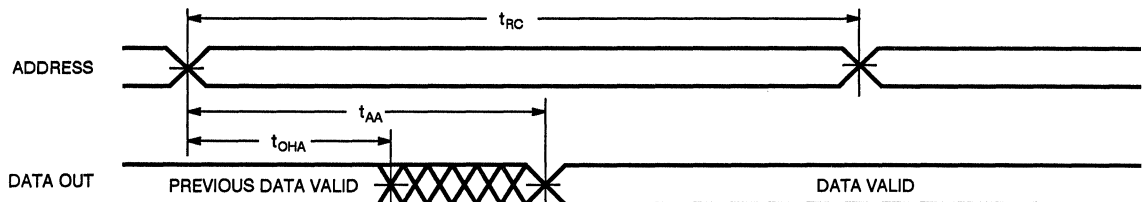
| Parameters                       | Description                                      | 1461PS-70<br>1461PF-70 |      | 1461PS-85<br>1461PF-85 |      | 1461PS-100<br>1461PF-100 |      | Units |
|----------------------------------|--|------------------------|------|------------------------|------|--------------------------|------|-------|
|                                  |  | Min.                   | Max. | Min.                   | Max. | Min.                     | Max. |       |
| <b>READ CYCLE</b>                |  |                        |      |                        |      |                          |      |       |
| t <sub>RC</sub>                  | Read Cycle Time                                  | 70                     |      | 85                     |      | 100                      |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid                            |                        | 70   |                        | 85   |                          | 100  | ns    |
| t <sub>OHA</sub>                 | Data Hold from Address Change                    | 20                     |      | 20                     |      | 20                       |      | ns    |
| t <sub>AMS</sub>                 | $\overline{MS}$ LOW to Data Valid                |                        | 70   |                        | 85   |                          | 100  | ns    |
| t <sub>DOE</sub>                 | $\overline{OE}$ LOW to Data Valid                |                        | 40   |                        | 50   |                          | 55   | ns    |
| t <sub>LZOE</sub>                | $\overline{OE}$ LOW to Low Z                     | 5                      |      | 5                      |      | 5                        |      | ns    |
| t <sub>HZOE</sub>                | $\overline{OE}$ HIGH to High Z <sup>[4]</sup>    |                        | 35   |                        | 35   |                          | 40   | ns    |
| t <sub>LZMS</sub>                | $\overline{MS}$ LOW to Low Z <sup>[5]</sup>      | 5                      |      | 5                      |      | 5                        |      | ns    |
| t <sub>HZMS</sub>                | $\overline{MS}$ HIGH to High Z <sup>[4, 5]</sup> |                        | 35   |                        | 35   |                          | 40   | ns    |
| <b>WRITE CYCLE<sup>[6]</sup></b> |  |                        |      |                        |      |                          |      |       |
| t <sub>WC</sub>                  | Write Cycle Time                                 | 70                     |      | 85                     |      | 100                      |      | ns    |
| t <sub>SMS</sub>                 | $\overline{MS}$ LOW to Write End                 | 70                     |      | 80                     |      | 85                       |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End                      | 70                     |      | 80                     |      | 85                       |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End                      | 5                      |      | 5                      |      | 5                        |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                    | 5                      |      | 5                      |      | 5                        |      | ns    |
| t <sub>PWE</sub>                 | WE Pulse Width                                   | 60                     |      | 65                     |      | 65                       |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End                         | 35                     |      | 40                     |      | 45                       |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End                         | 5                      |      | 5                      |      | 5                        |      | ns    |
| t <sub>HZWE</sub>                | WE LOW to High Z <sup>[4]</sup>                  |                        | 30   |                        | 35   |                          | 40   | ns    |
| t <sub>LZWE</sub>                | WE HIGH to Low Z                                 | 5                      |      | 5                      |      | 5                        |      | ns    |

**Notes:**

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZMS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZMS</sub> is less than t<sub>LZMS</sub> for any given device. These parameters are guaranteed and not 100% tested.
- The internal write time of the memory is defined by the overlap of  $\overline{MS}$  LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected.  $\overline{OE}, \overline{MS} = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{MS}$  transition LOW.
- Data I/O is HIGH impedance if  $\overline{OE} = V_{IH}$ .

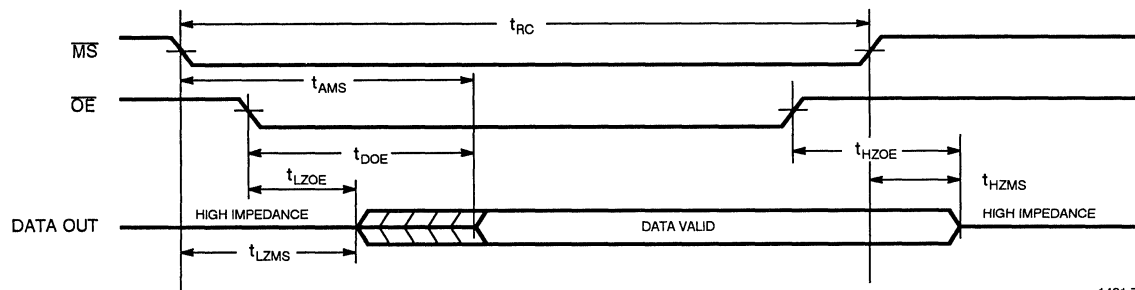
### Switching Waveforms

Read Cycle No. 1<sup>[8, 9]</sup>



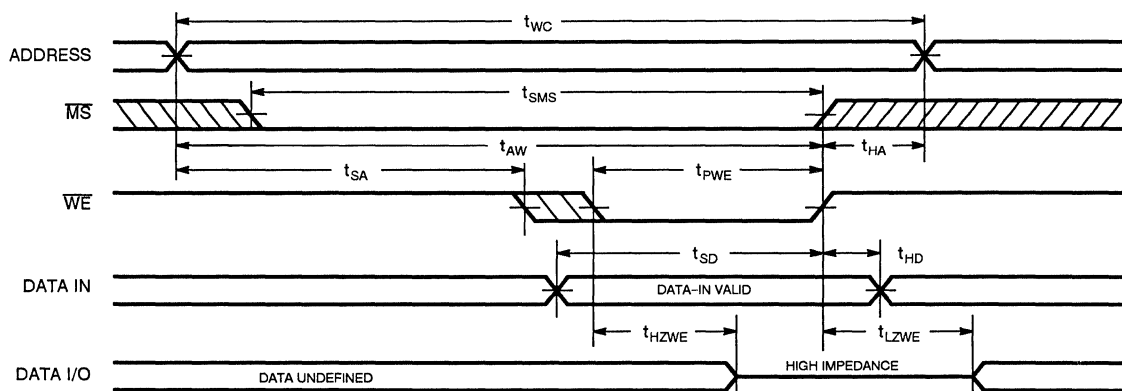
Switching Waveforms (Continued)

Read Cycle No. 2<sup>[7,9]</sup>



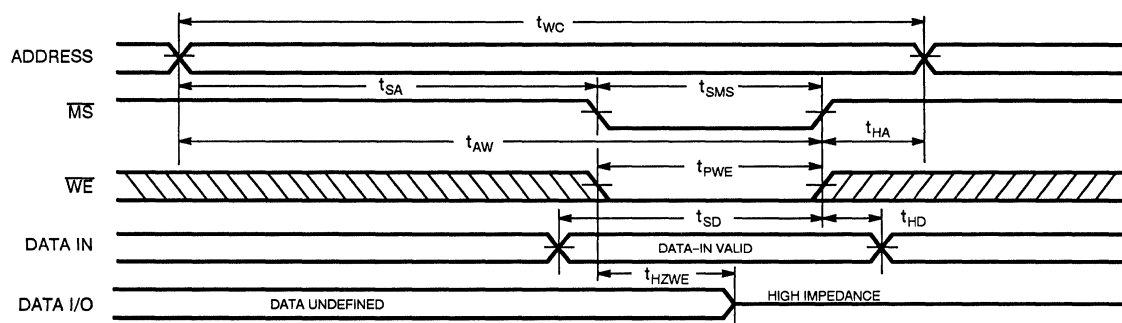
1461-7

Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[6,10]</sup>



1461-8

Write Cycle No. 2 ( $\overline{MS}$  Controlled)<sup>[6,10]</sup>



1461-9

Note: If  $\overline{MS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

### Truth Table

| $\overline{MS}$ | $\overline{WE}$ | $\overline{OE}$ | Input/Outputs | Mode                |
|-----------------|-----------------|-----------------|---------------|---------------------|
| H               | X               | X               | High Z        | Deselect Power Down |
| L               | H               | L               | Data Out      | Read                |
| L               | L               | X               | Data In       | Write               |
| L               | H               | H               | High Z        | Deselect            |

Document #: 38-M-00005

### Ordering Information

| Speed | Ordering Code                    | Package Type | Operating Range |
|-------|----------------------------------|--------------|-----------------|
| 70    | CYM1461PS-70C<br>CYM1461PF-70C   | PS01<br>PF01 | Commercial      |
| 85    | CYM1461PS-85C<br>CYM1461PF-85C   | PS01<br>PF01 | Commercial      |
| 100   | CYM1461PS-100C<br>CYM1461PF-100C | PS01<br>PF01 | Commercial      |



**Features**

- High-density 256K bit SRAM Module
- High speed CMOS SRAMs
  - Access times – 25 ns
- Low active power – 1.8 W (max)
- Hermetic SMD Technology
- TTL compatible inputs and outputs
- Low profile
  - Max. height – .215 in.
- Small PCB footprint – 1.2 sq in.
- JEDEC defined pinout
- Independent byte select
- 2 V data retention (L version)

**Functional Description**

The CYM1610 is a high performance 256K-bit Static RAM module organized as 16K words by 16 bits. This module is constructed from four 16K x 4 SRAMs in Leadless Chip Carriers mounted on a ceramic substrate with pins.

Selecting the device is achieved by a chip select input pin as well as two byte select pins ( $\overline{UB}$ ,  $\overline{LB}$ ) for independently selecting upper or lower byte for read or write operations.

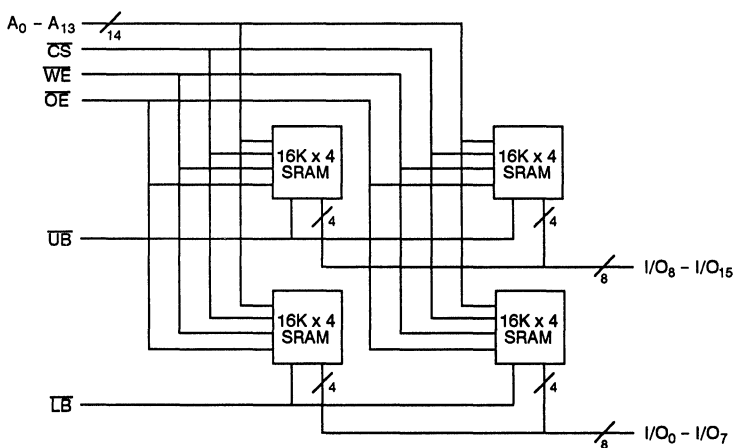
Writing to the memory module is accomplished when the chip select ( $\overline{CS}$ ), byte select ( $\overline{UB}$ ,  $\overline{LB}$ ) and write enable ( $\overline{WE}$ ) inputs are LOW. Data on the

input/output pins of the selected byte ( $I/O_8 - I/O_{15}$ ,  $I/O_0 - I/O_7$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{13}$ ).

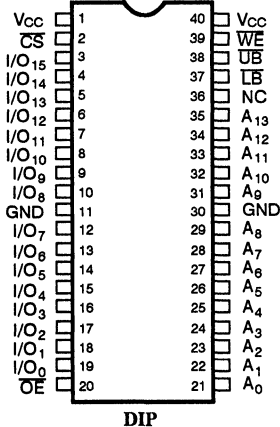
Reading the device is accomplished by taking chip select ( $\overline{CS}$ ), byte select ( $\overline{UB}$ ,  $\overline{LB}$ ) and output enable ( $\overline{OE}$ ) LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

The input/output pins remain in a high impedance state when chip select ( $\overline{CS}$ ), byte select ( $\overline{UB}$ ,  $\overline{LB}$ ) or output enable ( $\overline{OE}$ ) is HIGH, or write enable ( $\overline{WE}$ ) is LOW.

**Logic Block Diagram**



**Pin Configuration**



1610-1

1610-2

**Selection Guide**

|                                |            | 1610HD-25 | 1610HD-35 | 1610HD-45 | 1610HD-50 |
|--------------------------------|------------|-----------|-----------|-----------|-----------|
| Maximum Access time (ns)       |            | 25        | 35        | 45        | 50        |
| Maximum Operating Current (mA) | Commercial | 330       | 330       | 330       | 330       |
|                                | Military   |           | 330       | 330       | 330       |
| Maximum Standby Current (mA)   | Commercial | 80        | 80        | 80        | 80        |
|                                | Military   |           | 80        | 80        | 80        |



## Maximum Ratings

(Above which the useful life may be impaired)

|   |                 |
|---|-----------------|
| Storage Temperature .....                           | -65°C to +150°C |
| Ambient Temperature with Power Applied .....        | -55°C to +125°C |
| Supply Voltage to Ground Potential .....            | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State ..... | -0.5V to +7.0V  |
| DC Input Voltage .....                              | -3.0V to +7.0V  |
| Output Current into Outputs (Low) .....             | 20 mA           |

Static Discharge Voltage ..... >2001V  
(Per MIL-STD-883 Method 3015.2)

Latch-up Current ..... >200 mA

## Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C        | 5V ± 10%        |
| Military   | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over Operating Range

| Parameters         | Description                                    | Test Conditions  | CYM1610HD |                 | Units |
|--------------------|--|--|-----------|-----------------|-------|
|                    |  |  | Min.      | Max.            |       |
| V <sub>OH</sub>    | Output HIGH Voltage                            | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA  | 2.4       |                 | V     |
| V <sub>OL</sub>    | Output LOW Voltage                             | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA   |           | 0.4             | V     |
| V <sub>IH</sub>    | Input HIGH Voltage                             |  | 2.2       | V <sub>CC</sub> | V     |
| V <sub>IL</sub>    | Input LOW Voltage                              |  | -3.0      | 0.8             | V     |
| I <sub>IX</sub>    | Input Load Current                             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -15       | +15             | μA    |
| I <sub>OZ</sub>    | Output Leakage Current                         | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled   | -15       | +15             | μA    |
| I <sub>OS</sub>    | Output Short Circuit Current <sup>[1]</sup>    | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND   |           | -350            | mA    |
| I <sub>CCx16</sub> | V <sub>CC</sub> Operating Supply Current       | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS, UB, & LB = V <sub>IL</sub>  |           | 330             | mA    |
| I <sub>CCx8</sub>  | V <sub>CC</sub> Operating Supply Current       | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS = V <sub>IL</sub> , UB or LB = V <sub>IL</sub>                         |           | 200             | mA    |
| I <sub>SB1</sub>   | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> , CS ≥ V <sub>IH</sub> ,<br>Min. Duty Cycle = 100%  |           | 80              | mA    |
| I <sub>SB2</sub>   | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> , CS ≥ V <sub>CC</sub> - 0.3V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V |           | 80              | mA    |

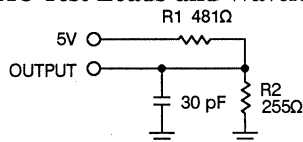
## Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions   | Max. | Units |
|------------------|--------------------|---|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 35   | pF    |
| C <sub>OUT</sub> | Output Capacitance |   | 40   |       |

### Notes:

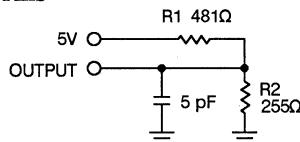
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the CE input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- Tested on a sample basis.

## AC Test Loads and Waveforms



INCLUDING  
JIG AND  
SCOPE

Figure 1a



INCLUDING  
JIG AND  
SCOPE

Figure 1b

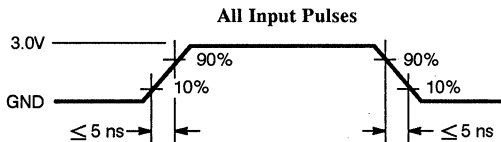
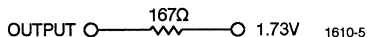


Figure 2

Equivalent to: THEVENIN EQUIVALENT



**Switching Characteristics** Over Operating Range<sup>[4]</sup>

| Parameters                       | Description                                      | 1610HD-25 |      | 1610HD-35 |      | 1610HD-45 |      | 1610HD-50 |      | Units |
|----------------------------------|--|-----------|------|-----------|------|-----------|------|-----------|------|-------|
|                                  |  | Min.      | Max. | Min.      | Max. | Min.      | Max. | Min.      | Max. |       |
| <b>READ CYCLE</b>                |  |           |      |           |      |           |      |           |      |       |
| t <sub>RC</sub>                  | Read Cycle Time                                  | 25        |      | 35        |      | 45        |      | 50        |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid                            |           | 25   |           | 35   |           | 45   |           | 50   | ns    |
| t <sub>OHA</sub>                 | Data Hold from Address Change                    | 5         |      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>ACS</sub>                 | $\overline{CS}$ LOW to Data Valid                |           | 25   |           | 35   |           | 45   |           | 50   | ns    |
| t <sub>DOE</sub>                 | $\overline{OE}$ LOW to Data Valid                |           | 15   |           | 20   |           | 25   |           | 30   | ns    |
| t <sub>LZOE</sub>                | $\overline{OE}$ LOW to LOW Z                     | 5         |      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>HZOE</sub>                | $\overline{OE}$ HIGH to HIGH Z                   |           | 15   |           | 15   |           | 15   |           | 20   | ns    |
| t <sub>LZCS</sub>                | $\overline{CS}$ LOW to Low Z <sup>[6]</sup>      | 5         |      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>HZCS</sub>                | $\overline{CS}$ HIGH to High Z <sup>[5, 6]</sup> |           | 10   |           | 15   |           | 15   |           | 20   | ns    |
| t <sub>PU</sub>                  | $\overline{CS}$ LOW to Power Up                  | 0         |      | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>PD</sub>                  | $\overline{CS}$ HIGH to Power Down               |           | 25   |           | 35   |           | 40   |           | 50   | ns    |
| <b>WRITE CYCLE<sup>[7]</sup></b> |  |           |      |           |      |           |      |           |      |       |
| t <sub>WC</sub>                  | Write Cycle Time                                 | 20        |      | 25        |      | 35        |      | 45        |      | ns    |
| t <sub>SCS</sub>                 | $\overline{CS}$ LOW to Write End                 | 22        |      | 25        |      | 35        |      | 45        |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End                      | 22        |      | 25        |      | 30        |      | 40        |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End                      | 2         |      | 2         |      | 2         |      | 2         |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                    | 2         |      | 2         |      | 2         |      | 2         |      | ns    |
| t <sub>PWE</sub>                 | $\overline{WE}$ Pulse Width                      | 20        |      | 25        |      | 30        |      | 30        |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End                         | 13        |      | 15        |      | 15        |      | 20        |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End                         | 3         |      | 3         |      | 5         |      | 5         |      | ns    |
| t <sub>LZWE</sub>                | $\overline{WE}$ HIGH to Low Z <sup>[6]</sup>     | 3         |      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>HZWE</sub>                | $\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>  | 0         | 7    | 0         | 12   | 0         | 12   | 0         | 15   | ns    |

**Notes:**

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZCS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device. These parameters are guaranteed and not 100% tested.
- The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CS} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{CS}$  transition low.
- Data I/O will be high impedance if  $\overline{OE} = V_{IH}$ .

**Data Retention Characteristics (L Version Only)**

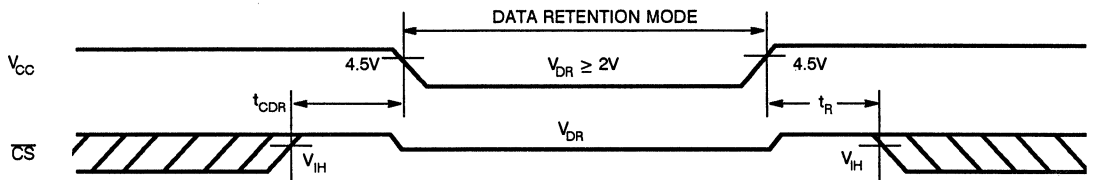
| Parameter        | Description                          | Test Conditions   | CYM1610         |      | Units   |
|------------------|--------------------------------------|---|-----------------|------|---------|
|                  |                                      |   | Min.            | Max. |         |
| $V_{DR}$         | $V_{CC}$ for Retention Data          | $V_{CC} = 2.0V$ ,<br>$\overline{CS} \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$<br>or $V_{IN} \leq 0.2V$ | 2.0             |      | V       |
| $I_{CCDR}$       | Data Retention Current               |   |                 | 4    | mA      |
| $t_{CDR}^{[13]}$ | Chip Deselect to Data Retention Time |   | 0               |      | ns      |
| $t_R^{[13]}$     | Operation Recovery Time              |   | $t_{RC}^{[12]}$ |      | ns      |
| $I_{LI}^{[13]}$  | Input Leakage Current                |   |                 | 8    | $\mu A$ |

Notes:

12.  $t_{RC}$  = Read Cycle Time.

13. Guaranteed, not tested.

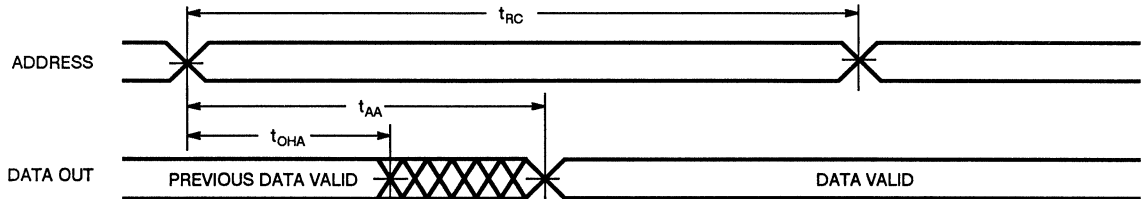
**Data Retention Waveform**



1610-6

**Switching Waveforms<sup>[10]</sup>**

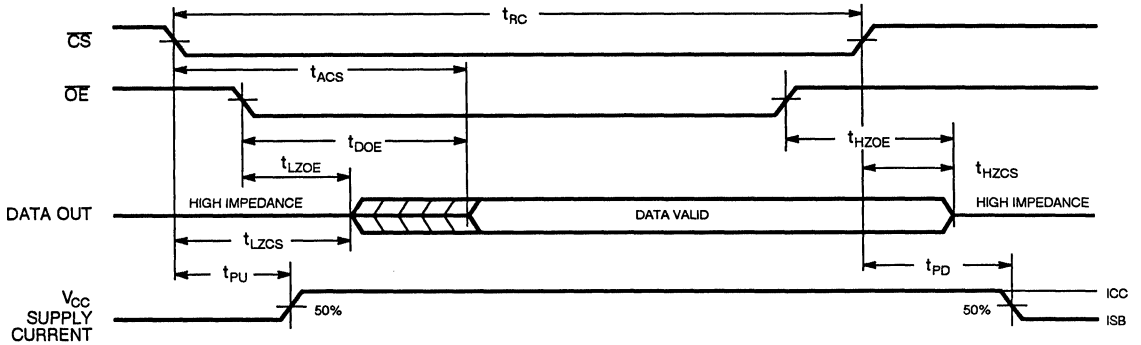
Read Cycle No. 1<sup>[7, 8]</sup>



1610-7

Switching Waveforms (Continued)

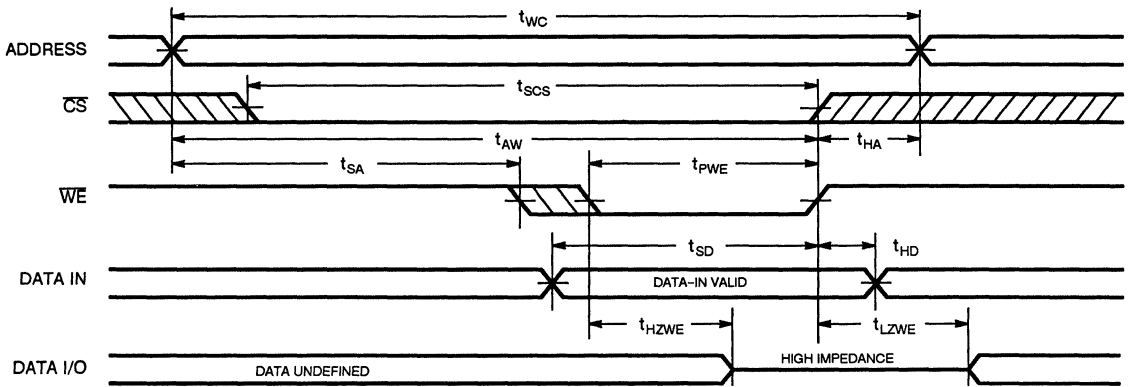
Read Cycle No. 2<sup>[8, 10]</sup>



2

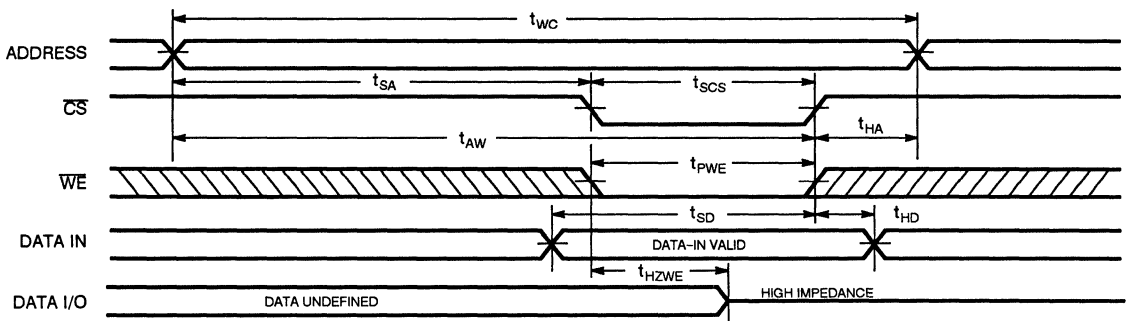
1610-8

Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[7, 11]</sup>



1610-9

Write Cycle No. 2 ( $\overline{CS}$  Controlled)<sup>[7, 11]</sup>



Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

1610-10

**Truth Table**

| CS | UB | LB | OE | WE | Input/Outputs            | Mode                |
|----|----|----|----|----|--------------------------|---------------------|
| H  | X  | X  | X  | X  | High Z                   | Deselect Power Down |
| L  | H  | H  | X  | X  | High Z                   | Deselect Power Down |
| L  | L  | L  | L  | H  | Data Out <sub>0-15</sub> | Read Word           |
| L  | H  | L  | L  | H  | Data Out <sub>0-7</sub>  | Read Lower Byte     |
| L  | L  | H  | L  | H  | Data Out <sub>8-15</sub> | Read Upper Byte     |
| L  | L  | L  | X  | L  | Data In <sub>0-15</sub>  | Write Word          |
| L  | H  | L  | X  | L  | Data In <sub>0-7</sub>   | Write Lower Byte    |
| L  | L  | H  | X  | L  | Data In <sub>8-15</sub>  | Write Upper Byte    |
| L  | L  | L  | H  | H  | High Z                   | Deselect            |
| L  | H  | L  | H  | H  | High Z                   | Deselect            |
| L  | L  | H  | H  | H  | High Z                   | Deselect            |

Document #: 38-M-00006

**Ordering Information**

| Speed | Ordering Code   | Package Type | Operating Range |
|-------|-----------------|--------------|-----------------|
| 25    | CYM1610HD-25C   | HD01         | Commercial      |
|       | CYM1610LHD-25C  | HD01         |                 |
| 35    | CYM1610HD-35C   | HD01         | Commercial      |
|       | CYM1610LHD-35C  | HD01         |                 |
|       | CYM1610HD-35MB  | HD01         | Military        |
|       | CYM1610LHD-35MB | HD01         |                 |
| 45    | CYM1610HD-45C   | HD01         | Commercial      |
|       | CYM1610LHD-45C  | HD01         |                 |
|       | CYM1610HD-45MB  | HD01         | Military        |
|       | CYM1610LHD-45MB | HD01         |                 |
| 50    | CYM1610HD-50C   | HD01         | Commercial      |
|       | CYM1610LHD-50C  | HD01         |                 |
|       | CYM1610HD-50MB  | HD01         | Military        |
|       | CYM1610LHD-50MB | HD01         |                 |



# 16K x 16 Static RAM Module

## Features

- High-density 256K bit SRAM Module
- High speed
  - Access time – 25 ns
- 16 bit wide organization
- Low active power – 1.8 W (max)
- Hermetic SMD Technology
- TTL compatible inputs and outputs
- Low profile
  - Max. height – .05 in.
- Small PCB footprint – 0.4 sq in.
- 2V data retention (L version)

## Functional Description

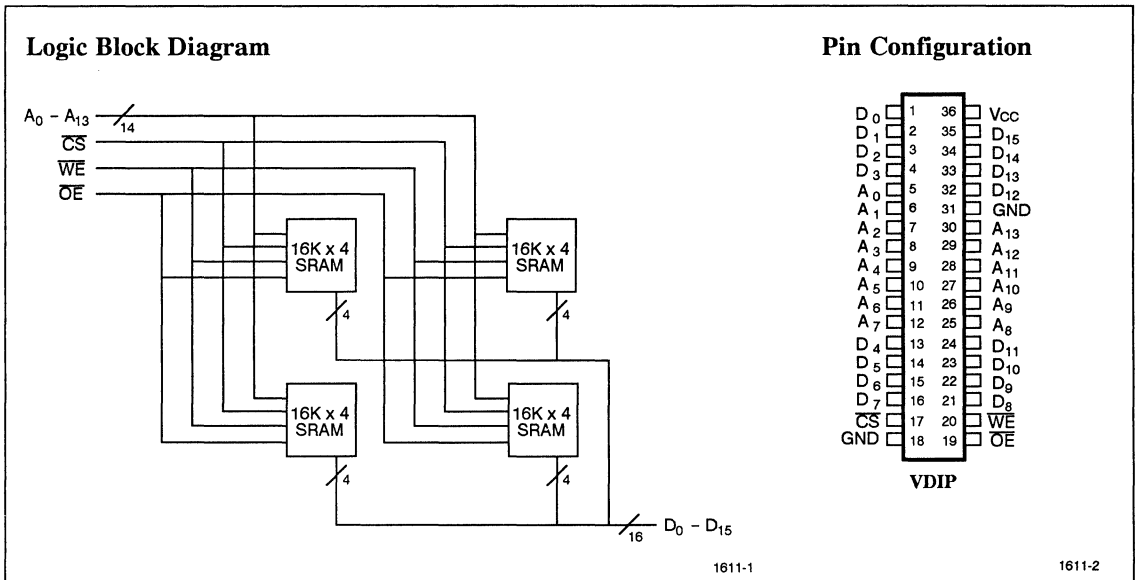
The CYM1611 is a very high performance 256K-bit Static RAM module organized as 16K words by 16 bits. The module is constructed from four 16K x 4 SRAMs in Leadless Chip Carriers mounted on a ceramic substrate with pins. A vertical DIP format minimizes board space (footprint = 0.4 sq in.) while still keeping a maximum height of 0.5 in.

Writing to the memory module is accomplished when the chip select ( $\overline{CS}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the sixteen input/output pins ( $D_0$

through  $D_{15}$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{13}$ ).

Reading the device is accomplished by taking chip select ( $\overline{CS}$ ) and output enable ( $\overline{OE}$ ) LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the sixteen data input/output pins.

The input/output pins remain in a high impedance state unless the module is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH.



## Selection Guide

|                                |            | 1611HV-25 | 1611HV-30 | 1611HV-35 | 1611HV-45 |
|--------------------------------|------------|-----------|-----------|-----------|-----------|
| Maximum Access time (ns)       |            | 25        | 30        | 35        | 45        |
| Maximum Operating Current (mA) | Commercial | 330       | 330       | 330       | 330       |
|                                | Military   |           | 330       | 330       | 330       |
| Maximum Standby Current (mA)   | Commercial | 80        | 80        | 80        | 80        |
|                                | Military   |           | 80        | 80        | 80        |

## Maximum Ratings

(Above which the useful life may be impaired)

|   |                 |
|---|-----------------|
| Storage Temperature .....                           | -65°C to +150°C |
| Ambient Temperature with Power Applied .....        | -55°C to +125°C |
| Supply Voltage to Ground Potential .....            | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State ..... | -0.5V to +7.0V  |
| DC Input Voltage .....                              | -3.0V to +7.0V  |
| Output Current into Outputs (Low) .....             | 20 mA           |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | > 2001V<br>(Per MIL-STD-883 Method 3015) |
| Latch-up Current .....         | > 200 mA                                 |

## Operating Range

| Range      | Ambient Temperature |      | V <sub>CC</sub> |
|------------|---------------------|------|-----------------|
|            | Min.                | Max. |                 |
| Commercial | 0°C to +70°C        |      | 5V ± 10%        |
| Military   | -55°C to +125°C     |      | 5V ± 10%        |

## Electrical Characteristics Over Operating Range

| Parameters       | Description                                  | Test Conditions  | CYM1611HV |                 | Units |
|------------------|--|--|-----------|-----------------|-------|
|                  |  |  | Min.      | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA  | 2.4       |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA   |           | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                           |  | 2.2       | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage                            |  | -3.0      | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current                           | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -20       | +20             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                       | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled   | -20       | +20             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>  | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND   |           | -350            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current     | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, $\overline{CS} \leq V_{IL}$   |           | 330             | mA    |
| I <sub>SB1</sub> | Automatic $\overline{CS}$ Power Down Current | Max. V <sub>CC</sub> , $\overline{CS} \geq V_{IH}$ ,<br>Min. Duty Cycle = 100%   |           | 80              | mA    |
| I <sub>SB2</sub> | Automatic $\overline{CS}$ Power Down Current | Max. V <sub>CC</sub> , $\overline{CS} \geq V_{CC} - 0.3V$ ,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V |           | 80              | mA    |

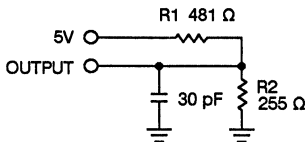
## Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 35   | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 15   |       |

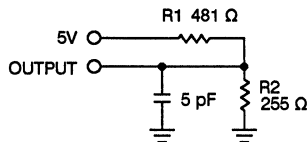
Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested on a sample basis.

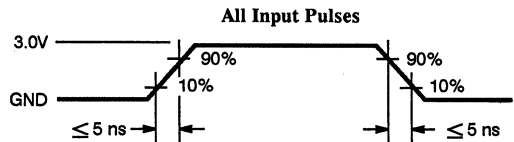
## AC Test Loads and Waveforms



INCLUDING  
JIG AND  
SCOPE  
Figure 1a

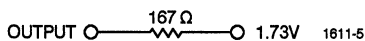


INCLUDING  
JIG AND  
SCOPE  
1611-3  
Figure 1b



1611-4  
Figure 2

Equivalent to: THEVENIN EQUIVALENT



Switching Characteristics Over Operating Range [2]

| Parameters             | Description   | 1611HV-25 |      | 1611HV-30 |      | 1611HV-35 |      | 1611HV-45 |      | Units |
|------------------------|---|-----------|------|-----------|------|-----------|------|-----------|------|-------|
|                        |   | Min.      | Max. | Min.      | Max. | Min.      | Max. | Min.      | Max. |       |
| <b>READ CYCLE</b>      |   |           |      |           |      |           |      |           |      |       |
| t <sub>RC</sub>        | Read Cycle Time   | 25        |      | 30        |      | 35        |      | 45        |      | ns    |
| t <sub>AA</sub>        | Address to Data Valid                                   |           | 25   |           | 30   |           | 35   |           | 45   | ns    |
| t <sub>OHA</sub>       | Data Hold from Address Change                           | 3         |      | 3         |      | 3         |      | 5         |      | ns    |
| t <sub>ACS</sub>       | $\overline{\text{CS}}$ LOW to Data Valid                |           | 25   |           | 30   |           | 35   |           | 45   | ns    |
| t <sub>DOE</sub>       | $\overline{\text{OE}}$ LOW to Data Valid                |           | 15   |           | 20   |           | 25   |           | 30   | ns    |
| t <sub>LZOE</sub>      | $\overline{\text{OE}}$ LOW to Low Z                     | 0         |      | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>HZOE</sub>      | $\overline{\text{OE}}$ HIGH to High Z <sup>[4]</sup>    |           | 10   |           | 15   |           | 20   |           | 20   | ns    |
| t <sub>LZCS</sub>      | $\overline{\text{CS}}$ LOW to Low Z <sup>[5]</sup>      | 5         |      | 10        |      | 10        |      | 10        |      | ns    |
| t <sub>HZCS</sub>      | $\overline{\text{CS}}$ HIGH to High Z <sup>[4, 5]</sup> |           | 10   |           | 15   |           | 15   |           | 20   | ns    |
| t <sub>PU</sub>        | $\overline{\text{CS}}$ LOW to Power Up                  | 0         |      | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>PD</sub>        | $\overline{\text{CS}}$ HIGH to Power Down               |           | 20   |           | 30   |           | 35   |           | 45   | ns    |
| <b>WRITE CYCLE</b> [6] |   |           |      |           |      |           |      |           |      |       |
| t <sub>WC</sub>        | Write Cycle Time  | 20        |      | 25        |      | 25        |      | 35        |      | ns    |
| t <sub>SCS</sub>       | $\overline{\text{CS}}$ LOW to Write End                 | 20        |      | 25        |      | 30        |      | 40        |      | ns    |
| t <sub>AW</sub>        | Address Set-up to Write End                             | 20        |      | 25        |      | 30        |      | 40        |      | ns    |
| t <sub>HA</sub>        | Address Hold from Write End                             | 2         |      | 2         |      | 2         |      | 2         |      | ns    |
| t <sub>SA</sub>        | Address Set-up to Write Start                           | 2         |      | 2         |      | 2         |      | 2         |      | ns    |
| t <sub>PWE</sub>       | $\overline{\text{WE}}$ Pulse Width                      | 20        |      | 25        |      | 25        |      | 30        |      | ns    |
| t <sub>SD</sub>        | Data Set-up to Write End                                | 13        |      | 20        |      | 20        |      | 25        |      | ns    |
| t <sub>HD</sub>        | Data Hold from Write End                                | 2         |      | 2         |      | 2         |      | 2         |      | ns    |
| t <sub>HZWE</sub>      | $\overline{\text{WE}}$ LOW to High Z <sup>[4]</sup>     | 0         | 7    | 0         | 12   | 0         | 12   | 0         | 15   | ns    |
| t <sub>LZWE</sub>      | $\overline{\text{WE}}$ HIGH to Low Z                    | 3         |      | 5         |      | 5         |      | 5         |      | ns    |

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device. These parameters are guaranteed and not 100% tested.

6. The internal write time of the memory is defined by the overlap of  $\overline{\text{CS}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

7.  $\overline{\text{WE}}$  is HIGH for read cycle.

8. Device is continuously selected.  $\overline{\text{OE}}, \overline{\text{CS}} = V_{IL}$

9. Address valid prior to or coincident with  $\overline{\text{CS}}$  transition LOW.

10. Data I/O is HIGH impedance if  $\overline{\text{OE}} = V_{IH}$ .



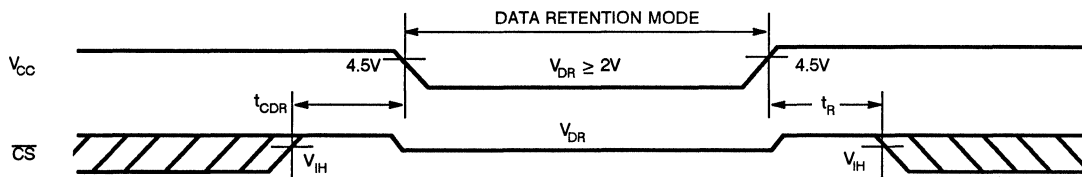
### Data Retention Characteristics (L Version Only)

| Parameter  | Description                          | Test Conditions  | CYM1611         |      | Units   |
|------------|--------------------------------------|--|-----------------|------|---------|
|            |                                      |  | Min.            | Max. |         |
| $V_{DR}$   | $V_{CC}$ for Retention of Data       | $V_{CC} = 2.0V,$<br>$\overline{CS} \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$<br>or $V_{IN} \leq 0.2V$ | 2.0             |      | V       |
| $I_{CCDR}$ | Data Retention Current               |  |                 | 4    | mA      |
| $t_{CDR}$  | Chip Deselect to Data Retention Time |  | 0               |      | ns      |
| $t_R$      | Operation Recovery Time              |  | $t_{RC}^{(11)}$ |      | ns      |
| $I_{LI}$   | Input Leakage Current                |  |                 | 5    | $\mu A$ |

Note:

11.  $t_{RC}$  = Read Cycle Time.

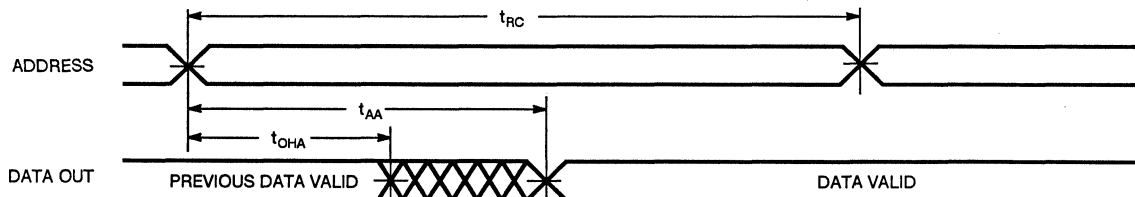
### Data Retention Waveform



1611-6

### Switching Waveforms

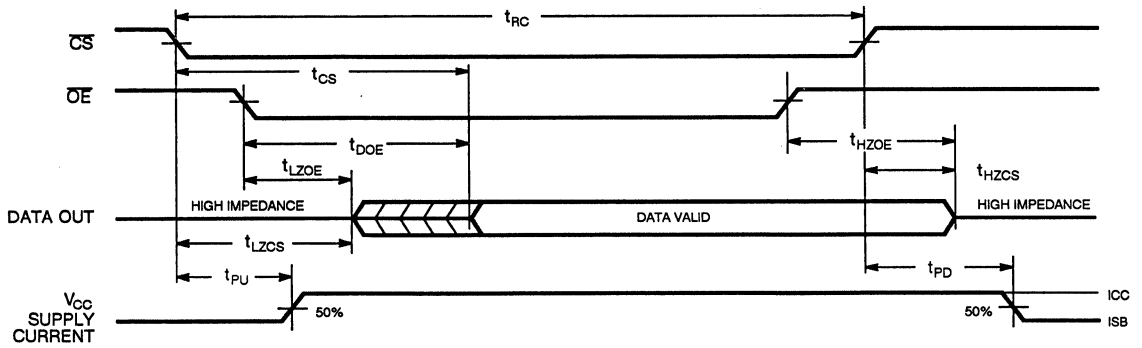
Read Cycle No. 1<sup>[7,8]</sup>



1611-7

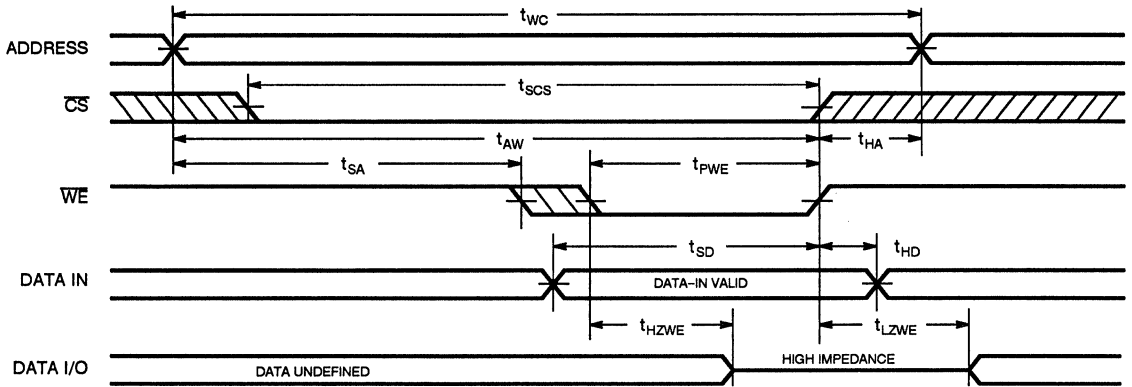
Switching Waveforms (Continued)

Read Cycle No. 2<sup>[7,9]</sup>



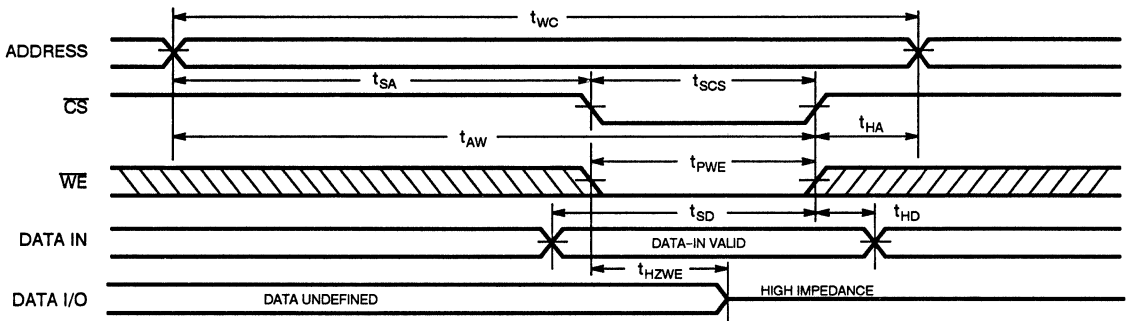
1611-8

Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[6, 10]</sup>



1611-9

Write Cycle No. 2 ( $\overline{CS}$  Controlled)<sup>[6, 10]</sup>



1611-10

Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

**Truth Table**

| $\overline{CS}$ | $\overline{WE}$ | $\overline{OE}$ | Input/Outputs | Mode                |
|-----------------|-----------------|-----------------|---------------|---------------------|
| H               | X               | X               | High Z        | Deselect Power Down |
| L               | H               | L               | Data Out      | Read                |
| L               | L               | X               | Data In       | Write               |
| L               | H               | H               | High Z        | Deselect            |

**Ordering Information**

| Speed | Ordering Code   | Package Type | Operating Range |
|-------|-----------------|--------------|-----------------|
| 25    | CYM1611HV-25C   | HV01         | Commercial      |
|       | CYM1611LHV-25C  |              |                 |
| 30    | CYM1611HV-30C   | HV01         | Commercial      |
|       | CYM1611LHV-30C  |              |                 |
|       | CYM1611HV-30MB  | HV01         | Military        |
|       | CYM1611LHV-30MB |              |                 |
| 35    | CYM1611HV-35C   | HV01         | Commercial      |
|       | CYM1611LHV-35C  |              |                 |
|       | CYM1611HV-35MB  | HV01         | Military        |
|       | CYM1611LHV-35MB |              |                 |
| 45    | CYM1611HV-45C   | HV01         | Commercial      |
|       | CYM1611LHV-45C  |              |                 |
|       | CYM1611HV-45MB  | HV01         | Military        |
|       | CYM1611LHV-45MB |              |                 |

Document #: 38-M-00007



**64K x 16 Static RAM  
Module**

**Features**

- High-density 1 Megabit SRAM Module
- High speed CMOS SRAMs  
— Access time – 45 ns
- 40 pin – 0.6 in. wide DIP package
- JEDEC compatible pin-out
- Low active power – 1.9 W (max)
- Hermetic SMD Technology
- TTL compatible inputs and outputs
- Commercial and Military Temperature Ranges
- 2 V data retention (L version)

**Functional Description**

The CYM1620 is a very high performance 1 Megabit Static RAM module organized as 64K words by 16 bits. The module is constructed using four 32K x 8 Static RAM's in Leadless Chip Carriers mounted onto a double sided multilayer ceramic substrate. A decoder is used to interpret the higher order address  $A_{16}$  and select one of the two pairs of RAMs.

Writing to the memory module is accomplished when the chip select ( $\overline{CS}$ ), byte select ( $\overline{UB}$ ,  $\overline{LB}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the input/output pins of the selected byte

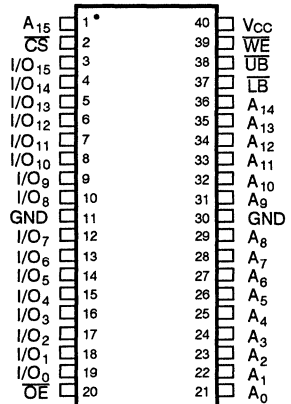
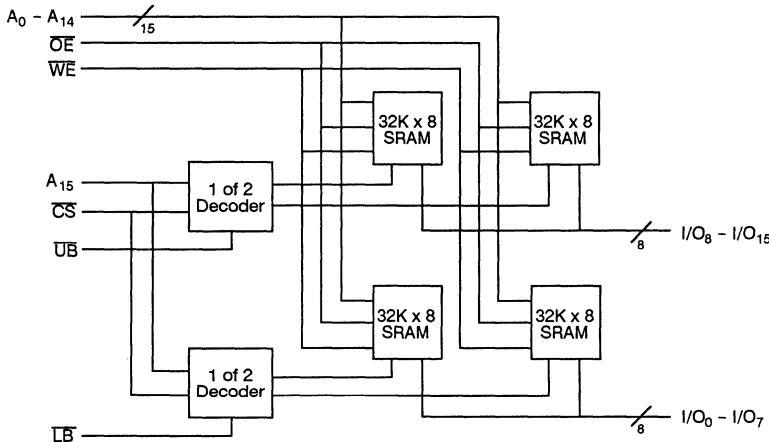
( $I/O_8 - I/O_{15}$ ,  $I/O_0 - I/O_7$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{15}$ ).

Reading the device is accomplished by taking chip select ( $\overline{CS}$ ), byte select ( $\overline{UB}$ ,  $\overline{LB}$ ) and output enable ( $\overline{OE}$ ) LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

The input/output pins remain in a high impedance state when chip select ( $\overline{CS}$ ), byte select ( $\overline{UB}$ ,  $\overline{LB}$ ) or output enable ( $\overline{OE}$ ) is HIGH, or write enable ( $\overline{WE}$ ) is LOW.

**Logic Block Diagram**

**Pin Configuration**



1620-1

1620-2

**Selection Guide**

|                                |            | 1620HD-45 | 1620HD-55 |
|--------------------------------|------------|-----------|-----------|
| Maximum Access time (ns)       |            | 45        | 55        |
| Maximum Operating Current (mA) | Commercial | 340       | 340       |
|                                | Military   | 340       | 340       |
| Maximum Standby Current (mA)   | Commercial | 80        | 80        |
|                                | Military   | 80        | 80        |

## Maximum Ratings

|  |                 |
|--|-----------------|
| Storage Temperature .....                              | -65°C to +150°C |
| Ambient Temperature with<br>Power Applied .....        | -55°C to +125°C |
| Supply Voltage to Ground Potential .....               | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs<br>in High Z State ..... | -0.5V to +7.0V  |
| DC Input Voltage .....                                 | -0.5V to +7.0V  |
| Output Current into Outputs (Low) .....                | 20 mA           |

## Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C        | 5V ± 10%        |
| Military   | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over Operating Range

| Parameters         | Description                                    | Test Conditions  | CYM1620HD |                 | Units |
|--------------------|--|--|-----------|-----------------|-------|
|                    |  |  | Min.      | Max.            |       |
| V <sub>OH</sub>    | Output HIGH Voltage                            | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA  | 2.4       |                 | V     |
| V <sub>OL</sub>    | Output LOW Voltage                             | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA   |           | 0.4             | V     |
| V <sub>IH</sub>    | Input HIGH Voltage                             |  | 2.2       | V <sub>CC</sub> | V     |
| V <sub>IL</sub>    | Input LOW Voltage                              |  | -0.5      | 0.8             | V     |
| I <sub>Ix</sub>    | Input Load Current                             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -15       | +15             | μA    |
| I <sub>OZ</sub>    | Output Leakage Current                         | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled   | -15       | +15             | μA    |
| I <sub>OS</sub>    | Output Short Circuit Current <sup>[1]</sup>    | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND   |           | -300            | mA    |
| I <sub>CCx16</sub> | V <sub>CC</sub> Operating Supply Current       | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS, UB, & LB = V <sub>IL</sub>  |           | 340             | mA    |
| I <sub>CCx8</sub>  | V <sub>CC</sub> Operating Supply Current       | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS = V <sub>IL</sub> , UB or LB = V <sub>IL</sub>                         |           | 200             | mA    |
| I <sub>SB1</sub>   | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> , CS ≥ V <sub>IH</sub> ,<br>Min. Duty Cycle = 100%  |           | 80              | mA    |
| I <sub>SB2</sub>   | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> , CS ≥ V <sub>CC</sub> - 0.3V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V |           | 80              | mA    |

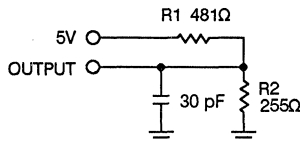
## Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions   | Max. | Units |
|------------------|--------------------|---|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 35   | pF    |
| C <sub>OUT</sub> | Output Capacitance |   | 40   |       |

### Notes:

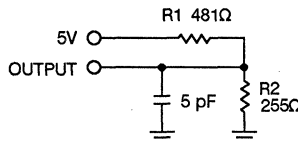
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the CS input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- Tested on a sample basis.

## AC Test Loads and Waveforms



INCLUDING  
JIG AND  
SCOPE

Figure 1a



INCLUDING  
JIG AND  
SCOPE

Figure 1b

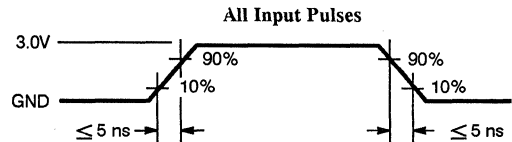
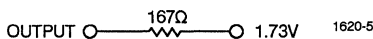


Figure 2

Equivalent to: THEVENIN EQUIVALENT



1620-5

Switching Characteristics Over Operating Range <sup>[4]</sup>

| Parameters                        | Description   | 1620HD-45 |      | 1620HD-55 |      | Units |
|-----------------------------------|---|-----------|------|-----------|------|-------|
|                                   |   | Min.      | Max. | Min.      | Max. |       |
| <b>READ CYCLE</b>                 |   |           |      |           |      |       |
| t <sub>RC</sub>                   | Read Cycle Time   | 45        |      | 55        |      | ns    |
| t <sub>AA</sub>                   | Address to Data Valid                                   |           | 45   |           | 55   | ns    |
| t <sub>OHA</sub>                  | Data Hold from Address Change                           | 5         |      | 5         |      | ns    |
| t <sub>ACS</sub>                  | $\overline{\text{CS}}$ LOW to Data Valid                |           | 45   |           | 55   | ns    |
| t <sub>DOE</sub>                  | $\overline{\text{OE}}$ LOW to Data Valid                |           | 25   |           | 30   | ns    |
| t <sub>LZOE</sub>                 | $\overline{\text{OE}}$ LOW to LOW Z                     | 5         |      | 5         |      | ns    |
| t <sub>HZOE</sub>                 | $\overline{\text{OE}}$ HIGH to HIGH Z                   |           | 20   |           | 25   | ns    |
| t <sub>LZCS</sub>                 | $\overline{\text{CS}}$ LOW to Low Z <sup>[6]</sup>      | 5         |      | 5         |      | ns    |
| t <sub>HZCS</sub>                 | $\overline{\text{CS}}$ HIGH to High Z <sup>[5, 6]</sup> |           | 20   |           | 25   | ns    |
| t <sub>PU</sub>                   | $\overline{\text{CS}}$ LOW to Power Up                  | 0         |      | 0         |      | ns    |
| t <sub>PD</sub>                   | $\overline{\text{CS}}$ HIGH to Power Down               |           | 45   |           | 55   | ns    |
| <b>WRITE CYCLE <sup>[7]</sup></b> |   |           |      |           |      |       |
| t <sub>WC</sub>                   | Write Cycle Time  | 45        |      | 55        |      | ns    |
| t <sub>SCS</sub>                  | $\overline{\text{CS}}$ LOW to Write End                 | 40        |      | 45        |      | ns    |
| t <sub>AW</sub>                   | Address Set-up to Write End                             | 40        |      | 45        |      | ns    |
| t <sub>HA</sub>                   | Address Hold from Write End                             | 5         |      | 5         |      | ns    |
| t <sub>SA</sub>                   | Address Set-up to Write Start                           | 5         |      | 5         |      | ns    |
| t <sub>PWE</sub>                  | $\overline{\text{WE}}$ Pulse Width                      | 25        |      | 30        |      | ns    |
| t <sub>SD</sub>                   | Data Set-up to Write End                                | 20        |      | 25        |      | ns    |
| t <sub>HD</sub>                   | Data Hold from Write End                                | 5         |      | 5         |      | ns    |
| t <sub>LZWE</sub>                 | $\overline{\text{WE}}$ HIGH to Low Z <sup>[6]</sup>     | 5         |      | 5         |      | ns    |
| t <sub>HZWE</sub>                 | $\overline{\text{WE}}$ LOW to High Z <sup>[5, 6]</sup>  | 0         | 15   | 0         | 25   | ns    |

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.

5. t<sub>HZCS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ±500 mV from steady state voltage.

6. At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device. These parameters are guaranteed and not 100% tested.

7. The internal write time of the memory is defined by the overlap of  $\overline{\text{CS}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

8.  $\overline{\text{WE}}$  is HIGH for read cycle.

9. Device is continuously selected,  $\overline{\text{CS}} = V_{IL}$  and  $\overline{\text{OE}} = V_{IL}$ .

10. Address valid prior to or coincident with  $\overline{\text{CS}}$  transition low.

11. Data I/O will be high impedance if  $\overline{\text{OE}} = V_{IH}$ .

### Data Retention Characteristics (L Version Only)

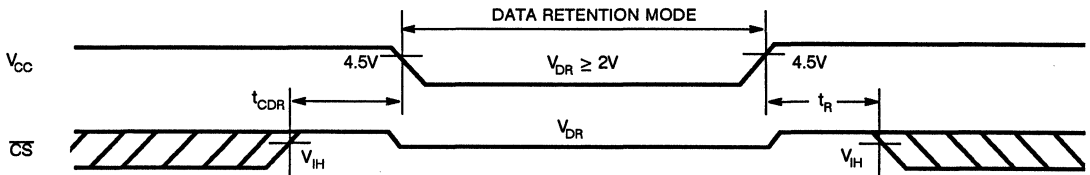
| Parameter        | Description                          | Test Conditions   | CYM1620         |      | Units   |
|------------------|--------------------------------------|---|-----------------|------|---------|
|                  |                                      |   | Min.            | Max. |         |
| $V_{DR}$         | $V_{CC}$ for Retention Data          | $V_{CC} = 2.0V$ ,<br>$\overline{CS} \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$<br>or $V_{IN} \leq 0.2V$ | 2.0             |      | V       |
| $I_{CCDR}$       | Data Retention Current               |   |                 | 16   | mA      |
| $t_{CDR}^{[13]}$ | Chip Deselect to Data Retention Time |   | 0               |      | ns      |
| $t_R^{[13]}$     | Operation Recovery Time              |   | $t_{RC}^{[12]}$ |      | ns      |
| $I_{LI}^{[13]}$  | Input Leakage Current                |   |                 | 8    | $\mu A$ |

**Notes:**

12.  $t_{RC}$  = Read Cycle Time.

13. Guaranteed, not tested.

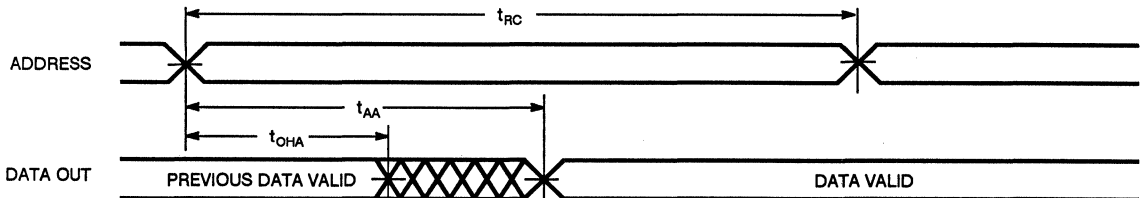
### Data Retention Waveform



1620-6

### Switching Waveforms<sup>[10]</sup>

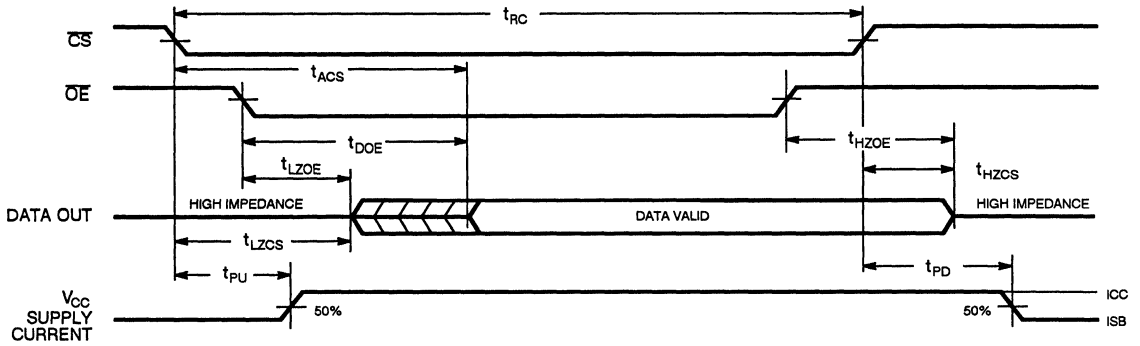
Read Cycle No. 1<sup>[8,9]</sup>



1620-7

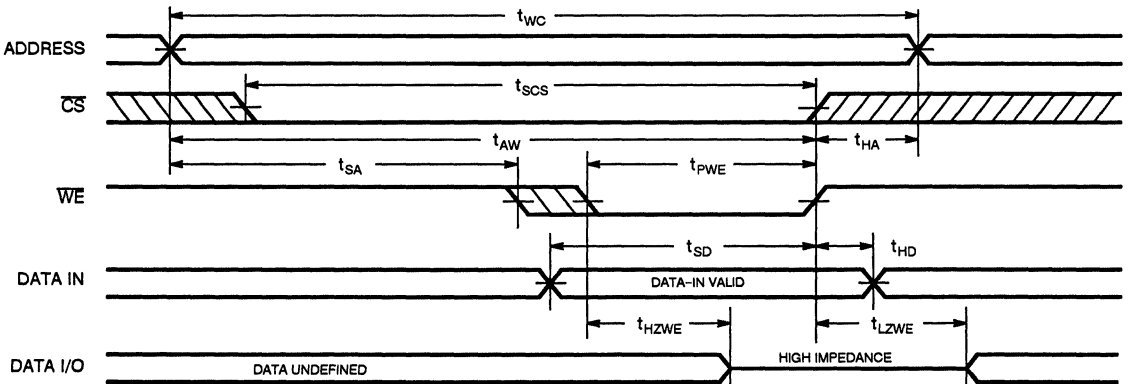
Switching Waveforms (Continued)

Read Cycle No. 2<sup>[8, 10]</sup>



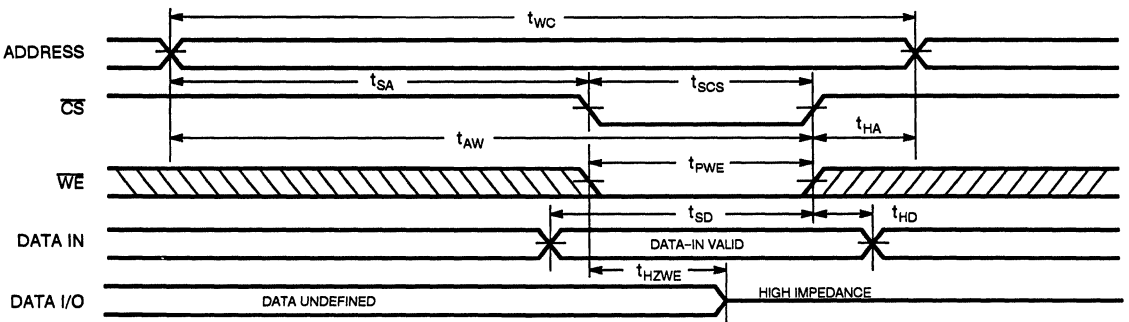
1620-8

Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[7, 11]</sup>



1620-9

Write Cycle No. 2 ( $\overline{CS}$  Controlled)<sup>[7, 11]</sup>



Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

1620-10



### Truth Table

| CS | UB | LB | OE | WE | Input/Outputs            | Mode                |
|----|----|----|----|----|--------------------------|---------------------|
| H  | X  | X  | X  | X  | High Z                   | Deselect Power Down |
| L  | H  | H  | X  | X  | High Z                   | Deselect Power Down |
| L  | L  | L  | L  | H  | Data Out <sub>0-15</sub> | Read                |
| L  | H  | L  | L  | H  | Data Out <sub>0-7</sub>  | Read Lower Byte     |
| L  | L  | H  | L  | H  | Data Out <sub>8-15</sub> | Read Upper Byte     |
| L  | L  | L  | X  | L  | Data In <sub>0-15</sub>  | Write               |
| L  | H  | L  | X  | L  | Data In <sub>0-7</sub>   | Write Lower Byte    |
| L  | L  | H  | X  | L  | Data In <sub>8-15</sub>  | Write Upper Byte    |
| L  | L  | L  | H  | H  | High Z                   | Deselect            |
| L  | H  | L  | H  | H  | High Z                   | Deselect            |
| L  | L  | H  | H  | H  | High Z                   | Deselect            |

Document #: 38-M-00008

### Ordering Information

| Speed | Ordering Code   | Package Type | Operating Range |
|-------|-----------------|--------------|-----------------|
| 45    | CYM1620HD-45C   | HD03         | Commercial      |
|       | CYM1620LHD-45C  | HD03         |                 |
|       | CYM1620HD-45MB  | HD03         | Military        |
|       | CYM1620LHD-45MB | HD03         |                 |
| 55    | CYM1620HD-55C   | HD03         | Commercial      |
|       | CYM1620LHD-55C  | HD03         |                 |
|       | CYM1620HD-55MB  | HD03         | Military        |
|       | CYM1620LHD-55MB | HD03         |                 |



# 64K x 16 Static RAM Module

2

### Features

- High-density 1 Megabit SRAM Module
- High speed CMOS SRAMs
  - Access time – 25 ns
- Customer configurable – x4, x8, x16
- Low active power – 6.8 W (max)
- Hermetic SMD Technology
- TTL compatible inputs and outputs
- Low profile
  - Max. height – .270 in.
- Small PCB footprint – 2 sq in.
- 2 V data retention (L version)

### Functional Description

The CYM1621 is a high performance 1-Megabit Static RAM module organized as 64K words by 16 bits. This module is constructed from sixteen 64K x 1 SRAMs in Leadless Chip Carriers mounted on a ceramic substrate with pins. Four separate  $\overline{CS}$  pins are used to control each 4-bit nibble of the 16-bit word. This feature permits the user to configure this module as either 256K x 4, 128K x 8 or 64K x 16 organization through external decoding and appropriate pairing of the outputs.

Writing to the device is accomplished when the chip select ( $\overline{CS}_{xx}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data

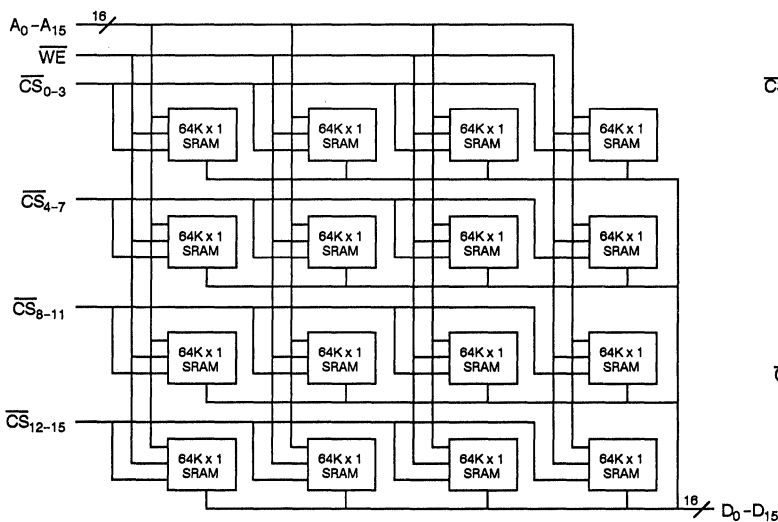
on the data lines ( $D_x$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{15}$ ).

Reading the device is accomplished by taking the chip select ( $\overline{CS}_{xx}$ ) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data lines ( $D_x$ ).

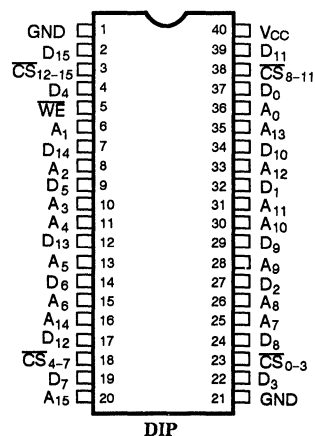
The Data output is in the high impedance state when chip enable ( $\overline{CS}_{xx}$ ) is HIGH or write enable ( $\overline{WE}$ ) is LOW.

Power is consumed in each 4-bit nibble only when the appropriate  $\overline{CS}$  is enabled, thus reducing power in the x4 or x8 mode.

### Logic Block Diagram



### Pin Configuration



1621-1

1621-2

### Selection Guide

|                                |            | 1621HD-25 | 1621HD-30 | 1621HD-35 | 1621HD-45 |
|--------------------------------|------------|-----------|-----------|-----------|-----------|
| Maximum Access time (ns)       |            | 25        | 30        | 35        | 45        |
| Maximum Operating Current (mA) | Commercial | 1250      | 1250      | 1250      | 1250      |
|                                | Military   |           | 1250      | 1250      | 1250      |
| Maximum Standby Current (mA)   | Commercial | 320       | 320       | 320       | 320       |
|                                | Military   |           | 320       | 320       | 320       |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential ..... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V  
(Per MIL-STD-883 Method 3015)

Latch-up Current ..... >200 mA

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[4]</sup> | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over Operating Range

| Parameters         | Description   | Test Conditions   | CYM1621HD |                 | Units |
|--------------------|---|---|-----------|-----------------|-------|
|                    |   |   | Min.      | Max.            |       |
| V <sub>OH</sub>    | Output HIGH Voltage                                 | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA   | 2.4       |                 | V     |
| V <sub>OL</sub>    | Output LOW Voltage                                  | V <sub>CC</sub> = Min.<br>I <sub>OOL</sub> = 8.0 mA Military<br>I <sub>OOL</sub> = 12.0 mA Commercial                                   |           | 0.4             | V     |
|                    |   |   |           |                 |       |
| V <sub>IH</sub>    | Input HIGH Voltage                                  |   | 2.2       | V <sub>CC</sub> | V     |
| V <sub>IL</sub>    | Input LOW Voltage                                   |   | -3.0      | 0.8             | V     |
| I <sub>IX</sub>    | Input Load Current                                  | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>  | -20       | +20             | μA    |
| I <sub>OZ</sub>    | Output Leakage Current                              | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled  | -20       | +20             | μA    |
| I <sub>OS</sub>    | Output Short Circuit Current <sup>[1]</sup>         | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND  |           | -350            | mA    |
| I <sub>CCx16</sub> | V <sub>CC</sub> Operating Supply Current by 16 mode | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS <sub>xx</sub> ≤ V <sub>IL</sub>   |           | 1250            | mA    |
| I <sub>CCx8</sub>  | V <sub>CC</sub> Operating Supply Current by 8 mode  | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS <sub>xx</sub> ≤ V <sub>IL</sub>   |           | 850             | mA    |
| I <sub>CCx4</sub>  | V <sub>CC</sub> Operating Supply Current by 4 mode  | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS <sub>xx</sub> ≤ V <sub>IL</sub>   |           | 650             | mA    |
| I <sub>SB1</sub>   | Automatic CS <sup>[2]</sup><br>Power Down Current   | Max. V <sub>CC</sub> , CS <sub>xx</sub> ≥ V <sub>IH</sub><br>Min. Duty Cycle = 100%   |           | 320             | mA    |
| I <sub>SB2</sub>   | Automatic CS <sup>[2]</sup><br>Power Down Current   | Max. V <sub>CC</sub> , CS <sub>xx</sub> ≥ V <sub>CC</sub> - 0.3V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V |           | 320             | mA    |

## Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 130  | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 35   |       |

### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the CS input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.

Switching Characteristics Over Operating Range <sup>[5]</sup>

| Parameters                        | Description                                      | 1621HD-25 |      | 1621HD-30 |      | 1621HD-35 |      | 1621HD-45 |      | Unit |
|-----------------------------------|--|-----------|------|-----------|------|-----------|------|-----------|------|------|
|                                   |  | Min.      | Max. | Min.      | Max. | Min.      | Max. | Min.      | Max. |      |
| <b>READ CYCLE</b>                 |  |           |      |           |      |           |      |           |      |      |
| t <sub>RC</sub>                   | Read Cycle Time                                  | 25        |      | 30        |      | 35        |      | 45        |      | ns   |
| t <sub>AA</sub>                   | Address to Data Valid                            |           | 25   |           | 30   |           | 35   |           | 45   | ns   |
| t <sub>OHA</sub>                  | Output Hold from Address Change                  | 5         |      | 5         |      | 5         |      | 5         |      | ns   |
| t <sub>ACS</sub>                  | $\overline{CS}$ LOW to Data Valid                |           | 25   |           | 30   |           | 35   |           | 45   | ns   |
| t <sub>LZCS</sub>                 | $\overline{CS}$ LOW to Low Z <sup>[7]</sup>      | 5         |      | 5         |      | 5         |      | 5         |      | ns   |
| t <sub>HZCS</sub>                 | $\overline{CS}$ HIGH to High Z <sup>[6, 7]</sup> |           | 20   |           | 25   |           | 30   |           | 30   | ns   |
| t <sub>PU</sub>                   | $\overline{CS}$ LOW to Power Up                  | 0         |      | 0         |      | 0         |      | 0         |      | ns   |
| t <sub>PD</sub>                   | $\overline{CS}$ HIGH to Power Down               |           | 25   |           | 30   |           | 35   |           | 35   | ns   |
| <b>WRITE CYCLE <sup>[8]</sup></b> |  |           |      |           |      |           |      |           |      |      |
| t <sub>WC</sub>                   | Write Cycle Time                                 | 25        |      | 30        |      | 35        |      | 45        |      | ns   |
| t <sub>SCS</sub>                  | $\overline{CS}$ LOW to Write End                 | 22        |      | 25        |      | 30        |      | 40        |      | ns   |
| t <sub>AW</sub>                   | Address Set-up to Write End                      | 22        |      | 25        |      | 30        |      | 40        |      | ns   |
| t <sub>HA</sub>                   | Address Hold from Write End                      | 0         |      | 0         |      | 0         |      | 0         |      | ns   |
| t <sub>SA</sub>                   | Address Set-up to Write Start                    | 2         |      | 3         |      | 5         |      | 5         |      | ns   |
| t <sub>PWE</sub>                  | $\overline{WE}$ Pulse Width                      | 20        |      | 20        |      | 25        |      | 30        |      | ns   |
| t <sub>SD</sub>                   | Data Set-up to Write End                         | 15        |      | 20        |      | 20        |      | 25        |      | ns   |
| t <sub>HD</sub>                   | Data Hold from Write End                         | 3         |      | 5         |      | 5         |      | 5         |      | ns   |
| t <sub>LZWE</sub>                 | $\overline{WE}$ HIGH to Low Z <sup>[7]</sup>     | 5         |      | 5         |      | 5         |      | 5         |      | ns   |
| t <sub>HZWE</sub>                 | $\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>  | 0         | 20   | 0         | 25   | 0         | 25   | 0         | 25   | ns   |

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZCS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CS} = V_{IL}$
- Address valid prior to or coincident with  $\overline{CS}$  transition LOW.

AC Test Loads and Waveforms

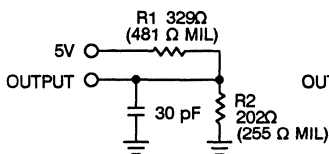


Figure 1a

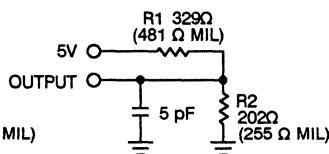


Figure 1b

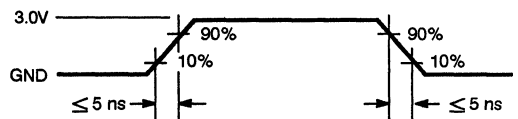
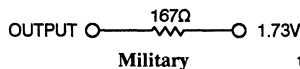


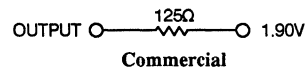
Figure 2

Equivalent to: THEVENIN EQUIVALENT



Military

1621-5



Commercial

1621-6

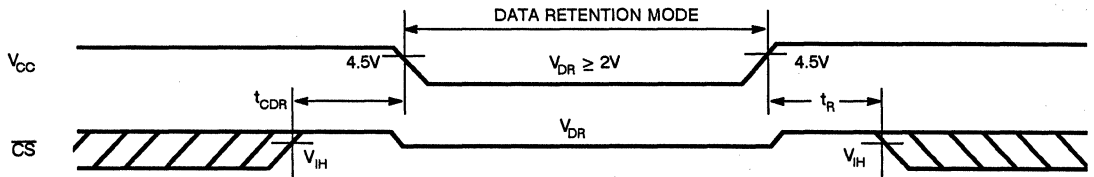
**Data Retention Characteristics (L Version Only)**

| Parameter  | Description                          | Test Conditions   | CYM1621         |      | Units   |
|------------|--------------------------------------|---|-----------------|------|---------|
|            |                                      |   | Min.            | Max. |         |
| $V_{DR}$   | $V_{CC}$ for Retention of Data       | $V_{CC} = 2.0V$ ,<br>$\overline{CS} \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$<br>or $V_{IN} \leq 0.2V$ | 2.0             |      | V       |
| $I_{CCDR}$ | Data Retention Current               |   |                 | 16   | mA      |
| $t_{CDR}$  | Chip Deselect to Data Retention Time |   | 0               |      | ns      |
| $t_R$      | Operation Recovery Time              |   | $t_{RC}^{(12)}$ |      | ns      |
| $I_{LI}$   | Input Leakage Current                |   |                 | 10   | $\mu A$ |

Notes:

12.  $t_{RC}$  = Read Cycle Time.

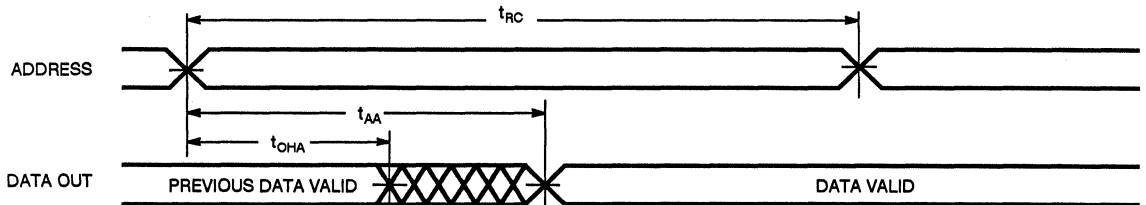
**Data Retention Waveform**



1621-7

**Switching Waveforms<sup>[10]</sup>**

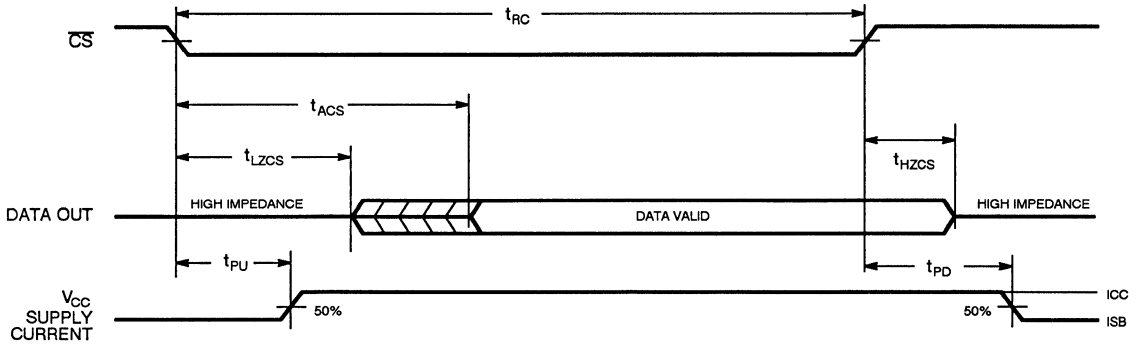
Read Cycle No. 1<sup>[9, 10]</sup>



1621-8

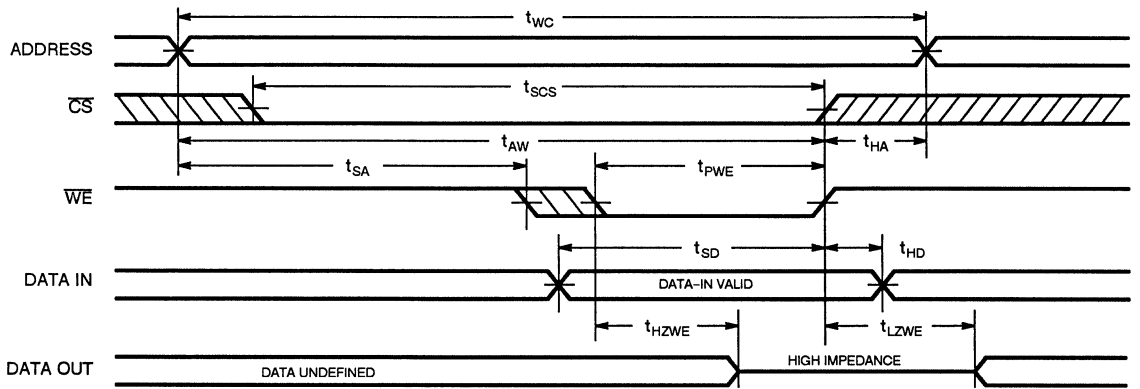
Switching Waveforms (Continued)

Read Cycle No. 2<sup>[9, 10]</sup>



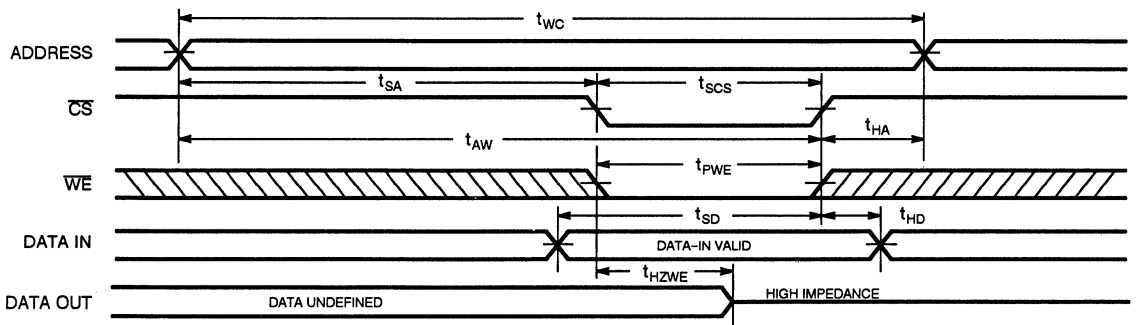
1621-9

Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[8]</sup>



1621-10

Write Cycle No. 2 ( $\overline{CS}$  Controlled)<sup>[8]</sup>



Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

1621-11

### Truth Table

| $\overline{CS}_{xx}$ | $\overline{WE}$ | Input/Outputs | Mode                |
|----------------------|-----------------|---------------|---------------------|
| H                    | X               | High Z        | Deselect Power Down |
| L                    | H               | Data Out      | Read                |
| L                    | L               | Data In       | Write               |

### Ordering Information

| Speed | Ordering Code   | Package Type | Operating Range |
|-------|-----------------|--------------|-----------------|
| 25    | CYM1621HD-25C   | HD02         | Commercial      |
|       | CYM1621LHD-25C  | HD02         |                 |
| 30    | CYM1621HD-30C   | HD02         | Commercial      |
|       | CYM1621LHD-30C  | HD02         |                 |
|       | CYM1621HD-30MB  | HD02         | Military        |
|       | CYM1621LHD-30MB | HD02         |                 |
| 35    | CYM1621HD-35C   | HD02         | Commercial      |
|       | CYM1621LHD-35C  | HD02         |                 |
|       | CYM1621HD-35MB  | HD02         | Military        |
|       | CYM1621LHD-35MB | HD02         |                 |
| 45    | CYM1621HD-45C   | HD02         | Commercial      |
|       | CYM1621LHD-45C  | HD02         |                 |
|       | CYM1621HD-45MB  | HD02         | Military        |
|       | CYM1621LHD-45MB | HD02         |                 |

Document #: 38-M-00009



## 64K x 16 Static RAM Module

### Features

- High-density 1M bit SRAM Module
- High speed
  - Access time - 30 ns
- 16 bit wide organization
- 40 pin Vertical DIP
- Low active power - 1.8 W
- Hermetic SMD Technology
- TTL compatible inputs and outputs
- Low profile
  - Max. height - 0.5 in.
- Small PCB footprint - 0.45 sq in.
- 2V data retention (L version)

### Functional Description

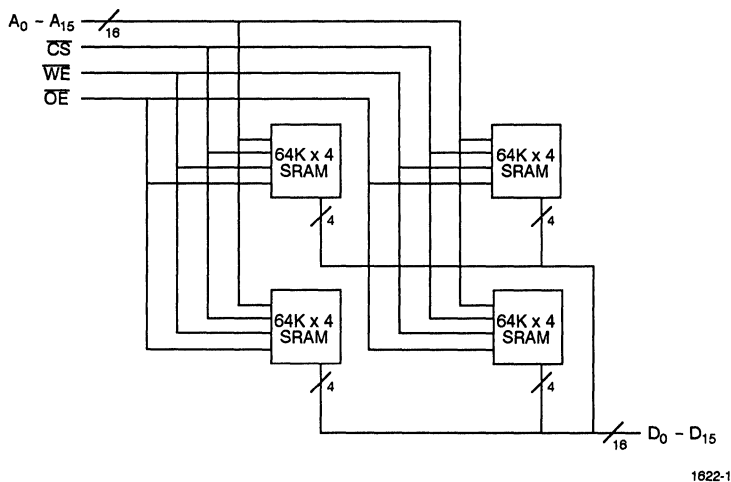
The CYM1622 is a very high performance 1M-bit Static RAM module organized as 64K words by 16 bits. The module is constructed from four 64K x 4 SRAMs in Leadless Chip Carriers mounted on a ceramic substrate with pins. A vertical DIP format minimizes board space (footprint = 0.45 sq in.) while still keeping a maximum height of 0.5 in.

Writing to the memory module is accomplished when the chip select ( $\overline{CS}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the sixteen input/output pins ( $D_0$  through  $D_{15}$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{15}$ ).

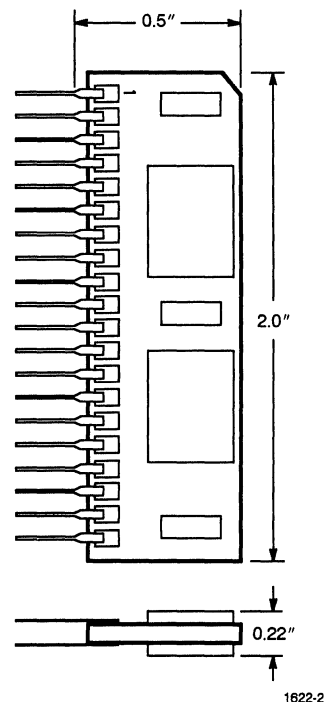
Reading the device is accomplished by taking chip select ( $\overline{CS}$ ) and output enable ( $\overline{OE}$ ) LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the sixteen data input/output pins.

The input/output pins remain in a high impedance state unless the module is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH.

### Logic Block Diagram



### Package Configuration







# 64K x 16 Static RAM Module

## Features

- High-density 1 Megabit SRAM Module
- High speed CMOS SRAMs
  - Access time – 70 ns
- 40 pin – 0.6 in. wide DIP package
- JEDEC compatible pin-out
- Low active power – 1.3 W (max)
- Hermetic SMD Technology
- TTL compatible inputs and outputs
- Commercial and Military Temperature Ranges
- 2 V data retention (L version)

## Functional Description

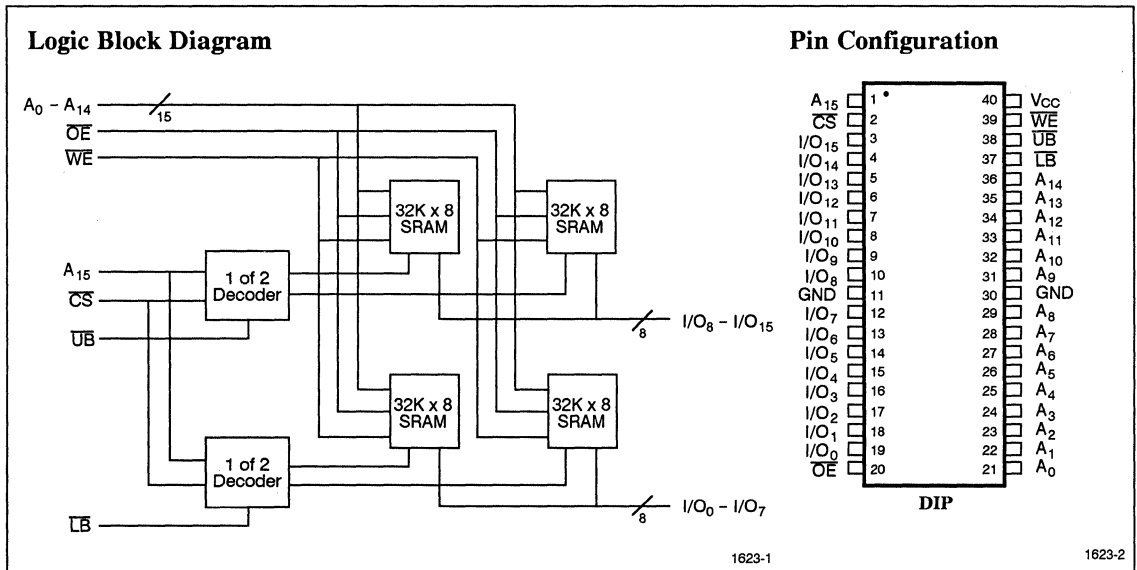
The CYM1623 is a high performance 1 Megabit Static RAM module organized as 64K words by 16 bits. The module is constructed using four 32K x 8 Static RAMs in Leadless Chip Carriers mounted onto a double sided multilayer ceramic substrate. A decoder is used to interpret the higher order address  $A_{15}$  and select one of the two pairs of RAMs.

Writing to the memory module is accomplished when the chip select ( $\overline{CS}$ ), byte select ( $\overline{UB}$ ,  $\overline{LB}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the input/output pins of the selected byte

( $I/O_8 - I/O_{15}$ ,  $I/O_0 - I/O_7$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{15}$ ).

Reading the device is accomplished by taking chip select ( $\overline{CS}$ ), byte select ( $\overline{UB}$ ,  $\overline{LB}$ ) and output enable ( $\overline{OE}$ ) LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

The input/output pins remain in a high impedance state when chip select ( $\overline{CS}$ ), byte select ( $\overline{UB}$ ,  $\overline{LB}$ ) or output enable ( $\overline{OE}$ ) is HIGH, or write enable ( $\overline{WE}$ ) is LOW.



## Selection Guide

|                                |            | 1623HD-70 | 1623HD-85 | 1623HD-100 |
|--------------------------------|------------|-----------|-----------|------------|
| Maximum Access time (ns)       |            | 70        | 85        | 100        |
| Maximum Operating Current (mA) | Commercial | 240       | 240       | 240        |
|                                | Military   | 240       | 240       | 240        |
| Maximum Standby Current (mA)   | Commercial | 70        | 70        | 70         |
|                                | Military   | 70        | 70        | 70         |

## Maximum Ratings

(Above which the useful life may be impaired.)

|   |                 |
|---|-----------------|
| Storage Temperature .....                           | -65°C to +150°C |
| Ambient Temperature with Power Applied .....        | -55°C to +125°C |
| Supply Voltage to Ground Potential .....            | -0.3V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State ..... | -0.3V to +7.0V  |
| DC Input Voltage .....                              | -0.3V to +7.0V  |
| Output Current into Outputs (Low) .....             | 50 mA           |

## Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C        | 5V ± 10%        |
| Military   | -55°C to +125°C     | 5V ± 10%        |

2

## Electrical Characteristics Over Operating Range

| Parameters         | Description                                    | Test Conditions  | CYM1623HD |                 | Units |
|--------------------|--|--|-----------|-----------------|-------|
|                    |  |  | Min.      | Max.            |       |
| V <sub>OH</sub>    | Output HIGH Voltage                            | V <sub>CC</sub> = Min., I <sub>OH</sub> = -1.0 mA  | 2.4       |                 | V     |
| V <sub>OL</sub>    | Output LOW Voltage                             | V <sub>CC</sub> = Min., I <sub>OL</sub> = 4.0 mA   |           | 0.4             | V     |
| V <sub>IH</sub>    | Input HIGH Voltage                             |  | 2.2       | V <sub>CC</sub> | V     |
| V <sub>IL</sub>    | Input LOW Voltage                              |  | -0.3      | 0.8             | V     |
| I <sub>Ix</sub>    | Input Load Current                             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -10       | +10             | μA    |
| I <sub>OZ</sub>    | Output Leakage Current                         | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled   | -10       | +10             | μA    |
| I <sub>CCx16</sub> | V <sub>CC</sub> Operating Supply Current       | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS, UB, & LB = V <sub>IL</sub>  |           | 240             | mA    |
| I <sub>CCx8</sub>  | V <sub>CC</sub> Operating Supply Current       | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS = V <sub>IL</sub> , UB or LB = V <sub>IL</sub>                         |           | 120             | mA    |
| I <sub>SB1</sub>   | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> , CS ≥ V <sub>IH</sub> ,<br>Min. Duty Cycle = 100%  |           | 70              | mA    |
| I <sub>SB2</sub>   | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> , CS ≥ V <sub>CC</sub> - 0.2V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or<br>V <sub>IN</sub> ≤ 0.2V |           | 20              | mA    |

## Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions   | Max. | Units |
|------------------|--------------------|---|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 35   | pF    |
| C <sub>OUT</sub> | Output Capacitance |   | 40   |       |

Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the CS input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- Tested on a sample basis.

## AC Test Loads and Waveforms

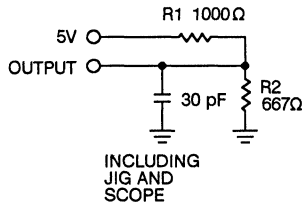


Figure 1a

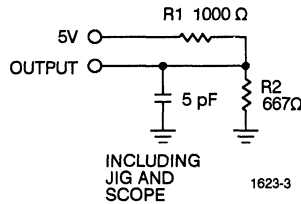


Figure 1b

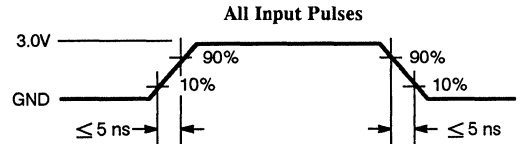
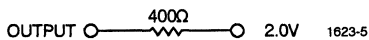


Figure 2

Equivalent to: THEVENIN EQUIVALENT



**Switching Characteristics** Over Operating Range <sup>[4]</sup>

| Parameters                        | Description   | 1623HD-70 |      | 1623HD-85 |      | 1623HD-100 |      | Units |
|-----------------------------------|---|-----------|------|-----------|------|------------|------|-------|
|                                   |   | Min.      | Max. | Min.      | Max. | Min.       | Max. |       |
| <b>READ CYCLE</b>                 |   |           |      |           |      |            |      |       |
| t <sub>RC</sub>                   | Read Cycle Time   | 70        |      | 85        |      | 100        |      | ns    |
| t <sub>AA</sub>                   | Address to Data Valid                                   |           | 70   |           | 85   |            | 100  | ns    |
| t <sub>OHA</sub>                  | Data Hold from Address Change                           | 5         |      | 5         |      | 5          |      | ns    |
| t <sub>ACS</sub>                  | $\overline{\text{CS}}$ LOW to Data Valid                |           | 70   |           | 85   |            | 100  | ns    |
| t <sub>DOE</sub>                  | $\overline{\text{OE}}$ LOW to Data Valid                |           | 40   |           | 50   |            | 60   | ns    |
| t <sub>LZOE</sub>                 | $\overline{\text{OE}}$ LOW to Low Z                     | 5         |      | 5         |      | 5          |      | ns    |
| t <sub>HZOE</sub>                 | $\overline{\text{OE}}$ HIGH to High Z                   |           | 35   |           | 35   |            | 40   | ns    |
| t <sub>LZCS</sub>                 | $\overline{\text{CS}}$ LOW to Low Z <sup>[6]</sup>      | 5         |      | 5         |      | 5          |      | ns    |
| t <sub>HZCS</sub>                 | $\overline{\text{CS}}$ HIGH to High Z <sup>[5, 6]</sup> |           | 35   |           | 35   |            | 40   | ns    |
| <b>WRITE CYCLE <sup>[7]</sup></b> |   |           |      |           |      |            |      |       |
| t <sub>WC</sub>                   | Write Cycle Time  | 70        |      | 85        |      | 100        |      | ns    |
| t <sub>SCS</sub>                  | $\overline{\text{CS}}$ LOW to Write End                 | 65        |      | 75        |      | 90         |      | ns    |
| t <sub>AW</sub>                   | Address Set-up to Write End                             | 65        |      | 75        |      | 90         |      | ns    |
| t <sub>HA</sub>                   | Address Hold from Write End                             | 10        |      | 15        |      | 15         |      | ns    |
| t <sub>SA</sub>                   | Address Set-up to Write Start                           | 25        |      | 25        |      | 30         |      | ns    |
| t <sub>PWE</sub>                  | $\overline{\text{WE}}$ Pulse Width                      | 30        |      | 35        |      | 35         |      | ns    |
| t <sub>SD</sub>                   | Data Set-up to Write End                                | 20        |      | 20        |      | 25         |      | ns    |
| t <sub>HD</sub>                   | Data Hold from Write End                                | 10        |      | 10        |      | 15         |      | ns    |
| t <sub>LZWE</sub>                 | $\overline{\text{WE}}$ HIGH to Low Z <sup>[6]</sup>     | 5         |      | 5         |      | 5          |      | ns    |
| t <sub>HZWE</sub>                 | $\overline{\text{WE}}$ LOW to High Z <sup>[5, 6]</sup>  | 0         | 30   | 0         | 35   | 0          | 40   | ns    |

**Notes:**

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
5. t<sub>HZCS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in *Figure 1b*. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device. These parameters are guaranteed and not 100% tested.

7. The internal write time of the memory is defined by the overlap of  $\overline{\text{CS}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8.  $\overline{\text{WE}}$  is HIGH for read cycle.
9. Device is continuously selected,  $\overline{\text{CS}} = V_{\text{IL}}$  and  $\overline{\text{OE}} = V_{\text{IL}}$ .
10. Address valid prior to or coincident with  $\overline{\text{CS}}$  transition low.
11. Data I/O will be high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .

**Data Retention Characteristics (L Version Only)**

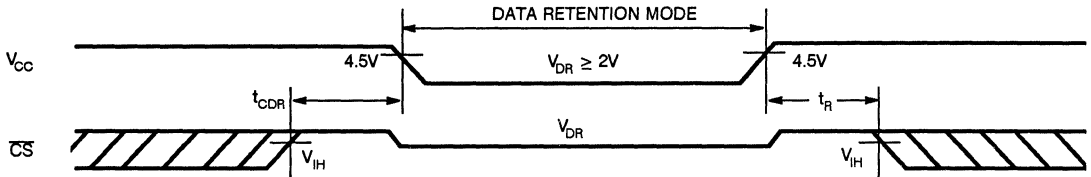
| Parameter        | Description                          | Test Conditions   | CYM1623         |      | Units   |
|------------------|--------------------------------------|---|-----------------|------|---------|
|                  |                                      |   | Min.            | Max. |         |
| $V_{DR}$         | $V_{CC}$ for Retention Data          | $V_{CC} = 2.0V$ ,<br>$\overline{CS} \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$<br>or $V_{IN} \leq 0.2V$ | 2.0             |      | V       |
| $I_{CCDR}$       | Data Retention Current               |   |                 | 250  | $\mu A$ |
| $t_{CDR}^{[13]}$ | Chip Deselect to Data Retention Time |   | 0               |      | ns      |
| $t_R^{[13]}$     | Operation Recovery Time              |   | $t_{RC}^{[12]}$ |      | ns      |

Notes:

12.  $t_{RC}$  = Read Cycle Time.

13. Guaranteed, not tested.

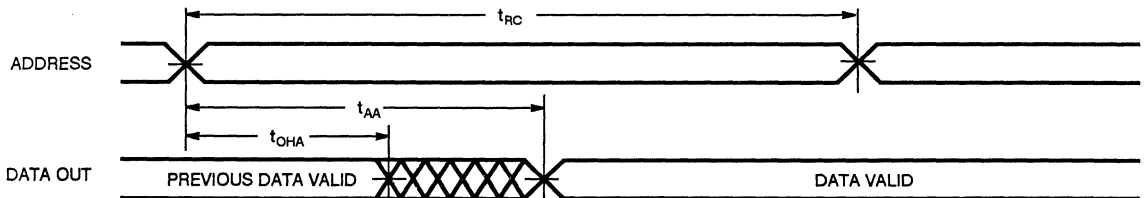
**Data Retention Waveform**



1623-6

**Switching Waveforms<sup>[10]</sup>**

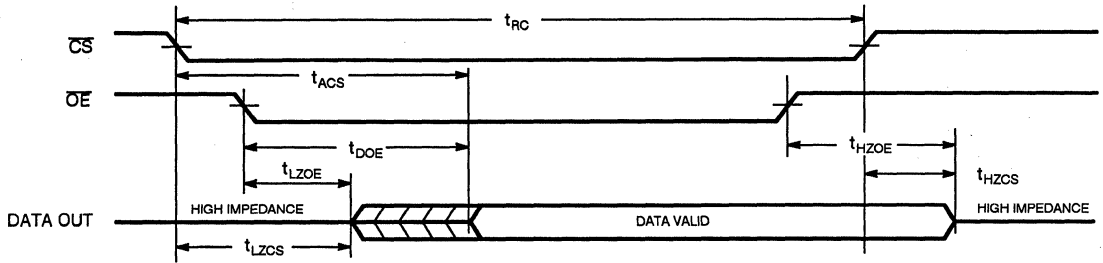
Read Cycle No. 1<sup>[8,9]</sup>



1623-7

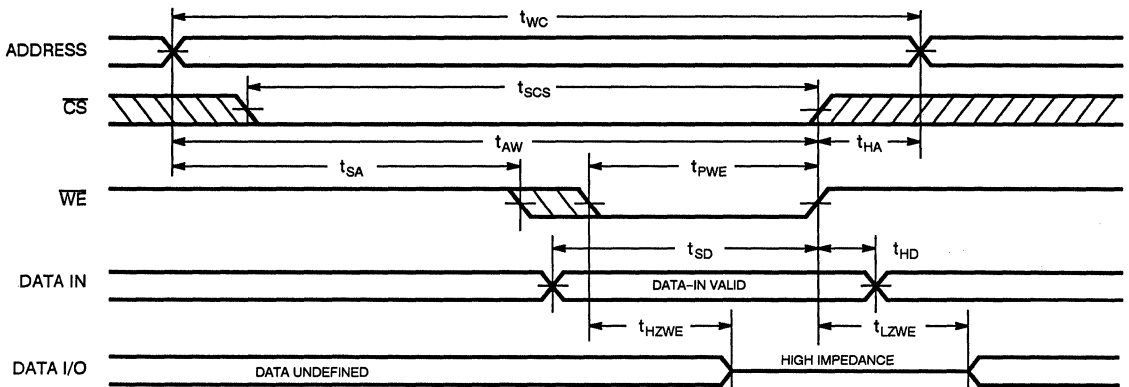
### Switching Waveforms (Continued)

#### Read Cycle No. 2<sup>[8, 10]</sup>



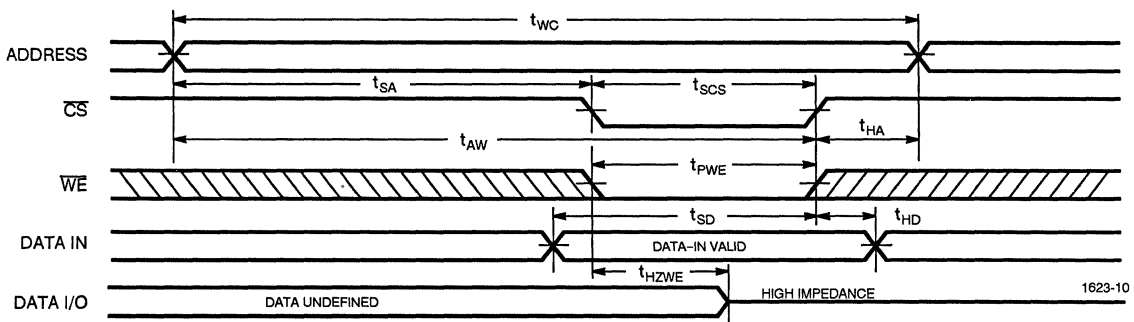
1623-8

#### Write Cycle No. 1 ( $\overline{WE}$ Controlled)<sup>[7, 11]</sup>



1623-9

#### Write Cycle No. 2 ( $\overline{CS}$ Controlled)<sup>[7, 11]</sup>



1623-10

Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

**Truth Table**

| $\overline{CS}$ | $\overline{UB}$ | $\overline{LB}$ | $\overline{OE}$ | $\overline{WE}$ | Input/Outputs            | Mode                |
|-----------------|-----------------|-----------------|-----------------|-----------------|--------------------------|---------------------|
| H               | X               | X               | X               | X               | High Z                   | Deselect Power Down |
| L               | H               | H               | X               | X               | High Z                   | Deselect Power Down |
| L               | L               | L               | L               | H               | Data Out <sub>0-15</sub> | Read                |
| L               | H               | L               | L               | H               | Data Out <sub>0-7</sub>  | Read Lower Byte     |
| L               | L               | H               | L               | H               | Data Out <sub>8-15</sub> | Read Upper Byte     |
| L               | L               | L               | X               | L               | Data In <sub>0-15</sub>  | Write               |
| L               | H               | L               | X               | L               | Data In <sub>0-7</sub>   | Write Lower Byte    |
| L               | L               | H               | X               | L               | Data In <sub>8-15</sub>  | Write Upper Byte    |
| L               | L               | L               | H               | H               | High Z                   | Deselect            |
| L               | H               | L               | H               | H               | High Z                   | Deselect            |
| L               | L               | H               | H               | H               | High Z                   | Deselect            |

Document #: 38-M-00011

**Ordering Information**

| Speed | Ordering Code   | Package Type | Operating Range |
|-------|-----------------|--------------|-----------------|
| 70    | CYM1623HD-70C   | HD03         | Commercial      |
|       | CYM1623LHD-70C  | HD03         |                 |
|       | CYM1623HD-70M   | HD03         | Military        |
|       | CYM1623LHD-70M  | HD03         |                 |
| 85    | CYM1623HD-85C   | HD03         | Commercial      |
|       | CYM1623LHD-85C  | HD03         |                 |
|       | CYM1623HD-85M   | HD03         | Military        |
|       | CYM1623LHD-85M  | HD03         |                 |
| 100   | CYM1623HD-100C  | HD03         | Commercial      |
|       | CYM1623LHD-100C | HD03         |                 |
|       | CYM1623HD-100M  | HD03         | Military        |
|       | CYM1623LHD-100M | HD03         |                 |



# 64K x 16 Static RAM Module

## Features

- High-density 1M bit SRAM Module
- High speed CMOS SRAMs
  - Access time - 30 ns
- Low active power - 2.4 W (max)
- SMD technology
- TTL compatible inputs and outputs
- Low profile
  - Max. height - .50 in.
- Small PCB footprint - 0.9 sq in.
- 2V data retention (L version)

## Functional Description

The CYM1626 is a high performance 1M-bit Static RAM module organized as 64K words by 16 bits. This module is constructed from four 16K x 4 SRAMs in SOJ packages mounted on an epoxy laminate board with pins.

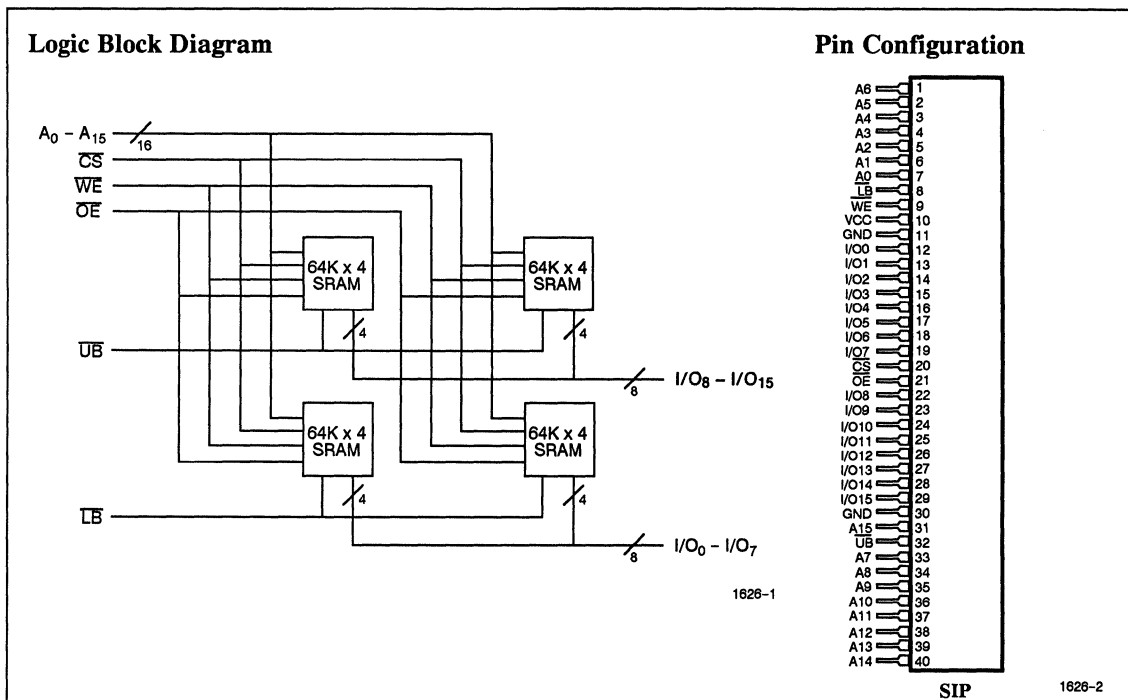
Selecting the device is achieved by a chip select input pin as well as two byte select pins ( $\overline{UB}$ ,  $\overline{LB}$ ) for independently selecting upper or lower byte for read or write operations.

Writing to the memory module is accomplished when the chip select ( $\overline{CS}$ ), byte select ( $\overline{UB}$ ,  $\overline{LB}$ ) and write enable ( $\overline{WE}$ ) inputs are LOW. Data on the input/out-

put pins of the selected byte ( $I/O_8 - I/O_{15}$ ,  $I/O_0 - I/O_7$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{15}$ ).

Reading the device is accomplished by taking chip select ( $\overline{CS}$ ), byte select ( $\overline{UB}$ ,  $\overline{LB}$ ) and output enable ( $\overline{OE}$ ) LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

The input/output pins remain in a high impedance state when chip select ( $\overline{CS}$ ), byte select ( $\overline{UB}$ ,  $\overline{LB}$ ) or output enable ( $\overline{OE}$ ) is HIGH, or write enable ( $\overline{WE}$ ) is LOW.



## Selection Guide

|                                | 1626PS-30 | 1626PS-35 | 1626PS-45 |
|--------------------------------|-----------|-----------|-----------|
| Maximum Access time (ns)       | 30        | 35        | 45        |
| Maximum Operating Current (mA) | 440       | 440       | 440       |
| Maximum Standby Current (mA)   | 160       | 160       | 160       |

## Maximum Ratings

(Above which the useful life may be impaired)

|   |                 |
|---|-----------------|
| Storage Temperature .....                           | -65°C to +150°C |
| Ambient Temperature with Power Applied .....        | -10°C to +90°C  |
| Supply Voltage to Ground Potential .....            | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State ..... | -0.5V to +7.0V  |

|   |                |
|---|----------------|
| DC Input Voltage .....                  | -0.5V to +7.0V |
| Output Current into Outputs (Low) ..... | 20 mA          |

2

## Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C        | 5V ± 10%        |

## Electrical Characteristics Over Operating Range

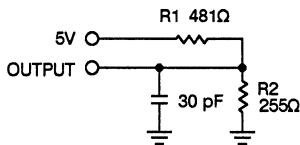
| Parameters         | Description                                    | Test Conditions  | CYM1626PS |                 | Units |
|--------------------|--|--|-----------|-----------------|-------|
|                    |  |  | Min.      | Max.            |       |
| V <sub>OH</sub>    | Output HIGH Voltage                            | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA  | 2.4       |                 | V     |
| V <sub>OL</sub>    | Output LOW Voltage                             | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA   |           | 0.4             | V     |
| V <sub>IH</sub>    | Input HIGH Voltage                             |  | 2.2       | V <sub>CC</sub> | V     |
| V <sub>IL</sub>    | Input LOW Voltage                              |  | -0.5      | 0.8             | V     |
| I <sub>IX</sub>    | Input Load Current                             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -20       | +20             | μA    |
| I <sub>OZ</sub>    | Output Leakage Current                         | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> . Output Disabled   | -20       | +20             | μA    |
| I <sub>OS</sub>    | Output Short Circuit Current <sup>[1]</sup>    | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND   |           | -350            | mA    |
| I <sub>CCx16</sub> | V <sub>CC</sub> Operating Supply Current       | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS, UB, & LB ≤ V <sub>IL</sub>  |           | 440             | mA    |
| I <sub>CCx8</sub>  | V <sub>CC</sub> Operating Supply Current       | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS ≤ V <sub>IL</sub> , UB or LB ≤ V <sub>IL</sub>                         |           | 290             | mA    |
| I <sub>SB1</sub>   | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> , CS ≥ V <sub>IH</sub> .<br>Min. Duty Cycle = 100%  |           | 160             | mA    |
| I <sub>SB2</sub>   | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> , CS ≥ V <sub>CC</sub> - 0.3V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V |           | 80              | mA    |

## Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions   | Max. | Units |
|------------------|--------------------|---|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 45   | pF    |
| C <sub>OUT</sub> | Output Capacitance |   | 35   |       |

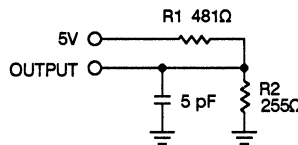
- Notes:
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
  - A pull-up resistor to V<sub>CC</sub> on the CS input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
  - Tested on a sample basis.

## AC Test Loads and Waveforms



INCLUDING  
JIG AND  
SCOPE

Figure 1a



INCLUDING  
JIG AND  
SCOPE

Figure 1b

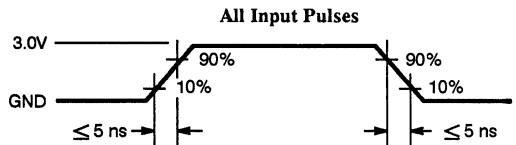
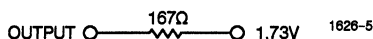


Figure 2

Equivalent to: THEVENIN EQUIVALENT





Switching Characteristics Over Operating Range<sup>[4]</sup>

| Parameters                       | Description                                     | 1626PS-30 |      | 1626PS-35 |      | 1626PS-45 |      | Units |
|----------------------------------|---|-----------|------|-----------|------|-----------|------|-------|
|                                  |   | Min.      | Max. | Min.      | Max. | Min.      | Max. |       |
| <b>READ CYCLE</b>                |   |           |      |           |      |           |      |       |
| t <sub>RC</sub>                  | Read Cycle Time                                 | 30        |      | 35        |      | 45        |      | ns    |
| t <sub>AA</sub>                  | Address to Data Valid                           |           | 30   |           | 35   |           | 45   | ns    |
| t <sub>OHA</sub>                 | Data Hold from Address Change                   | 3         |      | 3         |      | 3         |      | ns    |
| t <sub>ACS</sub>                 | $\overline{CS}$ LOW to Data Valid               |           | 30   |           | 35   |           | 45   | ns    |
| t <sub>DOE</sub>                 | $\overline{OE}$ LOW to Data Valid               |           | 20   |           | 25   |           | 30   | ns    |
| t <sub>LZOE</sub>                | $\overline{OE}$ LOW to LOW Z                    | 3         |      | 3         |      | 3         |      | ns    |
| t <sub>HZOE</sub>                | $\overline{OE}$ HIGH to HIGH Z                  |           | 20   |           | 20   |           | 20   | ns    |
| t <sub>LZCS</sub>                | $\overline{CS}$ LOW to Low Z <sup>[6]</sup>     | 3         |      | 3         |      | 3         |      | ns    |
| t <sub>HZCS</sub>                | $\overline{CS}$ HIGH to High Z <sup>[5,6]</sup> |           | 15   |           | 20   |           | 20   | ns    |
| t <sub>PU</sub>                  | $\overline{CS}$ LOW to Power Up                 | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>PD</sub>                  | $\overline{CS}$ HIGH to Power Down              |           | 30   |           | 35   |           | 45   | ns    |
| <b>WRITE CYCLE<sup>[7]</sup></b> |   |           |      |           |      |           |      |       |
| t <sub>WC</sub>                  | Write Cycle Time                                | 25        |      | 35        |      | 35        |      | ns    |
| t <sub>SCS</sub>                 | $\overline{CS}$ LOW to Write End                | 25        |      | 35        |      | 35        |      | ns    |
| t <sub>AW</sub>                  | Address Set-up to Write End                     | 25        |      | 30        |      | 35        |      | ns    |
| t <sub>HA</sub>                  | Address Hold from Write End                     | 2         |      | 3         |      | 3         |      | ns    |
| t <sub>SA</sub>                  | Address Set-up to Write Start                   | 2         |      | 2         |      | 2         |      | ns    |
| t <sub>PWE</sub>                 | $\overline{WE}$ Pulse Width                     | 20        |      | 25        |      | 35        |      | ns    |
| t <sub>SD</sub>                  | Data Set-up to Write End                        | 15        |      | 20        |      | 25        |      | ns    |
| t <sub>HD</sub>                  | Data Hold from Write End                        | 2         |      | 2         |      | 2         |      | ns    |
| t <sub>LZWE</sub>                | $\overline{WE}$ HIGH to Low Z <sup>[6]</sup>    | 3         |      | 3         |      | 3         |      | ns    |
| t <sub>HZWE</sub>                | $\overline{WE}$ LOW to High Z <sup>[5,6]</sup>  | 0         | 15   | 0         | 15   | 0         | 15   | ns    |

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZCS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device. These parameters are guaranteed and not 100% tested.
- The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CS} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{CS}$  transition low.
- $\overline{CS}$ ,  $\overline{UB}$  and  $\overline{LB}$  are represented by  $\overline{CS}$  in the switching Characteristics and Waveforms.

**Data Retention Characteristics (L Version Only)**

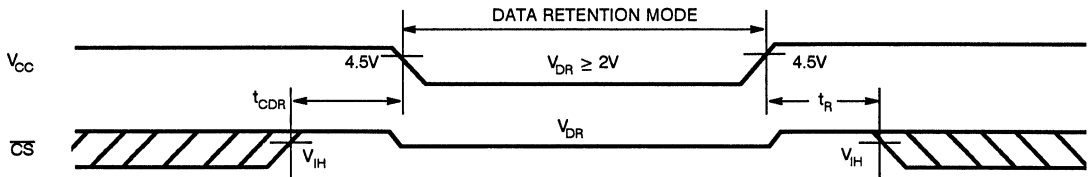
| Parameter        | Description                          | Test Conditions  | CYM1626         |      | Units   |
|------------------|--------------------------------------|--|-----------------|------|---------|
|                  |                                      |  | Min.            | Max. |         |
| $V_{DR}$         | $V_{CC}$ for Retention Data          | $V_{CC} = 2.0V,$<br>$\overline{CS} \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$<br>or $V_{IN} \leq 0.2V$ | 2.0             |      | V       |
| $I_{CCDR}$       | Data Retention Current               |  |                 | 16   | mA      |
| $t_{CDR}^{[13]}$ | Chip Deselect to Data Retention Time |  | 0               |      | ns      |
| $t_R^{[13]}$     | Operation Recovery Time              |  | $t_{RC}^{[12]}$ |      | ns      |
| $I_{LI}^{[13]}$  | Input Leakage Current                |  |                 | 5    | $\mu A$ |

Notes:

12.  $t_{RC}$  = Read Cycle Time.

13. Guaranteed, not tested.

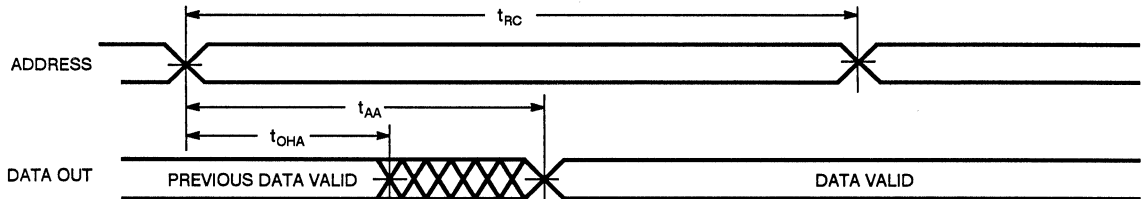
**Data Retention Waveform**



1626-6

**Switching Waveforms<sup>[11]</sup>**

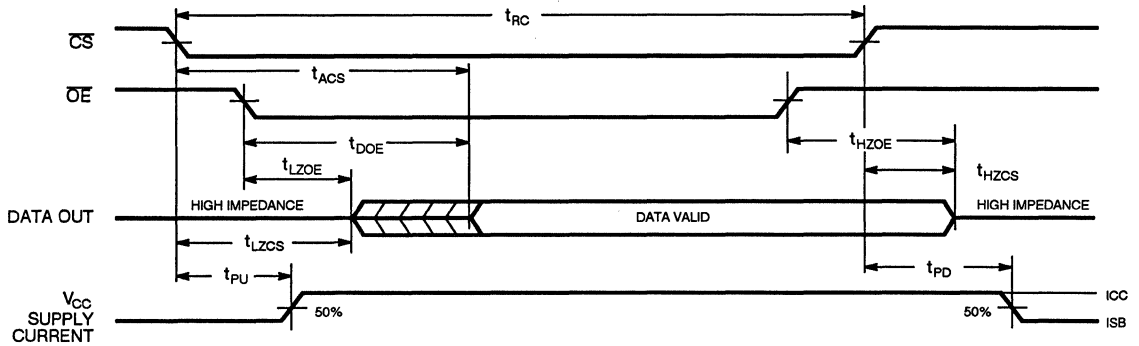
Read Cycle No. 1<sup>[8,9]</sup>



1626-7

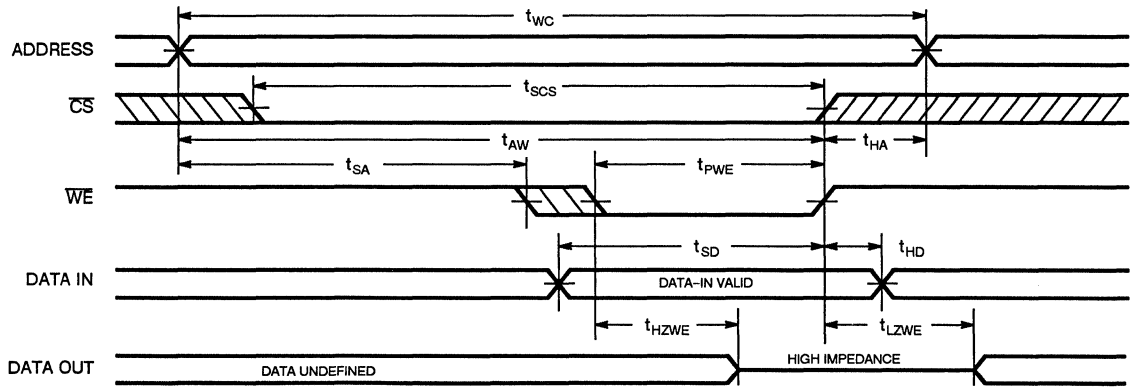
Switching Waveforms (Continued)

Read Cycle No. 2<sup>[8, 10]</sup>



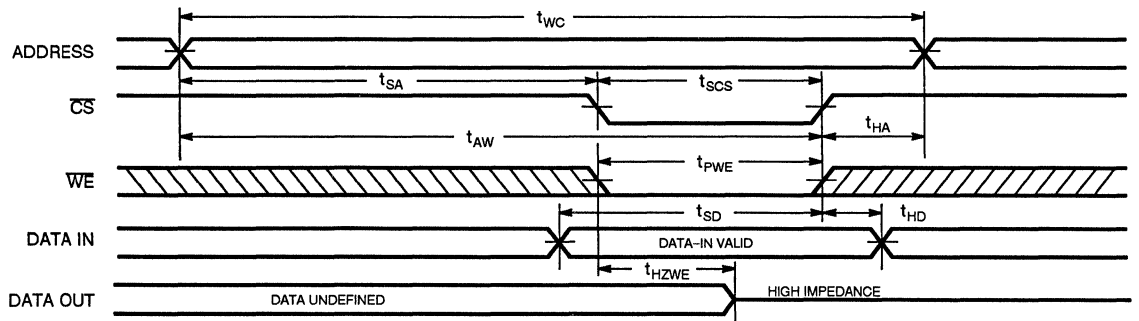
1626-8

Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[7]</sup>



1626-9

Write Cycle No. 2 ( $\overline{CS}$  Controlled)<sup>[7]</sup>



Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

1626-10

**Truth Table**

| CS | UB | LB | OE | WE | Input/Outputs            | Mode                |
|----|----|----|----|----|--------------------------|---------------------|
| H  | X  | X  | X  | X  | High Z                   | Deselect Power Down |
| L  | H  | H  | X  | X  | High Z                   | Deselect Power Down |
| L  | L  | L  | L  | H  | Data Out <sub>0-15</sub> | Read Word           |
| L  | H  | L  | L  | H  | Data Out <sub>0-7</sub>  | Read Lower Byte     |
| L  | L  | H  | L  | H  | Data Out <sub>8-15</sub> | Read Upper Byte     |
| L  | L  | L  | X  | L  | Data In <sub>0-15</sub>  | Write Word          |
| L  | H  | L  | X  | L  | Data In <sub>0-7</sub>   | Write Lower Byte    |
| L  | L  | H  | X  | L  | Data In <sub>8-15</sub>  | Write Upper Byte    |
| L  | L  | L  | H  | H  | High Z                   | Deselect            |
| L  | H  | L  | H  | H  | High Z                   | Deselect            |
| L  | L  | H  | H  | H  | High Z                   | Deselect            |

**Ordering Information**

| Speed | Ordering Code | Package Type | Operating Range |
|-------|---------------|--------------|-----------------|
| 30    | M1626PS-30C   | PS02         | Commercial      |
|       | M1626LPS-30C  | PS02         |                 |
| 35    | M1626PS-35C   | PS02         |                 |
|       | M1626LPS-35C  | PS02         |                 |
| 45    | M1626PS-45C   | PS02         |                 |
|       | M1626LPS-45C  | PS02         |                 |

Document #: 38-M-00012



## 256K x 16 Static RAM Module

### Features

- High-density 4 Megabit SRAM Module
- High speed CMOS SRAMs
  - Access time – 25 ns
- Customer configurable – x4, x8, x16
- Low active power – 7.2 W (max)
- Hermetic SMD Technology
- TTL compatible inputs and outputs
- Low profile
  - Max. height – .300 in.
- Small PCB footprint – 2.2 sq in.
- 2 V data retention (L version)

### Functional Description

The CYM1641 is a high performance 4-Megabit Static RAM module organized as 256K words by 16 bits. This module is constructed from sixteen 256K x 1 SRAMs in Leadless Chip Carriers mounted on a ceramic substrate with pins. Four separate  $\overline{CS}$  pins are used to control each 4-bit nibble of the 16-bit word. This feature permits the user to configure this module as either 1M x 4, 512K x 8 or 256K x 16 organization through external decoding and appropriate pairing of the outputs.

Writing to the device is accomplished when the chip select ( $\overline{CS}_{xx}$ ) and write enable ( $\overline{WE}_{U,L}$ ) inputs are both LOW.

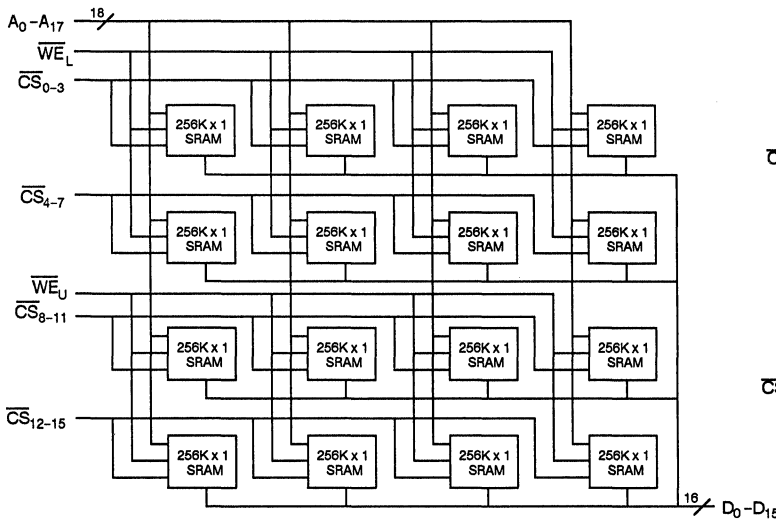
Data on the data lines ( $D_x$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{17}$ ).

Reading the device is accomplished by taking the chip select ( $\overline{CS}_{xx}$ ) LOW, while write enable ( $\overline{WE}_{U,L}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data lines ( $D_x$ ).

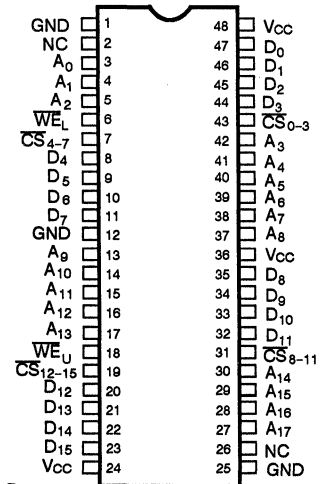
The Data output is in the high impedance state when chip enable ( $\overline{CS}_{xx}$ ) is HIGH or write enable ( $\overline{WE}_{U,L}$ ) is LOW.

Power is consumed in each 4-bit nibble only when the appropriate  $\overline{CS}$  is enabled, thus reducing power in the x4 or x8 mode.

### Logic Block Diagram



### Pin Configuration



DIP  
TOP VIEW

1641-1

1641-2

### Selection Guide

|                                |            | 1641HD-25 | 1641HD-35 | 1641HD-45 | 1641HD-55 |
|--------------------------------|------------|-----------|-----------|-----------|-----------|
| Maximum Access time (ns)       |            | 25        | 35        | 45        | 55        |
| Maximum Operating Current (mA) | Commercial | 1310      | 1310      | 1310      | 1310      |
|                                | Military   |           | 1310      | 1310      | 1310      |
| Maximum Standby Current (mA)   | Commercial | 320       | 320       | 320       | 320       |
|                                | Military   |           | 320       | 320       | 320       |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|  |                 |                                |  |
|--|-----------------|--------------------------------|--|
| Storage Temperature .....                              | -65°C to +150°C | Static Discharge Voltage ..... | > 2001V<br>(Per MIL-STD-883 Method 3015) |
| Ambient Temperature with<br>Power Applied .....        | -55°C to +125°C | Latch-up Current .....         | > 200 mA                                 |
| Supply Voltage to Ground Potential .....               | -0.5V to +7.0V  |                                |  |
| DC Voltage Applied to Outputs<br>in High Z State ..... | -0.5V to +7.0V  |                                |  |
| DC Input Voltage .....                                 | -3.0V to 7.0V   |                                |  |
| Output Current into Outputs (Low) .....                | 20 mA           |                                |  |

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[4]</sup> | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over Operating Range

| Parameters         | Description   | Test Conditions   | CYM1641HD |                 | Units |
|--------------------|---|---|-----------|-----------------|-------|
|                    |   |   | Min.      | Max.            |       |
| V <sub>OH</sub>    | Output HIGH Voltage                                 | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA   | 2.4       |                 | V     |
| V <sub>OL</sub>    | Output LOW Voltage                                  | V <sub>CC</sub> = Min.<br>I <sub>OL</sub> = 8.0 mA Military<br>I <sub>OL</sub> = 12.0 mA Commercial                                     |           | 0.4             | V     |
|                    |   |   |           |                 |       |
| V <sub>IH</sub>    | Input HIGH Voltage                                  |   | 2.2       | V <sub>CC</sub> | V     |
| V <sub>IL</sub>    | Input LOW Voltage                                   |   | -3.0      | 0.8             | V     |
| I <sub>IX</sub>    | Input Load Current                                  | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>  | -80       | +80             | μA    |
| I <sub>OZ</sub>    | Output Leakage Current                              | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled  | -10       | +10             | μA    |
| I <sub>OS</sub>    | Output Short Circuit Current <sup>[1]</sup>         | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND  |           | -350            | mA    |
| I <sub>CCx16</sub> | V <sub>CC</sub> Operating Supply Current by 16 mode | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS <sub>xx</sub> ≤ V <sub>IL</sub>   |           | 1310            | mA    |
| I <sub>CCx8</sub>  | V <sub>CC</sub> Operating Supply Current by 8 mode  | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS <sub>xx</sub> ≤ V <sub>IL</sub>   |           | 850             | mA    |
| I <sub>CCx4</sub>  | V <sub>CC</sub> Operating Supply Current by 4 mode  | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS <sub>xx</sub> ≤ V <sub>IL</sub>   |           | 650             | mA    |
| I <sub>SB1</sub>   | Automatic CS <sup>[2]</sup><br>Power Down Current   | Max. V <sub>CC</sub> , CS <sub>xx</sub> ≥ V <sub>IH</sub><br>Min. Duty Cycle = 100%   |           | 320             | mA    |
| I <sub>SB2</sub>   | Automatic CS <sup>[2]</sup><br>Power Down Current   | Max. V <sub>CC</sub> , CS <sub>xx</sub> ≥ V <sub>CC</sub> - 0.3V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V |           | 320             | mA    |

## Capacitance <sup>[3]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 130  | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 35   |       |

### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the CS input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.

Switching Characteristics Over Operating Range [5]

| Parameters             | Description                           | 1641HD-25 |      | 1641HD-35 |      | 1641HD-45 |      | 1641HD-55 |      | Unit |
|------------------------|---------------------------------------|-----------|------|-----------|------|-----------|------|-----------|------|------|
|                        |                                       | Min.      | Max. | Min.      | Max. | Min.      | Max. | Min.      | Max. |      |
| <b>READ CYCLE</b>      |                                       |           |      |           |      |           |      |           |      |      |
| t <sub>RC</sub>        | Read Cycle Time                       | 25        |      | 35        |      | 45        |      | 55        |      | ns   |
| t <sub>AA</sub>        | Address to Data Valid                 |           | 25   |           | 35   |           | 45   |           | 55   | ns   |
| t <sub>OHA</sub>       | Output Hold from Address Change       | 5         |      | 5         |      | 5         |      | 5         |      | ns   |
| t <sub>ACS</sub>       | $\overline{CS}$ LOW to Data Valid     |           | 25   |           | 35   |           | 45   |           | 55   | ns   |
| t <sub>LZCS</sub>      | $\overline{CS}$ LOW to Low Z [7]      | 3         |      | 3         |      | 3         |      | 3         |      | ns   |
| t <sub>HZCS</sub>      | $\overline{CS}$ HIGH to High Z [6, 7] |           | 15   |           | 20   |           | 25   |           | 25   | ns   |
| t <sub>PU</sub>        | $\overline{CS}$ LOW to Power Up       | 0         |      | 0         |      | 0         |      | 0         |      | ns   |
| t <sub>PD</sub>        | $\overline{CS}$ HIGH to Power Down    |           | 25   |           | 35   |           | 45   |           | 55   | ns   |
| <b>WRITE CYCLE [8]</b> |                                       |           |      |           |      |           |      |           |      |      |
| t <sub>WC</sub>        | Write Cycle Time                      | 25        |      | 35        |      | 45        |      | 55        |      | ns   |
| t <sub>SCS</sub>       | $\overline{CS}$ LOW to Write End      | 25        |      | 35        |      | 45        |      | 55        |      | ns   |
| t <sub>AW</sub>        | Address Set-up to Write End           | 25        |      | 35        |      | 45        |      | 55        |      | ns   |
| t <sub>HA</sub>        | Address Hold from Write End           | 2         |      | 2         |      | 2         |      | 2         |      | ns   |
| t <sub>SA</sub>        | Address Set-up to Write Start         | 0         |      | 0         |      | 2         |      | 2         |      | ns   |
| t <sub>PWE</sub>       | $\overline{WE}$ Pulse Width           | 25        |      | 35        |      | 35        |      | 35        |      | ns   |
| t <sub>SD</sub>        | Data Set-up to Write End              | 15        |      | 20        |      | 20        |      | 25        |      | ns   |
| t <sub>HD</sub>        | Data Hold from Write End              | 0         |      | 0         |      | 0         |      | 0         |      | ns   |
| t <sub>LZWE</sub>      | $\overline{WE}$ HIGH to Low Z [7]     | 3         |      | 3         |      | 3         |      | 3         |      | ns   |
| t <sub>HZWE</sub>      | $\overline{WE}$ LOW to High Z [6, 7]  | 0         | 20   | 0         | 25   | 0         | 25   | 0         | 25   | ns   |

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZCS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CS} = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{CS}$  transition LOW.
- $\overline{CS}_{0-3}$ ,  $\overline{CS}_{4-7}$ ,  $\overline{CS}_{8-11}$ , and  $\overline{CS}_{12-15}$  are represented by  $\overline{CS}$  and  $\overline{WE}_U$  and  $\overline{WE}_L$  are represented by  $\overline{WE}$  in the switching characteristics and timing waveforms.

AC Test Loads and Waveforms

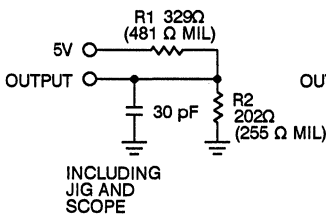


Figure 1a

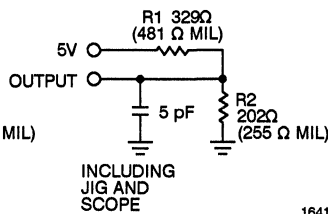


Figure 1b

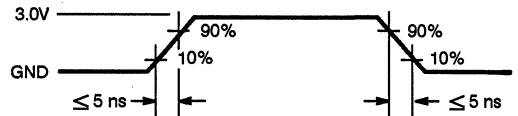
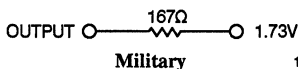


Figure 2

Equivalent to: THEVENIN EQUIVALENT



1641-5



1641-6

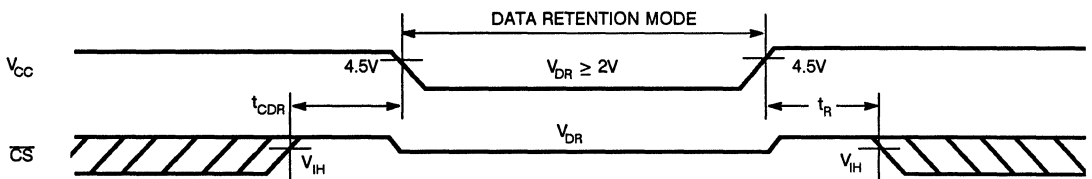
**Data Retention Characteristics (L Version Only)**

| Parameter         | Description                           | Test Conditions  | CYM1641                         |      | Units |
|-------------------|---------------------------------------|--|---------------------------------|------|-------|
|                   |                                       |  | Min.                            | Max. |       |
| V <sub>DR</sub>   | V <sub>CC</sub> for Retention of Data | $V_{CC} = 2.0V,$<br>$\overline{CS} \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$<br>or $V_{IN} \leq 0.2V$ | 2.0                             |      | V     |
| I <sub>CCDR</sub> | Data Retention Current                |  |                                 | 64   | mA    |
| t <sub>CDR</sub>  | Chip Deselect to Data Retention Time  |  | 0                               |      | ns    |
| t <sub>R</sub>    | Operation Recovery Time               |  | t <sub>RC</sub> <sup>[12]</sup> |      | ns    |
| I <sub>LI</sub>   | Input Leakage Current                 |  |                                 | 32   | μA    |

Notes:

12. t<sub>RC</sub> = Read Cycle Time.

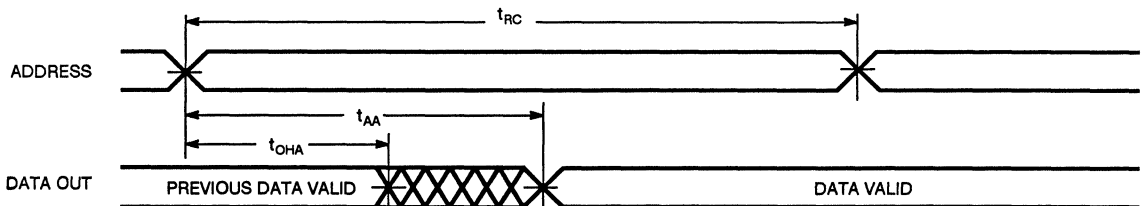
**Data Retention Waveform**



1641-7

**Switching Waveforms<sup>[10, 12]</sup>**

Read Cycle No. 1<sup>[9, 10]</sup>

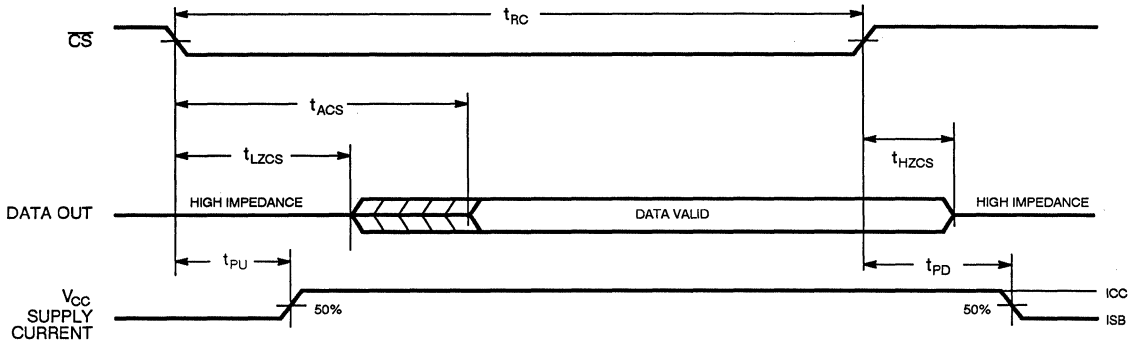


1641-8



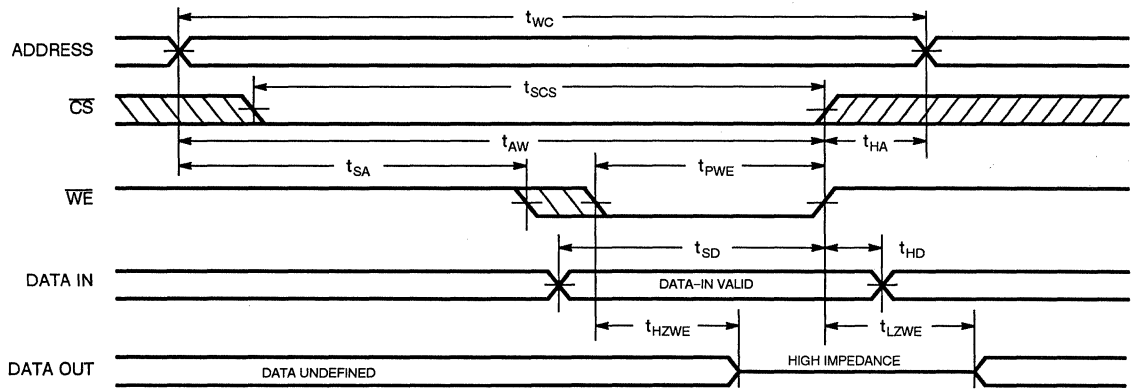
Switching Waveforms (Continued)

Read Cycle No. 2<sup>[9, 10]</sup>



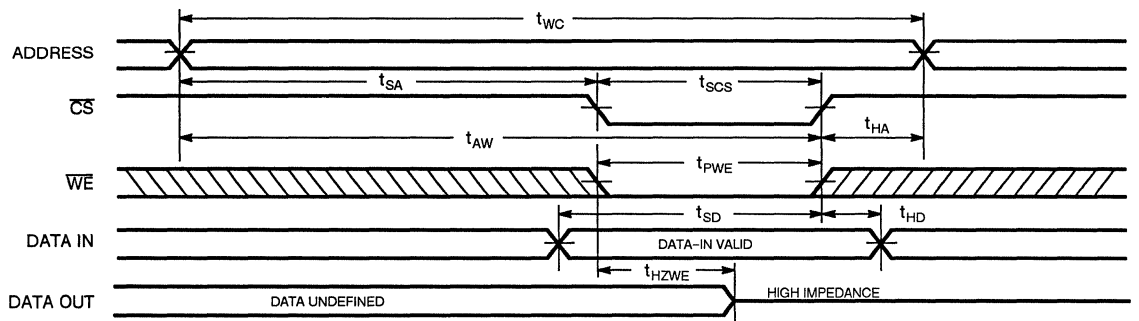
1641-9

Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[8]</sup>



1641-10

Write Cycle No. 2 ( $\overline{CS}$  Controlled)<sup>[8]</sup>



Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

1641-11

### Truth Table

| $\overline{CS}_{xx}$ | $\overline{WE}_n$ | Input/Outputs | Mode                |
|----------------------|-------------------|---------------|---------------------|
| H                    | X                 | High Z        | Deselect Power Down |
| L                    | H                 | Data Out      | Read                |
| L                    | L                 | Data In       | Write               |

2

### Ordering Information

| Speed | Ordering Code   | Package Type | Operating Range |
|-------|-----------------|--------------|-----------------|
| 25    | CYM1641HD-25C   | HD05         | Commercial      |
|       | CYM1641LHD-25C  | HD05         |                 |
| 35    | CYM1641HD-35C   | HD05         | Commercial      |
|       | CYM1641LHD-35C  | HD05         |                 |
|       | CYM1641HD-35MB  | HD05         | Military        |
|       | CYM1641LHD-35MB | HD05         |                 |
| 45    | CYM1641HD-45C   | HD05         | Commercial      |
|       | CYM1641LHD-45C  | HD05         |                 |
|       | CYM1641HD-45MB  | HD05         | Military        |
|       | CYM1641LHD-45MB | HD05         |                 |
| 55    | CYM1641HD-55C   | HD05         | Commercial      |
|       | CYM1641LHD-55C  | HD05         |                 |
|       | CYM1641HD-55MB  | HD05         | Military        |
|       | CYM1641LHD-55MB | HD05         |                 |

Document #: 38-M-00013



# 1K x 32 Static RAM Module with Separate I/O

## Features

- Ideal for Cache Tag Applications
- High speed CMOS SRAMs  
— Access time - 15 ns
- Low active power - 4 W (max)
- SMD Technology
- TTL compatible inputs and outputs
- 84 pin ZIP
- Low profile  
— Max. height - .50 in.
- Small PCB footprint - 1.4 sq in.
- Two cycle reset for cache flush
- Separate WE for "Valid Bits" update

## Functional Description

The CYM1804 is a high performance 32K-bit Static RAM module organized as 1K words by 32 bits. This module is constructed from eight resettable 1K x 4 SRAMs mounted on an epoxy laminate board with pins. The module's reset capability combined with the 15 ns access time makes it ideal for cache tag applications.

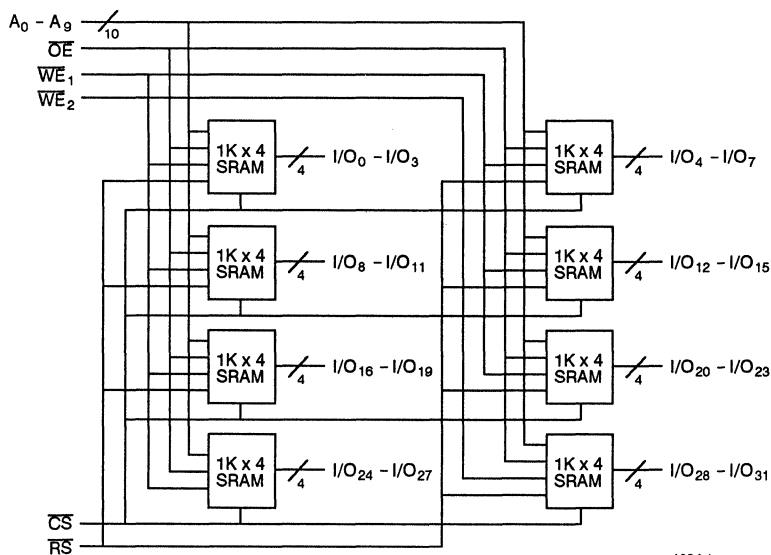
Writing to the module is accomplished when chip select ( $\overline{CS}$ ) and the appropriate write enables ( $WE_1$  and/or  $WE_2$ ) are both LOW. Data on the input pins ( $I_x$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_9$ ).

Reading the device is accomplished by taking the chip select ( $\overline{CS}$ ) LOW, while the write enables ( $WE_n$ ) remain HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output pins ( $O_x$ ).

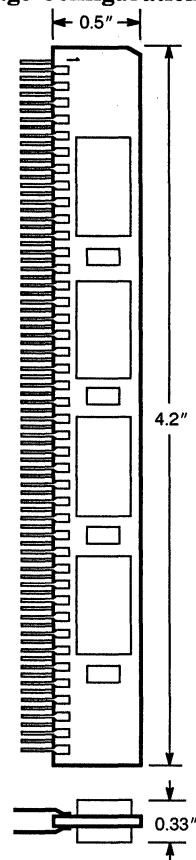
The data output pins stay in the high impedance state whenever chip select ( $\overline{CS}$ ) is HIGH, Reset ( $\overline{RS}$ ) is LOW, output enable ( $\overline{OE}$ ) is HIGH, or during the writing operation when Write Enable ( $WE_n$ ) is LOW.

Reset is initiated by selecting the device ( $\overline{CS} = \text{LOW}$ ) and pulsing the reset ( $\overline{RS}$ ) input LOW. Within two memory cycles all bits are internally cleared to zero.

## Logic Block Diagram



## Package Configuration





# 16K x 32 Static RAM Module

### Features

- High-density 512K bit SRAM Module
- High speed CMOS SRAMs
  - Access time – 25 ns
- Low active power – 4 W (max)
- SMD Technology
- TTL compatible inputs and outputs
- Low profile
  - Max. height – .50 in.
- Small PCB footprint – 1.0 sq in.
- JEDEC compatible pinout
- 2V data retention (L version)

### Functional Description

The CYM1821 is a high performance 512K-bit Static RAM module organized as 16K words by 32 bits. This module is constructed from eight 16K x 4 SRAMs SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ( $\overline{CS}_1$ ,  $\overline{CS}_2$ ,  $\overline{CS}_3$  and  $\overline{CS}_4$ ) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

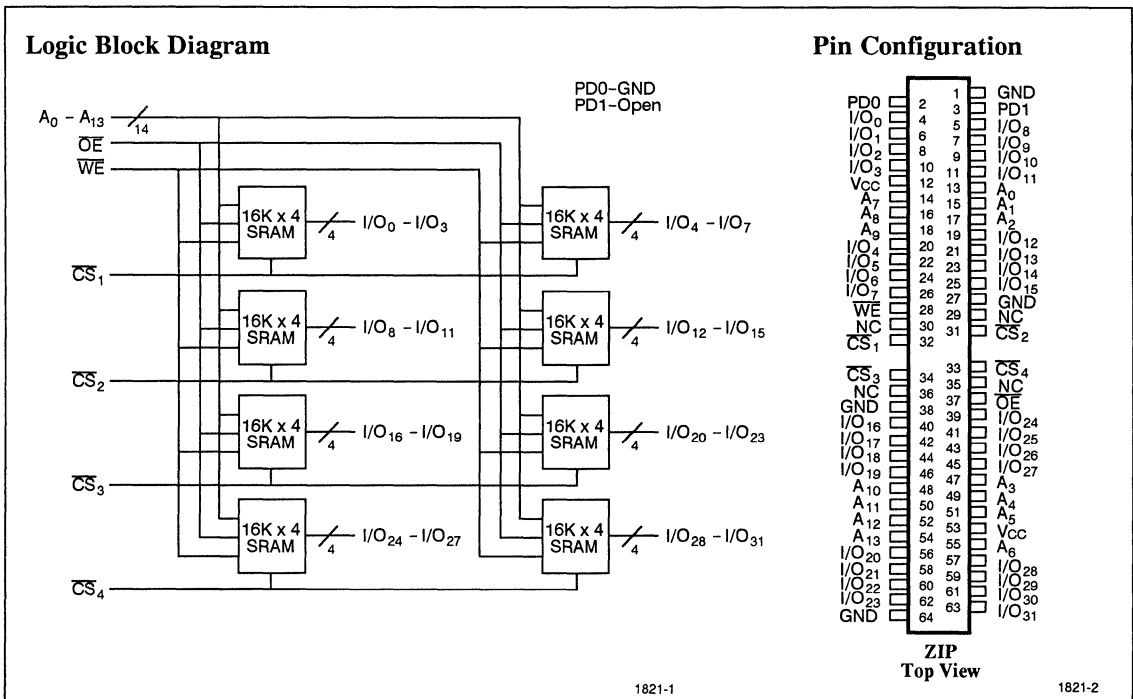
Writing to each byte is accomplished when the appropriate chip selects ( $\overline{CS}_N$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the input/output pins ( $I/O_X$ ) is written into the memory

location specified on the address pins ( $A_0$  through  $A_{13}$ ).

Reading the device is accomplished by taking the chip selects ( $\overline{CS}_N$ ) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins ( $I/O_X$ ).

The data input/output pins stay in the high impedance state when write enable ( $\overline{WE}$ ) is LOW, or the appropriate chip selects are HIGH.

Two pins (PD0 and PD1) are used to identify module memory density in applications where alternate versions of the JEDEC standard modules can be interchanged.



### Selection Guide

|                                | 1821PZ-25 | 1821PZ-35 | 1821PZ-45 |
|--------------------------------|-----------|-----------|-----------|
| Maximum Access time (ns)       | 25        | 35        | 45        |
| Maximum Operating Current (mA) | 720       | 720       | 720       |
| Maximum Standby Current (mA)   | 160       | 160       | 160       |

### Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Supply Voltage to Ground Potential ..... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V  
(Per MIL-STD-883 Method 3015.2)

Latch-up Current ..... >200 mA

### Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C        | 5V ± 10%        |

### Electrical Characteristics Over Operating Range

| Parameters       | Description                                    | Test Conditions   | CYM1821PZ |                 | Units |
|------------------|--|---|-----------|-----------------|-------|
|                  |  |   | Min.      | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                            | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA   | 2.4       |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                             | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA  |           | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                             |   | 2.2       | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage                              |   | -3.0      | 0.8             | V     |
| I <sub>Ix</sub>  | Input Load Current                             | GND ≤ V <sub>i</sub> ≤ V <sub>CC</sub>  | -20       | +20             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                         | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled  | -20       | +20             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>(1)</sup>    | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND  |           | -350            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current       | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS <sub>N</sub> ≤ V <sub>IL</sub>  |           | 720             | mA    |
| I <sub>SB1</sub> | Automatic CS <sup>(2)</sup> Power Down Current | Max. V <sub>CC</sub> ; CS <sub>N</sub> ≥ V <sub>IH</sub><br>Min. Duty Cycle = 100%  |           | 160             | mA    |
| I <sub>SB2</sub> | Automatic CS <sup>(2)</sup> Power Down Current | Max. V <sub>CC</sub> ; CS <sub>N</sub> ≥ V <sub>CC</sub> - 0.3V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V |           | 160             | mA    |

### Capacitance<sup>(3)</sup>

| Parameters       | Description        | Test Conditions   | Max. | Units |
|------------------|--------------------|---|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 70   | pF    |
| C <sub>OUT</sub> | Output Capacitance |   | 35   |       |

Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the CS input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- Tested on a sample basis.

### AC Test Loads and Waveforms

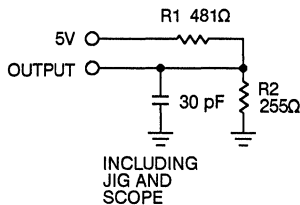


Figure 1a

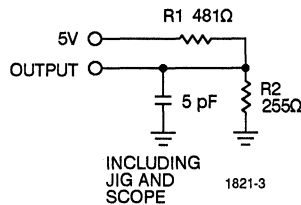


Figure 1b

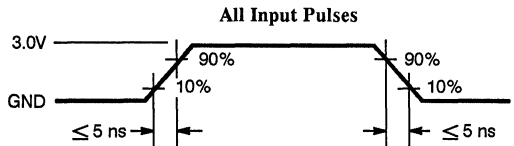
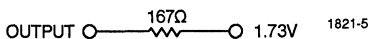


Figure 2

Equivalent to: THEVENIN EQUIVALENT



1821-5

Switching Characteristics Over Operating Range <sup>[4]</sup>

| Parameters                        | Description                                      | 1821PZ-25 |      | 1821PZ-35 |      | 1821PZ-45 |      | Units |
|-----------------------------------|--|-----------|------|-----------|------|-----------|------|-------|
|                                   |  | Min.      | Max. | Min.      | Max. | Min.      | Max. |       |
| <b>READ CYCLE</b>                 |  |           |      |           |      |           |      |       |
| t <sub>RC</sub>                   | Read Cycle Time                                  | 25        |      | 35        |      | 45        |      | ns    |
| t <sub>AA</sub>                   | Address to Data Valid                            |           | 25   |           | 35   |           | 45   | ns    |
| t <sub>OHA</sub>                  | Data Hold from Address Change                    | 3         |      | 3         |      | 3         |      | ns    |
| t <sub>ACS</sub>                  | $\overline{CS}$ LOW to Data Valid                |           | 25   |           | 35   |           | 45   | ns    |
| t <sub>DOE</sub>                  | $\overline{OE}$ LOW to Data Valid                |           | 15   |           | 25   |           | 30   | ns    |
| t <sub>LZOE</sub>                 | $\overline{OE}$ LOW to LOW Z                     | 3         |      | 3         |      | 3         |      | ns    |
| t <sub>HZOE</sub>                 | $\overline{OE}$ HIGH to HIGH Z                   |           | 15   |           | 20   |           | 20   | ns    |
| t <sub>LZCS</sub>                 | $\overline{CS}$ LOW to Low Z <sup>[6]</sup>      | 5         |      | 10        |      | 10        |      | ns    |
| t <sub>HZCS</sub>                 | $\overline{CS}$ HIGH to High Z <sup>[5, 6]</sup> |           | 10   |           | 15   |           | 20   | ns    |
| t <sub>PU</sub>                   | $\overline{CS}$ LOW to Power Up                  | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>PD</sub>                   | $\overline{CS}$ HIGH to Power Down               |           | 25   |           | 35   |           | 45   | ns    |
| <b>WRITE CYCLE <sup>[7]</sup></b> |  |           |      |           |      |           |      |       |
| t <sub>WC</sub>                   | Write Cycle Time                                 | 20        |      | 30        |      | 40        |      | ns    |
| t <sub>SCS</sub>                  | $\overline{CS}$ LOW to Write End                 | 20        |      | 25        |      | 35        |      | ns    |
| t <sub>AW</sub>                   | Address Set-up to Write End                      | 20        |      | 25        |      | 35        |      | ns    |
| t <sub>HA</sub>                   | Address Hold from Write End                      | 2         |      | 2         |      | 2         |      | ns    |
| t <sub>SA</sub>                   | Address Set-up to Write Start                    | 2         |      | 2         |      | 2         |      | ns    |
| t <sub>PWE</sub>                  | $\overline{WE}$ Pulse Width                      | 20        |      | 25        |      | 30        |      | ns    |
| t <sub>SD</sub>                   | Data Set-up to Write End                         | 13        |      | 15        |      | 20        |      | ns    |
| t <sub>HD</sub>                   | Data Hold from Write End                         | 2         |      | 2         |      | 2         |      | ns    |
| t <sub>LZWE</sub>                 | $\overline{WE}$ HIGH to Low Z <sup>[6]</sup>     | 3         |      | 5         |      | 5         |      | ns    |
| t <sub>HZWE</sub>                 | $\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>  | 0         | 7    | 0         | 10   | 0         | 15   | ns    |

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
5. t<sub>HZCS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8.  $\overline{WE}$  is HIGH for read cycle.
9. Device is continuously selected,  $\overline{CS} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .
10. Address valid prior to or coincident with  $\overline{CS}$  transition low.
11.  $\overline{CS}_1$ ,  $\overline{CS}_2$ ,  $\overline{CS}_3$  and  $\overline{CS}_4$  are represented by  $\overline{CS}$  in the switching Characteristics and Waveforms.

**Data Retention Characteristics (L Version Only)**

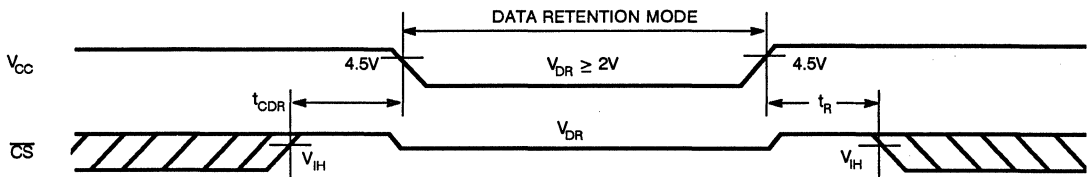
| Parameter        | Description                          | Test Conditions   | CYM1821         |      | Units   |
|------------------|--------------------------------------|---|-----------------|------|---------|
|                  |                                      |   | Min.            | Max. |         |
| $V_{DR}$         | $V_{CC}$ for Retention Data          | $V_{CC} = 2.0V$ ,<br>$\overline{CS} \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$<br>or $V_{IN} \leq 0.2V$ | 2.0             |      | V       |
| $I_{CCDR}$       | Data Retention Current               |   |                 | 8    | mA      |
| $t_{CDR}^{[13]}$ | Chip Deselect to Data Retention Time |   | 0               |      | ns      |
| $t_R^{[13]}$     | Operation Recovery Time              |   | $t_{RC}^{[12]}$ |      | ns      |
| $I_{LI}^{[13]}$  | Input Leakage Current                |   |                 | 10   | $\mu A$ |

Notes:

12.  $t_{RC}$  = Read Cycle Time.

13. Guaranteed, not tested.

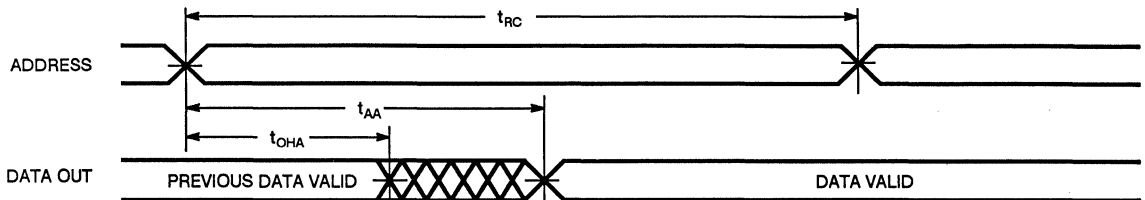
**Data Retention Waveform**



1821-6

**Switching Waveforms<sup>[11]</sup>**

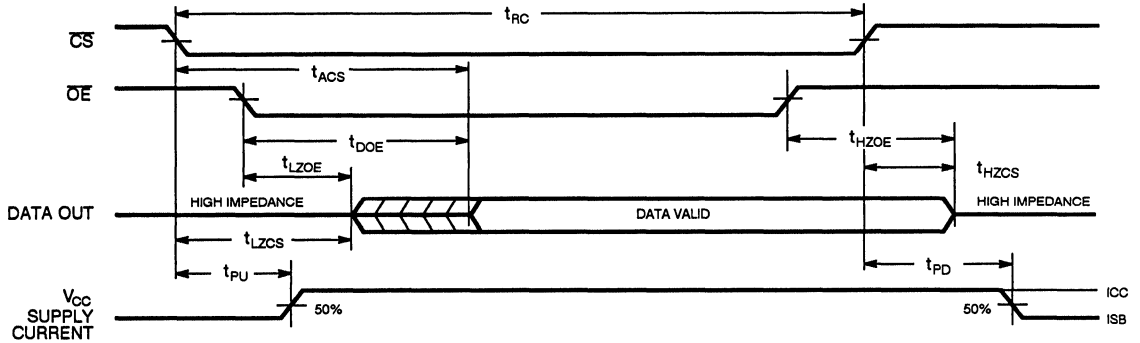
Read Cycle No. 1<sup>[8, 9]</sup>



1821-7

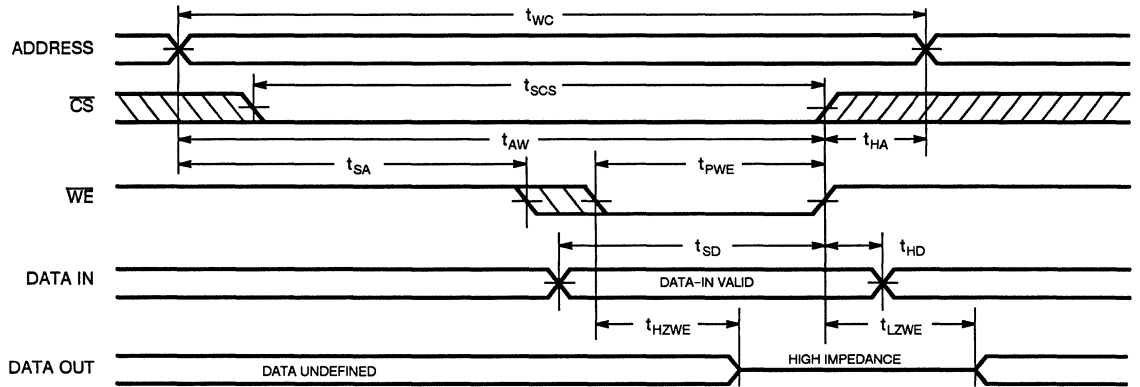
Switching Waveforms (Continued)

Read Cycle No. 2<sup>[8, 10]</sup>



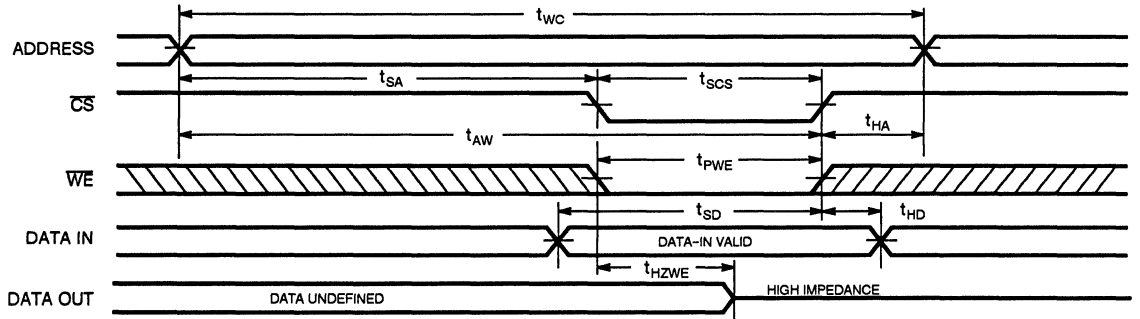
1821-8

Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[7]</sup>



1821-9

Write Cycle No. 2 ( $\overline{CS}$  Controlled)<sup>[7]</sup>



Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

1821-10



**Truth Table**

| $\overline{CS}_N$ | $\overline{WE}$ | $\overline{OE}$ | Input/Outputs | Mode                |
|-------------------|-----------------|-----------------|---------------|---------------------|
| H                 | X               | X               | High Z        | Deselect Power Down |
| L                 | H               | L               | Data Out      | Read                |
| L                 | L               | X               | Data In       | Write               |
| L                 | H               | H               | High Z        | Deselect            |

**Ordering Information**

| Speed | Ordering Code  | Package Type | Operating Range |
|-------|----------------|--------------|-----------------|
| 25    | CYM1821PZ-25C  | PZ01         | Commercial      |
|       | CYM1821LPZ-25C | PZ01         |                 |
| 35    | CYM1821PZ-35C  | PZ01         |                 |
|       | CYM1821LPZ-35C | PZ01         |                 |
| 45    | CYM1821PZ-45C  | PZ01         |                 |
|       | CYM1821LPZ-45C | PZ01         |                 |

Document #: 38-M-00015



# 16K x 32 Static RAM Module with Separate I/O

### Features

- High-density 512K bit SRAM Module
- High speed CMOS SRAMs  
— Access time – 25 ns
- Low active power – 4 W (max)
- Hermetic SMD Technology
- TTL compatible inputs and outputs
- Low profile  
— Max. height – .52 in.
- Small PCB footprint – 1.0 sq in.
- 2V data retention (L version)

### Functional Description

The CYM1822 is a high performance 512K-bit Static RAM module organized as 16K words by 32 bits. This module is constructed from eight 16K x 4 Separate I/O SRAMs in Leadless Chip Carriers mounted on a ceramic substrate with pins. Two chip selects ( $\overline{CS}_U$  and  $\overline{CS}_L$ ) are used to independently enable the upper and lower 16-bit Data words.

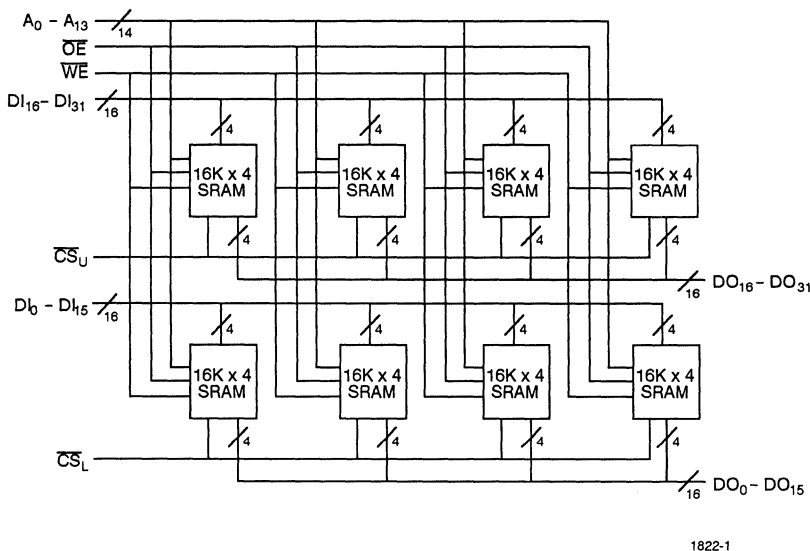
Writing to the device is accomplished when the chip selects ( $\overline{CS}_U$  and/or  $\overline{CS}_L$ ) and write enable ( $\overline{WE}$ ) inputs are both

LOW. Data on the input pins ( $DI_x$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{15}$ ).

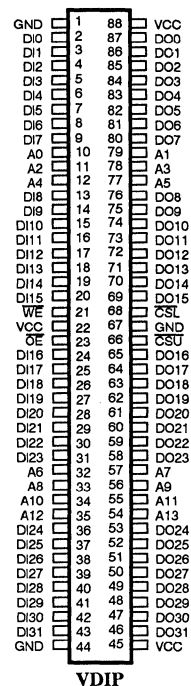
Reading the device is accomplished by taking the chip selects ( $\overline{CS}_U$  and/or  $\overline{CS}_L$ ) and output enable ( $\overline{OE}$ ) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output pins ( $DO_x$ ).

The output pins stay in the high impedance state when write enable ( $\overline{WE}$ ) is LOW, the appropriate chip selects are HIGH, or  $\overline{OE}$  is HIGH.

### Logic Block Diagram



### Pin Configuration



### Selection Guide

|                                |            | 1822HV-25 | 1822HV-30 | 1822HV-35 | 1822HV-45 |
|--------------------------------|------------|-----------|-----------|-----------|-----------|
| Maximum Access time (ns)       |            | 25        | 30        | 35        | 45        |
| Maximum Operating Current (mA) | Commercial | 720       | 720       | 720       | 720       |
|                                | Military   |           | 720       | 720       | 720       |
| Maximum Standby Current (mA)   | Commercial | 160       | 160       | 160       | 160       |
|                                | Military   |           | 160       | 160       | 160       |

## Maximum Ratings

(Above which the useful life may be impaired)

|  |                 |
|--|-----------------|
| Storage Temperature .....                              | -65°C to +150°C |
| Ambient Temperature with<br>Power Applied .....        | -55°C to +125°C |
| Supply Voltage to Ground Potential .....               | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs<br>in High Z State ..... | -0.5V to +7.0V  |
| DC Input Voltage .....                                 | -3.0V to +7.0V  |
| Output Current into Outputs (Low) .....                | 20 mA           |

Static Discharge Voltage ..... >2001V  
(Per MIL-STD-883 Method 3015.2)

Latch-up Current ..... >200 mA

## Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C        | 5V ± 10%        |
| Military   | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over Operating Range

| Parameters       | Description                                    | Test Conditions   | CYM1822HV |                 | Units |
|------------------|--|---|-----------|-----------------|-------|
|                  |  |   | Min.      | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                            | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA   | 2.4       |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                             | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA  |           | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                             |   | 2.2       | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage                              |   | -3.0      | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current                             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>  | -20       | +20             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                         | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled  | -20       | +20             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>    | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND  |           | -350            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current       | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS <sub>L</sub> , CS <sub>U</sub> ≤ V <sub>IL</sub>  |           | 720             | mA    |
| I <sub>SB1</sub> | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> ; CS <sub>U</sub> , CS <sub>L</sub> ≥ V <sub>IH</sub><br>Min. Duty Cycle = 100%  |           | 160             | mA    |
| I <sub>SB2</sub> | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> ; CS <sub>U</sub> , CS <sub>L</sub> ≥ V <sub>CC</sub> - 0.3V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V |           | 160             | mA    |

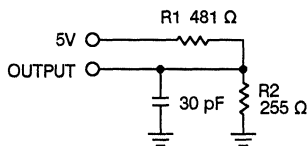
## Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions   | Max. | Units |
|------------------|--------------------|---|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 70   | pF    |
| C <sub>OUT</sub> | Output Capacitance |   | 35   |       |

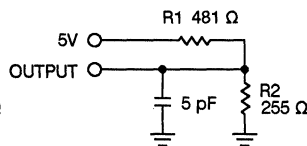
### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the CE input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- Tested on a sample basis.

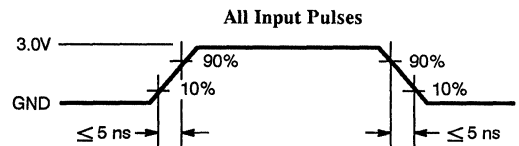
## AC Test Loads and Waveforms



INCLUDING  
JIG AND  
SCOPE  
Figure 1a

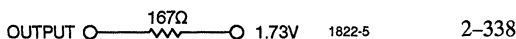


INCLUDING  
JIG AND  
SCOPE  
1822-3  
Figure 1b



1822-4  
Figure 2

Equivalent to: THEVENIN EQUIVALENT



1822-5

2-338

Switching Characteristics Over Operating Range <sup>[4]</sup>

| Parameters                        | Description                                      | 1822HV-25 |      | 1822HV-30 |      | 1822HV-35 |      | 1822HV-45 |      | Units |
|-----------------------------------|--|-----------|------|-----------|------|-----------|------|-----------|------|-------|
|                                   |  | Min.      | Max. | Min.      | Max. | Min.      | Max. | Min.      | Max. |       |
| <b>READ CYCLE</b>                 |  |           |      |           |      |           |      |           |      |       |
| t <sub>RC</sub>                   | Read Cycle Time                                  | 25        |      | 30        |      | 35        |      | 45        |      | ns    |
| t <sub>AA</sub>                   | Address to Data Valid                            |           | 25   |           | 30   |           | 35   |           | 45   | ns    |
| t <sub>OHA</sub>                  | Data Hold from Address Change                    | 5         |      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>ACS</sub>                  | $\overline{CS}$ LOW to Data Valid                |           | 25   |           | 30   |           | 35   |           | 45   | ns    |
| t <sub>DOE</sub>                  | $\overline{OE}$ LOW to Data Valid                |           | 15   |           | 20   |           | 25   |           | 30   | ns    |
| t <sub>LZOE</sub>                 | $\overline{OE}$ LOW to LOW Z                     | 3         |      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>HZOE</sub>                 | $\overline{OE}$ HIGH to HIGH Z                   |           | 15   |           | 20   |           | 20   |           | 20   | ns    |
| t <sub>LZCS</sub>                 | $\overline{CS}$ LOW to Low Z <sup>[6]</sup>      | 5         |      | 10        |      | 10        |      | 10        |      | ns    |
| t <sub>HZCS</sub>                 | $\overline{CS}$ HIGH to High Z <sup>[5, 6]</sup> |           | 10   |           | 15   |           | 15   |           | 20   | ns    |
| t <sub>PU</sub>                   | $\overline{CS}$ LOW to Power Up                  | 0         |      | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>PD</sub>                   | $\overline{CS}$ HIGH to Power Down               |           | 25   |           | 30   |           | 35   |           | 45   | ns    |
| <b>WRITE CYCLE <sup>[7]</sup></b> |  |           |      |           |      |           |      |           |      |       |
| t <sub>WC</sub>                   | Write Cycle Time                                 | 20        |      | 25        |      | 25        |      | 35        |      | ns    |
| t <sub>SCS</sub>                  | $\overline{CS}$ LOW to Write End                 | 20        |      | 25        |      | 30        |      | 40        |      | ns    |
| t <sub>AW</sub>                   | Address Set-up to Write End                      | 20        |      | 25        |      | 30        |      | 40        |      | ns    |
| t <sub>HA</sub>                   | Address Hold from Write End                      | 2         |      | 2         |      | 2         |      | 2         |      | ns    |
| t <sub>SA</sub>                   | Address Set-up to Write Start                    | 2         |      | 2         |      | 2         |      | 2         |      | ns    |
| t <sub>PWE</sub>                  | $\overline{WE}$ Pulse Width                      | 20        |      | 25        |      | 25        |      | 30        |      | ns    |
| t <sub>SD</sub>                   | Data Set-up to Write End                         | 13        |      | 20        |      | 20        |      | 25        |      | ns    |
| t <sub>HD</sub>                   | Data Hold from Write End                         | 3         |      | 3         |      | 3         |      | 3         |      | ns    |
| t <sub>LZWE</sub>                 | $\overline{WE}$ HIGH to Low Z <sup>[6]</sup>     | 3         |      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>HZWE</sub>                 | $\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>  | 0         | 7    | 0         | 12   | 0         | 12   | 0         | 15   | ns    |

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZCS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device. These parameters are guaranteed and not 100% tested.
- The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CS} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{CS}$  transition low.
- Both  $\overline{CS}_L$  and  $\overline{CS}_U$  are represented by  $\overline{CS}$  in the switching Characteristics and Waveforms.

**Data Retention Characteristics (L Version Only)**

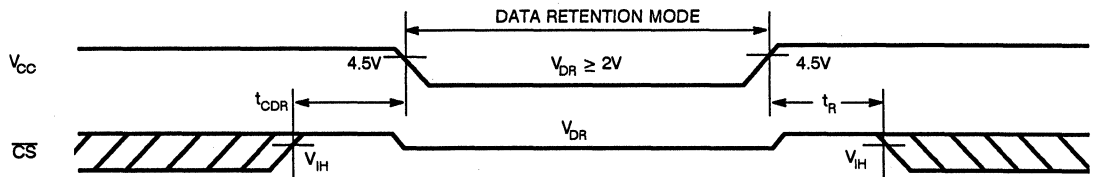
| Parameter        | Description                          | Test Conditions  | CYM1822         |      | Units   |
|------------------|--------------------------------------|--|-----------------|------|---------|
|                  |                                      |  | Min.            | Max. |         |
| $V_{DR}$         | $V_{CC}$ for Retention Data          | $V_{CC} = 2.0V,$<br>$\overline{CS} \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$<br>or $V_{IN} \leq 0.2V$ | 2.0             |      | V       |
| $I_{CCDR}$       | Data Retention Current               |  |                 | 8    | mA      |
| $t_{CDR}^{[13]}$ | Chip Deselect to Data Retention Time |  | 0               |      | ns      |
| $t_R^{[13]}$     | Operation Recovery Time              |  | $t_{RC}^{[12]}$ |      | ns      |
| $I_{LI}^{[13]}$  | Input Leakage Current                |  |                 | 10   | $\mu A$ |

Notes:

12.  $t_{RC}$  = Read Cycle Time.

13. Guaranteed, not tested.

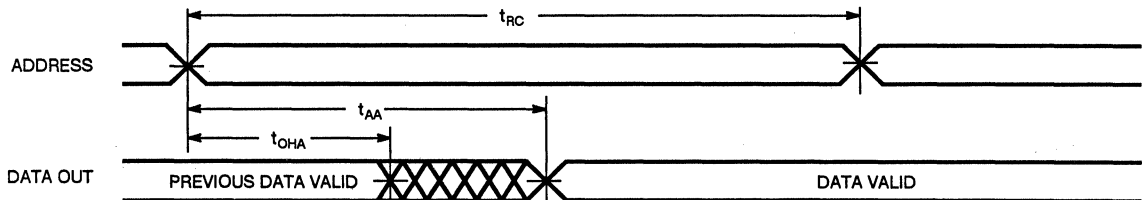
**Data Retention Waveform**



1822-6

**Switching Waveforms<sup>[11]</sup>**

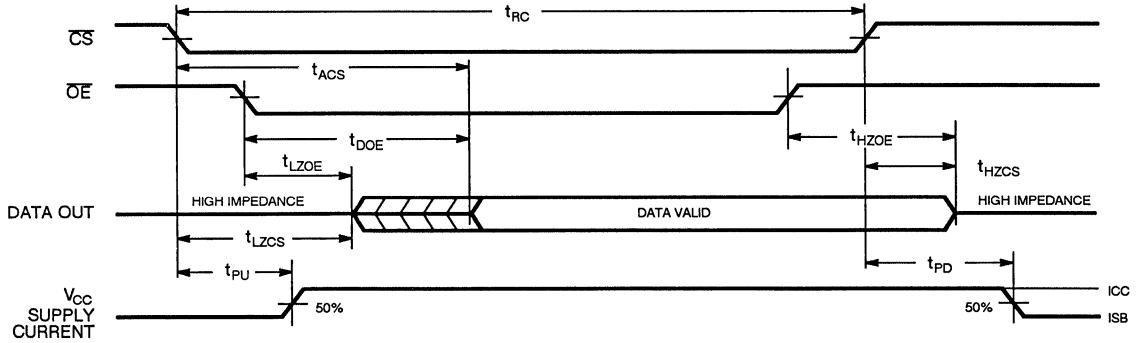
Read Cycle No. 1<sup>[8,9]</sup>



1822-7

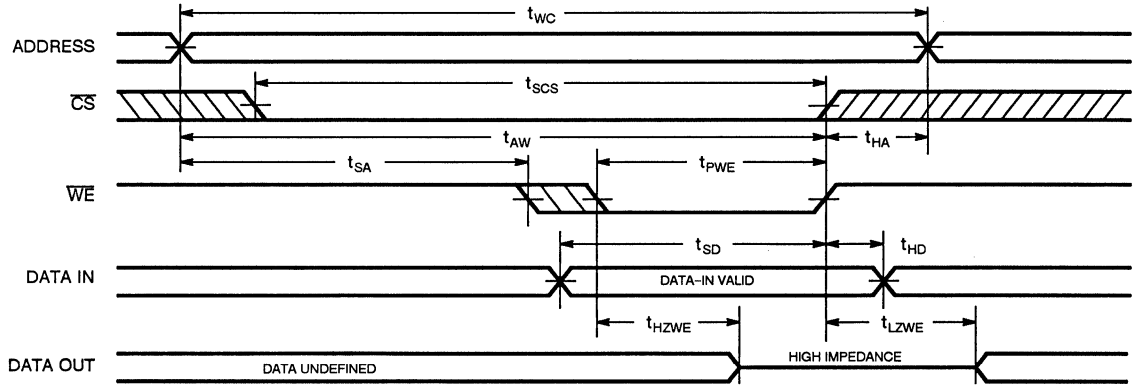
Switching Waveforms (Continued)

Read Cycle No. 2<sup>[8, 10]</sup>



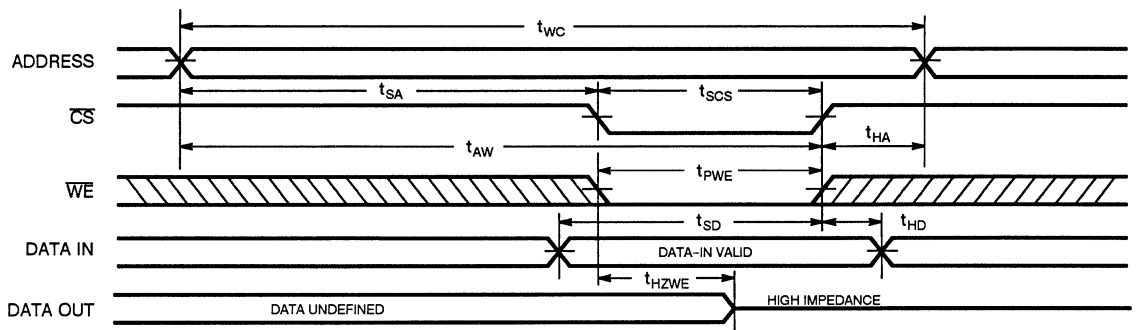
1822-8

Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[7]</sup>



1822-9

Write Cycle No. 2 ( $\overline{CS}$  Controlled)<sup>[7]</sup>



Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

1822-10

**Truth Table**

| $\overline{CS}_U$ | $\overline{CS}_L$ | $\overline{OE}$ | $\overline{WE}$ | Input/Outputs             | Mode                |
|-------------------|-------------------|-----------------|-----------------|---------------------------|---------------------|
| H                 | H                 | X               | X               | High Z                    | Deselect Power Down |
| L                 | L                 | L               | H               | Data Out <sub>0-31</sub>  | Read                |
| H                 | L                 | L               | H               | Data Out <sub>0-15</sub>  | Read Lower Word     |
| L                 | H                 | L               | H               | Data Out <sub>16-31</sub> | Read Upper Word     |
| L                 | L                 | X               | L               | Data In <sub>0-31</sub>   | Write               |
| H                 | L                 | X               | L               | Data In <sub>0-15</sub>   | Write Lower Word    |
| L                 | H                 | X               | L               | Data In <sub>16-31</sub>  | Write Upper Word    |
| L                 | L                 | H               | H               | High Z                    | Deselect            |
| H                 | L                 | H               | H               | High Z                    | Deselect            |
| L                 | H                 | H               | H               | High Z                    | Deselect            |

**Ordering Information**

| Speed | Ordering Code   | Package Type | Operating Range |
|-------|-----------------|--------------|-----------------|
| 25    | CYM1822HV-25C   | HV02         | Commercial      |
|       | CYM1822LHV-25C  | HV02         |                 |
| 30    | CYM1822HV-30C   | HV02         | Commercial      |
|       | CYM1822LHV-30C  | HV02         |                 |
|       | CYM1822HV-30MB  | HV02         | Military        |
|       | CYM1822LHV-30MB | HV02         |                 |
| 35    | CYM1822HV-35C   | HV02         | Commercial      |
|       | CYM1822LHV-35C  | HV02         |                 |
|       | CYM1822HV-35MB  | HV02         | Military        |
|       | CYM1822LHV-35MB | HV02         |                 |
| 45    | CYM1822HV-45C   | HV02         | Commercial      |
|       | CYM1822LHV-45C  | HV02         |                 |
|       | CYM1822HV-45MB  | HV02         | Military        |
|       | CYM1822LHV-45MB | HV02         |                 |

Document #: 38-M-00016



# 64K x 32 Static RAM Module

## Features

- High-density 2 Megabit SRAM Module
- High speed CMOS SRAMs
  - Access time – 25 ns
- Independent byte and word controls
- Low active power – 4.8 W (max)
- Hermetic SMD technology
- TTL compatible inputs and outputs
- Low profile
  - Max. height – .270 in.
- Small PCB footprint – 1.8 sq in.
- 2 V data retention (L version)

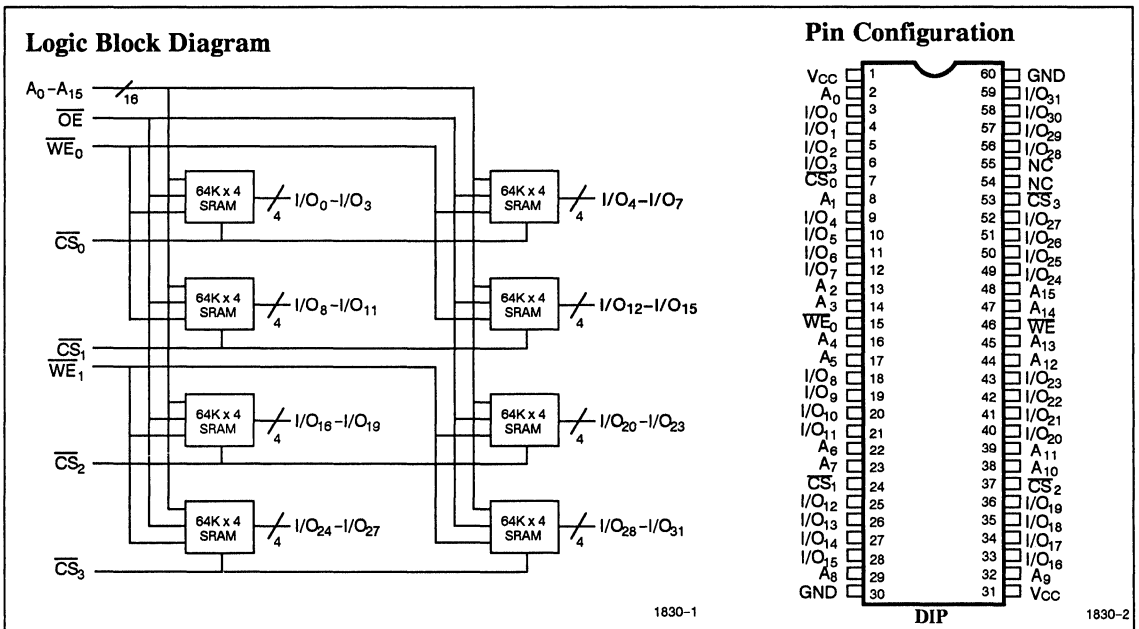
## Functional Description

The CYM1830 is a high performance 2M-bit Static RAM module organized as 64K words by 32 bits. This module is constructed from eight 64K x 4 SRAMs in LCC packages mounted on a ceramic substrate with pins. Four chip selects ( $\overline{CS}_0$ ,  $\overline{CS}_1$ ,  $\overline{CS}_2$  and  $\overline{CS}_3$ ) are used to independently enable the four bytes. Two write enables ( $\overline{WE}_0$  and  $\overline{WE}_1$ ) are used to independently write to either upper or lower 16 bit word of RAM. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects and write enables. Writing to each byte is accomplished when the appropriate chip select ( $\overline{CS}_x$ )

and write enable ( $\overline{WE}_x$ ) inputs are both LOW. Data on the input/output pins ( $I/O_x$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Reading the device is accomplished by taking the chip selects ( $\overline{CS}_x$ ) LOW, while write enables ( $\overline{WE}_x$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins ( $I/O_x$ ).

The Data input/output pins stay in the high impedance state when write enables ( $\overline{WE}_x$ ) are LOW, or the appropriate chip selects are HIGH.



## Selection Guide

|                                |            | 1830HD-30 | 1830HD-35 | 1830HD-45 | 1830HD-55 |
|--------------------------------|------------|-----------|-----------|-----------|-----------|
| Maximum Access time (ns)       |            | 30        | 35        | 45        | 55        |
| Maximum Operating Current (mA) | Commercial | 880       | 880       | 880       | 880       |
|                                | Military   |           | 880       | 880       | 880       |
| Maximum Standby Current (mA)   | Commercial | 320       | 320       | 320       | 320       |
|                                | Military   |           | 320       | 320       | 320       |



### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines not tested.)

|  |                 |
|--|-----------------|
| Storage Temperature .....                              | -65°C to +150°C |
| Ambient Temperature with<br>Power Applied .....        | -55°C to +125°C |
| Supply Voltage to Ground Potential .....               | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs<br>in High Z State ..... | -0.5V to +7.0V  |
| DC Input Voltage .....                                 | -0.5V to +70V   |
| Output Current into Outputs (Low) .....                | 20 mA           |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | > 2001V<br>(Per MIL-STD-883 Method 3015) |
| Latch-up Current .....         | > 200 mA                                 |

### Operating Range

| Range        | Ambient Temperature | V <sub>CC</sub> |
|--------------|---------------------|-----------------|
| Commercial   | 0°C to +70°C        | 5V ± 10%        |
| Military [4] | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range

| Parameters       | Description   | Test Conditions  | CYM1830HD |                 | Units |
|------------------|---|--|-----------|-----------------|-------|
|                  |   |  | Min.      | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                                 | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA  | 2.4       |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                                  | V <sub>CC</sub> = Min.<br>I <sub>OL</sub> = 8.0 mA Military<br>I <sub>OL</sub> = 12.0 mA Commercial                                    |           | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                                  |  | 2.2       | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage                                   |  | 0.5       | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current                                  | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -20       | +20             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                              | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled   | -10       | 10              | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>         | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND   |           | -350            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current by 16 mode | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS <sub>x</sub> ≤ V <sub>IL</sub>   |           | 880             | mA    |
| I <sub>SB1</sub> | Automatic CS <sup>[2]</sup><br>Power Down Current   | Max. V <sub>CC</sub> , CS <sub>x</sub> ≥ V <sub>IH</sub><br>Min. Duty Cycle = 100%   |           | 320             | mA    |
| I <sub>SB2</sub> | Automatic CS <sup>[2]</sup><br>Power Down Current   | Max. V <sub>CC</sub> , CS <sub>x</sub> ≥ V <sub>CC</sub> - 0.3V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V |           | 160             | mA    |

### Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 90   | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 30   |       |

#### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the CS input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.

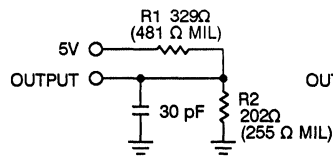
Switching Characteristics Over Operating Range <sup>[5]</sup>

| Parameters                        | Description                                      | 1830HD-30 |      | 1830HD-35 |      | 1830HD-45 |      | 1830HD-55 |      | Unit |
|-----------------------------------|--|-----------|------|-----------|------|-----------|------|-----------|------|------|
|                                   |  | Min.      | Max. | Min.      | Max. | Min.      | Max. | Min.      | Max. |      |
| <b>READ CYCLE</b>                 |  |           |      |           |      |           |      |           |      |      |
| t <sub>RC</sub>                   | Read Cycle Time                                  | 30        |      | 35        |      | 45        |      | 55        |      | ns   |
| t <sub>AA</sub>                   | Address to Data Valid                            |           | 30   |           | 35   |           | 45   |           | 55   | ns   |
| t <sub>OHA</sub>                  | Output Hold from Address Change                  | 3         |      | 3         |      | 3         |      | 3         |      | ns   |
| t <sub>ACS</sub>                  | $\overline{CS}$ LOW to Data Valid                |           | 30   |           | 35   |           | 45   |           | 55   | ns   |
| t <sub>LZCS</sub>                 | $\overline{CS}$ LOW to Low Z <sup>[7]</sup>      | 3         |      | 3         |      | 3         |      | 3         |      | ns   |
| t <sub>HZCS</sub>                 | $\overline{CS}$ HIGH to High Z <sup>[6, 7]</sup> |           | 15   |           | 20   |           | 20   |           | 20   | ns   |
| t <sub>PU</sub>                   | $\overline{CS}$ LOW to Power Up                  | 0         |      | 0         |      | 0         |      | 0         |      | ns   |
| t <sub>PD</sub>                   | $\overline{CS}$ HIGH to Power Down               |           | 30   |           | 35   |           | 45   |           | 55   | ns   |
| <b>WRITE CYCLE <sup>[8]</sup></b> |  |           |      |           |      |           |      |           |      |      |
| t <sub>WC</sub>                   | Write Cycle Time                                 | 30        |      | 35        |      | 45        |      | 55        |      | ns   |
| t <sub>SCS</sub>                  | $\overline{CS}$ LOW to Write End                 | 25        |      | 30        |      | 40        |      | 40        |      | ns   |
| t <sub>AW</sub>                   | Address Set-up to Write End                      | 25        |      | 30        |      | 40        |      | 40        |      | ns   |
| t <sub>HA</sub>                   | Address Hold from Write End                      | 2         |      | 2         |      | 2         |      | 2         |      | ns   |
| t <sub>SA</sub>                   | Address Set-up to Write Start                    | 2         |      | 2         |      | 2         |      | 2         |      | ns   |
| t <sub>PWE</sub>                  | $\overline{WE}$ Pulse Width                      | 25        |      | 25        |      | 30        |      | 40        |      | ns   |
| t <sub>SD</sub>                   | Data Set-up to Write End                         | 20        |      | 20        |      | 25        |      | 25        |      | ns   |
| t <sub>HD</sub>                   | Data Hold from Write End                         | 2         |      | 2         |      | 2         |      | 2         |      | ns   |
| t <sub>LZWE</sub>                 | $\overline{WE}$ HIGH to Low Z <sup>[7]</sup>     | 3         |      | 3         |      | 3         |      | 3         |      | ns   |
| t <sub>HZWE</sub>                 | $\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>  | 0         | 20   | 0         | 20   | 0         | 20   | 0         | 20   | ns   |

Notes:

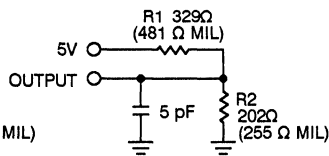
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZCS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CS} = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{CS}$  transition LOW.

AC Test Loads and Waveforms



INCLUDING  
JIG AND  
SCOPE

Figure 1a



INCLUDING  
JIG AND  
SCOPE

Figure 1b

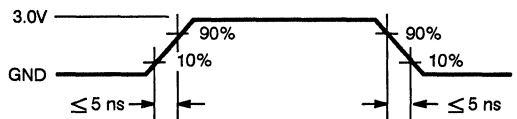
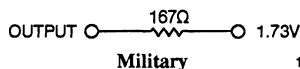


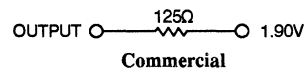
Figure 2

Equivalent to: THEVENIN EQUIVALENT



Military

1830-5



Commercial

1830-6

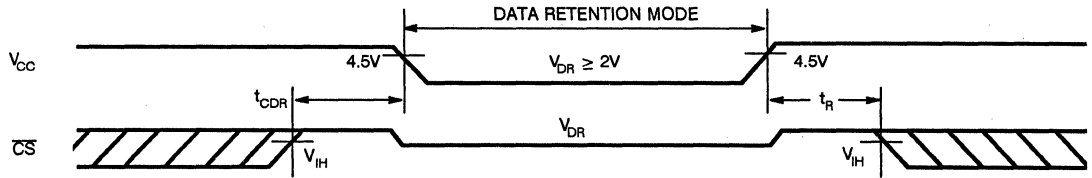
Data Retention Characteristics (L Version Only)

| Parameter  | Description                          | Test Conditions  | CYM1830         |      | Units   |
|------------|--------------------------------------|--|-----------------|------|---------|
|            |                                      |  | Min.            | Max. |         |
| $V_{DR}$   | $V_{CC}$ for Retention of Data       | $V_{CC} = 2.0V,$<br>$\overline{CS} \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$<br>or $V_{IN} \leq 0.2V$ | 2.0             |      | V       |
| $I_{CCDR}$ | Data Retention Current               |  |                 | 32   | mA      |
| $t_{CDR}$  | Chip Deselect to Data Retention Time |  | 0               |      | ns      |
| $t_R$      | Operation Recovery Time              |  | $t_{RC}^{[12]}$ |      | ns      |
| $I_{LI}$   | Input Leakage Current                |  |                 | 8    | $\mu A$ |

Notes:

12.  $t_{RC}$  = Read Cycle Time.

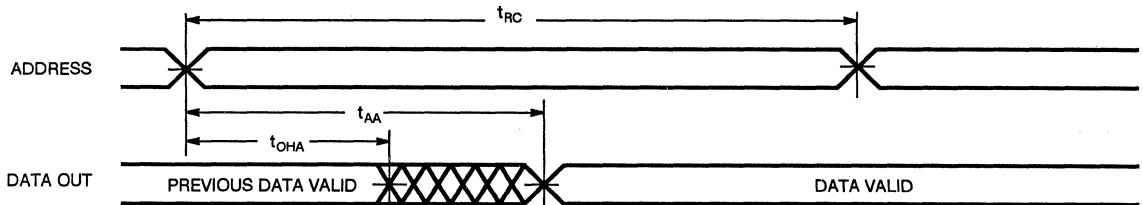
Data Retention Waveform



1830-7

Switching Waveforms<sup>[10]</sup>

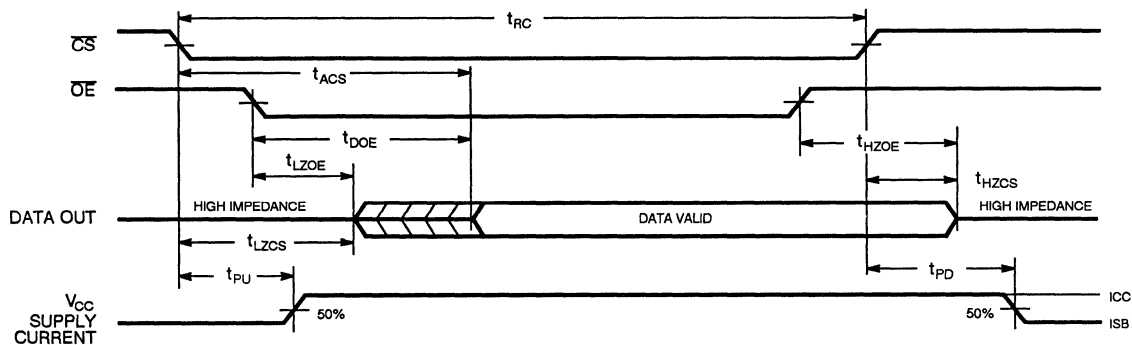
Read Cycle No. 1<sup>[9, 10]</sup>



1830-8

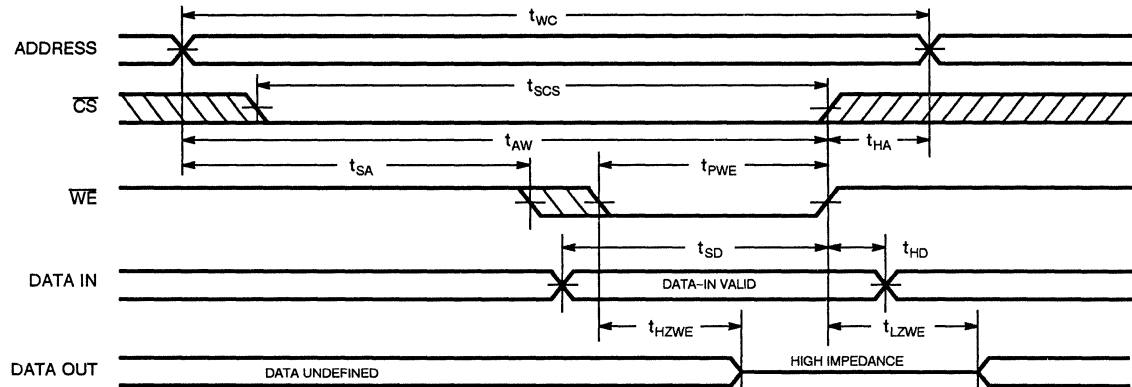
### Switching Waveforms (Continued)

Read Cycle No. 2<sup>[9, 10]</sup>



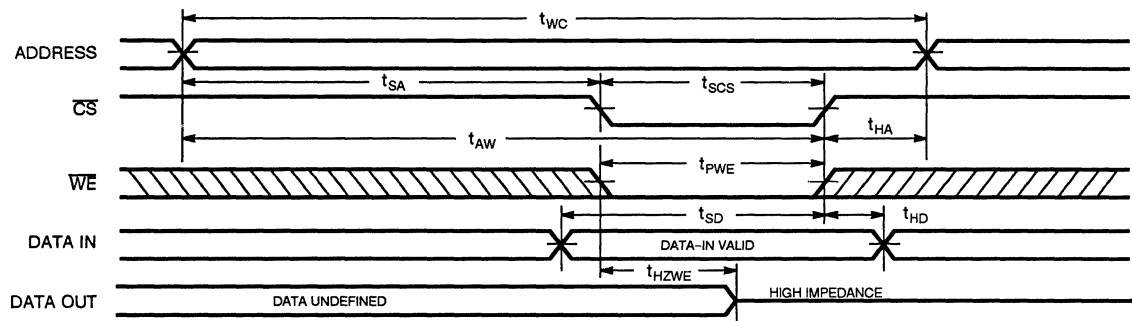
1830-9

Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[8]</sup>



1830-10

Write Cycle No. 2 ( $\overline{CS}$  Controlled)<sup>[8]</sup>



Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

1830-11

**Truth Table**

| $\overline{CS}_x$ | $\overline{WE}_x$ | Input/Outputs | Mode                |
|-------------------|-------------------|---------------|---------------------|
| H                 | X                 | High Z        | Deselect Power Down |
| L                 | H                 | Data Out      | Read                |
| L                 | L                 | Data In       | Write               |

**Ordering Information**

| Speed | Ordering Code | Package Type | Operating Range |
|-------|---------------|--------------|-----------------|
| 30    | M1830HD-30C   | HD06         | Commercial      |
|       | M1830LHD-30C  | HD06         |                 |
| 35    | M1830HD-35C   | HD06         | Commercial      |
|       | M1830LHD-35C  | HD06         |                 |
|       | M1830HD-35MB  | HD06         | Military        |
|       | M1830LHD-35MB | HD06         |                 |
| 45    | M1830HD-45C   | HD06         | Commercial      |
|       | M1830LHD-45C  | HD06         |                 |
|       | M1830HD-45MB  | HD06         | Military        |
|       | M1830LHD-45MB | HD06         |                 |
| 55    | M1830HD-55C   | HD06         | Commercial      |
|       | M1830LHD-55C  | HD06         |                 |
|       | M1830HD-55MB  | HD06         | Military        |
|       | M1830LHD-55MB | HD06         |                 |

Document #: 38-M-00017



# 64K x 32 Static RAM Module

## Features

- High-density 2M bit SRAM Module
- High speed CMOS SRAMs  
— Access time – 25 ns
- Low active power – 4 W (max)
- SMD Technology
- TTL compatible inputs and outputs
- Low profile  
— Max. height – .50 in.
- Small PCB footprint – 1.2 sq in.
- JEDEC compatible pinout
- 2V data retention (L version)

## Functional Description

The CYM1831 is a high performance 2M-bit Static RAM module organized as 64K words by 32 bits. This module is constructed from eight 64K x 4 SRAMs SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ( $\overline{CS}_1$ ,  $\overline{CS}_2$ ,  $\overline{CS}_3$  and  $\overline{CS}_4$ ) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

Writing to each byte is accomplished when the appropriate chip selects ( $\overline{CS}_N$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the input/output pins ( $I/O_X$ ) is written into the memory

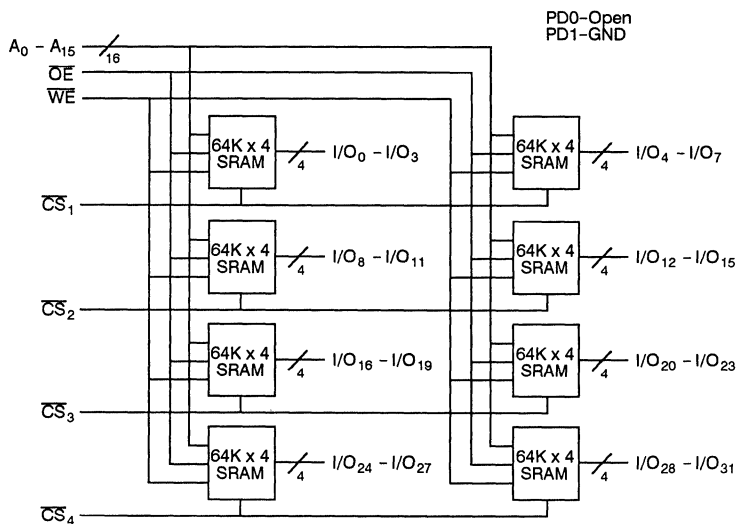
location specified on the address pins ( $A_0$  through  $A_{15}$ ).

Reading the device is accomplished by taking the chip selects ( $\overline{CS}_N$ ) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins ( $I/O_X$ ).

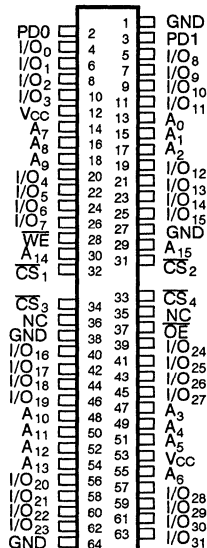
The data input/output pins stay in the high impedance state when write enable ( $\overline{WE}$ ) is LOW, or the appropriate chip selects are HIGH.

Two pins (PD0 and PD1) are used to identify module memory density in applications where alternate versions of the JEDEC standard modules can be interchanged.

## Logic Block Diagram



## Pin Configuration



ZIP  
Top View

1831-1

1831-2

## Selection Guide

|                                | 1831PZ-25 | 1831PZ-35 | 1831PZ-45 |
|--------------------------------|-----------|-----------|-----------|
| Maximum Access time (ns)       | 25        | 35        | 45        |
| Maximum Operating Current (mA) | 720       | 720       | 720       |
| Maximum Standby Current (mA)   | 160       | 160       | 160       |

### Maximum Ratings

(Above which the useful life may be impaired)

|   |                 |
|---|-----------------|
| Storage Temperature .....                           | -65°C to +150°C |
| Ambient Temperature with Power Applied .....        | 0°C to +70°C    |
| Supply Voltage to Ground Potential .....            | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State ..... | -0.5V to +7.0V  |
| DC Input Voltage .....                              | -3.0V to +7.0V  |
| Output Current into Outputs (Low) .....             | 20 mA           |

Static Discharge Voltage ..... >2001V  
(Per MIL-STD-883 Method 3015.2)

Latch-up Current ..... >200 mA

### Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C        | 5V ± 10%        |

### Electrical Characteristics Over Operating Range

| Parameters       | Description                                    | Test Conditions   | CYM1831PZ |                 | Units |
|------------------|--|---|-----------|-----------------|-------|
|                  |  |   | Min.      | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                            | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA   | 2.4       |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                             | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA  |           | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                             |   | 2.2       | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage                              |   | -3.0      | 0.8             | V     |
| I <sub>Ix</sub>  | Input Load Current                             | GND ≤ V <sub>i</sub> ≤ V <sub>CC</sub>  | -20       | +20             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                         | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled  | -20       | +20             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup>    | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND  |           | -350            | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current       | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS <sub>N</sub> ≤ V <sub>IL</sub>  |           | 720             | mA    |
| I <sub>SB1</sub> | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> ; CS <sub>N</sub> ≥ V <sub>IH</sub><br>Min. Duty Cycle = 100%  |           | 160             | mA    |
| I <sub>SB2</sub> | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> ; CS <sub>N</sub> ≥ V <sub>CC</sub> - 0.3V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or<br>V <sub>IN</sub> ≤ 0.3V |           | 160             | mA    |

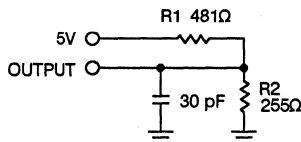
### Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions   | Max. | Units |
|------------------|--------------------|---|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 70   | pF    |
| C <sub>OUT</sub> | Output Capacitance |   | 35   |       |

#### Notes:

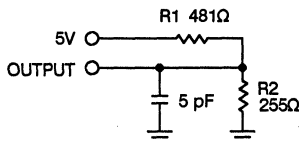
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the CS input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- Tested on a sample basis.

### AC Test Loads and Waveforms



INCLUDING  
JIG AND  
SCOPE

Figure 1a



INCLUDING  
JIG AND  
SCOPE

Figure 1b

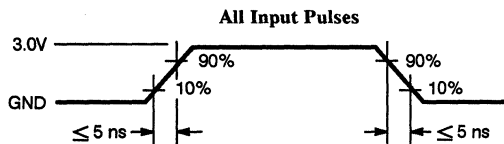
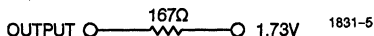


Figure 2

Equivalent to: THEVENIN EQUIVALENT



Switching Characteristics Over Operating Range <sup>[4]</sup>

| Parameters                        | Description   | 1831PZ-25 |      | 1831PZ-35 |      | 1831PZ-45 |      | Units |
|-----------------------------------|---|-----------|------|-----------|------|-----------|------|-------|
|                                   |   | Min.      | Max. | Min.      | Max. | Min.      | Max. |       |
| <b>READ CYCLE</b>                 |   |           |      |           |      |           |      |       |
| t <sub>RC</sub>                   | Read Cycle Time   | 25        |      | 35        |      | 45        |      | ns    |
| t <sub>AA</sub>                   | Address to Data Valid                                   |           | 25   |           | 35   |           | 45   | ns    |
| t <sub>OHA</sub>                  | Data Hold from Address Change                           | 3         |      | 3         |      | 3         |      | ns    |
| t <sub>ACS</sub>                  | $\overline{\text{CS}}$ LOW to Data Valid                |           | 25   |           | 35   |           | 45   | ns    |
| t <sub>DOE</sub>                  | $\overline{\text{OE}}$ LOW to Data Valid                |           | 15   |           | 25   |           | 30   | ns    |
| t <sub>LZOE</sub>                 | $\overline{\text{OE}}$ LOW to LOW Z                     | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>HZOE</sub>                 | $\overline{\text{OE}}$ HIGH to HIGH Z                   |           | 10   |           | 20   |           | 20   | ns    |
| t <sub>LZCS</sub>                 | $\overline{\text{CS}}$ LOW to Low Z <sup>[6]</sup>      | 3         |      | 3         |      | 3         |      | ns    |
| t <sub>HZCS</sub>                 | $\overline{\text{CS}}$ HIGH to High Z <sup>[5, 6]</sup> |           | 10   |           | 15   |           | 20   | ns    |
| t <sub>PU</sub>                   | $\overline{\text{CS}}$ LOW to Power Up                  | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>PD</sub>                   | $\overline{\text{CS}}$ HIGH to Power Down               |           | 25   |           | 35   |           | 45   | ns    |
| <b>WRITE CYCLE <sup>[7]</sup></b> |   |           |      |           |      |           |      |       |
| t <sub>WC</sub>                   | Write Cycle Time  | 20        |      | 25        |      | 35        |      | ns    |
| t <sub>SCS</sub>                  | $\overline{\text{CS}}$ LOW to Write End                 | 20        |      | 30        |      | 40        |      | ns    |
| t <sub>AW</sub>                   | Address Set-up to Write End                             | 20        |      | 30        |      | 40        |      | ns    |
| t <sub>HA</sub>                   | Address Hold from Write End                             | 2         |      | 2         |      | 2         |      | ns    |
| t <sub>SA</sub>                   | Address Set-up to Write Start                           | 2         |      | 2         |      | 2         |      | ns    |
| t <sub>PWE</sub>                  | WE Pulse Width  | 20        |      | 25        |      | 30        |      | ns    |
| t <sub>SD</sub>                   | Data Set-up to Write End                                | 13        |      | 20        |      | 25        |      | ns    |
| t <sub>HD</sub>                   | Data Hold from Write End                                | 2         |      | 2         |      | 2         |      | ns    |
| t <sub>LZWE</sub>                 | $\overline{\text{WE}}$ HIGH to Low Z <sup>[6]</sup>     | 3         |      | 5         |      | 5         |      | ns    |
| t <sub>HZWE</sub>                 | $\overline{\text{WE}}$ LOW to High Z <sup>[5, 6]</sup>  | 0         | 10   | 0         | 12   | 0         | 15   | ns    |

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
5. t<sub>HZCS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of  $\overline{\text{CS}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8.  $\overline{\text{WE}}$  is HIGH for read cycle.
9. Device is continuously selected,  $\overline{\text{CS}} = V_{\text{IL}}$  and  $\overline{\text{OE}} = V_{\text{IL}}$ .
10. Address valid prior to or coincident with  $\overline{\text{CS}}$  transition low.
11.  $\overline{\text{CS}}_1$ ,  $\overline{\text{CS}}_2$ ,  $\overline{\text{CS}}_3$  and  $\overline{\text{CS}}_4$  are represented by  $\overline{\text{CS}}$  in the switching Characteristics and Waveforms.

2



### Data Retention Characteristics (L Version Only)

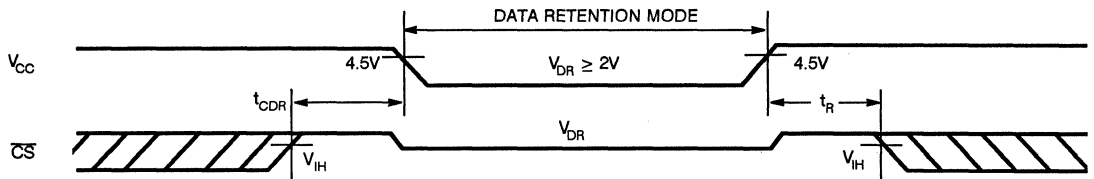
| Parameter        | Description                          | Test Conditions   | CYM1831         |      | Units   |
|------------------|--------------------------------------|---|-----------------|------|---------|
|                  |                                      |   | Min.            | Max. |         |
| $V_{DR}$         | $V_{CC}$ for Retention Data          | $V_{CC} = 2.0V$ ,<br>$\overline{CS} \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$<br>or $V_{IN} \leq 0.2V$ | 2.0             |      | V       |
| $I_{CCDR}$       | Data Retention Current               |   |                 | 32   | mA      |
| $t_{CDR}^{[13]}$ | Chip Deselect to Data Retention Time |   | 0               |      | ns      |
| $t_R^{[13]}$     | Operation Recovery Time              |   | $t_{RC}^{[12]}$ |      | ns      |
| $I_{LI}^{[13]}$  | Input Leakage Current                |   |                 | 20   | $\mu A$ |

**Notes:**

12.  $t_{RC}$  = Read Cycle Time.

13. Guaranteed, not tested.

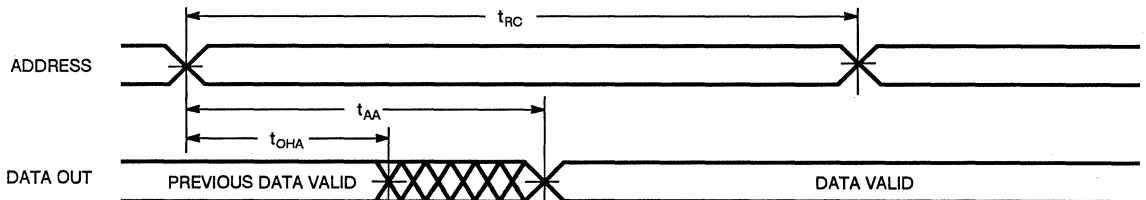
### Data Retention Waveform



1831-6

### Switching Waveforms<sup>[11]</sup>

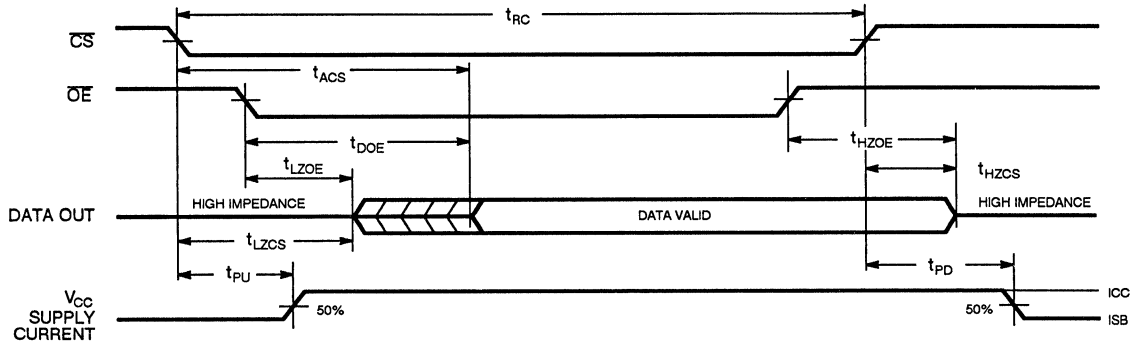
Read Cycle No. 1<sup>[8, 9]</sup>



1831-7

### Switching Waveforms (Continued)

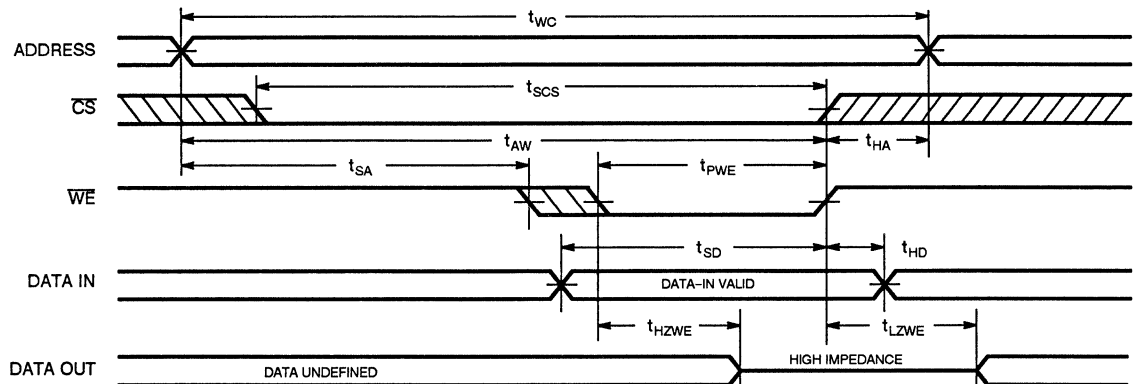
Read Cycle No. 2<sup>[8, 10]</sup>



2

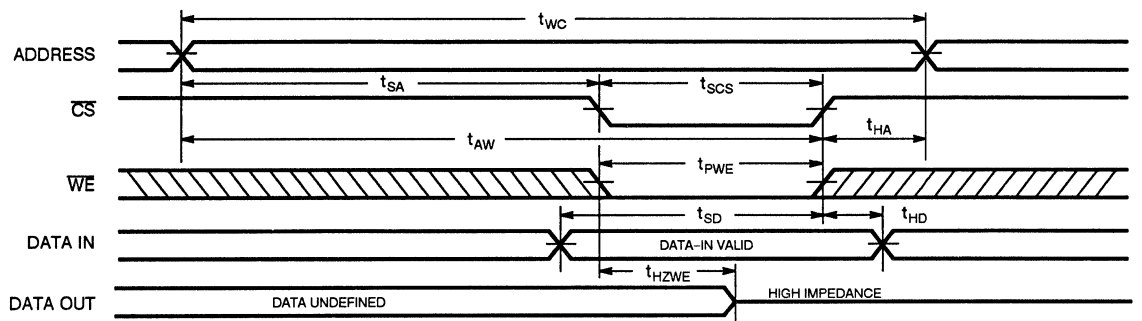
1831-8

Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[7]</sup>



1831-9

Write Cycle No. 2 ( $\overline{CS}$  Controlled)<sup>[7]</sup>



Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

1831-10

### Truth Table

| $\overline{CS}_N$ | $\overline{WE}$ | $\overline{OE}$ | Input/Outputs | Mode                |
|-------------------|-----------------|-----------------|---------------|---------------------|
| H                 | X               | X               | High Z        | Deselect Power Down |
| L                 | H               | L               | Data Out      | Read                |
| L                 | L               | X               | Data In       | Write               |
| L                 | H               | H               | High Z        | Deselect            |

### Ordering Information

| Speed | Ordering Code  | Package Type | Operating Range |
|-------|----------------|--------------|-----------------|
| 25    | CYM1831PZ-25C  | PZ01         | Commercial      |
|       | CYM1831LPZ-25C | PZ01         |                 |
| 35    | CYM1831PZ-35C  | PZ01         |                 |
|       | CYM1831LPZ-35C | PZ01         |                 |
| 45    | CYM1831PZ-45C  | PZ01         |                 |
|       | CYM1831LPZ-45C | PZ01         |                 |

Document #: 38-M-00018



**Features**

- High-density 2M bit SRAM Module
- High speed CMOS SRAMs
  - Access time – 35 ns
- Low active power – 5.4 W (max)
- SMD Technology
- TTL compatible inputs and outputs
- Low profile
  - Max. height – .50 in.
- Small PCB footprint – 1.0 sq in.

**Functional Description**

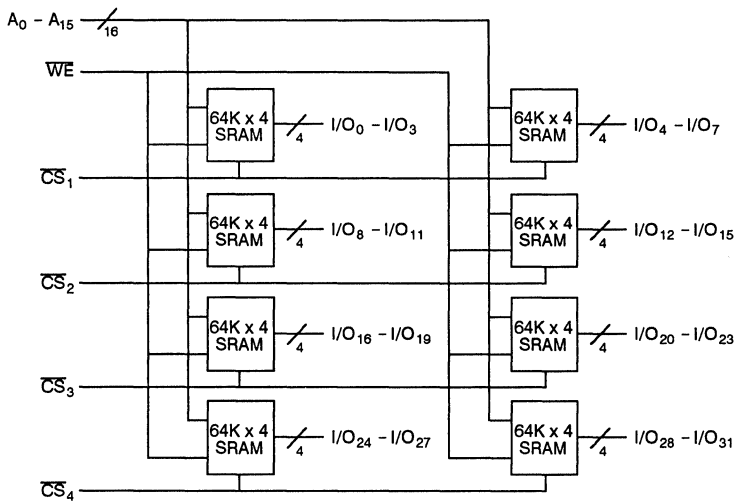
The CYM1832 is a high performance 2M-bit Static RAM module organized as 64K words by 32 bits. This module is constructed from eight 64K x 4 SRAMs SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ( $\overline{CS}_1$ ,  $\overline{CS}_2$ ,  $\overline{CS}_3$  and  $\overline{CS}_4$ ) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects. Writing to each byte is accomplished when the appropriate chip selects ( $\overline{CS}_N$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the input/output pins

( $I/O_x$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{16}$ ).

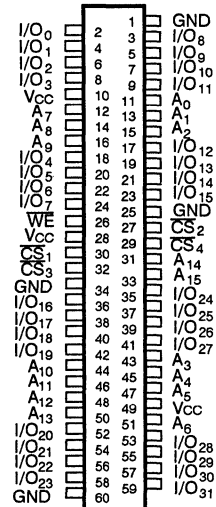
Reading the device is accomplished by taking the chip selects ( $\overline{CS}_N$ ) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins ( $I/O_x$ ).

The data input/output pins stay in the high impedance state when write enable ( $\overline{WE}$ ) is LOW, or the appropriate chip selects are HIGH.

**Logic Block Diagram**



**Pin Configuration**



ZIP  
Top View

1832-1

1832-2

**Selection Guide**

|                                | 1832PZ-35 | 1832PZ-45 | 1832PZ-55 |
|--------------------------------|-----------|-----------|-----------|
| Maximum Access time (ns)       | 35        | 45        | 55        |
| Maximum Operating Current (mA) | 980       | 980       | 980       |
| Maximum Standby Current (mA)   | 240       | 240       | 240       |

## Maximum Ratings

(Above which the useful life may be impaired)

|   |                 |
|---|-----------------|
| Storage Temperature .....                           | -45°C to +125°C |
| Ambient Temperature with Power Applied .....        | 10°C to +85°C   |
| Supply Voltage to Ground Potential .....            | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State ..... | -0.5V to +7.0V  |
| DC Input Voltage .....                              | -0.5V to +7.0V  |
| Output Current into Outputs (Low) .....             | 20 mA           |

## Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C        | 5V ± 10%        |

## Electrical Characteristics Over Operating Range

| Parameters       | Description                                    | Test Conditions   | CYM1832PZ |                 | Units |
|------------------|--|---|-----------|-----------------|-------|
|                  |  |   | Min.      | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                            | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA   | 2.4       |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                             | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA  |           | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                             |   | 2.2       | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage <sup>[1]</sup>               |   | -0.5      | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current                             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>  | -20       | +20             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                         | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled  | -100      | +100            | μA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current       | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>CS <sub>N</sub> ≤ V <sub>IL</sub>  |           | 980             | mA    |
| I <sub>SB1</sub> | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> ; CS <sub>N</sub> ≥ V <sub>IH</sub><br>Min. Duty Cycle = 100%  |           | 240             | mA    |
| I <sub>SB2</sub> | Automatic CS <sup>[2]</sup> Power Down Current | Max. V <sub>CC</sub> ; CS <sub>N</sub> ≥ V <sub>CC</sub> - 0.2V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or<br>V <sub>IN</sub> ≤ 0.2V |           | 120             | mA    |

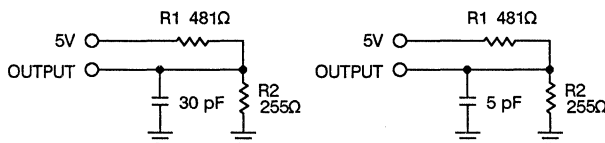
## Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions   | Max. | Units |
|------------------|--------------------|---|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 70   | pF    |
| C <sub>OUT</sub> | Output Capacitance |   | 35   |       |

### Notes:

- V<sub>IL(MIN)</sub> = -3.0V for pulse widths less than 20ns.
- A pull-up resistor to V<sub>CC</sub> on the CS input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
- Tested on a sample basis.

## AC Test Loads and Waveforms



INCLUDING  
JIG AND  
SCOPE

Figure 1a

INCLUDING  
JIG AND  
SCOPE

Figure 1b

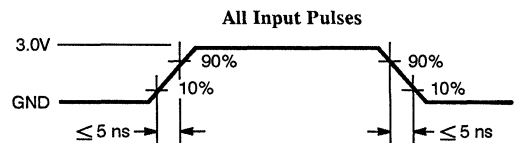
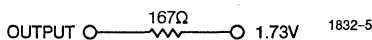


Figure 2

Equivalent to: THEVENIN EQUIVALENT



1832-5

### Switching Characteristics Over Operating Range <sup>[4]</sup>

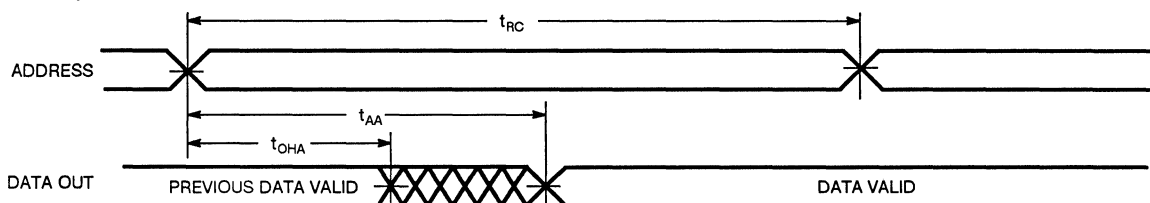
| Parameters                        | Description                                      | 1832PZ-35 |      | 1832PZ-45 |      | 1832PZ-55 |      | Units |
|-----------------------------------|--|-----------|------|-----------|------|-----------|------|-------|
|                                   |  | Min.      | Max. | Min.      | Max. | Min.      | Max. |       |
| <b>READ CYCLE</b>                 |  |           |      |           |      |           |      |       |
| t <sub>RC</sub>                   | Read Cycle Time                                  | 35        |      | 45        |      | 55        |      | ns    |
| t <sub>AA</sub>                   | Address to Data Valid                            |           | 35   |           | 45   |           | 55   | ns    |
| t <sub>OHA</sub>                  | Data Hold from Address Change                    | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>ACS</sub>                  | $\overline{CS}$ LOW to Data Valid                |           | 35   |           | 45   |           | 55   | ns    |
| t <sub>LZCS</sub>                 | $\overline{CS}$ LOW to Low Z <sup>[6]</sup>      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>HZCS</sub>                 | $\overline{CS}$ HIGH to High Z <sup>[5, 6]</sup> | 0         | 25   | 0         | 30   | 0         | 30   | ns    |
| t <sub>PU</sub>                   | $\overline{CS}$ LOW to Power Up                  | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>PD</sub>                   | $\overline{CS}$ HIGH to Power Down               |           | 35   |           | 45   |           | 55   | ns    |
| <b>WRITE CYCLE <sup>[7]</sup></b> |  |           |      |           |      |           |      |       |
| t <sub>WC</sub>                   | Write Cycle Time                                 | 35        |      | 45        |      | 55        |      | ns    |
| t <sub>SCS</sub>                  | $\overline{CS}$ LOW to Write End                 | 30        |      | 35        |      | 45        |      | ns    |
| t <sub>AW</sub>                   | Address Set-up to Write End                      | 30        |      | 35        |      | 45        |      | ns    |
| t <sub>HA</sub>                   | Address Hold from Write End                      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>SA</sub>                   | Address Set-up to Write Start                    | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>PWE</sub>                  | $\overline{WE}$ Pulse Width                      | 30        |      | 35        |      | 45        |      | ns    |
| t <sub>SD</sub>                   | Data Set-up to Write End                         | 20        |      | 25        |      | 35        |      | ns    |
| t <sub>HD</sub>                   | Data Hold from Write End                         | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>LZWE</sub>                 | $\overline{WE}$ HIGH to Low Z <sup>[6]</sup>     | 3         |      | 5         |      | 5         |      | ns    |
| t <sub>HZWE</sub>                 | $\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>  | 0         | 15   | 0         | 20   | 0         | 30   | ns    |

**Notes:**

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- t<sub>HZCS</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in Figure 1b. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCS</sub> is less than t<sub>LZCS</sub> for any given device. These parameters are guaranteed and not 100% tested.
- The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CS} = V_{IL}$ .
- Address valid prior to or coincident with  $\overline{CS}$  transition low.
- $\overline{CS}_1$ ,  $\overline{CS}_2$ ,  $\overline{CS}_3$  and  $\overline{CS}_4$  are represented by  $\overline{CS}$  in the switching Characteristics and Waveforms.

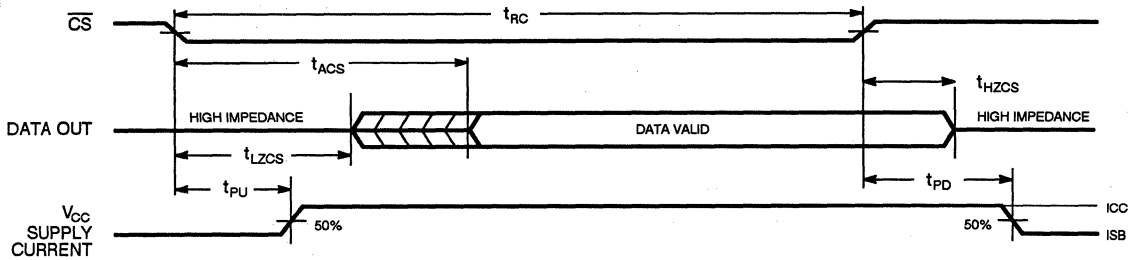
### Switching Waveforms <sup>[11]</sup>

Read Cycle No. 1 <sup>[8, 9]</sup>

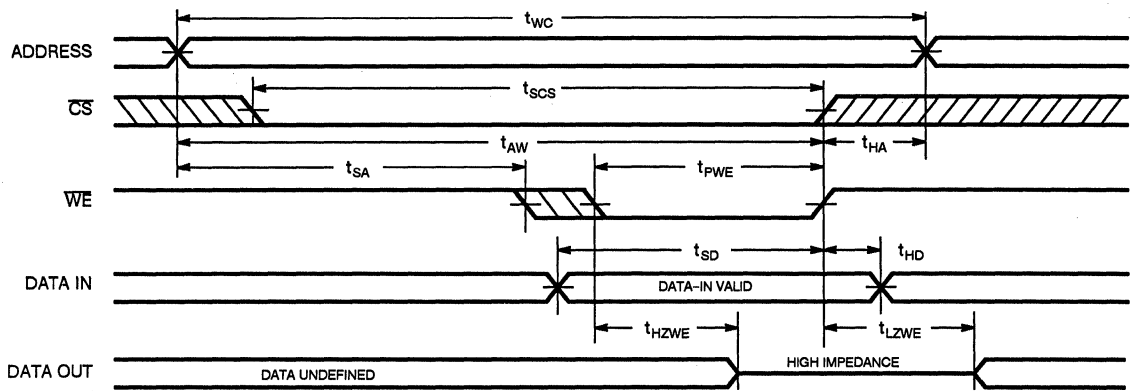


### Switching Waveforms (Continued)

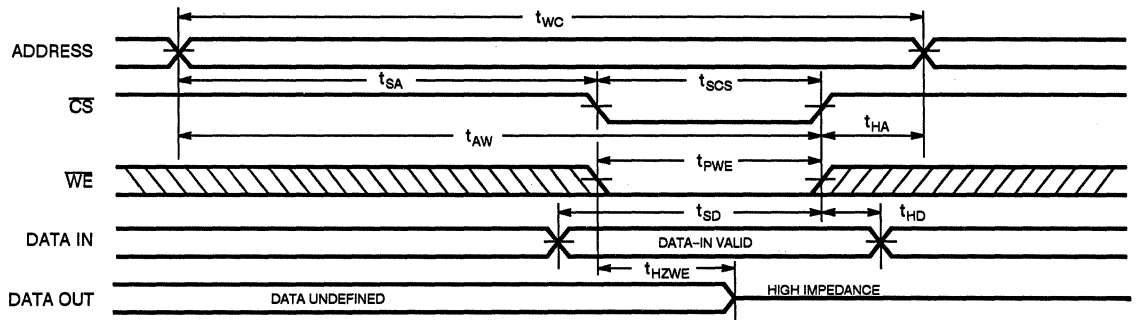
#### Read Cycle No. 2<sup>[8, 10]</sup>



#### Write Cycle No. 1 ( $\overline{WE}$ Controlled)<sup>[7]</sup>



#### Write Cycle No. 2 ( $\overline{CS}$ Controlled)<sup>[7]</sup>



Note: If  $\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.

**Truth Table**

| $\overline{CS}_N$ | $\overline{WE}$ | Input/Outputs | Mode                |
|-------------------|-----------------|---------------|---------------------|
| H                 | X               | High Z        | Deselect Power Down |
| L                 | H               | Data Out      | Read                |
| L                 | L               | Data In       | Write               |

2

**Ordering Information**

| Speed | Ordering Code | Package Type | Operating Range |
|-------|---------------|--------------|-----------------|
| 35    | CYM1832PZ-35C | PZ02         | Commercial      |
| 45    | CYM1832PZ-45C | PZ02         |                 |
| 55    | CYM1832PZ-55C | PZ02         |                 |

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## PROMs (Programmable Read Only Memory)

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## 1: Product Line Overview

The Cypress CMOS family of PROMs span 4K to 256K bit densities, three functional configurations, and are all byte-wide. The product line is available in both 0.3 and 0.6 inch wide dual-in-line plastic and CERDIP as well as LCC and PLCC packages. The programming technology is EPROM and therefore windowed packages are available in both dual-in-line and LCC configurations, providing erasable products. These byte-wide products are available in registered versions at the 512, 1K, 2K, and 8K by 8 densities, and in non-registered versions at the 1K, 2K, 8K, 16K and 32K by 8 densities. The registered devices operate in either synchronous or asynchronous output enable modes and may have an initialize feature to preload the pipeline register. The 8K by 8 registered devices feature a diagnostic shadow register which allows the pipeline register to be loaded or examined via a serial path.

Cypress PROMs perform at the level of their bipolar equivalents or beyond with reduced power levels of CMOS technology. They are capable of 2001 volts of ESD and operate with 10% power supply tolerances.

## 2: Technology Introduction

Cypress PROMs are executed in an "N" well CMOS EPROM process. Densities of 128K and under with the exception of the "A" series devices use the 1.2 micron PROM I technology. The 16K "A" series devices and the future 256K PROMs use the 0.8 micron PROM II technology with a single ended memory cell. The process provides basic gate delays of 235 picoseconds for a fanout of one at a power consumption of 45 femto joules. The process provides the basis for the development of LSI products that outperform the fastest bipolar products currently available.

Although CMOS static RAMs have challenged bipolar RAMs for speed, CMOS EPROMs have always been a factor of three to ten times slower than bipolar fuse PROMs. There have been two major limitations on CMOS EPROM speed; 1) the single transistor EPROM cell is inherently slower than the bipolar fuse element, and 2) CMOS EPROM technologies have been optimized for cell programmability and density, almost always at the expense of speed. In the Cypress CMOS EPROM technology, both of the aforementioned limitations have been overcome to create CMOS PROMs with performance superior to PROMs implemented in bipolar technology.

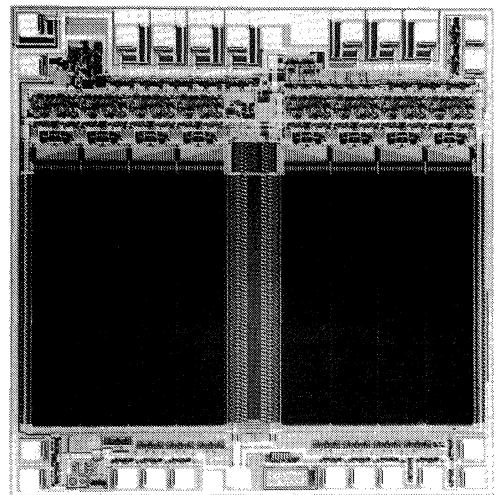
In all Cypress PROMs, speed and programmability are optimized independently by separating the read and write transistor functions. Also, for the first time a substrate bias generator is employed in an EPROM technology to improve performance and raise latchup immunity to greater than 200 mA. The result is a CMOS EPROM technology that challenges bipolar fuse technology for both density and speed. In addition, at higher densities, performance and density surpasses the best that bipolar can provide. Limitations of devices implemented in the bipolar fuse technology such as PROGRAMMING YIELD, POWER DISSIPATION and HIGHER DENSITY PERFORMANCE are eliminated or greatly reduced using Cypress CMOS EPROM technology.

## 3: Design Approach

### A. Four Transistor Differential Memory Cell

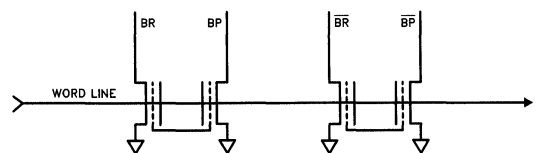
The 4K, 8K, and 16K PROM (except "A" version) use an N-Well CMOS technology along with a new differential four transistor EPROM cell that is optimized for speed. The area of the four transistor cell is 0.43 square mils and the die size is 19,321 square mils for the 2K by 8 PROM (Figure 1). The floating gate cell is optimized for high read current and fast programmability. This is accomplished by separating the read and program transistors (Figure 2). The program transistor has a separate implant to maximize the generation and collection of hot electrons while the read transistor implant dose is chosen to provide a large read current. Both the n and p channel peripheral transistors have self-aligned, shallow, lightly doped drain (LDD) junctions. The LDD structure reduces overlap capacitance for speed improvement and minimizes hot electron injection for improved reliability. Although common for NMOS static and dynamic RAMs, an on-chip substrate bias generator is used for the first time in an EPROM technology. The results are improved speed, greater than 200 mA latch-up immunity and high parasitic field inversion voltages during programming.

3



0034-1

Figure 1



0034-2

Figure 2. Non-volatile cell optimized for speed and programmability

Access times of less than 35 ns at 16K densities and 30 ns at 4K and 8K densities over the full operating range are achieved by using differential design techniques and by to-

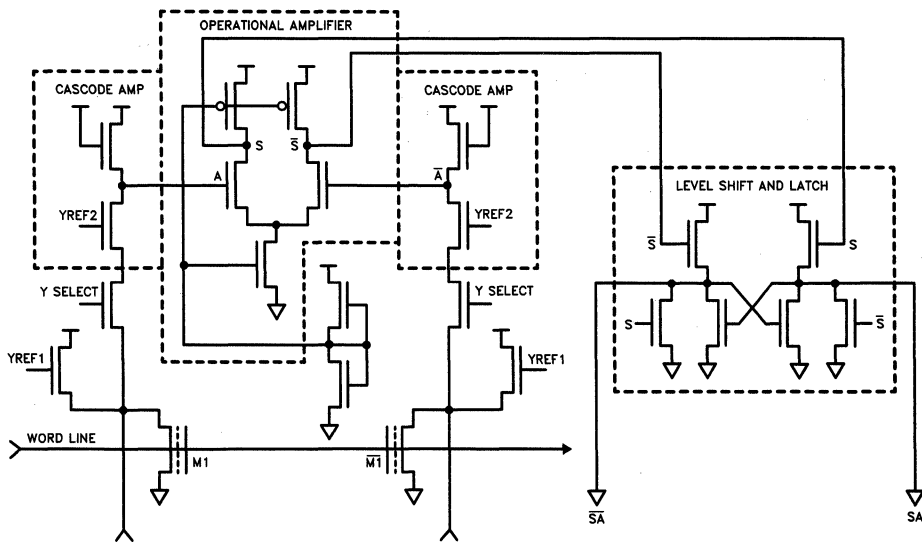


Figure 3. Differential sensing

0034-3

tally separating the read and program paths. This allows the read path to be optimized for speed. The X and Y decoding paths are predecoded to optimize the power-delay product. A differential sensing scheme and the four transistor cell are used to sense bit-line swings as low as 100 mV at high speed. The sense amplifier (Figure 3) consists of three stages of equal gain. A gain of 4 per stage was found to be optimum. The Cascode stage amplifies the bit line swings and feeds them into a differential amplifier. The output of the differential amplifier is further amplified and voltages shifted by a level shifter and latch. This signal is then fed into an output buffer having a TTL fan-out of ten.

## B. Two Transistor Memory Cell

The Cypress 64K and greater density PROMs use a two transistor memory cell. This cell uses a single ended sensing scheme with the exception of the 256K device which uses a differential sensing circuit. This combination allows for a more compact design and reduced manufacturing costs. This is an excellent compromise between performance and high density, allowing the development of devices with performance of 35 ns and 45 ns access times at densities from 64K to 256K bits and 25 ns for the "A" series 16K using the PROM II technology. This two transistor cell still uses the high speed read transistor and the optimized EPROM transistor for performance and reliable programming. The sense amplifier uses a reference voltage on one input and the read transistor on the other, instead of two read transistors. This single ended sensing is a more conventional technique and has the effect of causing an erased device to contain all "0"s.

## 4: Programming

### A. Differential Memory Cells

Cypress PROMs are programmed a BYTE at a time by applying 12 to 14 volts on one pin and the desired logic

levels to input pins. Both logic "ONE" and logic "ZERO" are programmed into the differential cell. A BIT is programmed by applying 12 to 14 volts on the control gate and 9 volts on the drain of the floating gate write transistor. This causes hot electrons from the channel to be injected onto the floating gate thereby raising the threshold voltage. Because the read transistor shares a common floating gate with the program transistor, the threshold of the read transistor is raised from about 1 volt to greater than 5 volts resulting in a transistor that is turned "OFF" when selected in a read mode of operation. Since both sides of the differential cell are at equal potential before programming, a threshold shift of 100 mV is enough to be determined as the correct logic state. Because an unprogrammed cell has neither a ONE nor a ZERO in it before programming, a special BLANK CHECK mode of operation is implemented. In this mode the output of each half of the cell is compared against a fixed reference which allows distinction of a programmed or unprogrammed cell. A MARGIN mode is also provided to monitor the thresholds of the individual BITs allowing the monitoring of the quality of programming during the manufacturing operation.

### B. Single Ended Memory Cells

The programming mechanism of the EPROM transistor in a single ended memory cell is the same as its counterpart in a double ended memory cell. The difference is that only ones "1"s are programmed in a single ended cell. A "1" applied to the I/O pin during programming causes an erased EPROM transistor to be programmed while a "0" allows the EPROM transistor to remain unprogrammed.

## 5: Erasability

For the first time at PROM speeds, Cypress PROMs using CMOS EPROM technology offer reprogrammability when packaged in windowed CERDIP. This is available at densities of 16K and larger, both registered and non-registered.



Wavelengths of light less than 4000 Angstroms begin to erase Cypress PROMs. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity  $\times$  exposure time) of 25 Wsec/cm<sup>2</sup>. For an ultraviolet lamp with a 12 mW/cm<sup>2</sup> power rating the exposure time would be approximately 30–35 minutes. The industry EPROM erasure standard is 15 Wsec/cm<sup>2</sup>. Cypress EPROMs require  $1\frac{2}{3}$  longer erase times.

The PROM needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity light for an extended period of time. 7258 Wsec/cm<sup>2</sup> is the recommended maximum dosage.

Some devices are sensitive to photo-electric effects during programming. Cypress recommends covering the windows of reprogrammable devices during programming.

### 6: Reliability

The CMOS EPROM approach to PROMs has some significant benefits to the user in the area of programming and functional yield. Since a cell may be programmed and erased multiple times, CMOS PROMs from Cypress can be tested 100% for programmability during the manufacturing process. Because each CMOS PROM contains a PHANTOM array, both the functionality and performance of the devices may be tested after they are packaged thus assuring the user that not only will every cell program, but that the product performs to the specification.





**Features**

- CMOS for optimum speed/power
- High speed
  - 25 ns max set-up
  - 12 ns clock to output
- Low power
  - 495 mW (commercial)
  - 660 mW (military)
- Synchronous and asynchronous output enables
- On-chip edge-triggered registers
- Buffered Common PRESET and CLEAR inputs
- EPROM technology, 100% programmable
- Slim, 300 mil, 24 pin plastic or hermetic DIP, or 28 pin LCC
- 5V ±10% V<sub>CC</sub>, commercial and military
- TTL compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 1500V static discharge

**Product Characteristics**

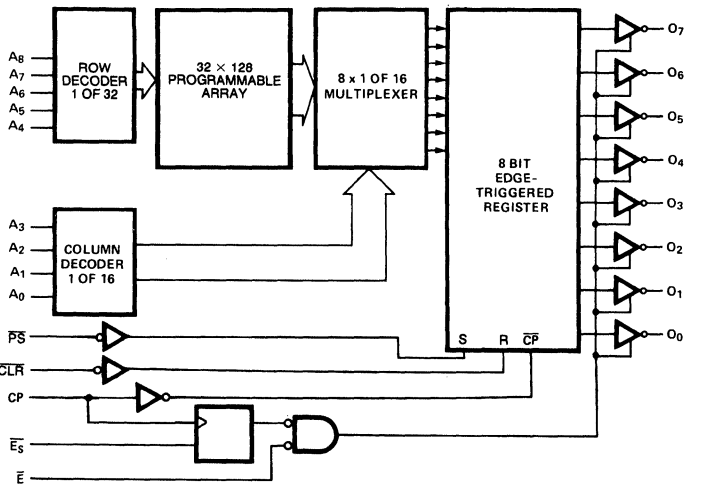
The CY7C225 is a high performance 512 word by 8 bit electrically Programmable Read Only Memory packaged in a slim 300 mil plastic or hermetic DIP and 28 pin Leadless Chip Carrier. The memory cells utilize proven EPROM

floating gate technology and byte-wide intelligent programming algorithms.

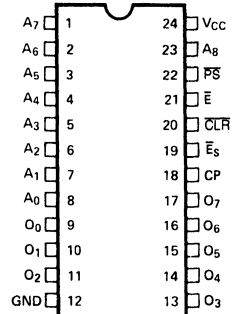
The CY7C225 replaces bipolar devices and offers the advantages of lower power, superior performance and high programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

The CY7C225 has asynchronous PRESET and CLEAR functions.

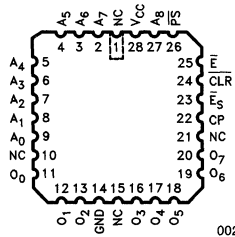
**Logic Block Diagram**



**Pin Configurations**



0020-2



0020-11

**Selection Guide**

|                                | 7C225-25   | 7C225-30 | 7C225-35 | 7C225-40 |
|--------------------------------|------------|----------|----------|----------|
| Maximum Set-up Time (ns)       | 25         | 30       | 35       | 40       |
| Maximum Clock to Output (ns)   | 12         | 15       | 20       | 25       |
| Maximum Operating Current (mA) | Commercial | 90       | 90       | 90       |
|                                | Military   |          | 120      | 120      |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential

(Pin 24 to Pin 12) ..... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) ..... 14.0V

Static Discharge Voltage ..... > 1500V  
 (Per MIL-STD-883 Method 3015)

Latch-up Current ..... > 200 mA

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[6]</sup> | -55°C to +125°C     | 5V ± 10%        |

**3**

## Electrical Characteristics Over Operating Range<sup>[7]</sup>

| Parameters      | Description                  | Test Conditions   | Min.       | Max. | Units |
|-----------------|------------------------------|---|------------|------|-------|
| V <sub>OH</sub> | Output HIGH Voltage          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | 2.4        |      | V     |
| V <sub>OL</sub> | Output LOW Voltage           | V <sub>CC</sub> = Min., I <sub>OL</sub> = -16 mA<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  |            | 0.4  | V     |
| V <sub>IH</sub> | Input HIGH Level             | Guaranteed Input Logical HIGH Voltage for All Inputs <sup>[2]</sup>                                       | 2.0        |      | V     |
| V <sub>IL</sub> | Input LOW Level              | Guaranteed Input Logical LOW Voltage for All inputs <sup>[2]</sup>  |            | 0.8  | V     |
| I <sub>IX</sub> | Input Leakage Current        | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>   | -10        | +10  | μA    |
| V <sub>CD</sub> | Input Clamp Diode Voltage    | Note 1  |            |      |       |
| I <sub>OZ</sub> | Output Leakage Current       | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> Output Disabled <sup>[4]</sup>                                     | -40        | +40  | μA    |
| I <sub>OS</sub> | Output Short Circuit Current | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0V <sup>[3]</sup>  | -20        | -90  | mA    |
| I <sub>CC</sub> | Power Supply Current         | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub><br>V <sub>CC</sub> = Max.   | Commercial | 90   | mA    |
|                 |                              |   | Military   | 120  |       |

## Capacitance<sup>[5]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 8    | pF    |

### Notes:

- The CMOS process does not provide a clamp diode. However, the CY7C225 is insensitive to -3V dc input levels and -5V undershoot pulses of less than 10 ns (measured at 50% point).
- These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

Switching Characteristics Over Operating Range<sup>[7, 8]</sup>

| Parameters                        | Description   | 7C225-25 |      | 7C225-30 |      | 7C225-35 |      | 7C225-40 |      | Units |
|-----------------------------------|---|----------|------|----------|------|----------|------|----------|------|-------|
|                                   |   | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.     | Max. |       |
| t <sub>SA</sub>                   | Address Setup to Clock HIGH                           | 25       |      | 30       |      | 35       |      | 40       |      | ns    |
| t <sub>HA</sub>                   | Address Hold from Clock HIGH                          | 0        |      | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>CO</sub>                   | Clock HIGH to Valid Output                            |          | 12   |          | 15   |          | 20   |          | 25   | ns    |
| t <sub>PWC</sub>                  | Clock Pulse Width                                     | 10       |      | 15       |      | 20       |      | 20       |      | ns    |
| t <sub>SE<sub>S</sub></sub>       | $\bar{E}_S$ Setup to Clock HIGH                       | 10       |      | 10       |      | 10       |      | 10       |      | ns    |
| t <sub>HE<sub>S</sub></sub>       | $\bar{E}_S$ Hold from Clock HIGH                      | 0        |      | 5        |      | 5        |      | 5        |      | ns    |
| t <sub>DP, t<sub>DC</sub></sub>   | Delay from PRESET or CLEAR to Valid Output            |          | 20   |          | 20   |          | 20   |          | 20   | ns    |
| t <sub>RP, t<sub>RC</sub></sub>   | PRESET or CLEAR Recovery to Clock HIGH                | 15       |      | 20       |      | 20       |      | 20       |      | ns    |
| t <sub>PWP, t<sub>PWC</sub></sub> | PRESET or CLEAR Pulse Width                           | 15       |      | 20       |      | 20       |      | 20       |      | ns    |
| t <sub>COS</sub>                  | Valid Output from Clock HIGH <sup>[1]</sup>           |          | 20   |          | 20   |          | 25   |          | 30   | ns    |
| t <sub>HZC</sub>                  | Inactive Output from Clock HIGH <sup>[1, 3]</sup>     |          | 20   |          | 20   |          | 25   |          | 30   | ns    |
| t <sub>DOE</sub>                  | Valid Output from $\bar{E}$ LOW <sup>[2]</sup>        |          | 20   |          | 20   |          | 25   |          | 30   | ns    |
| t <sub>HZE</sub>                  | Inactive Output from $\bar{E}$ HIGH <sup>[2, 3]</sup> |          | 20   |          | 20   |          | 25   |          | 30   | ns    |

Notes:

1. Applies only when the synchronous ( $\bar{E}_S$ ) function is used.
2. Applies only when the asynchronous ( $\bar{E}$ ) function is used.
3. Transition is measured at steady state HIGH level - 500 mV or steady state LOW level + 500 mV on the output from the 1.5V level on the input with loads shown in Figure 1b.
4. Tests are performed with rise and fall times of 5 ns or less.
5. See Figure 1a for all switching characteristics except t<sub>HZ</sub>.
6. See Figure 1b for t<sub>HZ</sub>.
7. All device test loads should be located within 2" of device outputs.
8. See the last page of this specification for Group A subgroup testing information.

AC Test Loads and Waveforms<sup>[5, 6, 7]</sup>

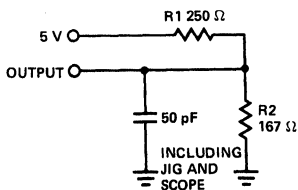


Figure 1a

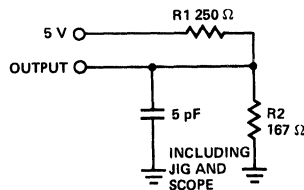


Figure 1b

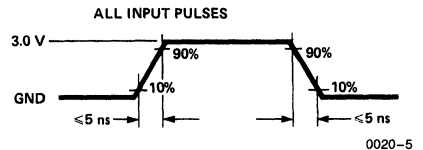
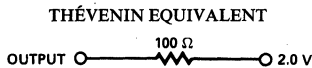


Figure 2

Equivalent to:



0020-4

Functional Description

The CY7C225 is a CMOS electrically programmable Read Only Memory organized as 512 words x 8-bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The CY7C225 incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous ( $\bar{E}_S$ ) and asynchronous ( $\bar{E}$ ) output enables, and CLEAR and PRESET inputs.

Upon power-up, the synchronous enable ( $\bar{E}_S$ ) flip-flop will be in the set condition causing the outputs ( $O_0$ - $O_7$ ) to be in the OFF or high impedance state. Data is read by

applying the memory location to the address inputs ( $A_0$ - $A_8$ ) and a logic LOW to the enable ( $\bar{E}_S$ ) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs ( $O_0$ - $O_7$ ) provided the asynchronous enable ( $\bar{E}$ ) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable ( $\bar{E}$ ) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

## Functional Description (Continued)

Regardless of the condition of  $\bar{E}$ , the outputs will go to the OFF or high impedance state upon the next positive clock edge after the synchronous enable ( $\bar{E}_S$ ) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if  $\bar{E}$  is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low to high transition of the clock. This unique feature allows the CY7C225 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

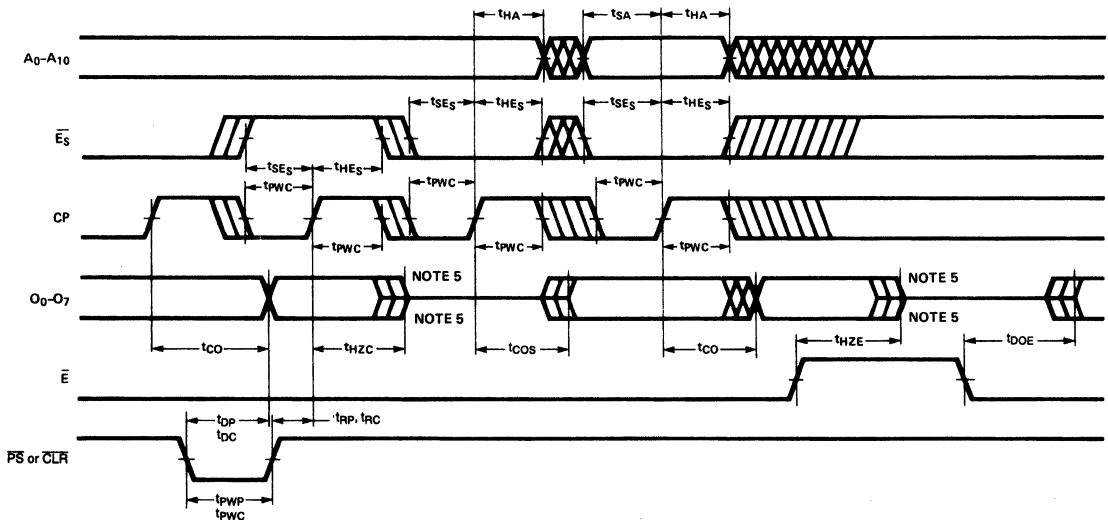
System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C225 has buffered asynchronous  $\overline{\text{CLEAR}}$  and  $\overline{\text{PRESET}}$  input ( $\overline{\text{INIT}}$ ). The initialize function is useful during power-up and time-out sequences.

Applying a LOW to the  $\overline{\text{PRESET}}$  input causes an immediate load of all ones into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). Applying a LOW to the  $\overline{\text{CLEAR}}$  input, resets the flip-flops to all zeros. The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ( $\bar{E}$ ) LOW.

When power is applied the (internal) synchronous enable flip-flop will be in a state such that the outputs will be in the high impedance state. In order to enable the outputs a clock must occur and the  $\bar{E}_S$  input pin must be LOW at least a setup time prior to the clock LOW to HIGH transition. The  $\bar{E}$  input may then be used to enable the outputs.

## Switching Waveforms



### Notes on Testing

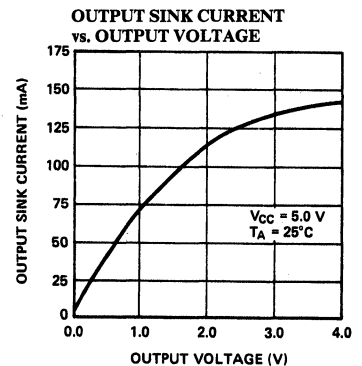
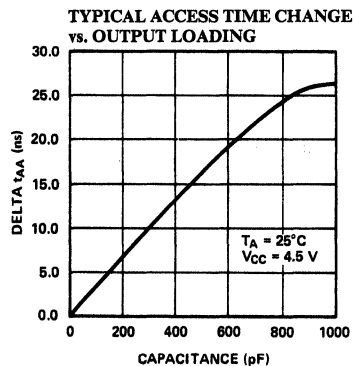
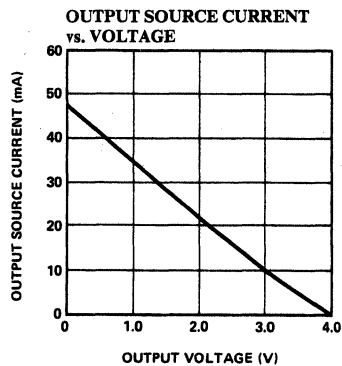
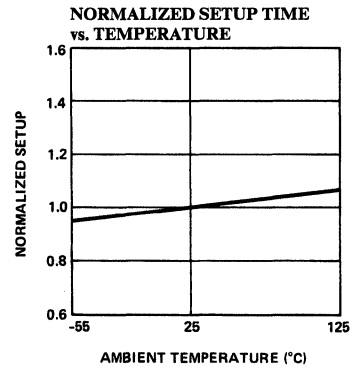
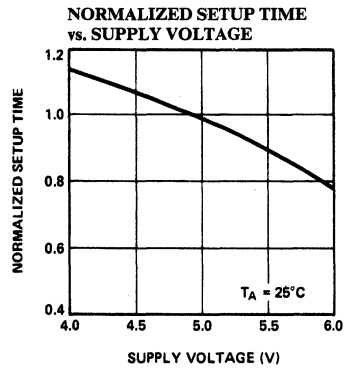
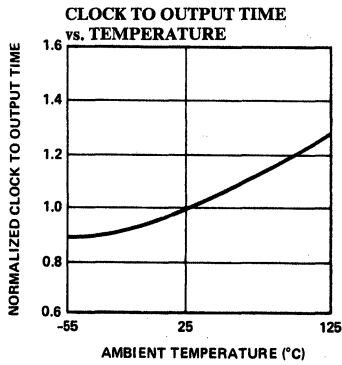
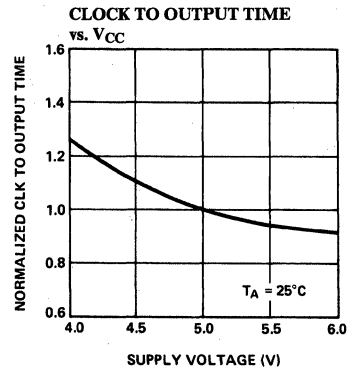
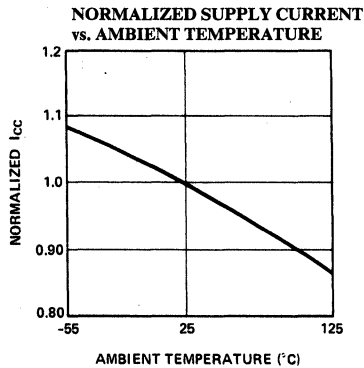
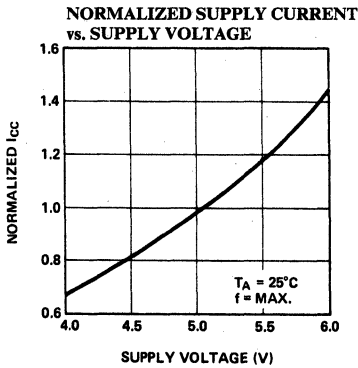
Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device  $V_{CC}$  and ground terminals. Multiple capacitors are recommended, including a 0.1  $\mu\text{F}$  or larger capacitor and a 0.01  $\mu\text{F}$  or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.

3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level  $-500\text{ mV}$  or steady state LOW level  $+500\text{ mV}$  on the output from the 1.5V level on inputs with load shown in Figure 1b.

0020-6

## Typical DC and AC Characteristics



## Device Programming

### Overview:

There is a programmable function contained in the 7C225 CMOS 512 x 8 Registered PROM; the 512 x 8 array. All of the programming elements are “EPROM” cells, and are in an erased state when the device is shipped.

The 512 x 8 array uses a differential memory cell, with differential sensing techniques. In the erased state the cell contains neither a one nor a zero. The erased state of this array may be verified by using the “BLANK CHECK ONES” and “BLANK CHECK ZEROS” function, see Table 3.

### DC Programming Parameters $T_A = 25^\circ\text{C}$

**Table 1**

| Parameter                      | Description                | Min. | Max. | Units |
|--------------------------------|----------------------------|------|------|-------|
| V <sub>PP</sub> <sup>[1]</sup> | Programming Voltage        | 13.0 | 14.0 | V     |
| V <sub>CCP</sub>               | Supply Voltage             | 4.75 | 5.25 | V     |
| V <sub>IHP</sub>               | Input High Voltage         | 3.0  |      | V     |
| V <sub>ILP</sub>               | Input Low Voltage          |      | 0.4  | V     |
| V <sub>OH</sub> <sup>[2]</sup> | Output High Voltage        | 2.4  |      | V     |
| V <sub>OL</sub> <sup>[2]</sup> | Output Low Voltage         |      | 0.4  | V     |
| I <sub>PP</sub>                | Programming Supply Current |      | 50   | mA    |

### AC Programming Parameters $T_A = 25^\circ\text{C}$

**Table 2**

| Parameter                                      | Description                        | Min. | Max.   | Units |
|--|------------------------------------|------|--------|-------|
| t <sub>PP</sub>                                | Programming Pulse Width            | 100  | 10,000 | μs    |
| t <sub>AS</sub>                                | Address Setup Time                 | 1.0  |        | μs    |
| t <sub>DS</sub>                                | Data Setup Time                    | 1.0  |        | μs    |
| t <sub>AH</sub>                                | Address Hold Time                  | 1.0  |        | μs    |
| t <sub>DH</sub>                                | Data Hold Time                     | 1.0  |        | μs    |
| t <sub>R</sub> , t <sub>F</sub> <sup>[3]</sup> | V <sub>PP</sub> Rise and Fall Time | 50   |        | ns    |
| t <sub>VD</sub>                                | Delay to Verify                    | 1.0  |        | μs    |
| t <sub>VP</sub>                                | Verify Pulse Width                 | 2.0  |        | μs    |
| t <sub>DV</sub>                                | Verify Data Valid                  |      | 1.0    | μs    |
| t <sub>DZ</sub>                                | Verify HIGH to High Z              |      | 1.0    | μs    |

**Notes:**

1. V<sub>CCP</sub> must be applied prior to V<sub>PP</sub>.
2. During verify operation.

3. Measured 10% and 90% points.

Mode Selection

Table 3

| Mode                               | Pin Function <sup>[1]</sup> |                  |                         |                         |                   |                  | Outputs<br>(9-11,13-17) |
|------------------------------------|-----------------------------|------------------|-------------------------|-------------------------|-------------------|------------------|-------------------------|
|                                    | Read or Output Disable      | CP               | $\bar{E}_S$             | CLR                     | $\bar{E}$         | PS               |                         |
|                                    | Other<br>Pin                | PGM<br>(18)      | V <sub>FY</sub><br>(19) | V <sub>PP</sub><br>(20) | $\bar{E}$<br>(21) | PS<br>(22)       |                         |
| Read <sup>[2,3]</sup>              |                             | X                | V <sub>IL</sub>         | V <sub>IH</sub>         | V <sub>IL</sub>   | V <sub>IH</sub>  | Data Out                |
| Output Disable <sup>[5]</sup>      |                             | X                | V <sub>IH</sub>         | V <sub>IH</sub>         | X                 | V <sub>IH</sub>  | High Z                  |
| Output Disable                     |                             | X                | X                       | V <sub>IH</sub>         | V <sub>IH</sub>   | V <sub>IH</sub>  | High Z                  |
| $\overline{\text{CLEAR}}$          |                             | X                | V <sub>IL</sub>         | V <sub>IL</sub>         | V <sub>IL</sub>   | V <sub>IH</sub>  | Zeros                   |
| $\overline{\text{PRESET}}$         |                             | X                | V <sub>IL</sub>         | V <sub>IH</sub>         | V <sub>IL</sub>   | V <sub>IL</sub>  | Ones                    |
| Program <sup>[4]</sup>             |                             | V <sub>ILP</sub> | V <sub>IHP</sub>        | V <sub>PP</sub>         | V <sub>IHP</sub>  | V <sub>IHP</sub> | Data In                 |
| Program Verify <sup>[4]</sup>      |                             | V <sub>IHP</sub> | V <sub>ILP</sub>        | V <sub>PP</sub>         | V <sub>IHP</sub>  | V <sub>IHP</sub> | Data Out                |
| Program Inhibit <sup>[4]</sup>     |                             | V <sub>IHP</sub> | V <sub>IHP</sub>        | V <sub>PP</sub>         | V <sub>IHP</sub>  | V <sub>IHP</sub> | High Z                  |
| Intelligent Program <sup>[4]</sup> |                             | V <sub>ILP</sub> | V <sub>IHP</sub>        | V <sub>PP</sub>         | V <sub>IHP</sub>  | V <sub>IHP</sub> | Data In                 |
| Blank Check Ones <sup>[4]</sup>    |                             | V <sub>PP</sub>  | V <sub>ILP</sub>        | V <sub>ILP</sub>        | V <sub>ILP</sub>  | V <sub>IHP</sub> | Ones                    |
| Blank Check Zeros <sup>[4]</sup>   |                             | V <sub>PP</sub>  | V <sub>IHP</sub>        | V <sub>ILP</sub>        | V <sub>ILP</sub>  | V <sub>IHP</sub> | Zeros                   |

Notes:

1. X = Don't care but not to exceed V<sub>pp</sub>.
2. During read operation, the output latches are loaded on a "0" to "1" transition of CP.
3. Pin 19 must be LOW prior to the "0" to "1" transition on CP (18) that loads the register.
4. During programming and verification, all unspecified pins to be at V<sub>IL</sub>.
5. Pin 19 must be HIGH prior to the "0" to "1" transition on CP (18) that loads the register.

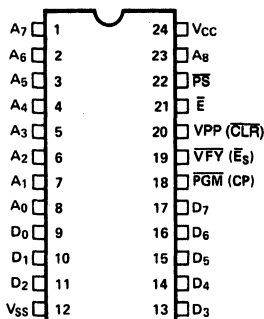


Figure 3. Programming Pinouts

0020-8

The CY7C225 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in Figure 4.

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the PGM pulse (t<sub>pp</sub>) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V<sub>CCP</sub> = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V<sub>CC</sub> = 5.0V.

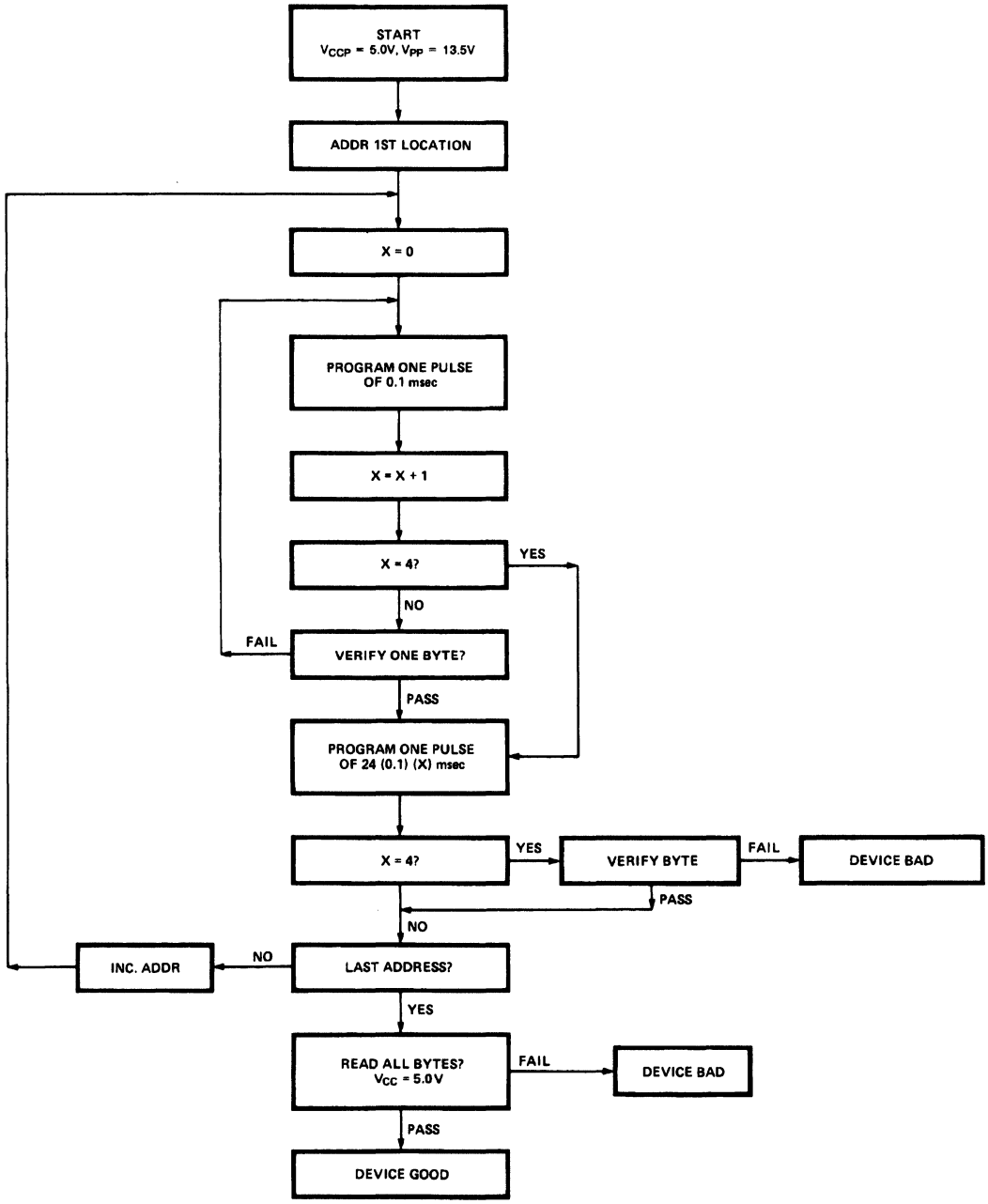


Figure 4. Programming Flowchart



## Programming Sequence 512 x 8 Array

Power the device for normal read mode operation with pin 18, 19, 20 and 21 at  $V_{IH}$ . Per *Figure 5* take pin 20 to  $V_{pp}$ . The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see *Figure 5*. Again per *Figure 5* address, program, and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100  $\mu$ s. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one

additional programming pulse should be applied of duration 24X the sum of the previous programming pulses before advancing to the next address to repeat the process.

## Blank Check

A virgin device contains neither one's nor zero's because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 511. A device is considered virgin if all locations are respectively "1's" and "0's" when addressed in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both one's and zero's. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

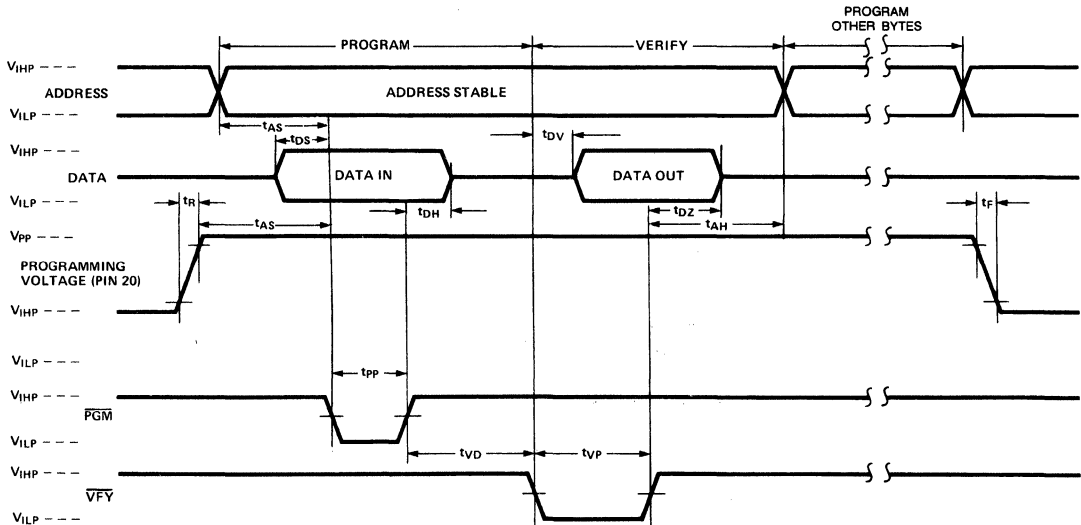


Figure 5. PROM Programming Waveforms

0020-10

**Ordering Information**

| Speed<br>ns |     | Ordering<br>Code | Package<br>Type | Operating<br>Range |
|-------------|-----|------------------|-----------------|--------------------|
| tSA         | tCO |                  |                 |                    |
| 25          | 12  | CY7C225-25PC     | P13             | Commercial         |
|             |     | CY7C225-25DC     | D14             |                    |
|             |     | CY7C225-25LC     | L64             |                    |
| 30          | 15  | CY7C225-30PC     | P13             | Commercial         |
|             |     | CY7C225-30DC     | D14             |                    |
|             |     | CY7C225-30LC     | L64             |                    |
| 35          | 20  | CY7C225-30DMB    | D14             | Military           |
|             |     | CY7C225-30LMB    | L64             |                    |
| 40          | 25  | CY7C225-35DMB    | D14             | Military           |
|             |     | CY7C225-35LMB    | L64             |                    |
| 40          | 25  | CY7C225-40PC     | P13             | Commercial         |
|             |     | CY7C225-40DC     | D14             |                    |
|             |     | CY7C225-40LC     | L64             |                    |
| 40          | 25  | CY7C225-40DMB    | D14             | Military           |
|             |     | CY7C225-40LMB    | L64             |                    |

**MILITARY SPECIFICATIONS****Group A Subgroup Testing****DC Characteristics**

| Parameters      | Subgroups |
|-----------------|-----------|
| V <sub>OH</sub> | 1,2,3     |
| V <sub>OL</sub> | 1,2,3     |
| V <sub>IH</sub> | 1,2,3     |
| V <sub>IL</sub> | 1,2,3     |
| I <sub>Ix</sub> | 1,2,3     |
| I <sub>OZ</sub> | 1,2,3     |
| I <sub>CC</sub> | 1,2,3     |

**Switching Characteristics**

| Parameters      | Subgroups   |
|-----------------|-------------|
| t <sub>SA</sub> | 7,8,9,10,11 |
| t <sub>HA</sub> | 7,8,9,10,11 |
| t <sub>CO</sub> | 7,8,9,10,11 |
| t <sub>DP</sub> | 7,8,9,10,11 |
| t <sub>RP</sub> | 7,8,9,10,11 |

Document #: 38-00002-B



**Features**

- CMOS for optimum speed/power
- High speed
  - 25 ns max set-up
  - 12 ns clock to output
- Low power
  - 495 mW (commercial)
  - 660 mW (military)
- Synchronous and asynchronous output enables
- On-chip edge-triggered registers
- Programmable asynchronous register (INIT)
- EPROM technology, 100% programmable
- Slim, 300 mil, 24 pin plastic or hermetic DIP or 28 pin LCC
- 5V ± 10% V<sub>CC</sub>, commercial and military
- TTL compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 1500V static discharge

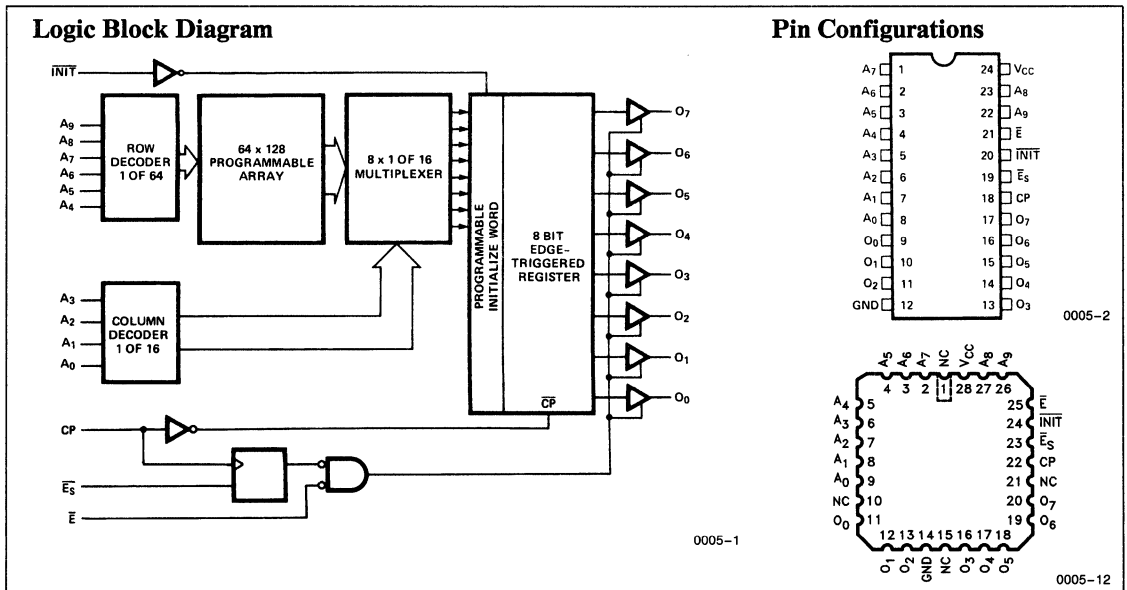
**Product Characteristics**

The CY7C235 is a high performance 1024 word by 8 bit electrically Programmable Read Only Memory packaged in a slim 300 mil plastic or hermetic DIP or 28-pin Leadless Chip carrier. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C235 replaces bipolar devices and offers the advantages of lower

power, superior performance and high programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

The CY7C235 has an asynchronous initialize function (INIT). This function acts as a 1025th 8-bit word loaded into the on-chip register. It is user programmable with any desired word or may be used as a PRESET or CLEAR function on the outputs.



**Selection Guide**

|                                |            | 7C235-25 | 7C235-30 | 7C235-40 |
|--------------------------------|------------|----------|----------|----------|
| Maximum Set-up Time (ns)       |            | 25       | 30       | 40       |
| Maximum Clock to Output (ns)   |            | 12       | 15       | 20       |
| Maximum Operating Current (mA) | Commercial | 90       | 90       | 90       |
|                                | Military   |          | 120      | 120      |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential

(Pin 24 to Pin 12 for DIP)..... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

DC Program Voltage

(Pins 7, 18, 20 for DIP) .....14.0V

Static Discharge Volume ..... >1500V  
 (Per MIL-STD-883 Method 3015)

Latch-up Current..... >200 mA

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[6]</sup> | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over Operating Range<sup>[7]</sup>

| Parameters      | Description                  | Test Conditions   | Min.       | Max. | Units |
|-----------------|------------------------------|---|------------|------|-------|
| V <sub>OH</sub> | Output HIGH Voltage          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | 2.4        |      | V     |
| V <sub>OL</sub> | Output LOW Voltage           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   |            | 0.4  | V     |
| V <sub>IH</sub> | Input HIGH Level             | Guaranteed Input Logical HIGH Voltage for All Inputs <sup>[2]</sup>                                       | 2.0        |      | V     |
| V <sub>IL</sub> | Input LOW Level              | Guaranteed Input Logical LOW Voltage for All Inputs <sup>[2]</sup>  |            | 0.8  | V     |
| I <sub>IX</sub> | Input Leakage Current        | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>   | -10        | +10  | μA    |
| V <sub>CD</sub> | Input Clamp Diode Voltage    | Note 1  |            |      |       |
| I <sub>OZ</sub> | Output Leakage Current       | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> Output Disabled <sup>[4]</sup>                                     | -40        | +40  | μA    |
| I <sub>OS</sub> | Output Short Circuit Current | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0V <sup>[3]</sup>  | -20        | -90  | mA    |
| I <sub>CC</sub> | Power Supply Current         | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub><br>V <sub>CC</sub> = Max.   | Commercial | 90   | mA    |
|                 |                              |   | Military   | 120  |       |

## Capacitance<sup>[5]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 8    |       |

### Notes:

- The CMOS process does not provide a clamp diode. However, the CY7C235 is insensitive to -3V dc input levels and -5V undershoot pulses of less than 10 ns (measured at 50% point).
- These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

**Switching Characteristics** Over Operating Range<sup>[4, 8]</sup>

| Parameters                  | Description   | 7C235-25 |      | 7C235-30 |      | 7C235-40 |      | Units |
|-----------------------------|---|----------|------|----------|------|----------|------|-------|
|                             |   | Min.     | Max. | Min.     | Max. | Min.     | Max. |       |
| t <sub>SA</sub>             | Address Setup to Clock HIGH                             | 25       |      | 30       |      | 40       |      | ns    |
| t <sub>HA</sub>             | Address Hold from Clock HIGH                            | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>CO</sub>             | Clock HIGH to Valid Output                              |          | 12   |          | 15   |          | 20   | ns    |
| t <sub>PWC</sub>            | Clock Pulse Width                                       | 12       |      | 15       |      | 20       |      | ns    |
| t <sub>SE<sub>S</sub></sub> | $\bar{E}_S$ Setup to Clock HIGH                         | 10       |      | 10       |      | 15       |      | ns    |
| t <sub>HE<sub>S</sub></sub> | $\bar{E}_S$ Hold from Clock HIGH                        | 5        |      | 5        |      | 5        |      | ns    |
| t <sub>DI</sub>             | Delay from $\bar{INIT}$ to Valid Output                 |          | 25   |          | 25   |          | 35   | ns    |
| t <sub>RI</sub>             | $\bar{INIT}$ Recovery to Clock HIGH                     | 20       |      | 20       |      | 20       |      | ns    |
| t <sub>PWI</sub>            | $\bar{INIT}$ Pulse Width                                | 20       |      | 20       |      | 25       |      | ns    |
| t <sub>COS</sub>            | Inactive to Valid Output from Clock HIGH <sup>[1]</sup> |          | 20   |          | 20   |          | 25   | ns    |
| t <sub>HZC</sub>            | Inactive Output from Clock HIGH <sup>[1, 3]</sup>       |          | 20   |          | 20   |          | 25   | ns    |
| t <sub>DOE</sub>            | Valid Output from $\bar{E}$ LOW <sup>[2]</sup>          |          | 20   |          | 20   |          | 25   | ns    |
| t <sub>HZE</sub>            | Inactive Output from $\bar{E}$ HIGH <sup>[2, 3]</sup>   |          | 20   |          | 20   |          | 25   | ns    |

**Notes:**

1. Applies only when the synchronous ( $\bar{E}_S$ ) function is used.
2. Applies only when the asynchronous ( $\bar{E}$ ) function is used.
3. Transition is measured at steady state High level - 500 mV or steady state Low level + 500 mV on the output from the 1.5V level on the input with loads shown in Figure 1b.
4. Tests are performed with rise and fall times of 5 ns or less.
5. See Figure 1a for all switching characteristics except t<sub>HZ</sub>.
6. See Figure 1b for t<sub>HZ</sub>.
7. All device test loads should be located within 2" of device outputs.
8. See the last page of this specification for Group A subgroup testing information.

**AC Test Loads and Waveforms** [5, 6, 7]

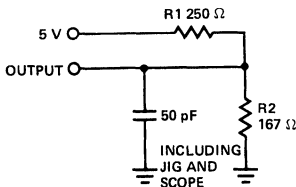


Figure 1a

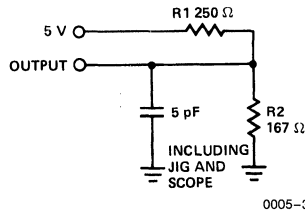
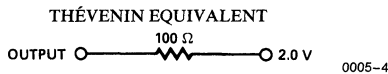


Figure 1b

Equivalent to:



0005-4

**Functional Description**

The CY7C235 is a CMOS electrically Programmable Read Only Memory organized as 1024 word x 8-bits and is a pin-pin replacement for bipolar TTL fusible link PROMs. The CY7C235 incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous ( $\bar{E}_S$ ) and asynchronous ( $\bar{E}$ ) output enables and asynchronous initialization ( $\bar{INIT}$ ).

Upon power-up, the synchronous enable ( $\bar{E}_S$ ) flip-flop will be in the set condition causing the outputs ( $O_0$ - $O_7$ ) to be in the OFF or high impedance state. Data is read by

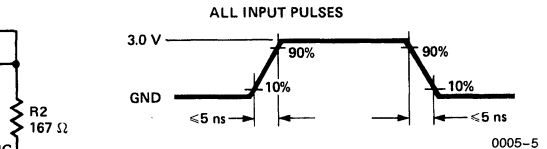


Figure 2

0005-5

applying the memory location to the address input ( $A_0$ - $A_9$ ) and a logic LOW to the enable ( $\bar{E}_S$ ) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs ( $O_0$ - $O_7$ ) provided the asynchronous enable ( $\bar{E}$ ) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable ( $\bar{E}$ ) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

## Functional Description (Continued)

Regardless of the condition of  $\bar{E}$ , the outputs will go to the OFF or high impedance state upon the next positive clock edge after the synchronous enable ( $\bar{E}_S$ ) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if  $\bar{E}$  is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low to high transition of the clock. This unique feature allows the CY7C235 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C235 has an asynchronous initialize input ( $\bar{INIT}$ ). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated the initialize control input causes the contents of a user programmed 1025th 8-bit word to be loaded into the on-chip register. Each bit is programmable

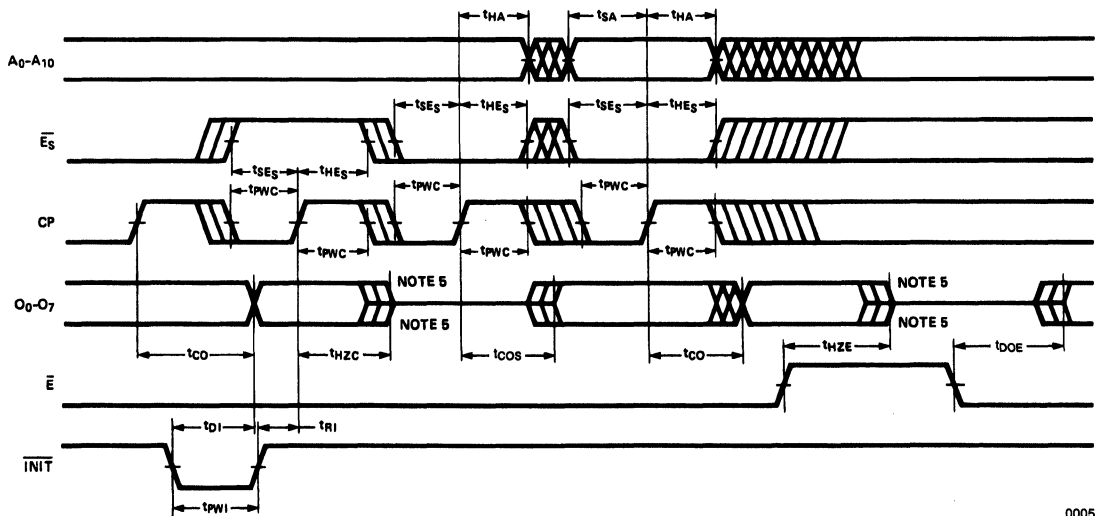
and the initialize function can be used to load any desired combination of "1"s and "0"s into the register. In the un-programmed state, activating  $\bar{INIT}$  will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating  $\bar{INIT}$  performs a register PRESET (all outputs HIGH).

Applying a LOW to the  $\bar{INIT}$  input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ( $\bar{E}$ ) LOW.

When power is applied the (internal) synchronous enable flip-flop will be in a state such that the outputs will be in the high impedance state. In order to enable the outputs, a clock must occur and the  $\bar{E}_S$  input pin must be LOW at least a setup time prior to the clock LOW to HIGH transition. The  $\bar{E}$  input may then be used to enable the outputs.

When the asynchronous initialize input,  $\bar{INIT}$ , is LOW, the data in the initialize byte will be asynchronously loaded into the output register. It will not, however, appear on the output pins until they are enabled, as described in the preceding paragraph.

## Switching Waveforms



0005-6

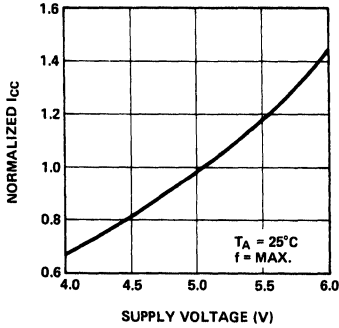
### Notes on Testing

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

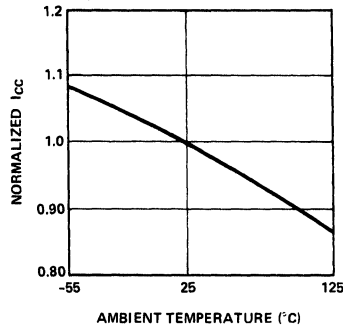
1. Ensure that adequate decoupling capacitance is employed across the device  $V_{CC}$  and ground terminals. Multiple capacitors are recommended, including a 0.1  $\mu F$  or larger capacitor and a 0.01  $\mu F$  or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level  $-500$  mV or steady state LOW level  $+500$  mV on the output from the 1.5V level on inputs with load shown in Figure 1b.

Typical DC and AC Characteristics

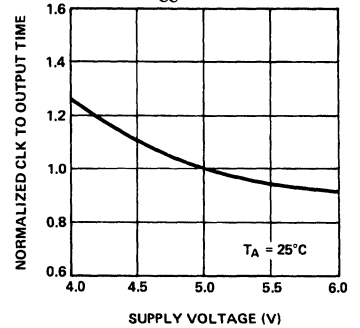
**NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE**



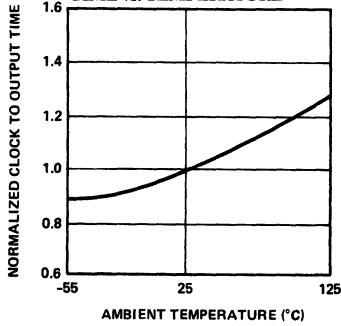
**NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE**



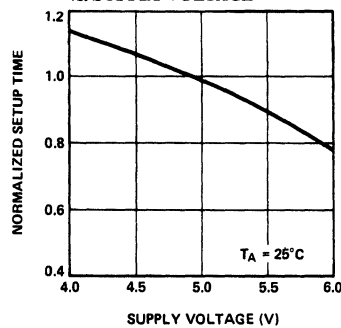
**NORMALIZED CLOCK TO OUTPUT TIME vs.  $V_{CC}$**



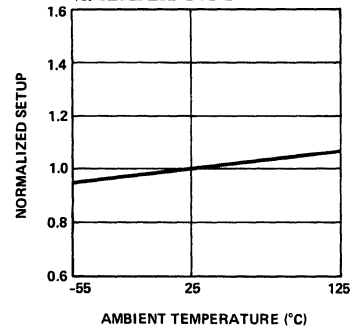
**NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE**



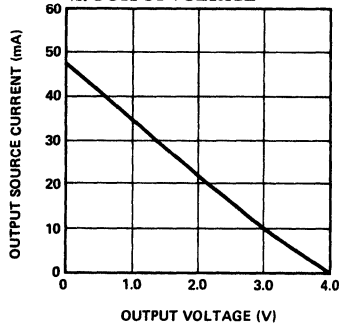
**NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE**



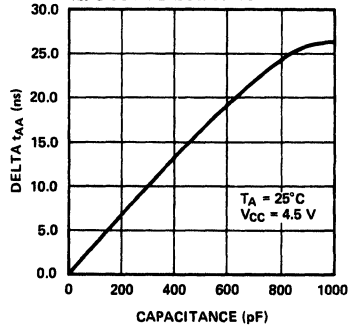
**NORMALIZED SETUP TIME vs. TEMPERATURE**



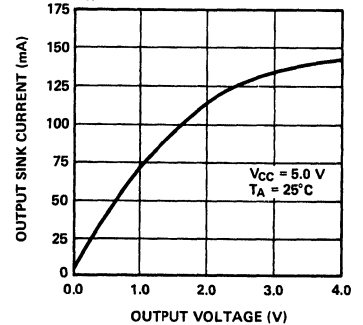
**OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE**



**TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING**



**OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE**





## Device Programming

### Overview:

There are two independent programmable functions contained in the 7C235 CMOS 1K x 8 Registered PROM; the 1K x 8 array, and the INITIAL BYTE. All of the programming elements are "EPROM" cells, and are in an erased state when the device is shipped. The erased state for the "INITIAL BYTE" is all "0's" or "LOW". The "INITIAL BYTE" may be accessed operationally through

the use of the initialize function. The 1K x 8 array uses a differential memory cell, with differential sensing techniques. In the erased state the cell contains neither a one nor a zero. The erased state of this array may be verified by using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see Table 3.

### DC Programming Parameters $T_A = 25^\circ\text{C}$

**Table 1**

| Parameter    | Description                | Min. | Max. | Units |
|--------------|----------------------------|------|------|-------|
| $V_{PP}$ [1] | Programming Voltage        | 13.0 | 14.0 | V     |
| $V_{CCP}$    | Supply Voltage             | 4.75 | 5.25 | V     |
| $V_{IHP}$    | Input High Voltage         | 3.0  |      | V     |
| $V_{ILP}$    | Input Low Voltage          |      | 0.4  | V     |
| $V_{OH}$ [2] | Output High Voltage        | 2.4  |      | V     |
| $V_{OL}$ [2] | Output Low Voltage         |      | 0.4  | V     |
| $I_{PP}$     | Programming Supply Current |      | 50   | mA    |

### AC Programming Parameters $T_A = 25^\circ\text{C}$

**Table 2**

| Parameter      | Description                 | Min. | Max.   | Units         |
|----------------|-----------------------------|------|--------|---------------|
| $t_{PP}$       | Programming Pulse Width     | 100  | 10,000 | $\mu\text{s}$ |
| $t_{AS}$       | Address Setup Time          | 1.0  |        | $\mu\text{s}$ |
| $t_{DS}$       | Data Setup Time             | 1.0  |        | $\mu\text{s}$ |
| $t_{AH}$       | Address Hold Time           | 1.0  |        | $\mu\text{s}$ |
| $t_{DH}$       | Data Hold Time              | 1.0  |        | $\mu\text{s}$ |
| $t_{R,tF}$ [3] | $V_{PP}$ Rise and Fall Time | 1.0  |        | $\mu\text{s}$ |
| $t_{VD}$       | Delay to Verify             | 1.0  |        | $\mu\text{s}$ |
| $t_{VP}$       | Verify Pulse Width          | 2.0  |        | $\mu\text{s}$ |
| $t_{DV}$       | Verify Data Valid           |      | 1.0    | $\mu\text{s}$ |
| $t_{DZ}$       | Verify HIGH to High Z       |      | 1.0    | $\mu\text{s}$ |

**Notes:**

1.  $V_{CCP}$  must be applied prior to  $V_{PP}$ .
2. During verify operation.
3. Measured 10% and 90% points.

## Mode Selection

Table 3

| Mode                                 | Pin Function           |                       |                  |                     |                         |                   |                       | Outputs<br>(9-11, 13-17)<br>DIP |
|--------------------------------------|------------------------|-----------------------|------------------|---------------------|-------------------------|-------------------|-----------------------|---------------------------------|
|                                      | Read or Output Disable | A <sub>2</sub>        | CP               | $\bar{E}_S$         | INIT                    | $\bar{E}$         | A <sub>1</sub>        |                                 |
|                                      | Other<br>(DIP) Pin     | A <sub>2</sub><br>(6) | PGM<br>(18)      | $\bar{V}FY$<br>(19) | V <sub>PP</sub><br>(20) | $\bar{E}$<br>(21) | A <sub>1</sub><br>(7) |                                 |
| Read <sup>[2,3]</sup>                |                        | X                     | X                | V <sub>IL</sub>     | V <sub>IH</sub>         | V <sub>IL</sub>   | X                     | Data Out                        |
| Output Disable <sup>[5]</sup>        |                        | X                     | X                | V <sub>IH</sub>     | V <sub>IH</sub>         | X                 | X                     | High Z                          |
| Output Disable                       |                        | X                     | X                | X                   | V <sub>IH</sub>         | V <sub>IH</sub>   | X                     | High Z                          |
| Initialize <sup>[6]</sup>            |                        | X                     | X                | X                   | V <sub>IL</sub>         | V <sub>IL</sub>   | X                     | 1025th word                     |
| Program <sup>[1,4]</sup>             |                        | X                     | V <sub>ILP</sub> | V <sub>IHP</sub>    | V <sub>PP</sub>         | V <sub>IHP</sub>  | X                     | Data In                         |
| Program Verify <sup>[1,4]</sup>      |                        | X                     | V <sub>IHP</sub> | V <sub>ILP</sub>    | V <sub>PP</sub>         | V <sub>IHP</sub>  | X                     | Data Out                        |
| Program Inhibit <sup>[1,4]</sup>     |                        | X                     | V <sub>IHP</sub> | V <sub>IHP</sub>    | V <sub>PP</sub>         | V <sub>IHP</sub>  | X                     | High Z                          |
| Intelligent Program <sup>[1,4]</sup> |                        | X                     | V <sub>ILP</sub> | V <sub>IHP</sub>    | V <sub>PP</sub>         | V <sub>IHP</sub>  | X                     | Data In                         |
| Program Initial Byte <sup>[4]</sup>  |                        | V <sub>ILP</sub>      | V <sub>ILP</sub> | V <sub>IHP</sub>    | V <sub>PP</sub>         | V <sub>IHP</sub>  | V <sub>PP</sub>       | Data In                         |
| Blank Check Ones <sup>[1,4]</sup>    |                        | X                     | V <sub>PP</sub>  | V <sub>ILP</sub>    | V <sub>ILP</sub>        | V <sub>ILP</sub>  | X                     | Ones                            |
| Blank Check Zeros <sup>[1,4]</sup>   |                        | X                     | V <sub>PP</sub>  | V <sub>IHP</sub>    | V <sub>ILP</sub>        | V <sub>ILP</sub>  | X                     | Zeros                           |

**Notes:**

1. X = Don't care but not to exceed V<sub>pp</sub>.
2. During read operation, the output latches are loaded on a "0" to "1" transition of CP.
3. Pin 19 must be LOW prior to the "0" to "1" transition on CP (18) that loads the register.
4. During programming and verification, all unspecified pins to be at V<sub>ILP</sub>.
5. Pin 19 must be HIGH prior to the "0" to "1" transition on CP (18) that loads the register.
6. LOW to HIGH clock transition required to enable outputs.

The CY7C235 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4*.

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the PGM pulse (t<sub>pp</sub>) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V<sub>CCP</sub> = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V<sub>CC</sub> = 5.0V.

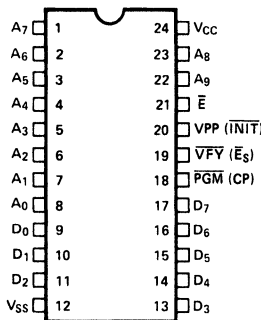


Figure 3. Programming Pinouts

0005-8

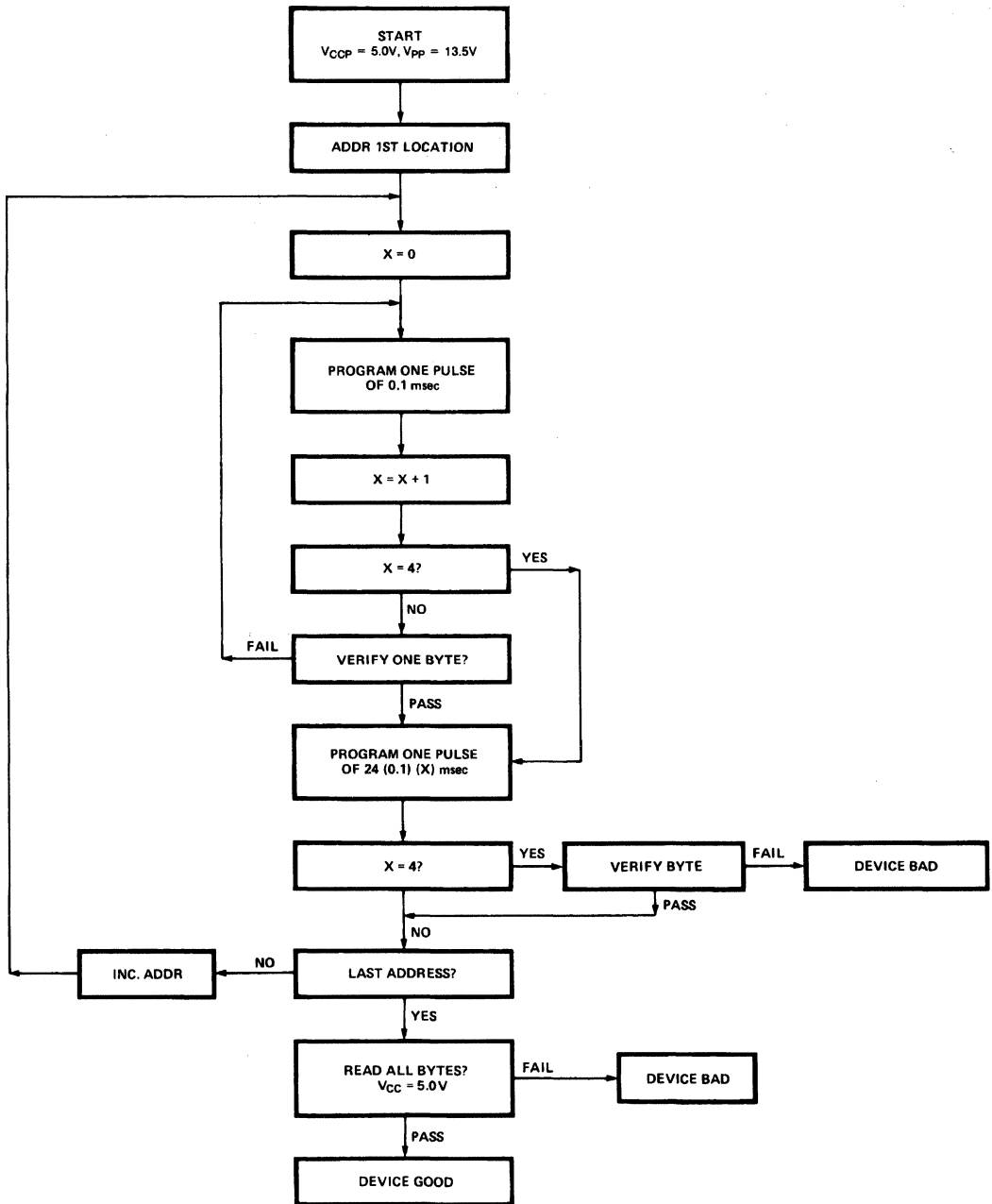


Figure 4. Programming Flowchart

### Programming Sequence 1K x 8 Array

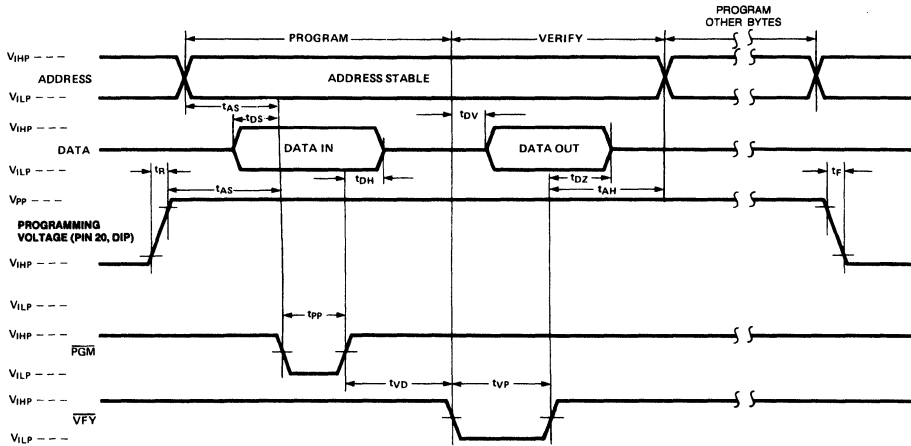
Power the device for normal read mode operation with pin 18, 19, 20 and 21 at  $V_{IH}$ . Per *Figure 6* take pin 20 to  $V_{pp}$ . The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see *Figures 5 and 6*. Again per *Figure 6* address program and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each

location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

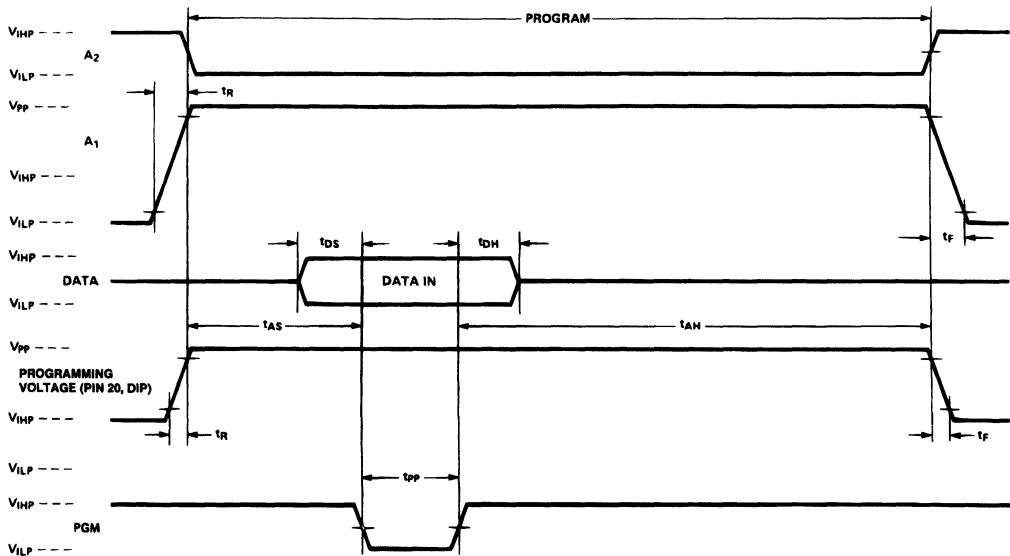
If the intelligent programming technique is used, the program pulse width should be 100  $\mu$ s. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24X the sum of the previous programming pulses before advancing to the next address to repeat the process.

3



0005-10

Figure 5. PROM Programming Waveforms



0005-11

Figure 6. Initial Byte Programming Waveforms

### Programming the Initial Byte

The CY7C235 registered PROM has a 1025th byte of data used to initialize the value of the register. This initial byte is value "0" when the part is received. If the user desires to have a value other than "0" for register initialization, this must be programmed into the 1025th byte. This byte is programmed in a similar manner to the 1024 normal bytes in the array except for two considerations. First, since all of the normal addresses of the part are used up, a super voltage will be used to create additional effective addresses. The actual address has V<sub>pp</sub> on A<sub>1</sub> pin 7, and V<sub>ILP</sub> on A<sub>2</sub> pin 6, per Table 3. The programming and verification of "INITIAL BYTE" is accomplished operationally by performing an initialize function.

### Bit Map Data

| Programmer Address |     | RAM Data  |
|--------------------|-----|-----------|
| Decimal            | Hex | Contents  |
| 0                  | 0   | Data      |
| •                  | •   | •         |
| •                  | •   | •         |
| •                  | •   | •         |
| 1023               | 3FF | Data      |
| 1024               | 400 | Init Byte |

### Blank Check

A virgin device contains neither one's nor zero's because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 1023. A device is considered virgin if all locations are respectively "1's" and "0's" when addresses in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both one's and zero's. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

### Ordering Information

| Speed ns        |                 | Ordering Code | Package Type      | Operating Range |
|-----------------|-----------------|---------------|-------------------|-----------------|
| t <sub>SA</sub> | t <sub>CO</sub> |               |                   |                 |
| 25              | 12              | CY7C235-25PC  | P13<br>D14        | Commercial      |
|                 |                 | CY7C235-25DC  |                   |                 |
| 30              | 15              | CY7C235-30PC  | P13<br>D14<br>J64 | Commercial      |
|                 |                 | CY7C235-30DC  |                   |                 |
| 40              | 20              | CY7C235-30JLC | D14<br>L64        | Military        |
|                 |                 | CY7C235-30DMB |                   |                 |
| 40              | 20              | CY7C235-40PC  | P13<br>D14        | Commercial      |
|                 |                 | CY7C235-40DC  |                   |                 |
| 40              | 20              | CY7C235-40DMB | D14<br>L64        | Military        |
|                 |                 | CY7C235-40LMB |                   |                 |

**MILITARY SPECIFICATIONS****Group A Subgroup Testing****DC Characteristics**

| Parameters      | Subgroups |
|-----------------|-----------|
| V <sub>OH</sub> | 1,2,3     |
| V <sub>OL</sub> | 1,2,3     |
| V <sub>IH</sub> | 1,2,3     |
| V <sub>IL</sub> | 1,2,3     |
| I <sub>IX</sub> | 1,2,3     |
| I <sub>OZ</sub> | 1,2,3     |
| I <sub>CC</sub> | 1,2,3     |

3

**Switching Characteristics**

| Parameters      | Subgroups   |
|-----------------|-------------|
| t <sub>SA</sub> | 7,8,9,10,11 |
| t <sub>HA</sub> | 7,8,9,10,11 |
| t <sub>CO</sub> | 7,8,9,10,11 |

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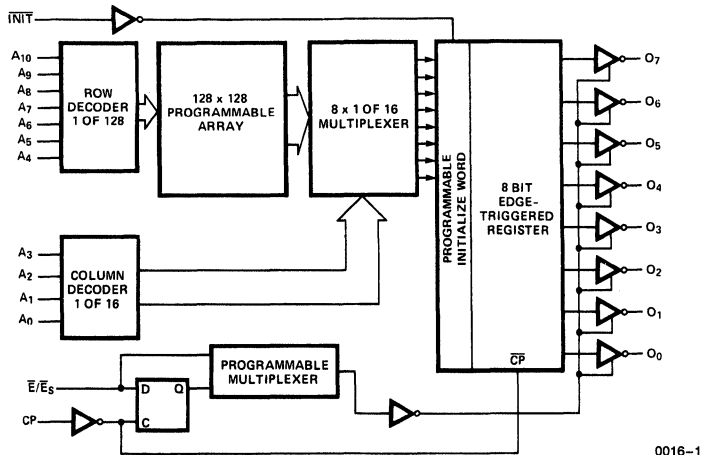


# Reprogrammable 2048 x 8 Registered PROM

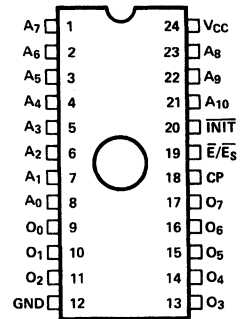
## Features

- Windowed for reprogrammability
- CMOS for optimum speed/power
- High speed
  - 25 ns max set-up
  - 12 ns clock to output
- Low power
  - 330 mW (commercial) for
  - 35 ns, -45 ns
  - 660 mW (military)
- Programmable synchronous or asynchronous output enable
- On-chip edge-triggered registers
- Programmable asynchronous register (INIT)
- EPROM technology, 100% programmable
- Slim, 300 mil, 24 pin plastic or hermetic DIP
- 5V ±10% V<sub>CC</sub>, commercial and military
- TTL compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 2000V static discharge

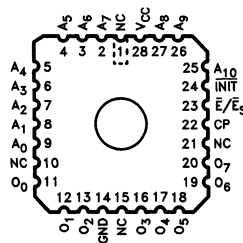
## Logic Block Diagram



## Pin Configurations



0016-2



0016-13

## Selection Guide

|                                |     |            | 7C245-25 | 7C245-35 | 7C245-45 |
|--------------------------------|-----|------------|----------|----------|----------|
| Maximum Setup Time (ns)        |     |            | 25       | 35       | 45       |
| Maximum Clock to Output (ns)   |     |            | 12       | 15       | 25       |
| Maximum Operating Current (mA) | STD | Commercial | 90       | 90       | 90       |
|                                |     | Military   |          | 120      | 120      |
|                                | L   | Commercial |          | 60       | 60       |

## Product Characteristics

The CY7C245 is a high performance 2048 word by 8 bit electrically Programmable Read Only Memory packaged in a slim 300 mil plastic or hermetic DIP. The ceramic package may be equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C245 replaces bipolar devices and offers the advantages of lower power, reprogrammability, superior performance and high programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

The CY7C245 has an asynchronous initialize function (INIT). This function acts as a 2049th 8-bit word loaded into the on-chip register. It is user programmable with any desired word or may be used as a PRESET or CLEAR function on the outputs.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|  |                           |
|--|---------------------------|
| Storage Temperature                                    | −65°C to +150°C           |
| Ambient Temperature with Power Applied                 | −55°C to +125°C           |
| Supply Voltage to Ground Potential (Pin 24 to Pin 12)  | −0.5V to +7.0V            |
| DC Voltage Applied to Outputs in High Z State          | −0.5V to +7.0V            |
| DC Input Voltage                                       | −3.0V to +7.0V            |
| DC Program Voltage (Pins 7, 18, 20)                    | 13.0V                     |
| UV Erasure   | 7258 Wsec/cm <sup>2</sup> |
| Static Discharge Voltage (Per MIL-STD-883 Method 3015) | > 2001V                   |
| Latchup Current  | > 200 mA                  |

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ±10%         |
| Military <sup>[7]</sup> | −55°C to +125°C     | 5V ±10%         |

## Electrical Characteristics Over Operating Range<sup>[6]</sup>

| Parameters      | Description                  | Test Conditions   | 7C245L-35, 45 |                 | 7C245-25 |                 | 7C245-35, 45 |                 | Units |
|-----------------|------------------------------|---|---------------|-----------------|----------|-----------------|--------------|-----------------|-------|
|                 |                              |   | Min.          | Max.            | Min.     | Max.            | Min.         | Max.            |       |
| V <sub>OH</sub> | Output HIGH Voltage          | V <sub>CC</sub> = Min., I <sub>OH</sub> = −4.0 mA<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | 2.4           |                 | 2.4      |                 | 2.4          |                 | V     |
| V <sub>OL</sub> | Output LOW Voltage           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   |               | 0.4             |          | 0.4             |              | 0.4             | V     |
| V <sub>IH</sub> | Input HIGH Level             | Guaranteed Input Logical HIGH Voltage for All Inputs <sup>[1]</sup>                                       | 2.0           | V <sub>CC</sub> | 2.0      | V <sub>CC</sub> | 2.0          | V <sub>CC</sub> | V     |
| V <sub>IL</sub> | Input LOW Level              | Guaranteed Input Logical LOW Voltage for All Inputs <sup>[1]</sup>  |               | 0.8             |          | 0.8             |              | 0.8             | V     |
| I <sub>IX</sub> | Input Leakage Current        | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>   | −10           | +10             | −10      | +10             | −10          | +10             | μA    |
| V <sub>CD</sub> | Input Clamp Diode Voltage    | Note 5  | Note 5        |                 |          |                 |              |                 |       |
| I <sub>OZ</sub> | Output Leakage Current       | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub><br>Output Disabled <sup>[3]</sup>                                  | −40           | +40             | −40      | +40             | −40          | +40             | μA    |
| I <sub>OS</sub> | Output Short Circuit Current | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0V <sup>[2]</sup>  | −20           | −90             | −20      | −90             | −20          | −90             | mA    |
| I <sub>CC</sub> | Power Supply Current         | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub><br>V <sub>CC</sub> = Max.   | Commercial    |                 | 90       |                 | 90           |                 | mA    |
|                 |                              |   | Military      |                 |          |                 | 120          |                 |       |

## Capacitance<sup>[4]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 8    |       |

### Notes:

- These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
- Tested initially and after any design or process changes that may affect these parameters.
- The CMOS process does not provide a clamp diode. However, the CY7C245 is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
- See the last page of this specification for Group A subgroup testing information.
- T<sub>A</sub> is the “instant on” case temperature.



### Switching Characteristics Over Operating Range<sup>[8]</sup>

| Parameters                  | Description   | 7C245-25 |      | 7C245-35 |      | 7C245-45 |      | Units |
|-----------------------------|---|----------|------|----------|------|----------|------|-------|
|                             |   | Min.     | Max. | Min.     | Max. | Min.     | Max. |       |
| t <sub>SA</sub>             | Address Setup to Clock HIGH                           | 25       |      | 35       |      | 45       |      | ns    |
| t <sub>HA</sub>             | Address Hold from Clock HIGH                          | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>CO</sub>             | Clock HIGH to Valid Output                            |          | 12   |          | 15   |          | 25   | ns    |
| t <sub>PWC</sub>            | Clock Pulse Width                                     | 15       |      | 20       |      | 20       |      | ns    |
| t <sub>SE<sub>S</sub></sub> | $\bar{E}_S$ Setup to Clock HIGH                       | 12       |      | 15       |      | 15       |      | ns    |
| t <sub>HE<sub>S</sub></sub> | $\bar{E}_S$ Hold from Clock HIGH                      | 5        |      | 5        |      | 5        |      | ns    |
| t <sub>DI</sub>             | Delay from $\bar{INIT}$ to Valid Output               |          | 20   |          | 20   |          | 35   | ns    |
| t <sub>RI</sub>             | $\bar{INIT}$ Recovery to Clock HIGH                   | 15       |      | 20       |      | 20       |      | ns    |
| t <sub>PWI</sub>            | $\bar{INIT}$ Pulse Width                              | 15       |      | 20       |      | 25       |      | ns    |
| t <sub>COS</sub>            | Valid Output from Clock HIGH <sup>[1]</sup>           |          | 15   |          | 20   |          | 30   | ns    |
| t <sub>HZC</sub>            | Inactive Output from Clock HIGH <sup>[1, 3]</sup>     |          | 15   |          | 20   |          | 30   | ns    |
| t <sub>DOE</sub>            | Valid Output from $\bar{E}$ LOW <sup>[2]</sup>        |          | 15   |          | 20   |          | 30   | ns    |
| t <sub>HZE</sub>            | Inactive Output from $\bar{E}$ HIGH <sup>[2, 3]</sup> |          | 15   |          | 20   |          | 30   | ns    |

**Notes:**

1. Applies only when the synchronous ( $\bar{E}_S$ ) function is used.
2. Applies only when the asynchronous ( $\bar{E}$ ) function is used.
3. Transition is measured at steady state High level - 500 mV or steady state Low level + 500 mV on the output from the 1.5V level on the input with loads shown in Figure 1b.
4. Tests are performed with rise and fall times of 5 ns or less.
5. See Figure 1a for all switching characteristics except t<sub>HZ</sub>.
6. See Figure 1b for t<sub>HZ</sub>.
7. All device test loads should be located within 2" of device outputs.
8. See the last page of this specification for Group A subgroup testing information.

### AC Test Loads and Waveforms<sup>[5, 6, 7]</sup>

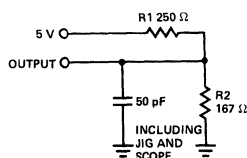


Figure 1a

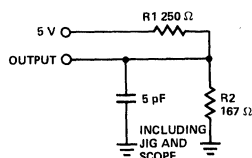


Figure 1b

0016-3

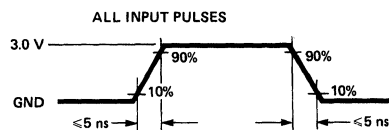
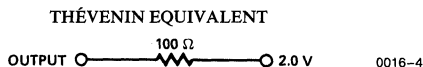


Figure 2

0016-5

Equivalent to:



0016-4

### Functional Description

The CY7C245 is a CMOS electrically Programmable Read Only Memory organized as 2048 words x 8-bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The CY7C245 incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with a programmable synchronous ( $\bar{E}_S$ ) or asynchronous ( $\bar{E}$ ) output enable and asynchronous initialization ( $\bar{INIT}$ ).

Upon power-up the state of the outputs will depend on the programmed state of the enable function ( $\bar{E}_S$  or  $\bar{E}$ ). If the synchronous enable ( $\bar{E}_S$ ) has been programmed, the register will be in the set condition causing the outputs

(O<sub>0</sub>-O<sub>7</sub>) to be in the OFF or high impedance state. If the asynchronous enable ( $\bar{E}$ ) is being used, the outputs will come up in the OFF or high impedance state only if the enable ( $\bar{E}$ ) input is at a HIGH logic level. Data is read by applying the memory location to the address inputs (A<sub>0</sub>-A<sub>10</sub>) and a logic LOW to the enable input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs (O<sub>0</sub>-O<sub>7</sub>).

If the asynchronous enable ( $\bar{E}$ ) is being used, the outputs may be disabled at any time by switching the enable to a

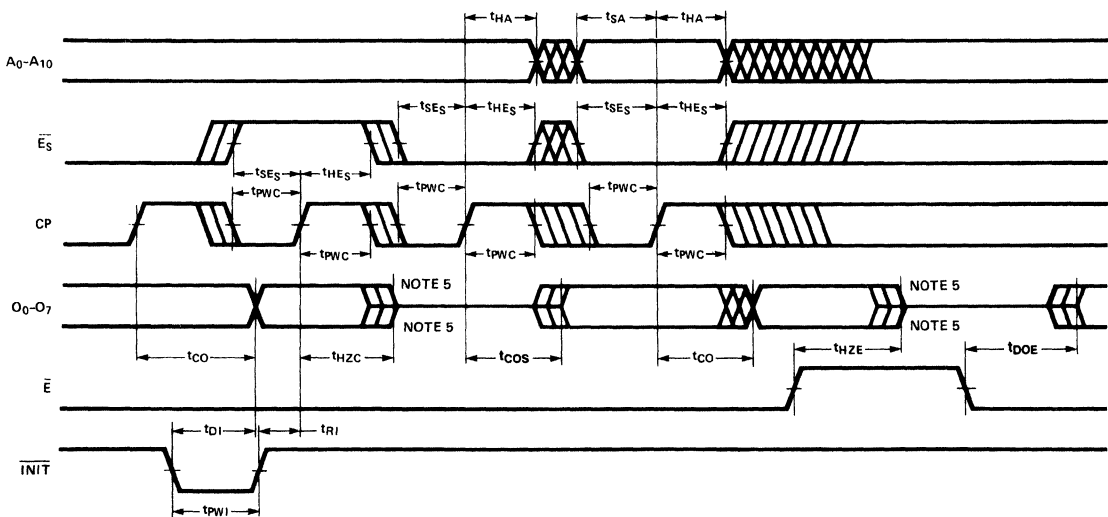
## Functional Description (Continued)

logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

If the synchronous enable ( $\overline{E}_S$ ) is being used, the outputs will go to the OFF or high impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low to high transition of the clock. This unique feature allows the CY7C245 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

## Switching Waveforms



0016-6

### Notes on Testing

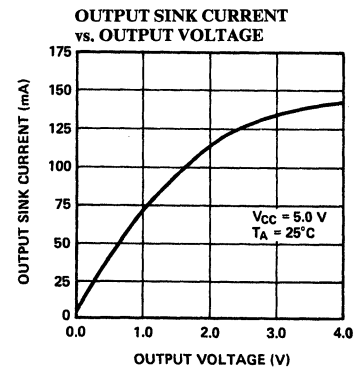
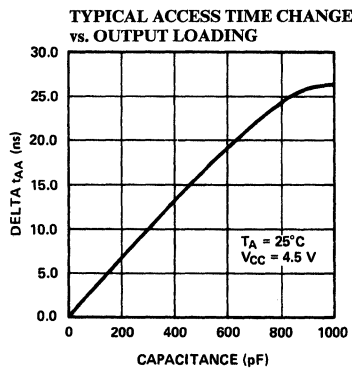
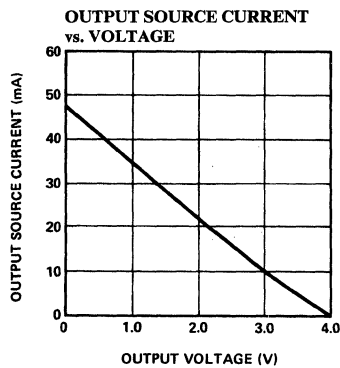
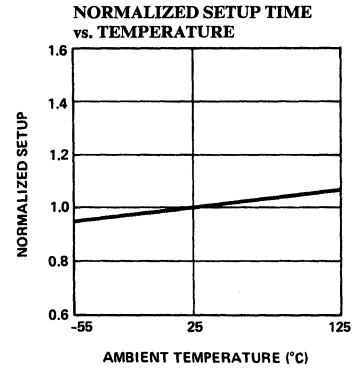
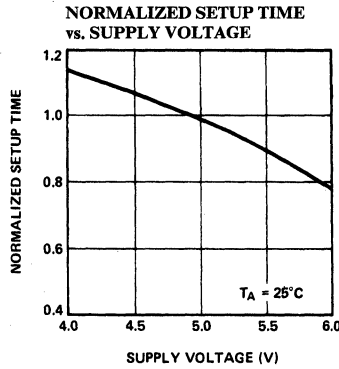
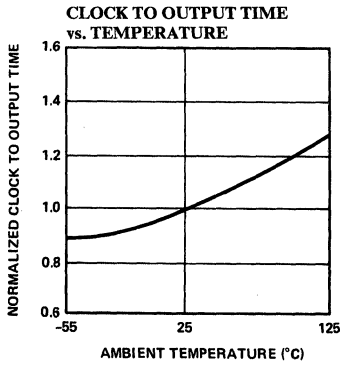
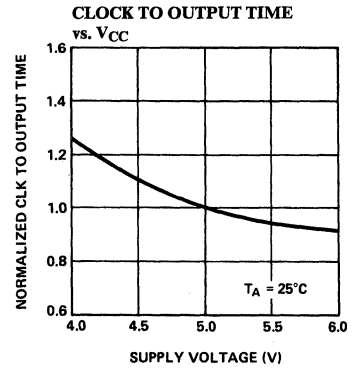
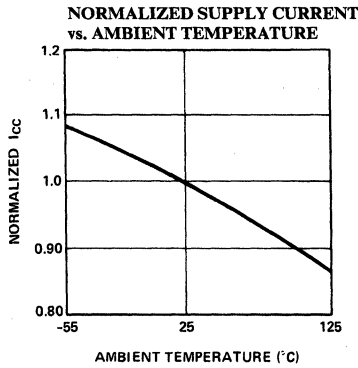
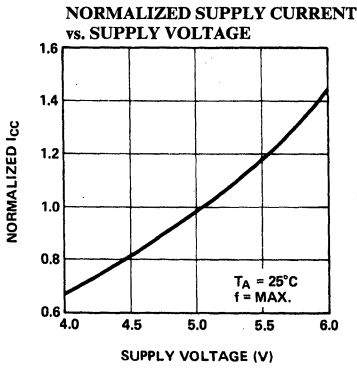
Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device  $V_{CC}$  and ground terminals. Multiple capacitors are recommended, including a 0.1  $\mu\text{F}$  or larger capacitor and a 0.01  $\mu\text{F}$  or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.

The CY7C245 has an asynchronous initialize input ( $\overline{INIT}$ ). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated the initialize control input causes the contents of a user programmed 2049th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of "1"s and "0"s into the register. In the unprogrammed state, activating  $\overline{INIT}$  will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating  $\overline{INIT}$  performs a register PRESET (all outputs HIGH).

Applying a LOW to the  $\overline{INIT}$  input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable (E) LOW.

Typical DC and AC Characteristics



## Erase Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C245. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity  $\times$  exposure time) of 25 Wsec/cm<sup>2</sup>. For an ultraviolet lamp with a 12 mW/cm<sup>2</sup> power rating the exposure time would be approximately 30–35 minutes. The 7C245 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm<sup>2</sup> is the recommended maximum dosage.

## Device Programming

### OVERVIEW:

There are three independent programmable functions contained in the 7C245 CMOS 2K x 8 Registered PROM; the 2K x 8 array, the initial byte, and the synchronous enable bit. All of the programming elements are “EPROM” cells, and are in an erased state when the device is shipped. This erased state manifests itself differently in each case. The erased state for ENABLE bit is the “ASYNCHRONOUS ENABLE” mode. The erased state for the “INITIAL BYTE” is all “0’s” or “LOW”. The “INITIAL BYTE” may be accessed operationally thru the use of the initialize function. The 2K x 8 array uses a differential memory cell, with differential sensing techniques. In the erased state the cell contains neither a one nor a zero. The erased state of this array may be verified by using the “BLANK CHECK ONES” and “BLANK CHECK ZEROS” function, see Table 3.

## DC Programming Parameters $T_A = 25^\circ\text{C}$

**Table 1**

| Parameter           | Description                | Min. | Max. | Units |
|---------------------|----------------------------|------|------|-------|
| V <sub>PP</sub> [1] | Programming Voltage        | 12.0 | 13.0 | V     |
| V <sub>CCP</sub>    | Supply Voltage             | 4.75 | 5.25 | V     |
| V <sub>IHP</sub>    | Input High Voltage         | 3.0  |      | V     |
| V <sub>ILP</sub>    | Input Low Voltage          |      | 0.4  | V     |
| V <sub>OH</sub> [2] | Output High Voltage        | 2.4  |      | V     |
| V <sub>OL</sub> [2] | Output Low Voltage         |      | 0.4  | V     |
| I <sub>PP</sub>     | Programming Supply Current |      | 50   | mA    |

## AC Programming Parameters $T_A = 25^\circ\text{C}$

**Table 2**

| Parameter                           | Description                        | Min. | Max.   | Units         |
|-------------------------------------|------------------------------------|------|--------|---------------|
| t <sub>PP</sub>                     | Programming Pulse Width            | 100  | 10,000 | $\mu\text{s}$ |
| t <sub>AS</sub>                     | Address Setup Time                 | 1.0  |        | $\mu\text{s}$ |
| t <sub>DS</sub>                     | Data Setup Time                    | 1.0  |        | $\mu\text{s}$ |
| t <sub>AH</sub>                     | Address Hold Time                  | 1.0  |        | $\mu\text{s}$ |
| t <sub>DH</sub>                     | Data Hold Time                     | 1.0  |        | $\mu\text{s}$ |
| t <sub>R</sub> , t <sub>F</sub> [3] | V <sub>PP</sub> Rise and Fall Time | 1.0  |        | $\mu\text{s}$ |
| t <sub>VD</sub>                     | Delay to Verify                    | 1.0  |        | $\mu\text{s}$ |
| t <sub>VP</sub>                     | Verify Pulse Width                 | 2.0  |        | $\mu\text{s}$ |
| t <sub>DV</sub>                     | Verify Data Valid                  |      | 1.0    | $\mu\text{s}$ |
| t <sub>DZ</sub>                     | Verify HIGH to High Z              |      | 1.0    | $\mu\text{s}$ |

**Notes:**

1. V<sub>CCP</sub> must be applied prior to V<sub>PP</sub>.
2. During verify operation.
3. Measured 10% and 90% points.

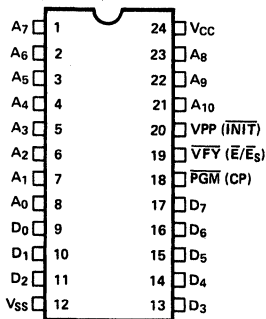
## Mode Selection

Table 3

| Mode                                 | Pin Function           |                  |                  |                     |                  |                 | Outputs<br>(9–11, 13–17) |
|--------------------------------------|------------------------|------------------|------------------|---------------------|------------------|-----------------|--------------------------|
|                                      | Read or Output Disable | A <sub>2</sub>   | CP               | $\bar{E}/\bar{E}_S$ | INIT             | A <sub>1</sub>  |                          |
|                                      | Other                  | A <sub>2</sub>   | PGM              | V <sub>FY</sub>     | V <sub>PP</sub>  | A <sub>1</sub>  |                          |
|                                      | Pin                    | (6)              | (18)             | (19)                | 20               | (7)             |                          |
| Read <sup>[2,3]</sup>                |                        | X                | X                | V <sub>IL</sub>     | V <sub>IH</sub>  | X               | Data Out                 |
| Output Disable <sup>[5]</sup>        |                        | X                | X                | V <sub>IH</sub>     | V <sub>IH</sub>  | X               | High Z                   |
| Program <sup>[1,4]</sup>             |                        | X                | V <sub>ILP</sub> | V <sub>IHP</sub>    | V <sub>PP</sub>  | X               | Data In                  |
| Program Verify <sup>[1,4]</sup>      |                        | X                | V <sub>IHP</sub> | V <sub>ILP</sub>    | V <sub>PP</sub>  | X               | Data Out                 |
| Program Inhibit <sup>[1,4]</sup>     |                        | X                | V <sub>IHP</sub> | V <sub>IHP</sub>    | V <sub>PP</sub>  | X               | High Z                   |
| Intelligent Program <sup>[1,4]</sup> |                        | X                | V <sub>ILP</sub> | V <sub>IHP</sub>    | V <sub>PP</sub>  | X               | Data In                  |
| Program Synch Enable <sup>[4]</sup>  |                        | V <sub>IHP</sub> | V <sub>ILP</sub> | V <sub>IHP</sub>    | V <sub>PP</sub>  | V <sub>PP</sub> | High Z                   |
| Program Initial Byte <sup>[4]</sup>  |                        | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>IHP</sub>    | V <sub>PP</sub>  | V <sub>PP</sub> | Data In                  |
| Blank Check Ones <sup>[1,4]</sup>    |                        | X                | V <sub>PP</sub>  | V <sub>ILP</sub>    | V <sub>ILP</sub> | X               | Ones                     |
| Blank Check Zeros <sup>[1,4]</sup>   |                        | X                | V <sub>PP</sub>  | V <sub>IHP</sub>    | V <sub>ILP</sub> | X               | Zeros                    |

**Notes:**

1. X = Don't care but not to exceed V<sub>pp</sub>.
2. During read operation, the output latches are loaded on a "0" to "1" transition of CP.
3. If the registered device is being operated in a synchronous mode, pin 19 must be LOW prior to the "0" to "1" transition on CP (18) that loads the register.
4. During programming and verification, all unspecified pins to be at V<sub>ILP</sub>.
5. If the registered device is being operated in a synchronous mode, pin 19 must be HIGH prior to the "0" to "1" transition on CP (18) that loads the register.



0016-8

Figure 3. Programming Pinouts

The CY7C245 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in Figure 4.

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the PGM pulse (t<sub>pp</sub>) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V<sub>CCP</sub> = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V<sub>CC</sub> = 5.0V.

## Bit Map Data

| Programmer | Address | RAM Data     |
|------------|---------|--------------|
| Decimal    | Hex     | Contents     |
| 0          | 0       | DATA         |
| •          | •       | •            |
| •          | •       | •            |
| •          | •       | •            |
| 2047       | 7FF     | DATA         |
| 2048       | 800     | INIT BYTE    |
| 2049       | 801     | CONTROL BYTE |

**Control Byte**

- 00 Asynchronous output enable (default state)
- 01 Synchronous output enable

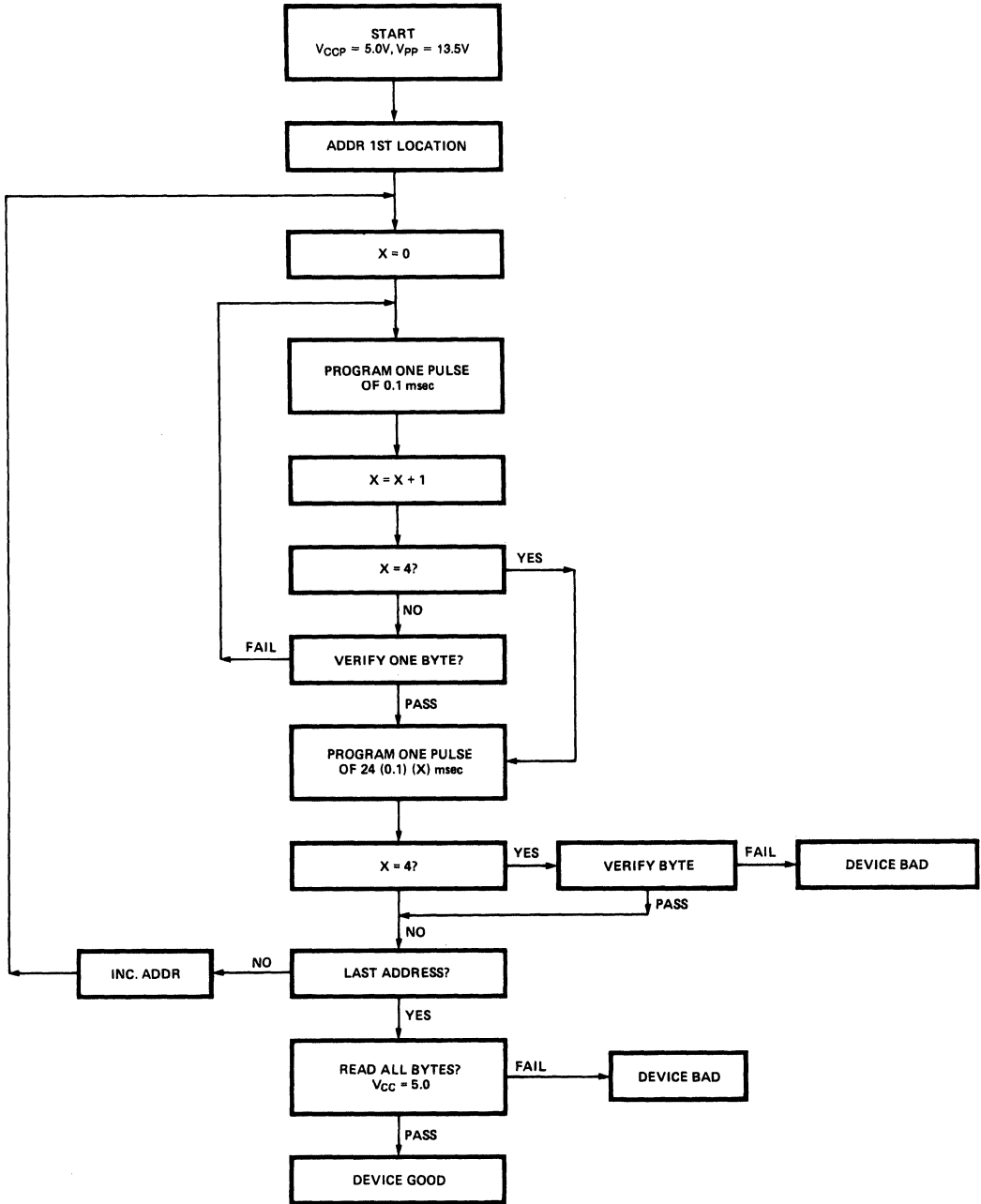


Figure 4. Programming Flowchart

### Programming Sequence 2K x 8 Array

Power the device for normal read mode operation with pin 18, 19 and 20 at  $V_{IH}$ . Per *Figure 5* take pin 20 to  $V_{pp}$ . The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see *Figures 5* and *6*. Again per *Figure 5* address program and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each

location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100  $\mu$ s. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24X the sum of the previous programming pulses before advancing to the next address to repeat the process.

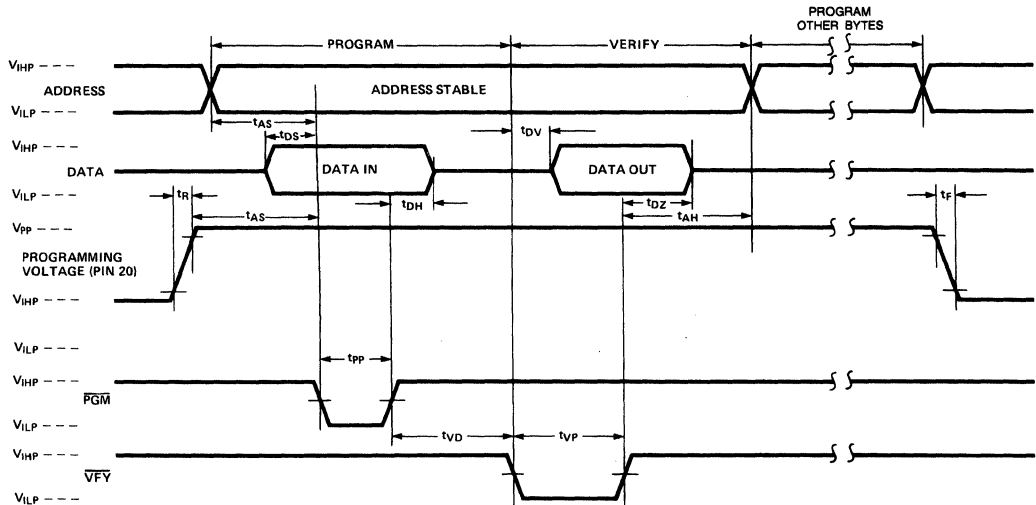


Figure 5. PROM Programming Waveforms

0016-10

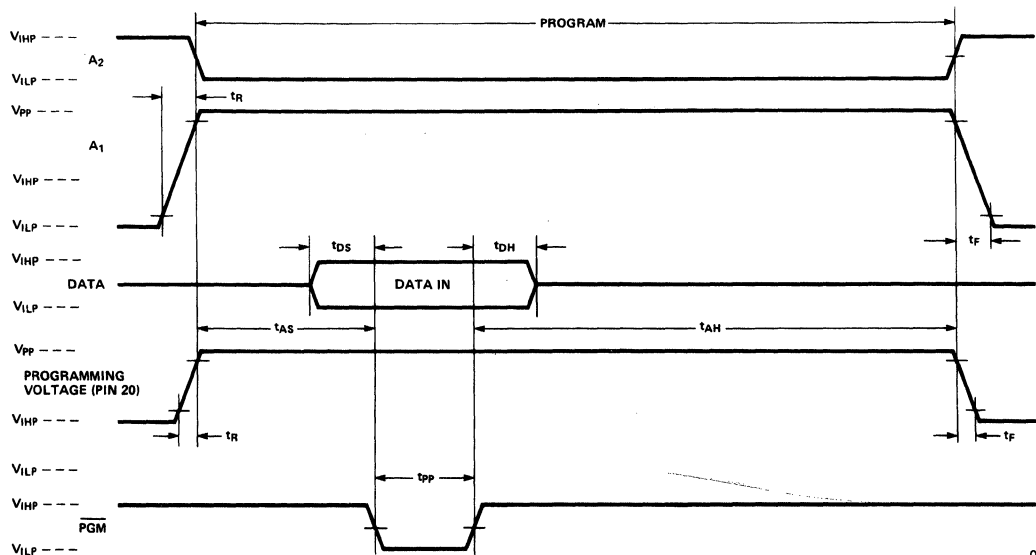


Figure 6. Initial Byte Programming Waveforms

0016-11

## Programming the Initialization Byte

The CY7C245 registered PROM has a 2049th byte of data used to initialize the value of the register. This initial byte is value "0" when the part is received. If the user desires to have a value other than "0" for register initialization, this must be programmed into the 2049th byte. This byte is programmed in a similar manner to the 2048 normal bytes in the array except for two considerations. First, since all of the normal addresses of the part are used up, a super voltage will be used to create additional effective addresses. The actual address has  $V_{pp}$  on  $A_1$  pin 7, and  $V_{ILP}$  on  $A_2$ , pin 6, per Table 3. The programming and verification of "INITIAL BYTE" is accomplished operationally by performing an initialize function.

## Programming Synchronous Enable

The CY7C245 provides for both a synchronous and asynchronous enable function. The device is delivered in an asynchronous mode of operation and only requires that the user alter the device if synchronous operation is required. The determination of the option is accomplished thru the use of an EPROM cell which is programmed only if synchronous operation is required. As with the INITIAL byte, this function is addressed thru the use of a supervoltage. Per Table 3,  $V_{pp}$  is applied to pin 7 ( $A_1$ ) with pin 6 ( $A_2$ ) at  $V_{IHP}$ . This addresses the cell that programs synchronous enable. Programming the cell is accomplished with a 10 ms program pulse on pin 18 (PGM) but does not require any data as there is no choice as to how synchronous enable may be programmed, only if it is to be programmed.

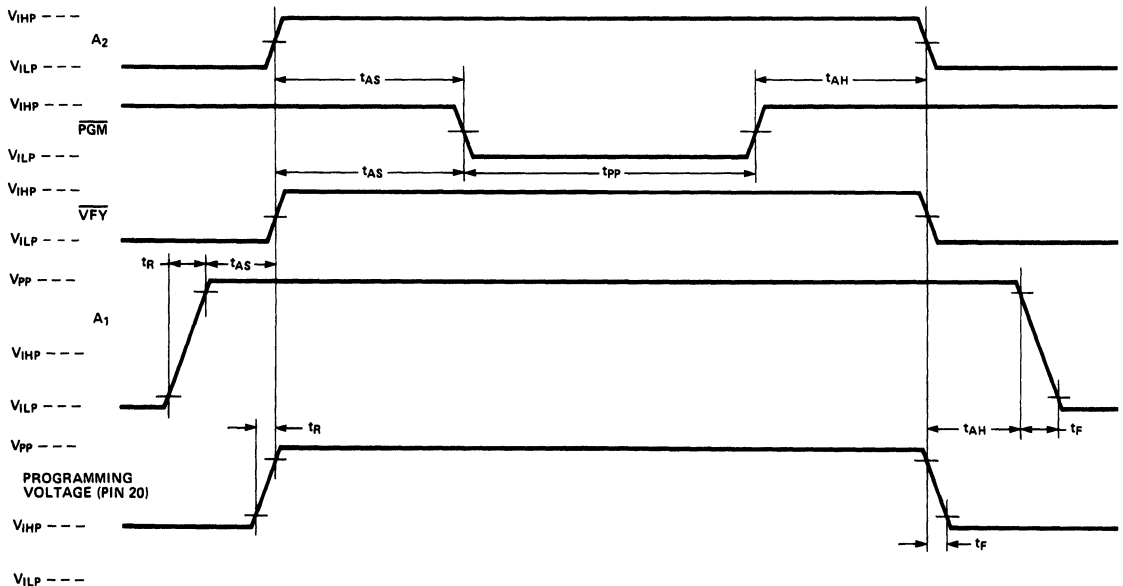
**3**


Figure 7. Program Synchronous Enable

0016-12

## Verification of Synchronous Enable

Verification of the synchronous enable function is accomplished operationally. Power the device for read operation with pin 20 at  $V_{IH}$ , cause clock pin 18 to transition from  $V_{IL}$  to  $V_{IH}$ . The output should be in a High Z state. Take pin 20,  $\overline{ENABLE}$ , to  $V_{IL}$ . The outputs should remain in a high Z state. Transition the clock from  $V_{IL}$  to  $V_{IH}$ , the outputs should now contain the data that is present. Again set pin 19 to  $V_{IH}$ . The output should remain driven. Clocking pin 18 once more from  $V_{IL}$  to  $V_{IH}$  should place the outputs again in a High Z state.

## Blank Check

A virgin device contains neither one's nor zero's because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 2047. A device is considered virgin if all locations are respectively "1's" and "0's" when addressed in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both one's and zero's. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.



**Ordering Information**

| Speed (ns)      |                 | I <sub>CC</sub><br>mA | Ordering<br>Code | Package<br>Type | Operating<br>Range |          |
|-----------------|-----------------|-----------------------|------------------|-----------------|--------------------|----------|
| t <sub>SA</sub> | t <sub>CO</sub> |                       |                  |                 |                    |          |
| 25              | 12              | 90                    | CY7C245-25PC     | P13             | Commercial         |          |
|                 |                 |                       | CY7C245-25WC     | W14             |                    |          |
| 35              | 15              | 60                    | CY7C245L-35PC    | P13             | Commercial         |          |
|                 |                 |                       | CY7C245L-35WC    | W14             |                    |          |
|                 |                 | 90                    | CY7C245-35PC     | P13             |                    |          |
|                 |                 |                       | CY7C245-35SC     | S13             |                    |          |
|                 |                 |                       | CY7C245-35WC     | W14             |                    |          |
|                 |                 |                       | CY7C245-35LC     | L64             |                    |          |
|                 |                 | 120                   | CY7C245-35DMB    | D14             |                    | Military |
|                 |                 |                       | CY7C245-35QMB    | Q64             |                    |          |
|                 |                 |                       | CY7C245-35WMB    | W14             |                    |          |
|                 |                 |                       | CY7C245-35LMB    | L64             |                    |          |

| Speed (ns)      |                 | I <sub>CC</sub><br>mA | Ordering<br>Code | Package<br>Type | Operating<br>Range |          |
|-----------------|-----------------|-----------------------|------------------|-----------------|--------------------|----------|
| t <sub>SA</sub> | t <sub>CO</sub> |                       |                  |                 |                    |          |
| 45              | 25              | 60                    | CY7C245L-45PC    | P13             | Commercial         |          |
|                 |                 |                       | CY7C245L-45WC    | W14             |                    |          |
|                 |                 | 90                    | CY7C245-45PC     | P13             |                    |          |
|                 |                 |                       | CY7C245-45SC     | S13             |                    |          |
|                 |                 |                       | CY7C245-45WC     | W14             |                    |          |
|                 |                 |                       | CY7C245-45LC     | L64             |                    |          |
|                 |                 | 120                   | CY7C245-45WMB    | W14             |                    | Military |
|                 |                 |                       | CY7C245-45LMB    | L64             |                    |          |
|                 |                 |                       | CY7C245-45DMB    | D14             |                    |          |
|                 |                 |                       | CY7C245-45QMB    | Q64             |                    |          |

**MILITARY SPECIFICATIONS****Group A Subgroup Testing****DC Characteristics**

| Parameters      | Subgroups |
|-----------------|-----------|
| V <sub>OH</sub> | 1,2,3     |
| V <sub>OL</sub> | 1,2,3     |
| V <sub>IH</sub> | 1,2,3     |
| V <sub>IL</sub> | 1,2,3     |
| I <sub>IX</sub> | 1,2,3     |
| I <sub>OZ</sub> | 1,2,3     |
| I <sub>CC</sub> | 1,2,3     |

3

**Switching Characteristics**

| Parameters      | Subgroups   |
|-----------------|-------------|
| t <sub>SA</sub> | 7,8,9,10,11 |
| t <sub>HA</sub> | 7,8,9,10,11 |
| t <sub>CO</sub> | 7,8,9,10,11 |

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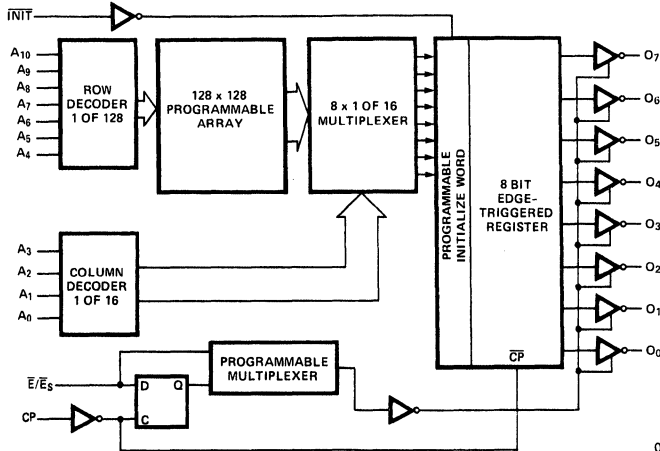


# Reprogrammable 2048 x 8 Registered PROM

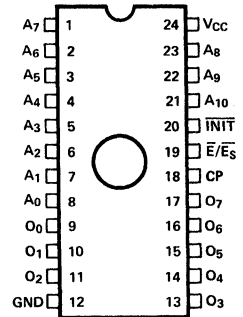
## Features

- **Wired for reprogrammability**
- **CMOS for optimum speed/power**
- **High speed**
  - 15 ns max set-up
  - 10 ns clock to output
- **Low power**
  - 330 mW (commercial) for — 35 ns
  - 660 mW (military)
- **Programmable synchronous or asynchronous output enable**
- **On-chip edge-triggered registers**
- **Programmable asynchronous register (INIT)**
- **EPROM technology, 100% programmable**
- **Slim, 300 mil, 24 pin plastic or hermetic DIP**
- **5V ± 10% V<sub>CC</sub>, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 2000V static discharge**

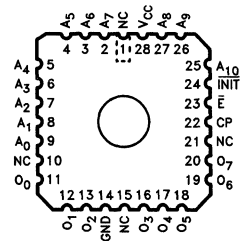
## Logic Block Diagram



## Pin Configurations



0121-2



0121-3

## Selection Guide

|                                |     | 7C245A-15  | 7C245A-18 | 7C245A-25 | 7C245A-35 |
|--------------------------------|-----|------------|-----------|-----------|-----------|
| Maximum Setup Time (ns)        |     | 15         | 18        | 25        | 35        |
| Maximum Clock to Output (ns)   |     | 10         | 12        | 15        | 20        |
| Maximum Operating Current (mA) | STD | Commercial | 120       | 120       | 90        |
|                                |     | Military   |           | 120       | 120       |
|                                | L   | Commercial |           |           | 60        |

## Product Characteristics

The CY7C245A is a high performance 2048 word by 8 bit electrically Programmable Read Only Memory packaged in a slim 300 mil plastic or hermetic DIP. The ceramic package may be equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C245A replaces bipolar devices and offers the advantages of lower power, reprogrammability, superior performance and high programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

The CY7C245A has an asynchronous initialize function (INIT). This function acts as a 2049th 8-bit word loaded into the on-chip register. It is user programmable with any desired word or may be used as a PRESET or CLEAR function on the outputs.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|  |                                 |
|--|---------------------------------|
| Storage Temperature                                    | ..... -65°C to +150°C           |
| Ambient Temperature with Power Applied                 | ..... -55°C to +125°C           |
| Supply Voltage to Ground Potential (Pin 24 to Pin 12)  | ..... -0.5V to +7.0V            |
| DC Voltage Applied to Outputs in High Z State          | ..... -0.5V to +7.0V            |
| DC Input Voltage                                       | ..... -3.0V to +7.0V            |
| DC Program Voltage (Pins 7, 18, 20)                    | ..... 13.0V                     |
| UV Erasure   | ..... 7258 Wsec/cm <sup>2</sup> |
| Static Discharge Voltage (Per MIL-STD-883 Method 3015) | ..... > 2001V                   |
| Latchup Current  | ..... > 200 mA                  |

**3**

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[4]</sup> | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over Operating Range<sup>[7]</sup>

| Parameters      | Description                  | Test Conditions   | 7C245A-15, 18 |                 | 7C245A-25, 35 |                 | 7C245AL-35 |                 | Units |    |
|-----------------|------------------------------|---|---------------|-----------------|---------------|-----------------|------------|-----------------|-------|----|
|                 |                              |   | Min.          | Max.            | Min.          | Max.            | Min.       | Max.            |       |    |
| V <sub>OH</sub> | Output HIGH Voltage          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | 2.4           |                 | 2.4           |                 | 2.4        |                 | V     |    |
| V <sub>OL</sub> | Output LOW Voltage           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 16 mA<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   |               | 0.4             |               | 0.4             |            | 0.4             | V     |    |
| V <sub>IH</sub> | Input HIGH Level             | Guaranteed Input Logical HIGH Voltage for All Inputs <sup>[1]</sup>                                       | 2.0           | V <sub>CC</sub> | 2.0           | V <sub>CC</sub> | 2.0        | V <sub>CC</sub> | V     |    |
| V <sub>IL</sub> | Input LOW Level              | Guaranteed Input Logical LOW Voltage for All Inputs <sup>[1]</sup>  |               | 0.8             |               | 0.8             |            | 0.8             | V     |    |
| I <sub>IX</sub> | Input Leakage Current        | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>   | -10           | +10             | -10           | +10             | -10        | +10             | μA    |    |
| V <sub>CD</sub> | Input Clamp Diode Voltage    | Note 5  | Note 5        |                 |               |                 |            |                 |       |    |
| I <sub>OZ</sub> | Output Leakage Current       | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub><br>Output Disabled <sup>[3]</sup>                                  | -40           | +40             | -40           | +40             | -40        | +40             | μA    |    |
| I <sub>OS</sub> | Output Short Circuit Current | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0V <sup>[2]</sup>  | -20           | -90             | -20           | -90             | -20        | -90             | mA    |    |
| I <sub>CC</sub> | Power Supply Current         | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub><br>V <sub>CC</sub> = Max.   | Commercial    |                 | 120           |                 | 90         |                 | 60    | mA |
|                 |                              |   | Military      |                 |               |                 | 120        |                 |       |    |

## Capacitance<sup>[6]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 8    |       |

### Notes:

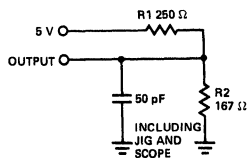
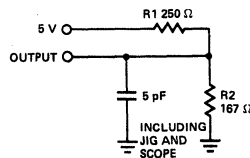
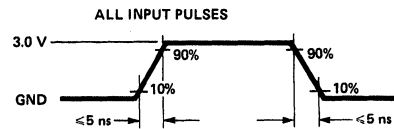
- These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
- T<sub>A</sub> is the "instant on" case temperature.
- The CMOS process does not provide a clamp diode. However, the CY7C245A is insensitive to -3V dc input levels and -5V under-shoot pulses of less than 10 ns (measured at 50% point).
- Tested initially and after any design or process changes that may affect these parameters.
- See the last page of this specification for Group A subgroup testing information.

**Switching Characteristics Over Operating Range<sup>[8]</sup>**

| Parameters                  | Description   | 7C245A-15 |      | 7C245A-18 |      | 7C245A-25 |      | 7C245A-35 |      | Units |
|-----------------------------|---|-----------|------|-----------|------|-----------|------|-----------|------|-------|
|                             |   | Min.      | Max. | Min.      | Max. | Min.      | Max. | Min.      | Max. |       |
| t <sub>SA</sub>             | Address Setup to Clock HIGH                           | 15        |      | 18        |      | 25        |      | 35        |      | ns    |
| t <sub>HA</sub>             | Address Hold from Clock HIGH                          | 0         |      | 0         |      | 0         |      | 0         |      | ns    |
| t <sub>CO</sub>             | Clock HIGH to Valid Output                            |           | 10   |           | 12   |           | 12   |           | 15   | ns    |
| t <sub>PWC</sub>            | Clock Pulse Width                                     | 10        |      | 12        |      | 15        |      | 20        |      | ns    |
| t <sub>SE<sub>S</sub></sub> | $\bar{E}_S$ Setup to Clock HIGH                       | 10        |      | 10        |      | 12        |      | 15        |      | ns    |
| t <sub>HE<sub>S</sub></sub> | $\bar{E}_S$ Hold from Clock HIGH                      | 5         |      | 5         |      | 5         |      | 5         |      | ns    |
| t <sub>DI</sub>             | Delay from INIT to Valid Output                       |           | 15   |           | 20   |           | 20   |           | 20   | ns    |
| t <sub>RI</sub>             | INIT Recovery to Clock HIGH                           | 10        |      | 15        |      | 15        |      | 20        |      | ns    |
| t <sub>PWI</sub>            | INIT Pulse Width                                      | 10        |      | 15        |      | 15        |      | 20        |      | ns    |
| t <sub>COS</sub>            | Valid Output from Clock HIGH <sup>[1]</sup>           |           | 15   |           | 15   |           | 15   |           | 20   | ns    |
| t <sub>HZC</sub>            | Inactive Output from Clock HIGH <sup>[1, 3]</sup>     |           | 15   |           | 15   |           | 15   |           | 20   | ns    |
| t <sub>DOE</sub>            | Valid Output from $\bar{E}$ LOW <sup>[2]</sup>        |           | 12   |           | 15   |           | 15   |           | 20   | ns    |
| t <sub>HZE</sub>            | Inactive Output from $\bar{E}$ HIGH <sup>[2, 3]</sup> |           | 15   |           | 15   |           | 15   |           | 20   | ns    |

**Notes:**

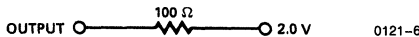
1. Applies only when the synchronous ( $\bar{E}_S$ ) function is used.
2. Applies only when the asynchronous ( $\bar{E}$ ) function is used.
3. Transition is measured at steady state High level - 500 mV or steady state Low level + 500 mV on the output from the 1.5V level on the input with loads shown in Figure 1b.
4. Tests are performed with rise and fall times of 5 ns or less.
5. See Figure 1a for all switching characteristics except t<sub>HZ</sub>.
6. See Figure 1b for t<sub>HZ</sub>.
7. All device test loads should be located within 2" of device outputs.
8. See the last page of this specification for Group A subgroup testing information.

**AC Test Loads and Waveforms<sup>[4, 5, 6, 7]</sup>**

**Figure 1a**

**Figure 1b**

**Figure 2**

0121-5

Equivalent to:

THÉVENIN EQUIVALENT



0121-6

**Functional Description**

The CY7C245A is a CMOS electrically Programmable Read Only Memory organized as 2048 words x 8-bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The CY7C245A incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with a programmable synchronous ( $\bar{E}_S$ ) or asynchronous ( $\bar{E}$ ) output enable and asynchronous initialization (INIT).

Upon power-up the state of the outputs will depend on the programmed state of the enable function ( $\bar{E}_S$  or  $\bar{E}$ ). If the synchronous enable ( $\bar{E}_S$ ) has been programmed, the register will be in the set condition causing the outputs

(O<sub>0</sub>-O<sub>7</sub>) to be in the OFF or high impedance state. If the asynchronous enable ( $\bar{E}$ ) is being used, the outputs will come up in the OFF or high impedance state only if the enable ( $\bar{E}$ ) input is at a HIGH logic level. Data is read by applying the memory location to the address inputs (A<sub>0</sub>-A<sub>10</sub>) and a logic LOW to the enable input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs (O<sub>0</sub>-O<sub>7</sub>).

If the asynchronous enable ( $\bar{E}$ ) is being used, the outputs may be disabled at any time by switching the enable to a

## Functional Description (Continued)

logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

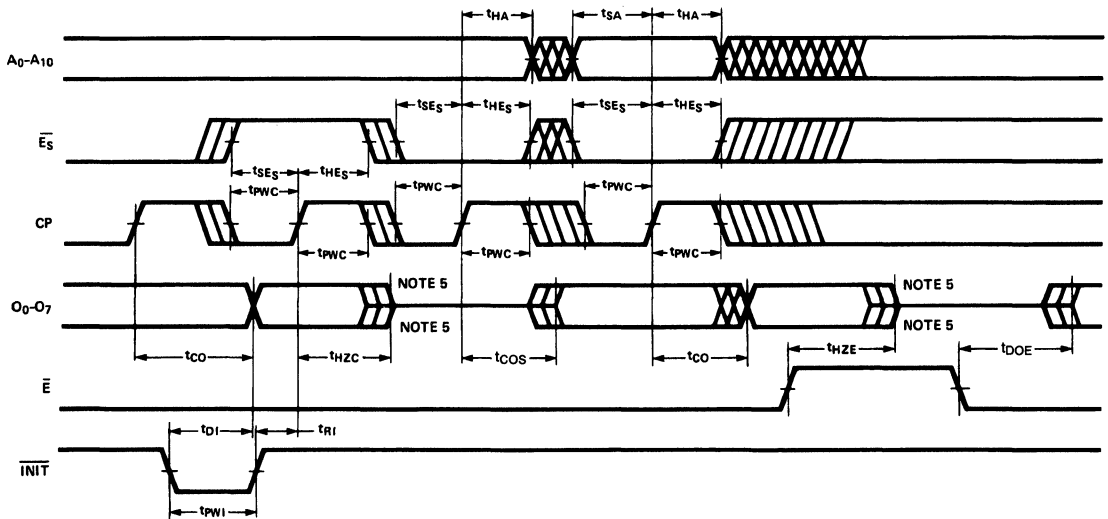
If the synchronous enable ( $\overline{E}_S$ ) is being used, the outputs will go to the OFF or high impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low to high transition of the clock. This unique feature allows the CY7C245A decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C245A has an asynchronous initialize input (INIT). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated the initialize control input causes the contents of a user programmed 2049th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of "1"s and "0"s into the register. In the unprogrammed state, activating INIT will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating INIT performs a register PRESET (all outputs HIGH).

Applying a LOW to the INIT input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ( $\overline{E}$ ) LOW.

## Switching Waveforms



0121-7

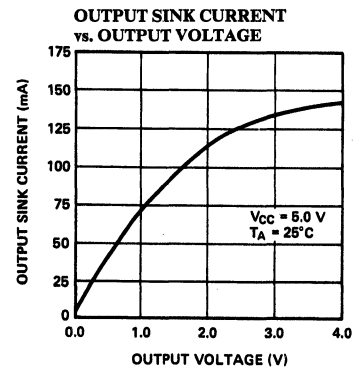
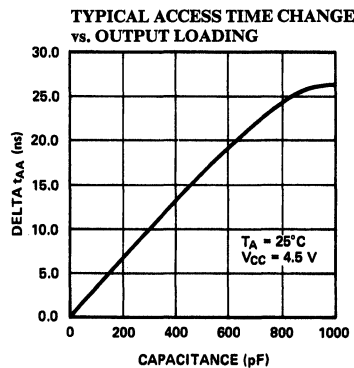
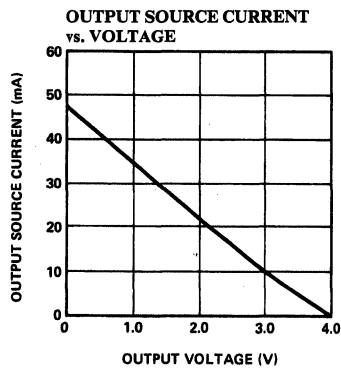
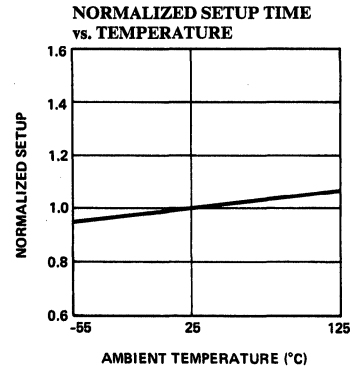
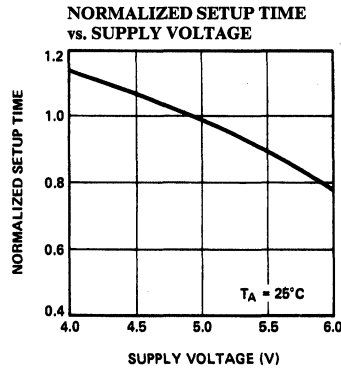
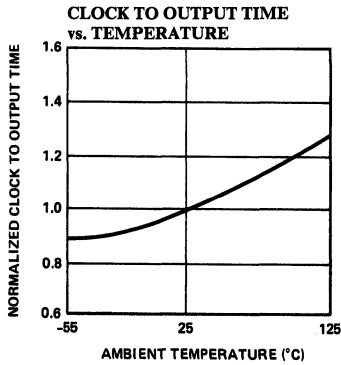
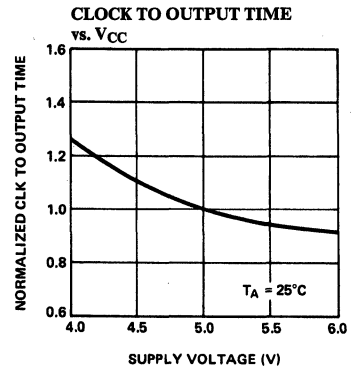
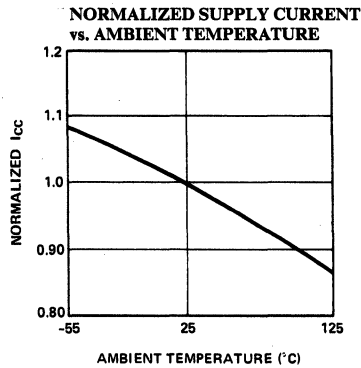
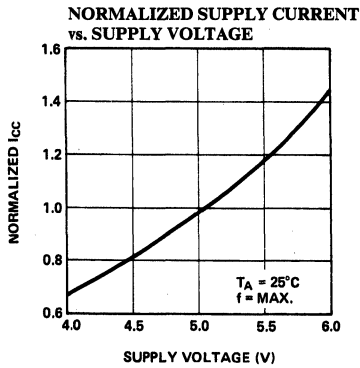
### Notes on Testing

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device  $V_{CC}$  and ground terminals. Multiple capacitors are recommended, including a 0.1  $\mu F$  or larger capacitor and a 0.01  $\mu F$  or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.

3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level  $-500$  mV or steady state LOW level  $+500$  mV on the output from the 1.5V level on inputs with load shown in Figure 1b.

Typical DC and AC Characteristics



## Erase Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C245A. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity  $\times$  exposure time) of 25 Wsec/cm<sup>2</sup>. For an ultraviolet lamp with a 12 mW/cm<sup>2</sup> power rating the exposure time would be approximately 30–35 minutes. The 7C245A needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm<sup>2</sup> is the recommended maximum dosage.

## DC Programming Parameters $T_A = 25^\circ\text{C}$

**Table 1**

| Parameter           | Description                | Min. | Max. | Units |
|---------------------|----------------------------|------|------|-------|
| V <sub>PP</sub> [1] | Programming Voltage        | 12.0 | 13.0 | V     |
| V <sub>CCP</sub>    | Supply Voltage             | 4.75 | 5.25 | V     |
| V <sub>IHP</sub>    | Input High Voltage         | 3.0  |      | V     |
| V <sub>ILP</sub>    | Input Low Voltage          |      | 0.4  | V     |
| V <sub>OH</sub> [2] | Output High Voltage        | 2.4  |      | V     |
| V <sub>OL</sub> [2] | Output Low Voltage         |      | 0.4  | V     |
| I <sub>PP</sub>     | Programming Supply Current |      | 50   | mA    |

## AC Programming Parameters $T_A = 25^\circ\text{C}$

**Table 2**

| Parameter                           | Description                        | Min. | Max.   | Units         |
|-------------------------------------|------------------------------------|------|--------|---------------|
| t <sub>PP</sub>                     | Programming Pulse Width            | 200  | 10,000 | $\mu\text{s}$ |
| t <sub>AS</sub>                     | Address Setup Time                 | 1.0  |        | $\mu\text{s}$ |
| t <sub>DS</sub>                     | Data Setup Time                    | 1.0  |        | $\mu\text{s}$ |
| t <sub>AH</sub>                     | Address Hold Time                  | 1.0  |        | $\mu\text{s}$ |
| t <sub>DH</sub>                     | Data Hold Time                     | 1.0  |        | $\mu\text{s}$ |
| t <sub>R</sub> , t <sub>F</sub> [3] | V <sub>PP</sub> Rise and Fall Time | 1.0  |        | $\mu\text{s}$ |
| t <sub>VD</sub>                     | Delay to Verify                    | 1.0  |        | $\mu\text{s}$ |
| t <sub>VP</sub>                     | Verify Pulse Width                 | 2.0  |        | $\mu\text{s}$ |
| t <sub>DV</sub>                     | Verify Data Valid                  |      | 1.0    | $\mu\text{s}$ |
| t <sub>DZ</sub>                     | Verify HIGH to High Z              |      | 1.0    | $\mu\text{s}$ |

**Notes:**

1. V<sub>CCP</sub> must be applied prior to V<sub>PP</sub>.
2. During verify operation.
3. Measured 10% and 90% points.

## Device Programming

### OVERVIEW:

There are three independent programmable functions contained in the 7C245A CMOS 2K x 8 Registered PROM; the 2K x 8 array, the initial byte, and the synchronous enable bit. All of the programming elements are "EPROM" cells, and are in an erased state when the device is shipped. This erased state manifests itself differently in each case. The erased state for ENABLE bit is the "ASYNCHRONOUS ENABLE" mode. The erased state for the "INITIAL BYTE" is all "0's" or "LOW". The "INITIAL BYTE" may be accessed operationally thru the use of the initialize function.



## Mode Selection

**Table 3**

| Mode                                | Pin Function <sup>[1]</sup> |                  |                  |                               |                   |                | Outputs<br>(9–11, 13–17) |
|-------------------------------------|-----------------------------|------------------|------------------|-------------------------------|-------------------|----------------|--------------------------|
|                                     | Read or Output Disable      | A <sub>3</sub>   | CP               | $\overline{E}/\overline{E}_S$ | $\overline{INIT}$ | A <sub>0</sub> |                          |
|                                     | Other                       | A <sub>3</sub>   | $\overline{PGM}$ | $\overline{VFY}$              | V <sub>PP</sub>   | A <sub>0</sub> |                          |
|                                     | Pin                         | (5)              | (18)             | (19)                          | 20                | (8)            |                          |
| Read <sup>[2,3]</sup>               | X                           | X                | V <sub>IL</sub>  | V <sub>IH</sub>               | X                 | Data Out       |                          |
| Output Disable <sup>[5]</sup>       | X                           | X                | V <sub>IH</sub>  | V <sub>IH</sub>               | X                 | High Z         |                          |
| Program <sup>[4]</sup>              | X                           | V <sub>ILP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>               | X                 | Data In        |                          |
| Program Verify <sup>[4]</sup>       | X                           | V <sub>IHP</sub> | V <sub>ILP</sub> | V <sub>PP</sub>               | X                 | Data Out       |                          |
| Program Inhibit <sup>[4]</sup>      | X                           | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>               | X                 | High Z         |                          |
| Intelligent Program <sup>[4]</sup>  | X                           | V <sub>ILP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>               | X                 | Data In        |                          |
| Program Synch Enable <sup>[4]</sup> | V <sub>IHP</sub>            | V <sub>ILP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>               | V <sub>PP</sub>   | High Z         |                          |
| Program Initial Byte <sup>[4]</sup> | V <sub>ILP</sub>            | V <sub>ILP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>               | V <sub>PP</sub>   | Data In        |                          |

**Notes:**

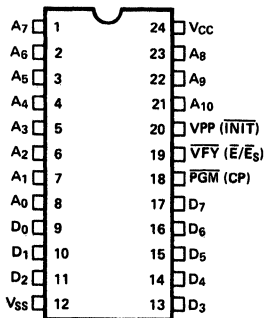
- X = Don't care but not to exceed V<sub>pp</sub>.
- During read operation, the output latches are loaded on a "0" to "1" transition of CP.
- If the registered device is being operated in a synchronous mode, pin 19 must be LOW prior to the "0" to "1" transition on CP (18) that loads the register.
- During programming and verification, all unspecified pins to be at V<sub>ILP</sub>.
- If the registered device is being operated in a synchronous mode, pin 19 must be HIGH prior to the "0" to "1" transition on CP (18) that loads the register.

The CY7C245A programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4*.

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the PGM pulse (t<sub>pp</sub>) is 0.2 msec which will then be followed by a longer overprogram pulse of 4 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.2 msec pulses applied before verification occurs. Up to ten 0.2 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V<sub>CCP</sub> = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V<sub>CC</sub> = 5.0V.



0121-10

**Figure 3. Programming Pinouts**

## Bit Map Data

| Programmer Address |     | RAM Data     |
|--------------------|-----|--------------|
| Decimal            | Hex | Contents     |
| 0                  | 0   | DATA         |
| •                  | •   | •            |
| •                  | •   | •            |
| •                  | •   | •            |
| 2047               | 7FF | DATA         |
| 2048               | 800 | INIT BYTE    |
| 2049               | 801 | CONTROL BYTE |

**Control Byte**

- 00 Asynchronous output enable (default state)
- 01 Synchronous output enable

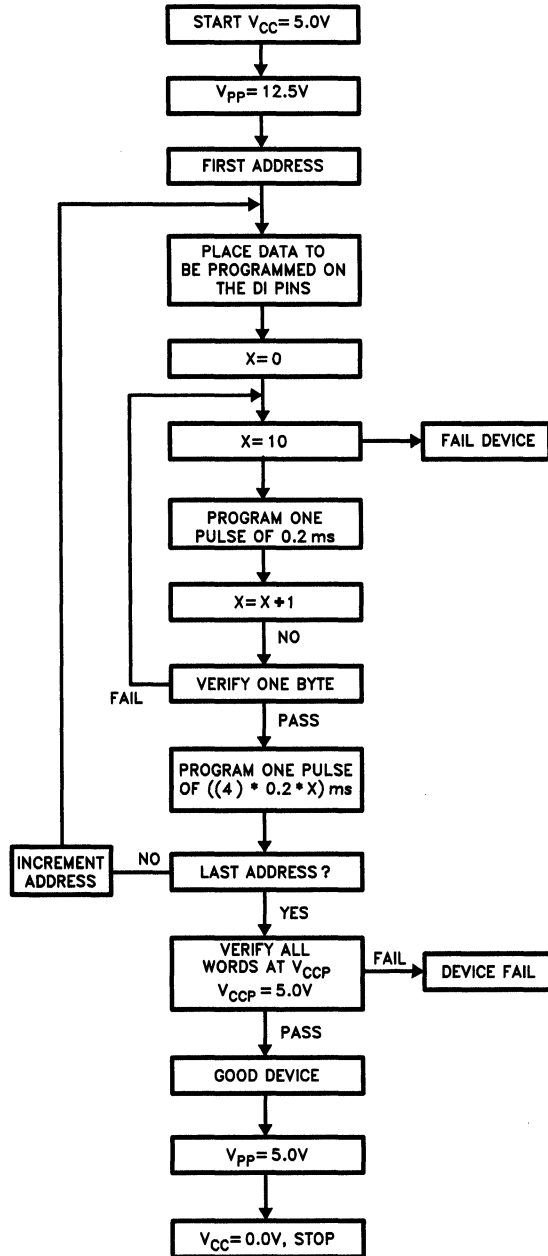


Figure 4. Programming Flowchart

0121-8

## Programming Sequence 2K x 8 Array

Power the device for normal read mode operation with pin 18, 19 and 20 at  $V_{IH}$ . Per *Figure 5* take pin 20 to  $V_{pp}$ . The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see *Figures 5* and *6*. Again per *Figure 5* address program and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each

location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be  $200 \mu\text{s}$ . Each location is ultimately programmed and verified until it verifies correctly up to and including 10 times. When the location verifies, one additional programming pulse should be applied of duration 4X the sum of the previous programming pulses before advancing to the next address to repeat the process.

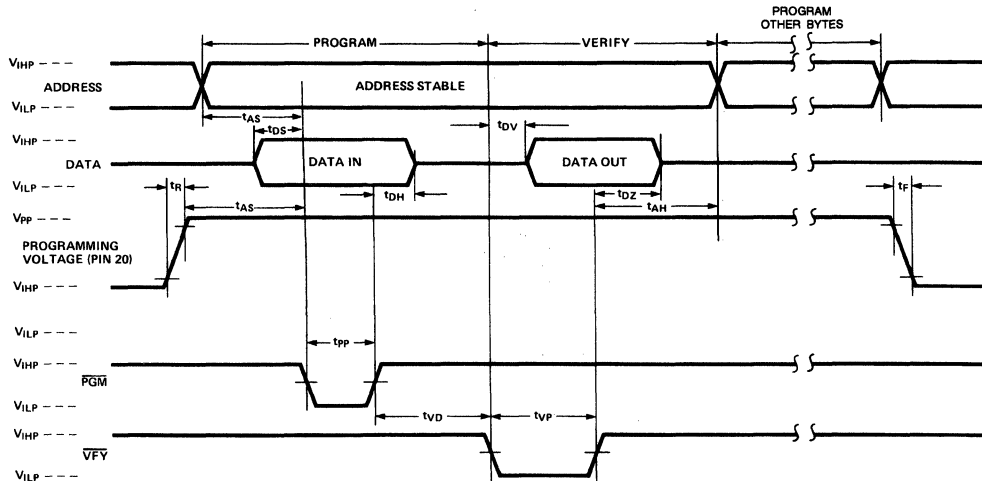


Figure 5. PROM Programming Waveforms

0121-11

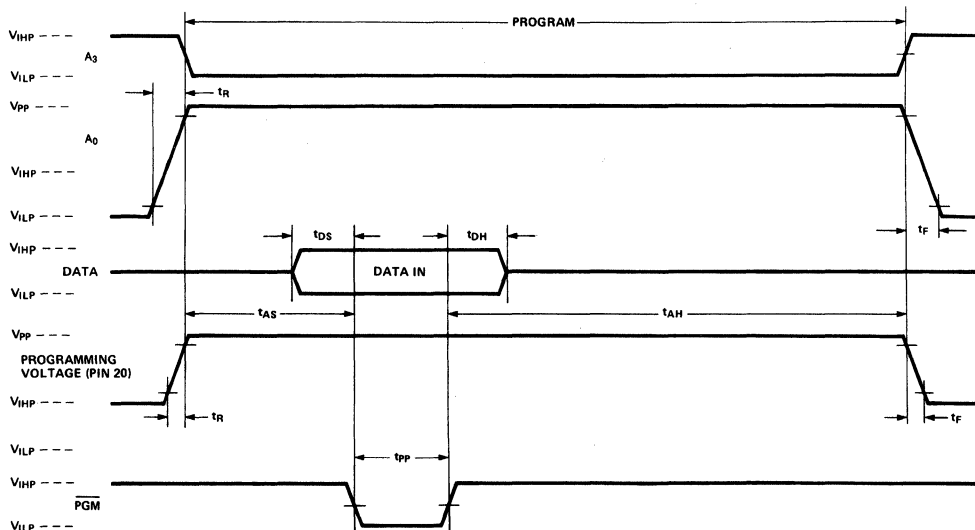


Figure 6. Initial Byte Programming Waveforms

0121-12

## Programming the Initialization Byte

The CY7C245A registered PROM has a 2049th byte of data used to initialize the value of the register. This initial byte is value "0" when the part is received. If the user desires to have a value other than "0" for register initialization, this must be programmed into the 2049th byte. This byte is programmed in a similar manner to the 2048 normal bytes in the array except for two considerations. First, since all of the normal addresses of the part are used up, a super voltage will be used to create additional effective addresses. The actual address has  $V_{PP}$  on  $A_0$  pin 8, and  $V_{ILP}$  on  $A_3$ , pin 5, per Table 3. The programming and verification of "INITIAL BYTE" is accomplished operationally by performing an initialize function.

## Programming Synchronous Enable

The CY7C245A provides for both a synchronous and asynchronous enable function. The device is delivered in an asynchronous mode of operation and only requires that the user alter the device if synchronous operation is required. The determination of the option is accomplished thru the use of an EPROM cell which is programmed only if synchronous operation is required. As with the INITIAL byte, this function is addressed thru the use of a supervoltage. Per Table 3,  $V_{PP}$  is applied to pin 8 ( $A_0$ ) with pin 5 ( $A_3$ ) at  $V_{IHP}$ . This addresses the cell that programs synchronous enable. Programming the cell is accomplished with a 10 ms program pulse on pin 18 (PGM) but does not require any data as there is no choice as to how synchronous enable may be programmed, only if it is to be programmed.

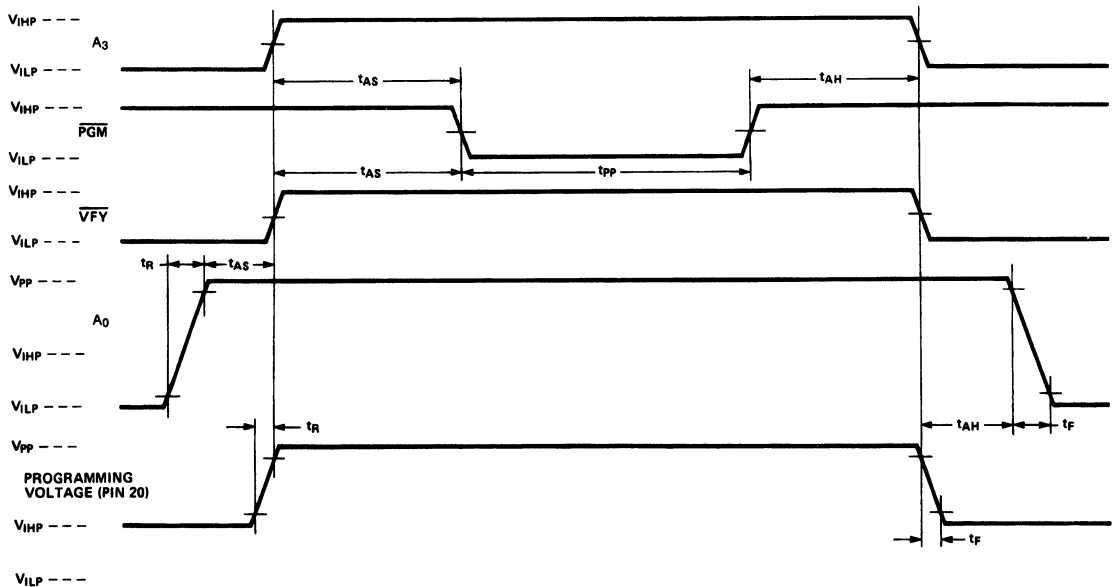


Figure 7. Program Synchronous Enable

0121-13

## Verification of Synchronous Enable

Verification of the synchronous enable function is accomplished operationally. Power the device for read operation with pin 20 at  $V_{IH}$ , cause clock pin 18 to transition from  $V_{IL}$  to  $V_{IH}$ . The output should be in a High Z state. Take pin 20,  $\overline{ENABLE}$ , to  $V_{IL}$ . The outputs should remain in a high Z state. Transition the clock from  $V_{IL}$  to  $V_{IH}$ , the outputs should now contain the data that is present. Again set pin 19 to  $V_{IH}$ . The output should remain driven. Clocking pin 18 once more from  $V_{IL}$  to  $V_{IH}$  should place the outputs again in a High Z state.

## Blank Check

A virgin device contains all zeros. To blank check this PROM, use the verify mode to read locations 0 thru 2047. A device is considered virgin if all locations are "0's" when addressed.

**Ordering Information**

| Speed (ns)      |                 | I <sub>CC</sub><br>mA | Ordering<br>Code | Package<br>Type | Operating<br>Range |
|-----------------|-----------------|-----------------------|------------------|-----------------|--------------------|
| t <sub>SA</sub> | t <sub>CO</sub> |                       |                  |                 |                    |
| 15              | 10              | 120                   | CY7C245A-15PC    | P13             | Commercial         |
|                 |                 |                       | CY7C245A-15WC    | W14             |                    |
| 18              | 12              | 120                   | CY7C245A-18PC    | P13             | Commercial         |
|                 |                 |                       | CY7C245A-18WC    | W14             |                    |
| 25              | 15              | 90                    | CY7C245A-25PC    | P13             | Commercial         |
|                 |                 |                       | CY7C245A-25SC    | S13             |                    |
|                 |                 |                       | CY7C245A-25WC    | W14             |                    |
|                 |                 |                       | CY7C245A-25LC    | L64             |                    |
|                 |                 | 120                   | CY7C245A-25DMB   | D14             | Military           |
|                 |                 |                       | CY7C245A-25QMB   | Q64             |                    |
|                 |                 |                       | CY7C245A-25WMB   | W14             |                    |
|                 |                 |                       | CY7C245A-25LMB   | L64             |                    |

| Speed (ns)      |                 | I <sub>CC</sub><br>mA | Ordering<br>Code | Package<br>Type | Operating<br>Range |          |
|-----------------|-----------------|-----------------------|------------------|-----------------|--------------------|----------|
| t <sub>SA</sub> | t <sub>CO</sub> |                       |                  |                 |                    |          |
| 35              | 20              | 60                    | CY7C245AL-35PC   | P13             | Commercial         |          |
|                 |                 |                       | CY7C245AL-35WC   | W14             |                    |          |
|                 |                 | 90                    | CY7C245A-35PC    | P13             |                    |          |
|                 |                 |                       | CY7C245A-35SC    | S13             |                    |          |
|                 |                 |                       | CY7C245A-35WC    | W14             |                    |          |
|                 |                 | 120                   | CY7C245A-35LC    | L64             |                    |          |
|                 |                 |                       | CY7C245A-35WMB   | W14             |                    | Military |
|                 |                 |                       | CY7C245A-35LMB   | L64             |                    |          |
|                 |                 |                       | CY7C245A-35DMB   | D14             |                    |          |
|                 |                 |                       | CY7C245A-35QMB   | Q64             |                    |          |

**MILITARY SPECIFICATIONS****Group A Subgroup Testing****DC Characteristics**

| Parameters      | Subgroups |
|-----------------|-----------|
| V <sub>OH</sub> | 1,2,3     |
| V <sub>OL</sub> | 1,2,3     |
| V <sub>IH</sub> | 1,2,3     |
| V <sub>IL</sub> | 1,2,3     |
| I <sub>X</sub>  | 1,2,3     |
| I <sub>OZ</sub> | 1,2,3     |
| I <sub>CC</sub> | 1,2,3     |

3

**Switching Characteristics**

| Parameters      | Subgroups   |
|-----------------|-------------|
| t <sub>SA</sub> | 7,8,9,10,11 |
| t <sub>HA</sub> | 7,8,9,10,11 |
| t <sub>CO</sub> | 7,8,9,10,11 |

Document #: 38-00004-B



# 16,384 x 8 PROM Power Switched and Reprogrammable

## Features

- CMOS for optimum speed/power
- Windowed for reprogrammability
- High speed
  - 45 ns (commercial)
  - 55 ns (military)
- Low power
  - 550 mW (commercial)
  - 660 mW (military)
- Super low standby power (7C251)
  - Less than 165 mW when deselected
  - Fast access: 50 ns
- EPROM technology 100% programmable
- Slim 300 mil or standard 600 mil packaging available
- 5V ± 10% V<sub>CC</sub>, commercial and military
- TTL compatible I/O

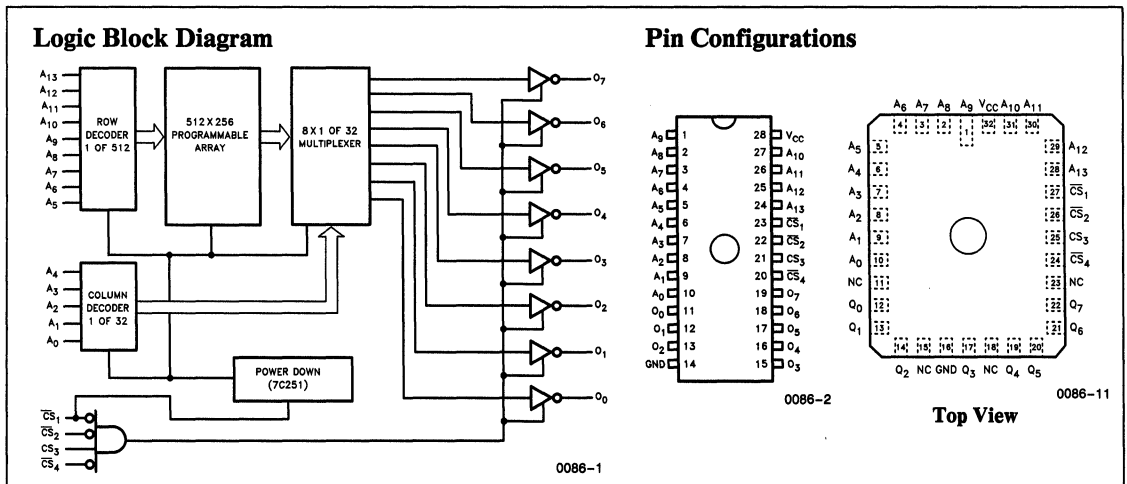
- Direct replacement for bipolar PROMs
- Capable of withstanding > 2001V static discharge

## Product Characteristics

The CY7C251 and CY7C254 are high performance 16,384 word by 8 bit CMOS PROMs. When deselected, the 7C251 automatically powers down into a low power stand-by mode. It is packaged in the 300 mil wide package. The 7C254 is packaged in 600 mil wide packages and does not power down when deselected. The 7C251 and 7C254 reprogrammable Cerdip packages are equipped with an erasure window; when exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C251 and CY7C254 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading is accomplished by placing all four chip selects in their active states. The contents of the memory location addressed by the address lines (A<sub>0</sub>–A<sub>13</sub>) will become available on the output lines (O<sub>0</sub>–O<sub>7</sub>).



## Selection Guide

|                                      |            | 7C251-45<br>7C254-45 | 7C251-55<br>7C254-55 | 7C251-65<br>7C254-65 |
|--------------------------------------|------------|----------------------|----------------------|----------------------|
| Maximum Access Time (ns)             |            | 45                   | 55                   | 65                   |
| Maximum Operating Current (mA)       | Commercial | 100                  | 100                  | 100                  |
|                                      | Military   |                      | 120                  | 120                  |
| Standby Current (mA)<br>(7C251 only) | Commercial | 30                   | 30                   | 30                   |
|                                      | Military   |                      | 35                   | 35                   |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature .....                                   | -65°C to +150°C |
| Ambient Temperature with Power Applied .....                | -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State .....         | -0.5V to +7.0V  |
| DC Input Voltage .....                                      | -3.0V to +7.0V  |
| DC Program Voltage (Pin 22) .....                           | 13.5V           |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | > 2001V (per MIL-STD-883, Method 3015) |
| Latchup Current .....          | > 200 mA                               |
| UV Exposure .....              | 7258 Wsec/cm <sup>2</sup>              |

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ±10%         |
| Military <sup>[5]</sup> | -55°C to +125°C     | 5V ±10%         |

3

## Electrical Characteristics Over the Operating Range<sup>[6]</sup>

| Parameters      | Description                                 | Test Conditions  | 7C251-45<br>7C254-45 |      | 7C251-55,65<br>7C254-55,65 |      | Units |
|-----------------|---|--|----------------------|------|----------------------------|------|-------|
|                 |   |  | Min.                 | Max. | Min.                       | Max. |       |
| V <sub>OH</sub> | Output HIGH Voltage                         | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA                                    | 2.4                  |      | 2.4                        |      | V     |
| V <sub>OL</sub> | Output LOW Voltage                          | V <sub>CC</sub> = Min., I <sub>OL</sub> = 16.0 mA                                    |                      | 0.5  |                            | 0.5  | V     |
| V <sub>IH</sub> | Input HIGH Level <sup>[1]</sup>             |  | 2.0                  |      | 2.0                        |      | V     |
| V <sub>IL</sub> | Input LOW Level <sup>[1]</sup>              |  |                      | 0.8  |                            | 0.8  | V     |
| I <sub>IX</sub> | Input Current                               | GND ≥ V <sub>IN</sub> ≤ V <sub>CC</sub>  | -10                  | +10  | -10                        | +10  | μA    |
| V <sub>CD</sub> | Input Diode Clamp Voltage                   |  | Note 2               |      | Note 2                     |      |       |
| I <sub>OZ</sub> | Output Leakage Current                      | V <sub>OL</sub> ≤ V <sub>OUT</sub> ≤ V <sub>OH</sub> , Output Disabled               | -40                  | +40  | -40                        | +40  | μA    |
| I <sub>OS</sub> | Output Short Circuit Current <sup>[3]</sup> | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND                                       | -20                  | -90  | -20                        | -90  | mA    |
| I <sub>CC</sub> | Power Supply Current                        | V <sub>CC</sub> = Max., V <sub>IN</sub> = 2.0V<br>I <sub>OUT</sub> = 0 mA            | Commercial           | 100  | 100                        |      | mA    |
|                 |   |  | Military             |      |                            | 120  | mA    |
| I <sub>SB</sub> | Standby Supply Current (7C251)              | V <sub>CC</sub> = Max., $\overline{CS}$ ≥ V <sub>IH</sub><br>I <sub>OUT</sub> = 0 mA | Commercial           | 30   | 30                         |      | mA    |
|                 |   |  | Military             |      |                            | 35   | mA    |

## Capacitance<sup>[4]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 10   | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 10   |       |

### Notes:

- These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
- The CMOS process does not provide a clamp diode. However, the CY7C251 and CY7C254 are insensitive to -3V dc input levels and -5V undershoot pulses of less than 10 ns (measured at 50% point).
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.



## Switching Characteristics Over the Operating Range<sup>[6, 7]</sup>

| Parameters                    | Description   | 7C251-45<br>7C254-45 |      | 7C251-55<br>7C254-55 |      | 7C251-65<br>7C254-65 |      | Units |
|-------------------------------|---|----------------------|------|----------------------|------|----------------------|------|-------|
|                               |   | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. |       |
| t <sub>AA</sub>               | Address to Output Valid   |                      | 45   |                      | 55   |                      | 65   | ns    |
| t <sub>HZCS<sub>1</sub></sub> | Chip Select Inactive to High Z <sup>[8, 9]</sup>                              |                      | 25   |                      | 30   |                      | 35   | ns    |
| t <sub>HZCS<sub>2</sub></sub> | Chip Select Inactive to High Z (7C251, $\overline{CS}_1$ Only) <sup>[8]</sup> |                      | 50   |                      | 60   |                      | 70   | ns    |
| t <sub>ACS<sub>1</sub></sub>  | Chip Select Active to Output Valid <sup>[9]</sup>                             |                      | 25   |                      | 30   |                      | 35   | ns    |
| t <sub>ACS<sub>2</sub></sub>  | Chip Select Active to Output Valid (7C251, $\overline{CS}_1$ Only)            |                      | 50   |                      | 60   |                      | 70   | ns    |
| t <sub>PU</sub>               | Chip Select Active to Power Up (7C251)  | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>PD</sub>               | Chip Select Inactive to Power Down (7C251)                                    |                      | 50   |                      | 60   |                      | 70   | ns    |

## AC Test Loads and Waveforms

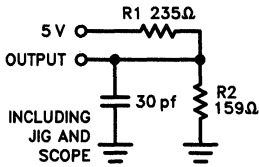


Figure 1a

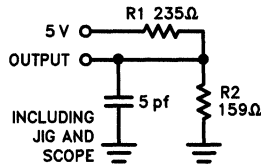


Figure 1b

0086-4

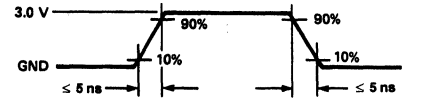
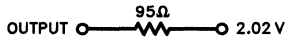


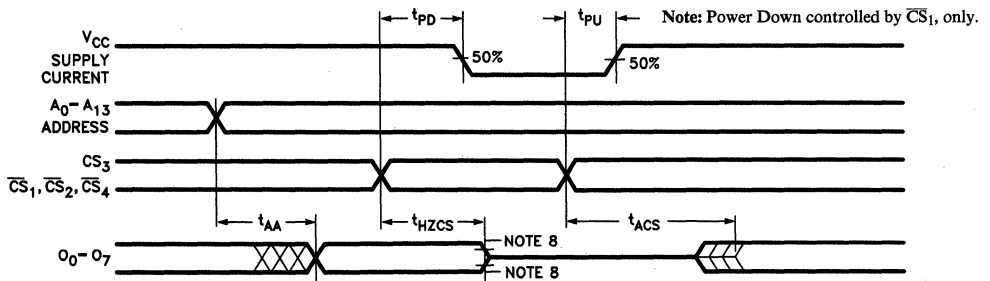
Figure 2. Input Pulses

0086-6

Equivalent to: THÉVENIN EQUIVALENT



0086-5



0086-7

### Notes:

7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and loads shown in Figure 1a, 1b.

8. t<sub>HZCS</sub> is tested with load shown in Figure 1b. Transition is measured at steady state High level - 300 mV or steady state Low level + 500 mV on the output from the 1.5V level on the input.

9. t<sub>HZCS<sub>1</sub></sub> and t<sub>ACS<sub>1</sub></sub> refers to 7C254 (all chip selects); and 7C251 ( $\overline{CS}_2$ ,  $\overline{CS}_3$  and  $\overline{CS}_4$  only).

## Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C251 and 7C254 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV

intensity × exposure time) or 25 Wsec/cm<sup>2</sup>. For an ultraviolet lamp with a 12 mW/cm<sup>2</sup> power rating the exposure time would be approximately 45 minutes. The 7C251 or 7C254 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258W × sec/cm<sup>2</sup> is the recommended maximum dosage.

## Device Programming

The CY7C251 and CY7C254 all program identically. They utilize an intelligent programming algorithm to assure consistent programming quality. These 128K PROMS use a single ended memory cell design. In an unprogrammed state, the memory contains all "0"s. During programming, a "1" on a data-in pin causes the addressed location to be programmed, and a "0" causes the location to remain unprogrammed.

## Programming Pinout

The Programming Pinout of all three devices are shown in Figure 3 below, and are identical. The programming mode is entered by raising the pin 22 to  $V_{PP}$ . The addressed location is programmed and verified with the application of a  $\overline{PGM}$  and  $\overline{VFY}$  pulse applied to pins 23 and 21 respectively. Entering and exiting the programming mode should be done with care. Proper sequencing as described in the dialog on the programming algorithm and shown in the timing diagram and programming flow chart must be implemented.

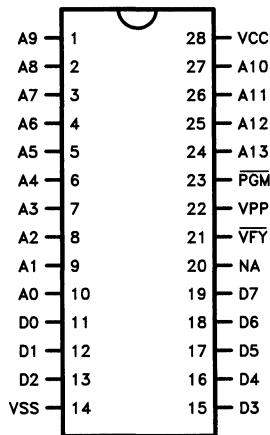
## Programming And Blankcheck

### Blankcheck

Blankcheck is accomplished by performing a verify cycle ( $\overline{VFY}$  toggles on each address), sequencing through all memory address locations, where all the data read will be "0"s.

## Programming Algorithm

Programming is accomplished with an intelligent algorithm. The sequence of operations is to enter the programming mode by placing  $V_{PP}$  on pin 22. This should be done after a minimum delay from power up, and be removed prior to power down by the same delay (see the timing diagram and AC specifications for details). Once in this mode, programming is accomplished by addressing a location, placing the data to be programmed into a location on the data pins, and clocking the  $\overline{PGM}$  signal from  $V_{IHP}$  to  $V_{ILP}$  and back to  $V_{IHP}$  with a pulse width of 200  $\mu$ s. The data is removed from the data pins and the content of the location is then verified by taking the  $\overline{VFY}$  signal from  $V_{IHP}$  to  $V_{ILP}$ , comparing the output with the desired data and then returning  $\overline{VFY}$  to  $V_{IHP}$ . If the contents are correct, a second overprogram pulse of 4 times the original 200  $\mu$ s is delivered with the data to be programmed again on the data pins. If the data is not correct, a second 200  $\mu$ s pulse is applied to  $\overline{PGM}$  with the data to be programmed on the data pins. The compare and overprogram operation is repeated with an overprogram pulse width 4 times the sum of the initial program pulses. This operation is continued until the location is programmed or 10 initial program pulses have been attempted. If on the 10th attempt, the location fails to verify, an overprogram pulse of 8 ms is applied, and the content of the location is once more verified. If the location still fails to verify, the device is rejected. Once a location verifies successfully, the address is advanced to the next location, and the process is repeated until all locations are programmed. After all locations are programmed, they should be verified at  $V_{CCP} = 5.0V$ .



0086-8

Figure 3. Programming Pinout (DIP Package)

## Operating Modes

### Read

Read is the normal operating mode for a programmed device. In this mode, all signals are normal TTL levels. The PROM is addressed with a 14 bit field, 4 chip select bits, and the contents of the addressed location appear on the data out pins.

### Program, Program Inhibit, Program Verify

These modes are entered by placing a high voltage  $V_{PP}$  on pin 22. Pin 23 becomes an active LOW program (PGM) signal and pin 21 becomes an active LOW verify (VFY) signal. Pins 21 and 23 should never be active LOW at the same time. The PROGRAM mode exists when PGM is LOW, and VFY is HIGH. The VERIFY mode exists when the reverse is true, PGM HIGH and VFY LOW and the PROGRAM INHIBIT mode is entered with both PGM and VFY HIGH. PROGRAM INHIBIT is specifically provided to allow data to be placed on and removed from the data pins without conflict.

### Blankcheck

Blankcheck mode is identical to PROGRAM VERIFY and is entered in the same manner as described above.

## Programming Sequence

The flowchart in Figure 4 is a detailed description of the intelligent programming cycle used to program the devices covered in this specification. Of particular importance are the areas of power sequencing used to enter and exit the programming operation. This flowchart combined with the timing diagrams AC and DC parameters accurately describe this complete operation.

The timing diagram in Figure 5 contains all of the timing information necessary for describing the relations required for programming the devices covered in this specification. Some of the information pertains to each cycle of programming as specified in Figure 4, and some pertains only to entry and exit from the programming mode of operation.

$T_P$ ,  $T_{PD}$  and  $T_{HP}$  refer to the entry and exit from the programming mode of operation. Note that this is referenced to PGM and VFY operations.

$T_{DS}$ ,  $T_{AS}$ ,  $T_{AH}$  and  $T_{DH}$  refer to the required setup and hold times for the address and data for PGM and VFY operations. These parameters must be adhered to, in all operations, including VFY. This precludes the option then of verifying the device by holding the VFY signal LOW, and sequencing the addresses.

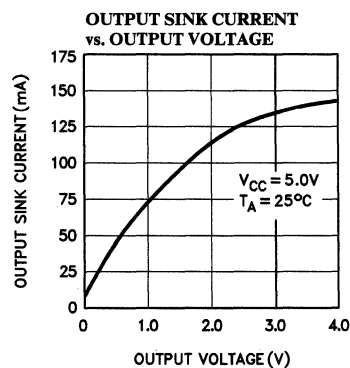
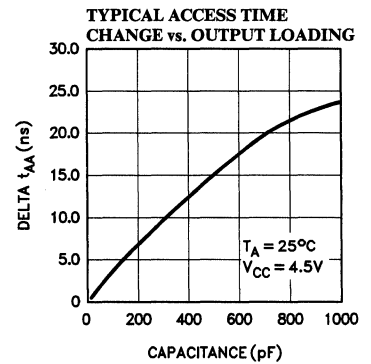
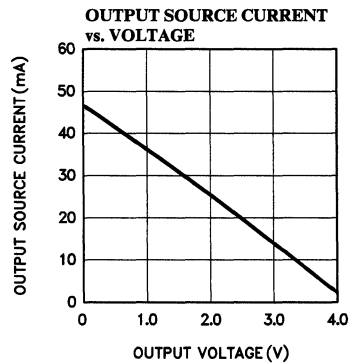
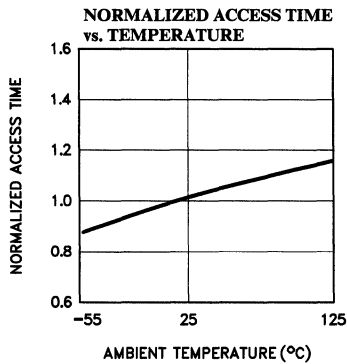
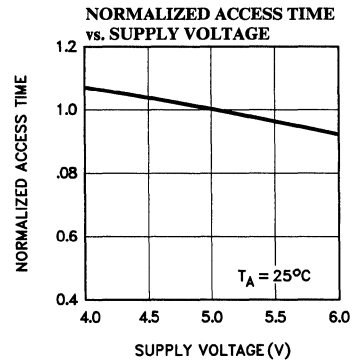
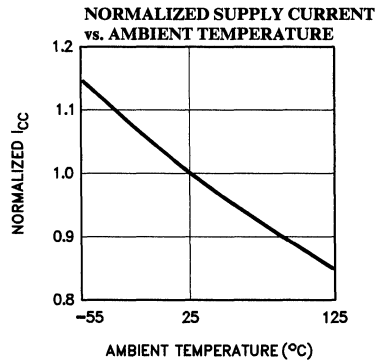
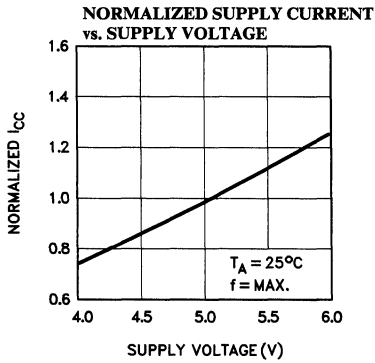
Table 1. Operating Modes

| Mode                          | Pin Function           |                   |           |                   |           | Outputs<br>(11-13, 15-19) |
|-------------------------------|------------------------|-------------------|-----------|-------------------|-----------|---------------------------|
|                               | Read or Output Disable | $\overline{CS}_4$ | $CS_3$    | $\overline{CS}_2$ | $CS_1$    |                           |
|                               | Other                  | N/A               | VFY       | $V_{PP}$          | PGM       |                           |
|                               | Pin Number             | (20)              | (21)      | (22)              | (23)      |                           |
| Read                          |                        | $V_{IL}$          | $V_{IH}$  | $V_{IL}$          | $V_{IL}$  | Data Out                  |
| Output Disable <sup>[1]</sup> |                        | X                 | X         | X                 | $V_{IH}$  | High Z                    |
| Output Disable <sup>[1]</sup> |                        | X                 | X         | $V_{IH}$          | X         | High Z                    |
| Output Disable <sup>[1]</sup> |                        | X                 | $V_{IL}$  | X                 | X         | High Z                    |
| Output Disable <sup>[1]</sup> |                        | $V_{IH}$          | X         | X                 | X         | High Z                    |
| Program                       |                        | X                 | $V_{IHP}$ | $V_{PP}$          | $V_{ILP}$ | Data In                   |
| Program Verify                |                        | X                 | $V_{ILP}$ | $V_{PP}$          | $V_{IHP}$ | Data Out                  |
| Program Inhibit               |                        | X                 | $V_{IHP}$ | $V_{PP}$          | $V_{IHP}$ | High Z                    |
| Blank Check                   |                        | X                 | $V_{ILP}$ | $V_{PP}$          | $V_{IHP}$ | Data Out                  |

Note:

1. X = Don't care but not to exceed  $V_{CC} + 5\%$ .

## Typical AC and DC Characteristics



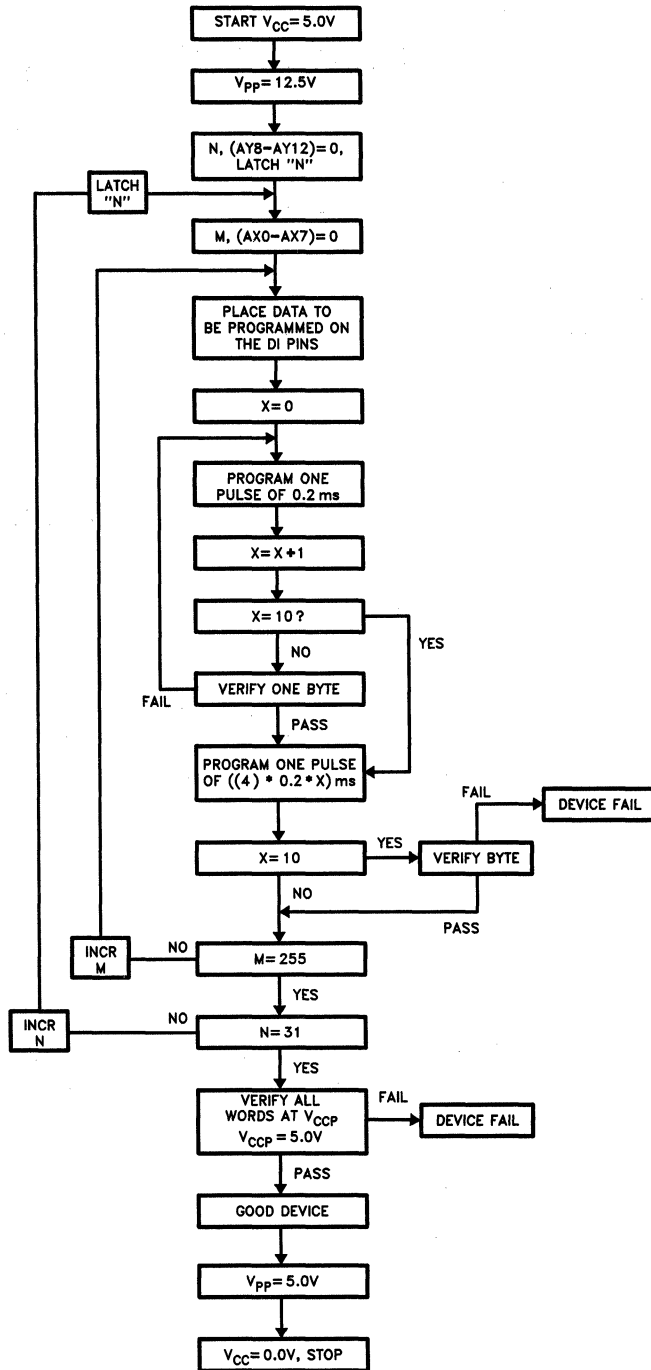
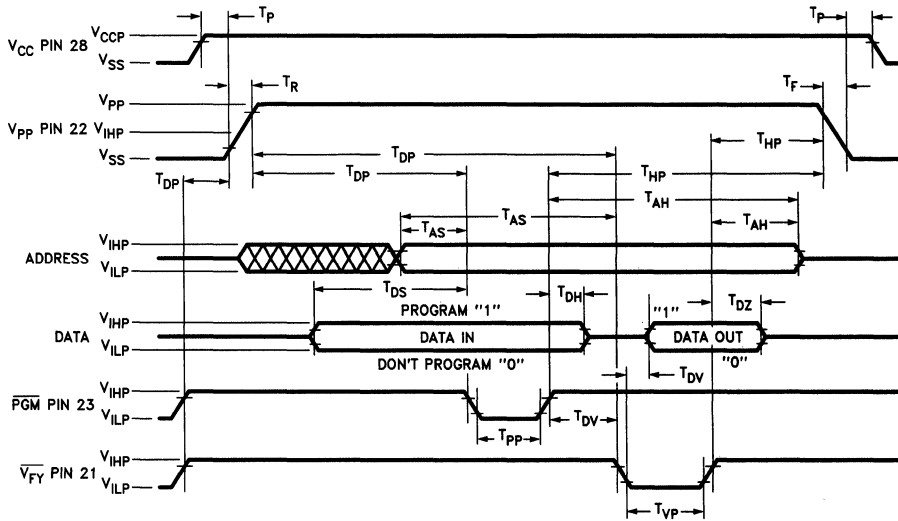


Figure 4. Programming Flowchart

0086-13



0086-14

**Figure 5. Programming Waveforms**

Note: Power,  $V_{PP}$  and  $V_{CC}$  should not be cycled for each program verify cycle but remain static during programming.

**Table 2. DC Programming Parameters  $T_A = 25^\circ\text{C}$**

| Parameter | Description                             | Min. | Max.      | Units |
|-----------|---|------|-----------|-------|
| $V_{PP}$  | Programming Voltage                     | 12.0 | 13.0      | V     |
| $V_{CCP}$ | Power Supply Voltage During Programming | 4.75 | 5.25      | V     |
| $I_{PP}$  | $V_{PP}$ Supply Current                 |      | 50        | mA    |
| $V_{IHP}$ | Input High Voltage During Programming   | 3.0  | $V_{CCP}$ | V     |
| $V_{ILP}$ | Input Low Voltage During Programming    | -3.0 | 0.4       | V     |
| $V_{OH}$  | Output High Voltage                     | 2.4  |           | V     |
| $V_{OL}$  | Output Low Voltage                      |      | 0.4       | V     |

**Table 3. AC Programming Parameters  $T_A = 25^\circ\text{C}$**

| Parameter  | Description                    | Min. | Max. | Units         |
|------------|--------------------------------|------|------|---------------|
| $t_{AS}$   | Address Setup Time to PGM/VFY  | 1.0  |      | $\mu\text{s}$ |
| $t_{AH}$   | Address Hold Time from PGM/VFY | 1.0  |      | $\mu\text{s}$ |
| $t_{DS}$   | Data Setup Time to PGM         | 1.0  |      | $\mu\text{s}$ |
| $t_{DH}$   | Data Hold Time PGM             | 1.0  |      | $\mu\text{s}$ |
| $t_{PP}$   | Program Pulse Width            | 0.2  | 10   | ms            |
| $t_{R, F}$ | $V_{PP}$ Rise and Fall Time    | 100  |      | ns            |
| $t_{DV}$   | Delay to Verify                | 1.0  |      | $\mu\text{s}$ |
| $t_{VD}$   | Verify to Data Out             |      | 1.0  | $\mu\text{s}$ |
| $t_{VH}$   | Data Hold Time from Verify     |      | 1.0  | $\mu\text{s}$ |
| $t_{VP}$   | Verify Pulse Width             | 2.0  |      | $\mu\text{s}$ |
| $t_{DZ}$   | Verify to High Z               |      | 1.0  | $\mu\text{s}$ |
| $t_{DP}$   | Delay to Function              | 1.0  |      | $\mu\text{s}$ |
| $t_{HP}$   | Hold from Function             | 1.0  |      | $\mu\text{s}$ |
| $t_p$      | Power Up/Down                  | 20.0 |      | ms            |

**Ordering Information**

| Speed (ns) | Ordering Code  | Package Type   | Operating Range                                      |
|------------|--|--|--|
| 45         | CY7C251-45PC<br>CY7C251-45WC<br>CY7C254-45WC<br>CY7C254-45PC<br>CY7C254-45DC | P21<br>W22<br>W16<br>P15<br>D16  | Commercial   |
|            | 55   | CY7C251-55PC<br>CY7C251-55WC<br>CY7C254-55WC<br>CY7C254-55PC<br>CY7C254-55DC   |  |
| 65         |  | CY7C251-55WMB<br>CY7C251-55DMB<br>CY7C254-55WMB<br>CY7C254-55DMB   | W22<br>D22<br>W16<br>D16                             |
|            | 65   | CY7C251-65PC<br>CY7C251-65WC<br>CY7C254-65WC<br>CY7C254-65PC<br>CY7C254-65DC   | P21<br>W22<br>W16<br>P15<br>D16                      |
|            |  | CY7C251-65WMB<br>CY7C251-65DMB<br>CY7C251-65LMB<br>CY7C251-65QMB<br>CY7C254-65WMB<br>CY7C254-65LMB<br>CY7C254-65QMB<br>CY7C254-65DMB | W22<br>D22<br>L55<br>Q55<br>W16<br>L55<br>Q55<br>D16 |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters                     | Subgroups |
|--------------------------------|-----------|
| V <sub>OH</sub>                | 1,2,3     |
| V <sub>OL</sub>                | 1,2,3     |
| V <sub>IH</sub>                | 1,2,3     |
| V <sub>IL</sub>                | 1,2,3     |
| I <sub>IX</sub>                | 1,2,3     |
| I <sub>OZ</sub>                | 1,2,3     |
| I <sub>CC</sub>                | 1,2,3     |
| I <sub>SB</sub> <sup>[2]</sup> | 1,2,3     |

3

#### Switching Characteristics

| Parameters                       | Subgroups   |
|----------------------------------|-------------|
| t <sub>AA</sub>                  | 7,8,9,10,11 |
| t <sub>ACS1</sub> <sup>[1]</sup> | 7,8,9,10,11 |
| t <sub>ACS2</sub> <sup>[2]</sup> | 7,8,9,10,11 |

**Notes:**

1. 7C254 and 7C251 ( $\overline{CS}_2$ , CS<sub>3</sub> and  $\overline{CS}_4$  only).
2. 7C251 ( $\overline{CS}_1$  only).

Document #: 38-00056-C





CYPRESS  
SEMICONDUCTOR

CY7C261  
CY7C263/CY7C264

## 8192 x 8 PROM Power Switched and Reprogrammable

### Features

- CMOS for optimum speed/power
- Windowed for reprogrammability
- High speed
  - 35 ns (commercial)
  - 45 ns (military)
- Low power
  - 550 mW (commercial)
  - 660 mW (military)
- Super low standby power (7C261)
  - Less than 185 mW when deselected
  - Fast access: 35 ns
- EPROM technology 100% programmable
- Slim 300 mil or standard 600 mil packaging available
- 5V  $\pm$  10% V<sub>CC</sub>, commercial and military
- TTL compatible I/O

- Direct replacement for bipolar PROMs
- Capable of withstanding > 2000V static discharge

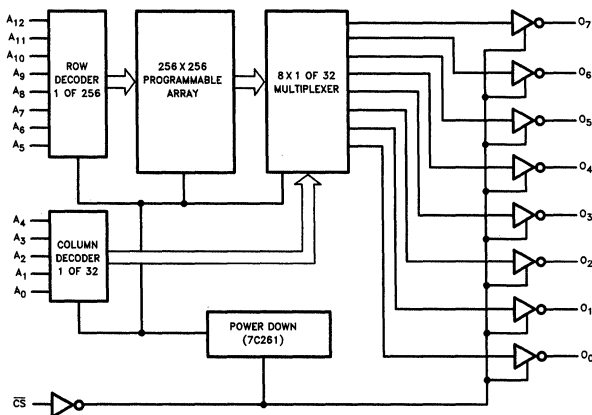
### Product Characteristics

The CY7C261, CY7C263 and CY7C264 are high performance 8192 word by 8 bit CMOS PROMs. When deselected, the 7C261 automatically powers down into a low power standby mode. It is packaged in the 300 mil wide package. The 7C263 and 7C264 are packaged in 300 mil and 600 mil wide packages respectively and do not power down when deselected. The reprogrammable CERDIP packages are equipped with an erasure window; when exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C261, CY7C263 and CY7C264 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

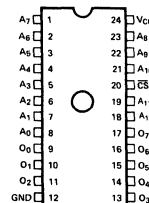
Reading is accomplished by placing an active LOW signal on CS. The contents of the memory location addressed by the address lines (A<sub>0</sub>–A<sub>12</sub>) will become available on the output lines (O<sub>0</sub>–O<sub>7</sub>).

### Logic Block Diagram

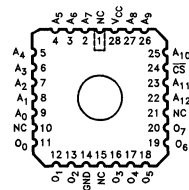


0052-1

### Pin Configurations



0052-2



0052-3

### Selection Guide

|                                      |            | 7C261-35<br>7C263-35<br>7C264-35 | 7C261-40<br>7C263-40<br>7C264-40 | 7C261-45<br>7C263-45<br>7C264-45 | 7C261-55<br>7C263-55<br>7C264-55 |
|--------------------------------------|------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| Maximum Access Time (ns)             |            | 35                               | 40                               | 45                               | 55                               |
| Maximum Operating Current (mA)       | Commercial | 100                              | 100                              | 100                              | 100                              |
|                                      | Military   |                                  |                                  | 120                              | 120                              |
| Standby Current (mA)<br>(7C261 only) | Commercial | 30                               | 30                               | 30                               | 30                               |
|                                      | Military   |                                  |                                  | 30                               | 30                               |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature                                   | -65°C to +150°C |
| Ambient Temperature with Power Applied                | -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 24 to Pin 12) | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State         | -0.5V to +7.0V  |
| DC Input Voltage                                      | -3.0V to +7.0V  |
| DC Program Voltage (Pin 19 DIP, Pin 23 LCC)           | 13.0V           |

|   |                           |
|---|---------------------------|
| Static Discharge Voltage (per MIL-STD-883, Method 3015) | > 2001V                   |
| Latchup Current   | > 200 mA                  |
| UV Exposure   | 7258 Wsec/cm <sup>2</sup> |

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[5]</sup> | -55°C to +125°C     | 5V ± 10%        |

**3**

## Electrical Characteristics Over the Operating Range<sup>[6]</sup>

| Parameters      | Description                                 | Test Conditions   | 7C261-35, 40<br>7C263-35, 40<br>7C264-35, 40 |      | 7C261-45,55<br>7C263-45,55<br>7C264-45,55 |      | Units |
|-----------------|---|---|--|------|---|------|-------|
|                 |   |   | Min.   | Max. | Min.                                      | Max. |       |
| V <sub>OH</sub> | Output HIGH Voltage                         | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA                                     | 2.4  |      | 2.4                                       |      | V     |
| V <sub>OL</sub> | Output LOW Voltage                          | V <sub>CC</sub> = Min., I <sub>OL</sub> = 16.0 mA                                     |  | 0.4  |   | 0.4  | V     |
| V <sub>IH</sub> | Input HIGH Level <sup>[1]</sup>             |   | 2.0  |      | 2.0                                       |      | V     |
| V <sub>IL</sub> | Input LOW Level <sup>[1]</sup>              |   |  | 0.8  |   | 0.8  | V     |
| I <sub>IX</sub> | Input Current                               | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>   | -10  | +10  | -10                                       | +10  | μA    |
| V <sub>CD</sub> | Input Diode Clamp Voltage                   |   | Note 2                                       |      | Note 2                                    |      |       |
| I <sub>OZ</sub> | Output Leakage Current                      | V <sub>OL</sub> ≤ V <sub>OUT</sub> ≤ V <sub>OH</sub> , Output Disabled                | -40  | +40  | -40                                       | +40  | μA    |
| I <sub>OS</sub> | Output Short Circuit Current <sup>[3]</sup> | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND  | -20  | -90  | -20                                       | -90  | mA    |
| I <sub>CC</sub> | Power Supply Current                        | V <sub>CC</sub> = Max., V <sub>IN</sub> = 2.0V<br>I <sub>OUT</sub> = 0 mA             | Commercial                                   | 100  | 100                                       |      | mA    |
|                 |   |   | Military                                     |      |   | 120  | mA    |
| I <sub>SB</sub> | Standby Supply Current (7C261)              | V <sub>CC</sub> = Max., $\overline{\text{CS}} \geq V_{IH}$<br>I <sub>OUT</sub> = 0 mA | Commercial                                   | 30   | 30  |      | mA    |
|                 |   |   | Military                                     |      |   | 30   | mA    |

## Capacitance<sup>[4]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 8    |       |

- Notes:
- These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
  - The CMOS process does not provide a clamp diode. However, the CY7C261, CY7C263 & CY7C264 are insensitive to -3V dc input levels and -5V undershoot pulses of less than 10 ns (measured at 50% point).
  - For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
  - Tested initially and after any design or process changes that may affect these parameters.
  - T<sub>A</sub> is the "instant on" case temperature.
  - See the last page of this specification for Group A subgroup testing information.

### Switching Characteristics Over the Operating Range<sup>[5, 6]</sup>

| Parameters   | Description   | 7C261-35<br>7C263-35<br>7C264-35 |                         | 7C261-40<br>7C263-40<br>7C264-40 |      | 7C261-45<br>7C263-45<br>7C264-45 |      | 7C261-55<br>7C263-55<br>7C264-55 |      | Units |
|--------------|---|----------------------------------|-------------------------|----------------------------------|------|----------------------------------|------|----------------------------------|------|-------|
|              |   | Min.                             | Max.                    | Min.                             | Max. | Min.                             | Max. | Min.                             | Max. |       |
|              |   | $t_{AA}$                         | Address to Output Valid |                                  | 35   |                                  | 40   |                                  | 45   |       |
| $t_{HZCS_1}$ | Chip Select Inactive to High Z <sup>[8]</sup>         |                                  | 25                      |                                  | 25   |                                  | 30   |                                  | 35   | ns    |
| $t_{HZCS_2}$ | Chip Select Inactive to High Z (7C261) <sup>[8]</sup> |                                  | 30                      |                                  | 35   |                                  | 45   |                                  | 55   | ns    |
| $t_{ACS1}$   | Chip Select Active to Output Valid                    |                                  | 25                      |                                  | 25   |                                  | 30   |                                  | 35   | ns    |
| $t_{ACS2}$   | Chip Select Active to Output Valid (7C261)            |                                  | 40                      |                                  | 45   |                                  | 45   |                                  | 55   | ns    |
| $t_{PU}$     | Chip Select Active to Power Up (7C261)                | 0                                |                         | 0                                |      | 0                                |      | 0                                |      | ns    |
| $t_{PD}$     | Chip Select Inactive to Power Down (7C261)            |                                  | 35                      |                                  | 40   |                                  | 45   |                                  | 55   | ns    |

### AC Test Loads and Waveforms

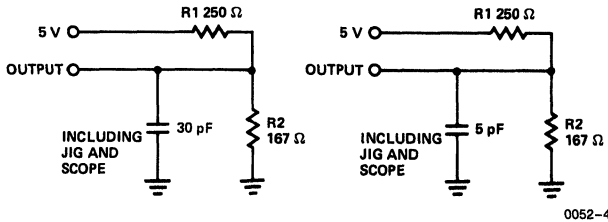


Figure 1a

Figure 1b

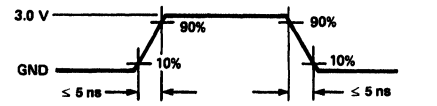
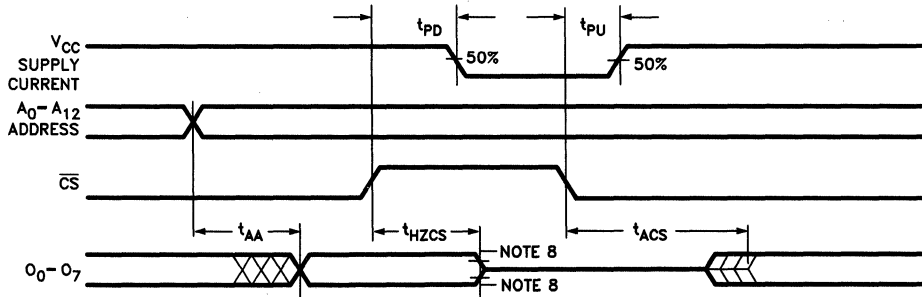
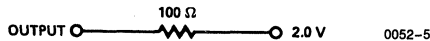


Figure 2. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



#### Notes:

7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified  $I_{OL}/I_{OH}$  and loads shown in Figure 1a, 1b.

8.  $t_{HZCS}$  is tested with load shown in Figure 1b. Transition is measured at steady state High level - 500 mV or steady state Low level + 500 mV on the output from the 1.5V level on the input.

### Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the devices in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV

intensity  $\times$  exposure time) or 25 Wsec/cm<sup>2</sup>. For an ultraviolet lamp with a 12 mW/cm<sup>2</sup> power rating the exposure time would be approximately 45 minutes. The 7C261 or 7C263 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258W  $\times$  sec/cm<sup>2</sup> is the recommended maximum dosage.

## Device Programming

The CY7C261, CY7C263 & CY7C264 all program identically. They utilize an intelligent programming algorithm to assure consistent programming quality. These 64K PROMS use a single ended memory cell design. In an unprogrammed state, the memory contains all "0"s. During programming, a "1" on a data-in pin causes the addressed location to be programmed, and a "0" causes the location to remain unprogrammed.

## Programming Pinout

The Programming Pinout of all three devices are shown in Figure 3 below, and are identical. The programming mode is entered by raising the pin 19 to  $V_{PP}$ . In this mode, pin 21 becomes a latch signal, allowing the upper 5 address bits to be latched and held in an onboard register, while the lower 8 address bits are presented on the same pins for selecting one of 256 memory bytes. The addressed location is programmed and verified with the application of a  $\overline{PGM}$  and  $\overline{VFY}$  pulse applied to pins 22 and 23 respectively. Entering and exiting the programming mode should be done with care. Proper sequencing as described in the dialog on the programming algorithm and shown in the timing diagram and programming flow chart must be implemented.

## Programming And Blankcheck

### Addressing During Programming and Blankcheck

Addressing to these devices in all modes of operation other than normal read operation is accomplished by multiplexing the upper 5 address bits with the lower 8. The address designations for the lower 8 addressing bits is AX0 through AX7 and the upper 5 address bits are designated AY8 through AY12. This allows sufficient pins for an intelligent programming algorithm to be implemented without the need to switch high voltage signals during the blankcheck, programming, and verification operation.

Addressing while in these modes is accomplished by placing the upper 5 bits of address on pins 8, 7, 6, 5, and 4 with the least significant bit on pin 8. These address bits are

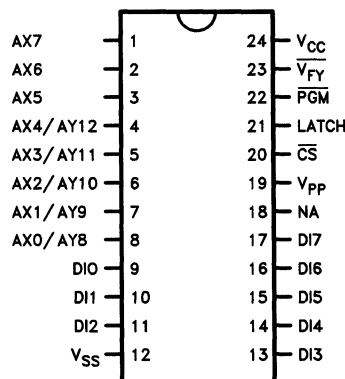
loaded into an onboard register by clocking pin 21, the latch signal, from  $V_{ILP}$  to  $V_{IHP}$  and back to  $V_{ILP}$ . The lower 8 address bits are then placed on pins 8 through 1, with the least significant bit on pin 8. The upper 5 bits remain in the onboard latch until a new value is loaded or power is removed from the device. All 256 bytes addressed by the lower 8 bits may be accessed by sequencing the lower 8 addresses without changing the upper 5 bits or relatching the value in the onboard register.

### Blankcheck

Blankcheck is accomplished by performing a verify cycle, sequencing through all memory address locations, where all the data read will be "0"s.

### Programming Algorithm

Programming is accomplished with an intelligent algorithm. The sequence of operations is to enter the programming mode by placing  $V_{PP}$  on pin 19. This should be done after a minimum delay from power up, and be removed prior to power down by the same delay (see the timing diagram and AC specifications for details). Once in this mode, programming is accomplished by addressing a location as described above, placing the data to be programmed into a location on the data pins, and clocking the  $\overline{PGM}$  signal from  $V_{IHP}$  to  $V_{ILP}$  and back to  $V_{IHP}$  with a pulse width of 200  $\mu s$ . The data is removed from the data pins and the content of the location is then verified by taking the  $\overline{VFY}$  signal from  $V_{IHP}$  to  $V_{ILP}$ , comparing the output with the desired data and then returning  $\overline{VFY}$  to  $V_{IHP}$ . If the contents are correct, a second overprogram pulse of 4 times the original 200  $\mu s$  is delivered with the data to be programmed again on the data pins. If the data is not correct, a second 200  $\mu s$  pulse is applied to  $\overline{PGM}$  with the data to be programmed on the data pins. The compare and overprogram operation is repeated with an overprogram pulse width 4 times the sum of the initial program pulses. This operation is continued until the location is programmed or 10 initial program pulses have been attempted. If on the 10th attempt, the location fails to verify, an overprogram pulse of 8 ms is applied, and the content of the



0052-8

Figure 3. Programming Pinout (DIP Package)

location is once more verified. If the location still fails to verify, the device is rejected. Once a location verifies successfully, the address is advanced to the next location, and the process is repeated until all locations are programmed. After all locations are programmed, they should be verified at  $V_{CCP} = 5.0V$ .

## Operating Modes

### Read

Read is the normal operating mode for a programmed device. In this mode, all signals are normal TTL levels. The PROM is addressed with a 13 bit field, a chip select, (active LOW), is applied to the  $\overline{CS}$  pin, and the contents of the addressed location appear on the data out pins.

### Program, Program Inhibit, Program Verify

These modes are entered by placing a high voltage  $V_{PP}$  on pin 19, with pins 18 and 20 set to  $V_{ILP}$ . In this state, pin 21 becomes a latch signal, allowing the upper 5 address bits to be latched into an onboard register, pin 22 becomes an active LOW program (PGM) signal and pin 23 becomes an active LOW verify (VFY) signal. Pins 22 and 23 should never be active LOW at the same time. The PROGRAM mode exists when PGM is LOW, and VFY is HIGH. The VERIFY mode exists when the reverse is true, PGM HIGH and VFY LOW and the PROGRAM INHIBIT mode is entered with both PGM and VFY HIGH. PROGRAM INHIBIT is specifically provided to allow data to be placed on and removed from the data pins without conflict.

### Blankcheck

Blankcheck mode is identical to PROGRAM VERIFY and is entered in the same manner as described above.

## Programming Sequence

The flowchart in Figure 4 is a detailed description of the intelligent programming cycle used to program the devices covered in this specification. Of particular importance are the areas of power sequencing used to enter and exit the programming operation. This flowchart combined with the timing diagrams AC and DC parameters accurately describe this complete operation. Note should be taken of the inner and outer addressing loops which allow 256 bytes to be programmed each time the onboard register containing the upper 5 address bits is loaded.

The timing diagram in Figure 5 contains all of the timing information necessary for describing the relations required for programming the devices covered in this specification. Some of the information pertains to each cycle of programming as specified in the inner loops of Figure 5, some for the outer loop where the upper address is advanced, and some pertains only to entry and exit from the programming mode of operation.

In particular, the timing sequence associated with the Latch signal on pin 21 and addresses AY8 through AY12 pertain only to the outer loop where the upper 5 (N in the flow chart) address bits are incremented.

$T_p$ ,  $T_{PD}$  and  $T_{HP}$  refer to the entry and exit from the programming mode of operation. Note that this is referenced to LATCH, PGM and VFY operations.

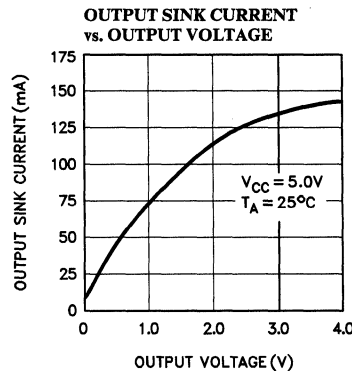
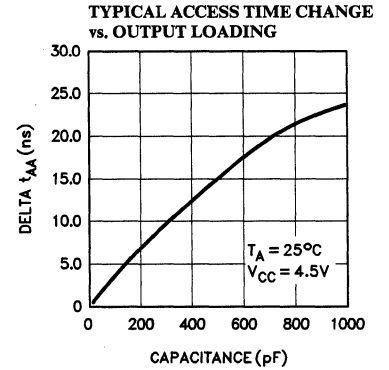
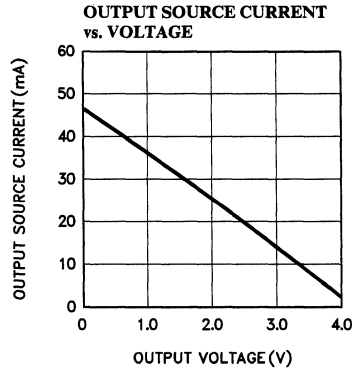
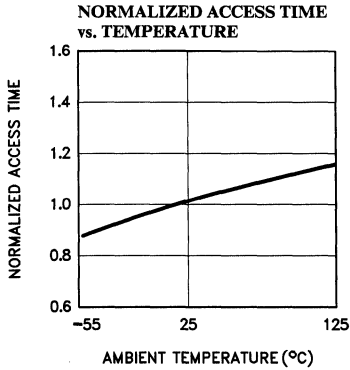
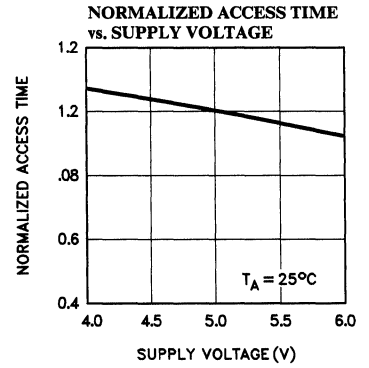
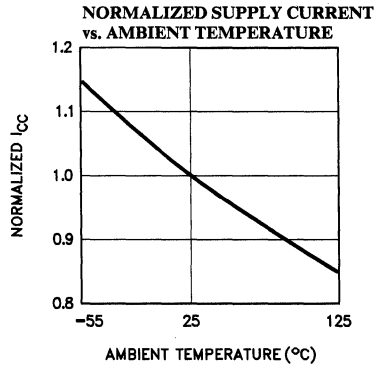
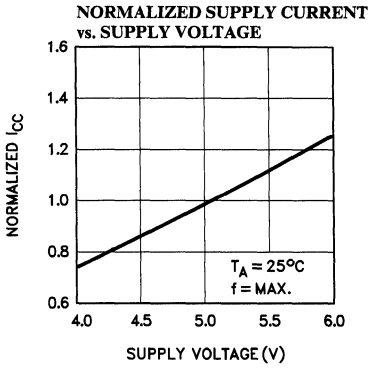
$T_{DS}$ ,  $T_{AS}$ ,  $T_{AH}$  and  $T_{DH}$  refer to the required setup and hold times for the address and data for PGM and VFY operations. These parameters must be adhered to, in all operations, including VFY. This precludes the option then of verifying the device by holding the VFY signal LOW, and sequencing the addresses.

**Table 1. Operating Modes**

| Mode            | Pins 1 thru 3<br>A7-A5, AX7-AX5 | Pins 4 thru 8<br>A4-A0, AX4-AX0<br>AY12-AY8 | Pins 9 thru 11<br>D0 thru D2                   | Pins 13 thru 17<br>D3 thru D7                  | Pin<br>18        | Pin<br>19       | Pin<br>20        | Pin<br>21 | Pin<br>22        | Pin<br>23        |
|-----------------|---------------------------------|---|--|--|------------------|-----------------|------------------|-----------|------------------|------------------|
| Read            | A7 thru A5                      | A4 thru A0                                  | DO0 thru DO2                                   | DO3 thru DO7                                   | A12              | A11             | $\overline{CS}$  | A10       | A9               | A8               |
| Program         | AX7 thru AX5                    | AX4 thru AX0<br>AY12-AY8                    | DI <sub>0</sub> thru DI <sub>2</sub><br>Input  | DI <sub>3</sub> thru DI <sub>7</sub><br>Input  | V <sub>ILP</sub> | V <sub>PP</sub> | V <sub>ILP</sub> | LAT       | V <sub>ILP</sub> | V <sub>IHP</sub> |
| Program Inhibit | AX7 thru AX5                    | AX4 thru AX0<br>AY12-AY8                    | High Z   | High Z   | V <sub>ILP</sub> | V <sub>PP</sub> | V <sub>ILP</sub> | LAT       | V <sub>IHP</sub> | V <sub>IHP</sub> |
| Program Verify  | AX7 thru AX5                    | AX4 thru AX0<br>AY12-AY8                    | DO0 thru DO2<br>Output                         | DO3 thru DO7<br>Output                         | V <sub>ILP</sub> | V <sub>PP</sub> | V <sub>ILP</sub> | LAT       | V <sub>IHP</sub> | V <sub>ILP</sub> |
| Blank Check     | AX7 thru AX5                    | AX4 thru AX0<br>AY12-AY8                    | DI <sub>0</sub> thru DI <sub>2</sub><br>Output | DI <sub>3</sub> thru DI <sub>7</sub><br>Output | V <sub>ILP</sub> | V <sub>PP</sub> | V <sub>ILP</sub> | LAT       | V <sub>IHP</sub> | V <sub>ILP</sub> |

Typical AC and DC Characteristics

3



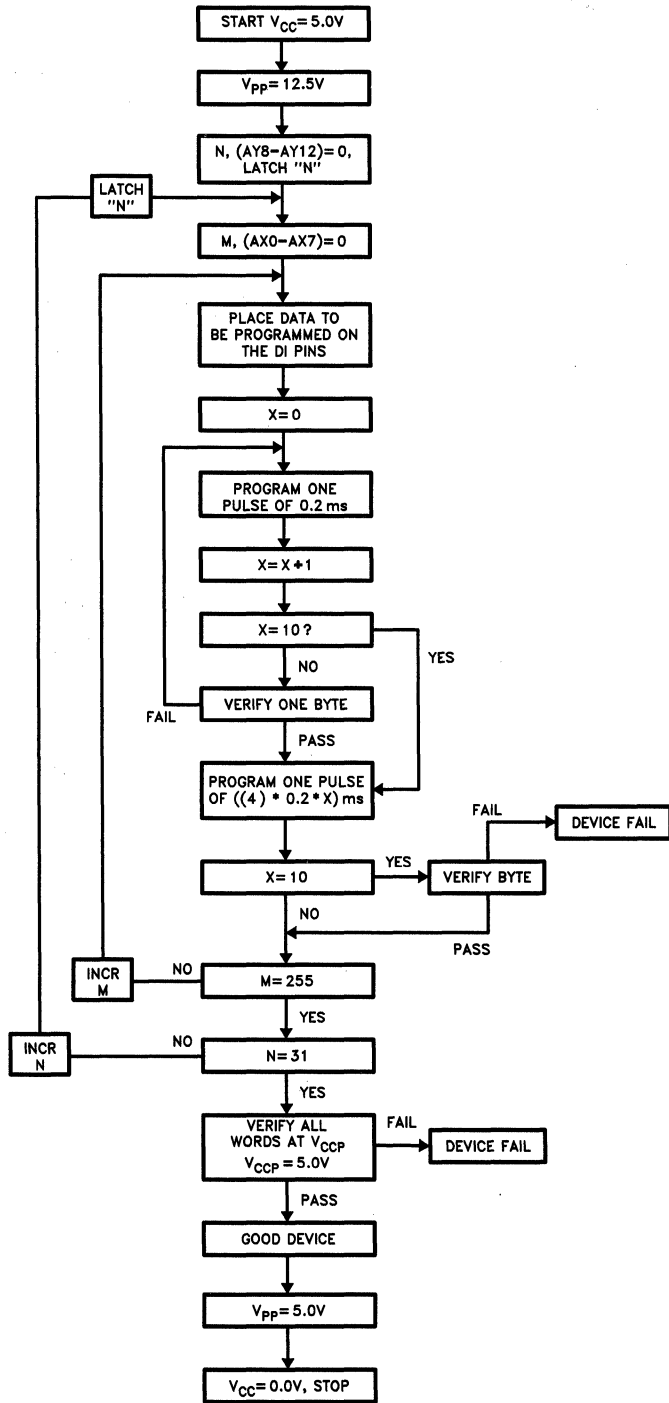
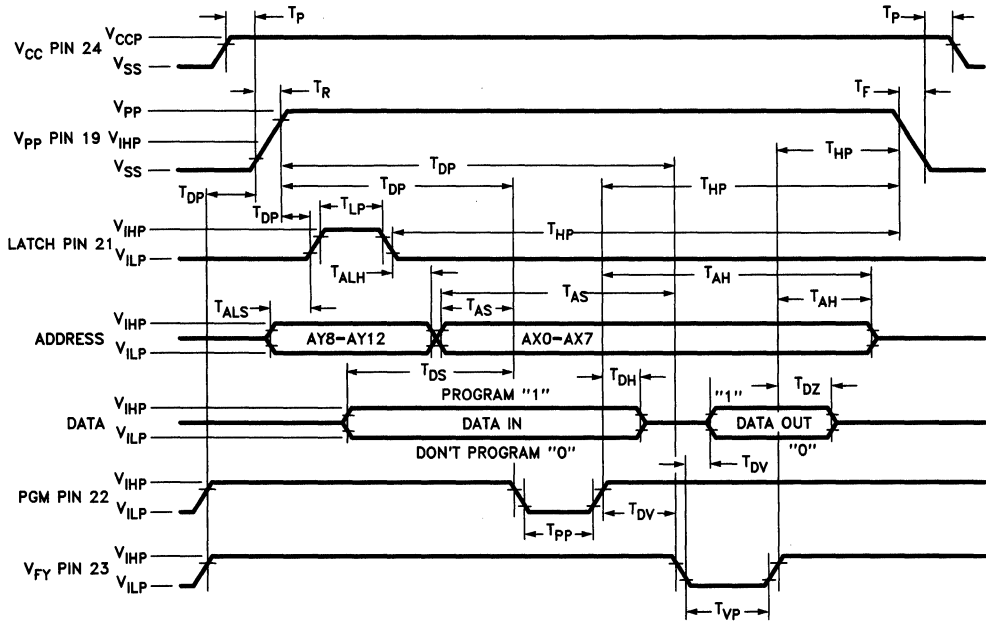


Figure 4. Programming Flowchart

0052-9



**Figure 5. Programming Waveforms**

0052-10

**Note:** Power,  $V_{pp}$  and  $V_{CC}$  should not be cycled for each program verify cycle but remain static during programming.



**Table 2. DC Programming Parameters  $T_A = 25^\circ\text{C}$** 

| Parameter        | Description                             | Min. | Max. | Units |
|------------------|---|------|------|-------|
| V <sub>PP</sub>  | Programming Voltage                     | 12.0 | 13.0 | V     |
| V <sub>CCP</sub> | Power Supply Voltage During Programming | 4.75 | 5.25 | V     |
| I <sub>PP</sub>  | V <sub>PP</sub> Supply Current          |      | 50   | mA    |
| V <sub>IHP</sub> | Input High Voltage During Programming   | 4.75 | 5.25 | V     |
| V <sub>ILP</sub> | Input Low Voltage During Programming    | -3.0 | 0.4  | V     |
| V <sub>OH</sub>  | Output High Voltage                     | 2.4  |      | V     |
| V <sub>OL</sub>  | Output Low Voltage                      |      | 0.4  | V     |

**Table 3. AC Programming Parameters  $T_A = 25^\circ\text{C}$** 

| Parameter         | Description                        | Min. | Max. | Units |
|-------------------|------------------------------------|------|------|-------|
| T <sub>AS</sub>   | Address Setup Time to PGM/VFY      | 1.0  |      | μs    |
| T <sub>AH</sub>   | Address Hold Time from PGM/VFY     | 1.0  |      | μs    |
| T <sub>DS</sub>   | Data Setup Time to PGM             | 1.0  |      | μs    |
| T <sub>DH</sub>   | Data Hold Time PGM                 | 1.0  |      | μs    |
| T <sub>PP</sub>   | Program Pulse Width                | 0.2  | 10   | ms    |
| T <sub>R, F</sub> | V <sub>PP</sub> Rise and Fall Time | 100  |      | ns    |
| T <sub>ALS</sub>  | Address Setup Time to Latch        | 1.0  |      | μs    |
| T <sub>ALH</sub>  | Address Hold Time from Latch       | 1.0  |      | μs    |
| T <sub>LP</sub>   | Latch Pulse Width                  | 1.0  |      | μs    |
| T <sub>DV</sub>   | Delay to Verify                    | 1.0  |      | μs    |
| T <sub>VD</sub>   | Verify to Data Out                 |      | 1.0  | μs    |
| T <sub>VH</sub>   | Data Hold Time from Verify         |      | 1.0  | μs    |
| T <sub>VP</sub>   | Verify Pulse Width                 | 2.0  |      | μs    |
| T <sub>DZ</sub>   | Verify to High Z                   |      | 1.0  | μs    |
| T <sub>DP</sub>   | Delay to Function                  | 1.0  |      | μs    |
| T <sub>HP</sub>   | Hold From Function                 | 1.0  |      | μs    |
| T <sub>P</sub>    | Power Up/Down                      | 20.0 |      | ms    |

**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 35         | CY7C261-35PC  | P13          | Commercial      |
|            | CY7C261-35WC  | W14          |                 |
|            | CY7C263-35PC  | P13          |                 |
|            | CY7C263-35WC  | W14          |                 |
|            | CY7C264-35PC  | P13          |                 |
|            | CY7C264-35WC  | W14          |                 |
|            | CY7C264-35DC  | D12          |                 |
|            | CY7C264-35DC  | D12          |                 |
| 40         | CY7C261-40PC  | P13          | Commercial      |
|            | CY7C261-40WC  | W14          |                 |
|            | CY7C263-40PC  | P13          |                 |
|            | CY7C263-40WC  | W14          |                 |
|            | CY7C264-40PC  | P11          |                 |
|            | CY7C264-40DC  | D12          |                 |
|            | CY7C264-40WC  | W12          |                 |
|            | CY7C264-40WC  | W12          |                 |
| 45         | CY7C261-45PC  | P13          | Commercial      |
|            | CY7C261-45WC  | W14          |                 |
|            | CY7C263-45PC  | P13          |                 |
|            | CY7C263-45WC  | W14          |                 |
|            | CY7C264-45PC  | P11          |                 |
|            | CY7C264-45DC  | D12          |                 |
|            | CY7C264-45WC  | W12          |                 |
|            | CY7C264-45WC  | W12          |                 |
|            | CY7C261-45WMB | W14          |                 |
|            | CY7C261-45DMB | D14          |                 |
|            | CY7C261-45LMB | L64          |                 |
|            | CY7C261-45QMB | Q64          |                 |
|            | CY7C263-45WMB | W14          |                 |
|            | CY7C263-45DMB | D14          |                 |
|            | CY7C263-45LMB | L64          |                 |
|            | CY7C263-45QMB | Q64          |                 |
|            | CY7C264-45DMB | D12          |                 |
|            | CY7C264-45WMB | W12          |                 |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 55         | CY7C261-55PC  | P13          | Commercial      |
|            | CY7C261-55WC  | W14          |                 |
|            | CY7C263-55PC  | P13          |                 |
|            | CY7C263-55WC  | W14          |                 |
|            | CY7C264-55PC  | P11          |                 |
|            | CY7C264-55DC  | D12          |                 |
|            | CY7C264-55WC  | W12          |                 |
|            | CY7C264-55WC  | W12          |                 |
|            | CY7C261-55WMB | W14          |                 |
|            | CY7C261-55DMB | D14          |                 |
|            | CY7C261-55LMB | L64          |                 |
|            | CY7C261-55QMB | Q64          |                 |
|            | CY7C263-55WMB | W14          |                 |
|            | CY7C263-55DMB | D14          |                 |
|            | CY7C263-55LMB | L64          |                 |
|            | CY7C263-55QMB | Q64          |                 |
|            | CY7C264-55DMB | D12          |                 |
|            | CY7C264-55WMB | W12          |                 |

3

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters                     | Subgroups |
|--------------------------------|-----------|
| V <sub>OH</sub>                | 1,2,3     |
| V <sub>OL</sub>                | 1,2,3     |
| V <sub>IH</sub>                | 1,2,3     |
| V <sub>IL</sub>                | 1,2,3     |
| I <sub>PX</sub>                | 1,2,3     |
| I <sub>OZ</sub>                | 1,2,3     |
| I <sub>CC</sub>                | 1,2,3     |
| I <sub>SB</sub> <sup>[2]</sup> | 1,2,3     |

#### Switching Characteristics

| Parameters                        | Subgroups   |
|-----------------------------------|-------------|
| t <sub>AA</sub>                   | 7,8,9,10,11 |
| t <sub>HZCS1</sub> <sup>[1]</sup> | 7,8,9,10,11 |
| t <sub>HZCS2</sub> <sup>[2]</sup> | 7,8,9,10,11 |
| t <sub>ACS1</sub> <sup>[1]</sup>  | 7,8,9,10,11 |
| t <sub>ACS2</sub> <sup>[2]</sup>  | 7,8,9,10,11 |

**Notes:**

1. 7C263 and 7C264 only.
2. 7C261 only.

Document #: 38-00005-D



**Features**

- CMOS for optimum speed/power
- High speed
  - 40 ns max set-up
  - 20 ns clock to output
- Low power
  - 550 mW (commercial)
  - 660 mW (military)
- On-chip edge-triggered registers
  - Ideal for pipelined microprogrammed systems
- EPROM technology
  - 100% programmable
  - Reprogrammable (7C265W)
- 5V ±10% V<sub>CC</sub>, commercial and military
- Capable of withstanding greater than 2001V static discharge

- Slim, 300 mil 28 pin plastic or hermetic DIP

**Functional Description**

The CY7C265 is a 64K Registered PROM. It is organized 8192 words by 8 bits wide, and has a Pipeline Output Register. In addition, the device features a Programmable Initialize Byte which may be loaded into the Pipeline Register with the Initialize signal. The Programmable Initialize Byte is the 8193rd byte in the PROM and its value is programmed at time of use.

Packaged in 28 pins, the PROM has 13 Address Signals (A<sub>0</sub> through A<sub>12</sub>), 8 Data Out Signals (O<sub>0</sub> through O<sub>7</sub>),  $\bar{E}/\bar{I}$ , (Enable or Initialize) and CLOCK.

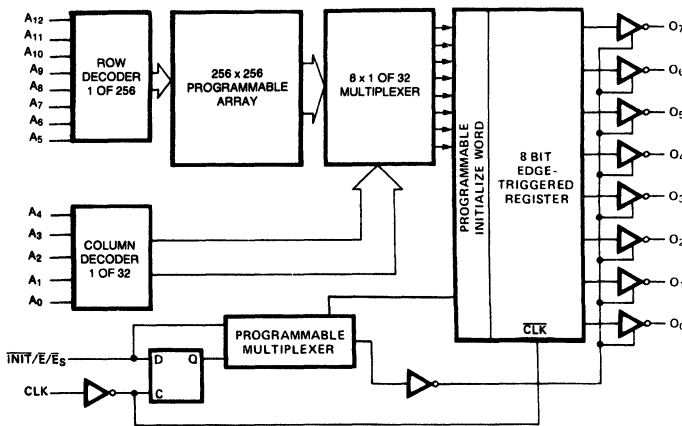
CLOCK functions as a pipeline clock, loading the contents of the addressed

memory location into the Pipeline Register on each rising edge. The data will appear on the Outputs if they are enabled. One pin on the CY7C265 is programmed to perform either the Enable or the Initialize function.

If the asynchronous enable ( $\bar{E}$ ) is being used, the outputs may be disabled at any time by switching the enable to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

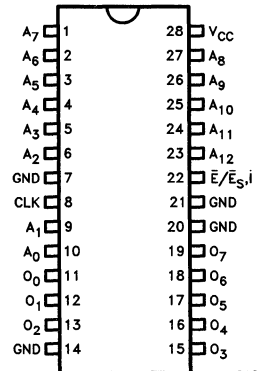
If the synchronous enable ( $\bar{E}_S$ ) is being used, the outputs will go to the OFF or high impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will

**Logic Block Diagram**

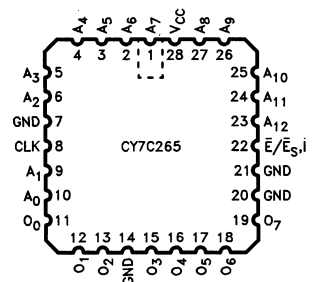


0126-1

**Pin Configurations**



0126-2



0126-3

**Selection Guide**

|                                |            | 7C265-40 | 7C265-50 | 7C265-60 |
|--------------------------------|------------|----------|----------|----------|
| Maximum Set-Up Time (ns)       |            | 40       | 50       | 60       |
| Maximum Clock to Output (ns)   |            | 20       | 25       | 25       |
| Maximum Operating Current (mA) | Commercial | 100      | 80       | 80       |
|                                | Military   |          | 120      | 100      |

**Functional Description (Continued)**

return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low to high transition of the clock. This unique feature allows the CY7C265 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

If the  $\bar{E}/I$  pin is used for  $\overline{INIT}$  (asynchronous) then the outputs are permanently enabled. The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated the initialize control input causes the contents of a user programmed 8193rd 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of "1"s and "0"s into the register. In the unprogrammed state, activating  $\overline{INIT}$  will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating  $\overline{INIT}$  performs a register PRESET (all outputs HIGH).

Applying a LOW to the  $\overline{INIT}$  input causes an immediate load of the programmed initialize word into the pipeline register and onto the outputs. The  $\overline{INIT}$  LOW disables clock and must return HIGH to enable CLOCK independent of all other inputs, including the clock.

**Electrical Characteristics Over the Operating Range<sup>[2]</sup>**

| Parameters      | Description                              | Test Conditions  | Commercial |      | Military |      | Units |
|-----------------|--|--|------------|------|----------|------|-------|
|                 |  |  | Min.       | Max. | Min.     | Max. |       |
| V <sub>OH</sub> | Output HIGH Voltage                      | V <sub>CC</sub> = Min., I <sub>OH</sub> = -2 mA  | 2.4        |      | 2.4      |      | V     |
| V <sub>OL</sub> | Output LOW Voltage                       | V <sub>CC</sub> = Min., I <sub>OL</sub> = 12 mA<br>(I <sub>OL</sub> = 8 mA for Military) |            | 0.4  |          | 0.4  | V     |
| V <sub>IH</sub> | Input HIGH Voltage                       |  | 2.0        |      | 2.0      |      | V     |
| V <sub>IL</sub> | Input LOW Voltage                        |  |            | 0.8  |          | 0.8  | V     |
| I <sub>IX</sub> | Input Load Current                       | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>  |            | 10   |          | 10   | μA    |
| I <sub>OZ</sub> | Output Leakage Current                   | GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub><br>Output Disabled                              |            | 40   |          | 40   | μA    |
| I <sub>OS</sub> | Output Short Circuit Current             | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND   |            | 90   |          | 90   | mA    |
| I <sub>CC</sub> | V <sub>CC</sub> Operating Supply Current | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA  | 7C265-40   | 100  |          |      | mA    |
|                 |  |  | 7C265-50   | 80   |          | 120  |       |
|                 |  |  | 7C265-60   | 80   |          | 100  |       |

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential .... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

DC Program Voltage ..... 13.0V

Static Discharge Voltage ..... > 2001V  
(per MIL-STD-883, Method 3015)

Latchup Current ..... > 200 mA

UV Exposure ..... 7258 Wsec/cm<sup>2</sup>

**Operating Range**

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to 70°C         | 5V ± 10%        |
| Military <sup>[1]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 8    |       |

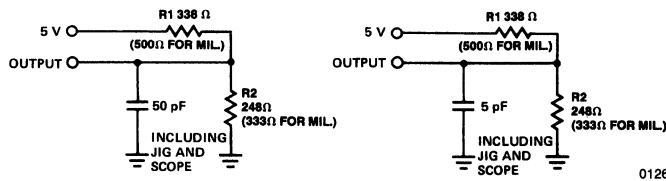
### Switching Characteristics Over the Operating Range<sup>[2]</sup>

| Parameters       | Description                                       | 7C265-40 |      | 7C265-50 |      | 7C265-60 |      | Units |
|------------------|---|----------|------|----------|------|----------|------|-------|
|                  |   | Min.     | Max. | Min.     | Max. | Min.     | Max. |       |
| t <sub>AS</sub>  | Address Set-Up to Clock                           | 40       |      | 50       |      | 60       |      | ns    |
| t <sub>HA</sub>  | Address Hold from Clock                           | 0        |      | 0        |      | 0        |      | ns    |
| t <sub>CO</sub>  | Clock to Output Valid                             |          | 20   |          | 25   |          | 25   | ns    |
| tpw              | Clock Pulse Width                                 | 15       |      | 20       |      | 20       |      | ns    |
| t <sub>SES</sub> | ES Set-Up to Clock (Sync Enable Only)             | 15       |      | 15       |      | 15       |      | ns    |
| t <sub>HES</sub> | ES Hold from Clock                                | 5        |      | 5        |      | 5        |      | ns    |
| t <sub>DI</sub>  | Init to Out Valid                                 |          | 25   |          | 35   |          | 35   | ns    |
| t <sub>RI</sub>  | Init Recovery to Clock                            | 20       |      | 25       |      | 25       |      | ns    |
| tpwi             | Init Pulse Width                                  | 25       |      | 35       |      | 35       |      | ns    |
| t <sub>COS</sub> | Output Valid from Clock (Sync. Mode)              |          | 20   |          | 25   |          | 25   | ns    |
| t <sub>HZC</sub> | Output Inactive from Clock (Sync. Mode)           |          | 20   |          | 25   |          | 25   | ns    |
| t <sub>DOE</sub> | Output Valid from $\bar{E}$ Low (Async. Mode)     |          | 20   |          | 25   |          | 25   | ns    |
| t <sub>HZE</sub> | Output Inactive from $\bar{E}$ High (Async. Mode) |          | 20   |          | 25   |          | 25   | ns    |

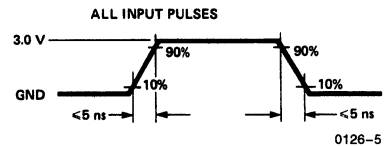
**Notes:**

- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.

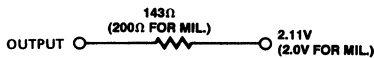
### AC Test Loads and Waveforms



0126-4

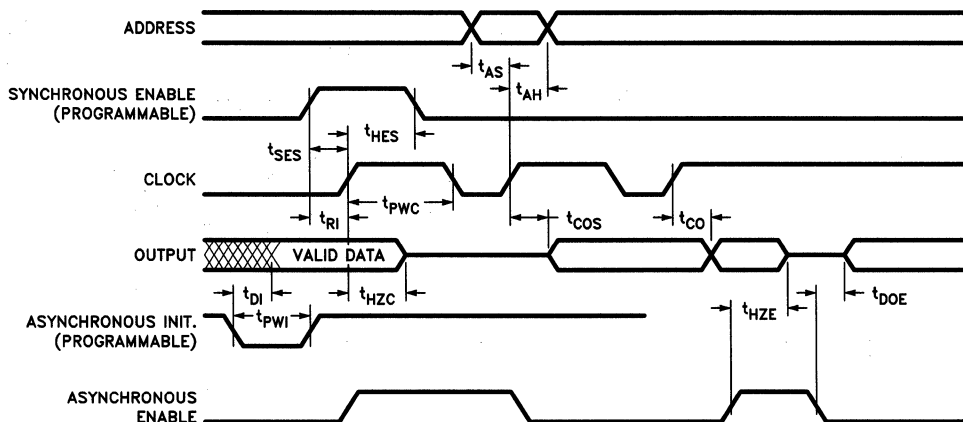


0126-5



0126-6

## Switching Waveforms



### Notes on Testing:

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device  $V_{CC}$  and ground terminals. Multiple capacitors are recommended, including a  $0.1 \mu\text{F}$  or larger capacitor and a  $0.01 \mu\text{F}$  or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.

3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level  $-500 \text{ mV}$  or steady state LOW level  $+500 \text{ mV}$  on the output from the 1.5V level on inputs with load shown in Figure 1b.

0126-7

## Device Programming

The CY7C265 utilizes an intelligent programming algorithm to assure consistent programming quality. These 64K PROMs use a single ended memory cell design. In an unprogrammed state, the memory contains all "0"s. During programming, a "1" on a data-in pin causes the addressed location to be programmed, and a "0" causes the location to remain unprogrammed.

### Programming Pinout

The Programming Pinout is shown in Figure 3. The programming mode is entered by putting 12.5V on the  $V_{pp}$  pin. The addressed location is programmed and verified with the application of a PGM and VFY pulse. Entering and exiting the programming mode should be done with care. Proper sequencing as described in the dialog on the programming algorithm and shown in the timing diagram and programming flow chart must be implemented.

## Programming and Blankcheck (Memory Bits)

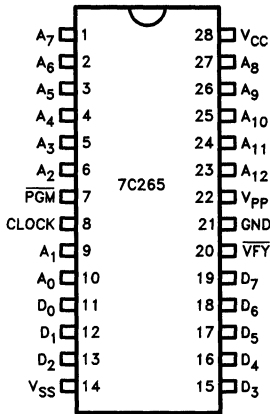
### Blankcheck

Blankcheck is accomplished by performing a verify cycle (VFY toggles on each address), sequencing through all memory address locations, where all the data read will be "0"s. (Refer to mode table for pin states)

### Programming Algorithm

Programming is accomplished with an intelligent algorithm. The sequence of operations is to enter the programming mode by placing 12.5V on  $V_{pp}$ . This should be done after a minimum delay from power up, and be removed prior to power down by the same delay (see the timing diagram and AC specifications for details). Once in this mode, programming is accomplished by addressing a location as described above, placing the data to be programmed into a location on the data pins, and clocking the PGM signal from  $V_{IHP}$  to  $V_{ILP}$  and back to  $V_{IHP}$  with a pulse width of  $200 \mu\text{s}$ . The data is removed from the data pins and the content of the location is then verified by taking the VFY signal from  $V_{IHP}$  to  $V_{ILP}$ , comparing the output with the desired data and then returning VFY to  $V_{IHP}$ . If the contents are correct, a second overprogram pulse of 4 times the original  $200 \mu\text{s}$  is delivered with the data to be programmed again on the data pins. If the data is not correct, a second  $200 \mu\text{s}$  pulse is applied to PGM with the data to be programmed on the data pins. The compare and overprogram operation is repeated with an overprogram pulse width 4 times the sum of the initial program pulses. This operation is continued until the location is programmed or 10 initial program pulses have been attempted. If on the 10th attempt, the location fails to verify, an overprogram pulse of 8 ms is applied, and the content of the

**Programming and Blankcheck (Memory Bits) (Continued)**



**Figure 3. 7C265 Programming Pinout**

0126-8

location is once more verified. If the location still fails to verify, the device is rejected. Once a location verifies successfully, the address is advanced to the next location, and the process is repeated until all locations are programmed.

After all locations are programmed, they should be verified at  $V_{CCP} = 5.0V$ .

**Programming Algorithm for the Architecture**

The CY7C265 offers a limited selection of programmed architecture. Programming these features should be done

**Mode Table**

| Mode Select                         | P2<br>A6 | P3<br>A5 | P26<br>A9 | P6<br>A2 | P7<br>PGM | P8<br>CLK | P9<br>A1 | P10<br>A0 | P20<br>VFY | P24<br>A11 | P22<br>E/I<br>VPP | P23<br>A12 |
|-------------------------------------|----------|----------|-----------|----------|-----------|-----------|----------|-----------|------------|------------|-------------------|------------|
| Normal Read                         | A6       | A5       | A9        | A2       | L         | L/H       | A1       | A0        | HI Z       | A11        | H/L               | A12        |
| Program (Memory)                    | A6       | A5       | A9        | A2       | L         | L         | A1       | A0        | H          | A11        | VPP               | A12        |
| Program Verify                      | A6       | A5       | A9        | A2       | H         | L         | A1       | A0        | L          | A11        | VPP               | A12        |
| Program Inhibit                     | A6       | A5       | A9        | A2       | H         | L         | A1       | A0        | H          | A11        | VPP               | A12        |
| Async. Enable Read                  | A6       | A5       | A9        | A2       | L         | L         | A1       | A0        | HI Z       | A11        | L                 | A12        |
| Sync. Enable Read                   | A6       | A5       | A9        | A2       | L         | L/H       | A1       | A0        | HI Z       | A11        | L                 | A12        |
| Async. Init. Read                   | A6       | A5       | A9        | A2       | L         | L         | A1       | A0        | HI Z       | A11        | L                 | A12        |
| Program Sync. Enable <sup>[1]</sup> | H        | VPP      | A9        | H        | L         | L         | VPP      | L         | H          | H          | VPP               | H          |
| Program Initialize <sup>[2]</sup>   | H        | VPP      | A9        | L        | L         | L         | VPP      | L         | H          | H          | VPP               | L          |
| Program Initial Byte                | H        | VPP      | A9        | L        | L         | L         | VPP      | H         | H          | L          | VPP               | A12        |

**Notes:**

1. Default is Async. Enable.
2. Default is Enable.

with a single 10 ms wide pulse in place of the intelligent algorithm mainly because these features are verified operationally, not with the VFY pin. Architecture programming is implemented by applying the supervoltage to two additional pins during programming. In programming the 7C265 architecture Vpp is applied to pins 3, 9 and 22. Specific choice of a particular mode will depend on the states of the other pins during programming so it is important that the condition of the other pins be met as set forth in the mode table. The same considerations with respect to power up and power down apply during architecture programming as during intelligent programming. Once the supervoltages have been established and the correct logic states exist on the other device pins, programming may begin. Programming is accomplished by pulling PGM from HIGH to LOW and then back to HIGH with a pulse width equal to 10 ms.

To check whether a 7C265 has been programmed as output enable or initialize enable, pin 22 (E/I) should be pulled LOW followed by a LOW to HIGH transition on pin 8 (CLOCK). The data read at the outputs is stored and complement data is shifted into the shadow register. A shift from shadow to pipeline is performed and the CLOCK is again pulled from LOW to HIGH. At this point, if the new data read is data-complement, the device has been programmed as Output enable while if the new data read-true then the device is programmed as Initialize enable. The configuration of the Initialize byte can be read directly by pulling E/I from HIGH to LOW.



**DC Programming Parameters**  $T_A = 25^\circ\text{C}$ 

| Parameter        | Description                             | Min. | Max. | Units |
|------------------|---|------|------|-------|
| V <sub>PP</sub>  | Programming Voltage                     | 12.0 | 13.0 | V     |
| V <sub>CCP</sub> | Power Supply Voltage During Programming | 4.75 | 5.25 | V     |
| I <sub>PP</sub>  | V <sub>PP</sub> Supply Current          |      | 50   | mA    |
| V <sub>IHP</sub> | Input High Voltage During Programming   | 3.0  |      | V     |
| V <sub>ILP</sub> | Input Low Voltage During Programming    | -3.0 | 0.4  | V     |
| V <sub>OH</sub>  | Output High Voltage                     | 2.4  |      | V     |
| V <sub>OL</sub>  | Output Low Voltage                      |      | 0.4  | V     |

**AC Programming Parameters**  $T_A = 25^\circ\text{C}$ 

| Parameter        | Description                        | Min. | Max. | Units |
|------------------|------------------------------------|------|------|-------|
| t <sub>PP</sub>  | Program Pulse Width (Per Byte)     |      | 10.0 | ms    |
| t <sub>AS</sub>  | Address Set-Up Time                | 1.0  |      | μs    |
| t <sub>AH</sub>  | Address Hold Time                  | 1.0  |      | μs    |
| t <sub>DH</sub>  | Data Hold Time                     | 1.0  |      | μs    |
| t <sub>DS</sub>  | Data Set-Up Time                   | 1.0  |      | μs    |
| t <sub>R,F</sub> | V <sub>PP</sub> Rise and Fall Time | 1.0  |      | μs    |
| t <sub>DV</sub>  | Delay to Verify                    | 1.0  |      | μs    |
| t <sub>VD</sub>  | Verify to Data Out                 |      | 1.0  | μs    |
| t <sub>VH</sub>  | Data Hold Time from Verify         |      | 1.0  | μs    |
| t <sub>VP</sub>  | Verify Pulse Width                 | 2.0  |      | μs    |
| t <sub>DZ</sub>  | Verify to High Z                   |      | 1.0  | μs    |

**Erase Characteristics**

Wavelengths of light less than 4000 Angstroms begin to erase the CY7C265 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV

intensity  $\times$  exposure time) or 25 Wsec/cm<sup>2</sup>. For an ultraviolet lamp with a 12 mW/cm<sup>2</sup> power rating the exposure time would be approximately 45 minutes. The CY7C265 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm<sup>2</sup> is the recommended maximum dosage.

**Bit Map Data**

| Programmer Address |      | RAM Data     |
|--------------------|------|--------------|
| Decimal            | Hex  | Contents     |
| 0                  | 0    | DATA         |
| •                  | •    | •            |
| •                  | •    | •            |
| •                  | •    | •            |
| 8191               | 1FFF | DATA         |
| 8192               | 2000 | INIT BYTE    |
| 8193               | 2001 | CONTROL BYTE |

**Control Byte**

- 00 Asynchronous output enable (default condition)
- 01 Synchronous output enable
- 02 Asynchronous initialize

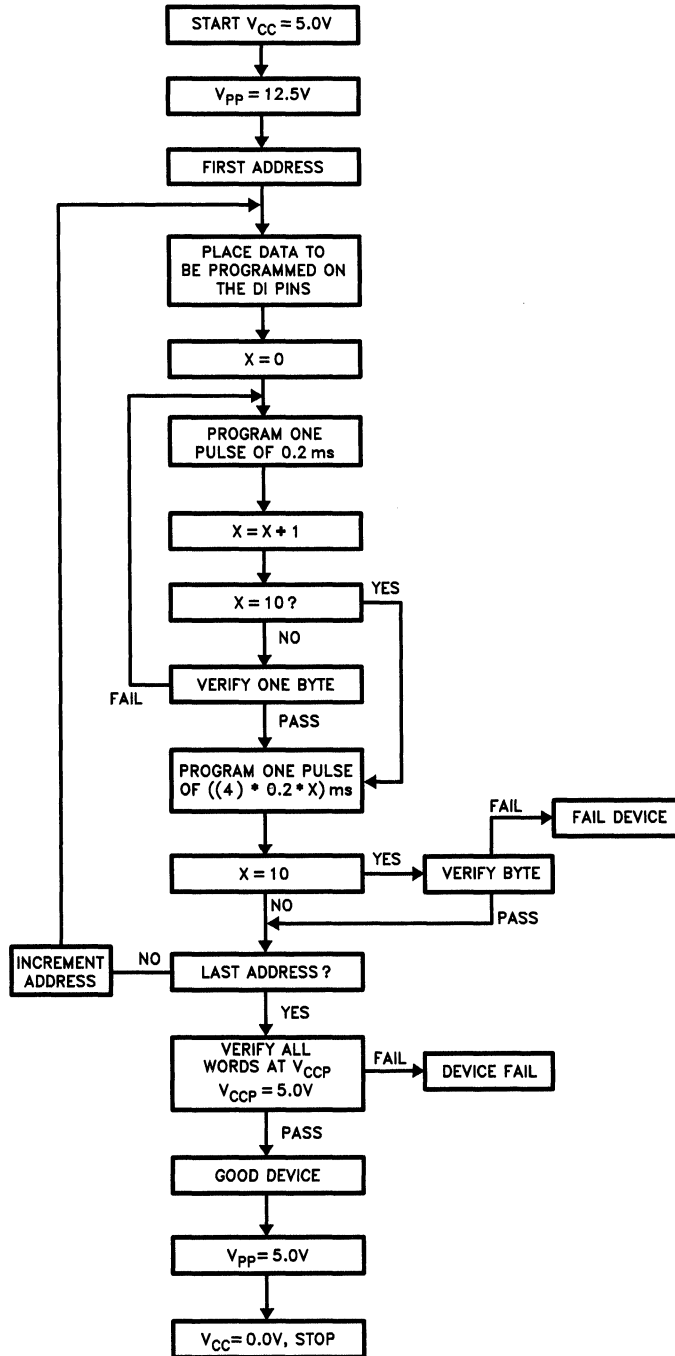
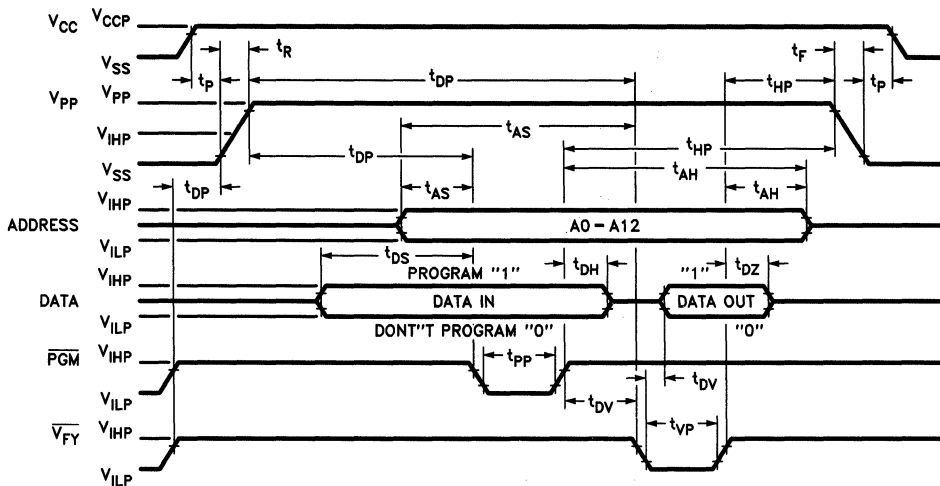


Figure 4. Programming Flowchart

0126-9

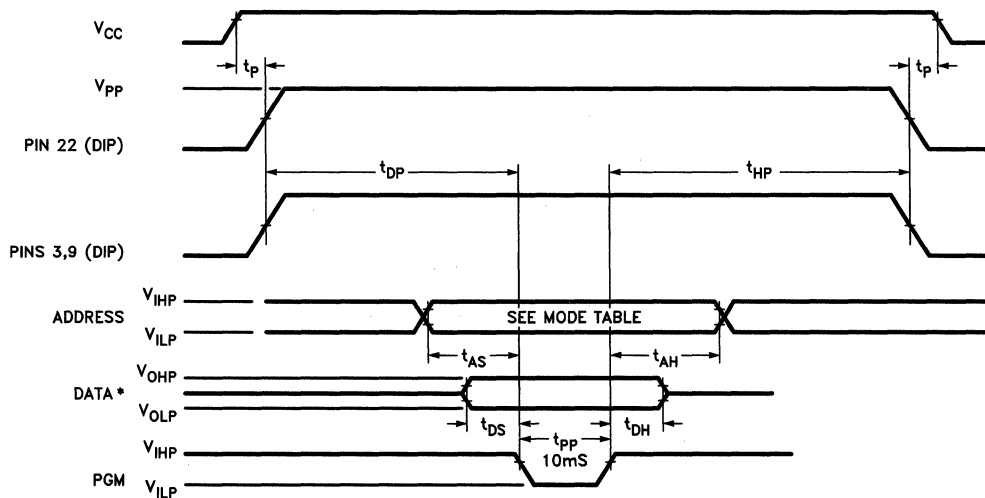


0126-10

Figure 5. Programming Waveforms (Memory)

Note:

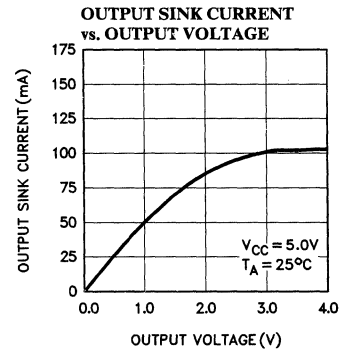
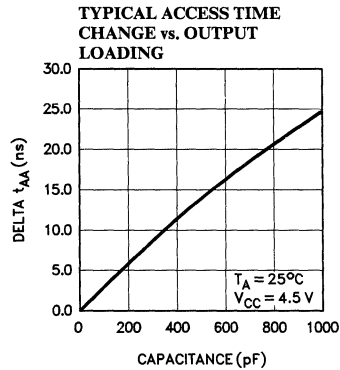
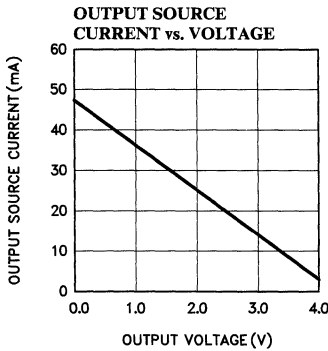
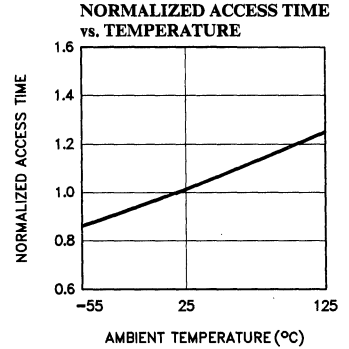
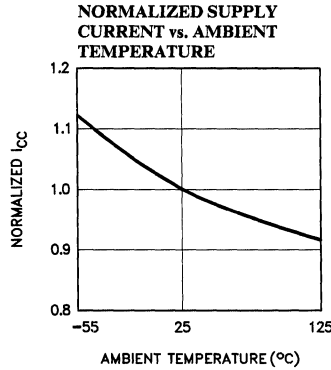
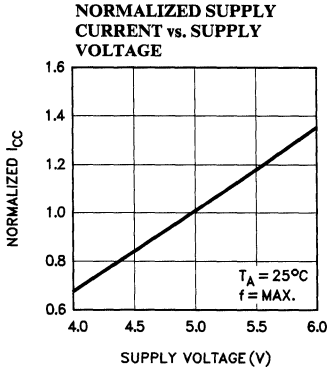
Power, Vpp and VCC should not be cycled for each program verify cycle but remain static during programming.



0126-11

\*Data required on I/O's only during initial programming.

Figure 6. Programming Waveforms for the Architecture

**Typical DC and AC Characteristics**


0126-12

**Ordering Information**

| Speed (ns) | $I_{CC}$ (mA) | Ordering Code | Package Type  | Operating Range |          |
|------------|---------------|---------------|---------------|-----------------|----------|
| 40         | 100           | CY7C265-40PC  | P21           | Commercial      |          |
|            |               | CY7C265-40DC  | D22           |                 |          |
|            |               | CY7C265-40WC  | W22           |                 |          |
| 50         | 80            | CY7C265-50PC  | P21           | Commercial      |          |
|            |               | CY7C265-50DC  | D22           |                 |          |
|            |               | CY7C265-50WC  | W22           |                 |          |
|            | 120           | 120           | CY7C265-50DMB | D22             | Military |
|            |               |               | CY7C265-50WMB | W22             |          |
|            |               |               | CY7C265-50LMB | L64             |          |
|            |               |               | CY7C265-50QMB | Q64             |          |

| Speed (ns) | $I_{CC}$ (mA) | Ordering Code | Package Type | Operating Range |
|------------|---------------|---------------|--------------|-----------------|
| 60         | 80            | CY7C265-60PC  | P21          | Commercial      |
|            |               | CY7C265-60DC  | D22          |                 |
|            |               | CY7C265-60WC  | W22          |                 |
| 100        | 100           | CY7C265-60DMB | D22          | Military        |
|            |               | CY7C265-60WMB | W22          |                 |
|            |               | CY7C265-60LMB | L64          |                 |
|            |               | CY7C265-60QMB | Q64          |                 |

**MILITARY SPECIFICATIONS****Group A Subgroup Testing****DC Characteristics**

| Parameters      | Subgroups |
|-----------------|-----------|
| V <sub>OH</sub> | 1,2,3     |
| V <sub>OL</sub> | 1,2,3     |
| V <sub>IH</sub> | 1,2,3     |
| V <sub>IL</sub> | 1,2,3     |
| I <sub>IX</sub> | 1,2,3     |
| I <sub>OZ</sub> | 1,2,3     |
| I <sub>CC</sub> | 1,2,3     |
| I <sub>SB</sub> | 1,2,3     |

**Switching Characteristics**

| Parameters       | Subgroups   |
|------------------|-------------|
| t <sub>AS</sub>  | 7,8,9,10,11 |
| t <sub>HA</sub>  | 7,8,9,10,11 |
| t <sub>CO</sub>  | 7,8,9,10,11 |
| tp <sub>W</sub>  | 7,8,9,10,11 |
| t <sub>SES</sub> | 7,8,9,10,11 |
| t <sub>HES</sub> | 7,8,9,10,11 |
| t <sub>COS</sub> | 7,8,9,10,11 |

Document #: 38-00084-A



# 8192 x 8 PROM Power Switched and Reprogrammable

3

## Features

- CMOS for optimum speed/power
- Windowed for reprogrammability
- High speed
  - 55 ns (commercial)
  - 55 ns (military)
- Low power
  - 440 mW (commercial)
  - 495 mW (military)
- Super low standby power
  - Less than 85 mW when deselected
- EPROM technology 100% programmable
- 5V ± 10% V<sub>CC</sub>, commercial and military
- TTL compatible I/O

- Direct replacement for EPROMs
- Capable of withstanding > 2000V static discharge

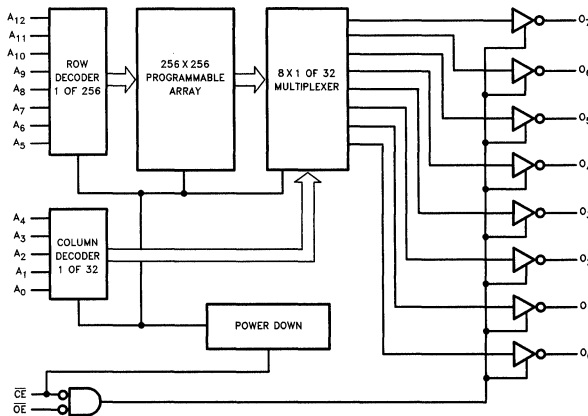
## Product Characteristics

The CY7C266 is a high performance 8192 word by 8 bit CMOS PROM. When deselected, the 7C266 automatically powers down into a low power stand-by mode. It is packaged in the 600 mil wide package. The reprogrammable CERDIP packages are equipped with an erasure window; when exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C266 is a plug-in replacement for EPROM devices. The EPROM cell requires only 12.5V for the superelectrode and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

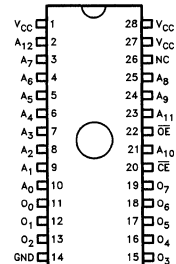
Reading is accomplished by placing an active LOW signal on OE and CE. The contents of the memory location addressed by the address lines (A<sub>0</sub>–A<sub>12</sub>) will become available on the output lines (O<sub>0</sub>–O<sub>7</sub>).

## Logic Block Diagram

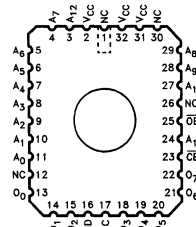


0137-1

## Pin Configurations



0137-2



0137-3

## Selection Guide

|                                |            | 7C266-55 |
|--------------------------------|------------|----------|
| Maximum Access Time (ns)       |            | 55       |
| Maximum Operating Current (mA) | Commercial | 80       |
|                                | Military   | 90       |
| Standby Current (mA)           | Commercial | 15       |
|                                | Military   | 15       |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|  |                 |
|--|-----------------|
| Storage Temperature .....                                      | -65°C to +150°C |
| Ambient Temperature with<br>Power Applied .....                | -55°C to +125°C |
| Supply Voltage to Ground Potential<br>(Pin 28 to Pin 14) ..... | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs<br>in High Z State .....         | -0.5V to +7.0V  |
| DC Input Voltage .....   | -3.0V to +7.0V  |
| DC Program Voltage .....                                       | 14.0V           |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | >2001V<br>(per MIL-STD-883, Method 3015) |
| Latchup Current .....          | >200 mA                                  |
| UV Exposure .....              | 7258 Wsec/cm <sup>2</sup>                |

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[5]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over the Operating Range<sup>[6]</sup>

| Parameters       | Description                                 | Test Conditions   | 7C266-55   |      | Units |
|------------------|---|---|------------|------|-------|
|                  |   |   | Min.       | Max. |       |
| V <sub>OH</sub>  | Output HIGH Voltage                         | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA                           | 2.4        |      | V     |
| V <sub>OL</sub>  | Output LOW Voltage                          | V <sub>CC</sub> = Min., I <sub>OL</sub> = 16.0 mA                           |            | 0.4  | V     |
| V <sub>IH</sub>  | Input HIGH Level <sup>[1]</sup>             |   | 2.0        |      | V     |
| V <sub>IL</sub>  | Input LOW Level <sup>[1]</sup>              |   |            | 0.8  | V     |
| I <sub>IX</sub>  | Input Current                               | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                                     | -10        | +10  | μA    |
| V <sub>CD</sub>  | Input Diode Clamp Voltage                   |   | Note 2     |      |       |
| I <sub>OZ</sub>  | Output Leakage Current                      | V <sub>OL</sub> ≤ V <sub>OUT</sub> ≤ V <sub>OH</sub> , Output Disabled      | -10        | +10  | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[3]</sup> | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND                              | -20        | -90  | mA    |
| I <sub>CC1</sub> | Power Supply Current <sup>[8]</sup>         | CMOS Inputs: GND ± 0.3V or V <sub>CC</sub> ± 0.3V                           | Commercial | 20   | mA    |
|                  |   |   | Military   | 30   | mA    |
| I <sub>CC2</sub> | Power Supply Current <sup>[8]</sup>         | TTL Inputs<br>V <sub>IL</sub> ≤ 0.8V, V <sub>IH</sub> ≥ 2.0V                | Commercial | 25   | mA    |
|                  |   |   | Military   | 35   | mA    |
| I <sub>SB1</sub> | Standby Supply Current <sup>[7]</sup>       | CE = V <sub>CC</sub> ± 0.3V<br>CMOS Inputs (GND or V <sub>CC</sub> ) ± 0.3V | Commercial | 15   | mA    |
|                  |   |   | Military   | 15   | mA    |
| I <sub>SB2</sub> | Standby Supply Current <sup>[7]</sup>       | TTL Inputs<br>V <sub>IL</sub> ≤ 0.8V, V <sub>IH</sub> ≥ 2.0V                | Commercial | 15   | mA    |
|                  |   |   | Military   | 15   | mA    |

### Capacitance<sup>[4]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 8    |       |

#### Notes:

1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. The CMOS process does not provide a clamp diode. However, the CY7C266 is insensitive to -3V dc input levels and -5V undershoot pulses of less than 10 ns (measured at 50% point).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.
5. T<sub>A</sub> is the "instant on" case temperature.
6. See the last page of this specification for Group A subgroup testing information.
7. AC power component add 1 mA/MHz, V<sub>CC</sub> = max, I<sub>OUT</sub> = 0.
8. AC power component add 3 mA/MHz, V<sub>CC</sub> = max, I<sub>OUT</sub> = 0.

Switching Characteristics Over the Operating Range<sup>[5, 6, 9]</sup>

| Parameters        | Description                                      | 7C266-55 |      | Units |
|-------------------|--|----------|------|-------|
|                   |  | Min.     | Max. |       |
| t <sub>AA</sub>   | Address to Output Valid                          |          | 55   | ns    |
| t <sub>HZCE</sub> | Chip Enable Inactive to High Z <sup>[10]</sup>   |          | 55   | ns    |
| t <sub>HZOE</sub> | Output Enable Inactive to High Z <sup>[10]</sup> |          | 20   | ns    |
| t <sub>AOE</sub>  | Output Enable Active to Output Valid             |          | 20   | ns    |
| t <sub>ACE</sub>  | Chip Enable Active to Output Valid               |          | 55   | ns    |
| t <sub>OHA</sub>  | Data Hold from Address Change                    | 3        |      | ns    |

3

AC Test Loads and Waveforms

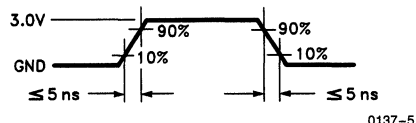
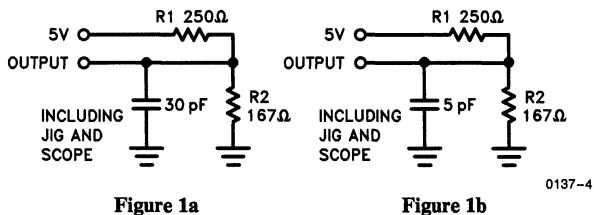
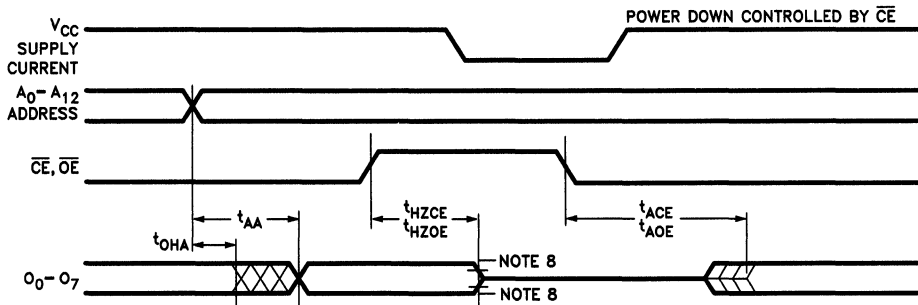
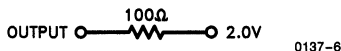


Figure 2. Input Pulses

Figure 1a

Figure 1b

Equivalent to: THÉVENIN EQUIVALENT



Notes:

9. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and loads shown in Figure 1a, 1b.

10. t<sub>HZCS</sub> is tested with load shown in Figure 1b. Transition is measured at steady state High level - 500 mV or steady state Low level + 500 mV on the output from the 1.5V level on the input.

Erasur Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the devices in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV

intensity × exposure time) or 25 Wsec/cm<sup>2</sup>. For an ultra-violet lamp with a 12 mW/cm<sup>2</sup> power rating the exposure time would be approximately 45 minutes. The 7C266 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high intensity UV light for an extended period of time. 7258W × sec/cm<sup>2</sup> is the recommended maximum dosage.



### Ordering Information

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 55         | CY7C266-55PC  | P15          | Commercial      |
|            | CY7C266-55WC  | W16          |                 |
|            | CY7C266-55DC  | D16          |                 |
|            | CY7C266-55WMB | W16          | Military        |
|            | CY7C266-55DMB | D16          |                 |
|            | CY7C266-55LMB | L55          |                 |
|            | CY7C266-55QMB | Q55          |                 |

**MILITARY SPECIFICATIONS****Group A Subgroup Testing****DC Characteristics**

| Parameters      | Subgroups |
|-----------------|-----------|
| V <sub>OH</sub> | 1,2,3     |
| V <sub>OL</sub> | 1,2,3     |
| V <sub>IH</sub> | 1,2,3     |
| V <sub>IL</sub> | 1,2,3     |
| I <sub>IX</sub> | 1,2,3     |
| I <sub>OZ</sub> | 1,2,3     |
| I <sub>CC</sub> | 1,2,3     |
| I <sub>SB</sub> | 1,2,3     |

3

**Switching Characteristics**

| Parameters        | Subgroups   |
|-------------------|-------------|
| t <sub>AA</sub>   | 7,8,9,10,11 |
| t <sub>HZOE</sub> | 7,8,9,10,11 |
| t <sub>HZCE</sub> | 7,8,9,10,11 |
| t <sub>AOE</sub>  | 7,8,9,10,11 |
| t <sub>ACE</sub>  | 7,8,9,10,11 |

Document #: 38-00086-C



# 64K Registered Diagnostic PROM

## Features

- CMOS for optimum speed/power
- High speed
  - 40 ns max set-up
  - 20 ns clock to output
- Low power
  - 550 mW (commercial)
  - 660 mW (military)
- On-chip edge-triggered registers
  - Ideal for pipelined microprogrammed systems
- On-chip diagnostic shift register
  - For serial observability and controllability of the output register
- EPROM technology
  - 100% programmable
  - Reprogrammable (7C269W)
- 5V ±10% V<sub>CC</sub>, commercial and military
- Capable of withstanding greater than 2001V static discharge
- Slim, 300 mil 28 pin plastic or hermetic DIP (7C269)

## Functional Description

The CY7C268 and CY7C269 are 64K Registered Diagnostic PROMs. They are both organized 8192 words by 8 bits wide, and have both a Pipeline Output Register and an Onboard Diagnostic Shift Register. In addition, both devices feature a Programmable Initialize Byte which may be loaded into the Pipeline Register with the Initialize signal. The Programmable Initialize Byte is the 8193rd byte in the PROM and its value is programmed at time of use.

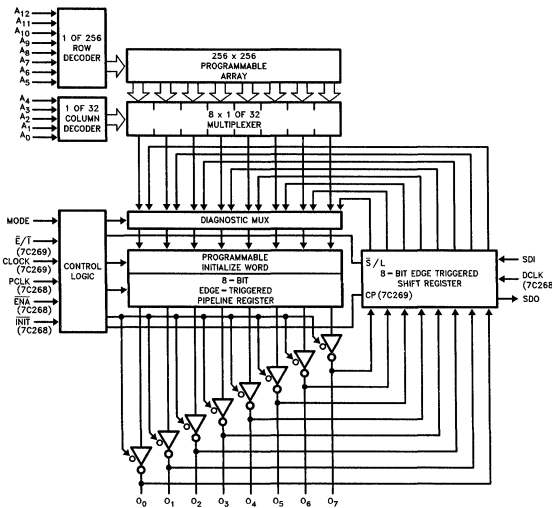
The 7C268 has 32 pins and features full diagnostic capabilities while the 7C269 provides limited diagnostics and is available in a space efficient 28 pin package. This allows the designer to optimize his design for either board area efficiency with the 7C269, or combine the 7C268 with other diagnostic products with the standard interface.

**CY7C268:** The 7C268 provides 13 address signals (A<sub>0</sub> through A<sub>12</sub>), 8 data out signals (O<sub>0</sub> through O<sub>7</sub>), ENA (enable), PCLK (pipeline clock) and INIT (initialize) for control. The full stan-

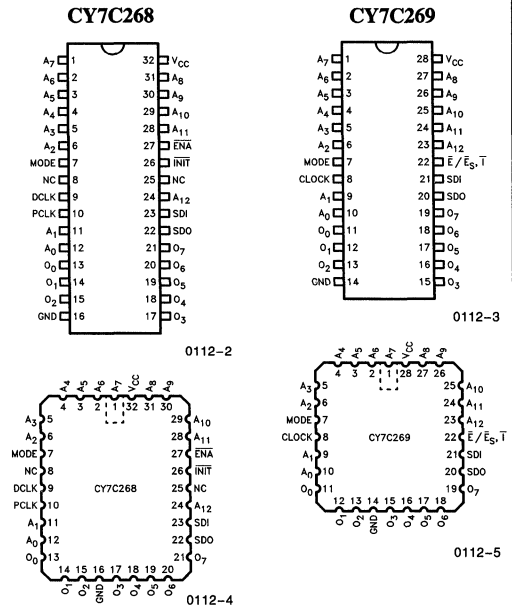
dard featured diagnostics of the 7C268 utilizes the SI and SO (shift in and shift out), MODE and DCLK signals. These signals allow serial data to be shifted into and out of the Diagnostic Shift Register at the same time the Pipeline Register is used for normal operation. The MODE signal is used to control the transfer of the information in the Diagnostic Register to the Pipeline Register or the data on the Output Bus into the Diagnostic Register. The data on the Output Bus may be provided from the Pipeline Register or an external source.

When the MODE signal is LOW, the PROM operates in a normal pipeline mode. The contents of the addressed memory location is loaded into the Pipeline Register on the rising edge of PCLK. The outputs are enabled with the ENA signal either synchronously or asynchronously, depending on how the device is configured when programmed. If programmed for asynchronous enable, ENA LOW enables

## Logic Block Diagram



## Pin Configurations



## Selection Guide

|                                |            | 7C268/9-40 | 7C268/9-50 | 7C268/9-60 |
|--------------------------------|------------|------------|------------|------------|
| Maximum Set-up Time (ns)       |            | 40         | 50         | 60         |
| Maximum Clock to Output (ns)   |            | 20         | 25         | 25         |
| Maximum Operating Current (mA) | Commercial | 100        | 80         | 80         |
|                                | Military   |            | 120        | 100        |

## Functional Description (Continued)

the outputs. If configured for synchronous enable,  $\overline{\text{ENA}}$  LOW during the rising edge of PCLK will enable the outputs synchronously with PCLK.  $\overline{\text{ENA}}$  HIGH during the rising edge of PCLK will synchronously disable the outputs. The asynchronous Initialize signal  $\overline{\text{INIT}}$  transfers the Initialize Byte into the Pipeline Register on a HIGH to LOW transition.  $\overline{\text{INIT}}$  LOW disables PCLK and needs to transition back to a HIGH in order to enable PCLK. DCLK shifts data into SI and out of SO on each rising edge.

When MODE is HIGH, the rising edge of the PCLK signal loads the Pipeline Register with the contents of the Diagnostic Register. Similarly, DCLK, in this mode, loads the Diagnostic Register with the information on the Data Output Pins. The information loaded will be either the contents of the Pipeline Register if the outputs are enabled, or data on the bus, if the outputs are disabled (in a high impedance state).

**CY7C269:** This product is optimized for applications that require diagnostics in a minimum amount of board area. Packaged in 28 pins, the PROM has 13 Address Signals ( $A_0$  through  $A_{12}$ ), 8 Data Out Signals ( $O_0$  through  $O_7$ ),  $\overline{\text{E/I}}$  (Enable or Initialize) and CLOCK (pipeline and diagnostic clock). Additional diagnostic signals consist of MODE, SI (shift in) and SO (shift out). Normal pipelined operation and Diagnostic operation are mutually exclusive.

When the MODE signal is LOW, the 7C269 operates in a normal pipelined mode. CLOCK functions as a pipeline clock, loading the contents of the addressed memory location into the Pipeline Register on each rising edge. The data will appear on the Outputs if they are enabled. One pin on the 7C269 is programmed to perform either the

Enable or the Initialize function. If the  $\overline{\text{E/I}}$  pin is used for a  $\overline{\text{INIT}}$  (Asynchronous Initialize) function, the outputs are permanently enabled and the Initialize Word is loaded into the Pipeline Register on a High to LOW transition of the  $\overline{\text{INIT}}$  signal. The  $\overline{\text{INIT}}$  LOW disables CLOCK and must return high to re-enable CLOCK. If the  $\overline{\text{E/I}}$  pin is used for an enable signal, it may be programmed for either synchronous or asynchronous operation. This enable function then operates exactly the same as the 7C268.

When the MODE signal is HIGH, the 7C269 operates in the diagnostic mode. The  $\overline{\text{E/I}}$  signal becomes a secondary mode signal designating whether to shift the Diagnostic Shift Register or to load either the Diagnostic Register or the Pipeline Register. If  $\overline{\text{E/I}}$  is HIGH, CLOCK performs the function of DCLK, shifting SI into the least significant location of the Diagnostic Register and all bits one location toward the most significant location on each rising edge. The contents of the most significant location in the Diagnostic Register are available on the SO pin.

If the  $\overline{\text{E/I}}$  signal is LOW, SI becomes a direction signal; transferring the contents of the Diagnostic Register into the Pipeline Register when SI is LOW. When SI is HIGH, the contents of the Output pins are transferred into the Diagnostic Register. Both transfers occur on a LOW to HIGH transition of the CLOCK. If the Outputs are enabled, the contents of the Pipeline Register are transferred into the Diagnostic Register. If the Outputs are disabled, an external source of data may be loaded into the Diagnostic Register. In this condition, the SO signal is internally driven to be the same as the SI signal thus propagating the "direction of transfer information" to the next device in the string.

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature .....                           | -65°C to +150°C |
| Ambient Temperature with Power Applied .....        | -55°C to +125°C |
| Supply Voltage to Ground Potential .....            | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State ..... | -0.5V to +7.0V  |
| DC Input Voltage .....                              | -3.0V to +7.0V  |
| DC Program Voltage .....                            | 13.0V           |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | >2001V<br>(per MIL-STD-883, Method 3015) |
| Latchup Current .....          | >200 mA                                  |
| UV Exposure .....              | 7258 Wsec/c                              |

### Operating Range

| Range       | Ambient Temperature | V <sub>CC</sub> |
|-------------|---------------------|-----------------|
| Commercial  | 0°C to 70°C         | 5V ± 10%        |
| Military[1] | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over the Operating Range[2]

| Parameters      | Description                              | Test Conditions  | Commercial |      | Military |      | Units |
|-----------------|--|--|------------|------|----------|------|-------|
|                 |  |  | Min.       | Max. | Min.     | Max. |       |
| V <sub>OH</sub> | Output HIGH Voltage                      | V <sub>CC</sub> = Min., I <sub>OH</sub> = -2 mA  | 2.4        |      | 2.4      |      | V     |
| V <sub>OL</sub> | Output LOW Voltage                       | V <sub>CC</sub> = Min., I <sub>OL</sub> = 12 mA<br>(I <sub>OL</sub> = 8 mA for Military) |            | 0.4  |          | 0.4  | V     |
| V <sub>IH</sub> | Input HIGH Voltage                       |  | 2.0        |      | 2.0      |      | V     |
| V <sub>IL</sub> | Input LOW Voltage                        |  |            | 0.8  |          | 0.8  | V     |
| I <sub>IX</sub> | Input Load Current                       | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>  |            | 10   |          | 10   | μA    |
| I <sub>OZ</sub> | Output Leakage Current                   | GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub><br>Output Disabled                              |            | 40   |          | 40   | μA    |
| I <sub>OS</sub> | Output Short Circuit Current             | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND   |            | 90   |          | 90   | mA    |
| I <sub>CC</sub> | V <sub>CC</sub> Operating Supply Current | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA  | 7C268/9-40 | 100  |          |      | mA    |
|                 |  |  | 7C268/9-50 | 80   |          | 120  |       |
|                 |  |  | 7C268/9-60 | 80   |          | 100  |       |

### Capacitance[3]

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 8    |       |

### Switching Characteristics Over the Operating Range[2]

| Parameters       | Description                                    | 7C268-40<br>7C269-40 |      | 7C268-50<br>7C269-50 |      | 7C268-60<br>7C269-60 |      | Units |
|------------------|--|----------------------|------|----------------------|------|----------------------|------|-------|
|                  |  | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. |       |
| t <sub>AS</sub>  | Address Set-Up to Clock                        | 40                   |      | 50                   |      | 60                   |      | ns    |
| t <sub>HA</sub>  | Address Hold from Clock                        | 0                    |      | 0                    |      | 0                    |      | ns    |
| t <sub>CO</sub>  | Clock to Output Valid                          |                      | 20   |                      | 25   |                      | 25   | ns    |
| t <sub>pw</sub>  | Clock Pulse Width                              | 15                   |      | 20                   |      | 20                   |      | ns    |
| t <sub>SES</sub> | $\bar{E}_S$ Set-Up to Clock (Sync Enable Only) | 15                   |      | 15                   |      | 15                   |      | ns    |
| t <sub>HES</sub> | $\bar{E}_S$ Hold from Clock                    | 5                    |      | 5                    |      | 5                    |      | ns    |
| t <sub>DI</sub>  | $\bar{INIT}$ to Out Valid                      |                      | 25   |                      | 35   |                      | 35   | ns    |
| t <sub>RI</sub>  | $\bar{INIT}$ Recovery to Clock                 | 20                   |      | 25                   |      | 25                   |      | ns    |

### Switching Characteristics Over the Operating Range<sup>[3]</sup> (Continued)

| Parameters | Description                                       | 7C268-40<br>7C269-40 |      | 7C268-50<br>7C269-50 |      | 7C268-60<br>7C269-60 |      | Units |
|------------|---|----------------------|------|----------------------|------|----------------------|------|-------|
|            |   | Min.                 | Max. | Min.                 | Max. | Min.                 | Max. |       |
| tpWI       | Init Pulse Width                                  | 25                   |      | 35                   |      | 35                   |      | ns    |
| tCOS       | Output Valid from Clock (Sync. Mode)              |                      | 20   |                      | 25   |                      | 25   | ns    |
| tHZC       | Output Inactive from Clock (Sync. Mode)           |                      | 20   |                      | 25   |                      | 25   | ns    |
| tDOE       | Output Valid from $\bar{E}$ Low (Async. Mode)     |                      | 20   |                      | 25   |                      | 25   | ns    |
| tHZE       | Output Inactive from $\bar{E}$ High (Async. Mode) |                      | 20   |                      | 25   |                      | 25   | ns    |

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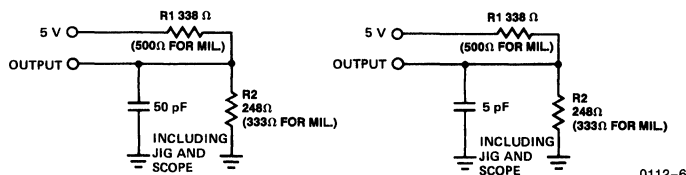
### Diagnostic Mode Switching Characteristics Over the Operating Range<sup>[2]</sup>

| Parameters | Description                   | Commercial |      | Military |      | Units |
|------------|-------------------------------|------------|------|----------|------|-------|
|            |                               | Min.       | Max. | Min.     | Max. |       |
| tSSDI      | Set-Up SDI to Clock           | 30         |      | 35       |      | ns    |
| tHSDI      | SDI Hold from Clock           | 0          |      | 0        |      | ns    |
| tDSDO      | SDO Delay from Clock          |            | 30   |          | 40   | ns    |
| tDCL       | Minimum Clock Low             | 25         |      | 25       |      | ns    |
| tDCH       | Minimum Clock High            | 25         |      | 25       |      | ns    |
| tSM        | Set-Up to Mode Change         | 25         |      | 30       |      | ns    |
| tHM        | Hold from Mode Change (7C269) | 0          |      | 0        |      | ns    |
| tMS        | Mode to SDO                   |            | 25   |          | 30   | ns    |
| tSS        | SDI to SDO                    |            | 40   |          | 45   | ns    |
| tSO        | Data Set-Up to DCLK           | 25         |      | 30       |      | ns    |
| tHO        | Data Hold from DCLK           | 10         |      | 15       |      | ns    |

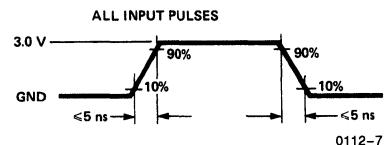
**Notes:**

1. T<sub>A</sub> is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Tested initially and after any design or process changes that may affect these parameters.

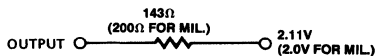
### AC Test Loads and Waveforms



0112-6



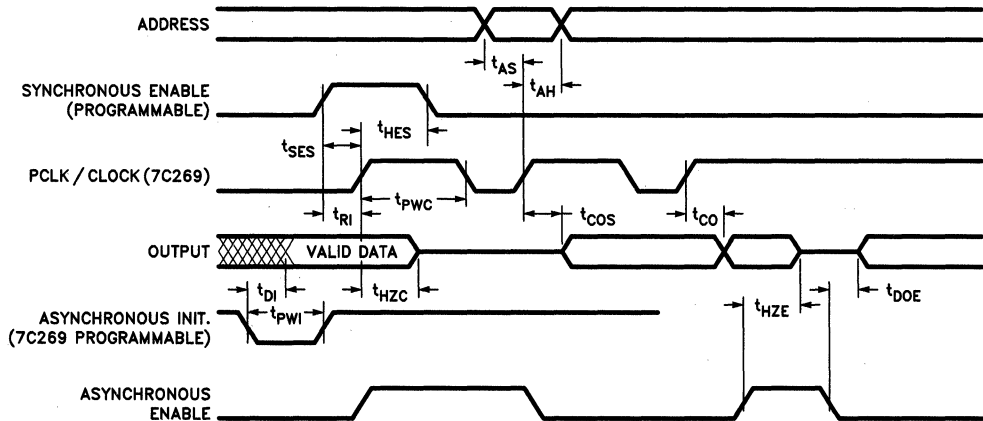
0112-7



0112-8

## Switching Waveforms 7C268, 7C269

Pipeline Operation (Mode = 0)



0112-9

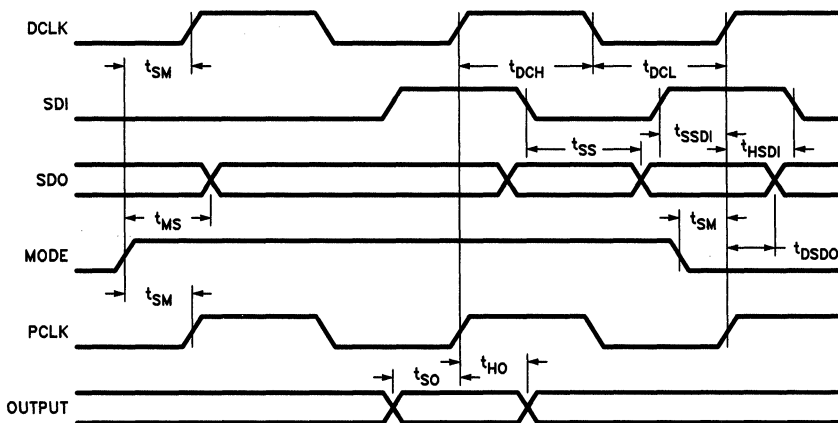
### Notes on Testing:

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device  $V_{CC}$  and ground terminals. Multiple capacitors are recommended, including a 0.1  $\mu\text{F}$  or larger capacitor and a 0.01  $\mu\text{F}$  or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.

3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level - 500 mV or steady state LOW level + 500 mV on the output from the 1.5V level on inputs with load shown in Figure 1b.

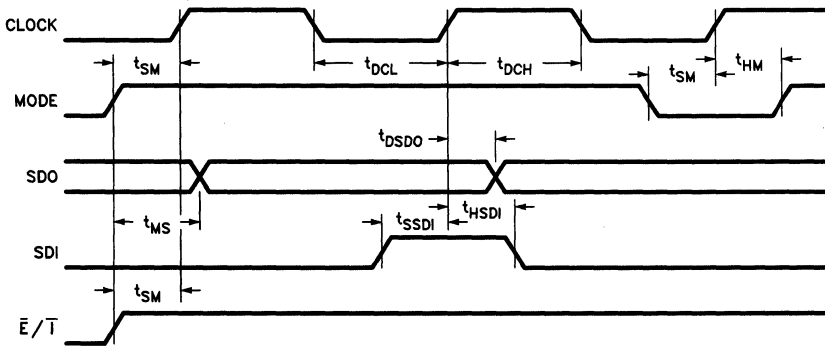
### 7C268 Diagnostic Waveforms



0112-10

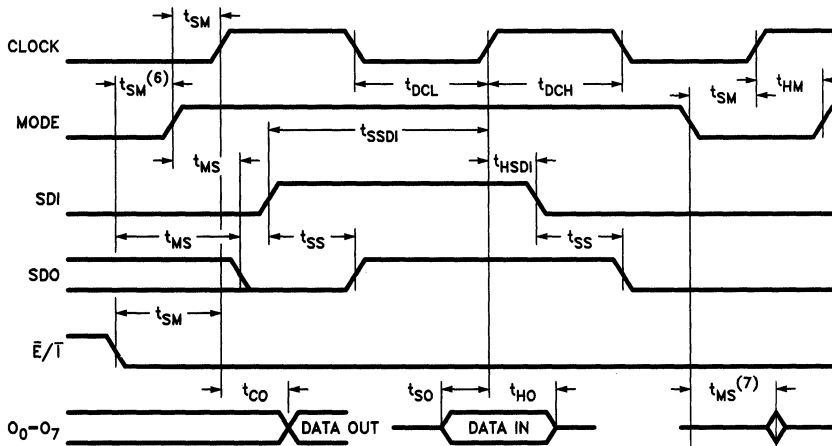
## Switching Waveforms (Continued)

### 7C269 Diagnostic Application (Shifting the Shadow Register)



0112-11

### 7C269 Diagnostic Application (Parallel Data Transfer)



0112-12

#### Notes:

6. Asynchronous enable mode only.

7. The mode transition to HIGH latches the asynchronous enable state. If the enable state is changed and held before leaving the diagnostic mode (mode H → L) then the output impedance change delay is  $t_{MS}$ .

## Device Programming

The CY7C268 and CY7C269 program identically. They utilize an intelligent programming algorithm to assure consistent programming quality. These 64K PROMS use a single ended memory cell design. In an unprogrammed state, the memory contains all "0"s. During programming, a "1" on a data-in pin causes the addressed location to be programmed, and a "0" causes the location to remain unprogrammed.

## Programming Pinout

The Programming Pinout of both devices is shown in *Figures 3a and 3b*. The programming mode is entered by putting 12.5V on the  $V_{pp}$  pin. The addressed location is programmed and verified with the application of a PGM and VFY pulse. Entering and exiting the programming mode should be done with care. Proper sequencing as described in the dialog on the programming algorithm and shown in the timing diagram and programming flow chart must be implemented.



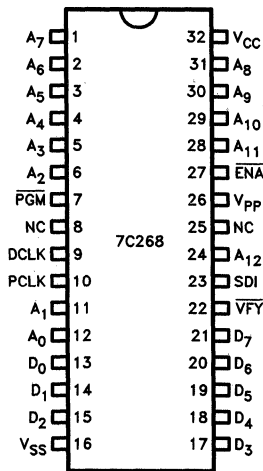


Figure 3a. 7C268 Programming Pinout

0112-13

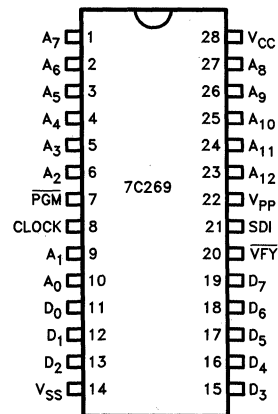


Figure 3b. 7C269 Programming Pinout

0112-14

## Programming and Blankcheck (Memory Bits)

### Blankcheck

Blankcheck is accomplished by performing a verify cycle (VFY toggles on each address), sequencing through all memory address locations, where all the data read will be "0"s. (Refer to mode table for pin states)

### Programming Algorithm

Programming is accomplished with an intelligent algorithm. The sequence of operations is to enter the programming mode by placing 12.5V on Vpp. This should be done after a minimum delay from power up, and be removed prior to power down by the same delay (see the timing diagram and AC specifications for details). Once in this mode, programming is accomplished by addressing a location as described above, placing the data to be programmed into a location on the data pins, and clocking the PGM signal from VIH to VIL and back to VIH with a pulse width of 200  $\mu$ s. The data is removed from the data pins and the content of the location is then verified by taking the VFY signal from VIH to VIL, comparing the output with the desired data and then returning VFY to VIH. If the contents are correct, a second overprogram pulse of 4 times the original 200  $\mu$ s is delivered with the data to be programmed again on the data pins. If the data is not correct, a second 200  $\mu$ s pulse is applied to PGM with the data to be programmed on the data pins. The compare and overprogram operation is repeated with an overprogram pulse width 4 times the sum of the initial program pulses. This operation is continued until the location is programmed or 10 initial program pulses have been attempted. If on the 10th attempt, the location fails to verify, an overprogram pulse of 8 ms is applied, and the content of the location is once more verified. If the location still fails to verify, the device is rejected. Once a location verifies successfully, the address is advanced to the next location, and the process is repeated until all locations are programmed.

After all locations are programmed, they should be verified at VCCP = 5.0V.

### Programming Algorithm for the Architecture

Both the 7C268 and 7C269 offer a limited selection of programmed architecture. Programming these features should be done with a single 10 ms wide pulse in place of the intelligent algorithm mainly because these features are verified operationally, not with the VFY pin. Architecture programming is implemented by applying the supervoltage to two additional pins during programming. In programming the 7C269 architecture Vpp is applied to pins 3, 9 and 22 while in programming the 7C268 architecture Vpp is applied to pins 3, 11, 26. Specific choice of a particular mode will depend on the states of the other pins during programming so it is important that the condition of the other pins be met as set forth in the mode table. The same considerations with respect to power up and power down apply during architecture programming as during intelligent programming. Once the supervoltages have been established and the correct logic states exist on the other device pins, programming may begin. Programming is accomplished by pulling PGM from HIGH to LOW and then back to HIGH with a pulse width equal to 10 ms.

To check whether a 7C269 has been programmed as output enable or initialize enable, pin 22 ( $\bar{E}/\bar{I}$ ) should be pulled LOW followed by a LOW to HIGH transition on pin 8 (CLOCK). The data read at the outputs is stored and complement data is shifted into the shadow register. A shift from shadow to pipeline is performed and the CLOCK is again pulled from LOW to HIGH. At this point, if the new data read is data-complement, the device has been programmed as Output enable while if the new data read-true then the device is programmed as Initialize enable and the configuration of the Initialize byte can be read directly by pulling  $\bar{E}/\bar{I}$  from HIGH to LOW.

Mode Table 7C268

| Mode Select                         | P2<br>A6 | P3<br>A5        | P30<br>A9 | P6<br>A2 | P7<br>MD<br>PGM | P9<br>DCLK | P10<br>PCLK | P11<br>A1       | P12<br>A0 | P22<br>SDO<br>VFY | P23<br>SDI | P24<br>A12 | P26<br>INT<br>VPP | P27<br>E/Es | P28<br>A11 |
|-------------------------------------|----------|-----------------|-----------|----------|-----------------|------------|-------------|-----------------|-----------|-------------------|------------|------------|-------------------|-------------|------------|
| Normal Read <sup>[2]</sup>          | A6       | A5              | A9        | A2       | L               | X          | L/H         | A1              | A0        | SDO               | X          | A12        | H                 | H/L         | A11        |
| Load SR to PR <sup>[2]</sup>        | A6       | A5              | A9        | A2       | H               | L          | L/H         | A1              | A0        | SDI               | X          | A12        | H                 | X           | A11        |
| Load Output to SR                   | A6       | A5              | A9        | A2       | H               | L/H        | L           | A1              | A0        | SDI               | L          | A12        | H                 | H           | A11        |
| Shift Shadow <sup>[2]</sup>         | A6       | A5              | A9        | A2       | L               | L/H        | L           | A1              | A0        | SDO               | DIN        | A12        | H                 | X           | A11        |
| Program (Memory)                    | A6       | A5              | A9        | A2       | L               | L          | L           | A1              | A0        | H                 | L          | A12        | V <sub>PP</sub>   | H           | A11        |
| Program Verify                      | A6       | A5              | A9        | A2       | H               | L          | L           | A1              | A0        | L                 | L          | A12        | V <sub>PP</sub>   | H           | A11        |
| Program Inhibit                     | A6       | A5              | A9        | A2       | H               | L          | L           | A1              | A0        | H                 | L          | A12        | V <sub>PP</sub>   | H           | A11        |
| Async. Enable Read                  | A6       | A5              | A9        | A2       | L               | L          | X           | A1              | A0        | SDO               | L          | A12        | H                 | H/L         | A11        |
| Sync. Enable Read                   | A6       | A5              | A9        | A2       | L               | L          | L/H         | A1              | A0        | SDO               | L          | A12        | H                 | H/L         | A11        |
| Async. Init. Read                   | A6       | A5              | A9        | A2       | L               | L          | X           | A1              | A0        | SDO               | L          | A12        | L                 | L           | A11        |
| Program Sync. Enable <sup>[1]</sup> | H        | V <sub>HH</sub> | X         | H        | L               | L          | L           | V <sub>HH</sub> | L         | H                 | L          | H          | V <sub>PP</sub>   | H           | H          |
| Program Initial Byte                | H        | V <sub>HH</sub> | X         | L        | L               | L          | L           | V <sub>HH</sub> | H         | H                 | L          | X          | V <sub>PP</sub>   | H           | L          |

Notes:

1. Default is Async. Enable.
2. For the asynchronous enable operation, the data out is enabled by bringing E LOW. For the synchronous enable operation, data out is enabled on the first LOW to HIGH clock transition after E is brought

LOW. When E goes from LOW to HIGH (enable to disable) the outputs will go to the high impedance state (after a propagation delay) immediately if the asynchronous enable was programmed. If the synchronous enable was selected, a LOW to HIGH clock transition is required.

Mode Table 7C269

| Mode Select                         | P2<br>A6 | P3<br>A5        | P26<br>A9 | P6<br>A2 | P7<br>MD<br>PGM | P8<br>CLK | P9<br>A1        | P10<br>A0 | P21<br>SDI | P20<br>SDO<br>VFY | P24<br>A11 | P22<br>E/I<br>VPP | P23<br>A12 |
|-------------------------------------|----------|-----------------|-----------|----------|-----------------|-----------|-----------------|-----------|------------|-------------------|------------|-------------------|------------|
| Normal Read                         | A6       | A5              | A9        | A2       | L               | L/H       | A1              | A0        | X          | HI Z              | A11        | H/L               | A12        |
| Load SR to PR <sup>[3]</sup>        | A6       | A5              | A9        | A2       | H               | L/H       | A1              | A0        | L          | SDI               | A11        | L                 | A12        |
| Load Output to SR <sup>[3]</sup>    | A6       | A5              | A9        | A2       | H               | L/H       | A1              | A0        | H          | SDI               | A11        | L                 | A12        |
| Shift Shadow <sup>[3]</sup>         | A6       | A5              | A9        | A2       | H               | L/H       | A1              | A0        | DIN        | SDO               | A11        | H                 | A12        |
| Program (Memory)                    | A6       | A5              | A9        | A2       | L               | L         | A1              | A0        | X          | H                 | A11        | V <sub>PP</sub>   | A12        |
| Program Verify                      | A6       | A5              | A9        | A2       | H               | L         | A1              | A0        | X          | L                 | A11        | V <sub>PP</sub>   | A12        |
| Program Inhibit                     | A6       | A5              | A9        | A2       | H               | L         | A1              | A0        | X          | H                 | A11        | V <sub>PP</sub>   | A12        |
| Async. Enable Read                  | A6       | A5              | A9        | A2       | L               | L         | A1              | A0        | X          | HI Z              | A11        | L                 | A12        |
| Sync. Enable Read                   | A6       | A5              | A9        | A2       | L               | L/H       | A1              | A0        | X          | HI Z              | A11        | L                 | A12        |
| Async. Init. Read                   | A6       | A5              | A9        | A2       | L               | L         | A1              | A0        | X          | HI Z              | A11        | L                 | A12        |
| Program Sync. Enable <sup>[1]</sup> | H        | V <sub>HH</sub> | A9        | H        | L               | L         | V <sub>HH</sub> | L         | X          | H                 | H          | V <sub>PP</sub>   | H          |
| Program Initialize <sup>[2]</sup>   | H        | V <sub>HH</sub> | A9        | L        | L               | L         | V <sub>HH</sub> | L         | X          | H                 | H          | V <sub>PP</sub>   | L          |
| Program Initial Byte                | H        | V <sub>HH</sub> | A9        | L        | L               | L         | V <sub>HH</sub> | H         | X          | H                 | L          | V <sub>PP</sub>   | A12        |

Notes:

1. Default is Async. Enable.
2. Default is Enable.
3. If I selected, outputs always enabled. If E selected, during diagnostic operation the data outputs will remain in the state they were in when the mode was entered. When enabled, the data outputs will reflect the outputs of the pipeline register. Any changes in the data in the pipeline register will appear on the data output pins.

**DC Programming Parameters**  $T_A = 25^\circ\text{C}$ 

| Parameter        | Description                             | Min. | Max. | Units |
|------------------|---|------|------|-------|
| V <sub>PP</sub>  | Programming Voltage                     | 12.0 | 13.0 | V     |
| V <sub>CCP</sub> | Power Supply Voltage During Programming | 4.75 | 5.25 | V     |
| I <sub>PP</sub>  | V <sub>PP</sub> Supply Current          |      | 50   | mA    |
| V <sub>IHP</sub> | Input High Voltage During Programming   | 3.0  |      | V     |
| V <sub>ILP</sub> | Input Low Voltage During Programming    | -3.0 | 0.4  | V     |
| V <sub>OH</sub>  | Output High Voltage                     | 2.4  |      | V     |
| V <sub>OL</sub>  | Output Low Voltage                      |      | 0.4  | V     |

**AC Programming Parameters**  $T_A = 25^\circ\text{C}$ 

| Parameter        | Description                        | Min. | Max. | Units |
|------------------|------------------------------------|------|------|-------|
| t <sub>pp</sub>  | Program Pulse Width (Per Byte)     |      | 10.0 | ms    |
| t <sub>AS</sub>  | Address Set-up Time                | 1.0  |      | μs    |
| t <sub>AH</sub>  | Address Hold Time                  | 1.0  |      | μs    |
| t <sub>DH</sub>  | Data Hold Time                     | 1.0  |      | μs    |
| t <sub>DS</sub>  | Data Set-up Time                   | 1.0  |      | μs    |
| t <sub>R,F</sub> | V <sub>PP</sub> Rise and Fall Time | 1.0  |      | μs    |
| t <sub>DV</sub>  | Delay to Verify                    | 1.0  |      | μs    |
| t <sub>VD</sub>  | Verify to Data Out                 |      | 1.0  | μs    |
| t <sub>VH</sub>  | Data Hold Time from Verify         |      | 1.0  | μs    |
| t <sub>VP</sub>  | Verify Pulse Width                 | 2.0  |      | μs    |
| t <sub>DZ</sub>  | Verify to High Z                   |      | 1.0  | μs    |

**Erase Characteristics**

Wavelengths of light less than 4000 Angstroms begin to erase the 7C268 and 7C269 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV

intensity  $\times$  exposure time) or 25 Wsec/cm<sup>2</sup>. For an ultraviolet lamp with a 12 mW/cm<sup>2</sup> power rating the exposure time would be approximately 45 minutes. The 7C268 or 7C269 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm<sup>2</sup> is the recommended maximum dosage.

**Bit Map Data**

| Programmer Address |      | RAM Data     |
|--------------------|------|--------------|
| Decimal            | Hex  | Contents     |
| 0                  | 0    | DATA         |
| •                  | •    | •            |
| •                  | •    | •            |
| •                  | •    | •            |
| 8191               | 1FFF | DATA         |
| 8192               | 2000 | INIT BYTE    |
| 8193               | 2001 | CONTROL BYTE |

**Control Byte**

- 00 Asynchronous output enable (default condition)
- 01 Synchronous output enable
- 02 Asynchronous initialize (CY7C269 only)

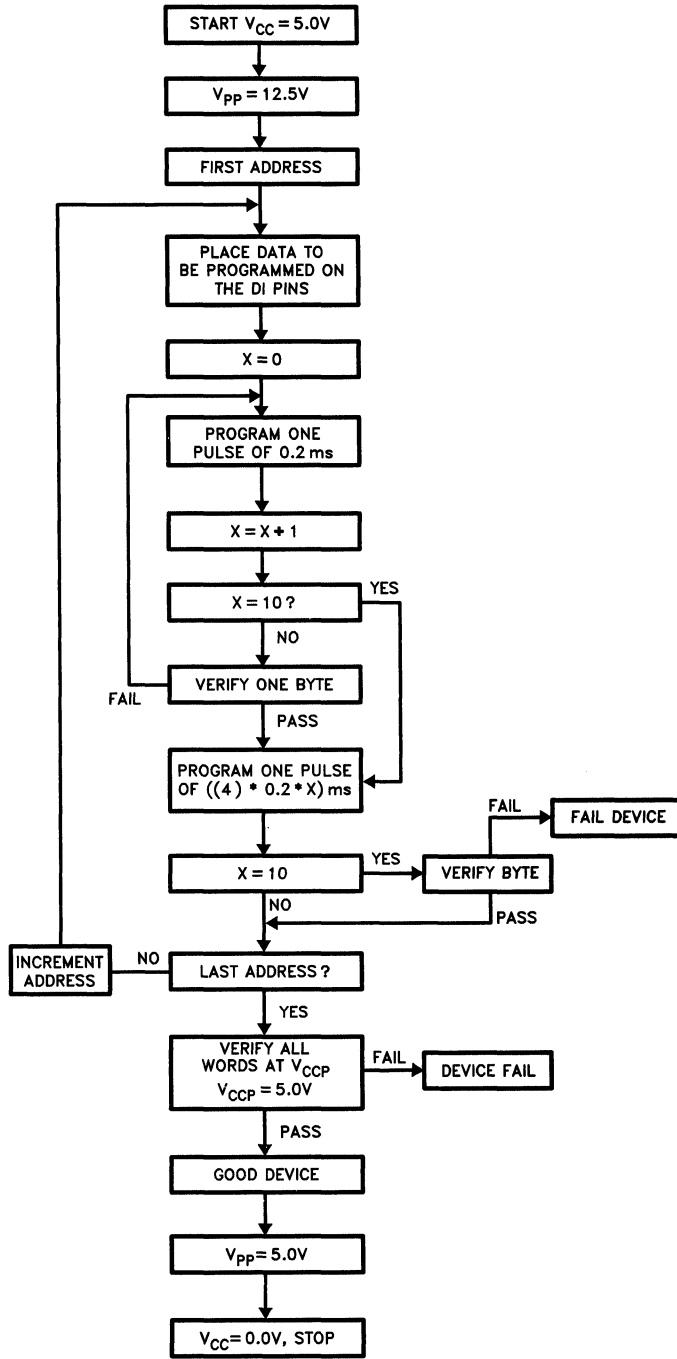


Figure 4. Programming Flowchart

0112-15

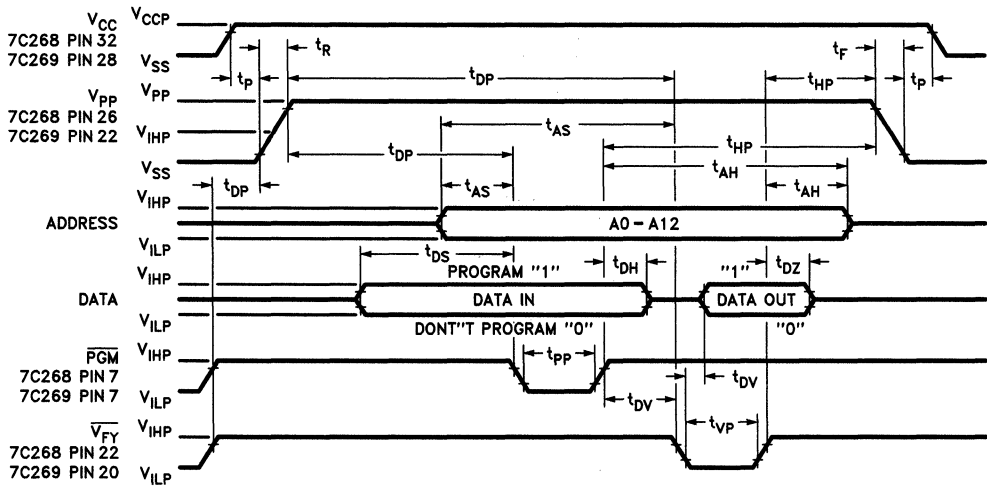
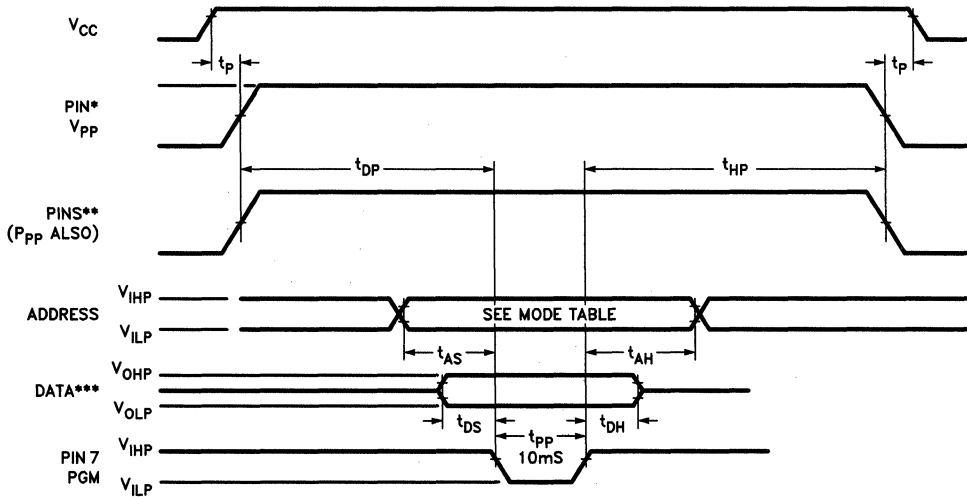


Figure 5. Programming Waveforms (Memory)

0112-16

Note:

Power, Vpp and VCC should not be cycled for each program verify cycle but remain static during programming.



\*7C268-pin 26  
7C269-pin 22

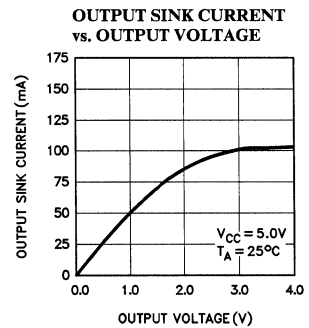
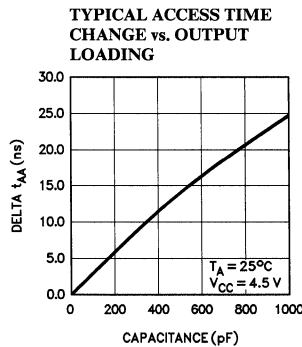
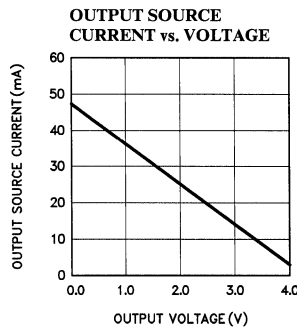
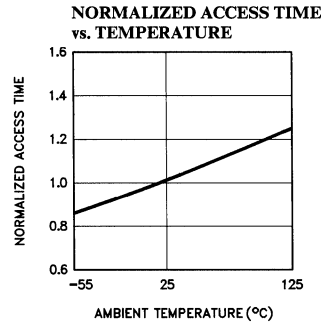
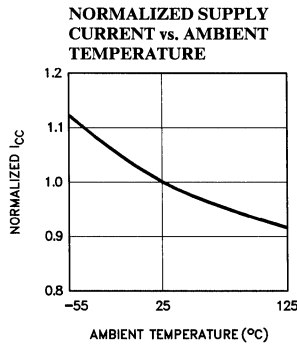
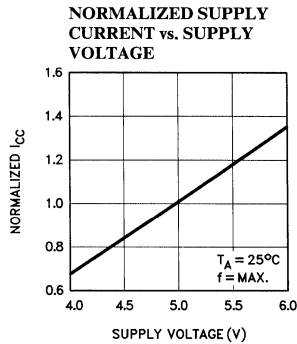
\*\*7C268-pins 3, 11  
7C269-pins 3, 9

\*\*\*Data required on I/O's only during initial byte programming

Figure 6. Programming Waveforms for the Architecture CY7C268 and CY7C269

0112-17

## Typical DC and AC Characteristics



0112-18

## Ordering Information

| Speed (ns) | $I_{CC}$ (mA) | Ordering Code | Package Type  | Operating Range |          |
|------------|---------------|---------------|---------------|-----------------|----------|
| 40         | 100           | CY7C268-40DC  | D20           | Commercial      |          |
|            |               | CY7C268-40WC  | W20           |                 |          |
|            |               | CY7C269-40PC  | P21           |                 |          |
|            |               | CY7C269-40DC  | D22           |                 |          |
|            |               | CY7C269-40WC  | W22           |                 |          |
| 50         | 80            | CY7C268-50DC  | D20           | Commercial      |          |
|            |               | CY7C268-50WC  | W20           |                 |          |
|            |               | CY7C269-50PC  | P21           |                 |          |
|            |               | CY7C269-50DC  | D22           |                 |          |
|            |               | CY7C269-50WC  | W22           |                 |          |
|            | 120           | 80            | CY7C268-50DMB | D20             | Military |
|            |               |               | CY7C268-50WMB | W20             |          |
|            |               |               | CY7C268-50LMB | L55             |          |
|            |               |               | CY7C268-50QMB | Q55             |          |
|            |               |               | CY7C269-50DMB | D22             |          |
| 120        | 120           | CY7C269-50WMB | W22           | Military        |          |
|            |               | CY7C269-50LMB | L64           |                 |          |
|            |               | CY7C269-50QMB | Q64           |                 |          |

| Speed (ns)    | $I_{CC}$ (mA) | Ordering Code | Package Type | Operating Range |
|---------------|---------------|---------------|--------------|-----------------|
| 60            | 80            | CY7C268-60DC  | D20          | Commercial      |
|               |               | CY7C268-60WC  | W20          |                 |
|               |               | CY7C269-60PC  | P21          |                 |
|               |               | CY7C269-60DC  | D22          |                 |
|               |               | CY7C269-60WC  | W22          |                 |
|               |               | 100           | 100          |                 |
| CY7C268-60WMB | W20           |               |              |                 |
| CY7C268-60LMB | L55           |               |              |                 |
| CY7C268-60QMB | Q55           |               |              |                 |
| CY7C269-60DMB | D22           |               |              |                 |
| CY7C269-60WMB | W22           |               |              |                 |
| 100           | 100           | CY7C269-60LMB | L64          | Military        |
|               |               | CY7C269-60QMB | Q64          |                 |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters      | Subgroups |
|-----------------|-----------|
| V <sub>OH</sub> | 1,2,3     |
| V <sub>OL</sub> | 1,2,3     |
| V <sub>IH</sub> | 1,2,3     |
| V <sub>IL</sub> | 1,2,3     |
| I <sub>IX</sub> | 1,2,3     |
| I <sub>OZ</sub> | 1,2,3     |
| I <sub>CC</sub> | 1,2,3     |
| I <sub>SB</sub> | 1,2,3     |

#### Switching Characteristics

| Parameters       | Subgroups   |
|------------------|-------------|
| t <sub>AS</sub>  | 7,8,9,10,11 |
| t <sub>HA</sub>  | 7,8,9,10,11 |
| t <sub>CO</sub>  | 7,8,9,10,11 |
| t <sub>pw</sub>  | 7,8,9,10,11 |
| t <sub>SES</sub> | 7,8,9,10,11 |
| t <sub>HES</sub> | 7,8,9,10,11 |
| t <sub>COS</sub> | 7,8,9,10,11 |

#### Diagnostic Mode Switching Characteristics

| Parameters                     | Subgroups   |
|--------------------------------|-------------|
| t <sub>SSDI</sub>              | 7,8,9,10,11 |
| t <sub>HSDI</sub>              | 7,8,9,10,11 |
| t <sub>DSDO</sub>              | 7,8,9,10,11 |
| t <sub>DCL</sub>               | 7,8,9,10,11 |
| t <sub>DCH</sub>               | 7,8,9,10,11 |
| t <sub>HM</sub> <sup>[1]</sup> | 7,8,9,10,11 |
| t <sub>MS</sub>                | 7,8,9,10,11 |
| t <sub>SS</sub>                | 7,8,9,10,11 |

**Note:**

1. 7C269 only.

Document #: 38-00069-A



## 32,768 x 8 PROM Power Switched and Reprogrammable

### Features

- CMOS for optimum speed/power
- Windowed for reprogrammability
- High speed
  - 45 ns (commercial)
  - 55 ns (military)
- Low power
  - 660 mW (commercial)
  - 715 mW (military)
- Super low standby power
  - Less than 165 mW when deselected
- EPROM technology  
100% programmable
- 5V ±10% V<sub>CC</sub>, commercial and military
- TTL compatible I/O
- Slim 300 mil package (7C271)
- Direct replacement for bipolar PROMs

- Capable of withstanding > 2001V static discharge

### Product Characteristics

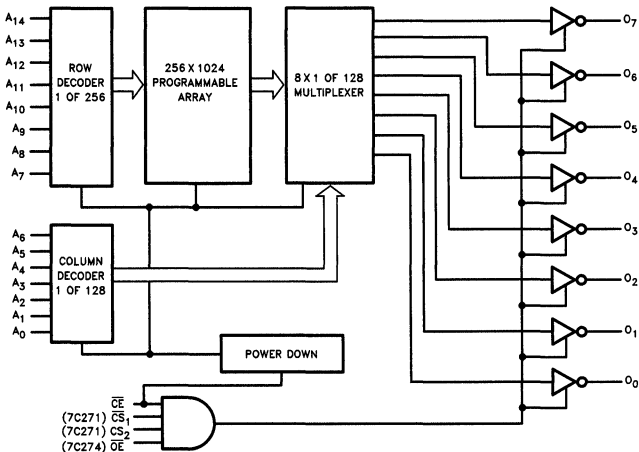
The CY7C271 and CY7C274 are high performance 32,768 word by 8 bit CMOS PROMS. When disabled ( $\overline{CE}$  HIGH), the 7C271/274 automatically powers down into a low power standby mode. The CY7C271 is packaged in the 300 mil slim package. The CY7C274 is packaged in the industry standard 600 mil package. Both the 7C271 and 7C274 are available in a CERDIP package equipped with an erasure window to provide for reprogrammability. When exposed to UV light, the PROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C271 and CY7C274 offer the advantage of lower power, superior

performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested, with each location being written into, erased and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading the 7C271 is accomplished by placing active LOW signals on  $\overline{CS}_1$  and  $\overline{CE}$ , and an active HIGH on  $CS_2$ . Reading the 7C274 is accomplished by placing active LOW signals on  $\overline{OE}$  and  $\overline{CE}$ . The contents of the memory location addressed by the address lines ( $A_0$ – $A_{14}$ ) will become available on the output lines ( $O_0$ – $O_7$ ).

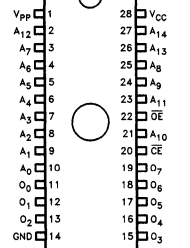
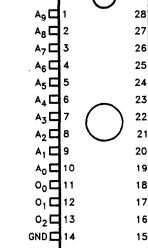
### Logic Block Diagram



### Pin Configurations

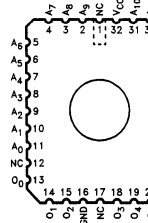
CY7C271

CY7C274

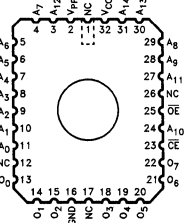


0102-2

0102-10



0102-3



0102-11



## Selection Guide

|                                |            | 7C271-45<br>7C274-45 | 7C271-55<br>7C274-55 |
|--------------------------------|------------|----------------------|----------------------|
| Maximum Access Time (ns)       |            | 45                   | 55                   |
| Maximum Operating Current (mA) | Commercial | 120                  | 120                  |
|                                | Military   |                      | 130                  |
| Standby Current (mA)           | Commercial | 30                   | 30                   |
|                                | Military   |                      | 40                   |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential .... -0.5V to +7.0V

DC Voltage Applied to Outputs  
in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

DC Program Voltage ..... 13.0V

Static Discharge Voltage ..... > 2001V  
(per MIL-STD-883, Method 3015)

Latchup Current ..... > 200 mA

UV Exposure ..... 7258 Wsec/cm<sup>2</sup>

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[4]</sup> | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over the Operating Range<sup>[5]</sup>

| Parameters      | Description                                 | Test Conditions  | 7C271-45<br>7C274-45 |                 | 7C271-55<br>7C274-55 |                 | Units |
|-----------------|---|--|----------------------|-----------------|----------------------|-----------------|-------|
|                 |   |  | Min.                 | Max.            | Min.                 | Max.            |       |
| V <sub>OH</sub> | Output HIGH Voltage                         | V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA                              | 2.4                  |                 | 2.4                  |                 | V     |
| V <sub>OL</sub> | Output LOW Voltage                          | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA*                              |                      | 0.4             |                      | 0.4             | V     |
| V <sub>IH</sub> | Input HIGH Level <sup>[1]</sup>             |  | 2.0                  | V <sub>CC</sub> | 2.0                  | V <sub>CC</sub> | V     |
| V <sub>IL</sub> | Input LOW Level <sup>[1]</sup>              |  |                      | 0.8             |                      | 0.8             | V     |
| I <sub>IX</sub> | Input Current                               | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>  | -10                  | +10             | -10                  | +10             | μA    |
| V <sub>CD</sub> | Input Diode Clamp Voltage                   |  | Note 2               |                 | Note 2               |                 |       |
| I <sub>OZ</sub> | Output Leakage Current                      | V <sub>OL</sub> ≤ V <sub>OUT</sub> ≤ V <sub>OH</sub> ,<br>Output Disabled      | -40                  | +40             | -40                  | +40             | μA    |
| I <sub>OS</sub> | Output Short Circuit Current <sup>[3]</sup> | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND                                 | -20                  | -90             | -20                  | -90             | mA    |
| I <sub>CC</sub> | Power Supply Current                        | V <sub>CC</sub> = Max., V <sub>IN</sub> = 2.0V<br>I <sub>OUT</sub> = 0 mA      | Commercial           | 120             | 120                  |                 | mA    |
|                 |   |  | Military             |                 |                      | 130             | mA    |
| I <sub>SB</sub> | Standby Supply Current                      | V <sub>CC</sub> = Max., $\overline{CS} \geq V_{IH}$<br>I <sub>OUT</sub> = 0 mA | Commercial           | 30              | 30                   |                 | mA    |
|                 |   |  | Military             |                 |                      | 40              | mA    |

\*6.0 mA military

## Capacitance<sup>[6]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 8    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 8    |       |

### Notes:

- These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
- The CMOS process does not provide a clamp diode. However, the CY7C271 and CY7C274 are insensitive to -3V dc input levels and -5V undershoot pulses of less than 10 ns (measured at 50% point).
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.

## Switching Characteristics Over the Operating Range<sup>[5, 7]</sup>

| Parameters        | Description   | 7C271-45<br>7C274-45 |      | 7C271-55<br>7C274-55 |      | Units |
|-------------------|---|----------------------|------|----------------------|------|-------|
|                   |   | Min.                 | Max. | Min.                 | Max. |       |
| t <sub>AA</sub>   | Address to Output Valid   |                      | 45   |                      | 55   | ns    |
| t <sub>HZCS</sub> | Chip Select Inactive to High Z <sup>[8]</sup> ( $\overline{CS}_1$ and $CS_2$ —7C271 Only) |                      | 30   |                      | 30   | ns    |
| t <sub>ACS</sub>  | Chip Select Active to Output Valid ( $\overline{CS}_1$ and $CS_2$ —7C271 Only)            |                      | 30   |                      | 30   | ns    |
| t <sub>HZOE</sub> | Output Enable Inactive to High Z <sup>[8]</sup> ( $\overline{OE}$ —7C274 Only)            |                      | 25   |                      | 30   | ns    |
| t <sub>OE</sub>   | Output Enable Active to Output Valid ( $\overline{OE}$ —7C274 Only)                       |                      | 25   |                      | 30   | ns    |
| t <sub>HZCE</sub> | Chip Enable Inactive to High Z <sup>[8]</sup> ( $\overline{CE}$ Only)                     |                      | 50   |                      | 60   | ns    |
| t <sub>ACE</sub>  | Chip Enable Active to Output Valid ( $\overline{CE}$ Only)                                |                      | 50   |                      | 60   | ns    |
| t <sub>PU</sub>   | Chip Enable Active to Power Up  | 0                    |      | 0                    |      | ns    |
| t <sub>PD</sub>   | Chip Enable Inactive to Power Down  |                      | 50   |                      | 60   | ns    |
| t <sub>OH</sub>   | Output Hold from Address Change   | 0                    |      | 0                    |      | ns    |

3

## AC Test Loads and Waveforms

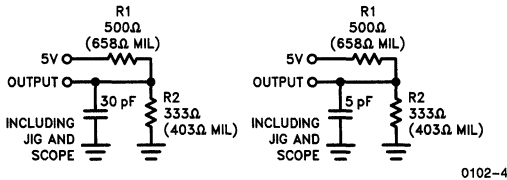


Figure 1a

Figure 1b

Equivalent to: THÉVENIN EQUIVALENT

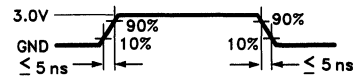
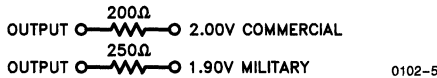
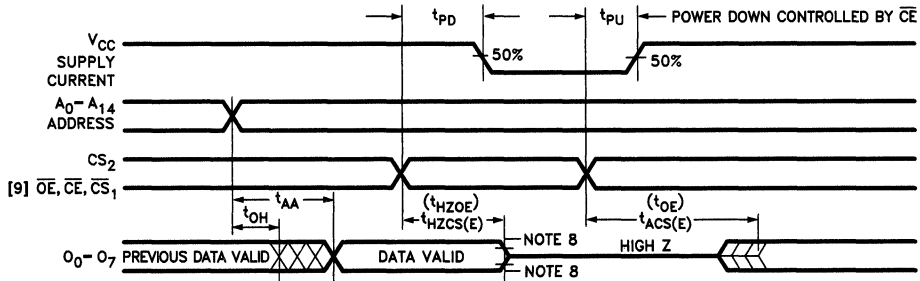


Figure 2. Input Pulses

0102-6



0102-7

### Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and loads shown in Figure 1a, 1b.
- t<sub>HZCS(E)</sub> and t<sub>HZOE</sub> are tested with the load shown in Figure 1b. Transition is measured at steady state High level +500 mV or steady

state Low level +500 mV on the output from the 1.5 level on the input.

- CS<sub>2</sub> and  $\overline{CS}_1$  are used on the 7C271 only.  $\overline{OE}$  is used on the 7C274 only.

## Erasure Characteristics

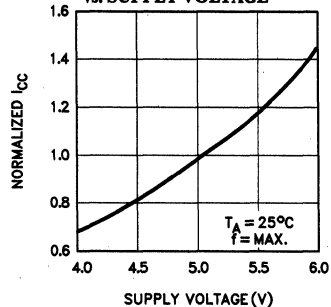
Wavelengths of light less than 4000 Angstroms begin to erase the 7C271 and 7C274 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV

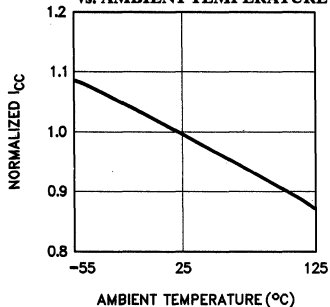
intensity × exposure time) or 25 Wsec/cm<sup>2</sup>. For an ultraviolet lamp with a 12 mW/cm<sup>2</sup> power rating the exposure time would be approximately 45 minutes. The 7C271 and 7C274 need to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258W × sec/cm<sup>2</sup> is the recommended maximum dosage.

## Typical DC and AC Characteristics

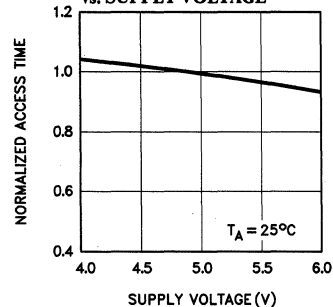
**NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE**



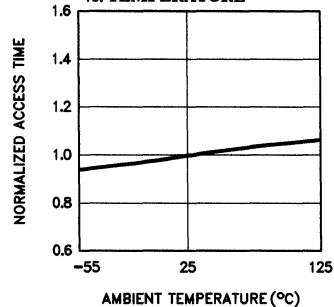
**NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE**



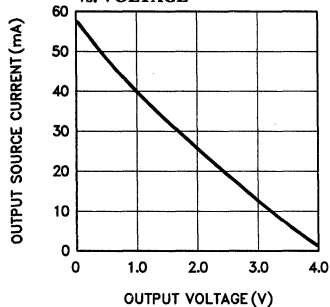
**NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE**



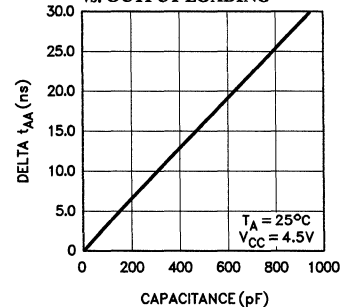
**NORMALIZED ACCESS TIME vs. TEMPERATURE**



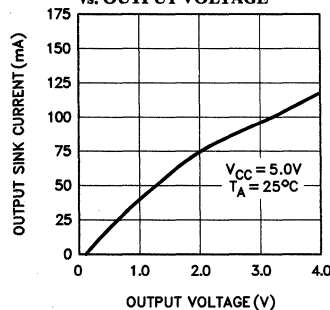
**OUTPUT SOURCE CURRENT vs. VOLTAGE**



**TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING**



**OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE**



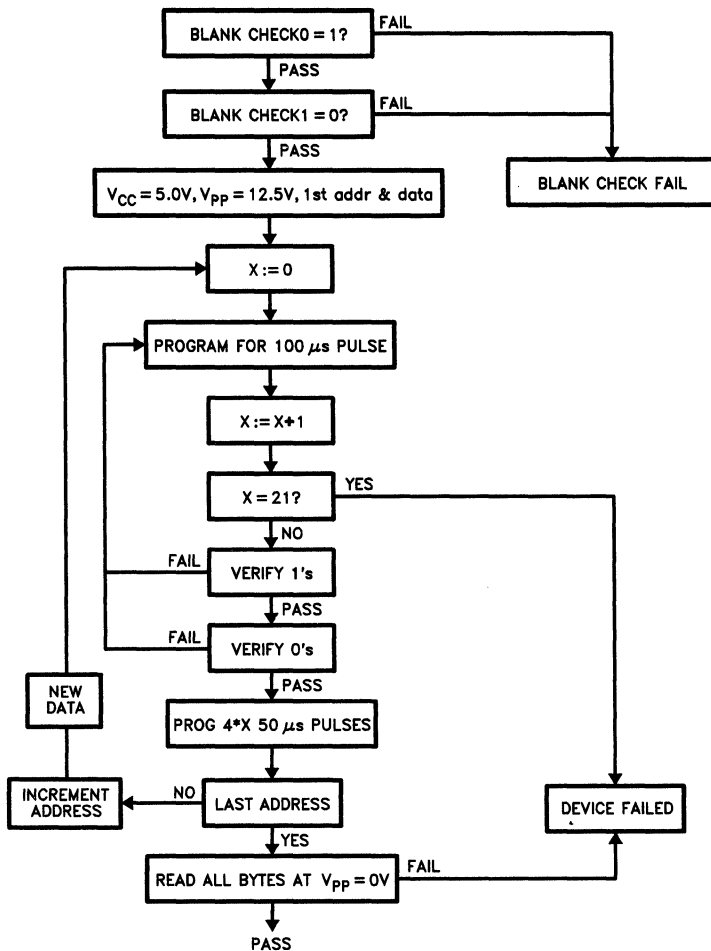


Figure 3. Programming Flowchart

0102-14

Note:  
For main array only. Sync. and ALE bits use 200 50 μs pulses.

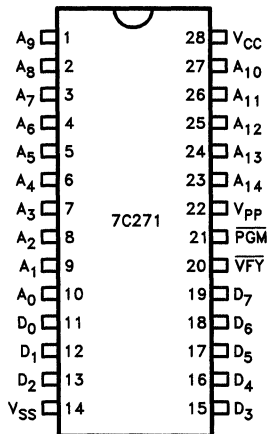
Table 2. DC Programming Parameters  $T_A = 25^\circ\text{C}$

| Parameters       | Description                             | Min. | Max.             | Units |
|------------------|---|------|------------------|-------|
| V <sub>PP</sub>  | Programming Voltage                     | 12.0 | 13.0             | V     |
| V <sub>CCP</sub> | Power Supply Voltage During Programming | 4.75 | 5.25             | V     |
| I <sub>PP</sub>  | V <sub>PP</sub> Supply Current          |      | 50               | mA    |
| V <sub>IHP</sub> | Input High Voltage During Programming   | 3.0  | V <sub>CCP</sub> | V     |
| V <sub>ILP</sub> | Input Low Voltage During Programming    |      | 0.4              | V     |
| V <sub>OH</sub>  | Output High Voltage                     | 2.4  |                  | V     |
| V <sub>OL</sub>  | Output Low Voltage                      |      | 0.4              | V     |

Table 3. AC Programming Parameters  $T_A = 25^\circ\text{C}$

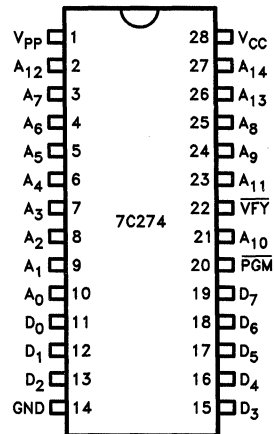
| Parameters       | Description                        | Min. | Max. | Units         |
|------------------|------------------------------------|------|------|---------------|
| t <sub>AS</sub>  | Address Setup Time to PGM/VFY      | 1.0  |      | $\mu\text{s}$ |
| t <sub>AH</sub>  | Address Hold Time from PGM/VFY     | 1.0  |      | $\mu\text{s}$ |
| t <sub>DS</sub>  | Data Setup Time to PGM             | 1.0  |      | $\mu\text{s}$ |
| t <sub>DH</sub>  | Data Hold Time PGM                 | 1.0  |      | $\mu\text{s}$ |
| t <sub>PP</sub>  | Program Pulse Width                | 0.1  | 10   | ms            |
| t <sub>R,F</sub> | V <sub>PP</sub> Rise and Fall Time | 1.0  |      | $\mu\text{s}$ |
| t <sub>DV</sub>  | Delay to Verify                    | 1.0  |      | $\mu\text{s}$ |
| t <sub>VD</sub>  | Verify to Data Out                 |      | 1.0  | $\mu\text{s}$ |
| t <sub>VP</sub>  | Verify Pulse Width                 | 5.0  |      | $\mu\text{s}$ |
| t <sub>DZ</sub>  | Verify to High Z                   |      | 1.0  | $\mu\text{s}$ |
| t <sub>p</sub>   | Power Up/Down                      | 20.0 |      | ms            |
| t <sub>PS</sub>  | Verify Setup/Hold to Program       | 1.0  |      | $\mu\text{s}$ |

7C271 Programming Pin-Out



0102-8

7C274 Programming Pin-Out



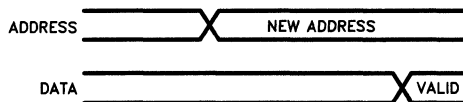
0102-12

## Read Mode Table

| Part  | V <sub>PP</sub> | PGM             | V <sub>FY</sub> |
|-------|-----------------|-----------------|-----------------|
| 7C271 | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub> |
| 7C274 | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IL</sub> |

## Reading PROMs

Below are timing diagrams for the final read of the PROMs. Use 1  $\mu$ s timing for pulse widths and overlaps.



0102-15

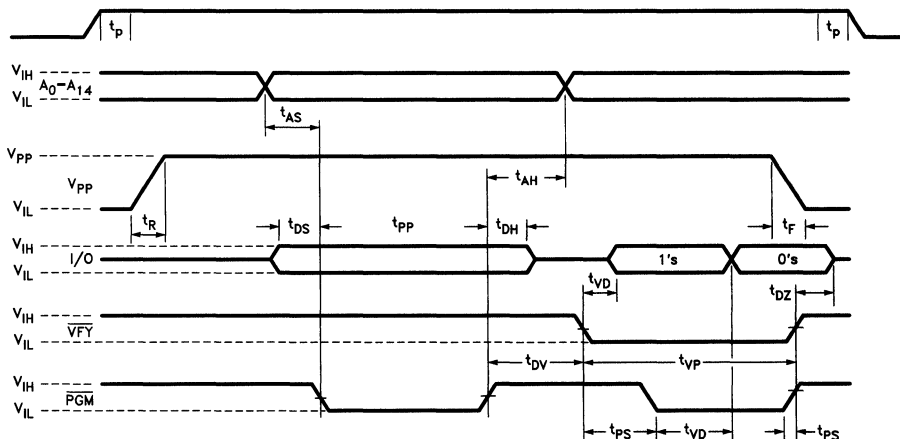


Figure 4. PROM Programming Waveforms

0102-9

## Ordering Information

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 45         | CY7C271-45PC  | P21          | Commercial      |
|            | CY7C271-45WC  | W22          |                 |
|            | CY7C274-45PC  | P15          |                 |
|            | CY7C274-45WC  | W16          |                 |
| 55         | CY7C271-55PC  | P21          | Commercial      |
|            | CY7C271-55WC  | W22          |                 |
|            | CY7C274-55PC  | P15          |                 |
|            | CY7C274-55WC  | W16          |                 |
|            | CY7C271-55DMB | D22          | Military        |
|            | CY7C271-55WMB | W22          |                 |
|            | CY7C271-55LMB | L55          |                 |
|            | CY7C271-55QMB | Q55          |                 |
|            | CY7C274-55DMB | D16          |                 |
|            | CY7C274-55WMB | W16          |                 |
|            | CY7C274-55LMB | L55          |                 |
|            | CY7C274-55QMB | Q55          |                 |

**MILITARY SPECIFICATIONS****Group A Subgroup Testing****DC Characteristics**

| Parameters      | Subgroups |
|-----------------|-----------|
| V <sub>OH</sub> | 1,2,3     |
| V <sub>OL</sub> | 1,2,3     |
| V <sub>IH</sub> | 1,2,3     |
| V <sub>IL</sub> | 1,2,3     |
| I <sub>IH</sub> | 1,2,3     |
| I <sub>OZ</sub> | 1,2,3     |
| I <sub>CC</sub> | 1,2,3     |
| I <sub>SB</sub> | 1,2,3     |

**Switching Characteristics**

| Parameters                      | Subgroups   |
|---------------------------------|-------------|
| t <sub>AA</sub>                 | 7,8,9,10,11 |
| t <sub>ACS</sub> <sup>[1]</sup> | 7,8,9,10,11 |
| t <sub>OE</sub> <sup>[2]</sup>  | 7,8,9,10,11 |
| t <sub>ACE</sub>                | 7,8,9,10,11 |

**Notes:**

1. 7C271 only.
2. 7C274 only.

Document #: 38-00068-C

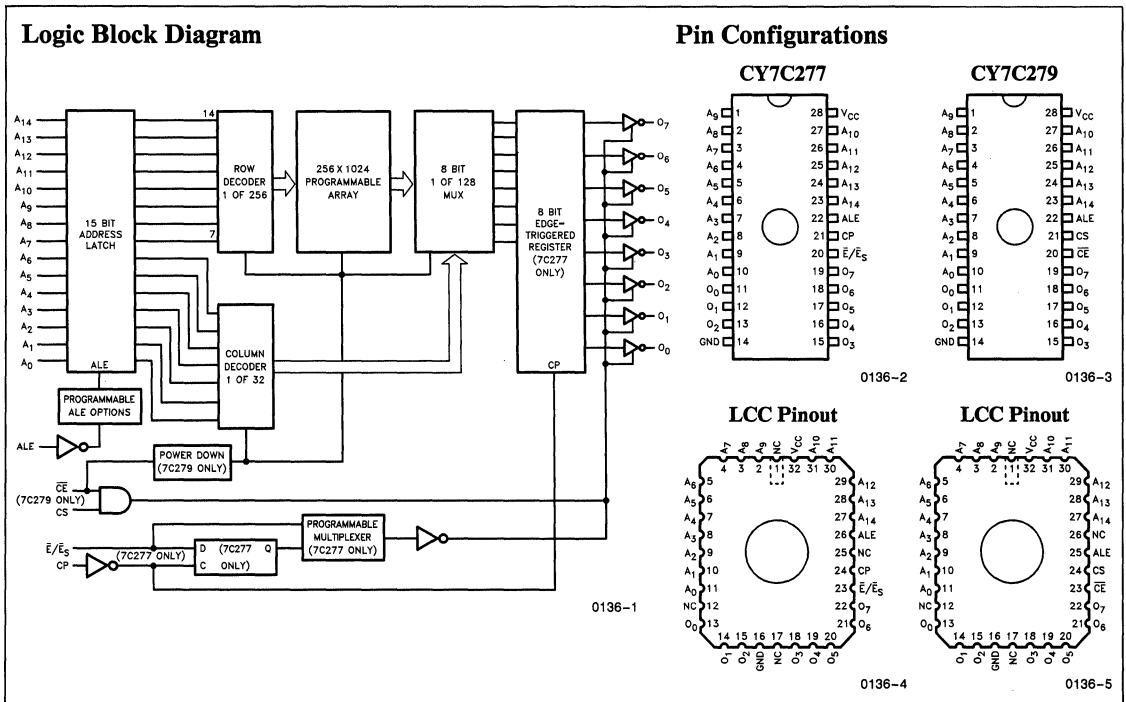


# Reprogrammable 32,768 x 8 Registered PROM

## Features

- Windowed for reprogrammability
- CMOS for optimum speed/power
- High speed
  - 40 ns max set-up
  - 20 ns clock to output
- Low power
  - 660 mW (commercial)
  - 715 mW (military)
- Programmable address latch enable input
- Programmable synchronous or asynchronous output enable (7C277)
- On-chip edge-triggered registers
- EPROM technology, 100% programmable
- Slim 300 mil, 28-pin plastic or hermetic DIP
- 5V ±10% V<sub>CC</sub>, commercial and military
- TTL compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 2000V static discharge

3



## Selection Guide

|                                | 7C279-45   | 7C277-40 | 7C279-55 | 7C277-50 |
|--------------------------------|------------|----------|----------|----------|
| Maximum Access Time (ns)       | 45         |          | 55       |          |
| Maximum Setup Time (ns)        |            | 40       |          | 50       |
| Maximum Clock to Output (ns)   |            | 20       |          | 25       |
| Maximum Operating Current (mA) | Commercial | 120      | 120      | 120      |
|                                | Military   |          | 130      | 130      |
| Maximum Standby Current (mA)   | Commercial | 30       |          | 30       |
|                                | Military   |          |          | 40       |



## Product Characteristics

The CY7C277 and CY7C279 are high performance 32,768 word by 8 bit CMOS PROMs. When deselected, the 7C279 automatically powers down into a low power standby mode. The 7C277 and the 7C279 both are packaged in the slim 28 pin 300 mil package. The ceramic package may be equipped with an erasure window; when exposed to UV light, the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide algorithms.

The CY7C277 and CY7C279 offer the advantages of lower power, reprogrammability, superior performance and high programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the project will meet DC and AC specification limits.

On the 7C277, the outputs are pipelined through a master-slave register. On the rising edge of CP, data is loaded into the 8 bit edge triggered output register. The  $\bar{E}/E_s$  provides a programmable bit to select between asynchronous and synchronous operation. The default condition is

asynchronous. When the asynchronous mode is selected, the  $\bar{E}/E_s$  pin is sampled continuously and operates as an output enable. If the synchronous mode is selected, then the  $\bar{E}/E_s$  pin is sampled only when CP is HIGH. Enabling the outputs in this mode is accomplished by bringing the  $\bar{E}_s$  pin LOW and pulsing the CP HIGH to latch the output enable state. The 7C277 also provides a programmable bit to enable the ADDRESS LATCH ENABLE (ALE) pin. If this bit is not programmed, then the device will ignore the ALE pin. If the ALE function is selected, the user may define the polarity of the ALE signal with the default being a positive ACTIVE signal.

On the 7C279, address registers are provided to easily interface with the Cypress 7C601 and other microprocessors that clock their addresses. A programmable bit is provided to select between Latched and Registered address inputs. The default is registered inputs, which will sample the address on the RISING EDGE of ALE and latch the address into the address register. The Latched address option will recognize any address changes while the ALE pin is ACTIVE and latch the address into the address registers on the FALLING EDGE of ALE. If the latched address option is selected, then another programmable bit is provided for the user to select the polarity that will define ALE ACTIVE, with the default being positive polarity.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential

(Pin 24 to Pin 12) ..... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) ..... 13.0V

UV Erasure ..... 7258 Wsec/cm<sup>2</sup>

Static Discharge Voltage ..... >2001V  
(Per MIL-STD-883 Method 3015)

Latchup Current ..... >200 mA

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ±10%         |
| Military <sup>[2]</sup> | -55°C to +125°C     | 5V ±10%         |

## Electrical Characteristics Over Operating Range<sup>[3]</sup>

| Parameters                     | Description                     | Test Conditions   | 7C277-40<br>7C279-45 |                 | 7C277-50<br>7C279-55 |                 | Units |
|--------------------------------|---------------------------------|---|----------------------|-----------------|----------------------|-----------------|-------|
|                                |                                 |   | Min.                 | Max.            | Min.                 | Max.            |       |
| V <sub>OH</sub>                | Output HIGH Voltage             | V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA                                     | 2.4                  |                 | 2.4                  |                 | V     |
| V <sub>OL</sub>                | Output LOW Voltage              | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA                                      |                      | 0.4             |                      | 0.4             | V     |
| V <sub>IH</sub>                | Input HIGH Level <sup>[4]</sup> |   | 2.0                  | V <sub>CC</sub> | 2.0                  | V <sub>CC</sub> | V     |
| V <sub>IL</sub>                | Input LOW Level <sup>[4]</sup>  |   |                      | 0.8             |                      | 0.8             | V     |
| I <sub>IX</sub>                | Input Leakage Current           | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>   | -10                  | +10             | -10                  | +10             | μA    |
| V <sub>CD</sub>                | Input Clamp Diode Voltage       |   | Note 5               |                 |                      |                 |       |
| I <sub>OZ</sub>                | Output Leakage Current          | V <sub>OL</sub> ≤ V <sub>OUT</sub> ≤ V <sub>OH</sub> , Output Disabled <sup>[6]</sup> | -40                  | +40             | -40                  | +40             | μA    |
| I <sub>OS</sub>                | Output Short Circuit Current    | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.0V <sup>[7]</sup>                        | -20                  | -90             | -20                  | -90             | mA    |
| I <sub>CC</sub>                | Power Supply Current            | V <sub>CC</sub> = Max., V <sub>IH</sub> = 2.0V<br>I <sub>OUT</sub> = 0 mA             | Commercial           | 120             | 120                  |                 | mA    |
|                                |                                 |   | Military             |                 | 130                  |                 |       |
| I <sub>SB</sub> <sup>[9]</sup> | Standby Supply Current          | V <sub>CC</sub> = Max., $\bar{CS} \geq V_{IH}$<br>I <sub>OUT</sub> = 0 mA             | Commercial           | 30              | 30                   |                 | mA    |
|                                |                                 |   | Military             |                 | 40                   |                 |       |

## Capacitance<sup>[8]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 8    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 8    |       |

### Notes:

- The 7C279 only has a standby mode.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
- The CMOS process does not provide a clamp diode. However, the CY7C277 and CY7C279 are insensitive to -3V dc input levels and -5V undershoot pulses of less than 10 ns (measured at 50% point).
- For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

3

## Switching Characteristics Over Operating Range<sup>[8]</sup>

| Parameters                          | Description                       | 7C277-40 |      | 7C277-50 |      | Units |
|-------------------------------------|-----------------------------------|----------|------|----------|------|-------|
|                                     |                                   | Min.     | Max. | Min.     | Max. |       |
| t <sub>AL</sub>                     | Address Setup to ALE Active       | 10       |      | 10       |      | ns    |
| t <sub>LA</sub>                     | Address Hold from ALE Inactive    | 10       |      | 15       |      | ns    |
| t <sub>LL</sub>                     | ALE Pulse Width                   | 10       |      | 15       |      | ns    |
| t <sub>SA</sub>                     | Address Setup to Clock HIGH       | 40       |      | 50       |      | ns    |
| t <sub>HA</sub>                     | Address Hold from Clock HIGH      | 0        |      | 0        |      | ns    |
| t <sub>SES</sub>                    | $\bar{E}_S$ Setup to Clock HIGH   | 15       |      | 15       |      | ns    |
| t <sub>HES</sub>                    | $\bar{E}_S$ Hold from Clock HIGH  | 10       |      | 10       |      | ns    |
| t <sub>CO</sub> <sup>[14]</sup>     | Clock HIGH to Output Valid        |          | 20   |          | 25   | ns    |
| t <sub>PWC</sub>                    | Clock Pulse Width                 | 20       |      | 20       |      | ns    |
| t <sub>LZC</sub>                    | Output Low Z from Clock HIGH      |          | 20   |          | 30   | ns    |
| t <sub>HZC</sub> <sup>[14, 9]</sup> | Output High Z from Clock HIGH     |          | 20   |          | 30   | ns    |
| t <sub>LZE</sub>                    | Output Low Z from $\bar{E}$ LOW   |          | 20   |          | 30   | ns    |
| t <sub>HZE</sub> <sup>[15, 9]</sup> | Output High Z from $\bar{E}$ HIGH |          | 20   |          | 30   | ns    |

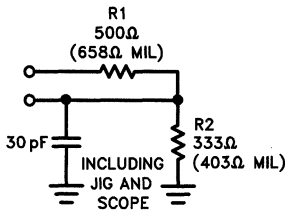
**Switching Characteristics Over Operating Range<sup>[8]</sup> (Continued)**

| Parameters                      | Description                          | 7C279-45 |      | 7C279-55 |      | Units |
|---------------------------------|--------------------------------------|----------|------|----------|------|-------|
|                                 |                                      | Min.     | Max. | Min.     | Max. |       |
| t <sub>AA</sub> <sup>[12]</sup> | Address Access to Output Valid       |          | 45   |          | 55   | ns    |
| t <sub>HZCS</sub>               | Chip Select Inactive to High Z       |          | 30   |          | 30   | ns    |
| t <sub>ACS</sub>                | Chip Select Inactive to Output Valid |          | 30   |          | 30   | ns    |
| t <sub>AR</sub>                 | Address Register Setup to ALE Active | 10       |      | 10       |      | ns    |
| t <sub>RA</sub>                 | Address Hold from ALE Active         | 10       |      | 10       |      | ns    |
| t <sub>ADH</sub>                | Data Hold from ALE Active            | 5        |      | 5        |      | ns    |
| t <sub>PU</sub>                 | Chip Enable Active to Power Up       | 0        |      | 0        |      | ns    |
| t <sub>PD</sub>                 | Chip Enable Inactive to Power Down   |          | 50   |          | 60   | ns    |
| t <sub>OH</sub> <sup>[12]</sup> | Output Hold from Address Change      | 0        |      | 0        |      | ns    |
| t <sub>PWA</sub>                | Address Register Pulse Width         |          | 20   |          | 30   | ns    |

**Notes:**

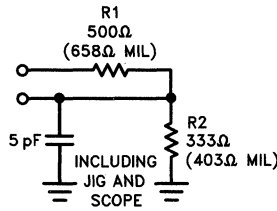
9. t<sub>HZCS</sub> and t<sub>HZE</sub> are tested with the load shown in *Figure 1b*. Transition is measured at steady state high level - 500 mV or steady state low level + 500 mV on the output from the 1.5V level on the input.
10. These parameters apply to the 7C277 only.
11. These parameters apply to the 7C279 only.
12. t<sub>AA</sub> and t<sub>OH</sub> apply only when the latched mode is selected.
13. Tests are performed with rise and fall times of 5 ns or less.
14. Applies only when the synchronous ( $\bar{E}_S$ ) function is used.
15. Applies only when the asynchronous ( $\bar{E}$ ) function is used.
16. See *Figure 1a* for all switching characteristics except t<sub>HZCS</sub> and t<sub>HZE</sub>.
17. See the last page of this specification for Group A subgroup testing information.
18. All device test loads should be located within 2" of device outputs.

**AC Test Loads and Waveforms<sup>[9, 16, 18]</sup>**



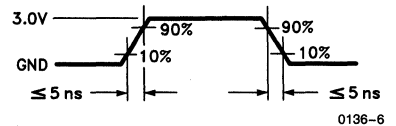
**Figure 1a**

0136-7



**Figure 1b**

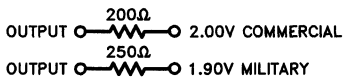
0136-8



**Figure 2**

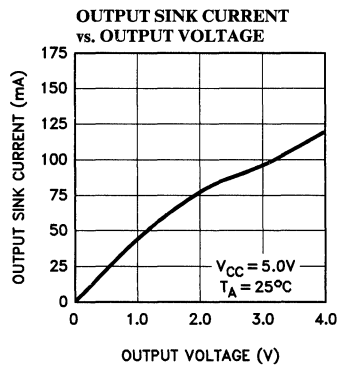
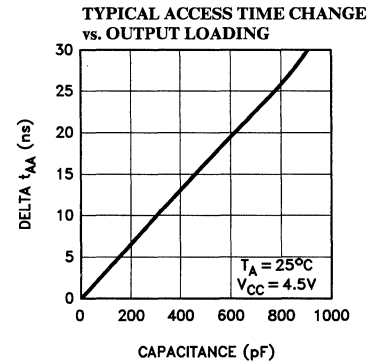
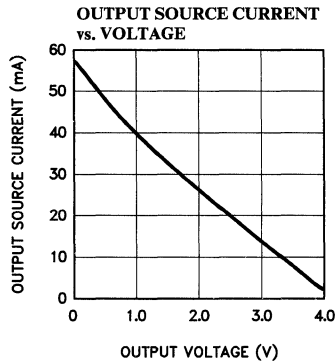
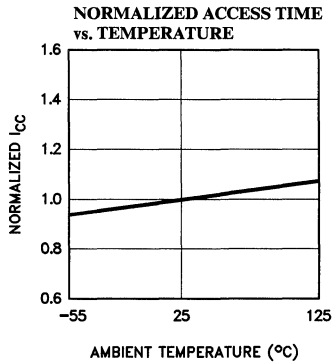
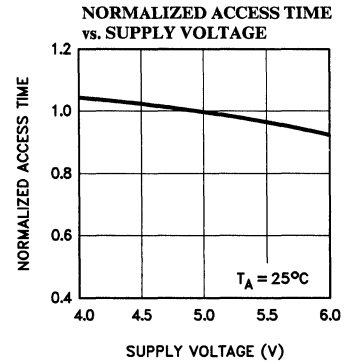
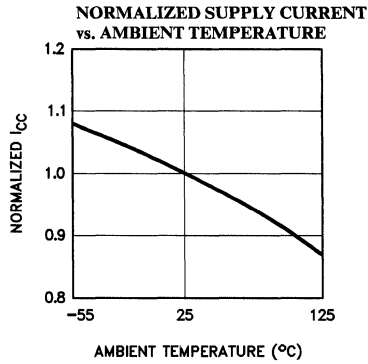
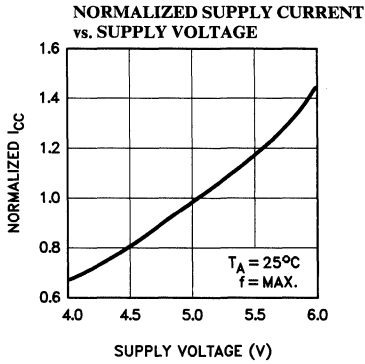
0136-6

Equivalent to: THÉVENIN EQUIVALENT



0136-14

## Typical DC and AC Characteristics



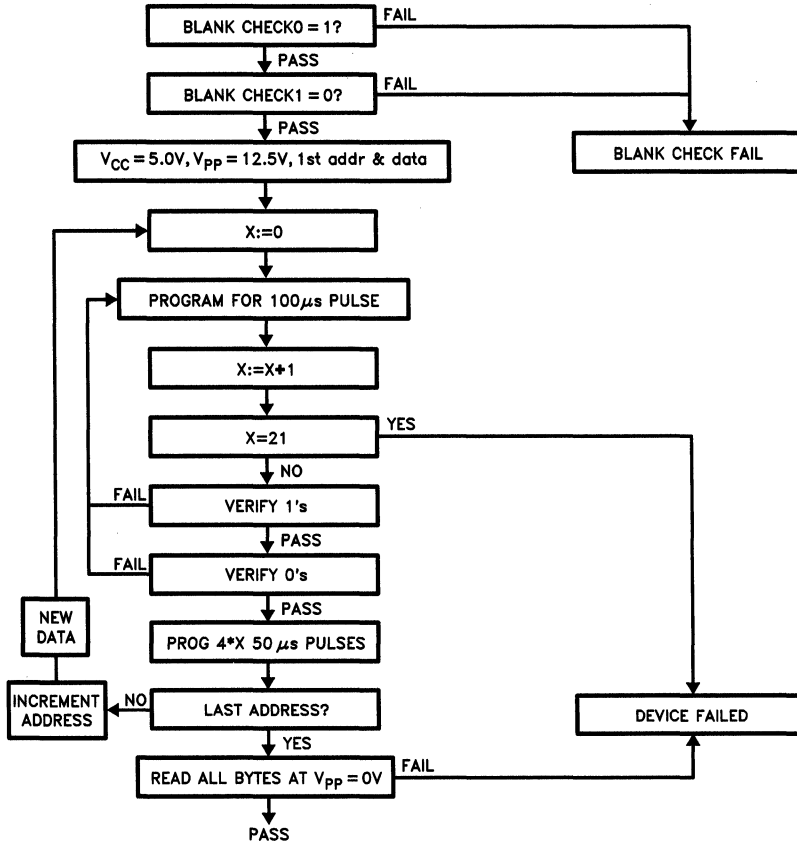
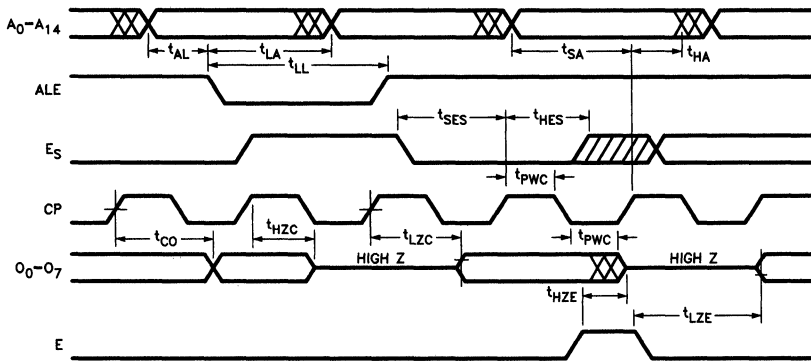


Figure 3. Programming Flowchart

0136-16

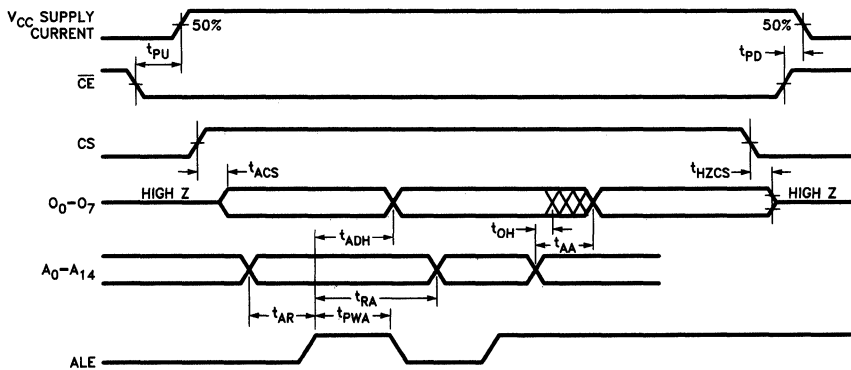
Note:  
For main array only. Sync. and ALE bits use 200 50 µs pulses.

### Timing Diagram (7C277)



0136-9

### Timing Diagram (7C279)



0136-10

Note:  
ALE is shown with positive polarity.

### Erase Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C277 and 7C279. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity  $\times$  exposure time) of 25 Wsec/cm<sup>2</sup>. For an ultraviolet lamp with a 12 mW/cm<sup>2</sup> power rating the exposure time would be approximately 45 minutes. The 7C277 and 7C279 need to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm<sup>2</sup> is the recommended maximum dosage.

### Device Programming

There are several independent programmable functions contained in the 7C277 and 7C279 CMOS 32K x 8 registered PROM. Both devices have the 32K x 8 array and a programmable ALE function. The 7C277 also contains a programmable synchronous function ( $\bar{E}/\bar{E}_s$ ).

All of the programming elements are EPROM cells and are in an erased state when they are shipped. This erased state manifests itself differently in each case. The erased state for the synchronous function is ASYNCHRONOUS mode. The erased state for the ALE function is: Registered inputs on the 7C279 and no ALE function on the 7C277. In the erased state, the memory location contains neither a one nor a zero. The erased state of the device can be verified by using the BLANK CHECK ONES and BLANK CHECK ZEROS function (see mode table).

To choose the ALE function, the ALE bit must be programmed. This is done by raising A<sub>9</sub> to V<sub>pp</sub>, taking A<sub>14</sub> LOW and pulsing PGM LOW. When the ALE function is chosen, it is active with positive polarity. To choose negative polarity, A<sub>9</sub> must be at V<sub>pp</sub>, A<sub>14</sub> must be raised HIGH and PGM must be pulsed LOW. The 7C277 comes with a synchronous option. To choose this option, the SYN bit must be programmed. This is done by taking A<sub>14</sub> to V<sub>pp</sub> and pulsing PGM LOW.

To verify these special bits, A<sub>14</sub> must be at V<sub>pp</sub> and the V<sub>pp</sub> must be held LOW with PGM held HIGH and CE LOW. The ALE bit is read on I/O<sub>1</sub>, the polarity bit is read on I/O<sub>2</sub> and the synchronous bit is read on I/O<sub>0</sub>.

**DC Programming Parameters**  $T_A = 25^\circ\text{C}$ 
**Table 1**

| Parameter    | Description                | Min. | Max.      | Units |
|--------------|----------------------------|------|-----------|-------|
| $V_{PP}$ [1] | Programming Voltage        | 12.0 | 13.0      | V     |
| $V_{CCP}$    | Supply Voltage             | 4.75 | 5.25      | V     |
| $V_{IHP}$    | Input High Voltage         | 3.0  | $V_{CCP}$ | V     |
| $V_{ILP}$    | Input Low Voltage          |      | 0.4       | V     |
| $V_{OH}$ [2] | Output High Voltage        | 2.4  |           | V     |
| $V_{OL}$ [2] | Output Low Voltage         |      | 0.4       | V     |
| $I_{PP}$     | Programming Supply Current |      | 50        | mA    |

**AC Programming Parameters**  $T_A = 25^\circ\text{C}$ 
**Table 2**

| Parameter      | Description  | Min. | Max. | Units         |
|----------------|--|------|------|---------------|
| $t_{PP}$       | Programming Pulse Width  | 0.1  | 10   | ms            |
| $t_{AS}$       | Address Setup Time to $\overline{\text{PGM}}/\overline{\text{VFY}}$  | 1.0  |      | $\mu\text{s}$ |
| $t_{DS}$       | Data Setup Time to $\overline{\text{PGM}}$                           | 1.0  |      | $\mu\text{s}$ |
| $t_{AH}$       | Address Hold Time from $\overline{\text{PGM}}/\overline{\text{VFY}}$ | 1.0  |      | $\mu\text{s}$ |
| $t_{DH}$       | Data Hold Time from $\overline{\text{PGM}}$                          | 1.0  |      | $\mu\text{s}$ |
| $t_R, t_F$ [3] | $V_{PP}$ Rise and Fall Time  | 1.0  |      | $\mu\text{s}$ |
| $t_{VD}$       | Verify to Data Out   |      | 1.0  | $\mu\text{s}$ |
| $t_{VP}$       | Verify Pulse Width   | 5.0  |      | $\mu\text{s}$ |
| $t_{DV}$       | Delay to Verify  | 1.0  |      | $\mu\text{s}$ |
| $t_{DZ}$       | Verify HIGH to High Z  |      | 1.0  | $\mu\text{s}$ |
| $t_P$          | Power Up/Down  | 20.0 |      | ms            |
| $t_{PS}$       | $\overline{\text{VFY}}$ Setup/Hold to $\overline{\text{PGM}}$        |      | 1.0  | $\mu\text{s}$ |

**Notes:**

1.  $V_{CCP}$  must be applied prior to  $V_{PP}$ .
2. During verify operation.
3. Measured 10% and 90% points.

## Mode Selection

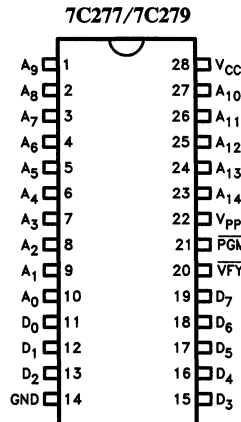
Mode Table

| Mode                            | Read    | A <sub>9</sub>  | A <sub>14</sub> | ALE                               | CP-7C277<br>CS-7C279              | $\bar{E}/\bar{E}_S$ -7C277<br>CE-7C279 | A <sub>0</sub> -A <sub>8</sub><br>A <sub>10</sub> -A <sub>13</sub> | Data |
|---------------------------------|---------|-----------------|-----------------|-----------------------------------|-----------------------------------|--|--|------|
|                                 | Program | A <sub>9</sub>  | A <sub>14</sub> | V <sub>PP</sub>                   | PGM                               | $\overline{VFY}$                       | A <sub>0</sub> -A <sub>8</sub><br>A <sub>10</sub> -A <sub>13</sub> | Data |
| Read                            |         | A               | A               | V <sub>IL</sub>                   | V <sub>IH</sub>                   | V <sub>IL</sub>                        | A  | Out  |
| Program                         |         | A               | A               | V <sub>PP</sub>                   | V <sub>IL</sub>                   | V <sub>IH</sub>                        | A  | In   |
| Program SYN Bit                 |         | X               | V <sub>PP</sub> | V <sub>PP</sub>                   | V <sub>IL</sub>                   | V <sub>IH</sub>                        | X  | X    |
| Program ALE Bit                 |         | V <sub>PP</sub> | V <sub>IL</sub> | V <sub>PP</sub>                   | V <sub>IL</sub>                   | V <sub>IH</sub>                        | X  | X    |
| Program ALE Low Polarity        |         | V <sub>PP</sub> | V <sub>IH</sub> | V <sub>PP</sub>                   | V <sub>IL</sub>                   | V <sub>IH</sub>                        | X  | X    |
| Program Verify <sup>[1]</sup>   |         | A               | A               | V <sub>PP</sub>                   | V <sub>IH</sub> , V <sub>IL</sub> | V <sub>IL</sub>                        | A  | Out  |
| Program Inhibit                 |         | A               | A               | V <sub>PP</sub>                   | V <sub>IH</sub>                   | V <sub>IH</sub>                        | A  | X    |
| Blank Check 0, 1 <sup>[2]</sup> |         | A               | A               | V <sub>IH</sub> , V <sub>IL</sub> | V <sub>PP</sub>                   | V <sub>PP</sub>                        | A  | Out  |
| Verify Special Bits             |         | X               | V <sub>PP</sub> | V <sub>IL</sub>                   | V <sub>IH</sub>                   | V <sub>IL</sub>                        | X  | Out  |

Notes:

1. During program verify PGM must first be held HIGH to verify ones and then LOW to verify zeros.

2. To blank check zeros, V<sub>PP</sub> is held to V<sub>IH</sub> and all ones should be read on the outputs. To blank check ones, V<sub>PP</sub> is held to V<sub>IL</sub> and all zeros should be read on the outputs.



0136-12

Figure 4. Programming Pinout

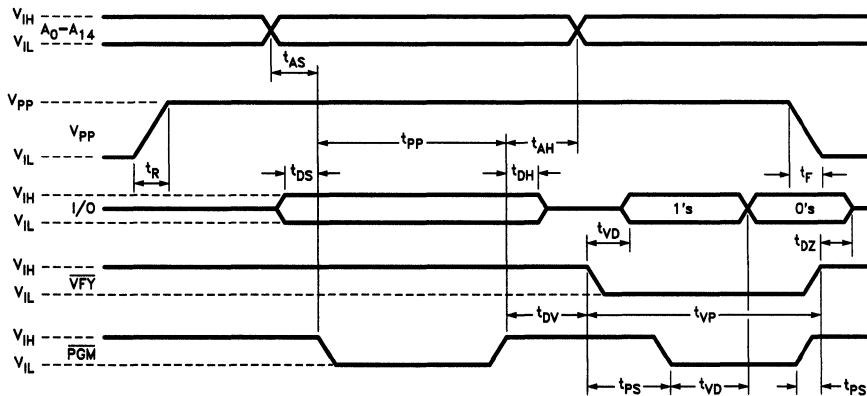


Figure 5. PROM Programming Waveforms

0136-13



**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 45         | CY7C277-40PC  | P21          | Commercial      |
|            | CY7C277-40WC  | W22          |                 |
|            | CY7C279-45PC  | P21          |                 |
|            | CY7C279-45 WC | W22          |                 |
| 55         | CY7C277-50 PC | P21          | Commercial      |
|            | CY7C277-50WC  | W22          |                 |
|            | CY7C279-55PC  | P21          |                 |
|            | CY7C279-55 WC | W22          |                 |
|            | CY7C277-50DMB | D22          | Military        |
|            | CY7C277-50WMB | W22          |                 |
|            | CY7C277-50LMB | L55          |                 |
|            | CY7C277-50QMB | Q55          |                 |
|            | CY7C279-55DMB | D22          |                 |
|            | CY7C279-55WMB | W22          |                 |
|            | CY7C279-55LMB | L55          |                 |
|            | CY7C279-55QMB | Q55          |                 |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters                      | Subgroups |
|---------------------------------|-----------|
| V <sub>OH</sub>                 | 1,2,3     |
| V <sub>OL</sub>                 | 1,2,3     |
| V <sub>IH</sub>                 | 1,2,3     |
| V <sub>IL</sub>                 | 1,2,3     |
| I <sub>IX</sub>                 | 1,2,3     |
| I <sub>OZ</sub>                 | 1,2,3     |
| I <sub>CC</sub>                 | 1,2,3     |
| I <sub>SB</sub> <sup>[11]</sup> | 1,2,3     |

3

#### Switching Characteristics

| Device | Parameters       | Subgroups   |
|--------|------------------|-------------|
| 7C277  | t <sub>SA</sub>  | 7,8,9,10,11 |
|        | t <sub>HA</sub>  | 7,8,9,10,11 |
|        | t <sub>CO</sub>  | 7,8,9,10,11 |
| 7C279  | t <sub>AR</sub>  | 7,8,9,10,11 |
|        | t <sub>RA</sub>  | 7,8,9,10,11 |
|        | t <sub>DHA</sub> | 7,8,9,10,11 |

**Note:**

11. These parameters apply to the 7C279 only.

Document #: 38-00085



**Features**

- CMOS for optimum speed/power
- High speed
  - 30 ns (commercial)
  - 45 ns (military)
- Low power
  - 495 mW (commercial)
  - 660 mW (military)
- EPROM technology 100% programmable
- Slim 300 or standard 600 mil DIP or 28 pin LCC
- 5V ± 10% V<sub>CC</sub>, commercial and military
- TTL compatible I/O
- Direct replacement for bipolar PROMs

- Capable of withstanding > 1500V static discharge

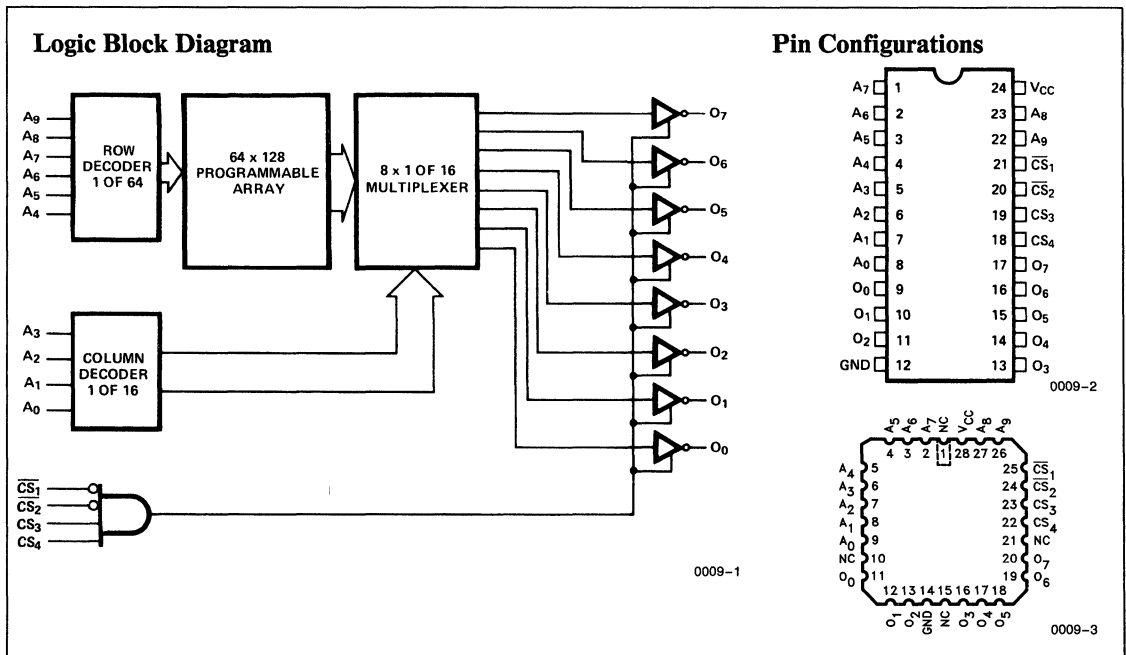
**Product Characteristics**

The CY7C281 and CY7C282 are high performance 1024 word by 8 bit CMOS PROMs. They are functionally identical, but are packaged in 300 mil and 600 mil wide packages respectively. The CY7C281 is also available in a 28 pin leadless chip carrier. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C281 and CY7C282 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 13.5V for the superevoltage and

low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW signal on CS<sub>1</sub> and CS<sub>2</sub>, and active HIGH signals on CS<sub>3</sub> and CS<sub>4</sub>. The contents of the memory location addressed by the address lines (A<sub>0</sub>–A<sub>9</sub>) will become available on the output lines (O<sub>0</sub>–O<sub>7</sub>).



**Selection Guide**

|                                |            | <b>7C281-30</b><br><b>7C282-30</b> | <b>7C281-45</b><br><b>7C282-45</b> |
|--------------------------------|------------|------------------------------------|------------------------------------|
| Maximum Access Time (ns)       |            | 30                                 | 45                                 |
| Maximum Operating Current (mA) | Commercial | 100                                | 90                                 |
|                                | Military   |                                    | 120                                |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential

(Pin 24 to Pin 12) ..... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

DC Program Voltage (Pins 18, 20) ..... 14.0V

Static Discharge Voltage ..... > 1500V  
 (per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[1]</sup> | -55°C to +125°C     | 5V ± 10%        |

**3**

### Electrical Characteristics Over the Operating Range<sup>[2]</sup>

| Parameters      | Description                                 | Test Conditions  | 7C281-30<br>7C282-30 |      | 7C281-45<br>7C282-45 |      | Units |
|-----------------|---|--|----------------------|------|----------------------|------|-------|
|                 |   |  | Min.                 | Max. | Min.                 | Max. |       |
| V <sub>OH</sub> | Output HIGH Voltage                         | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA                      | 2.4                  |      | 2.4                  |      | V     |
| V <sub>OL</sub> | Output LOW Voltage                          | V <sub>CC</sub> = Min., I <sub>OL</sub> = 16.0 mA                      |                      | 0.4  |                      | 0.4  | V     |
| V <sub>IH</sub> | Input HIGH Level <sup>[3]</sup>             |  | 2.0                  |      | 2.0                  |      | V     |
| V <sub>IL</sub> | Input LOW Level <sup>[3]</sup>              |  |                      | 0.8  |                      | 0.8  | V     |
| I <sub>Ix</sub> | Input Current                               | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                                | -10                  | +10  | -10                  | +10  | μA    |
| V <sub>CD</sub> | Input Diode Clamp Voltage                   |  | Note 4               |      | Note 4               |      |       |
| I <sub>OZ</sub> | Output Leakage Current                      | V <sub>OL</sub> ≤ V <sub>OUT</sub> ≤ V <sub>OH</sub> , Output Disabled | -40                  | +40  | -40                  | +40  | μA    |
| I <sub>OS</sub> | Output Short Circuit Current <sup>[5]</sup> | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND                         | -20                  | -90  | -20                  | -90  | mA    |
| I <sub>CC</sub> | Power Supply Current                        | V <sub>CC</sub> = Max.,<br>I <sub>OUT</sub> = 0 mA                     | Commercial           | 100  | 90                   |      | mA    |
|                 |   |  | Military             |      |                      | 120  | mA    |

### Capacitance<sup>[6]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 8    |       |

#### Notes:

1. T<sub>A</sub> is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. The CMOS process does not provide a clamp diode. However, the CY7C281 & CY7C282 are insensitive to -3V dc input levels and -5V undershoot pulses of less than 10 ns (measured at 50% point).
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
6. Tested initially and after any design or process changes that may affect these parameters.

**Switching Characteristics Over the Operating Range**<sup>[2, 7]</sup>

| Parameters        | Description                                   | CY7C281-30<br>CY7C282-30 |      | CY7C281-45<br>CY7C282-45 |      | Units |
|-------------------|---|--------------------------|------|--------------------------|------|-------|
|                   |   | Min.                     | Max. | Min.                     | Max. |       |
| t <sub>AA</sub>   | Address to Output Valid                       |                          | 30   |                          | 45   | ns    |
| t <sub>HZCS</sub> | Chip Select Inactive to High Z <sup>[8]</sup> |                          | 20   |                          | 25   | ns    |
| t <sub>ACS</sub>  | Chip Select Active to Output Valid            |                          | 20   |                          | 25   | ns    |

**AC Test Loads and Waveforms**

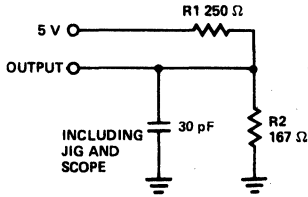


Figure 1a

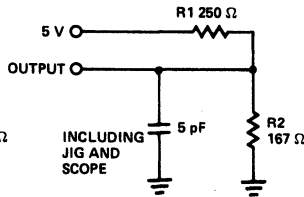


Figure 1b

0009-4

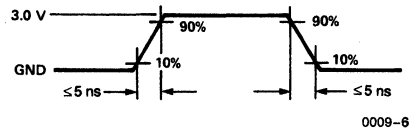
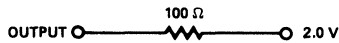


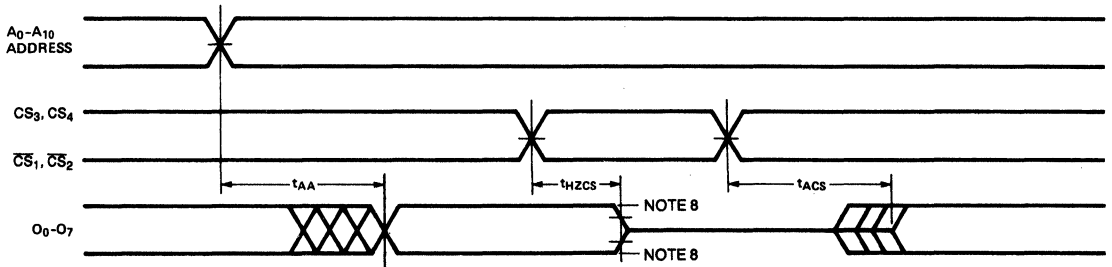
Figure 2. Input Pulses

0009-6

Equivalent to: THÉVENIN EQUIVALENT



0009-5



0009-7

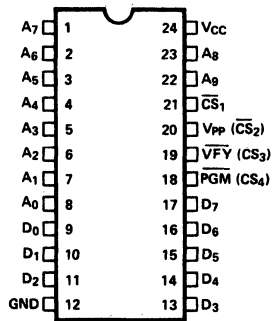
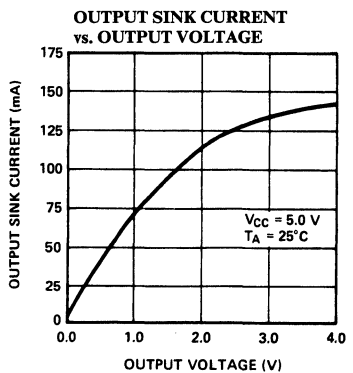
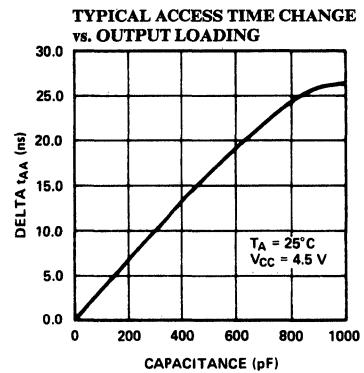
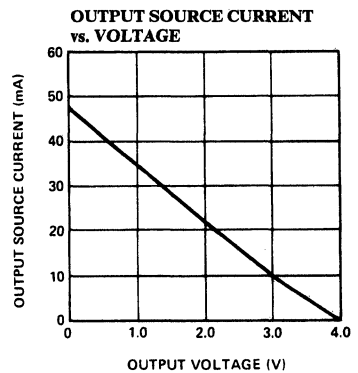
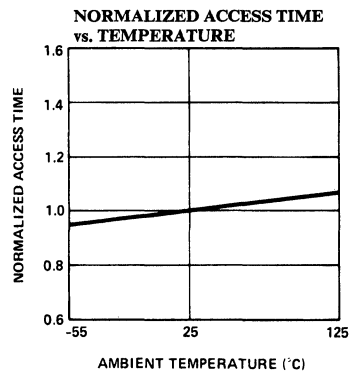
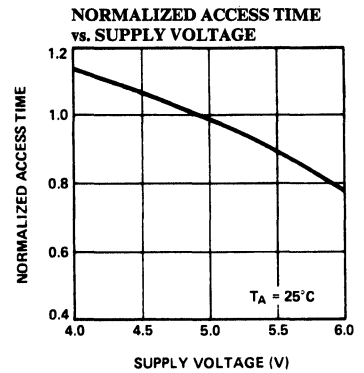
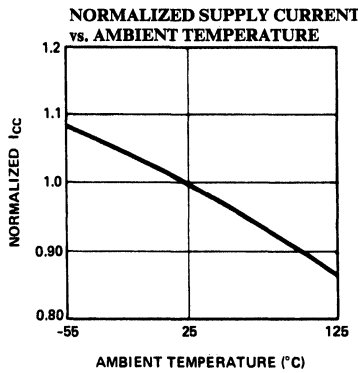
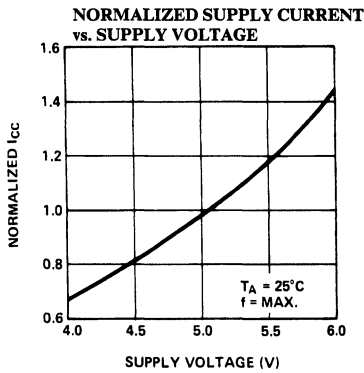
**Notes:**

7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and loads shown in Figure 1a, 1b.

8. t<sub>HZCS</sub> is tested with load shown in Figure 1b. Transition is measured at steady state High level + 500 mV or steady state Low level + 500 mV on the output from the 1.5V level on the input.

Typical DC and AC Characteristics

3

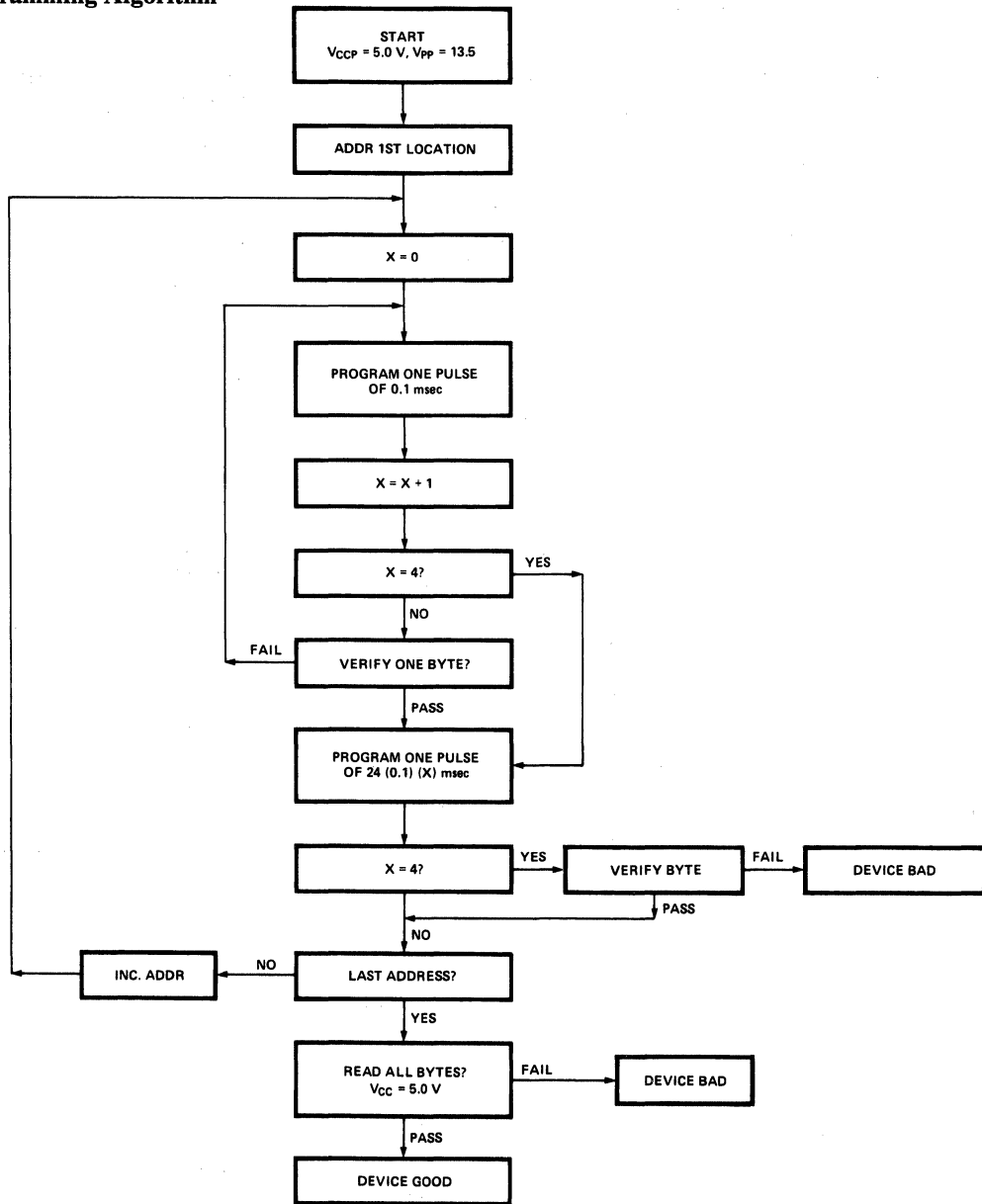


0009-9

Figure 3. Programming Pinout

0009-8

## Programming Algorithm



0009-10

The CY7C281 and CY7C282 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4*.

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the PGM pulse ( $t_{pp}$ ) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verification is performed at  $V_{CC} = 5.0$ . When all bytes have been programmed all bytes should be compared (Read mode) to original data with  $V_{CC} = 5.0V$ .

**Figure 4. Programming Flowchart**

## Programming Information

The 7C281 and 7C282 1K x 8 CMOS PROMs are implemented with a differential EPROM memory cell. The PROMs are delivered in an erased state, containing neither "1s" nor "0s". This erased condition of the array may be assessed using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see below.

## Blank Check

A virgin device contains neither ones nor zeros because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 1023. A device is considered virgin if all locations are respectively "1s" and "0s" when addressed in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both ones and zeros. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

**3**

## DC Programming Parameters $T_A = 25^\circ\text{C}$

**Table 1**

| Parameter        | Description                        | Min. | Max. | Units |
|------------------|------------------------------------|------|------|-------|
| V <sub>PP</sub>  | Programming Voltage <sup>[1]</sup> | 13.0 | 14.0 | V     |
| V <sub>CCP</sub> | Supply Voltage                     | 4.75 | 5.25 | V     |
| V <sub>IHP</sub> | Input HIGH Voltage                 | 3.0  |      | V     |
| V <sub>ILP</sub> | Input LOW Voltage                  |      | 0.4  | V     |
| V <sub>OH</sub>  | Output HIGH Voltage <sup>[2]</sup> | 2.4  |      | V     |
| V <sub>OL</sub>  | Output LOW Voltage <sup>[2]</sup>  |      | 0.4  | V     |
| I <sub>PP</sub>  | Programming Supply Current         |      | 50   | mA    |

## AC Programming Parameters $T_A = 25^\circ\text{C}$

**Table 2**

| Parameter                       | Description                                       | Min. | Max.   | Units |
|---------------------------------|---|------|--------|-------|
| t <sub>PP</sub>                 | Programming Pulse Width <sup>[3]</sup>            | 100  | 10,000 | μs    |
| t <sub>AS</sub>                 | Address Setup Time                                | 1.0  |        | μs    |
| t <sub>DS</sub>                 | Data Setup Time                                   | 1.0  |        | μs    |
| t <sub>AH</sub>                 | Address Hold Time                                 | 1.0  |        | μs    |
| t <sub>DH</sub>                 | Data Hold Time                                    | 1.0  |        | μs    |
| t <sub>R</sub> , t <sub>F</sub> | V <sub>PP</sub> Rise and Fall Time <sup>[3]</sup> | 1.0  |        | μs    |
| t <sub>VD</sub>                 | Delay to Verify                                   | 1.0  |        | μs    |
| t <sub>VP</sub>                 | Verify Pulse Width                                | 2.0  |        | μs    |
| t <sub>DV</sub>                 | Verify Data Valid                                 |      | 1.0    | μs    |
| t <sub>DZ</sub>                 | Verify to High Z                                  |      | 1.0    | μs    |

**Notes:**

1. V<sub>CCP</sub> must be applied prior to V<sub>PP</sub>.
2. During verify operation.

3. Measured 10% and 90% points.



**Mode Selection**
**Table 3**

| Mode                          | Pin Function           |                  |                  |                          |                  | Outputs<br>(9-11, 13-17) |
|-------------------------------|------------------------|------------------|------------------|--------------------------|------------------|--------------------------|
|                               | Read or Output Disable | CS <sub>4</sub>  | CS <sub>3</sub>  | $\overline{\text{CS}}_2$ | CS <sub>1</sub>  |                          |
|                               | Other                  | PGM              | VFY              | V <sub>PP</sub>          | CS <sub>1</sub>  |                          |
|                               | Pin Number             | (18)             | (19)             | (20)                     | (21)             |                          |
| Read                          |                        | V <sub>IH</sub>  | V <sub>IH</sub>  | V <sub>IL</sub>          | V <sub>IL</sub>  | Data Out                 |
| Output Disable <sup>[4]</sup> | X                      | X                | V <sub>IH</sub>  | X                        | X                | High Z                   |
| Output Disable <sup>[4]</sup> | X                      | V <sub>IL</sub>  | X                | X                        | X                | High Z                   |
| Output Disable <sup>[4]</sup> | V <sub>IL</sub>        | X                | X                | X                        | X                | High Z                   |
| Output Disable <sup>[4]</sup> | X                      | X                | X                | V <sub>IH</sub>          | X                | High Z                   |
| Program                       |                        | V <sub>ILP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>          | V <sub>ILP</sub> | Data In                  |
| Program Verify                |                        | V <sub>IHP</sub> | V <sub>ILP</sub> | V <sub>PP</sub>          | V <sub>ILP</sub> | Data Out                 |
| Program Inhibit               |                        | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>          | V <sub>ILP</sub> | High Z                   |
| Intelligent Program           |                        | V <sub>ILP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>          | V <sub>ILP</sub> | Data In                  |
| Blank Check Ones              |                        | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub>         | V <sub>ILP</sub> | Ones                     |
| Blank Check Zeros             |                        | V <sub>PP</sub>  | V <sub>IHP</sub> | V <sub>ILP</sub>         | V <sub>ILP</sub> | Zeros                    |

**Notes:**

4. X = Don't care but not to exceed V<sub>CC</sub> + 5%.

5. During programming and verification, all unspecified pins to be at V<sub>ILP</sub>.

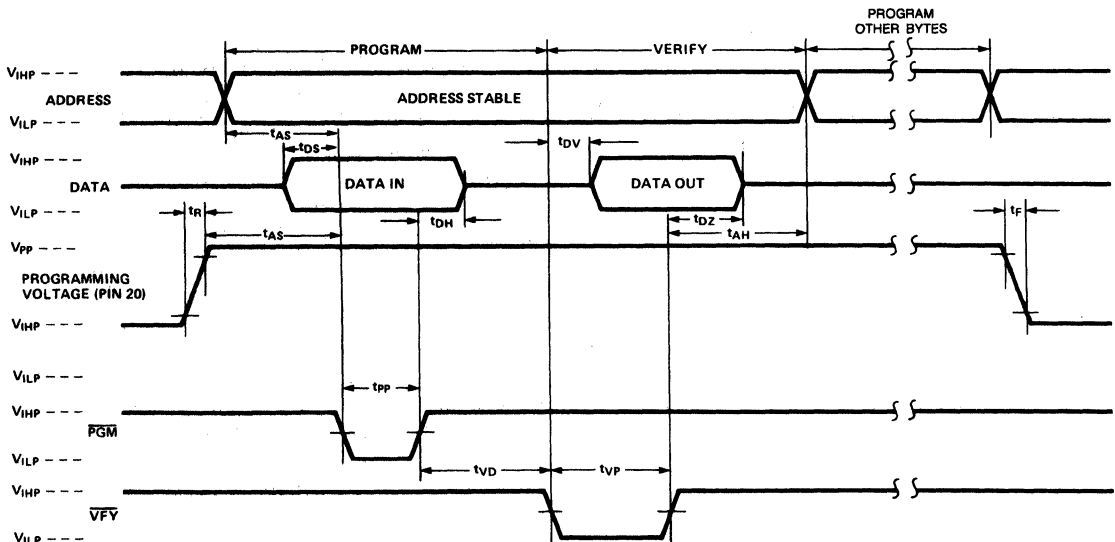
**Programming Sequence 1K x 8**

Power the device for normal read mode operation with pin 18, 19, 20, and 21 at V<sub>IH</sub>. Per *Figure 5* take pin 20 to V<sub>PP</sub>. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see Tables 3 and 4. Again per *Figure 5* address program and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each

location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100  $\mu$ s. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24  $\times$  the sum of the previous programming pulses before advancing to the next address to repeat the process.


**Figure 5. Programming Waveforms**

0009-11

**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 30 ns      | CY7C281-30PC  | P13          | Commercial      |
|            | CY7C282-30PC  | P11          |                 |
|            | CY7C281-30DC  | D14          |                 |
|            | CY7C281-30LC  | L64          |                 |
|            | CY7C282-30DC  | D12          |                 |
| 45 ns      | CY7C281-45PC  | P13          | Commercial      |
|            | CY7C282-45PC  | P11          |                 |
|            | CY7C281-45DC  | D14          |                 |
|            | CY7C281-45LC  | L64          |                 |
|            | CY7C282-45DC  | D12          |                 |
|            | CY7C281-45DMB | D14          | Military        |
|            | CY7C281-45LMB | L64          |                 |
|            | CY7C282-45DMB | D12          |                 |

**MILITARY SPECIFICATIONS****Group A Subgroup Testing****DC Characteristics**

| Parameters      | Subgroups |
|-----------------|-----------|
| V <sub>OH</sub> | 1,2,3     |
| V <sub>OL</sub> | 1,2,3     |
| V <sub>IH</sub> | 1,2,3     |
| V <sub>IL</sub> | 1,2,3     |
| I <sub>IX</sub> | 1,2,3     |
| I <sub>OZ</sub> | 1,2,3     |
| I <sub>CC</sub> | 1,2,3     |

**Switching Characteristics**

| Parameters       | Subgroups   |
|------------------|-------------|
| t <sub>AA</sub>  | 7,8,9,10,11 |
| t <sub>ACS</sub> | 7,8,9,10,11 |

Document #: 38-00006-B



**65,536 x 8 PROM**  
**Reprogrammable Fast**  
**Column Access**

**Features**

- CMOS for optimum speed/power
- Windowed for reprogrammability
- Unique fast column access  
— 30 ns  $t_{AA}$  (commercial)  
— 35 ns  $t_{AA}$  (military)
- WAIT signal
- Chip Select Decoding
- EPROM technology, 100% programmable
- 5V  $\pm$  10%  $V_{CC}$ , commercial and military
- TTL compatible I/O
- Slim 300 mil package
- Capable of withstanding  
> 2001V static discharge

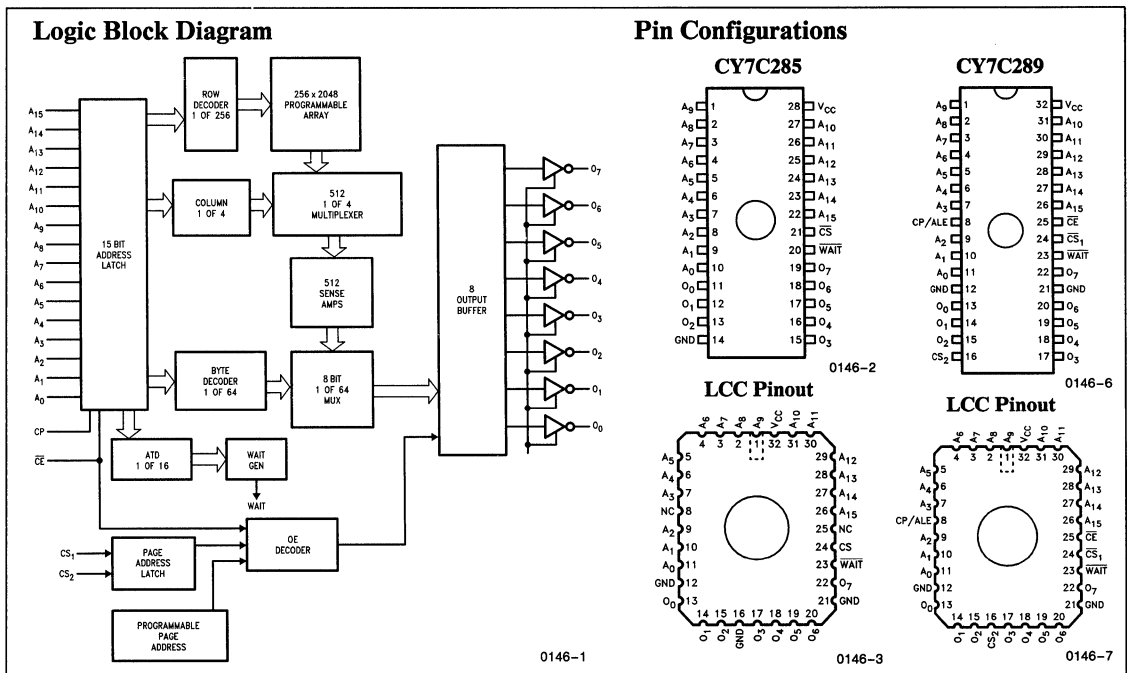
**Product Characteristics**

The CY7C285 and the CY7C289 are high performance 65,536 by 8 bit CMOS PROMs. The CY7C285 is available in a 28-pin 300 mil package. It features a unique fast column access feature which will allow access times as fast as 30 ns for each byte in a 64-byte page. There are 1024 pages in the device. The access time when changing pages will be 75 ns. In order to easily facilitate the use of the fast column access feature, a WAIT signal will be generated to advise the processor of a page change. The WAIT signal may be programmed as either active HIGH or active LOW. The CY7C289 also incorporates the fast column access feature and adds through the use of the ALE option either synchronous address registers or asynchronous address latches. The CY7C289 is particularly well suited to support applications using the CY7C601 as well as other RISC or CISC microprocessors. It is available in a 32-pin 300 mil package.

The CY7C285 and CY7C289 offer the advantage of low power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested, with each location being written into, erased and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading the CY7C285 is accomplished by placing an active LOW signal on the CS pin. Reading the CY7C289 is accomplished by placing an active LOW signal on the CE pin and by placing active HIGH signals on the CS<sub>1</sub> or CS<sub>2</sub> pins as appropriate. The contents of the memory location addressed by the address lines (A<sub>0</sub>–A<sub>15</sub>) will become available on the output lines (O<sub>0</sub>–O<sub>7</sub>).

3





65,536 x 8 PROM  
Reprogrammable Registered

Features

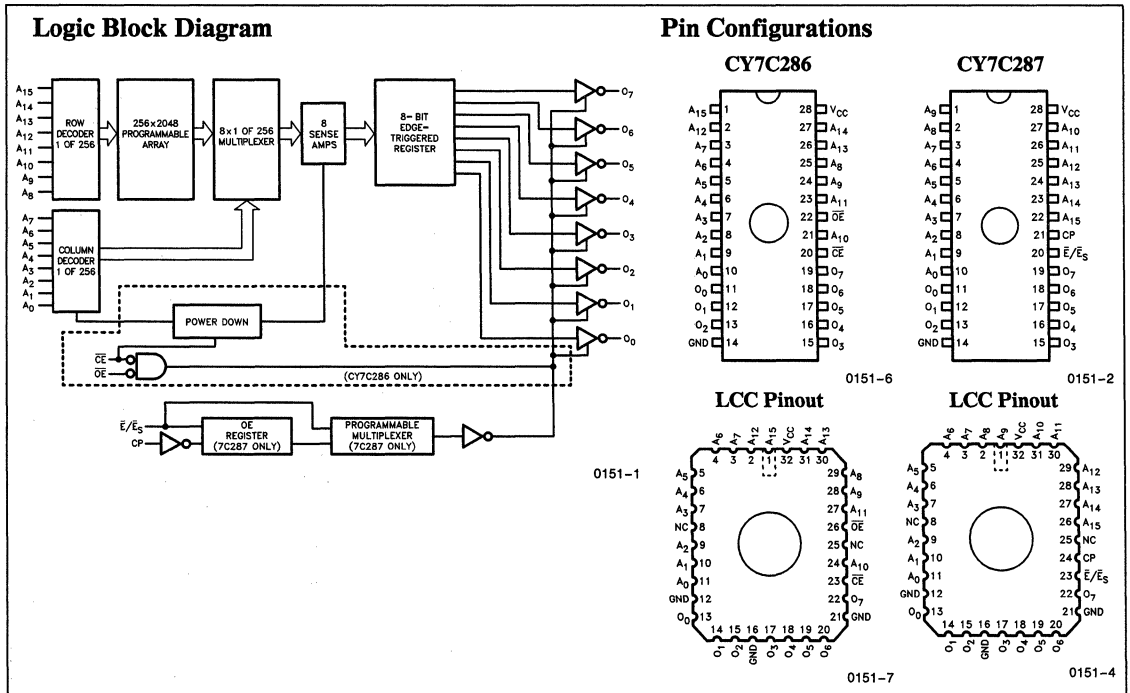
- CMOS for optimum speed/power
- Windowed for reprogrammability
- High speed
  - $t_{SU} = 55$  ns (7C287)
  - $t_{CO} = 20$  ns (7C287)
  - $t_{AA} = 60$  ns (7C286)
- Low power
  - 120 mA active (7C286)
  - 40 mA standby
- WAIT signal
- Chip Select Decoding
- EPROM technology, 100% programmable
- $5V \pm 10\%$   $V_{CC}$ , commercial and military
- TTL compatible I/O
- Slim 300 mil package (7C287)
- Capable of withstanding > 2001V static discharge

Product Characteristics

The CY7C286 and the CY7C287 are high performance 65,536 by 8 bit CMOS PROMs. The CY7C286 is configured in the JEDEC standard 512K EPROM pinout. It is available in a 28-pin, 600 mil package. Power consumption on the CY7C286 will be 120 mA in the active mode and 40 mA in the standby mode. Access time is 60 ns. The CY7C287 has registered outputs and operates in the synchronous mode. It is available in a 28-pin, 300 mil package. The address setup time is 55 ns and the time from clock high to output valid is 20 ns. Both the CY7C286 and CY7C287 are available in a CERDIP package equipped with an erasure window to provide reprogrammability. When exposed to UV light, the PROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C286 and CY7C287 offer the advantage of low power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested, with each location being written into, erased and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading the CY7C286 is accomplished by placing active LOW signals on the  $\overline{OE}$  and  $\overline{CE}$  pins. Reading the CY7C287 is accomplished by placing an active low signal on  $\overline{E}/\overline{ES}$ . The contents of the memory location addressed by the address line ( $A_0 - A_{15}$ ) will become available on the output lines ( $O_0 - O_7$ ).





# Reprogrammable 2048 x 8 PROM

## Features

- Windowed for reprogrammability
- CMOS for optimum speed/power
- High speed
  - 35 ns (commercial)
  - 35 ns (military)
- Low power
  - 330 mW (commercial)
  - 413 mW (military)
- EPROM technology 100% programmable
- Slim 300 mil or standard 600 mil packaging available
- 5V ±10% V<sub>CC</sub>, commercial and military
- TTL compatible I/O
- Direct replacement for bipolar PROMs

- Capable of withstanding > 2000V static discharge

## Product Characteristics

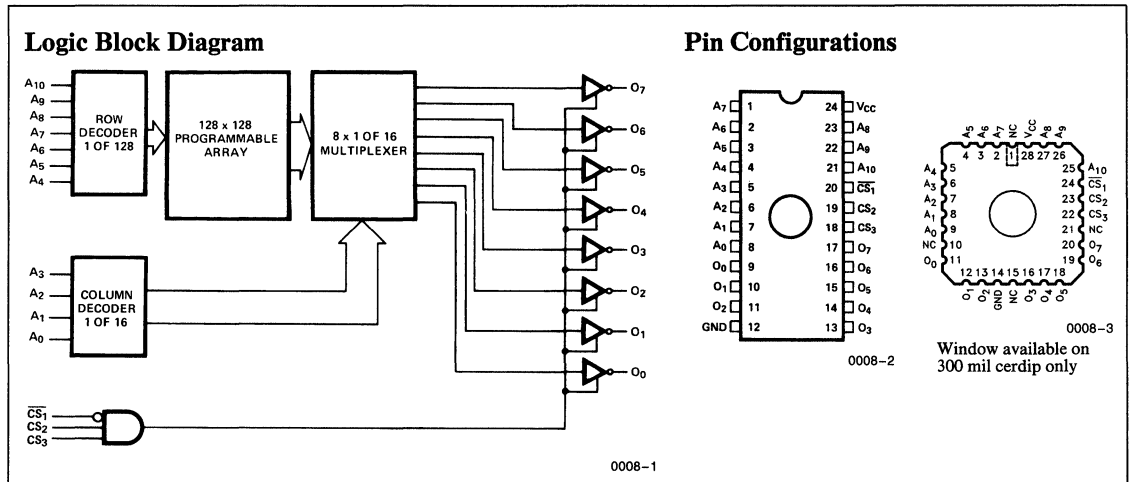
The CY7C291 and CY7C292 are high performance 2048 word by 8 bit CMOS PROMs. They are functionally identical, but are packaged in 300 mil and 600 mil wide plastic and hermetic DIP packages respectively. The 300 mil ceramic DIP package is equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C291 and CY7C292 are plug-in replacements for bipolar devices and offer the advantages of lower power,

reprogrammability, superior performance and programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW signal on  $\overline{CS}_1$ , and active HIGH signals on  $CS_2$  and  $CS_3$ . The contents of the memory location addressed by the address lines ( $A_0$ – $A_{10}$ ) will become available on the output lines ( $O_0$ – $O_7$ ).

3



## Selection Guide

|                                |     | 7C291-35<br>7C292-35 | 7C291-50<br>7C292-50 |
|--------------------------------|-----|----------------------|----------------------|
| Maximum Access Time (ns)       |     | 35                   | 50                   |
| Maximum Operating Current (mA) | STD | Commercial<br>90     | 90                   |
|                                | L   | Military<br>120*     | 120                  |
|                                |     | Commercial<br>60     | 60                   |

\*7C291 only

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|  |                           |
|--|---------------------------|
| Storage Temperature .....                                  | -65°C to +150°C           |
| Ambient Temperature with Power Applied .....               | -55°C to +125°C           |
| Supply Voltage to Ground Potential .... (Pin 24 to Pin 12) | -0.5V to +7.0V            |
| DC Voltage Applied to Outputs in High Z State .....        | -0.5V to +7.0V            |
| DC Input Voltage .....                                     | -3.0V to +7.0V            |
| DC Program Voltage (Pins 18, 20) .....                     | 13.0V                     |
| UV Exposure .....  | 7258 Wsec/cm <sup>2</sup> |

|                                |                                       |
|--------------------------------|---------------------------------------|
| Static Discharge Voltage ..... | >2001V (per MIL-STD-883, Method 3015) |
| Latchup Current .....          | >200 mA                               |

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[6]</sup> | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over the Operating Range<sup>[5]</sup>

| Parameters                     | Description                                 | Test Conditions  | 7C291L-35, 50<br>7C292L-35, 50 |                 | 7C291-35, 50<br>7C292-35, 50 |                 | Units |
|--------------------------------|---|--|--------------------------------|-----------------|------------------------------|-----------------|-------|
|                                |   |  | Min.                           | Max.            | Min.                         | Max.            |       |
| V <sub>OH</sub>                | Output HIGH Voltage                         | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA          | 2.4                            |                 | 2.4                          |                 | V     |
| V <sub>OL</sub>                | Output LOW Voltage                          | V <sub>CC</sub> = Min., I <sub>OL</sub> = 16.0 mA          |                                | 0.4             |                              | 0.4             | V     |
| V <sub>IH</sub> <sup>[1]</sup> | Input HIGH Voltage                          |  | 2.0                            | V <sub>CC</sub> | 2.0                          | V <sub>CC</sub> | V     |
| V <sub>IL</sub> <sup>[1]</sup> | Input LOW Voltage                           |  |                                | 0.8             |                              | 0.8             | V     |
| I <sub>IX</sub>                | Input Load Current                          | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                    | -10                            | +10             | -10                          | +10             | μA    |
| V <sub>CD</sub>                | Input Diode Clamp Voltage                   |  | Note 2                         |                 | Note 2                       |                 |       |
| I <sub>OZ</sub>                | Output Leakage Current                      | GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled | -40                            | +40             | -40                          | +40             | μA    |
| I <sub>OS</sub>                | Output Short Circuit Current <sup>[1]</sup> | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND             | -20                            | -90             | -20                          | -90             | mA    |
| I <sub>CC</sub>                | V <sub>CC</sub> Operating Supply Current    | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA            | Commercial                     | 60              |                              | 90              | mA    |
|                                |   |  | Military*                      |                 |                              | 120             | mA    |

\*-35: 7C291 only

## Capacitance<sup>[4]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 8    |       |

### Notes:

- These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
- The CMOS process does not provide a clamp diode. However, the CY7C291 and CY7C292 are insensitive to -3V dc input levels and -5V undershoot pulses of less than 10 ns (measured at 50% point).
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- See the last page of this specification for Group A subgroup testing information.
- T<sub>A</sub> is the "instant on" case temperature.

### Switching Characteristics Over the Operating Range<sup>[5, 7]</sup>

| Parameters | Description                                   | 7C291-35<br>7C292-35 |      | 7C291-50<br>7C292-50 |      | Units |
|------------|---|----------------------|------|----------------------|------|-------|
|            |   | Min.                 | Max. | Min.                 | Max. |       |
| $t_{AA}$   | Address to Output Valid                       |                      | 35   |                      | 50   | ns    |
| $t_{HZCS}$ | Chip Select Inactive to High Z <sup>[8]</sup> |                      | 25   |                      | 25   | ns    |
| $t_{ACS}$  | Chip Select Active to Output Valid            |                      | 25   |                      | 25   | ns    |

3

### AC Test Loads and Waveforms

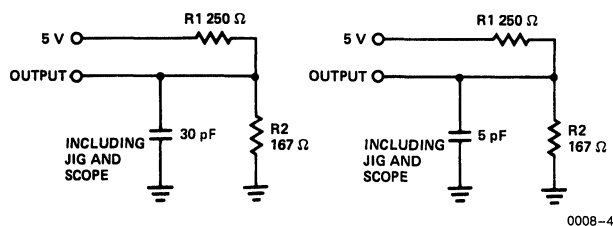


Figure 1a

Figure 1b

0008-4

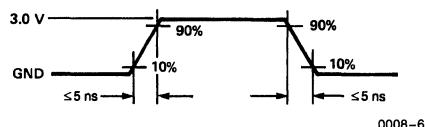
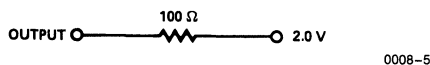


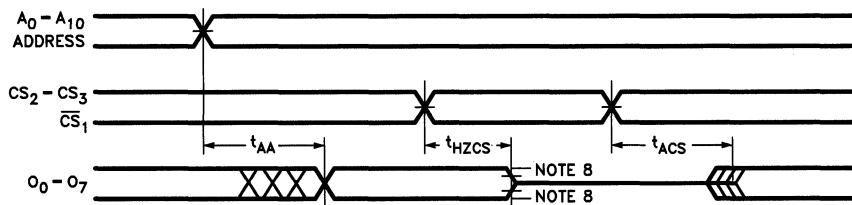
Figure 2. Input Pulses

0008-6

Equivalent to: THÉVENIN EQUIVALENT



0008-5



0008-7

#### Notes:

7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified  $I_{OL}/I_{OH}$  and loads shown in Figures 1a, 1b.

8.  $t_{HZCS}$  is tested with load shown in Figure 1b. Transition is measured at steady state High level - 500 mV or steady state Low level + 500 mV on the output from the 1.5V level on the input.



## Typical DC and AC Characteristics

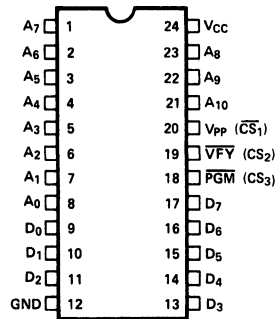
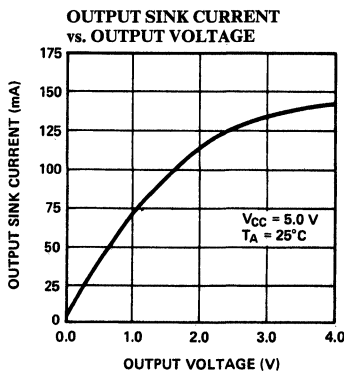
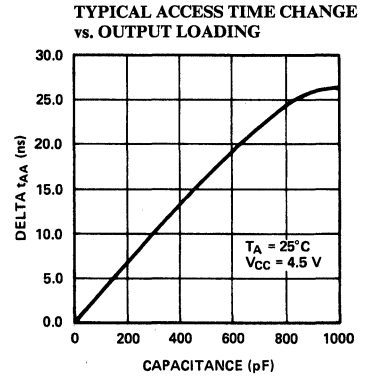
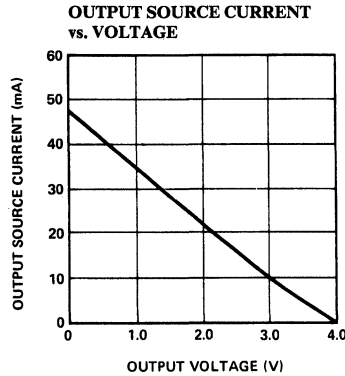
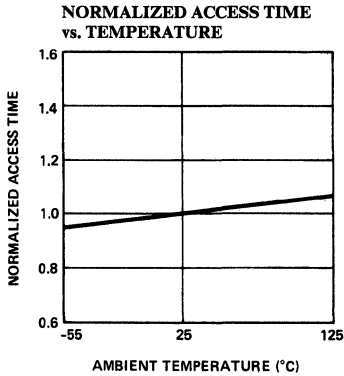
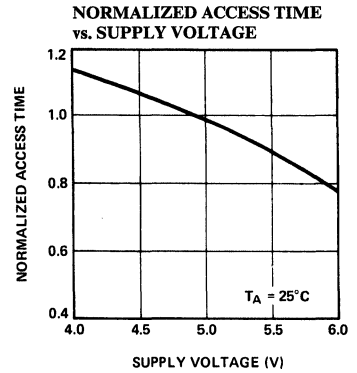
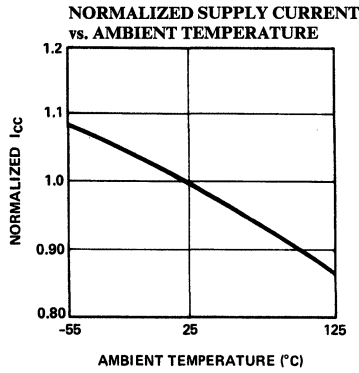
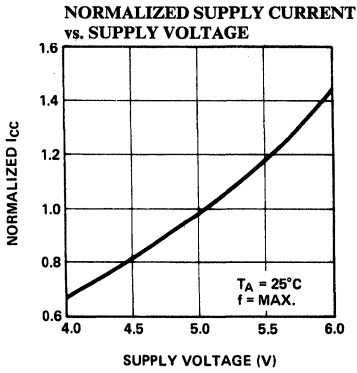
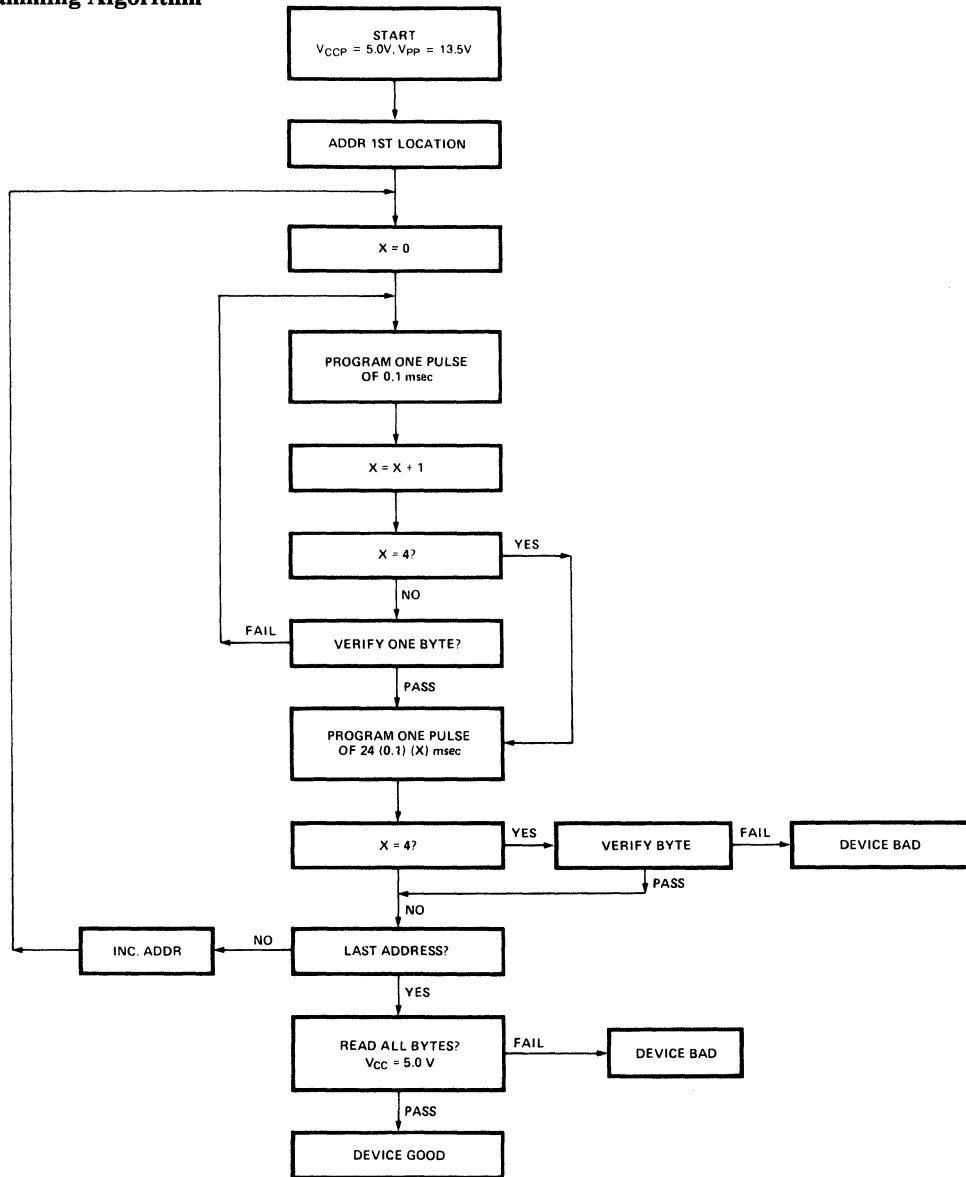


Figure 3. Programming Pinout

0008-9

0008-8

## Programming Algorithm



0008-10

The CY7C291 and CY7C292 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4*.

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the PGM pulse ( $t_{pp}$ ) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verification is performed at  $V_{CCP} = 5.0V$ . When all bytes have been programmed all bytes should be compared (Read mode) to original data with  $V_{CC} = 5.0V$ .

**Figure 4. Programming Flowchart**

## Programming Information

The 7C291 and 7C292 2K x 8 CMOS PROMs are implemented with a differential EPROM memory cell. The PROMs are delivered in an erased state, containing neither "1s" nor "0s". This erased condition of the array may be assessed using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see below.

## Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C291. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity  $\times$  exposure time) of 25 Wsec/cm<sup>2</sup>. For an ultraviolet lamp with a 12 mW/cm<sup>2</sup> power rating the exposure time would be approximately 30-35 minutes.

## DC Programming Parameters $T_A = 25^\circ\text{C}$

| Parameter        | Description                        | Min. | Max. | Units |
|------------------|------------------------------------|------|------|-------|
| V <sub>PP</sub>  | Programming Voltage <sup>[1]</sup> | 12.0 | 13.0 | V     |
| V <sub>CCP</sub> | Supply Voltage                     | 4.75 | 5.25 | V     |
| V <sub>IHP</sub> | Input HIGH Voltage                 | 3.0  |      | V     |
| V <sub>ILP</sub> | Input LOW Voltage                  |      | 0.4  | V     |
| V <sub>OH</sub>  | Output HIGH Voltage <sup>[2]</sup> | 2.4  |      | V     |
| V <sub>OL</sub>  | Output LOW Voltage <sup>[2]</sup>  |      | 0.4  | V     |
| I <sub>PP</sub>  | Programming Supply Current         |      | 50   | mA    |

## AC Programming Parameters $T_A = 25^\circ\text{C}$

| Parameter                       | Description                                       | Min. | Max.   | Units         |
|---------------------------------|---|------|--------|---------------|
| t <sub>PP</sub>                 | Programming Pulse Width <sup>[3]</sup>            | 100  | 10,000 | $\mu\text{s}$ |
| t <sub>AS</sub>                 | Address Setup Time                                | 1.0  |        | $\mu\text{s}$ |
| t <sub>DS</sub>                 | Data Setup Time                                   | 1.0  |        | $\mu\text{s}$ |
| t <sub>AH</sub>                 | Address Hold Time                                 | 1.0  |        | $\mu\text{s}$ |
| t <sub>DH</sub>                 | Data Hold Time                                    | 1.0  |        | $\mu\text{s}$ |
| t <sub>R</sub> , t <sub>F</sub> | V <sub>pp</sub> Rise and Fall Time <sup>[3]</sup> | 1.0  |        | $\mu\text{s}$ |
| t <sub>VD</sub>                 | Delay to Verify                                   | 1.0  |        | $\mu\text{s}$ |
| t <sub>VP</sub>                 | Verify Pulse Width                                | 2.0  |        | $\mu\text{s}$ |
| t <sub>DV</sub>                 | Verify Data Valid                                 |      | 1.0    | $\mu\text{s}$ |
| t <sub>DZ</sub>                 | Verify to High Z                                  |      | 1.0    | $\mu\text{s}$ |

### Notes:

1. V<sub>CCP</sub> must be applied prior to V<sub>pp</sub>.
2. During verify operation.

The 7C291 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258W  $\times$  sec/cm<sup>2</sup> is the recommended maximum dosage.

## Blank Check

A virgin device contains neither ones nor zeros because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In each of these modes, the locations 0 thru 2047 should be addressed and read. A device is considered virgin if all locations are respectively "1s" and "0s" when addressed in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both ones and zeros. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

3. Measured 10% and 90% points.

## Mode Selection

Table 3

| Mode                          | Pin Function           |                  |                  | Outputs<br>(9-11, 13-17) |                 |
|-------------------------------|------------------------|------------------|------------------|--------------------------|-----------------|
|                               | Read or Output Disable | CS <sub>3</sub>  | CS <sub>2</sub>  |                          | CS <sub>1</sub> |
|                               | Other                  | PGM              | VFY              |                          | V <sub>PP</sub> |
|                               | Pin Number             | (18)             | (19)             |                          | (20)            |
| Read                          |                        | V <sub>IH</sub>  | V <sub>IH</sub>  | V <sub>IL</sub>          | Data Out        |
| Output Disable <sup>[4]</sup> | X                      | X                | V <sub>IH</sub>  |                          | High Z          |
| Output Disable <sup>[4]</sup> | X                      | V <sub>IL</sub>  | X                |                          | High Z          |
| Output Disable <sup>[4]</sup> | V <sub>IL</sub>        | X                | X                |                          | High Z          |
| Program                       |                        | V <sub>ILP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>          | Data In         |
| Program Verify                |                        | V <sub>IHP</sub> | V <sub>ILP</sub> | V <sub>PP</sub>          | Data Out        |
| Program Inhibit               |                        | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>          | High Z          |
| Intelligent Program           |                        | V <sub>ILP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>          | Data In         |
| Blank Check Ones              |                        | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub>         | Ones            |
| Blank Check Zeros             |                        | V <sub>PP</sub>  | V <sub>IHP</sub> | V <sub>ILP</sub>         | Zeros           |

**Notes:**

4. X = Don't care but not to exceed  $V_{CC} + 5\%$ .

5. During programming and verification, all unspecified pins to be at V<sub>ILP</sub>.

### Programming Sequence 2K x 8

Power the device for normal read mode operation with pin 18, 19 and 20 at V<sub>IH</sub>. Per Figure 5 take pin 20 to V<sub>PP</sub>. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see Table 3. Again per Figure 5 address, program, and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each

location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24 x the sum of the previous programming pulses before advancing to the next address to repeat the process.

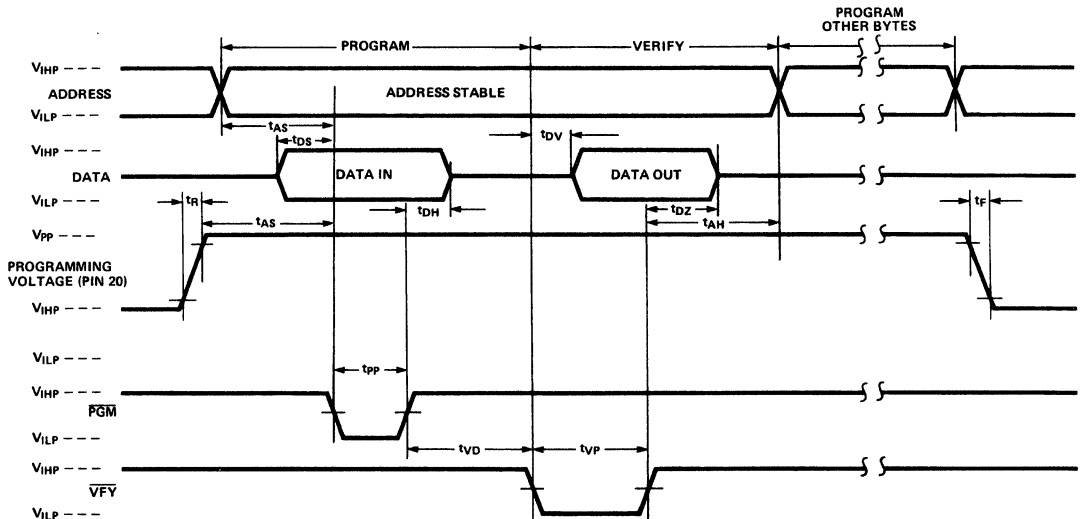


Figure 5. Programming Waveforms

**Ordering Information**

| Speed (ns) | ICC (mA) | Ordering Code | Package Type | Operating Range |          |
|------------|----------|---------------|--------------|-----------------|----------|
| 35         | 60       | CY7C291L-35PC | P13          | Commercial      |          |
|            |          | CY7C291L-35WC | W14          |                 |          |
|            | 90       | CY7C291-35PC  | P13          |                 |          |
|            |          | CY7C291-35SC  | S13          |                 |          |
|            |          | CY7C291-35WC  | W14          |                 |          |
|            |          | CY7C291-35LC  | L64          |                 |          |
|            | 120      | CY7C291-35WMB | W14          |                 | Military |
|            |          | CY7C291-35DMB | D14          |                 |          |
| 50         | 60       | CY7C291L-50PC | P13          | Commercial      |          |
|            |          | CY7C291L-50WC | W14          |                 |          |
|            | 90       | CY7C291-50PC  | P13          |                 |          |
|            |          | CY7C291-50SC  | S13          |                 |          |
|            |          | CY7C291-50WC  | W14          |                 |          |
|            |          | CY7C291-50LC  | L64          |                 |          |
|            | 120      | CY7C291-50WMB | W14          |                 | Military |
|            |          | CY7C291-50DMB | D14          |                 |          |
|            |          | CY7C291-50LMB | L64          |                 |          |
|            |          | CY7C291-50QMB | Q64          |                 |          |

| Speed (ns) | ICC (mA) | Ordering Code | Package Type | Operating Range |          |
|------------|----------|---------------|--------------|-----------------|----------|
| 35         | 60       | CY7C292L-35PC | P11          | Commercial      |          |
|            |          | CY7C292L-35DC | D12          |                 |          |
|            | 90       | CY7C292-35PC  | P11          |                 |          |
|            |          | CY7C292-35DC  | D12          |                 |          |
| 50         | 60       | CY7C292L-50PC | P11          | Commercial      |          |
|            |          | CY7C292L-50DC | D12          |                 |          |
|            | 90       | CY7C292-50PC  | P11          |                 |          |
|            |          | CY7C292-50DC  | D12          |                 |          |
|            | 120      | CY7C292-50DMB | D12          |                 | Military |

**MILITARY SPECIFICATIONS****Group A Subgroup Testing****DC Characteristics**

| Parameters      | Subgroups |
|-----------------|-----------|
| V <sub>OH</sub> | 1,2,3     |
| V <sub>OL</sub> | 1,2,3     |
| V <sub>IH</sub> | 1,2,3     |
| V <sub>IL</sub> | 1,2,3     |
| I <sub>IX</sub> | 1,2,3     |
| I <sub>OZ</sub> | 1,2,3     |
| I <sub>CC</sub> | 1,2,3     |

**3****Switching Characteristics**

| Parameters       | Subgroups   |
|------------------|-------------|
| t <sub>AA</sub>  | 7,8,9,10,11 |
| t <sub>ACS</sub> | 7,8,9,10,11 |

Document #: 38-00007-C



# Reprogrammable 2048 x 8 PROM

## Features

- Windowed for reprogrammability
- CMOS for optimum speed/power
- High speed
  - 25 ns (commercial)
  - 30 ns (military)
- Low power
  - 330 mW (commercial)
  - 660 mW (military)
- Low standby power
  - 165 mW (commercial)
  - 220 mW (military)
- EPROM technology 100% programmable
- Slim 300 mil or standard 600 mil packaging available
- 5V  $\pm$  10% V<sub>CC</sub>, commercial and military
- TTL compatible I/O
- Direct replacement for bipolar PROMs

- Capable of withstanding > 2001V static discharge

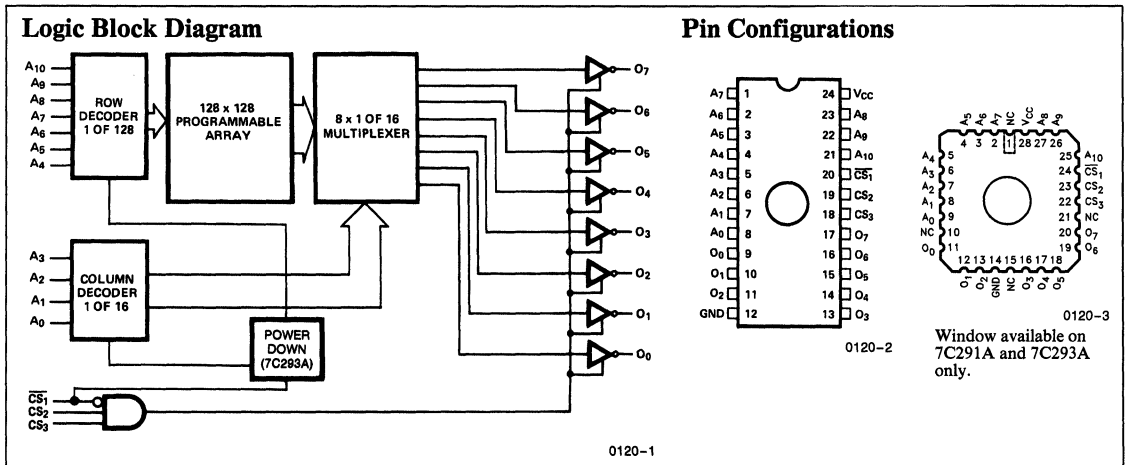
## Product Characteristics

The CY7C291A, CY7C292A, and CY7C293A are high performance 2048 word by 8 bit CMOS PROMs. They are functionally identical, but are packaged in 300 mil (7C291A, 7C293A) and 600 mil wide plastic and hermetic DIP packages (7C292A). The CY7C293A has an automatic power down feature which reduces the power consumption by over 70% when deselected. The 300 mil ceramic DIP package is equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C291A, CY7C292A, and CY7C293A are plug-in replacements

for bipolar devices and offer the advantages of lower power, reprogrammability, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW signal on CS<sub>1</sub>, and active HIGH signals on CS<sub>2</sub> and CS<sub>3</sub>. The contents of the memory location addressed by the address lines (A<sub>0</sub>–A<sub>10</sub>) will become available on the output lines (O<sub>0</sub>–O<sub>7</sub>).



## Selection Guide

|                                     |     | 7C291A-25<br>7C292A-25<br>7C293A-25 | 7C291A-30<br>7C292A-30<br>7C293A-30 | 7C291A-35<br>7C292A-35<br>7C293A-35 | 7C291A-50<br>7C292A-50<br>7C293A-50 |
|-------------------------------------|-----|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|
| Maximum Access Time (ns)            |     | 25                                  | 30                                  | 35                                  | 50                                  |
| Maximum Operating Current (mA)      | STD | Commercial                          | 120                                 | 90                                  | 90                                  |
|                                     |     | Military                            | 120                                 | 120                                 | 120                                 |
| Standby Current (mA)<br>7C293A Only | L   | Commercial                          |                                     | 60                                  | 60                                  |
|                                     |     | Commercial                          | 30                                  | 30                                  | 30                                  |
|                                     |     | Military                            | 40                                  | 40                                  | 40                                  |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                           |
|---|---------------------------|
| Storage Temperature .....                           | -65°C to +150°C           |
| Ambient Temperature with Power Applied .....        | -55°C to +125°C           |
| Supply Voltage to Ground Potential .....            | -0.5V to +7.0V            |
| DC Voltage Applied to Outputs in High Z State ..... | -0.5V to +7.0V            |
| DC Input Voltage .....                              | -3.0V to +7.0V            |
| DC Program Voltage .....                            | 13.0V                     |
| UV Exposure .....                                   | 7258 Wsec/cm <sup>2</sup> |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | > 2001V (per MIL-STD-883, Method 3015) |
| Latchup Current .....          | > 200 mA                               |

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[5]</sup> | -55°C to +125°C     | 5V ± 10%        |

**3**

## Electrical Characteristics Over the Operating Range<sup>[6]</sup>

| Parameters      | Description                                 | Test Conditions  | 7C291A-25 7C291A-30 7C291AL-35, 50 7C291A-35, 50 7C292A-25 7C292A-30 7C292AL-35, 50 7C292A-35, 50 7C293A-25 7C293A-30 7C293AL-35, 50 7C293A-35, 50 |                 |        |                 |        |                 |        |                 | Units  |                 |      |      |  |
|-----------------|---|--|--|-----------------|--------|-----------------|--------|-----------------|--------|-----------------|--------|-----------------|------|------|--|
|                 |   |  | Min.   |                 | Max.   |                 | Min.   |                 | Max.   |                 |        | Min.            |      | Max. |  |
|                 |   |  | Min.   | Max.            | Min.   | Max.            | Min.   | Max.            | Min.   | Max.            |        | Min.            | Max. |      |  |
| V <sub>OH</sub> | Output HIGH Voltage                         | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA          | 2.4  |                 | 2.4    |                 | 2.4    |                 | 2.4    |                 | 2.4    |                 | V    |      |  |
| V <sub>OL</sub> | Output LOW Voltage                          | V <sub>CC</sub> = Min., I <sub>OL</sub> = -16.0 mA         |  | 0.4             |        | 0.4             |        | 0.4             |        | 0.4             |        | 0.4             | V    |      |  |
| V <sub>IH</sub> | Input HIGH Voltage                          |  | 2.0  | V <sub>CC</sub> | 2.0    | V <sub>CC</sub> | 2.0    | V <sub>CC</sub> | 2.0    | V <sub>CC</sub> | 2.0    | V <sub>CC</sub> | V    |      |  |
| V <sub>IL</sub> | Input LOW Voltage                           |  |  | 0.8             |        | 0.8             |        | 0.8             |        | 0.8             |        | 0.8             | V    |      |  |
| I <sub>IX</sub> | Input Load Current                          | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                    | -10  | +10             | -10    | +10             | -10    | +10             | -10    | +10             | -10    | +10             | μA   |      |  |
| V <sub>CD</sub> | Input Diode Clamp Voltage                   |  | Note 2   |                 | Note 2 |                 | Note 2 |                 | Note 2 |                 | Note 2 |                 |      |      |  |
| I <sub>OZ</sub> | Output Leakage Current                      | GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled | -40  | +40             | -40    | +40             | -40    | +40             | -40    | +40             | -40    | +40             | μA   |      |  |
| I <sub>OS</sub> | Output Short Circuit Current <sup>[1]</sup> | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND             | -20  | -90             | -20    | -90             | -20    | -90             | -20    | -90             | -20    | -90             | mA   |      |  |
| I <sub>CC</sub> | V <sub>CC</sub> Operating Supply Current    | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA            | Commercial   |                 | 120    |                 |        |                 | 60     |                 | 90     |                 | mA   |      |  |
|                 |   | Military   |  |                 |        | 120             |        |                 |        | 120             |        | mA              |      |      |  |
| I <sub>SB</sub> | Standby Supply Current (7C293A Only)        | V <sub>CC</sub> = Max., CS <sub>1</sub> ≥ V <sub>IH</sub>  | Commercial   |                 | 30     |                 |        |                 | 30     |                 | 30     |                 | mA   |      |  |
|                 |   | Military   |  |                 |        | 40              |        |                 |        | 40              |        | mA              |      |      |  |

## Capacitance<sup>[4]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 8    |       |

### Notes:

- These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
- The CMOS process does not provide a clamp diode. However, the CY7C291A, CY7C292A and CY7C293A are insensitive to -3V dc input levels and -5V undershoot pulses of less than 10 ns (measured at 50% point).
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.



### Switching Characteristics Over the Operating Range<sup>[6, 7]</sup>

| Parameters   | Description  | 7C291A-25<br>7C292A-25<br>7C293A-25 |                         | 7C291A-30<br>7C292A-30<br>7C293A-30 |      | 7C291A-35<br>7C292A-35<br>7C293A-35 |      | 7C291A-50<br>7C292A-50<br>7C293A-50 |      | Units |
|--------------|--|-------------------------------------|-------------------------|-------------------------------------|------|-------------------------------------|------|-------------------------------------|------|-------|
|              |  | Min.                                | Max.                    | Min.                                | Max. | Min.                                | Max. | Min.                                | Max. |       |
|              |  | $t_{AA}$                            | Address to Output Valid |                                     | 25   |                                     | 30   |                                     | 35   |       |
| $t_{HZCS_1}$ | Chip Select Inactive to High Z <sup>[8]</sup>  |                                     | 20                      |                                     | 20   |                                     | 25   |                                     | 25   | ns    |
| $t_{ACS_1}$  | Chip Select Active to Output Valid   |                                     | 20                      |                                     | 20   |                                     | 25   |                                     | 25   | ns    |
| $t_{HZCS_2}$ | Chip Select Inactive to High Z <sup>[9]</sup><br>(7C293A $\overline{CS}_1$ Only)     |                                     | 27                      |                                     | 32   |                                     | 35   |                                     | 45   | ns    |
| $t_{ACS_2}$  | Chip Select Active to Output Valid<br>(7C293A $\overline{CS}_1$ Only) <sup>[9]</sup> |                                     | 27                      |                                     | 32   |                                     | 35   |                                     | 45   | ns    |
| $t_{PU}$     | Chip Select Active to Power Up<br>(7C293A $\overline{CS}_1$ Only)                    | 0                                   |                         | 0                                   |      | 0                                   |      | 0                                   |      | ns    |
| $t_{PD}$     | Chip Select Inactive to Power Down<br>(7C293A $\overline{CS}_1$ Only)                |                                     | 27                      |                                     | 32   |                                     | 35   |                                     | 45   | ns    |

### AC Test Loads and Waveforms

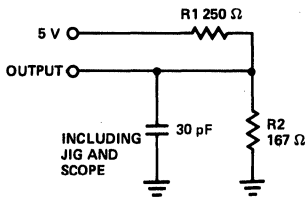


Figure 1a

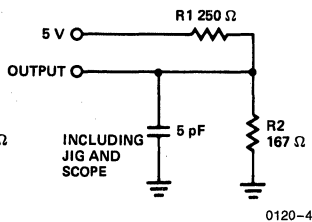


Figure 1b

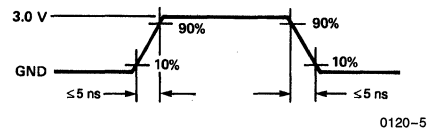
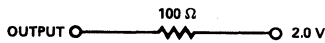
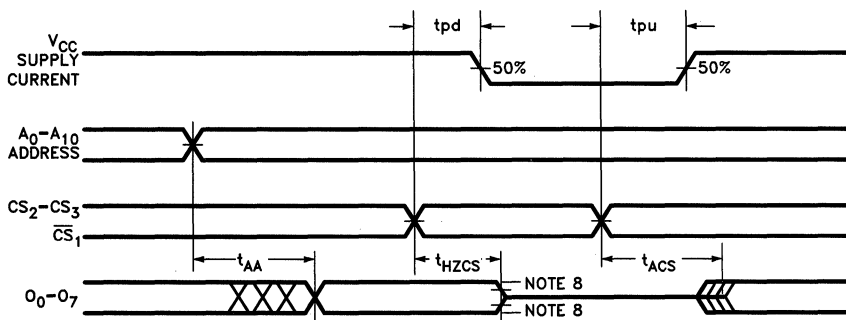


Figure 2. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



0120-6



0120-7

#### Notes:

7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified  $I_{OL}/I_{OH}$  and loads shown in Figures 1a, 1b.

8.  $t_{HZCS}$  is tested with load shown in Figure 1b. Transition is measured at steady state High level  $-500\text{ mV}$  or steady state Low level  $+500\text{ mV}$  on the output from the 1.5V level on the input.

9.  $t_{HZCS_2}$  and  $t_{ACS_2}$  refer to 7C293A  $\overline{CS}_1$  only.

### Typical DC and AC Characteristics

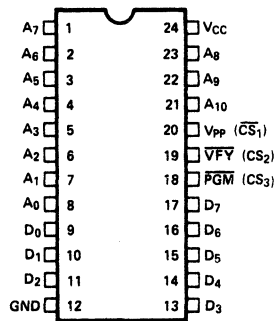
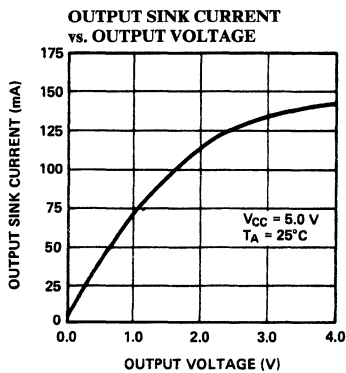
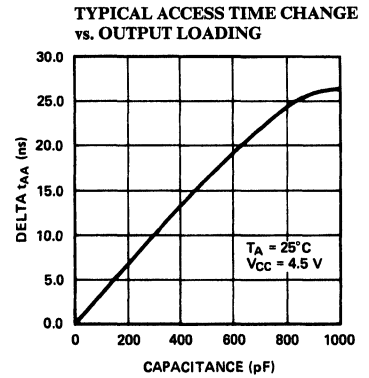
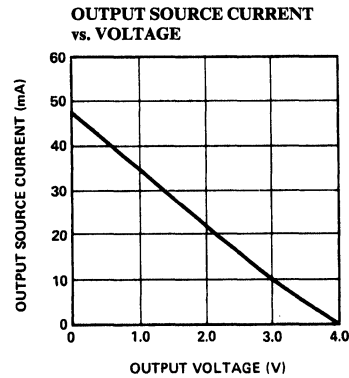
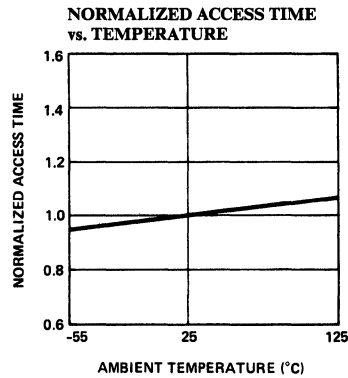
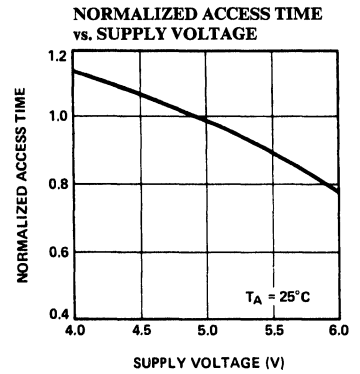
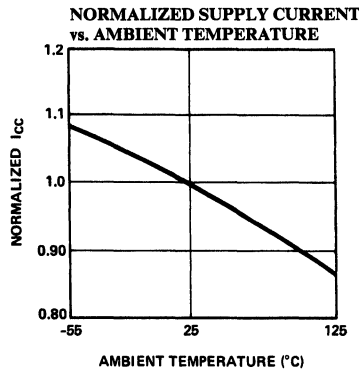
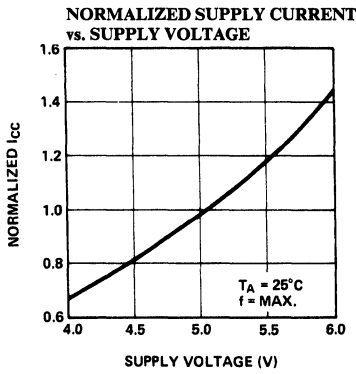
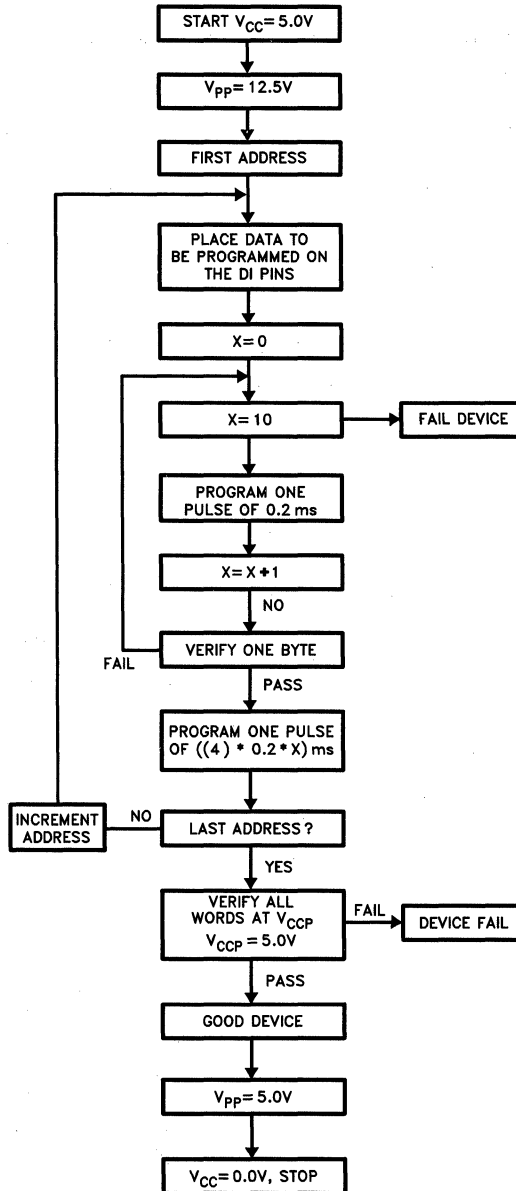


Figure 3. Programming Pinout

0120-10

0120-9

## Programming Algorithm



0120-8

The CY7C291A, CY7C292A and CY7C293A programming algorithm allows significantly faster programming than the "worst case" specification of 10 ms.

Typical programming time for a byte is less than 2.5 ms. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4*.

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the PGM pulse ( $t_{pp}$ ) is 0.1 ms which will then be followed by a longer overprogram pulse of 24 (0.1) (X) ms. X is an iteration counter and is equal to the NUMBER of the initial 0.1 ms pulses applied before verification occurs. Up to four 0.1 ms pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verification is performed at  $V_{CCP} = 5.0V$ . When all bytes have been programmed all bytes should be compared (Read mode) to original data with  $V_{CC} = 5.0V$ .

**Figure 4. Programming Flowchart**

## Programming Information

The 7C291A, 7C292A and 7C293A 2K x 8 CMOS PROMs are implemented with a single ended EPROM memory cell. The PROMs are delivered in an erased state, containing "0s". To verify that a PROM is unprogrammed, use the verify mode provided in Table 3. The locations 0 thru 2047 should be addressed and read.

## Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase these PROMs. For this reason, an opaque label should be placed over the window if the PROM is exposed

to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity  $\times$  exposure time) of 25 Wsec/cm<sup>2</sup>. For an ultraviolet lamp with a 12 mW/cm<sup>2</sup> power rating the exposure time would be approximately 30-35 minutes.

These PROMs need to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258W  $\times$  sec/cm<sup>2</sup> is the recommended maximum dosage.

## DC Programming Parameters T<sub>A</sub> = 25°C

**Table 1**

| Parameter        | Description                        | Min. | Max. | Units |
|------------------|------------------------------------|------|------|-------|
| V <sub>PP</sub>  | Programming Voltage <sup>[1]</sup> | 12.0 | 13.0 | V     |
| V <sub>CCP</sub> | Supply Voltage                     | 4.75 | 5.25 | V     |
| V <sub>IHP</sub> | Input HIGH Voltage                 | 3.0  |      | V     |
| V <sub>ILP</sub> | Input LOW Voltage                  |      | 0.4  | V     |
| V <sub>OH</sub>  | Output HIGH Voltage <sup>[2]</sup> | 2.4  |      | V     |
| V <sub>OL</sub>  | Output LOW Voltage <sup>[2]</sup>  |      | 0.4  | V     |
| I <sub>PP</sub>  | Programming Supply Current         |      | 50   | mA    |

## AC Programming Parameters T<sub>A</sub> = 25°C

**Table 2**

| Parameter                       | Description                                       | Min. | Max.   | Units |
|---------------------------------|---|------|--------|-------|
| t <sub>PP</sub>                 | Programming Pulse Width <sup>[3]</sup>            | 100  | 10,000 | μs    |
| t <sub>AS</sub>                 | Address Setup Time                                | 1.0  |        | μs    |
| t <sub>DS</sub>                 | Data Setup Time                                   | 1.0  |        | μs    |
| t <sub>AH</sub>                 | Address Hold Time                                 | 1.0  |        | μs    |
| t <sub>DH</sub>                 | Data Hold Time                                    | 1.0  |        | μs    |
| t <sub>R</sub> , t <sub>F</sub> | V <sub>PP</sub> Rise and Fall Time <sup>[3]</sup> | 1.0  |        | μs    |
| t <sub>VD</sub>                 | Delay to Verify                                   | 1.0  |        | μs    |
| t <sub>VP</sub>                 | Verify Pulse Width                                | 2.0  |        | μs    |
| t <sub>DV</sub>                 | Verify Data Valid                                 |      | 1.0    | μs    |
| t <sub>DZ</sub>                 | Verify to High Z                                  |      | 1.0    | μs    |

**Notes:**

1. V<sub>CCP</sub> must be applied prior to V<sub>PP</sub>.
2. During verify operation.

3. Measured 10% and 90% points.

## Mode Selection

Table 3

| Mode                          | Pin Function           |                  |                  |                 | Outputs<br>(9-11, 13-17) |
|-------------------------------|------------------------|------------------|------------------|-----------------|--------------------------|
|                               | Read or Output Disable | CS <sub>3</sub>  | CS <sub>2</sub>  | CS <sub>1</sub> |                          |
|                               | Other                  | PGM              | VFY              | VPP             |                          |
|                               | Pin Number             | (18)             | (19)             | (20)            |                          |
| Read                          |                        | V <sub>IH</sub>  | V <sub>IH</sub>  | V <sub>IL</sub> | Data Out                 |
| Output Disable <sup>[4]</sup> | X                      | X                | V <sub>IH</sub>  |                 | High Z                   |
| Output Disable <sup>[4]</sup> | X                      | V <sub>IL</sub>  | X                |                 | High Z                   |
| Output Disable <sup>[4]</sup> | V <sub>IL</sub>        | X                | X                |                 | High Z                   |
| Program                       |                        | V <sub>ILP</sub> | V <sub>IHP</sub> | V <sub>PP</sub> | Data In                  |
| Program Verify                |                        | V <sub>IHP</sub> | V <sub>ILP</sub> | V <sub>PP</sub> | Data Out                 |
| Program Inhibit               |                        | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub> | High Z                   |
| Intelligent Program           |                        | V <sub>ILP</sub> | V <sub>IHP</sub> | V <sub>PP</sub> | Data In                  |

**Notes:**

4. X = Don't care but not to exceed V<sub>CC</sub> + 5%.

5. During programming and verification, all unspecified pins to be at V<sub>ILP</sub>.

### Programming Sequence 2K x 8

Power the device for normal read mode operation with pin 18, 19 and 20 at V<sub>IH</sub>. Per *Figure 5* take pin 20 to V<sub>PP</sub>. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see Table 3. Again per *Figure 5* address, program, and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each

location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 200 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 10 times. When the location verifies, one additional programming pulse should be applied of duration 4 x the sum of the previous programming pulses before advancing to the next address to repeat the process.

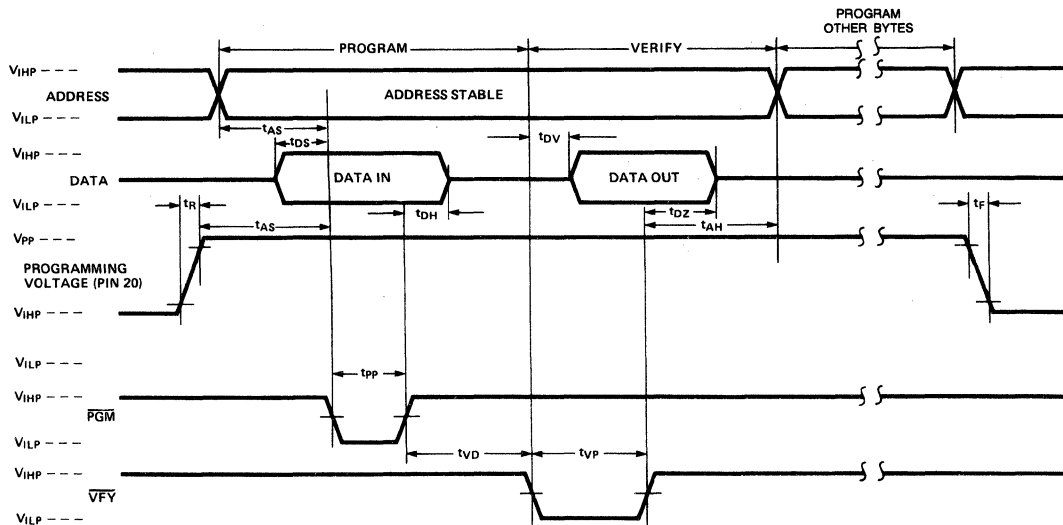


Figure 5. Programming Waveforms

### Ordering Information

| Speed (ns) | ICC (mA)       | Ordering Code  | Package Type  | Operating Range |
|------------|----------------|----------------|---------------|-----------------|
| 25         | 120            | CY7C291A-25PC  | P13           | Commercial      |
|            |                | CY7C291A-25WC  | W14           |                 |
|            |                | CY7C292A-25PC  | P11           |                 |
|            |                | CY7C292A-25DC  | D12           |                 |
|            |                | CY7C293A-25PC  | P13           |                 |
|            |                | CY7C293A-25WC  | W14           |                 |
| 30         | 120            | CY7C291A-30DMB | D14           | Military        |
|            |                | CY7C291A-30WMB | W14           |                 |
|            |                | CY7C291A-30LMB | L64           |                 |
|            |                | CY7C291A-30QMB | Q64           |                 |
|            |                | CY7C292A-30DMB | D12           |                 |
|            |                | CY7C293A-30DMB | D14           |                 |
|            |                | CY7C293A-30WMB | W14           |                 |
|            |                | CY7C293A-30LMB | L64           |                 |
|            |                | CY7C293A-30QMB | Q64           |                 |
| 35         | 60             | CY7C291AL-35PC | P13           | Commercial      |
|            |                | CY7C291AL-35WC | W14           |                 |
|            |                | CY7C292AL-35PC | P11           |                 |
|            |                | CY7C293AL-35PC | P13           |                 |
|            |                | CY7C293AL-35WC | W14           |                 |
|            | 90             | Commercial     | CY7C291A-35PC | P13             |
|            |                |                | CY7C291A-35DC | D14             |
|            |                |                | CY7C291A-35WC | W14             |
|            |                |                | CY7C291A-35LC | L64             |
|            |                |                | CY7C292A-35PC | P11             |
|            |                |                | CY7C292A-35DC | D12             |
|            |                |                | CY7C293A-35PC | P13             |
|            |                |                | CY7C293A-35DC | D14             |
|            |                |                | CY7C293A-35WC | W14             |
|            |                |                | CY7C293A-35LC | L64             |
|            |                |                | 120           | Military        |
|            | CY7C291A-35WMB | W14            |               |                 |
|            | CY7C291A-35LMB | L64            |               |                 |
|            | CY7C291A-35QMB | Q64            |               |                 |
|            | CY7C292A-35DMB | D12            |               |                 |
|            | CY7C293A-35DMB | D14            |               |                 |
|            | CY7C293A-35WMB | W14            |               |                 |
|            | CY7C293A-35LMB | L64            |               |                 |
|            | CY7C293A-35QMB | Q64            |               |                 |

| Speed (ns)    | ICC (mA) | Ordering Code  | Package Type | Operating Range |
|---------------|----------|----------------|--------------|-----------------|
| 50            | 60       | CY7C291AL-50PC | P13          | Commercial      |
|               |          | CY7C291AL-50WC | W14          |                 |
|               |          | CY7C292AL-50PC | P11          |                 |
|               |          | CY7C293AL-50PC | P13          |                 |
|               |          | CY7C293AL-50WC | W14          |                 |
|               |          | 90             | Commercial   |                 |
| CY7C291A-50DC | D14      |                |              |                 |
| CY7C291A-50WC | W14      |                |              |                 |
| CY7C291A-50LC | L64      |                |              |                 |
| CY7C292A-50PC | P11      |                |              |                 |
| CY7C292A-50DC | D12      |                |              |                 |
| CY7C293A-50PC | P13      |                |              |                 |
| CY7C293A-50DC | D14      |                |              |                 |
| CY7C293A-50WC | W14      |                |              |                 |
| CY7C293A-50LC | L64      |                |              |                 |
| 120           | Military |                |              | CY7C291A-50DMB  |
|               |          | CY7C291A-50WMB | W14          |                 |
|               |          | CY7C291A-50LMB | L64          |                 |
|               |          | CY7C291A-50QMB | Q64          |                 |
|               |          | CY7C292A-50DMB | D12          |                 |
|               |          | CY7C293A-50DMB | D14          |                 |
|               |          | CY7C293A-50WMB | W14          |                 |
|               |          | CY7C293A-50LMB | L64          |                 |
|               |          | CY7C293A-50QMB | Q64          |                 |

3

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters                     | Subgroups |
|--------------------------------|-----------|
| V <sub>OH</sub>                | 1,2,3     |
| V <sub>OL</sub>                | 1,2,3     |
| V <sub>IH</sub>                | 1,2,3     |
| V <sub>IL</sub>                | 1,2,3     |
| I <sub>IX</sub>                | 1,2,3     |
| I <sub>OZ</sub>                | 1,2,3     |
| I <sub>CC</sub>                | 1,2,3     |
| I <sub>SB</sub> <sup>[2]</sup> | 1,2,3     |

#### Switching Characteristics

| Parameters                       | Subgroups   |
|----------------------------------|-------------|
| t <sub>AA</sub>                  | 7,8,9,10,11 |
| t <sub>ACS1</sub> <sup>[1]</sup> | 7,8,9,10,11 |
| t <sub>ACS2</sub> <sup>[2]</sup> | 7,8,9,10,11 |

Notes:

1. 7C291A and 7C292A only.
2. 7C293A only.

Document #: 38-00075-B

## Introduction

PROMs or Programmable Read Only Memories have existed since the early 1970's and continue to provide the highest speed non-volatile form of semiconductor memory available. Until the introduction of CMOS PROMs from Cypress, all PROMs were produced in bipolar technology, because bipolar technology provided the highest possible performance at an acceptable cost level. All bipolar PROMs use a fuse for the programming element. The fuses are in tact when the product is delivered to the user, and may be programmed or written once with a pattern and used or read infinitely. The fuses are literally blown using a high current supplied by a Programming System. Since the fuses may only be blown or programmed once, they may not be programmed during test. In addition, since they may not be programmed until the user determines the pattern, they may not be completely tested prior to shipment from the supplier. This inability to completely test, results in less than 100% yield during programming and use by the customer for two reasons. First, some percentage of the product fails to program. These devices fall out during the programming operation, and although a nuisance are easily identified. Additional yield is lost because the device fails to perform even though it programs correctly. This failure is normally due to the device being too slow. This is a more subtle failure, and can only be found by 100% post program AC testing, or even worse by trouble shooting an assembled board or system.

Cypress CMOS PROMs use an EPROM programming mechanism. This technology has been in use in MOS technologies since the early 1970s. However, as with most MOS technologies the emphasis has been on density, not performance. CMOS at Cypress is as fast as or faster than Bipolar and coupled with EPROM, becomes a viable alternative to bipolar PROMs from a performance point-of-view. In the arena of programming, EPROM has some significant advantages over fuse technology. EPROM cells are programmed by injecting charge on an isolated gate which permanently turns off the transistor. This mechanism can be reversed by irradiating the device with ultraviolet light. The fact that programming can be erased, totally changes the testing and programming situation and philosophy. All cells can be programmed during the manufacturing process and then erased prior to packaging and subsequent shipment. While these cells are programmed, the performance of each cell in the memory can be tested allowing the shipment of devices that program every time, and will perform as specified when programmed. In addition when these devices are supplied in a windowed package they can be programmed and erased indefinitely providing the designer a RE-PROGRAMMABLE PROM for development.

## Programmable Technology

### EPROM Process Technology

EPROM technology employs a floating or isolated gate between the normal control gate and the source/drain region of a transistor. This gate may be charged with electrons during the programming operation and when charged with electrons, the transistor is permanently turned off. When uncharged (the transistor is unprogrammed) the device may be turned on and off normally

with the control gate. The state of the floating gate, charged or uncharged, is permanent because the gate is isolated in an extremely pure oxide. The charge may be removed if the device is irradiated with ultraviolet energy in the form of light. This ultraviolet light allows the electrons on the gate to recombine and discharge the gate. This process is repeatable and therefore can be used during the processing of the device repeatedly if necessary to assure programming function and performance.

### Two Transistor Cells

In order to provide an EPROM cell that is as fast as the fuse technology employed in bipolar processes, Cypress uses a two transistor EPROM cell. One transistor is optimized for reliable programming, and one transistor is optimized for high speed. The floating gates are connected such that charge injected on the floating gate of the programming transistor is conducted to the read transistor, biasing it off.

### Differential Memory Cells

In the 4K (CY7C225); 8K (CY7C235, CY7C281, CY7C282); and 16K (CY7C245, CY7C291, CY7C292) CMOS PROMs, Cypress employs a differential memory cell and sense amplifier technique. Higher density devices such as the 7C261, 7C263, 7C264 or 7C269 64K PROMs employ a single ended Cell and sense amplifier technique similar to the approach used in more conventional EPROMs.

In a conventional high density EPROM a single EPROM transistor is used to switch the input to one side of a differential sense amplifier. The other side of the sense amplifier is biased at an intermediate level with a dummy cell. An unprogrammed EPROM transistor will conduct and drive the sense amplifier to a logic "0". A programmed EPROM transistor will not conduct, and consequently drives the sense amplifier to a logic "1". A conventional EPROM cell therefore is delivered with a specific state "0" or "1" in it depending on the number of inversions after the sense amplifier and can always be programmed to the opposite state. Access time in this conventional approach is heavily dependent on the time the selected EPROM transistor takes to move the input of the sense amplifier from a quiescent condition to the threshold that the dummy cell is biasing the second input to the sense amplifier. This bias is several volts, and requires a significant delay before the sense amplifier begins to react.

Cypress PROMs employ a true differential cell approach, with EPROM cells attached to both inputs of the sense amplifier. As indicated above, the read transistor which is optimized for speed is actually the transistor attached to the sense amplifier. In the erased state, both EPROM transistors conduct when selected eccentrically biasing the input of the sense amplifier at the same level. If the inputs were at identical levels, the output of the sense amplifier would be in a metastable condition or, neither a "1" nor "0". In actual practice the natural bias and high gain of the sense amplifier combine to cause the output to favor one or the other stable conditions. The difference between the two conditions is however only a few millivolts and the memory cell should be considered to contain neither a "1" nor a "0". As a result of this design approach, the memory cell must be programmed to either a "1" or a "0" depending on the desired condition and the conventional BLANK



CHECK mechanism is invalid. The benefit of the approach however is that only a small differential signal from the cell begins the sense amplifier switching and the access time of the memory is extremely fast.

## Single Ended Memory Cells

Although a more conventional approach, single ended memory cells and sensing techniques offer a superior trade-off between die size and performance than the differential cell for devices of 64K densities and above. The Single ended technique employed by Cypress uses a dummy cell for the reference voltage thus providing a reference that tracks the programmed cell in process related parameters, power supply and temperature induced variations. The Memory cell used is a second generation two transistor cell derived from earlier work at the 16K density level. It has an optimized READ transistor that is matched to the sense amplifier, and a second transistor optimized for programming. The floating gates of the two transistors that make up a memory cell are connected electrically so that the charge programmed onto one device controls the threshold of the second transistor.

Unlike the differential memory approach, the erased single ended device contains all "0"s and on the the ones are programmed. Therefore a "1" on the data pins during programming causes a "1" to be programmed into the addressed location.

## Programming Algorithm

### Byte Addressing and Programming

All Cypress CMOS PROMs are addressed and programmed on a byte basis unlike the bipolar products that they replace. The address lines used to access the memory in a read mode are the same for programming, and the address map is identical. The information to be programmed into each byte is presented on the data out pins during the programming operation and the data is read from these same pins for verification that the byte has been programmed.

### Blank Check for Differential Cells

Since a differential cell contains neither a "1" nor a "0" before it is programmed, the conventional BLANK CHECK is not valid. For this reason, all Cypress CMOS PROMs contain a special BLANK CHECK mode of operation. Blank check is performed by separately examining the "0" and "1" sides of the differential memory cell to determine whether either side has been independently programmed. This is accomplished in two passes one comparing the "0" side of the differential cell against a reference voltage applied to the opposite side of the sense amplifier and then repeating this operation for the "1" side of the cell. The modes are called BLANK CHECK ONES, and BLANK CHECK ZEROS. These modes are entered by the application of a supervoltage to the device.

### Blank Check for Single Ended Cells

Single ended cells BLANK CHECK in a conventional manner. An erased device contains all "0"s and a programmed call will contain a "1". Cypress PROMs that use the single ended approach provide a specific mode to perform the BLANK CHECK which also provides the verify

function. This makes the need to switch high voltages unnecessary during the program verify operation. See specific data sheets for details.

## Programming the Data Array

Programming is accomplished by applying a supervoltage to one pin of the device causing it to enter the programming mode of operation. This also provides the programming voltage for the cells to be programmed. In this mode of operation, the address lines of the device are used to address each location to be programmed, and the data is presented on the pins normally used for reading the contents of the device. Each device has a READ and a WRITE pin in the programming mode. These are active low signals and cause the data on the output pins to be written into the addressed memory location in the case of the WRITE signal or read out of the device in the case of the READ signal. When both the READ and WRITE signals are high, the outputs are disabled and in a high impedance state. Programming therefore is accomplished by placing data on the output pins, and writing it into the addressed location with the WRITE signal. Verification of data is accomplished by reading the information on the output pins while the READ signal is active.

The timing for actual programming is supplied in the unique programming specification for each device.

## Special Features

Depending on the specific CMOS PROM in question, additional features that require programming may be available to the designer. Two of these features are a Programmable INITIAL BYTE and Programmable SYNCHRONOUS/ASYNCHRONOUS ENABLE available in some of the registered devices. Like programming the array, these features make use of EPROM cells and are programmed in a similar manner, using supervoltages. The specific timing and programming requirements are specified in the data sheet of the device employing the feature.

## Programming Support

Programming support for Cypress CMOS PROMs is available from a number of programmer manufacturers, some of which are listed below.

Data I/O Corporation  
 10525 Willows Rd. N.E.  
 P.O. Box 97046  
 Redmond, WA  
 98073-9746  
 (206) 881-6444

| Data I/O 29B Unipak II |                     |                        |    |          |
|------------------------|---------------------|------------------------|----|----------|
| Cypress Part Number    | Generic Part Number | Family Code and Pinout |    | Revision |
| CY7C225                | 27S25               | F0                     | B6 | V12      |
| CY7C235                | 27S35               | F0                     | B5 | V09      |
| CY7C245                | 27S45A              | F0                     | B0 | V09      |
| CY7C261/3/4            | 27S49               | EF                     | 31 | V11      |
| CY7C281/2              | 27S281/181          | EE                     | B4 | V09      |
| CY7C291/2              | 27S291/191          | EE                     | AF | V09      |



# PROM Programming Information (Continued)

Stag Microsystems  
 1600 Wyatt Dr.  
 Santa Clara, CA 95054  
 (408) 988-1118

Cypress Semiconductor, Inc.  
 3901 North First St.  
 San Jose, CA 95134  
 (408) 943-2600

| Stag PPZ Zm2000     |                     |                        |          |
|---------------------|---------------------|------------------------|----------|
| Cypress Part Number | Generic Part Number | Family Code and Pinout | Revision |
| CY7C225             | 27S25               | Menu Driven            | Rev 21   |
| CY7C235             | 27S35               |                        | Rev 21   |
| CY7C245             | 27S45A              |                        | Rev 24   |
| CY7C281/2           | 27S281/181          |                        | Rev 21   |
| CY7C291/2           | 27S291/191          |                        | Rev 21   |

| Cypress CY3000 QuickPro Rev. PROM 2.10 |                     |                        |
|--|---------------------|------------------------|
| Cypress Part Number                    | Generic Part Number | Family Code and Pinout |
| CY7C225                                | Menu Driven         | Menu Driven            |
| CY7C235                                |                     |                        |
| CY7C245                                |                     |                        |
| CY7C261/3/4                            |                     |                        |
| CY7C268                                |                     |                        |
| CY7C269                                |                     |                        |
| CY7C281/2                              |                     |                        |
| CY7C291/2                              |                     |                        |

3





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## EPLDs (Eraseable Programmable Logic Devices)

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## Cypress EPLD Family Features

Cypress Semiconductor's EPLD family offers the user the next generation in Erasable Programmable Logic Devices (EPLD) based on our high performance  $0.8\mu$  CMOS process. These devices offer the user the power saving of a CMOS-based process, with delay times equivalent to those previously found only in bipolar devices. No fuses are used in Cypress' EPLD family, rather all devices are based on an EPROM cell to facilitate programming. By using an EPROM cell instead of fuses, programming yields of 100% can be expected since all devices are functionally tested and erased prior to packaging. Therefore, no programming yield loss can be expected by the user.

The EPROM cell used by Cypress serves the same purpose as the fuse used in most bipolar PLD devices. Before programming, the AND gates or Product Terms are connected via the EPROM cells to both the true and complement inputs. When the EPROM cell is programmed, the inputs from a gate or Product Term are disconnected. Programming alters the transistor threshold of each cell so that no conduction can occur, which is equivalent to disconnecting the input from the gate or Product Terms. This is similar to "blowing" the fuses of a bipolar device which disconnects the input gate from the Product Term. Selective programming of each of these EPROM cells enables the specific logic function to be implemented by the user.

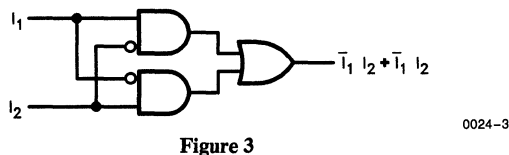
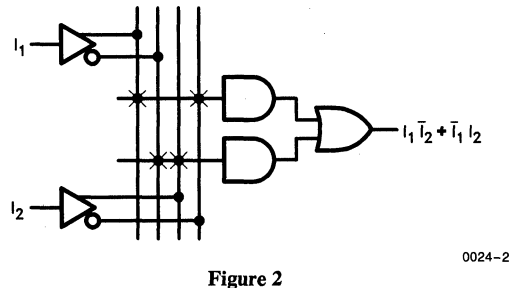
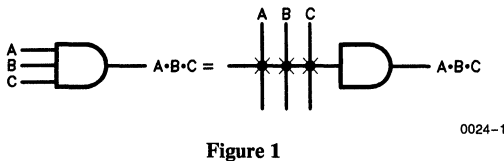
The programmability of Cypress' EPLDs allows the users to customize every device in a number of ways to implement their unique logic requirements. Using EPLDs in place of SSI or MSI components results in more effective utilization of boardspace, reduced cost and increased reli-

ability. The flexibility afforded by these EPLDs allows the designer to quickly and effectively implement a number of logic functions ranging from random logic gate replacement to complex combinatorial logic functions.

The EPLD family implements the familiar "sum of products" logic by using a programmable AND array whose output terms feed a fixed OR array. The sum of these can be expressed in a Boolean transfer function and is limited only by the number of product terms available in the AND-OR array. A variety of different sizes and architectures are available. This allows for more efficient logic optimization by matching input, output and product terms to the desired application.

## EPLD Notation

To reduce confusion and to have an orderly way of representing the complex logic networks, logic diagrams are provided for the various part types. In order to be useful, Cypress logic diagrams employ a common logic convention that is easy to use. *Figure 1* shows the adopted convention. In *Figure 1*, an "x" represents an unprogrammed EPROM cell that is used to perform the logical AND operation upon the input terms. The convention adopted does not imply that the input terms are connected on the common line that is indicated. A further extension of this convention is shown in *Figure 2* which shows the implementation of a simple transfer function. The normal logic representation of the transfer function logic convention is shown in *Figure 3*.





## PLD Circuit Configurations

Cypress EPLDs have several different output configurations that cover a wide spectrum of applications. The available output configurations offer the user the benefits of both lower package counts and reduced costs when used. This approach allows the designer to select a PLD that best fits the needs of his application. An example of some of the configurations that are available are listed below.

### Programmable I/O

Figure 4 illustrates the programmable I/O offered in the Cypress EPLD family which allows product terms to directly control the outputs of the device. One product term is used to directly control the three-state output buffer, which then gates the summation of the remaining terms to the output pin. The output of this summation can be fed back into the PLD as an input to the array. This programmable I/O feature allows the PLD to drive the output pin when the three-state output is enabled or, the I/O pin can be used as an input to the array when the three-state output is disabled.

### Registered Outputs with Feedback

Figure 5 illustrates the registered output offered on a number of the Cypress EPLDs which allow any of these circuits to function as a state sequencer. The summation of the product terms is stored in the D-type output flip-flop on the rising edge of the system clock. The Q output of the flip-flop can then be gated to the output pin by enabling the three-state output buffer. The output of the flip-flop can also be fed back into the array as an input term. The output feedback feature allows the PLD to remember and then alter its function based upon that state. This circuit can be used to execute such functions as counting, skip, shift and branch.

### Programmable Macro Cell

The Programmable Macro Cell, illustrated in Figure 10, provides the capability of defining the architecture of each output individually. Each of the potential outputs may be specified to be "REGISTERED" or "COMBINATORIAL". Polarity of each output may also be individually selected allowing complete flexibility of output configuration. Further configurability is provided through "ARRAY" configurable "OUTPUT ENABLE" for each potential output. This feature allows the outputs to be reconfigured as inputs on an individual basis or alternately used as a bidirectional I/O controlled by the programmable array.

### Buried Register Feedback

A number of Cypress EPLDs provide registers which may be "buried" or "hidden" to create registers for state machine implementation without sacrificing the use of the associated device pin. The device pin normally associated

with the register may still be used as a device input. The proprietary CY7C330 Reprogrammable Synchronous State Machine macrocell illustrates, in Figure 6, the use of buried registers with provision for saving the I/O pin for use as an input. If the feedback path is selected by the feedback multiplexer, the Q of the register is fed back to the array as an input. The I/O pin can still be routed to the array as an external input by use of a special multiplexer shown in Figure 7 provided for that purpose for each of the six macrocell pairs. A special configuration bit, C3, selects the input register output from one of the I/O pins of the pair of macrocell I/O pins which is to be fed to the array as an external input. By proper placement of buried register configured I/O macrocells adjacent to I/O macrocells used as normal registered outputs without feedback, maximum use of the buried macrocell I/O pins for inputs can be achieved. The CY7C330 also contains four dedicated buried or hidden registers with no external output, illustrated in Figure 8, which are used as additional state register resources for creation of high performance state machines.

### Asynchronous Register Control

Cypress also offers EPLDs which may be used in asynchronous systems in which register clock, set and reset are controlled by the outputs of the product term array. The clock signal is created by the processing of external inputs and/or internal feedback by the logic of the product term array which is then routed to the register clock. The register set and reset are similarly controlled by product term outputs and can be triggered at any time independent of the register clock in response to external and/or feedback inputs processed by the logic array. The proprietary CY7C331 Asynchronous Registered EPLD, for which the I/O macrocell is illustrated in Figure 9, is an example of such a device. The register clock, set and reset functions of the CY7C331 are all controlled by product terms and enable their respective functions dependent only on input signal timing and combinatorial delay through the device logic array.

### Input Register Cell

Other Cypress EPLDs provide input register cells which allow capture for processing of short duration inputs which would not otherwise be present at the inputs for sufficient time to allow the device to respond. Both the proprietary CY7C330 Reprogrammable Synchronous State Machine and the proprietary CY7C332 Combinatorial EPLD provide these input register cells which are shown in Figure 11. The clock for the input register may be provided from one of two external clock input pins selectable by a configuration bit, C4, dedicated for this purpose for each input register. This choice of input register clock allows signals to be captured and processed from two independent system sources each controlled by its own independent clock. These input register cells are provided within I/O macrocells, as well as, for dedicated input pins.

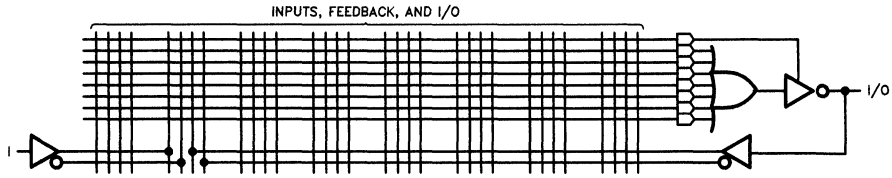


Figure 4. Programmable I/O

0024-4

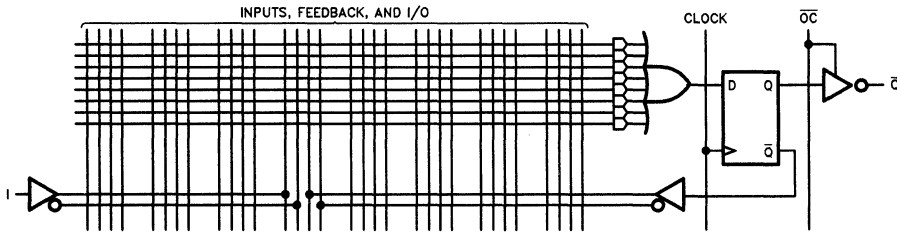


Figure 5. Registered Outputs with Feedback

0024-5

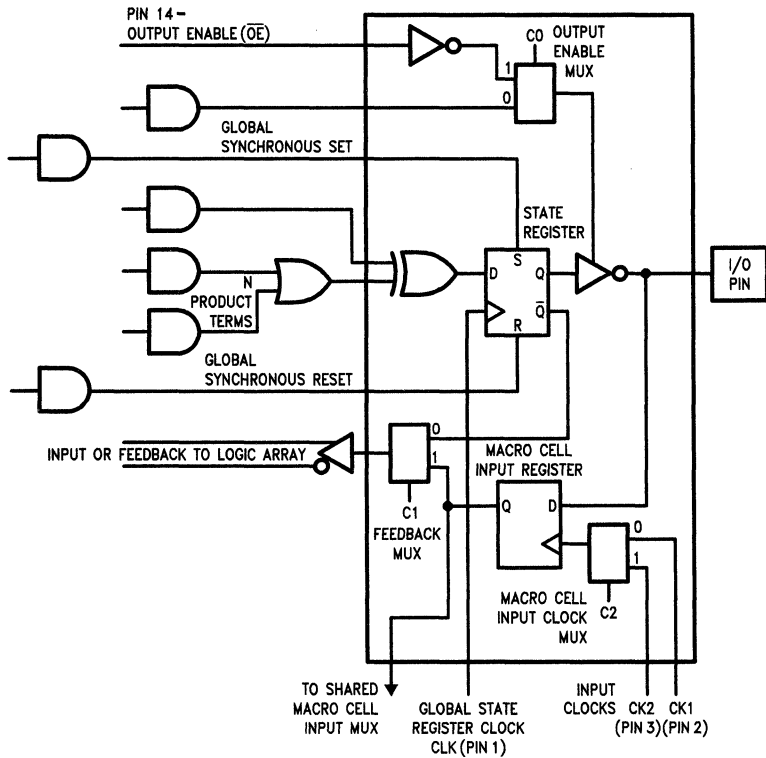
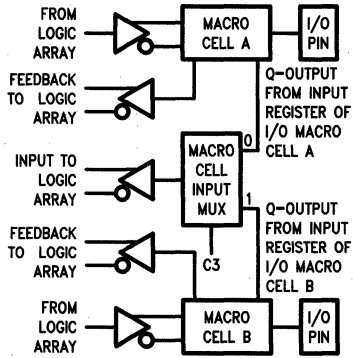


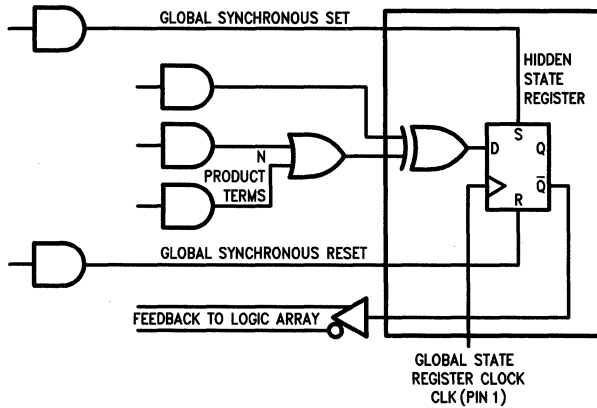
Figure 6. CY7C330 I/O Macro Cell

0024-7



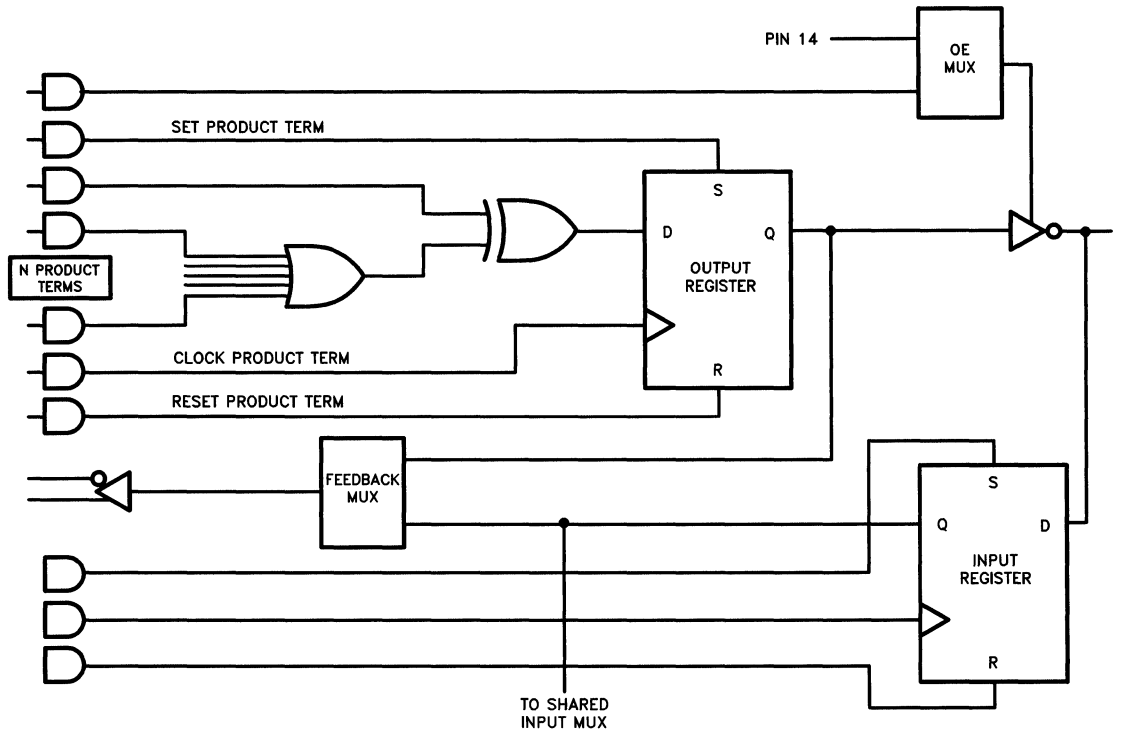
0024-8

**Figure 7. CY7C330 I/O Macro Cell Pair Shared Input MUX**



0024-9

**Figure 8. CY7C330 Hidden State Register Macro Cell**



4

Figure 9. CY7C331 Registered Asynchronous Macrocell

0024-10

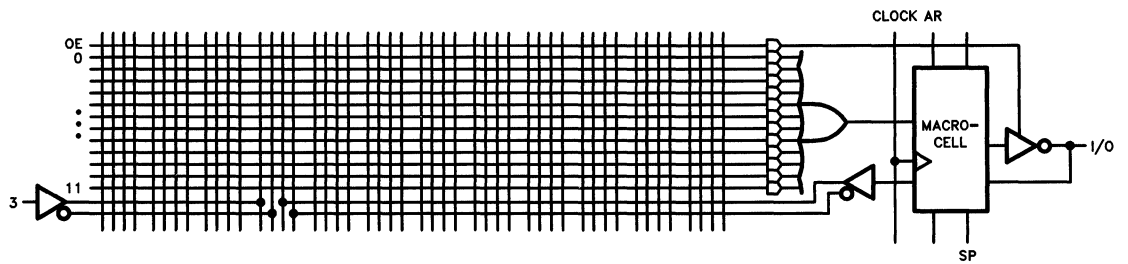
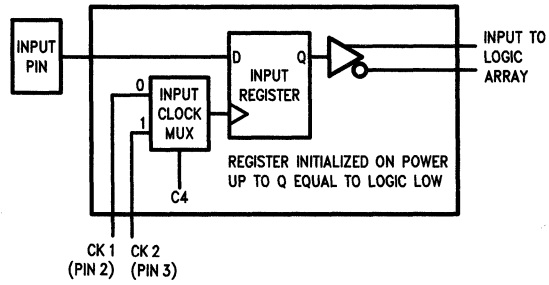


Figure 10. Programmable Macro Cell

0024-6



0024-11

**Figure 11. CY7C330 Dedicated Input Cell**



CYPRESS  
SEMICONDUCTOR

PAL® C 20 Series

# Reprogrammable CMOS PAL® C 16L8, 16R8, 16R6, 16R4

## Features

- CMOS EPROM technology for reprogrammability
- High performance at quarter power
  - $t_{PD} = 25$  ns
  - $t_S = 20$  ns
  - $t_{CO} = 15$  ns
  - $I_{CC} = 45$  mA
- High performance at military temperature
  - $t_{PD} = 20$  ns
  - $t_S = 20$  ns
  - $t_{CO} = 15$  ns
  - $I_{CC} = 70$  mA
- Commercial and military temperature range
- High reliability
  - Proven EPROM technology
  - > 1500V input protection from electrostatic discharge
  - 100% AC/DC tested
  - 10% power supply tolerances
  - High noise immunity
  - Security feature prevents pattern duplication
  - 100% programming and functional testing

gram custom logic functions serving unique requirements.

PALs are offered in 20-pin plastic and ceramic DIP, Plastic SOJ, and ceramic LCC packages. The ceramic package can be equipped with an erasure window; when exposed to UV light, the PAL is erased and can then be reprogrammed.

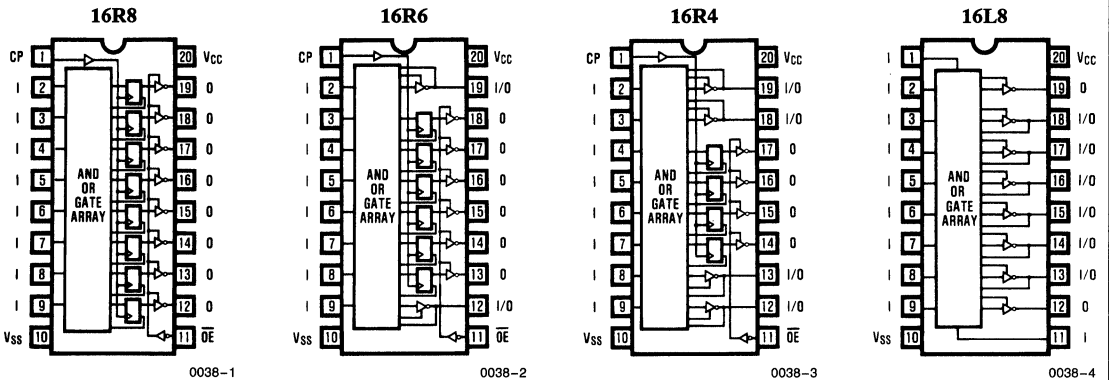
Before programming, AND gates or PRODUCT TERMS are connected via EPROM cells to both TRUE and COMPLEMENT inputs. Programming an EPROM cell disconnects an INPUT TERM from a PRODUCT TERM. Selective programming of these cells allows a specific logic function to be implemented in a PAL C device. PAL C devices are supplied in four functional configurations, design-

## Functional Description

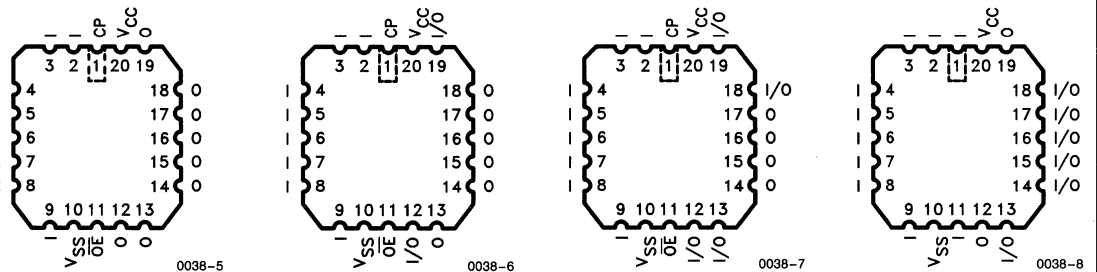
Cypress PAL C Series 20 devices are high speed electrically programmable and UV erasable logic devices produced in a proprietary "N" well CMOS EPROM process. These devices utilize the sum of products (AND-OR) structure providing users the ability to pro-

4

## Logic Symbols and DIP and SOJ Pinouts



## LCC Pinouts



PAL® is a registered trademark of Monolithic Memories Inc.  
CYPRESS SEMICONDUCTOR is a trademark of Cypress Semiconductor Corporation.

## Functional Description (Continued)

nated 16R8, 16R6, 16R4 and 16L8. These eight devices have potentially 16 inputs and 8 outputs configurable by the user. Output configurations of 8 registers, 8 combinatorial, 6 registers and 2 combinatorial as well as 4 registers and 4 combinatorial are provided by the four functional variations of the product family. All combinatorial outputs on the 16R6 and 16R4 as well as 6 of the combinatorial outputs on the 16L8 may be used as optional inputs. All registered outputs have the Q bar side of the register fed back into the main array. The registers are automatically initialized on power up to Q output LOW and Q output HIGH. All unused inputs should be tied to ground.

All PAL C devices feature a SECURITY function which provides the user protection for the implementation of proprietary logic. When invoked, the contents of the normal array may no longer be accessed in the verify mode. Because EPROM technology is used as a storage mechanism, the content of the array is not visible under a microscope. The PAL C device also contains a PHANTOM ARRAY used for functional and performance testing. The content of this array is always accessible, even when security is invoked.

Cypress PAL C products are produced in an advanced 1.2 micron "N" well CMOS EPROM technology. The use of this proven EPROM technology is the basis for a superior product with inherent advantages in reliability, testability, programming and functional yield. EPROM technology has the inherent advantage that all programmable elements may be programmed, tested and erased during the manufacturing process. This also allows the device to be 100%

functionally tested during manufacturing. An ability to preload the registers of registered devices during the testing operation makes the testing easier and more efficient. The PHANTOM ARRAY and PHANTOM operating mode allow the device to be tested for functionality and performance after it has been packaged. Combining these inherent and designed-in features, an extremely high degree of functionality, programmability and assured AC performance are provided and testing becomes an easy task.

The REGISTER PRELOAD allows the user to initialize the registered devices to a known state prior to testing the device, significantly simplifying and shortening the testing procedure.

The PHANTOM MODE of operation provides a completely separate operating mode where the functionality of the device along with its AC performance may be ascertained. The user need not be encumbered by programmed cells in the normal operating mode. This PHANTOM MODE of operation allows additional input lines to be programmed to operate the PAL C device, exercising the device functionally and allowing AC performance measurements to be made. The PHANTOM MODE of operation acknowledges only the INPUT TERMS shown shaded in the functional block diagrams. Likewise, the normal PHANTOM INPUT TERMS do not exist in the normal mode of operation. During the final stages of manufacturing, some cells in the PHANTOM ARRAY are programmed for final AC and functional testing. These cells remain programmed, and may be used at incoming inspection to verify both functional and AC performance.

## Commercial and Industrial Selection Guide

| Generic Part Number | Logic                    | Output Enable | Outputs                            | I <sub>CC</sub> (mA) |           | t <sub>PD</sub> (ns) |     | t <sub>S</sub> (ns) |     | t <sub>CO</sub> (ns) |     |
|---------------------|--------------------------|---------------|------------------------------------|----------------------|-----------|----------------------|-----|---------------------|-----|----------------------|-----|
|                     |                          |               |                                    | L                    | COMPL/IND | -25                  | -35 | -25                 | -35 | -25                  | -35 |
| 16L8                | (8) 7-wide AND-OR-Invert | Programmable  | (6) Bidirectional<br>(2) Dedicated | 45                   | 70        | 25                   | 35  | —                   | —   | —                    | —   |
| 16R8                | (8) 8-wide AND-OR        | Dedicated     | Registered Inverting               | 45                   | 70        | —                    | —   | 20                  | 30  | 15                   | 25  |
| 16R6                | (6) 8-wide AND-OR        | Dedicated     | Registered Inverting               | 45                   | 70        | 25                   | 35  | 20                  | 30  | 15                   | 25  |
|                     | (2) 7-wide AND-OR-Invert | Programmable  | Bidirectional                      |                      |           |                      |     |                     |     |                      |     |
| 16R4                | (4) 8-wide AND-OR        | Dedicated     | Registered Inverting               | 45                   | 70        | 25                   | 35  | 20                  | 30  | 15                   | 25  |
|                     | (4) 7-wide AND-OR-Invert | Programmable  | Bidirectional                      |                      |           |                      |     |                     |     |                      |     |

## Military Selection Guide

| Generic Part Number | Logic                    | Output Enable | Outputs                            | I <sub>CC</sub> (mA) | t <sub>PD</sub> (ns) |     |     | t <sub>S</sub> (ns) |     |     | t <sub>CO</sub> (ns) |     |     |
|---------------------|--------------------------|---------------|------------------------------------|----------------------|----------------------|-----|-----|---------------------|-----|-----|----------------------|-----|-----|
|                     |                          |               |                                    |                      | -20                  | -30 | -40 | -20                 | -30 | -40 | -20                  | -30 | -40 |
| 16L8                | (8) 7-wide AND-OR-Invert | Programmable  | (6) Bidirectional<br>(2) Dedicated | 70                   | 20                   | 30  | 40  | —                   | —   | —   | —                    | —   | —   |
| 16R8                | (8) 8-wide AND-OR        | Dedicated     | Registered Inverting               | 70                   | —                    | —   | —   | 20                  | 25  | 35  | 15                   | 20  | 25  |
| 16R6                | (6) 8-wide AND-OR        | Dedicated     | Registered Inverting               | 70                   | 20                   | 30  | 40  | 20                  | 25  | 35  | 15                   | 20  | 25  |
|                     | (2) 7-wide AND-OR-Invert | Programmable  | Bidirectional                      |                      |                      |     |     |                     |     |     |                      |     |     |
| 16R4                | (4) 8-wide AND-OR        | Dedicated     | Registered Inverting               | 70                   | 20                   | 30  | 40  | 20                  | 25  | 35  | 15                   | 20  | 25  |
|                     | (4) 7-wide AND-OR-Invert | Programmable  | Bidirectional                      |                      |                      |     |     |                     |     |     |                      |     |     |

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature .....                                   | -65°C to +150°C |
| Ambient Temperature with Power Applied .....                | -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 20 to Pin 10) ..... | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State .....         | -0.5V to +7.0V  |
| DC Input Voltage .....                                      | -3.0V to +7.0V  |
| Output Current into Outputs (Low) .....                     | 24 mA           |
| DC Programming Voltage .....                                | 14.0V           |

|                                |                                       |
|--------------------------------|---------------------------------------|
| UV Exposure .....              | 7258 Wsec/cm <sup>2</sup>             |
| Static Discharge Voltage ..... | > 1500V (per MIL-STD-883 Method 3015) |
| Latchup Current .....          | > 200 mA                              |

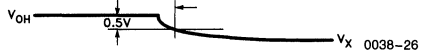
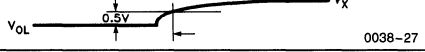

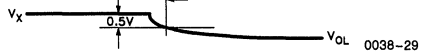
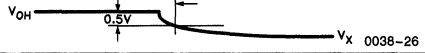
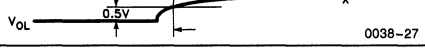

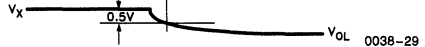
**Operating Range**

| Range       | Ambient Temperature | V <sub>CC</sub> |
|-------------|---------------------|-----------------|
| Commercial  | 0°C to +75°C        | 5V ± 10%        |
| Military[7] | -55°C to +125°C     | 5V ± 10%        |
| Industrial  | -40°C to +85°C      | 5V ± 10%        |

**4**
**Electrical Characteristics Over Operating Range (Unless Otherwise Noted)[6]**

| Parameters      | Description                  | Test Conditions  |   | Min. | Max. | Units |
|-----------------|------------------------------|--|---|------|------|-------|
|                 |                              | V <sub>CC</sub> = Min.<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>         | I <sub>OH</sub> = -3.2 mA<br>Commercial/Industrial<br>I <sub>OH</sub> = -2 mA<br>Military |      |      |       |
| V <sub>OH</sub> | Output HIGH Voltage          |  |   | 2.4  |      | V     |
| V <sub>OL</sub> | Output LOW Voltage           | V <sub>CC</sub> = Min.<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>         | I <sub>OL</sub> = 24 mA<br>Commercial/Industrial<br>I <sub>OL</sub> = 12 mA<br>Military   |      | 0.4  | V     |
| V <sub>IH</sub> | Input HIGH Level             | Guaranteed Input Logic HIGH <sup>[1]</sup> Voltage for all Inputs                      |   | 2.0  |      | V     |
| V <sub>IL</sub> | Input LOW Level              | Guaranteed Input Logical LOW <sup>[1]</sup> Voltage for all Inputs                     |   |      | 0.8  | V     |
| I <sub>IX</sub> | Input Leakage Current        | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                                    |   | -10  | 10   | μA    |
| V <sub>PP</sub> | Programming Voltage          | I <sub>PP</sub> = 50 mA Max.   |   | 13.0 | 14.0 | V     |
| I <sub>SC</sub> | Output Short Circuit Current | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V <sup>[2]</sup>                         |   |      | -300 | mA    |
| I <sub>CC</sub> | Power Supply Current         | All Inputs = GND,<br>V <sub>CC</sub> = Max.,<br>I <sub>OUT</sub> = 0 mA <sup>[5]</sup> | "L"   |      | 45   | mA    |
|                 |                              |  | COM'L/IND   |      | 70   | mA    |
|                 |                              |  | MIL   |      | 70   | mA    |
| I <sub>OZ</sub> | Output Leakage Current       | V <sub>CC</sub> = Max., V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>           |   | -100 | 100  | μA    |

**Table 1**

| Parameter            | V <sub>X</sub>   | Output Waveform—Measurement Level  |
|----------------------|------------------|--|
| t <sub>PXZ</sub> (-) | 1.5V             |  |
| t <sub>PXZ</sub> (+) | 2.6V             |  |
| t <sub>PZX</sub> (+) | V <sub>thc</sub> |  |
| t <sub>PZX</sub> (-) | V <sub>thc</sub> |  |
| t <sub>ER</sub> (-)  | 1.5V             |  |
| t <sub>ER</sub> (+)  | 2.6V             |  |
| t <sub>EA</sub> (+)  | V <sub>thc</sub> |  |
| t <sub>EA</sub> (-)  | V <sub>thc</sub> |  |



**Capacitance<sup>[3]</sup>**

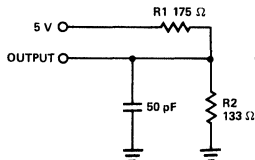
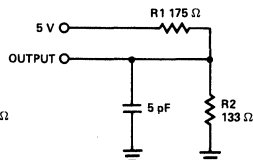
| Parameters       | Description        | Test Conditions                             | Max. | Units |
|------------------|--------------------|---|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz            | 7    | pF    |
| C <sub>OUT</sub> | Output Capacitance | V <sub>IN</sub> = 0, V <sub>CC</sub> = 5.0V | 7    |       |

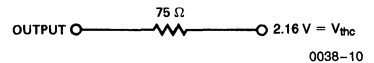
**Switching Characteristics PAL C 20 Series Over Operating Range<sup>[4, 6, 8]</sup>**

| Parameters       | Description   | Commercial/Industrial |      |      |      | Military |      |      |      |      | Units |      |
|------------------|---|-----------------------|------|------|------|----------|------|------|------|------|-------|------|
|                  |   | -25                   |      | -35  |      | -20      |      | -30  |      | -40  |       |      |
|                  |   | Min.                  | Max. | Min. | Max. | Min.     | Max. | Min. | Max. | Min. |       | Max. |
| t <sub>PD</sub>  | Input or Feedback to Non-Registered Output 16L8, 16R6, 16R4 |                       | 25   |      | 35   |          | 20   |      | 30   |      | 40    | ns   |
| t <sub>EA</sub>  | Input to Output Enable 16L8, 16R6, 16R4                     |                       | 25   |      | 35   |          | 20   |      | 30   |      | 40    | ns   |
| t <sub>ER</sub>  | Input to Output Disable 16L8, 16R6, 16R4                    |                       | 25   |      | 35   |          | 20   |      | 30   |      | 40    | ns   |
| t <sub>PZX</sub> | Pin 11 to Output Enable 16R8, 16R6, 16R4                    |                       | 20   |      | 25   |          | 20   |      | 25   |      | 25    | ns   |
| t <sub>PXZ</sub> | Pin 11 to Output Disable 16R8, 16R6, 16R4                   |                       | 20   |      | 25   |          | 20   |      | 25   |      | 25    | ns   |
| t <sub>CO</sub>  | Clock to Output 16R8, 16R6, 16R4                            |                       | 15   |      | 25   |          | 15   |      | 20   |      | 25    | ns   |
| t <sub>S</sub>   | Input or Feedback Setup Time 16R8, 16R6, 16R4               | 20                    |      | 30   |      | 20       |      | 25   |      | 35   |       | ns   |
| t <sub>H</sub>   | Hold Time 16R8, 16R6, 16R4                                  | 0                     |      | 0    |      | 0        |      | 0    |      | 0    |       | ns   |
| t <sub>p</sub>   | Clock Period  | 35                    |      | 55   |      | 35       |      | 45   |      | 60   |       | ns   |
| t <sub>w</sub>   | Clock Width   | 15                    |      | 20   |      | 12       |      | 20   |      | 25   |       | ns   |
| f <sub>MAX</sub> | Maximum Frequency   |                       | 28.5 |      | 18   |          | 28.5 |      | 22   |      | 16.5  | MHz  |

**Notes:**

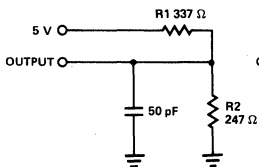
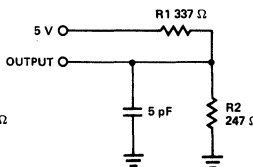
- These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V<sub>OUT</sub> = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.
- Figure 1a test load used for all parameters except t<sub>EA</sub>, t<sub>ER</sub>, t<sub>PZX</sub> and t<sub>PXZ</sub>. Figure 1b test load used for t<sub>EA</sub>, t<sub>ER</sub>, t<sub>PZX</sub> and t<sub>PXZ</sub>.
- I<sub>CC(AC)</sub> = (0.6 mA/MHz) × (Operating Frequency in MHz) + I<sub>CC(DC)</sub>. I<sub>CC(DC)</sub> is measured with an unprogrammed device.
- See the last page of this specification for Group A subgroup testing information.
- T<sub>A</sub> is the "instant on" case temperature.
- The parameters t<sub>ER</sub> and t<sub>PXZ</sub> are measured as the delay from the input disable logic threshold transition to V<sub>OH</sub> - 0.5V for an enabled HIGH output or V<sub>OL</sub> + 0.5V for an enabled LOW output. Please see Table 1 for waveforms and measurement reference levels.

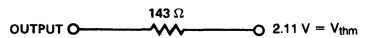
**AC Test Loads and Waveforms**

**Figure 1a. Commercial**

**Figure 1b. Commercial**

 Equivalent to:  
**THÉVENIN EQUIVALENT COMMERCIAL**


0038-11

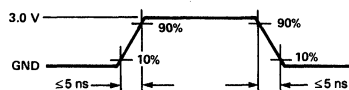
0038-10


**Figure 1c. Military**

**Figure 1d. Military**

 Equivalent to:  
**THÉVENIN EQUIVALENT MILITARY**


0038-9

0038-12


**Figure 2**

0038-13

## Switching Waveforms

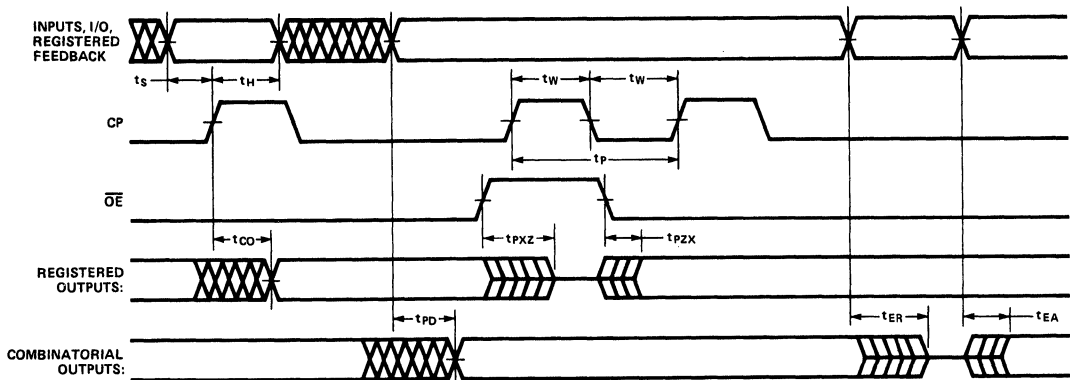


Figure 3

0038-14

## Erasure Characteristics

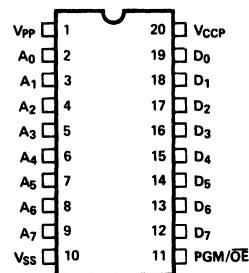
Wavelengths of light less than 4000 Angstroms begin to erase the PAL C device. For this reason, an opaque label should be placed over the window if the device is exposed to sunlight or fluorescent lighting for extended periods of time. In addition, high ambient light levels can create hole-electron pairs which may cause “blank” check failures or “verify errors” when programming “windowed” parts. This phenomenon can be avoided by use of an opaque label over the window during programming in high ambient light environments.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity x exposure time) of 25 Wsec/cm<sup>2</sup>. For an ultraviolet lamp with a 12 mW/cm<sup>2</sup> power rating, the exposure would be approximately 35 minutes. The PAL C device needs to be placed within 1 inch of the lamp during erasure. Permanent damage may result if the device is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm<sup>2</sup> is the recommended maximum dosage.

## Programming

PAL C devices are programmed a BYTE at a time using a voltage to transfer electrons to a floating gate. The array programmed is addressed as memory of 256 bytes, using address Tables 5 and 6. These addresses are supplied to the device over Pins 2 through 9. The data to be programmed is supplied on data inputs D0 through D7 (Pins 19 through

12 inclusive). In the unprogrammed state, all inputs are connected to product terms. A “1” on a data line causes a cell to be programmed, disconnecting an INPUT TERM from a PRODUCT TERM. During verify, an unprogrammed cell causes a “1” to appear on the output, while a programmed cell will appear as a “0”. Table 4 describes the operating modes of the device and the programming waveforms are described in Figures 6 through 9. The actual sequence required to program a cell is described in Figure 5 and applies for programming either standard or phantom portions of the array. The security bit should be programmed using a single 10 ms pulse, and verified per Figure 9.



0038-15

Figure 4. Programming Pin Configuration

## DC Programming Parameters Ambient Temperature = 25°C

Table 2

| Parameter        | Description                       | Min. | Max. | Units | Notes |
|------------------|-----------------------------------|------|------|-------|-------|
| V <sub>PP</sub>  | Programming Voltage               | 13.0 | 14.0 | V     |       |
| V <sub>CCP</sub> | Supply Voltage During Programming | 4.75 | 5.25 | V     |       |
| V <sub>IHP</sub> | Programming Input High Voltage    | 3.0  |      | V     |       |
| V <sub>ILP</sub> | Programming Input Low Voltage     |      | 0.4  | V     |       |
| V <sub>OH</sub>  | Output High Voltage               | 2.4  |      | V     | 1     |
| V <sub>OL</sub>  | Output Low Voltage                |      | 0.4  | V     | 1     |
| I <sub>PP</sub>  | Programming Supply Current        |      | 50   | mA    |       |

**AC Programming Parameters** Ambient Temperature = 25°C

**Table 3**

| Parameter                       | Description                        | Min. | Max.   | Units | Notes |
|---------------------------------|------------------------------------|------|--------|-------|-------|
| t <sub>pp</sub>                 | Programming Pulse Width            | 100  | 10,000 | μs    | 2     |
| t <sub>s</sub>                  | Setup Time                         | 1.0  |        | μs    |       |
| t <sub>H</sub>                  | Hold Time                          | 1.0  |        | μs    |       |
| t <sub>r</sub> , t <sub>f</sub> | V <sub>pp</sub> Rise and Fall Time | 1.0  |        | μs    | 2     |
| t <sub>VD</sub>                 | Delay to Verify                    | 1.0  |        | μs    |       |
| t <sub>VP</sub>                 | Verify Pulse Width                 | 2.0  |        | μs    |       |
| t <sub>DV</sub>                 | Verify to Data Valid               | 20.0 |        | μs    |       |
| t <sub>DZ</sub>                 | Verify to High Z                   |      | 1.0    | μs    |       |

**Table 4**

| Pin Name                   | V <sub>PP</sub> | PGM/OE           | A1              | A2              | A3              | A4              | A5              | D7–D0               | Notes    |
|----------------------------|-----------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|---------------------|----------|
| Pin Number                 | (1)             | (11)             | (3)             | (4)             | (5)             | (6)             | (7)             | (12–19)             |          |
| <b>Operating Modes</b>     |                 |                  |                 |                 |                 |                 |                 |                     |          |
| PAL                        | X               | X                | X               | X               | X               | X               | X               | Programmed Function | 3, 4     |
| Program PAL                | V <sub>PP</sub> | V <sub>PP</sub>  | X               | X               | X               | X               | X               | Data In             | 3, 5     |
| Program Inhibit            | V <sub>PP</sub> | V <sub>IHP</sub> | X               | X               | X               | X               | X               | High Z              | 3, 5     |
| Program Verify/Blank Check | V <sub>PP</sub> | V <sub>ILP</sub> | X               | X               | X               | X               | X               | Data Out            | 3, 5, 11 |
| Phantom PAL                | X               | X                | X               | X               | X               | V <sub>PP</sub> | X               | Programmed Function | 3, 6     |
| Program Phantom PAL        | V <sub>PP</sub> | V <sub>PP</sub>  | X               | X               | X               | X               | V <sub>PP</sub> | Data In             | 3, 7     |
| Phantom Program Inhibit    | V <sub>PP</sub> | V <sub>IHP</sub> | X               | X               | X               | X               | V <sub>PP</sub> | High Z              | 3, 7     |
| Phantom Program Verify     | V <sub>PP</sub> | V <sub>ILP</sub> | X               | X               | X               | X               | V <sub>PP</sub> | Data Out            | 3, 7     |
| Program Security Bit       | V <sub>PP</sub> | V <sub>PP</sub>  | V <sub>PP</sub> | X               | X               | X               | X               | High Z              | 3, 8     |
| Verify Security Bit        | X               | X                | Note 9          | V <sub>PP</sub> | X               | X               | X               | High Z              | 3        |
| Register Preload           | X               | X                | X               | X               | V <sub>PP</sub> | X               | X               | Data In             | 3, 10    |

**Notes:**

1. During verify operation
2. Measured at 10% and 90% points
3. V<sub>SS</sub> < X < V<sub>CCP</sub>
4. All "X" inputs operational per normal PAL function.
5. Address inputs occupy Pins 2 thru 9 inclusive, for both programming and verification see programming address Tables 5 and 6.
6. All "X" inputs operational per normal PAL function except that they operate on the function that occupies the phantom array.
7. Address inputs occupy Pins 2 thru 9 inclusive, for both programming and verification see programming address Tables 5 and 6. Pin 7

8. is used to select the phantom mode of operation and must be taken to V<sub>pp</sub> before selecting phantom program operation with V<sub>pp</sub> on Pin 1.
8. See Figure 8 for security programming sequence.
9. The state of Pin 3 indicates if the security function has been invoked or not. If Pin 3 = V<sub>OL</sub> security is in effect, if Pin 3 = V<sub>OH</sub>, the data is unsecured and may be directly accessed.
10. For testing purposes, the output latch on the 16R8, 16R6 and 16R4 may be preloaded with data from the appropriate associated output line.
11. It is necessary to toggle Pin 11 (OE) HIGH during all address transitions while in the Program Verify or Blank Check mode.

The programmable array is addressed as a basic 256 by 8 memory structure with a duplication of the phantom array located at the same addresses as columns 0, 1, 2 and 3. The ability to address the phantom array as differentiated from the first 4 columns of the normal array is accomplished by taking Pin 7 to V<sub>pp</sub> and entering the phantom mode of operation as shown in Tables 4 and 6. In either case, phantom or normal, product terms are addressed in groups of 8 per Table 5. Notice that this is accomplished by modulo 8

selecting every eighth product term starting with 0, 8, 16, 24, 32, 40, 48 and 56 corresponding to PROGRAMMED DATA INPUT on D0 through D7 respectively and incrementing each product term by one until all 64 PRODUCT TERMS are addressed. Each of the INPUT TERMS is addressed 8 times corresponding to the 8 groups of individual product terms addressed before being incremented.

**Table 5**

| Product Term Addresses |      |      |             |    |    |    |    |    |    |    |
|------------------------|------|------|-------------|----|----|----|----|----|----|----|
| Binary Addresses       |      |      | Line Number |    |    |    |    |    |    |    |
| Pin Numbers            |      |      |             |    |    |    |    |    |    |    |
| (4)                    | (3)  | (2)  |             |    |    |    |    |    |    |    |
| VILP                   | VILP | VILP | 0           | 8  | 16 | 24 | 32 | 40 | 48 | 56 |
| VILP                   | VILP | VIHP | 1           | 9  | 17 | 25 | 33 | 41 | 49 | 57 |
| VILP                   | VIHP | VILP | 2           | 10 | 18 | 26 | 34 | 42 | 50 | 58 |
| VILP                   | VIHP | VIHP | 3           | 11 | 19 | 27 | 35 | 43 | 51 | 59 |
| VIHP                   | VILP | VILP | 4           | 12 | 20 | 28 | 36 | 44 | 52 | 60 |
| VIHP                   | VILP | VIHP | 5           | 13 | 21 | 29 | 37 | 45 | 53 | 61 |
| VIHP                   | VIHP | VILP | 6           | 14 | 22 | 30 | 38 | 46 | 54 | 62 |
| VIHP                   | VIHP | VIHP | 7           | 15 | 23 | 31 | 39 | 47 | 55 | 63 |
|                        |      |      | D0          | D1 | D2 | D3 | D4 | D5 | D6 | D7 |
| Programmed Data Input  |      |      |             |    |    |    |    |    |    |    |

**Table 6**

| Input Term Addresses |                  |      |      |      |      |
|----------------------|------------------|------|------|------|------|
| Input Term Numbers   | Binary Addresses |      |      |      |      |
|                      | Pin Numbers      |      |      |      |      |
|                      | (9)              | (8)  | (7)  | (6)  | (5)  |
| 0                    | VILP             | VILP | VILP | VILP | VILP |
| 1                    | VILP             | VILP | VILP | VILP | VIHP |
| 2                    | VILP             | VILP | VILP | VIHP | VILP |
| 3                    | VILP             | VILP | VILP | VIHP | VIHP |
| 4                    | VILP             | VILP | VIHP | VILP | VILP |
| 5                    | VILP             | VILP | VIHP | VILP | VIHP |
| 6                    | VILP             | VILP | VIHP | VIHP | VILP |
| 7                    | VILP             | VILP | VIHP | VIHP | VIHP |
| 8                    | VILP             | VIHP | VILP | VILP | VILP |
| 9                    | VILP             | VIHP | VILP | VILP | VIHP |
| 10                   | VILP             | VIHP | VILP | VIHP | VILP |
| 11                   | VILP             | VIHP | VILP | VIHP | VIHP |
| 12                   | VILP             | VIHP | VIHP | VILP | VILP |
| 13                   | VILP             | VIHP | VIHP | VILP | VIHP |
| 14                   | VILP             | VIHP | VIHP | VIHP | VILP |
| 15                   | VILP             | VIHP | VIHP | VIHP | VIHP |
| 16                   | VIHP             | VILP | VILP | VILP | VILP |
| 17                   | VIHP             | VILP | VILP | VILP | VIHP |

| Input Term Addresses |                  |      |      |      |      |
|----------------------|------------------|------|------|------|------|
| Input Term Numbers   | Binary Addresses |      |      |      |      |
|                      | Pin Numbers      |      |      |      |      |
|                      | (9)              | (8)  | (7)  | (6)  | (5)  |
| 18                   | VIHP             | VILP | VILP | VIHP | VILP |
| 19                   | VIHP             | VILP | VILP | VIHP | VIHP |
| 20                   | VIHP             | VILP | VIHP | VILP | VILP |
| 21                   | VIHP             | VILP | VIHP | VILP | VIHP |
| 22                   | VIHP             | VILP | VIHP | VIHP | VILP |
| 23                   | VIHP             | VILP | VIHP | VIHP | VIHP |
| 24                   | VIHP             | VIHP | VILP | VILP | VILP |
| 25                   | VIHP             | VIHP | VILP | VILP | VIHP |
| 26                   | VIHP             | VIHP | VILP | VIHP | VILP |
| 27                   | VIHP             | VIHP | VILP | VIHP | VIHP |
| 28                   | VIHP             | VIHP | VIHP | VILP | VILP |
| 29                   | VIHP             | VIHP | VIHP | VILP | VIHP |
| 30                   | VIHP             | VIHP | VIHP | VIHP | VILP |
| 31                   | VIHP             | VIHP | VIHP | VIHP | VIHP |
| P0                   | VILP             | VILP | VPP  | X    | X    |
| P1                   | VILP             | VIHP | VPP  | X    | X    |
| P2                   | VIHP             | VILP | VPP  | X    | X    |
| P3                   | VIHP             | VIHP | VPP  | X    | X    |

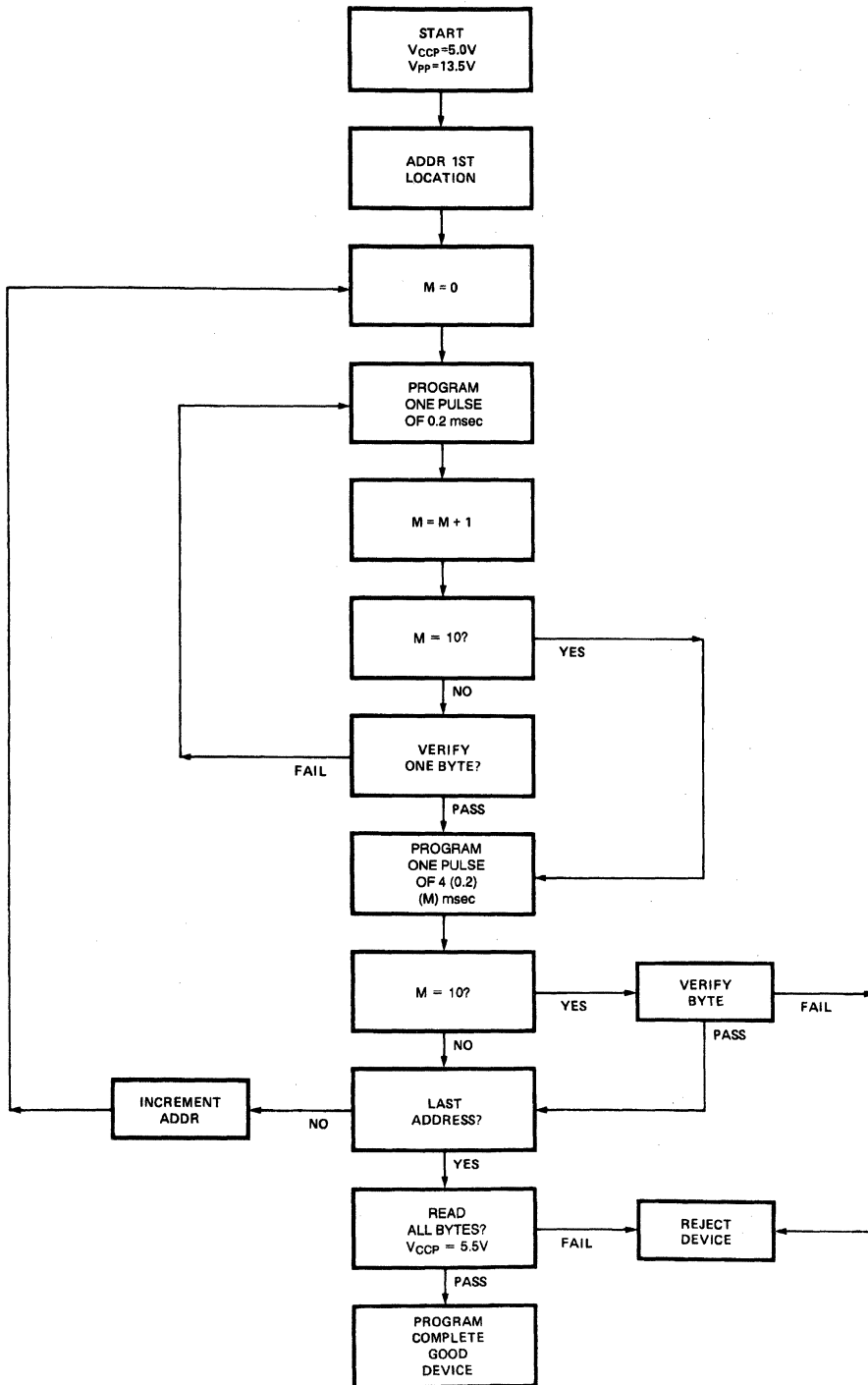


Figure 5. Programming Flowchart

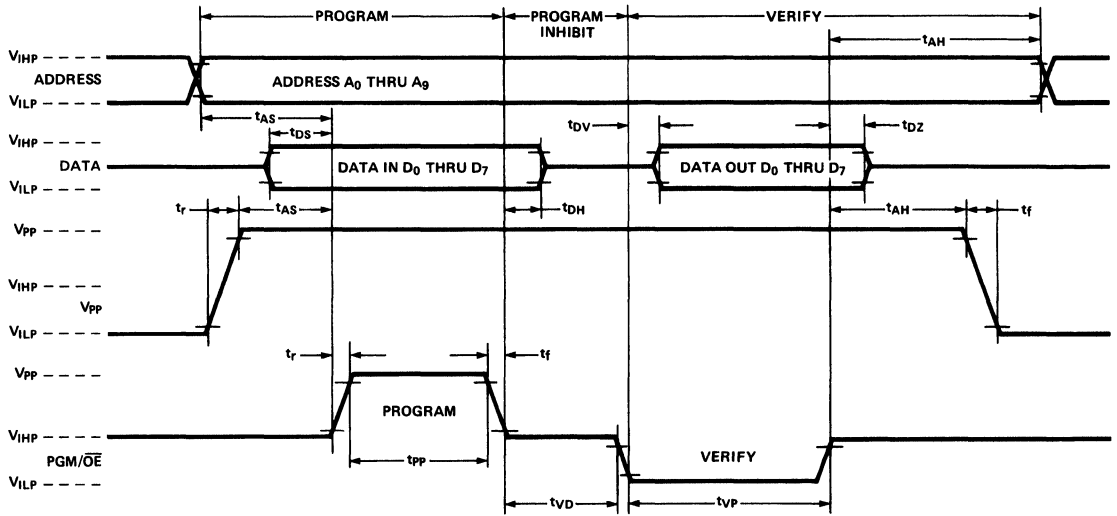


Figure 6. Programming Waveforms Normal Array

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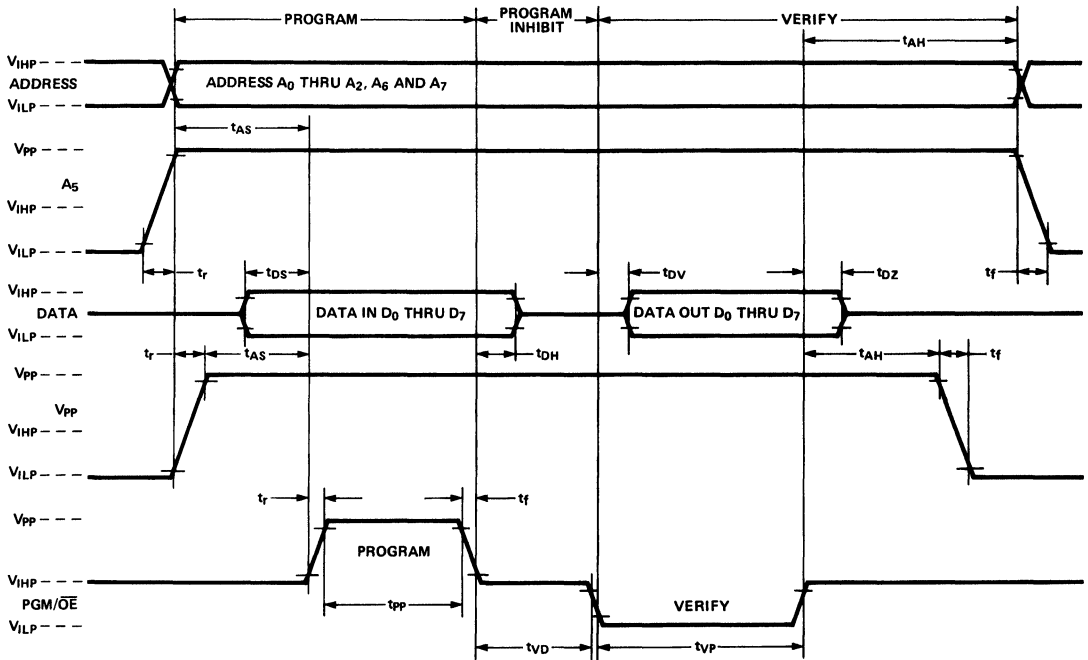
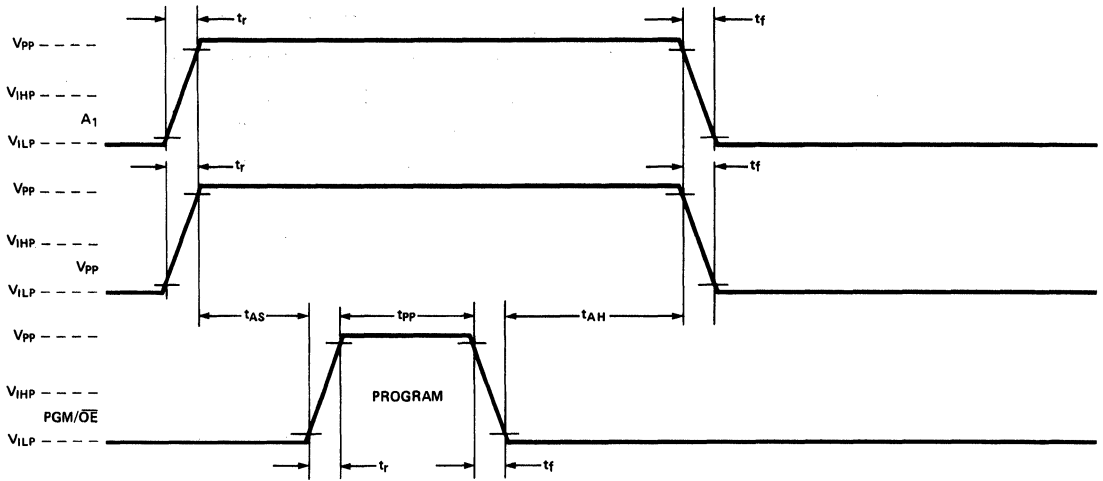


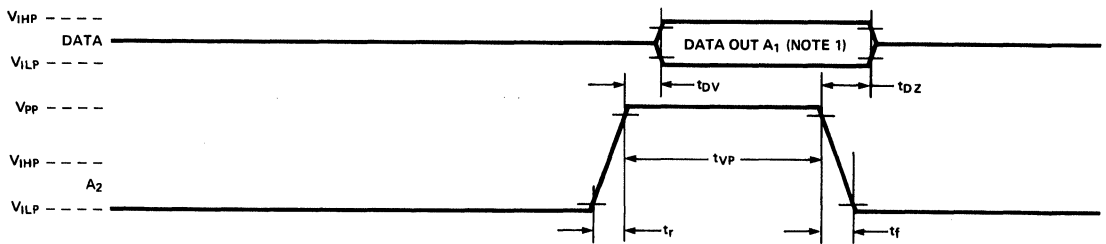
Figure 7. Program Waveforms Phantom Array

0038-18



0038-19

Figure 8. Activating Program Security

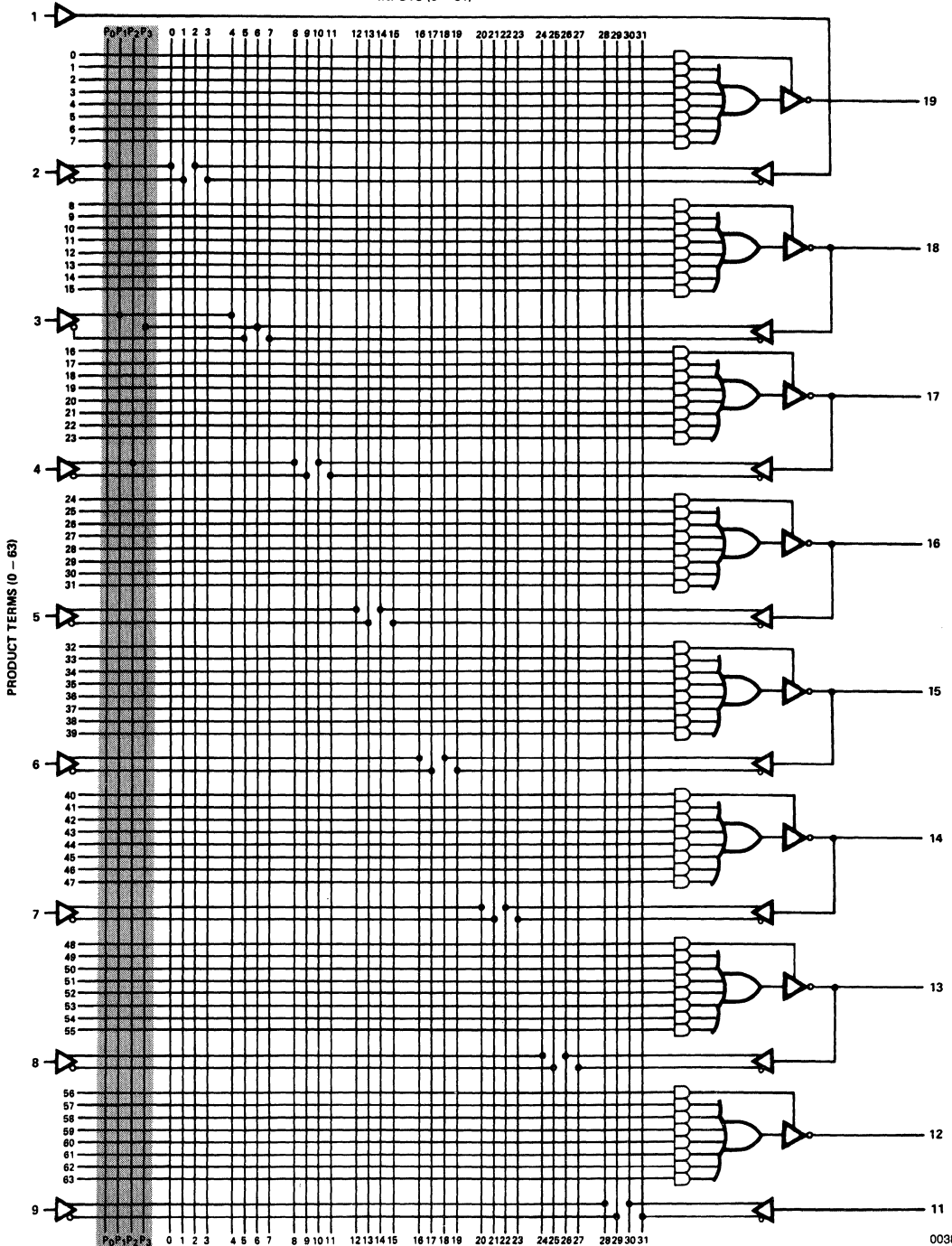


0038-20

Figure 9. Verify Program Security

Functional Logic Diagram PAL C 16L8

INPUTS (0 - 31)

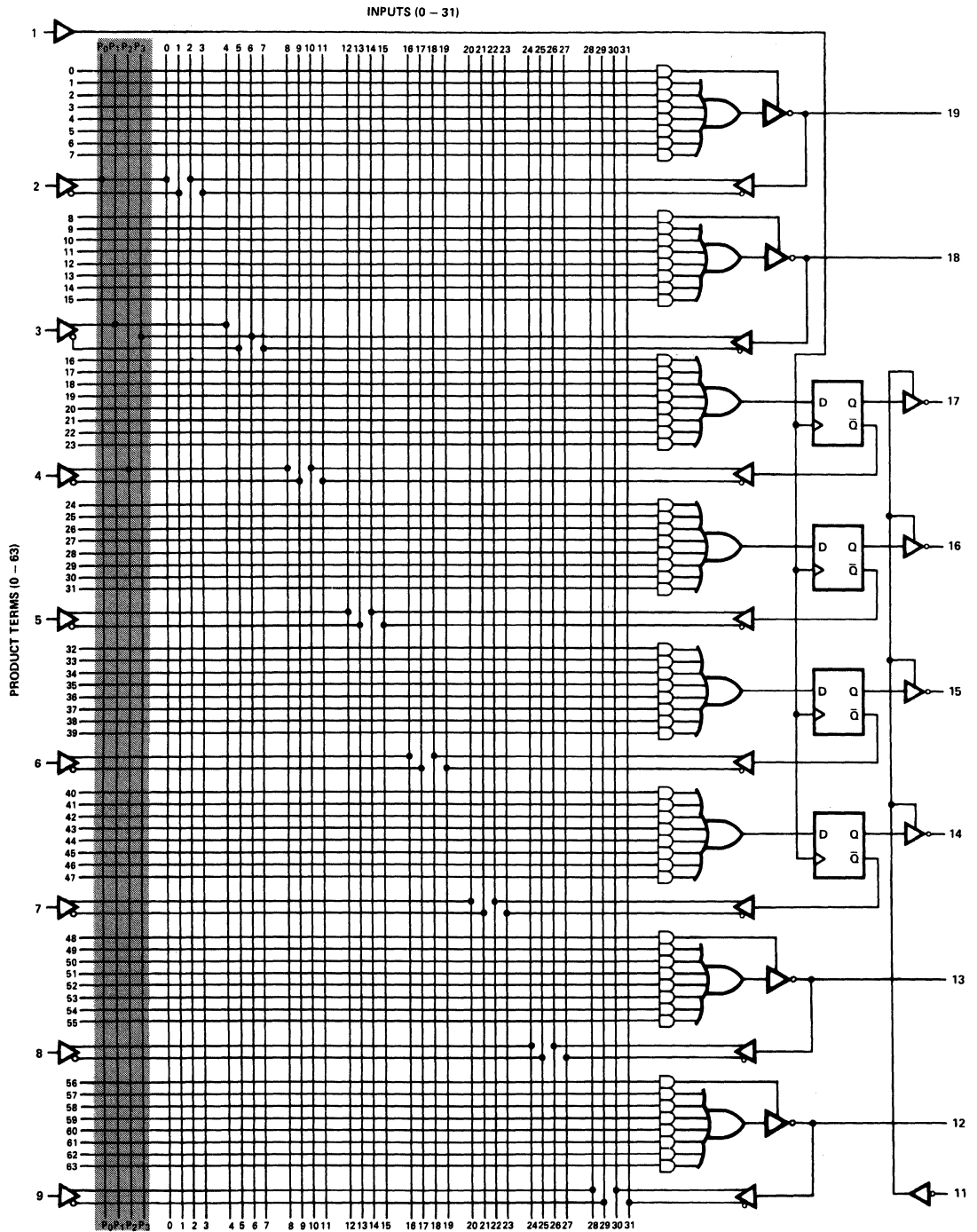


0038-21

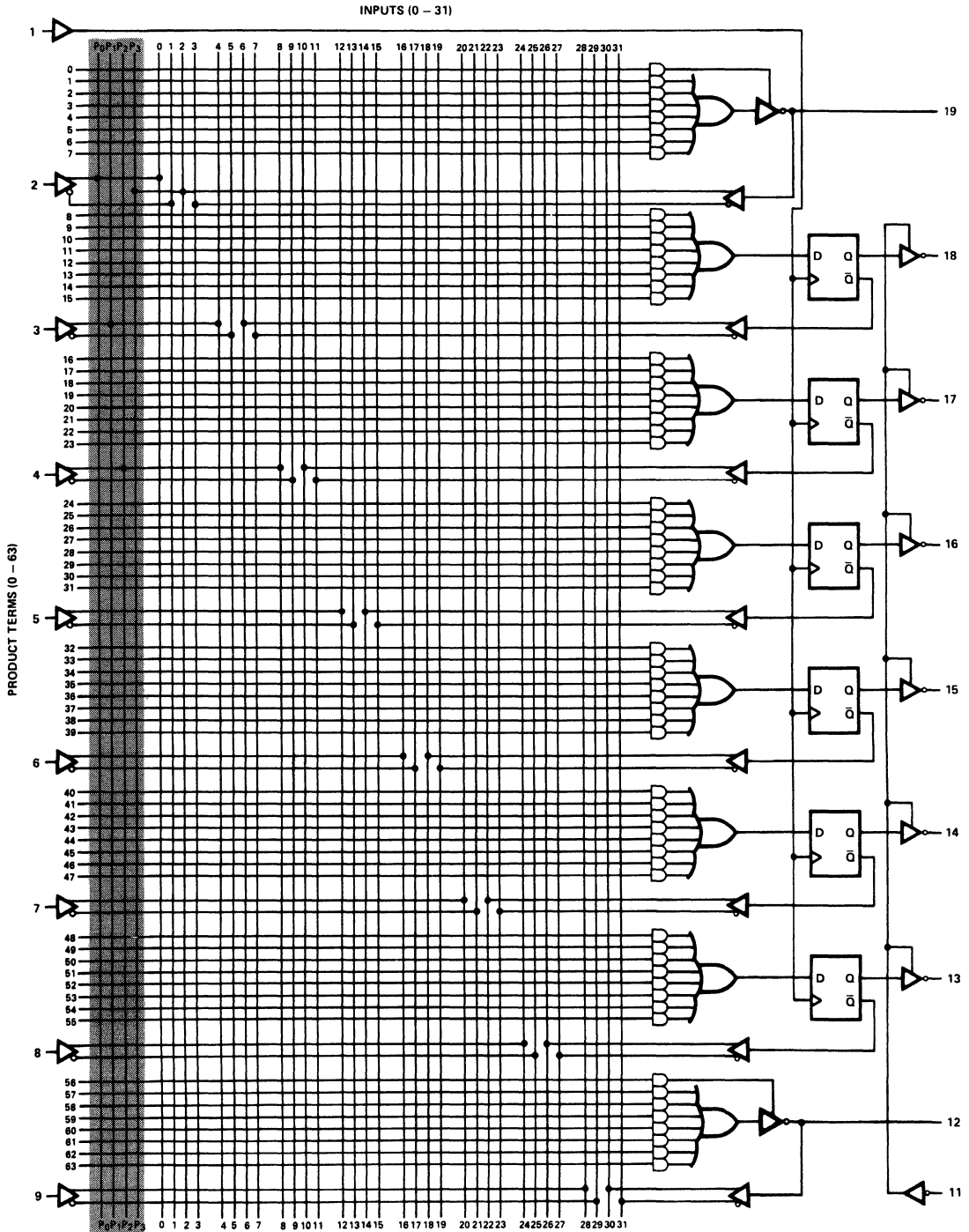
4



**Functional Logic Diagram PAL C 16R4**

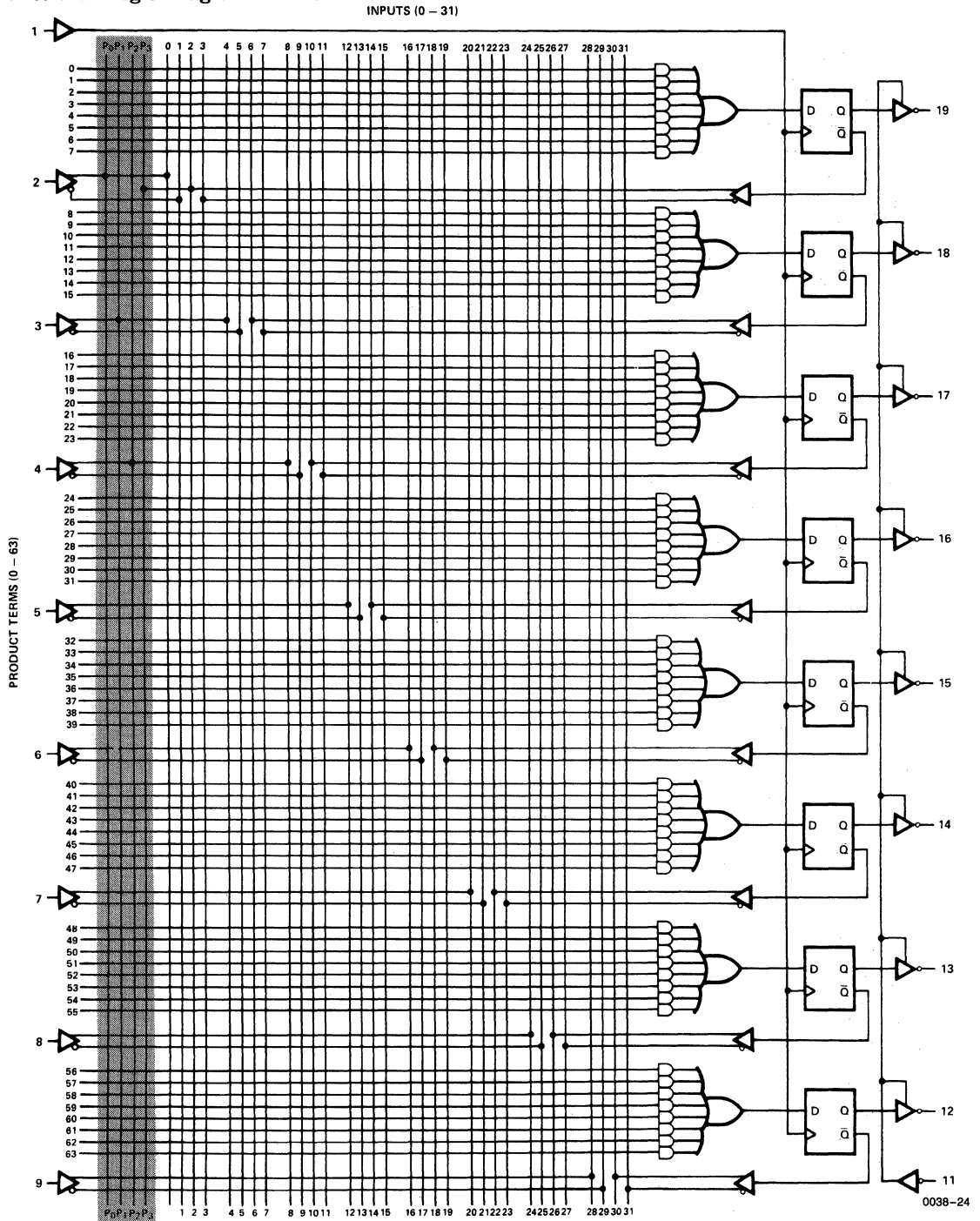


Functional Logic Diagram PAL C 16R6



4

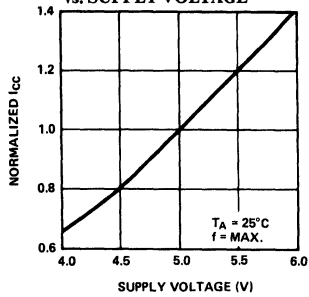
### Functional Logic Diagram PAL C 16R8



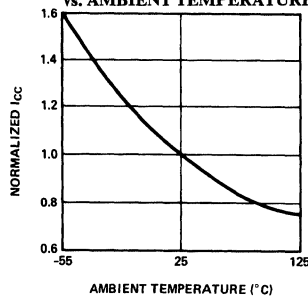
Typical DC and AC Characteristics

4

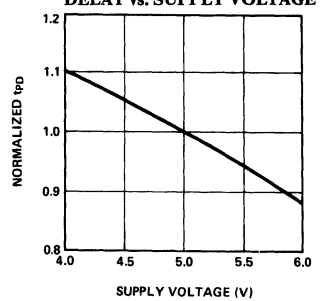
**NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE**



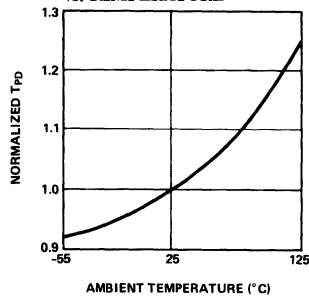
**NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE**



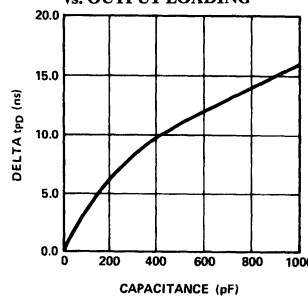
**NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE**



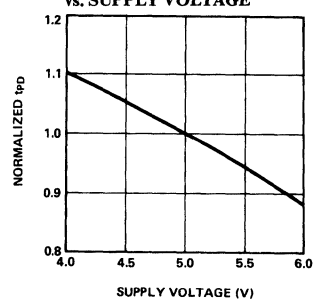
**NORMALIZED PROPAGATION DELAY vs. TEMPERATURE**



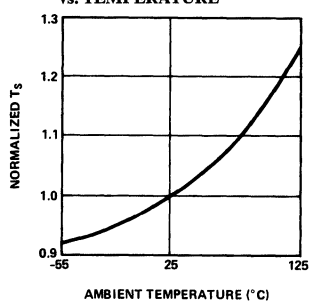
**DELTA PROPAGATION TIME vs. OUTPUT LOADING**



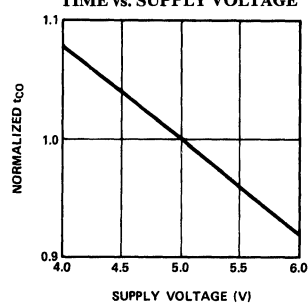
**NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE**



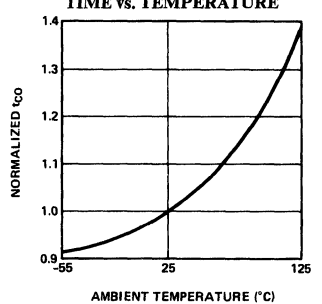
**NORMALIZED SETUP TIME vs. TEMPERATURE**



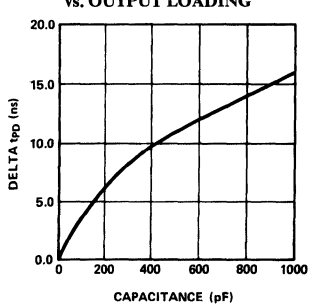
**NORMALIZED CLOCK TO OUTPUT TIME vs. SUPPLY VOLTAGE**



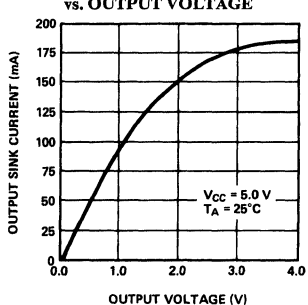
**NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE**



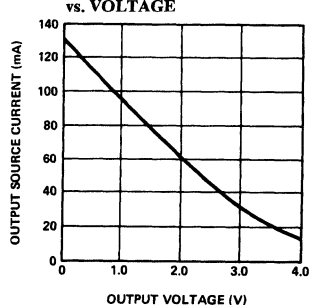
**DELTA CLOCK TO OUTPUT TIME vs. OUTPUT LOADING**



**OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE**



**OUTPUT SOURCE CURRENT vs. VOLTAGE**



**Ordering Information**

| t <sub>PD</sub><br>(ns) | t <sub>s</sub><br>(ns) | t <sub>CO</sub><br>(ns) | I <sub>CC</sub><br>(mA) | Ordering Code      | Package | Operating Range |
|-------------------------|------------------------|-------------------------|-------------------------|--------------------|---------|-----------------|
| 20                      | —                      | —                       | 70                      | PAL C 16L8-20DMB   | D6      | Military        |
|                         |                        |                         |                         | PAL C 16L8-20LMB   | L61     |                 |
|                         |                        |                         |                         | PAL C 16L8-20WMB   | W6      |                 |
|                         |                        |                         |                         | PAL C 16L8-20KMB   | K71     |                 |
|                         |                        |                         |                         | PAL C 16L8-20QMB   | Q61     |                 |
| 25                      | —                      | —                       | 45                      | PAL C 16L8L-25PC   | P5      | Commercial      |
|                         |                        |                         |                         | PAL C 16L8L-25VC   | V5      |                 |
|                         |                        |                         |                         | PAL C 16L8L-25LC   | L61     |                 |
|                         |                        |                         |                         | PAL C 16L8L-25WC   | W6      |                 |
|                         |                        |                         | 70                      | PAL C 16L8-25PC/PI | P5      |                 |
|                         |                        |                         |                         | PAL C 16L8-25VC/VI | V5      |                 |
|                         |                        |                         |                         | PAL C 16L8-25LC    | L61     |                 |
|                         |                        |                         |                         | PAL C 16L8-25WC/WI | W6      |                 |
| 30                      | —                      | —                       | 70                      | PAL C 16L8-30DMB   | D6      | Military        |
|                         |                        |                         |                         | PAL C 16L8-30LMB   | L61     |                 |
|                         |                        |                         |                         | PAL C 16L8-30WMB   | W6      |                 |
|                         |                        |                         |                         | PAL C 16L8-30KMB   | K71     |                 |
|                         |                        |                         |                         | PAL C 16L8-30QMB   | Q61     |                 |
| 35                      | —                      | —                       | 45                      | PAL C 16L8L-35PC   | P5      | Commercial      |
|                         |                        |                         |                         | PAL C 16L8L-35VC   | V5      |                 |
|                         |                        |                         |                         | PAL C 16L8L-35LC   | L61     |                 |
|                         |                        |                         |                         | PAL C 16L8L-35WC   | W6      |                 |
|                         |                        |                         | 70                      | PAL C 16L8-35PC/PI | P5      |                 |
|                         |                        |                         |                         | PAL C 16L8-35VC/VI | V5      |                 |
|                         |                        |                         |                         | PAL C 16L8-35LC    | L61     |                 |
|                         |                        |                         |                         | PAL C 16L8-35WC/WI | W6      |                 |
| 40                      | —                      | —                       | 70                      | PAL C 16L8-40DMB   | D6      | Military        |
|                         |                        |                         |                         | PAL C 16L8-40LMB   | L61     |                 |
|                         |                        |                         |                         | PAL C 16L8-40WMB   | W6      |                 |
|                         |                        |                         |                         | PAL C 16L8-40KMB   | K71     |                 |
|                         |                        |                         |                         | PAL C 16L8-40QMB   | Q61     |                 |
| 20                      | 20                     | 15                      | 70                      | PAL C 16R4-20DMB   | D6      | Military        |
|                         |                        |                         |                         | PAL C 16R4-20LMB   | L61     |                 |
|                         |                        |                         |                         | PAL C 16R4-20WMB   | W6      |                 |
|                         |                        |                         |                         | PAL C 16R4-20KMB   | K71     |                 |
|                         |                        |                         |                         | PAL C 16R4-20QMB   | Q61     |                 |
| 25                      | 20                     | 15                      | 45                      | PAL C 16R4L-25PC   | P5      | Commercial      |
|                         |                        |                         |                         | PAL C 16R4L-25VC   | V5      |                 |
|                         |                        |                         |                         | PAL C 16R4L-25LC   | L61     |                 |
|                         |                        |                         |                         | PAL C 16R4L-25WC   | W6      |                 |
|                         |                        |                         | 70                      | PAL C 16R4-25PC/PI | P5      |                 |
|                         |                        |                         |                         | PAL C 16R4-25VC/VI | V5      |                 |
|                         |                        |                         |                         | PAL C 16R4-25LC    | L61     |                 |
|                         |                        |                         |                         | PAL C 16R4-25WC/WI | W6      |                 |

Ordering Information (Continued)

| t <sub>PD</sub><br>(ns) | t <sub>S</sub><br>(ns) | t <sub>CO</sub><br>(ns) | I <sub>CC</sub><br>(mA) | Ordering Code    | Package | Operating Range |
|-------------------------|------------------------|-------------------------|-------------------------|------------------|---------|-----------------|
| 30                      | 25                     | 20                      | 70                      | PAL C 16R4-30DMB | D6      | Military        |
|                         |                        |                         |                         | PAL C 16R4-30LMB | L61     |                 |
|                         |                        |                         |                         | PAL C 16R4-30WMB | W6      |                 |
|                         |                        |                         |                         | PAL C 16R4-30KMB | K71     |                 |
|                         |                        |                         |                         | PAL C 16R4-30QMB | Q61     |                 |
| 35                      | 30                     | 25                      | 45                      | PAL C 16R4L-35PC | P5      | Commercial      |
|                         |                        |                         |                         | PAL C 16R4L-35VC | V5      |                 |
|                         |                        |                         |                         | PAL C 16R4L-35LC | L61     |                 |
|                         |                        |                         |                         | PAL C 16R4L-35WC | W6      |                 |
|                         |                        | 70                      | PAL C 16R4-35PC/PI      | P5               |         |                 |
|                         |                        |                         | PAL C 16R4-35VC/VI      | V5               |         |                 |
|                         |                        |                         | PAL C 16R4-35LC         | L61              |         |                 |
|                         |                        |                         | PAL C 16R4-35WC/WI      | W6               |         |                 |
| 40                      | 35                     | 25                      | 70                      | PAL C 16R4-40DMB | D6      | Military        |
|                         |                        |                         |                         | PAL C 16R4-40LMB | L61     |                 |
|                         |                        |                         |                         | PAL C 16R4-40WMB | W6      |                 |
|                         |                        |                         |                         | PAL C 16R4-40KMB | K71     |                 |
|                         |                        |                         |                         | PAL C 16R4-40QMB | Q61     |                 |
| 20                      | 20                     | 15                      | 70                      | PAL C 16R6-20DMB | D6      | Military        |
|                         |                        |                         |                         | PAL C 16R6-20LMB | L61     |                 |
|                         |                        |                         |                         | PAL C 16R6-20WMB | W6      |                 |
|                         |                        |                         |                         | PAL C 16R6-20KMB | K71     |                 |
|                         |                        |                         |                         | PAL C 16R6-20QMB | Q61     |                 |
| 25                      | 20                     | 15                      | 45                      | PAL C 16R6L-25PC | P5      | Commercial      |
|                         |                        |                         |                         | PAL C 16R6L-25VC | V5      |                 |
|                         |                        |                         |                         | PAL C 16R6L-25LC | L61     |                 |
|                         |                        |                         |                         | PAL C 16R6L-25WC | W6      |                 |
|                         |                        | 70                      | PAL C 16R6-25PC/PI      | P5               |         |                 |
|                         |                        |                         | PAL C 16R6-25VC/VI      | V5               |         |                 |
|                         |                        |                         | PAL C 16R6-25LC         | L61              |         |                 |
|                         |                        |                         | PAL C 16R6-25WC/WI      | W6               |         |                 |
| 30                      | 25                     | 20                      | 70                      | PAL C 16R6-30DMB | D6      | Military        |
|                         |                        |                         |                         | PAL C 16R6-30LMB | L61     |                 |
|                         |                        |                         |                         | PAL C 16R6-30WMB | W6      |                 |
|                         |                        |                         |                         | PAL C 16R6-30KMB | K71     |                 |
|                         |                        |                         |                         | PAL C 16R6-30QMB | Q61     |                 |
| 35                      | 30                     | 25                      | 45                      | PAL C 16R6L-35PC | P5      | Commercial      |
|                         |                        |                         |                         | PAL C 16R6L-35VC | V5      |                 |
|                         |                        |                         |                         | PAL C 16R6L-35LC | L61     |                 |
|                         |                        |                         |                         | PAL C 16R6L-35WC | W6      |                 |
|                         |                        | 70                      | PAL C 16R6-35PC/PI      | P5               |         |                 |
|                         |                        |                         | PAL C 16R6-35VC/VI      | V5               |         |                 |
|                         |                        |                         | PAL C 16R6-35LC         | L61              |         |                 |
|                         |                        |                         | PAL C 16R6-35WC/WI      | W6               |         |                 |

4

**Ordering Information (Continued)**

| tpD<br>(ns) | ts<br>(ns) | tCO<br>(ns) | ICC<br>(mA) | Ordering Code      | Package | Operating Range |
|-------------|------------|-------------|-------------|--------------------|---------|-----------------|
| 40          | 35         | 25          | 70          | PAL C 16R6-40DMB   | D6      | Military        |
|             |            |             |             | PAL C 16R6-40LMB   | L61     |                 |
|             |            |             |             | PAL C 16R6-40WMB   | W6      |                 |
|             |            |             |             | PAL C 16R6-40KMB   | K71     |                 |
|             |            |             |             | PAL C 16R6-40QMB   | Q61     |                 |
| —           | 20         | 15          | 70          | PAL C 16R8-20DMB   | D6      | Military        |
|             |            |             |             | PAL C 16R8-20LMB   | L61     |                 |
|             |            |             |             | PAL C 16R8-20WMB   | W6      |                 |
|             |            |             |             | PAL C 16R8-20KMB   | K71     |                 |
|             |            |             |             | PAL C 16R8-20QMB   | Q61     |                 |
| —           | 20         | 15          | 45          | PAL C 16R8L-25PC   | P5      | Commercial      |
|             |            |             |             | PAL C 16R8L-25VC   | V5      |                 |
|             |            |             |             | PAL C 16R8L-25LC   | L61     |                 |
|             |            |             |             | PAL C 16R8L-25WC   | W6      |                 |
|             |            |             | 70          | PAL C 16R8-25PC/PI | P5      |                 |
|             |            |             |             | PAL C 16R8-25VC/VI | V5      |                 |
|             |            |             |             | PAL C 16R8-25LC    | L61     |                 |
|             |            |             |             | PAL C 16R8-25WC/WI | W6      |                 |
| —           | 25         | 20          | 70          | PAL C 16R8-30DMB   | D6      | Military        |
|             |            |             |             | PAL C 16R8-30LMB   | L61     |                 |
|             |            |             |             | PAL C 16R8-30WMB   | W6      |                 |
|             |            |             |             | PAL C 16R8-30KMB   | K71     |                 |
|             |            |             |             | PAL C 16R8-30QMB   | Q61     |                 |
| —           | 30         | 25          | 45          | PAL C 16R8L-35PC   | P5      | Commercial      |
|             |            |             |             | PAL C 16R8L-35VC   | V5      |                 |
|             |            |             |             | PAL C 16R8L-35LC   | L61     |                 |
|             |            |             |             | PAL C 16R8L-35WC   | W6      |                 |
|             |            |             | 70          | PAL C 16R8-35PC/PI | P5      |                 |
|             |            |             |             | PAL C 16R8-35VC/VI | V5      |                 |
|             |            |             |             | PAL C 16R8-35LC    | L61     |                 |
|             |            |             |             | PAL C 16R8-35WC/WI | W6      |                 |
| —           | 35         | 25          | 70          | PAL C 16R8-40DMB   | D6      | Military        |
|             |            |             |             | PAL C 16R8-40LMB   | L61     |                 |
|             |            |             |             | PAL C 16R8-40WMB   | W6      |                 |
|             |            |             |             | PAL C 16R8-40KMB   | K71     |                 |
|             |            |             |             | PAL C 16R8-40QMB   | Q61     |                 |

**MILITARY SPECIFICATIONS****Group A Subgroup Testing****DC Characteristics**

| Parameters      | Subgroups |
|-----------------|-----------|
| V <sub>OH</sub> | 1,2,3     |
| V <sub>OL</sub> | 1,2,3     |
| V <sub>IH</sub> | 1,2,3     |
| V <sub>IL</sub> | 1,2,3     |
| I <sub>Ix</sub> | 1,2,3     |
| V <sub>PP</sub> | 1,2,3     |
| I <sub>CC</sub> | 1,2,3     |
| I <sub>OZ</sub> | 1,2,3     |

4

**Switching Characteristics**

| Parameters       | Subgroups |
|------------------|-----------|
| t <sub>PD</sub>  | 9,10,11   |
| t <sub>PZX</sub> | 9,10,11   |
| t <sub>CO</sub>  | 9,10,11   |
| t <sub>S</sub>   | 9,10,11   |
| t <sub>H</sub>   | 9,10,11   |

Document #: 38-00001-C





# CMOS Generic 20 Pin Programmable Logic Device

## Features

- **Fast**
  - Commercial:  $t_{PD} = 12$  ns,  $t_{CO} = 10$  ns,  $t_S = 12$  ns
  - Military:  $t_{PD} = 15$  ns,  $t_{CO} = 12$  ns,  $t_S = 15$  ns
- **Low power**
  - ICC max.: 80 mA, commercial
  - ICC max.: 110 mA, military
- **Commercial and military temperature range**
- **User-programmable output cells**
  - Selectable for registered or combinatorial operation
  - Output polarity control
  - Output enable source selectable from pin 11 or product term
- **Generic architecture to replace standard logic functions** including: 10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2, 10P8, 12P6, 14P4, 16P2, 16H8, 16L8, 16P8, 16R8, 16R6, 16R4, 16RP8, 16RP6, 16RP4, 18P8, 16V8
- **Eight product terms and one OE product term per output**
- **CMOS EPROM technology for reprogrammability**
- **Highly reliable**
  - Uses proven EPROM technology
  - Fully AC and DC tested
- Security feature prevents logic pattern duplication
- >2000V input protection for electrostatic discharge

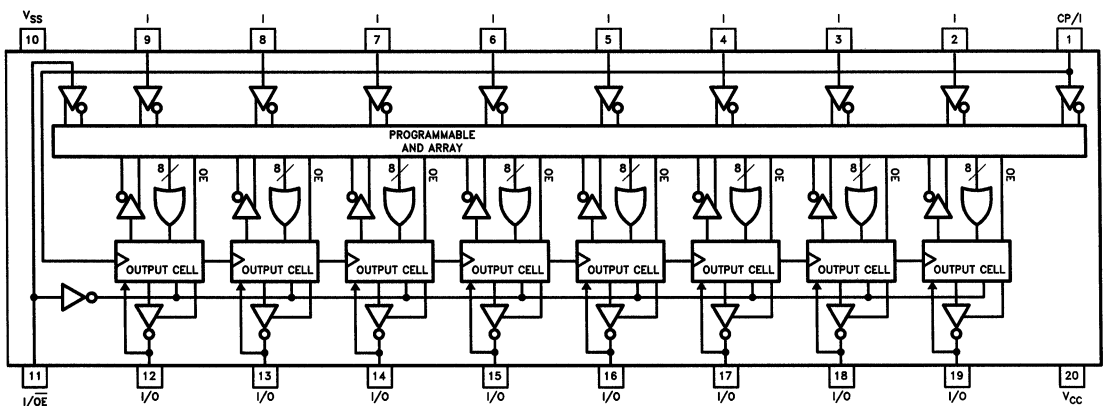
## Functional Description

Cypress PLD devices are high speed electrically programmable Logic Devices. These devices utilize the sum of products (AND-OR) structure providing users the ability to program custom logic functions for unique requirements.

In an unprogrammed state the AND gates are connected via EPROM cells to both the true and complement of every input. By selectively programming the EPROM cells, AND gates may be

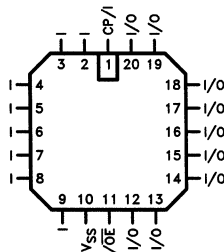
## Logic Symbol, DIP and SOJ Pinout

18G8



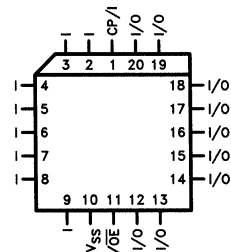
0139-1

## LCC Pinout



0139-2

## PLCC Pinout



0139-3

## Selection Guide

| Generic Part Number | I <sub>CC</sub> (mA) |     | t <sub>PD</sub> (ns) |     | t <sub>s</sub> |     | t <sub>CO</sub> |     |
|---------------------|----------------------|-----|----------------------|-----|----------------|-----|-----------------|-----|
|                     | Com                  | Mil | Com                  | Mil | Com            | Mil | Com             | Mil |
| 18G8-12             | 80                   |     | 12                   |     | 12             |     | 10              |     |
| 18G8-15             | 80                   | 110 | 15                   | 15  | 12             | 15  | 12              | 12  |
| 18G8-20             |                      | 110 |                      | 20  |                | 20  |                 | 15  |

### Functional Description (Continued)

connected to either the true or complement or disconnected from both true and complement inputs.

Cypress PLD C 18G8 uses an advanced 0.8 micron CMOS technology and a proven EPROM cell as the programmable element. This technology and the inherent advantage of being able to program and erase each cell enhances the reliability and testability of the circuit. This reduces the burden on the customer to test and to handle rejects.

A preload function allows the registered outputs to be preset to any pattern during testing. Preload is important for testing the functionality of the Cypress PLD device.

### 18G8 Functional Description

The PLD C 18G8 is a generic 20 pin device that can be programmed to logic functions which include but are not limited to: 10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2, 10P8, 12P6, 14P4, 16P2, 16H8, 16L8, 16P8, 16R8, 16R6, 16R4, 16RP8, 16RP6, 16RP4, 18P8, 16V8. Thus, the PLD C 18G8 provides significant design, inventory and programming flexibility over dedicated 20 pin devices. It is executed in a 20 pin 300 mil molded DIP and a 300 mil windowed Cerdip. It provides up to 18 inputs and 8 outputs. When the windowed CERDIP is exposed to UV light, the 18G8 is erased and then can be reprogrammed.

The Programmable Output Cell provides the capability of defining the architecture of each output individually. Each of the 10 output cells may be configured with "REGISTERED" or "COMBINATORIAL" outputs, "ACTIVE HIGH" or "ACTIVE LOW" outputs, and "PRODUCT TERM" or "PIN 11" generated output enables. Four Architecture Bits determine the configurations as shown in Table 1. A total of sixteen different configurations are possible. The default or unprogrammed state is REGISTERED/ACTIVE/LOW/Pin 11 OE. The entire Programmable Output Cell is shown in Figure 1.

The architecture bit 'C1' controls the REGISTERED/COMBINATORIAL option. In either "COMBINATORIAL" or "REGISTERED" configuration, the output can serve as an I/O pin, or if the output is disabled, as an input only. Any unused inputs should be tied to ground. In either "REGISTERED" or "COMBINATORIAL" configuration, the output of the register may be fed back to the array. This allows the creation of control-state machines by

providing the next state. The register is clocked by the signal from Pin 1. The register is initialized on power up to Q output LOW and  $\bar{Q}$  output HIGH.

In both the Combinatorial and Registered configurations, the source of the "OUTPUT ENABLE" signal can be individually chosen with architecture bit 'C2'. The OE signal may be generated within the array, or from the external  $\bar{O}E$  pin (Pin 11). The Pin 11 allows direct control of the outputs, hence having faster enable/disable times.

Each output cell can be configured for "OUTPUT POLARITY". The output can be either Active HIGH or Active LOW. This option is controlled by architecture bit 'C0'.

Along with this increase in functional density, the Cypress PLD C 18G8 provides lower power operation through the use of CMOS technology, increased testability with a register preload feature and guaranteed AC performance through the use of a phantom array. The phantom array allows the 18G8 to be programmed with a test pattern and tested prior to shipment for full AC specifications without using any of the functionality of the device specified for the product application. In addition, this same phantom array may be used to test the PLD C 18G8 at incoming inspection before committing the device to a specific function through programming.

### Programmable Output Cell

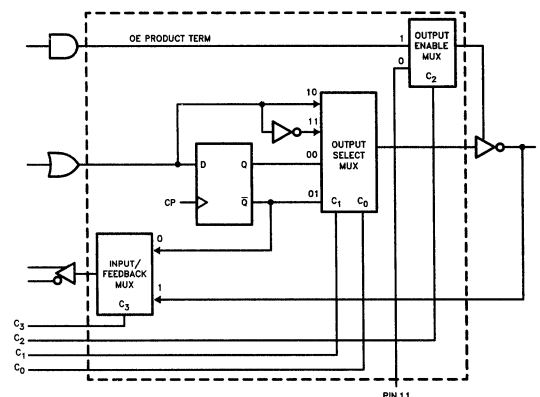


Figure 1

0139-4

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature                           | -65°C to +150°C |
| Ambient Temperature with Power Applied        | -55°C to +125°C |
| Supply Voltage to Ground Potential            | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State | -0.5V to +7.0V  |
| DC Input Voltage                              | -3.0V to +7.0V  |
| Output Current into Outputs (Low)             | 24 mA           |
| DC Programming Voltage                        | 13.0V           |

|  |          |
|--|----------|
| Static Discharge Voltage (per MIL-STD-883 Method 3015) | > 2001V  |
| Latchup Current  | > 200 mA |

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +75°C        | 5V ± 5%         |
| Military <sup>[7]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range (Unless Otherwise Noted)<sup>[7]</sup>

| Parameters      | Description                  | Test Conditions  |  | Min. | Max.      | Units |    |
|-----------------|------------------------------|--|--|------|-----------|-------|----|
|                 |                              | V <sub>CC</sub> = Min.<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>           | I <sub>OH</sub> = -3.2 mA<br>Commercial<br>I <sub>OH</sub> = -2 mA<br>Military |      |           |       |    |
| V <sub>OH</sub> | Output HIGH Voltage          |  |  | 2.4  |           | V     |    |
| V <sub>OL</sub> | Output LOW Voltage           | V <sub>CC</sub> = Min.<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>           | I <sub>OL</sub> = 24 mA<br>Commercial<br>I <sub>OL</sub> = 12 mA<br>Military   |      | 0.5       | V     |    |
| V <sub>IH</sub> | Input HIGH Level             | Guaranteed Input Logical HIGH <sup>[1]</sup> Voltage for all Inputs                      |  |      | 2.0       |       | V  |
| V <sub>IL</sub> | Input LOW Level              | Guaranteed Input Logical LOW <sup>[1]</sup> Voltage for all Inputs                       |  |      |           | 0.8   | V  |
| I <sub>IX</sub> | Input Leakage Current        | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                                      |  |      | -10       | 10    | μA |
| V <sub>PP</sub> |                              | Programming Voltage @ I <sub>PP</sub> = 50 mA Max.                                       |  |      | 12.0      | 13.0  | V  |
| I <sub>SC</sub> | Output Short Circuit Current | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V <sup>[2]</sup>                           |  |      | -30       | -90   | mA |
| I <sub>CC</sub> | Power Supply Current         | 0 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub><br>V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA | Commercial<br>Military   |      | 80<br>110 | mA    |    |
| I <sub>OZ</sub> | Output Leakage Current       | V <sub>CC</sub> = Max., V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>             |  |      | -40       | 40    | mA |

### Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions                                | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz               | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance | V <sub>IN</sub> = 2.0V, V <sub>CC</sub> = 5.0V | 8    |       |

### AC Test Loads and Waveforms (Commercial)

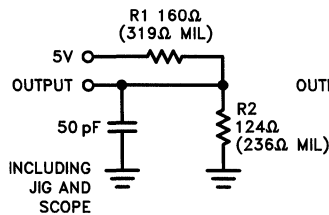
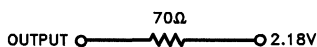


Figure 2a

Equivalent to: THÉVENIN EQUIVALENT (Commercial)



0139-6

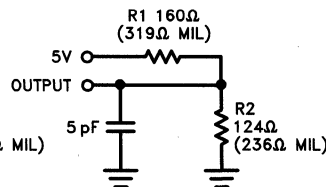
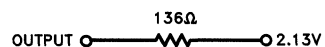


Figure 2b

Equivalent to: THÉVENIN EQUIVALENT (Military)



0139-7

**Configuration Table<sup>[8]</sup>**
**Table 1**

| C <sub>3</sub> | C <sub>2</sub> | C <sub>1</sub> | C <sub>0</sub> | Configuration   |
|----------------|----------------|----------------|----------------|---|
| 0              | 0              | 0              | 0              | Active LOW, Registered Mode, Registered Feedback, Pin 11 OE           |
| 0              | 0              | 0              | 1              | Active HIGH, Registered Mode, Registered Feedback, Pin 11 OE          |
| 0              | 0              | 1              | 0              | Active LOW, Combinatorial Mode, Registered Feedback, Pin 11 OE        |
| 0              | 0              | 1              | 1              | Active HIGH, Combinatorial Mode, Registered Feedback, Pin 11 OE       |
| 0              | 1              | 0              | 0              | Active LOW, Registered Mode, Registered Feedback, Product Term OE     |
| 0              | 1              | 0              | 1              | Active HIGH, Registered Mode, Registered Feedback, Product Term OE    |
| 0              | 1              | 1              | 0              | Active LOW, Combinatorial Mode, Registered Feedback, Product Term OE  |
| 0              | 1              | 1              | 1              | Active HIGH, Combinatorial Mode, Registered Feedback, Product Term OE |
| 1              | 0              | 0              | 0              | Active LOW, Registered Mode, Pin Feedback, Pin 11 OE                  |
| 1              | 0              | 0              | 1              | Active HIGH, Registered Mode, Pin Feedback, Pin 11 OE                 |
| 1              | 0              | 1              | 0              | Active LOW, Combinatorial Mode, Pin Feedback, Pin 11 OE               |
| 1              | 0              | 1              | 1              | Active HIGH, Combinatorial Mode, Pin Feedback, Pin 11 OE              |
| 1              | 1              | 0              | 0              | Active LOW, Registered Mode, Pin Feedback, Product Term OE            |
| 1              | 1              | 0              | 1              | Active HIGH, Registered Mode, Pin Feedback, Product Term OE           |
| 1              | 1              | 1              | 0              | Active LOW, Combinatorial Mode, Pin Feedback, Product Term OE         |
| 1              | 1              | 1              | 1              | Active HIGH, Combinatorial Mode, Pin Feedback, Product Term OE        |

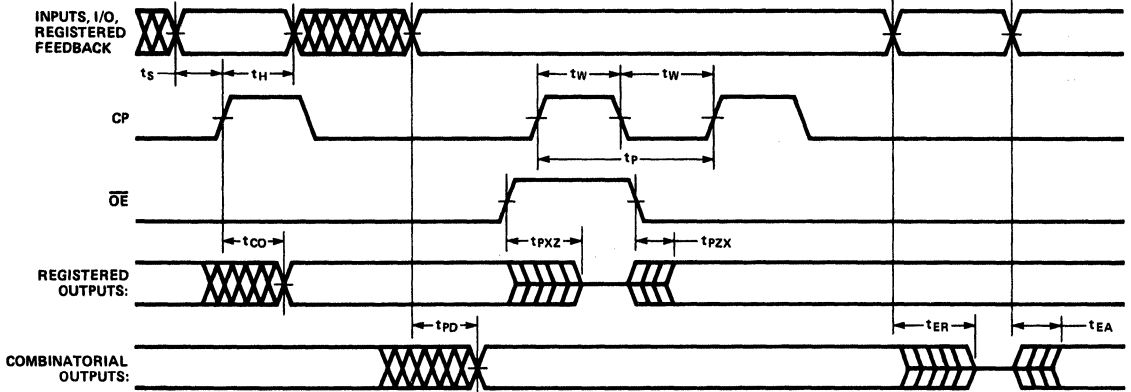
**4**
**Switching Characteristics PLD C 18G8 Over Operating Range<sup>[4, 9]</sup>**

| Parameters                      | Description                                | Commercial |      |      |      | Military |      |      |      | Units |
|---------------------------------|--|------------|------|------|------|----------|------|------|------|-------|
|                                 |  | - 12       |      | - 15 |      | - 15     |      | - 20 |      |       |
|                                 |  | Min.       | Max. | Min. | Max. | Min.     | Max. | Min. | Max. |       |
| t <sub>PD</sub>                 | Input or Feedback to Non-Registered Output |            | 12   |      | 15   |          | 15   |      | 20   | ns    |
| t <sub>EA</sub>                 | Input to Output Enable                     |            | 12   |      | 15   |          | 15   |      | 20   | ns    |
| t <sub>ER</sub>                 | Input to Output Disable                    |            | 12   |      | 15   |          | 15   |      | 20   | ns    |
| t <sub>PZX</sub>                | Pin 11 to Output Enable                    |            | 10   |      | 12   |          | 12   |      | 15   | ns    |
| t <sub>PXZ</sub>                | Pin 11 to Output Disable                   |            | 10   |      | 10   |          | 10   |      | 15   | ns    |
| t <sub>CO</sub>                 | Clock to Output                            |            | 10   |      | 12   |          | 12   |      | 15   | ns    |
| t <sub>S</sub>                  | Input or Feedback Setup Time               | 12         |      | 12   |      | 15       |      | 20   |      | ns    |
| t <sub>H</sub>                  | Hold Time                                  | 0          |      | 0    |      | 0        |      | 0    |      | ns    |
| t <sub>p</sub> <sup>[5]</sup>   | Clock Period                               | 22         |      | 24   |      | 27       |      | 35   |      | ns    |
| t <sub>WH</sub>                 | Clock High Time                            | 7          |      | 8    |      | 9        |      | 10   |      | ns    |
| t <sub>WL</sub>                 | Clock Low Time                             | 8          |      | 9    |      | 10       |      | 11   |      | ns    |
| f <sub>MAX</sub> <sup>[6]</sup> | Maximum Frequency                          | 45.5       |      | 41.6 |      | 37.0     |      | 28.6 |      | MHz   |

**Notes:**

- These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V<sub>OUT</sub> = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.
- Figure 2a test load used for all parameters except t<sub>ER</sub>, t<sub>PZX</sub> and t<sub>PXZ</sub>. Figure 2b test load used for t<sub>ER</sub>, t<sub>PZX</sub> and t<sub>PXZ</sub>.
- t<sub>p</sub>, minimum guaranteed clock period is that guaranteed for state machine operation and is calculated from t<sub>p</sub> = t<sub>S</sub> + t<sub>CO</sub>. The minimum guaranteed period for registered data path operation (no feedback) can be calculated as the greater of (t<sub>WH</sub> + t<sub>WL</sub>) or (t<sub>S</sub> + t<sub>H</sub>).
- f<sub>MAX</sub>, minimum guaranteed operating frequency, is that guaranteed for state machine operation and is calculated from f<sub>MAX</sub> = 1/(t<sub>S</sub> + t<sub>CO</sub>). The minimum guaranteed f<sub>MAX</sub> for registered data path operation (no feedback) can be calculated as the lower of 1/(t<sub>WH</sub> + t<sub>WL</sub>) or 1/(t<sub>S</sub> + t<sub>H</sub>).
- T<sub>A</sub> is the "instant on" case temperature.
- In the virgin or unprogrammed state, a configuration bit location is in the "0" state.
- The parameters t<sub>ER</sub> and t<sub>PXZ</sub> are measured as the delay from the input disable logic threshold transition to V<sub>OH</sub> - 0.5V for an enabled HIGH output or V<sub>OL</sub> + 0.5V for an enabled LOW output.

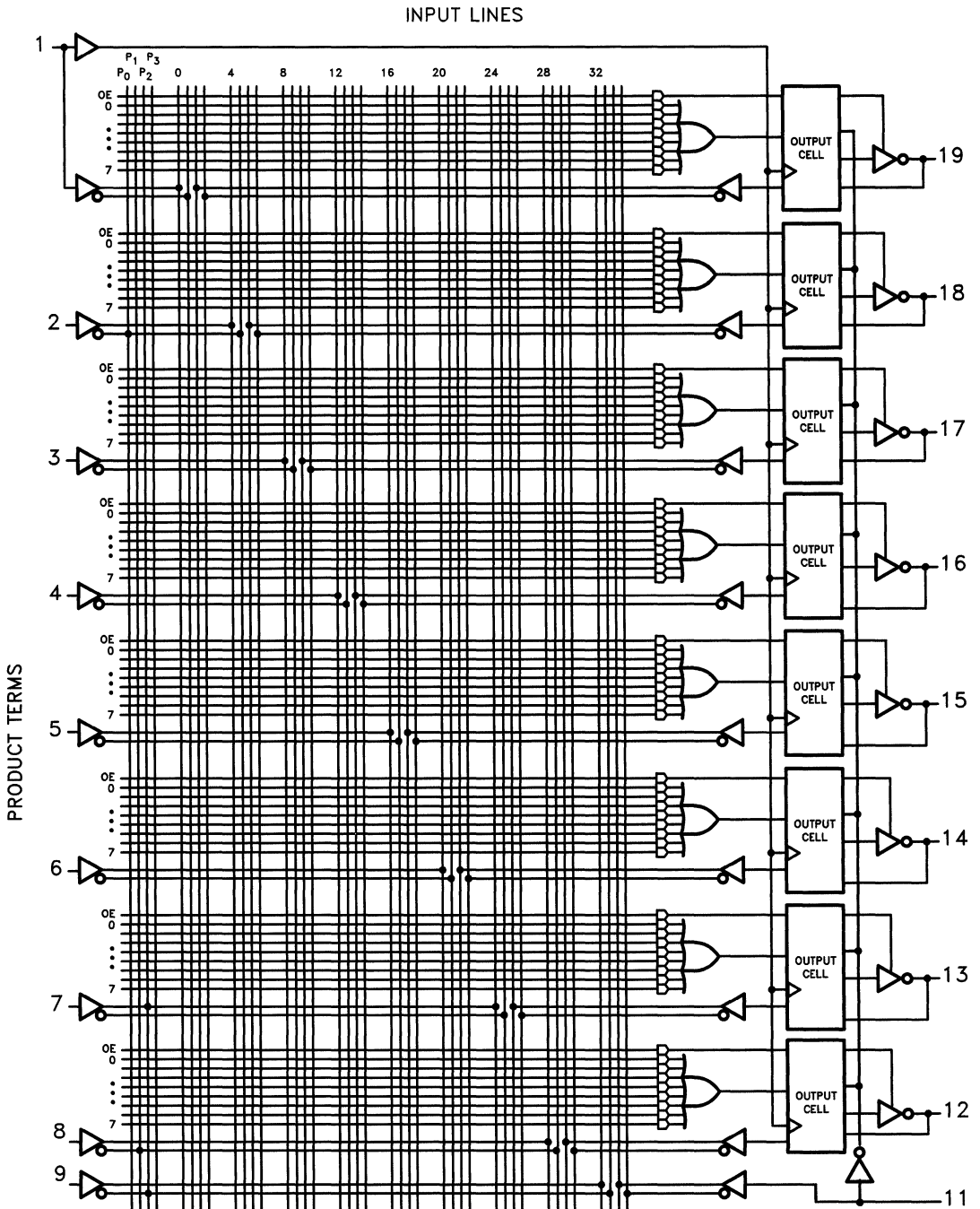
### Switching Waveform



0139-8

**Note:**  
For more information regarding PLD devices, refer to the Application Brief in the Appendix.

Functional Logic Diagram PLD C 18G8



4

**Ordering Information**

| Speed (ns) | Ordering Code    | Package Type | Operating Range |
|------------|------------------|--------------|-----------------|
| 12         | PLD C 18G8-12PC  | P5           | Commercial      |
|            | PLD C 18G8-12WC  | W6           |                 |
|            | PLD C 18G8-12VC  | V5           |                 |
|            | PLD C 18G8-12JC  | J61          |                 |
| 15         | PLD C 18G8-15PC  | P5           | Commercial      |
|            | PLD C 18G8-15WC  | W6           |                 |
|            | PLD C 18G8-15VC  | V5           |                 |
|            | PLD C 18G8-15JC  | J61          |                 |
|            | PLD C 18G8-15DMB | D6           | Military        |
|            | PLD C 18G8-15WMB | W6           |                 |
|            | PLD C 18G8-15LMB | L61          |                 |
| 20         | PLD C 18G8-20DMB | D6           | Military        |
|            | PLD C 18G8-20WMB | W6           |                 |
|            | PLD C 18G8-20LMB | L61          |                 |

Document #: 38-00080



CMOS Generic 24 Pin  
Reprogrammable Logic Device

Features

- Fast
  - Commercial:  $t_{PD} = 15$  ns,  $t_{CO} = 10$  ns,  $t_S = 12$  ns
  - Military:  $t_{PD} = 20$  ns,  $t_{CO} = 15$  ns,  $t_S = 17$  ns
- Low power
  - $I_{CC}$  max.: 70 mA, Commercial
  - $I_{CC}$  max.: 100 mA, Military
- Commercial and military temperature range
- User-programmable output cells
  - Selectable for registered or combinatorial operation
  - Output polarity control
  - Output enable source selectable from pin 13 or product term

- Generic architecture to replace standard logic functions including: 20L10, 20L8, 20R8, 20R6, 20R4, 12L10, 14L8, 16L6, 18L4, 20L2 and 20V8
- Eight product terms and one OE product term per output
- CMOS EPROM technology for reprogrammability
- Highly reliable
  - Uses proven EPROM technology
  - Fully AC and DC tested
  - Security feature prevents logic pattern duplication
  - > 2000V input protection for electrostatic discharge
  - $\pm 10\%$  power supply voltage and higher noise immunity

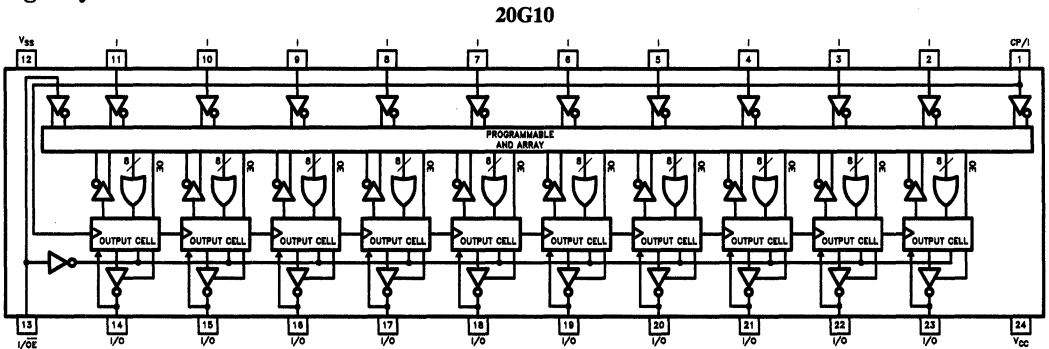
Functional Description

Cypress PLD devices are high speed electrically programmable Logic Devices. These devices utilize the sum of products (AND-OR) structure providing users the ability to program custom logic functions for unique requirements.

In an unprogrammed state the AND gates are connected via EPROM cells to both the true and complement of every input. By selectively programming the EPROM cells, AND gates may be connected to either the true or complement or disconnected from both true and complement inputs.

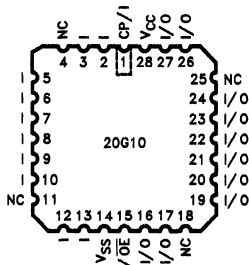
Cypress PLD C 20G10 uses an advanced 0.8 micron CMOS technology and a proven EPROM cell as the pro-

Logic Symbol



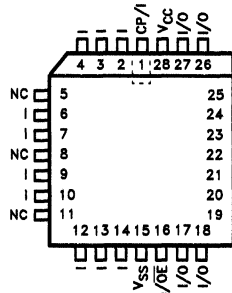
0053-15

LCC Pinout



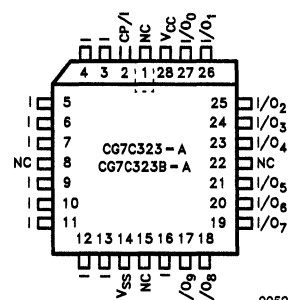
0053-17

STD PLCC Pinout



0053-26

JEDEC PLCC Pinout [16]



0053-41



## Selection Guide

| Generic Part Number | Icc |         |     | tpD     |     | ts      |     | tco     |     |
|---------------------|-----|---------|-----|---------|-----|---------|-----|---------|-----|
|                     | L   | Com/Ind | Mil | Com/Ind | Mil | Com/Ind | Mil | Com/Ind | Mil |
| 20G10B-15           | —   | 70      | —   | 15      | —   | 12      | —   | 10      | —   |
| 20G10B-20           | —   | 70      | 100 | 20      | 20  | —       | 17  | —       | 15  |
| 20G10B-25           | —   | —       | 100 | —       | 25  | —       | 18  | —       | 15  |
| 20G10-25            | —   | 55      | —   | 25      | —   | 15      | —   | 15      | —   |
| 20G10-30            | —   | —       | 80  | —       | 30  | —       | 20  | —       | 20  |
| 20G10-35            | —   | 55      | —   | 35      | —   | 30      | —   | 25      | —   |
| 20G10-40            | —   | —       | 80  | —       | 40  | —       | 35  | —       | 25  |

### Functional Description (Continued)

grammable element. This technology and the inherent advantage of being able to program and erase each cell enhances the reliability and testability of the circuit. This reduces the burden on the customer to test and to handle rejects.

A preload function allows the registered outputs to be preset to any pattern during testing. Preload is important for testing the functionality of the Cypress PLD device.

### 20G10 Functional Description

The PLD C 20G10 is a generic 24 pin device that can be programmed to logic functions which include but are not limited to: 20L10, 20L8, 20R8, 20R6, 20R4, 12L10, 14L8, 16L6, 18L4, 20L2 and 20V8. Thus, the PLD C 20G10 provides significant design, inventory and programming flexibility over dedicated 24 pin devices. It is executed in a 24 pin 300 mil molded DIP and a 300 mil windowed Cer-dip. It provides up to 22 inputs and 10 outputs. When the windowed CERDIP is exposed to UV light, the 20G10 is erased and then can be reprogrammed.

The Programmable Output Cell provides the capability of defining the architecture of each output individually. Each of the 10 output cells may be configured with "REGISTERED" or "COMBINATORIAL" outputs, "ACTIVE HIGH" or "ACTIVE LOW" outputs, and "PRODUCT TERM" or "PIN 13" generated output enables. Three Architecture Bits determine the configurations as shown in Table 1 and in Figures 2 through 9. A total of eight different configurations are possible, with the two most common shown in Figure 4 and Figure 6. The default or unprogrammed state is REGISTERED/ACTIVE LOW/PRODUCT TERM OE as shown in Figure 2. The entire Programmable Output Cell is shown in Figure 1.

The architecture bit 'C1' controls the REGISTERED/COMBINATORIAL option. In the "COMBINATORIAL" configuration, the output can serve as an I/O pin, or if the output is disabled, as an input only. Any unused inputs should be tied to ground. In the "REGISTERED" configuration, the output of the register is fed back to the array. This allows the creation of control-state machines by providing the next state. The register is clocked by the

signal from Pin 1. The register is initialized on power up to Q output LOW and Q output HIGH.

In both the Combinatorial and Registered configurations, the source of the "OUTPUT ENABLE" signal can be individually chosen with architecture bit 'C2'. The OE signal may be generated within the array, or from the external OE pin (Pin 13). The Pin 13 allows direct control of the outputs, hence having faster enable/disable times.

Each output cell can be configured for "OUTPUT POLARITY". The output can be either Active HIGH or Active LOW. This option is controlled by architecture bit 'CO'.

Along with this increase in functional density, the Cypress PLD C 20G10 provides lower power operation through the use of CMOS technology, increased testability with a register preload feature and guaranteed AC performance through the use of a phantom array. The phantom array allows the 20G10 to be programmed with a test pattern and tested prior to shipment for full AC specifications without using any of the functionality of the device specified for the product application. In addition, this same phantom array may be used to test the PLD C 20G10 at incoming inspection before committing the device to a specific function through programming.

### Programmable Output Cell

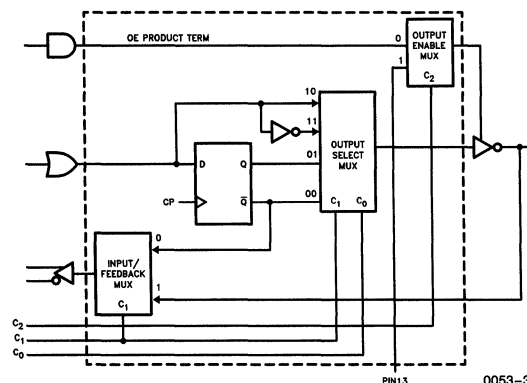


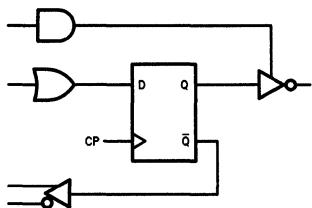
Figure 1

Configuration Table

Table 1

| Figure | C <sub>2</sub> | C <sub>1</sub> | C <sub>0</sub> | Configuration                             |
|--------|----------------|----------------|----------------|---|
| 2      | 0              | 0              | 0              | Product Term OE/Registered/Active LOW     |
| 3      | 0              | 0              | 1              | Product Term OE/Registered/Active HIGH    |
| 6      | 0              | 1              | 0              | Product Term OE/Combinatorial/Active LOW  |
| 7      | 0              | 1              | 1              | Product Term OE/Combinatorial/Active HIGH |
| 4      | 1              | 0              | 0              | Pin 13 OE/Registered/Active LOW           |
| 5      | 1              | 0              | 1              | Pin 13 OE/Registered/Active HIGH          |
| 8      | 1              | 1              | 0              | Pin 13 OE/Combinatorial/Active LOW        |
| 9      | 1              | 1              | 1              | Pin 13 OE/Combinatorial/Active HIGH       |

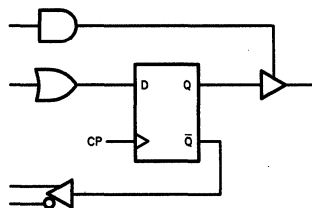
Registered Output Configurations



C<sub>2</sub> = 0  
C<sub>1</sub> = 0  
C<sub>0</sub> = 0

0053-37

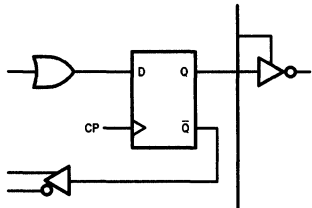
**Figure 2. Product Term OE/Active LOW**



C<sub>2</sub> = 0  
C<sub>1</sub> = 0  
C<sub>0</sub> = 1

0053-38

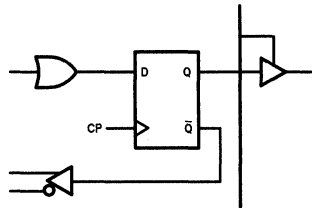
**Figure 3. Product Term OE/Active HIGH**



C<sub>2</sub> = 1  
C<sub>1</sub> = 0  
C<sub>0</sub> = 0

0053-39

**Figure 4. Pin 13 OE/Active LOW**

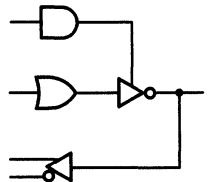


C<sub>2</sub> = 1  
C<sub>1</sub> = 0  
C<sub>0</sub> = 1

0053-40

**Figure 5. Pin 13 OE/Active HIGH**

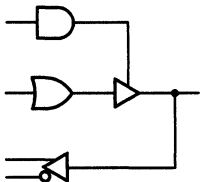
Combinatorial Output Configurations<sup>[6]</sup>



C<sub>2</sub> = 0  
C<sub>1</sub> = 1  
C<sub>0</sub> = 0

0053-33

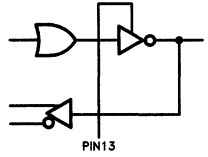
**Figure 6. Product Term OE/Active LOW**



C<sub>2</sub> = 0  
C<sub>1</sub> = 1  
C<sub>0</sub> = 1

0053-34

**Figure 7. Product Term OE/Active HIGH**

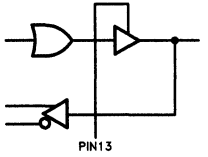


C<sub>2</sub> = 1  
C<sub>1</sub> = 1  
C<sub>0</sub> = 0

PIN13

0053-35

**Figure 8. Pin 13 OE/Active LOW**



C<sub>2</sub> = 1  
C<sub>1</sub> = 1  
C<sub>0</sub> = 1

PIN13

0053-36

**Figure 9. Pin 13 OE/Active HIGH**

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied ..... -55°C to +125°C  
 Supply Voltage to Ground Potential .... -0.5V to +7.0V  
 DC Voltage Applied to Outputs  
 in High Z State..... -0.5V to +7.0V  
 DC Input Voltage ..... -3.0V to +7.0V  
 Output Current into Outputs (Low) ..... 16 mA  
 DC Programming Voltage  
 PAL C 22V10B and CG7C323B-A ..... 13.0V  
 PAL C 22V10 and CG7C323-A ..... 14.0V

Static Discharge Voltage ..... > 2001V  
 (per MIL-STD-883 Method 3015)  
 Latchup Current ..... > 200 mA

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +75°C        | 5V ± 10%        |
| Military <sup>[8]</sup> | -55°C to +125°C     | 5V ± 10%        |
| Industrial              | -40°C to +85°C      | 5V ± 10%        |

### Electrical Characteristics Over Operating Range (Unless Otherwise Noted)<sup>[7]</sup>

| Parameters      | Description                  | Test Conditions  |                           | Min.      | Max. | Units |   |
|-----------------|------------------------------|--|---------------------------|-----------|------|-------|---|
|                 |                              |  |                           |           |      |       |   |
| V <sub>OH</sub> | Output HIGH Voltage          | V <sub>CC</sub> = Min.<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>           | I <sub>OH</sub> = -3.2 mA | COM'L/IND | 2.4  |       | V |
|                 |                              |  | I <sub>OH</sub> = -2 mA   | Military  |      |       |   |
| V <sub>OL</sub> | Output LOW Voltage           | V <sub>CC</sub> = Min.<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>           | I <sub>OL</sub> = 16 mA   | COM'L/IND |      | 0.5   | V |
|                 |                              |  | I <sub>OL</sub> = 12 mA   | Military  |      |       |   |
| V <sub>IH</sub> | Input HIGH Level             | Guaranteed Input Logical HIGH <sup>[1]</sup> Voltage for all Inputs                      |                           | 2.0       |      | V     |   |
| V <sub>IL</sub> | Input LOW Level              | Guaranteed Input Logical LOW <sup>[1]</sup> Voltage for all Inputs                       |                           |           | 0.8  | V     |   |
| I <sub>IX</sub> | Input Leakage Current        | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                                      |                           | -10       | 10   | μA    |   |
| I <sub>SC</sub> | Output Short Circuit Current | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V <sup>[2]</sup>                           |                           |           | -90  | mA    |   |
| I <sub>CC</sub> | Power Supply Current         | 0 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub><br>V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA | COM'L/IND -15, -20        |           | 70   | mA    |   |
|                 |                              |  | COM'L/IND -25, -35        |           | 55   |       |   |
|                 |                              |  | Military -20, -25         |           | 100  |       |   |
|                 |                              |  | Military -30, -40         |           | 80   |       |   |
| I <sub>OZ</sub> | Output Leakage Current       | V <sub>CC</sub> = Max., V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>             |                           | -100      | 100  | μA    |   |

Capacitance<sup>[3]</sup>


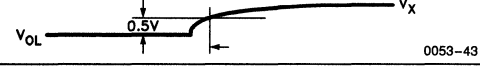
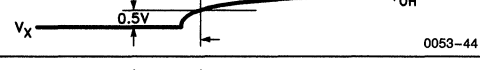
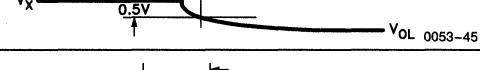
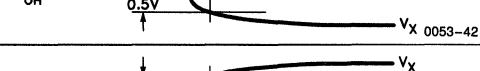
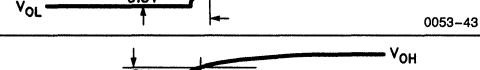
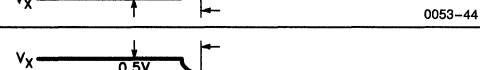
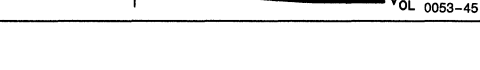
| Parameters       | Description        | Test Conditions                             | Max. | Units |
|------------------|--------------------|---|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz            | 4    | pF    |
| C <sub>OUT</sub> | Output Capacitance | V <sub>IN</sub> = 0, V <sub>CC</sub> = 5.0V | 7    |       |

Switching Characteristics PLD C 20G10 Over Operating Range<sup>[4, 7]</sup>

| Parameters        | Description   | Commercial |      |      |      |      |      |      |      | Military |      |      |      |      |      |      |      | Units |
|-------------------|---|------------|------|------|------|------|------|------|------|----------|------|------|------|------|------|------|------|-------|
|                   |   | B-15       |      | B-20 |      | -25  |      | -35  |      | B-20     |      | B-25 |      | -30  |      | -40  |      |       |
|                   |   | Min.       | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min.     | Max. | Min. | Max. | Min. | Max. | Min. | Max. |       |
| t <sub>PD</sub>   | Input to Output Propagation Delay <sup>[15]</sup>   |            | 15   |      | 20   |      | 25   |      | 35   |          | 20   |      | 25   |      | 30   |      | 40   | ns    |
| t <sub>EA</sub>   | Input to Output Enable Delay  |            | 15   |      | 20   |      | 25   |      | 35   |          | 20   |      | 25   |      | 30   |      | 40   | ns    |
| t <sub>ER</sub>   | Input to Output Disable Delay <sup>[10]</sup>   |            | 15   |      | 20   |      | 25   |      | 35   |          | 20   |      | 25   |      | 30   |      | 40   | ns    |
| t <sub>PZX</sub>  | OE Input to Output Enable Delay   |            | 12   |      | 15   |      | 20   |      | 25   |          | 17   |      | 20   |      | 25   |      | 25   | ns    |
| t <sub>PZX</sub>  | OE Input to Output Disable Delay  |            | 12   |      | 15   |      | 20   |      | 25   |          | 17   |      | 20   |      | 25   |      | 25   | ns    |
| t <sub>CO</sub>   | Clock to Output Delay <sup>[15]</sup>   |            | 10   |      | 12   |      | 15   |      | 25   |          | 15   |      | 15   |      | 20   |      | 25   | ns    |
| t <sub>S</sub>    | Input or Feedback Setup Time  | 12         |      | 12   |      | 15   |      | 30   |      | 15       |      | 18   |      | 20   |      | 35   |      | ns    |
| t <sub>H</sub>    | Input Hold Time   | 0          |      | 0    |      | 0    |      | 0    |      | 0        |      | 0    |      | 0    |      | 0    |      | ns    |
| t <sub>P</sub>    | External Clock Period (T <sub>CO</sub> + t <sub>S</sub> )                                   | 22         |      | 24   |      | 30   |      | 55   |      | 30       |      | 33   |      | 40   |      | 60   |      | ns    |
| t <sub>WH</sub>   | Clock Width HIGH <sup>[3,9]</sup>   | 8          |      | 10   |      | 12   |      | 17   |      | 12       |      | 14   |      | 16   |      | 22   |      | ns    |
| t <sub>WL</sub>   | Clock Width LOW <sup>[3,9]</sup>  | 8          |      | 10   |      | 12   |      | 17   |      | 12       |      | 14   |      | 16   |      | 22   |      | ns    |
| f <sub>MAX1</sub> | External Maximum Frequency (1/(t <sub>CO</sub> + t <sub>S</sub> )) <sup>[11]</sup>          | 45.4       |      | 41.6 |      | 33.3 |      | 18.1 |      | 33.3     |      | 30.3 |      | 25.0 |      | 16.6 |      | MHz   |
| f <sub>MAX2</sub> | Data Path Maximum Frequency (1/(t <sub>WH</sub> + t <sub>WL</sub> )) <sup>[12]</sup>        | 62.5       |      | 50.0 |      | 41.6 |      | 29.4 |      | 41.6     |      | 35.7 |      | 31.2 |      | 22.7 |      | MHz   |
| f <sub>MAX3</sub> | Internal Feedback Maximum Frequency (1/(t <sub>CF</sub> + t <sub>S</sub> )) <sup>[13]</sup> | 66.6       |      | 45.4 |      | 35.7 |      | 20.8 |      | 33.3     |      | 32.2 |      | 28.5 |      | 18.1 |      | MHz   |
| t <sub>CF</sub>   | Register Clock to Feedback Input <sup>[14]</sup>  |            | 3.0  |      | 10   |      | 13   |      | 18   |          | 13   |      | 13   |      | 15   |      | 20   | ns    |

Notes:

- These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V<sub>OUT</sub> = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.
- Figure 11a test load used for all parameters except t<sub>ER</sub>, t<sub>PZX</sub> and t<sub>PZX</sub>. Figure 11b test load used for t<sub>ER</sub>, t<sub>PZX</sub> and t<sub>PZX</sub>. See Figure 10 for waveforms.
- Preliminary specifications.
- Bidirectional I/O configurations are possible only when the combinatorial output option is selected.
- See the last page of this specification for Group A subgroup testing information.
- T<sub>A</sub> is the "instant on" case temperature.
- Tested by periodically sampling production product.
- This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous high level has fallen to 0.5 volts below V<sub>OH</sub> Min. or a previous low level has risen to 0.5 volts above V<sub>OL</sub> Max. Please see Figure 10 for enable and disable waveforms and measurement reference levels.
- This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feed back can operate.
- This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
- This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feed back can operate. This parameter is tested periodically by sampling production product.
- This parameter is calculated from the clock period at f<sub>MAX</sub> internal (f<sub>MAX3</sub>) as measured (see note 13 above) minus t<sub>S</sub>.
- This specification is guaranteed for all device outputs changing state in a given access cycle.

| Parameter    | $V_X$     | Output Waveform—Measurement Level  |
|--------------|-----------|--|
| $t_{PXZ}(-)$ | 1.5V      |  |
| $t_{PXZ}(+)$ | 2.6V      |  |
| $t_{PZX}(+)$ | $V_{thc}$ |  |
| $t_{PZX}(-)$ | $V_{thc}$ |  |
| $t_{ER}(-)$  | 1.5V      |  |
| $t_{ER}(+)$  | 2.6V      |  |
| $t_{EA}(+)$  | $V_{thc}$ |  |
| $t_{EA}(-)$  | $V_{thc}$ |  |

AC Test Loads and Waveforms (Commercial)

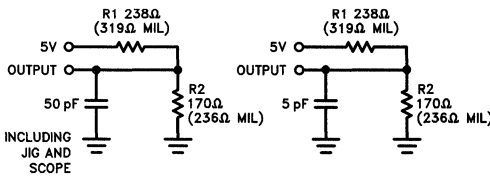


Figure 11a

Figure 11b

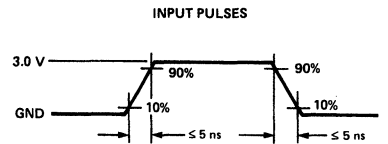
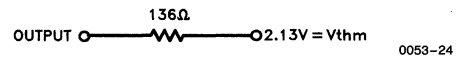
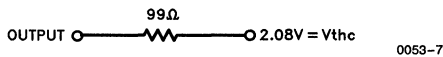


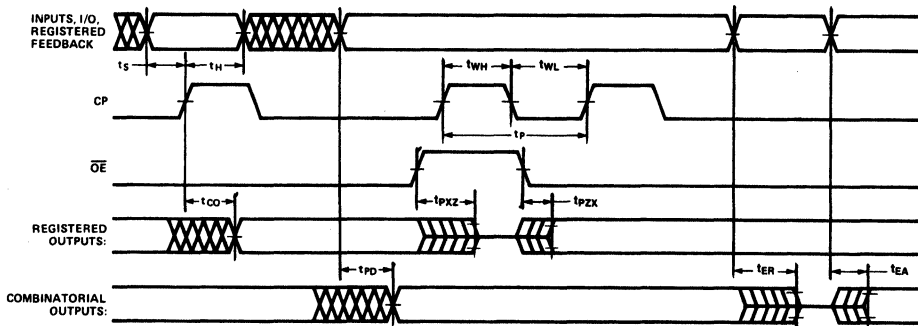
Figure 12

Equivalent to: THÉVENIN EQUIVALENT (Commercial)

Equivalent to: THÉVENIN EQUIVALENT (Military)

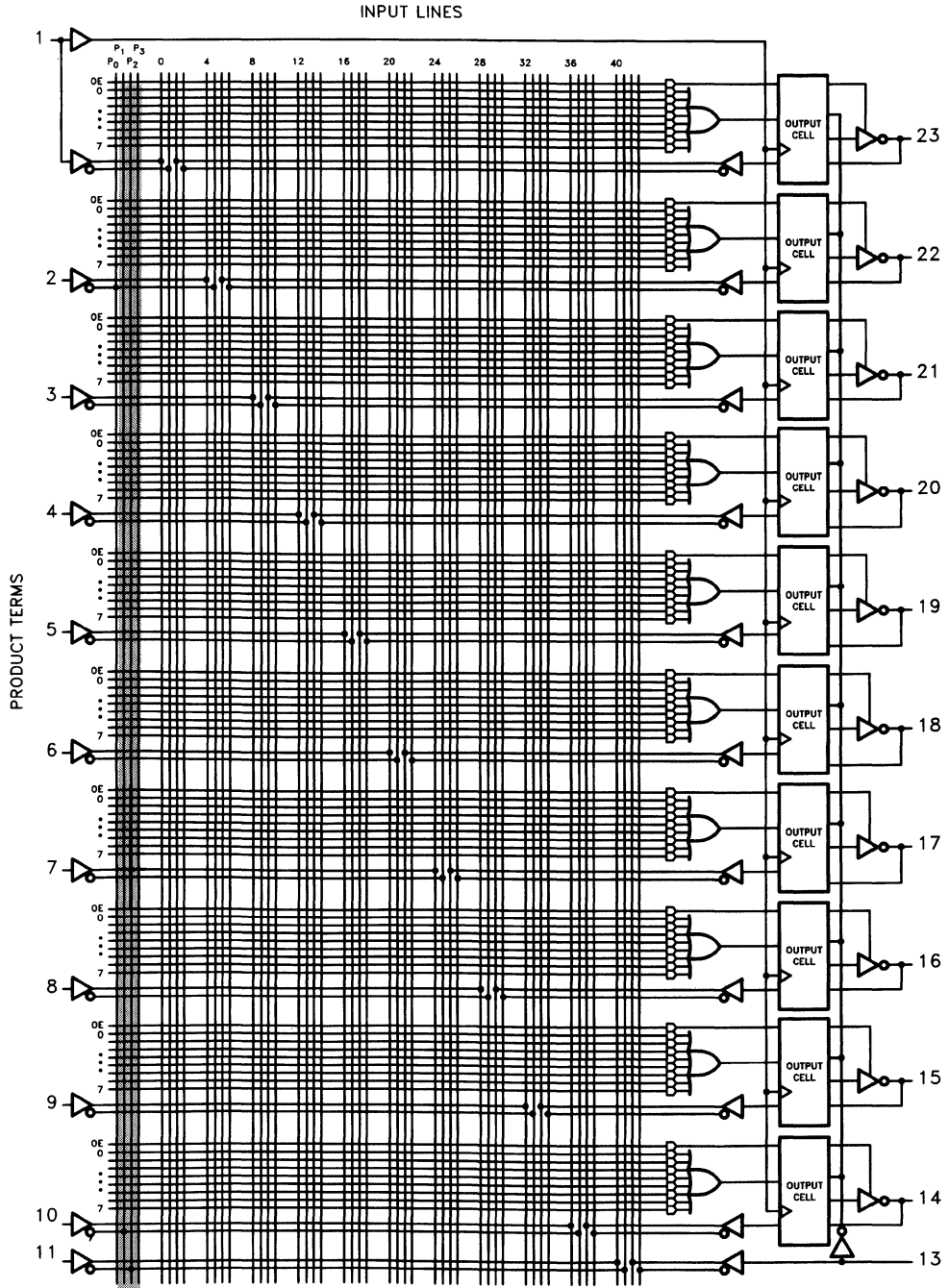


Switching Waveforms



Note:  
For more information regarding PLD devices, refer to the Application Brief in the Appendix.

Functional Logic Diagram PLD C 20G10



4

## Erase Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the PLD C 20G10. For this reason, an opaque label should be placed over the window if the device is exposed to sunlight or fluorescent lighting for extended periods of time. In addition, high ambient light levels can create hole-electron pairs which may cause "blank" check failures or "verify errors" when programming "windowed" parts. This phenomenon can be avoided by use of an opaque label over the window during programming in high ambient light environments.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity  $\times$  exposure time) of 25 Wsec/cm<sup>2</sup>. For an ultraviolet lamp with a 12 mW/cm<sup>2</sup> power rating, the exposure would be approximately 35 minutes. The PLD C 20G10 needs to be placed within 1 inch of the lamp during erasure. Permanent damage may result if the device is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm<sup>2</sup> is the recommended maximum dosage.

## Device Programming

The PLD C 20G10 can be programmed on inexpensive conventional PROM/EPROM programmers with appropriate personality or socket adapters and the CY3000 QuickPro programmer. Once the PLD device is programmed, one additional location can be programmed to prohibit logic pattern verification. This security feature gives the user additional protection to safeguard his proprietary logic. This feature is highly reliable and due to EPROM technology it is impossible to visually read the programmed cell locations.

The PLD C 20G10 has multiple programmable functions. In addition to the normal array, a "PHANTOM" array, "TOP and BOTTOM TEST" and a "SECURITY" feature are programmable. The PLD C 20G10 security mechanism, when invoked, prevents access to the "NORMAL" and "TOP/BOTTOM TEST" array. The "PHANTOM" array feature is still accessible, allowing programming and verification of the pattern in the "PHANTOM" array. Functional operation of all other features is allowed regardless of the state of the "SECURITY BIT". In addition, the device contains 10 programmable output cells which are programmed to configure the device functionality for each specific application.

The logic array is divided into a "NORMAL" array and a "PHANTOM" array. The normal array is used to configure the device to perform a specific function as required by the user, and the phantom array is provided as a test array for Cypress' testing the device prior to user programming thus assuring a reliable, thoroughly tested product. The "PHANTOM" array contains four additional columns connected to input pins 2 (TRUE), 7 (INVERTING), 10 (TRUE) and 11 (TRUE). These inputs may be programmed to be connected to all normal product terms. This allows all sense amplifiers and programmable output cells to be exercised for both functionality and performance after assembly and prior to shipment. These features are in addition to the normal array. They do not affect normal operation, allowing the user full programming of the normal array, while allowing the device to be fully tested.

The "TOP TEST" and "BOTTOM TEST" feature, allow connection of all input terms to either pin 23 or 13. These locations may be programmed and subsequently exercised in the "TOP TEST" and "BOTTOM TEST" mode. Like the Phantom array above, this feature has no effect in the normal mode of operation. Cells in the PHANTOM ARRAY, TOP TEST, and BOTTOM TEST areas are programmed at Cypress during the manufacturing operation, and they therefore will be programmed when received in a non-windowed package by the user. Consequently, the user will normally have no need to program these cells.

The architecture bits C<sub>0</sub>, C<sub>1</sub> and C<sub>2</sub> are used to configure each programmable output cell individually. C<sub>0</sub> selects output polarity, C<sub>1</sub> selects the combinatorial or registered mode of operation and C<sub>2</sub> selects the source of output enable. If the registered mode of operation is selected, the feedback path is automatically selected to be from the register. In the combinatorial mode the feedback path is automatically selected to be from the I/O pin. In this combinatorial mode, the output from the array may be fed into the array or if the output is deselected using the output enable product term the pin may be used as an external input. There is not a mode where the I/O pin may be used as a combinatorial output or an input pin, while the register is used as a state register. The architecture bits are programmed as a separate item during normal programming. An I/O pin is configured to be an input by programming the output cell into a combinatorial mode and disabling the output with the output enable product term.

## Pinout

The PLD C 20G10 PROGRAMMING pinout is shown in Figure 13. In the Programming pinout configuration, the device may be programmed and verified for the NORMAL mode of operation and also programmed, verified and operated in PHANTOM and TEST modes. These special modes of operation are achieved through the use of supervoltages applied to certain pins. Care should be exercised when entering and exiting these modes, paying specific attention to both the operating modes as specified in Table 1 and the sequencing of the supervoltages as shown in the timing diagrams.

## Programming Pinout

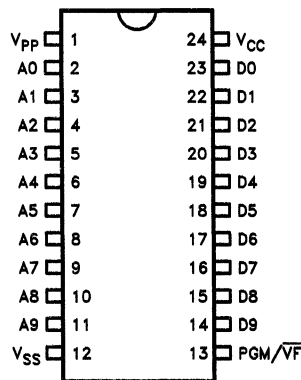


Figure 13

## Programming Algorithm

With the exception of the Security bit, all arrays are programmed in a similar manner. The data to be programmed is represented by a “1” or “0” on the I/O pins. A “1” indicates that an unprogrammed location is to be programmed and a “0” indicates that an unprogrammed location is to remain unprogrammed. All locations to be programmed are addressed as row and column locations. Table 2 “Operating Modes” along with Tables 3 through 6 provide the specific address for each addressed location to be programmed along with mode selection information for both programming and operation in the “PHANTOM” and “TEST” modes.

When programming the security bit, a supervoltage on pin 3 is used as data with a programming pulse on pin 13. Verification is controlled with a supervoltage on pins 4 and the data out on pin 3.

### 20G10 JEDEC Map

The 20G10 JEDEC Map is organized as follows: the EPROM fuses for the product terms and input lines are located between 0000 and 3959 (decimal). The architecture bits are located between locations 3960 and 3989. Location 3960 is the Polarity Bit (CO), location 3961 is the Registered/Combinatorial Bit (C1), and location 3962 is the Output Enable Bit (C2) for output pin 23. Locations 3963, 3964, and 3965 are the architecture bit locations for output pin 22. This pattern repeats for output pins 21, 20, 19, 18, 17, 16, 15, and 14.

### Operating Modes

Table 2 describes the operating and programming modes of the PLD C 20G10. The majority of the programming modes function with a PROGRAM, PROGRAM INHIBIT and PROGRAM VERIFY sequence. The exception is the Security Program operation, which shows no program inhibit function. Two timing diagrams are provided for these two different methodologies of programming in *Figures 15 & 16*. Tables 3 through 6 are used as indicated to provide the individual addresses of the various arrays and cells to be programmed. There are 5 operating modes in addition to the programming modes for the PAL C 22V10.

These provide NORMAL operation, PHANTOM operation, TOP TEST, BOTTOM TEST and a register preload feature for testing.

In the normal operating mode, all signals are TTL levels and the device functions as it is internally programmed in the NORMAL array. In the PHANTOM mode of operation, the device operates logically as a function of the contents of the PHANTOM array. In this mode pins 2, 10 & 11 are non-inverting inputs and pin 7 is an inverting input. The programmable output cells function as they are programmed for normal operation. If the programmable output cells have not yet been programmed, they are in a registered inverting configuration. The PHANTOM mode is invoked by placing a supervoltage  $V_{pp}$  on pin 6. Care should be exercised when entering and leaving this mode that the supervoltage is applied no sooner than 20 ms after the  $V_{CC}$  is stable, and removed a minimum of 20 ms before  $V_{CC}$  is removed.

### TOP and BOTTOM TEST

The TOP TEST and BOTTOM TEST modes are entered and exited in the same manner, with the same concern for power sequencing, but the supervoltage is applied to pins 9 & 10 respectively. In these modes an extra product term controls an output pin. TOP TEST controls pin 23, and BOTTOM TEST controls pin 14. These product terms are controlled by the normal device inputs, and allow testing of all input structures.

### Preload

Finally for testing of programmed functions, a preload feature allows any or all of the registers to be loaded with an initial value for testing. This is accomplished by raising pin 8 to a supervoltage  $V_{pp}$ , which puts the output drivers in a high impedance state. The data to be loaded is then placed on the I/O pins of the device and is loaded into the registers on the positive edge of the clock on pin 1. A “0” on the I/O pin preloads the register with a “0” and a “1” preloads the register with a “1”. The actual signal on the output pin will be the inversion of the input data. The data on the I/O pins is then removed, and pin 8 returned to a normal TTL voltage. Again care should be exercised to power sequence the device properly.



## Operating Modes

Table 2

| Operating Modes                     |                               | Pin 1            | Pin 2            | Pin 3            | Pin 4            | Pin 5            | Pin 6            | Pin 7            | Pin 8            | Pin 9            | Pin 10           | Pin 11           | Pin 13           | Pin 14           | Pin 17           | Pin 20           | Pins 15, 16, 18, 19, 21 & 22 | Pin 23           |          |
|-------------------------------------|-------------------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------------------|------------------|----------|
| Feature                             | Function                      |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                              |                  |          |
| Main Array Product                  | Program                       | V <sub>PP</sub>  | Table 3          |                  |                  |                  |                  |                  |                  | Table 4          |                  |                  |                  | V <sub>PP</sub>  | Data In          |                  |                              |                  |          |
|                                     | Program Inhibit               | V <sub>PP</sub>  | Table 3          |                  |                  |                  |                  |                  |                  | Table 4          |                  |                  |                  | V <sub>IHP</sub> | High Z           |                  |                              |                  |          |
|                                     | Program Verify <sup>[3]</sup> | V <sub>PP</sub>  | Table 3          |                  |                  |                  |                  |                  |                  | Table 4          |                  |                  |                  | V <sub>ILP</sub> | Data Out         |                  |                              |                  |          |
| Output Enable Product Terms         | Program                       | V <sub>PP</sub>  | Table 3          |                  |                  |                  |                  |                  |                  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>  | V <sub>PP</sub>  | Data In          |                  |                              |                  |          |
|                                     | Program Inhibit               | V <sub>PP</sub>  | Table 3          |                  |                  |                  |                  |                  |                  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>  | V <sub>IHP</sub> | High Z           |                  |                              |                  |          |
|                                     | Program Verify                | V <sub>PP</sub>  | Table 3          |                  |                  |                  |                  |                  |                  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>  | V <sub>ILP</sub> | Data Out         |                  |                              |                  |          |
| Top Test, Bottom Test Notes         | Program                       | V <sub>PP</sub>  | Table 3          |                  |                  |                  |                  |                  |                  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>  | Data In          | Data In          | Data In                      | V <sub>ILP</sub> | Data In  |
|                                     | Program Inhibit               | V <sub>PP</sub>  | Table 3          |                  |                  |                  |                  |                  |                  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | High Z           | High Z           | High Z                       | High Z           | High Z   |
|                                     | Program Verify                | V <sub>PP</sub>  | Table 3          |                  |                  |                  |                  |                  |                  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>ILP</sub> | Data Out         | Data Out         | Data Out                     | Driven           | Data Out |
| Architecture Bits                   | Program                       | V <sub>PP</sub>  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>ILP</sub> | Table 5          |                  |                  | V <sub>PP</sub>  | V <sub>PP</sub>  | Data In          |                  |                              |                  |          |
|                                     | Program Inhibit               | V <sub>PP</sub>  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>ILP</sub> | Table 5          |                  |                  | V <sub>PP</sub>  | V <sub>IHP</sub> | High Z           |                  |                              |                  |          |
|                                     | Program Verify                | V <sub>PP</sub>  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>ILP</sub> | Table 5          |                  |                  | V <sub>PP</sub>  | V <sub>ILP</sub> | Data Out         |                  |                              |                  |          |
| Security Bit                        | Program                       | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub>             | V <sub>ILP</sub> |          |
|                                     | Verify                        | V <sub>ILP</sub> | V <sub>ILP</sub> | Data Out         | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | Driven Outputs   |                  |                  |                              |                  |          |
| PAL Mode Operation                  | Normal                        | CP/I             | I                | I                | I                | I                | I                | I                | I                | I                | I                | I                | I                | I/O              |                  |                  |                              |                  |          |
|                                     | Phantom                       | CP/I             | I                | NA               | NA               | NA               | V <sub>PP</sub>  | I                | NA               | NA               | I                | I                | NA               | Output           |                  |                  |                              |                  |          |
|                                     | Top Test                      | I                | I                | I                | I                | I                | I                | I                | I                | V <sub>PP</sub>  | I                | I                | I                | NA               |                  |                  |                              | Out              |          |
|                                     | Bottom Test                   | I                | I                | I                | I                | I                | I                | I                | I                | I                | V <sub>PP</sub>  | I                | I                | Out              | NA               |                  |                              |                  |          |
|                                     | Reg Preload                   | Notes            | NA               | NA               | NA               | NA               | NA               | NA               | V <sub>PP</sub>  | NA               | NA               | NA               | V <sub>ILP</sub> | Data In          |                  |                  |                              |                  |          |
| Phantom Array Product Terms         | Program                       | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub> | Table 6          |                  |                  | V <sub>ILP</sub> | V <sub>PP</sub>  | Table 4          |                  |                  |                  | V <sub>PP</sub>  | Data In          |                  |                              |                  |          |
|                                     | Program Inhibit               | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub> | Table 6          |                  |                  | V <sub>ILP</sub> | V <sub>PP</sub>  | Table 4          |                  |                  |                  | V <sub>IHP</sub> | High Z           |                  |                              |                  |          |
|                                     | Program Verify                | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub> | Table 6          |                  |                  | V <sub>ILP</sub> | V <sub>PP</sub>  | Table 4          |                  |                  |                  | V <sub>ILP</sub> | Data Out         |                  |                              |                  |          |
| Phantom Output Enable Product Terms | Program                       | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub> | Table 6          |                  |                  | V <sub>ILP</sub> | V <sub>PP</sub>  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>  | V <sub>PP</sub>  | Data In          |                  |                              |                  |          |
|                                     | Program Inhibit               | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub> | Table 6          |                  |                  | V <sub>ILP</sub> | V <sub>PP</sub>  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>  | V <sub>IHP</sub> | High Z           |                  |                              |                  |          |
|                                     | Program Verify                | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub> | Table 6          |                  |                  | V <sub>ILP</sub> | V <sub>PP</sub>  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>  | V <sub>ILP</sub> | Data Out         |                  |                              |                  |          |

Notes:

1. DATA IN and DATA OUT for programming Synchronous Set, Asynchronous Reset, TOP TEST and BOTTOM TEST is programmed and verified on the following pins.  
Pin 14 = BOTTOM TEST  
Pin 17 = Synchronous Set  
Pin 20 = Asynchronous Reset  
Pin 23 = TOP TEST
2. The preload clock on pin 1 loads the Registers on a LOW going HIGH transition.
3. It is necessary to toggle OE (Pin 13) HIGH during all address transitions while in the program verify/blank check mode.

### Input Term Addresses

Table 3 is used during the programming and verification of the main array, output enable, asynchronous reset, synchronous preset, TOP and BOTTOM TEST as shown in Table 2.

It provides the addressing for the 44 normal input term columns which are connected with an EPROM transistor to the product terms.

### Input Term Addresses

Table 3

| Input Term | Pin 2 | Pin 3 | Pin 4 | Pin 5 | Pin 6 | Pin 7 |
|------------|-------|-------|-------|-------|-------|-------|
| 0          | VILP  | VILP  | VILP  | VILP  | VILP  | VILP  |
| 1          | VIHP  | VILP  | VILP  | VILP  | VILP  | VILP  |
| 2          | VILP  | VIHP  | VILP  | VILP  | VILP  | VILP  |
| 3          | VIHP  | VIHP  | VILP  | VILP  | VILP  | VILP  |
| 4          | VILP  | VILP  | VIHP  | VILP  | VILP  | VILP  |
| 5          | VIHP  | VILP  | VIHP  | VILP  | VILP  | VILP  |
| 6          | VILP  | VIHP  | VIHP  | VILP  | VILP  | VILP  |
| 7          | VIHP  | VIHP  | VIHP  | VILP  | VILP  | VILP  |
| 8          | VILP  | VILP  | VILP  | VIHP  | VILP  | VILP  |
| 9          | VIHP  | VILP  | VILP  | VIHP  | VILP  | VILP  |
| 10         | VILP  | VIHP  | VILP  | VIHP  | VILP  | VILP  |
| 11         | VIHP  | VIHP  | VILP  | VIHP  | VILP  | VILP  |
| 12         | VILP  | VILP  | VIHP  | VIHP  | VILP  | VILP  |
| 13         | VIHP  | VILP  | VIHP  | VIHP  | VILP  | VILP  |
| 14         | VILP  | VIHP  | VIHP  | VIHP  | VILP  | VILP  |
| 15         | VIHP  | VIHP  | VIHP  | VIHP  | VILP  | VILP  |
| 16         | VILP  | VILP  | VILP  | VILP  | VIHP  | VILP  |
| 17         | VIHP  | VILP  | VILP  | VILP  | VIHP  | VILP  |
| 18         | VILP  | VIHP  | VILP  | VILP  | VIHP  | VILP  |
| 19         | VIHP  | VIHP  | VILP  | VILP  | VIHP  | VILP  |
| 20         | VILP  | VILP  | VIHP  | VILP  | VIHP  | VILP  |
| 21         | VIHP  | VILP  | VIHP  | VILP  | VIHP  | VILP  |
| 22         | VILP  | VIHP  | VIHP  | VILP  | VIHP  | VILP  |
| 23         | VIHP  | VIHP  | VIHP  | VILP  | VIHP  | VILP  |
| 24         | VILP  | VILP  | VILP  | VIHP  | VIHP  | VILP  |
| 25         | VIHP  | VILP  | VILP  | VIHP  | VIHP  | VILP  |
| 26         | VILP  | VIHP  | VILP  | VIHP  | VIHP  | VILP  |
| 27         | VIHP  | VIHP  | VILP  | VIHP  | VIHP  | VILP  |
| 28         | VILP  | VILP  | VIHP  | VIHP  | VIHP  | VILP  |
| 29         | VIHP  | VILP  | VIHP  | VIHP  | VIHP  | VILP  |
| 30         | VILP  | VIHP  | VIHP  | VIHP  | VIHP  | VILP  |
| 31         | VIHP  | VIHP  | VIHP  | VIHP  | VIHP  | VILP  |
| 32         | VILP  | VILP  | VILP  | VILP  | VILP  | VIHP  |
| 33         | VIHP  | VILP  | VILP  | VILP  | VILP  | VIHP  |
| 34         | VILP  | VIHP  | VILP  | VILP  | VILP  | VIHP  |
| 35         | VIHP  | VIHP  | VILP  | VILP  | VILP  | VIHP  |
| 36         | VILP  | VILP  | VIHP  | VILP  | VILP  | VIHP  |
| 37         | VIHP  | VILP  | VIHP  | VILP  | VILP  | VIHP  |
| 38         | VILP  | VIHP  | VIHP  | VILP  | VILP  | VIHP  |
| 39         | VIHP  | VIHP  | VIHP  | VILP  | VILP  | VIHP  |
| 40         | VILP  | VILP  | VILP  | VIHP  | VILP  | VIHP  |
| 41         | VIHP  | VILP  | VILP  | VIHP  | VILP  | VIHP  |
| 42         | VILP  | VIHP  | VILP  | VIHP  | VILP  | VIHP  |
| 43         | VIHP  | VIHP  | VILP  | VIHP  | VILP  | VIHP  |

## Product Term Addresses

Table 4 is used for the programming of the "PHANTOM" and normal array. It provides the addressing for the 8 product terms associated with each input.

**Product Term Addresses**  
 Table 4

| Product Term | Pin 8 | Pin 9 | Pin 10 | Pin 11 |
|--------------|-------|-------|--------|--------|
| 0            | VILP  | VILP  | VILP   | VILP   |
| 1            | VIHP  | VILP  | VILP   | VILP   |
| 2            | VILP  | VIHP  | VILP   | VILP   |
| 3            | VIHP  | VIHP  | VILP   | VILP   |
| 4            | VILP  | VILP  | VIHP   | VILP   |
| 5            | VIHP  | VILP  | VIHP   | VILP   |
| 6            | VILP  | VIHP  | VIHP   | VILP   |
| 7            | VIHP  | VIHP  | VIHP   | VILP   |

## Architecture Bit Addressing

Table 5 provides the addressing for the architecture bits used to control the configuration of the individual Programmable Output Cells. In the unprogrammed state, the Programmable Output Cells are in a registered, active low or inverting configuration with output enable controlled from the product term. They are programmed with a "1" on the pin associated with the Programmable Output Cells and the appropriate address as shown in Table 5. Each architecture bit that is not to be programmed, requires a "0" on the I/O pin associated with the Programmable Output Cells.

**Architecture Bit Addressing**  
 Table 5

| Architecture Bit                      | Pin 9 | Pin 10 |
|---------------------------------------|-------|--------|
| Output Polarity C0                    | VILP  | VILP   |
| Register/Combinatorial Output C1      | VIHP  | VILP   |
| Product Term/ Pin 13 Output Enable C2 | VILP  | VIHP   |

## Phantom Input Term Addressing

Phantom input terms are addressed as columns P0 thru P3 and represent inputs from pins 2, 7, 10 and 11 respectively.

Pin 7 is inverted, and the remaining 3 are normal non-inverting. This PHANTOM array allows the output structures to be tested. They are only present in PHANTOM modes of operation.

**Phantom Input Term Addresses**  
 Table 6

| Phantom Input Term | Pin 4 | Pin 5 |
|--------------------|-------|-------|
| P0                 | VILP  | VILP  |
| P1                 | VIHP  | VILP  |
| P2                 | VILP  | VIHP  |
| P3                 | VIHP  | VIHP  |

## Programming Flow Chart

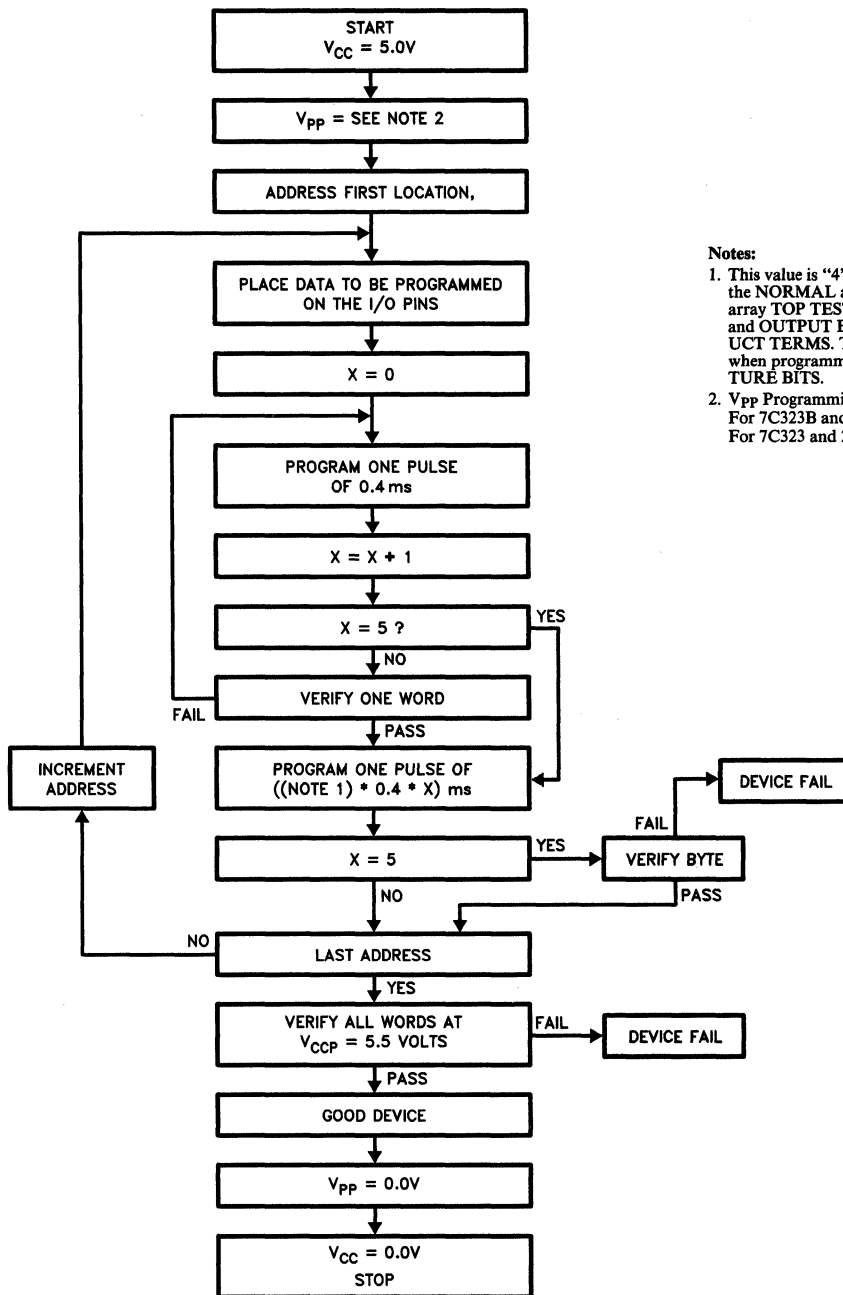
The programming flow chart describes the sequence of operations for programming the NORMAL and PHANTOM arrays, the NORMAL and PHANTOM output enable product terms, the set and preset product terms, the Top Test product term, the Bottom Test product term, and the architecture bits. The exact sequencing and timing of the signals is shown in the "Array Programming Timing Diagram".

The logical sequence to program the device is described in detail in the flow chart below, and should be followed exactly for optimum intelligent programming that both minimizes programming time and realizes reliable programming. Particular attention should be paid to the application of  $V_{CC}$  prior to  $V_{pp}$ , and removal of  $V_{pp}$  prior to  $V_{CC}$ . See *Figure 14* and Table 8 for specific timing and AC requirements. Notice that all programming is accomplished without switching  $V_{pp}$  on pin 1 and that after programming and verifying all locations individually, the programmed locations should be verified one final time.

The normal word programming cycle, programs and verifies a word at a time as shown in the programming flowchart, *Figure 13* and timing diagram *Figure 14*. After all locations are programmed, the flowchart requires a verify of all words. There is no independent timing diagram for this operation, rather *Figure 14* also provides the correct timing information for this operation. When performing this verify only operation, eliminate the program portion of the cycle but maintain the setup and hold timing relative to the verify pulse. Under no circumstances should the verify signal be held low and the addresses toggled.

Note that the overprogram pulse in step 10 of the programming flowchart is a variable, "4" times the initial value when programming the NORMAL, PHANTOM, TOP TEST, BOTTOM TEST and OUTPUT ENABLE product terms and "8" times the initial value when programming the ARCHITECTURE BITS.

Programming Flowchart



- Notes:
1. This value is "4" for programming the NORMAL array, PHANTOM array TOP TEST, BOTTOM TEST and OUTPUT ENABLE PRODUCT TERMS. The value is "8" when programming ARCHITECTURE BITS.
  2. V<sub>pp</sub> Programming Voltage:  
For 7C323B and 20G10B = 12.5V  
For 7C323 and 20G10 = 13.5V.

Figure 14

## Timing Diagrams

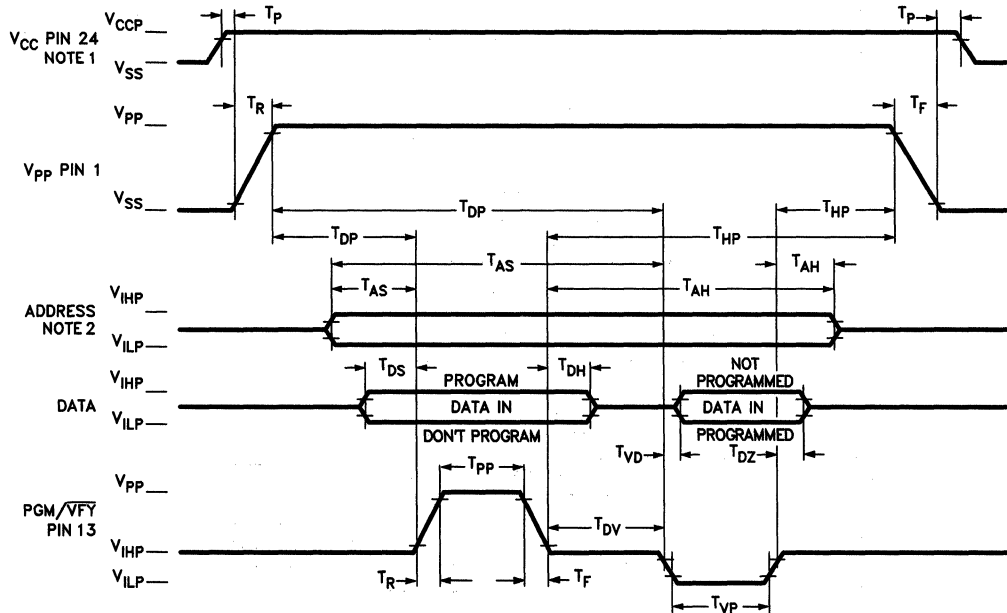
Programming timing diagrams are provided for two cases, programming of all cells except the SECURITY BIT and programming the SECURITY BIT.

### Array

Programming the NORMAL and PHANTOM arrays and output enables, reset, preset, architecture bits and the top/bottom test features uses the timing diagram in *Figure 15*. ADDRESS refers to all applicable information in Tables 2 through 6 that is not specifically referenced in the timing diagram. DATA IN is provided on the I/O pins and

DATA OUT is verified on the same pins. A "1" ( $V_{IHP}$ ) on an I/O pin causes the addressed location to be programmed. A "0" on the I/O pin leaves the addressed location to be unprogrammed. All setup hold and delay times must be met, and in particular the sequence of operations should be strictly followed. During verify only operation it is not acceptable to hold PGM/VFY low and sequence addresses, as it violates address setup and hold times. Proper sequencing of all power and supervoltages is essential, to reliable programming of the device as improper sequencing could result in device damage.

### Programming Waveforms



#### Notes:

1. Power,  $V_{PP}$  &  $V_{CC}$  should not be cycled for each program/verify cycle, but may remain static during programming.

2. For programming OE Product Terms & Architecture bits, Pin 11 (A9) must go to  $V_{PP}$  and satisfy  $T_{AS}$  and  $T_{AH}$ .

Figure 15

0053-29

## Security Cell

The security cell is programmed independently per the timing diagram in *Figure 16*, and the information in Table 2. Note again that proper sequencing of power and programming signals is required. Data in is represented as a supervoltage on pin 3 and verified as a TTL signal output on the

same pin. A “0” on pin 3 indicates that the security bit has been programmed, and a “1” indicates that security bit has not been programmed. Security is programmed with a single 50 ms pulse on pin 13. A supervoltage on pin 4 is used to verify security after  $V_{pp}$  has been removed from pin 1.

## Programming Waveforms Security Cell

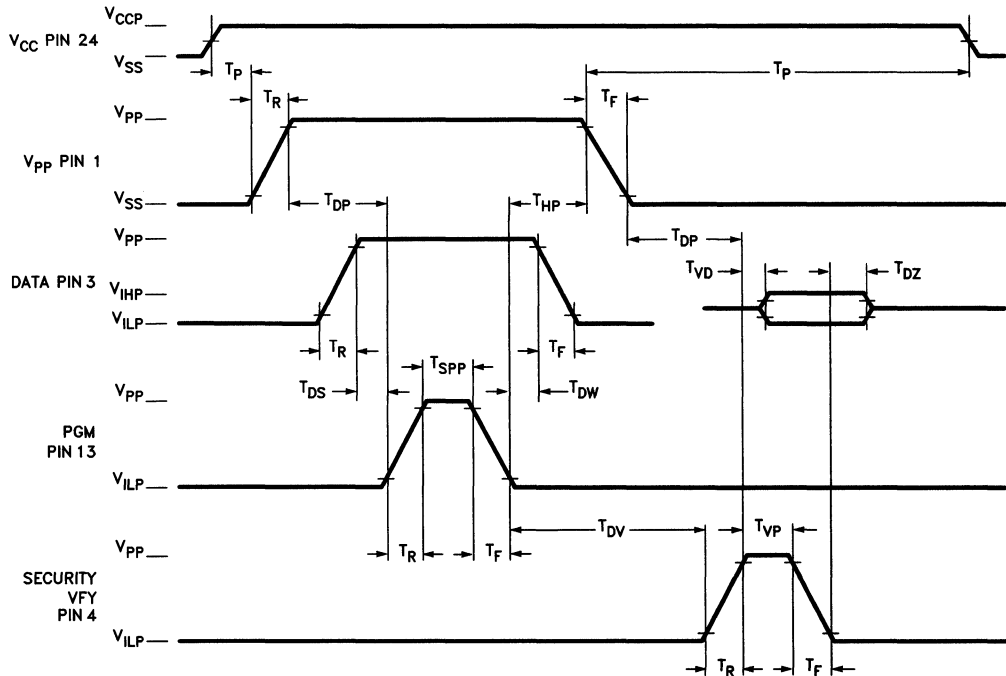


Figure 16

0053-30

**DC Programming Parameters**  $T_A = 25^\circ\text{C}$ 
**Table 7**

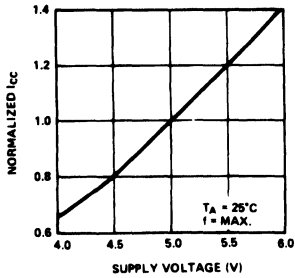
| Parameter                                    | Description                           | Min. | Max.      | Units |
|--|---------------------------------------|------|-----------|-------|
| $V_{PP}$ for PLD C 20G10B and for CG7C323B-A | Programming Voltage                   | 12.0 | 13.0      | Volts |
| $V_{PP}$ for PLD C 20G10 and for CG7C323-A   | Programming Voltage                   | 13.0 | 14.0      | Volts |
| $V_{CCP}$                                    | Supply Voltage During Programming     | 4.75 | 5.25      | Volts |
| $V_{IHP}$                                    | Input HIGH Voltage During Programming | 3.0  | $V_{CCP}$ | Volts |
| $V_{ILP}$                                    | Input LOW Voltage During Programming  | -3.0 | 0.4       | Volts |
| $V_{OH}$                                     | Output HIGH Voltage                   | 2.4  |           | Volts |
| $V_{OL}$                                     | Output LOW Voltage                    |      | 0.4       | Volts |
| $I_{PP}$                                     | Programming Supply Current            |      | 40        | mA    |

**AC Programming Parameters**
**Table 8**

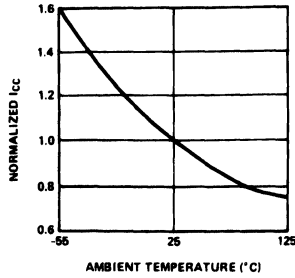
| Parameter | Description                         | Min. | Max. | Units         |
|-----------|-------------------------------------|------|------|---------------|
| $T_P$     | Delay to Programming Voltage        | 20   |      | ms            |
| $T_{DP}$  | Delay to Program                    | 1    |      | $\mu\text{s}$ |
| $T_{HP}$  | Hold from Program or Verify         | 1    |      | $\mu\text{s}$ |
| $T_{R,F}$ | $V_{pp}$ Rise & Fall Time           | 50   |      | ns            |
| $T_{AS}$  | Address Setup Time                  | 1    |      | $\mu\text{s}$ |
| $T_{AH}$  | Address Hold Time                   | 1    |      | $\mu\text{s}$ |
| $T_{DS}$  | Data Setup Time                     | 1    |      | $\mu\text{s}$ |
| $T_{DH}$  | Data Hold Time                      | 1    |      | $\mu\text{s}$ |
| $T_{PP}$  | Programming Pulsewidth              | 0.4  | 10   | ms            |
| $T_{SPP}$ | Programming Pulsewidth for Security | 50   |      | ms            |
| $T_{DV}$  | Delay from Program to Verify        | 2    |      | $\mu\text{s}$ |
| $T_{VD}$  | Delay to Data Out                   |      | 1    | $\mu\text{s}$ |
| $T_{VP}$  | Verify Pulse Width                  | 2    |      | $\mu\text{s}$ |
| $T_{DZ}$  | Verify to High Z                    |      | 1    | $\mu\text{s}$ |

Typical DC and AC Characteristics

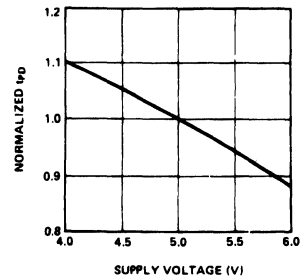
**NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE**



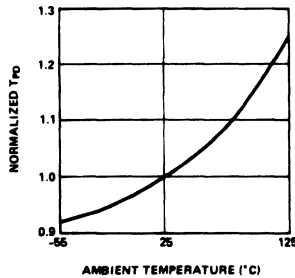
**NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE**



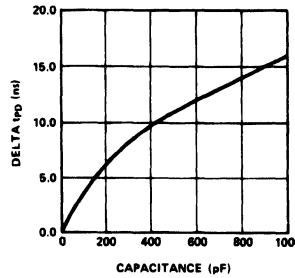
**NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE**



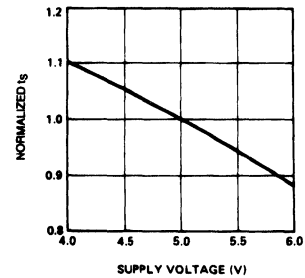
**NORMALIZED PROPAGATION DELAY vs. TEMPERATURE**



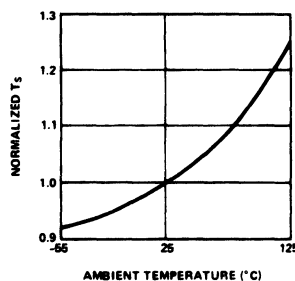
**DELTA PROPAGATION TIME vs. OUTPUT LOADING**



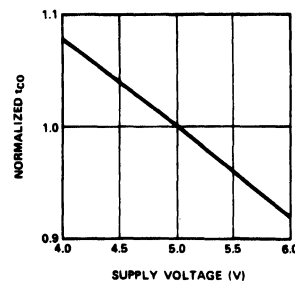
**NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE**



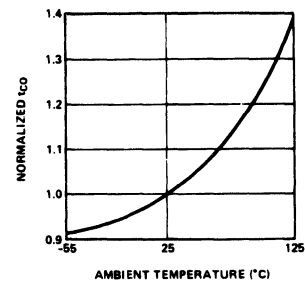
**NORMALIZED SETUP TIME vs. TEMPERATURE**



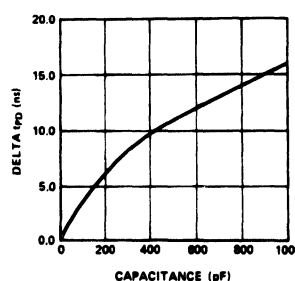
**NORMALIZED CLOCK TO OUTPUT TIME vs. SUPPLY VOLTAGE**



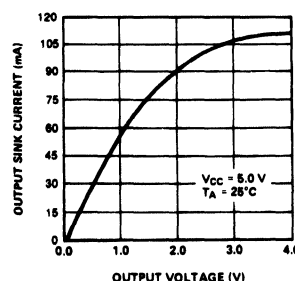
**NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE**



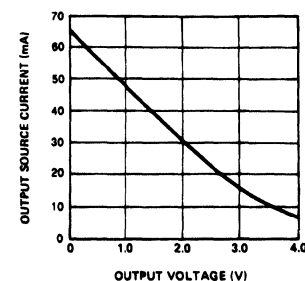
**DELTA CLOCK TO OUTPUT TIME vs. OUTPUT LOADING**



**OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE**



**OUTPUT SOURCE CURRENT vs. VOLTAGE**





**Ordering Information**

| t <sub>PD</sub><br>(ns) | t <sub>S</sub><br>(ns) | t <sub>CO</sub><br>(ns) | I <sub>CC</sub><br>(mA) | Ordering Code                     | Package | Operating Range           |
|-------------------------|------------------------|-------------------------|-------------------------|-----------------------------------|---------|---------------------------|
| 15                      | 12                     | 10                      | 70                      | PLD C 20G10B-15PC/PI              | P13     | Commercial/<br>Industrial |
|                         |                        |                         |                         | PLD C 20G10B-15WC/WI              | W14     |                           |
|                         |                        |                         |                         | PLD C 20G10B-15JC/JI*             | J64     |                           |
|                         |                        |                         |                         | CG7C323B-A15JC/JI <sup>[16]</sup> | J64     |                           |
| 20                      | 12                     | 12                      | 70                      | PLD C 20G10B-20PC/PI              | P13     | Commercial/<br>Industrial |
|                         |                        |                         |                         | PLD C 20G10B-20WC/WI              | W14     |                           |
|                         |                        |                         |                         | PLD C 20G10B-20JC/JI              | J64     |                           |
|                         |                        |                         |                         | CG7C323B-A20JC/JI <sup>[16]</sup> | J64     |                           |
| 20                      | 15                     | 15                      | 100                     | PLD C 20G10B-20DMB                | D14     | Military                  |
|                         |                        |                         |                         | PLD C 20G10B-20WMB                | W14     |                           |
|                         |                        |                         |                         | PLD C 20G10B-20LMB                | L64     |                           |
| 25                      | 15                     | 15                      | 55                      | PLD C 20G10-25PC/PI               | P13     | Commercial/<br>Industrial |
|                         |                        |                         |                         | PLD C 20G10-25WC/WI               | W14     |                           |
|                         |                        |                         |                         | PLD C 20G10-25JC/JI               | J64     |                           |
|                         |                        |                         |                         | CG7C323-A25JC/JI <sup>[16]</sup>  | J64     |                           |
| 25                      | 18                     | 15                      | 100                     | PLD C 20G10B-25DMB                | D14     | Military                  |
|                         |                        |                         |                         | PLD C 20G10B-25WMB                | W14     |                           |
|                         |                        |                         |                         | PLD C 20G10B-25LMB                | L64     |                           |
| 30                      | 20                     | 20                      | 80                      | PLD C 20G10-30DMB                 | D14     | Military                  |
|                         |                        |                         |                         | PLD C 20G10-30WMB                 | W14     |                           |
|                         |                        |                         |                         | PLD C 20G10-30LMB                 | L64     |                           |
| 35                      | 30                     | 25                      | 55                      | PLD C 20G10-35PC/PI               | P13     | Commercial/<br>Industrial |
|                         |                        |                         |                         | PLD C 20G10-35WC/WI               | W14     |                           |
|                         |                        |                         |                         | PLD C 20G10-35JC/JI               | J64     |                           |
|                         |                        |                         |                         | CG7C323-A35JC/JI <sup>[16]</sup>  | J64     |                           |
| 40                      | 35                     | 25                      | 80                      | PLD C 20G10-40DMB                 | D14     | Military                  |
|                         |                        |                         |                         | PLD C 20G10-40WMB                 | W14     |                           |
|                         |                        |                         |                         | PLD C 20G10-40LMB                 | L64     |                           |

**Note:**

16. The CG7C323 is the PLDC20G10 packaged in the JEDEC compatible 28 pin PLCC pinout. Pin function and pin order is identical for both PLCC pinouts. The principle difference is in the location of the "no connect" or NC pins.

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters      | Subgroups |
|-----------------|-----------|
| V <sub>OH</sub> | 1,2,3     |
| V <sub>OL</sub> | 1,2,3     |
| V <sub>IH</sub> | 1,2,3     |
| V <sub>IL</sub> | 1,2,3     |
| I <sub>IX</sub> | 1,2,3     |
| V <sub>PP</sub> | 1,2,3     |
| I <sub>CC</sub> | 1,2,3     |
| I <sub>OZ</sub> | 1,2,3     |

4

#### Switching Characteristics

| Parameters       | Subgroups   |
|------------------|-------------|
| t <sub>PD</sub>  | 7,8,9,10,11 |
| t <sub>PZX</sub> | 7,8,9,10,11 |
| t <sub>CO</sub>  | 7,8,9,10,11 |
| t <sub>S</sub>   | 7,8,9,10,11 |
| t <sub>H</sub>   | 7,8,9,10,11 |

Document #: 38-00019-C



# Reprogrammable Asynchronous CMOS Logic Device

## Features

- Advanced user programmable macro cell
- CMOS EPROM technology for reprogrammability
- Up to 20 input terms
- 10 programmable I/O macro cells
- Output macro cell programmable as combinatorial or asynchronous D-type registered output
- Product term control of register clock, reset and set and output enable
- Register preload and power-up reset
- Four uncommitted product terms per output macro cell

- **Fast**
  - Commercial
    - tpD = 20 ns
    - tCO = 20 ns
    - tSU = 10 ns
  - Military
    - tpD = 25 ns
    - tCO = 25 ns
    - tSU = 15 ns
- **Low power**
  - ICC max = 80 mA  
Commercial
  - ICC max = 100 mA  
Military
- **High reliability**
  - Proven EPROM technology
  - > 2001V input protection
  - 100% programming and functional testing
- **Windowed DIP, windowed LCC, DIP, LCC, PLCC available**

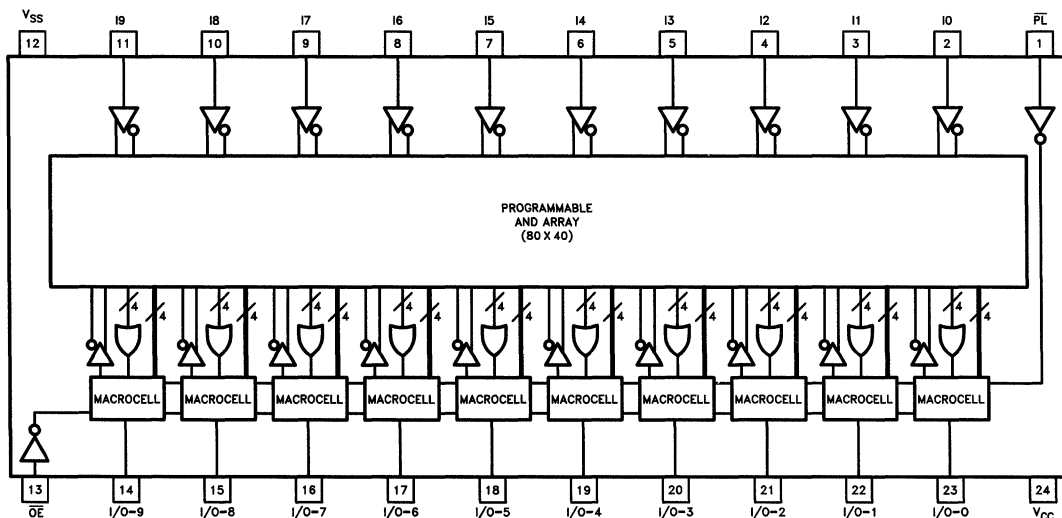
## Functional Description

The Cypress PLD C 20RA10 is a high performance, second generation programmable logic device employing a flexible macro cell structure which allows any individual output to be configured independently as a combinatorial output or as a fully asynchronous D-type registered output.

The Cypress PLD C 20RA10 provides lower power operation with superior speed performance than functionally equivalent bipolar devices through the use of high performance 0.8 micron CMOS manufacturing technology.

The PLD C 20RA10 is packaged in a 24 pin 300 mil molded DIP, a 300 mil windowed cerdip, and a 28 lead square leadless chip carrier and provides up to 20 inputs and 10 outputs. When the windowed device is exposed UV light, the 20RA10 is erased and then can be reprogrammed.

## Block Diagram and DIP Pinout



0118-1

## Macro Cell Architecture

Figure 1 illustrates the architecture of the 20RA10 macro cell. The cell dedicates three product terms for fully asynchronous control of the register set, reset and clock functions, as well as, one term for control of the output enable function.

The output enable product term output is “AND’ed” with the input from pin 13 to allow either product term or hard wired external control of the output or a combination of control from both sources. If product term only control is selected, it is automatically chosen for all outputs since, for this case, the external output enable pin must be tied LOW. The active polarity of each output may be programmed independently for each output cell and is subsequently fixed. Figure 2 illustrates the output enable options available.

When an I/O cell is configured as an output, combinatorial only capability may be selected by forcing the set and reset product term outputs to be HIGH under all input conditions. This is achieved by programming all input term programming cells for these two product terms. Figure 3 illustrates the available output configuration options.

An additional four uncommitted product terms are provided in each output macro cell as resources for creation of user defined logic functions.

### Programmable I/O

Because any of the 10 I/O pins may be selected as an input, the device input configuration programmed by the user may vary from a total of nine programmable plus ten dedicated inputs (a total of nineteen inputs) and one output down to a ten input, ten output configuration with all ten programmable I/O cells configured as outputs. Each input pin available in a given configuration is available as an input to the four control product terms and four uncom-

mitted product terms of each programmable I/O macro cell that has been configured as an output.

An I/O cell is programmed as an input by tying the output enable pin, pin 13, HIGH or by programming the output enable product term to provide a LOW, thereby disabling the output buffer, for all possible input combinations.

When utilizing the I/O macro cell as an output, the input path functions as a feedback path allowing the output signal to be fed back as an input to the product term array. When the output cell is configured as a registered output, this feed back path may be used to feed back the current output state to the device inputs to provide current state control of the next output state as required for state machine implementation.

### Preload and Power-up Reset

Functional testability of programmed devices is enhanced by inclusion of register preload capability which allows the state of each register to be set by loading each register from an external source prior to exercising the device. Testing of complex state machine designs is simplified by the ability to load an arbitrary state without cycling through long test vector sequences to reach the desired state. Recovery from illegal states can be verified by loading illegal states and observing recovery. Preload of a particular register is accomplished by impressing the desired state on the register output pin and lowering the signal level on the preload control pin (pin 1) to a logic LOW level. If the specified preload set up, hold and pulse width minimums have been observed, the desired state is loaded into the register. To insure predictable system initialization, all registers are preset to a logic LOW state upon power up, thereby setting the active LOW outputs to a logic HIGH.

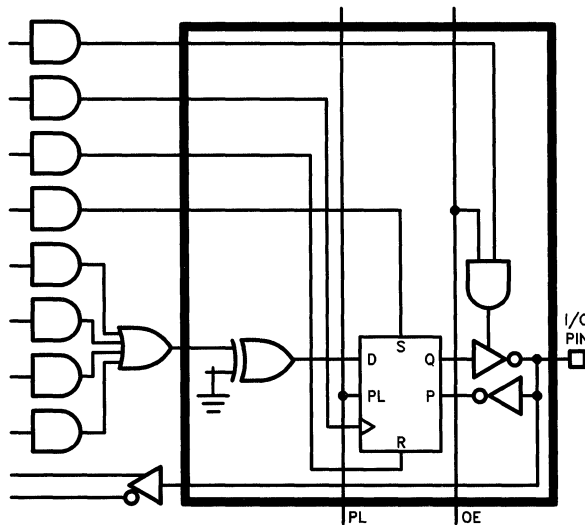


Figure 1. PLD C 20RA10 Macro Cell

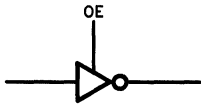
0118-4

**Output Always Enabled**



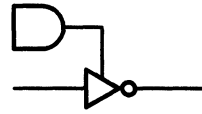
0118-13

**Hard-Wired**



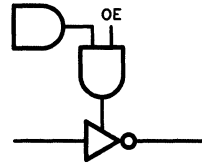
0118-15

**Programmable**



0118-14

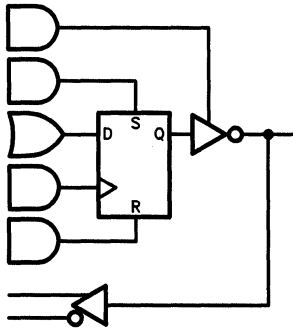
**Combination of Programmable and Hard-Wired**



0118-16

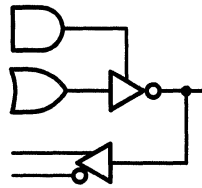
**Figure 2. Four Possible Output Enable Alternatives for the PLD C 20RA10**

**Registered/Active LOW**



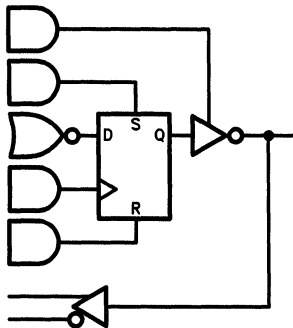
0118-17

**Combinatorial/Active LOW**



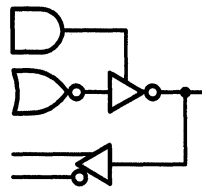
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**Registered/Active HIGH**



0118-19

**Combinatorial/Active HIGH**



0118-20

**Figure 3. Four Possible Macro Cell Configurations for the PLD C 20RA10**

## Selection Guide

| Generic Part Number | tpd ns |     | tsu ns |     | tco ns |     | ICC mA |     |
|---------------------|--------|-----|--------|-----|--------|-----|--------|-----|
|                     | Com    | Mil | Com    | Mil | Com    | Mil | Com    | Mil |
| 20RA10-20           | 20     | —   | 10     | —   | 20     | —   | 80     | —   |
| 20RA10-25           | —      | 25  | —      | 15  | —      | 25  | —      | 100 |
| 20RA10-30           | 30     | —   | 15     | —   | 30     | —   | 80     | —   |
| 20RA10-35           | —      | 35  | —      | 20  | —      | 35  | —      | 100 |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential

(Pin 24 to Pin 12) ..... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Output Current into Outputs (LOW) ..... 16 mA

Static Discharge Voltage ..... > 2001V  
(per MIL-STD-883 Method 3015)

Latchup Current ..... > 200 mA

DC Programming Voltage ..... 13.0V

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +75°C        | 5V ± 10%        |
| Military <sup>[5]</sup> | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over Operating Range<sup>[6]</sup>

| Parameters      | Description                  | Test Conditions   |                           | Min.  | Max. | Units |
|-----------------|------------------------------|---|---------------------------|-------|------|-------|
|                 |                              |   |                           |       |      |       |
| V <sub>OH</sub> | Output HIGH Voltage          | V <sub>CC</sub> = Min.,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | I <sub>OH</sub> = -3.2 mA | COM'L | 2.4  | V     |
|                 |                              |   | I <sub>OH</sub> = -2 mA   | MIL   |      |       |
| V <sub>OL</sub> | Output LOW Voltage           | V <sub>CC</sub> = Min.,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | I <sub>OL</sub> = 8 mA    |       | 0.5  | V     |
| V <sub>IH</sub> | Input HIGH Level             | Guaranteed Input Logical HIGH Voltage for All Inputs <sup>[1]</sup>             |                           | 2.0   |      | V     |
| V <sub>IL</sub> | Input LOW Level              | Guaranteed Input Logical LOW Voltage for All Inputs <sup>[1]</sup>              |                           |       | 0.8  | V     |
| I <sub>IX</sub> | Input Leakage Current        | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> , V <sub>CC</sub> = Max.    |                           | -10   | 10   | μA    |
| I <sub>OZ</sub> | Output Leakage Current       | V <sub>CC</sub> = Max., V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>    |                           | -40   | 40   | μA    |
| I <sub>SC</sub> | Output Short Circuit Current | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V <sup>[2]</sup>                  |                           | -30   | -90  | mA    |
| I <sub>CC</sub> | Power Supply Current         | V <sub>CC</sub> = Max., V <sub>IN</sub> = GND Outputs Open                      | COM'L                     |       | 80   | mA    |
|                 |                              |   | MIL                       |       | 100  | mA    |

## Capacitance<sup>[3]</sup>

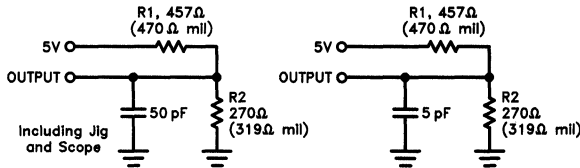
| Parameters       | Description        | Test Conditions                     | Min. | Max. | Units |
|------------------|--------------------|-------------------------------------|------|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | V <sub>IN</sub> = 2.0V @ f = 1 MHz  |      | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance | V <sub>OUT</sub> = 2.0V @ f = 1 MHz |      | 8    |       |

### Notes:

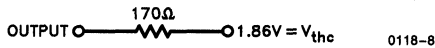
- These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V<sub>OUT</sub> = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.
- Figure 4a test load used for all parameters except t<sub>EA</sub>, t<sub>ER</sub>, t<sub>PZX</sub> and t<sub>PXZ</sub>. Figure 4b test load used for t<sub>EA</sub>, t<sub>ER</sub>, t<sub>PZX</sub> and t<sub>PXZ</sub>.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- The parameters t<sub>ER</sub> and t<sub>PXZ</sub> are measured as the delay from the input disable logic threshold transition to V<sub>OH</sub> - 0.5V for an enabled HIGH output or V<sub>OL</sub> + 0.5V for an enabled LOW output. Please see Table 1 for waveforms and measurement reference levels.

**Switching Characteristics PLD C 20RA10 Over Operating Range<sup>[4, 6, 7]</sup>**

| Parameters       | Description                                | Commercial |      |      |      | Military |      |      |      | Units |
|------------------|--|------------|------|------|------|----------|------|------|------|-------|
|                  |  | -20        |      | -30  |      | -25      |      | -35  |      |       |
|                  |  | Min.       | Max. | Min. | Max. | Min.     | Max. | Min. | Max. |       |
| t <sub>PD</sub>  | Input or Feedback to Non-Registered Output |            | 20   |      | 30   |          | 25   |      | 35   | ns    |
| t <sub>EA</sub>  | Input to Output Enable                     |            | 25   |      | 30   |          | 30   |      | 35   | ns    |
| t <sub>ER</sub>  | Input to Output Disable                    |            | 25   |      | 30   |          | 30   |      | 35   | ns    |
| t <sub>PZX</sub> | Pin 13 to Output Enable                    |            | 15   |      | 20   |          | 20   |      | 25   | ns    |
| t <sub>PXZ</sub> | Pin 13 to Output Disable                   |            | 15   |      | 20   |          | 20   |      | 25   | ns    |
| t <sub>CO</sub>  | Clock to Output                            |            | 20   |      | 30   |          | 25   |      | 35   | ns    |
| t <sub>SU</sub>  | Input or Feedback Setup Time               | 10         |      | 15   |      | 15       |      | 20   |      | ns    |
| t <sub>H</sub>   | Hold Time                                  | 0          |      | 5    |      | 0        |      | 5    |      | ns    |
| t <sub>p</sub>   | Clock Period                               | 30         |      | 45   |      | 40       |      | 55   |      | ns    |
| t <sub>WH</sub>  | Clock Width HIGH                           | 13         |      | 20   |      | 18       |      | 25   |      | ns    |
| t <sub>WL</sub>  | Clock Width LOW                            | 13         |      | 20   |      | 18       |      | 25   |      | ns    |
| f <sub>MAX</sub> | Maximum Frequency                          | 33.3       |      | 22.2 |      | 25.0     |      | 18.1 |      | MHz   |
| t <sub>S</sub>   | Input to Asynchronous Set                  |            | 20   |      | 35   |          | 25   |      | 40   | ns    |
| t <sub>R</sub>   | Input to Asynchronous Reset                |            | 25   |      | 40   |          | 30   |      | 45   | ns    |
| t <sub>AR</sub>  | Asynchronous Set/Reset Recovery Time       | 20         |      | 30   |      | 25       |      | 35   |      | ns    |
| t <sub>WP</sub>  | Preload Pulse Width                        | 30         |      | 35   |      | 35       |      | 40   |      | ns    |
| t <sub>SUP</sub> | Preload Setup Time                         | 20         |      | 25   |      | 25       |      | 30   |      | ns    |
| t <sub>HP</sub>  | Preload Hold Time                          | 20         |      | 25   |      | 25       |      | 30   |      | ns    |

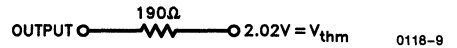
**AC Test Loads and Waveforms (Commercial)**

**Figure 4a**
**Figure 4b**

Equivalent to: THÉVENIN EQUIVALENT (Commercial)

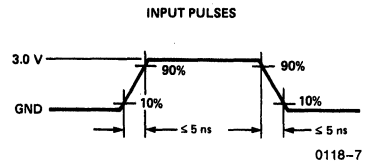


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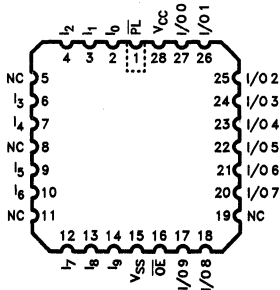
Equivalent to: THÉVENIN EQUIVALENT (Military)



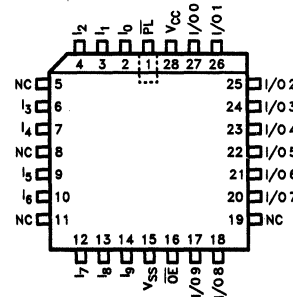
0118-9


**Figure 5**

0118-6


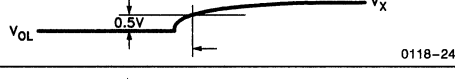
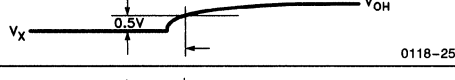
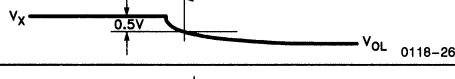
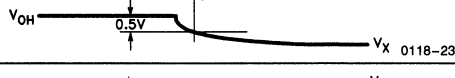
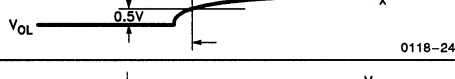
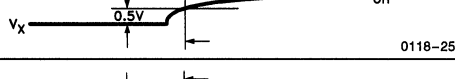

**LCC and PLCC Pinouts**


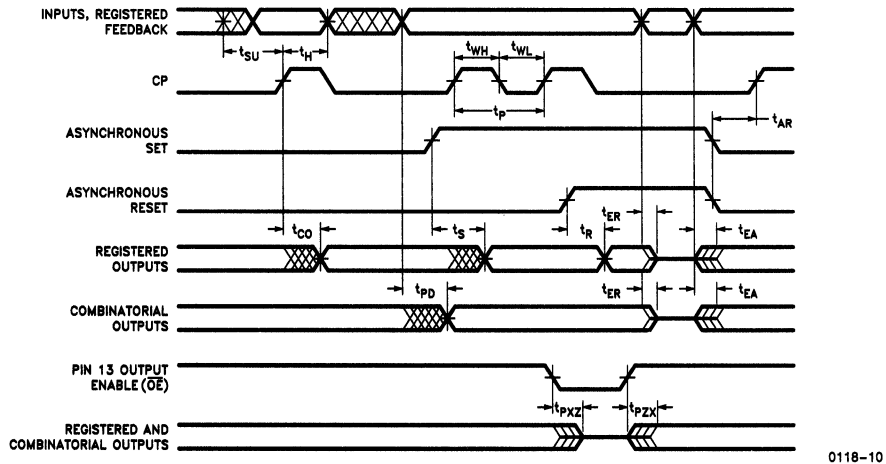
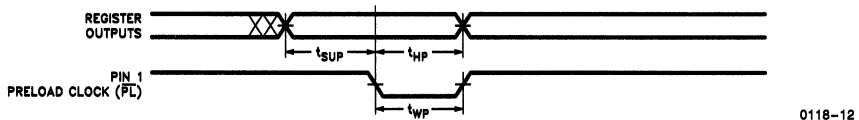
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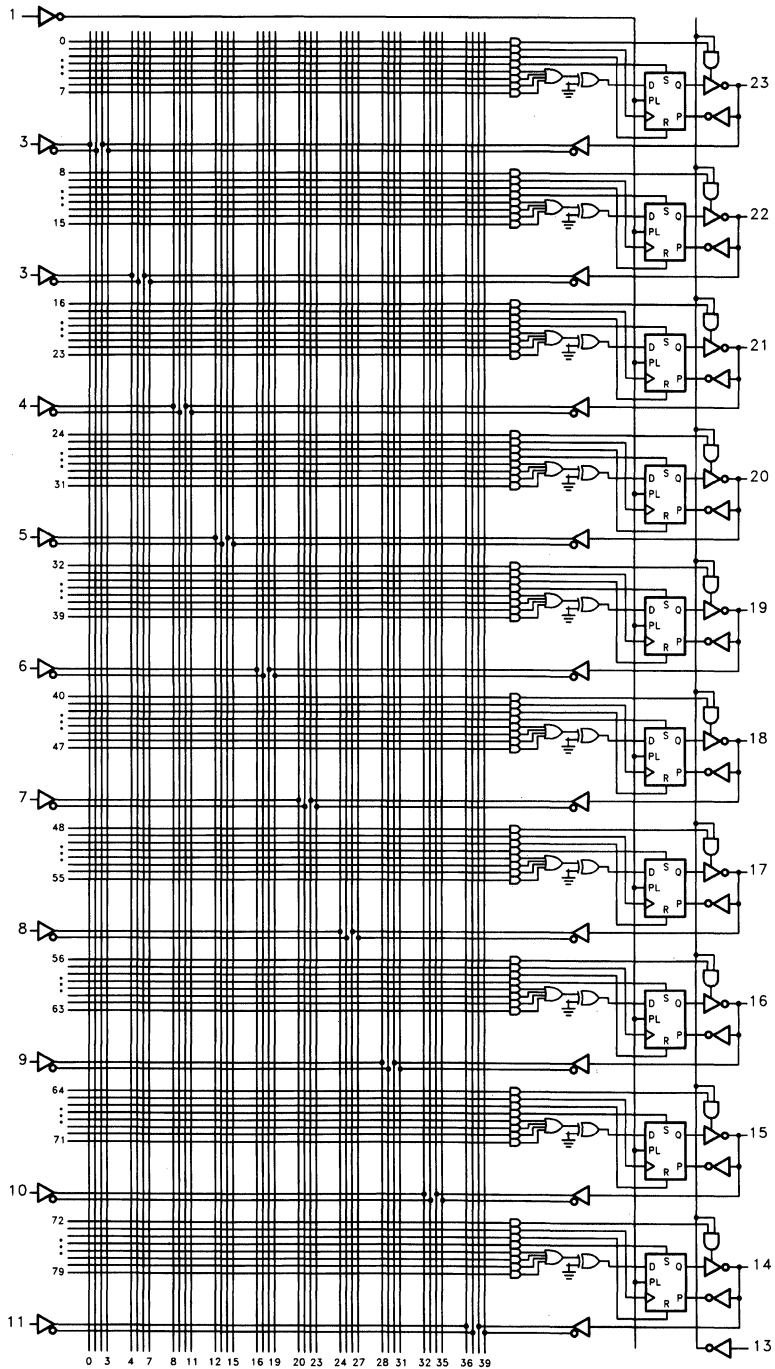
**Table 1**

| Parameter    | $V_X$     | Output Waveform—Measurement Level   |
|--------------|-----------|---|
| $t_{PXZ}(-)$ | 1.5V      |  $V_{OH}$ $V_X$ 0118-23 |
| $t_{PXZ}(+)$ | 2.6V      |  $V_{OL}$ $V_X$ 0118-24 |
| $t_{PZX}(+)$ | $V_{thc}$ |  $V_X$ $V_{OH}$ 0118-25 |
| $t_{PZX}(-)$ | $V_{thc}$ |  $V_X$ $V_{OL}$ 0118-26 |
| $t_{ER}(-)$  | 1.5V      |  $V_{OH}$ $V_X$ 0118-23 |
| $t_{ER}(+)$  | 2.6V      |  $V_{OL}$ $V_X$ 0118-24 |
| $t_{EA}(+)$  | $V_{thc}$ |  $V_X$ $V_{OH}$ 0118-25 |
| $t_{EA}(-)$  | $V_{thc}$ |  $V_X$ $V_{OL}$ 0118-26 |

**4**
**Switching Waveforms**

**Preload Switching Waveforms**




Functional Logic Diagram PLD C 20RA10



**Ordering Information**

| ICC (mA) | tpD (ns) | tSU (ns) | tCO (ns) | Ordering Code      | Package | Operating Range |
|----------|----------|----------|----------|--------------------|---------|-----------------|
| 80       | 20       | 10       | 20       | PLD C 20RA10-20PC  | P13     | Commercial      |
|          |          |          |          | PLD C 20RA10-20WC  | W14     |                 |
|          |          |          |          | PLD C 20RA10-20JC  | J64     |                 |
| 100      | 25       | 15       | 25       | PLD C 20RA10-25DMB | D14     | Military        |
|          |          |          |          | PLD C 20RA10-25WMB | W14     |                 |
|          |          |          |          | PLD C 20RA10-25LMB | L64     |                 |
|          |          |          |          | PLD C 20RA10-25QMB | Q64     |                 |
| 80       | 30       | 15       | 30       | PLD C 20RA10-30PC  | P13     | Commercial      |
|          |          |          |          | PLD C 20RA10-30WC  | W14     |                 |
|          |          |          |          | PLD C 20RA10-30JC  | J64     |                 |
| 100      | 35       | 20       | 35       | PLD C 20RA10-35DMB | D14     | Military        |
|          |          |          |          | PLD C 20RA10-35WMB | W14     |                 |
|          |          |          |          | PLD C 20RA10-35LMB | L64     |                 |
|          |          |          |          | PLD C 20RA10-35QMB | Q64     |                 |

**MILITARY SPECIFICATIONS****Group A Subgroup Testing****DC Characteristics**

| Parameters      | Subgroups |
|-----------------|-----------|
| V <sub>OH</sub> | 1,2,3     |
| V <sub>OL</sub> | 1,2,3     |
| V <sub>IH</sub> | 1,2,3     |
| V <sub>IL</sub> | 1,2,3     |
| I <sub>Ix</sub> | 1,2,3     |
| I <sub>OZ</sub> | 1,2,3     |
| I <sub>CC</sub> | 1,2,3     |

**Switching Characteristics**

| Parameters       | Subgroups |
|------------------|-----------|
| t <sub>PD</sub>  | 9,10,11   |
| t <sub>PZX</sub> | 9,10,11   |
| t <sub>CO</sub>  | 9,10,11   |
| t <sub>SU</sub>  | 9,10,11   |
| t <sub>H</sub>   | 9,10,11   |

Document #: 38-00073-A



**Features**

- Advanced second generation PAL architecture
- Low power
  - 55 mA max "I"
  - 90 mA max standard
  - 120 mA max military
- CMOS EPROM technology for reprogrammability
- Variable product terms
  - 2 × (8 thru 16) product terms
- User programmable macro cell
  - Output polarity control
  - Individually selectable for registered or combinatorial operation
  - "15" commercial & industrial
    - 10 ns tCO
    - 10 ns tS
    - 15 ns tPD
    - 50 MHz

- "20" military
  - 15 ns tCO
  - 17 ns tS
  - 20 ns tPD
  - 31 MHz
- Up to 22 input terms and 10 outputs
- Enhanced test features
  - Phantom array
  - Top Test
  - Bottom Test
  - Preload
- High reliability
  - Proven EPROM technology
  - > 2000V input protection
  - 100% programming and functional testing
- Windowed DIP, windowed LCC, DIP, LCC, PLCC available

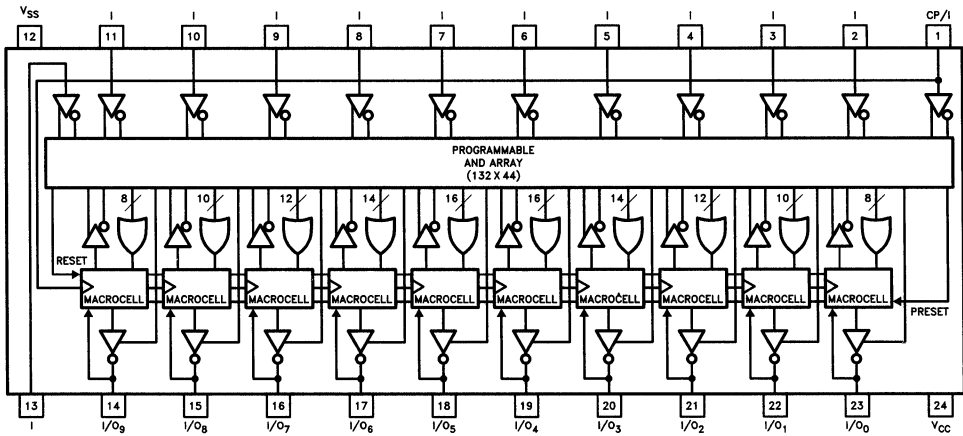
**Functional Description**

The Cypress PAL C 22V10 is a CMOS second generation Programmable Logic Array device. It is implemented with the familiar sum-of-products (AND-OR) logic structure and a new concept, the "Programmable Macro Cell".

The PAL C 22V10 is executed in a 24 pin 300 mil molded DIP, a 300 mil windowed Cerdip, a 28 lead square ceramic leadless chip carrier, a 28 lead square plastic leaded chip carrier and provides up to 22 inputs and 10 outputs. When the windowed CERDIP is exposed to UV light, the 22V10 is erased and then can be reprogrammed. The Programmable Macro Cell provides the capability of defining the architecture of each output individually. Each of the 10 potential outputs may be specified to be "REGISTERED" or "COMBINATORIAL". Polarity of

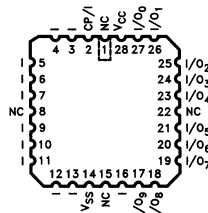
PAL® is a registered trademark of Monolithic Memories Inc.

**Logic Symbol and Pinout**



0023-1

**LCC and PLCC Pinout**



0023-10

## Functional Description (Continued)

each output may also be individually selected allowing complete flexibility of output configuration. Further configurability is provided through "ARRAY" configurable "OUTPUT ENABLE" for each potential output. This feature allows the 10 outputs to be reconfigured as inputs on an individual basis or alternately used as a combination I/O controlled by the programmable array.

The PAL C 22V10 features a "VARIABLE PRODUCT TERM" architecture. There are 5 pairs of product terms beginning at 8 product terms per output and incrementing by 2 to 16 product terms per output. By providing this variable structure the PAL C 22V10 is optimized to the configurations found in a majority of applications without creating devices that burden the product term structures with unuseable product terms and lower performance.

Additional features of the Cypress PAL C 22V10 include a synchronous PRESET and an asynchronous RESET product term. These product terms are common to all MACRO CELLS eliminating the need to dedicate standard product terms for initialization functions. The device automatically resets on power-up.

The PAL C 22V10 featuring programmable macro cells and variable product terms provides a device with the flexibility to implement logic functions in the 500 to 800 gate array complexity. Since each of the 10 output pins may be individually configured as inputs on a temporary or permanent basis, functions requiring up to 21 inputs and only a single output down to 12 inputs and 10 outputs are possible. The 10 potential outputs are enabled through the use of product terms. Any output pin may be permanently selected as an output or arbitrarily enabled as an output and an input through the selective use of individual product terms associated with each output. Each of these outputs is achieved through an individual programmable macro cell. These macro cells are programmable to provide a combinatorial or registered inverting or non-inverting output. In a

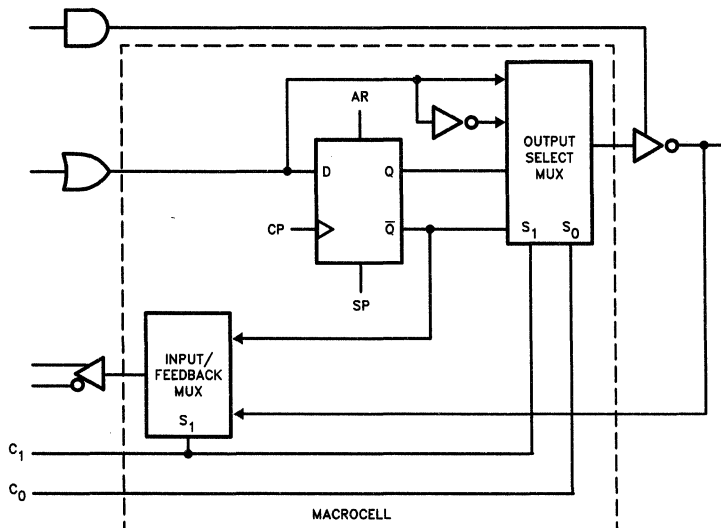
registered mode of operation, the output of the register is fed back into the array providing current status information to the array. This information is available for establishing the next result in applications such as control-state-machines. In a combinatorial configuration, the combinatorial output or, if the output is disabled, the signal present on the I/O pin is made available to the array. The flexibility provided by both programmable macro cell product term control of the outputs and variable product terms allows a significant gain in functional density through the use of programmable logic.

Along with this increase in functional density, the Cypress PAL C 22V10 provides lower power operation thru the use of CMOS technology, increased testability with a register preload feature and guaranteed AC performance through the use of a phantom array. This phantom array (P<sub>0</sub>-P<sub>3</sub>) and the "TOP TEST" and "BOTTOM TEST" features allow the 22V10 to be programmed with a test pattern and tested prior to shipment for full AC specifications without using any of the functionality of the device specified for the product application. In addition, this same phantom array may be used to test the PAL C 22V10 at incoming inspection before committing the device to a specific function through programming. PRELOAD facilitates testing programmed devices by loading initial values into the registers.

Configuration Table 1

| Registered/Combinatorial |                |                           |
|--------------------------|----------------|---------------------------|
| C <sub>1</sub>           | C <sub>0</sub> | Configuration             |
| 0                        | 0              | Registered/Active Low     |
| 0                        | 1              | Registered/Active High    |
| 1                        | 0              | Combinatorial/Active Low  |
| 1                        | 1              | Combinatorial/Active High |

## Macrocell



0023-2

**Selection Guide**

| Generic Part Number | ICC1 mA |         |     | tpD ns  |     | ts ns   |     | tCO ns  |     |
|---------------------|---------|---------|-----|---------|-----|---------|-----|---------|-----|
|                     | “L”     | Com/Ind | Mil | Com/Ind | Mil | Com/Ind | Mil | Com/Ind | Mil |
| 22V10B-15           |         | 90      | —   | 15      | —   | 10      | —   | 10      | —   |
| 22V10B-20           | —       | —       | 120 | —       | 20  | —       | 17  | —       | 15  |
| 22V10-20            |         | 90      | —   | 20      | —   | 12      | —   | 12      | —   |
| 22V10-25            | 55      | 90      | 100 | 25      | 25  | 15      | 18  | 15      | 15  |
| 22V10-30            |         | —       | 100 | —       | 30  | —       | 20  | —       | 20  |
| 22V10-35            | 55      | 90      | —   | 35      | —   | 30      | —   | 25      | —   |
| 22V10-40            |         | —       | 100 | —       | 40  | —       | 30  | —       | 25  |

**4**
**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied ..... -55°C to +125°C  
 Supply Voltage to Ground Potential  
 (Pin 24 to Pin 12) ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs  
 in High Z State ..... -0.5V to +7.0V  
 DC Input Voltage ..... -3.0V to +7.0V  
 Output Current into Outputs (Low) ..... 16 mA  
 UV Exposure ..... 7258 Wsec/cm<sup>2</sup>

DC Programming Voltage  
 PAL C 22V10B ..... 13.0V  
 PAL C 22V10 ..... 14.0V  
 Static Discharge Voltage ..... > 2001V  
 (per MIL-STD-883 Method 3015)  
 Latchup Current ..... > 200 mA

**Operating Range**

| Range                   | Ambient Temperature | VCC      |
|-------------------------|---------------------|----------|
| Commercial              | 0°C to +75°C        | 5V ± 10% |
| Military <sup>[7]</sup> | -55°C to +125°C     | 5V ± 10% |
| Industrial              | -40°C to +85°C      | 5V ± 10% |

**Electrical Characteristics Over Operating Range<sup>[6]</sup>**

| Parameters | Description                                   | Test Conditions   |               | Min.      | Max.       | Units |    |
|------------|---|---|---------------|-----------|------------|-------|----|
|            |   |   |               |           |            |       |    |
| VOH1       | Output HIGH Voltage                           | VCC = Min.,<br>VIN = VIH or VIL                                     | IOH = -3.2 mA | COM'L/IND | 2.4        | V     |    |
|            |   |   | IOH = -2 mA   | MIL       |            |       |    |
| VOH2       | HIGH Level CMOS Output Voltage <sup>[3]</sup> | VCC = Min.,<br>VIN = VIH or VIL                                     | IOH = 100 μA  |           | VCC - 1.0V | V     |    |
| VOL        | Output LOW Voltage                            | VCC = Min.,<br>VIN = VIH or VIL                                     | IOL = 16 mA   | COM'L/IND | 0.5        | V     |    |
|            |   |   | IOL = 12 mA   | MIL       |            |       |    |
| VIH        | Input HIGH Level                              | Guaranteed Input Logical HIGH Voltage for All Inputs <sup>[1]</sup> |               |           | 2.0        | V     |    |
| VIL        | Input LOW Level                               | Guaranteed Input Logical LOW Voltage for All Inputs <sup>[1]</sup>  |               |           | 0.8        | V     |    |
| IX         | Input Leakage Current                         | VSS ≤ VIN ≤ VCC, VCC = Max.   |               |           | -10        | 10    | μA |
| IOZ        | Output Leakage Current                        | VCC = Max., VSS ≤ VOUT ≤ VCC  |               |           | -40        | 40    | μA |
| ISC        | Output Short Circuit Current                  | VCC = Max., VOUT = 0.5V <sup>[2]</sup>                              |               |           | -30        | -90   | mA |
| ICC1       | Standby Power Supply Current                  | VCC = Max., VIN = GND Outputs Open                                  | “L”           |           | 55         | mA    |    |
|            |   |   | COM'L/IND     |           | 90         | mA    |    |
|            |   |   | MIL           |           | 100        | mA    |    |
|            |   |   | MIL-20        |           | 120        | mA    |    |

**Notes:**

- These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. VOUT = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.
- Figure 1a test load used for all parameters except tEA, tER, tpZX and tpXZ. Figure 1b test load used for tEA, tER, tpZX and tpXZ.
- Preliminary specifications.
- See the last page of this specification for Group A subgroup testing information.
- TA is the “instant on” case temperature.

**Capacitance<sup>[3]</sup>**

| Parameters       | Description        | Test Conditions                     | Min. | Max. | Units |
|------------------|--------------------|-------------------------------------|------|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | V <sub>IN</sub> = 2.0V @ f = 1 MHz  |      | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance | V <sub>OUT</sub> = 2.0V @ f = 1 MHz |      | 8    | pF    |

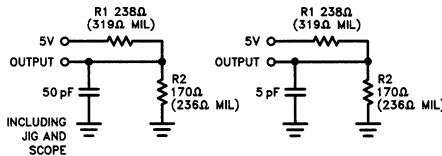
**Switching Characteristics PAL C 22V10<sup>[4, 6]</sup>**

| Parameters        | Description   | Commercial & Industrial |      |      |      |      |      |      |      | Military |      |      |      |      |      |      |      | Units |
|-------------------|---|-------------------------|------|------|------|------|------|------|------|----------|------|------|------|------|------|------|------|-------|
|                   |   | B-15                    |      | -20  |      | -25  |      | -35  |      | B-20     |      | -25  |      | -30  |      | -40  |      |       |
|                   |   | Min.                    | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min.     | Max. | Min. | Max. | Min. | Max. | Min. | Max. |       |
| t <sub>PD</sub>   | Input to Output Propagation Delay <sup>[14]</sup>   |                         | 15   |      | 20   |      | 25   |      | 35   |          | 20   |      | 25   |      | 30   |      | 40   | ns    |
| t <sub>EA</sub>   | Input to Output Enable Delay  |                         | 15   |      | 20   |      | 25   |      | 35   |          | 20   |      | 25   |      | 25   |      | 40   | ns    |
| t <sub>ER</sub>   | Input to Output Disable Delay <sup>[9]</sup>  |                         | 15   |      | 20   |      | 25   |      | 35   |          | 20   |      | 25   |      | 25   |      | 40   | ns    |
| t <sub>CO</sub>   | Clock to Output Delay <sup>[15]</sup>   |                         | 10   |      | 12   |      | 15   |      | 25   |          | 15   |      | 15   |      | 20   |      | 25   | ns    |
| t <sub>S</sub>    | Input or Feedback Setup Time  | 10                      |      | 12   |      | 15   |      | 30   |      | 17       |      | 18   |      | 20   |      | 30   |      | ns    |
| t <sub>H</sub>    | Input Hold Time   | 0                       |      | 0    |      | 0    |      | 0    |      | 0        |      | 0    |      | 0    |      | 0    |      | ns    |
| t <sub>P</sub>    | External Clock Period (t <sub>CO</sub> + t <sub>S</sub> )                                   | 20                      |      | 24   |      | 30   |      | 55   |      | 32       |      | 33   |      | 40   |      | 55   |      | ns    |
| t <sub>WH</sub>   | Clock Width HIGH <sup>[3]</sup>   | 6                       |      | 10   |      | 12   |      | 17   |      | 12       |      | 14   |      | 16   |      | 22   |      | ns    |
| t <sub>WL</sub>   | Clock Width LOW <sup>[3]</sup>  | 6                       |      | 10   |      | 12   |      | 17   |      | 12       |      | 14   |      | 16   |      | 22   |      | ns    |
| f <sub>MAX1</sub> | External Maximum Frequency (1/(t <sub>CO</sub> + t <sub>S</sub> )) <sup>[10]</sup>          | 50.0                    |      | 41.6 |      | 33.3 |      | 18.1 |      | 31.2     |      | 30.3 |      | 25.0 |      | 18.1 |      | MHz   |
| f <sub>MAX2</sub> | Data Path Maximum Frequency (1/(t <sub>WH</sub> + t <sub>WL</sub> )) <sup>[3, 11]</sup>     | 83.3                    |      | 50.0 |      | 41.6 |      | 29.4 |      | 41.6     |      | 35.7 |      | 31.2 |      | 22.7 |      | MHz   |
| f <sub>MAX3</sub> | Internal Feedback Maximum Frequency (1/(t <sub>CF</sub> + t <sub>S</sub> )) <sup>[12]</sup> | 80.0                    |      | 45.4 |      | 35.7 |      | 20.8 |      | 33.3     |      | 32.2 |      | 28.5 |      | 20.0 |      | MHz   |
| t <sub>CF</sub>   | Register Clock to Feedback Input <sup>[13]</sup>  |                         | 2.5  |      | 10   |      | 13   |      | 18   |          | 13   |      | 13   |      | 15   |      | 20   | ns    |
| t <sub>AW</sub>   | Asynchronous Reset Width  | 15                      |      | 20   |      | 25   |      | 35   |      | 20       |      | 25   |      | 30   |      | 40   |      | ns    |
| t <sub>AR</sub>   | Asynchronous Reset Recovery Time  | 10                      |      | 20   |      | 25   |      | 35   |      | 20       |      | 25   |      | 30   |      | 40   |      | ns    |
| t <sub>AP</sub>   | Asynchronous Reset to Registered Output Delay   |                         | 20   |      | 25   |      | 25   |      | 35   |          | 25   |      | 25   |      | 30   |      | 40   | ns    |
| t <sub>SPR</sub>  | Synchronous Preset Recovery Time  | 10                      |      | 20   |      | 25   |      | 35   |      | 20       |      | 25   |      | 30   |      | 40   |      | ns    |
| t <sub>PR</sub>   | Power Up Reset Time <sup>[16]</sup>   | 1.0                     |      | 1.0  |      | 1.0  |      | 1.0  |      | 1.0      |      | 1.0  |      | 1.0  |      | 1.0  |      | μs    |

**Notes:**

8. This parameter is sample tested periodically with the device clocked at  $f_{MAX}$  external ( $f_{MAX1}$ ) with all registers cycling on each cycle and outputs disabled (in high Z state).
9. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous high level has fallen to 0.5 volts below  $V_{OH}$  Min. or a previous low level has risen to 0.5 volts above  $V_{OL}$  Max. Please see *Figure 4* for enable and disable test waveforms and measurement reference levels.
10. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feed back can operate.
11. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feed back can operate. This parameter is tested periodically by sampling production product.
13. This parameter is calculated from the clock period at  $f_{MAX}$  internal ( $f_{MAX3}$ ) as measured (see note 12 above) minus  $t_s$ .
14. This specification is guaranteed for all device outputs changing state in a given access cycle. See *Figure 3* for the minimum guaranteed negative correction which may be subtracted from  $t_{pp}$  for cases in which fewer outputs are changing state per access cycle.
15. This specification is guaranteed for all device outputs changing state in a given access cycle. See *Figure 3* for the minimum guaranteed negative correction which may be subtracted from  $t_{CO}$  for cases in which fewer outputs are changing state per access cycle.
16. The registers in the PAL C 22V10 have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in  $V_{CC}$  must be monotonic and the timing constraints depicted in *Figure 5* must be satisfied.

**AC Test Loads and Waveforms (Commercial)**

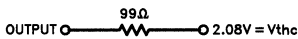


**Figure 1a**

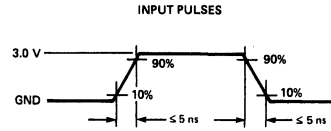
**Figure 1b**

0023-11

Equivalent to: THÉVENIN EQUIVALENT (Commercial)



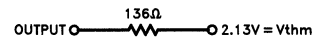
0023-13



**Figure 2**

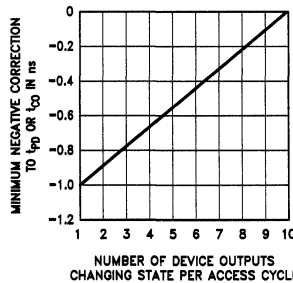
0023-12

Equivalent to: THÉVENIN EQUIVALENT (Military)



0023-14

**Minimum Negative Correction to  $t_{pp}$  and  $t_{CO}$  vs. Number of Outputs Switching**



**Figure 3**

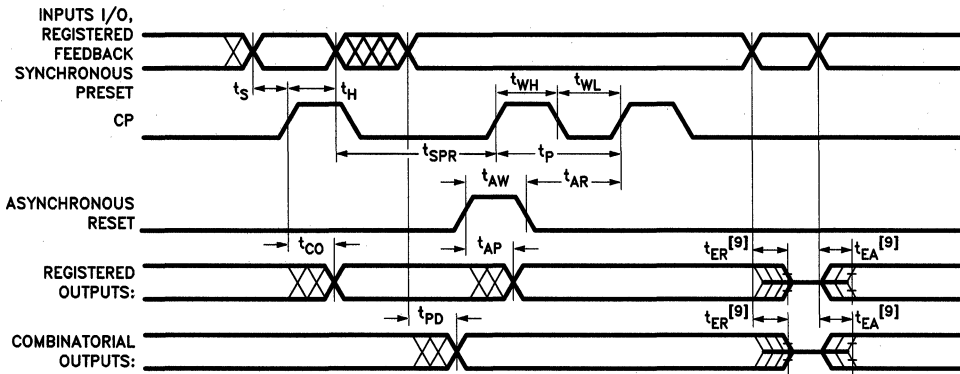
0023-20

| Parameter   | $V_X$     | Output Waveform—Measurement Level |
|-------------|-----------|-----------------------------------|
| $t_{ER}(-)$ | 1.5V      |                                   |
| $t_{ER}(+)$ | 2.6V      |                                   |
| $t_{EA}(+)$ | $V_{thc}$ |                                   |
| $t_{EA}(-)$ | $V_{thc}$ |                                   |

**Figure 4. Test Waveforms**



Switching Waveforms



0023-3

Power Up Reset Waveforms<sup>[16]</sup>

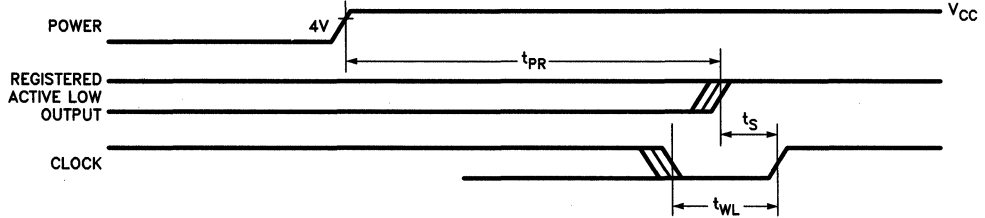
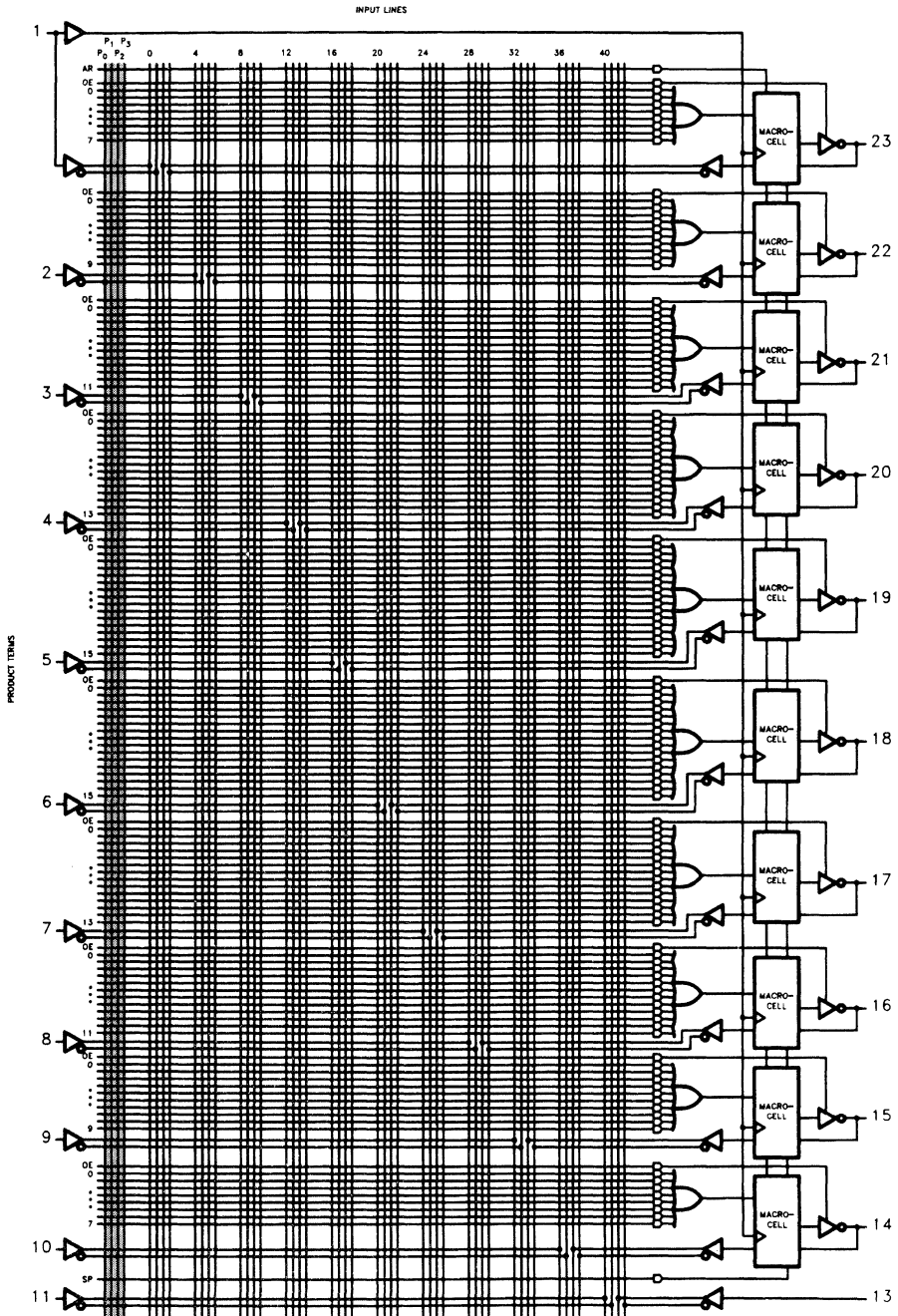


Figure 5

0023-21

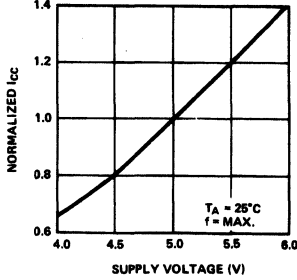
Functional Logic Diagram PAL C 22V10



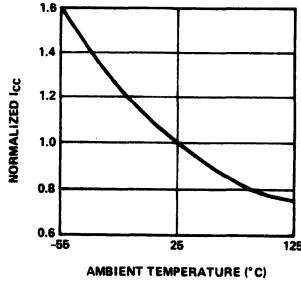
4

Typical DC and AC Characteristics

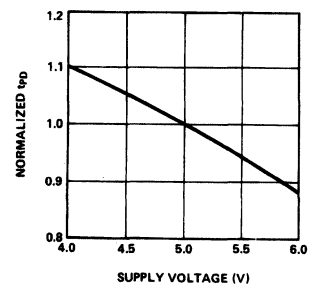
**NORMALIZED STANDBY SUPPLY CURRENT ( $I_{CC1}$ ) vs. SUPPLY VOLTAGE**



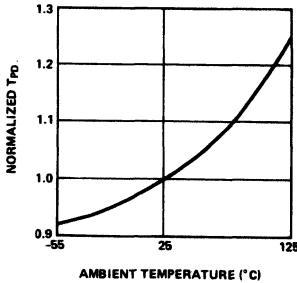
**NORMALIZED STANDBY SUPPLY CURRENT ( $I_{CC1}$ ) vs. AMBIENT TEMPERATURE**



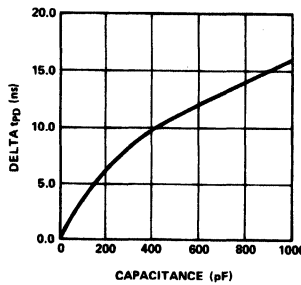
**NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE**



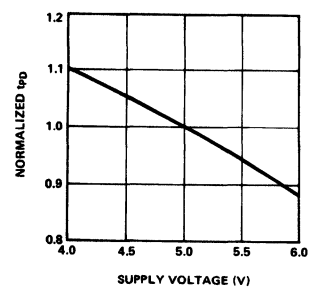
**NORMALIZED PROPAGATION DELAY vs. TEMPERATURE**



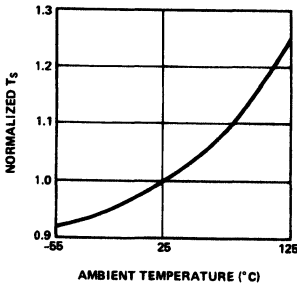
**DELTA PROPAGATION TIME vs. OUTPUT LOADING**



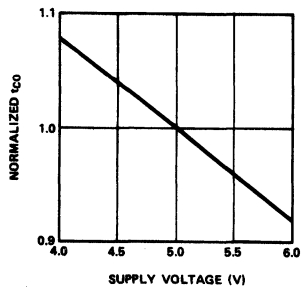
**NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE**



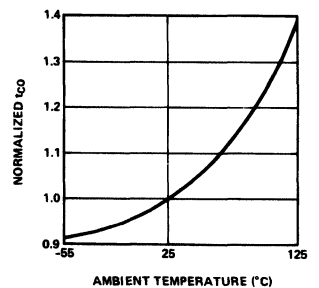
**NORMALIZED SETUP TIME vs. TEMPERATURE**



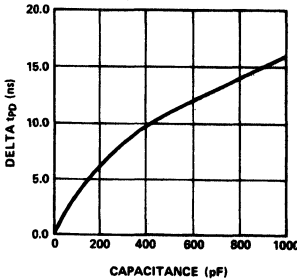
**NORMALIZED CLOCK TO OUTPUT TIME vs. SUPPLY VOLTAGE**



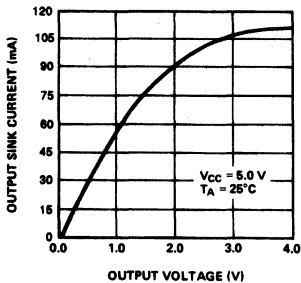
**NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE**



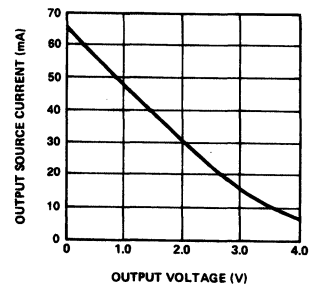
**DELTA CLOCK TO OUTPUT TIME vs. OUTPUT LOADING**



**OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE**



**OUTPUT SOURCE CURRENT vs. VOLTAGE**



## Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the PAL C 22V10. For this reason, an opaque label should be placed over the window if the device is exposed to sunlight or fluorescent lighting for extended periods of time. In addition, high ambient light levels can create hole-electron pairs which may cause “blank” check failures or “verify errors” when programming “windowed” parts. This phenomenon can be avoided by use of an opaque label over the window during programming in high ambient light environments.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity  $\times$  exposure time) of 25 Wsec/cm<sup>2</sup>. For an ultraviolet lamp with a 12 mW/cm<sup>2</sup> power rating, the exposure would be approximately 35 minutes. The PAL C 22V10 needs to be placed within 1 inch of the lamp during erasure. Permanent damage may result if the device is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm<sup>2</sup> is the recommended maximum dosage.

## Device Programming

The PAL C 22V10 has multiple programmable functions. In addition to the normal array, a “PHANTOM” array, “TOP and BOTTOM TEST” and a “SECURITY” feature are programmable. The PAL C 22V10 security mechanism, when invoked, prevents access to the “NORMAL” and “TOP/BOTTOM TEST” array. The “PHANTOM” array feature is still accessible, allowing programming and verification of the pattern in the “PHANTOM” array. Functional operation of all other features is allowed regardless of the state of the “SECURITY BIT”. In addition, the device contains 10 MACROCELLS which are programmed to configure the device functionality for each specific application.

The logic array is divided into a “NORMAL” array and a “PHANTOM” array. The normal array is used to configure the device to perform a specific function as required by the user, and the phantom array is provided as a test array for Cypress’ testing the device prior to user programming thus assuring a reliable, thoroughly tested product. The “PHANTOM” array contains four additional columns connected to input pins 2 (TRUE), 7 (INVERTING), 10 (TRUE) and 11 (TRUE). These inputs may be programmed to be connected to all normal product terms. This allows all sense amplifiers and macrocells to be exercised for both functionality and performance after assembly and prior to shipment. These features are in addition to the normal array. They do not affect normal operation, allowing the user full programming of the normal array, while allowing the device to be fully tested.

The “TOP TEST” and “BOTTOM TEST” feature, allow connection of all input terms to either pin 23 or 13. These locations may be programmed and subsequently exercised in the “TOP TEST” and “BOTTOM TEST” mode. Like the Phantom array above, this feature has no effect in the

normal mode of operation. Cells in the PHANTOM ARRAY, TOP TEST, and BOTTOM TEST areas are programmed at Cypress during the manufacturing operation, and they therefore will be programmed when received in a non-windowed package by the user. Consequently, the user will normally have no need to program these cells.

The Cypress PAL C 22V10 contains 10 identical MACROCELLS which may be individually configured. Each MACROCELL is associated with a single I/O pin and through the architecture bits, each associated pin may be permanently configured as an input, an output or be used as both input and output as a function of the logical function in the array. Each MACROCELL consists of a type “D” latch, an output multiplexer, a feedback multiplexer and a tristatable output driver that is controlled by a unique product term. The clock is common to all MACROCELLS, and comes from pin 1 of the device. Each register also has an asynchronous reset and a synchronous preset. These are each driven by product terms. These product terms are common to all MACROCELLS allowing all registers to either be asynchronously reset or synchronously preset by a logical function in the array. The device is automatically reset at power up. A preload feature allows the registers to be preloaded with any state for testing.

The architecture bits C0 and C1 are used to configure each MACROCELL individually. C0 selects the polarity of the output and C1 selects the combinatorial or registered mode of operation. If the registered mode of operation is selected, the feedback path is automatically selected to be from the register. In the combinatorial mode the feedback path is automatically selected to be from the I/O pin. In this combinatorial mode, the output from the array may be fed into the array or if the output is deselected using the output enable product term the pin may be used as an external input. There is not a mode where the I/O pin may be used as a combinatorial output or an input pin, while the register is used as a state register. The architecture bits are programmed as a separate item during normal programming. An I/O pin is configured to be an input by programming the MACROCELL into a combinatorial mode and disabling the output with the output enable product term.

## Pinout

The PAL C 22V10 PROGRAMMING pinout is shown in *Figure 6*. In the Programming pinout configuration, the device may be programmed and verified for the NORMAL mode of operation and also programmed, verified and operated in PHANTOM and TEST modes. These special modes of operation are achieved through the use of supervoltages applied to certain pins. Care should be exercised when entering and exiting these modes, paying specific attention to both the operating modes as specified in Table 1 and the sequencing of the supervoltages as shown in the timing diagrams.

## Programming Pinout

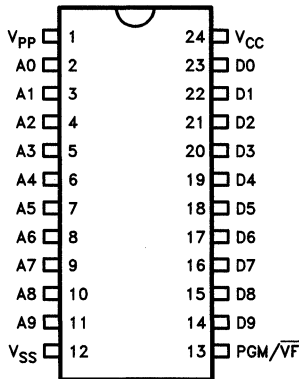


Figure 6

0023-6

## Programming Algorithm

With the exception of the Security bit, all arrays are programmed in a similar manner. The data to be programmed is represented by a "1" or "0" on the I/O pins. A "1" indicates that an unprogrammed location is to be programmed and a "0" indicates that an unprogrammed location is to remain unprogrammed. All locations to be programmed are addressed as row and column locations. Table 1 "Operating Modes" along with Tables 2 through 5 provide the specific address for each addressed location to be programmed along with mode selection information for both programming and operation in the "PHANTOM" and "TEST" modes.

When programming the security bit, a supervoltage on pin 3 is used as data with a programming pulse on pin 13. Verification is controlled with a supervoltage on pins 4 and the data out on pin 3.

## Operating Modes

Table 1 describes the operating and programming modes of the PAL C 22V10. The majority of the programming modes function with a PROGRAM, PROGRAM INHIBIT and PROGRAM VERIFY sequence. The exception is the Security Program operation, which shows no program inhibit function. Two timing diagrams are provided for these two different methodologies of programming in Figures 8 & 9. Tables 2 through 5 are used as indicated to

provide the individual addresses of the various arrays and cells to be programmed. There are 5 operating modes in addition to the programming modes for the PAL C 22V10. These provide NORMAL operation, PHANTOM operation, TOP TEST, BOTTOM TEST and a register preload feature for testing.

In the normal operating mode, all signals are TTL levels and the device functions as it is internally programmed in the NORMAL array. In the PHANTOM mode of operation, the device operates logically as a function of the contents of the PHANTOM array. In this mode pins 2, 10 & 11 are non-inverting inputs and pin 7 is an inverting input. The MACROCELLS function as they are programmed for normal operation. If the MACROCELLS have not yet been programmed, they are in a registered inverting configuration. The PHANTOM mode is invoked by placing a supervoltage  $V_{pp}$  on pin 6. Care should be exercised when entering and leaving this mode that the supervoltage is applied no sooner than 20 ms after the  $V_{CC}$  is stable, and removed a minimum of 20 ms before  $V_{CC}$  is removed.

## TOP and BOTTOM TEST

The TOP TEST and BOTTOM TEST modes are entered and exited in the same manner, with the same concern for power sequencing, but the supervoltage is applied to pins 9 & 10 respectively. In these modes an extra product term controls an output pin. TOP TEST controls pin 23, and BOTTOM TEST controls pin 14. These product terms are controlled by the normal device inputs, and allow testing of all input structures.

## Preload

Finally for testing of programmed functions, a preload feature allows any or all of the registers to be loaded with an initial value for testing. This is accomplished by raising pin 8 to a supervoltage  $V_{pp}$ , which puts the output drivers in a high impedance state. The data to be loaded is then placed on the I/O pins of the device and is loaded into the registers on the positive edge of the clock on pin 1. A "0" on the I/O pin preloads the register with a "0" and a "1" preloads the register with a "1". The actual signal on the output pin will depend on the output polarity selected when the MACROCELL is programmed. The data on the I/O pins is then removed, and pin 8 returned to a normal TTL voltage. Again care should be exercised to power sequence the device properly.

Operating Modes

Table 1

| Operating Modes                                    |                               | Pin 1            | Pin 2            | Pin 3            | Pin 4            | Pin 5            | Pin 6            | Pin 7            | Pin 8            | Pin 9            | Pin 10           | Pin 11           | Pin 13           | Pin 14           | Pin 17           | Pin 20           | Pins 15, 16, 18, 19, 21 & 22 |                  |                  | Pin 23 |  |  |
|--|-------------------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------------------|------------------|------------------|--------|--|--|
| Feature  | Function                      |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                  |                              |                  |                  |        |  |  |
| Main Array Product                                 | Program                       | V <sub>PP</sub>  | Table 2          |                  |                  |                  |                  |                  | Table 3          |                  |                  |                  |                  | V <sub>PP</sub>  | Data In          |                  |                              |                  |                  |        |  |  |
|  | Program Inhibit               | V <sub>PP</sub>  | Table 2          |                  |                  |                  |                  |                  | Table 3          |                  |                  |                  |                  | V <sub>IHP</sub> | High Z           |                  |                              |                  |                  |        |  |  |
|  | Program Verify <sup>[3]</sup> | V <sub>PP</sub>  | Table 2          |                  |                  |                  |                  |                  | Table 3          |                  |                  |                  |                  | V <sub>ILP</sub> | Data Out         |                  |                              |                  |                  |        |  |  |
| Output Enable Product Terms                        | Program                       | V <sub>PP</sub>  | Table 2          |                  |                  |                  |                  |                  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>  | V <sub>PP</sub>  | Data In          |                  |                  |                              |                  |                  |        |  |  |
|  | Program Inhibit               | V <sub>PP</sub>  | Table 2          |                  |                  |                  |                  |                  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>  | V <sub>IHP</sub> | High Z           |                  |                  |                              |                  |                  |        |  |  |
|  | Program Verify                | V <sub>PP</sub>  | Table 2          |                  |                  |                  |                  |                  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>  | V <sub>ILP</sub> | Data Out         |                  |                  |                              |                  |                  |        |  |  |
| Sync Set, Async Reset, Top Test, Bottom Test Notes | Program                       | V <sub>PP</sub>  | Table 2          |                  |                  |                  |                  |                  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>  | Data In          | Data In          | Data In          | V <sub>ILP</sub>             | Data In          |                  |        |  |  |
|  | Program Inhibit               | V <sub>PP</sub>  | Table 2          |                  |                  |                  |                  |                  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | High Z           | High Z           | High Z           | High Z                       | High Z           | High Z           |        |  |  |
|  | Program Verify                | V <sub>PP</sub>  | Table 2          |                  |                  |                  |                  |                  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>ILP</sub> | Data Out         | Data Out         | Data Out         | Driven                       | Data Out         |                  |        |  |  |
| Architecture Bits                                  | Program                       | V <sub>PP</sub>  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>ILP</sub> | Table 4          |                  |                  | V <sub>PP</sub>  | V <sub>PP</sub>  | Data In          |                  |                              |                  |                  |        |  |  |
|  | Program Inhibit               | V <sub>PP</sub>  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>ILP</sub> | Table 4          |                  |                  | V <sub>PP</sub>  | V <sub>IHP</sub> | High Z           |                  |                              |                  |                  |        |  |  |
|  | Program Verify                | V <sub>PP</sub>  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>ILP</sub> | Table 4          |                  |                  | V <sub>PP</sub>  | V <sub>ILP</sub> | Data Out         |                  |                              |                  |                  |        |  |  |
| Security Bit                                       | Program                       | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub>             | V <sub>ILP</sub> | V <sub>ILP</sub> |        |  |  |
|  | Verify                        | V <sub>ILP</sub> | V <sub>ILP</sub> | Data Out         | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | V <sub>ILP</sub> | Driven Outputs   |                  |                  |                              |                  |                  |        |  |  |
| PAL Mode Operation                                 | Normal                        | CP/I             | I                | I                | I                | I                | I                | I                | I                | I                | I                | I                | I                | I/O              |                  |                  |                              |                  |                  |        |  |  |
|  | Phantom                       | NA               | I                | NA               | NA               | NA               | V <sub>PP</sub>  | I                | NA               | NA               | I                | I                | NA               | Output           |                  |                  |                              |                  |                  |        |  |  |
|  | Top Test                      | I                | I                | I                | I                | I                | I                | I                | I                | V <sub>PP</sub>  | I                | I                | I                | NA               |                  |                  |                              |                  |                  | Out    |  |  |
|  | Bottom Test                   | I                | I                | I                | I                | I                | I                | I                | I                | I                | V <sub>PP</sub>  | I                | I                | Out              | NA               |                  |                              |                  |                  |        |  |  |
|  | Reg Preload                   | Notes            | NA               | NA               | NA               | NA               | NA               | NA               | V <sub>PP</sub>  | NA               | NA               | NA               | V <sub>ILP</sub> | Data In          |                  |                  |                              |                  |                  |        |  |  |
| Phantom Array Product Terms                        | Program                       | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub> | Table 5          |                  |                  | V <sub>ILP</sub> | V <sub>PP</sub>  | Table 3          |                  |                  |                  | V <sub>PP</sub>  | Data In          |                  |                              |                  |                  |        |  |  |
|  | Program Inhibit               | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub> | Table 5          |                  |                  | V <sub>ILP</sub> | V <sub>PP</sub>  | Table 3          |                  |                  |                  | V <sub>IHP</sub> | High Z           |                  |                              |                  |                  |        |  |  |
|  | Program Verify                | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub> | Table 5          |                  |                  | V <sub>ILP</sub> | V <sub>PP</sub>  | Table 3          |                  |                  |                  | V <sub>ILP</sub> | Data Out         |                  |                              |                  |                  |        |  |  |
| Phantom Output Enable Product Terms                | Program                       | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub> | Table 5          |                  |                  | V <sub>ILP</sub> | V <sub>PP</sub>  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>  | V <sub>PP</sub>  | Data In          |                  |                              |                  |                  |        |  |  |
|  | Program Inhibit               | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub> | Table 5          |                  |                  | V <sub>ILP</sub> | V <sub>PP</sub>  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>  | V <sub>IHP</sub> | High Z           |                  |                              |                  |                  |        |  |  |
|  | Program Verify                | V <sub>PP</sub>  | V <sub>ILP</sub> | V <sub>ILP</sub> | Table 5          |                  |                  | V <sub>ILP</sub> | V <sub>PP</sub>  | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>IHP</sub> | V <sub>PP</sub>  | V <sub>ILP</sub> | Data Out         |                  |                              |                  |                  |        |  |  |

Notes:

1. DATA IN and DATA OUT for programming Synchronous Set, Asynchronous Reset, TOP TEST and BOTTOM TEST is programmed and verified on the following pins.

- Pin 14 = BOTTOM TEST
- Pin 17 = Synchronous Set
- Pin 20 = Asynchronous Reset
- Pin 23 = TOP TEST

- 2. The preload clock on pin 1 loads the Registers on a LOW going HIGH transition.
- 3. It is necessary to toggle OE (Pin 13) HIGH during all address transitions while in the program verify/blank check mode.

4

### Input Term Addresses

Table 2 is used during the programming and verification of the main array, output enable, asynchronous reset, synchronous preset, TOP and BOTTOM TEST as shown in Table 1.

It provides the addressing for the 44 normal input term columns which are connected with an EPROM transistor to the product terms.

### Input Term Addresses

Table 2

| Input Term | Pin 2 | Pin 3 | Pin 4 | Pin 5 | Pin 6 | Pin 7 |
|------------|-------|-------|-------|-------|-------|-------|
| 0          | VILP  | VILP  | VILP  | VILP  | VILP  | VILP  |
| 1          | VIHP  | VILP  | VILP  | VILP  | VILP  | VILP  |
| 2          | VILP  | VIHP  | VILP  | VILP  | VILP  | VILP  |
| 3          | VIHP  | VIHP  | VILP  | VILP  | VILP  | VILP  |
| 4          | VILP  | VILP  | VIHP  | VILP  | VILP  | VILP  |
| 5          | VIHP  | VILP  | VIHP  | VILP  | VILP  | VILP  |
| 6          | VILP  | VIHP  | VIHP  | VILP  | VILP  | VILP  |
| 7          | VIHP  | VIHP  | VIHP  | VILP  | VILP  | VILP  |
| 8          | VILP  | VILP  | VILP  | VIHP  | VILP  | VILP  |
| 9          | VIHP  | VILP  | VILP  | VIHP  | VILP  | VILP  |
| 10         | VILP  | VIHP  | VILP  | VIHP  | VILP  | VILP  |
| 11         | VIHP  | VIHP  | VILP  | VIHP  | VILP  | VILP  |
| 12         | VILP  | VILP  | VIHP  | VIHP  | VILP  | VILP  |
| 13         | VIHP  | VILP  | VIHP  | VIHP  | VILP  | VILP  |
| 14         | VILP  | VIHP  | VIHP  | VIHP  | VILP  | VILP  |
| 15         | VIHP  | VIHP  | VIHP  | VIHP  | VILP  | VILP  |
| 16         | VILP  | VILP  | VILP  | VILP  | VIHP  | VILP  |
| 17         | VIHP  | VILP  | VILP  | VILP  | VIHP  | VILP  |
| 18         | VILP  | VIHP  | VILP  | VILP  | VIHP  | VILP  |
| 19         | VIHP  | VIHP  | VILP  | VILP  | VIHP  | VILP  |
| 20         | VILP  | VILP  | VIHP  | VILP  | VIHP  | VILP  |
| 21         | VIHP  | VILP  | VIHP  | VILP  | VIHP  | VILP  |
| 22         | VILP  | VIHP  | VIHP  | VILP  | VIHP  | VILP  |
| 23         | VIHP  | VIHP  | VIHP  | VILP  | VIHP  | VILP  |
| 24         | VILP  | VILP  | VILP  | VIHP  | VIHP  | VILP  |
| 25         | VIHP  | VILP  | VILP  | VIHP  | VIHP  | VILP  |
| 26         | VILP  | VIHP  | VILP  | VIHP  | VIHP  | VILP  |
| 27         | VIHP  | VIHP  | VILP  | VIHP  | VIHP  | VILP  |
| 28         | VILP  | VILP  | VIHP  | VIHP  | VIHP  | VILP  |
| 29         | VIHP  | VILP  | VIHP  | VIHP  | VIHP  | VILP  |
| 30         | VILP  | VIHP  | VIHP  | VIHP  | VIHP  | VILP  |
| 31         | VIHP  | VIHP  | VIHP  | VIHP  | VIHP  | VILP  |
| 32         | VILP  | VILP  | VILP  | VILP  | VILP  | VIHP  |
| 33         | VIHP  | VILP  | VILP  | VILP  | VILP  | VIHP  |
| 34         | VILP  | VIHP  | VILP  | VILP  | VILP  | VIHP  |
| 35         | VIHP  | VIHP  | VILP  | VILP  | VILP  | VIHP  |
| 36         | VILP  | VILP  | VIHP  | VILP  | VILP  | VIHP  |
| 37         | VIHP  | VILP  | VIHP  | VILP  | VILP  | VIHP  |
| 38         | VILP  | VIHP  | VIHP  | VILP  | VILP  | VIHP  |
| 39         | VIHP  | VIHP  | VIHP  | VILP  | VILP  | VIHP  |
| 40         | VILP  | VILP  | VILP  | VIHP  | VILP  | VIHP  |
| 41         | VIHP  | VILP  | VILP  | VIHP  | VILP  | VIHP  |
| 42         | VILP  | VIHP  | VILP  | VIHP  | VILP  | VIHP  |
| 43         | VIHP  | VIHP  | VILP  | VIHP  | VILP  | VIHP  |

## Product Term Addresses

Table 3 is used for the programming of the "PHANTOM" and normal array. It provides the addressing for the up to 16 product terms associated with each input. Notice that the number of product terms varies from 8 to 16 and back to 8 from the top to the bottom output. In Table 3, product term "0" refers to the top product term associated with the MACROCELLS on pins 18 and 19, while address 15 refers to the bottom or last product term associated with the same pins. In the same manner, the 8 product terms associated with pins 14 and 23 are addressed as "0" through "7". The balance of the product terms associated with the remaining I/O pins are addressed as "0" through "10", "12" and "14".

## Product Term Addresses

**Table 3**

| Product Term | Pin 8 | Pin 9 | Pin 10 | Pin 11 |
|--------------|-------|-------|--------|--------|
| 0            | VILP  | VILP  | VILP   | VILP   |
| 1            | VIHP  | VILP  | VILP   | VILP   |
| 2            | VILP  | VIHP  | VILP   | VILP   |
| 3            | VIHP  | VIHP  | VILP   | VILP   |
| 4            | VILP  | VILP  | VIHP   | VILP   |
| 5            | VIHP  | VILP  | VIHP   | VILP   |
| 6            | VILP  | VIHP  | VIHP   | VILP   |
| 7            | VIHP  | VIHP  | VIHP   | VILP   |
| 8            | VILP  | VILP  | VILP   | VIHP   |
| 9            | VIHP  | VILP  | VILP   | VIHP   |
| 10           | VILP  | VIHP  | VILP   | VIHP   |
| 11           | VIHP  | VIHP  | VILP   | VIHP   |
| 12           | VILP  | VILP  | VIHP   | VIHP   |
| 13           | VIHP  | VILP  | VIHP   | VIHP   |
| 14           | VILP  | VIHP  | VIHP   | VIHP   |
| 15           | VIHP  | VIHP  | VIHP   | VIHP   |

## Architecture Bit Addressing

Table 4 provides the addressing for the architecture bits used to control the configuration of the individual MACROCELLS. In the unprogrammed state, the MACROCELLS are in a registered, active low or inverting configuration. They are programmed with a "1" on the pin associated with the MACROCELL and the appropriate address as shown in Table 4. Each architecture bit that is not to be programmed, requires a "0" on the I/O pin associated with the MACROCELL.

## Architecture Bit Addressing

**Table 4**

| Architecture Bit                | Pin 9 | Pin 10 |
|---------------------------------|-------|--------|
| Output Polarity C0              | VILP  | VILP   |
| Register/Non-Register Output C1 | VIHP  | VILP   |

## Phantom Input Term Addressing

Phantom input terms are addressed as columns P0 thru P3 and represent inputs from pins 2, 7, 10 and 11 respectively. Pin 7 is inverted, and the remaining 3 are normal non-inverting. This PHANTOM array allows the output structures to be tested. They are only present in PHANTOM modes of operation.

## Phantom Input Term Addresses

**Table 5**

| Phantom Input Term | Pin 4 | Pin 5 |
|--------------------|-------|-------|
| P0                 | VILP  | VILP  |
| P1                 | VIHP  | VILP  |
| P2                 | VILP  | VIHP  |
| P3                 | VIHP  | VIHP  |

## Programming Flow Chart

The programming flow chart describes the sequence of operations for programming the NORMAL and PHANTOM arrays, the NORMAL and PHANTOM output enable product terms, the set and preset product terms, the Top Test product term, the Bottom Test product term, and the architecture bits. The exact sequencing and timing of the signals is shown in the "Array Programming Timing Diagram".

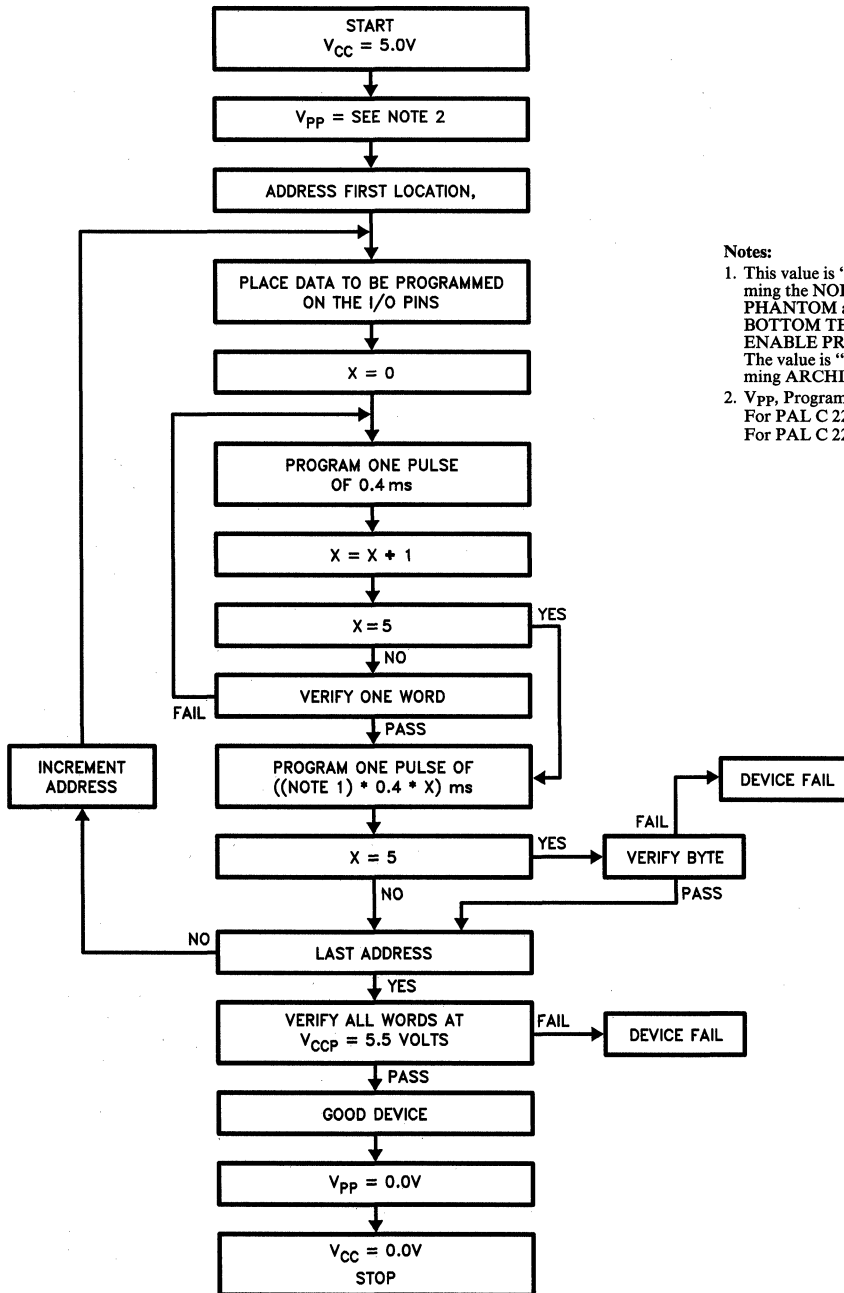
The logical sequence to program the device is described in detail in the flow chart below, and should be followed exactly for optimum intelligent programming that both minimizes programming time and realizes reliable programming. Particular attention should be paid to the application of  $V_{CC}$  prior to  $V_{pp}$ , and removal of  $V_{pp}$  prior to  $V_{CC}$ . See Figure 8 and Table 7 for specific timing and AC requirements. Notice that all programming is accomplished without switching  $V_{pp}$  on pin 1 and that after programming and verifying all locations individually, the programmed locations should be verified one final time.

The normal word programming cycle, programs and verifies a word at a time as shown in the programming flowchart, Figure 7 and timing diagram Figure 8. After all locations are programmed, the flowchart requires a verify of all words. There is no independent timing diagram for this operation, rather Figure 8 also provides the correct timing information for this operation. When performing this verify only operation, eliminate the program portion of the cycle but maintain the setup and hold timing relative to the verify pulse. Under no circumstances should the verify signal be held low and the addresses toggled.

Note that the overprogram pulse in step 10 of the programming flowchart is a variable, "4" times the initial value when programming the NORMAL, PHANTOM, TOP TEST, BOTTOM TEST and OUTPUT ENABLE product terms and "8" times the initial value when programming the ARCHITECTURE BITS.



Programming Flowchart



Notes:

1. This value is "4" for programming the NORMAL array, PHANTOM array TOP TEST, BOTTOM TEST and OUTPUT ENABLE PRODUCT TERMS. The value is "8" when programming ARCHITECTURE BITS.
2. V<sub>pp</sub>, Programming Voltage:  
For PAL C 22V10B = 12.5V  
For PAL C 22V10 = 13.5V

Figure 7

## Timing Diagrams

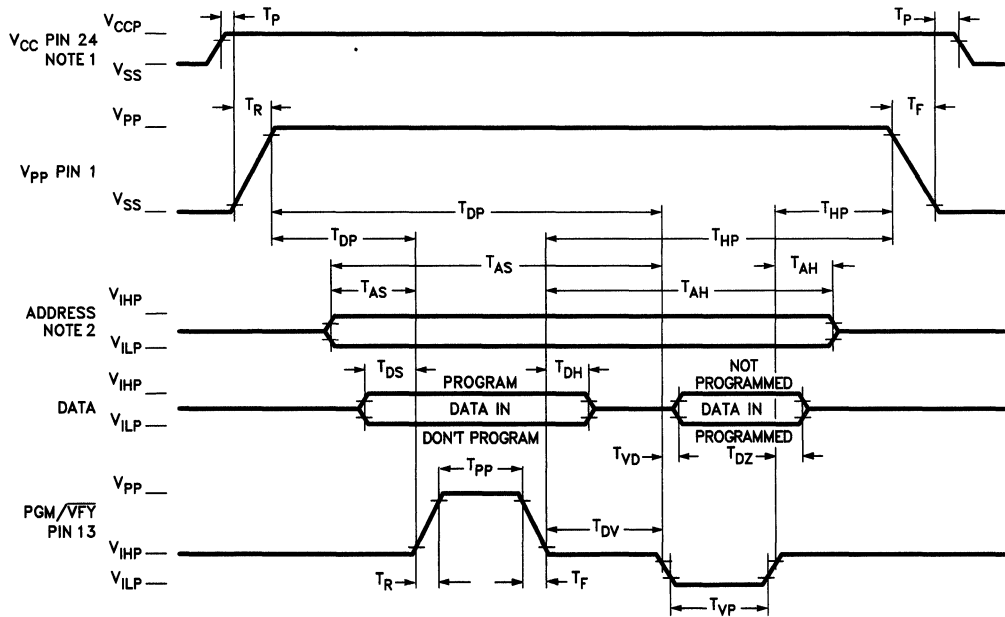
Programming timing diagrams are provided for two cases, programming of all cells except the SECURITY BIT and programming the SECURITY BIT.

### Array

Programming the NORMAL and PHANTOM arrays and output enables, reset, preset, architecture bits and the top/bottom test features uses the timing diagram in *Figure 8*. ADDRESS refers to all applicable information in Tables 1 through 5 that is not specifically referenced in the timing diagram. DATA IN is provided on the I/O pins and

DATA OUT is verified on the same pins. A "1" ( $V_{IHP}$ ) on an I/O pin causes the addressed location to be programmed. A "0" on the I/O pin leaves the addressed location to be unprogrammed. All setup hold and delay times must be met, and in particular the sequence of operations should be strictly followed. During verify only operation it is not acceptable to hold PGM/VFY low and sequence addresses, as it violates address setup and hold times. Proper sequencing of all power and supervoltages is essential, to reliable programming of the device as improper sequencing could result in device damage.

### Programming Waveforms



#### Notes:

1. Power,  $V_{pp}$  &  $V_{CC}$  should not be cycled for each program/verify cycle, but may remain static during programming.

2. For programming OE Product Terms & Architecture bits, Pin 11 (A9) must go to  $V_{pp}$  and satisfy  $T_{AS}$  and  $T_{AN}$ .

Figure 8

0023-8

## Security Cell

The security cell is programmed independently per the timing diagram in *Figure 9*, and the information in Table 1. Note again that proper sequencing of power and programming signals is required. Data in is represented as a supervoltage on pin 3 and verified as a TTL signal output on the

same pin. A "0" on pin 3 indicates that the security bit has been programmed, and a "1" indicates that security bit has not been programmed. Security is programmed with a single 50 ms pulse on pin 13. A supervoltage on pin 4 is used to verify security after  $V_{PP}$  has been removed from pin 1.

## Programming Waveforms Security Cell

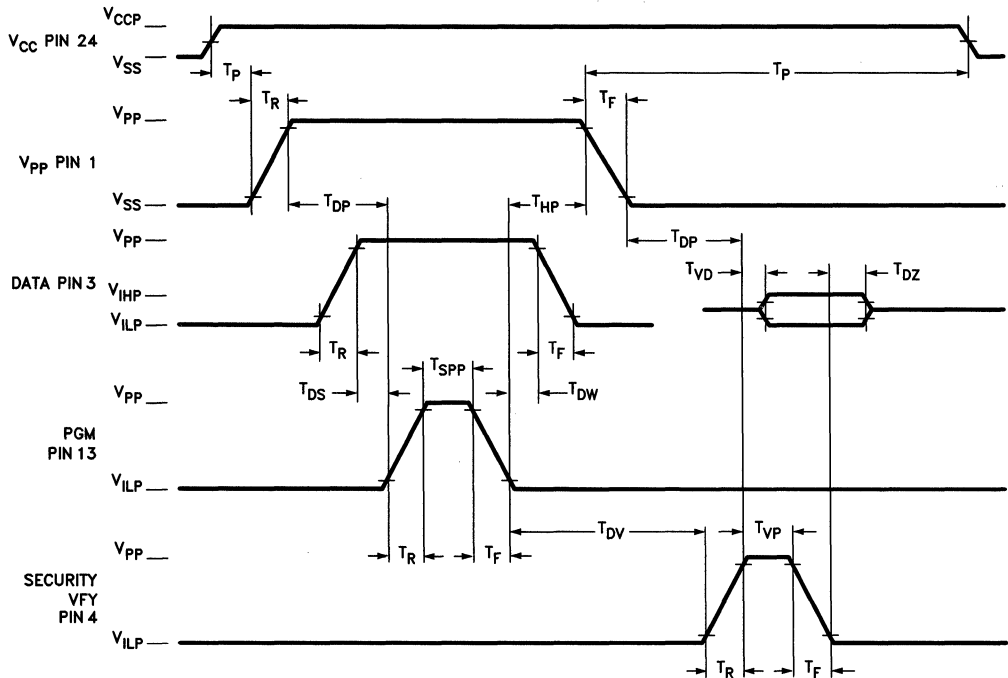


Figure 9

0023-9

**DC Programming Parameters**  $T_A = 25^\circ\text{C}$ 
**Table 6**

| Parameter                        | Description                              | Min. | Max.             | Units |
|----------------------------------|--|------|------------------|-------|
| V <sub>PP</sub> for PAL C 22V10B | Programming Voltage                      | 12.0 | 13.0             | Volts |
| V <sub>PP</sub> for PAL C 22V10  | Programming Voltage                      | 13.0 | 14.0             | Volts |
| V <sub>CCP</sub>                 | Supply Voltage<br>During Programming     | 4.75 | 5.25             | Volts |
| V <sub>IHP</sub>                 | Input HIGH Voltage<br>During Programming | 3.0  | V <sub>CCP</sub> | Volts |
| V <sub>ILP</sub>                 | Input LOW Voltage<br>During Programming  | -3.0 | 0.4              | Volts |
| V <sub>OH</sub>                  | Output HIGH Voltage                      | 2.4  |                  | Volts |
| V <sub>OL</sub>                  | Output LOW Voltage                       |      | 0.4              | Volts |
| I <sub>PP</sub>                  | Programming<br>Supply Current            |      | 40               | mA    |

**AC Programming Parameters**
**Table 7**

| Parameter        | Description                            | Min. | Max. | Units |
|------------------|--|------|------|-------|
| T <sub>P</sub>   | Delay to Programming<br>Voltage        | 20   |      | ms    |
| T <sub>DP</sub>  | Delay to Program                       | 1    |      | μs    |
| T <sub>HP</sub>  | Hold from Program<br>or Verify         | 1    |      | μs    |
| T <sub>R,F</sub> | V <sub>PP</sub> Rise & Fall Time       | 50   |      | ns    |
| T <sub>AS</sub>  | Address Setup Time                     | 1    |      | μs    |
| T <sub>AH</sub>  | Address Hold Time                      | 1    |      | μs    |
| T <sub>DS</sub>  | Data Setup Time                        | 1    |      | μs    |
| T <sub>DH</sub>  | Data Hold Time                         | 1    |      | μs    |
| T <sub>PP</sub>  | Programming Pulsewidth                 | 0.4  | 10   | ms    |
| T <sub>SPP</sub> | Programming Pulsewidth<br>for Security | 50   |      | ms    |
| T <sub>DV</sub>  | Delay from Program<br>to Verify        | 2    |      | μs    |
| T <sub>VD</sub>  | Delay to Data Out                      |      | 1    | μs    |
| T <sub>VP</sub>  | Verify Pulse Width                     | 2    |      | μs    |
| T <sub>DZ</sub>  | Verify to High Z                       |      | 1    | μs    |

**Ordering Information**

| I <sub>CC</sub><br>(mA) | t <sub>PD</sub><br>(ns) | t <sub>S</sub><br>(ns) | t <sub>CO</sub><br>(ns) | Ordering Code        | Package | Operating Range       |
|-------------------------|-------------------------|------------------------|-------------------------|----------------------|---------|-----------------------|
| 90                      | 15                      | 10                     | 10                      | PAL C 22V10B-15PC/PI | P13     | Commercial/Industrial |
|                         |                         |                        |                         | PAL C 22V10B-15WC/WI | W14     |                       |
|                         |                         |                        |                         | PAL C 22V10B-15JC/JI | J64     |                       |
| 90                      | 20                      | 12                     | 12                      | PAL C 22V10-20PC/PI  | P13     | Commercial/Industrial |
|                         |                         |                        |                         | PAL C 22V10-20WC/WI  | W14     |                       |
|                         |                         |                        |                         | PAL C 22V10-20JC/JI  | J64     |                       |
| 120                     | 20                      | 17                     | 15                      | PAL C 22V10B-20DMB   | D14     | Military              |
|                         |                         |                        |                         | PAL C 22V10B-20WMB   | W14     |                       |
|                         |                         |                        |                         | PAL C 22V10B-20LMB   | L64     |                       |
|                         |                         |                        |                         | PAL C 22V10B-20QMB   | Q64     |                       |
|                         |                         |                        |                         | PAL C 22V10B-20KMB   | K73     |                       |
| 55                      | 25                      | 15                     | 15                      | PAL C 22V10L-25PC    | P13     | Commercial            |
|                         |                         |                        |                         | PAL C 22V10L-25WC    | W14     |                       |
|                         |                         |                        |                         | PAL C 22V10L-25JC    | J64     |                       |
| 90                      | 25                      | 15                     | 15                      | PAL C 22V10-25PC/PI  | P13     | Commercial/Industrial |
|                         |                         |                        |                         | PAL C 22V10-25WC/WI  | W14     |                       |
|                         |                         |                        |                         | PAL C 22V10-25JC/JI  | J64     |                       |
| 100                     | 25                      | 18                     | 15                      | PAL C 22V10-25DMB    | D14     | Military              |
|                         |                         |                        |                         | PAL C 22V10-25WMB    | W14     |                       |
|                         |                         |                        |                         | PAL C 22V10-25LMB    | L64     |                       |
|                         |                         |                        |                         | PAL C 22V10-25QMB    | Q64     |                       |
|                         |                         |                        |                         | PAL C 22V10-25KMB    | K73     |                       |
| 100                     | 30                      | 20                     | 20                      | PAL C 22V10-30DMB    | D14     | Military              |
|                         |                         |                        |                         | PAL C 22V10-30WMB    | W14     |                       |
|                         |                         |                        |                         | PAL C 22V10-30LMB    | L64     |                       |
|                         |                         |                        |                         | PAL C 22V10-30QMB    | Q64     |                       |
|                         |                         |                        |                         | PAL C 22V10-30KMB    | K73     |                       |
| 55                      | 35                      | 30                     | 25                      | PAL C 22V10L-35PC    | P13     | Commercial            |
|                         |                         |                        |                         | PAL C 22V10L-35WC    | W14     |                       |
|                         |                         |                        |                         | PAL C 22V10L-35JC    | J64     |                       |
| 90                      | 35                      | 30                     | 25                      | PAL C 22V10-35PC/PI  | P13     | Commercial/Industrial |
|                         |                         |                        |                         | PAL C 22V10-35WC/WI  | W14     |                       |
|                         |                         |                        |                         | PAL C 22V10-35JC/JI  | J64     |                       |
| 100                     | 40                      | 30                     | 25                      | PAL C 22V10-40DMB    | D14     | Military              |
|                         |                         |                        |                         | PAL C 22V10-40WMB    | W14     |                       |
|                         |                         |                        |                         | PAL C 22V10-40LMB    | L64     |                       |
|                         |                         |                        |                         | PAL C 22V10-40QMB    | Q64     |                       |
|                         |                         |                        |                         | PAL C 22V10-40KMB    | K73     |                       |

**MILITARY SPECIFICATIONS****Group A Subgroup Testing****DC Characteristics**

| Parameters      | Subgroups |
|-----------------|-----------|
| V <sub>OH</sub> | 1,2,3     |
| V <sub>OL</sub> | 1,2,3     |
| V <sub>IH</sub> | 1,2,3     |
| V <sub>IL</sub> | 1,2,3     |
| I <sub>Ix</sub> | 1,2,3     |
| I <sub>OZ</sub> | 1,2,3     |
| I <sub>CC</sub> | 1,2,3     |

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**Switching Characteristics**

| Parameters      | Subgroups   |
|-----------------|-------------|
| t <sub>PD</sub> | 7,8,9,10,11 |
| t <sub>CO</sub> | 7,8,9,10,11 |
| t <sub>S</sub>  | 7,8,9,10,11 |
| t <sub>H</sub>  | 7,8,9,10,11 |
| t <sub>W</sub>  | 7,8,9,10,11 |

Document #: 38-00020-C



# CMOS Programmable Synchronous State Machine

## Features

- 12 I/O macro cells each having:
  - registered, three-state I/O pins
  - input register clock select multiplexer
  - feed back multiplexer
  - output enable (OE) multiplexer
- All twelve macro cell state registers can be hidden
- User configurable state registers—JK, RS, T, or D
- Input multiplexer per pair of I/O macro cells allows I/O pin associated with a hidden macro cell state register to be saved for use as an input
- 4 dedicated hidden registers
- 11 dedicated, registered inputs
- 3 separate clocks—2 inputs, 1 output
- Common (PIN 14 controlled) or product term controlled output enable for each I/O pin
- 256 product terms—32 per pair of macro cells, variable distribution
- Global, synchronous, product term controlled, state register set and reset—inputs to product term are clocked by input clock
- 66 MHz operation
  - 3 ns input setup and 12 ns clock to output
  - 15 ns input register clock to state register clock
- Low power
  - 130 mA I<sub>CC</sub>
- 28 pin 300 mil DIP, LCC
- Erasable and reprogrammable

## Product Characteristics

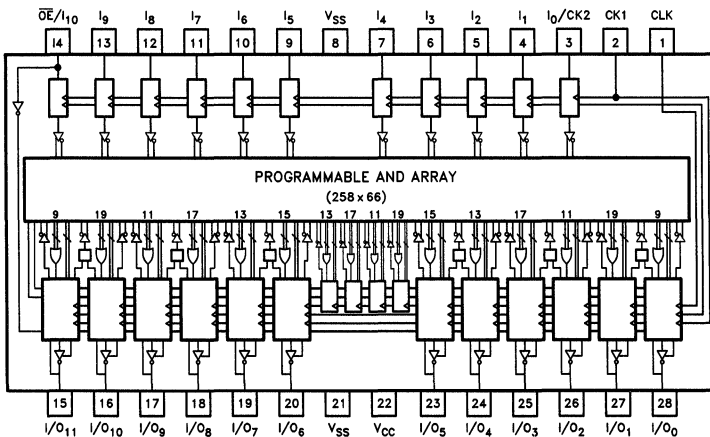
The CY7C330 is a high-performance, erasable, programmable, logic device (EPLD) whose architecture has been optimized to enable the user to easily and efficiently construct very high performance synchronous state machines.

The unique architecture of the CY7C330, consisting of the user-configurable output macrocell, bi-directional I/O capability, input registers, and three separate clocks, enables the user to design high performance state machines that can communicate either with each other or with microprocessors over bi-directional parallel busses of user-definable widths.

The three separate clocks permit independent, synchronous state machines to be synchronized to each other. The two input clocks, C1, C2, enable the state machine to sample input signals that may be generated by another system and that may be available on its bus for a short period of time.

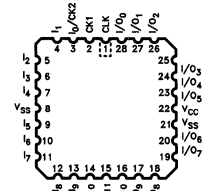
The user-configurable state register flip-flops enable the designer to designate JK, RS, T, or D type devices, so that the number of product terms required to implement the logic is minimized.

## Block Diagram and DIP Pinout



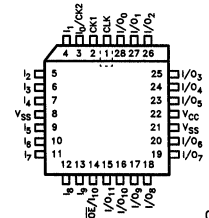
0101-1

## LCC Pinout



0101-14

## PLCC Pinout



0101-15

## Selection Guide

|  |            | CY7C330-66 | CY7C330-50 | CY7C330-40 | CY7C330-33 | CY7C330-28 |
|--|------------|------------|------------|------------|------------|------------|
| Maximum Operating Frequency (MHz)          | Commercial | 66.6       | 50.0       |            | 33.3       |            |
|  | Military   |            | 50.0       | 40.0       |            | 28.5       |
| Power Supply Current I <sub>CC1</sub> (mA) | Commercial | 130        | 130        |            | 130        |            |
|  | Military   |            | 150        | 150        |            | 150        |

## Product Characteristics (Continued)

The major functional blocks of the CY7C330 are (1) the input registers and (input) clock multiplexers, (2) the EPROM (AND) cell array, (3) the twelve I/O macrocells and (4) the four hidden registers.

### Input Registers and Clock Multiplexers

There are a total of eleven dedicated Input Registers. Each Input Register consists of a D flip-flop and a clock multiplexer. The clock multiplexer is user-programmable to select either CK1 or CK2 as the clock for the flip-flop. CK2 and  $\overline{OE}$  can alternatively be used as inputs to the array. The twenty-two outputs of the registers (i.e. the Q and  $\overline{Q}$  outputs of the input registers) drive the array of EPROM cells.

An architecture configuration bit (C4) is reserved for each Dedicated Input Register cell to allow selection of either input clock CK1 or CK2 as the input register clock for each Dedicated Input Cell. If the CK2 clock is not needed that input may also be used as a general purpose array input. In this case the Input Register for this input can only be clocked by input clock CK1. *Figure 1* illustrates the Dedicated Input Cell composed of input register, Input Clock Multiplexer, and architecture configuration bit C4 which determines the input clock selected.

### I/O Macro Cell

The logic diagram of the CY7C330 I/O macro cell is shown in *Figure 2*. There are a total of twelve identical macro cells.

Each macro cell consists of:

- An Output State Register which is clocked by the global state counter clock, CLK (PIN 1). The State Register can be configured as a D, JK, RS, or T flip-flop (default is a D-type flip-flop). Polarity can be controlled in the D flip-flop implementation by use of the exclusive or function. Data is sampled on the LOW to HIGH clock transition. All of the State Registers have a common reset and set which are controlled synchronously by Product Terms which are generated in the EPROM cell array.
- A Macro Cell Input Register which may be clocked by either the CK1 or CK2 input clock as programmed by the user by use of architecture configuration bit C2 which controls the I/O Macro Cell Input Clock Multiplexer. The Macro Cell Input Registers are initialized on power up such that all of the Q outputs are at logic LOW level and the  $\overline{Q}$  outputs are at a logic HIGH level.
- An Output Enable Multiplexer (OE), which is user-programmable, by architecture configuration bit C0, to select either the common  $\overline{OE}$  signal from pin 14 or, for each cell individually, the signal from the Output Enable product term associated with each macro cell. The Output Enable input signal to the array product term is clocked through the input register by the selected input register clock, CK1 or CK2.
- An input Feed Back Multiplexer which is user-programmable to select either the output of the State Register or the output of the Macro Cell Input Register to be fed back into the array. This option is programmed by architecture configuration bit C1. If the output of the Macro Cell Input Register is selected by the Feed Back Multiplexer, the I/O pin becomes bi-directional.

### Macro Cell Input Multiplexer

Each pair of I/O macro cells share a Macro Cell Input Multiplexer which selects the output of one or the other of the pair's input registers to be fed to the input array. This multiplexer is shown in *Figure 2*. The Macro Cell Input Multiplexer allows the input pin of a macro cell, for which the state register has been hidden by feeding back its input to the input array, to be preserved for use as an input pin. This is possible as long as the other macro cell of the pair is not needed as an input or does not require State Register feed back. The input pin input register output which would normally be blocked by the hidden State Register feed back can be routed to the array input path of the companion macro cell for use as array input.

### State Registers

By use of the exclusive or gate the State Register may be configured as a JK, RS or T Register. The default is a D-Type register. For the D-Type register, the exclusive or function can be used to select the polarity or the register output.

The set and reset of the State Register are global synchronous signals which are controlled by the logic of two global product terms for which input signals are clocked through the input registers by either of the input clocks, CK1 or CK2.

### Hidden Registers

In addition to the twelve macro cells, which contain a total of twenty-four registers, there are four hidden registers whose outputs are not brought out to the device output pins. The Hidden State Register Macro Cell is shown in *Figure 3*.

The four hidden registers are clocked by the same clock as the macrocell state registers. All of the hidden register flip-flops have a common, synchronous set, S, as well as a common, synchronous reset, R, which over-ride the data at the D input. The S and R signals are PRODUCT TERMS that are generated in the array and are the same signals used to preset and reset the state register flip-flops.

### Macrocell Product Term Distribution

Each pair of macrocells has a total of thirty-two product terms. Two product terms of each macrocell pair are used for the output enables (OEs) for the two output pins. Two product terms are also used as one input to each of the two exclusive OR gates in the macrocell pair. The number of product terms available to the designer is then  $32 - 4 = 28$  for each macrocell pair. These product terms are divided between the macro cell state register flip-flops as shown in Table 1.

**Table 1. Product Term Distribution**

| Macro Cell | Pin No. | Product Terms |
|------------|---------|---------------|
| 0          | 28      | 9             |
| 1          | 27      | 19            |
| 2          | 26      | 11            |
| 3          | 25      | 17            |
| 4          | 24      | 13            |
| 5          | 23      | 15            |
| 6          | 20      | 15            |
| 7          | 19      | 13            |
| 8          | 18      | 17            |
| 9          | 17      | 11            |
| 10         | 16      | 19            |
| 11         | 15      | 9             |



**Product Characteristics (Continued)**
**Hidden State Register Product Term Distribution**

Each pair of hidden registers also has a total of 32 product terms. Two product terms are used as one input to each of the exclusive OR gates. However, because the register outputs do not go to any output pins, output enable product terms are not required. Therefore, 30 product terms are available to the designer for each pair of hidden registers. The product term distribution for the four hidden registers are shown in Table 2.

**Table 2. Hidden State Register Product Term Distribution**

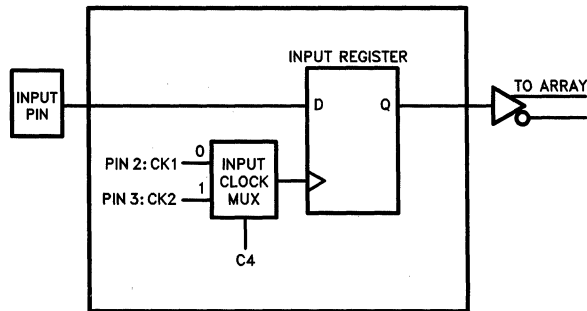
| Hidden Register Cell | Product Terms |
|----------------------|---------------|
| 0                    | 19            |
| 1                    | 11            |
| 2                    | 17            |
| 3                    | 13            |

**Architecture Configuration Bits**

The architecture configuration bits are used to program the multiplexers. The function of the architecture bits is outlined below.

**Table 3. Architecture Configuration Bits**

| Architecture Configuration Bit | Number of Bits                      | Value          | Function   |
|--------------------------------|-------------------------------------|----------------|--|
| C0                             | 12 Bits, 1 Per I/O Macro Cell       | 0—Virgin State | Output Enable Controlled by Product Term   |
|                                |                                     | 1—Programmed   | Output Enable Controlled by Pin 14   |
| C1                             | 12 Bits, 1 Per I/O Macro Cell       | 0—Virgin State | State Register Output is Fed Back to Input Array   |
|                                |                                     | 1—Programmed   | I/O Macro Cell is Configured as an Input and Output of Input Register is Fed to Array      |
| C2                             | 12 Bits, 1 Per I/O Macro Cell       | 0—Virgin State | CK1 Input Register Clock (Pin 2) is Connected to I/O Macro Cell Input Register Clock Input |
|                                |                                     | 1—Programmed   | CK2 Input Register Clock (Pin 3) is Connected to I/O Macro Cell Input Register Clock Input |
| C3                             | 6 Bits, 1 Per I/O Macro Cell Pair   | 0—Virgin State | Selects Data from I/O Macro Cell Input Register of Macro Cell A of Macro Cell Pair         |
|                                |                                     | 1—Programmed   | Selects Data from I/O Macro Cell Input Register of Macro Cell B of Macro Cell Pair         |
| C4                             | 11 Bits, 1 Per Dedicated Input Cell | 0—Virgin State | CK1 Input Register Clock (Pin 2) is Connected to Dedicated Input Register Clock Input      |
|                                |                                     | 1—Programmed   | CK2 Input Register Clock (Pin 3) is Connected to Dedicated Input Register Clock Input      |


**Figure 1. Dedicated Input Cell**

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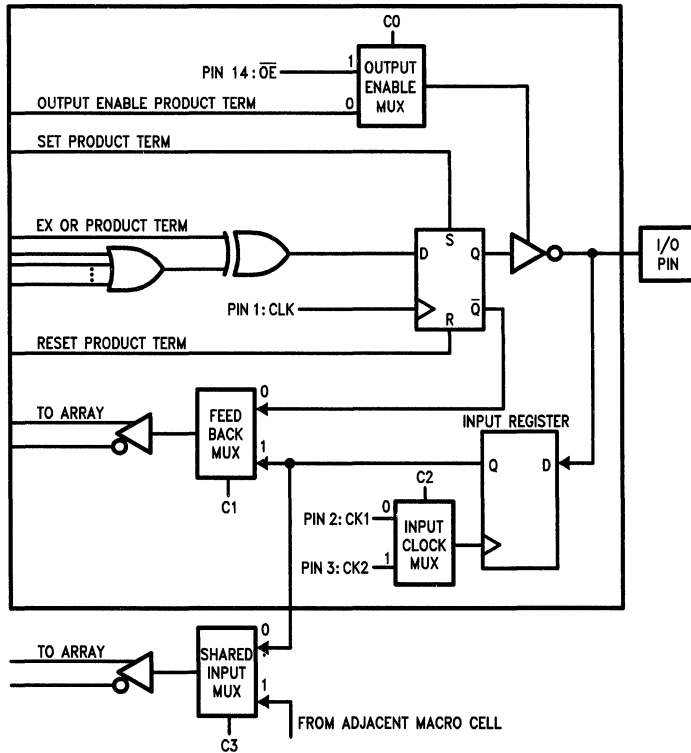


Figure 2. I/O Macro Cell and Shared Input Multiplexer

0101-6

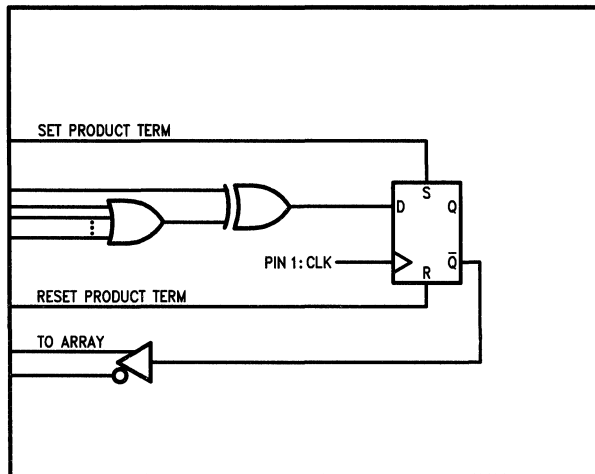


Figure 3. Hidden State Register Macro Cell

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## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|  |                 |
|--|-----------------|
| Storage Temperature .....  | -65°C to +150°C |
| Ambient Temperature with Power Applied .....                       | -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 22 to Pins 8 and 21) ..... | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State .....                | -0.5V to +7.0V  |
| DC Input Voltage .....   | -3.0V to +7.0V  |
| Output Current into Outputs (Low) .....                            | 12 mA           |

|                                |                                       |
|--------------------------------|---------------------------------------|
| Static Discharge Voltage ..... | > 2001V (per MIL-STD-883 Method 3015) |
| Latchup Current .....          | > 200 mA                              |
| DC Programming Voltage .....   | 13.0V                                 |

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +75°C        | 5V ± 10%        |
| Military <sup>[5]</sup> | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over Operating Range<sup>[6]</sup>

| Parameters       | Description  | Test Conditions   |                                 | Min.  | Max. | Units |
|------------------|--|---|---------------------------------|-------|------|-------|
|                  |  |   |                                 |       |      |       |
| V <sub>OH</sub>  | Output HIGH Voltage                                | V <sub>CC</sub> = Min.,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   | I <sub>OH</sub> = -3.2 mA       | COM'L | 2.4  | V     |
|                  |  |   | I <sub>OH</sub> = -2 mA         | MIL   |      |       |
| V <sub>OL</sub>  | Output LOW Voltage                                 | V <sub>CC</sub> = Min.,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   | I <sub>OL</sub> = 12 mA         | COM'L | 0.5  | V     |
|                  |  |   | I <sub>OL</sub> = 8 mA          | MIL   |      |       |
| V <sub>IH</sub>  | Input HIGH Level                                   | Guaranteed Input Logical HIGH Voltage for All Inputs <sup>[1]</sup>   |                                 | 2.2   |      | V     |
| V <sub>IL</sub>  | Input LOW Level                                    | Guaranteed Input Logical LOW Voltage for All Inputs <sup>[1]</sup>  |                                 |       | 0.8  | V     |
| I <sub>IX</sub>  | Input Leakage Current                              | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> , V <sub>CC</sub> = Max.  |                                 | -10   | 10   | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                             | V <sub>CC</sub> = Max. V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>   |                                 | -40   | 40   | μA    |
| I <sub>SC</sub>  | Output Short Circuit Current                       | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V <sup>[2]</sup>  |                                 | -30   | -90  | mA    |
| I <sub>CC1</sub> | Standby Power Supply Current                       | V <sub>CC</sub> = Max., V <sub>IN</sub> = GND<br>Outputs Open   | COM'L                           |       | 130  | mA    |
|                  |  |   | MIL                             |       | 150  | mA    |
| I <sub>CC2</sub> | Power Supply Current at Frequency <sup>[3,7]</sup> | V <sub>CC</sub> = Max.<br>Outputs Disabled (in High Z State)<br>Device Operating at f <sub>MAX</sub><br>External (f <sub>MAX1</sub> ) | COM'L (-33 MHz & -50 MHz)       |       | 160  | mA    |
|                  |  |   | COM'L (-66 MHz) <sup>[15]</sup> |       | 180  | mA    |
|                  |  |   | MIL (-28 MHz & -40 MHz)         |       | 180  | mA    |
|                  |  |   | MIL (-50 MHz) <sup>[15]</sup>   |       | 200  | mA    |

## Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions                     | Min | Max | Units |
|------------------|--------------------|-------------------------------------|-----|-----|-------|
| C <sub>IN</sub>  | Input Capacitance  | V <sub>IN</sub> = 2.0V @ f = 1 MHz  |     | 7   | pF    |
| C <sub>OUT</sub> | Output Capacitance | V <sub>OUT</sub> = 2.0V @ f = 1 MHz |     | 8   |       |

### Notes:

- These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V<sub>OUT</sub> = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.
- Figure 4a test load used for all parameters except t<sub>CEA</sub>, t<sub>CER</sub>, t<sub>PZX</sub> and t<sub>PKZ</sub>. Figure 4b test load for t<sub>CEA</sub>, t<sub>CER</sub>, t<sub>PZX</sub>, t<sub>PKZ</sub>.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- This parameter is sample tested periodically.
- This parameter is measured as the time after output register disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous high level has fallen to 0.5V below V<sub>OH</sub> Min or a previous low level has risen to 0.5V above V<sub>OL</sub> Max. Please see Figure 6 for enable and disable test waveforms and measurement reference levels.
- This parameter is measured as the time after output register clock input that the previous output data state remains stable on the output.
- This difference parameter is designed to guarantee that any CY7C330 output fed back to its own inputs externally or internally will satisfy the input register minimum input hold time. This parameter is guaranteed for a given individual device and is tested by a periodic sampling of production product.
- This specification is intended to guarantee feeding of this signal to another 33X family input register cycled by the same clock with sufficient output data stable time to insure that the input hold time minimum of the following input register is satisfied. This parameter difference specification is guaranteed by periodic sampling of production product of CYC330 and CY7C332. This difference parameter is guaranteed to be met only for devices at the same ambient temperature and V<sub>CC</sub> supply voltage.
- This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feed back can operate.
- This specification indicates the guaranteed maximum frequency at which an individual input or output register can be cycled.
- This specification indicates the guaranteed maximum frequency at which a state machine configuration with only internal feedback can operate. This parameter tested periodically on a sample basis.
- Preliminary specifications.

**Switching Characteristics Over the Operating Range<sup>[4, 6]</sup>**

| Parameters                            | Description   | Commercial          |      |      |      |      |      | Military            |      |      |      |      |      | Units |
|---------------------------------------|---|---------------------|------|------|------|------|------|---------------------|------|------|------|------|------|-------|
|                                       |   | -66 <sup>[15]</sup> |      | -50  |      | -33  |      | -50 <sup>[15]</sup> |      | -40  |      | -28  |      |       |
|                                       |   | Min.                | Max. | Min. | Max. | Min. | Max. | Min.                | Max. | Min. | Max. | Min. | Max. |       |
| t <sub>IS</sub>                       | Input or Feedback Setup Time to Input Register Clock  | 3                   |      | 5    |      | 10   |      | 5                   |      | 5    |      | 10   |      | ns    |
| t <sub>OS</sub>                       | Input Register Clock to Output Register Clock   | 15                  |      | 20   |      | 30   |      | 20                  |      | 25   |      | 35   |      | ns    |
| t <sub>CO</sub>                       | Output Register Clock to Output Delay   |                     | 12   |      | 15   |      | 20   |                     | 15   |      | 20   |      | 25   | ns    |
| t <sub>IH</sub>                       | Input Register Hold Time  | 5                   |      | 5    |      | 5    |      | 5                   |      | 5    |      | 5    |      | ns    |
| t <sub>CEA</sub>                      | Input Register Clock To Output Enable Delay   |                     | 15   |      | 20   |      | 30   |                     | 20   |      | 25   |      | 35   | ns    |
| t <sub>CER</sub>                      | Input Register Clock to Output Disable Delay <sup>[8]</sup>                                 |                     | 15   |      | 20   |      | 30   |                     | 20   |      | 25   |      | 35   | ns    |
| t <sub>PZX</sub>                      | Pin 14 Enable to Output Enable Delay  |                     | 15   |      | 20   |      | 30   |                     | 20   |      | 25   |      | 35   | ns    |
| t <sub>PXZ</sub>                      | Pin 14 Disable to Output Disable Delay <sup>[8]</sup>                                       |                     | 15   |      | 20   |      | 30   |                     | 20   |      | 25   |      | 35   | ns    |
| t <sub>WH</sub>                       | Input or Output Clock Width High <sup>[3, 7]</sup>  | 6                   |      | 8    |      | 12   |      | 8                   |      | 10   |      | 15   |      | ns    |
| t <sub>WL</sub>                       | Input or Output Clock Width Low <sup>[3, 7]</sup>   | 6                   |      | 8    |      | 12   |      | 8                   |      | 10   |      | 15   |      | ns    |
| t <sub>P</sub>                        | External Clock Period (t <sub>CO</sub> + t <sub>IS</sub> )<br>Input and Output Clock Common | 15                  |      | 20   |      | 30   |      | 20                  |      | 25   |      | 35   |      | ns    |
| t <sub>OH</sub>                       | Output Data Stable Time from Synchronous Clock Input <sup>[9]</sup>                         | 3                   |      | 3    |      | 3    |      | 3                   |      | 3    |      | 3    |      | ns    |
| t <sub>OH</sub> - t <sub>IH</sub>     | Output Data Stable Time This Device Minus I/P Reg Hold Time Same Device <sup>[10]</sup>     | 0                   |      | 0    |      | 0    |      | 0                   |      | 0    |      | 0    |      | ns    |
| t <sub>OH</sub> - t <sub>IH</sub> 33X | Output Data Stable Time Minus I/P Reg Hold Time 7C330 & 7C332 <sup>[11]</sup>               | 0                   |      | 0    |      | 0    |      | 0                   |      | 0    |      | 0    |      | ns    |
| f <sub>MAX1</sub>                     | External Maximum Frequency (1/(t <sub>CO</sub> + t <sub>IS</sub> )) <sup>[12]</sup>         | 66.6                |      | 50.0 |      | 33.3 |      | 50.0                |      | 40.0 |      | 28.5 |      | MHz   |
| f <sub>MAX2</sub>                     | Data Path Maximum Frequency (1/(t <sub>WH</sub> + t <sub>WL</sub> )) <sup>[7, 13]</sup>     | 83.3                |      | 62.5 |      | 41.6 |      | 62.5                |      | 50.0 |      | 33.3 |      | MHz   |
| f <sub>MAX3</sub>                     | Internal Maximum Frequency <sup>[14]</sup>  | 74.0                |      | 57.0 |      | 37.0 |      | 57.0                |      | 45.0 |      | 30.0 |      | MHz   |

**4**

AC Test Loads and Waveforms (Commercial)

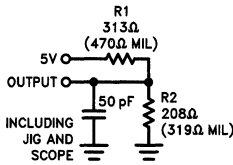


Figure 4a

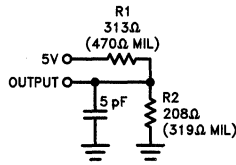


Figure 4b

0101-9

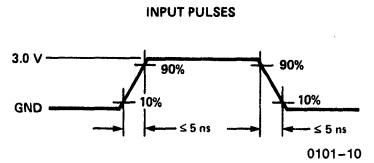
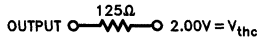


Figure 5

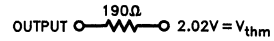
0101-10

Equivalent to: THEVENIN EQUIVALENT (Commercial)



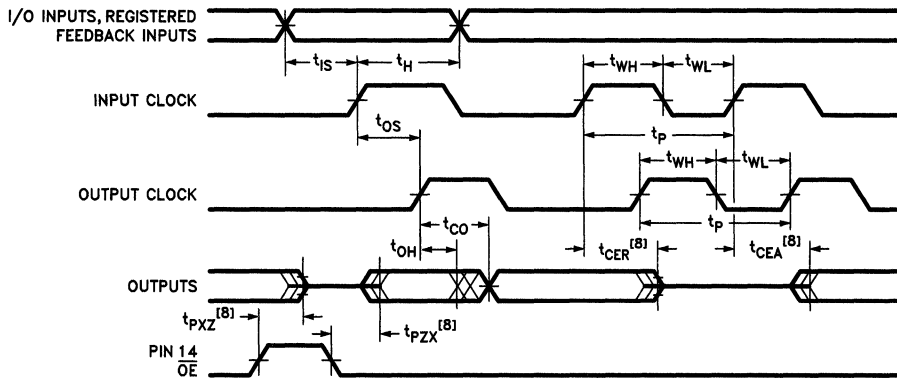
0101-11

Equivalent to: THEVENIN EQUIVALENT (Military)

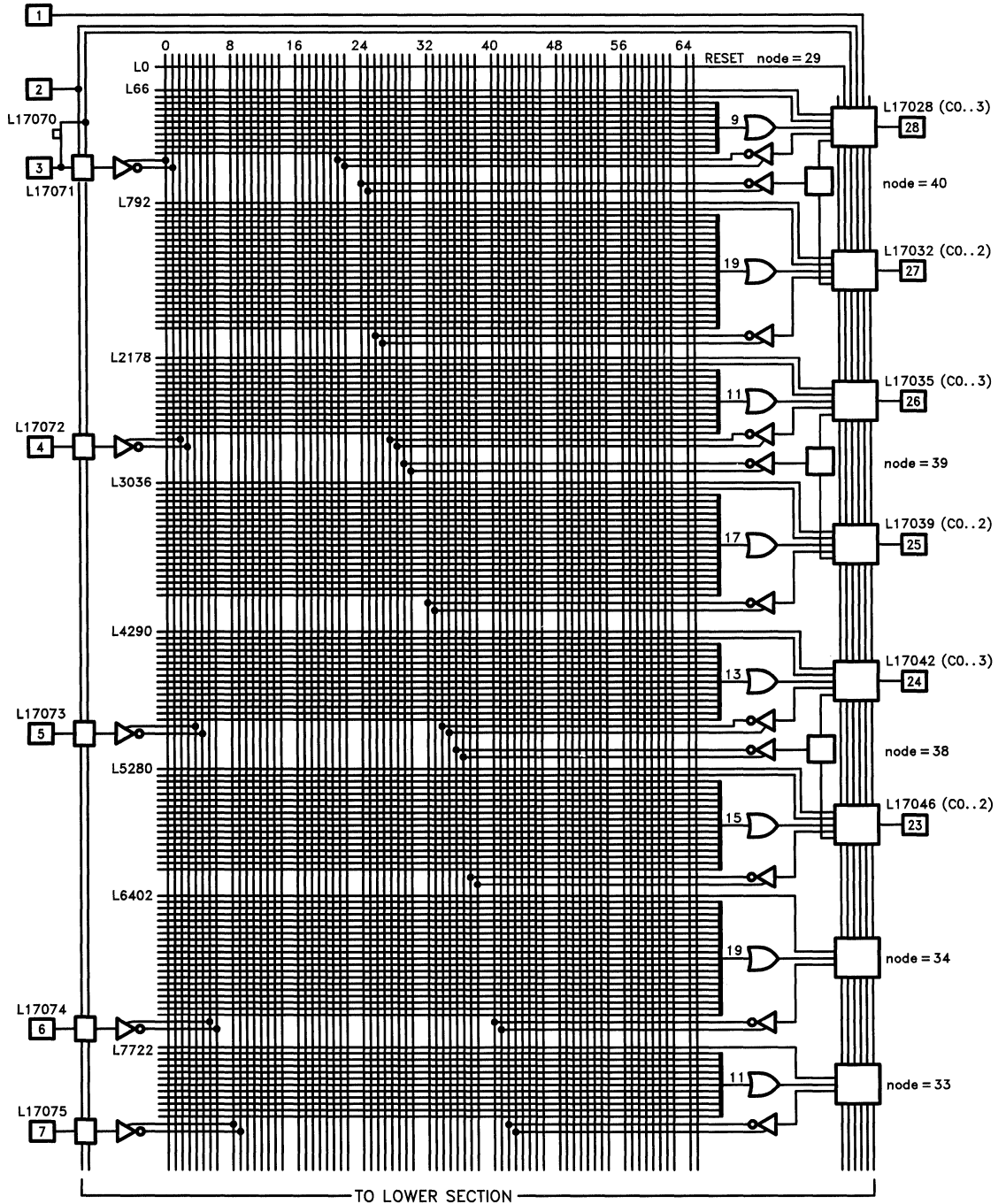


0101-12

Switching Waveforms

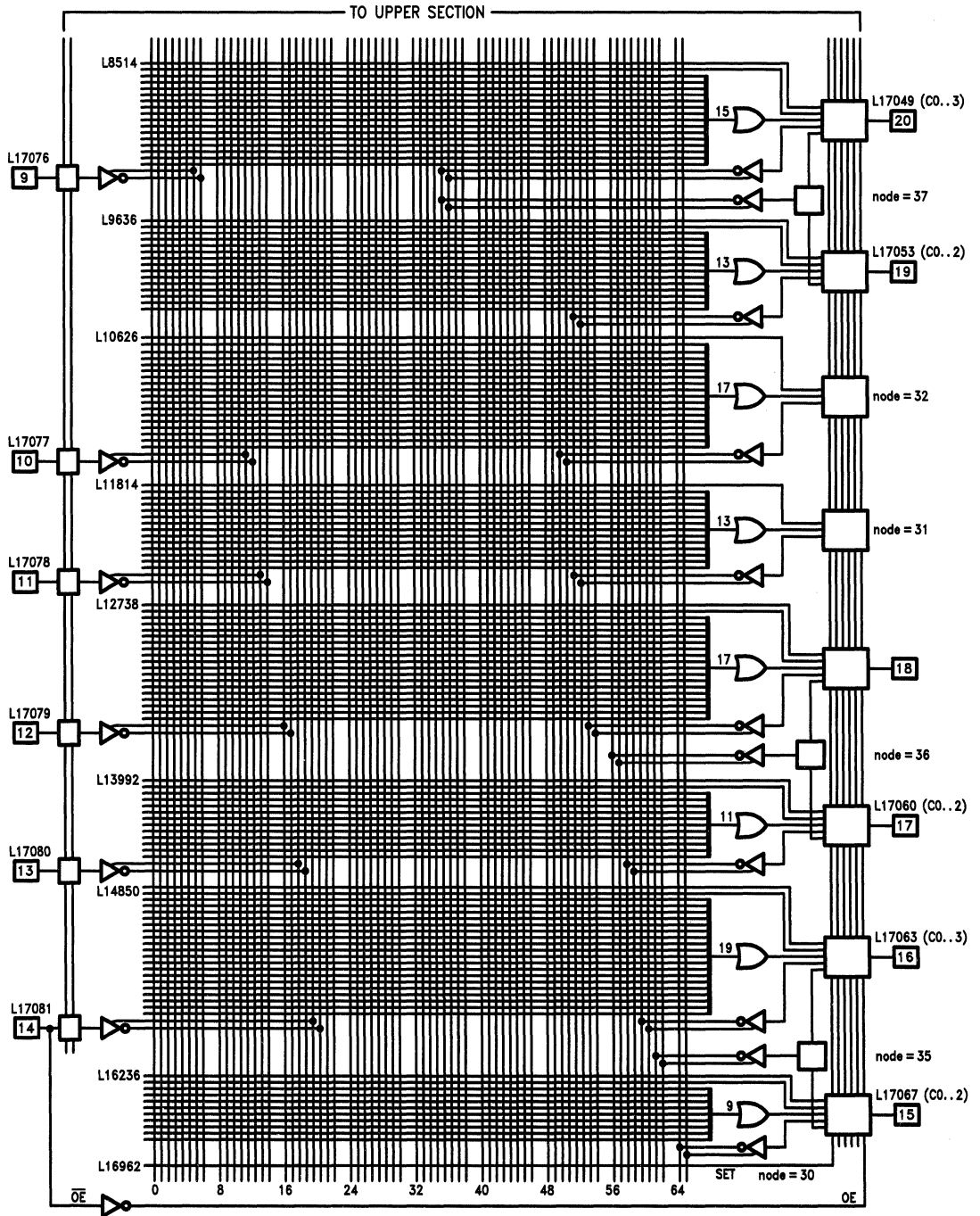


0101-13

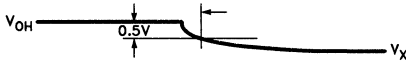

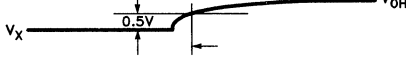
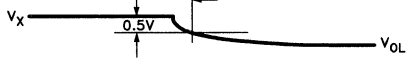
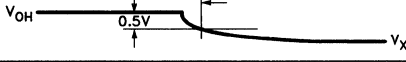
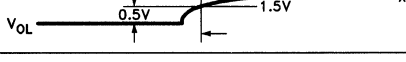
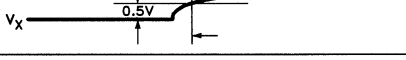
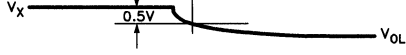


CY7C330 Block Diagram (Page 1 of 2)

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CY7C330 Block Diagram (Page 2 of 2)

| Parameter    | $V_x$     | Output Waveform—Measurement Level  |
|--------------|-----------|--|
| $tp_{XZ}(-)$ | 1.5V      | <br>$V_{OH}$ 0.5V $V_X$ 0101-19      |
| $tp_{XZ}(+)$ | 2.6V      | <br>$V_{OL}$ 0.5V 1.5V $V_X$ 0101-20 |
| $tp_{ZX}(+)$ | $V_{thc}$ | <br>$V_X$ 0.5V $V_{OH}$ 0101-21      |
| $tp_{ZX}(-)$ | $V_{thc}$ | <br>$V_X$ 0.5V $V_{OL}$ 0101-22      |
| $t_{CER}(-)$ | 1.5V      | <br>$V_{OH}$ 0.5V $V_X$ 0101-19      |
| $t_{CER}(+)$ | 2.6V      | <br>$V_{OL}$ 0.5V 1.5V $V_X$ 0101-20 |
| $t_{CEA}(+)$ | $V_{thc}$ | <br>$V_X$ 0.5V $V_{OH}$ 0101-21      |
| $t_{CEA}(-)$ | $V_{thc}$ | <br>$V_X$ 0.5V $V_{OL}$ 0101-22      |

**Figure 6. Test Waveforms**
**Ordering Information**

| $f_{max}$ (MHz) | $I_{CC1}$ (mA) | Ordering Code | Package | Operating Range |
|-----------------|----------------|---------------|---------|-----------------|
| 66.6            | 130            | CY7C330-66PC  | P21     | Commercial      |
|                 |                | CY7C330-66WC  | W22     |                 |
|                 |                | CY7C330-66JC  | J64     |                 |
| 50              | 150            | CY7C330-50DMB | D22     | Military        |
|                 |                | CY7C330-50WMB | W22     |                 |
|                 |                | CY7C330-50LMB | L64     |                 |
|                 |                | CY7C330-50TMB | T74     |                 |
|                 |                | CY7C330-50QMB | Q64     |                 |
| 50              | 130            | CY7C330-50PC  | P21     | Commercial      |
|                 |                | CY7C330-50WC  | W22     |                 |
|                 |                | CY7C330-50JC  | J64     |                 |
| 40              | 150            | CY7C330-40DMB | D22     | Military        |
|                 |                | CY7C330-40WMB | W22     |                 |
|                 |                | CY7C330-40LMB | L64     |                 |
|                 |                | CY7C330-40TMB | T74     |                 |
|                 |                | CY7C330-40QMB | Q64     |                 |
| 33.3            | 130            | CY7C330-33PC  | P21     | Commercial      |
|                 |                | CY7C330-33WC  | W22     |                 |
|                 |                | CY7C330-33JC  | J64     |                 |
| 28.5            | 150            | CY7C330-28DMB | D22     | Military        |
|                 |                | CY7C330-28WMB | W22     |                 |
|                 |                | CY7C330-28LMB | L64     |                 |
|                 |                | CY7C330-28TMB | T74     |                 |
|                 |                | CY7C330-28QMB | Q64     |                 |



**MILITARY SPECIFICATIONS****Group A Subgroup Testing****DC Characteristics**

| Parameters      | Subgroups |
|-----------------|-----------|
| V <sub>OH</sub> | 1,2,3     |
| V <sub>OL</sub> | 1,2,3     |
| V <sub>IH</sub> | 1,2,3     |
| V <sub>IL</sub> | 1,2,3     |
| I <sub>Ix</sub> | 1,2,3     |
| I <sub>OZ</sub> | 1,2,3     |
| I <sub>CC</sub> | 1,2,3     |

**Switching Characteristics**

| Parameters       | Subgroups |
|------------------|-----------|
| t <sub>ISU</sub> | 9,10,11   |
| t <sub>OSU</sub> | 9,10,11   |
| t <sub>CO</sub>  | 9,10,11   |
| t <sub>H</sub>   | 9,10,11   |
| t <sub>CEA</sub> | 9,10,11   |
| t <sub>PZX</sub> | 9,10,11   |

Document #: 38-00064-B



**Features**

- 12 I/O macrocells each having:
  - One state Flip-Flop with an XOR sum or products input
  - One feedback Flip-Flop with input coming from the I/O pin
  - Independent (product term) set, reset, and clock inputs on all registers
  - Asynchronous bypass capability on all registers, under product term control ( $r = s = 1$ )
  - Global or local output enable on tristate I/O
  - Feedback from either register to the array
- 192 product terms with variable distribution to macrocells
- 13 inputs, 12 feedback I/O pins, plus 6 shared I/O macrocell feedbacks for a total of 31 true and complementary inputs
- High speed: 20 tpd ns maximum
- Security bit
- Space saving 28 pin slim-line DIP package; also available in 28 pin PLCC
- Low power
  - 90 mA typical  $I_{CC}$  quiescent
  - 180 mA  $I_{CC}$  maximum
  - UV-Eraseable and reprogrammable
  - Programming and operation 100% testable

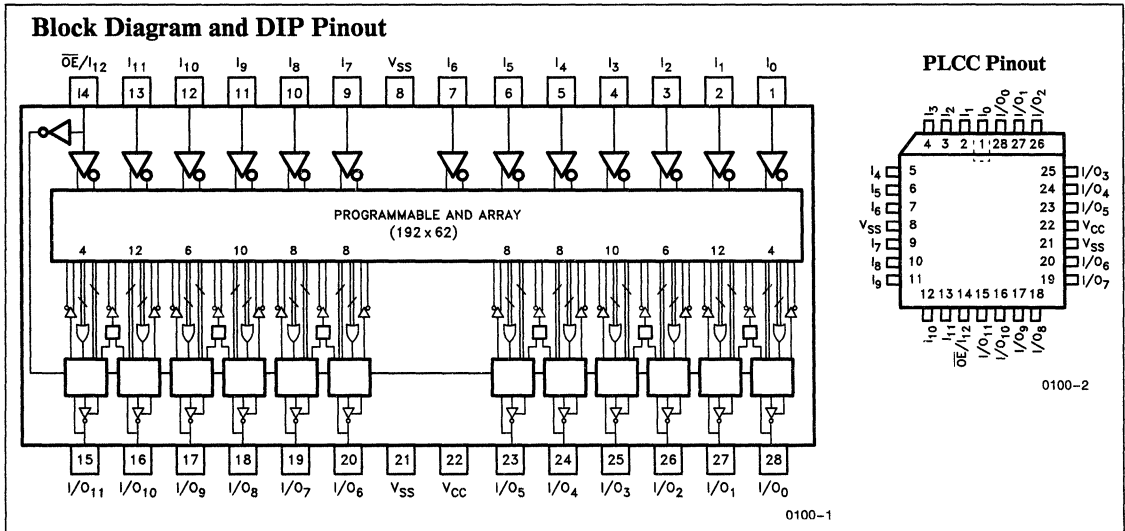
**Product Characteristics**

The CY7C331 is the most versatile PLD available for asynchronous designs. Central resources include 12 full D-type Flip-Flops with separate set, reset and clock capability. For increased utility, XOR gates are provided at the D-inputs and the product term allocation per Flip-Flop is variably distributed.

**I/O Resources**

Pins 1 through 7 and 9 through 14 serve as array inputs; pin 14 may also be used as a global output enable for the I/O macrocell tristate outputs. Pins 15 through 20 and 23 through 28 are connected to I/O macrocells and may be managed as inputs or outputs depending on the configuration and the macrocell OE terms.

4

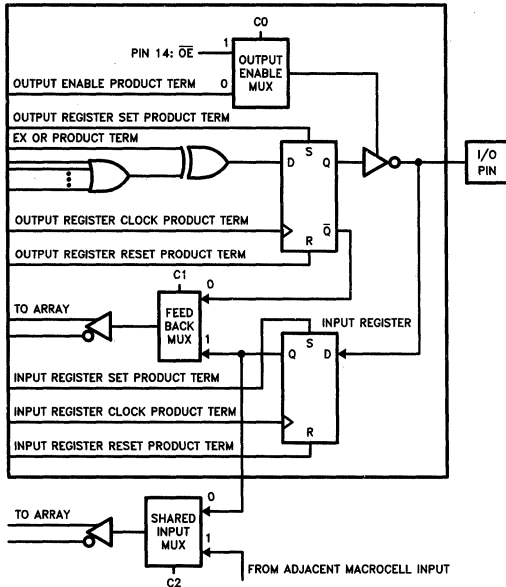


**Selection Guide**

| Generic Part Number        | $I_{CC1}$ mA |                     | tpd ns |                    | $t_s$ ns |                    | tco ns |                    |
|----------------------------|--------------|---------------------|--------|--------------------|----------|--------------------|--------|--------------------|
|                            | Com          | Mil                 | Com    | Mil                | Com      | Mil                | Com    | Mil                |
| CY7C331-20 <sup>[19]</sup> | 120          |                     | 20     |                    | 12       |                    | 20     |                    |
| CY7C331-25                 | 120          | 150 <sup>[19]</sup> | 25     | 25 <sup>[19]</sup> | 12       | 15 <sup>[19]</sup> | 25     | 25 <sup>[19]</sup> |
| CY7C331-30                 |              | 150                 |        | 30                 |          | 15                 |        | 30                 |
| CY7C331-35                 | 120          |                     | 35     |                    | 15       |                    | 35     |                    |
| CY7C331-40                 |              | 150                 |        | 40                 |          | 20                 |        | 40                 |

## I/O Resources (Continued)

It should be noted that there are two ground connections (pins 8 and 21) which, together with V<sub>CC</sub> (pin 22) are located centrally on the package. The reason for this placement and dual ground structure is to minimize the ground-loop noise when the outputs are driving simultaneously into a heavy capacitive load.



0100-3

**Figure 1. Macrocell**

The CY7C331 has 12 macrocells. Each macrocell has two D-type Flip-Flops. One is fed from the array, and one is fed from the I/O pin. For each Flip-Flop there are 3 dedicated product terms driving the R, S, and Clock inputs respectively. Each macrocell has one input to the array and for each pair of macrocells there is one shared input to the array. The macrocell input to the array may be configured to come from the 'Q' output of either Flip-Flop.

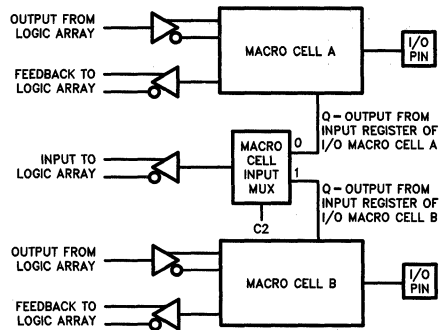
The D-type Flip-Flop which is fed from the array (i.e., the state Flip-Flop) has a logical XOR function on its input which combines a single product term with a sum (OR) of a number of product terms. The single product term is used to set the polarity of the output or to implement toggling (by including the current output in the product term).

The R and S inputs to the Flip-Flops override the current setting of the 'Q' output. The S input sets 'Q' true and the R input 'resets' 'Q' (sets it false). If both R and S are asserted (true) at once, then the output will follow the input ('Q' = 'D').

**Table 1**

| R | S | Q |
|---|---|---|
| 1 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 1 | D |

**R-S Truth Table**



0100-4

**Figure 2. Shared Input Multiplexer**

### Shared Input Multiplexer

The input associated with each pair of macrocells may be configured by the shared input multiplexer to come from either macrocell; the 'Q' output of the Flip-Flop coming from the I/O pin is used as the input signal source.

### Product Term Distribution

The product terms are distributed to the macrocells such that 32 product terms are distributed between two adjacent macrocells. The pairing of macrocells is the same as it is for the shared inputs. 8 of the product terms are used in each macrocell for set, reset, clock, OE and the upper part of the XOR gate. This leaves 16 product terms per pair of macrocells to be divided between the sum-of-product inputs to the two state registers. The following table shows the I/O pin pairing for shared inputs, and the product term (P-Term) allocation to macrocells associated with the I/O pins.

**Table 2**

| Macrocell | Pin Number | Product Terms |
|-----------|------------|---------------|
| 0         | 28         | 4             |
| 1         | 27         | 12            |
| 2         | 26         | 6             |
| 3         | 25         | 10            |
| 4         | 24         | 8             |
| 5         | 23         | 8             |
| 6         | 20         | 8             |
| 7         | 19         | 8             |
| 8         | 18         | 10            |
| 9         | 17         | 6             |
| 10        | 16         | 12            |
| 11        | 15         | 4             |

The CY7C331 is configured by three arrays of configuration bits (C0, C1, C2). For each macrocell, there is one C0 bit and one C1 bit. For each pair of macrocells, there is one C2 bit.

There are 12 C0 bits. If C0 is programmed for a macrocell, then the tristate enable (OE) will be controlled by pin 14 (the global OE). If C0 is not programmed, then the OE product term for that macrocell will be used.

There is one C1 bit for each macrocell. The C1 bit selects input for the product term (PT) array from either the state register (if the bit is unprogrammed) or the input register.

## I/O Resources (Continued)

There are 6 C2 bits, providing one C2 bit for each pair of macrocells. The C2 bit controls the shared input Multiplexer (Mux); if the C2 bit is not programmed, then the input to the product term array comes from the upper macrocell (A). If the C2 bit is programmed, then the input comes from the lower macrocell (B).

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|  |                                      |
|--|--------------------------------------|
| Storage Temperature .....  | -65°C to +150°C                      |
| Ambient Temperature with Power Applied .....                     | -55°C to +125°C                      |
| Supply Voltage to Group Potential (Pin 22 to Pins 8 or 21) ..... | -0.5V to +7.0V                       |
| DC Input Voltage .....   | -3.0V to +7.0V                       |
| Output Current into Outputs (Low) .....                          | 12 mA                                |
| Static Discharge Voltage .....                                   | >2001V (per MIL-STD-883 Method 3015) |

The timing diagrams for the CY7C331 cover state register, input register, and various combinational delays. Since internal clocks are the outputs of product terms, all timing is from the transition of inputs causing the clock transition.

|                              |         |
|------------------------------|---------|
| Latchup Current .....        | >200 mA |
| DC Programming Voltage ..... | 13.0V   |

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +75°C        | 5V ± 10%        |
| Military <sup>[5]</sup> | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over the Operating Range<sup>[6]</sup>

| Parameters       | Description                                       | Test Conditions  |  | Min.                   | Max. | Units |    |
|------------------|---|--|--|------------------------|------|-------|----|
|                  |   |  |  |                        |      |       |    |
| V <sub>OH</sub>  | Output HIGH Voltage                               | V <sub>CC</sub> = Min., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   | I <sub>OH</sub> = -3.2 mA<br>I <sub>OH</sub> = -2 mA | Commercial<br>Military | 2.4  | V     |    |
| V <sub>OL</sub>  | Output LOW Voltage                                | V <sub>CC</sub> = Min., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   | I <sub>OL</sub> = 12 mA<br>I <sub>OL</sub> = 8 mA    | Commercial<br>Military | 0.5  | V     |    |
| V <sub>IH</sub>  | Input HIGH Level                                  | Guaranteed HIGH Input, all Inputs <sup>[1]</sup>   |  |                        | 2.2  | V     |    |
| V <sub>IL</sub>  | Input LOW Level                                   | Guaranteed LOW Input, all Inputs <sup>[1]</sup>  |  |                        | 0.8  | V     |    |
| I <sub>IX</sub>  | Input Leakage Current                             | V <sub>SS</sub> < V <sub>IN</sub> < V <sub>CC</sub> , < V <sub>CC</sub> = Max.   |  |                        | -10  | 10    | μA |
| I <sub>OZ</sub>  | Output Leakage Current                            | V <sub>CC</sub> = Max., V <sub>SS</sub> < V <sub>OUT</sub> < V <sub>CC</sub>   |  |                        | -40  | 40    | μA |
| I <sub>SC</sub>  | Output Short Circuit Current                      | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V <sup>[2]</sup>   |  |                        | -30  | -90   | mA |
| I <sub>CC1</sub> | Standby Power Supply Current                      | V <sub>CC</sub> = Max., V <sub>IN</sub> = GND, Outputs Open  | Commercial   |                        | 120  | mA    |    |
|                  |   |  | Military   |                        | 150  | mA    |    |
| I <sub>CC2</sub> | Power Supply Current at Frequency <sup>[19]</sup> | V <sub>CC</sub> = Max. Outputs Disabled (in HIGH Z State) Device Operating at f <sub>MAX</sub> External (f <sub>MAX1</sub> ) | Commercial   |                        | 180  | mA    |    |
|                  |   |  | Military   |                        | 200  | mA    |    |

## Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions                     | Min. | Max. | Units |
|------------------|--------------------|-------------------------------------|------|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | V <sub>IN</sub> = 2.0V @ f = 1 MHz  |      | 7    | pF    |
| C <sub>OUT</sub> | Output Capacitance | V <sub>OUT</sub> = 2.0V @ f = 1 MHz |      | 8    |       |

### Notes:

- These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V<sub>OUT</sub> = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.
- Figure 3a test load used for all parameters except t<sub>PZX1</sub>, t<sub>PXZ1</sub>, t<sub>PZX</sub> and t<sub>PXZ</sub>. Figure 3b test load for t<sub>PZX1</sub>, t<sub>PXZ1</sub>, t<sub>PZX</sub> and t<sub>PXZ</sub>. Figure 3c shows test waveforms and measurement levels.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

**Switching Characteristics<sup>[6]</sup>**

| Parameters                             | Description   | Commercial          |      |      |      |      |      | Military            |      |      |      |      |      | Units |
|--|---|---------------------|------|------|------|------|------|---------------------|------|------|------|------|------|-------|
|  |   | -20 <sup>[19]</sup> |      | -25  |      | -35  |      | -25 <sup>[19]</sup> |      | -30  |      | -40  |      |       |
|  |   | Min.                | Max. | Min. | Max. | Min. | Max. | Min.                | Max. | Min. | Max. | Min. | Max. |       |
| t <sub>PD</sub>                        | Input to Output Propagation Delay <sup>[7]</sup>  |                     | 20   |      | 25   |      | 35   |                     | 25   |      | 30   |      | 40   | ns    |
| t <sub>ICO</sub>                       | Input Register Clock to Output Delay <sup>[8]</sup>   |                     | 35   |      | 40   |      | 55   |                     | 45   |      | 50   |      | 65   | ns    |
| t <sub>IOH</sub>                       | Output Data Stable Time from Input Clock <sup>[8]</sup>   | 5                   |      | 5    |      | 5    |      | 5                   |      | 5    |      | 5    |      | ns    |
| t <sub>IS</sub>                        | Input or Feedback Setup Time to Input Register Clock <sup>[8]</sup>   | 2                   |      | 2    |      | 2    |      | 5                   |      | 5    |      | 5    |      | ns    |
| t <sub>IH</sub>                        | Input Register Hold Time from Input Clock <sup>[8]</sup>  | 11                  |      | 13   |      | 15   |      | 13                  |      | 15   |      | 20   |      | ns    |
| t <sub>IAR</sub>                       | Input to Input Register Asynchronous Reset Delay <sup>[8]</sup>   |                     | 35   |      | 40   |      | 55   |                     | 45   |      | 50   |      | 65   | ns    |
| t <sub>IRW</sub>                       | Input Register Reset Width <sup>[8]</sup>   | 35                  |      | 40   |      | 55   |      | 45                  |      | 50   |      | 65   |      | ns    |
| t <sub>IRR</sub>                       | Input Register Reset Recovery Time <sup>[8]</sup>   | 35                  |      | 40   |      | 55   |      | 45                  |      | 50   |      | 65   |      | ns    |
| t <sub>IAS</sub>                       | Input to Input Register Asynchronous Set Delay <sup>[8]</sup>   |                     | 35   |      | 40   |      | 55   |                     | 45   |      | 50   |      | 65   | ns    |
| t <sub>ISW</sub>                       | Input Register Set Width <sup>[8]</sup>   | 35                  |      | 40   |      | 55   |      | 45                  |      | 50   |      | 65   |      | ns    |
| t <sub>ISR</sub>                       | Input Register Set Recovery Time <sup>[8]</sup>   | 35                  |      | 40   |      | 55   |      | 45                  |      | 50   |      | 65   |      | ns    |
| t <sub>WH</sub>                        | Input & Output Clock Width High <sup>[8, 9, 12]</sup>   | 12                  |      | 15   |      | 20   |      | 15                  |      | 20   |      | 25   |      | ns    |
| t <sub>WL</sub>                        | Input & Output Clock Width Low <sup>[8, 9, 12]</sup>  | 12                  |      | 15   |      | 20   |      | 15                  |      | 20   |      | 25   |      | ns    |
| f <sub>MAX1</sub>                      | Maximum Frequency with Feedback in Input Registered Mode (1/(t <sub>ICO</sub> + t <sub>IS</sub> )) <sup>[13]</sup>                      | 27.0                |      | 23.8 |      | 17.5 |      | 20.0                |      | 18.1 |      | 14.2 |      | MHz   |
| f <sub>MAX2</sub>                      | Maximum Frequency Data Path in Input Registered Mode (1/t <sub>ICO</sub> ) <sup>[8]</sup>   | 28.5                |      | 25.0 |      | 18.1 |      | 22.2                |      | 20.0 |      | 15.3 |      | ns    |
| t <sub>IOH</sub> - t <sub>IH</sub> 33X | Output Data Stable from Input Clock Minus Input Register Input Hold Time for 7C330 and 7C332 <sup>[15, 18]</sup>                        | 0                   |      | 0    |      | 0    |      | 0                   |      | 0    |      | 0    |      | ns    |
| t <sub>CO</sub>                        | Output Register Clock to Output Delay <sup>[9]</sup>  |                     | 20   |      | 25   |      | 35   |                     | 25   |      | 30   |      | 40   | ns    |
| t <sub>OH</sub>                        | Output Data Stable Time from Output Clock <sup>[9]</sup>  | 3                   |      | 3    |      | 3    |      | 3                   |      | 3    |      | 3    |      | ns    |
| t <sub>S</sub>                         | Output Register Input Set Up Time to Output Clock <sup>[9]</sup>  | 12                  |      | 12   |      | 15   |      | 15                  |      | 15   |      | 20   |      | ns    |
| t <sub>H</sub>                         | Output Register Input Hold Time from Output Clock <sup>[9]</sup>  | 8                   |      | 8    |      | 10   |      | 10                  |      | 10   |      | 12   |      | ns    |
| t <sub>OAR</sub>                       | Input to Output Register Asynchronous Reset Delay <sup>[9]</sup>  |                     | 20   |      | 25   |      | 35   |                     | 25   |      | 30   |      | 40   | ns    |
| t <sub>ORW</sub>                       | Output Register Reset Width <sup>[9]</sup>  | 20                  |      | 25   |      | 35   |      | 25                  |      | 30   |      | 40   |      | ns    |
| t <sub>ORR</sub>                       | Output Register Reset Recovery Time <sup>[9]</sup>  | 20                  |      | 25   |      | 35   |      | 25                  |      | 30   |      | 40   |      | ns    |
| t <sub>OAS</sub>                       | Input to Output Register Asynchronous Set Delay <sup>[9]</sup>  |                     | 20   |      | 25   |      | 35   |                     | 25   |      | 30   |      | 40   | ns    |
| t <sub>OSW</sub>                       | Output Register Set Width <sup>[9]</sup>  | 20                  |      | 25   |      | 35   |      | 25                  |      | 30   |      | 40   |      | ns    |
| t <sub>OSR</sub>                       | Output Register Set Recovery Time <sup>[9]</sup>  | 20                  |      | 25   |      | 35   |      | 25                  |      | 30   |      | 40   |      | ns    |
| t <sub>EA</sub>                        | Input to Output Enable Delay <sup>[4, 10]</sup>   |                     | 20   |      | 25   |      | 35   |                     | 25   |      | 30   |      | 40   | ns    |
| t <sub>ER</sub>                        | Input to Output Disable Delay <sup>[4, 10]</sup>  |                     | 20   |      | 25   |      | 35   |                     | 25   |      | 30   |      | 40   | ns    |
| t <sub>PZX</sub>                       | Pin 14 to Output Enable Delay <sup>[4, 10]</sup>  |                     | 17   |      | 20   |      | 30   |                     | 20   |      | 25   |      | 35   | ns    |
| t <sub>PXZ</sub>                       | Pin 14 to Output Disable Delay <sup>[4, 10]</sup>   |                     | 17   |      | 20   |      | 30   |                     | 20   |      | 25   |      | 35   | ns    |
| f <sub>MAX3</sub>                      | Maximum Frequency with Feedback in Output Registered Mode (1/(t <sub>CO</sub> + t <sub>S</sub> )) <sup>[14]</sup>                       | 31.2                |      | 27.0 |      | 20.0 |      | 25.0                |      | 22.2 |      | 16.6 |      | MHz   |
| f <sub>MAX4</sub>                      | Max. Frequency Data Path in Output Registered Mode (Lower of 1/t <sub>CO</sub> + 1/(t <sub>WH</sub> + t <sub>WL</sub> )) <sup>[9]</sup> | 41.6                |      | 33.3 |      | 25.0 |      | 33.3                |      | 25.0 |      | 20.0 |      | MHz   |
| t <sub>OH</sub> - t <sub>IH</sub> 33X  | Output Data Stable from Output Clock Minus Input Register Input Hold Time for 7C330 and 7C332 <sup>[16, 18]</sup>                       | 0                   |      | 0    |      | 0    |      | 0                   |      | 0    |      | 0    |      | ns    |
| f <sub>MAX5</sub>                      | Maximum Frequency Pipelined Mode <sup>[12, 17]</sup>  | 35.0                |      | 30.0 |      | 22.0 |      | 28.0                |      | 23.5 |      | 18.5 |      | MHz   |

Notes:

7. Refer to Figure 5 configuration 1.
8. Refer to Figure 5 configuration 2.
9. Refer to Figure 5 configuration 3.
10. Refer to Figure 5 configuration 4.
11. Refer to Figure 5 configuration 5.
12. Refer to Figure 5 configuration 6.
13. Refer to Figure 6 configuration 7.
14. Refer to Figure 6 configuration 8.
15. Refer to Figure 7 configuration 9.
16. Refer to Figure 7 configuration 10.
17. This specification is intended to guarantee that a state machine configuration created with internal or external feedback can be operated with output register and input register clocks controlled by the same source. These parameters are tested by periodic sampling of production product.
18. This specification is intended to guarantee interface compatibility of the other members of the CY7C330 family with the CY7C331. This specification is met for the devices noted operating at the same ambient temperature and at the same power supply voltage. These parameters are tested periodically by sampling of production product.
19. Preliminary specifications.

AC Test Loads and Waveforms

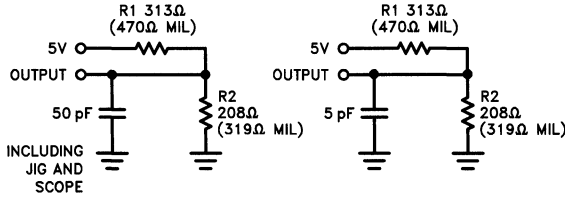


Figure 3a

Figure 3b

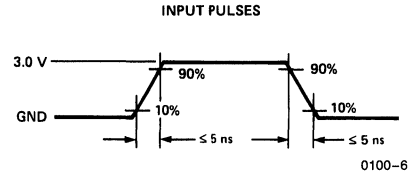
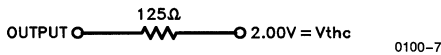


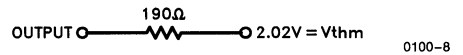
Figure 4

Equivalent to: THÉVENIN EQUIVALENT (Commercial)



0100-7

Equivalent to: THÉVENIN EQUIVALENT (Military)



0100-8


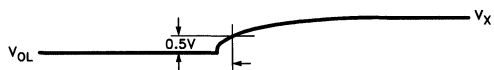
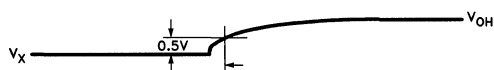

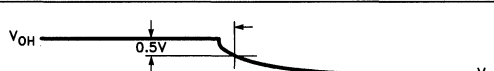
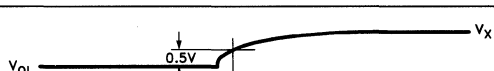
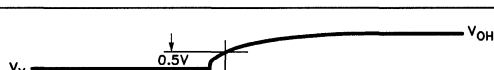
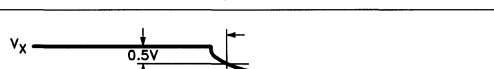
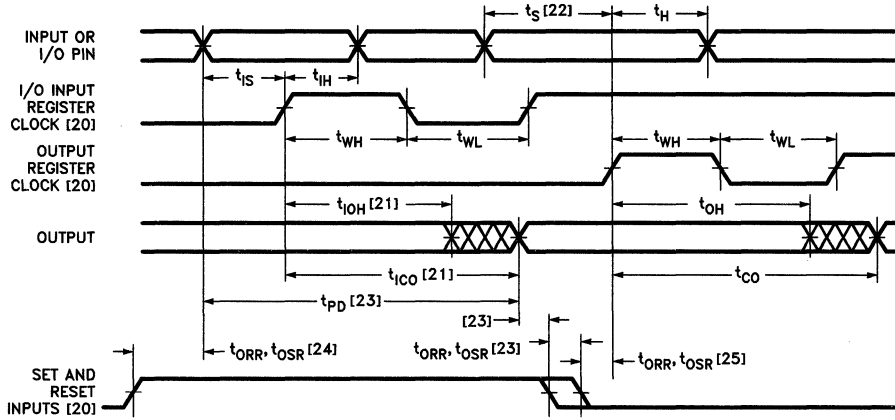
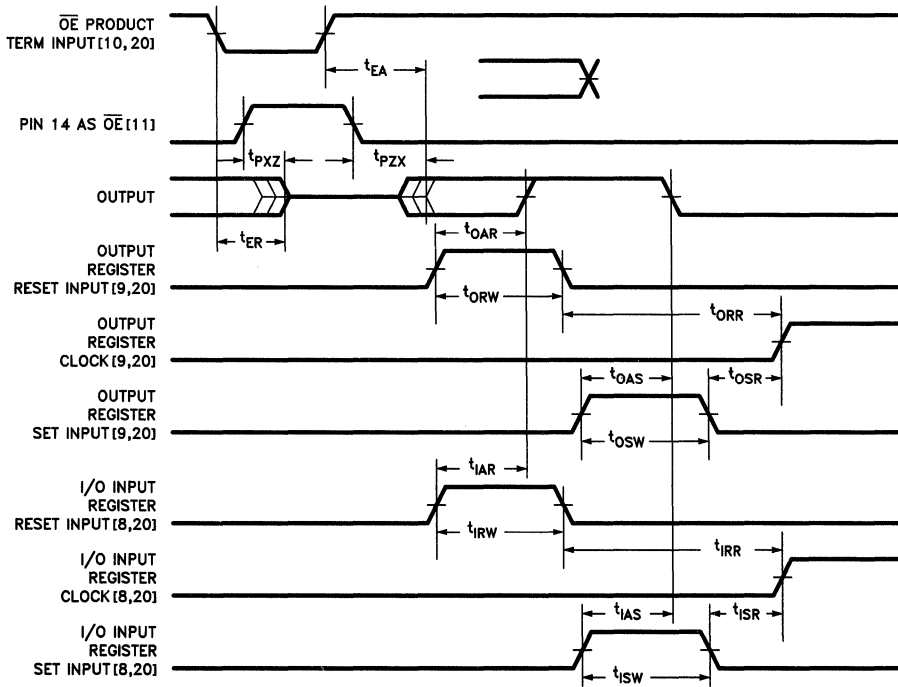
| Parameters   | $V_x$     | Output Waveform—Measurement Level  |
|--------------|-----------|--|
| $tp_{XZ}(-)$ | 1.5V      |  0100-16   |
| $tp_{XZ}(+)$ | 2.6V      |  0100-17  |
| $tp_{ZX}(+)$ | $V_{thc}$ |  0100-18 |
| $tp_{ZX}(-)$ | $V_{thc}$ |  0100-19 |
| $t_{ER}(-)$  | 1.5V      |  0100-16 |
| $t_{ER}(+)$  | 2.6V      |  0100-17 |
| $t_{EA}(+)$  | $V_{thc}$ |  0100-18 |
| $t_{EA}(-)$  | $V_{thc}$ |  0100-19 |

Figure 3c. Test Waveforms and Measurement Levels

## Switching Waveforms



0100-9



0100-10

### Notes:

20. Because these input signals are controlled by product terms, active input polarity may be of either polarity. Internal active input polarity has been shown for clarity.
21. Output register is set in Transparent Mode. Output register Set and Reset inputs are in a HIGH state.
22. Dedicated input or input register set in Transparent Mode. Input register Set and Reset inputs are in a HIGH state.
23. Combinatorial Mode. Reset and Set inputs of the input and output registers should remain in a HIGH state at least until the output responds at  $t_{pd}$ . When returning Set and Reset inputs to a LOW state, one of these signals should go LOW a MINIMUM of  $t_{OSR}$  (Set input) or  $t_{ORR}$  (Reset input) prior to the other. This guarantees predictable register states upon exit from Combinatorial Mode.
24. When entering the Combinatorial Mode, input and output register Set and Reset inputs must be stable in a HIGH state a MINIMUM of  $t_{ISR}/t_{IRR}$  and  $t_{OSR}/t_{ORR}$  respectively prior to application of logic input signals.
25. When returning to the input and/or output Registered Mode, register Set and Reset inputs must be stable in a LOW state a MINIMUM of  $t_{ISR}/t_{IRR}$  and  $t_{OSR}/t_{ORR}$  respectively prior to the application of the register clock input.

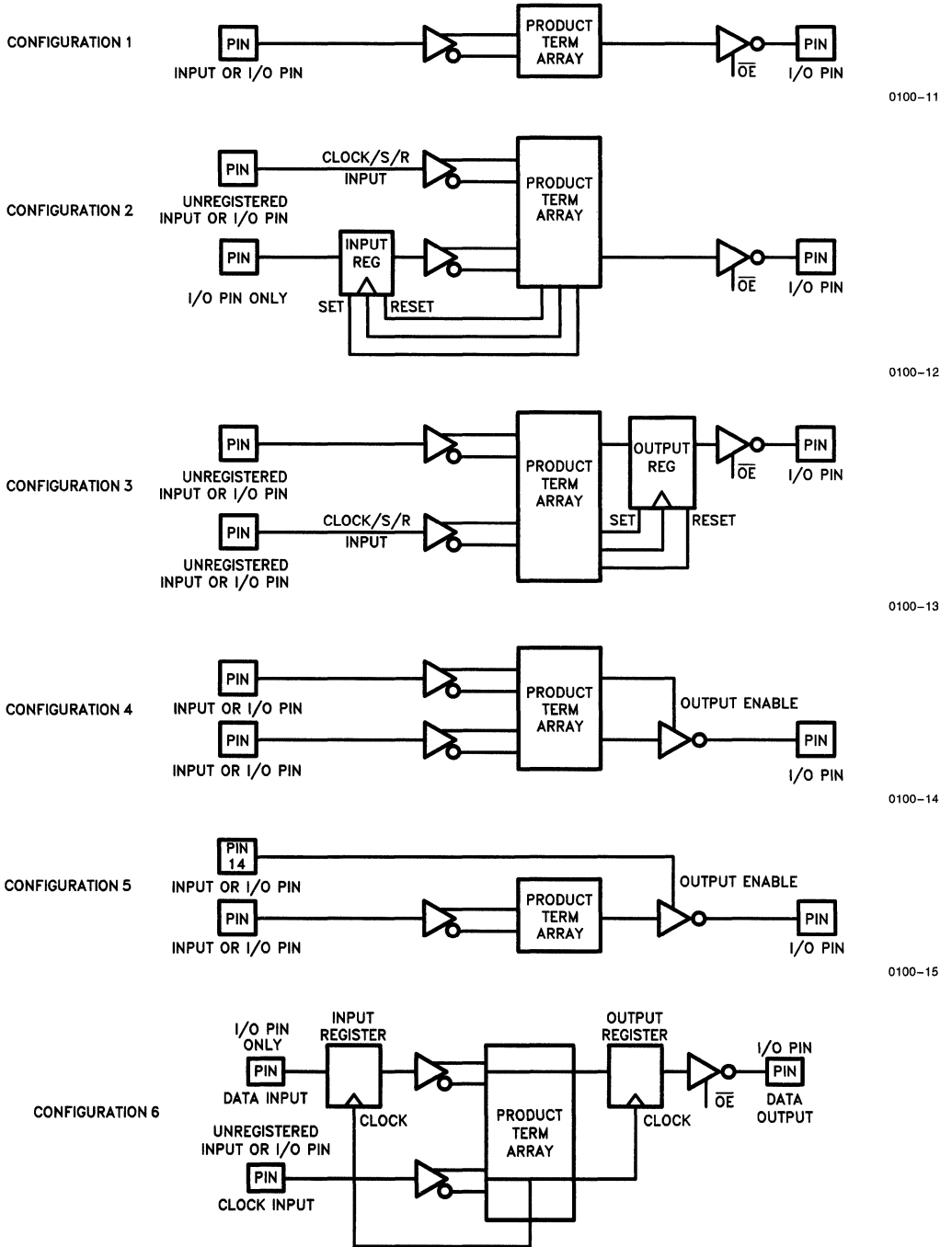
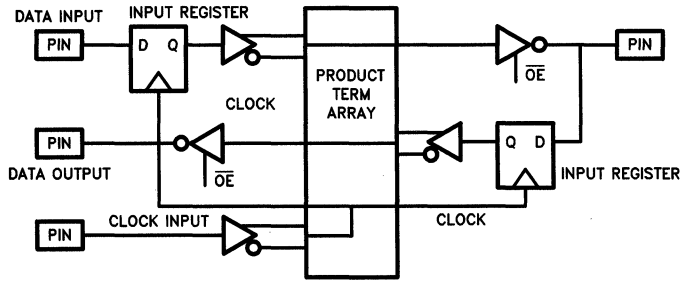


Figure 5. Timing Configurations

0100-20

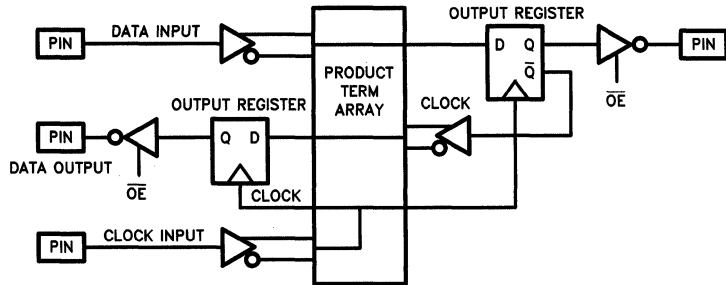


CONFIGURATION 7



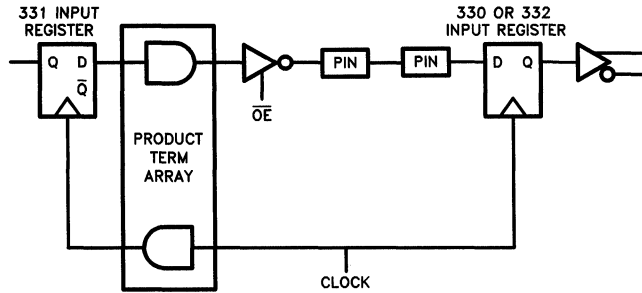
0100-21

CONFIGURATION 8



0100-22

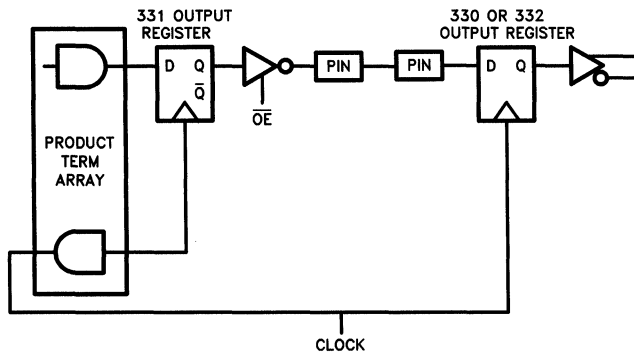
CONFIGURATION 9



0100-23

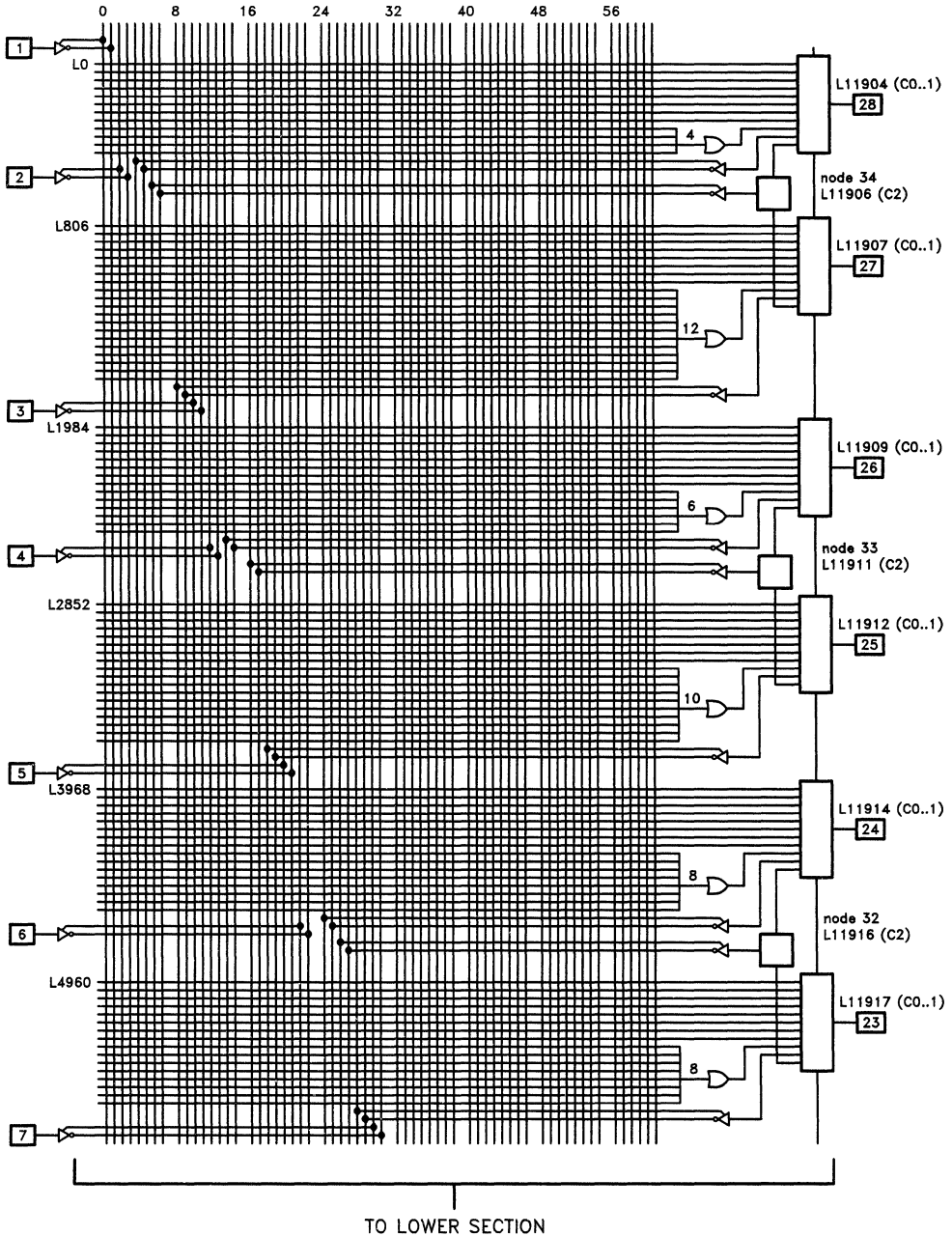
Figure 6

CONFIGURATION 10

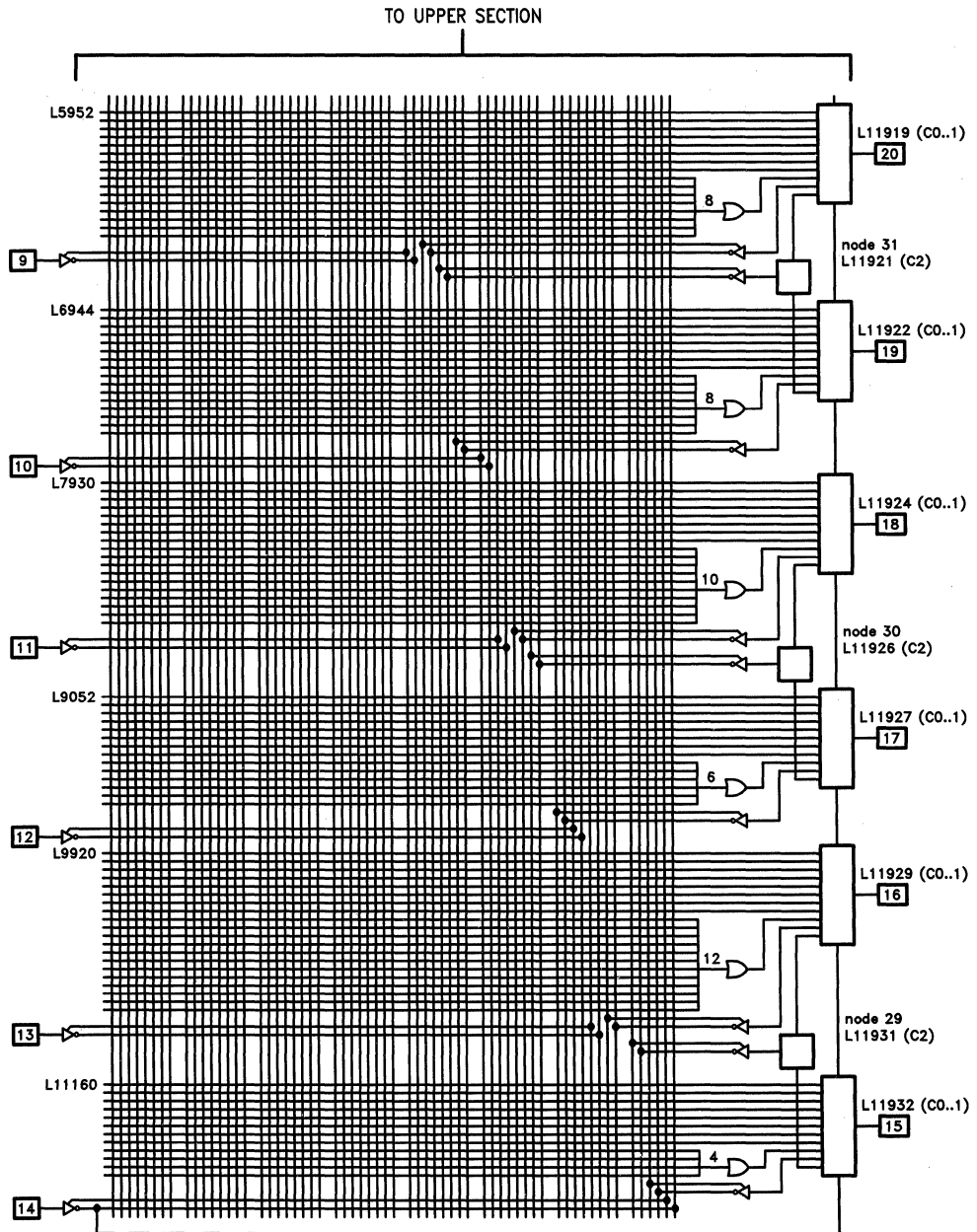


0100-26

Figure 7



CY7C331 Logic Diagram (Upper Half)



**CY7C331 Logic Diagram (Lower Half)**

**Ordering Information**

| ICC1<br>(mA) | t <sub>PD</sub><br>(ns) | t <sub>S</sub><br>(ns) | t <sub>CO</sub><br>(ns) | Ordering Code | Package<br>Type | Operating<br>Range |
|--------------|-------------------------|------------------------|-------------------------|---------------|-----------------|--------------------|
| 120          | 20                      | 12                     | 20                      | CY7C331-20PC  | P21             | Commercial         |
|              |                         |                        |                         | CY7C331-20WC  | W22             |                    |
|              |                         |                        |                         | CY7C331-20JC  | J64             |                    |
| 150          | 25                      | 15                     | 25                      | CY7C331-25DMB | D22             | Military           |
|              |                         |                        |                         | CY7C331-25WMB | W22             |                    |
|              |                         |                        |                         | CY7C331-25LMB | L64             |                    |
|              |                         |                        |                         | CY7C331-25TMB | T74             |                    |
|              |                         |                        |                         | CY7C331-25QMB | Q64             |                    |
| 180          | 25                      | 12                     | 25                      | CY7C331-25PC  | P21             | Commercial         |
|              |                         |                        |                         | CY7C331-25WC  | W22             |                    |
|              |                         |                        |                         | CY7C331-25JC  | J64             |                    |
| 200          | 30                      | 15                     | 30                      | CY7C331-30DMB | D22             | Military           |
|              |                         |                        |                         | CY7C331-30WMB | W22             |                    |
|              |                         |                        |                         | CY7C331-30LMB | L64             |                    |
|              |                         |                        |                         | CY7C331-30TMB | T74             |                    |
|              |                         |                        |                         | CY7C331-30QMB | Q64             |                    |
| 180          | 35                      | 15                     | 35                      | CY7C331-35PC  | P21             | Commercial         |
|              |                         |                        |                         | CY7C331-35WC  | W22             |                    |
|              |                         |                        |                         | CY7C331-35JC  | J64             |                    |
| 200          | 40                      | 20                     | 40                      | CY7C331-40DMB | D22             | Military           |
|              |                         |                        |                         | CY7C331-40WMB | W22             |                    |
|              |                         |                        |                         | CY7C331-40LMB | L64             |                    |
|              |                         |                        |                         | CY7C331-40TMB | T74             |                    |
|              |                         |                        |                         | CY7C331-40QMB | Q64             |                    |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters       | Subgroups |
|------------------|-----------|
| V <sub>OH</sub>  | 1,2,3     |
| V <sub>OL</sub>  | 1,2,3     |
| V <sub>IH</sub>  | 1,2,3     |
| V <sub>IL</sub>  | 1,2,3     |
| I <sub>IX</sub>  | 1,2,3     |
| I <sub>OZ</sub>  | 1,2,3     |
| I <sub>CC1</sub> | 1,2,3     |

**Switching Characteristics**

| Parameters       | Subgroups |
|------------------|-----------|
| t <sub>IS</sub>  | 9,10,11   |
| t <sub>IH</sub>  | 9,10,11   |
| t <sub>WH</sub>  | 9,10,11   |
| t <sub>WL</sub>  | 9,10,11   |
| t <sub>CO</sub>  | 9,10,11   |
| t <sub>PD</sub>  | 9,10,11   |
| t <sub>IAR</sub> | 9,10,11   |
| t <sub>IAS</sub> | 9,10,11   |
| t <sub>PXZ</sub> | 9,10,11   |
| t <sub>PZX</sub> | 9,10,11   |
| t <sub>ER</sub>  | 9,10,11   |
| t <sub>EA</sub>  | 9,10,11   |
| t <sub>S</sub>   | 9,10,11   |
| t <sub>H</sub>   | 9,10,11   |

Document #: 38-00066-B



**Features**

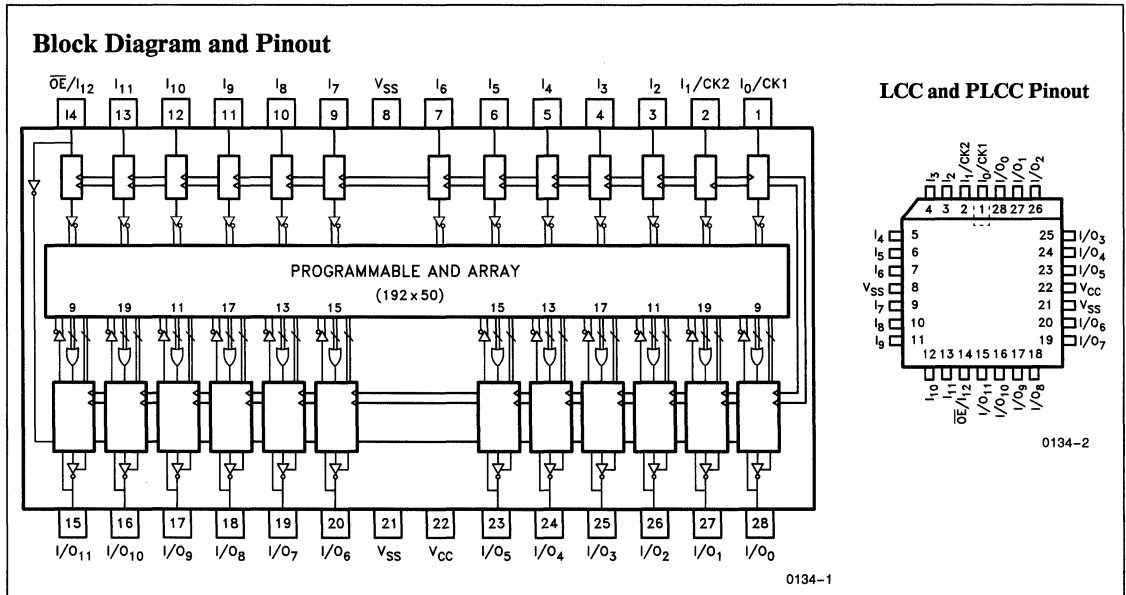
- 12 I/O macrocells each having:
  - Registered, latched, or transparent array input
  - A choice of two clock sources
  - Global or local output enable (OE)
  - Up to 19 product terms (PT) per output
  - Product term (PT) output polarity control
- 192 product terms with variable distribution to macrocells
  - An average of 14 PT's per macrocell sum node
  - Up to 19 PT's maximum for select nodes
- 2 clock inputs with configurable polarity control
- 13 input macrocells, each having:
  - Complementary input
  - Register, latch, or transparent access
  - Two clock sources
- 20 ns max. delay
- Low power
  - 120 mA typical I<sub>CC</sub> quiescent
  - 180 mA max.
  - Power saving "Miser Bit" feature
- Security fuse
- 28 pin slim-line package; also available in 28 pin PLC
- UV-Eraseable and reprogrammable
- Programming and operation 100% testable

**Product Characteristics**

The CY7C332 is a versatile combinatorial PLD with I/O registers onboard. There are 25 array inputs; each has a macrocell which may be configured as a register, latch or simple buffer. Outputs have polarity and tristate control product terms. The allocation of product terms to I/O macrocells is varied so that functions of up to 19 product terms can be accommodated.

**I/O Resources**

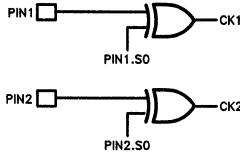
Pins 1 through 7 and 9 through 14 function as dedicated array inputs. Pins 1 and 2 function as input clocks as well as normal inputs. Pin 14 functions as a global output enable as well as a normal input.



**Selection Guide**

| Generic Part Number | I <sub>CC1</sub> mA |     | t <sub>1CO</sub> /t <sub>PD</sub> ns |     | t <sub>IS</sub> ns |     |
|---------------------|---------------------|-----|--------------------------------------|-----|--------------------|-----|
|                     | Com                 | Mil | Com                                  | Mil | Com                | Mil |
| 7C332-20            | 120                 |     | 20                                   |     | 3                  |     |
| 7C332-25            | 120                 | 150 | 25                                   | 25  | 3                  | 4   |
| 7C332-30            |                     | 150 |                                      | 30  |                    | 4   |

**I/O Resources (Continued)**

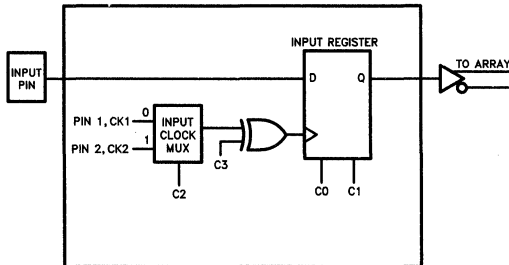


0134-3

**Figure 1. CK1 and CK2**

Pins 15 through 20 and 23 through 28 are connected to I/O macrocells and may be combinatorial outputs as well as registered or direct inputs.

**Input Macrocell**



0134-4

**Figure 2. Input Macrocell**

| C3 | C2 | C1 | C0 | Input Register Option          |
|----|----|----|----|--------------------------------|
| X  | X  | 0  | 0  | Combinatorial                  |
| X  | X  | 0  | 1  | Illegal                        |
| 0  | 0  | 1  | 1  | Registered, CLK1, Rising Edge  |
| 0  | 1  | 1  | 1  | Registered, CLK2, Rising Edge  |
| 1  | 0  | 1  | 1  | Registered, CLK1, Falling Edge |
| 1  | 1  | 1  | 1  | Registered, CLK2, Falling Edge |
| 0  | 0  | 1  | 0  | Latched, CLK1, High Asserted   |
| 0  | 1  | 1  | 0  | Latched, CLK2, High Asserted   |
| 1  | 0  | 1  | 0  | Latched, CLK1, Low Asserted    |
| 1  | 1  | 1  | 0  | Latched, CLK1, Low Asserted    |

There are 13 input macrocells, corresponding to pins 1 through 7 and 9 through 14. Each macrocell has a clock which is selected to come from either pin 1 or pin 2 by configuration bit C2. Pins 1 and 2 are clocks as well as normal inputs. There is no C2 configuration bit for either of these two input macrocells. Macrocells connected to pins 1 and 2 do not have a clock choice, but each has a clock coming from the other pin.

Each input macrocell can be configured as a register, latch or a simple buffer (transparent path) to the product term array. For a register the configuration bit, C0, is 1 (programmed) and C1 is 1. For a Latch, C0 is 0 and C1 is 1. If both C0 and C1 are 0 (unprogrammed) then the macrocell is completely transparent.

Configuration bit C3 determines the clock edge on which the register is triggered or the polarity for which the latch is asserted. This clock polarity can be programmed independently for each input register. These configuration options are available on all inputs, including those in the I/O macrocell.

If C3 is 0 (unprogrammed), the clock will be rising edge triggered (register mode) or high asserted (latch mode).

If C3 is 1 (programmed), the clock will be falling edge triggered (register mode) or low asserted (latch mode).

**I/O Macrocell**

There are 12 I/O macrocells corresponding to pins 15 through 20 and 23 through 28. Each macrocell has a tristate output control, an XOR product term to dynamically control polarity, and a configurable feedback path.

For each I/O macrocell, the tristate control for the output may be configured two ways. If the configuration bit, C4, is a 1 (programmed), then the global OE signal is selected. Otherwise, the OE product term is used.

For each I/O macrocell, the input/feedback path may be configured as a register, latch, or shunt. There are two configuration bits per I/O macrocell which configure the feedback path. These are programmed in the same way as for the input macrocells.

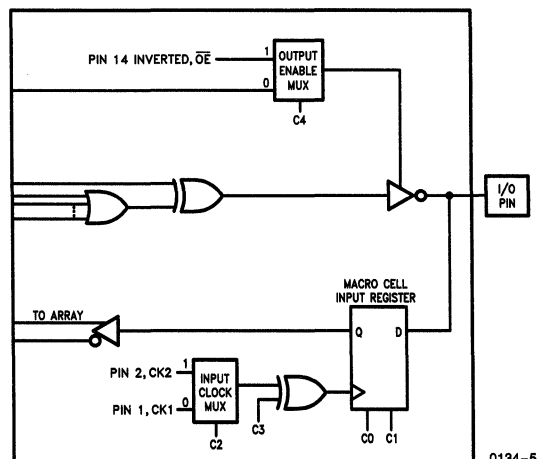
For each I/O macrocell, the input register clock (or Latch Enable) which is used for the input/feedback path may be selected as pin 1 (select bit, C2, not programmed) or pin 2 (select bit, C2, programmed).

**Array Allocation to Output Macrocell**

The number of product terms in each output macrocell sum is position dependent. The table below summarizes the allocation:

**Table 1**

| Macrocell | Pin Number | Product Terms |
|-----------|------------|---------------|
| 0         | 28         | 9             |
| 1         | 27         | 19            |
| 2         | 26         | 11            |
| 3         | 25         | 17            |
| 4         | 24         | 13            |
| 5         | 23         | 15            |
| 6         | 20         | 15            |
| 7         | 19         | 13            |
| 8         | 18         | 17            |
| 9         | 17         | 11            |
| 10        | 16         | 19            |
| 11        | 15         | 9             |



0134-5

**Figure 3. I/O Macrocell**

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential  
(Pin 22 to Pins 8 and 21) ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Output Current into Outputs (Low) ..... 12 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-up Current ..... >200 mA

DC Programming Voltage ..... 13.0V

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +75°C        | 5V ±10%         |
| Military <sup>[5]</sup> | -55°C to +125°C     | 5V ±10%         |

## Electrical Characteristics Over the Operating Range

| Parameter        | Description  | Test Conditions   | Min.                      | Max.       | Units |   |
|------------------|--|---|---------------------------|------------|-------|---|
| V <sub>OH</sub>  | Output HIGH Voltage                                | V <sub>CC</sub> = Min.,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   | I <sub>OH</sub> = -3.2 mA | Commercial | 2.4   | V |
|                  |  |   | I <sub>OH</sub> = -2 mA   | Military   |       |   |
| V <sub>OL</sub>  | Output LOW Voltage                                 | V <sub>CC</sub> = Min.,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>   | I <sub>OL</sub> = 12 mA   | Commercial | 0.5   | V |
|                  |  |   | I <sub>OL</sub> = 8 mA    | Military   |       |   |
| V <sub>IH</sub>  | Input LOW Level                                    | Guaranteed HIGH Input, all Inputs <sup>[1]</sup>  | 2.2                       |            | V     |   |
| V <sub>IL</sub>  | Input LOW Level                                    | Guaranteed LOW Input, all Inputs <sup>[1]</sup>   |                           | 0.8        | V     |   |
| I <sub>IX</sub>  | Input Leakage Current                              | V <sub>SS</sub> < V <sub>IN</sub> < V <sub>CC</sub> , V <sub>CC</sub> = Max.  | -10                       | 10         | μA    |   |
| I <sub>OZ</sub>  | Output Leakage Current                             | V <sub>CC</sub> = Max., V <sub>SS</sub> < V <sub>OUT</sub> < V <sub>CC</sub>  | -40                       | 40         | μA    |   |
| I <sub>SC</sub>  | Output Short Circuit Current                       | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V <sup>[2]</sup>  | -30                       | -90        | mA    |   |
| I <sub>CC1</sub> | Standby Power Supply Current                       | V <sub>CC</sub> = Max., V <sub>IN</sub> = GND<br>Outputs Open   | Commercial                | 120        | mA    |   |
|                  |  |   | Military                  | 150        | mA    |   |
| I <sub>CC2</sub> | Power Supply Current at Frequency <sup>[6,8]</sup> | V <sub>CC</sub> = Max.<br>Outputs Disabled (In High Z State)<br>Device Operating at f <sub>MAX</sub><br>External (f <sub>MAX1</sub> ) | Commercial                | 180        | mA    |   |
|                  |  |   | Military                  | 200        | mA    |   |

## Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions                     | Min. | Max. | Units |
|------------------|--------------------|-------------------------------------|------|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | V <sub>IN</sub> = 2.0V @ f = 1 MHz  |      | 7    | pF    |
| C <sub>OUT</sub> | Output Capacitance | V <sub>OUT</sub> = 2.0V @ f = 1 MHz |      | 8    |       |

### Notes:

1. These are absolute values with respect to device ground and all over-shoots due to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V<sub>OUT</sub> = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

3. Tested initially and after any design or process changes that may affect these parameters.
4. Figure 4a test load used for all parameters except t<sub>EA</sub>, t<sub>ER</sub>, t<sub>PZX</sub> and t<sub>PXZ</sub>. Figure 4b test load for t<sub>EA</sub>, t<sub>ER</sub>, t<sub>PZX</sub>, t<sub>PXZ</sub>. Figure 4c shows test waveforms and measurement reference levels.
5. T<sub>A</sub> is the "instant on" case temperature.
6. Tested by periodic sampling of production product.

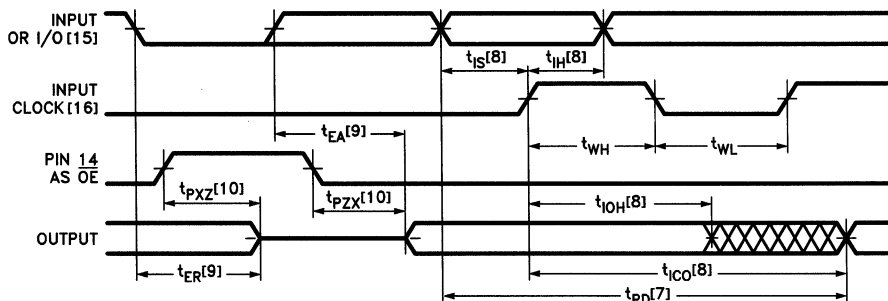


**Switching Characteristics Over the Operating Range<sup>[1]</sup>**

| Parameters            | Description   | Commercial |      |      |      | Military |      |      |      | Units |
|-----------------------|---|------------|------|------|------|----------|------|------|------|-------|
|                       |   | -20        |      | -25  |      | -25      |      | -30  |      |       |
|                       |   | Min.       | Max. | Min. | Max. | Min.     | Max. | Min. | Max. |       |
| $t_{PD}$              | Input to Output Propagation Delay <sup>[7]</sup>  |            | 20   |      | 25   |          | 25   |      | 30   | ns    |
| $t_{ICO}$             | Input Register Clock to Output Delay <sup>[8]</sup>   |            | 20   |      | 25   |          | 25   |      | 30   | ns    |
| $t_{IS}$              | Input or Feedback Setup Time to Input Register Clock <sup>[8]</sup>                             | 3          |      | 3    |      | 4        |      | 4    |      | ns    |
| $t_{IH}$              | Input Register Hold Time <sup>[8]</sup>   | 3          |      | 3    |      | 4        |      | 4    |      | ns    |
| $t_{EA}$              | Input to Output Enable Delay <sup>[4, 9]</sup>  |            | 20   |      | 25   |          | 25   |      | 30   | ns    |
| $t_{ER}$              | Input to Output Disable Delay <sup>[4, 9]</sup>   |            | 20   |      | 25   |          | 25   |      | 30   | ns    |
| $t_{PZX}$             | Pin 14 Enable to Output Enable Delay <sup>[4, 10]</sup>   |            | 15   |      | 20   |          | 20   |      | 25   | ns    |
| $t_{PXZ}$             | Pin 14 Disable to Output Disable Delay <sup>[4, 10]</sup>                                       |            | 15   |      | 20   |          | 20   |      | 25   | ns    |
| $t_{WH}$              | Input Clock Width High <sup>[6, 8]</sup>  | 10         |      | 10   |      | 10       |      | 12   |      | ns    |
| $t_{WL}$              | Input Clock Width Low <sup>[6, 8]</sup>   | 10         |      | 10   |      | 10       |      | 12   |      | ns    |
| $t_{IOH}$             | Output Data Stable Time from Input Register Clock Input <sup>[8, 14]</sup>                      | 3          |      | 3    |      | 4        |      | 4    |      | ns    |
| $t_{IOH} - t_{IH}$    | Output Data Stable Time This Device Minus I/P Reg Hold Time Same Device <sup>[11, 12, 14]</sup> | 0          |      | 0    |      | 0        |      | 0    |      | ns    |
| $t_{OH} - t_{IH} 33X$ | Output Data Stable Time Minus I/P Reg Hold Time 7C330 & 7C332 Device <sup>[13, 14]</sup>        | 0          |      | 0    |      | 0        |      | 0    |      | ns    |
| $t_{PE}$              | External Clock Period ( $t_{ICO} + t_{IS}$ ) <sup>[8]</sup>                                     | 23         |      | 28   |      | 29       |      | 34   |      | ns    |
| $f_{MAX1}$            | Maximum External Operating Frequency ( $1/(t_{ICO} + t_{IS})$ ) <sup>[8]</sup>                  | 43.4       |      | 35.7 |      | 34.4     |      | 29.4 |      | MHz   |
| $f_{MAX2}$            | Maximum Frequency Data Path <sup>[8]</sup>  | 50.0       |      | 40.0 |      | 40.0     |      | 33.3 |      | MHz   |

**Notes:**

7. Refer to Figure 8 configuration 1.
8. Refer to Figure 8 configuration 2.
9. Refer to Figure 8 configuration 3.
10. Refer to Figure 8 configuration 4.
11. Refer to Figure 8 configuration 5.
12. This specification is intended to guarantee that configuration 5 of Figure 8 with input registered feedback can be operated with all input register clocks controlled by the same source. These parameters are tested by periodic sampling of production product.
13. This specification is intended to guarantee interface compatibility of the other members of the CY7C330 family with the CY7C332. This specification is met for the devices noted operating at the same ambient temperature and at the same power supply voltage. These parameters are tested periodically by sampling of production product.
14. Preliminary specifications.

**Switching Waveforms**

**Notes:**

15. Because OE can be controlled by the  $\overline{OE}$  product term, input signal polarity for control of OE can be of either polarity. Internally the product term OE signal is active high.
16. Since the input register clock polarity is programmable, the input clock may be rising or falling edge triggered.

### AC Test Loads and Waveforms (Commercial)

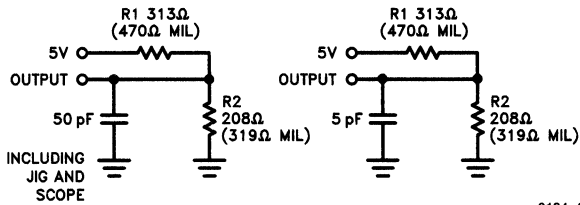


Figure 4a

Figure 4b

0134-6

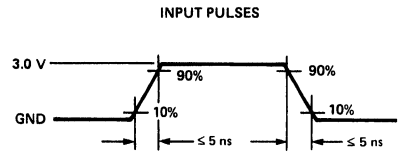
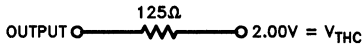


Figure 5. Input Pulses

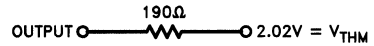
0134-7

Equivalent to: THÉVENIN EQUIVALENT (Commercial)



0134-8

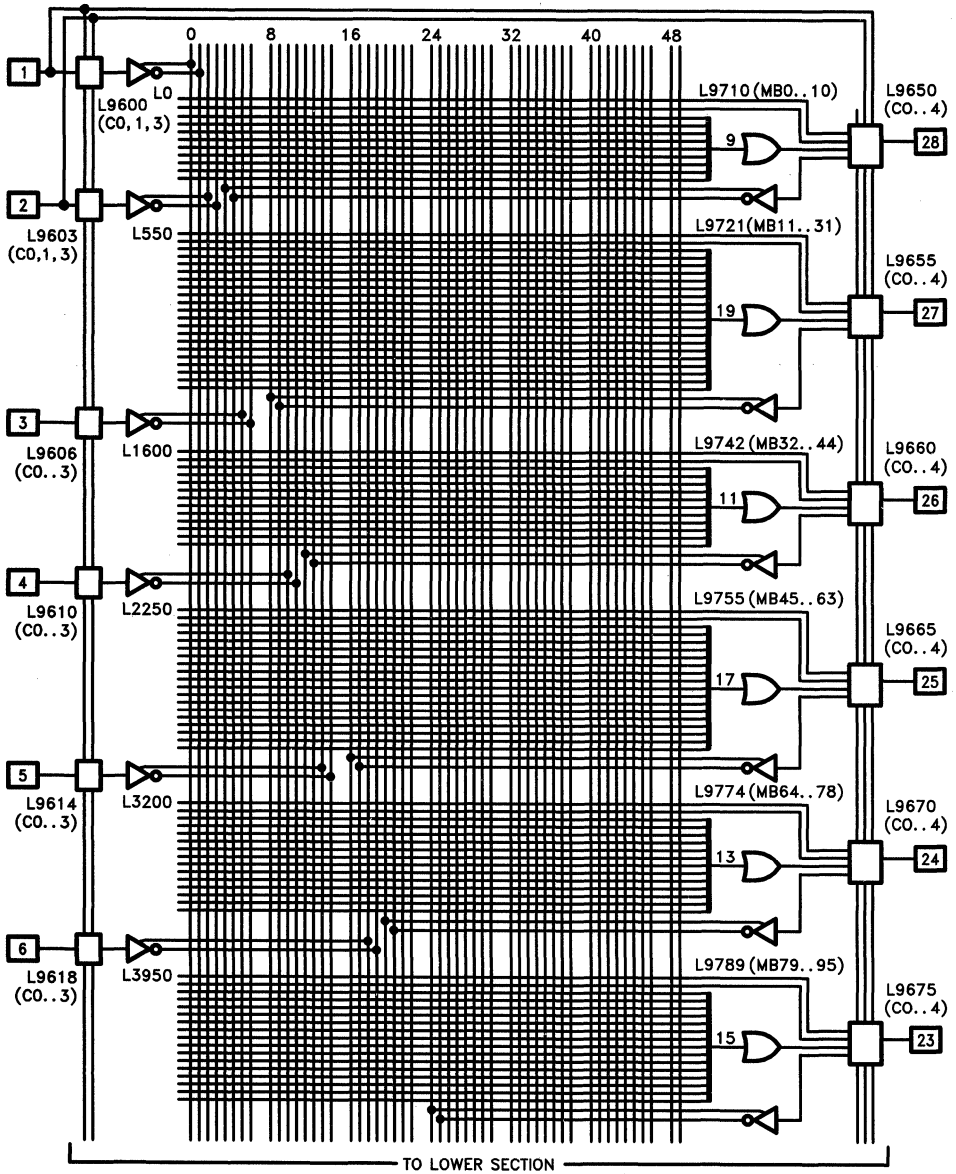
Equivalent to: THÉVENIN EQUIVALENT (Military)



0134-9

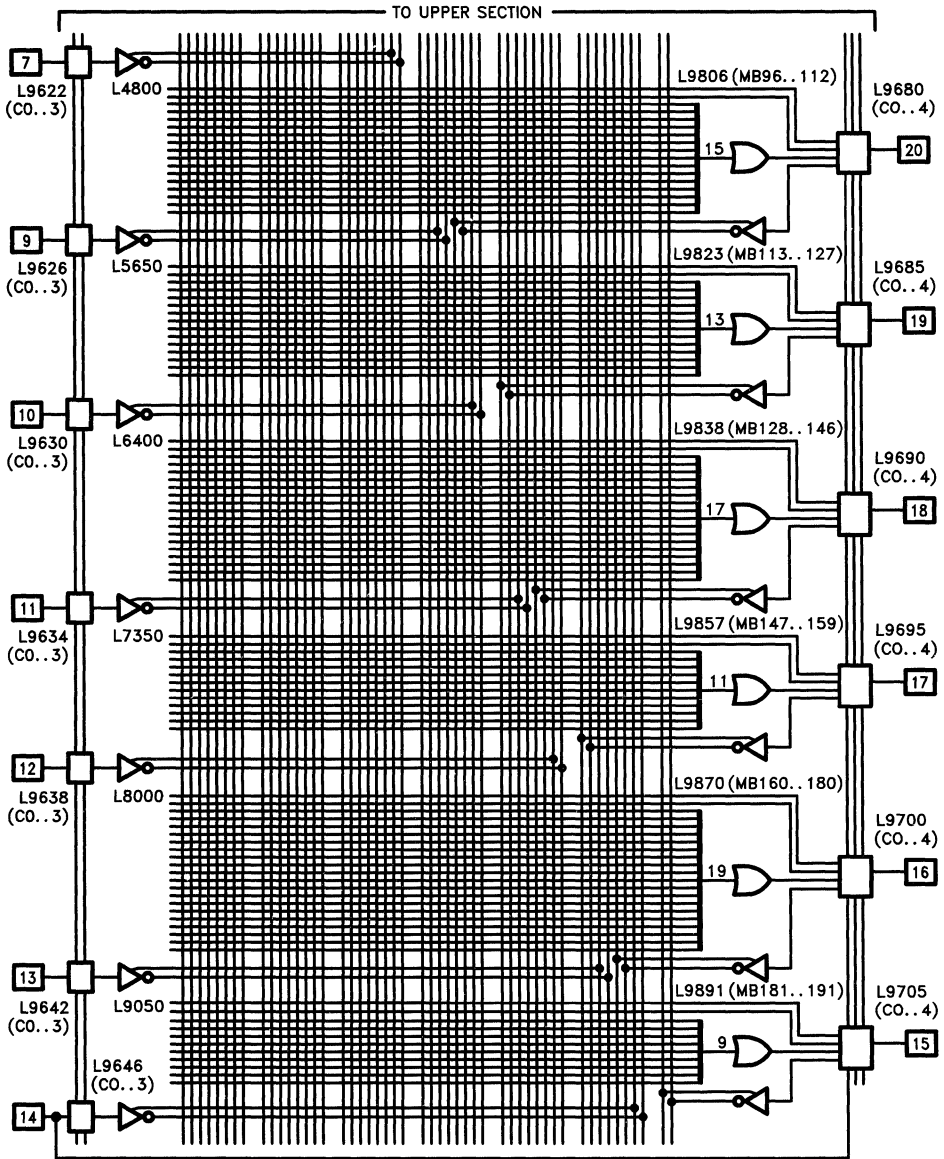
| Parameter    | $V_X$     | Output Waveform—Measurement Level |
|--------------|-----------|-----------------------------------|
| $tp_{XZ}(-)$ | 1.5V      |                                   |
| $tp_{XZ}(+)$ | 2.6V      |                                   |
| $tp_{ZX}(+)$ | $V_{thc}$ |                                   |
| $tp_{ZX}(-)$ | $V_{thc}$ |                                   |
| $t_{ER}(-)$  | 1.5V      |                                   |
| $t_{ER}(+)$  | 2.6V      |                                   |
| $t_{EA}(+)$  | $V_{thc}$ |                                   |
| $t_{EA}(-)$  | $V_{thc}$ |                                   |

Figure 4c. Test Waveforms and Measurement Levels



**CY7C332 Logic Diagram (Upper Half)**

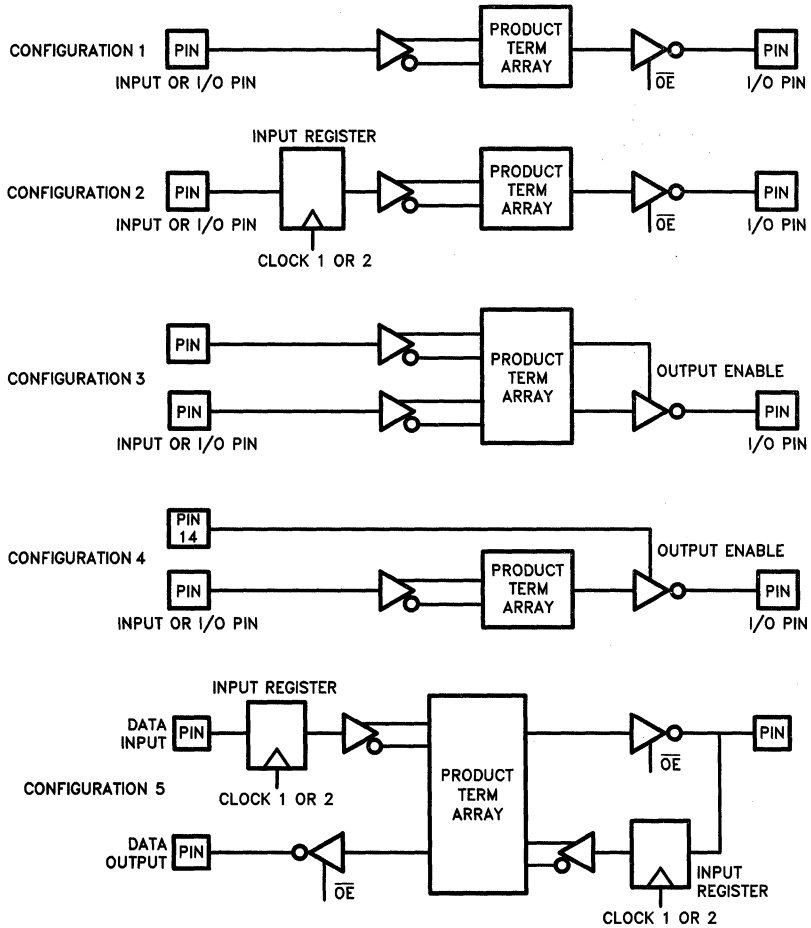
0134-16



**4**

**CY7C332 Logic Diagram (Lower Half)**

0134-17



0134-11

0134-18

Figure 6. Timing Configurations

**Ordering Information**

| ICC1 (max) | t <sub>CO</sub> /t <sub>PD</sub> (ns) | t <sub>IS</sub> (ns) | t <sub>IH</sub> (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------------------------------|----------------------|----------------------|---------------|--------------|-----------------|
| 120        | 20                                    | 3                    | 3                    | CY7C332-20PC  | P21          | Commercial      |
|            |                                       |                      |                      | CY7C332-20WC  | W22          |                 |
|            |                                       |                      |                      | CY7C332-20JC  | J64          |                 |
| 150        | 25                                    | 4                    | 4                    | CY7C332-25DMB | D22          | Military        |
|            |                                       |                      |                      | CY7C332-25WMB | W22          |                 |
|            |                                       |                      |                      | CY7C332-25LMB | L64          |                 |
|            |                                       |                      |                      | CY7C332-25TMB | T74          |                 |
| 120        | 25                                    | 3                    | 3                    | CY7C332-25PC  | P21          | Commercial      |
|            |                                       |                      |                      | CY7C332-25WC  | W22          |                 |
|            |                                       |                      |                      | CY7C332-25JC  | J64          |                 |
| 150        | 30                                    | 4                    | 4                    | CY7C332-30DMB | D22          | Military        |
|            |                                       |                      |                      | CY7C332-30WMB | W22          |                 |
|            |                                       |                      |                      | CY7C332-30LMB | L64          |                 |
|            |                                       |                      |                      | CY7C332-30TMB | T74          |                 |
|            |                                       |                      |                      | CY7C332-30QMB | Q64          |                 |

**4**



## Multiple Array MatriX High Density EPLDs

### Features

- Erasable, user-configurable CMOS EPLDs capable of implementing high density custom logic functions
- Advanced 0.8 micron double-metal CMOS EPROM technology
- Multiple Array MatriX Architecture optimized for speed, density and straightforward design implementation
  - Typical clock frequency = 50 MHz
  - Programmable Interconnect Array (PIA) simplifies routing
  - Flexible Macrocells increase utilization
  - Programmable clock control
  - Expander product terms implement complex logic functions
- MAX + PLUS™ development system eases design
  - Runs on IBM PC/AT™ and compatible machines
  - Hierarchical schematic capture with 7400 series TTL and custom Macrofunctions
  - State machine and Boolean entry
  - Graphical delay path calculator
  - Automatic error location
  - Timing simulation
  - Graphical interactive entry of waveforms

### General Description

The Cypress Multiple Array MatriX (MAX™) family of EPLDs provides a user-configurable, high-density solution to general purpose logic integration requirements. With the combination of innovative architecture and state of the art process, the MAX EPLDs offer LSI density, without sacrificing speed.

The MAX architecture makes it ideal for replacing large amounts of TTL SSI and MSI logic. For example, a 74161 counter utilizes only 3% of the 128 Macrocells available in the CY7C342. Similarly, a 74151 8 to 1 multiplexer consumes less than one percent of the over 1,000 product terms in the CY7C342. This allows the designer to replace 50 or more TTL packages with just one MAX EPLD. The family comes in a range of densities, shown below. By standardizing on a few MAX building blocks, the designer can replace hundreds of different 7400 series part numbers currently used in most digital systems.

The family is based on an architecture of flexible Macrocells grouped together into Logic Array Blocks (LABs). Within the LAB is a group of additional product terms called Expander Product Terms. These Expanders are used and shared by the Macrocells, allowing complex functions, up to 35 product terms, to be easily implemented in a single Macrocell. A Programmable Interconnect Array (PIA) globally

routes all signals within devices containing more than one LAB. This architecture is fabricated on the Cypress advanced 0.8 micron double layer metal CMOS EPROM process, yielding devices with 3 times the integration density at twice the system clock speed of the largest current generation EPLD.

The density and flexibility of the CY7C340 family is accessed using the MAX + PLUS development system. A PC based design system, MAX + PLUS is optimized specifically for the CY7C340 family architecture, providing efficient design processing within the time it takes to erase an EPLD. A hierarchical schematic entry mechanism is used to capture the design. State Machine, Truth Table and Boolean Equation entry mechanisms are also supported, and may be mixed with schematic capture. The powerful Design Processor performs minimization and logic synthesis, then automatically fits the design into the desired EPLD. Design verification is done using a timing simulator, which provides full A.C. simulation, along with an interactive graphic waveform editor package to speed waveform creation and debugging. During design processing a sophisticated automatic error locator shows exactly where the error occurred by popping the designer back into the schematic at the exact error location.

### MAX Family Members

| Feature                    | CY7C344    | CY7C343    | CY7C345    | CY7C342    |
|----------------------------|------------|------------|------------|------------|
| Macrocells                 | 32         | 64         | 128        | 128        |
| MAX Flip-Flops             | 32         | 64         | 128        | 128        |
| MAX Latches <sup>[1]</sup> | 64         | 128        | 256        | 256        |
| MAX Inputs <sup>[2]</sup>  | 23         | 35         | 35         | 59         |
| MAX Outputs                | 16         | 28         | 28         | 52         |
| Packages                   | 28D<br>28J | 44J<br>40D | 44J<br>40D | 68J<br>68G |

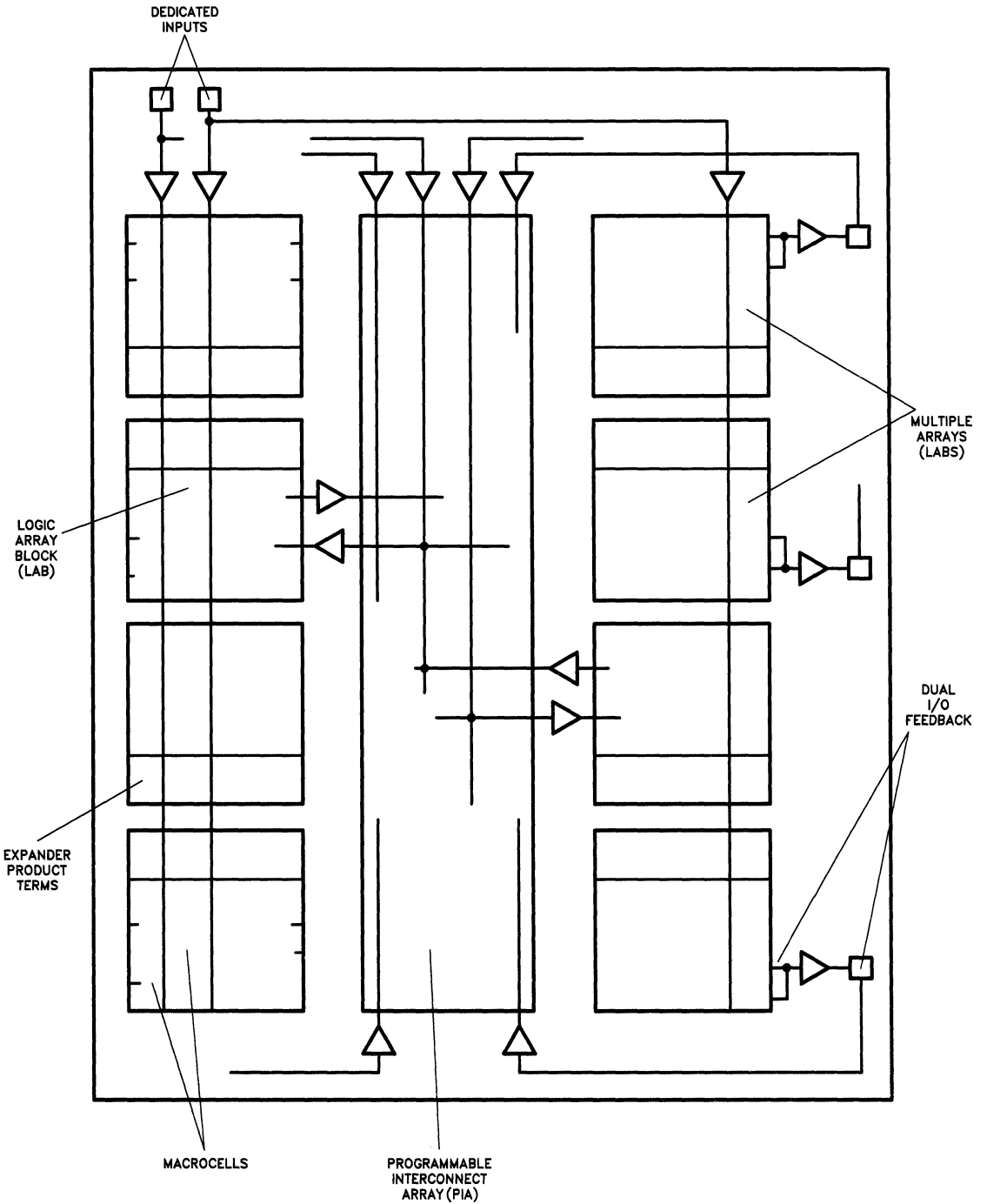
Key: D—DIP J—J-Lead Chip Carrier G—Pin Grid Array

Notes:

1. When all Expander Product Terms are used to implement latches.

2. With one output.

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 IBM® is a registered trademark of International Business Machines Corporation.  
 IBM PC/AT™ is a trademark of International Business Machines Corporation.  
 MAX™ and MAX + PLUS™ are trademarks of Altera Corporation.  
 Drawings courtesy of Altera Corporation.



4

Figure 1. Key MAX Features



## Functional Description

### The Logic Array Block

The Logic Array Block, shown in *Figure 2*, is the heart of the MAX architecture. It consists of a Macrocell Array, Expander Product Term Array, and an I/O Block. The number of Macrocells, Expanders, and I/O vary, depending upon the device used. Global feedback of all signals is

provided within an LAB, giving each functional block complete access to the LAB resources. The LAB itself is fed by the Programmable Interconnect Array and dedicated input bus. The feedbacks of the Macrocells and I/O pins feed the PIA, providing access to them by other LABs in the device. The CY7C340 family EPLDs having a single LAB use a global bus, and a PIA is not needed.

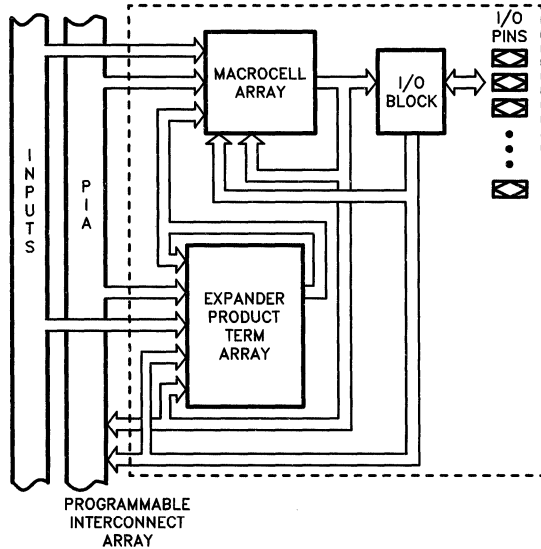


Figure 2. LAB Block Diagram

0138-3

**Functional Description** (Continued)

**The MAX Macrocell**

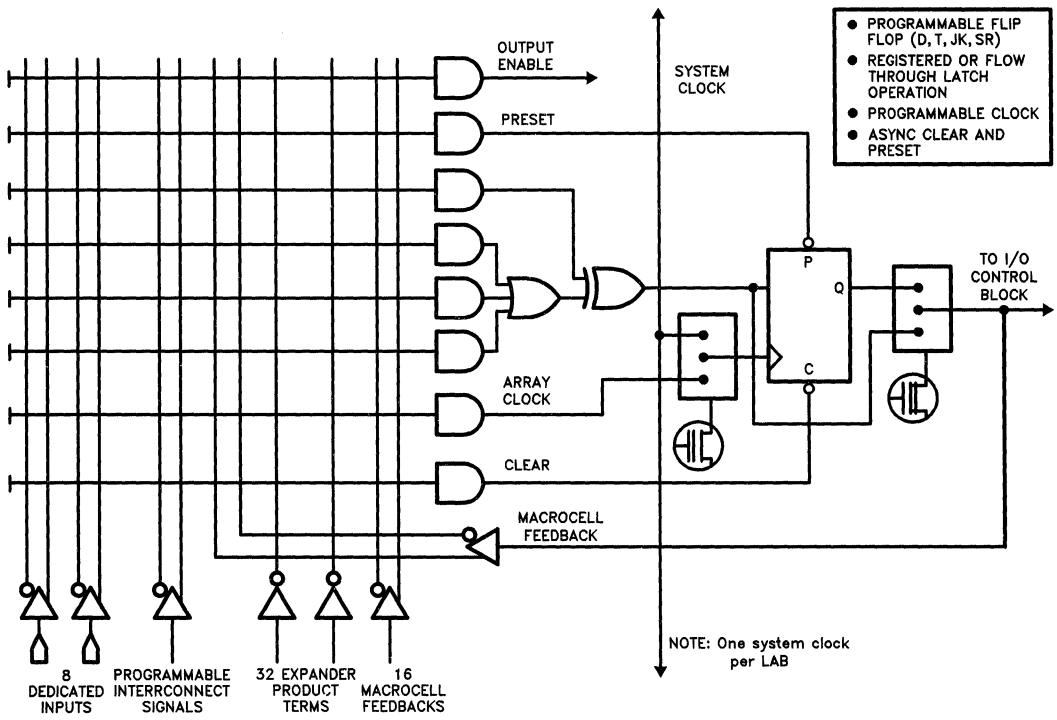
Traditionally, PLDs have been divided into either PLA (programmable AND, programmable OR), or PAL™ (programmable AND, fixed OR) architectures. PLDs of the latter type provide faster input-to-output delays, but can be inefficient due to fixed allocation of product terms. Statistical analysis of PLD logic designs has shown that 70% of all logic functions (per Macrocell) require 3 product terms or less.

The Macrocell structure of MAX has been optimized to handle variable product term requirements. As shown in *Figure 3*, each Macrocell consists of a product term array and a configurable register. In the Macrocell, combinatorial logic is implemented with 3 product terms OR'ed together, which then feeds an XOR gate. The second input to the XOR gate is also controlled by a product term, providing the ability to control active high or active low logic. The MAX + PLUS software will also use this gate to implement complex mutually exclusive-OR arithmetic logic functions, or to do DeMorgan's Inversion, reducing the number of product terms required to implement a function.

If more product terms are required to implement a given function, they may be added to the Macrocell from the Expander Product Term Array. These additional product terms may be added to any Macrocell, allowing the designer to build gate intensive logic, such as address decoders, adders, comparators, and complex state machines, without using extra Macrocells.

The register within the Macrocell may be programmed for either, D, T, JK, or SR operation. It may alternately be configured as a flow-through latch for minimum input to output delays, or by-passed entirely for purely combinatorial logic. In addition, each register supports both asynchronous preset and clear, allowing asynchronous loading of counters or shift registers, as found in many standard TTL functions. These registers may be clocked with a synchronous system clock, or clocked independently from the logic array.

4



**Figure 3. Macrocell Block Diagram**

0138-4

## Functional Description (Continued)

### Expander Product Terms

The Expander Product Terms, as shown in *Figure 4*, are fed by the Dedicated Input Bus, the Programmable Interconnect Array, the Macrocell Feedback, Expanders themselves, and the I/O pin feedbacks. The outputs of the Expanders then go to each and every product term in the Macrocell Array. This allows Expanders to be "shared" by the product terms in the Logic Array Block. One Expander may feed all Macrocells in the LAB, or even multiple product terms in the same Macrocell. Since these Expanders feed the secondary product terms (Preset, Clear, Clock, and Output Enable) of each Macrocell, complex logic functions may be implemented without utilizing another Macrocell. Likewise, Expanders may feed and be shared by other Expanders, to implement complex multi-level logic and input latches.

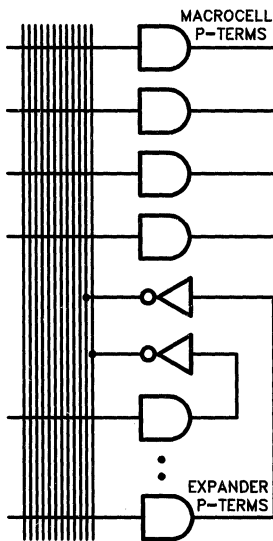


Figure 4

0138-5

### The I/O Block

Separate from the Macrocell Array is the I/O Control Block of the LAB. *Figure 5* shows the I/O block diagram. The tristate buffer is controlled by a Macrocell product term, and drives the I/O pad. The input of this buffer comes from a Macrocell within the associated LAB. The feedback path from the I/O pin may feed other blocks within the LAB, as well as PIA.

By decoupling the I/O pins from the flip-flops, all the registers in the LAB are "buried", allowing the I/O pins to be used as dedicated outputs, Bi-directional outputs or as additional dedicated inputs. Therefore, applications requiring many buried flip-flops, such as counters, shift registers, and state machines, no longer consume both the Macrocell register and the associated I/O pin, as in earlier devices.

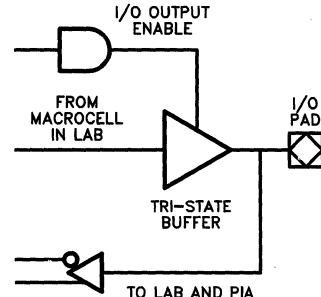


Figure 5. I/O Control

0138-6

### The Programmable Interconnect Array

A major problem which has limited PLD density and speed has been signal routing, i.e. getting signals from one Macrocell to another. For smaller devices, a single array is used and all signals are available to all Macrocells. But, as the devices increase in density, the number of signals being routed becomes very large, increasing the amount of silicon used for interconnections. Also, because the signal must be global, the added loading on the internal connection path reduces the overall speed performance of the device. The MAX architecture solves these problems. It is based on the concept of small, flexible Logic Array Blocks, which, in the larger devices, are interconnected by a Programmable Interconnect Array, or PIA.

The Programmable Interconnect Array solves interconnect limitations by routing only the signals needed by each LAB. The architecture is designed so that every signal on the chip is within the PIA. The PIA is then programmed to give each LAB access to the signals that it requires. Consequently, each LAB receives only the signals needed. This effectively solves any routing problems that may arise in a design, without degrading the performance of the device. Unlike masked or programmable gate arrays, which induce variable delays dependent on routing, the PIA has a fixed from point to point. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic.

**Functional Description (Continued)**

**Family Members**

The CY7C340 family is an entire set of modular building blocks, optimized for high speed and high density. Listed below are the 4 current members of the family.

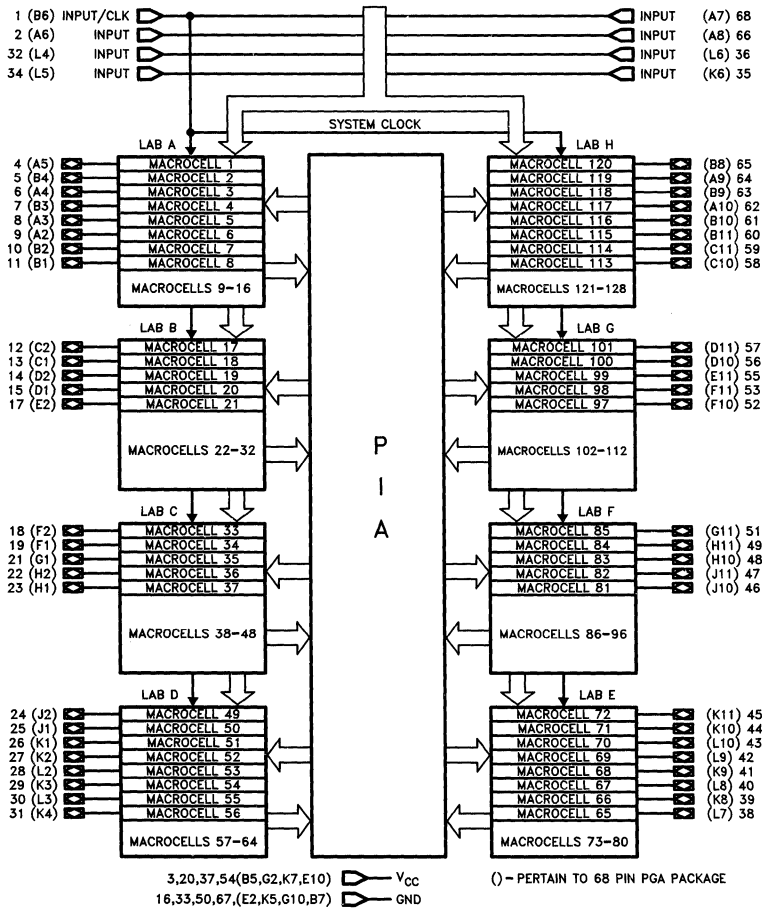
**CY7C342**

- 128 Macrocells in 8 LABs
- 8 dedicated inputs, 52 bi-directional I/O pins
- Programmable Interconnect Array
- Available in 68-pin JLCC, PLCC and PGA

The 128 Macrocells in the CY7C342 are divided into 8 Logic Array Blocks, 16 per LAB. There are 256 Expander Product Terms, 32 per LAB, to be used and shared by the Macrocells within each LAB. Each LAB is interconnected with a Programmable Interconnect Array, allowing all signals to be routed throughout the chip.

The speed and density of the CY7C342 allows it to be used in a wide range of applications, from replacement of large amounts of 7400 series TTL logic, to complex controllers and multi-function chips. With greater than 25 times the functionality of 20-pin PLDs, the CY7C342 allows the replacement of over 50 TTL devices. By replacing large amounts of logic, the CY7C342 reduces board space, part count, and increases system reliability.

4



**Figure 6. CY7C342 Block Diagram**

**Features**

| Inputs | I/O Pins | LABs | Macrocells per LAB | Total Macrocells | Expanders | PIA |
|--------|----------|------|--------------------|------------------|-----------|-----|
| 8      | 52       | 8    | 16                 | 128              | 256       | Yes |

0138-7

**Functional Description (Continued)**

**CY7C345**

- 128 Macrocells in 8 LABs
- 8 dedicated inputs, 28 bi-directional I/O pins
- 256 Expander Product Terms
- Programmable Interconnect Array
- Available in 40-pin CDIP, PDIP, and 44-pin JLCC or PLCC

The CY7C345 packs the same LSI density of the CY7C342 into a smaller, 40-pin DIP or 44-pin JLCC package. Designed for applications in which large amounts of logic

must be packed into a very small area, the CY7C345 is ideally suited for applications which require large amounts of buried logic.

It has the same number of Macrocells and expanders as the CY7C345, and a Programmable Interconnect Array to allow communications between the LABs. Each LAB has an I/O block, with LABs A, D, E and H having 4 Bi-directional tri-stateable I/O pins, and the rest having 3 I/O pins. Like all other EPLDs in the MAX family, these I/O pins support dual feedback. In this way any Macrocells can be buried, with only the output of Macrocells needed off-chip connected to I/O pins.

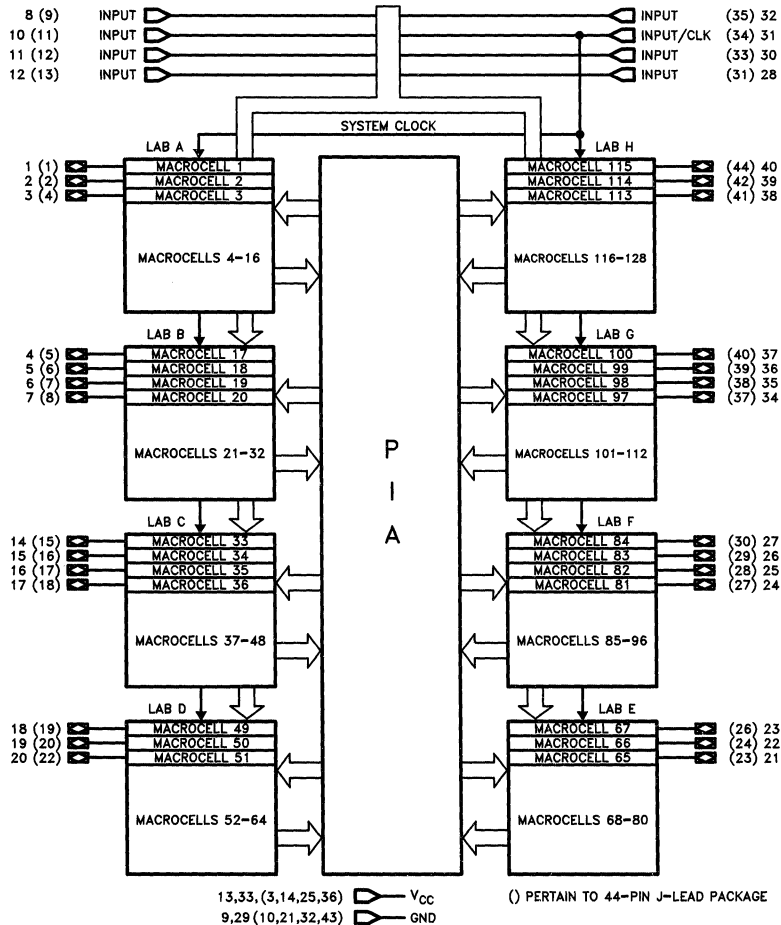


Figure 7. CY7C345 Block Diagram

0138-B

**Features**

| Inputs | I/O Pins | LABs | Macrocells per LAB | Total Macrocells | Expanders | PIA |
|--------|----------|------|--------------------|------------------|-----------|-----|
| 8      | 28       | 8    | 16                 | 128              | 256       | Yes |

**Functional Description (Continued)**

**CY7C343**

- 64 MAX Macrocells in 4 LABs
- 8 dedicated inputs, 28 tri-stateable, bi-directional I/O pins
- Programmable Interconnect Array
- Available in 40-pin CDIP, PDIP, and 44-pin JLCC, PLCC

The CY7C343 block diagram is shown in *Figure 8*. It has 16 Macrocells and 32 Expander Product Terms in each of its 4 Logic Array Blocks. Decoupled from the Macrocells

in the LABs, each I/O control block has 7 I/O pins. Therefore, if each I/O pin was fed by a Macrocell, there are still 9 buried Macrocells per LAB that may be used for embedded logic. The signals generated within each LAB are routed to every LAB through the Programmable Interconnect Array.

The CY7C343 is perfect for designs with large I/O requirements, along with healthy amounts of buried logic. Excellent for a wide range of applications, the CY7C343 can reduce board space by absorbing large amounts of glue logic. Due to the large number of I/O pins, 16-bit data paths are no problem.

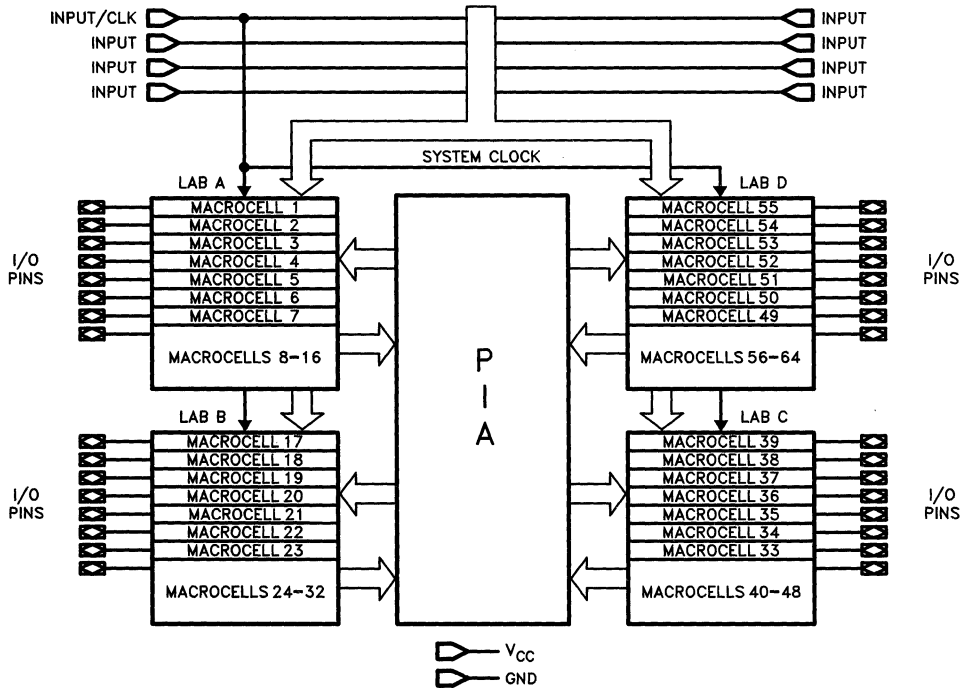


Figure 8. CY7C343 Block Diagram

0138-9

**Features**

| Inputs | I/O Pins | LABs | Macrocells per LAB | Total Macrocells | Expanders | PIA |
|--------|----------|------|--------------------|------------------|-----------|-----|
| 8      | 28       | 4    | 16                 | 64               | 128       | Yes |

**Functional Description (Continued)**

**CY7C344**

- High performance, high density replacement for TTL, 74HC, and custom logic
- 32 Macrocells, 64 Expander Product Terms in one LAB
- 8 dedicated inputs, 16 I/O pins
- Small outline 28-pin 300 mil CDIP, PDIP, or 28-pin JLCC, PLCC package

Available in a 28-pin 300 mil DIP or JLCC, the CY7C344 represents the densest EPLD of this size. 8 dedicated inputs and 16 bi-directional I/O pins communicate to one Logic Array Block. In the CY7C344 LAB there are 32

Macrocells and 64 Expander Product Terms. *Figure 9* shows that even if all of the I/O pins are being driven by Macrocells, there are still 16 "buried" Macrocells available. All inputs, Macrocells and I/O pins are interconnected within the LAB.

The speed and density of the CY7C344 makes it a natural for all types of applications. With just this one device, the designer can implement complex state machines, registered logic, and combinatorial "glue" logic, without using multiple chips. This architectural flexibility allows the CY7C344 to replace multi-chip TTL solutions, whether they are synchronous, asynchronous, combinatorial, or all three.

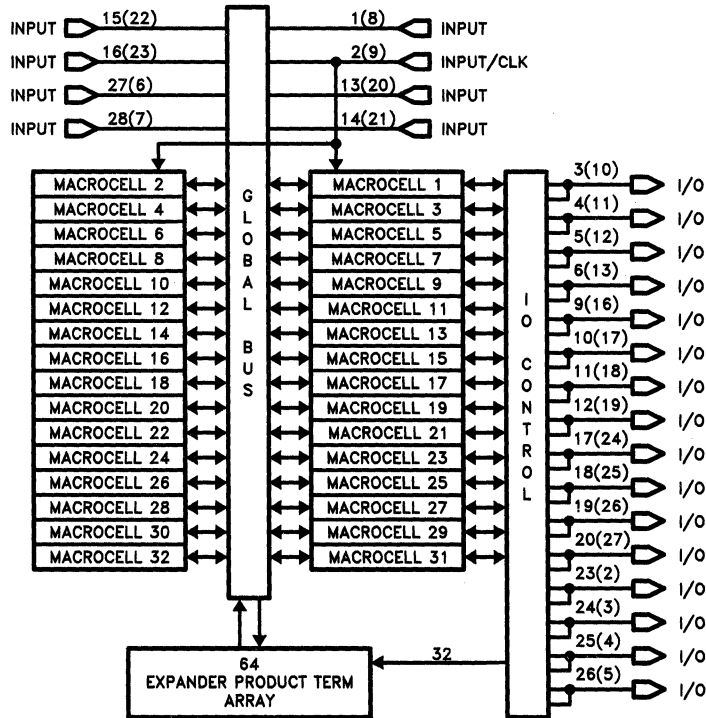


Figure 9. CY7C344 Block Diagram

0138-12

Note:  
Figures within ( ) pertain to J-leaded packages.

**Features**

| Inputs | I/O Pins | LABs | Macrocells per LAB | Total Macrocells | Expanders | PIA |
|--------|----------|------|--------------------|------------------|-----------|-----|
| 8      | 16       | 1    | 32                 | 32               | 64        | No  |

## MAX + PLUS™ Development System

### General Description

The MAX + PLUS Development System represents a complete hardware and software solution for implementing designs in the Cypress CY7C340 family of EPLDs.

MAX + PLUS is a sophisticated Computer Aided Design (CAD) system that includes design entry, design simulation, and device programming. Hosted on an IBM PC/AT or compatible machine. MAX + PLUS gives the designer the tools to quickly and efficiently implement complex logic designs. A block diagram is shown in *Figure 10*.

Designs are entered in MAX + PLUS using a hierarchical graphic editor. This editor has such features as multiple windows, multiple zoom levels, unlimited hierarchy levels, symbol editing, and a library of 7400 series devices in addition to basic SSI gate and register primitives. Also available is a Timing Calculator, in which the designer may pick two places in the schematic, and the software will display typical timing between those two points. Boolean Equation, Netlist, State Machine, and Truth Table entry mechanisms

may be used in conjunction with the graphic editor, giving added flexibility to the design environment.

In addition to a hierarchical design environment, MAX + PLUS has a sophisticated processing engine to exploit the CY7C340 family architecture. MAX + PLUS uses an advanced logic synthesizer and heuristic rules to process a design into a file for programming and/or simulation.

MAX + PLUS features a powerful event-driven simulator which displays typical timing results in an interactive waveform editor display. In this waveform editor, input vector waveforms may be directly modified and a new simulation run immediately.

Unlike most design environments, MAX + PLUS is unified, with all sections controlled by the Supervisor and Data Base Manager. By unifying the software, MAX + PLUS can offer an automatic error locator. If a design rule has been violated, the error processor will list an error message, the probable cause, and pop the designer into the schematic to the exact node where the mistake was made.

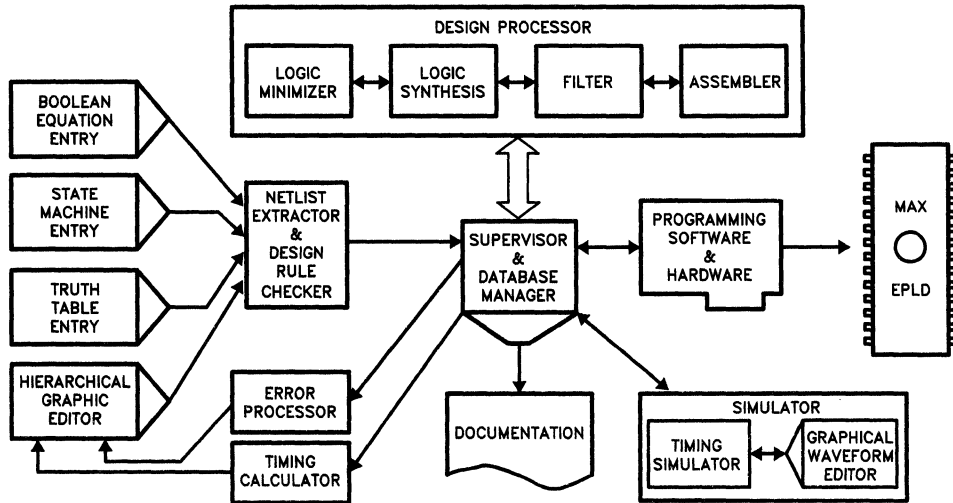


Figure 10. MAX + PLUS Block Diagram

0138-11



## MAX + PLUS Development System (Continued)

### Design Entry

Design entry is easily accomplished with MAX + PLUS. MAX + PLUS provides multiple entry mechanisms, including traditional Boolean equation entry. Also available are State Machine and Truth Table entry, using a high-level state machine language. Because the CY7C340 family of EPLDs offer the designer large amounts of logic capability, a Hierarchical Graphic Editor has been provided to ease the design process.

### Graphic Editor

The hierarchical design approach used by the graphic editor allows the designer to work with either a top-down or a bottom-up approach. The top down method allows the designer to start with a high level block diagram, and then move down and design each block individually. The bottom up method allows the simulation and verification of small building blocks, which may then be pieced together into a final design.

The Graphic Editor is mouse driven and uses pull down menus or single keystrokes to enter commands. Aiding in the design task is a library of 7400 series MSI and SSI logic gates. The designer may use these and/or create his own custom symbols. Custom functions are easily created in the hierarchy by first designing the function. Then a symbol is made, which represents that schematic. In this way a custom function may be used in multiple places in the current design, or saved and used in subsequent designs.

The function of any symbol created may be defined using graphic entry, state machine, Boolean, or truth table descriptions. This provides a wide range of flexibility for the designer, allowing Boolean equations to be combined with state machine entry in a hierarchical schematic.

The timing calculator within the graphic editor gives the designer instant feedback concerning timing delays inherent in a path. By placing two probes on different parts of the schematic, the designer immediately knows the worst case timing of the processed design. This is a valuable addition for design debugging and documentation.

### Design Processor

After the design is entered, a push of the mouse button invokes the powerful MAX + PLUS processor. First a netlist is extracted from the complete hierarchical design. During the extraction process, design rules are checked for any errors, and if errors are found, the error processor leads the designer directly to the schematic location where the error occurred. The extracted design is placed in the database, and the design is ready to be processed.

The versatile MAX architecture, with its Expander Product Terms and mutual exclusivity, requires a dedicated processor to take optimal advantage of the MAX features, one that does much more than simplify logic. The logic synthesizer in MAX + PLUS uses several knowledge-based synthesis rules to factor and map logic onto the multi-level MAX architecture. It will then choose the mapping approach that ensures the most efficient use of the silicon

resources. The synthesizer will also remove any unused logic or registers from the design.

The next module in the design processor is the fitter. Its function is similar to a placement and router used in semi-custom gate arrays. Using heuristic rules, it takes the synthesized design and optimally places it within the chosen CY7C340 EPLD. With the larger devices, it also routes the signals across the Programmable Interconnect Array, freeing the designer from interconnection issues.

### Timing Simulator

Rounding out the software offering is a powerful timing simulator to aid in the verification and debugging of designs. The simulator is a graphical, event driven software package that yields true, worst case timings based upon user-defined input vectors.

Waveforms may be viewed using a Graphical Waveform Editor, which allows graphical definitions and editing of input waveforms. The designer can define his input waveform using the mouse to draw the actual waveform as a function of time. There are also powerful waveform editing commands, all menu driven, to aid in the development of the input vectors. Such options as pre-defining, copying and repeating waveforms are all available to the user. If graphical definition is not desired, there is a powerful vector description language for developing input vectors.

The simulator itself has all the capabilities one would expect from this type of design environment. Observing buried nodes, accessing flip-flop control inputs, and initializing and forcing nodes to specified values are all available within the timing simulator. The user may also specify breakpoints during the simulation itself, and execute subroutines dependent upon the breakpoints. All of these tools aid the designer in verifying and debugging the design, even before breadboarding.

The simulator also has advanced A.C. timing detection. The software will warn the user when setup and hold times to flip flops are being violated, and when there is oscillation present in the simulation. Also, the user may define a minimum pulse width, in which any pulse within the design that is smaller than a certain size will be classified as a glitch and the designer will be informed.

### Supervisor and Error Processor

All facets of the MAX + PLUS system are overseen by the Supervisor and Data Base Manager. By tying all of the software together, the designer has a unified operational environment. All the software has the same "look and feel", so that complex commands and languages are not needed.

Automatic error processing is an added benefit of this approach. If an error occurs during the processing of the design, the software will automatically tell the user what the error is, and the probable cause.

Then, by pressing a single key, the software will automatically go the schematic in the graphic editor and pinpoint the location of the error.



# Ultra High Speed State Machine EPLD

## Features

- High speed: 125 MHz internal processing
  - Multiple, concurrent processes
  - Multiway branch or join
  - Full input field decode
- 32 synchronous macrocells
- Skew-controlled, OR output array
  - Outputs are sum of states like PLA
  - 3 ns skew overall
- Metastable hardened input registers
  - 10 year MTBF metastable
  - Configurable as 0, 1 or 2
  - Clock enables on all input registers
- 8 to 12 inputs, 10 to 14 outputs, 1 clock
- Programmable clock doubler and conditioner
  - 'Squares up' input clock
- Security fuse
- Space saving 28 pin slim-line DIP package; also available in 28 pin PLCC
- Low power
  - 140 mA max at 125 MHz
- UV-eraseable and reprogrammable
- Programming and operation 100% testable

## Product Characteristics

The CY7C361 is a CMOS eraseable, programmable logic device (EPLD) with very high speed sequencing and arbitration capabilities.

Applications include: cache and I/O subsystem control for high speed microprocessor based systems, control of high speed numeric processors, and control of asynchronous systems including dataflow organizations.

An onboard clock doubler and conditioning circuit allows the device to operate at 125 MHz based on a 62.5 MHz input reference. The same circuit guards against asymmetric clock wave-

forms and thus allows for the use of a clock with an imperfect duty cycle. The CY7C361 has two arrays which serve in function similar to the arrays in a PLA except that the registers are placed between the two arrays and the long feedback path of the PLA is eliminated.

In the CY7C361, the state information is contained in 32 macrocells sandwiched between the input and output arrays. The current state information is fed back in time to keep up with the 125 MHz operating frequency.

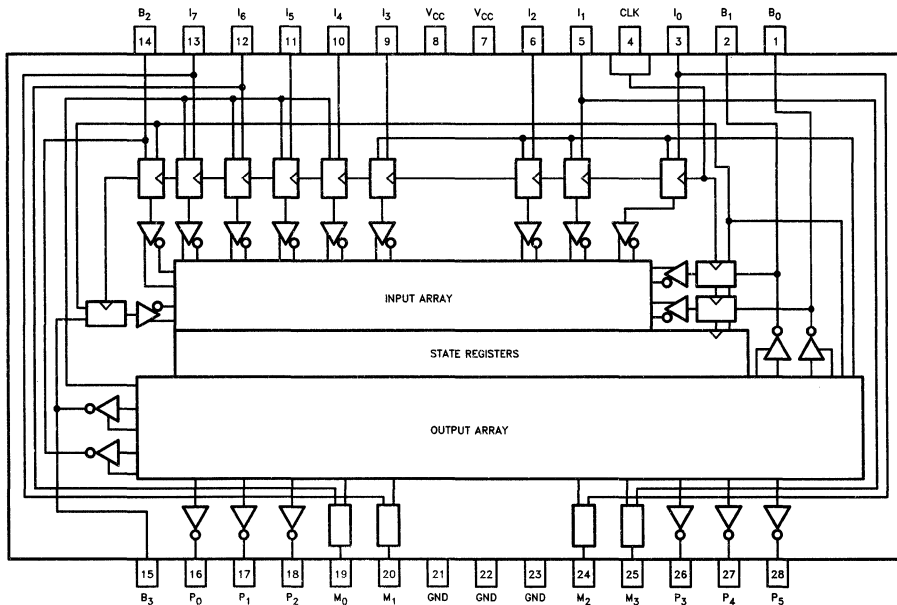
The output array performs an OR function over the state macrocell outputs. The signals from the output array are connected to 14 outputs; in addition they are connected to 3 groups of input macrocells to act as clock enables.

## Input Macrocells

The CY7C361 has 12 input macrocells. Each macrocell can be configured to have 0, 1 or 2 registers in the path of the input data. In the configuration

4

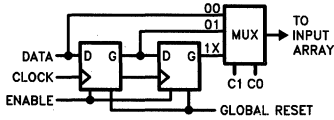
## Block Diagram



0165-1

## Product Characteristics (Continued)

where there is no input register, the setup time requirement is largest. In the single register configuration, the setup time is less than half. The double register configuration is used for asynchronous inputs.



**Figure 1. Input Macrocell**

0165-3

### Input Register Enables

The input macrocells are divided into 3 groups, each of which has a register clock enable signal coming from the output array. The purpose of the enable signal is to allow the inputs to be sampled at times controlled by the state of the device.

There is one enable signal per group of input macrocells. The assignment of enable signal node numbers to input macrocell groups is as follows:

| Input Nodes  | Enable Node |
|--------------|-------------|
| 3, 5, 6, 9   | 29          |
| 10,11,12,13  | 30          |
| 1, 2, 14, 15 | 31          |

When the enable node is true, data is clocked into the registers of the input macrocells on the rising edge of the internal global clock.

### Metastable Immunity

A high level of metastable immunity is afforded in the double register configuration. The CY7C361 input registers are of fast CMOS and resolve inputs in a minimal amount of time. With all inputs switching at the maximum frequency, one metastable event capable of violating the setup time window of the second input register occurs every 10 years. The probability of failure for the configured state machine is much lower than this calculation suggests, because there are more registers in the device and thus more decision time is allowed. No state machine failures due to metastable phenomena will be observed if the maximum frequency and double register operating mode are used.

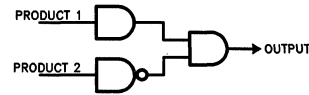
The CY7C361 is thus a superior device for constructing state machines requiring arbitration.

### Input Array

The input array has 41 condition decoders: one global reset decoder, 8 local reset decoders, and 32 macrocell decoders. The array has 44 true/complement inputs or 88 inputs in total; for speed reasons, the feedback signals are folded.

Folding or partitioning of the feedback part of the array reduces the number of inputs per decoder to 56. Because of the way the feedback signals are used, this array reduction has minimal impact on utility.

The CY7C361 condition decoder is shown in *Figure 2*. In a conventional PLA or PAL device, only PRODUCT 1 would be present in the first array and the output and feedback would be encoded by a second programmable or fixed OR array. The speed of state machines made from these conventional devices is limited mainly by the feedback path.

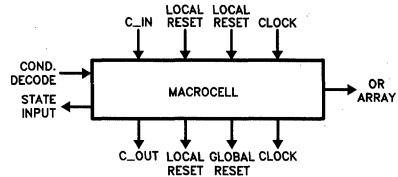


**Figure 2. Condition Decoder**

0165-4

The Condition Decoder of the CY7C361 forms a product of a product and a sum over the input field. Since there is immediate feedback information in the input field, multi-way fork and join operations can be performed using this type of condition decoder. State transitions can be made in half the time because there is no "state encoding" delay.

### State Machine Macrocells

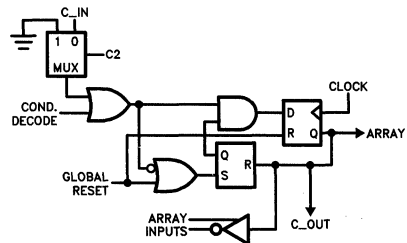


**Figure 3. CY7C361 Macrocell**

0165-5

The CY7C361 has 32 state Macrocells. The state Macrocells each have a single condition decode and share a common clock and global reset condition. For each 4 macrocell group there is a local reset condition.

There are 3 Macrocell configurations, named START, TERMINATE and TOGGLE. The purpose of the START configuration is to create a "token" based on a condition decode. The purpose of the TERMINATE configuration is to capture a token and maintain it until a particular condition is decoded, then terminate the token. The TOGGLE configuration is used to make counters.



C1,C0 = 0,1: START

**Figure 4**

0165-6

The start configuration is shown in *Figure 4*.

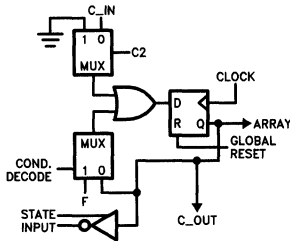
The start configuration creates a token at the leading edge of the condition decode or C\_IN. The token is represented by a true output on the macrocell register going to the output array and back as feedback to the input array. The CY7C361 consists of multiple machines or processes running concurrently, each with zero, one or more tokens active at a given time. As the output field is independent, the programmed pattern in the two arrays is one to one translatable to microcode. The microcode is concurrent in operation.

In addition to the main register going to the array, there is an R-S latch in the feedback path. The purpose of the R-S latch is to convert the input condition to a pulse.

**Product Characteristics (Continued)**

In operation, the start macrocell starts from a reset condition (array input = FALSE). When a condition decode “fires” or a token carries in (C\_IN), the register output (Q going to array) goes true for exactly one cycle. The OR of the condition decode and the C\_IN signal must go FALSE before the start configuration can “fire” again.

Configuration bit C2 is used in all state macrocells to select C\_OUT to be active (C2 = 1) or inactive (C2 = 0).



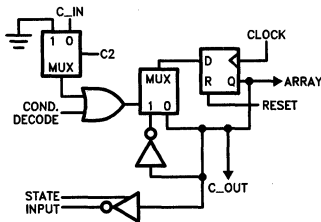
C0,C1 = 1,0: TERMINATE

0165-7

**Figure 5**

Figure 5 shows the terminate configuration which is used to maintain state tokens until a condition occurs.

In operation, the terminate configuration “captures” a token via. C\_IN and the OR gate. The condition decode is normally false or 0 so the token circulates and the register stays set. When the condition decode “fires”, the register resets.



C0,C1 = 11: TOGGLE

0165-8

**Figure 6**

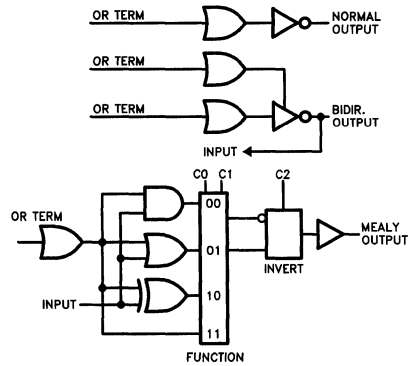
The third configuration, TOGGLE, is for counting and signalling. If the condition decode or the C\_IN signal is true, then the register will toggle. The TOGGLE configuration is intended to make counters and state machines with simple control requirements.

There is one local reset signal for each group of 4 macrocells. The local reset condition decoders will only work with TOGGLE configurations.

**The Output Section**

There are 3 types of outputs: normal, bidirectional and Mealy. All 3 types can function as normal outputs, but two types—the bidirectional type and the Mealy type—can be used for other purposes. The bidirectional type can be used as an input and the Mealy type can be used as a fast combinational output.

The different types of output structures are shown in Figure 7. Note that the only output type that has configuration information to be programmed is the Mealy type.



**Figure 7. Output Types**

0165-9

A normal output signal from the device is a boolean sum of a subset of the macrocell outputs. The subset selection is programmed into the output array. The number of state machines in the device, and the output mappings of each are determined by the user. The architecture is thus “horizontally divisible” and offers advantages in coding efficiency and event response time over the non-divisible architectures found in most PLA and sequencer types.

A normal output pin is low asserted. The output gate performs an OR function over the flip-flop outputs of the state macrocells. The OR function includes only the outputs which are programmably connected to the OR line in the output array. When none of the connected state macrocell flip-flops are in the true or set condition, the output is high. If any connected macrocell flip-flop is asserted (or true) then the OR gate function is true and the output pin is low.

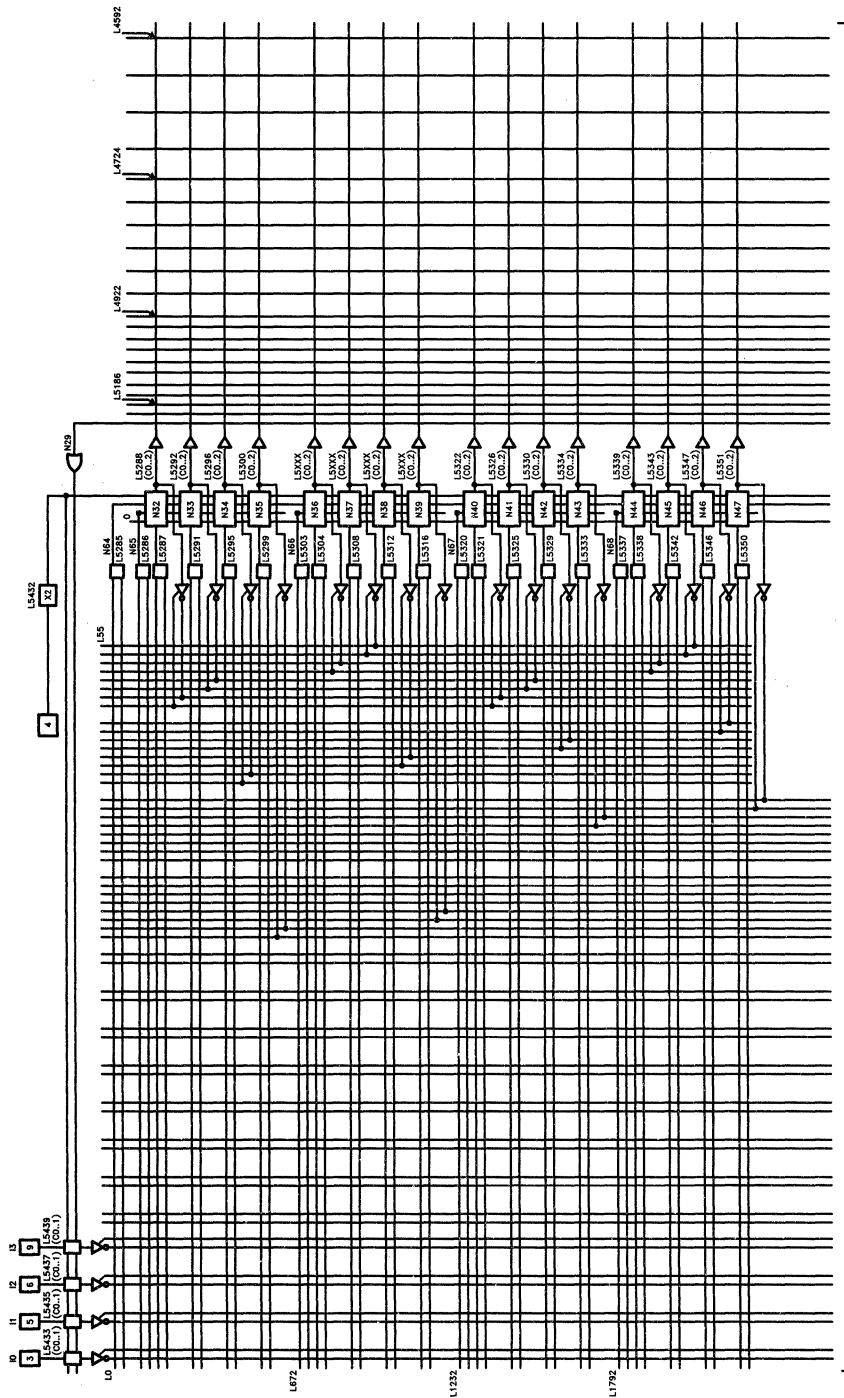
Forcing a false condition is easily accomplished by not connecting any state macrocells to the OR line. To force a true condition, line 33 (labelled V<sub>CC</sub>) is included in the output array. Any OR line connected to line 33 will be permanently true which will cause a normal output to be low.

The bidirectional outputs are I/O pins which may be used as either inputs or outputs. Under state machine control, these pins may be tristated and used as inputs or outputs depending on how the OE term is programmed.

Each bidirectional output has an OE or output enable control and an associated input path to the first array. The OE control is an OR term from the output array which enables the output when the OR function is true. Thus, an OE which has its OR term connected to line 33 will turn the output on permanently.

The Mealy outputs are designed to implement the fastest possible path between an input to the device and an output. Functions are available which combine the OR term and an input signal. These functions, XOR, AND, and OR, with true or negated assertion levels, are useful for data strobes and semaphore operations where signalling occurs depending on the state, but independent of a signal transition.

The AND and OR functions can be used to gate data strobe signals by the state. The XOR function can be used to implement 2 cycle signalling, which is used in self-timed systems to minimize signalling delays. If these functions are not needed, then the Mealy outputs can be configured as normal outputs.



0165-10

To Lower Half

Figure 8a. CY7C361 Block Diagram (Upper Half)

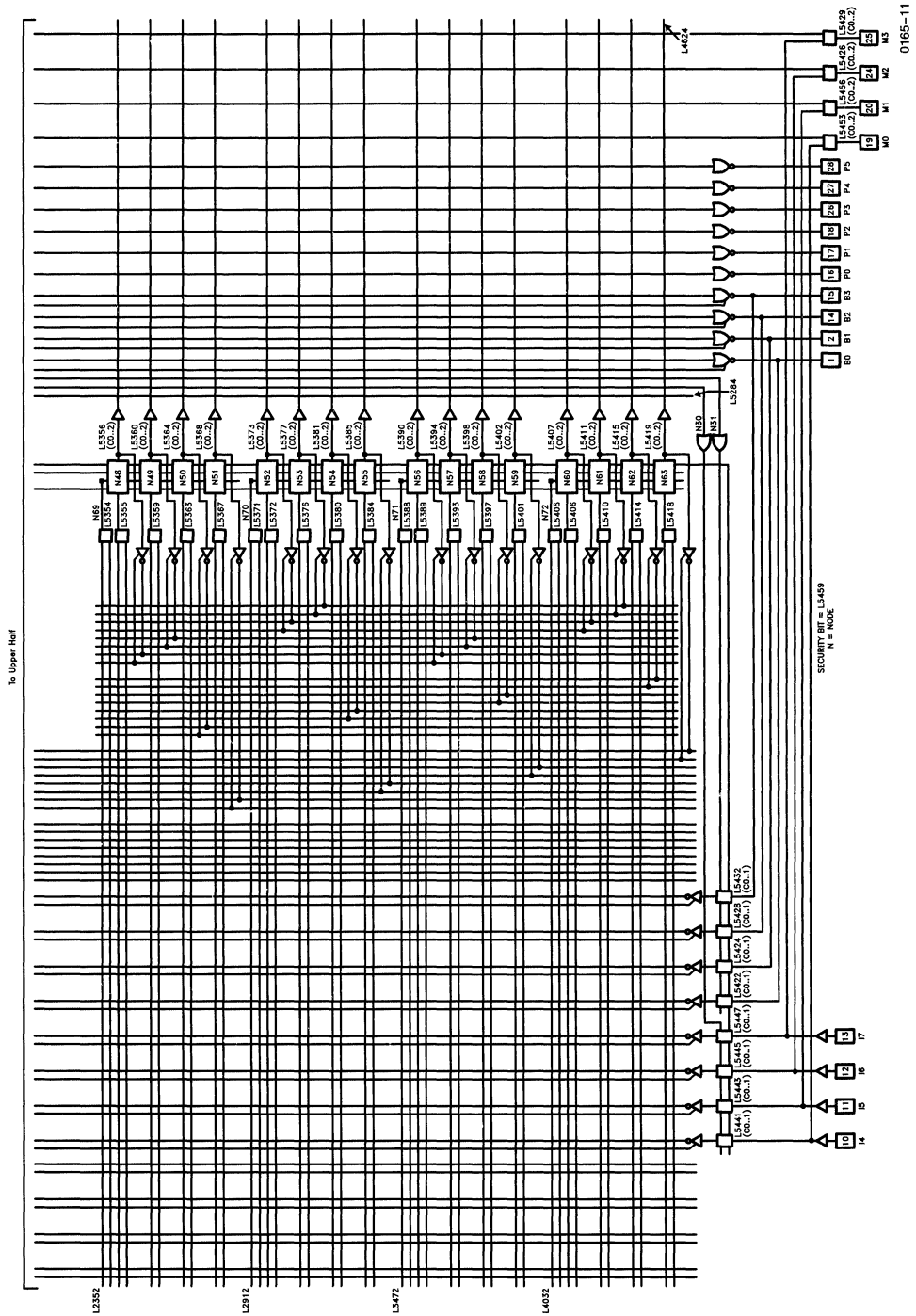


Figure 8b. CY7C361 Block Diagram (Lower Half)

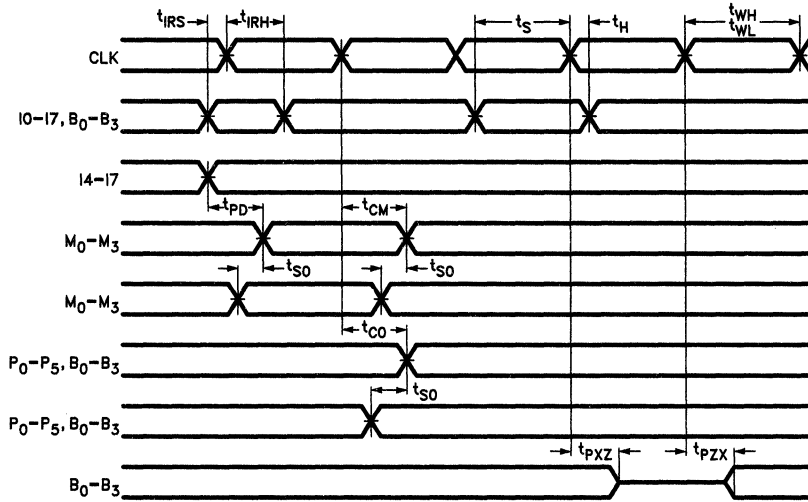
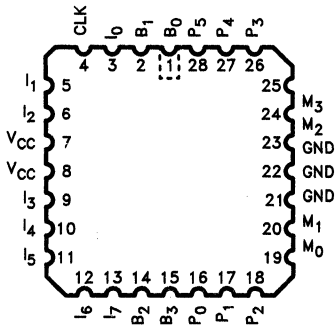


Figure 9. AC Timing Waveforms

0165-12

### Pin Configuration



0165-2

## Introduction

PLDs or Programmable Logic Devices provide an attractive alternative to logic implemented with discrete devices. Because the primary requirements for this logic has been to provide high performance and increased functional density, in the past all programmable logic functions have been implemented in a bipolar technology. Bipolar technology uses a fuse for the programming mechanism. The fuses are intact when the product is delivered to the user, and may be programmed once, then read and used indefinitely. The fuses are literally blown using a high current supplied by a programming system. Programming or blowing a fuse is a one time event, once blown the fuse is forever open. A fuse therefore may not be tested to see that it will blow or program properly before it is delivered to the user. This difficulty in testing fuses for programming results in less than 100% programming yield in the field, and this fallout falls into three categories.

A certain percentage of the product simply fails to program. These devices are easily identified, and may be returned for replacement. A small percentage of the product will program and verify correctly, but fail to function properly as a logic element. This can happen because, without programming each location, the connection between the programmed cell and the logic it is to control cannot be verified. Some programmers can test for this condition through the use of a set of test vectors for each unique code or part. Additional material will be lost, however, even if a structured set of test vectors is used due to the device functioning too slow. This failure is much more subtle and can only be found by 100% AC testing of the programmed device, or worse yet by troubleshooting an assembled board or system.

Cypress PLDs use an EPROM programming mechanism. This technology has been available since the early 1970's, however, as with most MOS technologies, the emphasis has been on density, not performance. CMOS at Cypress is as fast as or faster than Bipolar and coupled with EPROM programming, offers a viable alternative to bipolar programmable logic from a performance point of view. In addition, CMOS EPROM technology offers other overwhelming advantages. EPROM cells are programmed by injecting charge on an electrically isolated gate which causes the transistor to be permanently turned off. This mechanism may be reversed by irradiating the cell with ultraviolet light. This feature totally changes the testing philosophy and provides a new feature for the user. All programmable cells may now be tested by the manufacturer prior to delivery to the customer. This provides an easy methodology to certify programming, functionality, and performance. With built in test arrays, functionality and performance may be tested even if the device is packaged in a non-windowed package. Devices packaged in a windowed package may be programmed and erased indefinitely providing the designer a tool for the development of his logic without throwing away devices that are programmed incorrectly as the design proceeds.

## Programmable Technology

### EPROM Process Technology

EPROM technology employs a floating or isolated gate between the normal control gate and the source/drain region of a transistor. This gate may be charged with electrons during the programming operation and when charged with electrons, the transistor is permanently turned off. When uncharged (the transistor is unprogrammed) the device may be turned on and off normally with the control gate. The state of the floating gate, charged or uncharged, is permanent because the gate is isolated in an extremely pure oxide. The charge may be removed if the device is irradiated with ultraviolet energy in the form of light. This ultraviolet light allows the electrons on the gate to recombine and discharge the gate. This process is repeatable and therefore can be used during the processing of the device, repeatedly if necessary, to assure programming function and performance.

### Two Transistor Cells

In order to provide an EPROM cell that is as fast as the fuse technology employed in bipolar processes, Cypress uses a two transistor EPROM cell. One transistor is optimized for reliable programming, and one transistor is optimized for high speed. The floating gates are connected such that charge injected on the floating gate of the programming transistor is conducted to the read transistor biasing it off.

### Programming Algorithm

#### Byte Addressing and Programming

All Cypress Programmable Logic Devices are addressed and programmed on BYTE or EXTENDED BYTE basis where an EXTENDED BYTE is a field that is as wide as the output path of the device. Each device or family of devices has a unique address map which is available in the product data sheet. Each BYTE or EXTENDED BYTE is written into the addressed location from the pins that serve as the output pins in normal operation. To program a cell, a "1" or HIGH is placed on the input pin and a "0" or LOW is placed on pins corresponding to cells that are not to be programmed. Data is also read from these pins in parallel for verification after programming. A "1" or HIGH during program verify operation indicates an unprogrammed cell, while a "0" or LOW indicates that the cell accessed has been programmed.

#### Blank Check

Before programming all Programmable Logic Devices may be checked in a conventional manner to determine that they have not been previously programmed. This is accomplished in a program verify mode of operation by reading the contents of the array. During this operation, a "1" or HIGH output indicates that the addressed cell is unprogrammed, while a "0" or LOW indicates a programmed cell.





# PLD Programming Information (Continued)

## Programming The Data Array

Programming is accomplished by applying a supervoltage to one pin of the device causing it to enter the programming mode of operation. This also provides the programming voltage for the cells to be programmed. In this mode of operation, the address lines of the device are used to address each location to be programmed, and the data is presented on the pins normally used for reading the contents of the device. Each device has a READ/WRITE pin in the programming mode. This signal causes a write operation when switched to a supervoltage, and a read operation when switched to a logic "0" or LOW. In the logic HIGH state "1" the device is in a program inhibit condition and the output pins are in a high impedance state. During a WRITE operation, the data on the output pins is written into the addressed array location. In a READ operation the contents of the addressed location are present on the output pins and may be verified. Programming therefore is accomplished by placing data on the output pins, and writing it into the addressed location. Verification of data is accomplished by examining the information on the output pins during a READ operation.

The timing for actual programming is supplied in the unique programming specification for each device.

## Phantom Operating Modes

All Cypress Programmable Logic Devices contain a PHANTOM ARRAY for the purposes of post assembly testing. This array is accessed, programmed and operated in a special PHANTOM mode of operation. In this mode, the normal array is disconnected from control of the logic, and in its place the PHANTOM ARRAY is connected. In normal operation the PHANTOM ARRAY is disconnected and control is only via the normal array. This special feature allows every device to be tested for both functionality and performance after packaging and, if desired, by the user before programming and use. The PHANTOM modes are entered through the use of supervoltages and are unique for each device or family of devices. See specific data sheets for details.

## Special Features

Cypress Programmable Logic devices, depending on the device, have several special features. For example the security mechanism defeats the verify operation and therefore secures the contents of the device against unauthorized tampering or access. In advanced devices such as the PAL C 22V10, PLD C 20G10, and the CY7C330 the MACROCELLs are programmable through the use of the architecture bits. This allows the user to more effectively tailor the device architecture to his unique system requirements. These features are also programmed through the use of EPROM cells. Specific programming is detailed in the device data sheet.

## Programming Support

Programming support for Cypress CMOS Programmable Logic Devices is available from a number of programmer manufacturers, some of which are listed as follows. The hardware module version number listed is the earliest version qualified by Cypress. Any subsequent version is also qualified unless otherwise specifically noted.

Data I/O Corporation  
10525 Willows Rd. N.E.  
P.O. Box 97046  
Redmond, WA  
98073-9746  
(206) 881-6444

| Data I/O 29B<br>LOGICPAK V04 |                           |                              | Adapters:            |                         |
|------------------------------|---------------------------|------------------------------|----------------------|-------------------------|
| Cypress<br>Part Number       | Generic<br>Part<br>Number | Family<br>Code and<br>Pinout | PT                   | Generic                 |
|                              |                           |                              | 303A-009<br>Revision | 303A-011A/B<br>Revision |
| PALC16R8                     | 16R8 [1]                  | 28 24                        | V03                  | V01                     |
| PALC16R6                     | 16R6 [1]                  | 28 24                        | V03                  | V01                     |
| PALC16R4                     | 16R4 [1]                  | 28 24                        | V03                  | V01                     |
| PALC16L8                     | 16L8 [1]                  | 28 17                        | V03                  | V01                     |
| PALC22V10                    | 22V10                     | 28 28                        | V04                  | V01                     |
| PLDC20G10                    | 20G10                     | 28 56                        | V04                  | V01                     |
| PLDC20G10                    | 20R4                      | 28 65                        | V04                  | V02                     |
| PLDC20G10                    | 20R6                      | 28 66                        | V04                  | V02                     |
| PLDC20G10                    | 20R8                      | 28 27                        | V04                  | V02                     |
| PLDC20G10                    | 20L8                      | 28 26                        | V04                  | V01                     |
| PLDC20G10                    | 20L10                     | 28 6                         | V04                  | V01                     |
| PLDC20G10                    | 20L2                      | 28 5                         | V04                  | V02                     |
| PLDC20G10                    | 18L4                      | 28 4                         | V04                  | V01                     |
| PLDC20G10                    | 16L6                      | 28 3                         | V04                  | V01                     |
| PLDC20G10                    | 14L8                      | 28 2                         | V04                  | V01                     |
| PLDC20G10                    | 12L10                     | 28 1                         | V04                  | V01                     |
| CY7C330                      | 7C330                     | 28 1A                        | V06                  | V01                     |

Note:

1. Requires Design Adapter 100.

| Data I/O Model 60A, 60H |                        |                           |          |
|-------------------------|------------------------|---------------------------|----------|
| Cypress<br>Part Number  | Generic<br>Part Number | Family Code<br>and Pinout | Revision |
| PALC16R8                | 16R8                   | 28 24                     | V05      |
| PALC16R6                | 16R6                   | 28 24                     | V05      |
| PALC16R4                | 16R4                   | 28 24                     | V05      |
| PALC16L8                | 16L8                   | 28 17                     | V05      |
| PALC22V10               | 22V10                  | 28 28                     | V08      |
| PLDC20G10               | 20G10                  | 28 56                     | V08      |

| Data I/O Unisite       |                        |                           |          |
|------------------------|------------------------|---------------------------|----------|
| Cypress<br>Part Number | Generic<br>Part Number | Family Code<br>and Pinout | Revision |
| PALC16R8               | 16R8                   |                           | 2.0      |
| PALC16R6               | 16R6                   |                           | 2.0      |
| PALC16R4               | 16R4                   | Menu<br>Driven            | 2.0      |
| PALC16L8               | 16L8                   |                           | 2.0      |
| PALC22V10              | 22V10                  |                           | 2.0      |
| PLDC20G10              | 20G10                  |                           | 2.0      |



# PLD Programming Information (Continued)

Stag Microsystems  
1600 Wyatt Dr.  
Santa Clara, CA 95054  
(408) 988-1118  
STAG ZL32 Rev. 30A03

| STAG PPZ Zm2200 Rev. 18<br>ZL32 Rev. 30A03 |                     |                        |
|--|---------------------|------------------------|
| Cypress Part Number                        | Generic Part Number | Family Code and Pinout |
| PALC16R8                                   | 16R8                | Menu Driven            |
| PALC16R6                                   | 16R6                |                        |
| PALC16R4                                   | 16R4                |                        |
| PALC16L8                                   | 16L8                |                        |
| PALC22V10                                  | 22V10               |                        |

Cypress Semiconductor Inc.  
3901 North First Street  
San Jose, CA 95134  
(408) 943-2600

| Cypress CY3000 QuickPro Rev. PLD 2.0 |                     |                        |
|--------------------------------------|---------------------|------------------------|
| Cypress Part Number                  | Generic Part Number | Family Code and Pinout |
| PALC16R8                             | 16R8                | Menu Driven            |
| PALC16R6                             | 16R6                |                        |
| PALC16R4                             | 16R4                |                        |
| PALC16L8                             | 16L8                |                        |
| PALC22V10                            | 22V10               |                        |
| PLDC20G10                            | 20G10               |                        |
| PLDC20G10                            | 20R4                |                        |
| PLDC20G10                            | 20R6                |                        |
| PLDC20G10                            | 20R8                |                        |
| PLDC20G10                            | 20L8                |                        |
| PLDC20G10                            | 20L10               |                        |
| PLDC20G10                            | 20L2                |                        |
| PLDC20G10                            | 18L4                |                        |
| PLDC20G10                            | 16L6                |                        |
| PLDC20G10                            | 14L8                |                        |
| PLDC20G10                            | 12L10               |                        |
| PLD20RA10                            | 20RA10              |                        |
| CY7C330                              | 7C330               |                        |
| CY7C331                              | 7C331               |                        |
| CY7C332                              | 7C332               |                        |

Digelec Corporation  
1602 Lawrence Ave.  
Suite 113  
Ocean, NJ 07712  
(201) 493-2420

| DIGELEC 803 FAM-52 Rev. A-6.0 |                     |                        |                  |
|-------------------------------|---------------------|------------------------|------------------|
| Cypress Part Number           | Generic Part Number | Family Code and Pinout | Adapter Rev. A-3 |
| PALC16R8                      | 16R8                | Menu Driven            | DA-53            |
| PALC16R6                      | 16R6                |                        | DA-53            |
| PALC16R4                      | 16R4                |                        | DA-53            |
| PALC16L8                      | 16L8                |                        | DA-53            |
| PALC22V10                     | 22V10               |                        | DA-53            |

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ISDATA® is a registered trademark of ISDATA GmbH.  
LOG/iCT™ is a trademark of ISDATA GmbH.

Logical Devices Inc.  
1321 N.W. 65th Place  
Ft. Lauderdale, FL 33309  
(305) 974-0975

| Logical Devices ALLPRO Rev. V1.4 |                     |                        |
|----------------------------------|---------------------|------------------------|
| Cypress Part Number              | Generic Part Number | Family Code and Pinout |
| PALC16R8                         | 16R8                | Menu Driven            |
| PALC16R6                         | 16R6                |                        |
| PALC16R4                         | 16R4                |                        |
| PALC16L8                         | 16L8                |                        |
| PALC22V10                        | 22V10               |                        |

Kontron Electronics  
1230 Charleston Road  
Mountain View, CA  
94039-7230  
(415) 965-7020

| Kontron EPP 80 UPM-P |                     |                        |
|----------------------|---------------------|------------------------|
| Cypress Part Number  | Generic Part Number | Family Code and Pinout |
| PALC16R8             | 16R8                | Menu Driven            |
| PALC16R6             | 16R6                |                        |
| PALC16R4             | 16R4                |                        |
| PALC16L8             | 16L8                |                        |
| PALC22V10            | 22V10               |                        |

### Third Party Development Software

ABEL™  
Data I/O Corporation  
10525 Willows Rd. N.E.  
P.O. Box 97046  
Redmond, WA  
98073-9746  
(206) 881-6444

CUPL™  
Assisted Technology  
1290 Parkmoor Ave.  
San Jose, CA 95126  
(800) 523-5207  
(800) 628-8748 CA

LOG/iCT™  
ISDATA GmbH  
Haid-und-Neu-Strasse 7  
D-7500 Karlsruhe 1 West Germany  
(0721) 69 30 92

### Supported Devices:

PALC16R8  
PALC16R6  
PALC16R4  
PALC16L8  
PALC22V10  
PLDC20G10  
CY7C330  
  
PALC16R8  
PALC16R6  
PALC16R4  
PALC16L8  
PALC22V10  
CY7C330  
CY7C331



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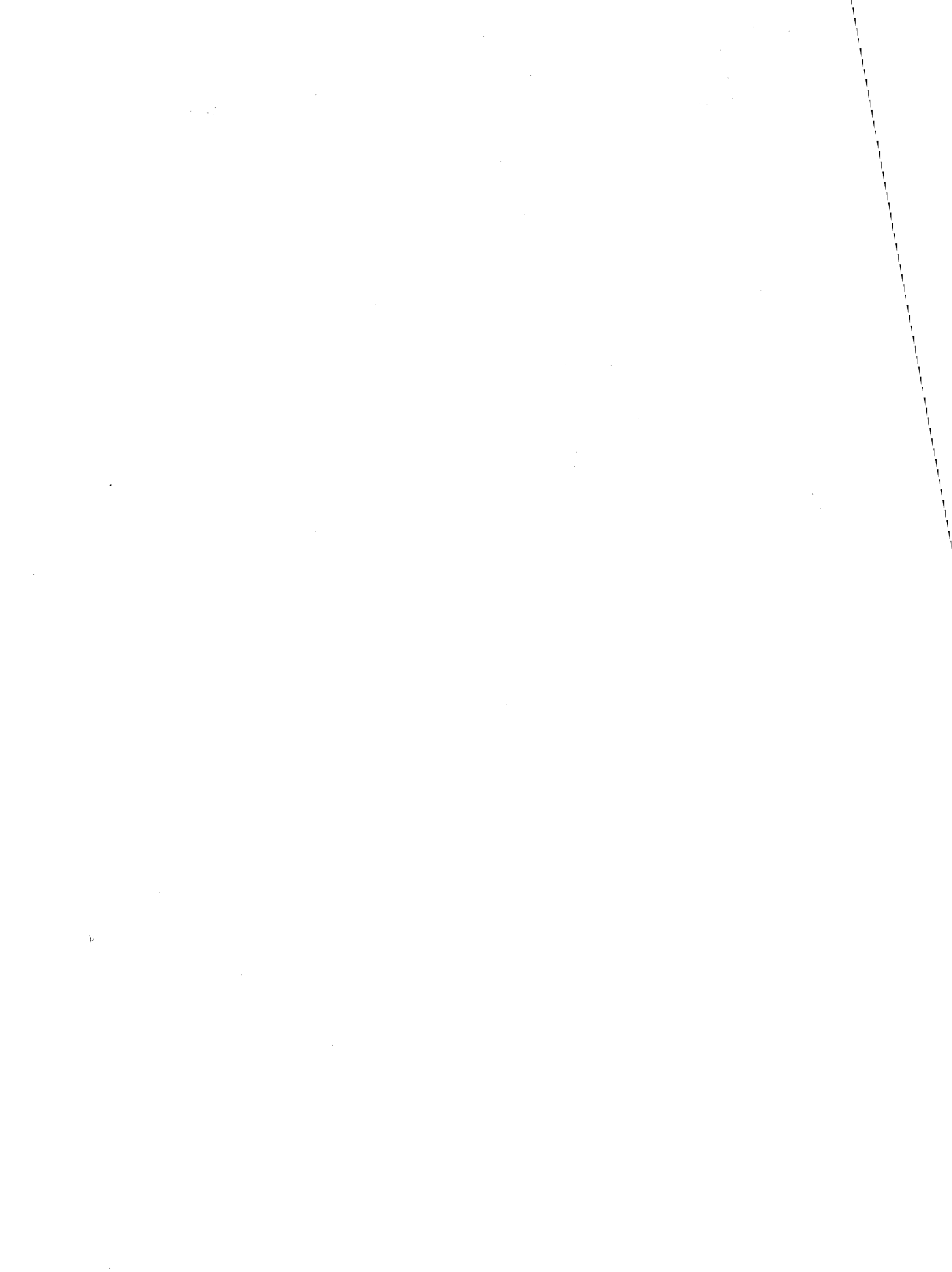
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## LOGIC

| Device Number | Description                                | Page Number |
|---------------|--|-------------|
| CY2901C       | CMOS 4-Bit Slice                           | 5-1         |
| CY2909A       | CMOS Microprogram Sequencer                | 5-9         |
| CY2911A       | CMOS Microprogram Sequencer                | 5-9         |
| CY2910A       | CMOS Microprogram Controller               | 5-14        |
| CY3341        | 64 x 4 FIFO Serial Memory                  | 5-19        |
| CY7C401       | Cascadeable 64 x 4 FIFO                    | 5-24        |
| CY7C402       | Cascadeable 64 x 5 FIFO                    | 5-24        |
| CY7C403       | Cascadeable 64 x 4 FIFO with Output Enable | 5-24        |
| CY7C404       | Cascadeable 64 x 5 FIFO with Output Enable | 5-24        |
| CY7C408A      | Cascadeable 64 x 8 FIFO with Output Enable | 5-34        |
| CY7C409A      | Cascadeable 64 x 9 FIFO                    | 5-34        |
| CY7C420       | Cascadeable 512 x 9 FIFO                   | 5-48        |
| CY7C421       | Cascadeable 512 x 9 FIFO                   | 5-48        |
| CY7C424       | Cascadeable 1024 x 9 FIFO                  | 5-48        |
| CY7C425       | Cascadeable 1024 x 9 FIFO                  | 5-48        |
| CY7C428       | Cascadeable 2048 x 9 FIFO                  | 5-48        |
| CY7C429       | Cascadeable 2048 x 9 FIFO                  | 5-48        |
| CY7C510       | 16 x 16 Multiplier Accumulator             | 5-60        |
| CY7C516       | 16 x 16 Multiplier                         | 5-72        |
| CY7C517       | 16 x 16 Multiplier                         | 5-72        |
| CY7C901       | CMOS 4-Bit Slice                           | 5-84        |
| CY7C909       | Microprogram Sequencer                     | 5-99        |
| CY7C911       | Microprogram Sequencer                     | 5-99        |
| CY7C910       | Microprogram Controller                    | 5-110       |
| CY7C9101      | CMOS 16-Bit Slice                          | 5-121       |
| CY7C9115      | CMOS 16-Bit Microprogrammed ALU            | 5-138       |
| CY7C9116      | CMOS 16-Bit Microprogrammed ALU            | 5-138       |
| CY7C9117      | CMOS 16-Bit Microprogrammed ALU            | 5-138       |





**Features**

- Pin compatible and functional equivalent to AMD AM2901C
- Low power
- $V_{CC}$  margin  
—  $5V \pm 10\%$   
— All parameters guaranteed over commercial and military operating temperature range
- Eight function ALU  
Performs eight operations on two 4-bit operands
- Expandable  
Infinitely expandable in 4-bit increments
- Four status flags  
Carry, overflow, negative, zero

- ESD protection  
Capable of withstanding greater than 2000V static discharge voltage

**Functional Description**

The CY2901 is a high-speed, expandable, 4-bit wide ALU that can be used to implement the arithmetic section of a CPU, peripheral controller, or programmable controller. The instruction set of the CY2901 is basic but yet so versatile that it can emulate the ALU of almost any digital computer.

The CY2901, as illustrated in the block diagram, consists of a 16-word by 4-bit dual-port RAM register file, a 4-bit ALU and the required data manipulation and control logic.

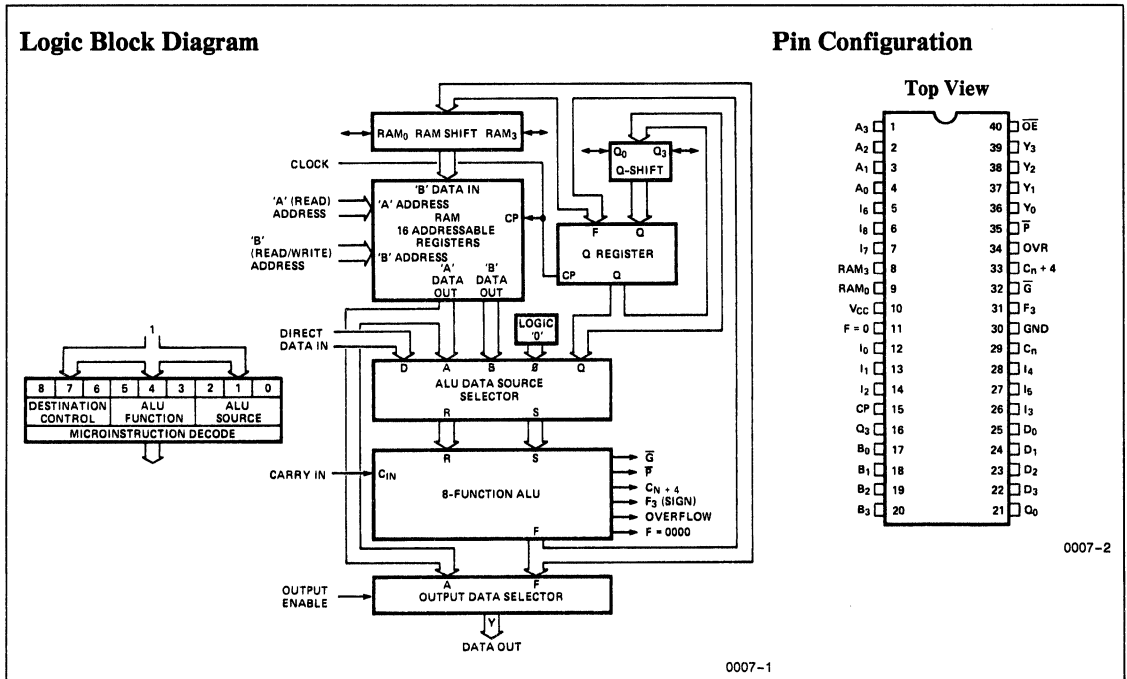
The operation performed is determined by nine input control lines ( $I_0$  to  $I_8$ ) that are usually inputs from an instruction register.

The CY2901 is expandable in 4-bit increments, has three-state data outputs as well as flag outputs, and can use either a full-look ahead carry or a ripple carry.

The CY2901 is a pin compatible, functional equivalent, improved performance replacement for the AM2901.

The CY2901 is fabricated using an advanced 1.2 micron CMOS process that eliminates latchup, results in ESD protection over 2000V and achieves superior performance at a low power dissipation.

5



**Selection Guide** See last page for ordering information.

| Read Modify-Write Cycle (Min.) in ns | Operating $I_{CC}$ (Max.) in mA | Operating Range | Part Number |
|--------------------------------------|---------------------------------|-----------------|-------------|
| 31                                   | 140                             | Commercial      | CY2901C     |
| 32                                   | 180                             | Military        | CY2901C     |



## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|  |                 |
|--|-----------------|
| Storage Temperature .....                                      | -65°C to +150°C |
| Ambient Temperature with<br>Power Applied .....                | -55°C to +125°C |
| Supply Voltage to Ground Potential<br>(Pin 10 to Pin 30) ..... | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs<br>in High Z State .....         | -0.5V to +7.0V  |
| DC Input Voltage .....   | -3.0V to +7.0V  |
| Output Current into Outputs (Low) .....                        | 30 mA           |

|                                 |   |
|---------------------------------|---|
| Static Discharge Voltage .....  | >2001V<br>(Per MIL-STD-883 Method 3015) |
| Latchup Current (Outputs) ..... | >200 mA                                 |

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[1]</sup> | -55°C to +125°C     | 5V ± 10%        |

Note:

1. T<sub>A</sub> is the "instant on" case temperature.

## Pin Definitions

| Signal Name                        | I/O | Description  |
|------------------------------------|-----|--|
| A <sub>0</sub> -A <sub>3</sub>     | I   | These 4 address lines select one of the registers in the stack and output its contents on the (internal) A port.   |
| B <sub>0</sub> -B <sub>3</sub>     | I   | These 4 address lines select one of the registers in the stack and output its contents on the (internal) B port. This can also be the destination address when data is written back into the register file.  |
| I <sub>0</sub> -I <sub>8</sub>     | I   | These 9 instruction lines select the ALU data sources (I <sub>0</sub> , 1, 2), the operation to be performed (I <sub>3</sub> , 4, 5) and what data is to be written into either the Q register or the register file (I <sub>6</sub> , 7, 8).   |
| D <sub>0</sub> -D <sub>3</sub>     | I   | These are 4 data input lines that may be selected by the I <sub>0</sub> , 1, 2 lines as inputs to the ALU.   |
| Y <sub>0</sub> -Y <sub>3</sub>     | O   | These are three-state data output lines that, when enabled, output either the output of the ALU or the data in the A latches, as determined by the code on the I <sub>6</sub> , 7, 8 lines.  |
| $\overline{OE}$                    | I   | Output Enable. This is an active LOW input that controls the Y <sub>0</sub> -Y <sub>3</sub> outputs. When this signal is LOW the Y outputs are enabled and when it is HIGH they are in the high impedance state.   |
| CP                                 | I   | Clock Input. The LOW level of the clock writes data to the 16 x 4 RAM. The HIGH level of the clock writes data from the RAM to the A-port and B-port latches. The operation of the Q register is similar. Data is entered into the master latch on the LOW level of the clock and transferred from master to slave when the clock is HIGH. |
| Q <sub>3</sub><br>RAM <sub>3</sub> | I/O | These two lines are bidirectional and are controlled by the I <sub>6</sub> , 7, 8 inputs. Electrically they are three-state output drivers connected to the TTL compatible CMOS inputs.  |

| Signal Name                                   | I/O | Description   |
|---|-----|---|
| Q <sub>3</sub><br>RAM <sub>3</sub><br>(Cont.) | I/O | <b>Outputs:</b> When the destination code on lines I <sub>6</sub> , 7, 8 indicates a shift left (UP) operation the three-state outputs are enabled and the MSB of the Q register is output on the Q <sub>3</sub> pin and the MSB of the ALU output (F <sub>3</sub> ) is output on the RAM 3 pin.<br><b>Inputs:</b> When the destination code indicates a shift right (DOWN) the pins are the data inputs to the MSB of the Q register and the MSB of the RAM. |
| Q <sub>0</sub><br>RAM <sub>0</sub>            | I/O | These two lines are bidirectional and function in a manner similar to the Q <sub>3</sub> and RAM <sub>3</sub> lines, except that they are the LSB of the Q register and RAM.  |
| C <sub>n</sub>                                | I   | The carry-in to the internal ALU.   |
| C <sub>n</sub> + 4                            | O   | The carry-out from the internal ALU.  |
| $\overline{G}$ , $\overline{P}$               | O   | The carry generate and the carry propagate outputs of the ALU, which may be used to perform a carry look-ahead operation over the 4 bits of the ALU.  |
| OVR   | O   | Overflow. This signal is logically the exclusive-OR of the carry-in and the carry-out of the MSB of the ALU. This pin indicates that the result of the ALU operation has exceeded the capacity of the machine. It is valid only for the sign bit and assumes two's complement coding for negative numbers.  |
| F = 0   | O   | Open collector output that goes HIGH if the data on the ALU outputs (F <sub>0</sub> , 1, 2, 3) are all LOW. It indicates that the result of an ALU operation is zero (positive logic).  |
| F <sub>3</sub>                                | O   | The most significant bit of the ALU output.   |

**Electrical Characteristics** Over Commercial and Military Operating Range<sup>[3]</sup>  
 $V_{CC}$  Min. = 4.5V,  $V_{CC}$  Max. = 5.5V

| Parameters | Description                                 | Test Conditions  | Min.       | Max.     | Units                          |
|------------|---|--|------------|----------|--------------------------------|
| $V_{OH}$   | Output HIGH Voltage                         | $V_{CC} = \text{Min.}$<br>$I_{OH} = -3.4 \text{ mA}$   | 2.4        |          | V                              |
| $V_{OL}$   | Output LOW Voltage                          | $V_{CC} = \text{Min.}$<br>$I_{OL} = 20 \text{ mA Commercial}$<br>$I_{OL} = 16 \text{ mA Military}$ |            | 0.4      | V                              |
| $V_{IH}$   | Input HIGH Voltage                          |  | 2.0        | $V_{CC}$ | V                              |
| $V_{IL}$   | Input LOW Voltage                           |  | -3.0       | 0.8      | V                              |
| $I_{IH}$   | Input HIGH Current                          | $V_{CC} = \text{Max.}$<br>$V_{IN} = V_{CC}$  |            | 10       | $\mu\text{A}$                  |
| $I_{IL}$   | Input LOW Current                           | $V_{CC} = \text{Max.}$<br>$V_{IN} = \text{GND}$  |            | -10      | $\mu\text{A}$                  |
| $I_{OH}$   | Output HIGH Current                         | $V_{CC} = \text{Min.}$<br>$V_{OH} = 2.4\text{V}$   | -3.4       |          | mA                             |
| $I_{OL}$   | Output LOW Current                          | $V_{CC} = \text{Min.}$<br>$V_{OL} = 0.4\text{V}$   | Commercial | 20       | mA                             |
|            |   |  | Military   | 16       | mA                             |
| $I_{OZ}$   | Output Leakage Current                      | $V_{CC} = \text{Max.}$<br>$V_{OUT} = \text{GND to } V_{CC}$  | -40        | +40      | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{SC}$   | Output Short Circuit Current <sup>[1]</sup> | $V_{CC} = \text{Max.}$<br>$V_{OUT} = 0\text{V}$  | -30        | -85      | mA                             |
| $I_{CC}$   | Supply Current                              | $V_{CC} = \text{Max.}$   | Commercial | 140      | mA                             |
|            |   |  | Military   | 180      | mA                             |

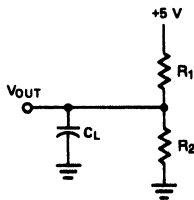
5

**Capacitance<sup>[2]</sup>**

| Parameters | Description        | Test Conditions  | Max. | Units |
|------------|--------------------|--|------|-------|
| $C_{IN}$   | Input Capacitance  | $T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$<br>$V_{CC} = 5.0\text{V}$ | 5    | pF    |
| $C_{OUT}$  | Output Capacitance |  | 7    |       |

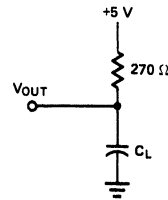
- Notes:
- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
  - Tested initially and after any design or process changes that may affect these parameters.
  - See the last page of this specification for Group A subgroup testing information.

**Output Loads used for AC Performance Characteristics**



0007-3

All outputs except open drain



0007-4

Open drain (F = 0)

- Notes:
- $C_L = 50 \text{ pF}$  includes scope probe, wiring and stray capacitance.
  - $C_L = 5 \text{ pF}$  for output disable tests.
  - Loads shown above are for commercial (20 mA)  $I_{OL}$  specifications only.

|       | Commercial   | Military     |
|-------|--------------|--------------|
| $R_1$ | 203 $\Omega$ | 252 $\Omega$ |
| $R_2$ | 148 $\Omega$ | 174 $\Omega$ |

## CY2901C Guaranteed Commercial Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Commercial (0°C to 70°C) operating temperature range with  $V_{CC}$  varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See previous page for loading circuit information.

This data applies to parts with the following numbers:  
 CY2901CPC CY2901CDC CY2901CLC

## Cycle Time and Clock Characteristics

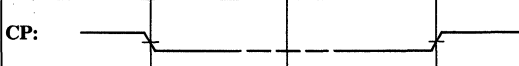
| CY2901-   | C      |
|---|--------|
| Read-Modify-Write Cycle (from selection of A, B registers to end of cycle). | 31 ns  |
| Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)         | 32 MHz |
| Minimum Clock LOW Time  | 15 ns  |
| Minimum Clock HIGH Time   | 15 ns  |
| Minimum Clock Period  | 31 ns  |

For faster performance see CY7C901-23 specification.

## Combinational Propagation Delays. $C_L = 50$ pF

| To Output<br>From Input   | Y  | F <sub>3</sub> | C <sub>n</sub> + 4 | $\bar{G}, \bar{P}$ | F = 0 | OVR | RAM <sub>0</sub><br>RAM <sub>3</sub> | Q <sub>0</sub><br>Q <sub>3</sub> |
|---------------------------|----|----------------|--------------------|--------------------|-------|-----|--------------------------------------|----------------------------------|
| A, B Address              | 40 | 40             | 40                 | 37                 | 40    | 40  | 40                                   | —                                |
| D                         | 30 | 30             | 30                 | 30                 | 38    | 30  | 30                                   | —                                |
| C <sub>n</sub>            | 22 | 22             | 20                 | —                  | 25    | 22  | 25                                   | —                                |
| I <sub>012</sub>          | 35 | 35             | 35                 | 37                 | 37    | 35  | 35                                   | —                                |
| I <sub>345</sub>          | 35 | 35             | 35                 | 35                 | 38    | 35  | 35                                   | —                                |
| I <sub>678</sub>          | 25 | —              | —                  | —                  | —     | —   | 26                                   | 26                               |
| A Bypass ALU<br>(I = 2XX) | 35 | —              | —                  | —                  | —     | —   | —                                    | —                                |
| Clock                     | 35 | 35             | 35                 | 35                 | 35    | 35  | 35                                   | 28                               |

## Set-up and Hold Times Relative to Clock (CP) Input

| Input                                   | CP:  |                          |                             |                          |
|---|---|--------------------------|-----------------------------|--------------------------|
|   | Set-up Time<br>Before H → L   | Hold Time<br>After H → L | Set-up Time<br>Before L → H | Hold Time<br>After L → H |
| A, B Source Address                     | 15  | 1<br>(Note 3)            | 30, 15 + tpWL<br>(Note 4)   | 1                        |
| B Destination Address                   | 15  | ← Do Not Change →        |                             | 1                        |
| D                                       | —   | —                        | 25                          | 0                        |
| C <sub>n</sub>                          | —   | —                        | 20                          | 0                        |
| I <sub>012</sub>                        | —   | —                        | 30                          | 0                        |
| I <sub>345</sub>                        | —   | —                        | 30                          | 0                        |
| I <sub>678</sub>                        | 10  | ← Do Not Change →        |                             | 0                        |
| RAM <sub>0, 3</sub> , Q <sub>0, 3</sub> | —   | —                        | 12                          | 0                        |

## Output Enable/Disable Times

Output disable tests performed with  $C_L = 5$  pF and measured to 0.5V change of output voltage level.

| Device  | Input      | Output | Enable | Disable |
|---------|------------|--------|--------|---------|
| CY2901C | $\bar{OE}$ | Y      | 23     | 23      |

### Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".


3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

## CY2901C Guaranteed Military Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Military ( $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ) operating temperature range with  $V_{CC}$  varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See "Electrical Characteristics" of this data sheet for loading circuit information.

This data applies to parts with the following numbers:  
CY2901CDBM

### Combinational Propagation Delays $C_L = 50 \text{ pF}$ [5]

| To Output   | Y  | F <sub>3</sub> | C <sub>n</sub> + 4 | $\bar{G}, \bar{P}$ | F = 0 | OVR | RAM <sub>0</sub><br>RAM <sub>3</sub> | Q <sub>0</sub><br>Q <sub>3</sub> |
|---|----|----------------|--------------------|--------------------|-------|-----|--------------------------------------|----------------------------------|
| From Input  |    |                |                    |                    |       |     |                                      |                                  |
| A, B Address  | 48 | 48             | 48                 | 44                 | 48    | 48  | 48                                   | —                                |
| D   | 37 | 37             | 37                 | 34                 | 40    | 37  | 37                                   | —                                |
| C <sub>n</sub>  | 25 | 25             | 21                 | —                  | 28    | 25  | 28                                   | —                                |
| I <sub>012</sub>  | 40 | 40             | 40                 | 44                 | 44    | 40  | 40                                   | —                                |
| I <sub>345</sub>  | 40 | 40             | 40                 | 40                 | 40    | 40  | 40                                   | —                                |
| I <sub>678</sub>  | 29 | —              | —                  | —                  | —     | —   | 29                                   | 29                               |
| A Bypass ALU<br>(I = 2XX)   | 40 | —              | —                  | —                  | —     | —   | —                                    | —                                |
| Clock  | 40 | 40             | 40                 | 40                 | 40    | 40  | 40                                   | 33                               |

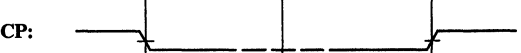
## Cycle Time and Clock Characteristics[5]

| CY2901-   | C      |
|---|--------|
| Read-Modify-Write Cycle (from selection of A, B registers to end of cycle). | 32 ns  |
| Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)         | 31 MHz |
| Minimum Clock LOW Time  | 15 ns  |
| Minimum Clock HIGH Time   | 15 ns  |
| Minimum Clock Period  | 32 ns  |

For faster performance see CY7C901-27 specification.

5

### Set-up and Hold Times Relative to Clock (CP) Input[5]

| Input                                 | CP:  |                          |                             |                          |
|---------------------------------------|---|--------------------------|-----------------------------|--------------------------|
|                                       | Set-up Time<br>Before H → L   | Hold Time<br>After H → L | Set-up Time<br>Before L → H | Hold Time<br>After L → H |
| A, B Source Address                   | 15  | 2<br>(Note 3)            | 30, 15 + tpWL<br>(Note 4)   | 2                        |
| B Destination Address                 | 15  | ← Do Not Change →        | →                           | 2                        |
| D                                     | —   | —                        | 25                          | 0                        |
| C <sub>n</sub>                        | —   | —                        | 20                          | 0                        |
| I <sub>012</sub>                      | —   | —                        | 30                          | 0                        |
| I <sub>345</sub>                      | —   | —                        | 30                          | 0                        |
| I <sub>678</sub>                      | 10  | ← Do Not Change →        | →                           | 0                        |
| RAM <sub>0, 3, Q<sub>0, 3</sub></sub> | —   | —                        | 12                          | 0                        |

### Output Enable/Disable Times[5]

Output disable tests performed with  $C_L = 5 \text{ pF}$  and measured to 0.5V change of output voltage level.

| Device  | Input | Output | Enable | Disable |
|---------|-------|--------|--------|---------|
| CY2901C | OE    | Y      | 25     | 25      |

#### Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".

3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.
5. See the last page of this specification for Group A subgroup testing information.

**Ordering Information**

| <b>Read<br/>Modify-<br/>Write<br/>Cycle (ns)</b> | <b>Ordering Code</b> | <b>Package<br/>Type</b> | <b>Operating<br/>Range</b> |
|--|----------------------|-------------------------|----------------------------|
| 31   | CY2901CPC            | P17                     | Commercial                 |
| 31   | CY2901CDC            | D18                     | Commercial                 |
| 32   | CY2901CDMB           | D18                     | Military                   |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IH</sub>      | 1,2,3     |
| I <sub>IL</sub>      | 1,2,3     |
| I <sub>OH</sub>      | 1,2,3     |
| I <sub>OL</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>SC</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |

#### Cycle Time and Clock Characteristics

| Parameters              | Subgroups   |
|-------------------------|-------------|
| Minimum Clock LOW Time  | 7,8,9,10,11 |
| Minimum Clock HIGH Time | 7,8,9,10,11 |

#### Combinational Propagation Delays

| Parameters   | Subgroups   |
|--|-------------|
| From A, B Address to Y                               | 7,8,9,10,11 |
| From A, B Address to F <sub>3</sub>                  | 7,8,9,10,11 |
| From A, B Address to C <sub>n</sub> + 4              | 7,8,9,10,11 |
| From A, B Address to $\overline{G}$ , $\overline{P}$ | 7,8,9,10,11 |
| From A, B Address to F = 0                           | 7,8,9,10,11 |
| From A, B Address to OVR                             | 7,8,9,10,11 |
| From A, B Address to RAM <sub>0,3</sub>              | 7,8,9,10,11 |
| From D to Y  | 7,8,9,10,11 |
| From D to F <sub>3</sub>                             | 7,8,9,10,11 |
| From D to C <sub>n</sub> + 4                         | 7,8,9,10,11 |
| From D to $\overline{G}$ , $\overline{P}$            | 7,8,9,10,11 |
| From D to F = 0                                      | 7,8,9,10,11 |
| From D to OVR  | 7,8,9,10,11 |
| From D to RAM <sub>0,3</sub>                         | 7,8,9,10,11 |

#### Combinational Propagation Delays (Continued)

| Parameters   | Subgroups   |
|--|-------------|
| From C <sub>n</sub> to Y   | 7,8,9,10,11 |
| From C <sub>n</sub> to F <sub>3</sub>                            | 7,8,9,10,11 |
| From C <sub>n</sub> to C <sub>n</sub> + 4                        | 7,8,9,10,11 |
| From C <sub>n</sub> to F = 0                                     | 7,8,9,10,11 |
| From C <sub>n</sub> to OVR                                       | 7,8,9,10,11 |
| From C <sub>n</sub> to RAM <sub>0,3</sub>                        | 7,8,9,10,11 |
| From I <sub>012</sub> to Y                                       | 7,8,9,10,11 |
| From I <sub>012</sub> to F <sub>3</sub>                          | 7,8,9,10,11 |
| From I <sub>012</sub> to C <sub>n</sub> + 4                      | 7,8,9,10,11 |
| From I <sub>012</sub> to $\overline{G}$ , $\overline{P}$         | 7,8,9,10,11 |
| From I <sub>012</sub> to F = 0                                   | 7,8,9,10,11 |
| From I <sub>012</sub> to OVR                                     | 7,8,9,10,11 |
| From I <sub>012</sub> to RAM <sub>0,3</sub>                      | 7,8,9,10,11 |
| From I <sub>345</sub> to Y                                       | 7,8,9,10,11 |
| From I <sub>345</sub> to F <sub>3</sub>                          | 7,8,9,10,11 |
| From I <sub>345</sub> to C <sub>n</sub> + 4                      | 7,8,9,10,11 |
| From I <sub>345</sub> to $\overline{G}$ , $\overline{P}$         | 7,8,9,10,11 |
| From I <sub>345</sub> to F = 0                                   | 7,8,9,10,11 |
| From I <sub>345</sub> to OVR                                     | 7,8,9,10,11 |
| From I <sub>345</sub> to RAM <sub>0,3</sub>                      | 7,8,9,10,11 |
| From I <sub>678</sub> to Y                                       | 7,8,9,10,11 |
| From I <sub>678</sub> to RAM <sub>0,3</sub>                      | 7,8,9,10,11 |
| From I <sub>678</sub> to Q <sub>0,3</sub>                        | 7,8,9,10,11 |
| From A Bypass ALU to Y<br>(I = 2XX)                              | 7,8,9,10,11 |
| From Clock $\curvearrowright$ to Y                               | 7,8,9,10,11 |
| From Clock $\curvearrowright$ to F <sub>3</sub>                  | 7,8,9,10,11 |
| From Clock $\curvearrowright$ to C <sub>n</sub> + 4              | 7,8,9,10,11 |
| From Clock $\curvearrowright$ to $\overline{G}$ , $\overline{P}$ | 7,8,9,10,11 |
| From Clock $\curvearrowright$ to F = 0                           | 7,8,9,10,11 |
| From Clock $\curvearrowright$ to OVR                             | 7,8,9,10,11 |
| From Clock $\curvearrowright$ to RAM <sub>0,3</sub>              | 7,8,9,10,11 |
| From Clock $\curvearrowright$ to Q <sub>0,3</sub>                | 7,8,9,10,11 |

**Set-up and Hold Times Relative to Clock (CP) Input**

| Parameters  | Subgroups   |
|---|-------------|
| A, B Source Address<br>Set-up Time Before H → L   | 7,8,9,10,11 |
| A, B Source Address<br>Hold Time After H → L      | 7,8,9,10,11 |
| A, B Source Address<br>Set-up Time Before L → H   | 7,8,9,10,11 |
| A, B Source Address<br>Hold Time After L → H      | 7,8,9,10,11 |
| B Destination Address<br>Set-up Time Before H → L | 7,8,9,10,11 |
| B Destination Address<br>Hold Time After H → L    | 7,8,9,10,11 |
| B Destination Address<br>Set-up Time Before L → H | 7,8,9,10,11 |
| B Destination Address<br>Hold Time After L → H    | 7,8,9,10,11 |
| D Set-up Time Before L → H                        | 7,8,9,10,11 |

| Parameters  | Subgroups   |
|---|-------------|
| D Hold Time After L → H   | 7,8,9,10,11 |
| C <sub>n</sub> Set-up Time Before L → H   | 7,8,9,10,11 |
| C <sub>n</sub> Hold Time After L → H  | 7,8,9,10,11 |
| I <sub>012</sub> Set-up Time Before L → H   | 7,8,9,10,11 |
| I <sub>012</sub> Hold Time After L → H  | 7,8,9,10,11 |
| I <sub>345</sub> Set-up Time Before L → H   | 7,8,9,10,11 |
| I <sub>345</sub> Hold Time After L → H  | 7,8,9,10,11 |
| I <sub>678</sub> Set-up Time Before H → L   | 7,8,9,10,11 |
| I <sub>678</sub> Hold Time After H → L  | 7,8,9,10,11 |
| I <sub>678</sub> Set-up Time Before L → H   | 7,8,9,10,11 |
| I <sub>678</sub> Hold Time After L → H  | 7,8,9,10,11 |
| RAM <sub>0</sub> , RAM <sub>3</sub> , Q <sub>0</sub> , Q <sub>3</sub><br>Set-up Time Before L → H | 7,8,9,10,11 |
| RAM <sub>0</sub> , RAM <sub>3</sub> , Q <sub>0</sub> , Q <sub>3</sub><br>Hold Time After L → H    | 7,8,9,10,11 |

Document #: 38-00008-B



Features

- **Fast**
  - CY2909A/11A has a 40 ns (min.) clock to output cycle time; commercial
  - CY2909/11 has a 40 ns (min.) clock to output cycle time; military
- **Low power**
  - I<sub>CC</sub> (max.) = 70 mA commercial
  - I<sub>CC</sub> (max.) = 90 mA military
- **V<sub>CC</sub> margin**
  - 5V ±10%
  - All parameters guaranteed over commercial and military operating temperature range
- **Expandable**
  - Infinitely expandable in 4-bit increments

- **ESD protection**
  - Capable of withstanding greater than 2000V static discharge voltage
- **Pin compatible and functional equivalent to AMD AM2909A/AM2911A**

Description

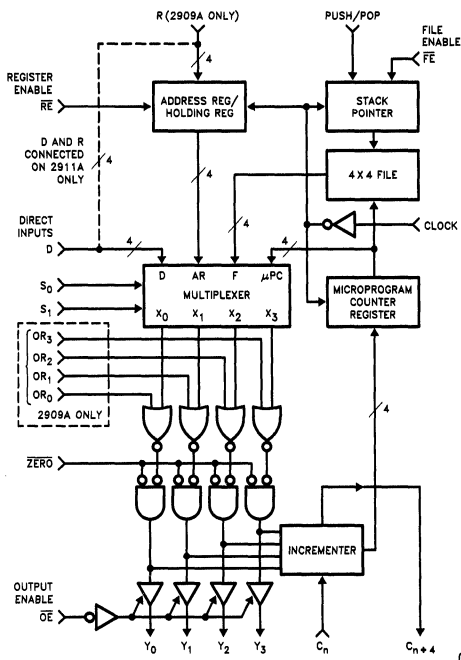
The CY2909A and CY2911A are high-speed, four-bit wide address sequencers intended for controlling the sequence of execution of microinstructions contained in microprogram memory. They may be connected in parallel to expand the address width in 4 bit increments. Both devices are implemented in high performance CMOS for optimum speed and power.

The CY2909A can select an address from any of four sources. They are:

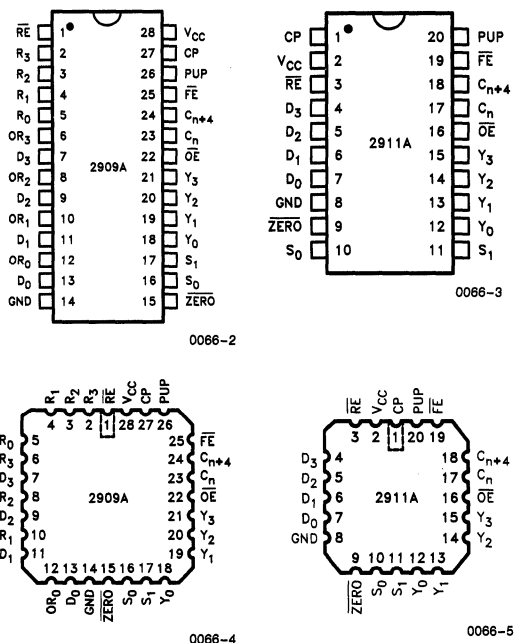
1) a set of four external direct inputs (D<sub>i</sub>); 2) external data stored in an internal register (R<sub>i</sub>); 3) a four word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs (Y<sub>i</sub>) can be OR'ed with an external input for conditional skip or branch instructions. A ZERO input line forces the outputs to all zeros. The outputs are three state, controlled by the Output Enable (OE) input.

The CY2911A is an identical circuit to the CY2909A, except the four OR inputs are removed and the D and R inputs are tied together. The CY2911A is available in a 20-pin, 300-mil package. The CY2909 is available in a 28-pin, 600-mil package.

Logic Block Diagram



Pin Configurations





### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential .... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Output Current, into Outputs (Low) ..... 30 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883 Method 3015)

Latch-Up Current ..... >200 mA

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[4]</sup>

| Parameters      | Description                                 | Test Conditions   | Min.       | Max.            | Units |
|-----------------|---|---|------------|-----------------|-------|
| V <sub>OH</sub> | Output HIGH Voltage                         | V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.6 mA (Comm.) | 2.4        |                 | V     |
|                 |   | V <sub>CC</sub> = Min., I <sub>OH</sub> = -1.0 mA (Mil.)  | 2.4        |                 | V     |
| V <sub>OL</sub> | Output LOW Voltage                          | V <sub>CC</sub> = Min., I <sub>OL</sub> = 16.0 mA         |            | 0.4             | V     |
| V <sub>IH</sub> | Input High Voltage                          |   | 2.0        | V <sub>CC</sub> | V     |
| V <sub>IL</sub> | Input Low Voltage                           |   | -2.0       | 0.8             | V     |
| I <sub>IX</sub> | Input Load Current                          | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                    | -10        | +10             | μA    |
| I <sub>OZ</sub> | Output Leakage Current                      | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub><br>Output Disabled | -20        | +20             | μA    |
| I <sub>OS</sub> | Output Short Circuit Current <sup>[1]</sup> | V <sub>CC</sub> = Max.      V <sub>OUT</sub> = GND        | -30        | -85             | mA    |
| I <sub>CC</sub> | V <sub>CC</sub> Operating Supply Current    | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA         | Commercial | 70              | mA    |
|                 |   |   | Military   | 90              |       |

### Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 7    |       |

#### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

### AC Test Loads and Waveforms

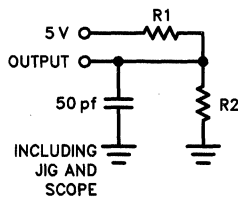


Figure 1a

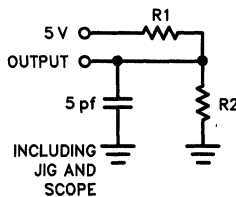


Figure 1b

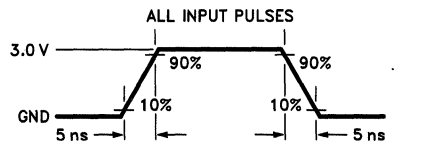


Figure 2

0066-6

0066-7

|                | Commercial | Military |
|----------------|------------|----------|
| R <sub>1</sub> | 254Ω       | 258Ω     |
| R <sub>2</sub> | 187Ω       | 216Ω     |

**Switching Characteristics** Over Operating Range<sup>[4]</sup>

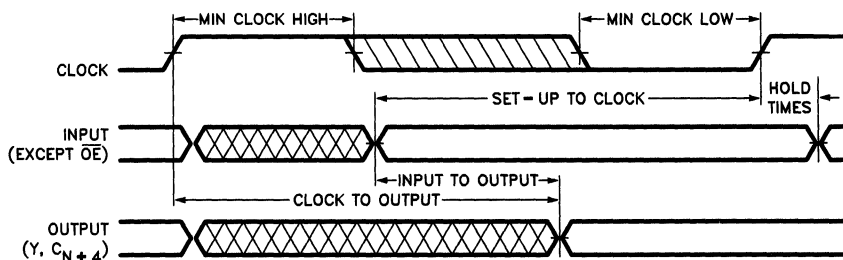
|   | 2909A<br>2911A |             | 2909A<br>2911A |             | Units |
|---|----------------|-------------|----------------|-------------|-------|
|   | Commercial     |             | Military       |             |       |
| Minimum Clock Low Time  | 20             |             | 20             |             | ns    |
| Minimum Clock High Time   | 20             |             | 20             |             | ns    |
| <b>MAXIMUM COMBINATIONAL PROPAGATION DELAYS</b>   |                |             |                |             |       |
| From Input To:  | Y              | $C_N + 4$   | Y              | $C_N + 4$   | ns    |
| $D_i$   | 17             | 22          | 20             | 25          | ns    |
| $S_0, S_1$  | 29             | 34          | 29             | 34          | ns    |
| $OR_i$ CY2909A  | 17             | 22          | 20             | 25          | ns    |
| $C_N$   | —              | 14          | —              | 16          | ns    |
| $\overline{ZERO}$   | 29             | 34          | 30             | 35          | ns    |
| $\overline{OE}$ Low to Output   | 25             | —           | 25             | —           | ns    |
| $\overline{OE}$ High to High Z <sup>[5]</sup>   | 25             | —           | 25             | —           | ns    |
| Clock High, $S_0, S_1 = LH$   | 39             | 44          | 45             | 50          | ns    |
| Clock High, $S_0, S_1 = LL$   | 39             | 44          | 45             | 50          | ns    |
| Clock High, $S_0, S_1 = HL$   | 44             | 49          | 53             | 58          | ns    |
| <b>MINIMUM SET-UP AND HOLD TIMES (All Times Relative to Clock LOW to HIGH Transition)</b> |                |             |                |             |       |
| <b>From Input</b>   | <b>Set-up</b>  | <b>Hold</b> | <b>Set-up</b>  | <b>Hold</b> |       |
| $\overline{RE}$   | 19             | 4           | 19             | 5           | ns    |
| $R_i$ [6]   | 10             | 4           | 12             | 5           | ns    |
| Push/Pop  | 25             | 4           | 27             | 5           | ns    |
| FE  | 25             | 4           | 27             | 5           | ns    |
| $C_N$   | 18             | 4           | 18             | 5           | ns    |
| $D_i$   | 25             | 0           | 25             | 0           | ns    |
| $OR_i$ (CY2909A)  | 25             | 0           | 25             | 0           | ns    |
| $S_0, S_1$  | 25             | 0           | 29             | 0           | ns    |
| $\overline{ZERO}$   | 25             | 0           | 29             | 0           | ns    |

Notes:

5. Output Loading as in Figure 1b.

6.  $R_i$  and  $D_i$  are internally connected on the CY2911A. Use  $R_i$  set-up and hold times for  $D_i$  inputs.

**Switching Waveforms**



0086-8

**Ordering Information**

| Ordering Code                       | Package Type      | Operating Range |
|-------------------------------------|-------------------|-----------------|
| CY2909APC<br>CY2909ADC<br>CY2909ALC | P15<br>D16<br>L64 | Commercial      |
| CY2909ADMB<br>CY2909ALMB            | D16<br>L64        | Military        |

| Ordering Code                       | Package Type    | Operating Range |
|-------------------------------------|-----------------|-----------------|
| CY2911APC<br>CY2911ADC<br>CY2911ALC | P5<br>D6<br>L61 | Commercial      |
| CY2911ADMB<br>CY2911ALMB            | D6<br>L61       | Military        |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL</sub> Max. | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>OS</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |

#### Switching Characteristics

| Parameters   | Subgroups   |
|--|-------------|
| Minimum Clock Low Time   | 7,8,9,10,11 |
| Minimum Clock High Time  | 7,8,9,10,11 |
| <b>MAXIMUM COMBINATIONAL PROPAGATION DELAYS</b>                      |             |
| D <sub>i</sub> to Y  | 7,8,9,10,11 |
| D <sub>i</sub> to C <sub>N+4</sub>                                   | 7,8,9,10,11 |
| S <sub>0</sub> , S <sub>1</sub> to Y                                 | 7,8,9,10,11 |
| S <sub>0</sub> , S <sub>1</sub> to C <sub>N+4</sub>                  | 7,8,9,10,11 |
| OR <sub>i</sub> (CY2909A) to Y                                       | 7,8,9,10,11 |
| OR <sub>i</sub> (CY2909A) to C <sub>N+4</sub>                        | 7,8,9,10,11 |
| C <sub>N</sub> to C <sub>N+4</sub>                                   | 7,8,9,10,11 |
| ZER $\bar{O}$ to C <sub>N+4</sub>                                    | 7,8,9,10,11 |
| Clock High, S <sub>0</sub> , S <sub>1</sub> = LH to Y                | 7,8,9,10,11 |
| Clock High, S <sub>0</sub> , S <sub>1</sub> = LH to C <sub>N+4</sub> | 7,8,9,10,11 |
| Clock High, S <sub>0</sub> , S <sub>1</sub> = LL to Y                | 7,8,9,10,11 |
| Clock High, S <sub>0</sub> , S <sub>1</sub> = LL to C <sub>N+4</sub> | 7,8,9,10,11 |
| Clock High, S <sub>0</sub> , S <sub>1</sub> = HL to Y                | 7,8,9,10,11 |
| Clock High, S <sub>0</sub> , S <sub>1</sub> = HL to C <sub>N+4</sub> | 7,8,9,10,11 |

| Parameters                                  | Subgroups   |
|---|-------------|
| <b>MINIMUM SET-UP AND HOLD TIMES</b>        |             |
| RE Set-up Time                              | 7,8,9,10,11 |
| RE Hold Time                                | 7,8,9,10,11 |
| Push/Pop Set-up Time                        | 7,8,9,10,11 |
| Push/Pop Hold Time                          | 7,8,9,10,11 |
| FE Set-up Time                              | 7,8,9,10,11 |
| FE Hold Time                                | 7,8,9,10,11 |
| C <sub>N</sub> Set-up Time                  | 7,8,9,10,11 |
| C <sub>N</sub> Hold Time                    | 7,8,9,10,11 |
| D <sub>i</sub> Set-up Time                  | 7,8,9,10,11 |
| D <sub>i</sub> Hold Time                    | 7,8,9,10,11 |
| OR <sub>i</sub> (CY2909A) Set-up Time       | 7,8,9,10,11 |
| OR <sub>i</sub> (CY2909A) Hold Time         | 7,8,9,10,11 |
| S <sub>0</sub> , S <sub>1</sub> Set-up Time | 7,8,9,10,11 |
| S <sub>0</sub> , S <sub>1</sub> Hold Time   | 7,8,9,10,11 |
| ZER $\bar{O}$ Set-up Time                   | 7,8,9,10,11 |
| ZER $\bar{O}$ Hold Time                     | 7,8,9,10,11 |

Document #: 38-00009-B



# CMOS Microprogram Controller

## Features

- **Fast**
  - CY2910AC has a 50 ns (min.) clock cycle; commercial
  - CY2910AM has a 51 ns (min.) clock cycle; military
- **Low power**
  - $I_{CC}$  (max.) = 170 mA
- **$V_{CC}$  Margin  $5V \pm 10\%$  commercial and military**
- **Sixteen powerful microinstructions**
- **Three output enable controls for three-way branch**
- **Twelve-bit address word**
- **Four sources for addresses: microprogram counter (MPC), branch address bus, 9-word stack, internal holding register**
- **Internal 9-word by 12-bit stack**  
The internal stack can be used for subroutine return address or data storage

- **12-bit Internal loop counter**
- **ESD protection**  
Capable of withstanding over 2000 volts static discharge voltage
- **Pin compatible and functional equivalent to Am2910A**

## Functional Description

The CY2910A is a stand-alone microprogram controller that selects, stores, retrieves, manipulates and tests addresses that control the sequence of execution of instructions stored in an external memory. All addresses are 12-bit binary values that designate an absolute memory location.

The CY2910A, as illustrated in the block diagram, consists of a 9-word by 12-bit LIFO (Last-In-First-Out) stack and SP (Stack Pointer), a 12-bit RC (Register/Counter), a 12-bit MPC (Microprogram Counter) and incrementer, a 12-bit wide by 4-input multiplexer

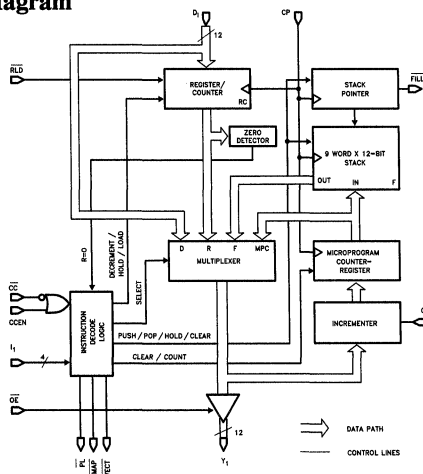
and the required data manipulation and control logic.

The operation performed is determined by four input instruction lines (I0–I3) that in turn select the (internal) source of the next micro-instruction to be fetched. This address is output on the Y0–Y11 pins. Two additional inputs (CC and CCEN) are provided that are examined during certain instructions and enable the user to make the execution of the instruction either unconditional or dependent upon an external test.

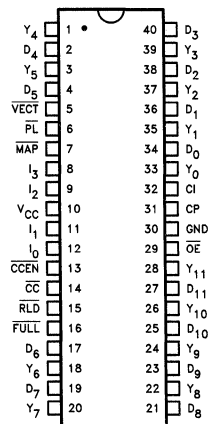
The CY2910A is a pin compatible, functional equivalent, improved performance replacement for the Am2910A.

The CY2910A is fabricated using an advanced 1.2 micron CMOS process that eliminates latchup, results in ESD protection of over 2000 volts and achieves superior performance and low power dissipation.

## Logic Block Diagram



## Pin Configuration



0040-2

0040-3

Top View

## Selection Guide

| Clock Cycle (Min.) in ns | Stack Depth | Operating Range | Part Number |
|--------------------------|-------------|-----------------|-------------|
| 50                       | 9 words     | Commercial      | CY2910AC    |
| 51                       | 9 words     | Military        | CY2910AM    |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature                                   | -65°C to +150°C |
| Ambient Temperature with Power Applied                | -55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 10 to Pin 30) | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State         | -0.5V to +7.0V  |
| DC Input Voltage                                      | -3.0V to +7.0V  |
| Output Current into Outputs (Low)                     | 30 mA           |

|  |          |
|--|----------|
| Static Discharge Voltage (Per MIL-STD-883 Method 3015) | > 2001V  |
| Latchup Current (Outputs)                              | > 200 mA |

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Commercial and Military Operating Range<sup>[4]</sup>

V<sub>CC</sub> Min. = 4.5V, V<sub>CC</sub> Max. = 5.5V

| Parameter       | Description                  | Test Condition   | Min. | Max.            | Units |
|-----------------|------------------------------|--|------|-----------------|-------|
| V <sub>OH</sub> | Output HIGH Voltage          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -1.6 mA              | 2.4  |                 | V     |
| V <sub>OL</sub> | Output LOW Voltage           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8 mA                 |      | 0.5             | V     |
| V <sub>IH</sub> | Input HIGH Voltage           |  | 2.0  | V <sub>CC</sub> | V     |
| V <sub>IL</sub> | Input LOW Voltage            |  | -3.0 | 0.8             | V     |
| I <sub>IH</sub> | Input HIGH Current           | V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>CC</sub>      |      | 10              | μA    |
| I <sub>IL</sub> | Input LOW Current            | V <sub>CC</sub> = Max., V <sub>IN</sub> = GND                  |      | -10             | μA    |
| I <sub>OH</sub> | Output HIGH Current          | V <sub>CC</sub> = Min., V <sub>IH</sub> = 2.4V                 | -1.6 |                 | mA    |
| I <sub>OL</sub> | Output LOW Current           | V <sub>CC</sub> = Min., V <sub>OL</sub> = 0.5V                 | 8    |                 | mA    |
| I <sub>OZ</sub> | Output Leakage Current       | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND/V <sub>CC</sub> | -40  | +40             | μA    |
| I <sub>SC</sub> | Output Short Circuit Current | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0V                  |      | -85             | mA    |
| I <sub>CC</sub> | Supply Current               | V <sub>CC</sub> = Max.   |      | 170             | mA    |

**5**

### Capacitance<sup>[2]</sup>

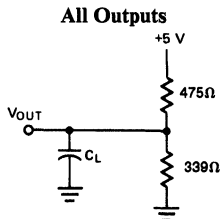
| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 8    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 10   | pF    |

#### Notes:

- Not more than one output should be tested at a time. Duration of the short circuit should not exceed one second.
- Tested initially and after any design or process changes that may affect these parameters.

- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

### Output Load for AC Performance Characteristics

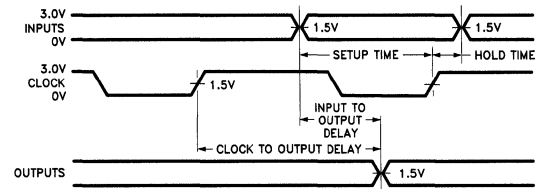


#### Notes:

- C<sub>L</sub> = 50 pF includes scope probe, wiring and stray capacitance.  
 C<sub>L</sub> = 5 pF for output disable tests.

0040-4

### Switching Waveforms



0040-5

### Guaranteed AC Performance Characteristics

The tables below specify the guaranteed AC performance of the CY2910A over the commercial (0°C to +70°C) and the military (-55°C to +125°C) temperature ranges with  $V_{CC}$  varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels.

The inputs switch between 0V and 3V with signal transition rates of 1 Volt per nanosecond. All outputs have maximum DC current loads.

### Clock Requirements<sup>[1, 4]</sup>

|   | Commercial | Military |
|---|------------|----------|
| Minimum Clock LOW                             | 20         | 25       |
| Minimum Clock HIGH                            | 20         | 25       |
| Minimum Clock Period I = 14                   | 50         | 51       |
| Minimum Clock Period<br>I = 8, 9, 15 (Note 2) | 50         | 50       |

### Combinational Propagation Delays. $C_L = 50$ pF<sup>[4]</sup>

| To Output<br>From Input        | Commercial |               |      | Military |               |      |
|--------------------------------|------------|---------------|------|----------|---------------|------|
|                                | Y          | PL, VECT, MAP | FULL | Y        | PL, VECT, MAP | FULL |
| D0–D11                         | 20         | —             | —    | 25       | —             | —    |
| I0–I3                          | 35         | 30            | —    | 40       | 35            | —    |
| $\overline{CC}$                | 30         | —             | —    | 36       | —             | —    |
| $\overline{CCEN}$              | 30         | —             | —    | 36       | —             | —    |
| CP<br>I = 8, 9, 15<br>(Note 2) | 40         | —             | 31   | —        | —             | 35   |
| CP<br>All Other I              | 40         | —             | 31   | 46       | —             | 35   |
| $\overline{OE}$<br>(Note 3)    | 25<br>27   | —             | —    | 25<br>30 | —             | —    |

### Minimum Set-up and Hold Times Relative to clock LOW to HIGH Transition. $C_L = 50$ pF<sup>[4]</sup>

| Input             | Commercial |      | Military |      |
|-------------------|------------|------|----------|------|
|                   | Set-up     | Hold | Set-up   | Hold |
| DI → RC           | 16         | 0    | 16       | 0    |
| DI → MPC          | 30         | 0    | 30       | 0    |
| I0–I3             | 35         | 0    | 38       | 0    |
| $\overline{CC}$   | 24         | 0    | 35       | 0    |
| $\overline{CCEN}$ | 24         | 0    | 35       | 0    |
| CI                | 18         | 0    | 18       | 0    |
| RLD               | 19         | 0    | 20       | 0    |

#### Notes:

1. A dash indicates that a propagation delay path or set-up time does not exist.
2. These instructions are dependent upon the register/counter. Use the shorter delay times if the previous instruction either does not change the register/counter or could only decrement it. Use the longer delay if the instruction prior to the clock was 4 or 12 or if RLD was LOW.
3. The enable/disable times are measured to a 0.5 Volt change on the output voltage level with  $C_L = 5$  pF.
4. See the last page of this specification for Group A subgroup testing information.

**Table of Instructions**

| I <sub>3</sub> -I <sub>0</sub> | MNEMONIC | NAME                     | REG/<br>CNTR<br>CON-<br>TENTS | RESULT                      |       |                            |       |              |        |
|--------------------------------|----------|--------------------------|-------------------------------|-----------------------------|-------|----------------------------|-------|--------------|--------|
|                                |          |                          |                               | FAIL<br>CCEN = L and CC = H |       | PASS<br>CCEN = H or CC = L |       | REG/<br>CNTR | ENABLE |
|                                |          |                          |                               | Y                           | STACK | Y                          | STACK |              |        |
| 0                              | JZ       | Jump Zero                | X                             | 0                           | Clear | 0                          | Clear | Hold         | PL     |
| 1                              | CJS      | Cond JSB PL              | X                             | PC                          | Hold  | D                          | Push  | Hold         | PL     |
| 2                              | JMAP     | Jump Map                 | X                             | D                           | Hold  | D                          | Hold  | Hold         | Map    |
| 3                              | CJP      | Cond Jump PL             | X                             | PC                          | Hold  | D                          | Hold  | Hold         | PL     |
| 4                              | PUSH     | Push/Cond LD CNTR        | X                             | PC                          | Push  | PC                         | Push  | (Note 1)     | PL     |
| 5                              | JSRP     | Cond JSB R/PL            | X                             | R                           | Push  | D                          | Push  | Hold         | PL     |
| 6                              | CJV      | Cond Jump Vector         | X                             | PC                          | Hold  | D                          | Hold  | Hold         | Vect   |
| 7                              | JRP      | Cond Jump R/PL           | X                             | R                           | Hold  | D                          | Hold  | Hold         | PL     |
| 8                              | RFCT     | Repeat Loop,<br>CNTR ≠ 0 | ≠0                            | F                           | Hold  | F                          | Hold  | Dec          | PL     |
|                                |          |                          | =0                            | PC                          | POP   | PC                         | Pop   | Hold         | PL     |
| 9                              | RPCT     | Repeat PL,<br>CNTR ≠ 0   | ≠0                            | D                           | Hold  | D                          | Hold  | Dec          | PL     |
|                                |          |                          | =0                            | PC                          | Hold  | PC                         | Hold  | Hold         | PL     |
| 10                             | CRTN     | Cond RTN                 | X                             | PC                          | Hold  | F                          | Pop   | Hold         | PL     |
| 11                             | CJPP     | Cond Jump PL & Pop       | X                             | PC                          | Hold  | D                          | Pop   | Hold         | PL     |
| 12                             | LDCT     | LD Cntr & Continue       | X                             | PC                          | Hold  | PC                         | Hold  | Load         | PL     |
| 13                             | LOOP     | Test End Loop            | X                             | F                           | Hold  | PC                         | Pop   | Hold         | PL     |
| 14                             | CONT     | Continue                 | X                             | PC                          | Hold  | PC                         | Hold  | Hold         | PL     |
| 15                             | TWB      | Three-Way Branch         | ≠0                            | F                           | Hold  | PC                         | Pop   | Dec          | PL     |
|                                |          |                          | =0                            | D                           | Pop   | PC                         | Pop   | Hold         | PL     |

**Notes:**

 1. If  $\overline{CCEN} = L$  and  $\overline{CC} = H$ , hold; else load.

H = HIGH

L = LOW

X = Don't Care

**Ordering Information**

| Clock Cycle (ns) | Ordering Code | Package Type | Operating Range |
|------------------|---------------|--------------|-----------------|
| 50               | CY2910ADC     | D18          | Commercial      |
|                  | CY2910AJC     | J67          |                 |
|                  | CY2910ALC     | L67          |                 |
|                  | CY2910APC     | P17          |                 |
| 51               | CY2910ADMB    | D18          | Military        |
|                  | CY2910ALMB    | L67          |                 |

**5**



**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IH</sub>      | 1,2,3     |
| I <sub>IL</sub>      | 1,2,3     |
| I <sub>OH</sub>      | 1,2,3     |
| I <sub>OL</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>SC</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |

**Clock Requirements**

| Parameters        | Subgroups   |
|-------------------|-------------|
| Minimum Clock LOW | 7,8,9,10,11 |

**Combinational Propagation Delays**

| Parameters   | Subgroups   |
|--|-------------|
| From D0–D11 to Y   | 7,8,9,10,11 |
| From I0–I3 to Y  | 7,8,9,10,11 |
| From I0–I3 to $\overline{PL}$ , $\overline{VECT}$ , $\overline{MAP}$ | 7,8,9,10,11 |
| From $\overline{CC}$ to Y  | 7,8,9,10,11 |
| From $\overline{CCEN}$ to Y  | 7,8,9,10,11 |
| From CP (I = 8, 9, 15) to $\overline{FULL}$                          | 7,8,9,10,11 |
| From CP (All Other I) to Y   | 7,8,9,10,11 |
| From CP (All Other I) to $\overline{FULL}$                           | 7,8,9,10,11 |

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**Minimum Set-up and Hold Times**

| Parameters                    | Subgroups   |
|-------------------------------|-------------|
| DI → RC Set-up Time           | 7,8,9,10,11 |
| DI → RC Hold Time             | 7,8,9,10,11 |
| DI → MPC Set-up Time          | 7,8,9,10,11 |
| DI → MPC Hold Time            | 7,8,9,10,11 |
| I0–I3 Set-up Time             | 7,8,9,10,11 |
| I0–I3 Hold Time               | 7,8,9,10,11 |
| $\overline{CC}$ Set-up Time   | 7,8,9,10,11 |
| $\overline{CC}$ Hold Time     | 7,8,9,10,11 |
| $\overline{CCEN}$ Set-up Time | 7,8,9,10,11 |
| $\overline{CCEN}$ Hold Time   | 7,8,9,10,11 |
| CI Set-up Time                | 7,8,9,10,11 |
| CI Hold Time                  | 7,8,9,10,11 |
| RLD Set-up Time               | 7,8,9,10,11 |
| RLD Hold Time                 | 7,8,9,10,11 |



**Features**

- 1.2/2 MHz data rate
- Fully TTL compatible
- Independent asynchronous inputs and outputs
- Direct replacement for PMOS 3341
- Expandable in word length and width
- CMOS for optimum speed/power
- Capable of withstanding greater than 2000V electrostatic discharge

**Functional Description**

The 3341 is a 64-word x 4-bit First-In First-Out (FIFO) Serial Memory. The inputs and outputs are completely independent (no common clocks) making the 3341 ideal for asynchronous buffer applications.

Control signals are provided for both vertical and horizontal expansion.

The 3341 is manufactured using Cypress CMOS technology and is available in both ceramic and plastic packages.

**Data Input**

The four bits of data on the D<sub>0</sub> through D<sub>3</sub> inputs are entered into the first location when both Input Ready (IR) and Shift In (SI) are HIGH. This causes IR to go LOW but data will stay locked in the first bit location until both IR and SI are LOW. Then data will propagate to the second bit location, provided the location is empty. When data is transferred, IR will go HIGH indicating that the device is ready to accept new data. If the memory is full, IR will stay LOW.

**Data Transfer**

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus, data will stack up at the end of the device while empty locations will “bubble” to the front. t<sub>BT</sub> defines the time required for the first data to travel from the input to the output of a previously empty device, or for the first empty space to travel from the output to the input of a previously full device.

**Data Output**

When data has been transferred into the last cell, Output Ready (OR) goes

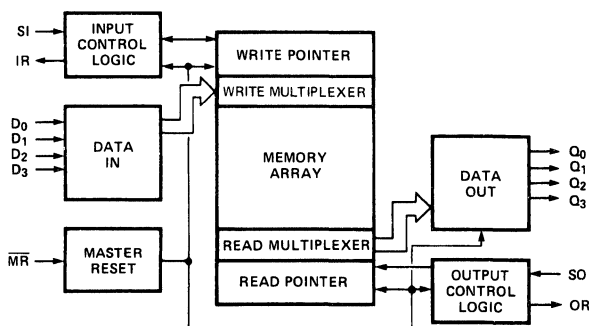
HIGH, indicating the presence of valid data at the output pins Q<sub>0</sub> through Q<sub>3</sub>. The transfer of data is initiated when both the Output Ready output from the device and the Shift Out (SO) input to the device are HIGH. This causes OR to go LOW; output data, however, is maintained until both OR and SO are LOW. Then the content of the adjacent (upstream) cell (provided it is full) will be transferred into the last cell, causing OR to go HIGH again. If the memory has been emptied, OR will stay LOW.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t<sub>BT</sub>) or completely empty (Output Ready stays LOW for at least t<sub>BT</sub>).

**Reset**

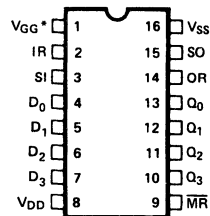
When Master Reset ( $\overline{MR}$ ) goes LOW, the control logic is cleared, and the data outputs enter a LOW state. When  $\overline{MR}$  returns HIGH, Output Ready (OR) stays LOW, and Input Ready (IR) goes HIGH if Shift In (SI) was LOW.

**Logic Block Diagram**



0004-1

**Pin Configuration**



\*Internally not connected

0004-2

**Selection Guide**

|                                |            | 3341    | 3341-2  |
|--------------------------------|------------|---------|---------|
| Maximum Operating Frequency    |            | 1.2 MHz | 2.0 MHz |
| Maximum Operating Current (mA) | Commercial | 45      | 45      |
|                                | Military   | 60      | 60      |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential

(Pin 16 to Pin 8) ..... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Output Current, into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883 Method 3015)

Latchup Current ..... >200 mA

### Operating Range

| Range                   | Ambient Temperature | V <sub>SS</sub> | V <sub>DD</sub> | V <sub>GG</sub> * |
|-------------------------|---------------------|-----------------|-----------------|-------------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        | GND             | NC                |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ± 10%        | GND             | NC                |

\*Internally Not Connected.

### Electrical Characteristics Over the Operating Range<sup>[4]</sup>

| Parameters      | Description                                 | Test Conditions  | Min.       | Max.            | Units |
|-----------------|---|--|------------|-----------------|-------|
| V <sub>OH</sub> | Output HIGH Voltage                         | V <sub>SS</sub> = Min., I <sub>OH</sub> = -0.3 mA          | 2.4        |                 | V     |
| V <sub>OL</sub> | Output LOW Voltage                          | V <sub>SS</sub> = Min., I <sub>OL</sub> = 1.6 mA           |            | 0.4             | V     |
| V <sub>IH</sub> | Input HIGH Voltage                          |  | 2.0        | V <sub>SS</sub> | V     |
| V <sub>IL</sub> | Input LOW Voltage                           |  | -3.0       | 0.8             | V     |
| I <sub>IX</sub> | Input Leakage Current                       | V <sub>DD</sub> ≤ V <sub>I</sub> ≤ V <sub>SS</sub>         | -10        | +10             | μA    |
| I <sub>OS</sub> | Output Short Circuit Current <sup>[1]</sup> | V <sub>SS</sub> = Max., V <sub>OUT</sub> = V <sub>DD</sub> |            | -90             | mA    |
| I <sub>DD</sub> | Power Supply Current                        | V <sub>SS</sub> = Max.,<br>I <sub>OUT</sub> = 0 mA         | Commercial | 45              | mA    |
|                 |   |  | Military   | 60              |       |
| I <sub>GG</sub> | V <sub>GG</sub> Current                     |  |            | 0               | mA    |

### Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions                  | Max. | Units |
|------------------|--------------------|----------------------------------|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz | 7    | pF    |
| C <sub>OUT</sub> | Output Capacitance | V <sub>SS</sub> = 5.0V           | 10   |       |

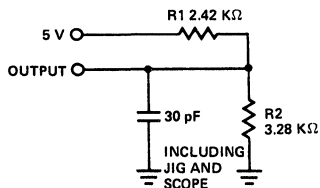
#### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

3. T<sub>A</sub> is the "instant on" case temperature.

4. See the last page of this specification for Group A subgroup testing information.

### AC Test Loads and Waveforms



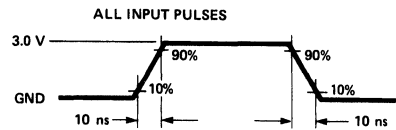
0004-3

Equivalent to:

THÉVENIN EQUIVALENT



0004-4



0004-5

Switching Characteristics Over the Operating Range<sup>[4, 5]</sup>

| Parameters        | Description                     | Test Conditions | 3341 |      | 3341-2 |      | Units |
|-------------------|---------------------------------|-----------------|------|------|--------|------|-------|
|                   |                                 |                 | Min. | Max. | Min.   | Max. |       |
| f <sub>MAX</sub>  | Operating Frequency             | Note 6          |      | 1.2  |        | 2    | MHz   |
| t <sub>PHSI</sub> | SI HIGH Time                    |                 | 80   |      | 80     |      | ns    |
| t <sub>PLSI</sub> | SI LOW Time                     |                 | 80   |      | 80     |      | ns    |
| t <sub>DD</sub>   | Data Setup to SI                |                 | 0    |      | 0      |      | ns    |
| t <sub>HSI</sub>  | Data Hold from SI               |                 | 200  |      | 100    |      | ns    |
| t <sub>IR+</sub>  | Delay, SI HIGH to IR LOW        |                 | 20   | 350  | 20     | 160  | ns    |
| t <sub>IR-</sub>  | Delay, SI LOW to IR HIGH        |                 | 20   | 450  | 20     | 200  | ns    |
| t <sub>PHSO</sub> | SO HIGH Time                    |                 | 80   |      | 80     |      | ns    |
| t <sub>PLSO</sub> | SO LOW Time                     |                 | 80   |      | 80     |      | ns    |
| t <sub>OR+</sub>  | Delay, SO HIGH to OR LOW        |                 | 20   | 370  | 20     | 160  | ns    |
| t <sub>OR-</sub>  | Delay, SO LOW to OR HIGH        |                 | 20   | 450  | 20     | 200  | ns    |
| t <sub>DA</sub>   | Data Setup to OR HIGH           |                 | 0    |      | 0      |      | ns    |
| t <sub>DH</sub>   | Data Hold from OR LOW           |                 | 75   |      | 20     |      | ns    |
| t <sub>BT</sub>   | Bubble through Time             |                 |      | 1000 |        | 500  | ns    |
| t <sub>MRW</sub>  | $\overline{MR}$ Pulse Width     |                 | 400  |      | 200    |      | ns    |
| t <sub>DSI</sub>  | $\overline{MR}$ HIGH to SI HIGH |                 | 30   |      | 30     |      | ns    |
| t <sub>DOR</sub>  | $\overline{MR}$ LOW to OR LOW   |                 |      | 400  |        | 200  | ns    |
| t <sub>DIR</sub>  | $\overline{MR}$ LOW to IR HIGH  |                 |      | 400  |        | 200  | ns    |

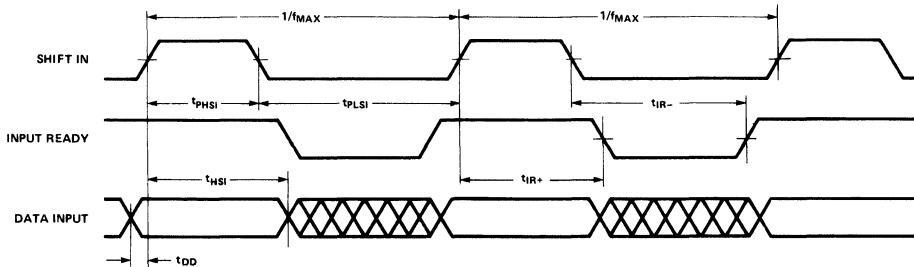
Notes:

5. Test conditions assume signal transitions of 10 ns or less. Timing reference levels of 1.5V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.

6.  $1/f_{MAX} > t_{PHSI} + t_{IR-}$ ,  $1/f_{MAX} > t_{PHSO} + t_{OR-}$ .

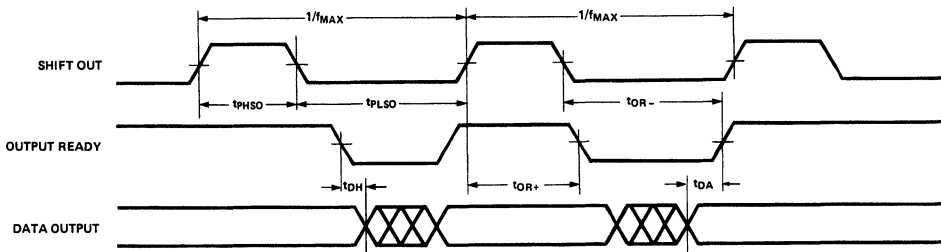
Switching Waveforms

Data In Timing Diagram



0004-6

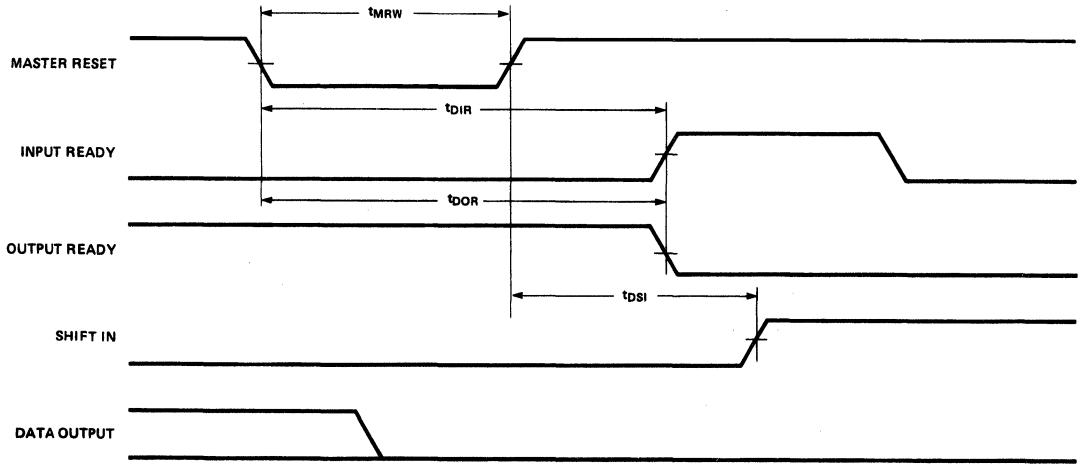
Data Out Timing Diagram



0004-7

**Switching Waveforms (Continued)**

**Master Reset Timing Diagram**



0004-8

**Ordering Information**

| Ordering Code<br>(1.2 MHz) | Package<br>Type | Operating<br>Range |
|----------------------------|-----------------|--------------------|
| CY3341PC<br>CY3341DC       | P1<br>D2        | Commercial         |
| CY3341DMB                  | D2              | Military           |

| Ordering Code<br>(2 MHz) | Package<br>Type | Operating<br>Range |
|--------------------------|-----------------|--------------------|
| CY3341-2PC<br>CY3341-2DC | P1<br>D2        | Commercial         |
| CY3341-2DMB              | D2              | Military           |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>DD</sub>      | 1,2,3     |

#### Switching Characteristics

| Parameters        | Subgroups   |
|-------------------|-------------|
| f <sub>MAX</sub>  | 7,8,9,10,11 |
| t <sub>PHSI</sub> | 7,8,9,10,11 |
| t <sub>PLSI</sub> | 7,8,9,10,11 |
| t <sub>DD</sub>   | 7,8,9,10,11 |
| t <sub>HSI</sub>  | 7,8,9,10,11 |
| t <sub>IR+</sub>  | 7,8,9,10,11 |
| t <sub>IR-</sub>  | 7,8,9,10,11 |
| t <sub>PHSO</sub> | 7,8,9,10,11 |
| t <sub>PLSO</sub> | 7,8,9,10,11 |
| t <sub>OR+</sub>  | 7,8,9,10,11 |
| t <sub>OR-</sub>  | 7,8,9,10,11 |
| t <sub>DA</sub>   | 7,8,9,10,11 |
| t <sub>DH</sub>   | 7,8,9,10,11 |
| t <sub>BT</sub>   | 7,8,9,10,11 |
| t <sub>MRW</sub>  | 7,8,9,10,11 |
| t <sub>DSI</sub>  | 7,8,9,10,11 |
| t <sub>DOR</sub>  | 7,8,9,10,11 |
| t <sub>DIR</sub>  | 7,8,9,10,11 |

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### Features

- 64 x 4 (CY7C401 and CY7C403)  
64 x 5 (CY7C402 and CY7C404)  
High speed first-in first-out memory (FIFO)
- Processed with high-speed CMOS for optimum speed/power
- 25 MHz data rates
- 50 ns bubble-through time—  
25 MHz
- Expandable in word width and/or length
- 5 volt power supply  $\pm 10\%$  tolerance both commercial and military
- Independent asynchronous inputs and outputs
- TTL compatible interface
- Output enable function available on CY7C403 and CY7C404
- Capable of withstanding greater than 2001V electrostatic discharge

- Pin compatible with MMI 67401A/67402A

### Functional Description

The CY7C401 and CY7C403 are asynchronous first-in first-out memories (FIFOs) organized as 64 four bit words. The CY7C402 and CY7C404 are similar FIFOs organized as 64 five bit words. Both the CY7C403 and CY7C404 have an Output Enable (OE) function.

The devices accept 4/5 bit words at the data input (DI<sub>0</sub>–DI<sub>n</sub>) under the control of the Shift In (SI) input. The stored words stack up at the output (DO<sub>0</sub>–DO<sub>n</sub>) in the order they were entered. A read command on the Shift Out (SO) input causes the next to last word to move to the output and all data shifts down once in the stack. The Input Ready (IR) signal acts as a flag to indicate when the input is ready to accept new data (HIGH), to indicate when the FIFO is full (LOW), and to provide a signal for cascading. The

Output Ready (OR) signal is a flag to indicate the output contains valid data (HIGH), to indicate the FIFO is empty (LOW), and to provide a signal for cascading.

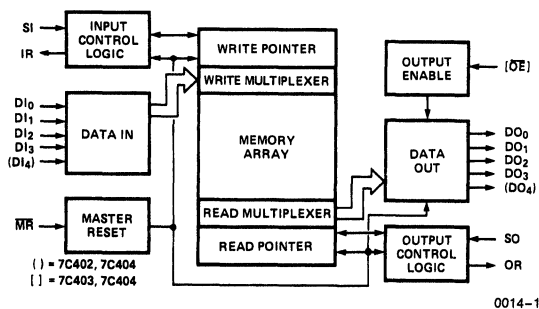
Parallel expansion for wider words is accomplished by logically ANDing the Input Ready (IR) and Output Ready (OR) signals to form composite signals.

Serial expansion is accomplished by tying the data inputs of one device to the data outputs of the previous device.

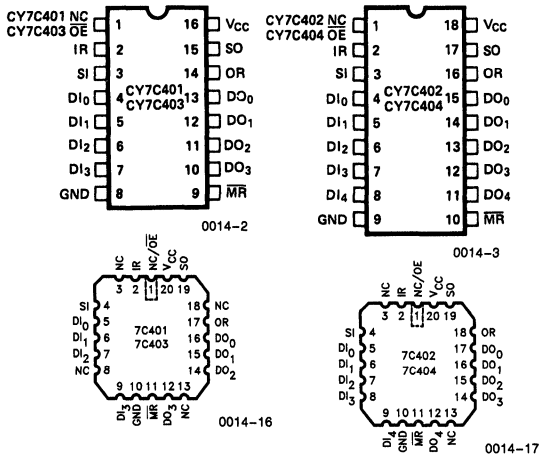
The Input Ready (IR) pin of the receiving device is connected to the Shift Out (SO) pin of the sending device, and the Output Ready (OR) pin of the sending device is connected to the Shift In (SI) pin of the receiving device.

Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely differing operating frequencies. The 25 MHz operation makes these FIFOs ideal for high speed communication and controller applications.

### Logic Block Diagram



### Pin Configurations



### Selection Guide

|                                |            | 7C401/2-5 | 7C40X-10 | 7C40X-15 | 7C40X-25 |
|--------------------------------|------------|-----------|----------|----------|----------|
| Maximum Shift Rate (MHz)       |            | 5         | 10       | 15       | 25       |
| Maximum Operating Current (mA) | Commercial | 75        | 75       | 75       | 75       |
|                                | Military   | —         | 90       | 90       | 90       |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature .....                           | -65°C to +150°C |
| Ambient Temperature with Power Applied .....        | -55°C to +125°C |
| Supply Voltage to Ground Potential ....             | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State ..... | -0.5V to +7.0V  |
| DC Input Voltage .....                              | -3.0V to +7.0V  |
| Power Dissipation .....                             | 1.0W            |
| Output Current, into Outputs (Low) .....            | 20 mA           |

Static Discharge Voltage .....

(per MIL-STD-883 Method 3015) > 2001V

Latch-up Current .....

> 200 mA

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ± 10%        |

## Electrical Characteristics Over Operating Range (Unless Otherwise Noted)<sup>[4]</sup>

| Parameters                     | Description                                 | Test Conditions  | 7C40X-10, 15, 25 |      | Units |
|--------------------------------|---|--|------------------|------|-------|
|                                |   |  | Min.             | Max. |       |
| V <sub>OH</sub>                | Output HIGH Voltage                         | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA  | 2.4              |      | V     |
| V <sub>OL</sub>                | Output LOW Voltage                          | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA   |                  | 0.4  | V     |
| V <sub>IH</sub>                | Input HIGH Voltage                          |  | 2.0              | 6.0  | V     |
| V <sub>IL</sub>                | Input LOW Voltage                           |  | -3.0             | 0.8  | V     |
| I <sub>IX</sub>                | Input Leakage Current                       | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -10              | +10  | μA    |
| V <sub>CD</sub> <sup>[1]</sup> | Input Diode Clamp Voltage <sup>[1]</sup>    |  |                  |      |       |
| I <sub>OZ</sub>                | Output Leakage Current                      | GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , V <sub>CC</sub> = 5.5V<br>Output Disabled (CY7C403 and CY7C404) | -50              | +50  | μA    |
| I <sub>OS</sub>                | Output Short Circuit Current <sup>[2]</sup> | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND   |                  | -90  | mA    |
| I <sub>CC</sub>                | Power Supply Current                        | V <sub>CC</sub> = Max.,<br>I <sub>OUT</sub> = 0 mA   | Commercial       | 75   | mA    |
|                                |   |  | Military         | 90   | mA    |

## Capacitance<sup>[5]</sup>

| Parameters       | Description        | Test Conditions                  | Max. | Units |
|------------------|--------------------|----------------------------------|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance | V <sub>CC</sub> = 4.5V           | 7    |       |

### Notes:

1. The CMOS process does not provide a clamp diode. However, the FIFO is insensitive to -3V dc input levels and -5V undershoot pulses of less than 10 ns (measured at 50% point).
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

3. T<sub>A</sub> is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. Tested initially and after any design or process changes that may affect these parameters.

### Note:

For more information on FIFOs, please refer to the FIFO Application Brief in the Appendix of this book.



## AC Test Load and Waveform

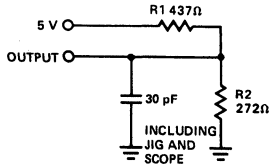


Figure 1a

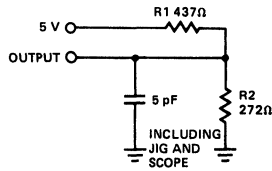
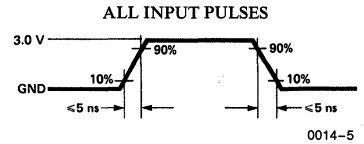
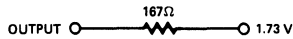


Figure 1b



Equivalent to: THÉVENIN EQUIVALENT



0014-6

## Switching Characteristics Over the Operating Range<sup>[4, 6]</sup>

| Parameters | Description                | Test Conditions | 7C401-5<br>7C402-5 |      | 7C40X-10 |      | 7C40X-15 |      | 7C40X-25 <sup>[12]</sup> |       | Units |
|------------|----------------------------|-----------------|--------------------|------|----------|------|----------|------|--------------------------|-------|-------|
|            |                            |                 | Min.               | Max. | Min.     | Max. | Min.     | Max. | Min.                     | Max.  |       |
| $f_O$      | Operating Frequency        | Note 7          |                    | 5    |          | 10   |          | 15   |                          | 25    | MHz   |
| $t_{PHSI}$ | SI HIGH Time               |                 | 20                 |      | 20       |      | 20       |      | 11                       |       | ns    |
| $t_{PLSI}$ | SI LOW Time                |                 | 45                 |      | 30       |      | 25       |      | 20                       |       | ns    |
| $t_{SSI}$  | Data Setup to SI           | Note 8          | 0                  |      | 0        |      | 0        |      | 0                        |       | ns    |
| $t_{HSI}$  | Data Hold from SI          | Note 8          | 60                 |      | 40       |      | 30       |      | 20                       |       | ns    |
| $t_{DLIR}$ | Delay, SI HIGH to IR LOW   |                 |                    | 75   |          | 40   |          | 35   |                          | 21/22 | ns    |
| $t_{DHIR}$ | Delay, SI LOW to IR HIGH   |                 |                    | 75   |          | 45   |          | 40   |                          | 28/30 | ns    |
| $t_{PHSO}$ | SO HIGH Time               |                 | 20                 |      | 20       |      | 20       |      | 11                       |       | ns    |
| $t_{PLSO}$ | SO LOW Time                |                 | 45                 |      | 25       |      | 25       |      | 20                       |       | ns    |
| $t_{DLOR}$ | Delay, SO HIGH to OR LOW   |                 |                    | 75   |          | 40   |          | 35   |                          | 19/21 | ns    |
| $t_{DHOR}$ | Delay, SO LOW to OR HIGH   |                 |                    | 80   |          | 55   |          | 40   |                          | 34/37 | ns    |
| $t_{SOR}$  | Data Setup to OR HIGH      |                 | 0                  |      | 0        |      | 0        |      | 0                        |       | ns    |
| $t_{HSO}$  | Data Hold from SO LOW      |                 | 5                  |      | 5        |      | 5        |      | 5                        |       | ns    |
| $t_{BT}$   | Bubble through Time        |                 |                    | 200  | 10       | 95   | 10       | 65   | 10                       | 50/60 | ns    |
| $t_{SIR}$  | Data Setup to IR           | Note 9          | 5                  |      | 5        |      | 5        |      | 5                        |       | ns    |
| $t_{HIR}$  | Data Hold from IR          | Note 9          | 30                 |      | 30       |      | 30       |      | 20                       |       | ns    |
| $t_{PIR}$  | Input Ready Pulse HIGH     |                 | 20                 |      | 20       |      | 20       |      | 15                       |       | ns    |
| $t_{POR}$  | Output Ready Pulse HIGH    |                 | 20                 |      | 20       |      | 20       |      | 15                       |       | ns    |
| $t_{PMR}$  | MR Pulse Width             |                 | 40                 |      | 30       |      | 25       |      | 25                       |       | ns    |
| $t_{DSI}$  | MR HIGH to SI HIGH         |                 | 40                 |      | 35       |      | 25       |      | 10                       |       | ns    |
| $t_{DOR}$  | MR LOW to OR LOW           |                 |                    | 85   |          | 40   |          | 35   |                          | 35    | ns    |
| $t_{DIR}$  | MR LOW to IR HIGH          |                 |                    | 85   |          | 40   |          | 35   |                          | 35    | ns    |
| $t_{LZMR}$ | MR LOW to Output LOW       | Note 10         |                    | 50   |          | 40   |          | 35   |                          | 25    | ns    |
| $t_{OOE}$  | Output Valid from OE LOW   |                 |                    | —    |          | 35   |          | 30   |                          | 20    | ns    |
| $t_{HZOE}$ | Output HIGH-Z from OE HIGH | Note 11         |                    | —    |          | 30   |          | 25   |                          | 15    | ns    |

### Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance, as in Figure 1a.
- $I/f_O > t_{PHSI} + t_{DHIR}$ ,  $I/f_O > t_{PHSO} + t_{DHOR}$
- $t_{SSI}$  and  $t_{HSI}$  apply when memory is not full.
- $t_{SIR}$  and  $t_{HIR}$  apply when memory is full, SI is high and minimum bubble through ( $t_{BT}$ ) conditions exist.
- All data outputs will be at LOW level after reset goes high until data is entered into the FIFO.
- HIGH-Z transitions are referenced to the steady-state  $V_{OH} - 500\text{ mV}$  and  $V_{OL} + 500\text{ mV}$  levels on the output.  $t_{HZOE}$  is tested with 5 pF load capacitance as in Figure 1b.
- Commercial/Military

## Operational Description

### CONCEPT

Unlike traditional FIFOs these devices are designed using a dual port memory, read and write pointer, and control logic. The read and write pointers are incremented by the Shift Out (SO) and Shift In (SI) respectively. The availability of an empty space to shift in data is indicated by the Input Ready (IR) signal, while the presence of data at the output is indicated by the Output Ready (OR) signal. The conventional concept of bubble through is absent. Instead, the delay for input data to appear at the output is the time required to move a pointer and propagate an Output Ready (OR) signal. The Output Enable (OE) signal provides the capability to OR tie multiple FIFOs together on a common bus.

### RESETTING THE FIFO

Upon power up, the FIFO must be reset with a Master Reset (MR) signal. This causes the FIFO to enter an empty condition signified by the Output Ready (OR) signal being LOW at the same time the Input Ready (IR) signal is HIGH. In this condition, the data outputs  $DO_0$ – $DO_n$  will be in a LOW state.

### SHIFTING DATA IN

Data is shifted in on the rising edge of the Shift In (SI) signal. This loads input data into the first word location of the FIFO. On the falling edge of the Shift In (SI) signal, the write pointer is moved to the next word position and the Input Ready (IR) signal goes HIGH indicating the readiness to accept new data. If the FIFO is full, the Input Ready (IR) will remain LOW until a word of data is shifted out.

### SHIFTING DATA OUT

Data is shifted out of the FIFO on the falling edge of the Shift Out (SO) signal. This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and the Output Ready (OR) signal will go HIGH. If data is not present, the Output Ready (OR) signal will stay LOW indicating the FIFO is empty. Upon the rising edge of Shift Out (SO), the Output Ready (OR) signal goes LOW. The data outputs of the FIFO should be sampled with edge sensitive type D flip-flop (or equivalent), using the SO signal as the clock input to the flip-flop.

### BUBBLE THROUGH

Two bubble through conditions exist. The first is when the device is empty. After a word is shifted into an empty device, the data propagates to the output. After a delay, the Output Ready (OR) flag goes HIGH indicating valid data at the output.

The second bubble through condition occurs when the device is full. Shifting data out creates an empty location which propagates to the input. After a delay, the Input Ready (IR) flag goes HIGH. If the Shift In (SI) signal is HIGH at this time, data on the input will be shifted in.

### APPLICATION OF THE 7C403-25/7C404-25 AT 25 MHz

Application of the CY7C403 or CY7C404 Cypress CMOS FIFO's requires attention to characteristics not easily spec-

ified in a Datasheet, but necessary for reliable operation under all conditions.

When an empty FIFO is filled with initial information, at maximum "shift in" SI frequency, followed by immediate shifting out of the data also at maximum "shift out" SO frequency, the designer must be aware of a window of time which follows the initial rising edge of the "output Ready" OR signal during which the SO signal is not recognized. This condition exists only at high speed operation where more than one SO may be generated inside the prohibited window. This condition does not inhibit the operation of the FIFO at full frequency operation, but rather delays the full 25 MHz operation until after the window has passed.

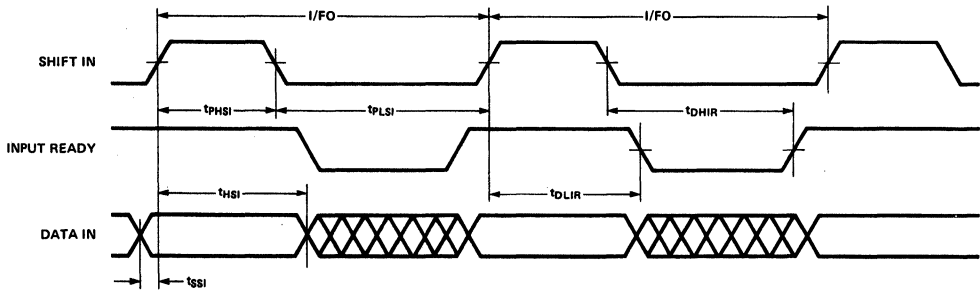
There are several implementation techniques to manage the window so that all SO signals are recognized:

1. The first involves delaying SO operation such that it does not occur in the critical window. This can be accomplished by causing a fixed delay of 40 ns "initiated by the SI signal only when the FIFO is empty" to inhibit or gate the SO activity. This however requires that the SO operation at least temporarily be synchronized with the input SI operation. In synchronous applications this may well be possible and a valid solution.
2. Another solution not uncommon in synchronous applications is to only begin shifting data out of the FIFO when it is greater than half full. This is a common method of FIFO application, as earlier FIFOs could not be operated at maximum frequency when near full or empty. Although Cypress FIFOs do not have this limitation, any system designed in this manner will not encounter the window condition described above.
3. The window may also be managed by not allowing the first SO signal to occur until the window in question has passed. This can be accomplished by delaying the SO 40 ns from the rising edge of the initial OR "output ready" signal. This however involves the requirement that this only occurs on the first occurrence of data being loaded into the FIFO from an empty condition and therefore requires the knowledge of "input ready" IR and SI conditions as well as SO.
4. Handshaking with the OR signal can be a third method of avoiding the window in question. With this technique the rising edge of SO, or the fact that the SO signal is HIGH, will cause the OR signal to go LOW. The SO signal is not taken low again, advancing the internal pointer to the next data, until the OR signal goes LOW. This assures that the SO pulse that is initiated in the window will be automatically extended sufficient time to be recognized.
5. There remains the decision as to what signal will be used to latch the data from the output of the FIFO into the receiving source. The leading edge of the SO signal is most appropriate because data is guaranteed to be stable prior to and after the SO leading edge for each FIFO. This is a solution for any number of FIFOs in parallel.

Any of the above solutions will provide a solution for correct operation of a Cypress FIFO at 25 MHz. The specific implementation is left to the designer and dependent on the specific application needs.

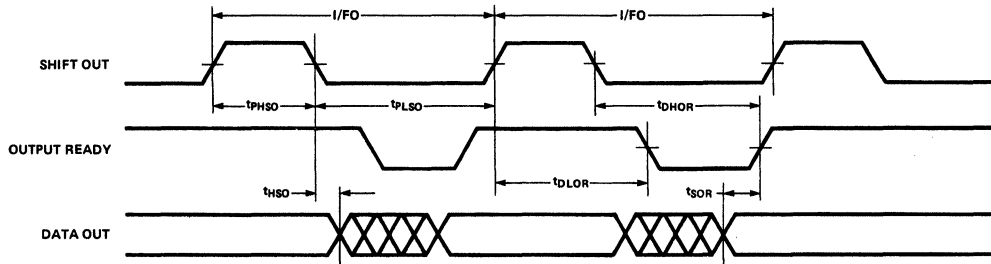
## Switching Waveforms

### Data In Timing Diagram



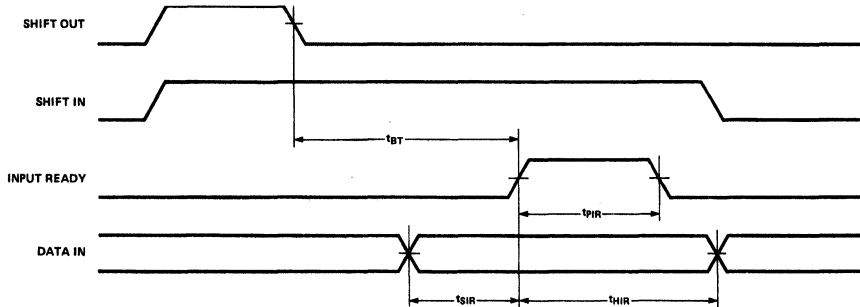
0014-7

### Data Out Timing Diagram



0014-8

### Bubble Through, Data Out To Data In Diagram

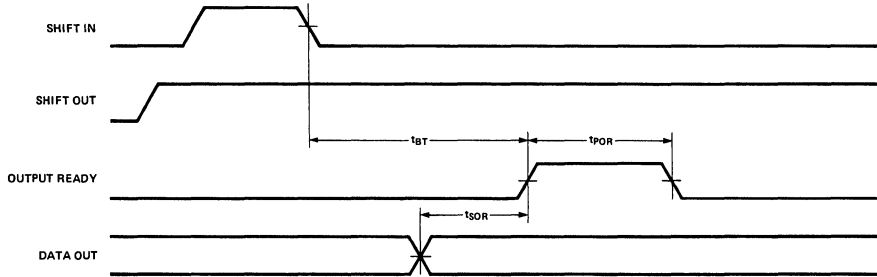


0014-9

**Note:**  
Interfacing to the FIFO—  
Please refer to the Interfacing to the FIFO applications brief in the Applications Section at the back of this data book.

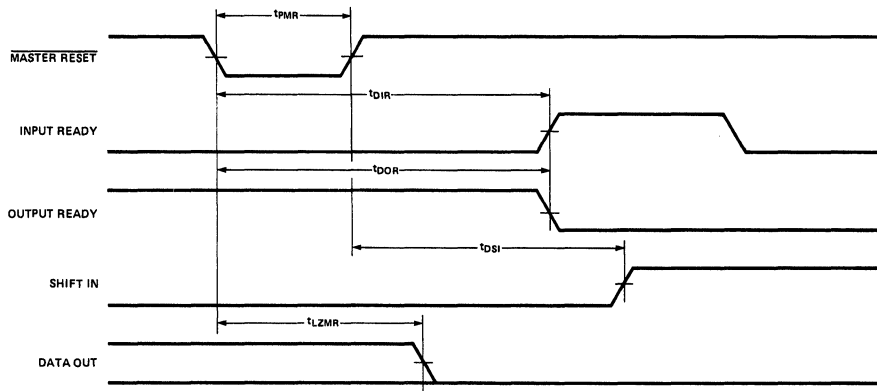
### Switching Waveforms (Continued)

#### Bubble Through, Data In To Data Out Diagram



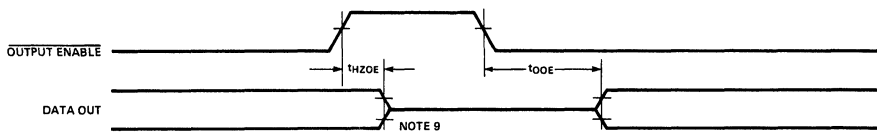
0014-10

#### Master Reset Timing Diagram



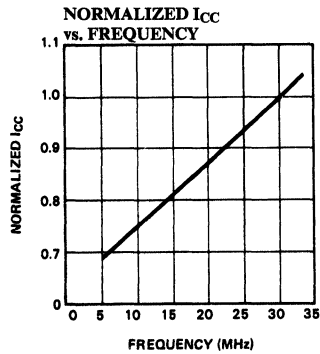
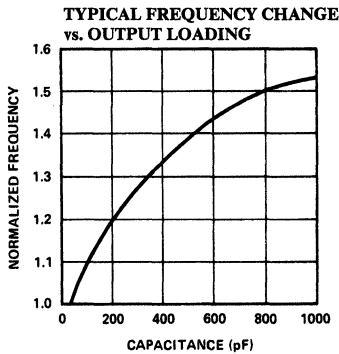
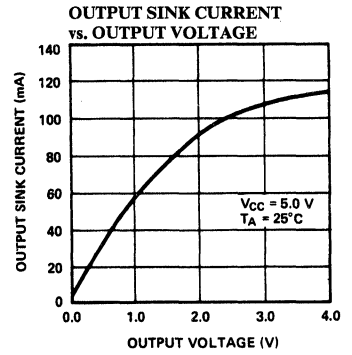
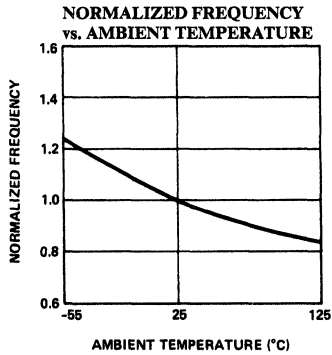
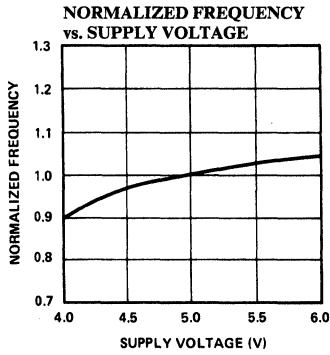
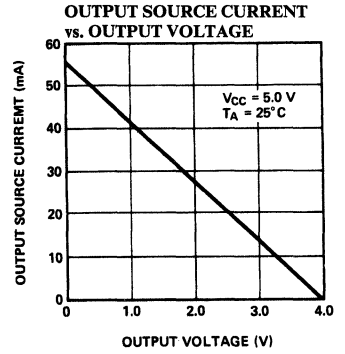
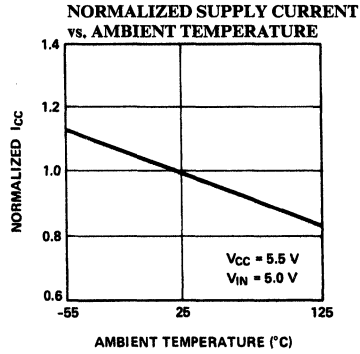
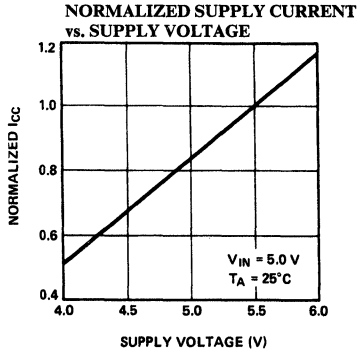
0014-11

#### Output Enable Timing Diagram



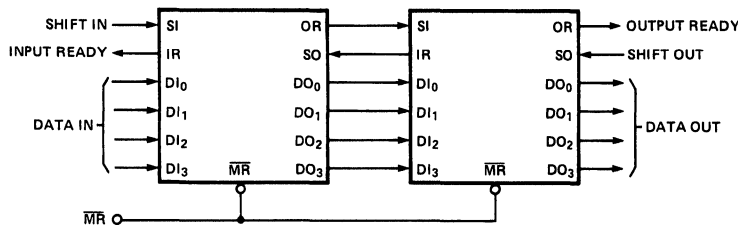
0014-12

## Typical DC and AC Characteristics



## FIFO Expansion

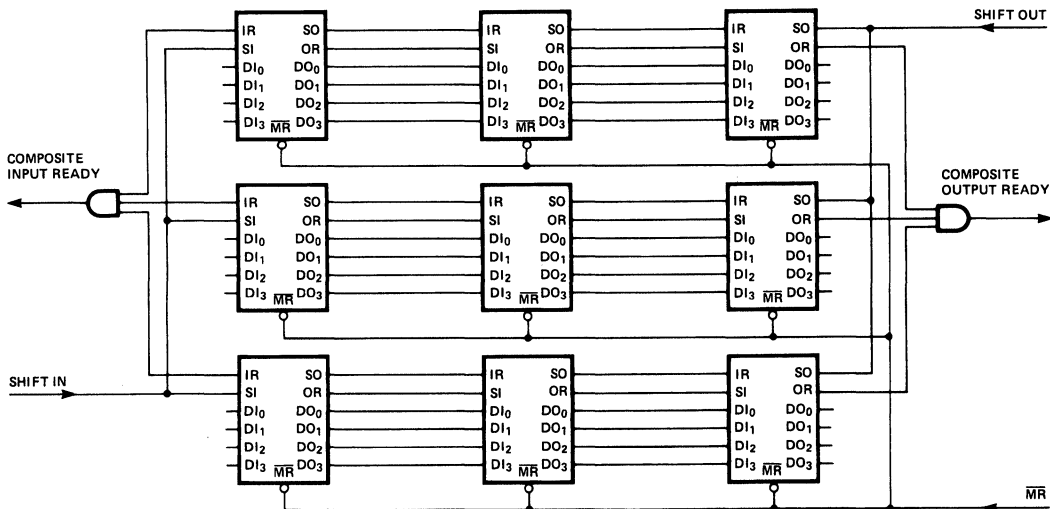
### 128 x 4 Application



0014-14

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

### 192 x 12 Application



0014-15

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the variation of delays of the FIFOs.

#### User Notes:

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word bubbles through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the memory to the output. OR will go HIGH for one internal cycle (at least  $t_{ORL}$ ) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, then IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.
5. All Cypress FIFOs will cascade with other Cypress FIFOs. However, they may not cascade with pin-compatible FIFO's from other manufacturers.

**Ordering Information**

| Ordering Code<br>(25 MHz) | Package<br>Type | Operating<br>Range |      |
|---------------------------|-----------------|--------------------|------|
| CY7C401-25PC              | P1              | Com.               |      |
| CY7C402-25PC              | P3              |                    |      |
| CY7C403-25PC              | P1              |                    |      |
| CY7C404-25PC              | P3              |                    |      |
| CY7C401-25DC              | D2              |                    |      |
| CY7C402-25DC              | D4              |                    |      |
| CY7C403-25DC              | D2              |                    |      |
| CY7C404-25DC              | D4              |                    |      |
| CY7C401-25LC              | L61             |                    |      |
| CY7C402-25LC              | L61             |                    |      |
| CY7C403-25LC              | L61             |                    |      |
| CY7C404-25LC              | L61             |                    |      |
| CY7C401-25DMB             | D2              |                    | Mil. |
| CY7C402-25DMB             | D4              |                    |      |
| CY7C403-25DMB             | D2              |                    |      |
| CY7C404-25DMB             | D4              |                    |      |
| CY7C401-25LMB             | L61             |                    |      |
| CY7C402-25LMB             | L61             |                    |      |
| CY7C403-25LMB             | L61             |                    |      |
| CY7C404-25LMB             | L61             |                    |      |

| Ordering Code<br>(15 MHz) | Package<br>Type | Operating<br>Range |      |
|---------------------------|-----------------|--------------------|------|
| CY7C401-15PC              | P1              | Com.               |      |
| CY7C402-15PC              | P3              |                    |      |
| CY7C403-15PC              | P1              |                    |      |
| CY7C404-15PC              | P3              |                    |      |
| CY7C401-15DC              | D2              |                    |      |
| CY7C402-15DC              | D4              |                    |      |
| CY7C403-15DC              | D2              |                    |      |
| CY7C404-15DC              | D4              |                    |      |
| CY7C401-15LC              | L61             |                    |      |
| CY7C402-15LC              | L61             |                    |      |
| CY7C403-15LC              | L61             |                    |      |
| CY7C404-15LC              | L61             |                    |      |
| CY7C401-15DMB             | D2              |                    | Mil. |
| CY7C402-15DMB             | D4              |                    |      |
| CY7C403-15DMB             | D2              |                    |      |
| CY7C404-15DMB             | D4              |                    |      |
| CY7C401-15LMB             | L61             |                    |      |
| CY7C402-15LMB             | L61             |                    |      |
| CY7C403-15LMB             | L61             |                    |      |
| CY7C404-15LMB             | L61             |                    |      |

| Ordering Code<br>(10 MHz) | Package<br>Type | Operating<br>Range |      |
|---------------------------|-----------------|--------------------|------|
| CY7C401-10PC              | P1              | Com.               |      |
| CY7C402-10PC              | P3              |                    |      |
| CY7C403-10PC              | P1              |                    |      |
| CY7C404-10PC              | P3              |                    |      |
| CY7C401-10DC              | D2              |                    |      |
| CY7C402-10DC              | D4              |                    |      |
| CY7C403-10DC              | D2              |                    |      |
| CY7C404-10DC              | D4              |                    |      |
| CY7C401-10LC              | L61             |                    |      |
| CY7C402-10LC              | L61             |                    |      |
| CY7C403-10LC              | L61             |                    |      |
| CY7C404-10LC              | L61             |                    |      |
| CY7C401-10DMB             | D2              |                    | Mil. |
| CY7C402-10DMB             | D4              |                    |      |
| CY7C403-10DMB             | D2              |                    |      |
| CY7C404-10DMB             | D4              |                    |      |
| CY7C401-10LMB             | L61             |                    |      |
| CY7C402-10LMB             | L61             |                    |      |
| CY7C403-10LMB             | L61             |                    |      |
| CY7C404-10LMB             | L61             |                    |      |

| Ordering Code<br>(5 MHz) | Package<br>Type | Operating<br>Range |
|--------------------------|-----------------|--------------------|
| CY7C401-5PC              | P1              | Com.               |
| CY7C402-5PC              | P3              |                    |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>Ix</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>OS</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |

**Switching Characteristics**

| Parameters        | Subgroups   |
|-------------------|-------------|
| f <sub>O</sub>    | 7,8,9,10,11 |
| t <sub>PHSI</sub> | 7,8,9,10,11 |
| t <sub>PLSI</sub> | 7,8,9,10,11 |
| t <sub>SSI</sub>  | 7,8,9,10,11 |
| t <sub>HSI</sub>  | 7,8,9,10,11 |
| t <sub>DLIR</sub> | 7,8,9,10,11 |
| t <sub>DHIR</sub> | 7,8,9,10,11 |
| t <sub>PHSO</sub> | 7,8,9,10,11 |
| t <sub>PLSO</sub> | 7,8,9,10,11 |
| t <sub>DLOR</sub> | 7,8,9,10,11 |
| t <sub>DHOR</sub> | 7,8,9,10,11 |
| t <sub>SOR</sub>  | 7,8,9,10,11 |
| t <sub>HSO</sub>  | 7,8,9,10,11 |
| t <sub>BT</sub>   | 7,8,9,10,11 |
| t <sub>SIR</sub>  | 7,8,9,10,11 |
| t <sub>HIR</sub>  | 7,8,9,10,11 |
| t <sub>PIR</sub>  | 7,8,9,10,11 |
| t <sub>POR</sub>  | 7,8,9,10,11 |
| t <sub>PMR</sub>  | 7,8,9,10,11 |
| t <sub>DSI</sub>  | 7,8,9,10,11 |
| t <sub>DOR</sub>  | 7,8,9,10,11 |
| t <sub>DIR</sub>  | 7,8,9,10,11 |
| t <sub>LZMR</sub> | 7,8,9,10,11 |

| Parameters        | Subgroups   |
|-------------------|-------------|
| t <sub>OOE</sub>  | 7,8,9,10,11 |
| t <sub>HZOE</sub> | 7,8,9,10,11 |





Cascadeable 64 x 8 FIFO  
Cascadeable 64 x 9 FIFO

Features

- 64 x 8 and 64 x 9 first-in first-out (FIFO) buffer memory
- 35 MHz shift-in and shift-out rates
- Almost Full/Almost Empty and Half Full flags
- Dual port RAM architecture
- Fast, 50 ns, bubblethrough
- Independent asynchronous inputs and outputs
- Output Enable (CY7C408A)
- Expandable in word width and FIFO depth
- 5V ±10% supply
- TTL compatible
- Capable of withstanding greater than 2000V electrostatic discharge voltage
- 300 mil, 28-pin DIP

Functional Description

The CY7C408A and CY7C409A are 64-word deep by 8- or 9-bit wide first-in first-out (FIFO) buffer memories. In addition to the industry standard handshaking signals, Almost Full/Almost Empty (AFE) and Half Full (HF) flags are provided.

AFE is HIGH when the FIFO is almost full or almost empty, otherwise AFE is LOW. HF is HIGH when the FIFO is half full, otherwise HF is LOW.

The CY7C408A has an Output Enable (OE) function.

The memory accepts 8- or 9-bit parallel words at its inputs (DI<sub>0</sub>-DI<sub>8</sub>) under the control of the Shift-In (SI) input when the Input-Ready (IR) control signal is HIGH. The data is output, in the same order as it was stored, on the DO<sub>0</sub>-DO<sub>8</sub> output pins under the control of the Shift-Out (SO) input when the Output-Ready (OR) control signal is HIGH. If the FIFO is full (IR LOW), pulses at the SI input are ignored; if the FIFO is empty (OR LOW), pulses at the SO input are ignored.

The IR and OR signals are also used to connect the FIFO's in parallel to make a wider word, or in series to make a deeper buffer, or both.

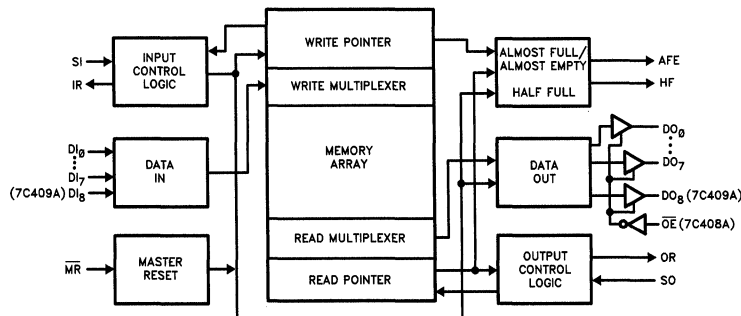
Parallel expansion for wider words is implemented by logically ANDing the IR and OR outputs (respectively) of the individual FIFOs together (Figure 7). The AND operation insures that all of the FIFOs are either ready to accept

more data (IR HIGH) or are ready to output data (OR HIGH) and thus compensate for variations in propagation delay times between devices.

Serial expansion (cascading) for deeper buffer memories is accomplished by connecting the data outputs of the FIFO closest to the data source (upstream device) to the data inputs of the following (downstream) FIFO (Figure 6). In addition, to insure proper operation, the SO signal of the upstream FIFO must be connected to the IR output of the downstream FIFO and the SI signal of the downstream FIFO must be connected to the OR output of the upstream FIFO. In this serial expansion configuration, the IR and OR signals are used to pass data through the FIFOs.

Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely differing operating frequencies. The high shift-in and shift-out rates of these FIFOs, and their high throughput rate due to the fast bubblethrough time, which is due to their dual port RAM architecture, make them ideal for high speed communications and controllers.

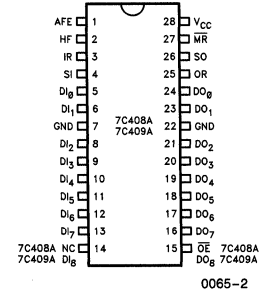
Logic Block Diagram



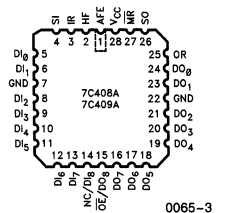
Flag Definitions

| HF | AFE | Words Stored |
|----|-----|--------------|
| L  | H   | 0-8          |
| L  | L   | 9-31         |
| H  | L   | 32-55        |
| H  | H   | 56-64        |

Pin Configurations



0065-1



0065-3

## Selection Guide

|   |            | 7C408A-15<br>7C409A-15 | 7C408A-25<br>7C409A-25 | 7C408A-35<br>7C409A-35 |
|---|------------|------------------------|------------------------|------------------------|
| Maximum Shift Rate (MHz)                      |            | 15                     | 25                     | 35                     |
| Maximum Operating Current (mA) <sup>[2]</sup> | Commercial | 115                    | 125                    | 135                    |
|   | Military   | 140                    | 150                    | N/A                    |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied ..... -55°C to +125°C  
 Supply Voltage to Ground Potential .... -0.5V to +7.0V  
 DC Voltage Applied to Outputs  
 in High Z State (7C408A) ..... -0.5V to +7.0V  
 DC Input Voltage ..... -3.0V to +7.0V  
 Power Dissipation ..... 1.0W  
 Output Current, into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... > 2001V  
 (per MIL-STD-883 Method 3015)

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[4]</sup> | -55°C to +125°C     | 5V ± 10%        |

5

## Electrical Characteristics Over Operating Range (Unless Otherwise Noted)<sup>[5]</sup>

| Parameters       | Description                                 | Test Conditions  | CY7C408A<br>CY7C409A |                 | Units |
|------------------|---|--|----------------------|-----------------|-------|
|                  |   |  | Min.                 | Max.            |       |
| V <sub>OH</sub>  | Output HIGH Voltage                         | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA  | 2.4                  |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                          | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA   |                      | 0.4             | V     |
| V <sub>IH</sub>  | Input HIGH Voltage                          |  | 2.2                  | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input LOW Voltage                           |  | -3.0                 | 0.8             | V     |
| I <sub>IX</sub>  | Input Leakage Current                       | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>   | -10                  | +10             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup> | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND   |                      | -90             | mA    |
| I <sub>CCQ</sub> | Quiescent Power Supply Current              | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA<br>V <sub>IN</sub> ≤ V <sub>IL</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> | Commercial           | 100             | mA    |
|                  |   |  | Military             | 125             | mA    |
| I <sub>CC</sub>  | Power Supply Current                        | I <sub>CC</sub> = I <sub>CCQ</sub> + 1 mA/MHz × (f <sub>SI</sub> + f <sub>SO</sub> )/2                                   |                      |                 |       |

## Capacitance<sup>[3]</sup>

| Parameters       | Description        | Test Conditions                  | Max. | Units |
|------------------|--------------------|----------------------------------|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance | V <sub>CC</sub> = 4.5V           | 7    |       |

### Notes:

- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- I<sub>CC</sub> = I<sub>CCQ</sub> + 1 mA/MHz × (f<sub>SI</sub> + f<sub>SO</sub>)/2

- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

## AC Test Load and Waveforms

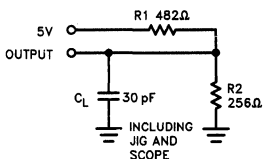


Figure 1a

0065-4

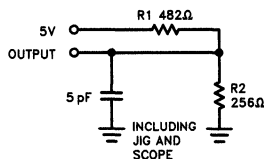


Figure 1b

0065-21

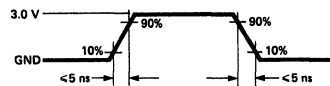


Figure 2. All Input Pulses

0065-5

Equivalent to: THÉVENIN EQUIVALENT



0065-6

**Switching Characteristics Over the Operating Range<sup>[5, 6]</sup>**

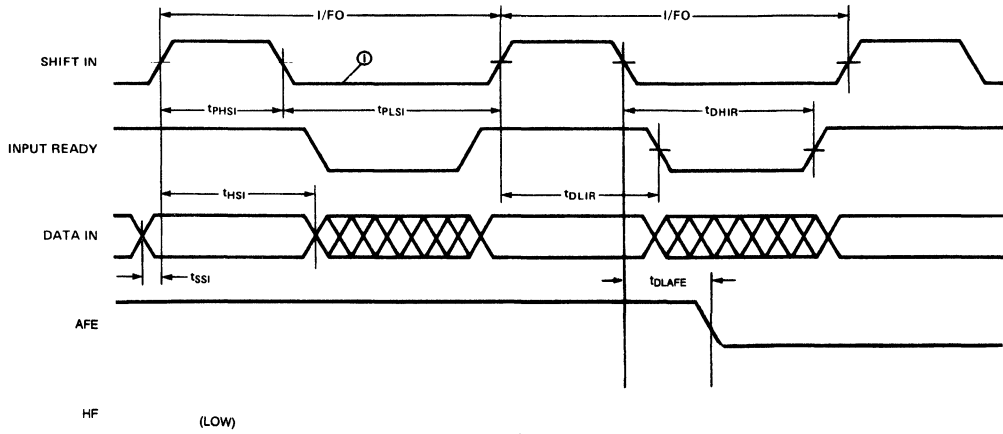
| Parameters         | Description                  | Test Conditions | CY7C408A-15<br>CY7C409A-15 |      | CY7C408A-25<br>CY7C409A-25 |      | CY7C408A-35<br>CY7C409A-35 |      | Units |
|--------------------|------------------------------|-----------------|----------------------------|------|----------------------------|------|----------------------------|------|-------|
|                    |                              |                 | Min.                       | Max. | Min.                       | Max. | Min.                       | Max. |       |
| f <sub>o</sub>     | Operating Frequency          | Note 7          |                            | 15   |                            | 25   |                            | 35   | MHz   |
| t <sub>PHSI</sub>  | SI HIGH Time                 | Note 7          | 23                         |      | 11                         |      | 9                          |      | ns    |
| t <sub>PLSI</sub>  | SI LOW Time                  | Note 7          | 25                         |      | 24                         |      | 17                         |      | ns    |
| t <sub>SSI</sub>   | Data Setup to SI             | Note 8          | 0                          |      | 0                          |      | 0                          |      | ns    |
| t <sub>HSI</sub>   | Data Hold from SI            | Note 8          | 30                         |      | 20                         |      | 12                         |      | ns    |
| t <sub>DLIR</sub>  | Delay, SI HIGH to IR LOW     |                 |                            | 35   |                            | 21   |                            | 15   | ns    |
| t <sub>DHIR</sub>  | Delay, SI LOW to IR HIGH     |                 |                            | 40   |                            | 23   |                            | 16   | ns    |
| t <sub>PHSO</sub>  | SO HIGH Time                 | Note 7          | 23                         |      | 11                         |      | 9                          |      | ns    |
| t <sub>PLSO</sub>  | SO LOW Time                  | Note 7          | 25                         |      | 24                         |      | 17                         |      | ns    |
| t <sub>DLOR</sub>  | Delay, SO HIGH to OR LOW     |                 |                            | 35   |                            | 21   |                            | 15   | ns    |
| t <sub>DHOR</sub>  | Delay, SO LOW to OR HIGH     |                 |                            | 40   |                            | 23   |                            | 16   | ns    |
| t <sub>SOR</sub>   | Data Setup to OR HIGH        |                 | 0                          |      | 0                          |      | 0                          |      | ns    |
| t <sub>HSO</sub>   | Data Hold from SO LOW        |                 | 0                          |      | 0                          |      | 0                          |      | ns    |
| t <sub>BT</sub>    | Fallthrough, Bubbleback Time |                 | 10                         | 65   | 10                         | 60   | 10                         | 50   | ns    |
| t <sub>SIR</sub>   | Data Setup to IR             | Note 9          | 5                          |      | 5                          |      | 5                          |      | ns    |
| t <sub>HIR</sub>   | Data Hold from IR            | Note 9          | 30                         |      | 20                         |      | 20                         |      | ns    |
| t <sub>PIR</sub>   | Input Ready Pulse HIGH       | Note 10         | 6                          |      | 6                          |      | 6                          |      | ns    |
| t <sub>POR</sub>   | Output Ready Pulse HIGH      | Note 11         | 6                          |      | 6                          |      | 6                          |      | ns    |
| t <sub>DLZOE</sub> | OE LOW to LOW Z (7C408)      | Note 12         |                            | 35   |                            | 30   |                            | 25   | ns    |
| t <sub>DHZOE</sub> | OE HIGH to HIGH Z (7C408)    | Note 12         |                            | 35   |                            | 30   |                            | 25   | ns    |
| t <sub>DHHF</sub>  | SI LOW to HF HIGH            |                 |                            | 65   |                            | 55   |                            | 45   | ns    |
| t <sub>DLHF</sub>  | SO LOW to HF LOW             |                 |                            | 65   |                            | 55   |                            | 45   | ns    |
| t <sub>DLAFE</sub> | SO or SI LOW to AFE LOW      |                 |                            | 65   |                            | 55   |                            | 45   | ns    |
| t <sub>DHAFE</sub> | SO or SI LOW to AFE HIGH     |                 |                            | 65   |                            | 55   |                            | 45   | ns    |
| t <sub>PMR</sub>   | MR Pulse Width               |                 | 55                         |      | 45                         |      | 35                         |      | ns    |
| t <sub>DSI</sub>   | MR HIGH to SI HIGH           |                 | 25                         |      | 10                         |      | 10                         |      | ns    |
| t <sub>DOR</sub>   | MR LOW to OR LOW             |                 |                            | 55   |                            | 45   |                            | 35   | ns    |
| t <sub>DIR</sub>   | MR LOW to IR HIGH            |                 |                            | 55   |                            | 45   |                            | 35   | ns    |
| t <sub>LZMR</sub>  | MR LOW to Output LOW         | Note 13         |                            | 55   |                            | 45   |                            | 35   | ns    |
| t <sub>AFE</sub>   | MR LOW to AFE HIGH           |                 |                            | 55   |                            | 45   |                            | 35   | ns    |
| t <sub>HF</sub>    | MR LOW to HF LOW             |                 |                            | 55   |                            | 45   |                            | 35   | ns    |

**Notes:**

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance, as in *Figure 1*.
- 1/f<sub>o</sub> ≥ (t<sub>PHSI</sub> + t<sub>PLSI</sub>), 1/f<sub>o</sub> ≥ (t<sub>PHSO</sub> + t<sub>PLSO</sub>).
- t<sub>SSI</sub> and t<sub>HSI</sub> apply when memory is not full.
- t<sub>SIR</sub> and t<sub>HIR</sub> apply when memory is full, SI is HIGH and minimum bubblethrough (t<sub>BT</sub>) conditions exist.
- At any given operating condition t<sub>PIR</sub> ≥ (t<sub>PHSO</sub> required).
- At any given operating condition t<sub>POR</sub> ≥ (t<sub>PHSI</sub> required).
- t<sub>DHZOE</sub> and t<sub>DLZOE</sub> are specified with C<sub>L</sub> = 5 pF as in *Figure 1b*. t<sub>DHZOE</sub> transition is measured ± 500 mV from steady state voltage. t<sub>DLZOE</sub> transition is measured ± 100 mV from steady state voltage. These parameters are guaranteed and not 100% tested.
- All data outputs will be at LOW level after reset goes HIGH until data is entered into the FIFO.

## Switching Waveforms

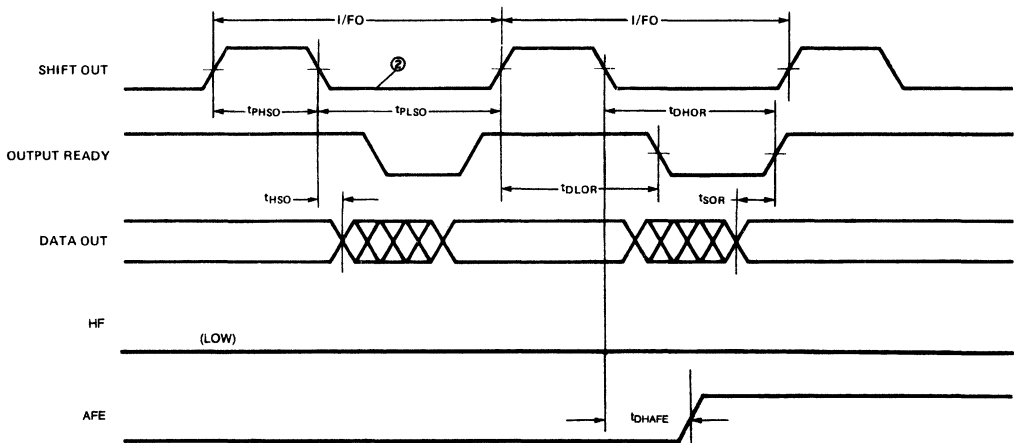
### Data In Timing Diagram



① FIFO Contains 8 Words

0065-7

### Data Out Timing Diagram



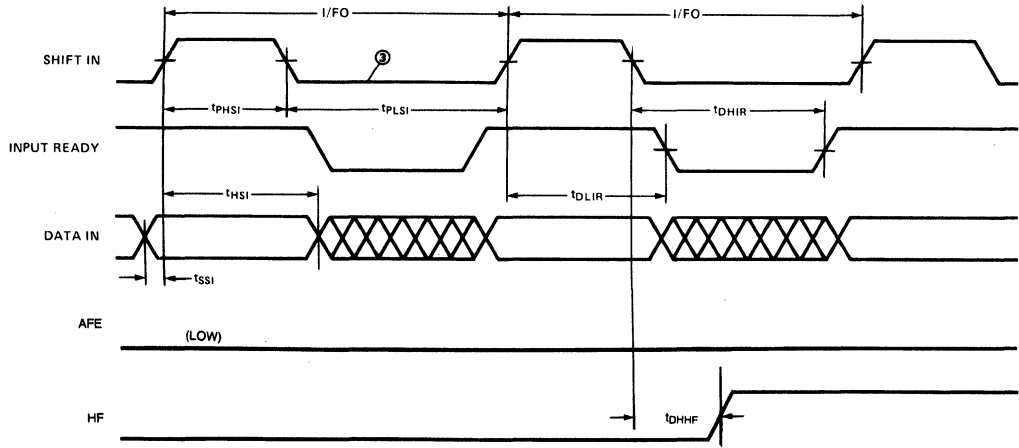
② FIFO Contains 9 Words

0065-8

5

## Switching Waveforms (Continued)

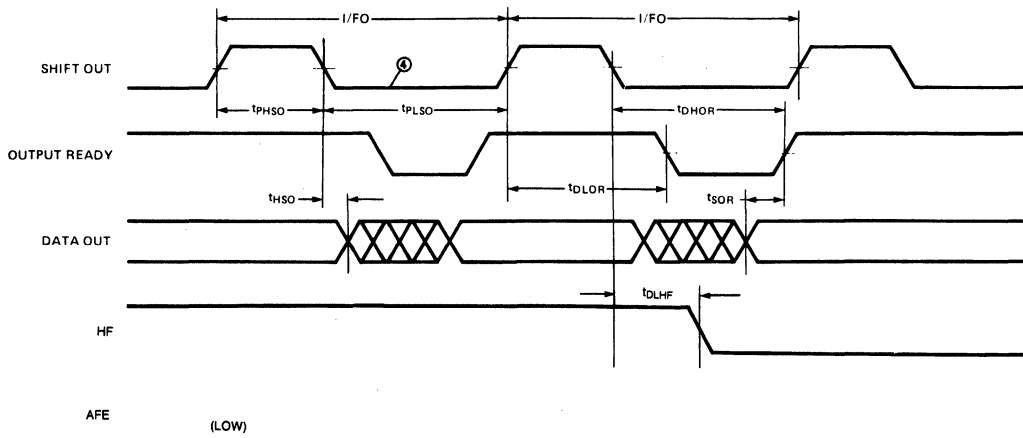
### Data In Timing Diagram



③ FIFO Contains 31 Words

0065-14

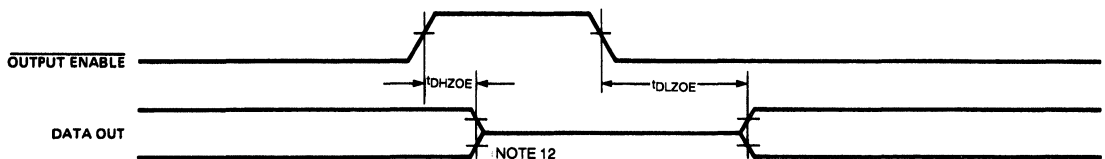
### Data Out Timing Diagram



④ FIFO Contains 32 Words

0065-15

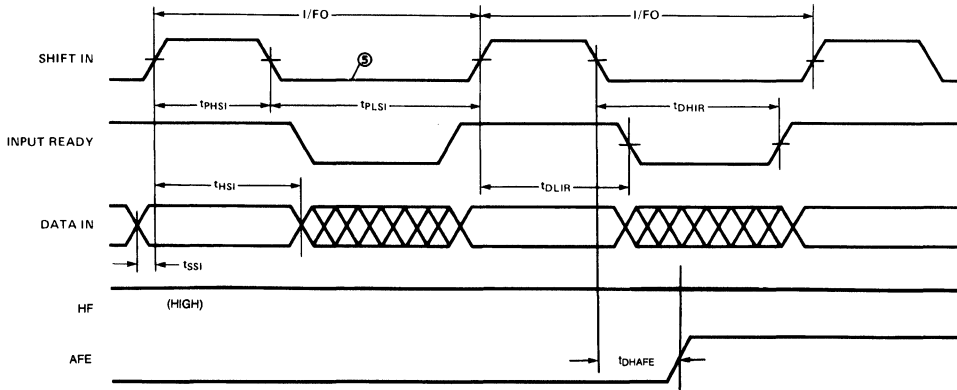
### Output Enable (CY7C408A only)



0065-20

## Switching Waveforms (Continued)

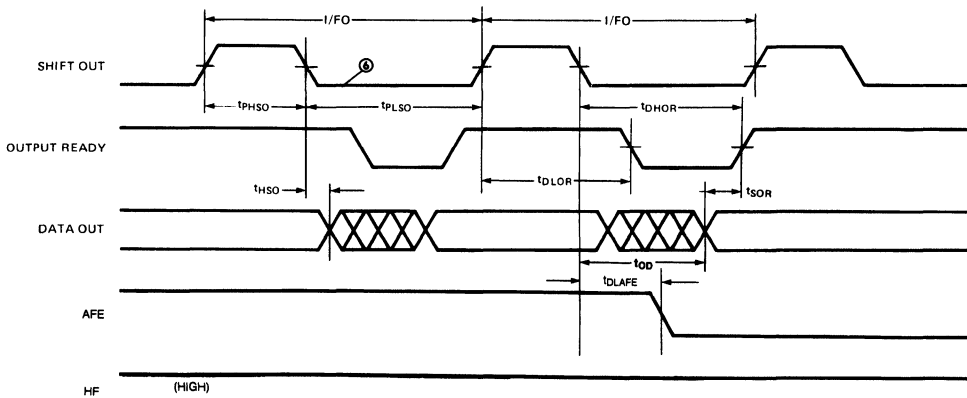
### Data In Timing Diagram



© FIFO Contains 55 Words

0065-16

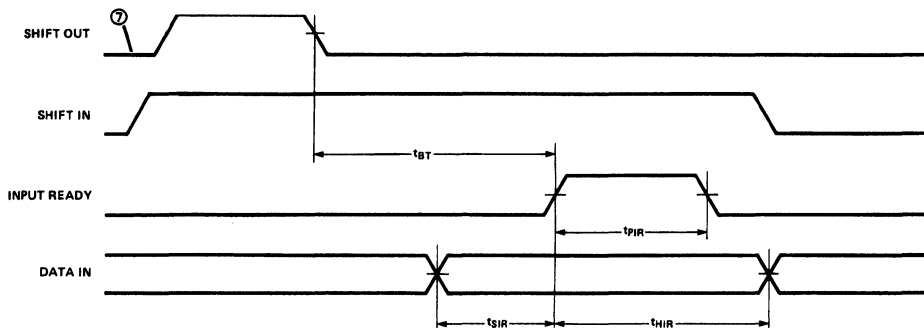
### Data Out Timing Diagram



© FIFO Contains 56 Words

0065-17

### Bubbleback, Data Out to Data In Diagram

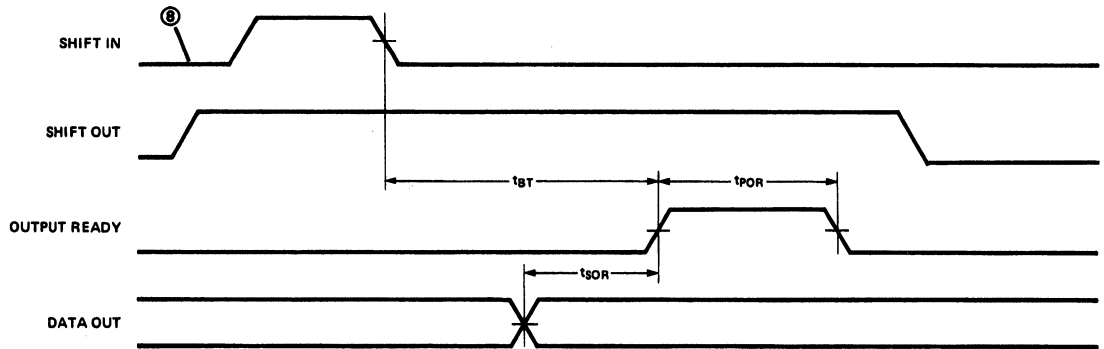


© FIFO Contains 64 Words

0065-9

## Switching Waveforms (Continued)

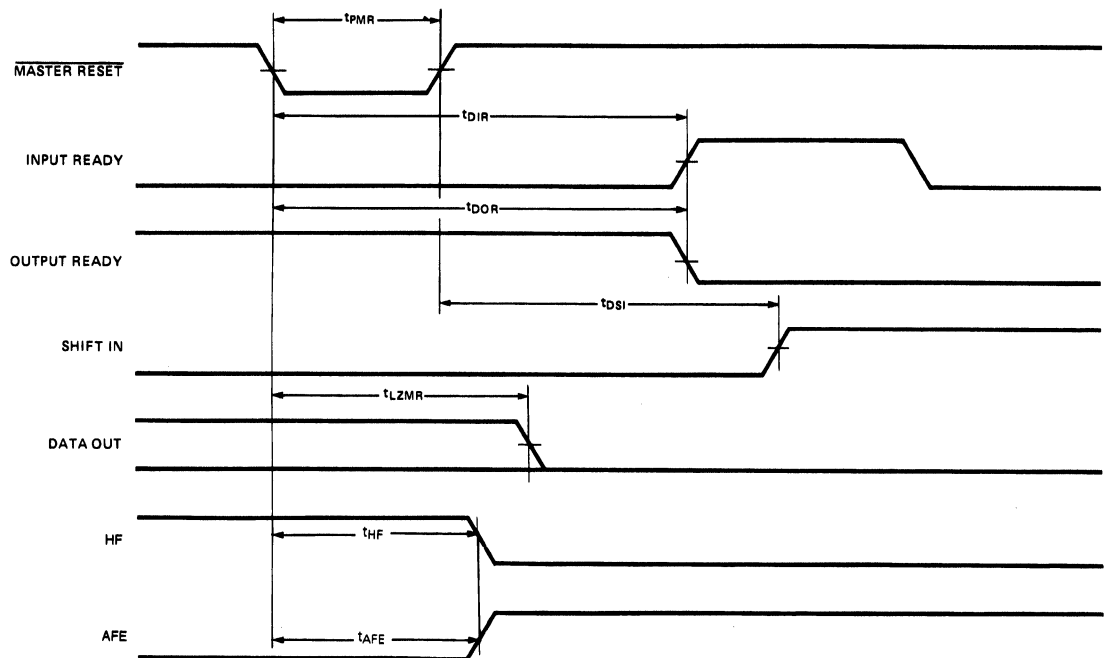
### Fallthrough, Data In to Data Out Diagram



0065-10

© FIFO Is Empty

### Master Reset Timing Diagram



0065-11

## Shifting Words In

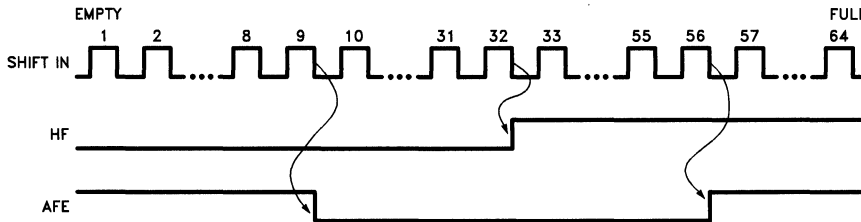


Figure 3

0065-18

## Shifting Words Out

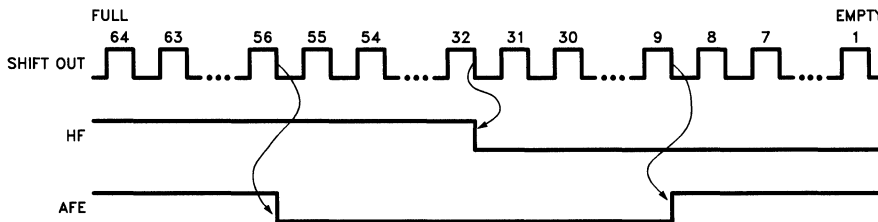


Figure 4

0065-19

5

## Architecture of the CY7C408A and CY7C409A

The CY7C408A and CY7C409A FIFOs consist of an array of 64 words of 8- or 9-bits each (which are implemented using a dual port RAM cell), a write pointer, a read pointer and the control logic necessary to generate the handshaking (SI/IR, SO/OR) signals as well as the Almost Full/Almost Empty (AFE) and the Half Full (HF) flags. The handshaking signals operate in a manner identical to those of the industry standard CY7C401/402/403/404 FIFOs.

### Dual Port RAM

The dual port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data to propagate through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

### Fallthrough and Bubbleback

The time required for data to propagate from the input to the output of an initially empty FIFO is defined as the Fallthrough time.

The time required for an empty location to propagate from the output to the input of an initially full FIFO is defined as the Bubbleback time.

The maximum rate at which data can be passed through the FIFO (called the throughput) is limited by the fall-

through time when it is empty (or near empty) and by the bubbleback time when it is full (or near full).

The conventional definitions of fallthrough and bubbleback do not apply to the CY7C408A and CY7C409A FIFOs because the data is not physically propagated through the memory. The read and write pointers are incremented instead of moving the data. However, the parameter is specified because it does represent the worst case propagation delay for the control signals. That is, the time required to increment the write pointer and propagate a signal from the SI input to the OR output of an empty FIFO or the time required to increment the read pointer and propagate a signal from the SO input to the IR output of a full FIFO.

### Resetting the FIFO

Upon power up, the FIFO must be reset with a Master Reset (MR) signal. This causes the device to enter the empty condition, which is signified by the OR signal being LOW at the same time that the IR signal is HIGH. In this condition, the data outputs (DO<sub>0</sub>-DO<sub>8</sub>) will be LOW. The AFE flag will be HIGH and the HF flag will be LOW.

### Shifting Data Into the FIFO

The availability of an empty location is indicated by the HIGH state of the Input Ready (IR) signal. When IR is HIGH a LOW to HIGH transition on the Shift-In (SI) pin will load the data on the DI<sub>0</sub>-DI<sub>8</sub> inputs into the FIFO.

The IR output will then go LOW, indicating that the data has been sampled. The HIGH to LOW transition of the SI signal initiates the LOW to HIGH transition of the IR signal if the FIFO is not full. If the FIFO is full, IR will remain LOW.



## Shifting Data Out of the FIFO

The availability of data at the outputs of the FIFO is indicated by the HIGH state of the Output Ready (OR) signal. After the FIFO is reset all data outputs (DO<sub>0</sub>–DO<sub>8</sub>) will be in the LOW state. As long as the FIFO remains empty the OR signal will be LOW and all Shift Out (SO) pulses applied to it will be ignored. After data is shifted into the FIFO the OR signal will go HIGH. The external control logic (designed by the user) should use the HIGH state of the OR signal to generate a SO pulse. The data outputs of the FIFO should be sampled with edge sensitive type D flip-flops (or equivalent), using the SO signal as the clock input to the flip-flop.

### Interfacing to the FIFO Application Brief

See the application brief in the back of this databook for information regarding interfacing to the FIFO under asynchronous operating conditions.

### AFE and HF Flags

Two flags, Almost Full/Almost Empty (AFE) and Half Full (HF), describe how many words are stored in the FIFO. AFE is HIGH when there are eight or less, or 56 or more, words stored in the FIFO. Otherwise the AFE flag is LOW. HF is HIGH when there are 32 or more words stored in the FIFO, otherwise the HF flag is LOW. Flag transitions occur relative to the falling edges of SI and SO (Figures 3 and 4).

Due to the asynchronous nature of the SI and SO signals, it is possible to encounter specific timing relationships which may cause short pulses on the AFE and HF flags. These pulses are entirely due to the dynamic relationship of the SI and SO signals. The flags, however, will always settle to their correct state after the appropriate delay ( $t_{DHAFE}$ ,  $t_{DLAFE}$ ,  $t_{DHHF}$  or  $t_{DLHF}$ ). Therefore, use of level-sensitive rather than edge-sensitive flag detection devices is recommended to avoid false flag encoding.

### Cascading the 7C408/9A-35 Above 25 MHz

If cascaded FIFOs are to be operated with an external clock rate greater than 25 MHz, the interface IR signal

must be inverted before being fed back to the interface SO pin (Figure 5). Two things should be noted when this configuration is implemented.

First, the capacity of N cascaded FIFOs is decreased from  $N \times 64$  to  $(N \times 63) + 1$ .

Secondly, the frequency at the cascade interface is less than the 35 MHz rate at which the external clocks may operate. Therefore, the first device has its data Shifted-In faster than it is Shifted-Out and eventually this device becomes momentarily full. When this occurs, the maximum sustainable external clock frequency changes from 35 MHz to the cascade interface frequency.<sup>[14]</sup>

When data packets<sup>[15]</sup> are transmitted, this phenomenon does not occur unless more than three FIFOs are depth cascaded. For example, if two FIFOs are cascaded, a packet of 127 ( $= 2 \times 63 + 1$ ) words may be shifted-in at up to 35 MHz and then the entire packet may be shifted-out at up to 35 MHz.

If data is to be shifted-out simultaneously with the data being shifted-in, the concept of “virtual capacity” is introduced. Virtual capacity is simply how large a packet of data can be shifted-in at a fixed frequency, e.g., 35 MHz, simultaneously with data being shifted-out at any given frequency. Figure 8 is a graph of packet size<sup>[16]</sup> vs. shift-out frequency ( $f_{SOX}$ ) for two different values of Shift-In frequency ( $f_{SIX}$ ) when two FIFOs are cascaded.

The exact complement of this occurs if the FIFOs initially contain data and a high Shift-Out frequency is to be maintained, i.e., a 35 MHz  $f_{SOX}$  can be sustained when reading data packets from devices cascaded two or three deep. If data is shifted-in simultaneously, Figure 8 applies with  $f_{SIX}$  and  $f_{SOX}$  interchanged.

#### Notes:

14. Because the data throughput in the cascade interface is dependent on the inverter delay, it is recommended that the fastest available inverter be used.
15. Transmission of data packets assumes that up to the maximum cumulative capacity of the FIFOs is Shifted-In without simultaneous Shift-Out clocks occurring. The complement of this holds when data is Shifted-Out as a packet.
16. These are typical packet sizes using an inverter whose delay is 4 ns.
17. Only devices with the same speed grade are specified to cascade together.

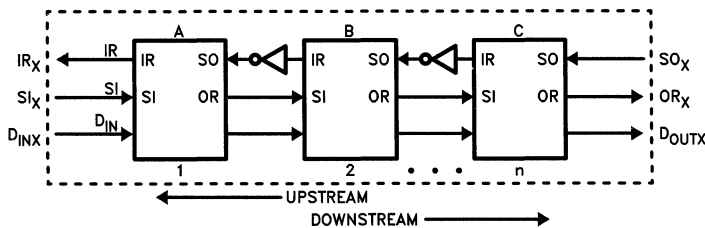
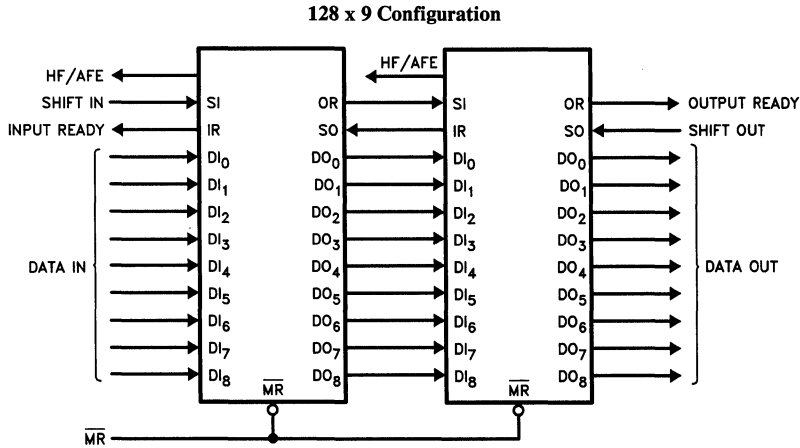


Figure 5. Cascaded Configuration Above 25 MHz

0065-22

## FIFO Expansion



**Figure 6. Cascaded Configuration at or below 25 MHz**

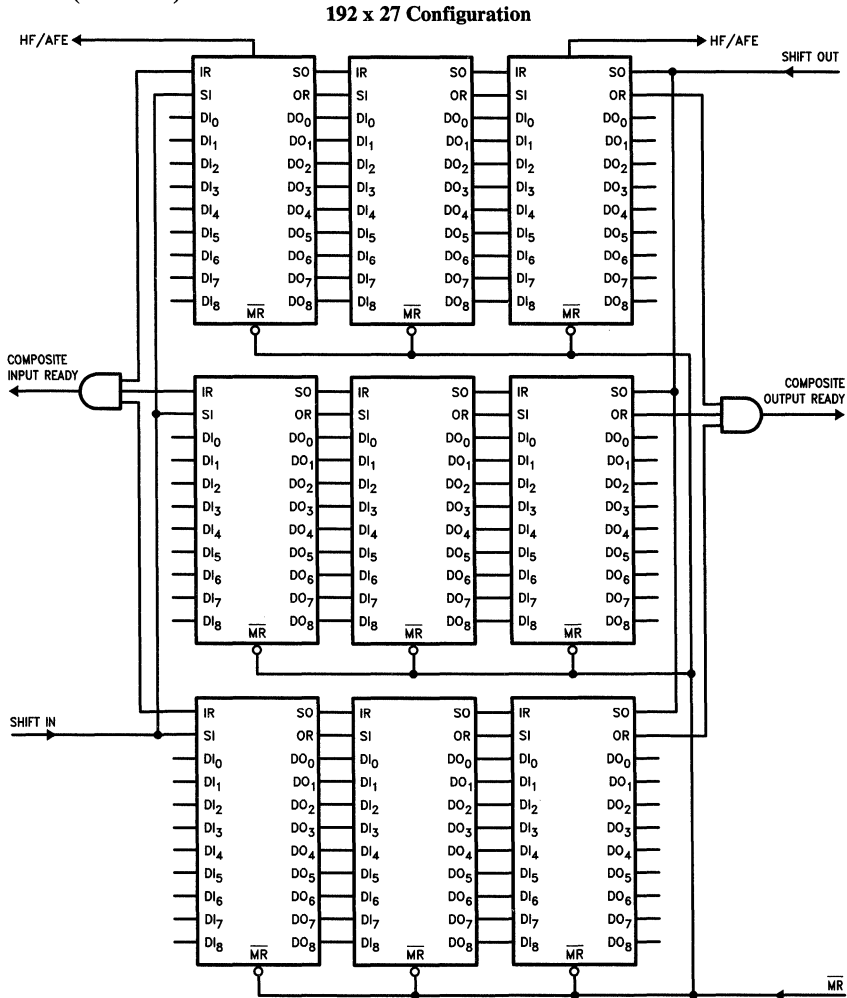
0065-12

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

### User Notes referencing *Figures 6 and 7:*

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will fall through the memory to the output. OR will go HIGH for one internal cycle (at least  $t_{POR}$ ) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW.

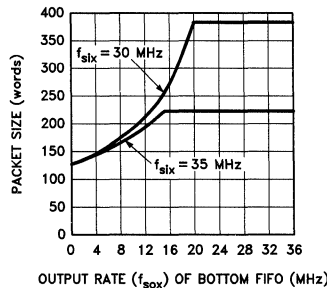
FIFO Expansion (Continued)



0065-13

**Figure 7. Depth and Width Expansion**

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the variation of delays of the FIFOs.



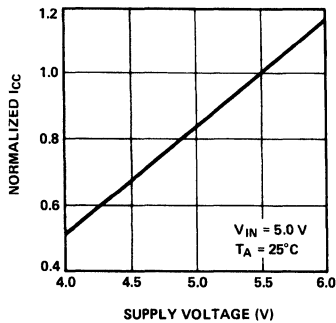
OUTPUT RATE ( $f_{sock}$ ) OF BOTTOM FIFO (MHz)

0065-24

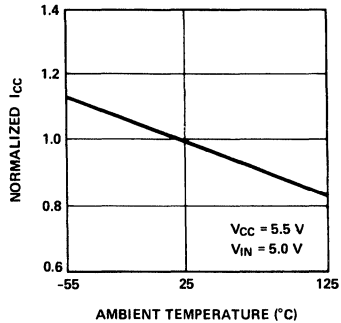
**Figure 8. Virtual Capacity vs. Output Rate for Two FIFOs Cascaded Using an Inverter**

## Typical DC and AC Characteristics

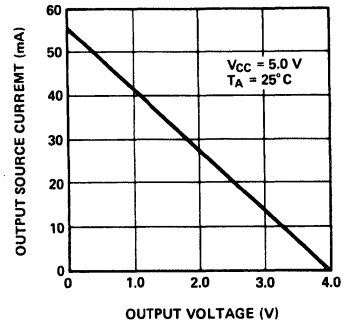
**NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE**



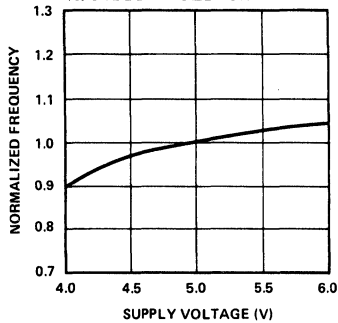
**NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE**



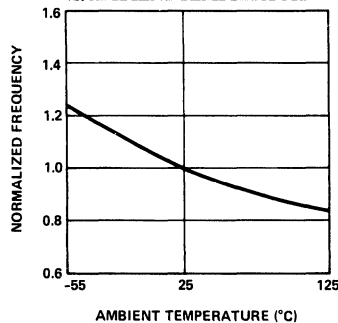
**OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE**



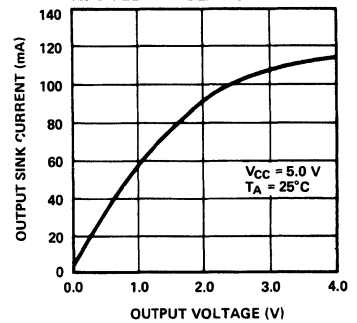
**NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE**



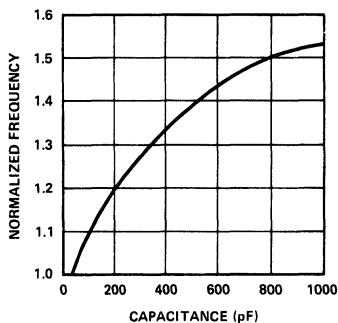
**NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE**



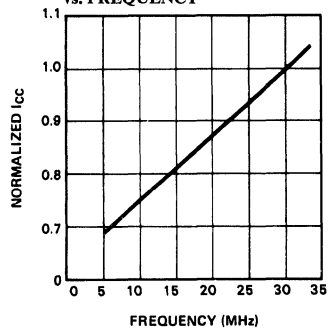
**OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE**



**TYPICAL FREQUENCY CHANGE vs. OUTPUT LOADING**



**NORMALIZED  $I_{CC}$  vs. FREQUENCY**



**Ordering Information**

| Frequency (MHz) | Ordering Code  | Package Type | Operating Range |
|-----------------|----------------|--------------|-----------------|
| 35              | CY7C408A-35PC  | P21          | Commercial      |
|                 | CY7C408A-35DC  | D22          |                 |
|                 | CY7C408A-35LC  | L64          |                 |
|                 | CY7C408A-35VC  | V21          |                 |
| 25              | CY7C408A-25PC  | P21          | Commercial      |
|                 | CY7C408A-25DC  | D22          |                 |
|                 | CY7C408A-25LC  | L64          |                 |
|                 | CY7C408A-25VC  | V21          |                 |
|                 | CY7C408A-25DMB | D22          | Military        |
|                 | CY7C408A-25LMB | L64          |                 |
| 15              | CY7C408A-15PC  | P21          | Commercial      |
|                 | CY7C408A-15DC  | D22          |                 |
|                 | CY7C408A-15LC  | L64          |                 |
|                 | CY7C408A-15VC  | V21          |                 |
|                 | CY7C408A-15DMB | D22          | Military        |
|                 | CY7C408A-15LMB | L64          |                 |

| Frequency (MHz) | Ordering Code  | Package Type | Operating Range |
|-----------------|----------------|--------------|-----------------|
| 35              | CY7C409A-35PC  | P21          | Commercial      |
|                 | CY7C409A-35DC  | D22          |                 |
|                 | CY7C409A-35LC  | L64          |                 |
|                 | CY7C409A-35VC  | V21          |                 |
| 25              | CY7C409A-25PC  | P21          | Commercial      |
|                 | CY7C409A-25DC  | D22          |                 |
|                 | CY7C409A-25LC  | L64          |                 |
|                 | CY7C409A-25VC  | V21          |                 |
|                 | CY7C409A-25DMB | D22          | Military        |
|                 | CY7C409A-25LMB | L64          |                 |
| 15              | CY7C409A-15PC  | P21          | Commercial      |
|                 | CY7C409A-15DC  | D22          |                 |
|                 | CY7C409A-15LC  | L64          |                 |
|                 | CY7C409A-15VC  | V21          |                 |
|                 | CY7C409A-15DMB | D22          | Military        |
|                 | CY7C409A-15LMB | L64          |                 |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>Ix</sub>      | 1,2,3     |
| I <sub>OS</sub>      | 1,2,3     |
| I <sub>CCQ</sub>     | 1,2,3     |

**5**

#### Switching Characteristics

| Parameters         | Subgroups   |
|--------------------|-------------|
| f <sub>O</sub>     | 7,8,9,10,11 |
| t <sub>PHSI</sub>  | 7,8,9,10,11 |
| t <sub>PLSI</sub>  | 7,8,9,10,11 |
| t <sub>SSI</sub>   | 7,8,9,10,11 |
| t <sub>HSI</sub>   | 7,8,9,10,11 |
| t <sub>DLIR</sub>  | 7,8,9,10,11 |
| t <sub>DHIR</sub>  | 7,8,9,10,11 |
| t <sub>PHSO</sub>  | 7,8,9,10,11 |
| t <sub>PLSO</sub>  | 7,8,9,10,11 |
| t <sub>DLOR</sub>  | 7,8,9,10,11 |
| t <sub>DHOR</sub>  | 7,8,9,10,11 |
| t <sub>SOR</sub>   | 7,8,9,10,11 |
| t <sub>HSO</sub>   | 7,8,9,10,11 |
| t <sub>BT</sub>    | 7,8,9,10,11 |
| t <sub>SIR</sub>   | 7,8,9,10,11 |
| t <sub>HIR</sub>   | 7,8,9,10,11 |
| t <sub>PIR</sub>   | 7,8,9,10,11 |
| t <sub>POR</sub>   | 7,8,9,10,11 |
| t <sub>SIIR</sub>  | 7,8,9,10,11 |
| t <sub>SOOR</sub>  | 7,8,9,10,11 |
| t <sub>DLZOE</sub> | 7,8,9,10,11 |
| t <sub>DHZOE</sub> | 7,8,9,10,11 |
| t <sub>DHHF</sub>  | 7,8,9,10,11 |
| t <sub>DLHF</sub>  | 7,8,9,10,11 |

| Parameters         | Subgroups   |
|--------------------|-------------|
| t <sub>DLAFE</sub> | 7,8,9,10,11 |
| t <sub>DHAFE</sub> | 7,8,9,10,11 |
| t <sub>B</sub>     | 7,8,9,10,11 |
| t <sub>OD</sub>    | 7,8,9,10,11 |
| t <sub>PMR</sub>   | 7,8,9,10,11 |
| t <sub>DSI</sub>   | 7,8,9,10,11 |
| t <sub>DOR</sub>   | 7,8,9,10,11 |
| t <sub>DIR</sub>   | 7,8,9,10,11 |
| t <sub>LZMR</sub>  | 7,8,9,10,11 |
| t <sub>AFE</sub>   | 7,8,9,10,11 |
| t <sub>HF</sub>    | 7,8,9,10,11 |



Cascadeable 512 x 9 FIFO  
Cascadeable 1024 x 9 FIFO  
Cascadeable 2048 x 9 FIFO

Features

- 512 x 9, 1024 x 9, 2048 x 9 FIFO buffer memory
- Dual port RAM cell
- Asynchronous read/write
- High speed 25 MHz read/write independent of depth/width
- Low operating power  
ICC (max.) = 125 mA commercial  
ICC (max.) = 140 mA military
- Half full flag in standalone
- Empty and full flags
- Retransmit in standalone
- Expandable in width and depth
- Parallel Cascade minimizes bubblethrough
- 5V ± 10% supply
- 300 mil DIP packaging
- 300 mil SOJ (512 x 9) packaging
- TTL compatible
- Three-state outputs

- CY7C421 pin compatible and functional equivalent to IDT7201

Functional Description

The (CY7C420, CY7C421,) (CY7C424, CY7C425,) and (CY7C428, CY7C429) are, respectively, 512, 1024 and 2048 words by 9-bit wide first-in first-out (FIFO) memories offered in 600 mil wide and 300 mil wide packages, respectively. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent over-run and under-run. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays so that throughput is not reduced. Data is steered in a similar manner.

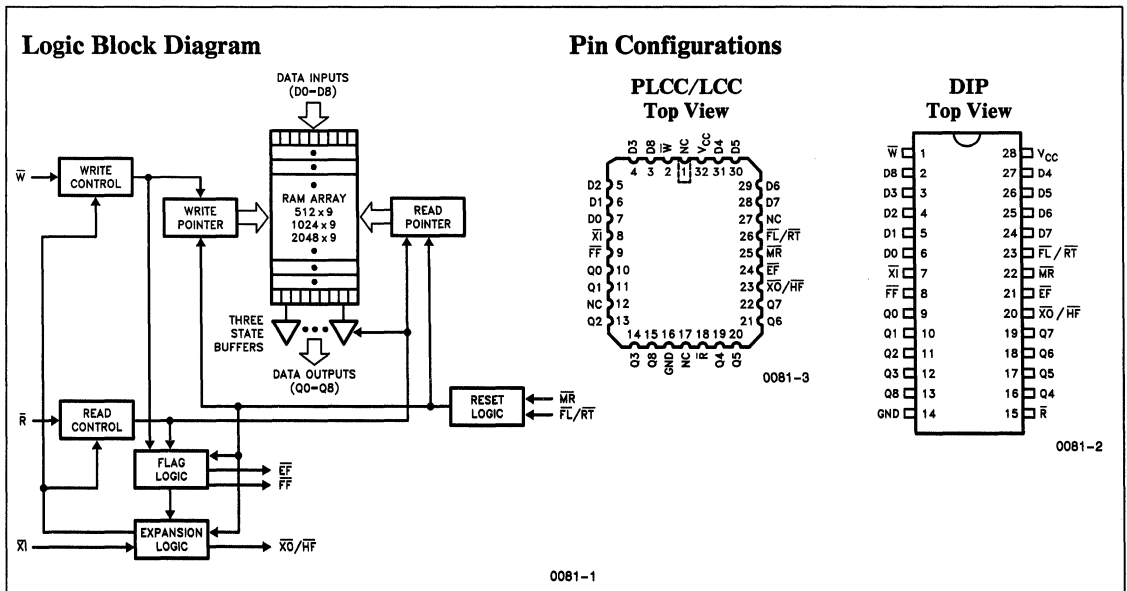
The read and write operations may be asynchronous; each can occur at a rate of 25 MHz. The write operation occurs

when the Write ( $\bar{W}$ ) signal is LOW. Read occurs when Read ( $\bar{R}$ ) goes LOW. The 9 data outputs go to the high impedance state when  $\bar{R}$  is HIGH.

A Half-Full ( $\bar{HF}$ ) output flag is provided that is valid in the standalone and width expansion configurations. In the depth expansion configuration this pin provides the expansion out ( $\bar{XO}$ ) information which is used to tell the next FIFO that it will be activated.

In the standalone and width expansion configurations a LOW on the Retransmit ( $\bar{RT}$ ) input causes the FIFO's to retransmit the data. Read Enable ( $\bar{R}$ ) and Write Enable ( $\bar{W}$ ) must both be HIGH during a retransmit cycle, and then  $\bar{R}$  is used to access the data.

The CY7C420, CY7C421, CY7C424, CY7C425, CY7C428 and CY7C429 are fabricated using an advanced 0.8 micron N-well CMOS technology. Input ESD protection is greater than 2000V and latchup is prevented by careful layout, guard rings and a substrate bias generator.



## Selection Guide

|                                |            | 7C420-30, 7C421-30<br>7C424-30, 7C425-30<br>7C428-30, 7C429-30 | 7C420-40, 7C421-40<br>7C424-40, 7C425-40<br>7C428-40, 7C429-40 | 7C420-65, 7C421-65<br>7C424-65, 7C425-65<br>7C428-65, 7C429-65 |
|--------------------------------|------------|--|--|--|
| Frequency (MHz)                |            | 25   | 20   | 12.5   |
| Access Time (ns)               |            | 30   | 40   | 65   |
| Maximum Operating Current (mA) | Commercial | 125  | 115  | 100  |
|                                | Military   | 140  | 130  | 115  |

Shaded area contains preliminary information.

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential .... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Power Dissipation ..... 1.0W

Output Current, into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... > 2001V  
(per MIL-STD-883 Method 3015)

Latch-up Current ..... > 200 mA

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ± 10%        |

**5**

### Electrical Characteristics Over Operating Range<sup>[4]</sup>

| Parameters       | Description                                 | Test Conditions   | CY7C420-30<br>CY7C421-30<br>CY7C424-30<br>CY7C425-30<br>CY7C428-30<br>CY7C429-30 |      | CY7C420-40<br>CY7C421-40<br>CY7C424-40<br>CY7C425-40<br>CY7C428-40<br>CY7C429-40 |      | CY7C420-65<br>CY7C421-65<br>CY7C424-65<br>CY7C425-65<br>CY7C428-65<br>CY7C429-65 |      | Units           |   |
|------------------|---|---|--|------|--|------|--|------|-----------------|---|
|                  |   |   | Min.   | Max. | Min.   | Max. | Min.   | Max. |                 |   |
| V <sub>OH</sub>  | Output HIGH Voltage                         | V <sub>CC</sub> = Min., I <sub>OH</sub> = -2 mA               | 2.4  |      | 2.4  |      | 2.4  |      | V               |   |
| V <sub>OL</sub>  | Output LOW Voltage                          | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA              |  | 0.4  |  | 0.4  |  | 0.4  | V               |   |
| V <sub>IH</sub>  | Input HIGH Voltage                          |   | Commercial   | 2.0  | V <sub>CC</sub>  | 2.0  | V <sub>CC</sub>  | 2.0  | V <sub>CC</sub> | V |
|                  |   |   | Military   | 2.2  | V <sub>CC</sub>  | 2.2  | V <sub>CC</sub>  | 2.2  | V <sub>CC</sub> | V |
| V <sub>IL</sub>  | Input LOW Voltage                           |   | -3.0   | 0.8  | -3.0   | 0.8  | -3.0   | 0.8  | V               |   |
| I <sub>IX</sub>  | Input Leakage Current                       | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                        | -10  | +10  | -10  | +10  | -10  | +10  | μA              |   |
| I <sub>OZ</sub>  | Output Leakage Current                      | R̄ ≥ V <sub>IH</sub> , GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> | -10  | +10  | -10  | +10  | -10  | +10  | μA              |   |
| I <sub>CC</sub>  | Operating Current                           | V <sub>CC</sub> = Max.,<br>I <sub>OUT</sub> = 0 mA            | Commercial <sup>[5]</sup>  | 125  |  | 115  |  | 100  | mA              |   |
|                  |   |   | Military <sup>[6]</sup>  | 140  |  | 130  |  | 115  | mA              |   |
| I <sub>SB1</sub> | Standby Current                             | All Inputs = V <sub>IH</sub> Min.                             | Commercial   | 25   |  | 25   |  | 25   | mA              |   |
|                  |   |   | Military   | 30   |  | 30   |  | 30   | mA              |   |
| I <sub>SB2</sub> | Power Down Current                          | All Inputs<br>V <sub>CC</sub> - 0.2V                          | Commercial   | 20   |  | 20   |  | 20   | mA              |   |
|                  |   |   | Military   | 25   |  | 25   |  | 25   | mA              |   |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[1]</sup> | V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND                |  | -90  |  | -90  |  | -90  | mA              |   |

Shaded area contains preliminary information.

### Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions                  | Max. | Units |
|------------------|--------------------|----------------------------------|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance | V <sub>CC</sub> = 4.5V           | 7    |       |

#### Notes:

- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

$$5. I_{CC}(\text{commercial}) = 100 \text{ mA} + [(\hat{f} - 12.5) * 2 \text{ mA/MHz}] \text{ for } \hat{f} \geq 12.5 \text{ MHz}$$

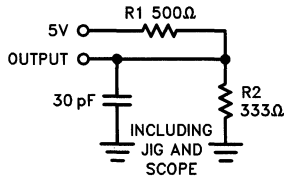
where  $\hat{f}$  = the larger of the write or read operating frequency.

$$6. I_{CC}(\text{military}) = 115 \text{ mA} + [(\hat{f} - 12.5) * 2 \text{ mA/MHz}] \text{ for } \hat{f} \geq 12.5 \text{ MHz}$$

where  $\hat{f}$  = the larger of the write or read operating frequency.

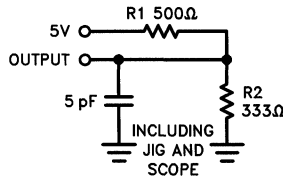


## AC Test Load and Waveform



0081-4

Figure 1a



0081-18

Figure 1b

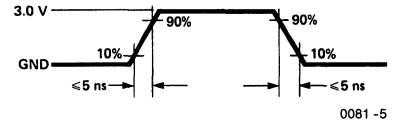
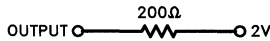


Figure 2. All Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



0081-6

## Switching Characteristics Over the Operating Range<sup>[1, 4]</sup>

| Parameter          | Description              | 7C420-30, 7C421-30<br>7C424-30, 7C425-30<br>7C428-30, 7C429-30 |      | 7C420-40, 7C421-40<br>7C424-40, 7C425-40<br>7C428-40, 7C429-40 |      | 7C420-65, 7C421-65<br>7C424-65, 7C425-65<br>7C428-65, 7C429-65 |      | Units |
|--------------------|--------------------------|--|------|--|------|--|------|-------|
|                    |                          | Min.   | Max. | Min.   | Max. | Min.   | Max. |       |
| $t_{RC}$           | Read Cycle Time          | 40   |      | 50   |      | 80   |      | ns    |
| $t_A$              | Access Time              |  | 30   |  | 40   |  | 65   | ns    |
| $t_{RR}$           | Read Recovery Time       | 10   |      | 10   |      | 15   |      | ns    |
| $t_{PR}$           | Read Pulse Width         | 30   |      | 40   |      | 65   |      | ns    |
| $t_{LZR}^{[3]}$    | Read LOW to Low Z        | 3  |      | 3  |      | 3  |      | ns    |
| $t_{DVR}^{[2, 3]}$ | Read HIGH to Data Valid  | 3  |      | 3  |      | 3  |      | ns    |
| $t_{HZR}^{[2, 3]}$ | Read HIGH to High Z      |  | 20   |  | 25   |  | 30   | ns    |
| $t_{WC}$           | Write Cycle Time         | 40   |      | 50   |      | 80   |      | ns    |
| $t_{PW}$           | Write Pulse Width        | 30   |      | 40   |      | 65   |      | ns    |
| $t_{HWZ}^{[3]}$    | Write HIGH to Low Z      | 10   |      | 10   |      | 10   |      | ns    |
| $t_{WR}$           | Write Recovery Time      | 10   |      | 10   |      | 15   |      | ns    |
| $t_{SD}$           | Data Set-Up Time         | 18   |      | 20   |      | 30   |      | ns    |
| $t_{HD}$           | Data Hold Time           | 0  |      | 0  |      | 10   |      | ns    |
| $t_{MRSC}$         | MR Cycle Time            | 40   |      | 50   |      | 80   |      | ns    |
| $t_{PMR}$          | MR Pulse Width           | 30   |      | 40   |      | 65   |      | ns    |
| $t_{RMR}$          | MR Recovery Time         | 10   |      | 10   |      | 15   |      | ns    |
| $t_{RPW}$          | Read HIGH to MR HIGH     | 30   |      | 40   |      | 65   |      | ns    |
| $t_{WPW}$          | Write HIGH to MR HIGH    | 30   |      | 40   |      | 65   |      | ns    |
| $t_{RTC}$          | Retransmit Cycle Time    | 40   |      | 50   |      | 80   |      | ns    |
| $t_{PRT}$          | Retransmit Pulse Width   | 30   |      | 40   |      | 65   |      | ns    |
| $t_{RTR}$          | Retransmit Recovery Time | 10   |      | 10   |      | 15   |      | ns    |
| $t_{EFL}$          | MR to EF LOW             |  | 40   |  | 50   |  | 80   | ns    |
| $t_{HFH}$          | MR to HF HIGH            |  | 40   |  | 50   |  | 80   | ns    |
| $t_{FFH}$          | MR to FF HIGH            |  | 40   |  | 50   |  | 80   | ns    |
| $t_{REF}$          | Read LOW to EF LOW       |  | 30   |  | 35   |  | 60   | ns    |
| $t_{RFF}$          | Read HIGH to FF HIGH     |  | 30   |  | 35   |  | 60   | ns    |
| $t_{WEF}$          | Write HIGH to EF HIGH    |  | 30   |  | 35   |  | 60   | ns    |
| $t_{WFF}$          | Write LOW to FF LOW      |  | 30   |  | 35   |  | 60   | ns    |

Shaded area contains preliminary information.

Switching Characteristics Over the Operating Range<sup>[1, 4]</sup> (Continued)

| Parameter | Description  | 7C420-30, 7C421-30<br>7C424-30, 7C425-30<br>7C428-30, 7C429-30 |                                  | 7C420-40, 7C421-40<br>7C424-40, 7C425-40<br>7C428-40, 7C429-40 |      | 7C420-65, 7C421-65<br>7C424-65, 7C425-65<br>7C428-65, 7C429-65 |      | Units |
|-----------|--|--|----------------------------------|--|------|--|------|-------|
|           |  | Min.   | Max.                             | Min.   | Max. | Min.   | Max. |       |
|           |  | $t_{WHF}$  | Write LOW to $\overline{HF}$ LOW |  | 40   |  | 50   |       |
| $t_{RHF}$ | Read HIGH to $\overline{HF}$ HIGH                      |  | 40                               |  | 50   |  | 80   | ns    |
| $t_{RAE}$ | Effective Read from Write HIGH                         |  | 30                               |  | 35   |  | 60   | ns    |
| $t_{RPE}$ | Effective Read Pulse Width after EF HIGH               | 30   |                                  | 40   |      | 65   |      | ns    |
| $t_{WAF}$ | Effective Write from Read HIGH                         |  | 30                               |  | 35   |  | 60   | ns    |
| $t_{WPF}$ | Effective Write Pulse Width after $\overline{FF}$ HIGH | 30   |                                  | 40   |      | 65   |      | ns    |
| $t_{XOL}$ | Expansion Out LOW Delay from Clock                     |  | 30                               |  | 40   |  | 65   | ns    |
| $t_{XOH}$ | Expansion Out HIGH Delay from Clock                    |  | 30                               |  | 40   |  | 65   | ns    |

5

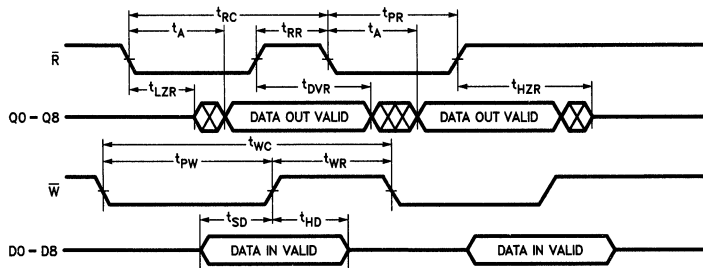
Shaded area contains preliminary information.

Notes:

1. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance, as in Figure 1a, unless otherwise specified.
2.  $t_{HZR}$  and  $t_{DVR}$  use capacitance loading as in Figure 1b.
3.  $t_{HZR}$  transition is measured at +500 mV from  $V_{OL}$  and -500 mV from  $V_{OH}$ .  $t_{DVR}$  transition is measured at the 1.5V level.  $t_{HWZ}$  and  $t_{LZR}$  transition is measured at  $\pm 100$  mV from the steady state.
4. See the last page of this specification for Group A subgroup testing information.

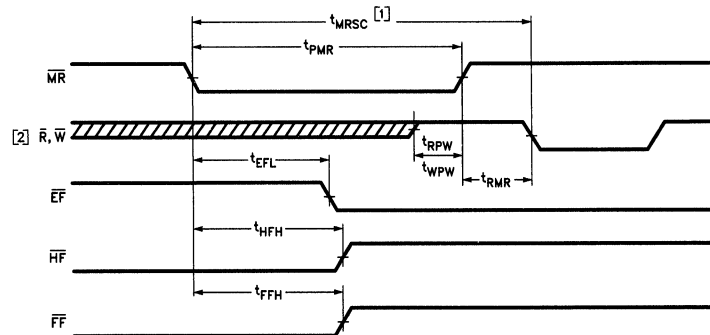
Switching Waveforms

Asynchronous Read and Write Timing Diagram



0081-7

Master Reset Timing Diagram



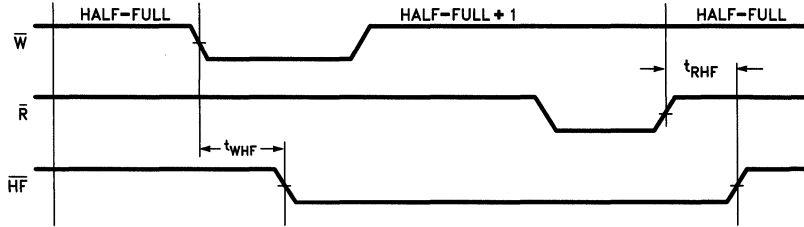
0081-8

Notes:

1.  $t_{MRSC} = t_{PMR} + t_{RMR}$ .
2.  $\overline{W}$  and  $\overline{R} = V_{IH}$  around the rising edge of  $\overline{MR}$ .

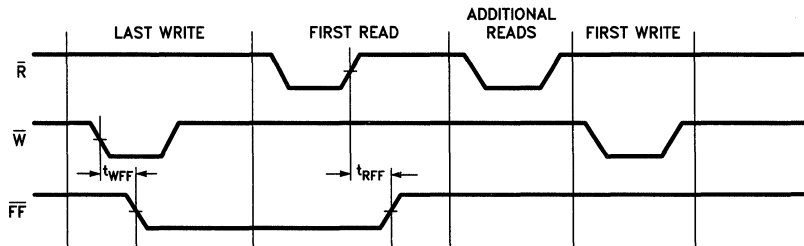
## Switching Waveforms (Continued)

### Half-Full Flag Timing Diagram



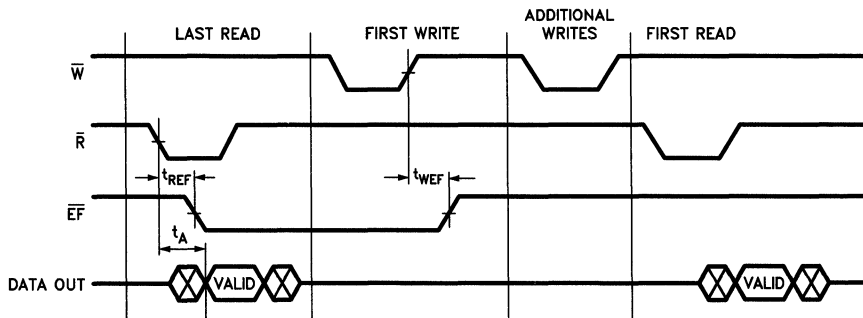
0081-9

### Last WRITE to First READ Full Flag Timing Diagram



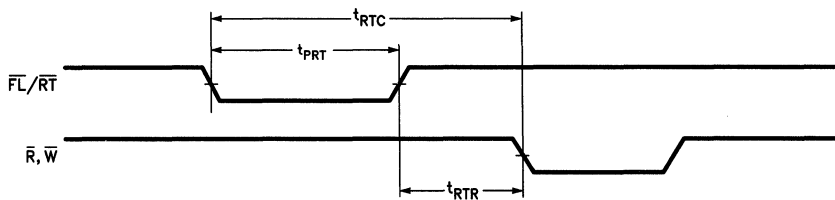
0081-10

### Last READ to First WRITE Empty Flag Timing Diagram



0081-11

### Retransmit Timing Diagram



0081-12

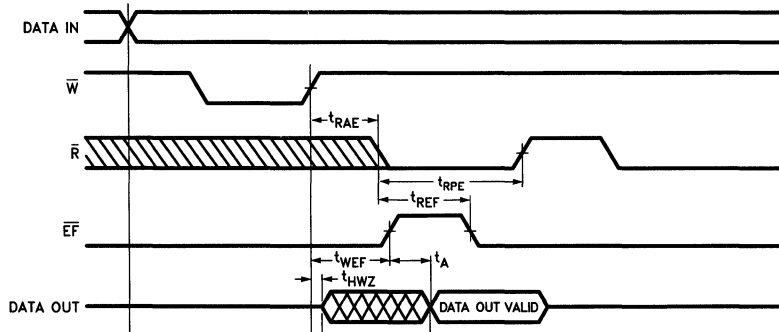
#### Notes:

1.  $t_{RTC} = t_{RT} + t_{RTR}$ .

2. EF, HF and FF may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at  $t_{RTC}$ .

## Switching Waveforms (Continued)

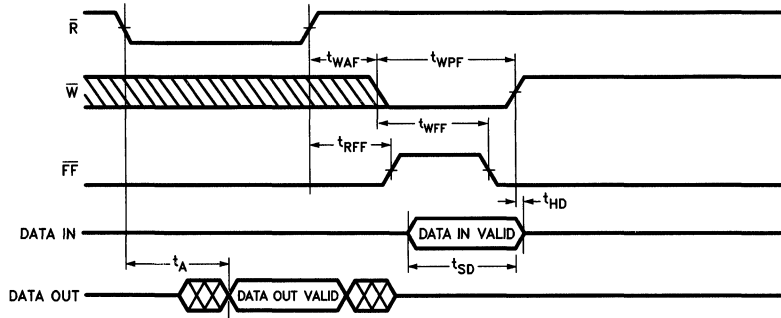
### Empty Flag and Read Bubble-Through Mode Timing Diagram



0081-13

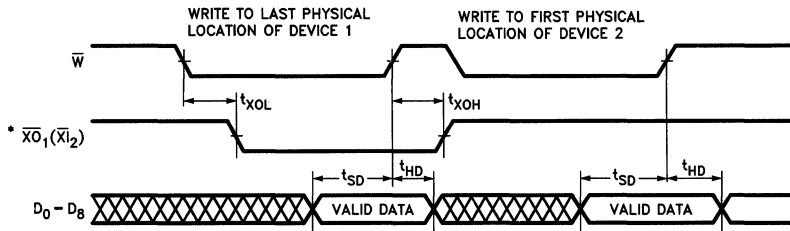
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### Full Flag and Write Bubble-Through Mode Timing Diagram

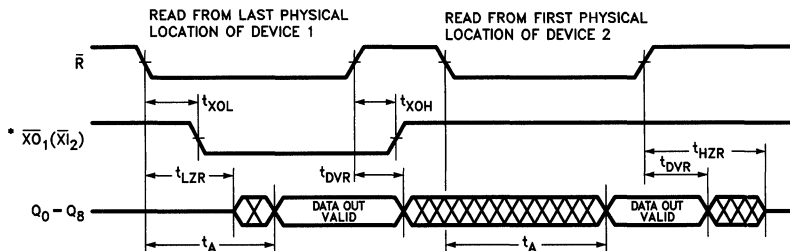


0081-14

### Expansion Timing Diagrams



0081-15



0081-16

\*Expansion Out of Device 1 ( $\overline{XO_1}$ ) is connected to Expansion In of Device 2 ( $\overline{XI_2}$ ).

## Architecture

The CY7C420/421/424/425/428/429 FIFOs consist of an array of 512/1024/2048 words of 9-bits each (implemented by an array of dual port RAM cells), a read pointer, a write pointer, control signals ( $\bar{W}$ ,  $\bar{R}$ ,  $\bar{X}$ ,  $\bar{I}$ ,  $\bar{X}$ ,  $\bar{O}$ ,  $\bar{F}$ ,  $\bar{L}$ ,  $\bar{R}$ ,  $\bar{T}$ ,  $\bar{M}$ ) and Full, Half Full, and Empty flags.

### Dual Port RAM

The dual port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data to propagate through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

### Resetting the FIFO

Upon power up, the FIFO must be reset with a Master Reset ( $\bar{M}$ ) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ( $\bar{E}$ ) being LOW, and both the Half-Full ( $\bar{H}$ ) and Full flag ( $\bar{F}$ ) resetting to HIGH. Read ( $\bar{R}$ ) and Write ( $\bar{W}$ ) must be HIGH  $t_{RPW}/t_{WPW}$  before and  $t_{RMR}$  after the rising edge of  $\bar{M}$  for a valid reset cycle.

### Writing Data to the FIFO

The availability of an empty location is indicated by the HIGH state of the Full flag ( $\bar{F}$ ). A falling edge of Write ( $\bar{W}$ ) initiates a write cycle. Data appearing at the inputs ( $D_0$ – $D_8$ )  $t_{SD}$  before and  $t_{HD}$  after the rising edge of  $\bar{W}$  will be stored sequentially in the FIFO.

The Empty flag ( $\bar{E}$ ) LOW to HIGH transition occurs  $t_{WEF}$  after the first LOW to HIGH transition on the write clock of an empty FIFO. The Half-Full flag ( $\bar{H}$ ) will go LOW on the falling edge of the write clock following the occurrence of half full.  $\bar{H}$  will remain LOW while less than one half of the total memory of this device is available for writing. The LOW to HIGH transition of the  $\bar{H}$  flag occurs on the rising edge of Read ( $\bar{R}$ ).  $\bar{H}$  is available in Single Device Mode only. The Full flag ( $\bar{F}$ ) goes low on the falling edge of  $\bar{W}$  during the cycle in which the last available location in the FIFO is written, prohibiting overflow.  $\bar{F}$  goes HIGH  $t_{RFF}$  after the completion of a valid read of a full FIFO.

### Reading Data from the FIFO

The falling edge of Read ( $\bar{R}$ ) initiates a read cycle if the Empty flag ( $\bar{E}$ ) is not LOW. Data outputs ( $Q_0$ – $Q_8$ ) are in a high impedance condition between read operations ( $\bar{R}$  HIGH), when the FIFO is empty, or when the FIFO is in the Depth Expansion Mode but is not the active device.

The falling edge of  $\bar{R}$  during the last read cycle before the empty condition triggers a HIGH to LOW transition of  $\bar{E}$ , prohibiting any further read operations until  $t_{WEF}$  after a valid write.

### Retransmit

The Retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be interrogated by the receiver and retransmitted if necessary.

The Retransmit ( $\bar{R}$ ) input is active in the Single Device Mode only. The Retransmit feature is intended for use when 512/1024/2048 (corresponding to device depth) or less writes have occurred since the previous  $\bar{M}$  cycle. A LOW pulse on  $\bar{R}$  resets the internal read pointer to the first physical location of the FIFO. The write pointer is unaffected.  $\bar{R}$  and  $\bar{W}$  must both be HIGH during a retransmit cycle. Full, Half Full and Empty flags are governed by the relative locations of the Read and Write pointers and will be updated by a retransmit operation.

After a retransmit cycle, previously read data may be reaccessed using  $\bar{R}$  to initiate standard read cycles beginning with the first physical location.

### Single Device/Width Expansion Modes

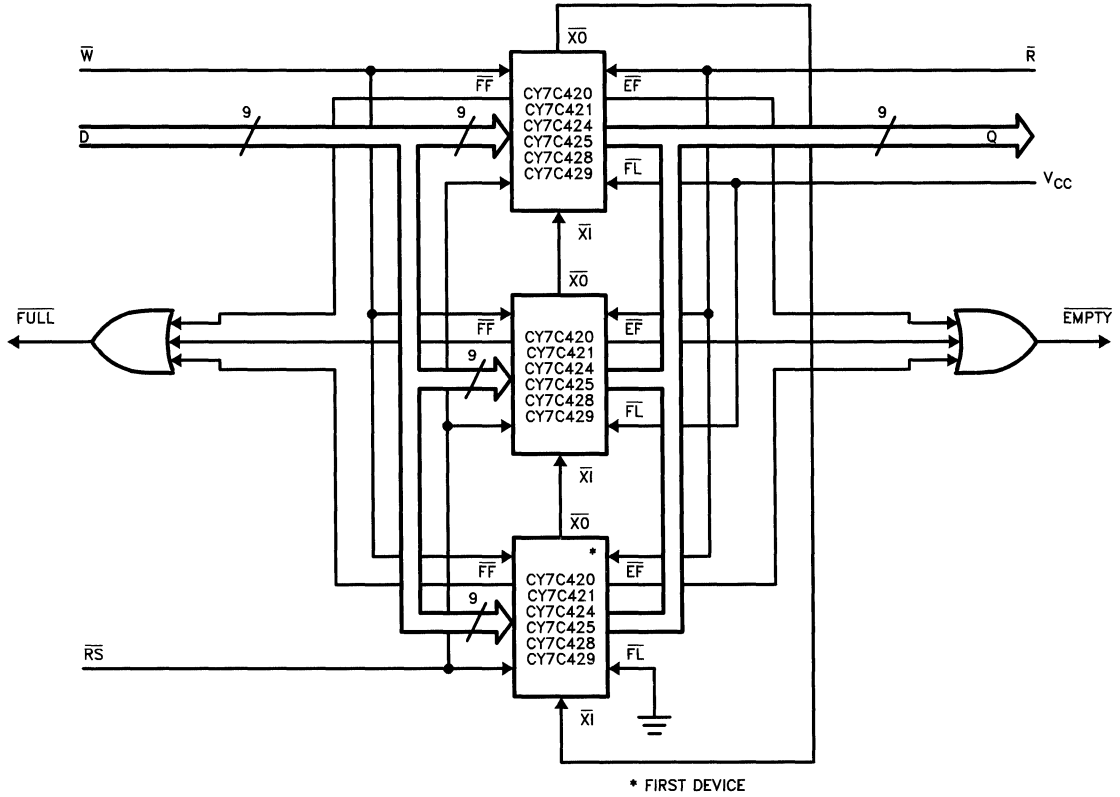
Single Device and Width Expansion Modes are entered by grounding  $\bar{X}$  during a  $\bar{M}$  cycle. During these modes the  $\bar{H}$  and  $\bar{R}$  features are available. FIFOs can be expanded in width to provide word widths greater than 9 in increments of 9. During Width Expansion Mode all control line inputs are common to all devices and flag outputs from any device can be monitored.

### Depth Expansion Mode (Figure 3)

Depth Expansion Mode is entered when, during a  $\bar{M}$  cycle, Expansion Out ( $\bar{X}$ ) of one device is connected to Expansion In ( $\bar{X}$ ) of the next device, with  $\bar{X}$  of the last device connected to  $\bar{X}$  of the first device. In the Depth Expansion Mode the First Load ( $\bar{F}$ ) input, when grounded, indicates that this part is the first to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO,  $\bar{X}$  is pulsed LOW when the last physical location of the previous FIFO is written to and is pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one is enabled for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created of word widths in increments of 9. When expanding in depth, a composite  $\bar{F}$  must be created by OR-ing the  $\bar{F}$ s together. Likewise, a composite  $\bar{E}$  is created by OR-ing the  $\bar{E}$ s together.  $\bar{H}$  and  $\bar{R}$  functions are not available in Depth Expansion Mode.

Architecture (Continued)

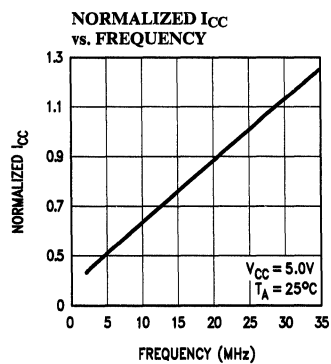
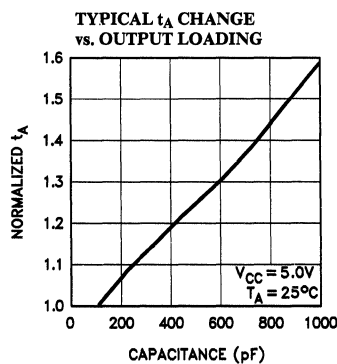
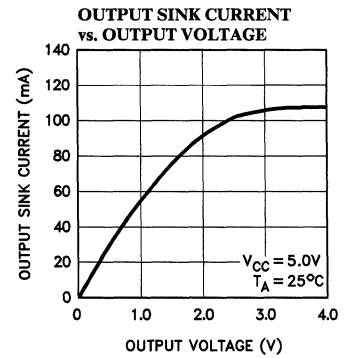
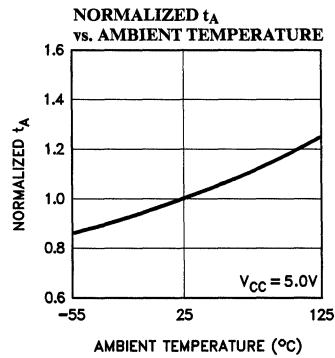
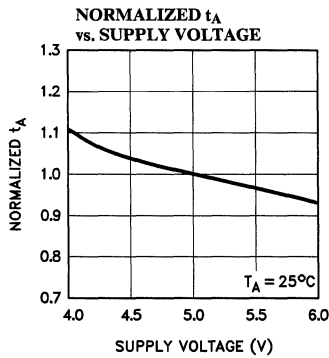
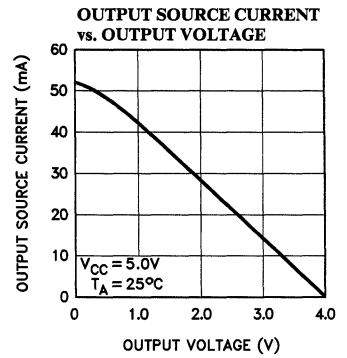
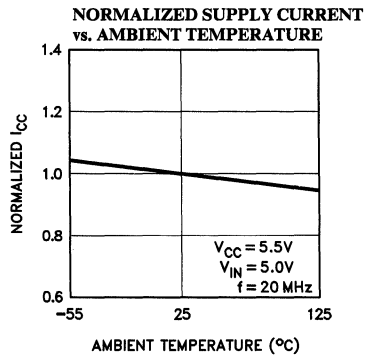
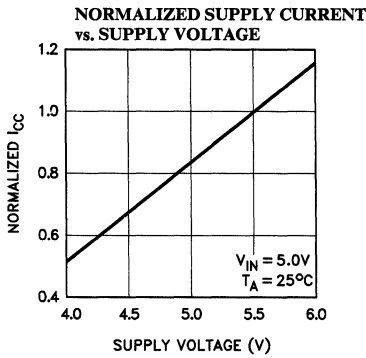


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Figure 3. Depth Expansion

0081-17

## Typical DC and AC Characteristics



**Ordering Information**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 30         | CY7C420-30PC  | P15          | Commercial      |
|            | CY7C420-30DC  | D16          |                 |
|            | CY7C420-30DMB | D16          | Military        |
| 40         | CY7C420-40PC  | P15          | Commercial      |
|            | CY7C420-40DC  | D16          |                 |
|            | CY7C420-40DMB | D16          | Military        |
| 65         | CY7C420-65PC  | P15          | Commercial      |
|            | CY7C420-65DC  | D16          |                 |
|            | CY7C420-65DMB | D16          | Military        |

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 30         | CY7C421-30PC  | P21          | Commercial      |
|            | CY7C421-30JC  | J65          |                 |
|            | CY7C421-30VC  | V21          |                 |
|            | CY7C421-30DC  | D22          |                 |
|            | CY7C421-30LC  | L55          |                 |
|            | CY7C421-30DMB | D22          |                 |
|            | CY7C421-30LMB | L55          |                 |
| 40         | CY7C421-40PC  | P21          | Commercial      |
|            | CY7C421-40JC  | J65          |                 |
|            | CY7C421-40VC  | V21          |                 |
|            | CY7C421-40DC  | D22          |                 |
|            | CY7C421-40LC  | L55          |                 |
|            | CY7C421-40DMB | D22          |                 |
|            | CY7C421-40LMB | L55          |                 |
| 65         | CY7C421-65PC  | P21          | Commercial      |
|            | CY7C421-65JC  | J65          |                 |
|            | CY7C421-65VC  | V21          |                 |
|            | CY7C421-65DC  | D22          |                 |
|            | CY7C421-65LC  | L55          |                 |
|            | CY7C421-65DMB | D22          |                 |
|            | CY7C421-65LMB | L55          |                 |

**5**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 30         | CY7C424-30PC  | P15          | Commercial      |
|            | CY7C424-30DC  | D16          |                 |
|            | CY7C424-30DMB | D16          | Military        |
| 40         | CY7C424-40PC  | P15          | Commercial      |
|            | CY7C424-40DC  | D16          |                 |
|            | CY7C424-40DMB | D16          | Military        |
| 65         | CY7C424-65PC  | P15          | Commercial      |
|            | CY7C424-65DC  | D16          |                 |
|            | CY7C424-65DMB | D16          | Military        |

Shaded area contains preliminary information.

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 30         | CY7C425-30PC  | P21          | Commercial      |
|            | CY7C425-30JC  | J65          |                 |
|            | CY7C425-30DC  | D22          |                 |
|            | CY7C425-30LC  | L55          |                 |
|            | CY7C425-30VC  | V21          |                 |
|            | CY7C425-30DMB | D22          |                 |
|            | CY7C425-30LMB | L55          |                 |
| 40         | CY7C425-40PC  | P21          | Commercial      |
|            | CY7C425-40JC  | J65          |                 |
|            | CY7C425-40DC  | D22          |                 |
|            | CY7C425-40LC  | L55          |                 |
|            | CY7C425-40VC  | V21          |                 |
|            | CY7C425-40DMB | D22          |                 |
|            | CY7C425-40LMB | L55          |                 |
| 65         | CY7C425-65PC  | P21          | Commercial      |
|            | CY7C425-65JC  | J65          |                 |
|            | CY7C425-65DC  | D22          |                 |
|            | CY7C425-65LC  | L55          |                 |
|            | CY7C425-65VC  | V21          |                 |
|            | CY7C425-65DMB | D22          |                 |
|            | CY7C425-65LMB | L55          |                 |



**Ordering Information (Continued)**

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 30         | CY7C428-30PC  | P15          | Commercial      |
|            | CY7C428-30DC  | D16          |                 |
|            | CY7C428-30DMB | D16          | Military        |
| 40         | CY7C428-40PC  | P15          | Commercial      |
|            | CY7C428-40DC  | D16          |                 |
|            | CY7C428-40DMB | D16          | Military        |
| 65         | CY7C428-65PC  | P15          | Commercial      |
|            | CY7C428-65DC  | D16          |                 |
|            | CY7C428-65DMB | D16          | Military        |

Shaded area contains preliminary information.

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 30         | CY7C429-30PC  | P21          | Commercial      |
|            | CY7C429-30JC  | J65          |                 |
|            | CY7C429-30DC  | D22          |                 |
|            | CY7C429-30LC  | L55          |                 |
|            | CY7C429-30VC  | V21          |                 |
|            | CY7C429-30DMB | D22          |                 |
|            | CY7C429-30LMB | L55          |                 |
| 40         | CY7C429-40PC  | P21          | Commercial      |
|            | CY7C429-40JC  | J65          |                 |
|            | CY7C429-40DC  | D22          |                 |
|            | CY7C429-40LC  | L55          |                 |
|            | CY7C429-40VC  | V21          |                 |
|            | CY7C429-40DMB | D22          | Military        |
|            | CY7C429-40LMB | L55          |                 |
| 65         | CY7C429-65PC  | P21          | Commercial      |
|            | CY7C429-65JC  | J65          |                 |
|            | CY7C429-65DC  | D22          |                 |
|            | CY7C429-65LC  | L55          |                 |
|            | CY7C429-65VC  | V21          |                 |
|            | CY7C429-65DMB | D22          |                 |
|            | CY7C429-65LMB | L55          |                 |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>SB1</sub>     | 1,2,3     |
| I <sub>SB2</sub>     | 1,2,3     |
| I <sub>OS</sub>      | 1,2,3     |

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#### Switching Characteristics

| Parameters        | Subgroups |
|-------------------|-----------|
| t <sub>RC</sub>   | 9,10,11   |
| t <sub>A</sub>    | 9,10,11   |
| t <sub>RR</sub>   | 9,10,11   |
| t <sub>PR</sub>   | 9,10,11   |
| t <sub>LZR</sub>  | 9,10,11   |
| t <sub>DVR</sub>  | 9,10,11   |
| t <sub>HZR</sub>  | 9,10,11   |
| t <sub>WC</sub>   | 9,10,11   |
| t <sub>PW</sub>   | 9,10,11   |
| t <sub>HWZ</sub>  | 9,10,11   |
| t <sub>WR</sub>   | 9,10,11   |
| t <sub>SD</sub>   | 9,10,11   |
| t <sub>HD</sub>   | 9,10,11   |
| t <sub>MRSC</sub> | 9,10,11   |
| t <sub>PMR</sub>  | 9,10,11   |
| t <sub>RMR</sub>  | 9,10,11   |
| t <sub>RPW</sub>  | 9,10,11   |
| t <sub>WPW</sub>  | 9,10,11   |
| t <sub>RTC</sub>  | 9,10,11   |
| t <sub>PRT</sub>  | 9,10,11   |
| t <sub>RTR</sub>  | 9,10,11   |
| t <sub>EFL</sub>  | 9,10,11   |
| t <sub>HFH</sub>  | 9,10,11   |
| t <sub>FFH</sub>  | 9,10,11   |

| Parameters       | Subgroups |
|------------------|-----------|
| t <sub>REF</sub> | 9,10,11   |
| t <sub>RFF</sub> | 9,10,11   |
| t <sub>WEF</sub> | 9,10,11   |
| t <sub>WFF</sub> | 9,10,11   |
| t <sub>WHF</sub> | 9,10,11   |
| t <sub>RHF</sub> | 9,10,11   |
| t <sub>RAE</sub> | 9,10,11   |
| t <sub>RPE</sub> | 9,10,11   |
| t <sub>WAF</sub> | 9,10,11   |
| t <sub>WPF</sub> | 9,10,11   |
| t <sub>XOL</sub> | 9,10,11   |
| t <sub>XOH</sub> | 9,10,11   |



# 16 x 16 Multiplier Accumulator

## Features

- **Fast**
  - CY7C510-45 has a 45 ns (max.) clock cycle (commercial)
  - CY7C510-55 has a 55 ns (max.) clock cycle (military)
- **Low Power**
  - $I_{CC}$  (max. at 10 MHz) = 100 mA (commercial)
  - $I_{CC}$  (max. at 10 MHz) = 110 mA (military)
- **V<sub>CC</sub> Margin**
  - $5V \pm 10\%$
  - All parameters guaranteed over commercial and military operating temperature range
- **16 × 16 bit parallel multiplication with accumulation to 35-bit result**

- **Two's complement or unsigned magnitude operation**
- **ESD Protection**
  - Capable of withstanding greater than 2000V static discharge voltage
- **Pin compatible and functionally equivalent to Am29510 and TMC2110**

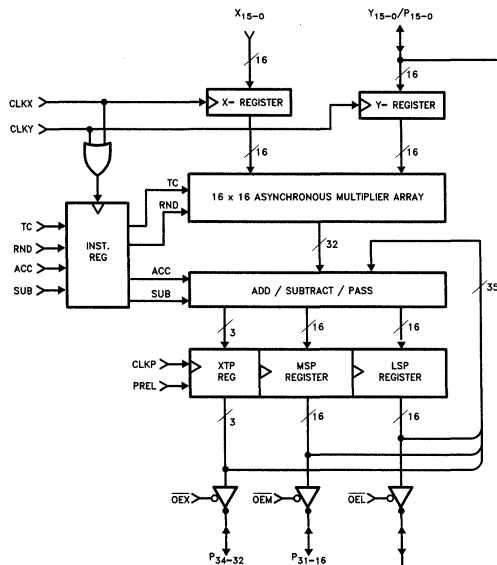
## Functional Description

The CY7C510 is a high-speed 16 × 16 parallel multiplier accumulator which operates at 45 ns clocked multiply accumulate (MAC) time (22 MHz multiply accumulate rate). The operands may be specified as either two's complement or unsigned magnitude 16-bit numbers. The accumulator functions

include loading the accumulator with the current product, adding or subtracting the accumulator contents and the current product, or preloading the accumulator from the external world.

All inputs (data and instructions) and outputs are registered. These independently clocked registers are positive edge triggered D-type flip-flops. The 35-bit accumulator/output register is divided into a 3-bit extended product (XTP), a 16-bit most significant product (MSP), and a 16-bit least significant product (LSP). The XTP and MSP have dedicated ports for three-state output; the LSP is multiplexed with the Y-input. The 35-bit accumulator/output register may be preloaded through the bidirectional output ports.

## Logic Block Diagram



0057-1

## Selection Guide

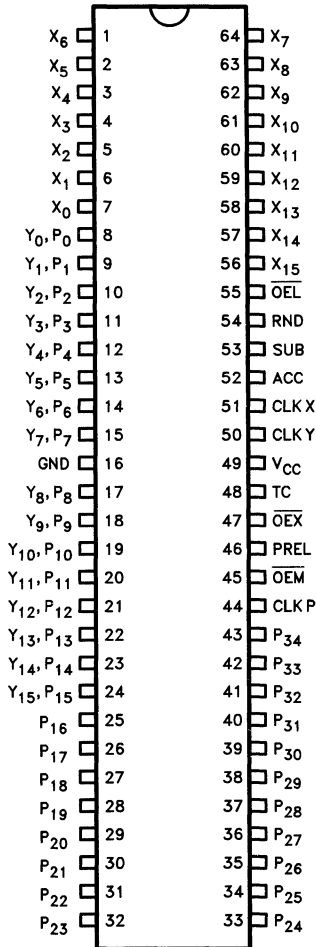
|                                       |            | 7C510-45 | 7C510-55 | 7C510-65 | 7C510-75 |
|---------------------------------------|------------|----------|----------|----------|----------|
| Maximum Multiply-Accumulate Time (ns) | Commercial | 45       | 55       | 65       | 75       |
|                                       | Military   |          | 55       | 65       | 75       |

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Ambient Temperature Under Bias . . . . -55°C to +125°C
- Supply Voltage to Ground Potential . . . . -0.5V to +7.0V
- DC Input Voltage . . . . . -0.5V to +7.0V
- DC Voltage Applied to Outputs . . . . . -0.5V to V<sub>CC</sub> Max.
- Output Current, into Outputs (low) . . . . . 10 mA
- Static Discharge Voltage . . . . . > 2001V (per MIL-STD-883 Method 3015)

### Pin Configurations

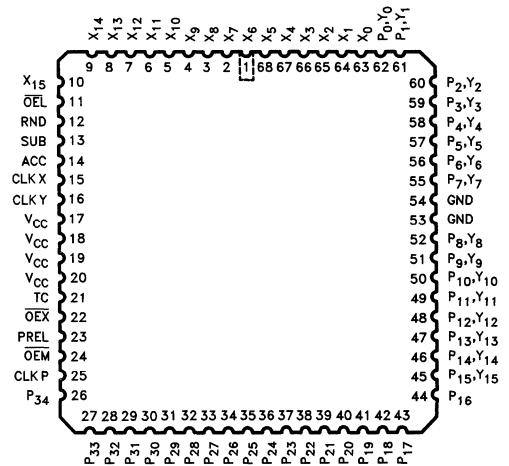


### Operating Range

| Range       | Temperature    | V <sub>CC</sub> |
|-------------|----------------|-----------------|
| Commercial  | 0°C to +70°C   | 5V ± 10%        |
| Military[1] | -55° to +125°C | 5V ± 10%        |

Note:

1. T<sub>A</sub> is the "instant on" case temperature.

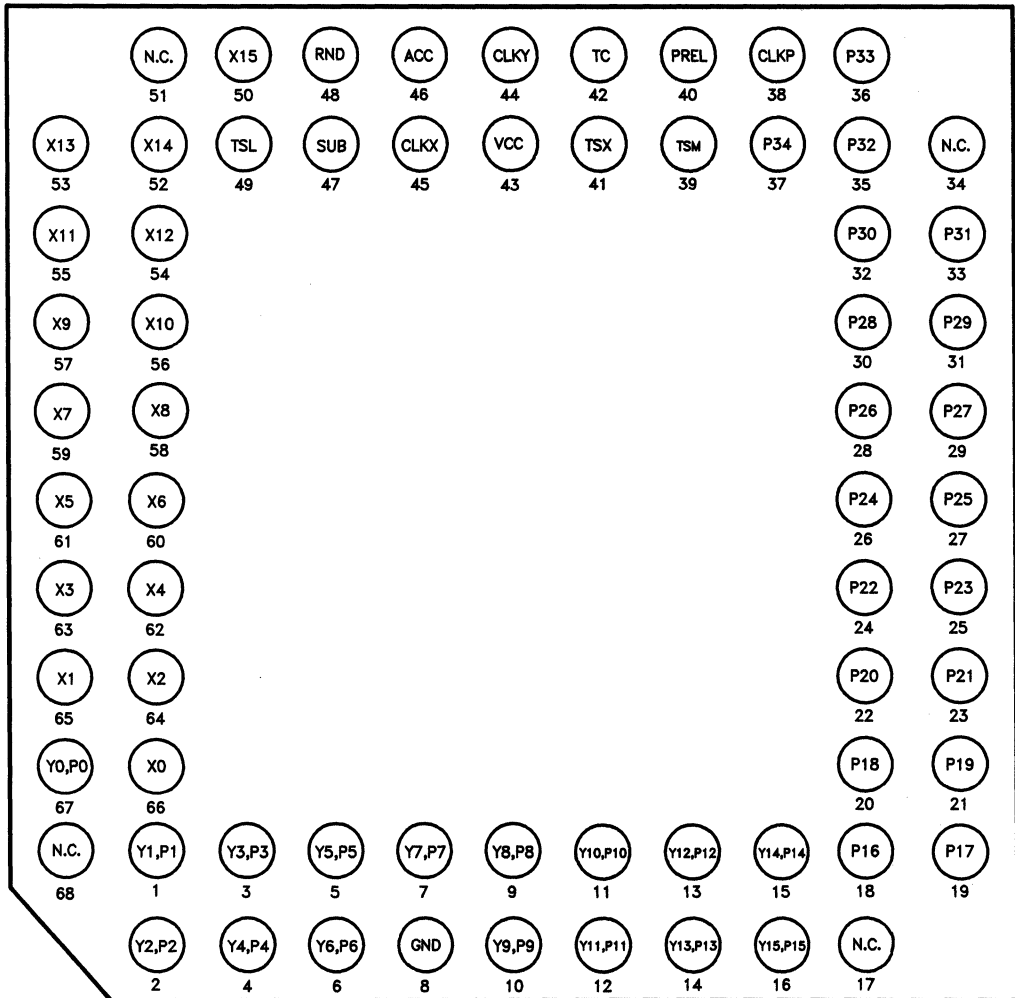


0057-3

0057-2

Pin Configurations (Continued)

Pin Configuration for 68-Pin Grid Array



0057-13

## Pin Definitions

| Signal Name                               | I/O | Description   |
|---|-----|---|
| X <sub>15-0</sub>                         | I   | X-Input Data. This 16-bit number may be interpreted as two's complement or unsigned magnitude.  |
| Y <sub>15-0</sub><br>(P <sub>15-0</sub> ) | I/O | Y-Input Data/LSP Output Data. When this port is used to input a Y value, the 16-bit number may be interpreted as two's complement or unsigned magnitude. This bidirectional port is multiplexed with the LSP output (P <sub>15-0</sub> ), and can also be used to preload the LSP register.   |
| P <sub>34-32</sub>                        | I/O | Extended Product (XTP) Output Data. This port is bidirectional. The extended product emerges through this port. The XTP register may also be preloaded through this port.   |
| P <sub>31-16</sub>                        | I/O | MSP Output Data. This port is bidirectional. The most significant product emerges through this port. The MSP register may also be preloaded through this port.  |
| P <sub>15-0</sub>                         | I/O | LSP Output Data. This port is bidirectional. The least significant product emerges through this port. The LSP register may also be preloaded through this port.   |
| CLKX                                      | I   | X-Register Clock. X-Input Data are latched into the X-register at the rising edge of CLKX.  |
| CLKY                                      | I   | Y-Register Clock. Y-Input Data are latched into the Y-register at the rising edge of CLKY.  |
| CLKP                                      | I   | Product Register Clock. XTP, MSP, and LSP are latched into their respective registers at the rising edge of CLKP. If preload is selected, these registers are loaded with the preload data at the output pins via the bidirectional ports. If preload is not selected, these registers are loaded with the current accumulated product. |
| OEX                                       | I   | Output Enable Extended. When LOW, the extended product bidirectional port is enabled for output. When HIGH, the outputs drivers are disabled (high impedance) and the XTP port may be used for preloading. See Preload Function Table.  |
| OEM                                       | I   | Output Enable Most. When LOW, the MSP bidirectional port is enabled for output. When HIGH, the output drivers are disabled (high impedance) and the MSP port may be used for preloading. See Preload Function Table.  |

| Signal Name | I/O | Description   |
|-------------|-----|---|
| OEL         | I   | Output Enable Least. When LOW, the LSP bidirectional port is enabled for output. When HIGH, the output drivers are disabled (high impedance) and the MSP port may be used for preloading. See Preload Function Table.   |
| PREL        | I   | Preload. When HIGH, the three bidirectional ports may be used to preload data into the accumulator register at the rising edge of CLKP. The three-state controls (OEX, OEM, OEL) must be HIGH to preload data. When LOW, the accumulated product is loaded into the accumulator/output register at the rising edge of CLKP. The output drivers must be enabled (OEX, OEM, OEL must be LOW) for the accumulated product to be output. Ordinarily, PREL, OEX, OEM, and OEL are tied together. See accumulator function table. |
| TC          | I   | Two's Complement Control. When HIGH, the 7C510 is in two's complement mode, where the input and output data are interpreted as two's complement numbers. The device is in unsigned magnitude mode when TC is LOW. This control is loaded into the instruction register at the rising edge of CLKX + CLKY.   |
| RND         | I   | Round Control. When HIGH, rounding is enabled and a "1" is added to the MSB of the LSB (P <sub>15</sub> ). When LOW, the product is unchanged. This control is loaded into the instruction register at the rising edge of CLKX + CLKY.  |
| ACC         | I   | Accumulate Control. When HIGH, the accumulator/output register contents are added to or subtracted from the current product (XY) and this result is stored back into the accumulator/output register. When LOW, the product is loaded into the accumulator register, overwriting the current contents. This control is loaded into the instruction register at the rising edge of CLKX + CLKY. See accumulator function table.  |
| SUB         | I   | Subtract Control. When both ACC and SUB are HIGH, the accumulator register contents are subtracted from the current product XY and this result is written back into the accumulator register. When ACC is HIGH and SUB is LOW, the accumulator register contents and current product are summed, then written back to the accumulator register. This control is loaded into the instruction register at the rising edge of CLKX + CLKY. See accumulator function table.   |

## Functional Description

The CY7C510 is a high-speed  $16 \times 16$ -bit multiplier accumulator (MAC). It comprises a 16-bit parallel multiplier followed by a 35-bit accumulator. All inputs (data and instructions) and outputs are registered. The 7C510 is divided into four sections: the input section, the  $16 \times 16$  asynchronous multiplier array, the accumulator, and the output/preload section.

The input section has two 16-bit operand input registers for the X and Y operands, clocked by the rising edge of CLKX and CLKY, respectively. The four-bit instruction register (TC, RND, ACC, SUB) is clocked by the rising edge of the logical OR of CLKX, CLKY.

The  $16 \times 16$  asynchronous multiplier array produces the 32-bit product of the input operands. Either two's complement or unsigned magnitude operation is selected, based on control TC. If rounding is selected, (RND = 1), a "1" is added to the MSB of the LSP (position P<sub>15</sub>). The 32-bit product is zero-filled or sign-extended as appropriate and passed as a 35-bit number to the accumulator section.

The accumulator function is controlled by ACC, SUB, and PREL. Four functions may be selected: the accumulator may be loaded with the current product; the product may be added to the accumulator contents; the accumulator contents may be subtracted from the current product; or the accumulator may be preloaded from the bidirectional ports.

The output/preload section contains the accumulator/output register and the bidirectional ports. This section is controlled by the signals PREL, OEX, OEM, and OEL. When PREL is HIGH, the output buffers are in high impedance state. When the controls OEX, OEM, and OEL are also high, data present at the output pins will be preloaded into the appropriate accumulator register at the rising edge of CLKP. When PREL is LOW, the signals OEX, OEM, and OEL are enable controls for their respective three-state output ports.

## Preload Function Table

| PREL | OEX | OEM | OEL | Output Register |     |     |
|------|-----|-----|-----|-----------------|-----|-----|
|      |     |     |     | XTP             | MSP | LSP |
| 0    | 0   | 0   | 0   | Q               | Q   | Q   |
| 0    | 0   | 0   | 1   | Q               | Q   | Z   |
| 0    | 0   | 1   | 0   | Q               | Z   | Q   |
| 0    | 0   | 1   | 1   | Q               | Z   | Z   |
| 0    | 1   | 0   | 0   | Z               | Q   | Q   |
| 0    | 1   | 0   | 1   | Z               | Q   | Z   |
| 0    | 1   | 1   | 0   | Z               | Z   | Q   |
| 0    | 1   | 1   | 1   | Z               | Z   | Z   |
| 1    | 0   | 0   | 0   | Z               | Z   | Z   |
| 1    | 0   | 0   | 1   | Z               | Z   | PL  |
| 1    | 0   | 1   | 0   | Z               | PL  | Z   |
| 1    | 0   | 1   | 1   | Z               | PL  | PL  |
| 1    | 1   | 0   | 0   | PL              | Z   | Z   |
| 1    | 1   | 0   | 1   | PL              | Z   | PL  |
| 1    | 1   | 1   | 0   | PL              | PL  | Z   |
| 1    | 1   | 1   | 1   | PL              | PL  | PL  |

Z = Output buffers at High impedance (disabled.)

Q = Output buffers at Low impedance. Contents of output register available through output ports.

PL = Output disabled. Preload data supplied to the output pins will be loaded into the output register at the rising edge of CLKP.

## Accumulator Function Table

| PREL | ACC | SUB | P  | OPERATION |
|------|-----|-----|----|-----------|
| L    | L   | X   | Q  | Load      |
| L    | H   | L   | Q  | Add       |
| L    | H   | H   | Q  | Subtract  |
| H    | X   | X   | PL | Preload   |

## CY7C510 Input Formats

### Fractional Two's Complement Input

| $X_{IN}$  | $Y_{IN}$  |
|---|---|
| 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0   | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0   |
| $-2^0$ $2^{-1}$ $2^{-2}$ $2^{-3}$ $2^{-4}$ $2^{-5}$ $2^{-6}$ $2^{-7}$ $2^{-8}$ $2^{-9}$ $2^{-10}$ $2^{-11}$ $2^{-12}$ $2^{-13}$ $2^{-14}$ $2^{-15}$ | $-2^0$ $2^{-1}$ $2^{-2}$ $2^{-3}$ $2^{-4}$ $2^{-5}$ $2^{-6}$ $2^{-7}$ $2^{-8}$ $2^{-9}$ $2^{-10}$ $2^{-11}$ $2^{-12}$ $2^{-13}$ $2^{-14}$ $2^{-15}$ |
| (Sign)  | (Sign)  |

### Integer Two's Complement Input

| $X_{IN}$   | $Y_{IN}$   |
|--|--|
| 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0  | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0  |
| $-2^{15}$ $2^{14}$ $2^{13}$ $2^{12}$ $2^{11}$ $2^{10}$ $2^9$ $2^8$ $2^7$ $2^6$ $2^5$ $2^4$ $2^3$ $2^2$ $2^1$ $2^0$ | $-2^{15}$ $2^{14}$ $2^{13}$ $2^{12}$ $2^{11}$ $2^{10}$ $2^9$ $2^8$ $2^7$ $2^6$ $2^5$ $2^4$ $2^3$ $2^2$ $2^1$ $2^0$ |
| (Sign)   | (Sign)   |

### Unsigned Fractional Input

| $X_{IN}$   | $Y_{IN}$   |
|--|--|
| 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0  | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0  |
| $2^{-1}$ $2^{-2}$ $2^{-3}$ $2^{-4}$ $2^{-5}$ $2^{-6}$ $2^{-7}$ $2^{-8}$ $2^{-9}$ $2^{-10}$ $2^{-11}$ $2^{-12}$ $2^{-13}$ $2^{-14}$ $2^{-15}$ $2^{-16}$ | $2^{-1}$ $2^{-2}$ $2^{-3}$ $2^{-4}$ $2^{-5}$ $2^{-6}$ $2^{-7}$ $2^{-8}$ $2^{-9}$ $2^{-10}$ $2^{-11}$ $2^{-12}$ $2^{-13}$ $2^{-14}$ $2^{-15}$ $2^{-16}$ |

### Unsigned Integer Input

| $X_{IN}$  | $Y_{IN}$  |
|---|---|
| 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0   | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0   |
| $2^{15}$ $2^{14}$ $2^{13}$ $2^{12}$ $2^{11}$ $2^{10}$ $2^9$ $2^8$ $2^7$ $2^6$ $2^5$ $2^4$ $2^3$ $2^2$ $2^1$ $2^0$ | $2^{15}$ $2^{14}$ $2^{13}$ $2^{12}$ $2^{11}$ $2^{10}$ $2^9$ $2^8$ $2^7$ $2^6$ $2^5$ $2^4$ $2^3$ $2^2$ $2^1$ $2^0$ |

## CY7C510

### Output Formats

#### Two's Complement Fractional Output

| $X_{TP}$                    | $MSP$   | $LSP$   |
|-----------------------------|---|---|
| 34 33 32                    | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16   | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0   |
| $-2^{34}$ $2^{33}$ $2^{32}$ | $2^{31}$ $2^{30}$ $2^{29}$ $2^{28}$ $2^{27}$ $2^{26}$ $2^{25}$ $2^{24}$ $2^{23}$ $2^{22}$ $2^{21}$ $2^{20}$ $2^{19}$ $2^{18}$ $2^{17}$ $2^{16}$ | $2^{15}$ $2^{14}$ $2^{13}$ $2^{12}$ $2^{11}$ $2^{10}$ $2^9$ $2^8$ $2^7$ $2^6$ $2^5$ $2^4$ $2^3$ $2^2$ $2^1$ $2^0$ |
| (Sign)                      |   |   |

#### Two's Complement Integer Output

| $X_{TP}$                    | $MSP$   | $LSP$   |
|-----------------------------|---|---|
| 34 33 32                    | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16   | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0   |
| $-2^{34}$ $2^{33}$ $2^{32}$ | $2^{31}$ $2^{30}$ $2^{29}$ $2^{28}$ $2^{27}$ $2^{26}$ $2^{25}$ $2^{24}$ $2^{23}$ $2^{22}$ $2^{21}$ $2^{20}$ $2^{19}$ $2^{18}$ $2^{17}$ $2^{16}$ | $2^{15}$ $2^{14}$ $2^{13}$ $2^{12}$ $2^{11}$ $2^{10}$ $2^9$ $2^8$ $2^7$ $2^6$ $2^5$ $2^4$ $2^3$ $2^2$ $2^1$ $2^0$ |
| (Sign)                      |   |   |

#### Unsigned Fractional Output

| $X_{TP}$                | $MSP$  | $LSP$   |
|-------------------------|--|---|
| 34 33 32                | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16  | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0   |
| $2^{22}$ $2^{21}$ $2^0$ | $2^{-1}$ $2^{-2}$ $2^{-3}$ $2^{-4}$ $2^{-5}$ $2^{-6}$ $2^{-7}$ $2^{-8}$ $2^{-9}$ $2^{-10}$ $2^{-11}$ $2^{-12}$ $2^{-13}$ $2^{-14}$ $2^{-15}$ $2^{-16}$ | $2^{-17}$ $2^{-18}$ $2^{-19}$ $2^{-20}$ $2^{-21}$ $2^{-22}$ $2^{-23}$ $2^{-24}$ $2^{-25}$ $2^{-26}$ $2^{-27}$ $2^{-28}$ $2^{-29}$ $2^{-30}$ $2^{-31}$ $2^{-32}$ |

#### Unsigned Integer Output

| $X_{TP}$                   | $MSP$   | $LSP$   |
|----------------------------|---|---|
| 34 33 32                   | 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16   | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0   |
| $2^{34}$ $2^{33}$ $2^{32}$ | $2^{31}$ $2^{30}$ $2^{29}$ $2^{28}$ $2^{27}$ $2^{26}$ $2^{25}$ $2^{24}$ $2^{23}$ $2^{22}$ $2^{21}$ $2^{20}$ $2^{19}$ $2^{18}$ $2^{17}$ $2^{16}$ | $2^{15}$ $2^{14}$ $2^{13}$ $2^{12}$ $2^{11}$ $2^{10}$ $2^9$ $2^8$ $2^7$ $2^6$ $2^5$ $2^4$ $2^3$ $2^2$ $2^1$ $2^0$ |



### Electrical Characteristics Over Operating Range<sup>[4]</sup>

| Parameters                            | Description                       | Test Conditions   | Min.  | Max. | Units |
|---------------------------------------|-----------------------------------|---|---|------|-------|
| V <sub>OH</sub>                       | Output HIGH Voltage               | V <sub>CC</sub> = Min., I <sub>OH</sub> = -0.4 mA   | 2.4   |      | V     |
| V <sub>OL</sub>                       | Output LOW Voltage                | V <sub>CC</sub> = Min., I <sub>OL</sub> = 4.0 mA  |   | 0.4  | V     |
| V <sub>IH</sub>                       | Input HIGH Voltage                |   | 2.0   |      | V     |
| V <sub>IL</sub>                       | Input LOW Voltage                 |   |   | 0.8  | V     |
| I <sub>OH</sub>                       | Output HIGH Current               | V <sub>CC</sub> = Min., V <sub>OH</sub> = 2.4V  | -0.4  |      | mA    |
| I <sub>OL</sub>                       | Output LOW Current                | V <sub>CC</sub> = Min., V <sub>OL</sub> = 0.4V  | 4.0   |      | mA    |
| I <sub>IX</sub>                       | Input Leakage Current             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>  | -10   | +10  | μA    |
| I <sub>I</sub>                        | Input Current, Max. Input Voltage | V <sub>CC</sub> = Max., V <sub>IN</sub> = 7.0V  |   | 10   | mA    |
| I <sub>OS</sub> <sup>[1]</sup>        | Output Short Circuit Current      | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V   | -3  | -30  | mA    |
| I <sub>OZL</sub>                      | Output OFF (Hi-Z) Current         | V <sub>CC</sub> = Max., $\overline{OE}$ = 2.0V  |   | -25  | μA    |
| I <sub>OZH</sub>                      | Output OFF (Hi-Z) Current         | V <sub>CC</sub> = Max., $\overline{OE}$ = 2.0V  | 25  |      | μA    |
| I <sub>CC</sub> (Q1) <sup>[2]</sup>   | Supply Current (Quiescent)        | V <sub>CC</sub> = Max.,<br>V <sub>IN</sub> = [GND to V <sub>IL</sub> ] or [V <sub>IH</sub> to V <sub>CC</sub> ] |   | 30   | mA    |
| I <sub>CC</sub> (Q2) <sup>[2]</sup>   | Supply Current (Quiescent)        | V <sub>CC</sub> = Max<br>V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ 3.85V<br>0.4V ≥ V <sub>IN</sub> ≥ GND              | Commercial  | 20   | mA    |
|                                       |                                   |   | Military  | 25   |       |
| I <sub>CC</sub> (Max.) <sup>[2]</sup> | Supply Current                    | Commercial<br>Military  | V <sub>CC</sub> = Max., f <sub>CLK</sub> = 10 MHz | 100  | mA    |
|                                       |                                   |   |   | 110  |       |

### Capacitance<sup>[3]</sup>

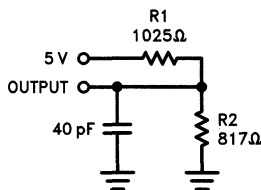
| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 8    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 10   |       |

**Notes:**

- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
- For I<sub>CC</sub> measurements, the outputs are three-stated. Two quiescent figures are given for different input voltage ranges. To calculate I<sub>CC</sub> at any given clock frequency, use 30 mA + I<sub>CC</sub> (A.C.), where I<sub>CC</sub> (A.C.) = (7 mA/MHz) × Clock Frequency for the Commercial temperature range. I<sub>CC</sub> (A.C.) = (8 mA/MHz) × Clock Frequency for Military temperature range.
- Tested initially and after any design or process changes that may affect these parameters.
- See the last page of this specification for Group A subgroup testing information.

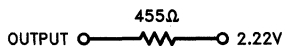
### Output Loads Used for A.C. Performance Characteristics

#### Normal Load (Load 1)



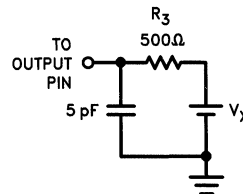
0057-4

Equivalent to: THÉVENIN EQUIVALENT



0057-6

#### Three-State Delay Load (Load 2)



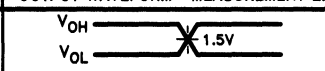
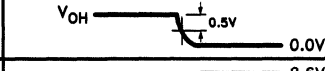
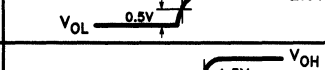
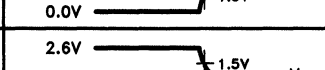

0057-5

Switching Characteristics Over Operating Range<sup>[3]</sup>

| Parameters       | Description   | 7C510-45  |      | 7C510-55 |      | 7C510-65 |      | 7C510-75 |      | Units |
|------------------|---|-----------|------|----------|------|----------|------|----------|------|-------|
|                  |   | Min.      | Max. | Min.     | Max. | Min.     | Max. | Min.     | Max. |       |
| t <sub>MA</sub>  | Multiply Accumulate Time  |           | 45   |          | 55   |          | 65   |          | 75   | ns    |
| t <sub>S</sub>   | Setup Time  | 20        |      | 20       |      | 25       |      | 25       |      | ns    |
| t <sub>H</sub>   | Hold Time   | 3         |      | 3        |      | 3        |      | 3        |      | ns    |
| t <sub>PW</sub>  | Clock Pulse Width   | 25        |      | 25       |      | 30       |      | 30       |      | ns    |
| t <sub>PDP</sub> | Output Clock to P   |           | 30   |          | 30   |          | 35   |          | 35   | ns    |
| t <sub>PDY</sub> | Output Clock to Y   |           | 30   |          | 30   |          | 35   |          | 35   | ns    |
| t <sub>PHZ</sub> | OE $\bar{X}$ , OE $\bar{M}$ to P;<br>OE $\bar{L}$ to Y (Disable Time) | HIGH to Z | 25   | 25       | 30   | 30       |      |          |      | ns    |
| t <sub>PLZ</sub> | OE $\bar{L}$ to Y (Enable Time)                                       | LOW to Z  | 25   | 25       | 30   | 30       |      |          |      | ns    |
| t <sub>PZH</sub> | OE $\bar{X}$ , OE $\bar{M}$ to P;<br>OE $\bar{L}$ to Y (Enable Time)  | Z to HIGH | 30   | 30       | 35   | 35       |      |          |      | ns    |
| t <sub>PZL</sub> | OE $\bar{L}$ to Y (Enable Time)                                       | Z to LOW  | 30   | 30       | 35   | 35       |      |          |      | ns    |
| t <sub>HCL</sub> | Relative Hold Time  | 0         |      | 0        |      | 0        |      |          |      | ns    |

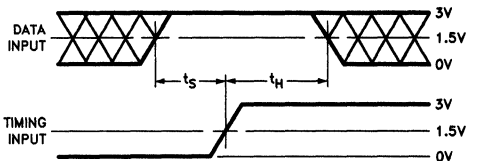
5

Test Waveforms

| TEST                   | V <sub>X</sub>  | OUTPUT WAVEFORM - MEASUREMENT LEVEL   |
|------------------------|-----------------|---|
| ALL t <sub>pd</sub> 's | V <sub>CC</sub> |    |
| t <sub>PHZ</sub>       | 0.0V            |    |
| t <sub>PLZ</sub>       | 2.6V            |    |
| t <sub>PZH</sub>       | 0.0V            |   |
| t <sub>PZL</sub>       | 2.6V            |  |

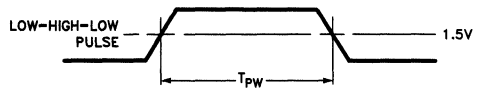
0057-7

Setup and Hold Time



0057-8

Pulse Width



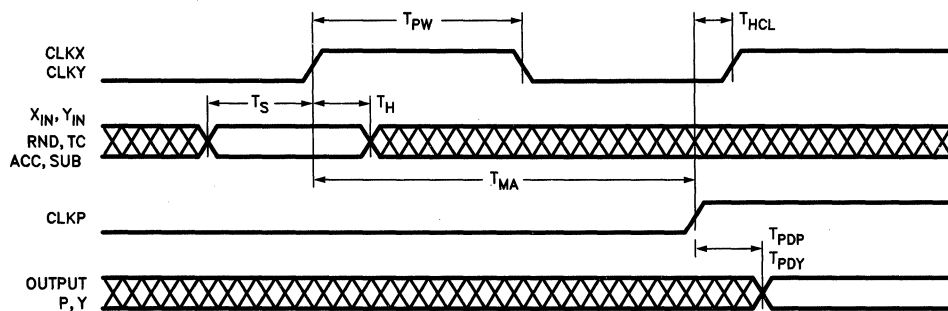
0057-9

Notes:

1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

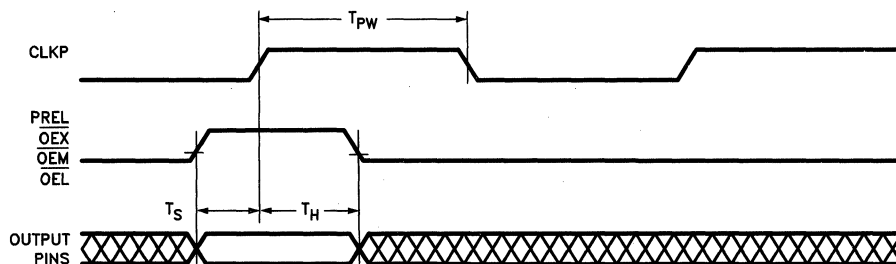
3. See the last page of this specification for Group A subgroup testing information.

### CY7C510 Timing Diagram



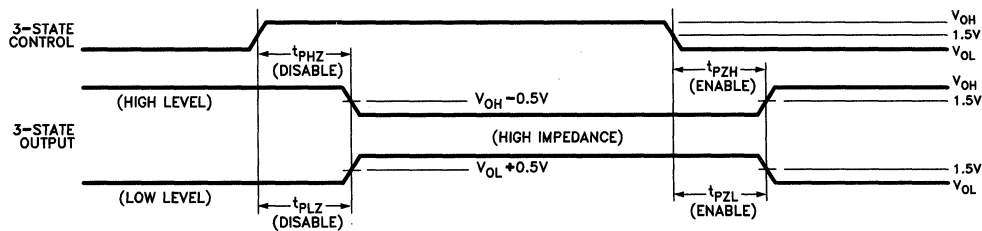
0057-10

### Preload Timing Diagram



0057-11

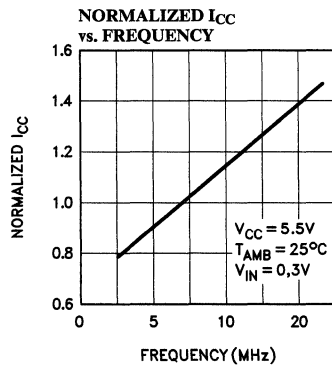
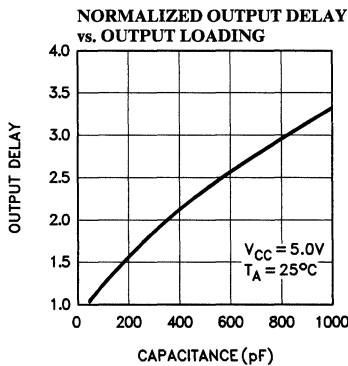
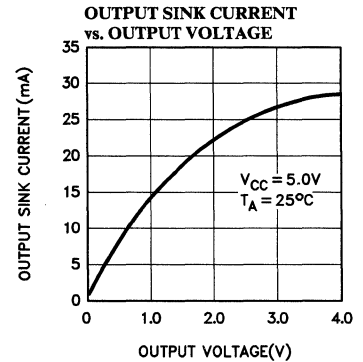
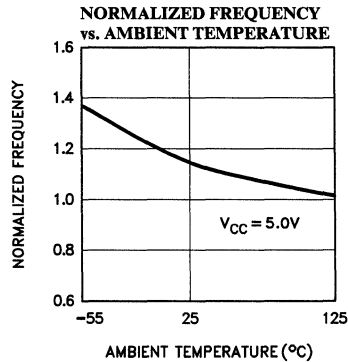
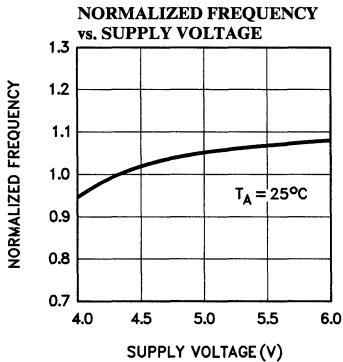
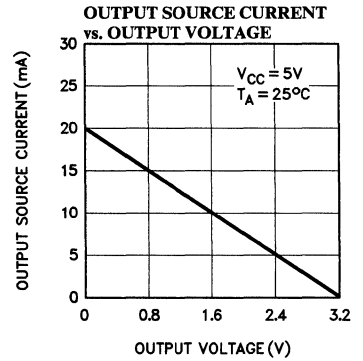
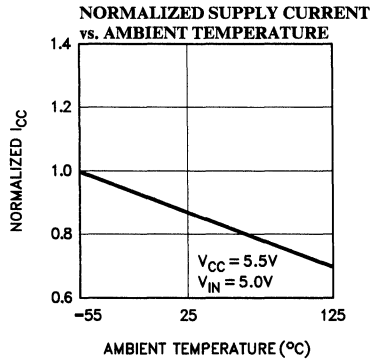
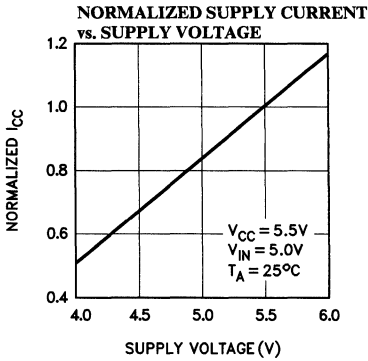
### Three-State Timing Diagram



0057-12

Typical AC and DC Characteristics

5



**Ordering Information**

| Speed (ns)     | Ordering Code  | Package Type | Operating Range |
|----------------|----------------|--------------|-----------------|
| 45             | CY7C510-45 PC  | P29          | Commercial      |
|                | CY7C510-45 LC  | L81          |                 |
|                | CY7C510-45 JC  | J81          |                 |
|                | CY7C510-45 DC  | D30          |                 |
|                | CY7C510-45 GC  | G68          |                 |
| 55             | CY7C510-55 PC  | P29          | Commercial      |
|                | CY7C510-55 LC  | L81          |                 |
|                | CY7C510-55 JC  | J81          |                 |
|                | CY7C510-55 DC  | D30          |                 |
|                | CY7C510-55 GC  | G68          |                 |
|                | CY7C510-55 LMB | L81          | Military        |
|                | CY7C510-55 DMB | D30          |                 |
| CY7C510-55 GMB | G68            |              |                 |
| 65             | CY7C510-65 PC  | P29          | Commercial      |
|                | CY7C510-65 LC  | L81          |                 |
|                | CY7C510-65 JC  | J81          |                 |
|                | CY7C510-65 DC  | D30          |                 |
|                | CY7C510-65 GC  | G68          |                 |
|                | CY7C510-65 LMB | L81          | Military        |
|                | CY7C510-65 DMB | D30          |                 |
| CY7C510-65 GMB | G68            |              |                 |
| 75             | CY7C510-75 PC  | P29          | Commercial      |
|                | CY7C510-75 LC  | L81          |                 |
|                | CY7C510-75 JC  | J81          |                 |
|                | CY7C510-75 DC  | D30          |                 |
|                | CY7C510-75 GC  | G68          |                 |
|                | CY7C510-75 LMB | L81          | Military        |
|                | CY7C510-75 DMB | D30          |                 |
| CY7C510-75 GMB | G68            |              |                 |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters       | Subgroups |
|------------------|-----------|
| V <sub>OH</sub>  | 1,2,3     |
| V <sub>OL</sub>  | 1,2,3     |
| V <sub>IH</sub>  | 1,2,3     |
| V <sub>IL</sub>  | 1,2,3     |
| I <sub>OH</sub>  | 1,2,3     |
| I <sub>OL</sub>  | 1,2,3     |
| I <sub>IX</sub>  | 1,2,3     |
| I <sub>I</sub>   | 1,2,3     |
| I <sub>OS</sub>  | 1,2,3     |
| I <sub>OZL</sub> | 1,2,3     |
| I <sub>OZH</sub> | 1,2,3     |

| Parameters             | Subgroups |
|------------------------|-----------|
| I <sub>CC (Q1)</sub>   | 1,2,3     |
| I <sub>CC (Q2)</sub>   | 1,2,3     |
| I <sub>CC (Max.)</sub> | 1,2,3     |

**5**
**Switching Characteristics**

| Parameters       | Subgroups   |
|------------------|-------------|
| t <sub>MA</sub>  | 7,8,9,10,11 |
| t <sub>S</sub>   | 7,8,9,10,11 |
| t <sub>H</sub>   | 7,8,9,10,11 |
| t <sub>PW</sub>  | 7,8,9,10,11 |
| t <sub>PDP</sub> | 7,8,9,10,11 |
| t <sub>PDY</sub> | 7,8,9,10,11 |
| t <sub>PHZ</sub> | 7,8,9,10,11 |
| t <sub>PLZ</sub> | 7,8,9,10,11 |
| t <sub>PZH</sub> | 7,8,9,10,11 |
| t <sub>PZL</sub> | 7,8,9,10,11 |
| t <sub>HCL</sub> | 7,8,9,10,11 |

Document #: 38-00014-B



**Features**

- **Fast**
  - 38 ns clock cycle (commercial)
  - 42 ns clock cycle (military)
- **Low Power**
  - I<sub>CC</sub> (max. at 10 MHz) = 100 mA (commercial)
  - I<sub>CC</sub> (max. at 10 MHz) = 110 mA (military)
- **V<sub>CC</sub> Margin**
  - 5V ± 10%
  - All parameters guaranteed over commercial and military operating temperature range
- **16 x 16 bit parallel multiplication with full precision 32-bit product output**

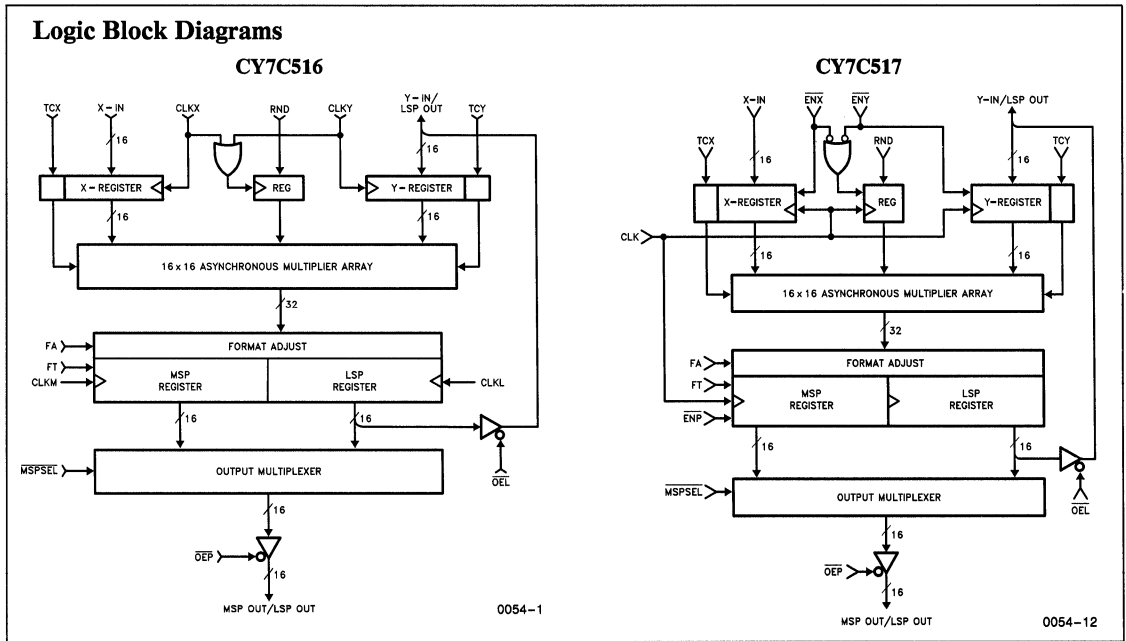
- **Two's complement, unsigned magnitude, or mixed mode multiplication**
- **CY7C516 pin compatible and functionally equivalent to Am29516, MPY016K, MPY016H**
- **CY7C517 pin compatible and functionally equivalent to Am29517**

as either two's complement or unsigned magnitude numbers. Controls are provided for rounding and format adjustment of the full precision 32-bit product.

On the 7C516, individually clocked input and output registers are provided to maximize throughput and to simplify bus interfacing. On the 7C517, a single clock (CLK) is provided, along with three register enables. This facilitates the use of the 7C517 in microprogrammed systems. The input and output registers are positive edge triggered D-type flip-flops. The output register may be made transparent for asynchronous output.

**Functional Description**

The CY7C516/517 are high-speed 16 x 16 parallel multipliers which operate at 38 ns clocked multiply times (26 MHz multiplication rate). The two input operands may be independently specified



**Selection Guide**

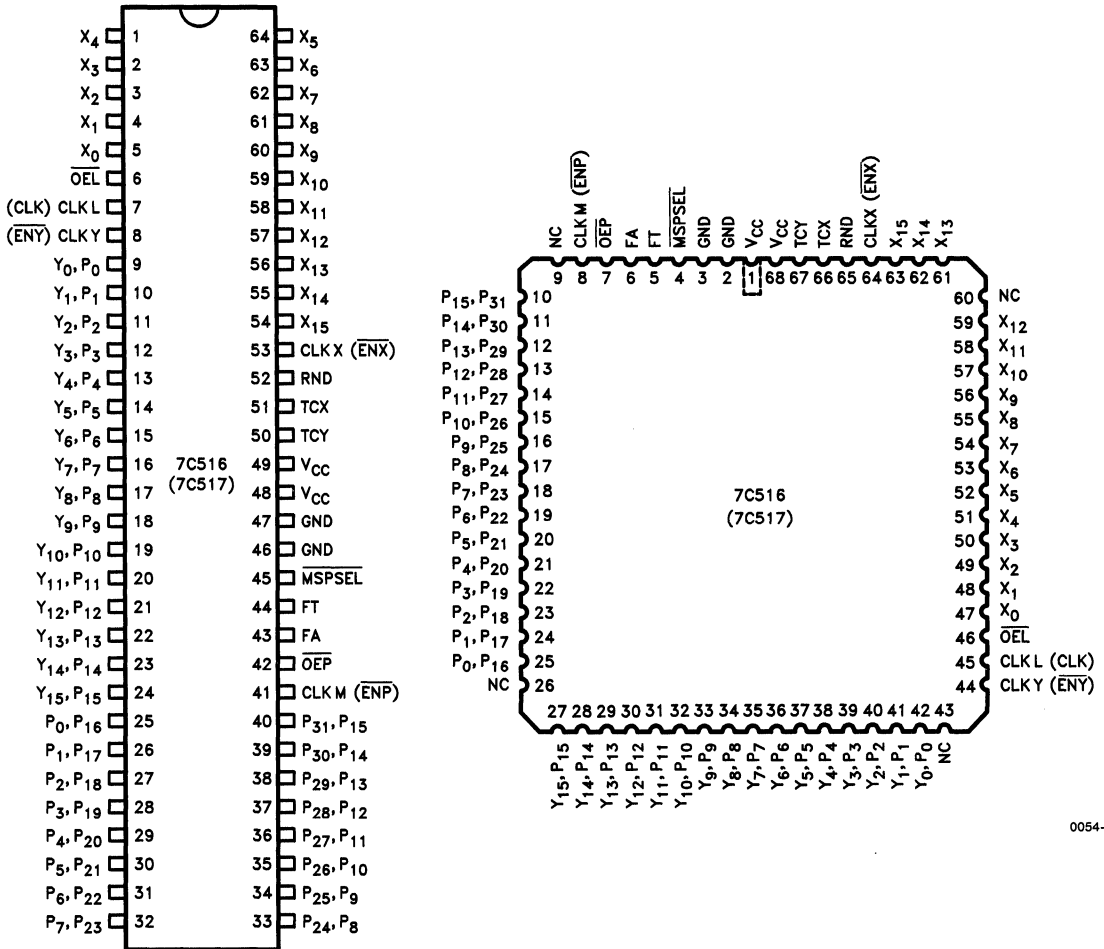
|  |            | <b>7C516-38</b><br><b>7C517-38</b> | <b>7C516-42</b><br><b>7C517-42</b> | <b>7C516-45</b><br><b>7C517-45</b> | <b>7C516-55</b><br><b>7C517-55</b> | <b>7C516-75</b><br><b>7C517-75</b> |
|--|------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|
| Maximum Multiply Time (ns)<br>Clocked/Unlocked | Commercial | 38/58                              |                                    | 45/65                              | 55/75                              | 75/100                             |
|  | Military   |                                    | 42/65                              |                                    | 55/75                              | 75/100                             |

## Functional Description (Continued)

Two output modes may be selected by using the output multiplexer control, **MSPSEL**. Holding **MSPSEL** LOW causes the most significant product (**MSP**) to be available at the dedicated output port. The **LSP** is simultaneously available at the bidirectional port shared with the **Y**-inputs.

The other mode of output involves toggling of the **MSPSEL** control, allowing both the **MSP** and **LSP** to be available for output through the dedicated 16-bit output port.

## Pin Configurations



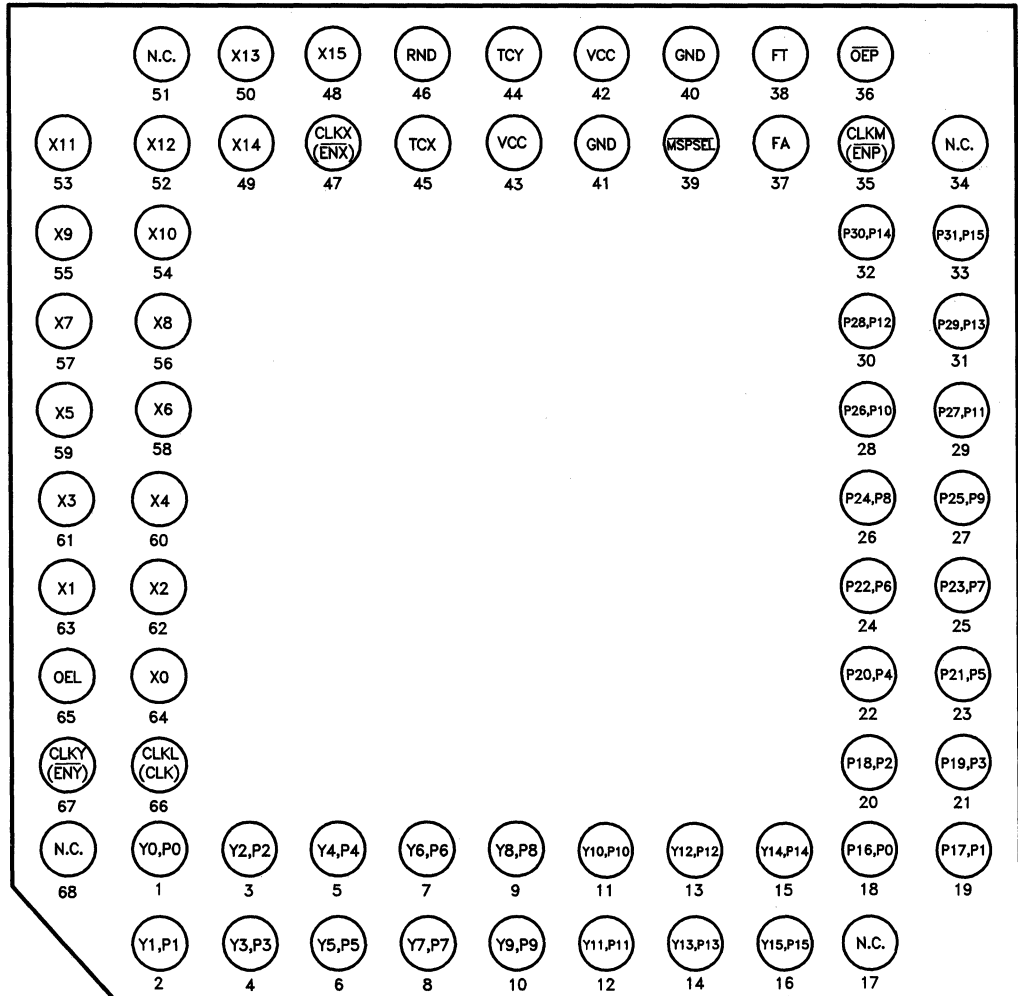
0054-2

0054-3



Pin Configurations (Continued)

Pin Configuration for 68-Pin Grid Array



0054-16

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|  |  |
|--|--|
| Ambient Temperature Under Bias . . . .       | -55°C to +125°C                          |
| Supply Voltage to Ground Potential . . . .   | -0.5V to +7.0V                           |
| DC Input Voltage . . . . .                   | -0.5V to +7.0V                           |
| DC Voltage Applied to Outputs . . . . .      | -0.5V to V <sub>CC</sub> Max.            |
| Output Current, into Outputs (low) . . . . . | 10 mA                                    |
| Static Discharge Voltage . . . . .           | > 1000V<br>(per MIL-STD-883 Method 3015) |

## Pin Definitions

| Signal Name                                | I/O | Description   |
|--|-----|---|
| X <sub>15-0</sub>                          | I   | <b>X-Input Data.</b> This 16-bit number may be interpreted as two's complement or unsigned magnitude.   |
| Y <sub>15-0</sub><br>(P <sub>15-0</sub> )  | I/O | <b>Y-Input/LSP Output Data.</b> This 16-bit number may be interpreted as two's complement or unsigned magnitude. The Y-input port may be multiplexed with the LSP output (P <sub>15-0</sub> ).  |
| P <sub>31-16</sub><br>(P <sub>15-0</sub> ) | O   | <b>Output Data.</b> This 16-bit port may carry either the MSP (P <sub>31-16</sub> ) or the LSP (P <sub>15-0</sub> ).  |
| FT   | I   | The MSP and LSP registers are made transparent (asynchronous operation) if FT is HIGH.  |
| FA   | I   | <b>Format Adjust Control.</b> If FA is HIGH, a full 32-bit product is output. If FA is LOW, a left-shifted product is output, with the sign bit replicated in the LSP. FA must be HIGH for two's complement integer, unsigned magnitude, and mixed mode multiplication.                                       |
| $\overline{\text{MSPSEL}}$                 | I   | <b>Output Multiplexer Control.</b> When $\overline{\text{MSPSEL}}$ is LOW, the MSP is available for output at the MSP output port, and the LSP is available at the Y-input/LSP output port. When $\overline{\text{MSPSEL}}$ is HIGH, the LSP is available at both ports (above) and the MSP is not available. |
| RND  | I   | <b>Round Control.</b> When RND is HIGH, a one is added to the MSB of the LSP. This position is dependent on the FA control; FA = HIGH means RND adds to the 2 <sup>-15</sup> bit (P <sub>15</sub> ), FA = LOW means RND adds to the 2 <sup>-16</sup> bit (P <sub>14</sub> ).                                  |
| TCX  | I   | <b>Two's Complement Control X.</b> X-input data are interpreted as two's complement when TCX is HIGH. TCX LOW means the data are interpreted as unsigned magnitude.   |

## Operating Range

| Range       | Temperature     | V <sub>CC</sub> |
|-------------|-----------------|-----------------|
| Commercial  | 0°C to +70°C    | 5V ± 10%        |
| Military[1] | -55°C to +125°C | 5V ± 10%        |

Note:

1. T<sub>A</sub> is the "instant on" case temperature.

| Signal Name             | I/O | Description  |
|-------------------------|-----|--|
| TCY                     | I   | <b>Two's Complement Control Y.</b> Y-Input data are interpreted as two's complement when TCY is HIGH. TCY LOW means the data are interpreted as unsigned magnitude.  |
| $\overline{\text{OEP}}$ | I   | <b>P<sub>31-16</sub>/P<sub>15-0</sub> Output Port Three-State Control.</b> When $\overline{\text{OEP}}$ is LOW, the output port is enabled; when $\overline{\text{OEP}}$ is HIGH, the drivers are in a high impedance state.                                     |
| $\overline{\text{OEL}}$ | I   | <b>Y-in/P<sub>15-0</sub> Port Three State Control.</b> When $\overline{\text{OEL}}$ is LOW, the timeshared port is enabled for LSP output. When $\overline{\text{OEL}}$ is HIGH, the output drivers are in a high impedance state. This is required for Y-input. |
| <b>CY7C516 Only</b>     |     |  |
| CLKX                    | I   | <b>X-Register Clock.</b> X-input data and TCX are latched in at the rising edge of CLKX.   |
| CLKY                    | I   | <b>Y-Register Clock.</b> Y-input data and TCY are latched in at the rising edge of CLKY.   |
| CLKM                    | I   | <b>MSP Register Clock.</b> The most significant product (MSP) is latched in at the MSP Register at the rising edge of CLKM.  |
| CLKL                    | I   | <b>LSP Register Clock.</b> The least significant product (LSP) is latched in at the LSP Register at the rising edge of CLKL.   |
| <b>CY7C517 Only</b>     |     |  |
| CLK                     | I   | <b>Clock.</b> All enabled registers latch in their data at the rising edge of CLK.   |
| $\overline{\text{ENX}}$ | I   | <b>X-Register Enable.</b> When $\overline{\text{ENX}}$ is LOW, the X-Register is enabled. X-input data and TCX will be latched in at the rising edge of CLK when the register is enabled. When $\overline{\text{ENX}}$ is HIGH, the X-Register is in hold mode.  |
| $\overline{\text{ENY}}$ | I   | <b>X-Register Enable.</b> $\overline{\text{ENY}}$ enables the Y-Register. (See $\overline{\text{ENX}}$ .)  |
| $\overline{\text{ENP}}$ | I   | <b>Product Register Enable.</b> $\overline{\text{ENP}}$ enables the product register. Both the MSP and LSP Sections are enabled by $\overline{\text{ENP}}$ . (See $\overline{\text{ENX}}$ .)   |

## Input Formats (All Devices)

### Fractional Two's Complement Input Format

TCX, TCY = 1

| $X_{IN}$ |          |          |          |          |          |          |          |          |          |           |           |           |           |           |           | $Y_{IN}$ |          |          |          |          |          |          |          |          |          |           |           |           |           |           |           |
|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 15       | 14       | 13       | 12       | 11       | 10       | 9        | 8        | 7        | 6        | 5         | 4         | 3         | 2         | 1         | 0         | 15       | 14       | 13       | 12       | 11       | 10       | 9        | 8        | 7        | 6        | 5         | 4         | 3         | 2         | 1         | 0         |
| $-2^0$   | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-7}$ | $2^{-8}$ | $2^{-9}$ | $2^{-10}$ | $2^{-11}$ | $2^{-12}$ | $2^{-13}$ | $2^{-14}$ | $2^{-15}$ | $-2^0$   | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-7}$ | $2^{-8}$ | $2^{-9}$ | $2^{-10}$ | $2^{-11}$ | $2^{-12}$ | $2^{-13}$ | $2^{-14}$ | $2^{-15}$ |
| (Sign)   |          |          |          |          |          |          |          |          |          |           |           |           |           |           |           | (Sign)   |          |          |          |          |          |          |          |          |          |           |           |           |           |           |           |

### Integer Two's Complement Input Format

TCX, TCY = 1

| $X_{IN}$  |          |          |          |          |          |       |       |       |       |       |       |       |       |       |       | $Y_{IN}$  |          |          |          |          |          |       |       |       |       |       |       |       |       |       |       |
|-----------|----------|----------|----------|----------|----------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|----------|----------|----------|----------|----------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 15        | 14       | 13       | 12       | 11       | 10       | 9     | 8     | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 15        | 14       | 13       | 12       | 11       | 10       | 9     | 8     | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
| $-2^{15}$ | $2^{14}$ | $2^{13}$ | $2^{12}$ | $2^{11}$ | $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ | $-2^{15}$ | $2^{14}$ | $2^{13}$ | $2^{12}$ | $2^{11}$ | $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
| (Sign)    |          |          |          |          |          |       |       |       |       |       |       |       |       |       |       | (Sign)    |          |          |          |          |          |       |       |       |       |       |       |       |       |       |       |

### Unsigned Fractional Input Format

TCX, TCY = 0

| $X_{IN}$ |          |          |          |          |          |          |          |          |           |           |           |           |           |           |           | $Y_{IN}$ |          |          |          |          |          |          |          |          |           |           |           |           |           |           |           |
|----------|----------|----------|----------|----------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 15       | 14       | 13       | 12       | 11       | 10       | 9        | 8        | 7        | 6         | 5         | 4         | 3         | 2         | 1         | 0         | 15       | 14       | 13       | 12       | 11       | 10       | 9        | 8        | 7        | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
| $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-7}$ | $2^{-8}$ | $2^{-9}$ | $2^{-10}$ | $2^{-11}$ | $2^{-12}$ | $2^{-13}$ | $2^{-14}$ | $2^{-15}$ | $2^{-16}$ | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-7}$ | $2^{-8}$ | $2^{-9}$ | $2^{-10}$ | $2^{-11}$ | $2^{-12}$ | $2^{-13}$ | $2^{-14}$ | $2^{-15}$ | $2^{-16}$ |

### Unsigned Integer Input Format

TCX, TCY = 0

| $X_{IN}$ |          |          |          |          |          |       |       |       |       |       |       |       |       |       |       | $Y_{IN}$ |          |          |          |          |          |       |       |       |       |       |       |       |       |       |       |
|----------|----------|----------|----------|----------|----------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|----------|----------|----------|----------|----------|----------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 15       | 14       | 13       | 12       | 11       | 10       | 9     | 8     | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     | 15       | 14       | 13       | 12       | 11       | 10       | 9     | 8     | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
| $2^{15}$ | $2^{14}$ | $2^{13}$ | $2^{12}$ | $2^{11}$ | $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ | $2^{15}$ | $2^{14}$ | $2^{13}$ | $2^{12}$ | $2^{11}$ | $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |

**Output Formats (All Devices)**
**Fractional Two's Complement (Shifted)\* Format**

FA = 0

| MSP  | LSP   |
|--|---|
| 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16<br>-2 <sup>0</sup> 2 <sup>-1</sup> 2 <sup>-2</sup> 2 <sup>-3</sup> 2 <sup>-4</sup> 2 <sup>-5</sup> 2 <sup>-6</sup> 2 <sup>-7</sup> 2 <sup>-8</sup> 2 <sup>-9</sup> 2 <sup>-10</sup> 2 <sup>-11</sup> 2 <sup>-12</sup> 2 <sup>-13</sup> 2 <sup>-14</sup> 2 <sup>-15</sup> | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0<br>-2 <sup>0</sup> 2 <sup>-16</sup> 2 <sup>-17</sup> 2 <sup>-18</sup> 2 <sup>-19</sup> 2 <sup>-20</sup> 2 <sup>-21</sup> 2 <sup>-22</sup> 2 <sup>-23</sup> 2 <sup>-24</sup> 2 <sup>-25</sup> 2 <sup>-26</sup> 2 <sup>-27</sup> 2 <sup>-28</sup> 2 <sup>-29</sup> 2 <sup>-30</sup> |
| (Sign)   | (Sign)  |

**Fractional Two's Complement Output**

FA = 1

| MSP  | LSP  |
|--|--|
| 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16<br>-2 <sup>1</sup> 2 <sup>0</sup> 2 <sup>-1</sup> 2 <sup>-2</sup> 2 <sup>-3</sup> 2 <sup>-4</sup> 2 <sup>-5</sup> 2 <sup>-6</sup> 2 <sup>-7</sup> 2 <sup>-8</sup> 2 <sup>-9</sup> 2 <sup>-10</sup> 2 <sup>-11</sup> 2 <sup>-12</sup> 2 <sup>-13</sup> 2 <sup>-14</sup> | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0<br>2 <sup>-15</sup> 2 <sup>-16</sup> 2 <sup>-17</sup> 2 <sup>-18</sup> 2 <sup>-19</sup> 2 <sup>-20</sup> 2 <sup>-21</sup> 2 <sup>-22</sup> 2 <sup>-23</sup> 2 <sup>-24</sup> 2 <sup>-25</sup> 2 <sup>-26</sup> 2 <sup>-27</sup> 2 <sup>-28</sup> 2 <sup>-29</sup> 2 <sup>-30</sup> |
| (Sign)   |  |

**Integer Two's Complement Output**

FA = 1

| MSP   | LSP  |
|---|--|
| 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16<br>-2 <sup>31</sup> 2 <sup>30</sup> 2 <sup>29</sup> 2 <sup>28</sup> 2 <sup>27</sup> 2 <sup>26</sup> 2 <sup>25</sup> 2 <sup>24</sup> 2 <sup>23</sup> 2 <sup>22</sup> 2 <sup>21</sup> 2 <sup>20</sup> 2 <sup>19</sup> 2 <sup>18</sup> 2 <sup>17</sup> 2 <sup>16</sup> | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0<br>2 <sup>15</sup> 2 <sup>14</sup> 2 <sup>13</sup> 2 <sup>12</sup> 2 <sup>11</sup> 2 <sup>10</sup> 2 <sup>9</sup> 2 <sup>8</sup> 2 <sup>7</sup> 2 <sup>6</sup> 2 <sup>5</sup> 2 <sup>4</sup> 2 <sup>3</sup> 2 <sup>2</sup> 2 <sup>1</sup> 2 <sup>0</sup> |
| (Sign)  |  |

**Unsigned Fractional Output**

FA = 1

| MSP   | LSP  |
|---|--|
| 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16<br>2 <sup>-1</sup> 2 <sup>-2</sup> 2 <sup>-3</sup> 2 <sup>-4</sup> 2 <sup>-5</sup> 2 <sup>-6</sup> 2 <sup>-7</sup> 2 <sup>-8</sup> 2 <sup>-9</sup> 2 <sup>-10</sup> 2 <sup>-11</sup> 2 <sup>-12</sup> 2 <sup>-13</sup> 2 <sup>-14</sup> 2 <sup>-15</sup> 2 <sup>-16</sup> | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0<br>2 <sup>-17</sup> 2 <sup>-18</sup> 2 <sup>-19</sup> 2 <sup>-20</sup> 2 <sup>-21</sup> 2 <sup>-22</sup> 2 <sup>-23</sup> 2 <sup>-24</sup> 2 <sup>-25</sup> 2 <sup>-26</sup> 2 <sup>-27</sup> 2 <sup>-28</sup> 2 <sup>-29</sup> 2 <sup>-30</sup> 2 <sup>-31</sup> 2 <sup>-32</sup> |

**Unsigned Integer Output**

FA = 1

| MSP  | LSP  |
|--|--|
| 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16<br>2 <sup>31</sup> 2 <sup>30</sup> 2 <sup>29</sup> 2 <sup>28</sup> 2 <sup>27</sup> 2 <sup>26</sup> 2 <sup>25</sup> 2 <sup>24</sup> 2 <sup>23</sup> 2 <sup>22</sup> 2 <sup>21</sup> 2 <sup>20</sup> 2 <sup>19</sup> 2 <sup>18</sup> 2 <sup>17</sup> 2 <sup>16</sup> | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0<br>2 <sup>15</sup> 2 <sup>14</sup> 2 <sup>13</sup> 2 <sup>12</sup> 2 <sup>11</sup> 2 <sup>10</sup> 2 <sup>9</sup> 2 <sup>8</sup> 2 <sup>7</sup> 2 <sup>6</sup> 2 <sup>5</sup> 2 <sup>4</sup> 2 <sup>3</sup> 2 <sup>2</sup> 2 <sup>1</sup> 2 <sup>0</sup> |

\*In this format an overflow occurs in the attempted multiplication of the two's complement number 1.000...(-1) with itself, yielding a product of 1.000... or -1.

### Electrical Characteristics Over Operating Range<sup>[4]</sup>

| Parameters                                       | Description                  | Test Conditions  | Min.  | Max. | Units |    |
|--|------------------------------|--|---|------|-------|----|
| V <sub>OH</sub>                                  | Output HIGH Voltage          | V <sub>CC</sub> = Min., I <sub>OH</sub> = -0.4 mA                            | 2.4   |      | V     |    |
| V <sub>OL</sub>                                  | Output LOW Voltage           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 4.0 mA                             |   | 0.4  | V     |    |
| V <sub>IH</sub>                                  | Input HIGH Voltage           |  | 2.0   |      | V     |    |
| V <sub>IL</sub>                                  | Input LOW Voltage            |  |   | 0.8  | V     |    |
| I <sub>OH</sub>                                  | Output HIGH Current          | V <sub>CC</sub> = Min., V <sub>OH</sub> = 2.4V                               | -0.4  |      | mA    |    |
| I <sub>OL</sub>                                  | Output LOW Current           | V <sub>CC</sub> = Min., V <sub>OL</sub> = 0.4V                               | 4.0   |      | mA    |    |
| I <sub>IX</sub>                                  | Input Leakage Current        | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> , V <sub>CC</sub> = Max. | -10   | 10   | μA    |    |
| I <sub>OS</sub> <sup>[1]</sup>                   | Output Short Circuit Current | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0V                                | -3  | -30  | mA    |    |
| I <sub>OZL</sub>                                 | Output OFF (Hi-Z) Current    | V <sub>CC</sub> = Max., $\overline{OE}$ = 2.0V                               |   | -25  | μA    |    |
| I <sub>OZH</sub>                                 | Output OFF (Hi-Z) Current    | V <sub>CC</sub> = Max., $\overline{OE}$ = 2.0V                               | 25  |      | μA    |    |
| I <sub>CC</sub> (Q <sub>1</sub> ) <sup>[2]</sup> | Supply Current (Quiescent)   | Commercial (-38)   | GND ≤ V <sub>IN</sub> ≤ V <sub>IL</sub> or<br>V <sub>IH</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> ;<br>$\overline{OE}$ = HIGH |      | 40    | mA |
|  |                              | Military (-42)   |   |      | 45    |    |
|  |                              | All Others   |   |      | 30    |    |
| I <sub>CC</sub> (Q <sub>2</sub> ) <sup>[2]</sup> | Supply Current (Quiescent)   | Commercial   | GND ≤ V <sub>IN</sub> ≤ 0.4V or<br>3.85V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> ; $\overline{OE}$ = HIGH                         |      | 20    | mA |
|  |                              | Military   |   |      | 25    |    |
| I <sub>CC</sub> (Max.) <sup>[2]</sup>            | Supply Current               | Commercial   | V <sub>CC</sub> = Max., f <sub>CLK</sub> = 10 MHz;<br>$\overline{OE}$ = HIGH  |      | 100   | mA |
|  |                              | Military   |   |      | 110   |    |

### Capacitance<sup>[3]</sup>

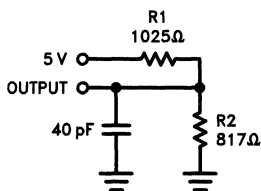
| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 8    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 10   |       |

#### Notes:

- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
- Two quiescent figures are given for different input voltage ranges. To calculate I<sub>CC</sub> at any given clock frequency, use 30 mA + I<sub>CC</sub> (A.C.), where I<sub>CC</sub> (A.C.) = (7 mA/MHz) × Clock Frequency for the Commercial temperature range. I<sub>CC</sub> (A.C.) = (8 mA/MHz) × Clock Frequency for the Military temperature range.
- Tested initially and after any design or process changes that may affect these parameters.
- See the last page of this specification for Group A subgroup testing information.

### Output Loads Used for A.C. Performance Characteristics

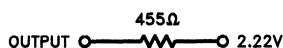
#### Normal Load (Load 1)



0054-4

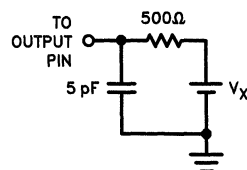
Equivalent to:

THÉVENIN EQUIVALENT



0054-6

#### Three-State Delay Load (Load 2)



0054-5

**Switching Characteristics Over Operating Range<sup>[2]</sup>**

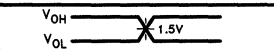
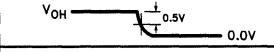
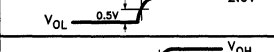
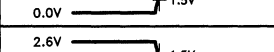
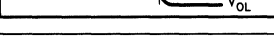
| Parameters                          | Description   |           | Test Conditions | 7C516-38 |      | 7C516-42 |      | 7C516-45 |      | 7C516-55 |      | 7C516-75 |      | Units |    |
|-------------------------------------|---|-----------|-----------------|----------|------|----------|------|----------|------|----------|------|----------|------|-------|----|
|                                     |   |           |                 | 7C517-38 |      | 7C517-42 |      | 7C517-45 |      | 7C517-55 |      | 7C517-75 |      |       |    |
|                                     |   |           |                 | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.     | Max. | Min.     | Max. |       |    |
| t <sub>MUC</sub>                    | Unlocked Multiply Time                                      |           | Load 1          |          | 58   |          | 65   |          | 65   |          | 75   |          | 100  | ns    |    |
| t <sub>MC</sub>                     | Clocked Multiply Time                                       |           |                 |          | 38   |          | 42   |          | 45   |          | 55   |          | 75   | ns    |    |
| t <sub>S</sub>                      | X <sub>i</sub> , Y <sub>i</sub> , RND, TCX, TCY Set-up Time |           |                 |          | 7    |          | 8    |          | 20   |          | 20   |          | 25   | ns    |    |
| t <sub>H</sub>                      | X <sub>i</sub> , Y <sub>i</sub> , RND, TCX, TCY Hold Time   |           |                 |          | 3    |          | 3    |          | 3    |          | 3    |          | 3    | ns    |    |
| t <sub>SE</sub>                     | ENX, ENY, ENP Set-up Time (7C517 Only)                      |           |                 |          | 10   |          | 15   |          | 20   |          | 20   |          | 25   | ns    |    |
| t <sub>HE</sub>                     | ENX, ENY, ENP Hold Time (7C517 Only)                        |           |                 |          | 3    |          | 3    |          | 3    |          | 3    |          | 3    | ns    |    |
| t <sub>PDW</sub> , t <sub>PWL</sub> | Clock Pulse Width (HIGH and LOW)                            |           |                 |          | 10   |          | 10   |          | 20   |          | 25   |          | 30   | ns    |    |
| t <sub>PDSEL</sub>                  | MSPSEL to Product Out                                       |           |                 |          | 18   |          | 21   |          | 25   |          | 25   |          | 30   | ns    |    |
| t <sub>PDP</sub>                    | Output Clock to P   |           |                 |          | 25   |          | 30   |          | 30   |          | 30   |          | 35   | ns    |    |
| t <sub>PDY</sub>                    | Output Clock to Y   |           |                 |          | 25   |          | 30   |          | 30   |          | 30   |          | 35   | ns    |    |
| t <sub>PHZ</sub>                    | OEP Disable Time  | HIGH to Z |                 | Load 2   |      | 15       |      | 17       |      | 25       |      | 25       |      | 30    | ns |
| t <sub>PLZ</sub>                    |   | LOW to Z  |                 |          |      | 15       |      | 17       |      | 25       |      | 25       |      | 30    | ns |
| t <sub>PZH</sub>                    | OEP Enable Time   | Z to HIGH |                 |          |      | 23       |      | 25       |      | 30       |      | 30       |      | 35    | ns |
| t <sub>PZL</sub>                    |   | Z to LOW  |                 |          | 23   |          | 25   |          | 30   |          | 30   |          | 35   | ns    |    |
| t <sub>PHZ</sub>                    | OEL Disable Time  | HIGH to Z |                 |          | 15   |          | 17   |          | 25   |          | 25   |          | 30   | ns    |    |
| t <sub>PLZ</sub>                    |   | LOW to Z  |                 |          | 15   |          | 17   |          | 25   |          | 25   |          | 30   | ns    |    |
| t <sub>PZH</sub>                    | OEL Enable Time   | Z to HIGH |                 |          | 23   |          | 25   |          | 30   |          | 30   |          | 35   | ns    |    |
| t <sub>PZL</sub>                    |   | Z to LOW  |                 |          | 23   |          | 25   |          | 30   |          | 30   |          | 35   | ns    |    |
| t <sub>HCL</sub>                    | Clock Low Hold Time CLKXY Relative to CLKML <sup>[1]</sup>  |           | Load 1          |          | 0    |          | 0    |          | 0    |          | 0    |          | 0    | ns    |    |

**5**

**Notes:**

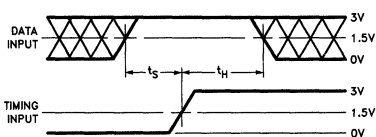
- To ensure that the correct product is entered in the output registers, new data may not be entered into the input registers before the output registers have been clocked.
- See the last page of this specification for Group A subgroup testing information.

**Test Waveforms (All Devices)**

| TEST                   | V <sub>X</sub>  | OUTPUT WAVEFORM – MEASUREMENT LEVEL   |
|------------------------|-----------------|---|
| ALL t <sub>pd</sub> 's | V <sub>CC</sub> |  |
| t <sub>PHZ</sub>       | 0.0V            |  |
| t <sub>PLZ</sub>       | 2.6V            |  |
| t <sub>PZH</sub>       | 0.0V            |  |
| t <sub>PZL</sub>       | 2.6V            |  |

0054-7

**Setup and Hold Time (All Devices)**

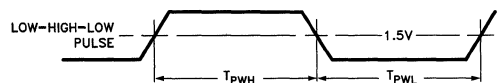


0054-8

**Notes:**

- Diagram shown for HIGH data only. Output transition may be opposite sense.

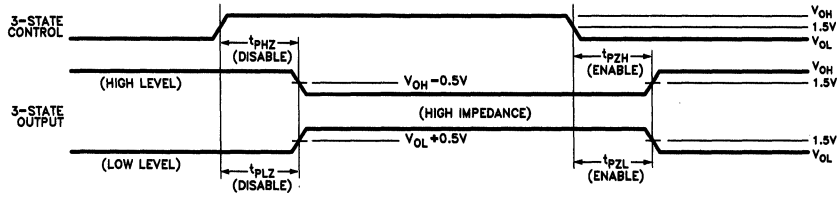
**Pulse Width (All Devices)**



0054-9

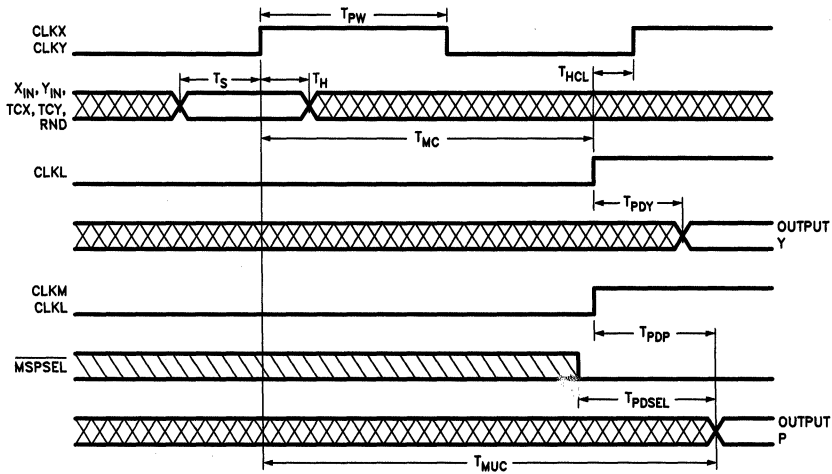
- Cross hatched area is don't care condition.

### Three-State Timing Diagram



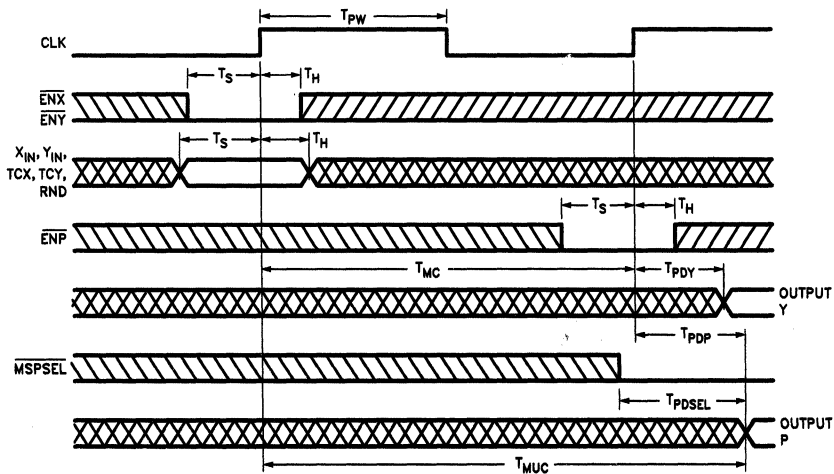
0054-10

### Timing Diagram 7C516



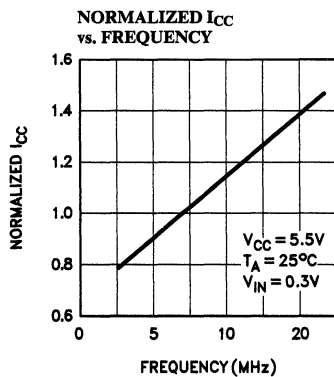
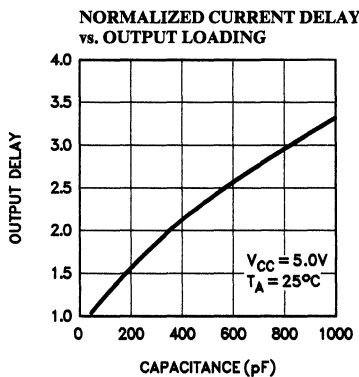
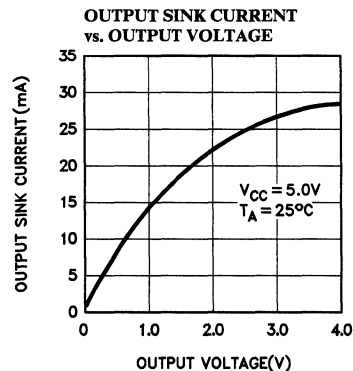
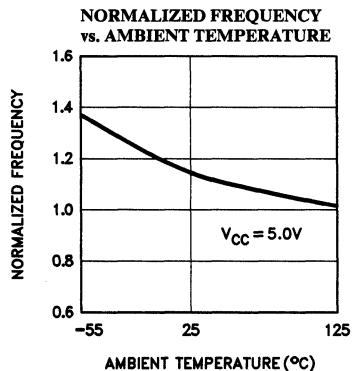
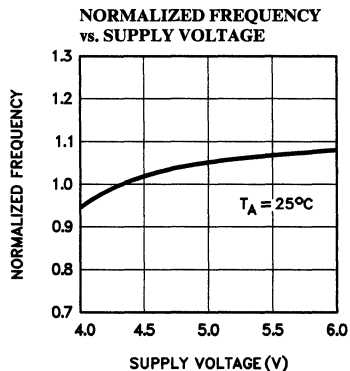
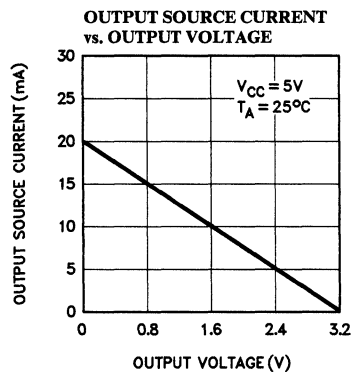
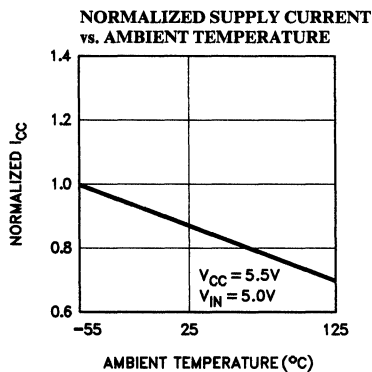
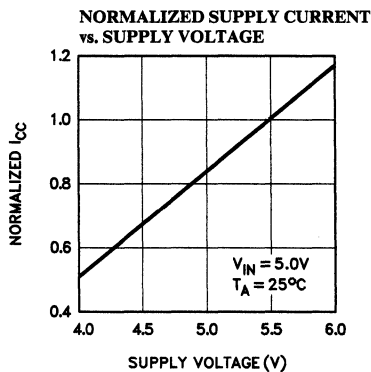
0054-11

### Timing Diagram 7C517



0054-15

## Typical DC and AC Characteristics





### Ordering Information

| Speed (ns) | Ordering Code                  | Package Type | Operating Range |
|------------|--------------------------------|--------------|-----------------|
| 38         | CY7C516-38PC<br>CY7C517-38PC   | P29          | Commercial      |
|            | CY7C516-38LC<br>CY7C517-38LC   | L81          |                 |
|            | CY7C516-38JC<br>CY7C517-38JC   | J81          |                 |
|            | CY7C516-38DC<br>CY7C517-38DC   | D30          |                 |
|            | CY7C516-38GC<br>CY7C517-38GC   | G68          |                 |
| 42         | CY7C516-42LMB<br>CY7C517-42LMB | L81          | Military        |
|            | CY7C516-42DMB<br>CY7C517-42DMB | D30          |                 |
|            | CY7C516-42GMB<br>CY7C517-42GMB | G68          |                 |
| 45         | CY7C516-45PC<br>CY7C517-45PC   | P29          | Commercial      |
|            | CY7C516-45LC<br>CY7C517-45LC   | L81          |                 |
|            | CY7C516-45JC<br>CY7C517-45JC   | J81          |                 |
|            | CY7C516-45DC<br>CY7C517-45DC   | D30          |                 |
|            | CY7C516-45GC<br>CY7C517-45GC   | G68          |                 |

| Speed (ns) | Ordering Code                  | Package Type | Operating Range |          |
|------------|--------------------------------|--------------|-----------------|----------|
| 55         | CY7C516-55PC<br>CY7C517-55PC   | P29          | Commercial      |          |
|            | CY7C516-55LC<br>CY7C517-55LC   | L81          |                 |          |
|            | CY7C516-55JC<br>CY7C517-55JC   | J81          |                 |          |
|            | CY7C516-55DC<br>CY7C517-55DC   | D30          |                 |          |
|            | CY7C516-55GC<br>CY7C517-55GC   | G68          |                 |          |
|            | CY7C516-55LMB<br>CY7C517-55LMB | L81          |                 | Military |
|            | CY7C516-55DMB<br>CY7C517-55DMB | D30          |                 |          |
| 75         | CY7C516-75PC<br>CY7C517-75PC   | P29          | Commercial      |          |
|            | CY7C516-75LC<br>CY7C517-75LC   | L81          |                 |          |
|            | CY7C516-75JC<br>CY7C517-75JC   | J81          |                 |          |
|            | CY7C516-75DC<br>CY7C517-75DC   | D30          |                 |          |
|            | CY7C516-75GC<br>CY7C517-75GC   | G68          |                 |          |
|            | CY7C516-75LMB<br>CY7C517-75LMB | L81          |                 | Military |
|            | CY7C516-75DMB<br>CY7C517-75DMB | D30          |                 |          |
|            | CY7C516-75GMB<br>CY7C517-75GMB | G68          |                 |          |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters                        | Subgroups |
|-----------------------------------|-----------|
| V <sub>OH</sub>                   | 1,2,3     |
| V <sub>OL</sub>                   | 1,2,3     |
| V <sub>IH</sub>                   | 1,2,3     |
| V <sub>IL</sub>                   | 1,2,3     |
| I <sub>OH</sub>                   | 1,2,3     |
| I <sub>OL</sub>                   | 1,2,3     |
| I <sub>IX</sub>                   | 1,2,3     |
| I <sub>OS</sub>                   | 1,2,3     |
| I <sub>OZL</sub>                  | 1,2,3     |
| I <sub>OZH</sub>                  | 1,2,3     |
| I <sub>CC</sub> (Q <sub>1</sub> ) | 1,2,3     |

| Parameters                        | Subgroups |
|-----------------------------------|-----------|
| I <sub>CC</sub> (Q <sub>2</sub> ) | 1,2,3     |
| I <sub>CC</sub> (Max.)            | 1,2,3     |

**Switching Characteristics**

| Parameters                          | Subgroups   |
|-------------------------------------|-------------|
| t <sub>MUC</sub>                    | 7,8,9,10,11 |
| t <sub>MC</sub>                     | 7,8,9,10,11 |
| t <sub>S</sub>                      | 7,8,9,10,11 |
| t <sub>H</sub>                      | 7,8,9,10,11 |
| t <sub>SE</sub>                     | 7,8,9,10,11 |
| t <sub>HE</sub>                     | 7,8,9,10,11 |
| t <sub>PWH</sub> , t <sub>PWL</sub> | 7,8,9,10,11 |
| t <sub>PDSEL</sub>                  | 7,8,9,10,11 |
| t <sub>PDY</sub>                    | 7,8,9,10,11 |
| t <sub>PHZ</sub>                    | 7,8,9,10,11 |
| t <sub>PLZ</sub>                    | 7,8,9,10,11 |
| t <sub>PZH</sub>                    | 7,8,9,10,11 |
| t <sub>PZL</sub>                    | 7,8,9,10,11 |
| t <sub>PHZ</sub>                    | 7,8,9,10,11 |
| t <sub>PLZ</sub>                    | 7,8,9,10,11 |
| t <sub>PZH</sub>                    | 7,8,9,10,11 |
| t <sub>PZL</sub>                    | 7,8,9,10,11 |
| t <sub>HCL</sub>                    | 7,8,9,10,11 |

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**Features**

- **Fast**  
CY7C901-23 has a 23 ns Read Modify-Write Cycle; Commercial 25% Faster than "C" Spec 2901  
CY7C901-27 has a 27 ns Read Modify-Write Cycle; Military 15% Faster than "C" Spec 2901
- **Low Power**  
70 mA (commercial)  
90 mA (military)
- **V<sub>CC</sub> 5V ±10%**  
Commercial and military
- **Eight Function ALU**
- **Infinitely expandable in 4-bit increments**
- **Four Status Flags:**  
Carry, overflow, negative, zero
- **Capable of withstanding greater than 2000V static discharge voltage**

- **Pin Compatible and Functional Equivalent to Am2901B, C**

**Functional Description**

The CY7C901 is a high-speed, expandable, 4-bit wide ALU that can be used to implement the arithmetic section of a CPU, peripheral controller, or programmable controller. The instruction set of the CY7C901 is basic but yet so versatile that it can emulate the ALU of almost any digital computer.

The CY7C901, as illustrated in the block diagram, consists of a 16-word by 4-bit dual-port RAM register file, a 4-bit ALU and the required data manipulation and control logic.

The operation performed is determined by nine input control lines (I<sub>0</sub> to I<sub>8</sub>)

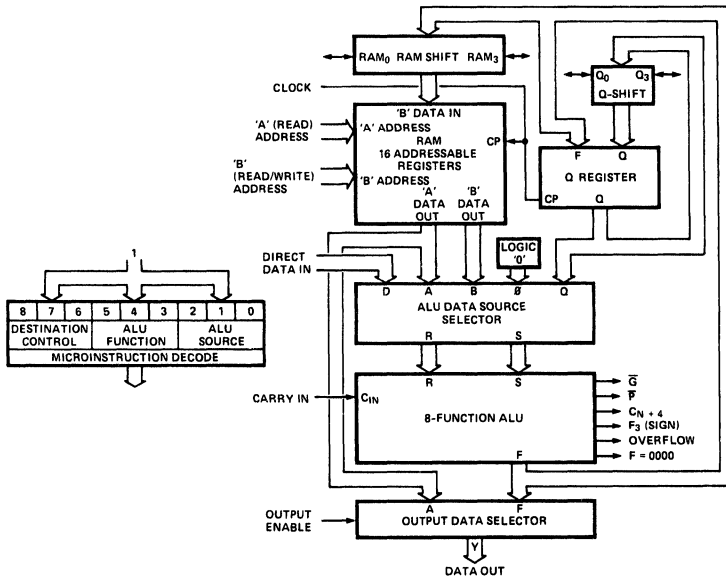
that are usually inputs from a microinstruction register.

The CY7C901 is expandable in 4-bit increments, has three-state data outputs as well as flag output, and can use either a full look ahead carry or a ripple carry.

The CY7C901 is a pin compatible, functional equivalent, improved performance replacement for the Am2901.

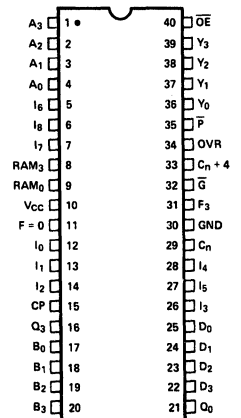
The CY7C901 is fabricated using an advanced 1.2 micron CMOS process that eliminates latchup, results in ESD protection over 2000V and achieves superior performance with low power dissipation.

**Logic Block Diagram**



**Pin Configuration**

**Top View**



0030-2

0030-1

**Selection Guide** See last page for ordering information.

| Read Modify-Write Cycle (Min.) in ns | Operating I <sub>CC</sub> (Max.) in mA | Operating Range | Part Number |
|--------------------------------------|--|-----------------|-------------|
| 23                                   | 80                                     | Commercial      | CY7C901-23  |
| 27                                   | 90                                     | Military        | CY7C901-27  |
| 31                                   | 70                                     | Commercial      | CY7C901-31  |
| 32                                   | 90                                     | Military        | CY7C901-32  |

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied ..... -55°C to +125°C  
 Supply Voltage to Ground Potential  
 (Pin 10 to Pin 30) ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs  
 in High Z State ..... -0.5V to +7.0V  
 DC Input Voltage ..... -3.0V to +7.0V  
 Output Current into Outputs (Low) ..... 30 mA

Static Discharge Voltage ..... > 2001V  
 (Per MIL-STD-883 Method 3015)

Latchup Current (Outputs) ..... > 200 mA

**Operating Range**

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[1]</sup> | -55°C to +125°C     | 5V ± 10%        |

Note:

 1. T<sub>A</sub> is the "instant on" case temperature.

**Pin Definitions**

| Signal Name                     | I/O | Description   |
|---------------------------------|-----|---|
| A <sub>0</sub> -A <sub>3</sub>  | I   | These 4 address lines select one of the registers in the stack and output its contents on the (internal) A port.  |
| B <sub>0</sub> -B <sub>3</sub>  | I   | These 4 address lines select one of the registers in the stack and output its contents on the (internal) B port. This can also be the destination address when data is written back into the register file.   |
| I <sub>0</sub> -I <sub>8</sub>  | I   | These 9 instruction lines select the ALU data sources (I <sub>0</sub> , 1, 2), the operation to be performed (I <sub>3</sub> , 4, 5) and what data is to be written into either the Q register or the register file (I <sub>6</sub> , 7, 8).  |
| D <sub>0</sub> -D <sub>3</sub>  | I   | These are 4 data input lines that may be selected by the I <sub>0</sub> , 1, 2 lines as inputs to the ALU.  |
| Y <sub>0</sub> -Y <sub>3</sub>  | O   | These are three-state data output lines that, when enabled, output either the output of the ALU or the data in the A latches, as determined by the code on the I <sub>6</sub> , 7, 8 lines.   |
| $\overline{OE}$                 | I   | Output Enable. This is an active LOW input that controls the Y <sub>0</sub> -Y <sub>3</sub> outputs. When this signal is LOW the Y outputs are enabled and when it is HIGH they are in the high impedance state.  |
| CP                              | I   | Clock Input. The LOW level of the clock write data to the 16 x 4 RAM. The HIGH level of the clock writes data from the RAM to the A-port and B-port latches. The operation of the Q register is similar. Data is entered into the master latch on the LOW level of the clock and transferred from master to slave when the clock is HIGH. |
| Q <sub>3</sub> RAM <sub>3</sub> | I/O | These two lines are bidirectional and are controlled by the I <sub>6</sub> , 7, 8 inputs. Electrically they are three-state output drivers connected to the TTL compatible CMOS inputs.   |

| Signal Name                             | I/O | Description   |
|---|-----|---|
| Q <sub>3</sub> RAM <sub>3</sub> (Cont.) | I/O | <b>Outputs:</b> When the destination code on lines I <sub>6</sub> , 7, 8 indicates a shift left (UP) operation the three-state outputs are enabled and the MSB of the Q register is output on the Q <sub>3</sub> pin and the MSB of the ALU output (F <sub>3</sub> ) is output on the RAM 3 pin.<br><b>Inputs:</b> When the destination code indicates a shift right (DOWN) the pins are the data inputs to the MSB of the Q register and the MSB of the RAM. |
| Q <sub>0</sub> RAM <sub>0</sub>         | I/O | These two lines are bidirectional and function in a manner similar to the Q <sub>3</sub> and RAM <sub>3</sub> lines, except that they are the LSB of the Q register and RAM.  |
| C <sub>n</sub>                          | I   | The carry-in to the internal ALU.   |
| C <sub>n</sub> + 4                      | O   | The carry-out from the internal ALU.  |
| $\overline{G}$ , $\overline{P}$         | O   | The carry generate and the carry propagate outputs of the ALU, which may be used to perform a carry look-ahead operation over the 4-bits of the ALU.  |
| OVR                                     | O   | Overflow. This signal is logically the exclusive-OR of the carry-in and the carry-out of the MSB of the ALU. This pin indicates that the result of the ALU operation has exceeded the capacity of the machine. It is valid only for the sign bit and assumes two's complement coding for negative numbers.  |
| F = 0                                   | O   | Open drain output that goes HIGH if the data on the ALU outputs (F <sub>0</sub> , 1, 2, 3) are all LOW. It indicates that the result of an ALU operation is zero (positive logic).  |
| F <sub>3</sub>                          | O   | The most significant bit of the ALU output.   |

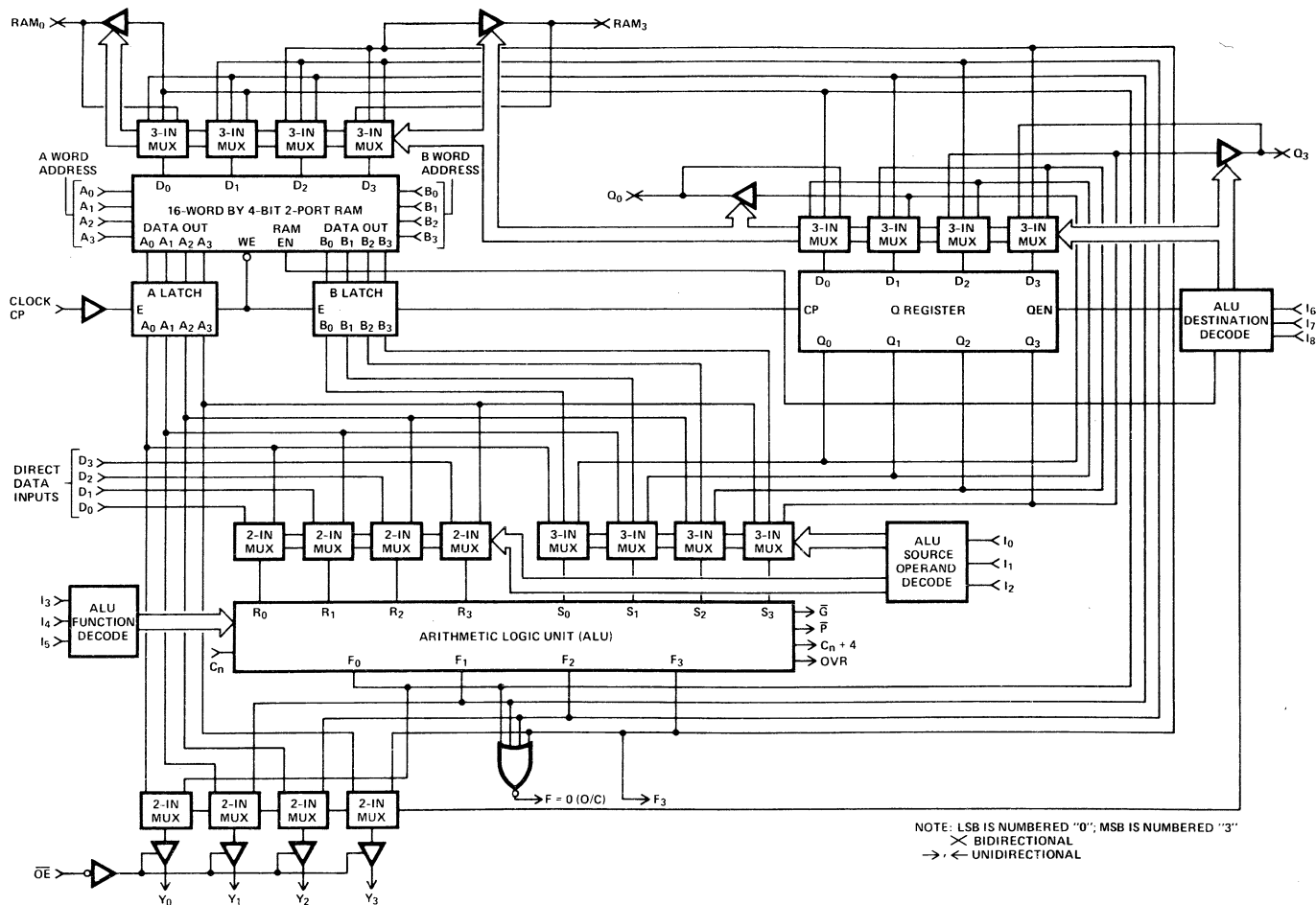


Figure 1. CY7C901 Block Diagram

0030-3

**Functional Tables**

| Mnemonic | Micro Code     |                |                |            | ALU Source Operands |   |
|----------|----------------|----------------|----------------|------------|---------------------|---|
|          | I <sub>2</sub> | I <sub>1</sub> | I <sub>0</sub> | Octal Code | R                   | S |
| AQ       | L              | L              | L              | 0          | A                   | Q |
| AB       | L              | L              | H              | 1          | A                   | B |
| ZQ       | L              | H              | L              | 2          | O                   | Q |
| ZB       | L              | H              | H              | 3          | O                   | B |
| ZA       | H              | L              | L              | 4          | O                   | A |
| DA       | H              | L              | H              | 5          | D                   | A |
| DQ       | H              | H              | L              | 6          | D                   | Q |
| DZ       | H              | H              | H              | 7          | D                   | O |

Figure 2. ALU Source Operand Control

| Mnemonic | Micro Code     |                |                |            | ALU Function | Symbol |
|----------|----------------|----------------|----------------|------------|--------------|--------|
|          | I <sub>5</sub> | I <sub>4</sub> | I <sub>3</sub> | Octal Code |              |        |
| ADD      | L              | L              | L              | 0          | R Plus S     | R + S  |
| SUBR     | L              | L              | H              | 1          | S Minus R    | S - R  |
| SUBS     | L              | H              | L              | 2          | R Minus S    | R - S  |
| OR       | L              | H              | H              | 3          | R OR S       | R ∨ S  |
| AND      | H              | L              | L              | 4          | R AND S      | R ∧ S  |
| NOTRS    | H              | L              | H              | 5          | R AND S      | R ∧ S  |
| EXOR     | H              | H              | L              | 6          | R EX-OR S    | R ⊕ S  |
| EXNOR    | H              | H              | H              | 7          | R EX-NOR S   | R ⊖ S  |

Figure 3. ALU Function Control

| Mnemonic | Micro Code     |                |                |            | RAM Function |         | Q-Reg. Function |         | Y Output | RAM Shifter      |                  | Q Shifter       |                 |
|----------|----------------|----------------|----------------|------------|--------------|---------|-----------------|---------|----------|------------------|------------------|-----------------|-----------------|
|          | I <sub>8</sub> | I <sub>7</sub> | I <sub>6</sub> | Octal Code | Shift        | Load    | Shift           | Load    |          | RAM <sub>0</sub> | RAM <sub>3</sub> | Q <sub>0</sub>  | Q <sub>3</sub>  |
| QREG     | L              | L              | L              | 0          | X            | None    | None            | F → Q   | F        | X                | X                | X               | X               |
| NOP      | L              | L              | H              | 1          | X            | None    | X               | None    | F        | X                | X                | X               | X               |
| RAMA     | L              | H              | L              | 2          | None         | F → B   | X               | None    | A        | X                | X                | X               | X               |
| RAMF     | L              | H              | H              | 3          | None         | F → B   | X               | None    | F        | X                | X                | X               | X               |
| RAMQD    | H              | L              | L              | 4          | DOWN         | F/2 → B | DOWN            | Q/2 → Q | F        | F <sub>0</sub>   | IN <sub>3</sub>  | Q <sub>0</sub>  | IN <sub>3</sub> |
| RAMD     | H              | L              | H              | 5          | DOWN         | F/2 → B | X               | None    | F        | F <sub>0</sub>   | IN <sub>3</sub>  | Q <sub>0</sub>  | X               |
| RAMQU    | H              | H              | L              | 6          | UP           | 2F → B  | UP              | 2Q → Q  | F        | IN <sub>0</sub>  | F <sub>3</sub>   | IN <sub>0</sub> | Q <sub>3</sub>  |
| RAMU     | H              | H              | H              | 7          | UP           | 2F → B  | X               | None    | F        | IN <sub>0</sub>  | F <sub>3</sub>   | X               | Q <sub>3</sub>  |

X = Don't care. Electrically, the input shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.  
A = Register Addressed by A inputs.  
B = Register Addressed by B inputs.  
UP is toward MSB, DOWN is toward LSB.

Figure 4. ALU Destination Control

| Octal I <sub>543</sub> | I <sub>210</sub> Octal                                | 0         | 1         | 2      | 3      | 4      | 5         | 6         | 7      |
|------------------------|---|-----------|-----------|--------|--------|--------|-----------|-----------|--------|
|                        | ALU Source  |           |           |        |        |        |           |           |        |
|                        | ALU Function  | A, Q      | A, B      | O, Q   | O, B   | O, A   | D, A      | D, Q      | D, O   |
| 0                      | C <sub>n</sub> = L<br>R plus S<br>C <sub>n</sub> = H  | A + Q     | A + B     | Q      | B      | A      | D + A     | D + Q     | D      |
| 1                      | C <sub>n</sub> = L<br>S minus R<br>C <sub>n</sub> = H | Q - A - 1 | B - A - 1 | Q - 1  | B - 1  | A - 1  | A - D - 1 | Q - D - 1 | -D - 1 |
| 2                      | C <sub>n</sub> = L<br>R minus S<br>C <sub>n</sub> = H | A - Q - 1 | A - B - 1 | -Q - 1 | -B - 1 | -A - 1 | D - A - 1 | D - Q - 1 | D - 1  |
| 3                      | RORS  | A ∨ Q     | A ∨ B     | Q      | B      | A      | D ∨ A     | D ∨ Q     | D      |
| 4                      | RANDS   | A ∧ Q     | A ∧ B     | 0      | 0      | 0      | D ∧ A     | D ∧ Q     | 0      |
| 5                      | RANDS   | A ∧ Q     | A ∧ B     | Q      | B      | A      | D ∧ A     | D ∧ Q     | 0      |
| 6                      | REX-ORS   | A ⊕ Q     | A ⊕ B     | Q      | B      | A      | D ⊕ A     | D ⊕ Q     | D      |
| 7                      | REX-NORS  | A ⊖ Q     | A ⊖ B     | Q      | B      | A      | D ⊖ A     | D ⊖ Q     | D      |

+ = Plus; - = Minus; ∨ = OR; ∧ = AND; ⊕ = EX-OR

Figure 5. Source Operand and ALU Function Matrix

## Description of Architecture

### General Description

A block diagram of the CY7C901 is shown in *Figure 1*. The circuit is a 4-bit slice consisting of a register file (16 x 4 dual port RAM), the ALU, the Q register and the necessary control logic. It is expandable in 4-bit increments.

### RAM

The RAM is addressed by two 4-bit address fields ( $A_0$ – $A_3$ ,  $B_0$ – $B_3$ ) that cause the data to appear at the A or B (internal) ports. If the A and B addresses are the same, the data at the A and B ports will be identical.

New data is written into the RAM location specified by the B address when the RAM write enable (RAM EN) is active and the clock input is LOW. Each of the four RAM inputs is driven by a 3-input multiplexer that allows the outputs of the ALU ( $F_0, 1, 2, 3$ ) to be shifted one bit position to the left, the right, or not to be shifted. The other inputs to the multiplexer are from the  $RAM_3$  and  $RAM_0$  I/O pins.

For a shift left (up) operation, the  $RAM_3$  output buffer is enabled and the  $RAM_0$  multiplexer input is enabled. For a shift right (down) operation the  $RAM_0$  output buffer is enabled and the  $RAM_3$  multiplexer input is enabled.

The data to be written into the RAM is applied to the D inputs of the CY7C901 and is passed (unchanged) through the ALU to the RAM location addressed by the B word address.

The outputs of the RAM A and B ports drive separate 4-bit latches that are enabled (follow the RAM data) when the clock is HIGH. The outputs of the A latches go to three multiplexers whose outputs drive the two inputs to the ALU ( $R_0, 1, 2, 3$ ) and ( $S_0, 1, 2, 3$ ) and the ( $Y_0, 1, 2, 3$ ) chip outputs.

### ALU (Arithmetic Logic Unit)

The ALU can perform three arithmetic and five logical operations on two 4-bit input words, R and S. The R inputs are driven from four 2-input multiplexers whose inputs are from either the (RAM) A-port or the external data (D) inputs. The S inputs are driven from four 3-input multiplexers whose inputs are from the A-port, the B-port, or the Q register. Both multiplexers are controlled by the

$I_0, 1, 2$  inputs as shown in *Figure 2*. This configuration of multiplexers on the ALU R and S inputs enables the user to select eight pairs of combinations of A, B, D, Q and "0" (unselected) inputs as 4-bits operands to the ALU. The logical and arithmetic operations performed by the ALU upon the data present at its R and S inputs are tabulated in *Figure 3*. The ALU has a carry-in ( $C_n$ ) input, carry-propagate ( $\bar{P}$ ) output, carry-generate ( $\bar{G}$ ) output, carry-out ( $C_n + 4$ ) and overflow (OVR) pins to enable the user to (1) speed up arithmetic operations by implementing carry look-ahead logic and (2) determine if an arithmetic overflow has occurred.

The ALU data outputs ( $F_0, 1, 2, 3$ ) are routed to the RAM, the Q register inputs and the Y outputs under control of the  $I_6, 7, 8$  control signal inputs as shown in *Figure 4*. In addition, the MSB of the ALU is output as  $F_3$  so that the user can examine the sign bit without enabling the three-state outputs. The  $F = 0$  output, used for zero detection, is HIGH when all bits of the F output are LOW. It is an open-drain output which may be wire OR'ed across multiple 7C901 processor slices.

### Q Register

The Q register functions as an accumulator or temporary storage register. Physically it is a 4-bit register implemented with master-slave latches. The inputs to the Q register are driven by the outputs from four 3-input multiplexers under control of the  $I_6, 7, 8$  inputs. The  $Q_0$  and  $Q_3$  I/O pins function in a manner similar to the  $RAM_0$  and  $RAM_3$  pins. The other inputs to the multiplexer enable the contents of the Q register to be shifted up or down, or the outputs of the ALU to be entered into the master latches. Data is entered into the master latches when the clock is LOW and transferred from master to slave (output) when the clock changes from LOW to HIGH.

### ALU Source Operand and ALU Functions

The ALU source operands and ALU function matrix is summarized in *Figure 5* and separated by logic operation or arithmetic operation in *Figures 6* and *7*, respectively. The  $I_0, 1, 2$  lines select eight pairs of source operands and the  $I_3, 4, 5$  lines select the operation to be performed. The carry-in ( $C_n$ ) signal affects the arithmetic result and the internal flags; not the logical operations.

**Conventional Addition and Pass-Increment/  
Decrement**

When the carry-in is HIGH and either a conventional addition or a PASS operation is performed, one (1) is added to the result. If the DECREMENT operation is performed when the carry-in is LOW, the value of the operand is reduced by one. However, when the same operation is performed when the carry-in is HIGH, it nullifies the DECREMENT operation so that the result is equivalent to the PASS operation.

| Octal<br>I543, I210  | Group  | Function   |
|----------------------|--------|--|
| 40<br>41<br>45<br>46 | AND    | $A \wedge Q$<br>$A \wedge B$<br>$D \wedge A$<br>$D \wedge Q$   |
| 30<br>31<br>35<br>36 | OR     | $A \vee Q$<br>$A \vee B$<br>$D \vee A$<br>$D \vee Q$   |
| 60<br>61<br>65<br>66 | EX-OR  | $A \nabla Q$<br>$A \nabla B$<br>$D \nabla A$<br>$D \nabla Q$   |
| 70<br>71<br>75<br>76 | EX-NOR | $\overline{A \nabla Q}$<br>$\overline{A \nabla B}$<br>$\overline{D \nabla A}$<br>$\overline{D \nabla Q}$ |
| 72<br>73<br>74<br>77 | INVERT | $\overline{Q}$<br>$\overline{B}$<br>$\overline{A}$<br>$\overline{D}$                                     |
| 62<br>63<br>64<br>67 | PASS   | Q<br>B<br>A<br>D   |
| 32<br>33<br>34<br>37 | PASS   | Q<br>B<br>A<br>D   |
| 42<br>43<br>44<br>47 | "ZERO" | 0<br>0<br>0<br>0   |
| 50<br>51<br>55<br>56 | MASK   | $\overline{A} \wedge Q$<br>$\overline{A} \wedge B$<br>$\overline{D} \wedge A$<br>$\overline{D} \wedge Q$ |

**Figure 6. ALU Logic Mode Functions**
**Subtraction**

Recall that in two's complement integer coding  $-1$  is equal to all ones and that in one's complement integer coding zero is equal to all ones. To convert a positive integer to its two's complement (negative) equivalent, invert (complement) the number and add 1 to it; i.e.,  $TWC = ONC + 1$ . In Figure 7 the symbol  $-Q$  represents the two's complement of Q so that the one's complement of Q is then  $-Q - 1$ .

| Octal<br>I543, I210                          | $C_n = 0$ (Low)      |  | $C_n = 1$ (High)     |  |
|--|----------------------|--|----------------------|--|
|  | Group                | Function   | Group                | Function   |
| 00<br>01<br>05<br>06                         | ADD                  | $A + Q$<br>$A + B$<br>$D + A$<br>$D + Q$   | ADD plus one         | $A + Q + 1$<br>$A + B + 1$<br>$D + A + 1$<br>$D + Q + 1$                             |
| 02<br>03<br>04<br>07                         | PASS                 | Q<br>B<br>A<br>D   | Increment            | $Q + 1$<br>$B + 1$<br>$A + 1$<br>$D + 1$   |
| 12<br>13<br>14<br>27                         | Decrement            | $Q - 1$<br>$B - 1$<br>$A - 1$<br>$D - 1$   | PASS                 | Q<br>B<br>A<br>D   |
| 22<br>23<br>24<br>17                         | 1's Comp.            | $-Q - 1$<br>$-B - 1$<br>$-A - 1$<br>$-D - 1$   | 2's Comp. (Negate)   | $-Q$<br>$-B$<br>$-A$<br>$-D$   |
| 10<br>11<br>15<br>16<br>20<br>21<br>25<br>26 | Subtract (1's Comp.) | $Q - A - 1$<br>$B - A - 1$<br>$A - D - 1$<br>$Q - D - 1$<br>$A - Q - 1$<br>$A - B - 1$<br>$D - A - 1$<br>$D - Q - 1$ | Subtract (2's Comp.) | $Q - A$<br>$B - A$<br>$A - D$<br>$Q - D$<br>$A - Q$<br>$A - B$<br>$D - A$<br>$D - Q$ |

**Figure 7. ALU Arithmetic Mode Functions**



### Logic Functions for $\bar{G}$ , $\bar{P}$ , $C_n + 4$ , and OVR

The four signals  $G$ ,  $P$ ,  $C_n + 4$ , and OVR are designed to indicate carry and overflow conditions when the CY7C901 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The  $R$  and  $S$  inputs are the two inputs selected according to Figure 2.

#### Definitions (+ = OR)

$$\begin{aligned}
 P_0 &= R_0 + S_0 & G_0 &= R_0 S_0 \\
 P_1 &= R_1 + S_1 & G_1 &= R_1 S_1 \\
 P_2 &= R_2 + S_2 & G_2 &= R_2 S_2 \\
 P_3 &= R_3 + S_3 & G_3 &= R_3 S_3 \\
 C_4 &= G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 G_0 + P_3 P_2 P_1 P_0 C_n \\
 C_3 &= G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n
 \end{aligned}$$

| I543 | Function                 | $\bar{P}$  | $\bar{G}$   | $C_n + 4$   | OVR                                |
|------|--------------------------|--|---|---|------------------------------------|
| 0    | $R + S$                  | $\overline{P_3 P_2 P_1 P_0}$   | $\overline{G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0}$                            | $C_4$   | $C_3 \vee C_4$                     |
| 1    | $S - R$                  | ←  | Same as $R + S$ equations, but substitute $\bar{R}_i$ for $R_i$ in definitions        |   | →                                  |
| 2    | $R - S$                  | ←  | Same as $R + S$ equations, but substitute $\bar{S}_i$ for $S_i$ in definitions        |   | →                                  |
| 3    | $R \vee S$               | LOW  | $P_3 P_2 P_1 P_0$   | $\overline{P_3 P_2 P_1 P_0} + C_n$  | $\overline{P_3 P_2 P_1 P_0} + C_n$ |
| 4    | $R \wedge S$             | LOW  | $\overline{G_3 + G_2 + G_1 + G_0}$  | $G_3 + G_2 + G_1 + G_0 + C_n$   | $G_3 + G_2 + G_1 + G_0 + C_n$      |
| 5    | $\bar{R} \wedge S$       | LOW  | ← Same as $R \wedge S$ equations, but substitute $\bar{R}_i$ for $R_i$ in definitions |   | →                                  |
| 6    | $R \nabla S$             | ← Same as $R \nabla S$ , but substitute $\bar{R}_i$ for $R_i$ in definitions |   | →   |                                    |
| 7    | $\bar{R} \nabla \bar{S}$ | $G_3 + G_2 + G_1 + G_0$  | $G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 P_0$                                       | $\overline{G_3 + P_3 G_2 + P_3 P_2 G_1} + \overline{P_3 P_2 P_1 P_0} (G_0 + \bar{C}_n)$ | See note                           |

**Notes:**

$$[P_2 + G_2 P_1 + \bar{G}_2 \bar{G}_1 \bar{P}_0 + \bar{G}_2 \bar{G}_1 \bar{G}_0 C_n] \vee [P_3 + \bar{G}_3 \bar{P}_2 + \bar{G}_3 \bar{G}_2 \bar{P}_1 + \bar{G}_3 \bar{G}_2 \bar{G}_1 \bar{P}_0 + \bar{G}_3 \bar{G}_2 \bar{G}_1 \bar{G}_0 C_n]$$

+ = OR

Figure 8

**Electrical Characteristics** Over Commercial and Military Operating Range<sup>[3]</sup>
 $V_{CC}$  Min. = 4.5V,  $V_{CC}$  Max. = 5.5V

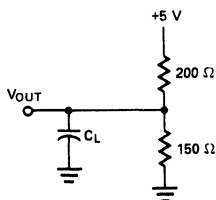
| Parameters | Description                                 | Test Conditions  | Min.                   | Max.       | Units                          |
|------------|---|--|------------------------|------------|--------------------------------|
| $V_{OH}$   | Output HIGH Voltage                         | $V_{CC} = \text{Min.}$<br>$I_{OH} = -3.4 \text{ mA}$   | 2.4                    |            | V                              |
| $V_{OL}$   | Output LOW Voltage                          | $V_{CC} = \text{Min.}$<br>$I_{OL} = 20 \text{ mA Commercial}$<br>$I_{OL} = 16 \text{ mA Military}$ |                        | 0.4        | V                              |
| $V_{IH}$   | Input HIGH Voltage                          |  | 2.0                    | $V_{CC}$   | V                              |
| $V_{IL}$   | Input LOW Voltage                           |  | -3.0                   | 0.8        | V                              |
| $I_{IX}$   | Input Leakage Current                       | $V_{SS} \leq V_{IN} \leq V_{CC}$<br>$V_{CC} = \text{Max.}$   | -10                    | 10         | $\mu\text{A}$                  |
| $I_{OH}$   | Output HIGH Current                         | $V_{CC} = \text{Min.}$<br>$V_{OH} = 2.4\text{V}$   | -3.4                   |            | mA                             |
| $I_{OL}$   | Output LOW Current                          | $V_{CC} = \text{Min.}$<br>$V_{OL} = 0.4\text{V}$   | Commercial<br>20       |            | mA                             |
|            |   |  | Military<br>16         |            |                                |
| $I_{OZ}$   | Output Leakage Current                      | $V_{CC} = \text{Max.}$<br>$V_{OUT} = V_{SS} \text{ to } V_{CC}$                                    | -40                    | +40        | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{SC}$   | Output Short Circuit Current <sup>[1]</sup> | $V_{CC} = \text{Max.}$<br>$V_{OUT} = 0\text{V}$  |                        | -85        | mA                             |
| $I_{CC}$   | Supply Current                              | $V_{CC} = \text{Max.}$   | Commercial -31         | 70         | mA                             |
|            |   |  | Commercial -23         | 80         |                                |
|            |   |  | Military -27, -32      | 90         |                                |
| $I_{CC1}$  | Supply Current                              | $V_{IH} \geq V_{CC} - 1.2\text{V}$ , 10 MHz<br>$V_{IL} \leq 0.4\text{V}$                           | Commercial<br>Military | 26.5<br>31 | mA                             |

**5**
**Capacitance**<sup>[2]</sup>

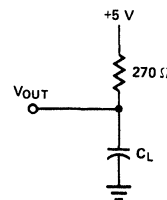
| Parameters | Description        | Test Conditions  | Max. | Units |
|------------|--------------------|--|------|-------|
| $C_{IN}$   | Input Capacitance  | $T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$<br>$V_{CC} = 5.0\text{V}$ | 5    | pF    |
| $C_{OUT}$  | Output Capacitance |  | 7    |       |

**Notes:**

- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
- Tested initially and after any design or process changes that may affect these parameters.
- See the last page of this specification for Group A subgroup testing information.

**Output Loads used for AC Performance Characteristics**


0030-4

**All outputs except open drain**


0030-5

**Open drain (F = 0)**
**Notes:**

- $C_L = 50 \text{ pF}$  includes scope probe, wiring and stray capacitance.
- $C_L = 5 \text{ pF}$  for output disable tests.
- Loads shown above are for commercial (20 mA)  $I_{OL}$  spec only.

**CY7C901-23 Commercial and  
 CY7C901-27 Military AC Performance  
 Characteristics**

The tables below specify the guaranteed AC performance of these devices over the Commercial (0°C to 70°C) and Military (-55°C to +125°C) operating temperature range with V<sub>CC</sub> varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See "Electrical Characteristics" for loading circuit information.

This data applies to parts with the following numbers:

CY7C901-23PC      CY7C901-23DC      CY7C901-23LC  
 CY7C901-23JC      CY7C901-27DMB      CY7C901-27LMB

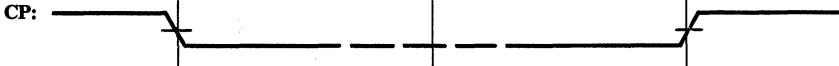
**Combinational Propagation Delays. C<sub>L</sub> = 50 pF<sup>[5]</sup>**

| To Output<br>From Input   | Y              |    | F <sub>3</sub> |    | C <sub>n+4</sub> |    | G, P |    | F = 0 |    | OVR |    | RAM <sub>0</sub><br>RAM <sub>3</sub> |    | Q <sub>0</sub><br>Q <sub>3</sub> |    |
|---------------------------|----------------|----|----------------|----|------------------|----|------|----|-------|----|-----|----|--------------------------------------|----|----------------------------------|----|
|                           | <b>CY7C901</b> | 23 | 27             | 23 | 27               | 23 | 27   | 23 | 27    | 23 | 27  | 23 | 27                                   | 23 | 27                               | 23 |
| A, B Address              | 30             | 33 | 30             | 33 | 30               | 33 | 28   | 33 | 30    | 33 | 30  | 33 | 30                                   | 33 | —                                | —  |
| Data                      | 21             | 24 | 20             | 23 | 20               | 23 | 20   | 21 | 24    | 25 | 21  | 24 | 22                                   | 25 | —                                | —  |
| C <sub>n</sub>            | 17             | 18 | 16             | 17 | 14               | 14 | —    | —  | 18    | 19 | 16  | 17 | 18                                   | 19 | —                                | —  |
| I <sub>012</sub>          | 26             | 28 | 25             | 27 | 24               | 26 | 24   | 28 | 25    | 29 | 24  | 27 | 25                                   | 27 | —                                | —  |
| I <sub>345</sub>          | 26             | 27 | 24             | 27 | 24               | 26 | 24   | 26 | 26    | 27 | 24  | 26 | 26                                   | 27 | —                                | —  |
| I <sub>678</sub>          | 16             | 18 | —              | —  | —                | —  | —    | —  | —     | —  | —   | —  | 21                                   | 21 | 21                               | 21 |
| A Bypass ALU<br>(I = 2XX) | 24             | 26 | —              | —  | —                | —  | —    | —  | —     | —  | —   | —  | —                                    | —  | —                                | —  |
| Clock                     | 24             | 27 | 23             | 26 | 23               | 26 | 23   | 25 | 24    | 27 | 24  | 26 | 24                                   | 27 | 19                               | 20 |

**Cycle Time and Clock Characteristics<sup>[5]</sup>**

| CY7C901   | -23    | -27    |
|---|--------|--------|
| Read-Modify-Write Cycle (from selection of A, B registers to end of cycle). | 23 ns  | 27 ns  |
| Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)         | 43 MHz | 37 MHz |
| Minimum Clock LOW Time  | 13 ns  | 15 ns  |
| Minimum Clock HIGH Time   | 10 ns  | 12 ns  |
| Minimum Clock Period  | 23 ns  | 27 ns  |

**Set-up and Hold Times Relative to Clock (CP) Input<sup>[5]</sup>**

| Input                                   | CP:  |    | Set-up Time Before H → L |    | Hold Time After H → L  |    | Set-up Time Before L → H |    | Hold Time After L → H |    |
|---|--|----|--------------------------|----|------------------------|----|--------------------------|----|-----------------------|----|
|   | 23   | 27 | 23                       | 27 | 23                     | 27 | 23                       | 27 | 23                    | 27 |
| <b>CY7C901</b>                          | 23   | 27 | 23                       | 27 | 23                     | 27 | 23                       | 27 | 23                    | 27 |
| A, B Source Address                     | 10   | 12 | 0 (Note 3)               |    | 21, 10 + tpWL (Note 4) |    | 0                        |    | 0                     |    |
| B Destination Address                   | 10   | 12 | ← Do Not Change →        |    |                        |    |                          |    | 0                     |    |
| Data                                    | —  | —  | —                        |    | 16                     |    | 0                        |    | 0                     |    |
| C <sub>n</sub>                          | —  | —  | —                        |    | 13                     |    | 0                        |    | 0                     |    |
| I <sub>012</sub>                        | —  | —  | —                        |    | 19                     |    | 0                        |    | 0                     |    |
| I <sub>345</sub>                        | —  | —  | —                        |    | 19                     |    | 0                        |    | 0                     |    |
| I <sub>678</sub>                        | 7  | 9  | ← Do Not Change →        |    |                        |    |                          |    | 0                     |    |
| RAM <sub>0, 3</sub> , Q <sub>0, 3</sub> | —  | —  | —                        |    | 9                      |    | 0                        |    | 0                     |    |

**Output Enable/Disable Times<sup>[5]</sup>**

Output disable tests performed with C<sub>L</sub> = 5 pF and measured to 0.5V change of output voltage level.

| Device     | Input | Output | Enable | Disable |
|------------|-------|--------|--------|---------|
| CY7C901-23 | OE    | Y      | 14     | 16      |
| CY7C901-27 | OE    | Y      | 16     | 18      |

**Notes:**

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".

3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.
5. See the last page of this specification for Group A subgroup testing information.


## CY7C901-31 Commercial and CY7C901-32 Military AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Commercial (0°C to 70°C) and Military (-55°C to +125°C) operating temperature range with  $V_{CC}$  varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See "Electrical Characteristics" for loading circuit information.

This data applies to parts with the following numbers:

CY7C901-31PC CY7C901-31DC CY7C901-31LC CY7C901-31JC CY7C901-32DMB CY7C901-32LMB

### Combinational Propagation Delays. $C_L = 50 \text{ pF}^{[5]}$

| To Output   | Y   |     | F <sub>3</sub> |     | C <sub>n+4</sub> |     | $\bar{G}, \bar{P}$ |     | F = 0 |     | OVR |     | RAM <sub>0</sub><br>RAM <sub>3</sub> |     | Q <sub>0</sub><br>Q <sub>3</sub> |     |
|---|-----|-----|----------------|-----|------------------|-----|--------------------|-----|-------|-----|-----|-----|--------------------------------------|-----|----------------------------------|-----|
| From Input  | -31 | -32 | -31            | -32 | -31              | -32 | -31                | -32 | -31   | -32 | -31 | -32 | -31                                  | -32 | -31                              | -32 |
| A, B Address  | 40  | 48  | 40             | 48  | 40               | 48  | 37                 | 44  | 40    | 48  | 40  | 48  | 40                                   | 48  | —                                | —   |
| D   | 30  | 37  | 30             | 37  | 30               | 37  | 30                 | 34  | 38    | 40  | 30  | 37  | 30                                   | 37  | —                                | —   |
| C <sub>n</sub>  | 22  | 25  | 22             | 25  | 20               | 21  | —                  | —   | 25    | 28  | 22  | 25  | 25                                   | 28  | —                                | —   |
| I <sub>012</sub>  | 35  | 40  | 35             | 40  | 35               | 40  | 37                 | 44  | 37    | 44  | 35  | 40  | 35                                   | 40  | —                                | —   |
| I <sub>345</sub>  | 35  | 40  | 35             | 40  | 35               | 40  | 35                 | 40  | 38    | 40  | 35  | 40  | 35                                   | 40  | —                                | —   |
| I <sub>678</sub>  | 25  | 29  | —              | —   | —                | —   | —                  | —   | —     | —   | —   | —   | 26                                   | 29  | 26                               | 29  |
| A Bypass ALU<br>(I = 2XX)   | 35  | 40  | —              | —   | —                | —   | —                  | —   | —     | —   | —   | —   | —                                    | —   | —                                | —   |
| Clock  | 35  | 40  | 35             | 40  | 35               | 40  | 35                 | 40  | 35    | 40  | 35  | 40  | 35                                   | 40  | 28                               | 33  |

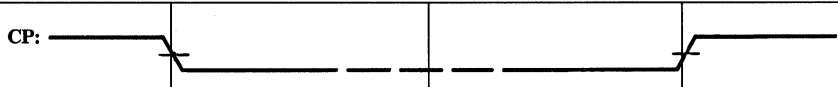
### Cycle Time and Clock Characteristics<sup>[5]</sup>

| CY7C901-  | -31    | -32    |
|---|--------|--------|
| Read-Modify-Write Cycle (from selection of A, B registers to end of cycle). | 31 ns  | 32 ns  |
| Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)         | 32 MHz | 31 MHz |
| Minimum Clock LOW Time  | 16 ns  | 17 ns  |
| Minimum Clock HIGH Time   | 15 ns  | 15 ns  |
| Minimum Clock Period  | 31 ns  | 32 ns  |

For faster performance see CY7C901-23 specification on page 9.

**5**

### Set-up and Hold Times Relative to Clock (CP) Input<sup>[5]</sup>

| Input                                   | CP:  |                          |                                       |                          |
|---|--|--------------------------|---------------------------------------|--------------------------|
|   | Set-up Time<br>Before H → L  | Hold Time<br>After H → L | Set-up Time<br>Before L → H           | Hold Time<br>After L → H |
| A, B Source Address                     | 15   | 0<br>(Note 3)            | 30, 15 + t <sub>PWL</sub><br>(Note 4) | 0                        |
| B Destination Address                   | 15   | ← Do Not Change →        |                                       | 0                        |
| D                                       | —  | —                        | 25                                    | 0                        |
| C <sub>n</sub>                          | —  | —                        | 20                                    | 0                        |
| I <sub>012</sub>                        | —  | —                        | 30                                    | 0                        |
| I <sub>345</sub>                        | —  | —                        | 30                                    | 0                        |
| I <sub>678</sub>                        | 10   | ← Do Not Change →        |                                       | 0                        |
| RAM <sub>0, 3</sub> , Q <sub>0, 3</sub> | —  | —                        | 12                                    | 0                        |

### Output Enable/Disable Times<sup>[5]</sup>

Output disable tests performed with  $C_L = 5 \text{ pF}$  and measured to 0.5V change of output voltage level.

| Device     | Input      | Output | Enable | Disable |
|------------|------------|--------|--------|---------|
| CY7C901-31 | OE         | Y      | 23     | 23      |
| CY7C901-32 | $\bar{O}E$ | Y      | 25     | 25      |

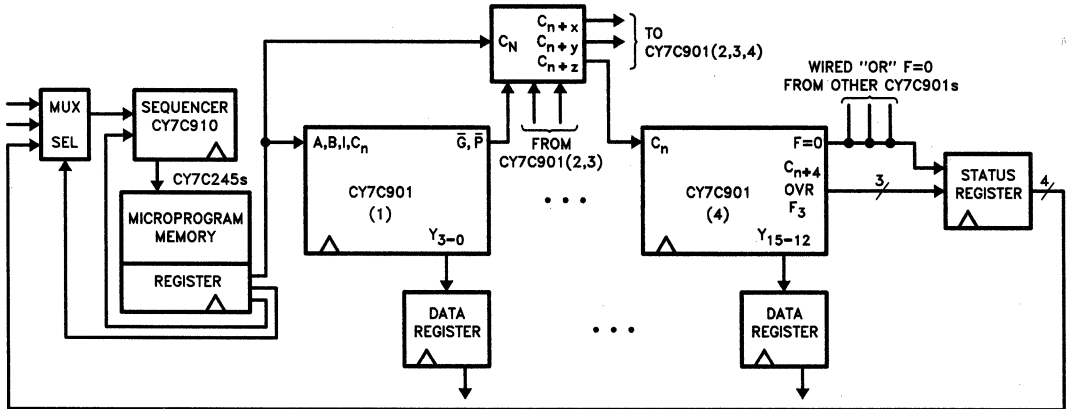
#### Notes:

- A dash indicates a propagation delay path or set-up time constraint does not exist.
- Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".

- Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
- The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.
- See the last page of this specification for Group A subgroup testing information.

## Minimum Cycle Time Calculations for 16-Bit Systems

Speed used in calculations for parts other than CY7C901 are representative for MSI parts.

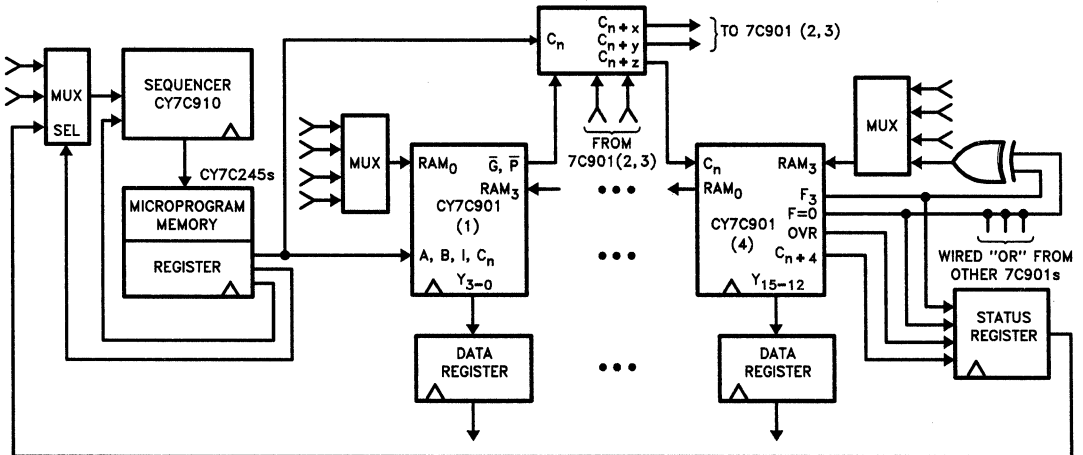


**Pipelined System, Add without Simultaneous Shift**

0030-11

| Data Loop   |  |              | Control Loop |                  |       |
|-------------|--|--------------|--------------|------------------|-------|
| CY7C245     | Clock to Output                        | 12           | CY7C245      | Clock to Output  | 12    |
| CY7C901     | A, B to $\bar{G}$ , P                  | 28           | MUX          | Select to Output | 12    |
| Carry Logic | $\bar{G}_0$ , $\bar{P}_0$ to $C_n + Z$ | 9            | CY7C910      | CC to Output     | 22    |
| CY7C901     | $C_n$ to Worst Case                    | 18           | CY7C245      | Access Time      | 20    |
| Register    | Setup                                  | 4            |              |                  | 66 ns |
|             |  | <u>71 ns</u> |              |                  |       |

**Minimum Clock Period = 71 ns**



**Pipelined System, Simultaneous Add and Shift Down (RIGHT)**

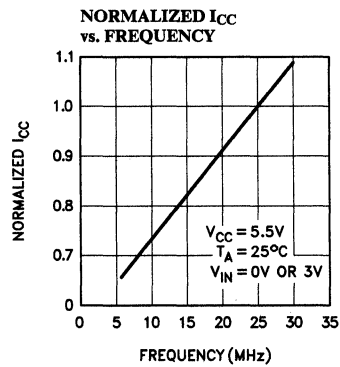
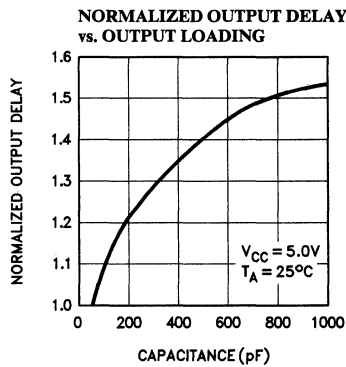
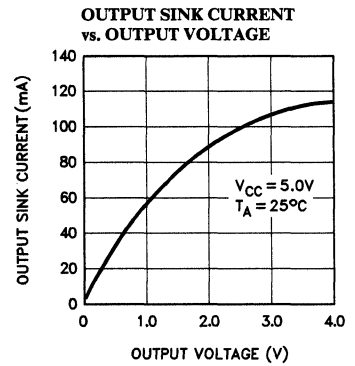
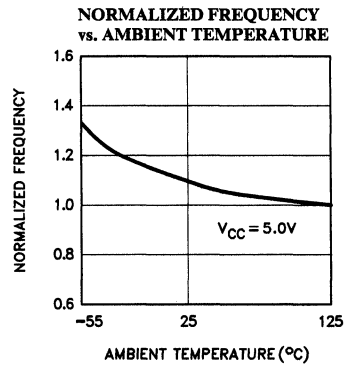
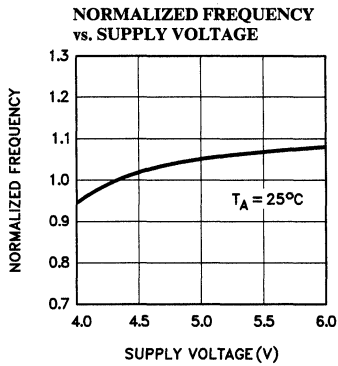
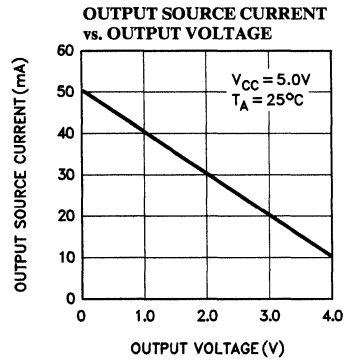
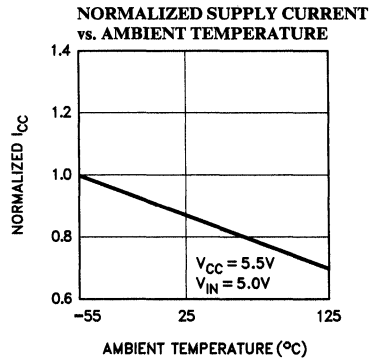
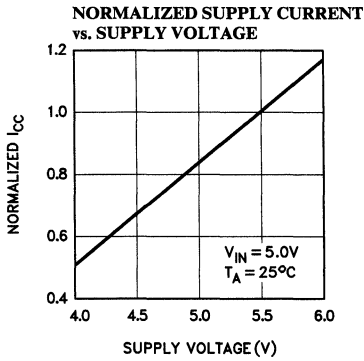
0030-12

| Data Loop   |  |              | Control Loop |                  |       |
|-------------|--|--------------|--------------|------------------|-------|
| CY7C245     | Clock to Output                        | 12           | CY7C245      | Clock to Output  | 12    |
| CY7C901     | A, B to $\bar{G}$ , P                  | 28           | MUX          | Select to Output | 12    |
| Carry Logic | $\bar{G}_0$ , $\bar{P}_0$ to $C_n + Z$ | 9            | CY7C910      | CC to Output     | 22    |
| CY7C901     | $C_n$ to Worst Case                    | 18           | CY7C245      | Access Time      | 20    |
| XOR and MUX | Prop. Delay, Select to Output          | 20           |              |                  | 66 ns |
| CY7C901     | RAM <sub>3</sub> Setup                 | 9            |              |                  |       |
|             |  | <u>96 ns</u> |              |                  |       |

**Minimum Clock Period = 96 ns**

Typical DC and AC Characteristics

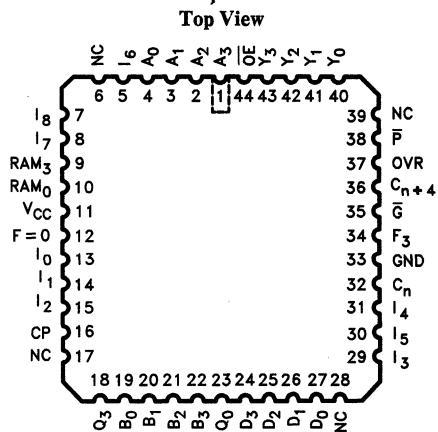
5



### Ordering Information

| Read Modify-Write Cycle (ns) | Ordering Code | Package Type | Operating Range |
|------------------------------|---------------|--------------|-----------------|
| 23                           | CY7C901-23PC  | P17          | Commercial      |
|                              | CY7C901-23DC  | D18          | Commercial      |
|                              | CY7C901-23JC  | J67          | Commercial      |
|                              | CY7C901-23LC  | L67          | Commercial      |
| 27                           | CY7C901-27DMB | D18          | Military        |
|                              | CY7C901-27LMB | L67          | Military        |
| 31                           | CY7C901-31PC  | P17          | Commercial      |
|                              | CY7C901-31DC  | D18          | Commercial      |
|                              | CY7C901-31JC  | J67          | Commercial      |
|                              | CY7C901-31LC  | L67          | Commercial      |
| 32                           | CY7C901-32DMB | D18          | Military        |
|                              | CY7C901-32LMB | L67          | Military        |

### Pin Configuration



0030-9

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>Ix</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>sc</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>CC1</sub>     | 1,2,3     |

**Cycle Time and Clock Characteristics**

| Parameters              | Subgroups   |
|-------------------------|-------------|
| Minimum Clock LOW Time  | 7,8,9,10,11 |
| Minimum Clock HIGH Time | 7,8,9,10,11 |

**Combinational Propagation Delays**

| Parameters   | Subgroups   |
|--|-------------|
| From A, B Address to Y                               | 7,8,9,10,11 |
| From A, B Address to F <sub>3</sub>                  | 7,8,9,10,11 |
| From A, B Address to C <sub>n+4</sub>                | 7,8,9,10,11 |
| From A, B Address to $\overline{G}$ , $\overline{P}$ | 7,8,9,10,11 |
| From A, B Address to F=0                             | 7,8,9,10,11 |
| From A, B Address to OVR                             | 7,8,9,10,11 |
| From A, B Address to RAM <sub>0,3</sub>              | 7,8,9,10,11 |
| From D to Y  | 7,8,9,10,11 |
| From D to F <sub>3</sub>                             | 7,8,9,10,11 |
| From D to C <sub>n+4</sub>                           | 7,8,9,10,11 |
| From D to $\overline{G}$ , $\overline{P}$            | 7,8,9,10,11 |
| From D to F = 0                                      | 7,8,9,10,11 |
| From D to OVR  | 7,8,9,10,11 |
| From D to RAM <sub>0,3</sub>                         | 7,8,9,10,11 |
| From C <sub>n</sub> to Y                             | 7,8,9,10,11 |
| From C <sub>n</sub> to F <sub>3</sub>                | 7,8,9,10,11 |

**Combinational Propagation Delays (Continued)**

| Parameters   | Subgroups   |
|--|-------------|
| From C <sub>n</sub> to C <sub>n+4</sub>                          | 7,8,9,10,11 |
| From C <sub>n</sub> to F = 0                                     | 7,8,9,10,11 |
| From C <sub>n</sub> to OVR                                       | 7,8,9,10,11 |
| From C <sub>n</sub> to RAM <sub>0,3</sub>                        | 7,8,9,10,11 |
| From I <sub>012</sub> to Y                                       | 7,8,9,10,11 |
| From I <sub>012</sub> to F <sub>3</sub>                          | 7,8,9,10,11 |
| From I <sub>012</sub> to C <sub>n+4</sub>                        | 7,8,9,10,11 |
| From I <sub>012</sub> to $\overline{G}$ , $\overline{P}$         | 7,8,9,10,11 |
| From I <sub>012</sub> to F=0                                     | 7,8,9,10,11 |
| From I <sub>012</sub> to OVR                                     | 7,8,9,10,11 |
| From I <sub>012</sub> to RAM <sub>0,3</sub>                      | 7,8,9,10,11 |
| From I <sub>345</sub> to Y                                       | 7,8,9,10,11 |
| From I <sub>345</sub> to F <sub>3</sub>                          | 7,8,9,10,11 |
| From I <sub>345</sub> to C <sub>n+4</sub>                        | 7,8,9,10,11 |
| From I <sub>345</sub> to $\overline{G}$ , $\overline{P}$         | 7,8,9,10,11 |
| From I <sub>345</sub> to F=0                                     | 7,8,9,10,11 |
| From I <sub>345</sub> to OVR                                     | 7,8,9,10,11 |
| From I <sub>345</sub> to RAM <sub>0,3</sub>                      | 7,8,9,10,11 |
| From I <sub>678</sub> to Y                                       | 7,8,9,10,11 |
| From I <sub>678</sub> to RAM <sub>0,3</sub>                      | 7,8,9,10,11 |
| From I <sub>678</sub> to Q <sub>0,3</sub>                        | 7,8,9,10,11 |
| From A Bypass ALU to Y<br>(I = 2XX)                              | 7,8,9,10,11 |
| From Clock $\curvearrowright$ to Y                               | 7,8,9,10,11 |
| From Clock $\curvearrowright$ to F <sub>3</sub>                  | 7,8,9,10,11 |
| From Clock $\curvearrowright$ to C <sub>n+4</sub>                | 7,8,9,10,11 |
| From Clock $\curvearrowright$ to $\overline{G}$ , $\overline{P}$ | 7,8,9,10,11 |
| From Clock $\curvearrowright$ to F=0                             | 7,8,9,10,11 |
| From Clock $\curvearrowright$ to OVR                             | 7,8,9,10,11 |
| From Clock $\curvearrowright$ to RAM <sub>0,3</sub>              | 7,8,9,10,11 |
| From Clock $\curvearrowright$ to Q <sub>0,3</sub>                | 7,8,9,10,11 |



**Set-up and Hold Times Relative to Clock (CP) Input**

| Parameters  | Subgroups   |
|---|-------------|
| A, B Source Address<br>Set-up Time Before H → L   | 7,8,9,10,11 |
| A, B Source Address<br>Hold Time After H → L      | 7,8,9,10,11 |
| A, B Source Address<br>Set-up Time Before L → H   | 7,8,9,10,11 |
| A, B Source Address<br>Hold Time After L → H      | 7,8,9,10,11 |
| B Destination Address<br>Set-up Time Before H → L | 7,8,9,10,11 |
| B Destination Address<br>Hold Time After H → L    | 7,8,9,10,11 |
| B Destination Address<br>Set-up Time Before L → H | 7,8,9,10,11 |
| B Destination Address<br>Hold Time After L → H    | 7,8,9,10,11 |
| D Set-up Time Before L → H                        | 7,8,9,10,11 |

| Parameters  | Subgroups   |
|---|-------------|
| D Hold Time After L → H   | 7,8,9,10,11 |
| C <sub>n</sub> Set-up Time Before L → H   | 7,8,9,10,11 |
| C <sub>n</sub> Hold Time After L → H  | 7,8,9,10,11 |
| I <sub>012</sub> Set-up Time Before L → H   | 7,8,9,10,11 |
| I <sub>012</sub> Hold Time After L → H  | 7,8,9,10,11 |
| I <sub>345</sub> Set-up Time Before L → H   | 7,8,9,10,11 |
| I <sub>345</sub> Hold Time After L → H  | 7,8,9,10,11 |
| I <sub>678</sub> Set-up Time Before H → L   | 7,8,9,10,11 |
| I <sub>678</sub> Hold Time After H → L  | 7,8,9,10,11 |
| I <sub>678</sub> Set-up Time Before L → H   | 7,8,9,10,11 |
| I <sub>678</sub> Hold Time After L → H  | 7,8,9,10,11 |
| RAM <sub>0</sub> , RAM <sub>3</sub> , Q <sub>0</sub> , Q <sub>3</sub><br>Set-up Time Before L → H | 7,8,9,10,11 |
| RAM <sub>0</sub> , RAM <sub>3</sub> , Q <sub>0</sub> , Q <sub>3</sub><br>Hold Time After L → H    | 7,8,9,10,11 |

Document #: 38-00021-B



**Features**

- **Fast**  
— CY7C909/11 has a 30 ns (min.) clock to output cycle time; commercial and military
- **Low Power**  
—  $I_{CC} (max.) = 55 \text{ mA}$ ; commercial and military
- **V<sub>CC</sub> margin**  
—  $5 \text{ V} \pm 10\%$   
— All parameters guaranteed over commercial and military operating temperature range
- **Expandable**  
Infinitely expandable in 4-bit increments

- **Capable of withstanding greater than 2000V static discharge voltage**
- **Pin compatible and functional equivalent to 2909A/2911A**

**Description**

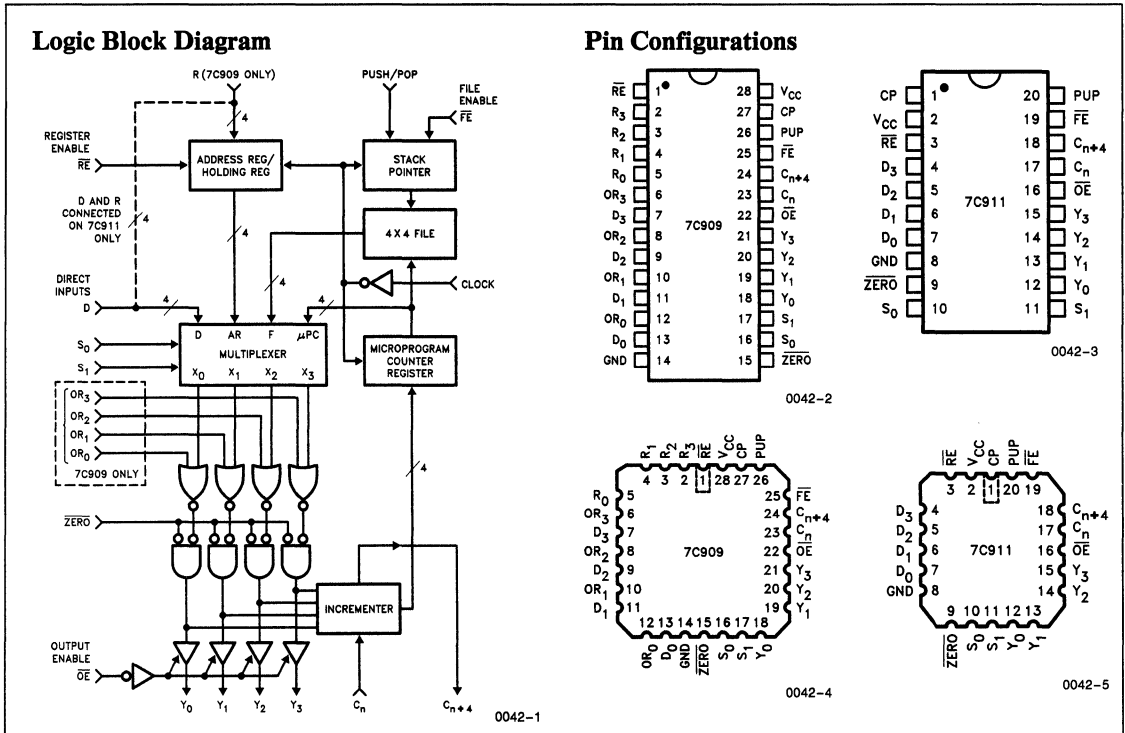
The CY7C909 and CY7C911 are high-speed, four-bit wide address sequencers intended for controlling the sequence of execution of microinstructions contained in microprogram memory. They may be connected in parallel to expand the address width in 4 bit increments. Both devices are implemented in high performance CMOS for optimum speed and power.

The CY7C909 can select an address from any of four sources. They are:

1) a set of four external direct inputs (D<sub>i</sub>); 2) external data stored in an internal register (R<sub>i</sub>); 3) a four word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs (Y<sub>i</sub>) can be OR'ed with an external input for conditional skip or branch instructions. A ZERO input line forces the outputs to all zeros. The outputs are three state, controlled by the Output Enable (OE) input.

The CY7C911 is an identical circuit to the CY7C909, except the four OR inputs are removed and the D and R inputs are tied together. The CY7C911 is available in a 20-pin, 300-mil package.

5



### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                 |
|---|-----------------|
| Storage Temperature .....                             | -65°C to +150°C |
| Ambient Temperature with<br>Power Applied .....       | -55°C to +125°C |
| Supply Voltage to Ground Potential ....               | -0.5V to +7.0V  |
| DC Voltage Applied to Outputs<br>in High Z State..... | -0.5V to +7.0V  |
| DC Input Voltage .....                                | -3.0V to +7.0V  |
| Output Current, into Outputs (Low) .....              | 30 mA           |

|                                |  |
|--------------------------------|--|
| Static Discharge Voltage ..... | > 2001V<br>(per MIL-STD-883 Method 3015) |
| Latch-Up Current .....         | > 200 mA                                 |

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Operating Range<sup>[4]</sup>

| Parameters       | Description                                    | Test Conditions  | Min.       | Max.            | Units |
|------------------|--|--|------------|-----------------|-------|
| V <sub>OH</sub>  | Output HIGH Voltage                            | V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.6 mA (Comm.)                | 2.4        |                 | V     |
|                  |  | V <sub>CC</sub> = Min., I <sub>OH</sub> = -1.0 mA (Mil.)                 | 2.4        |                 | V     |
| V <sub>OL</sub>  | Output LOW Voltage                             | V <sub>CC</sub> = Min., I <sub>OL</sub> = 16.0 mA                        |            | 0.4             | V     |
| V <sub>IH</sub>  | Input High Voltage                             |  | 2.0        | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Input Low Voltage                              |  | -2.0       | 0.8             | V     |
| I <sub>IX</sub>  | Input Load Current                             | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                                   | -10        | +10             | μA    |
| I <sub>OZ</sub>  | Output Leakage Current                         | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub><br>Output Disabled                | -20        | +20             | μA    |
| I <sub>OS</sub>  | Output Short <sup>[1]</sup><br>Circuit Current | V <sub>CC</sub> = Max.      V <sub>OUT</sub> = GND                       | -30        | -85             | mA    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating<br>Supply Current    | V <sub>CC</sub> = Max.<br>I <sub>OUT</sub> = 0 mA                        | Commercial | 55              | mA    |
|                  |  |  | Military   | 55              |       |
| I <sub>CC1</sub> | V <sub>CC</sub> Operating<br>Supply Current    | V <sub>CC</sub> = Max.<br>V <sub>IH</sub> ≥ 3.0V, V <sub>IL</sub> ≤ 0.4V | Commercial | 35              | mA    |
|                  |  |  | Military   | 35              |       |

### Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 5    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 7    |       |

#### Notes:

- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

### AC Test Loads and Waveforms

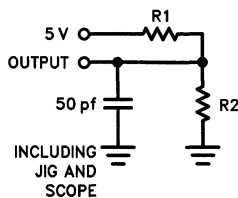


Figure 1a

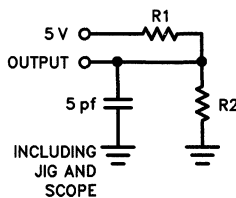


Figure 1b

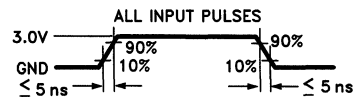


Figure 2

0042-7

0042-6

|                | Commercial | Military |
|----------------|------------|----------|
| R <sub>1</sub> | 254Ω       | 258Ω     |
| R <sub>2</sub> | 187Ω       | 216Ω     |

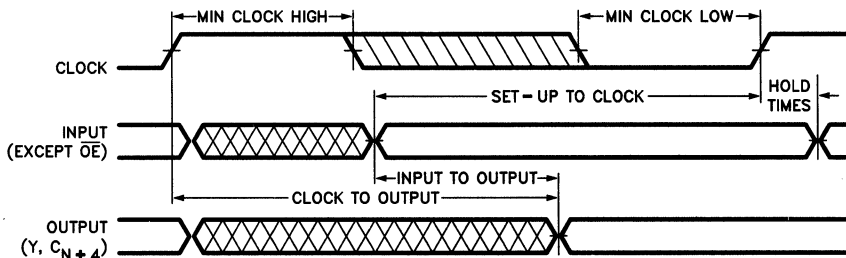
**Switching Characteristics Over Operating Range<sup>[4, 5]</sup>**

|   | 7C909-30<br>7C911-30 |                    | 7C909-30<br>7C911-30 |                    | 7C909-40<br>7C911-40 |                    | 7C909-40<br>7C911-40 |                    | Units |
|---|----------------------|--------------------|----------------------|--------------------|----------------------|--------------------|----------------------|--------------------|-------|
|   | Commercial           |                    | Military             |                    | Commercial           |                    | Military             |                    |       |
| Minimum Clock Low Time  | 15                   |                    | 15                   |                    | 20                   |                    | 20                   |                    | ns    |
| Minimum Clock High Time   | 15                   |                    | 15                   |                    | 20                   |                    | 20                   |                    | ns    |
| <b>MAXIMUM COMBINATIONAL PROPAGATION DELAYS</b>   |                      |                    |                      |                    |                      |                    |                      |                    |       |
| <b>From Input To:</b>   | Y                    | C <sub>N</sub> + 4 | Y                    | C <sub>N</sub> + 4 | Y                    | C <sub>N</sub> + 4 | Y                    | C <sub>N</sub> + 4 | ns    |
| D <sub>i</sub>  | 17                   | 18                 | 18                   | 19                 | 17                   | 22                 | 20                   | 25                 | ns    |
| S <sub>0</sub> , S <sub>1</sub>   | 18                   | 18                 | 20                   | 20                 | 29                   | 34                 | 29                   | 34                 | ns    |
| OR <sub>i</sub> (7C909)   | 16                   | 16                 | 17                   | 17                 | 17                   | 22                 | 20                   | 25                 | ns    |
| C <sub>N</sub>  | —                    | 13                 | —                    | 15                 | —                    | 14                 | —                    | 16                 | ns    |
| ZERØ  | 18                   | 18                 | 20                   | 20                 | 29                   | 34                 | 30                   | 35                 | ns    |
| OE Low to Output  | 16                   | —                  | 18                   | —                  | 25                   | —                  | 25                   | —                  | ns    |
| OE HIGH to HIGH Z <sup>[5]</sup>  | 16                   | —                  | 18                   | —                  | 25                   | —                  | 25                   | —                  | ns    |
| Clock HIGH, S <sub>1</sub> , S <sub>0</sub> = LH  | 20                   | 20                 | 22                   | 22                 | 39                   | 44                 | 45                   | 50                 | ns    |
| Clock HIGH, S <sub>1</sub> , S <sub>0</sub> = LL  | 20                   | 20                 | 22                   | 22                 | 39                   | 44                 | 45                   | 50                 | ns    |
| Clock HIGH, S <sub>1</sub> , S <sub>0</sub> = HL  | 20                   | 20                 | 22                   | 22                 | 44                   | 49                 | 53                   | 58                 | ns    |
| <b>MINIMUM SET-UP AND HOLD TIMES (All Times Relative to Clock LOW to HIGH Transition)</b> |                      |                    |                      |                    |                      |                    |                      |                    |       |
| <b>From Input</b>   | <b>Set-up</b>        | <b>Hold</b>        | <b>Set-up</b>        | <b>Hold</b>        | <b>Set-up</b>        | <b>Hold</b>        | <b>Set-up</b>        | <b>Hold</b>        |       |
| RE  | 11                   | 0                  | 12                   | 0                  | 19                   | 0                  | 19                   | 0                  | ns    |
| R <sub>i</sub> [6]  | 10                   | 0                  | 11                   | 0                  | 10                   | 0                  | 12                   | 0                  | ns    |
| Push/Pop  | 12                   | 0                  | 13                   | 0                  | 25                   | 0                  | 27                   | 0                  | ns    |
| FE  | 12                   | 0                  | 13                   | 0                  | 25                   | 0                  | 27                   | 0                  | ns    |
| C <sub>N</sub>  | 10                   | 0                  | 11                   | 0                  | 18                   | 0                  | 18                   | 0                  | ns    |
| D <sub>i</sub>  | 14                   | 0                  | 16                   | 0                  | 25                   | 0                  | 25                   | 0                  | ns    |
| OR <sub>i</sub> (7C909)   | 12                   | 0                  | 14                   | 0                  | 25                   | 0                  | 25                   | 0                  | ns    |
| S <sub>0</sub> , S <sub>1</sub>   | 14                   | 0                  | 16                   | 0                  | 25                   | 0                  | 29                   | 0                  | ns    |
| ZERØ  | 12                   | 0                  | 13                   | 0                  | 25                   | 0                  | 29                   | 0                  | ns    |

**Notes:**

- Output Loading as in Figure 1b.
- R<sub>i</sub> and D<sub>i</sub> are internally connected on the CY7C911. Use R<sub>i</sub> set-up and hold times when D<sub>i</sub> inputs are used to load register.
- System clock cycle time (Clock Low Time and Clock High Time) cannot be less than maximum propagation delay.

**Switching Waveforms**



0042-8

## Functional Description

The tables below define the control logic of the 7C909/911. Table 1 contains the Multiplexer Control Logic which selects the address source to appear on the outputs.

**Table 1. Address Source Selection**

| OCTAL | S <sub>1</sub> | S <sub>0</sub> | SOURCE FOR Y OUTPUTS             |
|-------|----------------|----------------|----------------------------------|
| 0     | L              | L              | Microprogram Counter ( $\mu$ PC) |
| 1     | L              | H              | Address/Holding Register (AR)    |
| 2     | H              | L              | Push-Pop stack (STK)             |
| 3     | H              | H              | Direct inputs (D <sub>i</sub> )  |

Control of the Push/Pop Stack is contained in Table 2. FILE ENABLE (FE) enables stack operations, while Push/Pop (PUP) controls the stack.

**Table 2. Synchronous Stack Control**

| FE | PUP | PUSH-POP STACK CHANGE                                 |
|----|-----|---|
| H  | X   | No change   |
| L  | H   | Push current PC into stack<br>increment stack pointer |
| L  | L   | pop stack, decrement stack pointer                    |

Table 3 illustrates the Output Control Logic of the 7C909/911. The ZERO control forces the outputs to zero. The OR inputs are OR'ed with the output of the multiplexer.

**Table 3. Output Control**

| OR <sub>i</sub> | ZERO | OE | Y <sub>i</sub>                                   |
|-----------------|------|----|--|
| X               | X    | H  | High Z   |
| X               | L    | L  | L  |
| H               | H    | L  | H  |
| L               | H    | L  | Source selected by S <sub>0</sub> S <sub>1</sub> |

Table 4 defines the effect of S<sub>0</sub>, S<sub>1</sub>, FE and PUP control signals on the 7C909. It illustrates the Address Source on the outputs and the contents of the Internal Registers for every combination of these signals. The Internal Register contents are illustrated before and after the Clock LOW to HIGH edge.

**Table 4**

| CYCLE      | S <sub>1</sub> , S <sub>0</sub> , FE, PUP | $\mu$ PC    | REG    | STK0     | STK1     | STK2     | STK3     | YOUT    | COMMENT                                   | PRINCIPLE USE    |
|------------|---|-------------|--------|----------|----------|----------|----------|---------|---|------------------|
| N<br>N + 1 | 0000<br>—                                 | J<br>J + 1  | K<br>K | Ra<br>Rb | Rb<br>Rc | Rc<br>Rd | Rd<br>Ra | J<br>—  | Pop Stack                                 | End Loop         |
| N<br>N + 1 | 0001<br>—                                 | J<br>J + 1  | K<br>K | Ra<br>J  | Rb<br>Ra | Rc<br>Rb | Rd<br>Rc | J<br>—  | Push $\mu$ PC                             | Set-up Loop      |
| N<br>N + 1 | 001X<br>—                                 | J<br>J + 1  | K<br>K | Ra<br>Ra | Rb<br>Rb | Rc<br>Rc | Rd<br>Rd | J<br>—  | Continue                                  | Continue         |
| N<br>N + 1 | 0100<br>—                                 | J<br>K + 1  | K<br>K | Ra<br>Rb | Rb<br>Rc | Rc<br>Rd | Rd<br>Ra | K<br>—  | Use AR for Address;<br>Pop Stack          | End Loop         |
| N<br>N + 1 | 0101<br>—                                 | J<br>K + 1  | K<br>K | Ra<br>J  | Rb<br>Ra | Rc<br>Rb | Rd<br>Rc | K<br>—  | Jump to Address in AR;<br>Push $\mu$ PC   | JSR AR           |
| N<br>N + 1 | 011X<br>—                                 | J<br>K + 1  | K<br>K | Ra<br>Ra | Rb<br>Rb | Rc<br>Rc | Rd<br>Rd | K<br>—  | Jump to Address in AR                     | JMP AR           |
| N<br>N + 1 | 1000<br>—                                 | J<br>Ra + 1 | K<br>K | Ra<br>Rb | Rb<br>Rc | Rc<br>Rd | Rd<br>Ra | Ra<br>— | Jump to Address in STK0;<br>Pop Stack     | RTS              |
| N<br>N + 1 | 1001<br>—                                 | J<br>Ra + 1 | K<br>K | Ra<br>J  | Rb<br>Ra | Rc<br>Rb | Rd<br>Rc | Ra<br>— | Jump to Address in STK0;<br>Push $\mu$ PC |                  |
| N<br>N + 1 | 101X<br>—                                 | J<br>Ra + 1 | K<br>K | Ra<br>Ra | Rb<br>Rb | Rc<br>Rc | Rd<br>Rd | Ra<br>— | Jump to Address in STK0                   | Stack Ref (Loop) |
| N<br>N + 1 | 1100<br>—                                 | J<br>D + 1  | K<br>K | Ra<br>Rb | Rb<br>Rc | Rc<br>Rd | Rd<br>Ra | D<br>—  | Jump to Address on D;<br>Pop Stack        | End Loop         |
| N<br>N + 1 | 1101<br>—                                 | J<br>D + 1  | K<br>K | Ra<br>J  | Rb<br>Ra | Rc<br>Rb | Rd<br>Rc | D<br>—  | Jump to Address on D;<br>Push $\mu$ PC    | JSR D            |
| N<br>N + 1 | 111X<br>—                                 | J<br>D + 1  | K<br>K | Ra<br>Ra | Rb<br>Rb | Rc<br>Rc | Rd<br>Rd | D<br>—  | Jump to Address on D                      | JMP D            |

J = Contents of Microprogram Counter

K = Contents of Address Register

R<sub>a</sub>, R<sub>b</sub>, R<sub>c</sub>, R<sub>d</sub> = Contents in Stack

### Functional Description (Continued)

Two examples of Subroutine Execution appear below. *Figure 3* illustrates a single subroutine while *Figure 4* illustrates two nested subroutines.

The instruction being executed at any given time is the one contained in the microword register ( $\mu$ WR). The contents of the  $\mu$ WR also controls the four signals  $S_0$ ,  $S_1$ ,  $\overline{FE}$ , and PUP. The starting address of the subroutine is applied to the D inputs of the 7C909 at the appropriate time.

In the columns on the left is the sequence of microinstructions to be executed. At address  $J + 2$ , the sequence control portion of the microinstruction contains the command

“Jump to sub-routine at A”. At the time  $T_2$ , this instruction is in the  $\mu$ WR, and the 7C909 inputs are set-up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the  $\mu$ WR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the  $\mu$ WR. On the next clock transition, I(A) is loaded into the  $\mu$ WR for execution, and the return address  $J + 3$  is pushed onto the stack. The return instruction is executed at  $T_5$ . *Figure 4* is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

#### CONTROL MEMORY

| Execute Cycle | Microprogram |                       | Execute Cycle | Clock Signals | $S_1, S_0$ | FE | PUP | D   | $\mu$ PC | STK0 | STK1 | STK2 | STK3 | Y   | ROM Output | Contents of $\mu$ WR (Instruction being executed) |  |  |  |
|---------------|--------------|-----------------------|---------------|---------------|------------|----|-----|-----|----------|------|------|------|------|-----|------------|---|--|--|--|
|               | Address      | Sequencer Instruction |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
| $T_0$         | J-1          | -                     | $T_0$         |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
| $T_1$         | J            | -                     | $T_1$         | 0             | 0          | H  | X   | J+1 | -        | -    | -    | -    | -    | J+1 | I(J+1)     | I(J)  |  |  |  |
| $T_2$         | J+1          | -                     | $T_2$         | 3             | L          | H  | X   | J+2 | -        | -    | -    | -    | -    | J+2 | JSR A      | I(J+1)  |  |  |  |
| $T_3$         | J+2          | JSR A                 | $T_3$         | 0             | H          | X  | X   | J+3 | -        | -    | -    | -    | -    | A   | I(A)       | JSR A   |  |  |  |
| $T_4$         | J+3          | -                     | $T_4$         | 0             | H          | X  | X   | A+1 | J+3      | -    | -    | -    | -    | A+1 | I(A+1)     | I(A)  |  |  |  |
| $T_5$         | J+4          | -                     | $T_5$         | 2             | L          | H  | X   | A+2 | J+3      | -    | -    | -    | -    | A+2 | RTS        | I(A+1)  |  |  |  |
| $T_6$         | -            | -                     | $T_6$         | 0             | H          | X  | X   | A+3 | -        | -    | -    | -    | -    | J+3 | I(J+3)     | RTS   |  |  |  |
| $T_7$         | -            | -                     | $T_7$         | 0             | H          | X  | X   | J+4 | -        | -    | -    | -    | -    | J+4 | I(J+4)     | I(J+3)  |  |  |  |
| $T_8$         | -            | -                     | $T_8$         | 0             | H          | X  | X   | J+5 | -        | -    | -    | -    | -    | J+5 | I(J+5)     | I(J+4)  |  |  |  |
| $T_9$         | -            | -                     | $T_9$         | -             | -          | -  | -   | -   | -        | -    | -    | -    | -    | -   | -          | -   |  |  |  |
| $T_3$         | A            | I(A)                  |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
| $T_4$         | A+1          | -                     |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
| $T_5$         | A+2          | RTS                   |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
|               | -            | -                     |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
|               | -            | -                     |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
|               | -            | -                     |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
|               | -            | -                     |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |

Figure 3. Subroutine Execution.

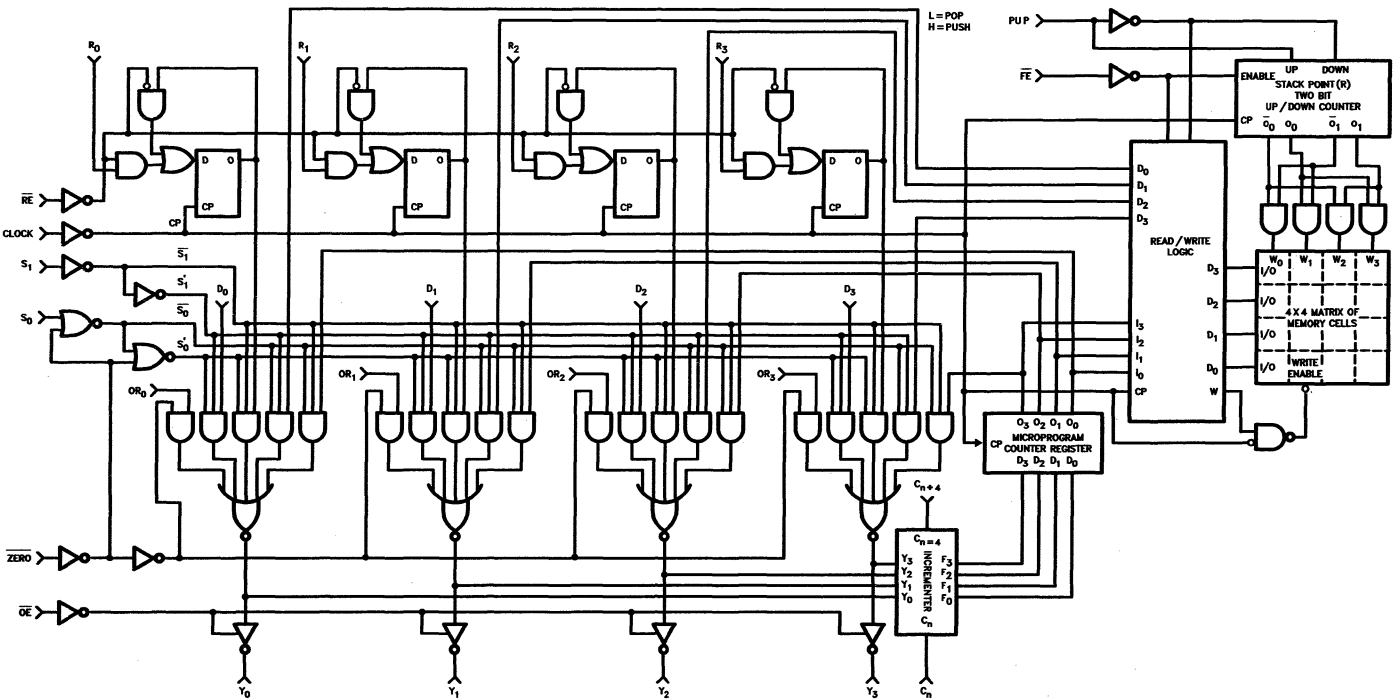
$C_n = \text{HIGH}$

#### CONTROL MEMORY

| Execute Cycle | Microprogram |                       | Execute Cycle | Clock Signals | $S_1, S_0$ | FE | PUP | D   | $\mu$ PC | STK0 | STK1 | STK2 | STK3 | Y   | ROM Output | Contents of $\mu$ WR (Instruction being executed) |  |  |  |
|---------------|--------------|-----------------------|---------------|---------------|------------|----|-----|-----|----------|------|------|------|------|-----|------------|---|--|--|--|
|               | Address      | Sequencer Instruction |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
| $T_0$         | J-1          | -                     | $T_0$         |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
| $T_1$         | J            | -                     | $T_1$         | 0             | 0          | H  | X   | J+1 | -        | -    | -    | -    | -    | J+1 | I(J+1)     | I(J)  |  |  |  |
| $T_2$         | J+1          | -                     | $T_2$         | 3             | L          | H  | X   | J+2 | -        | -    | -    | -    | -    | J+2 | JSR A      | I(J+1)  |  |  |  |
| $T_3$         | J+2          | JSR A                 | $T_3$         | 0             | H          | X  | X   | J+3 | -        | -    | -    | -    | -    | A   | I(A)       | JSR A   |  |  |  |
| $T_4$         | J+3          | -                     | $T_4$         | 0             | H          | X  | X   | A+1 | J+3      | -    | -    | -    | -    | A+1 | I(A+1)     | I(A)  |  |  |  |
| $T_5$         | -            | -                     | $T_5$         | 2             | L          | H  | X   | A+2 | J+3      | -    | -    | -    | -    | A+2 | JSR B      | I(A+1)  |  |  |  |
| $T_6$         | -            | -                     | $T_6$         | 0             | H          | X  | X   | A+3 | -        | -    | -    | -    | -    | B   | RTS        | I(A+1)  |  |  |  |
| $T_7$         | -            | -                     | $T_7$         | 0             | H          | X  | X   | B+1 | J+3      | J+3  | -    | -    | -    | A+3 | I(A+3)     | JSR B   |  |  |  |
| $T_8$         | -            | -                     | $T_8$         | 0             | H          | X  | X   | A+4 | J+3      | J+3  | -    | -    | -    | A+4 | RTS        | RTS   |  |  |  |
| $T_9$         | -            | -                     | $T_9$         | 2             | L          | H  | X   | A+5 | J+3      | J+3  | -    | -    | -    | J+3 | I(J+3)     | RTS   |  |  |  |
| $T_3$         | A            | I(A)                  |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
| $T_4$         | A+1          | -                     |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
| $T_5$         | A+2          | JSR B                 |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
| $T_6$         | A+3          | -                     |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
| $T_7$         | A+4          | RTS                   |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
| $T_8$         | -            | -                     |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
| $T_9$         | -            | -                     |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
| $T_6$         | B            | RTS                   |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
|               | -            | -                     |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
|               | -            | -                     |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
|               | -            | -                     |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |
|               | -            | -                     |               |               |            |    |     |     |          |      |      |      |      |     |            |   |  |  |  |

Figure 4. Two Nested Subroutines. Routine B is Only One Instruction.

$C_n = \text{HIGH}$



Note:  
 $R_1$  and  $D_1$  connected together and  $OR_1$  Inputs removed on CY7C911  
**Figure 5. Microprogram Sequencer Block Diagram**

## Functional Description (Continued)

### Architecture

The CY7C909 and CY7C911 are CMOS microprogram sequencers for use in high speed processor applications. They are cascadable in 4-bit increments. Two devices can address 256 words of microprogram, three can address up to 4K words, and so on. The architecture of the CY7C909/911 is illustrated in the logic diagram in *Figure 5*. The various blocks are described below.

### Multiplexer

The Multiplexer is controlled by the  $S_0$  and  $S_1$  inputs to select the address source. It selects either the Direct Inputs ( $D_i$ ), the Address Register (AR), the Microprogram Counter ( $\mu$ PC), or the stack (SP) as the source of the next microinstruction address.

### Direct Inputs

The Direct Inputs ( $D_i$ ) allow addresses from an external source to be output on the Y outputs. On the CY7C911, the direct inputs are also the inputs to the Address Register.

### Address Register

The Address Register (AR) consists of four D-type, edge-triggered flip-flops which are controlled by the Register Enable (RE) input. When Register Enable is LOW, new data is entered into the register on the LOW to HIGH clock transition.

### Microprogram Counter

The Microprogram Counter ( $\mu$ PC) is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has a Carry-in ( $C_N$ ) input and a Carry-out ( $C_N + 4$ ) output to facilitate cascading. The Carry-in input controls the microprogram counter. When Carry-in is HIGH the incrementer counts sequentially. The counter register is loaded with the current Y output plus one ( $Y + 1 \rightarrow \mu$ PC) on the next clock cycle. When Carry-in is LOW the incrementer does not count. The microprogram counter register is

loaded with the same Y output ( $Y \rightarrow \mu$ PC) on the next clock cycle.

### Stack

The Stack consists of a 4 x 4 memory array and a built-in Stack Pointer (SP) which always points to the last word written. The Stack is used to store return addresses when executing microsubroutines.

The Stack Pointer is an up/down counter controlled by File Enable (FE) and Push/Pop (PUP) inputs. The File Enable input allows stack operations only when it is LOW. The Push/Pop input controls the stack pointer position.

The PUSH operation is initiated at the beginning of a microsubroutine. Push/Pop is set HIGH while File Enable is kept LOW. The stack pointer is incremented and the memory array is written with the microinstruction address following the subroutine jump that initiated the push.

The POP operation is initiated at the end of a microsubroutine to obtain the return address. Both Push/Pop and File Enable are set LOW. The return address is already available to the multiplexer. The stack pointer is decremented on the next LOW to HIGH clock transition, effectively removing old information from the top of the stack. The stack is configured so that data will roll-over if more than four POPs are performed, thus preventing data from being lost.

The contents of the memory position pointed to by the Stack Pointer is always available to the multiplexer. Stack reference operations can thus be performed without a push or a pop. Since the stack is four words deep, up to four microsubroutines can be nested.

The ZERO input resets the four Y outputs to a binary zero state. The OR inputs (7C909 only) are connected to the Y outputs such that any output can be set to a logical one.

The Output Enable (OE) input controls the Y outputs. A HIGH on Output Enable sets the outputs into a high impedance state.

## Definition of Terms

| Name            | Description   |
|-----------------|---|
| <b>INPUTS</b>   |   |
| $S_1, S_0$      | Multiplexer Control Lines, for Access Source Selection  |
| FE              | File Enable, Enables Stack Operation, Active LOW        |
| PUP             | Push/Pop, Selects Stack Operation                       |
| RE              | Register Enable, Enables Address Register Active LOW    |
| ZERO            | Forces Output to Logical Zero                           |
| OE              | Output Enable, Controls Three-State Outputs Active LOW  |
| OR <sub>i</sub> | Logic OR Input to each Address Output Line (7C909 only) |
| $C_n$           | Carry-In, Controls Microprogram Counter                 |
| $R_i$           | Inputs to the Internal Address Register                 |
| $D_i$           | Direct Inputs to the Multiplexer                        |
| CP              | Clock Input   |

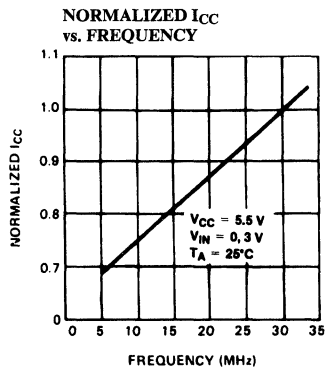
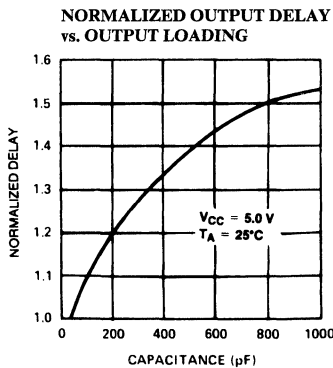
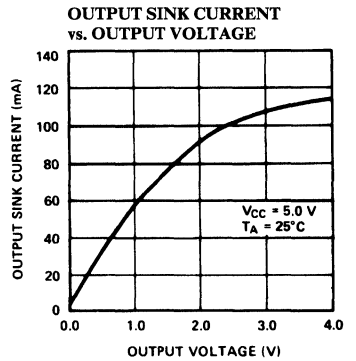
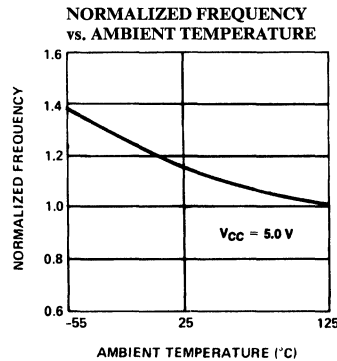
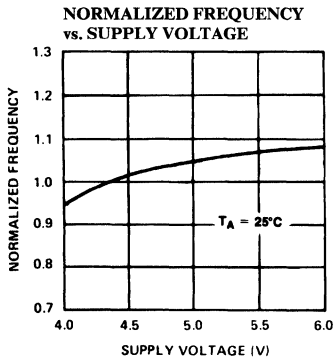
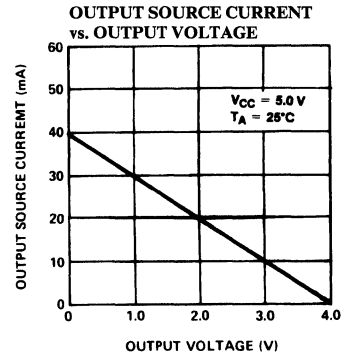
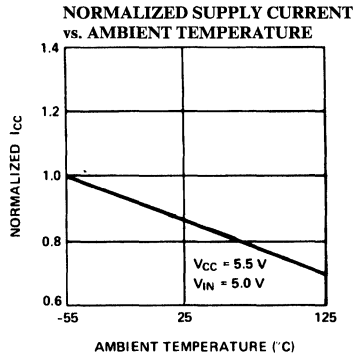
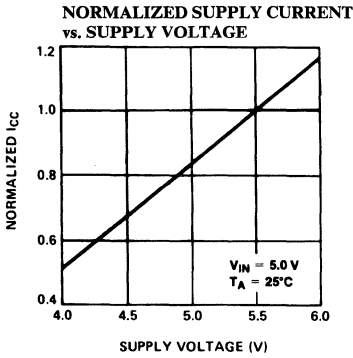


**Definition of Terms (Continued)**

| Name                    | Description  |
|-------------------------|--|
| <b>OUTPUTS</b>          |  |
| $Y_i$                   | Address Outputs  |
| $C_{N+4}$               | Carry-Out from Incrementer   |
| <b>INTERNAL SIGNALS</b> |  |
| $\mu PC$                | Contents of the Microprogram Counter                                   |
| AR                      | Contents of the Address Register                                       |
| STK0-<br>STK3           | Contents of the Push/Pop Stack   |
| SP                      | Contents of the Stack Pointer  |
| <b>EXTERNAL SIGNALS</b> |  |
| A                       | Address to the Counter Memory  |
| I(A)                    | Instruction in Control Memory at Address A                             |
| $\mu WR$                | Contents of the Microword Register at the Output of the Control Memory |
| $T_N$                   | Time Period (Cycle) n  |

Typical DC and AC Characteristics

5



**Ordering Information**

| Clock Cycle (ns) | Ordering Code | Package Type | Operating Range |
|------------------|---------------|--------------|-----------------|
| 30               | CY7C909-30PC  | P15          | Commercial      |
| 40               | CY7C909-40PC  | P15          | Commercial      |
| 30               | CY7C909-30JC  | J64          | Commercial      |
| 40               | CY7C909-40JC  | J64          | Commercial      |
| 30               | CY7C909-30DC  | D16          | Commercial      |
| 40               | CY7C909-40DC  | D16          | Commercial      |
| 40               | CY7C909-40LC  | L64          | Commercial      |
| 30               | CY7C909-30DMB | D16          | Military        |
| 40               | CY7C909-40DMB | D16          | Military        |
| 40               | CY7C909-40LMB | L64          | Military        |

| Clock Cycle (ns) | Ordering Code | Package Type | Operating Range |
|------------------|---------------|--------------|-----------------|
| 30               | CY7C911-30PC  | P5           | Commercial      |
| 40               | CY7C911-40PC  | P5           | Commercial      |
| 30               | CY7C911-30JC  | J61          | Commercial      |
| 40               | CY7C911-40JC  | J61          | Commercial      |
| 30               | CY7C911-30DC  | D6           | Commercial      |
| 40               | CY7C911-40DC  | D6           | Commercial      |
| 40               | CY7C911-40LC  | L61          | Commercial      |
| 30               | CY7C911-30DMB | D6           | Military        |
| 40               | CY7C911-40DMB | D6           | Military        |
| 40               | CY7C911-40LMB | L61          | Military        |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>OS</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>CC1</sub>     | 1,2,3     |

**5**

#### Switching Characteristics

| Parameters   | Subgroups   |
|--|-------------|
| Minimum Clock Low Time   | 7,8,9,10,11 |
| Minimum Clock High Time  | 7,8,9,10,11 |
| <b>MAXIMUM COMBINATIONAL PROPAGATION DELAYS</b>                      |             |
| D <sub>i</sub> to Y  | 7,8,9,10,11 |
| D <sub>i</sub> to C <sub>N+4</sub>                                   | 7,8,9,10,11 |
| S <sub>0</sub> , S <sub>1</sub> to Y                                 | 7,8,9,10,11 |
| S <sub>0</sub> , S <sub>1</sub> to C <sub>N+4</sub>                  | 7,8,9,10,11 |
| OR <sub>i</sub> (7C909) to Y   | 7,8,9,10,11 |
| OR <sub>i</sub> (7C909) to C <sub>N+4</sub>                          | 7,8,9,10,11 |
| C <sub>N</sub> to C <sub>N+4</sub>                                   | 7,8,9,10,11 |
| ZER <sub>0</sub> to C <sub>N+4</sub>                                 | 7,8,9,10,11 |
| Clock High, S <sub>0</sub> , S <sub>1</sub> = LH to Y                | 7,8,9,10,11 |
| Clock High, S <sub>0</sub> , S <sub>1</sub> = LH to C <sub>N+4</sub> | 7,8,9,10,11 |
| Clock High, S <sub>0</sub> , S <sub>1</sub> = LL to Y                | 7,8,9,10,11 |
| Clock High, S <sub>0</sub> , S <sub>1</sub> = LL to C <sub>N+4</sub> | 7,8,9,10,11 |
| Clock High, S <sub>0</sub> , S <sub>1</sub> = HL to Y                | 7,8,9,10,11 |
| Clock High, S <sub>0</sub> , S <sub>1</sub> = HL to C <sub>N+4</sub> | 7,8,9,10,11 |

| Parameters                                  | Subgroups   |
|---|-------------|
| <b>MINIMUM SET-UP AND HOLD TIMES</b>        |             |
| RE Set-up Time                              | 7,8,9,10,11 |
| RE Hold Time                                | 7,8,9,10,11 |
| Push/Pop Set-up Time                        | 7,8,9,10,11 |
| Push/Pop Hold Time                          | 7,8,9,10,11 |
| FE Set-up Time                              | 7,8,9,10,11 |
| FE Hold Time                                | 7,8,9,10,11 |
| C <sub>N</sub> Set-up Time                  | 7,8,9,10,11 |
| C <sub>N</sub> Hold Time                    | 7,8,9,10,11 |
| D <sub>i</sub> Set-up Time                  | 7,8,9,10,11 |
| D <sub>i</sub> Hold Time                    | 7,8,9,10,11 |
| OR <sub>i</sub> (7C909) Set-up Time         | 7,8,9,10,11 |
| OR <sub>i</sub> (7C909) Hold Time           | 7,8,9,10,11 |
| S <sub>0</sub> , S <sub>1</sub> Set-up Time | 7,8,9,10,11 |
| S <sub>0</sub> , S <sub>1</sub> Hold Time   | 7,8,9,10,11 |
| ZER <sub>0</sub> Set-up Time                | 7,8,9,10,11 |
| ZER <sub>0</sub> Hold Time                  | 7,8,9,10,11 |

Document #: 38-00015-B



**Features**

- **Fast**
  - CY7C910-40 has a 40 ns (min.) clock cycle; commercial
  - CY7C910-46 has a 46 ns (min.) clock cycle; military
- **Low power**
  - ICC (max.) = 70 mA
- **VCC margin 5V ± 10% commercial and military**
- **Sixteen powerful microinstructions**
- **Three output enable controls for three-way branch**
- **Twelve-bit address word**
- **Four sources for addresses: microprogram counter (MPC), stack, branch address bus, internal holding register**
- **12-bit internal loop counter**
- **Internal 17-word by 12-bit stack**  
The internal stack can be used

for subroutine return address or data storage

- **ESD protection**  
Capable of withstanding over 2000V static discharge voltage
- **Pin compatible and functional equivalent to AM2910A**

**Functional Description**

The CY7C910 is a stand-alone microprogram controller that selects, stores, retrieves, manipulates and tests addresses that control the sequence of execution of instructions stored in an external memory. All addresses are 12-bit binary values that designate an absolute memory location.

The CY7C910, as illustrated in the block diagram, consists of a 17-word by 12-bit LIFO (Last-In-First-Out) stack and SP (Stack Pointer), a 12-bit RC (Register/Counter), a 12-bit MPC (Microprogram Counter) and incrementer, a 12-bit wide by 4-input multi-

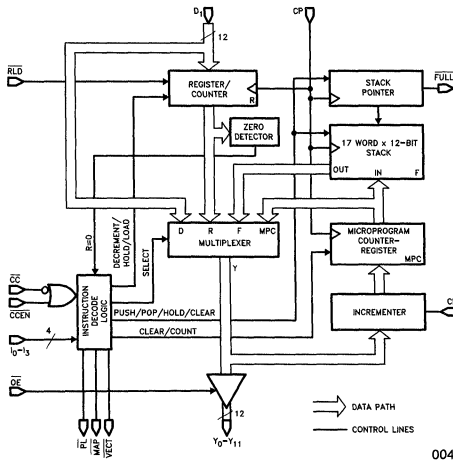
plexer and the required data manipulation and control logic.

The operation performed is determined by four input instruction lines (I0–I3) that in turn select the (internal) source of the next micro-instruction to be fetched. This address is output on the Y0–Y11 pins. Two additional inputs (CC and CCEN) are provided that are examined during certain instructions and enable the user to make the execution of the instruction either unconditional or dependent upon an external test.

The CY7C910 is a pin compatible, functional equivalent, improved performance replacement for the AM2910A.

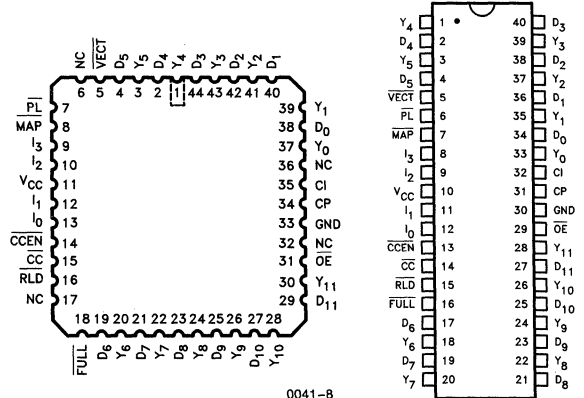
The CY7C910 is fabricated using an advanced 1.2 micron CMOS process that eliminates latchup, results in ESD protection of over 2000 volts and achieves superior performance and low power dissipation.

**Logic Block Diagram**



0041-1

**Pin Configurations**



0041-8

Top View

0041-2

**Selection Guide**

| Clock Cycle (Min.) in ns | Stack Depth | Operating Range | Part Number |
|--------------------------|-------------|-----------------|-------------|
| 40                       | 17 words    | Commercial      | CY7C910-40  |
| 46                       | 17 words    | Military        | CY7C910-46  |
| 50                       | 17 words    | Commercial      | CY7C910-50  |
| 51                       | 17 words    | Military        | CY7C910-51  |
| 93                       | 17 words    | Commercial      | CY7C910-93  |
| 99                       | 17 words    | Military        | CY7C910-99  |

**Pin Definitions**

| Signal Name     | I/O | Description   |
|-----------------|-----|---|
| D0-D11          | I   | Direct inputs to the RC (Register/Counter) and multiplexer. D0 is LSB and D11 is MSB.   |
| RLD             | I   | Register load. Control input to RC that, when LOW, loads data on the D0-D11 pins into RC on the LOW to HIGH clock (CP) transition.              |
| I0-I3           | I   | Instruction inputs that select one of sixteen instructions to be performed by the CY7C910.  |
| $\overline{CC}$ | I   | Control input that, when LOW, signifies that a test has passed.   |
| CCEN            | I   | Enable for $\overline{CC}$ input. When HIGH $\overline{CC}$ is ignored and a pass is forced. When LOW the state of $\overline{CC}$ is examined. |
| CP              | I   | Clock input. All internal states are changed on the LOW to HIGH clock transitions.  |

| Signal Name       | I/O | Description   |
|-------------------|-----|---|
| CI                | I   | Carry input to the LSB of the incrementer for the MPC.                      |
| $\overline{OE}$   | I   | Control for Y0-Y11 outputs. LOW to enable; High to disable.                 |
| Y0-Y11            | O   | Address output to microprogram memory. Y0 is LSB and Y11 is MSB.            |
| $\overline{FULL}$ | O   | When LOW indicates the stack is full.                                       |
| $\overline{PL}$   | O   | When LOW selects the pipeline register as the direct input (D0-D11) source. |
| $\overline{MAP}$  | O   | When LOW selects the Mapping PROM (or PLA) as the direct input source.      |
| $\overline{VECT}$ | O   | When LOW selects the Interrupt Vector as the direct input source.           |

## Architecture of the CY7C910

### Introduction

The CY7C910 is a high performance CMOS microprogram controller that produces a sequence of 12-bit addresses that control the execution of a microprogram. The addresses are selected from one of four sources, depending upon the (internal) instruction being executed (I0–I3), and other external inputs. The sources are (1) the (external) D0–D11 inputs, (2) the RC, (3) the stack and (4) the MPC. Twelve bit lines from each of these four sources are the inputs to a multiplexer, as shown in *Figure 1*, whose outputs are applied to the inputs of the Y0–Y11 three-state output drivers.

### External Inputs: D0–D11

The external inputs are used as the source for destination addresses for the jump or branch type of instructions. These are shown as Ds in the two columns in the Table of Instructions. A second use of these inputs is to load the RC.

### Register Counter: RC

The RC is implemented as 12 D-type, edge-triggered flip-flops that are synchronously clocked on the LOW to HIGH transition of the clock, CP. The data on the D inputs is synchronously loaded into the RC when the load control input, RLD, is LOW. The output of the RC is available to the multiplexer as its R input and is output on the Y outputs during certain instructions, as shown by R in the Table of Instructions.

The RC is operated as a 12-bit down counter and its contents decremented and tested if zero during instructions 8, 9 and 15. This enables micro-instructions to be repeated up to 4096 times. The RC is arranged such that if it is loaded with a number, N, the sequence will be executed exactly  $N + 1$  times.

### The Stack and Stack Pointer: SP

The 17-word by 12-bit stack is used to provide return addresses from micro-subroutines or from loops. Intergal to it is a SP, which points to (addresses) the last word written.

This permits reference to the data on the top of the stack without having to perform a POP operation.

The SP operates as an up/down counter that is incremented when a PUSH operation (instructions 1, 4 or 5) is performed or decremented when a POP operation (instructions 8, 10, 11, 13 or 15) is performed. The PUSH operation writes the return address on the stack and the POP operation effectively removes it. The actual operation occurs on the LOW to HIGH clock transition following the instruction.

The stack is initialized by executing instruction zero (JUMP TO LOCATION 0 or RESET). Every time a “jump to subroutine” instruction (1, 5) or a loop instruction (4) is executed, the return address is PUSHed onto the stack; and every time a “return from subroutine (or loop)” instruction is executed, the return address is POPed off the stack.

When one subroutine calls another or a loop occurs within a loop (or a combination), which is called nesting, the Logical depth of the stack increases. The physical stack depth is 17 words. When this depth occurs, the FULL signal goes LOW on the next LOW to HIGH clock transition. Any further PUSH operations on a full stack will cause the data at that location to be over-written, but will not increment the SP. Similarly, performing a POP operation on an empty stack will not decrement the SP and may result in non-meaningful data being available at the Y outputs.

### The Microprocessor Counter: MPC

The MPC consists of a 12-bit incremter followed by a 12-bit register. The register usually holds the address of the instruction being fetched. When sequential instructions are fetched, the carry input (CI) to the incremter is HIGH and one is added to the Y outputs of the multiplexer, which is loaded into the MPC on the next LOW to HIGH clock transition. When the CI input is LOW, the Y outputs of the multiplexer are loaded directly into the MPC, so that the same instruction is fetched and executed.

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied ..... -55°C to +125°C  
 Supply Voltage to Ground Potential  
 (Pin 10 to Pin 30) ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs  
 in High Z State ..... -0.5V to +7.0V  
 DC Input Voltage ..... -3.0V to +7.0V  
 Output Current into Outputs (Low) ..... 30 mA

Static Discharge Voltage ..... > 2001V  
 (Per MIL-STD-883 Method 3015)

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[3]</sup> | -55°C to +125°C     | 5V ± 10%        |

### Electrical Characteristics Over Commercial and Military Operating Range, V<sub>CC</sub> Min. = 4.5V, V<sub>CC</sub> Max. = 5.5V<sup>[4]</sup>

| Parameter        | Description                  | Test Condition  | Min.  | Max.            | Units    |
|------------------|------------------------------|---|---|-----------------|----------|
| V <sub>OH</sub>  | Output HIGH Voltage          | V <sub>CC</sub> = Min.<br>I <sub>OH</sub> = -1.6 mA                           | 2.4   |                 | V        |
| V <sub>OL</sub>  | Output LOW Voltage           | V <sub>CC</sub> = Min.<br>I <sub>OL</sub> = 12 mA                             |   | 0.4             | V        |
| V <sub>IH</sub>  | Input HIGH Voltage           |   | 2.0   | V <sub>CC</sub> | V        |
| V <sub>IL</sub>  | Input LOW Voltage            |   | -3.0  | 0.8             | V        |
| I <sub>IH</sub>  | Input HIGH Current           | V <sub>CC</sub> = Max.<br>V <sub>IN</sub> = V <sub>CC</sub>                   |   | 10              | μA       |
| I <sub>IL</sub>  | Input LOW Current            | V <sub>CC</sub> = Max.<br>V <sub>IN</sub> = V <sub>SS</sub>                   |   | -10             | μA       |
| I <sub>OH</sub>  | Output HIGH Current          | V <sub>CC</sub> = Min.<br>V <sub>IH</sub> = 2.4V                              | -1.6  |                 | mA       |
| I <sub>OL</sub>  | Output LOW Current           | V <sub>CC</sub> = Min.<br>V <sub>OL</sub> = 0.4V                              | 12  |                 | mA       |
| I <sub>OZ</sub>  | Output Leakage Current       | V <sub>CC</sub> = Max.<br>V <sub>OUT</sub> = V <sub>SS</sub> /V <sub>CC</sub> | -40   | +40             | μA<br>μA |
| I <sub>SC</sub>  | Output Short Circuit Current | V <sub>CC</sub> = Max.<br>V <sub>OUT</sub> = 0V                               |   | -85             | mA       |
| I <sub>CC</sub>  | Supply Current               | Commercial  | V <sub>CC</sub> = Max.                          | 70              | mA       |
|                  |                              | Military  |   | 90              |          |
| I <sub>CC1</sub> | Supply Current               | Commercial  | V <sub>IH</sub> ≥ 3.85V, V <sub>IL</sub> ≤ 0.4V | 35              | mA       |
|                  |                              | Military  |   | 50              |          |

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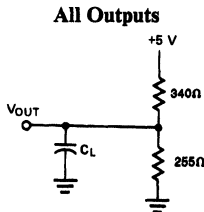
### Capacitance<sup>[2]</sup>

| Parameters       | Description        | Test Conditions  | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz<br>V <sub>CC</sub> = 5.0V | 8    | pF    |
| C <sub>OUT</sub> | Output Capacitance |  | 10   | pF    |

Notes:

- Not more than one output should be tested at a time. Duration of the short circuit should not exceed one second.
- Tested initially and after any design or process changes that may affect these parameters.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

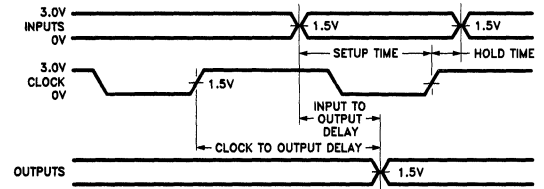
### Output Load used for AC Performance Characteristics



Notes:

- C<sub>L</sub> = 50 pF includes scope probe, writing and stray capacitance.
- C<sub>L</sub> = 5 pF for output disable tests.

### Switching Waveforms





## Guaranteed AC Performance Characteristics

The tables below specify the guaranteed AC performance of the CY7C910 over the commercial (0°C to +70°C) and the military (-55°C to +125°C) temperature ranges with V<sub>CC</sub> varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels.

The inputs switch between 0V and 3V with signal transition rates of 1 Volt per nanosecond. All outputs have maximum DC current loads.

### Clock Requirements<sup>[1, 3]</sup>

|                                   | Commercial |    |     | Military |    |     |
|-----------------------------------|------------|----|-----|----------|----|-----|
| CY7C910-                          | 40         | 50 | 93  | 46       | 51 | 99  |
| Minimum Clock LOW                 | 20         | 20 | 50  | 23       | 25 | 58  |
| Minimum Clock HIGH                | 20         | 20 | 35  | 23       | 25 | 42  |
| Minimum Clock Period I = 14       | 40         | 50 | 93  | 46       | 51 | 100 |
| Minimum Clock Period I = 8, 9, 15 | 40         | 50 | 113 | 46       | 51 | 114 |

### Combinatorial Propagation Delays. C<sub>L</sub> = 50 pF<sup>[3]</sup>

| From Input                     | Commercial |    |    |               |    |    |      |    |    | Military |    |    |               |    |    |      |    |    |
|--------------------------------|------------|----|----|---------------|----|----|------|----|----|----------|----|----|---------------|----|----|------|----|----|
|                                | Y          |    |    | PL, VECT, MAP |    |    | FULL |    |    | Y        |    |    | PL, VECT, MAP |    |    | FULL |    |    |
| CY7C910-                       | 40         | 50 | 93 | 40            | 50 | 93 | 40   | 50 | 93 | 46       | 51 | 99 | 46            | 51 | 99 | 46   | 51 | 99 |
| D0-D11                         | 17         | 20 | 20 | —             | —  | —  | —    | —  | —  | 21       | 25 | 25 | —             | —  | —  | —    | —  | —  |
| I0-I3                          | 25         | 35 | 50 | 20            | 30 | 51 | —    | —  | —  | 30       | 40 | 54 | 25            | 35 | 58 | —    | —  | —  |
| CC                             | 22         | 30 | 30 | —             | —  | —  | —    | —  | —  | 27       | 36 | 35 | —             | —  | —  | —    | —  | —  |
| CCEN                           | 22         | 30 | 30 | —             | —  | —  | —    | —  | —  | 27       | 36 | 37 | —             | —  | —  | —    | —  | —  |
| CP<br>I = 8, 9, 15<br>(Note 2) | 30         | 40 | 75 | —             | —  | —  | 25   | 31 | 60 | 35       | 46 | 77 | —             | —  | —  | 30   | 35 | 67 |
| CP<br>All Other I              | 30         | 40 | 55 | —             | —  | —  | 25   | 31 | 60 | 35       | 46 | 61 | —             | —  | —  | 30   | 35 | 67 |
| OE<br>(Note 2)                 | 21         | 25 | 35 | —             | —  | —  | —    | —  | —  | 22       | 25 | 40 | —             | —  | —  | —    | —  | —  |
|                                | 21         | 27 | 30 | —             | —  | —  | —    | —  | —  | 22       | 30 | 30 | —             | —  | —  | —    | —  | —  |

### Minimum Set-Up and Hold Times Relative to clock LOW to HIGH Transition. C<sub>L</sub> = 50 pF<sup>[3]</sup>

| Input    | Commercial |    |    |      |    |    | Military |    |    |      |    |    |
|----------|------------|----|----|------|----|----|----------|----|----|------|----|----|
|          | Set-Up     |    |    | Hold |    |    | Set-Up   |    |    | Hold |    |    |
| CY7C910- | 40         | 50 | 93 | 40   | 50 | 93 | 46       | 51 | 99 | 46   | 51 | 99 |
| DI → RC  | 13         | 16 | 24 | 0    | 0  | 0  | 13       | 16 | 28 | 0    | 0  | 0  |
| DI → MPC | 20         | 30 | 58 | 0    | 0  | 0  | 20       | 30 | 62 | 0    | 0  | 0  |
| I0-I3    | 25         | 35 | 75 | 0    | 0  | 0  | 27       | 38 | 81 | 0    | 0  | 0  |
| CC       | 20         | 24 | 63 | 0    | 0  | 0  | 25       | 35 | 65 | 0    | 0  | 0  |
| CCEN     | 20         | 24 | 63 | 0    | 0  | 0  | 25       | 35 | 63 | 0    | 0  | 0  |
| CI       | 15         | 18 | 46 | 0    | 0  | 0  | 15       | 18 | 58 | 0    | 0  | 0  |
| RLD      | 15         | 19 | 36 | 0    | 0  | 0  | 15       | 20 | 42 | 0    | 0  | 0  |

#### Notes:

1. A dash indicates that a propagation delay path or set-up time does not exist.

2. The enable/disable times are measured to a 0.5 Volt change on the output voltage level with C<sub>L</sub> = 5 pF.

3. See the last page of this specification for Group A subgroup testing information.

**Table of Instructions**

| I <sub>3</sub> -I <sub>0</sub> | Mnemonic | Name                     | Reg/<br>Cntr<br>Con-<br>tents | Result                      |       |                            |       |              |        |
|--------------------------------|----------|--------------------------|-------------------------------|-----------------------------|-------|----------------------------|-------|--------------|--------|
|                                |          |                          |                               | Fail<br>CCEN = L and CC = H |       | Pass<br>CCEN = H or CC = L |       | Reg/<br>Cntr | Enable |
|                                |          |                          |                               | Y                           | Stack | Y                          | Stack |              |        |
| 0                              | JZ       | Jump Zero                | X                             | 0                           | Clear | 0                          | Clear | Hold         | PL     |
| 1                              | CJS      | Cond JSB PL              | X                             | PC                          | Hold  | D                          | Push  | Hold         | PL     |
| 2                              | JMAP     | Jump Map                 | X                             | D                           | Hold  | D                          | Hold  | Hold         | Map    |
| 3                              | CJP      | Cond Jump PL             | X                             | PC                          | Hold  | D                          | Hold  | Hold         | PL     |
| 4                              | PUSH     | Push/Cond LD CNTR        | X                             | PC                          | Push  | PC                         | Push  | (Note 1)     | PL     |
| 5                              | JSRP     | Cond JSB R/PL            | X                             | R                           | Push  | D                          | Push  | Hold         | PL     |
| 6                              | CJV      | Cond Jump Vector         | X                             | PC                          | Hold  | D                          | Hold  | Hold         | Vect   |
| 7                              | JRP      | Cond Jump R/PL           | X                             | R                           | Hold  | D                          | Hold  | Hold         | PL     |
| 8                              | RFCT     | Repeat Loop,<br>CNTR ≠ 0 | ≠0                            | F                           | Hold  | F                          | Hold  | Dec          | PL     |
|                                |          |                          | =0                            | PC                          | POP   | PC                         | Pop   | Hold         | PL     |
| 9                              | RPCT     | Repeat PL,<br>CNTR ≠ 0   | ≠0                            | D                           | Hold  | D                          | Hold  | Dec          | PL     |
|                                |          |                          | =0                            | PC                          | Hold  | PC                         | Hold  | Hold         | PL     |
| 10                             | CRTN     | Cond RTN                 | X                             | PC                          | Hold  | F                          | Pop   | Hold         | PL     |
| 11                             | CJPP     | Cond Jump PL & Pop       | X                             | PC                          | Hold  | D                          | Pop   | Hold         | PL     |
| 12                             | LDCT     | LD Cntr & Continue       | X                             | PC                          | Hold  | PC                         | Hold  | Load         | PL     |
| 13                             | LOOP     | Test End Loop            | X                             | F                           | Hold  | PC                         | Pop   | Hold         | PL     |
| 14                             | CONT     | Continue                 | X                             | PC                          | Hold  | PC                         | Hold  | Hold         | PL     |
| 15                             | TWB      | Three-Way Branch         | ≠0                            | F                           | Hold  | PC                         | Pop   | Dec          | PL     |
|                                |          |                          | =0                            | D                           | Pop   | PC                         | Pop   | Hold         | PL     |

**Notes:**

 1. If  $\overline{CCEN} = L$  and  $\overline{CC} = H$ , hold; else load.

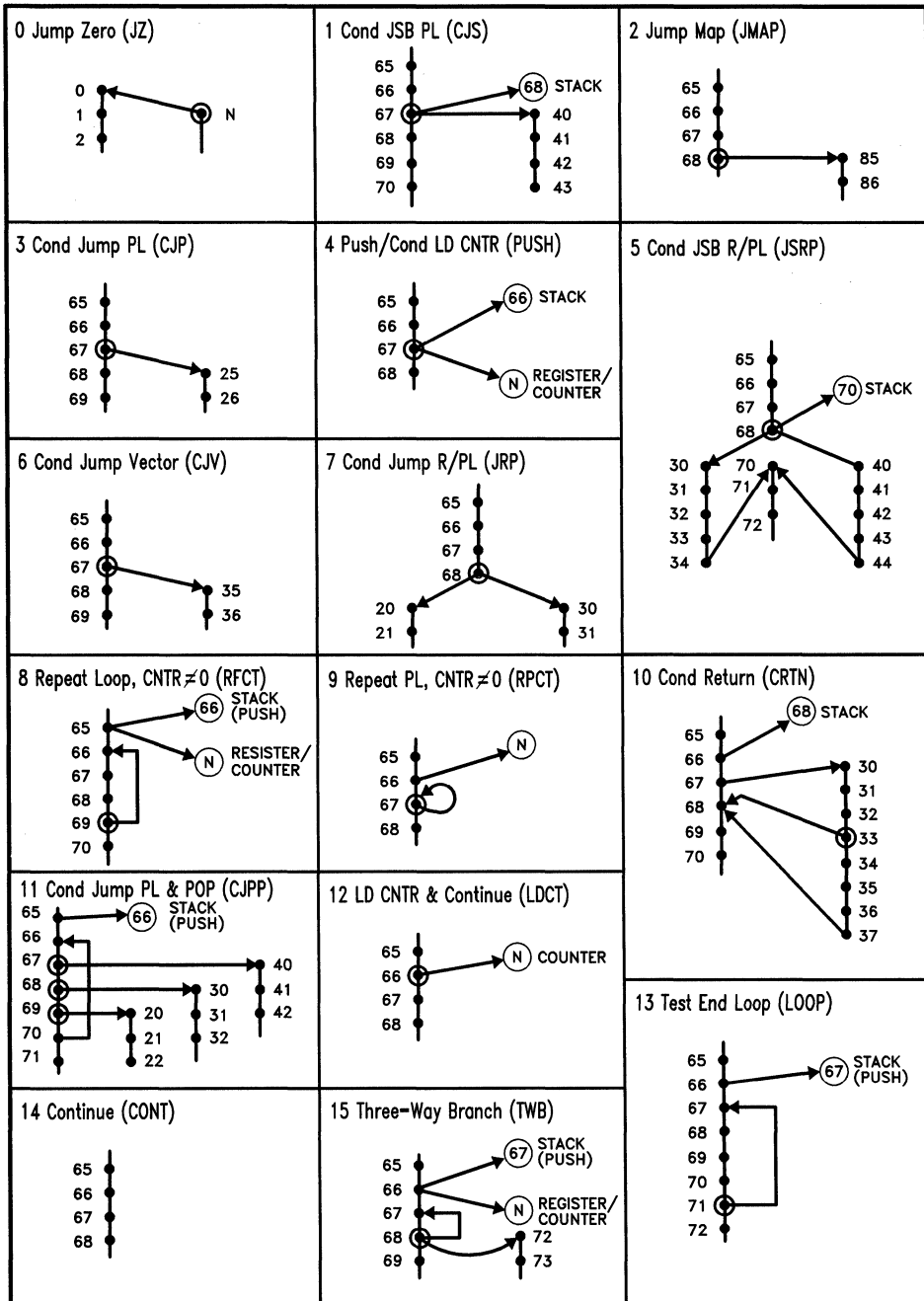
H = HIGH

L = LOW

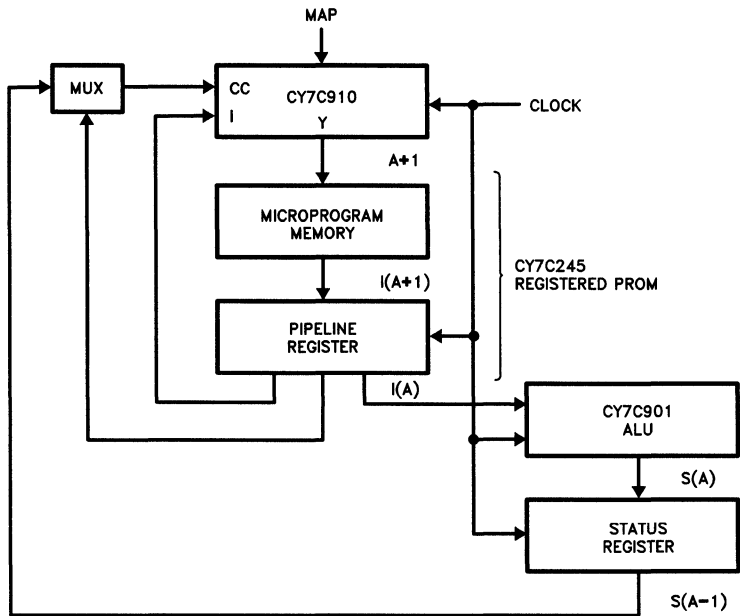
X = Don't Care

CY7C910 CMOS Microprogram Controller

CY7C910 Flow Diagrams

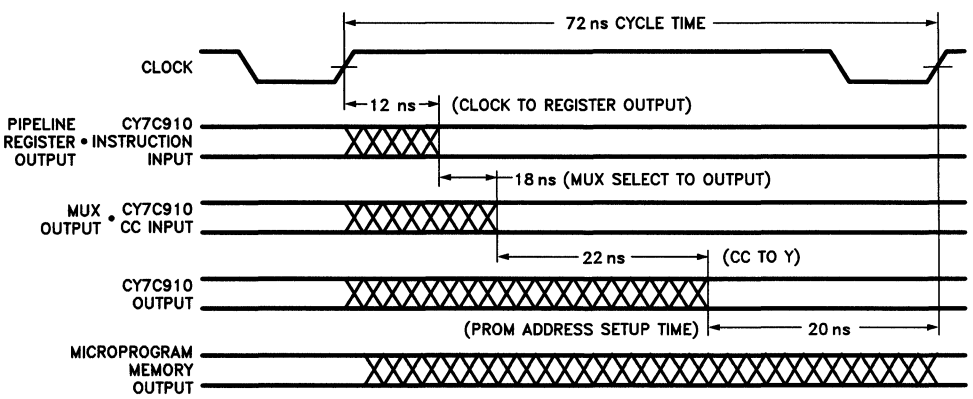


One Level Pipeline Based Architecture (Recommended)



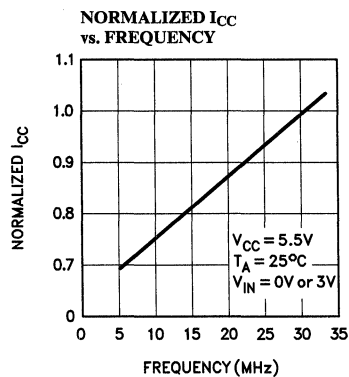
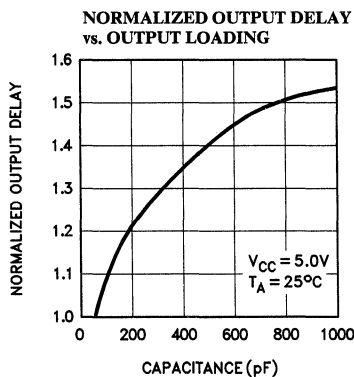
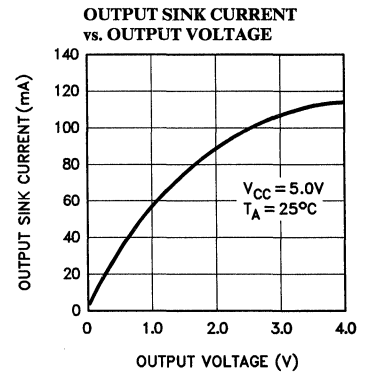
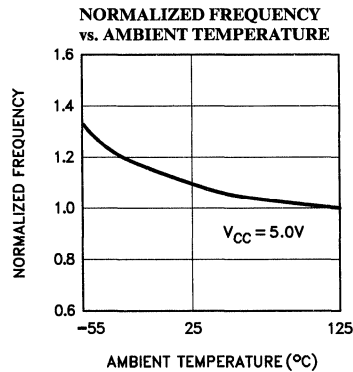
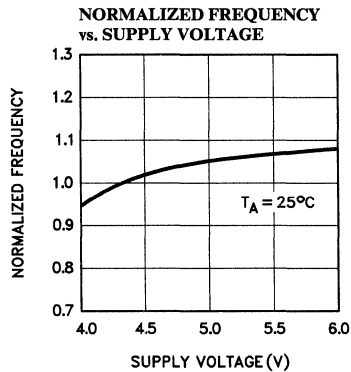
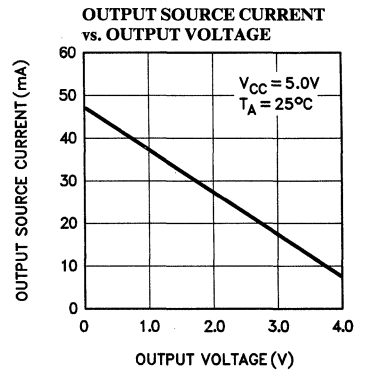
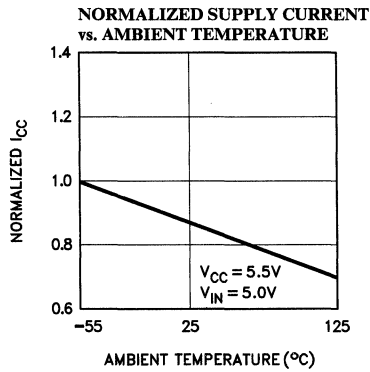
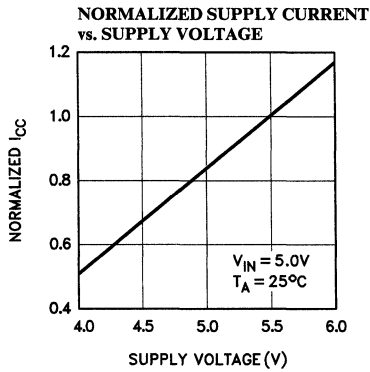
0041-6

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0041-7

Typical DC and AC Characteristics



**Ordering Information**

| <b>Clock Cycle (ns)</b> | <b>Ordering Code</b> | <b>Package Type</b> | <b>Operating Range</b> |
|-------------------------|----------------------|---------------------|------------------------|
| 40                      | CY7C910-40PC         | P17                 | Commercial             |
|                         | CY7C910-40DC         | D18                 |                        |
|                         | CY7C910-40JC         | J67                 |                        |
|                         | CY7C910-40LC         | L67                 |                        |
| 46                      | CY7C910-46DMB        | D18                 | Military               |
|                         | CY7C910-46LMB        | L67                 |                        |
| 50                      | CY7C910-50PC         | P17                 | Commercial             |
|                         | CY7C910-50DC         | D18                 |                        |
|                         | CY7C910-50JC         | J67                 |                        |
|                         | CY7C910-50LC         | L67                 |                        |
| 51                      | CY7C910-51DMB        | D18                 | Military               |
|                         | CY7C910-51LMB        | L67                 |                        |
| 93                      | CY7C910-93PC         | P17                 | Commercial             |
|                         | CY7C910-93DC         | D18                 |                        |
|                         | CY7C910-93JC         | J67                 |                        |
|                         | CY7C910-93LC         | L67                 |                        |
| 99                      | CY7C910-99DMB        | D18                 | Military               |
|                         | CY7C910-99LMB        | L67                 |                        |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL</sub> Max. | 1,2,3     |
| I <sub>IH</sub>      | 1,2,3     |
| I <sub>IL</sub>      | 1,2,3     |
| I <sub>OH</sub>      | 1,2,3     |
| I <sub>OL</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>SC</sub>      | 1,2,3     |
| I <sub>CC</sub>      | 1,2,3     |
| I <sub>CC1</sub>     | 1,2,3     |

**Clock Requirements**

| Parameters        | Subgroups   |
|-------------------|-------------|
| Minimum Clock LOW | 7,8,9,10,11 |

**Combinational Propagation Delays**

| Parameters   | Subgroups   |
|--|-------------|
| From D0–D11 to Y   | 7,8,9,10,11 |
| From I0–I3 to Y  | 7,8,9,10,11 |
| From I0–I3 to $\overline{PL}$ , $\overline{VECT}$ , $\overline{MAP}$ | 7,8,9,10,11 |
| From $\overline{CC}$ to Y  | 7,8,9,10,11 |
| From $\overline{CCEN}$ to Y  | 7,8,9,10,11 |
| From CP (I = 8,9,15) to $\overline{FULL}$                            | 7,8,9,10,11 |
| From CP (All Other I) to Y   | 7,8,9,10,11 |
| From CP (All Other I) to $\overline{FULL}$                           | 7,8,9,10,11 |

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**Minimum Set-up and Hold Times**

| Parameters                    | Subgroups   |
|-------------------------------|-------------|
| DI → RC Set-up Time           | 7,8,9,10,11 |
| DI → RC Hold Time             | 7,8,9,10,11 |
| DI → MPC Set-up Time          | 7,8,9,10,11 |
| DI → MPC Hold Time            | 7,8,9,10,11 |
| I0–I3 Set-up Time             | 7,8,9,10,11 |
| I0–I3 Hold Time               | 7,8,9,10,11 |
| $\overline{CC}$ Set-up Time   | 7,8,9,10,11 |
| $\overline{CC}$ Hold Time     | 7,8,9,10,11 |
| $\overline{CCEN}$ Set-up Time | 7,8,9,10,11 |
| $\overline{CCEN}$ Hold Time   | 7,8,9,10,11 |
| CI Set-up Time                | 7,8,9,10,11 |
| CI Hold Time                  | 7,8,9,10,11 |
| $\overline{RLD}$ Set-up Time  | 7,8,9,10,11 |
| $\overline{RLD}$ Hold Time    | 7,8,9,10,11 |



**Features**

- **Fast**
  - CY7C9101-30 has a 30 ns (max.) clock cycle (commercial)
  - CY7C9101-35 has a 35 ns (max.) clock cycle (military)
- **Low Power**
  - $I_{CC}$  (max. at 10 MHz) = 60 mA (commercial)
  - $I_{CC}$  (max. at 10 MHz) = 85 mA (military)
- **$V_{CC}$  Margin**
  - $5V \pm 10\%$
- **All parameters guaranteed over commercial and military operating temperature range**
- **Replaces four 2901's with carry look-ahead logic**
- **Eight Function ALU**
  - Performs three arithmetic and five logical operations on two 16-bit operands
- **Expandable**
  - Infinitely expandable in 16-bit increments
- **Four Status Flags**
  - Carry, overflow, negative, zero
- **ESD Protection**
  - Capable of withstanding greater than 2000V static discharge voltage
- **Pin compatible and functionally equivalent to AM29C101**

**Functional Description**

The CY7C9101 is a high-speed, expandable, 16-bit wide ALU slice which can be used to implement the arithmetic section of a CPU, peripheral controller, or programmable controller. The instruction set of the CY7C9101 is basic, yet so versatile that it can emulate the ALU of almost any digital computer.

The CY7C9101, as shown in the block diagram, consists of a 16-word by 16-bit dual-port RAM register file, a 16-bit ALU, and the necessary data manipulation and control logic.

The function performed is determined by the nine-bit instruction word ( $I_8$  to  $I_0$ ) which is usually input via a micro-instruction register.

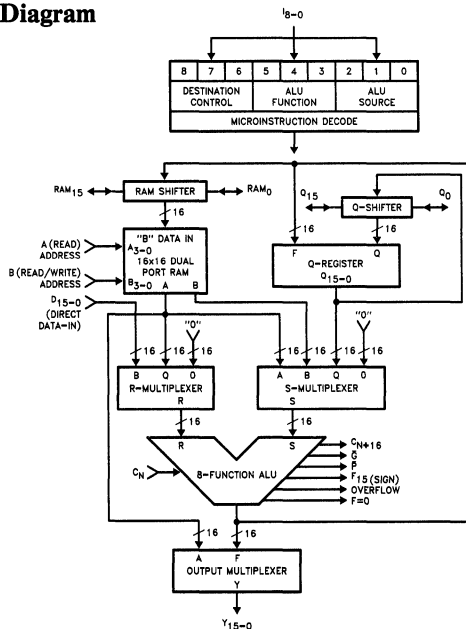
The CY7C9101 is expandable in 16-bit increments, has three-state data outputs as well as flag outputs, and can implement either a full look-ahead carry or a ripple carry.

The CY7C9101 is a pin compatible, functional equivalent of the Am29C101 with improved performance. The 7C9101 replaces four 2901's and includes on-chip carry look-ahead logic.

Fabricated in an advanced 1.2 micron CMOS process, the 7C9101 eliminates latchup, has ESD protection greater than 2000V, and achieves superior performance with low power dissipation.

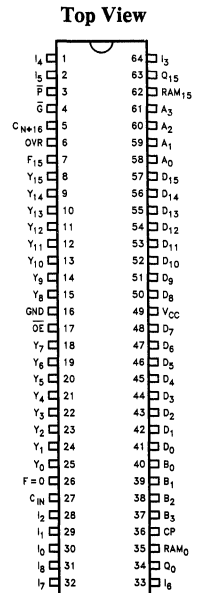
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**Logic Block Diagram**



**Figure 1**

**Pin Configuration**



0079-2

0079-1



## Selection Guide

|  |            | 7C9101-30<br>7C9101-35 | 7C9101-40<br>7C9101-45 |
|--|------------|------------------------|------------------------|
| Minimum Clock Cycle (ns)                 | Commercial | 30                     | 40                     |
|  | Military   | 35                     | 45                     |
| Maximum Operating Current at 10 MHz (mA) | Commercial | 60                     | 60                     |
|  | Military   | 85                     | 85                     |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage to Ground

Potential ..... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Output Current into Outputs (Low) ..... 30 mA

Static Discharge Voltage ..... >2001V  
(Per MIL-STD-883 Method 3015)

Latchup Current (Outputs) ..... >200 mA

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +70°C        | 5V ± 10%        |
| Military <sup>[1]</sup> | -55°C to +125°C     | 5V ± 10%        |

Note:

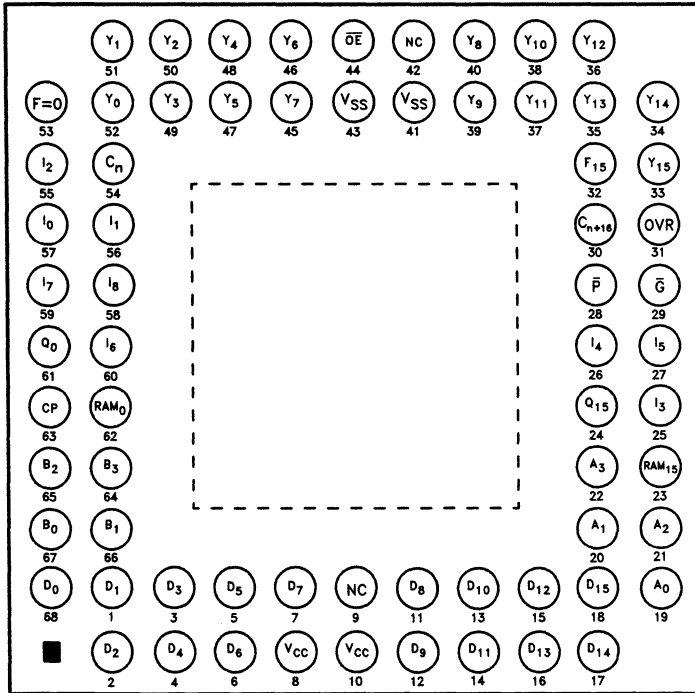
1. T<sub>A</sub> is the "instant on" case temperature.

## Pin Definitions

| Signal Name                            | I/O | Description   |
|--|-----|---|
| A <sub>3-0</sub>                       | I   | <b>RAM Address A.</b> This 4-bit address word selects one of the 16 registers in the register file for output on the (internal) A-port.   |
| B <sub>3-0</sub>                       | I   | <b>RAM Address B.</b> This 4-bit address word selects one of the 16 registers in the register file for output on the (internal) B-port. When data is written back to the register file, this is the destination address.  |
| I <sub>8-0</sub>                       | I   | <b>Instruction Word.</b> This nine-bit word is decoded to determine the ALU data sources (I <sub>0</sub> , 1, 2), the ALU operation (I <sub>3</sub> , 4, 5), and the data to be written to the Q-register or register file (I <sub>6</sub> , 7, 8).   |
| D <sub>15-0</sub>                      | I   | <b>Direct Data Input.</b> This 16-bit data word may be selected by the I <sub>0</sub> , 1, 2 lines as an input to the ALU.  |
| Y <sub>15-0</sub>                      | I   | <b>Data Output.</b> These are three-state data output lines which, when enabled, output either the ALU result or the data in the A latch, as determined by the code on I <sub>6</sub> , 7, 8.   |
| $\overline{OE}$                        | I   | <b>Output Enable.</b> This is an active LOW input which controls the Y <sub>15-0</sub> outputs. A HIGH level on this signal places the output drivers at the high impedance state.  |
| CP                                     | I   | <b>Clock.</b> The LOW level of CP is used to write data to the RAM register file. A HIGH level of CP writes data from the dual port RAM to the A and B latches. The operation of the Q register is similar; data is entered into the master latch on the LOW level of CP and transferred from master to slave during CP = HIGH. |
| Q <sub>15</sub> ,<br>RAM <sub>15</sub> | I/O | These two lines are bidirectional and are controlled by I <sub>6</sub> , 7, 8. They are three-state output drivers connected to the TTL compatible CMOS inputs.   |

| Signal Name                            | I/O | Description   |
|--|-----|---|
| Q <sub>15</sub> ,<br>RAM <sub>15</sub> | I/O | <b>Output Mode:</b> When the destination code on lines I <sub>6</sub> , 7, 8 indicates a left shift (UP) operation, the three-state outputs are enabled and the MSB of the Q register is output on the Q <sub>15</sub> pin and likewise, the MSB of the ALU output (F <sub>15</sub> ) is output on the RAM 15 pin.<br><b>Input Mode:</b> When the destination code indicates a right shift (DOWN), the pins are the data inputs to the MSB of the Q register and the RAM, respectively. |
| Q <sub>0</sub> ,<br>RAM <sub>0</sub>   | I/O | These two lines are bidirectional and function similarly to the Q <sub>15</sub> and RAM <sub>15</sub> lines. The Q <sub>0</sub> and RAM <sub>0</sub> lines are the LSB of the Q register and the RAM.   |
| C <sub>n</sub>                         | I   | <b>Carry In.</b> The carry in to the internal ALU.  |
| C <sub>n</sub> + 16                    | O   | <b>Carry Out.</b> The carry out from the internal ALU.  |
| $\overline{G}$ , $\overline{P}$        | O   | <b>Carry Generate, Carry Propagate.</b> Outputs from the ALU which may be used to perform a carry look-ahead operation over the 16-bits of the ALU.   |
| OVR                                    | O   | <b>Overflow.</b> This signal is the logical exclusive-OR of the carry-in and carry-out of the MSB of the ALU. This indicates when the result of the ALU operation exceeded the capacity of the machine's two's complement number range. It is valid only for the sign bit.  |
| F = 0                                  | O   | <b>Zero Detect.</b> Open drain output which goes HIGH when the data on outputs (F <sub>15-0</sub> ) are all LOW. It indicates that the result of an ALU operation is zero (positive logic assumed).   |
| F <sub>15</sub>                        | O   | <b>Sign.</b> The MSB of the ALU output.   |

Top View



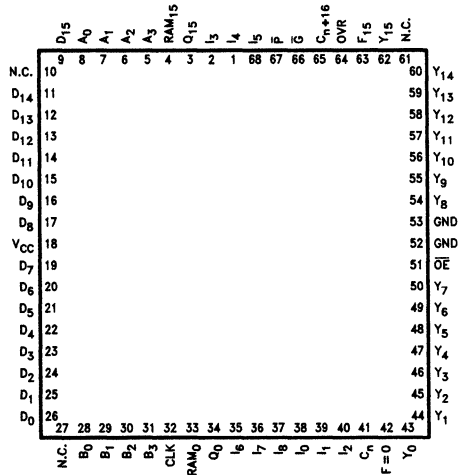
CY7C9101 Pinout for 68PGA

NC = No Connect

0079-11

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Top View



CY7C9101 Pinout for LCC/PLCC

NC = No Connect

0079-3

**Functional Tables**
**Table 1. ALU Source Operand Control**

| Mnemonic | Micro Code     |                |                |            | ALU Source Operands |   |
|----------|----------------|----------------|----------------|------------|---------------------|---|
|          | I <sub>2</sub> | I <sub>1</sub> | I <sub>0</sub> | Octal Code | R                   | S |
| AQ       | L              | L              | L              | 0          | A                   | Q |
| AB       | L              | L              | H              | 1          | A                   | B |
| ZQ       | L              | H              | L              | 2          | O                   | Q |
| ZB       | L              | H              | H              | 3          | O                   | B |
| ZA       | H              | L              | L              | 4          | O                   | A |
| DA       | H              | L              | H              | 5          | D                   | A |
| DQ       | H              | H              | L              | 6          | D                   | Q |
| DZ       | H              | H              | H              | 7          | D                   | O |

**Table 2. ALU Function Control**

| Mnemonic | Micro Code     |                |                |            | ALU Function    | Symbol                  |
|----------|----------------|----------------|----------------|------------|-----------------|-------------------------|
|          | I <sub>5</sub> | I <sub>4</sub> | I <sub>3</sub> | Octal Code |                 |                         |
| ADD      | L              | L              | L              | 0          | R Plus S        | R + S                   |
| SUBR     | L              | L              | H              | 1          | S Minus R       | S - R                   |
| SUBS     | L              | H              | L              | 2          | R Minus S       | R - S                   |
| OR       | L              | H              | H              | 3          | R OR S          | R ∨ S                   |
| AND      | H              | L              | L              | 4          | R AND S         | R ∧ S                   |
| NOTRS    | H              | L              | H              | 5          | $\bar{R}$ AND S | $\bar{R} \wedge S$      |
| EXOR     | H              | H              | L              | 6          | R EX-OR S       | R ⊕ S                   |
| EXNOR    | H              | H              | H              | 7          | R EX-NOR S      | $\overline{R \oplus S}$ |

**Table 3. ALU Destination Control**

| Mnemonic | Micro Code     |                |                |            | RAM Function |         | Q-Reg. Function |         | Y Output | RAM Shifter      |                   | Q Shifter       |                  |
|----------|----------------|----------------|----------------|------------|--------------|---------|-----------------|---------|----------|------------------|-------------------|-----------------|------------------|
|          | I <sub>8</sub> | I <sub>7</sub> | I <sub>6</sub> | Octal Code | Shift        | Load    | Shift           | Load    |          | RAM <sub>0</sub> | RAM <sub>15</sub> | Q <sub>0</sub>  | Q <sub>15</sub>  |
| QREG     | L              | L              | L              | 0          | X            | None    | None            | F → Q   | F        | X                | X                 | X               | X                |
| NOP      | L              | L              | H              | 1          | X            | None    | X               | None    | F        | X                | X                 | X               | X                |
| RAMA     | L              | H              | L              | 2          | None         | F → B   | X               | None    | A        | X                | X                 | X               | X                |
| RAMF     | L              | H              | H              | 3          | None         | F → B   | X               | None    | F        | X                | X                 | X               | X                |
| RAMQD    | H              | L              | L              | 4          | DOWN         | F/2 → B | DOWN            | Q/2 → Q | F        | F <sub>0</sub>   | IN <sub>15</sub>  | Q <sub>0</sub>  | IN <sub>15</sub> |
| RAMD     | H              | L              | H              | 5          | DOWN         | F/2 → B | X               | None    | F        | F <sub>0</sub>   | IN <sub>15</sub>  | Q <sub>0</sub>  | X                |
| RAMQU    | H              | H              | L              | 6          | UP           | 2F → B  | UP              | 2Q → Q  | F        | IN <sub>0</sub>  | F <sub>15</sub>   | IN <sub>0</sub> | Q <sub>15</sub>  |
| RAMU     | H              | H              | H              | 7          | UP           | 2F → B  | X               | None    | F        | IN <sub>0</sub>  | F <sub>15</sub>   | X               | Q <sub>15</sub>  |

X = Don't care. Electrically, the input shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.

A = Register Addressed by A inputs.

B = Register Addressed by B inputs.

UP is toward MSB, DOWN is toward LSB.

**Table 4. Source Operand and ALU Function Matrix**

| Octal I <sub>543</sub> | ALU Source Function                                   | 0                       | 1                       | 2         | 3         | 4         | 5                       | 6                       | 7         |
|------------------------|---|-------------------------|-------------------------|-----------|-----------|-----------|-------------------------|-------------------------|-----------|
|                        |   | A, Q                    | A, B                    | O, Q      | O, B      | O, A      | D, A                    | D, Q                    | D, O      |
| 0                      | C <sub>n</sub> = L<br>R plus S<br>C <sub>n</sub> = H  | A+Q                     | A+B                     | Q         | B         | A         | D+A                     | D+Q                     | D         |
|                        |   | A+Q+1                   | A+B+1                   | Q+1       | B+1       | A+1       | D+A+1                   | D+Q+1                   | D+1       |
| 1                      | C <sub>n</sub> = L<br>S minus R<br>C <sub>n</sub> = H | Q-A-1                   | B-A-1                   | Q-1       | B-1       | A-1       | A-D-1                   | Q-D-1                   | -D-1      |
|                        |   | Q-A                     | B-A                     | Q         | B         | A         | A-D                     | Q-D                     | -D        |
| 2                      | C <sub>n</sub> = L<br>R minus S<br>C <sub>n</sub> = H | A-Q-1                   | A-B-1                   | -Q-1      | -B-1      | -A-1      | D-A-1                   | D-Q-1                   | D-1       |
|                        |   | A-Q                     | A-B                     | -Q        | -B        | -A        | D-A                     | D-Q                     | D         |
| 3                      | R OR S  | A ∨ Q                   | A ∨ B                   | Q         | B         | A         | D ∨ A                   | D ∨ Q                   | D         |
| 4                      | R AND S   | A ∧ Q                   | A ∧ B                   | 0         | 0         | 0         | D ∧ A                   | D ∧ Q                   | 0         |
| 5                      | $\bar{R}$ AND S                                       | $\bar{A} \wedge Q$      | $\bar{A} \wedge B$      | Q         | B         | A         | $\bar{D} \wedge A$      | $\bar{D} \wedge Q$      | 0         |
| 6                      | R EX-OR S   | A ⊕ Q                   | A ⊕ B                   | Q         | B         | A         | D ⊕ A                   | D ⊕ Q                   | D         |
| 7                      | R EX-NOR S  | $\overline{A \oplus Q}$ | $\overline{A \oplus B}$ | $\bar{Q}$ | $\bar{B}$ | $\bar{A}$ | $\overline{D \oplus A}$ | $\overline{D \oplus Q}$ | $\bar{D}$ |

+ = Plus; - = Minus; ∨ = OR; ∧ = AND; ⊕ = EX-OR

## Description of Architecture

### General Description

The 7C9101 diagram is shown in Figure 1. Detailed block diagrams show the operation of specific sections as described below. The device is a 16-bit slice consisting of a register file (16-word by 16-bit dual port RAM), the ALU, the Q-register and the necessary control logic. It is expandable in 16-bit increments.

### Register File

The dual port RAM is addressed by two 4-bit address fields ( $A_{3-0}$  and  $B_{3-0}$ ) which cause the data to simultaneously appear at the A or B (internal) ports. Both the A and B addresses may be identical; in this case, the same data will appear at both the A and B ports.

Data to be written to RAM is applied to the D inputs of the 7C9101 and is passed (unchanged) through the ALU to the RAM location specified by the B-address word. New data is written into the RAM by specifying a B address

while RAM write enable (RAM EN) is active and the clock input is LOW. RAM EN is an internal signal decoded from the signals  $I_6, 7, 8$ . As shown below, each of the 16 RAM inputs is driven by a three-input multiplexer that allows the ALU output ( $F_{15-0}$ ) to be shifted one bit position to the left, right, or not shifted. The  $RAM_{15}$  and  $RAM_0$  I/O pins are also inputs to the 16-bit, 3-input multiplexer.

During the left shift (upshift) operation, the  $RAM_{15}$  output buffer and  $RAM_0$  input multiplexer are enabled. For the down shift (right) operation, the  $RAM_0$  output buffer and the  $RAM_{15}$  input multiplexer are enabled.

The A and B outputs of the RAM drive separate 16-bit latches that are enabled (track the RAM data) when the clock is HIGH. The outputs of the A latch go to three multiplexers which feed the two ALU inputs ( $R_{15-0}$  and  $S_{15-0}$ ) and the chip output ( $Y_{15-0}$ ). The B latch outputs are directed to the multiplexer which feeds the S input to the ALU.

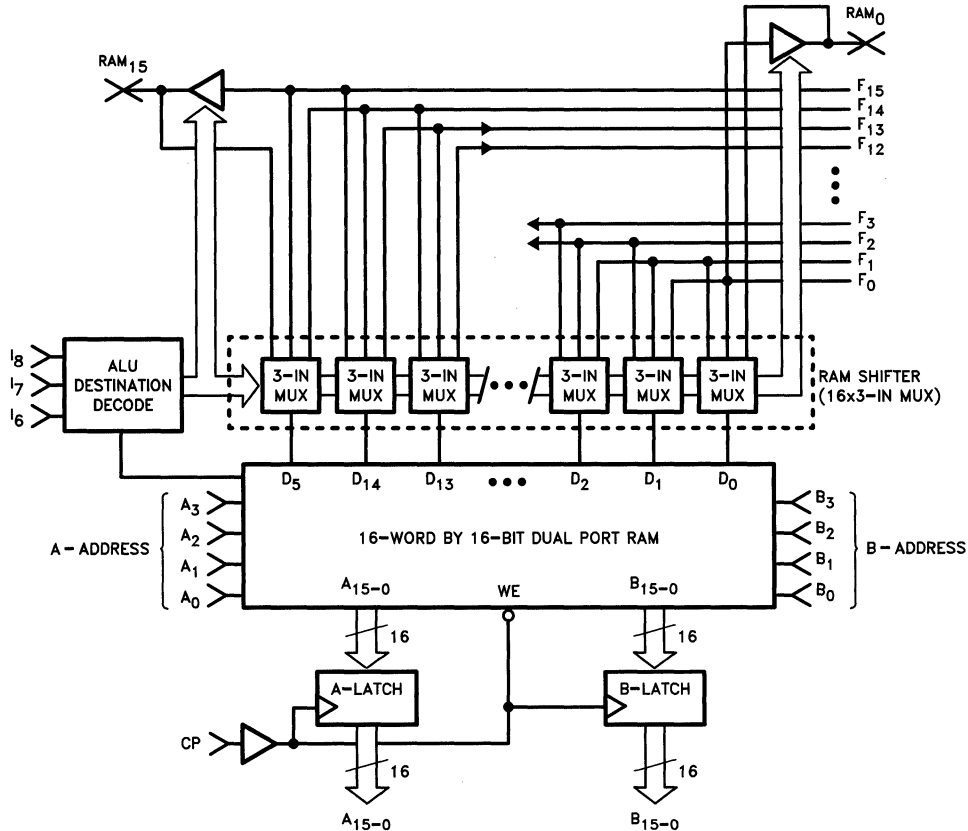


Figure 2. Register File

0079-4

**Description of Architecture (Continued)**

**Q-Register**

The Q-register is mainly intended for use as a separate working register for multiplication and division routines. It may also function as an accumulator or temporary storage register. Sixteen master-slave latches are used to implement the Q-register. As shown below, the Q-register inputs are driven by the outputs of the Q-shifter (sixteen 3-input mul-

tiplexers, under the control of  $I_6, 7, 8$ ). The function of the Q-register input multiplexers is to allow the ALU output ( $F_{15-0}$ ) to be either shifted left, right, or directly entered into the master latches. The  $Q_{15}$  and  $Q_0$  pins (I/O) function similarly to the  $RAM_{15}$  and  $RAM_0$  pins described earlier. Data is entered into the master latches when the clock is LOW and transferred to the slave (output) at the clock LOW to HIGH transition.

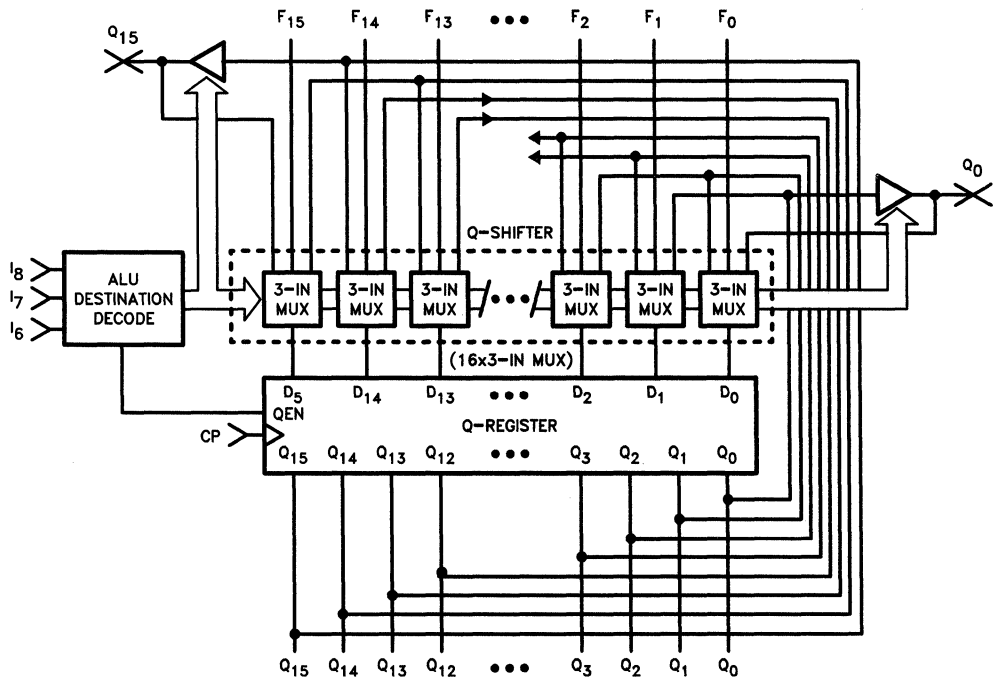


Figure 3. Q-Register

0079-5

**Description of Architecture (Continued)**

**ALU (Arithmetic Logic Unit)**

The ALU can perform three arithmetic and five logical operations on the two 16-bit input operands, R and S. The R-input multiplexer selects between data from the RAM A-port and data at the external data input, D<sub>15-0</sub>. The S-input multiplexer selects between data from the RAM A-port, the RAM B-port, and the Q-register. The R and S multiplexers are controlled by the I<sub>0, 1, 2</sub> inputs as shown in Table 1. The R and S input multiplexers each have an "inhibit capability," offering a state where no data is passed. This is equivalent to a source operand consisting of all zeroes. The R and S ALU source multiplexers are configured to allow eight pairs of combinations of A, B, D, Q, and "0" to be selected as ALU input operands.

The ALU functions, which are controlled by I<sub>3, 4, 5</sub>, are shown in Table 2. Carry lookahead logic is resident on the

7C9101, using the ALU inputs carry in (C<sub>n</sub>) and the ALU outputs carry propagate (P), carry generate (G), carry out (C<sub>n+16</sub>), and overflow to implement carry lookahead arithmetic and determine if arithmetic overflow has occurred. Note that the carry in (C<sub>n</sub>) signal affects the arithmetic result and internal flags; it has no effect on the logical operations.

Control signals I<sub>6, 7, 8</sub> route the ALU data output (F<sub>15-0</sub>) to the RAM, the Q-register inputs, and the Y-outputs as shown in Table 3. The ALU result MSB (F<sub>15</sub>) is output so the user may examine the sign bit without needing to enable the three-state outputs. The F = 0 output, used for zero detection, is HIGH when all bits of the F output are LOW. It is an open drain output which may be wire OR'ed across multiple 7C9101 processor slices.

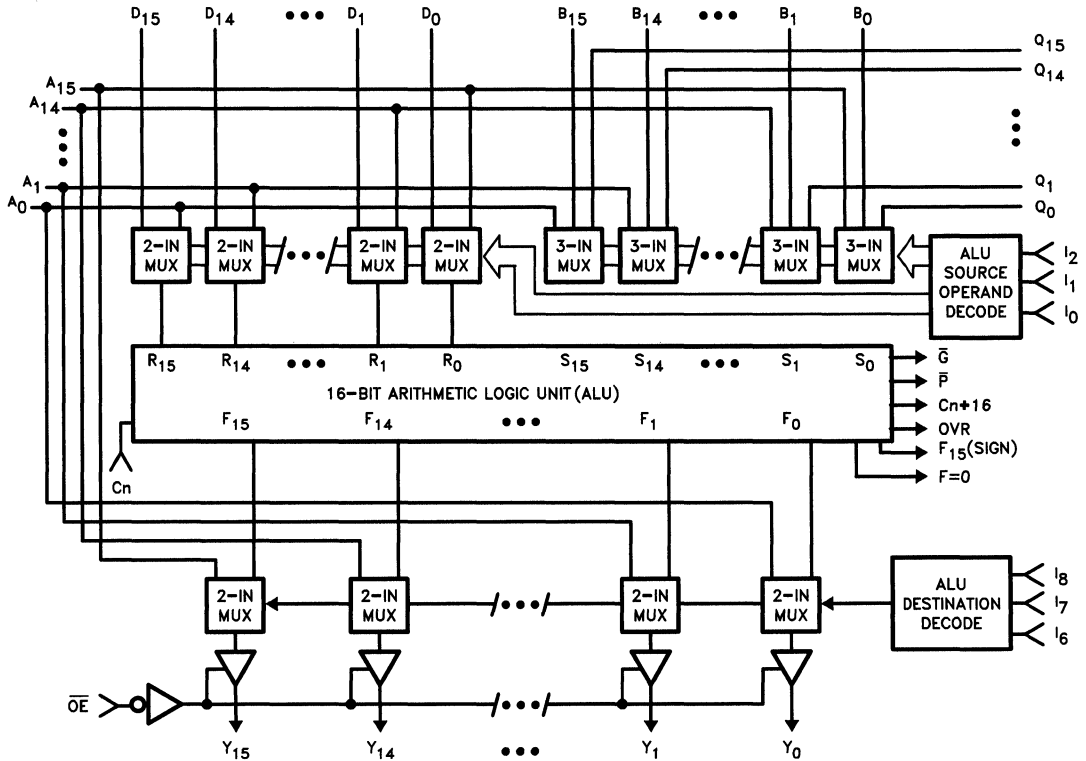


Figure 4. ALU

**Description of Architecture (Continued)**
**Table 5. ALU Logic Mode Functions**

| Octal<br>I543, I210 | Group  | Function                |
|---------------------|--------|-------------------------|
| 40                  | AND    | $A \wedge Q$            |
| 41                  |        | $A \wedge B$            |
| 45                  |        | $D \wedge A$            |
| 46                  |        | $D \wedge Q$            |
| 30                  | OR     | $A \vee Q$              |
| 31                  |        | $A \vee B$              |
| 35                  |        | $D \vee A$              |
| 36                  |        | $D \vee Q$              |
| 60                  | EX-OR  | $A \nabla Q$            |
| 61                  |        | $A \nabla B$            |
| 65                  |        | $D \nabla A$            |
| 66                  |        | $D \nabla Q$            |
| 70                  | EX-NOR | $\overline{A \nabla Q}$ |
| 71                  |        | $\overline{A \nabla B}$ |
| 75                  |        | $\overline{D \nabla A}$ |
| 76                  |        | $\overline{D \nabla Q}$ |
| 72                  | INVERT | $\overline{Q}$          |
| 73                  |        | $\overline{B}$          |
| 74                  |        | $\overline{A}$          |
| 77                  |        | $\overline{D}$          |
| 62                  | PASS   | Q                       |
| 63                  |        | B                       |
| 64                  |        | A                       |
| 67                  |        | D                       |
| 32                  | PASS   | Q                       |
| 33                  |        | B                       |
| 34                  |        | A                       |
| 37                  |        | D                       |
| 42                  | "ZERO" | 0                       |
| 43                  |        | 0                       |
| 44                  |        | 0                       |
| 47                  |        | 0                       |
| 50                  | MASK   | $\overline{A} \wedge Q$ |
| 51                  |        | $\overline{A} \wedge B$ |
| 55                  |        | $\overline{D} \wedge A$ |
| 56                  |        | $\overline{D} \wedge Q$ |

**Table 6. ALU Arithmetic Mode Functions**

| Octal<br>I543, I210 | $C_n = 0$ (Low)         |          | $C_n = 1$ (High)        |          |
|---------------------|-------------------------|----------|-------------------------|----------|
|                     | Group                   | Function | Group                   | Function |
| 00                  | ADD                     | $A+Q$    | ADD plus one            | $A+Q+1$  |
| 01                  |                         | $A+B$    |                         | $A+B+1$  |
| 05                  |                         | $D+A$    |                         | $D+A+1$  |
| 06                  |                         | $D+Q$    |                         | $D+Q+1$  |
| 02                  | PASS                    | Q        | Increment               | $Q+1$    |
| 03                  |                         | B        |                         | $B+1$    |
| 04                  |                         | A        |                         | $A+1$    |
| 07                  |                         | D        |                         | $D+1$    |
| 12                  | Decrement               | $Q-1$    | PASS                    | Q        |
| 13                  |                         | $B-1$    |                         | B        |
| 14                  |                         | $A-1$    |                         | A        |
| 27                  |                         | $D-1$    |                         | D        |
| 22                  | 1's Comp.               | $-Q-1$   | 2's Comp.<br>(Negate)   | $-Q$     |
| 23                  |                         | $-B-1$   |                         | $-B$     |
| 24                  |                         | $-A-1$   |                         | $-A$     |
| 17                  |                         | $-D-1$   |                         | $-D$     |
| 10                  | Subtract<br>(1's Comp.) | $Q-A-1$  | Subtract<br>(2's Comp.) | $Q-A$    |
| 11                  |                         | $B-A-1$  |                         | $B-A$    |
| 15                  |                         | $A-D-1$  |                         | $A-D$    |
| 16                  |                         | $Q-D-1$  |                         | $Q-D$    |
| 20                  |                         | $A-Q-1$  |                         | $A-Q$    |
| 21                  |                         | $A-B-1$  |                         | $A-B$    |
| 25                  |                         | $D-A-1$  |                         | $D-A$    |
| 26                  |                         | $D-Q-1$  |                         | $D-Q$    |

**Conventional Addition and Pass-Increment/  
Decrement**

When the carry-in is HIGH and either a conventional addition or a PASS operation is performed, one (1) is added to the result. If the DECREMENT operation is performed when the carry-in is LOW, the value of the operand is reduced by one. However, when the same operation is performed when the carry-in is HIGH, it nullifies the DECREMENT operation so that the result is equivalent to the PASS operation. In logical operations, the carry-in ( $C_n$ ) will not affect the ALU output.

**Subtraction**

Recall that in two's complement integer coding  $-1$  is equal to all ones and that in one's complement integer coding zero is equal to all ones. To convert a positive integer to its two's complement (negative) equivalent, invert (complement) the number and add 1 to it; i.e.,  $TWC = ONC + 1$ . In Table 6 the symbol  $-Q$  represents the two's complement of Q so that the one's complement of Q is then  $-Q - 1$ .

**Electrical Characteristics Over Commercial and Military Operating Range<sup>[4]</sup>**
 $V_{CC} \text{ Min.} = 4.5\text{V}, V_{CC} \text{ Max.} = 5.5\text{V}$ 

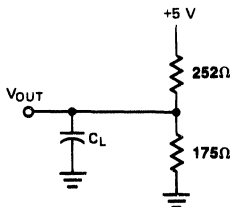
| Parameters                           | Description                                 | Test Conditions   | Min.  | Max.     | Units                          |
|--------------------------------------|---|---|---|----------|--------------------------------|
| $V_{OH}$                             | Output HIGH Voltage                         | $V_{CC} = \text{Min.}$<br>$I_{OH} = -3.4 \text{ mA}$            | 2.4   |          | V                              |
| $V_{OL}$                             | Output LOW Voltage                          | $V_{CC} = \text{Min.}$<br>$I_{OL} = 16 \text{ mA}$              |   | 0.4      | V                              |
| $V_{IH}$                             | Input HIGH Voltage                          |   | 2.0   | $V_{CC}$ | V                              |
| $V_{IL}$                             | Input LOW Voltage                           |   | -3.0  | 0.8      | V                              |
| $I_{IX}$                             | Input Leakage Current                       | $V_{SS} \leq V_{IN} \leq V_{CC}$<br>$V_{CC} = \text{Max.}$      | -10   | 10       | $\mu\text{A}$                  |
| $I_{OH}$                             | Output HIGH Current                         | $V_{CC} = \text{Min.}$<br>$V_{OH} = 2.4\text{V}$                | -3.4  |          | mA                             |
| $I_{OL}$                             | Output LOW Current                          | $V_{CC} = \text{Min.}$<br>$V_{OL} = 0.4\text{V}$                | 16  |          | mA                             |
| $I_{OZ}$                             | Output Leakage Current                      | $V_{CC} = \text{Max.}$<br>$V_{OUT} = V_{SS} \text{ to } V_{CC}$ | -40   | +40      | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{SC}$                             | Output Short Circuit Current <sup>[1]</sup> | $V_{CC} = \text{Max.}$<br>$V_{OUT} = 0\text{V}$                 |   | -85      | mA                             |
| $I_{CC}(Q_1)$ <sup>[2]</sup>         | Supply Current (Quiescent)                  | Commercial  | $V_{SS} \leq V_{IN} \leq V_{IL}$ or<br>$V_{IH} \leq V_{IN} \leq V_{CC}; \overline{OE} = \text{HIGH}$            |          | mA                             |
|                                      |   | Military  |   |          |                                |
| $I_{CC}(Q_2)$ <sup>[2]</sup>         | Supply Current (Quiescent)                  | Commercial  | $V_{SS} \leq V_{IN} \leq 0.4\text{V}$ or<br>$3.85\text{V} \leq V_{IN} \leq V_{CC}; \overline{OE} = \text{HIGH}$ |          | mA                             |
|                                      |   | Military  |   |          |                                |
| $I_{CC}(\text{Max.})$ <sup>[2]</sup> | Supply Current                              | Commercial  | $V_{CC} = \text{Max.}, f_{CLK} = 10 \text{ MHz};$<br>$\overline{OE} = \text{HIGH}$                              |          | mA                             |
|                                      |   | Military  |   |          |                                |

**5**
**Capacitance<sup>[3]</sup>**

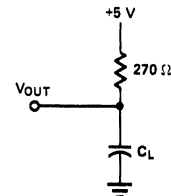
| Parameters | Description        | Test Conditions   | Max. | Units |
|------------|--------------------|---|------|-------|
| $C_{IN}$   | Input Capacitance  | $T_A = 25^\circ\text{C}, f = 1 \text{ MHz}$<br>$V_{CC} = 5.0\text{V}$ | 5    | pF    |
| $C_{OUT}$  | Output Capacitance |   | 7    |       |

**Notes:**

- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
- Two quiescent figures are given for different input voltage ranges. To calculate  $I_{CC}$  at any given frequency, use  $I_{CC}(Q_1) + I_{CC}(A.C.)$  where  $I_{CC}(Q_1)$  is shown above and  $I_{CC}(A.C.) = (3 \text{ mA/MHz}) \times \text{Clock Frequency}$  for the Commercial temperature range.  $I_{CC}(A.C.) = (5 \text{ mA/MHz}) \times \text{Clock Frequency}$  for Military temperature range.
- Tested initially and after any design or process changes that may affect these parameters.
- See the last page of this specification for Group A subgroup testing information.

**Output Loads used for AC Performance Characteristics**


0079-9

**All Outputs except Open Drain**


0079-10

**Open Drain (F = 0)**
**Notes:**

- $C_L = 50 \text{ pF}$  includes scope probe, wiring and stray capacitance.
- $C_L = 5 \text{ pF}$  for output disable tests.



**Table 7. Logic Functions for CARRY and OVERFLOW Conditions**

| I <sub>543</sub> | Function           | $\bar{P}$   | $\bar{G}$   | C <sub>n + 16</sub> | OVR                                      |
|------------------|--------------------|---|---|---------------------|--|
| 0                | R + S              | $\overline{P_0 - P_{15}}$   | $\overline{G_{15} + P_{15}G_{14} + P_{15}P_{14}G_{13} + \dots + P_{1-15}G_0}$ | C <sub>16</sub>     | C <sub>16</sub> $\nabla$ C <sub>15</sub> |
| 1                | S - R              | ← Same as R + S equations, but substitute $\bar{R}_i$ for R <sub>i</sub> in definitions → |   |                     |  |
| 2                | R - S              | ← Same as R + S equations, but substitute $\bar{S}_i$ for S <sub>i</sub> in definitions → |   |                     |  |
| 3                | R $\vee$ S         | HIGH  | HIGH  | LOW                 | LOW                                      |
| 4                | R $\wedge$ S       |   |   |                     |  |
| 5                | $\bar{R} \wedge S$ |   |   |                     |  |
| 6                | R $\nabla$ S       |   |   |                     |  |
| 7                | $\bar{R} \nabla S$ |   |   |                     |  |

**Definitions: + = OR**

$$P_{0-15} = P_{15} P_{14} P_{13} P_{12} P_{11} P_{10} P_9 P_8 P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0$$

$$P_0 = R_0 + S_0$$

$$P_1 = R_1 + S_2$$

$$P_2 = R_2 + S_2$$

$$P_3 = R_3 + S_3, \text{ etc.}$$

$$G_{0-15} = G_{15} G_{14} G_{13} G_{12} G_{11} G_{10} G_9 G_8 G_7 G_6 G_5 G_4 G_3 G_2 G_1 G_0$$

$$G_0 = R_0 S_0$$

$$G_1 = R_1 S_1$$

$$G_2 = R_2 S_2$$

$$G_3 = R_3 S_3, \text{ etc.}$$

$$C_{16} = G_{15} + P_{15} G_{14} + P_{15} P_{14} G_{13} + \dots + P_{0-15} C_n$$

$$C_{15} = G_{14} + P_{14} G_{13} + P_{14} P_{13} G_{12} + \dots + P_{0-14} C_n$$

**CY7C9101-30 and CY7C9101-40 Guaranteed Commercial Range AC Performance Characteristics**
**Characteristics**


The tables below specify the guaranteed AC performance of these devices over the Commercial (0°C to 70°C) and Military (-55°C to +125°C) operating temperature range with V<sub>CC</sub> varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See also loading circuit information.

This data applies to parts with the following numbers:

CY7C9101-30PC CY7C9101-30DC CY7C9101-30LC CY7C9101-30JC CY7C9101-30GC

CY7C9101-40PC CY7C9101-40DC CY7C9101-40LC CY7C9101-40JC CY7C9101-40GC


**Combinational Propagation Delays. C<sub>L</sub> = 50 pF**

| To Output<br>From Input   | Y  |    | F <sub>15</sub> |    | C <sub>n + 16</sub> |    | $\bar{G}, \bar{P}$ |    | F = 0 |    | OVR |    | RAM <sub>0</sub><br>RAM <sub>15</sub> |    | Q <sub>0</sub><br>Q <sub>15</sub> |    |
|---|----|----|-----------------|----|---------------------|----|--------------------|----|-------|----|-----|----|---------------------------------------|----|-----------------------------------|----|
|   | 30 | 40 | 30              | 40 | 30                  | 40 | 30                 | 40 | 30    | 40 | 30  | 40 | 30                                    | 40 | 30                                | 40 |
| <b>CY7C9101-</b>  | 30 | 40 | 30              | 40 | 30                  | 40 | 30                 | 40 | 30    | 40 | 30  | 40 | 30                                    | 40 | 30                                | 40 |
| A, B Address  | 37 | 47 | 36              | 47 | 35                  | 44 | 32                 | 41 | 35    | 46 | 32  | 42 | 32                                    | 40 | —                                 | —  |
| D   | 29 | 34 | 28              | 34 | 25                  | 32 | 25                 | 30 | 29    | 36 | 21  | 26 | 27                                    | 33 | —                                 | —  |
| C <sub>n</sub>  | 22 | 27 | 22              | 27 | 20                  | 25 | —                  | —  | 22    | 26 | 22  | 26 | 24                                    | 30 | —                                 | —  |
| I <sub>0, 1, 2</sub>  | 32 | 40 | 32              | 40 | 30                  | 38 | 28                 | 36 | 34    | 42 | 26  | 32 | 27                                    | 35 | —                                 | —  |
| I <sub>3, 4, 5</sub>  | 34 | 43 | 33              | 42 | 33                  | 42 | 27                 | 35 | 34    | 40 | 32  | 42 | 29                                    | 38 | —                                 | —  |
| I <sub>6, 7, 8</sub>  | 19 | 22 | —               | —  | —                   | —  | —                  | —  | —     | —  | —   | —  | 22                                    | 26 | 22                                | 26 |
| A Bypass ALU<br>(I = 2XX)   | 25 | 30 | —               | —  | —                   | —  | —                  | —  | —     | —  | —   | —  | —                                     | —  | —                                 | —  |
| Clock  | 31 | 40 | 30              | 39 | 30                  | 38 | 27                 | 34 | 28    | 37 | 27  | 34 | 27                                    | 35 | 20                                | 23 |

**Cycle Time and Clock Characteristics**

| CY7C9101-   | 30     | 40     |
|---|--------|--------|
| Read-Modify-Write Cycle (from selection of A, B registers to end of cycle). | 30 ns  | 40 ns  |
| Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)         | 33 MHz | 25 MHz |
| Minimum Clock LOW Time  | 20 ns  | 25 ns  |
| Minimum Clock HIGH Time   | 10 ns  | 15 ns  |
| Minimum Clock Period  | 30 ns  | 40 ns  |

**Set-Up and Hold Times Relative to Clock (CP) Input<sup>[1]</sup>**

| Input   | CP:  |                       | Hold Time After H → L            |                       | Set-up Time Before L → H |                       | Hold Time After L → H    |                       |
|---|--|-----------------------|----------------------------------|-----------------------|--------------------------|-----------------------|--------------------------|-----------------------|
|   | Set-Up Time Before H → L   | Hold Time After H → L | Set-up Time Before L → H         | Hold Time After L → H | Set-up Time Before L → H | Hold Time After L → H | Set-up Time Before L → H | Hold Time After L → H |
| <b>CY7C9101-</b>  | <b>30</b>  | <b>40</b>             | <b>30</b>                        | <b>40</b>             | <b>30</b>                | <b>40</b>             | <b>30</b>                | <b>40</b>             |
| A, B Source Address   | 10   | 15                    | 3 <sup>[3]</sup>                 | 3 <sup>[3]</sup>      | 30 <sup>[4]</sup>        | 40 <sup>[4]</sup>     | 0                        | 0                     |
| B Destination Address   | 10   | 15                    | ← Do Not Change <sup>[2]</sup> → |                       |                          |                       | 0                        | 0                     |
| D   | —  | —                     | —                                | —                     | 22                       | 28                    | 0                        | 0                     |
| C <sub>n</sub>  | —  | —                     | —                                | —                     | 16                       | 22                    | 0                        | 0                     |
| I <sub>0, 1, 2</sub>  | —  | —                     | —                                | —                     | 26                       | 35                    | 0                        | 0                     |
| I <sub>3, 4, 5</sub>  | —  | —                     | —                                | —                     | 29                       | 37                    | 0                        | 0                     |
| I <sub>6, 7, 8</sub>  | 10   | 12                    | ← Do Not Change <sup>[2]</sup> → |                       |                          |                       | 0                        | 0                     |
| RAM <sub>0</sub> , RAM <sub>15</sub> , Q <sub>0</sub> , Q <sub>15</sub> | —  | —                     | —                                | —                     | 11                       | 14                    | 0                        | 0                     |

**5**
**Output Enable/Disable Times**

 Output disable tests performed with C<sub>L</sub> = 5 pF and measured to 0.5V change of output voltage level.

| Device      | Input           | Output | Enable | Disable |
|-------------|-----------------|--------|--------|---------|
| CY7C9101-30 | $\overline{OE}$ | Y      | 18     | 16      |
| CY7C9101-40 | $\overline{OE}$ | Y      | 22     | 19      |

**Notes:**

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".

3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.


## CY7C9101-35 and CY7C9101-45 Guaranteed Military Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Military ( $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ) operating temperature range with  $V_{\text{CC}}$  varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See also loading circuit information.

This data applies to parts with the following numbers:

CY7C9101-35DMB CY7C9101-35LMB CY7C9101-35GMB  
 CY7C9101-45DMB CY7C9101-45LMB CY7C9101-45GMB

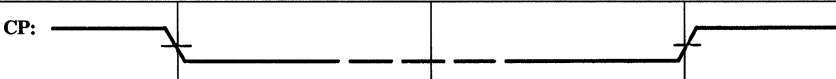
### Combinational Propagation Delays $C_L = 50 \text{ pF}^{[5]}$

| To Output<br>From Input   | Y  |    | F <sub>15</sub> |    | C <sub>n</sub> + 16 |    | G, P |    | F = 0 |    | OVR |    | RAM <sub>0</sub><br>RAM <sub>15</sub> |    | Q <sub>0</sub><br>Q <sub>15</sub> |    |
|---|----|----|-----------------|----|---------------------|----|------|----|-------|----|-----|----|---------------------------------------|----|-----------------------------------|----|
|   | 35 | 45 | 35              | 45 | 35                  | 45 | 35   | 45 | 35    | 45 | 35  | 45 | 35                                    | 45 | 35                                | 45 |
| CY7C9101-   | 35 | 45 | 35              | 45 | 35                  | 45 | 35   | 45 | 35    | 45 | 35  | 45 | 35                                    | 45 | 35                                | 45 |
| A, B Address  | 41 | 52 | 40              | 51 | 38                  | 48 | 37   | 45 | 40    | 48 | 36  | 46 | 36                                    | 43 | —                                 | —  |
| D   | 31 | 37 | 31              | 36 | 29                  | 36 | 28   | 32 | 33    | 40 | 23  | 32 | 30                                    | 35 | —                                 | —  |
| C <sub>n</sub>  | 25 | 30 | 24              | 29 | 23                  | 27 | —    | —  | 24    | 29 | 23  | 27 | 26                                    | 31 | —                                 | —  |
| I <sub>0, 1, 2</sub>  | 36 | 44 | 35              | 43 | 33                  | 41 | 31   | 38 | 38    | 46 | 29  | 38 | 30                                    | 38 | —                                 | —  |
| I <sub>3, 4, 5</sub>  | 38 | 48 | 37              | 47 | 37                  | 46 | 31   | 38 | 38    | 45 | 36  | 45 | 33                                    | 41 | —                                 | —  |
| I <sub>6, 7, 8</sub>  | 21 | 24 | —               | —  | —                   | —  | —    | —  | —     | —  | —   | —  | 24                                    | 28 | 24                                | 28 |
| A Bypass ALU<br>(I = 2XX)   | 28 | 33 | —               | —  | —                   | —  | —    | —  | —     | —  | —   | —  | —                                     | —  | —                                 | —  |
| Clock  | 35 | 44 | 34              | 43 | 34                  | 42 | 30   | 37 | 34    | 40 | 28  | 38 | 30                                    | 37 | 21                                | 25 |

## Cycle Time and Clock Characteristics<sup>[5]</sup>

| CY7C9101-   | 35     | 45     |
|---|--------|--------|
| Read-Modify-Write Cycle (from selection of A, B registers to end of cycle). | 35 ns  | 45 ns  |
| Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)         | 28 MHz | 22 MHz |
| Minimum Clock LOW Time  | 23 ns  | 28 ns  |
| Minimum Clock HIGH Time   | 12 ns  | 17 ns  |
| Minimum Clock Period  | 35 ns  | 45 ns  |

## Set-Up and Hold Times Relative to Clock (CP) Input<sup>[1, 5]</sup>

| Input   | CP:  |    |                                  |                  |                          |                   |                       |    |
|---|---|----|----------------------------------|------------------|--------------------------|-------------------|-----------------------|----|
|   | Set-Up Time Before H → L  |    | Hold Time After H → L            |                  | Set-Up Time Before L → H |                   | Hold Time After L → H |    |
| CY7C9101-   | 35  | 45 | 35                               | 45               | 35                       | 45                | 35                    | 45 |
| A, B Source Address   | 12  | 17 | 3 <sup>[3]</sup>                 | 3 <sup>[3]</sup> | 35 <sup>[4]</sup>        | 45 <sup>[4]</sup> | 0                     | 0  |
| B Destination Address   | 12  | 17 | ← Do Not Change <sup>[2]</sup> → |                  |                          |                   | 1                     | 1  |
| D   | —   | —  | —                                | —                | 25                       | 30                | 0                     | 0  |
| C <sub>n</sub>  | —   | —  | —                                | —                | 19                       | 24                | 0                     | 0  |
| I <sub>0, 1, 2</sub>  | —   | —  | —                                | —                | 30                       | 37                | 0                     | 0  |
| I <sub>3, 4, 5</sub>  | —   | —  | —                                | —                | 33                       | 40                | 0                     | 0  |
| I <sub>6, 7, 8</sub>  | 12  | 16 | ← Do Not Change <sup>[2]</sup> → |                  |                          |                   | 0                     | 0  |
| RAM <sub>0</sub> , RAM <sub>15</sub> , Q <sub>0</sub> , Q <sub>15</sub> | —   | —  | —                                | —                | 13                       | 15                | 1                     | 1  |

## Output Enable/Disable Times<sup>[5]</sup>

Output disable tests performed with  $C_L = 5 \text{ pF}$  and measured to 0.5V change of output voltage level.

| Device      | Input                  | Output | Enable | Disable |
|-------------|------------------------|--------|--------|---------|
| CY7C9101-35 | $\overline{\text{OE}}$ | Y      | 20     | 17      |
| CY7C9101-45 | $\overline{\text{OE}}$ | Y      | 23     | 20      |

### Notes:

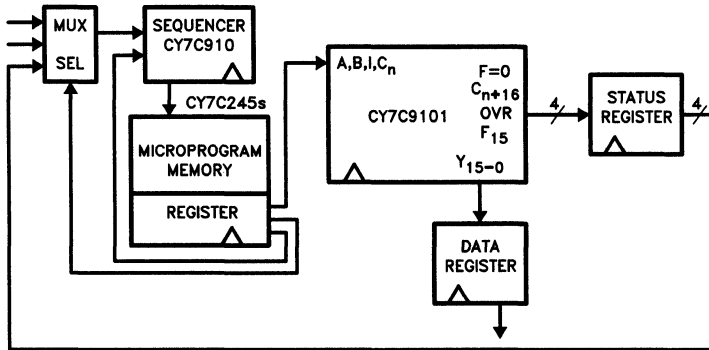
- A dash indicates a propagation delay path or set-up time constraint does not exist.
- Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".

- Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
- The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.
- See the last page of this specification for Group A subgroup testing information.

## Applications

### Minimum Cycle Time Calculations for 16-Bit Systems

Speeds used in calculations for parts other than CY7C9101 and CY7C910 are representative for available MSI parts.

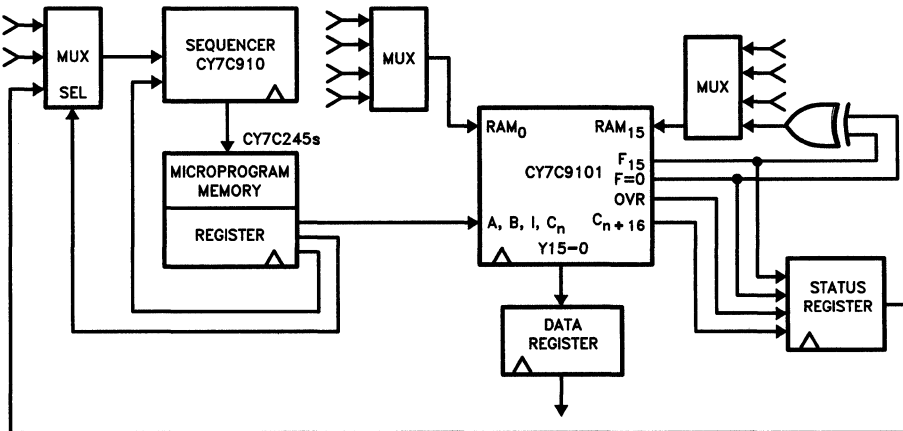


0079-15

**Pipelined System, Add without Simultaneous Shift**

| Data Loop |                           |              | Control Loop |                  |              |
|-----------|---------------------------|--------------|--------------|------------------|--------------|
| CY7C245   | Clock to Output           | 12           | CY7C245      | Clock to Output  | 12           |
| CY7C901   | A, B to Y, $C_n+16$ , OVR | 37           | MUX          | Select to Output | 12           |
| Register  | Setup                     | 4            | CY7C910      | CC to Output     | 22           |
|           |                           | <u>53 ns</u> | CY7C245      | Access Time      | 20           |
|           |                           |              |              |                  | <u>66 ns</u> |

Minimum Clock Period = 66 ns



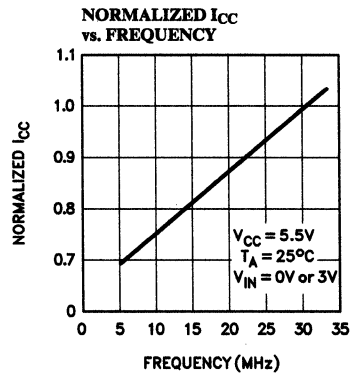
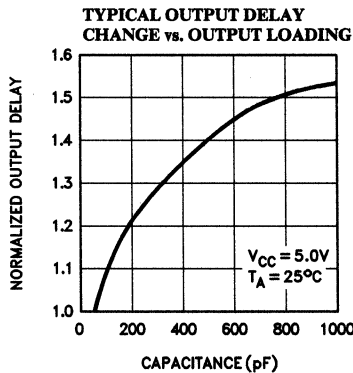
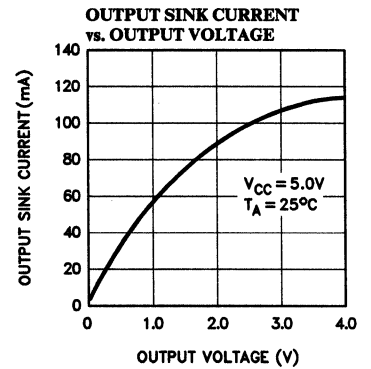
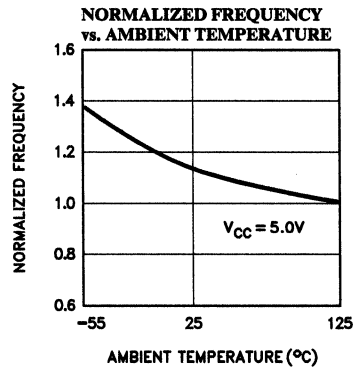
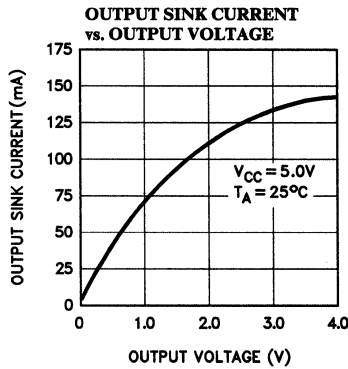
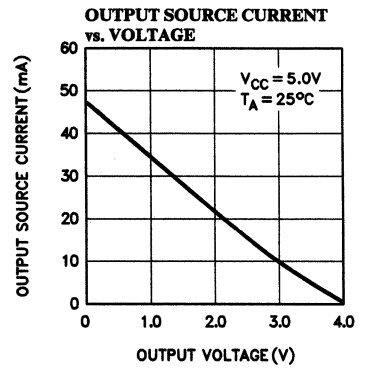
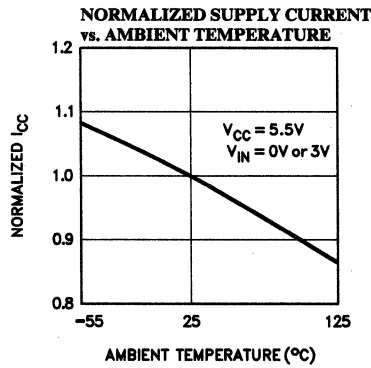
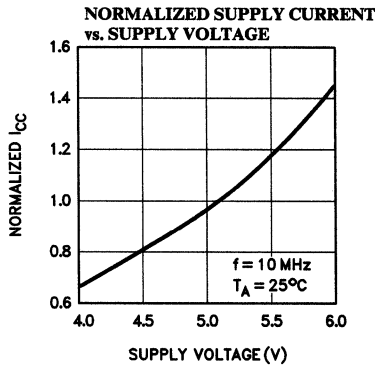
0079-13

**Pipelined System, Simultaneous Add and Shift Down (RIGHT)**

| Data Loop   |                               |              | Control Loop |                  |              |
|-------------|-------------------------------|--------------|--------------|------------------|--------------|
| CY7C245     | Clock to Output               | 12           | CY7C245      | Clock to Output  | 12           |
| CY7C9101    | A, B to Y, $C_n+16$ , OVR     | 37           | MUX          | Select to Output | 12           |
| XOR and MUX | Prop. Delay, Select to Output | 20           | CY7C910      | CC to Output     | 22           |
| CY7C9101    | $RAM_{15}$ Setup              | 11           | CY7C245      | Access Time      | 20           |
|             |                               | <u>80 ns</u> |              |                  | <u>66 ns</u> |

Minimum Clock Period = 80 ns

Typical DC and AC Characteristics



**Ordering Information**

| Speed (ns) | Ordering Code   | Package Type | Operating Range |
|------------|-----------------|--------------|-----------------|
| 30         | CY7C9101-30 PC  | P29          | Commercial      |
|            | CY7C9101-30 LC  | L81          |                 |
|            | CY7C9101-30 JC  | J81          |                 |
|            | CY7C9101-30 DC  | D30          |                 |
|            | CY7C9101-30 GC  | G68          |                 |
| 40         | CY7C9101-40 PC  | P29          | Commercial      |
|            | CY7C9101-40 LC  | L81          |                 |
|            | CY7C9101-40 JC  | J81          |                 |
|            | CY7C9101-40 DC  | D30          |                 |
|            | CY7C9101-40 GC  | G68          |                 |
| 35         | CY7C9101-35 LMB | L81          | Military        |
|            | CY7C9101-35 DMB | D30          |                 |
|            | CY7C9101-35 GMB | G68          |                 |
| 45         | CY7C9101-45 LMB | L81          | Military        |
|            | CY7C9101-45 DMB | D30          |                 |
|            | CY7C9101-45 GMB | G68          |                 |









**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters             | Subgroups |
|------------------------|-----------|
| V <sub>OH</sub>        | 1,2,3     |
| V <sub>OL</sub>        | 1,2,3     |
| V <sub>IH</sub>        | 1,2,3     |
| V <sub>IL</sub> Max.   | 1,2,3     |
| I <sub>IX</sub>        | 1,2,3     |
| I <sub>OZ</sub>        | 1,2,3     |
| I <sub>SC</sub>        | 1,2,3     |
| I <sub>CC</sub> (Q1)   | 1,2,3     |
| I <sub>CC</sub> (Q2)   | 1,2,3     |
| I <sub>CC</sub> (Max.) | 1,2,3     |

**Combinational Propagation Delays**

| Parameters   | Subgroups   |
|--|-------------|
| From A, B Address to Y                               | 7,8,9,10,11 |
| From A, B Address to F <sub>15</sub>                 | 7,8,9,10,11 |
| From A, B Address to C <sub>n+16</sub>               | 7,8,9,10,11 |
| From A, B Address to $\overline{G}$ , $\overline{P}$ | 7,8,9,10,11 |
| From A, B Address to F = 0                           | 7,8,9,10,11 |
| From A, B Address to OVR                             | 7,8,9,10,11 |
| From A, B Address to RAM <sub>0, 15</sub>            | 7,8,9,10,11 |
| From D to Y  | 7,8,9,10,11 |
| From D to F <sub>15</sub>                            | 7,8,9,10,11 |
| From D to C <sub>n+16</sub>                          | 7,8,9,10,11 |
| From D to $\overline{G}$ , $\overline{P}$            | 7,8,9,10,11 |
| From D to F = 0                                      | 7,8,9,10,11 |
| From D to OVR  | 7,8,9,10,11 |
| From D to RAM <sub>0, 15</sub>                       | 7,8,9,10,11 |
| From C <sub>n</sub> to Y                             | 7,8,9,10,11 |
| From C <sub>n</sub> to F <sub>15</sub>               | 7,8,9,10,11 |
| From C <sub>n</sub> to C <sub>n+16</sub>             | 7,8,9,10,11 |

**Combinational Propagation Delays (Continued)**

| Parameters  | Subgroups   |
|---|-------------|
| From C <sub>n</sub> to F = 0  | 7,8,9,10,11 |
| From C <sub>n</sub> to OVR  | 7,8,9,10,11 |
| From C <sub>n</sub> to RAM <sub>0, 15</sub>   | 7,8,9,10,11 |
| From I <sub>012</sub> to Y  | 7,8,9,10,11 |
| From I <sub>012</sub> to F <sub>15</sub>  | 7,8,9,10,11 |
| From I <sub>012</sub> to C <sub>n+16</sub>  | 7,8,9,10,11 |
| From I <sub>012</sub> to $\overline{G}$ , $\overline{P}$  | 7,8,9,10,11 |
| From I <sub>012</sub> to F = 0  | 7,8,9,10,11 |
| From I <sub>012</sub> to OVR  | 7,8,9,10,11 |
| From I <sub>012</sub> to RAM <sub>0, 15</sub>   | 7,8,9,10,11 |
| From I <sub>345</sub> to Y  | 7,8,9,10,11 |
| From I <sub>345</sub> to F <sub>15</sub>  | 7,8,9,10,11 |
| From I <sub>345</sub> to C <sub>n+16</sub>  | 7,8,9,10,11 |
| From I <sub>345</sub> to $\overline{G}$ , $\overline{P}$  | 7,8,9,10,11 |
| From I <sub>345</sub> to F = 0  | 7,8,9,10,11 |
| From I <sub>345</sub> to OVR  | 7,8,9,10,11 |
| From I <sub>345</sub> to RAM <sub>0, 15</sub>   | 7,8,9,10,11 |
| From I <sub>678</sub> to Y  | 7,8,9,10,11 |
| From I <sub>678</sub> to RAM <sub>0, 15</sub>   | 7,8,9,10,11 |
| From I <sub>678</sub> to Q <sub>0, 15</sub>   | 7,8,9,10,11 |
| From A Bypass ALU to Y<br>(I = 2XX)   | 7,8,9,10,11 |
| From Clock  to Y                                | 7,8,9,10,11 |
| From Clock  to F <sub>15</sub>                 | 7,8,9,10,11 |
| From Clock  to C <sub>n+16</sub>               | 7,8,9,10,11 |
| From Clock  to $\overline{G}$ , $\overline{P}$ | 7,8,9,10,11 |
| From Clock  to F = 0                           | 7,8,9,10,11 |
| From Clock  to OVR                             | 7,8,9,10,11 |
| From Clock  to RAM <sub>0, 15</sub>            | 7,8,9,10,11 |
| From Clock  to Q <sub>0, 15</sub>              | 7,8,9,10,11 |

**Set-up and Hold Times Relative to Clock (CP) Input**

| Parameters  | Subgroups   |
|---|-------------|
| A, B Source Address<br>Set-up Time Before H → L   | 7,8,9,10,11 |
| A, B Source Address<br>Hold Time After H → L      | 7,8,9,10,11 |
| A, B Source Address<br>Set-up Time Before L → H   | 7,8,9,10,11 |
| A, B Source Address<br>Hold Time After L → H      | 7,8,9,10,11 |
| B Destination Address<br>Set-up Time Before H → L | 7,8,9,10,11 |
| B Destination Address<br>Hold Time After H → L    | 7,8,9,10,11 |
| B Destination Address<br>Set-up Time Before L → H | 7,8,9,10,11 |
| B Destination Address<br>Hold Time After L → H    | 7,8,9,10,11 |
| D Set-up Time Before L → H                        | 7,8,9,10,11 |

| Parameters  | Subgroups   |
|---|-------------|
| D Hold Time After L → H   | 7,8,9,10,11 |
| C <sub>n</sub> Set-up Time Before L → H   | 7,8,9,10,11 |
| C <sub>n</sub> Hold Time After L → H  | 7,8,9,10,11 |
| I <sub>012</sub> Set-up Time Before L → H   | 7,8,9,10,11 |
| I <sub>012</sub> Hold Time After L → H  | 7,8,9,10,11 |
| I <sub>345</sub> Set-up Time Before L → H   | 7,8,9,10,11 |
| I <sub>345</sub> Hold Time After L → H  | 7,8,9,10,11 |
| I <sub>678</sub> Set-up Time Before H → L   | 7,8,9,10,11 |
| I <sub>678</sub> Hold Time After H → L  | 7,8,9,10,11 |
| I <sub>678</sub> Set-up Time Before L → H   | 7,8,9,10,11 |
| I <sub>678</sub> Hold Time After L → H  | 7,8,9,10,11 |
| RAM <sub>0</sub> , RAM <sub>15</sub> , Q <sub>0</sub> , Q <sub>15</sub><br>Set-up Time Before L → H | 7,8,9,10,11 |
| RAM <sub>0</sub> , RAM <sub>15</sub> , Q <sub>0</sub> , Q <sub>15</sub><br>Hold Time After L → H    | 7,8,9,10,11 |

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**5**





**CMOS 16-Bit  
Microprogrammed ALU**

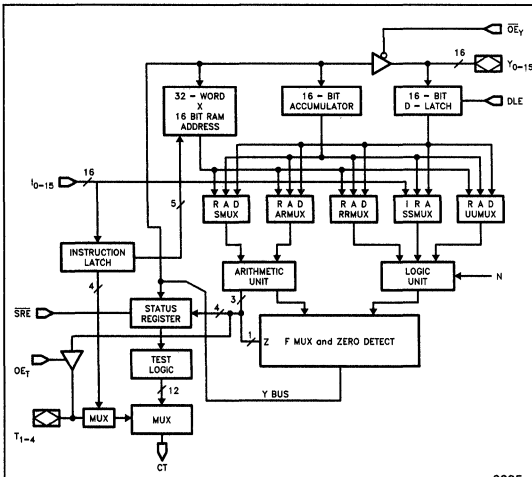
**Features**

- **Fast**
  - 35 ns worst case propagation delay, I to Y
- **Low power CMOS**
  - $I_{CC}$  (max. at 10 MHz) = 145 mA (commercial)
  - $I_{CC}$  (max. static) = 68 mA (commercial)
- **$V_{CC}$  margin**
  - $5V \pm 10\%$
  - All parameters guaranteed over commercial and military operating temperature range
- **Instruction set and architecture optimized for high speed controller applications**
- **CY7C9117 separate I/O**
  - One and two operand arithmetic and logical operations
  - Bit manipulation, field insertion/extraction instructions
  - Eleven types of instructions
- **Immediate instruction capability**
- **16-bit barrel shifter capability**
- **32-word x 16-bit register file**
- **8-bit status register**
  - Four ALU status bits
  - Link bit and three user definable status bits
- **ESD protection**
  - Capable of withstanding greater than 2001V static discharge voltage
- **Pin compatible and functionally equivalent to 29116, 29116A, 29C116, 29117, 29117A, 29C117**

**Functional Description**

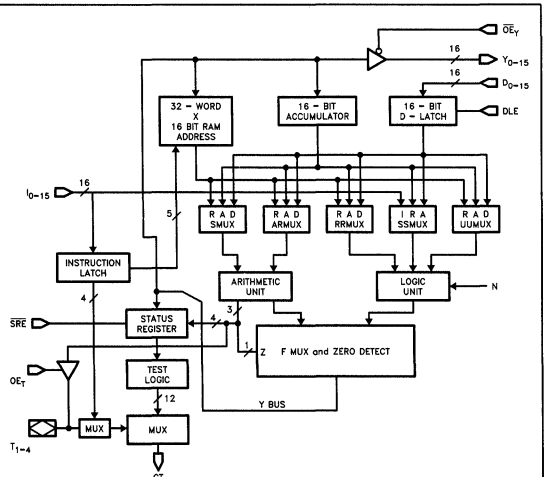
The CY7C9115, CY7C9116 and CY7C9117 are high speed 16-bit microprogrammed Arithmetic and Logic Units, (ALU).

The architecture and instruction set of the devices are optimized for peripheral controller applications such as disk controllers, graphics controllers, communications controllers, and modems.



0085-4

**Figure 1. CY7C9115, CY7C9116 Block Diagram**



0085-5

**Figure 2. CY7C9117 Block Diagram**

**Selection Guide**

|  |                   | <b>7C911X-35</b> | <b>7C911X-40/45</b> | <b>7C911X-65</b> | <b>7C911X-79</b> |
|--|-------------------|------------------|---------------------|------------------|------------------|
| <b>Worst Case I-Y Propagation Delay (ns)</b>   | <b>Commercial</b> | 35               | 45                  | 65               |                  |
|  | <b>Military</b>   |                  | 40                  | 65               | 79               |
| <b>Maximum Operating Current @ 10 MHz (mA)</b> | <b>Commercial</b> | 145              | 145                 | 145              |                  |
|  | <b>Military</b>   |                  | 166                 | 166              | 166              |

### Functional Description (Continued)

When used with the CY7C517 multiplier, the CY7C9115, CY7C9116 and CY7C9117 also support microprogrammed processor applications.

The CY7C9115, CY7C9116 and CY7C9117 are shown in the block diagram, consists of a 32-word by 16-bit single-port RAM register file, a 16-bit arithmetic unit and logic unit, an instruction latch and decoder, a data latch, an accumulator register, a 16-bit barrel shifter, a priority encoder, a status register, a condition code generator and multiplexer, and three-state output buffers.

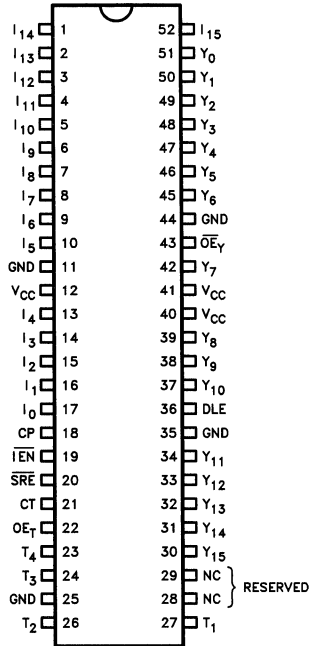
The instruction set of the CY7C9115, CY7C9116 and CY7C9117 can be divided into eleven instruction types: single-operand, two-operand, single-bit shifts, rotate and merge, rotate and compare, rotate by n-bits, bit oriented

instructions, prioritize, Cyclic Redundancy Check (CRC), status, and NO-OP. Instruction execution occurs in a single clock cycle except for Immediate Instructions, which require two clock cycles to execute.

The CY7C9116 and CY7C9117 are pin compatible, functional equivalent of the industry standard 29116, 29116A, 29C116, 29117, 29117A, 29C117 with improved performance.

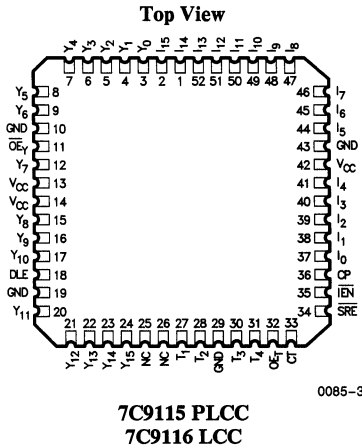
Fabricated in an advanced 1.2 micron, two-level metal CMOS process, the CY7C9115, CY7C9116 and CY7C9117 eliminates latchup, has ESD protection greater than 2001V, and achieves superior performance with low power dissipation.

### Pin Configurations CY7C9115, CY7C9116

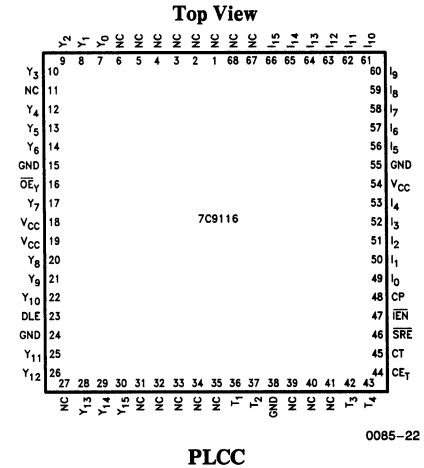


**7C9116  
DIP**

0085-2

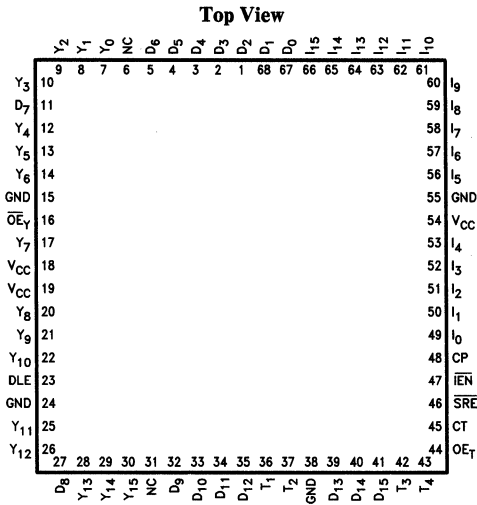


0085-3



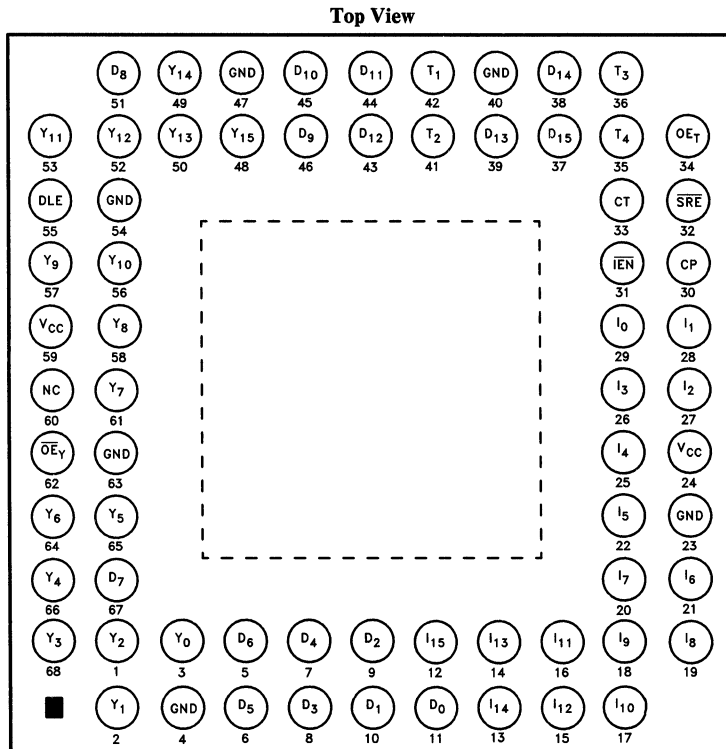
0085-22

**Pin Configurations CY7C9117**



0085-6

**LCC/PLCC**  
**NC = No Connect**



0085-7

**CY7C9117 Pin for 68 PGA**  
**NC = No Connect**

## Description of Architecture

The CY7C9115, CY7C9116 and CY7C9117 are 16-bit microprogrammed arithmetic and logic units comprised of the following sections (see block diagram):

- 32 Word x 16-Bit Register File
- Data Latch
- Instruction Latch and Decoder
- Accumulator
- Logic Unit with a 16-bit Barrel Shift Capability
- Arithmetic Unit
- Priority Encoder
- Condition Code Generator and Multiplexer
- Status Register
- Output Buffers

### 32-Word x 16-Bit Register File

The 32-word x 16-bit register file is a single port RAM with a 16-bit latch at the output. The latch is transparent while CP is HIGH and latched when CP is LOW. If IEN is LOW and the current instruction specifies the RAM as its destination, data is written into the RAM while CP is LOW. Word instructions write into all 16-bits of the RAM word addressed; byte instructions write into only the lower eight bits.

Use of an external multiplexer on five of the instruction inputs makes it possible to select separate read and write addresses for the same NON-IMMEDIATE instruction. Immediate Instructions do not allow this two-address operation for the 7C9115 and 7C9116. The 7C9117 does support two-address Immediate Instructions.

### Data Latch

The data latch holds the 16-bit input to the CY7C9115, CY7C9116 and CY7C9117 from the Y (bidirectional) bus for the 7C9115 and 7C9116 and the data bus for the 7C9117. When DLE is HIGH, the latch is transparent, it is latched when DLE is LOW.

### Instruction Latch and Decoder

The 16-bit instruction latch is always transparent, except when Immediate Instructions are executed. The Instruction Decoder decodes the instruction inputs into the internal signals which control the CY7C9115, CY7C9116 and CY7C9117. All instructions other than Immediate Instructions execute in a single clock cycle.

Execution of Immediate Instructions takes two clock cycles. During the first clock cycle, the Instruction Decoder identifies the instruction as an Immediate Instruction and the Instruction Latch captures the instruction at the instruction inputs. For Immediate Instructions, the data at the instruction inputs during the second clock cycle is used as one of the operands for the Immediate Instruction specified during the first clock cycle. Upon completion of the Immediate Instruction (the end of the second clock cycle), the Instruction Latch again becomes transparent.

### Accumulator

The accumulator is a 16-bit edge triggered register. If the IEN is LOW and the current instruction specifies the accumulator as its destination, the accumulator accepts Y input

data at the clock LOW to HIGH transition. Word instructions write into all 16 bits of the accumulator, byte instructions write into the lower eight bits.

### 16-Bit Barrel Shifter

The barrel shifter can rotate data input to it from either the register file, the accumulator, or the data latch from 0 to 15 bit positions. In word mode, the barrel shifter rotates a 16-bit word; in byte mode, it only affects the lower eight bits. The barrel shifter is used as one of the ALU inputs.

### Arithmetic and Logic Unit

The CY7C9115, CY7C9116 and the CY7C9117 have an arithmetic unit and a logic unit. The arithmetic unit is capable of operating on one or two operands while the logic unit is capable of operating on one, two or three operands. The two units in parallel are able to execute the one and two operand instructions such as pass, complement, two's complement, add, subtract, AND, OR, EXOR, NAND, NOR, and EXNOR. Three operand instructions include rotate/merge and rotate/masked compare. There are three data types supported by the CY7C9115, CY7C9116 and CY7C9117; bit, byte, and 16-bit word.

All arithmetic and logic unit operations can be performed in either word or byte mode, with byte instructions performed only on the lower eight bits.

Three status output are generated by the arithmetic unit: carry (C), negative (N), and overflow (OVR). A zero flag (Z) detects a zero condition, though this flag is not generated by the arithmetic unit or the logic unit. These flags are generated in either word or byte mode, as appropriate.

The arithmetic unit uses full carry look-ahead across all 16 bits during arithmetic operations. The carry input to the arithmetic unit comes from the carry multiplexer, which can select either zero, one, or a stored carry bit (QC) from the status register. Multiprecision arithmetic uses QC as the carry input.

### Priority Encoder

The priority encoder generates a binary-weighted code based on the location of the highest order ONE in its input word or byte. The operand to be prioritized may be AND-ed with a mask to eliminate certain bits from the priority encoding. This masking is performed by the logic unit.

In word mode, the output is a binary one if bit 15 is the first (unmasked) HIGH encountered, a binary two if bit 14 is the first HIGH and so on. If bit 0 is the only HIGH, the output of the priority encoder is binary 16. If no bits are HIGH, a binary zero is output.

In byte mode, only bits 7 through 0 are examined. Bit 7 HIGH produces a binary one, bit 6 a binary two, and so on. If bit 0 is the only HIGH, a binary eight is output; if no bits are HIGH, a binary zero is output.

### Condition Code Generator and Multiplexer

The twelve condition code test signals are generated in this section. The multiplexer selects one of these twelve and places it at the CT output. The multiplexer is addressed by either using the Test Instruction or by using the bidirec-

## Description of Architecture (Continued)

tional T bus as an input. The test instruction specifies the test condition to be placed at the CT output, but it does not allow an ALU operation at the same time. Using the T bus as input, the CY7C9115, CY7C9116 and CY7C9117 may simultaneously test and execute an instruction. The test instruction lines (I<sub>4-0</sub>) take precedence over T<sub>4-1</sub> for test-ing status.

### Status Register

The 8-bit status word is held by the status register. The status register is updated at the end of all instructions ex-cept NO-OP, Save Status, and Test Status, provided the status register enable ( $\overline{SRE}$ ) and instruction enable ( $\overline{IEN}$ ) are both LOW. The status register is inhibited from chang-ing if either  $\overline{SRE}$  or  $\overline{IEN}$  are HIGH.

The lower four status bits are the ALU status: OVR (over-flow), N (negative), C (carry), and Z (zero). The upper four bits are a link bit and three user-defined status bits (Flag1, Flag2, Flag3).

As stated above, when  $\overline{IEN}$  and  $\overline{SRE}$  are LOW, the status register is updated at the end of all instructions other than NO-OP, Save Status, and Test Status. The lower four status bits are updated under the above conditions, with the additional exception of when  $\overline{IEN}$  and  $\overline{SRE}$  are LOW and the Status Set/Reset instruction is performed on the upper four bits. When  $\overline{IEN}$  and  $\overline{SRE}$  are LOW, the upper four status bits are only changed during their correspond-ing Status Set/Reset instructions and during Status Load instructions in word mode. The Link-Status bit is also up-dated after every shift instruction.

The status register can be loaded via the internal Y bus; it can also be selected as a source for the internal Y bus. Loading the status register in word mode updates all eight bits of the status register. In byte mode, only the lower four bits are updated.

Using the status register as a source in the word mode loads all eight bits into the lower byte of the destination; the upper byte is zero-filled. In byte mode, the status regis-ter loads the lower byte of the destination; however the upper byte is unchanged. Interrupt and subroutine process-ing is facilitated by this store/load combination, which al-lows saving and restoring the status register. The lower four bits of the status register can be read directly by out-putting them to the T<sub>4-1</sub> outputs. These outputs are en-abled when OE<sub>T</sub> is HIGH.

### Output Buffers

Two sets of bidirectional buses exist on the CY7C9115 and CY7C9116. The bidirectional Y bus (16 bits) is controlled by  $\overline{OE}_Y$ . The three state outputs are enabled when  $\overline{OE}_Y$  is LOW, they are at high impedance when  $\overline{OE}_Y$  is HIGH. This will allow data to be input to the data latch from the external world. The second bidirectional bus is the four-bit T bus. These three state buffers are enabled by a HIGH on OE<sub>T</sub>, which will output the internal ALU status bits (OVR, N, C, Z). If OE<sub>T</sub> is LOW, the T outputs are at high impedance, and a test condition can be input on the T bus to determine the CT output.

The 7C9117 has separate Y bus output and Data Input buses. All other pins are functionally equivalent to the 7C9115 and 7C9116.

## Pin Definitions

| Signal Name       | I/O | Description  |
|-------------------|-----|--|
| Y <sub>15-0</sub> | I/O | <b>Data Input/Output.</b> These bidirectional lines are used to directly load the 16-bit data latch when $\overline{OE}_Y$ is HIGH. When $\overline{OE}_Y$ is LOW, the arithmetic unit or the logic unit output data is output on Y <sub>15-0</sub> .  |
| I <sub>15-0</sub> | I   | <b>Instruction Word.</b> This 16-bit word selects the functions performed by the 7C9116. These lines are also used to input data when executing Imme-diate Instructions.   |
| T <sub>4-1</sub>  | I/O | <b>Status Input/Output.</b> These bidirectional pins are used to output the lower four status bits (OVR, N, C, and Z) when OE <sub>T</sub> is HIGH. When OE <sub>T</sub> is LOW, these lines are used as inputs to generate the conditional test (CT) output.  |
| CT                | O   | <b>Conditional Test.</b> One of twelve condition code signals is selected by the condition code multi-plexer to be placed on the CT output. CT = HIGH for a pass condition; CT = LOW for a fail condition.   |
| DLE               | I   | <b>Data Latch Enable.</b> The 16-bit data latch is trans-pareant when DLE is HIGH and latched when DLE is LOW.   |
| $\overline{IEN}$  | I   | <b>Instruction Enable.</b> The following occurs with $\overline{IEN}$ LOW: Data may be written into the RAM when the clock is LOW, the Accumulator can accept data during the clock LOW to HIGH transition, and the Status Register can be updated when $\overline{SRE}$ is LOW. If $\overline{IEN}$ is HIGH, CT is dis-abled as a function of the instruction inputs. $\overline{IEN}$ should be LOW during the first half of the first cycle of Immediate Instructions.  |
| $\overline{SRE}$  | I   | <b>Status Register Enable.</b> The Status Register is updated at the end of all instructions except NO-OP, Save Status, and Test Status when $\overline{SRE}$ and $\overline{IEN}$ are both LOW. The Status Register is in-hibited from changing when either $\overline{SRE}$ or $\overline{IEN}$ are HIGH.  |
| $\overline{OE}_Y$ | I   | <b>Y Output Enable.</b> This controls the 16-bit Y <sub>15-0</sub> I/O port. When $\overline{OE}_Y$ is LOW, the Y-outputs are enabled, when $\overline{OE}_Y$ is HIGH, the Y outputs are disabled (high impedance).  |
| OE <sub>T</sub>   | I   | <b>T Output Enable.</b> The four bit T outputs are en-abled when OE <sub>T</sub> is HIGH; they are disabled (high impedance) when OE <sub>T</sub> is LOW.  |
| CP                | I   | <b>Clock Pulse.</b> The RAM output latch is transpar-ent when CP is HIGH; the RAM output is latched when CP goes LOW. If $\overline{IEN}$ is LOW and the current instruction specifies the RAM as the destination, then data is written into the RAM while CP is LOW. If $\overline{IEN}$ is LOW, the Accumu-lator and Status Register will accept data at the clock LOW to HIGH transition. The instruction latch becomes transparent upon exiting an Imme-diate Instruction during a LOW to HIGH clock transition. |
| D <sub>15-0</sub> | I   | These input lines are used to directly load the data latch.  |
| Y <sub>15-0</sub> | I/O | These output lines are used to present the arith-metic unit or the logic unit output when $\overline{OE}_Y$ is LOW. (CY7C9117 Y <sub>15-0</sub> and output only)   |

## Instruction Set

The instruction set of the CY7C9115, CY7C9116 and CY7C9117 is optimized for peripheral controller applications. It features: Bit Set, Bit Reset, Bit Test, Rotate and Merge, Rotate and Compare, and Cyclic-Redundancy-Check (CRC) generation, in addition to standard Single- or Two-Operand logical and arithmetic instructions. A single clock cycle will execute all but the Immediate Instructions which take 2 clock cycles.

The CY7C9115, CY7C9116 and CY7C9117 can operate in three different data modes: bit, byte and word (16 bits). The LSB of the word is used for Byte Mode. Also in Byte Mode when the status register is specified as the destination, only the LSH (OVR, N, C, Z) of the register is

updated. Save Status and Test Status instructions do not change the status register. During Test Status instructions the Y-bus (or D-bus for the CY7C9117) is undefined; the result is in the CT output.

The eleven instruction types outlined below are described in detail on the following pages.

|                  |                    |
|------------------|--------------------|
| Single-Operand   | Rotate and Compare |
| Two-Operand      | Prioritize         |
| Single Bit Shift | CRC                |
| Rotate and Merge | Status             |
| Bit-Oriented     | No-Op              |
| Rotate by n Bits |                    |

**Table 1. Operand Source-Destination Combinations**

| Instruction Type                         | Operand Combinations (Note 1) |            |  |
|--|-------------------------------|------------|--|
|  | Source (R/S)                  |            | Destination                            |
| Single Operand<br>SOR<br>SONR            | RAM (Note 2)                  |            | RAM                                    |
|  | ACC                           |            | ACC                                    |
|  | D                             |            | Y Bus                                  |
|  | D(OE)                         |            | Status                                 |
|  | D(SE)                         |            | ACC and Status                         |
|  | I                             |            | Status                                 |
| O  |                               |            |  |
| Two Operand<br>TOR1<br>TOR2<br>TONR      | Source (R)                    | Source (S) | Destination                            |
|  | RAM                           | ACC        | RAM                                    |
|  | RAM                           | I          | ACC                                    |
|  | D                             | RAM        | Y Bus                                  |
|  | D                             | ACC        | Status                                 |
|  | ACC                           | I          | ACC and Status                         |
| D  |                               | I          | Status                                 |
| Single Bit Shift<br>SHFTR<br>SHFTNR      | Source (U)                    |            | Destination                            |
|  | RAM                           |            | RAM                                    |
|  | ACC                           |            | ACC                                    |
|  | ACC                           |            | Y Bus                                  |
|  | D                             |            | RAM                                    |
|  | D                             |            | ACC                                    |
| D  |                               | Y Bus      |  |
| Rotate n Bits<br>ROTR1<br>ROTR2<br>ROTNR | Source (U)                    |            | Destination                            |
|  | RAM                           |            | RAM                                    |
|  | ACC                           |            | ACC                                    |
|  | D                             |            | Y Bus                                  |
| Bit Oriented<br>BOR1<br>BOR2<br>BONR     | Source (R/S)                  |            | Destination                            |
|  | RAM                           |            | RAM                                    |
|  | ACC                           |            | ACC                                    |
|  | D                             |            | Y Bus                                  |
| Rotate and Merge<br>ROTM<br>ROTC         | Rotated Source (U)            | Mask (S)   | Non-Rotated Source/<br>Destination (R) |
|  | D                             | I          | ACC                                    |
|  | D                             | RAM        | ACC                                    |
|  | D                             | I          | RAM                                    |
|  | D                             | ACC        | RAM                                    |
|  | ACC                           | I          | RAM                                    |
|  | RAM                           | I          | ACC                                    |
|  | RAM                           | I          | ACC                                    |

**Notes:**

1. If there is no division between the R/S operand or SOURCE and DESTINATION, the two are a given pair. If a division exists, any combination is possible.
2. RAM cannot be used as source when both ACC and STATUS are designated as a DESTINATION.
3. OPERAND and MASK must be different sources.

| Instruction Type  | Operand Combinations (Note 1) |             |  |
|---|-------------------------------|-------------|--|
|   | Rotated Source (U)            | Mask (S)    | Non-Rotated Source/<br>Destination (R) |
| Rotate and Compare<br>CDAI<br>CDRI<br>CDRA<br>CRAI            | D                             | I           | ACC                                    |
|   | D                             | I           | RAM                                    |
|   | D                             | ACC         | RAM                                    |
|   | RAM                           | I           | ACC                                    |
|   |                               |             |  |
| Prioritize (Note 3)<br>PRT1<br>PRT2<br>PRTNR                  | Source (R)                    | Mask (S)    | Destination                            |
|   | RAM                           | RAM         | RAM                                    |
|   | ACC                           | ACC         | ACC                                    |
|   | D                             | I           | Y Bus                                  |
| Cyclic Redundancy Check<br>CRCF<br>CRCR                       | Data In                       | Destination | Polynomial                             |
|   | QLINK                         | RAM         | ACC                                    |
| No Operation<br>NOOP  | —                             |             |  |
| Set Reset Status<br>SETST<br>RSTST<br>SVSTR<br>SVSTNR<br>TEST | Bits Affected                 |             |  |
|   | OVR, N, C, Z                  |             |  |
|   | LINK                          |             |  |
|   | Flag1                         |             |  |
|   | Flag2                         |             |  |
| Store Status  | Source                        |             | Destination                            |
|   | Status                        |             | RAM<br>ACC<br>Y Bus                    |
| Status Load   | Source (R)                    | Source (S)  | Destination                            |
|   | D                             | ACC         | Status                                 |
|   | ACC                           | I           | Status and ACC                         |
| Test Status   | Test Condition (CT)           |             |  |
|   | (N ⊕ OVR) + Z                 |             | Z + $\bar{C}$                          |
|   | N ⊕ OVR                       |             | N                                      |
|   | Z                             |             | LINK                                   |
|   | OVR                           |             | Flag1                                  |
|   | Low                           |             | Flag2                                  |
|   | C                             |             | Flag3                                  |

### Instruction Set (Continued)

$OE_Y$  is assumed LOW for all cases, allowing ALU outputs on the Y- or D-bus.

Instructions are individually distinguished by using OP-CODES and 2 assigned quadrant bits. Four quadrants, 0 to 3, have been assigned to each instruction type in order to ease groupings of instructions and addressing modes.

#### Single Operand Instructions

Each Single Operand Instruction contains four designators:

1. Mode (Byte or Word)
2. Opcode
3. Source
4. Address or Destination

These designators are divided into two basic categories, those which use RAM addresses and those that do not.

The instruction formats shown below are unique for each category. In both cases the desired operation, controlled by the instruction inputs, is performed on the source with the result either placed on the Y-bus or stored in the destination or both. The functions of Extending Sign Bit (D(SE)) and Binary Zero (D(OE)) over 16 bits in the Word Mode are available for cases where 8-bit to 16-bit conversion is necessary. The functions performed using Single Operand instructions update the LSB of the Status Register (OVR, N, C, Z) but do not effect the MSB (FLAG1, FLAG2, FLAG3, LINK). Single Operation instructions are limited when both the ACC and Status Register are the destination, the source cannot be RAM.

#### Single Operand Field Definitions

|      |     |    |          |    |        |   |          |   |             |
|------|-----|----|----------|----|--------|---|----------|---|-------------|
|      | 15  | 14 | 13       | 12 | 9      | 8 | 5        | 4 | 0           |
| SOR  | B/W |    | Quadrant |    | Opcode |   | SRC-Dest |   | RAM Address |
|      | 15  | 14 | 13       | 12 | 9      | 8 | 5        | 4 | 0           |
| SONR | B/W |    | Quadrant |    | Opcode |   | SRC      |   | Destination |

#### Single Operand Instruction Set

|                            | 15                 | 14                  | 13                                    | 12   | 9                                     | 8                  | 5      | 4                   | 0     |                         |                            |            |
|----------------------------|--------------------|---------------------|---------------------------------------|------|---------------------------------------|--------------------|--------|---------------------|-------|-------------------------|----------------------------|------------|
| Instruction <sup>[1]</sup> | B/W <sup>[2]</sup> | Quad <sup>[3]</sup> | Opcode                                |      |                                       | R/S <sup>[4]</sup> |        | Dest <sup>[4]</sup> |       | RAM Address/Destination |                            |            |
| SOR                        | 0 = B<br>1 = W     | 10                  | 1100                                  | MOVE | SRC → Dest                            | 0000               | SORA   | RAM                 | ACC   | 00000                   | R00                        | RAM Reg 00 |
|                            |                    |                     | 1101                                  | COMP | $\overline{SRC} \rightarrow Dest$     | 0010               | SORY   | RAM                 | Y Bus | ...                     | ...                        | ...        |
|                            | 1110               | INC                 | SRC + 1 → Dest                        | 0011 | SORS                                  | RAM                | Status | 11111               | R31   | RAM Reg 31              |                            |            |
|                            | 1111               | NEG                 | $\overline{SRC} + 1 \rightarrow Dest$ | 0100 | SOAR                                  | ACC                | RAM    |                     |       |                         |                            |            |
|                            |                    |                     |                                       | 0110 | SODR                                  | D                  | RAM    |                     |       |                         |                            |            |
|                            |                    |                     |                                       | 0111 | SOIR                                  | I                  | RAM    |                     |       |                         |                            |            |
|                            |                    |                     |                                       | 1000 | SOZR                                  | O                  | RAM    |                     |       |                         |                            |            |
|                            |                    |                     |                                       | 1001 | SOZER                                 | D(OE)              | RAM    |                     |       |                         |                            |            |
|                            |                    |                     |                                       | 1010 | SOSER                                 | D(SE)              | RAM    |                     |       |                         |                            |            |
|                            |                    |                     |                                       | 1011 | SORR                                  | RAM                | RAM    |                     |       |                         |                            |            |
| Instruction                | B/W                | Quad                | Opcode                                |      |                                       | R/S <sup>[4]</sup> |        | Destination         |       |                         |                            |            |
| SONR                       | 0 = B<br>1 = W     | 11                  | 1100                                  | MOVE | SRC → Dest                            | 0100               | SOA    | ACC                 | 00000 | NRY                     | Y Bus                      |            |
|                            |                    |                     | 1101                                  | COMP | $\overline{SRC} \rightarrow Dest$     | 0110               | SOD    | D                   | 00001 | NRA                     | ACC                        |            |
|                            |                    |                     | 1110                                  | INC  | SRC + 1 → Dest                        | 0111               | SOI    | I                   | 00100 | NRS                     | Status <sup>[5]</sup>      |            |
|                            |                    |                     | 1111                                  | NEG  | $\overline{SRC} + 1 \rightarrow Dest$ | 1000               | SOZ    | O                   | 00101 | NRAS                    | ACC, Status <sup>[5]</sup> |            |
|                            |                    |                     |                                       |      |                                       | 1001               | SOZE   | D(OE)               |       |                         |                            |            |
|                            |                    |                     | 1010                                  | SOSE | D(SE)                                 |                    |        |                     |       |                         |                            |            |

**Notes:**

1. Instruction mnemonic.
2. B = Byte Mode, W = Word Mode.
3. Quadrant subdivides instructions into categories.
4. R = Source; S = Source; Dest = Destination.
5. Status is destination,  
Status  $i \leftarrow Y_i$   $i = 0$  to 3 (byte mode)  
 $i = 0$  to 7 (word mode)

#### Y Bus and Status

| Instruction | Opcode | Description                           | B/W            | Y-Bus       | Flag3 | Flag2 | Flag1 | LINK | OVR | N | C | Z |
|-------------|--------|---------------------------------------|----------------|-------------|-------|-------|-------|------|-----|---|---|---|
| SOR<br>SONR | COMP   | $\overline{SCR} \rightarrow Dest$     | 1 = W<br>0 = B | Y → SRC     | NC    | NC    | NC    | NC   | 0   | U | 0 | U |
|             | INC    | SCR + 1 → Dest                        |                | Y → SRC + 1 | NC    | NC    | NC    | NC   | U   | U | U | U |
|             | MOVE   | SCR → Dest                            |                | Y → SRC     | NC    | NC    | NC    | NC   | 0   | U | 0 | U |
|             | NEG    | $\overline{SCR} + 1 \rightarrow Dest$ |                | Y → SRC + 1 | NC    | NC    | NC    | NC   | U   | U | U | U |

SRC = Source  
U = Update

NC = No Change  
0 = Reset

1 = Set  
 $i = 0$  to 15 when not specified

### Instruction Set (Continued)

Each Two Operand Instruction is constructed of 5 fields:

1. Mode (Byte or Word)
2. Opcode
3. R Source
4. S Source
5. Address or Destination

These instructions are further divided into those using RAM addresses and those that do not. The first type uses two formats which differ only by quadrant designator.

Functions are performed on the specified R and S sources and results are stored in the specified destination and/or placed on the Y-bus. Arithmetic functions update the least significant nibble of the Status Register (OVR, N, C, Z) while logical functions affect only the N and Z bits. Execution of logical functions clear the OVR and C bits of the Status Register.

#### Two Operand Field Definitions

|      | 15  | 14       | 13 | 12            | 9 | 8      | 5 | 4           | 0 |
|------|-----|----------|----|---------------|---|--------|---|-------------|---|
| TOR1 | B/W | Quadrant |    | SRC-SRC, Dest |   | Opcode |   | RAM Address |   |
| TOR2 | B/W | Quadrant |    | SRC-SRC, Dest |   | Opcode |   | RAM Address |   |
| TONR | B/W | Quadrant |    | SRC-SRC, Dest |   | Opcode |   | Destination |   |

#### Two Operand Instruction Set

| Instruction | B/W   | Quad  | R <sup>[1]</sup> | S <sup>[1]</sup>     | Dest <sup>[1]</sup> | Opcode | RAM Address |                                     |  |            |
|-------------|-------|-------|------------------|----------------------|---------------------|--------|-------------|-------------------------------------|--|------------|
| TOR1        | 0 = B | 00    | 0000             | TORAA                | RAM                 | ACC    | ACC         | 0000 SUBR S minus R                 | 00000 R00 RAM Reg 00<br>... ..<br>11111 R31 RAM Reg 31 |            |
|             | 1 = W |       | 0010             | TORIA                | RAM                 | I      | ACC         | 0001 SUBRC <sup>[2]</sup> S minus R |  |            |
|             |       |       | 0011             | TODRA                | D                   | RAM    | ACC         | with carry                          |  |            |
|             |       |       | 1000             | TORAY                | RAM                 | ACC    | Y Bus       | 0010 SUBS R minus S                 |  |            |
|             |       |       | 1010             | TORIY                | RAM                 | I      | Y Bus       | 0011 SUBSC <sup>[2]</sup> R minus S |  |            |
|             |       |       | 1011             | TODRY                | D                   | RAM    | Y Bus       | with carry                          |  |            |
|             |       |       | 1100             | TORAR                | RAM                 | ACC    | RAM         | 0100 ADD R plus S                   |  |            |
|             |       |       | 1110             | TORIR                | RAM                 | I      | RAM         | 0101 ADDC R plus S                  |  |            |
|             |       |       | 1111             | TODRR                | D                   | RAM    | RAM         | with carry                          |  |            |
|             |       |       | 0110             | AND                  | R • S               |        |             |                                     |  |            |
|             |       |       | 0111             | NAND                 | R • S               |        |             |                                     |  |            |
|             |       |       | 1000             | EXOR                 | R ⊕ S               |        |             |                                     |  |            |
| 1001        | NOR   | R + S |                  |                      |                     |        |             |                                     |  |            |
| 1010        | OR    | R + S |                  |                      |                     |        |             |                                     |  |            |
| 1011        | EXNOR | R ⊕ S |                  |                      |                     |        |             |                                     |  |            |
| TOR2        | 0 = B | 10    | 0001             | TODAR                | D                   | ACC    | RAM         | 0000 SUBR S minus R                 | 00000 R00 RAM Reg 00<br>... ..<br>11111 R31 RAM Reg 31 |            |
|             | 1 = W |       | 0010             | TOAIR                | ACC                 | I      | RAM         | 0001 SUBRC <sup>[2]</sup> S minus R |  |            |
|             |       |       | 0101             | TODIR                | D                   | I      | RAM         | with carry                          |  |            |
|             |       |       | 0010             | SUBS                 | R minus S           |        |             |                                     |  |            |
|             |       |       | 0011             | SUBSC <sup>[2]</sup> | R minus S           |        |             |                                     |  |            |
|             |       |       |                  |                      |                     |        |             |                                     |  | with carry |
|             |       |       | 0100             | ADD                  | R plus S            |        |             |                                     |  |            |
|             |       |       | 0101             | ADDC                 | R plus S            |        |             |                                     |  |            |
|             |       |       |                  |                      |                     |        |             |                                     |  | with carry |
|             |       |       | 0110             | AND                  | R • S               |        |             |                                     |  |            |
|             |       |       | 0111             | NAND                 | R • S               |        |             |                                     |  |            |
|             |       |       | 1000             | EXOR                 | R ⊕ S               |        |             |                                     |  |            |
| 1001        | NOR   | R + S |                  |                      |                     |        |             |                                     |  |            |
| 1010        | OR    | R + S |                  |                      |                     |        |             |                                     |  |            |
| 1011        | EXNOR | R ⊕ S |                  |                      |                     |        |             |                                     |  |            |

**Notes:**

1. R = Source
- S = Source
- Dest = Destination
2. For subtraction the carry is interpreted as borrow.



## Instruction Set (Continued)

### Two Operand Instruction Set

| Instruction | B/W   | Quad | R[1] | S[1]             | Opcode | Destination                     |                                       |
|-------------|-------|------|------|------------------|--------|---------------------------------|---------------------------------------|
| TONR        | 0 = B | 11   | 0001 | TODA             | D      | ACC                             | 0000 NRY Y Bus                        |
|             | 1 = W |      | 0010 | TOAI             | ACC    | I                               | 00001 NRA ACC                         |
|             |       |      | 0101 | TODI             | D      | I                               | 00100 NRS Status <sup>[2]</sup>       |
|             |       |      |      |                  |        |                                 | 00101 NRAS ACC, Status <sup>[2]</sup> |
|             |       |      |      |                  |        | 0000 SUBR S minus R             |                                       |
|             |       |      |      |                  |        | 0001 SUBRC S minus R with carry |                                       |
|             |       |      |      |                  |        | 0010 SUBS R minus S             |                                       |
|             |       |      |      |                  |        | 0011 SUBSC R minus S with carry |                                       |
|             |       |      |      |                  |        | 0100 ADD R plus S               |                                       |
|             |       |      |      |                  |        | 0101 ADDC R plus S with carry   |                                       |
|             |       |      |      |                  |        | 0110 AND R • S                  |                                       |
|             |       |      |      |                  |        | 0111 NAND R • S                 |                                       |
|             |       |      |      |                  |        | 1000 EXOR R ⊕ S                 |                                       |
|             |       |      |      |                  |        | 1001 NOR R + S                  |                                       |
|             |       |      |      | 1010 OR R + S    |        |                                 |                                       |
|             |       |      |      | 1011 EXNOR R ⊕ S |        |                                 |                                       |

#### Notes:

- R = Source  
S = Source
- Status is destination,  
Status  $i \leftarrow Y_i$ ,  $i = 0$  to 3 (byte mode)  
 $i = 0$  to 7 (word mode)
- For subtraction the carry is inverted.

### Y Bus and Status Contents

| Instruction          | Opcode | Description          | B/W   | Y-Bus                                   | Flag3 | Flag2 | Flag1 | LINK | OVR | N | C | Z |   |
|----------------------|--------|----------------------|-------|---|-------|-------|-------|------|-----|---|---|---|---|
| TOR1<br>TOR2<br>TONR | ADD    | R plus S             | 0 = B | $Y \leftarrow R + S$                    | NC    | NC    | NC    | NC   | U   | U | U | U |   |
|                      | ADDC   | R plus S with carry  | 1 = W | $Y \leftarrow R + S + QC$               | NC    | NC    | NC    | NC   | U   | U | U | U |   |
|                      | AND    | R • S                |       | $Y \leftarrow R_i \text{ AND } S_i$     | NC    | NC    | NC    | NC   | 0   | U | 0 | U |   |
|                      | EXOR   | R ⊕ S                |       | $Y_i \leftarrow R_i \text{ EXOR } S_i$  | NC    | NC    | NC    | NC   | 0   | U | 0 | U |   |
|                      | EXNOR  | R ⊕ S                |       | $Y_i \leftarrow R_i \text{ EXNOR } S_i$ | NC    | NC    | NC    | NC   | 0   | 0 | 0 | U |   |
|                      | NAND   | R • S                |       | $Y_i \leftarrow R_i \text{ NAND } S_i$  | NC    | NC    | NC    | NC   | 0   | U | 0 | U |   |
|                      | NOR    | R + S                |       | $Y_i \leftarrow R_i \text{ NOR } S_i$   | NC    | NC    | NC    | NC   | 0   | U | 0 | U |   |
|                      | OR     | R + S                |       | $Y_i \leftarrow R_i \text{ OR } S_i$    | NC    | NC    | NC    | NC   | 0   | U | 0 | U |   |
|                      | SUBR   | S minus R            |       | $Y \leftarrow S + \bar{R} + 1$          | NC    | NC    | NC    | NC   | NC  | U | U | U | U |
|                      | SUBRC  | S minus R with carry |       | $Y \leftarrow S + \bar{R} + QC$         | NC    | NC    | NC    | NC   | NC  | U | U | U | U |
|                      | SUBS   | R minus S            |       | $Y \leftarrow R + \bar{S} + 1$          | NC    | NC    | NC    | NC   | NC  | U | U | U | U |
|                      | SUBSC  | R minus S with carry |       | $Y \leftarrow R + \bar{S} + QC$         | NC    | NC    | NC    | NC   | NC  | U | U | U | U |

U = Update  
NC = No Change  
0 = Reset  
1 = Set  
i = 0 to 15 when not specified

## Single Bit Shift Instructions

Single Bit Shift Instructions are constructed of four fields:

- Mode (Byte or Word)
- Direction (up or down) and shift linkage
- Source
- Destination

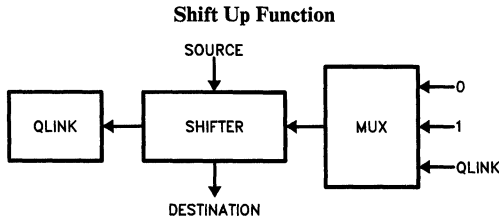
These instructions are further divided into those using RAM addresses and those that do not. The shift linkage indicator indicates what is to be loaded into the vacant bit.

During a shift up the LSB may be loaded with a zero, one or with the link status bit (QLINK), while the MSB is shifted into the QLINK bit. During a shift down, the MSB is loaded with a zero, one, the Status Carry bit (QC), the Exclusive-Or of the Negative-Status bit and the Overflow-Status bit ( $QN \oplus QOVR$ ), or the Link-Status bit. The Status Register's N and Z bits are updated, while the OVR and C bits are reset. Shift down with  $QN \oplus QOVR$  can be used in Two's Complement Multiplication.

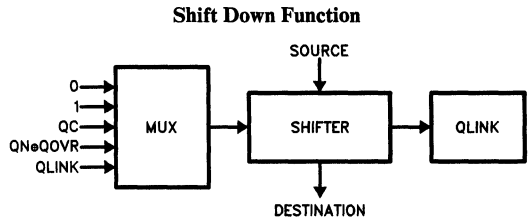
**Single Bit Shift Instructions (Continued)**

**Single Bit Shift Field Definitions**

|               |     |    |          |    |          |   |        |   |             |
|---------------|-----|----|----------|----|----------|---|--------|---|-------------|
|               | 15  | 14 | 13       | 12 | 9        | 8 | 5      | 4 | 0           |
| <b>SHFTR</b>  | B/W |    | Quadrant |    | SRC-Dest |   | Opcode |   | RAM Address |
| <b>SHFTNR</b> | B/W |    | Quadrant |    | Source   |   | Opcode |   | Destination |



0085-8



0085-9

**5**

**Single Bit Shift Instruction Set**

| Instruction | B/W                       | Quad | U[1] | Dest[1]           | Opcode              | RAM Address/Destination |                      |
|-------------|---------------------------|------|------|-------------------|---------------------|-------------------------|----------------------|
| SHFTR       | 0 = B<br>1 = W            | 10   | 0110 | SHRR              | RAM                 | 0000 SHUPZ Up 0         | 00000 R00 RAM Reg 00 |
|             |                           |      |      | RAM               | 0001 SHUP1 Up 1     |                         |                      |
|             | 0111                      |      | SHDR | D                 | 0010 SHUPL Up QLINK | 11111 R31 RAM Reg 31    |                      |
|             |                           |      | RAM  | 0100 SHDNZ Down 0 |                     |                         |                      |
|             | 0101 SHDN1 Down 1         |      |      |                   |                     |                         |                      |
|             | 0110 SHDNL Down QLINK     |      |      |                   |                     |                         |                      |
|             | 0111 SHDNC Down QC        |      |      |                   |                     |                         |                      |
|             | 1000 SHDNOV Down QN@ QOVR |      |      |                   |                     |                         |                      |
|             |                           |      |      |                   |                     |                         |                      |
| Instruction | B/W                       | Quad | U[1] |                   | Opcode              | Destination             |                      |
| SHFTNR      | 0 = B<br>1 = W            | 11   | 0110 | SHA               | ACC                 | 0000 SHUPZ Up 0         | 00000 NRY Y-Bus      |
|             |                           |      |      | D                 | 0001 SHUP1 Up 1     | 00001 NRA ACC           |                      |
|             | 0111                      |      | SHD  |                   | 0010 SHUPL Up QLINK |                         |                      |
|             |                           |      |      | 0100 SHDNZ Down 0 |                     |                         |                      |
|             | 0101 SHDN1 Down 1         |      |      |                   |                     |                         |                      |
|             | 0110 SHDNL Down QLINK     |      |      |                   |                     |                         |                      |
|             | 0111 SHDNC Down QC        |      |      |                   |                     |                         |                      |
|             | 1000 SHDNOV Down QN@ QOVR |      |      |                   |                     |                         |                      |
|             |                           |      |      |                   |                     |                         |                      |

Note:  
1. U = Source  
Dest = Destination

**Y Bus and Status**

| Instruction                                | Opcode   | Description  | B/W   | Y-Bus  | Flag3 | Flag2 | Flag1 | LINK                | OVR | N                 | C | Z |
|--|--|--|-------|--|-------|-------|-------|---------------------|-----|-------------------|---|---|
| SHR<br>SHNR                                | SHUPZ<br>SHUP1<br>SHUPL                                    | Up 0<br>Up 1<br>Up QLINK                                   | 1 = W | Y <sub>i</sub> ← SRC <sub>i-1</sub> , i = 1 to 15;<br>Y <sub>0</sub> ← Shift Input   | NC    | NC    | NC    | SRC <sub>15</sub> * | 0   | SRC <sub>14</sub> | 0 | U |
|  |  |  | 0 = B | Y <sub>i</sub> ← SRC <sub>i-1</sub> , i = 1 to 7;<br>Y <sub>0</sub> ← Shift Input;<br>Y <sub>8</sub> ← SRC <sub>7</sub> , Y <sub>i</sub> ← SRC <sub>i-9</sub><br>for i = 9 to 15 | NC    | NC    | NC    | SRC <sub>7</sub> *  | 0   | SRC <sub>6</sub>  | 0 | U |
| SHDNZ<br>SHDN1<br>SHDNL<br>SHDNC<br>SHCNOV | Down 0<br>Down 1<br>Down QLINK<br>Down QC<br>Down QN@ QOVR | Down 0<br>Down 1<br>Down QLINK<br>Down QC<br>Down QN@ QOVR | 1 = W | Y <sub>i</sub> ← SRC <sub>i+1</sub> , i = 0 to 14;<br>Y <sub>15</sub> ← Shift Input  | NC    | NC    | NC    | SRC <sub>0</sub> *  | 0   | Shift Input       | 0 | U |
|  |  |  | 0 = B | Y <sub>i</sub> ← SRC <sub>i+1</sub> , i = 0 to 6;  | NC    | NC    | NC    | SRC <sub>0</sub> *  | 0   | Shift Input       | 0 | U |
|  |  |  |       | Y <sub>i</sub> ← SRC <sub>i-7</sub> , i = 8 to 14;<br>Y <sub>7,15</sub> ← Shift Input  |       |       |       |                     |     |                   |   |   |

\*Shifted output is loaded into the QLINK.  
SRC = Source                      0 = Reset  
U = Update                        1 = Set  
NC = No Change                 i = 0 to 15 when not specified

## Instruction Set (Continued)

### Bit-Oriented Instructions

Bit-Oriented Instructions are constructed from four fields:

1. Mode (Byte or Word)
2. Operation
3. Source or Destination
4. Bit position operated on (0 = LSB)

These instructions are further divided into those using RAM addresses and those that do not. The specified function operates on the given source and the result is stored in the specified destination and/or on the Y-bus.

**Set Bit n:** Forces the nth bit to ONE without affecting other bit positions.

**Reset Bit n:** Forces the nth bit to ZERO without affecting other bit positions.

**Test Bit n:** Sets the Z status bit to the state of bit n.

**Load 2<sup>n</sup>:** Loads ZERO in bit position n and sets all other bits.

**Load 2<sup>n</sup>:** Loads ONE in bit position n and clears all other bits.

**Increment 2<sup>n</sup>:** Adds 2<sup>n</sup> to the operand.

**Decrement 2<sup>n</sup>:** Subtracts 2<sup>n</sup> from the operand.

Load, Set, Reset and Test instructions update N and Z status bits while forcing OVR and C bits to ZERO. Arithmetic operations affect the entire lower nibble of the Status Register (OVR, C, N, and Z).

### Bit Oriented Field Definitions

|      | 15  | 14 | 13       | 12 | 9 | 8 | 5      | 4 | 0           |
|------|-----|----|----------|----|---|---|--------|---|-------------|
| BOR1 | B/W |    | Quadrant |    | N |   | Opcode |   | RAM Address |
| BOR2 | B/W |    | Quadrant |    | N |   | Opcode |   | RAM Address |
| BONR | B/W |    | Quadrant |    | N |   | 1100   |   | Opcode      |

### Bit Oriented Instruction Set

| Instruction  | B/W                    | Quadrant | n       | Opcode      | RAM Address                    |                                |                 |  |
|--------------|------------------------|----------|---------|-------------|--------------------------------|--------------------------------|-----------------|--|
| BOR1         | 0 = B<br>1 = W         | 11       | 0 to 15 | 1101 SETNR  | Set RAM, bit n                 | 00000 R00                      | RAM Reg 00      |  |
|              |                        |          |         | 1110 RSTNR  | Reset RAM, bit n               | ...                            | ...             |  |
|              |                        |          |         | 1111 TSTNR  | Test RAM, bit n                | 11111 R31                      | RAM Reg 31      |  |
| BOR2         | 0 = B<br>1 = W         | 10       | 0 to 15 | 1100 LD2NR  | 2 <sup>n</sup> → RAM           | 00000 R00                      | RAM Reg 00      |  |
|              |                        |          |         | 1101 LDC2NR | 2 <sup>n</sup> → RAM           | ...                            | ...             |  |
|              |                        |          |         | 1110 A2NR   | RAM plus 2 <sup>n</sup> → RAM  | 11111 R31                      | RAM Reg 31      |  |
|              |                        |          |         | 1111 S2NR   | RAM minus 2 <sup>n</sup> → RAM |                                |                 |  |
| BONR         | 0 = B<br>1 = W         | 11       | 0 to 15 | 1100        |                                | 00000 TSTNA                    | Test ACC, bit n |  |
|              |                        |          |         |             | 00001 RSTNA                    | Reset ACC, bit n               |                 |  |
|              |                        |          |         |             | 00010 SETNA                    | Set ACC, bit n                 |                 |  |
|              |                        |          |         |             | 00100 A2NA                     | ACC plus 2 <sup>n</sup> → ACC  |                 |  |
|              |                        |          |         |             | 00101 S2NA                     | ACC minus 2 <sup>n</sup> → ACC |                 |  |
|              |                        |          |         |             | 00110 LD2NA                    | 2 <sup>n</sup> → ACC           |                 |  |
|              |                        |          |         |             | 00111 LDC2NA                   | 2 <sup>n</sup> → ACC           |                 |  |
|              |                        |          |         |             | 10000 TSTND                    | Test D, bit n                  |                 |  |
|              |                        |          |         |             | 10001 RSTND                    | Reset D, bit n                 |                 |  |
|              |                        |          |         |             | 10010 SETND                    | Set D, bit n                   |                 |  |
|              |                        |          |         |             | 10100 A2NDY                    | D plus 2 <sup>n</sup> → Y Bus  |                 |  |
|              |                        |          |         |             | 10101 S2NDY                    | D minus 2 <sup>n</sup> → Y Bus |                 |  |
|              |                        |          |         |             | 10110 LS2NY                    | 2 <sup>n</sup> → Y Bus         |                 |  |
| 10111 LDC2NY | 2 <sup>n</sup> → Y Bus |          |         |             |                                |                                |                 |  |

## Instruction Set (Continued)

### Rotate By n Bits Instructions

The Rotate by n Bits Instructions contain four indicators: byte or word mode, source, destination and the number of places the source is to be rotated. They are further subdivided into two types. The first type uses RAM as a source and/or a destination and the second type does not use RAM as a source or destination. The first type has two different formats and the only difference is in the quadrant. The second type has only one format as shown in the table. Under the control of instruction inputs, the n indicator

specifies the number of bit positions the source is to be rotated up (0 to 15), and the result is either stored in the specified destination or placed on the Y bus or both. An example of this instruction is given in Figure 5. In the Word mode, all 16-bits are rotated up; while in the Byte mode, only the lower 8-bits (0-7) are rotated up. In the Word Mode, a rotate up by n bits is equivalent to a rotate down by (16-n) bits. Similarly, in the Byte mode a rotate up by n bits is equivalent to a rotate down by (8-n) bits. The N and Z bits of the Status Register are affected and OVR and C bits are forced to ZERO.

### Rotate By n Bits Field Definitions

|       | 15 14 | 13 12    | 9 8 | 5 4      | 0           |
|-------|-------|----------|-----|----------|-------------|
| ROTR1 | B/W   | Quadrant | n   | SRC-Dest | RAM Address |
| ROTR2 | B/W   | Quadrant | n   | SRC-Dest | RAM Address |
| ROTRN | B/W   | Quadrant | n   | 1100     | SRC-Dest    |

### Rotate by n Example

EXAMPLE: n = 4, Word Mode

|             |      |      |      |      |
|-------------|------|------|------|------|
| Source      | 0001 | 0011 | 0111 | 1111 |
| Destination | 0011 | 0111 | 1111 | 0001 |

EXAMPLE: n = 4, Byte Mode

|             |      |      |      |      |
|-------------|------|------|------|------|
| Source      | 0001 | 0011 | 0111 | 1111 |
| Destination | 0001 | 0011 | 1111 | 0111 |

### Rotate By n Bits Instruction Set

| Instruction | B/W            | Quadrant | n       | U[1] |       |      | Dest[1] |       | RAM Address |            |       |     |
|-------------|----------------|----------|---------|------|-------|------|---------|-------|-------------|------------|-------|-----|
| ROTR1       | 0 = B<br>1 = W | 00       | 0 to 15 | 1100 | RTRA  | RAM  | ACC     | 00000 | R00         | RAM Reg 00 |       |     |
|             |                |          |         | 1110 | RTRY  | RAM  | Y Bus   | ...   | ...         | ...        |       |     |
|             |                |          |         | 1111 | RTRR  | RAM  | RAM     | 11111 | R31         | RAM Reg 31 |       |     |
| Instruction | B/W            | Quadrant | n       | U[1] |       |      | Dest[1] |       | RAM Address |            |       |     |
| ROTR2       | 0 = B<br>1 = W | 01       | 0 to 15 | 0000 | RTAR  | ACC  | RAM     | 00000 | R00         | RAM Reg 00 |       |     |
|             |                |          |         | 0001 | RTDR  | D    | RAM     | ...   | ...         | ...        | 11111 | R31 |
| Instruction | B/W            | Quadrant | n       | U[1] |       |      | Dest[1] |       | RAM Address |            |       |     |
| ROTRN       | 0 = B<br>1 = W | 11       | 0 to 15 | 1100 | 11000 | RTDY | D       | Y Bus | 11001       | RTDA       | D     | ACC |
|             |                |          |         |      | 11100 | RTAY | ACC     | Y Bus | 11101       | RTAA       | ACC   | ACC |

Note:

- 1. U = Source
- Dest = Destination

### Y Bus and Status

| Instruction | Opcode | B/W   | Y-Bus  | Flag3 | Flag2 | Flag1 | LINK | OVR | N            | C | Z |
|-------------|--------|-------|--|-------|-------|-------|------|-----|--------------|---|---|
| ROTR1       |        | 1 = W | $Y_i \leftarrow SRC_{(i-n) \bmod 16}$                              | NC    | NC    | NC    | NC   | 0   | $SRC_{15-n}$ | 0 | U |
| ROTR2       |        | 0 = B | $Y_i \leftarrow SRC_{i+8} = SRC_{(i-n) \bmod 8}$<br>for i = 0 to 7 | NC    | NC    | NC    | NC   | 0   | $SRC_{6-n}$  | 0 | U |
| ROTRN       |        |       |  |       |       |       |      |     |              |   |   |

SRC = Source  
U = No Change  
0 = Reset  
1 = Set

i = 0 to 15 when not specified

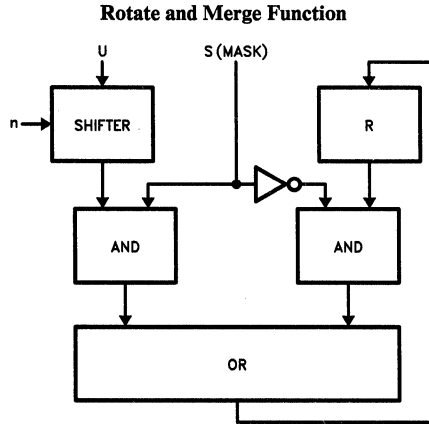
## Instruction Set (Continued)

### Rotate and Merge Instructions

Each Rotate and Merge instruction consists of five fields:

1. Mode (Byte or Word)
2. Rotated Source (U)
3. Non-Rotated Source (R)
4. Mask Location (S)
5. Number of bits Rotated (n)

The shift register rotates source U up n places. ANDing with the mask causes any bit i to be passed from the rotated source that corresponds to a set bit in mask position i. The R input is not shifted, but is masked by the compliment of mask S, so that a ZERO in mask bit i will pass bit i of R. The ORed result is stored in register R. Rotate and Merge operations update the N and Z status bits, while clearing the OVR and C bits.



0085-10

### Rotate and Merge Field Definitions

|      |       |          |     |       |             |
|------|-------|----------|-----|-------|-------------|
|      | 15 14 | 13 12    | 9 8 | 5 4   | 0           |
| ROTM | B/W   | Quadrant | n   | U,R,S | RAM Address |

EXAMPLE: n = 4, Word Mode

|             |      |      |      |      |
|-------------|------|------|------|------|
| U           | 0011 | 0001 | 0101 | 0110 |
| Rotated U   | 0001 | 0101 | 0110 | 0011 |
| R           | 1010 | 1010 | 1010 | 1010 |
| Mask (S)    | 0000 | 1111 | 0000 | 1111 |
| Destination | 1010 | 0101 | 1010 | 0011 |

### Rotate and Merge Instruction Set

| Instruction | B/W            | Quadrant | n       | U[1]  | R/Dest[1] | S[1]       | RAM Address |     |       |     |            |
|-------------|----------------|----------|---------|-------|-----------|------------|-------------|-----|-------|-----|------------|
| ROTM        | 0 = B<br>1 = W | 01       | 0 to 15 | 0111  | MDAI      | D          | ACC         | I   | 00000 | R00 | RAM Reg 00 |
|             |                |          |         | 1000  | MDAR      | D          | ACC         | RAM |       |     |            |
|             |                |          |         | 1001  | MDRI      | D          | RAM         | I   |       |     |            |
|             |                |          |         | 1010  | MDRA      | D          | RAM         | ACC |       |     |            |
|             |                |          |         | 1100  | MARI      | ACC        | RAM         | I   |       |     |            |
|             |                |          |         | 1110  | MRAI      | RAM        | ACC         | I   |       |     |            |
|             |                |          |         | 11111 | R31       | RAM Reg 31 |             |     |       |     |            |

**Note:**

1. U = Rotated Source
- R/Dest = Non-Rotated Source/Destination
- S = Mask

### Y Bus and Status

| Instruction | Opcode | B/W   | Y-Bus   | Flag3 | Flag2 | Flag1 | LINK | OVR | N | C | Z |
|-------------|--------|-------|---|-------|-------|-------|------|-----|---|---|---|
| ROTM        |        | 1 = W | $Y_i \leftarrow (\text{Non Rot Op})_i * (\text{mask})_i + (\text{Rot Op})_{(i-n) \bmod 16} * (\text{mask})_i$ | NC    | NC    | NC    | NC   | 0   | U | 0 | U |
|             |        | 0 = B | $Y_i \leftarrow (\text{Non Rot Op})_i * (\text{mask})_i + (\text{Rot Op})_{(i-n) \bmod 8} * (\text{mask})_i$  | NC    | NC    | NC    | NC   | 0   | U | 0 | U |

U = Update  
NC = No Change  
0 = Reset  
1 = Set

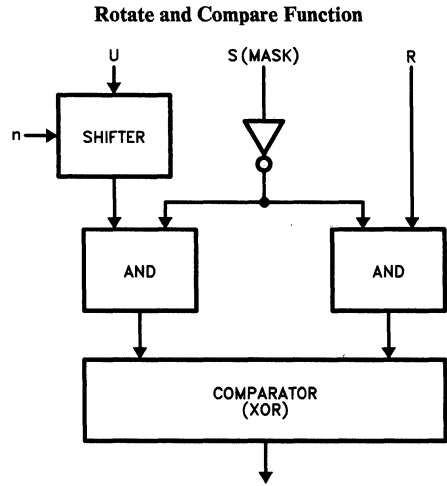
## Instruction Set (Continued)

### Rotate and Compare Instructions

The five fields of the Rotate and Compare instructions are:

1. Mode (Byte or Word)
2. Rotated Source (U)
3. Non-Rotated Source (R)
4. Mask (S)
5. Number of bits Rotated (n)

Input U is rotated n bits, ANDed with the inversion of S and compared with the input R ANDed with the inversion of S. Thus, a zero in the mask S will allow that bit of both inputs to be compared. The Z bit of the Status Register is set if the comparison passes, and reset if it does not. OVR and C bits are reset in the Status Register.



0085-11

### Rotate and Compare Field Definitions

|      | 15 14 | 13 12    | 9 8 | 5 4   | 0           |
|------|-------|----------|-----|-------|-------------|
| ROTC | B/W   | Quadrant | n   | U,R,S | RAM Address |

EXAMPLE: n = 4, Word Mode

|              |      |      |      |      |
|--------------|------|------|------|------|
| U            | 0011 | 0001 | 0101 | 0110 |
| Rotated U    | 0001 | 0101 | 0110 | 0011 |
| R            | 0001 | 0101 | 1111 | 0000 |
| Mask (S)     | 0001 | 0101 | 1111 | 1111 |
| Z (Status) = | 1    |      |      |      |

### Rotate and Compare Instruction Set

| Instruction | B/W            | Quad | n       | U[1] | R[1] | S[1] | RAM Address |     |       |     |            |
|-------------|----------------|------|---------|------|------|------|-------------|-----|-------|-----|------------|
| ROTC        | 0 = B<br>1 = W | 01   | 0 to 15 | 0010 | CDAI | D    | ACC         | I   | 00000 | R00 | RAM Reg 00 |
|             |                |      |         | 0011 | CDRI | D    | RAM         | I   | ...   | ... | ...        |
|             |                |      |         | 0100 | CDRA | D    | RAM         | ACC | ...   | ... | ...        |
|             |                |      |         | 0101 | CRAI | RAM  | ACC         | I   | 11111 | R31 | RAM Reg 31 |

Note:

- 1. U = Rotated Source
- R = Non-Rotated Source
- S = Mask

### Y Bus and Status

| Instruction | Opcode | B/W   | Y-Bus  | Flag3 | Flag2 | Flag1 | LINK | OVR | N | C | Z |
|-------------|--------|-------|--|-------|-------|-------|------|-----|---|---|---|
| ROTC        |        | 1 = W | $Y_i \leftarrow (\text{Non Rot Op})_i * (\text{mask})_i \oplus (\text{Rot Op})_{(i-n) \bmod 16} * (\text{mask})_i$ | NC    | NC    | NC    | NC   | 0   | U | 0 | U |
|             |        | 0 = B | $Y_i \leftarrow (\text{Non Rot Op})_i * (\text{mask})_i \oplus (\text{Rot Op})_{(i-n) \bmod 8} * (\text{mask})_i$  | NC    | NC    | NC    | NC   | 0   | U | 0 | U |

U = Update

NC = No Change

0 = Reset

1 = Set

i = 0 to 15 when not specified

## Instruction Set (Continued)

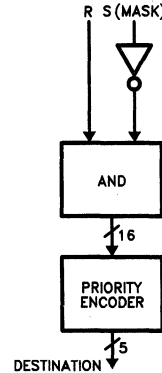
### Prioritize Instruction

The four fields of the Prioritize instruction are:

1. Mode (Byte or Word)
2. Mask Source (S)
3. Operand Source (R)
4. Destination

The inverted mask, S is ANDed with R. A "one" in S prohibits that bit from participating in the priority encoding. From the 16-bit input, the priority encoder outputs a 5-bit binary weighted code indicating the bit-position of the highest priority active bit. If there are no active bits, the output is zero. See Figure for operation in both word and byte mode. Using Prioritize updates the N and Z bits of the Status Register, and forces C and OVR to zero. This instruction is limited in that the operand and the mask must be different sources.

### Prioritize Function



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### Prioritize Instruction Field Definitions

|     | 15 14 | 13 12       | 9 8         | 5 4                         | 0 |
|-----|-------|-------------|-------------|-----------------------------|---|
| B/W | Quad  | Destination | Source (R)  | RAM Address/<br>Mask (S)    |   |
| B/W | Quad  | Mask (S)    | Destination | RAM Address/<br>Source (R)  |   |
| B/W | Quad  | Mask (S)    | Source (R)  | RAM Address/<br>Destination |   |
| B/W | Quad  | Mask (S)    | Source (R)  | Destination                 |   |

#### Word Mode

#### Byte Mode

| Highest Priority Bit Active | Encoder Output | Highest Priority Bit Active | Encoder Output |
|-----------------------------|----------------|-----------------------------|----------------|
| None                        | 0              | None                        | 0              |
| 15                          | 1              | 7                           | 1              |
| 14                          | 2              | 6                           | 2              |
| *                           | *              | *                           | *              |
| *                           | *              | *                           | *              |
| 1                           | 15             | 1                           | 7              |
| 0                           | 16             | 0                           | 8              |

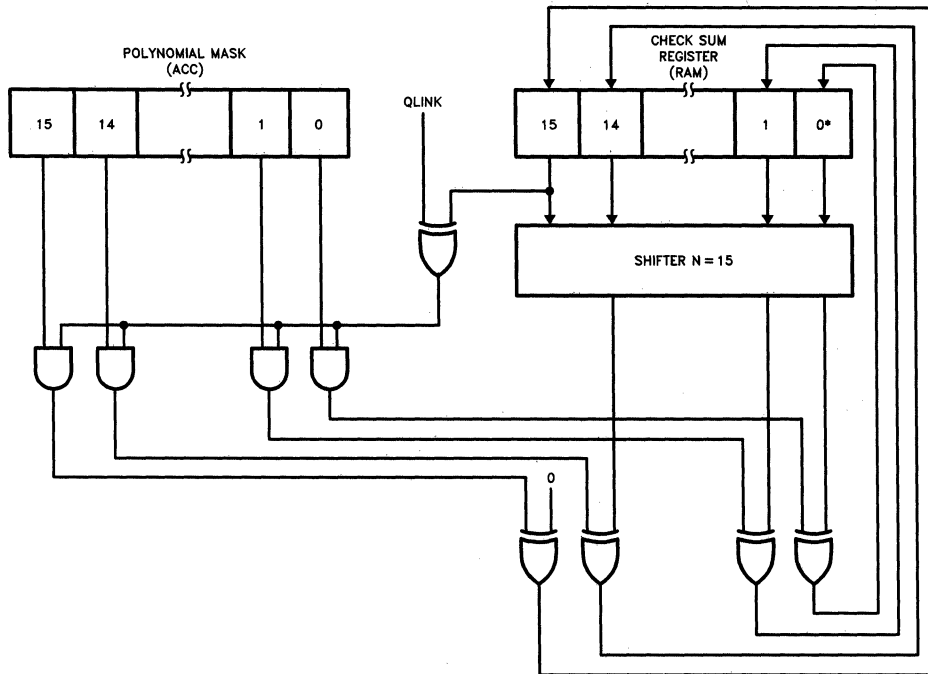
\*Bits 8 through 15 not available.

### Prioritize Instruction

| Instruction | B/W            | Quad | Destination |      |       | Source (R)  |       |       | RAM Address/Mask (S)    |            |            |
|-------------|----------------|------|-------------|------|-------|-------------|-------|-------|-------------------------|------------|------------|
| PRT1        | 0 = B<br>1 = W | 10   | 1000        | PRIA | ACC   | 0111        | RPT1A | ACC   | 00000                   | R00        | RAM Reg 00 |
|             |                |      | 1010        | PR1Y | Y Bus | 1001        | PR1D  | D     | .....                   | .....      | .....      |
|             |                |      | 1011        | PR1R | RAM   |             |       | 11111 | R31                     | RAM Reg 31 |            |
| Instruction | B/W            | Quad | Mask (S)    |      |       | Destination |       |       | RAM Address/Source (R)  |            |            |
| PRT2        | 0 = B<br>1 = W | 10   | 1000        | PRA  | ACC   | 0000        | PR2A  | ACC   | 00000                   | R00        | RAM Reg 00 |
|             |                |      | 1010        | PRZ  | O     | 0010        | PR2Y  | Y Bus | .....                   | .....      | .....      |
|             |                |      | 1011        | PRI  | I     |             |       | 11111 | R31                     | RAM Reg 31 |            |
| Instruction | B/W            | Quad | Mask (S)    |      |       | Source (R)  |       |       | RAM Address/Destination |            |            |
| PRT3        | 0 = B<br>1 = W | 10   | 1000        | PRA  | ACC   | 0011        | PR3R  | RAM   | 00000                   | R00        | RAM Reg 00 |
|             |                |      | 1010        | PRZ  | O     | 0100        | PR3A  | ACC   | .....                   | .....      | .....      |
|             |                |      | 1011        | PRI  | I     | 0110        | PR3D  | D     | 11111                   | R31        | RAM Reg 31 |
| Instruction | B/W            | Quad | Mask (S)    |      |       | Source (R)  |       |       | Destination             |            |            |
| PRTNR       | 0 = B<br>1 = W | 11   | 1000        | PRA  | ACC   | 0100        | PRTA  | ACC   | 00000                   | NR Y       | Y Bus      |
|             |                |      | 1010        | PRZ  | O     | 0110        | PRTD  | D     | 00001                   | NRA        | ACC        |
|             |                |      | 1011        | PRI  | I     |             |       |       |                         |            |            |





**Instruction Set (Continued)**
**CRC Reverse Function**


\*This bit must be transmitted first.

0085-14

**Cyclic Redundancy Check Instruction Set**

| Instruction | B/W | Quad |      |      | RAM Address |     |            |
|-------------|-----|------|------|------|-------------|-----|------------|
| CRCF        | 1   | 10   | 0110 | 0011 | 00000       | R00 | RAM Reg 00 |
|             |     |      |      |      | 11111       | R31 | RAM Reg 31 |
| Instruction | B/W | Quad |      |      | RAM Address |     |            |
| CRCR        | 1   | 10   | 0110 | 1001 | 00000       | R00 | RAM Reg 00 |
|             |     |      |      |      | 11111       | R31 | RAM Reg 31 |

**Y Bus and Status**

| Instruction | Opcode | B/W   | Y-Bus   | Flag3 | Flag2 | Flag1 | LINK         | OVR | N | C | Z |
|-------------|--------|-------|---|-------|-------|-------|--------------|-----|---|---|---|
| CRCF        |        | 1 = W | $Y_i \leftarrow [(QLINK \oplus RAM_{15}) \cdot ACC_i]$<br>$\oplus RAM_{i-1}$ for $i = 15$ to $1$<br>$Y_0 \leftarrow [(QLINK \oplus RAM_{15}) \cdot ACC_0] \oplus 0$ | NC    | NC    | NC    | $RAM_{15}^*$ | 0   | U | 0 | U |
| CRCR        |        | 1 = W | $Y_i \leftarrow [(QLINK \oplus RAM_0) \cdot ACC_i]$<br>$\oplus RAM_{i+1}$ for $i = 14$ to $0$<br>$Y_{15} \leftarrow [(QLINK \oplus RAM_0) \cdot ACC_{15}] \oplus 0$ | NC    | NC    | NC    | $RAM_0^*$    | 0   | U | 0 | U |

\*QLINK is loaded with the shifted out bit from the checksum register.

U = Update  
NC = No Change

0 = Reset  
1 = Set  
 $i = 0$  to  $15$  when not specified

### Instruction Set (Continued)

#### Status Instructions

|       |       |       |      |     |   |   |   |
|-------|-------|-------|------|-----|---|---|---|
| 7     | 6     | 5     | 4    | 3   | 2 | 1 | 0 |
| Flag3 | Flag2 | Flag1 | Link | OVR | N | C | Z |

**Set Status:** Specifies which bits in the Status Register are to be set.

**Reset Status:** Specifies which bits in the Status Register are to be cleared.

**Store Status:** Indicates byte or word and the destination into which the processor status is saved. The register is always stored in the low byte of the destination. The high byte is unchanged for RAM storage and is loaded with zeroes for ACC storage.

**Load Status:** Imbedded in the Single- and Two-Operand Instructions.

**Test Status:** Instructions specify which of the 12 possible test conditions are to be placed on the conditional test output. In addition to the 8 status bits, four logical functions may be selected:  $N \oplus OVR$ ,  $(N \oplus OVR) + Z$ ,  $Z + \bar{C}$ , and LOW. These functions are useful in testing two's complement and unsigned number arithmetic operations.

The status register may also be tested via the T bus as shown below. The instruction lines I<sub>1</sub> thru I<sub>4</sub> have bus priority for testing the status register on the CT output.

| T <sub>4</sub><br>I <sub>4</sub> | T <sub>3</sub><br>I <sub>3</sub> | T <sub>2</sub><br>I <sub>2</sub> | T <sub>1</sub><br>I <sub>1</sub> | CT                   |
|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------|
| 0                                | 0                                | 0                                | 0                                | $(N \oplus OVR) + Z$ |
| 0                                | 0                                | 0                                | 1                                | $N \oplus OVR$       |
| 0                                | 0                                | 1                                | 0                                | Z                    |
| 0                                | 0                                | 1                                | 1                                | OVR                  |
| 0                                | 1                                | 0                                | 0                                | LOW                  |
| 0                                | 1                                | 0                                | 1                                | C                    |
| 0                                | 1                                | 1                                | 0                                | $Z + \bar{C}$        |
| 0                                | 1                                | 1                                | 1                                | N                    |
| 1                                | 0                                | 0                                | 0                                | LINK                 |
| 1                                | 0                                | 0                                | 1                                | Flag1                |
| 1                                | 0                                | 1                                | 0                                | Flag2                |
| 1                                | 0                                | 1                                | 1                                | Flag3                |

#### Status

|        | 15 14 | 13 12 | 9 8  | 5 4  | 0                    |
|--------|-------|-------|------|------|----------------------|
| SETST  | 0     | Quad  | 1011 | 1010 | Opcode               |
| RSTST  | 0     | Quad  | 1010 | 1010 | Opcode               |
| SVSTR  | B/W   | Quad  | 0111 | 1010 | RAM Address/<br>Dest |
| SVSTNR | B/W   | Quad  | 0111 | 1010 | Destination          |

#### Status Instruction Set

| Instruction | B/W            | Quad |      |      | Opcode  |   |  |
|-------------|----------------|------|------|------|---|---|--|
| SETST       | 0              | 11   | 1011 | 1010 | 00011 SONCZ<br>00101 SL<br>00110 SF1<br>01001 SF2<br>01010 SF3  | Set OVR, N, C, Z<br>Set LINK<br>Set Flag1<br>Set Flag2<br>Set Flag3   |  |
| RSTST       | 0              | 11   | 1010 | 1010 | 00011 RONCZ<br>00101 RL<br>00110 RF1<br>01001 RF2<br>01010 RF3  | Reset OVR, N, C, Z<br>Reset LINK<br>Reset Flag1<br>Reset Flag2<br>Reset Flag3   |  |
| SVSTR       | 0 = B<br>1 = W | 10   | 0111 | 1010 | 00000 R00<br>11111 R31  | RAM Address/Destination<br>RAM Reg 00<br>RAM Reg 31   |  |
| SVSTNR      | 0 = B<br>1 = W | 11   | 0111 | 1010 | 00000 NRY<br>00001 NRA  | Destination<br>Y Bus<br>ACC   |  |
| Instruction | B/W            | Quad |      |      | Opcode (CT)   |   |  |
| Test        | 0              | 11   | 1001 | 1010 | 00000 TNOZ<br>00010 TNO<br>00100 TZ<br>00110 TOVR<br>01000 TLOW<br>01010 TC<br>01100 TZC<br>01110 TN<br>10000 TL<br>10010 TF1<br>10100 TF2<br>10110 TF3 | Test $(N \oplus OVR) + Z$<br>Test $N \oplus OVR$<br>Test Z<br>Test OVR<br>Test LOW<br>Test C<br>Test $Z + \bar{C}$<br>Test N<br>Test LINK<br>Test Flag1<br>Test Flag2<br>Test Flag3 |  |

Note: IEN \* test status instruction has priority over T<sub>1-4</sub> instruction.

**Instruction Set (Continued)**
**Y Bus and Status**

| Instruction     | Opcode | Description               | B/W            | Y-Bus  | Flag3 | Flag2 | Flag1 | LINK | OVR | N  | C  | Z  |
|-----------------|--------|---------------------------|----------------|--|-------|-------|-------|------|-----|----|----|----|
| RSTST           | RONCZ  | Reset OVR, N, C, Z        | 0 = B          | $Y_i \leftarrow 0$ for $i = 0$ to 15   | NC    | NC    | NC    | NC   | 0   | 0  | 0  | 0  |
|                 | RL     | Reset LINK                |                |  | NC    | NC    | NC    | 0    | NC  | NC | NC | NC |
|                 | RF1    | Reset Flag1               |                |  | NC    | NC    | 0     | NC   | NC  | NC | NC | NC |
|                 | RF2    | Reset Flag2               |                |  | NC    | 0     | NC    | NC   | NC  | NC | NC | NC |
|                 | RF3    | Reset Flag3               |                |  | 0     | NC    | NC    | NC   | NC  | NC | NC | NC |
| SETST           | SONCZ  | Set OVR, N, C, Z          | 0 = B          | $Y_i \leftarrow 1$ for $i = 0$ to 15   | NC    | NC    | NC    | NC   | 1   | 1  | 1  | 1  |
|                 | SL     | Set LINK                  |                |  | NC    | NC    | NC    | 1    | NC  | NC | NC | NC |
|                 | SF1    | Set Flag1                 |                |  | NC    | NC    | 1     | NC   | NC  | NC | NC | NC |
|                 | SF2    | Set Flag2                 |                |  | NC    | 1     | NC    | NC   | NC  | NC | NC | NC |
|                 | SF3    | Set Flag3                 |                |  | 1     | NC    | NC    | NC   | NC  | NC | NC | NC |
| SVSTR<br>SVSTNR |        | Save Status*              | 0 = B<br>1 = W | $Y_i \leftarrow$ Status for $i \leftarrow 0$ to 7;<br>$Y_i \leftarrow 0$ for $i = 8$ to 15 | NC    | NC    | NC    | NC   | NC  | NC | NC |    |
| Test            | TNOZ   | Test $(N \oplus OVR) + Z$ | 0 = B          | **   | NC    | NC    | NC    | NC   | NC  | NC | NC | NC |
|                 | TNO    | Test $(N \oplus OVR)$     |                |  | NC    | NC    | NC    | NC   | NC  | NC | NC | NC |
|                 | TZ     | Test Z                    |                |  | NC    | NC    | NC    | NC   | NC  | NC | NC | NC |
|                 | TOVR   | Test OVR                  |                |  | NC    | NC    | NC    | NC   | NC  | NC | NC | NC |
|                 | TLOW   | Test LOW                  |                |  | NC    | NC    | NC    | NC   | NC  | NC | NC | NC |
|                 | TC     | Test C                    |                |  | NC    | NC    | NC    | NC   | NC  | NC | NC | NC |
|                 | TZC    | Test $Z + \bar{C}$        |                |  | NC    | NC    | NC    | NC   | NC  | NC | NC | NC |
|                 | TN     | Test N                    |                |  | NC    | NC    | NC    | NC   | NC  | NC | NC | NC |
|                 | TL     | Test LINK                 |                |  | NC    | NC    | NC    | NC   | NC  | NC | NC | NC |
|                 | TF1    | Test Flag1                |                |  | NC    | NC    | NC    | NC   | NC  | NC | NC | NC |
|                 | TF2    | Test Flag2                |                |  | NC    | NC    | NC    | NC   | NC  | NC | NC | NC |
|                 | TF3    | Test Flag3                |                |  | NC    | NC    | NC    | NC   | NC  | NC | NC | NC |

U = Update  
 NC = No Change  
 0 = Reset  
 1 = Set  
 i = 0 to 15 when not specified

\*In byte mode only the lower byte from the Y bus is loaded into the RAM or ACC and in word mode all 16-bits from the Y bus are loaded into the RAM or ACC.

\*\*Y-Bus is Undefined.

**No-Op Instruction**

The No-Op Instruction does not affect any internal registers; the Status Register, RAM register and AC register are left unchanged. The 16-bit opcode is fixed.

**No Operation Field Definition**

|       |       |       |      |      |       |
|-------|-------|-------|------|------|-------|
|       | 15 14 | 13 12 | 9 8  | 5 4  | 0     |
| No-Op | 0     | 11    | 1000 | 1010 | 00000 |

**No-Op Instruction**

| Instruction | B/W | Quad |      |      |      |
|-------------|-----|------|------|------|------|
| No-Op       | 0   | 11   | 1000 | 1010 | 0000 |

**Y Bus and Status**

| Instruction | Opcode | B/W   | Y-Bus | Flag3 | Flag2 | Flag1 | LINK | OVR | N  | C  | Z  |
|-------------|--------|-------|-------|-------|-------|-------|------|-----|----|----|----|
| No-Op       |        | 0 = B | *     | NC    | NC    | NC    | NC   | NC  | NC | NC | NC |

\*Y-Bus is undefined.  
 SRC = Source  
 U = Update  
 NC = No Change

0 = Reset  
 1 = Set  
 i = 0 to 15 when not specified

**Electrical Characteristics** Over Commercial and Military Operating Range  $V_{CC}$  Min. = 4.5V,  $V_{CC}$  Max. = 5.5V

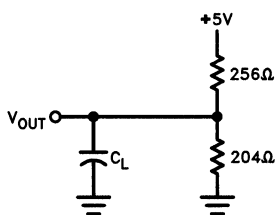
| Parameters                           | Description                                 | Test Conditions   | Min.  | Max.     | Units         |    |
|--------------------------------------|---|---|---|----------|---------------|----|
| $V_{OH}$                             | Output HIGH Voltage                         | $V_{CC} = \text{Min.}$<br>$I_{OH} = -1.6 \text{ mA}$            | 2.4   |          | V             |    |
| $V_{OL}$                             | Output LOW Voltage                          | $V_{CC} = \text{Min.}$<br>$I_{OL} = 16 \text{ mA}$              |   | 0.4      | V             |    |
| $V_{IH}$                             | Input HIGH Voltage                          |   | 2.0   | $V_{CC}$ | V             |    |
| $V_{IL}$                             | Input LOW Voltage                           |   |   | 0.8      | V             |    |
| $I_{IX}$                             | Input Leakage Current                       | $V_{SS} \leq V_{IN} \leq V_{CC}$<br>$V_{CC} = \text{Max.}$      | -10   | +10      | $\mu\text{A}$ |    |
| $I_{OZ}$                             | Output Leakage Current                      | $V_{CC} = \text{Max.}$<br>$V_{OUT} = V_{SS} \text{ to } V_{CC}$ |   | +10      | $\mu\text{A}$ |    |
|                                      |   |   | -10   |          | $\mu\text{A}$ |    |
| $I_{SC}$                             | Output Short Circuit Current <sup>[1]</sup> | $V_{CC} = \text{Max.}$<br>$V_{OUT} = 0\text{V}$                 |   | -85      | mA            |    |
| $I_{CC}(Q1)$ <sup>[2]</sup>          | Supply Current (Quiescent)                  | Commercial  | $V_{SS} \leq V_{IN} \leq V_{IL}$ or<br>$V_{IH} \leq V_{IN} \leq V_{CC}$ ; $\overline{OE}_Y = \text{HIGH}$ |          | 126           | mA |
|                                      |   | Military  |   |          | 145           |    |
| $I_{CC}(Q2)$                         | Supply Current (Static)                     | Commercial  | $V_{IN} = V_{CC}$ or GND<br>$V_{CC} = \text{Max.}$<br>$I_{OPER} = 0 \mu\text{A}$                          |          | 68            | mA |
|                                      |   | Military  |   |          | 78            |    |
| $I_{CC}(\text{Max.})$ <sup>[2]</sup> | Supply Current                              | Commercial  | $V_{CC} = \text{Max.}$ , $f_{CLK} = 10 \text{ MHz}$<br>$\overline{OE}_Y = \text{HIGH}$                    |          | 145           | mA |
|                                      |   | Military  |   |          | 166           |    |

**5**
**Capacitance<sup>[3]</sup>**

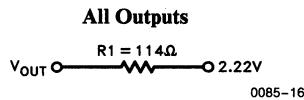
| Parameters | Description        | Test Conditions  | Max. | Units |
|------------|--------------------|--|------|-------|
| $C_{IN}$   | Input Capacitance  | $T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$<br>$V_{CC} = 5.0\text{V}$ | 5    | pF    |
| $C_{OUT}$  | Output Capacitance |  | 7    |       |

**Notes:**

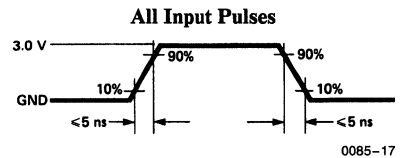
- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
- To calculate  $I_{CC}$  at any given frequency, use  $I_{CC}(Q1) + I_{CC}(A.C.)$  where  $I_{CC}(Q1)$  is shown above and  $I_{CC}(A.C.) = 1.9 \text{ mA/MHz} \times \text{Clock Frequency}$  for the Commercial temperature range.  $I_{CC}(A.C.) = 2.1 \text{ mA/MHz} \times \text{Clock Frequency}$  for Military temperature range.
- Tested on a sample basis.

**Output Loads Used for AC Performance Characteristics**


0085-15



0085-16



0085-17

**Notes:**

- $C_L = 50 \text{ pF}$  includes scope probe, wiring and stray capacitance.
- $C_L = 5 \text{ pF}$  for output disable tests.

### Commercial Switching Characteristics

#### Guaranteed Commercial Range A.C. Performance Characteristics

( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 4.5\text{V}$  to  $5.5\text{V}$ ,  $C_L = 50\text{ pF}$ )

#### Combinational Propagation Delays (ns)

| To Output From Input        | Y <sub>0-15</sub> |    |    | T <sub>1-4</sub> |    |    | CT |    |    |
|-----------------------------|-------------------|----|----|------------------|----|----|----|----|----|
| CY7C9116<br>CY7C9117        | 35                | 45 | 65 | 35               | 45 | 65 | 35 | 45 | 65 |
| I <sub>0-4</sub><br>(ADDR)  | 35                | 45 | 65 | 35               | 52 | 73 |    |    |    |
| I <sub>0-15</sub><br>(DATA) | 35                | 45 | 65 | 35               | 52 | 73 |    |    |    |
| I <sub>0-15</sub><br>(INST) | 35                | 45 | 65 | 35               | 52 | 73 | 20 | 29 | 30 |
| DLE*                        | 20                | 32 | 55 | 30               | 32 | 55 |    |    |    |
| T <sub>1-4</sub>            |                   |    |    |                  |    |    | 15 | 25 | 27 |
| CP                          | 30                | 32 | 60 | 30               | 32 | 66 | 25 | 25 | 37 |
| Y <sub>0-15</sub>           | 20                | 32 | 53 | 30               | 32 | 53 |    |    |    |
| IEN                         |                   |    |    |                  |    |    | 15 | 25 | 25 |

\*DLE is guaranteed by other tests.

#### Enable/Disable Times (ns) ( $C_L = 5\text{ pF}$ , Disable Only)

| From Input               | To Output                       | Enable |    |    |      |    |    | Disable |    |    |      |    |    |
|--------------------------|---------------------------------|--------|----|----|------|----|----|---------|----|----|------|----|----|
|                          |                                 | TPZH   |    |    | TPZL |    |    | TPHZ    |    |    | TPLZ |    |    |
|                          |                                 | 35     | 45 | 65 | 35   | 45 | 65 | 35      | 45 | 65 | 35   | 45 | 65 |
| $\overline{\text{OE}}_Y$ | Y <sub>0</sub> -Y <sub>15</sub> | 18     | 20 | 22 | 18   | 20 | 22 | 18      | 20 | 22 | 18   | 20 | 22 |
| OE <sub>T</sub>          | T <sub>1</sub> -T <sub>4</sub>  | 15     | 20 | 22 | 15   | 20 | 22 | 15      | 20 | 22 | 15   | 20 | 22 |

#### Clock and Pulse Requirements (ns)

| Input | Minimum Low Time |    |    | Minimum High Time |    |    |
|-------|------------------|----|----|-------------------|----|----|
|       | 35               | 45 | 65 | 35                | 45 | 65 |
| CP    | 15               | 15 | 20 | 15                | 15 | 15 |
| DLE   |                  |    |    | 15                | 15 | 15 |
| IEN   | 15               | 15 | 20 |                   |    |    |

**Set-up and Hold Times (ns)**

| [5]                          | Input                                      | With Respect To | High to Low Transition |                   |                   |                   |                  |                   | Low to High Transition |           |           |           |           |           | Comments               |
|------------------------------|--|-----------------|------------------------|-------------------|-------------------|-------------------|------------------|-------------------|------------------------|-----------|-----------|-----------|-----------|-----------|------------------------|
|                              |  |                 | Set-up                 |                   |                   | Hold              |                  |                   | Set-up                 |           |           | Hold      |           |           |                        |
|                              |  |                 | 35                     | 45                | 65                | 35                | 45               | 65                | 35                     | 45        | 65        | 35        | 45        | 65        |                        |
| <b>CY7C9116 and CY7C9117</b> |  |                 | <b>35</b>              | <b>45</b>         | <b>65</b>         | <b>35</b>         | <b>45</b>        | <b>65</b>         | <b>35</b>              | <b>45</b> | <b>65</b> | <b>35</b> | <b>45</b> | <b>65</b> |                        |
| 1                            | I <sub>0-4</sub> (RAM Addr)                | CP              | 12                     | 13                | 13                | 0                 | 0                | 0                 |                        |           |           |           |           |           | Single Addr (Source)   |
| 2                            | I <sub>0-4</sub> (RAM Addr)                | CP & IEN        | 5                      | 5                 | 5                 | ← Do Not Change → |                  |                   |                        |           |           | 0         | 2         | 0         | Two Addr (Destination) |
| 3                            | I <sub>0-15</sub> (Data)                   | CP              |                        |                   |                   |                   |                  |                   | 40                     | 43        | 60        | 0         | 0         | 0         |                        |
| 4                            | I <sub>0-4</sub> (RAM Addr) <sup>[2]</sup> | IEN             | 15 <sup>[1]</sup>      | 18 <sup>[1]</sup> | 24 <sup>[1]</sup> | 4 <sup>[1]</sup>  | 5 <sup>[1]</sup> | 10 <sup>[1]</sup> |                        |           |           |           |           |           | Two Addr (Immediate)   |
| 5                            | I <sub>0-15</sub> (Instr) <sup>[3]</sup>   | CP              | 15 <sup>[1]</sup>      | 18 <sup>[1]</sup> | 24 <sup>[1]</sup> | 4 <sup>[1]</sup>  | 5 <sup>[1]</sup> | 10 <sup>[1]</sup> | 40                     | 43        | 60        | 0         | 0         | 0         |                        |
| 6                            | IEN <sup>[2]</sup>                         | CP              |                        |                   |                   |                   |                  |                   |                        |           |           | 8         | 8         | 8         | Two Addr (Immediate)   |
| 7                            | IEN HIGH                                   | CP              | 5                      | 5                 | 5                 |                   |                  |                   |                        |           |           | 0         | 1         | 2         | Disable                |
| 8                            | IEN LOW                                    | CP              |                        |                   |                   |                   |                  |                   | 10                     | 10        | 10        | 0         | 1         | 1         | Enable                 |
| 9                            | IEN LOW                                    | CP              | 5                      | 5                 | 5                 | 1                 | 1                | 0                 |                        |           |           |           |           |           | Note 1                 |
| 10                           | SRE  | CP              |                        |                   |                   |                   |                  |                   | 12                     | 12        | 12        | 0         | 2         | 0         |                        |
| 11                           | Y <sup>[4]</sup>                           | CP              |                        |                   |                   |                   |                  |                   | 32                     | 32        | 42        | 0         | 0         | 0         |                        |
| 12                           | Y <sup>[4]</sup>                           | DLE             | 6                      | 6                 | 6                 | 5                 | 5                | 5                 |                        |           |           |           |           |           |                        |
| 13                           | DLE  | CP              |                        |                   |                   |                   |                  |                   | 20                     | 25        | 43        | 0         | 0         | 0         |                        |

**Notes:**

- Timing for immediate instruction for first cycle.
- CY7C9117 only.
- CY7C9115 and CY7C9116 only.
- Y = D for CY7C9117.
- tsx and tHK referenced on the waveforms are looked up on this table by x = line number on the left. Ex: ts1 = 13 ns for -53 ns devices.

**Military Switching Characteristics**
**Guaranteed Military Range A.C. Performance Characteristics**

 (T<sub>A</sub> = -55°C to +125°C, V<sub>CC</sub> = 4.5V to 5.5V, C<sub>L</sub> = 50 pF)

**Combinational Propagation Delays (ns)**

| To Output From Input               | Y <sub>0-15</sub> |           |           | T <sub>1-4</sub> |           |           | CT        |           |           |
|------------------------------------|-------------------|-----------|-----------|------------------|-----------|-----------|-----------|-----------|-----------|
| <b>CY7C9116</b><br><b>CY7C9117</b> | <b>40</b>         | <b>65</b> | <b>79</b> | <b>40</b>        | <b>65</b> | <b>79</b> | <b>40</b> | <b>65</b> | <b>79</b> |
| I <sub>0-4</sub> (ADDR)            | 40                | 65        | 79        | 40               | 65        | 79        |           |           |           |
| I <sub>0-15</sub> (DATA)           | 40                | 65        | 79        | 40               | 65        | 79        |           |           |           |
| I <sub>0-15</sub> (INST)           | 40                | 65        | 79        | 40               | 65        | 79        | 22        | 26        | 29        |
| DLE*                               | 20                | 52        | 62        | 30               | 52        | 62        |           |           |           |
| T <sub>1-4</sub>                   |                   |           |           |                  |           |           | 15        | 26        | 29        |
| CP                                 | 30                | 57        | 67        | 35               | 65        | 75        | 33        | 33        | 39        |
| Y <sub>0-15</sub>                  | 20                | 52        | 60        | 30               | 52        | 60        |           |           |           |
| IEN                                |                   |           |           |                  |           |           | 20        | 26        | 29        |

\*DLE is guaranteed by other tests.

**5**

**Military Switching Characteristics (Continued)**

**Enable/Disable Times (ns)** ( $C_L = 5$  pF, Disable Only)

| From Input        | To Output    | Enable |    |    |      |    |    | Disable |    |    |      |    |    |
|-------------------|--------------|--------|----|----|------|----|----|---------|----|----|------|----|----|
|                   |              | TPZH   |    |    | TPZL |    |    | TPHZ    |    |    | TPLZ |    |    |
|                   |              | 40     | 65 | 79 | 40   | 65 | 79 | 40      | 65 | 79 | 40   | 65 | 79 |
| $\overline{OE}_Y$ | $Y_0-Y_{15}$ | 18     | 22 | 25 | 18   | 22 | 25 | 18      | 18 | 25 | 18   | 18 | 25 |
| $OE_T$            | $T_1-T_4$    | 18     | 18 | 20 | 18   | 18 | 20 | 15      | 15 | 20 | 15   | 15 | 20 |

**Clock and Pulse Requirements (ns)**

| Input            | Minimum Low Time |    |    | Minimum High Time |    |    |
|------------------|------------------|----|----|-------------------|----|----|
|                  | 40               | 65 | 79 | 40                | 65 | 79 |
| CP               | 15               | 20 | 25 | 15                | 15 | 15 |
| DLE              |                  |    |    | 15                | 15 | 15 |
| $\overline{IEN}$ | 15               | 15 | 15 |                   |    |    |

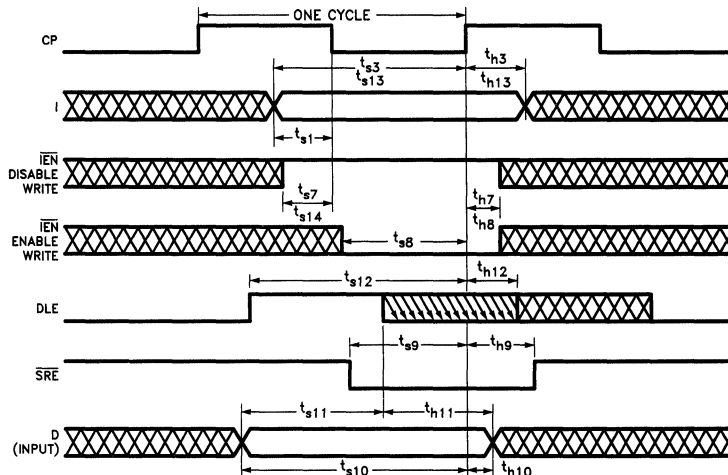
**Set-up and Hold Times (ns)**

| [5]                          | Input                   | With Respect To       | High to Low Transition |    |       |                   |    |       | Low to High Transition |    |    |      |    |    | Comments               |
|------------------------------|-------------------------|-----------------------|------------------------|----|-------|-------------------|----|-------|------------------------|----|----|------|----|----|------------------------|
|                              |                         |                       | Set-up                 |    |       | Hold              |    |       | Set-up                 |    |    | Hold |    |    |                        |
|                              |                         |                       | 40                     | 65 | 79    | 40                | 65 | 79    | 40                     | 65 | 79 | 40   | 65 | 79 |                        |
| <b>CY7C9116 and CY7C9117</b> |                         |                       | 40                     | 65 | 79    | 40                | 65 | 79    | 40                     | 65 | 79 | 40   | 65 | 79 |                        |
| 1                            | $I_{0-4}$ (RAM Addr)    | CP                    | 12                     | 12 | 12    | 0                 | 1  | 1     |                        |    |    |      |    |    | Single Addr (Source)   |
| 2                            | $I_{0-4}$ (RAM Addr)    | CP & $\overline{IEN}$ | 5                      | 7  | 7     | ← Do Not Change → |    |       |                        |    |    | 0    | 0  | 0  | Two Addr (Destination) |
| 3                            | $I_{0-15}$ (Data)       | CP                    |                        |    |       |                   |    |       | 43                     | 56 | 65 | 0    | 0  | 0  |                        |
| 4                            | $I_{0-4}$ (RAM Addr)[2] | $\overline{IEN}$      | 15[1]                  | 25 | 27[1] | 5[1]              | 12 | 12[1] |                        |    |    |      |    |    | Two Addr (Immediate)   |
| 5                            | $I_{0-15}$ (Instr)[3]   | CP                    | 15[1]                  | 25 | 27[1] | 5[1]              | 12 | 12[1] | 45                     | 56 | 65 | 0    | 2  | 2  |                        |
| 6                            | $\overline{IEN}$ [2]    | CP                    |                        |    |       |                   |    |       |                        |    |    | 8    | 8  | 8  | Two Addr (Immediate)   |
| 7                            | $\overline{IEN}$ HIGH   | CP                    | 5                      | 5  | 5     |                   |    |       |                        |    |    | 0    | 2  | 2  | Disable                |
| 8                            | $\overline{IEN}$ LOW    | CP                    |                        |    |       |                   |    |       | 10                     | 10 | 12 | 0    | 3  | 3  | Enable                 |
| 9                            | $\overline{IEN}$ LOW    | CP                    | 7                      | 7  | 7     | 0                 | 3  | 3     |                        |    |    |      |    |    | Note 1                 |
| 10                           | SRE                     | CP                    |                        |    |       |                   |    |       | 10                     | 10 | 12 | 0    | 1  | 1  |                        |
| 11                           | Y[4]                    | CP                    |                        |    |       |                   |    |       | 39                     | 45 | 53 | 0    | 0  | 0  |                        |
| 12                           | Y[4]                    | DLE                   | 7                      | 7  | 7     | 3                 | 3  | 3     |                        |    |    |      |    |    |                        |
| 13                           | DLE                     | CP                    |                        |    |       |                   |    |       | 20                     | 46 | 54 | 0    | 0  | 0  |                        |

- Notes:
- Timing for immediate instruction for first cycle.
  - CY7C9117 only.
  - CY7C9115 and CY7C9116 only.
  - Y = D for CY7C9117.
  - $t_{SX}$  and  $t_{HX}$  referenced on the waveforms are looked up on this table by x = line number on the left. Ex:  $t_{S1} = 24$  ns for - 79 ns devices.

## Switching Waveforms

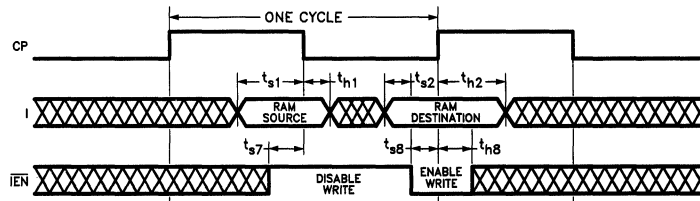
### Single Address Access Timing



If  $t_{h11}$  is satisfied,  $t_{h10}$  need not be satisfied

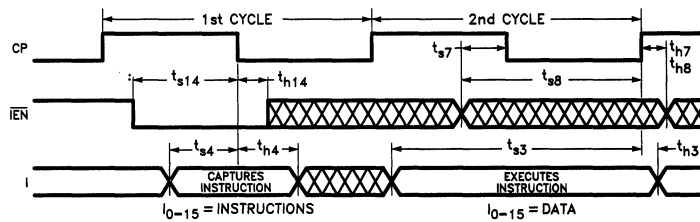
0085-18

### Double Address Access Timing



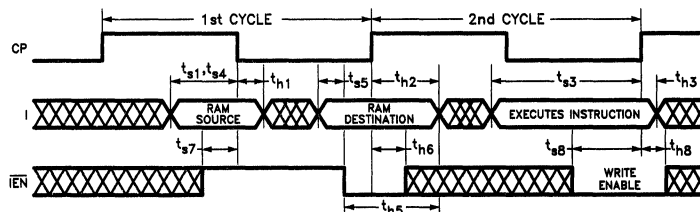
0085-19

### One-Address Immediate Instruction Cycle Timing



0085-20

### Two-Address Immediate Instruction Timing (7C9117 Only)



0085-21



### Set-up and Hold Times (Cross Ref. Table)

| [1] | High to Low Transition |      | Low to High Transition |      |
|-----|------------------------|------|------------------------|------|
|     | Set-up                 | Hold | Set-up                 | Hold |
| 1   | ts1                    | th1  |                        |      |
| 2   | ts2                    |      |                        | th2  |
| 3   |                        |      | ts3                    | th3  |
| 4   | ts5                    | th5  |                        |      |
| 5   | ts4                    | th4  | ts13                   | th13 |
| 6   |                        |      |                        | th6  |
| 7   | ts7                    |      |                        | th7  |
| 8   |                        |      | ts8                    | th8  |
| 9   | ts14                   | th14 |                        |      |
| 10  |                        |      | ts9                    | th9  |
| 11  |                        |      | ts10                   | th10 |
| 12  | ts11                   | th11 |                        |      |
| 13  |                        |      | ts12                   | th12 |

Note:

1. Refer to Set-up and Hold times shown on pages 22 & 23.

### Ordering Information

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|--------------|-----------------|
| 35         | CY7C9115-35JC | J69          | Commercial      |
| 45         | CY7C9115-45JC | J69          |                 |
| 65         | CY7C9115-65JC | J69          |                 |

| Speed (ns) | Ordering Code  | Package Type | Operating Range |
|------------|----------------|--------------|-----------------|
| 35         | CY7C9116-35LC  | L69          | Commercial      |
|            | CY7C9116-35JC  | J81          |                 |
|            | CY7C9116-35DC  | D28          |                 |
| 45         | CY7C9116-45LC  | L69          |                 |
|            | CY7C9116-45JC  | J81          |                 |
|            | CY7C9116-45DC  | D28          |                 |
| 65         | CY7C9116-65LC  | L69          |                 |
|            | CY7C9116-65JC  | J81          |                 |
|            | CY7C9116-65DC  | D28          |                 |
| 40         | CY7C9116-40LC  | L69          | Military        |
|            | CY7C9116-40JC  | J81          |                 |
|            | CY7C9116-40DC  | D28          |                 |
| 65         | CY7C9116-65LMB | L69          |                 |
|            | CY7C9116-65DMB | D28          |                 |
| 79         | CY7C9116-79LMB | L69          |                 |
|            | CY7C9116-79DMB | D28          |                 |

| Speed (ns) | Ordering Code  | Package Type | Operating Range |
|------------|----------------|--------------|-----------------|
| 35         | CY7C9117-35GC  | G68          | Commercial      |
|            | CY7C9117-35JC  | J81          |                 |
|            | CY7C9117-35LC  | L81          |                 |
| 45         | CY7C9117-45GC  | G68          |                 |
|            | CY7C9117-45JC  | J81          |                 |
|            | CY7C9117-45LC  | L81          |                 |
| 65         | CY7C9117-65GC  | G68          |                 |
|            | CY7C9117-65JC  | J81          |                 |
|            | CY7C9117-65LC  | L81          |                 |
| 40         | CY7C9117-40GC  | G68          | Military        |
|            | CY7C9117-40JC  | J81          |                 |
|            | CY7C9117-40LC  | L81          |                 |
| 65         | CY7C9117-65GMB | G68          |                 |
|            | CY7C9117-65LMB | L81          |                 |
| 79         | CY7C9117-79GMB | G68          |                 |
|            | CY7C9117-79LMB | L81          |                 |

**Military Specifications**  
**Group A Subgroup Testing**

**DC Characteristics**

| Parameters           | Subgroups |
|----------------------|-----------|
| V <sub>OH</sub>      | 1,2,3     |
| V <sub>OL</sub>      | 1,2,3     |
| V <sub>IH</sub>      | 1,2,3     |
| V <sub>IL Max.</sub> | 1,2,3     |
| I <sub>IX</sub>      | 1,2,3     |
| I <sub>OZ</sub>      | 1,2,3     |
| I <sub>SC</sub>      | 1,2,3     |
| I <sub>CC(Q1)</sub>  | 1,2,3     |
| I <sub>CC(Max)</sub> | 1,2,3     |

5

**Switching Characteristics**

| Parameters                | Subgroups   |
|---------------------------|-------------|
| I <sub>0-4</sub> (Addr)   | 7,8,9,10,11 |
| I <sub>0-15</sub> (Data)  | 7,8,9,10,11 |
| I <sub>0-15</sub> (Instr) | 7,8,9,10,11 |
| DLE                       | 7,8,9,10,11 |
| t <sub>1-4</sub>          | 7,8,9,10,11 |
| CP                        | 7,8,9,10,11 |
| Y <sub>0-15</sub>         | 7,8,9,10,11 |
| IEN                       | 7,8,9,10,11 |
| OE <sub>Y</sub>           | 7,8,9,10,11 |
| OE <sub>T</sub>           | 7,8,9,10,11 |
| CP                        | 7,8,9,10,11 |

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# Introduction to RISC

## Introduction

This section provides an overview of the basic concepts and advantages of RISC computer architectures in general and a brief summary of the specific features of the RISC computer implemented in Cypress' CY7C600 family.

## Scalable Processor Architecture

The Cypress CY7C600 family implements a RISC architecture called SPARC™. SPARC stands for Scalable Processor ARCHitecture. It is applicable to large high performance as well as small machines. The term "scalable" refers to the size of the smallest lines on a chip. As lines become smaller, chips get faster. However, some chip designs do not shrink well (they do not scale properly) because the architecture is too complicated. Because of its simplicity, the CY7C600 scales well. Consequently, CY7C600 systems will become faster as better semiconductor techniques are perfected. SPARC is an open computer architecture. We believe that the intelligent and aggressive nature of the SPARC design will make it an industry standard. The design specification is published, and other vendors are also producing SPARC microprocessors.

## What is RISC?

RISC, an acronym for Reduced Instruction Set Computer, is a style of computer architecture emphasizing simplicity and efficiency. RISC designs begin with a necessary and sufficient instruction set. Typically, a few simple operations account for almost all computations. RISC machines are about two to five times faster than machines with traditional complex instruction set architectures. Also, RISC machine's simpler designs are easier to implement, resulting in shorter design cycles.

RISC architectures are a response to the evolution from assembly language to high-level languages. Assembly language programs occasionally employ elaborate machine instructions, whereas high-level language compilers rarely do. For example, most C compilers use only about 30% of the available instructions on CISC machines. Studies show that approximately 80% of a typical program's computations require only about 20% of a processor's instruction set.

RISC is to hardware what the UNIX® operating system is to software. The UNIX system proves that operating systems can be both simple and useful. Hardware studies suggest the same conclusion. As advances in semiconductor technology reduce the cost of processing and memory, overly complex instruction sets become a performance liability. The designers of RISC machines strive for hardware simplicity, with close cooperation between machine architecture and compiler design. At each step, computer architects must ask: to what extent does a feature improve or degrade performance and is it worth the cost of implementation? Each additional feature, no matter how useful it is in an isolated instance, makes all others perform more slowly by its mere presence.

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The goal of RISC architecture is to maximize the effective speed of a design by performing infrequent functions in software, including hardware-only features that yield a net performance gain. Performance gains are measured by conducting detailed studies of large high-level language programs. RISC improves performance by providing the building blocks from which high-level functions can be synthesized without the overhead of general but complex instructions.

The following characteristics are typical of RISC architectures, including the CY7C600 design:

## RISC Architecture

The following characteristics are typical of RISC architectures, including the CY7C600 design:

**Single-cycle execution.** Most instructions are executed in a single machine cycle.

**Hardwired control** with no microcode. Microcode adds a level of complexity and raises the number of cycles per instruction.

**Load/Store, register-to-register design.** All computational instructions involve registers. Memory accesses are made with only load and store instructions.

**Simple fixed-format instructions** with few addressing modes. All instructions are one word long (typically 32 bits) and have few addressing modes.

**Pipelining.** The instruction set design allows for the processing of several instructions at the same time.

**High-performance memory.** RISC machines have at least 32 general-purpose registers (the 7C600 has 136) and large cache memories.

**Migration of functions to software.** Only those features that measurably improve performance are implemented in hardware. Programs contain sequences of simple instructions.



tions for executing complex functions rather than the complex instructions themselves.

**Simple, efficient instruction pipeline visible to compilers.** For example, branches take effect after execution of the following instruction, permitting a fetch of the next instruction during execution of the current instruction.

The real keys to enhanced performance are single-cycle execution and keeping the cycle time as short as possible. Many characteristics of RISC architectures, such as load/store and register-to-register design, facilitate single-cycle execution. Simple fixed-format instructions, on the other hand, permit shorter cycles by reducing decoding time.

Note that some of these features, particularly pipelining and high-performance memories, have been used in supercomputer designs for many years. The difference is that in RISC architectures these ideas are integrated into a processor with a simple instruction set and no microcode.

Moving functionality from run time to compile time also enhances performance. Functions calculated at compile time do not require further calculating each time the program runs. Furthermore, optimizing compilers can rearrange pipelined instruction sequences and arrange register-to-register operations to reuse computational results.

A new set of simplified design criteria has emerged:

Instructions should be simple unless there is a good reason for complexity. To be worthwhile, a new instruction that increases cycle time by 10% must reduce the total number of cycles executed by at least 10%.

Microcode is generally no faster than sequences of hardwired instructions. Moving software into microcode does not make it better, it just makes it harder to modify.

Fixed-format instructions and pipelined execution are more important than program size. As memory gets cheaper and faster, the space/time tradeoff resolves in favor of time. Reducing space no longer decreases time.

Compiler technology should use simple instructions to generate more complex instructions. Instead of substituting a complicated microcoded instruction for several simple instructions, which compilers did in the 1970s, optimizing compilers can form sequences of simple, fast instructions out of complex high-level code. Operands can be kept in registers to increase speed even further.

## RISC's Speed Advantage

Using any given benchmark, the performance  $P$  of a particular computer is inversely proportional to the product of the benchmark's instruction count ( $I$ ), the average number of clock cycles per instruction ( $C$ ), and the inverse of the clock speed ( $S$ ). Assuming that a RISC machine runs at the same clock speed as a corresponding traditional machine;  $S$  is identical. The number of clock cycles per instruction ( $C$ ), is around 1.3 to 1.7 for RISC machines, and between 4 and 10 for traditional machines. This makes the instruction execution rate of RISC machines about 3 to 6 times faster than traditional machines. But, because traditional machines have more powerful instructions, RISC machines must execute more instructions for the same program, typically about 10% to 30% more. Since RISC machines execute 10% to 30% more instructions 3 to 6 times more quickly, they are about 2 to 5 times faster than traditional machines for executing typical large programs.

$$P = \frac{1}{I \times C \times \frac{1}{S}}$$

Compiled programs on RISC machines are somewhat larger than compiled programs on traditional machines, because several simple instructions replace one complex instruction resulting in decreased code density. All SPARC instructions are 32 bits wide, whereas some instructions on traditional machines are narrower. But the number of instructions actually executed may not be as great as the increased program size would indicate. A windowed register file, for example, often simplifies call/return sequences so that context switches become less expensive.

## CY7C600 Architecture

The SPARC CPU is composed of a CY7C601 Integer Unit (IU) that performs basic processing and a CY7C608 Floating-Point Controller (FPC) interface to the CY7C609 Floating-Point Processor that performs floating-point calculations. The CY7C608/CY7C609 combination acts as a SPARC compatible Floating-Point Unit (FPU). CY7C600-based computers typically have a memory management unit (MMU), a large virtual-address cache for instructions and data, and are organized around a 32-bit data and instruction bus.

The integer and floating-point units operate concurrently. The FPU performs floating-point calculations with a set number of floating-point arithmetic units. The CY7C600 architecture also specifies an interface for the connection of an additional coprocessor.

## Instruction Categories

The CY7C600 architecture has about 50 integer instructions. CY7C600 instructions fall into seven basic categories:

**Load and store instructions** (the only way to access memory). These instructions use two registers or a register and a constant to calculate the memory address involved. Half-word accesses must be aligned on 2-byte boundaries, word accesses on 4-byte boundaries, and double-word accesses on 8-byte boundaries. These alignment restrictions greatly speed up memory access.

**Arithmetic/logical/shift instructions.** These instructions compute a result that is a function of two source operands and then place the result in a register. They perform arithmetic, logical, or shift operations.

**Floating-point and coprocessor instructions.** These include floating-point calculations, operations on floating-point registers, and instructions involving the optional coprocessor. Floating-point operations execute concurrently with IU instructions and with other floating-point operations when necessary. This concurrency is transparent to the programmer.

**Control-transfer instructions.** These include jumps, calls, traps, and branches. Control transfers are usually delayed until after execution of the next instruction, so that the pipeline is not emptied every time a control transfer occurs. Thus, compilers can be optimized for delayed branching.

**Read/write control register instructions.** These include instructions to read and write the contents of various control registers. Generally the source or destination is implied by the instruction.

**Artificial intelligence instructions.** These include the tagged arithmetic instructions Tagged Add and Tagged Subtract. Tagged instructions are useful for implementing artificial intelligence languages such as LISP, because tags can automatically indicate to software interpreters the data type of arithmetic operands.

**Multiprocessing instructions.** These include two instructions for implementing semaphores in memory: Atomic Load/Store Unsigned Byte which loads a byte from memory then sets the location to all "1's" and SWAP which exchanges the contents of a register and a memory location. Both of these instructions are "atomic" or uninteruptable.

## Register Windows

A unique feature contributing to the high performance of the CY7C600 design is its overlapping register windows. Results left in registers by a calling routine automatically become available operands for the called routine, reducing the need for load and store instructions to main memory.

According to the architectural specification, there may be anywhere between 2 and 32 register windows, each window having 24 working registers, plus 8 global registers. The first implementation has 8 register windows with 24 registers each (but count only 16 since 8 overlap), plus 8 global registers, for a total of 136 registers. Recent research suggests that register windows and tagged arithmetic, found in CY7C600 systems, but not in other commercial RISC machines, are sufficient to provide excellent performance for expert system development requiring AI languages such as Lisp and Smalltalk.

## Traps and Interrupts

The CY7C600 design supports a full set of traps and interrupts. They are handled by a table that supports 128 hardware and 128 software traps. Even though floating-point instructions can execute concurrently with integer instructions, floating-point traps are precise because the FPU supplies (from the table) the address of the instruction that failed.

## Protection

Some CY7C600 instructions are privileged and can only be executed while the processor is in supervisor mode. This instruction execution protection ensures that user programs cannot accidentally alter the state of the machine with respect to its peripherals.

The CY7C600 design also provides memory protection, which is essential for smooth multitasking operation. Memory protection makes it impossible for user programs to corrupt the system, other user programs, or themselves.

## An Open Architecture

### Advantages of Open Architecture

The CY7C600 design is the first open RISC architecture, and one of the few open CPU architectures. Standard products are more beneficial than proprietary ones, because

standards allow users to acquire the most cost-effective hardware and software in a competitive multi-vendor marketplace. Integrated circuits come from several competing semiconductor vendors, while software is supplied by systems vendors. This advantage is lost when users are limited by a processor with proprietary hardware and software.

RISC architectures, and the CY7C600 design in particular, are easy to implement because they are relatively simple. Since they have short design cycles, RISC machines can absorb new technologies almost immediately, unlike more complicated computer architectures.

CY7C600 systems were designed to support:

- The C programming language and the UNIX operating system,

- Numerical applications (using FORTRAN), and

- Artificial intelligence and expert system applications using Lisp and Prolog.

Supporting C is relatively easy; most modern hardware architectures are able to do so. The one essential feature is byte addressability. However, numerical applications require fast floating-point operations and artificial intelligence applications require large address spaces and interchangeability of data types.

The floating-point processor, with pipelined floating-point operation capabilities, achieves the high performance needed for numerical applications.

For artificial intelligence and expert system applications, CY7C600 systems offer tagged instructions and word alignment. Because languages such as Lisp and Prolog are often interpreted, word alignment makes it easier for interpreters to manipulate and interchange integers and different types of pointers. In the tagged instructions, the two low-order bits of an operand specify the type of operand. If an operand is an integer, most of the time it is added to (or subtracted from) a register. If an operand is a pointer, most of the time a memory reference is involved. Language interpreters can leave operands in the appropriate registers, greatly improving the performance of exploratory programming environments.

The CY7C600 architecture does not dictate a memory management unit (MMU), although a high performance unit has been specified for the SPARC architecture. The same processor will be used in different types of machines. For example, a single-user machine with embedded applications does not need an MMU. By contrast, a multitasking machine used for timesharing, such as a traditional UNIX workstation, needs a paging MMU. Furthermore, a multiprocessor such as a vector machine or hypercube requires specialized memory management facilities. The CY7C600 architecture can be implemented with a different MMU configuration for each of these purposes, without affecting user software.

## CY7C600 Machines and Other RISC Machines

The CY7C600 design has more similarities to Berkeley's RISC-II architecture than to any other RISC architecture. Like the RISC-II architecture, it uses register windows in order to reduce the number of load/store instructions. The CY7C600 architecture allows 32 register windows, but the

initial implementation has 8 windows. The tagged instructions are derived from SOAR, the "Smalltalk On A RISC" processor developed at Berkeley after implementing RISC-II.

CY7C600 systems are designed for optimal floating-point performance, and support single-, double-, and extended-precision operands and operations, as specified by the ANSI/IEEE 754 floating-point standard. High floating-point performance results from concurrency of the IU and FPU. The integer unit loads and stores floating-point operands, while the floating-point unit performs calculations. If an error (such as a floating-point exception) occurs, the floating-point unit specifies precisely where the trap took place; execution is expediently resumed at the discretion of the integer unit. Furthermore, the floating-point unit has an internal instruction queue; it can operate while the integer unit is processing unrelated functions.

CY7C600 systems deliver very high levels of performance. The flexibility of the architecture makes future systems capable of delivering performance many times greater than the performance of the initial implementation. Moreover, the openness of the architecture makes it possible to absorb technological advances almost as soon as they occur.

## CY7C600 Product Family

Since the CY7C600 has been designed to offer a complete solution for the implementation of high performance computers and controllers, the family consists of several members including an Integer Unit, a Floating-Point Controller, a Floating-Point Processor, a Cache Controller and Memory Management Unit, and a Cache Data RAM.

The SPARC processor family consists of a CY7C601 Integer Unit (IU) to perform all non-floating-point operations and a CY7C608 Floating-Point Controller (FPC) which interfaces to a CY7C609 Floating-Point Processor to perform floating-point arithmetic concurrent with the IU. Support is also provided for a second generic coprocessor interface. The IU communicates with external memory via a 32-bit address bus and a 32-bit data/instruction bus. In typical data processing applications, the IU and FPU are combined with a high performance CY7C604 Cache Controller and Memory Management Unit and a cache memory implemented with CY7C157 Cache RAMs. In many dedicated controller applications the IU can function by itself with high speed local memory only.

### CY7C601 Integer Unit

The IU is the basic processing engine which executes all of the instruction set except for floating-point operations. The CY7C601 IU contains a large 136 x 32 triple-port register file which is divided into 8 windows. Each window contains 24 working registers and has access to the same 8 global registers. A current window pointer (CWP) field in the Processor State Register keeps track of which window is currently active. The CWP is decremented when the processor calls a subroutine and is incremented when the processor returns.

The registers in each window are divided into ins, outs, and locals. Each window shares its ins and outs with adjacent windows. The outs of the previous window are the ins of the current window, and the outs of the current window are the ins of the next window. The globals are equally available to all windows and the locals are unique to each

window. The windows are joined together in a circular stack where the outs of the last window are the ins of the first window.

The IU supports a multitasking operating system by providing user and supervisor modes. Some instructions are privileged and can only be executed while the processor is in supervisor mode. Changing from user to supervisor mode requires taking a hardware interrupt or executing a trap instruction.

The IU supports both asynchronous traps (interrupts) and synchronous traps (error conditions and trap instructions). Traps transfer control to an offset within a table. The base address of the table is specified by a Trap Base Register and the offset is a function of the trap type. Traps are taken before the current instruction causes any changes visible to the programmer and can therefore be considered to occur between instructions.

### CY7C608 Floating-Point Controller

The CY7C608 Floating-Point Controller (FPC), in combination with a CY7C609 Floating-Point Processor (FPP), form a SPARC compatible Floating-Point Unit or FPU. The FPU and CY7C601 IU operate concurrently. The FPU recognizes floating-point instructions and places them in a queue while the IU continues to execute non-floating-point instructions. If the FPU encounters an instruction which will not fit in its queue, the FPU holds the IU until the instruction can be stored.

The FPU contains its own set of registers on which it operates. The contents of these registers are transferred to and from external memory under control of the IU via floating-point load/store instructions. Processor interlock hardware provides floating-point concurrency which guarantees that the programming model is preserved from the point of view of the compiler or assembly language programmer. A program containing floating-point computations generates the same results as if instructions were executed sequentially.

### CY7C609 Floating-Point Processor

The CY7C609 combines a multiplier and an arithmetic logic unit in a single microprogrammable VLSI device. The CY7C609 is capable of operating at the same clock rate as the Cypress IU and FPC and provides on the order of 4 to 4.9 Megaflops of double precision Linpack floating-point performance when operated at 33 MHz with these devices. The CY7C609 is fully compatible with the IEEE standard for binary floating-point arithmetic, STD 754-1985. The Floating-Point Processor performs both single and double precision operations, including division and square root.

### CY7C604 Cache Controller and Memory Management Unit

The CY7C604 Cache Controller and Memory Management Unit (CMU) provides hardware support for a demand-paged virtual memory environment for the CY7C601 processor. The CY7C604 conforms to the standard SPARC architecture definition for memory management. Page size is fixed at 4K bytes. The CMU translates 32-bit virtual addresses from the processor into 36-bit physical addresses and provides both write-through and buffered copy-back cache policies. The on-chip context register allows support of up to 4096 contexts.

High speed address look-up is provided by an on-chip translation lookaside buffer. Each entry contains the virtual to physical mapping of a 4K byte page. If a virtual address match is detected in one of the TLB entries, the physical address translation contained in that entry will be delivered to the outputs of the CMU. If the virtual address from the processor has no corresponding entry in the CMU, the CMU will automatically perform address translation for the virtual address using on-chip hardware to access a main memory resident three-level page table. Each "matched" TLB entry is checked for protection violation automatically and violations are reported to the Integer Unit as memory exceptions.

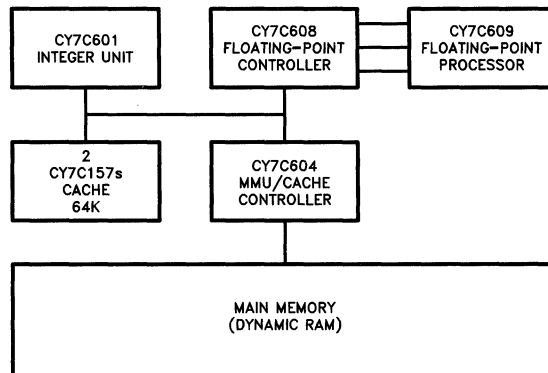
The CMU also provides storage for 2048 cache address tags for a 64K byte cache with a 32 byte line size. The tag entries can be directly written or read by the processor. In normal operation, twelve low order bits 15-5 of the virtual address from the processor are used to select one of the tag entries in the CY7C604 and its 16-bit contents are compared on chip with the 16 high order processor address bits to determine if the cache contains the required data or instruction. This cache hit/miss comparison is then qualified by various built-in protection checks and the result is output. Pipelined accesses are supported via on-chip registers which capture both address and data from the processor.

The CY7C604 also contains the logic required in a system to implement the byte and half-word write capabilities provided in the SPARC instruction set. Cache tag update is also simplified by an automatic tag update on miss feature which eliminates the need for processor accesses during tag update.

### CY7C157 Cache Data RAM

The CY7C157 16K x 16 static RAMs are designed to interface easily to and provide maximum performance for the CY7C600 processor. The RAM has registered address inputs and latched data inputs and outputs as well as a self-timed write pulse which greatly simplifies the design of cache memories for the CY7C601 Integer Unit. The device has a single clock that controls loading of the address register, data input latches, data output latches, pipeline control latch, and chip enable register. The chip enable is clocked into a register and pipelined through a control register to condition the output enable. This pipelined design allows a cache that works as an extension of the internal instruction pipeline of the CY7C601 Integer Unit thereby maximizing performance. The write enable is edge-activated and self-timed thereby eliminating the need for the user to generate accurate write pulses in external logic. A separate asynchronous output enable is provided to disable outputs during a write or to allow other devices access to the bus.

6



Full System Block Diagram

0132-1



# Very High Performance 32-Bit RISC Processor

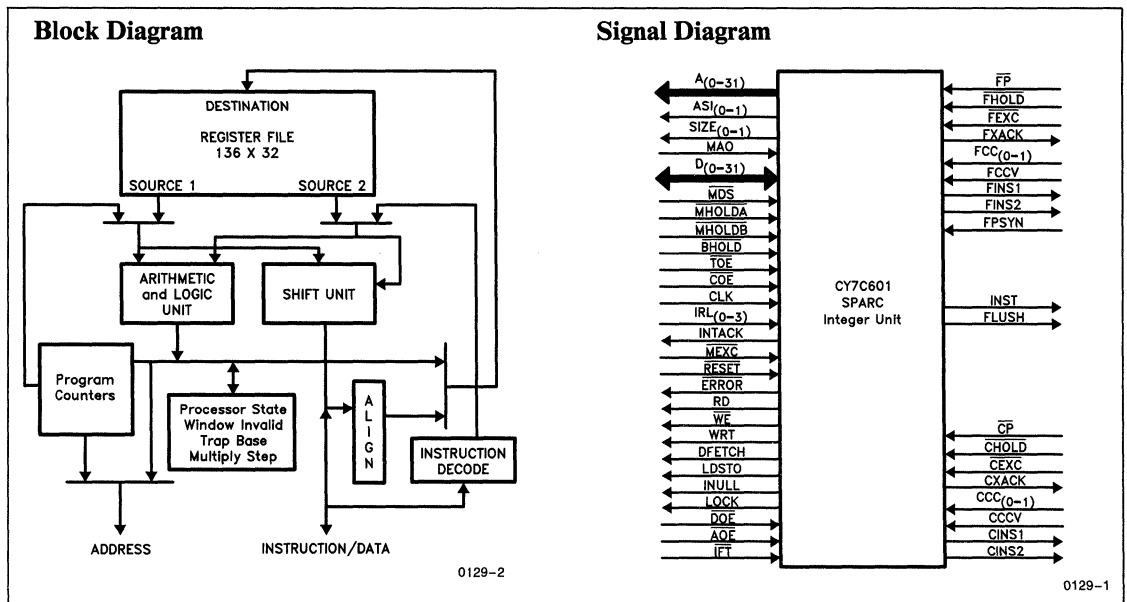
## Features

- **Reduced Instruction Set Computer (RISC) architecture**
  - Simple format instructions
  - Most instructions execute in single cycle
- **Very high performance**
  - 25 ns instruction cycle with 4-stage pipeline
  - 33 Million Instructions Per Second (MIPS)
  - 27 equivalent VAX® MIPS
  - 150 ns Interrupt Response
- **Large windowed register file**
  - 136 general purpose 32-bit registers
  - 8 overlapping windows of 24 registers each
  - 4 separate register banks
- **Large virtual address space**
  - 32-bit virtual address bus
  - 8-bit address space identifier
- **Hardware Pipeline Interlocks**
- **Multitasking support**
  - User/supervisor modes
  - Privileged instructions
- **Parallel processing support**
- **Artificial intelligence support**
- **High performance coprocessor interface**
  - Concurrent execution of floating-point instructions
- **0.8 micron CMOS technology**
- **207 pin grid array package**
- **Power 3.3 watts maximum**

## Overview

The CY7C601 Integer Unit is a high speed CMOS implementation of the SPARC™ 32-bit RISC architecture processor. This architecture makes possible the creation of a processor which can execute instructions at rates approaching one instruction per processor clock. The CY7C601 supports a tightly-coupled floating-point coprocessor and a second implementation-definable coprocessor. The CY7C601 SPARC processor provides the following features:

**Simple Instruction Format**—All instructions are 32 bits wide and are aligned on 32-bit boundaries in memory. There are only three basic instruction formats which feature uniform placement of opcode and address fields.



## Selection Guide

|  |            | 7C601-40 | 7C601-33 | 7C601-25 |
|--|------------|----------|----------|----------|
| Maximum Operating Current (mA) I <sub>CC</sub> | Commercial | 650      | 600      | 500      |
|  | Military   |          |          | 500      |

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## Overview (Continued)

**Register-Intensive Architecture**—Most instructions operate on either two registers or one register and a constant, and place the result in a third register. Only load and store instructions access off chip memory.

**A Large “Windowed” Register File**—The processor has 136 on-chip 32-bit registers configured as 8 overlapping sets of 24 registers each and 8 global registers. This scheme allows compilers to cache local values across subroutine calls, and provides a register-based parameter passing mechanism.

**Delayed Control Transfer**—The processor always fetches the next instruction after a control transfer, and either executes it or annuls it depending on the state of a bit in the control transfer instruction. This feature allows compilers to rearrange code to place a useful instruction after a delayed control transfer and thereby take better advantage of the processor’s pipeline.

**Concurrent Floating Point**—Floating point instructions can execute concurrently with each other and with non-floating point instructions.

**Fast Interrupt Response**—Interrupt inputs are sampled on every clock cycle and can be acknowledged in one to three cycles. The first instruction of an interrupt service routine can be executed within 6 to 8 cycles of receiving the interrupt request.

## The 7C600 Family

The SPARC processor family consists of a CY7C601 Integer Unit (IU) to perform all non-floating point operations and a CY7C608 Floating Point Controller (FPC) which interfaces to a CY7C608 Floating Point Processor (FPP) to perform floating point arithmetic concurrent with the IU. Support is also provided for a second generic coprocessor interface. The IU communicates with external memory via a 32-bit address bus and a 32-bit data/instruction bus. In typical data processing applications, the IU and FPC (FPC/FPP) are combined with a high performance CY7C604 Memory Management Unit and Cache Controller and a cache memory implemented with CY7C157 16K x 16 Cache RAMs. In many dedicated controller applications the IU can function by itself with high speed local memory.

## Coprocessor Interface

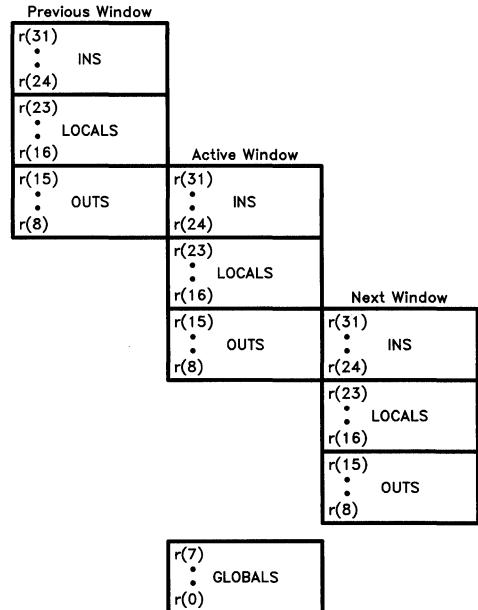
The IU is the basic processing engine which executes all of the instruction set except for floating point operations. The FPC/FPP and IU operate concurrently. The FPC/FPP recognizes floating point instructions and places them in a queue while the IU continues to execute non-floating point instructions. If the FPC/FPP encounters an instruction which will not fit in its queue, the FPC/FPP holds the IU until the instruction can be stored. The FPC/FPP contains its own set of registers on which it operates. The contents of these registers are transferred to and from external memory under control of the IU via floating point load/store instructions. Processor interlock hardware hides floating point concurrency from the compiler or assembly language programmer. A program containing floating point

computations generates the same results as if instructions were executed sequentially.

## Registers

The CY7C601 IU contains a large 136 X 32 triple port register file which is divided into 8 windows, each with twenty-four working registers, and each having access to the same eight 32-bit global registers. A current window pointer (CWP) field in the processor state register (PSR) keeps track of which window is currently active.

The CWP is decremented when the processor executes a call to a subroutine and is incremented when the processor returns.



0129-3

The registers in each window are divided into ins, outs, and locals. The eight global registers are shared by all windows and appear as registers 0–7 in each window. Registers 8–15 serve as outs, registers 16–23 as locals, and 24–31 as ins. Each window shares its ins and outs with adjacent windows. The outs of a previous window are the ins of the current window, and the outs of the current window are the ins of the next window. The globals are equally available to all windows and the locals are unique to each window. The windows are joined together in a circular stack where the outs of window 7 are the ins of window 0.

## Multitasking Support

The IU supports a multitasking operating system by providing user and supervisor modes. Some instructions are privileged and can only be executed while the processor is in supervisor mode. Changing from user to supervisor mode requires taking a hardware interrupt or executing a trap instruction.

## Interrupts and Traps

The IU supports both asynchronous traps (interrupts) and synchronous traps (error conditions and trap instructions). Traps transfer control to an offset within a table. The base address of the table is specified by a Trap Base Register and the offset is a function of the type of trap. Traps are taken before the current instruction causes any changes visible to the programmer and therefore can be considered to occur “between” instructions.

## Instruction Set Summary

Instructions fall into five basic categories:

**1. Load and Store Instructions**—Load and store instructions are the only instructions which access external memory. They use two IU registers or one IU register and a signed immediate value to generate the memory address. The instructions destination field specifies either an IU register, a FPC register or a coprocessor register as the destination for a load or the source for a store. Integer load and store instructions support 8, 16, 32, and 64 bit accesses while floating point and coprocessor instructions support 32- and 64-bit accesses.

**2. Arithmetic/Logical/Shift**—These instructions compute a result that is a function of two source operands and write the result into a destination register or discard it. They perform arithmetic, tagged arithmetic, logical and shift operations. An instruction SETHI, useful in creating a 32-bit constant in two instructions, writes a 22-bit constant into the high order bits of a register and zeroes the remaining bits. The contents of any register can be shifted left or right any number of bits in one clock cycle as specified by the instruction itself or by another register. The tagged arithmetic instructions are useful in artificial intelligence applications.

**3. Control Transfer**—Control transfer instructions include jumps, calls, traps and branches. Control transfer is usually delayed so that the instruction immediately following the control transfer (called the delay instruction) is executed before control is transferred to the target location. The delay instruction is always fetched, however a bit in the control transfer instruction can cause the delay instruction to be nullified if the branch is not taken. This flexibility increases the likelihood that a useful instruction can be placed after a control transfer instruction thereby filling an otherwise unused hole in the processor’s pipeline. Branch and call instructions use program counter relative displacements. A jump and link instruction uses a register indirect displacement: computing its target address as either the sum of two registers, or the sum of a register and a 13-bit signed immediate value. The branch instruction provides a displacement of plus or minus 8 megabytes, and the call instructions 30-bit displacement allows transfer to almost any address.

**4. Read/Write Control Registers**—The processor provides instructions to read and write the contents of the various control registers within the machine. These registers include the Multiply Step Register, Processor State Register, Window Invalid Mask Register, and Trap Base Register. An instruction is also provided to flush the processor’s internal instruction cache.

**5. Floating Point and Coprocessor Operations**—Floating point operations include floating point calculations and operations on floating point registers. These operations execute concurrently with both IU instructions and with other floating point instructions whenever possible. Coprocessor operations are instructions which will be executed by an optional coprocessor.

The Instruction set of the processor is summarized in Table 1.

**Table 1. Instruction Set Summary**

| Name          | Operation                                     | Cycles |
|---------------|---|--------|
| LDSB (LDSBA*) | Load Signed Byte (from Alternate Space)       | 2      |
| LDSH (LDSHA*) | Load Signed Halfword (from Alternate Space)   | 2      |
| LDUB (LDUBA*) | Load Unsigned Byte (from Alternate Space)     | 2      |
| LDUH (LDUHA*) | Load Unsigned Halfword (from Alternate Space) | 2      |
| LD (LDA*)     | Load Word (from Alternate Space)              | 2      |
| LDD (LDDA*)   | Load Doubleword (from Alternate Space)        | 3      |
| LDF           | Load Floating Point                           | 2      |
| LDDF          | Load Double Floating Point                    | 3      |
| LDFSR         | Load Floating Point State Register            | 2      |
| LDC           | Load Coprocessor                              | 2      |
| LDDC          | Load Double Coprocessor                       | 3      |
| LDCSR         | Load Coprocessor State Register               | 2      |
| STB (STBA*)   | Store Byte (into Alternate Space)             | 3      |
| STH (STHA*)   | Store Halfword (into Alternate Space)         | 3      |
| ST (STA*)     | Store Word (into Alternate Space)             | 3      |
| STD (STDA*)   | Store Doubleword (into Alternate Space)       | 4      |

**Table 1. Instruction Set Summary (Continued)**

| Name              | Operation   | Cycles         |
|-------------------|---|----------------|
| STF               | Store Floating Point                                  | 3              |
| STDF              | Store Double Floating Point                           | 4              |
| STFSR             | Store Floating Point State Register                   | 3              |
| STDFQ*            | Store Double Floating Point Queue                     | 4              |
| STC               | Store Coprocessor                                     | 3              |
| STDC              | Store Double Coprocessor                              | 4              |
| STCSR             | Store Coprocessor State Register                      | 3              |
| STDCQ*            | Store Double Coprocessor Queue                        | 4              |
| LDSTUB (LDSTUBA*) | Atomic Load/Store Unsigned Byte (in Alternate Space)  | 4              |
| SWAP (SWAPA*)     | Swap r Register with Memory (in Alternate Space)      | 4              |
| ADD (ADDcc)       | Add (and modify icc)                                  | 1              |
| ADDX (ADDXcc)     | Add with Carry (and modify icc)                       | 1              |
| TADDcc (TADDccTV) | Tagged Add and modify icc (and Trap on overflow)      | 1              |
| SUB (SUBcc)       | Subtract (and modify icc)                             | 1              |
| SUBX (SUBXcc)     | Subtract with Carry (and modify icc)                  | 1              |
| TSUBcc (TSUBccTV) | Tagged Subtract and modify icc (and Trap on overflow) | 1              |
| MULScc            | Multiply Step and modify icc                          | 1              |
| AND (ANDcc)       | And (and modify icc)                                  | 1              |
| ANDN (ANDNcc)     | And Not (and modify icc)                              | 1              |
| OR (ORcc)         | Inclusive Or (and modify icc)                         | 1              |
| ORN (ORNcc)       | Inclusive Or Not (and modify icc)                     | 1              |
| XOR (XORcc)       | Exclusive Or (and modify icc)                         | 1              |
| XNOR (XNORcc)     | Exclusive Nor (and modify icc)                        | 1              |
| SLL               | Shift Left Logical                                    | 1              |
| SRL               | Shift Right Logical                                   | 1              |
| SRA               | Shift Right Arithmetic                                | 1              |
| SETHI             | Set High 22 Bits of r Register                        | 1              |
| SAVE              | Save caller's window                                  | 1              |
| RESTORE           | Restore caller's window                               | 1              |
| Bicc              | Branch on integer condition codes                     | 1**            |
| FBicc             | Branch on floating point condition codes              | 1**            |
| CBicc             | Branch on coprocessor condition codes                 | 1**            |
| CALL              | Call  | 1**            |
| JMPL              | Jump and Link   | 2**            |
| RETT              | Return from Trap                                      | 2**            |
| Ticc              | Trap on integer condition codes                       | 1 (4 if Taken) |
| RDY               | Read Y Register                                       | 1              |
| RDPSR             | Read Processor State Register                         | 1              |
| RDWIM             | Read Window Invalid Mask                              | 1              |
| RDTBR             | Read Trap Base Register                               | 1              |
| WRY               | Write Y Register                                      | 1              |
| WRPSR*            | Write Processor State Register                        | 1              |
| WRWIM*            | Write Window Invalid Mask                             | 1              |
| WRTBR*            | Write Trap Base Register                              | 1              |
| UNIMP             | Unimplemented Instruction                             | 1              |
| IFLUSH            | Instruction Cache Flush                               | 1              |
| FPop              | Floating Point Unit Operations                        | 1 to Launch    |
| CPop              | Coprocessor Operations                                | 1 to Launch    |

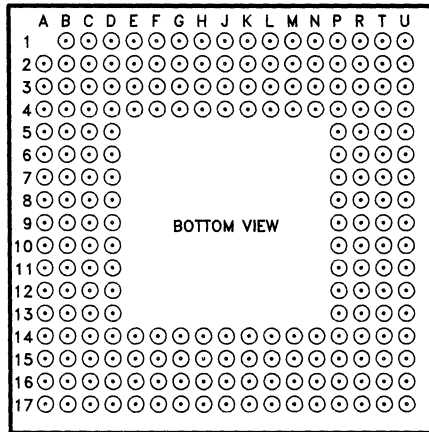
\*privileged instruction

\*\*assuming delay slot is filled with useful instruction



Table 2. Pin Table

| Pin Name        | Pin Number | Pin Name          | Pin Number | Pin Name          | Pin Number  |
|-----------------|------------|-------------------|------------|-------------------|---|
| A <sub>0</sub>  | K2         | D <sub>23</sub>   | J17        | CINS <sub>2</sub> | C17   |
| A <sub>1</sub>  | K1         | D <sub>24</sub>   | H17        | CXACK             | C13   |
| A <sub>2</sub>  | L3         | D <sub>25</sub>   | H15        | IRL <sub>0</sub>  | A10   |
| A <sub>3</sub>  | L1         | D <sub>26</sub>   | G17        | IRL <sub>1</sub>  | C11   |
| A <sub>4</sub>  | L2         | D <sub>27</sub>   | H16        | IRL <sub>2</sub>  | D10   |
| A <sub>5</sub>  | M2         | D <sub>28</sub>   | G16        | IRL <sub>3</sub>  | B12   |
| A <sub>6</sub>  | N2         | D <sub>29</sub>   | F16        | INTACK            | A13   |
| A <sub>7</sub>  | M1         | D <sub>30</sub>   | F15        | RESET             | A9  |
| A <sub>8</sub>  | M3         | D <sub>31</sub>   | G15        | ERROR             | B15   |
| A <sub>9</sub>  | P1         | ASI <sub>0</sub>  | F3         | TOE               | C15   |
| A <sub>10</sub> | P2         | ASI <sub>1</sub>  | F2         | FP SYN            | C12   |
| A <sub>11</sub> | N1         | ASI <sub>2</sub>  | G3         | CLK               | K3  |
| A <sub>12</sub> | N3         | ASI <sub>3</sub>  | G2         | VSSO              | B16 F17 R5<br>B17 H4 R14<br>C3 J2 T16<br>C4 K14 T17<br>D6 N14 U16<br>D14 P4 U17<br>F1 P6<br>F4 P11<br>F14 P14 |
| A <sub>13</sub> | R3         | ASI <sub>4</sub>  | G1         | VCCO              | A15 L4<br>A16 M14<br>A17 N4<br>D1 P8<br>D12 P12<br>D17 P16<br>E1 P17<br>G4 R16<br>K4 R17<br>K15               |
| A <sub>14</sub> | R2         | ASI <sub>5</sub>  | H2         | VSSI              | A3 J3 U2<br>A14 L14 U10<br>B2 M4<br>B3 P5<br>B9 P7<br>C1 R1<br>C16 R11<br>D13 T1<br>E15 T15<br>H14 U1         |
| A <sub>15</sub> | R4         | ASI <sub>6</sub>  | H1         | VCCI              | A2 R7<br>B1 R12<br>D7 T2<br>E14 T3<br>E16 U3<br>G14 U4<br>H3<br>J15<br>P10                                    |
| A <sub>16</sub> | T4         | ASI <sub>7</sub>  | J1         | VSST              | D9 J14<br>J4 P9   |
| A <sub>17</sub> | T5         | SIZE <sub>0</sub> | E2         | VCCCT             | D5 P13  |
| A <sub>18</sub> | R6         | SIZE <sub>1</sub> | D2         |                   |   |
| A <sub>19</sub> | T6         | MEXC              | D8         |                   |   |
| A <sub>20</sub> | U5         | MHOLDA            | C8         |                   |   |
| A <sub>21</sub> | U6         | MHOLDB            | B8         |                   |   |
| A <sub>22</sub> | U7         | BHOLD             | A7         |                   |   |
| A <sub>23</sub> | T7         | AOE               | P3         |                   |   |
| A <sub>24</sub> | U8         | DOE               | N17        |                   |   |
| A <sub>25</sub> | T8         | COE               | C2         |                   |   |
| A <sub>26</sub> | U9         | MDS               | B7         |                   |   |
| A <sub>27</sub> | R8         | MAO               | E3         |                   |   |
| A <sub>28</sub> | T9         | IFT               | C14        |                   |   |
| A <sub>29</sub> | R9         | RD                | A4         |                   |   |
| A <sub>30</sub> | T10        | WE                | B4         |                   |   |
| A <sub>31</sub> | U11        | LDSTO             | C5         |                   |   |
| D <sub>0</sub>  | R10        | I NULL            | B5         |                   |   |
| D <sub>1</sub>  | T11        | LOCK              | D4         |                   |   |
| D <sub>2</sub>  | U12        | DXFER             | D3         |                   |   |
| D <sub>3</sub>  | T12        | WRT               | E4         |                   |   |
| D <sub>4</sub>  | U13        | FP                | C7         |                   |   |
| D <sub>5</sub>  | T13        | FCC <sub>0</sub>  | A11        |                   |   |
| D <sub>6</sub>  | T14        | FCC <sub>1</sub>  | B11        |                   |   |
| D <sub>7</sub>  | R13        | FCCV              | C10        |                   |   |
| D <sub>8</sub>  | U14        | FHOLD             | A8         |                   |   |
| D <sub>9</sub>  | U15        | FEXC              | A5         |                   |   |
| D <sub>10</sub> | R15        | CP                | B6         |                   |   |
| D <sub>11</sub> | P15        | CCC <sub>0</sub>  | A12        |                   |   |
| D <sub>12</sub> | N15        | CCC <sub>1</sub>  | B13        |                   |   |
| D <sub>13</sub> | M15        | CCC <sub>2</sub>  | B10        |                   |   |
| D <sub>14</sub> | M16        | CHOLD             | C9         |                   |   |
| D <sub>15</sub> | N16        | CEXC              | A6         |                   |   |
| D <sub>16</sub> | L15        | INST              | C6         |                   |   |
| D <sub>17</sub> | M17        | FLUSH             | B14        |                   |   |
| D <sub>18</sub> | L16        | FINS <sub>1</sub> | E17        |                   |   |
| D <sub>19</sub> | L17        | FINS <sub>2</sub> | D16        |                   |   |
| D <sub>20</sub> | K16        | FXACK             | D11        |                   |   |
| D <sub>21</sub> | K17        | CINS <sub>1</sub> | D15        |                   |   |
| D <sub>22</sub> | J16        |                   |            |                   |   |



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### Ordering Information

| Clock Frequency (MHz) | Ordering Code | Package Type | Operating Range |
|-----------------------|---------------|--------------|-----------------|
| 40                    | CY7C601-40GC  | G208         | Commercial      |
| 40                    | CY7C601-40BC  | B208         |                 |
| 33                    | CY7C601-33GC  | G208         |                 |
| 33                    | CY7C601-33BC  | B208         |                 |
| 25                    | CY7C601-25GC  | G208         |                 |
| 25                    | CY7C601-25BC  | B208         |                 |
| 25                    | CY7C601-25GMB | G208         | Military        |



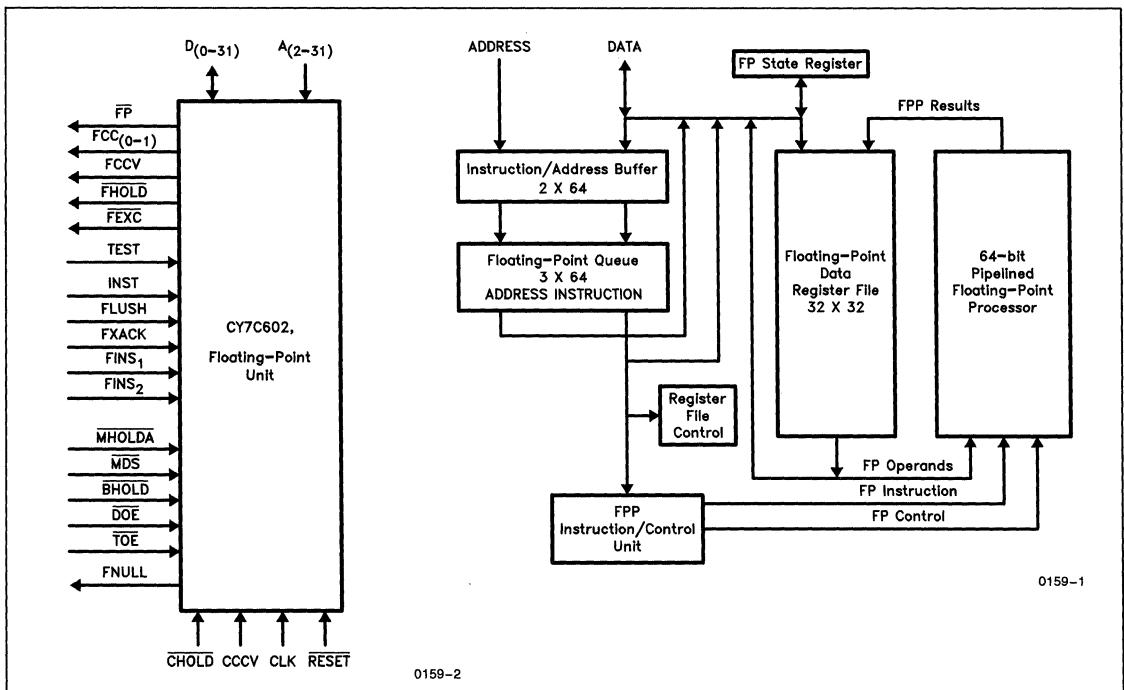
**Features**

- Combines functions of CY7C608 floating-point controller and CY7C609 floating-point processor in a single package
- Provides SPARC™ compatible floating-point arithmetic and registers
- Very high performance
  - 30 ns cycle
  - Instructions launched in single cycle
  - 4.2 million double precision linpack floating-point operations per second
- 3 deep floating-point queue stores both instructions and addresses to provide precise exceptions
- 32 x 32 floating-point register file
- High performance coprocessor interface
  - Concurrent execution of integer and floating-point instructions
  - Hardware interlocks synchronize integer and floating-point operations
- Meets IEEE standard 754-1985 for single and double precision formats
- 144 pin grid array package

chip floating-point solution for the CY7C601 Integer Unit by integrating the CY7C609 Floating-Point Processor (FPP) and CY7C608 Floating-Point Controller (FPC) into a single device. The CY7C602 provides high performance SPARC compatible single and double precision floating-point arithmetic. The FPU performs add, subtract, multiply, divide, square root, compare, and convert as well as register to register move instructions, floating-point loads and stores, floating-point state register, and floating-point queue store instructions. Instructions which are unimplemented by the FPU (extended precision operations) will cause an Unimplemented FPop trap, in which case the instruction will be emulated in software.

**Overview**

The CY7C602 Floating-Point Unit (FPU) is designed to provide a single



**Selection Guide**

|                                |            | 7C602-33 | 7C602-25 |
|--------------------------------|------------|----------|----------|
| Maximum Operating Current (mA) | Commercial | TBD      | TBD      |

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# Cache Controller and Memory Management Unit (CMU)

## Features

- Fully conforms to the SPARC™ reference Memory Management Unit (MMU) architecture
- Supports 4096 contexts
- Fixed 4K-byte page size
- On-chip translation lookaside buffer (TLB)
  - 64 fully associative entries
  - Multi level flush and probe support
  - Lockable entries
  - Random replacement algorithm
- Page level protection
- Large address space support
  - 32-bit virtual address
  - 36-bit physical address
- Hardware table walk
- Sparse address space support with 3-level map
- 2048 direct mapped cache tag entries
- Write through and copy-back cache policies
  - 1 32-byte read line buffer
  - 1 32-byte write line buffer
- 32 byte cache line size
- Aliasing detection
- Byte write generation
- Scalable cache architecture
  - Cascadeable
- 0.8 micron CMOS technology
- 244 pin grid array package and 196 plastic quad flatpack

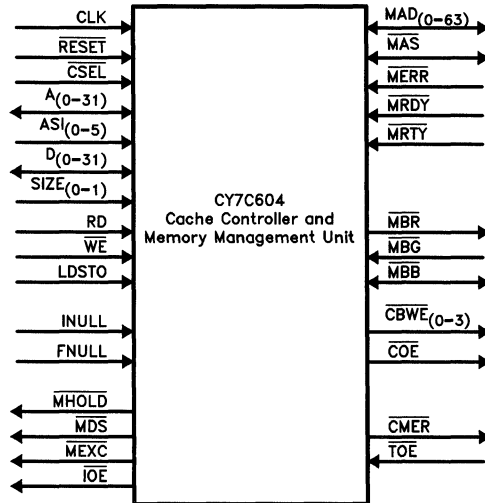
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## Introduction

The CY7C604 comprises a Cache Tag and a Memory Management Unit (CMU). It is a high speed CMOS implementation of the SPARC reference Memory Management architecture, Cache Tag, and Cache Controller. The CY7C604 directly connects to the CY7C601 processor and CY7C157 cache data RAM without any external circuitry.

The CMU, when combined with two CY7C157 16K x 16 cache RAMs, forms a complete 64K-byte direct mapped cache. Cache size can be scaled. The CMU translates 32-bit virtual addresses from the processor into 36-bit physical addresses. The on-chip context register allows support of

## Signal Diagram



0157-1

## Selection Guide

|                                |            | 7C604-40 | 7C604-33 | 7C604-25 |
|--------------------------------|------------|----------|----------|----------|
| Maximum Operating Current (mA) | Commercial | 650      | 600      | 550      |
|                                | Military   |          | 650      | 600      |

## Introduction (Continued)

up to 4096 contexts. High speed address translation is provided by a 64-entry fully associative Translation Lookaside Buffer (TLB). If the CMU processes a virtual address that matches one of the TLB entries, the physical address contained in that entry will be delivered to the outputs of the CMU. If the virtual address from the processor has no corresponding entry in the TLB, the CMU will perform address translation for the virtual address using a three-level page table map.

The CMU supports lockable TLB entries and a random replacement algorithm. Each matched TLB entry is checked for protection and privilege violations. If violations occur, these are reported to the 7C601 Integer Unit as memory exceptions. Each page can be declared as either cacheable or non-cacheable by using the cacheable "C" bit.

The CMU provides 2048 direct mapped cache tag entries. The cache tag entries and the TLB are searched concurrently for a match with the virtual address. Both write-through and copy-back cache policies are supported with a 32-byte line size. Address aliasing is checked each time a cache tag entry is replaced. If the new virtual address is mapped to the cache line selected for replacement, the CMU will ignore the main memory access and modify the cache tag accordingly.

The CMU provides on-chip buffer to enhance data transfers between cache memory and main memory: a 32-byte read buffer and a set of write buffers. In copy-back mode, the 32-byte write buffer is used to store the modified cache line being replaced in the cache, allowing the main memory read to proceed as soon as the memory bus is acquired. The read buffer stores data from main memory temporarily before it is written into the cache memory. The write buffers are used in the write through mode to capture address and data from the IU during write accesses, and allow the IU to continue processing while the buffer contents are transferred into main memory over the memory bus.

The memory bus implements the 64-bit Mbus SPARC reference specification. Architecturally, up to 16 CMUs can be used in the same system to expand the cache tag, cache size and TLB storage. The CMU is fabricated with Cypress' 0.8 micron CMOS drawn process and is available in a 196-pin plastic quad flatpack and a 244-pin ceramic PGA.

## Memory Management Unit

### Translation Look-aside Buffer

The TLB contains 64 fully associative entries. All entries are searched simultaneously when a virtual address is presented to the CMU. The virtual tag and the context field from each entry are compared with the virtual address bits from the processor and the current context in the Context Register (CXR), respectively. If a match is found in one of the entries, the physical address field of that entry will be passed to the Physical Address outputs of the CMU. If no match is found, the CMU will perform dynamic address

translation on the virtual address and store the new mapping into a TLB entry selected by a random replacement algorithm.

### TLB Entry Contents

Each entry in the TLB contains a 20-bit Virtual Address Tag, a 12-bit context field (CXT 11–0), two shorted translation indicator bits (ST1, ST0), a 24-bit Physical Page Number (PPN), a cacheable bit (C), a Modified bit (M), three access permission bits (ACC 2–0) and a Valid bit (V).

During a TLB look-up, the upper 20 bits of the virtual address and the context number of the access are compared with the virtual address and context number fields of each entry based on the short translation bits in each entry. The short translation bits are included in order to provide a linear address mapping facility of 256K, 16M, or 4G bytes with a single TLB entry.

The 24-bit Physical Page Number field contains the higher order bits of the physical address. This field, when concatenated with the 12-bit byte offset from the virtual address, forms a complete 36-bit physical address.

The Modified (M) bit of an entry is set whenever the page has been modified. During page replacement, the operating system uses this bit to determine whether the selected page must be copied to secondary storage or not.

The Cacheable (C) bit determines whether an access associated with that page is cacheable or not. The state of the C bit in a matched entry is available on the Mbus during the address phase of a transaction. If the cacheable bit is set high, then the entry is cacheable. If this bit is cleared, the data accessed by the IU will not be written into the cache.

The three Access Permission (ACC 2–0) bits indicate whether access to the page is allowed for the current transaction. The Address Space Identifier (ASI) from the IU specifies whether a given access is a data or instruction reference, and whether it is performed in the supervisor or user space. Read and write information is derived from the RD and WE inputs.

### Multiple Contexts

4096 contexts are supported in the CMU via a 12-bit field in the Context Register (CXR). The context is used by both the cache tag and the TLB. For supervisor accesses, if the "S" bit is set the context number comparison is ignored.

### Fault Reporting

The CMU detects and reports the following faults:

- Instruction access error
- Data access error
- Translation access error
- Bus error
- Privilege Violation
- Protection Violation

|     |           |     |   |   |          |         |   |
|-----|-----------|-----|---|---|----------|---------|---|
| VAT | CXT(11–0) | PPN | C | M | ACC(2–0) | ST(1–0) | V |
|-----|-----------|-----|---|---|----------|---------|---|

Figure 1. TLB Entry Format

## Memory Management Unit (Continued)

### Linear Address Mapping

The 7C604 CMU provides the ability to translate a contiguous virtual address space to a contiguous physical address space of equal size with a single TLB entry. This function is achieved by placing a page table entry (Entry Type = 2) in a location normally occupied by a page pointer (Entry Type = 1) such as the context table, the first level page table, or the second level page table. By replacing a page pointer with a page entry, the table walk process stops as soon as the page table entry is encountered. Depending on where the PTE is placed, 4 mapping sizes are available:

| PTE Location            | Linear Map Size |
|-------------------------|-----------------|
| Third Level Page Table  | 4 Kb            |
| Second Level Page Table | 256 Kb          |
| First Level Page Table  | 16 Mb           |
| Context Table           | 4 Gb            |

### Flush and Probe Operations

Flushing causes the invalidation of TLB entries while probing returns the physical translation of virtual addresses generated by the IU. A flush is accomplished by writing to an alternate address space recognized by the CMU. Flushing can be performed on the entire TLB, on matching any index level in the TLB, or on any context within the TLB. A probe is accomplished by reading from the same alternate address space. Both flush and probe operation are word accesses.

## Cache TAG and Controller

### Cache Operations

The CMU supports both write-through with no write allocate and copy-back with write allocate modes. Two types of buffers: write buffer and read buffer are provided on-chip to enhance cache operations. In write-through mode, the write buffer is used to store four double store data. In copy-back mode, the same write buffer is used to hold the dirty line from cache memory when a line is replaced. A 32-byte read buffer is provided to load data from main memory.

### Address Synonyms or Aliasing Detection

Virtual addressing allows multiple virtual addresses to map into the same physical address. Any modification to a virtual location may cause data inconsistency in the cache because the change is not reflected in other cache locations mapped to the same physical address. Address aliasing is checked by the CMU whenever a cache line is replaced in the copy back mode and during read misses in the write through mode. The physical address of the displaced line is obtained by passing the virtual tag through the memory management unit. An alias is detected if the new and the displaced virtual addresses are mapped to the same physical location. If the miss was caused by a read, no cache updating is required because the existing line will already contain the correct data. In this case the tag is simply updated to reflect the new address. If the miss was caused by a write, the location addressed by the IU will be modified and the tag is updated to reflect the new address.

### Write Buffer

The write buffers are used in the copy back mode to provide temporary storage for the dirty cache line being replaced while the new line is being transferred from main memory. Buffering the dirty line speeds up cache miss processing because the IU can be released as soon as the cache RAMs are updated. The line buffer contents are written back to main memory only when free memory bus cycles become available. When the line buffer is full, the cache controller will wait for it to empty before processing the cache miss. The same write buffers are used in the write-through mode to store four double store data. The processor is allowed to continue without waiting for the main memory update to complete. The buffer contents are written back to main memory whenever the memory bus becomes available.

### Read Buffer

The read buffer is 32 bytes. It is used to hold data being retrieved from main memory. Since memory bus access begins as soon as a miss is detected, it is likely that the cache memory will still be busy when the first data from memory is returned. The read line buffer stores the information temporarily until the cache RAM is ready to be updated.

### Cache Miss Processing

If the physical translation of the missed address is available in the TLB, then miss processing will commence. Otherwise, the cache controller will wait for the memory management section to retrieve the physical address from the page tables before starting its actions. The first step in miss processing is the acquisition of the virtual bus by tri-stating the IU outputs. Once the control of the virtual bus is achieved, the cache controller is ready to process the cache miss. If the cacheable (C) bit is set, the cache controller will transfer data from main memory according to the programmed cache policy and update the cache. If the C bit is cleared, the cache controller simply transfers data between the IU and main memory without updating the cache.

### Non-Cacheable Accesses

During a write operation the IU data will be written into main memory over the Mbus. During a read operation the requested data will be read from main memory and presented to the IU via the virtual data bus. The cache tag is not updated.

### Cacheable Accesses

Two cache policies are supported in the CMU. They are write-through with no write allocate and copy-back with write allocate.

### Write-Through with No Write Allocate

In this mode, all write hits must update both the cache and main memory. In a write miss, only the main memory is updated. No address alias checking is performed for write accesses. Protection against aliasing is achieved by invalidating the selected cache line when a write miss is detected. Upon write misses, the physical translation of the missed address and the IU data are placed on the physical bus and a write cycle is initiated. If the miss was caused by a read, an alias check is performed. A new line will be loaded from main memory if no alias is detected. The physical address

## Cache TAG and Controller (Continued)

of the first word in the new cache line is placed on the Mbus and a burst read cycle is initiated. Each 64-bit word returning from main memory is temporarily stored in the read line buffer while the cache RAM is updated 32 bits at a time. After the last word in the line has been stored in the cache, the cache controller will drive the missed address on the virtual address lines and initiate a read. Data returning from the cache is strobed into the IU via MDS.

### Copy-Back with Write Allocate

In this mode, a write hit only modifies the data in the cache. Main memory is updated when a cache line is replaced. A write miss will cause the loading of a new line from main memory into the cache RAMs. If the tag is valid, the cache controller will check for aliasing between the cache line to be replaced and the missed address by comparing the physical translations of both virtual addresses. The virtual address of the displaced line is obtained by reading the cache tag. If the selected tag entry is invalid, no alias checking is necessary. An alias is signaled if both physical addresses match.

### Alias Detected

When an alias is detected, no loading from main memory is necessary because the cache line selected for replacement is mapped to the missed address. If the miss was caused by a read access, data originally requested by the IU is retrieved from the cache by placing the missed address on the virtual bus. Information returning on D<sub>31</sub>–D<sub>0</sub> is strobed into the IU in the following clock by the assertion of the MDS signal. The cache tag is updated to reflect the new address assignment. If the old cache line was dirty, the tag will be updated with the dirty bit set, otherwise the tag will be updated with the dirty bit cleared. If the miss was caused by a write, the cache location originally addressed by the processor will be updated with the IU data. After the write is completed, the cache is updated with the dirty bit set.

### Alias Not Detected

If the two virtual addresses are not mapped to the same physical location, the state of the dirty bit in the tag entry selected for replacement will determine whether the cache line should be copied back to main memory. Contents of the line buffer are loaded back to main memory using the burst write feature of the memory bus after the cache miss has been processed.

### Loading the New Cache Line

The physical address of the first word in the new line is placed on the physical bus and a burst read cycle is

initiated. Each 64-bit word returning from main memory is stored in the read line buffer and driven onto the virtual data lines 32 bits at a time. Cache update is activated by asserting the CWE<sub>3</sub>–CWE<sub>0</sub> outputs. When the last word in the cache line is received, the cache controller will update the cache tag with the dirty bit cleared if the miss was a read or update the cache tag with the dirty bit set if the miss was a write.

### Cache Tag

The CMU provides 2048 entries of cache tag and status information. Tag selection is controlled by the 11 address lines (A<sub>5</sub>–A<sub>15</sub>), from the IU. Each entry contains a 12-bit context field, a 16-bit cache tag field, and a 3-bit status field. The status field includes the valid (V) bit, the dirty (D) bit, and a supervisor (S) bit.

The valid bit specifies the validity of the tag entry and the dirty bit indicates whether the cache line has been modified or not. The supervisor bit indicates that the tag entry can only be accessed by the supervisor.

If a copy back cache policy is selected, the dirty bit in the tag is used by the cache controller to determine whether a cache line should be copied back to main memory when it is replaced.

### Main Memory Interface

The CMU supports a 64-bit synchronous interface with multiplexed address and data for main memory access. The main memory interface has 36 bits of address and 64 bits of data. The interface is capable of bursting information to support fast cache line fills.

### Byte Write Generation

The CY7C601 processor is capable of accessing bytes, half-words and words. The CMU decodes the size and access direction information from the IU and generates the necessary cache write enable signals.

### Multiple CMU Support

Up to 16 CMUs can be used in a system to increase the number of tags, TLB entries, and cache size. CMU configuration information is contained in the MMU Control Register (MCR). Multi-chip address (MCA) field is a 4-bit address that identifies a particular CMU. The Multi-chip Mask (MCM) field is a 4-bit code specifying the number of CMUs in the system. Five configurations: 1, 2, 4, 8, and 16 CMUs are supported. In order to initialize system configuration, the chip select input of each CMU must be connected to a different address line from the IU.



# Multiprocessor Cache Controller and Memory Management Unit (CMU-MP)

## Features

- Fully compatible with SPARC™ reference Memory Management Unit (MMU) architecture
- Multiprocessor support
  - Direct data intervention with and without reflectivity
  - Dual cache tag architecture
- Superset of CY7C604 CMU
- Direct mapped cache tag entries
  - 2048 virtual tags
  - 2048 physical tags
- Automatic miss processing via hardware table walking
- On-chip 64 entry translation lookaside buffer (TLB)
- Supports 4096 contexts
- Scalable cache architecture
  - Cascadeable: 1-16
- Page level protection
- Sparse address space support with 3-level map
- Supports write through and copy-back cache policies
  - 1 32-byte read line buffer
  - 1 32-byte write line buffer
- Aliasing detection
- Fixed 4K-byte page size
- 32 byte cache line size
- 0.8 micron CMOS technology
- 244 pin grid array package

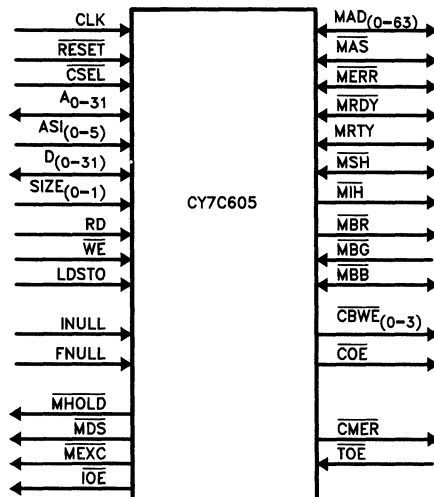
## Introduction

The CY7C605 Multiprocessor Cache Controller and Memory Management Unit (CMU-MP) is a high speed CMOS implementation of the SPARC reference Memory Management architecture. The CY7C605 directly connects to the CY7C601 processor and CY7C157 cache data RAM without any external circuitry to form a complete memory management and cache subsystem.

Multiple CY7C601, CY7C605 and CY7C157 subsystems can be used together to achieve higher performance. The CY7C605 supports a direct data intervention protocol with and without reflectivity via the SPARC reference standard 64-bit Mbus.

6

## Signal Diagram



0156-1

## Selection Guide

|                                |            | 7C605-40 | 7C605-33 | 7C605-25 |
|--------------------------------|------------|----------|----------|----------|
| Maximum Operating Current (mA) | Commercial | 650      | 600      | 550      |
|                                | Military   |          | 650      | 600      |

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Document #: 38-00092





**Features**

- Provides interface between the CY7C601 Integer Unit and CY7C609 Floating-Point Unit
- Provides SPARC™ compatible Floating-Point Arithmetic and registers
- Very high performance
  - 30 ns cycle
  - Instructions launched in single cycle
  - 4.2 million double precision lincpack Floating-Point operations per second
- 32 x 32 Floating-Point Register File
- 3 deep floating-point queue stores both instructions and addresses to provide precise exceptions

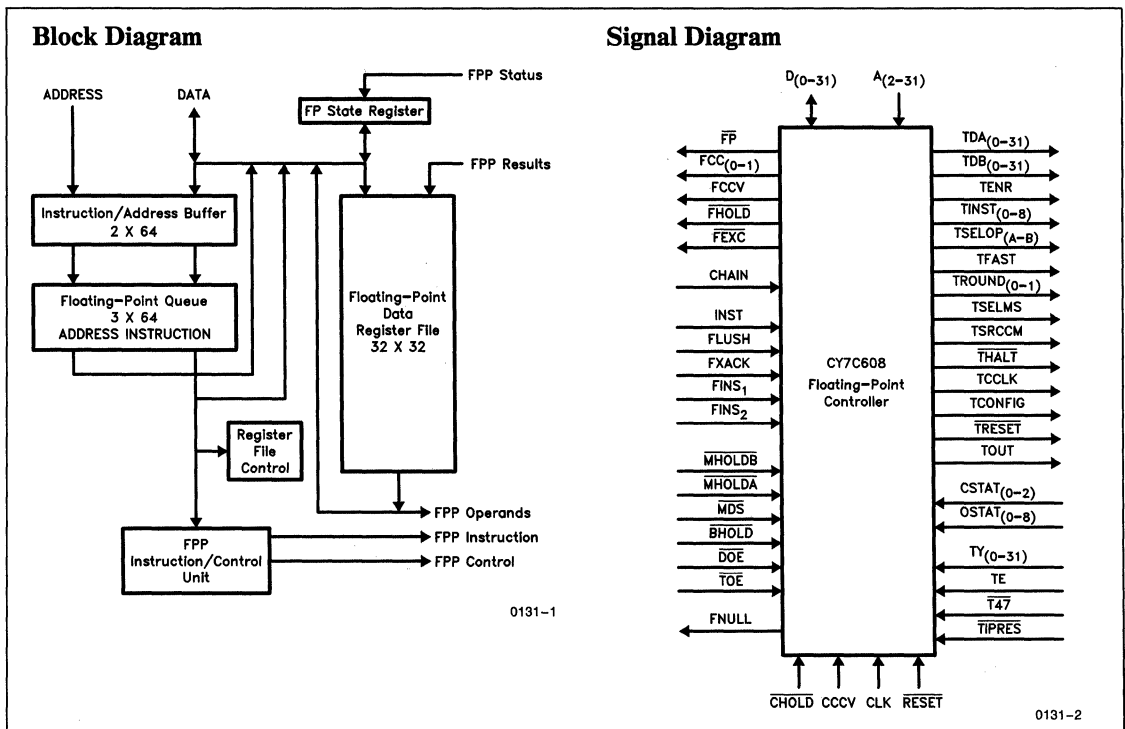
- High performance coprocessor interface
  - Concurrent execution of Integer and Floating-Point Instructions
  - Hardware Interlocks synchronize Integer and Floating-Point Operations
- 1.2 micron CMOS technology
- 299 pin grid array package
- Power 3.3 watts maximum

**Overview**

The CY7C608 Floating-Point Controller (FPC) is designed to interface the CY7C609 Floating-Point Processor

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(FPP) to the CY7C601 Integer Unit (IU). Together, the FPC and FPP provide high performance SPARC compatible single and double precision floating-point arithmetic. The FPP performs add, subtract, multiply, divide, square root, compare, and convert; while the CY7C608 FPC performs register to register move instructions, floating-point loads and stores, floating-point state register, and floating-point queue store instructions. Instructions which are unimplemented by the FPC (extended precision operations) will cause an Unimplemented FPop trap, in which case the instruction will be emulated in software.



**Selection Guide**

|                                |            | 7C608-33 | 7C608-25 |
|--------------------------------|------------|----------|----------|
| Maximum Operating Current (mA) | Commercial | 600      | 550      |

**Table 1. Floating-Point Instruction Set Summary**

| Name   | Operation  | Cycles |
|--------|--|--------|
| LDF    | Load Floating-Point Register                           | 2      |
| LDDF   | Load Double Floating-Point Register                    | 3      |
| LDFSR  | Load Floating-Point State Register                     | 2      |
| STF    | Store Floating-Point                                   | 3      |
| STDF   | Store Double Floating-Point                            | 4      |
| STFSR  | Store Floating-Point State Register                    | 3      |
| STDFQ* | Store Double Floating-Point Queue                      | 4      |
| FiTOs  | Convert Integer to Single Precision                    | 8      |
| FiTOd  | Convert Integer to Double Precision                    | 8      |
| FiTOx  | Convert Integer to Extended Precision                  | #      |
| FsTOi  | Convert Single Precision to Integer                    | 8      |
| FdTOi  | Convert Double Precision to Integer                    | 8      |
| FxTOi  | Convert Extended Precision to Integer                  | #      |
| FsTOd  | Convert Single Precision to Double Precision           | 8      |
| FsTOx  | Convert Single Precision to Extended Precision         | #      |
| FdTOs  | Convert Double Precision to Single Precision           | 8      |
| FdTOx  | Convert Double Precision to Extended Precision         | #      |
| FxTOs  | Convert Extended Precision to Single Precision         | #      |
| FxTOd  | Convert Extended Precision to Double Precision         | #      |
| FMOVs  | Move Single Precision                                  | 8      |
| FNEGs  | Negate Single Precision                                | 8      |
| FABSS  | Absolute Value Single Precision                        | 8      |
| FSQRTs | Square Root Single Precision                           | 15     |
| FSQRTd | Square Root Double Precision                           | 22     |
| FSQRTx | Square Root Extended Precision                         | #      |
| FADDs  | Add Single Precision                                   | 8      |
| FADDd  | Add Double Precision                                   | 8      |
| FADDx  | Add Extended Precision                                 | #      |
| FSUBs  | Subtract Single Precision                              | 8      |
| FSUBd  | Subtract Double Precision                              | 8      |
| FSUBx  | Subtract Extended Precision                            | #      |
| FMULs  | Multiply Single Precision                              | 8      |
| FMULd  | Multiply Double Precision                              | 9      |
| FMULx  | Multiply Extended Precision                            | #      |
| FDIVs  | Divide Single Precision                                | 13     |
| FDIVd  | Divide Double Precision                                | 18     |
| FDIVx  | Divide Extended Precision                              | #      |
| FCMPs  | Compare Single Precision                               | 8      |
| FCMPd  | Compare Double Precision                               | 8      |
| FCMPx  | Compare Extended Precision                             | #      |
| FCMPEs | Compare Single Precision with Exception if Unordered   | 8      |
| FCMPED | Compare Double Precision with Exception if Unordered   | 8      |
| FCMPEx | Compare Extended Precision with Exception if Unordered | #      |

\* privileged instruction

# currently supported via software emulation only

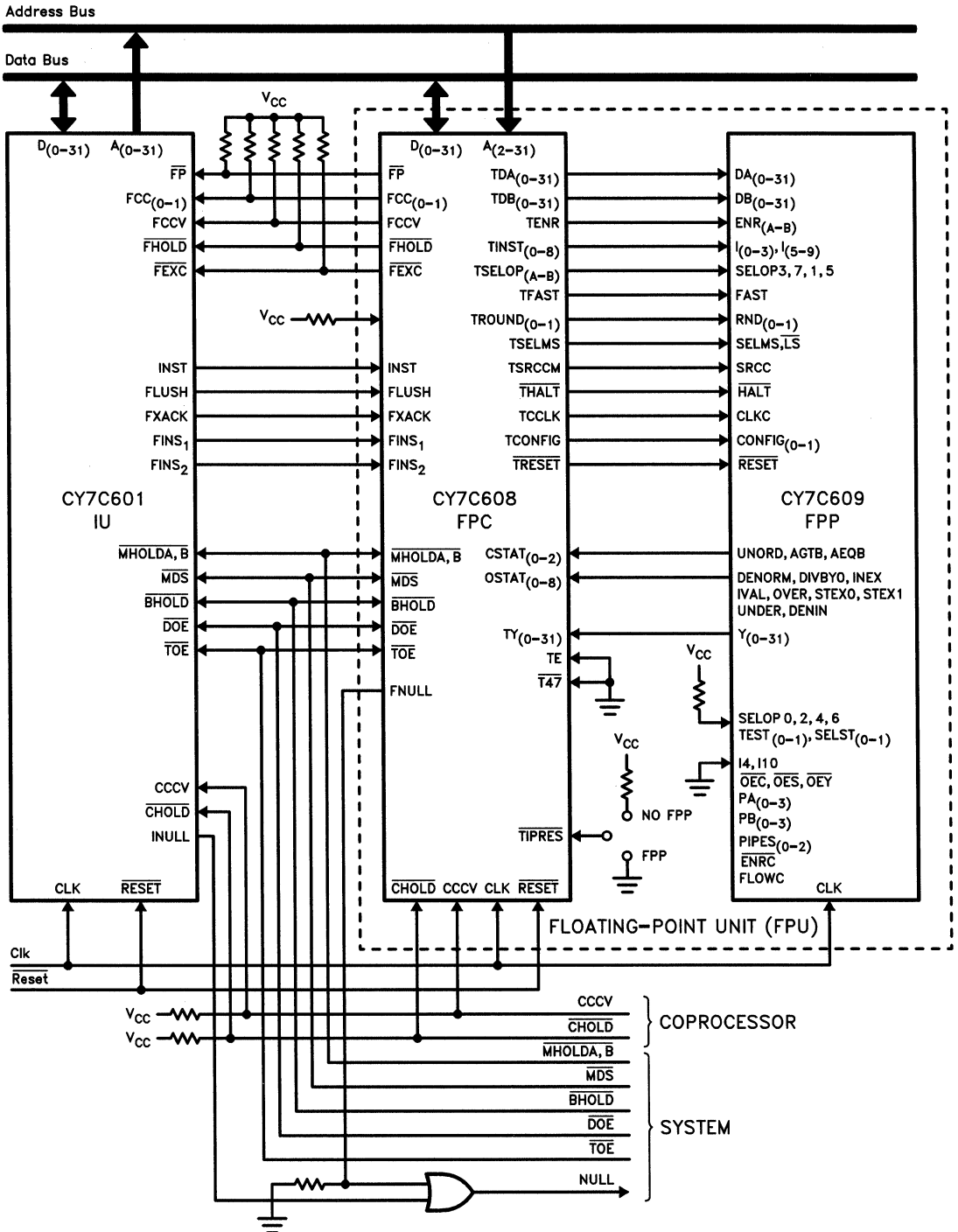


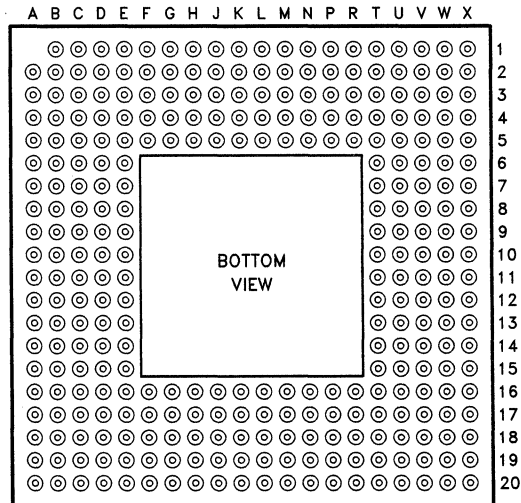
Figure 1. Floating-Point Controller System Connections

**Table 2. Pin Table**

| Pin Name        | Pin Number | Pin Name           | Pin Number | Pin Name            | Pin Number |
|-----------------|------------|--------------------|------------|---------------------|------------|
| A <sub>2</sub>  | X13        | D <sub>27</sub>    | D10        | TIN                 | D18        |
| A <sub>3</sub>  | X14        | D <sub>28</sub>    | C10        | TIPRES              | X6         |
| A <sub>4</sub>  | X15        | D <sub>29</sub>    | C9         | TOUT                | D19        |
| A <sub>5</sub>  | W15        | D <sub>30</sub>    | D9         | TRESET              | T10        |
| A <sub>6</sub>  | X16        | D <sub>31</sub>    | C8         | TROUND <sub>0</sub> | E9         |
| A <sub>7</sub>  | W16        | MHOLDA             | J17        | TROUND <sub>1</sub> | E8         |
| A <sub>8</sub>  | V16        | MHOLDB             | J18        | TSELMS              | E10        |
| A <sub>9</sub>  | W17        | BHOLD              | H18        | TSELOPA             | N5         |
| A <sub>10</sub> | U16        | DOE                | E19        | TSELOPB             | N4         |
| A <sub>11</sub> | V17        | MDS                | N18        | TSRCCM              | E11        |
| A <sub>12</sub> | W18        | FNULL              | L16        | TY <sub>0</sub>     | B18        |
| A <sub>13</sub> | R17        | RESET              | G20        | TY <sub>1</sub>     | B17        |
| A <sub>14</sub> | U18        | CLK                | U10        | TY <sub>2</sub>     | A17        |
| A <sub>15</sub> | P16        | FP                 | F20        | TY <sub>3</sub>     | B16        |
| A <sub>16</sub> | T17        | FCC <sub>0</sub>   | L17        | TY <sub>4</sub>     | A16        |
| A <sub>17</sub> | P17        | FCC <sub>1</sub>   | L18        | TY <sub>5</sub>     | A15        |
| A <sub>18</sub> | U19        | FCCV               | M17        | TY <sub>6</sub>     | A14        |
| A <sub>19</sub> | T18        | FHOLD              | N16        | TY <sub>7</sub>     | B13        |
| A <sub>20</sub> | U20        | FEXC               | M16        | TY <sub>8</sub>     | B12        |
| A <sub>21</sub> | T19        | INST               | N17        | TY <sub>9</sub>     | B11        |
| A <sub>22</sub> | R18        | FLUSH              | M18        | TY <sub>10</sub>    | B10        |
| A <sub>23</sub> | T20        | FINS <sub>1</sub>  | G19        | TY <sub>11</sub>    | B9         |
| A <sub>24</sub> | R19        | FINS <sub>2</sub>  | H19        | TY <sub>12</sub>    | A8         |
| A <sub>25</sub> | P18        | FXACK              | L19        | TY <sub>13</sub>    | B8         |
| A <sub>26</sub> | R20        | CCCV               | F19        | TY <sub>14</sub>    | A7         |
| A <sub>27</sub> | P19        | CHOLD              | K18        | TY <sub>15</sub>    | D8         |
| A <sub>28</sub> | P20        | CHAIN              | X5         | TY <sub>16</sub>    | B7         |
| A <sub>29</sub> | N19        | TOE                | E20        | TY <sub>17</sub>    | C7         |
| A <sub>30</sub> | N20        | CSTAT <sub>0</sub> | R1         | TY <sub>18</sub>    | A6         |
| A <sub>31</sub> | M19        | CSTAT <sub>1</sub> | U1         | TY <sub>19</sub>    | D7         |
| D <sub>0</sub>  | H17        | CSTAT <sub>2</sub> | T1         | TY <sub>20</sub>    | B6         |
| D <sub>1</sub>  | G18        | OSTAT <sub>0</sub> | D2         | TY <sub>21</sub>    | C6         |
| D <sub>2</sub>  | H16        | OSTAT <sub>1</sub> | E2         | TY <sub>22</sub>    | A5         |
| D <sub>3</sub>  | G17        | OSTAT <sub>2</sub> | F1         | TY <sub>23</sub>    | B5         |
| D <sub>4</sub>  | F18        | OSTAT <sub>3</sub> | D3         | TY <sub>24</sub>    | C5         |
| D <sub>5</sub>  | E18        | OSTAT <sub>4</sub> | E1         | TY <sub>25</sub>    | B4         |
| D <sub>6</sub>  | G16        | OSTAT <sub>5</sub> | G1         | TY <sub>26</sub>    | D5         |
| D <sub>7</sub>  | E17        | OSTAT <sub>6</sub> | H1         | TY <sub>27</sub>    | D6         |
| D <sub>8</sub>  | F17        | OSTAT <sub>7</sub> | G2         | TY <sub>28</sub>    | C4         |
| D <sub>9</sub>  | F16        | OSTAT <sub>8</sub> | F2         | TY <sub>29</sub>    | E4         |
| D <sub>10</sub> | D15        | TINST <sub>0</sub> | E7         | TY <sub>30</sub>    | C2         |
| D <sub>11</sub> | E14        | TINST <sub>1</sub> | E6         | TY <sub>31</sub>    | E3         |
| D <sub>12</sub> | C17        | TINST <sub>2</sub> | F4         | TDA <sub>0</sub>    | V5         |
| D <sub>13</sub> | D14        | TINST <sub>3</sub> | G5         | TDA <sub>1</sub>    | W4         |
| D <sub>14</sub> | D16        | TINST <sub>4</sub> | F3         | TDA <sub>2</sub>    | U7         |
| D <sub>15</sub> | C16        | TINST <sub>5</sub> | G3         | TDA <sub>3</sub>    | U5         |
| D <sub>16</sub> | C15        | TINST <sub>6</sub> | H3         | TDA <sub>4</sub>    | T7         |
| D <sub>17</sub> | B15        | TINST <sub>7</sub> | H5         | TDA <sub>5</sub>    | V4         |
| D <sub>18</sub> | E13        | TINST <sub>8</sub> | H4         | TDA <sub>6</sub>    | U6         |
| D <sub>19</sub> | C14        | T <sub>47</sub>    | X7         | TDA <sub>7</sub>    | R4         |
| D <sub>20</sub> | D13        | TCCLK              | T4         | TDA <sub>8</sub>    | U3         |
| D <sub>21</sub> | B14        | TCONFIG            | R5         | TDA <sub>9</sub>    | U2         |
| D <sub>22</sub> | D12        | TE                 | D20        | TDA <sub>10</sub>   | T3         |
| D <sub>23</sub> | C13        | TENR               | P5         | TDA <sub>11</sub>   | T2         |
| D <sub>24</sub> | C12        | TFAST              | H2         | TDA <sub>12</sub>   | R3         |
| D <sub>25</sub> | C11        | THALT              | T11        | TDA <sub>13</sub>   | P4         |
| D <sub>26</sub> | D11        |                    |            | TDA <sub>14</sub>   | R2         |

**Table 2. Pin Table (Continued)**

| Pin Name          | Pin Number | Pin Name          | Pin Number  | Pin Name        | Pin Number      |             |
|-------------------|------------|-------------------|-------------|-----------------|-----------------|-------------|
| TDA <sub>15</sub> | P3         | TDB <sub>9</sub>  | U12         | V <sub>SS</sub> | J1 N1 X1        |             |
| TDA <sub>16</sub> | M5         | TDB <sub>10</sub> | V12         |                 | J16 P1 X11      |             |
| TDA <sub>17</sub> | P2         | TDB <sub>11</sub> | V13         |                 | K16 T12 X17     |             |
| TDA <sub>18</sub> | M4         | TDB <sub>12</sub> | V11         |                 | K20 V1 X19      |             |
| TDA <sub>19</sub> | N3         | TDB <sub>13</sub> | W13         |                 | L1 V2 X3        |             |
| TDA <sub>20</sub> | M3         | TDB <sub>14</sub> | U11         |                 | M20 W20 X9      |             |
| TDA <sub>21</sub> | L3         | TDB <sub>15</sub> | W12         |                 | V <sub>CC</sub> | A11 D1 X12  |
| TDA <sub>22</sub> | N2         | TDB <sub>16</sub> | W11         |                 |                 | A13 J20 X18 |
| TDA <sub>23</sub> | L5         | TDB <sub>17</sub> | W10         |                 |                 | A18 K1 X2   |
| TDA <sub>24</sub> | M2         | TDB <sub>18</sub> | V10         |                 |                 | A20 L20 X20 |
| TDA <sub>25</sub> | L4         | TDB <sub>19</sub> | W9          | A3 M1 X4        |                 |             |
| TDA <sub>26</sub> | K5         | TDB <sub>20</sub> | V9          | A9 V20 X8       |                 |             |
| TDA <sub>27</sub> | J2         | TDB <sub>21</sub> | W8          | B1 W1           |                 |             |
| TDA <sub>28</sub> | K3         | TDB <sub>22</sub> | U9          | C20 X10         |                 |             |
| TDA <sub>29</sub> | J3         | TDB <sub>23</sub> | T9          | NO<br>CONNECT   |                 | B19 F5 T6   |
| TDA <sub>30</sub> | J4         | TDB <sub>24</sub> | V8          |                 |                 | B2 G4 U17   |
| TDA <sub>31</sub> | J5         | TDB <sub>25</sub> | U8          |                 | B3 J19 U4       |             |
| TDB <sub>0</sub>  | T15        | TDB <sub>26</sub> | W7          |                 | C18 K17 V18     |             |
| TDB <sub>1</sub>  | U15        | TDB <sub>27</sub> | T8          |                 | C19 K19 V19     |             |
| TDB <sub>2</sub>  | T14        | TDB <sub>28</sub> | V7          |                 | C3 K2 V3        |             |
| TDB <sub>3</sub>  | V15        | TDB <sub>29</sub> | W6          |                 | D17 K4 W19      |             |
| TDB <sub>4</sub>  | U14        | TDB <sub>30</sub> | V6          |                 | D4 L2 W2        |             |
| TDB <sub>5</sub>  | T13        | TDB <sub>31</sub> | W5          |                 | E15 R16 W3      |             |
| TDB <sub>6</sub>  | U13        | V <sub>SS</sub>   | A10 A2 C1   |                 | E16 T16         |             |
| TDB <sub>7</sub>  | V14        |                   | A12 A4 E12  | E5 T5           |                 |             |
| TDB <sub>8</sub>  | W14        |                   | A19 B20 H20 |                 |                 |             |



0131-4

**Ordering Information**

| Clock Frequency (MHz) | Ordering Code | Package Type | Operating Range |
|-----------------------|---------------|--------------|-----------------|
| 33                    | CY7C608-33GC  | G300         | Commercial      |
| 25                    | CY7C608-25GC  | G300         | Commercial      |



**Features**

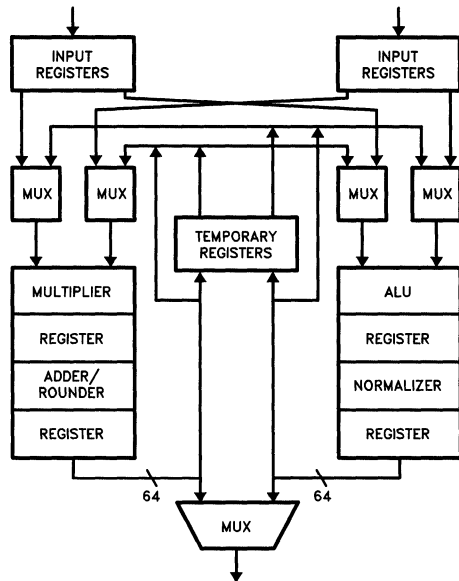
- Provides high performance 64-bit floating-point arithmetic for CY7C601 RISC integer unit
- Provides SPARC™ compatible floating-point arithmetic
- Very high performance
  - Fully pipelined
  - 30 ns cycle
  - Instructions launched in single cycle
  - 4.2 million double precision linpack floating-point operations per second
- High performance coprocessor interface
  - Concurrent execution of integer and floating-point instructions
  - Hardware interlocks synchronize integer and floating-point operations
- Meets IEEE standard 754-1985 for single and double precision formats
- 1 micron CMOS technology
- 208 pin grid array package

**Overview**

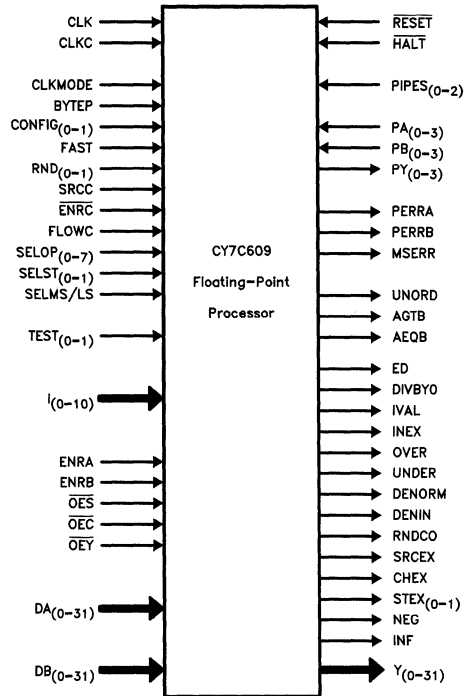
The CY7C609 is a high-speed double precision Floating-Point Processor (FPP) which when used in conjunction with the CY7C608 Floating-Point Controller (FPC) provides high performance SPARC compatible single and double precision floating-point arithmetic. The FPP performs add, subtract, multiply, divide, square root, compare, and convert; while the CY7C608 FPC performs register to register move instructions, floating-point loads and stores, floating-point state register, and floating-point queue store instructions.

6

**Block Diagram**



**Signal Diagram**



**Selection Guide**

|                                |            | 7C609-33 | 7C609-25 |
|--------------------------------|------------|----------|----------|
| Maximum Operating Current (mA) | Commercial | 600      | 550      |

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Document #: 38-00101



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# Section Contents

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## Modules

## Page Number

|                                  |     |
|----------------------------------|-----|
| Custom Module Capabilities ..... | 7-1 |
|----------------------------------|-----|

1. The first part of the document discusses the importance of maintaining accurate records of all transactions and activities. It emphasizes that this is crucial for ensuring transparency and accountability in the organization's operations.

2. The second part of the document outlines the various methods and tools used to collect and analyze data. It highlights the need for consistent and reliable data collection processes to support informed decision-making.

3. The third part of the document focuses on the role of technology in data management and analysis. It discusses how modern software solutions can streamline data collection, storage, and reporting, thereby improving efficiency and accuracy.

4. The fourth part of the document addresses the challenges associated with data management, such as data quality, security, and privacy. It provides strategies to mitigate these risks and ensure that data is used responsibly and ethically.

5. The fifth part of the document concludes by summarizing the key findings and recommendations. It stresses the importance of ongoing monitoring and evaluation to ensure that data management practices remain effective and up-to-date.



## Custom Module Capabilities

Cypress' Multichip Products group is a leading supplier of custom memory and/or logic modules. This turnkey capability provides Cypress customers with a fast, low-risk solution for designs requiring the ultimate in system performance and density. Detailed information on our standard modules can be found in the Static RAM section of this book (Section 2).

### Custom Capabilities

Cypress' Multichip Products Division is currently supporting custom modules with the following technical requirements:

|                    |                                      |
|--------------------|--------------------------------------|
| Substrate Type:    | Ceramic, Epoxy Laminate              |
| Comp. Packaging:   | LCC, SOJ, SOIC, PLCC                 |
| Pin Configuration: | DIP, VDIP(DSIP), ZIP, SIP, QUIP, PGA |
| Data Word Width:   | Up to 72 Bits                        |
| Pin Count:         | Up to 200 Pins                       |
| Access Time:       | 12 ns and up                         |

As 1989 progresses, we will be introducing new technologies which will extend each of these capabilities.

Multichip modules are typically SRAM based. However, other types of components can be used in addition to or instead of SRAMs—Logic, PLDs, EPROM, Gate Arrays, Microprocessors, etc.

### Advantages of Custom Modules

Custom modules provide the memory system designer with the ultimate in flexibility and performance. For example, using a custom module it is very straightforward to implement unusual memory word widths—a capability that becomes critical in high speed applications such as digital signal processing and RISC-based systems.

Custom modules are built using fully tested components, and are rigorously tested before they are shipped. This testing redundancy saves time and effort during system testing and provides an added degree of reliability.

### Performance and Density Improvements

Using modules, far greater memory densities can be achieved than even the most advanced surface mount technologies. This density can be attained for several reasons:

- **Orientation.** Modules substrates can be oriented vertically, with devices mounted on both sides.

- **Routing Efficiency.** Due to compact module size, more efficient routing techniques can be used. These include tighter line spacing, blind and buried vias, and selective manual routing.
- **Pin Reduction.** The reduced number of device pins which results from the use of modules allows the memory system itself to be routed more efficiently.
- **Ceramic Substrates.** Ceramic is the highest density interconnect medium for surface mount packages. Thus, modules provide large density improvements, while satisfying hermeticity requirements if desired.

Module usage also improves memory system performance. These performance advantages include the following:

- Interconnect capacitance is reduced by approximately 50%.
- Crosstalk Characteristics are substantially improved.
- Number of pins is minimized.
- Ceramic may be used to improve thermal characteristics.

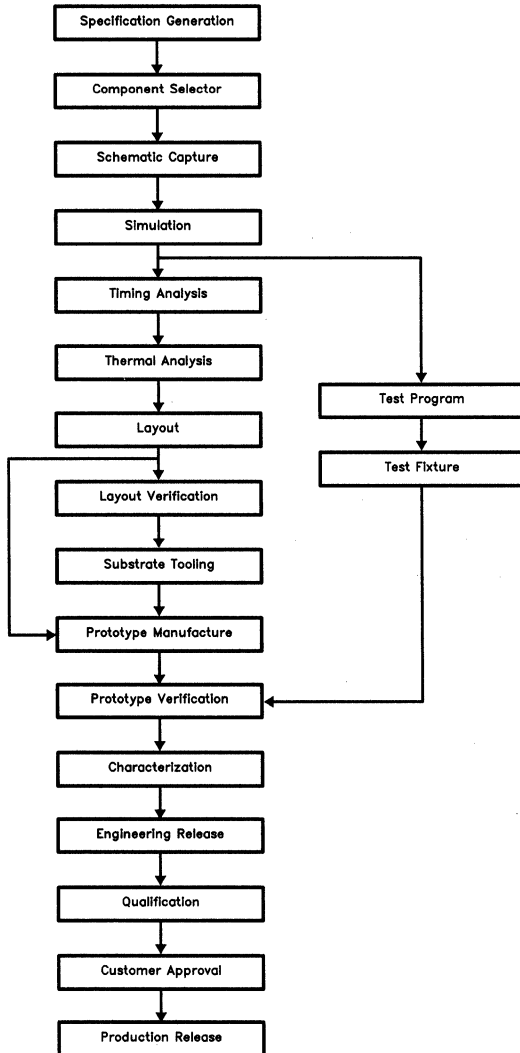
### Custom Module Flow

Multichip's focus is on providing turnkey memory modules. *Figure 1* illustrates the tasks performed during the development of the module.

Module development commences with the generation of a detailed Objective Specification. The module is designed to this specification, and once in production it will be guaranteed to perform as indicated in the Objective Spec.

Components are selected while the specification is being generated. In many cases, the spec is designed such that multiple sources of components can be utilized. Once the spec is complete and the components are selected, a schematic for the module is generated. The netlist from the schematic is used to drive the circuit simulator.

During simulation, several types of analysis are performed. A functional simulation is used to ensure that the module's logic is designed properly. Timing simulation is run to verify that the module will function when subject to the worst case timing delays of the components. Finally, thermal analysis may be performed to determine the thermal characteristic of the module.

**Custom Module Flow (Continued)**

**Figure 1. Custom Module Flow**

0168-1

The layout of the module is also netlist driven. An auto-router may or may not be used, depending on the complexity and density of the module. Design rule checks are run to ensure that the layout does not violate any electrical or mechanical design rules. Finally, the layout output is used to generate the module substrate.

The layout output is also used to drive the pick and place equipment. This ensures consistency between design and manufacturing. While the module prototypes are being assembled, the test program is generated and the test fixture is constructed. Test program generation is largely automated, using as inputs the simulation outputs and pre-defined test program subroutines for common configurations.

Once prototypes have been generated, the standard release procedure is initiated. This procedure includes steps such as bench testing, module characterization and qualification, and fine tuning of the test program. Following customer approval of the module, it is released to production.

### Future Technologies

Cypress is committed to providing the most advanced custom module capability in the industry. This commitment includes more than simply modularizing the most advanced Cypress memory products. As part of our commitment to redefining the leading edge in module technology, we are pioneering the use of several advanced technologies:

- ECL and BiCMOS products of Cypress' Aspen Semiconductor subsidiary.
- Advanced packaging techniques such as Tape Automated Bonding (TAB).
- Advanced module package formats, such as ZIP packaging and sub-one hundred mil pin spacing.
- Application of design automation techniques to module products.

### Quoting Information

In order to prepare a quotation or proposal, we need as much as possible of the following information:

- Circuit Schematic
- Functional Description
- Mechanical dimensions required
- Speed and power requirements
- Prototype and production deadlines
- Production Quantity estimates
- An Engineering contact to answer questions

Once the above information is received, a budgetary quotation will typically be provided within one to two weeks.

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# Section Contents

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## ECL

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| CY100E301 | Combinatorial ECL 16P8 PLD..... | 8-1  |
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| CY100E302 | Combinatorial ECL 16P4 PLD..... | 8-6  |
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| CY100E474 | 1024 x 4 ECL Static RAM .....   | 8-16 |







## Combinatorial ECL 16P8 Programmable Logic Device

### Features

- Standard 16P8 pinout and architecture
  - 16 inputs, 8 outputs
  - User programmable output polarity
- Ultra high speed/standard power
  - $t_{PD} = 3 \text{ ns}$  (max)
  - $I_{EE} = 240 \text{ mA}$  (max)
- Low power version
  - $t_{PD} = 6 \text{ ns}$  (max)
  - $I_{EE} = 170 \text{ mA}$  (max)
- Both 10KH and 100K I/O compatible versions available
- Enhanced test features
  - Additional test input terms
  - Additional test product terms
- Security fuse

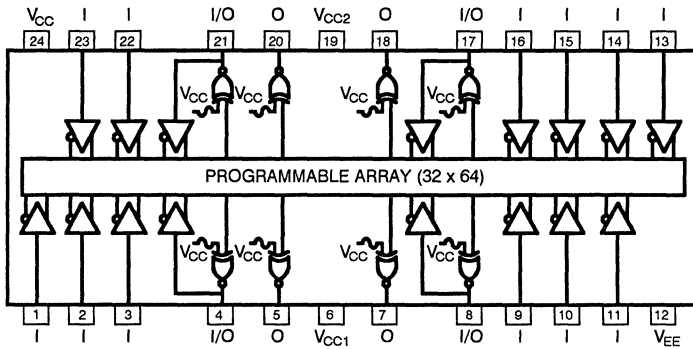
### Functional Description

Cypress Semiconductor's PLD family offers the user the highest level of performance in ECL Programmable Logic Devices. These PLDs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor, using an advanced Bipolar process incorporating proven Ti-W fuses.

The CY10E301 is 10KH compatible and the CY100E301 is 100K compatible. These PLDs implement the familiar sum-of-products logic functions by selectively programming cell elements to configure the AND gates by disconnecting either the true or complement input term. If all inputs are disconnected from an AND gate, then a logical true will exist at the output of this AND gate. An output polarity fuse is also provided to allow an

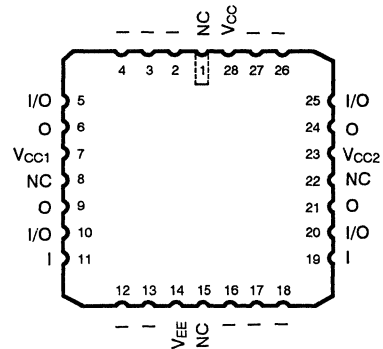
active LOW to occur if this fuse is blown. A security feature provides the user protection for the implementation of proprietary logic. When invoked by blowing the security fuse, the contents of the array cannot be accessed in the verify mode. The CY10E301 and CY100E301 can be programmed using Cypress' QuickPro or other industry standard programming equipment. Programming support information can be obtained from local Cypress sales offices.

### Logic Symbol and Pinout



C301-1

### LCC and PLCC Pinout



C301-2

### Selection Guide

|  |            | 10E301-3<br>100E301-3 | 10E301-4<br>100E301-4 | 10E301-6 | 10E301L-6<br>100E301L-6 |
|--|------------|-----------------------|-----------------------|----------|-------------------------|
| Maximum Input to Output Propagation Delay (ns) |            | 3                     | 4                     | 6        | 6                       |
| $I_{EE}$ (mA)                                  | Commercial | -240                  | -240                  |          | -170                    |
|  | Military   |                       |                       | -240     |                         |

## Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

|   |                   |
|---|-------------------|
| Storage Temperature .....                                   | -65°C to +150°C   |
| Ambient Temperature with Power Applied <sup>[1]</sup> ..... | -55°C to +125°C   |
| Supply Voltage $V_{EE}$ to $V_{CC}$ .....                   | -7.0 V to +0.5V   |
| Input Voltage .....   | $V_{EE}$ to +0.5V |
| Output Current .....  | -50 mA            |

## Operating Range Referenced to $V_{CC}$ at ground

| Range                      | I/O  | Temperature          | $V_{EE}$     |
|----------------------------|------|----------------------|--------------|
| Commercial (Standard, "L") | 10KH | 0°C to +75°C Ambient | -5.2V ± 5%   |
| Commercial (Standard, "L") | 100K | 0°C to +85°C Ambient | -4.5V ± 0.3V |
| Military                   | 10KH | -55°C to +125°C Case | -5.2V ± 5%   |

## Electrical Characteristics Over Operating Range <sup>[2]</sup>

| Parameters | Description                                  | Test Conditions   | Temperature <sup>[1]</sup>  | 10E301                           |       | 100E301 |               | Units |
|------------|--|---|---|----------------------------------|-------|---------|---------------|-------|
|            |  |   |   | Min.                             | Max.  | Min.    | Max.          |       |
| $V_{OH}$   | Output HIGH Voltage                          | 10KH, $R_L = 50 \Omega$ to -2V<br>$V_{IN} = V_{IH}$ Min. or $V_{IL}$ Max. | $T_C = -55^\circ\text{C}$   | -1110                            | -930  |         |               | mV    |
|            |  |   | $T_A = 0^\circ\text{C}$   | -1020                            | -840  |         |               | mV    |
|            |  |   | $T_A = +25^\circ\text{C}$   | -980                             | -810  |         |               | mV    |
|            |  |   | $T_A = +75^\circ\text{C}$   | -920                             | -735  |         |               | mV    |
|            |  |   | $T_C = +125^\circ\text{C}$  | -830                             | -660  |         |               | mV    |
|            |  |   | 100K, $R_L = 50 \Omega$ to -2V<br>$V_{IN} = V_{IH}$ Min. or $V_{IL}$ Max. | $T_A = 0^\circ\text{C}$ to +85°C |       |         | -1025         | -880  |
| $V_{OL}$   | Output LOW Voltage                           | 10KH, $R_L = 50 \Omega$ to -2V<br>$V_{IN} = V_{IH}$ Min. or $V_{IL}$ Max. | $T_C = -55^\circ\text{C}$   | -1950                            | -1630 |         |               | mV    |
|            |  |   | $T_A = 0^\circ\text{C}$   | -1950                            | -1630 |         |               | mV    |
|            |  |   | $T_A = +25^\circ\text{C}$   | -1950                            | -1630 |         |               | mV    |
|            |  |   | $T_A = +75^\circ\text{C}$   | -1950                            | -1600 |         |               | mV    |
|            |  |   | $T_C = +125^\circ\text{C}$  | -1950                            | -1570 |         |               | mV    |
|            |  |   | 100K, $R_L = 50 \Omega$ to -2V<br>$V_{IN} = V_{IH}$ Min. or $V_{IL}$ Max. | $T_A = 0^\circ\text{C}$ to +85°C |       |         | -1810         | -1620 |
| $V_{IH}$   | Input HIGH Voltage                           | 10KH  | $T_C = -55^\circ\text{C}$   | -1250                            | -930  |         |               | mV    |
|            |  |   | $T_A = 0^\circ\text{C}$   | -1170                            | -840  |         |               | mV    |
|            |  |   | $T_A = +25^\circ\text{C}$   | -1130                            | -810  |         |               | mV    |
|            |  |   | $T_A = +75^\circ\text{C}$   | -1070                            | -735  |         |               | mV    |
|            |  |   | $T_C = +125^\circ\text{C}$  | -1000                            | -660  |         |               | mV    |
|            |  |   | 100K  | $T_A = 0^\circ\text{C}$ to +85°C |       |         | -1165         | -880  |
| $V_{IL}$   | Input LOW Voltage                            | 10KH  | $T_C = -55^\circ\text{C}$   | -1950                            | -1480 |         |               | mV    |
|            |  |   | $T_A = 0^\circ\text{C}$   | -1950                            | -1480 |         |               | mV    |
|            |  |   | $T_A = +25^\circ\text{C}$   | -1950                            | -1480 |         |               | mV    |
|            |  |   | $T_A = +75^\circ\text{C}$   | -1950                            | -1450 |         |               | mV    |
|            |  |   | $T_C = +125^\circ\text{C}$  | -1950                            | -1420 |         |               | mV    |
|            |  |   | 100K  | $T_A = 0^\circ\text{C}$ to +85°C |       |         | -1810         | -1475 |
| $I_{IH}$   | Input HIGH Current                           | $V_{IN} = V_{IH}$ Max.  |   | 220                              |       | 220     | $\mu\text{A}$ |       |
| $I_{IL}$   | Input LOW Current                            | $V_{IN} = V_{IL}$ Min. (Except I/O pins)                                  | 0.5   |                                  | 0.5   |         | $\mu\text{A}$ |       |
| $I_{EE}$   | Supply Current (All inputs and outputs open) | Commercial "L" (Low Power)  |   | -170                             |       | -170    | mA            |       |
|            |  | Commercial (Standard Power)   |   | -240                             |       | -240    | mA            |       |
|            |  | Military  |   | -240                             |       | -240    | mA            |       |

### Notes:

- Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute. Military grade is specified as case temperature.
- See AC Test Loads and Waveforms for test conditions.

### Capacitance<sup>[3]</sup>

| Parameters       | Description        | Min. | Typ. | Max. | Units |
|------------------|--------------------|------|------|------|-------|
| C <sub>IN</sub>  | Input Capacitance  |      | 4    | 10   | pF    |
| C <sub>OUT</sub> | Output Capacitance |      | 6    | 13   | pF    |

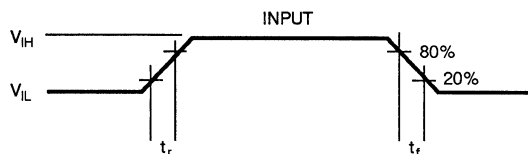
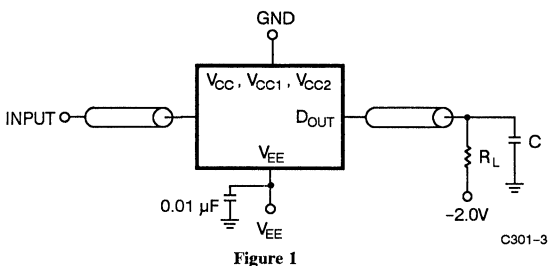
**Note:**

3. Tested initially and after any design or process changes that may affect these parameters.

### Switching Characteristics Over Operating Range<sup>[2]</sup>

| Parameters      | Description                       | 10E301-3<br>100E301-3 |      | 10E301-4<br>100E301-4 |      | 10E301L-6<br>100E301L-6 |      | Units |
|-----------------|-----------------------------------|-----------------------|------|-----------------------|------|-------------------------|------|-------|
|                 |                                   | Min.                  | Max. | Min.                  | Max. | Min.                    | Max. |       |
| t <sub>PD</sub> | Input to Output Propagation Delay |                       | 3.0  |                       | 4.0  |                         | 6.0  | ns    |
| t <sub>r</sub>  | Output Rise Time                  | 0.7                   | 1.5  | 0.7                   | 1.5  | 0.7                     | 1.5  | ns    |
| t <sub>f</sub>  | Output Fall Time                  | 0.7                   | 1.5  | 0.7                   | 1.5  | 0.7                     | 1.5  | ns    |

### AC Test Loads and Waveforms<sup>[4, 5, 6, 7, 8, 9]</sup>



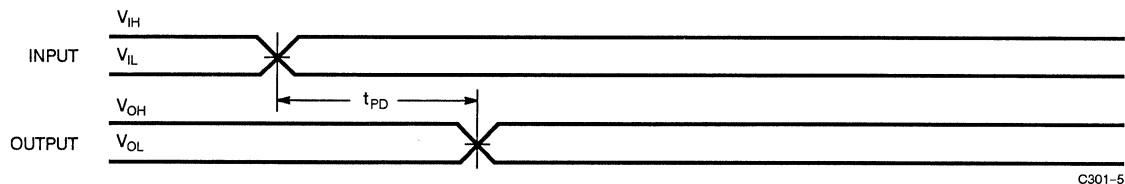
**Figure 2**

**Notes:**

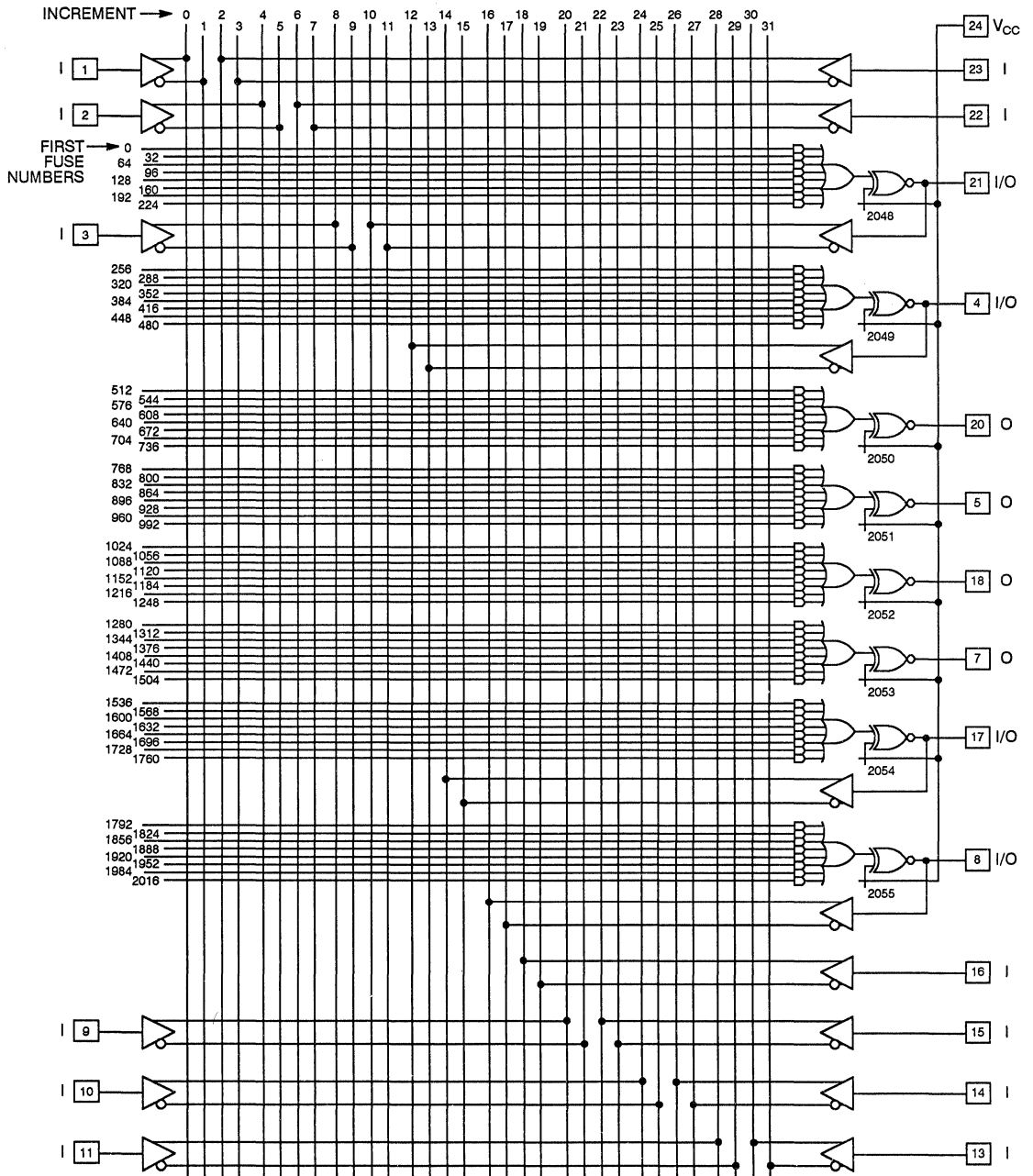
4. V<sub>IL</sub> = V<sub>IL</sub> Min., V<sub>IH</sub> = V<sub>IH</sub> Max. on 10KH version.
5. V<sub>IL</sub> = -1.7V, V<sub>IH</sub> = -0.9V on 100K version.
6. R<sub>L</sub> = 50 Ω, C < 5 pF (includes fixture and stray capacitance).
7. All coaxial cables should be 50 Ω with equal lengths. The delay of the coaxial cables should be “nulled” out of the measurement.

8. t<sub>r</sub> = t<sub>f</sub> = 0.7 ns.
9. All timing measurements are made from the 50% point of all waveforms.

### Switching Waveforms



### Functional Logic Diagram



JEDEC fuse number = first fuse number + increment

### Ordering Information

| I/O            | t <sub>PD</sub><br>(ns) | I <sub>EE</sub><br>(mA) | Ordering Code  | Package Type | Operating Range |
|----------------|-------------------------|-------------------------|----------------|--------------|-----------------|
| 10KH           | 3.0                     | 240                     | CY10E301-3DC   | D14          | Commercial      |
|                |                         |                         | CY10E301-3LC   | L64          |                 |
|                | 4.0                     | 240                     | CY10E301-4DC   | D14          | Commercial      |
|                |                         |                         | CY10E301-4LC   | L64          |                 |
|                | 6.0                     | 150                     | CY10E301L-6JC  | J64          | Commercial      |
|                |                         |                         | CY10E301L-6PC  | P13A         |                 |
|                |                         |                         | CY10E301L-6DC  | D14          |                 |
|                | 6.0                     | 240                     | CY10E301-6DMB  | D14          | Military        |
| CY10E301-6LMB  |                         |                         | L64            |              |                 |
| 100K           | 3.0                     | 240                     | CY100E301-3DC  | D14          | Commercial      |
|                |                         |                         | CY100E301-3LC  | L64          |                 |
|                | 4.0                     | 240                     | CY100E301-4DC  | D14          | Commercial      |
|                |                         |                         | CY100E301-4LC  | L64          |                 |
|                | 6.0                     | 159                     | CY100E301L-6JC | J64          | Commercial      |
|                |                         |                         | CY100E301L-6PC | P13A         |                 |
| CY100E301L-6DC |                         |                         | D14            |              |                 |

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## Combinatorial ECL 16P4 Programmable Logic Device

### Features

- Standard 16P4 pinout and architecture
  - 16 inputs, 4 outputs
  - User programmable output polarity
- Ultra high speed/standard power
  - t<sub>PD</sub> = 2.5 ns (max)
  - I<sub>EE</sub> = 220 mA (max)
- Low power version
  - t<sub>PD</sub> = 6 ns (max)
  - I<sub>EE</sub> = 170 mA (max)
- Both 10KH and 100K I/O compatible versions available
- Enhanced test features
  - Additional test input terms
  - Additional test product terms
- Security fuse

### Functional Description

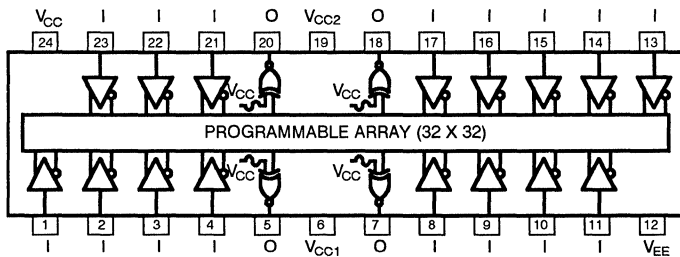
Cypress Semiconductor's PLD family offers the user the highest level of performance in ECL Programmable Logic Devices. These PLDs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor, using an advanced process incorporating proven Ti-W fuses.

The CY10E302 is 10KH compatible and the CY100E302 is 100K compatible. These PLDs implement the familiar sum-of-products logic functions by selectively programming cell elements to configure the AND gates by disconnecting either the true or complement input term. If all inputs are disconnected from an AND gate, then a logical true will exist at the output of this AND gate. An output polarity fuse is also provided to allow an

active LOW to occur if this fuse is blown. A security feature provides the user protection for the implementation of proprietary logic. When invoked by blowing the security fuse, the contents of the array cannot be accessed in the verify mode.

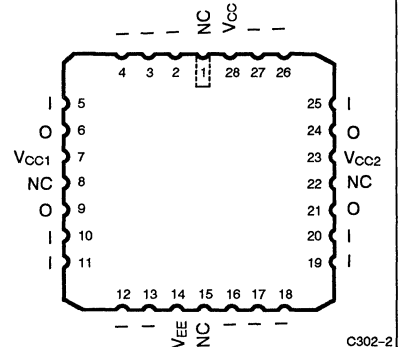
The CY10E302 and CY100E302 can be programmed using Cypress' QuickPro or other industry standard programming equipment. Programming support information can be obtained from local Cypress Semiconductor sales offices.

### Logic Symbol and Pinout



C302-1

### LCC and PLCC Pinout



C302-2

### Selection Guide

|  | 10E302-2.5<br>100E302-2.5 | 10E302-4<br>100E302-4 | 10E302-6 | 10E302L-6<br>100E302L-6 |
|--|---------------------------|-----------------------|----------|-------------------------|
| Maximum Input to Output Propagation Delay (ns) | 2.5                       | 4                     | 6        | 6                       |
| I <sub>EE</sub> (mA)                           | Commercial                | -220                  |          | -170                    |
|  | Military                  |                       | -220     |                         |

### Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied <sup>[1]</sup> ..... -55°C to +125°C  
 Supply Voltage V<sub>EE</sub> to V<sub>CC</sub> ..... -7.0 V to +0.5V  
 Input Voltage ..... V<sub>EE</sub> to +0.5V  
 Output Current ..... -50 mA

### Operating Range Referenced to V<sub>CC</sub> at ground

| Range                      | I/O  | Temperature          | V <sub>EE</sub> |
|----------------------------|------|----------------------|-----------------|
| Commercial (Standard, "L") | 10KH | 0°C to +75°C Ambient | -5.2V ± 5%      |
| Commercial (Standard, "L") | 100K | 0°C to +85°C Ambient | -4.5V ± 0.3V    |
| Military                   | 10KH | -55°C to +125°C Case | -5.2V ± 5%      |

### Electrical Characteristics Over Operating Range <sup>[2]</sup>

| Parameters      | Description                                     | Test Conditions  | Temperature <sup>[1]</sup>   | 10E302 |       | 100E302 |       | Units |
|-----------------|---|--|------------------------------|--------|-------|---------|-------|-------|
|                 |   |  |                              | Min.   | Max.  | Min.    | Max.  |       |
| V <sub>OH</sub> | Output HIGH Voltage                             | 10KH, R <sub>L</sub> = 50 Ω to -2V<br>V <sub>IN</sub> = V <sub>IH</sub> Min. or V <sub>IL</sub> Max. | T <sub>C</sub> = -55°C       | -1110  | -930  |         |       | mV    |
|                 |   |  | T <sub>A</sub> = 0°C         | -1020  | -840  |         |       | mV    |
|                 |   |  | T <sub>A</sub> = +25°C       | -980   | -810  |         |       | mV    |
|                 |   |  | T <sub>A</sub> = +75°C       | -920   | -735  |         |       | mV    |
|                 |   |  | T <sub>C</sub> = +125°C      | -830   | -660  |         |       | mV    |
|                 |   | 100K, R <sub>L</sub> = 50 Ω to -2V<br>V <sub>IN</sub> = V <sub>IH</sub> Min. or V <sub>IL</sub> Max. | T <sub>A</sub> = 0°C to 85°C |        |       | -1025   | -880  | mV    |
| V <sub>OL</sub> | Output LOW Voltage                              | 10KH, R <sub>L</sub> = 50 Ω to -2V<br>V <sub>IN</sub> = V <sub>IH</sub> Min. or V <sub>IL</sub> Max. | T <sub>C</sub> = -55°C       | -1950  | -1630 |         |       | mV    |
|                 |   |  | T <sub>A</sub> = 0°C         | -1950  | -1630 |         |       | mV    |
|                 |   |  | T <sub>A</sub> = +25°C       | -1950  | -1630 |         |       | mV    |
|                 |   |  | T <sub>A</sub> = +75°C       | -1950  | -1600 |         |       | mV    |
|                 |   |  | T <sub>C</sub> = +125°C      | -1950  | -1570 |         |       | mV    |
|                 |   | 100K, R <sub>L</sub> = 50 Ω to -2V<br>V <sub>IN</sub> = V <sub>IH</sub> Min. or V <sub>IL</sub> Max. | T <sub>A</sub> = 0°C to 85°C |        |       | -1810   | -1620 | mV    |
| V <sub>IH</sub> | Input HIGH Voltage                              | 10KH   | T <sub>C</sub> = -55°C       | -1250  | -930  |         |       | mV    |
|                 |   |  | T <sub>A</sub> = 0°C         | -1170  | -840  |         |       | mV    |
|                 |   |  | T <sub>A</sub> = +25°C       | -1130  | -810  |         |       | mV    |
|                 |   |  | T <sub>A</sub> = +75°C       | -1070  | -735  |         |       | mV    |
|                 |   |  | T <sub>C</sub> = +125°C      | -1000  | -660  |         |       | mV    |
|                 |   | 100K   | T <sub>A</sub> = 0°C to 85°C |        |       | -1165   | -880  | mV    |
| V <sub>IL</sub> | Input LOW Voltage                               | 10KH   | T <sub>C</sub> = -55°C       | -1950  | -1480 |         |       | mV    |
|                 |   |  | T <sub>A</sub> = 0°C         | -1950  | -1480 |         |       | mV    |
|                 |   |  | T <sub>A</sub> = +25°C       | -1950  | -1480 |         |       | mV    |
|                 |   |  | T <sub>A</sub> = +75°C       | -1950  | -1450 |         |       | mV    |
|                 |   |  | T <sub>C</sub> = +125°C      | -1950  | -1420 |         |       | mV    |
|                 |   | 100K   | T <sub>A</sub> = 0°C to 85°C |        |       | -1810   | -1475 | mV    |
| I <sub>IH</sub> | Input HIGH Current                              | V <sub>IN</sub> = V <sub>IH</sub> Max.   |                              | 220    |       | 220     |       | μA    |
| I <sub>IL</sub> | Input LOW Current                               | V <sub>IN</sub> = V <sub>IL</sub> Min.   | 0.5                          |        | 0.5   |         |       | μA    |
| I <sub>EE</sub> | Supply Current<br>(All inputs and outputs open) | Commercial "L" (Low Power)   |                              | -170   |       | -170    |       | mA    |
|                 |   | Commercial (Standard Power)  |                              | -220   |       | -220    |       | mA    |
|                 |   | Military   |                              | -220   |       |         |       | mA    |

Notes:

- Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute. Military grade is specified as case temperature.
- See AC Test Loads and Waveforms for test conditions.



### Capacitance<sup>[3]</sup>

| Parameters | Description        | Min. | Typ. | Max. | Units |
|------------|--------------------|------|------|------|-------|
| $C_{IN}$   | Input Capacitance  |      | 4    | 10   | pF    |
| $C_{OUT}$  | Output Capacitance |      | 6    | 13   | pF    |

**Note:**

3. Tested initially and after any design or process changes that may affect these parameters.

### Switching Characteristics Over Operating Range<sup>[2]</sup>

| Parameters | Description                       | 10E302-2.5<br>100E302-2.5 |      | 10E302-4<br>100E302-4 |      | 10E302L-6<br>100E302L-6 |      | Units |
|------------|-----------------------------------|---------------------------|------|-----------------------|------|-------------------------|------|-------|
|            |                                   | Min.                      | Max. | Min.                  | Max. | Min.                    | Max. |       |
| $t_{PD}$   | Input to Output Propagation Delay |                           | 2.5  |                       | 4.0  |                         | 6.0  | ns    |
| $t_r$      | Output Rise Time                  | 0.7                       | 1.5  | 0.7                   | 1.5  | 0.7                     | 1.5  | ns    |
| $t_f$      | Output Fall Time                  | 0.7                       | 1.5  | 0.7                   | 1.5  | 0.7                     | 1.5  | ns    |

### AC Test Loads and Waveforms<sup>[4, 5, 6, 7, 8, 9]</sup>

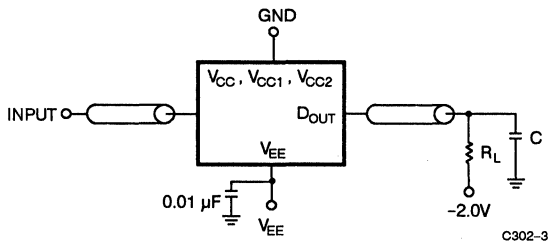


Figure 1

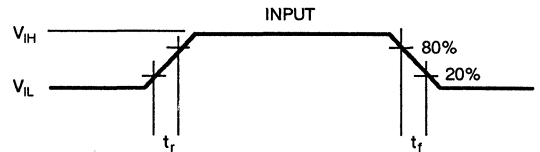
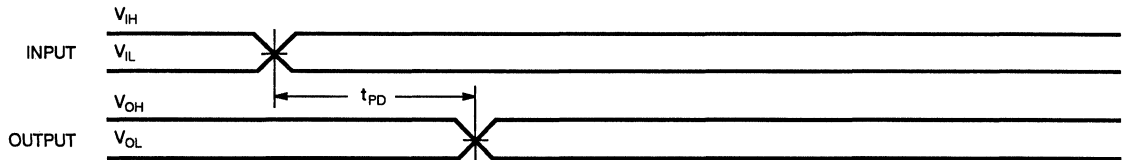


Figure 2

**Notes:**

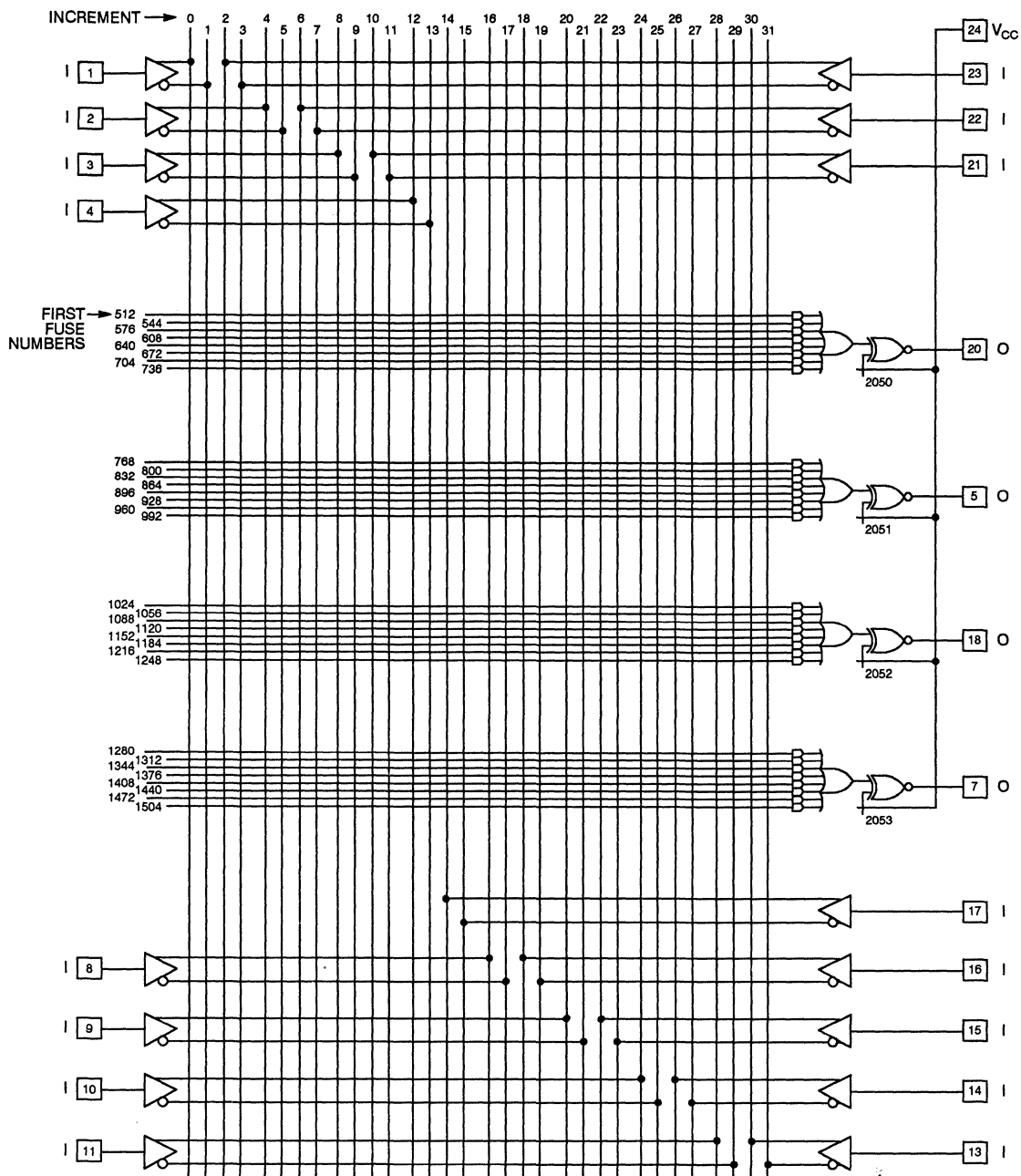
4.  $V_{IL} = V_{IL} \text{ Min.}$ ,  $V_{IH} = V_{IH} \text{ Max.}$  on 10KH version.
5.  $V_{IL} = -1.7V$ ,  $V_{IH} = -0.9V$  on 100K version.
6.  $R_L = 50 \Omega$ ,  $C < 5 \text{ pF}$  (includes fixture and stray capacitance).
7. All coaxial cables should be  $50 \Omega$  with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
8.  $t_r = t_f = 0.7 \text{ ns}$ .
9. All timing measurements are made from the 50% point of all waveforms.

### Switching Waveforms



C302-5

### Functional Logic Diagram



8

JEDEC fuse number = first fuse number + increment

C302-6

**Ordering Information**

| I/O             | t <sub>PD</sub><br>(ns) | I <sub>EE</sub><br>(mA) | Ordering Code  | Package Type    | Operating Range |
|-----------------|-------------------------|-------------------------|----------------|-----------------|-----------------|
| 10KH            | 2.5                     | 220                     | CY10E302-2.5DC | D14             | Commercial      |
|                 |                         |                         | CY10E302-2.5LC | L64             |                 |
|                 | 4.0                     | 220                     | CY10E302-4DC   | D14             | Commercial      |
|                 |                         |                         | CY10E302-4LC   | L64             |                 |
|                 | 6.0                     | 150                     | CY10E302-6JC   | J64             | Commercial      |
|                 |                         |                         | CY10E302L-6PC  | P13A            |                 |
|                 |                         |                         | CY10E302L-6DC  | D14             |                 |
|                 | 6.0                     | 220                     | CY10E302-6DMB  | D1              | Military        |
|                 |                         |                         | CY10E302-6LMB  | L64             |                 |
|                 | 100K                    | 2.5                     | 220            | CY100E302-2.5DC | D14             |
| CY100E302-2.5LC |                         |                         |                | L64             |                 |
| 4.0             |                         | 220                     | CY100E302-4DC  | D14             | Commercial      |
|                 |                         |                         | CY100E302-4LC  | L64             |                 |
| 6.0             |                         | 150                     | CY100E302L-6JC | J64             | Commercial      |
|                 |                         |                         | CY100E302L-6PC | P13A            |                 |
|                 |                         |                         | CY100E302L-6DC | D14             |                 |

Document #: 38-A-00012



256 x 4 ECL  
Static RAM

Features

- 256 x 4 bits organization
- Ultra high speed/standard power
  - $t_{AA} = 3 \text{ ns}$ ,  $t_{ABS} = 2 \text{ ns}$
  - $I_{EE} = 220 \text{ mA}$
- Low power version
  - $t_{AA} = 5 \text{ ns}$
  - $I_{EE} = 150 \text{ mA}$
- Both 10KH/10K and 100K compatible I/O versions
- On chip voltage compensation for improved noise margin

- Open emitter output for ease of memory expansion
- Industry standard pinout

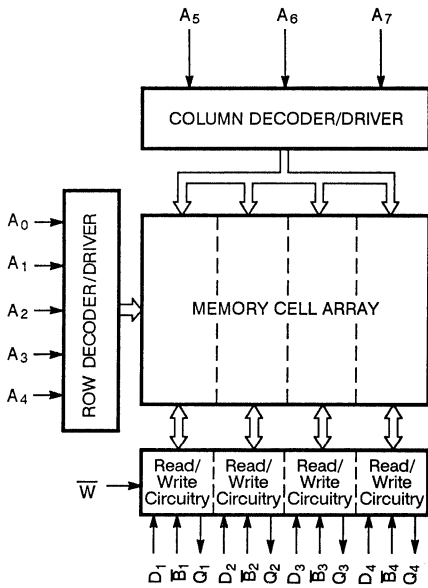
Functional Description

The Cypress CY10E422 and CY100E422 are 256 x 4 ECL RAMs designed for scratch pad, control and Buffer Storage applications. These RAMs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor. Both parts are fully decoded random access memories organized as 256 words by 4 bits. The CY10E422 is 10KH/10K

compatible. The CY100E422 is 100K compatible.

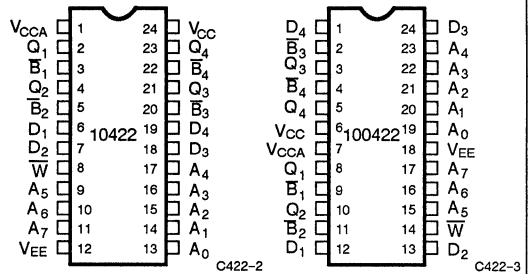
The four independent active LOW block select ( $\bar{B}$ ) inputs control memory selection and allow for memory expansion and re-configuration. The read and write operations are controlled by the state of the active LOW write enable ( $\bar{W}$ ) input. With  $\bar{W}$  and  $\bar{B}_x$  LOW, the corresponding data at  $D_x$  is written into the addressed location. To read  $\bar{W}$  is held HIGH, while  $\bar{B}$  is held LOW. Open emitter outputs allow for wired-OR connection to expand or reconfigure the memory.

Logic Block Diagram



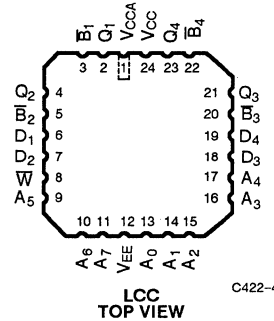
C422-1

Pin Configurations



C422-2

C422-3



C422-4

Selection Guide

|                          | 10E422-3<br>100E422-3 | 10E422-5<br>100E422-5 | 10E422-7<br>100E422-7 |
|--------------------------|-----------------------|-----------------------|-----------------------|
| Maximum Access Time (ns) | 3                     | 5                     | 7                     |
| $I_{EE}$ Max. (mA)       | Commercial            | -220                  |                       |
|                          | "L" (Low Power)       |                       | -150                  |

## Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

|  |                   |
|--|-------------------|
| Storage Temperature .....                    | -65°C to +150°C   |
| Ambient Temperature with Power Applied ..... | -55°C to +125°C   |
| Supply Voltage $V_{EE}$ to $V_{CC}$ .....    | -7.0 to +0.5V     |
| Input Voltage .....                          | $V_{EE}$ to +0.5V |
| Output Current .....                         | -50 mA            |

## Operating Range

 referenced to  $V_{CC}$ 

| Range                      | I/O      | Ambient Temperature | $V_{EE}$     |
|----------------------------|----------|---------------------|--------------|
| Commercial (Standard, "L") | 10KH/10K | 0°C to 75°C         | -5.2V ± 5%   |
| Commercial (Standard, "L") | 100K     | 0°C to 85°C         | -4.5V ± 0.3V |

## Electrical Characteristics

| Parameters | Description                                  | Test Conditions  | Temperature <sup>[1]</sup> | Min.  | Max.  | Units   |
|------------|--|--|----------------------------|-------|-------|---------|
| $V_{OH}$   | Output HIGH Voltage                          | 10E <sup>[2]</sup> $R_L = 50 \Omega$ to -2V<br>$V_{EE} = -5.2V$<br>$V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min. | $T_A = 0^\circ C$          | -1000 | -840  | mV      |
|            |  |  | $T_A = +25^\circ C$        | -960  | -810  | mV      |
|            |  |  | $T_A = +75^\circ C$        | -900  | -735  | mV      |
|            |  | 100K $R_L = 50 \Omega$ to -2V<br>$V_{EE} = -4.5V$<br>$V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min.               | $T_A = 0^\circ C$ to 85°C  | -1025 | -880  | mV      |
| $V_{OL}$   | Output LOW Voltage                           | 10E $R_L = 50 \Omega$ to -2V<br>$V_{EE} = -5.2V$<br>$V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min.                | $T_A = 0^\circ C$          | -1870 | -1665 | mV      |
|            |  |  | $T_A = +25^\circ C$        | -1850 | -1650 | mV      |
|            |  |  | $T_A = +75^\circ C$        | -1830 | -1625 | mV      |
|            |  | 100K $R_L = 50 \Omega$ to -2V<br>$V_{EE} = -4.5V$<br>$V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min.               | $T_A = 0^\circ C$ to 85°C  | -1810 | -1620 | mV      |
| $V_{IH}$   | Input HIGH Voltage                           | 10E<br>$V_{EE} = -5.2V$  | $T_A = 0^\circ C$          | -1170 | -840  | mV      |
|            |  |  | $T_A = +25^\circ C$        | -1130 | -810  | mV      |
|            |  |  | $T_A = +75^\circ C$        | -1070 | -720  | mV      |
|            |  | 100K $V_{EE} = -4.5V$  | $T_A = 0^\circ C$ to 85°C  | -1165 | -880  | mV      |
| $V_{IL}$   | Input LOW Voltage                            | 10E<br>$V_{EE} = -5.2V$  | $T_A = 0^\circ C$          | -1950 | -1480 | mV      |
|            |  |  | $T_A = +25^\circ C$        | -1950 | -1480 | mV      |
|            |  |  | $T_A = +75^\circ C$        | -1950 | -1450 | mV      |
|            |  | 100K $V_{EE} = -4.5V$  | $T_A = 0^\circ C$ to 85°C  | -1810 | -1475 | mV      |
| $I_{IH}$   | Input HIGH Current                           | $V_{IN} = V_{IH}$ Max.   |                            |       | 220   | $\mu A$ |
| $I_{IL}$   | Input LOW Current                            | $V_{IN} = V_{IL}$ Min.   | $\bar{B}$ inputs           | 0.5   | 170   | $\mu A$ |
|            |  |  | All other inputs           | -50   |       | $\mu A$ |
|            |  |  |                            |       |       |         |
| $I_{EE}$   | Supply Current (All inputs and outputs open) | Commercial "L" (Low Power)   |                            |       | -150  | mA      |
|            |  | Commercial Standard  |                            |       | -220  | mA      |

### Notes:

- Commercial grade is specified as ambient Temperature with transverse air flow greater than 500 linear feet per minute.
- 10E specifications support both 10K and 10KH compatibility.

## Capacitance<sup>[3]</sup>

| Parameters | Description        | Min. | Typ. | Max. <sup>[4]</sup> | Units |
|------------|--------------------|------|------|---------------------|-------|
| $C_{IN}$   | Input Capacitance  |      | 4    | 5                   | pF    |
| $C_{OUT}$  | Output Capacitance |      | 6    | 8                   | pF    |

### Notes:

- Tested initially and after any design or process changes that may affect these parameters.
- For all packages except Cerdip (D40) which has maximums of  $C_{IN} = 10$  pF,  $C_{OUT} = 12$  pF.

## AC Test Loads and Waveforms [5, 6, 7, 8, 9, 10]

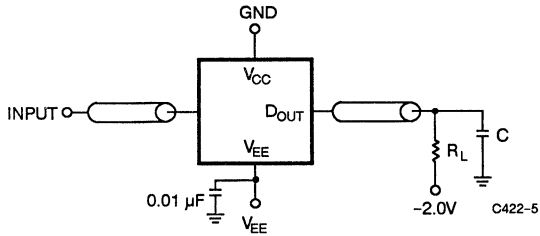


Figure 1

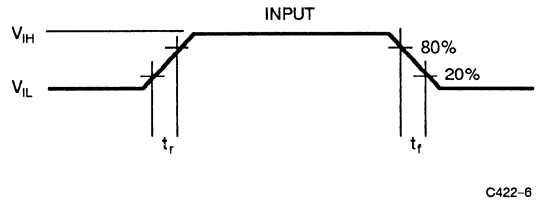


Figure 2

**Notes:**

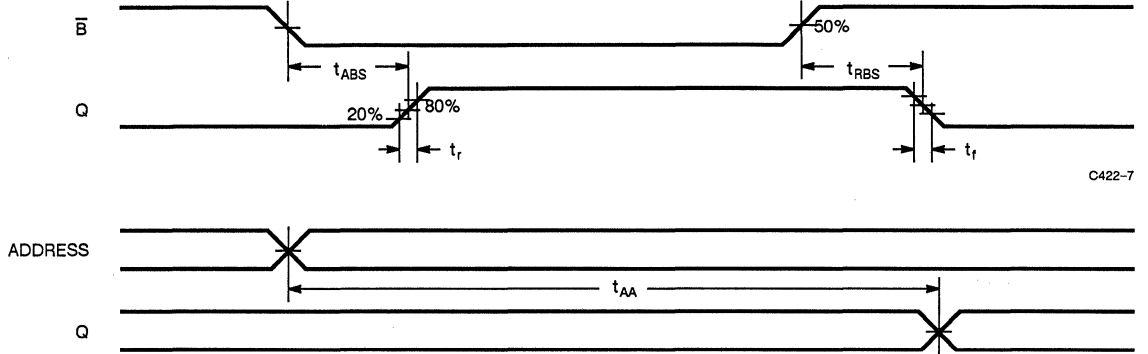
5.  $V_{IL} = V_{IL} \text{ Min.}$ ,  $V_{IH} = V_{IH} \text{ Max.}$  on 10E version.
6.  $V_{IL} = -1.7V$ ,  $V_{IH} = -0.9V$  on 100K version.
7.  $R_L = 50 \Omega$ ,  $C < 5 \text{ pF}$  (3 ns grade) or  $< 30 \text{ pF}$  (5, 7 ns grade) (includes fixture and stray capacitance).
8. All coaxial cables should be  $50 \Omega$  with equal lengths. The delay of the coaxial cables should be “nulled” out of the measurement.
9.  $t_r = t_f = 0.7 \text{ ns}$ .
10. All timing measurements are made from the 50% point of all waveforms.

## Switching Characteristics Over Operating Range

| Parameters | Description                  | 10E422-3<br>100E422-3 |      | 10E422-5<br>100E422-5 |      | 10E422-7<br>100E422-7 |      | Units |
|------------|------------------------------|-----------------------|------|-----------------------|------|-----------------------|------|-------|
|            |                              | Min.                  | Max. | Min.                  | Max. | Min.                  | Max. |       |
| $t_{ABS}$  | Block Select to Output delay |                       | 2.0  |                       | 3.0  |                       | 4.0  | ns    |
| $t_{RBS}$  | Block Select Recovery        |                       | 2.0  |                       | 3.0  |                       | 4.0  | ns    |
| $t_{AA}$   | Address Access Time          |                       | 3.0  |                       | 5.0  |                       | 7.0  | ns    |
| $t_w$      | Write Pulse Width            | 3.0                   |      | 3.0                   |      | 5.0                   |      | ns    |
| $t_{WSD}$  | Data Setup to Write          | 0.5                   |      | 1.0                   |      | 1.0                   |      | ns    |
| $t_{WHD}$  | Data Hold to Write           | 0.5                   |      | 1.0                   |      | 1.0                   |      | ns    |
| $t_{WSA}$  | Address Setup/Write          | 0.5                   |      | 1.0                   |      | 1.0                   |      | ns    |
| $t_{WHA}$  | Address Hold/Write           | 0.5                   |      | 1.0                   |      | 1.0                   |      | ns    |
| $t_{WSBS}$ | Block Select Setup/Write     | 0.5                   |      | 1.0                   |      | 1.0                   |      | ns    |
| $t_{WHBS}$ | Block Select Hold/Write      | 0.5                   |      | 1.0                   |      | 1.0                   |      | ns    |
| $t_{WS}$   | Write Disable                | 2.0                   |      | 3.0                   |      | 4.0                   |      | ns    |
| $t_{WR}$   | Write Recovery               | 3.5                   |      | 6.0                   |      | 8.0                   |      | ns    |
| $t_r$      | Output Rise Time             | 0.7                   | 1.5  | 0.7                   | 2.5  | 1.0                   | 2.5  | ns    |
| $t_f$      | Output Fall Time             | 0.7                   | 1.5  | 0.7                   | 2.5  | 1.0                   | 2.5  | ns    |

## Switching Waveforms

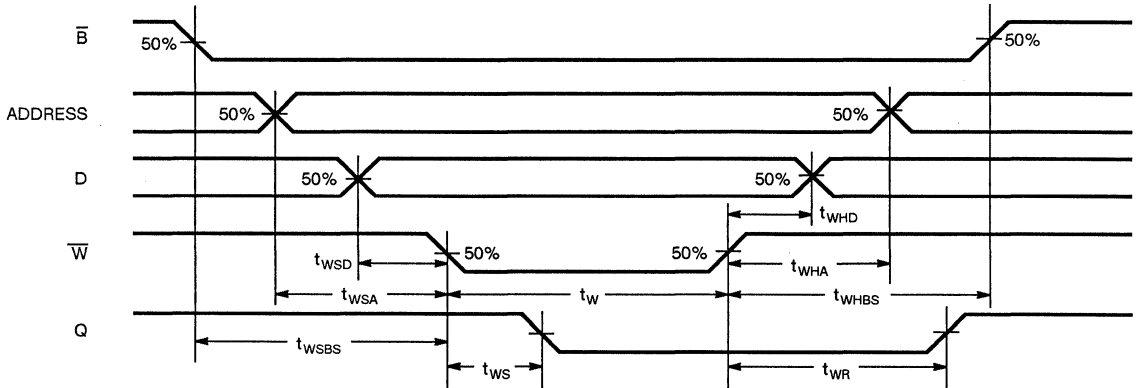
### Read Mode



C422-7

C422-8

### Write Mode



C422-9

### Truth Table

| Inputs      |           |       | Outputs | Mode      |
|-------------|-----------|-------|---------|-----------|
| $\bar{B}_x$ | $\bar{W}$ | $D_x$ | $Q_x$   |           |
| H           | X         | X     | L       | Disabled  |
| L           | L         | H     | L       | Write "H" |
| L           | L         | L     | L       | Write "L" |
| L           | H         | X     | Out     | Read      |

### Ordering Information

| I/O                 | $I_{EE}$<br>(mA) | $t_{AA}$<br>(ns) | Ordering Code  | Package Type | Operating Range |
|---------------------|------------------|------------------|----------------|--------------|-----------------|
| 10E <sup>[11]</sup> | 220              | 3.0              | CY10E422-3LC   | L63          | Commercial      |
|                     |                  | 5.0              | CY10E422-5LC   | L63          |                 |
|                     |                  | 5.0              | CY10E422-5DC   | D40          |                 |
| 10E                 | 150              | 5.0              | CY10E422L-5LC  | L63          | Commercial      |
|                     |                  | 5.0              | CY10E422L-5DC  | D40          |                 |
|                     |                  | 7.0              | CY10E422L-7LC  | L63          |                 |
|                     |                  | 7.0              | CY10E422L-7DC  | D40          |                 |
| 100K                | 220              | 3.0              | CY100E422-3LC  | L63          | Commercial      |
|                     |                  | 5.0              | CY100E422-5LC  | L63          |                 |
|                     |                  | 5.0              | CY100E422-5DC  | D40          |                 |
| 100K                | 150              | 5.0              | CY100E422L-5LC | L63          | Commercial      |
|                     |                  | 5.0              | CY100E422L-5DC | D40          |                 |
|                     |                  | 7.0              | CY100E422L-7LC | L63          |                 |
|                     |                  | 7.0              | CY100E422L-7DC | D40          |                 |

Note:

11. 10E specifications support both 10K and 10KH compatibility.  
Document #: 38-A-00002





1024 x 4 ECL  
Static RAM

Features

- 1024 x 4 bits organization
- Ultra high speed/standard power
  - $t_{AA} = 3 \text{ ns}$ ,  $t_{ACS} = 2 \text{ ns}$
  - $I_{EE} = 275 \text{ mA}$
- Low power version
  - $t_{AA} = 5 \text{ ns}$
  - $I_{EE} = 190 \text{ mA}$
- Both 10KH/10K and 100K compatible I/O versions
- On chip voltage compensation for improved noise margin

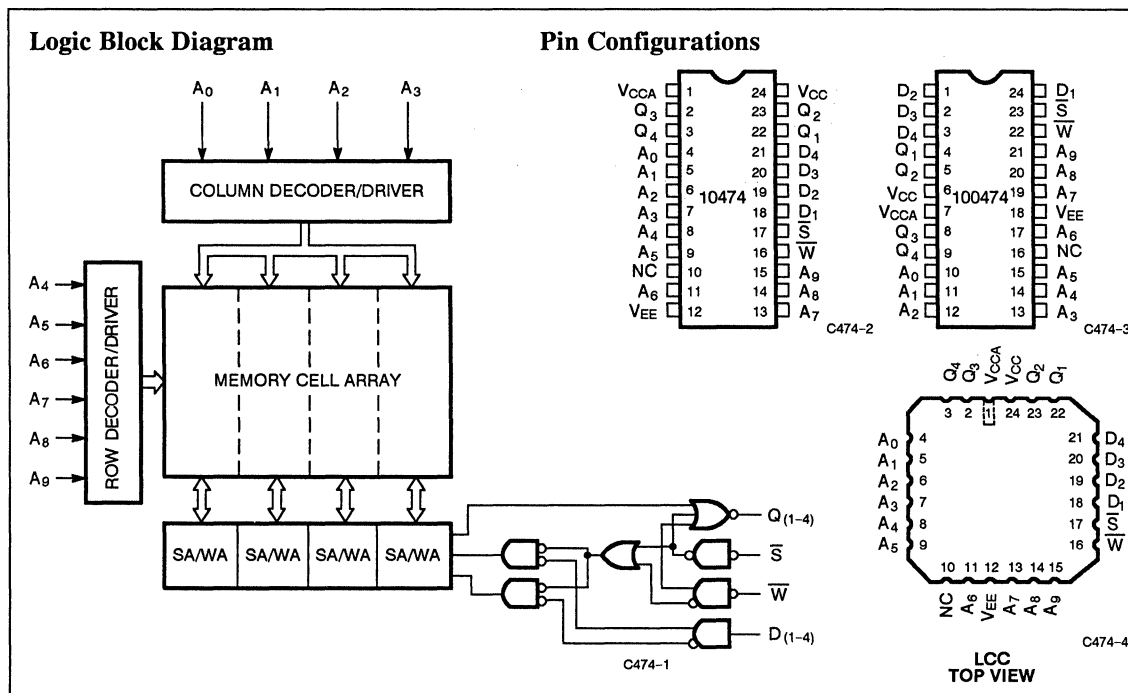
- Open emitter output for ease of memory expansion
- Industry standard pinout

Functional Description

The Cypress CY10E474 and CY100E474 are 1K x 4 ECL RAMs designed for scratch pad, control and Buffer Storage applications. These RAMs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor. Both parts are fully decoded random access memories organized as 1024 words

by 4 bits. The CY10E474 is 10KH/10K compatible. The CY100E474 is 100K compatible.

The active LOW chip select ( $\bar{S}$ ) input controls memory selection and allows for memory expansion. The read and write operations are controlled by the state of the active LOW write enable ( $\bar{W}$ ) input. With  $\bar{W}$  and  $\bar{S}$  LOW, the data at D(1-4) is written into the addressed location. To read  $\bar{W}$  is held HIGH, while  $\bar{S}$  is held LOW. Open emitter outputs allow for wired-OR connection to expand the memory.



Selection Guide

|                          | 10E474-3<br>100E474-3 | 10E474-5<br>100E474-5 | 10E474-7<br>100E474-7 |
|--------------------------|-----------------------|-----------------------|-----------------------|
| Maximum Access Time (ns) | 3                     | 5                     | 7                     |
| $I_{EE}$ Max. (mA)       | Commercial            | -275                  |                       |
|                          | "L"                   | -190                  | -190                  |

### Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied ..... -55°C to +125°C  
 Supply Voltage  $V_{EE}$  to  $V_{CC}$  ..... -7.0 to +0.5V  
 Input Voltage .....  $V_{EE}$  to +0.5V  
 Output Current ..... -50 mA

### Operating Range

 referenced to  $V_{CC}$ 

| Range                      | I/O      | Ambient Temperature | $V_{EE}$     |
|----------------------------|----------|---------------------|--------------|
| Commercial (Standard, "L") | 10KH/10K | 0°C to 75°C         | -5.2V ± 5%   |
| Commercial (Standard, "L") | 100K     | 0°C to 85°C         | -4.5V ± 0.3V |

### Electrical Characteristics

| Parameters | Description                                     | Test Conditions  | Temperature <sup>[1]</sup>   | Min.                              | Max.  | Units   |
|------------|---|--|--|-----------------------------------|-------|---------|
| $V_{OH}$   | Output HIGH Voltage                             | 10E <sup>[2]</sup> $R_L = 50 \Omega$ to -2V<br>$V_{EE} = -5.2V$<br>$V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min. | $T_A = 0^\circ C$  | -1000                             | -840  | mV      |
|            |   |  | $T_A = +25^\circ C$  | -960                              | -810  | mV      |
|            |   |  | $T_A = +75^\circ C$  | -900                              | -735  | mV      |
|            |   |  | 100K $R_L = 50 \Omega$ to -2V<br>$V_{EE} = -4.5V$<br>$V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min. | $T_A = 0^\circ C$ to $85^\circ C$ | -1025 | -880    |
| $V_{OL}$   | Output LOW Voltage                              | 10E $R_L = 50 \Omega$ to -2V<br>$V_{EE} = -5.2V$<br>$V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min.                | $T_A = 0^\circ C$  | -1870                             | -1665 | mV      |
|            |   |  | $T_A = +25^\circ C$  | -1850                             | -1650 | mV      |
|            |   |  | $T_A = +75^\circ C$  | -1830                             | -1625 | mV      |
|            |   |  | 100K $R_L = 50 \Omega$ to -2V<br>$V_{EE} = -4.5V$<br>$V_{IN} = V_{IH}$ Max. or $V_{IL}$ Min. | $T_A = 0^\circ C$ to $85^\circ C$ | -1810 | -1620   |
| $V_{IH}$   | Input HIGH Voltage                              | 10E<br>$V_{EE} = -5.2V$  | $T_A = 0^\circ C$  | -1170                             | -840  | mV      |
|            |   |  | $T_A = +25^\circ C$  | -1130                             | -810  | mV      |
|            |   |  | $T_A = +75^\circ C$  | -1070                             | -720  | mV      |
|            |   |  | 100K $V_{EE} = -4.5V$  | $T_A = 0^\circ C$ to $85^\circ C$ | -1165 | -880    |
| $V_{IL}$   | Input LOW Voltage                               | 10E<br>$V_{EE} = -5.2V$  | $T_A = 0^\circ C$  | -1950                             | -1480 | mV      |
|            |   |  | $T_A = +25^\circ C$  | -1950                             | -1480 | mV      |
|            |   |  | $T_A = +75^\circ C$  | -1950                             | -1450 | mV      |
|            |   |  | 100K $V_{EE} = -4.5V$  | $T_A = 0^\circ C$ to $85^\circ C$ | -1810 | -1475   |
| $I_{IH}$   | Input HIGH Current                              | $V_{IN} = V_{IH}$ Max.   |  |                                   | 220   | $\mu A$ |
| $I_{IL}$   | Input LOW Current                               | $V_{IN} = V_{IL}$ Min.   |  | 10                                |       | $\mu A$ |
| $I_{EE}$   | Supply Current<br>(All inputs and outputs open) | Commercial "L" (Low Power)   |  |                                   | -190  | mA      |
|            |   | Commercial Standard  |  |                                   | -275  | mA      |

**Notes:**

- Commercial grade is specified as ambient Temperature with transverse air flow greater than 500 linear feet per minute.
- 10E specifications support both 10K and 10KH compatibility.

### Capacitance<sup>[3]</sup>

| Parameters | Description            | Min. | Typ. | Max. <sup>[4]</sup> | Units |
|------------|------------------------|------|------|---------------------|-------|
| $C_{IN}$   | Input Pin Capacitance  |      | 4    | 5                   | pF    |
| $C_{OUT}$  | Output Pin Capacitance |      | 6    | 8                   | pF    |

**Notes:**

- Tested initially and after any design or process changes that may affect these parameters.
- For all packages except Cerdip (D40) which has maximums of  $C_{IN} = 10$  pF,  $C_{OUT} = 12$  pF.

### AC Test Loads and Waveforms [5, 6, 7, 8, 9, 10]

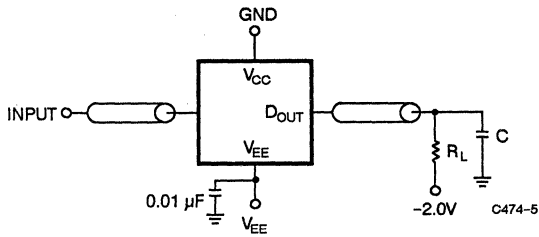
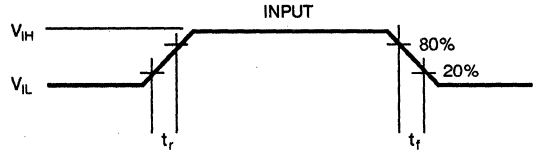


Figure 1



C474-6

Figure 2

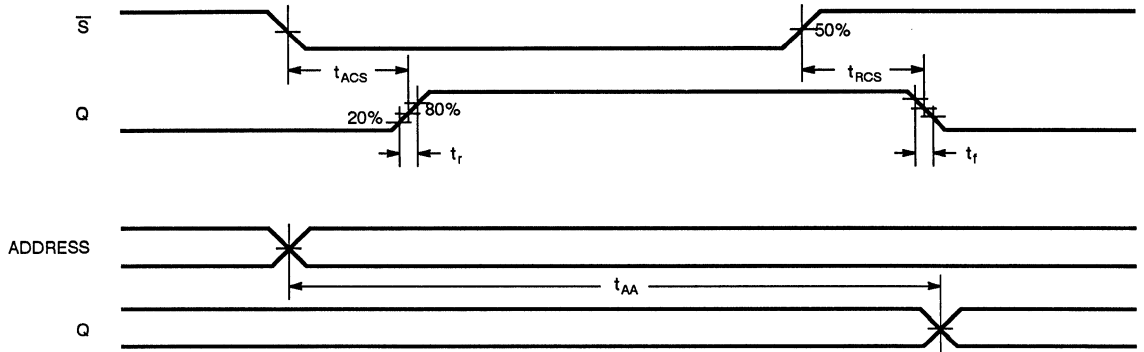
- Notes:
5.  $V_{IL} = V_{IL} \text{ Min.}$ ,  $V_{IH} = V_{IH} \text{ Max.}$  on 10E version.
  6.  $V_{IL} = -1.7V$ ,  $V_{IH} = -0.9V$  on 100K version.
  7.  $R_L = 50 \Omega$ ,  $C < 5 \text{ pF}$  (3 ns grade) or  $< 30 \text{ pF}$  (5, 7 ns grade) (includes fixture and stray capacitance).
  8. All coaxial cables should be  $50 \Omega$  with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
  9.  $t_r = t_f = 0.7 \text{ ns}$ .
  10. All timing measurements are made from the 50% point of all waveforms.

### Switching Characteristics Over Operating Range

| Parameters | Description             | 10E474-3<br>100E474-3 |      | 10E474-5<br>100E474-5 |      | 10E474-7<br>100E474-7 |      | Units |
|------------|-------------------------|-----------------------|------|-----------------------|------|-----------------------|------|-------|
|            |                         | Min.                  | Max. | Min.                  | Max. | Min.                  | Max. |       |
| $t_{ACS}$  | Input to Output delay   |                       | 2.0  |                       | 3.0  |                       | 3.0  | ns    |
| $t_{RCS}$  | Chip Select Recovery    |                       | 2.0  |                       | 3.0  |                       | 3.0  | ns    |
| $t_{AA}$   | Address Access Time     |                       | 3.0  |                       | 5.0  |                       | 7.0  | ns    |
| $t_w$      | Write Pulse Width       | 3.0                   |      | 3.0                   |      | 4.0                   |      | ns    |
| $t_{WSD}$  | Data Setup to Write     | 0.5                   |      | 0.5                   |      | 1.0                   |      | ns    |
| $t_{WHD}$  | Data Hold to Write      | 0.5                   |      | 1.5                   |      | 2.0                   |      | ns    |
| $t_{WSA}$  | Address Setup/Write     | 0.5                   |      | 0.5                   |      | 1.0                   |      | ns    |
| $t_{WHA}$  | Address Hold/Write      | 0.5                   |      | 1.5                   |      | 2.0                   |      | ns    |
| $t_{WSCS}$ | Chip Select Setup/Write | 0.5                   |      | 0.5                   |      | 1.0                   |      | ns    |
| $t_{WHCS}$ | Chip Select Hold/Write  | 0.5                   |      | 1.5                   |      | 2.0                   |      | ns    |
| $t_{WS}$   | Write Disable           | 2.0                   |      | 3.0                   |      | 4.0                   |      | ns    |
| $t_{WR}$   | Write Recovery          | 3.5                   |      | 6.5                   |      | 9.0                   |      | ns    |
| $t_r$      | Output Rise Time        | 0.7                   | 1.5  | 0.7                   | 2.5  | 1.0                   | 2.5  | ns    |
| $t_f$      | Output Fall Time        | 0.7                   | 1.5  | 0.7                   | 2.5  | 1.0                   | 2.5  | ns    |

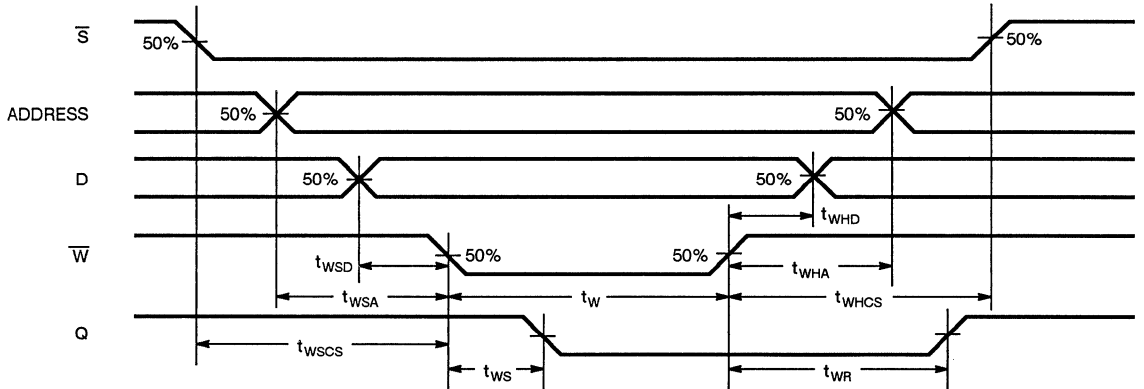
## Switching Waveforms

### Read Mode



C474-7

### Write Mode



C474-8

### Ordering Information

| I/O                 | I <sub>EE</sub><br>(mA) | t <sub>AA</sub><br>(ns) | Ordering Code  | Package Type | Operating Range |
|---------------------|-------------------------|-------------------------|----------------|--------------|-----------------|
| 10E <sup>(11)</sup> | 275                     | 3.0                     | CY10E474-3LC   | L63          | Commercial      |
|                     |                         | 5.0                     | CY10E474-5LC   | L63          |                 |
|                     |                         | 5.0                     | CY10E474-5DC   | D40          |                 |
| 10E                 | 190                     | 5.0                     | CY10E474L-5LC  | L63          | Commercial      |
|                     |                         | 5.0                     | CY10E474L-5DC  | D40          |                 |
|                     |                         | 7.0                     | CY10E474L-7LC  | L63          |                 |
|                     |                         | 7.0                     | CY10E474L-7DC  | D40          |                 |
| 100K                | 275                     | 3.0                     | CY100E474-3LC  | L63          | Commercial      |
|                     |                         | 5.0                     | CY100E474-5LC  | L63          |                 |
|                     |                         | 5.0                     | CY100E474-5DC  | D40          |                 |
| 100K                | 190                     | 5.0                     | CY100E474L-5LC | L63          | Commercial      |
|                     |                         | 5.0                     | CY100E474L-5DC | D40          |                 |
|                     |                         | 7.0                     | CY100E474L-7LC | L63          |                 |
|                     |                         | 7.0                     | CY100E474L-7DC | D40          |                 |

**Note:**

11. 10E specifications support both 10K and 10KH compatibility.

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## Introduction

Success at any endeavor requires a high level of dedication to the task. Cypress Semiconductor has demonstrated its dedication through its corporate commitment to support the military marketplace. The commitment starts with product design. All products are designed on our state-of-the-art CMOS, BiCMOS and Bipolar processes and they must meet the full  $-55$  to  $+125$  degree C operational criteria for military use. The commitment continues with the 1986 DESC certification of our automated U.S. facility in San Jose, California. The commitment shows in our dedication to meet and exceed the stringent quality and reliability requirements of MIL-STD-883 and MIL-M-38510. It shows in Cypress' participation in each of the military processing programs: 883C-Compliant, SMD (Standard Military Drawing) and JAN. Finally, our commitment shows in our leadership position in special packages for military use.

## Product Design

Every Cypress product is designed to meet or exceed the full temperature and functional requirements of military product. This means that Cypress builds military product as a matter of course, rather than as an accidental benefit of favorable test yield. Designs are being carried out on our industry-leading 0.8 micron CMOS, BiCMOS and Bipolar processes. Cypress is able to offer a family of products that are industry leaders in density, low operating and standby current and high speed. In addition, our technology results in products with very small manufacturable die sizes that will fit into the LCC's and flatpacks so often used on military programs.

## DESC-Certified Facility

On May 8, 1986, the Cypress facility at 3901 North First Street in San Jose, California was certified by DESC for the production of JAN Level B CMOS Microcircuits. This certification not only provided Cypress with the ability to qualify product for JAN use, but it also benefitted all of our customers by acknowledging that our San Jose facility has the necessary documentation and procedures in place to manufacture product to the most stringent of quality and reliability requirements. Our wafer fabrication facilities are Class 10 (San Jose) and Class 1 (Round Rock, TX) manufacturing environments and our assembly facility is also a clean room. In addition, our highly automated assembly facility is entirely located in the U.S.A. and is capable of handling virtually any hermetic package configuration.

## Data Sheet Documentation

Every Cypress final data sheet is a corporate document with a revision history. The document number and revision appears on each final data sheet. Cypress maintains a listing of all data sheet documentation and a copy is available to customers upon request. This gives a customer the ability to verify the current status of any data sheet and it also gives that customer the ability to obtain updated specifications as required.

Every final data sheet also contains detailed Group A subgroup testing information. Each of the specified parameters that are tested at Group A are listed in a table at the end of each final data sheet, with a notation as to which specific Group A test subgroups apply.

## Assembly Traceability Code™

Cypress Semiconductor marks an assembly traceability code on every military package that is large enough to contain the code. The ATC automatically provides traceability for that product to the individual wafer lot. This unique code provides Cypress with the ability to determine which operators and equipment were used in the manufacture of that product from start to finish.

## Quality and Reliability

MIL-STD-883 and MIL-M-38510 spell out the toughest of quality and reliability standards for military products. Cypress products meet all of these requirements and more. Our in-house quality and reliability programs are being updated regularly with tighter and tighter objectives. Please refer to the chapter on Quality, Reliability and Process Flows for further details.

## Military Product Offerings

Cypress offers three different levels of processing for military product.

First, all Cypress products are available with processing in full compliance with MIL-STD-883, Revision C.

Secondly, selected products are available to the SMD (Standard Military Drawing) program supervised by DESC. These products are not only fully 883C-compliant but they are also screened to the electrical requirements of the applicable military drawing.

Third, selected products are available as JAN devices. These products are processed in full accordance with MIL-M-38510 and they are screened to the electrical requirements of the applicable JAN slash sheet.

## Product Packaging

All packages for military product are hermetic. A look at the package appendix in the back of this data book will give the reader an appreciation of the variety of packages offered. Included are cerdips, windowed cerdips, leadless chip carriers (LCC's), leadless chip carriers with windows for reprogrammable products, cerpack, windowed cerpack, bottom-brazed flatpacks and pin grid arrays. As indicated above, all of these packages are assembled in the U.S. in our highly automated San Jose plant.

## Summary

Cypress Semiconductor is committed to the support of the military marketplace. Our commitment is demonstrated by our product designs, our DESC-certified facility, our documentation and traceability, our quality and reliability programs, our support of all levels of military processing and by our leadership in special packaging.



# Military Product Selection Guide

|       | Size                       | Organization               | Pins    | Part Number      | JAN/SMD Number           | Speed (ns)                       | Icc/Isb/IccDR (mA @ ns) |
|-------|----------------------------|----------------------------|---------|------------------|--------------------------|----------------------------------|-------------------------|
| SRAMs | 64                         | 16 x 4—Inverting           | 16      | CY7C189          |                          | t <sub>AA</sub> = 25             | 70 @ 25                 |
|       | 64                         | 16 x 4—Non-Inverting       | 16      | CY7C190          |                          | t <sub>AA</sub> = 25             | 70 @ 25                 |
|       | 64                         | 16 x 4—Inverting           | 16      | CY27S03/A        |                          | t <sub>AA</sub> = 25, 35         | 100 @ 25                |
|       | 64                         | 16 x 4—Non-Inverting       | 16      | CY27S07/A        |                          | t <sub>AA</sub> = 25, 35         | 100 @ 25                |
|       | 64                         | 16 x 4—Inverting/Low Power | 16      | CY27LS03         |                          | t <sub>AA</sub> = 65             | 38 @ 65                 |
|       | 1K                         | 256 x 4                    | 22      | CY7C122          | 5962-88594               | t <sub>AA</sub> = 25, 35         | 90 @ 25                 |
|       | 1K                         | 256 x 4                    | 24S     | CY7C123          |                          | t <sub>AA</sub> = 10, 12, 15     | 150 @ 15                |
|       | 1K                         | 256 x 4                    | 22      | CY9122/91L22     | 5962-88594               | t <sub>AA</sub> = 35, 45         | 90 @ 45                 |
|       | 1K                         | 256 x 4                    | 22      | CY93422A/93L422A |                          | t <sub>AA</sub> = 45, 55, 60, 75 | 90 @ 55                 |
|       | 4K                         | 4K x 1—CS Power Down       | 18      | CY7C147          | M38510/289               | t <sub>AA</sub> = 35, 45         | 110/10 @ 35             |
|       | 4K                         | 4K x 1—CS Power Down       | 18      | CY2147           | M38510/289               | t <sub>AA</sub> = 45, 55         | 140/25 @ 45             |
|       | 4K                         | 4K x 1—CS Power Down       | 18      | CY7C147          | 5962-88587               | t <sub>AA</sub> = 35, 45         | 110/10 @ 35             |
|       | 4K                         | 4K x 1—CS Power Down       | 18      | CY2147           | 5962-88587               | t <sub>AA</sub> = 45, 55         | 140/25 @ 45             |
|       | 4K                         | 1K x 4—CS Power Down       | 18      | CY7C148          |                          | t <sub>AA</sub> = 35, 45         | 110/10 @ 35             |
|       | 4K                         | 1K x 4—CS Power Down       | 18      | CY2148           |                          | t <sub>AA</sub> = 45, 55         | 140/25 @ 45             |
|       | 4K                         | 1K x 4                     | 18      | CY7C149          |                          | t <sub>AA</sub> = 35, 45         | 110 @ 35                |
|       | 4K                         | 1K x 4                     | 18      | CY2149           |                          | t <sub>AA</sub> = 45, 55         | 140 @ 45                |
|       | 4K                         | 1K x 4—Separate I/O        | 24S     | CY7C150          | 5962-88588               | t <sub>AA</sub> = 15, 25, 35     | 100 @ 15                |
|       | 8K                         | 1K x 8—Dual Port           | 48      | CY7C130/31       | 5962-86875               | t <sub>AA</sub> = 35, 45, 55     | 120/40 @ 35             |
|       | 8K                         | 1K x 8—Dual Port Slave     | 48      | CY7C140/41       | 5962-86875               | t <sub>AA</sub> = 35, 45, 55     | 120/40 @ 35             |
|       | 16K                        | 2K x 8—CS Power Down       | 24S     | CY7C128          | 84036                    | t <sub>AA</sub> = 35, 45, 55     | 100/20 @ 55             |
|       | 16K                        | 2K x 8—CS Power Down       | 24S     | CY7C128A         | 84036                    | t <sub>AA</sub> = 25, 35, 45, 55 | 125/40 @ 25             |
|       | 16K                        | 2K x 8—CS Power Down       | 24      | CY6116/7         | 84036                    | t <sub>AA</sub> = 35, 45, 55     | 130/20 @ 35             |
|       | 16K                        | 16K x 1—CS Power Down      | 20      | CY7C167          | 84132                    | t <sub>AA</sub> = 35, 45         | 50/20 @ 45              |
|       | 16K                        | 16K x 1—CS Power Down      | 20      | CY7C167A         | 84132                    | t <sub>AA</sub> = 25, 35, 45     | 70/20 @ 25              |
|       | 16K                        | 4K x 4—CS Power Down       | 20      | CY7C168          | 5962-86705               | t <sub>AA</sub> = 35, 45         | 70/20 @ 45              |
|       | 16K                        | 4K x 4—CS Power Down       | 20      | CY7C168A         | 5962-86705               | t <sub>AA</sub> = 25, 35, 45     | 80/20 @ 25              |
|       | 16K                        | 4K x 4                     | 20      | CY7C169          |                          | t <sub>AA</sub> = 35, 40         | 70 @ 40                 |
|       | 16K                        | 4K x 4                     | 20      | CY7C169A         |                          | t <sub>AA</sub> = 25, 35, 40     | 70/20 @ 35              |
|       | 16K                        | 4K x 4—Output Enable       | 22S     | CY7C170          |                          | t <sub>AA</sub> = 35, 45         | 120 @ 35                |
|       | 16K                        | 4K x 4—Output Enable       | 22S     | CY7C170A         |                          | t <sub>AA</sub> = 25, 35, 45     | 120 @ 25                |
|       | 16K                        | 4K x 4—Separate I/O        | 24S     | CY7C171          |                          | t <sub>AA</sub> = 35, 45         | 70 @ 45                 |
|       | 16K                        | 4K x 4—Separate I/O        | 24S     | CY7C172          |                          | t <sub>AA</sub> = 35, 45         | 70 @ 45                 |
|       | 16K                        | 4K x 4—Separate I/O        | 24S     | CY7C171A/2A      |                          | t <sub>AA</sub> = 25, 35, 45     | 80/20 @ 25              |
|       | 16K                        | 2K x 8—Dual Port           | 48      | CY7C132/36       | 5962-87002               | t <sub>AA</sub> = 35, 45, 55     | 170/65 @ 35             |
|       | 16K                        | 2K x 8—Dual Port Slave     | 48      | CY7C142/46       | 5962-87002               | t <sub>AA</sub> = 35, 45, 55     | 120/40 @ 45             |
|       | 64K                        | 8K x 8—CS Power Down       | 28S     | CY7C185/L        | 5962-85525               | t <sub>AA</sub> = 35, 45, 55     | 100/20/1 @ 45           |
|       | 64K                        | 8K x 8—CS Power Down       | 28S     | CY7C185          |                          | t <sub>AA</sub> = 12, 15         | 155/50 @ 12             |
|       | 64K                        | 8K x 8—CS Power Down       | 28      | CY7C186/L        | 5962-85525               | t <sub>AA</sub> = 35, 45, 55     | 100/20/1 @ 45           |
|       | 64K                        | 8K x 8—CS Power Down       | 28      | CY7C186          |                          | t <sub>AA</sub> = 12, 15         | 145/50 @ 15             |
|       | 64K                        | 16K x 4—CS Power Down      | 22S     | CY7C164/L        | 5962-86859               | t <sub>AA</sub> = 35, 45         | 70/20/1 @ 35            |
|       | 64K                        | 16K x 4—CS Power Down      | 22S     | CY7C164          |                          | t <sub>AA</sub> = 12, 15         | 150/50 @ 12             |
|       | 64K                        | 16K x 4—Output Enable      | 24S     | CY7C166/L        | 5962-86859               | t <sub>AA</sub> = 35, 45         | 70/20/1 @ 35            |
|       | 64K                        | 16K x 4—Output Enable      | 24S     | CY7C166          |                          | t <sub>AA</sub> = 12, 15         | 135/50 @ 15             |
|       | 64K                        | 16K x 4—Separate I/O       | 28S     | CY7C161/L        |                          | t <sub>AA</sub> = 35, 45         | 70/20/1 @ 35            |
|       | 64K                        | 16K x 4—Separate I/O       | 28S     | CY7C162/L        |                          | t <sub>AA</sub> = 35, 45         | 70/20/1 @ 35            |
|       | 64K                        | 16K x 4—Separate I/O       | 28S     | CY7C161/2        |                          | t <sub>AA</sub> = 12, 15         | 135/50 @ 15             |
|       | 64K                        | 64K x 1—CS Power Down      | 22      | CY7C187/L        | 5962-86015               | t <sub>AA</sub> = 35, 45         | 70/20/1 @ 35            |
|       | 256K                       | 16K x 16—Cache RAM         | 44      | CY7C157          |                          | t <sub>AA</sub> = 24, 33         | 300 @ 24                |
|       | 256K                       | 32K x 8—CS Power Down      | 28      | CY7C198          | 5962-88662               | t <sub>AA</sub> = 45, 55         | 120/20 @ 45             |
| 256K  | 32K x 8—CS Power Down      | 28S                        | CY7C199 |                  | t <sub>AA</sub> = 45, 55 | 120/20 @ 45                      |                         |
| 256K  | 64K x 4—CS Power Down      | 24S                        | CY7C194 | 5962-88681       | t <sub>AA</sub> = 35, 45 | 90/20 @ 35                       |                         |
| 256K  | 64K x 4—CS Power Down + OE | 28S                        | CY7C196 |                  | t <sub>AA</sub> = 35, 45 | 90/20 @ 35                       |                         |
| 256K  | 64K x 4—Separate I/O       | 28S                        | CY7C191 |                  | t <sub>AA</sub> = 35, 45 | 90/20 @ 35                       |                         |
| 256K  | 64K x 4—Separate I/O       | 28S                        | CY7C192 |                  | t <sub>AA</sub> = 35, 45 | 90/20 @ 35                       |                         |
| 256K  | 256K x 1—CS Power Down     | 24S                        | CY7C197 | 5962-88725       | t <sub>AA</sub> = 35, 45 | 80/20 @ 35                       |                         |

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\*(W) = Windowed Package

(O) = Opaque Package

22S stands for 22-pin 300 mil DIP.

24S stands for 24-pin 300 mil DIP.

28S stands for 28-pin 300 mil DIP.



# Military Product Selection Guide (Continued)

|              | Size                  | Organization                 | Pins    | Part Number | JAN/SMD Number*      | Speed (ns)                                | I <sub>CC</sub> /I <sub>SB</sub> (mA @ ns) |
|--------------|-----------------------|------------------------------|---------|-------------|----------------------|---|--|
| <b>PROMs</b> | 4K                    | 512 x 8—Registered           | 24S     | CY7C225     | 5962-88518(O)        | t <sub>SA</sub> /CO = 30/15, 35/20, 40/25 | 120 @ 30/15                                |
|              | 8K                    | 1K x 8—Registered            | 24S     | CY7C235     | 5962-88636(O)        | t <sub>SA</sub> /CO = 30/15, 40/20        | 120 @ 30/15                                |
|              | 8K                    | 1K x 8                       | 24S     | CY7C281     | 5962-87651(O)        | t <sub>AA</sub> = 45                      | 120 @ 45                                   |
|              | 8K                    | 1K x 8                       | 24      | CY7C282     | 5962-87651(O)        | t <sub>AA</sub> = 45                      | 120 @ 45                                   |
|              | 16K                   | 2K x 8—Registered            | 24S     | CY7C245     | 5962-87529(W)        | t <sub>SA</sub> /CO = 35/15, 45/25        | 120 @ 35/15                                |
|              | 16K                   | 2K x 8—Registered            | 24S     | CY7C245     | 5962-88735(O)        | t <sub>SA</sub> /CO = 35/15, 45/25        | 120 @ 35/15                                |
|              | 16K                   | 2K x 8—Registered            | 24S     | CY7C245A    |                      | t <sub>SA</sub> /CO = 25/15, 35/20        | 120 @ 25/15                                |
|              | 16K                   | 2K x 8—Registered            | 24S     | CY7C245A    | 5962-88735(O)        | t <sub>SA</sub> /CO = 25/15, 35/20        | 120 @ 25/15                                |
|              | 16K                   | 2K x 8                       | 24S     | CY7C291     | 5962-87650(W)        | t <sub>AA</sub> = 35, 50                  | 120 @ 35                                   |
|              | 16K                   | 2K x 8                       | 24S     | CY7C291     | 5962-88734(O)        | t <sub>AA</sub> = 35, 50                  | 120 @ 35                                   |
|              | 16K                   | 2K x 8                       | 24S     | CY7C291A    | 5962-87650           | t <sub>AA</sub> = 30, 35, 50              | 120 @ 30                                   |
|              | 16K                   | 2K x 8—CS Power Down         | 24S     | CY7C293A    | 5962-88680(W)        | t <sub>AA</sub> = 30, 35, 50              | 120/30 @ 35                                |
|              | 16K                   | 2K x 8                       | 24      | CY7C292     | 5962-88734(O)        | t <sub>AA</sub> = 50                      | 120 @ 50                                   |
|              | 16K                   | 2K x 8                       | 24      | CY7C292A    |                      | t <sub>AA</sub> = 30, 35, 50              | 120 @ 30                                   |
|              | 64K                   | 8K x 8—CS Power Down         | 24S     | CY7C261     | 5962-87515(W)        | t <sub>AA</sub> = 45, 55                  | 120/30 @ 45                                |
|              | 64K                   | 8K x 8                       | 24S     | CY7C263     |                      | t <sub>AA</sub> = 45, 55                  | 120 @ 45                                   |
|              | 64K                   | 8K x 8                       | 24      | CY7C264     |                      | t <sub>AA</sub> = 45, 55                  | 120 @ 45                                   |
|              | 64K                   | 8K x 8—Registered            | 28S     | CY7C265     |                      | t <sub>SA</sub> /CO = 50/25, 60/25        | 120 @ 50/25                                |
|              | 64K                   | 8K x 8                       | 28      | CY7C266     |                      | t <sub>AA</sub> = 55                      | 90   |
|              | 64K                   | 8K x 8—Registered/Diagnostic | 28S     | CY7C269     |                      | t <sub>SA</sub> /CO = 50/25, 60/25        | 100 @ 60/25                                |
|              | 64K                   | 8K x 8—Registered/Diagnostic | 32      | CY7C268     |                      | t <sub>SA</sub> /CO = 50/25, 60/25        | 100 @ 60/25                                |
|              | 128K                  | 16K x 8—CS Power Down        | 28S     | CY7C251     | 5962-89537           | t <sub>AA</sub> = 55, 65                  | 120/35 @ 55                                |
|              | 128K                  | 16K x 8                      | 28      | CY7C254     | 5962-89538           | t <sub>AA</sub> = 55, 65                  | 120 @ 55                                   |
|              | 256K                  | 32K x 8—CS Power Down        | 28S     | CY7C271     |                      | t <sub>AA</sub> = 55, 65                  | 130/40 @ 55                                |
|              | 256K                  | 32K x 8                      | 28      | CY7C274     |                      | t <sub>AA</sub> = 55                      | 130/40 @ 55                                |
|              | 256K                  | 32K x 8—Registered           | 28S     | CY7C277     |                      | t <sub>SA</sub> /CO = 50/25               | 130/40 @ 55                                |
|              | 256K                  | 32K x 8—Latched              | 28S     | CY7C279     |                      | t <sub>AA</sub> = 55                      | 130/40 @ 55                                |
|              | 512K                  | 64K x 8—FCA                  | 28S     | CY7C285     |                      | t <sub>AA</sub> /CAA = 75/35              | 200 @ 35                                   |
| 512K         | 64K x 8—CE Power Down | 28                           | CY7C286 |             | t <sub>AA</sub> = 75 | 150/50 @ 75                               |  |
|              | Size                  | Organization                 | Pins    | Part Number | JAN/SMD Number*      | Speed (ns/MHz)                            | I <sub>CC</sub> (mA @ ns/MHz)              |
| <b>PLDs</b>  | PALC20                | 16L8, 16R8, 16R6, 16R4       | 20      | PALC16XX    | 5962-88678(W)        | t <sub>PD</sub> = 20, 30, 40              | 70 @ 20                                    |
|              | PALC20                | 16L8, 16R8, 16R6, 16R4       | 20      | PALC16XX    | 5962-88713(O)        | t <sub>PD</sub> = 20, 30, 40              | 70 @ 20                                    |
|              | PLD20                 | 18G8—Generic                 | 20      | PLDC18G8    |                      | t <sub>PD</sub> /S/CO = 15/15/12          | 110  |
|              | PLDC24                | 22V10—Macro Cell             | 24S     | PALC22V10   | 5962-87539(W)        | t <sub>PD</sub> /S/CO = 20/17/15          | 100 @ 25/20/20                             |
|              | PLDC24                | 22V10—Macro Cell             | 24S     | PALC22V10   | 5962-88670(O)        | t <sub>PD</sub> /S/CO = 20/17/15          | 100 @ 25/20/20                             |
|              | PLDC24                | 20G10—Generic                | 24S     | PLDC20G10   | 5962-88637(O)        | t <sub>PD</sub> /S/CO = 20/17/15          | 80 @ 30/20/20                              |
|              | PLDC24                | 20RA10—Asynchronous          | 24S     | PLDC20RA10  |                      | t <sub>PD</sub> /SU/CO = 25/15/25         | 100 @ 25/15/25                             |
|              | PLD                   | 16P8—100K ECL                | 24      | CY100E301   |                      | t <sub>PD</sub> = 6                       | -240 @ 6                                   |
|              | PLD                   | 16P8—10KH ECL                | 24      | CY10E301    |                      | t <sub>PD</sub> = 6                       | -240 @ 6                                   |
|              | PLD                   | 16P4—100K ECL                | 24      | CY100E302   |                      | t <sub>PD</sub> = 6                       | -220 @ 6                                   |
|              | PLD                   | 16P4—10KH ECL                | 24      | CY10E302    |                      | t <sub>PD</sub> = 6                       | -220 @ 6                                   |
|              | PLDC28                | 7C330—State Machine          | 28S     | CY7C330     | 5962-89546(W)        | 40, 28 MHz                                | 150 @ 40 MHz                               |
|              | PLDC28                | 7C331—Asynchronous           | 28S     | CY7C331     |                      | t <sub>PD</sub> /S/CO = 30/25/30          | 150 @ 30/25/30                             |
|              | PLDC28                | 7C332—Combinatorial          | 28S     | CY7C332     |                      | t <sub>CO</sub> /IS/TH = 25/5/7           | 150 @ 25/5/7                               |

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# Military Product Selection Guide (Continued)

| Size    |                                | Organization   | Pins        | Part Number    | JAN/SMD Number                | Speed (ns/MHz)                 | I <sub>CC</sub> /I <sub>SB</sub> (mA @ ns/MHz) |
|---------|--------------------------------|--|-------------|----------------|-------------------------------|--------------------------------|--|
| FIFOs   | 256                            | 64 x 4—Cascadeable   | 16          | CY3341         |                               | 1.2, 2.0 MHz                   | 60 @ 2.0 MHz                                   |
|         | 256                            | 64 x 4—Cascadeable   | 16          | CY7C401        |                               | 10, 15, 25 MHz                 | 90 @ 15 MHz                                    |
|         | 256                            | 64 x 4—Cascadeable/OE  | 16          | CY7C403        |                               | 10, 15, 25 MHz                 | 90 @ 25 MHz                                    |
|         | 320                            | 64 x 5—Cascadeable   | 18          | CY7C402        |                               | 10, 15 MHz                     | 90 @ 15 MHz                                    |
|         | 320                            | 64 x 5—Cascadeable/OE  | 18          | CY7C404        | 5962-86846                    | 10, 15, 25 MHz                 | 90 @ 25 MHz                                    |
|         | 512                            | 64 x 8—Cascadeable/OE  | 28S         | CY7C408        |                               | 15, 25 MHz                     | 120 @ 25 MHz                                   |
|         | 576                            | 64 x 9—Cascadeable   | 28S         | CY7C409        |                               | 15, 25 MHz                     | 120 @ 25 MHz                                   |
|         | 4K                             | 512 x 9—Cascadeable  | 28          | CY7C420        |                               | t <sub>A</sub> = 30, 40, 65 ns | 120/20 @ 30                                    |
|         | 4K                             | 512 x 9—Cascadeable  | 28S         | CY7C421        |                               | t <sub>A</sub> = 30, 40, 65 ns | 120/20 @ 30                                    |
|         | 9K                             | 1K x 9—Cascadeable   | 28          | CY7C424        |                               | t <sub>A</sub> = 30, 40, 65 ns | 120/20 @ 30                                    |
|         | 9K                             | 1K x 9—Cascadeable   | 28S         | CY7C425        |                               | t <sub>A</sub> = 30, 40, 65 ns | 120/20 @ 30                                    |
|         | 18K                            | 2K x 9—Cascadeable   | 28          | CY7C428        | 5962-88669                    | t <sub>A</sub> = 30, 40, 65 ns | 120/20 @ 30                                    |
|         | 18K                            | 2K x 9—Cascadeable   | 28S         | CY7C429        | 5962-88669                    | t <sub>A</sub> = 30, 40, 65 ns | 120/20 @ 30                                    |
|         | Size                           | Organization   | Pins        | Part Number    | JAN/SMD Number*               | Speed (ns)                     | I <sub>CC</sub> /I <sub>SB</sub> (mA @ ns)     |
| LOGIC   | 2901—4 Bit Slice               | 40   | CY7C901     | 5962-88535     | t <sub>CLK</sub> = 27, 32     | 90 @ 27                        |  |
|         | 2901—4 Bit Slice               | 40   | CY2901C     | 5962-88535     | C Speed                       | 180 @ 32                       |  |
|         | 4 x 2901—16 Bit Slice          | 64   | CY7C9101    | 5962-89517     | t <sub>CLK</sub> = 35, 45     | 85 @ 35                        |  |
|         | 2909—Sequencer                 | 28   | CY7C909     |                | t <sub>CLK</sub> = 30, 40     | 55 @ 30                        |  |
|         | 2911—Sequencer                 | 20   | CY7C911     |                | t <sub>CLK</sub> = 30, 40     | 55 @ 30                        |  |
|         | 2909—Sequencer                 | 28   | CY2909A     |                | A Speed                       | 90 @ 40                        |  |
|         | 2911—Sequencer                 | 20   | CY2911A     |                | A Speed                       | 90 @ 40                        |  |
|         | 2910—Controller (17 Word)      | 40   | CY7C910     | 5962-87708     | t <sub>CLK</sub> = 46, 51, 99 | 90 @ 46                        |  |
|         | 2910—Controller (9 Word)       | 40   | CY2910A     | 5962-87708     | A Speed                       | 170 @ 51                       |  |
|         | 16-Bit Microprogrammed ALU     | 52   | CY7C9116    | 5962-88612     | 65, 79, 100                   | 166 @ 10 MHz                   |  |
|         | 16-Bit Microprogrammed ALU     | 68   | CY7C9117    |                | 65, 79, 100                   | 166 @ 10 MHz                   |  |
|         | 16 x 16 Multiplier             | 64   | CY7C516     | 5962-87686     | t <sub>MC</sub> = 42, 55, 75  | 110 @ 10 MHz                   |  |
|         | 16 x 16 Multiplier             | 64   | CY7C517     | 5962-87686     | t <sub>MC</sub> = 42, 55, 75  | 110 @ 10 MHz                   |  |
|         | 16 x 16 Multiplier/Accumulator | 64   | CY7C510     | 5962-88733     | t <sub>MC</sub> = 55, 65, 75  | 110 @ 10 MHz                   |  |
| Type    | Organization                   | Pins   | Part Number | JAN/SMD Number | Speed (ns)                    | I <sub>CC</sub> (mA @ MHz)     |  |
| RISC    | IU                             | SPARC 32 Bit Integer Unit                                    | 207         | CY7C601        |                               | t <sub>CYC</sub> = 33, 25 MHz  | TBD  |
|         | FPU                            | Floating Point Unit  | 144         | CY7C602        |                               | t <sub>CYC</sub> = 25 MHz      | TBD  |
|         | CMU                            | Cache Controller Memory Management Unit                      | 207         | CY7C604        |                               | t <sub>CYC</sub> = 33, 25 MHz  | TBD  |
|         | CMU-MP                         | Cache Controller and Multi-Processing Memory Management Unit | 207         | CY7C605        |                               | t <sub>CYC</sub> = 33, 25 MHz  | TBD  |
| Size    | Organization                   | Pins   | Part Number | Packages       | Speed (ns)                    | I <sub>CC</sub> (mA @ ns)      |  |
| Modules | 256K                           | 16K x 16—SRAM (JEDEC)  | 40          | CYM1610        | HD                            | t <sub>AA</sub> = 35, 45, 50   | 330 @ 35                                       |
|         | 1M                             | 128K x 8—SRAM (JEDEC)  | 32          | CYM1420        | HD                            | t <sub>AA</sub> = 45, 55       | 210 @ 45                                       |
|         | 1M                             | 64K x 16—SRAM (JEDEC)  | 40          | CYM1620        | HD                            | t <sub>AA</sub> = 45, 55       | 340 @ 45                                       |
|         | 1M                             | 64K x 16—SRAM  | 40          | CYM1621        | HD                            | t <sub>AA</sub> = 30, 35, 45   | 1250 @ 30                                      |
|         | 2M                             | 64K x 32—SRAM  | 60          | CYM1830        | HD                            | t <sub>AA</sub> = 35, 45, 55   | 550 @ 35                                       |
|         | 4M                             | 256K x 16—SRAM   | 48          | CYM1641        | HD                            | t <sub>AA</sub> = 35, 45, 55   | 1760 @ 35                                      |

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## DESC SMD (Standardized Military Drawing) Approvals<sup>[1]</sup>

| SMD Number |      | Cypress <sup>[2]</sup><br>Part Number | Package <sup>[3]</sup> |      | Product<br>Description |
|------------|------|---------------------------------------|------------------------|------|------------------------|
|            |      |                                       | Description            | Type |                        |
| 84036      | 09JX | CY6116-45DMB                          | 24.6 DIP               | D12  | 2K x 8 SRAM            |
| 84036      | 09KX | CY7C128-45KMB                         | 24 CP                  | K73  | 2K x 8 SRAM            |
| 84036      | 09LX | CY7C128-45DMB                         | 24.3 DIP               | D14  | 2K x 8 SRAM            |
| 84036      | 09XX | CY6117-45LMB                          | 32 R LCC               | L55  | 2K x 8 SRAM            |
| 84036      | 09YX | CY7C128-45LMB                         | 24 R LCC               | L53  | 2K x 8 SRAM            |
| 84036      | 093X | CY6116-45LMB                          | 28 S LCC               | L64  | 2K x 8 SRAM            |
| 84036      | 11JX | CY6116-55DMB                          | 24.6 DIP               | D12  | 2K x 8 SRAM            |
| 84036      | 11KX | CY7C128-55KMB                         | 24 CP                  | K73  | 2K x 8 SRAM            |
| 84036      | 11LX | CY7C128-55DMB                         | 24.3 DIP               | D14  | 2K x 8 SRAM            |
| 84036      | 11XX | CY6117-55LMB                          | 32 R LCC               | L55  | 2K x 8 SRAM            |
| 84036      | 11YX | CY7C128-55LMB                         | 24 R LCC               | D14  | 2K x 8 SRAM            |
| 84036      | 113X | CY6116-55LMB                          | 28 S LCC               | L64  | 2K x 8 SRAM            |
| 84132      | 02RX | CY7C167-45DMB                         | 20.3 DIP               | D6   | 16K x 1 SRAM           |
| 84132      | 02SX | CY7C167-45KMB                         | 20 CP                  | K71  | 16K x 1 SRAM           |
| 84132      | 02YX | CY7C167-45LMB                         | 20 R LCC               | L51  | 16K x 1 SRAM           |
| 84132      | 05RX | CY7C167-35DMB                         | 20.3 DIP               | D6   | 16K x 1 SRAM           |
| 84132      | 05SX | CY7C167-35KMB                         | 20 CP                  | K71  | 16K x 1 SRAM           |
| 84132      | 05YX | CY7C167-35LMB                         | 20 R LCC               | L51  | 16K x 1 SRAM           |
| 5962-85525 | 05TX | CY7C185-55KMB                         | 28 CP                  | K74  | 8K x 8 SRAM            |
| 5962-85525 | 05UX | CY7C185-55LMB                         | 28 R TLCC              | L54  | 8K x 8 SRAM            |
| 5962-85525 | 05XX | CY7C186-55DMB                         | 28.6 DIP               | D16  | 8K x 8 SRAM            |
| 5962-85525 | 05ZX | CY7C185-55DMB                         | 28.3 DIP               | D22  | 8K x 8 SRAM            |
| 5962-85525 | 06TX | CY7C185-45KMB                         | 28 CP                  | K74  | 8K x 8 SRAM            |
| 5962-85525 | 06UX | CY7C185-45LMB                         | 28 R TLCC              | L54  | 8K x 8 SRAM            |
| 5962-85525 | 06XX | CY7C186-45DMB                         | 28.6 DIP               | D16  | 8K x 8 SRAM            |
| 5962-85525 | 06ZX | CY7C185-45DMB                         | 28.3 DIP               | D22  | 8K x 8 SRAM            |
| 5962-85525 | 07TX | CY7C185-35KMB                         | 28 CP                  | K74  | 8K x 8 SRAM            |
| 5962-85525 | 07UX | CY7C185-35LMB                         | 28 R TLCC              | L54  | 8K x 8 SRAM            |
| 5962-85525 | 07XX | CY7C186-35DMB                         | 28.6 DIP               | D16  | 8K x 8 SRAM            |
| 5962-85525 | 07ZX | CY7C185-35DMB                         | 28.3 DIP               | D22  | 8K x 8 SRAM            |
| 5962-86015 | 01YX | CY7C187-35DMB                         | 22.3 DIP               | D10  | 64K x 1 SRAM           |
| 5962-86015 | 01ZX | CY7C187-35LMB                         | 22 R LCC               | L52  | 64K x 1 SRAM           |
| 5962-86015 | 02YX | CY7C187L-35DMB                        | 22.3 DIP               | D10  | 64K x 1 SRAM           |
| 5962-86015 | 02ZX | CY7C187L-35LMB                        | 22 R LCC               | L52  | 64K x 1 SRAM           |
| 5962-86015 | 03YX | CY7C187-45DMB                         | 22.3 DIP               | D10  | 64K x 1 SRAM           |
| 5962-86015 | 03ZX | CY7C187-45LMB                         | 22 R LCC               | L52  | 64K x 1 SRAM           |
| 5962-86015 | 04YX | CY7C187L-45DMB                        | 22.3 DIP               | D10  | 64K x 1 SRAM           |
| 5962-86015 | 04ZX | CY7C187L-45LMB                        | 22 R LCC               | L52  | 64K x 1 SRAM           |
| 5962-86705 | 12RX | CY7C168-35DMB                         | 20.3 DIP               | D6   | 4K x 4 SRAM            |
| 5962-86705 | 12XX | CY7C168-35LMB                         | 20 R LCC               | L51  | 4K x 4 SRAM            |
| 5962-86859 | 15KX | CY7C166L-45KMB                        | 24 CP                  | K73  | 16K x 4 SRAM W/OE      |
| 5962-86859 | 15LX | CY7C166L-45DMB                        | 24.3 DIP               | D14  | 16K x 4 SRAM W/OE      |
| 5962-86859 | 15UX | CY7C166L-45LMB                        | 28 R LCC               | L54  | 16K x 4 SRAM W/OE      |
| 5962-86859 | 15XX | CY7C166L-45LMB                        | 28 R TLCC              | L54  | 16K x 4 SRAM W/OE      |
| 5962-86859 | 16KX | CY7C166-45KMB                         | 24 CP                  | K73  | 16K x 4 SRAM W/OE      |
| 5962-86859 | 16LX | CY7C166-45DMB                         | 24.3 DIP               | D14  | 16K x 4 SRAM W/OE      |
| 5962-86859 | 16UX | CY7C166-45LMB                         | 28 R LCC               | L54  | 16K x 4 SRAM W/OE      |
| 5962-86859 | 16XX | CY7C166-45LMB                         | 28 R TLCC              | L54  | 16K x 4 SRAM W/OE      |
| 5962-86859 | 17KX | CY7C166L-35KMB                        | 24 CP                  | K73  | 16K x 4 SRAM W/OE      |
| 5962-86859 | 17LX | CY7C166L-35DMB                        | 24.3 DIP               | D14  | 16K x 4 SRAM W/OE      |



# Military Ordering Information (Continued)

## DESC SMD (Standardized Military Drawing) Approvals<sup>[1]</sup> (Continued)

| SMD Number      | Cypress <sup>[2]</sup><br>Part Number | Package <sup>[3]</sup> |      | Product<br>Description |
|-----------------|---------------------------------------|------------------------|------|------------------------|
|                 |                                       | Description            | Type |                        |
| 5962-86859 17UX | CY7C166L-35LMB                        | 28 R LCC               | L54  | 16K x 4 SRAM W/OE      |
| 5962-86859 17XX | CY7C166L-35LMB                        | 28 R TLCC              | L54  | 16K x 4 SRAM W/OE      |
| 5962-86859 18KX | CY7C166-35KMB                         | 24 CP                  | K73  | 16K x 4 SRAM W/OE      |
| 5962-86859 18LX | CY7C166-35DMB                         | 24.3 DIP               | D14  | 16K x 4 SRAM W/OE      |
| 5962-86859 18UX | CY7C166-35LMB                         | 28 R LCC               | L54  | 16K x 4 SRAM W/OE      |
| 5962-86859 18XX | CY7C166-35LMB                         | 28 R TLCC              | L54  | 16K x 4 SRAM W/OE      |
| 5962-86859 21KX | CY7C164L-45KMB                        | 24 CP                  | K73  | 16K x 4 SRAM           |
| 5962-86859 21YX | CY7C164L-45DMB                        | 22.3 DIP               | D10  | 16K x 4 SRAM           |
| 5962-86859 21ZX | CY7C164L-45LMB                        | 22 R LCC               | L52  | 16K x 4 SRAM           |
| 5962-86859 22KX | CY7C164-45KMB                         | 24 CP                  | K73  | 16K x 4 SRAM           |
| 5962-86859 22YX | CY7C164-45DMB                         | 22.3 DIP               | D10  | 16K x 4 SRAM           |
| 5962-86859 22ZX | CY7C164-45LMB                         | 22 R LCC               | L52  | 16K x 4 SRAM           |
| 5962-86859 23KX | CY7C164L-35KMB                        | 24 CP                  | K73  | 16K x 4 SRAM           |
| 5962-86859 23YX | CY7C164L-35DMB                        | 22.3 DIP               | D10  | 16K x 4 SRAM           |
| 5962-86859 23ZX | CY7C164L-35LMB                        | 22 R LCC               | L52  | 16K x 4 SRAM           |
| 5962-86859 24KX | CY7C164-35KMB                         | 24 CP                  | K73  | 16K x 4 SRAM           |
| 5962-86859 24YX | CY7C164-35DMB                         | 22.3 DIP               | D10  | 16K x 4 SRAM           |
| 5962-86859 24ZX | CY7C164-35LMB                         | 22 R LCC               | L52  | 16K x 4 SRAM           |
| 5962-86873 01XX | CY7C516-42DMB                         | 64 DIP                 | D30  | 16 x 16 Multiplier     |
| 5962-86873 01YX | CY7C516-42LMB                         | 68 S LCC               | L81  | 16 x 16 Multiplier     |
| 5962-86873 01ZX | CY7C516-42GMB                         | 68 PGA                 | G68  | 16 x 16 Multiplier     |
| 5962-86873 02XX | CY7C516-55DMB                         | 64 DIP                 | D30  | 16 x 16 Multiplier     |
| 5962-86873 02YX | CY7C516-55LMB                         | 68 S LCC               | L81  | 16 x 16 Multiplier     |
| 5962-86873 02ZX | CY7C516-55GMB                         | 68 PGA                 | G68  | 16 x 16 Multiplier     |
| 5962-86873 03XX | CY7C516-75DMB                         | 64 DIP                 | D30  | 16 x 16 Multiplier     |
| 5962-86873 03YX | CY7C516-75LMB                         | 68 S LCC               | L81  | 16 x 16 Multiplier     |
| 5962-86873 03ZX | CY7C516-75GMB                         | 68 PGA                 | G68  | 16 x 16 Multiplier     |
| 5962-86875 03XX | CY7C130-55DMB                         | 48.6 DIP               | D26  | 1K x 8 Dual Port SRAM  |
| 5962-86875 03YX | CY7C130-55LMB                         | 48 LCC                 | L68  | 1K x 8 Dual Port SRAM  |
| 5962-86875 03ZX | CY7C131-55LMB                         | 52 LCC                 | L69  | 1K x 8 Dual Port SRAM  |
| 5962-86875 04XX | CY7C130-45DMB                         | 48.6 DIP               | D26  | 1K x 8 Dual Port SRAM  |
| 5962-86875 04YX | CY7C130-45LMB                         | 48 LCC                 | L68  | 1K x 8 Dual Port SRAM  |
| 5962-86875 04ZX | CY7C131-45LMB                         | 52 LCC                 | L69  | 1K x 8 Dual Port SRAM  |
| 5962-86875 11XX | CY7C140-55DMB                         | 48.6 DIP               | D26  | 1K x 8 Dual Port SRAM  |
| 5962-86875 11YX | CY7C140-55LMB                         | 48 LCC                 | L68  | 1K x 8 Dual Port SRAM  |
| 5962-86875 11ZX | CY7C141-55LMB                         | 52 LCC                 | L69  | 1K x 8 Dual Port SRAM  |
| 5962-86875 12XX | CY7C140-45DMB                         | 48.6 DIP               | D26  | 1K x 8 Dual Port SRAM  |
| 5962-86875 12YX | CY7C140-45LMB                         | 48 LCC                 | L68  | 1K x 8 Dual Port SRAM  |
| 5962-86875 12ZX | CY7C141-45LMB                         | 52 LCC                 | L69  | 1K x 8 Dual Port SRAM  |
| 5962-86875 17XX | CY7C130-35DMB                         | 48.6 DIP               | D26  | 1K x 8 Dual Port SRAM  |
| 5962-86875 17YX | CY7C130-35LMB                         | 48 LCC                 | L68  | 1K x 8 Dual Port SRAM  |
| 5962-86875 17ZX | CY7C131-35LMB                         | 52 LCC                 | L69  | 1K x 8 Dual Port SRAM  |
| 5962-86875 18XX | CY7C140-35DMB                         | 48.6 DIP               | D26  | 1K x 8 Dual Port SRAM  |
| 5962-86875 18YX | CY7C140-35LMB                         | 48 LCC                 | L68  | 1K x 8 Dual Port SRAM  |
| 5962-86875 18ZX | CY7C141-35LMB                         | 52 LCC                 | L69  | 1K x 8 Dual Port SRAM  |
| 5962-87515 05KX | CY7C261-45TMB                         | 24 CP                  | T73  | 8K x 8 UV EPROM        |
| 5962-87515 05LX | CY7C261-45WMB                         | 24.3 DIP               | W14  | 8K x 8 UV EPROM        |
| 5962-87515 053X | CY7C261-45QMB                         | 28 S LCC               | Q64  | 8K x 8 UV EPROM        |
| 5962-87515 06KX | CY7C261-55TMB                         | 24 CP                  | T73  | 8K x 8 UV EPROM        |
| 5962-87515 06LX | CY7C261-55WMB                         | 24.3 DIP               | W14  | 8K x 8 UV EPROM        |
| 5962-87515 063X | CY7C261-55QMB                         | 28 S LCC               | Q64  | 8K x 8 UV EPROM        |



# Military Ordering Information (Continued)

## DESC SMD (Standardized Military Drawing) Approvals<sup>[1]</sup> (Continued)

| SMD Number      | Cypress <sup>[2]</sup><br>Part Number | Package <sup>[3]</sup> |      | Product<br>Description    |
|-----------------|---------------------------------------|------------------------|------|---------------------------|
|                 |                                       | Description            | Type |                           |
| 5962-87529 01KX | CY7C245-45TMB                         | 24 CP                  | T73  | 2K x 8 Registered UV PROM |
| 5962-87529 01LX | CY7C245-45WMB                         | 24.3 DIP               | W14  | 2K x 8 Registered UV PROM |
| 5962-87529 013X | CY7C245-45QMB                         | 28 S LCC               | Q64  | 2K x 8 Registered UV PROM |
| 5962-87529 02KX | CY7C245-35TMB                         | 24 CP                  | T73  | 2K x 8 Registered UV PROM |
| 5962-87529 02LX | CY7C245-35WMB                         | 24.3 DIP               | W14  | 2K x 8 Registered UV PROM |
| 5962-87529 023X | CY7C245-35QMB                         | 28 S LCC               | Q64  | 2K x 8 Registered UV PROM |
| 5962-87539 01KX | PALC22V10-25TMB                       | 24 CP                  | T73  | 24-Pin CMOS UV E PLD      |
| 5962-87539 01LX | PALC22V10-25WMB                       | 24.3 DIP               | W14  | 24-Pin CMOS UV E PLD      |
| 5962-87539 013X | PALC22V10-25QMB                       | 28 S LCC               | Q64  | 24-Pin CMOS UV E PLD      |
| 5962-87539 02KX | PALC22V10-30TMB                       | 24 CP                  | T73  | 24-Pin CMOS UV E PLD      |
| 5962-87539 02LX | PALC22V10-30WMB                       | 24.3 DIP               | W14  | 24-Pin CMOS UV E PLD      |
| 5962-87539 023X | PALC22V10-30QMB                       | 28 S LCC               | Q64  | 24-Pin CMOS UV E PLD      |
| 5962-87539 03KX | PALC22V10-40TMB                       | 24 CP                  | T73  | 24-Pin CMOS UV E PLD      |
| 5962-87539 03LX | PALC22V10-40WMB                       | 24.3 DIP               | W14  | 24-Pin CMOS UV E PLD      |
| 5962-87539 033X | PALC22V10-40QMB                       | 28 S LCC               | Q64  | 24-Pin CMOS UV E PLD      |
| 5962-87650 01KX | CY7C291-50TMB                         | 24 CP                  | T73  | 2K x 8 UV EPROM           |
| 5962-87650 01LX | CY7C291-50WMB                         | 24.3 DIP               | W14  | 2K x 8 UV EPROM           |
| 5962-87650 013X | CY7C291-50QMB                         | 28 S LCC               | Q64  | 2K x 8 UV EPROM           |
| 5962-87650 03KX | CY7C291-35TMB                         | 24 CP                  | T73  | 2K x 8 UV EPROM           |
| 5962-87650 03LX | CY7C291-35WMB                         | 24.3 DIP               | W14  | 2K x 8 UV EPROM           |
| 5962-87650 033X | CY7C291-35QMB                         | 28 S LCC               | Q64  | 2K x 8 UV EPROM           |
| 5962-87651 01JX | CY7C282-45DMB                         | 24.6 DIP               | D12  | 1K x 8 PROM               |
| 5962-87651 01KX | CY7C281-45KMB                         | 24 CP                  | K73  | 1K x 8 PROM               |
| 5962-87651 01LX | CY7C281-45DMB                         | 24.3 DIP               | D14  | 1K x 8 PROM               |
| 5962-87651 013X | CY7C281-45LMB                         | 28 S LCC               | L64  | 1K x 8 PROM               |
| 5962-87686 01XX | CY7C517-42DMB                         | 64 DIP                 | D30  | 16 x 16 Multiplier        |
| 5962-87686 01YX | CY7C517-42LMB                         | 68 S LCC               | L81  | 16 x 16 Multiplier        |
| 5962-87686 01ZX | CY7C517-42GMB                         | 68 PGA                 | G68  | 16 x 16 Multiplier        |
| 5962-87686 01UX | CY7C517-42FMB                         | 64 Q FP                | F78  | 16 x 16 Multiplier        |
| 5962-87686 02XX | CY7C517-55DMB                         | 64 DIP                 | D30  | 16 x 16 Multiplier        |
| 5962-87686 02YX | CY7C517-55LMB                         | 68 S LCC               | L81  | 16 x 16 Multiplier        |
| 5962-87686 02ZX | CY7C517-55GMB                         | 68 PGA                 | G68  | 16 x 16 Multiplier        |
| 5962-87686 02UX | CY7C517-55FMB                         | 64 Q FP                | F78  | 16 x 16 Multiplier        |
| 5962-87686 03XX | CY7C517-75DMB                         | 64 DIP                 | D30  | 16 x 16 Multiplier        |
| 5962-87686 03YX | CY7C517-75LMB                         | 68 S LCC               | L81  | 16 x 16 Multiplier        |
| 5962-87686 03ZX | CY7C517-75GMB                         | 68 PGA                 | G68  | 16 x 16 Multiplier        |
| 5962-87686 03UX | CY7C517-75FMB                         | 64 Q FP                | F78  | 16 x 16 Multiplier        |
| 5962-87518 01LX | CY7C225-30DMB                         | 24.3 DIP               | D14  | 512 x 8 Registered PROM   |
| 5962-87518 013X | CY7C225-30LMB                         | 28 S LCC               | L64  | 512 x 8 Registered PROM   |
| 5962-87518 02LX | CY7C225-35DMB                         | 24.3 DIP               | D14  | 512 x 8 Registered PROM   |
| 5962-87518 023X | CY7C225-35LMB                         | 28 S LCC               | L64  | 512 x 8 Registered PROM   |
| 5962-87518 03LX | CY7C225-40DMB                         | 24.3 DIP               | D14  | 512 x 8 Registered PROM   |
| 5962-87518 033X | CY7C225-40LMB                         | 28 S LCC               | L64  | 512 x 8 Registered PROM   |
| 5962-88535 01QX | CY7C901-32DMB                         | 40.6 DIP               | D18  | 4-Bit Slice               |
| 5962-88535 01XX | CY7C901-32LMB                         | 44 LCC                 | L67  | 4-Bit Slice               |
| 5962-88535 01YX | CY7C901-32FMB                         | 42 FP                  | F76  | 4-Bit Slice               |
| 5962-88535 02QX | CY7C901-27DMB                         | 40.6 DIP               | D18  | 4-Bit Slice               |
| 5962-88535 02XX | CY7C901-27LMB                         | 44 LCC                 | L67  | 4-Bit Slice               |
| 5962-88535 02YX | CY7C901-27FMB                         | 42 FP                  | F76  | 4-Bit Slice               |





# Military Ordering Information (Continued)

## DESC SMD (Standardized Military Drawing) Approvals<sup>[1]</sup> (Continued)

| SMD Number      | Cypress <sup>[2]</sup><br>Part Number | Package <sup>[3]</sup> |      | Product<br>Description     |
|-----------------|---------------------------------------|------------------------|------|----------------------------|
|                 |                                       | Description            | Type |                            |
| 5962-88587 01VX | CY7C147-45DMB                         | 18.3 DIP               | D4   | 4K x 1 SRAM                |
| 5962-88587 01XX | CY7C147-45KMB                         | 18 CP                  | K70  | 4K x 1 SRAM                |
| 5962-88587 01YX | CY7C147-45LMB                         | 18 R LCC               | L50  | 4K x 1 SRAM                |
| 5962-88587 02VX | CY7C147-35DMB                         | 18.3 DIP               | D4   | 4K x 1 SRAM                |
| 5962-88587 02XX | CY7C147-35KMB                         | 18 CP                  | K70  | 4K x 1 SRAM                |
| 5962-88587 02YX | CY7C147-35LMB                         | 18 R LCC               | L50  | 4K x 1 SRAM                |
| 5962-88588 01KX | CY7C150-35KMB                         | 24 CP                  | K73  | 1K x 4 SRAM with Reset     |
| 5962-88588 01LX | CY7C150-35DMB                         | 24.3 DIP               | D14  | 1K x 4 SRAM with Reset     |
| 5962-88588 01XX | CY7C150-35LMB                         | 28 R LCC               | L54  | 1K x 4 SRAM with Reset     |
| 5962-88588 02KX | CY7C150-25KMB                         | 24 CP                  | K73  | 1K x 4 SRAM with Reset     |
| 5962-88588 02LX | CY7C150-25DMB                         | 24.3 DIP               | D14  | 1K x 4 SRAM with Reset     |
| 5962-88588 02XX | CY7C150-25LMB                         | 28 R LCC               | L54  | 1K x 4 SRAM with Reset     |
| 5962-88588 03KX | CY7C150-15KMB                         | 24 CP                  | K73  | 1K x 4 SRAM with Reset     |
| 5962-88588 03LX | CY7C150-15DMB                         | 24.3 DIP               | D14  | 1K x 4 SRAM with Reset     |
| 5962-88588 03XX | CY7C150-15LMB                         | 28 R LCC               | L54  | 1K x 4 SRAM with Reset     |
| 5962-88594 02WX | CY7C122-35DMB                         | 22.4 DIP               | D8   | 256 x 4 SRAM               |
| 5962-88594 03WX | CY7C122-25DMB                         | 22.4 DIP               | D8   | 256 x 4 SRAM               |
| 5962-88612 01XX | CY7C9116-99DMB                        | 52.8 DIP               | D28  | 16-Bit Microprogrammed ALU |
| 5962-88612 01YX | CY7C9116-99FMB                        | 64 FP                  | F78  | 16-Bit Microprogrammed ALU |
| 5962-88612 01UX | CY7C9116-99LMB                        | 52 S LCC               | L69  | 16-Bit Microprogrammed ALU |
| 5962-88612 02XX | CY7C9116-75DMB                        | 52.8 DIP               | D28  | 16-Bit Microprogrammed ALU |
| 5962-88612 02YX | CY7C9116-75FMB                        | 64 FP                  | F78  | 16-Bit Microprogrammed ALU |
| 5962-88612 02UX | CY7C9116-75LMB                        | 52 S LCC               | L69  | 16-Bit Microprogrammed ALU |
| 5962-88612 03XX | CY7C9116-65DMB                        | 52.8 DIP               | D28  | 16-Bit Microprogrammed ALU |
| 5962-88612 03YX | CY7C9116-65FMB                        | 64 FP                  | F78  | 16-Bit Microprogrammed ALU |
| 5962-88612 03UX | CY7C9116-65LMB                        | 52 S LCC               | L69  | 16-Bit Microprogrammed ALU |
| 5962-88636 01KX | CY7C235-40KMB                         | 24 CP                  | K73  | 1K x 8 Registered PROM     |
| 5962-88636 01LX | CY7C235-40DMB                         | 24.3 DIP               | D14  | 1K x 8 Registered PROM     |
| 5962-88636 013X | CY7C235-40LMB                         | 28 S LCC               | L64  | 1K x 8 Registered PROM     |
| 5962-88636 02KX | CY7C235-30KMB                         | 24 CP                  | K73  | 1K x 8 Registered PROM     |
| 5962-88636 02LX | CY7C235-30DMB                         | 24.3 DIP               | D14  | 1K x 8 Registered PROM     |
| 5962-88636 023X | CY7C235-30LMB                         | 28 S LCC               | L64  | 1K x 8 Registered PROM     |
| 5962-88637 01KX | PLDC20G10-40KMB                       | 24 CP                  | K73  | Generic CMOS PLD           |
| 5962-88637 01LX | PLDC20G10-40DMB                       | 24.3 DIP               | D14  | Generic CMOS PLD           |
| 5962-88637 013X | PLDC20G10-40LMB                       | 28 S LCC               | L64  | Generic CMOS PLD           |
| 5962-88637 02KX | PLDC20G10-30KMB                       | 24 CP                  | K73  | Generic CMOS PLD           |
| 5962-88637 02LX | PLDC20G10-30DMB                       | 24.3 DIP               | D14  | Generic CMOS PLD           |
| 5962-88637 023X | PLDC20G10-30LMB                       | 28 S LCC               | L64  | Generic CMOS PLD           |
| 5962-88670 01KX | PALC22V10-25KMB                       | 24 CP                  | K73  | 24-Pin CMOS PLD            |
| 5962-88670 01LX | PALC22V10-25DMB                       | 24.3 DIP               | D14  | 24-Pin CMOS PLD            |
| 5962-88670 013X | PALC22V10-25LMB                       | 28 S LCC               | L64  | 24-Pin CMOS PLD            |
| 5962-88670 02KX | PALC22V10-30KMB                       | 24 CP                  | K73  | 24-Pin CMOS PLD            |
| 5962-88670 02LX | PALC22V10-30DMB                       | 24.3 DIP               | D14  | 24-Pin CMOS PLD            |
| 5962-88670 023X | PALC22V10-30LMB                       | 28 S LCC               | L64  | 24-Pin CMOS PLD            |
| 5962-88670 03KX | PALC22V10-40KMB                       | 24 CP                  | K73  | 24-Pin CMOS PLD            |
| 5962-88670 03LX | PALC22V10-40DMB                       | 24.3 DIP               | D14  | 24-Pin CMOS PLD            |
| 5962-88670 033X | PALC22V10-40LMB                       | 28 S LCC               | L64  | 24-Pin CMOS PLD            |



# Military Ordering Information (Continued)

## DESC SMD (Standardized Military Drawing) Approvals<sup>[1]</sup> (Continued)

| SMD Number      | Cypress <sup>[2]</sup><br>Part Number | Package <sup>[3]</sup> |      | Product<br>Description |
|-----------------|---------------------------------------|------------------------|------|------------------------|
|                 |                                       | Description            | Type |                        |
| 5962-88678 01RX | PALC16L8-40WMB                        | 20.3 DIP               | W6   | 20-Pin CMOS UV E PLD   |
| 5962-88678 01XX | PALC16L8-40QMB                        | 20 S LCC               | Q61  | 20-Pin CMOS UV E PLD   |
| 5962-88678 02RX | PALC16R8-40WMB                        | 20.3 DIP               | W6   | 20-Pin CMOS UV E PLD   |
| 5962-88678 02XX | PALC16R8-40QMB                        | 20 S LCC               | Q61  | 20-Pin CMOS UV E PLD   |
| 5962-88678 03RX | PALC16R6-40WMB                        | 20.3 DIP               | W6   | 20-Pin CMOS UV E PLD   |
| 5962-88678 03XX | PALC16R6-40QMB                        | 20 S LCC               | Q61  | 20-Pin CMOS UV E PLD   |
| 5962-88678 04RX | PALC16R4-40WMB                        | 20.3 DIP               | W6   | 20-Pin CMOS UV E PLD   |
| 5962-88678 04XX | PALC16R4-40QMB                        | 20 S LCC               | Q61  | 20-Pin CMOS UV E PLD   |
| 5962-88678 05RX | PALC16L8-30WMB                        | 20.3 DIP               | W6   | 20-Pin CMOS UV E PLD   |
| 5962-88678 05XX | PALC16L8-30QMB                        | 20 S LCC               | Q61  | 20-Pin CMOS UV E PLD   |
| 5962-88678 06RX | PALC16R8-30WMB                        | 20.3 DIP               | W6   | 20-Pin CMOS UV E PLD   |
| 5962-88678 06XX | PALC16R8-30QMB                        | 20 S LCC               | Q61  | 20-Pin CMOS UV E PLD   |
| 5962-88678 07RX | PALC16R6-30WMB                        | 20.3 DIP               | W6   | 20-Pin CMOS UV E PLD   |
| 5962-88678 07XX | PALC16R6-30QMB                        | 20 S LCC               | Q61  | 20-Pin CMOS UV E PLD   |
| 5962-88678 08RX | PALC16R4-30WMB                        | 20.3 DIP               | W6   | 20-Pin CMOS UV E PLD   |
| 5962-88678 08XX | PALC16R4-30QMB                        | 20 S LCC               | Q61  | 20-Pin CMOS UV E PLD   |
| 5962-88678 09RX | PALC16L8-20WMB                        | 20.3 DIP               | W6   | 20-Pin CMOS UV E PLD   |
| 5962-88678 09XX | PALC16L8-20QMB                        | 20 S LCC               | Q61  | 20-Pin CMOS UV E PLD   |
| 5962-88678 10RX | PALC16R8-20WMB                        | 20.3 DIP               | W6   | 20-Pin CMOS UV E PLD   |
| 5962-88678 10XX | PALC16R8-20QMB                        | 20 S LCC               | Q61  | 20-Pin CMOS UV E PLD   |
| 5962-88678 11RX | PALC16R6-20WMB                        | 20.3 DIP               | W6   | 20-Pin CMOS UV E PLD   |
| 5962-88678 11XX | PALC16R6-20QMB                        | 20 S LCC               | Q61  | 20-Pin CMOS UV E PLD   |
| 5962-88678 12RX | PALC16R4-20WMB                        | 20.3 DIP               | W6   | 20-Pin CMOS UV E PLD   |
| 5962-88678 12XX | PALC16R4-20QMB                        | 20 S LCC               | Q61  | 20-Pin CMOS UV E PLD   |
| 5962-88713 01RX | PALC16L8-40DMB                        | 20.3 DIP               | D6   | 20-Pin CMOS PLD        |
| 5962-88713 01SX | PALC16L8-40KMB                        | 20 CP                  | K71  | 20-Pin CMOS PLD        |
| 5962-88713 01XX | PALC16L8-40LMB                        | 20 S LCC               | L61  | 20-Pin CMOS PLD        |
| 5962-88713 02RX | PALC16R8-40DMB                        | 20.3 DIP               | D6   | 20-Pin CMOS PLD        |
| 5962-88713 02SX | PALC16R8-40KMB                        | 20 CP                  | K71  | 20-Pin CMOS PLD        |
| 5962-88713 02XX | PALC16R8-40LMB                        | 20 S LCC               | L61  | 20-Pin CMOS PLD        |
| 5962-88713 03RX | PALC16R6-40DMB                        | 20.3 DIP               | D6   | 20-Pin CMOS PLD        |
| 5962-88713 03SX | PALC16R6-40KMB                        | 20 CP                  | K71  | 20-Pin CMOS PLD        |
| 5962-88713 03XX | PALC16R6-40LMB                        | 20 S LCC               | L61  | 20-Pin CMOS PLD        |
| 5962-88713 04RX | PALC16R4-40DMB                        | 20.3 DIP               | D6   | 20-Pin CMOS PLD        |
| 5962-88713 04SX | PALC16R4-40KMB                        | 20 CP                  | K71  | 20-Pin CMOS PLD        |
| 5962-88713 04XX | PALC16R4-40LMB                        | 20 S LCC               | L61  | 20-Pin CMOS PLD        |
| 5962-88713 05RX | PALC16L8-30DMB                        | 20.3 DIP               | D6   | 20-Pin CMOS PLD        |
| 5962-88713 05SX | PALC16L8-30KMB                        | 20 CP                  | K71  | 20-Pin CMOS PLD        |
| 5962-88713 05XX | PALC16L8-30LMB                        | 20 S LCC               | L61  | 20-Pin CMOS PLD        |
| 5962-88713 06RX | PALC16R8-30DMB                        | 20.3 DIP               | D6   | 20-Pin CMOS PLD        |
| 5962-88713 06SX | PALC16R8-30KMB                        | 20 CP                  | K71  | 20-Pin CMOS PLD        |
| 5962-88713 06XX | PALC16R8-30LMB                        | 20 S LCC               | L61  | 20-Pin CMOS PLD        |
| 5962-88713 07RX | PALC16R6-30DMB                        | 20.3 DIP               | D6   | 20-Pin CMOS PLD        |
| 5962-88713 07SX | PALC16R6-30KMB                        | 20 CP                  | K71  | 20-Pin CMOS PLD        |
| 5962-88713 07XX | PALC16R6-30LMB                        | 20 S LCC               | L61  | 20-Pin CMOS PLD        |
| 5962-88713 08RX | PALC16R4-30DMB                        | 20.3 DIP               | D6   | 20-Pin CMOS PLD        |
| 5962-88713 08SX | PALC16R4-30KMB                        | 20 CP                  | K71  | 20-Pin CMOS PLD        |
| 5962-88713 08XX | PALC16R4-30LMB                        | 20 S LCC               | L61  | 20-Pin CMOS PLD        |
| 5962-88713 09RX | PALC16L8-20DMB                        | 20.3 DIP               | D6   | 20-Pin CMOS PLD        |
| 5962-88713 09SX | PALC16L8-20KMB                        | 20 CP                  | K71  | 20-Pin CMOS PLD        |
| 5962-88713 09XX | PALC16L8-20LMB                        | 20 S LCC               | L61  | 20-Pin CMOS PLD        |
| 5962-88713 10RX | PALC16R8-20DMB                        | 20.3 DIP               | D6   | 20-Pin CMOS PLD        |
| 5962-88713 10SX | PALC16R8-20KMB                        | 20 CP                  | K71  | 20-Pin CMOS PLD        |
| 5962-88713 10XX | PALC16R8-20LMB                        | 20 S LCC               | L61  | 20-Pin CMOS PLD        |



# Military Ordering Information (Continued)

## DESC SMD (Standardized Military Drawing) Approvals<sup>[1]</sup> (Continued)

| SMD Number      | Cypress <sup>[2]</sup><br>Part Number | Package <sup>[3]</sup> |      | Product<br>Description |
|-----------------|---------------------------------------|------------------------|------|------------------------|
|                 |                                       | Description            | Type |                        |
| 5962-88713 11RX | PALC16R6-20DMB                        | 20.3 DIP               | D6   | 20-Pin CMOS PLD        |
| 5962-88713 11SX | PALC16R6-20KMB                        | 20 CP                  | K71  | 20-Pin CMOS PLD        |
| 5962-88713 11XX | PALC16R6-20LMB                        | 20 S LCC               | L61  | 20-Pin CMOS PLD        |
| 5962-88713 12RX | PALC16R4-20DMB                        | 20.3 DIP               | D6   | 20-Pin CMOS PLD        |
| 5962-88713 12SX | PALC16R4-20KMB                        | 20 CP                  | K71  | 20-Pin CMOS PLD        |
| 5962-88713 12XX | PALC16R4-20LMB                        | 20 S LCC               | L61  | 20-Pin CMOS PLD        |
| 5962-88735 01KX | CY7C245-45KMB                         | 24 CP                  | K73  | 2K x 8 Registered PROM |
| 5962-88735 01LX | CY7C245-45DMB                         | 24.3 DIP               | D14  | 2K x 8 Registered PROM |
| 5962-88735 013X | CY7C245-45LMB                         | 28 S LCC               | L64  | 2K x 8 Registered PROM |
| 5962-88735 02KX | CY7C245-35KMB                         | 24 CP                  | K73  | 2K x 8 Registered PROM |
| 5962-88735 02LX | CY7C245-35DMB                         | 24.3 DIP               | D14  | 2K x 8 Registered PROM |
| 5962-88735 023X | CY7C245-35LMB                         | 28 S LCC               | L64  | 2K x 8 Registered PROM |
| 5962-88735 03KX | CY7C245A-35KMB                        | 24 CP                  | K73  | 2K x 8 Registered PROM |
| 5962-88735 03LX | CY7C245A-35DMB                        | 24.3 DIP               | D14  | 2K x 8 Registered PROM |
| 5962-88735 033X | CY7C245A-35LMB                        | 28 S LCC               | L64  | 2K x 8 Registered PROM |
| 5962-88735 04KX | CY7C245A-25KMB                        | 24 CP                  | K73  | 2K x 8 Registered PROM |
| 5962-88735 04LX | CY7C245A-25DMB                        | 24.3 DIP               | D14  | 2K x 8 Registered PROM |
| 5962-88735 043X | CY7C245A-25LMB                        | 28 S LCC               | L64  | 2K x 8 Registered PROM |

**Notes:**

- SMD approvals are continually being updated. Contact your local Cypress representative for the latest update.
- Use the SMD part number as the ordering code.
- Package: 24.3 DIP = 24-pin 0.300" DIP; 24.6 DIP = 24-pin 0.600" DIP  
 28 R LCC = 28 terminal Rectangular LCC; S = Square LCC; TLCC = Thin LCC  
 24 CP = 24-pin Ceramic flatpack (Configuration 1); FP = Brazed flatpack  
 PGA = Pin Grid Array

## SMD Ordering Information

**5962-8XXXX 01 L X**

LEAD FINISH

A = Solder Dip

B = Tin Plate

C = Gold

X = Don't Care (The letter "X" will not be marked on the device, but will be replaced with the applicable lead finish designation.)

PACKAGE TYPE (Not a complete list)

V = 18-pin 0.300 DIP      J = 24-pin 0.600 DIP

R = 20-pin 0.300 DIP      Q = 40-pin 0.600 DIP

S = 20-pin Cerpack      K = 24-pin Cerpack

W = 22-pin 0.400 DIP      2 = 20-pin SQ LCC

L = 24-pin 0.300 DIP      3 = 28-pin SQ LCC

X, Y, Z, U, T, N = Non-dedicated package designations and will vary per drawing.

DEVICE TYPE

01 = 7CXXX XX ns

02 = 7CXXX XX ns

DRAWING NUMBER

DRAWING PREFIX

5962 = Microcircuits (Pre-1985 drawings do not have this prefix.)



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## BridgeMOS

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### Device Number

### Description

|         |   |      |
|---------|---|------|
| CY8C150 | BridgeMOS 1024 x 4 Static RAM Separate I/O .....        | 10-1 |
| CY8C245 | BridgeMOS 2048 x 8 Reprogrammable Registered PROM ..... | 10-1 |
| CY8C291 | BridgeMOS Reprogrammable 2048 x 8 PROM .....            | 10-1 |
| CY8C901 | BridgeMOS 4-Bit Slice .....                             | 10-1 |
| CY8C909 | BridgeMOS Microprogram Sequencer .....                  | 10-1 |
| CY8C911 | BridgeMOS Microprogram Sequencer .....                  | 10-1 |







### Features

- May be driven by CMOS or TTL
- Drives fully loaded TTL
  - Inputs switch at 1.5V
- Can drive CMOS to full input levels
  - $V_{OL} = 0.2V @ I_{OL} = 20 \mu A$
  - $V_{OH} = 0.9 V_{CC} @ I_{OH} = -20 \mu A$
- SRAM, PROM, LOGIC
- 2.0V ( $V_{CC}$ ) Data Retention on all devices

### Overview

The BridgeMOS™ product line from Cypress Semiconductor provides an electrical bridge between CMOS and TTL or TTL and CMOS devices.

BridgeMOS devices may be driven by either TTL or CMOS devices and in turn can drive either fully loaded TTL or CMOS to full input levels. As a result, any combination of TTL and/or CMOS may be interfaced to Cypress BridgeMOS products.

All devices in the BridgeMOS product line are specified at a 2.0V ( $V_{CC}$ ) standby mode of operation. This allows the device to be powered at 2.0 volts and maintain the integrity of the data in any volatile storage element.

The output drivers in the 7CXXX Cypress products are designed for TTL signals and pull up to 2.4 volts. For

BridgeMOS, Cypress has designed an output driver which boosts the output voltage sufficiently to drive the inputs of a device to greater than 3.85 volts, thus guaranteeing that the input converter will draw minimum power. The output drivers source 20 microamps at their rated BridgeMOS levels. They will also source and drive normal TTL loads. Therefore, they are capable of driving other non-BridgeMOS loads and normal TTL loads at the same time.

Although the TTL to CMOS input converters power down as described above, they switch at TTL levels and all timing is referenced to 1.5 volts. The device will operate at normal TTL levels with no AC performance degradation.

### CY8C150 Selection Guide

|                                |            | 8C150-15 | 8C150-25 | 8C150-35 |
|--------------------------------|------------|----------|----------|----------|
| Maximum Access Time (ns)       | Commercial | 15       | 25       | 35       |
|                                | Military   |          | 25       | 35       |
| Maximum Operating Current (mA) | Commercial | 100      | 100      | 100      |
|                                | Military   |          | 125      | 125      |

### CY8C245 Selection Guide

|                                |            | 8C245-35 | 8C245-45 |
|--------------------------------|------------|----------|----------|
| Maximum Access Time (ns)       |            | 35       | 50       |
| Maximum Operating Current (mA) | Commercial | 45       | 45       |
|                                | Military   | 80       | 80       |

### CY8C291 Selection Guide

|                                |            | 8C291-35 | 8C291-50 |
|--------------------------------|------------|----------|----------|
| Maximum Access Time (ns)       |            | 35       | 50       |
| Maximum Operating Current (mA) | Commercial | 45       | 45       |
|                                | Military   | 80       | 80       |

### CY8C901 Selection Guide

| Read Modify-Write Cycle (min.) in ns | Operating I <sub>CC</sub> (max.) in mA | Operating Range | Part Number |
|--------------------------------------|--|-----------------|-------------|
| 31                                   | 26.5                                   | Commercial      | 8C901-31    |
| 32                                   | 31.0                                   | Military        | 8C901-32    |

### CY8C909/8C911 Selection Guide

|   | 8C909-30<br>8C911-30 | 8C909-40<br>8C911-40 |
|---|----------------------|----------------------|
| Minimum Clock to Output Cycle Time (ns) | 30                   | 40                   |
| Maximum Operating Current (mA)          | 15                   | 15                   |

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## QuickPro

### Device Number

CY3000

### Description

Combined PROM, PLD, and EPROM Programmer ..... 11-1

### Page Number





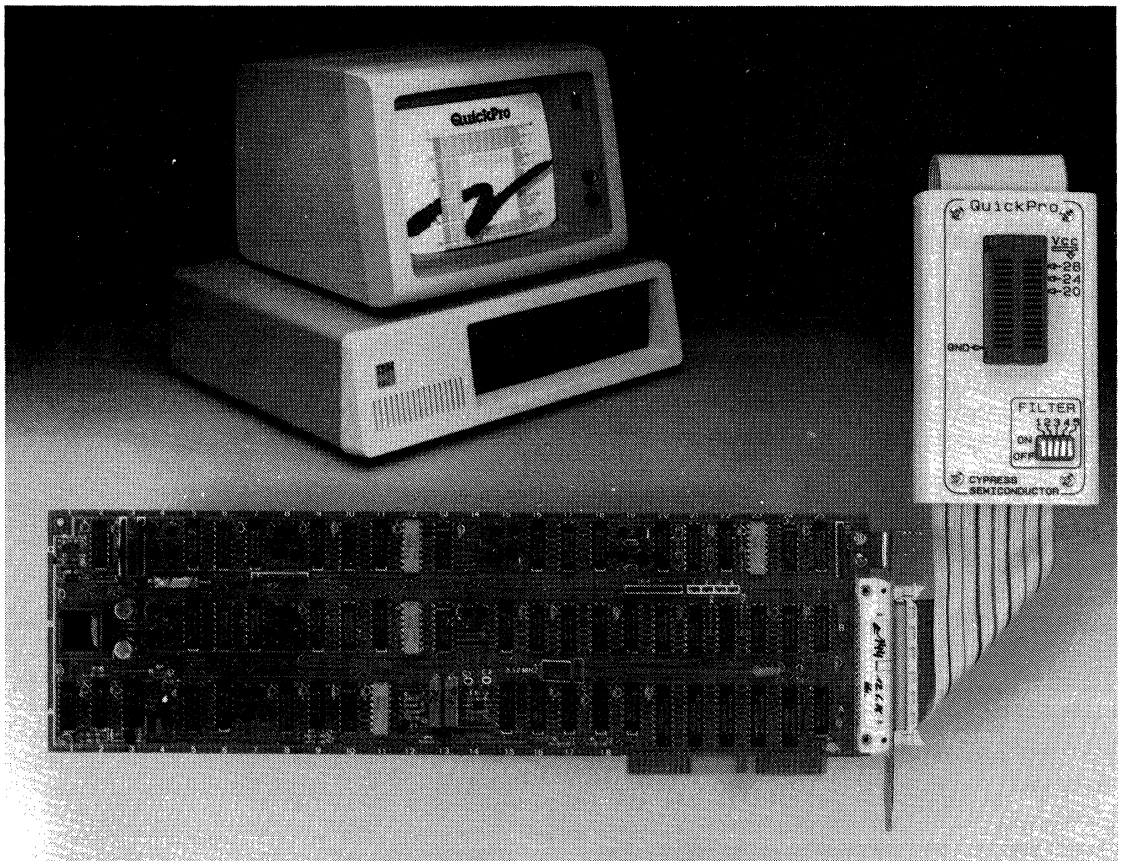
### Features

- Combined PROM, PLD, and EPROM programmer
- Programs Cypress CMOS PLDs and PROMs
- Reads bipolar PLDs and PROMs
- Easy to use, menu-driven software
- New device updates via floppy disk
- IBM-PC® plug-in card format, external ZIF-DIP socket
- Compatible with the IBM PC family of computers and plug compatibles
- Programs 24- and 28-pin NMOS and CMOS EPROMs
- One long slot and 256K bytes of memory required
- Designed for present and future NMOS and CMOS devices
- Optional LCC, PLCC, SOIC socket adapters

### Description

QuickPro is a development tool for present and future CMOS PROM and PLD devices, and is used within the IBM PC and compatible environment. Older generation bipolar PLDs and PROMs required special programming voltages and current difficult to generate within the IBM PC.

QuickPro is designed for new generation of CMOS PLDs and PROMs which obsolete the older technology, and use a programming technique



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IBM and IBM PC are registered trademarks of International Business Machines Corporation.  
ABEL™ is a registered trademark of Data I/O Corporation.  
CUPL™ is a registered trademark of Assisted Technology.  
PALASM™ is a registered trademark of Monolithic Memories Inc.  
Intellec 86™ is a trademark of Intel Corporation.

0095-1



## Description (Continued)

which is more compatible with low cost programming methods.

QuickPro can also program standard NMOS and CMOS EPROMs in packages up to 28 pins. And QuickPro is fast; intelligent programming is used to reduce programming time to a minimum.

QuickPro is future oriented. Each I/O pin is fully programmable, allowing the parameters and timing of each device to be handled via software. As new devices become available, they will be supported by QuickPro. Updates are managed by a simple exchange of floppy disks.

QuickPro includes a comprehensive set of commands to make programming PLDs and PROMs as easy as possible.

For PLDs, QuickPro uses the JEDEC standard data format, so present and future logic design tools such as ABEL™, CUPL™, and PALASM™ can be used. QuickPro avoids serial download problems from a PC to a stand-alone programmer. For PROMs, QuickPro reads Intellec 86™, Motorola S, TEK and space format files. QuickPro also reads and writes PROM PCDOS binary files for use with assemblers and compilers. QuickPro is low cost. Each workstation can have one, eliminating the inconvenience of sharing one expensive programmer. All actions are menu-driven, with complete explanations provided on-screen, in clear text. There is no need to look up manufacturer's codes in a table.

## QuickPro Commands

|                             |                       |
|-----------------------------|-----------------------|
| Program device              | Write disk file       |
| Select device type          | Verify device         |
| Edit memory                 | Blank check device    |
| Display memory              | Program security fuse |
| Change PROM memory location | Fill memory           |
| Read device                 | Convert PLD type      |
| Test PLD device             | Summary display       |
| Read disk file              |                       |

## Technical Information

### Size

IBM PC standard full length card. Selectable port addresses 300–31F, 320–33F, 340–35F, 360–37F hex.

### Power

|       |                                |
|-------|--------------------------------|
| + 5V  | 1.0 amp                        |
| + 12V | 1.0 amp (peak) 0.4 amp average |
| - 12V | 0.05 amp                       |

### Socket Pod

This is the external socket for connection to the device to be programmed or read. It provides a 28-pin 300/600 mil socket for compatibility with a wide range of devices. Other adapters for leadless packages are also available. Five filter switches are located on the pod for bypass capacitors according to manufacturers' published programming specifications.

## Memory

256K bytes of total memory is sufficient to operate QuickPro.

## Devices Supported

Cypress CMOS PROMs:

CY7C225, CY7C235, CY7C245, CY7C245A, CY7C251, CY7C254, CY7C261, CY7C263, CY7C264, CY7C268, CY7C269, CY7C271, CY7C274, CY7C277, CY7C279, CY7C281, CY7C282, CY7C291, CY7C291A, CY7C292, CY7C292A, CY7C293A

Cypress CMOS PLDs:

PALC16L8, PALC16R4, PALC16R6, PALC16R8, PALC22V10, PLDC20G10, PLDC20RA10, CY7C330, CY7C331, CY7C332

QuickPro can read 20 and 24 pin Bipolar PLDs, for conversion to Cypress PLDs.

EPROMs: (NMOS and CMOS)

2716, 2732, 2732A, 2764, 2764A, 27128, 27256, 27512

## Ordering Information

CY3000 QuickPro System (\$995.00) contains:

CY3001 QuickPro Board

CY3002 QuickPro Pod

CY3003 QuickPro System Disc  
Quick Pro Manual

Optional QuickPro Package Adaptors Include:

CY3004 (CY3006) 28 Lead Square (P)LCC:\*  
7C225, 7C235, 7C245, 7C261, 7C263, 7C264, 7C281, 7C282, 7C291, 7C292, PALC22V10

CY3005 (CY3007) 20 Lead Square (P)LCC:  
16L8, 16R4, 16R6, 16R8

CY3008 (CY3009) 28 Lead Square (P)LCC:  
7C269, 7C271, 7C330, 7C331, 7C332

CY3010 (CY3011) 28 Lead Square (P)LCC:  
PLDC20G10

CY3012 (CY3013) 32 Lead Rectangular (P)LCC:  
7C268

CY3014 28 Pin SOIC:  
7C225, 7C235, 7C245, 7C251, 7C254, 7C261, 7C263, 7C264, 7C269, 7C271, 7C281, 7C282, 7C291, 7C292

CY3015 32 Pin SOIC:  
7C268

CY3016 32 Pin DIP:  
7C268

CY3017 (CY3018) 28 Lead Square (P)LCC:  
7C251, 7C254

\*Switch Settings

A = PALC22V10, B = PROMs

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## PLD ToolKit

## Page Number

CY3101

Programmable Logic Design Tool ..... 12-1





## Features

- Logic Assembler, Reverse Assembler
- Concise easy to use syntax
- JEDEC read/write capability
- Integrated Waveform Logic Simulator
- Mouse Driven Simulation Editor
- Integrated menu oriented user interface
- Mouse, keyboard, command line interface
- CGA, EGA, VGA, Hercules support
- Supports all Cypress PLDs

## Description

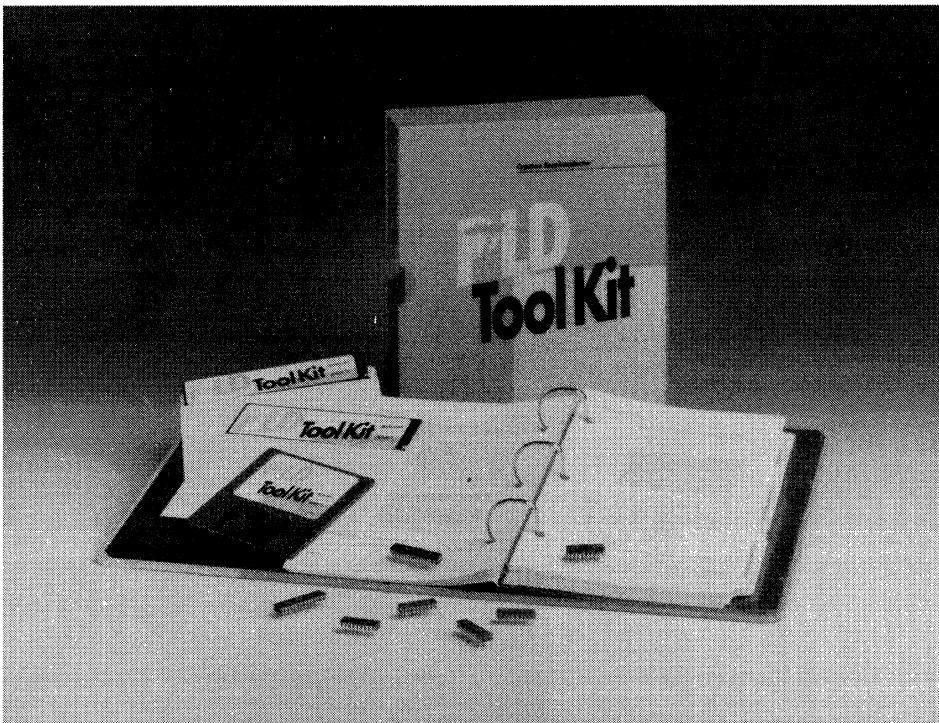
The Cypress PLD ToolKit is a sophisticated programmable logic design tool for supporting the Cypress family of programmable logic products. The ToolKit includes the ability to assemble a logic source file, interactively perform logic simulation on the result, and write a standard JEDEC output file for programming the PLD. In addition, JEDEC files may be read, simulated and reverse assembled, creating source files that may be modified and re-assembled.

The PLD ToolKit runs on any standard IBM PC®, AT®, 386 or compatible Personal Computer with a CGA, EGA, VGA or Hercules display. The ToolKit features mouse, keyboard or command line interface and supports Logitech™ and Microsoft® mouse

compatibility. Command line control is provided for assembly from a source file to JEDEC file or disassembly of a JEDEC file to a source file.

The language contains syntax that allows the management of programmable logic device macrocells in all possible configurations, as well as default conditions that provide concise source files. In addition, there are language constructs called connectives that provide expressions for connecting any product term to a macrocell.

The ToolKit Simulator features waveform entry, multiple views and multi-segment simulation. The Simulator provides the capability to specify initial design conditions, and "View Nodes" may be created and used to probe internal nodes in the device.



## PLD ToolKit Command Menus

### Mouse Test

If no response, then check mouse installation Provides the ability to test Mouse Interface

Supports Logitech and Microsoft

ESCAPE

### Command Menu

Assemble Invokes Assembles  
 Disassemble Invokes Disassembler  
 Write JEDEC Writes JEDEC Output File  
 Read JEDEC Reads JEDEC File into PLD ToolKit

Simulate Invokes Simulator  
 Options Selects Option Menu  
 Information Selects System Information Menu

Clear Resets ToolKit

ESCAPE

### Information

Release Number Information about the PLD ToolKit for registration purposes  
 Release Date  
 Serial Number  
 Free Memory  
 Screen Size  
 Colors

ESCAPE

### Options

Simulation Colors Selects Simulation Colors Menu

Menu Colors Selects Menu Color Menu

JEDEC Brief/Annotate Toggles JEDEC Annotated or Brief Listing

G Fuse (JEDEC Security): ON/OFF Toggles Security Fuse

Working Directory Path ( ) Sets Path to Working Directory

ESCAPE

### Simulation Colors

Background Allows the selection of colors for the Simulator Display  
 Input Trace  
 Output Trace

Name of Pin or Node

Pin or Node Background

Trace Selected

Selected Trace Background

### Memory

512K bytes of total memory is required to operate the PLD ToolKit.

### Devices Supported

CYPAL16R8, CYPAL16R6, CYPAL16R4, CYPAL16L8, CYPAL22V10, CYPLD20G10, CY7C330, CY7C331

### Ordering Information

CY3101 Cypress PLD ToolKit Level 1 contains:

Two 5 $\frac{1}{4}$ " Floppy Disks  
 One 3 $\frac{1}{2}$ " Floppy Disk  
 One Manual  
 One Registration Card

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## Quality and Reliability

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# Quality, Reliability and Process Flows

## Corporate Views on Quality and Reliability

Cypress believes in product excellence. Excellence can only be defined by how the users perceive both our product quality and reliability. If you, the user, are not satisfied with every device that is shipped, then product excellence has not been achieved.

Product excellence does not occur by following the industry norms. It begins by being better than one's competitors, with better designs, processes, controls and materials. Therefore, product quality and reliability are built into every Cypress product from the start.

Some of the techniques used to insure product excellence are the following:

- Product Reliability starts at the initial design inception. It is built into every product design from the very start.
- Product Quality is built into every step of the manufacturing process through stringent inspections of incoming materials and conformance checks after critical process steps.
- Stringent inspections and reliability conformance checks are done on finished product to insure the finished product quality requirements are met.
- Field data test results are encouraged and tracked so that accelerated testing can be correlated to actual use experiences.

## Product Assurance Documents

Cypress Semiconductor uses MIL-STD-883C and MIL-M-38510H as baseline documents to determine our Test Methods, Procedures and General Specifications for semiconductors.

Customers using our Commercial and Industrial grade product receive the benefit of a military patterned process flow at no additional charge.

## Product Testing Categories

Five different testing categories are offered by Cypress:

- 1) Commercial operating range product: 0°C to +70°C.
- 2) Industrial operating range product: -40°C to +85°C.
- 3) Military Grade product processed to MIL-STD-883C; Military operating range: -55°C to +125°C.

4) SMD (Standard Military Drawing) approved product; Military operating range: -55°C to +125°C, electrically tested per the applicable Military Drawing.

5) JAN qualified product; Military operating range: -55°C to +125°C, electrically tested per MIL-M-38510 slash sheet requirements.

Category 1, 2, and 3 are available on all products offered by Cypress Semiconductor. Category 4 and 5 are offered on a more limited basis, dependent upon the specific part type in question.

## Commercial Product Assurance Categories

Commercial grade devices are offered with two different classes of product assurance. Every device shipped, as a minimum, meets the processing and screening requirements of level 1.

Level 1: For commercial or industrial systems where the demand for quality and reliability is high, but where field service and device replacement can be reasonably accomplished.

Level 2: For enhanced reliability applications and commercial or industrial systems where maintenance is difficult and/or expensive and reliability is paramount.

Devices are upgraded from Level 1 to Level 2 by additional testing and a burn-in to MIL-STD-883, Method 1015.

Table 1 lists the 100% screening and quality conformance testing performed by Cypress Semiconductor in order to meet the requirements of these programs.

## Military Product Assurance Categories

Only one standard product assurance category exists for JAN, SMD and Military grade products. Cypress' military grade devices are processed per MIL-STD-883C using methods 5004 and 5005 to define our screening and quality conformance procedures. The processing performed by Cypress results in a product that meets the class B screening requirements as called out by these methods. Every device shipped, as a minimum, meets these requirements.

JAN, SMD and Military grade devices supplied by Cypress are processed for applications where maintainance is difficult or expensive and reliability is paramount. Tables 2 through 6 list the screening and quality conformance testing that is performed in order to meet the processing requirements required by MIL-STD-883C and MIL-M-38510.

**Table 1. Cypress Commercial and Industrial Product Screening Flows—Components**

| Screen   | MIL-STD-883 Method   | Product Temperature Ranges   |  |  |  |
|--|--|--|--|--|--|
|  |  | Commercial 0°C to +70°C; Industrial -40°C to +85°C                                 |  |  |  |
|  |  | Level 1  |  | Level 2  |  |
|  |  | Plastic  | Hermetic   | Plastic  | Hermetic   |
| <b>Visual/Mechanical</b><br>• Internal Visual<br>• High Temperature Storage<br>• Temperature Cycle<br>• Constant Acceleration<br><br>• Hermeticity Check:<br>Fine/Gross Leak | 2010<br>1008, Cond C<br>1010, Cond C<br>2001, Cond E, Y1<br>Orientation<br>1014, Cond A & B; Fine Leak<br>Cond C; Gross Leak | 0.4% AQL<br>Not Performed<br>Not Performed<br><br>Does Not Apply<br>Does Not Apply | 100%<br>100%<br>Not Performed<br><br>Not Performed<br>LTPD = 5;<br>77(1,2) | 0.4% AQL<br>Not Performed<br>Not Performed<br><br>Does Not Apply<br>Does Not Apply | 100%<br>100%<br>Not Performed<br><br>Not Performed<br>LTPD = 5;<br>77(1,2) |
| <b>Burn-in</b><br>• Pre-Burn-in Electrical<br>• Burn-in<br>• Post-Burn-In Electrical<br>• Percent Defective Allowable (PDA)  | Per Device Specification<br>1015<br>Per Device Specification   | Does Not Apply<br>Does Not Apply<br>Does Not Apply<br>Does Not Apply               | Does Not Apply<br>Does Not Apply<br>Does Not Apply<br>Does Not Apply       | 100%<br>100% <sup>[2]</sup><br>100%<br>5% (max) <sup>[1]</sup>                     | 100%<br>100% <sup>[2]</sup><br>100%<br>5% (max) <sup>[1]</sup>             |
| <b>Final Electrical</b><br>• Functional, Switching, Dynamic (AC) and Static (DC) Tests   | Per Device Specification<br>1) At 25°C and Power Supply Extremes<br>2) At Hot Temperature and Power Supply Extremes          | Not Performed<br><br>100%  | Not Performed<br><br>100%  | 100% <sup>[1]</sup><br><br>100%  | 100% <sup>[1]</sup><br><br>100%  |
| <b>Cypress Quality Lot Acceptance</b><br>• External Visual<br>• Final Electrical Conformance<br>• Fine & Gross Leak Conformance  | 2009<br><br>Cypress Method 17-00064<br><br>1014, Cond A & B; Fine Leak<br>Cond C; Gross Leak                                 | [3]<br><br>[3]<br>Does Not Apply   | [3]<br><br>[3]<br>LTPD = 5;<br>77(1,2)                                     | [3]<br><br>[3]<br>Does Not Apply   | [3]<br><br>[3]<br>LTPD = 5;<br>77(1,2)                                     |

**Table 1a. Cypress Commercial and Industrial Product Screening Flows—Modules**

| Screen  | MIL-STD-883 Method  | Product Temperature Ranges   |   |
|---|---|--|---|
|   |   | Commercial 0°C to +70°C; Industrial -40°C to +85°C                   |   |
|   |   | Level 1  | Level 2   |
|   |   |  |   |
| <b>Burn-in</b><br>• Pre-Burn-in Electrical<br>• Burn-in<br>• Post-Burn-In Electrical<br>• Percent Defective Allowable (PDA)     | Per Device Specification<br>1015<br>Per Device Specification  | Does Not Apply<br>Does Not Apply<br>Does Not Apply<br>Does Not Apply | 100%<br>100%<br>100%<br>15%                                   |
| <b>Final Electrical</b><br>• Functional, Switching, Dynamic (AC) and Static (DC) Tests  | Per Device Specification<br>1) At 25°C and Power Supply Extremes<br>2) At Hot Temperature and Power Supply Extremes | Not Performed<br><br>100%  | 100%<br><br>100%  |
| <b>Cypress Quality Lot Acceptance</b><br>• External Visual<br>• Final Electrical Conformance<br>• Fine & Gross Leak Conformance | 2009<br><br>Cypress Method 17-00064<br><br>1014; Cond A & B; Fine Leak<br>Cond C; Gross Leak                        | Per Cypress Module Specification<br><br>[3]<br>Does Not Apply        | Per Cypress Module Specification<br><br>[3]<br>Does Not Apply |

**Notes:**

- 1) Electrical Test is performed after burn-in. Results of this are used to determine PDA percentage.
- 2) Burn-in is performed as a standard for 12 hours at 150°C.

- 3) Lot acceptance testing is performed on every lot to guarantee 200 PPM average outgoing quality.

**Table 2. Cypress JAN/SMD/Military Product Screening Flows**

| Screen   | Screening Per Method 5004 of MIL-STD-883C                            | Product Temperature Range: -55°C to +125°C |  |                                       |
|--|--|--|--|---------------------------------------|
|  |  | JAN  | SMD/Military Product                         | Military Grade Module                 |
| <b>Visual/Mechanical</b><br>• Internal Visual<br>• Stabilization Bake (No End Pt. Electricals)<br>• Temperature Cycling<br>• Constant Acceleration<br><br>• Hermeticity<br>—Fine Leak<br>—Gross Leak | Method 2010, Cond B  | 100%                                       | 100%   | N/A                                   |
|  | Method 1008, 24 Hrs<br>Cond C, Minimum                               | 100%                                       | 100%   | N/A                                   |
|  | Method 1010, Cond C  | 100%                                       | 100%   | Optional                              |
|  | Method 2001, Cond E (Min),<br>Y1 Orientation Only                    | 100%                                       | 100%   | N/A                                   |
|  | Method 1014, Cond A & B<br>Method 1014, Cond C                       | 100%                                       | 100%   | N/A<br>N/A                            |
| <b>Burn-in</b><br>• Initial (Pre-Burn-in) Electrical Parameters<br>• Burn-in Test<br><br>• Interim (Post-Burn-in) Electrical Parameters, Percent Defective Allowable (PDA)                           | Per Applicable Device Specification                                  | 100%                                       | 100%   | 100%                                  |
|  | Method 1015, 160 Hrs at 125°C Min or 80 hours at 150°C               | 100%                                       | 100%   | 100%<br>(48 Hours at 125°C)           |
|  | Per Applicable Device Specification<br>Maximum PDA, for All Lots, 5% | 100%                                       | 100%   | 100%<br>(PDA 10%)                     |
| <b>Final Electrical Tests</b><br>• Static Tests<br><br>• Dynamic and Switching Tests<br><br>• Functional Tests   | Method 5005, Table 1, Subgroups 1, 2 and 3                           | 100% Test to Slash Sheet                   | 100% Test to Applicable Device Specification | 100% Test to Applicable Specification |
|  | Method 5005, Table 1, Subgroups 4, 5, 6, 9, 10 and 11                | 100% Test to Slash Sheet                   | 100% Test to Applicable Device Specification | 100% Test to Applicable Specification |
|  | Method 5005, Table 1, Subgroups 7 and 8                              | 100% Test to Slash Sheet                   | 100% Test to Applicable Device Specification | 100% Test to Applicable Specification |
| <b>Quality Conformance Tests</b><br>• Group A<br>• Group B<br>• Group C<br>• Group D   | Method 5005, See Table 3-6 for Details                               | Sample<br>Sample<br>Sample<br>Sample       | Sample<br>Sample<br>Sample<br>Sample         | Sample<br>Sample<br>Sample<br>Sample  |

**Table 3. Group A Test Descriptions**

Cypress uses an LTPD sampling plan that was developed by the Military to assure product quality. Testing is performed to the subgroups found to be appropriate for the particular device type. All Military products have a Group A sample test performed as outlined by the particular screen flow.

| Sub-group | Description  | Sample Size/Accept No. |         |
|-----------|--|------------------------|---------|
|           |  | Components             | Modules |
| 1         | Static Tests at 25°C                                 | 116/0                  | 77/1    |
| 2         | Static Tests at Maximum Rated Operating Temperature  | 116/0                  | 55/1    |
| 3         | Static Tests at Minimum Rated Operating Temperature  | 116/0                  | 55/1    |
| 4         | Dynamic Tests at 25°C                                | 116/0                  | 77/1    |
| 5         | Dynamic Tests at Minimum Rated Operating Temperature | 116/0                  | 55/1    |
| 6         | Dynamic Tests at Minimum Rated Operating Temperature | 116/0                  | 55/1    |
| 7         | Functional Tests at 25°C                             | 116/0                  | 77/1    |
| 8         | Functional Tests at Minimum and Maximum Temperatures | 116/0                  | 55/1    |
| 9         | Switching Tests at 25°C                              | 116/0                  | 77/1    |
| 10        | Switching Tests at Maximum Temperature               | 116/0                  | 55/1    |
| 11        | Switching Tests at Minimum Temperature               | 116/0                  | 55/1    |

**Table 4. Group B Quality Tests**

Group B testing is performed for each inspection lot. An inspection lot is defined as a group of material of the same device type, package type and lead finish built within a six week seal period and submitted to Group B testing at the same time.

| Sub-group | Description                         | Quality/Accept # or LTPD |         |
|-----------|-------------------------------------|--------------------------|---------|
|           |                                     | Components               | Modules |
| 2         | Resistance to Solvents, Method 2015 | 4/0                      | 4/0     |
| 3         | Solderability, Method 2003          | 10                       | 10/0    |
| 5         | Bond Strength, Method 2011          | 15                       | N/A     |

**Table 5. Group C Quality Tests**

Group C tests for JAN product are performed on one device type from one inspection lot representing each technology. Sample tests are performed per MIL-M-38510 from each three months production of devices, which is based upon the lot inspection identification (or date) codes.

Group C tests for SMD and Military products are performed on one device type from one inspection lot representing each technology. Sample tests are performed per MIL-STD-883 from each twelve months production of devices, which is based upon the lot inspection identification (or date) codes.

End-point electrical tests and parameters are performed per detailed device specification.

| Sub-group | Description  | LTPD   |             |
|-----------|--|--|-------------|
|           |  | Components                                       | Modules     |
| 1         | Steady State Life Test, End Point Electricals, Method 1005   | 5  | 15/2        |
| 2         | Temp Cycling<br>Constant Acceleration<br>Hermeticity Fine<br>Visual Inspection<br>End Point Electrical | Method<br>1010<br>2001<br>1014<br>M + 1<br>M + 1 | N/A<br>15/2 |

**Table 6. Group D Quality Tests (Package Related)**

Group D tests for JAN product are performed per MIL-M-38510 on each package type from each six months of production, based on the lot inspection identification (or date) codes.

Group D tests for SMD and Military product are performed per MIL-STD-883 on each package type from each twelve months of production, based on the lot inspection identification (or date) codes.

End-point electrical tests and parameters are performed per detailed device specification.

| Sub-group | Description  | Quantity/Accept # or LTPD |         |
|-----------|--|---------------------------|---------|
|           |  | Components                | Modules |
| 1         | Physical Dimensions, Method 2016   | 15                        | 15/2    |
| 2         | Lead Integrity, Seal: Fine & Gross Leak, Methods 2004 & 1014   | 15                        | 15/2    |
| 3         | Thermal Shock, Temp Cycling, Moisture Resistance, Seal: Fine & Gross Leak, Visual Examination, End-Point Electricals, Methods 1011, 1010, 1004 & 1014                        | 15                        | 15/2    |
| 4         | Mechanical Shock, Vibration - Variable Frequency, Constant Acceleration, Seal: Fine & Gross Leak, Visual Examination, End-Point Electricals, Methods 2002, 2007, 2001 & 1014 | 15                        | 15/2    |

**Table 6. Group D Quality Tests (Package Related)**  
(Continued)

| Sub-group | Description   | Quantity/Accept # or LTPD |         |
|-----------|---|---------------------------|---------|
|           |   | Components                | Modules |
| 5         | Salt Atmosphere, Seal: Fine & Gross Leak, Visual Examination, Methods 1009 & 1014 | 15                        | 15/2    |
| 6         | Internal Water-Vapor Content; 5000 ppm maximum @ 100°C. Method 1018               | 3/0 or 5/1                | N/A     |
| 7         | Adhesion of Lead Finish, <sup>[1]</sup> Method 2025                               | 15                        | 15/2    |
| 8         | Lid Torque, Method 2024 <sup>[2]</sup>  | 5/0                       | N/A     |

**Notes:**

- 1) Does not apply to leadless chip carriers.
- 2) Applies only to packages with glass seals.

## Product Screening Summary

### Commercial and Industrial Product

- Screened to either Level 1 or Level 2 product assurance flows
- Hermetic and Molded packages available
- Incoming Mechanical and Electrical performance guaranteed:
  - 0.1% AQL Electrical Sample test performed on every lot prior to shipment
  - 0.65% AQL External Visual Sample inspection
- Electrically tested to Cypress datasheet

### Ordering Information

#### Product Assurance Grade: Level 1

- Order Standard Cypress part number
- Parts marked the same as ordered part number  
Ex: CY7C122-15PC, PALC22V10-25PI

#### Product Assurance Grade: Level 2

- Burn-in performed on all devices to Cypress detailed circuit specification
- Add “B” Suffix to Cypress standard part number when ordering to designate Burn-in option
- Parts marked the same as ordered part number  
Ex: CY7C122-15PCB, PALC22V10-25PIB

## Military Product

- Product processed per MIL-STD-883C, method 5004 product test flows
  - Military grade devices electrically tested to:
    - Cypress datasheet specifications

OR

  - SMD (Standard Military Drawing) devices electrically tested to military drawing specifications

OR

  - JAN devices electrically tested to slash sheet specifications
- All devices supplied in Hermetic packages
  - Quality conformance assured: Method 5005, Groups A, B, C and D performed as part of the standard process flow
  - Burn-in performed on all devices
    - Cypress detailed circuit specification for non-JAN devices

OR

- Slash sheet requirements for JAN products
- AC, DC, Functionally and Dynamically tested at 25°C as well as temperature and power supply extremes on 100% of the product in every lot
- JAN product manufactured in a DESC certified facility

### Ordering Information

#### JAN Product:

- Order per Military document
- Marked per Military document  
Ex: JM38510/28901BVA

#### SMD Product:

- Order per Military document
- Marked per Military document  
Ex: 5962-8684601EA

#### Military Grade Product:

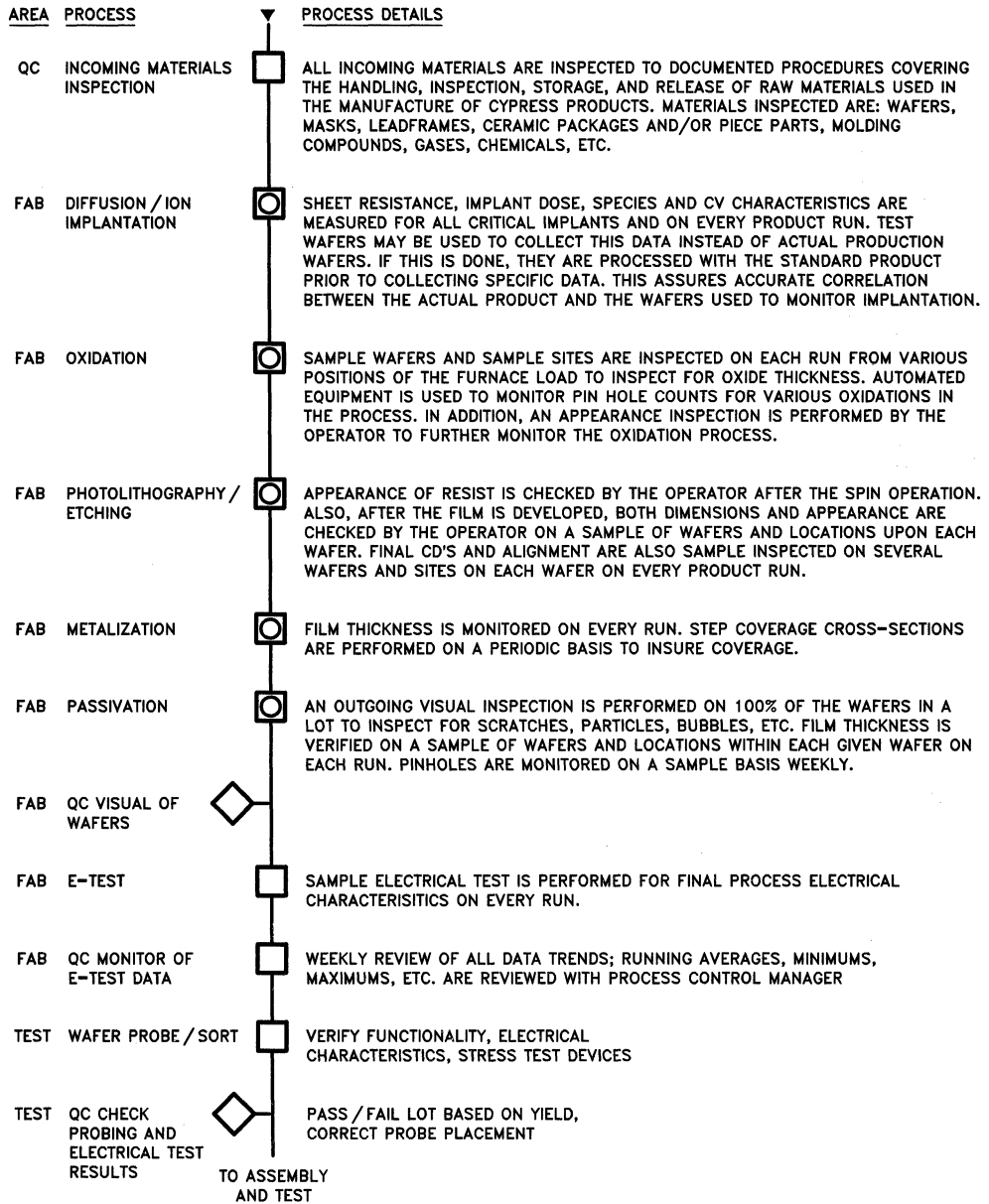
- Order per Cypress standard Military part number
- Marked the same as ordered part number  
Ex: CY7C122-25DMB

## Military Modules

- Military Temperature Grade Modules are designated with a ‘M’ suffix only. These modules are screened to standard combined flows and tested at both Military temperature extremes.
- MIL-883C Equivalent Modules are processed to proposed JEDEC standard flows for MIL-883C compliant modules. All 883C equivalent modules are fully compliant 883C components.



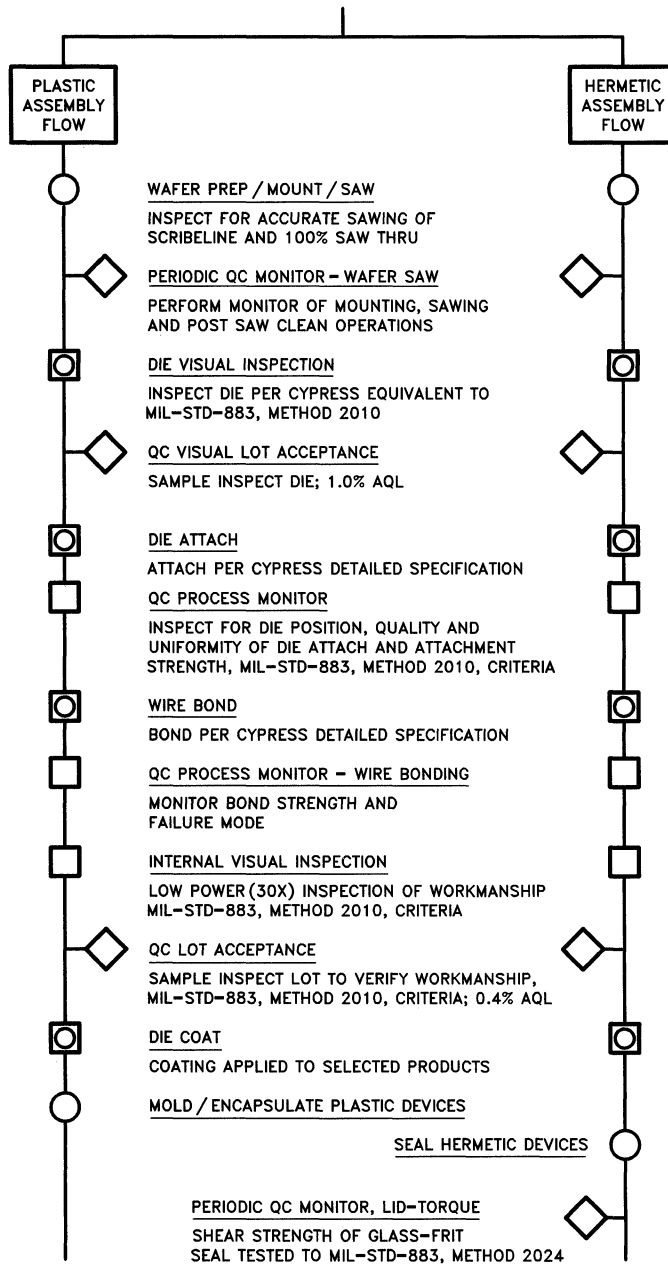
Product Quality Assurance Flow—Components



0032-1

(Continued)

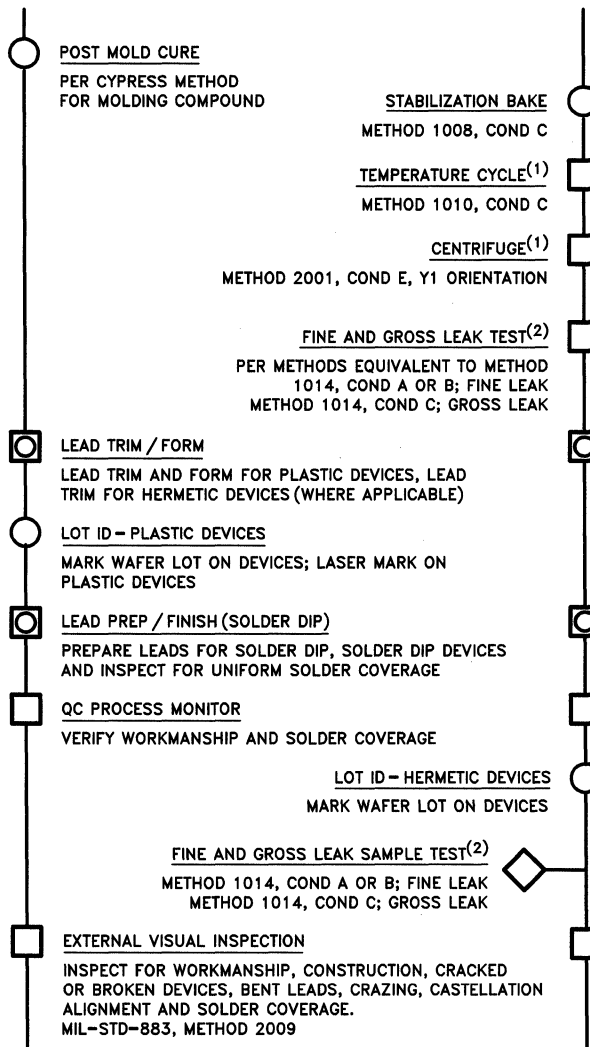
Product Quality Assurance Flow—Components (Continued)



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0032-2

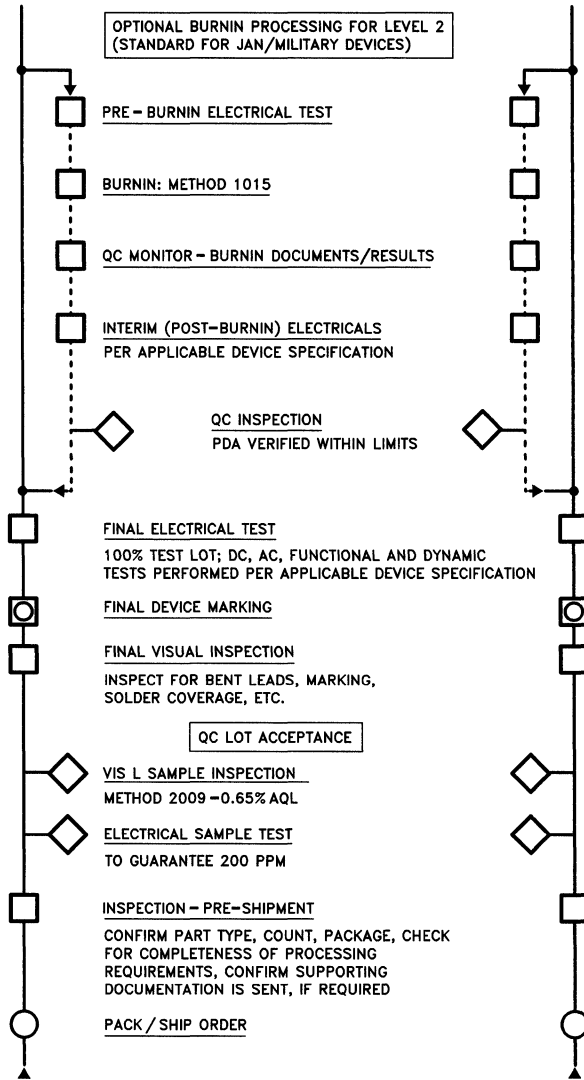
Product Quality Assurance Flow—Components (Continued)



0032-3





(Continued)

Product Quality Assurance Flow—Components (Continued)



0032-4

Key

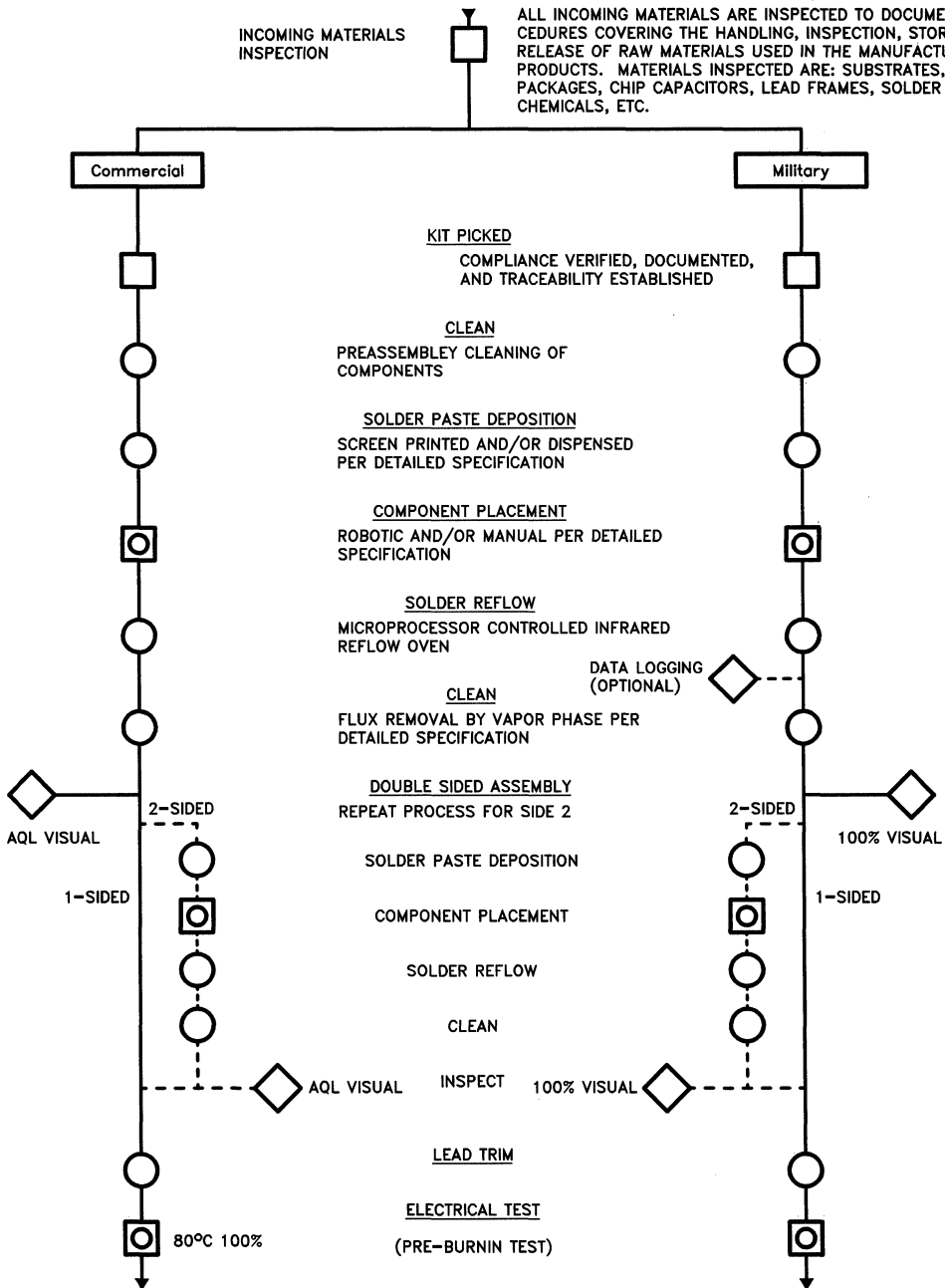
-  PRODUCTION PROCESS
-  TEST / INSPECTION
-  PRODUCTION PROCESS AND TEST INSPECTION
-  QC SAMPLE GATE AND INSPECTION

0032-5

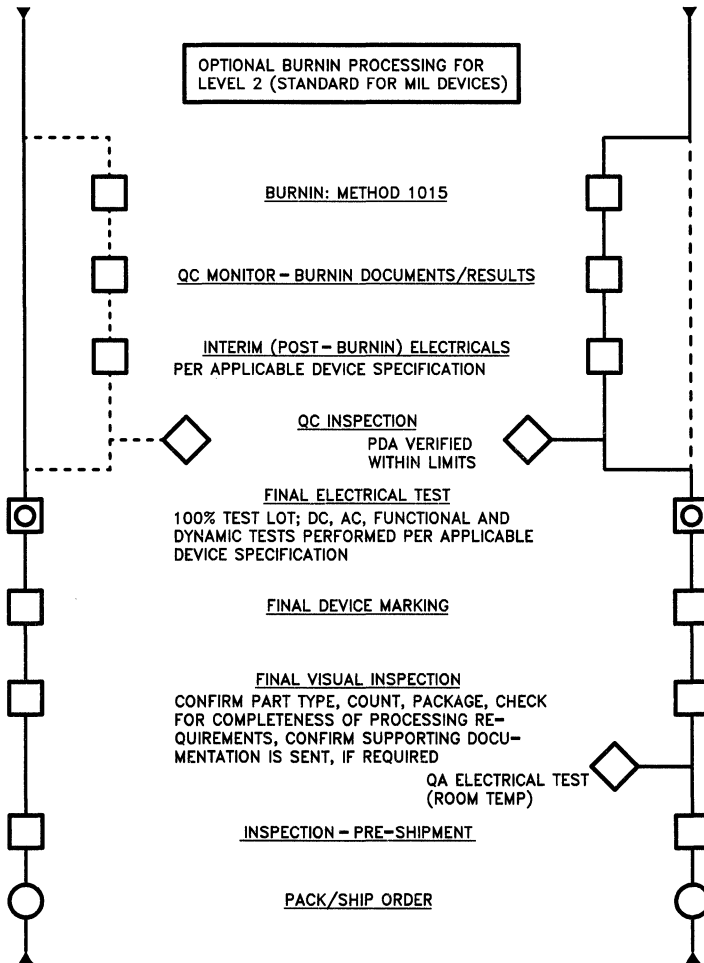
Notes:

1. Temp Cycle and Centrifuge performed per Applicable Product Screening Flow.
2. JAN/SMD/Military grade products are 100% Fine and Gross Leak tested and sample tested after wafer lot I.D. Commercial grade devices received sample test only. Sample size is per Commercial Product Screening Flow.

Product Quality Assurance Flow—Modules



**Product Quality Assurance Flow—Modules (Continued)**



0032-7

**Key:**

- PRODUCTION PROCESS
- TEST / INSPECTION
- ◉ PRODUCTION PROCESS AND TEST INSPECTION
- ◇ QC SAMPLE GATE AND INSPECTION

0032-5

## Reliability Monitor Program

The Reliability Monitor Program is a documented Cypress procedure that is described in Cypress specification #25-00008 which is available to Cypress customers upon request. This specification describes a procedure that provides for periodic reliability monitors to insure that all Cypress products comply with established goals for reliability improvement and to minimize reliability risks for

Cypress customers. The Reliability Monitor Program is designed to monitor key products within each generic process family. This procedure requires that detailed failure analysis be performed on all test rejects and the corrective actions be taken as indicated by the analysis. A summary of the Reliability Monitor Program test and sampling plan is shown below.

## Reliability Monitor Program Sampling Plan

| Test Description   | Duration                 | Sample Size | Frequency[1]        |
|--|--------------------------|-------------|---------------------|
| Early Failure Rate (EFR)<br>150°C HTOL<br>125°C HTOL                                     | 12 Hours<br>80 Hours     | 200<br>200  | Weekly<br>Bi-weekly |
| Latent Failure Rate (LFR)<br>150°C HTOL<br>125°C HTOL                                    | 1000 Hours<br>2000 Hours | 200<br>200  | Monthly<br>Monthly  |
| High Temp Steady State Life (HTSSL)<br>150°C HTOL<br>150°C HTOL (1 lot/quarter extended) | 168 Hours<br>1000 Hours  | 100<br>100  | Weekly<br>Quarterly |
| Plastic Package Data Retention (DRET)<br>165°C Bake                                      | 1000 Hours               | 55          | Bi-weekly           |
| Hermetic Package Data Retention (DRET)<br>250°C Bake                                     | 1000 Hours               | 55          | Monthly             |
| Pressure Cooker (PCT)<br>121°C/100% R.H.   | 288 Hours                | 55          | Weekly              |
| Pre-conditioned Temperature-Humidity Life (PCTH)<br>96 Hrs. PCT + Biased 85°C/85% R.H.   | 1000 Hours               | 55          | Every 6 Weeks       |
| High-Acceleration Saturation (HAST)<br>Biased 121°C/85% R.H.                             | 200 Hours                | 55          | Every 6 Weeks       |
| Temperature Cycle (T/C)<br>-65°C to +150°C<br>-65°C to +150°C (1 lot/quarter extended)   | 15 Cycles<br>1000 Cycles | 55<br>55    | Weekly<br>Quarterly |

**Note:**

1) Maximum period between samples is listed. More frequent sampling may occur.

PRODUCT INFORMATION 1

STATIC RAMS 2

PROMS 3

EPLDS 4

LOGIC 5

RISC 6

MODULES 7

ECL 8

MILITARY 9

BRIDGEMOS 10

QUICKPRO 11

PLD TOOLKIT 12

QUALITY AND RELIABILITY 13



APPLICATION BRIEFS 14

PACKAGES 15







# Section Contents

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## Application Briefs

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| RAM Input and Output Characteristics .....                    | 14-1  |
| Power Characteristics of Cypress Products .....               | 14-8  |
| Pin-Out Compatibility Considerations of SRAMs and PROMs ..... | 14-15 |





# Application Briefs

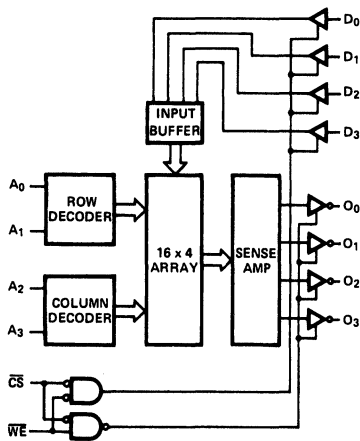
## RAM Input Output Characteristics

### Introduction to Cypress RAMs

Cypress Semiconductor Corporation uses a speed optimized CMOS technology to manufacture high speed static RAMs which meet and exceed the performance of competitive bipolar devices while consuming significantly less power and providing superior reliability characteristics. While providing identical functionality, these devices exhibit slightly differing input and output characteristics which provide the designer opportunities to improve overall system performance. The balance of this application note describes the devices, their functionality and specifically their I/O characteristics.

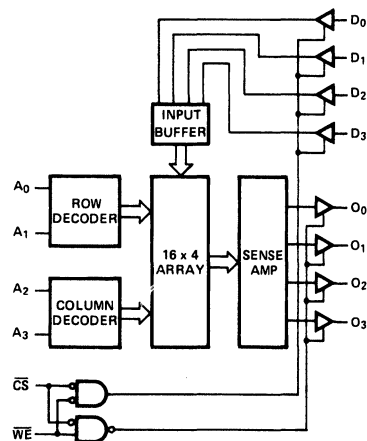
### PRODUCT DESCRIPTION

The five parts in *Figure 1* constitute three basic devices of 64, 1024 and 4096 bits respectively. The 7C189 and 7C190 feature inverting and non-inverting outputs respectively in a 16 x 4 bit organization. Four address lines address the 16 words, which are written to and read from over separate input and output lines. Both of these 64 bit devices have separate active LOW select and write enable signals. The 256 x 4 7C122 is packaged in a 22 pin DIP, and features separate input and output lines, both active LOW and active HIGH select lines, eight address lines, an active LOW output enable, and an active LOW write enable. Both the



7C189

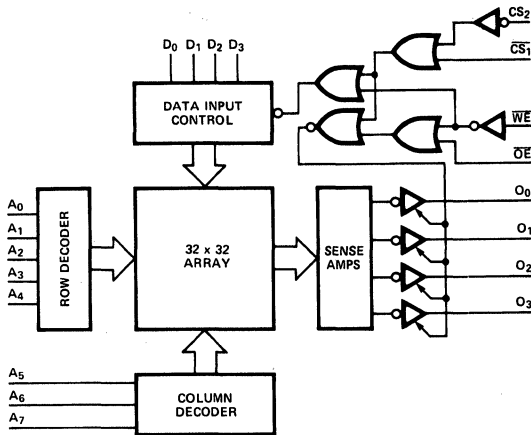
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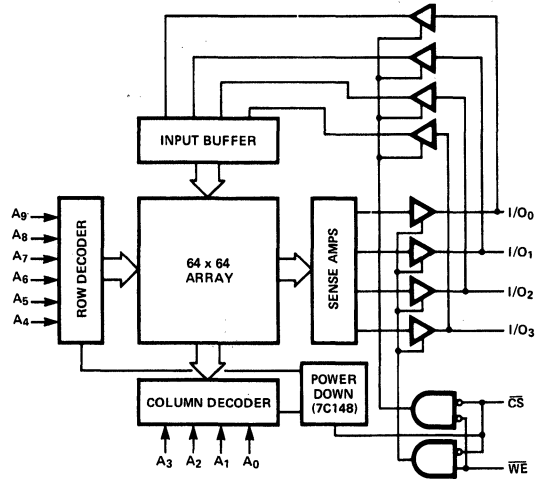
7C190

0027-2

Figure 1. RAM Block Diagrams



0027-3

**7C122**


0027-4

**7C148/9**
**Figure 1. RAM Block Diagrams (Continued)**

7C148 and 7C149 are organized 1024 x 4 bits and feature common pins for the input and output of data. Both parts have 10 address lines, a single active LOW chip select and an active LOW write enable. The 7C148 features automatic power down whenever the device is not selected, while the 7C149 has a high speed, 15 ns, chip select for applications which do not require power control. This family of high speed static RAMs is available with access times of 15 to 45 ns with power in the 300 to 500 mW range. They are designed from a common core approach, and share the same memory cell, input structures and many other characteristics. The outputs are similar, with the exception of output drive, and the common I/O optimization for the 7C148 and 7C149. For more detailed information on these products, refer to the available data sheets.

### GENERIC I/O CHARACTERISTICS

Input and output characteristics fall generally into two categories, when the area of operation falls within the normal limits of  $V_{CC}$  and  $V_{SS}$  plus or minus approximately 600 mV, and abnormal circumstances, when these limits are exceeded. Inputs under normal operating conditions are voltages that switch between logic "0" and logic "1". We will consider operation in a positive true environment and therefore a logic "1" is more positive than a logic "0". The I/O characteristics of the devices we are concerned with are what is considered to be TTL compatible. Therefore a logic "1" is 2.0V, while a logic "0" is 0.8V. The input of a device must be driven greater than 2.0V, not to exceed  $V_{CC} + 0.6V$  to be considered a logic "1" and, to less than 0.8V, but not less than  $V_{SS} - 0.6V$ , to be considered a logic "0".

Output characteristics represent a signal that will drive the input of the next device in the system. Since the levels we are dealing with are TTL, we may assume that the  $V_{IL}$  and

$V_{IH}$  values of 0.8 and 2.0V referenced above are valid. In consideration of noise margin however, driving the input of the next stage to the required  $V_{IL}$  or  $V_{IH}$  is not sufficient. Noise margins of 200 to 400 mV are considered more than adequate, and therefore the  $V_{OH}$  we deal with is 2.4V while the  $V_{OL}$  is 0.4V, providing a noise margin of 400 mV. Since the driven node consists of both a resistive and a capacitive component, output characteristics are specified such that the output driver is capable of sinking  $I_{OL}$  at the specified  $V_{OL}$ , and capable of sourcing  $I_{OH}$  at  $V_{OH}$ . Since the values of  $I_{OL}$  and  $I_{OH}$  differ depending on the device, these values are shown in Table 1. Outputs have one other characteristic that we need to be concerned with, Output Short Circuit Current or  $I_{OS}$ . This is the maximum current that the output will source when driving a logic "1" into  $V_{SS}$ . We need to be concerned for two reasons. First, the output should be capable of supplying this current for some reasonable period of time without damage, and second, this is the current that charges the capacitive load when switching the output from a "0" to a "1" and will control the output rise time.

Since memories such as these are often tied together, we are also concerned about the output characteristics of the devices when they are deselected. All of the devices in this family feature three state outputs such that in addition to their active conditions when selected, when deselected, the outputs are in a high impedance condition which does not source or sink any current. In this condition, as long as the input is driven in its normal operating mode, it appears as an open, with less than 10  $\mu A$  of leakage. Thus to any other device driving this node, it is non-existent.

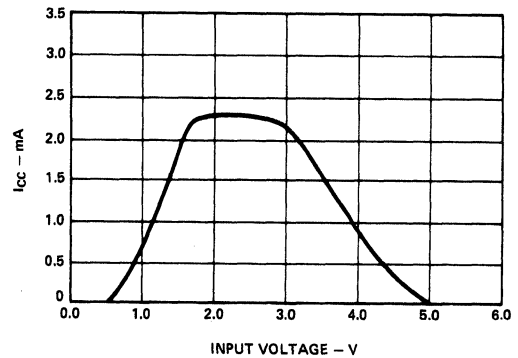
## TECHNOLOGY DEPENDENCIES AND BENEFITS

Some of the products in this application note were originally produced in a BIPOLAR technology, some have since been re-engineered in NMOS technology and Cypress has now produced them in a speed optimized CMOS technology. There are both technology dependencies and benefits relative to the design of input and output structures that are associated with each technology. The designer who uses these products should be knowledgeable of these characteristics and how they can benefit or impede a design effort. One of the most obvious is that both NMOS and CMOS device inputs are high impedance, with less than 10  $\mu\text{A}$  of input leakage. Bipolar devices, however, require that the driver of an input sink current when driving to  $V_{IL}$ , but appear as high impedance at  $V_{IH}$  levels. This is due to the fact that the input of a bipolar device is the emitter of a bipolar NPN type device with its base biased positive. The bias is what establishes the point at which the input changes from requiring current to be sourced to high impedance and is 1.5V. This switching level is the reason that AC measurements are done at the 1.5V level. Although NMOS and CMOS device inputs do not change from low to high impedance, great care is taken to balance their switching threshold at 1.5V. To a system designer this allows fanout to consider only capacitive loading with MOS devices while bipolar has both a capacitive and DC component. The other input characteristic which differs from bipolar to MOS is the clamp diode structure. This structure exists in both MOS and bipolar, however in MOS that uses BIAS GENERATOR techniques, all high speed MOS devices, the diode does not become forward biased until the input goes more negative than the substrate bias generator plus one diode drop. Since the bias generator is usually about  $-3\text{V}$  this has the effect of removing the clamping effect.

## I/O Parameters

### CMOS/NMOS/BIPOLAR INPUT CHARACTERISTICS

Although NMOS, CMOS and BIPOLAR technologies differ widely, the I/O characteristics tend to fall into two areas. The traditional characteristics are the TTL derivatives that have been covered above, and are documented in Table 1. With the exception of the differences in input impedance between MOS and BIPOLAR devices all three technologies are used to produce TTL compatible products. The second camp is the true CMOS interface where signals swing from  $V_{SS}$  to  $V_{CC}$ . These interface specifications define a "1" as greater than  $V_{CC} - 1.5\text{V}$  and a "0" as less than  $V_{SS} + 1.5\text{V}$ . In addition, loads are primarily capacitive. Only devices produced in a CMOS technology are capable of behaving in this manner. CMOS devices can, however, handle both TTL and CMOS inputs. Devices such as the ones described in this application note have input characteristics depicted in Figure 2.



0027-5

Figure 2. Input Voltage vs. Current

Table 1. DC Parameters

| Parameters | Description                  | Test Conditions  | 7C122 |          | 7C148/9 |          | 7C189/90 |          | Units         |
|------------|------------------------------|--|-------|----------|---------|----------|----------|----------|---------------|
|            |                              |  | Min.  | Max.     | Min.    | Max.     | Min.     | Max.     |               |
| $V_{OH}$   | Output High Voltage          | $V_{CC} = \text{Min.}, I_{OH} = -5.2 \text{ mA}$                 | 2.4   |          | 2.4     |          | 2.4      |          | V             |
| $V_{OL}$   | Output Low Voltage           | $V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$                  |       | 0.4      |         | 0.4      |          | 0.4      | V             |
| $V_{IH}$   | Input High Voltage           |  | 2.1   | $V_{CC}$ | 2.0     | $V_{CC}$ | 2.0      | $V_{CC}$ | V             |
| $V_{IL}$   | Input Low Voltage            |  | -3.0  | 0.8      | -3.0    | 0.8      | -3.0     | 0.8      | V             |
| $I_{IL}$   | Input Low Current            | $V_{CC} = \text{Max.}, V_{IN} = V_{SS}$                          |       | 10       |         | 10       |          | 10       | $\mu\text{A}$ |
| $I_{IH}$   | Input High Current           | $V_{CC} = \text{Max.}, V_{IN} = V_{CC}$                          |       | 10       |         | 10       |          | 10       | $\mu\text{A}$ |
| $I_{OFF}$  | Output Current (High Z)      | $V_{OL} < V_{OUT} < V_{OH}, T_A = \text{Max.}$                   | -10   | +10      | -10     | +10      | -10      | +10      | $\mu\text{A}$ |
| $I_{OS}$   | Output Short Circuit Current | $V_{CC} = \text{Max.}, 0^\circ\text{C} < T_A < 70^\circ\text{C}$ |       | -70      |         | -90      |          | -275     | mA            |
|            |                              | $V_{OUT} = V_{SS}, -55^\circ\text{C} < T_A < 125^\circ\text{C}$  |       | -80      |         | -90      |          | -350     | mA            |

When operated in the TTL range, they perform normally. Operated in full CMOS mode, an additional benefit of power savings is realized as the current consumed in the input converter decreases as the input voltage rises above 3.0V, or falls below 1.5V. Since the input signal is in the 1.5 to 3.0V range only when transitioning between logic states, the power savings in a large array with true CMOS inputs can be significant. With input signals on over half of the pins of a device, significant savings in a large system can be realized by using CMOS input voltage swings even in TTL systems.

## Switching Characteristics

Although this application note does not directly deal with the AC characteristics of high speed RAMs, the input and output characteristics of these devices have a great deal to do with the actual AC specifications. Conventionally, all AC measurements associated with high speed devices are done at 1.5V and assume a maximum rise and fall time. This eliminates the variations associated with the various configurations that the device will be used in (as a figure of merit when testing the device) but, does not mean that the designer can ignore these influences when designing a system. Maximum rise and fall time is usually found in the notes included on every data sheet. For the products referred to in this application note, a 10 ns maximum rise and fall time is specified for all devices with access times equal to or greater than 25 ns and a 5 ns maximum rise and fall time for all devices with access times less than 25 ns. The AC load and its Thévenin equivalent in *Figure 3* represent the resistive and capacitive components of load which the devices are specified to drive. With either of these loads, the device will be required to source or sink its rated output current at its specified output voltage. The capacitance stresses the ability of the device output to source or sink sufficient current to slew the outputs at a high enough rate to meet the AC specifications. The high impedance load is a convenience to testing when trying to determine how rapidly the output enters a high impedance condition. Once the output enters a high impedance mode, the resistive divider will charge the capacitance until equilibrium is reached. Allowing for noise margin, testing for a 500 mV change is normal. By using a smaller capacitance

than normal, the change will occur more quickly, allowing a more accurate determination of entry into the high impedance state.

## SWITCHING THRESHOLD VARIATIONS

Switching threshold variations along with input rise and fall times can have an effect on the performance of any device. Input rise and fall times are under the control of the designer, and are primarily affected by capacitive loading, the driver and bus termination techniques. Switching threshold is affected by process variations, changes in  $V_{CC}$  and temperature. Compensation of these variables is the territory of the manufacturer, both at the design stage and the manufacturing of the device. Combined threshold shifts over full military temperature ranges and process variations average less than 100 mV. This translates directly to  $V_{IL}$  and  $V_{IH}$  variations which track well within the noise margins of normal system design particularly since the  $V_{OL}$  and  $V_{OH}$  changes track to the same 100 mV.

## Input Protection Mechanisms

### THE ELECTROSTATIC DISCHARGE PHENOMENON

Because of their extremely high input impedance and relatively low (approximately 30V) breakdown voltage, MOS devices have always suffered from destruction caused by ESD (Electro Static Discharge). This has caused two actions. First, major efforts to design input protection circuits without impeding performance has resulted in MOS devices that are now superior to bipolar devices. Second, care in handling semiconductors is now common practice. Interestingly enough, bipolar products that once did not suffer from ESD have now suddenly become sensitive to the phenomenon, primarily because new processing technology involving shallow junctions is in itself sensitive. MOS devices are in many cases now superior to bipolar products. A sampling of competitive BIPOLAR and NMOS 64 bit, 1K bit and 4K bit products reveals breakdown voltages as low as  $\pm 150V$  to greater than  $\pm 2001V$  magnitudes. The circuit in *Figure 4* is used to protect Cypress products against ESD. It consists of two thick oxide field transistors wrapped around an input resistor and a thin oxide device

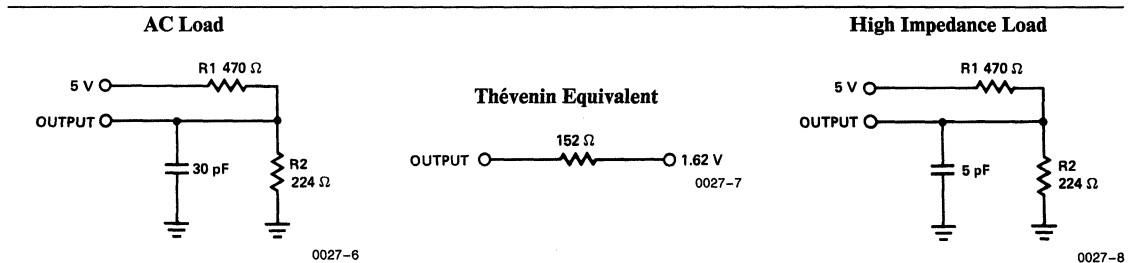
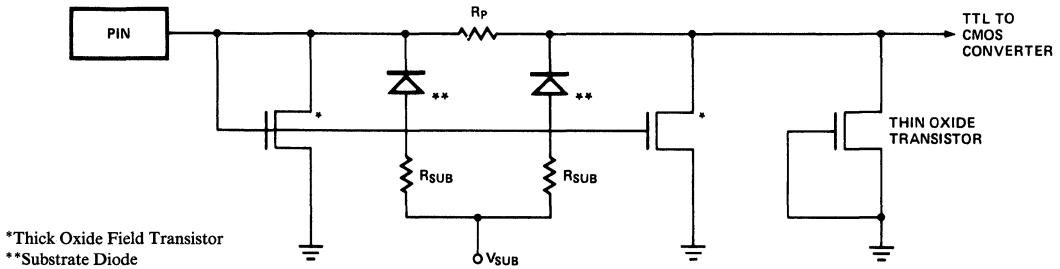


Figure 3. Test Loads



0027-9

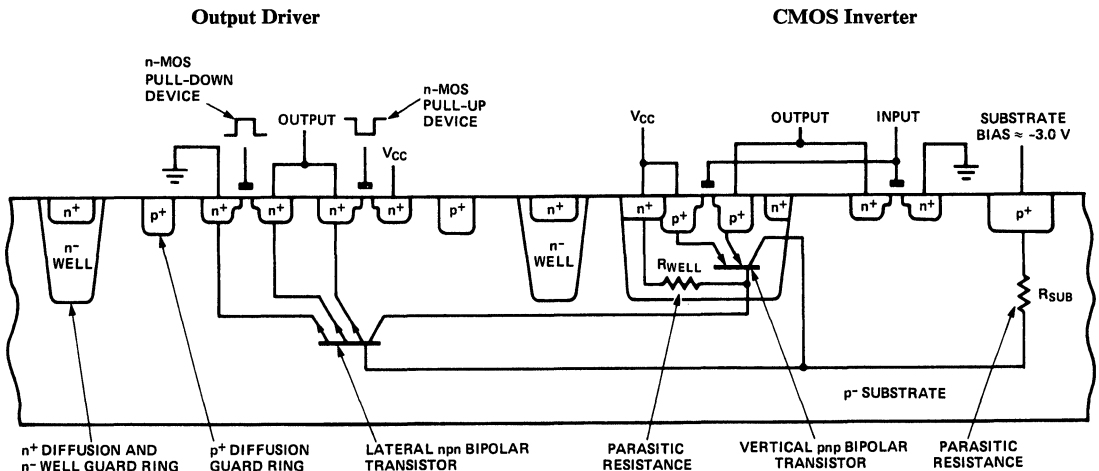
Figure 4. Input Protection Circuit

with a relatively low breakdown voltage of approximately 12V. Large input voltages cause the field transistors to turn on discharging the ESD current harmlessly to ground. The thin oxide transistor breaks down when the voltage across it exceeds the 12V level and it is protected from destruction by the current limiting of  $R_p$ . The combination of these two structures provides ESD protection greater than 2250V, the limit of the testing equipment available. In addition, repeated applications of this stress do not cause a degradation that could lead to eventual device failure as observed in functionally equivalent devices.

### CMOS Latchup

The parasitic bipolar transistors shown in *Figure 5* result in a built-in silicon controlled rectifier illustrated in *Figure 6*. Under normal circumstances the substrate resistor  $R_{SUB}$  is connected to ground. Therefore, whenever the signal on the pin goes below ground by one diode drop, current flows

from ground through  $R_{SUB}$  forward biasing the lower transistor in the effective SCR. If this current is sufficient to turn on the transistor, the upper PNP transistor is forward biased, the SCR turns on and normally destroys the device. Several solutions are obvious, decreasing the substrate resistance, or adding a substrate bias generator are two. The bias generator technique has several additional benefits, however, such as threshold voltage control which increases device performance and is employed in all Cypress products, along with guard rings which effectively isolate input and output structures from the core of the device and thus effectively decrease the substrate resistance by short circuiting the current paths. Latchup can potentially be induced at either the inputs or outputs. In true CMOS output structures as discussed above, the output driver has a PMOS pullup which creates additional vertical bipolar PNP transistors compounding the latchup problem. Additional isolation using the guard ring technique can be used to solve this problem, at the expense of additional silicon

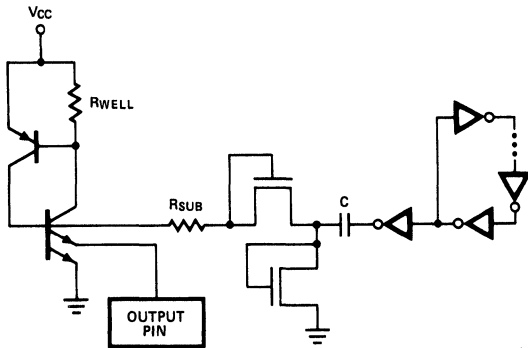


0027-10

Figure 5. CMOS Cross Section and Parasitic Circuits



Substrate Bias Generator



0027-11

Figure 6. Parasitic SCR and Bias Generator

area. Since all of the devices of concern here require TTL outputs, the problem is totally eliminated through the use of an NMOS pullup.

LATCHUP CHARACTERISTICS

Inducing Latchup for Testing Purposes

Care needs to be exercised in testing for latchup since it is normally a destructive phenomena. The normal method is to power the device under test with a supply that can be current limited, such that when latchup is induced, insufficient current exists to destroy the device. Once this setup exists, driving the inputs or outputs with a current, and measuring the point at which the power supply collapses will allow non-destructive measurement of the latchup characteristics of the devices under question. In actual testing, with the device under power, individual inputs and outputs are driven positive and negative with a voltage and the current measured at which the device latches up. This provides the DC latchup data for each pin on the device as a function of trigger current.

Measurement of Latchup Susceptibility

Actually measuring the latchup characteristics of devices should encompass ranges of reasonable positive and negative currents for trigger sources. Depending on the device, latchup can occur as low as a few mA to as high as several hundred mA of sink or source current. Devices which latch at trigger currents of less than 20 to 30 mA are in danger of encountering system conditions that will cause latchup failure.

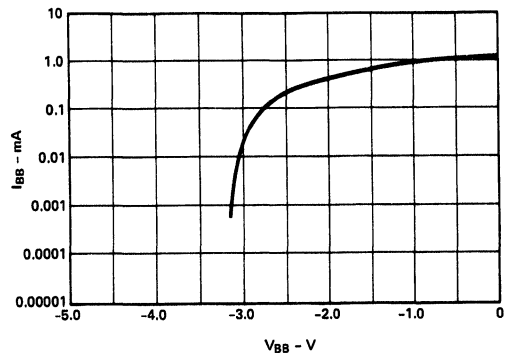
Competitive Devices

Although there are few devices directly competitive with the Cypress devices covered in this application note, the latchup characteristics of the closest functionally similar devices were measured. The results show devices that latchup at as low as 10 mA all the way to devices that can sustain greater than 100 mA of trigger current without

latchup. The Cypress devices covered in this document can sustain greater than 200 mA without incurring latchup, far more than is possible to encounter in any reasonable system environment.

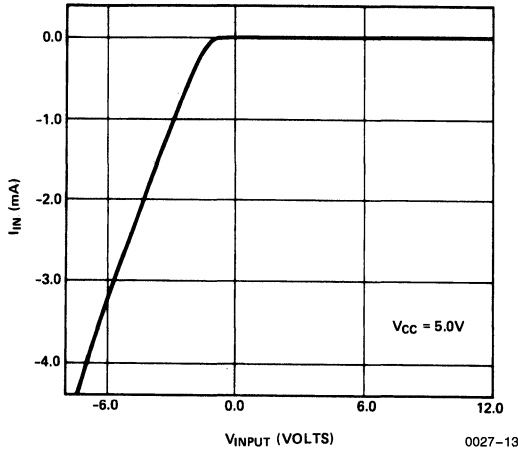
Elimination of Latchup in Cypress RAMs

Since the latchup characteristic is one that inherently exists in any CMOS device, rather than change the laws of physics, we design to minimize its effects over the operating environment that the device must endure. These include temperature, power supply and signal levels as well as process variations. There are several techniques employed to eliminate the latchup phenomenon. Two of them involve moving the trigger threshold outside the operating range as to make it impossible to ever encounter it. These are either using low impedance, epitaxial, substrates and/or a substrate bias generator. The use of a low impedance substrate has the effect of increasing the undershoot voltage required to generate the required trigger current that causes latchup. A substrate bias generator has two effects which help to eliminate latchup. First, by biasing the substrate at a negative, -3.0V, voltage, the parasitic diodes can not be forward biased unless the undershoot exceeds the -3V by at least one diode drop. Second, if undershoot is this severe, the impedance of the bias generator itself is sufficient to deter sufficient trigger from being generated. The bias generator has one additional noticeable characteristic, it effectively removes the input clamp diode. This is due to the anode of the diode connecting to the substrate which is at -3.0V. Therefore, even though the diode exists as shown in Figure 4, DC signals of -3.0V do not forward bias the diode and exhibit the clamp condition. The benefits of this are apparent in higher noise tolerance as substrate currents due to input undershoot do not occur.



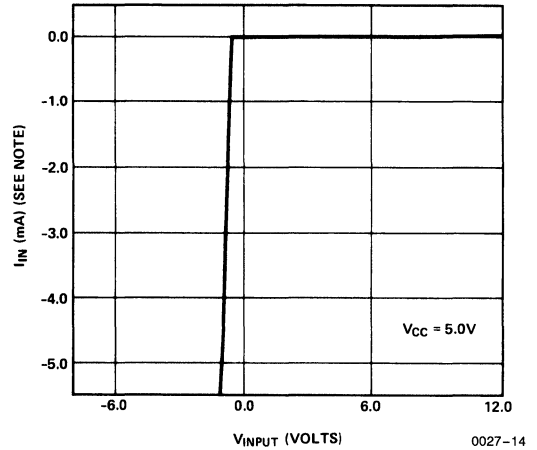
0027-12

Figure 7. Bias Generator Characteristics



**Figure 8. Input V/I Characteristics**

Figures 8 and 9 represent the voltage and current characteristics of the devices discussed in this application brief. Figure 8 is characteristic of an input pin, and Figure 9 an output pin in a high impedance state. In Figure 8, the input covers +12V to -6V, well outside the +7V to -3V specification. Referring to Figure 4 to understand these characteristics, when the input voltage goes negative, the thin oxide transistor acts as a forward biased diode and the



Note: Output is in a High Impedance Condition.

**Figure 9. Output V/I Characteristics**

slope of the curve is set by the value of  $R_p$ . As the input voltage goes positive, only leakage current flows. The output characteristics in Figure 9 show the same phenomenon, with the exception that, since this is not an input, no protection circuit exists, and therefore no  $R_p$  exists. An equivalent thin film device acts as a clamp diode which limits the output voltage to approximately -1V at -5 mA.



# Power Characteristics of Cypress Products

## Introduction

### SCOPE AND PURPOSE

This document presents and analyzes the power dissipation characteristics of Cypress products. The purpose of this document is to provide the user with the knowledge and the tools to manage power when using Cypress CMOS products.

### DESIGN PHILOSOPHY

The design philosophy for all Cypress products is to achieve superior performance at reasonable power dissipation levels. The CMOS technology, the circuit design techniques, architecture and the topology have been carefully combined in order to optimize the speed/power ratio.

### SOURCES OF POWER DISSIPATION

Power is dissipated within the integrated circuit as well as external to it. Both internal and external power have a quiescent (or DC) component and a frequency dependent component. The relative magnitudes of each depend upon the circuit design objectives. In circuits designed to minimize power dissipation at low to moderate performance, the internal frequency dependent component is significantly greater than the DC component. In the high performance circuits designed and manufactured by Cypress, the internal frequency dependent power component is much less than the DC component. The reason for this is that a large percentage of the internal power is dissipated in linear circuits such as sense amplifiers, bias generators and voltage/current references that are required for high performance.

#### External Power Dissipation

The input impedance of CMOS circuits is extremely high. As a result, the DC input current is essentially zero (10  $\mu$ A or less). When CMOS circuits drive other CMOS circuits there is practically no DC output current. However,

#### Note:

The Cypress Power/Speed Program, which implements the equations in this application note, is available from Cypress for your use on personal computers.

when CMOS circuits drive either bipolar circuits or DC loads, external DC power is dissipated. It is standard practice in the semiconductor industry to NOT include the current from a DC load in the device  $I_{CC}$  specification. Cypress supports this practice. It is also standard practice to NOT include the current required to charge and discharge capacitive loads in the data sheet  $I_{CC}$  specification. Cypress also supports this standard practice.

#### Frequency Dependent Power

CMOS integrated circuits inherently dissipate significantly less power than either bipolar or NMOS circuits. In the ideal digital CMOS circuit there is no direct current path between  $V_{CC}$  and  $V_{SS}$ ; in circuits using other technologies such paths exist and DC power is dissipated while the device is in a static state.

The principal component of power dissipation in a power-optimized CMOS circuit is the transient power required to charge and discharge the capacitances associated with the inputs, outputs, and internal nodes. This component is commonly called  $CV^2f$  power and is directly proportional to the operating frequency,  $f$ . The corresponding current is given by the formula

$$I_{CC}(f) = CVf.$$

The primary sources of frequency dependent power are due to the capacitances associated with the internal nodes and the output pins. For "regular" logic structures, such as RAMs, PROMs and FIFOs the internal capacitances are "balanced" so that the same delay and, therefore, the same frequency dependent power is dissipated independent of the location that is addressed. This is not true for programmable devices such as PALs because the capacitive loading of the internal nodes is a function of the logic implemented by the device. In addition, PALs and other types of logic devices may contain sequential circuits so the input frequency and the output frequency may be different.

The capacitance of each input pin is typically 5 pF, so its contribution to the total power is usually insignificant.

**Introduction (Continued)**
**Derivation of Applicable Equations**

The charge,  $Q$ , stored on a capacitor,  $C$ , that is charged to a voltage,  $V$ , is given by the equation;

$$Q = CV. \quad \text{EQ. 1}$$

Dividing both sides of equation 1 by the time required to charge and discharge the capacitor (one period or  $T$ ) yields;

$$\frac{Q}{T} = \frac{CV}{T} \quad \text{EQ. 2}$$

By definition, current ( $I$ ) is the charge per unit time and

$$f = \frac{1}{T}.$$

Therefore,

$$I = CVf. \quad \text{EQ. 3}$$

The power ( $P = VI$ ) required to charge and discharge the capacitor is obtained by multiplying both sides of equation 3 by  $V$ .

$$P = VI = CV^2f \quad \text{EQ. 4}$$

It is standard practice to make the assumption that the capacitor is charged to the supply voltage ( $V_{CC}$ ) so that

$$P = V_{CC}I = C [V_{CC}]^2f \quad \text{EQ. 5}$$

The total power consumption for a CMOS integrated circuit is dependent upon:

- the static (quiescent or DC) power consumption.
- the internal frequency of operation
- the internal equivalent (device) capacitance
- the number of inputs, their associated capacitance, and the frequency at which they are changing
- the number of outputs, their associated capacitance, and the frequency at which they are changing

In equation form:

$$P_D = [(C_{IN})(F_{IN}) + (C_{INT})(F_{INT}) + (C_{LOAD})(F_{LOAD})] [V_{CC}]^2 + I_{CC} \text{ (quiescent)} V_{CC}. \quad \text{EQ. 6}$$

The first three terms are frequency dependent and the last is not. This equation can be used to describe the power dissipation of every IC in the system. The total system power dissipation is then the algebraic sum of the individual components.

The relative magnitudes of the various terms in the equation are device dependent. Note that equation 6 must be modified if all of the inputs, internal nodes or all of the outputs are not switching at the same frequency. In the general case, each of the terms is of the form  $C_1 F_1 + C_2 F_2 + C_3 F_3 + \dots C_n F_n$ . In practical reality the terms are estimated using an equivalent capacitance and frequency.

**Transient Power: Input Buffers and Internal**

In the N-well CMOS inverter, the P-channel pullup transistor and the N-channel pulldown transistor (which are in series with each other between  $V_{CC}$  and  $V_{SS}$ ) are never on

at the same time. This means that there is no direct current path between  $V_{CC}$  and ground, so that the quiescent power is very nearly zero. In the real world, when the input signal makes the transition through the linear region (i.e., between logic levels) both the N-channel and the P-channel transistors are partially turned ON. This creates a low impedance path between  $V_{CC}$  and  $V_{SS}$ , whose resistance is the sum of the N-channel and P-channel resistances. These gates are used internally in Cypress products.

**DC or Static Power**

In addition to the conventional gates there are sense amplifiers, input buffers and output buffers, bias generators and reference generators that all dissipate power. The RAMs and FIFOs also have memory cells that dissipate standby power whether the IC is selected or not. The PROM and PAL® products have EPROM memory cells that do not dissipate as much standby power as a RAM cell.

**Power Down Options**

Many of the Cypress static RAMs have power down options that enable the user to reduce the power dissipation of these devices by approximately an order of magnitude when they are not accessed. The technique used is to disable or turn-off the input buffers and the sense amplifiers.

**Worst Case Device Power Specifications**

All Cypress products are specified with  $I_{CC}$  under worst, worst, worst case conditions. This means that the  $V_{CC}$  voltage is at its maximum (5.5V), the operating temperature is at its minimum, which is 0°C for commercial product and -55°C for military product and all inputs are at  $V_{IN} = 1.5V$ .

 **$I_{CC}$  TEMPERATURE DEPENDENCE**

For all Cypress products operating under all conditions, the  $I_{CC}$  current increases as the temperature decreases. The  $I_{CC}$  temperature coefficient is -0.12% per °C. To calculate the percentage change in  $I_{CC}$  from one temperature to another, this temperature coefficient is multiplied by the temperature difference.

If, for example, it is required to calculate the expected reduction in  $I_{CC}$  if either a commercial or a military grade Cypress IC is operated at room temperature (25°C), the calculations are:

For commercial products

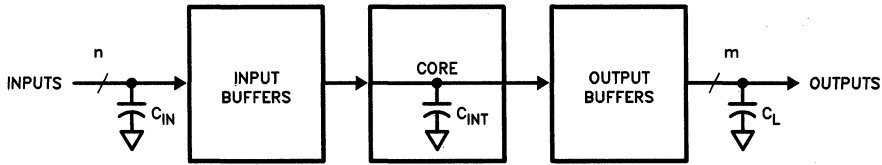
$$[0 - 25] \times [-0.12\%] = 3\% \text{ less } I_{CC} \text{ at room temperature than at } 0^\circ\text{C}.$$

For military products

$$[-55 - (25)] \times [-0.12\%] = 9.6\% \text{ less } I_{CC} \text{ at room temperature than at } -55^\circ\text{C}.$$

**Procedure**

The procedure will be to develop a general purpose power dissipation model that applies to all of the Cypress CMOS products and to then present tables so that users can estimate typical and worst case power dissipations for each product. The data will be presented in chart form as functions of product type and capacitance, that is: SRAM, PROM, PAL or Logic; including FIFOs.


**Figure 1. Power Dissipation Model**

0059-1

## Power Dissipation Model

A general purpose power dissipation model for all Cypress integrated circuits is shown in Figure 1.

The procedure will be to isolate the four components of power dissipation described by equation 6 by controlling the inputs to the IC. The quiescent ( $I_{CC}$ ) current is measured with the inputs to the IC at 0.4V or less. Under this condition the input buffers and output buffers (unloaded DC wise) draw only leakage currents. All other direct currents are due to the substrate bias generator, sense amplifiers, other internal voltage or current references and NMOS memory circuits.

At  $V_{IN} = 1.5V$  the input buffers draw maximum  $I_{CC}$  current. The total current is measured and the quiescent current subtracted to find the total input buffer  $I_{CC}$  current. The current per input buffer is then calculated by dividing the total input buffer current by the number of input buffers.

### INPUT BUFFERS

Three different types of input buffers are used in Cypress products. For purposes of illustration they are referred to as types A, B and C. Table 1 lists the maximum  $I_{CC}$ s.

**Table 1. Types of Input Buffers**

| Buffer Type | $I_{CC}$<br>(max. in mA) |
|-------------|--------------------------|
| A           | 1.3                      |
| B           | 0.8                      |
| C           | 0.6                      |

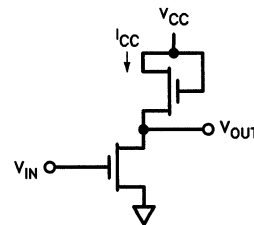
The schematics and input characteristics for the three types of buffers are illustrated in Figure 2. A circle on the gate of a transistor means that it is a P-channel device.

As can be seen from the figure, the input buffers draw essentially zero  $I_{CC}$  current when  $V_{IN}$  is 0.4V or less or

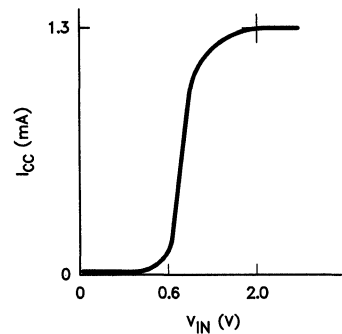
(except for type A) when  $V_{IN}$  is 4V or more. In other words, if the inputs are driven "rail to rail" the B and C input buffers will dissipate power only during the input signal transitions.

To reach these levels the input pins should be either driven by a CMOS driver or by a TTL driver whose output does not drive any other TTL inputs.

When the inputs are driven by the minimum TTL levels ( $V_{IH} = 2V$ ,  $V_{IL} = 0.8V$ ) each input buffer draws 20% more  $I_{CC}$  current than if it were driven rail to rail.


**Figure 2A**

0059-3


**Figure 2B  
Type A**

0059-4

Power Dissipation Model (Continued)

DUTY CYCLE CONSIDERATIONS

The input characteristics of the type B (Figure 2D) and the type C (Figure 2F) buffers may be approximated by triangles symmetric about the  $V_{IN} = 1.5V$  points, whose amplitudes are 0.8 mA and 0.6 mA, respectively. Therefore, between the  $V_{IN} = 0.5V$  and  $V_{IN} = 3.5V$  points the average current is one-half the peak current, or 0.4 mA and 0.3 mA, respectively. In most systems the input signal slew rates are two volts per nanosecond or greater so the input transitions occur quickly. Under these conditions the duty cycle of the input buffers must be considered.

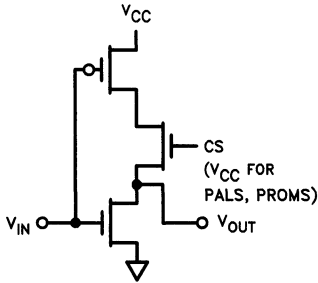


Figure 2C

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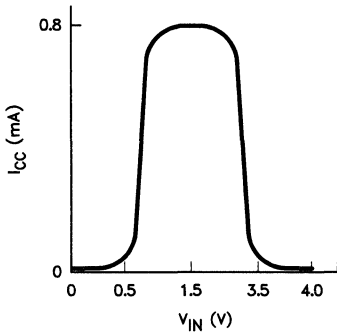


Figure 2D  
Type B

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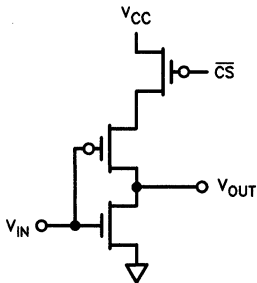


Figure 2E

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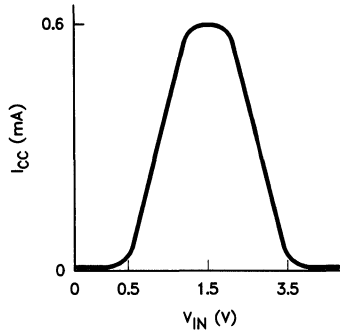


Figure 2F  
Type C

0059-8

For example, if the CY7C167-35 RAM were used with input signals having a slew rate of two volts per nanosecond it would take

$$[3.5V - 0.5V] \times \frac{1}{2V/ns} = 1.5 ns$$

for the input signals to go through the 3V transition. During the transition each input buffer would be drawing 0.3 mA of current from the  $I_{CC}$  supply. However, this time is only  $1.5 ns/35 ns = 0.0429$  or 4.29% of the access cycle. Therefore, the actual input buffer transient current is only  $0.0429 \times 0.3 mA = 0.01287 mA$ . It will be shown that this is insignificant in most power calculations.

INPUT BUFFER FREQUENCY DEPENDENT CURRENT

This is the current required to charge and discharge the capacitance associated with each input buffer. The capacitance is typically 5 pF and the voltage swing is typically 4V.

Using equation 3;  $I = CVf$

$$I_{CC}(f) = 5 \times 10^{-12} \times 4 \times f.$$

$$I_{CC}(f) = 20 \times 10^{-12}f.$$

CORE AND OUTPUT BUFFERS

The memory array will have a standby power dissipation due to the substrate bias generator, reference generators, sense amplifiers, and polyload RAM cells or EPROM cells. This current is measured with  $V_{IN} = 0V$ , so that the input buffers draw no current. Under these conditions the output buffers will draw only leakage current and dissipate essentially no power.

The output buffers have N-channel pullup devices that cause the output voltage level to reach  $V_{OH} = V_{CC} - 1V$ .

The capacitance of the output buffers, including stray capacitance, is typically 10 pF.

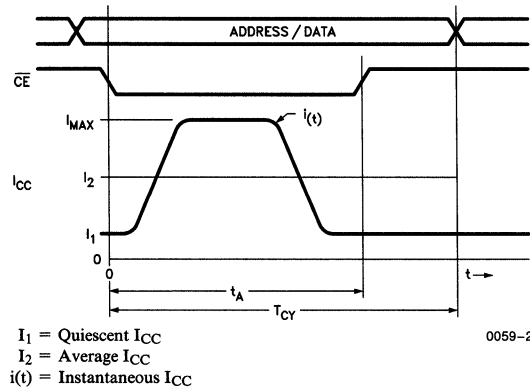
$$I_{CL} = 10 pF, V_{OH} \cong 4V.$$

Again, using equation 3,  $I_{CC}(f) = 40 \times 10^{-12}f$  for the output buffers.

## Current Measurement

### INSTANTANEOUS CURRENT

Figure 3 illustrates the instantaneous current drawn by a Cypress RAM. The instantaneous power is calculated by multiplying this current times the constant supply voltage,  $V_{CC}$ . Most of the power is dissipated in the time corresponding to the access time. This is also true for PROMs and PALs.



**Figure 3. RAM  $I_{CC}$**

### AVERAGE CURRENT

The current measurement unit in an automatic tester integrates the instantaneous current over the measurement cycle and arrives at an equivalent average current. In other words, the average current,  $I_2$ , during time  $T_{CY}$  is equal to the area between the instantaneous current,  $i(t)$ , and the X axis during  $T_{CY}$ . Therefore, when the frequency is decreased, the "current pulse" is (figuratively) spread over a longer time, so the average current is proportionately less.

### DC Load Current

Note that the preceding calculations have not accounted for any DC loads. The user must calculate these separately.

## Product Characteristic Tables

The following tables are listed to enable the user to calculate the current requirements for Cypress products.  $C_{INT}$  is the equivalent device internal capacitance,  $I_{CC}(Q)$  is the quiescent or DC current and  $I_{CC}(MAX)$  is the maximum  $I_{CC}$  current (as specified on the data sheet) for the commercial operating temperature range. Conditions are  $V_{CC} = 5V$  and  $T_A = 25^\circ C$ .

### STATIC RAMs

**Table 2**

| Part No.    | Buffer Type | No. Inputs | No. Outputs | $C_{INT}$ (pF) | $I_{CC}(Q)$ (mA) | $I_{CC}(Max.)$ (mA) |
|-------------|-------------|------------|-------------|----------------|------------------|---------------------|
| CY7C122/123 | A           | 16         | 4           | 24             | 50               | 90                  |
| CY7C128     | B           | 14         | 8           | 27             | 59               | 120                 |
| CY7C147     | B           | 15         | 1           | 34             | 28               | 90                  |
| CY7C148/149 | B           | 12         | 1           | 32             | 45               | 90                  |
| CY7C150     | B           | 18         | 4           | 20             | 44               | 90                  |

**Table 2 (Continued)**

| Part No.    | Buffer Type | No. Inputs | No. Outputs | $C_{INT}$ (pF) | $I_{CC}(Q)$ (mA) | $I_{CC}(Max.)$ (mA) |
|-------------|-------------|------------|-------------|----------------|------------------|---------------------|
| CY7C161/162 | B           | 22         | 4           | 300            | 13               | 70                  |
| CY7C164     | B           | 20         | 4           | 300            | 13               | 70                  |
| CY7C166     | B           | 21         | 4           | 300            | 13               | 70                  |
| CY7C167     | C           | 17         | 1           | 75             | 25               | 70                  |
| CY7C168/169 | C           | 18         | 4           | 75             | 50               | 70                  |
| CY7C170     | B           | 18         | 4           | 50             | 33               | 90                  |
| CY7C171/172 | B           | 18         | 4           | 100            | 27               | 70                  |
| CY7C185/186 | B           | 25         | 8           | 330            | 13               | 100                 |
| CY7C187     | B           | 19         | 1           | 150            | 7                | 100                 |
| CY7C189/190 | B           | 10         | 4           | 21             | 32               | 90                  |

### PROMs

**Table 3**

| Part No.    | Buffer Type | No. Inputs | No.* Outputs | $C_{INT}$ (pF) | $I_{CC}(Q)$ (mA) | $I_{CC}(Max.)$ (mA) |
|-------------|-------------|------------|--------------|----------------|------------------|---------------------|
| CY7C225     | B           | 12         | 8            | 32             | 35               | 90                  |
| CY7C235     | B           | 13         | 8            | 35             | 35               | 90                  |
| CY7C245     | B           | 13         | 8            | 35             | 50               | 90                  |
| CY7C251     | C           | 18         | 8            | 43             | 9.5              | 100                 |
| CY7C254     | C           | 18         | 8            | 43             | 35               | 100                 |
| CY7C261/3/4 | C           | 14         | 8            | 60             | 45               | 100                 |
| CY7C268     | C           | 19         | 1/8          | 60             | 60               | 100                 |
| CY7C269     | C           | 17         | 1/8          | 60             | 60               | 100                 |
| CY7C281/282 | B           | 14         | 8            | 35             | 35               | 100                 |
| CY7C291/292 | B           | 14         | 8            | 35             | 50               | 100                 |

\*/Bidirectional pins

### PALs

For the 16L8, 16R8, 16R6 and 16R4 the number of inputs and outputs is, within limits, user configurable. All use type B buffers.

**Table 4**

| Part No.          | $C_{INT}$ (pF) | $I_{CC}(Q)$ (mA) | $I_{CC}(Max.)$ (mA) |
|-------------------|----------------|------------------|---------------------|
| PALC16L8/R8/R6/R4 | 40             | 25               | 45                  |
| PLDC20G10         | 50             | 30               | 55                  |
| PALC22V10         | 50             | 40               | 80                  |
| PLDCY7C330        | 300            | 42               | 120                 |

## LOGIC PRODUCTS

**Table 5**

| Part No.  | Buffer Type | No. Inputs | No.* Outputs | $C_{INT}$ (pF) | $I_{CC}(Q)$ (mA) | $I_{CC}(Max.)$ (mA) |
|-----------|-------------|------------|--------------|----------------|------------------|---------------------|
| CY7C401   | B           | 6          | 6            | 53             | 30               | 75                  |
| CY7C402   | B           | 7          | 7            | 53             | 30               | 75                  |
| CY7C403   | B           | 7          | 6            | 53             | 30               | 75                  |
| CY7C404   | B           | 8          | 7            | 53             | 30               | 75                  |
| CY7C408   | B           | 11         | 12           | 100            | 42               | 135                 |
| CY7C409   | B           | 11         | 13           | 100            | 42               | 135                 |
| CY7C428/9 | C           | 14         | 12           | 190            | 18               | 80                  |
| CY7C510   | C           | 24         | 19/16        | 60             | 30               | 100                 |
| CY7C516   | C           | 28         | 16/16        | 60             | 30               | 100                 |
| CY7C517   | C           | 28         | 16/16        | 60             | 30               | 100                 |
| CY3341    | B           | 6          | 6            | 53             | 30               | 45                  |
| CY7C601   | C           | 25         | 19/64        | 950            | 89               | 600                 |

**Product Characteristic Tables (Continued)**
**Table 5 (Continued)**

| Part No. | Buffer Type | No. Inputs | No.* Outputs | C <sub>INT</sub> (pF) | I <sub>CC</sub> (Q) (mA) | I <sub>CC</sub> (Max.) (mA) |
|----------|-------------|------------|--------------|-----------------------|--------------------------|-----------------------------|
| CY7C901  | C           | 24         | 10/4         | 160                   | 25                       | 80                          |
| CY7C909  | C           | 21         | 5            | 80                    | 25                       | 55                          |
| CY7C910  | C           | 22         | 16           | 150                   | 2.6                      | 70                          |
| CY7C911  | C           | 13         | 5            | 80                    | 25                       | 55                          |
| CY7C9101 | C           | 36         | 22/4         | 70                    | 30                       | 60                          |
| CY7C9116 | C           | 22         | 1/20         | 1000                  | 35                       | 150                         |
| CY7C9117 | C           | 38         | 1/4          | 1000                  | 35                       | 150                         |

\*/Bidirectional pins

**Static RAM Example**

To illustrate how to use the preceding tables and perform the required calculations the following example is provided.

Estimate the typical I<sub>CC</sub> current for the CY7C169-35 RAM at room temperature (T<sub>A</sub> = 25°C) and V<sub>CC</sub> = 5V. Assume the duty cycle is 100% at the specified access time. Calculate typical and worst case I<sub>CC</sub> (all inputs and outputs changing) with output loading of 10 pF.

From the RAM product characteristic table;

$$\# \text{ inputs} = 18$$

$$\# \text{ outputs} = 4$$

$$C_{INT} = 75 \text{ pF}$$

$$I_{CC} (Q) = 50 \text{ mA}$$

**TRANSIENT INPUT BUFFER CURRENT**

The input buffers on the CY7C169 are type C, so the average current is 0.3 mA. If the input signal level transitions are 4V and the transition times are 2 V/ns, the transition time is:

$$T_t = \frac{4V}{2 \text{ V/ns}} = 2 \text{ ns.}$$

The duty cycle is then;

$$2 \text{ ns}/35 \text{ ns} = 0.057.$$

Therefore, each input buffer draws

$$0.3 \text{ mA} \times 0.057 = 0.0171 \text{ mA.}$$

If all inputs change, the total transient input buffer current is

$$18 \times 0.0171 = 0.31 \text{ mA.}$$

**CVf Input Buffer Current**

$$I = CVf \quad C_{IN} = 5 \text{ pF}$$

$$I = 0.57 \text{ mA} \quad V = 4V$$

$$f = 1/35 \text{ ns}$$

$$\text{Total} = 18 \times 0.57 = 10.28 \text{ mA}$$

**Internal CVf Current**

$$I = CVf \quad C_{INT} = 75 \text{ pF}$$

$$I = 10.71 \text{ mA} \quad V = 5V$$

$$f = 1/35 \text{ ns}$$

**Output CVf Current**

$$I = CVf \quad C_{OUT} = 10 \text{ pF}$$

$$I = 1.15 \text{ mA} \quad V = 4V$$

$$f = 1/35 \text{ ns}$$

$$\text{Total} = 4 \times 1.15 = 4.6 \text{ mA}$$

The Quiescent Current is 50 mA

The Total Current At TCY = 35 ns is;

$$\text{Input Transient} \quad 0.31 \text{ mA}$$

$$\text{Input CVf} \quad 10.28 \text{ mA}$$

$$\text{Internal CVf} \quad 10.71 \text{ mA}$$

$$\text{Output CVf} \quad 4.6 \text{ mA}$$

$$\text{Quiescent} \quad 50 \text{ mA}$$

$$\text{Total } I_{CC} \quad 75.9 \text{ mA (all inputs/outputs changing)}$$

Note that the worst case transient current is 25.9 mA.

If one-half of the inputs and outputs change this is reduced to 12.95 mA, which gives a total current of 63 mA (typical I<sub>CC</sub>).

If the duty cycle is 10% the transient current is reduced to 1.3 mA, which results in a total current of 51.3 mA.

Note also that the Input CVf current and the output CVf current would have the same values for a bipolar device.

**WORST, WORST, WORST CASE I<sub>CC</sub>**

Next, let's estimate the I<sub>CC</sub> for worst case V<sub>CC</sub> and low temperature, in addition to all inputs and outputs changing and compare it with the I<sub>CC</sub> specified on the data sheet.

The I<sub>CC</sub> current will be greater at high V<sub>CC</sub>, which is 5.5V or 1.1 × the nominal 5V V<sub>CC</sub>. The increase in I<sub>CC</sub> due to the lower temperature is 3%, so the total increase is 13%. These factors apply to the internal CVf current (10.71 mA), the output CVf current (4.6 mA), and the quiescent current (50 mA), (total 65.31 mA).

$$\text{Total } I_{CC} = \text{Input Transient } I_{CC} + \text{Input CVf } I_{CC} +$$

$$[\text{Internal CVf} + \text{Output CVf} + I_{CC}(Q)] \times 1.13$$

$$I_{CC} = 0.31 + 10.28 + [65.31] \times 1.13 = 84.4 \text{ mA.}$$

This is approximately 94% of the 90 mA specified on the data sheet.

Note, however, that the data sheet I<sub>CC</sub> maximum does NOT include the output CVf current.

**Typical I<sub>CC</sub> Versus Frequency Characteristic**

The I<sub>CC</sub> versus frequency curves for all Cypress products have the same basic shape, which is illustrated by the PAL 16R8 curve of Figure 4. The current remains essentially constant at the quiescent I<sub>CC</sub> value until the frequency increases to the point where the capacitances begin to cause appreciable currents. This point depends upon the capacitances (input, internal, and output), the number of inputs and outputs, the rate at which they change, and the voltage levels that they are switched between. For Cypress products this point is in the 1–10 MHz range.



### Typical $I_{CC}$ Versus Frequency Characteristic (Continued)

The PAL 16R8 devices that were tested to obtain the data for the curve were exercised such that all inputs and all outputs changed every cycle. Curve A shows the total  $I_{CC}$  current for a 50 pF load on each of the eight outputs. Curve B shows the total  $I_{CC}$  current when the outputs are disabled. The B curve results from the input and the internal capacitances. In most applications the actual operation of the device will be somewhere between the A and B curves.

The A and B curves may be extrapolated backwards until they intersect the quiescent current (point C in Figure 4).

Point C is approximately 5.6 MHz. This gives the user an easy to use approximate formula to calculate the  $I_{CC}$  current.

For frequencies less than 5.6 MHz

$$I_{CC} = I_{CC}(Q) = 25 \text{ mA}$$

For frequencies greater than 5.6 MHz

$$I_{CC} = I_{CC}(Q) + 3.5 \text{ mA per MHz (all outputs changing)}$$

or,

$$I_{CC} = I_{CC}(Q) + 0.5 \text{ mA per MHz (no outputs changing)}$$

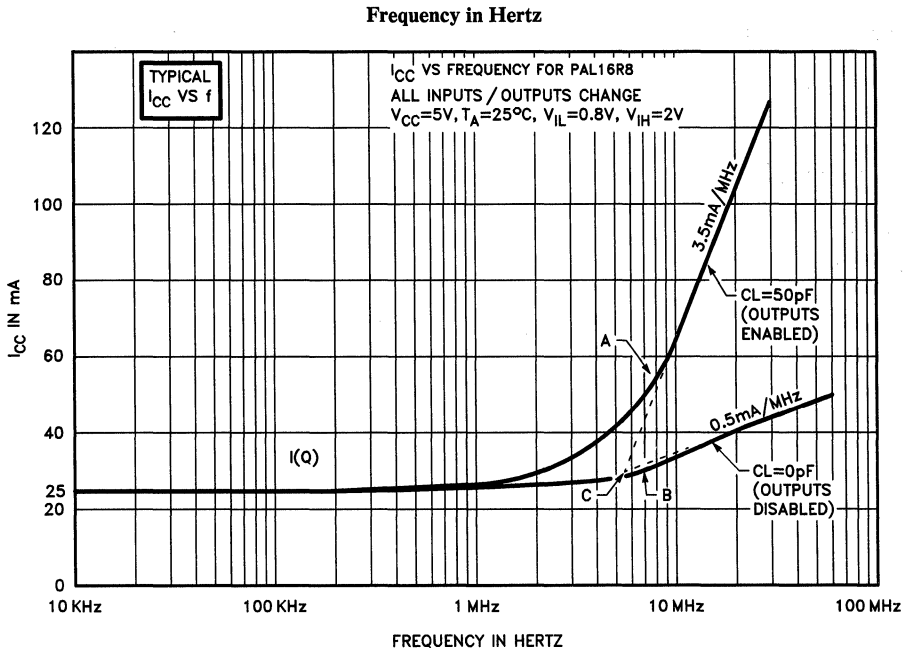


Figure 4. Typical  $I_{CC}$  vs f



# Pin-Out Compatibility Considerations of SRAMs and PROMs

When looking for pin compatible replacements for PROMs, there are a number of key parameters that must be met. This application brief discusses the non-electrical parameters of pin-out and programming involved in finding socket compatible second sources for PROMs. Comparison with the selection of a socket compatible SRAM second source is provided. Additionally, an example of a verified conversion from the Motorola 68764 to the Cypress CY7C264, a PROM conversion that is not address line compatible, is presented.

Ignoring the AC/DC characteristics, finding a second source for an SRAM is relatively simple. As long as the power, ground, control (chip select, read, write), address, and data lines are on the same pins the devices should be compatible. **Specifically, on SRAMs, the address and data lines need not be numbered identically between the two devices being compared for them to function identically in the same socket.** As an example, on several Cypress SRAMs, the address pin numbering is not the same as some of our competitors. Let's look at a simplified example that illustrates why this is not a problem. Let's assume that we have a new device, the 2 bit x 4 location SRAM:

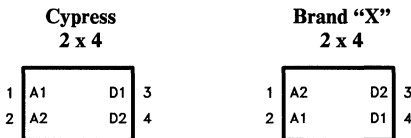


Figure 1. Example 2 x 4 Simplified SRAMs

Note that the inferior pin-out chosen by the Brand "X" 2 x 4 assigns Address line 2 (A2) to pin 1 whereas the superior pin-out used by the Cypress device has A1 at pin 1, etc. It is our assertion that these simplified devices are pin compatible. Let's assume that our engineering staff designed an infrared scanning pattern recognizing toaster oven with the Brand "X" data sheet. Just as your company is about to ramp into volume production, Brand "X" sends out an End Of Life notice on their 2 x 4, because they are converting all of their capacity to making DRAM memories. At this point, you have no desire to layout a new PC board, so let's take a look at how these devices would look in your design.

In this case,  $\mu P$  is a microprocessor interfacing to the SRAM. What is of key importance is that the data read from a given address generated by the microprocessor is

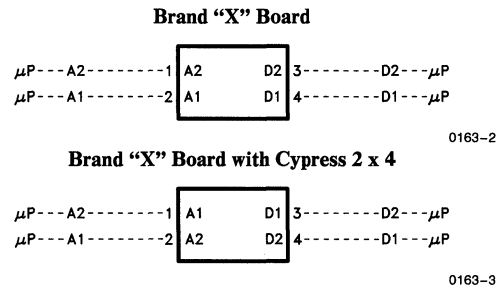


Figure 2. Example System with 2 x 4 SRAMs

the same as data written to the same location earlier. With the SRAM, any inconsistency between the Address and Data line numbering does not really matter because the data read will be the same as the data previously written. This occasionally causes some concern with customers who have not seen this before. To illustrate our point, suppose that we write a value of 1 ( $\mu P:D2, D1 = 0, 1$ ) at location 2 ( $\mu P:A2, A1 = 1, 0$ ). If we read location 2, we will obtain the value 1 that was written, because the address presented to the SRAM during the read is the same as the address for the previous write. Similarly, the data read will be in the same bit order as presented during the previous write to the location. As far as our system is concerned, the two SRAM devices are compatible. The only difference, which is not significant to our system, is where the data was physically stored inside the SRAM. In the Cypress device, the  $\mu P$  address of 2 ( $\mu P:A2, A1 = 1, 0$ ) actually stored the data at SRAM location 2 (Cypress:A2, A1 = 0, 1). In the brand X RAM, the data is physically stored in location 1. However, the address translation is transparent to the  $\mu P$ . Since the same location is accessed for the subsequent reads, the difference in address numbering between the two devices doesn't really matter to our system. Similarly, any numbering difference on the data lines doesn't matter either. The point that is of primary importance here is that for SRAMs, all writes and reads are generated in your system, and so long as the address and data lines are on the same pins, differences in the numbering don't matter.

For PROMs, the scenario becomes slightly more complex. Since PROMs are programmed using a programmer that is separate from the system in which they are used, it becomes more difficult to substitute a PROM with a device that does not have the same address and/or data pin

numbering. Let's assume that our Hi-Tek toaster oven's 2 x 4 are now PROMs. If we programmed each location with data, we would find that the Cypress device would not work properly when used in the Brand "X" designed socket. In this case our programmer put the data at location 2, and board would read this data when the microprocessor requested the data at location 1. Additionally, the data bits will be swapped on this read. What a mess! It becomes apparent that it is easiest to replace this PROM with a device that has the same address and data line numbering. There are still methods that we can use that will allow us to use the Cypress 2 x 4 PROM in this socket.

The objective in trying to make the Cypress PROM work in the foreign pin-out socket is to have the data read by the system be the same as the data read when the Brand "X" device is used. In our 2 x 4 example, there are two problems—address line numbering mismatch and Data line numbering mismatch. Let's first address the data line mismatch. As it stands, data that was written in as bit1,bit2 is read as bit2,bit1 or swapped. If we were able to change our PC Board layout, we could fix this problem by swapping the printed traces for D1 and D2. Unfortunately, this would prevent the use of the Brand "X" device on our board. We can internally swap the data bits in the Cypress device, then they would be in the correct order. This swapping of the data bits in the Cypress device can be achieved through several means. First, we might modify our programming adapter such that D2 and D1 are swapped from the normal order when programming the part. Then when the device is read, we would get the bits in the same order as presented by the Brand "X" device. This is not a recommended method of solving the problem, because modifying programmers tends to make the manufacturer of the programmer unhappy. A second method of solving this problem is to alter the binary image of the PROM contents such that bits D1 and D2 are swapped in a file on your computer's disk, then using this altered binary image file to program the Cypress PROM. This is less likely to cause damage than modifying a programmer, but requires some skill in altering the binary file. Finally, the easiest solution to this problem is to trick the PROM programmer into swapping the bits for you. If you set your programmer for the Cypress device type, read a programmed Brand "X" device into memory, then program the Cypress part with the image in programmer memory, the bits will have been swapped for you. Let's look at how this works.

- |                         |               |
|-------------------------|---------------|
| 1) Brand "X" 2 x 4      | :Bit 2, Bit 1 |
| 2) Programmer (Cypress) | :Bit 1, Bit 2 |
| 3) Cypress 2 x 4        | :Bit 1, Bit 2 |
| 4) System Board $\mu$ P | :Bit 2, Bit 1 |

**Figure 3. PROM Bit Swapping with Programmer**

From the diagram above, we can see that the bits in the Brand "X" device are stored in the order Bit2,Bit1. This is the same order that the  $\mu$ P will read them on our board. When we set the programmer to read the Cypress part, the data lines are logically swapped from the Brand "X" ordering. Thus when we read the Brand "X" part, the data bits will be swapped as shown. When the Brand "X" part is removed from the socket, and the Cypress device is plugged in and programmed, the bits will be programmed into the Cypress part in this same 'reversed' order. When we place the Cypress part into our board, the bits will be

swapped again due to the difference in numbering between the Cypress part and the board layout, and the  $\mu$ P will get the data in the correct order.

The second problem that exists is the difference in address line numbering. This problem can be resolved in exactly the same manner as the data swap problem. By simply setting the programmer to the Cypress device type, reading the Brand "X" part, then programming the Cypress part, any addressing differences will be solved allowing the use of the Cypress device. The difference here is that the location of data words will be swapped to allow for the difference in pin-outs, just as the bits were swapped in the data line mismatch case.

Many programmers will allow you to read a device different than the part selected, complaining only during a program if the device types do not match. With such a programmer, carrying out the above procedures to convert a PROM should not present a problem. However, there are some programmers that will not allow the user to read a device if it is different from the part selected. These programmers will prevent our method from working. Fortunately, the Cypress' CY3000 QuickPro programmer will allow this approach to solving our problem. Cypress Field Applications Engineers, Sales Offices and Distributors can use their QuickPro to generate a Cypress master PROM that can be used as a source for copying with un-cooperative programmers.

As an example of such a conversion, the Motorola 68764 8K x 8 PROM has a similar pin-out to the Cypress 7C264 with the exception of address lines 10, 11, and 12.

| Pin | Cypress 7C264 | Motorola 68764 |
|-----|---------------|----------------|
| 21  | A10           | A12            |
| 19  | A11           | A10            |
| 18  | A12           | A11            |

**Figure 4. Cypress 7C264 vs. Motorola 68764 Pin-Out**

The following procedure will program a Cypress 7C264 such that it will work properly in a socket designed to accept Motorola device.

- 1) Invoke the Cypress QuickPro (or other usable programmer) and select the Cypress 7C264 as the device to be programmed.
- 2) Place the Motorola part in the programmer adapter socket and read the device. Optionally write the device contents to a disk file.
- 3) Place a Cypress 7C264 into the programmer adapter socket and program the part. Optionally the contents of the disk file may be read as the source for programming.

The programmed device will now work in the Motorola designed socket.

### Summary

If the pins used for power, ground, control, address, and data line numbering are the same for two devices, they may be used in the same socket if the other electrical parameters are compatible. Differences in Address and Data line numbering are of no consequence in SRAM use. Differences in Address and Data line numbering in a PROM device can be compensated for by using a simple programming procedure.

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PACKAGES 15





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## Packages

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# Thermal Management and Component Reliability

One of the key variables determining the long-term reliability of an integrated circuit is the junction temperature of the device during operation. Long-term reliability of the semiconductor chip degrades proportionally with increasing temperatures following an exponential function described by the Arrhenius equation of the kinetics of chem-

ical reactions. The slope of the logarithmic plots is given by the activation energy of the failure mechanisms causing thermally activated wear out of the device (*Figure 1*).

Typical activation energies for commonly observed failure mechanism in CMOS devices are shown in Table 2.

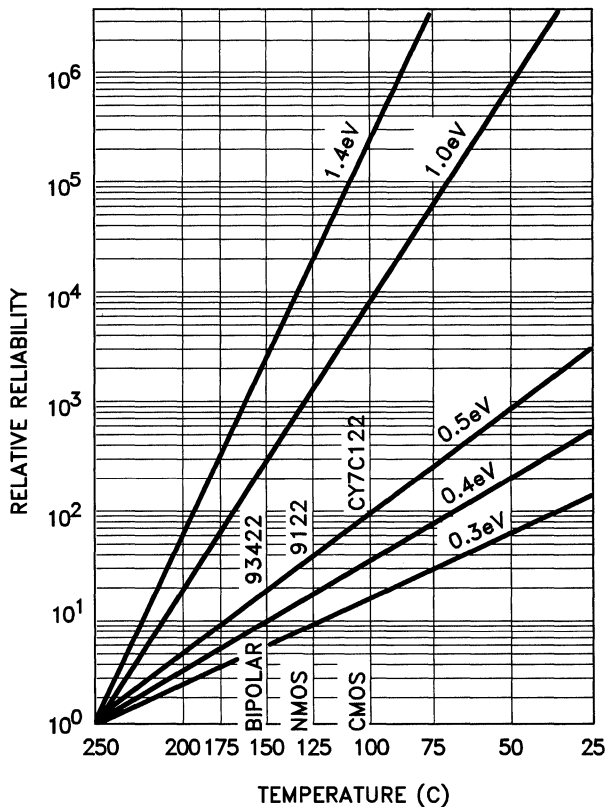


Figure 1. Arrhenius plot, which assumes a failure rate proportional to  $\text{EXP}(-E_A/kT)$  where  $E_A$  is the activation energy for the particular failure mechanism



**Table 2. Failure Mechanisms and Activation Energies in CMOS Devices**

| Failure Mode       | Approximate Activation Energy (EQ) |
|--------------------|------------------------------------|
| Oxide Defects      | 0.3 eV                             |
| Silicon Defects    | 0.3 eV                             |
| Electromigration   | 0.6 eV                             |
| Contact Metallurgy | 0.9 eV                             |
| Surface Charge     | 0.5–1.0 eV                         |
| Slow Trapping      | 1.0 eV                             |
| Plastic Chemistry  | 1.0 eV                             |
| Polarization       | 1.0 eV                             |
| Microcracks        | 1.3 eV                             |
| Contamination      | 1.4 eV                             |

To reduce thermally-activated reliability failures, Cypress Semiconductor has optimized both their low power generating 1.2 $\mu$  CMOS device fabrication process and their high heat dissipation packaging capabilities. Table 3 demonstrates this optimized thermal performance by comparing bipolar, NMOS and Cypress high speed 1K SRAM CMOS devices in their respective plastic packaging environments under standard operating conditions.

**Table 3. Thermal Performance of Fast 1K SRAMS in Plastic Packages**

| Technology   | Bipolar | NMOS | Cypress CMOS |
|--|---------|------|--------------|
| Device Number  | 93422   | 9122 | 7C122        |
| Speed (ns)   | 30      | 25   | 25           |
| I <sub>CC</sub> (mA)                                       | 150     | 110  | 60           |
| V <sub>CC</sub> (V)  | 5.0     | 5.0  | 5.0          |
| P <sub>MAX</sub> (MW)                                      | 750     | 550  | 300          |
| Package RTH (JA) (°C/W)                                    | 120     | 120  | 70           |
| Junction Temperature (°C) at Data Sheet P <sub>MAX</sub> * | 160     | 136  | 91           |

\*T<sub>ambient</sub> = 70°C

The Cypress 7C122 device, during its normal operation, experiences a 91°C junction temperature, whereas competitive devices in their respective packaging environments see a 45°C and 69°C higher junction temperature. In terms of relative reliability life expectancy, assuming a 1.0 eV activation energy failure mechanisms, this translates into an improvement in excess of two orders of magnitude (100X) over the bipolar 93422 device and more than one order of magnitude (30X) over the NMOS 9122 device.

## Thermal Performance Data of Cypress Component Packages

The thermal performance of a semiconductor device in its package is determined by many factors, including package design and construction, packaging materials, chip size, chip thickness, chip attachment process and materials, package size, etc.

### Thermal Resistance ( $\theta_{JA}$ , $\theta_{JC}$ )

For a packaged semiconductor device, heat generated near the junction of the powered chip causes the junction temperature to rise above the ambient temperature. The total thermal resistance is defined as,

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

and  $\theta_{JA}$  physically represents the temperature differential between the die junction and the surrounding ambient at a power dissipation of 1 watt.

The junction temperature is given by the equation:

$$T_J = T_A + P [\theta_{JA}] = T_A + P [\theta_{JC} + \theta_{CA}]$$

where:

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad \text{and} \quad \theta_{CA} = \frac{T_C - T_A}{P}$$

T<sub>A</sub> = Ambient temperature at which the device is operated; Most common standard temperature of operation equals 70°C

T<sub>J</sub> = Junction temperature of the IC chip

T<sub>C</sub> = Temperature of the case (package)

P = Power at which the device operates

$\theta_{JC}$  = Junction to case thermal resistance

$\theta_{JA}$  = Junction to ambient thermal resistance

$\theta_{CA}$  = Case to ambient thermal resistance

The junction-to-ambient environment is a still-air environment where the device is inserted into a low-cost standard device socket and mounted on a standard .062" G10 PC board. For junction-to-case measurements, the same assembly is immersed into a constant temperature liquid reservoir approaching infinite heat sinking for the heat dissipated from the package surface.

The thermal resistance values of Cypress standard packages are graphically illustrated in Figures 4 through 7. Each envelope represents a spread of typical Cypress integrated circuit chip sizes (upper boundary = 5000 Mils<sup>2</sup>, lower boundary = 30,000 Mils<sup>2</sup>) in their thermally optimized packaging environment.

All thermal characteristics are measured using the TSP (Temperature Sensitive Parameter) test method described in MIL STD 883C, Method 1012.1. A thermal silicon test chip, containing a 25 $\Omega$  diffused resistor to heat the chip and a calibrated TSP diode to measure the junction temperature, is used for all characterizations.

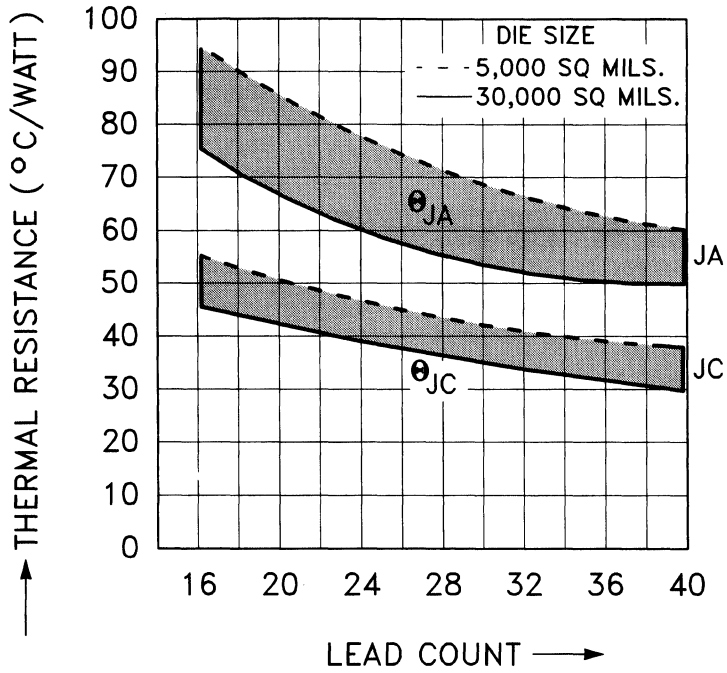


Figure 4. Thermal Resistance of Cypress Plastic DIP Packages

0064-2

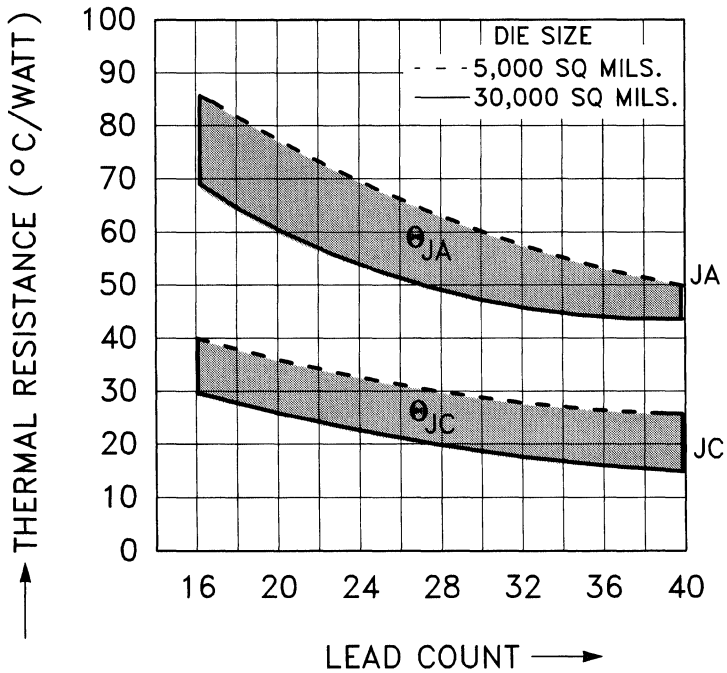


Figure 5. Thermal Resistance of Cypress Cerdip Packages

0064-3

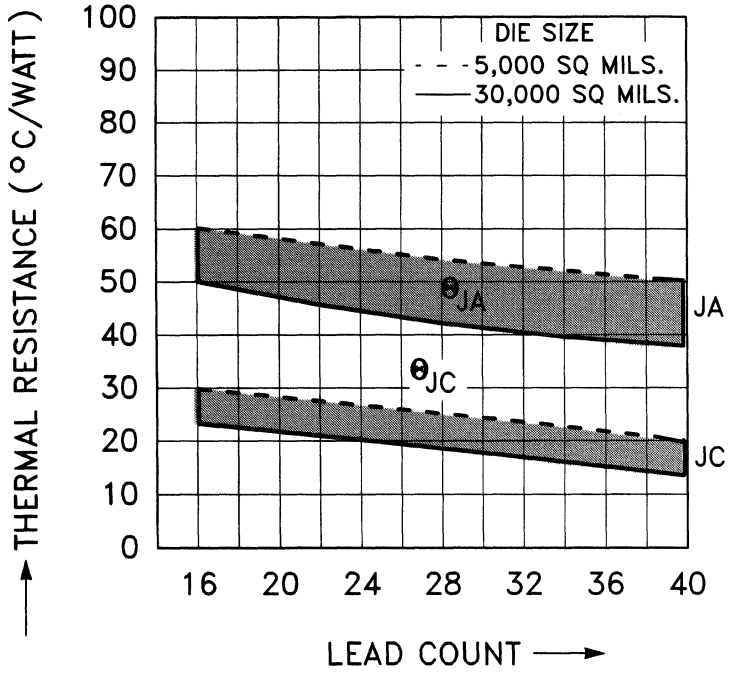


Figure 6. Thermal Resistance of Cypress Hermetic Chip Carriers (HLCC)

0064-4

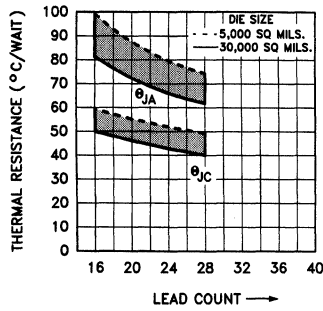


Figure 7. Thermal Resistance of Cypress SOICs

0064-5

## **Packaging Materials**

### **CYPRESS PLASTIC PACKAGES INCORPORATE:**

- High thermal conductivity copper lead frame.
- Molding compound with high thermal conductivity.
- Silver filled conductive epoxy as die attach material.
- Gold bond wires.

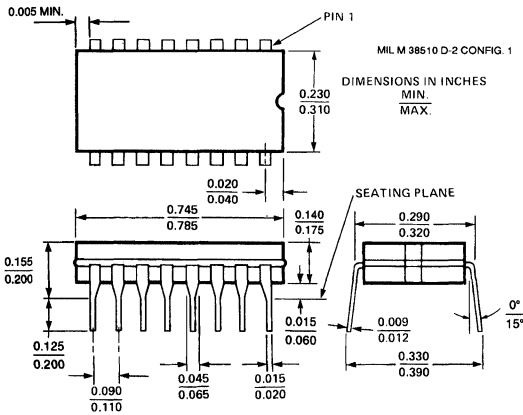
### **CYPRESS CERDIP PACKAGES INCORPORATE:**

- High conductivity Alumina substrates.
- Silver filled glass as die attach material.
- Alloy 42 lead frame.
- Aluminum bond wires.

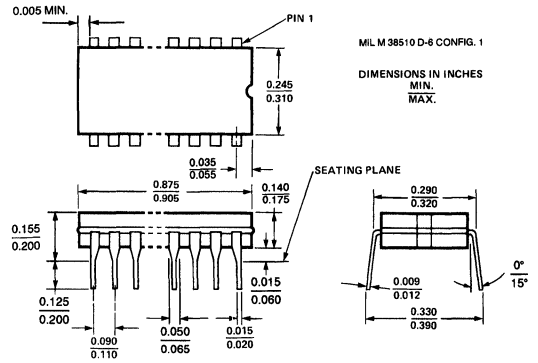


# Package Diagrams

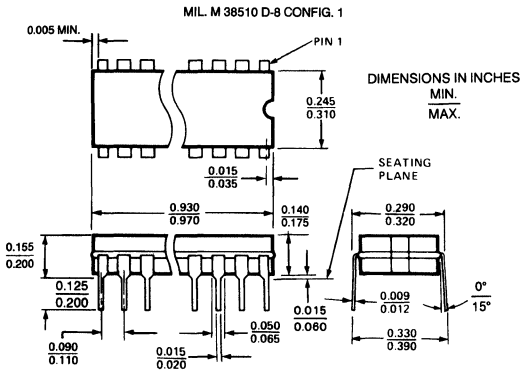
### 16 Lead (300 MIL) Cerdip D2



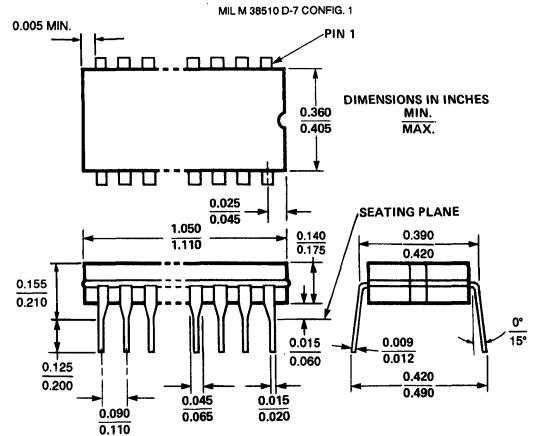
### 18 Lead (300 MIL) Cerdip D4



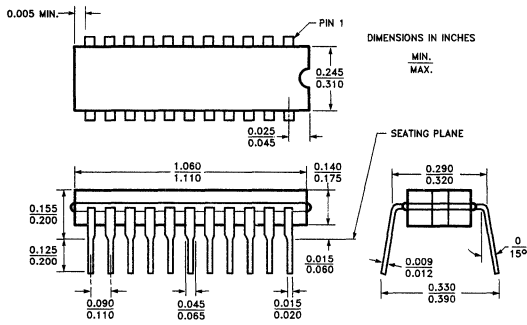
### 20 Lead (300 MIL) Cerdip D6



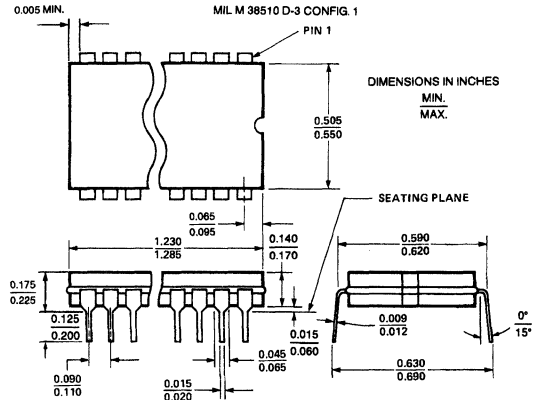
### 22 Lead (400 MIL) Cerdip D8



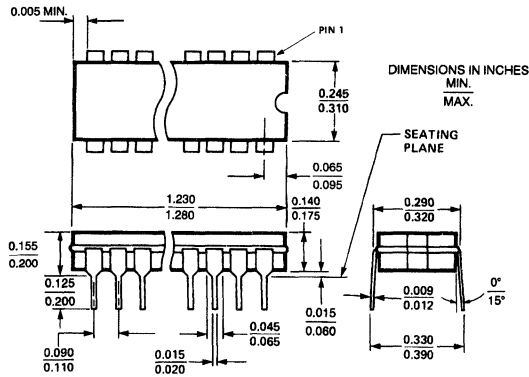
22 Lead (300 MIL) Cerdip D10



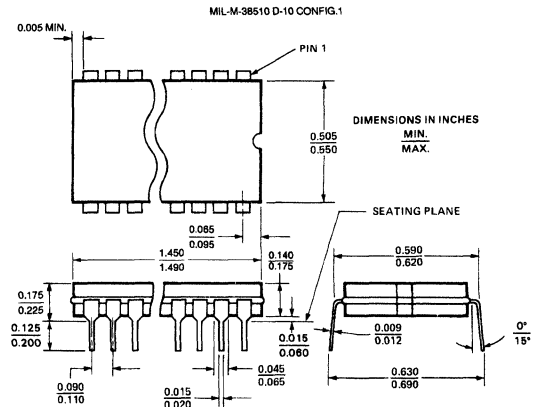
24 Lead (600 MIL) Cerdip D12



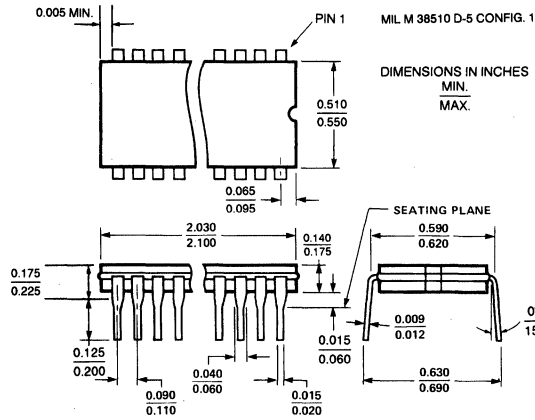
24 Lead (300 MIL) Cerdip D14



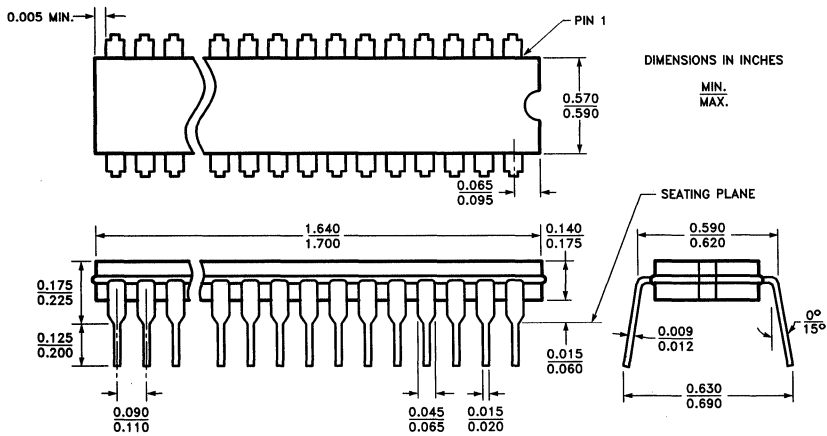
28 Lead (600 MIL) Cerdip D16



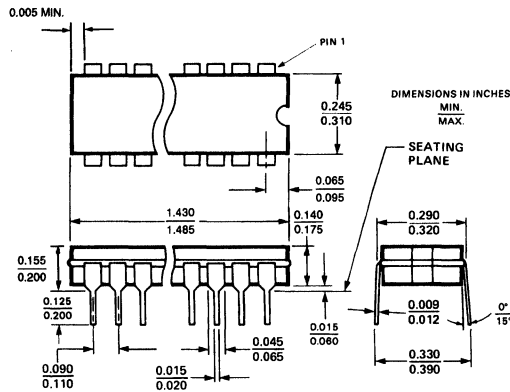
40 Lead (600 MIL) Cerdip D18



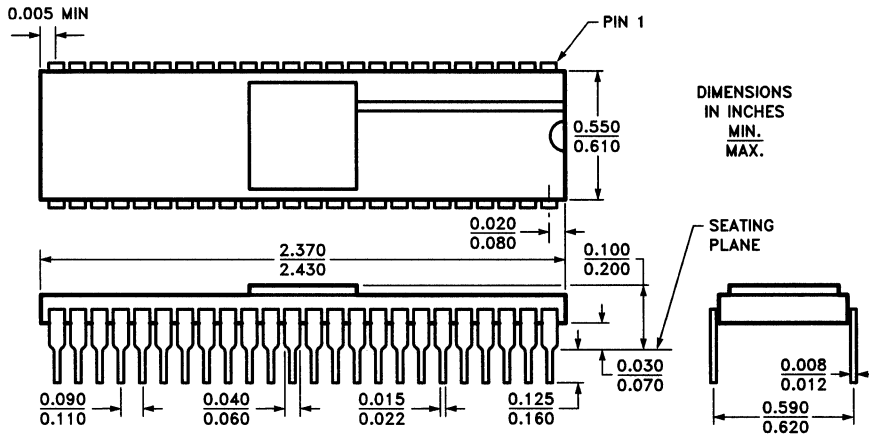
32 Lead (600 MIL) Cerdip D20



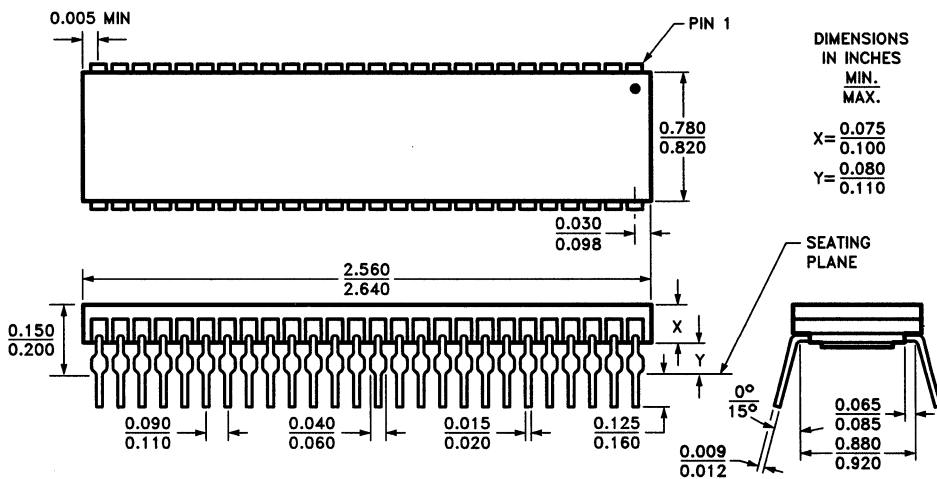
28 Lead (300 MIL) Cerdip D22



48 Lead (600 MIL) Sidebrazed DIP D26

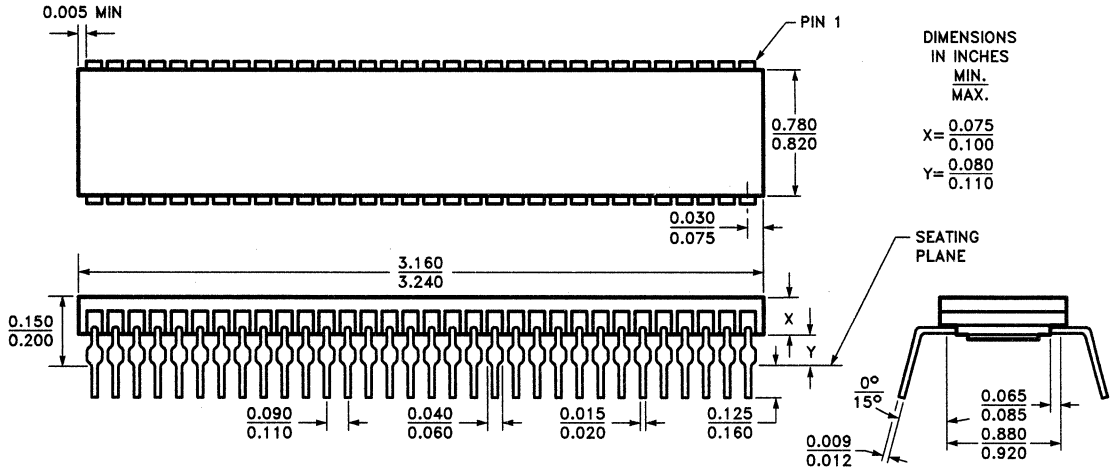


52 Lead (900 MIL) Bottombrazed DIP D28

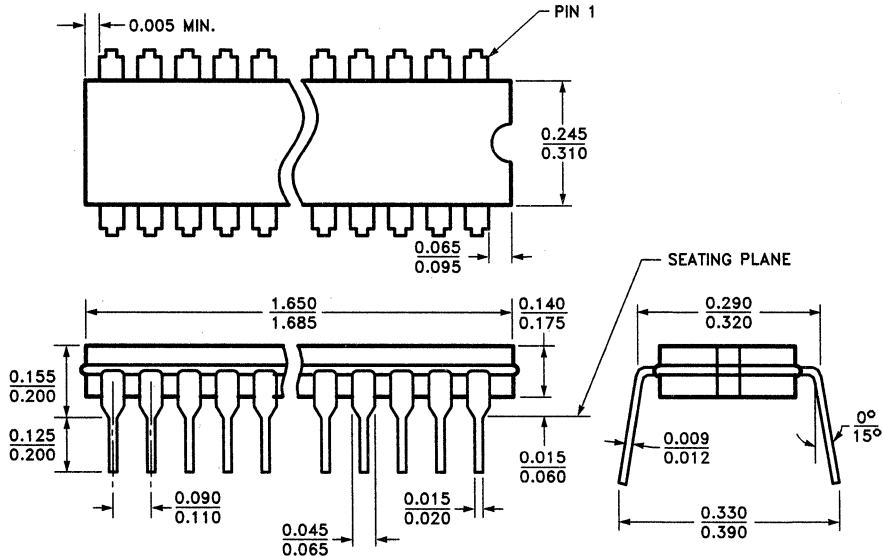




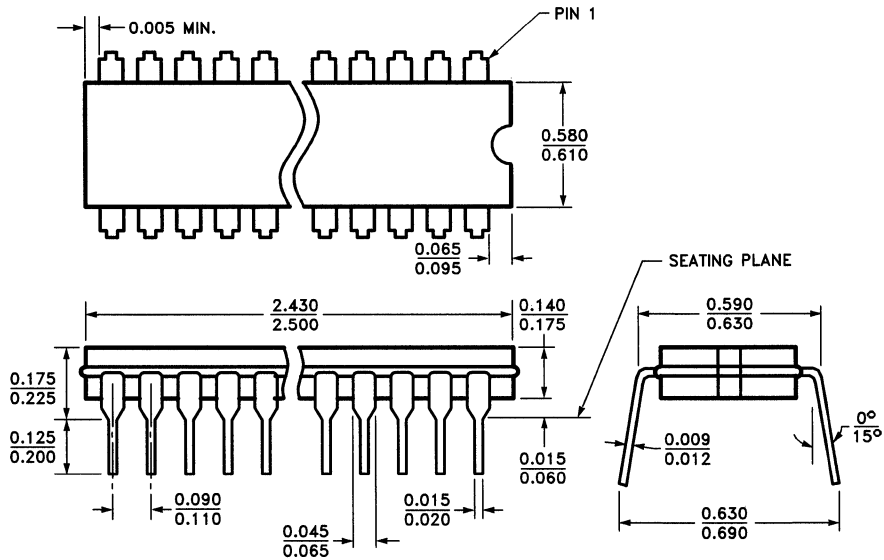
64 Lead (900 MIL) Bottombrazed DIP D30



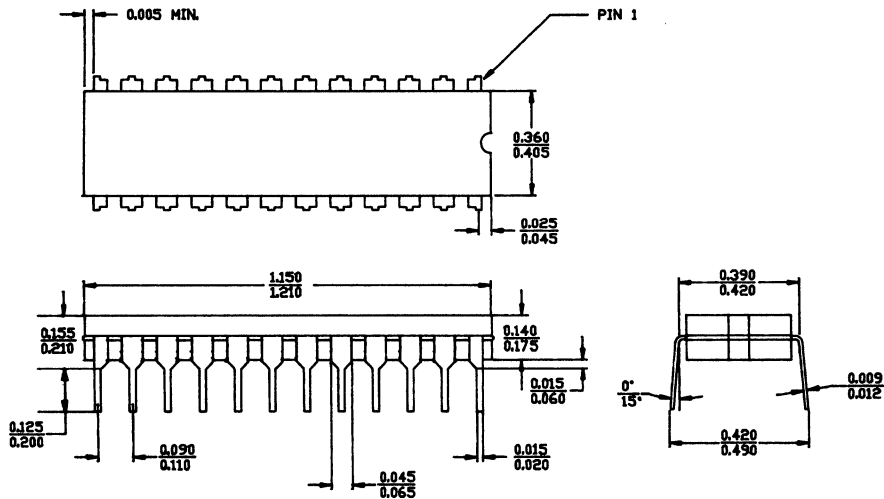
32 Lead (300 MIL) Cerdip D32



48 Lead (600 MIL) Cerdip D34

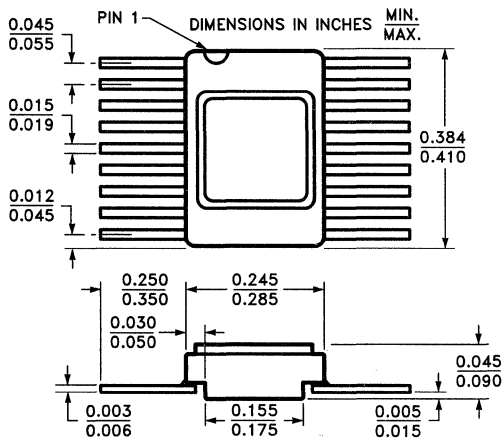


24 Lead (400 MIL) Cerdip D40

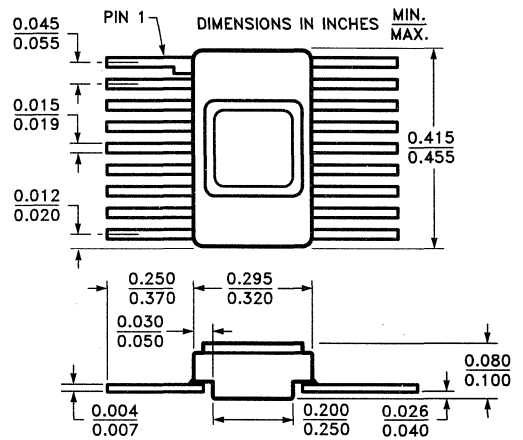


**16 Lead Rectangular Flatpack F69**

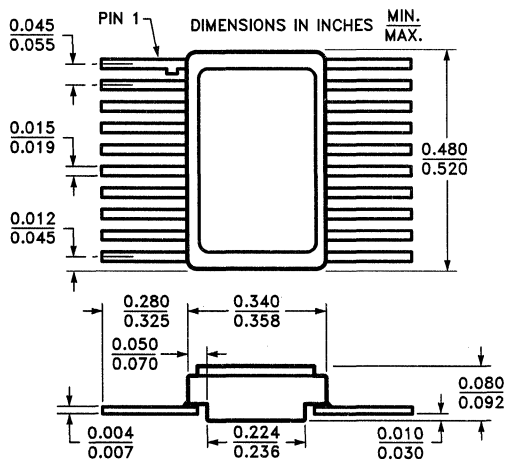
(MIL-M-38510 F-5 CONFIG 2)



**18 Lead Rectangular Flatpack F70**

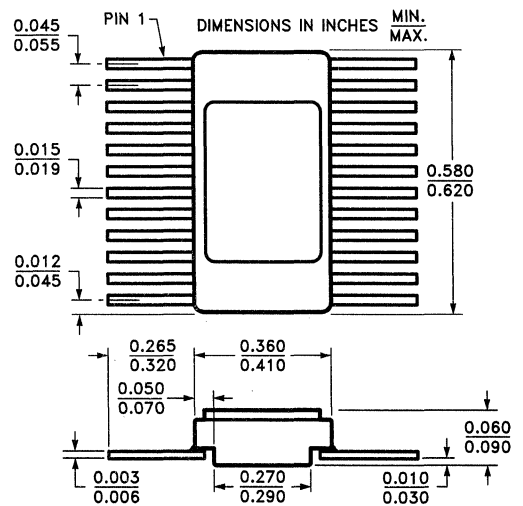


**20 Lead Rectangular Flatpack F71**

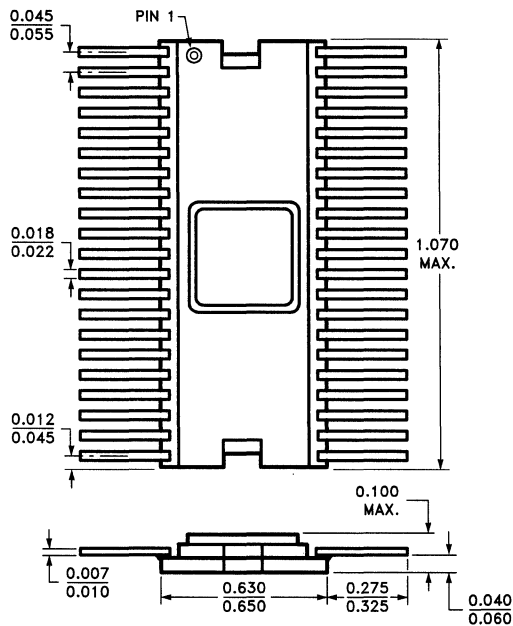


**24 Lead Rectangular Flatpack F73**

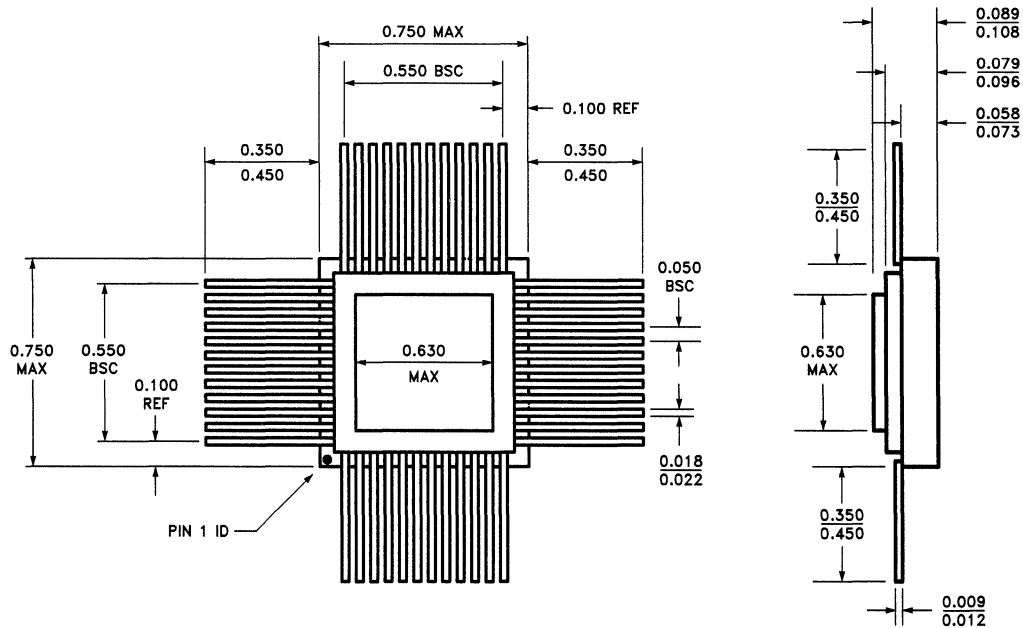
(MIL-M-38510 F-6 CONFIG 2)



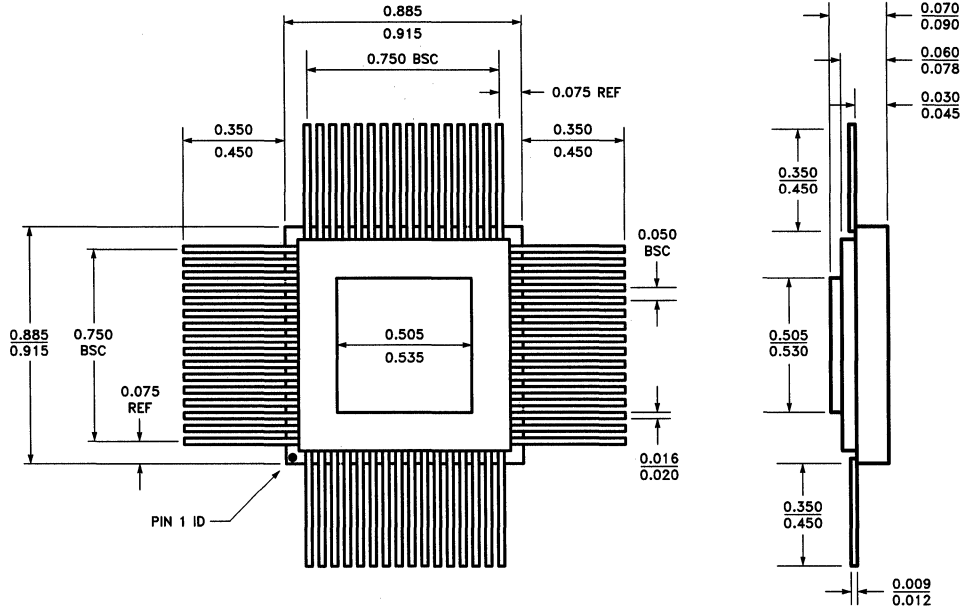
**42 Lead Rectangular Flatpack F76**



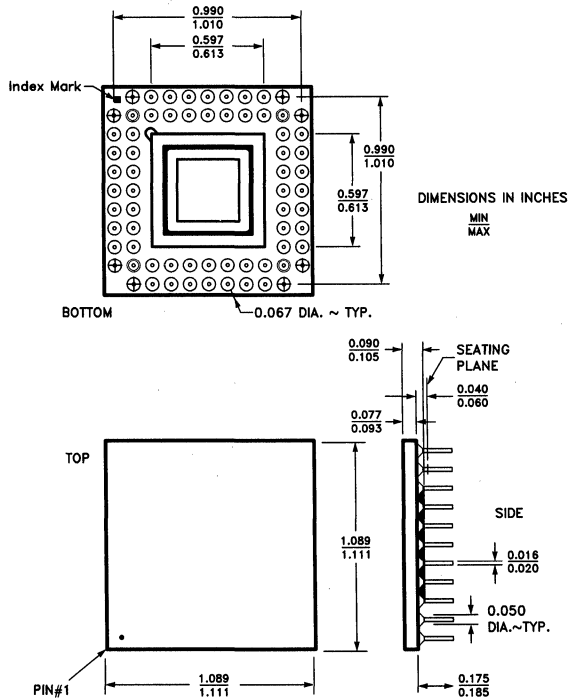
**48 Lead Quad Flatpack F78  
(Preliminary)**



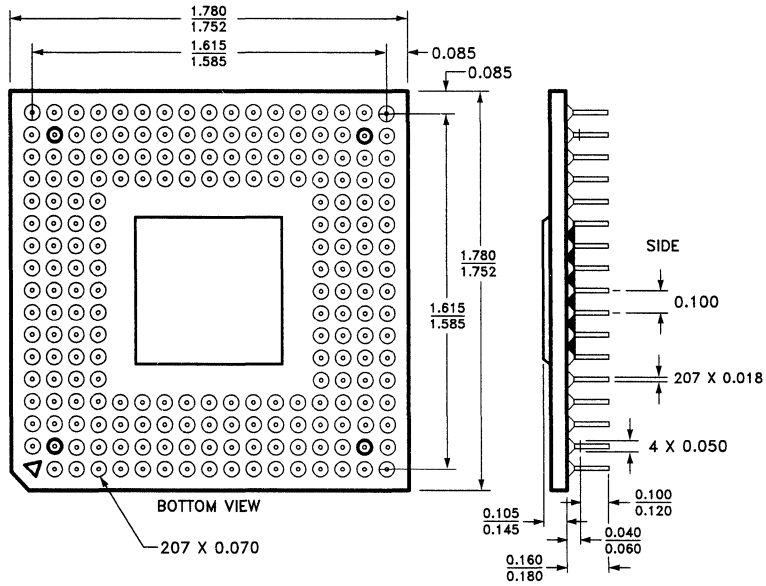
**64 Lead Quad Flatpack F90  
(Preliminary)**



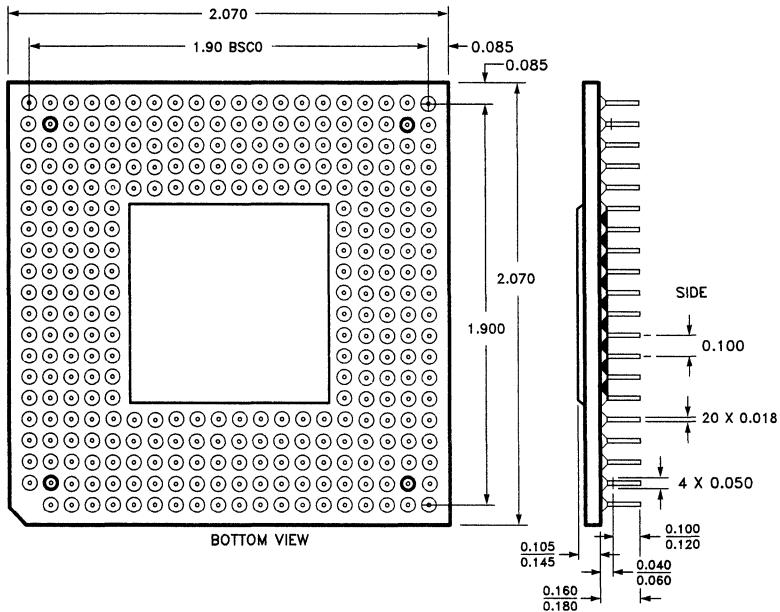
**68 Pin Grid Array Package G68**



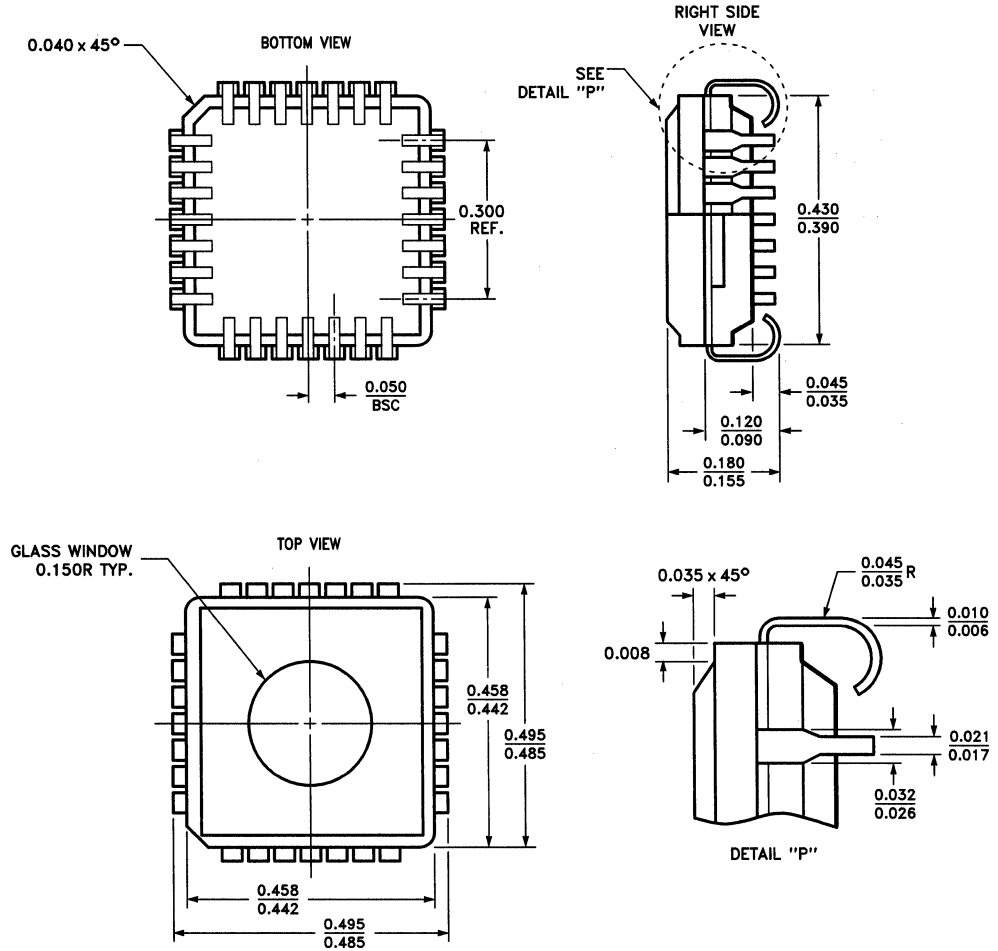
207 Pin Grid Array G207



299 Pin Grid Array G299  
(Preliminary)

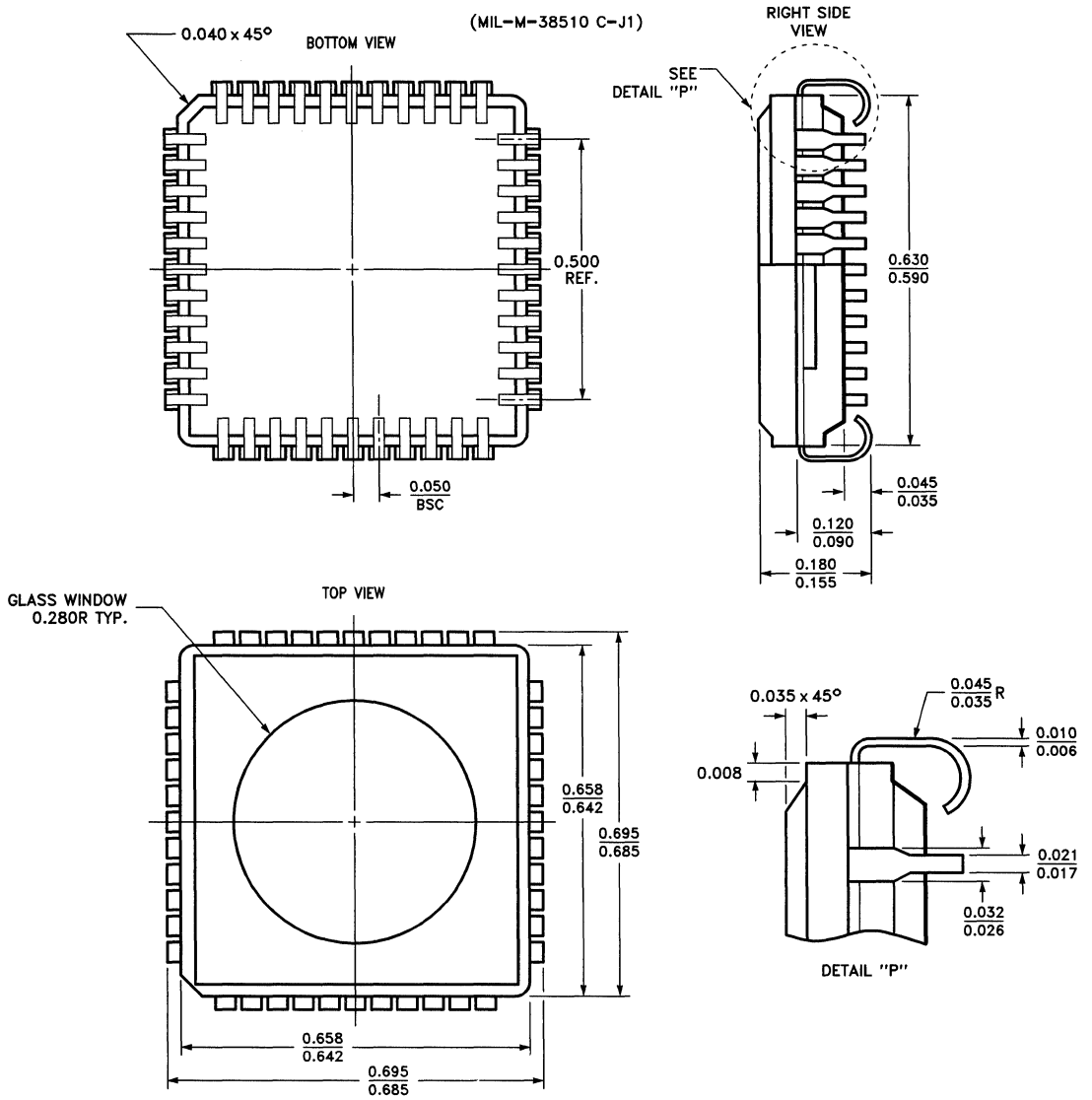


**28 Pin Windowed Leaded Chip Carrier H64**



44 Pin Windowed Leaded Chip Carrier H67

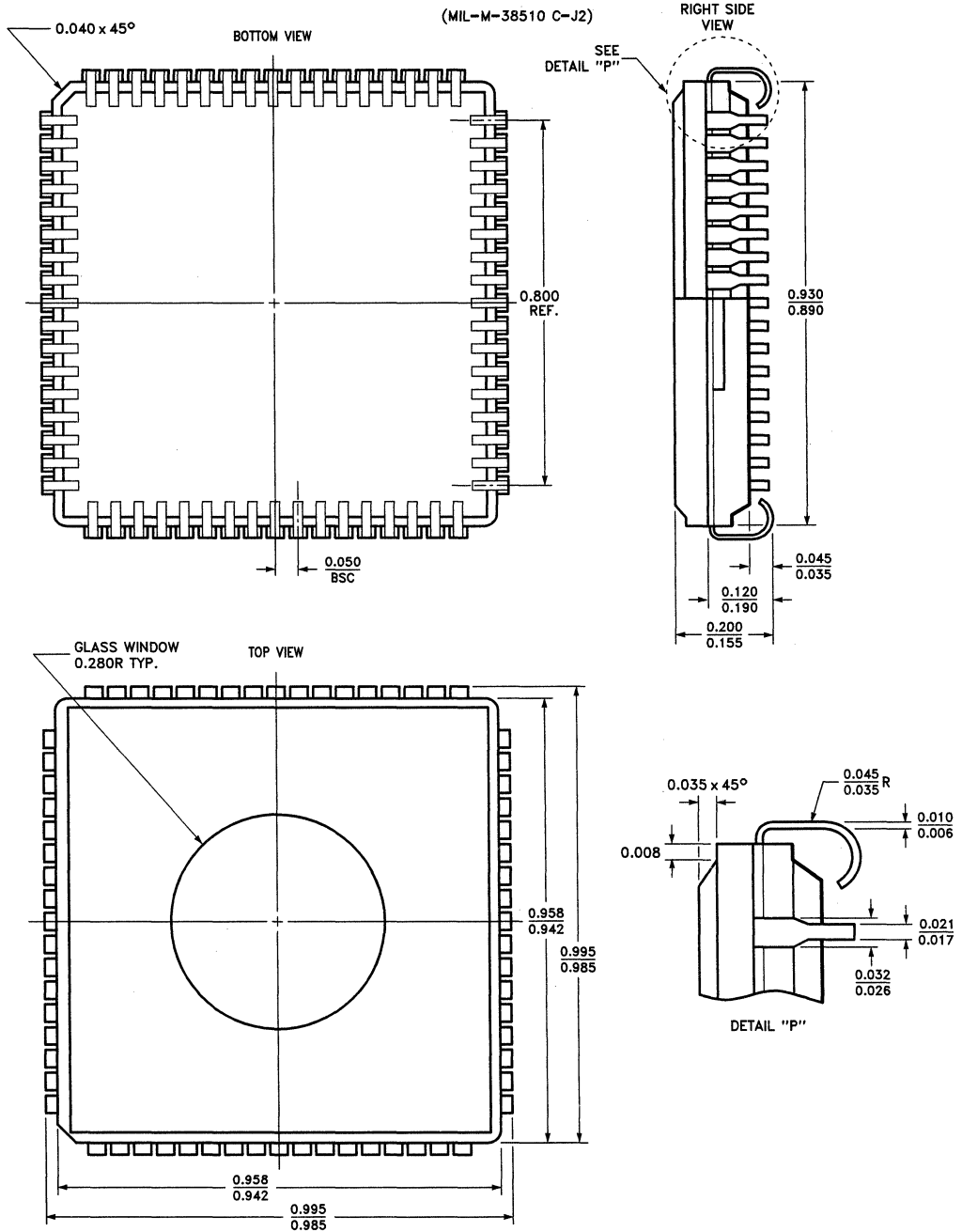
(MIL-M-38510 C-J1)



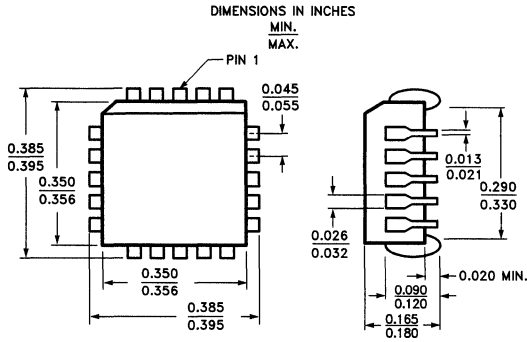


**68 Pin Windowed Leaded Chip Carrier H81**

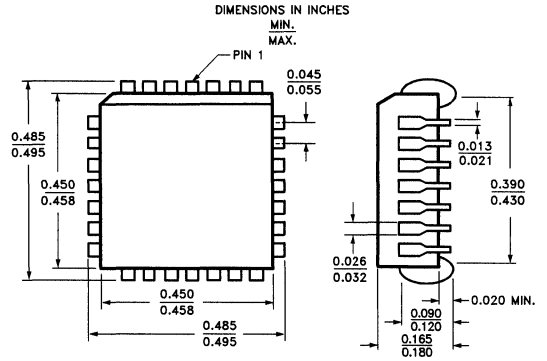
(MIL-M-38510 C-J2)



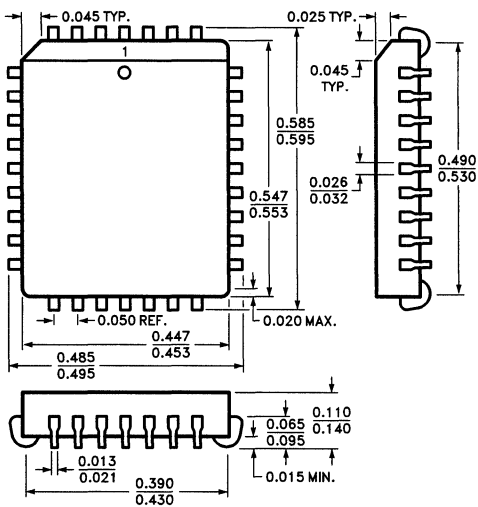
20 Lead Plastic Leadless Chip Carrier J61



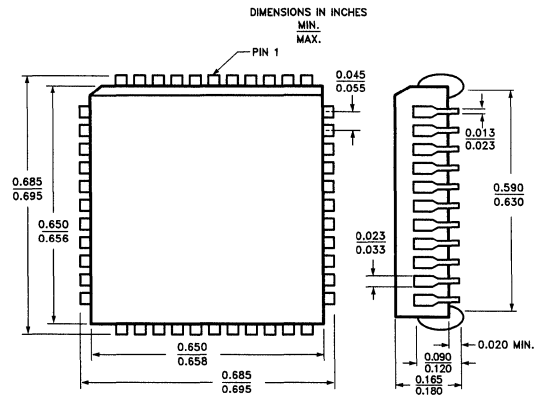
28 Lead Plastic Leadless Chip Carrier J64



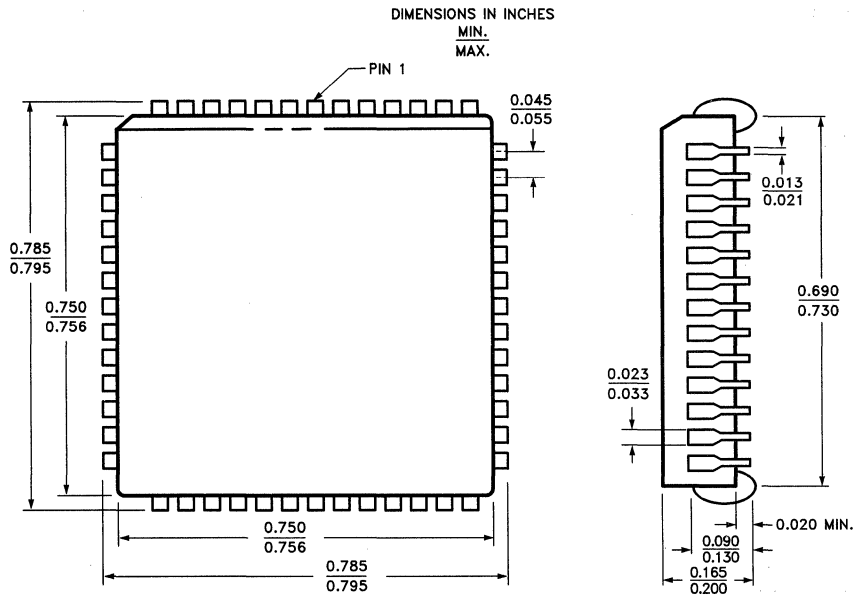
32 Lead Plastic Leadless Chip Carrier J65



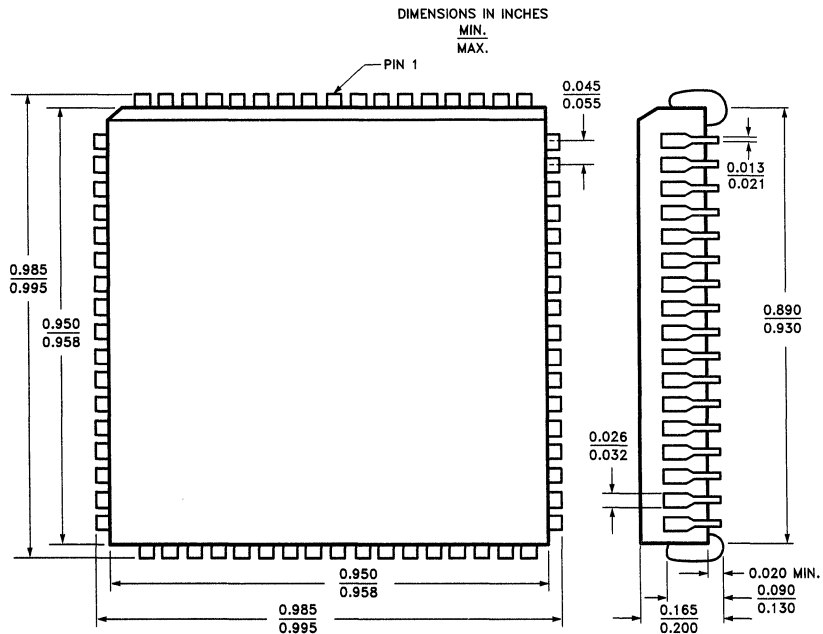
44 Lead Plastic Leadless Chip Carrier J67



52 Lead Plastic Leadless Chip Carrier J69

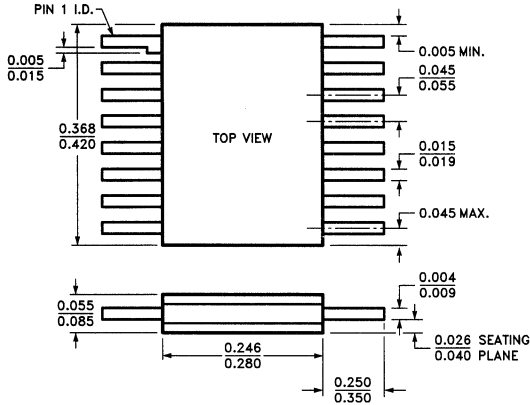


68 Lead Plastic Leadless Chip Carrier J81



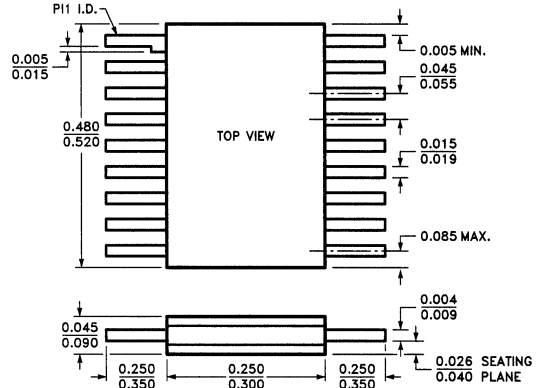
**16 Lead Rectangular Cerpack K69**

(MIL-M-38510 F-5 CONFIG 1)



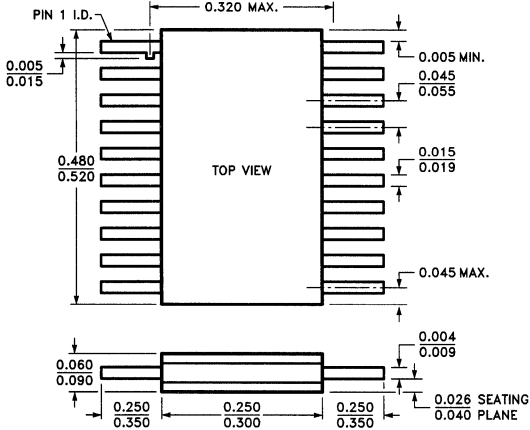
**18 Lead Rectangular Cerpack K70**

(MIL-M-38510 F-10 CONFIG 1)



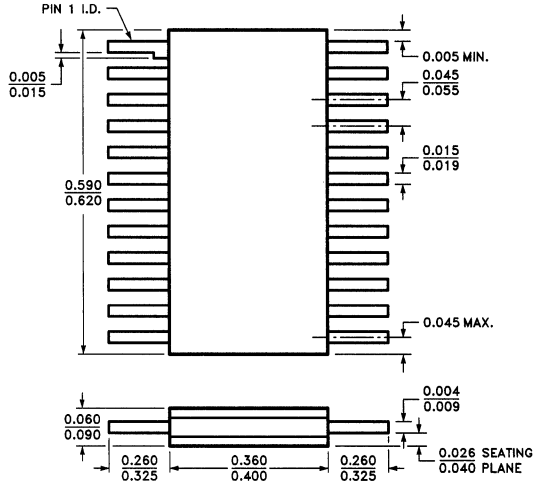
**20 Lead Rectangular Cerpack K71**

(MIL-M-38510 F-9 CONFIG 1)



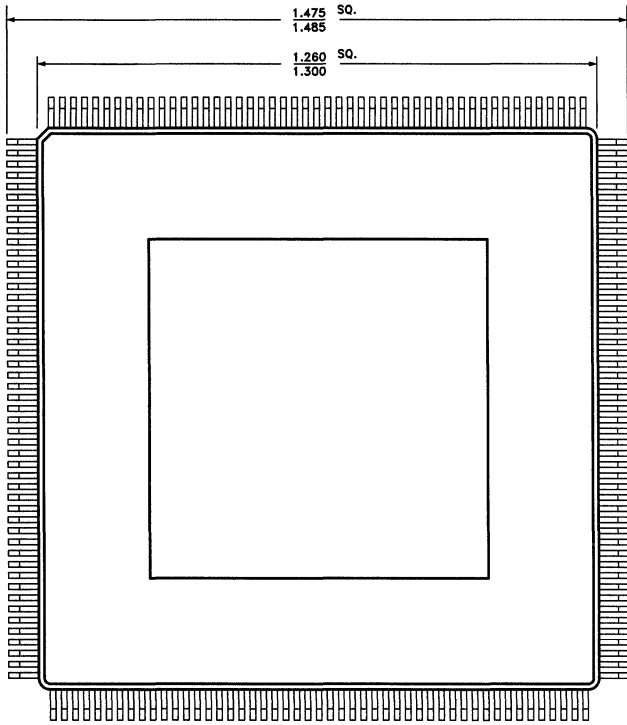
**24 Lead Rectangular Cerpack K73**

(MIL-M-38510 F-8 CONFIG 1)



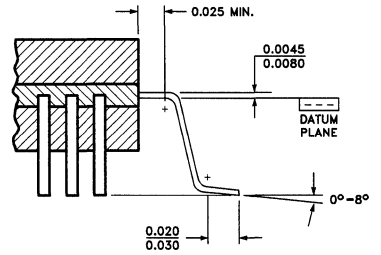


**196 Lead Quad Flatpack Package K196**

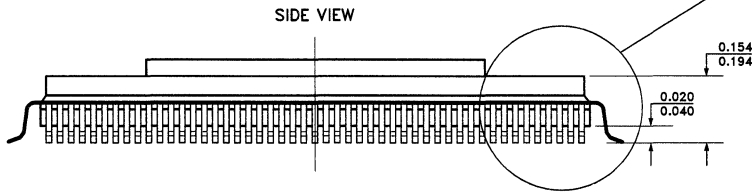


TOP VIEW

0.008  
0.013  
0.025



LEAD FORM DETAIL



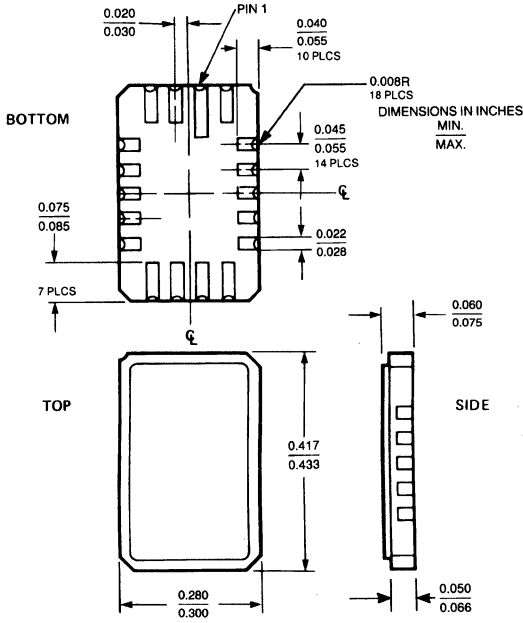
SIDE VIEW

0.154  
0.194

0.020  
0.040

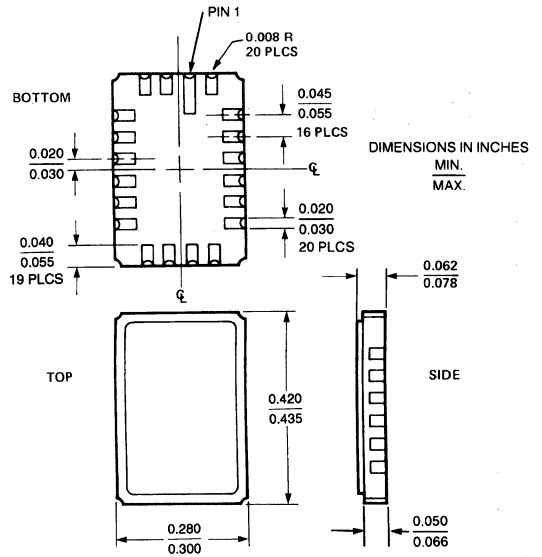
18 Pin Rectangular Leadless Chip Carrier L50

(MIL-M-38510 C-10A)

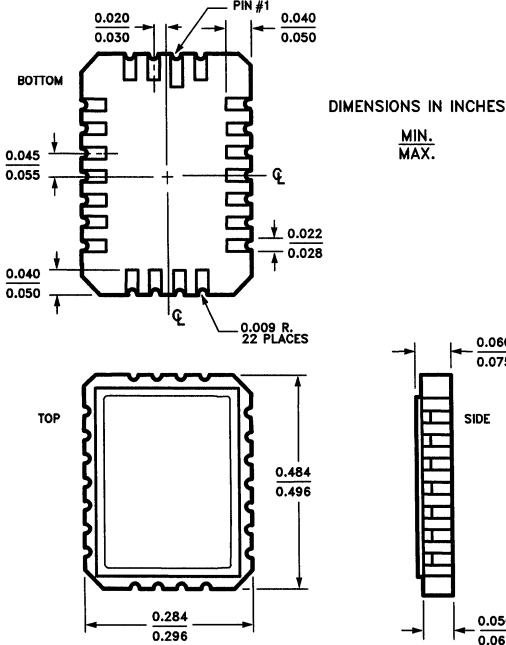


20 Pin Rectangular Leadless Chip Carrier L51

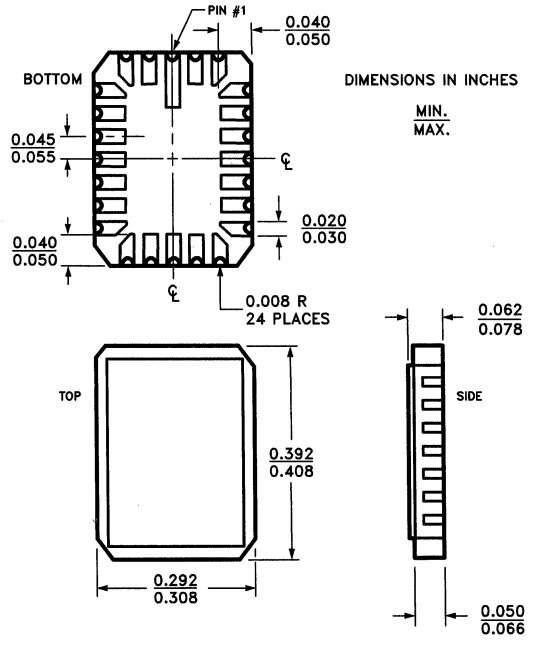
(MIL-M-38510 C-13)



22 Pin Rectangular Leadless Chip Carrier L52

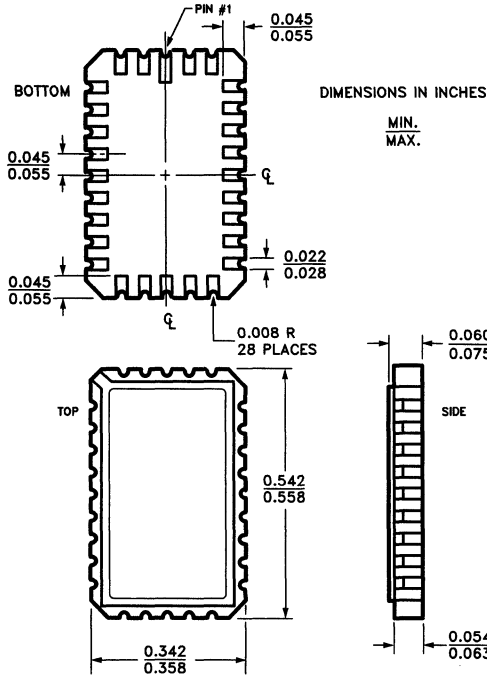


24 Pin Rectangular Leadless Chip Carrier L53



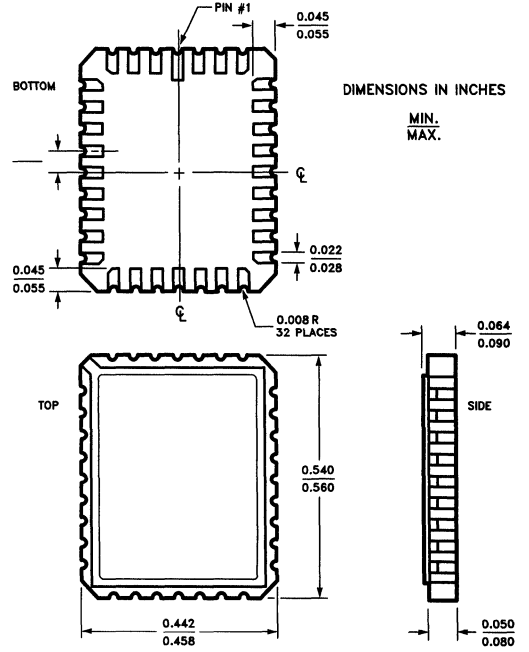
**28 Pin Rectangular Leadless Chip Carrier L54**

(MIL-M-38510 C-11A)



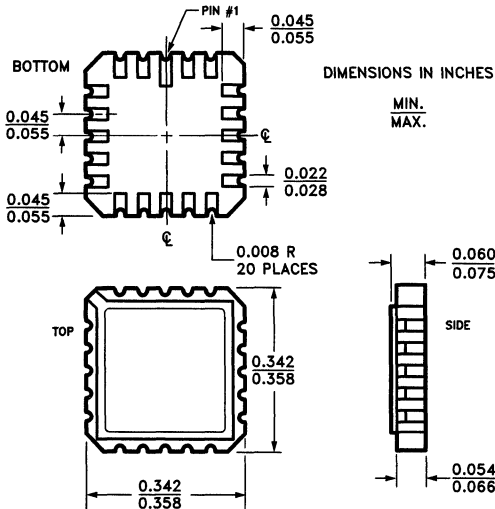
**32 Pin Rectangular Leadless Chip Carrier L55**

(MIL-M-38510 C-12)

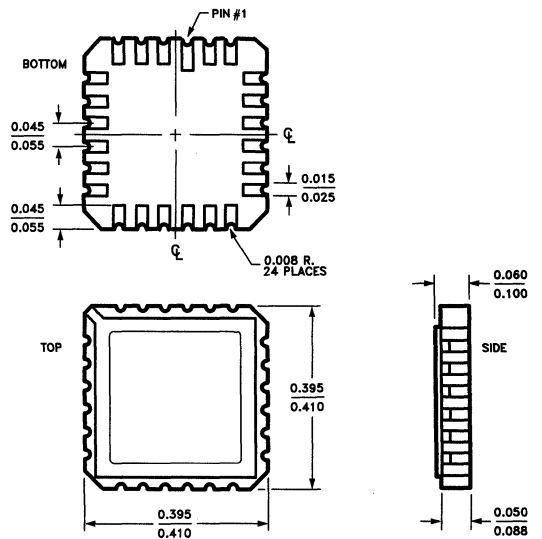


**20 Pin Square Leadless Chip Carrier L61**

(MIL-M-38510 C-2A)



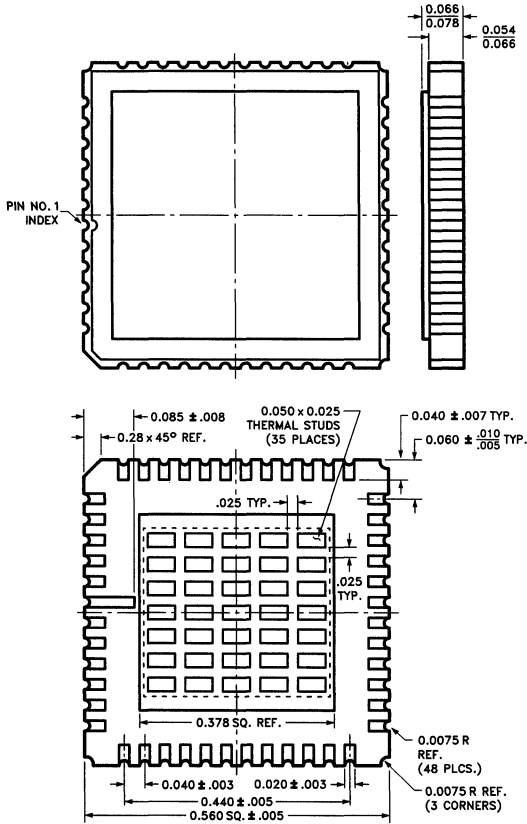
**24 Pin Square Leadless Chip Carrier L63**



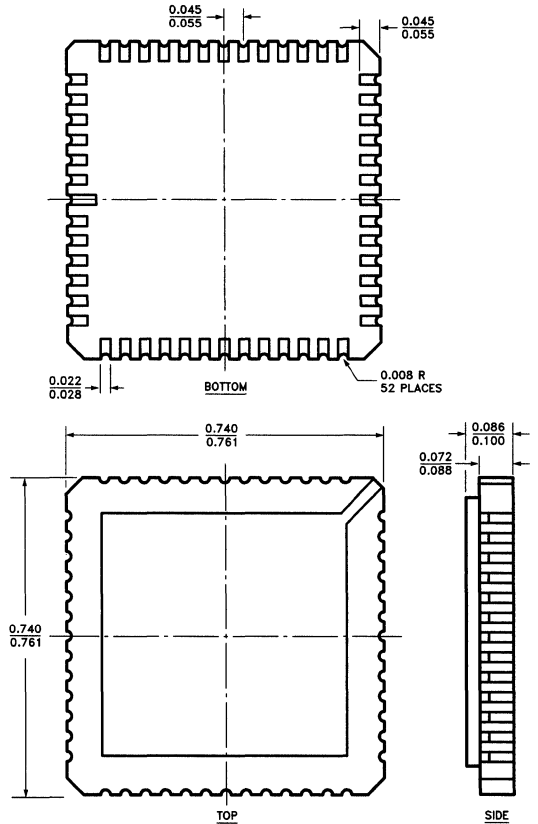




**48 Pin Square Leadless Chip Carrier L68**

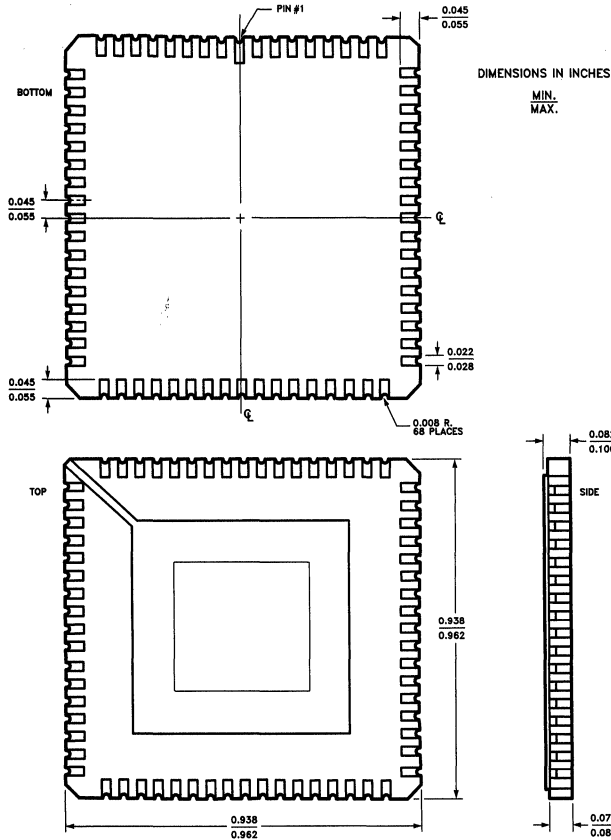


**52 Pin Square Leadless Chip Carrier L69**

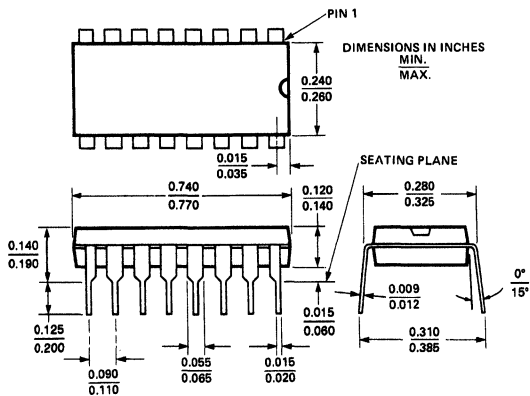


**68 Pin Square Leadless Chip Carrier L81**

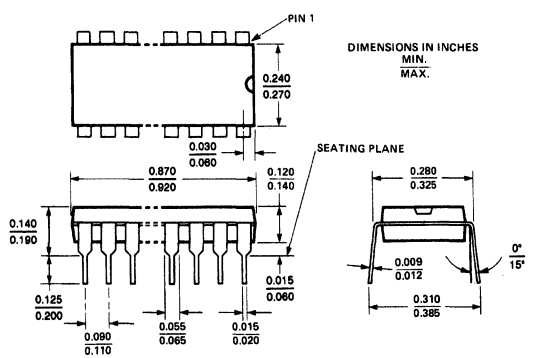
(MIL-M-38510 C-7)



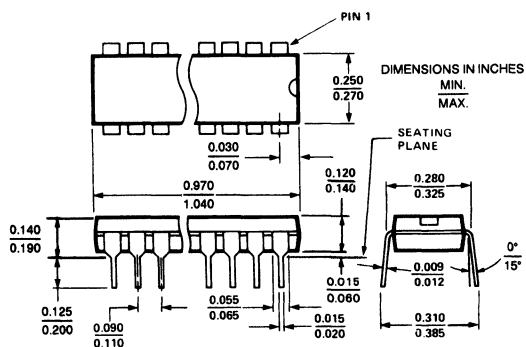
**16 Lead (300 MIL) Molded DIP P1**



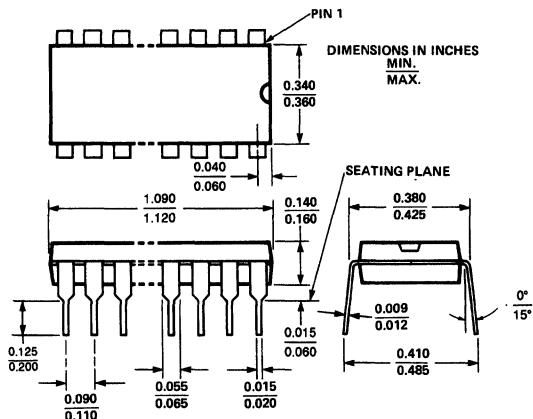
**18 Lead (300 MIL) Molded DIP P3**



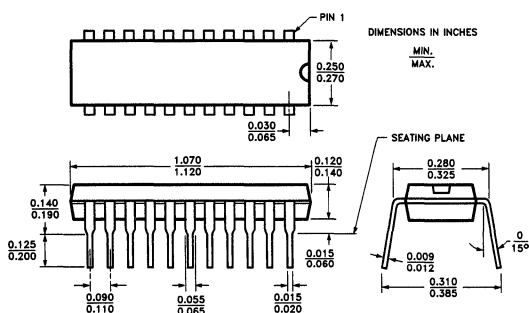
### 20 Lead (300 MIL) Molded DIP P5



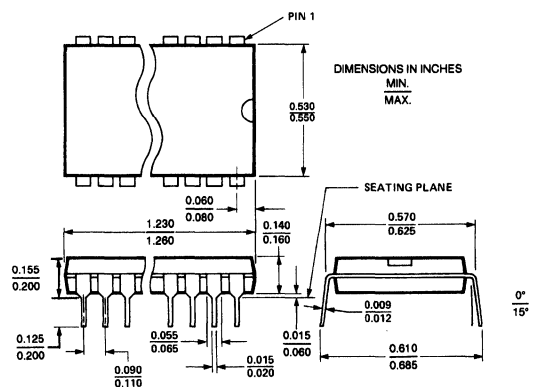
### 22 Lead (400 MIL) Molded DIP P7



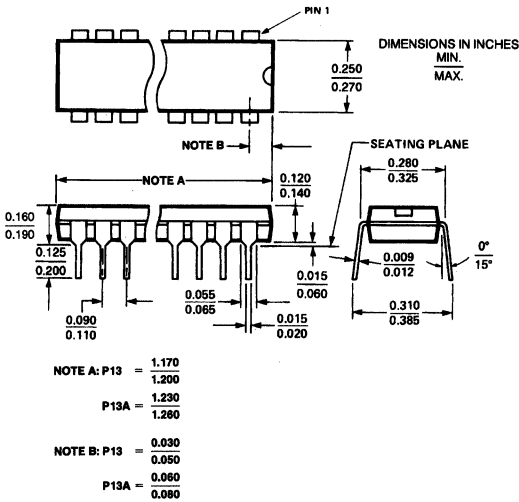
### 22 Lead (300 MIL) Molded DIP P9



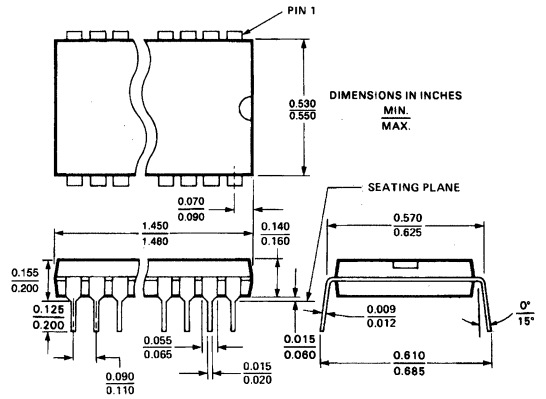
### 24 Lead (600 MIL) Molded DIP P11



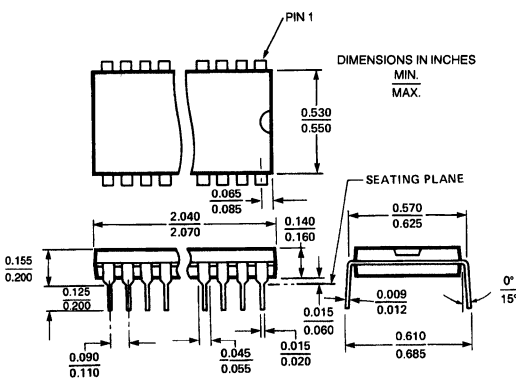
24 Lead (300 MIL) Molded DIP P13/P13A



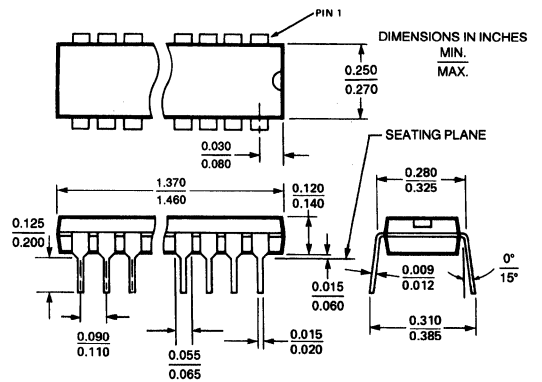
28 Lead (600 MIL) Molded DIP P15



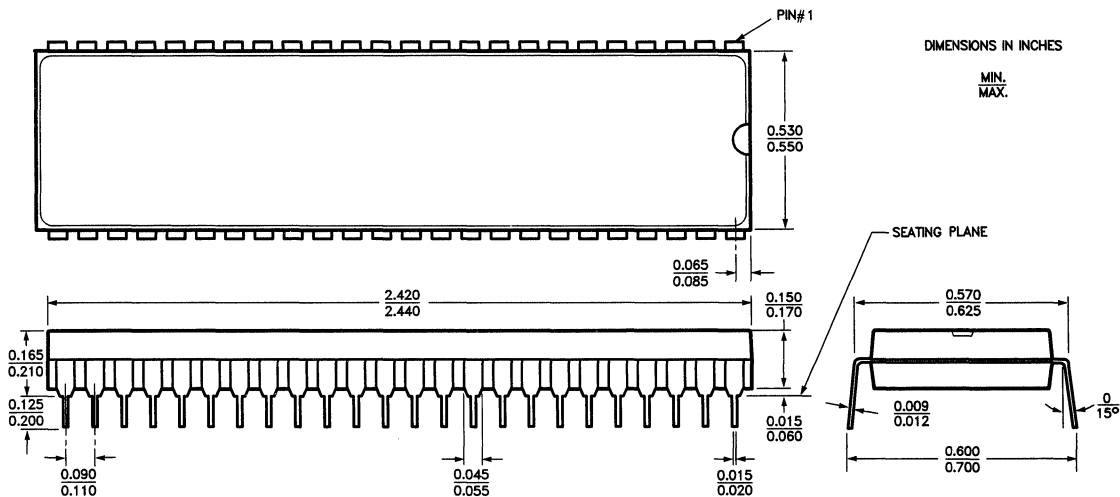
40 Lead (600 MIL) Molded DIP P17



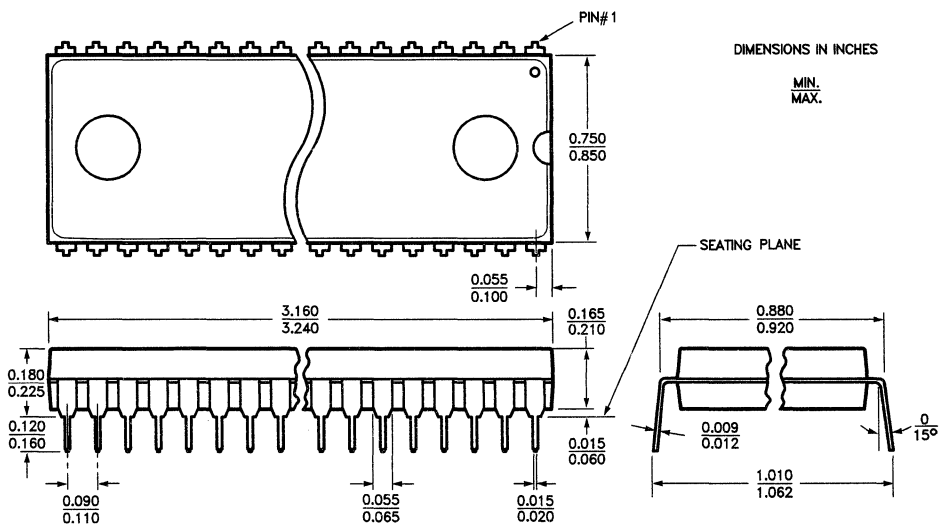
28 Lead (300 MIL) Molded DIP P21



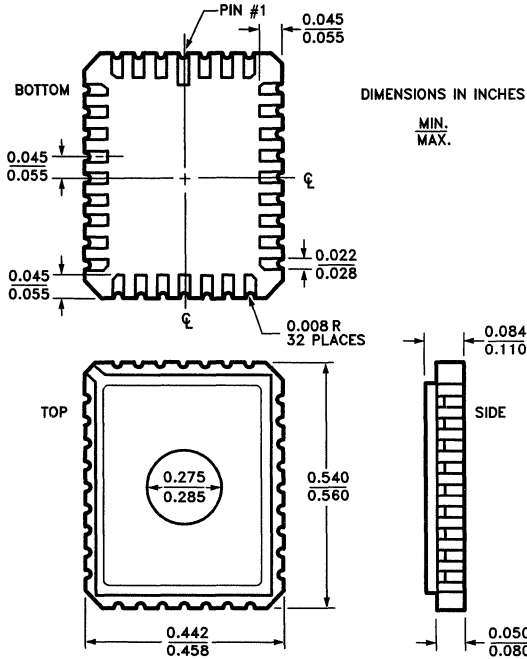
48 Lead (600 MIL) Molded DIP P25



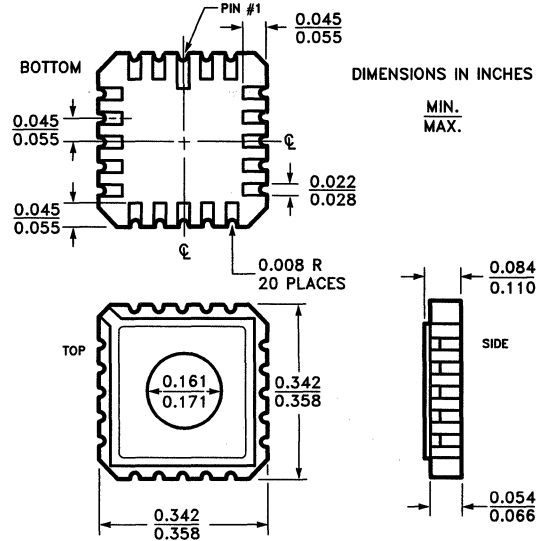
64 Lead (900 MIL) Molded DIP P29



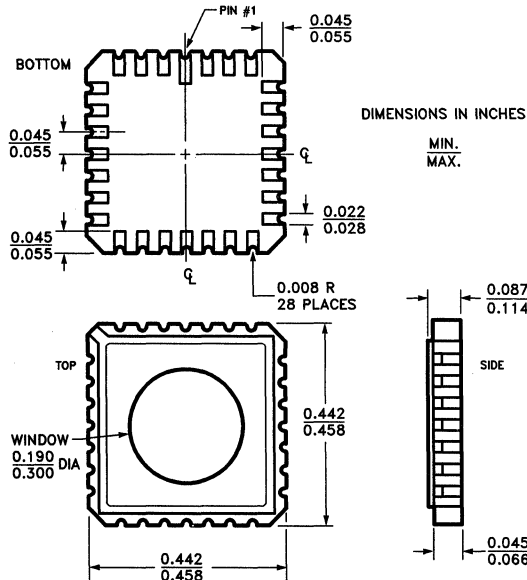
32 Pin Windowed Rectangular Leadless Chip Carrier Q55



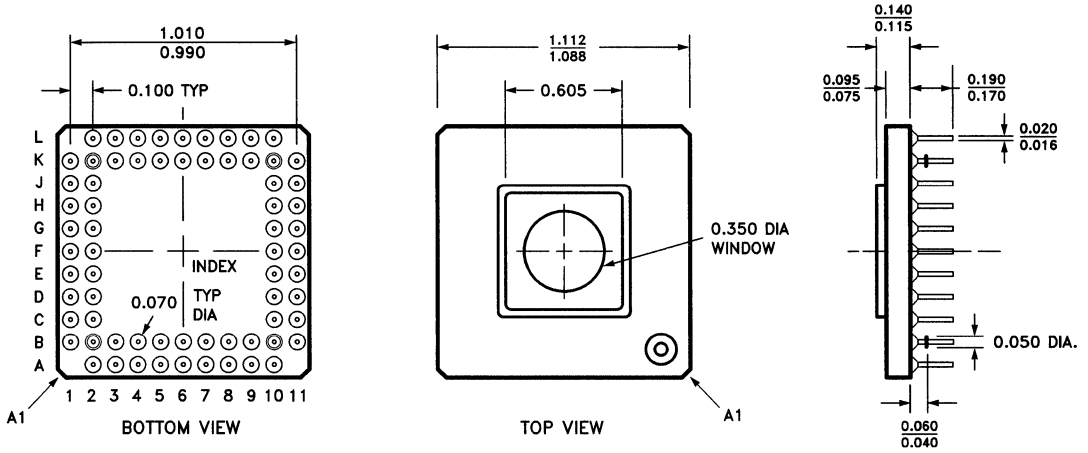
20 Pin Windowed Square Leadless Chip Carrier Q61



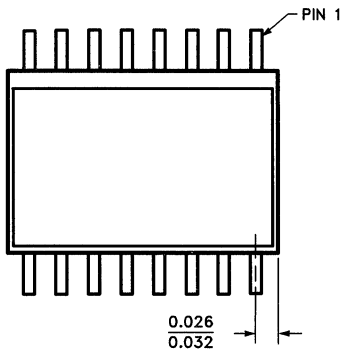
28 Pin Windowed Leadless Chip Carrier Q64



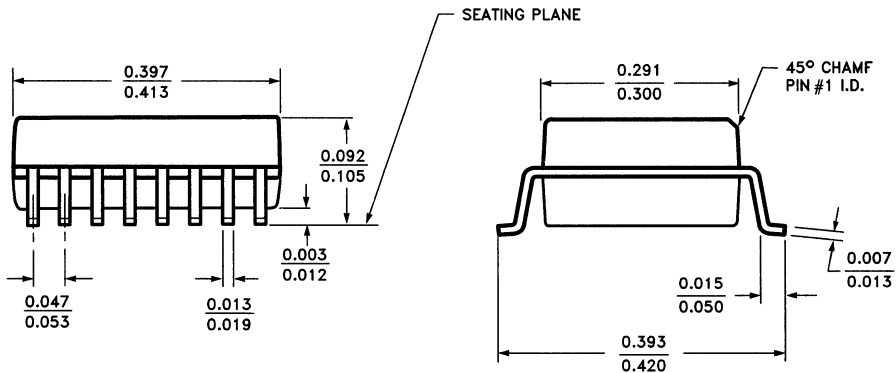
68 Pin Windowed PGA Ceramic R68



16 Lead Molded SOIC S1

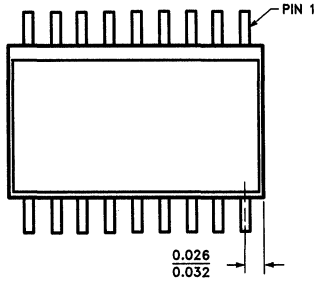


DIMENSIONS IN INCHES  
MIN.  
MAX.  
LEAD COPLANIARITY 0.004 MAX.





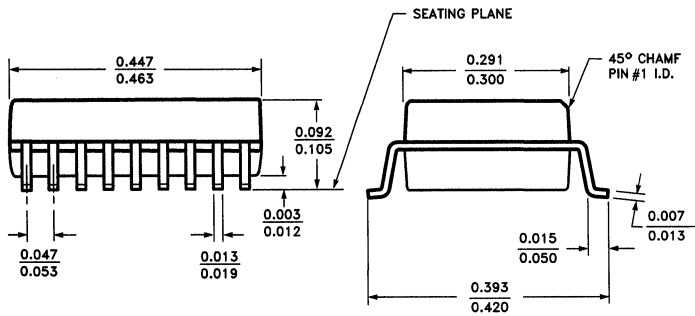
18 Lead Molded SOIC S3



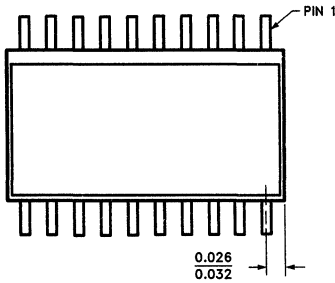
DIMENSIONS IN INCHES

MIN.  
MAX.

LEAD COPLANIARITY 0.004 MAX.



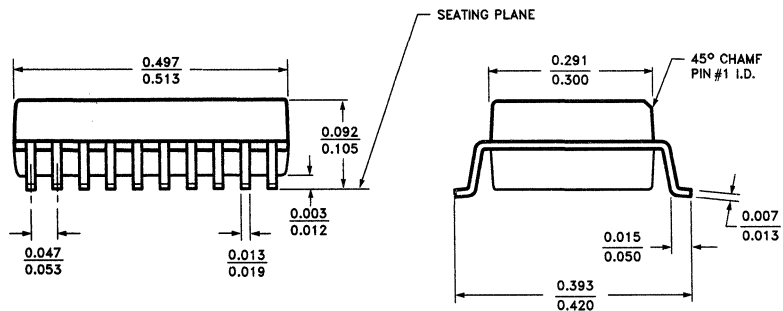
20 Lead Molded SOIC S5



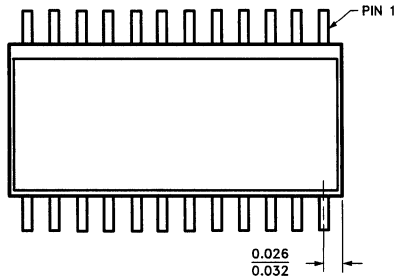
DIMENSIONS IN INCHES

MIN.  
MAX.

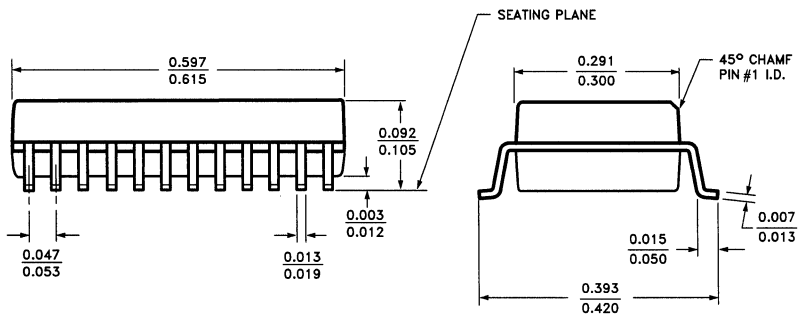
LEAD COPLANIARITY 0.004 MAX.



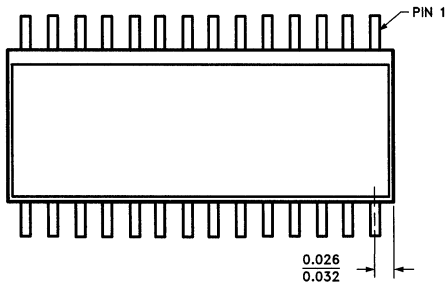
**24 Lead Molded SOIC S13**



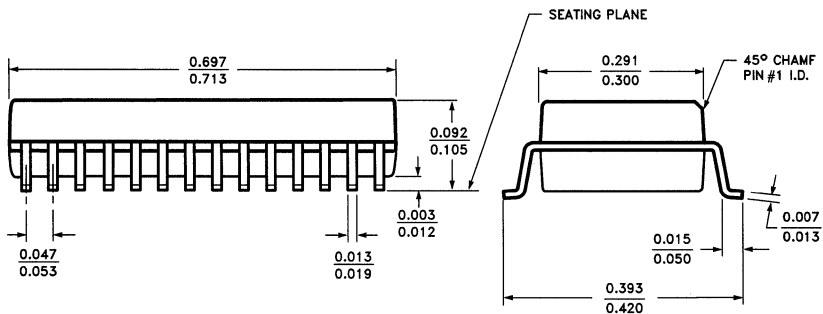
DIMENSIONS IN INCHES  
MIN.  
MAX.  
LEAD COPLANARITY 0.004 MAX.



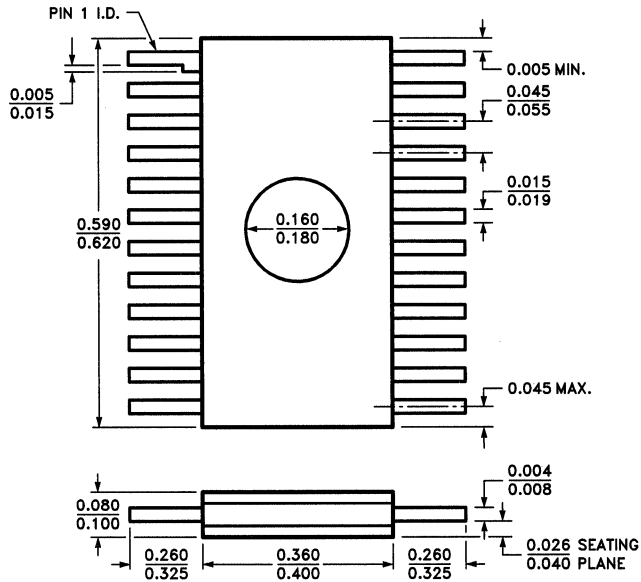
**28 Lead Molded SOIC S21**



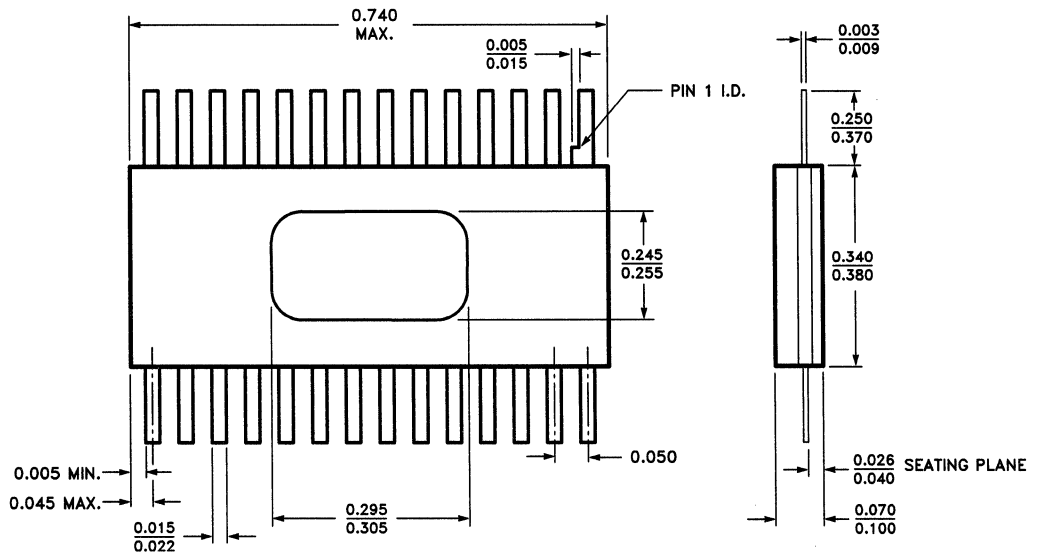
DIMENSIONS IN INCHES  
MIN.  
MAX.  
LEAD COPLANARITY 0.004 MAX.



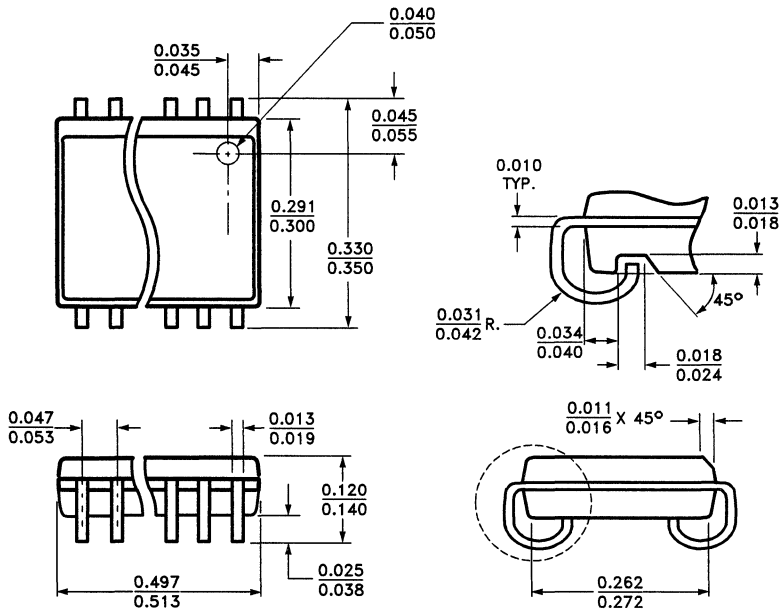
24 Lead Windowed Cerpack T73



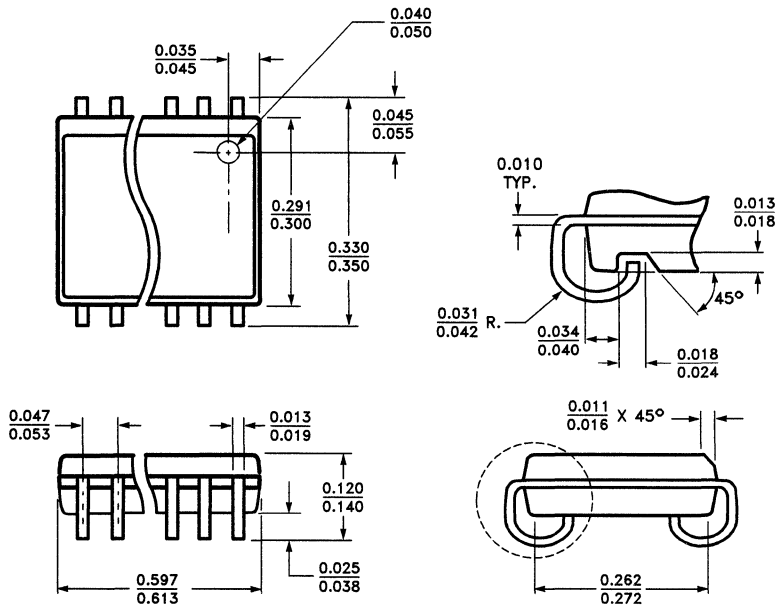
28 Lead Windowed Cerpack T74



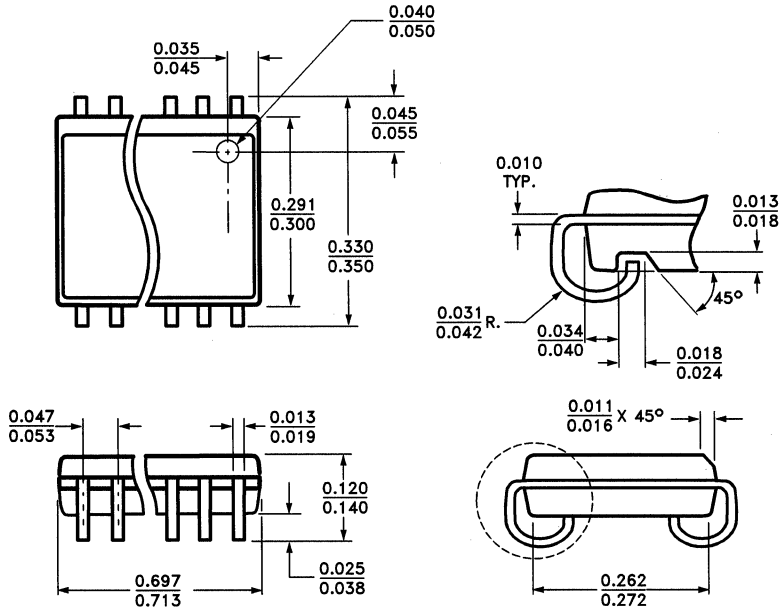
20 Lead Molded SOJ V5



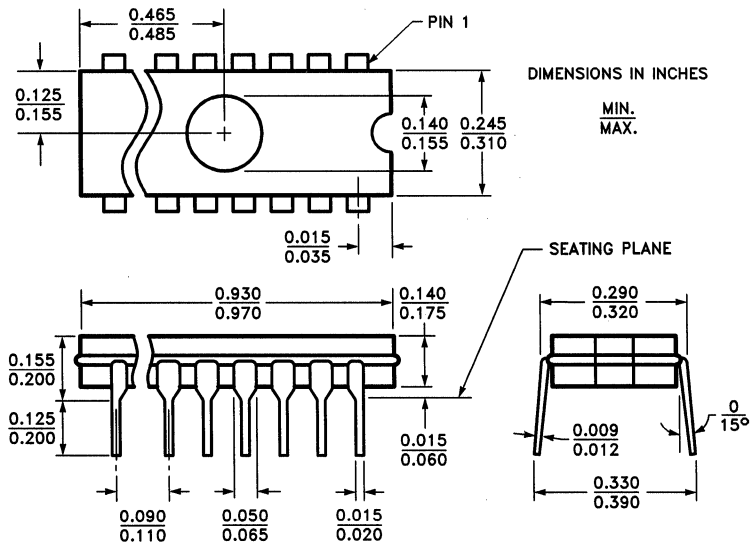
24 Lead Molded SOJ V13



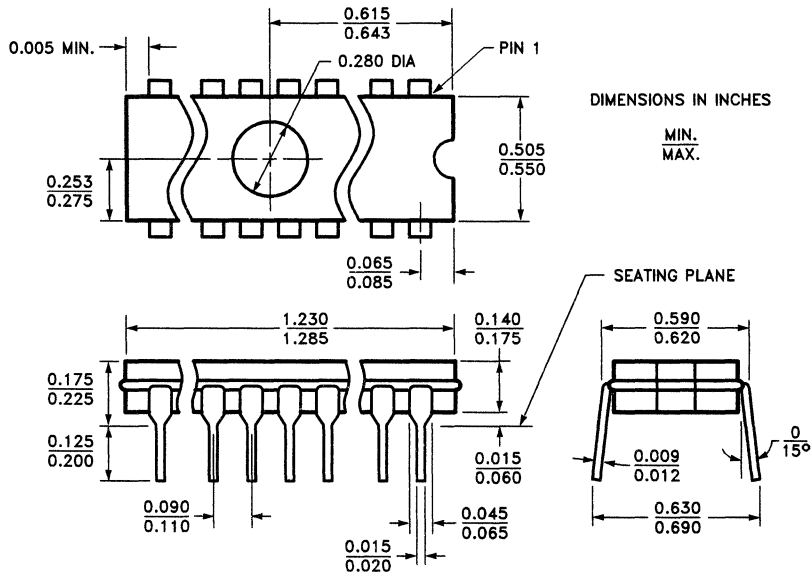
28 Lead Molded SOJ V21



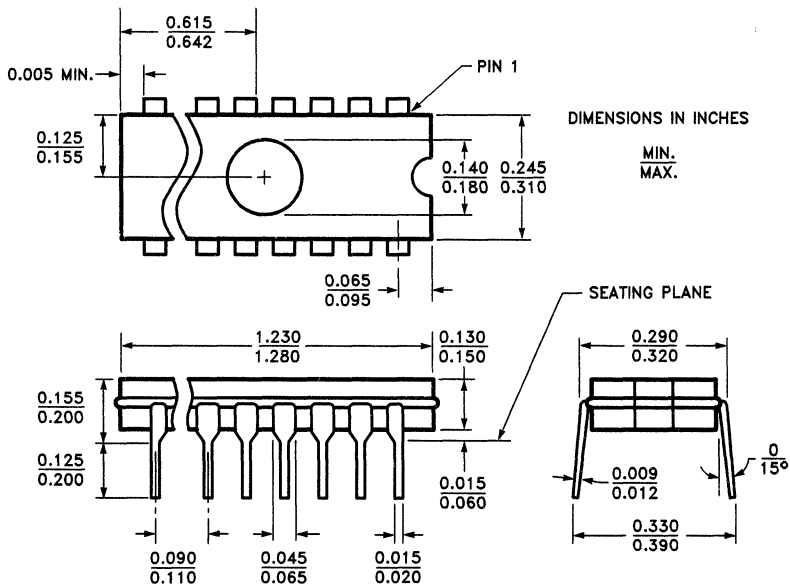
20 Lead (300 MIL) Windowed Cerdip W6



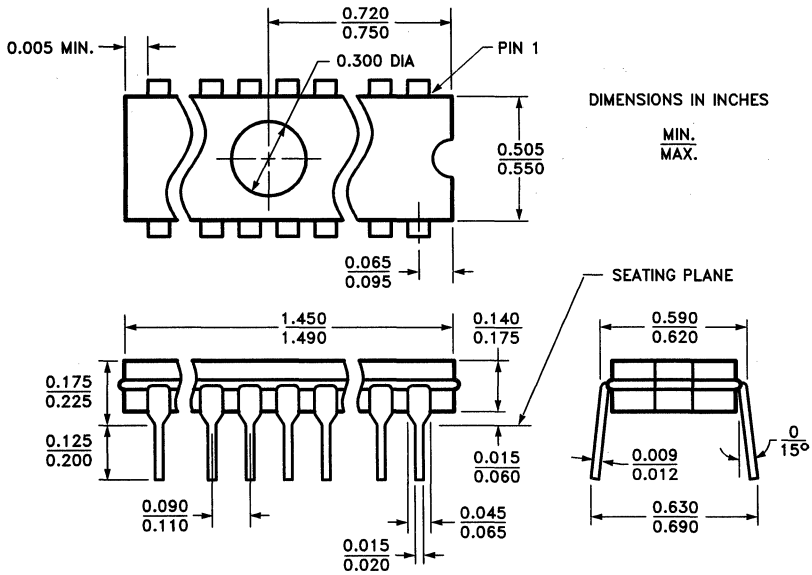
24 Lead (600 MIL) Windowed Cerdip W12



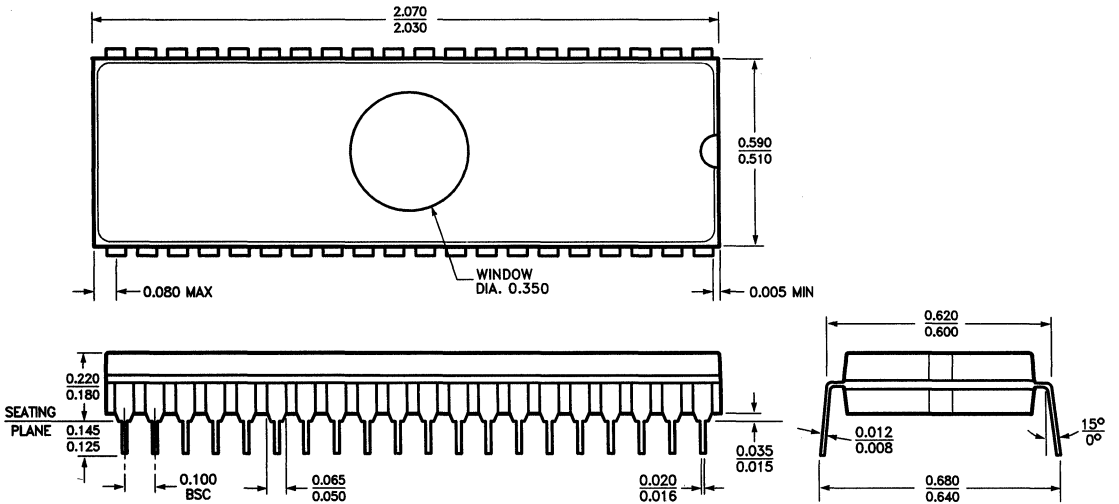
24 Lead (300 MIL) Windowed Cerdip W14



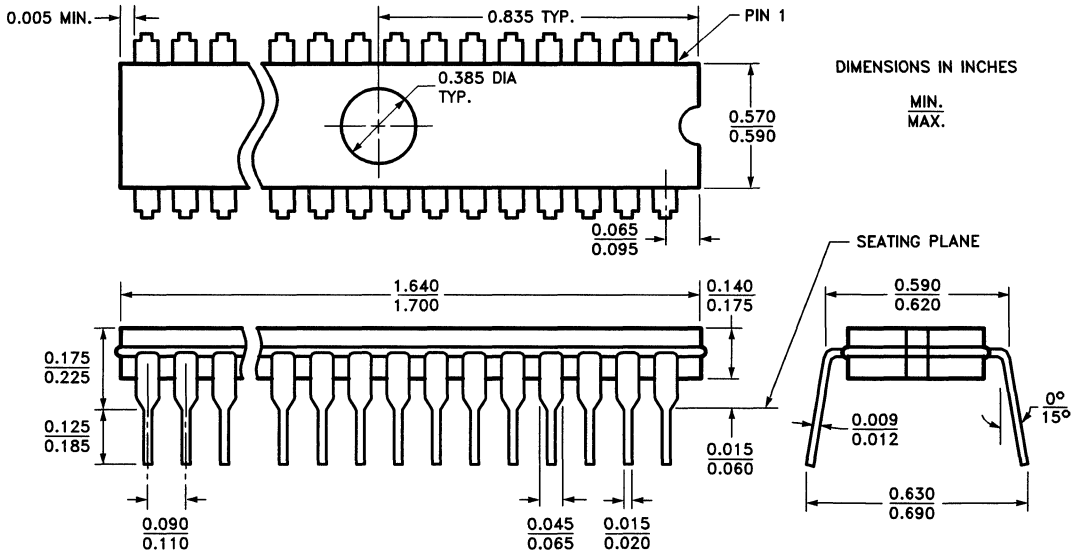
**28 Lead (600 MIL) Windowed Cerdip W16**



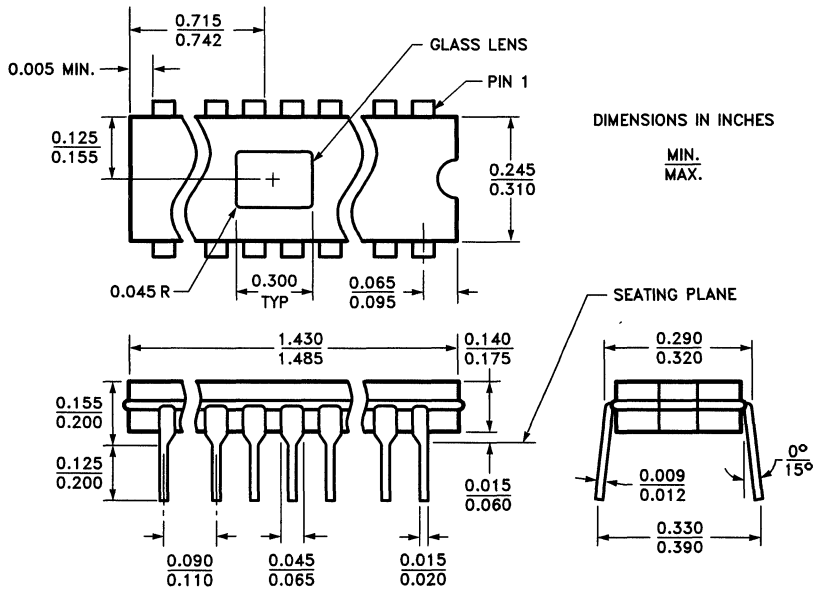
**40 Lead (600 MIL) Windowed Cerdip W18**



32 Lead (600 MIL) Windowed Cerdip W20

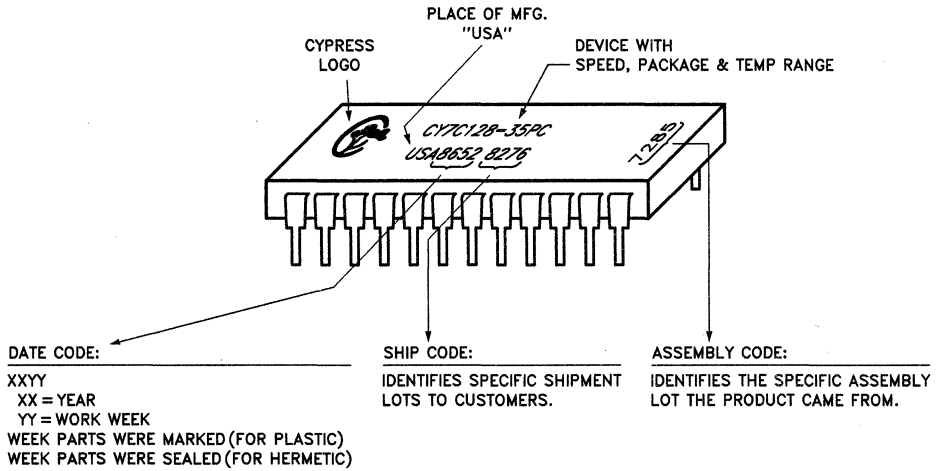


28 Lead (300 MIL) Windowed Cerdip W22





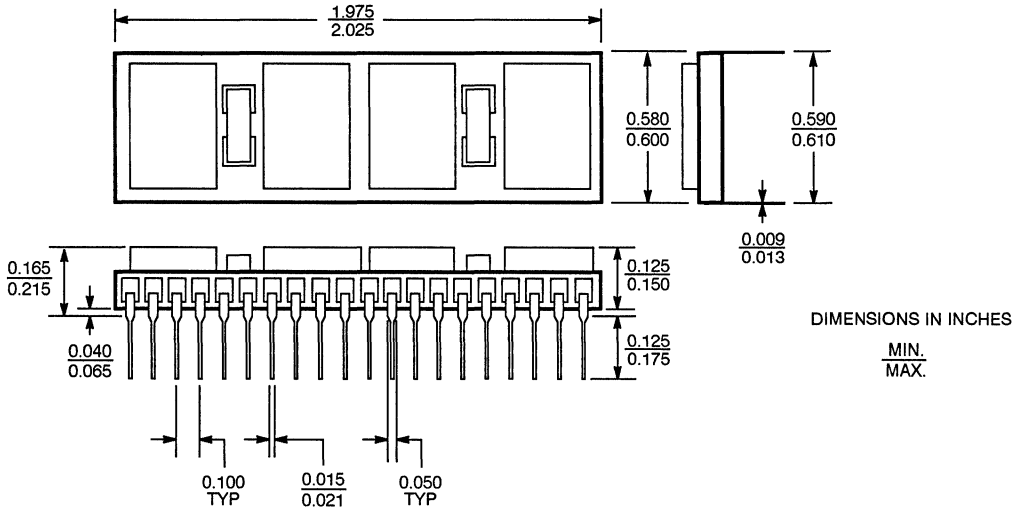
Typical Marking for DIP Packages (P and D Type)



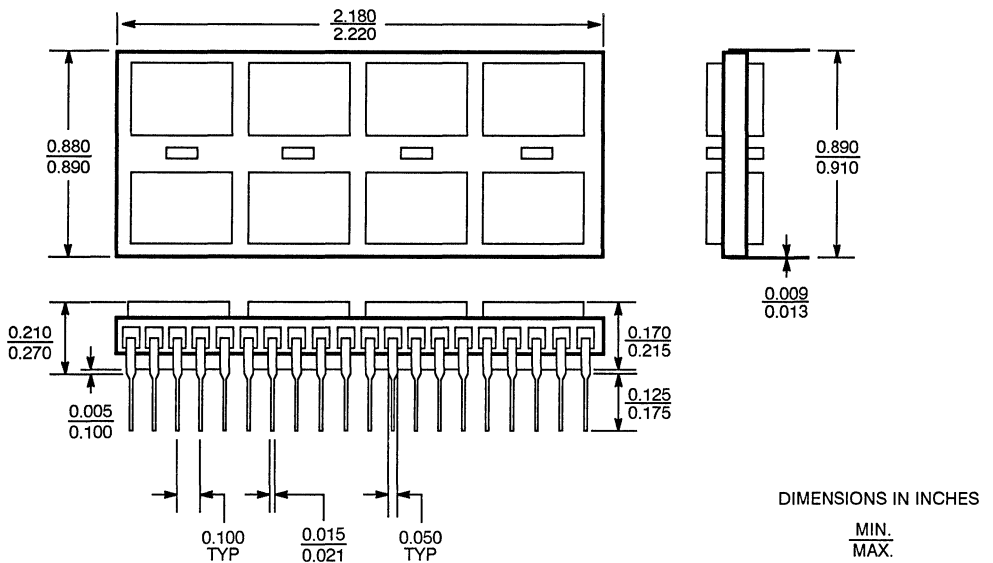
0047-1

## Package Diagrams for Modules

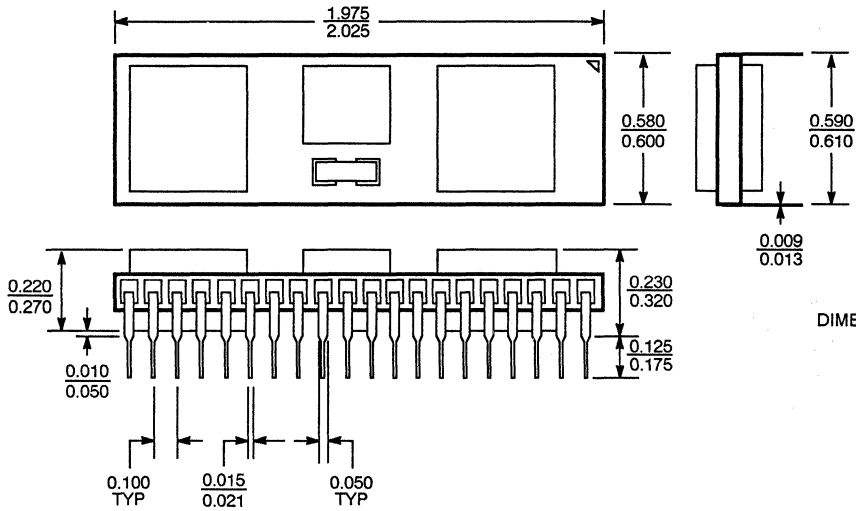
40 Pin DIP Module HD01



40 Pin Ceramic DIP Module HD02

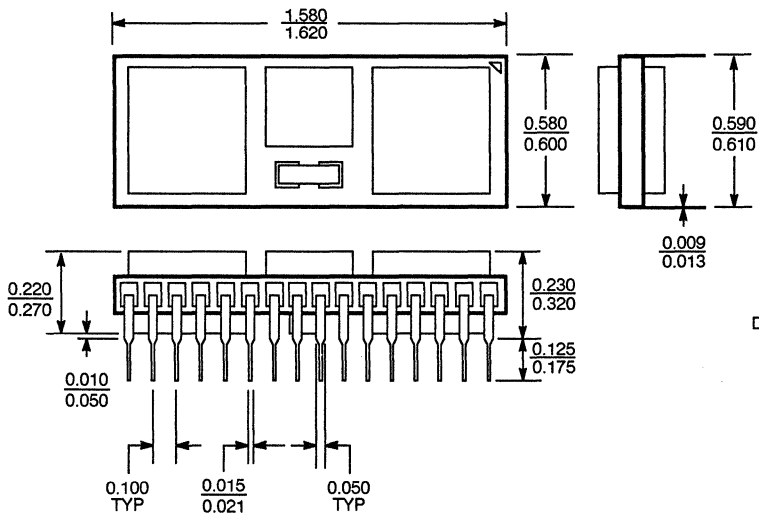


40 Pin DIP Module HD03



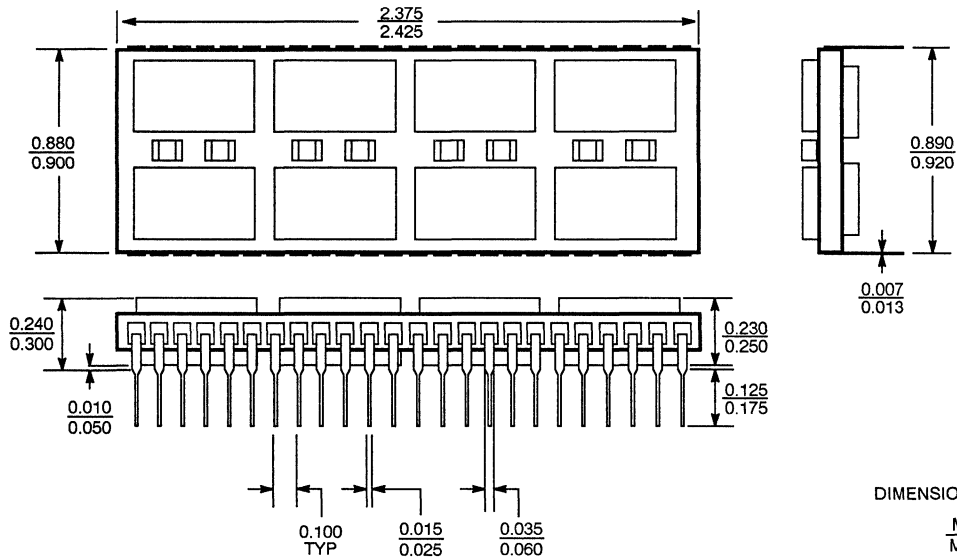
DIMENSIONS IN INCHES  
MIN.  
MAX.

32 Pin DIP Module HD04

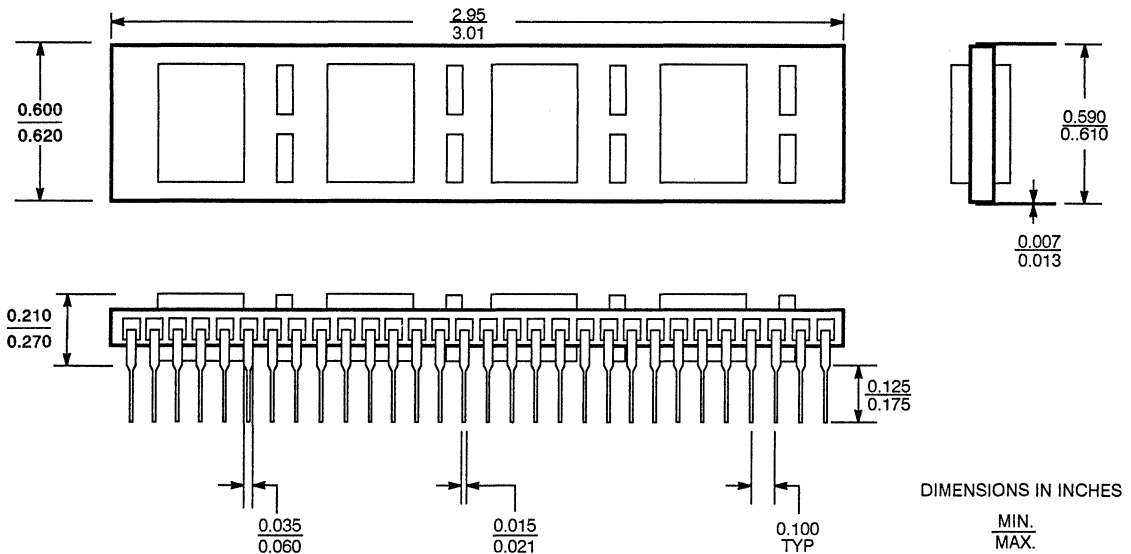


DIMENSIONS IN INCHES  
MIN.  
MAX.

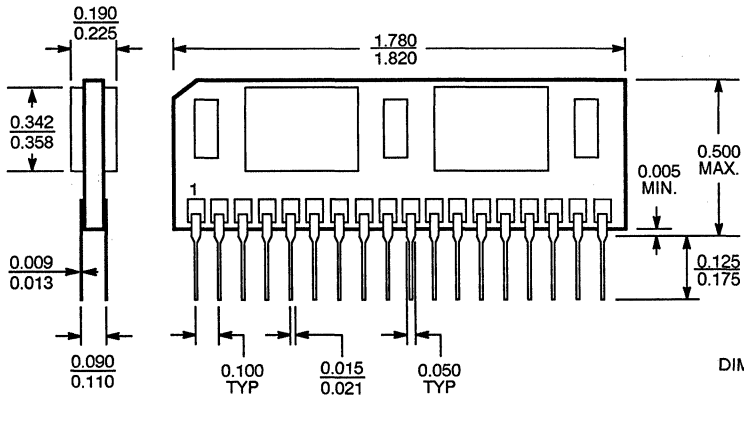
48 Pin Ceramic DIP Module HD05



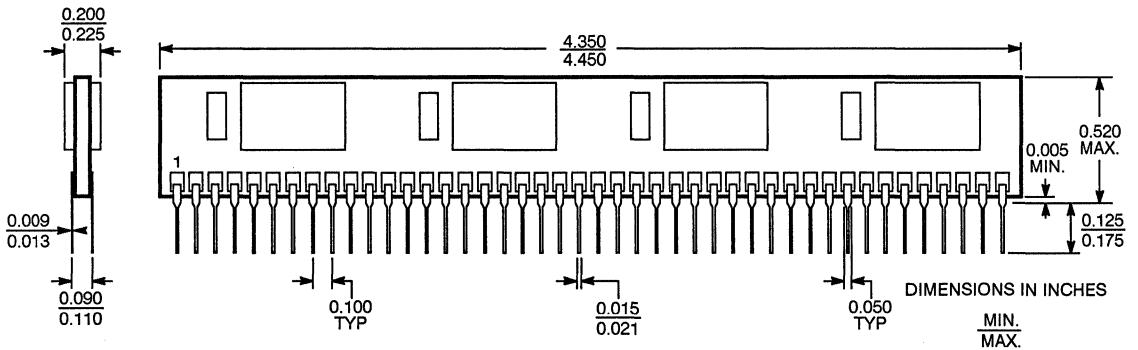
60 Pin Ceramic DIP Module HD06



36 Pin Vertical DIP Module HV01

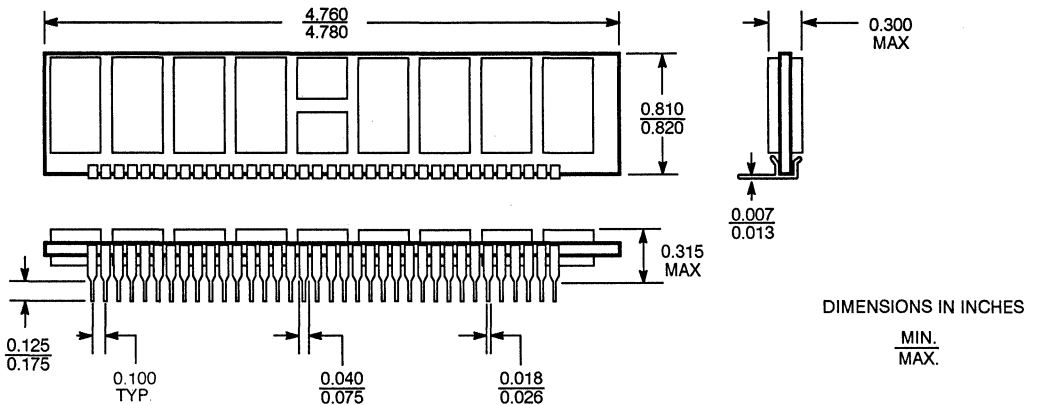


88 Pin Vertical DIP Module HV02

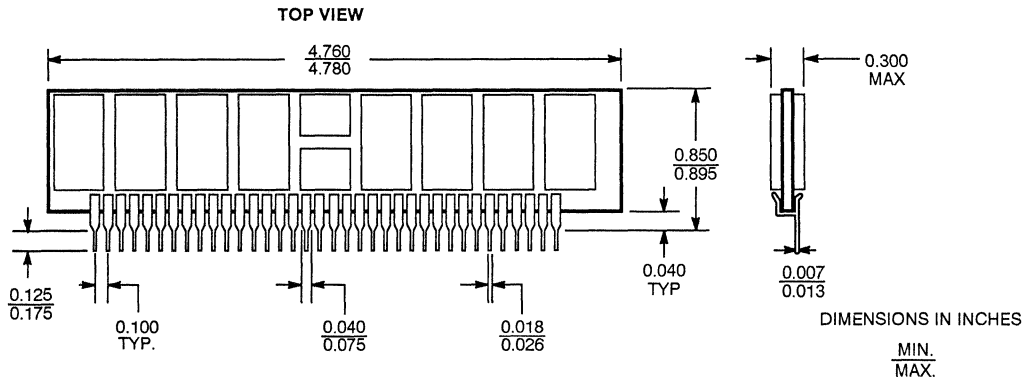


36 Pin Flat SIP Module PF01

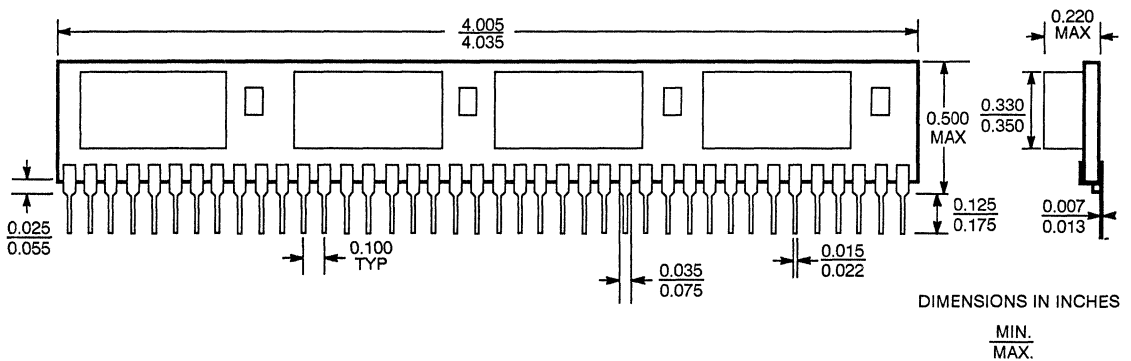
TOP VIEW



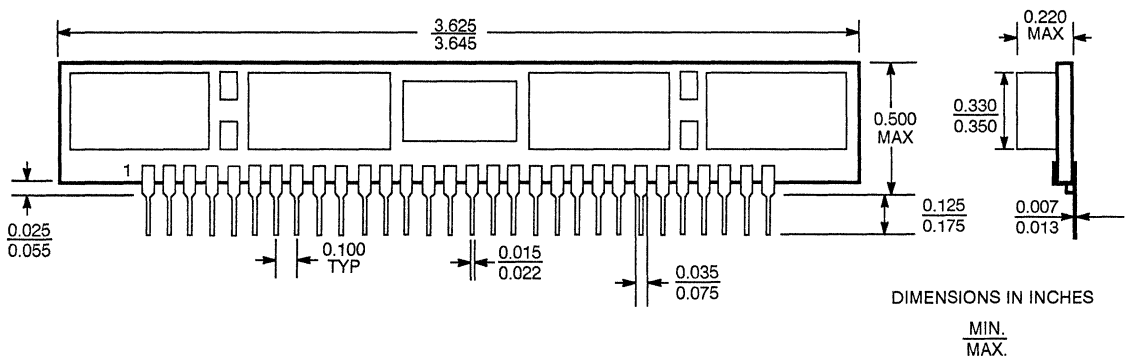
36 Pin SIP Module PS01



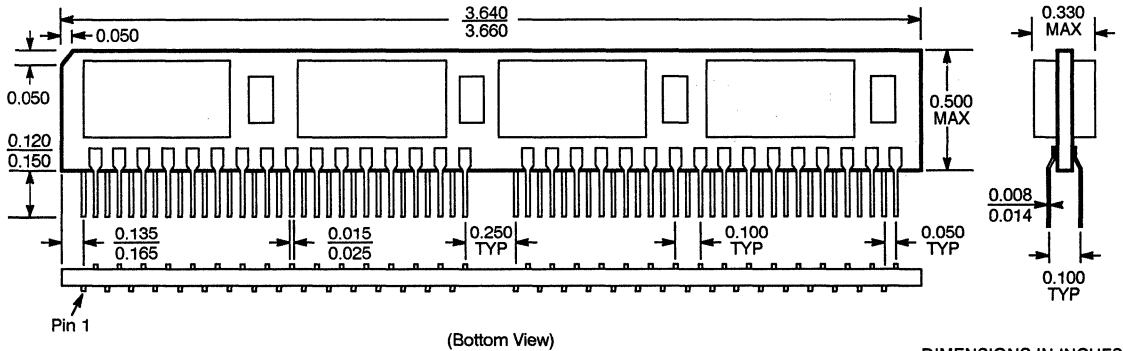
40 Pin Plastic SIP Module PS02



30 Pin Plastic SIP PS03



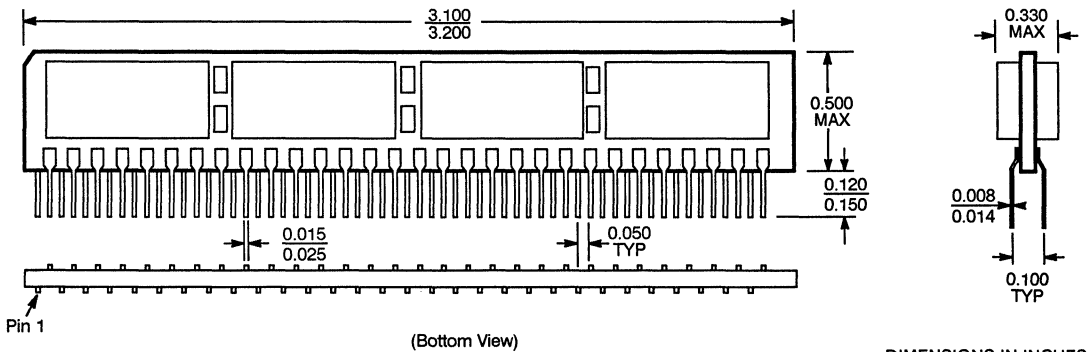
64 Pin Plastic ZIP Module PZ01



DIMENSIONS IN INCHES

MIN.  
MAX.

60 Pin Plastic ZIP Module PZ02



DIMENSIONS IN INCHES

MIN.  
MAX.



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Reagan/Compar  
42 Winding Brook Drive  
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Reagan/Compar  
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