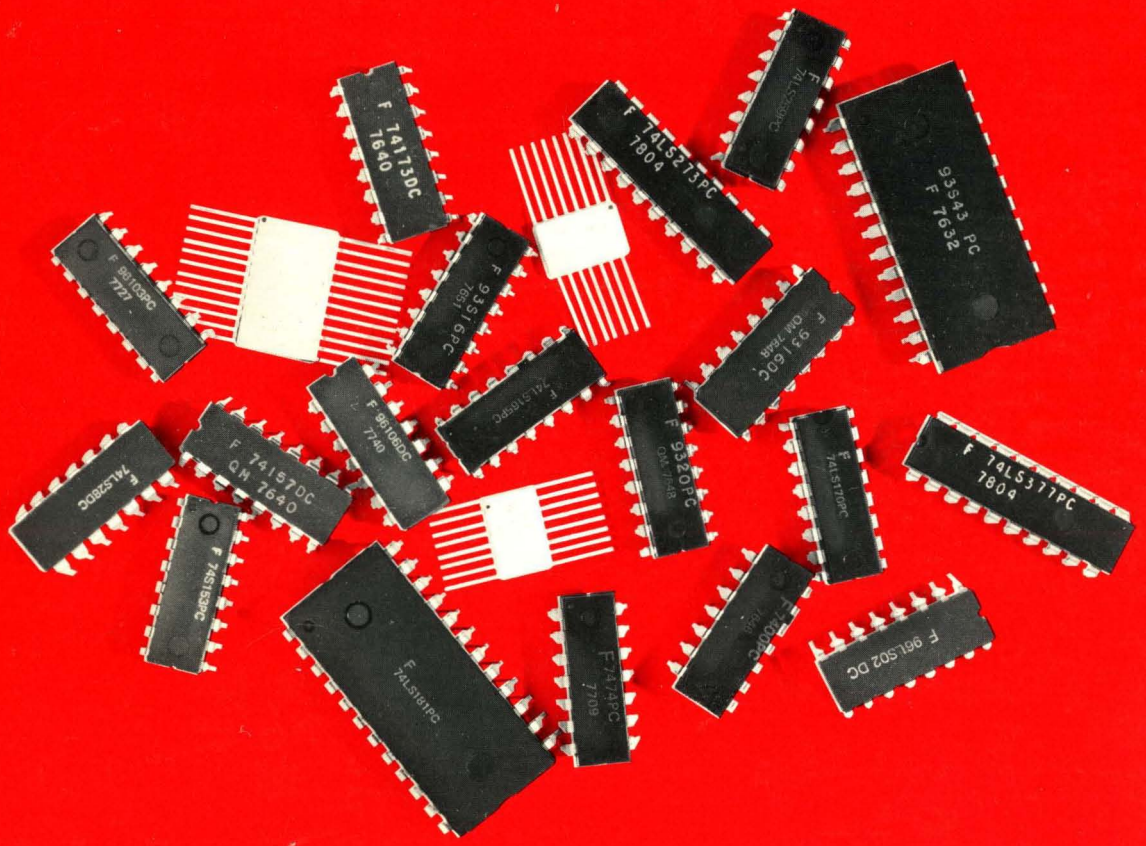
TTL DATA BOOK



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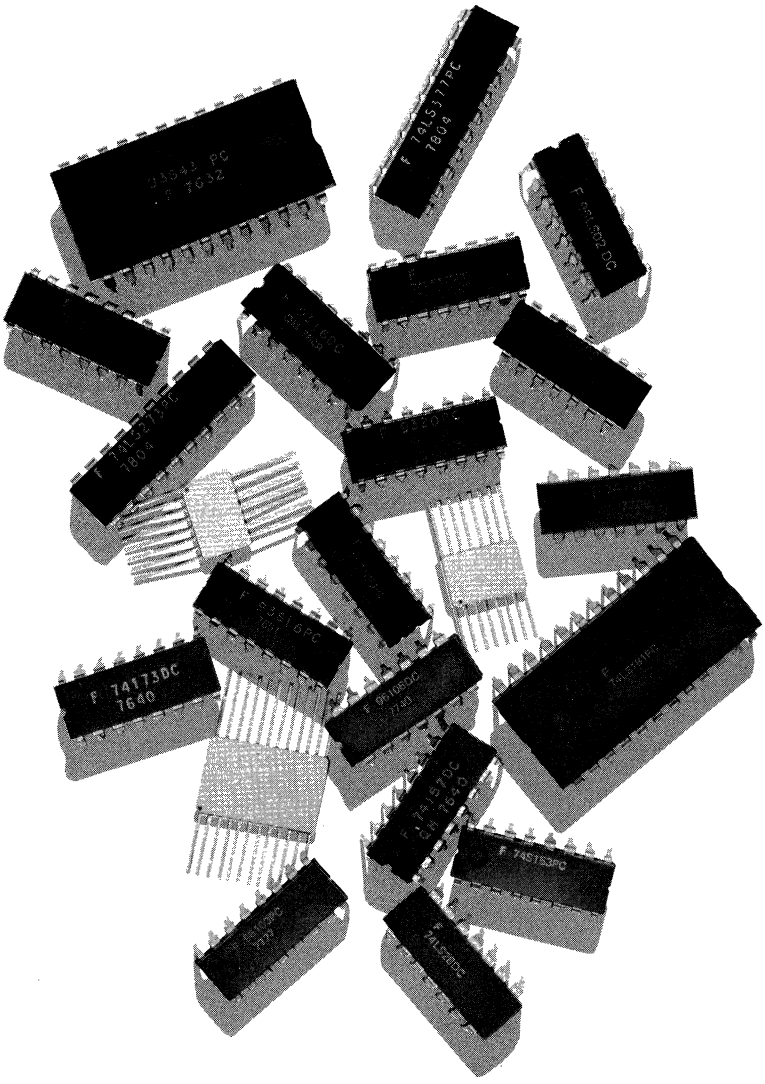
TTL DATA BOOK



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INTRODUCTION

This TTL DATA BOOK is a complete reference source for all Fairchild semiconductor SSI/MSI TTL products (except Fairchild Advanced Schottky TTL, FAST, devices). It is organized into the following sections:

Section 1 — Product Indices and Selection Guides
The Product Indices are divided according to the numbering system used, i.e., 54/74 Family TTL, 9XXX Family TTL, etc. Each index indicates which speed versions are available for the given product number and on which page the data sheet can be found. Selection Guides within this section are divided according to the device function. SSI functions are tabulated by speed family, MSI functions by their significant parameters.

Section 2 — TTL Characteristics
Section 2 defines the dc and ac parameter symbols used throughout this data book and discusses the general scheme for naming the various types of logic inputs and outputs. Speed/power trade-offs and basic gate schematics are compared for the different TTL circuit families. Input/output characteristics, thresholds and noise margins are discussed. Wiring, line driving and decoupling recommendations, as well as specific examples of interfacing TTL to other types of logic circuits, are included.

Section 3 — Loading, Specifications and Waveforms
This section contains dc specifications and ratings common to all devices in each family of circuits. Included is a discussion of the unit load method of normalizing the input and output characteristics of a circuit, and how to translate the numbers given in the Input Loading/Fan-Out table of a data sheet into the actual values of I_{IH}, I_{IL}, I_{OH} and I_{OL} currents. The various load configurations for ac testing, a table of R_L and C_L values for SSI gates and waveforms that help to define the various ac parameters are also included.

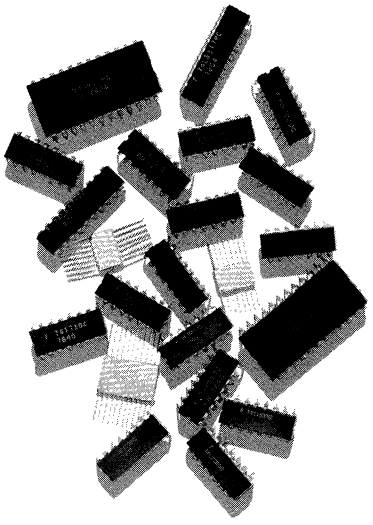
Section 4 through 7 — Family Data Sheets
Individual data sheets are grouped by product family (i.e., 54/74, 9XXX TTL, etc.) and arranged in numerical order within these families. The last two digits of the device number are repeated on the outside corner of each page for the convenience of the reader.

Section 8 — Other Digital Products
Shortform information on older logic families (DTL, CTL, RTL) is given for reference.

Section 9 — Ordering Information and Package Outlines
The simplified purchasing code which identifies not only the device type, but also the package type and temperature range, is explained. Detailed physical dimension drawings for each package are given.

Section 10 — Fairchild Field Sales Offices, Representatives and Distributors

TABLE OF CONTENTS



SECTION 1

- Indices
  54/74 Family TTL
  9XXX Family TTL
  93XX Family TTL
  96XX Family TTL

- Selection Guides
  SSI Functions
  Single and Dual Flip-Flops
  Latches
  Multiple Flip-Flops
  Multiplexers
  Decoders/Demultiplexers
  Registers
  Counters
  Monostables (One-Shots)
  Line and Bus Drivers/Transceivers/Receivers
  Display Decoder/Drivers
  Arithmetic Operators
  Random Access Memories

Section 1
PRODUCT INDICES AND SELECTION GUIDES

INDICES

54/74 FAMILY TTL

DEVICE NO.	DESCRIPTION	54/74 TTL	54H/74H H-TTL	54S/74S S-TTL	54LS/74LS LS-TTL	PAGE NO.
00	Quad 2-Input NAND Gate	X	X	X	X	4-3
01	Quad 2-Input NAND Gate	X	X			4-4
02	Quad 2-Input NOR Gate	X		X	X	4-5
03	Quad 2-Input NAND Gate	X		X	X	4-6
04	Hex Inverter	X	X	X	X	4-7
04A	Hex Inverter			X		4-7
05	Hex Inverter	X	X	X	X	4-8
05A	Hex Inverter			X		4-8
06	Hex Inverter Buffer/Driver	X				4-9
07	Hex Buffer/Driver	X				4-10
08	Quad 2-Input AND Gate	X	X	X	X	4-11
09	Quad 2-Input AND Gate	X		X	X	4-12
10	Triple 3-Input NAND Gate	X	X	X	X	4-13
11	Triple 3-Input AND Gate	X	X	X	X	4-14
12	Triple 3-Input NAND Gate	X				4-15
13	Dual 4-Input Schmitt Trigger	X			X	4-16
14	Hex Schmitt Trigger Inverter	X			X	4-17
15	Triple 3-Input AND Gate			X	X	4-18
16	Hex Inverter Buffer/Driver	X				4-19
17	Hex Buffer/Driver	X				4-20
20	Dual 4-Input NAND Gate	X	X	X	X	4-21
21	Dual 4-Input Positive AND Gate	X	X		X	4-22
22	Dual 4-Input NAND Gate	X	X	X	X	4-23
23	Expandable Dual 4-Input NOR Gate	X				4-24
25	Dual 4-Input NOR Gate	X				4-26
26	Quad 2-Input NAND Buffer	X			X	4-27
27	Triple 3-Input NOR Gate	X			X	4-28
28	Quad 2-Input NOR Buffer				X	4-29
30	8-Input NAND Gate	X	X	X	X	4-30

54/74 FAMILY TTL (Cont'd)

DEVICE NO.	DESCRIPTION	54/74 TTL	54H/74H H-TTL	54S/74S S-TTL	54LS/74LS LS-TTL	PAGE NO.
32	Quad 2-Input OR Gate	X		X	X	4-31
33	Quad 2-Input NOR Buffer				X	4-32
37	Quad 2-Input NAND Buffer	X			X	4-33
38	Quad 2-Input NAND Buffer	X			X	4-34
39	Quad 2-Input NAND Buffer	X				4-35
40	Dual 4-Input NAND Buffer	X	X	X	X	4-36
41	1-of-10 Decoder/Driver (Nixie)	9315				6-48
42	1-of-10 Decoder				X	4-37
42A	1-of-10 Decoder	X				4-37
43A	1-of-10 Decoder	X				4-37
44A	1-of-10 Decoder	X				4-37
45	1-of-10 Decoder/Driver	X				4-41
46A	BCD to 7-Segment Decoder/Driver	X				4-44
47	BCD to 7-Segment Decoder/Driver				X	4-44
47A	BCD to 7-Segment Decoder/Driver	X				4-44
48	BCD to 7-Segment Decoder	X			X	4-48
49	BCD to 7-Segment Decoder	X			X	4-51
50	Expandable Dual 2-Wide, 2-Input AND-OR-Invert Gate	X	X			4-54
51	Dual 2-Wide AND-OR-Invert Gate	X	X	X	X	4-56
52	Expandable 2-2-2-3-Input AND-OR Gate		X			4-57
53	Expandable AND-OR-Invert Gate	X	X			4-59
54	4-Wide, 2-Input AND-OR-Invert Gate	X	X		X	4-61
55	AND-OR-Invert Gate		X		X	4-63
60	Dual 4-Input Expander	X	X			4-64
61	Triple 3-Input Expander		X			4-67
62	3-2-2-3-Input AND-OR Expander		X			4-68
64	4-2-3-2-Input AND-OR-Invert Gate			X		4-70
65	4-2-3-2-Input AND-OR-Invert Gate			X		4-71
70	JK Edge-Trigger Flip-Flop	X				4-72
71	JK Master/Slave Flip-Flop		X			4-74
72	JK Master/Slave Flip-Flop	X	X			4-76
73	Dual JK Flip-Flop	X	X		X	4-78

54/74 FAMILY TTL (Cont'd)

DEVICE NO.	DESCRIPTION	54/74 TTL	54H/74H H-TTL	54S/74S S-TTL	54LS/74LS LS-TTL	PAGE NO.
74	Dual D-Type Positive Edge-Triggered Flip-Flop	X	X	X	X	4-81
75	4-Bit Bistable Latch	X				4-84
76	Dual JK Flip-Flop	X	X		X	4-86
77	Quad D-Type Latch	X				4-89
78	Dual JK Flip-Flop		X		X	4-90
80	Gated Full Adder	X				4-93
82	2-Bit Full Adder	X				4-95
83A	4-Bit Binary Full Adder	X			X	4-98
85	4-Bit Magnitude Comparator	X			X	4-101
86	Quad 2-Input Exclusive-OR Gate	X		X	X	4-105
87	4-Bit True/Complement, Zero/One Element		X			4-106
89	64-Bit Random Access Memory	X			X	4-108
90	Decade Counter				X	4-111
90A	Decade Counter	X				4-111
91A	8-Bit Shift Register	X				4-114
92	Divide-by-Twelve Counter				X	4-117
92A	Divide-by-Twelve Counter	X				4-117
93	Divide-by-Sixteen Counter				X	4-120
93A	Divide-by-Sixteen Counter	X				4-120
94	4-Bit Shift Register	X				4-123
95A	4-Bit Right/Left Shift Register	X				4-126
95B	4-Bit Right/Left Shift Register				X	4-126
96	5-Bit Shift Register	X				4-129
97	Synchronous Modulo-64 Bit Rate Multiplier	X				4-132
101	JK Edge-Triggered Flip-Flop		X			4-138
102	JK Edge-Triggered Flip-Flop		X			4-140
103	Dual JK Edge-Triggered Flip-Flop		X			4-142
106	Dual JK Edge-Triggered Flip-Flop		X			4-144
107	Dual JK Flip-Flop	X			X	4-146
108	Dual JK Edge-Triggered Flip-Flop		X			4-149
109	Dual $J\overline{K}$ Positive Edge-Triggered Flip-Flop			X	X	4-151

54/74 FAMILY TTL (Cont'd)

DEVICE NO.	DESCRIPTION	54/74 TTL	54H/74H H-TTL	54S/74S S-TTL	54LS/74LS LS-TTL	PAGE NO.
112	Dual JK Negative Edge-Triggered Flip-Flop			X	X	4-153
113	Dual JK Edge-Triggered Flip-Flop			X	X	4-155
114	Dual Negative Edge-Triggered Flip-Flop			X	X	4-157
116	Dual 4-Bit Latch	9308				6-24
121	Monostable Multivibrator	X				4-159
122	Retriggerable Resettable Multivibrator	X				4-163
123	Dual Retriggerable Resettable Multivibrator	X				4-166
125	Quad Bus Buffer Gate	X				4-169
125A	Quad Bus Buffer Gate				X	4-169
126	Quad Bus Buffer Gate	X			X	4-170
132	Quad 2-Input Schmitt Trigger NAND Gate	X		X	X	4-171
133	13-Input NAND Gate			X	X	4-172
134	12-Input NAND Gate			X		4-173
135	Quad Exclusive-OR/NOR Gate			X		4-174
136	Quad 2-Input Exclusive-OR Gate				X	4-175
137	1-of-8 Decoder/Demultiplexer			X		4-176
138	1-of-8 Decoder/Demultiplexer			X	X	4-180
139	Dual 1-of-4 Decoder			X	X	4-183
140	Dual 4-Input NAND Line Driver			X		4-186
141	1-of-10 Decoder/Driver (Nixie)	X				4-187
145	1-of-10 Decoder/Driver	X				4-189
150	16-Input Multiplexer	X				4-192
151	8-Input Multiplexer			X	X	4-194
151A	8-Input Multiplexer	X				4-194
152	8-Input Multiplexer				X	4-197
152A	8-Input Multiplexer	X				4-197
153	Dual 4-Input Multiplexer	X		X	X	4-199
154	1-of-16 Decoder/Demultiplexer	X				4-202
155	Dual 1-of-4 Decoder/Demultiplexer	X			X	4-205
156	Dual 1-of-4 Decoder/Demultiplexer	X			X	4-208
157	Quad 2-Input Multiplexer	X		X	X	4-210

54/74 FAMILY TTL (Cont'd)

DEVICE NO.	DESCRIPTION	54/74 TTL	54H/74H H-TTL	54S/74S S-TTL	54LS/74LS LS-TTL	PAGE NO.
158	Quad 2-Input Multiplexer			X	X	4-213
160	Synchronous Presettable BCD Decade Counter	X		93S10	X	4-215/ 6-30
161	Synchronous Presettable Binary Counter	X			X	4-221
162	Synchronous Presettable BCD Decade Counter	X			X	4-215
163	Synchronous Presettable Binary Counter	X			X	4-221
164	Serial-In Parallel-Out Shift Register	X			X	4-224
165	8-Bit Parallel-to-Serial Converter	X			X	4-227
166	8-Bit Shift Register	X				4-230
167	Synchronous Decade Rate Multiplier	X				4-232
168	Synchronous Bidirectional BCD Decade Counter				X	4-239
169	Synchronous Bidirectional Modulo-16 Binary Counter				X	4-242
170	4 x 4 Register File	X			X	4-244
173	4-Bit D-Type Register	X			X	4-247
174	Hex D Flip-Flop	X		X	X	4-250
175	Quad D Flip-Flop	X		X	X	4-253
176	Presettable Decade Counter	X				4-256
177	Presettable Binary Counter	X				4-260
178	4-Bit Shift Register	X				4-262
179	4-Bit Shift Register	X				4-264
180	8-Bit Parity Generator/Checker	X				4-267
181	4-Bit Arithmetic Logic Unit	9341		93S41	X	4-269/ 6-87
182	Carry Lookahead Generator	9342		93S42		6-94
183	Dual High Speed Adder		X			4-275
189	64-Bit Random Access Memory			X	X	4-277
190	Up/Down Decade Counter	X			X	4-280
191	Up/Down Binary Counter	X			X	4-285
192	Up/Down Decade Counter	X			X	4-287
193	Up/Down Binary Counter	X			X	4-291

54/74 FAMILY TTL (Cont'd)

DEVICE NO.	DESCRIPTION	54/74 TTL	54H/74H H-TTL	54S/74S S-TTL	54LS/74LS LS-TTL	PAGE NO.
194	4-Bit Bidirectional Universal Shift Register	X		X		4-293
194A	4-Bit Bidirectional Universal Shift Register				X	4-293
195	Universal 4-Bit Shift Register	X	93H00	93S00		4-296/ 6-3
195A	Universal 4-Bit Shift Register				X	4-296
196	Presettable Decade Counter	X			X	4-299
197	Presettable Binary Counter	X			X	4-303
198	8-Bit Right/Left Shift Register	X				4-305
199	8-Bit Parallel I/O Shift Register	X				4-308
240	Octal Buffer/Line Driver			X	X	4-311
241	Octal Buffer/Line Driver			X	X	4-311
242	Quad Bus Transceiver				X	4-314
243	Quad Bus Transceiver				X	4-314
244	Octal Buffer/Line Driver				X	4-311
245	Octal Bus Transceiver				X	4-316
247	BCD to 7-Segment Decoder/Driver				X	4-318
248	BCD to 7-Segment Decoder				X	4-319
249	BCD to 7-Segment Decoder				X	4-320
251	8-Input Multiplexer			X	X	4-321
253	Dual 4-Input Multiplexer			X	X	4-324
256	Dual 4-Bit Addressable Latch				X	4-327
257	Quad 2-Input Multiplexer			X	X	4-330
257A	Quad 2-Input Multiplexer				X	4-333
258	Quad 2-Input Multiplexer			X	X	4-334
258A	Quad 2-Input Multiplexer				X	4-337
259	8-Bit Addressable Latch				X	4-338
260	Dual 5-Input NOR Gate			X	X	4-341
266	Quad 2-Input Exclusive-NOR Gate				X	4-342
273	8-Bit Register				X	4-343
279	Quad Set-Reset Latch	X			X	4-345
280	9-Bit Parity Generator/Checker			X		4-346
283	4-Bit Binary Full Adder	X			X	4-348
289	64-Bit Random Access Memory			X	X	4-352

54/74 FAMILY TTL (Cont'd)

DEVICE NO.	DESCRIPTION	54/74 TTL	54H/74H H-TTL	54S/74S S-TTL	54LS/74LS LS-TTL	PAGE NO.
290	BCD Decade Counter	X			X	4-355
293	Modulo-16 Binary Counter	X			X	4-356
295A	4-Bit Shift Register				X	4-357
298	Quad 2-Port Register	X			X	4-360
299	8-Input Universal Shift/Storage Register				X	4-363
322	8-Bit Serial/Parallel Register				X	4-366
323	8-Bit Universal Shift/Storage Register				X	4-370
347	BCD to 7-Segment Decoder				X	4-373
352	Dual 4-Input Multiplexer				X	4-374
353	Dual 4-Input Multiplexer				X	4-377
365A	Hex 3-State Buffer				X	4-380
366A	Hex 3-State Inverter Buffer				X	4-381
367A	Hex 3-State Buffer				X	4-382
368A	Hex 3-State Inverter Buffer				X	4-383
373	Octal Transparent Latch				X	4-384
374	Octal D-Type Flip-Flop				X	4-387
375	4-Bit Latch				X	4-389
377	Octal D Flip-Flop				X	4-391
378	Parallel D Register				X	4-394
379	Quad Parallel Register				X	4-397
384	8-Bit Serial/Parallel Twos Complement Multiplier				X	4-400
390	Dual Decade Counter				X	4-405
393	Dual Modulo-16 Counter				X	4-408
395	Shift Register				X	4-410
447	BCD to 7-Segment Decoder				X	4-413
490	Dual Decade Counter				X	4-414
502	8-Bit Successive Approximation Register				X	4-416
503	8-Bit Successive Approximation Register				X	4-420
504	12-Bit Successive Approximation Register				X	4-423
533	Octal Transparent Latch				X	4-425

54/74 FAMILY TTL (Cont'd)

DEVICE NO.	DESCRIPTION	54/74 TTL	54H/74H H-TTL	54S/74S S-TTL	54LS/74LS LS-TTL	PAGE NO.
534	Octal D-Type Flip-Flop				X	4-426
540	Octal Buffer/Line Driver				X	4-427
541	Octal Buffer/Line Driver				X	4-427
563	Octal D-Type Latch				X	4-429
564	Octal D-Type Latch				X	4-430
573	Octal D-Type Flip-Flop				X	4-431
574	Octal D-Type Flip-Flop				X	4-432
670	4 x 4 Register File				X	4-433

9XXX FAMILY TTL

DEVICE NO.	DESCRIPTION	PAGE NO.	DEVICE NO.	DESCRIPTION	PAGE NO.
9000	JK Flip-Flop	5-3	**9009**	NAND Buffer	5-17
9001	JK Flip-Flop	5-3	**9012**	NAND Gate	5-10
9002	NAND Gate	5-10	**9014**	Quad Exclusive-OR Gate	5-19
9003	NAND Gate	5-10	**9015**	Quad NOR Gate	5-22
9004	NAND Gate	5-10	**9016**	Hex Inverter	5-10
9005	Extendable AND-OR-Invert Gate	5-13	**9017**	Hex Inverter	5-10
9006	Extender	5-13	**9020**	Dual JK Flip-Flop	5-3
9007	NAND Gate	5-10	**9022**	Dual JK Flip-Flop	5-3
9008	Entendable AND-OR-Invert Gate	5-13	**9024**	Dual JK (or D) Flip-Flop	5-24

93XX FAMILY TTL

DEVICE NO.	DESCRIPTION	93XX TTL	93H H-TTL	93L L-TTL	93S S-TTL	PAGE NO.
00	4-Bit Universal Shift Register	X	X	X	X	6-3
01	1-of-10 Decoder	X		X		6-7
02	1-of-10 Decoder	X				6-10
04	Dual Full Adder	X				6-13
05	Variable Modulus Counter	X				6-16
07	7-Segment Decoder	X				6-20
08	Dual 4-Bit Latch	X		X		6-24
09	Dual 4-Input Multiplexer	X		X		6-27

93XX FAMILY TTL (Cont'd)

DEVICE NO.	DESCRIPTION	93XX TTL	93H H-TTL	93L L-TTL	93S S-TTL	PAGE NO.
10	BCD Decade Counter	X		X	X	6-30
11	1-of-16 Decoder/Demultiplexer	X		X		6-36
12	8-Input Multiplexer	X		X	X	6-39
13	8-Input Multiplexer	X				6-42
14	Quad Latch	X		X		6-45
15	1-of-10 Decoder	X				6-48
16	4-Bit Binary Counter	X		X	X	6-30
17B	7-Segment Decoder/Driver	X				6-51
17C	7-Segment Decoder/Driver	X				6-51
18	8-Input Priority Encoder	X		X		6-56
19	Decade Sequencer	X				6-59
20	Decade Sequencer	X				6-59
21	Dual 1-of-4 Decoder	X		X		6-64
22	Quad 2-Input Multiplexer	X		X		6-66
24	5-Bit Comparator	X		X		6-69
28	Dual 8-Bit Shift Register	X		X		6-72
34	8-Input Addressable Latch	X		X		6-75
38	8-Bit Multiple Port Register	X		X		6-78
40	4-Bit Arithmetic Logic Unit	X				6-82
41	4-Bit Arithmetic Logic Unit	X		X	X	6-87
42	Carry Lookahead Generator	X			X	6-94
43	4-Bit by 2-Bit Twos Complement Multiplier				X	6-98
44	Binary (4-Bit by 2-Bit) Full Multiplier	X				6-101
46	High Speed 6-Bit Identity Comparator				X	6-106
47	High Speed 6-Bit Identity Comparator				X	6-109
48	12-Input Parity Checker/Generator	X				6-111
62	9-Input Parity Checker/Generator				X	6-114
68	7-Segment Decoder/Driver/Latch	X				6-117
70	7-Segment Decoder/Driver/Latch	X				6-123
72	High Speed 4-Bit Shift Register		X			6-127
74	7-Segment Decoder/Driver/Latch	X				6-130
86	4-Bit Quad Exclusive-NOR	X				6-138

96XX FAMILY TTL

DEVICE NO.	DESCRIPTION	96XX TTL	96L L-TTL	96S S-TTL	96LS LS-TTL	PAGE NO.
00	Retriggerable Resettable Monostable Multivibrator	X				7-3
01	Retriggerable Monostable Multivibrator	X				7-8
02	Dual Retriggerable Resettable Monostable Multivibrator	X	X	X	X	7-14/ 7-20
32	Address Multiplexer/Refresh Counter				X	7-27
42	Address Multiplexer/Refresh Counter				X	7-30
101	Quad 2-Input Positive NAND Buffer	X				7-33
103	Quad Bus Transceiver	X				7-34
106	Quad 2-Input NOR Receiver	X				7-36

SELECTION GUIDES

SSI FUNCTIONS

FUNCTION	9XXX	54/74	54H/74H	54S/74S	54LS/74LS
NAND Gates					
Hex Inverters	9016	54/7404	54H/74H04	54S/74S04 54S/74S04A	54LS/74LS04
Hex Inverters (OC*)	9017	54/7405	54H/74H05	54S/74S05 54S/74S05A	54LS/74LS05
Hex Inverter (15 V)		54/7416			
Hex Inverter (30 V)		54/7406			
Hex Schmitt Trigger		54/7414			54LS/74LS14
Quad 2-Input	9002	54/7400	54H/74H00	54S/74S00	54LS/74LS00
Quad 2-Input (OC*)	9012	54/7403		54S/74S03	54LS/74LS03
Quad 2-Input (OC*)		54/7401	54H/74H01		
Quad 2-Input (12 V)		7426			54LS/74LS26
Quad 2-Input (48 V)		54/7437			54LS/74LS37

*OC = Open-collector; 3S = 3-State

SSI FUNCTIONS (Cont'd)

FUNCTION	9XXX	54/74	54H/74H	54S/74S	54LS/74LS
NAND Gates (Cont'd)					
Quad 2-Input (OC*/48 mA)		54/7438			54LS/74LS38
Quad 2-Input Line Driver	96101	54/7439			
Quad 2-Input Schmitt		54/74132		54S/74S132	54LS/74LS132
Triple 3-Input	9003	54/7410	54H/74H10	54S/74S10	54LS/74LS10
Triple 3-Input (OC*)		54/7412			
Dual 4-Input	9004	54/7420	54H/74H20	54S/74S20	54LS/74LS20
Dual 4-Input Schmitt		54/7413			54LS/74LS13
Dual 4-Input (OC*)		54/7422	54H/74H22	54S/74S22	54LS/74LS22
Dual 4-Input Buffer	9009	54/7440	54H/74H40	54S/74S40	54LS/74LS40
Dual 4-Input Line Driver				54S/74S140	
8-Input	9007				
8-Input		54/7430	54H/74H30	54S/74S30	54LS/74LS30
13-Input				54S/74S133	54LS/74LS133
12-Input (3S*)				54S/74S134	
NOR Gates					
Quad 2-Input		54/7402		54S/74S02	54LS/74LS02
Quad 2-Input	9015				
Triple 3-Input		54/7427			54LS/74LS27
Dual 4-Input w/Strobe		54/7425			
Dual 4-Input (Exp)		54/7423			
Dual 5-Input				54S/74S260	54LS/74LS260
Quad 2-Input					54LS/74LS28
Quad 2-Input (OC*)					54LS/74LS33
AND Gates					
Hex Buffer (OC*/15 V)		54/7417			
Hex Buffer (OC*/30 V)		54/7407			
Quad 2-Input		54/7408	54H/74H08	54S/74S08	54LS/74LS08
Quad 2-Input (OC*)		54/7409		54S/74S09	54LS/74LS09
Triple 3-Input		54/7411	54H/74H11	54S/74S11	54LS/74LS11
Triple 3-Input (OC*)				54S/74S15	54LS/74LS15
Dual 4-Input		54/7421	54H/74H21		54LS/74LS21

*OC = Open-Collector; 3S = 3-State

SSI FUNCTIONS (Cont'd)

FUNCTION	9XXX	54/74	54H/74H	54S/74S	54LS/74LS
OR Gates					
Quad 2-Input		54/7432		54S/74S32	54LS/74LS32
Exclusive-OR Gates					
Quad 2-Input		54/7486		54S/74S86	54LS/74LS86
Quad 2-Input (OC*)					54LS/74LS136
Quad 2-Input OR/NOR	9014				
Quad 2-Input OR/NOR				54S/74S135	
Exclusive-NOR Gate					
Quad 2-Input (OC*)		9386 (8242)			54LS/74LS266
AND-OR Gates					
2-2-2-3 Input (Exp)			54H/74H52		
AND-OR-INVERT Gates					
Dual 2-2 Input (Exp)	9005	54/7450	54H/74H50		
Dual 2-2 Input		54/7451	54H/74H51	54S/74S51	54LS/74LS51
2-2-2-3 Input (Exp)	9008	54/7453	54H/74H53		
2-2-2-3 Input		54/7454	54H/74H54		
2-2-3-3 Input					54LS/74LS54
2-2-3-4 Input				54S/74S64	
2-2-3-4 Input (OC*)				54S/74S65	
4-4 Input (Exp)			54H/74H55		
4-4 Input					54LS/74LS55
Gate Expanders					
Triple 3-Input			54H/74H61		
Dual 4-Input	9006	54/7460	54H/74H60		
2-2-3-3 AND-OR			54H/74H62		
Buffer Gates and Drivers					
Quad Buffer (3S*)		54/74125			54LS/74LS125A
Quad Buffer (3S*)		54/74126			54LS/74LS126
Hex (3S*)					54LS/74LS365A
Hex Inverter (3S*)					54LS/74LS366A
Hex (3S*)					54LS/74LS367A
Hex Inverter (3S*)					54LS/74LS368A

*OC = Open-Collector; 3S = 3-State

SINGLE AND DUAL FLIP-FLOPS

FUNCTION	DEVICE NO.	INPUTS	CLOCK EDGE	DIRECT SET	DIRECT CLEAR	GUARANTEED CLOCK FREQ. MHz
Single JK	**9000**	3J, 3K, JK	↓	X	X	20 (Typ)
Single JK	**9001**	2J, 2K, J, K, JK	↓	X	X	50 (Typ)
Single JK	**54H/74H71**	(AOI) (2 + 2)J, (2 + 2)K	↓	X		25
Single JK	**54H/74H101**	(AOI) (2 + 2)J, (2 + 2)K	↓	X		40
Single JK	**54/7472**	3J, 3K	↓	X	X	15
Single JK	**54H/74H72**	3J, 3K	↓	X	X	25
Single JK	**54H/74H102**	3J, 3K	↓	X	X	40
Single JK	**54/7470**	2J, 2K, $\overline{J}$, $\overline{K}$	↓	X	X	20
Dual D	**54/7474**	D	↓	X	X	15
Dual D	**54H/74H74**	D	↓	X	X	35
Dual D	**54S/74S74**	D	↓	X	X	75
Dual D	**54LS/74LS74**	D	↓	X	X	30
Dual JK	**9020**	J, K, $\overline{J}$, $\overline{K}$, JK	↓		X	50 (Typ)
Dual JK	**9022**	J, $\overline{K}$, JK	↓	X	X	50 (Typ)
Dual JK	**54/7473**	J, K	↓		X	15
Dual JK	**54/74107**	J, K	↓		X	15
Dual JK	**54H/74H73**	J, K	↓		X	25
Dual JK	**54H/74H103**	J, K	↓		X	40
Dual JK	**54S/74S113**	J, K	↓	X		80
Dual JK	**54LS/74LS113**	J, K	↓	X		30
Dual JK	**54/7476**	J, K	↓	X	X	15
Dual JK	**54H/74H76**	J, K	↓	X	X	25
Dual JK	**54H/74H106**	J, K	↓	X	X	40
Dual JK	**54S/74S112**	J, K	↓	X	X	80
Dual JK	**54LS/74LS112**	J, K	↓	X	X	30
Dual JK	**54H/74H78**	J, K	↓	X	X	25
Dual JK	**54H/74H108**	J, K	↓	X	X	40
Dual JK	**54LS/74LS73**	J, K	↓		X	30
Dual JK	**54S/74S114**	J, K	↓	X	X	80
Dual JK	**54LS/74LS114**	J, K	↓	X	X	30
Dual JK	**9024, 54/74109**	J, K	↓	X	X	25

SINGLE AND DUAL FLIP-FLOPS (Cont'd)

FUNCTION	DEVICE NO.	INPUTS	CLOCK EDGE	DIRECT SET	DIRECT CLEAR	GUARANTEED CLOCK FREQ. MHz
Dual JK	**54S/74S109**	J, K	↓	X	X	75
Dual JK	**54LS/74LS109**	J, K	↓	X	X	30
Dual JK	**54LS/74LS76**	J, K	↓	X	X	30
Dual JK	**54LS/74LS107**	J, K	↓		X	30
Dual JK	**54LS/74LS78**	J, K	↓	X	X	30

LATCHES

FUNCTION	DEVICE NO.	DATA INPUTS	COMMON CLEAR	ENABLE INPUTS (LEVEL)	MIN ENABLE PULSE WIDTH ns	MAX DELAY ENABLE TO OUTPUT-ns
4-Bit RS Latch	**9314**	4 X ($\overline{R}_1\overline{S}_1$)	L	1 (L)	18	24
4-Bit RS Latch	**93L14**	4 X ($\overline{R}_1\overline{S}_1$)	L	1 (L)	30	45
4-Bit D Latch	**9314**	4 X D	L	1 (L)	18	24
4-Bit D Latch	**93L14**	4 X D	L	1 (L)	30	45
Dual 4-Bit D Latch	**9308 (54/74116)**	8 X D	2 X L	2 X 2 AND	18	30
Dual 4-Bit D Latch	**93L08**	8 X D	2 X L	2 X 2 AND	30	45
4-Bit RS Latch	**54/74279**	4 X ($\overline{R}\overline{S}$)				
4-Bit RS Latch	**54LS/74LS279**	4 X ($\overline{R}\overline{S}$)				
4-Bit D Latch	**54/7475**	4 X D		2 (H)	20	30
4-Bit D Latch	**54/7477**	4 X D		2 (H)	20	30
4-Bit D Latch	**54LS/74LS375**	4 X D		2 (H)	20	30
Dual 4-Bit Addr. Latch	**54LS/74LS256**	8 X D	L	2 (L)	17	27
8-Bit Addr. Latch	**9334**	1 X D	L	1 (L)	17	24
8-Bit Addr. Latch	**93L34**	1 X D	L	1 (L)	26	45
8-Bit D Latch	**54LS/74LS373**	8 X D		1 (H)	15	30
8-Bit D Latch	**54LS/74LS573**	8 X D		1 (L)	15	30
8-Bit D Latch	**54LS/74LS533**	8 X D		1 (H)	15	30
8-Bit D Latch	**54LS/74LS563**	8 X D		1 (H)	15	30
8-Bit Addr. Latch	**54LS/74LS259**	1 X D	L	1 (L)	17	27
16-Bit D Latch	**54/74170**	4 X D		2	25	45
16-Bit D Latch	**54LS/74LS170**	4 X D		2	25	35
16-Bit D Latch	**54LS/74LS670**	4 X D		2	25	35
64-Bit Memory	**54/7489**	4 X D		2 (L)	40	70

LATCHES (Cont'd)

FUNCTION	DEVICE NO.	DATA INPUTS	COMMON CLEAR	ENABLE INPUTS (LEVEL)	MIN ENABLE PULSE WIDTH ns	MAX DELAY ENABLE TO OUTPUT-ns
64-Bit Memory	**54LS/74LS89**	4 X D		2 (L)	25 (Typ)	30 (Typ)
64-Bit Memory	**54S/74S189**	4 X D		2 (L)	20	40
64-Bit Memory	**54LS/74LS189**	4 X D		2 (L)	25 (Typ)	30 (Typ)
64-Bit Memory	**54S/74S289**	4 X D		2 (L)	20	40
64-Bit Memory	**54LS/74LS289**	4 X D		2 (L)	25 (Typ)	30 (Typ)

MULTIPLE FLIP-FLOPS

FUNCTION	DEVICE NO.	DATA INPUTS	COMMON CLEAR	CP INPUTS (LEVEL)	GUARANTEED CLOCK FREQ. MHz
4-Bit D Flip-Flop	**54/74175**	4 X D	L	1 (↑)	25
4-Bit D Flip-Flop	**54S/74S175**	4 X D	L	1 (↑)	75
4-Bit D Flip-Flop	**54LS/74LS175**	4 X D	L	1 (↑)	30
4-Bit D Flip-Flop	**54/74298**	2 X 4 X D		1 (↓)	25
4-Bit D Flip-Flop	**54LS/74LS298**	2 X 4 X D		1 (↓)	25
6-Bit D Flip-Flop	**54/74174**	6 X D	L	1 (↑)	25
6-Bit D Flip-Flop	**54S/74S174**	6 X D	L	1 (↑)	75
6-Bit D Flip-Flop	**54LS/74LS174**	6 X D	L	1 (↑)	30
8-Bit Multiple Port Register	**9338**	1 X D		1 (L)	27
8-Bit Multiple Port Register	**93L38**	1 X D		1 (L)	14
8-Bit D Flip-Flop	**54LS/74LS374**	8 X D		1 (↑)	35
8-Bit D Flip-Flop	**54LS/74LS534**	8 X D		1 (↑)	35
8-Bit D Flip-Flop	**54LS/74LS564**	8 X D		1 (↑)	35

MULTIPLEXERS

FUNCTION	DEVICE NO.	ENABLE INPUTS	TRUE OUTPUT	COMPLEMENT OUTPUT
Quad 2-Input	**9322**	1	X	
Quad 2-Input	**93L22**	1	X	
Quad 2-Input	**54/74157**	1	X	
Quad 2-Input	**54S/74S157**	1	X	
Quad 2-Input	**54LS/74LS157**	1	X	
Quad 2-Input	**54S/74S158**	1		X
Quad 2-Input	**54LS/74LS158**	1		X

MULTIPLEXERS (Cont'd)

FUNCTION	DEVICE NO.	ENABLE INPUTS	TRUE OUTPUT	COMPLEMENT OUTPUT
Quad 2-Input	**54S/74S257**	1	3S*	
Quad 2-Input	**54LS/74LS257**	1	3S*	
Quad 2-Input	**54LS/74LS257A**	1	3S*	
Quad 2-Input	**54S/74S258**	1		3S*
Quad 2-Input	**54LS/74LS258**	1		3S*
Quad 2-Input	**54LS/74LS258A**	1		3S*
Quad 2-Input	**54/74298**	Clocked (Edge-Trigger)	X (Latched)	
Quad 2-Input	**54LS/74LS298**	Clocked (Edge-Trigger)	X (Latched)	
Dual 4-Input	**9309**		X	X
Dual 4-Input	**93L09**		X	X
Dual 4-Input	**54/74153**	2	X	
Dual 4-Input	**54S/74S153**	2	X	
Dual 4-Input	**54LS/74LS153**	2	X	
Dual 4-Input	**54S/74S253**	2	3S*	
Dual 4-Input	**54LS/74LS253**	2	3S*	
Dual 4-Input	**54LS/74LS352**	2		X
Dual 4-Input	**54LS/74LS353**	2		3S*
8-Input	**9312**	1	X	X
8-Input	**93L12**	1	X	X
8-Input	**93S12**	1	X	X
8-Input	**9313**	1	X	OC*
8-Input	**54/74151A**	1	X	X
8-Input	**54S/74S151**	1	X	X
8-Input	**54LS/74LS151**	1	X	X
8-Input	**54S/74S251**	1	3S*	3S*
8-Input	**54LS/74LS251**	1	3S*	3S*
8-Input	**54/74152A**			X
8-Input	**54LS/74LS152**			X
12-Input	**96LS42**	1		X
14-Input	**96LS32**	1		X
16-Input	**54/74150**	1		X

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DECODERS/DEMULTIPLEXERS

FUNCTION	DEVICE NO.	ADDRESS INPUTS	ACTIVE LOW ENABLE	ACTIVE LOW OUTPUTS	OPEN-COLLECTOR OUTPUT VOLTAGE V
Dual 1-of-4	**9321**	2 + 2	1 + 1	4 + 4	
Dual 1-of-4	**93L21**	2 + 2	1 + 1	4 + 4	
Dual 1-of-4	**54S/74S139**	2 + 2	1 + 1	4 + 4	
Dual 1-of-4	**54LS/74LS139**	2 + 2	1 + 1	4 + 4	
Dual 1-of-4	**54/74155**	2	2 + 1	4 + 4	
Dual 1-of-4	**54LS/73LS155**	2	2 + 1	4 + 4	
Dual 1-of-4	**54/74156**	2	2 + 1	4 + 4	5.5
Dual 1-of-4	**54LS/74LS156**	2	2 + 1	4 + 4	5.5
1-of-8	**9301**	3	1	8	
1-of-8	**93L01**	3	1	8	
1-of-8	**9302**	3	1	8	5.5
1-of-8	**9334**	3	1	8	
1-of-8	**93L34**	3	1	8	
1-of-8	**54LS/74LS259**	3	1	8 H	
1-of-8	**54/7445**	3	1	8	30
1-of-8	**54/7442A**	3	1	8	
1-of-8	**54LS/74LS42**	3	1	8	
1-of-8	**54S/74S138**	3	2	8	
1-of-8	**54LS/74LS138**	3	2	8	
1-of-8	**54/74145**	3	1	8	15
1-of-8 w/Input Latches	**54S/74S137**	3	2	8	
1-of-10	**9301**	4 (BCD)		10	
1-of-10	**93L01**	4 (BCD)		10	
1-of-10	**9302**	4 (BCD)		10	5.5
1-of-10	**54/7445**	4 (BCD)		10	30
1-of-10	**54/7442A**	4 (BCD)		10	
1-of-10	**54LS/74LS42**	4 (BCD)		10	
1-of-10	**54/7443A**	4 (Excess-3)		10	
1-of-10	**54/7444A**	4 (Excess-3 Gray)		10	
1-of-10	**54/74145**	4 (BCD)		10	15
1-of-16	**9311**	4	2	16	

DECODERS/DEMULTIPLEXERS (Cont'd)

FUNCTION	DEVICE NO.	ADDRESS INPUTS	ACTIVE LOW ENABLE	ACTIVE LOW OUTPUTS	OPEN-COLLECTOR OUTPUT VOLTAGE V
1-of-16	**93L11**	4	2	16	
1-of-16	**54/74154**	4	2	16	
1-of-10 Decade Sequencer	**9319**		Clock	10	
1-of-10 Decade Sequencer	**9320**		Clock	10	3 K Pull-up

REGISTERS

FUNCTION	DEVICE NO.	NO. OF BITS	SERIAL ENTRY	PARALLEL ENTRY NO. OF BITS[1]	CLOCK EDGE	GUARANTEED CLOCK FREQ. MHz
Parallel-in/Parallel-out Shift Right	**9300**	4	J, $\overline{K}$	4S	⎍	30
Parallel-in/Parallel-out Shift Right	**93H00**	4	J, $\overline{K}$	4S	⎍	45
Parallel-in/Parallel-out Shift Right	**93L00**	4	J, $\overline{K}$	4S	⎍	10
Parallel-in/Parallel-out Shift Right	**93S00**	4	J, $\overline{K}$	4S	⎍	70
Parallel-in/Parallel-out Shift Right	**93H72**	4	D	4S	⎍	45
Serial/Parallel-in, Parallel-out, Shift Right	**54/7494**	4	D	2 X 4A (MUX)	⎍	10
Parallel-in/Parallel-out Shift Right	**54/7495A**	4	D	4S	⎎	25
Parallel-in/Parallel-out Shift Right	**54LS/74LS95B**	4	D	4S	⎎	30
Parallel-in/Parallel-out Shift Right	**54/74178**	4	D	4S	⎎	25
Parallel-in/Parallel-out Shift Right	**54/74179**	4	D	4S	⎎	25
Parallel-in/Parallel-out Shift Right	**54LS/74LS195A**	4	J, $\overline{K}$	4S	⎍	30
Parallel-in/Parallel-out Shift Right (3S[2])	**54LS/74LS295A**	4	D	4S	⎎	30

1. S = Synchronous; A = Asynchronous
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REGISTERS (Cont'd)

FUNCTION	DEVICE NO.	NO. OF BITS	SERIAL ENTRY	PARALLEL ENTRY NO. OF BITS[1]	CLOCK EDGE	GUARANTEED CLOCK FREQ. MHz
Parallel-in/Parallel-out Shift Right (3S[2])	**54LS/74LS395**	4	D	4S	↘	30
Parallel-in/Parallel-out Bidirectional	**54/74194**	4	DR, DL	4S	↗	25
Parallel-in/Parallel-out Bidirectional	**54S/74S194**	4	DR, DL	4S	↗	70
Parallel-in/Parallel-out Bidirectional	**54LS/74LS194A**	4	DR, DL	4S	↗	30
Quad D (3S[2])	**54/74173**	4		4S	↗	25
Quad D (3S[2])	**54LS/74LS173**	4		4S	↗	30
Quad D Flip-Flop	**54/74175**	4		4S	↗	25
Quad D Flip-Flop	**54S/74S175**	4		4S	↗	75
Quad D Flip-Flop	**54LS/74LS175**	4		4S	↗	30
Quad 2-Port Register	**54/74298**	4		2 D (MUX)	↘	30
Quad 2-Port Register	**54LS/74LS298**	4		2 D (MUX)	↘	30
Quad D	**54LS/74LS379**	4		4S	↗	30
Parallel-in/Parallel-out Shift Right	**54/7496**	5	D	5A	↗	10
Hex D Flip-Flop	**54/74174**	6		6S	↗	25
Hex D Flip-Flop	**54S/74S174**	6		6S	↗	75
Hex D Flip-Flop	**54LS/74LS174**	6		6S	↗	30
Parallel D Register	**54LS/74LS378**	6		6S	↗	30
Multiport Register	**9338**	8	D		↗	25
Multiport Register	**93L38**	8	D		↗	20
Parallel-in/Parallel-out Shift Right	**54/74199**	8	J, $\overline{K}$	8S	↗	25
Serial/Parallel-in, Parallel/Serial-out Shift Right (3S[2])	**54LS/74LS322**	8	2D	8S	↗	35
Serial-in/Parallel-out Shift Right	**54/74164**	8	2D		↗	25
Serial-in/Parallel-out Shift Right	**54LS/74LS164**	8	2D		↗	25

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REGISTERS (Cont'd)

FUNCTION	DEVICE NO.	NO. OF BITS	SERIAL ENTRY	PARALLEL ENTRY NO. OF BITS[1]	CLOCK EDGE	GUARANTEED CLOCK FREQ. MHz
Parallel/Serial-in, Serial-out, Shift Right	**54/74165**	8	D	8A	↓	25
Parallel/Serial-in, Serial-out, Shift Right	**54LS/74LS165**	8	D	8A	↓	30
Parallel/Serial-in, Serial-out, Shift Right	**54/74166**	8	D	8S	↓	25
Serial-in/Serial-out Shift Right	**54/7491A**	8	2D		↓	10
Successive Approx Register	**54LS/74LS502**	8	D		↓	15
Successive Approx Register	**54LS/74LS503**	8	D		↓	15
Parallel-in/Parallel-out Bidirectional	**54/74198**	8	DR, DL	8S	↓	25
Parallel-in/Parallel-out Bidirectional (3S[2])	**54LS/74LS299**	8	DR, DL	8S	↓	35
Parallel-in/Parallel-out Bidirectional (3S[2])	**54LS/74LS323**	8	DR, DL	8S	↓	35
Octal D Register	**54LS/74LS273**	8		8S	↓	30
Octal D Flip-Flop (3S[2])	**54LS/74LS374**	8		8S	↓	35
Octal D Flip-Flop	**54LS/74LS377**	8		8S	↓	30
Octal D Flip-Flop (3S[2])	**54LS/74LS574**	8		8S	↓	35
Successive Approx Register	**54LS/74LS504**	12	D		↓	15
Serial-in/Serial-out Shift Right	**9328**	2 X 8	2 X 2 D (MUX)		↓	20
Serial-in/Serial-out Shift Right	**93L28**	2 X 8	2 X 2 D (MUX)		↓	5.0
Register File (OC[2])	**54/74170**	4 X 4		4A	↑	
Register File (OC[2])	**54LS/74LS170**	4 X 4		4A	↑	
Register File (3S[2])	**54LS/74LS670**	4 X 4		4A	↑	

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COUNTERS

FUNCTION	DEVICE NO.	MODULUS	PARALLEL ENTRY*	CLOCK EDGE	GUARANTEED CLOCK FREQ. MHz
Asynchronous	**54/74290**	2 X 5		↘	32
Asynchronous	**54/7490A**	2 x 5		↘	32
Asynchronous	**54LS/74LS90**	2 X 5		↘	32
Asynchronous	**54/7492A**	2 X 6		↘	32
Asynchronous	**54LS/74LS92**	2 X 6		↘	32
Asynchronous	**54/74293**	2 X 8		↘	32
Asynchronous	**54/7493A**	2 X 8		↘	32
Asynchronous	**54LS/74LS93**	2 X 8		↘	32
Asynchronous	**54/74176**	2 X 5	A	↘	35
Asynchronous	**54/74177**	2 X 8	A	↘	35
Asynchronous	**54/74196**	2 X 5	A	↘	50
Asynchronous	**54LS/74LS196**	2 X 5	A	↘	45
Asynchronous	**54/74197**	2 X 8	A	↘	50
Asynchronous	**54LS/74LS197**	2 X 8	A	↘	50
Asynchronous	**54LS/74LS290**	2 X 5		↘	32
Asynchronous	**54LS/74LS293**	2 X 8		↘	32
Asynchronous	**54LS/74LS390**	2 X 5		↘	40
Asynchronous	**54LS/74LS393**	2 X 8		↘	40
Asynchronous	**54LS/74LS490**	2 X 5		↘	40
Variable Modulo	**9305**	2 X 5, 6, 7, 8		↗	23
Synchronous	**9310**	10 (Presettable)	S	↗	30
Synchronous	**93L10**	10 (Presettable)	S	↗	13
Synchronous	**93S10**	10 (Presettable)	S	↗	70
Synchronous	**9316**	16 (Presettable)	S	↗	30
Synchronous	**93L16**	16 (Presettable)	S	↗	13
Synchronous	**93S16**	16 (Presettable)	S	↗	70
Synchronous	**54/74160**	10 (Presettable)	S	↗	25
Synchronous	**54LS/74LS160**	10 (Presettable)	S	↗	25
Synchronous	**54/74161**	16 (Presettable)	S	↗	25
Synchronous	**54LS/74LS161**	16 (Presettable)	S	↗	25
Synchronous	**54/74162**	10 (Presettable)	S	↗	25
Synchronous	**54LS/74LS162**	10 (Presettable)	S	↗	25
Synchronous	**54/74163**	16 (Presettable)	S	↗	25

*S = Synchronous; A = Asynchronous

COUNTERS (Cont'd)

FUNCTION	DEVICE NO.	MODULUS	PARALLEL ENTRY*	CLOCK EDGE	GUARANTEED CLOCK FREQ. MHz
Synchronous	**54LS/74LS163**	16 (Presettable)	S	↓	25
Up/Down	**54LS/74LS168**	10 (Presettable)	S	↓	25
Up/Down	**54LS/74LS169**	16 (Presettable)	S	↓	25
Up/Down	**54/74192**	10	A	↓	25
Up/Down	**54LS/74LS192**	10	A	↓	30
Up/Down	**54/74193**	16	A	↓	25
Up/Down	**54LS/74LS193**	16	A	↓	30
Up/Down	**54/74190**	10	A	↓	20
Up/Down	**54LS/74LS190**	10	A	↓	20
Up/Down	**54/74191**	16	A	↓	20
Up/Down	**54LS/74LS191**	16	A	↓	20
Rate Multiplier	**54/7497**	m.f./64		↓	25
Rate Multiplier	**54/74167**	m.f./10		↓	25

MONOSTABLES (ONE-SHOTS)

FUNCTION	DEVICE NO.	PULSE WIDTH VARIATION (%)		NO. OF INPUTS		RESETTABLE	MIN OUTPUT
		vs. TEMP	vs. V_{CC}	POS	NEG		(t_W) ns
Single Retriggerable	**9600**	±1.5	±1.5	3	2	X	75
Single Retriggerable	**9601**	±2.7	±1.0	2	2		50
Dual Retriggerable	**9602**	±1.5	±1.5	1	1	X	72
Dual Retriggerable	**96L02**	±1.6	±1.5	1	1	X	110
Dual Retriggerable	**96S02**	±1.0	±1.0	1	1	X	27
Single Non-Retriggerable	**54/74121**	±0.25	±0.15	1	2		40
Single Retriggerable	**54/74122**	±2.7	±1.0	2	2	X	45
Dual Retriggerable	**54/74123**	±2.7	±1.0	1	1	X	45
Dual Retriggerable	**96LS02**	±1.0	±0.8	1	1	X	35

*S = Synchronous; A = Asynchronous

LINE AND BUS DRIVERS/TRANSCEIVERS/RECEIVERS

FUNCTION	DEVICE NO.	COMPANION RECEIVER	I_{OL} mA	I_{OS} mA (MIN)
Quad 2 NAND Driver	**54/7437**	Any TTL	48	-20
Quad 2 NAND Driver (OC*)	**54/7438**	96106	48	OC*
Quad 2 NAND Driver (OC*)	**96101**	96106	80	OC*
Quad 2 NAND Driver	**9009**	Any TTL	52.8	-40
Dual 2 NAND Driver	**54/7440**	Any TTL	48	-20
Dual 2 NAND Driver	**54H/74H40**	Any TTL	60	-40
Dual 2 NAND Driver	**54S/74S40**	Any TTL	60	-50
Dual 2 NAND Driver (50 Ω)	**54S/74S140**	Any TTL	60	-50
Octal Inverting Bus Driver (3S*)	**54LS/74LS240**	Any TTL	64	-40
Octal Inverting Bus Driver (3S*)	**54S/74S240**	Any TTL	64	-50
Octal Non-Inverting Bus Driver (3S*)	**54LS/74LS241**	Any TTL	64	-40
Octal Non-Inverting Bus Driver (3S*)	**54S/74S241**	Any TTL	64	-50
Octal Bus Transceiver	**54LS/74LS245**	Any TTL	24	-40
Octal Inverting Bus Transceiver	**54LS/74LS540**	Any TTL	64	-40
Octal Non-Inverting Bus Transceiver	**54LS/74LS541**	Any TTL	64	-40
Quad Inverting Bus Transceiver	**54LS/74LS242**	Any TTL	24	-40
Quad Non-Inverting Bus Transceiver	**54LS/74LS243**	Any TTL	24	-40
Quad Bus Transceiver	**96103**	96103	70	-18
Quad 2-NOR Receiver	**96106**		7.8	-18

*OC = Open-Collector; 3S = 3-State

DISPLAY DECODER/DRIVERS

FUNCTION	DEVICE NO.	OUTPUT CURRENT mA	OUTPUT VOLTAGE V	ACTIVE HIGH/LOW	RIPPLE BLANKING	BLANKING ABOVE BCD 9-INPUT
1-of-10 Cold Cathode (OC*)	**9315 (54/7441)**	7.0	55	L		
1-of-10 Cold Cathode	**74141**	7.0	55	L		X
1-of-10 Driver (OC*)	**9302**	16	5.5	L		X
1-of-10 Driver (OC*)	**54/7445**	80	30	L		X
1-of-10 Driver (OC*)	**54/74145**	80	15	L		X
7-Seg Decoder	**9307**	12.5	5.5	H	X	
7-Seg Decoder	**54/7448**	1.3	5.5	H	X	
7-Seg Decoder (OC*)	**54/7449**	10	5.5	H	X	
7-Seg Decoder/Driver	**9317B**	40	20	L	X	X
7-Seg Decoder/Driver	**9317C**	20	30	L	X	X
7-Seg Decoder/Driver (OC*)	**54/7446A**	40	30	L	X	
7-Seg Decoder/Driver (OC*)	**54/7447A**	40	15	L	X	
7-Seg Decoder/Driver (OC*)	**54LS/74LS47**	24	15	L	X	
7-Seg Decoder/Driver	**54LS/74LS48**	1.3	5.5	H	X	
7-Seg Decoder/Driver (OC*)	**54LS/74LS49**	8.0	5.5	H	X	
7-Seg Decoder/Driver (OC*)	**54LS/74LS247**	24	15	L	X	
7-Seg Decoder/Driver	**54LS/74LS248**	1.3	5.5	H	X	
7-Seg Decoder/Driver (OC*)	**54LS/74LS249**	8.0	5.5	H	X	
7-Seg Decoder/Driver (OC*)	**54LS/74LS347**	24	7.0	L	X	
7-Seg Decoder/Driver (OC*)	**54LS/74LS447**	24	7.0	L	X	
7-Seg LED Driver Common Cathode	**9368**	20	1.7	H	X	
7-Seg LED Driver Common Anode (OC*)	**9370**	25	5.5	L	X	
7-Seg LED Driver Common Anode (OC*)	**9374**	15	10	L	X	

*OC = Open-Collector

ARITHMETIC OPERATORS

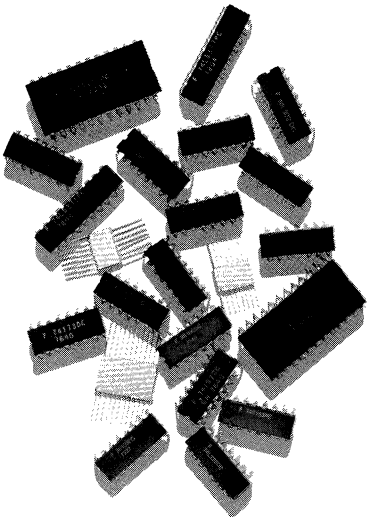
FUNCTION	DEVICE NO.	DESCRIPTION	NO. OF BITS
Adder	**54/7480**	Gated 1-Bit with Carry	1
Adder	**9304**	Dual 1-Bit with Carry	2
Adder	**54H/74H183**	Dual 1-Bit with Carry	2
Adder	**54/7482**	Full 2-Bit with Carry	2
Adder	**54/7483A**	Full Binary 4-Bit with Carry	4
Adder	**54LS/74LS83A**	Full Binary 4-Bit with Carry	4
Adder	**54/74283**	Full Binary 4-Bit with Carry	4
Adder	**54LS/74LS283**	Full Binary 4-Bit with Carry	4
Arithmetic Logic Unit	**9340**	ALU with Internal CLA*	4
Arithmetic Logic Unit	**9341 (54/74181)**	ALU with External CLA*	4
Arithmetic Logic Unit	**93L41**	ALU with External CLA*	4
Arithmetic Logic Unit	**54LS/74LS181**	ALU with External CLA*	4
Arithmetic Logic Unit	**93S41**	ALU with External CLA*	4
Carry Lookahead	**9342 (54/74182)**	CLA generator for 9341	
Carry Lookahead	**93S42 (54S/74S182)**	CLA generator for 93S41/9405	
Comparator	**9386 (8242)**	4-Bit Indentity Exclusive-NOR (OC*)	4
Comparator	**54/7485**	4-Bit Magnitude with Expander	4
Comparator	**54LS/74LS85**	4-Bit Magnitude with Expander	4
Comparator	**9324**	5-Bit Magnitude	5
Comparator	**93L24**	5-Bit Magnitude	5
Comparator	**93S46**	6-Bit Identity with Expander	6
Comparator	**93S47**	6-Bit Identity (OC*)	6
Encoder	**9318**	Priority 8-Bit with Expander	8
Encoder	**93L18**	Priority 8-Bit with Expander	8
Multiplier	**9344**	Binary 4 X 2-Bit	4 X 2
Multiplier	**93S43**	2s Complement	4 X 2
Multiplier	**54LS/74LS384**	Serial/Parallel 2s Complement	8
Parity	**54/74180**	8-Bit Parity Generator/Checker	8
Parity	**93S62**	9-Bit Parity Generator/Checker	9
Parity	**9348**	12-Bit Parity Generator/Checker	12
Parity	**54LS/74LS280**	9-Bit Parity Generator/Checker	9
True/Complement	**54H/74H87**	4-Bit True/Complement Zero/One Element	4
True/Complement	**54S/74S135**	Dual 2-Bit Exclusive OR/NOR	4

*CLA = Carry Lookahead; OC = Open-Collector

RANDOM ACCESS MEMORIES

ORGANIZATION	DEVICE NO.	DESCRIPTION	ADDRESS ACCESS TIME-ns (MAX) MIL/COM	CHIP SELECT ACCESS TIME-ns (MAX) MIL/COM	READ/WRITE CYCLE TIME	
					COM	MIL
					0°C to +70°C ns (MAX)	-55°C to +125°C ns (MAX)
TTL						
16 X 4	**7489**	OC[1]	60/60	50/50	115	115
SCHOTTKY						
16 X 4	**54S/74S189**	3S[1]	50/35	32/22	55	70
16 X 4	**54S/74S289**	OC[1]	50/35	25/17	55	70
LOW POWER SCHOTTKY						
16 X 4	**54LS/74LS89**	OC[1]	37/37[2]	10/10[2]	72[2]	72[2]
16 X 4	**54LS/74LS189**	3S[1]	37/37[2]	10/10[2]	72[2]	72[2]
16 X 4	**54LS/74LS289**	OC[1]	37/37[2]	10/10[2]	72[2]	72[2]

1. OC = Open-Collector; 3S = 3-State
2. Typical Value



SECTION 2

- Glossary
- Logic Symbols and Terminology
- TTL Circuit Families
- Input Characteristics
- Unused Inputs
- Output Characteristics
- Increasing Fan-Out
- 3-State Outputs
- Open-Collector Outputs
- Thresholds and Noise Margins
- Crosstalk
- Transmission Lines
- Transmission Line Effects
- Backplane Data Bus
- Decoupling
- Grounds
- Supply Voltage and Temperature
- Interfacing

Section 2
TTL CHARACTERISTICS

GLOSSARY

Currents — Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

I_{CC} **Supply Current** — The current flowing into the V_{CC} supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst case operation.

I_{IH} **Input HIGH Current** — The current flowing into an input when a specified HIGH voltage is applied.

I_{IL} **Input LOW Current** — The current flowing out of an input when a specified LOW voltage is applied.

I_{OH} **Output HIGH Current** — The leakage current flowing into a turned off open-collector output with a specified HIGH output voltage applied. For an output with an internal pull-up circuit, the I_{OH} is the current flowing out of the output when it is in the HIGH state.

I_{OL} **Output LOW Current** — The current flowing into an output when it is in the LOW state.

I_{OS} **Output Short Circuit Current** — The current flowing out of a HIGH-state output when that output is short circuited to ground (or other specified potential).

I_{OZH} **Output OFF Current HIGH** — The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.

I_{OZL} **Output OFF Current LOW** — The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.

Voltages — All voltages are referenced to the ground pin. Negative voltage limits are specified as absolute values (i.e., -10 V is greater than -1.0 V).

V_{CC} **Supply Voltage** — The range of power supply voltage over which the device is guaranteed to operate within the specified limits.

$V_{CD(Max)}$ **Input Clamp Diode Voltage** — The most negative voltage at an input when a specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode, intended to clamp negative ringing at the input terminal.

V_{IH} **Input HIGH Voltage** — The range of input voltages that represents a logic HIGH in the system.

$V_{IH(Min)}$ **Minimum Input HIGH Voltage** — The minimum allowed input HIGH in a logic system. This value represents the guaranteed input HIGH threshold for the device.

V_{IL} **Input LOW Voltage** — The range of input voltages that represents a logic LOW in the system.

$V_{IL(Max)}$ **Maximum Input LOW Voltage** — The maximum allowed input LOW in a system. This value represents the guaranteed input LOW threshold for the device.

GLOSSARY (Cont'd)

$V_{OH(Min)}$ **Output HIGH Voltage** — The minimum voltage at an output terminal for the specified output current I_{OH} and at the minimum value of V_{CC}.

$V_{OL(Max)}$ **Output LOW Voltage** — The maximum voltage at an output terminal sinking the maximum specified load current I_{OL}.

V_{T+} **Positive-Going Threshold Voltage** — The input voltage of a variable threshold device (i.e., Schmitt Trigger) that is interpreted as a V_{IH} as the input transition rises from below $V_{T-(Min)}$.

V_{T-} **Negative-Going Threshold Voltage** — The input voltage of a variable threshold device (i.e., Schmitt Trigger) that is interpreted as a V_{IL} as the input transition falls from above $V_{T+(Max)}$.

AC Switching Parameters

f_{max} **Toggle Frequency/Operating Frequency** — The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

t_{PLH} **Propagation Delay Time** — The time between the specified reference points, normally 1.5 V (1.3 V for LS) on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} **Propagation Delay Time** — The time between the specified reference points, normally 1.5 V (1.3 V for LS) on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

t_w **Pulse Width** — The time between 1.5 V (1.3 V for LS) amplitude points on the leading and trailing edges of a pulse.

t_h **Hold Time** — The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s **Setup Time** — The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} **Output Disable Time (of a 3-State Output) from HIGH Level** — The time between the 1.5 V (1.3 V for LS) level on the input and a voltage 0.5 V below the steady state output HIGH level with the 3-state output changing from the defined HIGH level to a high impedance (off) state.

t_{PLZ} **Output Disable Time (of a 3-State Output) from LOW Level** — The time between the 1.5 V (1.3 V for LS) level on the input and a voltage 0.5 V above the steady state output LOW level with the 3-state output changing from the defined LOW level to a high impedance (off) state.

t_{PZH} **Output Enable Time (of a 3-State Output) to a HIGH Level** — The time between the 1.5 V (1.3 V for LS) levels of the input and output voltage waveforms with the 3-state output changing from a high impedance (off) state to a HIGH level.

GLOSSARY (Cont'd)

t_{PZL} **Output Enable Time (of a 3-State Output) to a LOW Level** — The time between the 1.5 V (1.3 V for LS) levels of the input and output voltage waveforms with the 3-state output changing from a high impedance (off) state to a LOW level.

t_{rec} **Recovery Time** — The time between the 1.5 V (1.3 V for LS) level on the trailing edge of an asynchronous input control pulse and the same level on a synchronous input (clock) pulse such that the device will respond to the synchronous input.

Miscellaneous

C Marking code letter indicating that the device is guaranteed to meet the specifications for the Commercial temperature range.

D Package code letter for ceramic Dual In-line Packages.

F Package code letter for ceramic flatpaks.

M Marking code letter indicating that the device is guaranteed to meet the specifications for the Military temperature range.

P Package code letter for plastic Dual In-line Packages.

QB Marking code indicating in-house 38510, level B reliability screening (military grade only).

QM, QR Marking code indicating Matrix VI commercial/industrial reliability screening.

XC, XM Shorthand for the commercial or military temperature range specifications or devices; the letter X stands for the code letter of any package in which the device is available.

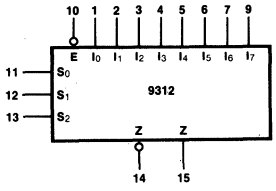
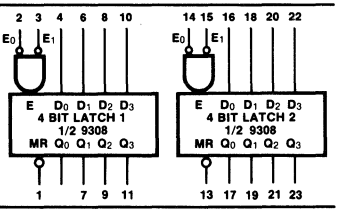
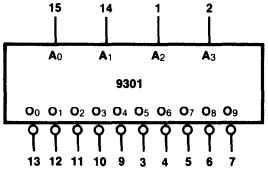
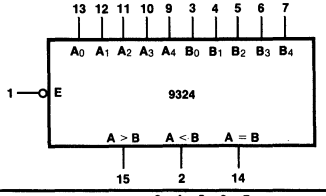
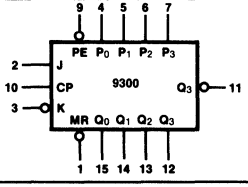
LOGIC SYMBOLS AND TERMINOLOGY

The logic symbols used to represent the MSI devices follow Mil Std 806B for logic symbols. MSI elements are represented by rectangular blocks with appropriate external AND/OR gates when necessary. A small circle at an external input means that the specific input is active LOW; i.e., it produces the desired function, in conjunction with other inputs, if its voltage is the lower of the two logic levels in the system. A circle at the output indicates that when the function designated is True, the output is LOW. Generally, inputs are at the top and left and outputs appear at the bottom and right of the logic symbol. An exception is the asynchronous Master Reset in some sequential circuits which is always at the left hand bottom corner.

Inputs and outputs are labeled with mnemonic letters as illustrated in *Table 2-1*. Note that an active LOW function labeled outside of the logic symbol is given a bar over the label, while the same function inside the symbol is labeled without the bar. When several inputs or outputs use the same letter, subscript numbers starting with zero are used in an order natural for device operation.

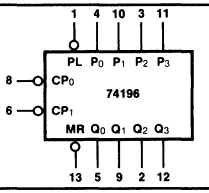
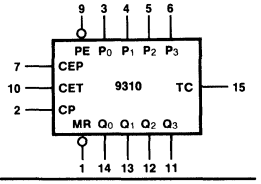
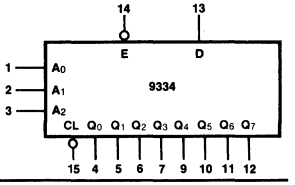
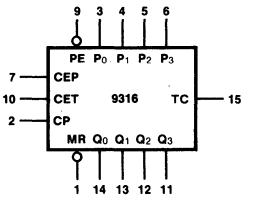
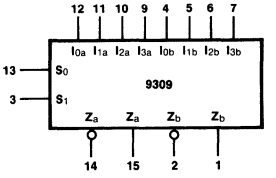
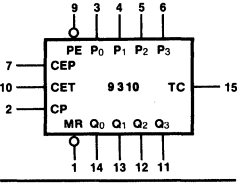
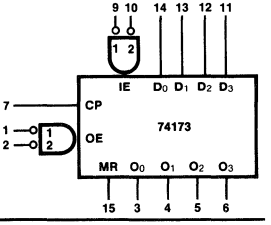
This nomenclature is used throughout this book and may differ from nomenclature used on other data books (notably early 7400 MSI), where outputs use alphabetic subscripts or use number sequences starting with one.

TABLE 2-1

LABEL	MEANING	EXAMPLE
Ix	General term for inputs to combinatorial circuits.	
J, K S, R D	Inputs to JK, SR, and D flip-flops and latches.	
Ax, Sx	Address or Select inputs, used to select an input, output, data route, junction, or memory location.	
$\overline{E}$	Enable, active LOW on all TTL/MSI. A latch can receive new data when its Enable input is in the active state.	
$\overline{PE}$ P	Parallel Enable, a control input used to synchronously load information in parallel into an otherwise autonomous circuit. Parallel data inputs to shift registers and counters.	

LOGIC SYMBOLS AND TERMINOLOGY (Cont'd)

TABLE 2-1 (Cont'd)

LABEL	MEANING	EXAMPLE
$\overline{PL}$	Parallel Load; similar to Parallel Enable except that $\overline{PL}$ overrides the clock and forces parallel loading asynchronously.	
$\overline{MR}$	Master Reset, asynchronously resets all outputs to zero, overriding all other inputs.	
$\overline{CL}$	Clear, resets outputs to zero but does not override all other inputs.	
CP CE, CEP, CET	Clock Pulse, generally a HIGH-to-LOW-to-HIGH transition. An active HIGH clock (no circle) means outputs change on LOW-to-HIGH clock transition. Count Enable inputs for counters.	
Zx, Ox, Fx	General terms for outputs of combinatorial circuits.	
Qx TC	General term for latch and flip-flop outputs. If they pass through an enable gate before exiting the package, Q or $\overline{Q}$ changes to O or $\overline{O}$. Terminal Count output (1111 for up binary counters, 1001 for up decimal counters, or 0000 for down counters).	
$\overline{OE}$	Output Enable, used to force 3-state outputs into the high impeddance state.	

TTL CIRCUIT FAMILIES

Each family is designed around certain performance objectives, within the economic limitations of a particular process. The key performance factors that distinguish the families are power consumption, speed and the ability to drive wiring capacitance. For comparison purposes the power supply current and propagation delay or switching rate for several popular circuit types in the various families are shown in *Table 2-2* below. The propagation delays are in ns, the supply currents in mA and the toggle frequencies in MHz. All values listed are worst-case guaranteed, rather than typical figures.

TABLE 2-2

CIRCUIT TYPE		TTL	H-TTL	S-TTL	LP-TTL	LS-TTL
2-Input NAND	t_{PLH}/t_{PHL}	22/15	10/10	4.5/5.0		10/10
7400	I_{CC}	2.0/5.5	4.2/10	4.0/9.0		0.4/1.1
D-Type Flip-Flop	f_{max}	15	35	75		30
7474	I_{CC}	7.0	38	25		4.0
JK Flip-flop	f_{max}	25	40	80		30
9024/74112/74H108	I_{CC}	7.0	38	25		4.0
4-Input Multiplexer	t_{PLH}/t_{PHL}	14/14		7.5/6.5	22/30	14/14
9322/74157	I_{CC}	23.5		39	6.6	8.0
Synchronous Counter	f_{max}	30		70	13	25
9310/74160	I_{CC}	92		127	27.5	32
4-Bit Shift Register	f_{max}	30	45	70	10	30
9300/74195	I_{CC}	63	112	120	23	21

In three of the families — TTL, H-TTL and LP-TTL — the transistors are turned on by applying sufficient base current for the lowest expected current gain. The average transistor, having greater current gain, receives far more base current than necessary, which forward biases the collector-base junction and saturates the transistor. In order to turn off such a saturated transistor, the excess base charge must first be removed, resulting in considerable delay. Gold doping is commonly used to speed up the charge recombination, but this decreases the current gain.

Schottky clamped transistors *(Figure 2-1)* overcome this limitation. They use a surface barrier diode with very low forward voltage drop (0.3 V) as a bypass between base and collector. When the transistor starts conducting and is about to become saturated, the excess input current is not fed into the base, but routed through the Schottky diode into the collector (Baker Clamp). As a result the transistor is never fully saturated and recovers quickly when the base current is interrupted. Since gold doping is not required, the transistors also have higher current gain, require less base current, and turn on faster.

As a result of the faster turn-on and recovery, S-TTL circuits achieve roughly twice the speed of H-TTL at about the same level of power consumption, as indicated in the table. On the other hand, LS-TTL circuits (also Schottky clamped) use much less power than H-TTL, yet operate at about the same speed. Compared to S-TTL, LS-TTL processing produces shallower diffusions and smaller transistors with greater bandwidth. Thus, LS-TTL circuits operate at about half the speed of S-TTL while using only about 20% as much power.

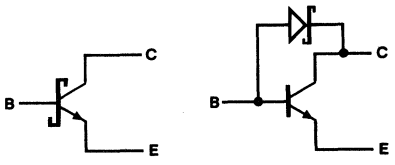


Fig. 2-1 Schottky Transistor

TTL CIRCUIT FAMILIES (Cont'd)

Schematics of the basic gates of the various families are shown in *Figures 2-2* through *2-7*. All are similar, containing an input AND gate, a phase splitter Q2 with emitter and collector load resistors, a pull-up mechanism Q3/Q4 and a pull-down transistor Q5. In all except the LS-TTL circuit, the AND function is formed by a multi-emitter transistor in which the emitter-base junctions serve to isolate the input signal sources from each other and steer the current from the 4 kΩ gate resistor. When an input is LOW, the gate current flows out through the base-emitter junction and Q1 is saturated, making the base voltage of Q2 only slightly more positive than the LOW input voltage, and Q2 does not conduct. Moreover, the low emitter-to-collector resistance of Q1 in this condition allows the input signal source to withdraw charge from the base of Q2 and help to turn it off quickly. With all inputs HIGH, the gate current flows through the base-collector junction of Q1 and turns on Q2. In this situation, a small quantity of charge is injected into the base of Q1. Part of this charge recombines in the base region and part of it drifts over to be "collected" by the emitters. This inverse beta current is a significant part of the input leakage current I_{IH}. This same phenomenon occurs when the gate current exits through a LOW input. Current is injected into the base from the LOW emitter and part of it is collected by the HIGH emitters. An input signal exceeding the +5.5 V rating applied to one input can cause breakdown between it and a LOW input, with the possibility of damage or of being biased in a negative resistance region, depending on the source impedance. Biasing in the negative resistance region can lead to oscillation that is difficult to diagnose.

The phase splitter Q2 is so named because the collector and emitter voltages change in opposite directions when Q2 turns on or off. When Q2 turns off, the emitter voltage falls and it stops providing base current to the pull-down transistor Q5; simultaneously the Q2 collector voltage rises and pulls up the base of Q3. The Q3/Q4 circuitry provides current gain and the low impedance necessary to pull the output up to the HIGH level while charging wiring capacitance. The amount of current available to charge capacitance is limited by the small resistor(s) connected from V_{CC} to the collector(s) of Q3/Q4. This charging current shows up as a current spike at the V_{CC} pin and it is normal practice to add rf bypass capacitors on logic boards to supply this sudden demand for current and thus prevent negative-going spikes on V_{CC}.

When Q2 turns on, the collector voltage falls and pulls down the base of Q3; simultaneously Q2 emitter voltage rises and supplies base current to Q5. As Q5 starts conducting, it begins to discharge load capacitance and pull the output down to the LOW level. The discharge current shows up as a current spike at the ground pin and is one of the principal reasons for recommending that system designers allow generous amounts of ground metal on circuit boards.

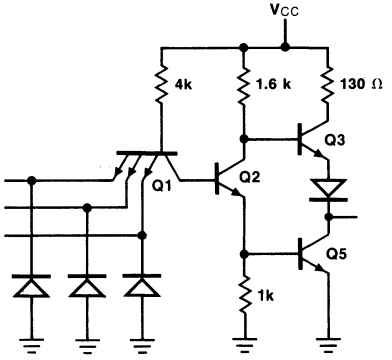


Fig. 2-2 7410 Gate

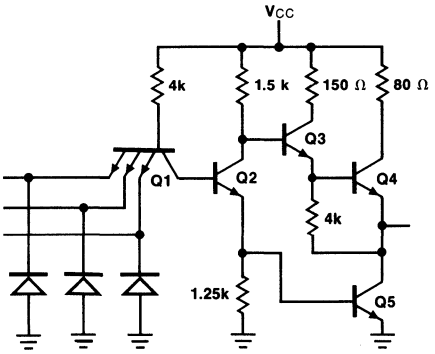


Fig. 2-3 9003 Gate

TTL CIRCUIT FAMILIES (Cont'd)

Although Fairchild does not offer LP-TTL gates or flip-flops, the input and output circuitry of *Figure 2-4* is representative of 93L Series MSI. As shown, the resistor values are four times those of *Figures 2-2* and *2-3*. This decreases the input loading I_{IL}, the output drive capability and the power consumption. The speed-power trade-off is evident from the values listed in the table for the LP-TTL multiplexer, counter and shift register, compared to the TTL counterparts.

Another speed-power trade-off is evident in the H-TTL gate of *Figure 2-5*. Compared to *Figure 2-2*, several resistor values are halved and the output pull-up changed to a Darlington configuration. As seen from the values listed in the table, both speed and power consumption are approximately doubled.

The S-TTL gate of *Figure 2-6* is quite similar to the H-TTL gate and consumes about the same amount of power, yet operates at twice the speed. The base of the pull-down output transistor Q5 is returned to ground through Q6 and a pair of resistors instead of through a simple resistor. This arrangement is called a squaring network since it squares up the transfer characteristics by preventing conduction in the phase splitter Q2 until the input voltage rises high enough to allow Q2 to supply base current to Q5. The squaring network also improves the propagation delay by providing a low resistance path to discharge capacitance at the base of Q5 during turn-off.

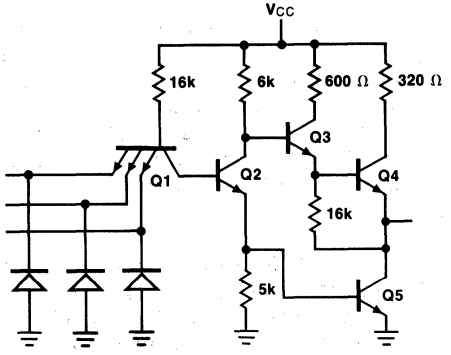


Fig. 2-4 LP-TTL Gate

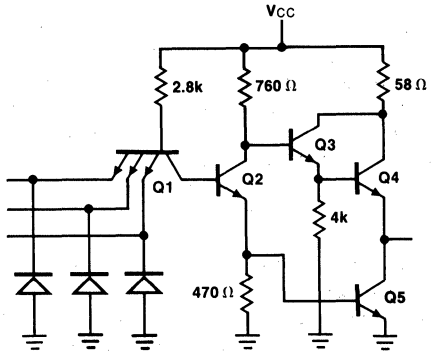


Fig. 2-5 74H10 Gate

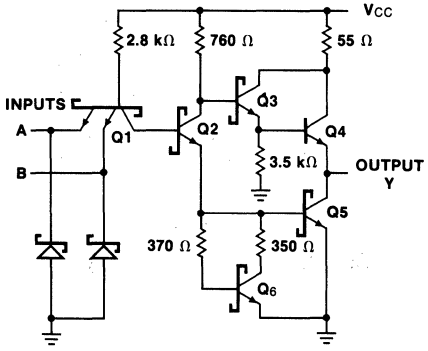


Fig. 2-6 74S00 Gate

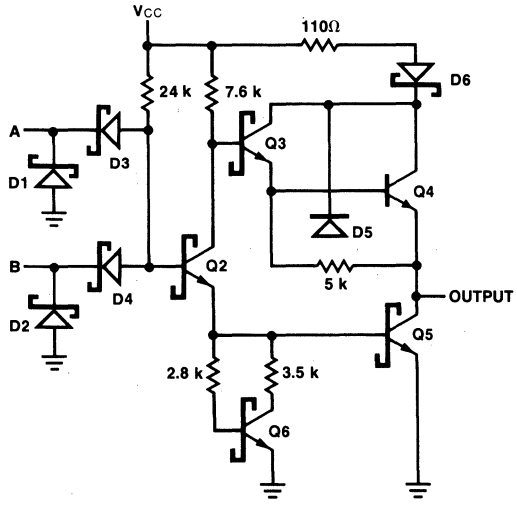


Fig. 2-7 74LS00 Gate

TTL CIRCUIT FAMILIES (Cont'd)

With a few exceptions, LS-TTL circuits do not use the multi-emitter input structure that originally gave TTL its name. Most LS elements use a DTL type input circuit with Schottky diodes to perform the AND function, as exemplified by D3 and D4 in *Figure 2-7*. Compared to the classical multi-emitter structure, this circuit is faster and it increases the input breakdown voltage. Inputs of this type are tested for leakage with an applied input voltage of 10V, and the input breakdown voltage is guaranteed to be 15 V or more.

Another input arrangement often used in LS-TTL MSI has three diodes connected as shown in *Figure 2-8*. This configuration gives a slightly higher input threshold than that of *Figure 2-7*. A third input configuration sometimes used employs a vertical pnp transistor as shown in *Figure 2-9*. This arrangement also gives a higher input threshold and has the additional advantage of reducing the amount of current that the signal source must sink. Both the diode cluster arrangement and the pnp input configuration have breakdown voltage ratings greater than 15 V.

A few LS-TTL circuits use the traditional emitter inputs and thus have input breakdown ratings of 5.5 V. These circuits are the open-collector gate types 'LS03, 'LS05, 'LS22, 'LS26 and 'LS136; flip-flop types 'LS74, 'LS109, 'LS112, 'LS113 and 'LS114; and the clock inputs of ripple counter types 'LS90, 'LS92, 'LS93, 'LS196, 'LS197, 'LS290, 'LS293, 'LS390, 'LS393 and 'LS490.

The LS-TTL pull-up circuitry has some features not found in the other TTL circuits. The 5 kΩ resistor bridging the base-emitter junction of Q4 is diffused into the same isolation region as the Q4/Q5 collectors, thus the sneak diode D5 does not return to V_{CC} as it does in other diffused resistors. This feature, in conjunction with the blocking diode D6, allows a HIGH state output to be pulled up higher than V_{CC}, e.g., to +10 V, convenient for interfacing with CMOS. Some early FSC LS designs — the 'LS00, 'LS02, 'LS04, 'LS10, 'LS11, 'LS20, 'LS32, 'LS74, 'LS86, 'LS109, 'LS112, 'LS113 and 'LS114 — do not have the diode in series with the Darlington collector resistor. These outputs are, therefore, clamped one diode drop above the positive supply voltage V_{CC}.

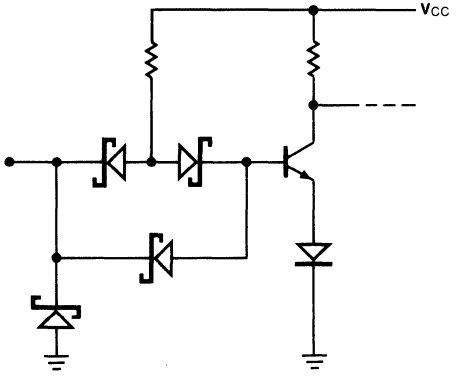


Fig. 2-8 Diode Cluster Input

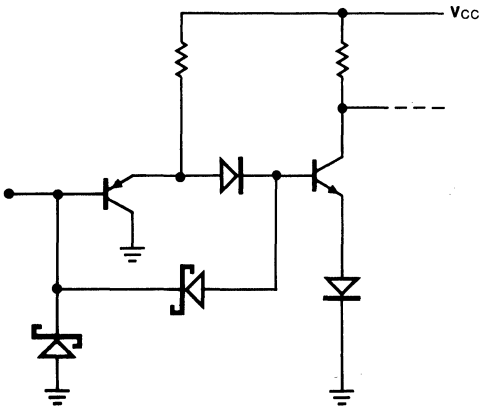


Fig. 2-9 PNP Input

INPUT CHARACTERISTICS

Figure 2-10 shows the input current-voltage characteristics of a TTL buffer. For input voltage levels around 6.0 V the emitter inputs avalanche. In this condition an input has very low series resistance and the avalanche current increases rapidly with input voltage. To avoid permanent damage, the input signal source must have either a current limit of 5.0 mA or less, or the input voltage must be limited to 5.5 V. For input voltages between 2.0 V and 5.5 V, the current flow is only the input leakage current I_{IH}, guaranteed not to exceed 40 μA or 50 μA, depending on the circuit family, for a single input. As the input voltage decreases below 2.0 V, current starts flowing from the input and increases rapidly as the voltage decreases. The slope of the characteristics in this region is only about 200 Ω, indicating that part of the current from the gate pull-up resistor is still flowing inward through the internal junctions of the circuit. This marks the transition region, since at some point the buffer pull-down transistor will not have sufficient base current to stay on and the output will start to switch from LOW to HIGH.

As the input voltage decreases from about 1.0 V to -0.5 V, the slope of the characteristic equals the gate pull-up resistor, in this case about 2 kΩ. As the input goes below about -0.7 V the current increases rapidly as the input clamping diode conducts.

Figure 2-11 shows the input characteristic of an LS-TTL circuit. Input diode breakdown is typically greater than 15 V and input leakage current above 1.5 V is negligible. As the input voltage falls below 1.3 V, gate current starts flowing out of the input, denoting the transition region. For input voltage between 1.0 V and -0.3 V, the I-V characteristic has the slope of the 24 kΩ gate pull-up resistor. The clamping diode conducts and the current increases rapidly when the input voltage goes below about -0.3 V. The LS-TTL clamping diodes are intended only for the suppression of transient currents and should not be used as steady-state clamps in interface applications. A clamp current exceeding 2.0 mA and with a duration greater than 500 ns can activate a parasitic lateral npn transistor, which in turn can steal current from internal nodes of the LS circuit and thus cause logic errors. The effective capacitance of a TTL input is 5.0 pF for DIP and 4.0 pF for Flatpak. For an input that serves more than one internal function, each additional function adds 1.5 pF.

In the 9000 series, the input leakage I_{IH} is measured at a reverse bias of 4.5 V, as opposed to 2.4 V for the other families. This is a more severe test and a standard 9000 series input has a limit of 60 μA. At the more conventional bias of 2.4 V, the leakage will not exceed 40 μA under most operating conditions.

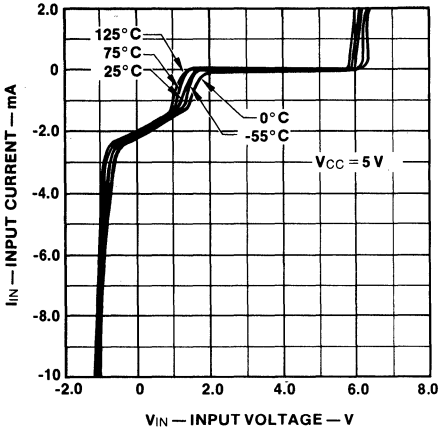


Fig. 2-10 TTL Buffer Input Characteristics

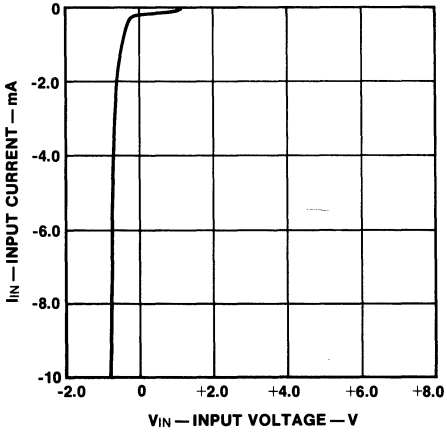


Fig. 2-11 LS-TTL Input Characteristics

UNUSED INPUTS

Theoretically, an unconnected input assumes the HIGH logic level, but practically speaking it is in an undefined logic state because it tends to act as an antenna for noise. Only a few hundred millivolts of noise causes the unconnected input to go to the logic LOW state. On devices with memory (flip-flops, latches, registers, counters), it is particularly important to terminate unused inputs (MR, PE, PL, CP) properly since a noise spike on these inputs might change the contents of the memory. It is poor design practice to leave unused inputs floating.

If the logic function calls for a LOW input, such as in NOR or OR gates, ground the unused inputs. For a permanent HIGH signal, unused inputs can be tied to V_{CC}. A current limiting resistor, in the range of 1 kΩ to 5 kΩ, is recommended for emitter-type inputs since these break down at some unspecified voltage above 5.5 V and power supply misadjustment or malfunction can cause damage unless the current is limited. Note that one resistor can serve several inputs, provided only that the cumulative I_{IH} current does not cause the voltage to drop below 2.4 V. Note also that diode-type LS-TTL inputs have breakdown voltages above 15 V and thus protective resistors are not normally required. An unused input may also be tied to a used input having the same logic function, such as NAND or AND gates, provided that the driver can handle the added I_{IH}. This practice is not recommended for diode-type LS-TTL inputs in a noisy environment, since each diode represents a small capacitor and two or more in parallel can act as an entry port for negative spikes superimposed on a HIGH level and cause momentary turn-off of Q2 *(Figure 2-7)*.

OUTPUT CHARACTERISTICS

Figure 2-12 shows the LOW state output characteristics of a 5400 gate at three temperatures. With no load current the output level is the offset voltage of about 90 mV. The slope of the 25° C characteristic indicates a saturation resistance of 8 Ω, increasing to 9 Ω at 125° C and decreasing to 6 Ω at -55° C. At low temperature, transistor beta decreases such that the output transistor pulls out of saturation for currents above 25 mA. Not shown is the effect of the collector-substrate junction for negative output currents. In some cases a negative output current can occur as a reflection from the unterminated end of a long interconnection following a HIGH-to-LOW transition. The collector-substrate diode acts as a negative current clamp and limits the undershoot to the -0.7 V to -1.0 V range, depending on the current.

Figure 2-13 shows the LOW state output characteristics of an LS-TTL gate. For LOW I_{OL} values, the pull-down transistor is clamped out of deep saturation to shorten the turn-off delay. The curves also show the clamping effect when I_{OL} tends to go negative. In S-TTL and LS-TTL circuits, the anti-saturation clamping of Q5 means that the output LOW voltage will be slightly higher than for the equivalent saturated circuits at the same current levels. For example, both the 74S00 and 74H00 are guaranteed to sink 20 mA (12.5 unit loads) but the V_{OL} specifications are 0.5 V and 0.4 V, respectively. Similarly, standard 93L and 74LS circuits are guaranteed to sink 8.0 mA (5 unit loads) but the V_{OL} specifications are 0.4 V and 0.5 V respectively.

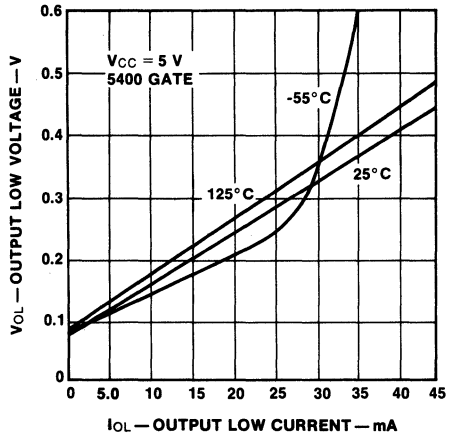


Fig. 2-12 TTL Gate Output LOW Characteristics

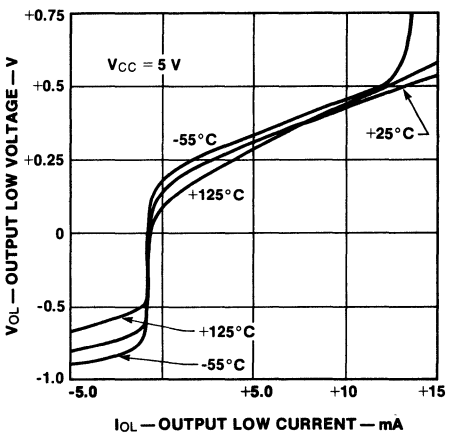


Fig. 2-13 LS-TTL Gate Output LOW Characteristics

OUTPUT CHARACTERISTICS (Cont'd)

In the HIGH state a totem-pole output presents a low impedance and is capable of sourcing considerable current. *Figure 2-14* shows the output HIGH characteristics of a 5400 gate at three temperatures. With no load current the V_{OH} is about 3.5 V at 25° C. For I_{OH} increasing to about 6.0 mA, the characteristic has the shape of a fixed voltage minus the logarithmically increasing voltage drop across two pn junctions. For I_{OH} greater than 6.0 mA, the pull-up transistor Q3 *(Figure 2-2)* saturates and the slope of the characteristic is just the 130 Ω current limiting resistor plus the saturation resistance of Q3. The maximum I_{OH} current, where the characteristic intersects the horizontal axis, correlates with the short-circuit output current parameter I_{OS} and is often regarded as a measure of the circuit's ability to charge line capacitance.

The output HIGH characteristics of the 54S140 Line Driver are shown in *Figure 2-15*, with the axes oriented differently than in *Figure 2-13*. The 'S140 pull-up is a Darlington circuit with a 25 Ω collector resistor to limit the short-circuit output current. This low resistance allows the 'S140 to source very large values of I_{OH}, as suggested by the graph. The 'S140 is guaranteed to force a 2.0 V signal across a 50 Ω load to ground, making it an attractive circuit for driving long interconnections that must be treated as transmission lines.

Figure 2-16 shows the 54LS00 output HIGH characteristic, which is quite similar to the 5400 gate of *Figure 2-14*. Due to the 5.0 kΩ resistor from Q3 to output *(Figure 2-7)* the LS circuits provide higher output voltage for low values of I_{OH}, as shown in *Figure 2-17*. This provides greater protection against negative-going noise on a quiescent HIGH signal.

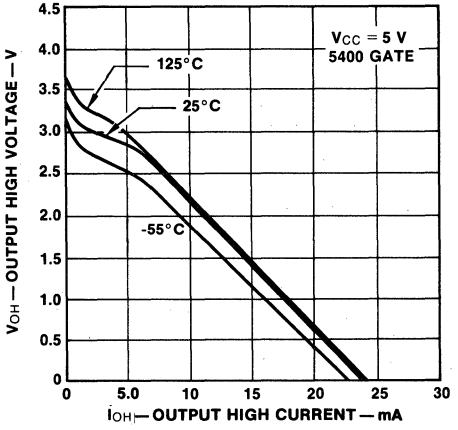


Fig. 2-14 TTL Output HIGH Characteristics

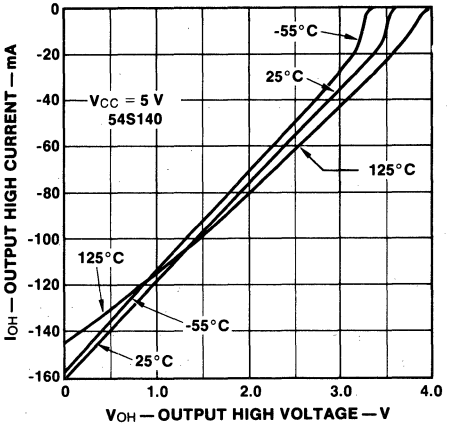


Fig. 2-15 S-TTL Line Driver Output HIGH Characteristics

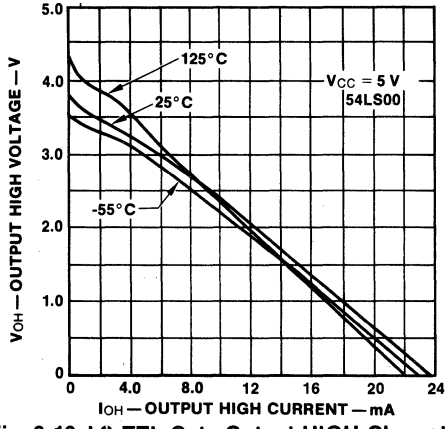


Fig. 2-16 LS-TTL Gate Output HIGH Characteristics

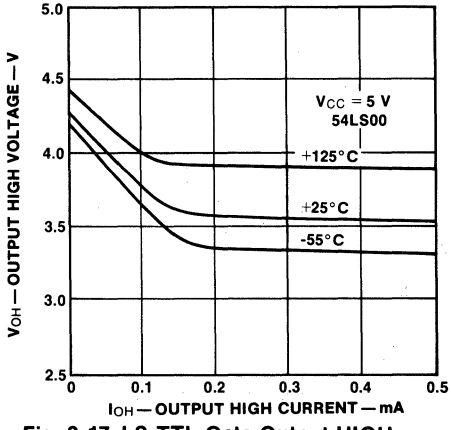


Fig. 2-17 LS-TTL Gate Output HIGH Characteristics at Low Loading

INCREASING FAN OUT

To increase fan-out, inputs and outputs of gates on the same package may be paralleled. It is advisable to limit the gates being paralleled to those in a single package to avoid large transient supply currents due to different switching times of the gates. This is not detrimental to the devices, but could cause logic problems if the gates are being used as clock drivers.

3-STATE OUTPUTS

In the newer TTL families there are many circuits that have an auxilliary control input whereby both the output pull-up and pull-down circuitry can be disabled. This condition is called the high impedance (high-Z) state and allows the outputs of different circuits to be connected to a common line or data bus. A typical 3-state output, shown in *Figure 2-18*, has pull-up and pull-down circuitry quite similar to *Figure 2-7*. The significant difference is that the enable function is connected through a diode to the base of Q3. A LOW signal on the enable turns off both Q2 and Q3 and thus disables both the pull-up and pull-down circuitry. In this disabled condition the outputs are tested for leakage at 2.4 V (I_{OZH}) and at 0.4 V or 0.5 V (I_{OZL}) to ensure that they do not cause excessive loading on a data bus. When the circuit is in the bi-state mode, i.e., enabled, the output HIGH and LOW characteristics are the same as those of other circuit types having the same drive capabilities.

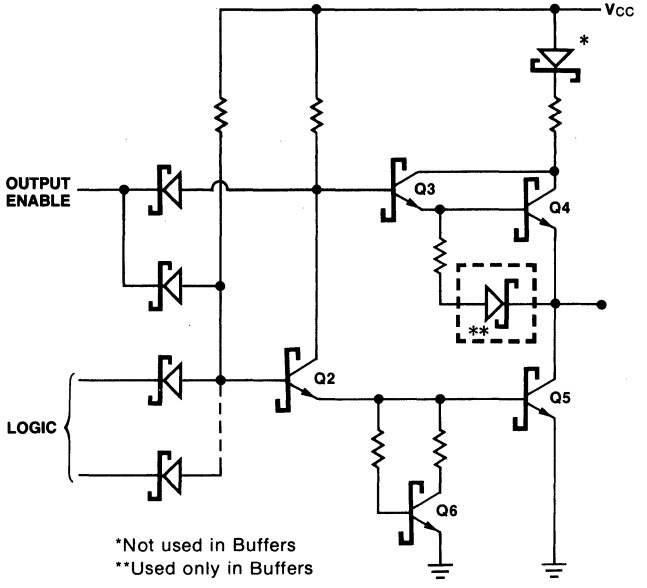


Fig. 2-18 Typical 3-State Output Control

OPEN-COLLECTOR OUTPUTS

A number of available circuits have no pull-up circuit on the outputs. Some are special purpose, such as the 74141 high voltage display driver, the 7445 high current display driver, the 9370 LED driver or the 96101 terminated bus driver. For circuits of this type, no external pull-up is necessary other than the intended load. Other open-collector circuits, less dedicated in nature, are used for interfacing or for wired-OR (actually wired-AND) functions. The latter is achieved by connecting open-collector outputs together and adding an external pull-up resistor.

The value of the pull-up resistor is determined by considering the fan-out of the OR tie and the number of devices in the OR tie. The pull-up resistor value is chosen from a range between maximum value (established to maintain the required V_{OH} with all the OR-tied outputs HIGH) and a minimum value (established so that the OR tie fan-out is not exceeded when only one output is LOW).

MINIMUM AND MAXIMUM PULL-UP RESISTOR VALUES

$$R_{X(Min)} = \left(\frac{V_{CC(Max)} - V_{OL}}{I_{OL} - N_2(LOW) \bullet 1.6\,mA} \right) \quad R_{X(Max)} = \left(\frac{V_{CC(Min)} - V_{OH}}{N_1 \bullet I_{OH} + N_2(HIGH) \bullet 40\,\mu A} \right)$$

where:	R_X	= External Pull-Up Resistor
	N_1	= Number of Wired-OR Outputs
	N_2	= Number of Input Unit Loads Being Driven
	$I_{OH} = I_{CEX}$	= Output HIGH Leakage Current
	I_{OL}	= LOW Level Fan-Out Current of Driving Element
	V_{OL}	= Output LOW Voltage Level (0.5 V)
	V_{OH}	= Output HIGH Voltage Level (2.4 V)
	V_{CC}	= Power Supply Voltage

Example: Four 74LS03 gate outputs driving four other LS gates or MSI inputs.

$$R_{X(Min)} = \left(\frac{5.25\,V - 0.5\,V}{8.0\,mA - 1.6\,mA} = \frac{4.75\,V}{6.4\,mA} \right) = 742\,\Omega$$

$$R_{X(Max)} = \left(\frac{4.75\,V - 2.4\,V}{4 \bullet 100\,\mu A + 2 \bullet 40\,\mu A} = \frac{2.35\,V}{0.48\,mA} \right) = 4.9\,k\Omega$$

where:	N_1	= 4
	$N_2(HIGH)$	= 4 • 0.5 U.L. = 2 U.L.
	$N_2(LOW)$	= 4 • 0.25 U.L. = 1 U.L.
	I_{OH}	= 100 μA
	I_{OL}	= 8.0 mA
	V_{OL}	= 0.5 V
	V_{OH}	= 2.4 V

Any value of pull-up resistor between 742 Ω and 4.9 Ω can be used. The lower values yield the fastest speeds while the higher values yield the lowest power dissipation.

THRESHOLDS AND NOISE MARGINS

The noise margins most often cited for TTL are obtained by subtracting the guaranteed maximum input HIGH level V_{IH} of a driven input from the guaranteed minimum output HIGH level V_{OH} of the driving source, and subtracting the guaranteed maximum output LOW level V_{OL} of the driver from the guaranteed minimum input LOW level V_{IL} of a driven circuit. The guaranteed worst-case values of these parameters vary slightly among the various circuit families and are summarized in *Table 2-3*. Note that although the 9000 Series V_{IH} and V_{IL} specifications have different limits at different temperatures (see data sheets), they are grouped with the 54/74 family in the table as a matter of convenience. Note also that the V_{OL} limit listed for 74LS is 0.5 V, whereas these circuits are also specified at 0.4 V at a lower level of I_{OL}. Noise margins obtained by the aforementioned subtractions are listed in *Tables 2-4* through *2-7*, for all combinations of driving and driven circuit types in the various circuit families. Noise margins calculated in this manner are quite conservative, since it is assumed that both the driver output characteristics and the receiver input characteristics are worst-case and that V_{CC} is on the low side for the driver and on the high side for the receiver.

Table 2-3 Parameter Limits

Fairchild TTL Families		Military (-55 to +125°C)				Commercial (0 to +70°C)				Units
		V_{IL}	V_{IH}	V_{OL}	V_{OH}	V_{IL}	V_{IH}	V_{OL}	V_{OH}	
TTL	Standard TTL, 9000, 54/74	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
H-TTL	High Speed TTL, 54H/74H	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
LP-TTL	Low Power TTL, 93L (MSI)	0.7	2.0	0.3	2.4	0.8	2.0	0.3	2.4	V
S-TTL	Schottky TTL, 54S/74S, 93S	0.8	2.0	0.5	2.5	0.8	2.0	0.5	2.7	V
LS-TTL	Low Power Schottky TTL, 54LS/74LS	0.7	2.0	0.4	2.5	0.8	2.0	0.5	2.7	V

V_{OL} and V_{OH} are the voltges generated at the output. V_{IL} and V_{IH} are the voltage required at the input to generate the appropriate levels. The numbers given above are guaranteed worst-case values.

Table 2-4 LOW Level Noise Margins (Military)

From \ To	TTL	H-TTL	LP-TTL	S-TTL	LS-TTL	Units
TTL	400	400	300	400	300	mV
H-TTL	400	400	300	400	300	mV
LP-TTL	500	500	400	500	400	mV
S-TTL	300	300	200	300	200	mV
LS-TTL	400	400	300	400	300	mV

From "V_{OL}" to "V_{IL}"

Table 2-5 HIGH Level Noise Margins (Military)

From \ To	TTL	H-TTL	LP-TTL	S-TTL	LS-TTL	Units
TTL	400	400	400	400	400	mV
H-TTL	400	400	400	400	400	mV
LP-TTL	400	400	400	400	400	mV
S-TTL	500	500	500	500	500	mV
LS-TTL	500	500	500	500	500	mV

From "V_{OH}" to "V_{IH}"

Table 2-6 LOW Level Noise Margins (Commercial)

From \ To	TTL	H-TTL	LP-TTL	S-TTL	LS-TTL	Units
TTL	400	400	400	400	400	mV
H-TTL	400	400	400	400	400	mV
LP-TTL	500	500	500	500	500	mV
S-TTL	300	300	300	300	300	mV
LS-TTL	300	300	300	300	300	mV

From "V_{OL}" to "V_{IL}"

Table 2-7 HIGH Level Noise Margins (Commercial)

From \ To	TTL	H-TTL	LP-TTL	S-TTL	LS-TTL	UNITS
TTL	400	400	400	400	400	mV
H-TTL	400	400	400	400	400	mV
LP-TTL	400	400	400	400	400	mV
S-TTL	700	700	700	700	700	mV
LS-TTL	700	700	700	700	700	mV

From "V_{OH}" to "V_{IH}"

THRESHOLDS AND NOISE MARGINS (Cont'd)

A more meaningful interpretation of noise margin can be gained by examining the relationship between input and output voltage of a circuit. *Figures 2-19, 2-20* and *2-21* show the voltage transfer function of TTL, S-TTL and LS-TTL inverting gates, respectively. The steepest part of a particular curve, where the output changes rapidly for small changes in input, is called the threshold region. Input signals above or below this region cause little or no change in output and thus are of no concern. Problems can occur when an input voltage, whether steady-state, transient or a combination of both, causes an output voltage to rise or fall into the threshold region of its driven loads. Thus, noise of this magnitude can propagate, which is a useful criterion.

The transfer characteristics of *Figures 2-19* through *2-21* are essentially steady-state and thus apply for noise disturbances of long duration. For short pulses, however, the finite response time of a circuit has an effect on noise sensitivity. *Figure 2-22* illustrates pulse noise immunity of TTL gates of the various families. These data are obtained by applying positive pulses to an otherwise LOW input and noting the combinations of pulse amplitude and duration required to cause the output to fall to 2.0 V, which is the guaranteed input HIGH level for TTL circuits. The curves show that S-TTL responds to the shortest pulses, as might be expected, and that pulse durations greater than about 4.0 ns have essentailly the same effect as dc input voltge. The curves show that plain TTL (7400) is the least sensitive to noise pulses, with H-TTL and LS-TTL responses intermediate between those of 7400 and S-TTL. The flat portion of the various curves shows that LS-TTL is the most sensitive to long duration pulses, while 7400 is least sensitive. This can also be deduced by comparing the transfer functions of *Figures 2-19* and *2-21*; the LS-TTL threshold regions are nearer the left hand axis, indicating that a lower value of input voltage is required to affect the output voltage than is the case with plain TTL.

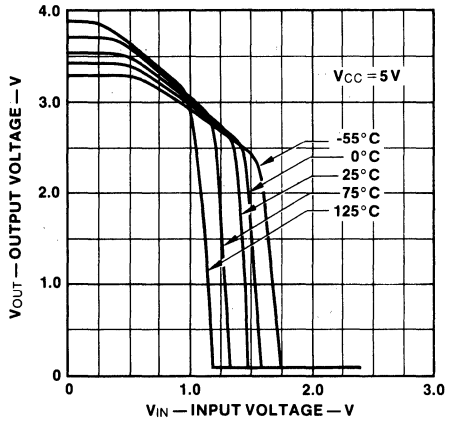


Fig. 2-19 Voltage Transfer Function of a 9000 Series Gate

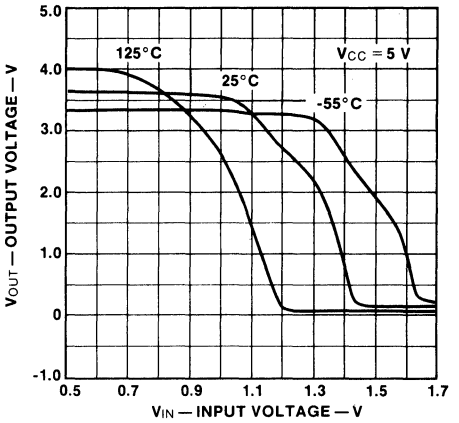


Fig. 2-20 Voltage Transfer Function of an S-TTL Gate

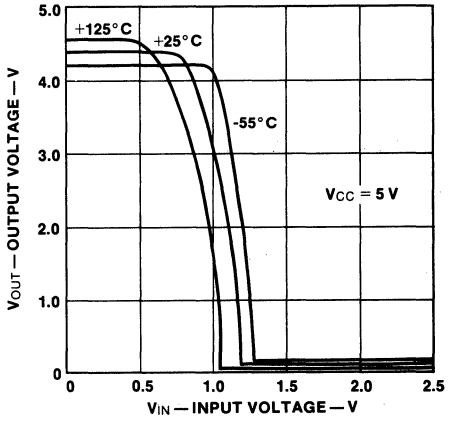


Fig. 2-21 Voltage Transfer Function of an LS-TTL Gate

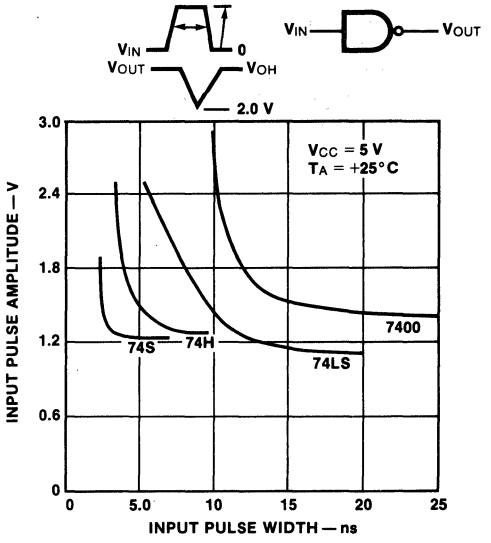


Fig. 2-22 Pulse Noise Immunity of TTL Gates

CROSSTALK

Crosstalk, the coupling of energy from one circuit to another via parasitic capacitance and inductance, causes increased problems in digital systems as the rise and fall times of the circuit decrease. The subject is extremely complicated, and no simple formula can give correct values in all cases for the amplitude of noise coupled from one circuit to another. In some circumstances where the input and output resistances of the circuits are high, a lumped equivalent circuit model can be drawn and reasonable calculations made. However, when the connections act as transmission lines, the situation is extremely complicated. TTL elements have a low output impedance in both HIGH and LOW logic states, and it is very difficult to couple enough energy into a short interconnection between devices to switch an adjacent circuit erroneously.

Noise introduced via capacitive coupling will have the same polarity as the disturbing signal and its amplitude will be inversely proportional to the rise or fall time of the disturbing signal. Noise introduced via magnetic coupling can be of either polarity. Open wire connections between TTL circuits should not be bundled, tied or routed together.

CROSSTALK (Cont'd)
Long parallel signal wires should be separated by ground wires to minimize coupling, particularly if one leads to the Clock (or asynchronous Set or Clear) input of a flip-flop, counter or register. In the case of ripple counters such as the 'LS90/'92/'93/'290/'293/'390/'393 and '490, the output of one stage may be internally connected to the Clock input of the next stage. Excessive coupling between outputs can therefore cause erratic counting. This situation most often occurs when counter outputs are taken off-card to a display unit by means of flat cable. In these cases it is best to use every other wire in the cable for ground in order to prevent erratic operation. In the case of parallel signal wires that do not involve a Clock or Asynchronous Set/Reset input, and close coupling of signal wires is unavoidable, it is advisable to wait until induced disturbances (following a signal change on one or more wires) have died out before sampling the data on a line. A disturbance induced in one wire by a signal change on another will have a time duration equal to twice the propagation delay of the wires. If two wires are closely coupled over a distance of three feet, involving a propagation delay of perhaps 5.0 ns, for example, an induced disturbance will have a duration of 10 ns.

TRANSMISSION LINES
Practical transmission lines, cables and strip lines used for TTL interconnections have a characteristic impedance between 50 Ω and 150 Ω. Thus none of the standard or low power TTL circuits can drive a transmission line, and only the 'S40/'S140 is truly capable of driving a 50 Ω line under worst case conditions.

These considerations, applicable only when the round trip delay of the line is longer than the rise or fall time of the driving signal ($2t_d > t_r$), do not affect most TTL interconnections. Short interconnections do not behave like a resistive transmission line, but more like a capacitive load. Since the rise time of different TTL outputs is known, the longest interconnection that can be tolerated without causing transmission line effects can easily be calculated and is listed in *Table 2-8* below.

Table 2-8 PC Board Interconnections

TTL FAMILY	RISE TIME	FALL TIME	MAX INTERCONNECTION LENGTH
93L	14 — 18 ns	4 — 6 ns	18 in. (45 cm)
9XXX, 93XX, 54/74	6 — 9 ns	4 — 6 ns	18 in. (45 cm)
54H/74H, 54LS/74LS	4 — 6 ns	2 — 3 ns	9 in. (22.5 cm)
54S/74S, 93S	1.8 — 2.8 ns	1.6 — 2.6 ns	7.5 in. (19 cm)

Assuming 1.7 ns/foot propagation speed, typical for epoxy fiberglass PC boards with $\Sigma_r = 4.7$.

Slightly longer interconnections show minimal transmission line effects; the longer the interconnections, the greater the chance that system performance may be degraded due to reflections and ringing. The discussion of transmission line effects gives additional information on transmission line phenomena on longer lines. Good system operation can generally be obtained by designing around 100 Ω lines. A 0.026 inch (0.65 mm) trace on an epoxy-glass board ($\Sigma_r = 4.7$) with a ground plane on the other side represents a 100 Ω line. Wire of 28 to 30 gauge (0.25 mm to 0.30 mm) twisted together forms a twisted pair line with a characteristic impedance of 100 Ω to 115 Ω. Wire over ground screen (3/4" squares) gives 150 Ω to 250 Ω impedance with a significant improvement in propagation speed, since the dielectric constant approaches that of air.

Transmission lines are also discussed in the FAIRCHILD ECL DATABOOK, the FAIRCHILD INTERFACE HANDBOOK and the FAIRCHILD TTL APPLICATIONS BOOK.

TRANSMISSION LINE EFFECTS

The fast rise and fall times of TTL outputs (2.0 ns to 6.0 ns) produce transmission line effects even with relatively short (< 2 ft) interconnections. Consider one TTL device driving another, and the driver switching from the LOW to the HIGH state. If the propagation delay of the interconnection is long compared to the rise time of the signal, the arrangement behaves like a transmission line driven by a generator with a non-linear output impedance. Simple transmission line theory shows that the initial voltage step at the output just after the driver has switched is

$$V_{OUT} = V_E \left(\frac{Z_o}{Z_o + R_o} \right)$$

where Z_o is the characteristic impedance of the line, R_o is the output impedance of the driver, and V_E is the equivalent output voltage source in the driver, V_{CC} minus the forward drop of the pull-up transistors.

Figure 2-23 shows how the initial voltge step can be determined graphically by superimposing lines of constant impedance on the static input and output characteristics of TTL elements. The constant impedance lines are drawn from the intersection of the V_{IN} and V_{OL} characteristics, which is the quiescent condition preceding a LOW-to-HIGH transition. After this transition the V_{OH} characteristic applies, and the intersection of a particular impedance line with the V_{OH} characteristic determines the initial voltage step. The V_{OH} characteristic shown in *Figure 2-23* has an R_o of about 80 Ω and V_E of approximately 4.0 V, for calculation purposes.

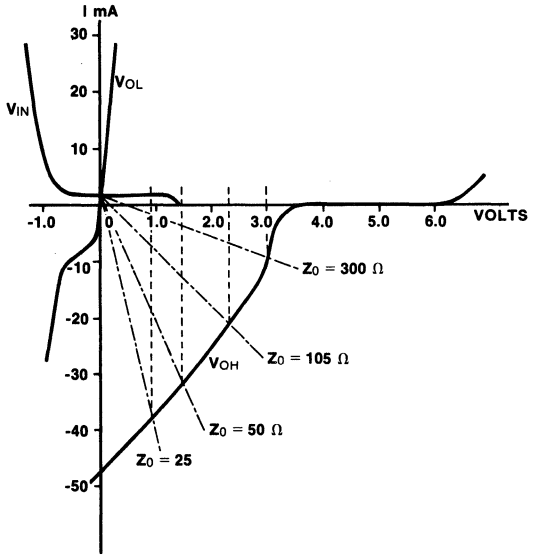


Fig. 2-23 Initial Output Voltage of TTL Driving Transmission Line

TRANSMISSION LINE EFFECTS (Cont'd)

This initial voltage step propagates down the line and reflects at the end, assuming the typical case where the line is open-ended or terminated in an impedance greater than its characteristic impedance Z_o. Arriving back at the source, this reflected wave increases V_{OUT}. If the total round-trip delay is larger than the rise time of the driving signal, there is a staircase response at the driver output and anywhere along the line. If one of the loads (gate inputs) is connected to the line close to the driver, the initial output voltage V_{OUT} might not exceed V_{IH}. This input is then undetermined until after the round trip of the transmission line, thus slowing down the response of the system. *Figure 2-24* shows the driver output waveform for four different line impedances. For Z_o of 25 Ω and 50 Ω the initial voltage step is in the threshold region of a TTL input and the output voltage only rises above the guaranteed 2.0 V V_{IH} level after a reflection returns from the end of the line. If V_{OUT} is increased to >2.0 V by either increasing Z_o or decreasing R_o, additional delay does not occur. R_o is a characteristic of the driver output configuration, varying between the different TTL speed categories. Z_o can be changed by varying the width of the conductor and its distance from ground. *Table 2-9* lists the lowest transmission line impedance that can be driven by different TTL devices to insure an initial voltage step of 2.0 V. Note that the worst case value, assuming a +30% tolerance on the current limiting resistor and a -10% tolerance on V_{CC}, is 80% higher than the value for nominal conditions.

Table 2-9 Transmission Line Drive Capability

TTL FAMILY OR DEVICE	COLLECTOR RESISTOR R Ω	Lowest Transmission Line Impedance Ω				
		WORST CASE (R + 30%)		NOMINAL	BEST CASE (R - 30%)	
54/74	130	241.4	204.8	136.8	84.6	75.8
9XXX, 93XX	80	148.5	126.0	84.2	52.0	46.6
54H/74H	58	107.7	91.3	61.0	37.7	33.8
54S/74S	55	110.0	92.2	61.1	37.5	33.4
93L	320	594.2	504.2	336.8	208.3	186.6
9009	50	92.8	78.7	52.6	32.5	29.1
5440/7440	100	185.7	157.5	105.2	65.1	58.3
54H/74H40	60	111.4	94.5	63.1	39.0	35.0
54S/74S40	25	50.0	41.9	27.7	17.0	15.2
54S140/74S140						
Supply Voltage (V_{CC})		4.50	4.75	5.00	5.25	5.50

Commercial grade range

Military grade range

A graphical method provides excellent insight into the effects of high speed digital circuits driving interconnections acting as transmission lines. The method is basically to draw a load line for each input and output situation. Each load line starts at the previous quiescent point, determined where the previous load line cuts the appropriate characteristic. The magnitude of the slope of the load lines is identical and equal to the characteristic impedance of the line, but alternate load lines have opposite signs representing the change in direction of current flow. The points where the load lines cut the input and output characteristics represent the voltage and current value at the input or output, respectively, for that reflection. This method, illustrated in *Figure 2-25*, is shown with and without the input diode, and illustrates how the input diode on TTL elements assists in eliminating spurious switching due to reflection.

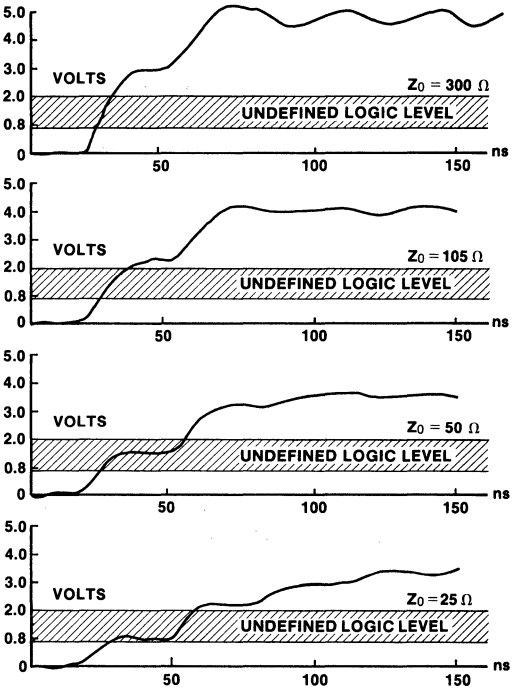


Fig. 2-24 TTL Driving Transmission Line

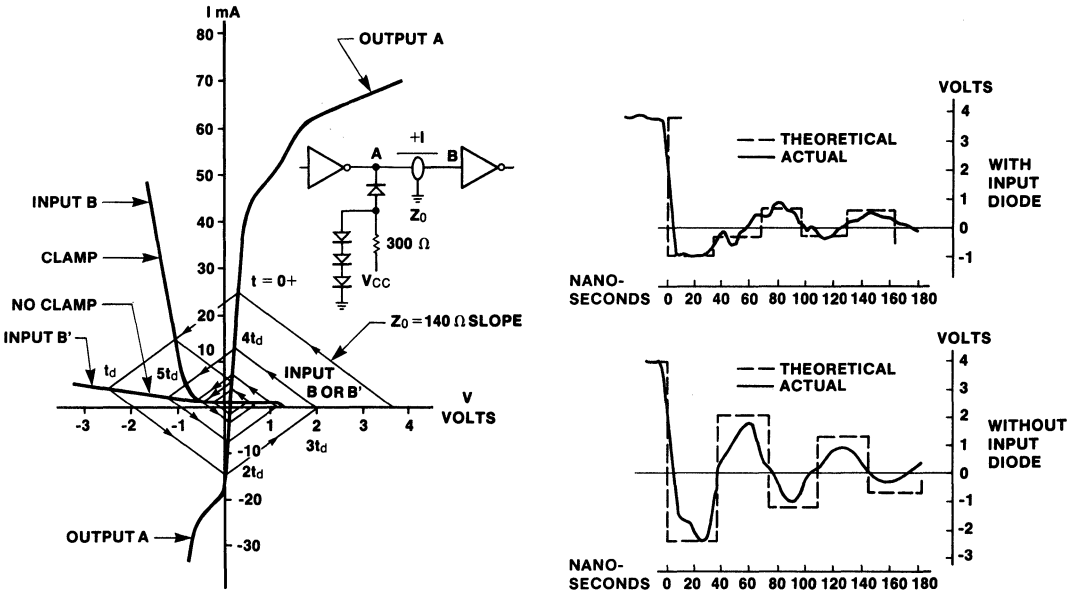


Fig. 2-25 Ringing Caused by Reflections

BACKPLANE DATA BUS

Unterminated lines can impose a limitation on maximum data rate because of the waiting time required for reflections and ringing to damp out. For higher data rates, wherein terminations are required to control reflections, a common technique is to use open-collector drivers and terminate each end of a signal wire with a resistive divider between V_{CC} and ground as shown in *Figure 2-26*. To terminate a 120 Ω twisted pair, for example, a 180 Ω resistor to V_{CC} and a 390 Ω resistor to ground offers a Thevenin equivalent resistance of 123 Ω and a no-load voltage of 3.4 V with a V_{CC} of 5.0 V. Under nominal conditions and assuming a quiescent LOW level of 0.5 V, a driver must be able to sink about 24 mA from each end of the line, or 48 mA total. The quiescent LOW current flowing in the line furnishes the pull-up mechanism when a driver turns off. When the quiescent current is interrupted, a voltage change is generated whose magnitude is the product of the line impedance and the current. Thus the interruption of 24 mA flowing in a 120 Ω line causes a voltage rise of about 2.9 V, from the quiescent 0.5 V to 3.4 V. With variations in V_{CC} and resistor tolerances, the quiescent LOW current can be considerably more than 48 mA, and a circuit such as the 96101 Quad Bus Driver, which is guaranteed to sink 80 mA, is recommended. The 96106 Quad NOR has higher noise margin and lower input loading than other TTL gates and is therefore well suited as a line receiver. The 96103 Quad Transceiver combines the input attributes of the 96106 with an open-collector driver capable of sinking 70 mA.

For communications between subsystems that are located in separate enclosures, wherein attenuation and noise are important factors, the general practice is to use specialized drivers and receivers. Drivers with complementary outputs*, such as the 9614, 9634 or 9638, can drive terminated twisted pair lines. Line receivers with differential inputs*, such as the 9615, 9620 or 9637 provide good common-mode noise rejection and accommodate attenuated input signals.

DECOUPLING

Decoupling capacitors should be used on every pc card, at least one for every 5 to 10 standard TTL packages, one for every five 74H and 74S packages and one for every one-shot (monostable), line driver and line receiver package. They should be good quality rf capacitors of 0.01 μF to 0.1 μF with short leads. It is particularly important to place good rf capacitors near sequential (bistable) devices. In addition, a larger capacitor (preferably a tantalum capacitor) of 2.0 μF to 20 μF should be included on each card.

GROUNDS

A good ground system is essential for a pc card containing a large number of packages. The ground can either be a good ground bus, or better yet, a ground plane which, incorporated with the V_{CC} supply, forms a transmission line power system. Power transmission systems, which can be attached to a pc card to give an excellent power system without the cost of a multilayer pc card, are commercially available. Ground loops on or off pc cards are to be avoided unless they approximate a ground plane.

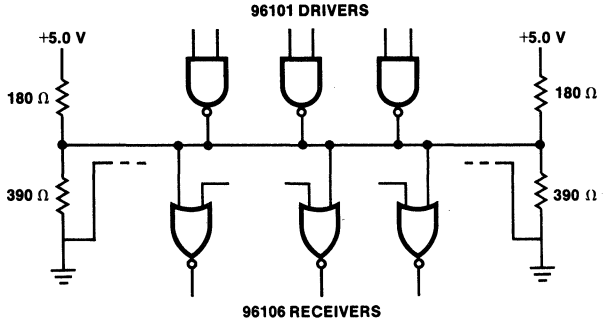


Fig. 2-26 High Speed Backplane Data Bus Using Twisted Pair or Flat Cable

*Refer to FAIRCHILD LINEAR INTEGRATED CIRCUIT DATA BOOK

SUPPLY VOLTAGE AND TEMPERATURE

The nominal supply voltage V_{CC} for all TTL circuits is +5.0 V. Commercial grade parts are guaranteed to perform with ±5% supply tolerance (±250 mV) over an ambient temperature range of 0°C to 75°C (some to 70°C). Mil grade parts are guaranteed to perform with a ±10% supply tolerance (±500 mV) over an ambient temperature range of -55°C to 125°C.

The actual junction temperature can be calculated by multiplying the power dissipation of the device with the thermal resistance of the package and adding it to the measured ambient temperature T_A or package (case) temperature T_C.

Table 2-1 lists some of the standard Dual In-line Packages (DIP) and Flatpaks used by Fairchild, including typical junction-to-ambient thermal resistance θ_{JA} and typical junction-to-case thermal resistance θ_{JC}. Designers should bear in mind that localized temperatures can rise well above the general ambient in a system enclosure. On a large pc board mounted in a horizontal plane, for example, the local temperature surrounding an IC in the middle of the board can be quite high due to the heating effect of the surrounding packages and the very poor natural convection. Low velocity forced air cooling is usually sufficient to alleviate such stagnant air conditions.

Table 2-10 Thermal Resistances

PACKAGE	θ_{JA}, °C/W	θ_{JC}, °C/W
14-Pin Flatpak	128	50
16-Pin Flatpak	123	47
24-Pin Flatpak	90	44
14-Pin CerDIP	115	35
16-Pin CerDIP	100	30
24-Pin CerDIP	60	25
14-Pin Plastic DIP	125	48
16-Pin Plastic DIP	120	45
24-Pin Plastic DIP	74	40

Example: A 9301 in CerDIP dissipates typically 145 mW. At +55°C ambient temperature the junction temperature is:

$$T_J = (0.145 \times 100) + 55 = 70°C$$

INTERFACING

All circuits in the Fairchild TTL families, in fact all TTL devices presently manufactured, are compatible. Any TTL output can drive a certain number of TTL inputs, as described in Section 3. There are only subtle differences in the worst case noise immunity when low power, standard and Schottky TTL circuits are intermixed. Open-collector outputs, however, require a pull-up resistor to drive TTL inputs reliably, as discussed earlier.

While TTL is the dominating logic family, and many systems use TTL exclusively, there are cases where different semiconductor technologies are used in one system, either to improve the performance or to lower the cost, size and power dissipation. The following explains how TTL circuits can interface with DTL, ECL (CML), CTL, and discrete transistors.

Interfacing TTL and DTL — Both DTL and TTL are current sinking families, operating on a +5.0 V supply. They interface perfectly. When TTL drives DTL, one DTL input represents 1 U.L. in the LOW state, much less than 1 U.L. in the HIGH state. When DTL drives TTL, a 2 kΩ output has a drive capability of 8 U.L., a 6 kΩ output has a drive capability of 4 U.L.

INTERFACING (Cont'd)

Interfacing TTL and ECL — Mixing ECL and TTL logic families offers the design engineer a new level of freedom and opens the entire vhf frequency spectrum to the advantages of digital measurement, control and logic operation.

The chief advantages of emitter coupled logic are high speed, flexibility, design versatility and transmission line compatibility. But application and interfacing cost problems have traditionally discouraged the use of ECL in many areas, particularly in low cost, less sophisticated systems. Using 95K or 10K compensated ECL with new ECL/TTL interface devices and several new interfacing methods promises to extend the advantages of ECL to many low cost systems.

The most practical interfacing method for smaller systems involves using a common supply of +5.0 V to +5.2 V. Care must be exercised with both logic families when using this technique to assure proper bypassing of the power supply to prevent any coupling of noise between circuit families. If only a few 95K or 10K ECL packages are designed into a predominantly TTL system the safest method is to use a 0.01 μF miniature ceramic capacitor across each ECL device. This value capacitor has the highest Q, or bypassing efficiency. When larger systems are operated on a common supply, separate power busses to each logic family help prevent problems. Otherwise, good high frequency bypassing techniques are usually sufficient.

95K series ECL devices are fully compensated so that input thresholds and output levels are immune to broad variations in ambient temperature and supply voltage. This feature makes it easier to interface with TTL and to operate with the TTL power supply. 95K and 10K devices have high input impedance with input pull-down resistors (> 20 kΩ) to the negative supply. In the TTL to ECL interface circuits in *Figure 2-27* it is assumed that the ECL devices have high input impedance.

9500 series ECL elements are temperature compensated and have internal 2 kΩ pull-down resistors at each input and output. These resistors provide partial termination of interconnecting transmission lines, in many cases eliminating the need for external terminations. For ECL inputs with 2 kΩ pull-down resistors, the 750 Ω resistors shown in the TTL to ECL circuits should be changed to 1.2 kΩ in order to provide the proper ECL input signal levels.

All circuits described operate with ±5% ECL and ±10% TTL supply variations, except those with ECL and TTL on a common supply. In those cases the supply can be ±10% with 95K or 10K ECL, ±5% with 9500 series ECL. All resistors are 1/4 W, ±5% composition type.

TTL to ECL conversion is easily accomplished with resistors, which simultaneously attenuate the TTL signal swing, shift the signal levels, and provide low impedance for damping and immunity to stray noise pick-up. The resistors should be located as near as possible to the ECL circuit for optimum effect. The circuits in *Figure 2-27* assume an unloaded TTL gate as the standard TTL source. ECL input impedance is predominately capacitive (≈3 pF); the net RC time constant of this capacitance with the indicated resistors assures a net propagation delay governed primarily by the TTL signal.

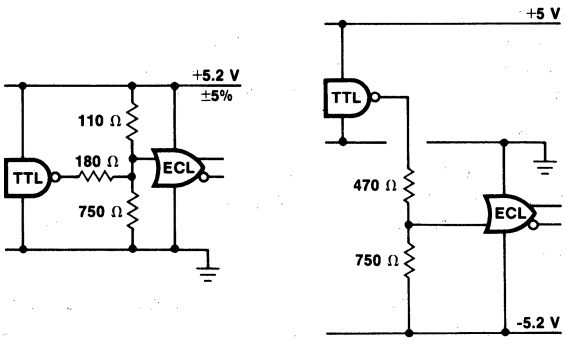
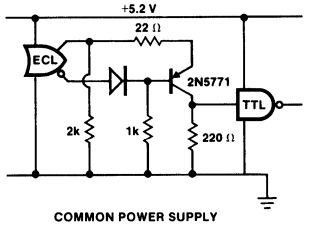


Fig. 2-27 TTL to ECL Conversion

INTERFACING (Cont'd)
When interfacing between high voltage-swing TTL logic and low voltage-swing ECL logic, the more difficult conversion is from ECL to TTL. This requires a voltage amplifier to build up the 0.8 V logic swing to a minimum of 2.5 V. The circuits shown in *Figure 2-28* may be used to interface from ECL to TTL.

The higher speed converters usually have the lowest fan-out — only one or two TTL gates. This fan-out can be increased simply by adding a TTL buffer gate to the output of the converter. Another option, if ultimate speed is required, is to use additional logic converters.

Interfacing TTL and CTL — CTL (Complementary Transistor Logic) is a family of high speed digital circuits used mainly in computers. It uses AND gates and wired-OR outputs for logic flexibility, but logic levels are not restored in each gate. Level restoring buffers (956) are therefore required, and all interfacing should be done with restored logic levels. The CTL input threshold is ≈ 1 V, similar to TTL, but 1.0 mA to 2.0 mA are required to pull the CTL input reliably over the threshold. A normal TTL output can drive a CTL input, but noise immunity is improved considerably by a 1 kΩ pull-up resistor *(Figure 2-29)*. The CTL output emitter follower can source >30 mA but cannot sink current. A resistive termination is therefore required. When the resistor is returned to ground, it may not exceed 250 Ω to guarantee a V_{OL} of < 400 mV at a fan-out of 1 U.L. A better, less power consuming way for a fan-out of 1 U.L. is to use the built-in pull-down resistor (1 kΩ to -2.0 V). For increased fan-out, this resistor can be reduced by a parallel external resistor to 180 Ω (8 U.L.), as indicated in *Figure 2-30*.



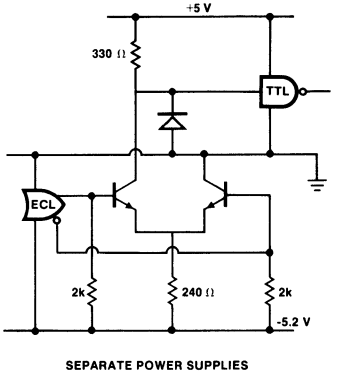


Fig. 2-28 ECL to TTL Conversion

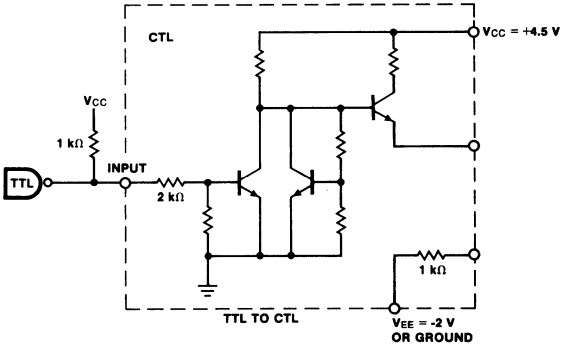


Fig. 2-29 TTL to CTL Conversion

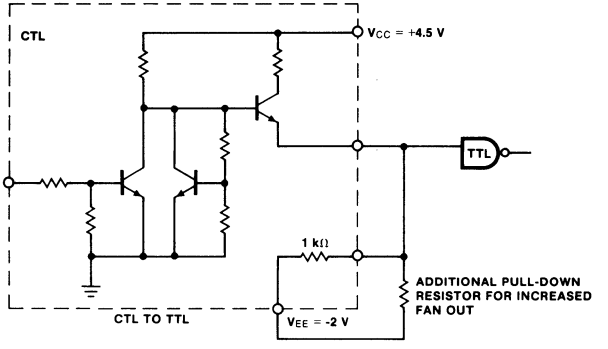


Fig. 2-30 CTL to TTL Conversion

INTERFACING (Cont'd)

Interfacing TTL and CMOS — With a 5.0 V power supply, a B Series (buffered) CMOS output is guaranteed to sink 0.4 mA at V_{OL} = 0.4 V, which matches the input requirements of a standard LS-TTL input. If the CMOS supply voltage V_{DD} is greater than 5.0 V, the LS-TTL input must be one having an input diode, as opposed to an emitter. This insures that the high V_{OH} of CMOS ($\simeq V_{DD}$) will not cause breakdown of the LS-TTL input. A CMOS input threshold V_{IH} may be as high as 70% of V_{DD}, while its V_{IL} will be no lower than 30% of V_{DD}. Thus a TTL output signal is satisfactory at the LOW level, but a pull-up resistor is required to ensure an adequate HIGH level for the CMOS input. The resistor should connect to the CMOS V_{DD} supply, and if this exceeds 5.5 V, the TTL driver must have the capability of not conducting appreciably at this higher voltage. Most LS-TTL outputs can withstand 10 V, as discussed in Section 3.

TTL Driving Transistors — Although high voltage, high current ICs, such as the 9644, are available, it is sometimes necessary to control greater currents or voltages than integrated circuits are capable of handling. When this condition arises, a discrete transistor with sufficient capacity can be driven from a TTL output. Discrete transistors are also used to shift voltages from TTL levels to logic levels for which a standard interface driver is not available.

The two circuits of *Figure 2-31* show how TTL can drive npn transistors. The first circuit is the most efficient but requires an open-collector TTL or DTL output. The other circuit limits the output current from the TTL totem-pole output through a series resistor.

Shifting a TTL Output to Negative Levels — The circuit of *Figure 2-32* uses a pnp transistor to shift the TTL output to a negative level. When the TTL output is HIGH, the transistor is cut off and the output voltage is $-V_X$. When the TTL output is LOW, the transistor conducts and the output voltage is

$$-V_X + \frac{R1}{R2}(V_{CC} - 2.0\,V)$$

if the transistor is not saturated, or slightly positive if the transistor is allowed to saturate.

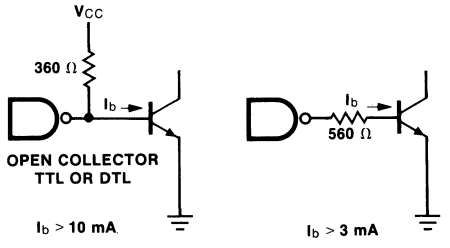


Fig. 2-31 TTL Driving NPN Transistors

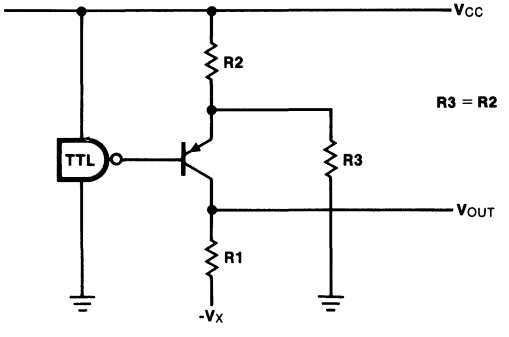


Fig. 2-32 PNP Transistor Shifting TTL Output

INTERFACING (Cont'd)

High Voltage Drivers — A TTL output can be used to drive high voltage, low current loads through the simple, non-inverting circuits shown in *Figure 2-33*. This can be useful for driving gas discharge displays or small relays, where the TTL output can handle the current but not the voltage. Load current should not exceed (I_{OL} - 4) mA.

Transistors Driving TTL — It is sometimes difficult to drive the relatively low impedance and narrow voltage range of TTL inputs directly from external sources, particularly in a rough, electrically noisy environment. The circuits shown in *Figure 2-34* can handle input signal swings in excess of ±100 V without harming the circuits. The second circuit has an input RC filter that suppresses noise. Unambiguous TTL voltage levels are generated by the positive feedback (Schmitt trigger) connection.

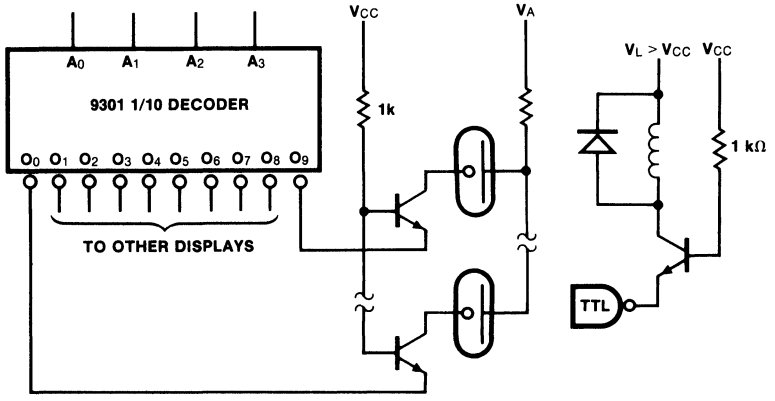


Fig. 2-33 Non-Inverting High Voltage Drivers

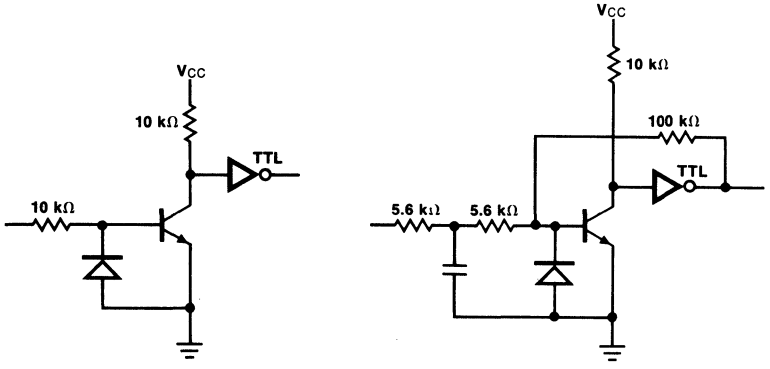
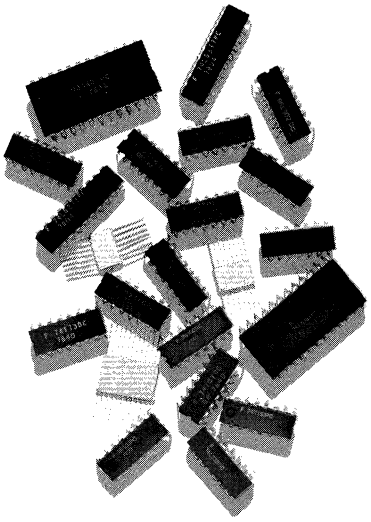


Fig. 2-34 Transistors Driving TTL



SECTION 3

- Unit Loads (U.L.)
- Absolute Maximum Ratings
- Recommended Operating Conditions
- DC Characteristics Tables
  - 54XX, 74XX & 93XX Family DC Characteristics
  - 54H, 74H, & 93H Family DC Characteristics
  - 54S, 74S & 93S Family DC Characteristics
  - 54LS, 74LS & 96LS Family DC Characteristics
  - 9XXX Family DC Characteristics
  - 93L Family DC Characteristics
- AC Loading and Waveforms
  - AC Loads for SSI Gates Waveforms

Section 3
LOADING, SPECIFICATIONS AND WAVEFORMS

This section contains dc specifications and ratings common to all devices in each family of circuits. These specifications plus the distinctive characteristics given in the individual data sheet are necessary to fully define a circuit for testing or procurement purposes. Included is a discussion of the Unit Load method of normalizing the input and output characteristics of a circuit, and how to translate the numbers given in the Input Loading/Fan-Out table of a data sheet into the actual values of I_{IH}, I_{IL}, I_{OH} and I_{OL} currents. The various load configurations for ac testing, a table of R_L and C_L values for SSI gates and waveforms that help to define the various ac parameters are also included.

UNIT LOADS (U.L.)

For convenience in system design the input loading and fan-out characteristics of each circuit are specified in terms of unit loads. One unit load in the HIGH state is defined as 40 μA; thus both the input HIGH leakage current I_{IH} and the output HIGH current sourcing capability I_{OH} are normalized to 40 μA. Similarly, one unit load in the LOW state is defined as 1.6 mA and both the input LOW current I_{IL} and the output LOW current sinking capability I_{OL} are normalized to 1.6 mA. On the data sheets the input and output load factors are listed in the Input Loading/Fan-Out table. The table from the 54/7404 Hex Inverter is reproduced below.

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	**54/74 (U.L.)** HIGH/LOW	**54/74H (U.L.)** HIGH/LOW	**54/74S (U.L.)** HIGH/LOW	**54/74LS (U.L.)** HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

The input loading and fan-out factors are arranged in four columns, since this hex inverter is available in standard TTL, H-TTL, S-TTL and LS-TTL. Under the 54/74H heading, for example, the input HIGH/LOW load factors are 1.25/1.25, with the first number representing I_{IH} and the second representing I_{IL}. For purposes of testing or procurement these load factors can be easily translated to actual test limits by simply multiplying them by 40 μA and 1.6 mA, respectively. The second set of numbers represents the rated output HIGH/LOW load currents I_{OH} and I_{OL}, respectively. In the 54/74S column the output HIGH/LOW drive factors of 25/12.5 translate to 1.0 mA and 20 mA by multiplying them by 40 μA and 1.6 mA, respectively.

For any input or output for which the Military and Commercial grade specifications differ, the Military grade loading or fan-out factors are shown in parenthesis immediately below the Commercial grade factors. In the case of the 54/74LS04 in the sample table shown, the output LOW fan-out for the Commercial grade (74LS04) is shown as 5.0 (equivalent to 8.0 mA), while the rating for the Military grade (54LS04) is 2.5 (or 4.0 mA). The output HIGH fan-out rating for the Military grade is the same as for the Commercial grade and thus the rating of 10 loads (or 400 μA I_{OH}) is not repeated in parenthesis.

For convenience in system design the input and output loading factors should not be translated into μA and mA. It is only necessary to add up the input loading factors of all inputs connected to a particular logic function and compare the total unit loading with the fan-out capability of the source of that particular function. For example, a function that connects to one input of each of the hex inverter types in the table above must drive the total loading calculated below.

Input HIGH Loading = 1.0 + 1.25 + 1.25 + 0.5 = 4.0 Unit Loads
Input LOW Loading = 1.0 + 1.25 + 1.25 + 0.25 = 3.75 Unit Loads

UNIT LOADS (U.L.) (Cont'd)
To extend the example, this amount of loading can be driven by any one of the hex inverters in the Commercial grade, since all outputs have fan-out capabilities greater than 4.0/3.75. In the Military grade, however, the 54LS04 has a rated output LOW drive factor of only 2.5 and thus could not be guaranteed to drive 3.75 unit loads. Thus a different type of driver would be selected for operation over the Military temperature range.

In the case of an open-collector output, which is not capable of supplying I_{OH} current or of establishing a V_{OH} level, the output HIGH load factor does not apply and thus the abbreviation OC is substituted. It is assumed that the system designer will specify a pull-up resistor value that will establish the desired V_{OH} while supplying the cumulative I_{IH} of the driven loads plus the I_{OH} leakage current of the output (or outputs, in the case of wired-collector logic) as specified in either the pertinent Family DC Characteristics table or on the data sheet.

ABSOLUTE MAXIMUM RATINGS[1] (beyond which useful life may be impaired)

Storage Temperature	-65°C to +150°C
Ambient Temperature Under Bias	-55°C to +125°C
Junction Temperature Under Bias	-55°C to +175°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
Input Voltage[2]:	
Emitter Inputs	-0.5 V to +5.5 V
LS-TTL[3] Diode and pnp Inputs	-0.5 V to +15 V
Input Current[2,4]	-30 mA to +5.0 mA
Voltage Applied to Outputs in HIGH State:	
Open Collector	-0.5 V to +7.0 V
Standard TTL, H-TTL, S-TTL, LP-TTL	-0.5 V to V_{CC} Value
Standard LS-TTL[5] (with recommended operating V_{CC})	-0.5 V to +10 V
3-State LS-TTL (with V_{CC} = 0 V)	-0.5 V to +5.5 V
Current Applied to Outputs in LOW State (Max)	twice the rated I_{OL}

RECOMMENDED OPERATING CONDITIONS[1]

	Min	Max
Free Air Ambient Temperature		
Military (XM)	-55°C	+125°C
Commercial (XC)	0°C	+70°C
Supply Voltage		
Military (XM)	+4.5 V	+5.5 V
Commercial (XC)	+4.75 V	+5.25 V

NOTES:
1. Unless otherwise restricted or extended by detail specifications.
2. Either input voltage limit or input current limit is sufficient to protect inputs.
3. Refer to input breakdown test in 54LS/74LS family DC Characteristics or individual data sheets for emitter type LS-TTL inputs.
4. Except 9315/7441 limited to -10 mA to +1.0 mA. Also, steady-state clamp diode currents greater than -2.0 mA in LS-TTL inputs can cause logic malfunctions; see discussion in Section 2.
5. Except 'LS00, 'LS02, 'LS04, 'LS10, 'LS11, 'LS20, 'LS32, 'LS74, 'LS86, 'LS109, 'LS112, 'LS113 and 'LS114 limited to -0.5 V to +V_{CC} Value.

DC CHARACTERISTICS TABLES

Most of the circuits described in this data book were designed within the general framework of one of the distinctive families of TTL circuits, i.e., TTL, H-TTL, S-TTL, LP-TTL or LS-TTL. Many dc specifications are common to almost all circuits of a particular family, e.g., V_{IH}, V_{IL}, V_{OH}, V_{CD}, etc. and to avoid needless repetition these common parameters do not appear on the individual data sheets. On the following pages are tables of dc characteristics containing the parameters, limits and conditions common to the various families of TTL circuits. These are intended to augment the distinctive parameters, such as ac characteristics, input loading, fan-out and power supply current listed on the individual data sheets. In some cases a particular circuit will depart from its family characteristics in one or more parameters and in these cases the limits or conditions shown on the individual data sheets take precedence over the values listed in the family characteristics table.

54XX, 74XX, 93XX & 96XX FAMILY DC CHARACTERISTICS[1]

SYMBOL[2]	PARAMETER		LIMITS[3] Min	Typ[4]	Max	UNITS	V_{CC}[5]	CONDITIONS[3]
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal Over Recommended V_{CC} and T_A Range
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal Over Recommended V_{CC} and T_A Range
V_{CD}	Input Clamp Diode Voltage				-1.5	V	Min	I_{IN} = -12 mA
V_{OH}	Output HIGH Voltage		2.4	3.4		V	Min	I_{OH} = 40 μA Multiplied by Output HIGH U.L. Shown on Data Sheet
V_{OL}	Output LOW Voltage			0.2	0.4	V	Min	I_{OL} = 1.6 mA Multiplied by Output LOW U.L. Shown on Data Sheet
I_{IH}	Input HIGH Current	1.0 U.L.			40	μA	Max	I_{IH} = 40 μA Multiplied by Input HIGH U.L. Shown on Data Sheet; V_{IN} = 2.4 V
		2.0 U.L.			80			
		n U.L.			n(40)			
	Input HIGH Current, Breakdown Test, All Inputs				1.0	mA	Max	V_{IN} = 5.5 V
I_{IL}	Input LOW Current	1.0 U.L.			-1.6	mA	Max	I_{IL} = 1.6 mA Multiplied by Input LOW U.L. Shown on Data Sheet; V_{IN} = 0.4 V
		2.0 U.L.			-3.2			
		n U.L.			n(-1.6)			
I_{OH}	Output HIGH Current, Open-Collector				250	μA	Min	V_{OH} = 5.5 V
I_{OZH}	3-State Output OFF Current HIGH				40	μA	Max	V_{OUT} = 2.4 V
I_{OZL}	3-State Output OFF Current LOW				-40	μA	Max	V_{OUT} = 0.4 V
I_{OS}[6]	Output Short Circuit Current	Std.[7] 54XX	-20		-57	mA	Max	V_{OUT} = 0 V
		Std.[7] 74XX	-18		-57			
		Buffers 54XX	-20		-70			
		Buffers 74XX	-18		-70			
		93XX	-20		-70			

Notes on following pages.

54H, 74H, & 93H FAMILY DC CHARACTERISTICS[1]

SYMBOL[2]	PARAMETER		LIMITS[3] Min	Typ[4]	Max	UNITS	V_{CC}[5]	CONDITIONS[3]
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal Over Recommended V_{CC} and T_A Range
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal Over Recommended V_{CC} and T_A Range
V_{CD}	Input Clamp Diode Voltage				-1.5	V	Min	I_{IN} = -12 mA
V_{OH}	Output HIGH Voltage		2.4	3.4		V	Min	I_{OH} = 40 μA Multiplied by Output HIGH U.L. Shown on Data Sheet
V_{OL}	Output LOW Voltage			0.2	0.4	V	Min	I_{OL} = 1.6 mA Multiplied by Output LOW U.L. Shown on Data Sheet
I_{IH}	Input HIGH Current	1.25 U.L.			50	μA	Max	I_{IH} = 40 μA Multiplied by Input HIGH U.L. Shown on Data Sheet; V_{IN} = 2.4 V
		2.5 U.L.			100			
		n U.L.			n(40)			
	Input HIGH Current, Breakdown Test, All Inputs				1.0	mA	Max	V_{IN} = 5.5 V
I_{IL}	Input LOW Current	1.25 U.L.			-2.0	mA	Max	I_{IL} = 1.6 mA Multiplied by Input LOW U.L. Shown on Data Sheet; V_{IN} = 0.4 V
		2.5 U.L.			-4.0			
		n U.L.			n(-1.6)			
I_{OH}	Output HIGH Current, Open-Collector				250	μA	Min	V_{OH} = 5.5 V
I_{OS}[6]	Output Short Circuit Current		-40		-100	mA	Max	V_{OUT} = 0 V

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. For definitions of symbols and terminology please see Section 2.
3. Unless otherwise stated on individual data sheets.
4. Typical characteristics refer to T_A = +25°C and V_{CC} = +5.0 V.
5. Min and Max refer to the values listed in the table of recommended operating conditions.
6. For testing I_{OS}, the use of high speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
7. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-state outputs.

54S, 74S & 93S FAMILY DC CHARACTERISTICS[1]

SYMBOL[2]	PARAMETER		LIMITS[3] Min	Typ[4]	Max	UNITS	V_{CC}[5]	CONDITIONS[3]
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal Over Recommended V_{CC} and T_A Range
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal Over Recommended V_{CC} and T_A Range
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage	Std.[7] Mil.	2.5	3.4		V	Min	I_{OH} = 40 μA Multiplied by Output HIGH U.L. Shown on Data Sheet
		Std.[7] Com.	2.7	3.4				
		3-State	2.4	3.2				
V_{OL}	Output LOW Voltage			0.35	0.5	V	Min	I_{OL} = 1.6 mA Multiplied by Output LOW U.L. Shown on Data Sheet
I_{IH}	Input HIGH Current	1.25 U.L.			50	μA	Max	I_{IH} = 40 μA Multiplied by Input HIGH U.L. Shown on Data Sheet; V_{IN} = 2.7 V
		2.5 U.L.			100			
		n U.L.			n(40)			
	Input HIGH Current, Breakdown Test, All Inputs				1.0	mA	Max	V_{IN} = 5.5 V
I_{IL}	Input LOW Current	1.25 U.L.			-2.0	mA	Max	I_{IL} = -1.6 mA Multiplied by Input LOW U.L. Shown on Data Sheet; V_{IN} = 0.5 V
		2.5 U.L.			-4.0			
		n U.L.			n(-1.6)			
I_{OH}	Output HIGH Current, Open-Collector				250	μA	Min	V_{OH} = 5.5 V
I_{OZH}	3-State Output OFF Current HIGH				50	μA	Max	V_{OUT} = 2.4 V
I_{OZL}	3-State Output OFF Current LOW				-50	μA	Max	V_{OUT} = 0.5 V
I_{OS}[6]	Output Short Circuit Current	Standard[7]/ 3-State	-40		-100	mA	Max	V_{OUT} = 0 V
		Buffers/ Line Dvrs	-50		-225			

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. For definitions of symbols and terminology please see Section 2.
3. Unless otherwise stated on individual data sheets.
4. Typical characteristics refer to T_A = +25°C and V_{CC} = +5.0 V.
5. Min and Max refer to the values listed in the table of recommended operating conditions.
6. For testing I_{OS}, the use of high speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
7. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-state outputs.

54LS, 74LS & 96LS FAMILY DC CHARACTERISTICS[1]

SYMBOL[2]	PARAMETER		LIMITS[3] Min	Typ[4]	Max	UNITS	V_{CC}[5]	CONDITIONS[3]
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal Over Recommended V_{CC} and T_A Range
V_{IL}	Input LOW Voltage	Mil.			0.7	V		Recognized as a LOW Signal Over Recommended V_{CC} and T_A Range
		Com.			0.8			
V_{CD}	Input Clamp Diode Voltage				-1.5	V	Min	I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage	Std.[7] Mil.	2.5	3.4		V	Min	I_{OH} = 40 μA Multiplied by Output HIGH U.L. Shown on Data Sheet
		Std.[7] Com.	2.7	3.4				
		3-State/Buffers	2.4	3.3				
		Line Dvrs	2.0	2.9				
V_{OL}	Output LOW Voltage	Com.		0.35	0.5	V	Min	I_{OL} = 1.6 mA Multiplied by Output LOW U.L. Shown on Data Sheet
		Mil. & Com.		0.25	0.4	V	Min	I_{OL} = 1.6 mA Multiplied by Output LOW U.L. Shown in Parenthesis on Data Sheet
I_{IH}	Input HIGH Current	0.5 U.L.			20	μA	Max	I_{IH} = 40 μA Multiplied by Input HIGH U.L. Shown on Data Sheet; V_{IN} = 2.7 V
		1.0 U.L.			40			
		n U.L.			n(40)			
	Input HIGH Current, Breakdown Test, All Inputs				100	μA	Max	V_{IN} = 10 V[8]
I_{IL}	Input LOW Current	0.25 U.L.			-0.4	mA	Max	I_{IL} = -1.6 mA Multiplied by Input LOW U.L. Shown on Data Sheet; V_{IN} = 0.4 V
		0.5 U.L.			-0.8			
		n U.L.			n(-1.6)			
I_{OH}	Output HIGH Current, Open-Collector				100	μA	Min	V_{OH} = 5.5 V
I_{OZH}	3-State Output OFF Current HIGH				20	μA	Max	V_{OUT} = 2.4 V
I_{OZL}	3-State Output OFF Current LOW				-20	μA	Max	V_{OUT} = 0.4 V
I_{OS}[6]	Output Short Circuit Current	Standard[7]	-20		-100	mA	Max	V_{OUT} = 0 V
		3-State/ Buffers	-30		-130			
		Line Dvrs	-40		-225			

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. For definitions of symbols and terminology please see Section 2.
3. Unless otherwise stated on individual data sheets.
4. Typical characteristics refer to T_A = +25°C and V_{CC} = +5.0 V.
5. Min and Max refer to the values listed in the table of recommended operating conditions.
6. For testing I_{OS}, the use of high speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
7. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-state outputs.
8. Except 5.5 V for 'LS03, 'LS05, 'LS22, 'LS74, 'LS109, 'LS112, 'LS113, 'LS114, 'LS136 (which have emitter inputs) and as shown on other data sheets.

9XXX FAMILY DC CHARACTERISTICS[1]

SYMBOL[2]	PARAMETER		LIMITS[3] Min	Typ[4]	Max	UNITS	V_{CC}[5]	CONDITIONS[3]
V_{IH}	Input HIGH Voltage (See Data Sheets)					V		Recognized as a HIGH Signal Over Recommended V_{CC} and T_A Range
V_{IL}	Input LOW Voltage (See Data Sheets)					V		Recognized as a LOW Signal Over Recommended V_{CC} and T_A Range
V_{CD}	Input Clamp Diode Voltage				-1.5	V	Min	I_{IN} = -12 mA
V_{OH}	Output HIGH Voltage		2.4	3.4		V	Min	I_{OH} = 40 μA Multiplied by Output HIGH U.L. Shown on Data Sheet
V_{OL}	Output LOW Voltage (See Data Sheets)							
I_{IH}	Input HIGH Current	1.0 U.L.			40	μA	Max	I_{IH} = 40 μA Multiplied by Input HIGH U.L. Shown on Data Sheet; V_{IN} = 4.5 V
		2.0 U.L.			80			
		n U.L.			n(40)			
I_{IL}	Input LOW Current (See Data Sheets)							
I_{OH}	Output HIGH Current, Open-Collector				250	μA	Min	V_{OH} = 5.5 V
I_{OS}[6]	Output Short Circuit Current	Std.[7] Mil.	-30		-100	mA	Max	V_{OUT} = 0 V
		Std.[7] Com.	-30		-120			
		9009	-40		-150			
		9024 Mil.	-40		-100			
		9024 Com.	-35		-110			

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. For definitions of symbols and terminology please see Section 2.
3. Unless otherwise stated on individual data sheets.
4. Typical characteristics refer to T_A = +25°C and V_{CC} = +5.0 V.
5. Min and Max refer to the values listed in the table of recommended operating conditions.
6. For testing I_{OS}, the use of high speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
7. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-state outputs.

93L FAMILY DC CHARACTERISTICS[1]

SYMBOL[2]	PARAMETER		LIMITS[3] Min	Typ[4]	Max	UNITS	V_{CC}[5]	CONDITIONS[3]
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal Over Recommended V_{CC} and T_A Range
V_{IL}	Input LOW Voltage	Mil.			0.7	V		Recognized as a LOW Signal Over Recommended V_{CC} and T_A Range
		Com.			0.8			
V_{CD}	Input Clamp Diode Voltage				-1.5	V	Min	I_{IN} = -10 mA
V_{OH}	Output HIGH Voltage		2.4	3.6		V	Min	I_{OH} = -400 μA
V_{OL}	Output LOW Voltage	Mil. & Com.			0.3	V	Min	I_{OL} = 4.8 mA
		Com.			0.4	V	Min	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current	0.5 U.L.			20	μA	Max	I_{IH} = 40 μA Multiplied by Input HIGH U.L. Shown on Data Sheet; V_{IN} = 2.4 V
		1.0 U.L.			40			
		n U.L.			n(40)			
	Input HIGH Current, Breakdown Test, All Inputs				1.0	mA	Max	V_{IN} = 5.5 V
I_{IL}	Input LOW Current	0.25 U.L.			-0.4	mA	Max	I_{IL} = -1.6 mA Multiplied by Input LOW U.L. Shown on Data Sheet; V_{IN} = 0.3 V
		0.5 U.L.			-0.8			
		n U.L.			n(-1.6)			
I_{OS}[6]	Output Short Circuit Current		-2.5		-25	mA	Max	V_{OUT} = 0 V

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. For definitions of symbols and terminology please see Section 2.
3. Unless otherwise stated on individual data sheets.
4. Typical characteristics refer to T_A = +25°C and V_{CC} = +5.0 V.
5. Min and Max refer to the values listed in the table of recommended operating conditions.
6. For testing I_{OS}, the use of high speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

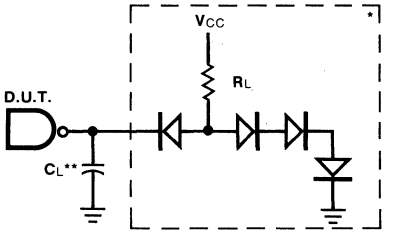
AC LOADING AND WAVEFORMS

Figure 3-1 shows the ac test load configuration used for circuits of the 54/74, 54/74H and 54/74S families having totem-pole outputs. The diodes and resistor are not used for testing circuits of the 54/74LS, 9XXX, 93XX, 93H, 93S, 93L, 96XX or 96LS families. *Figure 3-2* shows the test load configuration for open-collector outputs. For SSI gates, R_L and C_L values are listed in the table below. For flip-flops and MSI, R_L and C_L values are listed in the column headings of the ac tables on the data sheets. *Figure 3-3* shows the test circuit for measuring Enable and Disable times of 3-state outputs; R_L and C_L values are given in the column headings of the ac table in the data sheet, except in certain tests they are superceded by R_L or C_L values listed in the Test Conditions column of the same table.

A pulse generator signal swing of 0 V to +3.0 V, terminated at the test socket, is recommended for ac testing. A 1.0 MHz square wave is recommended for most propagation delay tests, with rise and fall times of 2.5 ns for S-TTL, 10 ns for LP-TTL and 6.0 ns for circuits of other families. The generator PRR must necessarily be increased for testing f_{max} and decreased for testing one-shot pulse widths. Two pulse generators are usually required for testing such parameters as set-up time, hold time, recovery time, etc.

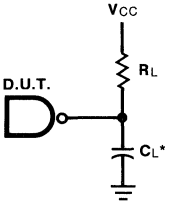
AC LOADS FOR SSI GATES

SSI DEVICES	AC TEST	54/74		54H/74H		54S/74S		54LS/74LS	
		C_L	R_L	C_L	R_L	C_L	R_L	C_L	R_L
'01, '03, '05	t_{PLH}	15 pF	4 kΩ	25 pF	280 Ω	15 pF	280 Ω	15 pF	2 kΩ
'12, '22	t_{PHL}	15 pF	400 Ω	25 pF	280 Ω	15 pF	280 Ω	15 pF	2 kΩ
'09, '15, '65	t_{PLH}/t_{PHL}	15 pF	400 Ω			15 pF	280 Ω	15 pF	2 kΩ
'06, '07, '16, '17	t_{PLH}/t_{PHL}	15 pF	110 Ω						
'26	t_{PLH}/t_{PHL}	15 pF	1 kΩ					15 pF	2 kΩ
'28, '33, '37, '38	t_{PLH}/t_{PHL}	45 pF	133 Ω					50 pF	667 Ω
'40, '140	t_{PLH}/t_{PHL}	15 pF	133 Ω	25 pF	93 Ω	50 pF	93Ω	50 pF	667 Ω
'125, '126, '365	$t_{PLH, HL, ZL, ZH}$	50 pF	400 Ω					50 pF	667 Ω
'366, '367, '368	$t_{PHZ, LZ}$	5 pF	400 Ω					5 pF	667 Ω
'134	t_{PLH}/t_{PHL}					15 pF	280 Ω		
	t_{PZH}/t_{PZL}					50 pF	280 Ω		
	t_{PHZ}/t_{PLZ}					50 pF	280 Ω		
All Standard Gates with Totem Pole Outputs	t_{PLH}/t_{PHL}	15 pF	400 Ω	25 pF	280 Ω	15 pF	280 Ω	15 pF	—



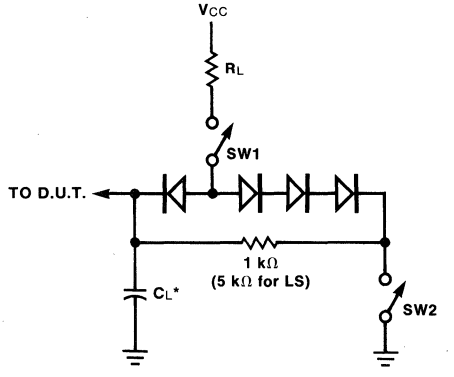
*Not Used for LS-TTL
**Includes Jig and Probe Capacitance

Fig. 3-1 Test Load for Totem-Pole Outputs in Bi-State Mode



*Includes Jig and Probe Capacitance

Fig. 3-2 Test Load for Open-Collector Outputs



PARAMETER	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

*Includes Jig and Probe Capacitance

Fig. 3-3 Enable and Disable Test Loads for 3-State Outputs

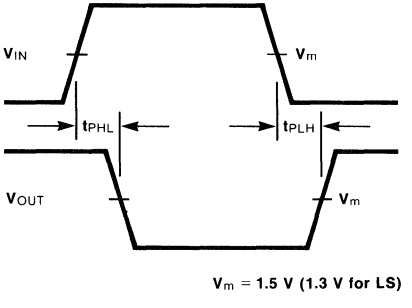


Fig. 3-4. Waveform for Inverting Functions

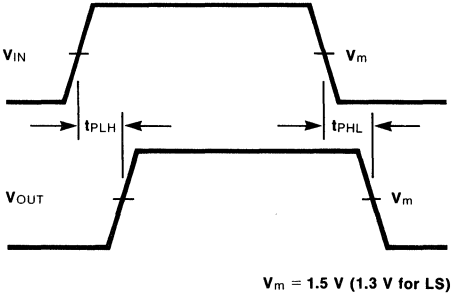


Fig. 3-5 Waveform for Non-Inverting Functions

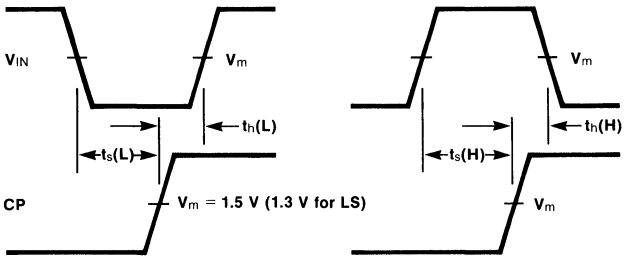


Fig. 3-6 Set-up and Hold Times, Rising-Edge Clock

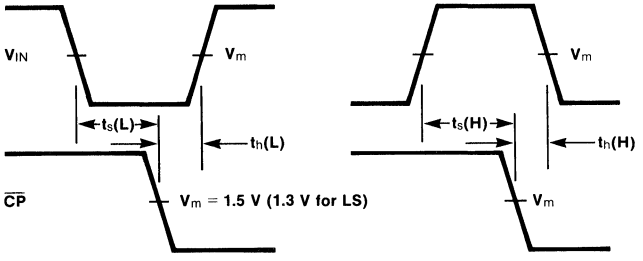


Fig. 3-7 Set-up and Hold Times, Falling-Edge Clock

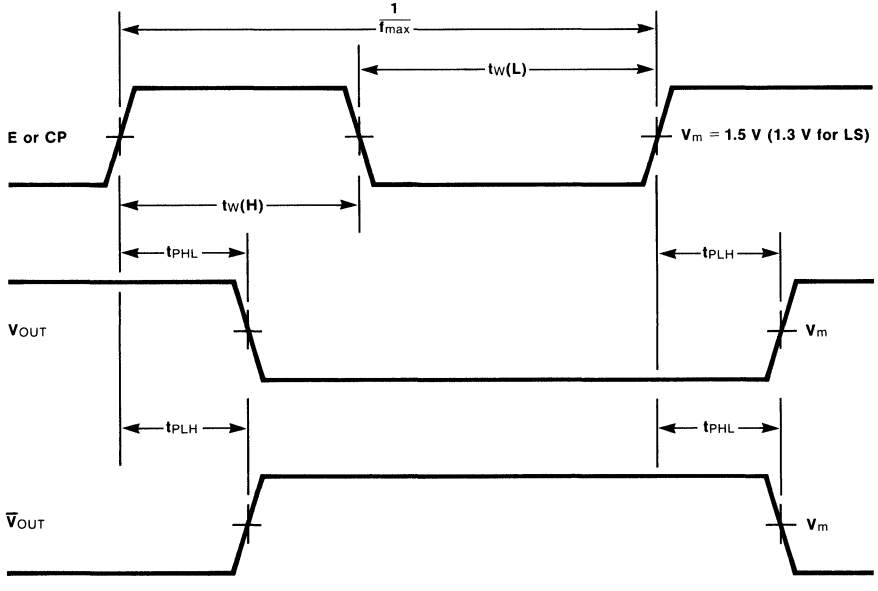


Fig. 3-8 Propagation Delays from Rising-Edge Clock or Enable

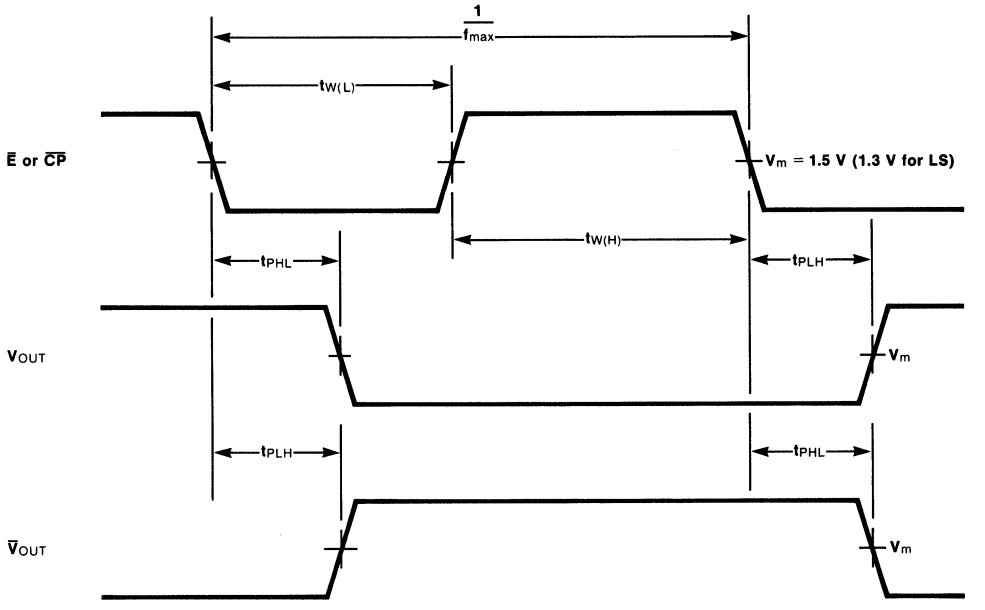


Fig. 3-9 Propagation Delays from Falling-Edge Clock or Enable

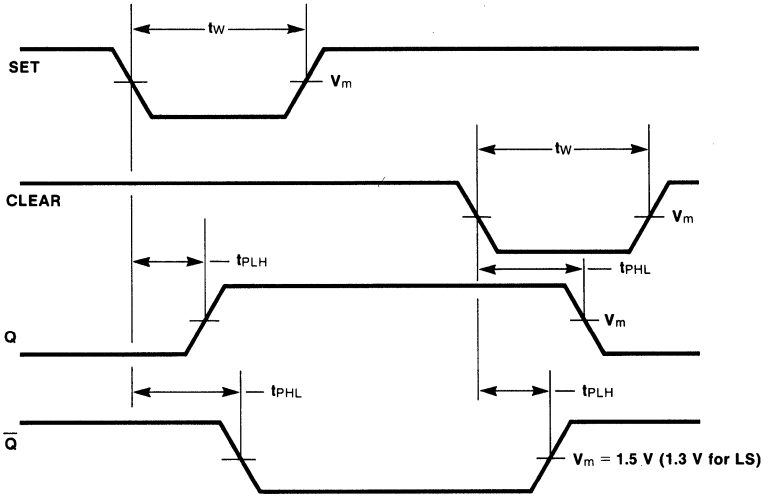


Fig. 3-10 Propagation Delays from Set and Clear (or Reset)

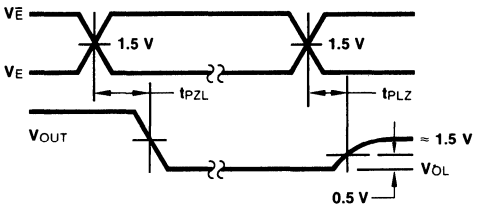


Fig. 3-11 3-State Output LOW Enable and Disable Times

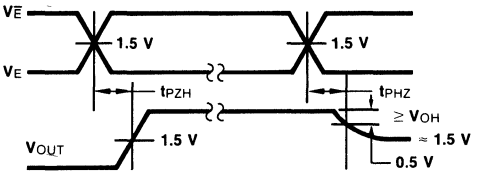


Fig. 3-12 3-State Output HIGH Enable and Disable Times

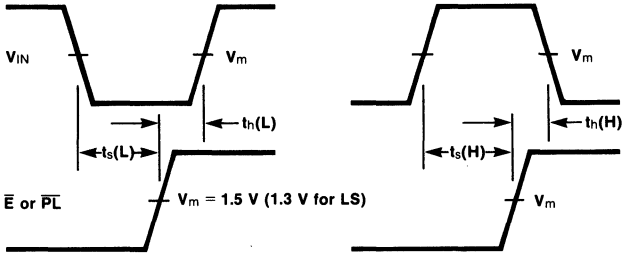


Fig. 3-13 Setup and Hold Times to Active LOW Enable or Parallel Load

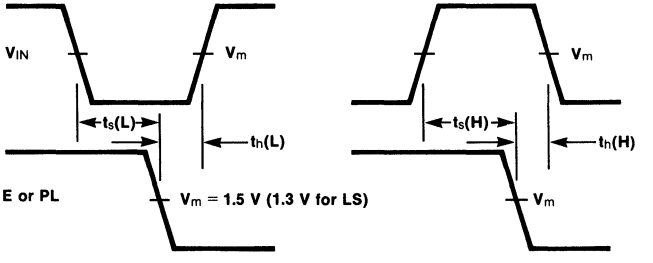
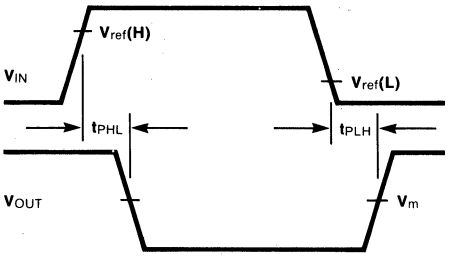


Fig. 3-14 Setup and Hold Times to Active HIGH Enable or Parallel Load



PARAMETER	FAMILY		
	54/74	54LS/74LS	54S/74S
$V_{ref}(H)$	1.7 V	1.6 V	1.8 V
$V_{ref}(L)$	0.9 V	0.8 V	1.2 V
V_m	1.5 V	1.3 V	1.5 V

Fig. 3-15 Waveforms for Schmitt Trigger Devices

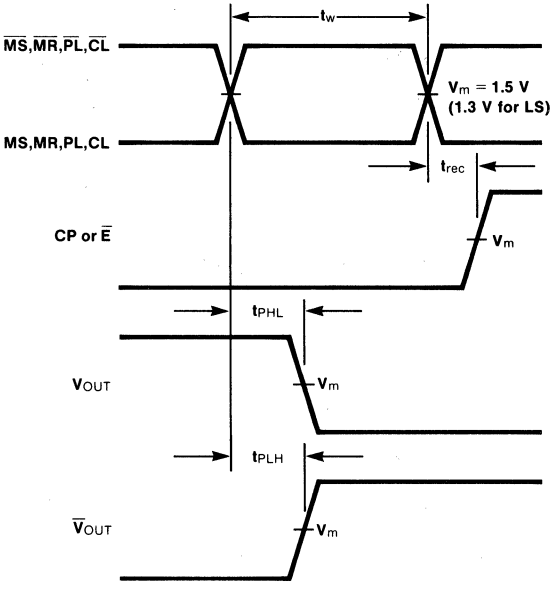


Fig. 3-16 Asynchronous Set, Reset, Parallel Load or Clear, Active Rising Edge Clock or Active LOW Enable

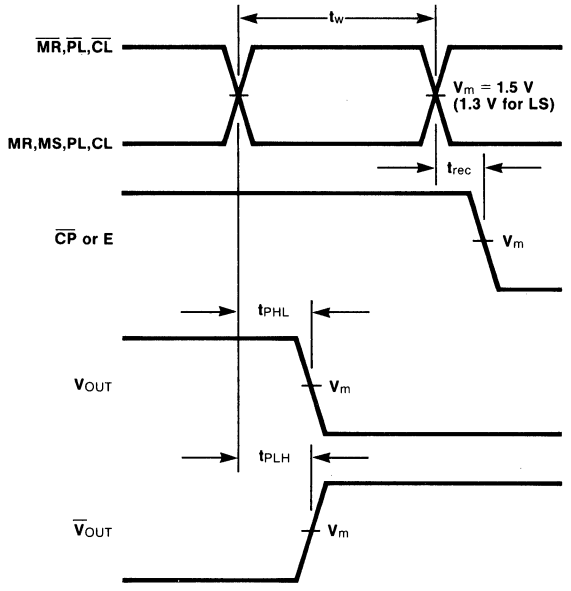


Fig. 3-17 Asynchronous Set, Reset, Parallel Load or Clear, Active Falling Edge Clock or Active HIGH Enable

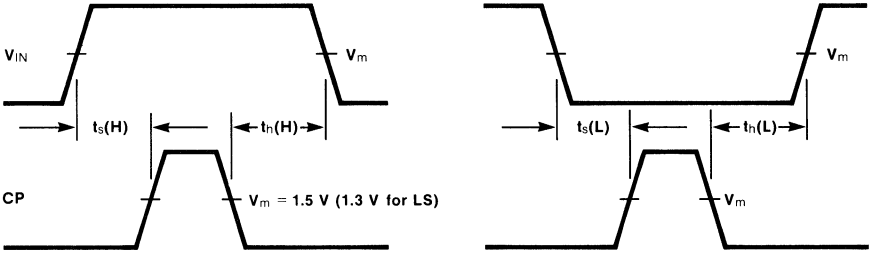


Fig. 3-18 Setup and Hold Times, Active HIGH Clock

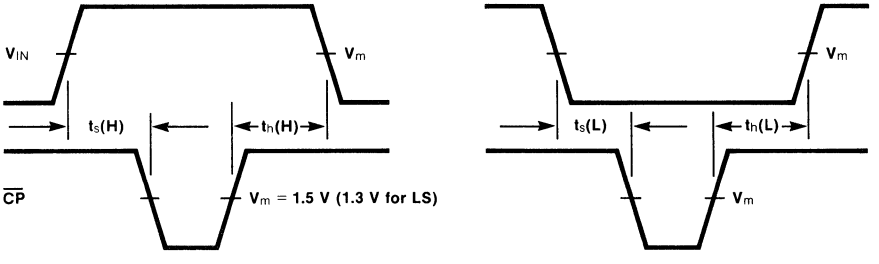


Fig. 3-19 Setup and Hold Times, Active LOW Clock

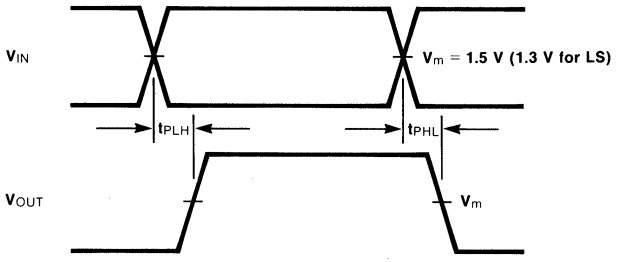


Fig. 3-20 Whether Response is Inverting or Non-Inverting Depends on Specific Truth Table Conditions

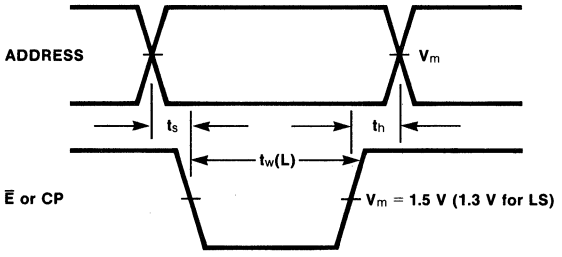
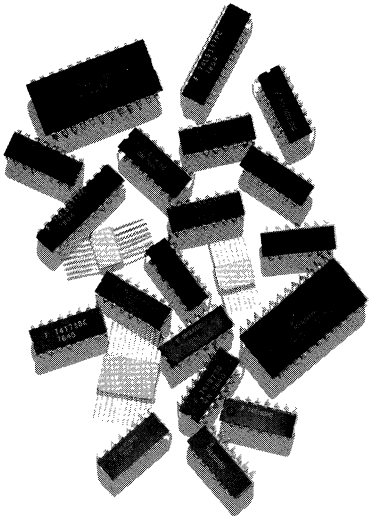


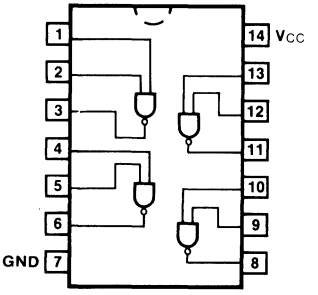
Fig. 3-21 Storage Address Setup and Hold Times



54/7400
54H/74H00
54S/74S00
54LS/74LS00

QUAD 2-INPUT NAND GATE

CONNECTION DIAGRAMS
PINOUT A

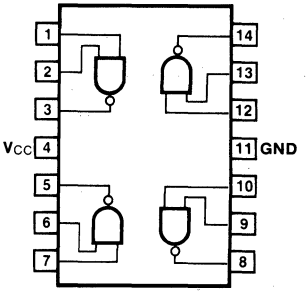


4

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7400PC, 74H00PC 74LS00PC, 74S00PC		9A
Ceramic DIP (D)	A	7400DC, 74H00DC 74LS00DC, 74S00DC	5400DM, 54H00DM 54LS00DM, 54S00DM	6A
Flatpak (F)	A	74LS00FC, 74S00FC	54LS00FM, 54S00FM	3I
	B	7400FC, 74H00FC	5400FM, 54H00FM	

PINOUT B



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply		8.0		16.8		16		1.6	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}	Current		22		40		36		4.4		V_{IN} = Open	
t_{PLH}	Propagation Delay		22		10	2.0	4.5		10	ns	Figs. 3-1, 3-4	
t_{PHL}			15		10	2.0	5.0		10			

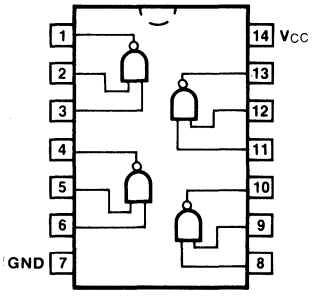
*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54/7401
54H/74H01

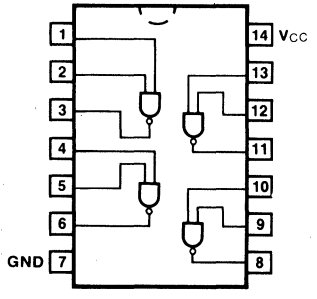
QUAD 2-INPUT NAND GATE
(With Open-Collector Output)

CONNECTION DIAGRAMS

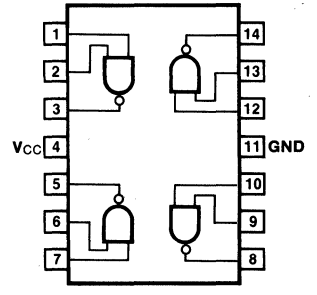
PINOUT A



PINOUT B



PINOUT C



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7401PC		9A
	B	74H01PC		
Ceramic DIP (D)	A	7401DC	5401DM	6A
	B	74H01DC	54H01DM	
Flatpak (F)	C	7401FC, 74H01FC	5401FM, 54H01FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25
Outputs	OC**/10	OC**/12.5

DC AND AC CHARACTERISTICS: See Section 3*

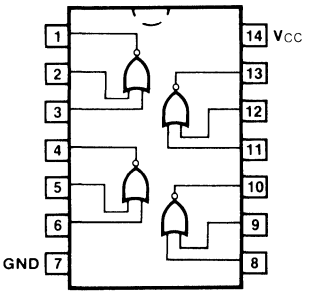
SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply		8.0		10	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}	Current		22		40		V_{IN} = Open	
t_{PLH}	Propagation Delay		45		15	ns	Figs. 3-2, 3-4	
t_{PHL}			15		12			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

**OC — Open Collector

54/7402
54S/74S02
54LS/74LS02
QUAD 2-INPUT NOR GATE

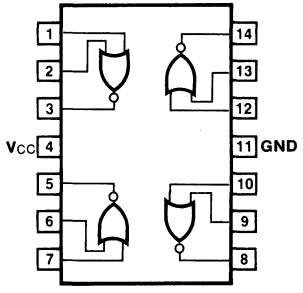
CONNECTION DIAGRAMS
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7402PC, 74LS02PC 74S02PC		9A
Ceramic DIP (D)	A	7402DC, 74LS02DC 74S02DC	5402DM, 54LS02DM 54S02DM	6A
Flatpak (F)	A	74LS02FC, 74S02FC	54LS02FM, 54S02FM	3I
	B	7402FC	5402FM	

PINOUT B



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Outputs	20/10	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

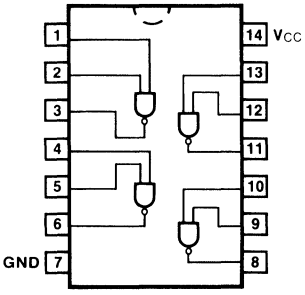
SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply Current		16		29		3.2	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			27		45		5.4		V_{IN} = Open	
t_{PLH}	Propagation Delay		15	2.0	5.5		10	ns	Figs. 3-1, 3-4	
t_{PHL}			15	2.0	5.5		10			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54/7403
54S/74S03
54LS/74LS03

QUAD 2-INPUT NAND GATE
(With Open-Collector Output)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7403PC, 74S03PC 74LS03PC		9A
Ceramic DIP (D)	A	7403DC, 74S03DC 74LS03DC	5403DM, 54S03DM 54LS03DM	6A
Flatpak (F)	A	7403FC, 74S03FC 74LS03FC	5403FM, 54S03FM 54LS03FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Outputs	OC**/10	OC**/12.5	OC**/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply Current		8.0		13.2		1.6	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			22		36		4.4		V_{IN} = Open	
t_{PLH}	Propagation Delay		45	2.0	7.5		22	mA	Figs. 3-2, 3-4	
t_{PHL}			15	2.0	7.0		18			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
**OC — Open Collector

54/7404
54H/74H04
54S/74S04
54S/74S04A
54LS/74LS04
HEX INVERTER

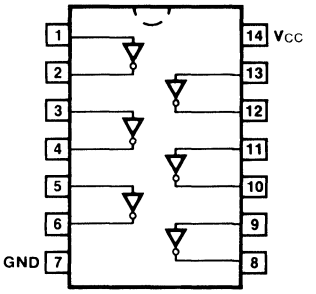
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7404PC, 74H04PC 74S04PC, 74S04APC 74LS04PC		9A
Ceramic DIP (D)	A	7404DC, 74H04DC 74S04DC, 74S04ADC 74LS04DC	5404DM, 54H04DM 54S04DM, 54S04ADM 54LS04DM	6A
Flatpak (F)	A	74S04FC, 74S04AFC 74LS04FC	54S04FM, 54S04AFM 54LS04FM	3I
	B	7404FC, 74H04FC	5404FM, 54H04FM	

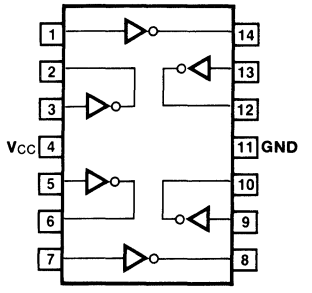
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

CONNECTION DIAGRAMS
PINOUT A



PINOUT B



DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CCH}	Power Supply		12		26		24		2.4	mA	V_{IN} = Gnd, V_{CC} = Max
I_{CCL}	Power Supply		33		58		54		6.6	mA	V_{IN} = Open, V_{CC} = Max
t_{PLH}	Propagation Delay		22		10	2.0	4.5		10	ns	Fig. 3-1, 3-4
t_{PHL}	Propagation Delay		15		10	2.0	5.0		10	ns	Fig. 3-1, 3-4
t_{PLH}	Propagation Delay (54/74S04A only)					1.0	3.5			ns	Fig. 3-1, 3-4
t_{PHL}	Propagation Delay (54/74S04A only)					1.0	4.0			ns	Fig. 3-1, 3-4

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54/7405
54H/74H05
54S/74S05
54S/74S05A
54LS/74LS05

HEX INVERTER
(With Open-Collector Output)

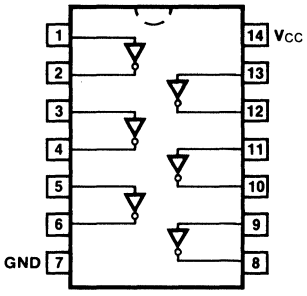
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	MILITARY GRADE V_{CC} = +5.0 V, ±10%, T_A = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	7405PC, 74H05PC 74S05PC, 74S05APC 74LS05PC		9A
Ceramic DIP (D)	A	7405DC, 74H05DC 74S05DC, 74S05ADC 74LS05DC	5405DM, 54H05DM 54S05DM, 54S05ADM 54LS05DM	6A
Flatpak (F)	A	74S05FC, 74S05AFC 74LS05FC	54S05FM, 54S05AFM 54LS05FM	3I
	B	7405FC, 74H05FC	5405FM, 54H05FM	

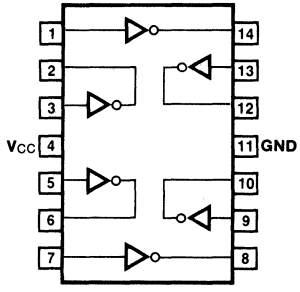
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	OC**/10	OC**/12.5	OC**/12.5	OC**/5.0 (2.5)

CONNECTION DIAGRAMS
PINOUT A



PINOUT B



DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply		12		26		19.8		2.4	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}	Current		33		58		54		6.6		V_{IN} = Open	
t_{PLH} t_{PHL}	Propagation Delay		55 15		18 15	2.0 2.0	7.5 7.0		22 18	ns	Fig. 3-2, 3-4	
t_{PLH} t_{PHL}	Propagation Delay (54S/74S05A only)					2.0 1.5	5.5 5.0			ns	Fig. 3-2, 3-4	

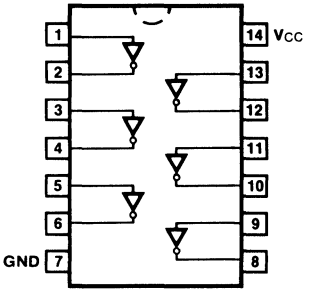
*DC limits apply over operating temperature range; AC limits apply at T_A = +25° C and V_{CC} = +5.0 V.
**OC — Collector

54/7406

HEX INVERTER BUFFER/DRIVER

(With Open-Collector High-Voltage Output)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7406PC		9A
Ceramic DIP (D)	A	7406DC	5406DM	6A
Flatpak (F)	A	7406FC	5406FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW
Inputs	1.0/1.0
Outputs	OC**/10

DC AND AC CHARATERISTICS: See Section 3*

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage	XC		0.7	V	I_{OL} = 40 mA	V_{CC} = Min, V_{IN} = V_{IH}
		XM		0.7		I_{OL} = 30 mA	
		XC, XM		0.4		I_{OL} = 16 mA	
I_{OH}	Output HIGH Current			0.25	mA	V_{OH} = 30 V, V_{CC} = Min, V_{IN} = V_{IL}	
I_{CCH}	Power Supply Current			48	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}				51		V_{IN} = Open	
t_{PLH} t_{PHL}	Propagation Delay			15 23	ns	Fig. 3-2, 3-4	

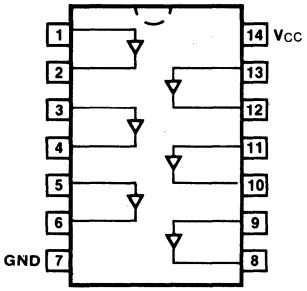
*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
**OC—Open Collector

54/7407

HEX BUFFER/DRIVER

(With Open-Collector High-Voltage Output)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7407PC		9A
Ceramic DIP (D)	A	7407DC	5407DM	6A
Flatpak (F)	A	7407FC	5407FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW
Inputs	1.0/1.0
Outputs	OC**/10

DC AND AC CHARACTERISTICS: See Section 3*

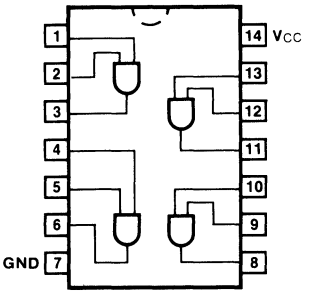
SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage	XC		0.7	V	I_{OL} = 40 mA	V_{CC} = Min, V_{IN} = V_{IL}
		XM		0.7		I_{OL} = 30 mA	
		XC, XM		0.4		I_{OL} = 16 mA	
I_{OH}	Output HIGH Current			0.25	mA	V_{OH} = 30 V, V_{CC} = Min, V_{IN} = V_{IH}	
I_{CCH}	Power Supply Current			41	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}				30		V_{IN} = Gnd	
t_{PLH} t_{PHL}	Propagation Delay			10 30	ns	Fig. 3-2, 3-5	

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
**OC—Open Collector

54/7408
54H/74H08
54S/74S08
54LS/74LS08

QUAD 2-INPUT AND GATE

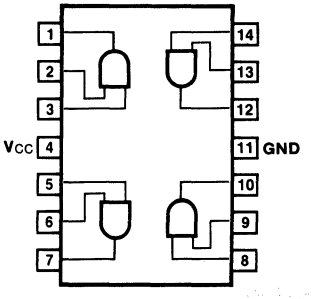
CONNECTION DIAGRAMS
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7408PC, 74H08PC 74S08PC, 74LS08PC		9A
Ceramic DIP (D)	A	7408DC, 74H08DC 74S08DC, 74LS08DC	5408DM, 54H08DM 54S08DM, 54LS08DM	6A
Flatpak (F)	A	7408FC, 74S08FC 74LS08FC	5408FM, 54S08FM 54LS08FM	3I
	B	74H08FC	54H08FM	

PINOUT B



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

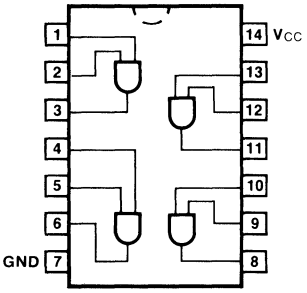
SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CCH}	Power Supply		21		40		32		4.8	mA	V_{IN} = Open; V_{CC} = Max
I_{CCL}	Current		33		64		57		8.8		V_{IN} = Gnd; V_{CC} = Max
t_{PLH}	Propagation Delay		27		12	2.5	7.0		13	ns	Fig. 3-1, 3-5
t_{PHL}			19		12	2.5	7.5		11		

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54/7409
54S/74S09
54LS/74LS09

QUAD 2-INPUT AND GATE
(With Open-Collector Output)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7409PC, 74S09PC 74LS09PC		9A
Ceramic DIP (D)	A	7409DC, 74S09DC 74LS09DC	5409DM, 54S09DM 54LS09DM	6A
Flatpak (F)	A	7409FC, 74S09FC 74LS09FC	5409FM, 54S09FM 54LS09FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Outputs	OC**/10	OC**/12.5	OC**/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

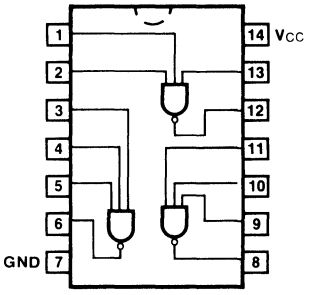
SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply Current		21		32		4.8	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}			33		57		8.8		V_{IN} = Gnd	
t_{PLH}	Propagation Delay		32	2.0	10		20	ns	Fig. 3-2, 3-5	
t_{PHL}			24	2.0	10		15			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
**OC — Open Collector

54/7410
54H/74H10
54S/74S10
54LS/74LS10

TRIPLE 3-INPUT NAND GATE

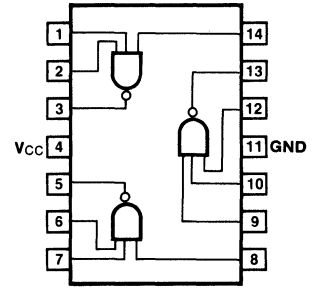
CONNECTION DIAGRAMS
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	7410PC, 74H10PC 74S10PC, 74LS10PC		9A
Ceramic DIP (D)	A	7410DC, 74H10DC 74S10DC, 74LS10DC	5410DM, 54H10DM 54S10DM, 54LS10DM	6A
Flatpak (F)	A	74S10FC, 74LS10FC	54S10FM, 54LS10FM	3I
	B	7410FC, 74H10FC	5410FM, 54H10FM	

PINOUT B



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

DC AND AC CHARATERISTICS: See Section 3*

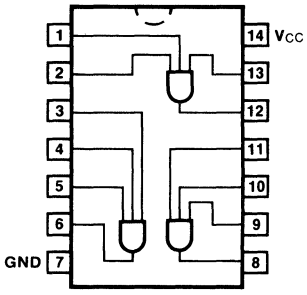
SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply		6.0		12.6		12		1.2	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}	Current		16.5		30		27		3.3		V_{IN} = Open	
t_{PLH}	Propagation Delay		22		10	2.0	4.5		15	ns	Fig. 3-1, 3-4	
t_{PHL}			15		10	2.0	5.0		15			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25° C and V_{CC} = +5.0 V.

54/7411
54H/74H11
54S/74S11
54LS/74LS11

TRIPLE 3-INPUT AND GATE

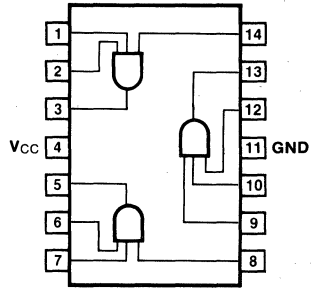
CONNECTION DIAGRAMS
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7411PC, 74H11PC 74S11PC, 74LS11PC		9A
Ceramic DIP (D)	A	7411DC, 74H11DC 74S11DC, 74LS11DC	5411DM, 54H11DM 54S11DM, 54LS11DM	6A
Flatpak (F)	A	74S11FC, 74LS11FC	54S11FM, 54LS11FM	3I
	B	7411FC, 74H11FC	5411FM, 54H11FM	

PINOUT B



INPUT LOADING/FAN-OUT: See Section 3 for U.L definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply	15		30			24		3.6	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}	Current	24		48			42		6.6		V_{IN} = Gnd	
t_{PLH}	Propagation Delay	27		12		2.5	7.0		13	ns	Figs. 3-1, 3-5	
t_{PHL}		19		12		2.5	7.5		11			

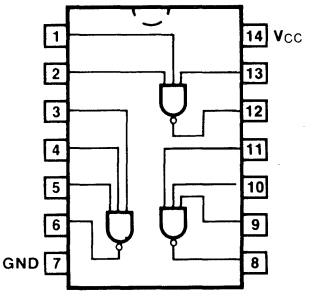
*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54/7412

TRIPLE 3-INPUT NAND GATE

(With Open-Collector Output)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7412PC		9A
Ceramic DIP (D)	A	7412DC	5412DM	6A
Flatpak (F)	A	7412FC	5412FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW
Inputs	1.0/1.0
Outputs	OC**/10

DC AND AC CHARACTERISTICS: See Section 3*

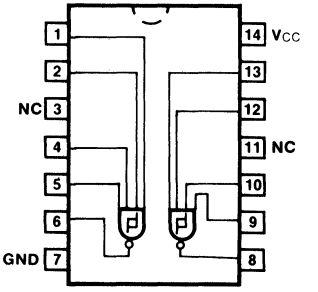
SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply Current		6.0	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			16.5		V_{IN} = Open	
t_{PLH}	Propagation Delay		45	ns	Figs. 3-2, 3-4	
t_{PHL}			15			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

**OC — Open Collector

54/7413
54LS/74LS13
DUAL 4-INPUT SCHMITT TRIGGER

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	7413PC, 74LS13PC		9A
Ceramic DIP (D)	A	7413DC, 74LS13DC	5413DM, 54LS13DM	6A
Flatpak (F)	A	7413FC, 74LS13FC	5413FM, 54LS13FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	20/10	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
V_{T+}	Positive-going Threshold Voltage	1.5	2.0	1.5	2.0	V	V_{CC} = +5.0 V	
V_{T-}	Negative-going Threshold Voltage	0.6	1.1	0.6	1.1	V	V_{CC} = +5.0 V	
V_{T+}—V_{T-}	Hysteresis Voltage	0.4		0.4		V	V_{CC} = +5.0 V	
I_{T+}	Input Current at Positive-going Threshold	-0.65**		-0.14**		mA	V_{CC} = +5.0 V, V_{IN} = V_{T+}	
I_{T-}	Input Current at Negative-going Threshold	-0.85**		-0.18**		mA	V_{CC} = +5.0 V, V_{IN} = V_{T-}	
I_{OS}	Output Short Circuit Current	-18	-55	-20	-100	mA	V_{CC} = Max	
I_{CCH}	Power Supply Current		23		6.0	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			32		7.0		V_{IN} = Open	
t_{PLH} t_{PHL}	Propagation Delay		27 22		22 27	ns	Fig. 3-1, 3-15	

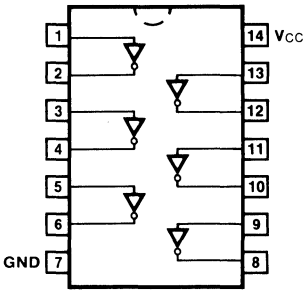
*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V. **Typical Value

54/7414
54LS/74LS14
HEX SCHMITT TRIGGER INVERTER

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7414PC, 74LS14PC		9A
Ceramic DIP (D)	A	7414DC, 74LS14DC	5414DM, 54LS14DM	6A
Flatpak (F)	A	7414FC, 74LS14FC	5414FM, 54LS14FM	3I

CONNECTION DIAGRAM
PINOUT A



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	20/10	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

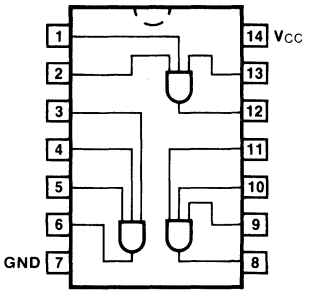
SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
V_{T+}	Positive-going Threshold Voltage	1.5	2.0	1.5	2.0	V	V_{CC} = +5.0 V
V_{T-}	Negative-going Threshold Voltage	0.6	1.1	0.6	1.1	V	V_{CC} = +5.0 V
$V_{T+} - V_{T-}$	Hysteresis Voltage	0.4		0.4		V	V_{CC} = +5.0 V
I_{T+}	Input Current at Positive-going Threshold	-0.43**		-0.14**		mA	V_{CC} = +5.0 V, V_{IN} = V_{T+}
I_{T-}	Input Current at Negative-going Threshold	-0.56**		-0.18**		mA	V_{CC} = +5.0 V, V_{IN} = V_{T-}
I_{IL}	Input LOW Current		-1.2		-0.4	mA	V_{CC} = Max, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current	-18	-55	-20	-100	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CCH}	Power Supply Current		36		16	mA	V_{IN} = Gnd; V_{CC} = Max
I_{CCL}			60		21		V_{IN} = Open; V_{CC} = Max
t_{PLH}	Propagation Delay		22		22	ns	Figs. 3-1, 3-15
t_{PHL}			22		22		

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V. **Typical Value

54S/74S15
54LS/74LS15

TRIPLE 3-INPUT AND GATE
(With Open-Collector Outputs)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S15PC, 74LS15PC		9A
Ceramic DIP (D)	A	74S15DC, 74LS15DC	54S15DM, 54LS15DM	6A
Flatpak (F)	A	74S15FC, 74LS15FC	54S15FM, 54LS15FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.25/1.25	0.5/0.25
Outputs	OC**/12.5	OC**/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply		19.5		3.6	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}	Current		42		6.6		V_{IN} = Gnd	
t_{PLH} t_{PHL}	Propagation Delay		8.5 9.0		20 15	ns	Figs. 3-2, 3-5	

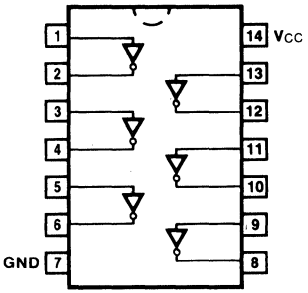
*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
**OC—Open Collector

54/7416

HEX INVERTER BUFFER/DRIVER

(With Open-Collector High-Voltage Output)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7416PC		9A
Ceramic DIP (D)	A	7416DC	5416DM	6A
Flatpak (F)	A	7416FC	5416FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW
Inputs	1.0/1.0
Outputs	OC**/10

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage	XC		0.7	V	I_{OL} = 40 mA	V_{CC} = Min V_{IN} = V_{IH}
		XM		0.7		I_{OL} = 30 mA	
		XC, XM		0.4		I_{OL} = 16 mA	
I_{OH}	Output HIGH Current			0.25	mA	V_{OH} = 15 V, V_{CC} = Min V_{IN} = V_{IL}	
I_{CCH}	Power Supply Current			48	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}				51		V_{IN} = Open	
t_{PLH} t_{PHL}	Propagation Delay			15 23	ns	Figs. 3-2, 3-4	

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

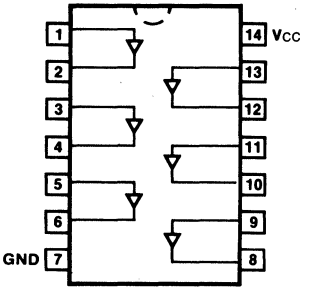
**OC — Open Collector

54/7417

HEX BUFFER/DRIVER

(With Open-Collector High-Voltage Output)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	7417PC		9A
Ceramic DIP (D)	A	7417DC	5417DM	6A
Flatpak (F)	A	7417FC	5417FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW
Inputs	1.0/1.0
Outputs	OC**/10

DC AND AC CHARACTERISTICS: See Section 3*

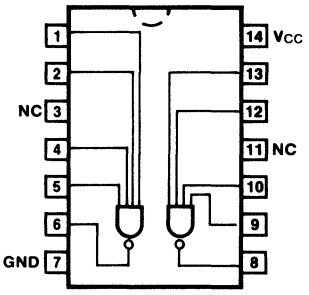
SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage	XC		0.7	V	I_{OL} = 40 mA	V_{CC} = Min, V_{IN} = V_{IL}
		XM		0.7		I_{OL} = 30 mA	
		XC, XM		0.4		I_{OL} = 16 mA	
I_{OH}	Output HIGH Current			0.25	mA	V_{OH} = 15 V, V_{CC} = Min, V_{IN} = V_{IH}	
I_{CCH}	Power Supply Current			41	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}				30		V_{IN} = Gnd	
t_{PLH} t_{PHL}	Propagation Delay			10 30	ns	Figs. 3-2, 3-5	

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
**OC—Open Collector

54/7420
54H/74H20
54S/74S20
54LS/74LS20

DUAL 4-INPUT NAND GATE

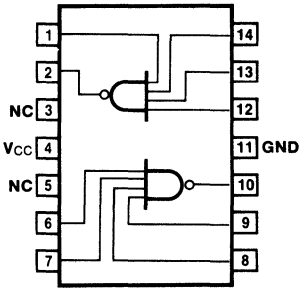
CONNECTION DIAGRAMS
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7420PC, 74H20PC 74S20PC, 74LS20PC		9A
Ceramic DIP (D)	A	7420DC, 74H20DC 74S20DC, 74LS20DC	5420DM, 54H20DM 54S20DM, 54LS20DM	6A
Flatpak (F)	A	74S20FC, 74LS20FC	54S20FM, 54LS20FM	3I
	B	7420FC, 74H20FC	5420FM, 54H20FM	

PINOUT B



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

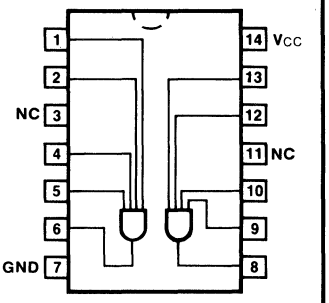
SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply	4.0		8.4		8.0		0.8		mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}	Current	11		20		18		2.2			V_{IN} = Open	
t_{PLH} t_{PHL}	Propagation Delay	22 15		10 10		2.0 2.0	4.5 5.0	15 15		ns	Figs. 3-1, 3-4	

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54/7421
54H/74H21
54LS/74LS21

DUAL 4-INPUT POSITIVE AND GATE

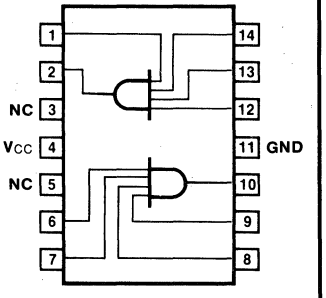
CONNECTION DIAGRAMS
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7421PC, 74H21PC 74LS21PC		9A
Ceramic DIP (D)	A	7421DC, 74H21DC 74LS21DC	5421DM, 54H21DM 54LS21DM	6A
Flatpak (F)	A	7421FC, 74LS21FC	5421FM, 54LS21FM	3I
	B	74H21FC	54H21FM	

PINOUT B



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

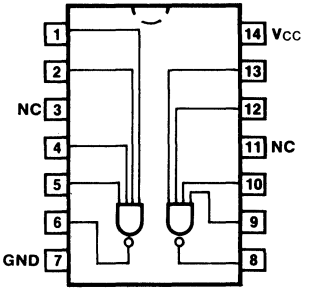
SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply Current		10		20		2.4	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}			16		32		4.4		V_{IN} = Gnd	
t_{PLH}	Propagation Delay		27		12		15	ns	Figs. 3-1, 3-5	
t_{PHL}			19		12		15			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

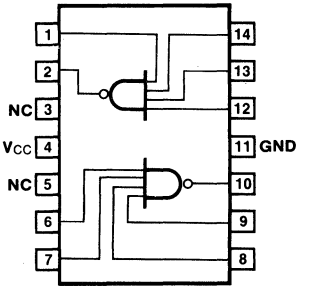
54/7422
54H/74H22
54S/74S22
54LS/74LS22

DUAL 4-INPUT NAND GATE
(With Open-Collector Output)

CONNECTION DIAGRAMS
PINOUT A



PINOUT B



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7422PC, 74H22PC 74S22PC, 74LS22PC		9A
Ceramic DIP (D)	A	7422DC, 74H22DC 74S22DC, 74LS22DC	5422DM, 54H22DM 54S22DM, 54LS22DM	6A
Flatpak (F)	A	7422FC, 74S22FC 74LS22FC	5422FM, 54S22FM 54LS22FM	3I
	B	74H22FC	54H22FM	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	OC**/10	OC**/12.5	OC**/12.5	OC**/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply		4.0		5.0		6.6		0.8	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}	Current		11		20		18		2.2		V_{IN} = Open	
t_{PLH}	Propagation Delay		45		15	2.0	7.5		22	ns	Figs. 3-2, 3-4	
t_{PHL}			15		12	2.0	7.0		18			

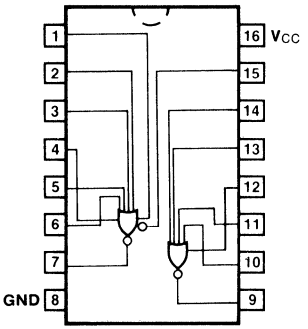
*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
**OC — Open Collector

54/7423

EXPANDABLE DUAL 4-INPUT NOR GATE

(With Strobe)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7423PC		9B
Ceramic DIP (D)	A	7423DC	5423DM	6B
Flatpak (F)	A	7423FC	5423FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. defintions

PINS	54/74 (U.L.) HIGH/LOW
Data Inputs	1.0/1.0
Strobe Inputs	4.0/4.0
Outputs	20/10

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE: Expander Inputs Open

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS	
I_{CCH} I_{CCL}	Power Supply Current		16 19	mA	V_{IN} = Gnd V_{IN} = Open	V_{CC} = Max

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE: Using Expander Inputs

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS	
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q	XM		1.1	V	I_1 = 0.41 mA	I_{OL} = 16 mA
		XC		1.0		I_1 = 0.62 mA	R_1 = 0 Ω
V_{OH}	Output HIGH Voltage	XM	2.4		V	I_1 = 0.15 mA, I_2 = -0.15 mA	I_{OH} = -400 μA
		XC	2.4			I_1 = 0.27 mA, I_2 = -0.27 mA	
V_{OL}	Output LOW Voltage	XM		0.4	V	I_1 = 0.3 mA, R_1 = 138 Ω	I_{OL} = 16 mA
		XC		0.4		I_1 = 0.43 mA, R_1 = 130 Ω	
I_X	Expander Current	XM		-2.9	V	V_1 = 0.4 V, I_{OL} = 16 mA	
		XC		-3.1			

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

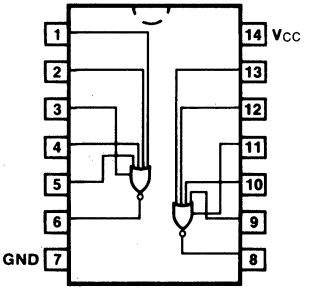
SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
t_{PLH}	Propagation Delay		22	ns	Expander Pins Open
t_{PHL}			15		Figs. 3-1, 3-4

54/7425

DUAL 4-INPUT NOR GATE

(With Strobe)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG OUT
Plastic DIP (P)	A	7425PC		9A
Ceramic DIP (D)	A	7425DC	5425DM	6A
Flatpak (F)	A	7425FC	5425FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW
Data Inputs	1.0/1.0
Strobe Inputs	4.0/4.0
Outputs	20/10

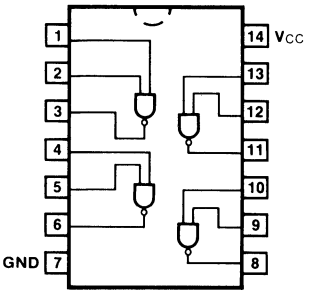
DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply Current		16	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			19		V_{IN} = Open	
t_{PLH}	Propagation Delay		22	ns	Figs. 3-1, 3-4	
t_{PHL}			15			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

7426
54LS/74LS26
QUAD 2-INPUT NAND BUFFER
(With Open-Collector Outputs)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7426PC, 74LS26PC		9A
Ceramic DIP (D)	A	7426DC, 74LS26DC	54LS26DM	6A
Flatpak (F)	A	7426FC, 74LS26FC	54LS26FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	OC**/10	OC**/5.0 (2.5)

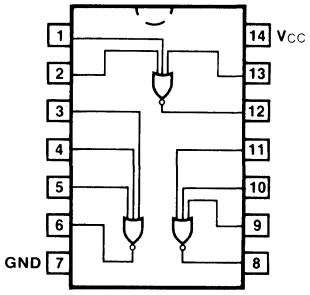
DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{OH}	Output HIGH Current		50		50	μA	V_{OH} = 12 V	V_{CC} = Min
			1000		1000		V_{OH} = 15 V	V_{IN} = V_{IL}
I_{CCH}	Power Supply Current		8.0		1.6	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			22		4.4		V_{IN} = Open	
t_{PLH}	Propagation Delay		24		22	ns	Figs. 3-2, 3-4	
t_{PHL}			17		18			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
**OC — Open Collector

54/7427
54LS/74LS27
TRIPLE 3-INPUT NOR GATE

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7427PC, 74LS27PC		9A
Ceramic DIP (D)	A	7427DC, 74LS27DC	5427DM, 54LS27DM	6A
Flatpak (F)	A	7427FC, 74LS27FC	5427FM, 54LS27FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	20/10	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

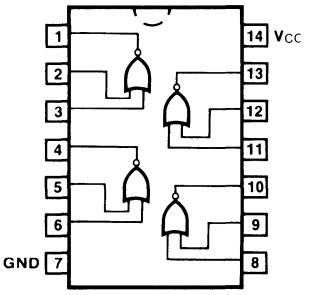
SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS	
		Min	Max	Min	Max			
I_{CCH}	Power Supply Current		16		4.0	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			26		6.8		V_{IN} = Open	
t_{PLH}	Propagation Delay		15		13	ns	Figs. 3-1, 3-4	
t_{PHL}			11		13			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54LS/74LS28

QUAD 2-INPUT NOR BUFFER

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS28PC		9A
Ceramic DIP (D)	A	74LS28DC	54LS28DM	6A
Flatpak (F)	A	74LS28FC	54LS28FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74LS (U.L.) HIGH/LOW
Inputs	0.5/0.25
Outputs	30/15 (7.5)

DC AND AC CHARACTERISTICS: See Section 3*

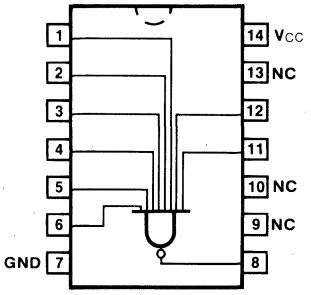
SYMBOL	PARAMETER	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply Current		3.6	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			13.8		V_{IN} = Open	
t_{PLH} t_{PHL}	Propagation Delay		20 20	ns	Figs. 3-1, 3-4	

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54/7430
54H/74H30
54S/74S30
54LS/74LS30

8-INPUT NAND GATE

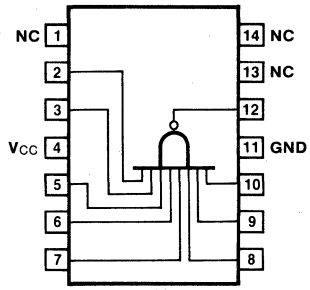
CONNECTION DIAGRAMS
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7430PC, 74H30PC 74S30PC, 74LS30PC		9A
Ceramic DIP (D)	A	7430DC, 74H30DC 74S30DC, 74LS30DC	5430DM, 54H30DM 54S30DM, 54LS30DM	6A
Flatpak (F)	A	74S30FC, 74LS30FC	54S30FM, 54LS30FM	3I
	B	7430FC, 74H30FC	5430FM, 54H30FM	

PINOUT B



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

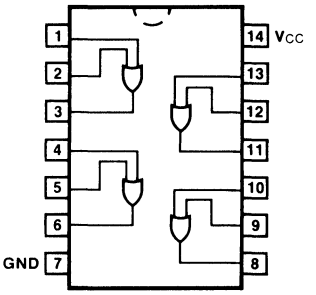
SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply		2.0		4.2		5.0		0.5	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}	Current		6.0		10		10		1.1		V_{IN} = Open	
t_{PLH}	Propagation Delay		22		10	2.0	6.0		12	ns	Figs. 3-1, 3-4	
t_{PHL}			15		12	2.0	7.0		20			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54/7432
54S/74S32
54LS/74LS32

QUAD 2-INPUT OR GATE

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7432PC, 74S32PC 74LS32PC		9A
Ceramic DIP (D)	A	7432DC, 74S32DC 74LS32DC	5432DM, 54S32DM 54LS32DM	6A
Flatpak (F)	A	7432FC, 74S32FC 74LS32FC	5432FM, 54S32FM 54LS32FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Outputs	20/10	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3 for U.L. definitions

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply Current		22		32		6.2	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}			38		68		9.8		V_{IN} = Gnd	
t_{PLH}	Propagation Delay		15	2.0	7.0		15	ns	Figs. 3-1, 3-5	
t_{PHL}			22	2.0	7.0		15			

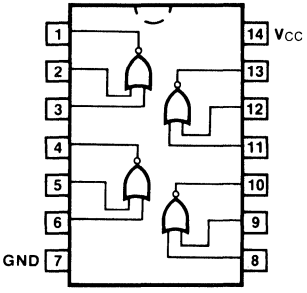
*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54LS/74LS33

QUAD 2-INPUT NOR BUFFER

(With Open-Collector Outputs)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS33PC		9A
Ceramic DIP (D)	A	74LS33DC	54LS33DM	6A
Flatpak (F)	A	74LS33FC	54LS33FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74LS (U.L.) HIGH/LOW
Inputs	0.5/0.25
Outputs	OC**/15 (7.5)

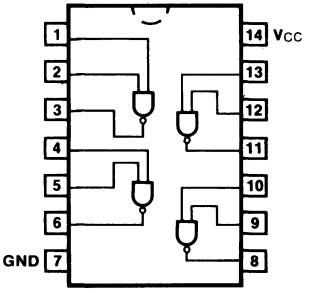
DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER		54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage	XM, XC		0.4	V	I_{OL} = 12 mA	V_{CC} = Min
		XC		0.5		I_{OL} = 24 mA	V_{IN} = 2.0 V
I_{OH}	Output HIGH Current			250	µA	V_{OH} = 5.5 V, V_{CC} = Min, V_{IN} = V_{IL}	
I_{CCH}	Power Supply Current			3.6	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}				13.8		V_{IN} = Open	
t_{PLH}	Propagation Delay			22	ns	Figs. 3-2, 3-4	
t_{PHL}				22			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
**OC — Open Collector

54/7437
54LS/74LS37
QUAD 2-INPUT NAND BUFFER

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°c to +125°C	PKG TYPE
Plastic DIP (P)	A	7437PC, 74LS37PC		9A
Ceramic DIP (D)	A	7437DC, 74LS37DC	5437DM, 54LS37DM	6A
Flatpak (F)	A	7437FC, 74LS37FC	5437FM, 54LS37FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	30/30	30/15 (7.5)

DC AND AC CHARACTERISTICS: See Section 3*

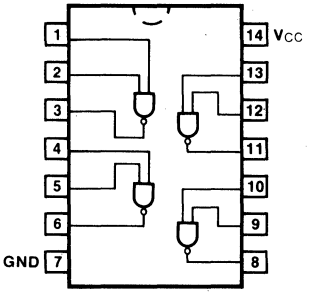
SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	XM	2.4		2.5		V	V_{CC} = Max, I_{OH} = -1.2 mA V_{IN} = V_{IL}	
		XC	2.4		2.7				
V_{OL}	Output LOW Voltage	XM, XC		0.4			V	I_{OL} = 48 mA	V_{CC} = Min V_{IN} = 2.0 V
		XM				0.4		I_{OL} = 12 mA	
		XC				0.5		I_{OL} = 24 mA	
I_{OS}	Output Short Circuit Current	XM	-20	-70	-30	-130	mA	V_{CC} = Min, V_{OUT} = 0 V	
		XC	-18	-70	-30	-130			
I_{CCH} I_{CCL}	Power Supply Current			15.5 54		2.0 12	mA	V_{IN} = Gnd V_{IN} = Open	V_{CC} = Max
t_{PLH} t_{PHL}	Propagation Delay			22 15		20 20	ns	Figs. 3-1, 3-4	

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54/7438
54LS/74LS38

QUAD 2-INPUT NAND BUFFER
(With Open-Collector Output)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	7438PC, 74LS38PC		9A
Ceramic DIP (D)	A	7438DC, 74LS38DC	5438DM, 54LS38DM	6A
Flatpak (F)	A	7438FC, 74LS38FC	5438FM, 54LS38FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	OC**/30	OC**/15 (7.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage		0.4			V	V_{IN} = 2.0 V, V_{CC} = Min, I_{OL} = 48 mA	
I_{OH}	Output HIGH Current				250	µA	V_{OH} = 5.5 V, V_{CC} = Min, V_{IN} = V_{IL}	
I_{CCH}	Power Supply Current		8.5		2.0	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			54		12		V_{IN} = Open	
t_{PLH}	Propagation Delay		22		22	ns	Figs. 3-2, 3-4	
t_{PHL}			18		22			

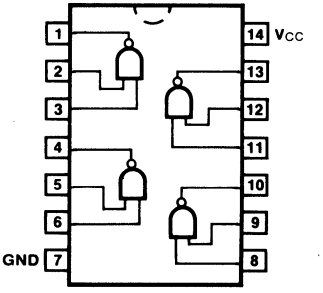
*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
**OC — Open Collector

54/7439

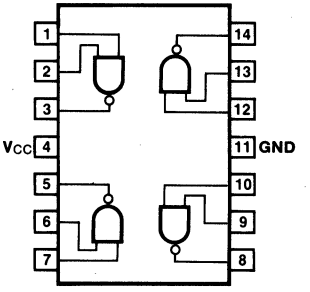
QUAD 2-INPUT NAND BUFFER

(With Open-Collector Output)

CONNECTION DIAGRAMS
PINOUT A



PINOUT B



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE: V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7439PC		9A
Ceramic DIP (D)	A	7439DC	5439DM	6A
Flatpak (F)	B	7439FC	5439FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW
Inputs	1.0/1.0
Outputs	OC**/30

DC AND AC CHARACTERISTICS: See Section 3*

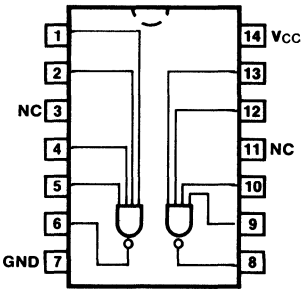
SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage	XM, XC		0.4	V	I_{OL} = 48 mA	V_{CC} = Min, V_{IN} = 2.0 V, Other Inputs = 2.0 V
		XM, XC		0.5		I_{OL} = 60 mA	
		XC		0.6		I_{OL} = 80 mA	
I_{CCH}	Power Supply Current			8.5	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}				54		V_{IN} = Open	
t_{PLH}	Propagation Delay			22	ns	Figs. 3-2, 3-4	
t_{PHL}				18			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
**OC — Open Collector

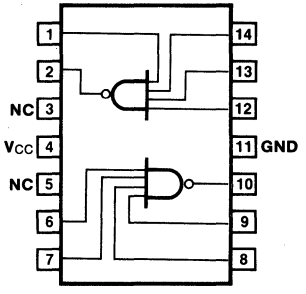
54/7440
54H/74H40
54S/74S40
54LS/74LS40

DUAL 4-INPUT NAND BUFFER

CONNECTION DIAGRAMS
PINOUT A



PINOUT B



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7440PC, 74H40PC 74S40PC, 74LS40PC		9A
Ceramic DIP (D)	A	7440DC, 74H40DC 74S40DC, 74LS40DC	5440DM, 54H40DM 54S40DM, 54LS40DM	6A
Flatpak (F)	A	74S40FC, 74LS40FC	54S40FM, 54LS40FM	3I
	B	7440FC, 74H40FC	5440FM, 54H40FM	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	2.5/2.5	2.5/2.5	0.5/0.25
Outputs	30/30	37.5/37.5	70/37.5	30/15 (7.5)

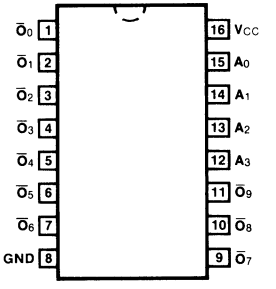
DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	XC	-18	-70	-40	-125	-50	-225			mA	V_{CC} = Max, V_{OUT} = 0 V
		XM	-20	-70	-40	-125	-50	-225				
I_{CCH}	Power Supply Current			8.0		16		18		1.0	mA	V_{IN} = Gnd; V_{CC} = Max
I_{CCL}				27		40		44		6.0		V_{IN} = Open; V_{CC} = Max
t_{PLH}	Propagation Delay			22		12		6.5		24	ns	Figs. 3-1, 3-4
t_{PHL}				15		12		6.5		24		

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54/7442A • 54LS/74LS42
54/7443A • 54/7444A
1-of-10 DECODER

CONNECTION DIAGRAM
PINOUT A



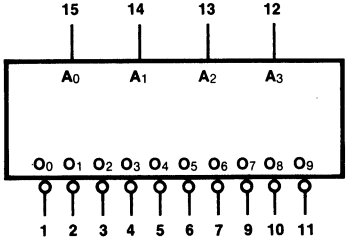
DESCRIPTION - The '42, '43 and '44 are multipurpose decoders. For any valid input combination, one and only one output is LOW. For all invalid input combinations all outputs are HIGH. The '42 accepts four BCD inputs and provides ten mutually exclusive outputs; the '43 accepts four lines of EXCESS-3 encoded data and provides ten mutually exclusive outputs; the '44 accepts four lines of EXCESS-3 Gray encoded data and provides ten mutually exclusive totem pole outputs.

- **MULTIFUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **DEMULTIPLEXING CAPABILITY**
- **FULLY TTL AND CMOS COMPATIBLE**

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	7442APC, 74LS42PC 7443APC, 7444APC		9B
Ceramic DIP (D)	A	7442ADC, 74LS42DC 7443ADC, 7444ADC	5442ADM, 54LS42DM 5443ADM, 5444ADM	6B
Flatpak (F)	A	7442AFC, 74LS42FC 7443AFC, 7444AFC	5442AFM, 54LS42FM 5443AFM, 5444AFM	4L

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	BCD Inputs ('42)	1.0/1.0	0.5/0.25
$A_0 - A_3$	EXCESS-3 Inputs ('43)	1.0/1.0	
$A_0 - A_3$	EXCESS-3 GRAY Inputs ('44)	1.0/1.0	
$\overline{O}_0 - \overline{O}_0$	Decimal Outputs (Active LOW)	20/10	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — Logically, the '42, '43 and '44 differ only in their input codes. The '42 accepts the standard 8421 BCD code. The '43 accepts the EXCESS-3 decimal code while the '44 accepts the EXCESS-3 Gray code. For any input combination within the assigned ten states, only one output is LOW, as shown in the Truth Table. For all invalid input combinations, all ten outputs are HIGH.

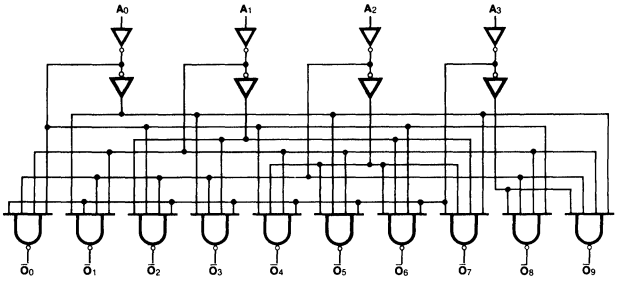
The '42 can be used as a conventional 1-of-8 decoder by treating the most significant input A_3 as an active LOW Enable. Similarly, it can be used as an 8-output demultiplexer by using A_3 as the data input.

TRUTH TABLE

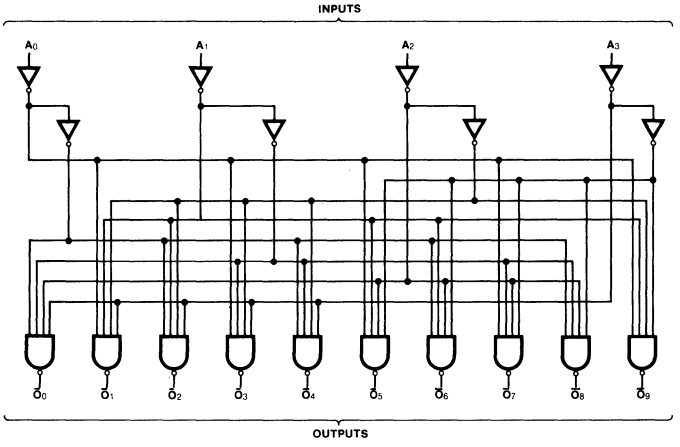
'42A • 'LS42 BCD INPUT				'43A EXCESS-3 INPUT				'44A EXCESS-3 GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
A_3	A_2	A_1	A_0	A_3	A_2	A_1	A_0	A_3	A_2	A_1	A_0	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$	$\overline{O}_8$	$\overline{O}_9$
L	L	L	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	L	L	L	H	H	L	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	H	L	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	L	L	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
H	H	H	L	L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

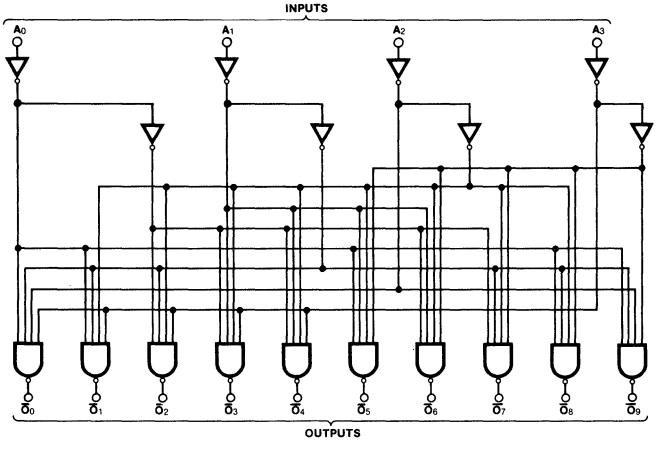
LOGIC DIAGRAMS
'42A • 'LS42



'43A



'44A



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74		54/74LS		UNITS	CONDITIONS
			Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current	XM	-20	-55	-20	-100	mA	V_{CC} = Max
		XC	-18	-55	-20	-100		
I_{CC}	Power Supply Current	XM		41		12	mA	V_{CC} = Max
		XC		56		12		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω		54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$, 2 Levels		25 25		18 25	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$, 3 Levels		30 30		20 27	ns	Figs. 3-1, 3-20

54/7445

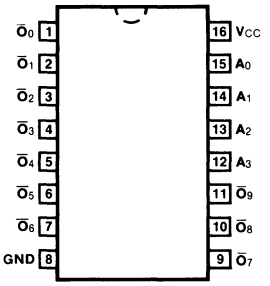
1-OF-10 DECODER/DRIVER

(With Open-Collector Outputs)

DESCRIPTION — The '45 decoder/drivers are designed to accept BCD inputs and provide appropriate outputs to drive 10-digit numerical displays. All outputs remain OFF for all invalid binary input conditions. These devices are designed for use as indicator/relay drivers or as open-collector logic circuit drivers. Each of the high breakdown (30 V) output transistors will sink up to 80 mA of current.

- **OPEN-COLLECTOR OUTPUTS**
- **80 mA CURRENT SINKING**
- **30 V GUARANTEED BREAKDOWN**

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

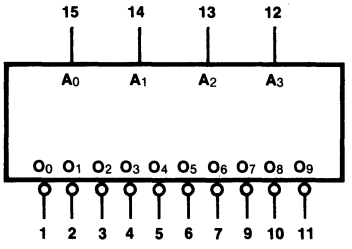
PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	7445PC		9B
Ceramic DIP (D)	A	7445DC	5445DM	7B
Flatpak (F)	A	7445FC	5445FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
A_0 — A_3	BCD Inputs	1.0/1.0
$\overline{O}_0$ — $\overline{O}_9$	Outputs (Active LOW)	OC*/12.5

*OC — Open Collector

LOGIC SYMBOL



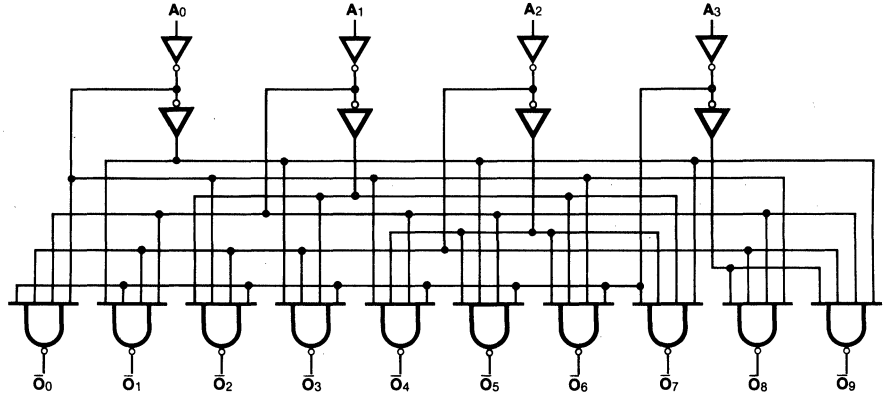
V_{CC} = Pin 16
Gnd = Pin 8

TRUTH TABLE

INPUTS				OUTPUTS									
A_0	A_1	A_2	A_3	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$	$\overline{O}_8$	$\overline{O}_9$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage			0.9	V	V_{CC} = Min, I_{OL} = 80 mA
I_{OH}	Output HIGH Current			250	μA	V_{CC} = Max, V_{OH} = 30 V
I_{CC}	Power Supply Current	XC		70	mA	V_{CC} = Max
		XM		62		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 100 Ω Min	54/74 C_L = 15 pF R_L = 100 Ω Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$		50 50	ns	Figs. 3-2, 3-20

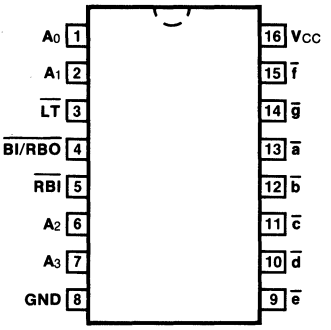
54/7446A • 54/7447A
54LS/74LS47

BCD TO 7-SEGMENT DECODER/DRIVER

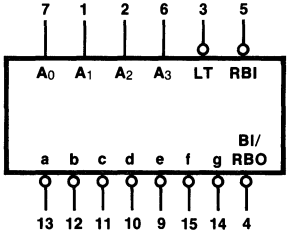
DESCRIPTION — The '46A, '47A and 'LS47 accept four lines of BCD (8421) input data, generate their complements internally and decode the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 40 mA (24 mA for the 'LS47) in the ON (LOW) state and withstand 15 V (30 V for the '46A) in the OFF (HIGH) state with a maximum leakage current of 250 μA. Auxiliary inputs provide blanking, lamp test and cascadable zero-suppression fuctions. Also see the 'LS247 data sheet.

- **OPEN-COLLECTOR OUTPUTS**
- **DRIVE INDICATOR SEGMENTS DIRECTLY**
- **CASCADABLE ZERO-SUPPRESSION CAPABILITY**
- **LAMP TEST INPUT**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0° C to +70° C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	7446APC, 7447APC 74LS47PC		9B
Ceramic DIP)D)	A	7446ADC, 7447ADC 74LS47DC	5446ADM, 5447ADM 54LS47DM	7B
Flatpak (F)	A	7446AFC, 7447AFC 74LS47FC	5446AFM, 5447AFM 54LS47FM	4L

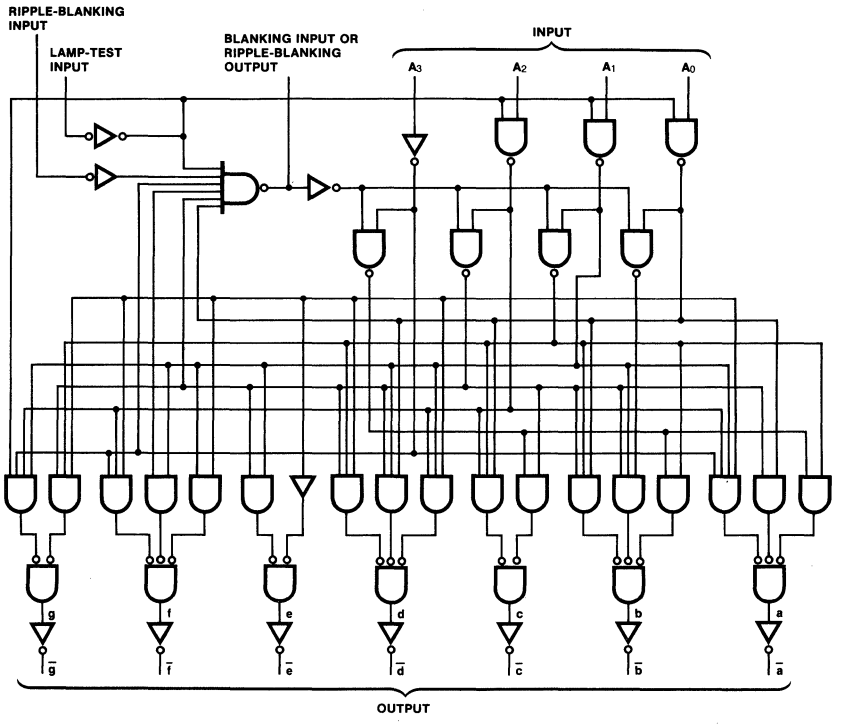
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{A_0} - \overline{A_3}$	BCD Inputs	1.0/1.0	0.5/0.25
$\overline{RBI}$	Ripple Blanking Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{LT}$	Lamp Test Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{BI/RBO}$	Blanking Input (Active LOW) or	-/2.5	-/0.75
	Ripple Blanking Output (Active LOW)	5.0/5.0	1.25/2.0 (1.0)
$\overline{a} - \overline{g}$	Segment Outputs (Active LOW)	OC*/25	OC*/15 (7.5)

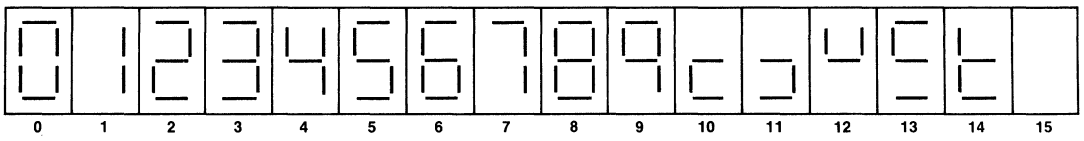
*OC — Open Collector

FUNCTIONAL DESCRIPTION — The '46A, '47A and 'LS47 decode the input data in the pattern indicated in the Truth Table and the segment identification illustration. If the input data is decimal zero, a LOW signal applied to the $\overline{RBI}$ blanks the display and causes a multidigit display. For example, by grounding the $\overline{RBI}$ of the highest order decoder and connecting its $\overline{BI/RBO}$ to $\overline{RBI}$ of the next lowest order decoder, etc., leading zeros will be suppressed. Similarly, by grounding $\overline{RBI}$ of the lowest order decoder and connecting its $\overline{BI/RBO}$ to $\overline{RBI}$ of the next highest order decoder, etc., trailing zeros will be suppressed. Leading and trailing zeros can be suppressed simultaneously by using external gates, ie: by driving $\overline{RBI}$ of an intermediate decoder from an OR gate whose inputs are $\overline{BI/RBO}$ of the next highest and lowest order decoders. $\overline{BI/RBO}$ also serves as an unconditional blanking input. The internal NAND gate that generates the $\overline{RBO}$ signal has a resistive pull-up, as opposed to a totem pole, and thus $\overline{BI/RBO}$ can be forced LOW by enternal means, using wired-collector logic. A LOW signal thus applied to $\overline{BI/RBO}$ turns off all segment outputs. This blanking feature can be used to control display intensity by varying the duty cycle of the blanking signal. A LOW signal applied to $\overline{LT}$ turns on all segment outputs, provided that $\overline{BI/RBO}$ is not forced LOW.

LOGIC DIAGRAM



NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS



TRUTH TABLE

DECIMAL OR FUNCTION	INPUTS							OUTPUTS							NOTE
	$\overline{LT}$	$\overline{RBI}$	A_3	A_2	A_1	A_0	$\overline{BI/RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	1
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	1
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	2
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	3
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	4

NOTES:

(1) $\overline{BI/RBO}$ is wire-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking or a decimal 0 is not desired. X = input may be HIGH or LOW.

(2) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a HIGH level regardless of the state of any other input condition.

(3) When ripple-blanking input ($\overline{RBI}$) and inputs A_0, A_1, A_2 and A_3 are LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

(4) When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{OH}	Output HIGH Current	'46		250			μA	V_{OH} = 30 V	V_{CC} = Max
	OFF State at $\overline{a}$—$\overline{g}$	'47		250		250		V_{OH} = 15 V	
I_{OS}	Output Short Circuit Current at $\overline{BI/RBO}$			-4.0	-0.3	-2.0	mA	V_{CC} = Max	
I_{CC}	Power Supply Current	XM		85		13	mA	V_{CC} = Max	
		XC		103		13			

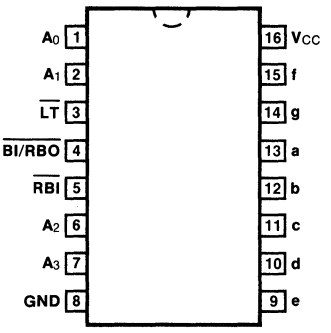
AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 120 Ω Min	54/74 Max	54/74LS C_L = 15 pF R_L = 665 Ω Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{a}$—$\overline{g}$		100 100		100 100	ns	Figs. 3-2, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{RBI}$ to $\overline{a}$—$\overline{f}$		100 100		100 100	ns	Figs. 3-2, 3-4 $\overline{LT}$ = HIGH, A_0 - A_3 = LOW

4

54/7448
54LS/74LS48
BCD TO 7-SEGMENT DECODER

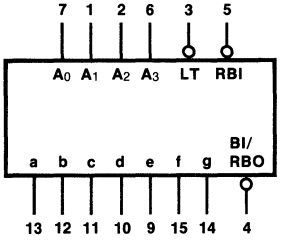
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '48 translates four lines of BCD (8421) input data into the 7-segment numeral code and provides seven corresponding outputs having pull-up resistors, as opposed to totem pole pull-ups. These outputs can serve as logic signals, with a HIGH output corresponding to a lighted lamp segment, or can provide a 1.3 mA base current to npn lamp driver transistors. Auxiliary inputs provide lamp test, blanking and cascadable zero-suppression functions.

The '48 decodes the input data in the pattern indicated in the Truth Table and the segment identification illustration. For a detailed description of the blanking, lamp test and zero-suppression functions refer to the '46A data sheet, but note that the segment output states of the '48 are the logical inverse of those of the '46A. Also see the 'LS248 data sheet.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

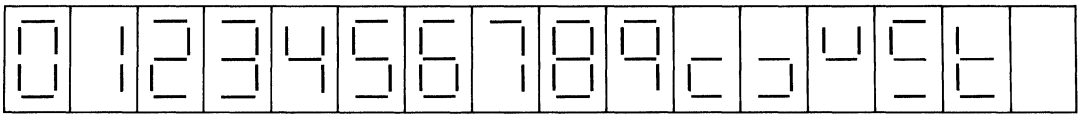
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7448PC, 74LS48PC		9B
Ceramic DIP (D)	A	7448DC, 74LS48DC	5448DM, 54LS48DM	7B
Flatpak (F)	A	7448FC, 74LS48FC	5448FM, 54LS48FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{A_0} - \overline{A_3}$	BCD Inputs	1.0/1.0	0.5/0.25
$\overline{RBI}$	Ripple Blanking Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{LT}$	Lamp Test Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{BI/RBO}$	Blanking Input (Active LOW) or	-/2.5	-/0.75
	Ripple Blanking Output (Active LOW)	5.0/5.0	1.25/2.0 (1.0)
a — g	Segment Outputs (Active HIGH)	10/4.0	2.5/3.75 (1.25)

NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS



TRUTH TABLE

DECIMAL OR FUNCTION	INPUTS							OUTPUTS							NOTE
	$\overline{LT}$	$\overline{RBI}$	A_3	A_2	A_1	A_0	$\overline{BI/RBO}$	a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
$\overline{BI}$	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
$\overline{RBI}$	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
$\overline{LT}$	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

NOTES:

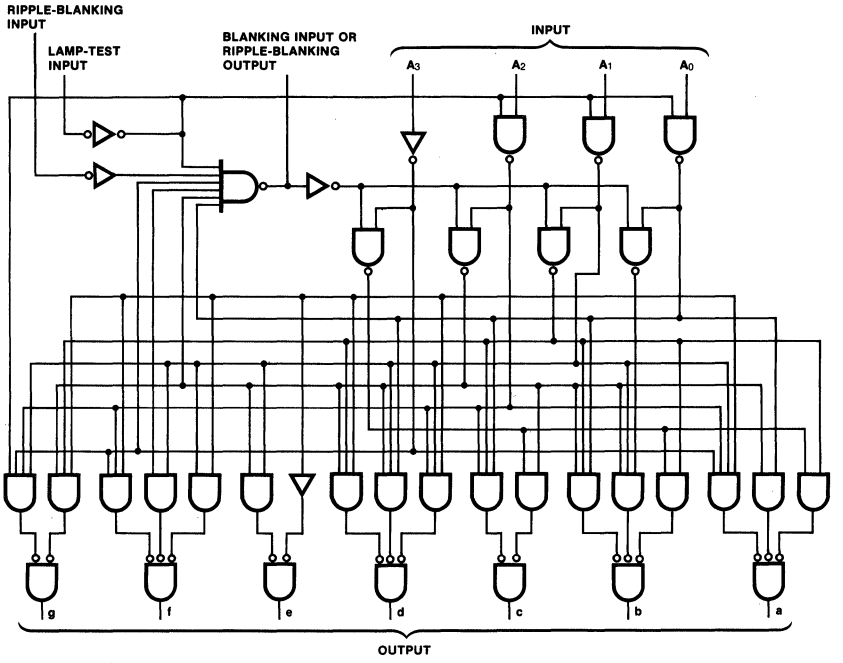
(1) $\overline{BI/RBO}$ is wired-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

(2) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level, regardless of the state of any other input condition.

(3) When ripple-blanking input ($\overline{RBI}$) and inputs A_0, A_1, A_2, and A_3 are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a LOW level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

(4) When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a HIGH level.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

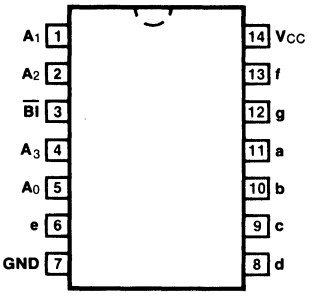
SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OH}	Output HIGH Current at a—g		-1.3		-1.3		mA	V_{CC} = Min, V_{OUT} = 0.85 V
I_{OS}	Output Short Circuit Current at $\overline{BI}/\overline{RBO}$			-4.0	-0.3	-2.0	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current	XM		76		38	mA	V_{CC} = Max All Inputs = 4.5 V
		XC		90		38		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 1 kΩ Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_n to a—g		100 100		100 100	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{RBI}$ to a—f		100 100		100 100	ns	Figs. 3-1, 3-5 $\overline{LT}$=HIGH, A_0—A_3=HIGH

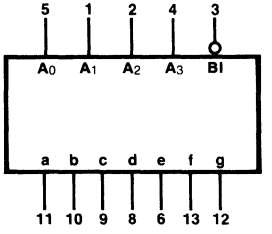
54/7449
54LS/74LS49
BCD TO 7-SEGMENT DECODER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '49 translates four lines of BCD (8421) input data into the 7-segment numeral code as shown in the Truth Table. It has open-collector outputs and is logically the 14-pin version of the '48, without the lamp test and ripple blanking features. Also see the 'LS249 data sheet.

LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

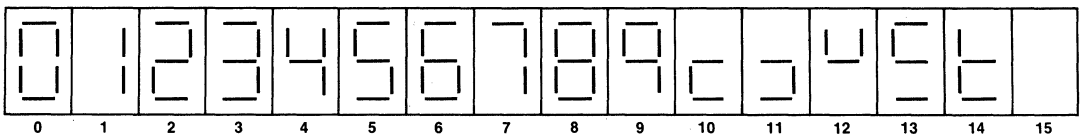
PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS49PC		9A
Ceramic DIP (D)	A	74LS49DC	54LS49DM	6A
Flatpak (F)	A	7449FC, 74LS49FC	5449FM, 54LS49FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	BCD Inputs	1.0/1.0	0.5/0.25
$\overline{BI}$	Blanking Input (Active LOW)	1.0/1.0	0.5/0.25
a — g	Segment Outputs (Active HIGH)	OC*/6.25	OC*/5.0 OC*/(2.5)

* OC — Open Collector

NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS



TRUTH TABLE

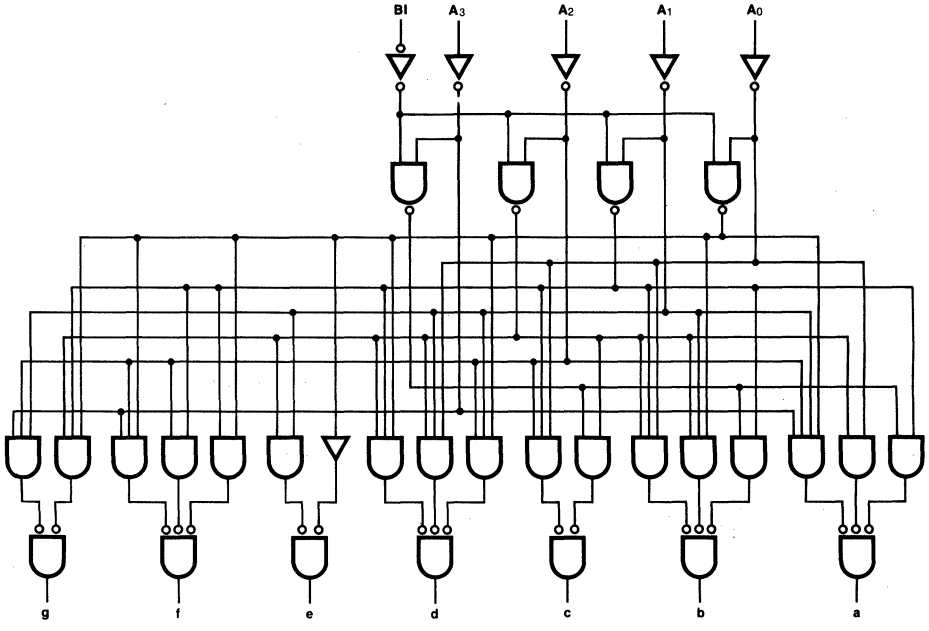
DECIMAL OR FUNCTION	INPUTS					OUTPUTS							NOTE
	A_3	A_2	A_1	A_0	$\overline{BI}$	a	b	c	d	e	f	g	
0	L	L	L	L	H	H	H	H	H	H	H	L	1
1	L	L	L	H	H	L	H	H	L	L	L	L	
2	L	L	H	L	H	H	H	L	H	H	L	H	
3	L	L	H	H	H	H	H	H	H	L	L	H	
4	L	H	L	L	H	L	H	H	L	L	H	H	
5	L	H	L	H	H	H	L	H	H	L	H	H	
6	L	H	H	L	H	L	L	H	H	H	H	H	
7	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	L	L	L	L	L	L	L	L	2

NOTES:

(1) The blanking input must be open or held at a HIGH level when output functions 0 through 15 are desired.
(2) When a LOW level is applied to the blanking input all segment outputs go to a LOW level regardless of the state of any other input condition. X = input may be HIGH or LOW.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
V_{IL}	Input LOW Voltage	XM		0.6		0.7	V	
		XC		0.8		0.8		
I_{OH}	Output HIGH Current			250		250	μA	V_{CC} = Min, V_{OH} = 5.5 V
I_{CC}	Power Supply Current	XM		47		15	mA	V_{CC} = Max, Inputs = 4.5 V
		XC		56		15		

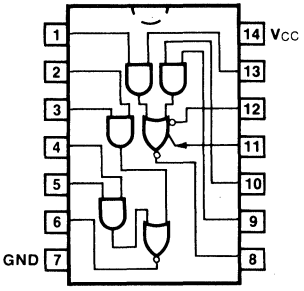
AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 665 Ω Min	54/74 C_L = 15 pF, R_L = 665 Ω Max	54/74LS C_L = 15 pF, R_L = 3 kΩ Min	54/74LS C_L = 15 pF, R_L = 3 kΩ Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_n to a—g		100 100		100 100	ns	Figs. 3-2, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{BI}$ to a—g		100 100		100 100	ns	Figs. 3-2, 3-5 R_L = 6 kΩ for 'LS49

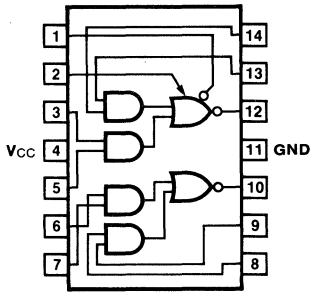
54/7450
54H/74H50

EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE

CONNECTION DIAGRAMS
PINOUT A



PINOUT B



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7450PC, 74H50PC		9A
Ceramic DIP (D)	A	7450DC, 74H50DC	5450DM, 54H50DM	6A
Flatpak (F)	B	7450FC, 74H50FC	5450FM, 54H50FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25
Outputs	20/10	12.5/12.5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE: Expander Pins Open

SYMBOL	PARAMETER	54/74		54/74H		UNITS	CONDITIONS	
		Min	Max	Min	Max			
I_{CCH}	Power Supply Current		8.0		12.8	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			14		24		V_{IN} = Open	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE: Using Expander Pins

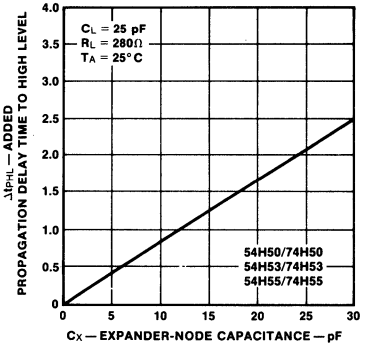
SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74H Min	54/74H Max	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	XM			2.4		V	I_1 = 320 μA I_2 = -320 μA	I_{OH} = -500 μA
		XC			2.4			I_1 = 570 μA I_2 = -570 μA	
V_{OH}	Output HIGH Voltage	XM	2.4				V	I_1 = 0.15 mA I_2 = -0.15 mA	I_{OH} = -400 mA
		XC	2.4					I_1 = 270 mA I_2 = -270 mA	
V_{OL}	Output LOW Voltage	XM				0.4	V	I_1 = 470 μA R_1 = 68 Ω	I_{OL} = 20 mA
		XC				0.4		I_1 = 600 μA R_1 = 63 Ω	
V_{OL}	Output LOW Voltage	XM		0.4			V	I_1 = 0.3 mA R_1 = 138 Ω	I_{OL} = 16 mA
		XC		0.4				I_1 = 0.43 mA R_1 = 130 Ω	
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q	XM				1.0	V	I_1 = 700 μA	I_{OL} = 20 mA R_1 = 0 Ω
		XC				1.0		I_1 = 1.1 mA	
		XM		1.1				I_1 = 0.41 mA	I_{OL} = 16 mA R_1 = 0 Ω
		XC		1.0				I_1 = 0.62 mA	
I_{INX}	Expander-Node Input Current	XM				-5.85	mA	V_X = 1.4 V, V_{CC} = Min T_A = Min	
		XC				-6.3			
I_X	Expander Current	XM		2.9			mA	V_1 = 0.4 V, I_{OL} = 16 mA V_{CC} = Min, T_A = Min	
		XC		3.1					

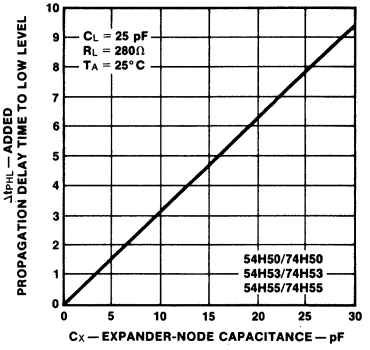
AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay		22 15		11 11	ns	Expander Pins Open Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay				11* 7.4*	ns	C_L = 25 pF R_L = 280 Ω, C_X = 15 pF

*Typical Value

ADDED PROPAGATION DELAY TIME vs EXPANDER-NODE CAPACITANCE



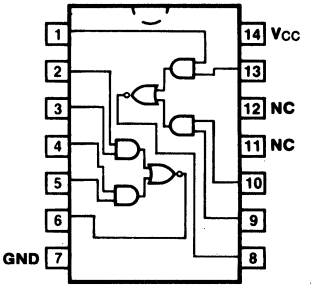


54/7451
54H/74H51
54S/74S51
54LS/74LS51

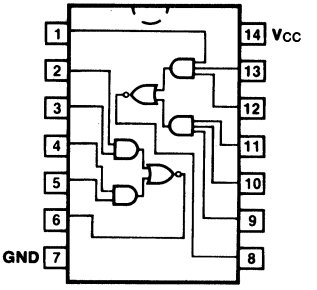
DUAL 2-WIDE, 2-INPUT AOI GATE
DUAL 2-WIDE, 2-INPUT/3-INPUT AOI GATE ('LS51)

CONNECTION DIAGRAMS

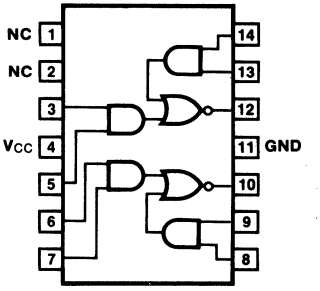
PINOUT A



PINOUT B



PINOUT C



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7451PC, 74H51PC 74S51PC		9A
	B	74LS51PC		
Ceramic DIP (D)	A	7451DC, 74H51DC 74S51DC	5451DM, 54H51DM 54S51DM	6A
	B	74LS51DC	54LS51DM	
Flatpak (F)	A	74S51FC	54S51FM	3I
	B	74LS51FC	54LS51FM	
	C	7451FC, 74H51FC	5451FM, 54H51FM	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

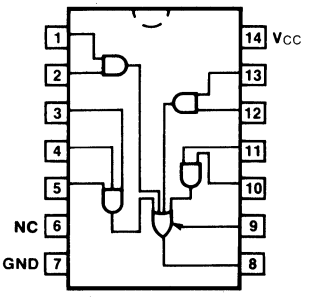
SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CCH}	Power Supply		8.0		12.8		17.8		1.6	mA	V_{IN} = Gnd; V_{CC} = Max
I_{CCL}	Current		14		24		22		2.8		V_{IN} = Open; V_{CC} = Max
t_{PLH}	Propagation Delay		22		11	2.0	5.5		20	ns	Figs. 3-1, 3-4
t_{PHL}			15		11	2.0	5.5		20		

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

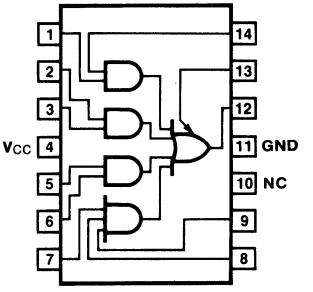
54H/74H52

EXPANDABLE 2-2-2-3-INPUT AND-OR GATE

CONNECTION DIAGRAMS
PINOUT A



PINOUT B



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74H52PC		9A
Ceramic DIP (D)	A	74H52DC	54H52DM	6A
Flatpak (F)	B	74H52FC	54H52FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74H (U.L.) HIGH/LOW
Inputs	1.25/1.25
Outputs	12.5/12.5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE: Expander Pins Open

SYMBOL	PARAMETER	54/74H Min	54/74H Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply Current		31	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}			24		V_{IN} = Gnd	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE: Using Expander Pins

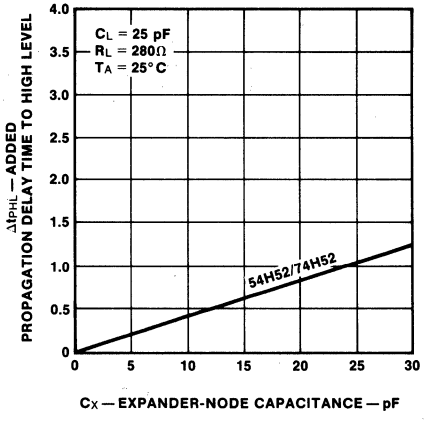
SYMBOL	PARAMETER		54/74H Min	54/74H Max	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	XM	2.4		V	T_A = -55°C	V_{CC} = Min, V_X = 1.0 V I_{OH} = -500 μA
		XC	2.4			T_A = 0 °C	
V_{OL}	Output LOW Voltage	XM		0.4	V	T_A = +125°C	V_{CC} = Min, I_{INX} = -300 μA I_{OL} = 20 mA
		XC		0.4		T_A = +70°C	
I_{INX}	Expander-Node Input Current	XM	-2.7	-4.5	mA	T_A = -55°C	V_{CC} = Min, V_X = 1.0 V, I_{OH} = -500 μA
		XC	-2.9	-5.35		T_A = 0°C	

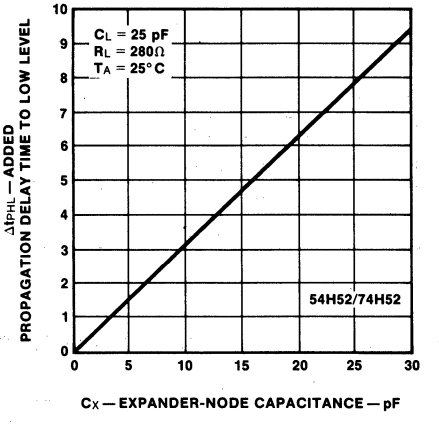
AC CHARACTERISITCS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74H Min	54/74H Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay		15 15	ns	Expander Pins Open Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay		14.8* 9.8*	ns	C_X = 15 pF

*Typical Value

ADDED PROPAGATION DELAY TIME vs EXPANDER-NODE CAPACITANCE





54/7453
54H/74H53

EXPANDABLE 4-WIDE, 2-INPUT AOI GATE ('53)
EXPANDABLE 2-2-2-3-INPUT AOI GATE ('H53)

ORDERING CODE: See Section 9

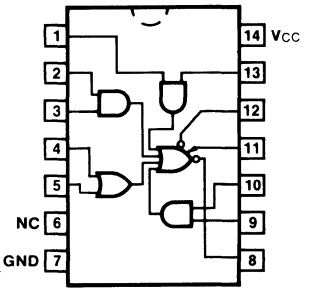
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7453PC		9A
	B	74H53PC		
Ceramic DIP (D)	A	7453DC	5453DM	6A
	B	74H53DC	54H53DM	
Flatpak (F)	C	7453FC	5453FM	3I
	D	74H53FC	54H53FM	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

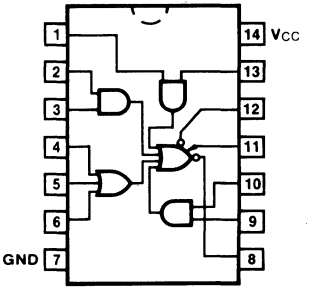
PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25
Outputs	20/10	12.5/12.5

CONNECTION DIAGRAMS

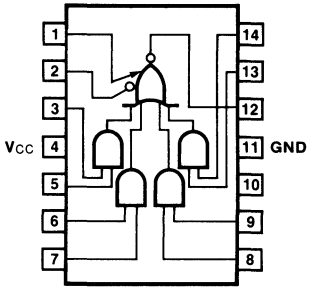
PINOUT A



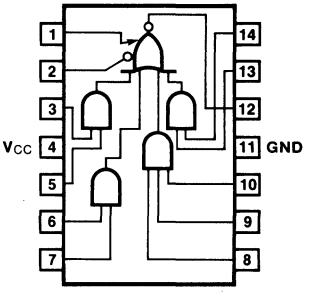
PINOUT B



PINOUT C



PINOUT D



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE: Using Expander Pins

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74H Min	54/74H Max	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	XM			2.4		V	I_1 = 320 μA I_2 = -320 μA	I_{OH} = -500 μA
		XC			2.4			I_1 = 570 μA I_2 = -570 μA	
V_{OH}	Output HIGH Voltage	XM	2.4				V	I_1 = 0.15 mA I_2 = -0.15 mA	I_{OH} = -400 μA
		XC	2.4					I_1 = 270 μA I_2 = -270 μA	
V_{OL}	Output LOW Voltage	XM				0.4	V	I_1 = 470 μA R_1 = 68 Ω	I_{OL} = 20 mA
		XC				0.4		I_1 = 600 μA R_1 = 63 Ω	
V_{OL}	Output LOW Voltage	XM		0.4			V	I_1 = 0.3 mA R_1 = 138 Ω	I_{OL} = 16 mA
		XC		0.4				I_1 = 0.43 mA R_1 = 130 Ω	
$V_{BE(Q)}$	Base-Emitter Voltage of Output Transistor Q	XM				1.0	V	I_1 = 700 μA	I_{OL} = 20 mA R_1 = 0 Ω
		XC				1.0		I_1 = 1.1 mA	
		XM		1.1				I_1 = 0.41 mA	I_{OL} = 16 mA R_1 = 0 Ω
		XC		1.0				I_1 = 0.62 mA	
I_{INX}	Expander-Node Input Current	XM				-5.85	mA	V_X = 1.4 V	
		XC				-6.3			
I_X	Expander Current	XM		2.9			mA	V_1 = 0.4 V, I_{OL} = 16 mA	
		XC		3.1					
I_{CCH} I_{CCL}	Power Supply Current			8.0 9.5		11 14	mA	V_{IN} = Gnd V_{IN} = Open	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay		22 15		11 11	ns	Expander Pins Open Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay				11.4* 7.4*	ns	C_X = 15 pF

*Typical Value

54/7454
54H/74H54
54LS/74LS54

4-WIDE, 2-INPUT AND-OR-INVERT GATE

ORDERING CODE: See Section 9

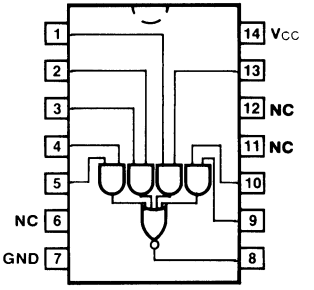
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7454PC		9A
	B	74H54PC		
	C	74LS54PC		
Ceramic DIP (D)	A	7454DC	5454DM	6A
	B	74H54DC	54H54DM	
	C	74LS54DC	54LS54DM	
Flatpak (F)	C	74LS54FC	54LS54FM	3I
	D	74H54FC	54H54FM	
	E	7454FC	5454FM	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

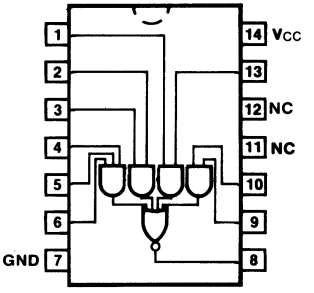
PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	10/5.0 (2.5)

CONNECTION DIAGRAMS

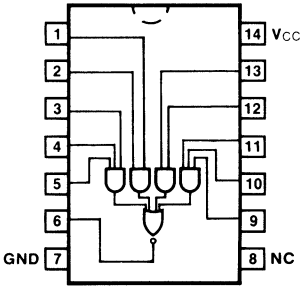
PINOUT A



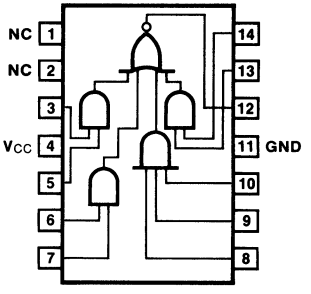
PINOUT B



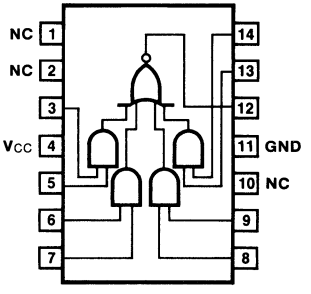
PINOUT C



PINOUT D



PINOUT E



DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74		54/74H		54/74LS		UNITS	CONDITIONS	
		Min	Max	Min	max	Min	Max			
I_{CCH} I_{CCL}	Power Supply Current		8.0 9.5		11 14		1.6 2.0	mA	V_{IN} = Gnd V_{IN} = Open	V_{CC} = Max
t_{PLH} t_{PHL}	Propagation Delay		22 15		11 11		15 15	ns	Figs. 3-1, 3-4	

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54H/74H55
54LS/74LS55

EXPANDABLE 4-INPUT AOI GATE ('H55)
2-WIDE, 4-INPUT AOI GATE ('LS55)

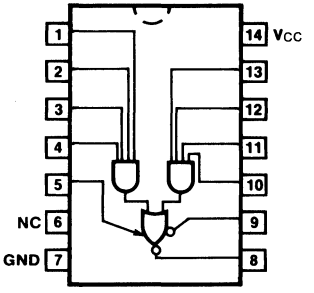
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74H55PC		9A
	B	74LS55PC		
Ceramic DIP (D)	A	74H55DC	54H55DM	6A
	B	74LS55DC	54LS55DM	
Flatpak (F)	B	74LS55FC	54LS55FM	3I
	C	74H55FC	54H55FM	

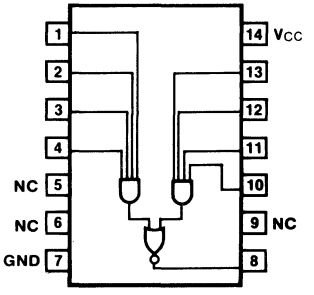
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74H (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.25/1.25	0.5/0.25
Outputs	12.5/12.5	10/5.0 (2.5)

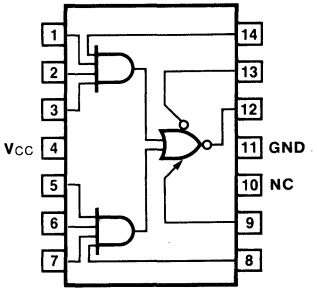
CONNECTION DIAGRAMS
PINOUT A



PINOUT B



PINOUT C



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE: Using Expander Pins

SYMBOL	PARAMETER		54/74H Min	54/74H Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	XM	2.4				V	I_1 = 320 μA I_2 = -320 μA	I_{OH} = -500 μA
		XC	2.4					I_1 = 570 μA I_2 = -570 μA	
V_{OL}	Output LOW Voltage	XM		0.4			V	I_1 = 470 μA R_1 = 68 Ω	I_{OL} = 20 mA
		XC		0.4				I_1 = 600 μA R_1 = 63 Ω	
$V_{BE(Q)}$	Base-Emitter Voltage of Input Transistor Q	XM		1.0			V	I_1 = 700 μA	I_{OL} = 20 mA
		XC		1.0				I_1 = 1.1 mA	R_1 = 0 Ω
$I_{IN\overline{X}}$	Expander-Node Input Current	XM		-5.85			mA	$V_{\overline{X}}$ = 1.4 V	
		XC		-6.3					
I_{CCH} I_{CCL}	Power Supply Current			6.4 12		0.8 1.3	mA	V_{IN} = Gnd V_{IN} = Open	V_{CC} = Max

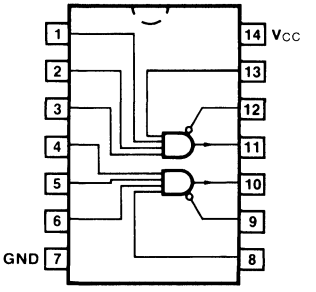
AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74H Min	54/74H Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay		11 11		15 15	ns	Expander Pins Open Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay		11.4* 7.7*			ns	C_L = 25 pF (Gnd to $\overline{X}$) C_X = 15 pF

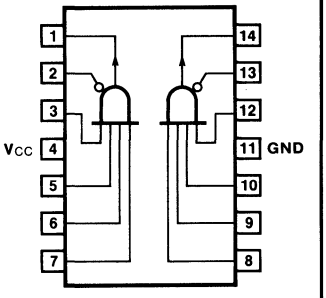
*Typical Value

54/7460
54H/74H60
DUAL 4-INPUT EXPANDER

CONNECTION DIAGRAMS
PINOUT A



PINOUT B



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	7460PC, 74H60PC		9A
Ceramic DIP (D)	A	7460DC, 74H60DC	5460DM, 54H60DM	6A
Flatpak (F)	B	7460FC, 74H60FC	5460FM, 54H60FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25
Outputs[1]	Note 2	Note 2

DC AND AC CHARACTERISTICS: See Section 3[3]

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	UNITS	CONDITIONS[4]	
V_{ON}	Output ON Voltage		0.4			V	V_{CC} = Min, V_{IN} = 2.0 V V_I = 1.0 V, R = 1.1 kΩ T_A = Min	
V_{ON}	Output ON Voltage				0.4	V	T_A = -55°C I_{ON} = 5.85 mA	V_{CC} = Min, V_{IN} = 2.0 V V_I = 1.0 V
					0.4		T_A = 0°C I_{ON} = 6.3 mA	
V_{ON}	Output ON Voltage				0.4	V	T_A = +125°C I_{ON} = 7.85 mA	V_{CC} = Max, V_{IN} = 2.0 V, V_I = 0.6 V
					0.4		T_A = +70°C I_{ON} = 7.4 mA	

1. A maximum of four expanders may be connected to one expandable AND-OR-Invert gate
2. Expander Outputs
3. DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
4. V_I is applied to x output terminal during test.

DC AND AC CHARACTERISTICS: See Section 3[1] (Cont'd)

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	UNITS	CONDITIONS[2]	
I_{OFF}	Output OFF Current		150			μA	T_A = -55°C	V_{CC} = Min, V_{IN} = 0.8 V, V_1 = 4.5 V, R = 1.2 kΩ
			270				T_A = 0°C	
I_{OFF}	Output OFF Current				320	μA	T_A = -55°C	V_{CC} = Min, V_{IN} = 0.8 V, V_1 = 4.5 V, R = 575 Ω
					570		T_A = 0°C	
I_{ON}	Output ON Current	-0.3		-0.47		mA	T_A = -55°C	V_{CC} = Min, V_{IN} = 2.0 V, V_1 = 1.0 V
		-0.43		-0.6			T_A = 0°C	
$I_{CC(OFF)}$	Power Supply Current		4.0		4.5	mA	V_{IN} = Open	V_{CC} = Max, V_1 = 0.85 V
$I_{CC(ON)}$			2.5		3.5		V_{IN} = Gnd	
t_{PLH}	Propagation Delay		30			ns	Figs. 3-1, 3-4	
t_{PHL}			20					

OUTPUT CAPACITANCE: V_{CC} and Ground Terminals Open

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	UNITS	CONDITIONS
$C_{\overline{X}}$	Effective Capacitance of Output Transistor Q_1				1.3[3]	pF	f = 1.0 MHz, T_A = +25°C

1. DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
2. V_1 is applied to x output terminal during test.
3. Typical Value

54H/74H61

TRIPLE 3-INPUT EXPANDER

ORDERING CODE: See Section 9

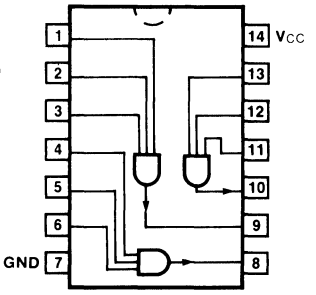
PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74H61PC		9A
Ceramic DIP (D)	A	74H61DC	54H61DM	6A
Flatpak (F)	B	74H61FC	54H61FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

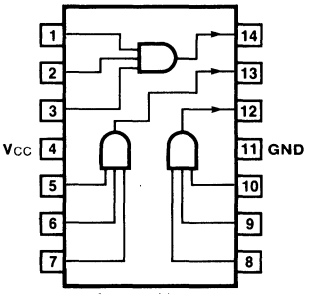
PINS	54/74H (U.L.) HIGH/LOW
Inputs	1.25/1.25
Outputs	*/*

CONNECTION DIAGRAMS

PINOUT A



PINOUT B



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74H Min	54/74H Max	UNITS	CONDITIONS	
V_{ON}	Output ON Voltage		1.0	V	T_A = -55°C, I_{ON} = 4.5 mA	V_{CC} = Min, V_{IH} = 2.0 V
			1.0		T_A = 0°C, I_{ON} = 5.35 mA	
I_{OFF}	Output OFF Current		50	μA	V_{CC} = Min, V_{IL} = 0.8 V, T_A = Max, V_{OFF} = 2.2 V	
$I_{CC(ON)}$	Power Supply Current		16	mA	V_{IN} = Open	V_{CC} = Max
$I_{CC(OFF)}$			7.0		V_{IN} = Gnd	

OUTPUT CAPACITANCE: V_{CC} and Ground Terminals Open

SYMBOL	PARAMETER	54/74H Min	54/74H Max	UNITS	CONDITIONS
C_X	Effective Capacitance of Output Transistor Q_1		1.3**	pF	f = 1.0 MHz, T_A = +25°C

*Expander Outputs
**Typical Value

54H/74H62

3-2-2-3-INPUT AND-OR EXPANDER

ORDERING CODE: See Section 9

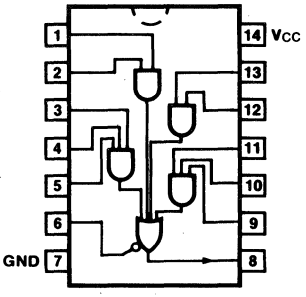
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74H62PC		9A
Ceramic DIP (D)	A	74H62DC	54H62DM	6A
Flatpak (F)	B	74H62FC	54H62FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

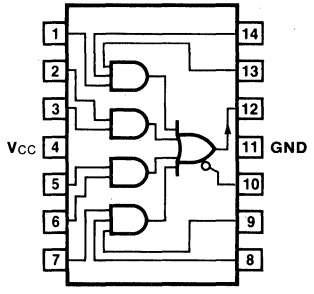
PINS	54/74H (U.L.) HIGH/LOW
Inputs	1.25/1.25
Outputs[1]	Note 2

CONNECTION DIAGRAMS

PINOUT A



PINOUT B



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74H Min	54/74H Max	UNITS	CONDITIONS[3]	
V_{ON}	Output ON Voltage		0.4 0.4	V	T = -55°C, I_{ON} = 5.85 mA T_A = 0°C, I_{ON} = 6.3 mA	V_{CC} = Min, V_{IN} = 2.0 V, V_I = 1.0 V
V_{ON}	Output ON Voltage		0.4 0.4	V	T_A = +125°C, I_{ON} = 7.85 mA T_A = +70°C, I_{ON} = 7.4 mA	V_{CC} = Max, V_{IN} = 2.0 V, V_I = 0.6 V
I_{OFF}	Output OFF Current		320 570	μA	T_A = -55°C T_A = 0°C	V_{CC} = Min, V_{IN} = 0.8 V, V_I = 4.5 V, R = 575 Ω
I_{ON}	Output ON Current	-470 -600		μA	T_A = -55°C T_A = 0°C	V_{CC} = Min, V_{IN} = 2.0 V, V_I = 1.0 V
$I_{CC(ON)}$ $I_{CC(OFF)}$	Power Supply Current		7.0 9.0	mA	V_{IN} = Open V_{IN} = Gnd	V_{CC} = Max, V_I = 0.85 V

1. A maximum of one expander may be connected to one expandable AND-OR-Invert gate
2. Expander Outputs
3. V_I is applied to x output terminal during test

OUTPUT CAPACITANCE: V_{CC} and Ground Terminals Open

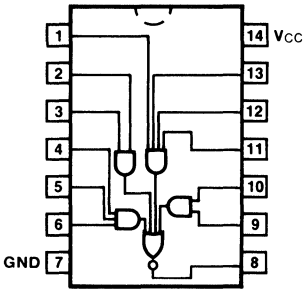
SYMBOL	PARAMETER	54/74H		UNITS	CONDITIONS
		Min	Max		
$C_{\overline{X}}$	Effective Capacitance of Output Transistor Q_1		1.3*	pF	f = 1.0 MHz, T_A = +25°C

*Typical Value

54S/74S64

4-2-3-2-INPUT AND-OR-INVERT GATE

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	74S64PC		9A
Ceramic DIP (D)	A	74S64DC	54S64DM	6A
Flatpak (F)	A	74S64FC	54S64FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L definitions

PINS	54/74S (U.L.) HIGH/LOW
Inputs	1.25/1.25
Outputs	25/12.5

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74S Min	54/74S Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply Current		12.5	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			16		**	
t_{PLH}	Propagation Delay	2.0	5.5	ns	Figs. 3-1, 3-4	
t_{PHL}		2.0	5.5			

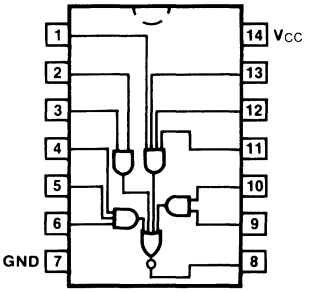
*DC limits apply over operating temperature range; AC limits apply at T_A = +25° C and V_{CC} = +5.0 V.
**I_{CCL} is measured with all inputs of one gate open and remaining inputs grounded.

54S/74S65

4-2-3-2-INPUT AND-OR-INVERT GATE

(With Open-Collector Output)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	74S65PC		9A
Ceramic DIP (D)	A	74S65DC	54S65DM	6A
Flatpak (F)	A	74S65FC	54S65FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74S (U.L.) HIGH/LOW
Inputs	1.25/1.25
Outputs	OC[1]/12.5

DC AND AC CHARACTERISTICS: See Section 3[2]

SYMBOL	PARAMETER	54/74S Min	54/74S Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply Current		11	mA	V_{IN} = 0 V	V_{CC} = Max
I_{CCL}			16		Note 3	
t_{PLH}	Propagation Delay	2.0	7.5	ns	Figs. 3-2, 3-4	
t_{PHL}		2.0	8.5			

[1]OC — Open Collector
[2]DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
[3]I_{CCL} is measured with all inputs of one gate open and remaining inputs grounded.

54/7470

JK EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The '70 is a gated input edge-triggered JK flip-flop offering Direct Clear and Set inputs, and complementary Q and $\overline{Q}$ outputs. Information at the J and K inputs is tranferred to the outputs on the positive edge of the clock pulse. Direct-coupled clock triggering occurs at a specified voltage level of the clock pulse. When the clock input threshold voltage has been passed, the gate inputs are locked out. These flip-flops are designed for medium to high speed applications and offer a significant saving in system power dissipation and package count where input gating is required.

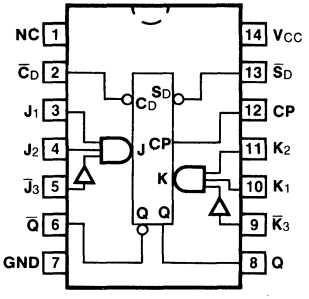
TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

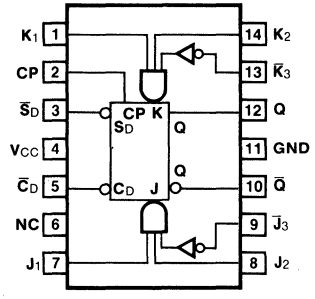
Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear or Set function can only occur when clock input is LOW
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ is indeterminate

$J = J_1 \bullet J_2 \bullet \overline{J}_3$
$K = K_1 \bullet K_2 \bullet \overline{K}_3$
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
If inputs $\overline{J}_3$ or $\overline{K}_3$ are not used they must be grounded.
H = HIGH Voltage Level
L = LOW Voltage Level

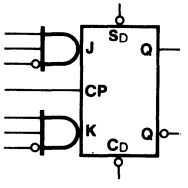
CONNECTION DIAGRAMS
PINOUT A



PINOUT B



LOGIC SYMBOL



V_{CC} = Pin 14 (4)
GND = Pin 7 (11)

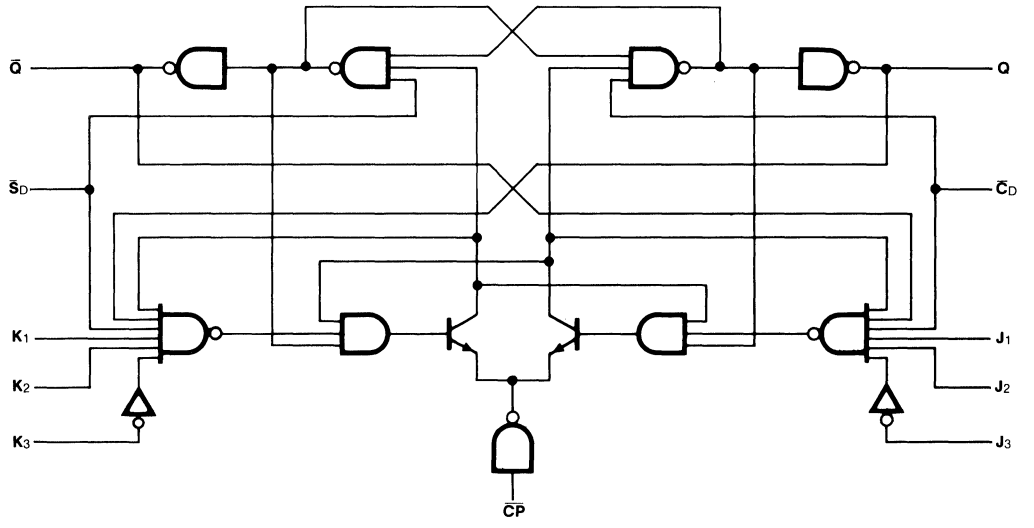
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7470PC		9A
Ceramic DIP (D)	A	7470DC	5470DM	6A
Flatpak (F)	B	7470FC	5470FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
J_1, J_2, $\overline{J}_3$ / K_1, K_2, $\overline{K}_3$	Data Inputs	1.0/1.0
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0
$\overline{C}_D$	Direct Clear Input (Active LOW)	2.0/2.0
$\overline{S}_D$	Direct Set Input (Active LOW)	2.0/2.0
Q, $\overline{Q}$	Outputs	20/10

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		26	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	DESCRIPTION	54/74 C_L = 15 pF, R_L = 400 Ω		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	20		MHz	Fig. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q or $\overline{Q}$		50 50	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_D$ or $\overline{C}_D$ to Q or $\overline{Q}$		50 50	ns	Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
t_s (H)	Setup Time HIGH, J_n or K_n to CP	20		ns	Fig. 3-6
t_h (H)	Hold Time HIGH, J_n or K_n to CP	5.0		ns	Fig. 3-6
t_s (L)	Setup Time LOW, J_n or K_n to CP	20		ns	Fig. 3-6
t_h (L)	Hold Time LOW, J_n or K_n to CP	5.0		ns	Fig. 3-6
t_w (H) t_w (L)	CP Pulse Width	20 30		ns	Fig. 3-8
t_w (L)	$\overline{S}_D$ or $\overline{C}_D$ Pulse Width LOW	25		ns	Fig. 3-10

54H/74H71

JK MASTER/SLAVE FLIP-FLOP

(With AND-OR Inputs)

DESCRIPTION — The '71 is a high speed JK master/slave flip-flop with AND-OR gate inputs. The AND-OR gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) isolate slave from master; 2) enter information from AND-OR gate inputs to master; 3) disable AND-OR gate inputs; 4) transfer information from master to slave. The logic state of J and K inputs must not be allowed to change when the clock pulse is in a HIGH state.

TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

H = HIGH Voltage Level
L = LOW Voltage Level

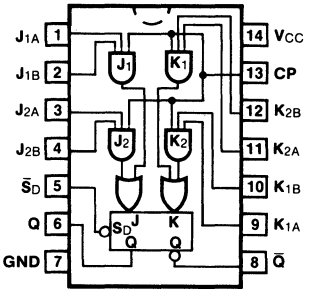
CLOCK WAVEFORM

Asynchronous Input:
LOW input to $\overline{S}_D$ sets Q to HIGH level
Set is independent of clock

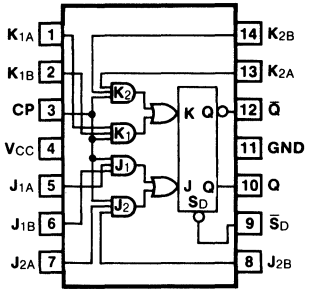
$J = (J_{1A} \bullet J_{1B}) + (J_{2A} \bullet J_{2B})$
$K = (K_{1A} \bullet K_{1B}) + (K_{2A} \bullet K_{2B})$
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CONNECTION DIAGRAMS

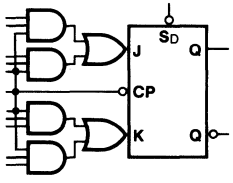
PINOUT A



PINOUT B



LOGIC SYMBOL



VCC = Pin 14 (4)
GND = Pin 7 (11)

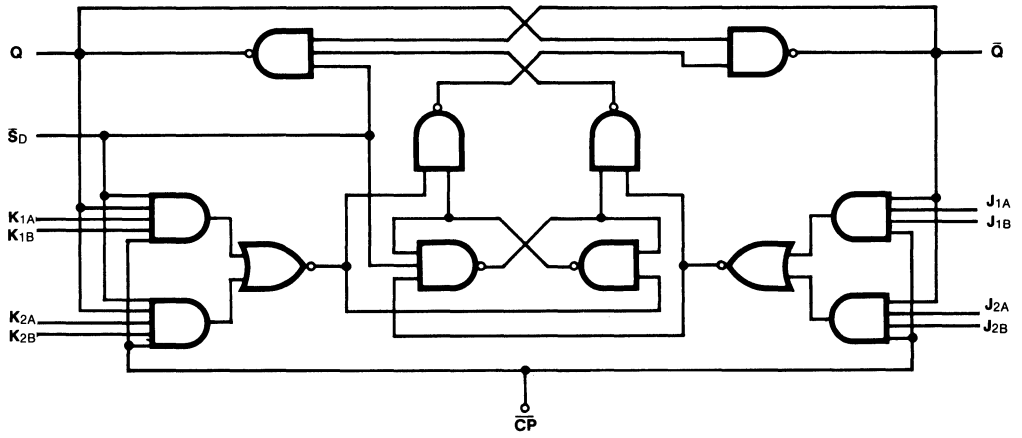
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74H71PC		9A
Ceramic DIP (D)	A	74H71DC	54H71DM	6A
Flatpak (F)	B	74H71FC	54H71FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74H (U.L.) HIGH/LOW
J_{1A}, J_{1B}, J_{2A}, J_{2B} / K_{1A}, K_{1B}, K_{2A}, K_{2B}	Data Inputs	1.25/1.25
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	2.5/2.5
$\overline{S}_D$	Direct Set Input (Active LOW)	3.75/3.75
Q, $\overline{Q}$	Outputs	12.5/12.5

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74H		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		30	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74H C_L = 25 pF R_L = 280 Ω		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	25		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q or $\overline{Q}$		21 27	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_D$ to Q or $\overline{Q}$		13 24	ns	Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74H		UNITS	CONDITIONS
		Min	Max		
t_s (H)	Setup Time HIGH, J_n or K_n to $\overline{CP}$	0		ns	Fig. 3-18
t_h (H)	Hold Time HIGH, J_n or K_n to $\overline{CP}$	0		ns	Fig. 3-18
t_s (L)	Setup Time LOW, J_n or K_n to $\overline{CP}$	0		ns	Fig. 3-18
t_h (L)	Hold Time LOW, J_n or K_n to $\overline{CP}$	0		ns	Fig. 3-18
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width	12 28		ns	Fig. 3-9
t_w (L)	$\overline{S}_D$ Pulse Width LOW	16		ns	Fig. 3-10

54/7472
54H/74H72

JK MASTER/SLAVE FLIP-FLOP
(With AND Inputs)

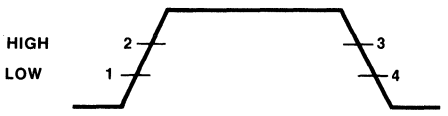
DESCRIPTION — The '72 is a high speed JK master/slave flip-flop with AND gate inputs. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) isolate slave from master; 2) enter information from AND gate inputs to master; 3) disable AND gate inputs; 4) transfer information from master to slave. The logic state of J and K inputs must not be allowed to change when the clock pulse is in a HIGH state.

TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ $t_n + 1$
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	Q_n

$J = (J_{1A} \bullet J_{1B}) + (J_{2A} \bullet J_{2B})$
$K = (K_{1A} \bullet K_{1B}) + (K_{2A} \bullet K_{2B})$
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

CLOCK WAVEFORM

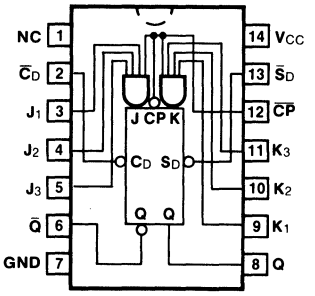


Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ is indeterminate

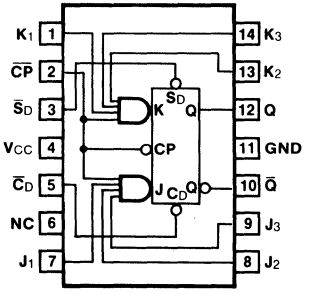
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	7472PC, 74H72PC		9A
Ceramic DIP (D)	A	7472DC, 74H72DC	5472DM, 54H72DM	6A
Flatpak (F)	B	7472FC, 74H72FC	5472FM, 54H72FM	3I

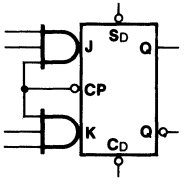
CONNECTION DIAGRAMS
PINOUT A



PINOUT B



LOGIC SYMBOL

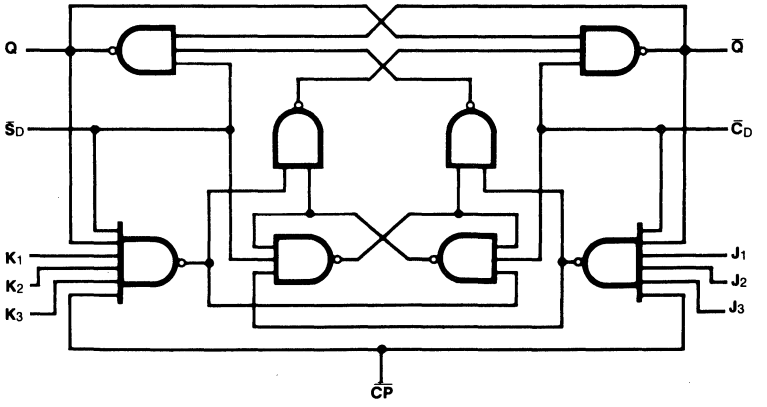


V_{CC} = Pin 14 (4)
GND = Pin 7 (11)
NC = Pin 1 (6)

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW
$J_1 - J_3$, $K_1 - K_3$	Data Inputs	1.0/1.0	1.25/1.25
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	2.0/2.0	2.5/2.5
$\overline{C}_D$	Direct Clear Input (Active LOW)	2.0/2.0	2.5/2.5
$\overline{S}_D$	Direct Set Input (Active LOW)	2.0/2.0	2.5/2.5
Q, $\overline{Q}$	Outputs	20/10	12.5/12.5

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74H		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		20		25	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74H		UNITS	CONDITIONS
		C_L = 15 pF, R_L = 400 Ω		C_L = 25 pF, R_L = 280 Ω			
		Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	15		25		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q or $\overline{Q}$		25 40		21 27	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_D$ or $\overline{C}_D$ to Q or $\overline{Q}$		25 40		13 24	ns	Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74		54/74H		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time J_n or K_n to $\overline{CP}$	0		0		ns	Fig. 3-18
t_h (H) t_h (L)	Hold Time J_n or K_n to $\overline{CP}$	0		0		ns	Fig. 3-18
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width	20 47		12 28		ns	Fig. 3-9
t_w (L)	$\overline{S}_D$ or $\overline{C}_D$ Pulse Width LOW	25		16		ns	Fig. 3-10

54/7473
54H/74H73
54LS/74LS73

DUAL JK FLIP-FLOP

(With Separate Clears and Clocks)

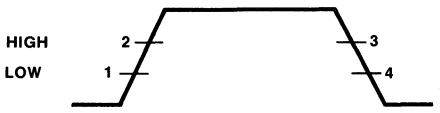
DESCRIPTION — The '73 and 'H73 dual JK master/slave flip-flops have a separate clock for each flip-flop. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) isolate slave from master; 2) enter information from J and K inputs to master; 3) disable J and K inputs; 4) transfer information from master to slave.

TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORM



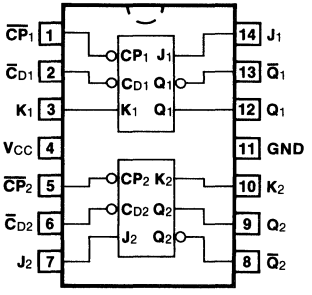
Asynchronous Input:
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear is independent of clock

The 'LS73 offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

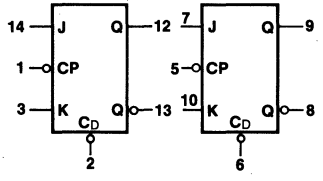
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	7473PC, 74H73PC 74LS73PC		9A
Ceramic DIP (D)	A	7473DC, 74H73DC 74LS73DC	5473DM, 54H73DM 54LS73DM	6A
Flatpak (F)	A	7473FC, 74H73FC 74LS73FC	5473FM, 54H73FM 54LS73FM	3I

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



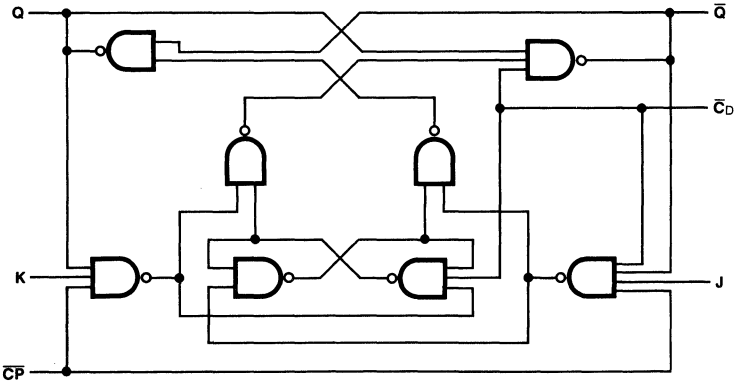
V_{CC} = Pin 4
GND = Pin 11

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

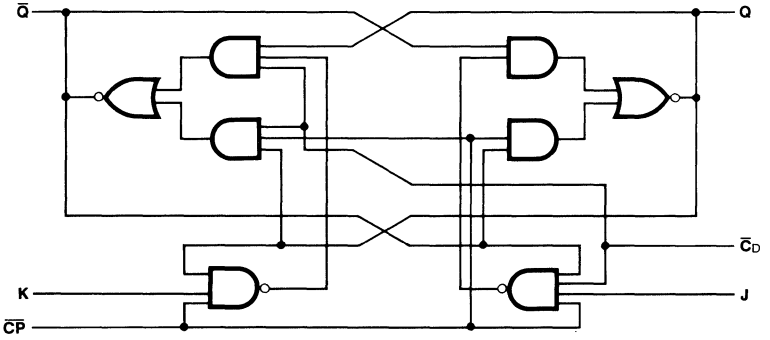
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	2.0/2.0	1.25/1.25	2.0/0.5
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	2.0/2.0	2.5/2.5	1.5/0.5
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	20/10	12.5/12.5	10/5.0 (2.5)

LOGIC DIAGRAMS (one half shown)

'73, 'H73



'LS73



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74H		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
I_{CC}	Power Supply Current		40		50		8.0	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74H		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF, R_L = 400 Ω		C_L = 25 pF, R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	15		25		30		MHz	Fig. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q or $\overline{Q}$		25 40		21 27		20 30	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ to Q or $\overline{Q}$		25 40		13 24		20 30	ns	Figs. 3-1, 3-10

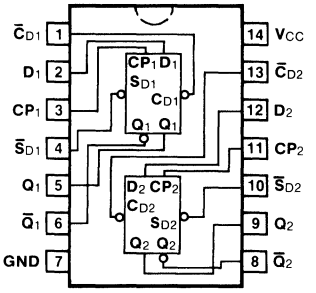
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V T_A = +25°C

SYMBOL	PARAMETER	54/74		54/74H		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_s (H)	Setup Time HIGH J_n or K_n to $\overline{CP}_n$	0		0		20		ns	Fig. 3-18 ('73, 'H73) Fig. 3-7 ('LS73)
t_h (H)	Hold Time HIGH J_n or K_n to $\overline{CP}_n$	0		0		0		ns	
t_s (L)	Setup Time LOW J_n or K_n to $\overline{CP}_n$	0		0		20		ns	
t_h (L)	Hold Time LOW J_n or K_n to $\overline{CP}_n$	0		0		0		ns	
t_w (H) t_w (L)	$\overline{CP}_n$ Pulse Width	20 47		12 16		13.5 20		ns	Fig. 3-9
t_w (L)	$\overline{C}_{Dn}$ Pulse Width LOW	25		16		25		ns	Figs. 3-1, 3-10

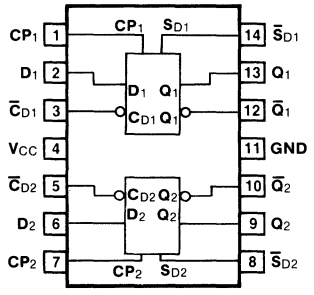
54/7474
54H/74H74
54S/74S74
54LS/74LS74

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

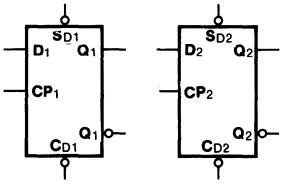
CONNECTION DIAGRAMS
PINOUT A



PINOUT B



LOGIC SYMBOL



V_{CC} = Pin 14 (4)
GND = Pin 7 (11)

DESCRIPTION — The '74 devices are dual D-type flip-flops with Direct Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

TRUTH TABLE
(Each Half)

INPUT	OUTPUTS	
@ t_n	@ t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

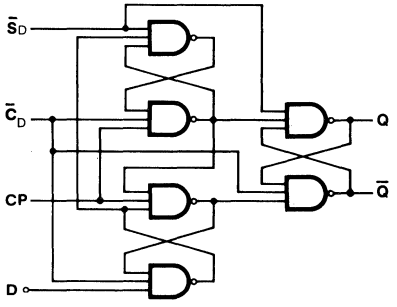
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7474PC, 74H74PC 74S74PC, 74LS74PC		9A
Ceramic DIP (D)	A	7474DC, 74H74DC 74S74DC, 74LS74DC	5474DM, 54H74DM 54S74DM, 54LS74DM	6A
Flatpak (F)	A	74S74FC, 74LS74FC	54S74FM, 54LS74FM	3I
	B	7474FC, 74H74FC	5474FM, 54H74FM	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
D_1, D_2	Data Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	2.0/2.0	2.5/2.5	2.5/2.5	1.0/0.5
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	3.0/2.0	3.75/2.5	3.75/3.75	1.5/0.75
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	2.0/1.0	2.5/1.25	2.5/2.5	1.0/0.5
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		30		42		50		8.0	mA	V_{CC} = Max, V_{CP} = 0 V
		XC		30		50		50		8.0		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74H C_L = 25 pF, R_L = 280 Ω Min	54/74H Max	54/74S C_L = 15 pF, R_L = 280 Ω Min	54/74S Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	15		35		75		30		MHz	Figs. 3-1, 3-8
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$		25		15		9.0		25	ns	Figs. 3-1, 3-8
t_{PHL}			40		20		11		35		
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		25		20		6.0		15	ns	$V_{CP} \geq$ 2.0 V Figs. 3-1, 3-10
t_{PHL}			40		30		13.5		35		
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		25		20		6.0		15	ns	$V_{CP} \leq$ 0.8 V Figs. 3-1, 3-10
t_{PHL}			40		30		8.0		24		

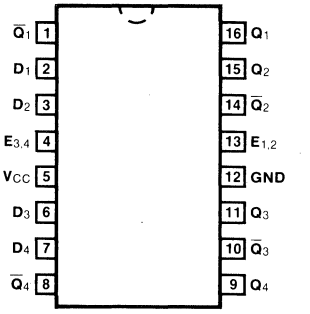
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74		54/74H		54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max	Min	Max		
t_s (H)	Setup Time HIGH D_n to CP_n	20		10		3.0		10		ns	Fig. 3-6
t_h (H)	Hold Time HIGH D_n to CP_n	5.0		0		0		5.0		ns	
t_s (L)	Setup Time LOW D_n to CP_n	20		15		3.0		20		ns	Fig. 3-6
t_h (L)	Hold Time LOW D_n to CP_n	5.0		0		0		5.0		ns	
t_w (H) t_w (L)	CP_n Pulse Width	30 37		15 13.5		6.0 7.3		18 15.5		ns	Fig. 3-8
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	30		25		7.0		15		ns	Fig. 3-10

54/7475

4-BIT BISTABLE LATCH

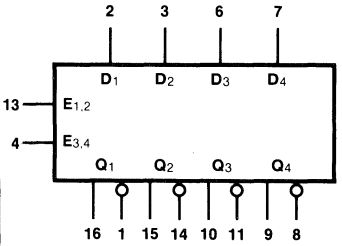
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '75 latch is used as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the Enable is HIGH and the Q output will follow the data input as long as the Enable remains HIGH. When the Enable goes LOW, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the Enable is permitted to go HIGH.

The '75 features complementary Q and $\overline{Q}$ output from a 4-bit latch and is available in 16-pin packages. For higher component density applications, the '77 4-bit latch is available in the 14-pin package with $\overline{Q}$ outputs omitted.

LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 12

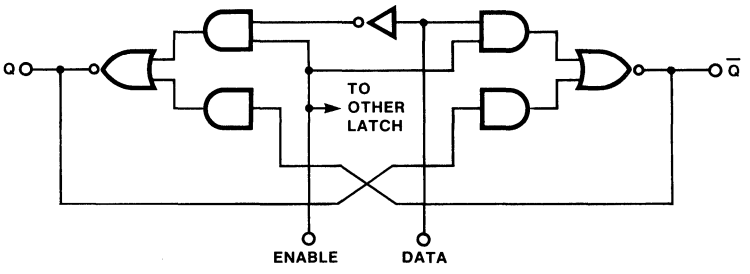
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7475PC		9B
Ceramic DIP (D)	A	7475DC	5475DM	6B
Flatpak (F)	A	7475FC	5475FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
D_1 — D_4	Data Inputs	2.0/2.0
$E_{1,2}$	Enable Input, Latches 1, 2	4.0/4.0
$E_{2,3}$	Enable Input, Latches 3, 4	4.0/4.0
Q_1 — Q_4	Latch Outputs	10/10
$\overline{Q}_1$ — $\overline{Q}_4$	Complementary Latch Outputs	10/10

LOGIC DIAGRAM



TRUTH TABLE
(Each Latch)

INPUT	OUTPUT
@ t_n	@ t_{n+1}
D	Q
H L	H L

NOTES:
t_n = bit time before enable negative-going transition.
t_{n+1} = bit time after enable negative-going transition.
H = HIGH Voltage Level
L = LOW Voltage Level

4

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		46	mA	V_{CC} = Max, All Inputs = Gnd
		XC		53		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω Min	54/74 C_L = 15 pF R_L = 400 Ω Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay D to Q		30 25	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay D to $\overline{Q}$		40 15	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay E to Q, $\overline{Q}$		30 15	ns	Figs. 3-1, 3-8

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
t_s (H)	Setup Time HIGH, D to E	20		ns	Fig. 3-14
t_h (H)	Hold Time HIGH, D to E	0		ns	Fig. 3-14
t_s (L)	Setup Time LOW, D to E	20		ns	Fig. 3-14
t_h (L)	Hold Time LOW, D to E	0		ns	Fig. 3-14
t_w (H)	E Pulse Width HIGH	20		ns	Fig. 3-8

54/7476
54H/74H76
54LS/74LS76

DUAL JK FLIP-FLOP

(With Separate Sets, Clears and Clocks)

DESCRIPTION — The '76 and 'H76 are dual JK master/slave flip-flops with separate Direct Set, Direct Clear and Clock Pulse inputs for each flip-flop. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) isolate slave from master; 2) enter information from J and K inputs to master; 3) disable J and K inputs; 4) transfer information from master to slave.

TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

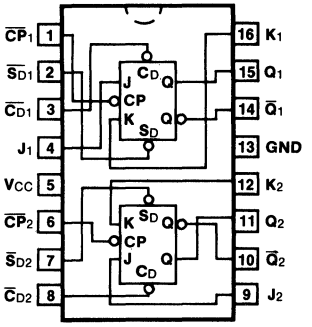
H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORM

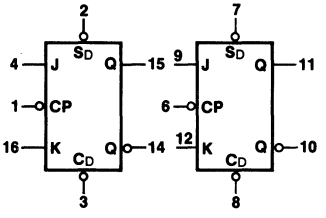
Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

The 'LS76 is a dual JK, negative edge-triggered flip-flop also offering individual Direct Set, Direct Clear and Clock Pulse inputs. When the Clock Pulse input is HIGH, the JK inputs are enabled and data is accepted. This data will be transferred to the outputs according to the Truth Table on the HIGH-to-LOW clock transitions.

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 13

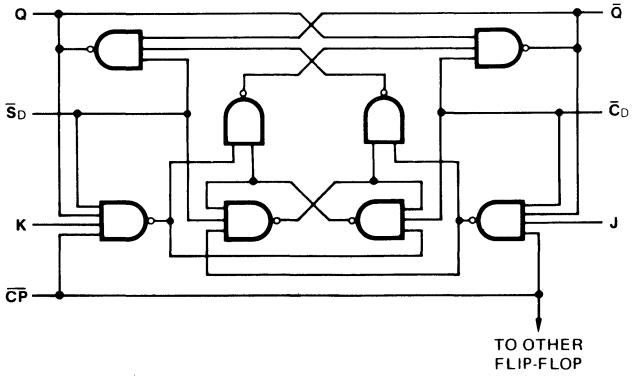
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	7476PC, 74H76PC 74LS76PC		9B
Ceramic DIP (D)	A	7476DC, 74H76DC 74LS76DC	5476DM, 54H76DM 54LS76DM	6B
Flatpak (F)	A	7476FC, 74H76FC 74LS76FC	5476FM, 54H76FM 54LS76FM	4L

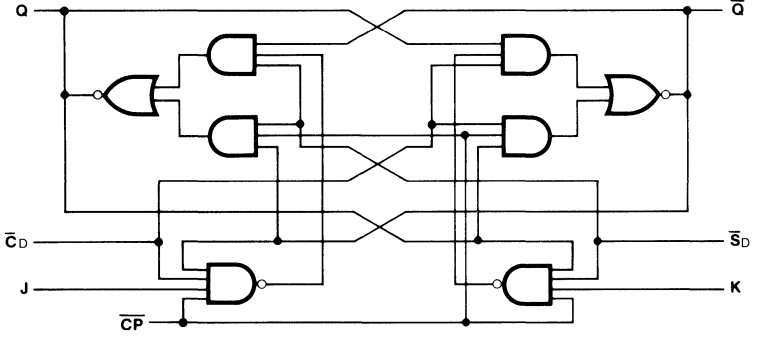
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	2.0/2.0	2.5/2.5	2.0/0.5
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	2.0/2.0	2.5/2.5	1.5/0.5
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	2.0/2.0	2.5/2.5	1.5/0.5
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs	20/10	12.5/12.5	10/5.0 (2.5)

LÓGIC DIAGRAMS (one half shown)
'76, 'H76



'LS76



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74H		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
I_{CC}	Power Supply Current		40		50		8.0	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74H		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF, R_L = 400 Ω		C_L = 25 pF, R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	15		25		30		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$		25 40		21 27		20 30	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		25 40		13 24		20 30	ns	Figs. 3-1, 3-10

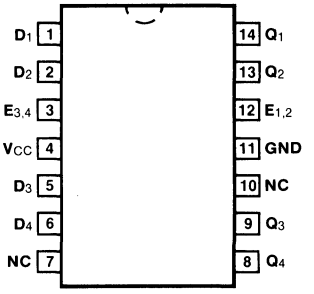
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		54/74H		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_s (H)	Setup Time HIGH J_n or K_n to $\overline{CP}_n$	0		0		20		ns	Fig. 3-18 ('76, 'H76) Fig. 3-7 ('LS76)
t_h (H)	Hold Time HIGH J_n or K_n to $\overline{CP}_n$	0		0		0		ns	
t_s (L)	Setup Time LOW J_n or K_n to $\overline{CP}_n$	0		0		20		ns	
t_h (L)	Hold Time LOW J_n or K_n to $\overline{CP}_n$	0		0		0		ns	
t_w (H) t_w (L)	$\overline{CP}_n$ Pulse Width	20 47		12 28		20 13.5		ns	Fig. 3-9
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	25		16		25		ns	Fig. 3-10

54/7477

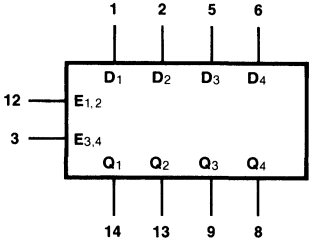
QUAD D-TYPE LATCH

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '77 contains four D-type latches used for temporary storage. Each latch shares an Enable input with one other latch. When the Enable input is HIGH, a latch is transparent, i.e., the Q output follows the D input each time it changes. When the Enable goes LOW, the information (that was present at the D input when the transition occurred) is retained at the Q output. For Truth Table, specifications, and logic diagrams, refer to the '75 data sheet, but note that $\overline{Q}$ is not available on the '77.

LOGIC SYMBOL



VCC = Pin 4
GND = Pin 11
NC = Pin 7, 10

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7477PC		9A
Ceramic DIP (D)	A	7477DC	5477DM	6A
Flatpak (F)	A	7477FC	5477FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
D1 — D4	Data Inputs	2.0/2.0
E1,2	Enable Input, Latches 1, 2	4.0/4.0
E3,4	Enable Input, Latches 3, 4	4.0/4.0
Q1 — Q4	Latch Outputs	10/10

54H/74H78
54LS/74LS78

DUAL JK FLIP-FLOP

(With Common Clear and Clock and Separate Set Inputs)

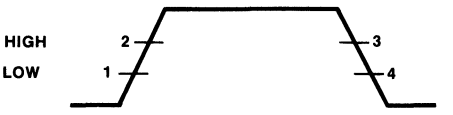
DESCRIPTION — The 'H78 is a dual JK master/slave flip-flop with separate Direct Set inputs, a common Direct Clear input and a common Clock Pulse input. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) isolate slave from mas-2ter; 2) enter information from J and K inputs to master; 3) disable J and K inputs; 4) transfer information from master to slave. The logic state of the J and K inputs must not be allowed to change when the clock pulse is in a HIGH state.

TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORM



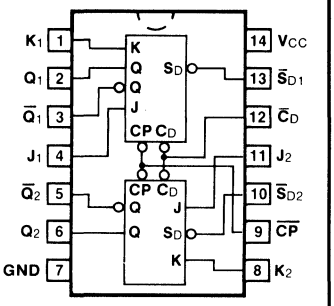
Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ is makes both Q and $\overline{Q}$ HIGH

The 'LS78 is a dual JK, negative edge-triggered flip-flop which also offers separate Direct Set inputs, a common Direct Clear and common Clock Pulse input. When the Clock Pulse input is HIGH, the JK inputs are enabled and data is accepted. This data will be transferred to the outputs according to the Truth Table on the HIGH-to-LOW clock transitions.

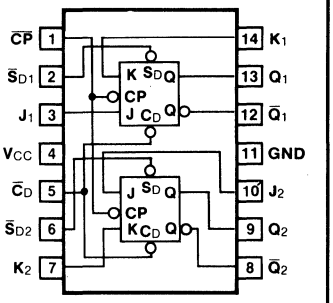
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74H78PC		9A
	B	74LS78PC		
Ceramic DIP (D)	A	74H78DC	54H78DM	6A
	B	74LS78DC	54LS78DM	
Flatpak (F)	A	74H78FC	54H78FM	3I
	B	74LS78FC	54LS78FM	

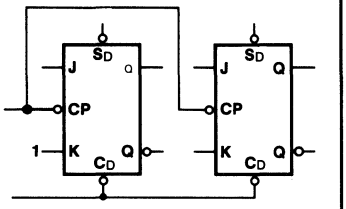
CONNECTION DIAGRAMS
PINOUT A



PINOUT B



LOGIC SYMBOL

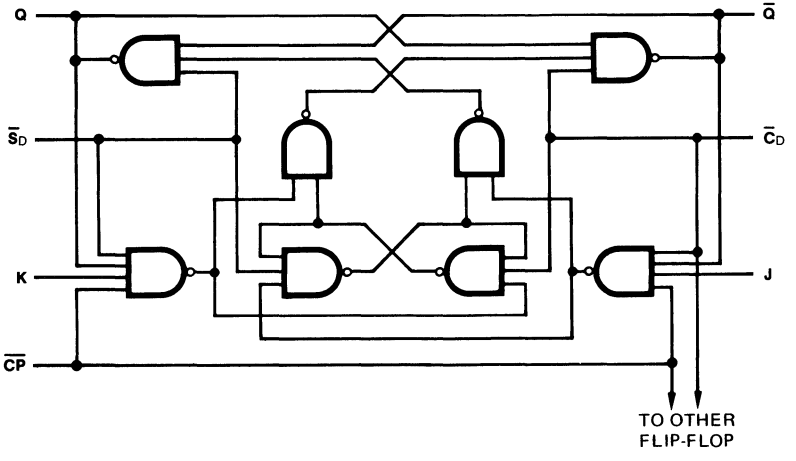


VCC = Pin 14 (4)
GND = Pin 7 (11)

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74H (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	1.25/1.25	0.5/0.25
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	2.5/2.5	4.0/1.0
$\overline{C}_D$	Direct Clear Input (Active LOW)	5.0/5.0	3.0/1.0
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	2.5/2.5	1.5/0.5
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs	12.5/12.5	10/5.0 (2.5)

LOGIC DIAGRAM
(one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74H		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		50		8.0	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISITICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74H		54/74LS		UNITS	CONDITIONS
		C_L = 25 pF, R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	25		30		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_n or $\overline{Q}_n$		21 27		20 30	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_D$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		13 24		20 30	ns	Figs. 3-1, 3-10

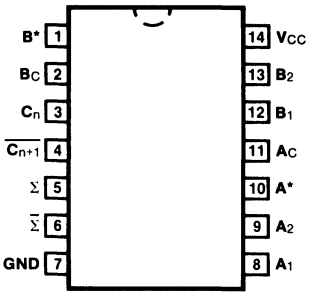
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74H		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H)	Setup Time HIGH J_n or K_n to $\overline{CP}$	0		20		ns	Fig. 3-18 ('H78) Fig. 3-7 ('LS78)
t_h (H)	Hold Time HIGH J_n or K_n to $\overline{CP}$	0		0		ns	
t_s (L)	Setup Time LOW J_n or K_n to $\overline{CP}$	0		20		ns	
t_h (L)	Hold Time LOW J_n or K_n to $\overline{CP}$	0		0		ns	
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width	12 28		20 13.5		ns	Fig. 3-9
t_w (L)	$\overline{C}_D$ or $\overline{S}_{Dn}$ Pulse Width LOW	16		25		ns	Fig. 3-10

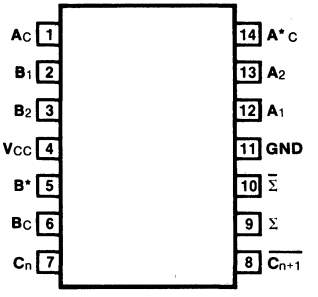
54/7480

GATED FULL ADDER

CONNECTION DIAGRAMS
PINOUT A

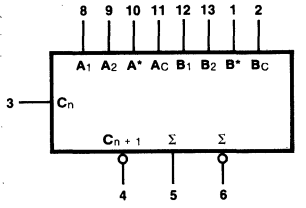


PINOUT B



DESCRIPTION — The '80 is a single-bit, high speed, binary full adder with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output. It is designed for medium and high speed, multiple-bit, parallel-add/serial carry applications. The circuit utilizes DTL for the gated inputs and high speed, high fan-out TTL for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7480PC		9A
Ceramic DIP (D)	A	7480DC	5480DM	6A
Flatpak (F)	B	7480FC	5480FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
A_1, A_2, B_1, B_2	Operand Inputs	0.4/1.0
A*, B*	Inverted Operand Inputs	-/1.63
A_C, B_C	Control Inputs	0.4/1.0
C_n	Carry Input	5.0/5.0
$\overline{C_{n+1}}$	Inverted Carry Output	5.0/5.0
Σ, $\overline{\Sigma}$	Sum Outputs	10/10
A*, B*	When Used As Outputs	3.0/3.0

TRUTH TABLE

INPUTS			OUTPUTS		
C_n	B	A	$\overline{C_{n+1}}$	$\overline{\Sigma}$	Σ
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

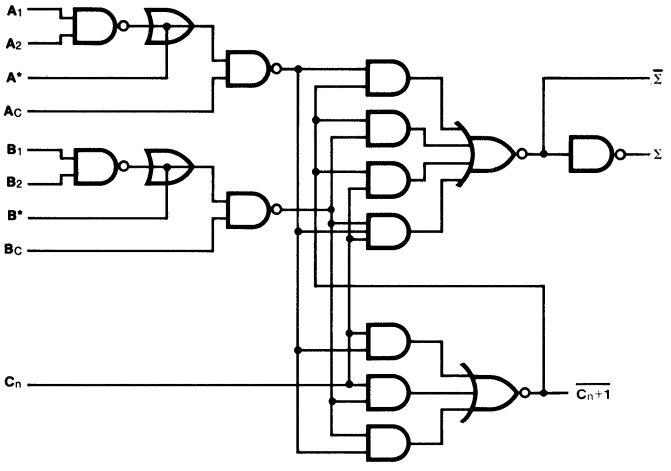
NOTES:

(1) $A = \overline{A^* \bullet A_C}$, $B = \overline{B^* \bullet B_C}$ where $\overline{A_1 \bullet A_2}$. $B^* = \overline{B_1 \bullet B_2}$

(2) When A* or B* are used as inputs, A_1 and A_2 or B_1 and B_2 respectively must be connected to Gnd.

(3) When A_1 and A_2 or B_1 and B_2 are used as inputs, A* or B* respectively must be open or used to perform Dot-OR logic.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unlsess otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current at $\overline{C_{n+1}}$	XM	-20	-70	mA	V_{CC} = Max
		XC	-18	-70		
I_{OS}	Output Short Circuit Current at A*, B*	XM	-0.9	-2.9	mA	V_{CC} = Max
		XC	-0.9	-2.9		
I_{CC}	Power Supply Current	XM		31	mA	V_{CC} = Max
		XC		35		

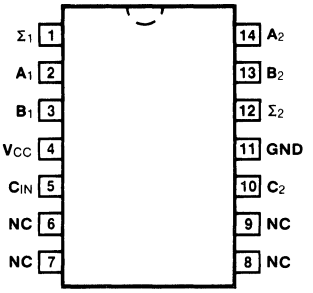
AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF Min	54/74 C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay C_n to $\overline{C_{n+1}}$		17 12	ns	Figs. 3-1, 3-4 R_L = 780 Ω
t_{PLH} t_{PHL}	Propagation Delay B_C to $\overline{C_{n+1}}$		25 55	ns	Figs. 3-1, 3-5 R_L = 780 Ω
t_{PLH} t_{PHL}	Propagation Delay A_C to Σ		70 80	ns	Figs. 3-1, 3-4 R_L = 400 Ω
t_{PLH} t_{PHL}	Propagation Delay B_C to $\overline{\Sigma}$		55 75	ns	Figs. 3-1, 3-5 R_L = 400 Ω
t_{PLH} t_{PHL}	Propagation Delay A_1 to A* or B_1 to B*		65 25	ns	Figs. 3-1, 3-4 R_L not used

54/7482

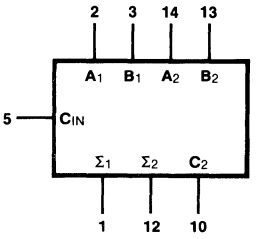
2-BIT FULL ADDER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '82 is a full adder which performs the addition of two 2-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_2) is obtained from the second bit. Designed for medium to high speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high speed, high fan-out TTL. The implementation of a single-inversion, high speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 11
NC = Pins 6,7,8,9

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	7482PC		9A
Ceramic DIP (D)	A	7482DC	5482DM	6A
Flatpak (F)	A	7482FC	5482FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

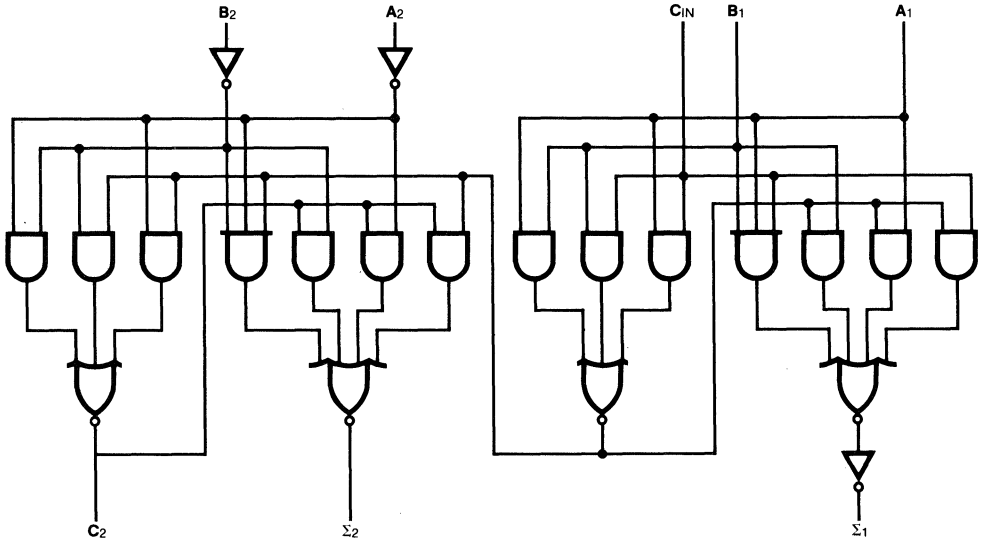
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
A_1, B_1	Bit 1 Operand Inputs	4.0/4.0
A_2, B_2	Bit 2 Operand Inputs	1.0/1.0
C_{IN}	Bit 1 Carry Input	4.0/4.0
Σ_1	Bit 1 Sum Output	10/10
Σ_2	Bit 2 Sum Output	10/10
C_2	Bit 2 Carry Output	5.0/5.0

TRUTH TABLE

INPUTS				OUTPUTS					
				$C_{IN} = 0$			$C_{IN} = 1$		
A_1	B_1	A_2	B_2	Σ_1	Σ_2	C_2	Σ_1	Σ_2	C_2
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current at Σ_n	XM	-20	-55	mA	V_{CC} = Max
		XC	-18	-55		
I_{OS}	Output Short Circuit Current at C_2	XM	-20	-70	mA	V_{CC} = Max
		XC	-18	-70		
I_{CC}	Power Supply Current	XM		50	mA	V_{CC} = Max; A_1, A_2, C_{IN} = 4.5 V; B_1, B_2 = Gnd
		XC		58		

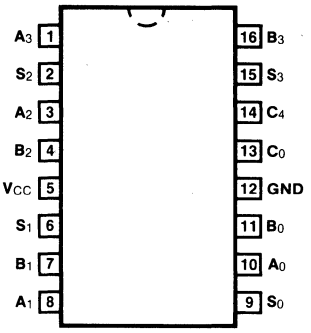
AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω Min	54/74 C_L = 15 pF R_L = 400 Ω Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay C_{IN} to Σ_1		34 40	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay B_2 to Σ_2		40 35	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay C_{IN} to Σ_2		38 42	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay C_{IN} to C_2		19 27	ns	Figs. 3-1, 3-5 R_L = 780 Ω

54/7483A
54LS/74LS83A

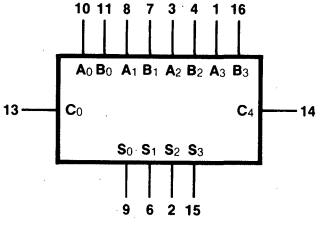
4-BIT BINARY FULL ADDER
(With Fast Carry)

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '83A high speed 4-bit binary full adders with internal carry lookahead accept two 4-bit binary words ($A_0 — A_3$, $B_0 — B_3$) and a Carry input (C_0). They generate the binary Sum outputs ($S_0 — S_3$) and the Carry output (C_4) from the most significant bit. They operate with either HIGH or active LOW operands (positive or negative logic). The '283 is recommended for new designs since it features standard corner power pins.

LOGIC SYMBOL



VCC = Pin 5
GND = Pin 12

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7483APC, 74LS83APC		9B
Ceramic DIP (D)	A	7483ADC, 74LS83ADC	5483ADM, 54LS83ADM	6B
Flatpak (F)	A	7483AFC, 74LS83AFC	5483AFM, 54LS83AFM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 — A_3$	A Operand Inputs	1.0/1.0	1.0/0.5
$B_0 — B_3$	B Operand Inputs	1.0/1.0	1.0/0.5
C_0	Carry Input	1.0/1.0	0.5/0.25
$S_0 — S_3$	Sum Outputs	20/10	10/5.0 (2.5)
C_4	Carry Output	10/5.0	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '83A adds two 4-bit binary words (A and B) plus the incoming carry. The binary sum appears on the sum outputs (S_0 — S_3) and outgoing carry (C_4) outputs.

$$C_0 + (A_0 + B_0) + 2(A_1 + B_1) + 4(A_2 + B_2) + 8(A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

Where: (+) = plus

Due to the symmetry of the binary add function the '83A can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry In can not be left open, but must be held LOW when no carry in is intended.

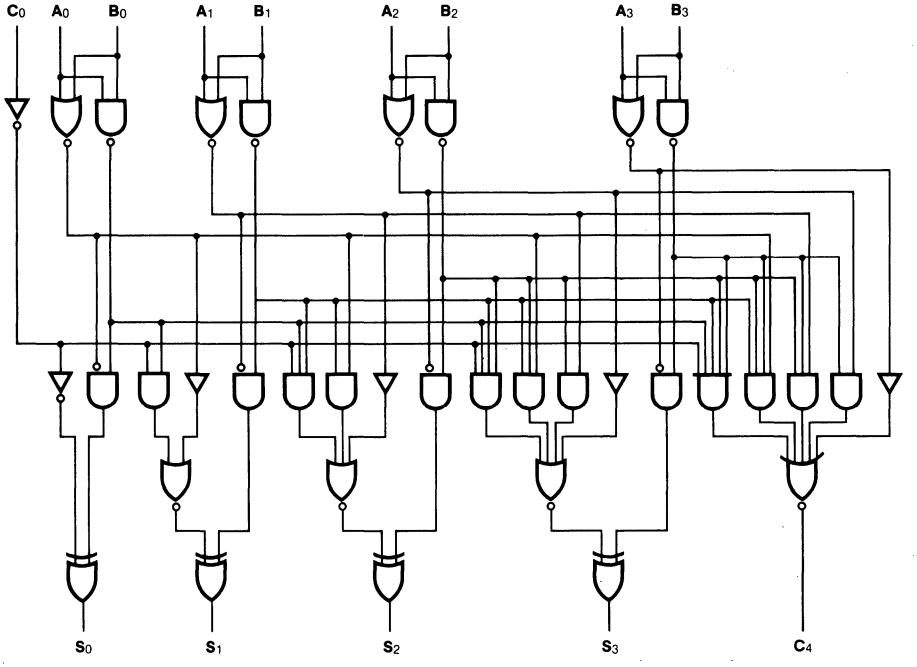
Interchanging inputs of equal weight does not affect the operation, thus C_0, A_0, B_0 can be arbitrarily assigned to pins 10, 11, 13, etc.

TRUTH TABLE

	INPUTS									OUTPUTS					
	C_0	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	S_0	S_1	S_2	S_3	C_4	
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10 + 9 = 19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry + 5 + 6 = 12)

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

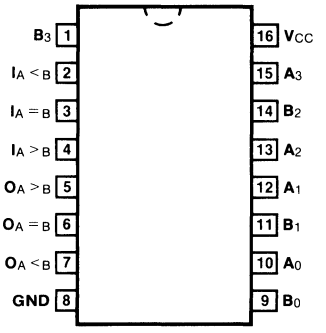
SYMBOL	PARAMETER		54/74		54/74LS		UNITS	CONDITIONS
			Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current at S_n	XM	-20	-55	-20	-100	mA	V_{CC} = Max
		XC	-18	-55	-20	-100		
I_{OS}	Output Short Circuit Current at C_4	XM	-20	-70	-20	-100	mA	V_{CC} = Max
		XC	-18	-70	-20	-100		
I_{CC}	Power Supply Current	XM		99		39	mA	V_{CC} = Max, Inputs = Gnd ('LS83A)
		XC		110		39		Inputs = 4.5 V ('83A)

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω		54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay C_0 to S_n		21 21		24 24	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to S_n		24 24		24 24	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay C_0 to C_4		14 16		17 17	ns	Figs. 3-1, 3-5 R_L = 780 Ω ('83A)
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to C_4		14 16		17 17	ns	Figs. 3-1, 3-5 R_L = 780 Ω ('83A)

54/7485
54LS/74LS85
4-BIT MAGNITUDE COMPARATOR

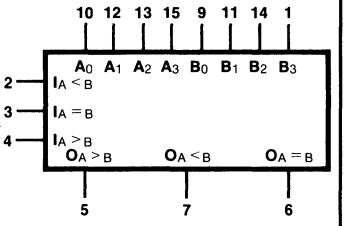
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '85 is a high speed, expandable 4-bit magnitude comparator which compares two 4-bit words in any monotonic code (binary, BCD or other) and generates three outputs: A less than B, A greater than B, and A equal to B. Three expansion inputs allow serial (ripple) expansion over any word length without external gates.

- **EASILY EXPANDABLE**
- **BINARY OR BCD COMPARISON**
- **A > B, A < B, A = B OUTPUTS AVAILABLE**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

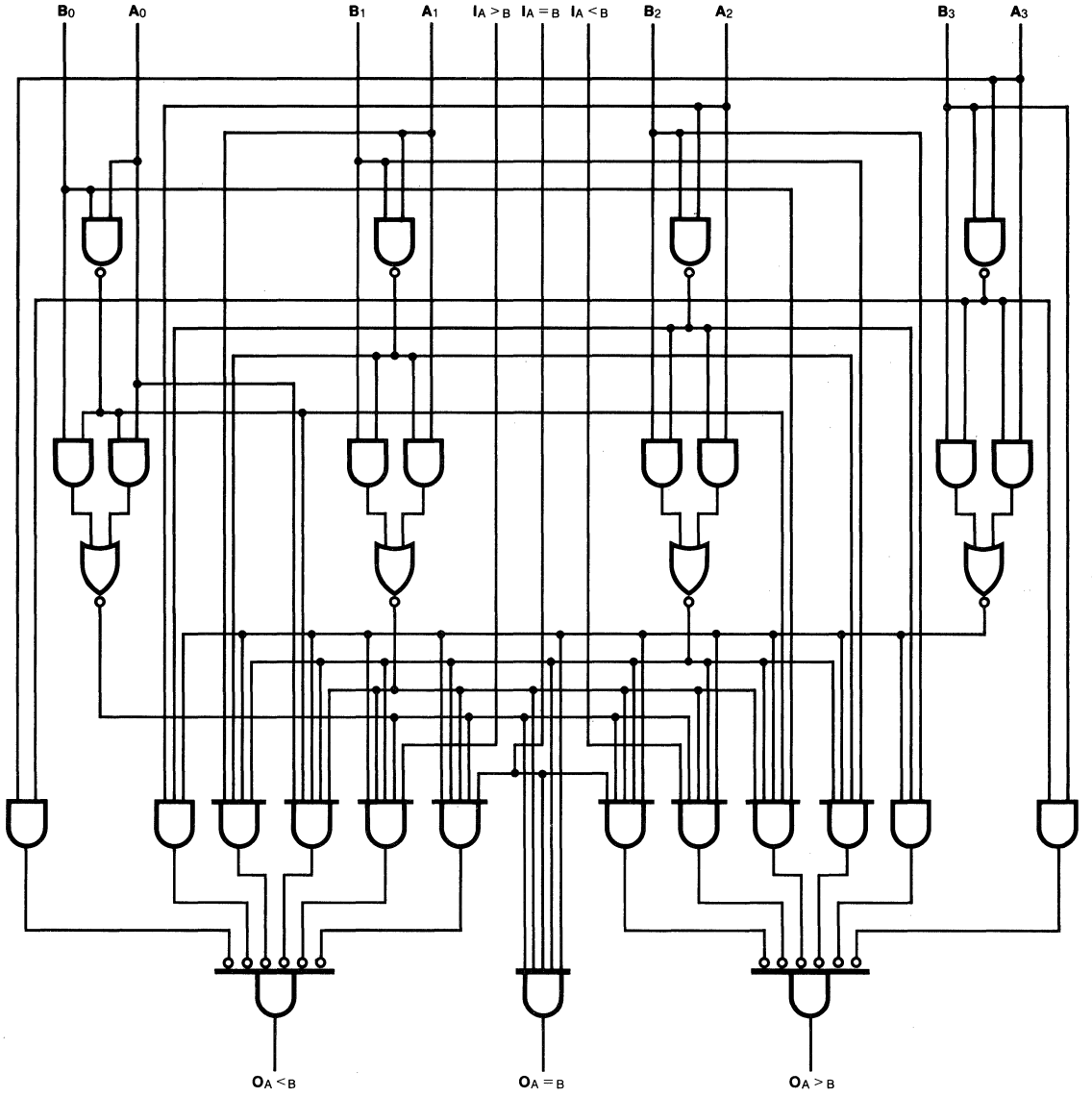
PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7485PC, 74LS85PC		9B
Ceramic DIP (D)	A	7485DC, 74LS85DC	5485DM, 54LS85DM	6B
Flatpak (F)	A	7485FC, 74LS85FC	5485FM, 54LS85FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	Word A Inputs	3.0/3.0	1.5/0.75
$B_0 - B_3$	Word B Inputs	3.0/3.0	1.5/0.75
$I_{A=B}$	A = B Expansion Input	3.0/3.0	1.5/0.75
$I_{A<B}$, $I_{A>B}$	A < B, A > B Expansion Inputs	1.0/1.0	0.5/0.25
$O_{A>B}$	A Greater Than B Output	10/10	10/5.0 (2.5)
$O_{A<B}$	A Less Than B Output	10/10	10/5.0 (2.5)
$O_{A=B}$	A Equal B Output	10/10	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION—The '85 compares two 4-bit words (A, B). Each word has four parallel inputs (A_0—A_3, B_0—B_3) of which A_3 and B_3 are the most significant. Three expander inputs ($I_{A>B}$, $I_{A<B}$, $I_{A=B}$) allow cascading without external gates. The three outputs ($O_{A>B}$, $O_{A<B}$, $O_{A=B}$) have only two gate delays from the expander inputs, thus reducing the delay time when units are cascaded for long words. The $I_{A=B}$ input to the least significant position must be held HIGH for proper compare operation. For serial (ripple) expansion, the A > B, A < B and A = B outputs are connected respectively to the $I_{A>B}$, $I_{A<B}$, and $I_{A=B}$ inputs of the next most significant comparator.

LOGIC DIAGRAM



TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3 > B_3$	X	X	X	X	X	X	H	L	L
$A_3 < B_3$	X	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	X	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	H	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	H	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

APPLICATIONS — *Figure a* shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in *Figure b* six levels of device delay result when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table I.

TABLE I

WORD LENGTH	NUMBER OF PKGS.
1-4 Bits	1
5-24 Bits	2-6
25-120 Bits	8-31

NOTE:
The 54LS/74LS85 can be used as a 5-bit comparator only when the outputs are used to drive the A_0 — A_3 and B_0 — B_3 inputs of another 54LS/74LS85 as shown in Figure 2 in positions #1, 2, 3, and 4.

MSB = Most Significant Bit
LSB = Least Significant Bit

L = LOW Level
H = HIGH Level
NC = No Connection

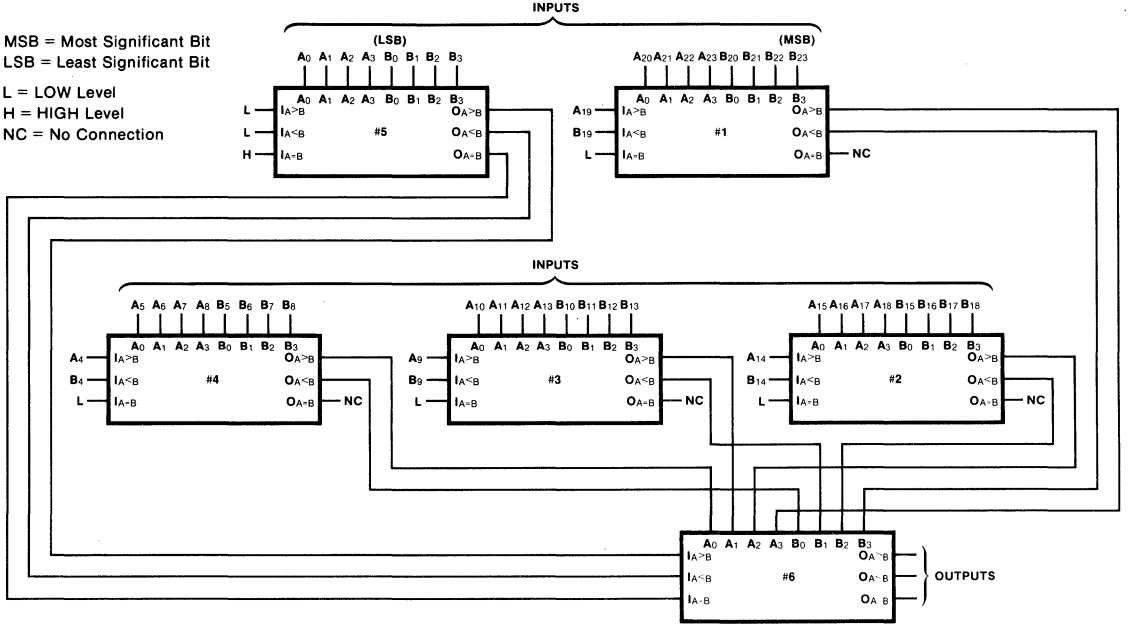
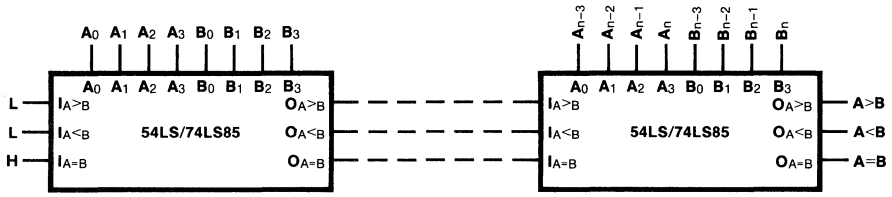


Fig. a Comparison of Two 24-Bit Words



L = LOW Level
H = HIGH Level

Fig. b Comparison of Two n-Bit Words

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	XM	-20	-55	-20	-100	mA	V_{CC} = Max
		XC	-18	-55				
I_{CC}	Power Supply Current			88		20	mA	V_{CC} = Max $I_{A=B}$ = Gnd Other Inputs Open

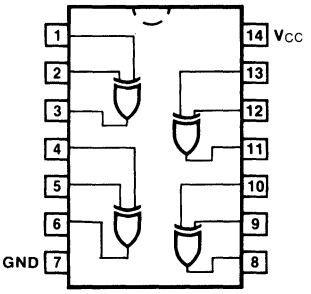
AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to $O_{A>B}$ or $O_{A<B}$		26 30		36 30	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to $O_{A=B}$		35 30		45 45	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay A_n I_{xx} to $O_{A>B}$ or $O_{A<B}$		11 17		22 17	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay $I_{A=B}$ to $O_{A=B}$		20 17		22 17	ns	Figs. 3-1, 3-5

54/7486
54S/74S86
54LS/74LS86

QUAD 2-INPUT EXCLUSIVE-OR GATE

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7486PC, 74S86PC 74LS86PC		9A
Ceramic DIP (D)	A	7486DC, 74S86DC 74LS86DC	5486DM, 54S86DM 54LS86DM	6A
Flatpak (F)	A	7486FC, 74S86FC 74LS86FC	5486FM, 54S86FM 54LS86FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.0/0.375
Outputs	20/10	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		43		75		10	mA	V_{CC} = Max, V_{IN} = Gnd
		XC		50		75		10		
t_{PLH}	Propagation Delay			23	3.5	10.5		12	ns	Other Input LOW
t_{PHL}				17	3.0	10		17		Figs. 3-1, 3-5
t_{PLH}	Propagation Delay			30	3.5	10.5		13	ns	Other Input HIGH
t_{PHL}				22	3.0	10		12		Figs. 3-1, 3-4

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54H/74H87

4-BIT TRUE/COMPLEMENT, ZERO/ONE ELEMENT

DESCRIPTION — The '87 performs four operations at its outputs, depending on the state of the Select inputs S_1 and S_2. The outputs can be forced HIGH or LOW, or can follow the Data inputs in either the True or Complement form. The Select input coding and the output responses are shown in the Truth Table.

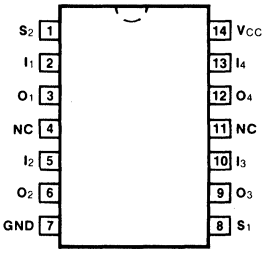
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74H87PC		9A
Ceramic DIP (D)	A	74H87DC	54H87DM	6A
Flatpak (F)	A	74H87FC	54H87FM	3I

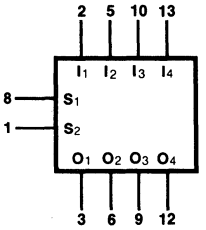
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74H (U.L.) HIGH/LOW
I_1 — I_4	Data Inputs	1.25/1.25
S_1, S_2	Select Inputs	1.25/1.25
O_1 — O_4	Outputs	25/12.5

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



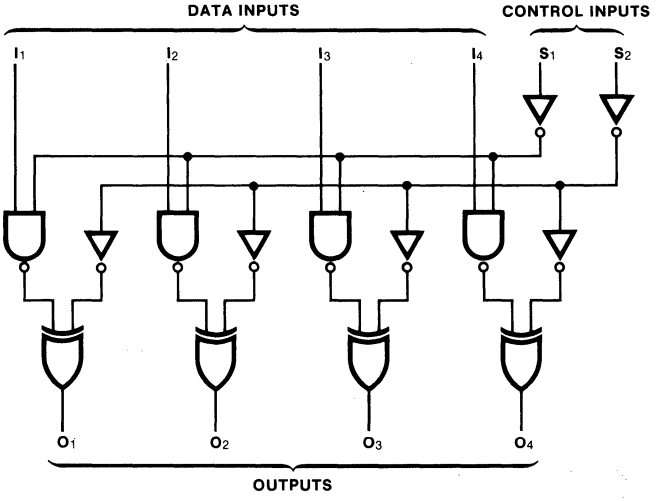
V_{CC} = Pin 14
GND = Pin 7

TRUTH TABLE

SELECT INPUTS		OUTPUTS			
S_1	S_2	O_1	O_2	O_3	O_4
L	L	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$
L	H	I_1	I_2	I_3	I_4
H	L	H	H	H	H
H	H	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74H Min	54/74H Max	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage		2.4		V	V_{CC} = Min, I_{OH} = -1.0 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V
I_{CC}	Power Supply Current	XM		78	mA	V_{CC} = Max
		XC		89		

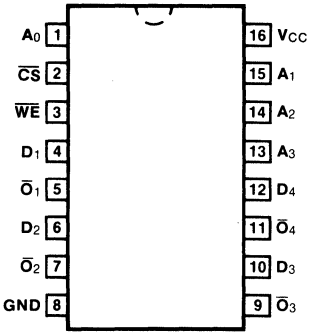
AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74H C_L = 25 pF R_L = 280 Ω Min	54/74H Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay I_n to O_n		20 19	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay S_n to O_n		25 25	ns	

54/7489
54LS/74LS89

64-BIT RANDOM ACCESS MEMORY
(With Open-Collector Outputs)

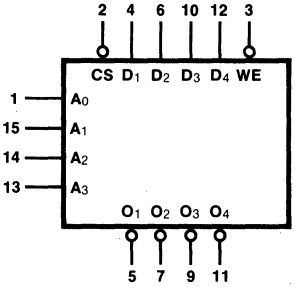
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '89 a high speed, low power 64-bit Random Access Memory organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading, and addresses are fully decoded on-chip. Outputs are open-collector type and are in the off (HIGH) state when both the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) are HIGH. For all other combinations of $\overline{CS}$ and $\overline{WE}$ the outputs are active, presenting the complement of either the stored data (READ mode) or the information present on the D inputs.

- **OPEN-COLLECTOR OUTPUTS FOR WIRED-AND APPLICATIONS**
- **BUFFERED INPUTS MINIMIZE LOADING**
- **ADDRESS DECODING ON-CHIP**
- **DIODE CLAMPED INPUTS MINIMIZE RINGING**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7489PC, 74LS89PC		9B
Ceramic DIP (D)	A	7489DC, 74LS89DC	5489DM, 54LS89DM	7B
Flatpak (F)	A	7489FC, 74LS89FC	5489FM, 54LS89FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	1.0/1.0	0.5/0.013
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	0.5/0.013
$\overline{WE}$	Write Enable Input (Active LOW)	1.0/1.0	0.5/0.013
$D_1 - D_4$	Data Inputs	1.0/1.0	0.5/0.013
$\overline{O}_1 - \overline{O}_4$	Inverted Data Outputs	OC*/7.5	OC*/10 (5.0)

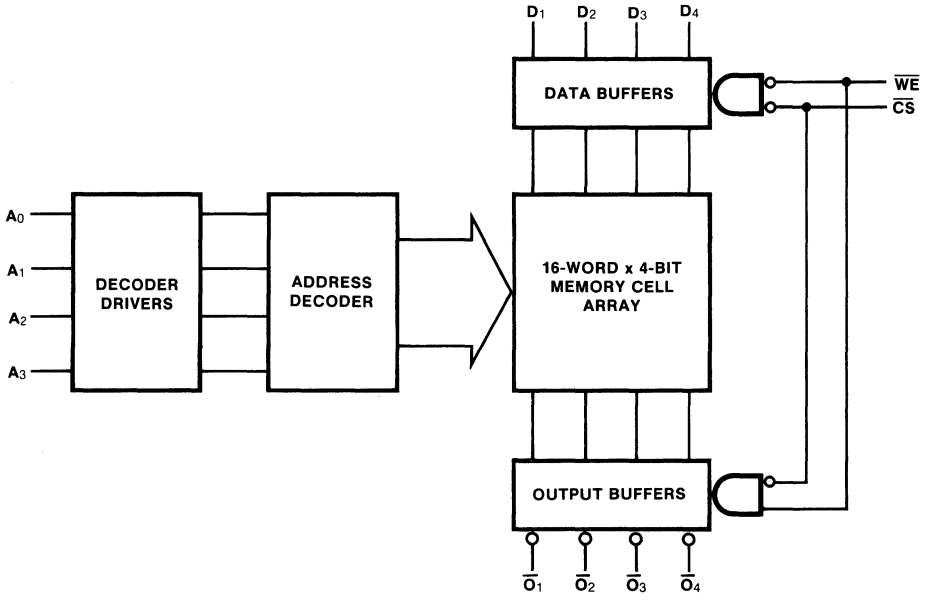
*OC — Open Collector

FUNCTION TABLE

INPUTS		OPERATION	CONDITION OF OUTPUTS
$\overline{CS}$	$\overline{WE}$		
L	L	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Entry	Undetermined
H	H	Hold	(Off) HIGH

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{OH}	Output HIGH Current			20		20	μA	V_{CC} = Min, V_{OH} = 5.5 V	
V_{OL}	Output LOW Voltage			0.4			V	I_{OL} = 12 mA	V_{CC} = Min
				0.45				I_{OL} = 16 mA	
		XM, XC				0.4	V	I_{OL} = 8.0 mA	V_{CC} = Min
		XC				0.5		I_{OL} = 16 mA	
I_{CC}	Power Supply Current			105		40	mA	V_{CC} = Min, $\overline{CS}$ = Gnd	
C_O	Off-State Output Capacitance			4.0*		4.0*	pF	V_O = 2.4 V, f = 1 MHz	

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 30 pF, R_L = 300 Ω Min	54/74 Max	54/74LS C_L = 15 pF, R_L = 2 kΩ Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay $\overline{CS}$ to $\overline{O}_n$		50 50		10* 10*	ns	Figs. 3-2, 3-5 '89 has 600 Ω to Gnd
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$		60 60		37* 37*	ns	Figs. 3-2, 3-20 '89 has 600 Ω to Gnd
t_{rec}	Recovery Time $\overline{WE}$ to $\overline{O}_n$		70		30*	ns	Figs. 3-2, 3-4, 3-5 '89 has 600 Ω to Gnd

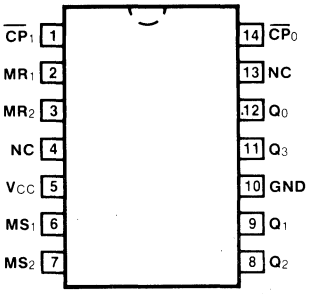
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to $\overline{WE}$	40 40		25* 25*		ns	Fig. 3-13
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to $\overline{WE}$	0 0		10* 10*		ns	Fig. 3-21
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n or A_n to $\overline{WE}$	5.0 5.0		0* 0*		ns	Figs. 3-13, 3-21
t_w (L)	$\overline{WE}$ Pulse Width LOW	40		25*		ns	Fig. 3-21

*Typical Value

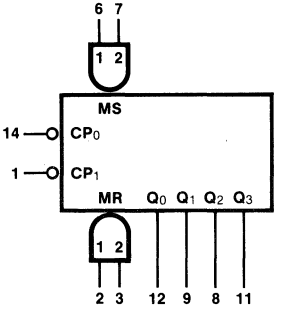
54/7490A
54LS/74LS90
DECADE COUNTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '90 is a 4-stage ripple counter containing a high speed flip-flop acting as a divide-by-two and three flip-flops connected as a divide-by-five counter. It can be connected to operate with a conventional BCD output pattern or it can be connected to provide a 50% duty cycle output. In the BCD mode, HIGH signals on the Master Set (MS) inputs set the outputs to BCD nine. HIGH signals on the Master Reset (MR) inputs force all outputs LOW. For a similar counter with corner power pins, see the 'LS290; for dual versions, see the 'LS390 and 'LS490.

LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 10
NC = Pins 4, 13

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7490APC, 74LS90PC		9A
Ceramic DIP (D)	A	7490ADC, 74LS90DC	5490ADM, 54LS90DM	6A
Flatpak (F)	A	7490AFC, 74LS90FC	5490AFM, 54LS90FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. defintions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CP}_0$	÷2 Section Clock Input (Active Falling Edge)	2.0/2.0	0.125/1.5
$\overline{CP}_1$	÷5 Section Clock Input (Active Falling Edge)	3.0/3.0	0.250/2.0
MR_1, MR_2	Asynchronous Master Reset Inputs (Active HIGH)	1.0/1.0	0.5/0.25
MS_1, MS_2	Asynchronous Master Set (Preset 9) Inputs (Active HIGH)	1.0/1.0	0.5/0.25
Q_0	÷2 Section Output*	20/10	10/5.0 (2.5)
Q_1 — Q_3	÷5 Section Outputs	20/10	10/5.0 (2.5)

*The Q_0 output is guaranteed to drive the full rated fan-out plus the $\overline{CP}_1$ input.

FUNCTIONAL DESCRIPTION — The '90 is a 4-bit ripple type decade counter. It consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input. A gated AND asynchronous Master Reset (MR_1, MR_2) is provided which overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set (MS_1, MS_2) is provided which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH). Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.:

A. BCD Decade (8421) Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_3	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

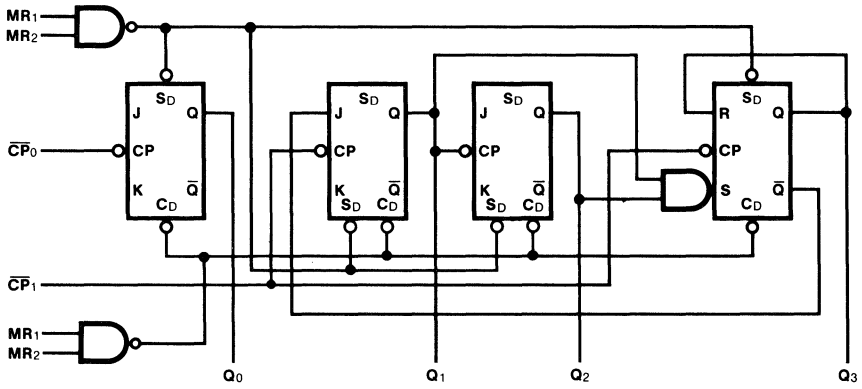
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

BCD COUNT SEQUENCE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input $\overline{CP}_1$ for BCD count.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max				
I_{IH}	Input HIGH Current, $\overline{CP}_0$		1.0		0.2	mA	V_{CC} = Max, V_{IN} = 5.5 V
I_{IH}	Input HIGH Current $\overline{CP}_1$		1.0		0.4	mA	V_{CC} = Max, V_{IN} = 5.5 V
I_{CC}	Power Supply Current		42		15	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω		54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max	Min	Max		
f_{max}	Maximum Count Frequency, $\overline{CP}_0$	32		32		MHz	Figs. 3-1, 3-9
f_{max}	Maximum Count Frequency, $\overline{CP}_1$	16		16		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_0$ to Q_0		16 18		16 18	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_0$ to Q_3		48 50		48 50	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_1$ to Q_1		16 21		16 21	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_1$ to Q_2		32 35		32 35	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_1$ to Q_3		32 35		32 35	ns	Figs. 3-1, 3-9
t_{PLH}	Propagation Delay MS to Q_0 and Q_3		30		30	ns	Figs. 3-1, 3-17
t_{PHL}	Propagation Delay MS to Q_1 and Q_3		40		40	ns	Figs. 3-1, 3-17
t_{PHL}	Propagation Delay MR to Q_n		40		40	ns	Figs. 3-1, 3-17

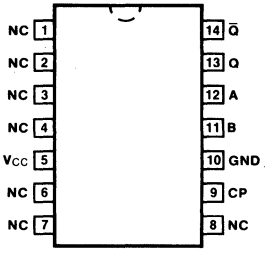
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_w (H)	$\overline{CP}_0$ Pulse Width HIGH	15		15		ns	Fig. 3-9
t_w (H)	$\overline{CP}_1$ Pulse Width HIGH	30		30		ns	Fig. 3-9
t_w (H)	MS Pulse Width HIGH	15		15		ns	Fig. 3-17
t_w (H)	MR Pulse Width HIGH	15		15		ns	Fig. 3-17
t_{rec}	Recovery Time, MS to $\overline{CP}$	25		25		ns	Fig. 3-17
t_{rec}	Recovery Time, MR to $\overline{CP}$	25		25		ns	Fig. 3-17

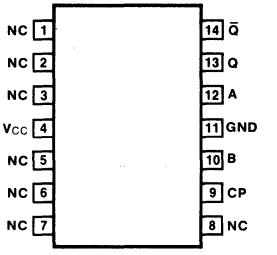
54/7491A

8-BIT SHIFT REGISTER

CONNECTION DIAGRAMS
PINOUT A

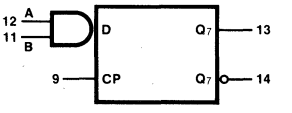


PINOUT B



DESCRIPTION — The '91 is a serial-in, serial-out, 8-bit shift register. It is composed of eight RS master/slave flip-flops, input gating and a clock driver. The register is capable of storing and transferring data at clock rates up to 18 MHz while maintaining a typical noise immunity level of 1.0 V.

LOGIC SYMBOL
(Pinout A only)



VCC = Pin 5
GND = Pin 10

ORDERING CODE: See Section 9

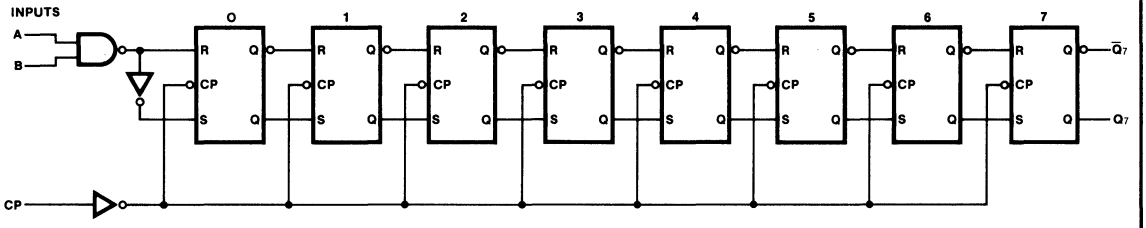
PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7491APC		9A
Ceramic DIP (D)	A	7491ADC	7491ADM	6A
Flatpak (F)	B	7491AFC	7491AFM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
A, B	Serial Data Inputs	1.0/1.0
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0
Q_7	Data Output	10/10
$\bar{Q}_7$	Complementary Data Output	10/10

FUNCTIONAL DESCRIPTION — Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B, and CP) appear as only one TTL input load. The clock pulse inverter/driver causes these circuits to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift register to be fully compatible with other edge-triggered synchronous functions.

LOGIC DIAGRAM

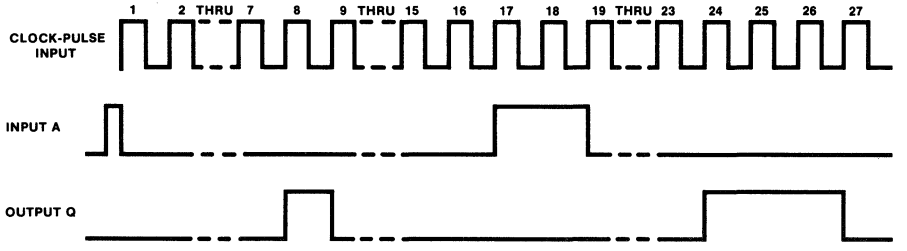


TRUTH TABLE

INPUTS		OUTPUT
t_n		t_{n+8}
A	B	Q_7
L	L	L
L	H	L
H	L	L
H	H	H

NOTES:
t_n = Bit time before clock pulse.
t_{n+8} = Bit time after eight clock pulses.
H = HIGH Voltage Level
L = LOW Voltage Level

TYPICAL INPUT/OUTPUT WAVEFORMS



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		50	mA	V_{CC} = Max*
		XC		58		

*I_{CC} is measured after the eighth clock pulse with the output open and A and B inputs grounded

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

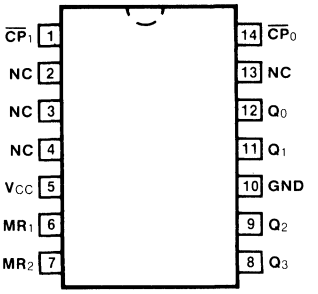
SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 C_L = 15 pF, R_L = 400 Ω Max	UNITS	CONDITIONS
f_{max}	Maximum Shift Frequency	10		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_7 or $\overline{Q}_7$		40 40	ns	Figs. 3-1, 3-8

AC OPERATING REQUIREMENTS: V_{CC} +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
t_s (H)	Setup Time HIGH, D to CP	25		ns	Fig. 3-6
t_h (H)	Hold Time HIGH, D to CP	0		ns	Fig. 3-6
t_s (L)	Setup Time LOW, D to CP	25		ns	Fig. 3-6
t_h (L)	Hold Time LOW, D to CP	0		ns	Fig. 3-6
t_w (H)	CP Pulse Width HIGH	25		ns	Fig. 3-8

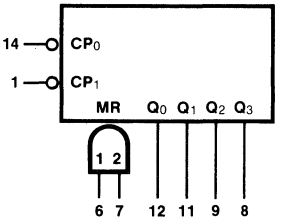
54/7492A
54LS/74LS92
DIVIDE-BY-TWELVE COUNTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '92 is a 4-stage ripple counter containing a high speed flip-flop acting as a divide-by-two and three flip-flops connected as a divide-by-six. HIGH signals on the Master Reset (MR) inputs override the clocks and force all outputs to the LOW state.

LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 10
NC = Pins 2, 3, 4, 13

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	7492APC, 74LS92PC		9A
Ceramic DIP (D)	A	7492ADC, 74LS92DC	5492ADM, 54LS92DM	6A
Flatpak (F)	A	7492AFC, 74LS92FC	5492AFM, 54LS92FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CP}_0$	÷2 Section Clock Input (Active Falling Edge)	2.0/2.0	0.125/1.5
$\overline{CP}_1$	÷6 Section Clock Input (Active Falling Edge)	3.0/3.0	0.250/2.0
MR_1, MR_2	Asynchronous Master Reset Input (Active HIGH)	1.0/1.0	0.5/0.25
Q_0	÷2 Section Output*	20/10	10/5.0 (2.5)
Q_1 — Q_3	÷6 Section Outputs	20/10	10/5.0 (2.5)

*The Q_0 output is guaranteed to drive the full rated fan-out plus the $\overline{CP}_1$ input.

FUNCTIONAL DESCRIPTION — The '92 is a 4-bit ripple type divide-by-twelve counter. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divideby-six section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device. A gated AND asynchronous Master Reset (MR_1, MR_2) is provided which overrides the clocks and resets (clears) all the flip-flops. Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

A. Modulo 12, Divide-By-Twelve Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and Q_3 produces a symmetrical divide-by-twelve square wave output.

B. Divide-By-Two and Divide-By-Six Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The $\overline{CP}_1$ input is used to obtain divide-by-three operation at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

MODE SELECTION TABLE

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

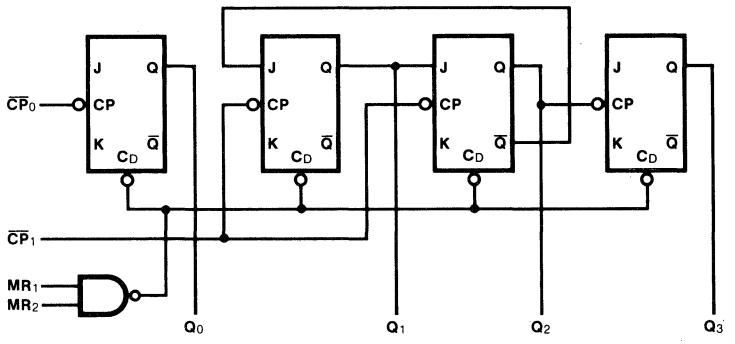
H = HIGH Voltage Level
L = LOW Voltage Level

TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

NOTE: Output Q_0 connected to $\overline{CP}_1$

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{IH}	Input HIGH Current, $\overline{CP}_0$		1.0		0.2	mA	V_{CC} = Max, V_{IN} = 5.5 V
I_{IH}	Input HIGH Current, $\overline{CP}_1$		1.0		0.4	mA	V_{CC} = Max, V_{IN} = 5.5 V
I_{CC}	Power Supply Current		39		15	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25° C (See Section 3 for waveforms and load configurations)

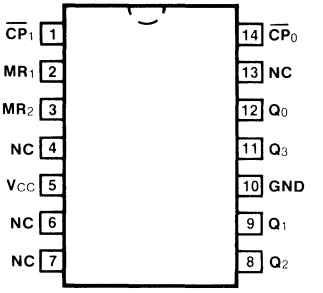
SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω		54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max	Min	Max		
f_{max}	Maximum Count Frequency, $\overline{CP}_0$ Input	32		32		MHz	Figs. 3-1, 3-9
f_{max}	Maximum Count Frequency, $\overline{CP}_1$ Input	16		16		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_0$ to Q_0		16 18		16 18	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_0$ to Q_3		48 50		48 50	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_1$ to Q_1		16 21		16 21	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_1$ to Q_2		16 21		16 21	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_1$ to Q_3		32 35		32 35	ns	Figs. 3-1, 3-9
t_{PHL}	Propagation Delay, MR to Q_n		40		40	ns	Figs. 3-1, 3-17

AC OPERATING REQUIREMENTS: V_{CC} = 5.0 V, T_A = 25° C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_w (H)	$\overline{CP}_0$ Pulse Width HIGH	15		15		ns	Fig. 3-9
t_w (H)	$\overline{CP}_1$ Pulse Width HIGH	30		30		ns	
t_w (H)	MR Pulse Width HIGH	15		15		ns	Fig. 3-17
t_{rec}	Recovery Time, MR to CP	25		25		ns	

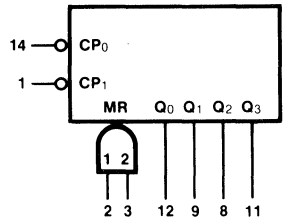
54/7493A
54LS/74LS93
DIVIDE-BY-SIXTEEN COUNTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '93 is a 4-stage ripple counter containing a high speed flip-flop acting as a divide-by-two and three flip-flops connected as a divide-by-eight. HIGH signals on the Master Reset (MR) inputs override the clocks and force all outputs to the LOW state.

LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 10
NC = Pins 4, 6, 7, 13

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	7493APC, 74LS93PC		9A
Ceramic DIP (D)	A	7493ADC, 74LS93DC	5493ADM, 54LS93DM	6A
Flatpak (F)	A	7493AFC, 74LS93FC	5493AFM, 54LS93FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CP}_0$	÷2 Section Clock Input (Active Falling Edge)	2.0/2.0	1.0/1.5
$\overline{CP}_1$	÷5 Section Clock Input (Active Falling Edge)	2.0/2.0	1.0/1.0
MR_1, MR_2	Asynchronous Master Reset Inputs (Active HIGH)	1.0/1.0	0.5/0.25
Q_0	÷2 Section Output*	20/10	10/5.0 (2.5)
Q_1 — Q_3	÷8 Section Outputs	20/10	10/5.0 (2.5)

*The Q_0 output is guaranteed to drive the full rated fan-out plus the $\overline{CP}_1$ input.

FUNCTIONAL DESCRIPTION — The '93 is a 4-bit ripple type binary counter. It consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device. A gated AND asynchronous Master Reset (MR_1, MR_2) is provided which overrides the clocks and resets (clears) all the flip-flops. Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

A. 4-Bit Ripple Counter — The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the Truth Table.

B. 3-Bit Ripple Counter — The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

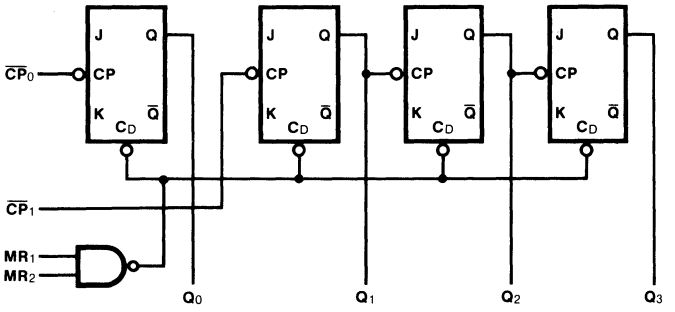
H = HIGH Voltage Level
L = LOW Voltage Level

TRUTH TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE: Output Q_0 connected to $\overline{CP}_1$.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{IH}	Input HIGH Current $\overline{CP_0}$ or $\overline{CP_1}$		1.0		0.2	mA	V_{CC} = Max, V_{IN} = 5.5 V
I_{CC}	Power Supply Current		39		15	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω		54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max	Min	Max		
f_{max}	Maximum Count Frequency $\overline{CP_0}$ Input	32		32		MHz	Figs. 3-1, 3-9
f_{max}	Maximum Count Frequency $\overline{CP_1}$ Input	16		16		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_0}$ to Q_0		16 18		16 18	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_0}$ to Q_3		70 70		70 70	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_1		16 21		16 21	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_2		32 35		32 35	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_3		51 51		51 51	ns	Figs. 3-1, 3-9
t_{PHL}	Propagation Delay MR to Q_n		40		40	ns	Figs. 3-1, 3-17

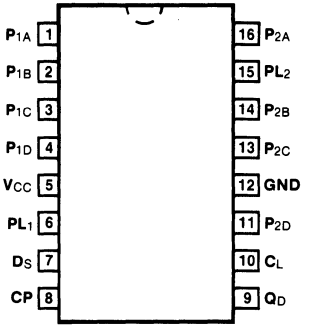
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_w (H)	$\overline{CP_0}$ Pulse Width HIGH	15		15		ns	Fig. 3-9
t_w (H)	$\overline{CP_1}$ Pulse Width HIGH	30		30		ns	Fig. 3-9
t_w (H)	MR Pulse Width HIGH	15		15		ns	Fig. 3-17
t_{rec}	Recovery Time, MR to $\overline{CP}$	25		25		ns	Fig. 3-17

54/7494

4-BIT SHIFT REGISTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '94 contains four dc coupled RS master/slave flip-flops with serial data entry into the first stage for synchronous Serial-in/ Serial-out operation, and with a common asynchronous Clear and two sets of individual asynchronous Preset inputs. Preset inputs P_{1X} are enabled by a HIGH signal on PL_1 and Preset inputs P_{2X} are enabled by a HIGH signal on PL_2. The normal procedure for paralled entry of data consists of re-setting the flip-flops by applying a momentary HIGH signal to CL, followed by a HIGH signal on either PL_1, or PL_2, depending on which set of parallel data is desired. For serial operation the CL and both PL inputs must be LOW. Serial transfer is initiated by the rising edge of the clock.

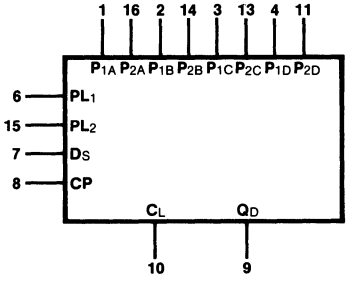
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7494PC		9B
Ceramic DIP (D)	A	7494DC	5494DM	7B
Flatpak (F)	A	7494FC	5494FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
P_{1A} — P_{1D}	Source 1 Parallel Data Inputs	1.0/1.0
P_{2A} — P_{2D}	Source 2 Parallel Data Inputs	1.0/1.0
PL_1	Asynchronous Parallel Load Input (Source 1)	4.0/4.0
PL_2	Asynchronous Parallel Load Input (Source 2)	4.0/4.0
D_S	Serial Data Input	1.0/1.0
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0
CL	Asynchronous Clear Input (Active HIGH)	1.0/1.0
Q_D	Serial Data Output	10/10

LOGIC SYMBOL



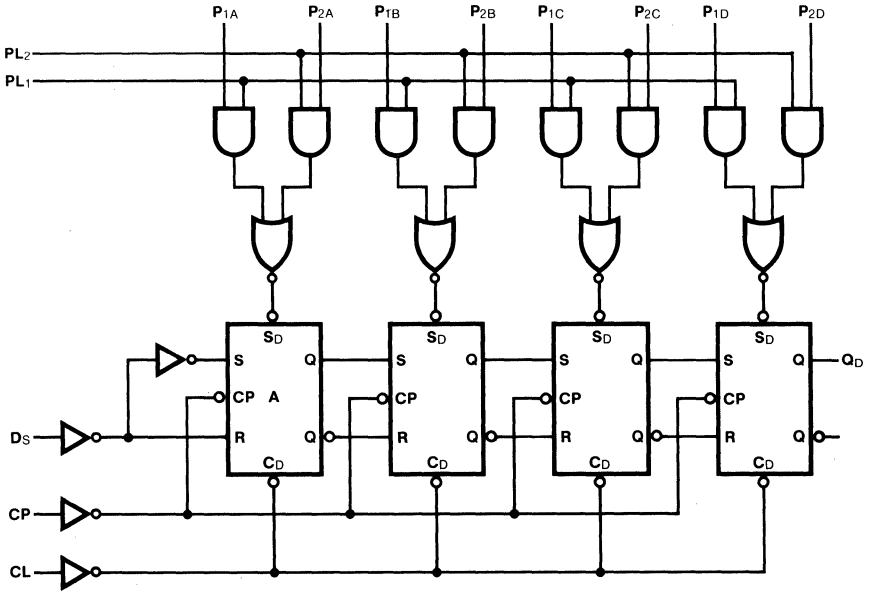
V_{CC} = Pin 5
GND = Pin 12

TRUTH TABLE

INPUTS				OUTPUTS	RESPONSE
CP	CL	$PL_1 \bullet P_{1D}$	$PL_2 \bullet P_{2D}$	Q_D	
X	H	L	L	L	Clear
X	L	H	X	H	Preset
X	L	X	H	H	Preset
X	H	H	X	H	Indeterminate
X	H	X	H	H	Indeterminate
⎍	L	L	L	Q_C	Shift Right

NOTE: All four flip-flops respond in a similar manner.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		50	mA	V_{CC} = Max
		XC		58		

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C (See Section 3 for waveforms and load configurations)

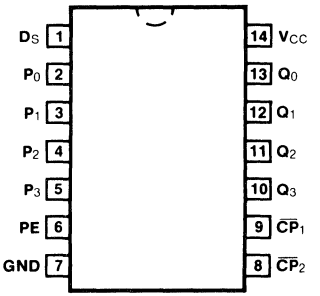
SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 C_L = 15 pF, R_L = 400 Ω Max	UNITS	CONDITIONS
f_{max}	Maximum Shift Frequency	10		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_D		40 40	ns	Figs. 3-1, 3-8
t_{PLH}	Propagation Delay, PL_n to Q_D		35	ns	Figs. 3-1, 3-17
t_{PHL}	Propagation Delay, CL to Q_D		40		

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
t_s (H)	Setup Time HIGH, D_S to CP	35		ns	Fig. 3-6
t_h (H)	Hold Time HIGH, D_S to CP	0		ns	
t_s (L)	Setup Time LOW, D_S to CP	25		ns	Fig. 3-6
t_h (L)	Hold Time LOW, D_S to CP	0		ns	
t_w (H)	CP Pulse Width HIGH	35		ns	Fig. 3-8
t_w (H)	CL Pulse Width HIGH	30		ns	Fig. 3-16
t_w (H)	PL_n Pulse Width HIGH	30		ns	Fig. 3-16

54/7495A
54LS/74LS95B
4-BIT RIGHT/LEFT SHIFT REGISTER

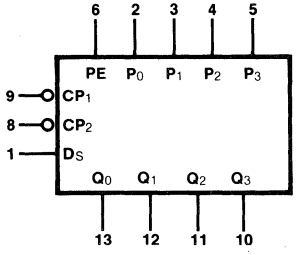
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '95 is a 4-bit shift register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH-to-LOW transition of the appropriate clock input.

- **SYNCHRONOUS, EXPANDABLE SHIFT RIGHT**
- **SYNCHRONOUS SHIFT LEFT CAPABILITY**
- **SYNCHRONOUS PARALLEL LOAD**
- **SEPARATE SHIFT AND LOAD CLOCK INPUTS**

LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7495APC, 74LS95BPC		9A
Ceramic DIP (D)	A	7495ADC, 74LS95BDC	5495ADM, 54LS95BDM	6A
Flatpak (F)	A	7495AFC, 74LS95BFC	5495AFM, 54LS95BFM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CP}_1$	Serial Clock Input (Active Falling Edge)	1.0/1.0	0.5/0.25
$\overline{CP}_2$	Parallel Clock Input (Active Falling Edge)	1.0/1.0	0.5/0.25
D_S	Serial Data Input	1.0/1.0	0.5/0.25
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0	0.5/0.25
PE	Parallel Enable Input (Active HIGH)	2.0/2.0	1.0/0.5
$Q_0 - Q_3$	Parallel Outputs	20/10	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '95 is a 4-bit shift register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel (P_0 — P_3) Data inputs and four Parallel Data outputs (Q_0 — Q_3). The serial or parallel mode of operation is controlled by a Parallel Enable input (PE) and two Clock inputs, $\overline{CP}_1$ and $\overline{CP}_2$. The serial (right-shift) or parallel data transfers occur synchronous with the HIGH-to-LOW transition of the selected clock input.

When PE is HIGH, $\overline{CP}_2$ is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}_2$ transfers parallel data from the P_0 — P_3 inputs to the Q_0 — Q_3 outputs. When PE is LOW, $\overline{CP}_1$ is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}_1$ transfers the data from Serial input (D_S) to Q_0 and shifts the data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3 respectively (right-shift). A left-shift is accomplished by externally connecting Q_3 to P_2, Q_2 to P_1, and Q_1 to P_0, and operating the '95 in the parallel mode (PE = HIGH). For normal operation, PE should only change states when both Clock inputs are LOW. However, changing PE from LOW to HIGH while $\overline{CP}_2$ is HIGH, or changing PE from HIGH to LOW while $\overline{CP}_1$ is HIGH and $\overline{CP}_2$ is LOW will not cause any changes on the register outputs.

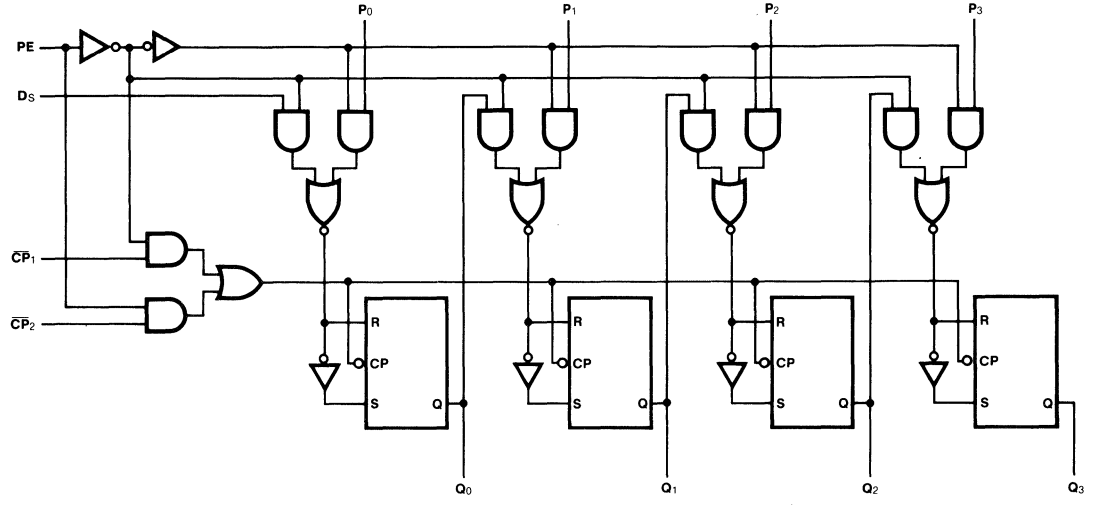
MODE SELECT TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	PE	$\overline{CP}_1$	$\overline{CP}_2$	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift	L	↓	X	l	X	L	q_0	q_1	q_2
	L	↓	X	h	X	H	q_0	q_1	q_2
Parallel Load	H	X	↓	X	p_n	p_0	p_1	p_2	p_3
Mode Change	↓	L	L	X	X	No Change			
	↑	L	L	X	X	No Change			
	↓	H	L	X	X	No Change			
	↑	H	L	X	X	Undetermined			
	↓	L	H	X	X	Undetermined			
	↑	L	H	X	X	No Change			
	↓	H	H	X	X	Undetermined			
	↑	H	H	X	X	No Change			

l = LOW Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.
p_n = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		63		21	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω		54/74LS C_L = 15 pF		UNITS	CONDITONS
		Min	Max	Min	Max		
f_{max}	Maximum Shift Frequency	25		30		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ or $\overline{CP_2}$ to Q_n		27 32		27 27	ns	Figs. 3-1, 3-9

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_S or P_n to $\overline{CP_n}$	15 15		20 20		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time HIGH or LOW D_S or P_n to $\overline{CP_n}$	0 0		10 10		ns	Fig. 3-7
t_w (H)	$\overline{CP_n}$ Pulse Width HIGH	20		20		ns	Fig. 3-9
t_{en} (L)	Enable Time LOW PE to $\overline{CP_1}$	15		25		ns	Fig. a
t_{inh} (H)	Inhibit Time HIGH PE to $\overline{CP_1}$	5.0		20		ns	Fig. a
t_{en} (H)	Enable Time HIGH PE to $\overline{CP_2}$	15		25		ns	Fig. a
t_{inh} (L)	Inhibit Time LOW PE to $\overline{CP_2}$	5.0		20		ns	Fig. a

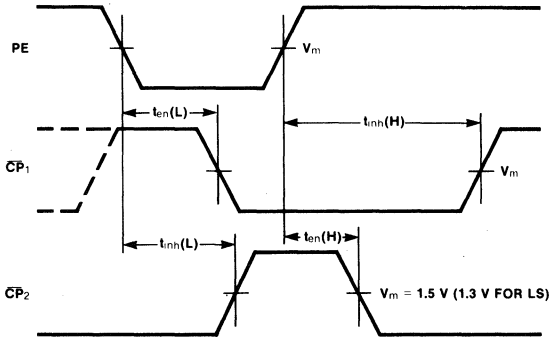


Fig. a

54/7496

5-BIT SHIFT REGISTER

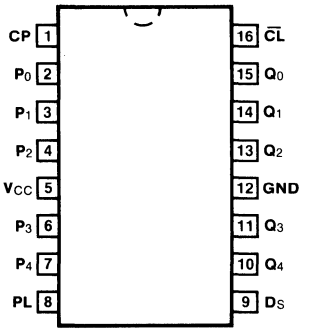
DESCRIPTION — The '96 consists of five RS master/slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to the LOW state by applying a low level voltage to the clear input. This condition may be applied independent of the state of the clock input.

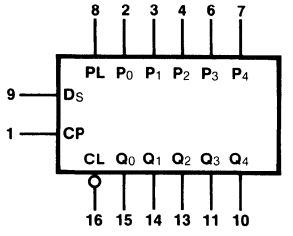
The flip-flops may be independently set to the HIGH state by applying a high level voltage to both the preset input of the specific flip-flop and the common parallel load input. The parallel enable input is provided to allow setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is independent of the state of the clock input or clear input.

Transfer of information to the output pins occurs when the clock input goes from a LOW level to a HIGH level. Since the flip-flops are RS master/slave circuits, the proper information must appear at the RS inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining RS inputs. The clear input must be at a HIGH level and the parallel load input must be at a LOW level for serial shifting.

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 5
GND= Pin 12

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	7496PC		9B
Ceramic DIP (D)	A	7496DC	5496DM	7B
Flatpak (F)	A	7496FC	5496FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

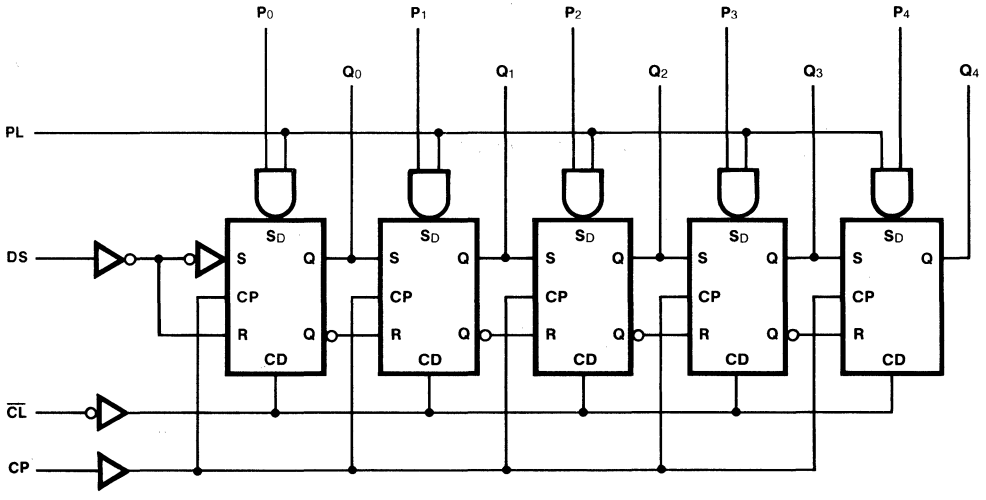
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\overline{CP}$	Clock Pulse Input (Active Rising Edge)	1.0/1.0
$\overline{CL}$	Asynchronous Clear Input (Active LOW)	1.0/1.0
D_S	Serial Data Input	1.0/1.0
P_0 — P_4	Parallel Data Inputs	1.0/1.0
PL	Asynchronous Parallel Load Input (Active HIGH)	5.0/5.0
Q_0 — Q_4	Parallel Outputs	10/10

MODE SELECT TABLE

INPUTS						OPERATION*
PL	P_n	$\overline{CL}$	D_S	CP	Q_n	
L	X	L	X	X	L	Clear; all outputs forced LOW
H	H**	H	X	X	H	Selectively Preset; each output
H	L**	H	X	X	L	set to its P input
L	X	H	H, L	⎍	Q_{n-1}	Shift right; $D_S \rightarrow Q_0$; $Q_0 \rightarrow Q_1$, etc.

*Simultaneous Preset and Clear operations produce undefined states.
**To insure proper presetting, P inputs must remain stable while PL is LOW.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		68	mA	V_{CC} = Max
		XC		79		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω Min	54/74 C_L = 15 pF R_L = 400 Ω Max	UNITS	CONDITIONS
f_{max}	Maximum Shift Frequency	10		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		40 40	ns	Figs. 3-1, 3-8
t_{PLH}	Propagation Delay, PL or P_n to Q_n		35	ns	Figs. 3-1, 3-16
t_{PHL}	Propagation Delay, $\overline{CL}$ to Q_n		55	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

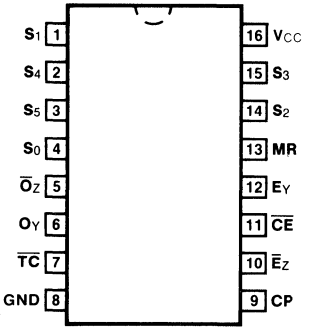
SYMBOL	PARAMETER	54/54 Min	54/54 Max	UNITS	CONDITIONS
t_w (L)	CP Pulse Width LOW	35		ns	Fig. 3-8
t_w (L)	$\overline{CL}$ Pulse Width LOW	30		ns	Fig. 3-16
t_w (H)	PL Pulse Width HIGH	30		ns	Fig. 3-16
t_s (H)	Setup Time HIGH, D_S to CP	30		ns	Fig. 3-6
t_h (H)	Hold Time HIGH, D_S to CP	0		ns	Fig. 3-6
t_s (L)	Setup Time LOW, D_S to CP	30		ns	Fig. 3-6
t_h (L)	Hold Time LOW, D_S to CP	0		ns	Fig. 3-6

54/7497

SYNCHRONOUS MODULO-64 BIT RATE MULTIPLIER

DESCRIPTION — The '97 contains a synchronous 6-stage binary counter and six decoding gates that serve to gate the clock through to the output at a sub-multiple of the input frequency. The output pulse rate, relative to the clock frequency, is determined by signals applied to the Select (S_0 — S_5) inputs. Both true and complement outputs are available, along with an enable input for each. A Count Enable input and a Terminal Count output are provided for cascading two or more packages. An asynchronous Master Reset input prevents counting and resets the counter.

CONNECTION DIAGRAM
PINOUT A



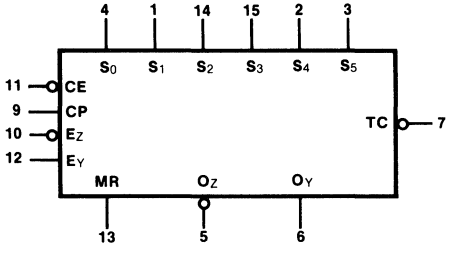
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7497PC		9B
Ceramic DIP (D)	A	7497DC	5497DM	7B
Flatpak (F)	A	7497FC	5497FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
S_0 — S_5	Rate Select Inputs	1.0/1.0
$\overline{E}_Z$	$\overline{O}_Z$ Enable Input (Active LOW)	1.0/1.0
E_Y	O_Y Enable Input	1.0/1.0
$\overline{CE}$	Count Enable Input (Active LOW)	1.0/1.0
CP	Clock Pulse Input (Active Rising Edge)	2.0/2.0
MR	Asynchronous Master Reset Input (Active HIGH)	1.0/1.0
$\overline{O}_Z$	Gated Clock Output (Active LOW)	10/10
O_y	Complement Output (Active HIGH)	10/10
$\overline{TC}$	Terminal Count Output (Active LOW)	10/10

LOGIC SYMBOL



V_{CC} = Pin 16
Gnd = Pin 8

FUNCTIONAL DESCRIPTION — The '97 contains six JK flip-flops connected as a synchronous modulo-64 binary counter. A LOW signal on the Count Enable ($\overline{CE}$) input permits counting, with all state changes initiated simultaneously by the rising edge of the clock. When the count reaches maximum (63), with all Qs HIGH, the Terminal Count ($\overline{TC}$) output will be LOW if $\overline{CE}$ is LOW. A HIGH signal on Master Reset (MR) resets the flip-flops and prevents counting, although output pulses can still occur if the clock is running, $\overline{E}_Z$ is LOW and S_5 is HIGH.

The flip-flop outputs are decoded by a 6-wide AND-OR-INVERT gate. Each AND gate also contains the buffered and inverted CP and Z-enable ($\overline{E}_Z$) functions, as well as one of the Select ($S_0 - S_5$) inputs. The Z output, $\overline{O}_Z$ is normally HIGH and goes LOW when CP and $\overline{E}_Z$ are LOW and any of the AND gates has its other inputs HIGH. The AND gates are enabled by the counter at different times and different rates relative to the clock. For example, the gate to which S_5 is connected is enabled during every other clock period, assuming S_5 is HIGH. Thus, during one complete cycle of the counter (64 clocks) the S_5 gate is enabled 32 times and can therefore gate 32 clocks per cycle to the output. The S_4 gate is enabled 16 times per cycle, the S_3 gate 8 times per cycle, etc. The output pulse rate thus depends on the clock rate and which of the $S_0 - S_5$ inputs is HIGH.

$$f_{out} = \frac{m}{64} \bullet f_{in}$$

Where: $m = S_5 \bullet 2^5 + S_4 \bullet 2^4 + S_3 \bullet 2^3 + S_2 \bullet 2^2 + S_1 \bullet 2^1 + S_0 \bullet 2^0$

Thus by appropriate choice of signals applied to the $S_0 - S_5$ inputs, the output pulse rate can range from 1/64 to 63/64 of the clock rate, as suggested in the Rate Select Table. There is no output pulse when the counter is in the "all ones" condition. When m is 1, 2, 4, 8, 16 or 32, the output pulses are evenly spaced, assuming that the clock frequency is constant. For any other value of m the output pulses are not evenly spaced, since the pulse train is formed by interleaving pulses passed by two or more of the AND gates. The Pulse Pattern Table indicates the output pattern for several values of m. In each row, a one means that the $\overline{O}_Z$ output will be HIGH during that entire clock period, while a zero means that $\overline{O}_Z$ will be LOW when the clock is LOW in that period. The first column in the output field coincides with the "all zeroes" condition of the counter, while the last column represents the "all ones" condition. The pulse pattern for any particular value of m can be deduced by factoring it into the sum of appropriate powers of two (e.g. 19 = 16 + 2 + 1) and combining the pulses (i.e., the zeroes) shown for each for the relevant powers of two (e.g., for m = 16, 2 and 1).

The Y output O_Y is the complement of $\overline{O}_Z$ and is thus normally LOW. A LOW signal on the Y-enable input, E_Y, disables O_Y. To expand the multiplier to 12-bit rate select, two packages can be cascaded as shown in *Figure a*. Both circuits operate from the basic clock, with the $\overline{TC}$ output of the first acting to enable both counting and the output pulses of the second package. Thus the second counter advances at only 1/64 the rate of the first and a full cycle of the two counters combined requires 4096 clocks. Each rate select input of the first package has 64 times the weight of its counterpart in the second package.

$$f_{out} = \frac{m_1 + m_2}{64 \bullet 64} \bullet f_{in}$$

Where: $m_1 = S_5 \bullet 2^{11} + S_4 \bullet 2^{10} + S_3 \bullet 2^9 + S_2 \bullet 2^8 + S_1 \bullet 2^7 + S_0 \bullet 2^6$ (first package)

$m_2 = S_5 \bullet 2^5 + S_4 \bullet 2^4 + S_3 \bullet 2^3 + S_2 \bullet 2^2 + S_1 \bullet 2^1 + S_0 \bullet 2^0$ (second package)

Combined output pulses are obtained in *Figure a* by letting the Z output of the first circuit act as the Y-enable function for the second, with the interleaved pulses obtained from the Y output of the second package being opposite in phase to the clock.

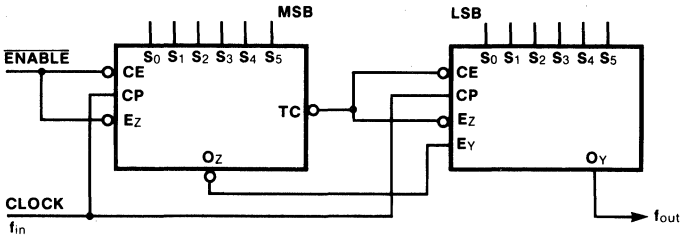
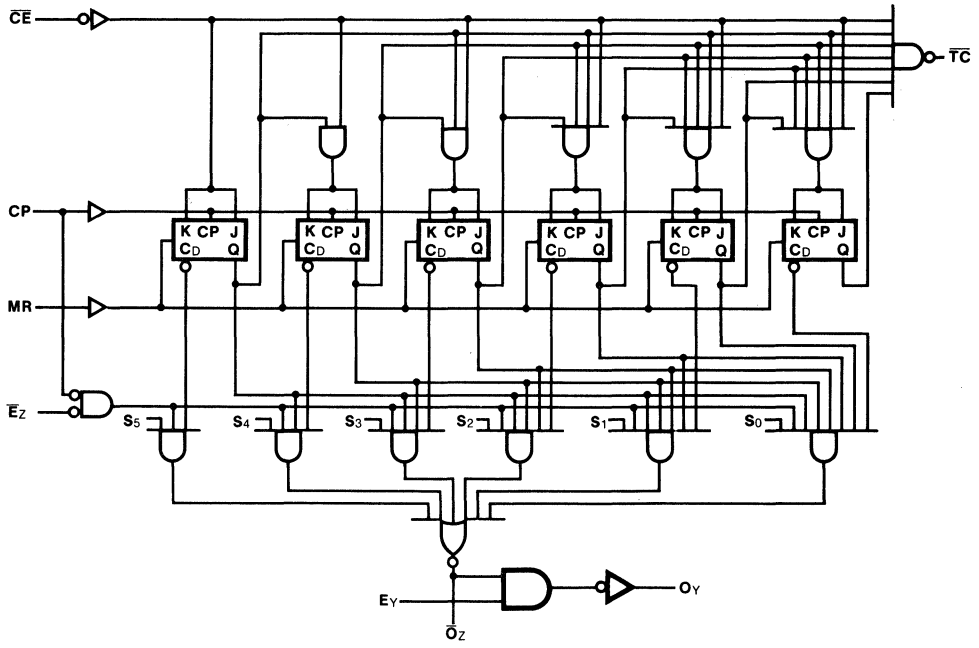


Fig. a. Cascading for 12-bit Rate Select

LOGIC DIAGRAM



MODE AND RATE SELECT TABLE (Note 1)

INPUTS									CLOCK PULSES	OUTPUTS				NOTES
MR	$\overline{CE}$	$\overline{E}_Z$	S_5	S_4	S_3	S_2	S_1	S_0		E_Y	O_Y	$\overline{O}_Z$	$\overline{TC}$	
H	X	H	X	X	X	X	X	X	X	H	L	H	H	2
L	L	L	L	L	L	L	L	L	64	H	L	H	1	3
L	L	L	L	L	L	L	L	H	64	H	1	1	1	3
L	L	L	L	L	L	L	H	L	64	H	2	2	1	3
L	L	L	L	L	L	H	L	L	64	H	4	4	1	3
L	L	L	L	L	H	L	L	L	64	H	8	8	1	3
L	L	L	L	H	L	L	L	L	64	H	16	16	1	3
L	L	L	H	L	L	L	L	L	64	H	32	32	1	3
L	L	L	H	H	H	H	H	H	64	H	63	63	1	3
L	L	L	H	H	H	H	H	H	64	L	H	63	1	4
L	L	L	H	L	H	L	L	L	64	H	40	40	1	5

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

NOTES:
1. Numerals indicate number of pulses per cycle.
2. This is a simplified illustration of the clear function. CP and $\overline{E}_Z$ also affect the logic level of O_Y and $\overline{O}_Z$. A LOW signal on E_Y will cause O_Y to remain HIGH.
3. Each rate illustrated assumes S_0 — S_5 are constant throughout the cycle; however, these illustrations in no way prohibit variable-rate operation.
4. E_Y is used to inhibit output Y.
5. $f_{out} = m \bullet \frac{f_{in}}{64} = \frac{(32 + 8)\, f_{in}}{64} = \frac{40\, f_{in}}{64} = 0.625\, f_{in}$

PULSE PATTERN TABLE

m	OUTPUT PULSE PATTERN AT $\overline{O}_Z$
1	11111111111111111111111111111101111111111111111111111111111111
2	11111111111111101111111111111111111111111111111101111111111111
3	11111111111111101111111111111101111111111111111011111111111111
4	11111110111111111111111011111111111111101111111111111011111111
5	11111110111111111111111011111110111111101111111111111011111111
6	11111110111111101111111011111111111111101111110111111101111111
8	11101111111011111110111111101111111011111110111111101111111101111
10	11101111111011101110111111101111111011111110111011101111111101111
12	11101110111011111110111011101111111011101110111111101110111101111
14	11101110111011101110111011101111111011101110111011101110111101111
16	10111011101110111011101110111011101110111011101110111011101110111
20	10111010101110111011101010111011101110101011101110111011101110111
24	10101011101010111010101110101011101010111010101110101011101010111
28	10101010101010111010101010101011101010101010101110101010101011
32	010101.... 0101

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
I_{OS}	Output Short Circuit Current	-18	-55	mA	V_{CC} = Max
I_{CC}	Power Supply Current		120	mA	V_{CC} = Max All Inputs = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	25		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_Z$ to $\overline{O}_Z$		18 23	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_Z$ to O_Y		30 33	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay E_Y to O_Y		14 10	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to O_Y		23 23	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{O}_Z$		14 14	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay CP to O_Y		39 30	ns	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_Z$		18 26	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$		30 33	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{TC}$		20 21	ns	Figs. 3-1, 3-5
t_{PLH}	Propagation Delay MR to O_Y		36	ns	Figs. 3-1, 3-16
t_{PHL}	Propagation Delay MR to $\overline{O}_Z$		23	ns	

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
t_s (L)	Setup Time LOW $\overline{CE}$ to CP Rising	25		ns	Fig. b
t_h (L)	Hold Time LOW $\overline{CE}$ to CP Rising	0	t_w CP -10	ns	
t_s (L)	Setup Time LOW $\overline{CE}$ to CP Falling	0	t_w CP -10	ns	Fig. c
t_h (L)	Hold Time LOW $\overline{CE}$ to CP Falling	20	T -10	ns	
t_{inh} (H)	Inhibit Time HIGH $\overline{CE}$ to CP Falling	10		ns	Fig. b
t_w (H)	CP Pulse Width HIGH	20		ns	Fig. 3-8
t_w (H)	MR Pulse Width HIGH	15		ns	Fig. 3-16

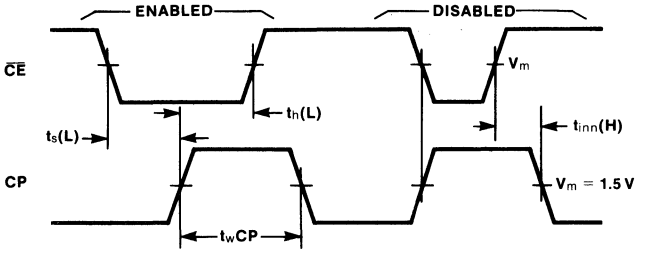


Fig. b

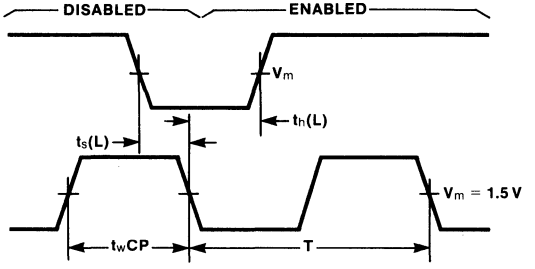


Fig. c

54H/74H101

JK EDGE-TRIGGERED FLIP-FLOP

(with AND-OR Inputs)

DESCRIPTION — The '101 is a high speed JK negative edge-triggered flip-flop. The AND-OR gate inputs are inhibited while the clock input is LOW. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic state of J and K inputs may be allowed to change when the clock pulse is in a HIGH state and the bistable will perform according to the Truth Table as long as minimum setup times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

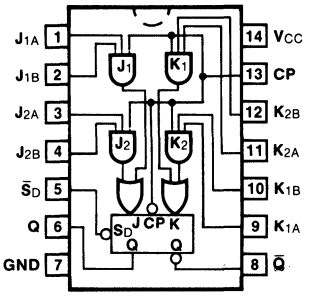
TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

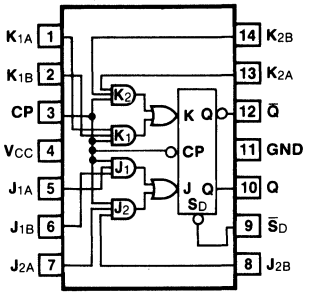
Asynchronous Input:
LOW input to $\overline{S}_D$ sets Q to HIGH level
Set is independent of clock

$J = (J_{1A} \bullet J_{1B}) + (J_{2A} \bullet J_{2B})$
$K = (K_{1A} \bullet K_{1B}) + (K_{2A} \bullet K_{2B})$
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

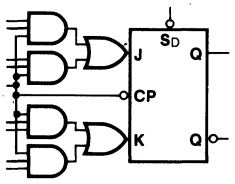
CONNECTION DIAGRAMS
PINOUT A



PINOUT B



LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

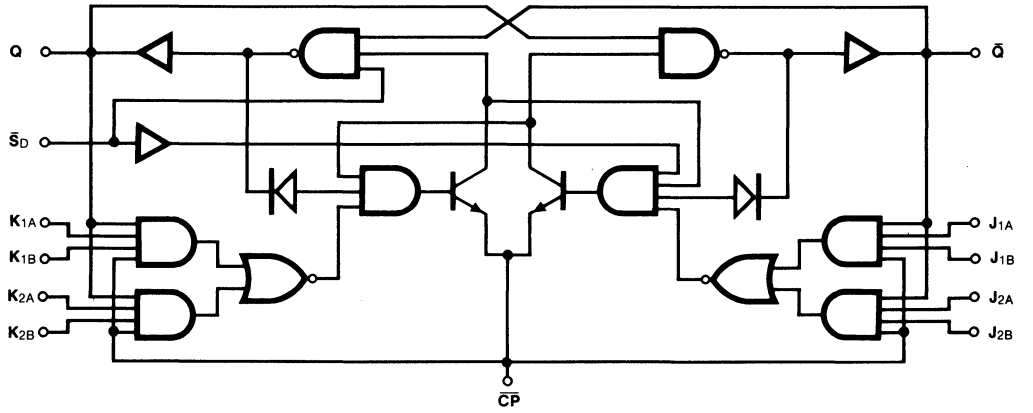
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74H101PC		9A
Ceramic DIP (D)	A	74H101DC	54H101DM	6A
Flatpak (F)	B	74H101FC	54H101FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74H (U.L.) HIGH/LOW
J_{1A}, J_{1B}, J_{2A}, J_{2B} K_{1A}, K_{1B}, K_{2A}, K_{2B}	Data Inputs	1.25/1.25
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	0*/3.0
$\overline{S}_D$	Direct Set Input (Active LOW)	2.5/1.25
Q, $\overline{Q}$	Outputs	12.5/12.5

*$\overline{CP}$ Sourcing Current, see DC Characteristics Table

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74H Min	54/74H Max	UNITS	CONDITIONS
I_{IH}	Input HIGH Current at $\overline{CP}$	0	-1.0	mA	V_{CC} = Max, V_{CP} = 2.4 V
I_{CC}	Power Supply Current		38	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74H C_L = 25 pF, R_L = 280 Ω Min	54/74H C_L = 25 pF, R_L = 280 Ω Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	40		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q or $\bar{Q}$		15 20	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\bar{S}_D$ to Q or $\bar{Q}$		12 20	ns	$V_{CP} \geq$ 2.0 V Figs. 3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay $\bar{S}_D$ to Q or $\bar{Q}$		12 35	ns	$V_{CP} \leq$ 0.8 V Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74H Min	54/74H Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time J_n or K_n to $\overline{CP}$	10 13		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time J_n or K_n to $\overline{CP}$	0 0		ns	
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width	10 15		ns	Fig. 3-9
t_w (L)	$\bar{S}_D$ Pulse Width LOW	16		ns	Fig. 3-10

54H/74H102

JK EDGE-TRIGGERED FLIP-FLOP

(With AND Inputs)

DESCRIPTION — The '102 is a high speed JK negative edge-triggered flip-flop. It features gated JK inputs and an asynchronous Clear input. The AND gate inputs are inhibited while the clock input is LOW. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic state of J and K inputs may be allowed to change when the clock pulse is in a HIGH state and the bistable will perform according to the Truth Table as long as minimum setup times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

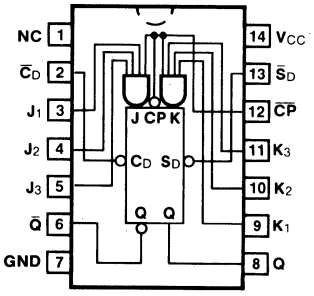
TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

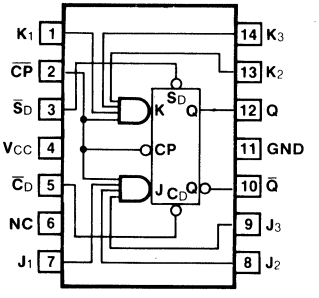
Asynchronous Inputs:
- LOW input to $\overline{S}_D$ sets Q to HIGH level
- LOW input to $\overline{C}_D$ sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

$J = (J_{1A} \bullet J_{1B}) + (J_{2A} \bullet J_{2B})$
$K = (K_{1A} \bullet K_{1B}) + (K_{2A} \bullet K_{2B})$
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

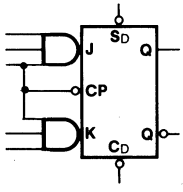
CONNECTION DIAGRAMS
PINOUT A



PINOUT B



LOGIC SYMBOL



V_{CC} = Pin 14 (4)
GND = Pin 7 (11)

ORDERING CODE: See Section 9

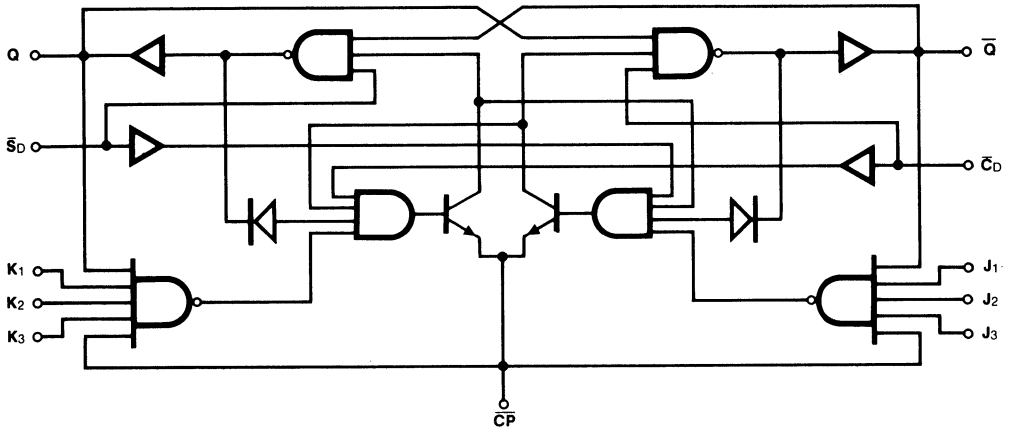
PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10% T_A = -55°C to +125°C	
Plastic DIP (P)	A	74H102PC		9A
Ceramic DIP (D)	A	74H102DC	54H102DM	6A
Flatpak (F)	B	74H102FC	54H102FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74H HIGH/LOW
J_1, J_2, J_3 } K_1, K_2, K_3 }	Data Inputs	1.25/1.25
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	0*/3.0
$\overline{C}_D$	Direct Clear Input (Active LOW)	2.5/1.25
$\overline{S}_D$	Direct Set Input (Active LOW)	2.5/1.25
Q, $\overline{Q}$	Outputs	12.5/12.5

*$\overline{CP}$ Sourcing Current, see DC Characteristics Table

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74H		UNITS	CONDITIONS
		Min	Max		
I_{IH}	Input HIGH Current at $\overline{CP}$	0	-1.0	mA	V_{CC} = Max, V_{CP} = 2.4 V
I_{CC}	Power Supply Current		38	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74H C_L = 25 pF, R_L = 280 Ω		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	40		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q or $\overline{Q}$		15 20	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_D$ or $\overline{S}_D$ to Q or $\overline{Q}$		12 20	ns	$V_{CP} \geq$ 2.0 V Figs. 3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_D$ or $\overline{S}_D$ to Q or $\overline{Q}$		12 35	ns	$V_{CP} \leq$ 0.8 V Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74H		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time J_n or K_n to $\overline{CP}$	10 13		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time J_n or K_n to $\overline{CP}$	0 0		ns	
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width	10 15		ns	Fig. 3-9
t_w (L)	$\overline{C}_D$ or $\overline{S}_D$ Pulse Width LOW	16		ns	Fig. 3-10

54H/74H103

DUAL JK EDGE-TRIGGERED FLIP-FLOP

(With Separate Clears and Clocks)

DESCRIPTION — The '103 is a high speed JK negative edge-triggered flip-flop. It features individual J, K, clock and asynchronous clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic state of J and K inputs may be allowed to change when the clock pulse is in a HIGH state and the bistable will perform according to the Truth Table as long as minimum setup times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

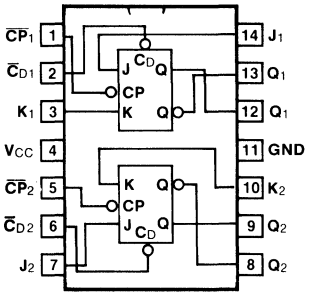
TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

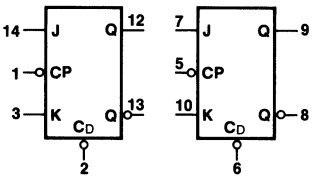
Asynchronous Input:
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear is independent of clock

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

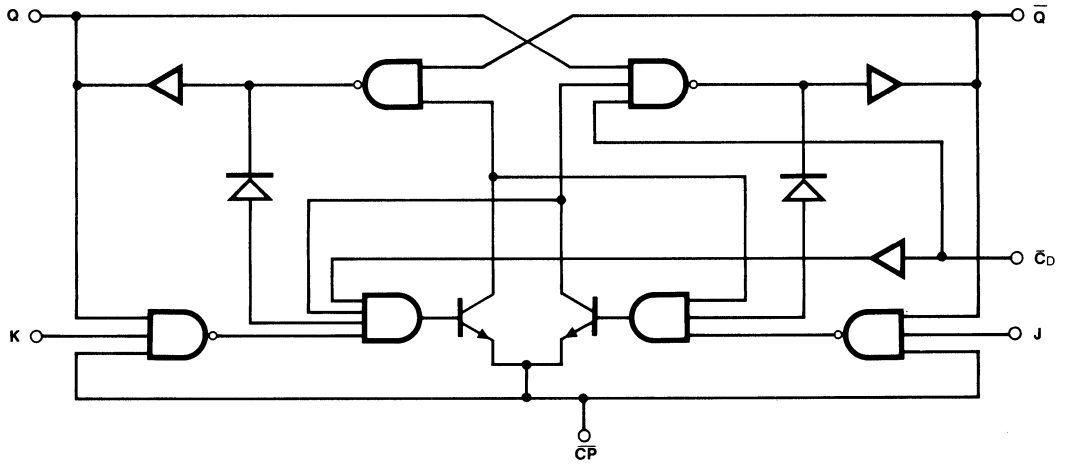
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74H103PC		9A
Ceramic DIP (D)	A	74H103DC	54H103DM	6A
Flatpak (F)	A	74H103FC	54H103FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74H (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	1.25/1.25
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	0*/3.0
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	2.5/1.25
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	12.5/12.5

*$\overline{CP}$ Sourcing Current, see DC Characteristics Table

LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74H Min	54/74H Max	UNITS	CONDITIONS
I_{IH}	Input HIGH Current at $\overline{CP}$	0	-1.0	mA	V_{CC} = Max, V_{CP} = 2.4 V
I_{CC}	Power Supply Current		76	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74H C_L = 25 pF R_L = 280 Ω Min	54/74H C_L = 25 pF R_L = 280 Ω Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	40		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$		15 20	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ to Q_n or $\overline{Q}_n$		12 20	ns	$V_{CP} \geq$ 2.0 V Figs. 3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ to Q_n or $\overline{Q}_n$		12 35	ns	$V_{CP} \leq$ 0.8 V Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74H Min	54/74H Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time J_n or K_n to $\overline{CP}_n$	10 13		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time J_n or K_n to $\overline{CP}_n$	0 0		ns	
t_w (H) t_w (L)	$\overline{CP}_n$ Pulse Width	10 15		ns	Fig. 3-9
t_w (L)	$\overline{C}_{Dn}$ Pulse Width LOW	16		ns	Fig. 3-10

54H/74H106

DUAL JK EDGE-TRIGGERED FLIP-FLOP

(With Separate Sets, Clear and Clocks)

DESCRIPTION — The '106 is a high speed JK negative edge-triggered flip-flop. It features individual J, K, clock and asynchronous set and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic state of J and K inputs may be allowed to change when the clock pulse is in a HIGH state and the bistable will perform according to the Truth Table as long as minimum setup times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

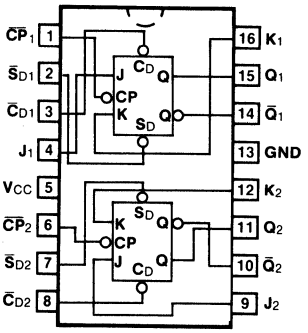
TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

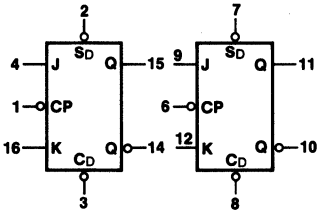
Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 13

ORDERING CODE: See Section 9

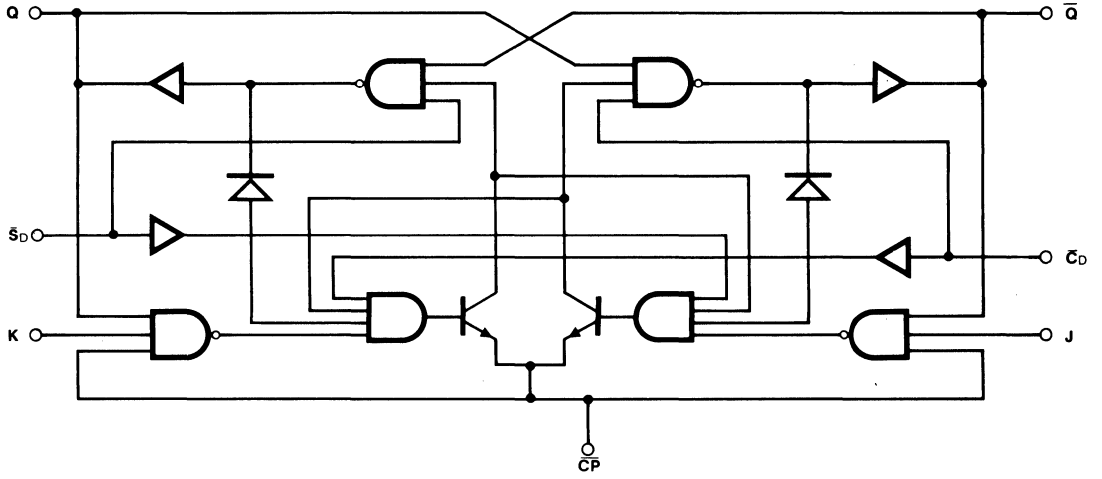
PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74H106PC		9B
Ceramic DIP (D)	A	74H106DC	54H106DM	6B
Flatpak (F)	A	74H106FC	54H106FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74H (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	1.25/1.25
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	0*/3.0
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	2.5/1.25
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	2.5/1.25
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	12.5/12.5

*$\overline{CP}$ Sourcing Current, see DC Characteristics Table

LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74H Min	54/74H Max	UNITS	CONDITIONS
I_{IH}	Input HIGH Current at $\overline{CP}_n$	0	-1.0	mA	V_{CC} = Max, V_{CP} = 2.4 V
I_{CC}	Power Supply Current		76	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74H C_L = 25 pF, R_L = 280 Ω Min	54/74H C_L = 25 pF, R_L = 280 Ω Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	40		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$		15 20	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		12 20	ns	$V_{CP} \geq$ 2.0 V Figs. 3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		12 35	ns	$V_{CP} \leq$ 0.8 V Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74H Min	54/74H Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time J_n or K_n to $\overline{CP}_n$	10 13		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time J_n or K_n to $\overline{CP}_n$	0 0		ns	
t_w (H) t_w (L)	$\overline{CP}_n$ Pulse Width	10 15		ns	Fig. 3-9
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	16		ns	Fig. 3-10

54/74107
54LS/74LS107

DUAL JK FLIP-FLOP
(With Separate Clears and Clocks)

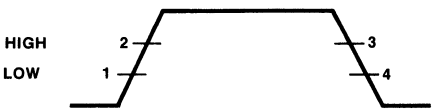
DESCRIPTION — The '107 dual JK master/slave flip-flops have a separate clock for each flip-flop. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) isolate slave from master; 2) enter information from J and K inputs to master; 3) disable J and K inputs; 4) transfer information from master to slave.

TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORM



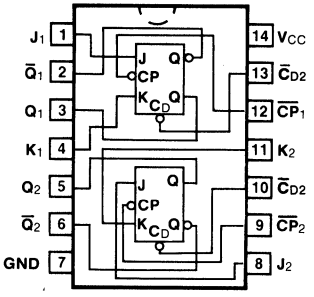
Asynchronous Input:
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear is independent of clock

The 'LS107 offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock is HIGH and the bistable will perform according to the Truth Table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

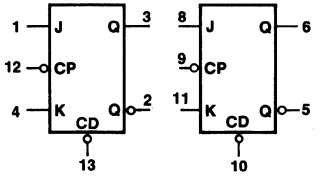
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +125°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74107PC, 74LS107PC		9A
Ceramic DIP (D)	A	74107DC, 74LS107DC	54107DM, 54LS107DM	6A
Flatpak (F)	A	74107FC, 74LS107FC	54107FM, 54LS107FM	3I

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL

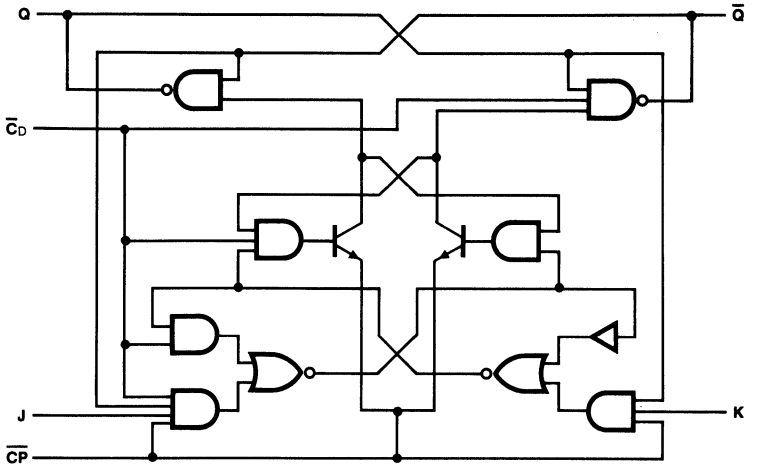


V_{CC} = Pin 14
GND = Pin 7

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	1.0/1.0	0.5/0.25
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	2.0/2.0	2.0/0.5
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	2.0/2.0	1.5/0.5
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	20/10	10/5.0 (2.5)

LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current		40		8.0	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	15		30		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$		25 40		20 30	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ to Q_n or $\overline{Q}_n$		25 40		20 30	ns	Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H)	Setup Time HIGH J_n or K_n to $\overline{CP}_n$	0		20		ns	Fig. 3-18 ('107) Fig. 3-7 ('LS107)
t_h (H)	Hold Time HIGH J_n or K_n to $\overline{CP}_n$	0		0		ns	
t_s (L)	Setup Time LOW J_n or K_n to $\overline{CP}_n$	0		20		ns	
t_h (L)	Hold Time LOW J_n or K_n to $\overline{CP}_n$	0		0		ns	
t_w (H) t_w (L)	$\overline{CP}_n$ Pulse Width	20 47		13.5 20		ns	Fig. 3-9
t_w (L)	$\overline{C}_{Dn}$ Pulse Width LOW	25		25		ns	Fig. 3-10

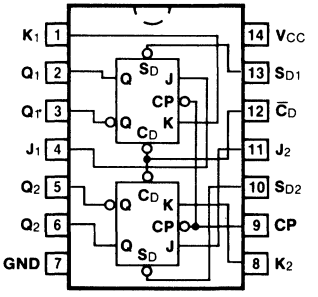
54H/74H108

DUAL JK EDGE-TRIGGERED FLIP-FLOP

(With Separate Sets, A Common Clear and Clock)

DESCRIPTION — The '108 is a high speed JK negative edge-triggered flip-flop. It features individual J, K, and asynchronous Set inputs to each flip-flop as well as common clock and asynchronous Clear inputs. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic state of J and K inputs may be allowed to change when the clock pulse is in a HIGH state and the bistable will perform according to the Truth Table as long as minimum setup times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

CONNECTION DIAGRAM
PINOUT A



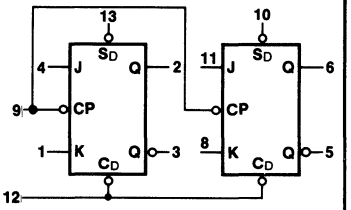
TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

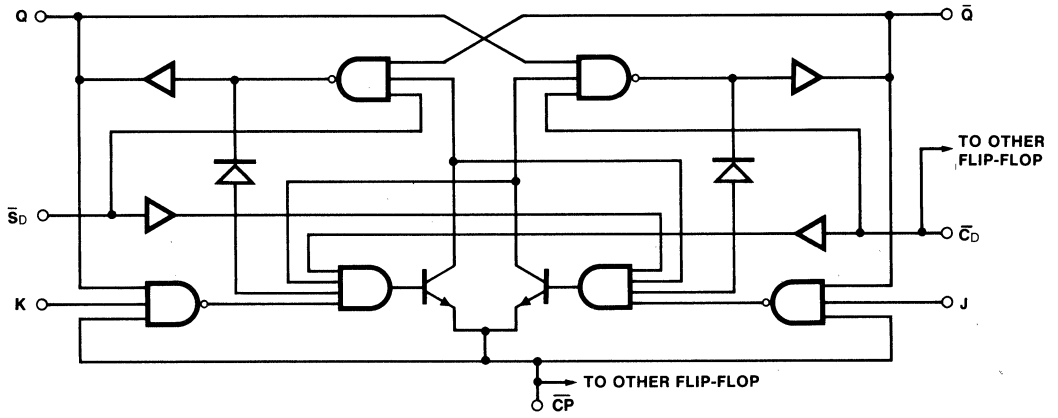
PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74H108PC		9A
Ceramic DIP (D)	A	74H108DC	54H108DM	6A
Flatpak (F)	A	74H108FC	54H108FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74H (U.L.) HIGH/LOW
J_1, J_2, K_1,K_2	Data Inputs	1.25/1.25
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	0*/6.0
$\overline{C}_D$	Direct Clear Input (Active LOW)	5.0/2.5
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	2.5/1.25
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	12.5/12.5

*$\overline{CP}$ Sourcing Current, see DC Characteristics Table

LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74H		UNITS	CONDITIONS
		Min	Max		
I_{IH}	Input HIGH Current at $\overline{CP}$	0	-1.0	mA	V_{CC} = Max, V_{CP} = 2.4 V
I_{CC}	Power Supply Current		76	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74H C_L = 25 pF R_L = 280 Ω		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	40		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_n or $\overline{Q}_n$		15 20	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_D$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		12 20	ns	V_{CP} = ≥ 2.0 V Figs. 3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_D$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		12 35	ns	V_{CP} = ≤ 0.8 V Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74H		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time J_n or K_n to $\overline{CP}$	10 13		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time J_n or K_n to $\overline{CP}$	0 0		ns	
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width	10 15		ns	Fig. 3-9
t_w (L)	$\overline{C}_D$ or $\overline{S}_{Dn}$ Pulse Width LOW	16		ns	Fig. 3-10

54S/74S109
54LS/74LS109

DUAL JK POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The '109 consists of two high speed, completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D flip-flop (refer to '74 data sheet) by connecting the J and $\overline{K}$ inputs together. The '109 is functionally equivalent to the 9024.

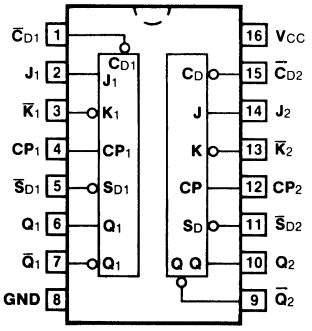
TRUTH TABLE

INPUTS		OUTPUTS
@ t_n		@ t_{n+1}
J	K	Q Q
L	H	No Change
L	L	L H
H	H	H L
H	L	Toggles

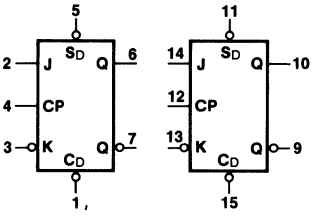
Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

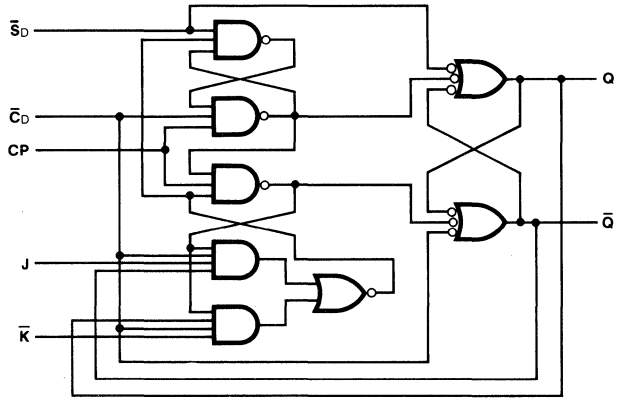
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE: V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S109PC, 74LS109PC		9A
Ceramic DIP (D)	A	74S109DC, 74LS109DC	54S109DM, 54LS109DM	6A
Flatpak (F)	A	74S109FC, 74LS109FC	54S109FM, 54LS109FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J_1, J_2, $\overline{K}_1$, $\overline{K}_2$	Data Inputs	1.25/1.25	0.5/0.25
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	2.5/2.5	1.0/0.5
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	5.0/5.0	1.0/1.0
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	2.5/2.5	1.0/0.5
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	25/12.5	10/5.0 (2.5)

LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		52		8.0	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF, R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	75		30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$		9.0 11		25 35	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		6.0 12		15 35	ns	$V_{CP} \geq 2.0$ V Figs. 3-1, 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		6.0 12		15 24	ns	$V_{CP} \leq 0.8$ V Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

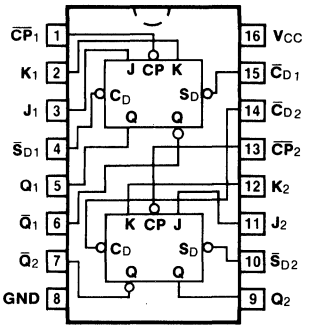
SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time J_n or $\overline{K}_n$ to CP_n	6.0 6.0		18 18		ns	Fig.3-6
t_h (H) t_h (L)	Hold Time J_n or $\overline{K}_n$ to CP_n	0 0		0 0		ns	
t_w (H) t_w (L)	CP_n Pulse Width	7.0 6.5		20 13.5		ns	Fig. 3-8
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	6.0		15		ns	Fig. 3-10

54S/74S112
54LS/74LS112

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The '112 features individual J, K, Clock and asynchronous Set and Clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may change when the clock is HIGH and the bistable will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

CONNECTION DIAGRAM
PINOUT A



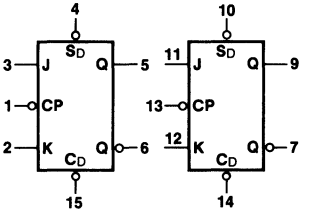
TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

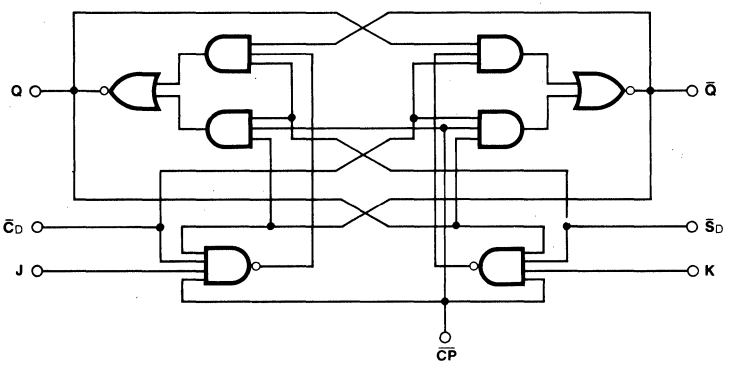
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S112PC, 74LS112PC		9B
Ceramic DIP (D)	A	74S112DC, 74LS112DC	54S112DM, 54LS112DM	6B
Flatpak (F)	A	74S112FC, 74LS112FC	54S112FM, 54LS112FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	1.25/1.0	0.5/0.25
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	2.5/2.5	2.0/0.5
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	2.5/4.375	1.5/0.5
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	2.5/4.375	1.5/0.5
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	25/12.5	10/5.0 (2.5)

LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		50		8.0	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF, R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	80		30		MHz	Figs. 3-1, 3-9
t_{PLH}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$		7.0		16	ns	Figs. 3-1, 3-9
t_{PHL}			7.0		24		
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		7.0		16	ns	Figs. 3-1, 3-10
t_{PHL}			7.0		24		

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H)	Setup Time J_n or K_n to $\overline{CP}_n$	7.0		20		ns	Fig. 3-7
t_s (L)		7.0		15			
t_h (H)	Hold Time J_n or K_n to $\overline{CP}_n$	0		0		ns	
t_h (L)		0		0			
t_w (H)	$\overline{CP}_n$ Pulse Width	6.0		20		ns	Fig. 3-9
t_w (L)		6.5		15			
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	8.0		15		ns	Fig. 3-10

54S/74S113
54LS/74LS113
DUAL JK EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The '113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

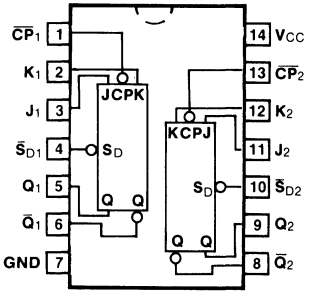
TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

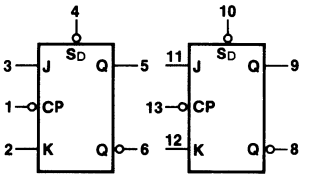
Asynchronous Input:
LOW input to $\overline{S}_D$ sets Q to HIGH level
Set is independent of clock

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

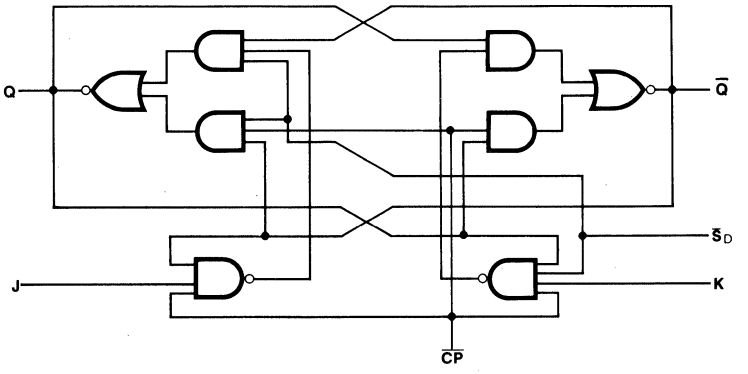
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74S113PC, 74LS113PC		9A
Ceramic DIP (D)	A	74S113DC, 74LS113DC	54S113DM, 54LS113DM	6A
Flatpak (F)	A	74S113FC, 74LS113FC	54S113FM, 54LS113FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	1.25/1.0	0.5/0.25
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	2.5/2.5	2.0/0.5
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	2.5/4.375	1.5/0.5
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	25/12.5	10/5.0 (2.5)

LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		50		8.0	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF, R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	80		30		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$		7.0 7.0		16 24	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		7.0 7.0		16 24	ns	Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time J_n or K_n to $\overline{CP}_n$	7.0 7.0		20 15		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time J_n or K_n to $\overline{CP}_n$	0 0		0 0		ns	
t_w (H) t_w (L)	$\overline{CP}_n$ Pulse Width	6.0 6.5		20 15		ns	Fig. 3-9
t_w (L)	$\overline{S}_{Dn}$ Pulse Width LOW	8.0		15		ns	Fig. 3-10

54S/74S114
54LS/74LS114

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

(With Common Clocks and Clears)

DESCRIPTION — The '114 features individual J, K and set inputs and common clock and common clear inputs. When the clock goes HIGH the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the Clock Pulse is HIGH and the bistable will perform according to the truth table as long as the minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

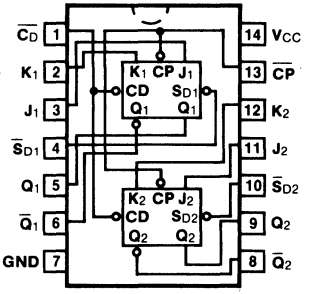
TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

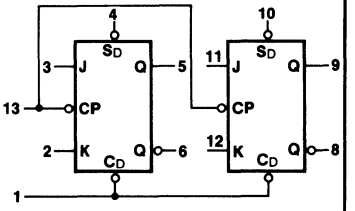
Asynchronous Inputs:
- LOW input to $\overline{S}_D$ sets Q to HIGH level
- LOW input to $\overline{C}_D$ sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

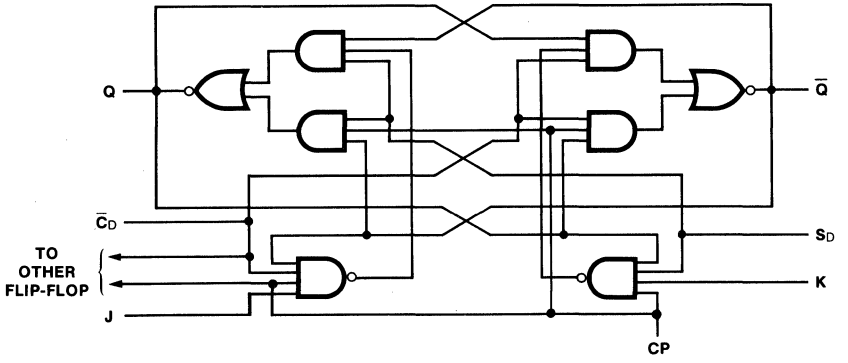
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE: V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S114PC, 74LS114PC		9A
Ceramic DIP (D)	A	74S114DC, 74LS114DC	54S114DM, 54LS114DM	6A
Flatpak (F)	A	74S114FC, 74LS114FC	54S114FM, 54LS114FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	1.25/1.0	0.5/0.25
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	5.0/5.0	2.0/0.5
$\overline{C}_D$	Direct Clear Input (Active LOW)	5.0/8.75	1.5/0.5
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	2.5/4.375	1.5/0.5
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	25/12.5	10/5.0 (2.5)

LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		50		8.0	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF, R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	80		30		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q or $\overline{Q}$		7.0 7.0		16 24	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_D$ or $\overline{S}_{Dn}$ to Q or $\overline{Q}$		7.0 7.0		16 24	ns	Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_C = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time J_n or K_n to $\overline{CP}$	7.0 7.0		20 15		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time J_n or K_n to $\overline{CP}$	0 0		0 0		ns	Fig. 3-7
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width	6.0 6.5		20 15		ns	Fig. 3-9
t_w	$\overline{C}_D$ or $\overline{S}_{Dn}$ Pulse Width	8.0		15		ns	Fig. 3-10

54/74121

MONOSTABLE MULTIVIBRATOR

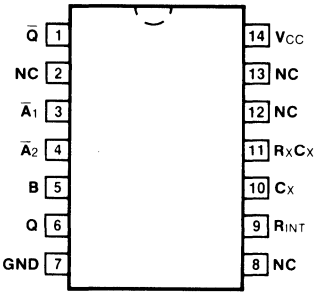
DESCRIPTION — The '121 features positive and negative dc level triggering inputs and complementary outputs. Input pin 5 directly activates a Schmitt circuit which provides temperature compensated level detection, increases immunity to positive-going noise and assures jitter-free response to slowly rising triggers.

When triggering occurs, internal feedback latches the circuit, prevents re-triggering while the output pulse is in progress and increases immunity to negative-going noise. Noise immunity is typically 1.2 V at the inputs and 1.5 V on V_{CC}.

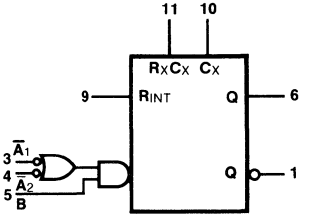
Output pulse width stability is primarily a function of the external R_x and C_x chosen for the application. A 2 kΩ internal resistor is provided for optional use where output pulse width stability requirements are less stringent. Maximum duty cycle capability ranges from 67% with a 2 kΩ resistor to 90% with a 40 kΩ resistor. Duty cycles beyond this range tend to reduce the output pulse width. Otherwise, output pulse width follows the relationship:

$$t_w = 0.69\ R_X C_X$$

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 2,8,12,13

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74121PC		9A
Ceramic DIP (D)	A	74121DC	54121DM	6A
Flatpak (F)	A	74121FC	54121FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L.definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\bar{A}_1$, $\bar{A}_2$	Trigger Inputs (Active Falling Edge)	1.0/1.0
B	Schmitt Trigger Input (Active Rising Edge)	2.0/2.0
Q, $\bar{Q}$	Outputs	20/10

TRIGGERING TRUTH TABLE

INPUTS $\bar{A}_1$	INPUTS $\bar{A}_2$	INPUTS B	RESPONSE
H	H	↓	No Trigger
L	X	↓	Trigger
X	L	↓	Trigger
↑	L	X	No Trigger
↑	X	L	No Trigger
↑	H	H	Trigger
L	↑	X	No Trigger
X	↑	L	No Trigger
H	↑	H	Trigger

NOTE:
Triggering occurs only when the $\bar{Q}$ output is HIGH (not in timing cycle) and one of the above triggering situations is satisfied.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
V_{T+}	Positive-going Threshold Voltage at $\bar{A}_n$ or B Inputs			2.0	V	V_{CC} = Min
V_{T-}	Negative-going Threshold Voltage at $\bar{A}_n$ or B Inputs		0.8		V	V_{CC} = Min
I_{OS}	Output Short Circuit Current	XM	-20	-55	mA	V_{CC} = Max
		XC	-18	-55		
I_{CC}	Power Supply Current	Quiescent State		25	mA	V_{CC} = Max
		Fired State		40		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF Min	54/74 C_L = 15 pF Max	UNITS	CONDITIONS	
t_{PLH}	Propagation Delay B to Q	15	55	ns	C_X = 80 pF Fig. 3-1, Fig. a	
t_{PLH}	Propagation Delay $\bar{A}_n$ to Q	25	70	ns		
t_{PHL}	Propagation Delay B to $\bar{Q}$	20	65	ns		
t_{PHL}	Propagation Delay $\bar{A}_n$ to $\bar{Q}$	30	80	ns		
t_W	Pulse Width Using Internal Timing Resistor	70	150	ns	C_X = 80 pF	R_X = Open Fig. 3-1
t_W	Pulse Width with Zero Timing Capacitance	20	50	ns	C_X = 0 pF	Fig. a Pin 9 = V_{CC}
t_W	Pulse Width Using External Timing Resistor	600	800	ns	C_X = 100 pF	R_X = 10 kΩ Pin 9 = Open
		6.0	8.0	ms	C_X = 1.0 μF	Fig. 3-1, a
t_{HOLD}	Minimum Duration of Trigger Pulse		50	ns	C_X = 80 pF, R_X = Open Pin 9 = V_{CC}, Fig. a	

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYBMOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
V_{r-f}	Input Pulse Rise/Fall Slew Rate	@ A_n		1.0	V/μs	
		@ B		1.0	V/s	
Rx	External Timing Resistor	XC	1.4	40	kΩ	
		XM	1.4	30		
Cx	External Timing Capacitor		0	1000	μF	
t_w	Output Pulse Width			40	sec	Fig. a
	Duty Cycle	XM,XC		67	%	Rx = 2 kΩ
		XM		90		Rx = 30 kΩ
		XC		90		Rx = 40 kΩ

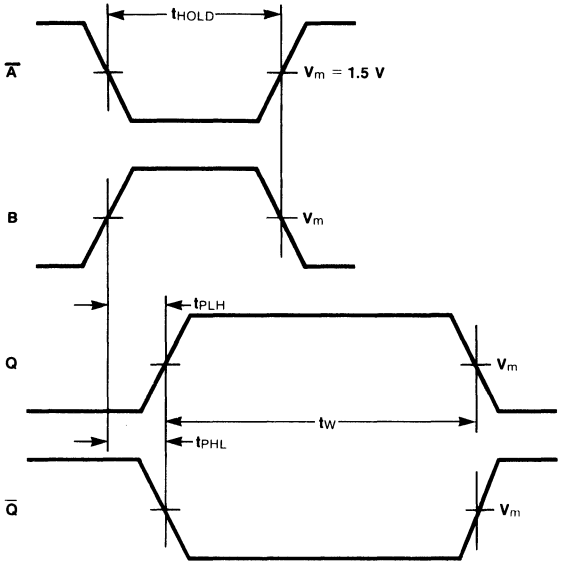


Fig. a

TYPICAL CHARACTERISTICS

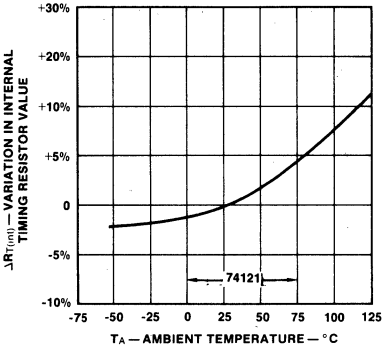


Fig. b Variation in Internal Timing Resistor Value Versus Ambient Temperaure

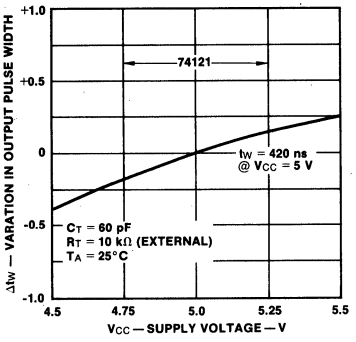


Fig. c Variation in Output Pulse Width Versus Supply Voltage

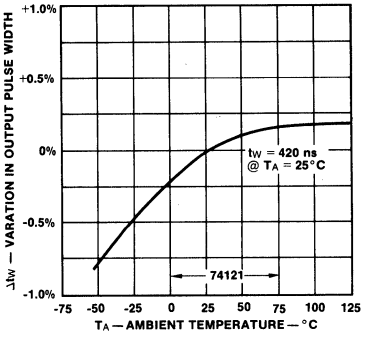


Fig. d Variation in Output Pulse Width Versus Ambient Temperature

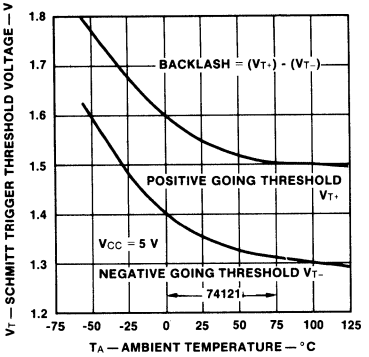


Fig. e Schmitt Trigger Threshold Voltage Versus Ambient Temperature

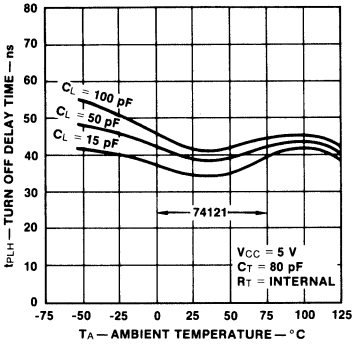


Fig. f Propagation Delay Time B Input to Q Output Versus Ambient Temperature

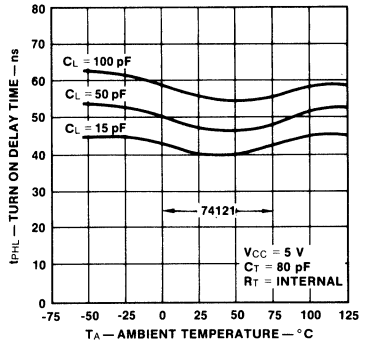


Fig. g Propagation Delay Time B Input to $\overline{Q}$ Output Versus Ambient Temperature

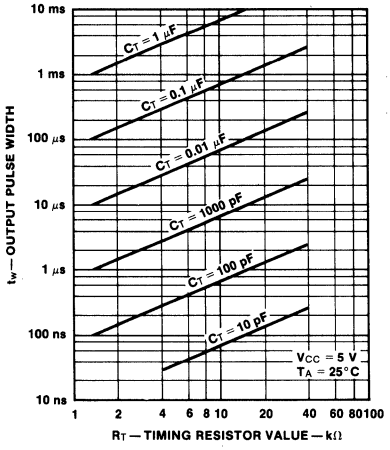


Fig. h Output Pulse Width Versus Timing Resistor Value

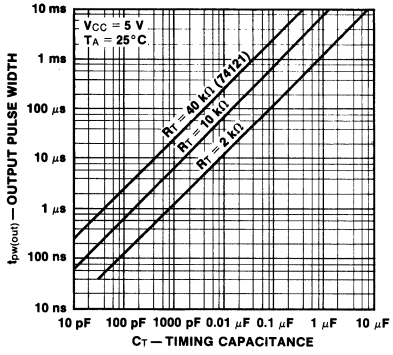
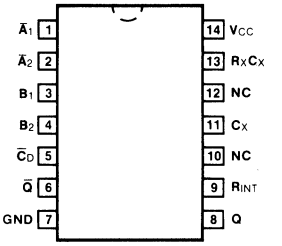


Fig. i Output Pulse Width Versus External Capacitance

54/74122

RETRIGGERABLE RESETTABLE MULTIVIBRATOR

CONNECTION DIAGRAM
PINOUT A

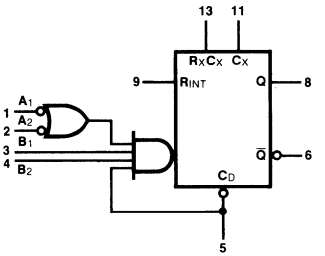


DESCRIPTION — The '122 features positive and negative dc level triggering inputs, complementary outputs, an optional 10 kΩ internal timing resistor and an overiding Direct Clear ($\overline{C}_D$) input. When the circuit is in the quasi-stable (delay) state, another trigger applied to the inputs (per Truth Table) will cause the delay period to start again, without disturbing the outputs. This process can be repeated indefinitely and thus the output pulse period (Q HIGH, $\overline{Q}$ LOW) can be made as long as desired. Alternatively, a delay period can be terminated by a LOW signal applied to $\overline{C}_D$, which also prevents triggering. An internal connection from $\overline{C}_D$ to the input gate makes it possible to trigger the circuit by a positive-going signal on $\overline{C}_D$, as shown in the Truth Table. For timing capacitor values greater than 1000 pF, the output pulse width is defined as follows:

$$t_w = 0.32\ R_X C_X\ (1.0 + 0.7/R_X)$$

Where t_w is in ns, R_X is in kΩ and C_X is in pF.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 10, and 12

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V, ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74122PC		9A
Ceramic DIP (D)	A	74122DC	54122DM	6A
Flatpak (F)	A	74122FC	54122FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

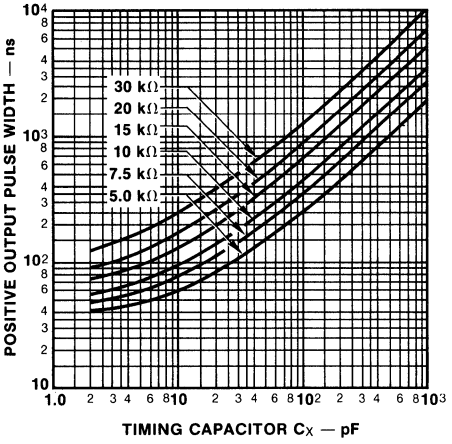
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\overline{A}_1$, $\overline{A}_2$	Trigger Inputs (Active Falling Edge)	1.0/1.0
B_1, B_2	Trigger Inputs (Active Rising Edge)	1.0/1.0
$\overline{C}_D$	Direct Clear Inputs (Active LOW)	2.0/2.0
Q, $\overline{Q}$	Outputs	20/10

TRIGGERING TRUTH TABLE

INPUTS*					RESPONSE
$\overline{C}_D$	$\overline{A}_1$	$\overline{A}_2$	B_1	B_2	
L	X	X	X	X	No Trigger
X	↘	L	X	X	No Trigger
X	↘	X	L	X	No Trigger
H	↘	H	H	H	Trigger
X	X	X	↗	L	No Trigger
X	H	H	↗	X	No Trigger
H	L	X	↗	H	Trigger
↗	L	X	H	H	Trigger

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
*Input pins 1 and 2 are logically interchangeable, as are input pins 3 and 4.

PULSE WIDTH vs R_X AND C_X



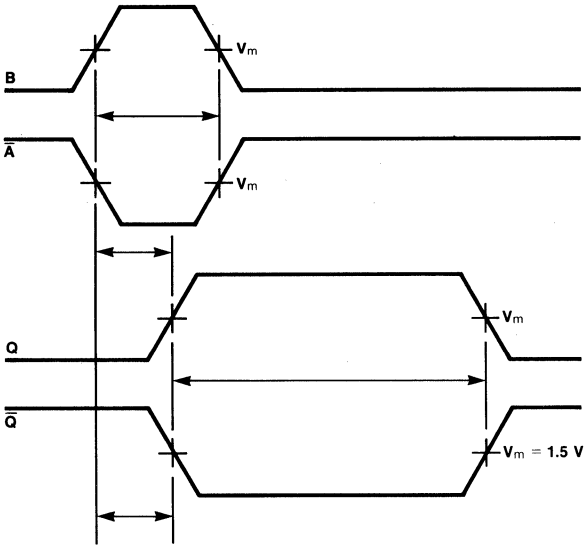


Fig. a

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	-10	-40	mA	V_{CC} = Max
I_{CC}	Power Supply Current		28	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω Min	54/74 C_L = 15 pF R_L = 400 Ω Max	UNITS	CONDITIONS
t_{PLH}	Propagation Delay B to Q		28	ns	C_X = 0 pF, R_X = 5 kΩ Fig. 3-1, Fig. a
t_{PLH}	Propagation Delay $\overline{A}_n$ to Q		33	ns	
t_{PHL}	Propagation Delay B to $\overline{Q}$		36	ns	
t_{PHL}	Propagation Delay $\overline{A}_n$ to $\overline{Q}$		40	ns	
t_{PLH}	Propagation Delay $\overline{C}_D$ to $\overline{Q}$		40	ns	C_X = 0 pF, R_X = 5 kΩ Figs. 3-1, 3-10
t_{PHL}	Propagation Delay $\overline{C}_D$ to Q		27	ns	
$t_{w(out)}$	Pulse Width at Q with Zero Timing Capacitor		65	ns	C_X = 0 pF, R_X = 5 kΩ Fig. 3-1, Fig. a
$t_{w(out)}$	Pulse Width with External Timing Components	3.08	3.76	μs	C_X = 1000 pF, R_X = 10 kΩ Figs. 3-1, Fig. a

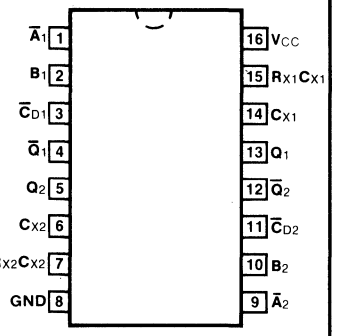
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
t_w	Trigger Pulse Width		40		ns	Over Operating V_{CC} and Temperature Range
R_X	External Timing Resistor	XC	5.0	50	kΩ	
		XM	5.0	25		
C_X	External Timing Capacitor		No Restrictions		pF	

54/74123

DUAL RETRIGGERABLE RESETTABLE MULTIVIBRATOR

CONNECTION DIAGRAM
PINOUT A

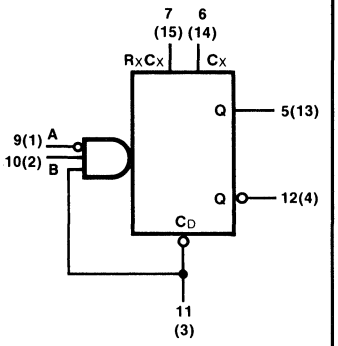


DESCRIPTION — Each half of the '123 features retriggerable capability, complementary dc level triggering and overriding Direct Clear. When a circuit is in the quasi-stable (delay) state, another trigger applied to the inputs (per the Truth Table) will cause the delay period to start again, without disturbing the outputs. By repeating this process, the output pulse period (Q HIGH, $\overline{Q}$ LOW) can be made as long as desired. Alternatively, a delay period can be terminated at any time by a LOW signal on $\overline{C}_D$, which also inhibits triggering. An internal connection from $\overline{C}_D$ to the input gate makes it possible to trigger the circuit by a positive-going signal on $\overline{C}_D$, as shown in the Truth Table. For timing capacitor values greater than 1000 pF, the output pulse width is defined as follows.

$$t_w = 0.28\ R_X C_X\ (1.0 + 0.7/R_X)$$

Where t_w is in ns, R_X is in kΩ and C_X is in pF.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74123PC		9B
Ceramic DIP (D)	A	74123DC	54123DM	6B
Flatpak (F)	A	74123FC	54123FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

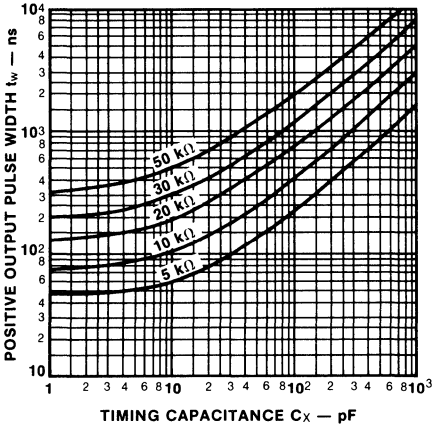
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\overline{A}_1$, $\overline{A}_2$	Trigger Inputs (Active Falling Edge)	1.0/1.0
B_1, B_2	Trigger Inputs (Active Rising Edge)	1.0/1.0
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	2.0/2.0
Q_1, Q_2	Positive Pulse Output	20/10
$\overline{Q}_1$, $\overline{Q}_2$	Negative Pulse Output	20/10

TRIGGERING TRUTH TABLE

INPUTS			RESPONSE
A	B	$\overline{C}_D$	
X	X	L	No Trigger
↘	L	X	No Trigger
↘	H	H	Trigger
H	↗	X	No Trigger
L	↗	H	Trigger
L	H	↗	Trigger

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

PULSE WIDTH vs R_X AND C_X



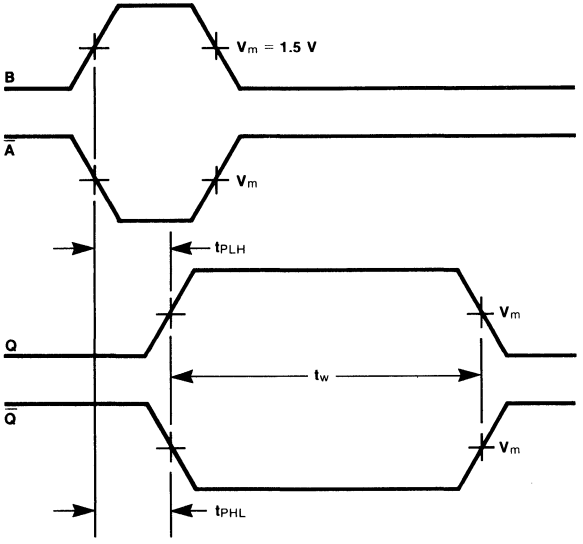


Fig. a.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	-10	-40	mA	V_{CC} = Max
I_{CC}	Power Supply Current		66	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω Min	54/74 C_L = 15 pF R_L = 400 Ω Max	UNITS	CONDITIONS
t_{PLH}	Propagation Delay B to Q		28	ns	C_X = 0 pF, R_X = 5 kΩ Fig. 3-1, Fig. a
t_{PLH}	Propagation Delay $\overline{A}$ to Q		33	ns	
t_{PHL}	Propagation Delay B to $\overline{Q}$		36	ns	
t_{PHL}	Propagation Delay $\overline{A}$ to $\overline{Q}$		40	ns	
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ to $\overline{Q}$		40	ns	C_X = 0 pF, R_X = 5 kΩ Figs. 3-1, 3-10
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ to Q		27	ns	
$t_{w(min)}$	Pulse Width with Zero Timing Capacitor		65	ns	C_X = 0 pF, R_X = 5 kΩ Fig. 3-1, Fig. a
t_w	Pulse Width with External Timing Components	2.76	3.37	μs	C_X = 1000 pF, R_X = 10 kΩ Fig. 3-1, Fig. a

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
t_w	Trigger Pulse Width		40		ns	Over Operating Temperature Range
R_X	External Timing Resistor	XC	5.0	50	kΩ	
		XM	5.0	25		
C_X	External Timing Capacitor		No Restrictions		pF	

54/74125
54LS/74LS125A

QUAD BUS BUFFER GATE

(With 3-State Outputs)

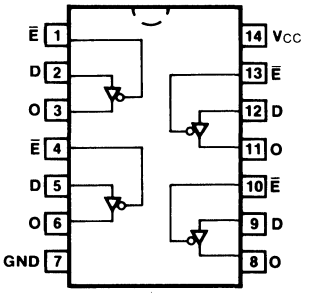
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74125PC, 74LS125APC		9A
Ceramic DIP (D)	A	74125DC, 74LS125ADC	54125DM, 54LS125ADM	6A
Flatpak (F)	A	74125FC, 74LS125AFC	54125FM, 54LS125AFM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	130/10	65/15
	(50)	(25)/(7.5)

CONNECTION DIAGRAM
PINOUT A



TRUTH TABLE

INPUTS Ē	INPUTS D	OUTPUT
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

DC AND AC CHARACTERISTICS: See Seciton 3*

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	XM	2.4				V	I_{OH} = -2.0 mA; V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}
		XC	2.4					I_{OH} = -5.2 mA
		XM			2.4			I_{OH} = -1.0 mA
		XC			2.4			I_{OH} = -2.6 mA
I_{OS}	Output Short Circuit Current	XM	-30	-70	-30	-130	mA	V_{CC} = Max
		XC	-28	-70	-30	-130		
I_{CC}	Power Supply Current			54		20	mA	Outputs OFF, V_{IN} = Gnd, V_E = 4.5 V, V_{CC} = Max
t_{PLH} t_{PHL}	Propagation Delay Data to Output			13 18		15 18	ns	Figs. 3-3, 3-5
t_{PZH} t_{PZL}	Output Enable Time			17 25		16 25	ns	Figs. 3-3, 3-11, 3-12
t_{PLZ} t_{PHZ}	Output Disable Time			8.0 12		25 25	ns	Figs. 3-3, 3-11, 3-12

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54/74126
54LS/74LS126
QUAD BUS BUFFER GATE
(With 3-State Outputs)

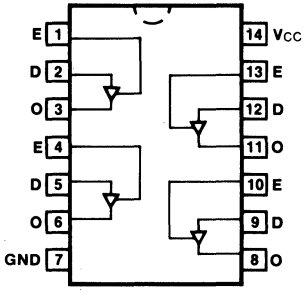
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74126PC, 74LS126PC		9A
Ceramic DIP (D)	A	74126DC, 74LS126DC	54126DM, 54LS126DM	6A
Flatpak (F)	A	74126FC, 74LS126FC	54126FM, 54LS126FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	130/10	65/15
	(50)	(25)/(7.5)

CONNECTION DIAGRAM
PINOUT A



TRUTH TABLE

INPUTS E	INPUTS D	OUTPUT
H	L	L
H	H	H
L	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	XM	2.4				V	I_{OH} = -2.0 mA	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}
		XC	2.4					I_{OH} = -5.2 mA	
		XM			2.4			I_{OH} = -1.0 mA	
		XC			2.4			I_{OH} = -2.6 mA	
I_{OS}	Output Short Circuit Current	XM	-30	-70	-30	-130	mA	V_{CC} = Max	
		XC	-28	-70	-30	-130			
I_{CC}	Power Supply Current			62		24 20	mA	Outputs LOW, V_E = 4.5 V	V_{CC} = Max
								Outputs OFF, V_E = 0 V	V_{IN} = Gnd
t_{PLH} t_{PHL}	Propagation Delay Data to Output			13 18		15 18	ns	Figs. 3-3, 3-5	
t_{PZH} t_{PZL}	Output Enable Time			18 25		20 30	ns	Figs. 3-3, 3-11, 3-12	
t_{PLZ} t_{PHZ}	Output Disable Time			16 18		30 30	ns	Figs. 3-3, 3-11, 3-12	

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

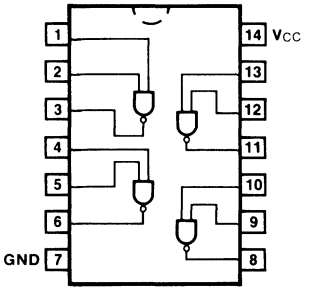
54/74132
54S/74S132
54LS/74LS132

QUAD 2-INPUT SCHMITT TRIGGER NAND GATE

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74132PC, 74S132PC 74LS132PC		9A
Ceramic DIP (D)	A	74132DC, 74S132DC 74LS132DC	54132DM, 54S132DM 54LS132DM	6A
Flatpak (F)	A	74132FC, 74S132FC 74LS132FC	54132FM, 54S132FM 54LS132FM	3I

CONNECTION DIAGRAM
PINOUT A



INPUT LOADING/FAN-OUT: See Section 3 for U.L. defintions

PINS	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/0.75	1.25/1.25	0.5/0.25
Outputs	20/10	25/12.5	10/5.0 (2.5)

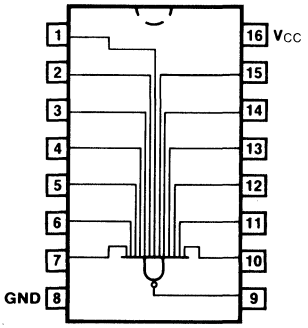
DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
V_{T+}	Positive-going Threshold Voltage	1.5	2.0	1.6	1.9	1.4	1.9	V	V_{CC} = +5.0 V
V_{T-}	Negative-going Threshold Voltage	0.6	1.1	1.1	1.4	0.5	1.0	V	V_{CC} = +5.0 V
$V_{T+} - V_{T-}$	Hysteresis Voltage	0.4		0.2		0.4		V	V_{CC} = +5.0 V
I_{T+}	Input Current at Positive-going Threshold	-0.43**		-0.9 **		-0.14**		mA	V_{CC} = +5.0 V, V_{IN} = V_{T+}
I_{T-}	Input Current at Negative-going Threshold	-0.56**		-1.1 **		-0.18**		mA	V_{CC} = +5.0 V, V_{IN} = V_{T-}
I_{OS}	Output Short Circuit Current	-18	-55					mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CCH}	Power Supply Current		24		44		11	mA	V_{IN} = Gnd; V_{CC} = Max
I_{CCL}			40		68		14		V_{IN} = Open; V_{CC} = Max
t_{PLH}	Propagation Delay		22		10.5		20	ns	Figs. 3-1, 3-4
t_{PHL}			22		13		20		

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V. **Typical Value

54S/74S133
54LS/74LS133
13-INPUT NAND GATE

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S133PC, 74LS133PC		9B
Ceramic DIP (D)	A	74S133DC, 74LS133DC	54S133DM, 54LS133DM	6B
Flatpak (F)	A	74S133FC, 74LS133FC	54S133FM, 54LS133FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.25/1.25	0.5/0.25
Outputs	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply Current		5.0		0.5	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			10		1.1		V_{IN} = Open	
t_{PLH}	Propagation Delay		6.0		15	ns	Figs. 3-1, 3-4	
t_{PHL}			7.0		38			

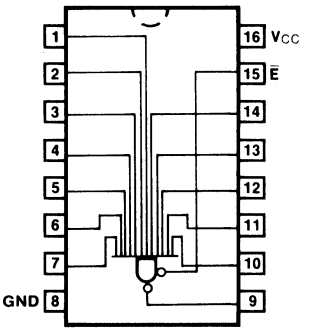
*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54S/74S134

12-INPUT NAND GATE

(With 3-State Outputs)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	74S134PC		9B
Ceramic DIP (D)	A	74S134DC	54S134DM	6B
Flatpak (F)	A	74S134FC	54S134FM	4L

TRUTH TABLE

INPUTS	OUTPUTS	
A..... L	Enable	Y
H..... H	L	L
Any In LOW	L	H
X..... X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74S (U.L.) HIGH/LOW
Inputs	1.25/1.25
Outputs	50/12.5

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER		54/74S Min	54/74S Max	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	XM	2.4		V	I_{OH} = -2.0 mA	V_{CC} = Min
		XC	2.4			I_{OH} = -6.5 mA	V_{IN} = 0.8 V
I_{CC}	Power Supply Current	Outputs HIGH		13	mA	V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V	V_{CC} = Max
		Outputs LOW		16		V_{IN} = 5.0 V, $V_{\overline{E}}$ = 0 V	
		Outputs OFF		25		V_{IN} = 5.0 V, $V_{\overline{E}}$ = 5.0 V	
t_{PLH} t_{PHL}	Propagation Delay Data to Output		2.0 2.0	6.0 7.5	ns	Figs. 3-3, 3-4	
t_{PZH} t_{PZL}	Output Enable Time			19.5 21	ns	Figs. 3-3, 3-11, 3-12	
t_{PHZ} t_{PLZ}	Output Disable Time			8.5 14	ns	Figs. 3-3, 3-11, 3-12	

*DC limits apply over operating temperature range; AC limits apply at T_A = +25° C and V_{CC} = +5.0 V.

54S/74S135

QUAD EXCLUSIVE-OR/NOR GATE

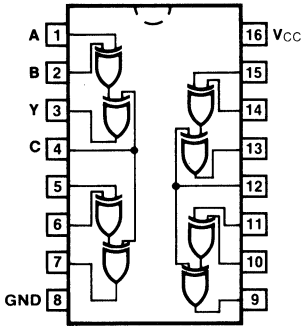
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S135PC		9B
Ceramic DIP (D)	A	74S135DC	54S135DM	6B
Flatpak (F)	A	74S135FC	54S135FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74S (U.L.) HIGH/LOW
Inputs	1.25/1.25
Outputs	25/12.5

CONNECTION DIAGRAM
PINOUT A



TRUTH TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74S Min	54/74S Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current		99	mA	V_{CC} = Max, V_{IN} = Gnd
t_{PLH} t_{PHL}	Propagation Delay from A or B to Y		13 10	ns	A or B = L, C = L Fig. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay from A or B to Y		12 13.5	ns	A or B = H, C = L Fig. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay from A or B to Y		13 10	ns	A or B = L, C = H Fig. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay from A or B to Y		12 13	ns	A or B = H, C = H Fig. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay from C to Y		12 12	ns	A = B, Fig. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay from C to Y		11.5 12	ns	A ≠ B, Fig. 3-1, 3-4

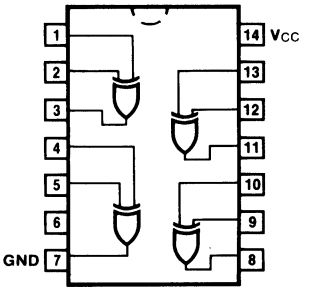
*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = + 5.0 V.

54LS/74LS136

QUAD 2-INPUT EXCLUSIVE-OR GATE

(With Open-Collector Outputs)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS136PC		9A
Ceramic DIP (D)	A	74LS136DC	54LS136DM	6A
Flatpak (F)	A	74LS136FC	54LS136FM	3I

TRUTH TABLE

INPUTS		OUTPUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/0.375
Outputs	OC**/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current		10	mA	V_{CC} = Max
t_{PLH} t_{PHL}	Propagation Delay		23 23	ns	Other Input LOW Figs. 3-2, 3-5
t_{PLH} t_{PHL}	Propagation Delay		23 23	ns	Other Input HIGH Figs. 3-2, 3-4

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
**OC — Open Collector

54S/74S137

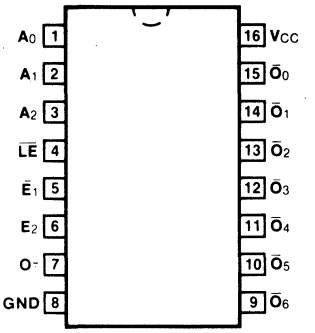
1-OF-8 DECODER/DEMULTIPLEXER

(With Input Latches)

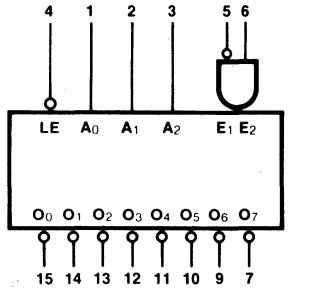
DESCRIPTION — The 'S137 is a very high speed 1-of-8 decoder/demultiplexer with latches on the three address inputs. This device essentially combines the function and speed of the 'S138 1-of-8 decoder with a 3-bit storage latch. When the latch is enabled ($\overline{LE}$ = LOW), the 'S137 acts as a 1-of-8 active LOW decoder. When the Latch Enable ($\overline{LE}$) goes from LOW to HIGH, the last data present at the inputs before this transition is stored in the latches. Further address changes are ignored as long as $\overline{LE}$ remains HIGH. The output enable gate ($\overline{E}_1 \bullet E_2$) controls the state of the outputs independent of the Address inputs or latch operation. All outputs are HIGH unless $\overline{E}_1$ is LOW and E_2 is HIGH. The 'S137 is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems. The 'S137 is fabricated with the Schottky barrier diode process for high speed.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **COMBINES 1-OF-8 DECODER WITH 3-BIT LATCH**
- **MULTIPLE INPUT ENABLE FOR EASY EXPANSION OR INDEPENDENT CONTROLS**
- **ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S137PC		9B
Ceramic DIP (D)	A	74S137DC	54S137DM	6B
Flatpak (F)	A	74S137FC	54S137FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

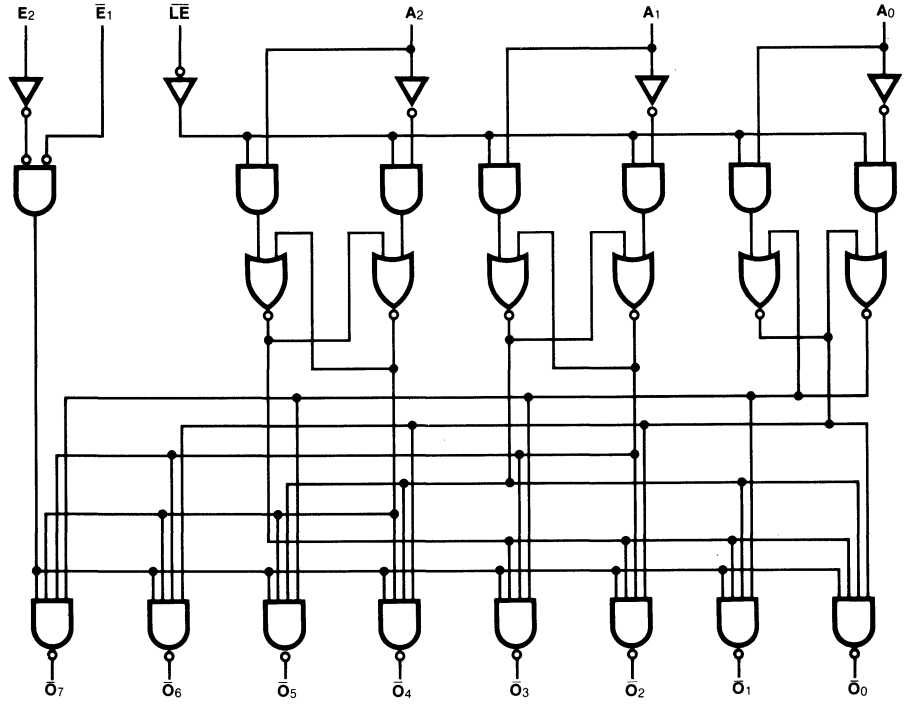
PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW
$A_0 - A_2$	Address Inputs	1.25/1.25
$\overline{LE}$	Latch Enable Input (Active LOW)	1.25/1.25
$\overline{E}_1$	Enable Input (Active LOW)	1.25/1.25
E_2	Enable Input (Active HIGH)	1.25/1.25
$\overline{O}_0 - \overline{O}_7$	Outputs (Active LOW)	25/12.5

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{LE}$	$\overline{E}_1$	E_2	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	L	H	X	X	X	STABLE							
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The 'S137 is a very high speed 1-of-8 decoder/demultiplexer fabricated with the Schottky barrier diode process. The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW outputs ($\overline{O}_0$ — $\overline{O}_7$). The 'S137 also features a 3-bit latch on the Address inputs. The device functions as a 1-of-8 decoder (same as 'S138) when the Latch Enable ($\overline{LE}$) is LOW. When $\overline{LE}$ is HIGH, the address present one setup time prior to the LOW-to-HIGH transition of $\overline{LE}$ will be stored in the address latches and the outputs will not be affected by further address changes. The output enable control is an AND gate comprised of one active LOW input ($\overline{E}_1$) and one active HIGH input (E_2). All outputs are HIGH unless the enable inputs ($\overline{E}_1 \bullet E_2$) are in their true (active) state.

A non-overlapping decoder with edge-triggered address inputs can be easily implemented by tying the Latch Enable input $\overline{LE}$ to the active HIGH Enable input (E_2). When this input ($\overline{LE} \bullet E_2$) is LOW, all outputs are forced HIGH and a new address enters the latches. When the $\overline{LE} \bullet E_2$ input goes HIGH, the address is stored in the latches and the corresponding output gate is enabled (goes LOW). In this configuration, the address must be stable only one setup time prior to the LOW-to-HIGH transition of the $\overline{LE} \bullet E_2$ input. The addressed output remains active LOW as long as the ($\overline{LE} \bullet E_2$) input remains HIGH, even if the address changes. Data or control information can thus be strobed into the 'S137 from very noisy or bus oriented systems using a LOW pulse width equal to the minimum latch enable pulse width $t_w(L)$.

The multiple enable inputs along with the address latches allows easy expansion to a 1-of-64 decoder with nonoverlapping outputs (see *Figure a*).

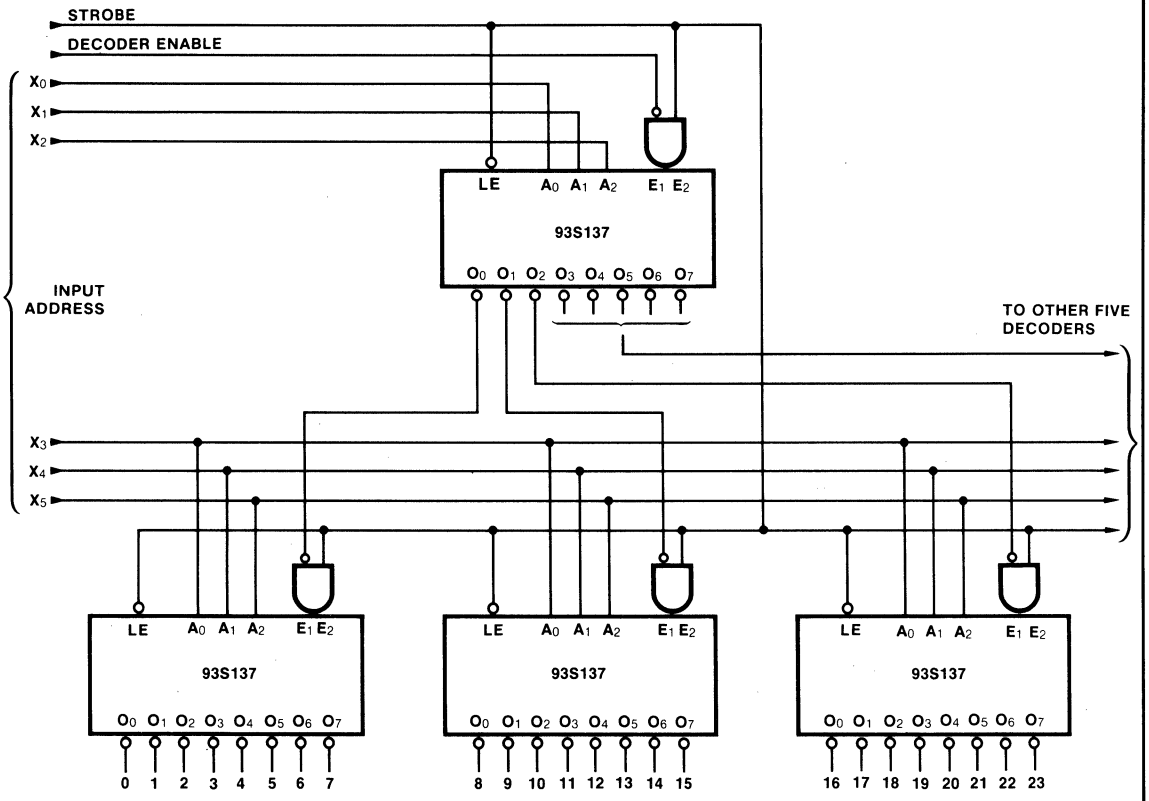


Fig. a High Speed 1-of-64 Decoder with Input Data Storage

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		95	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

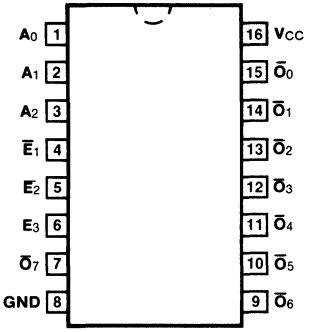
SYMBOL	PARAMETER	54/74S C_L = 15 pF, R_L = 280 Ω		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$		12 20	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ to $\overline{O}_n$		10 12	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay E_2 to $\overline{O}_n$		12 12	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$ to $\overline{O}_n$		12 20	ns	Figs. 3-1, 3-9

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74S		UNITS	CONDITIONS
		Min	Max		
t_s (H)	Setup Time HIGH A_n to $\overline{LE}$	4.5		ns	Fig. 3-13
t_h (H)	Hold Time HIGH A_n to $\overline{LE}$	0		ns	
t_s (L)	Setup Time LOW A_n to $\overline{LE}$	6.5		ns	Fig. 3-13
t_h (L)	Hold Time LOW A_n to $\overline{LE}$	0		ns	
t_w (L)	$\overline{LE}$ Pulse Width LOW	7.0		ns	Fig. 3-21

54S/74S138
54LS/74LS138
1-OF-8 DECODER/DEMULTIPLEXER

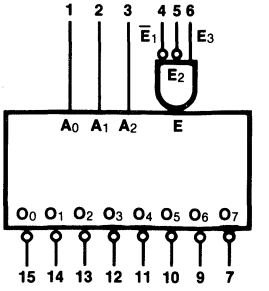
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '138 is a high speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three '138 devices or to a 1-of-32 decoder using four '138 devices and one inverter. The '138 is fabricated with the Schottky barrier diode process for high speed.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **DEMULTIPLEXING CAPABILITY**
- **MULTIPLE INPUT ENABLE FOR EASY EXPANSION**
- **ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S138PC, 74LS138PC		9B
Ceramic DIP (D)	A	74S138DC, 74LS138DC	54S138DM, 54LS138DM	6B
Flatpak (F)	A	74S138FC, 74LS138FC	54S138FM, 54LS138FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_2$	Address Inputs	1.25/1.25	0.5/0.25
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)	1.25/1.25	0.5/0.25
E_3	Enable Input (Active HIGH)	1.25/1.25	0.5/0.25
$\overline{O}_0 - \overline{O}_7$	Outputs (Active LOW)	25/12.5	10/5.0 (2.5)

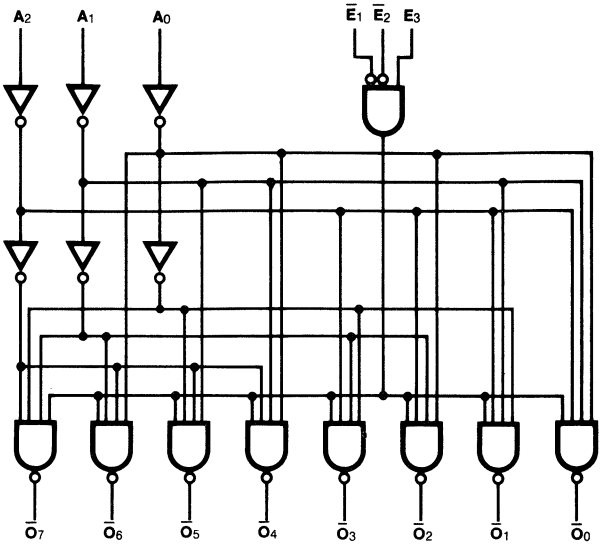
FUNCTIONAL DESCRIPTION — The '138 is a high speed 1-of-8 decoder/demultiplexer fabricated with the low power Schottky barrrier diode process. The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW outputs ($\overline{O}_0$ — $\overline{O}_7$). The '138 features three Enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four '138 devices and one inverter. (See *Figure a.*) The '138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



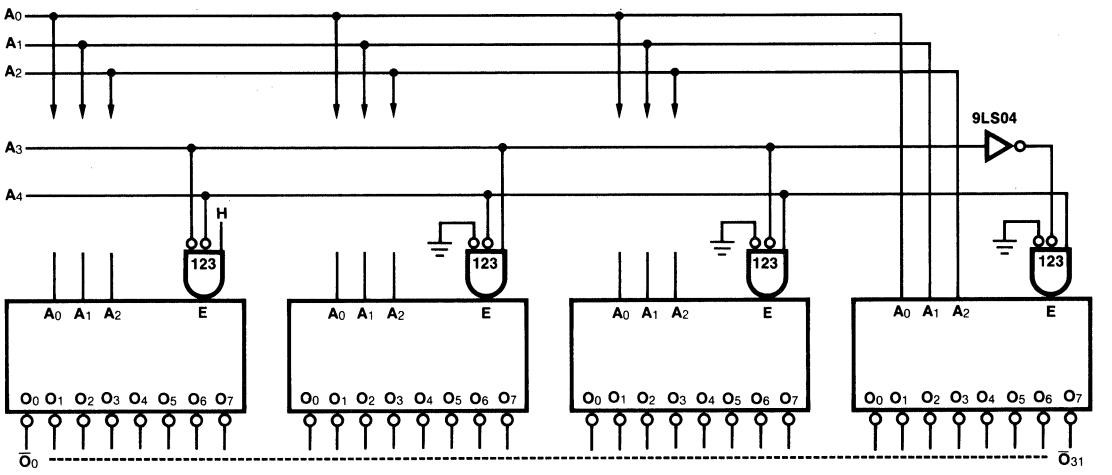


Fig. a

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		74		10	mA	V_{CC} = Max

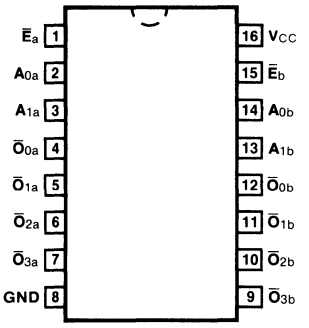
AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF, R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$		12 12		18 27	ns	Figs. 3-1, 3-4, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$		8.0 11		15 24	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay E_3 to $\overline{O}_n$		11 11		18 28	ns	Figs. 3-1, 3-4

139

54S/74S139
54LS/74LS139
DUAL 1-OF-4 DECODER

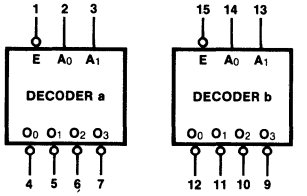
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '139 is a high speed dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the '139 can be used as a function generator providing all four minterms of two variables. The '139 is fabricated with the Schottky barrier diode process for high speed.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **TWO COMPLETELY INDEPENDENT 1-OF-4 DECODERS**
- **ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74S139PC, 74LS139PC		9B
Ceramic DIP (D)	A	74S139DC, 74LS139DC	54S139DM, 54LS139DM	6B
Flatpak (F)	A	74S139FC, 74LS139FC	54S139FM, 54LS139FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
A_0, A_1	Address Inputs	1.25/1.25	0.5/0.25
$\overline{E}$	Enable Input (Active LOW)	1.25/1.25	0.5/0.25
$\overline{O}_0 - \overline{O}_3$	Outputs (Active LOW)	25/12.5	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '139 is a high speed dual 1-of-4 decoder/demultiplexer fabricated with the Schottky barrier diode process. The device has two independent decoders, each of which accepts two binary weighted inputs (A_0, A_1) and provides four mutually exclusive active LOW outputs ($\overline{O}_0 - \overline{O}_3$). Each decoder has an active LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application. Each half of the '139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in *Figure a*, and thereby reducing the number of packages required in a logic network.

TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

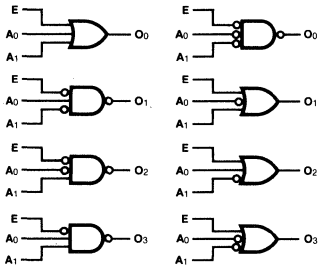
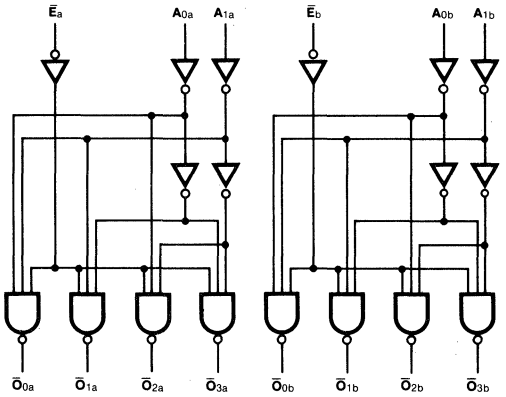


Fig. a

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwisespecified)

SYMBOL	PARAMETER	54/74LS		54/74S		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		11		90	mA	V_{CC} = Max

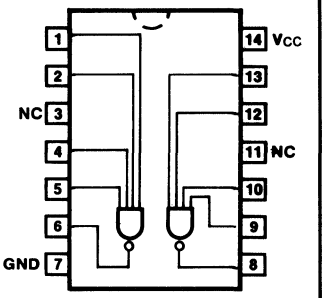
AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		54/74S		UNITS	CONDITIONS
		C_L = 15 pF		C_L = 15 pF R_L = 280 Ω			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_0 or A_1 to $\overline{O}_n$		18 27		12 12	ns	Figs. 3-1, 3-4, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{O}_n$		15 24		8.0 10	ns	Figs. 3-1, 3-5

54S/74S140

DUAL 4-INPUT NAND LINE DRIVER

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S140PC		9A
Ceramic DIP (D)	A	74S140DC	54S140DM	6A
Flatpak (F)	A	74S140FC	54S140FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74S (U.L.) HIGH/LOW
Inputs	2.5/2.5
Outputs	75/37.5

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74S Min	54/74S Max	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.0		V	V_{CC} = Min, V_{IN} = 0.5 V, R_0 = 50 Ω to Gnd
V_{OL}	Output LOW Voltage		0.5	V	V_{CC} = Min, I_{OL} = 60 mA, V_{IN} = 2.0 V
I_{OS}	Output Short Circuit Current	-50	-225	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CCH} I_{CCL}	Power Supply Current		18 44	mA	V_{IN} = Gnd V_{IN} = Open V_{CC} = Max
t_{PLH} t_{PHL}	Propagation Delay		6.5 6.5	ns	Figs. 3-1, 3-4

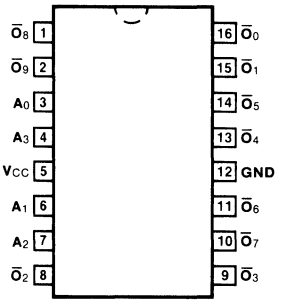
*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

74141

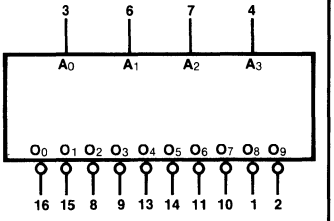
1-OF-10 DECODER/DRIVER (NIXIE)

(With Open-Collector Outputs)

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 12

DESCRIPTION — The '141 is a BCD-to-decimal decoder driver that is designed to accept a 4-bit BCD code input and drive cold-cathode indicator tubes. This decoder utilizes design improvements that minimize switching transients in order to maintain a stable display. The segments and numeric designations chosen to represent the decimal numbers are shown in the Truth Table. For binary inputs 10 through 15, the outputs are OFF. These invalid codes can be used in blanking leading or trailing-edge zeroes in a display. The ten high performance, npn output transistors have a maximum reverse current of 50 μA at 55 V. Typical power dissipation is 55 mW.

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	PKG TYPE
Plastic DIP (P)	A	74141PC	9B
Ceramic DIP (D)	A	74141DC	6B

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

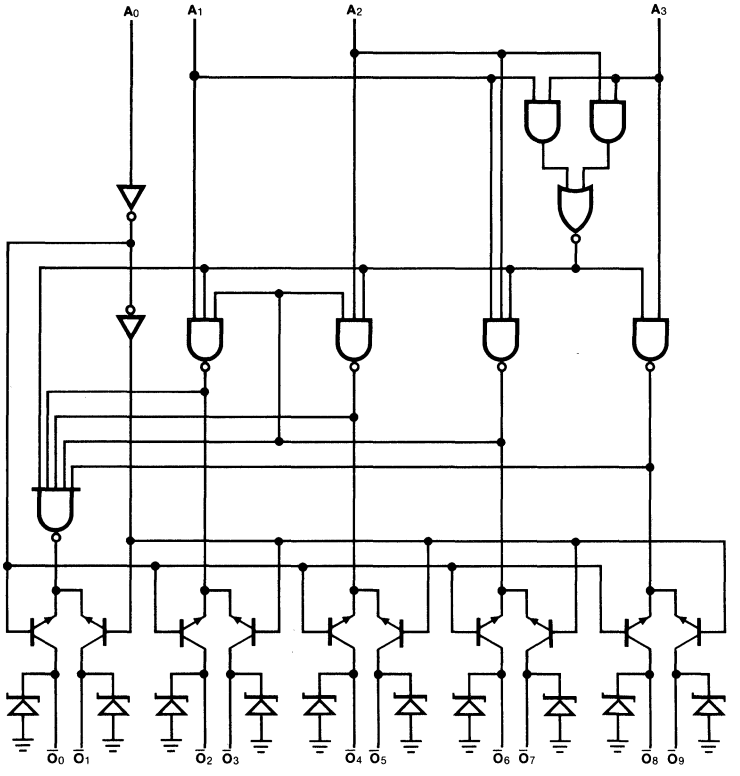
PIN NAMES	DESCRIPTION	74XX (U.L.) HIGH/LOW
A_0	BCD Input	1.0/1.0
A_1 — A_3	BCD Inputs	2.0/2.0
$\overline{O}_0$ — $\overline{O}_9$	Outputs (Active LOW)	OC*/7.0 mA

*OC — Open Collector

141

FUNCTIONAL DESCRIPTION — The 1-of-10 decoder/driver accepts BCD inputs from all TTL circuits and produces the correct output selection to directly drive gas filled cold cathode indicator tubes. The outputs are selected as shown in the Truth Table. It is capable of driving all known available cold cathode indicator tubes having 7.0 mA or less cathode current.

LOGIC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUT
A_3	A_2	A_1	A_0	ON†
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	X	H	X	NONE
H	H	X	X	NONE

†All other outputs are off
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	74XX Min	74XX Max	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage		2.5	V	V_{CC} = Min I_O = 7.0 mA
V_{OH}	Output HIGH Voltage (for Input Counts 0 thru 9)	60		V	V_{CC} = Max I_O = 0.5 mA
I_{OH}	Output HIGH Current		50	μA	V_{CC} = Max V_O = 55 V
I_{OH}	Output HIGH Current (for Input Counts 10 thru 15)		5.0 15	μA	T_A = 55°C T_A = 70°C V_{CC} = Max V_O = 30 V
I_{CC}	Power Supply Current		25	mA	V_{CC} = Max All Inputs = Gnd

54/74145

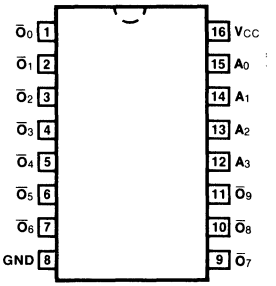
1-OF-10 DECODER/DRIVER

(With Open-Collector Outputs)

DESCRIPTION — The '145 decoder/drivers are designed to accept BCD inputs and provide appropriate outputs to drive 7-segment numerical displays. All outputs remain OFF for all invalid binary input conditions. These devices are designed for use as indicator/relay drivers or as open-collector logic circuit drivers. Each of the high breakdown (15 V) output transistors will sink up to 80 mA of current.

- **OPEN-COLLECTOR OUTPUTS**
- **80 mA CURRENT SINKING**
- **15 V GUARANTEED BREAKDOWN**

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

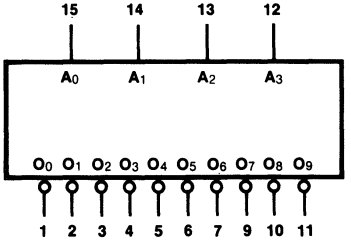
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	74145PC		9B
Ceramic DIP (D)	A	74145DC	54145DM	7B
Flatpak (F)	A	74145FC	54145FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
A_0 — A_3	BCD Inputs	1.0/1.0
$\overline{O}_0$ — $\overline{O}_9$	Outputs (Active LOW)	OC*/12.5

*OC — Open Collector

LOGIC SYMBOL

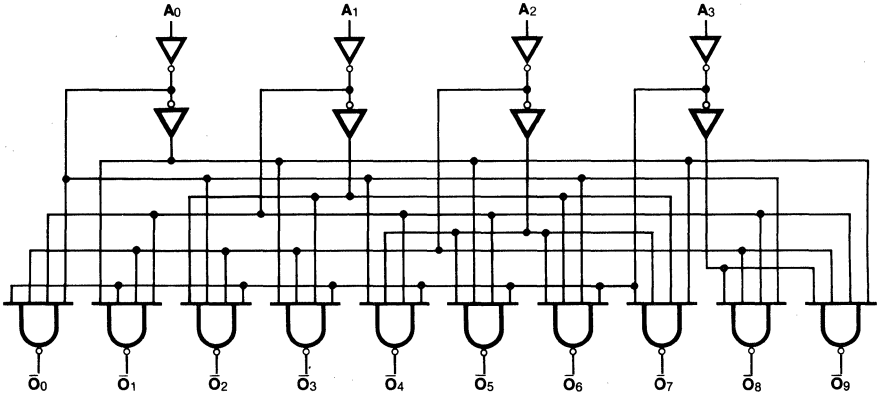


TRUTH TABLE

INPUTS				OUTPUTS									
A_0	A_1	A_2	A_3	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$	$\overline{O}_8$	$\overline{O}_9$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage			0.9	V	V_{CC} = Min, I_{OL} = 80 mA
I_{OH}	Output HIGH Current			250	μA	V_{CC} = Max, V_{OH} = 15 V
I_{CC}	Power Supply Current	XC		70	mA	V_{CC} = Max, V_{IN} = Gnd
		XM		62		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 100 Ω Min	54/74 C_L = 15 pF R_L = 100 Ω Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$		50 50	ns	Figs. 3-2, 3-20

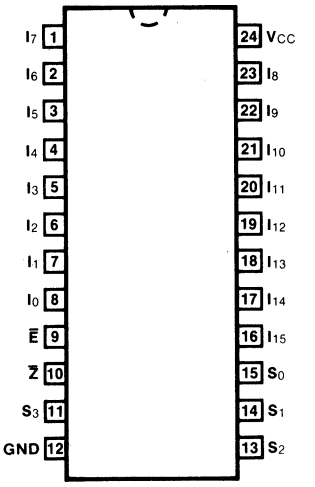
4

54/74150

16-INPUT MULTIPLEXER

DESCRIPTION — Signals applied to the Select ($S_0 - S_3$) inputs determine which of the data inputs ($I_0 - I_{15}$) is routed through to the output. Data from the selected input appears at the output ($\overline{Z}$) in inverted form. When the active-LOW Enable input is HIGH, the output will be HIGH, regardless of other input conditions.

CONNECTION DIAGRAM
PINOUT A



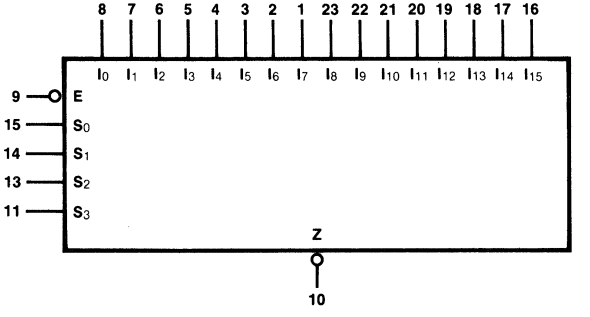
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +70°C	
Plastic DIP (P)	A	74150PC		9N
Ceramic DIP (D)	A	74150DC	54150DM	6N
Flatpak (F)	A	74150FC	54150FM	4M

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

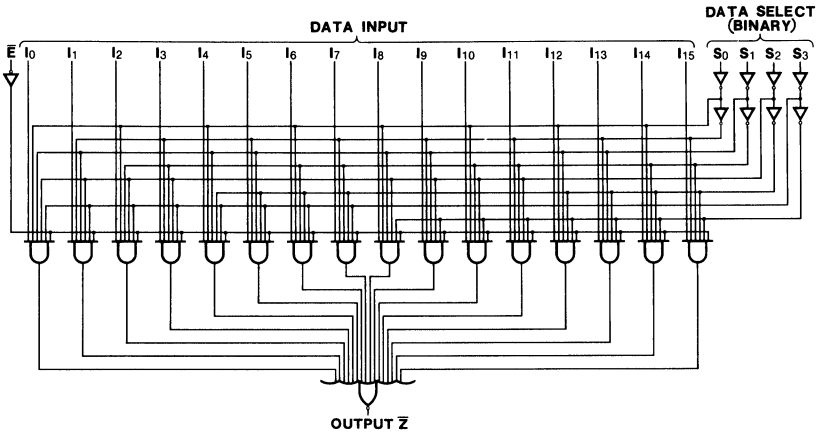
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$I_0 - I_{15}$	Data Inputs	1.0/1.0
$S_0 - S_3$	Select Inputs	1.0/1.0
$\overline{E}$	Enable Input (Active LOW)	1.0/1.0
$\overline{Z}$	Inverted Data Output	20/10

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM



TRUTH TABLE

INPUTS					OUTPUT
S_3	S_2	S_1	S_0	$\overline{E}$	$\overline{Z}$
X	X	X	X	H	H
L	L	L	L	L	$\overline{I}_0$
L	L	L	H	L	$\overline{I}_1$
L	L	H	L	L	$\overline{I}_2$
•	•	•	•	•	•
H	H	L	L	L	$\overline{I}_{12}$
H	H	L	H	L	$\overline{I}_{13}$
H	H	H	L	L	$\overline{I}_{14}$
H	H	H	H	L	$\overline{I}_{15}$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

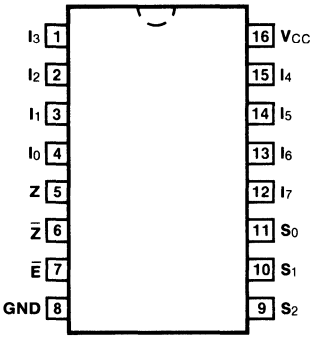
SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	XM	-20	-55	mA	V_{CC} = Max
		XC	-18	-55		
I_{CC}	Power Supply Current			68	mA	V_{CC} = Max, V_{IN} = 4.5V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

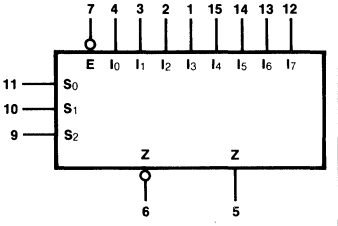
SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 C_L = 15 pF, R_L = 400 Ω Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}$, 3 Levels		35 33	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}$		20 14	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$		24 30	ns	Figs. 3-1, 3-5

54/74151A
54S/74S151
54LS/74LS151
8-INPUT MULTIPLEXER

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

DESCRIPTION — The '151 is a high speed 8-input digital multiplexer. It provides in one package, the ability to select one line of data from up to eight sources. The '151 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74151APC, 74S151PC 74LS151PC		9B
Ceramic DIP (D)	A	74151ADC, 74S151DC 74LS151DC	54151ADM, 54S151DM 54LS151DM	6B
Flatpak (F)	A	74151AFC, 74S151FC 74LS151FC	54151AFM, 54S151FM 54LS151FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$I_0 - I_7$	Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
$S_0 - S_2$	Select Inputs	1.0/1.0	1.25/1.25	0.5/0.25
$\overline{E}$	Enable Input (Active LOW)	1.0/1.0	1.25/1.25	0.5/0.25
Z	Data Output	20/10	25/12.5	10/5.0 (2.5)
$\overline{Z}$	Inverted Data Output	20/10	25/12.5	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '151 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Enable input ($\overline{E}$) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2).$$

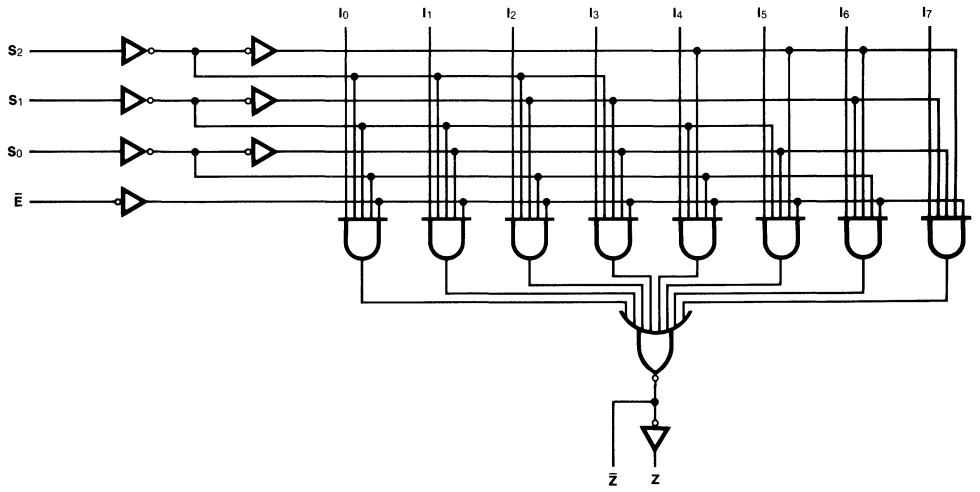
The '151 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the '151 can provide any logic function of four variables and its negation.

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{E}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

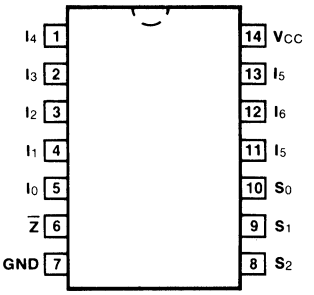
SYMBOL	PARAMETER		54/74		54/74S		54/74LS		UNITS	CONDITIONS
			Min	Max	Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current	XM	-20	-55	-40	-100	-20	-100	mA	V_{CC} = Max
		XC	-18	-55	-40	-100	-20	-100		
I_{CC}	Power Supply Current			48		70		10	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF, R_L = 400 Ω		C_L = 15 pF, R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}$		26 30		15 13.5		23 34	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay S_n to Z		38 38		18 18		48 30	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$		21 23		13 12		24 30	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z		33 33		16.5 18		42 32	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}$		14 14		7.0 7.0		21 20	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay I_n to Z		20 27		12 12		32 26	ns	Figs. 3-1, 3-5

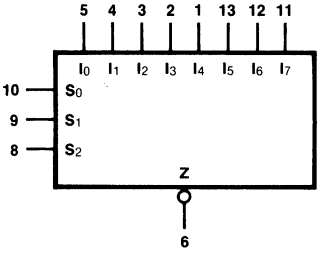
54/74152A
54LS/74LS152
8-INPUT MULTIPLEXER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '152 is a high speed 8-input digital multiplexer. It provides, in one package, the ability to select one line of data from up to eight sources. The '152 can be used as a universal function generator to generate any logic function of four variables. It is supplied in Flatpak only; for Dual In-line Package applications use the 'LS151.

LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

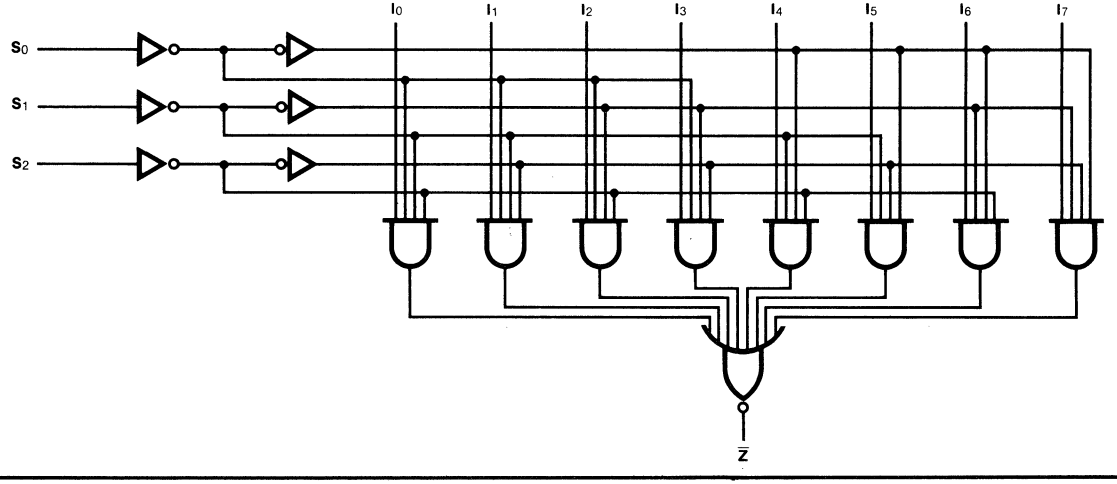
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		VCC = +5.0 V ±5%, TA = 0° C to +70° C	VCC = +5.0 V ±10%, TA = -55° C to +125° C	
Flatpak (F)	A	74152AFC, 74LS152FC	54152AFM, 54LS152FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$I_0 - I_7$	Data Inputs	1.0/1.0	0.5/0.25
$S_0 - S_2$	Select Inputs	1.0/1.0	0.5/0.25
$\overline{Z}$	Inverted Data Output	20/10	10/5.0 (2.5)

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The '152 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. The logic function provided at the output is:

$$Z = (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2).$$

The '152 provides the ability, in one package, to select from eight sources of data or control information.

TRUTH TABLE

INPUTS			OUTPUT
S_2	S_1	S_0	$\overline{Z}$
L	L	L	$\overline{I}_0$
L	L	H	$\overline{I}_1$
L	H	L	$\overline{I}_2$
L	H	H	$\overline{I}_3$
H	L	L	$\overline{I}_4$
H	L	H	$\overline{I}_5$
H	H	L	$\overline{I}_6$
H	H	H	$\overline{I}_7$

H = HIGH Voltage Level
L = LOW Voltage Level

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74		54/74LS		UNITS	CONDITIONS
			Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current	XM	-20	-55	-20	-100	mA	V_{CC} = Max
		XC	-18	-55	-20	-100		
I_{CC}	Power Supply Current			43		9.0	mA	V_{CC} = Max

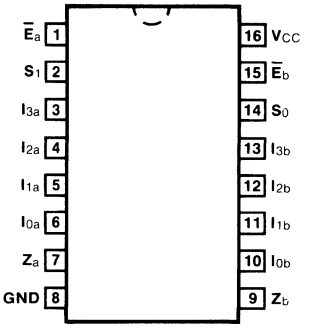
AC CHARACTERISTICS: V_{CC} = +5.0V, T_A = +125° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω		54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}$		26 30		23 32	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}$		14 14		21 20	ns	Figs. 3-1, 3-4

54/74153
54S/74S153
54LS/74LS153

DUAL 4-INPUT MULTIPLEXER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '153 is a high speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the '153 can generate any two functions of three variables.

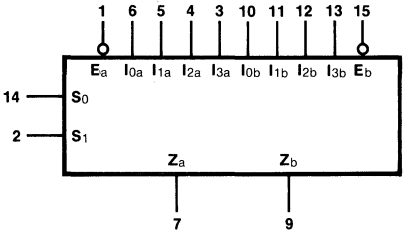
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	A	74153PC, 74S153PC 74LS153PC		9B
Ceramic DIP (D)	A	74153DC, 74S153DC 74LS153DC	54153DM, 54S153DM 53LS153DM	6B
Flatpak (F)	A	74153FC, 74S153FC 74LS153FC	54153FM, 54S153FM 54LS153FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
I_{0a} — I_{3a}	Side A Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
I_{0b} — I_{3b}	Side B Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
S_0, S_1	Common Select Inputs	1.0/1.0	1.25/1.25	0.5/0.25
$\overline{E}_a$	Side A Enable Input (Active LOW)	1.0/1.0	1.25/1.25	0.5/0.25
$\overline{E}_b$	Side B Enable Input (Active LOW)	1.0/1.0	1.25/1.25	0.5/0.25
Z_a	Side A Output	20/10	25/12.5	10/5.0 (2.5)
Z_b	Side B Output	20/10	25/12.5	10/5.0 (2.5)

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW. The '153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$
$$Z_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

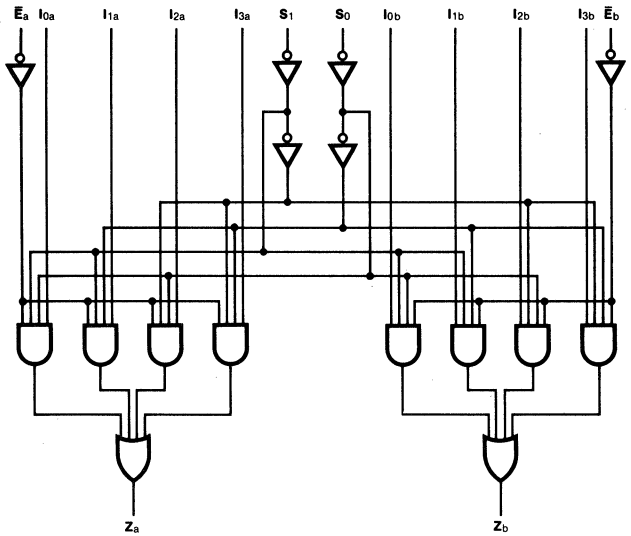
The '153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is a function generator. The '153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74		54/74S		54/74LS		UNITS	CONDITIONS
			Min	Max	Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current	XM	-20	-55	-40	-100	-20	-100	mA	V_{CC} = Max
		XC	-18	-57	-40	-100	-20	-100		
I_{CC}	Power Supply Current	XM		52		70		10	mA	V_{CC} = Max
		XC		60		70		10		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configuration)

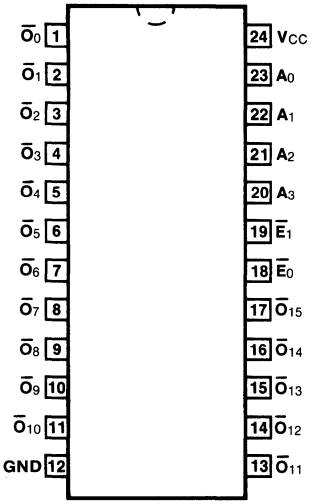
SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		C_L = 30 pF, R_L = 400 Ω		C_L = 15 pF, R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to Z_n		34 34		18 18		29 29	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n		30 23		15 13.5		29 32	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n		18 23		9.0 9.0		15 20	ns	Figs. 3-1, 3-5

54/74154

1-OF-16 DECODER/DEMULTIPLEXER

DESCRIPTION — The '154 is a multipurpose decoder designed to accept four inputs and provide 16 mutually exclusive outputs. By means of the Address (A_0 — A_3) inputs, data applied to one of the Enable inputs can be routed to any one of the outputs in True (non-inverted) form.

CONNECTION DIAGRAM
PINOUT A



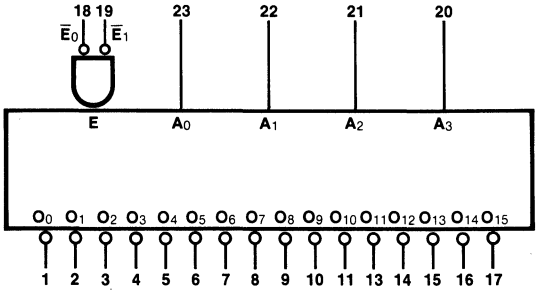
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74154PC		9N
Ceramic DIP (D)	A	74154DC	54154DM	6N
Flatpak (F)	A	74154FC	54154FM	4M

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
A_0 — A_3	Address Inputs	1.0/1.0
$\overline{E}_0$, $\overline{E}_1$	Enable Inputs (Active LOW)	1.0/1.0
$\overline{O}_0$ — $\overline{O}_{15}$	Outputs (Active LOW)	20/10

LOGIC SYMBOL



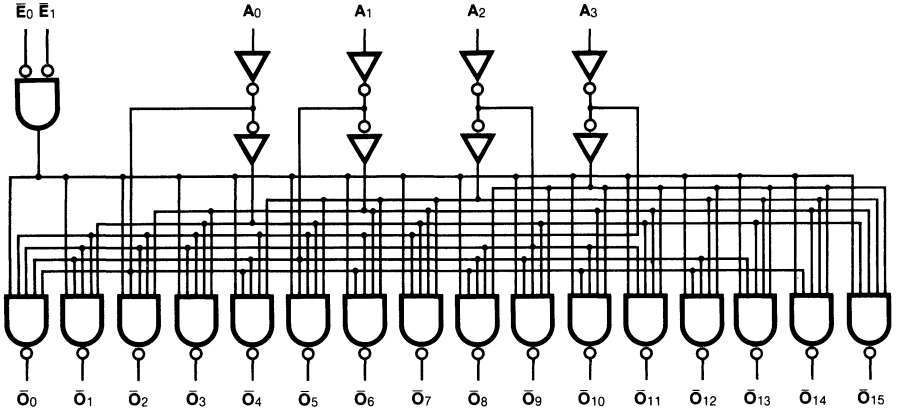
V_{CC} = Pin 24
GND = Pin 12

TRUTH TABLE

INPUTS						OUTPUTS														
$\overline{E}_0$	$\overline{E}_1$	A_0	A_1	A_2	A_3	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$	$\overline{O}_8$	$\overline{O}_9$	$\overline{O}_{10}$	$\overline{O}_{11}$	$\overline{O}_{12}$	$\overline{O}_{13}$	$\overline{O}_{14}$	$\overline{O}_{15}$
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The '154 decoder accepts four inputs and provides 16 mutually exclusive active LOW outputs, as shown by the logic symbol. The active LOW outputs facilitate addressing other MSI units with active LOW enable.

The '154 can demultiplex data by routing it from one input to one of 16 possible decoder outputs. The desired output is addressed and the data is applied to one of the enable inputs. Providing that the other enable is LOW, the addressed output will follow the state of the applied data.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

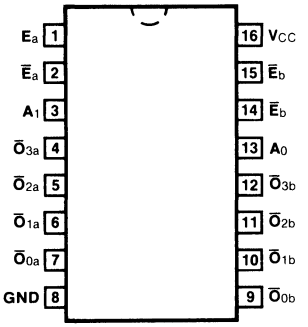
SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	XM	-20	-55	mA	V_{CC} = Max
		XC	-18	-57		
I_{CC}	Power Supply Current	XM		49	mA	V_{CC} = Max
		XC		56		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω Min	54/74 C_L = 15 pF R_L = 400 Ω Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$		31 28	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$		23 24	ns	Figs. 3-1, 3-5

54/74155
54LS/74LS155
DUAL 1-OF-4 DECODER/DEMULTIPLEXER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '155 contains two decoders with common Address (A_0, A_1) inputs and separate enable gates. Decoder "a" has an enable gate with one active HIGH and one active LOW input, while decoder "b" has two active LOW inputs. If the enable functions are satisfied, one output of each decoder will be LOW, as selected by the Address inputs.

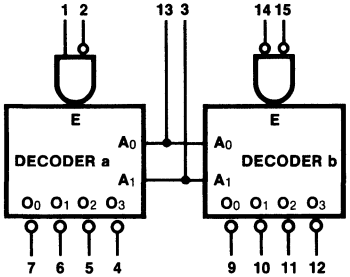
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74155PC, 74LS155PC		9B
Ceramic DIP (D)	A	74155DC, 74LS155DC	54155DM, 54LS155DM	6B
Flatpak (F)	A	74155FC, 74LS155FC	54155FM, 54LS155FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
A_0, A_1	Address Inputs	1.0/1.0	0.5/0.25
$\bar{E}_a$, $\bar{E}_b$	Enable Inputs (Active LOW)	1.0/1.0	0.5/0.25
E_a	Enable Input (Active HIGH)	1.0/1.0	0.5/0.25
$\bar{O}_0 - \bar{O}_3$	Outputs (Active LOW)	20/10	10/5.0 (2.5)

LOGIC DIAGRAM



VCC = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '155 and '156 are dual 1-of-4 decoder/demultiplexers with common Address inputs and separate gated Enable inputs. When enabled, each decoder section accepts the binary weighted Address inputs (A_0, A_1) and provides four mutually exclusive active LOW outputs ($\overline{O}_0$ - $\overline{O}_3$). If the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Each decoder section has a 2-input enable gate. The enable gate for decoder "a" requires one active HIGH input and one active LOW input (E_a, $\overline{E}_a$). In demultiplexing applications, decoder "a" can accept either true or complemented data by using the $\overline{E}_a$ or E_a inputs respectively. The enable gate for decoder "b" requires two active LOW inputs ($\overline{E}_b$, $\overline{E}_b$). The devices can be used as a 1-of-8 decoder/demultiplexer by tying E_a to $\overline{E}_b$ and relabeling the common connection as A_2. The other $\overline{E}_b$ and $\overline{E}_a$ are connected together to form the common enable.

The '155 and '156 can be used to generate all four minterms of two variables. These four minterms are useful in some applications replacing multiple gate functions as shown in *Figure a*. The '156 has the further advantage of being able to AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown below.

$$f = (E + A_0 + A_1) \bullet (E + \overline{A}_0 + A_1) \bullet (E + A_0 + \overline{A}_1) \bullet (E + \overline{A}_0 + \overline{A}_1)$$
$$\text{where} = E = E_a + \overline{E}_a;\ E = E_b + E_b$$

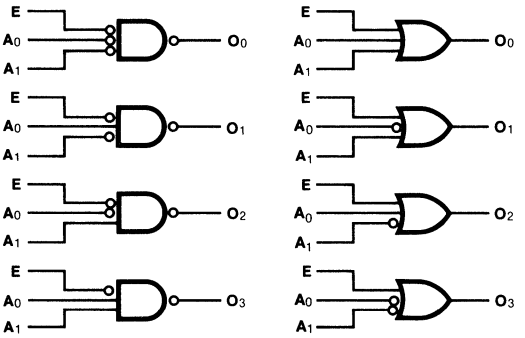
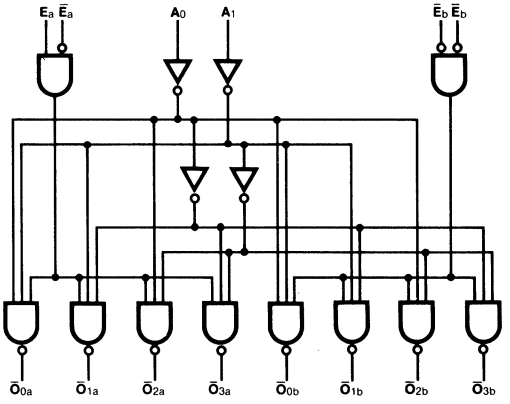


Fig. a

LOGIC DIAGRAM



TRUTH TABLE

ADDRESS		ENABLE a		OUTPUT a				ENABLE b		OUTPUT b			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{E}_b$	$\overline{E}_b$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

4

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	XM	-20	-55	-20	-100	ns	V_{CC} = Max
		XC	-18	-57	-20	-100		
I_{CC}	Power Supply Current	XM		35		10	mA	V_{CC} = Max; $\overline{E}_a$, $\overline{E}_b$ = Gnd
		XC		40		10		A_0, A_1, E_a = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

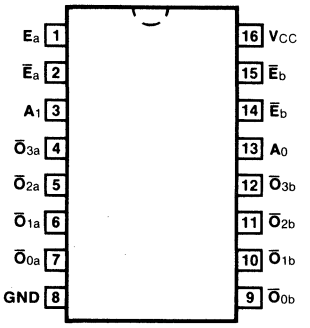
SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$		32 32		18 27	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_a$ or $\overline{E}_b$ to $\overline{O}_n$		20 27		15 24	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay E_a to $\overline{O}_n$		24 30		25 25	ns	Figs. 3-1, 3-4

54/74156
54LS/74LS156

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

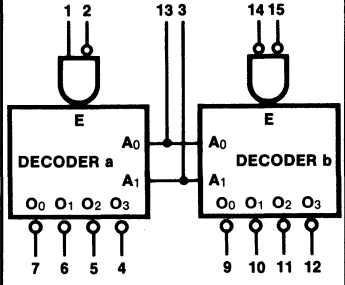
(With Open-Collector Outputs)

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '156 contains two decoders with common Address (A_0, A_1) inputs and separate enable gates. Decoder "a" has an enable gate with one active HIGH and one active LOW input, while decoder "b" has two active LOW inputs. If the enable functions are satistied, one output of each decoder will be LOW, as selected by the Address inputs. For functional description, truth table and logic diagram, please refer to the '155 data sheet.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	A	74156PC, 74LS156PC		9B
Ceramic DIP (D)	A	74156DC, 74LS156DC	54156DM, 54LS156DM	6B
Flatpak (F)	A	74156FC, 74LS156FC	54156FM, 54LS156FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
A_0, A_1	Address Inputs	1.0/1.0	0.5/0.25
$\bar{E}_a$, $\bar{E}_b$	Enable Inputs (Active LOW)	1.0/1.0	0.5/0.25
E_a	Enable Input (Active HIGH)	1.0/1.0	0.5/0.25
$\bar{O}_0 - \bar{O}_3$	Outputs (Active LOW)	OC*/10	OC*/5.0 (2.5)

*OC — Open Collector

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

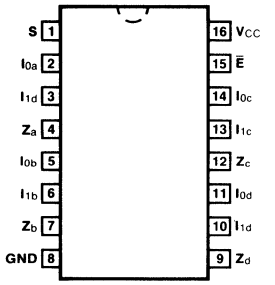
SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OH}	Output HIGH Current, OFF State			250		100	μA	V_{CC}=Min, V_{OH} = 5.5 V
I_{CC}	Power Supply Current	XM		35		10	mA	V_{CC}=Max; $\overline{E}_a$, E_b = GND
		XC		40		10		A_0, A_1, E_a=4.5 V

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25° C (See Section 3 for waveforms and load configurations)

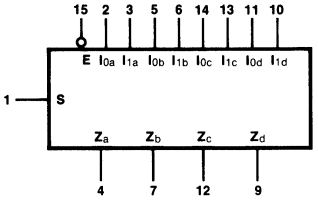
SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 C_L = 15 pF, R_L = 400 Ω Max	54/74LS C_L = 15 pF, R_L = 2 kΩ Min	54/74LS C_L = 15 pF, R_L = 2 kΩ Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$		34 34		28 33	ns	Figs. 3-2, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_a$ or $\overline{E}_b$ to $\overline{O}_n$		23 30		25 30	ns	Figs. 3-2, 3-5
t_{PLH} t_{PHL}	Propagation Delay E_a to $\overline{O}_n$		27 33		34 34	ns	Figs. 3-2, 3-4

54/74157
54S/74S157
54LS/74LS157
QUAD 2-INPUT MULTIPLEXER

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

DESCRIPTION — The '157 is a high speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The '157 can also be used to generate any four of the 16 different functions to two variables.

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74157PC, 74S157PC 74LS157PC		9B
Ceramic DIP (D)	A	74157DC, 74S157DC 74LS157DC	54157DM, 54S157DM 54LS157DM	6B
Flatpak (F)	A	74157FC, 74S157FC 74LS157FC	54157FM, 54S157FM 54LS157FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

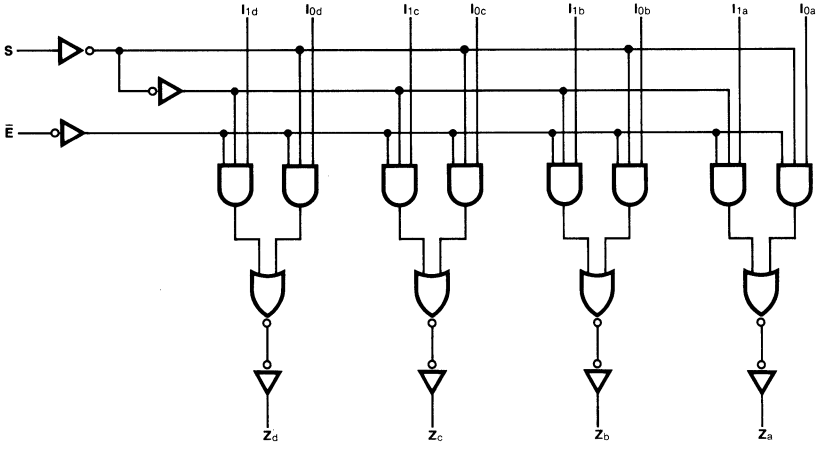
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
I0a — I0d	Source 0 Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
I1a — I1d	Source 1 Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
$\overline{E}$	Enable Input (Active LOW)	1.0/1.0	2.5/2.5	1.0/0.5
S	Select Input	1.0/1.0	2.5/2.5	1.0/0.5
Za — Zd	Outputs	20/10	25/12.5	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The '157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

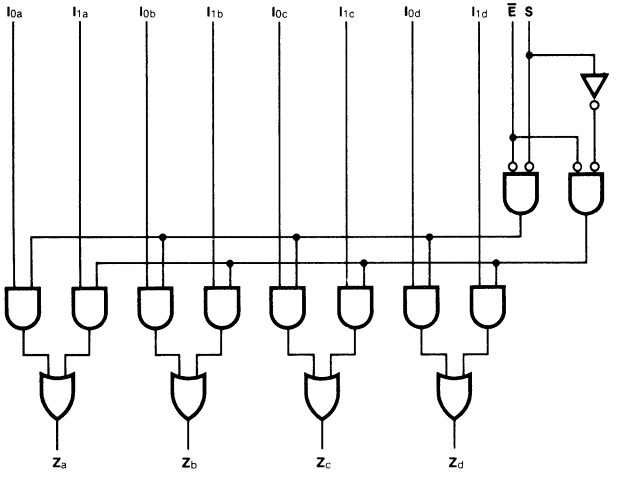
$$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S}) \qquad Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S}) \qquad Z_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

A common use of the '157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The '157 can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

LOGIC DIAGRAMS
'157



'S157 • 'LS157



TRUTH TABLE

INPUTS				OUTPUT
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74		54/74S		54/74LS		UNITS	CONDITIONS
			Min	Max	Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current	XM	-20	-55	-40	-100	-20	-100	mA	V_{CC} = Max
		XC	-18	-55	-40	-100	-20	-100		
I_{CC}	Power Supply Current			48		78		16	mA	V_{CC} = Max All Inputs = 4.5 V

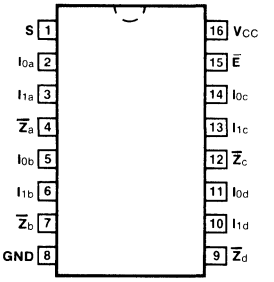
AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF R_L = 400 Ω		C_L = 15 pF R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S to Z_n		23 27		15 15		26 24	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z_n		20 21		12.5 12		20 21	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n		14 14		7.5 6.5		14 14	ns	Figs. 3-1, 3-5

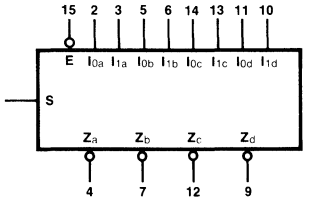
54S/74S158
54LS/74LS158
QUAD 2-INPUT MULTIPLEXER

DESCRIPTION — The '158 is a high speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The '158 can also generate any four of the 16 different functions of two variables.

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S158PC, 74LS158PC		9B
Ceramic DIP (D)	A	74S158DC, 74LS158DC	54S158DM, 54LS158DM	6B
Flatpak (F)	A	74S158FC, 74LS158FC	54S158FM, 54LS158FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
I_{0a} — I_{0d}	Source 0 Data Inputs	1.25/1.25	0.5/0.25
I_{1a} — I_{1d}	Source 1 Data Inputs	1.25/1.25	0.5/0.25
$\overline{E}$	Enable Input (Active LOW)	2.5/2.5	1.0/0.5
S	Select Input	2.5/2.5	1.0/0.5
$\overline{Z}_a$ — $\overline{Z}_d$	Inverted Outputs	25/12.5	10/5.0 (2.5)

TRUTH TABLE

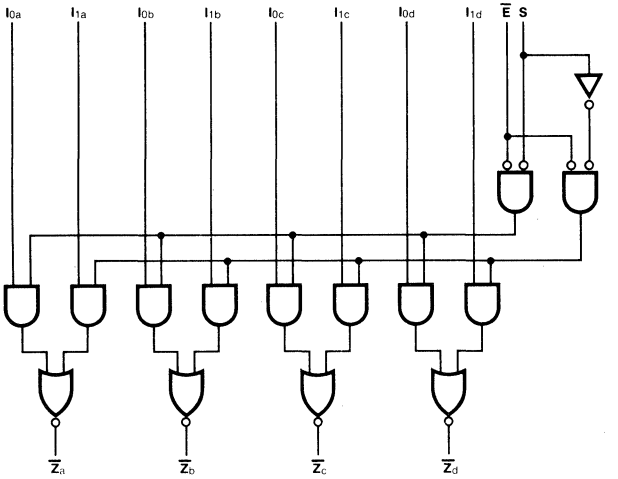
INPUTS				OUTPUTS
$\overline{E}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

FUNCTIONAL DESCRIPTION — The '158 is a quad 2-input multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs ($\overline{Z}$) are forced HIGH regardless of all other inputs. The '158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

A common use of the '158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The '158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		61		8.0	mA	V_{CC} = Max*

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF, R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay, S to $\overline{Z}$		12 12		20 24	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}$ to $\overline{Z}$		11.5 12		16 16	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay, I_n to $\overline{Z}$		6.0 6.0		13 11	ns	Figs. 3-1, 3-4

*I_{CC} measured with outputs open and 4.5 V applied to all inputs.

54/74160 • 54LS/74LS160
54/74162 • 54LS/74LS162

SYNCHRONOUS PRESETTABLE BCD DECADE COUNTERS

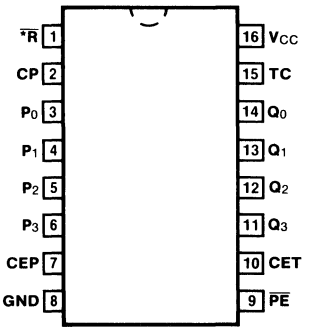
DESCRIPTION — The '160 and '162 are high speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The '160 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The '162 has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock. For the S-TTL and LP-TTL versions, please see the 9310 data sheet.

- **SYNCHRONOUS COUNTING AND LOADING**
- **HIGH SPEED SYNCHRONOUS EXPANSION**
- **TYPICAL COUNT RATE OF 35 MHz**
- **LS VERSIONS FULLY EDGE TRIGGERED**

ORDERING CODE: See Section 9

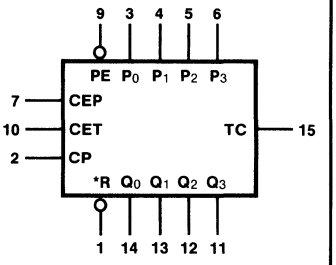
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°	PKG TYPE
Plastic DIP (P)	A	74160PC, 74LS160PC 74162PC, 74LS162PC		9B
Ceramic DIP (D)	A	74160DC, 74LS160DC 74162DC, 74LS162DC	54160DM, 54LS160DM 54162DM, 54LS162DM	7B
Flatpak (F)	A	74160FC, 74LS160FC 74162FC, 74LS162FC	54160FM, 54LS160FM 54162FM, 54LS162FM	4L

CONNECTION DIAGRAM
PINOUT A



*$\overline{MR}$ for '160
*$\overline{SR}$ for '162

LOGIC SYMBOL



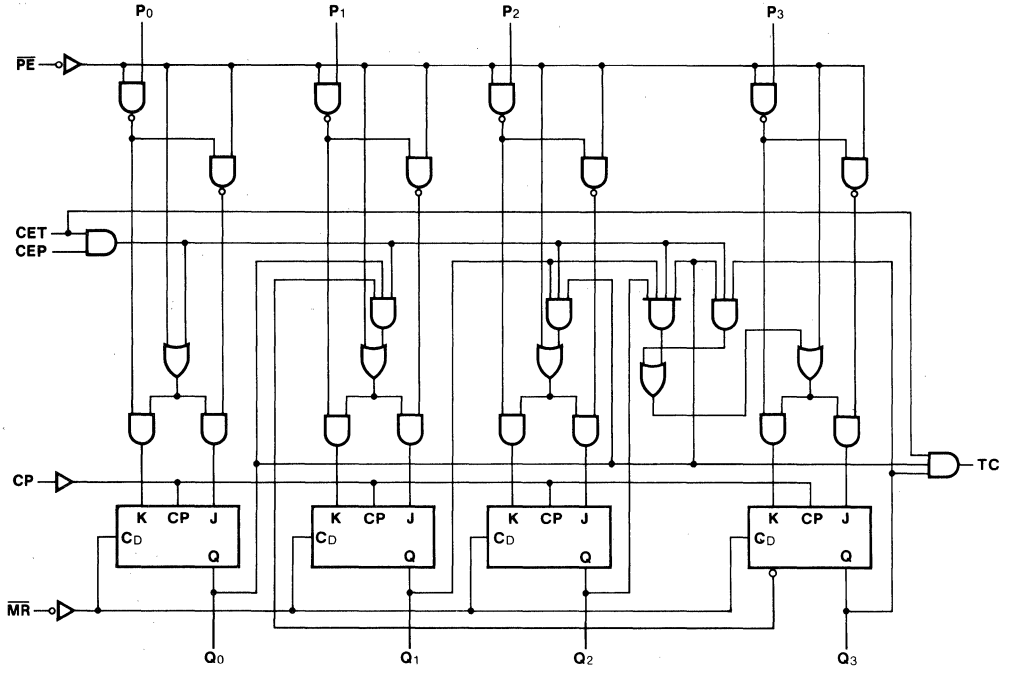
V_{CC} = Pin 16 *$\overline{MR}$ for '160
GND = Pin 8 *$\overline{SR}$ for '162

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

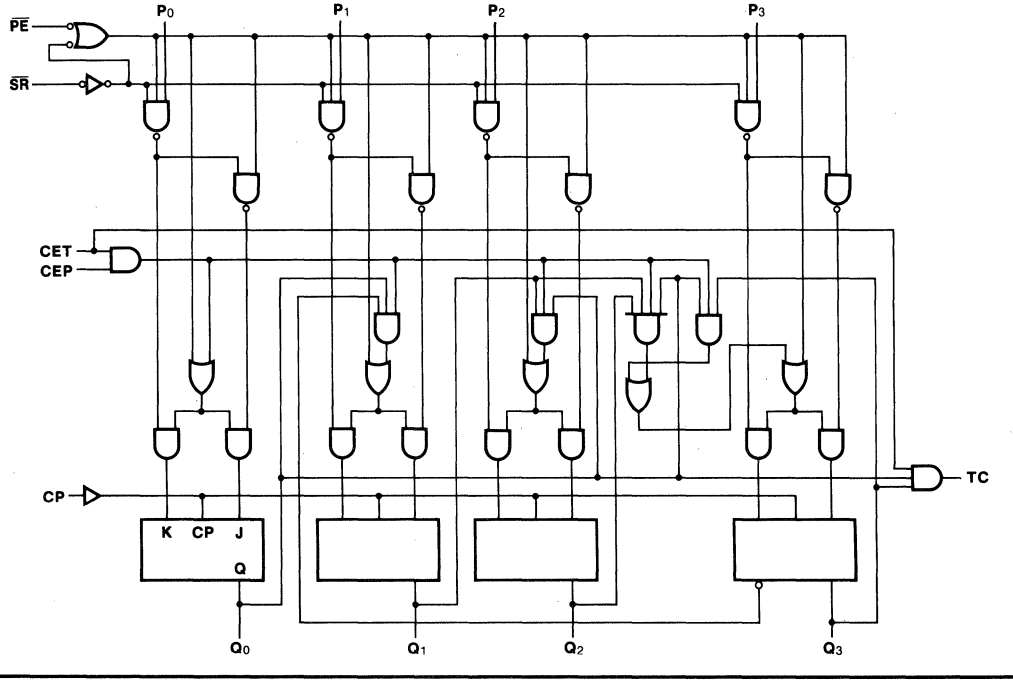
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
CEP	Count Enable Parallel Input	1.0/1.0	0.6/0.3
CET	Count Enable Trickle Input	2.0/2.0	1.0/0.5
CP	Clock Pulse Input (Active Rising Edge)	2.0/2.0	0.6/0.3
$\overline{MR}$ ('160)	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{SR}$ ('162)	Synchronous Reset Input (Active LOW)	1.0/1.0	0.5/0.25
P_0 — P_3	Parallel Data Inputs	1.0/1.0	0.5/0.25
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0	0.6/0.3
Q_0 — Q_3	Flip-flop Outputs	20/10	10/5.0 (2.5)
TC	Terminal Count Output	20/10	10/5.0 (2.5)

LOGIC DIAGRAMS

'160

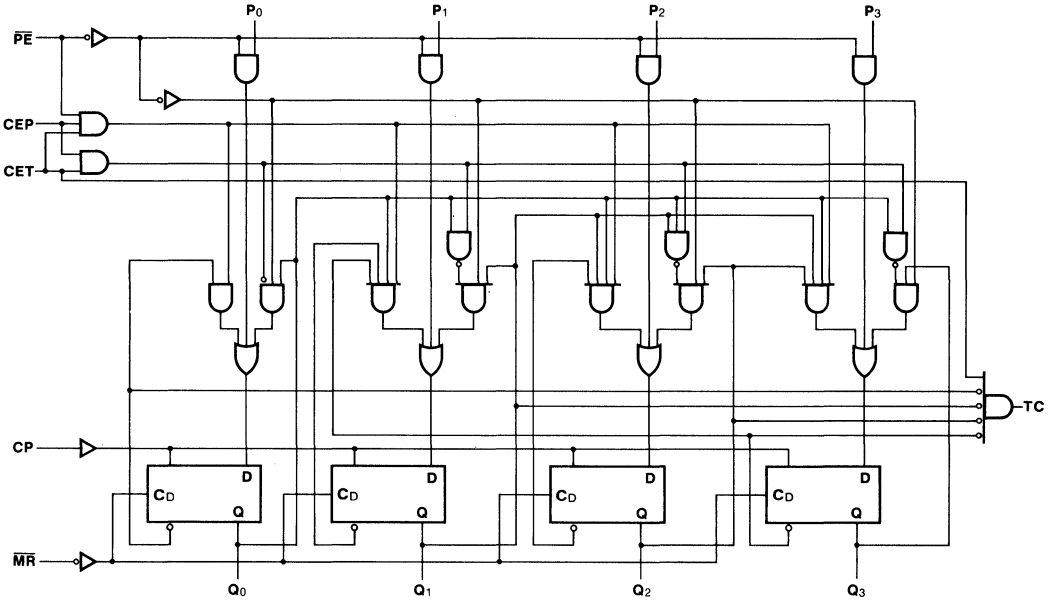


'162

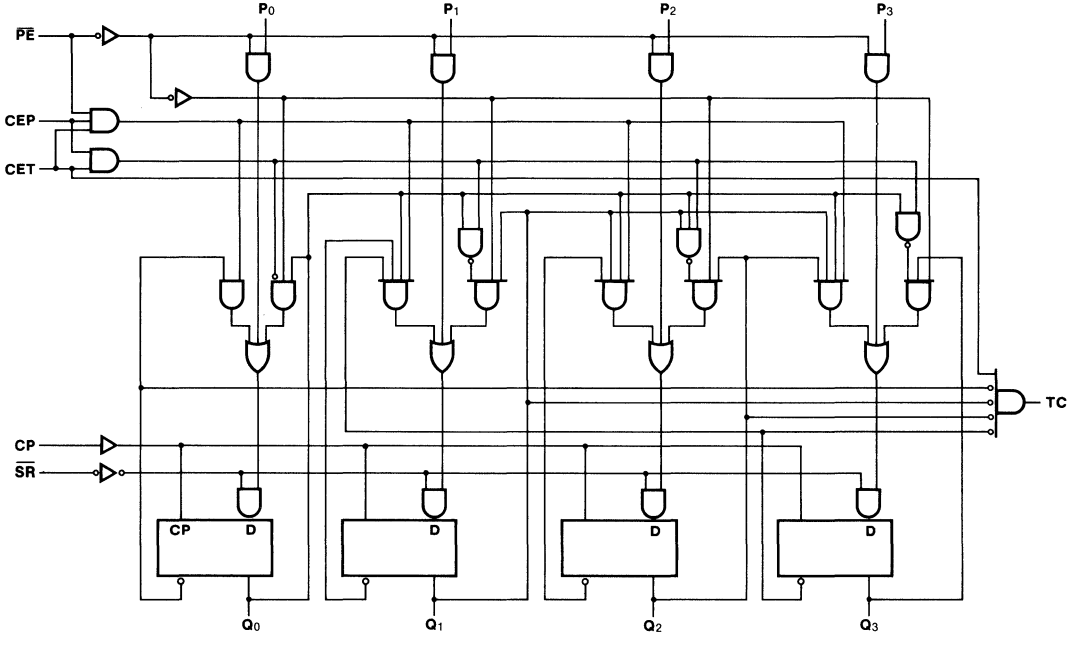


LOGIC DIAGRAMS

'LS160



'LS162



FUNCTIONAL DESCRIPTION — The '160 and '162 count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The '161 and '163 count modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the '160 and '161) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('160 and '161), synchronous reset ('162 and '163), parallel load, count-up and hold. Five control inputs — Master Reset ($\overline{MR}$, '160 and '161), Synchronous Reset ($\overline{SR}$, '162 and '163), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('160, '161) or $\overline{SR}$ ('162, '163) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The TTL versions ('160 — '163, as opposed to the 'LS160 — 'LS163) contain master/slave flip-flops which are "next-state catching" because of the JK feedback. This means that when CP is LOW, information that would change the state of a flip-flop, whether from the counting logic or the parallel entry logic if either mode is momentarily enabled, enters the master and is locked in. Thus to avoid inadvertently changing the state of a master latch, and the subsequent transfer of the erroneous information to the slave when the clock rises, it is necessary to insure that neither the counting mode, the synchronous reset mode, nor the parallel entry mode is momentarily enabled while CP is LOW.

The LS-TTL versions ('LS160 — 'LS163) use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in its maximum count state (9 for the decade counters, 15 for the binary counters). To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. These two schemes are shown in the 9310 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the LS-TTL versions ('LS160, 'LS162) of the decade counters, the TC output is fully decoded and can only be HIGH in state 9. In the TTL versions ('160, '162), however, the TC output can also be HIGH in the illegal states 11, 13 and 15. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the state diagrams.

LOGIC EQUATIONS: Count Enable = CEP • CET • PE

('160, '162) $TC = Q_0 \cdot Q_3 \cdot CET$

('LS160, 'LS162) $TC = Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3 \cdot CET$

('161, 'LS161, '163, 'LS163) $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CET$

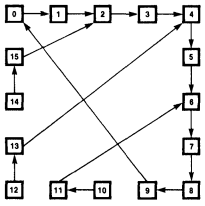
MODE SELECT TABLE

*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐¬)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

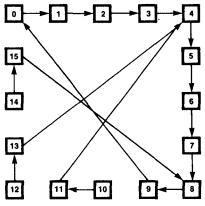
*For the '162 and '163 only.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

STATE DIAGRAMS

'160, '162



'LS160, 'LS162



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CCH}	Power Supply Current Outputs HIGH	XM		85		31	mA	V_{CC} = Max, $\overline{PE}$ = Gnd Other Inputs = 4.5 V CP = ⎍
		XC		94		31		
I_{CCL}	Power Supply Current Outputs LOW	XM		91		32	mA	V_{CC} = Max All Inputs = Gnd CP = ⎍
		XC		101		32		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
f_{max}	Maximum Count Frequency	25		25		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to TC		35 35		25 21	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagtion Delay CP to Q_n		20 23		24 27	ns	Figs. 3-1, 3-8 $\overline{PE}$ = 4.5 V
t_{PLH} t_{PHL}	Propagtion Delay CP to Q_n		25 29		24 27	ns	Figs. 3-1, 3-8 $\overline{PE}$ = Gnd
t_{PLH} t_{PHL}	Propagation Delay CET to TC		16 16		14 23	ns	Figs. 3-1, 3-5
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('160 and '161)		38		28	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW P_n to CP	20 20		20 20		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time, HIGH or LOW P_n to CP	0 0		5.0 5.0		ns	
t_s (H) t_s (L)	Setup Time, HIGH or LOW $\overline{PE}$ to CP	25 25		25 25		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{PE}$ to CP	0 0		0 0		ns	
t_s (H) t_s (L)	Setup Time, HIGH or LOW CEP, CET or $\overline{SR}$ to CP	20 20		25 25		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time, HIGH or LOW CEP, CET or $\overline{SR}$ to CP	0 0		0 0		ns	
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	15 25		15 25		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW ('160 and '161)	20		15		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP ('160 and '161)			20		ns	Fig. 3-16

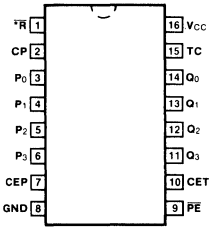
54/74161 • 54LS/74LS161
54/74163 • 54LS/74LS163

SYNCHRONOUS PRESETTABLE BINARY COUNTERS

DESCRIPTION — The '161 and '163 are high speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The '161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The '163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock. For functional description and detail specifications please refer to the '160 data sheet. For S-TTL and LP-TTL versions please see the 9316 data sheet.

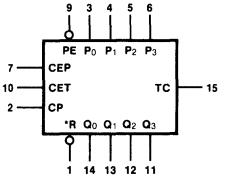
- **SYNCHRONOUS COUNTING AND LOADING**
- **HIGH SPEED SYNCHRONOUS EXPANSION**
- **LS VERSIONS FULLY EDGE TRIGGERED**

CONNECTION DIAGRAM
PINOUT A



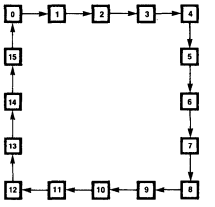
*$\overline{MR}$ for '161
*$\overline{SR}$ for '163

LOGIC SYMBOL



*$\overline{MR}$ for '161 V_{CC} = Pin 16
*$\overline{SR}$ for '163 Gnd = Pin 8

STATE DIAGRAM



ORDERING CODE: See Section 9

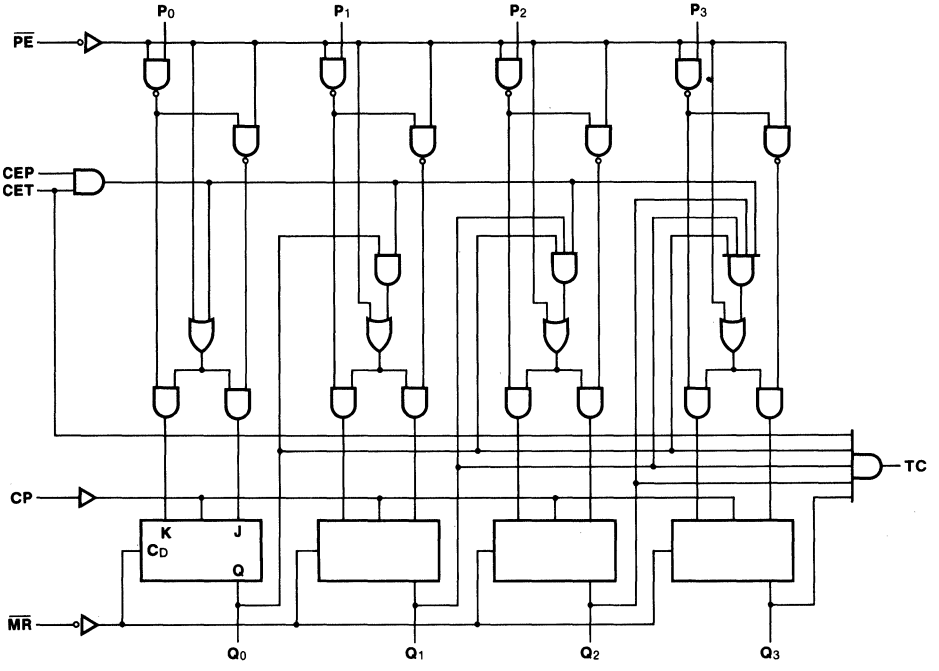
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74161PC, 74LS161PC 74163PC, 74LS163PC		9B
Ceramic DIP (D)	A	74161DC, 74LS161DC 74163DC, 74LS163DC	54161DM, 54LS161DM 54163DM, 54LS163DM	7B
Flatpak (F)	A	74161FC, 74LS161FC 74163FC, 74LS163FC	54161FM, 54LS161FM 54163FM, 54LS163FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

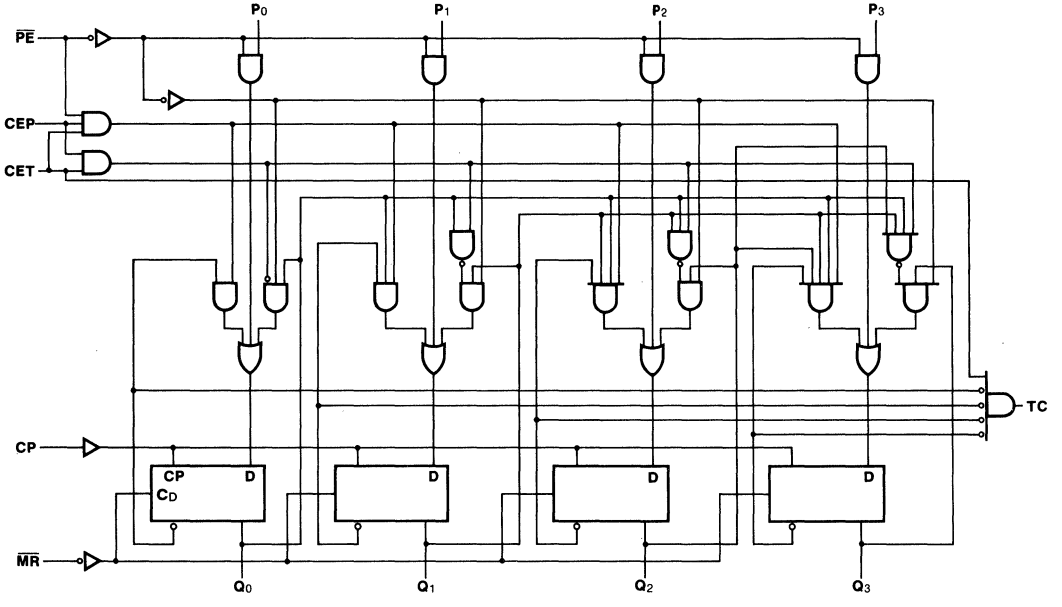
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
CEP	Count Enable Parallel Input	1.0/1.0	0.6/0.3
CET	Count Enable Trickle Input	2.0/2.0	1.0/0.5
CP	Clock Pulse Input (Active Rising Edge)	2.0/2.0	0.6/0.3
$\overline{MR}$ ('161)	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{SR}$ ('163)	Synchronous Reset Input (Active LOW)	1.0/1.0	0.5/0.25
P_0 — P_3	Parallel Data Inputs	1.0/1.0	0.5/0.25
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0	0.6/0.3
Q_0 — Q_3	Flip-flop Outputs	20/10	10/5.0 (2.5)
TC	Terminal Count Output	20/10	10/5.0 (2.5)

LOGIC DIAGRAMS

'161

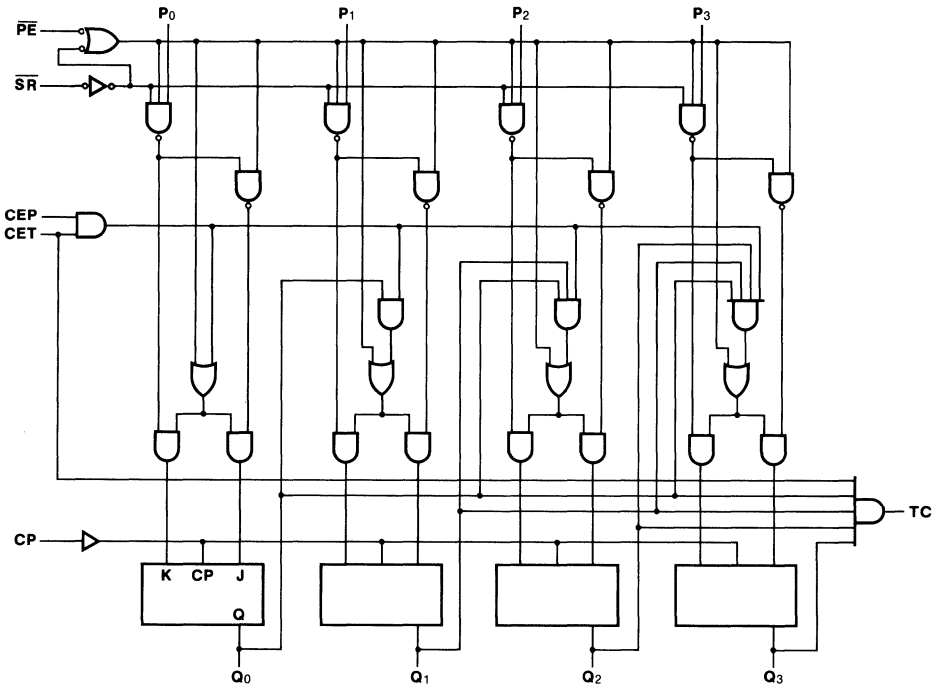


'LS161

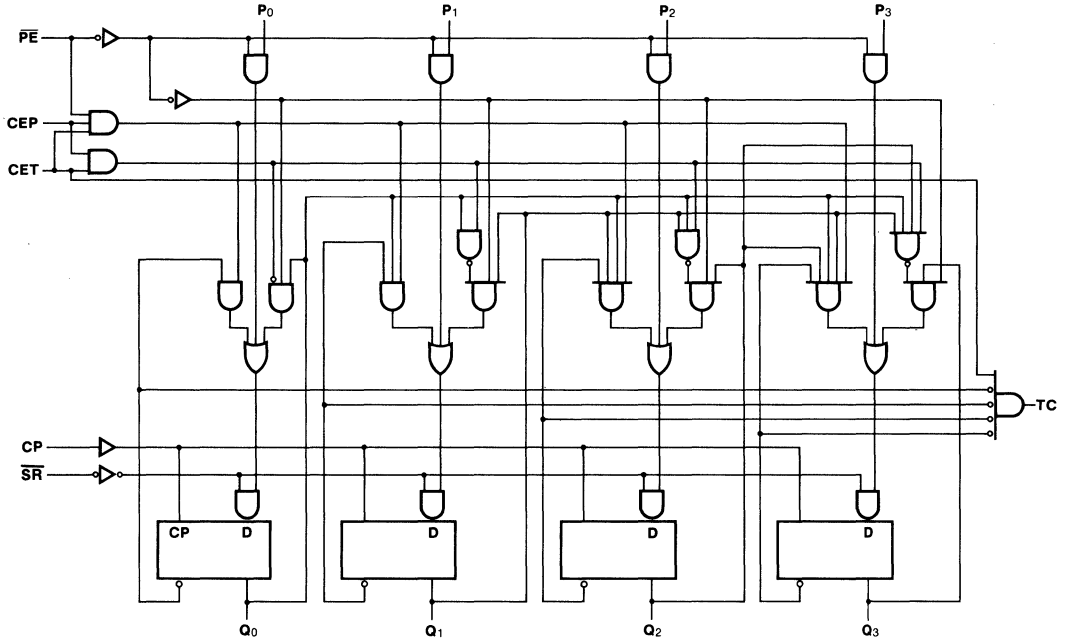


LOGIC DIAGRAMS

'163



'LS163

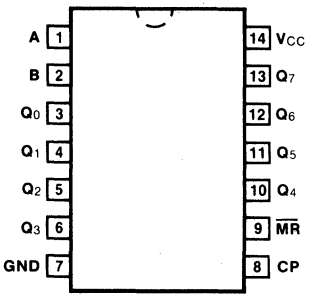


54/74164
54LS/74LS164
SERIAL-IN PARALLEL-OUT SHIFT REGISTER

DESCRIPTION — The '164 is a high speed 8-bit serial-in parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds.

- **TYPICAL SHIFT FREQUENCY OF 35 MHz**
- **ASYNCHRONOUS MASTER RESET**
- **GATED SERIAL DATA INPUT**
- **FULLY SYNCHRONOUS DATA TRANSFERS**

CONNECTION DIAGRAM
PINOUT A



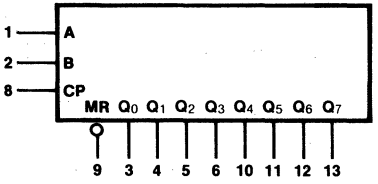
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74164PC, 74LS164PC		9A
Ceramic DIP (D)	A	74164DC, 74LS164DC	54164DM, 54LS164DM	6A
Flatpak (F)	A	74164FC, 74LS164FC	54164FM, 54LS164FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
A, B	Data Inputs	1.0/1.0	0.5/0.25
$\overline{CP}$	Clock Pulse Input (Active Rising Edge)	1.0/1.0	0.5/0.25
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0	0.5/0.25
$Q_0 - Q_7$	Outputs	10/5.0	10/5.0 (2.5)

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

FUNCTIONAL DESCRIPTION — The '164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

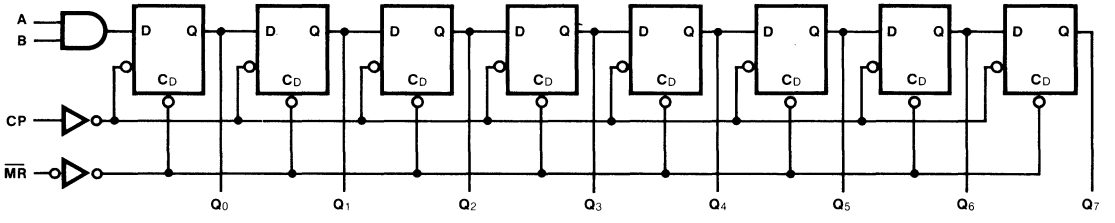
Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs (A • B) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

MODE SELECT TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	A	B	Q_0	$Q_1 - Q_7$
Reset (Clear)	L	X	X	L	L — L
Shift	H	l	l	L	$q_0 - q_6$
	H	l	h	L	$q_0 - q_6$
	H	h	l	L	$q_0 - q_6$
	H	h	h	H	$q_0 - q_6$

L (l) = LOW Voltage Levels
H (h) = HIGH Voltage Levels
X = Immaterial
q_n = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMTER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	XM	-10	-27.5	-20	-100	mA	V_{CC} = Max
		XC	-9.0	-27.5	-20	-100		
I_{CC}	Power Supply Current			54		27	mA	A, B = Gnd, V_{CC} = Max CP = 2.4 V, $\overline{MR}$ = ⌐¯¯

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 800 Ω Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	25		25		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		27 32		27 32	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		30 37			ns	Figs. 3-1, 3-8 C_L = 50 pF
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		36		36	ns	Figs. 3-1, 3-16
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		42			ns	Figs. 3-1, 3-16 C_L = 50 pF

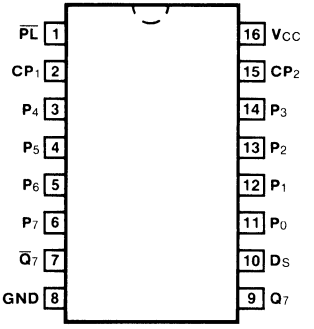
AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW A or B to CP	15 15		15 15		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW A or B to CP	0 0		5.0 5.0		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	20 20		20 20		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		20		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP			20		ns	Fig. 3-16

54/74165
54LS/74LS165
8-BIT PARALLEL-TO-SERIAL CONVERTER

DESCRIPTION — The '165 is an 8-bit parallel load or serial-in register with complementary outputs available from the last stage. Parallel inputing occurs asynchronously when the Parallel Load ($\overline{PL}$) input is LOW. With $\overline{PL}$ HIGH, serial shifting occurs on the rising edge of the clock; new data enters via the Serial Data (D_S) input. The 2-input OR clock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

CONNECTION DIAGRAM
PINOUT A



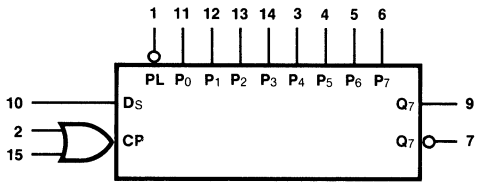
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74165PC, 74LS165PC		9B
Ceramic DIP (D)	A	74165DC, 74LS165DC	54165DM, 54LS165DM	6B
Flatpak (F)	A	74165FC, 74LS165FC	54165FM, 54LS165FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0	0.5/0.25
D_S	Serial Data Input	1.0/1.0	0.5/0.25
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	2.0/2.0	1.5/0.75
P_0 — P_7	Parallel Data Inputs	1.0/1.0	0.5/0.25
Q_7	Serial Output From Last Stage	20/10	10/5.0 (2.5)
$\overline{Q}_7$	Complementary Output	20/10	10/5.0 (2.5)

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '165 contains eight clocked master/slave RS flip-flops connected as a shift register with auxiliary gating to provide overriding asynchronous parallel entry. Parallel data enters when the $\overline{PL}$ signal is LOW. The parallel data can change while $\overline{PL}$ is LOW provided that the recommended setup and hold times are observed.

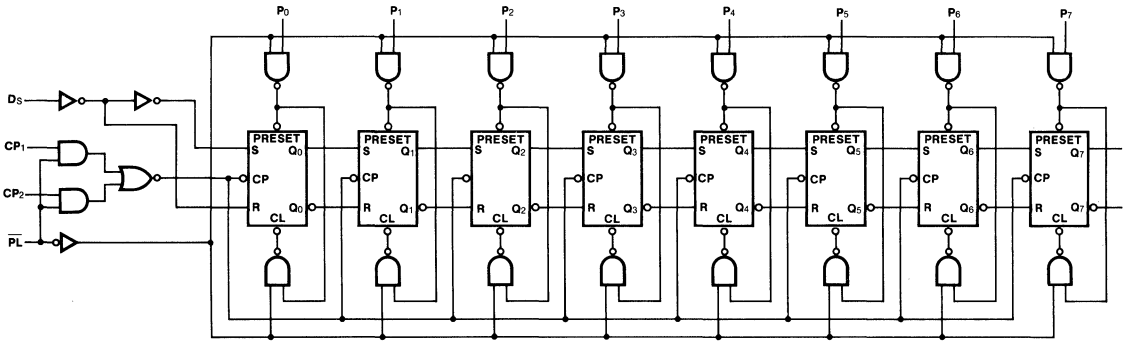
For clocked operation, $\overline{PL}$ must be HIGH. The two clock inputs perform identically; one can be used as a clock inhibit by applying a HIGH signal. To avoid double clocking, however, the inhibit signal should only go HIGH while the clock is HIGH. Otherwise, the rising inhibit signal will cause the same response as a rising clock edge. The flip-flops are edge-triggered for serial operations. The serial input data can change at any time, provided only that the recommended setup and hold times are observed, with respect to the rising edge of the clock.

TRUTH TABLE

	CP		CONTENTS								RESPONSE
$\overline{PL}$	1	2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	X	X	P_0	P_1	P_2	P_3	P_4	P_5	P_6	P_7	Parallel Entry
H	L	↑	D_S	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Right Shift
H	H	↑	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	No Change
H	↑	L	D_S	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Right Shift
H	↑	H	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	XM	-20	-55			mA	V_{CC} = Max
		XC	-18	-55				
I_{CC}	Power Supply Current			63		36	mA	V_{CC} = Max, $\overline{PL}$ = ⌐⌐ P_n = ⌊ CP_1, CP_2 = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	20		30		MHz	Figs. 3-1, 3-8
t_{PLH}	Propagation Delay		31		30	ns	Figs. 3-1, 3-16
t_{PHL}	$\overline{PL}$ to Q_7 or $\overline{Q}_7$		40		30		
t_{PLH}	Propagation Delay		24		30	ns	Figs. 3-1, 3-8
t_{PHL}	CP_1 to Q_7 or $\overline{Q}_7$		31		30		
t_{PLH}	Propagation Delay		17		25	ns	Figs. 3-1, 3-5
t_{PHL}	P_7 to Q_7		36		30		
t_{PLH}	Propagation Delay		27		30	ns	Figs. 3-1, 3-4
t_{PHL}	P_7 to $\overline{Q}_7$		27		25		

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H)	Setup Time HIGH or LOW	10		10		ns	Fig. 3-13
t_s (L)	P_n to $\overline{PL}$	10		10			
t_h (H)	Hold Time HIGH or LOW	0		5.0		ns	
t_h (L)	P_n to $\overline{PL}$	0		5.0			
t_s (H)	Setup Time HIGH or LOW	20		10		ns	Fig. 3-6
t_s (L)	D_S to CP_n	20		10			
t_h (H)	Hold Time HIGH or LOW	0		5.0		ns	
t_h (L)	D_S to CP_n	0		5.0			
t_s (H)	Setup Time HIGH CP_1 to CP_2 or CP_2 to CP_1	30		30		ns	
t_w (H)	CP_n Pulse Width HIGH	25		20		ns	Fig. 3-8
t_w (L)	$\overline{PL}$ Pulse Width LOW	15		15		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{PL}$ to CP_n	45		15		ns	

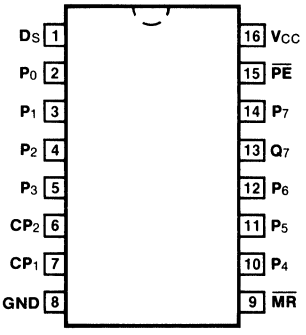
54/74166

8-BIT SHIFT REGISTER

DESCRIPTION — The '166 is an 8-bit, serial- or parallel-in, serial-out shift register using edge triggered D-type flip-flops. Serial and parallel entry are synchronous, with state changes initiated by the rising edge of the clock. An asynchronous Master Reset overrides other inputs and clears all flip-flops. The circuit can be clocked from two sources or one CP input can be used to trigger the other.

- **35 MHz TYPICAL SHIFT FREQUENCY**
- **ASYNCHRONOUS MASTER RESET**
- **SYNCHRONOUS PARALLEL ENTRY**
- **GATED CLOCK INPUT CIRCUITRY**

CONNECTION DIAGRAM
PINOUT A



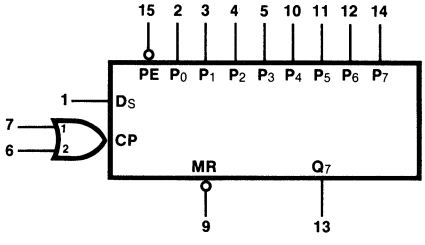
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74166PC		9B
Ceramic DIP (D)	A	74166DC	54166DM	7B
Flatpak (F)	A	74166FC	54166FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0
D_S	Serial Data Input	1.0/1.0
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0
P_0 — P_7	Parallel Data Inputs	1.0/1.0
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0
Q_7	Last Stage Output	20/10

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

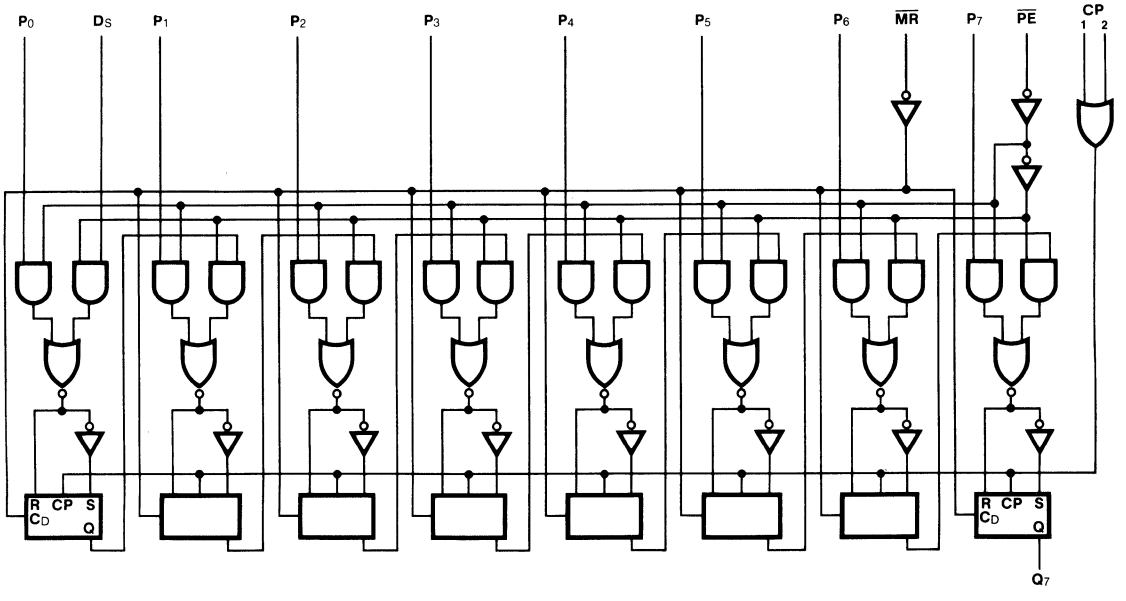
FUNCTIONAL DESCRIPTION — Operation is synchronous (except for Master Reset) and state changes are initiated by the rising edge of either clock input if the other clock input is LOW. When one of the clock inputs is used as an active HIGH clock inhibit, it should attain the HIGH state while the other clock is still in the HIGH state following the previous operation. When the Parallel Enable ($\overline{PE}$) input is LOW, data is loaded into the register from the Parallel Data ($P_0 - P_7$) inputs on the next rising edge of the clock. When $\overline{PE}$ is HIGH, information is shifted from the Serial Data (D_S) input to Q_0 and all data in the register is shifted one bit position (i.e., $Q_0 \rightarrow Q_1$, $Q_1 \rightarrow Q_2$, etc.) on the rising edge of the clock.

MODE SELECT TABLE

INPUTS				RESPONSE
$\overline{MR}$	$\overline{PE}$	CP_1	CP_2	
L	X	X	X	Asynchronous Reset; Q_n = LOW
H H	X X	H* X	X H*	Hold
H H	L L	L ↑	↑ L	Parallel Load; $P_n \rightarrow Q_n$
H H	H H	L ↑	↑ L	Shift; $D_S \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.

*The HIGH signal on one CP input must be established while the other CP input is HIGH.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current		127	mA	V_{CC} = Max, CP_1 = ⎍⎍ D_S = 4.5 V CP_2, $\overline{MR}$, $\overline{PE}$, P_n = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 C_L = 15 pF, R_L = 400 Ω Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	25		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_7		26 30	ns	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_7		35	ns	Figs. 3-1, 3-16

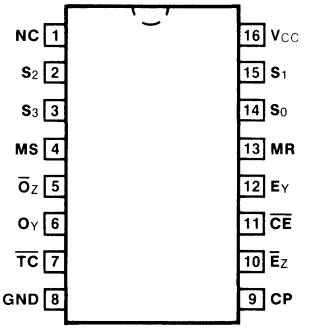
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW D_S or P_n to CP_n	20 20		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D_S or P_n to CP_n	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{PE}$ to CP_n	30 30		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{PE}$ to CP_n	0 0		ns	
t_w (H)	CP_n Pulse Width HIGH	20		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		ns	Fig. 3-16

54/74167

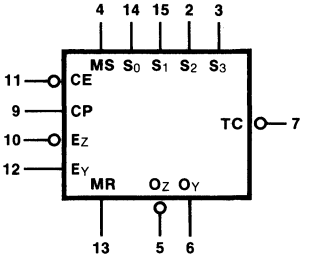
SYNCHRONOUS DECADE RATE MULTIPLIER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '167 contains a synchronous decade counter and four decoding gates that serve to gate the clock through to the output at a sub-multiple of the clock frequency. The output pulse rate, relative to the clock frequency, is determined by signals applied to the Select (S_0 — S_3) inputs. Both true and complement outputs are available, along with an enable input for each. A Count Enable input and a Terminal Count output are provided for cascading two or more packages. Asynchronous Master Reset and Master Set inputs prevent counting and clear the counter or set it to maximum, respectively.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

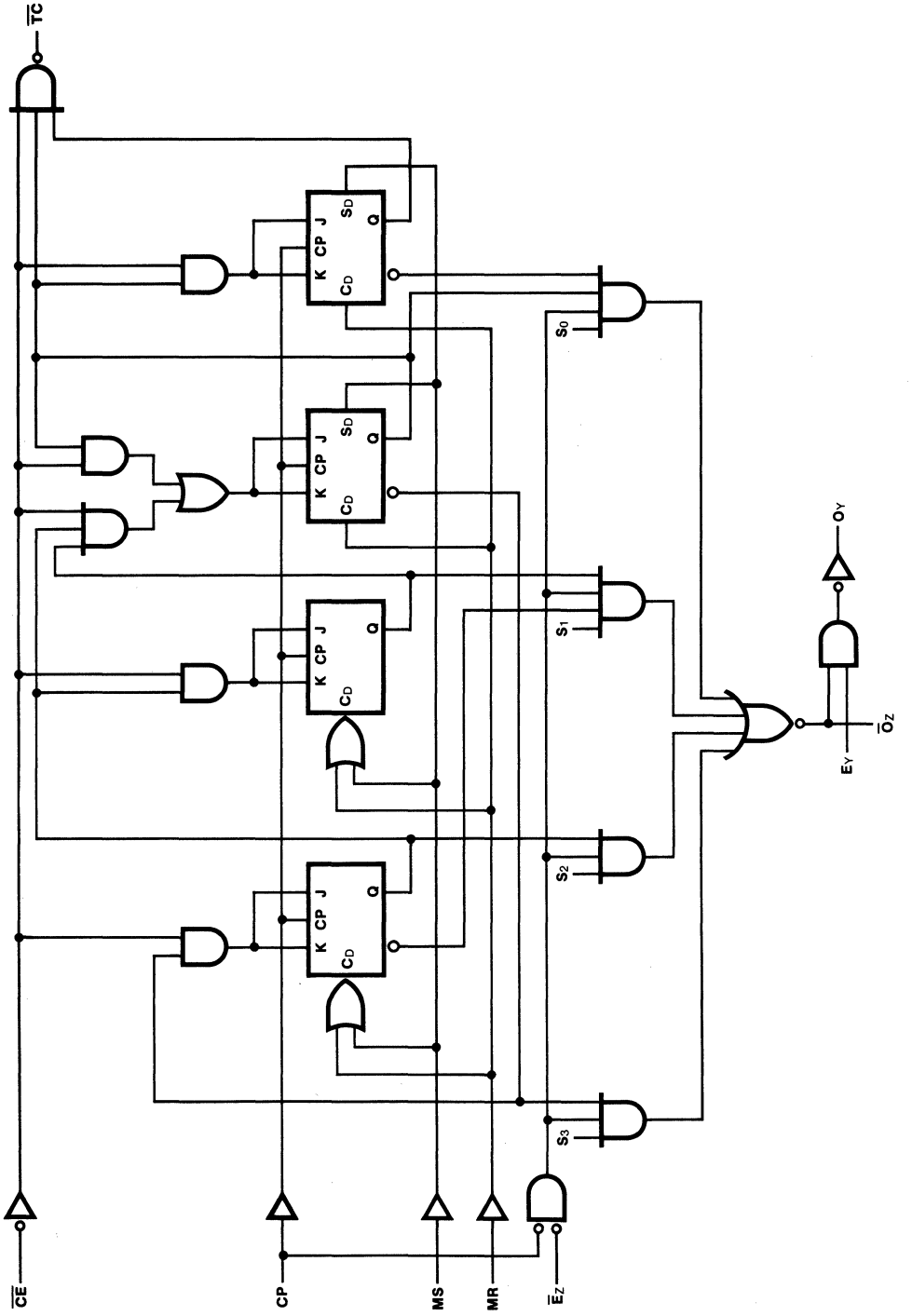
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74167PC		9B
Ceramic DIP (D)	A	74167DC	54167DM	7B
Flatpak (F)	A	74167FC	54167FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\underline{S_0}$ — $\underline{S_3}$	Rate Select Inputs	1.0/1.0
$\overline{E_Z}$	$\overline{O_Z}$ Enable Input (Active LOW)	1.0/1.0
$\underline{E_Y}$	O_Y Enable Input	1.0/1.0
$\overline{CE}$	Count Enable Input (Active LOW)	1.0/1.0
CP	Clock Pulse Input (Active Rising Edge)	2.0/2.0
MS	Asynchronous Master Set Input (Active HIGH) (Set to 9)	1.0/1.0
MR	Asynchronous Master Reset Input (Active HIGH)	1.0/1.0
$\overline{O_Z}$	Gated Clock Output (Active LOW)	10/10
$\underline{O_Y}$	Complement Output (Active HIGH)	10/10
$\overline{TC}$	Terminal Count Output (Active LOW)	10/10

LOGIC DIAGRAM



TRUTH TABLE

INPUTS									OUTPUTS			
MR	$\overline{CE}$	$\overline{E}_Z$	S_3	S_2	S_1	S_0	CLOCK PULSES	E_Y	O_Y	$\overline{O}_Z$	$\overline{TC}$	NOTES
H	X	H	X	X	X	X	X	H	L	H	H	1
L	L	L	L	L	L	L	10	H	L	H	1	2
L	L	L	L	L	L	H	10	H	1	1	1	2
L	L	L	L	L	H	L	10	H	2	2	1	2
L	L	L	L	L	H	H	10	H	3	3	1	2
L	L	L	L	H	L	L	10	H	4	4	1	2
L	L	L	L	H	L	H	10	H	5	5	1	2
L	L	L	L	H	H	L	10	H	6	6	1	2
L	L	L	L	H	H	H	10	H	7	7	1	2
L	L	L	H	L	L	L	10	H	8	8	1	2
L	L	L	H	L	L	H	10	H	9	9	1	2
L	L	L	H	L	H	L	10	H	8	8	1	2, 3
L	L	L	H	L	H	H	10	H	9	9	1	2, 3
L	L	L	H	H	L	L	10	H	8	8	1	2, 3
L	L	L	H	H	L	H	10	H	9	9	1	2, 3
L	L	L	H	H	H	L	10	H	8	8	1	2, 3
L	L	L	H	H	H	H	10	H	9	9	1	2, 3
L	L	L	H	L	L	H	10	L	H	9	1	4

1. This is a simplified illustration of the clear function. CP and $\overline{E}_Z$ also affect the logic level of O_Y and $\overline{O}_Z$. A LOW signal on E_Y will cause O_Y to remain HIGH.
2. Each rate illustrated assumes $S_0 - S_3$ are constant throughtout the cycle; however, these illustrations in no way prohibit variable-rate operation.
3. These input condtions exceed the range of the decade rate Select inputs.
4. E_Y can be used to inhibit output O_Y.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

PULSE PATTERN TABLE

S_3	S_2	S_1	S_0	m	$\overline{O}_Z$ PULSE PATTERN
L	L	L	H	1	1 1 1 1 0 1 1 1 1 1
L	L	H	L	2	1 1 0 1 1 1 1 0 1 1
L	L	H	H	3	1 1 0 1 0 1 1 0 1 1
L	H	L	L	4	1 0 1 0 1 1 0 1 0 1
L	H	L	H	5	1 0 1 0 0 1 0 1 0 1
L	H	H	L	6	1 0 0 0 1 1 0 0 0 1
L	H	H	H	7	1 0 0 0 0 1 0 0 0 1
H	L	L	L	8	0 0 0 0 1 0 0 0 0 1
H	L	L	H	9	0 0 0 0 0 0 0 0 0 1

H = HIGH Voltage Level
L = LOW Voltage Level

FUNCTIONAL DESCRIPTION — The '167 contains four JK flip-flops connected as a synchronous decade counter with a count sequence of 0-1-2-3-4-8-9-10-11-12. A LOW signal on the Count Enable ($\overline{CE}$) input permits counting, with all state changes initiated simultaneously by the rising edge of the clock. When the count reaches maximum (12) the Terminal Count ($\overline{TC}$) output goes LOW if $\overline{CE}$ is LOW. A HIGH signal on Master Reset ($\overline{MR}$) clears the flip-flops and prevents counting, although output pulses can still occur if the clock is running, $\overline{E}_Z$ is LOW and S_3 is HIGH. A HIGH signal on Master Set (MS) prevents counting and sets the counter to 12, the only state in which no output pulses can occur.

The flip-flop outputs are decoded by a 4-wide AND-OR-INVERT gate. Each AND gate also contains the buffered and inverted CP and Z-enable ($\overline{E}_Z$) functions, as well as one of the Select ($S_0 - S_3$) inputs. The Z output $\overline{O}_Z$ is normally HIGH and goes LOW when CP and $\overline{E}_Z$ are LOW and any of the AND gates has its other inputs HIGH. The AND gates are enabled at different times and different rates relative to the clock. For example, the gate to which S_0 is connected is enabled only when the counter is in state five, assuming that S_0 is HIGH. Thus, during one complete cycle of the counter (10 clocks) the S_0 gate can contribute only pulse to the output rate. The S_1 gate is enabled twice per cycle, the S_2 gate four times per cycle (etc.). The output pulse rate thus depends on the clock rate and which of the $S_0 - S_3$ inputs are HIGH, as expressed in the following formula.

$$f_{out} = \frac{m}{10} \bullet f_{in}$$

$$\text{where } m = S_3 \bullet 2^3 + S_2 \bullet 2^2 + S_1 \bullet 2^1 + S_0 \bullet 2^0$$

Thus by appropriate choice of signals applied to the $S_0 - S_3$ inputs, the output pulse rate can range from 1/10 to 9/10 of the clock rate. The select codes, m values and $\overline{O}_Z$ pulse pattern are shown in the Pulse Pattern Table. In the $\overline{O}_Z$ pattern, each column represents a clock period, with the state-12 column on the right. A one indicates that the $\overline{O}_Z$ output will be HIGH during that entire clock period, while a zero indicates that $\overline{O}_Z$ will be LOW when the clock is LOW during that period. Note that the output pulses are evenly spaced only when m is one or two, assuming that the clock frequency is constant, and that no output pulses can occur in state 12 of the counter.

The Y output O_Y is the complement of $\overline{O}_Z$ and is thus normally LOW. A LOW signal on the Y-enable input E_Y disables O_Y. To expand the multiplier to 2-digit rate select, two packages can be cascaded as shown in *Figure a*. Both circuits operate from the basic clock, with the $\overline{TC}$ output of the first acting to enable both counting and the output pulses of the second package. Thus the second counter advances at only 1/10 the rate of the first and a full cycle of the two counters combined requires 100 clocks. Output pulses contributed by the second counter occur only when the first counter is in state 12. All output pulses are opposite in phase to the clock.

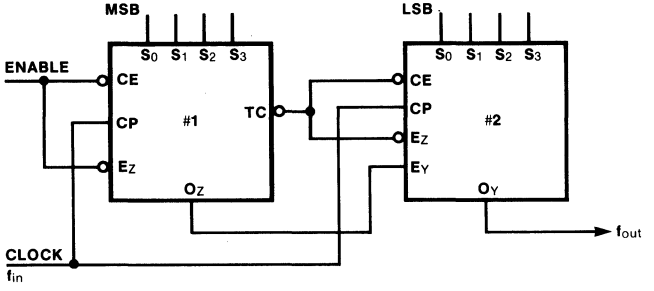


Fig. a Cascading for 2-Digit Rate Select

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
I_{OS}	Output Short Circuit Current	-18	-55	mA	V_{CC} = Max
I_{CC}	Power Supply Current		99	mA	V_{CC} = Max; MS = Gnd Other Inputs = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	25		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$		30 33	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_Z$ to O_Y		30 33	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay E_Y to O_Y		14 10	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{O}_Z$		14 10	ns	
t_{PLH} t_{PHL}	Propagation Delay CP to O_Y		39 30	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_Z$ to $\overline{O}_Z$		18 23	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay S_n to O_Y		23 23	ns	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_Z$		18 26	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{TC}$		20 21	ns	
t_{PHL}	Propagation Delay MS to $\overline{TC}$		27	ns	Figs. 3-1, 3-16
t_{PLH}	Propagation Delay MR to O_Y		36	ns	
t_{PHL}	Propagation Delay MR TO $\overline{O}_Z$		23	ns	

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = 25° C

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
t_s (L)	Setup Time LOW $\overline{CE}$ to CP Rising	25		ns	Fig. b
t_h (H)	Hold Time HIGH $\overline{CE}$ to CP Rising	0	t_w CP-10	ns	
t_s (L)	Setup Time LOW $\overline{CE}$ to CP Falling	0	t_w CP-10	ns	Fig. c
t_h (L)	Hold Time LOW $\overline{CE}$ to CP Falling	20	T-10	ns	
t_{inh} (H)	Inhibit Time HIGH $\overline{CE}$ to CP Falling	10		ns	Fig. b
t_w (H)	CP Pulse Width HIGH	20		ns	Fig. 3-8
t_w (H)	MR Pulse Width HIGH	15		ns	Fig. 3-16
t_w (H)	MS Pulse Width HIGH	15		ns	

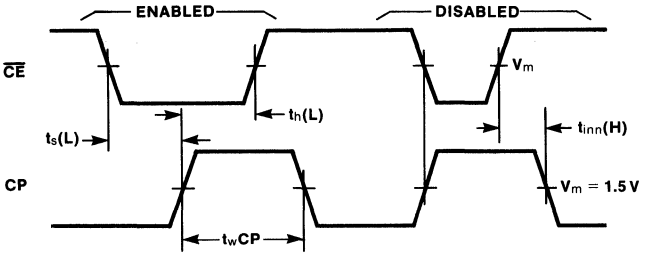


Fig. b

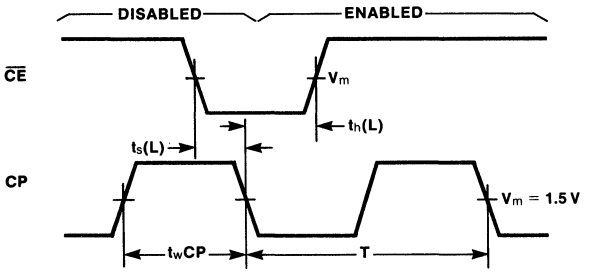
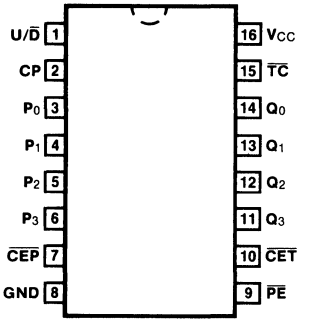


Fig. c

54LS/74LS168

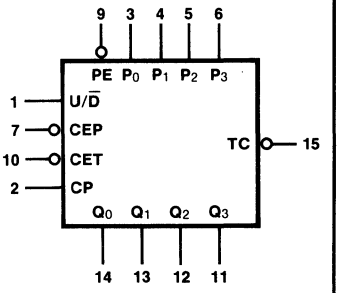
SYNCHRONOUS BI-DIRECTIONAL BCD DECADE COUNTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '168 is a fully synchronous 4-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. It counts in the BCD (8421) sequence and all state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	A	74LS168PC		9B
Ceramic DIP (D)	A	74LS168DC	54LS168DM	6B
Flatpak (F)	A	74LS168FC	54LS168FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	0.5/0.25
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	1.0/0.5
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$P_0 - P_3$	Parallel Data Inputs	0.5/0.25
$\overline{PE}$	Parallel Enable Input (Active LOW)	0.5/0.25
U/$\overline{D}$	Up-Down Count Control Input	0.5/0.25
$Q_0 - Q_3$	Flip-flop Outputs	10/5.0 (2.5)
$\overline{TC}$	Terminal Count Output (Active LOW)	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '168 and '169 use edge-triggered D-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the $P_0 - P_3$ inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH. The U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the COUNT DOWN mode or reaches 9 (15 for the '169) in the COUNT UP mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the '168 decade counter can also be LOW in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the '168 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

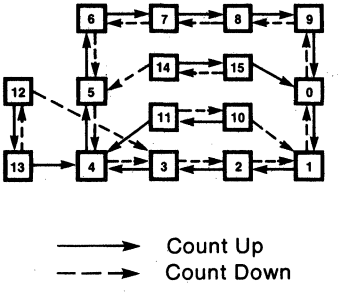
1) Count Enable = $\overline{CEP} \bullet \overline{CET} \bullet \overline{PE}$
2) Up: $\overline{TC} = Q_0 \bullet Q_3 \bullet (U/\overline{D}) \bullet \overline{CET}$
3) Down: $\overline{TC} = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet (U/\overline{D}) \bullet \overline{CET}$

'168 and '169 MODE SELECT TABLE

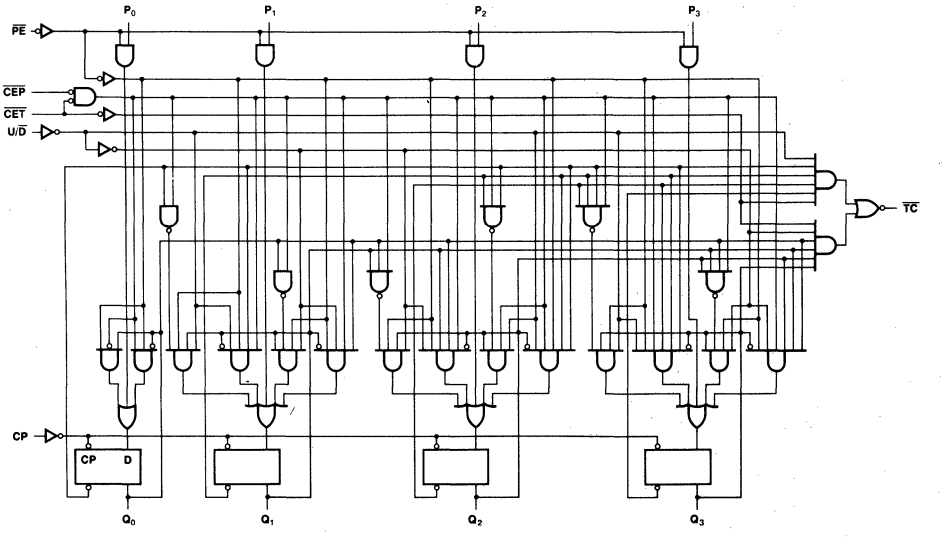
$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load ($P_n \rightarrow Q_n$)
H	L	L	H	Count Up (increment)
H	L	L	L	Count Down (decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

STATE DIAGRAM
54LS/74LS168



LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		34	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		C_L = 15 pF			
		Min	Max		
f_{max}	Maximum Clock Frequency	25		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		20 20	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$		30 30	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$		15 20	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$		25 25	ns	Figs. 3-1, 3-20

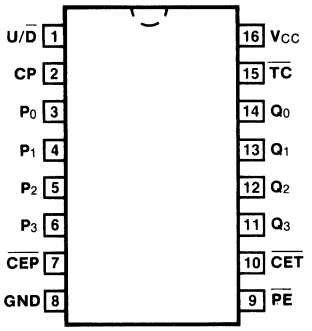
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n, $\overline{CEP}$ or $\overline{CET}$ to CP	15 15		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n, $\overline{CEP}$ or $\overline{CET}$ to CP	5.0 5.0		ns	Fig. 3-6
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{PE}$ to CP	20 20		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{PE}$ to CP	0 0		ns	Fig. 3-6
t_s (H) t_s (L)	Setup Time HIGH or LOW U/$\overline{D}$ to CP	25 25		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW U/$\overline{D}$ to CP	0 0		ns	Fig. 3-6
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	10 20		ns	Fig. 3-8

54LS/74LS169

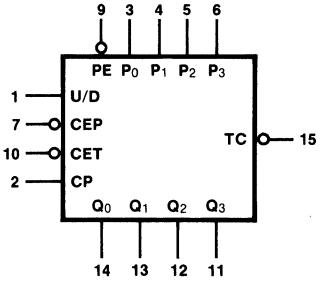
SYNCHRONOUS BI-DIRECTIONAL MODULO-16 BINARY COUNTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '169 is a fully synchronous 4-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock. For a functional description and detail specifications, please refer to the '168 data sheet.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

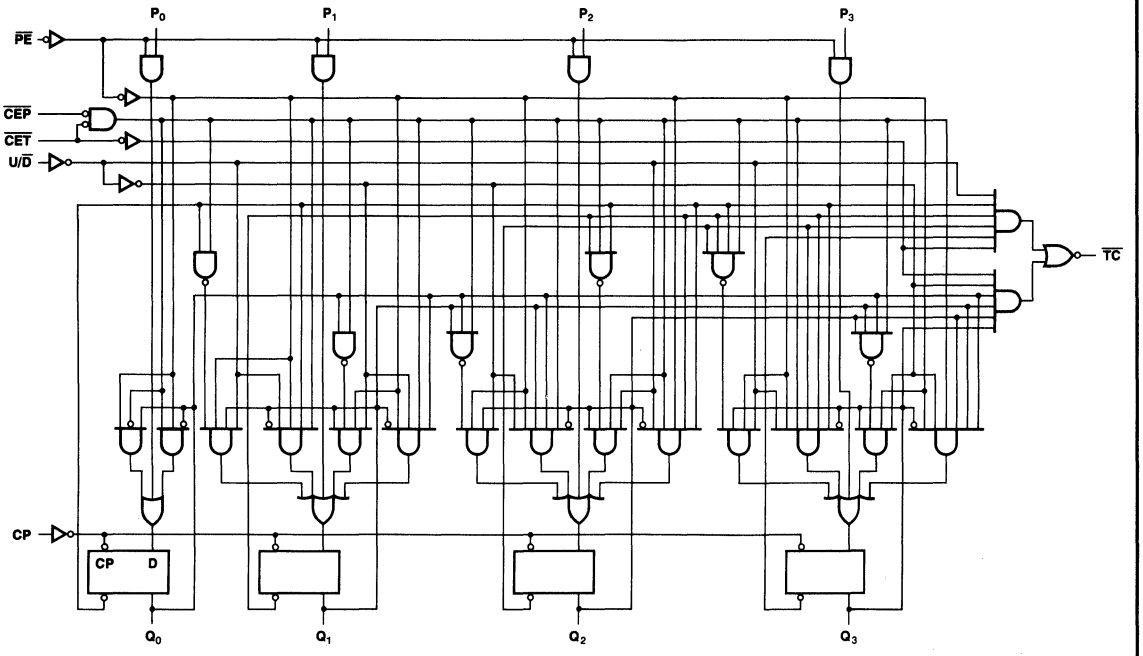
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS169PC		9B
Ceramic DIP (D)	A	74LS169DC	54LS169DM	6B
Flatpak (F)	A	74LS169FC	54LS169FM	4L

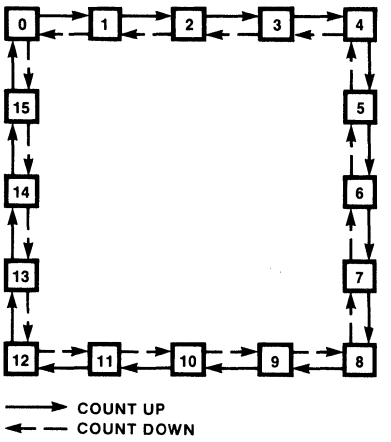
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	0.5/0.25
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	1.0/0.5
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$P_0 - P_3$	Parallel Data Inputs	0.5/0.25
$\overline{PE}$	Parallel Enable Input (Active LOW)	0.5/0.25
U/$\overline{D}$	Up-Down Count Control Input	0.5/0.25
$Q_0 - Q_3$	Flip-flop Outputs	10/5.0 (2.5)
$\overline{TC}$	Terminal Count Output (Active LOW)	10/5.0 (2.5)

LOGIC DIAGRAM



STATE DIAGRAM



MODE SELECT TABLE

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load ($P_n \rightarrow Q_n$)
H	L	L	H	Count Up (increment)
H	L	L	L	Count Down (decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

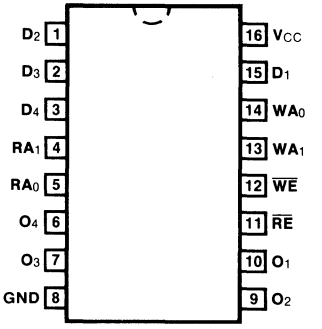
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

54/74170
54LS/74LS170

4 X 4 REGISTER FILE

(With Open-Collector Outputs)

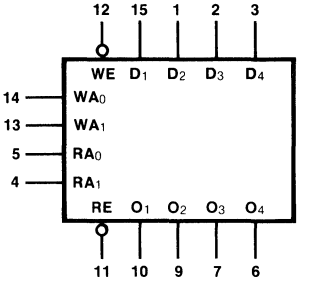
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '170 contains 16 high speed, low power, transparent D-type latches arranged as four words of four bits each, to function as a 4 X 4 register file. Separate read and write inputs, both address and enable, allow simultaneous read and write operation. Open-collector outputs make it possible to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length. The '670 provides a similar function to this device but it features 3-state outputs.

- **SIMULTANEOUS READ/WRITE OPERATION**
- **EXPANDABLE TO 512 WORDS OF n-BITS**
- **TYPICAL ACCESS TIME OF 20 ns**
- **LOW LEAKAGE OPEN-COLLECTOR OUTPUTS FOR EXPANSION**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

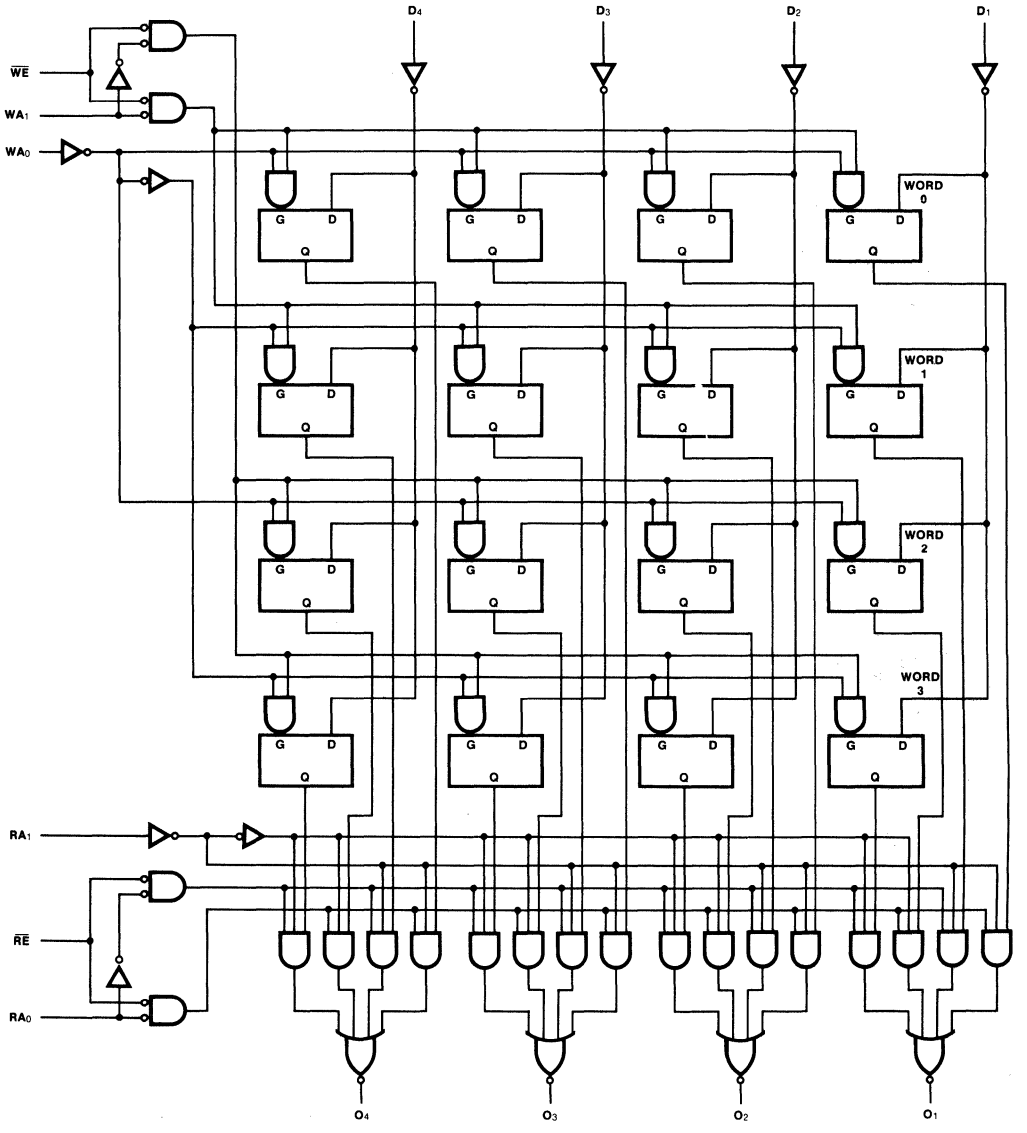
PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		VCC = +5.0 V ±5%, TA = 0° C to +70° C	VCC = +5.0 V ±10%, TA = -55° C to +125° C	
Plastic DIP (P)	A	74170PC, 74LS170PC		9B
Ceramic DIP (D)	A	74170DC, 74LS170DC	54170DM, 54LS170DM	7B
Flatpak (F)	A	74170FC, 74LS170FC	54170FM, 54LS170DM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$D_1 - D_4$	Data Inputs	1.0/1.0	0.5/0.25
WA_0, WA_1	Write Address Inputs	1.0/1.0	0.5/0.25
$\overline{WE}$	Write Enable Input (Active LOW)	1.0/1.0	1.0/0.5
RA_0, RA_1	Read Address Inputs	1.0/1.0	0.5/0.25
$\overline{RE}$	Read Enable Input (Active LOW)	1.0/1.0	1.0/0.5
$O_1 - O_4$	Data Outputs	OC*/10	OC*/5.0 (2.5)

*OC — Open Collector

LOGIC DIAGRAM



WRITE FUNCTION TABLE

WRITE INPUTS			D INPUTS TO
$\overline{WE}$	WA_1	WA_0	
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (hold)

READ FUNCTION TABLE

READ INPUTS			OUTPUTS FROM
$\overline{RE}$	RA_1	RA_0	
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (HIGH Z)

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OH}	Output HIGH Current			30		20	μA	V_{CC} = Min, V_{OH} = 5.5 V
I_{CC}	Power Supply Current	XC		150		40	mA	V_{CC} = Max; D_n, $\overline{WE}$, $\overline{RE}$ = 4.5 V; WA_n, RA_n = Gnd
		XM		140		40		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay* RA_0 or RA_1 to O_n		35 40		35 35	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{RE}$ to O_n		15 30		30 30	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{WE}$ to O_n		40 45		35 35	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n		30 45		35 35	ns	Figs. 3-1, 3-5

*Measured at least 25 ns after entry of new data at selected location.

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s	Setup Time HIGH or LOW D_n to rising $\overline{WE}$	10		10		ns	Fig. a
t_h	Hold Time HIGH or LOW D_n to rising $\overline{WE}$	15		5.0		ns	
t_s	Setup Time HIGH or LOW WA_n to falling $\overline{WE}$	15		10		ns	
t_h	Hold Time HIGH or LOW WA_n to rising $\overline{WE}$	5.0		5.0		ns	
t_w (L)	$\overline{WE}$ or $\overline{RE}$ Pulse Width LOW	25		25		ns	

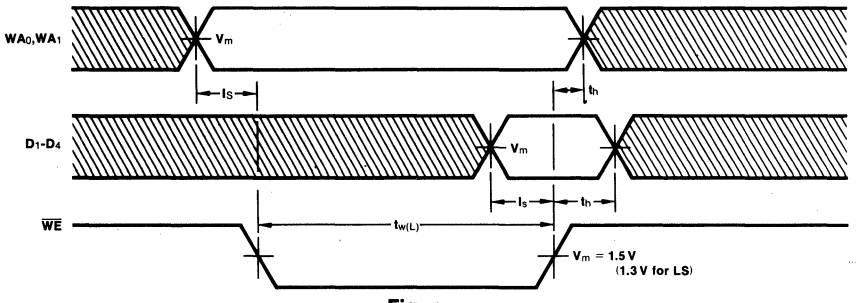


Fig. a

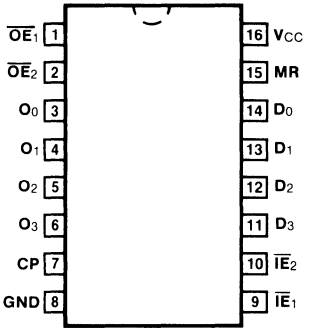
54/74173
54LS/74LS173

4-BIT D-TYPE REGISTER
(With 3-State Outputs)

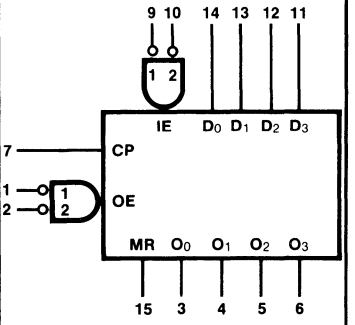
DESCRIPTION — The '173 is a high speed 4-bit register featuring 3-state outputs for use in bus-organized systems. The clock is fully edge-triggered allowing either a load from the D inputs or a hold (retain register contents) depending on the state of the Input Enable lines ($\overline{IE}_1$, $\overline{IE}_2$). A HIGH on either Output Enable line ($\overline{OE}_1$, $\overline{OE}_2$) brings the output to a high impedence state without affecting the actual register contents. A HIGH on the Master Reset (MR) input resets the register regardless of the state of the Clock (CP), the Output Enable ($\overline{OE}_1$, $\overline{OE}_2$) or the Input Enable ($\overline{IE}_1$, $\overline{IE}_2$) lines.

- **FULLY EDGE-TRIGGERED**
- **3-STATE OUTPUTS**
- **GATED INPUT AND OUTPUT ENABLES**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74173PC, 74LS173PC		9B
Ceramic DIP (D)	A	74173DC, 74LS173DC	54173DM, 54LS173DM	7B
Flatpak (F)	A	74173FC, 74LS173FC	54173FM, 54LS173FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$D_0 - D_3$	Data Inputs	1.0/1.0	0.5/0.25
$\overline{IE}_1$, $\overline{IE}_2$	Input Enable Inputs (Active LOW)	1.0/1.0	0.5/0.25
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)	1.0/1.0	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	0.5/0.25
MR	Asynchronous Master Reset Input (Active HIGH)	1.0/1.0	0.5/0.25
$O_0 - O_3$	3-State Outputs	130/10 (50)	65/5.0 (25)/(2.5)

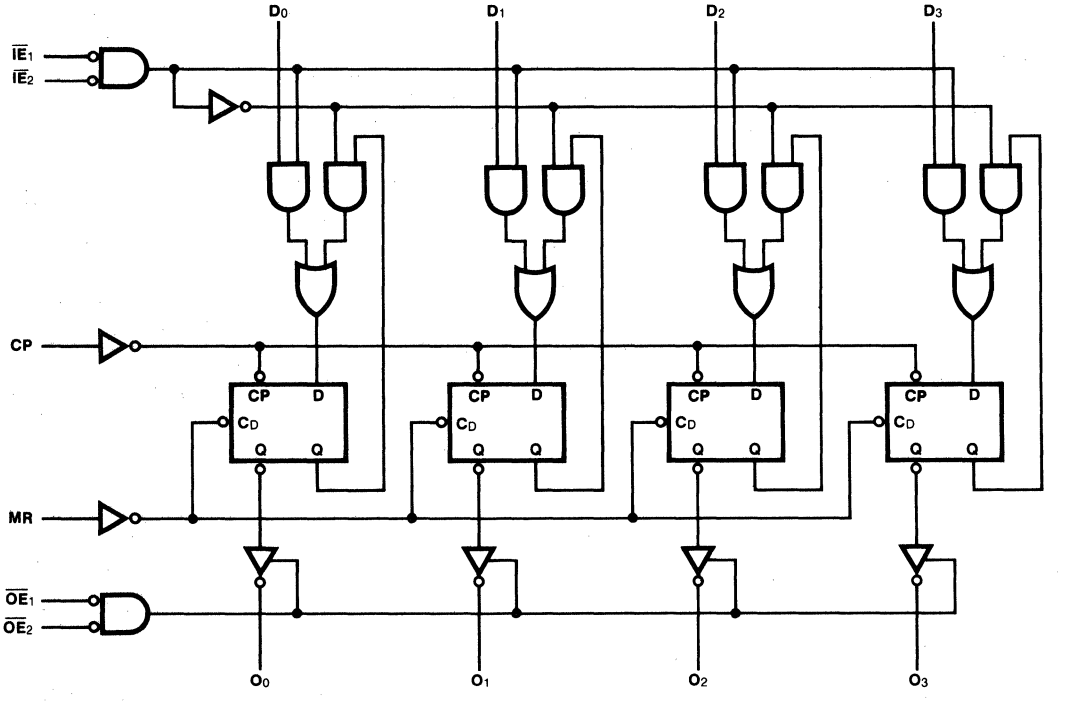
TRUTH TABLE

INPUTS					OUTPUT
MR	CP	$\overline{IE}_1$	$\overline{IE}_2$	D_n	Q_n
H	X	X	X	X	L
L	L	X	X	X	Q_n
L	⌐	H	X	X	Q_n
L	⌐	X	H	X	Q_n
L	⌐	L	L	L	L
L	⌐	L	L	H	H

When either $\overline{OE}_1$ or $\overline{OE}_2$ are HIGH, the output is in the OFF state (high impedenace); however this does not affect the contents or sequential operating of the register.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current	-30	-70	-20	-100	mA	V_{CC} = Max
I_{CC}	Power Supply Current		72		28	mA	V_{CC} = Max, MR = ⌜⌞ CP, $\overline{OE}_1$ = 4.5 V $\overline{OE}_2$, $\overline{IE}_1$, $\overline{IE}_2$, D_n = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

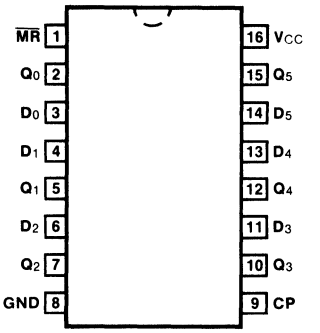
SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		C_L = 50 pF R_L = 400 Ω		C_L = 15 pF			
		Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	25		30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to O_n		43 31		40 25	ns	
t_{PHL}	Propagation Delay, MR to O_n		27		25	ns	Figs. 3-1, 3-16
t_{PZH} t_{PZL}	Output Enable Time		30 30		20 20	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS173)
t_{PHZ} t_{PLZ}	Output Disable Time		14 20		16 16	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS173) C_L = 5 pF

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to CP	10 10		10 10		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to CP	10 10		10 10		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{IE}$ to CP	17 17		17 17		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{IE}$ to CP	2.0 2.0		2.0 2.0		ns	
t_w (L)	CP Pulse Width LOW	20		17		ns	Fig. 3-8
t_w (H)	MR Pulse Width HIGH	20		17		ns	Fig. 3-16
t_{rec}	Recovery Time, MR to CP	10		15		ns	

54/74174
54S/74S174
54LS/74LS174
HEX D FLIP-FLOP

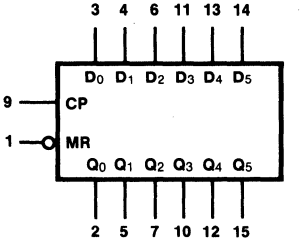
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '174 is a high speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **ASYNCHRONOUS COMMON RESET**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74174PC, 74S174PC, 74LS174PC		9B
Ceramic DIP (D)	A	74174DC, 74S174DC, 74LS174DC	54174DM, 54S174DM, 54LS174DM	6B
Flatpak (F)	A	74174FC, 74S174FC, 74LS174FC	54174FM, 54S174FM, 54LS174FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$D_0 - D_5$	Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	1.25/1.25	0.5/0.25
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0	1.25/1.25	0.5/0.25
$Q_0 - Q_5$	Flip-Flop Outputs	20/10	25/12.5	10/5.0 (2.5)

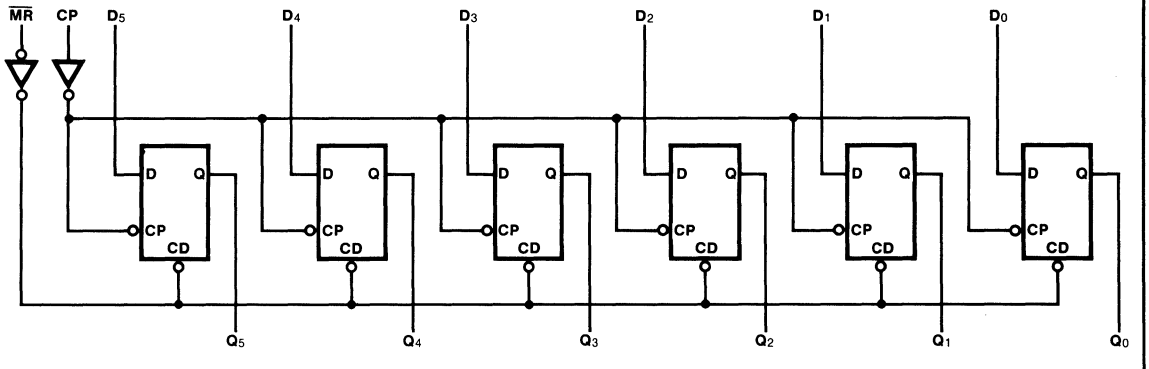
FUNCTIONAL DESCRIPTION — The '174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The '174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

TRUTH TABLE

INPUTS	OUTPUTS
@ t_n, $\overline{MR}$ = H	@ t_{n+1}
D_n	Q_n
H	H
L	L

t_n = Bit time before positive-going clock transition
t_{n+1} = Bit time after positive-going clock transition
H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
I_{CC}	Power Supply Current		65		144		26	mA	V_{CC} = Max D_n = $\overline{MR}$ = 4.5 V CP = ⎍

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF R_L = 400 Ω		C_L = 15 pF R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	25		75		30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		30 35		12 17		25 22	ns	Figs. 3-1, 3-8
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		35		22		35	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

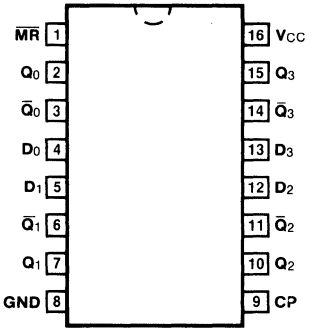
SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to CP	20 20		5.0 5.0		10 10		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to CP	5.0 5.0		3.0 3.0		5.0 5.0		ns	
t_w (H)	CP Pulse Width HIGH	20		7.0		18		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		7.0		18		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	25		5.0		12		ns	

54/74175
54S/74S175
54LS/74LS175
QUAD D FLIP-FLOP

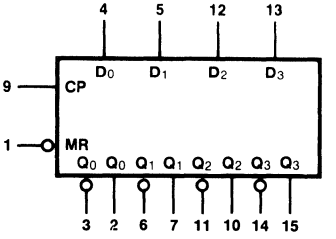
DESCRIPTION — The '175 is a high speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **ASYNCHRONOUS COMMON RESET**
- **TRUE AND COMPLEMENT OUTPUT**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5% TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74175PC, 74S175PC 74LS175PC		9B
Ceramic DIP (D)	A	74175DC, 74S175DC 74LS175DC	54175DM, 54S175DM 54LS175DM	6B
Flatpak (F)	A	74175FC, 74S175FC 74LS175FC	54175FM, 54S175FM 54LS175FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$D_0 - D_3$	Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	1.25/1.25	0.5/0.25
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0	1.25/1.25	0.5/0.25
$Q_0 - Q_3$	True Outputs	20/10	25/12.5	10/5.0 (2.5)
$\overline{Q}_0 - \overline{Q}_3$	Complement Outputs	20/10	25/12.5	10/5.0 (2.5)

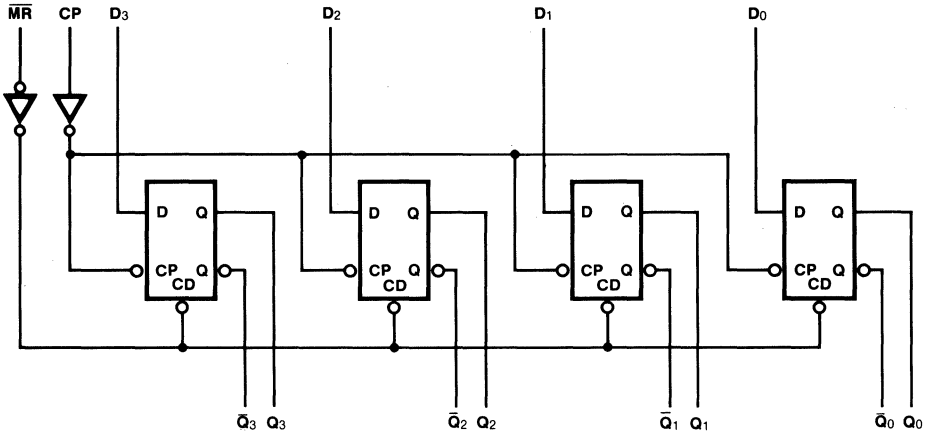
FUNCTIONAL DESCRIPTION — The '175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The '175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

INPUTS	OUTPUTS	
@ t_n, $\overline{MR}$ = H	@ t_{n+1}	
D_n	Q_n	$\overline{Q}_n$
L	L	H
H	H	L

t_n = Bit time before clock positive-going transition
t_{n+1} = Bit time after clock positive-going transition
H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
I_{CC}	Power Supply Current		45		96		18	mA	V_{CC} = Max D_n = $\overline{MR}$ = 4.5 V CP = ⎍

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF R_L = 400 Ω		C_L = 15 pF R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	25		75		30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		30 35		12 17		25 25	ns	Figs. 3-1, 3-8
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		35		22		33	ns	Figs. 3-1, 3-16
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$		25		15		24	ns	Figs. 3-1, 3-16

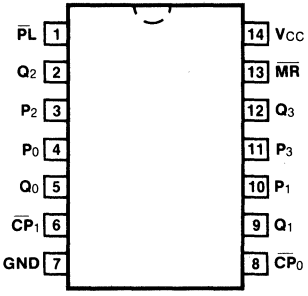
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to CP	20 20		5.0 5.0		10 10		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to CP	5.0 5.0		3.0 3.0		5.0 5.0		ns	
t_w (H)	CP Pulse Width HIGH	20		7.0		15		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		7.0		18		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	25		5.0		12		ns	Fig. 3-16

54/74176

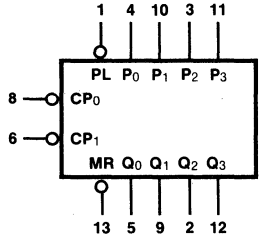
PRESETTABLE DECADE COUNTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '176 is a presettable decade ripple counter partitioned into divide-by-two and divide-by-five sections, with separate clock inputs for the two sections. It can be connected to operate either in a BCD (8421) sequence or in a bi-quinary sequence producing a 50% duty cycle output. A LOW signal on the Master Reset ($\overline{MR}$) input overrides all other inputs and forces the Q outputs LOW. A LOW signal on the Parallel Load ($\overline{PL}$) input causes the Q outputs to assume the state of their respective Parallel Data (P_n) inputs, regardless of the clock. In the counting mode, state changes are initiated by the falling edge of the clock.

LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0° C to +70° C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	74176PC		9A
Ceramic DIP (D)	A	74176DC	54176DM	6A
Flatpak (F)	A	74176FC	54176FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\overline{CP_0}$	÷2 Section Clock Input (Active Falling Edge)	2.0/3.0
$\overline{CP_1}$	÷5 Section Clock Input (Active Falling Edge)	3.0/3.0
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	2.0/2.0
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0
$Q_0 - Q_3$	Flip-flop Outputs*	20/10

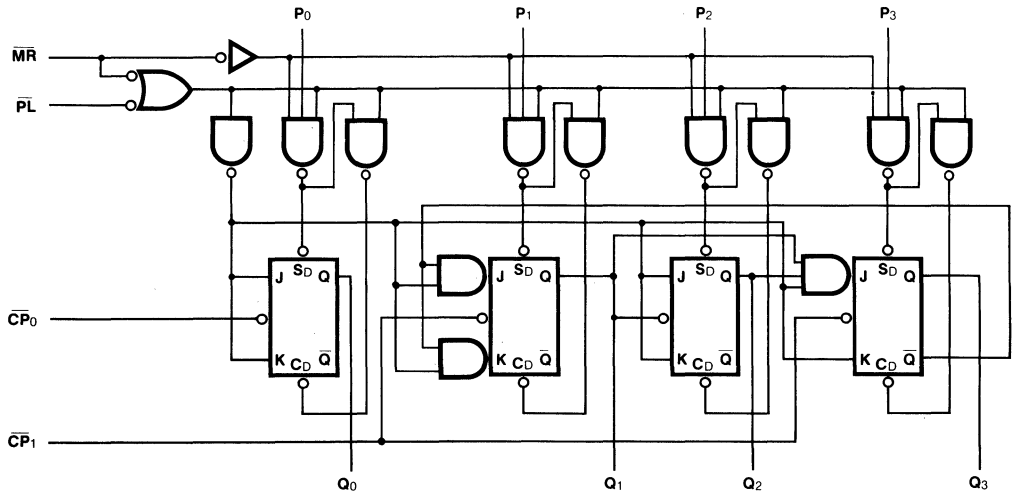
*Q_0 is guaranteed to drive $\overline{CP_1}$ in addition to the full rated load.

FUNCTIONAL DESCRIPTION — The '176 is an asynchronously presettable decade ripple counter partitioned into divide-by-two and divide-by-five sections. In the counting modes, state changes are initiated by the HIGH-to-LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The $\overline{CP}_0$ input serves the Q_0 flip-flop while the $\overline{CP}_1$ input serves the divide-by-five section. The Q_0 output is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input.

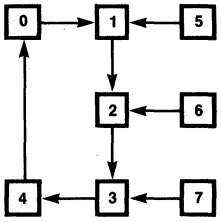
The '176 can be connected up to operate in two different count sequences. With the input frequency connected to $\overline{CP}_0$ and with Q_0 driving $\overline{CP}_1$, the circuit counts in the BCD (8421) sequence. With the input frequency connected to $\overline{CP}_1$ and Q_3 driving $\overline{CP}_0$, Q_0 becomes the low frequency output and has a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the latter (bi-quinary) configuration because of the interstage gating delay within the divide-by-five section.

The '176 has an asynchronous active LOW Master Reset input ($\overline{MR}$) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input ($\overline{PL}$) overrides the clock inputs and loads the data from Parallel Data (P_0 — P_3) inputs into flip-flops. While $\overline{PL}$ is LOW, the counters act as transparent latches and any change in the P_n inputs will be reflected in the outputs. In order for the intended parallel data to be entered and stored, the recommended setup and hold times with respect to the rising edge of $\overline{PL}$ should be observed.

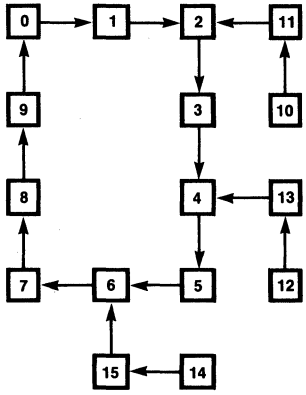
LOGIC DIAGRAM



÷5 STATE DIAGRAM



BCD STATE DIAGRAM



MODE SELECT TABLE

INPUTS			RESPONSE
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Q_n forced LOW
H	L	X	$P_n \rightarrow Q_n$
H	H	⌐	Count Up

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
Icc	Power Supply Current		48	mA	V_{CC} = Max All inputs = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω Min	54/74 Max	UNITS	CONDITIONS
f_{max}	Maximum Count Frequency at $\overline{CP_0}$	35		MHz	Figs. 3-1, 3-9
f_{max}	Maximum Count Frequency at $\overline{CP_1}$	17.5		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_0}$ to Q_0		13 17	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_1		17 26	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_2		41 51	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_3 for '176		20 26	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_3 for '177		66 75	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		29 46	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		43 48	ns	Figs. 3-1, 3-16
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		48	ns	Figs. 3-1, 3-16

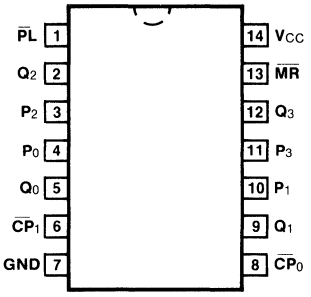
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
t_s (H)	Setup Time HIGH P_n to $\overline{PL}$	15		ns	Fig. 3-13
t_h (H)	Hold Time HIGH P_n to $\overline{PL}$	0		ns	Fig. 3-13
t_s (L)	Setup Time LOW P_n to $\overline{PL}$	20		ns	Fig. 3-13
t_h (L)	Hold Time LOW P_n to $\overline{PL}$	0		ns	Fig. 3-13
t_w (H)	$\overline{CP_0}$ Pulse Width HIGH	14		ns	Fig. 3-9
t_w (H)	$\overline{CP_1}$ Pulse Width HIGH	28		ns	Fig. 3-9
t_w (L)	$\overline{PL}$ Pulse Width LOW	25		ns	Fig. 3-16
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ or $\overline{PL}$ to $\overline{CP_n}$	25		ns	Fig. 3-16

54/74177

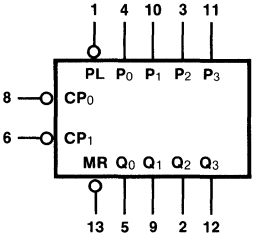
PRESETTABLE BINARY COUNTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The'177 is a presettable modulo-16 ripple counter partitioned into divide-by-two and divide-by-eight sections, with a separate clock input for each section. In the counting mode, state changes are initiated by the falling edge of the clock. A LOW signal on the Master Reset ($\overline{MR}$) input overrides all other inputs and forces the outputs LOW. A LOW signal on the Parallel Load ($\overline{PL}$) input overrides the clocks and causes the Q outputs to assume the state of their respective Parallel Data (P_n) inputs. For detail specifications, please refer to the '176 data sheet.

LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	A	74177PC		9A
Ceramic DIP (D)	A	74177DC	54177DM	6A
Flatpak (F)	A	74177FC	54177FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\overline{CP_0}$	÷2 Section Clock Input (Active Falling Edge)	2.0/3.0
$\overline{CP_1}$	÷8 Section Clock Input (Active Falling Edge)	2.0/2.0
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	2.0/2.0
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0
$Q_0 - Q_3$	Flip-flop Outputs*	20/10

*Q_0 is guaranteed to drive $\overline{CP_1}$ in addition to the full rated load.

FUNCTIONAL DESCRIPTION—The '177 is an asynchronously presettable binary ripple counter partitioned into divide-by-two and divide-by-eight sections. In the counting modes, state changes are initiated by the HIGH-to-LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q_n outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The $\overline{CP}_0$ input serves the Q_0 flip-flop while the $\overline{CP}_1$ input serves the divide-by-eight section. The Q_0 output is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input. With the input frequency connected to $\overline{CP}_0$ and with Q_0 driving $\overline{CP}_1$, the '177 forms a straightforward modulo-16 counter, with Q_0 the least significant output and Q_3 the most significant output.

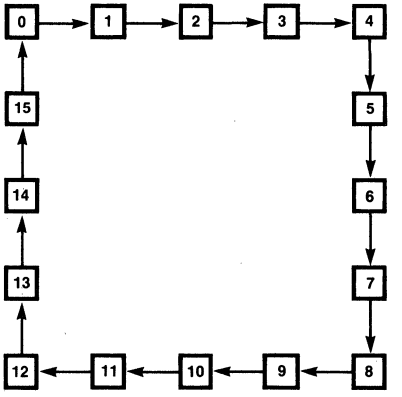
The '177 has an asynchronous active LOW Master Reset input ($\overline{MR}$) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input ($\overline{PL}$) overrides the clock inputs and loads the data from Parallel Data ($P_0 - P_3$) inputs into the flip-flops. While $\overline{PL}$ is LOW, the counters act as transparent latches and any change in the P_n inputs will be reflected in the outputs.

MODE SELECT TABLE

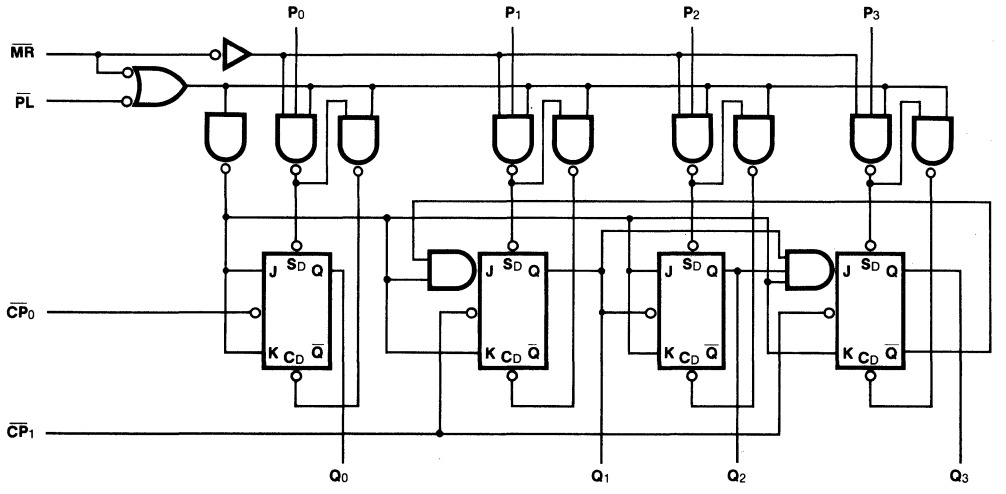
INPUTS			RESPONSE
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Q_n forced LOW
H	L	X	$P_n \rightarrow Q_n$
H	H	⌐_	Count Up

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

STATE DIAGRAM



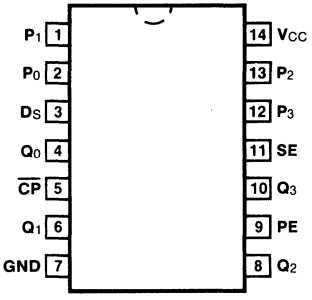
LOGIC DIAGRAM



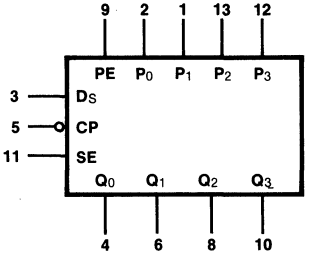
54/74178

4-BIT SHIFT REGISTER

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

DESCRIPTION — The '178 features synchronous parallel or serial entry and parallel outputs. The flip-flops are fully edge-triggered, with state changes initiated by a HIGH-to-LOW transition of the clock. Parallel Enable and Serial Enable inputs are used to select Load, Shift and Hold modes of operation. The '178 is the 14-pin version of the '179. For detail specifications, please refer to the '179 data sheet.

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74178PC		9A
Ceramic DIP (D)	A	74178DC	54178DM	6A
Flatpak (F)	A	74178FC	54178FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
PE	Parallel Enable Input	1.0/1.0
P0 — P3	Parallel Data Inputs	1.0/1.0
DS	Serial Data Input	1.0/1.0
$\overline{SE}$	Shift Enable Input	1.0/1.0
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	1.0/1.0
Q0 — Q3	Flip-flop Outputs	20/10

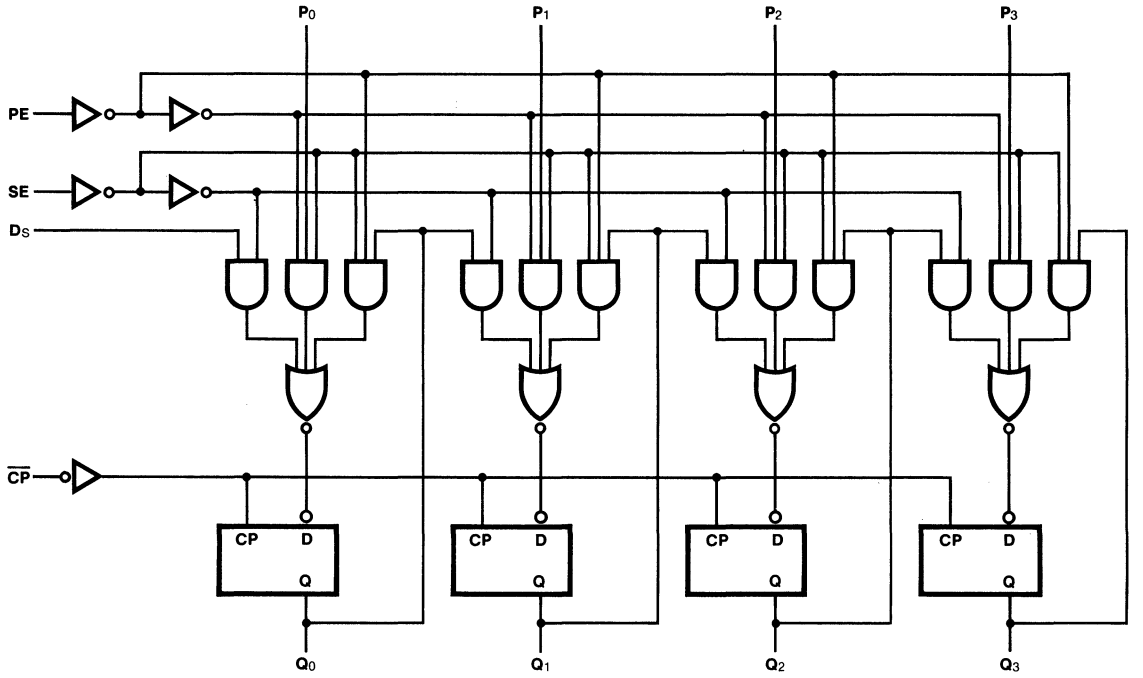
FUNCTIONAL DESCRIPTION — The '178 contains four D-type edge-triggered flip-flops and sufficient interstage logic to perform parallel load, shift right or hold operations. All state changes are initiated by a HIGH-to-LOW transition of the clock. A HIGH signal on the Shift Enable (SE) input prevents parallel loading and permits a right shift each time the clock makes a negative transition. When the SE input is LOW, the signal applied to the Parallel Enable (PE) input determines whether the circuit is in a parallel load or a hold mode, as shown in the Mode Select Table. The SE, PE, D_S and P_n inputs can change when the clock is in either state, provided only that the recommended setup and hold times are observed.

MODE SELECT TABLE

INPUTS			RESPONSE
SE	PE	$\overline{CP}$	
H	X	⊓	Right Shift. $D_S \rightarrow Q_0$; $Q_0 \rightarrow Q_1$, etc.
L	H	⊓	Parallel load $P_n \rightarrow Q_n$.
L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial.

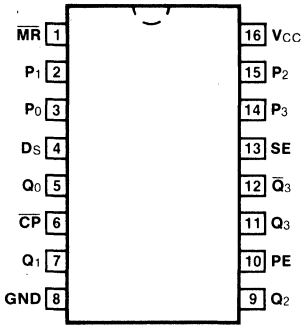
LOGIC DIAGRAM



54/74179

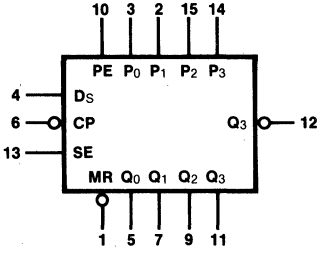
4-BIT SHIFT REGISTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '179 features synchronous parallel or serial entry, asynchronous reset and parallel outputs, with the complement output of the fourth stage also available. The flip-flops are fully edge-triggered, with state changes initiated by a HIGH-to-LOW transition of the clock. Parallel Enable and Serial Enable inputs are used to select Load, Shift and Hold modes of operation. A LOW signal on the Master Reset input overrides all other inputs and forces the Q outputs to the LOW state.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	A	74179PC		9B
Ceramic DIP (D)	A	74179DC	54179DM	6B
Flatpak (F)	A	74179FC	54179FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
PE	Parallel Enable Input	1.0/1.0
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0
D_S	Serial Data Input	1.0/1.0
SE	Shift Enable Input	1.0/1.0
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	1.0/1.0
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0
$Q_0 - Q_3$	Flip-flop Outputs	20/10
$\overline{Q}_3$	Fourth Stage Complement Output	20/10

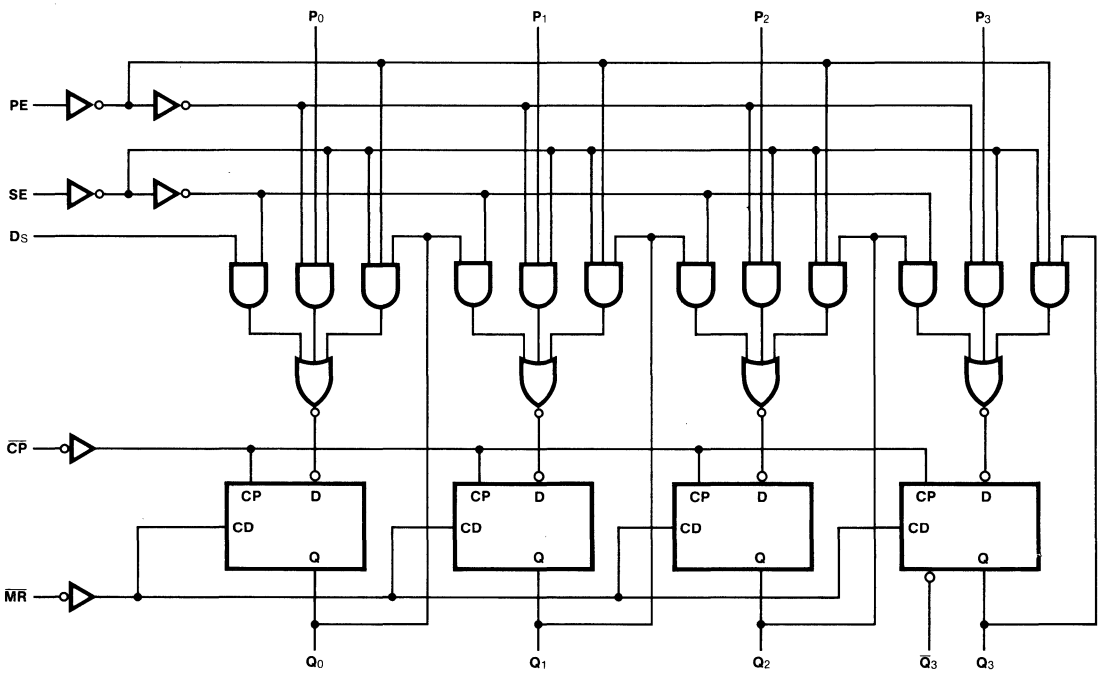
FUNCTIONAL DESCRIPTION — The '179 contains four D-type edge-triggered flip-flops and sufficient inter-stage logic to perform parallel load, shift right or hold operations. All state changes except reset are initiated by a HIGH-to-LOW transition of the clock. A LOW signal on $\overline{MR}$ overrides all other inputs and forces the Q outputs LOW and $\overline{Q}_3$ HIGH. With $\overline{MR}$ HIGH, a HIGH signal on SE prevents parallel loading and permits a right shift each time the clock makes a HIGH-to-LOW transition. When $\overline{MR}$ and SE are LOW, the signal applied to PE determines whether the circuit is in a parallel load or a hold mode, as shown in the Mode Select Table. The SE, PE, D_S and P_n inputs can change when the clock is in either state, provided only that the recommended setup and hold times are observed.

MODE SELECT TABLE

INPUTS				RESPONSE
$\overline{MR}$	SE	PE	$\overline{CP}$	
L	X	X	X	Asynchronous Reset; $Q_n \rightarrow$ LOW; $Q_3 \rightarrow$ HIGH
H	H	X	⌐	Right Shift. $D_S \rightarrow Q_0$; $Q_0 \rightarrow Q_1$, etc.
H	L	H	⌐	Parallel load. $P_n \rightarrow Q_n$
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		70	mA	V_{CC} = Max, P_n = Gnd D_S, $\overline{PE}$, SE, $\overline{MR}$ = 4.5 V $\overline{CP}$ = ⌝⌞
		XC		75		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 C_L = 15 pF, R_L = 400 Ω Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	25		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_n		26 35	ns	Figs. 3-1, 3-9
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_3		23	ns	Figs. 3-1, 3-17
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		36	ns	

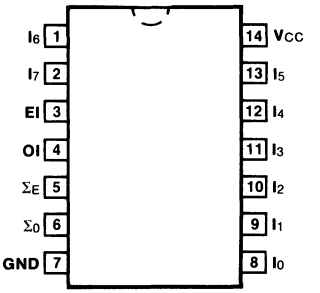
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW D_S or P_n to $\overline{CP}$	30 30		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time HIGH or LOW D_S or P_n to $\overline{CP}$	5.0 5.0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW PE or SE to $\overline{CP}$	35 35		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW PE or SE to $\overline{CP}$	5.0 5.0		ns	
t_w (H)	$\overline{CP}$ Pulse Width HIGH	20		ns	Fig. 3-9
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		ns	Fig. 3-17
t_{rec}	Recovery Time $\overline{MR}$ to $\overline{CP}$	15		ns	Fig. 3-17

54/74180

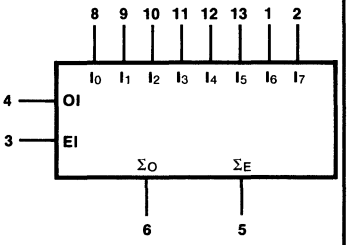
8-BIT PARITY GENERATOR/CHECKER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '180 is a monolithic, 8-bit parity checker/generator which features control inputs and even/odd outputs to enhance operation in either odd or even parity applications. Cascading these circuits allows unlimited word length expansion. Typical application would be to generate and check parity on data being transmitted from one register to another. Typical power dissipation is 170 mW.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V, ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74180PC		9A
Ceramic DIP (D)	A	74180DC	54180DM	6A
Flatpak (F)	A	74180FC	54180FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

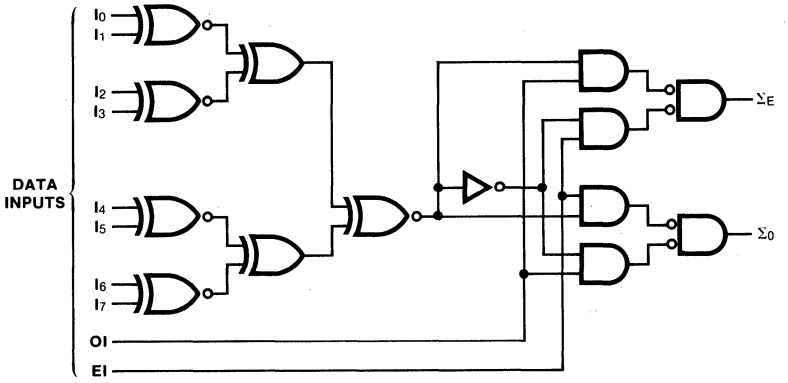
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
I_0 — I_7	Data Inputs	1.0/1.0
OI	Odd Input	2.0/2.0
EI	Even Input	2.0/2.0
Σ_O	Odd Parity Output	20/10
Σ_E	Even Parity Output	20/10

TRUTH TABLE

INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	XM	-20	-55	mA	V_{CC} = Max
		XC	-18	-55		
I_{CC}	Power Supply Current	XM		49	mA	V_{CC} = Max, I_n = Open OI, EI = 4.5 V
		XC		56		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω Min	54/74 C_L = 15 pF R_L = 400 Ω Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_E		60 68	ns	Figs. 3-1, 3-5 OI = Gnd
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_O		48 38	ns	Figs. 3-1, 3-4 OI = Gnd
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_E		48 38	ns	Figs. 3-1, 3-5 EI = Gnd
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_O		60 68	ns	Figs. 3-1, 3-4 EI = Gnd
t_{PLH} t_{PHL}	Propagation Delay EI or OI to Σ_E		20 10	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay EI or OI to Σ_O		20 10	ns	Figs. 3-1, 3-4

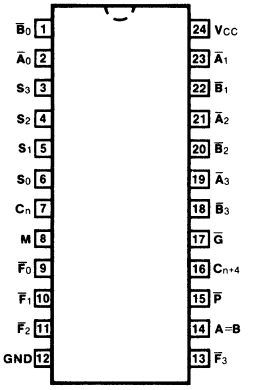
54LS/74LS181

4-BIT ARITHMETIC LOGIC UNIT

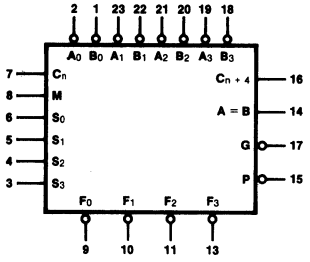
DESCRIPTION — The '181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations. For improved TTL, S-TTL and LP-TTL versions, please see the 9341 data sheet.

- **PROVIDES 16 ARITHMETIC OPERATIONS**
  ADD, SUBTRACT, COMPARE, DOUBLE, PLUS
  TWELVE OTHER ARITHMETIC OPERATIONS
- **PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES**
  EXCLUSIVE-OR, COMPARE, AND, NAND, OR, NOR,
  PLUS TEN OTHER LOGIC OPERATIONS
- **FULL LOOKAHEAD FOR HIGH SPEED ARITHMETIC**
  OPERATION ON LONG WORDS

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS181PC		9N
Ceramic DIP (D)	A	74LS181DC	54LS181DM	6N
Flatpak (F)	A	74LS181FC	54LS181FM	4M

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$\overline{A}_0$ — $\overline{A}_3$	Operand Inputs (Active LOW)	1.5/0.75
$\overline{B}_0$ — $\overline{B}_3$	Operand Inputs (Active LOW)	1.5/0.75
S_0 — S_3	Function Select Inputs	2.0/1.0
M	Mode Control Input	0.5/0.25
C_n	Carry Input	2.5/1.25
$\overline{F}_0$ — $\overline{F}_3$	Function Outputs (Active LOW)	10/5.0 (2.5)
A = B	Comparator Output	OC*/5.0 (2.5)
$\overline{G}$	Carry Generate Output (Active LOW)	10/10
$\overline{P}$	Carry Propagate Output (Active LOW)	10/5.0
C_{n+4}	Carry Output	10/5.0 (2.5)

*OC — Open Collector

FUNCTIONAL DESCRIPTION — The 'LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0 — S_3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). In the ADD mode, $\overline{P}$ indicates that $\overline{F}$ is 15 or more, while $\overline{G}$ indicates that $\overline{F}$ is 16 or more. In the SUBTRACT mode, $\overline{P}$ indicates that $\overline{F}$ is zero or less, while $\overline{G}$ indicates that $\overline{F}$ is less than zero. $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high speed operation the device is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of four 'LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open-collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

FUNCTION TABLE

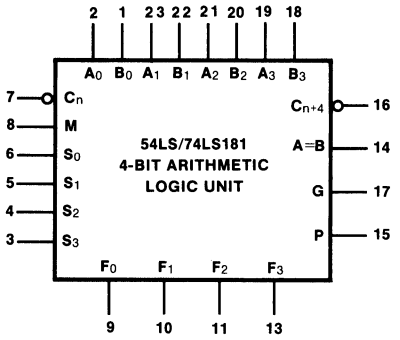
MODE SELECT INPUTS				ACTIVE LOW OPERANDS & F_n OUTPUTS		ACTIVE HIGH OPERANDS & F_n OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A + B
L	L	H	L	$\overline{A+B}$	A$\overline{B}$ minus 1	$\overline{A}B$	A + $\overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A+B}$	A plus (A + $\overline{B}$)	$\overline{AB}$	A plus A$\overline{B}$
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)	$\overline{B}$	(A + B) plus A$\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	A $\oplus$ B	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$	A$\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}B$	A plus (A + B)	$\overline{A+B}$	A plus AB
H	L	L	H	A $\oplus$ B	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	A$\overline{B}$ plus (A + B)	B	(A + $\overline{B}$) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A*	Logic 1	A plus A*
H	H	L	H	A$\overline{B}$	AB plus A	A + $\overline{B}$	(A + B) plus A
H	H	H	L	AB	A$\overline{B}$ minus A	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A	A	A minus 1

*each bit is shifted to the next more significant position

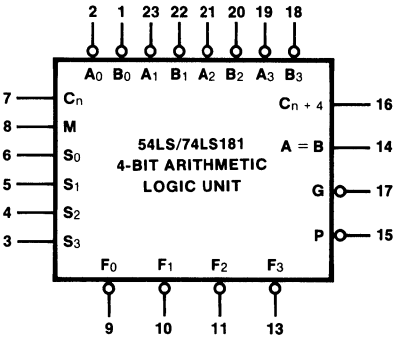
**arithmetic operations expressed in 2s complement notation

LOGIC SYMBOLS

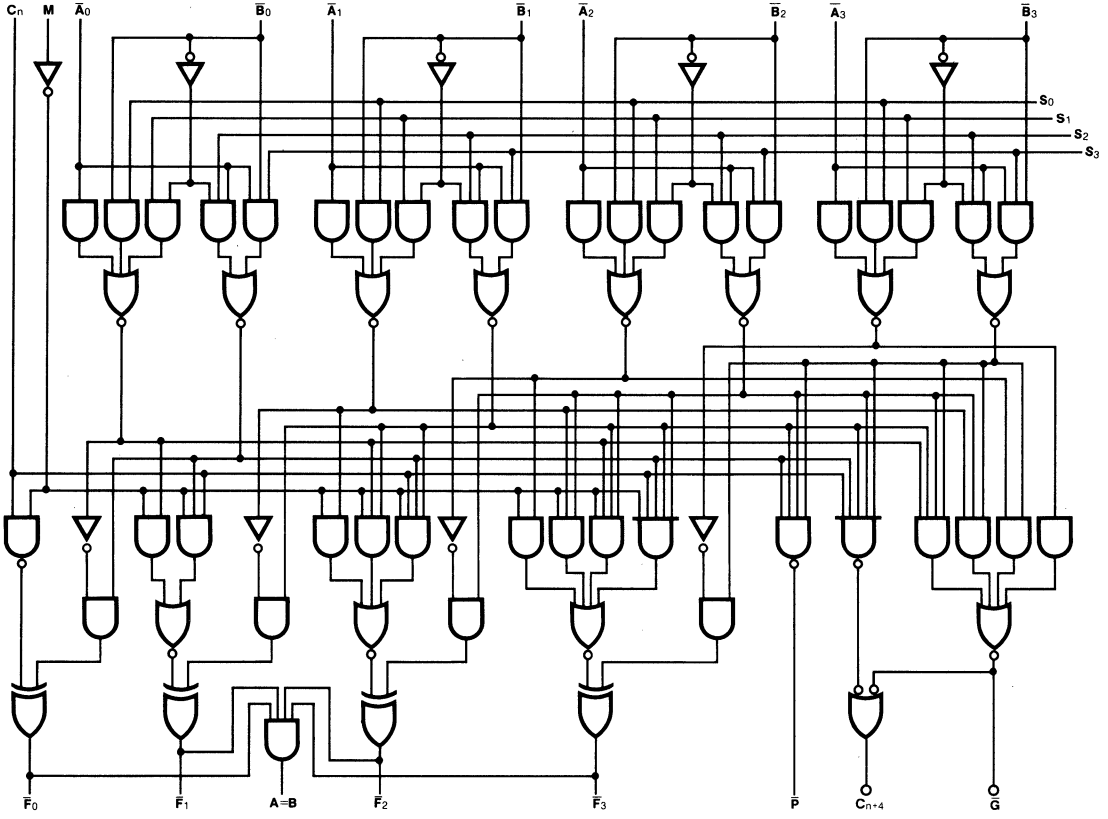
ACTIVE HIGH OPERANDS



ACTIVE LOW OPERANDS



LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OH}	Output HIGH Current, A = B			100	μA	V_{CC} = Min, V_{OH} = 5.5 V
I_{CC}	Power Supply Current	XM		32	mA	V_{CC} = Max $\overline{B}_n$, C_n = Gnd S_n, M, $\overline{A}_n$ = 4.5 V
		XC		34		
		XM		35	mA	V_{CC} = Max $\overline{A}_n$, $\overline{B}_n$, C_n = Gnd M, S_n = 4.5 V
		XC		37		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF Min	54/74LS C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+4}		27 20	ns	M = Gnd, Figs. 3-1, 3-5 Tables I & II
t_{PLH} t_{PHL}	Propagation Delay C_n to $\overline{F}$		26 20	ns	M = Gnd, Figs. 3-1, 3-5 Table I
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$		29 23	ns	M, S_1, S_2 = Gnd; S_1, S_3 = 4.5 V; Figs. 3-1, 3-5 Table I
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$		32 26	ns	M, S_0, S_3 = Gnd; S_1, S_2 = 4.5 V; Figs. 3-1, 3-4, 3-5; Table II
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$		30 30	ns	M, S_1, S_2 = Gnd; S_0, S_3 = 4.5 V; Figs. 3-1, 3-4; Table I
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$		30 33	ns	M, S_0, S_3 = Gnd; S_1, S_2 = 4.5 V; Figs. 3-1, 3-4, 3-5; Table II
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$		32 25	ns	M, S_1, S_2 = Gnd; S_0, S_3 = 4.5 V; Figs. 3-1, 3-5: Table I
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$		32 32	ns	M, S_0, S_3 = Gnd; S_1, S_2 = 4.5 V; Figs. 3-1, 3-4, 3-5; Table II
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F}$		33 29	ns	M = 4.5 V; Figs. 3-1, 3-5; Table III
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to C_{n+4}		38 38	ns	M, S_1, S_2 = Gnd; S_0, S_3 = 4.5 V; Figs. 3-1, 3-4; Table I

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (Cont'd)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF Min	54/74LS C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to C_{n+4}		41 41	ns	M, S_0, S_3 = Gnd; S_1, S_2 = 4.5 V; Figs. 3-1, 3-4, 3-5; Table II
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to A = B		50 62	ns	M, S_0, S_3 = Gnd; S_1, S_2 = 4.5 V; R_L = 2 kΩ to 5.0 V; Figs. 3-2, 3-4, 3-5; Table II

SUM MODE TEST TABLE I **FUNCTION INPUTS:** $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = M = 0$ V

SYMBOL	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE II **FUNCTION INPUTS:** $S_1 = S_2 = 4.5$ V, $S_0 = S_3 = M = 0$ V

SYMBOL	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}

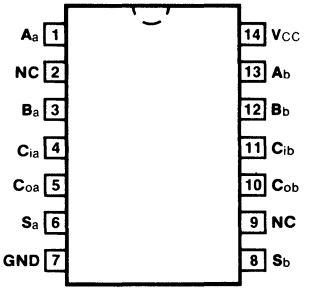
LOGIC MODE TEST TABLE III **FUNCTION INPUTS:** $S_1 = S_2 = M = 4.5$ V, $S_0 = S_3 = 0$ V

SYMBOL	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$

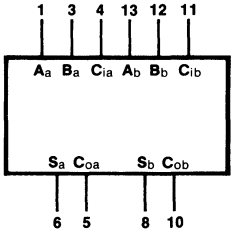
54H/74H183

DUAL HIGH SPEED ADDER

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

DESCRIPTION — The '183 contains two independent full adders. Each adder has an individual carry output for use in multiple-input, carry-save techniques to produce the true sum and true carry outputs with no more than two gate delays. Typical propagation delay is 12 ns.

TRUTH TABLE
(Each Half)

INPUTS			OUTPUTS	
A	B	Ci	S	Co
L	L	L	L	L
H	L	L	H	L
L	H	L	H	L
L	L	H	H	L
H	H	L	L	H
H	L	H	L	H
L	H	H	L	H
H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

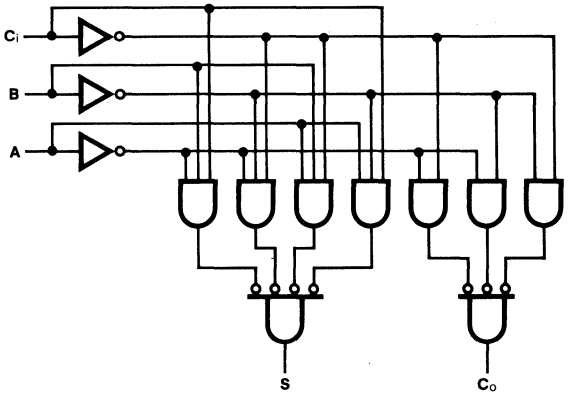
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74H183PC		9A
Ceramic DIP (D)	A	74H183DC	54H183DM	6A
Flatpak (F)	A	74H183FC	54H183FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74H (U.L.) HIGH/LOW
Aa, Ba	Side a Operand Inputs	3.75/3.75
Ab, Bb	Side b Operand Inputs	3.75/3.75
Cia, Cib	Carry Inputs	3.75/3.75
Sa, Bb	Sum Outputs	25/12.5
Coa, Cob	Carry Outputs	25/12.5

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74H Min	54/74H Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		69	mA	V_{CC} = Max All Inputs = Gnd
		XC		75		

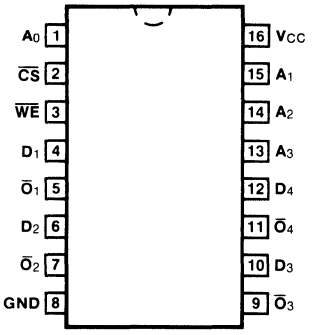
AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74H C_L = 25 pF R_L = 280 Ω Min	Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_x, B_x or C_{ix} to S_x		15 18	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay A_x, B_x or C_{ix} to C_{ox}		15 18	ns	Figs. 3-1, 3-5

54S/74S189
54LS/74LS189

64-BIT RANDOM ACCESS MEMORY
(With 3-State Outputs)

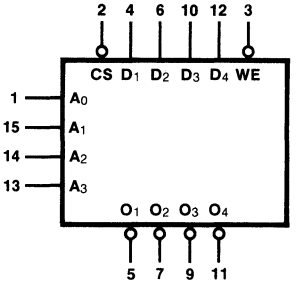
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '189 is a high speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-state and are in the high impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

- **3-STATE OUTPUTS FOR DATA BUS APPLICATIONS**
- **BUFFERED INPUTS MINIMIZE LOADING**
- **ADDRESS DECODING ON-CHIP**
- **DIODE CLAMPED INPUTS MINIMIZE RINGING**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S189PC, 74LS189PC		9B
Ceramic DIP (D)	A	74S189DC, 74LS189DC	54S189DM, 54LS189DM	6B
Flatpak (F)	A	74S189FC, 74LS189FC	54S189FM, 54LS189FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

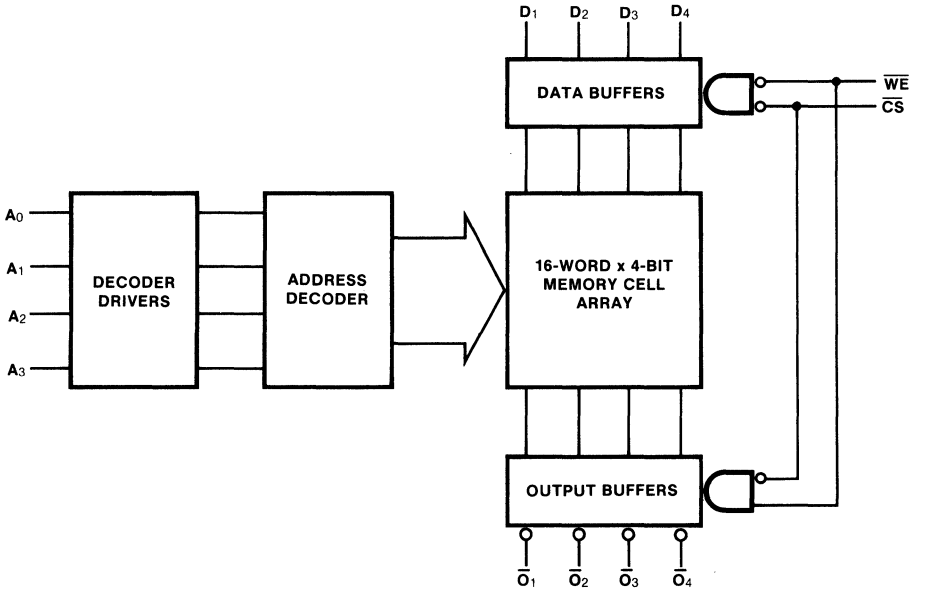
PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	0.63/0.16	0.5/0.013
$\overline{CS}$	Chip Select Input (Active LOW)	0.63/0.16	0.5/0.013
$\overline{WE}$	Write Enable Input (Active LOW)	0.63/0.16	0.5/0.013
$D_1 - D_4$	Data Inputs	0.63/0.16	0.5/0.013
$\overline{O}_1 - \overline{O}_4$	Inverted Data Outputs	162/10 (50)	10/10 (5.0)

FUNCTION TABLE

INPUTS		OPERATION	CONDITION OF OUTPUTS
$\overline{CS}$	$\overline{WE}$		
L	L	Write	High Impedance
L	H	Read	Complement of Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S		54/74LS		UNITS	CONDITIONS
			Min	Max	Min	Max		
V_{OL}	Output LOW Voltage	XM		0.5		0.4	V	V_{CC} = Min I_{OL} = 16 mA ('S189) I_{OL} = 8.0 mA (54LS189) I_{OL} = 16 mA (74LS189)
		XC		0.45		0.5		
V_{OH}	Output HIGH Voltage	XM		2.4		2.8	V	V_{CC} = Min I_{OH} = 2.0 mA (54S189) I_{OH} = 6.5 mA (74S189) I_{OH} = 0.4 mA ('LS189)
		XC		2.4		2.8		
I_{OS}	Output Short Circuit Current		-30	-100	-80*		mA	V_{CC} = Max
I_{CC}	Power Supply Current			110		40	mA	V_{CC} = Max; $\overline{WE}$, $\overline{CS}$, Gnd

*Typical Value

AC CHARACTERISTICS OVER RECOMMENDED V_{CC} AND T_A RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S C_L = 30 pF, R_L = 300 Ω Min	54/74S Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Access Time, HIGH or LOW, A_n to $\overline{O}_n$	XM XC		50 35		37* 37*	ns	Figs. 3-1, 3-20
t_{PZH} t_{PZL}	Access Time, HIGH or LOW, $\overline{CS}$ to $\overline{O}_n$	XM XC		32 22		10* 10*	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS189)
t_{PHZ}	Disable Time $\overline{CS}$ to $\overline{O}_n$	XM XC		25 25			ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS189) C_L = 5 pF
t_{PLZ}	Disable Time $\overline{CS}$ to $\overline{O}_n$	XM XC		25 17				
t_{PZH} t_{PZL}	Access Time, HIGH or LOW, $\overline{WE}$ to $\overline{O}_n$	XM XC		40 30			ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS189)
t_{PHZ}	Disable Time $\overline{WE}$ to $\overline{O}_n$	XM XC		30 20			ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS189) C_L = 5 pF
t_{PLZ}	Disable Time $\overline{WE}$ to $\overline{O}_n$	XM XC		32 20				

AC OPERATING REQUIREMENTS OVER RECOMMENDED V_{CC} AND T_A RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to $\overline{WE}$	0 0		10* 10*		ns	Fig. 3-21
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n to $\overline{WE}$	0 0		0* 0*		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to $\overline{WE}$	20 20		25* 25*		ns	Fig. 3-13
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to $\overline{WE}$	0 0		0* 0*		ns	
t_s (L)	Setup Time LOW $\overline{CS}$ to $\overline{WE}$	0				ns	Fig. 3-14
t_h (L)	Hold Time LOW $\overline{CS}$ to $\overline{WE}$	0				ns	Fig. 3-13
t_w (L)	$\overline{WE}$ Pulse Width LOW	20		25*		ns	Fig. 3-14

*Typical Value

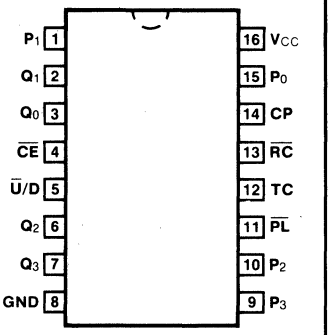
54/74190
54LS/74LS190

UP/DOWN DECADE COUNTER
(With Preset and Ripple Clock)

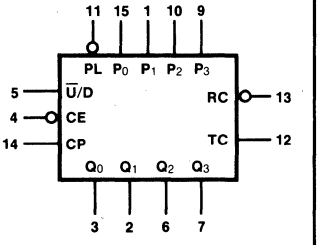
DESCRIPTION — The '190 is a reversible BCD (8421) decade counter featuring synchronous counting and asynchronous presetting. The preset feature allows the '190 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multi-stage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

- **HIGH SPEED — 30 MHz TYPICAL COUNT FREQUENCY**
- **SYNCHRONOUS COUNTING**
- **ASYNCHRONOUS PARALLEL LOAD**
- **CASCADABLE**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

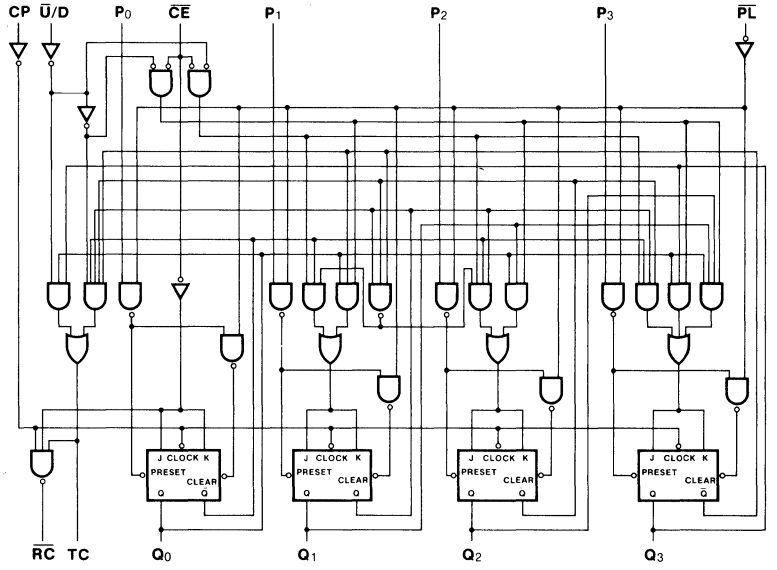
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74190PC, 74LS190PC		9B
Ceramic DIP (D)	A	74190DC, 74LS190DC	54190DM, 54LS190DM	7B
Flatpak (F)	A	74190FC, 74LS190FC	54190FM, 54LS190FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CE}$	Count Enable Input (Active LOW)	3.0/3.0	1.5/0.75
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	0.5/0.25
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0	0.5/0.25
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{U}$/D	Up/Down Count Control Input	1.0/1.0	0.5/0.25
$Q_0 - Q_3$	Flip-flop Outputs	20/10	10/5.0 (2.5)
$\overline{RC}$	Ripple Clock Output (Active LOW)	20/10	10/5.0 (2.5)
TC	Terminal Count Output (Active HIGH)	20/10	10/5.0 (2.5)

LOGIC DIAGRAM



MODE SELECT TABLE

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⎍	Count Up
H	L	H	⎍	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

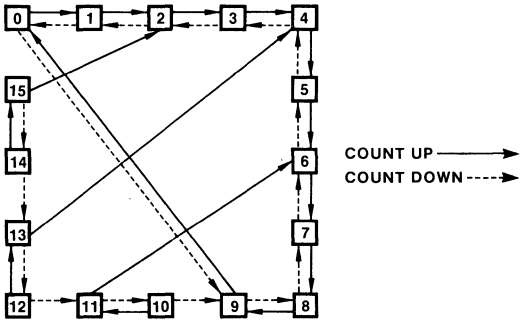
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

RC TRUTH TABLE

INPUTS			OUTPUT
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⎍	⎍
H	X	X	H
X	L	X	H

*TC is generated internally

STATE DIAGRAM



FUNCTIONAL DESCRIPTION — The '190 is a synchronous up/down BCD decade counter and the '191 is a synchronous up/down 4-bit binary counter. The operating modes of the '190 decade counter and the '191 binary counter are identical, with the only difference being the count sequences as noted in the state diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs (P_0 — P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. When counting is to be enabled, the $\overline{CE}$ signal can be made LOW when the clock is in either state. However, when counting is to be inhibited, the LOW-to-HIGH $\overline{CE}$ transition must occur only while the clock is HIGH. Similarly, the $\overline{U}$/D signal should only be changed when either $\overline{CE}$ or the clock is HIGH. These restrictions do not apply to the 'LS190 and 'LS191; $\overline{CE}$ and $\overline{U}$/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches maximum (9 for the '190, 15 for the '191) in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multi-stage counters, as indicated in *Figures a and b*. In *Figure a*, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages in shown in *Figure b*. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH.

The configuration shown in *Figure c* avoids ripple delays and their associated restrictions. The $\overline{CE}$ input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of *Figures a and b* doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

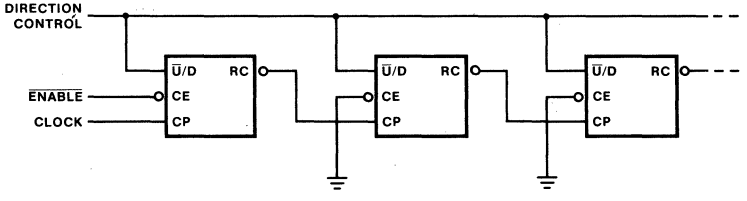


Fig. a N-Stage Counter Using Ripple Clock

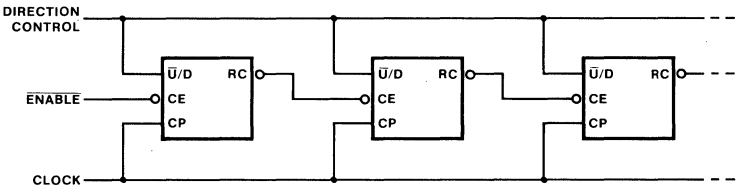


Fig. b Synchronous N-Stage Counter Using Ripple Carry/Borrow

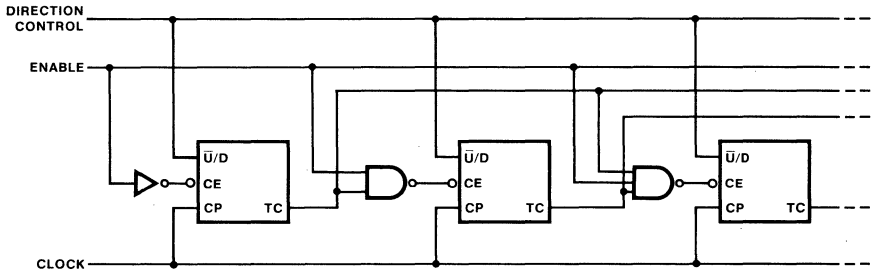


Fig. c Synchronous N-Stage Counter with Parallel Gated Carry/Borrow

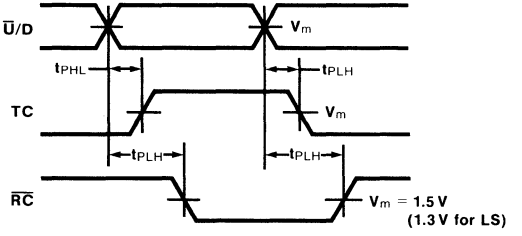


Fig. d

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		99		35	mA	V_{CC} = Max All Inputs = Gnd
		XC		105		35		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
f_{max}	Maximum Count Frequency	20		20		MHz	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		24 36		24 36	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to TC		42 52		42 52	ns	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$		20 24		20 24	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		22 50		22 50	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$		33 33		33 33	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		33 50		33 50	ns	Figs. 3-1, 3-16
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$		45 45		45 45	ns	Fig. 3-1, Fig. d
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{TC}$		33 33		33 33	ns	

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n to $\overline{PL}$	20 20		20 20		ns	Fig. 3-13
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n to $\overline{PL}$	0 0		5.0 5.0		ns	
t_s (L)	Setup Time LOW $\overline{CE}$ to CP	20		20		ns	Fig. 3-6
t_h (L)	Hold Time LOW $\overline{CE}$ to CP	0		0		ns	
t_w (L)	CP Pulse Width LOW	25		20		ns	Fig. 3-8
t_w (L)	$\overline{PL}$ Pulse Width LOW	35		35		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{PL}$ to CP	20		20		ns	Fig. 3-16

54/74191
54LS/74LS191

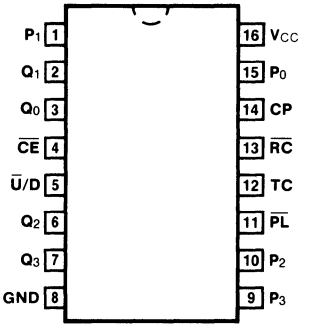
UP/DOWN BINARY COUNTER

(With Preset and Ripple Clock)

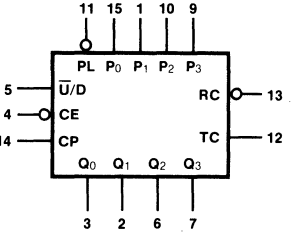
DESCRIPTION — The '191 is a reversible modulo-16 binary counter featuring synchronous counting and asychronous presetting. The preset feature allows the '191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multi-stage counters. In the counting modes, state changes are initiated by the rising edge of the clock. For detail specifications and functional description, please refer to the '190 data sheet.

- **HIGH SPEED — 30 MHz TYPICAL COUNT FREQUENCY**
- **SYNCHRONOUS COUNTING**
- **ASYNCHRONOUS PARALLEL LOAD**
- **CASCADABLE**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10% TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74191PC, 74LS191PC		9B
Ceramic DIP (D)	A	74191DC, 74LS191DC	54191DM, 54LS191DM	7B
Flatpak (F)	A	74191FC, 74LS191FC	54191FM, 54LS191FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CE}$	Count Enable Input (Active LOW)	3.0/3.0	1.5/0.75
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	0.5/0.25
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0	0.5/0.25
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{U}$/D	Up/Down Count Control Input	1.0/1.0	0.5/0.25
$Q_0 - Q_3$	Flip-flop Outputs	20/10	10/5.0 (2.5)
$\overline{RC}$	Ripple Clock Output (Active LOW)	20/10	10/5.0 (2.5)
TC	Terminal Count Output (Active HIGH)	20/10	10/5.0 (2.5)

MODE SELECT TABLE

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⌐	Count Up
H	L	H	⌐	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

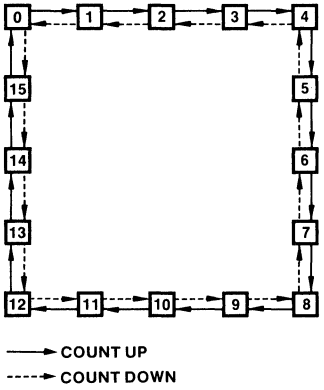
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

RC TRUTH TABLE

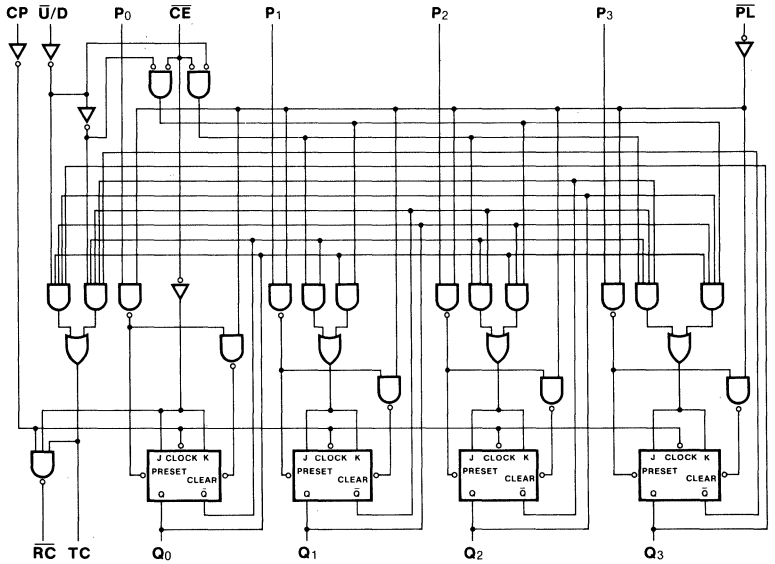
INPUTS			OUTPUT
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⊓	⊓
H	X	X	H
X	L	X	H

*TC is generated internally

STATE DIAGRAM



LOGIC DIAGRAM



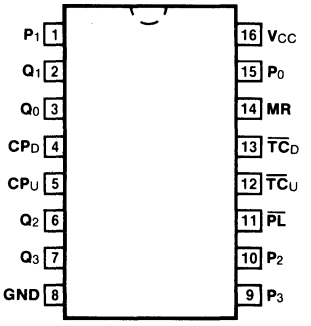
54/74192
54LS/74LS192

UP/DOWN DECADE COUNTER
(With Separate Up/Down Clocks)

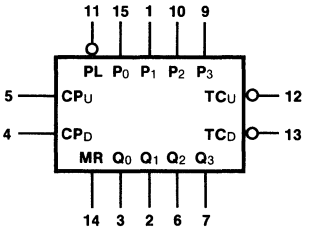
DESCRIPTION — The '192 is an up/down BCD decade (8421) counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74192PC, 74LS192PC		9B
Ceramic DIP (D)	A	74192DC, 74LS192DC	54192DM, 54LS192DM	6B
Flatpak (F)	A	74192FC, 74LS192FC	54192FM, 54LS192FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
CP_U	Count Up Clock Input (Active Rising Edge)	1.0/1.0	0.5/0.25
CP_D	Count Down Clock Input (Active Rising Edge)	1.0/1.0	0.5/0.25
MR	Asynchronous Master Reset Input (Active HIGH)	1.0/1.0	0.5/0.25
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	0.5/0.25
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0	0.5/0.25
$Q_0 - Q_3$	Flip-flop Outputs	20/10	10/5.0 (2.5)
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)	20/10	10/5.0 (2.5)
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)	20/10	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '192 and '193 are asynchronously presettable decade and 4-bit binary synchronous up/down (reversible) counters. The operating modes of the '192 decade counter and the '193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagram. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

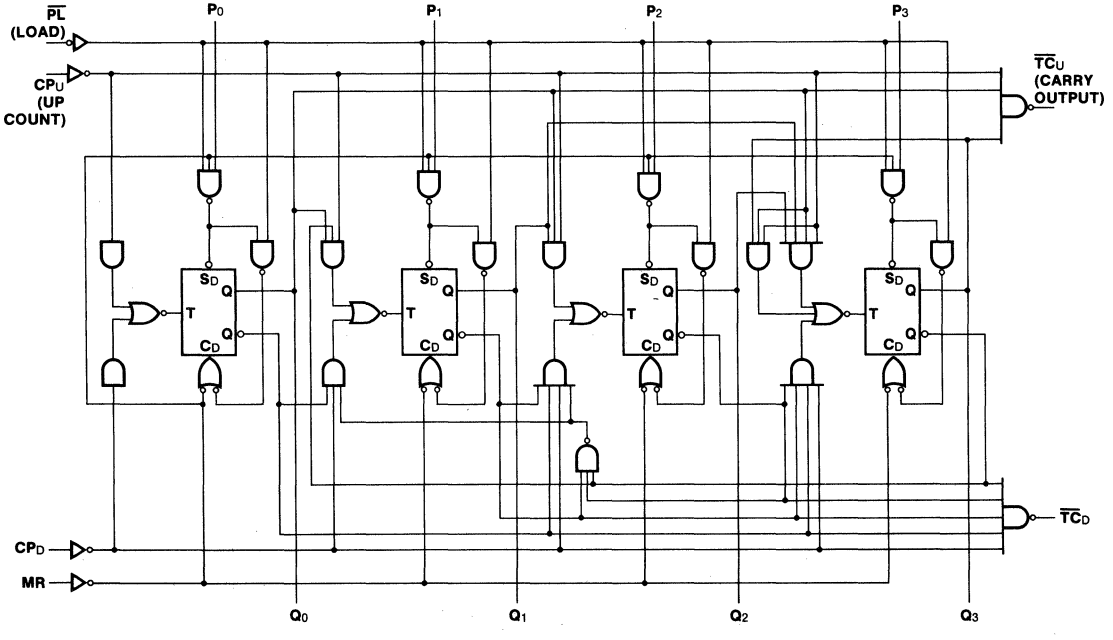
Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the '192, 15 for the '193), the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the $\overline{TC}$ outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

$$\overline{TC}_U = Q_0 \bullet Q_3 \bullet \overline{CP}_U$$
$$\overline{TC}_D = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet \overline{CP}_D$$

Each circuit has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P_0 — P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

LOGIC DIAGRAM

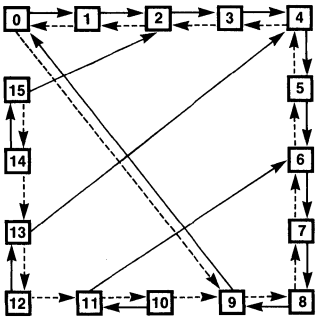


MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⎍	H	Count Up
L	H	H	⎍	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

STATE DIAGRAM



4

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	XM	-20	-65	-20	-100	mA	V_{CC} = Max
		XC	-18	-65	-20	-100		
I_{CC}	Power Supply Current	XM		89		34	mA	V_{CC} = Max; MR, $\overline{PL}$ = Gnd Other Inputs = 4.5 V
		XC		102		34		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
f_{max}	Maximum Count Frequency	25		30		MHz	Figs. 3-1, 3-8
t_{PLH}	Propagation Delay CP_U or CP_D to Q_n		38		31	ns	
t_{PHL}			47		28		
t_{PLH}	Propagation Delay CP_U to $\overline{TC_U}$		26		16	ns	Figs. 3-1, 3-5
t_{PHL}			24		21		
t_{PLH}	Propagation Delay CP_D to $\overline{TC_D}$		24		16		
t_{PHL}			24		24		
t_{PLH}	Propagation Delay P_n to Q_n				20	ns	Figs. 3-1, 3-5
t_{PHL}					30		
t_{PLH}	Propagation Delay $\overline{PL}$ to Q_n		40		32	ns	Figs. 3-1, 3-16
t_{PHL}			40		30		
t_{PHL}	Propagation Delay, MR to Q_n		35		25		

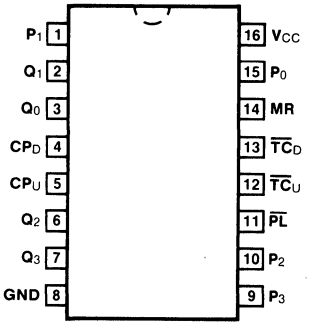
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n to $\overline{PL}$	20 20		20 10		ns	Fig. 3-13 $CP_U = CP_D$ = LOW
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n to $\overline{PL}$	0 3.0		3.0 3.0			
t_w (L)	CP Pulse Width LOW	20		17		ns	Fig. 3-8
t_w (L)	$\overline{PL}$ Pulse Width LOW	20		20		ns	Fig. 3-16
t_w (H)	MR Pulse Width HIGH	20		15			
t_{rec}	Recovery Time, MR to CP	6.0		3.0			
t_{rec}	Recovery Time, $\overline{PL}$ to CP	6.0		10			

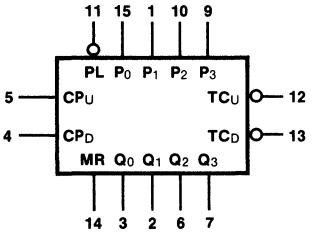
54/74193
54LS/74LS193
UP/DOWN BINARY COUNTER
(With Separate Up/down Clocks)

DESCRIPTION — The '193 is an up/down modulo-16 binary counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs. Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks. For functional description and detail specifications please refer to the '192 data sheet.

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74193PC, 74LS193PC		9B
Ceramic DIP (D)	A	74193DC, 74LS193DC	54193DM, 54LS193DM	6B
Flatpak (F)	A	74193FC, 74LS193FC	54193FM, 54LS193FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

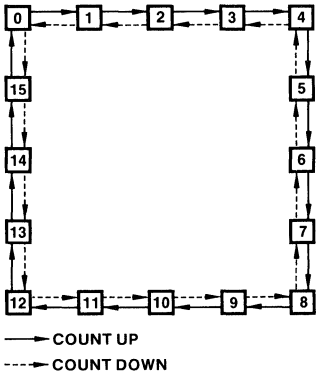
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
CP_U	Count Up Clock Input (Active Rising Edge)	1.0/1.0	0.5/0.25
CP_D	Count Down Clock Input (Active Rising Edge)	1.0/1.0	0.5/0.25
MR	Asynchronous Master Reset Input (Active HIGH)	1.0/1.0	0.5/0.25
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	0.5/0.25
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0	0.5/0.25
$Q_0 - Q_3$	Flip-flop Outputs	20/10	10/5.0 (2.5)
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)	20/10	10/5.0 (2.5)
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)	20/10	10/5.0 (2.5)

MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⌐¬	H	Count Up
L	H	H	⌐¬	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

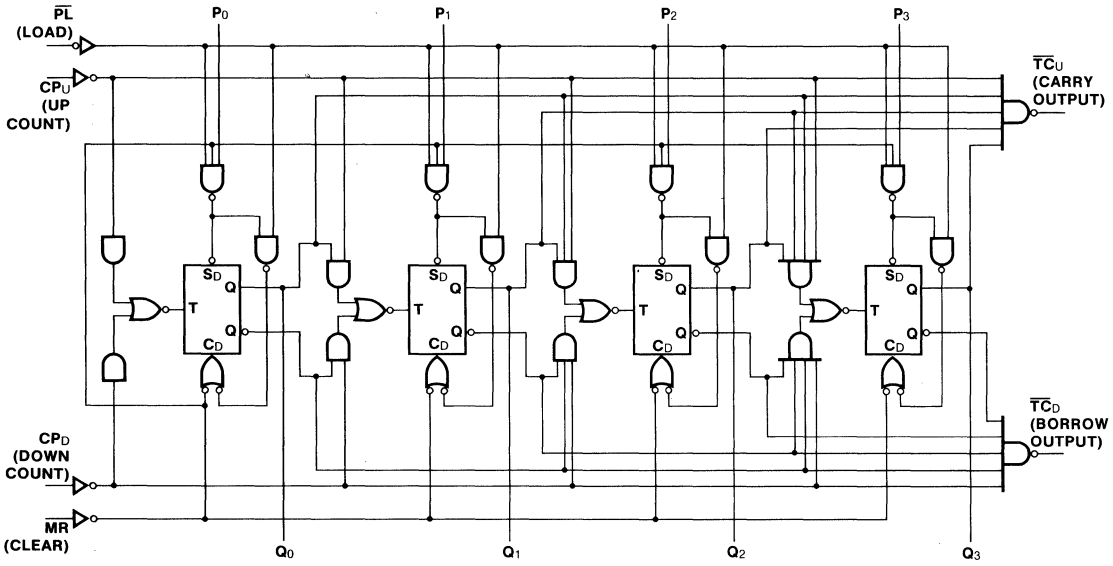
STATE DIAGRAM



LOGIC EQUATIONS FOR TERMINAL COUNT

$$\overline{TC}_U = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet \overline{CP}_U$$
$$\overline{TC}_D = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet \overline{CP}_D$$

LOGIC DIAGRAM



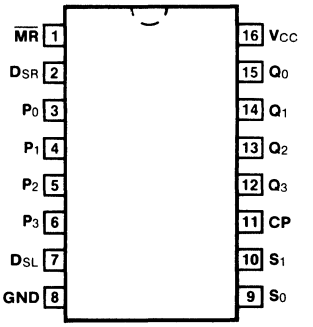
54/74194
54S/74S194
54LS/74LS194A

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

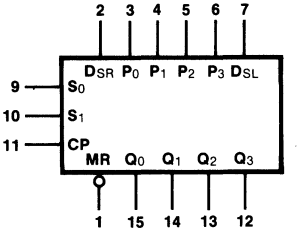
DESCRIPTION — The '194 is a high speed 4-bit bidirectional universal shift register. As a high speed multifunctional sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The '194 is similar in operation to the '195 universal shift register, with added features of shift left without external connections and hold (do nothing) modes of operation.

- **GUARANTEED SHIFT FREQUENCY OF 30 MHz ('LS194A) OR 70 MHz ('S194)**
- **ASYNCHRONOUS MASTER RESET**
- **HOLD (DO NOTHING) MODE**
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74194PC 74S194PC, 74LS194APC		9B
Ceramic DIP (D)	A	74194DC, 74S194DC, 74LS194ADC	54194DM 54S194DM, 54LS194ADM	6B
Flatpak (F)	A	74194FC, 74S194FC, 74LS194AFC	54194FM 54S194FM, 54LS194AFM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
S_0, S_1	Mode Control Inputs	1.0/1.0	1.25/1.25	0.5/0.25
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0	1.0/1.0	0.5/0.25
D_{SR}	Serial Data Input (Shift Right)	1.0/1.0	1.0/1.0	0.5/0.25
D_{SL}	Serial Data Input (Shift Left)	1.0/1.0	1.0/1.0	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	1.25/1.25	0.5/0.25
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	1.25/1.25	0.5/0.25
$Q_0 - Q_3$	Parallel Outputs	20/10	25/12.5	10/5.0 (2.5)

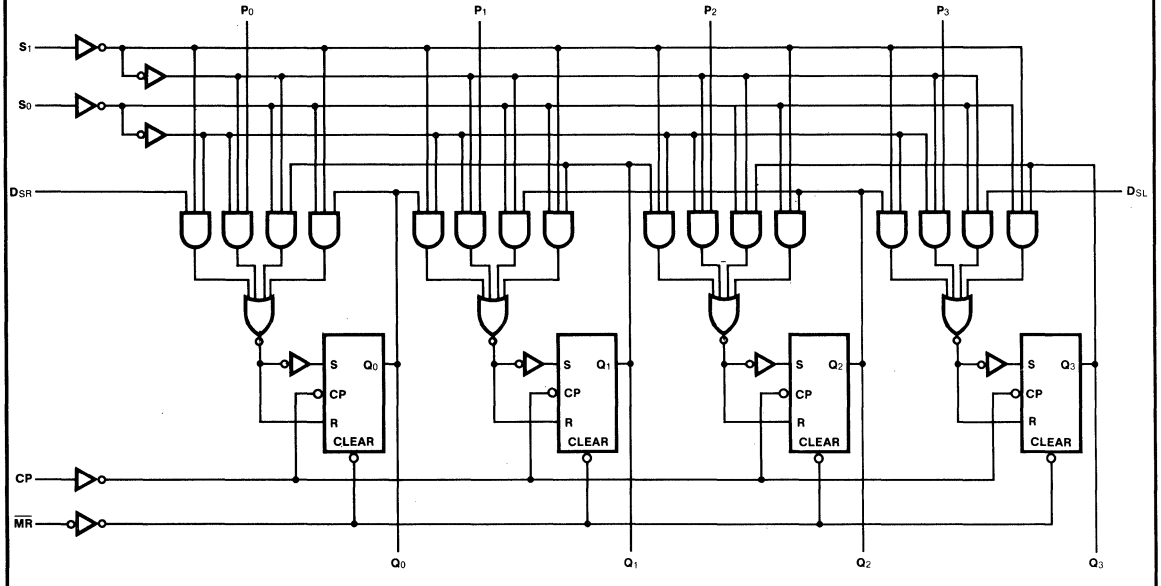
FUNCTIONAL DESCRIPTION — The '194 contains four edge-triggered D flip-flops and the necessary interstage logic to synchronously perform shift right, shift left, parallel load and hold operations. Signals applied to the Select (S_0, S_1) inputs determine the type of operation, as shown in the Mode Select Table. Signals on the Select, Parallel data (P_0 — P_3) and Serial data (D_{SR}, D_{SL}) inputs can change when the clock is in either state, provided only that the recommended setup and hold times, with respect to the clock rising edge, are observed. Synchronous state changes occur within 8.0 ns (typical, '194) or 15 ns (typical, 'LS194A), making the devices especially useful for implementing high speed memory or CPU buffer registers. A LOW signal on Master Reset ($\overline{MR}$) overrides all other inputs and forces the outputs LOW.

MODE SELECT TABLE

OPERATING MODE	INPUTS						OUTPUTS			
	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H	h	l	X	l	X	q_1	q_2	q_3	L
	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	H	l	h	l	X	X	L	q_0	q_1	q_2
	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	H	h	h	X	X	p_n	p_0	p_1	p_2	p_3

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
I_{CC}	Power Supply Current		63		135		23	mA	V_{CC} = Max S_n, $\overline{MR}$, D_{SR}, D_{SL} = 4.5 V P_n = Gnd CP = ⎍

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configuration)

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF R_L = 400 Ω		C_L = 15 pF R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max	Min	Max		
f_{max}	Maximum Shift Frequency	25		70		30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		22 26		8.0 12		21 24	ns	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		30		23		26	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

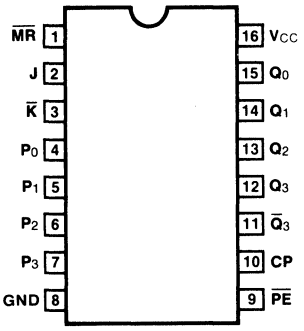
SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n or D_{SR} or D_{SL} to CP	20 20		6.0 6.0		16 16		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n or D_{SR} or D_{SL} to CP	0 0		0 0		0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW S_n to CP	30 30		9.0 9.0		25 25		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW S_n to CP	0 0		0 0		0 0		ns	
t_w (H)	CP Pulse Width HIGH	20		7.0		17		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		12		12		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	25		5.0		18		ns	

54/74195
54LS/74LS195A
UNIVERSAL 4-BIT SHIFT REGISTER

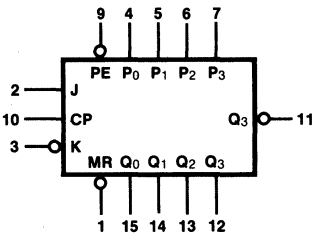
DESCRIPTION — The '195 is a high speed 4-bit shift register offering typical shift frequencies of 50 MHz. It is useful for a wide variety of register and counting applications. The '195 is pin and functionally identical to the 9300, 93L00 and 93H00.

- **TYPICAL SHIFT RIGHT FREQUENCY OF 50 MHz ('LS195A)**
- **ASYNCHRONOUS MASTER RESET**
- **J, $\overline{K}$ INPUTS TO FIRST STAGE**
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
Gnd = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74195PC, 74LS195APC		9B
Ceramic DIP (D)	A	74195DC, 74LS195ADC	54195DM, 54LS195ADM	6B
Flatpak (F)	A	74195FC, 74LS195AFC	54195FM, 54LS195AFM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0	0.5/0.25
P_0 — P_3	Parallel Data Inputs	1.0/1.0	0.5/0.25
J	First Stage J Input (Active HIGH)	1.0/1.0	0.5/0.25
$\overline{K}$	First Stage K Input (Active LOW)	1.0/1.0	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	0.5/0.25
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	0.5/0.25
Q_0 — Q_3	Parallel Outputs	20/10	10/5.0 (2.5)
$\overline{Q}_3$	Complementary Last Stage Output (Active LOW)	20/10	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The Logic Diagram and Truth Table indicate the functional characteristics of the '195 4-bit shift register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The '195 has two primary modes of operation, shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ input is HIGH, serial data enters the first flip-flop Q_0 via the J and $\overline{K}$ inputs and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The $J\overline{K}$ inputs provide the flexibility of the JK type input for special applications, and the simple D type input for general applications by tying the two pins together. When the $\overline{PE}$ input is LOW, the '195 appears as four common clocked D flip-flops. The data on the parallel inputs P_0, P_1, P_2, P_3 is transferred to the respective Q_0, Q_1, Q_2, Q_3 outputs following the LOW-to-HIGH clock transition. Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the P_{n-1} inputs and holding the $\overline{PE}$ input LOW.

All serial and parallel data transfers are synchronous, occuring after each LOW-to-HIGH clock transition. Since the '195 utilizes edge-triggering, there is no restriction on the activity of the J, $\overline{K}$, P_n and $\overline{PE}$ inputs for logic operation — except for the setup and release time requirements. A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

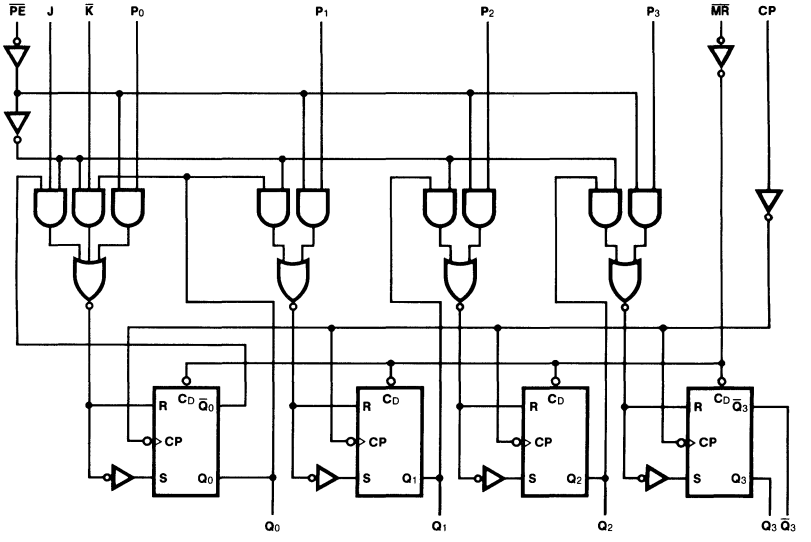
4

MODE SELECT† TABLE

OPERATING MODES	INPUTS					OUTPUTS				
	$\overline{MR}$	$\overline{PE}$	J	$\overline{K}$	P_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	l	X	X	p_n	p_0	p_1	p_2	p_3	$\overline{p}_3$

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial
l = LOW voltage level one setup time prior to the LOW to HIGH clock transition.
h = HIGH voltage level one setup time prior to the LOW to HIGH clock transition.
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW to HIGH clock transition.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		63		21	mA	V_{CC} = Max, $\overline{PE}$ = Gnd J, $\overline{K}$, P_n, $\overline{MR}$ = 4.5 V CP = ⎍

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω		54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	30		30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		22 26		21 24	ns	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q_n		30		26	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

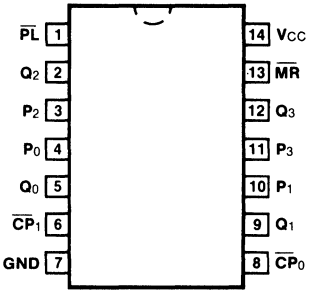
SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW J, $\overline{K}$ or P_n to CP	20 20		15 15		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW J, $\overline{K}$ or P_n to CP	0 0		0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{PE}$ to CP	25 25		25 25		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{PE}$ to CP	-10 -10		0 0		ns	
t_w (H)	CP Pulse Width HIGH	16		16		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	12		12		ns	Fig. 3-16
t_{rec}	Recovery Time, $\overline{MR}$ to CP	25		20		ns	

54/74196
54LS/74LS196
PRESETTABLE DECADE COUNTERS

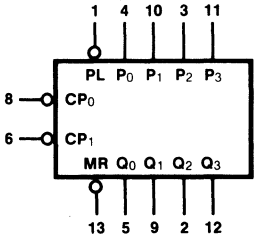
DESCRIPTION — The '196 decade ripple counter is partitioned into divide-by-two and divide-by-five sections which can be combined to count either in BCD (8421) sequence or in a bi-quinary mode producing a 50% duty cycle output. Both circuit types have a Master Reset ($\overline{MR}$) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ($\overline{PL}$) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops. This preset feature makes the circuits usable as programmable counters. The circuits can also be used as 4-bit latches, loading data from the Parallel Data inputs when $\overline{PL}$ is LOW and storing the data when $\overline{PL}$ is HIGH. In the counting modes, state changes are initiated by the falling edge of the clock.

- **HIGH COUNTING RATES — TYPICALLY 60 MHz**
- **CHOICE OF COUNTING MODES — BCD, BI-QUINARY, BINARY**
- **ASYNCHRONOUS PRESET AND MASTER RESET**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74196PC, 74LS196PC		9A
Ceramic DIP (D)	A	74196DC, 74LS196DC	54196DM, 54LS196DM	6A
Flatpak (F)	A	74196FC, 74LS196FC	54196FM, 54LS196FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CP_0}$	÷2 Section Clock Input (Active Falling Edge)	2.0/3.0	1.0/1.5
$\overline{CP_1}$	÷5 Section Clock Input (Active Falling Edge)	3.0/4.0	2.0/1.75
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	2.0/2.0	1.0/0.5
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0	0.5/0.25
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	0.5/0.25
$Q_0 - Q_3$*	Flip-flop Outputs*	20/10	10/5.0 (2.5)

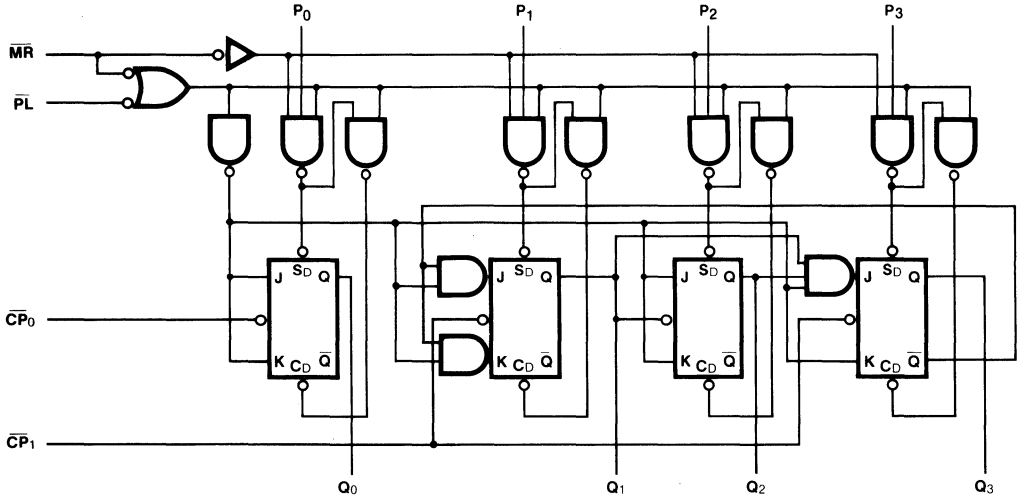
*Q_0 is guaranteed to drive the full rated fan-out plus the $\overline{CP_1}$ input.

FUNCTIONAL DESCRIPTION — The '196 and '197 are asynchronous presettable decade and binary ripple counters. The '196 decade counter is partitioned into divide-by-two and divide-by-five sections while the '197 is partitioned into divide-by-two and divide-by-eight sections, with all sections having a separate Clock input. In the counting modes, state changes are initiated by the HIGH-to-LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The $\overline{CP}_0$ input serves the Q_0 flip-flop in both circuit types while the $\overline{CP}_1$ input serves the divide-by-five or divide-by-eight section. The Q_0 output is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input. With the input frequency connected to $\overline{CP}_0$ and with Q_0 driving $\overline{CP}_1$, the '197 forms a straight forward modulo-16 counter, with Q_0 the least significant output and Q_3 the most significant output.

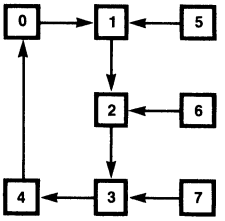
The '196 decade counter can be connected up to operate in two different count sequences. With the input frequency connected to $\overline{CP}_0$ and with Q_0 driving $\overline{CP}_1$, the circuit counts in the BCD (8421) sequence. With the input frequency connected to $\overline{CP}_1$ and Q_3 driving $\overline{CP}_0$, Q_0 becomes the low frequency output and has a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the latter (bi-quinary) configuration because of the interstage gating delay within the divide-by-five section.

The '196 and '197 have an asynchronous active LOW Master Reset input ($\overline{MR}$) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input ($\overline{PL}$) overrides the clock inputs and loads the data from Parallel Data ($P_0 - P_3$) inputs into the flip-flops. While $\overline{PL}$ is LOW, the counters act as transparent latches and any change in the P_n inputs will be reflected in the outputs. In order for the intended parallel data to be entered and stored, the recommended setup and hold times with respect to the rising edge of $\overline{PL}$ should be observed.

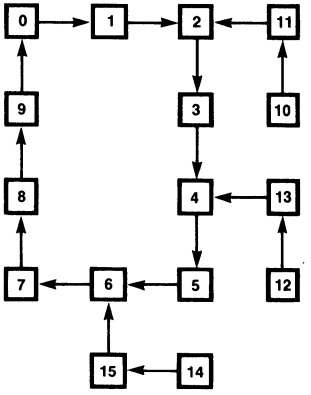
LOGIC DIAGRAM



÷5 STATE DIAGRAM



BCD STATE DIAGRAM



MODE SELECT TABLE

INPUTS			RESPONSE
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Q_n forced LOW
H	L	X	$P_n \rightarrow Q_n$
H	H	⊓	Count Up

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{IH}	Input HIGH Current	$\overline{CP_0}$		1.0		0.2	mA	V_{CC} = Max, V_{IN} = 5.5 V
		'196 $\overline{CP_1}$		1.0		0.4		
		'197 $\overline{CP_1}$		1.0		0.2		
I_{CC}	Power Supply Current			59		20	mA	V_{CC} = Max All Inputs = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER		54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
f_{max}	Maximum Count Frequency at $\overline{CP_0}$	'196 '197	50 50		45 50		MHz	Figs. 3-1, 3-9
f_{max}	Maximum Count Frequency at $\overline{CP_1}$	'196 '197	25 25		22.5 25		MHz	Fig. 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_0}$ to Q_0			12 15		12 12	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_1			18 21		14 14	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_2	'196		36 42		34 32	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_2	'197		36 42		36 34	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_3	'196		21 18		18 18	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_3	'197		54 63		50 55	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n			24 38		15 35	ns	Figs. 3-2, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n			33 36		24 35	ns	Figs. 3-1, 3-17
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n			37		37	ns	Figs. 3-1, 3-17

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

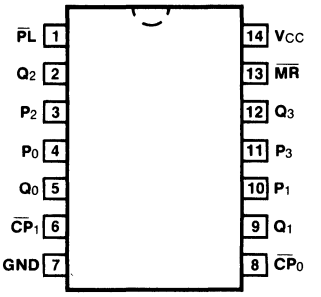
SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n to $\overline{PL}$		10 15		8.0 12		ns	Fig. 3-13
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n to $\overline{PL}$		0 0		0 6.0		ns	Fig. 3-13
t_w (H)	$\overline{CP_0}$ Pulse Width HIGH	'196 '197	20 20		12 10		ns	Fig. 3-9
t_w (H)	$\overline{CP_1}$ Pulse Width HIGH	'196 '197	30 30		24 20		ns	Fig. 3-9
t_w (L)	$\overline{PL}$ Pulse Width LOW		20		18		ns	Fig. 3-17
t_w (L)	$\overline{MR}$ Pulse Width LOW		15		12		ns	Fig. 3-17
t_{rec}	Recovery Time $\overline{PL}$ to $\overline{CP_n}$		20		16		ns	Fig. 3-17
t_{rec}	Recovery Time $\overline{MR}$ to $\overline{CP_n}$		20		18		ns	Fig. 3-17

54/74197
54LS/74LS197
PRESETTABLE BINARY COUNTERS

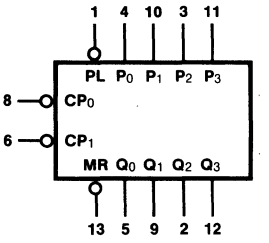
DESCRIPTION — The '197 ripple counter contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. State changes are initiated by the falling edge of the clock. The '197 has a Master Reset ($\overline{MR}$) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ($\overline{PL}$) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops.This preset feature makes the circuit usable as a programmable counter. The circuit can also be used as a 4-bit latch, loading data from the Parallel Data inputs when $\overline{PL}$ is LOW and storing the data when $\overline{PL}$ is HIGH. For detail specifications and functional description, please refer to the '196 data sheet.

- **HIGH COUNTING RATES — TYPICALLY 70 MHz**
- **ASYNCHRONOUS PRESET**
- **ASYNCHRONOUS MASTER RESET**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74197PC, 74LS197PC		9A
Ceramic DIP (D)	A	74197DC, 74LS197DC	54197DM, 54LS197DM	6A
Flatpak (F)	A	74197FC, 74LS197FC	54197FM, 54LS197FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CP_0}$	÷2 Section Clock Input (Active Falling Edge)	2.0/3.0	1.0/1.5
$\overline{CP_1}$	÷8 Section Clock Input (Active Falling Edge)	2.0/2.0	1.0/0.81
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	2.0/2.0	1.0/0.5
P_0 — P_3	Parallel Data Inputs	1.0/1.0	0.5/0.25
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	0.5/0.25
Q_0	÷2 Section Output*	20/10	10/5.0 (2.5)
Q_1 — Q_3	÷8 Section Outputs	20/10	10/5.0 (2.5)

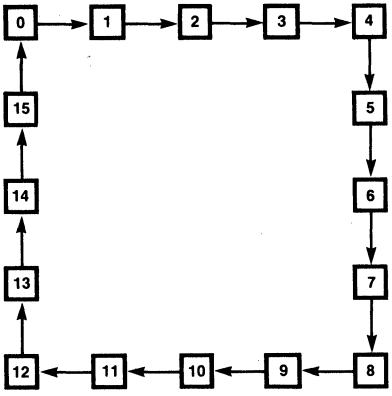
*Q_0 output is guaranteed to drive the full rated fan-out plus the $\overline{CP_1}$ input.

MODE SELECTION TABLE

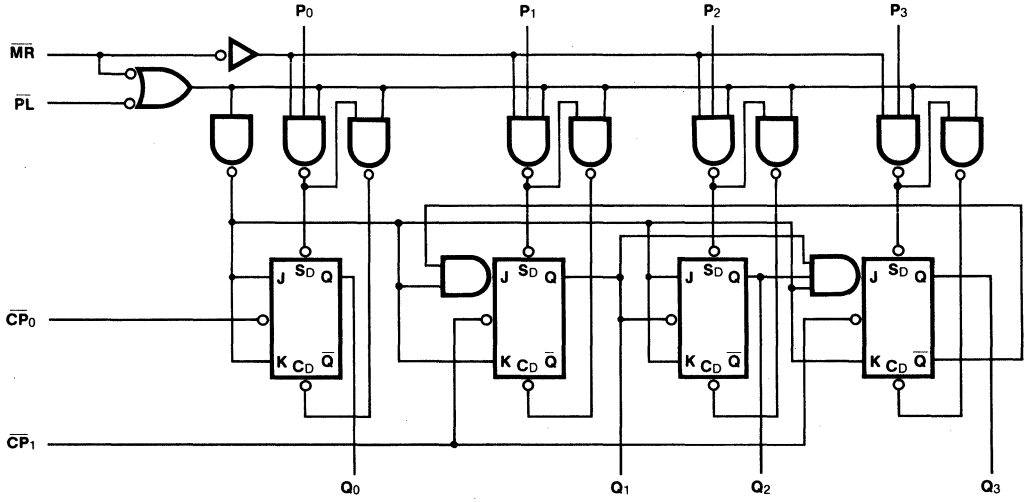
INPUTS			RESPONSE
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Q_n forced LOW
H	L	X	$P_n \rightarrow Q_n$
H	H	⌐_	Count Up

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

÷ 16 STATE DIAGRAM



LOGIC DIAGRAM



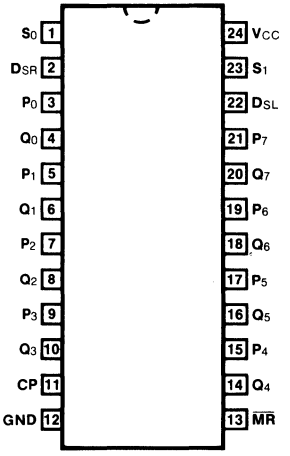
54/74198

8-BIT R/L SHIFT REGISTER

DESCRIPTION — The '198 features synchronous parallel load, hold, shift right and shift left modes, as determined by the Select (S_0, S_1) inputs. State changes are initiated by the rising edge of the clock. An asynchronous Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register. The '198 is useful for serial-serial, serial-parallel, parallel-serial and parallel-parallel register transfers.

- **PARALLEL IN/PARALLEL OUT**
- **SYNCHRONOUS PARALLEL LOAD**
- **SHIFT RIGHT AND SHIFT LEFT CAPABILITY**
- **ASYNCHRONOUS OVERRIDING CLEAR**

CONNECTION DIAGRAM
PINOUT A



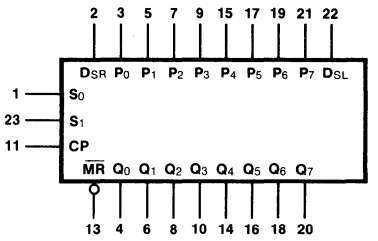
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74198PC		9N
Ceramic DIP (D)	A	74198DC	54198DM	6N
Flatpak (F)	A	74198FC	54198FM	4M

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
S_0, S_1	Mode Select Inputs	1.0/1.0
P_0 — P_7	Parallel Data Inputs	1.0/1.0
D_{SR}	Serial Data Input (Shift Right)	1.0/1.0
D_{SL}	Serial Data Input (Shift Left)	1.0/1.0
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0
Q_0 — Q_7	Flip-flop Outputs	20/10

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

FUNCTIONAL DESCRIPTION — The '198 contains eight edge-triggered D-type flip-flops and the interstage gating required to perform synchronous parallel load, shift right, and shift left operations. Serial data enters at D_{SR} for shift right and at D_{SL} for shift left operations. Parallel data is applied to the $P_0 - P_7$ inputs. State changes are initiated by the rising edge of the clock. The D_{SR}, D_{SL} and $P_0 - P_7$ inputs can change when the clock is in either state, provided only that the recommended setup and hold times are observed.

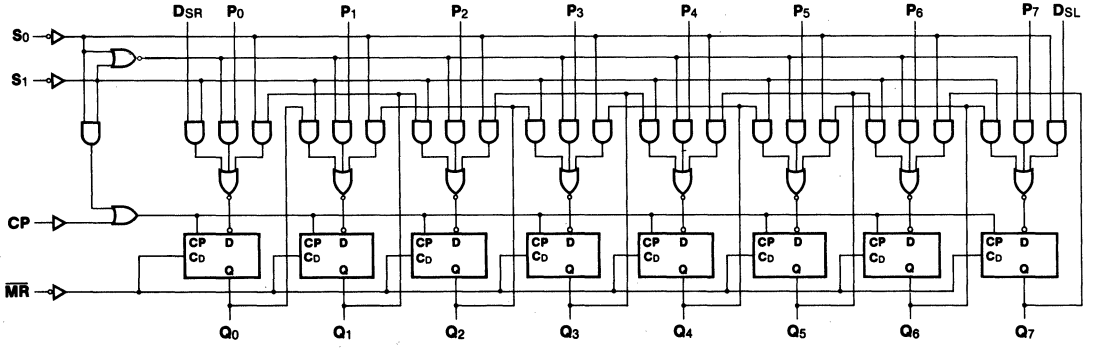
The operating mode is determined by S_0 and S_1, as shown in the Mode Select Table. Clocking of the flip-flops is inhibited when both S_0 and S_1 are LOW. To avoid inadvertently clocking the register, the Select inputs should only be changed while CP is HIGH. A LOW signal on $\overline{MR}$ overrides all other inputs and forces the outputs LOW.

MODE SELECT TABLE

INPUTS				RESPONSE
$\overline{MR}$	CP	S_0*	S_1*	
L	X	X	X	Asynchronous Reset; Outputs = LOW
H	↑	H	H	Parallel Load; $P_n \rightarrow Q_n$
H	↑	L	H	Shift Right; $D_{SR} \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	↑	H	L	Shift Left; $D_{SL} \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	X	L	L	Hold

*Select inputs should be changed only while CP is HIGH
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XC		116	mA	V_{CC} = Max; S_0, S_1 = 4.5 V
		XM		104		CP = ⌐¬ ; $\overline{MR}$, P_n = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 C_L = 15 pF, R_L = 400 Ω Max	UNITS	CONDITIONS
f_{max}	Maximum Shift Frequency	25		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		26 30	ns	Figs. 3-1, 3-8
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		35	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n, D_{SL}, D_{SR} to CP	20 20		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n, D_{SL}, D_{SR} to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW S_0 or S_1 to CP	30 30		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW S_0 or S_1 to CP	0 0		ns	
t_w (H)	CP Pulse Width HIGH	20		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		ns	Fig. 3-16

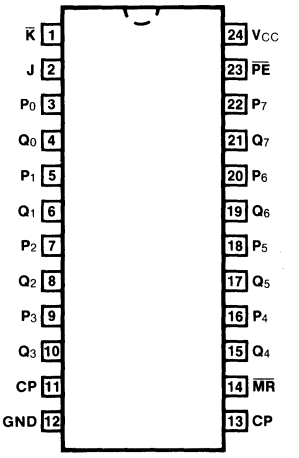
54/74199

8-BIT PARALLEL I/O SHIFT REGISTER

DESCRIPTION — The '199 is a parallel in, parallel out register featuring synchronous parallel load, shift right and hold modes. State changes are initiated by the rising edge of the clock. Serial entry into the first stage is via J and $\overline{K}$ inputs for maximum flexibility. Two clock inputs are provided and it is possible to use one as an inhibit. An asynchronous Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register.

- **PARALLEL IN/PARALLEL OUT**
- **SYNCHRONOUS PARALLEL LOAD**
- **ASYNCHRONOUS OVERRIDING CLEAR**
- **J$\overline{K}$ ENTRY TO FIRST STAGE**

CONNECTION DIAGRAM
PINOUT A



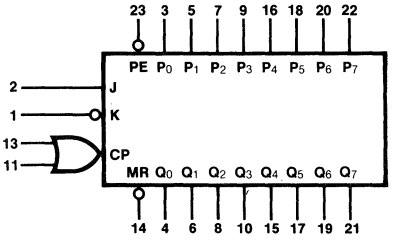
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74199PC		9N
Ceramic DIP (D)	A	74199DC	54199DM	6N
Flatpak (F)	A	74199FC	54199FM	4M

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\overline{K}$	Serial Data Input (Active LOW)	1.0/1.0
J	Serial Data Input (Active HIGH)	1.0/1.0
P_0 — P_7	Parallel Data Inputs	1.0/1.0
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0
Q_0 — Q_7	Flip-flop Outputs	20/10

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

FUNCTIONAL DESCRIPTION — The '199 contains eight edge-triggered D-type flip-flops and the interstage gating required to perform synchronous parallel load and shift right operations. Parallel input data is applied to the P_0 — P_7 inputs, while serial entry to Q_0 is via J and $\overline{K}$. State changes are initiated by the rising edge of the clock. The J, $\overline{K}$, P_0 — P_7 and $\overline{PE}$ inputs can change while the clock is in either state, provided only that the recommended setup and hold times are observed.

Either CP input can be used as the clock; if one is not used it must be tied LOW. One CP input can be used to inhibit the other by applying a HIGH signal, but this should only be done while the other CP is in the HIGH state or else false triggering may result. A LOW signal on $\overline{MR}$ overrides all other inputs and forces the outputs LOW.

MODE SELECT TABLE

INPUTS				RESPONSE
$\overline{MR}$	$\overline{PE}$	CP_1*	CP_2*	
L	X	X	X	Asynchronous Reset; Outputs = LOW
H H	X X	H X	X H	Hold
H H	L L	L ↓	↓ L	Parallel Load; $P_n \longrightarrow Q_n$
H H	H H	L ↓	↓ L	Shift Right, $Q_0 \longrightarrow Q_1$, $Q_1 \longrightarrow Q_2$, etc.

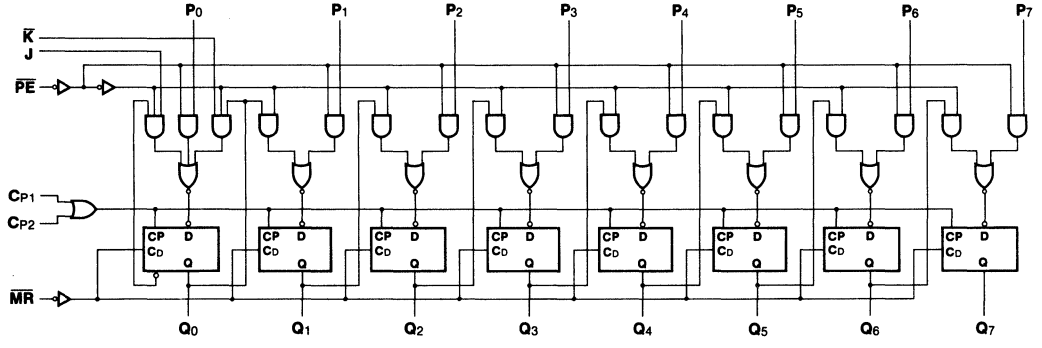
*See discussion for precautions on CP changes
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

SERIAL ENTRY TABLE
($\overline{MR}$ = $\overline{PE}$ = HIGH)

INPUTS		Q_0 at t_{n+1}*
J	$\overline{K}$	
L	L	L
L	H	Q_0 at t_n (No Change)
H	L	$\overline{Q}_0$ at t_n (Toggles)
H	H	H

*t_n, t_{n+1} = time before, after rising CP edge

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XC		116	mA	V_{CC} = Max; J, $\overline{K}$, P_n = 4.5 V CP_1 = ⎍⎍ CP_2, $\overline{MR}$, $\overline{PE}$ = Gnd
		XM		104		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 C_L = 15 pF, R_L = 400 Ω Max	UNITS	CONDITIONS
f_{max}	Maximum Shift Frequency	25		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP_1 or CP_2 to Q_n		26 30	ns	Figs. 3-1, 3-8
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		35	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n, $\overline{K}$, J to CP	20 20		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n, $\overline{K}$, J to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{PE}$ to CP	30 30		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{PE}$ to CP	0 0		ns	
t_w (H)	CP Pulse Width HIGH	20		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		ns	Fig. 3-16

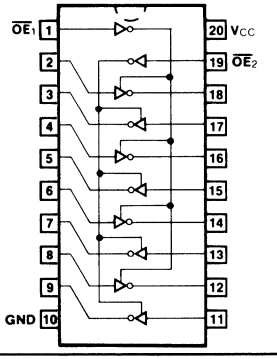
54S/74S240 • 54LS/74LS240
54S/74S241 • 54LS/74LS241
54LS/74LS244

OCTAL BUFFER/LINE DRIVER

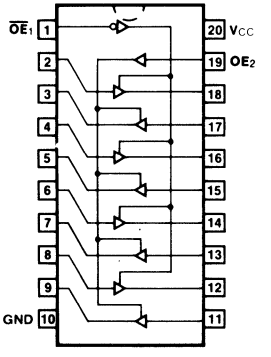
(With 3-State Outputs)

CONNECTION DIAGRAMS

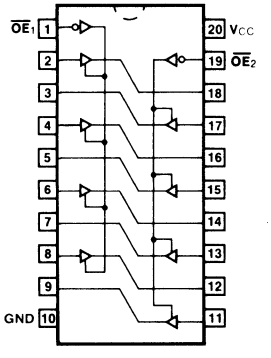
PINOUT A



PINOUT B



PINOUT C



DESCRIPTION — The '240, '241 and '244 are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers and bus oriented transmitters/receivers which provide improved PC board density.

- **HYSTERESIS AT INPUTS TO IMPROVE NOISE MARGINS**
- **3-STATE OUTPUTS DRIVE BUS LINES OR BUFFER MEMORY ADDRESS REGISTERS**
- **OUTPUTS SINK 24 mA (74LS) OR 40 mA(74S)**
- **15 mA SOURCE CURRENT**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V, ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V, ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S240PC, 74LS240PC		9Z
	B	74S241PC, 74LS241PC		
	C	74LS244PC		
Ceramic DIP (D)	A	74S240DC, 74LS240DC	54S240DM, 54LS240DM	4E
	B	74S241DC, 74LS241DC	54S241DM, 54LS241DM	
	C	74LS244DC	54LS244DM	
Flatpak (F)	A	74S240FC, 74LS240FC	54S240FM, 54LS240FM	4F
	B	74S241FC, 74LS241FC	54S241FM, 54LS241FM	
	C	74LS244FC	54LS244FM	

INPUT LOADING/FAN-OUT: See Section 9

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable (Active LOW)	1.25/1.25	0.5/0.25
OE_2	3-State Output Enable (Active HIGH)	1.25/1.25	0.5/0.25
	Inputs	1.25/0.25	0.5/0.125
	Outputs	75/40 (30)	75/15 (7.5)

TRUTH TABLES

'S240, 'LS240

INPUTS			OUTPUT
$\overline{OE_1}$, $\overline{OE_2}$		D	
L		L	H
L		H	L
H		X	Z

'S241, 'LS241

INPUTS			OUTPUT
$\overline{OE_1}$	OE_2	D	
L	H	L	L
L	H	H	H
H	L	X	Z

'LS244

INPUTS			OUTPUT
$\overline{OE_1}$, $\overline{OE_2}$		D	
L		L	L
L		H	H
H		X	Z

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	DESCRIPTION				54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage			XM	2.0		2.0		V	I_{OH} = -12 mA, V_{IH} = 2.0 V, V_{IL} = 0.5 V
				XC	2.0		2.0			I_{OH} = -15 mA, V_{CC} = Min
				XM	2.4		2.4		V	V_{CC} = Min, V_{IH} = 2.0 V, V_{IL} = Max, I_{OH} = -3.0 mA
				XC	2.4		2.4			
				XC	2.7		2.7		V	V_{CC} = Min, V_{IH} = 2.0 V, V_{IL} = Max, I_{OH} = -1.0 mA
V_{OL}	Output LOW Voltage			XM				0.4	V	I_{OL} = 12 mA, V_{CC} = Min
				XC				0.4		I_{OL} = 12 mA, V_{CC} = Min
				XC				0.5		I_{OL} = 24 mA, V_{CC} = Min
				XM		0.55			V	I_{OL} = 48 mA, V_{CC} = Min
				XC		0.55				I_{OL} = 64 mA, V_{CC} = Min
I_{OS}	Output Short Circuit Current				-50	-225	-40	-225	mA	V_{CC} = Max
I_{CC}	Power Supply Current	HIGH	('240)	XM		123		23	mA	V_{CC} = Max
				XC		135		23		
			('241)	XM		147		23		
				XC		160		23		
			('244)	XM				23		
				XC				23		
		LOW	('240)	XM		145		44	mA	V_{CC} = Max
				XC		150		44		
			('241)	XM		170		46		
				XC		180		46		
			('244)	XM				46		
				XC				46		
		OFF	('240)	XM		145		50	mA	V_{CC} = Max
				XC		150		50		
			('241)	XM		170		54		
				XC		180		54		
			('244)	XM				54		
				XC				54		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S C_L = 50 pF, R_L = 90 Ω Min	54/74S Max	54/74LS C_L = 50 pF Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('240)		7.0 7.0		14 18	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('241)		9.0 9.0		18 18	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('244)				18 18	ns	
t_{PZH} t_{PZL}	Output Enable Time ('S240)		10 15			ns	Figs. 3-3, 3-11, 3-12
t_{PZH} t_{PZL}	Output Enable Time ('LS240, 'LS241, 'S241)		12 15		23 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω ('LS)
t_{PLZ} t_{PHZ}	Output Disable Time		15 9.0		25 18	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 5 pF ('LS)

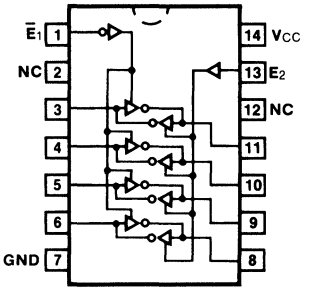
4

54LS/74LS242
54LS/74LS243

QUAD BUS TRANSCEIVER

(With 3-State Outputs)

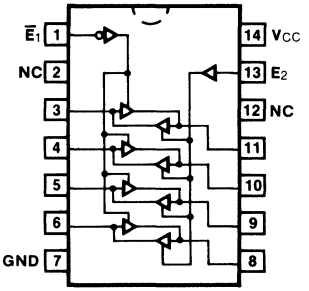
CONNECTION DIAGRAMS
PINOUT A



DESCRIPTION — The 'LS242 and '243 are quad bus transmitters/receivers designed for 4-line asynchronous 2-way data communications between data buses.

- **HYSTERESIS AT INPUTS TO IMPROVE NOISE IMMUNITY**
- **2-WAY ASYNCHRONOUS DATA BUS COMMUNICATION**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PINOUT B



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS242PC		9A
	B	74LS243PC		
Ceramic DIP (D)	A	74LS242DC	54LS242DM	6A
	B	74LS243DC	54LS243DM	
Flatpak (F)	A	74LS242FC	54LS242FM	3I
	B	74LS243FC	54LS243FM	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74LS (U.L.) HIGH/LOW
Inputs	0.5/0.125
Outputs	75/15 (7.5)

TRUTH TABLES

'LS242

INPUTS		OUTPUT
$\overline{E}_1$	D	
L	L	H
L	H	L
H	X	Z
H	X	Z

INPUTS		OUTPUT
E_2	D	
L	X	Z
L	X	Z
H	L	H
H	H	L

'LS243

INPUTS		OUTPUT
$\overline{E}_1$	D	
L	L	L
L	H	H
H	X	Z
H	X	Z

INPUTS		OUTPUT
E_2	D	
L	X	Z
L	X	Z
H	L	L
H	H	H

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	XM	2.0		V	I_{OH} = -12 mA	V_{CC} = Min, V_{IH} = 2.0 V, V_{IL} = 0.5 V
		XC	2.0			I_{OH} = -15 mA	
V_{OH}	Output HIGH Voltage		2.4		V	I_{OH} = -3.0 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} per Truth Table	
I_{OS}	Output Short Circuit Current		-40	-225	mA	V_{CC} = Max, V_{OUT} = 0 V	
I_{CC}	Power Supply Current	HIGH		38	mA	V_{CC} = Max	
		LOW		50			
		OFF ('242)		50			
		OFF ('243)		54			

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 45 pF Min	54/74LS C_L = 45 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('242)		14 18	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('243)		18 18	ns	Figs. 3-1, 3-5
t_{PZH} t_{PZL}	Output Enable Time		23 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω
t_{PLZ} t_{PHZ}	Output Disable Time		25 18	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 5 pF

54LS/74LS245

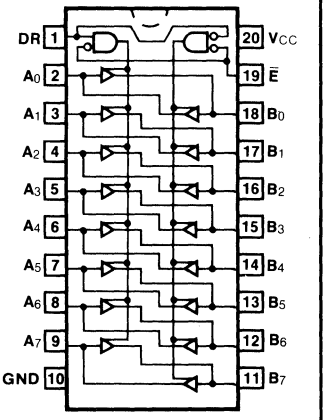
OCTAL BUS TRANSCEIVER

(With 3-State Outputs)

DESCRIPTION — The 'LS245 is an octal bus transmitter/receiver designed for 8-line asynchronous 2-way data communication between data busses. Direction input (DR) controls transmission of data from bus A to bus B or bus B to bus A depending upon its logic level. The Enable input ($\overline{E}$) can be used to isolate the busses.

- **HYSTERESIS INPUTS TO IMPROVE NOISE IMMUNITY**
- **2-WAY ASYNCHRONOUS DATA BUS COMMUNICATION**
- **INPUT DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74LS245PC		9Z
Ceramic DIP (D)	A	74LS245DC	54LS245DM	4E
Flatpak (F)	A	74LS245FC	54LS245FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	**54/74LS (U.L.)** HIGH/LOW
Inputs	0.5/0.125
Outputs	75/15 (7.5)

TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	DR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYBMOL	PARAMETER		54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	XM	2.0		V	I_{OH} = -12 mA	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} per Truth Table
		XC	2.0			I_{OH} = -15 mA	
V_{OH}	Output HIGH Voltage		2.4		V	I_{OH} = -3.0 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} per Truth Table	
$V_{T+} - V_{T-}$	Hysteresis Voltage		0.2		V	V_{CC} = Min	
I_{OS}	Output Short Circuit Current		-40	-225	mA	V_{CC} = Max, V_{OUT} = 0 V	
I_{CC}	Power Supply Current	HIGH		70	mA	V_{CC} = Max	
		LOW		90			
		OFF		95			

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 45 pF Min	54/74LS C_L = 45 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay Data to Output		18 18	ns	Figs. 3-1, 3-5
t_{PZH} t_{PZL}	Output Enable Time		25 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω
t_{PLZ} t_{PHZ}	Output Disable Time		25 18	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 5 pF

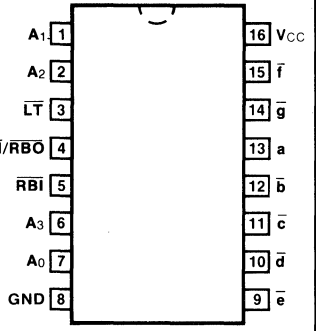
4

54LS/74LS247

BCD TO 7-SEGMENT DECODER/DRIVER

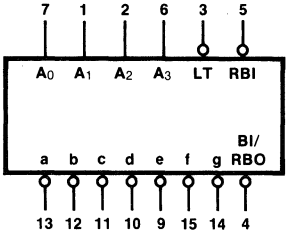
(With Open-Collector Outputs)

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The 'LS247 has active LOW open-collector outputs guaranteed to sink 12 mA (Military) or 24 mA (Commercial). It has the same electrical characteristics and pin connections as the 'LS47. The only difference is that the 'LS247 will light the top bar (segment a) for numeral 6 and the bottom bar (segment d) for numeral 9. For detailed description and specifications please refer to the 'LS47 data sheet.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS247PC		9B
Ceramic DIP (D)	A	74LS247DC	54LS247DM	6B
Flatpak (F)	A	74LS247FC	54LS247FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	BCD Inputs	0.5/0.25
$\overline{RBI}$	Ripple Blanking Input (Active LOW)	0.5/0.25
$\overline{LT}$	Lamp Test Input (Active LOW)	0.5/0.25
$\overline{BI/RBO}$	Blanking Input (Active LOW) or	0.5/0.25
	Ripple Blanking Output (Active LOW)	1.25/2.0 (1.0)
$\bar{a} - \bar{g}$	Segment Outputs (Active LOW)	OC*/15 (7.5)

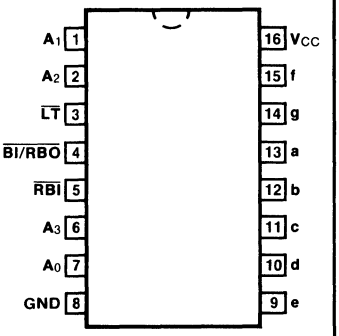
*OC — Open Collector

54LS/74LS248

BCD TO 7-SEGMENT DECODER

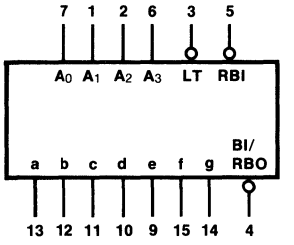
(With 2 kΩ Pull-up Resistors)

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The 'LS248 has active HIGH outputs with internal 2 kΩ pull-up resistors. It has the same electrical characteristics and pin connections as the 'LS48. The only difference is that the 'LS248 will light the top bar (segment a) for numeral 6 and the bottom bar (segment d) for numeral 9. For detailed description and specifications please refer to the 'LS48 data sheet.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS248PC		9B
Ceramic DIP (D)	A	74LS248DC	54LS248DM	6B
Flatpak (F)	A	74LS248FC	54LS248FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

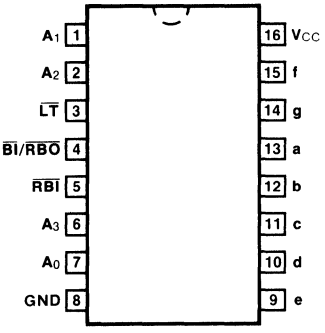
PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	BCD Inputs	0.5/0.25
$\overline{RBI}$	Ripple Blanking Input (Active LOW)	0.5/0.25
$\overline{LT}$	Lamp Test Input (Active LOW)	0.5/0.25
$\overline{BI/RBO}$	Blanking Input (Active LOW) or	0.5/0.25
	Ripple Blanking Output (Active LOW)	1.25/2.0 (1.0)
a — g	Segment Outputs (Active HIGH)	2.5/3.75 (1.25)

54LS/74LS249

BCD TO 7-SEGMENT DECODER

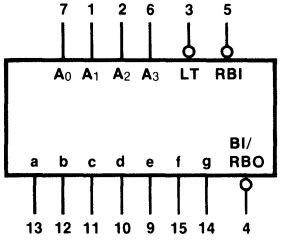
(With Open-Collector Outputs)

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The 'LS249 has active HIGH open-collector outputs and is the 16-pin version of the 14-pin 'LS49. The 'LS249 incorporates the Lamp Test and $\overline{BI/RBO}$ inputs that are omitted in the 'LS49. Additionally, the 'LS249 will light the top bar (segment a) for numeral 6 and the bottom bar (segment d) for numeral 9. For detailed description and specifications please refer to the 'LS49 data sheet.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	A	74LS249PC		9B
Ceramic DIP (D)	A	74LS249DC	54LS249DM	6B
Flatpak (F)	A	74LS249FC	54LS249FM	4L

INPTU LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	BCD Inputs	0.5/0.25
$\overline{BI}$	Blanking Input (Active LOW)	0.5/0.25
$\overline{LT}$	Lamp Test Input (Active LOW)	0.5/0.25
$\overline{BI/RBO}$	Blanking Input (Active LOW) or	0.5/0.25
	Ripple Blanking Output (Active LOW)	1.25/2.0 (1.0)
a — g	Segment Outputs (Active HIGH)	OC*/5.0 (2.5)

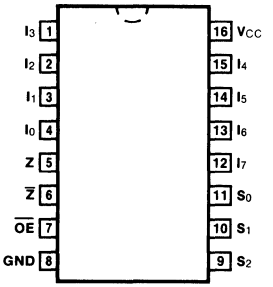
*OC — Open Collector

54S/74S251
54LS/74LS251

8-INPUT MULTIPLEXER

(With 3-State Outputs)

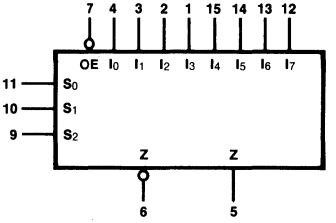
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '251 is a high speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- **MULTIFUNCTIONAL CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **INVERTING AND NON-INVERTING 3-STATE OUTPUTS**

LOGIC SYMBOL



VCC = Pin 16
GND 4 Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S251PC, 74LS251PC		9B
Ceramic DIP (D)	A	74S251DC, 74LS251DC	54S251DM, 54LS251DM	6B
Flatpak (F)	A	74S251FC, 74LS251FC	54S251FM, 54LS251FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. defintions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$S_0 - S_2$	Select Inputs	1.25/1.25	0.5/0.25
$\overline{OE}$	3-State Output Enable Inputs (Active LOW)	1.25/1.25	0.5/0.25
$I_0 - I_7$	Multiplexer Input	1.25/1.25	0.5/0.25
Z	Multiplexer Output	162/12.5 (50)	65/5.0 (25)/(2.5)
$\overline{Z}$	Complementary Multiplexer Output	162/12.5 (50)	65/5.0 (25)/(2.5)

FUNCTIONAL DESCRIPTION — This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Output Enable input ($\overline{OE}$) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

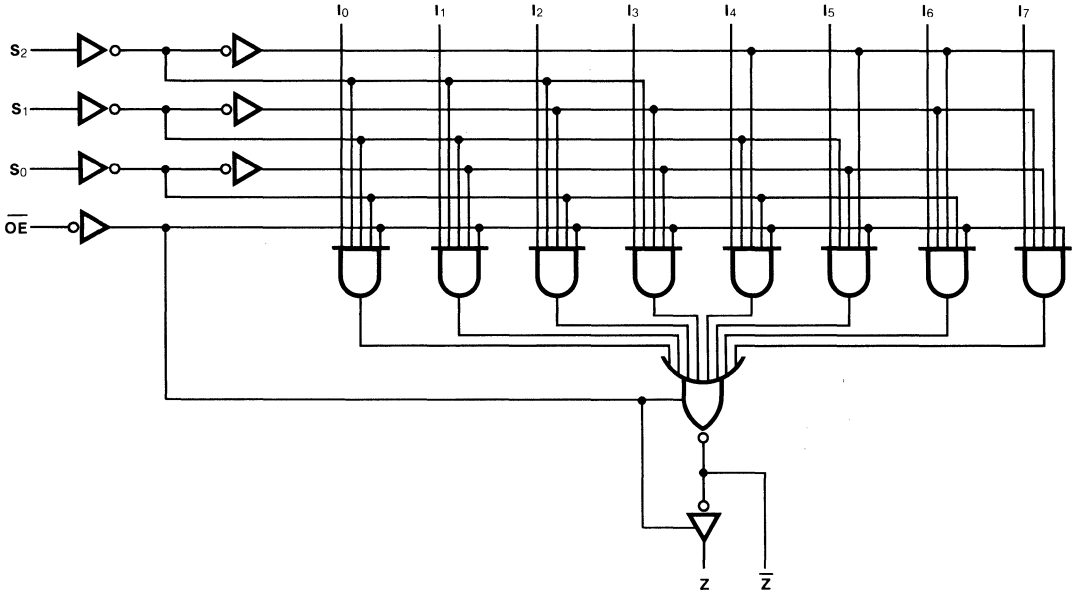
When the Output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{OE}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	$\overline{Z}$	Z
L	L	L	L	$\overline{I_0}$	I_0
L	L	L	H	$\overline{I_1}$	I_1
L	L	H	L	$\overline{I_2}$	I_2
L	L	H	H	$\overline{I_3}$	I_3
L	H	L	L	$\overline{I_4}$	I_4
L	H	L	H	$\overline{I_5}$	I_5
L	H	H	L	$\overline{I_6}$	I_6
L	H	H	H	$\overline{I_7}$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current		-40	-100	-20	-100	mA	V_{CC} = Max
I_{CC}	Power Supply Current	Outputs ON				10	mA	V_{CC} = Max; I_n, S_n = 4.5 V; $\overline{OE}$ = Gnd
		Outputs OFF		85		12		V_{CC} = Max; $\overline{OE}$, I_n = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S C_L = 15 pF, R_L = 280 Ω Min	54/74S Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}$		15 13.5		23 33	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay S_n to Z		18 19.5		45 30	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay I_n to Z		12 12		28 26	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}$		7.0 7.0		15 15	ns	Figs. 3-1, 3-4
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$		19.5 21		20 25	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS251)
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$		8.5 14		25 20	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS251) C_L = 5 pF

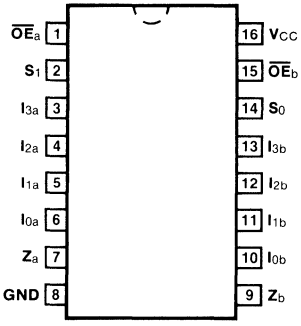
4

54S/74S253
54LS/74LS253

DUAL 4-INPUT MULTIPLEXER

(With 3-State Outputs)

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '253 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **NON-INVERTING 3-STATE OUTPUTS**

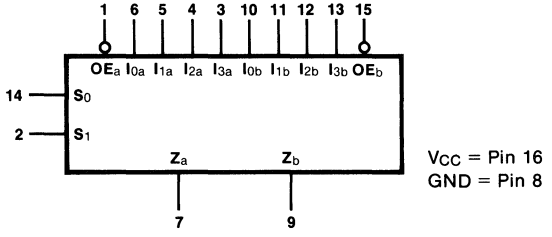
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74S253PC, 74LS253PC		9B
Ceramic DIP (D)	A	74S253DC, 74LS253DC	54S253DM, 54LS253DM	6B
Flatpak (F)	A	74S253FC, 74LS253FC	54S253FM, 54LS253FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
I_{0a} — I_{3a}	Side A Data Inputs	1.25/1.25	0.5/0.25
I_{0b} — I_{3b}	Side B Data Inputs	1.25/1.25	0.5/0.25
S_0, S_1	Common Select Inputs	1.25/1.25	0.5/0.25
$\overline{OE}_a$	Side A Output Enable Input (Active LOW)	1.25/1.25	0.5/0.25
$\overline{OE}_b$	Side B Output Enable Input (Active LOW)	1.25/1.25	0.5/0.25
Z_a, Z_b	3-State Outputs	162/12.5 (50)	65/5.0 (25)/(2.5)

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — This device contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which when HIGH, force the outputs to a high impedance (high Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$Z_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

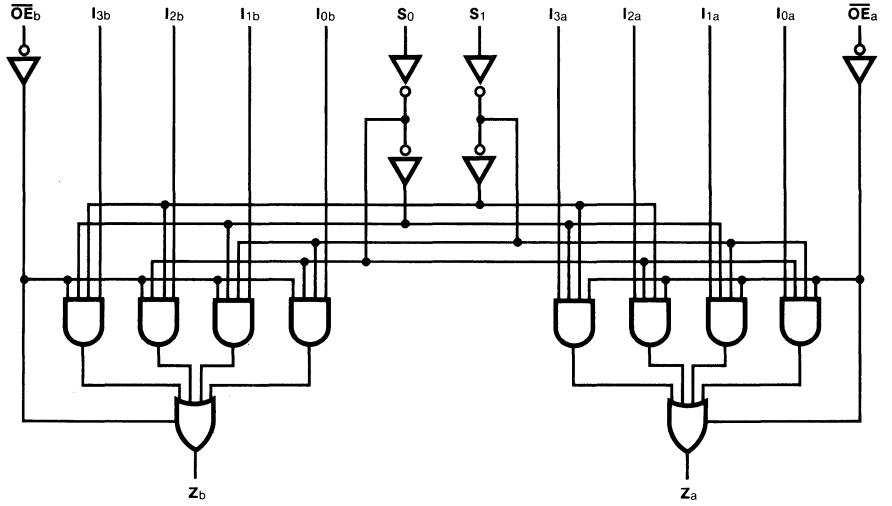
If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs S_0 and S_1 are common to both sections.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z)= High Impedance

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current		-40	-100	-20	-100	mA	V_{CC} = Max
I_{CC}	Power Supply Current	Outputs HIGH		70			mA	V_{CC} = Max, $\overline{OE}_n$ = Gnd I_n, S_n = 4.5 V
		Outputs LOW		80		12		V_{CC} = Max I_n, S_n, $\overline{OE}_n$ = Gnd
		Outputs OFF		100		14		V_{CC} = Max, $\overline{OE}_n$ = 4.5 V I_n, S_n = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S C_L = 15 pF, R_L = 280 Ω Min	54/74S Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay S_n to Z_n		18 18		29 24	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n		9.0 9.0		20 15	ns	Figs. 3-1, 3-5
t_{PZH} t_{PZL}	Output Enable Time		19.5 21		22 22	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ, C_L = 15 pF ('LS253); C_L = 50 pF ('S253)
t_{PHZ} t_{PLZ}	Output Disable Time		8.5 14		32 22	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ, ('LS253) C_L = 5 pF

54LS/74LS256

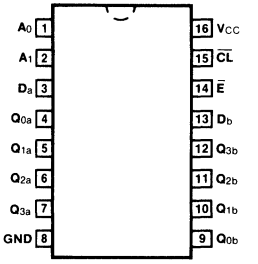
DUAL 4-BIT ADDRESSABLE LATCH

DESCRIPTION — The '256 is a dual 4-bit addressable latch with common control inputs; these include two Address inputs (A_0, A_1), an active LOW Enable input ($\overline{E}$) and an active LOW Clear input ($\overline{CL}$). Each latch has a Data input (D) and four outputs (Q_0 — Q_3).

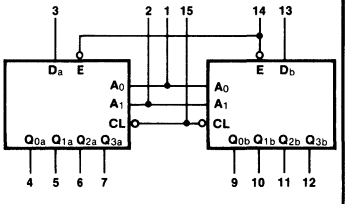
When the Enable ($\overline{E}$) is HIGH and the Clear input ($\overline{CL}$) is LOW, all outputs (Q_0 — Q_3) are LOW. Dual 4-channel demultiplexing occurs when the $\overline{CL}$ and $\overline{E}$ are both LOW. When $\overline{CL}$ is HIGH and $\overline{E}$ is LOW, the selected output (Q_0 — Q_3), determined by the Address inputs, follows D. When the $\overline{E}$ goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\overline{E}$ = LOW, $\overline{CL}$ = HIGH), changing more than one bit of the Address (A_0, A_1) could impose a transient wrong address. Therefore, this should be done only while in the memory mode ($\overline{E}$ = $\overline{CL}$ = HIGH).

- **SERIAL-TO-PARALLEL CAPABILITY**
- **OUTPUT FROM EACH STORAGE BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **EASILY EXPANDABLE**
- **ACTIVE LOW COMMON CLEAR**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0° C to +70° C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	74LS256PC		9B
Ceramic DIP (D)	A	74LS256DC	54LS256DM	6B
Flatpak (F)	A	74LS256FC	54LS256FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
A_0, A_1	Common Address Inputs	0.5/0.25
D_a, D_b	Data Inputs	0.5/0.25
$\overline{E}$	Common Enable Input (Active LOW)	1.0/0.5
$\overline{CL}$	Conditional Clear Input (Active LOW)	0.5/0.25
Q_{0a} — Q_{3a}	Side A Latch Outputs	10/5.0 (2.5)
Q_{0b} — Q_{3b}	Side B Latch Outputs	10/5.0 (2.5)

TRUTH TABLE

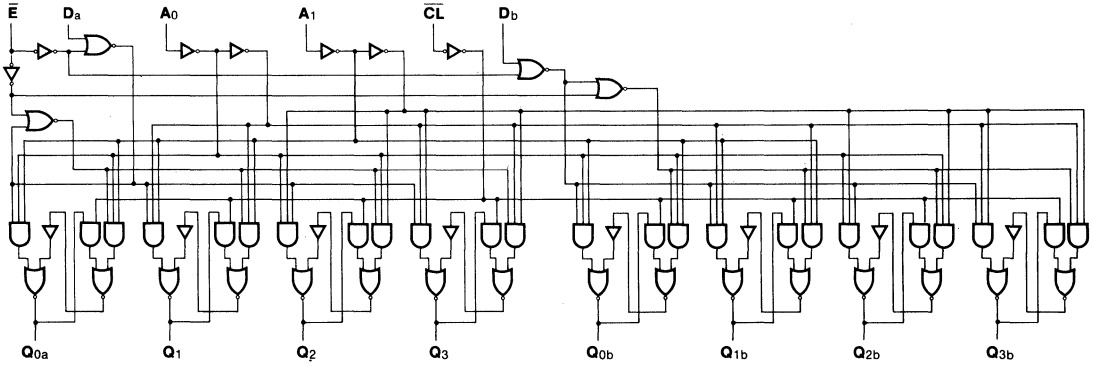
INPUTS				OUTPUTS				MODE
$\overline{CL}$	$\overline{E}$	A_0	A_1	Q_0	Q_1	Q_2	Q_3	
L	H	X	X	L	L	L	L	Clear
L	L	L	L	D	L	L	L	Demultiplex
L	L	H	L	L	D	L	L	
L	L	L	H	L	L	D	L	
L	L	H	H	L	L	L	D	
H	H	X	X	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Memory
H	L	L	L	D	Q_{t-1}	Q_{t-1}	Q_{t-1}	Addressable Latch
H	L	H	L	Q_{t-1}	D	Q_{t-1}	Q_{t-1}	
H	L	L	H	Q_{t-1}	Q_{t-1}	D	Q_{t-1}	
H	L	H	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	D	

t-1 = Bit time before address change or rising edge of E
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

MODE SELECTION

$\overline{E}$	$\overline{CL}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 4-Channel Demultiplexers
H	L	Clear

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		25	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n		27 24	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		30 20	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n		30 20	ns	Figs. 3-1, 3-20
t_{PHL}	Propagation Delay $\overline{CL}$ to Q_n		18	ns	Figs. 3-1, 3-16

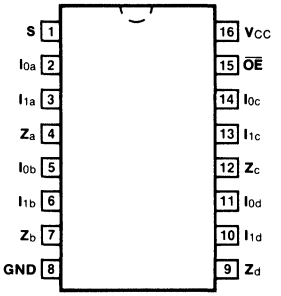
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H)	Setup Time HIGH D_n to $\overline{E}$	20		ns	Fig. 3-13
t_h (H)	Hold Time HIGH D_n to $\overline{E}$	0		ns	Fig. 3-13
t_s (L)	Setup Time LOW D_n to $\overline{E}$	15		ns	Fig. 3-13
t_h (L)	Hold Time LOW D_n to $\overline{E}$	0		ns	Fig. 3-13
t_s (H) t_s (L)	Setup Time HIGH or LOW, A_n to $\overline{E}$	0		ns	Fig. 3-21
t_w (L)	$\overline{E}$ Pulse Width LOW	17		ns	Fig. 3-21

54S/74S257
54LS/74LS257

QUAD 2-INPUT MULTIPLEXER
(With 3-State Outputs)

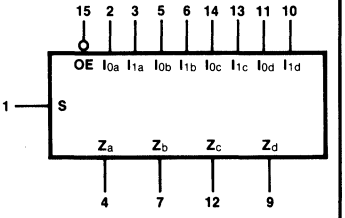
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '257 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER**
- **NON-INVERTING 3-STATE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

LOGIC SYMBOL



VCC = Pin 16
Gnd = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S257PC, 74LS257PC		9B
Ceramic DIP (D)	A	74S257DC, 74LS257DC	54S257DM, 54LS257DM	6B
Flatpak (F)	A	74S257FC, 74LS257FC	54S257FM, 54LS257FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{S}$	Common Data Select Input	2.5/2.5	1.0/0.5
$\overline{OE}$	3-State Output Enable Input (Active LOW)	1.25/1.25	0.5/0.25
$I_{0a} - I_{0d}$	Data Inputs from Source 0	1.25/1.25	0.5/0.25
$I_{1a} - I_{1d}$	Data Inputs from Source 1	1.25/1.25	0.5/0.25
$Z_a - Z_d$	Multiplexer Outputs	162/12.5 (50)	65/5.0 (25)/(2.5)

FUNCTIONAL DESCRIPTION — This device is a quad 2-input mulitplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S}) \qquad Z_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S}) \qquad Z_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

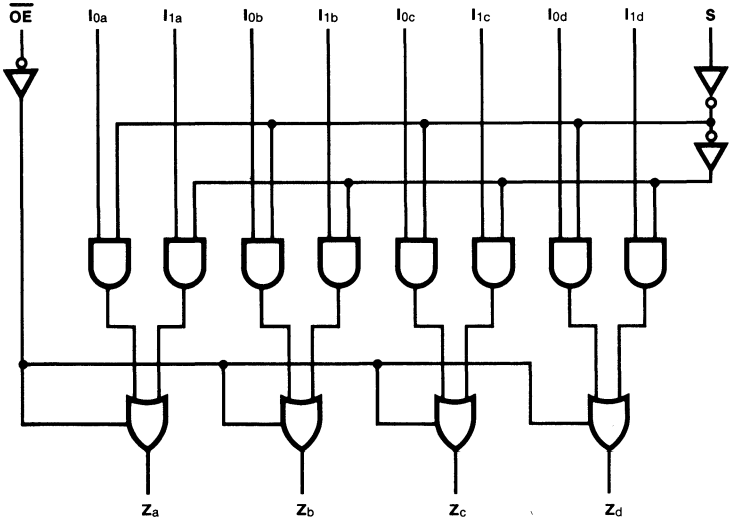
4

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	Z
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z)= High Impedance

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	Outputs HIGH		68		10	mA	V_{CC} = Max; S, I_{1x} = 4.5 V; $\overline{OE}$, I_{0x} = Gnd
		Outputs LOW		93		16		V_{CC} = Max; I_{1x} = 4.5 V; $\overline{OE}$, I_{0x}, S = Gnd
		Outputs OFF		99		19		V_{CC} = Max; S, I_{0x} = Gnd $\overline{OE}$, I_{1x} = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

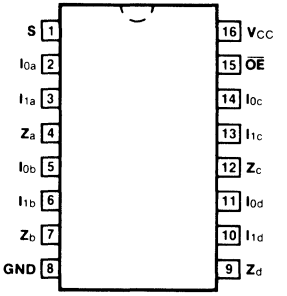
SYMBOL	PARAMETER	54/74S C_L = 15 pF, R_L = 280 Ω Min	54/74S Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n		7.5 6.5		18 18	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay S to Z_n		15 15		21 21	ns	Figs. 3-1, 3-20
t_{PZH} t_{PZL}	Output Enable Time		19.5 21		30 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS257)
t_{PHZ} t_{PLZ}	Output Disable Time		8.5 14		30 25	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ, C_L = 5 pF ('LS257)

54LS/74LS257A

QUAD 2-INPUT MULTIPLEXER

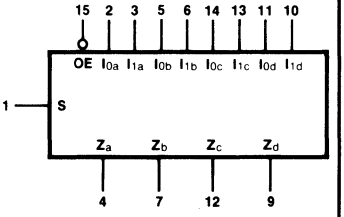
(With 3-State Outputs)

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '257A is the same as the '257, except that the output drive capability is increased as indicated in the tables below. The ac test limits are the same as the '257 but with the test load changed to 667 Ω and 45 pF, except for the Output Disable Time tests, whose load is 667 Ω and 5 pF. For all other information please refer to the '257 data sheet.

LOGIC SYMBOL



VCC = Pin 16
Gnd = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0° C to +70° C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	74LS257APC		9B
Ceramic DIP (D)	A	74LS257ADC	54LS257ADM	6B
Flatpak (F)	A	74LS257AFC	54LS257AFM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
Z_n	3-State Outputs	65/15 (25)/(7.5)

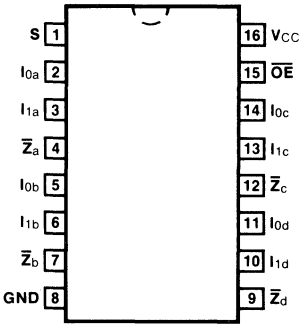
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage	XM, XC		0.4	V	I_{OL} = 12 mA	VCC = Min
		XC		0.5		I_{OL} = 24 mA	
I_{OS}	Output Short Circuit Current		-30	-130	mA	VCC = Max	

54S/74S258
54LS/74LS258

QUAD 2-INPUT MULTIPLEXER
(With 3-State Outputs)

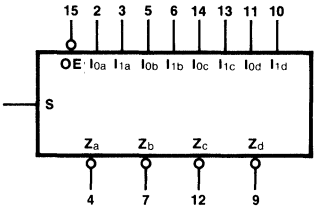
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '258 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER**
- **INVERTING 3-STATE OUTPUTS**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S258PC, 74LS258PC		9B
Ceramic DIP (D)	A	74S258DC, 74LS258DC	54S258DM, 54LS258DM	6B
Flatpak (F)	A	74S258FC, 74LS258FC	54S258FM, 54LS258FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. defintions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{S}$	Common Data Select Input	2.5/2.5	1.0/0.5
$\overline{OE}$	3-State Output Enable Input (Active LOW)	1.25/1.25	0.5/0.25
$I_{0a} - I_{0d}$	Data Inputs from Source 0	1.25/1.25	0.5/0.25
$I_{1a} - I_{1d}$	Data Inputs from Source 1	1.25/1.25	0.5/0.25
$\overline{Z}_a - \overline{Z}_d$	Inverting Data Outputs	162/12.5 (50)	65/15 (25)/(7.5)

FUNCTIONAL DESCRIPTION — This device is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The '258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{\overline{OE}} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S}) \qquad \overline{Z}_b = \overline{\overline{OE}} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$\overline{Z}_c = \overline{\overline{OE}} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S}) \qquad \overline{Z}_d = \overline{\overline{OE}} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

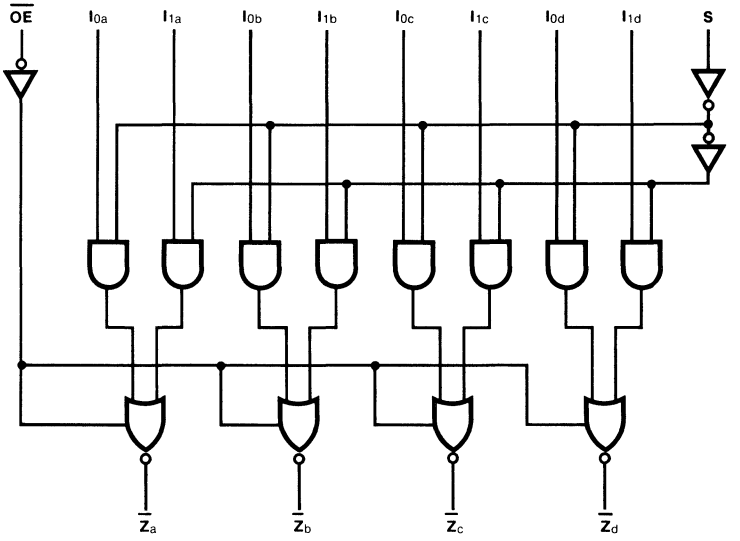
4

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current		-40	-100	-20	-100	mA	V_{CC} = Max
I_{CC}	Power Supply Current	Outputs HIGH		56		7.0	mA	V_{CC} = Max; S, I_{1x} = 4.5 V $\overline{OE}$, I_{0x} = Gnd
		Outputs LOW		81		14		V_{CC} = Max; I_{1x} = 4.5 V $\overline{OE}$, I_{0x}, S = Gnd
		Outputs OFF		87		19		V_{CC} = Max; S, I_{0x} = Gnd $\overline{OE}$ = I_{1x} = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

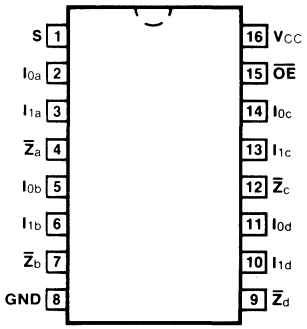
SYMBOL	PARAMETER	54/74S C_L = 15 pF, R_L = 280 Ω Min	54/74S Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$		6.0 6.0		18 18	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay S to $\overline{Z}_n$		12 12		21 21	ns	Figs. 3-1, 3-4
t_{PZH} t_{PZL}	Output Enable Time		19.5 21		30 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS258)
t_{PHZ} t_{PLZ}	Output Disable Time		8.5 14		30 25	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ, C_L = 5 pF ('LS258)

54LS/74LS258A

QUAD 2-INPUT MULTIPLEXER

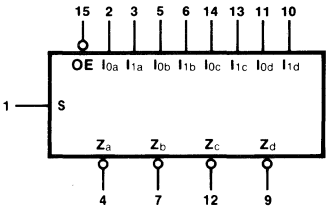
(With 3-State Outputs)

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '258A is the same as the '258, except that the output drive capability is increased as indicated in the tables below. The ac test limits are the same as the '258 but with the test load changed to 667 Ω and 45 pF, except for the Output Disable Time tests, whose load is 667 Ω and 5 pF. For all other information please refer to the '258 data sheet.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0° C to +70° C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	74LS258APC		9B
Ceramic DIP (D)	A	74LS258ADC	54LS258ADM	6B
Flatpak (F)	A	74LS258AFC	54LS258AFM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$\overline{Z}_n$	Inverting 3-State Outputs	65/15 (25)/(7.5)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
VOL	Output LOW Voltage	XM, XC		0.4	V	IOL = 12 mA	VCC = Min
		XC		0.5		IOL = 24 mA	
IOS	Output Short Circuit Current		-30	-130	mA	VCC = Max	

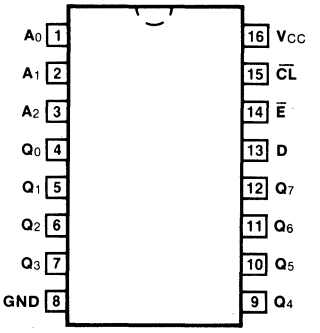
54LS/74LS259

8-BIT ADDRESSABLE LATCH

DESCRIPTION — The '259 is a high speed 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multi-functional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW common Clear for resetting all latches, as well as, an active LOW Enable. It is functionally identical to the 9334 and 93L34 8-bit addressable latch.

- **SERIAL-TO-PARALLEL CONVERSION**
- **EIGHT BITS OF STORAGE WITH OUTPUT OF EACH BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY**
- **EASILY EXPANDABLE**
- **COMMON CLEAR**
- **FULLY TTL AND CMOS COMPATIBLE**

CONNECTION DIAGRAM
PINOUT A



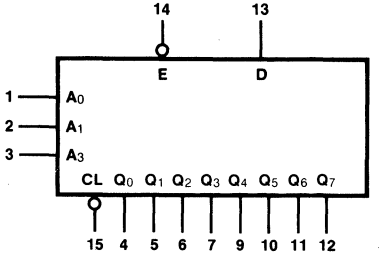
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS259PC		9B
Ceramic DIP (D)	A	74LS259DC	54LS259DM	6B
Flatpak (F)	A	74LS259FC	54LS259FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$A_0 - A_2$	Address Inputs	0.5/0.25
D	Data Input	0.5/0.25
$\overline{E}$	Enable Input (Active LOW)	1.0/0.5
$\overline{CL}$	Conditional Clear Input (Active LOW)	0.5/0.25
$Q_0 - Q_7$	Latch Outputs	10/5.0 (2.5)

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '259 has four modes of operation as shown in the Mode Selection Table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. in the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the '259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode. The Truth Table below summarizes the operations of the '259.

MODE SELECT TABLE

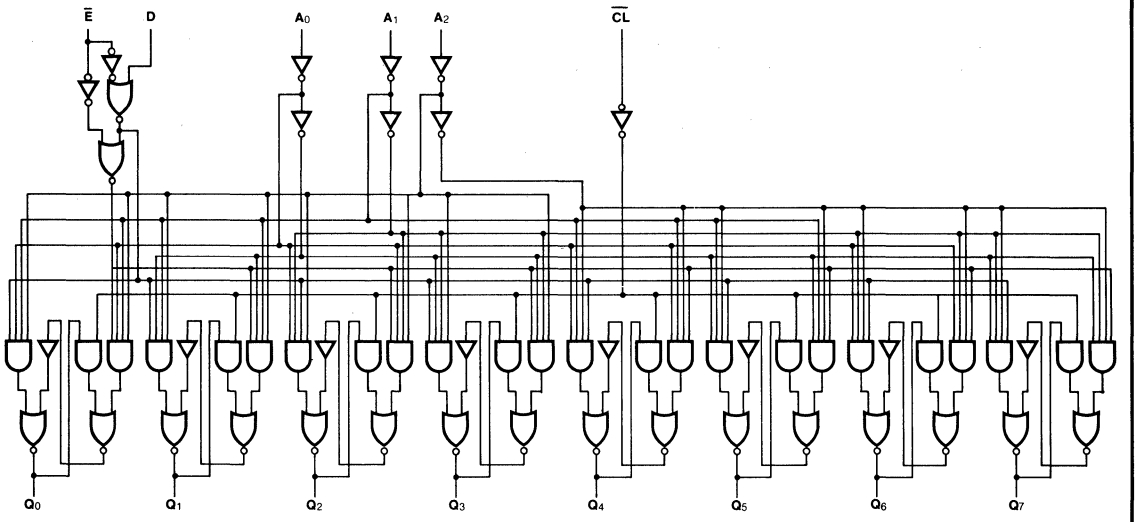
$\overline{E}$	$\overline{CL}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 8-Channel Demultiplexer
H	L	Clear

TRUTH TABLE

INPUTS						OUTPUTS								
$\overline{CL}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Memory
H	I	I	L	L	L	L	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Addressable
H	L	H	L	L	L	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Latch
H	L	L	H	L	L	Q_{t-1}	L	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	
H	L	H	H	L	L	Q_{t-1}	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
H	L	L	H	H	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	L	
H	L	H	H	H	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	H	

Q_{t-1} = Previous Output State
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		36	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

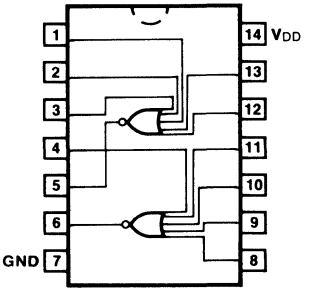
SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}$ to Q_n		27 24	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay, D to Q_n		30 20	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay, A_n to Q_n		30 20	ns	Figs. 3-1, 3-20
t_{PHL}	Propagation Delay, $\overline{CL}$ to Q_n		18	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H)	Setup Time HIGH, D to $\overline{E}$	20		ns	Fig. 3-13
t_h (H)	Hold Time HIGH, D to $\overline{E}$	0		ns	
t_s (L)	Setup Time LOW, D to $\overline{E}$	15		ns	
t_h (L)	Hold Time LOW, D to $\overline{E}$	0		ns	
t_s	Setup Time HIGH or LOW, A_n to $\overline{E}$	0		ns	Fig. 3-21
t_w (L)	$\overline{E}$ Pulse Width LOW	17			

54S/74S260
54LS/74LS260
DUAL 5-INPUT NOR GATE

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S260PC, 74LS260PC		9A
Ceramic DIP (D)	A	74S260DC, 74LS260DC	54S260DM, 54LS260DM	6A
Flatpak (F)	A	74S260FC, 74LS260FC	54S260FM, 54LS260FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.25/1.25	0.5/0.25
Outputs	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply Current		29		4.0	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			45		5.5		V_{IN} = Open	
t_{PLH}	Propagation Delay		5.5		10	ns	Figs. 3-1, 3-4	
t_{PHL}			6.0		12			

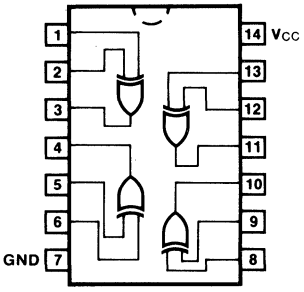
*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54LS/74LS266

QUAD 2-INPUT EXCLUSIVE-NOR GATE

(With Open-Collector Outputs)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS266PC		9A
Ceramic DIP (D)	A	74LS266DC	54LS266DM	6A
Flatpak (F)	A	74LS266FC	54LS266FM	3I

TRUTH TABLE

INPUTS		OUTPUT
A	B	Z
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/0.375
Outputs	OC**/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current		13	mA	V_{CC} = Max
t_{PLH} t_{PHL}	Propagation Delay		23 23	ns	Other Input LOW Figs. 3-2, 3-5
t_{PLH} t_{PHL}	Propagation Delay		23 23	ns	Other Input HIGH Figs. 3-2, 3-5

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
**OC — Open Collector

54LS/74LS273

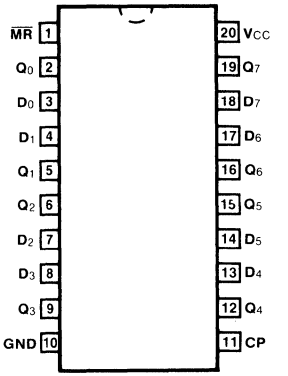
8-BIT REGISTER

(With Clear)

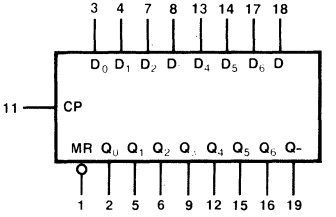
DESCRIPTION — The '273 is a high speed 8-bit register, consisting of eight D-type flip-flops with a common Clock and an asynchronous active LOW Master Reset. This device is supplied in a 20-pin package featuring 0.3 inch row spacing.

- **EDGE-TRIGGERED**
- **8-BIT HIGH SPEED REGISTER**
- **PARALLEL IN AND OUT**
- **COMMON CLOCK AND MASTER RESET**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

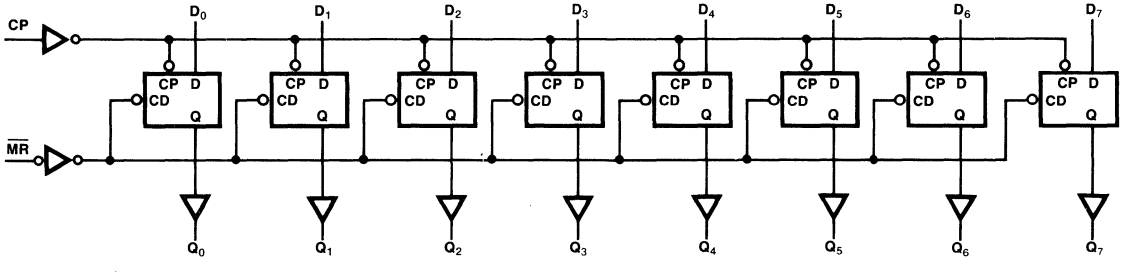
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS273PC		9Z
Ceramic DIP (D)	A	74LS273DC	54LS273DM	4E
Flatpak (F)	A	74LS273FC	54LS273FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$D_0 - D_7$	Data Inputs	0.5/0.25
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	0.5/0.25
$Q_0 - Q_7$	Flip-flop Outputs	10/5.0 (2.5)

LOGIC DIAGRAM



273

FUNCTIONAL DESCRIPTION — The '273 is an 8-bit parallel register with a common Clock and common Master Reset. When the $\overline{MR}$ input is LOW, the Q outputs are LOW, independent of the other inputs. Information meeting the setup and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

TRUTH TABLE

INPUTS			OUTPUTS
MR	CP	D_n	Q_n
L	X	X	L
H	↑	H	H
H	↑	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specifed)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		27	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

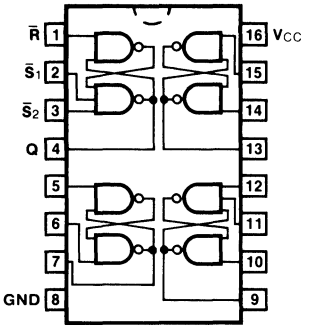
SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		24 24	ns	Figs. 3-1, 3-8
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		27	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to CP	15 15		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to CP	5.0 5.0		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	20 20		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	15		ns	Fig. 3-16

54/74279
54LS/74LS279
QUAD SET-RESET LATCH

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74279PC, 74LS279PC		9B
Ceramic DIP (D)	A	74279DC, 74LS279DC	54279DM, 54LS279DM	6B
Flatpak (F)	A	74279FC, 74LS279FC	54279FM, 54LS279FM	4L

TRUTH TABLE

INPUTS $\bar{S}_1$	INPUTS $\bar{S}_2$	INPUTS $\bar{R}$	OUTPUT Q
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
h = The output is HIGH as long as S_1 or S_2 is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the Truth Table.

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	20/10	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

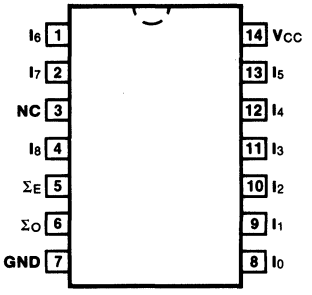
SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current		30		7.0	mA	V_{CC} = Max, $\bar{R}$ = Gnd
t_{PLH} t_{PHL}	Propagation Delay $\bar{S}$ to Q		22 15		22 15	ns	Figs. 3-1, 3-10
t_{PHL}	Propagation Delay $\bar{R}$ to Q		27		27	ns	Figs. 3-1, 3-10

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54S/74S280

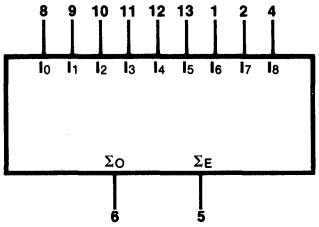
9-BIT PARITY GENERATOR/CHECKER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '280 is a high speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number or these inputs are HIGH. If an even number of inputs are HIGH, the Sum Even output is HIGH. If an odd number are HIGH, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output.

LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +70°C	PKG TYPE
Plastic DIP (P)	A	74S280PC		9A
Ceramic DIP (D)	A	74S280DC	54S280DM	6A
Flatpak (F)	A	74S280FC	54S280FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

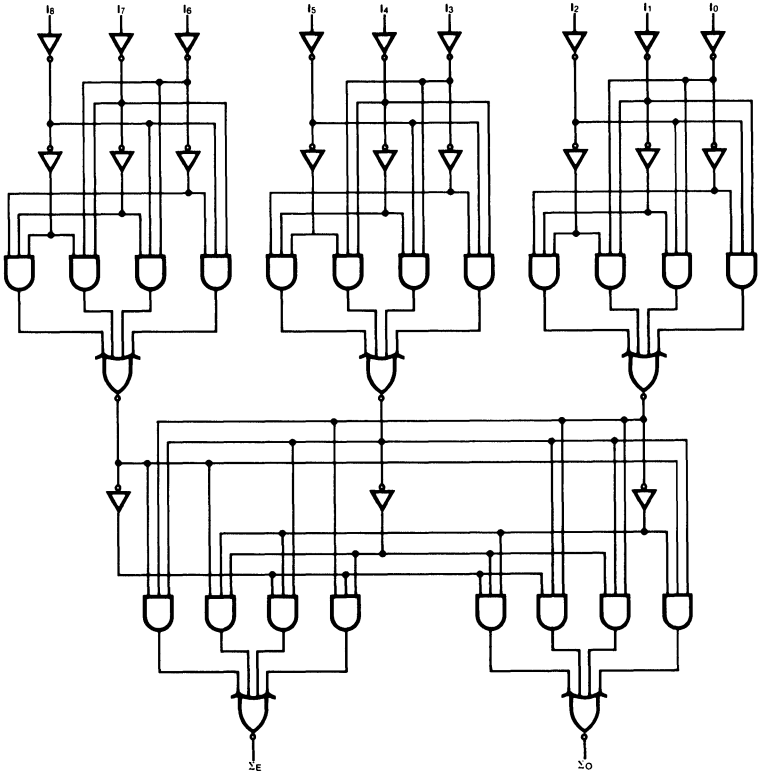
PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW
$I_0 - I_8$	Data Inputs	1.25.1.25
Σ_O	Odd Parity Output	25/12.5
Σ_E	Even Parity Output	25/12.5

TRUTH TABLE

NUMBER OF INPUTS $I_0 - I_8$ THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8,	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S Min	54/74S Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		99	mA	V_{CC} = Max, T_A = 25°C All Inputs = Gnd
		XC		105		
		XM		94	mA	V_{CC} = Max, T_A = 125°C All Inputs = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

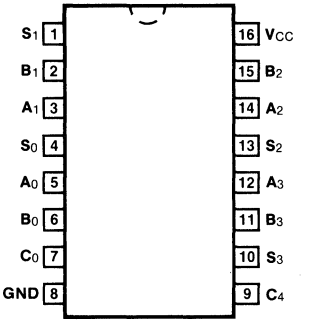
SYMBOL	PARAMETER	54/47S C_L = 15 pF R_L = 280 Ω Min	54/47S Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_E		21 18	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_O		21 18	ns	Figs. 3-1, 3-20

54/74283
54LS/74LS283

4-BIT BINARY FULL ADDER
(With Fast Carry)

DESCRIPTION — The '283 high speed 4-bit binary full adders with internal carry lookahead accept two 4-bit binary words (A_0 — A_3, B_0 — B_3) and a Carry input (C_0). They generate the binary Sum outputs (S_0 — S_3) and the Carry output (C_4) from the most significant bit. They operate with either active HIGH or active LOW operands (positive or negative logic).

CONNECTION DIAGRAM
PINOUT A



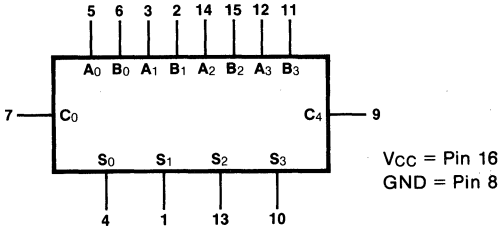
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74283PC, 74LS283PC		9B
Ceramic DIP (D)	A	74283DC, 74LS283DC	54283DM, 54LS283DM	6B
Flatpak (F)	A	74283FC, 74LS283FC	54283FM, 54LS283FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
A_0 — A_3	A Operand Inputs	1.0/1.0	1.0/0.5
B_0 — B_3	B Operand Inputs	1.0/1.0	1.0/0.5
C_0	Carry Input	1.0/1.0	0.5/0.25
S_0 — S_3	Sum Outputs	20/10	10/5.0 (2.5)
C_4	Carry Output	10/5.0	10/5.0 (2.5)

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '283 adds two 4-bit binary words (A plus B) plus the incoming carry C_0. The binary sum appears on the Sum (S_0 — S_3) and outgoing carry (C_4) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus C_0, A_0, B_0 can be arbitrarily assigned to pins 5, 6 and 7. Due to the symmetry of the binary add function, the '283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that if C_0 is not used it must be tied LOW for active HIGH logic or tied HIGH for active LOW logic.

Example:

	C_0	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	S_0	S_1	S_2	S_3	C_4
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH: 0 + 10 + 9 = 3 + 16 Active LOW: 1 + 5 + 6 = 12 + 0

Due to pin limitations, the intermediate carries of the '283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. *Figure a* shows a way of making a 3-bit adder. Tying the operand inputs of the fourth adder (A_3, B_3) LOW makes S_3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, *Figure b* shows a way of dividing the '283 into a 2-bit and a 1-bit adder. The third stage adder (A_2, B_2, S_2) is used merely as a means of getting a carry (C_{10}) signal into the fourth stage (via A_2 and B_2) and bringing out the carry from the second stage on S_2. Note that as long as A_2 and B_2 are the same, whether HIGH or LOW, they do not influence S_2. Similarly, when A_2 and B_2 are the same the carry into the third stage does not influence the carry out of the third stage. *Figure c* shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S_0, S_1 and S_2 present a binary number equal to the number of inputs I_1 — I_5 that are true. *Figure d* shows one method of implementing a 5-input majority gate. When three or more of the inputs I_1 — I_5 are true, the output M_5 is true.

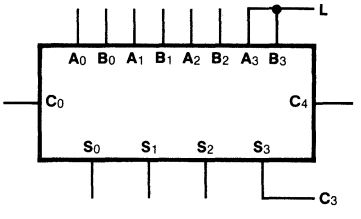


Fig. a 3-Bit Adder

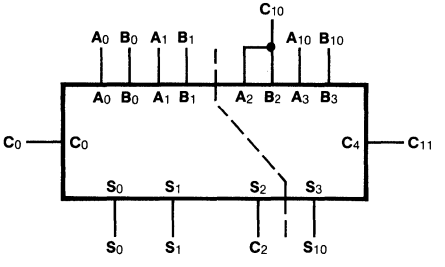


Fig. b 2-Bit and 1-Bit Adders

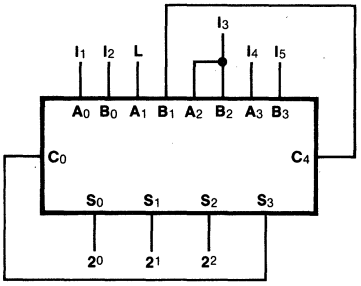


Fig. c 5-Input Encoder

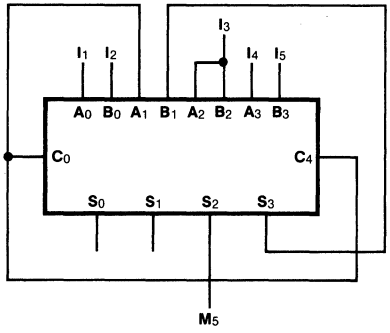
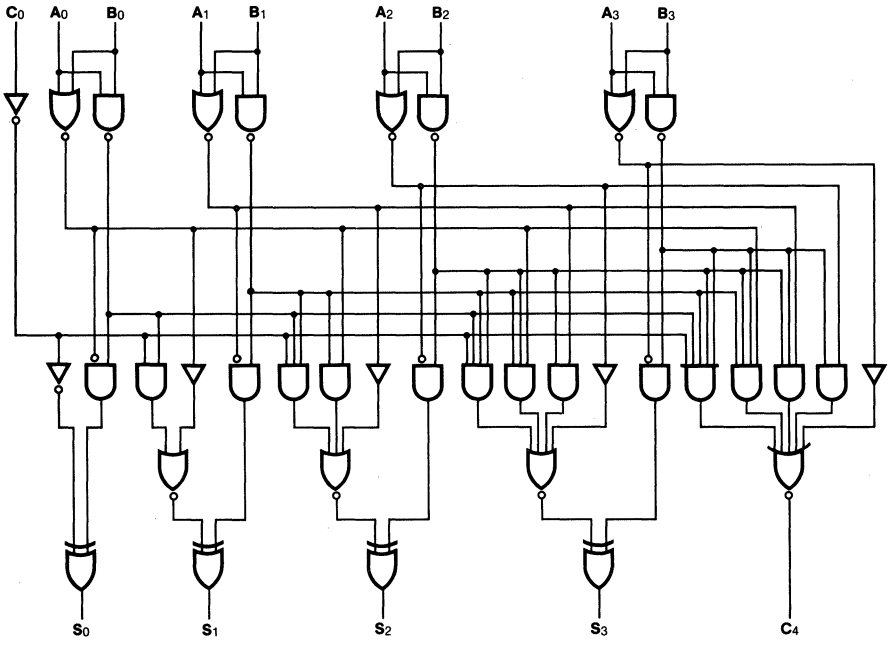


Fig. d 5-Input Majority Gate

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current at S_n	XM	-20	-55	-20	-100	mA	V_{CC} = Max
		XC	-18	-55	-20	-100		
I_{OS}	Output Short Circuit Current at C_4	XM	-20	-70	-20	-100	mA	V_{CC} = Max
		XC	-18	-70	-20	-100		
I_{CC}	Power Supply Current	XM		99		39	mA	V_{CC} = Max, Inputs = Gnd ('LS283) Inputs = 4.5 V ('283)
		XC		110		39		
		XM, XC				34	mA	V_{CC} = Max Inputs = 4.5 V ('LS283)

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH}	Propagation Delay C_0 to S_n		21		24	ns	Figs. 3-1, 3-20
t_{PHL}			21		24		
t_{PLH}	Propagation Delay A_n or B_n to S_n		24		24	ns	Figs. 3-1, 3-20
t_{PHL}			24		24		
t_{PLH}	Propagation Delay C_0 to C_4		14		17	ns	Figs. 3-1, 3-5 R_L = 780 Ω ('283)
t_{PHL}			16		17		
t_{PLH}	Propagation Delay A_n or B_n to C_4		14		17	ns	Figs. 3-1, 3-5 R_L = 780Ω ('283)
t_{PHL}			16		17		

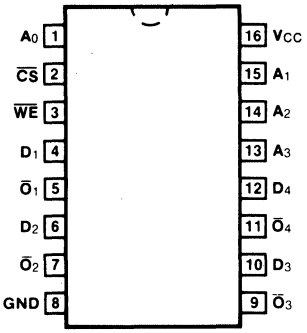
4

54S/74S289
54LS/74LS289

64-BIT RANDOM ACCESS MEMORY

(With Open-Collector Outputs)

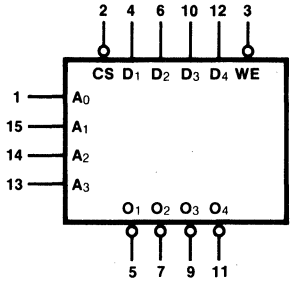
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '289 is a high speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading, and addresses are fully decoded on-chip. Outputs are open-collector type and are in the off (HIGH) state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode; output data is the complement of the stored data.

- **OPEN-COLLECTOR OUTPUTS FOR WIRED-AND APPLICATIONS**
- **BUFFERED INPUTS MINIMIZE LOADING**
- **ADDRESS DECODING ON-CHIP**
- **DIODE CLAMPED INPUTS MINIMIZE RINGING**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S289PC, 74LS289PC		9B
Ceramic DIP (D)	A	74S289DC, 74LS289DC	54S289DM, 54LS289DM	6B
Flatpak (F)	A	74S289FC, 74LS289FC	54S289FM, 54LS289FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	0.63/0.16	0.5/0.013
$\overline{CS}$	Chip Select Input (Active LOW)	0.63/0.16	0.5/0.013
$\overline{WE}$	Write Enable Input (Active LOW)	0.63/0.16	0.5/0.013
$D_1 - D_4$	Data Inputs	0.63/0.16	0.5/0.013
$\overline{O}_1 - \overline{O}_4$	Inverted Data Outputs	OC*/10	OC*/10 (5.0)

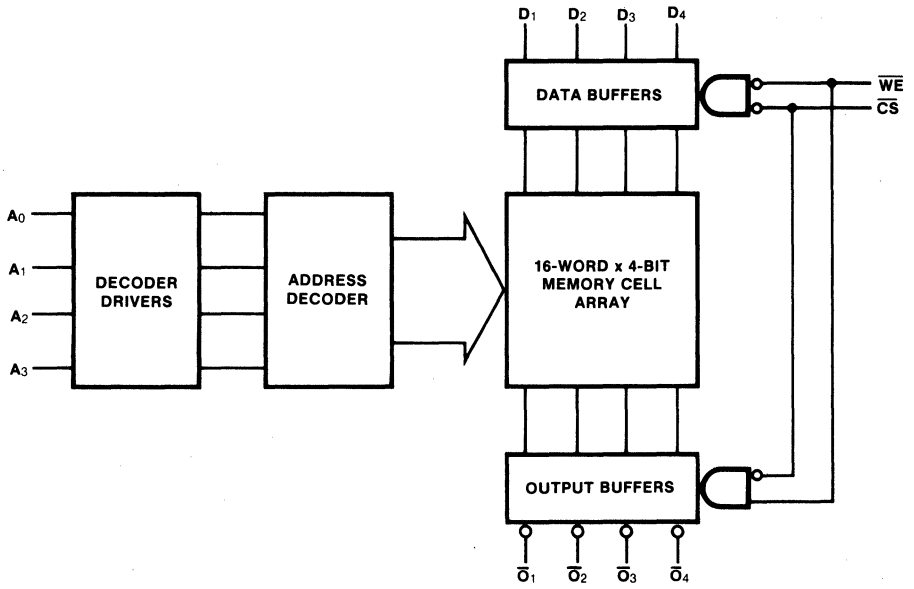
*OC — Open Collector

FUNCTION TABLE

INPUTS		OPERATION	CONDITION OF OUTPUTS
$\overline{CS}$	$\overline{WE}$		
L	L	Write	Off (HIGH)
L	H	Read	Complement of Stored Data
H	X	Inhibit	Off (HIGH)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage	XM		0.5		0.4	V	V_{CC} = Min I_{OL} = 16 mA ('S289) I_{OL} = 8.0 mA (54LS289) I_{OL} = 16 mA (74LS289)	
		XC		0.45		0.5			
I_{OH}	Output HIGH Current			40		20	μA	V_{OH} = 2.4 V	V_{CC} = Min
				100		100		V_{OH} = 5.5 V	
I_{CC}	Power Supply Current			105		40	mA	V_{CC} = Max	

AC CHARACTERISTICS OVER RECOMMENDED V_{CC} AND T_A RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S C_L = 30 pF, R_L = * Min	54/74S Max	54/74LS C_L = 15 pF, R_L = 2 kΩ Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Access Time, HIGH or LOW, A_n to $\overline{O}_n$	XM		50		37**	ns	Figs. 3-2, 3-20
		XC		35		37**		
t_{PHL}	Access Time $\overline{CS}$ to $\overline{O}_n$	XM		25		10**	ns	Figs. 3-2, 3-5
		XC		17		10**		
t_{PLH}	Disable Time $\overline{CS}$ to $\overline{O}_n$	XM		20			ns	
		XC		17				
t_{PHL}	Recovery Time $\overline{WE}$ to $\overline{O}_n$	XM		40		30**	ns	Figs. 3-2, 3-4
		XC		35		30**		
t_{PLH}	Disable Time $\overline{WE}$ to $\overline{O}_n$	XM		30			ns	
		XC		25				

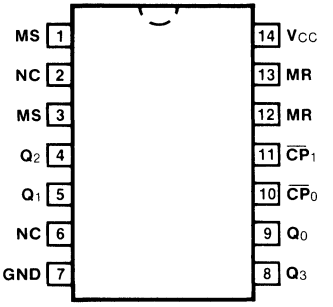
AC OPERATING REQUIREMENTS OVER RECOMMENDED V_{CC} AND T_A RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time, HIGH or LOW A_n to $\overline{WE}$	0 0		10** 10**		ns	Fig. 3-21
t_h (H) t_h (L)	Hold Time, HIGH or LOW A_n to $\overline{WE}$	0 0		0** 0**		ns	
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to $\overline{WE}$	20 20		25** 25**		ns	Fig. 3-13
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to WE	0 0		0* 0*		ns	
t_s (L)	Setup Time LOW $\overline{CS}$ to $\overline{WE}$	0				ns	Fig. 3-14
t_h (L)	Hold Time LOW $\overline{CS}$ to $\overline{WE}$	0				ns	Fig. 3-13
t_w (L)	$\overline{WE}$ Pulse Width LOW	20		25**		ns	Fig. 3-14

*R_L = 300 Ω to V_{CC} and 600 Ω to Gnd.
**Typical Value

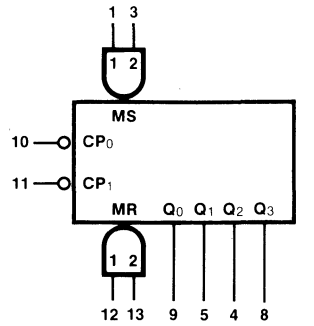
54/74290
54LS/74LS290
BCD DECADE COUNTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '290 is a 4-stage ripple counter containing a high speed flip-flop acting as a divide-by-two and three flip-flops connected as a divide-by-five. HIGH signals on the Master Reset (MR) inputs override the clocks and force all outputs to the LOW state. HIGH signals on the Master Set (MS) inputs override the clocks and MR and force the outputs to the BCD nine state. The '290 is the same circuit as the '90 except that it has corner power pins and is therefore recommended for new designs. For detail specifications, truth tables and functional description, please refer to the '90 data sheet.

LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7
NC = Pin 2,6

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	A	74290PC, 74LS290PC		9A
Ceramic DIP (D)	A	74290DC, 74LS290DC	54290DM, 54LS290DM	6A
Flatpak (F)	A	74290FC, 74LS290FC	54290FM, 54LS290FM	3I

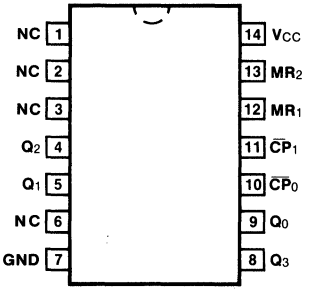
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CP_0}$	÷2 Section Clock Input (Active Falling Edge)	2.0/2.0	1.0/1.5
$\overline{CP_1}$	÷5 Section Clock Input (Active Falling Edge)	3.0/3.0	2.0/2.0
MR_1, MR_2	Asynchronous Master Reset Inputs (Active HIGH)	1.0/1.0	0.5/0.25
MS_1, MS_2	Asynchronous Master Set (Set to 9) Inputs (Active HIGH)	1.0/1.0	0.5/0.25
Q_0	÷2 Flip-flop Output*	20/10	10/5.0 (2.5)
Q_1 — Q_3	÷5 Flip-flop Outputs	20/10	10/5.0 (2.5)

*The Q_0 output is guaranteed to drive the full rated fan-out plus the $\overline{CP_1}$ input.

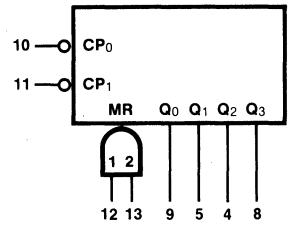
54/74293
54LS/74LS293
MODULO-16 BINARY COUNTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '293 is a 4-stage ripple counter containing a high speed flip-flop acting as a divide-by-two and three flip-flops acting as a divide-by-eight. HIGH signals on the Master Reset (MR) inputs override the clocks and force all outputs to the LOW state. The '293 is the same circuit as the '93 except that it has corner power pins and is therefore recommended for new designs. For detail specifications, truth tables and functional description, please refer to the '93 data sheet.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 1, 2, 3, 6

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74293PC, 74LS293PC		9A
Ceramic DIP (D)	A	74293DC, 74LS293DC	54293DM, 54LS293DM	6A
Flatpak (F)	A	74293FC, 74LS293FC	54293FM, 54LS293FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CP}_0$	÷2 Section Clock Input (Active Falling Edge)	2.0/2.0	1.0/1.5
$\overline{CP}_1$	÷8 Section Clock Input (Active Falling Edge)	2.0/2.0	1.0/1.0
MR_1, MR_2	Asynchronous Master Reset Inputs (Active HIGH)	1.0/1.0	0.5/0.25
Q_0	÷2 Flip-flop Output*	20/10	10/5.0 (2.5)
Q_1 — Q_3	÷8 Flip-flop Outputs	20/10	10/5.0 (2.5)

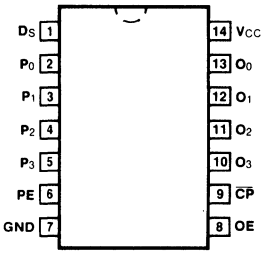
*The Q_0 output is guaranteed to drive the full rated fan-out plus the $\overline{CP}_1$ input.

54LS/74LS295A

4-BIT SHIFT REGISTER

(With 3-State Outputs)

CONNECTION DIAGRAM
PINOUT A

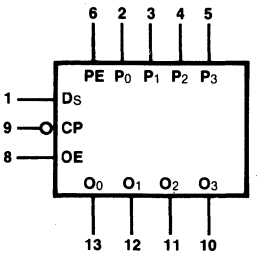


DESCRIPTION — The '295A is a 4-bit shift register with serial and parallel synchronous operating modes, and independent 3-state output buffers. The Parallel Enable input (PE) controls the shift-right or parallel load operation. All data transfers and shifting occur synchronous with the HIGH-to-LOW clock transition.

The 3-state output buffers are controlled by an active HIGH Output Enable input (OE). Disabling the output buffers does not affect the shifting or loading of input data, but it does inhibit serial expansion. The device is fabricated with the Schottky barrier diode process for high speed.

- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**
- **NEGATIVE EDGE-TRIGGERED CLOCK INPUT**
- **PARALLEL ENABLE MODE CONTROL INPUT**
- **3-STATE BUSSABLE OUTPUT BUFFERS**

LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0° C to +70° C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	74LS295APC		9A
Ceramic DIP (D)	A	74LS295ADC	54LS295ADM	6A
Flatpak (F)	A	74LS295AFC	54LS295AFM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
PE	Parallel Enable Input (Active HIGH)	0.5/0.25
DS	Serial Data Input	0.5/0.25
P0 — P3	Parallel Data Inputs	0.5/0.25
OE	3-State Output Enable Input (Active HIGH)	0.5/0.25
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	0.5/0.25
O0 — O3	3-State Outputs	65/5.0 (25)/(2.5)

FUNCTIONAL DESCRIPTION — This device is a 4-bit shift register with serial and parallel synchronous operating modes. It has a Serial Data (D_S) and four Parallel Data (P_0 — P_3) inputs and four parallel 3-State output buffers (O_0 — O_3). When the Parallel Enable (PE) input is HIGH, data is transferred from the Parallel Data inputs (P_0 — P_3) into the register synchronous with the HIGH-to-LOW transition of the Clock ($\overline{CP}$). When the PE is LOW, a HIGH-to-LOW transition on the clock transfers the serial data on the D_S input to register Q_0, and shifts data from Q_0 to Q_1, Q_1 to Q_2 and Q_2 to Q_3. The input data and parallel enable are fully edged-triggered and must be stable only one setup time before the HIGH-to-LOW clock transition.

The 3-state output buffers are controlled by an active HIGH Output Enable input (OE). When the OE is HIGH, the four register outputs appear at the O_0 — O_3 outputs. When OE is LOW, the outputs are forced to a high impedance OFF state. The 3-state output buffers are completely independent of the register operation, i.e., the input transitions on the OE input do not affect the serial or parallel data transfers of the register. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

MODE SELECT TABLE

OPERATING MODE	INPUTS				OUTPUTS			
	PE	$\overline{CP}$	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift Right	l	⌐	l	X	L	q_0	q_1	q_2
	l	⌐	h	X	H	q_0	q_1	q_2
Parallel Load	h	⌐	X	p_n	p_0	p_1	p_2	p_3

*The indicated data appears at the Q outputs when OE is HIGH. When OE is LOW, the indicated data is loaded into the register, but the outputs are all forced to the high impedance OFF state.

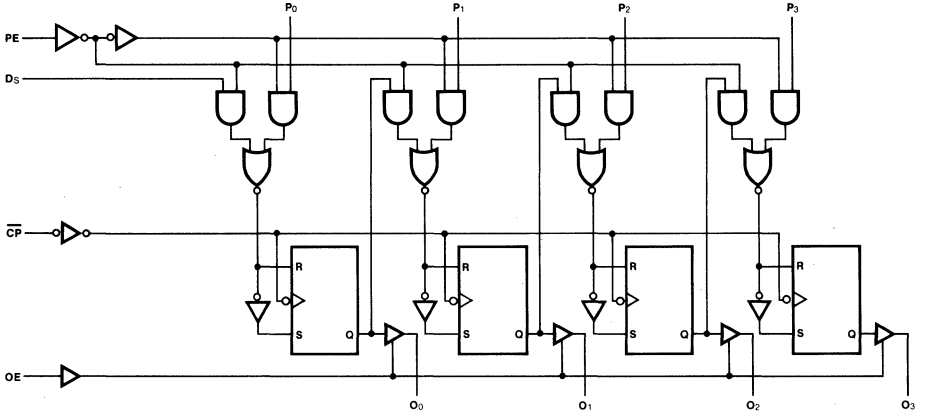
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.

l = LOW Voltage Level one set-up time prior to the HIGH-to-LOW clock transition

h = HIGH Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Curent		-20	-100	mA	V_{CC} = Max
I_{CC}	Power Supply Current	Outputs ON		23	mA	V_{CC} = Max, P_n = Gnd PE, D_S, OE = 4.5 V $\overline{CP}$ = ⊓_
		Outputs OFF		25		V_{CC} = Max, PE, D_S = 4.5 V P_n, OE, $\overline{CP}$ = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

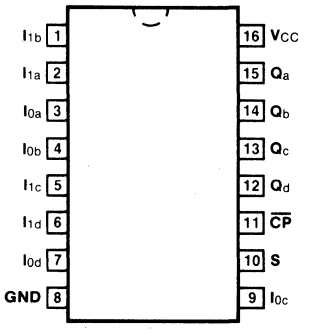
SYMBOL	PARAMETER	54/74LS C_L = 15 pF Min	54/74LS C_L = 15 pF Max	UNITS	CONDITIONS
f_{max}	Maximum Shift Frequency	30		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_n		30 26	ns	Figs. 3-1, 3-9
t_{PZH} t_{PZL}	Output Enable Time		18 20	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ,
t_{PHZ} t_{PLZ}	Output Disable Time		24 20	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ, C_L = 5 pF

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW D_S , P_n to $\overline{CP}$	20 20		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time HIGH or LOW D_S, P_n to $\overline{CP}$	10 10		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW PE to $\overline{CP}$	20 20		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time HIGH or LOW PE to $\overline{CP}$	0 0		ns	
t_w (L)	$\overline{CP}$ Pulse Width LOW	20		ns	Fig. 3-9

54/74298
54LS/74LS298
QUAD 2-PORT REGISTER
(Multiplexer with Storage)

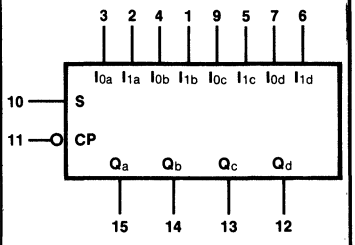
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '298 is a quad 2-port register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register synchronous with the HIGH-to-LOW transition of the Clock input.

- **SELECT FROM TWO DATA SOURCES**
- **FULLY EDGE-TRIGGERED OPERATION**
- **TYPICAL POWER DISSIPATION OF 65 mW ('LS298)**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74298PC, 74LS298PC		9B
Ceramic DIP (D)	A	74298DC, 74LS298DC	54298DM, 54LS298DM	6B
Flatpak (F)	A	74298FC, 74LS298FC	54298FM, 54LS298FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{S}$	Common Select Input	1.0/1.0	0.5/0.25
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	1.0/1.0	0.5/0.25
I_{0a} — I_{0d}	Source 0 Data Inputs	1.0/1.0	0.5/0.25
I_{1a} — I_{1d}	Source 1 Data Inputs	1.01/.0	0.5/0.25
Q_a — Q_d	Flip-flop Outputs	20/10	10/5.0 (2.5)

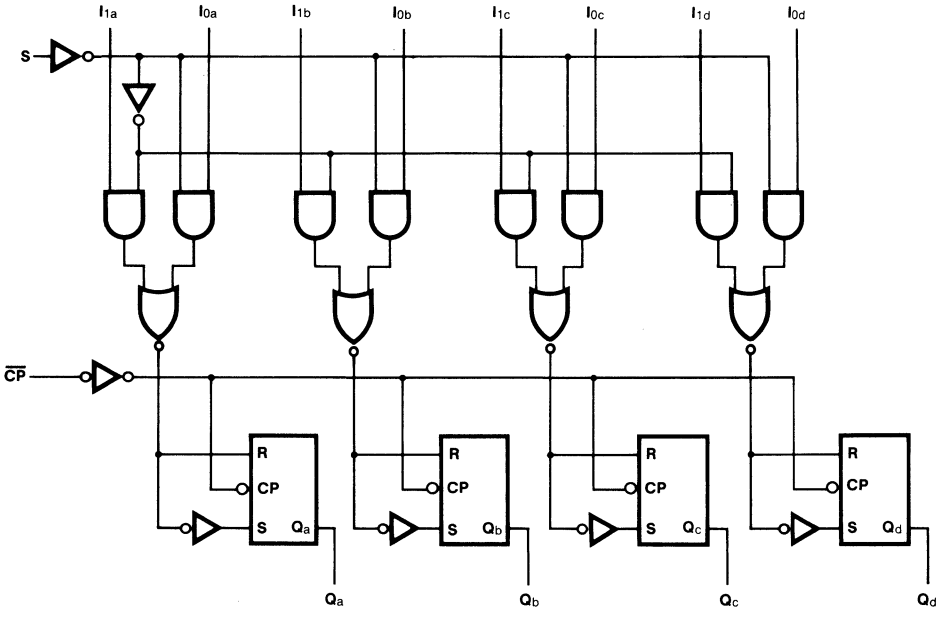
FUNCTIONAL DESCRIPTION — This device is a high speed quad 2-port register. It selects four bits of data from two sources (ports) under the control of a Common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). The 4-bit output register is fully edge-triggered. The Data inputs (I_{nx}) and Select input (S) need be stable only one setup time prior to the HIGH-to-LOW transition of the clock for predicatable operation.

TRUTH TABLE

INPUTS			OUTPUT
S	I_{0x}	I_{1x}	Q_x
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

l = LOW Voltage Level one setup time prior to the HIGH-to-LOW clock transition.
h = HIGH Voltage Level one setup time prior to the HIGH-to-LOW clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74LS	UNITS	CONDITIONS
		Min	Max			
I_{CC}	Power Supply Current		65	21	mA	I_{0n}, I_{1n}, S = Gnd $\overline{CP}$ = ⊓⊔, V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF R_L = 400 Ω		C_L = 15 pF			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_n		27 32		25 25	ns	Figs. 3-1, 3-9

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW S to $\overline{CP}$	25 25		25 25		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time HIGH or LOW S to $\overline{CP}$	0 0		0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW I_{0x} or I_{1x} to $\overline{CP}$	15 15		15 15		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW I_{0x} or I_{1x} to $\overline{CP}$	5.0 5.0		5.0 5.0		ns	
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width HIGH or LOW	20 20		20 20		ns	Fig. 3-9

54LS/74LS299

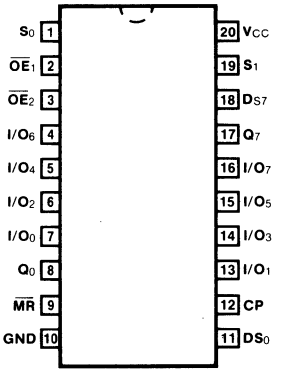
8-INPUT UNIVERSAL SHIFT/STORAGE REGISTER

(With Common Parallel I/O Pins)

DESCRIPTION — The '299 is an 8-bit universal shift/storage register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q_0 and Q_7 to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

- **COMMON I/O FOR REDUCED PIN COUNT**
- **FOUR OPERATION MODES: SHIFT LEFT, SHIFT RIGHT, LOAD AND STORE**
- **SEPARATE SHIFT RIGHT SERIAL INPUT AND SHIFT LEFT SERIAL INPUT FOR EASY CASCADING**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**

CONNECTION DIAGRAM
PINOUT A



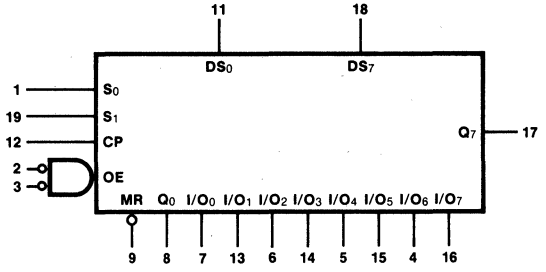
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS299PC		9Z
Ceramic DIP (D)	A	74LS299DC	54LS299DM	4E
Flatpak (F)	A	74LS299FC	54LS299FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
D_{S0}	Serial Data Input for Right Shift	0.5/0.25
D_{S7}	Serial Data Input for Left Shift	0.5/0.25
S_0, S_1	Mode Select Inputs	1.0/0.50
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	0.5/0.25
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)	0.5/0.25
I/O_0 — I/O_7	Parallel Data Inputs or 3-State Parallel Outputs	0.5/0.25 65/15 (25)/(7.5)
Q_0, Q_7	Serial Outputs	10/5.0 (2.5)

LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

FUNCTIONAL DESCRIPTION — The '299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by the S_0 and S_1, as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

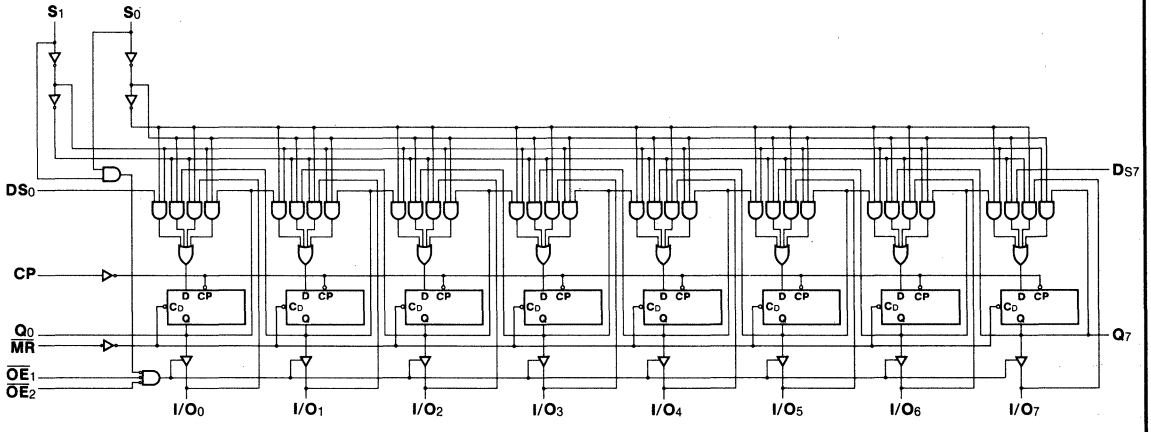
A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

MODE SELECT TABLE

INPUTS				RESPONSE
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; $Q_0 - Q_7$ = LOW
H	H	H	⎍	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⎍	Shift Right; $D_{S0} \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⎍	Shift Left; $D_{S7} \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		65	mA	V_{CC} = Max, $\overline{OE}$ = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		MIN	Max		
f_{max}	Maximum Input Frequency	35		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7		23 25	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n		25 29	ns	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7		30	ns	Figs. 3-1, 3-16
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n		33	ns	
t_{PZH} t_{PZL}	Output Enable Time		18 23	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ
t_{PHZ} t_{PLZ}	Output Disable Time		15 15	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ, C_L = 5 pF

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW S_0 or S_1 to CP	24 24		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW S_0 or S_1 to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW I/O_n, D_{S0}, D_{S7} to CP	10 10		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW I/O_n, D_{S0}, D_{S7} to CP	0 0		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	15 15		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	15		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	10		ns	Fig. 3-16

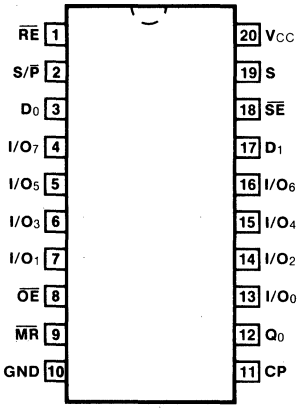
54LS/74LS322

8-BIT SERIAL/PARALLEL REGISTER

(With Sign Extend)

DESCRIPTION — The '322 is an 8-bit shift register with provision for either serial or parallel loading and with 3-state parallel outputs plus a bi-state serial output. Parallel data inputs and parallel outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with sign extend and parallel load. An asynchronous Master Reset ($\overline{MR}$) input overrides clocked operation and clears the register. The '322 is specifically designed for operation with the '384 Multiplier and provides the sign extend function required for the '384.

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

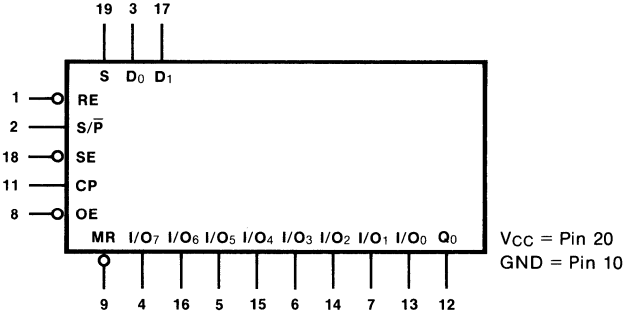
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS322PC		9Z
Ceramic DIP (D)	A	74LS322DC	54LS322DM	4E
Flatpak (F)	A	74LS322FC	54LS322FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

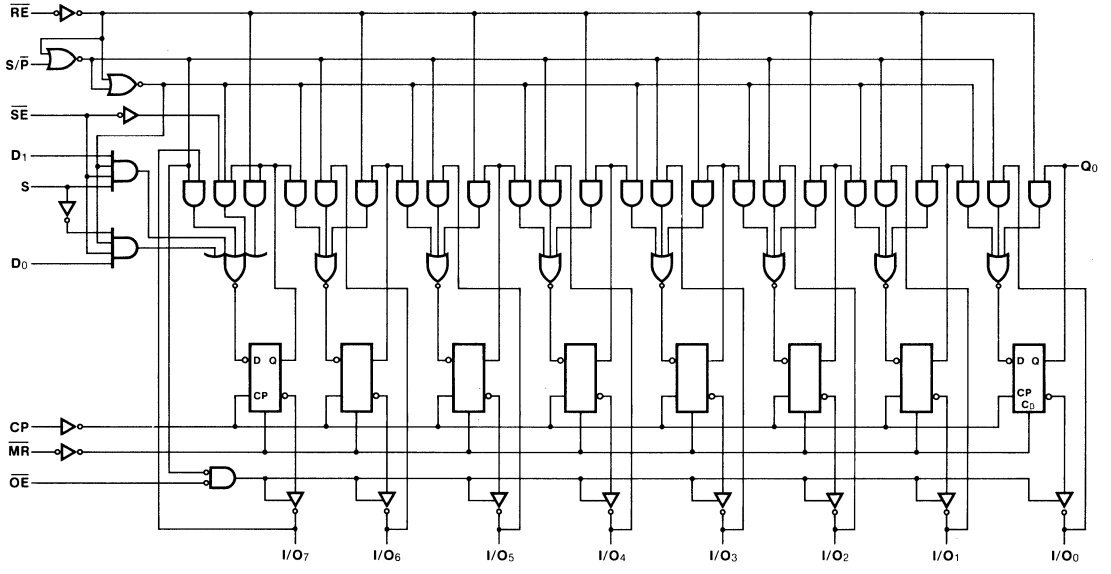
PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$\overline{RE}$	Register Enable Input (Active LOW)	0.5/0.23
S/$\overline{P}$	Serial (HIGH) or Parallel (LOW) Mode Control Input	0.5/0.23
$\overline{SE}$	Sign Extend Input (Active LOW)	1.5/0.68
S	Serial Data Select Input	1.0/0.45
D_0, D_1	Serial Data Inputs	0.5/0.23
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.23
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	0.5/0.23
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.23
Q_0	Bi-State Serial Output	11/5.0 (2.5)
I/O_0 — I/O_7	Multiplexed Parallel Inputs or 3-State Parallel Outputs	0.5/0.23 65/5.0 (25)/(2.5)

FUNCTIONAL DESCRIPTION — The '322 contains eight D-type edge triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A LOW signal on $\overline{RE}$ enables shifting or parallel loading, while a HIGH signal enables the hold mode. A HIGH signal on S/$\overline{P}$ enables shift right, while a LOW signal disables the 3-state output buffers and enables parallel loading. In the shift right mode a HIGH signal on $\overline{SE}$ enables serial entry from either D_0 or D_1, as determined by the S input. A LOW signal on $\overline{SE}$ enables shift right but Q_7 reloads its contents, thus performing the sign extend function required for the '384 Twos Complement Multiplier. A HIGH signal on $\overline{OE}$ disables the 3-state output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

LOGIC SYMBOL



LOGIC DIAGRAM



MODE TABLE

MODE	INPUTS							OUTPUTS								
	$\overline{MR}$	$\overline{RE}$	S/$\overline{P}$	$\overline{SE}$	S	$\overline{OE}$*	CP	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Q_0
Clear	L	X	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	X	X	X	X	H	X	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel Load	H	L	L	X	X	X	⎍	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	I_0
Shift Right	H	L	H	H	L	L	⎍	D_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
	H	L	H	H	H	L	⎍	D_1	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
Sign Extend	H	L	H	L	X	L	⎍	O_7	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
Hold	H	H	X	X	X	L	⎍	NC	NC	NC	NC	NC	NC	NC	NC	NC

*When the $\overline{OE}$ input is HIGH, all I/O_n terminals are at the high-impedance state; sequential operation or clearing of the register is not affected.
1. $I_7 - I_0$ = The level of the steady-state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q_0) are isolated from the I/O terminal.
2. D_0, D_1 = The level of the steady-state inputs to the serial multiplexer input.
3. $O_7 - O_0$ = The level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.

NC = No Change Z = High-Impedance Output State H = HIGH Voltage Level L = LOW Voltage Level

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		60	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	35		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n		23 25	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0		25 29	ns	Figs. 3-1, 3-16
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n		33	ns	Figs. 3-1, 3-16
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0		30	ns	Figs. 3-1, 3-16
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n		18 23	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n		15 15	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ, C_L = 5 pF
t_{PZH} t_{PZL}	Output Enable Time S/$\overline{P}$ to I/O_n		25 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ
t_{PHZ} t_{PLZ}	Output Disable Time S/$\overline{P}$ to I/O_n		23 23	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ, C_L = 5 pF

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{RE}$ to CP	24 24		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{RE}$ to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW D_0, D_1 or I/O_n to CP	10 10		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW D_0, D_1 or I/O_n to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{SE}$ to CP	15 15		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{SE}$ to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW S/$\overline{P}$ to CP	24 24		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW S to CP	15 15		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW S or S/$\overline{P}$ to CP	0 0		ns	
t_w (H)	CP Pulse Width HIGH	15		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	15		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	15		ns	

54LS/74LS323

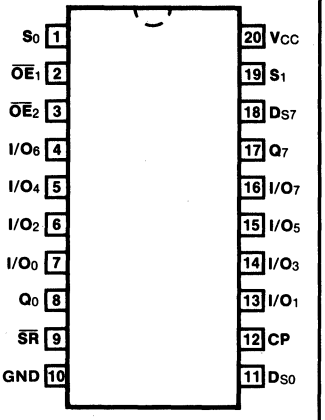
8-BIT UNIVERSAL SHIFT/STORAGE REGISTER

(With Synchronous Reset and Common I/O Pins)

DESCRIPTION — The '323 is an 8-bit universal shift/storage register with 3-state outputs. Its function is similar to the '299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate inputs and outputs are provided for flip-flops Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right, and parallel load. All modes are activated on the LOW-to-HIGH transition of the Clock.

- **COMMON I/O FOR REDUCED PIN COUNT**
- **FOUR OPERATION MODES: SHIFT LEFT, SHIFT RIGHT, PARALLEL LOAD AND STORE**
- **SEPARATE CONTINUOUS INPUTS AND OUTPUTS FROM Q_0 AND Q_7 ALLOW EASY CASCADING**
- **FULLY SYNCHRONOUS RESET**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**

CONNECTION DIAGRAM
PINOUT A



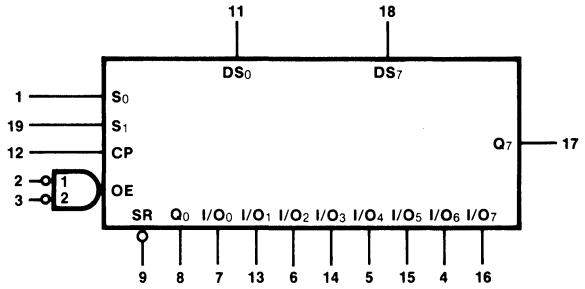
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS323PC		9Z
Ceramic DIP (D)	A	74LS323DC	54LS323DM	4E
Flapak (F)	A	74LS323FC	54LS323FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
D_{S0}	Serial Data Input for Right Shift	0.5/0.25
D_{S7}	Serial Data Input for Left Shift	0.5/0.25
S_0, S_1	Mode Select Inputs	1.0/0.50
$\overline{SR}$	Synchronous Reset Input (Active LOW)	0.5/0.25
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)	0.5/0.25
I/O_0 — I/O_7	Parallel Data Inputs or 3-State Parallel Outputs	1.0/0.50 65/15 (25)/(7.5)
Q_0, Q_7	Serial Outputs	10/5.0 (2.5)

LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

FUNCTIONAL DESCRIPTION — The '323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

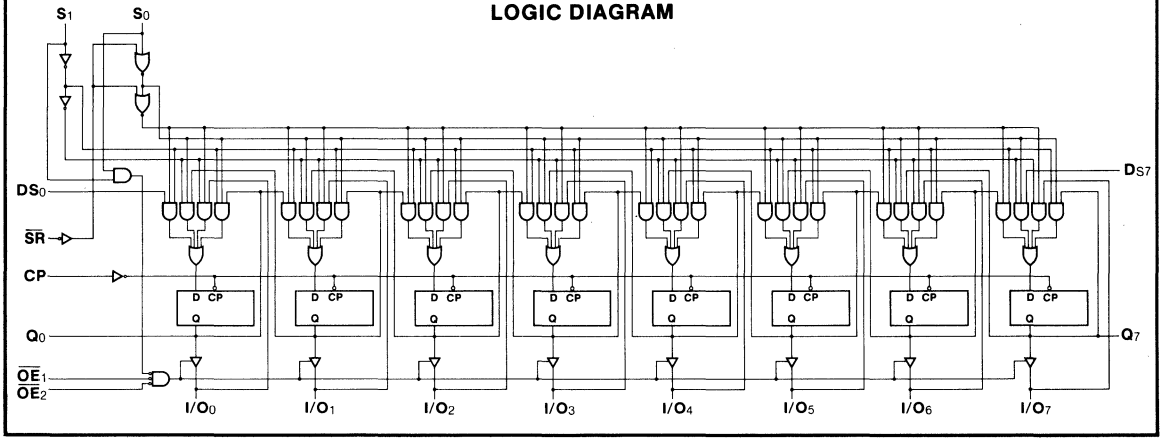
A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

MODE SELECT TABLE

INPUTS				RESPONSE
$\overline{SR}$	S_1	S_0	CP	
L	X	X	⎍	Synchronous Reset; $Q_0 - Q_7$ = LOW
H	H	H	⎍	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⎍	Shift Right; $D_{S0} \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⎍	Shift Left; $D_{S7} \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	H	H	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		60	mA	V_{CC} = Max, Outputs Disabled

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Input Frequency	35		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7		23 25	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n		25 29	ns	
t_{PZH} t_{PZL}	Output Enable Time		18 23	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ
t_{PHZ} t_{PLZ}	Output Disable Time		15 15	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ, C_L = 5 pF

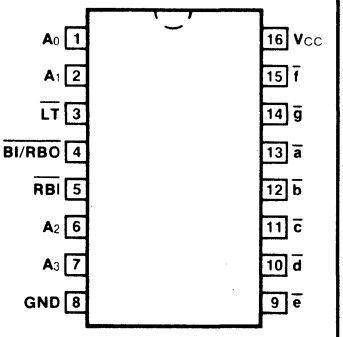
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW S_0 or S_1 to CP	24 24		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW S_0 or S_1 to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW I/O_n, D_{S0}, D_{S7} to CP	10 10		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW I/O_n, D_{S0}, D_{S7} to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{SR}$ to CP	15 15		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{SR}$ to CP	0 0		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	15 15		ns	Fig. 3-8

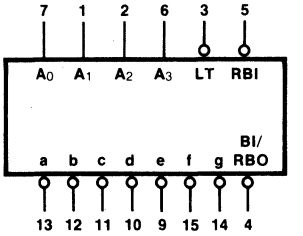
54LS/74LS347

BCD TO 7-SEGMENT DECODER/DRIVER

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

DESCRIPTION — The '347 is the same as the '47 except that the Output OFF Voltage, V_{OH}, is specified as 7.0 V rather than 15 V, with the same I_{OH} limit of 250 μA. For all other information please refer to the '47 data sheet.

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	74LS347PC		9B
Ceramic DIP (D)	A	74LS347DC	54LS347DM	7B
Flatpak (F)	A	74LS347FC	54LS347FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS HIGH/LOW
$A_0 - A_3$	BCD Inputs	0.5/0.25
$\overline{RBI}$	Ripple Blanking Input (Active LOW)	0.5/0.25
$\overline{LT}$	Lamp Test Input (Active LOW)	0.5/0.25
$\overline{BI}/\overline{RBO}$	Blanking Input (Active LOW) or	-/0.75
	Ripple Blanking Output (Active LOW)	1.25/2.0 (1.0)
$\overline{a} - \overline{g}$	Segment Outputs (Active LOW)	OC*/15 (7.5)

*OC — Open Collector

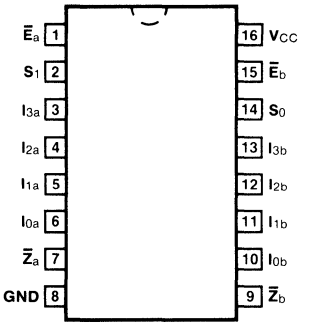
54LS/74LS352

DUAL 4-INPUT MULTIPLEXER

DESCRIPTION — The '352 is a very high speed dual 4-input multiplexer with Common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The '352 is the functional equivalent of the '153 except with inverted outputs.

- **INVERTED VERSION OF THE '153**
- **SEPARATE ENABLES FOR EACH MULTIPLEXER**
- **INPUT CLAMP DIODE LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

CONNECTION DIAGRAM
PINOUT A



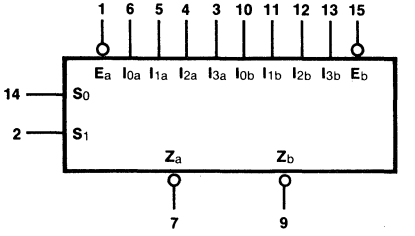
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74LS352PC		9B
Ceramic DIP (D)	A	74LS352DC	54LS352DM	6B
Flatpak (F)	A	74LS352FC	54LS352FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
I_{0a} — I_{3a}	Side A Data Inputs	0.5/0.25
I_{0b} — I_{3b}	Side B Data Inputs	0.5/0.25
S_0, S_1	Common Select Inputs	0.5/0.25
$\bar{E}_a$	Side A Enable Input (Active LOW)	0.5/0.25
$\bar{E}_b$	Side B Enable Input (Active LOW)	0.5/0.25
$\bar{Z}_a$, $\bar{Z}_b$	Multiplexer Outputs (Inverted)	10/5.0 (2.5)

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '352 is a dual 4-input multiplexer. It selects two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs ($\overline{Z}_a$, $\overline{Z}_b$) are forced HIGH.

The logic equations for the outputs are shown below.

$$\overline{Z}_a = \overline{\overline{E}_a \bullet (I_{0a} \bullet S_1 \bullet S_0 + I_{1a} \bullet S_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet S_0 + I_{3a} \bullet S_1 \bullet S_0)}$$

$$\overline{Z}_b = \overline{\overline{E}_b \bullet (I_{0b} \bullet S_1 \bullet S_0 + I_{1b} \bullet S_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet S_0 + I_{3b} \bullet S_1 \bullet S_0)}$$

The '352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is a function generator. The '352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

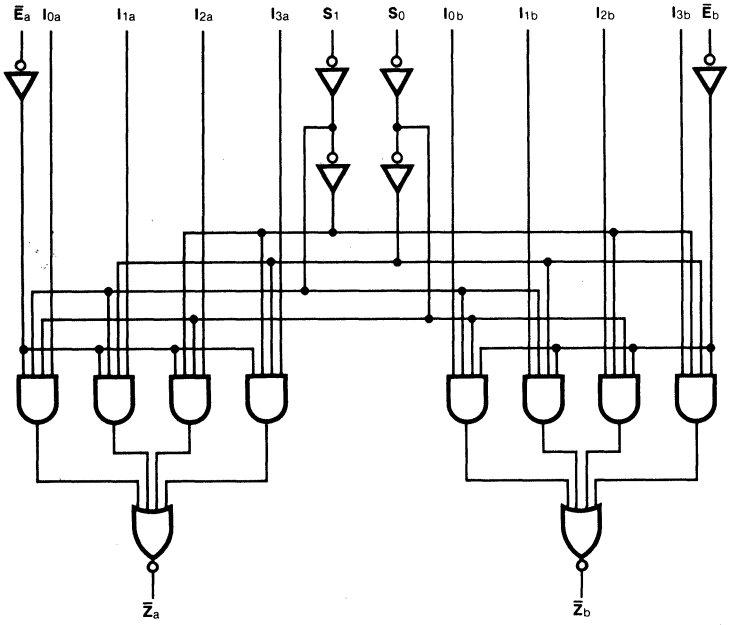
4

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	$\overline{Z}$
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		10	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$		22 38	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$		15 20	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$		12 12	ns	Figs. 3-1, 3-4

54LS/74LS353

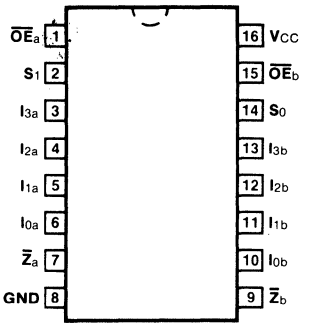
DUAL 4-INPUT MULTIPLEXER

(With 3-State Outputs)

DESCRIPTION — The '353 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

- **INVERTED VERSION OF 'LS253**
- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**

CONNECTION DIAGRAM
PINOUT A



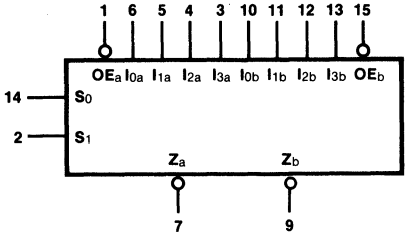
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS353PC		9B
Ceramic DIP (D)	A	74LS353DC	54LS353DM	6B
Flatpak (F)	A	74LS353FC	54LS353FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
I_{0a} — I_{3a}	Side A Data Inputs	0.5/0.25
I_{0b} — I_{3b}	Side B Data Inputs	0.5./0.25
S_0, S_1	Common Select Inputs	0.5/0.25
$\overline{OE}_a$	Side A Output Enable Input (Active LOW)	0.5/0.25
$\overline{OE}_b$	Side B Output Enable Input (Active LOW)	0.5/0.25
$\overline{Z}_a$, $\overline{Z}_b$	3-State Outputs (Inverted)	65/15 (25)/(7.5)

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '353 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which when HIGH, force the outputs to a high impedance (high Z) state. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{\overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)}$$

$$\overline{Z}_b = \overline{\overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)}$$

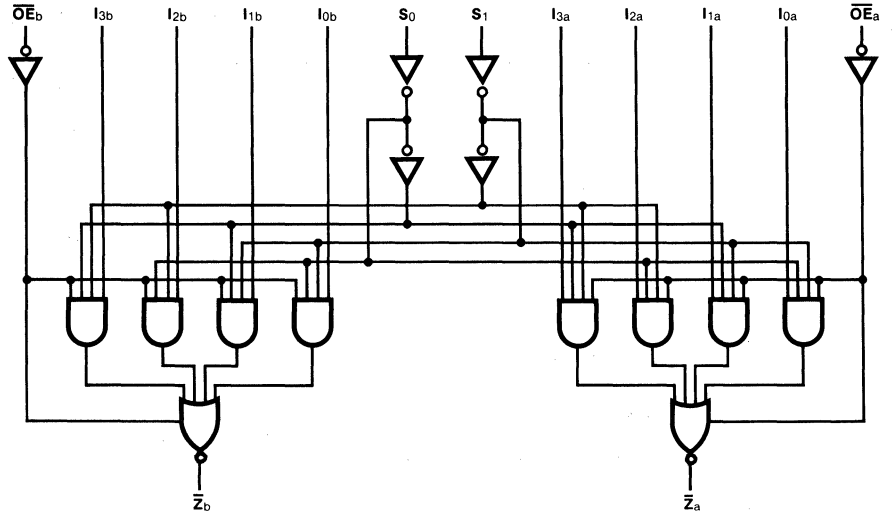
If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	$\overline{Z}$
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs S_0 and S_1 are common to both sections.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High Impedance

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	Outputs HIGH		12	mA	V_{CC} = Max I_n, S_n, $\overline{OE}_n$ = Gnd
		Outputs OFF		14		V_{CC} = Max, $\overline{OE}_n$ = 4.5 V I_n, S_n = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

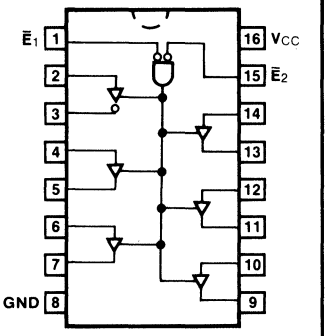
SYMBOL	PARAMETER	54/74LS C_L = 45 pF Min	54/74LS C_L = 45 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$		24 32	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$		15 15	ns	Figs. 3-1, 3-4
t_{PZH} t_{PZL}	Output Enable Time		18 18	ns	Figs. 3-3, 3-11, 3-12 R_L = 667Ω
t_{PHZ} t_{PLZ}	Output Disable Time		18 18	ns	Figs. 3-3, 3-11, 3-12 R_L = 667Ω, C_L = 5 pF

54LS/74LS365A

HEX 3-STATE BUFFER

(With Common 2-Input NOR Enable)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS365APC		9B
Ceramic DIP (D)	A	74LS365ADC	54LS365ADM	6B
Flatpak (F)	A	74LS365AFC	54LS365AFM	4L

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{E}_1$	$\overline{E}_2$	D	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74LS (U.L.) HIGH/LOW
Inputs	0.5/0.25
Outputs	25/15 (7.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current		24	mA	V_{CC} = Max, V_{IN} = 0 V, $V\overline{E}$ = 4.5 V
t_{PLH} t_{PHL}	Propagation Delay Data to Output		16 22	ns	Figs. 3-1, 3-4 C_L = 50 pF
t_{PZH} t_{PZL}	Output Enable Time		24 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 50 pF
t_{PLZ} t_{PHZ}	Output Disable Time		20 25	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 5 pF

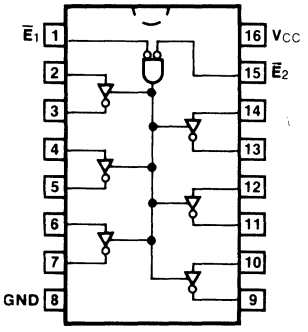
*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54LS/74LS366A

HEX 3-STATE INVERTER BUFFER

(With Common 2-Input NOR Enable)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS366APC		9B
Ceramic DIP (D)	A	74LS366ADC	54LS366ADM	6B
Flatpak (F)	A	74LS366AFC	54LS366AFM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74LS (U.L.) HIGH/LOW
Inputs	0.5/0.25
Outputs	25/15 (7.5)

TRUTH TABLE

INPUTS			OUTPUT
$\overline{E}_1$	$\overline{E}_2$	D	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current		21	mA	V_{CC} = Max, V_{IN} = 0 V, $V\overline{E}$ = 4.5 V
t_{PLH} t_{PHL}	Propagation Delay		12 22	ns	Figs. 3-1, 3-5 C_L = 50 pF
t_{PZH} t_{PZL}	Output Enable Time		24 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 50 pF
t_{PLZ} t_{PHZ}	Output Disable Time		20 25	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 5 pF

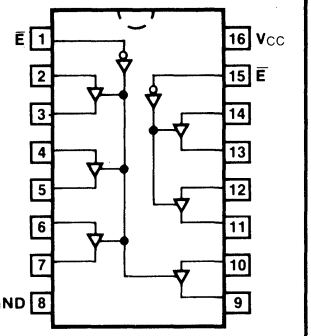
*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54LS/74LS367A

HEX 3-STATE BUFFER

(With Separate 2-Bit and 4-Bit Sections)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10% T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS367APC		9B
Ceramic DIP (D)	A	74LS367ADC	54LS367ADM	6B
Flatpak (F)	A	74LS367AFC	54LS367AFM	4L

TRUTH TABLE

INPUTS		OUTPUT
Ē	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74LS (U.L.) HIGH/LOW
Inputs	0.5/0.25
Outputs	25/15 (7.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current		24	mA	V_{CC} = Max, V_{IN} = 0 V, $V_{\bar{E}}$ = 4.5 V
t_{PLH} t_{PHL}	Propagation Delay		16 22	ns	Figs. 3-1, 3-4 C_L = 50 pF
t_{PZH} t_{PZL}	Output Enable Time		24 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 50 pF
t_{PLZ} t_{PHZ}	Output Disable Time		20 25	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 5 pF

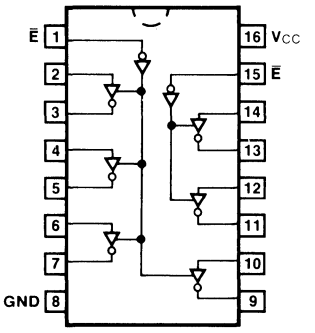
*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54LS/74LS368A

HEX 3-INPUT INVERTER BUFFER

(With Separate 2-Bit and 4-Bit Sections)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS368APC		9B
Ceramic DIP (D)	A	74LS368ADC	54LS368ADM	6B
Flatpak (F)	A	74LS368AFC	54LS368AFM	4L

TRUTH TABLE

INPUTS $\overline{E}$	INPUTS D	OUTPUT
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74LS (U.L.) HIGH/LOW
Inputs	0.5/0.25
Outputs	25/15 (7.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current		21	mA	V_{CC} = Max, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V
t_{PLH} t_{PHL}	Propagation Delay		12 22	ns	Figs. 3-1, 3-5 C_L = 50 pF
t_{PZH} t_{PZL}	Output Enable Time		24 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 50 pF
t_{PLZ} t_{PHZ}	Output Disable Time		20 25	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 5 pF

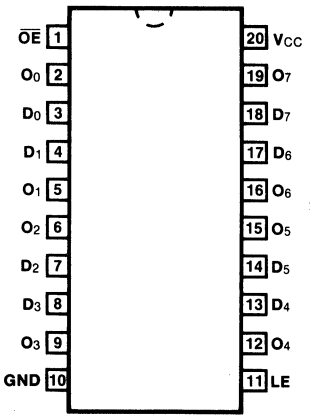
*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54LS/74LS373

OCTAL TRANSPARENT LATCH

(With 3-State Outputs)

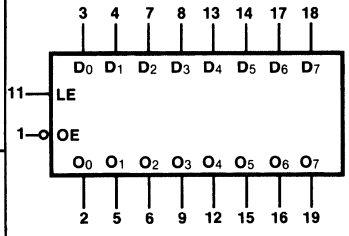
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

- **EIGHT LATCHES IN A SINGLE PACKAGE**
- **3-STATE OUTPUTS FOR BUS INTERFACING**

LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

ORDERING CODE: See Section 9

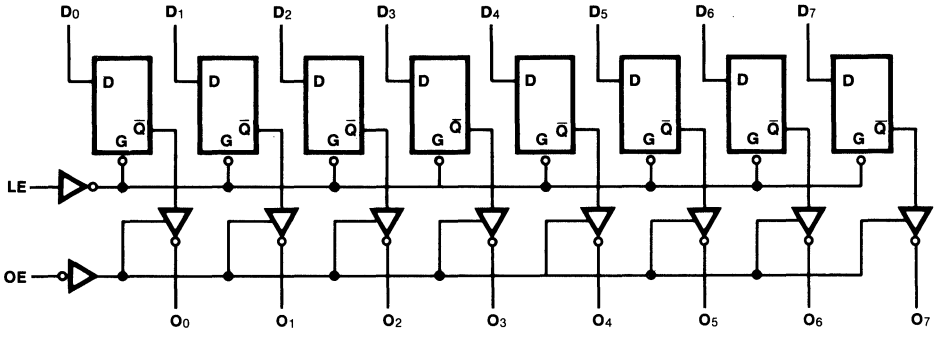
PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS373PC		9Z
Ceramic DIP (D)	A	74LS373DC	54LS373DM	4E
Flatpak (F)	A	74LS373FC	54LS373FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$D_0 - D_7$	Data Inputs	0.5/0.25
LE	Latch Enable Input (Active HIGH)	0.5/0.25
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.25
$O_0 - O_7$	3-State Latch Outputs	65/15 (25)/(7.5)

FUNCTIONAL DESCRIPTION — The '373 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	Outputs OFF		40	mA	V_{CC} = Max, $\overline{OE}$ = 4.5 V D_n, LE = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 50 pF Min	Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n		18 20	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay LE to O_n		30 30	ns	Figs. 3-1, 3-8
t_{PZH} t_{PZL}	Output Enable Time		28 36	ns	Figs. 3-3, 3-11, 3-12 R_L = 667Ω
t_{PHZ} t_{PLZ}	Output Disable Time		20 25	ns	Figs. 3-3, 3-11, 3-12 R_L = 667Ω, C_L = 5.0 pF

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to LE	0 0		ns	Fig. 3-14
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to LE	10 10		ns	
t_w (H) t_w (L)	LE Pulse Width HIGH or LOW	15 15		ns	Fig. 3-8

54LS/74LS374

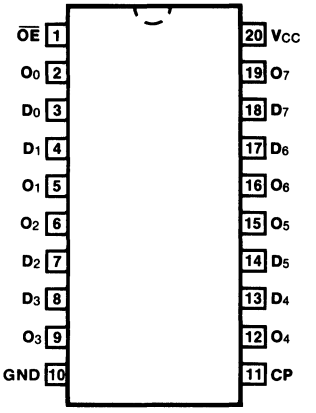
OCTAL D-TYPE FLIP-FLOP

(With 3-State Outputs)

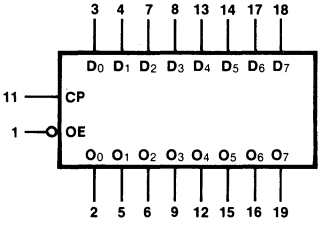
DESCRIPTION — The '374 is a high speed, low power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) is common to all flip-flops. The '374 is manufactured using advanced low power Schottky technology and is compatible with all Fairchild TTL families.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

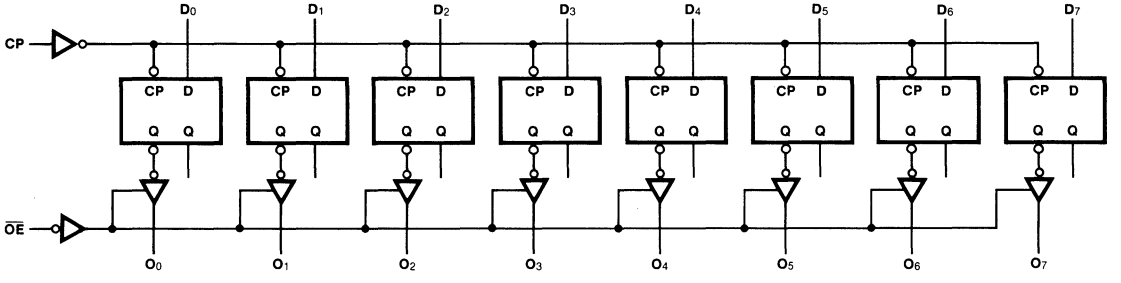
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS374PC		9Z
Ceramic DIP (D)	A	74LS374DC	54LS374DM	4E
Flatpak (F)	A	74LS374FC	54LS374FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$D_0 - D_7$	Data Inputs	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.25
$O_0 - O_7$	3-State Outputs	65/15 (25)/(7.5)

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The '374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedence state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

TRUTH TABLE

INPUTS			OUTPUTS
D_n	CP	OE	O_n
H	⎍	L	H
L	⎍	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current, Outputs OFF		45	mA	V_{CC} = Max, D_n = Gnd $\overline{OE}$ = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 45 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	35		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to O_n		28 28	ns	Figs. 3-1, 3-8
t_{PZH} t_{PZL}	Output Enable Time		28 28	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω
t_{PHZ} t_{PLZ}	Output Disable Time		20 25	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 5 pF

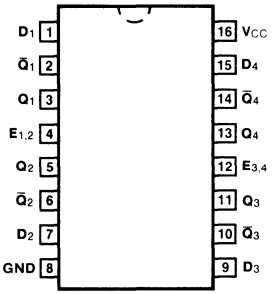
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to CP	20 20		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to CP	0 0		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	15 15		ns	Fig. 3-8

54LS/74LS375

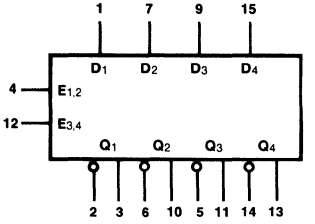
4-BIT LATCH

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '375 is a 4-bit D-type latch for use as temporary storage for binary information between processing units and input/output or indicator units. When its Enable (E) input is HIGH, a latch is transparent, i.e., the Q output will follow the D input each time it changes. When E is LOW a latch stores the last valid data present on the D input preceding the HIGH-to-LOW transition of E. The '375 is functionally identical to the '75 except for the corner power pins.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

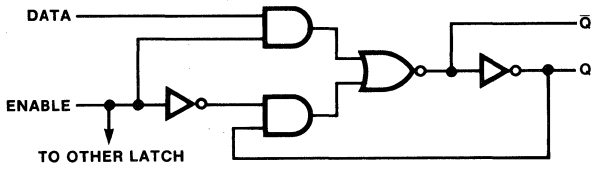
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS375PC		9B
Ceramic DIP (D)	A	74LS375DC	54LS375DM	6B
Flatpak (F)	A	74LS375FC	54LS375FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L.definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$D_1 - D_4$	Data Inputs	0.5/0.25
$E_{1,2}$	Latches 1, 2 Enable Input	2.0/1.0
$E_{3,4}$	Latches 3, 4 Enable Input	2.0/1.0
$Q_1 - Q_4$	Latch Outputs	10/5.0 (2.5)
$\bar{Q}_1 - \bar{Q}_4$	Complementary Latch Outputs	10/5.0 (2.5)

LOGIC DIAGRAM
(1/4 of diagram shown)



TRUTH TABLE
(Each Latch)

t_n	t_{n+1}
D	Q
H	H
L	L

t_n = Bit time before Enable negative going transition.
t_{n+1} = Bit time after Enable negative going transition.
H = HIGH Voltage Level
L = LOW Voltage Level

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		12	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		27 17	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{Q}_n$		20 15	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay E_n to Q_n		27 25	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay E_n to $\overline{Q}_n$		30 15	ns	

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

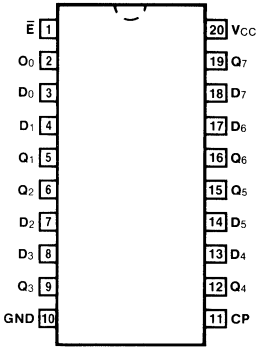
SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to E_n	20		ns	Fig. 3-14
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to E_n	0		ns	
t_w (H)	E_n Pulse Width HIGH	20		ns	Fig. 3-8

54LS/74LS377

OCTAL D FLIP-FLOP

(With Common Enable and Clock)

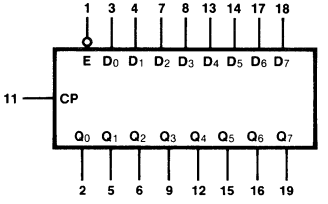
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '377 is an 8-bit register built using advanced low power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common input enable. The device is packaged in the space-saving (0.3 inch row spacing) 20-pin package.

- **8-BIT HIGH SPEED PARALLEL REGISTERS**
- **POSITIVE EDGE-TRIGGERED D-TYPE FLIP-FLOPS**
- **FULLY BUFFERED COMMON CLOCK AND ENABLE INPUTS**

LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS377PC		9Z
Ceramic DIP (D)	A	74LS377DC	54LS377DM	4E
Flatpak (F)	A	74LS377FC	54LS377FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$\overline{E}$	Enable Input (Active LOW)	0.5/0.25
$D_0 - D_7$	Data Inputs	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$Q_0 - Q_7$	Flip-flop Outputs	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '377 consists of eight edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable input ($\overline{E}$) are common to all flip-flops.

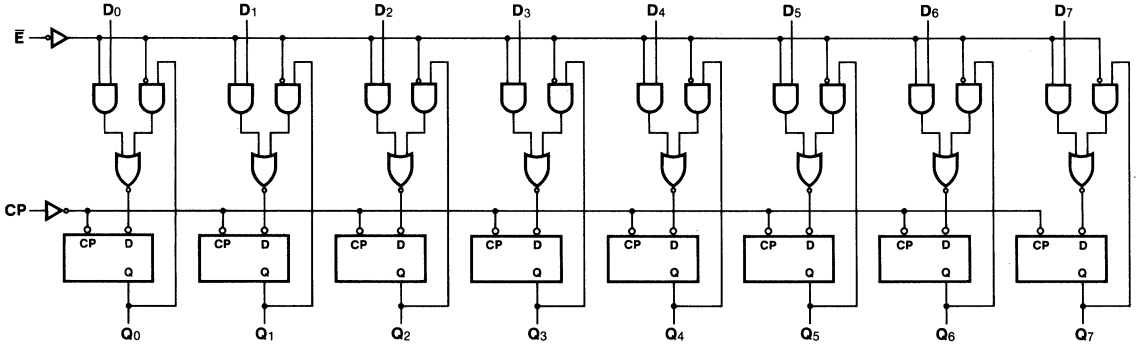
When $\overline{E}$ is LOW, new data is entered into the register on the next LOW-to-HIGH transition of CP. When $\overline{E}$ is HIGH, the register will retain the present data independent of the CP.

TRUTH TABLE

INPUTS			OUTPUT
$\overline{E}$	CP	D_n	Q_n
H	X	X	No change
L	⎍	H	H
L	⎍	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		28	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		C_L = 15 pF			
		Min	Max		
f_{max}	Maximum Clock Frequency	30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		25 25	ns	Figs. 3-1, 3-8

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

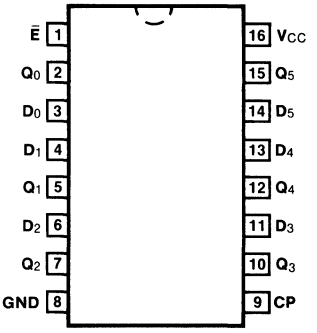
SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to CP	10 10		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to CP	5.0 5.0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{E}$ to CP	10 20		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{E}$ to CP	5.0 5.0		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	20 20		ns	Fig. 3-8

54LS/74LS378

PARALLEL D REGISTER

(With Enable)

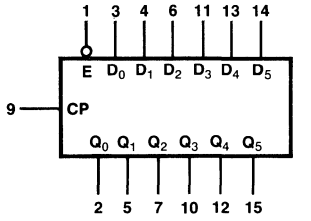
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '378 is a 6-bit register with a buffered common enable. This device is similar to the '174, but with common Enable rather than common Master Reset.

- **6-BIT HIGH SPEED PARALLEL REGISTER**
- **POSITIVE EDGE-TRIGGERED D-TYPE INPUTS**
- **FULLY BUFFERED COMMON CLOCK AND ENABLE INPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULL TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS378PC		9B
Ceramic DIP (D)	A	74LS378DC	54LS378DM	6B
Flatpak (F)	A	74LS378FC	54LS378FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
Ē	Enable Input (Active LOW)	0.5/0.25
D0 — D5	Data Inputs	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
Q0 — Q5	Flip-flop Outputs	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '378 consists of eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops.

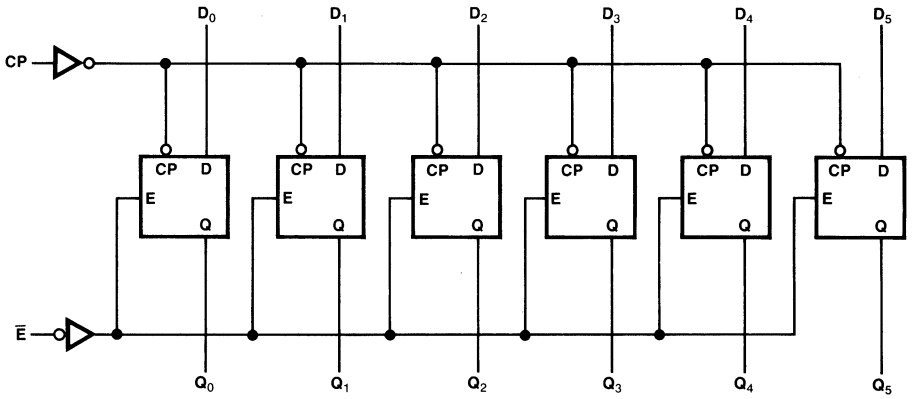
When the $\overline{E}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the $\overline{E}$ input is HIGH the register will retain the present data independent of the CP input.

TRUTH TABLE

INPUTS			OUTPUT
$\overline{E}$	CP	D_n	Q_n
H	⎍⎍	X	No change
L	⎍⎍	H	H
L	⎍⎍	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		22	mA	V_{CC} = Max, D_n = $\overline{E}$ = Gnd CP = ⎍⎾

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		C_L = 15 pF			
		Min	Max		
f_{max}	Maximum Clock Frequency	30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		27 27	ns	Figs. 3-1, 3-8

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

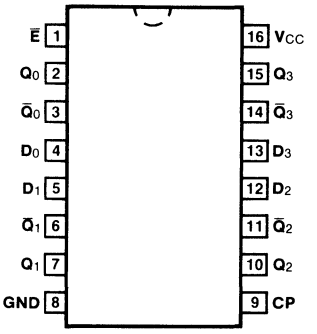
SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H)	Setup Time HIGH, D_n to CP	20		ns	Fig. 3-6
t_h (H)	Hold Time HIGH, D_n to CP	5.0		ns	Fig. 3-6
t_s (L)	Setup Time LOW, D_n to CP	20		ns	Fig. 3-6
t_h (L)	Hold Time LOW, D_n to CP	5.0		ns	Fig. 3-6
t_s (H)	Setup Time HIGH, $\overline{E}$ to CP	30		ns	Fig. 3-6
t_h (H)	Hold Time HIGH, $\overline{E}$ to CP	5.0		ns	Fig. 3-6
t_s (L)	Setup Time LOW, $\overline{E}$ to CP	30		ns	Fig. 3-6
t_h (L)	Hold Time LOW, $\overline{E}$ to CP	5.0		ns	Fig. 3-6
t_w (H)	CP Pulse Width HIGH	20		ns	Fig. 3-8

54LS/74LS379

QUAD PARALLEL REGISTER

(With Enable)

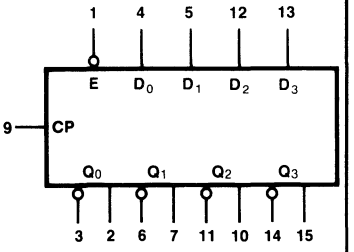
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '379 is a 4-bit register with buffered common Enable. This device is similar to the '175 but features the common Enable rather than common Master Reset.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **BUFFERED COMMON ENABLE INPUT**
- **TRUE AND COMPLEMENT OUTPUTS**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS379PC		9B
Ceramic DIP (D)	A	74LS379DC	54LS379DM	6B
Flatpak (F)	A	74LS379FC	54LS379FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$\overline{E}$	Enable Input (Active LOW)	0.5/0.25
$D_0 - D_3$	Data Inputs	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$Q_0 - Q_3$	Flip-flop Outputs	10/5.0 (2.5)
$\overline{Q}_0 - \overline{Q}_3$	Complement Outputs	10/5.0 (2.5)

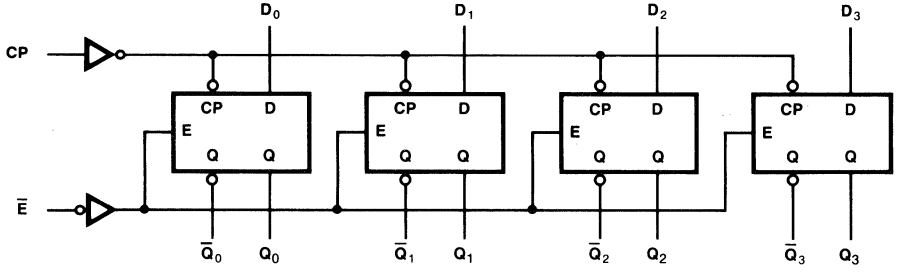
FUNCTIONAL DESCRIPTION — The '379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops. When the $\overline{E}$ input is HIGH, the register will retain the present data independent of the CP input. The D_n and $\overline{E}$ inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed.

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	⎍	X	No Change	No Change
L	⎍	H	H	L
L	⎍	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		18	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		27 27	ns	

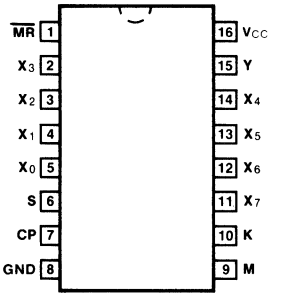
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to CP	20 20		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to CP	5.0 5.0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{E}$ to CP	25 25		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{E}$ to CP	5.0 5.0		ns	
t_w (L)	CP Pulse Width LOW	17		ns	Fig. 3-8

54LS/74LS384

8-BIT SERIAL/PARALLEL TWOS COMPLEMENT MULTIPLIER

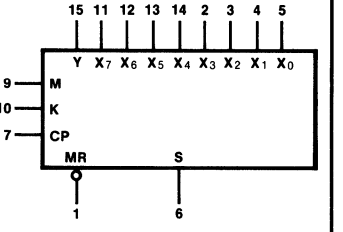
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '384 is an 8-bit by 1-bit sequential logic element that multiplies two numbers represented in twos complement notation. The device implements Booth's algorithm internally to produce a twos complement product that needs no subsequent correction. Parallel inputs accept and store an 8-bit multiplicand (X_0 — X_7). The multiplier word is applied to the Y input in a serial bit stream, least significant bit first. The product is clocked out at the S output, least significant bit first.

The K input is used for expansion to longer X words, using two or more '384 packages. The Mode Control (M) input is used to establish the most significant package. An asynchronous Master Reset ($\overline{MR}$) input clears the internal flip-flops to the start condition and enables the X latches to accept new multiplicand data.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

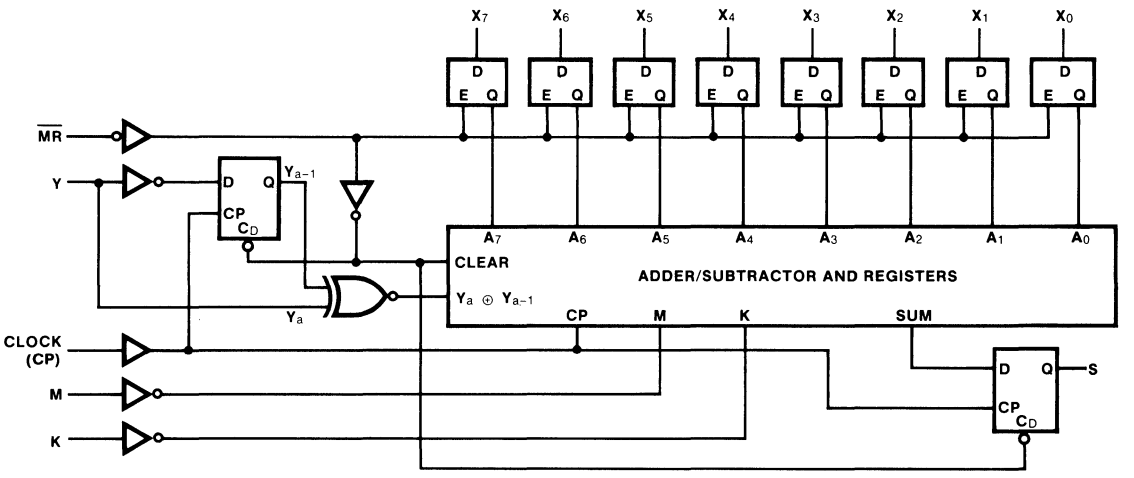
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS384PC		9B
Ceramic DIP (D)	A	74LS384DC	54LS384DM	6B
Flatpak (F)	A	74LS384FC	54LS384FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0
K	Serial Expansion Input	0.75/0.75
M	Mode Control Input	0.5/0.3
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	0.75/0.75
X_0 — X_7	Multiplicand Data Inputs	0.5/0.3
Y	Serial Multiplier Input	2.0/2.0
S	Serial Product Output	25/7.5 (5.0)

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						INTERNAL	OUTPUT	FUNCTION
$\overline{MR}$	CP	K	M	X_i	Y	Y_{a-1}	S	
-		L	L					Most Significant Multiplier Device
-		CS	H					Devices Cascaded in Multiplier String
L				OP		L	L	Load New Multiplicand and Clear Internal Sum and Carry Registers
H								Device Enabled
H	⌐¬				L	L	AR	Shift Sum Register
H	⌐¬				L	H	AR	Add Multiplicand to Sum Register and Shift
H	⌐¬				H	L	AR	Subtract Multiplicand from Sum Register and Shift
H	⌐¬				H	H	AR	Shift Sum Register

⌐¬ = LOW-to-HIGH transition
CS = Connected to S output of high order device
OP = X_i latches open for new data (i = 0, 7)
AR = Output as required per Booth's algorithm

FUNCTIONAL DESCRIPTION — Referring to the logic diagram, the multiplicand (X_0 — X_7) latches are enabled to receive new data when $\overline{MR}$ is LOW. Data that meet the setup time requirements is latched and stored when $\overline{MR}$ goes HIGH. The LOW signal on MR also clears the Y_{a-1} flip-flop as well as the carry-save flip-flops and the partial product register in the arithmetic section. *Figure a* is a conceptual logic diagram of a typical cell in the arithmetic section, except for the first (X_7) cell, in which K is the B_i input and M is incorporated into the carry logic. The cells use the carry-save technique to avoid the complexity and delays inherent in look-ahead carry schemes for longer words.

Figure b is a timing diagram for an 8 x 8 multiplication process. New multiplicand data enters the X latches during bit time T_0. It is assumed that MR goes LOW shortly after the CP rising edge that marks the beginning of T_0 and goes HIGH again shortly after the beginning of T_1. The LSB (Y_0) of the multiplier is applied to the Y input during T_1 and combines with X_0 in the least significant cell to form the appropriate D input (X_0 Y_0) to the sum flip-flop. This is clocked into the sum flip-flop by the CP rising edge at the beginning of T_2 and this LSB (S_0) of the product is available shortly thereafter at the S output of the package. The next-least bit Y_1 of the multiplier is also applied during T_2. The detailed logic design of the cell is such that during T_2 the D input to the sum flip-flop of the least significant cell contains not only X_0Y_1 but also, thanks to storage in its carry flip-flop and in the sum flip-flop of the next-least cell, the X_1Y_0 product. Thus the term ($X_1Y_0 + X_0Y_1$) is formed at the D input of the least significant sum flip-flop during T_2 and this next-least term S_1 of the product is available at the S output shortly after the CP rising edge at the beginning of T_3. Due to storage in the two preceding cells and in its own carry flip-flop, the D input to the least significant sum flip-flop during T_3 will contain the products X_2Y_0 and X_1Y_1 as well as X_0Y_2. During each succeeding bit time the S output contains information formed one stage further upstream. For example, the S output during T_9 contains X_7Y_0, which was actually formed during T_1.

The MSB Y_7 (the sign bit Y_S) of the multiplier is first applied to the Y input during T_8 and must also be applied during bit times T_9 through T_{16}. This extension of the sign bit is a necessary adjunct to the implementation of Booth's algorithm and is a built-in feature of the '322 Shift Register. *Figure c* shows the method of using two '384s to perform a 12 x n bit multiplication. Notice that the sign of X is effectively extended by connecting X_{11} to X_4 — X_7 of the most significant package. Whereas the 8 x 8 multiplication required 18 clock periods (m + n to form the product terms plus T_0 to clear the multiplier plus T_{17} to recognize and store S_{15}), the arrangement of *Figure c* requires 12 + n bits to form the product terms plus the bit times to clear the multiplier and to recognize and store S_{n+11}.

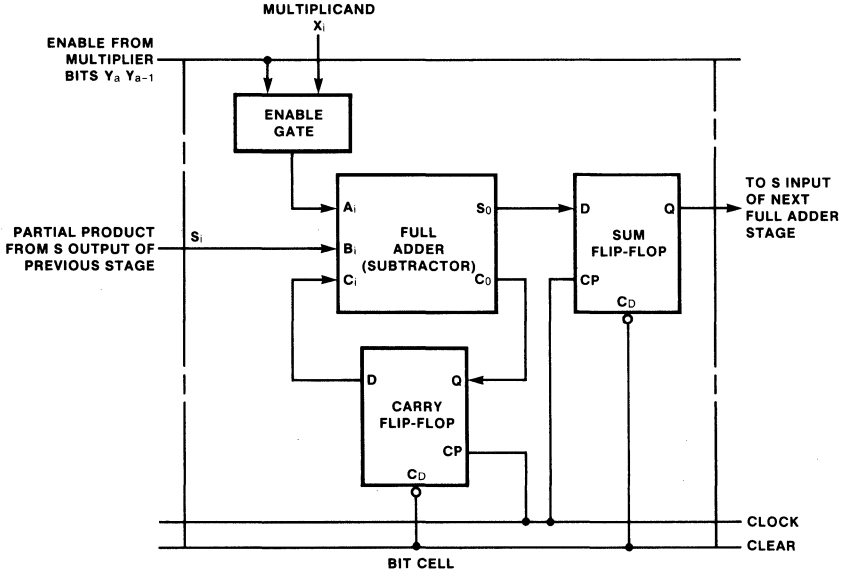


Fig. a Conceptual Carry Save Adder Cell

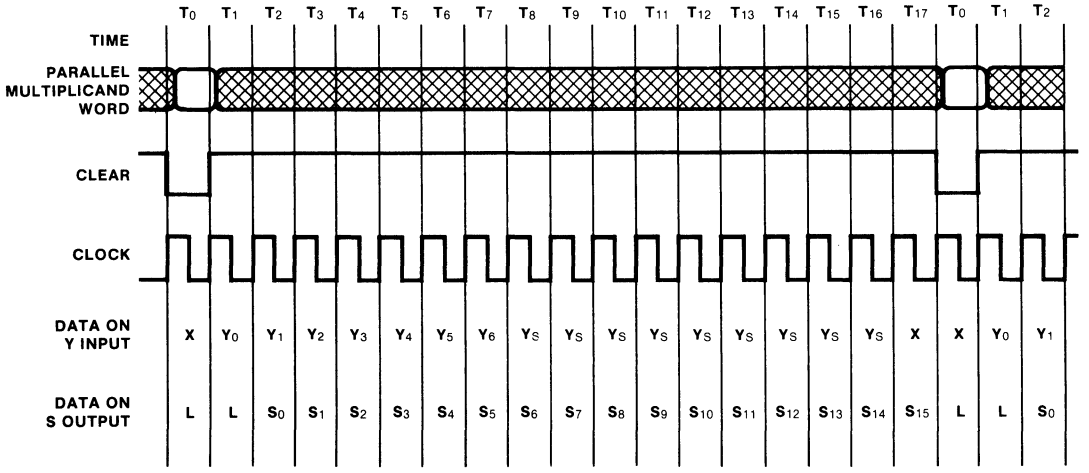


Fig. b Timing Diagram Showing 18 Clock Cycle Operation of 8 x 8 Multiplication

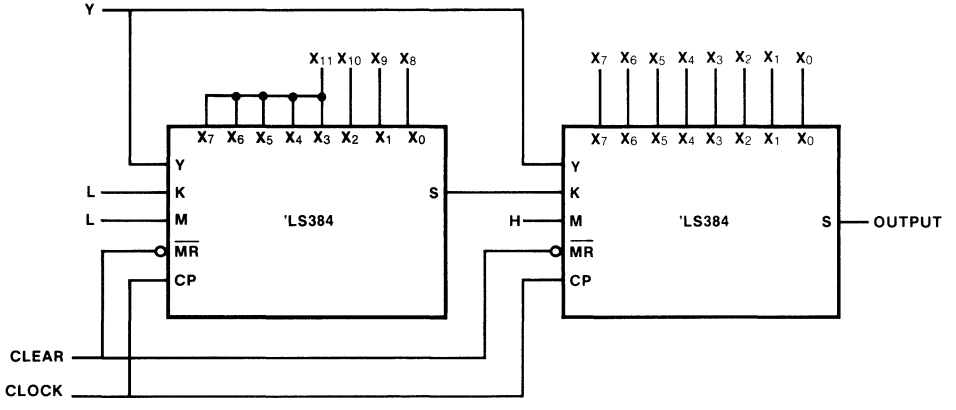


Fig. c A 12-Bit by N-Bit Two's Complement Multiplier

DC CHARATERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{OS}	Output Short Circuit Current	-20	-100	mA	V_{CC} = Max
I_{CC}	Power Supply Current		155	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	25		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to S		20 20	ns	
t_{PHL}	Propagation Delay $\overline{MR}$ to S		25	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW K to CP	18 18		ns	Fig. 3-6
t_s (H) t_s (L)	Setup Time HIGH or LOW Y to CP	32 32		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW K or Y to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW X_i to $\overline{MR}$	13 13		ns	Fig. 3-13
t_h (H) t_h (L)	Hold Time HIGH or LOW X_i to $\overline{MR}$	0 0		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	15 15		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	18		ns	

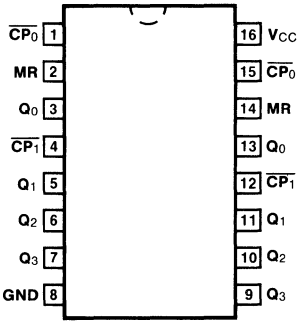
54LS/74LS390

DUAL DECADE COUNTER

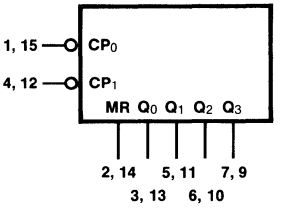
DESCRIPTION — The '390 contains a pair of high speed 4-stage ripple counters. Each half of the '390 is partitioned into a divide-by-two section and a divide-by-five section, with a separate clock input for each section. The two sections can be connected to count in the 8421 BCD code or they can count in a bi-quinary sequence to provide a square wave (50% duty cycle) at the final output.

Each half of the '390 contains a ÷5 section that is independent except for the common MR function. The ÷5 section operates in 421 binary sequence, as shown in the ÷5 Truth Table, with the third stage output exhibiting a 20% duty cycle when the input frequency is constant. To obtain a ÷10 function having a 50% duty cycle output, connect the input signal to $\overline{CP}_1$ and connect the Q_3 output to the $\overline{CP}_0$ input; the Q_0 output provides the desired 50% duty cycle output. If the input frequency is connected to $\overline{CP}_0$ and the Q_0 output is connected to $\overline{CP}_1$, a decade divider operating in the 8421 BCD code is obtained, as shown in the BCD Truth Table. Since the flip-flops change state asynchronously, logic signals derived from combinations of '390 outputs are also subject to decoding spikes. A HIGH signal on MR forces all outputs LOW and prevents counting.

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

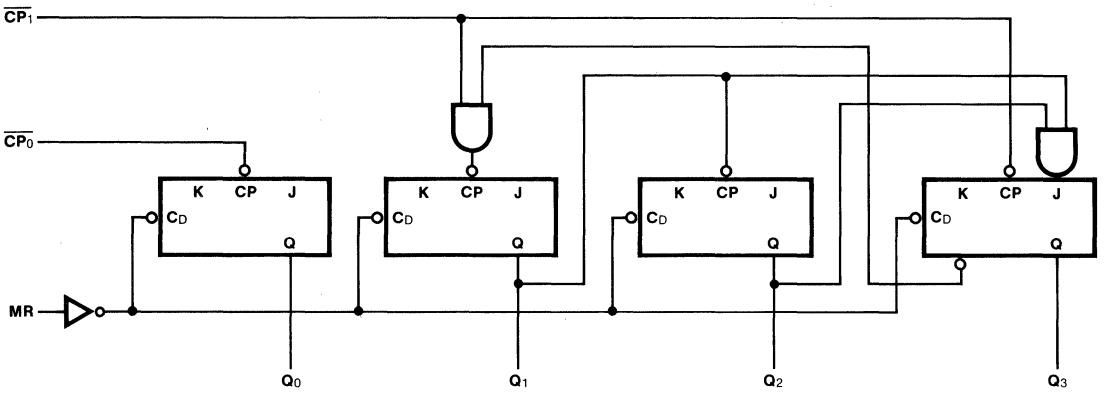
PKGS	PIN OUT	COMMERCIAL GRADE: V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE: V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS390PC		9B
Ceramic DIP (D)	A	74LS390DC	54LS390DM	6B
Flatpak (F)	A	74LS390FC	54LS390FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$\overline{CP}_0$	÷2 Section Clock Input (Active Falling Edge)	1.0/1.5
$\overline{CP}_1$	÷5 Section Clock Input (Active Falling Edge)	2.0/2.0
MR	Asynchronous Master Reset Input (Active HIGH)	0.5/0.25
Q_0 — Q_3	Flip-flop Outputs*	10/5.0 (2.5)

*The Q_0 Output is guaranteed to drive the full rated fan-out plus the $\overline{CP}_1$ input.

LOGIC DIAGRAM (one half shown)



BCD TRUTH TABLE
(Input on $\overline{CP_0}$; Q_0 to $\overline{CP_1}$)

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

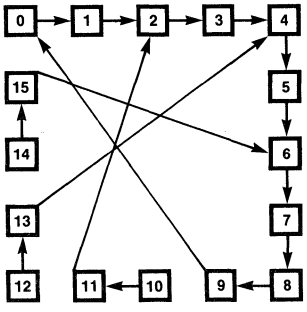
H = HIGH Voltage Level
L = LOW Voltage Level

÷5 TRUTH TABLE
(Input on $\overline{CP_1}$)

COUNT	OUTPUTS		
	Q_3	Q_2	Q_1
0	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level

STATE DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{IH}	Input HIGH Current, $\overline{CP}_0$, $\overline{CP}_1$			0.1	mA	V_{CC} = Max, V_{IN} = 5.5 V
I_{CC}	Power Supply Current	'390		30	mA	V_{CC} = Max
		'393				

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF Min	54/74LS C_L = 15 pF Max	UNITS	CONDITIONS
f_{max}	Maximum Count Frequency $\overline{CP}_0$ ('390) or $\overline{CP}$ ('393)	40		MHz	Figs. 3-1, 3-9
f_{max}	$\overline{CP}_1$ Maximum Count Frequency	20		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_0$ ('390) or $\overline{CP}$ ('393) to Q_0		15 15	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_1$ ('390) to Q_1		21 21	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_1$ ('390) to Q_2		30 30	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_1$ ('390) to Q_3		21 21	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ ('393) to Q_1		30 30	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ ('393) to Q_2		40 40	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ ('393) to Q_3		54 54	ns	Figs. 3-1, 3-9
t_{PHL}	Propagation Delay MR to Q_n		35	ns	Figs. 3-1, 3-17

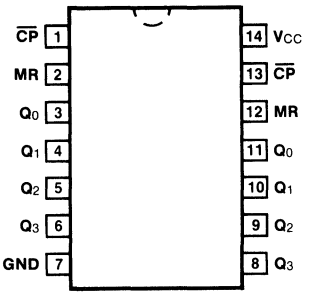
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_w (L)	CP or CP_0 Pulse Width LOW	12		ns	Fig. 3-9
t_w (L)	CP_1 Pulse Width LOW	25		ns	Fig. 3-9
t_w (H)	MR Pulse Width HIGH	20		ns	Fig. 3-17
t_{rec}	Recovery Time MR to CP	15		ns	Fig. 3-17

54LS/74LS393

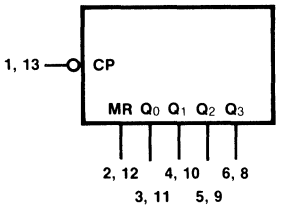
DUAL MODULO-16 COUNTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '393 contains a pair of high speed 4-stage ripple counters. Each half of the '393 operates as a modulo-16 binary divider, with the last three stages triggered in a ripple fashion. The flip-flops are triggered by a HIGH-to-LOW transition of their $\overline{CP}$ inputs. Each half of each circuit type has a Master Reset input which responds to a HIGH signal by forcing all four outputs to the LOW state. For detail specifications, please refer to the '390 data sheet.

LOGIC SYMBOL
(each half)



V_{CC} = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

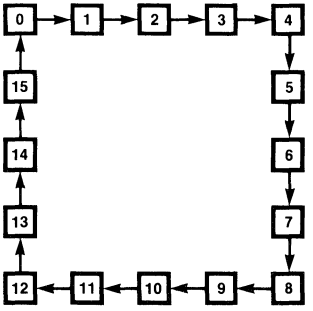
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS393PC		9A
Ceramic DIP (D)	A	74LS393DC	54LS393DM	6A
Flatpak (F)	A	74LS393FC	54LS393FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	1.0/1.5
MR	Asynchronous Master Reset Input (Active HIGH)	0.5/0.25
Q_0 — Q_3	Flip-flop Outputs	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — Each half of the '393 operates in the modulo-16 binary sequence, as indicated in the ÷16 Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the $\overline{CP}$ input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs do not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting.

STATE DIAGRAM

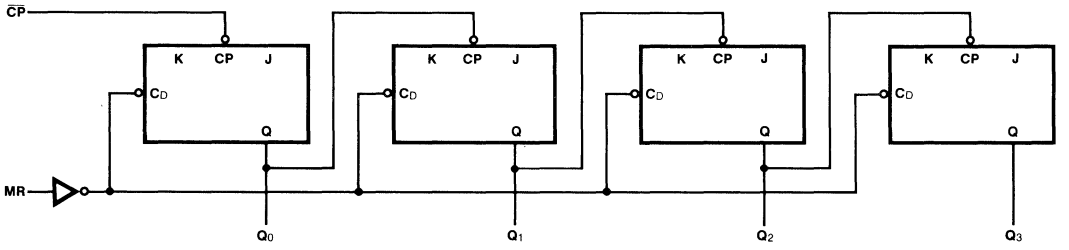


TRUTH TABLE

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM (one half shown)



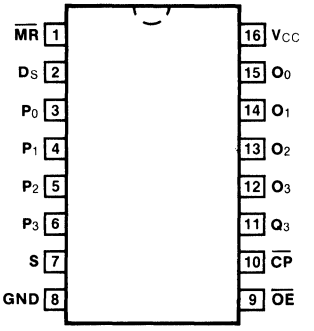
54LS/74LS395

4-BIT SHIFT REGISTER
(With 3-State Outputs)

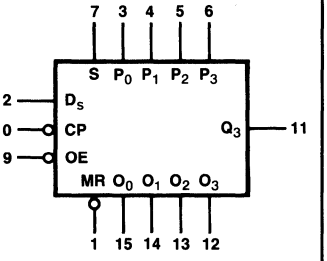
DESCRIPTION — The '395 is a 4-bit register with 3-state outputs and can operate in either a synchronous parallel load or a serial shift-right mode, as determined by the Select input. An asynchronous active LOW Master Reset ($\overline{MR}$) input overrides the synchronous operations and clears the register. An active LOW Output Enable ($\overline{OE}$) input controls the 3-state output buffers, but does not interfere with the other operations. The fourth stage also has a conventional output for linking purposes in multi-stage serial operations.

- **SHIFT RIGHT OR PARALLEL 4-BIT REGISTER**
- **3-STATE OUTPUTS**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY CMOS AND TTL COMPATIBLE**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS395PC		9B
Ceramic DIP (D)	A	74LS395DC	54LS395DM	6B
Flatpak (F)	A	74LS395FC	54LS395FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$P_0 - P_3$	Parallel Data Inputs	0.5/0.25
D_S	Serial Data Input	0.5/0.25
S	Mode Select Input	0.5/0.25
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	0.5/0.25
$\overline{MR}$	Master Reset Input (Active LOW)	0.5/0.25
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.25
$O_0 - O_3$	3-State Register Outputs	65/5.0 (25)/(2.5)
Q_3	Flip-flop Output	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '395 contains four D-type edge-triggered flip-flops and auxiliary gating to select a D input either from a Parallel (P_n) input or from the preceding stage. When the Select input is HIGH, the P_n inputs are enabled. A LOW signal on the S input enables the serial inputs for shift-right operations, as indicated in the Truth Table.

State changes are initiated by HIGH-to-LOW transitions on the Clock Pulse ($\overline{CP}$) input. Signals on the P_n, D_S and S inputs can change when the Clock is in either state, provided that the recommended setup and hold times are ovserved. When the S input is LOW, a $\overline{CP}$ HIGH-LOW transition transfers data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3. A left-shift is accomplished by connecting the outputs back to the P_n inputs, but offset one place to the left, i.e., O_3 to P_2, O_2 to P_1, and O_1 to P_0, with P_3 acting as the linking input from another package.

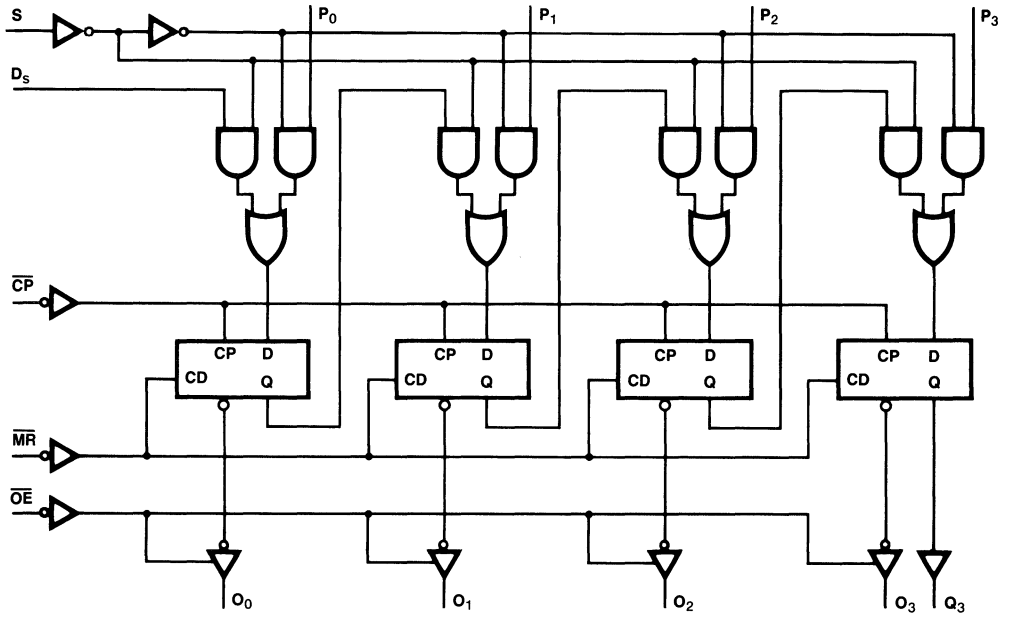
When the $\overline{OE}$ input is HIGH, the output buffers are disabled and the O_0 — O_3 outputs are in a high impedance condition. The shifting, parallel loading or resetting operations can still be accomplished, however.

MODE SELECT TABLE

OPERATING MODE	INPUTS @ t_n					OUTPUTS @ t_{n+1}			
	$\overline{MR}$	$\overline{CP}$	S	D_S	P_n	O_0	O_1	O_2	O_3
Asynchronous Reset	L	X	X	X	X	L	L	L	L
Shift, SET First Stage	H	⊓	L	H	X	H	O_{0n}	O_{1n}	O_{2n}
Shift, RESET First Stage	H	⊓	L	L	X	L	O_{0n}	O_{1n}	O_{2n}
Parallel Load	H	⊓	H	X	P_n	P_0	P_1	P_2	P_3

t_n, t_{n+1} = Time before and after CP HIGH-to-LOW transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current		-20	-100	mA	V_{CC} = Max
I_{CC}	Power Supply Current	Output OFF		29	mA	V_{CC} = Max; P_n = Gnd $\overline{CP}$ = ⌜⌞ $\overline{OE}$, D_S, S = 4.5 V
		Outputs ON		25		V_{CC} = Max; D_S, S = 4.5 V $\overline{OE}$, $\overline{CP}$, P_n = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF Min	54/74LS C_L = 15 pF Max	UNITS	CONDITIONS
f_{max}	Maximum Shift Frequency	30		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to O_n		35 25	ns	Figs. 3-1, 3-9
t_{PHL}	Propagation Delay $\overline{MR}$ to O_n		35	ns	Figs. 3-1, 3-17
t_{PZH} t_{PZL}	Output Enable Time		20 20	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ
t_{PHZ} t_{PLZ}	Output Disable Time		17 23	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ C_L = 5 pF

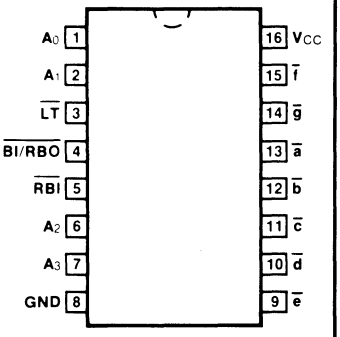
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW S, D_S or P_n to $\overline{CP}$	20 20		ns	Fig. 3-7
t_h (H) t_h (L)	Hold Time HIGH or LOW S, D_S or P_n to $\overline{CP}$	5.0 5.0		ns	Fig. 3-7
t_w (L)	$\overline{CP}$ Pulse Width LOW	18		ns	Fig. 3-9
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		ns	Fig. 3-17

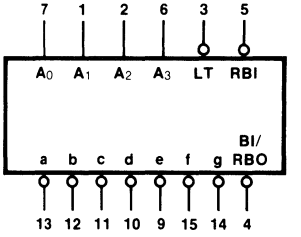
54LS/74LS447

BCD TO 7-SEGMENT DECODER/DRIVER

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

DESCRIPTION — The '447 is the same as the '247 except that the Output OFF Voltage, V_{OH}, is specified as 7.0 V rather than 15 V, with the same I_{OH} limit of 250 μA. For all other information please refer to the '247 data sheet.

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	
Plastic DIP (P)	A	74LS447PC		9B
Ceramic DIP (D)	A	74LS447DC	54LS447DM	7B
Flatpak (F)	A	74LS447FC	54LS447FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	BCD Inputs	0.5/0.25
$\overline{RBI}$	Ripple Blanking Input (Active LOW)	0.5/0.25
$\overline{LT}$	Lamp Test Input (Active LOW)	0.5/0.25
$\overline{BI}/\overline{RBO}$	Blanking Input (Active LOW) or	-/0.75
	Ripple Blanking Output (Active LOW)	1.25/2.0 (1.0)
$\overline{a} - \overline{g}$	Segment Outputs (Active LOW)	OC*/15 (7.5)

*OC — Open Collector

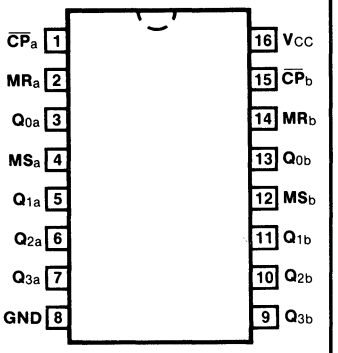
54LS/74LS490

DUAL DECADE COUNTER

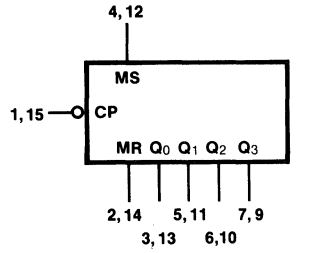
DESCRIPTION — The '490 contains a pair of high speed 4-stage ripple counters. Each half of the '490 has individual Clock, Master Reset and Master Set (Preset 9) inputs. Each section counts in the 8421 BCD code.

- **DUAL VERSION OF 54LS/74LS90**
- **INDIVIDUAL ASYNCHRONOUS CLEAR AND PRESET TO 9 FOR EACH COUNTER**
- **COUNT FREQUENCY — TYPICALLY 65 MHz**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **TTL AND CMOS COMPATIBLE**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

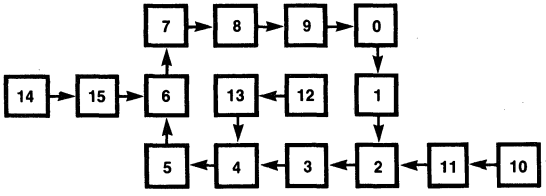
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS490PC		9B
Ceramic DIP (D)	A	74LS490DC	54LS490DM	6B
Flatpak (F)	A	74LS490FC	54LS490FM	4L

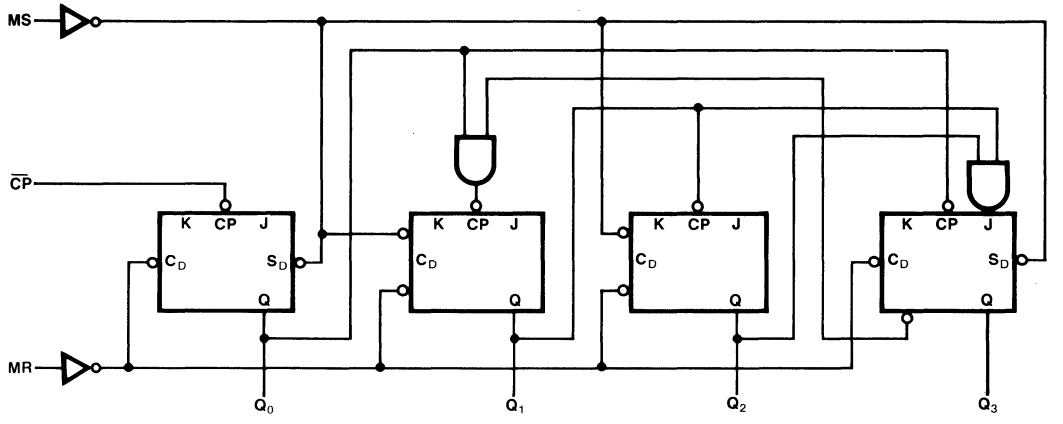
INPUT LOADING/FAN-OUT: See Section 3 for U.L definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
MS	Master Set (Set to 9) Input (Active HIGH)	0.5/0.25
MR	Master Reset Input (Active HIGH)	0.5/0.25
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	1.5/1.5
$Q_0 - Q_3$	Counter Outputs	10/5.0 (2.5)

STATE DIAGRAM



LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		26	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Count Frequency	40		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_0		15 15	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_1 or Q_3		30 30	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_2		45 45	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay MS to Q_n		35 35	ns	Figs. 3-1, 3-17
t_{PHL}	Propagation Delay MR to Q_n		39	ns	Figs. 3-1, 3-17

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_w (H)	$\overline{CP}$ Pulse Width HIGH	20		ns	Fig. 3-9
t_w (H)	MR, MS Pulse Width HIGH	20		ns	Fig. 3-17
t_{rec}	Recovery Time, MR or MS to $\overline{CP}$	15		ns	Fig. 3-17

54LS/74LS502

8-BIT SUCCESSIVE APPROXIMATION REGISTER

DESCRIPTION—The 'LS502 is an 8-bit register with the interstage logic necessary to perform serial-to-parallel conversion and provide an active LOW Conversion Complete ($\overline{CC}$) signal coincident with storage of the eighth bit. An active LOW Start ($\overline{S}$) input performs synchronous initialization which forces Q_7 LOW and all other outputs HIGH. Subsequent clocks shift this Q_7 LOW signal downstream which simultaneously backfills the register such that the first serial data (D input) bit is stored in Q_7, the second bit in Q_6, the third in Q_5, etc. The serial input data is also synchronized by an auxiliary flip-flop and brought out on Q_D.

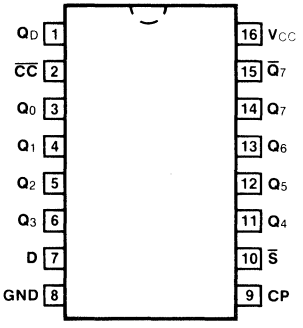
Designed primarily for use in the successive approximation technique for analog-to-digital conversion, the 'LS502 can also be used as a serial-to-parallel converter ring counter and as the storage and control element in recursive digital routines.

- **LOW POWER SCHOTTKY VERSION OF 2502**
- **STORAGE AND CONTROL FOR SUCCESSIVE APPROXIMATION A TO D CONVERSION**
- **PERFORMS SERIAL-TO-PARALLEL CONVERSION**

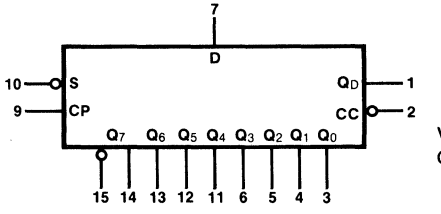
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74LS502PC		9B
Ceramic DIP (D)	A	74LS502DC	54LS502DM	6B
Flatpak (F)	A	74LS502FC	54LS502FM	4L

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL

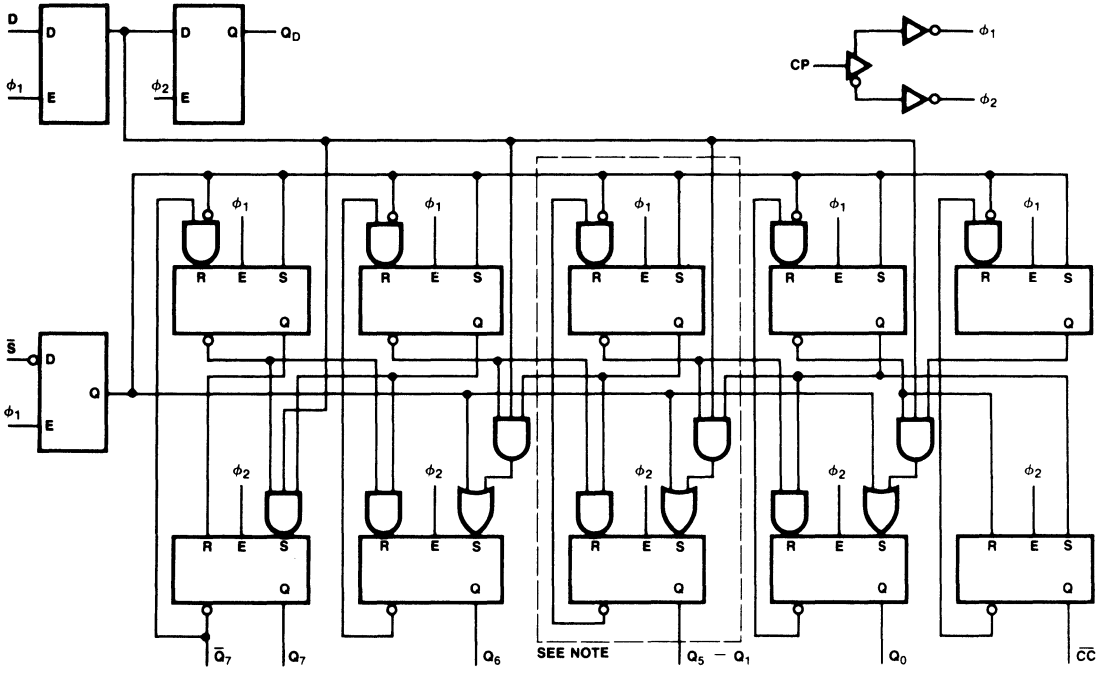


V_{CC} = Pin 16
GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
D	Serial Data Input	0.5/0.25
$\overline{S}$	Start Input (Active LOW)	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
Q_D	Synchronized Serial Data Output	10/5.0 (2.5)
$\overline{CC}$	Conversion Complete Output (Active LOW)	10/5.0 (2.5)
$Q_0 - Q_7$	Parallel Register Outputs	10/5.0 (2.5)
$\overline{Q}_7$	Complement of Q_7 Output	10/5.0 (2.5)

LOGIC DIAGRAM



Note: Cell logic is repeated for register stages Q_5 to Q_1.

FUNCTIONAL DESCRIPTION — The register stages are composed of transparent RS latches arranged in master/slave pairs. The master and slave latches are enabled separately by non-overlapping complementary signals ϕ_1 and ϕ_2 derived internally from the CP input. Master latches are enabled when CP is LOW and slave latches are enabled when CP is HIGH. Information is transferred from master to slave, and thus to the outputs, by the LOW-to-HIGH transition of CP.

Initializing the register requires a LOW signal on $\overline{S}$ while exercising CP. With $\overline{S}$ and CP LOW, all master latches are SET (Q side HIGH). A LOW-to-HIGH CP transition, with $\overline{S}$ remaining LOW, then forces the slave latches to the condition wherein Q_7 is LOW and all other register outputs, including $\overline{CC}$, are HIGH. This condition will prevail as long as $\overline{S}$ remains LOW, regardless of subsequent CP rising edge. To start the conversion process, $\overline{S}$ must return to the HIGH state. On the next CP rising edge, the information stored in the serial data input latch is transferred to Q_D and Q_7, while Q_6 is forced to the LOW state. On the rising edge of the next seven clocks, this LOW signal is shifted downstream, one bit at a time, while the serial data enters the register position one bit behind this LOW signal, as shown in the Truth Table. Note that after a serial data bit appears at a particular output, that register position undergoes no further changes. After the shifted LOW signal reaches $\overline{CC}$, the register is locked up and no further changes can occur until the register is initialized for the next conversion process.

Figure a shows a simplified hook-up of a 'LS502, a D/A converter and a comparator arranged to convert an analog input voltage into an 8-bit binary number by the successive approximation technique. *Figure b* is an idealized graph showing the various values that the D/A converter output voltage can assume in the course of the conversion. The vertical axis is calibrated in fractions of the full-scale output capability of the D/A converter and the horizontal axis represents the successive states of the Truth Table. At time t_1, Q_7 is LOW and $Q_6 - Q_0$ are HIGH, causing the D/A output to be one-half of full scale. If the analog input voltage is greater than this voltage the comparator output (hence the D input of the 'LS502) will be LOW, and at times t_2 the D/A output will rise to three-fourths of full scale because Q_7 will remain LOW and contribute 50% while Q_6 is forced LOW and contributes another 25%. On the other hand, if the analog input voltage is less than one-half of full scale, the comparator output will be HIGH and Q_7 will go HIGH at t_2. Q_6 will still be forced LOW at t_2, and the D/A output will decrease to 25% of full scale. Thus with each successive clock, the D/A output will change by smaller increments. When the conversion is completed at t_9, the binary number represented by the register outputs will be the numerator of the fraction n/256, representing the analog input voltage as a fraction of the fullscale output D/A converter.

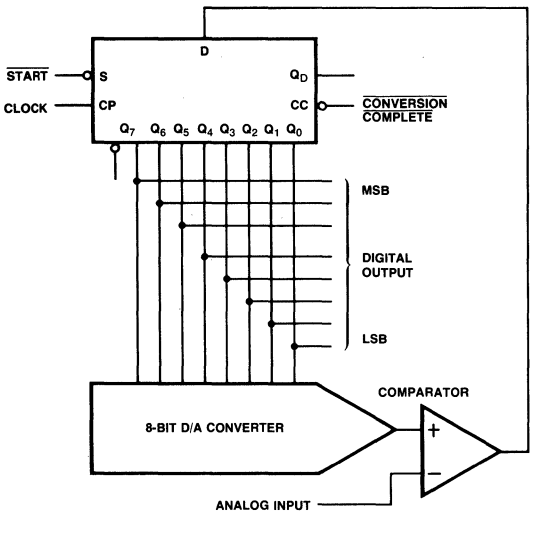


Fig. a

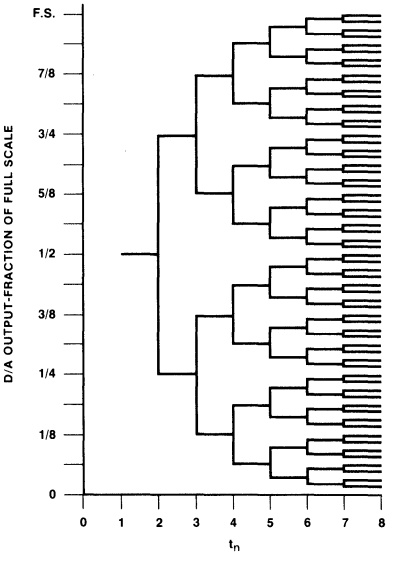


Fig. b

TRUTH TABLE

Time	INPUTS		OUTPUTS									
t_n	D	$\overline{S}$	Q_D	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{CC}$
0	X	L	X	X	X	X	X	X	X	X	X	X
1	D_7	H	X	L	H	H	H	H	H	H	H	H
2	D_6	H	D_7	D_7	L	H	H	H	H	H	H	H
3	D_6	H	D_6	D_7	D_6	L	H	H	H	H	H	H
4	D_4	H	D_5	D_7	D_6	D_5	L	H	H	H	H	H
5	D_3	H	D_4	D_7	D_6	D_5	D_4	L	H	H	H	H
6	D_2	H	D_3	D_7	D_6	D_5	D_4	D_3	L	H	H	H
7	D_1	H	D_2	D_7	D_6	D_5	D_4	D_3	D_2	L	H	H
8	D_0	H	D_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	L	H
9	X	H	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
10	X	H	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

4

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		65	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for U.L. waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	15		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n or $\overline{CC}$		38 28	ns	

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{S}$ to CP	16 16		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{S}$ to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW D to CP	8.0 8.0		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D to CP	10 10		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	20 46		ns	Fig. 3-8

54LS/74LS503

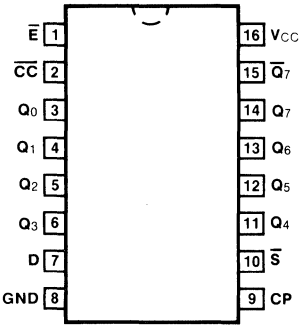
8-BIT SUCCESSIVE APPROXIMATION REGISTER

(With Expansion Control)

DESCRIPTION — The 'LS503 register is basically the same as the 'LS502 except that it has an active LOW Enable ($\overline{E}$) input that is used in cascading two or more packages for longer word lengths. A HIGH signal on $\overline{E}$, after a START operation, forces Q_7 HIGH and prevents the device from accepting serial data. With the $\overline{E}$ input of an 'LS503 connected to the $\overline{CC}$ output of a preceding (more significant) device, the 'LS503 will be inhibited until the preceding device is filled, causing its $\overline{CC}$ output to go LOW. This LOW signal then enables the 'LS503 to accept the serial data on subsequent clocks. For a description of the starting, shifting and conversion operations, please see the 'LS502 data sheet.

- **PERFORMS SERIAL-TO-PARALLEL CONVERSION**
- **EXPANSION CONTROL FOR LONGER WORDS**
- **STORAGE AND CONTROL FOR SUCCESSIVE APPROXIMATION A TO D CONVERSION**
- **LOW POWER SCHOTTKY VERSION OF 2503**

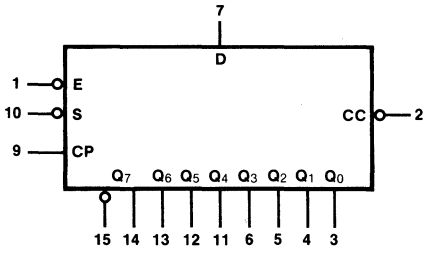
CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74LS503PC		9B
Ceramic DIP (D)	A	74LS503DC	54LS503DM	6B
Flatpak (F)	A	74LS503FC	54LS503FM	4L

LOGIC SYMBOL

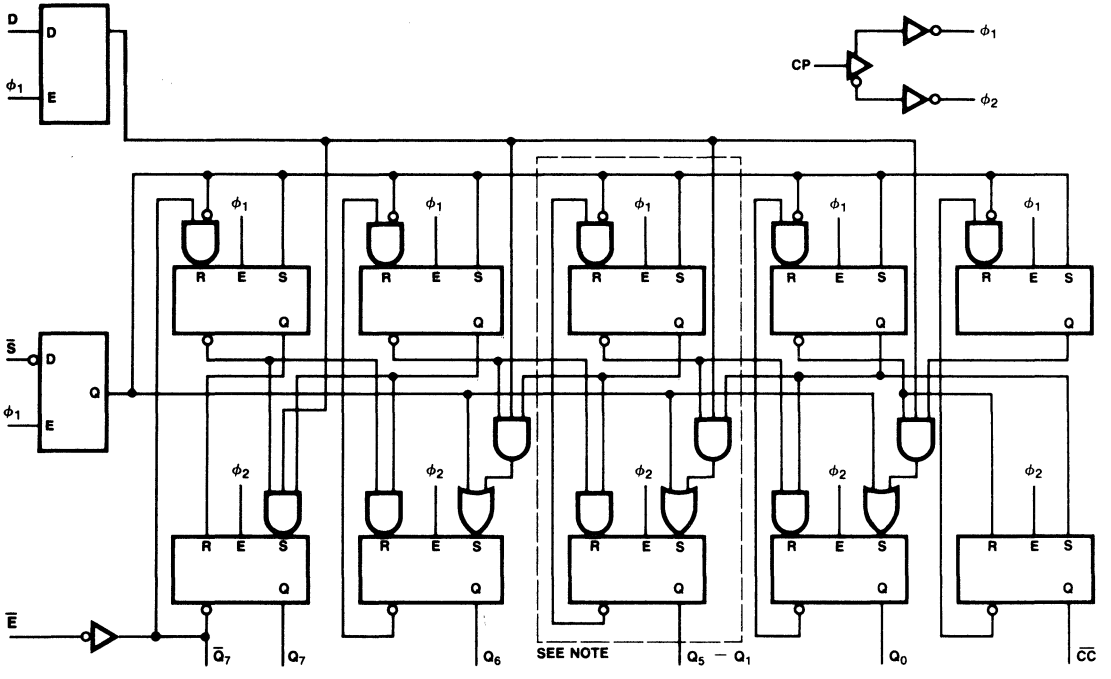


V_{CC} = Pin 16
GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

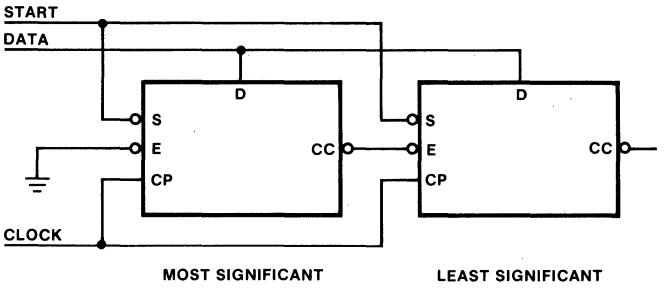
PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
D	Serial Data Input	0.5/0.25
$\overline{S}$	Start Input (Active LOW)	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$\overline{E}$	Conversion Enable Input (Active LOW)	10/5.0 (2.5)
$\overline{CC}$	Conversion Complete Output (Active LOW)	10/5.0 (2.5)
$Q_0 - Q_7$	Parallel Register Outputs	10/5.0 (2.5)
$\overline{Q}_7$	Complement of Q_7 Output	10/5.0 (2.5)

LOGIC DIAGRAM



Note: Cell logic is repeated for register stages Q_5 to Q_1.

CONNECTION FOR LONGER WORD LENGTHS



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		65	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	15		MHz	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n or $\overline{CC}$		38 28	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_7		19 24	ns	Figs. 3-1, 3-5 CP = 4.5 V, $\overline{S}$ = Gnd

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

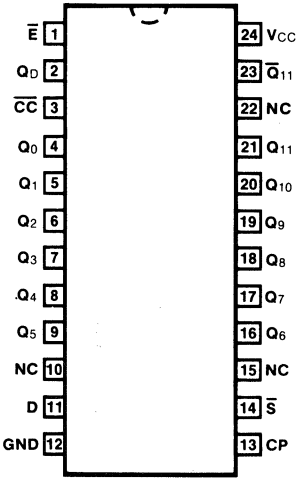
SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{S}$ to CP	16 16		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{S}$ to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW D to CP	8.0 8.0		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D to CP	10 10		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	20 46		ns	Fig. 3-8

54LS/74LS504

12-BIT SUCCESSIVE APPROXIMATION REGISTER

(With Expansion Control)

CONNECTION DIAGRAM
PINOUT A



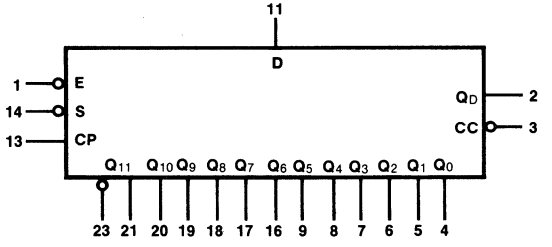
DESCRIPTION — The 'LS504 performs serial-to-parallel conversion and provides a Conversion Complete ($\overline{CC}$) signal. The 'LS504 is a 12-bit version of the 8-bit 'LS502 and has an active LOW Enable ($\overline{E}$) input for expansion, similar to the 'LS503. For detailed discussion of the various operations, please see the 'LS502 and 'LS503 data sheets.

- **PERFORMS SERIAL-TO-PARALLEL CONVERSION**
- **EXPANSION CONTROL FOR LONGER WORDS**
- **STORAGE AND CONTROL FOR SUCCESSIVE APPROXIMATION A TO D CONVERSION**
- **LOW POWER SCHOTTKY VERSION OF 2504**

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS504PC		9N
Ceramic DIP (D)	A	74LS504DC	54LS504DM	6N
Flatpak (F)	A	74LS504FC	54LS504FM	4M

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
D	Serial Data Input	0.5/0.25
$\overline{S}$	Start Input (Active LOW)	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$\overline{E}$	Conversion Enable Input (Active LOW)	0.5/0.25
Q_D	Synchronized Serial Data Output	10/5.0 (2.5)
$\overline{CC}$	Conversion Complete Output (Active LOW)	10/5.0 (2.5)
$Q_0 - Q_{11}$	Parallel Register Outputs	10/5.0 (2.5)
$\overline{Q}_{11}$	Complement of Q_{11} Output	10/5.0 (2.5)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		90	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	15		MHz	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n or $\overline{CC}$		38 28	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_7		19 24	ns	Figs. 3-1, 3-5 CP = 4.5, $\overline{S}$ = Gnd

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

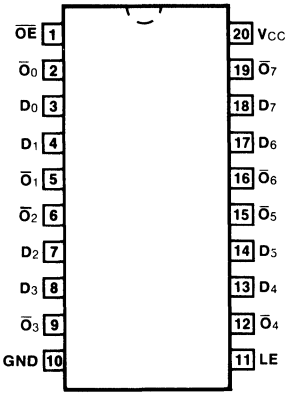
SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{S}$ to CP	16 16		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{S}$ to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW D to CP	8.0 8.0		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D to CP	10 10		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	20 46		ns	Fig. 3-8

54LS/74LS533

OCTAL TRANSPARENT LATCH

(With 3-State Outputs)

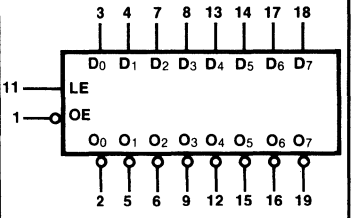
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '533 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state. The '533 is the same as the '373, except that the outputs are inverted. For detailed specifications please see the '373 data sheet, but note that the propagation delays from data to output are 5.0 ns longer for the 'LS533 than for the 'LS373.

- **EIGHT LATCHES IN A SINGLE PACKAGE**
- **3-STATE OUTPUTS FOR BUS INTERFACING**

LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V, ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS533PC		9Z
Ceramic DIP (D)	A	74LS533DC	54LS533DM	4E
Flatpak (F)	A	74LS533FC	54LS533FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

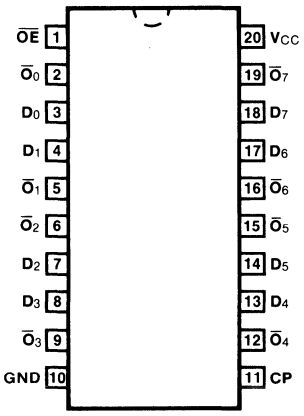
PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
D0 — D7	Data Inputs	0.5/0.25
LE	Latch Enable Input (Active HIGH)	0.5/0.25
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.25
$\overline{O}_0$ — $\overline{O}_7$	Complementary 3-State Outputs	65/15 (25)/(7.5)

54LS/74LS534

OCTAL D-TYPE FLIP-FLOP

(With 3-State Outputs)

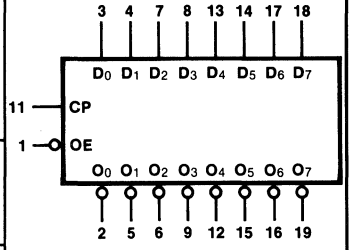
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '534 is a high speed, low power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) is common to all flip-flops. The '534 is manufactured using advanced low power Schottky technology and is compatible with all Fairchild TTL families. The '534 is the same as the '374 except that the outputs are inverted. For detailed specifications please see the '374 data sheet.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**

LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS534PC		9Z
Ceramic DIP (D)	A	74LS534DC	54LS534DM	4E
Flatpak (F)	A	74LS534FC	54LS534FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
D0 — D7	Data Inputs	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.25
$\overline{O}_0$ — $\overline{O}_7$	Complementary 3-State Outputs	65/15 (25)/(7.5)

54LS/74LS540
54LS/74LS541

OCTAL BUFFER/LINE DRIVER

(With 3-State Outputs)

DESCRIPTION — The 'LS540 and 'LS541 are similar in function to the 'LS240 and 'LS241, respectively, except that the inputs and outputs are on opposite sides of the package (see Connection Diagrams). This pinout arrangement makes these devices expecially useful as output ports for microprocessors, allowing ease of layout and greater PC board density.

- **HYSTERESIS AT INPUTS TO IMPROVE NOISE MARGIN**
- **PNP INPUTS REDUCE LOADING**
- **3-STATE OUTPUTS DRIVE BUS LINES**
- **INPUTS AND OUTPUTS OPPOSITE SIDE OF PACKAGE, ALLOWING EASIER INTERFACE TO MICROPROCESSORS**
- **FULLY TTL AND CMOS COMPATIBLE**

ORDERING CODE: See Section 9

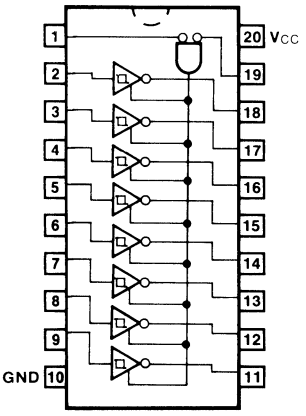
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS540PC		9Z
	B	74LS541PC		
Ceramic DIP (D)	A	74LS540DC	54LS540DM	4E
	B	74LS541DC	54LS541DM	
Flatpak (F)	A	74LS540FC	54LS540FM	4F
	B	74LS541FC	54LS541FM	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

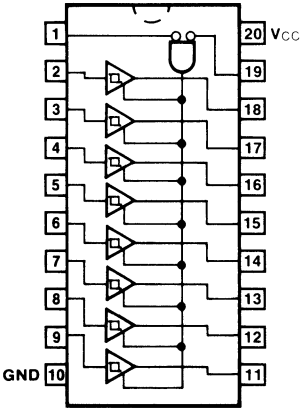
PINS	54/74LS (U.L.) HIGH/LOW
Inputs	0.5/0.125
Outputs	75/15 (7.5)

CONNECTION DIAGRAMS

PINOUT A



PINOUT B



4

TRUTH TABLE

INPUTS			OUTPUTS	
E_1	E_2	D	LS540	LS541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER		54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	'LS540		50	mA	V_{CC} = Max, V_{IN} = 0 V
		'LS541		54		V_E = 4.5 V
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('LS540)			14 18	ns	Figs. 3-1, 3-4, C_L = 50 pF
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('LS541)			18 18	ns	Figs. 3-1, 3-5, C_L = 50 pF
t_{PZH} t_{PZL}	Output Enable Time			23 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 50 pF
t_{PLZ} t_{PHZ}	Output Disable Time			25 18	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 5 pF

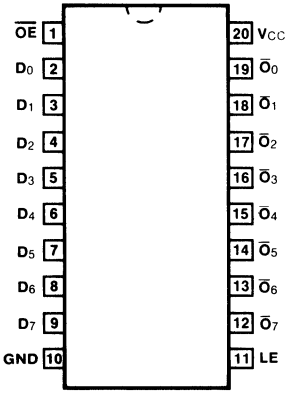
*DC limits apply over operating temperature range; AC limits apply at T_A = +25° C and V_{CC} = +5.0 V.

54LS/74LS563

OCTAL D-TYPE LATCH

(With 3-State Outputs)

CONNECTION DIAGRAM
PINOUT A

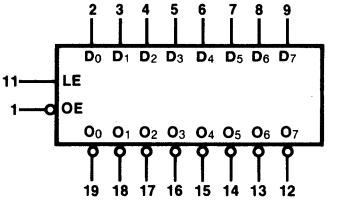


DESCRIPTION — The '563 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

This device is functionally indentical to the 'LS573, but has inverted outputs. For truth tables, discussion of operations and ac and dc specifications, please refer to the 'LS373 data sheet, but note that the data to output delays are 5.0 ns longer for the 'LS563 than for the 'LS373.

- **INPUTS AND OUTPUTS ON OPPOSITE SIDES OF PACKAGE ALLOWING EASY INTERFACE WITH MICROPROCESSORS**
- **USEFUL AS INPUT OR OUTPUT PORT FOR MICROPROCESSORS**
- **FUNCTIONALLY IDENTICAL TO 'LS573**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS563PC		9Z
Ceramic DIP (D)	A	74LS563DC	54LS563DM	4E
Flatpak (F)	A	74LS563FC	54LS563FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

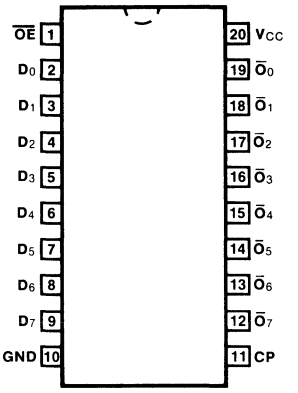
PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$D_0 - D_7$	Data Inputs	0.5/0.25
LE	Latch Enable Input (Active HIGH)	0.5/0.25
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.25
$\overline{O}_0 - \overline{O}_7$	3-State Latch Outputs	65/15 (25)/(7.5)

54LS/74LS564

OCTAL D-TYPE FLIP-FLOP

(With 3-State Outputs)

CONNECTION DIAGRAM
PINOUT A

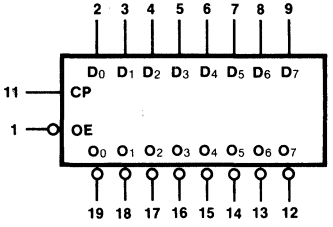


DESCRIPTION — The '564 is a high speed low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

This device is functionally identical to the 'LS574, but has inverted outputs. For complete discussions of operations, truth tables, ac and dc electrical specifications, refer to the 'LS374 data sheet.

- **INPUTS AND OUTPUTS ON OPPOSITE SIDES OF PACKAGE ALLOWING EASY INTERFACE WITH MICROPROCESSORS**
- **USEFUL AS INPUT OR OUTPUT PORT FOR MICROPROCESSORS**
- **FUNCTIONALLY IDENTICAL TO 'LS574**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS564PC		9Z
Ceramic DIP (D)	A	74LS564DC	54LS564DM	4E
Flatpak (F)	A	74LS564FC	54LS564FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

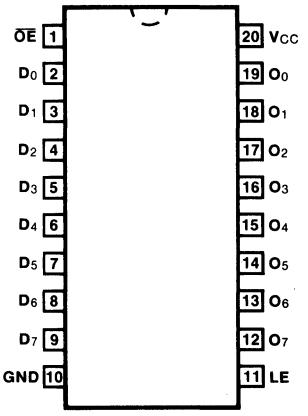
PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
D_0 — D_7	Data Inputs	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.25
$\overline{O}_0$ — $\overline{O}_7$	3-State Outputs	65/15 (25)/(7.5)

54LS/74LS573

OCTAL D-TYPE LATCH

(With 3-State Outputs)

CONNECTION DIAGRAM
PINOUT A

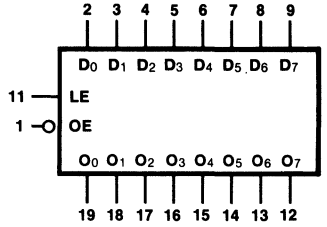


DESCRIPTION — The '573 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

This device is functionally identical to the 'LS373, but has different pinouts. For truth tables, discussion of operations and ac and dc specifications, please refer to the 'LS373 data sheet.

- **INPUTS AND OUTPUTS ON OPPOSITE SIDES OF PACKAGE ALLOWING EASY INTERFACE WITH MICROPROCESSORS**
- **USEFUL AS INPUT OR OUTPUT PORT FOR MICROPROCESSORS**
- **FUNCTIONALLY IDENTICAL TO 'LS373**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



VCC = Pin 20
Gnd = Pin 10

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS573PC		9Z
Ceramic DIP (D)	A	74LS573DC	54LS573DM	4E
Flatpak (F)	A	74LS573FC	54LS573FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

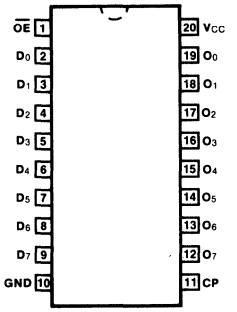
PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
D0 — D7	Data Inputs	0.5/0.25
LE	Latch Enable Input (Active HIGH)	0.5/0.25
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.25
O0 — O7	3-State Latch Outputs	65/15 (25)/(7.5)

54LS/74LS574

OCTAL D-TYPE FLIP-FLOP

(With 3-State Outputs)

CONNECTION DIAGRAM
PINOUT A

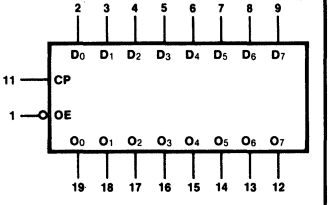


DESCRIPTION — The '574 is a high speed low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

This device is functionally identical to the 'LS374 except for the pinouts. For complete discussions of operations, truth tables, ac and dc electrical specifications, refer to the 'LS374 data sheet.

- **INPUTS AND OUTPUTS ON OPPOSITE SIDES OF PACKAGE ALLOWING EASY INTERFACE WITH MICROPROCESSORS**
- **USEFUL AS INPUT OR OUTPUT PORT FOR MICROPROCESSORS**
- **FUNCTIONALLY IDENTICAL TO 'LS374**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS574PC		9Z
Ceramic DIP (D)	A	74LS574DC	54LS574DM	4E
Flatpak (F)	A	74LS574FC	54LS574FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

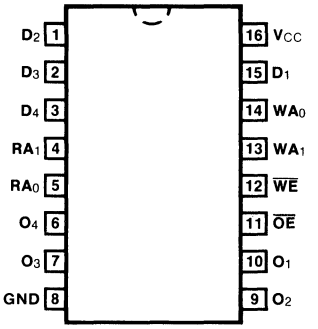
PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$D_0 - D_7$	Data Inputs	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.25
$O_0 - O_7$	3-State Outputs	65/15 (25)/(7.5)

54LS/74LS670

4 X 4 REGISTER FILE

(With 3-State Outputs)

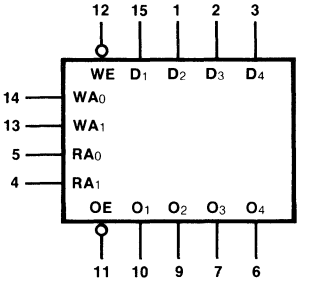
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '670 contains 16 high speed, low power, transparent D-type latches arranged as four words of four bits each, to function as a 4 X 4 register file. Separate read and write inputs, both address and enable, allow simultaneous read and write operation. The 3-state outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length. The '170 provides a similar function to this device but it features open-collector outputs.

- **SIMULTANEOUS READ/WRITE OPERATION**
- **EXPANDABLE TO 512 WORDS BY n-BITS**
- **TYPICAL ACCESS TIME OF 20 ns**
- **3-STATE OUTPUTS FOR EXPANSION**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

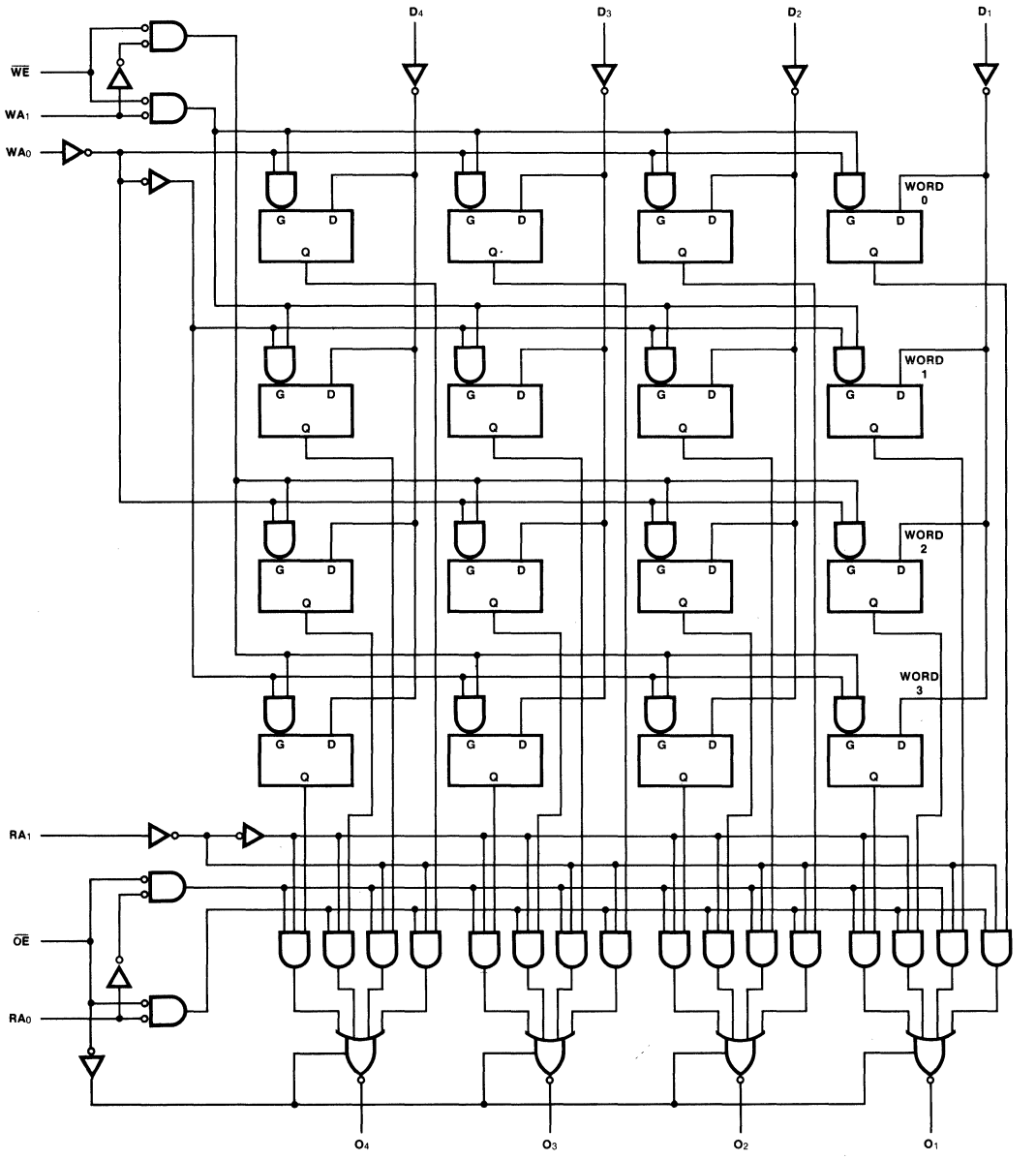
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0° C to +70° C	MILITARY GRADE VCC = +5.0 V ±10% TA = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	74LS670PC		9B
Ceramic DIP (D)	A	74LS670DC	54LS670DM	6B
Flatpak (F)	A	74LS670FC	54LS670FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$D_1 - D_4$	Data Inputs	0.5/0.25
WA_0, WA_1	Write Address Inputs	0.5/0.25
$\overline{WE}$	Write Enable Input (Active LOW)	1.0/0.5
RA_0, RA_1	Read Address Inputs	0.5/0.25
$\overline{OE}$	3-State Output Enable Input (Active LOW)	1.5/0.75
$O_1 - O_4$	Data Outputs	65/5.0 (25)/(2.5)

LOGIC DIAGRAM



WRITE FUNCTION TABLE

WRITE INPUTS			D INPUTS TO
$\overline{WE}$	WA_1	WA_0	
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (hold)

READ FUNCTION TABLE

READ INPUTS			OUTPUTS FROM
$\overline{OE}$	RA_1	RA_0	
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (HIGH Z)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

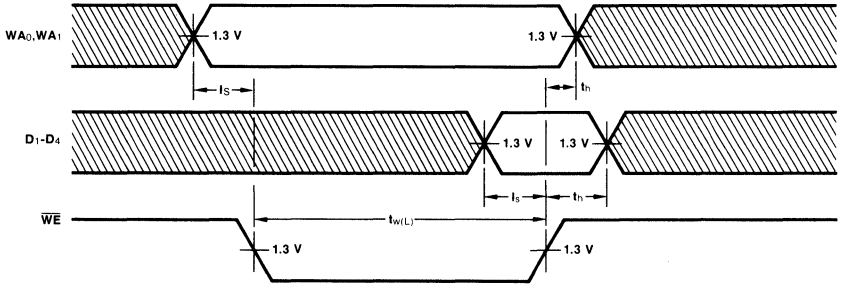


Fig. a

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

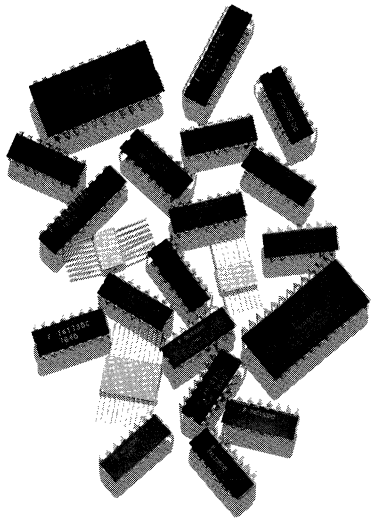
SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{OS}	Output Short Circuit Current	-20	-100	mA	V_{CC} = Max
I_{CC}	Power Supply Current		50	mA	V_{CC} = Max; WA_n, RA_n = Gnd; D_n, $\overline{WE}$ = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay RA_0 or RA_1 to O_n		35 35	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{WE}$ to O_n		35 35	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n		35 35	ns	Figs. 3-1, 3-5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n		30 35	ns	Figs. 3-3, 3-11, 3,12 R_L = 2 kΩ
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n		40 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ C_L = 5 pF

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s	Setup Time HIGH or LOW D_n to Rising $\overline{WE}$	10		ns	Fig. a
t_h	Hold Time HIGH or LOW D_n to Rising $\overline{WE}$	10		ns	
t_s	Setup Time HIGH or LOW WA_n to Falling $\overline{WE}$	10		ns	
t_h	Hold Time HIGH or LOW WA_n to Rising $\overline{WE}$	5.0		ns	
t_w (L)	$\overline{WE}$ Pulse Width LOW	25		ns	Fig. a



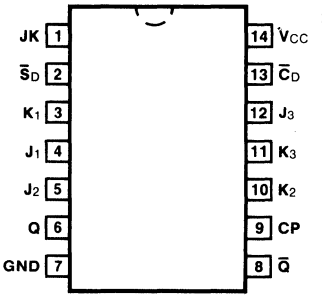
9000 • 9001
9020 • 9022

JK FLIP-FLOPS ('00, '01)
DUAL JK FLIP-FLOPS ('20, '22)

ORDERING CODE: See Section 9

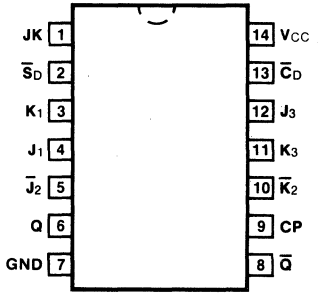
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +75°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Ceramic DIP (D)	A	9000DC	9000DM	6A
	B	9001DC	9001DM	
	C	9020DC	9020DM	6B
	D	9022DC	9022DM	
Flatpak (F)	A	9000FC	9000FM	3I
	B	9001FC	9001FM	
	C	9020FC	9020FM	4L
	D	9022FC	9022FM	

CONNECTION DIAGRAMS
PINOUT A



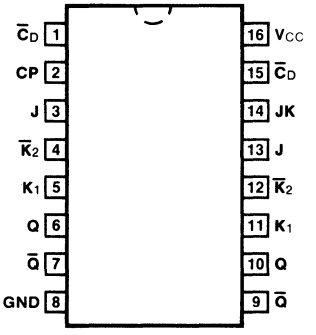
$J = A \bullet B \bullet C \bullet D$
$K = A \bullet B \bullet C \bullet D$

PINOUT B

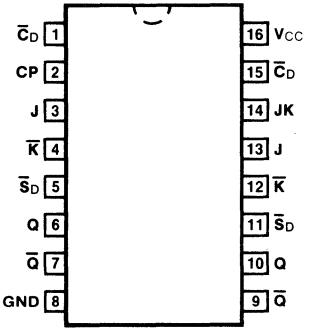


$J = A \bullet \overline{B} \bullet C \bullet D$
$K = A \bullet B \bullet \overline{C} \bullet D$

PINOUT C



PINOUT D



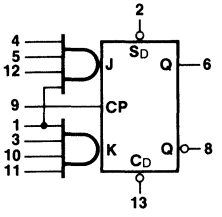
5

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	9000 (U.L.) HIGH/LOW	9001 (U.L.) HIGH/LOW	9020 (U.L.) HIGH/LOW	9022 (U.L.) HIGH/LOW
JK	JK Input	3.0/2.0	3.0/2.0	6.0/4.0	6.0/4.0
J_n, K_n, $\overline{J}_n$, $\overline{K}_n$	Data Inputs	1.5/1.0	1.5/1.0	1.5/1.0	1.5/1.0
CP	Clock Pulse Input	1.5/1.0	1.5/1.0	3.0/2.0	3.0/2.0
$\overline{C}_D$	Direct Clear Input	4.0/2.7	4.0/2.7	4.0/2.7	4.0/2.7
$\overline{S}_D$	Direct Set Input	4.0/2.7	4.0/2.7		4.0/2.7
Q, $\overline{Q}$	Outputs	30/8.8 (7.8)	30/8.8 (7.8)	30/8.8 (7.8)	30/8.8 (7.8)

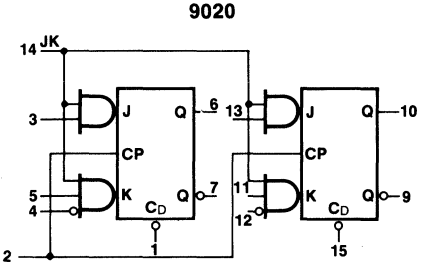
LOGIC SYMBOLS

9000



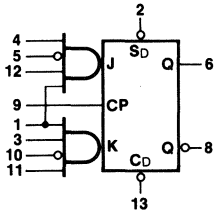
V_{CC} = Pin 14
GND = Pin 7

9020



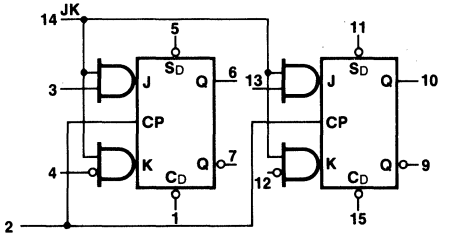
V_{CC} = Pin 16
GND = Pin 8

9001



V_{CC} = Pin 14
GND = Pin 7

9022



V_{CC} = Pin 16
GND = Pin 8

ASYNCHRONOUS OPERATION

INPUTS		OUTPUTS	
$\overline{S}_D$	$\overline{C}_D$	Q	$\overline{Q}$
L	L	H	H
L	H	H	L
H	L	L	H
H	H	SYNCHRONOUS INPUTS CONTROL	

H = HIGH Voltage Level
L = LOW Voltage Level

SYNCHRONOUS OPERATION

BEFORE CLOCK				AFTER CLOCK	
OUTPUTS		INPUTS		OUTPUTS	
Q	$\overline{Q}$	J	K	Q	$\overline{Q}$
L	H	L*	X	L	H
L	H	H*	X	H	L
H	L	X	L*	H	L
H	L	X	H*	L	H

L* = Input does not go HIGH at any time while the clock is LOW.
H* = Input is HIGH at some time while the clock is LOW.
X = Immaterial

FUNCTIONAL DESCRIPTION — The TTL 9000 series has four flip-flops to satisfy the storage requirements of a logic system. All are master/slave JK designs and have the same high speed and high noise immunity as the rest of the 9000 series. As with the gates, all inputs have diode clamps to reduce ringing caused by long lines and impedance mismatches.

The JK type flip-flop was chosen for all flip-flop elements in this family because of its inherent logic power. The input function required to produce a given sequence of states for a JK flip-flop will, in general, contain more "don't care" conditions than the corresponding function for an RS flip-flop. These additional "don't care" conditions will, in most cases, reduce the amount of gating elements required to implement the input function.

The master/slave design offers the advantage of a dc threshold on the clock input initiating the transition of the outputs, so that careful control of clock pulse rise and fall times is not required.

Data is accepted by the master while the clock is in the LOW state. Refer to the truth tables for definition of HIGH and LOW data. Transfer from the master to the slave occurs on the LOW-to-HIGH transition of the clock. When the clock is HIGH, the J and K inputs are inhibited.

A joint (JK) input is provided for all flip-flops in this family. The common input removes the necessity of gating the clock signal with an external gate in many applications. This not only reduces package count, but also reduces the possibility of clock skew problems, since with internal gating provided, all flip-flops may be driven from a common clock line. Several TTL drivers may be used in parallel to drive this common clock line if the load exceeds the fan-out capability of the 9009 buffer.

The asynchronous inputs provide ability to control the state of the flip-flop independent of static conditions of the clock and synchronous inputs. Both asynchronous set and clear are provided on all flip-flops except the 9020, which because of a logic trade-off has only clear inputs. The set or clear pin being LOW absolutely guarantees that one output will be HIGH, but if opposing data is present at the synchronous inputs and the flip-flop is clocked, the LOW output may momentarily spike HIGH synchronous with a positive transition of the clock. If the LOW output of the flip-flop is connected to other flip-flop inputs clocked from the same line, the spike will be masked by the clock. If the clock is suspended during the time when the asynchronous inputs are activated, no spike will occur. When the spikes can cause problems, a simple solution is to common the joint JK inputs with the synchronous set or reset signal.

Synchronous Operation — The truth table defines the next state of the flip-flop after a LOW-to-HIGH transition of the clock pulse. The next state is a function of the present state and the J and K inputs as shown in the table. The J and K inputs in the table refer to the basic flip-flop J and K inputs as indicated on the logic symbols. These internal inputs are for every flip-flop the result of a logic operation on the external J and K inputs. This operation is represented symbolically by AND gates in the logic symbol for each flip-flop. Logic symbols are in accordance with MIL Standard 806B.

The L* symbol in the J and K input column is defined as meaning that **input does not go HIGH at any time while the clock is LOW.**

The H* symbol in the J or K input column is defined as meaning that the **input is HIGH at some time while the clock is LOW.**

The X symbol indicates that the condition of that input has no effect on the next state of the flip-flop.

The H and L symbols refer to steady state HIGH and LOW voltage levels, respectively.

Unused Inputs — The 9001, 9020 and 9022 all have active level LOW synchronous inputs. When not in use they must be grounded. All other unused inputs, including asynchronous, should be tied HIGH for maximum operating speed.

DC AND AC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE: V_{CC} = +5.0 V ±5%

SYMBOL	PARAMETER	0°C		25°C		75°C		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
V_{IH}	Input HIGH Voltage	1.9		1.8		1.6		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage		0.85		0.85		0.85	V	Guaranteed Input LOW Threshold
V_{OL}	Output LOW Voltage		0.45		0.45		0.45	V	V_{CC} = 4.75 V, I_{OL} = 14.1 mA V_{CC} = 5.25 V, I_{OL} = 16 mA
I_{IL}	Input LOW Current All J, K Inputs CP Inputs 9000, 9001 JK Inputs 9000, 9001 CP Inputs 9020, 9022 JK inputs 9020, 9022 $\overline{S}_D$, $\overline{C}_D$ (all Flip-flops)		-1.60 -3.20 -6.40 -4.32		-1.60 -3.20 -6.40 -4.32		-1.60 -3.20 -6.40 -4.32	mA	V_{CC} = 5.25 V V_{IN} = 0.45 V 5.25 V on Other Inputs
	Input LOW Current All J, K Inputs CP Inputs 9000, 9001 JK Inputs 9000, 9001 CP Inputs 9020, 9022 JK Inputs 9020, 9022 $\overline{S}_D$, $\overline{C}_D$ (all Flip-flops)		-1.41 -2.82 -5.64 -3.78		-1.41 -2.82 -5.64 -3.78		-1.41 -2.82 -5.64 -3.78	mA	V_{CC} = 4.75 V V_{IN} = 0.45 V 5.25 V on Other Inputs
I_{CC}	Power Supply Current 9000 9001 9020, 9022 each Flip-flop		 28 33 30		 28 33 30		 28 33 30	mA	 $\overline{S}_D$ at Gnd $\overline{S}_D$ at Gnd $\overline{C}_{D1}$, $\overline{C}_{D2}$ at Gnd

DC AND AC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE: V_{CC} = +5.0 V ±10%

SYMBOL	PARAMETER	-55°C		25°C		125°C		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
V_{IH}	Input HIGH Voltage	2.0		1.7		1.4		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage		0.8		0.9		0.8	V	Guaranteed Input LOW Threshold
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 12.4 mA V_{CC} = 5.5 V, I_{OL} = 16 mA

DC AND AC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE: (Cont'd)

SYMBOL	PARAMETER	-55°C Min	-55°C Max	25°C Min	25°C Max	125°C Min	125°C Max	UNITS	CONDITIONS
I_{IL}	Input LOW Current All J, K Inputs CP Inputs 9000, 9001 JK Inputs 9000, 9001 CP Inputs 9020, 9022 JK Inputs 9020, 9022 $\overline{S}_D$, $\overline{C}_D$ (all Flip-flops)		-1.60 -3.20 -6.40 -4.32		-1.60 -3.20 -6.40 -4.32		-1.60 -3.20 -6.40 -4.32	mA	V_{CC} = 5.5 V V_{IN} = 4.5 V 5.5 V on Other Inputs
	Input LOW Current All J, K Inputs CP Inputs 9000, 9001 JK Inputs 9000, 9001 CP Inputs 9020, 9022 JK Inputs 9020, 9022 $\overline{S}_D$, $\overline{C}_D$ (all Flip-flops)		-1.24 -2.48 -4.96 -3.35		-1.24 -2.48 -4.96 -3.75		-1.24 -2.48 -4.96 -3.35	mA	V_{CC} = 4.5 V V_{IN} = 0.4 V 5.5 V on Other Inputs
I_{CC}	Power Supply Current 9000 9001 9020, 9022 each Flip-flop		 24 28 27		 24 28 27		 24 28 27	mA	 $\overline{S}_D$ at Gnd $\overline{S}_D$ at Gnd $\overline{C}_{D1}$, $\overline{C}_{D2}$, at Gnd

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, C_L = C_1 = 15 pF of all flip-flops unless otherwise noted)

SYMBOL	PARAMETER			LIMITS Min	LIMITS Max	UNITS	CONDITIONS
t_{PLH}	Clock to Output $\overline{S}_D$ or $\overline{C}_D$ to Output				20 20	ns	Figs. a, b, c
t_{PHL}	Clock to Output $\overline{S}_D$ or $\overline{C}_D$ to Output				30 35	ns	Figs. a, b, c
t_{setup}	J, K or JK		9000XM	30		ns	Figs. a, c
			9000XC	35			
		9001XM, 9020XM, 9022XM		10		ns	Figs. a, b, c
		9001XC, 9020XC, 9022XC		15			
	$\overline{J}$ or $\overline{K}$ Data Entry			17			
$t_{release}$	J, K or JK		9000 only		10	ns	Figs. a, c
			9001, 9020, 9022		1.0	ns	Figs. a, b, c
	$\overline{J}$ or $\overline{K}$ Data Entry				4.0		
Pulse Widths	Clock	9000 only	Positive		20*	ns	Figs. a, c
			Negative		25*		
		9001, 9020, 9022	Positive		8.0*	ns	Figs. a, b, c
			Negative		10*		
	$\overline{S}_D$ or $\overline{C}_D$		Negative		25*		
	Toggle Frequency		9000 only		20*	MHz	Figs. a, c
			9001, 9020, 9022		50*	MHz	Figs. a, b, c

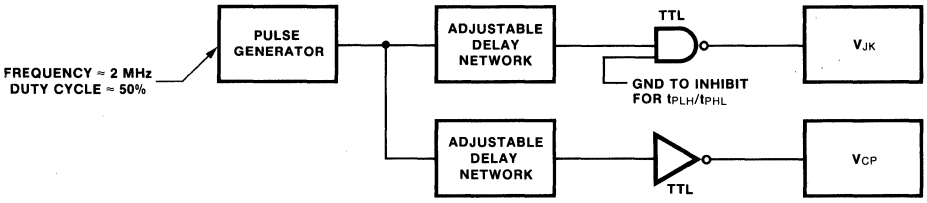
*Typical Value

SWITCHING TEST NOTES

t_{PLH} and t_{PHL}

1. V_{JK} should be kept at the HIGH level when performing t_{PLH}/t_{PHL} test.
2. Drive the clock pulse input with a suitable pulse source. t_{PLH} and t_{PHL} delays are as defined in the waveforms.

RECOMMENDED INPUT PULSE SOURCES



DTL9932 gates with adjustable capacitors connected from extender inputs to ground make suitable delay elements.

t_{setup}

1. t_{setup} is defined as the minimum time required for a HIGH to be present at a synchronous logic input at any time during the LOW state of the clock in order for the flip-flop to respond to the data.
2. The test for t_{setup} is performed by adjusting the timing relationship between the V_{CP} and V_{JK} inputs to the t_{setup} minimum value. A device that passes the test will have the output waveform shown. The output of a device that does not pass the t_{setup} test will remain at a static logic level (no switching will occur).

$t_{release}$

1. $t_{release}$ is defined as the maximum time allowed for a HIGH to be present at a synchronous logic input at any time during the LOW state of the clock and not be recognized.
2. The test for $t_{release}$ is performed by adjusting the timing relationship between V_{CP} and V_{JK} to the $t_{release}$ maximum value. The outputs of devices that pass will remain at static logic levels. In order to check both J and K sides of the flip-flop it is necessary to perform the test with the flip-flop in each of its two possible states, i.e., set and clear. This can be accomplished by making use of the appropriate direct inputs to establish the state before a test. The outputs of devices that do not pass the $t_{release}$ test will exhibit pulses instead of static levels.

SWITCHING TEST CIRCUITS

9000/9001

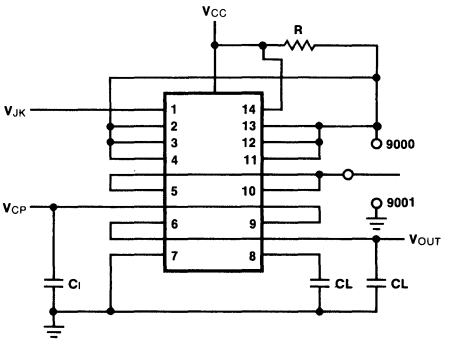


Fig. a

9020/9022

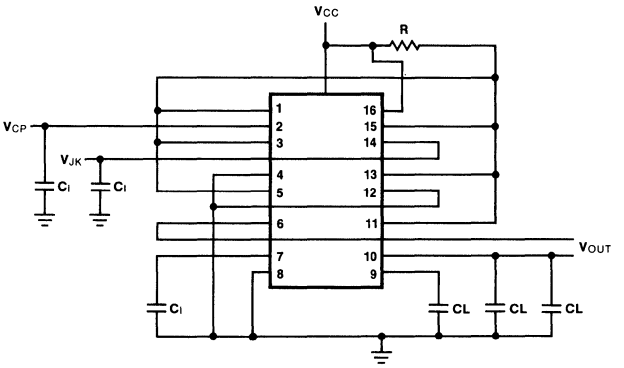


Fig. b

V_{CC} = Pin 5.0 V
R = 2.0 kΩ
$C_I = C_L$ = 15 pF including probe and jig capacitance

WAVEFORM

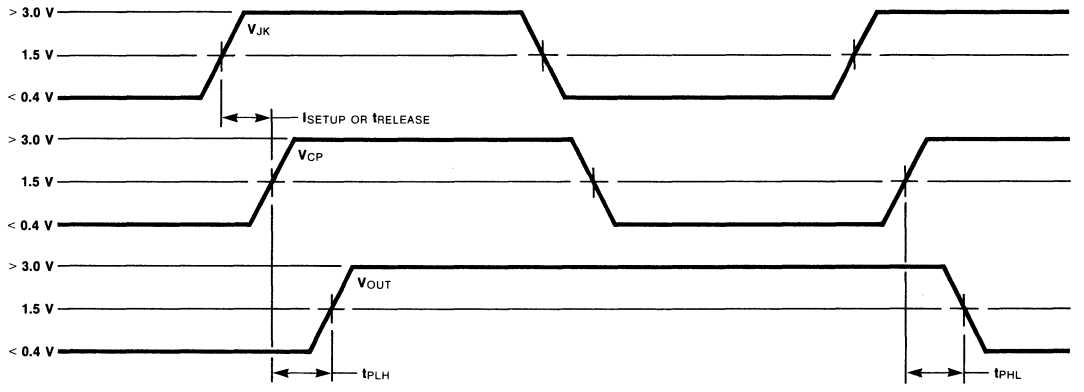


Fig. c

9002 • 9003 • 9004
9007 • 9012
9016 • 9017

NAND GATES/HEX INVERTERS

DESCRIPTION — The 9002, 9003, 9004, 9007, and 9012 are active LOW level output AND gates commonly know as NAND gates. The 9016 and 9017 are hex inverters with input and output characteristics identical to a NAND gate.

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +75°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Ceramic DIP (D)	A	9002DC, 9012DC	9002DM, 9012DM	6A
	B	9003DC	9003DM	
	C	9004DC	9004DM	
	D	9007DC	9007DM	
	E	9016DC, 9017DC	9016DM, 9017DM	
Flatpak (F)	A	9002FC, 9012FC	9002FM, 9012FM	3I
	B	9003FC	9003FM	
	C	9004FC	9004FM	
	D	9007FC	9007FM	
	E	9016FC, 9017FC	9016FM, 9017FM	

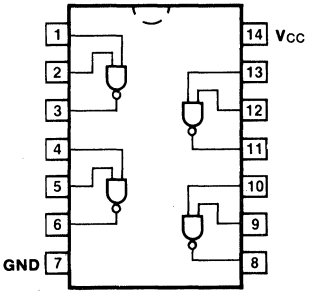
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	9XXX (U.L.) HIGH/LOW
Inputs	1.5/1.0
Outputs	30*/8.8

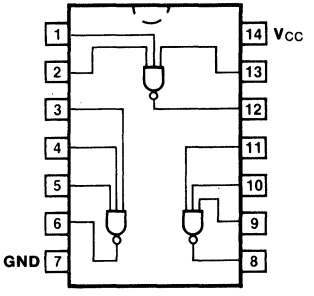
*9012 and 9017 have open-collector outputs

CONNECTION DIAGRAMS

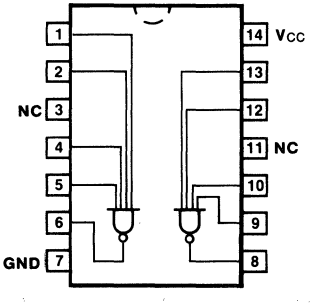
PINOUT A



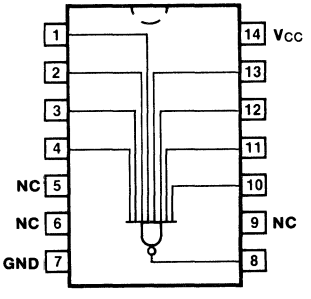
PINOUT B



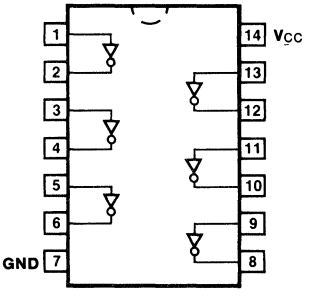
PINOUT C



PINOUT D



PINOUT E



DC AND AC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE: V_{CC} = +5.0 V ±5%

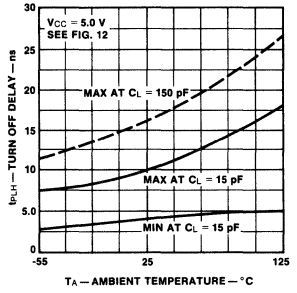
SYMBOL	PARAMETER		0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage		1.9		1.8		1.6		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage			0.85		0.85		0.85	V	Guaranteed Input LOW Threshold
V_{OH}	Output HIGH Voltage (except 9012, 9017)		2.4		2.4		2.4		V	V_{CC} = 4.75 V, I_{OH} = -1.2 mA, Inputs at V_{IL}
V_{OL}	Output LOW Voltage			0.45		0.45		0.45	V	V_{CC} = 5.25 V, I_{OL} = 16 mA, V_{IN} = 5.25 V
				0.45		0.45		0.45		V_{CC} = 4.75 V, I_{OL} = 14.1 mA, Inputs at V_{IH}
I_{IH}	Input HIGH Current					60		60	μA	V_{CC} = 5.25 V, V_{IN} = 4.5 V Gnd on Other Inputs
I_{IL}	Input LOW Current			-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V V_{IN} = 0.45 V, 5.25 V on Other Inputs
				-1.41		-1.41		-1.41		V_{CC} = 4.75 V V_{IN} = 0.45 V, 5.25 V on Other Inputs
I_{OH}	Output HIGH Current 9012, 9017					250		250	μA	V_{CC} = 4.75 V, V_{IN} = V_{IL}, V_{OUT} = 5.5 V
I_{CC}	Power Supply Current, each gate	ON		6.1		6.1		6.1	mA	V_{IN} = Open
		OFF		1.7		1.7		1.7		V_{IN} = Gnd
t_{PLH}	Propagation Delay Input to Output				3.0	13			ns	C_L = 15 pF, Fig. 3-4
		9012, 9017			3.0	45				R_L = 4.0 kΩ C_L = 15 pF, Fig. 3-4
t_{PHL}	Propagation Delay Input to Output				3.0	15			ns	C_L = 15 pF, Fig. 3-4
		9012, 9017			3.0	15				R_L = 400 Ω C_L = 15 pF, Fig. 3-4

5

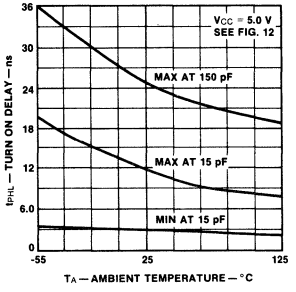
DC AND AC CHARACTERISITICS OVER MILITARY TEMPERATURE RANGE: V_{CC} = +5.0 V ±10%

SYMBOL	PARAMETER		-55°C Min	-55°C Max	25°C Min	25°C Max	125°C Min	125°C Max	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage		2.0		1.7		1.4		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage			0.8		0.9		0.8	V	Guaranteed Input LOW Threshold
V_{OH}	Output HIGH Voltage (except 9012, 9017)		2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = -1.32 mA, Inputs at V_{IL}
V_{OL}	Output LOW Voltage			0.4		0.4		0.4	V	V_{CC} = 5.5 V, I_{OL} = 17.6 mA, V_{IN} = 5.5 V
				0.4		0.4		0.4		V_{CC} = 4.5 V, I_{OL} = 13.6 mA, Inputs at V_{IH}
I_{IH}	Input HIGH Current					60		60	μA	V_{CC} = 5.5 V, V_{IN} = 4.5 V Gnd on Other Inputs
I_{IL}	Input LOW Current			-1.6		-1.6		-1.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, 5.5 V on Other Inputs
				-1.24		-1.24		-1.24		V_{CC} = 4.5 V, V_{IN} = 0.4 V, 5.5 V on Other Inputs
I_{OH}	Output HIGH Current 9012, 9017					250		250	μA	V_{CC} = 4.5, V_{IN} = V_{IL}, V_{OUT} = 5.5 V
I_{CC}	Power Supply Current, each gate	ON		5.5		5.5		5.5	mA	V_{IN} = Open
		OFF		1.6		1.6		1.6		V_{IN} = Gnd
t_{PLH}	Propagation Delay Input to Output				3.0	10			ns	C_L = 15 pF, Fig. 3-4
		9012, 9017			3.0	45				R_L = 4.0 kΩ, C_L = 15 pF, Fig. 3-4
t_{PHL}	Propagation Delay Input to Output				3.0	12			ns	C_L = 15 pF, Fig. 3-4
		9012,9017			3.0	15				R_L = 400 Ω, C_L = 15 pF, Fig. 3-4

WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE



WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE



9005 • 9008
9006

EXTENDABLE AND-OR-INVERT GATES
EXTENDER (9006)

DESCRIPTION: — The 9005 and 9008 are AND-OR-INVERT gates which may be OR extended with the use of the 9006.

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +75°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Ceramic DIP (D)	A	9005DC	9005DM	6A
	B	9006DC	9006DM	
	C	9008DC	9008DM	
Flatpak (F)	A	9005FC	9005FM	3I
	B	9006FC	9006FM	
	C	9008FC	9008FM	

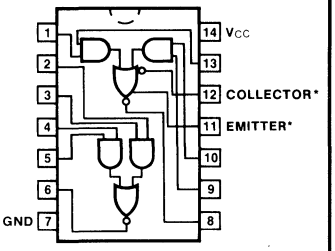
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	9005 (U.L.) HIGH/LOW	9006 (U.L.) HIGH/LOW	9008 (U.L.) HIGH/LOW
Non-extendable Gate Inputs	1.5/1.0		
Extendable Gate Inputs	2.25/1.5		
All Inputs		2.25/1.5	2.25/1.5
Outputs	30/8.8 (33)/(8.5)	*	30/8.8 (33)/(8.5)

*Outputs on 9006 have open-emitter and collector

CONNECTION DIAGRAMS

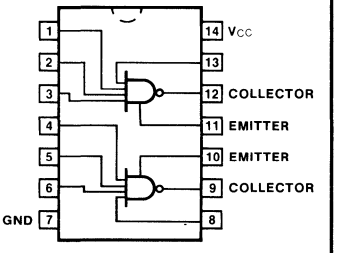
PINOUT A



*Four extenders (9006) may be tied to these terminals

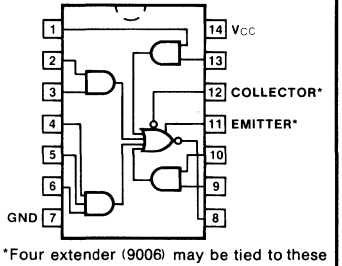
V_{CC} = Pin 14
GND = Pin 7

PINOUT B



V_{CC} = Pin 14
GND = Pin 7

PINOUT C



*Four extender (9006) may be tied to these terminals

V_{CC} = Pin 14
GND = Pin 7

5

DC AND AC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE: V_{CC} = +5.0 V ±5%

SYMBOL	PARAMETER	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	1.9		1.8		1.6		V	Guaranteed Input HIGH Threshold Voltage
V_{IL}	Input LOW Voltage		0.85		0.85		0.85	V	Guaranteed Input LOW Threshold Voltage
V_{OL}	Output LOW Voltage		0.45		0.45		0.45	V	V_{CC} = 5.25 V, I_{OL} = 16 mA,
			0.45		0.45		0.45	V	V_{CC} = 4.75 V, I_{OL} = 14.1 mA
I_{IL}	Input LOW Current 9005 Non-Extendable Gate	-1.6	-1.41	-1.6	-1.41	-1.6	-1.41	mA	V_{CC} = Max / Min; V_{IN} = .45 V, 5.25 V on Other Inputs
	Input LOW Current Extendable Gates and Extender	-2.4	-2.12	-2.4	-2.12	-2.4	-2.12	mA	V_{CC} = Max / Min; V_{IN} = .45 V, 5.25 V on Other Inputs
I_{CC}	Power Supply Current, ON 9005 Non-Extendable Gate		7.7		7.7		7.7	mA	All Inputs Open
	Power Supply Current, ON 9005 Extendable Gate		13.6		13.6		13.6	mA	All Inputs Open
	Power Supply Current, ON 9008		17.7		17.7		17.7	mA	All Inputs Open
	Power Supply Current, OFF 9005 Non-Extendable Gate		3.4		3.4		3.4	mA	All Inputs Except Extender Inputs Gnd
	Power Supply Current, OFF 9005 Extendable Gate		5.1		5.1		5.1	mA	All Inputs Except Extender Inputs Gnd
	Power Supply Current, OFF 9008		10.2		10.2		10.2	mA	All Inputs Except Extender Inputs Gnd
ΔI_{CC}	Extra Current Drain when one 9006 Extender is attached to a 9005 Gate ON		2.05		2.05		2.05	mA	All Inputs HIGH
	Extra Current Drain when one 9006 Extender is attached to a 9005 gate OFF		2.54		2.54		2.54	mA	All Inputs Gnd

DC AND AC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE: V_{CC} = +5.0 V ±10%

SYMBOL	PARAMETER	-55°C Min	-55°C Max	25°C Min	25°C Max	125°C Min	125°C Max	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	2.0		1.7		1.4		V	Guaranteed Input HIGH Threshold Voltage
V_{IL}	Input LOW Voltage		0.8		0.9		0.8	V	Guaranteed Input LOW Threshold Voltage
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	V_{CC} = 5.5 V, I_{OL} = 17.6 mA
			0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 13.6 mA
I_{IL}	Input LOW Current 9005 Non-extendable Gate	-1.6	-1.24	-1.6	-1.24	-1.6	-1.24	mA	V_{CC} = Max / Min; V_{IN} = .4 V, 5.5 V on Other Inputs
	Input LOW Current Extendable Gate and Extender	-2.4	-1.86	-2.4	-1.86	-2.4	-1.86	mA	V_{CC} = Max / Min; V_{IN} = .4 V, 5.5 V on Other Inputs

NOTE:
Output characteristics above apply to a 9005 (both gates) or a 9008.
Input characteristics above apply to a 9005 (both gates) or a 9008 using either the internal gates or an external 9006 extender.

DC AND AC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE: V_{CC} = +5.0 V ±10% (Cont'd)

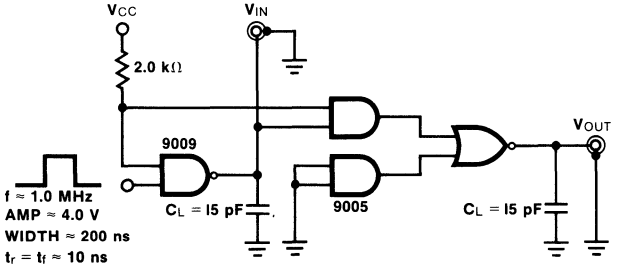
SYMBOL	PARAMETER	-55°C Min	-55°C Max	25°C Min	25°C Max	125°C Min	125°C Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current, ON								
	9005 Non-extendable Gate		6.5		6.5		6.5		
	9005 Extendable Gate		11.3		11.3		11.3	mA	All Inputs Open
	9008		12.5		12.5		12.5		
	Power Supply Current, OFF								
	9005 Non-extendable Gate		3.1		3.1		3.1		
	9005 Extendable Gate		4.7		4.7		4.7	mA	All Inputs Except Extender Inputs Gnd
	9008		9.4		9.4		9.4		
ΔI_{CC}	Extra Current Drain from one 9006 Extender Gate ON		1.61		1.61		1.61	mA	All Inputs HIGH
	Extra Current Drain from one 9006 Extender Gate OFF		2.35		2.35		2.35	mA	All Inputs Gnd 9006 Attached to a 9005

NOTE:
Output characteristics apply to a 9005 (both gates) or a 9008.
Input characteristics apply to a 9005 (both gates) or a 9008 using either the internal gates or an external 9006 extender.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	LIMITS Min	LIMITS Max	UNITS	TEST CONDITIONS
t_{PLH}	3.0	12	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	3.0	14		9005 Non-extendable Gate Only, See Figure a
t_{PLH}	3.0	15	ns	V_{CC} = 5.0 V, C_L = 15 pF, C_N = 5.0 pF
t_{PHL}	3.0	12		9005 Extendable Gate and 9008, See Figure b
Δt_{PLH}	-2.0	4.0	ns	9006 Only
Δt_{PHL}	-2.0	4.0		The 9006 is tested by measuring its propagation time through the 9005. The delay readings shall not exceed the 9005 readings by the specified amount. See Figure c

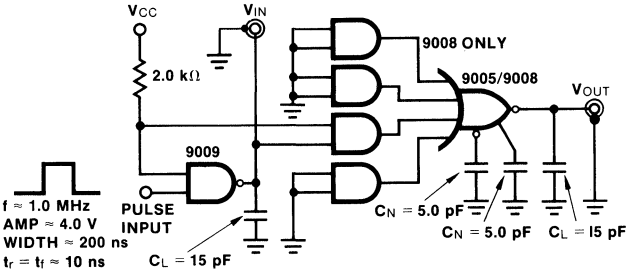
SWITCHING CHARACTERISTICS TEST CIRCUITS



Note: Capacitance includes probe and jig capacitance

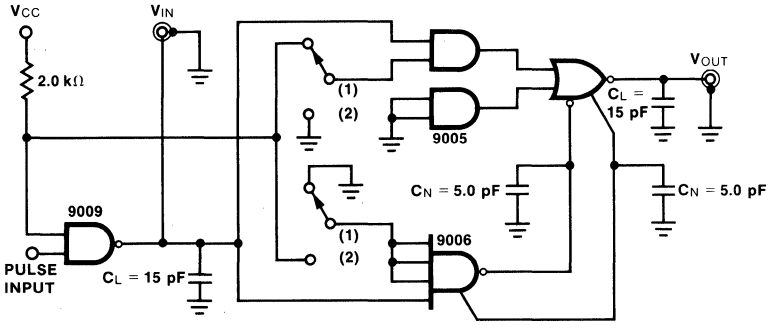
Fig. a 9005 Non-Extendable Gate

SWITCHING CHARACTERISTICS (Cont'd)
TEST CIRCUITS



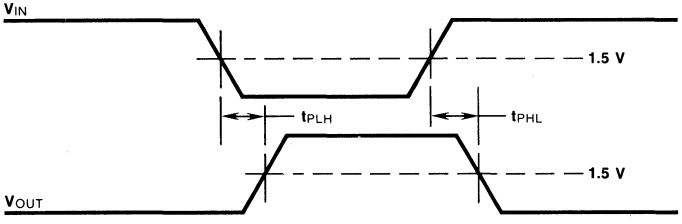
Note: Capacitance includes probe and jig capacitance

Fig. b 9005 or 9008 Extendable Gate



Note: Capacitance includes probe and jig capacitance

Fig. c 9006 Extender



NOTES:
With switch in postion (1) measure delay of 9005. With switch in position (2) measure delay (9005) + Δdelay (9006). Capacitances include probe and jig capacitances.

Fig. d Switching Waveform

9009

NAND BUFFER

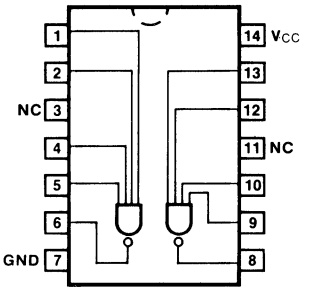
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V, ±5%, T_A = 0°C to +75°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Ceramic DIP (D)	A	9009DC	9009DM	6A
Flatpak (F)	A	9009FC	9009FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	9XXX (U.L.) HIGH/LOW
Inputs	3.0/2.0
Outputs	90/26 (99)/(25.5)

CONNECTION DIAGRAM
PINOUT A



V_{CC} = Pin 14
GND = Pin 7

DC AND AC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE: V_{CC} = +5.0 V ±5%

SYMBOL	PARAMETER		0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage		1.9		1.8		1.6		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage			0.85		0.85		0.85	V	Guaranteed Input LOW Threshold
V_{OL}	Output LOW Voltage			0.45		0.45		0.45	V	V_{CC} = 5.25 V, I_{OL} = 48 mA, V_{IN} = 5.25 V
										V_{CC} = 4.75 V, I_{OL} = 42.3 mA, Inputs at V_{IH}
I_{IH}	Input HIGH Current					120		120	μA	V_{CC} = 5.25 V, V_{IN} = 4.5 V Gnd on Other Inputs
I_{IL}	Input LOW Current			-3.2		-3.2		-3.2	mA	V_{CC} = 5.25 V, V_{IN} = .45 V 5.25 V on Other Inputs
				-2.82		-2.82		-2.82		V_{CC} = 4.75 V, V_{IN} = .45 V 5.25 V on Other Inputs
I_{CCH}	Power Supply	ON		14.6		14.6		14.6	mA	V_{IN} = Open
I_{CCL}	Current (each gate)	OFF		3.4		3.4		3.4		V_{IN} = Gnd
t_{PLH}	Propagation Delay				3.0	17			ns	Figs. 3-1, 3-4
t_{PHL}					2.0	13				C_L = 15 pF

DC AND AC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE: V_{CC} = +5.0 V ±10%

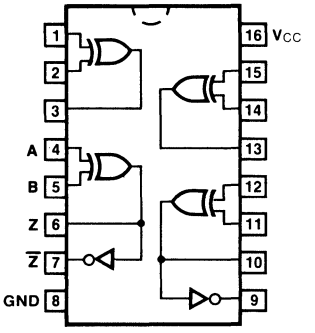
SYMBOL	PARAMETER		-55°C Min	-55°C Max	25°C Min	25°C Max	125°C Min	125°C Max	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage		2.0		1.7		1.4		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage			0.8		0.9		0.8	V	Guaranteed Input LOW Threshold
V_{OL}	Output LOW Voltage			0.4		0.4		0.4	V	V_{CC} = 5.5 V, I_{OL} = 52.8 mA V_{IN} = 5.5 V
										V_{CC} = 4.5 V, I_{OL} = 40.8 mA, Inputs at V_{IH}
I_{IH}	Input HIGH Current					120		120	μA	V_{CC} = 5.5 V, V_{IN} = 4.5 V Gnd on Other Inputs
I_{IL}	Input LOW Current			-3.2		-3.2		-3.2	mA	V_{CC} = 5.5 V V_{IN} = 0.4 V 5.5 V on Other Inputs
				-2.48		-2.48		-2.48		V_{CC} = 4.5 V V_{IN} = 0.4 V 5.5 V on Other Inputs
I_{CCH}	Power Supply	ON		12.9		12.9		12.9	mA	V_{IN} = Open
I_{CCL}	Current (each gate)	OFF		3.2		3.2		3.2		V_{IN} = Gnd
t_{PLH}	Propagation Delay				4.0	15			ns	Figs. 3-1, 3-4
t_{PHL}					3.0	10				C_L = 15 pF

9014

QUAD EXCLUSIVE-OR GATE

DESCRIPTION — The 9014 consists of four Exclusive-OR gates, useful in a large number of code conversion, parity generation/checking, and comparison applications. The Exclusive-OR gate produces an output when the inputs are complementary. Two gates have an additional inverted output which provides directly a compare capability. The Boolean expressions for the gates are: $Z = A\overline{B} + \overline{A}B$; $\overline{Z} = AB + \overline{A}\overline{B}$.

CONNECTION DIAGRAM
PINOUT A



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +75°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Ceramic DIP (D)	A	9014DC	9014DM	6B
Flatpak (F)	A	9014FC	9014FM	4L

TRUTH TABLE

INPUTS		OUTPUTS	
A	B	Z	$\overline{Z}$
L	L	L	H
L	H	H	L
H	L	H	L
H	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	9XXX Series HIGH/LOW
Inputs	2.25/1.5
Outputs	
Pins 3, 7, 9, 13	30/8.8 (33)/(8.5)
Pins 6, 10	28.5/7.9 (30)/(7.75)

DC AND AC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE: V_{CC} = +5.0 V ±5%

SYMBOL	PARAMETER	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	1.9		1.8		1.6		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage		0.85		0.85		0.85	V	Guaranteed Input LOW Threshold
V_{OL}	Output LOW Voltage		0.45		0.45		0.45	V	V_{CC} = 5.25 V, I_{OL} = 16 mA I_{OL} = 14.4 mA (Pins 6 & 10) Inputs = 5.25 V or 0 V per Truth Table

DC AND AC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE: V_{CC} = +5.0 V ±5%

SYMBOL	PARAMETER		0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage			0.45		0.45		0.45	V	V_{CC} = 4.75 V, I_{OL} = 14.1 mA I_{OL} = 12.7 mA (Pins 6 & 10) Inputs = 5.25 V or 0 V per Truth Table
I_{IL}	Input LOW Current			-2.4 -2.1		-2.4 -2.1		-2.4 -2.1	mA	V_{CC} = 5.25 V, V_{IN} = .45 V Other Inputs = 5.25 V V_{CC} = 4.75 V, V_{IN} = .45 V Other Inputs = 5.25 V
I_{CC}	Power Supply Current, each gate	ON		4.5		4.5		4.5	mA	One Input = 5.5 V, One Input = Gnd
		OFF		8.7 7.6		8.7 7.6		8.7 7.6	mA	Inputs = Gnd Inputs = 5.5 V
	Power Supply Current Per Inverter	ON		6.1		6.1		6.1	mA	Input Node HIGH
		OFF		1.7		1.7		1.7		Input Node LOW
$t_{PLH\ 1}$ $t_{PHL\ 1}$ $t_{PHH\ 1}$ $t_{PLL\ 1}$	Switching Tests				3.0 3.0 6.0 6.0	13 15 28 28			ns	C_L = 15 pF, V_{IN1} = 5.0 V Fig. a, Fig. b
$t_{PHH\ 2}$ $t_{PLL\ 2}$ $t_{PLH\ 2}$ $t_{PHL\ 2}$	Switching Tests				7.0 7.0 10 10	17 19 32 32			ns	C_L = 15 pF, V_{IN1} = 0 V Fig. a, Fig. c

DC AND AC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE: V_{CC} = +5.0 V ±10%

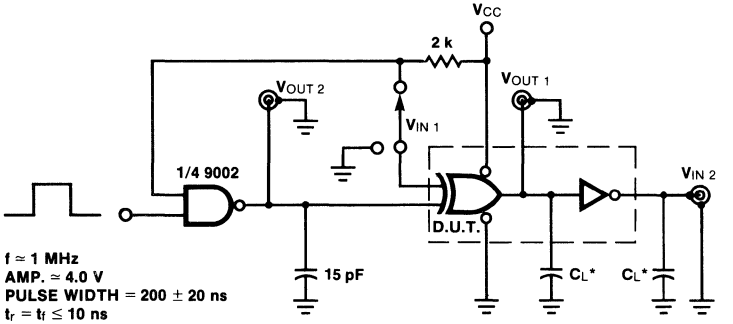
SYMBOL	PARAMETER	-55°C Min	-55°C Max	25°C Min	25°C Max	125°C Min	125°C Max	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	2.0		1.7		1.4		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage		0.8		0.9		0.8	V	Guaranteed Input LOW Threshold
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	V_{CC} = 5.5 V, I_{OL} = 17.6 mA I_{OL} = 16 mA (Pins 6 & 10) Inputs = 5.5 V or 0 V per Truth Table
			0.4		0.4		0.4		V_{CC} = 4.5 V, I_{OL} = 13.6 mA I_{OL} = 12.4 mA (Pins 6 & 10) Inputs = 5.5 V or 0 V per Truth Table

DC AND AC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE: V_{CC} = +5.0 V ±10%

SYMBOL	PARAMETER		-55°C Min	-55°C Max	25°C Min	25°C Max	125°C Min	125°C Max	UNITS	CONDITIONS
I_{IL}	Input LOW Current			-2.4		-2.4		-2.4	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V Other Inputs = 5.5 V
				-1.86		-1.86		-1.86		V_{CC} = 4.5 V, V_{IN} = 0.4 V Other Inputs = 5.5 V
I_{CC}	Power Supply Current, each gate	ON		4.2		4.2		4.2	mA	One Input = 5.5 V One Input = Gnd
		OFF		8.1		8.1		8.1	mA	Inputs = Gnd
				7.2		7.2		7.2		Inputs = 5.5 V
	Power Supply Current Per Inverter	ON		5.5		5.5		5.5	mA	Input Node HIGH
		OFF		1.6		1.6		1.6		Input Node LOW
$t_{PLH\ 1}$ $t_{PHL\ 1}$ $t_{PHH\ 1}$ $t_{PLL\ 1}$	Switching Tests				3.0 3.0 6.0 6.0	10 12 22 22			ns	C_L = 15 pF, V_{IN1} = 5.0 V Fig. a, Fig. b
$t_{PHH\ 2}$ $t_{PLL\ 2}$ $t_{PLH\ 2}$ $t_{PHL\ 2}$	Switching Tests				7.0 7.0 10 10	14 16 26 26			ns	C_L = 15 pF, V_{IN1} = 0 V Fig. a, Fig. c

5

SWITCHING TEST CIRCUIT



*C_L includes probe and jig capacity

Fig. a

WAVEFORMS

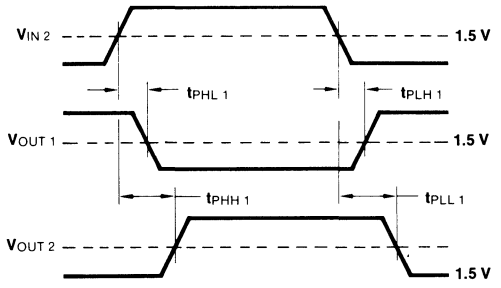


Fig. b

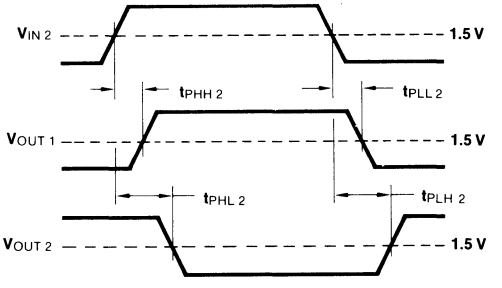


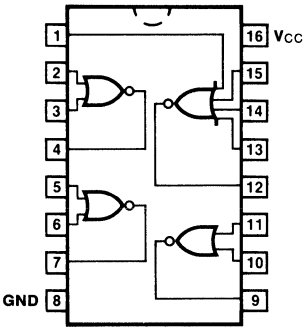
Fig. c

9015

QUAD NOR GATE

DESCRIPTION — The 9015 consists of three 2-input and one 4-input NOR gates. The NOR gate produces a LOW output if any of the inputs are HIGH.

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +75°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Ceramic DIP (D)	A	9015DC	9015DM	6B
Flatpak (F)	A	9015FC	9015FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	9XXX (U.L.) HIGH/LOW
Inputs Outputs	1.5/1.0 30/8.8 (33)/(8.5)

DC AND AC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE: V_{CC} = +5.0 V ±5%

SYMBOL	PARAMETER	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	1.9		1.8		1.6		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage		0.85		0.85		0.85	V	Guaranteed Input LOW Threshold
V_{OH}	Output HIGH Voltage	2.4		2.4		2.4		V	V_{CC} = 4.75 V, I_{OH} = -1.2 mA, Inputs = V_{IL}
V_{OL}	Output LOW Voltage		0.45		0.45		0.45	V	V_{CC} = 5.25 V, I_{OL} = 16 mA, Inputs = 5.25 V
			0.45		0.45		0.45		V_{CC} = 4.75 V, I_{OL} = 14.1 mA, Inputs = V_{IH}

DC AND AC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE (Cont'd)

SYBMOL	PARAMETER		0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	UNITS	CONDITIONS
I_{IL}	Input LOW Current			-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V, V_{IN} = .45 V 5.25 V on Other Inputs
				-1.41		-1.41		-1.41	mA	V_{CC} = 4.75 V, V_{IN} = .45 V 5.25 V on Other Inputs
I_{CC}	Power Supply Current, each gate	ON		6.55		6.55		6.55	mA	Inputs HIGH
				8.75		8.75		8.75		Inputs HIGH (4-Input Gate Only)
		OFF		3.38		3.38		3.38	mA	Inputs LOW
				6.77		6.77		6.77		Inputs LOW (4-Input Gate Only)
t_{PLH} t_{PHL}	Propagation Delay				3.0 3.0	13 15			ns	C_L = 15 pF Fig. 3-4

DC AND AC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE: V_{CC} = +5.0 V ±10%

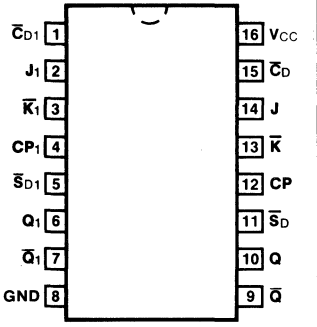
SYMBOL	PARAMETER		-55° Min	-55° Max	25°C Min	25°C Max	125°C Min	125°C Max	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage		2.0		1.7		1.4		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage			0.8		0.9		0.8	V	Guaranteed Input LOW Threshold
V_{OH}	Output HIGH Voltage		2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = -1.32 mA, Inputs = V_{IL}
V_{OL}	Output LOW Voltage			0.4		0.4		0.4	V	V_{CC} = 5.5 V, Inputs = 5.5 V, I_{OL} = 17.6 mA
				0.4		0.4		0.4		V_{CC} = 4.5 V, V_{IN} = V_{IH}, I_{OL} = 13.6 mA
I_{IL}	Input LOW Current			-1.6		-1.6		-1.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V 5.5 V on Other Inputs
				-1.24		-1.24		-1.24	mA	V_{CC} = 4.5 V V_{IN} = 0.4 V 5.5 V on Other Inputs
I_{CC}	Power Supply Current, each gate	ON		6.07		6.07		6.07	mA	Inputs HIGH
				8.14		8.14		8.14		Inputs HIGH (4-Input Gate Only)
		OFF		3.2		3.2		3.2	mA	Inputs LOW
				6.4		6.4		6.4		Inputs LOW (4-Input Gate Only)
t_{PLH} t_{PHL}	Propagation Delay				3.0 3.0	10 12			ns	C_L = 15 pF Fig. 3-4

5

9024

DUAL J$\overline{K}$ (OR D) FLIP-FLOP

CONNECTION DIAGRAM
PINOUT A

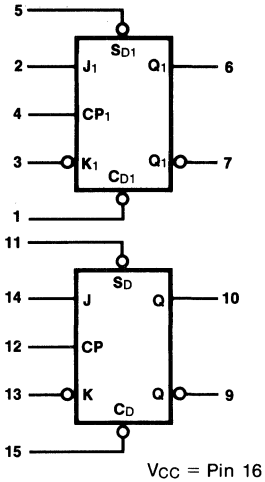


DESCRIPTION — The 9024 consists of two high speed, clocked J$\overline{K}$ flip-flops. The Clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and $\overline{K}$ pins together.

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +75°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Ceramic DIP (D)	A	9024DC	9024DM	6B
Flatpak (F)	A	9024FC	9024FM	4L

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	9XXX (U.L.) HIGH/LOW
J, $\overline{K}$ Inputs	1.5/1.0
Clock, $\overline{S}_D$ Inputs	3.0/2.0
$\overline{C}_D$ Input	6.0/3.0
Outputs	30/8.8 (7.8)

SYNCHRONOUS ENTRY J-$\overline{K}$ MODE OPERATION

INPUTS @ t_n		OUTPUTS @ t_{n+1}	
J	$\overline{K}$	Q	$\overline{Q}$
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

SYNCHRONOUS ENTRY D MODE OPERATION

INPUTS @ t_n	OUTPUTS @ t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
t_n, t_{n+1} = time before and after rising edge of CP.

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS		OUTPUTS	
$\overline{S}_D$ 5(11)	$\overline{C}_D$ 1(15)	Q 6(10)	$\overline{Q}$ 7(9)
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

DC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE: V_{CC} = +5.0 V ±5%

SYMBOL	PARAMETER	0°C		25°C		75°C		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
V_{IH}	Input HIGH Voltage	1.9		1.8		1.6		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage		0.85		0.85		0.85	V	Guaranteed Input LOW Threshold
V_{OL}	Output LOW Voltage		0.45		0.45		0.45	V	V_{CC} = 4.75 V, I_{OL} = 14.1 mA V_{CC} = 5.25 V, I_{OL} = 16 mA
I_{IH}	Input HIGH Current J, $\overline{K}$ Clock Input, $\overline{S}_D$ $\overline{C}_D$				60 120 240		60 120 240	μA	V_{CC} = 5.25 V, V_{IN} = 4.5 V Gnd on Other Inputs
I_{IL}	Input LOW Current J, $\overline{K}$ Clock Input, $\overline{S}_D$ $\overline{C}_D$*		-1.6 -3.2 -4.8		-1.6 -3.2 -4.8		-1.6 -3.2 -4.8	mA	V_{CC} = 5.25 V, V_{IN} = .45 V 4.5 V on Other Inputs
	J, $\overline{K}$ Clock Input, $\overline{S}_D$ $\overline{C}_D$*		-1.41 -2.82 -4.23		-1.41 -2.82 -4.23		-1.41 -2.82 -4.23	mA	V_{CC} = 4.75 V, V_{IN} = .45 V 4.5 V on Other Inputs
I_{OS}	Output Short Circuit Current	-30	-100	-30	-100	-30	-100	mA	V_{CC} = 5.25 V, V_{OUT} = 0 V
I_{CC}	Power Supply Current				14			mA	Per Flip-Flop in Worst Logic State

*Denotes maximum current under normal operation. These currents may increase up to 4 I_{IL} if J, K = HIGH and $\overline{S}_D$ = LOW.

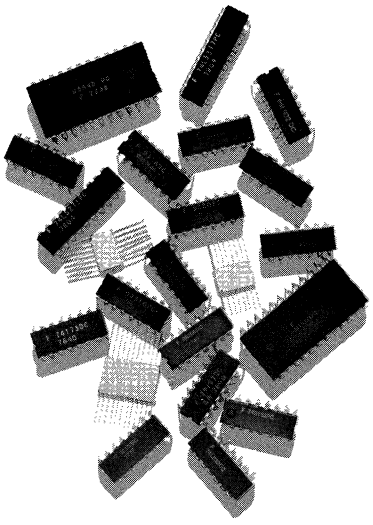
DC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE: V_{CC} = +5.0 ±10%

SYMBOL	PARAMETER	-55°C		25°C		125°C		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
V_{IH}	Input HIGH Voltage	2.0		1.7		1.4		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage		0.8		0.9		0.8	V	Guaranteed Input LOW Threshold
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 12.4 mA
									V_{CC} = 5.5 V, I_{OL} = 16 mA
I_{IH}	Input HIGH Current								
	J, $\overline{K}$				60		60	μA	V_{CC} = 5.5 V, V_{IN} = 4.5 V Gnd on Other Inputs
	Clock Input, $\overline{S}_D$				120		120		
	$\overline{C}_D$				240		240		
I_{IL}	Input LOW Current								
	J, $\overline{K}$		-1.6		-1.6		-1.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V 4.5 V on Other Inputs
	Clock Input, $\overline{S}_D$		-3.2		-3.2		-3.2		
	$\overline{C}_D$ (Note 4)		-4.8		-4.8		-4.8		
	J, $\overline{K}$		-1.24		-1.24		-1.24	mA	V_{CC} = 4.5 V, V_{IN} = 0.4 V 4.5 V on Other Inputs
	Clock Input, $\overline{S}_D$		-2.48		-2.48		-2.48		
	$\overline{C}_D$*		-3.72		-3.72		-3.72		
I_{OS}	Output Short Circuit Current	-30	-100	-30	-100	-30	-100	mA	V_{CC} = 5.5 V, V_{OUT} = 0 V
I_{CC}	Power Supply Current				14			mA	Per Flip-Flop in Worst Logic State

*Denotes maximum current under normal operation. These currents may increase up to 4 I_{IL} if J, K = HIGH and $\overline{S}_D$ = LOW.

SWITCHING CHARACTERISTICS: T_A = 25°C, V_{CC} = +5.0 V, C_L = 15 pF

SYMBOL	PARAMETER	9XXX		UNITS	TEST CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CP to Q or $\overline{Q}$		20 33	ns	Figs. 3-1, 3-8
t_h (H) t_h (L)	Hold Time HIGH or LOW J, $\overline{K}$ to CP	0		ns	Figs. 3-1, 3-6
t_s (H) t_s (L)	Setup Time HIGH or LOW J, $\overline{K}$ to CP	20	1.0	ns	
t_{PLH}	Propagation Delay $\overline{S}_D$ to Q, $\overline{C}_D$ to $\overline{Q}$		12	ns	Figs. 3-1, 3-16
t_{PHL}	Propagation Delay $\overline{S}_D$ to $\overline{Q}$, $\overline{C}_D$ to Q		25	ns	
f_{max}	Maximum Toggle Frequency	25		MHz	Figs. 3-1, 3-8



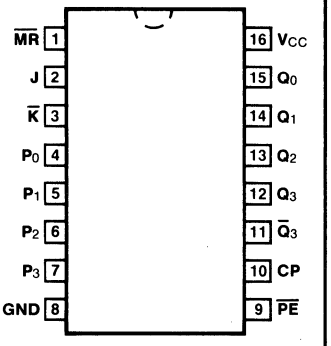
9300
93H00
93L00
93S00

4-BIT UNIVERSAL SHIFT REGISTER

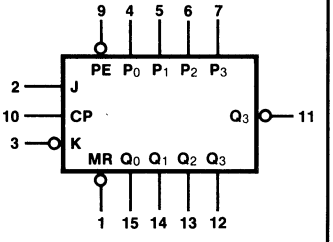
DESCRIPTION — The '00 is a 4-bit universal shift register. As a high speed multifunctional sequential logic block, it is useful in a wide variety of register and counter applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers.

- **ASYNCHRONOUS MASTER RESET**
- **J, $\overline{K}$ INPUTS TO FIRST STAGE**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

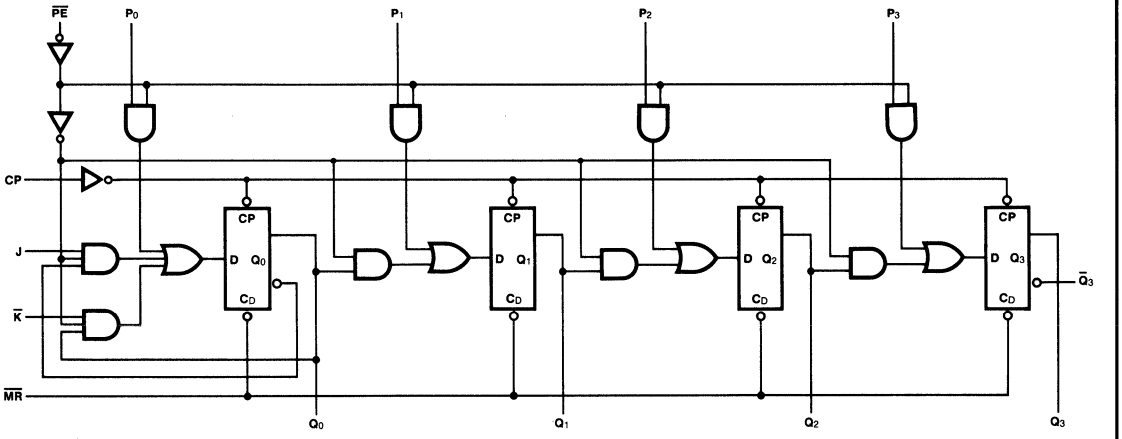
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9300PC, 93H00PC 93L00PC, 93S00PC		9B
Ceramic DIP (D)	A	9300DC, 93H00DC 93L00DC, 93S00DC	9300DM, 93H00DM 93L00DM, 93S00DM	6B
Flatpak (F)	A	9300FC, 93H00FC 93L00FC, 93S00FC	9300FM, 93H00FM 93L00FM, 93S00FM	4L

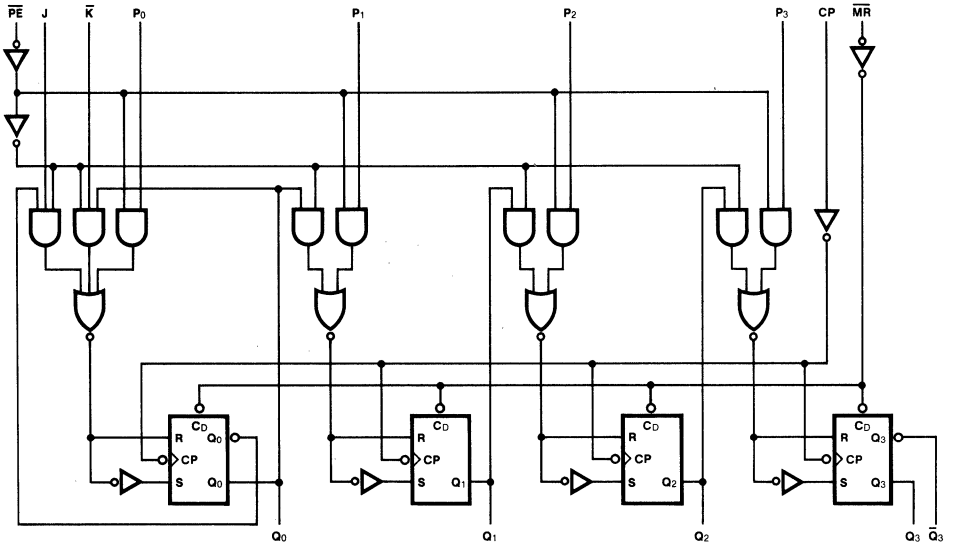
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93H (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW	93S (U.L.) HIGH/LOW
$\overline{PE}$	Parallel Enable Input (Active LOW)	2.3/2.3	1.0/1.0	1.15/0.575	1.25/1.25
$P_0 - P_3$	Parallel Inputs	1.0/1.0	1.0/1.0	0.5/0.25	1.0/1.0
J	First Stage J Input (Active HIGH)	1.0/1.0	1.0/1.0	0.5/0.25	1.0/1.0
$\overline{K}$	First Stage K Input (Active LOW)	1.0/1.0	1.0/1.0	0.5/0.25	1.0/1.0
CP	Clock Pulse Input (Active Rising Edge)	2.0/2.0	2.0/2.0	1.0/0.5	2.5/2.5
$\overline{MR}$	Master Reset Input	1.0/1.0	1.0/1.0	0.5/0.25	1.25/1.25
$Q_0 - Q_3$	Parallel Outputs	12/6.0	16/8.0	10/5.0 (3.0)	25/12.5
$\overline{Q}_3$	Complementary Last Stage Output	16/8.0	20/10	10/5.0 (3.0)	25/12.5

LOGIC DIAGRAMS
'00, 'H00, 'L00



'S00



FUNCTIONAL DESCRIPTION — The Logic Diagrams and Truth Table indicate the functional characteristics of the '00 4-bit shift register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers.

The '00 has two primary modes of operation, shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ input is HIGH, serial data enters the first flip-flop Q_0 via the J and $\overline{K}$ inputs and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The $J\overline{K}$ inputs provide the flexibility of the JK type input for special applications, and the simple D-type input for general applications by tying the two pins together. When the $\overline{PE}$ input is LOW, the '00 appears as four common clocked D flip-flops. The data on the parallel inputs $P_0 — P_3$ is transferred to the respective $Q_0 — Q_3$ outputs following the LOW-to-HIGH clock transition. Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the P_{n-1} inputs and holding the $\overline{PE}$ input LOW.

All serial and parallel data transfers are synchronous, occuring after each LOW-to-HIGH clock transition. Since the '00 utilizes edge triggering, there is no restriction on the activity of the J, $\overline{K}$, P_n and $\overline{PE}$ inputs for logic operation — except for the setup and release time requirements. A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

TRUTH TABLE

OPERATING MODE	INPUTS ($\overline{MR}$ = H)							OUTPUTS @ t_{n+1}				
	$\overline{PE}$	J	$\overline{K}$	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
SHIFT MODE	H	L	L	X	X	X	X	L	Q_0	Q_1	Q_2	$\overline{Q}_2$
	H	L	H	X	X	X	X	Q_0	Q_0	Q_1	Q_2	$\overline{Q}_2$
	H	H	L	X	X	X	X	$\overline{Q}_0$	Q_0	Q_1	Q_2	$\overline{Q}_2$
	H	H	H	X	X	X	X	H	Q_0	Q_1	Q_2	$\overline{Q}_2$
PARALLEL ENTRY MODE	L	X	X	L	L	L	L	L	L	L	L	H
	L	X	X	H	H	H	H	H	H	H	H	L

*t_{n+1} = Indicates state after next LOW-to-HIGH clock transition.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		93XX		93H		93L		93S		UNITS	CONDITIONS
			Min	Max	Min	Max	Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current		-20	-80	-30	-100					mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current	XC		92		112		23		120	mA	V_{CC} = Max
		XM		86		102						

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C)See Section 3 for waveforms and load configurations)

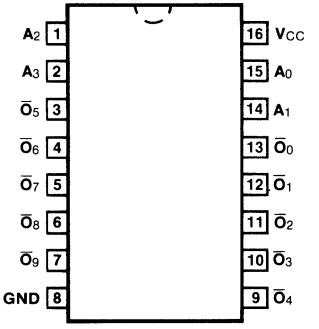
SYMBOL	PARAMETER	93XX		93H		93L		93S		UNITS	CONDITIONS
		C_L = 15 pF		C_L = 15 pF		C_L = 15 pF		C_L = 15 pF			
		Min	Max	Min	Max	Min	Max	Min	Max		
f_{max}	Maximum Shift Frequency	30		45		10		70		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		22 26		16 21		35 51		8.5 12	ns	Figs. 3-1, 3-8
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		40		28		60		23	ns	Figs. 3-1, 3-17

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	93XX		93H		93L		93S		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW, J, $\overline{K}$ and $P_0 - P_3$ to CP	20 20		12 12		60 60		6.0 6.0		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW, J, $\overline{K}$ and $P_0 - P_3$ to CP	0 0		0 0		0 0		0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW, $\overline{PE}$ to CP	39 39		15 15		68 68		8.0 8.0		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW, $\overline{PE}$ to CP	-10 -10		0 0		-20 -20		0 0		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	17 17		12 12		38 38		7.0 7.0		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	25		19		53		12		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	25		7.0		70		5.0		ns	

9301
93L01
1-OF-10 DECODER

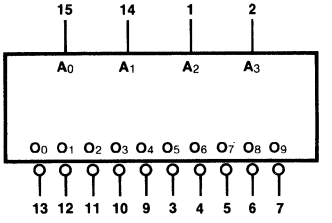
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '01 multipurpose decoders are designed to accept four inputs and provide ten mutually exclusive outputs.

- **MULTIFUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **DEMULTIPLEXING CAPABILITY**
- **TYPICAL POWER DISSIPATION OF 145 mW for '01, 45mW for 'L01**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9301PC, 93L01PC		9B
Ceramic DIP (D)	A	9301DC, 93L01DC	9301DM, 93L01DM	6B
Flatpak (F)	A	9301FC, 93L01FC	9301FM, 93L01FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	1.0/1.0	0.5/0.25
$\overline{O}_0 - \overline{O}_9$	Decoder Outputs (Active LOW)	20/10	10/5.0 (3.0)

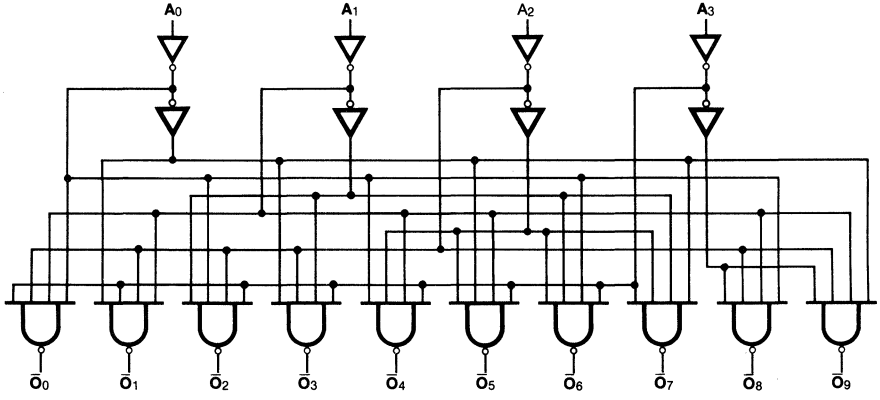
FUNCTIONAL DESCRIPTION — The '01 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with active LOW input enables. The logic design of the '01 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs. The most significant input A_3 produces a useful inhibit function when the '01 is used as a 1-of-8 decoder.

TRUTH TABLE

INPUTS				OUTPUTS									
A_0	A_1	A_2	A_3	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$	$\overline{O}_8$	$\overline{O}_9$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		44		13	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

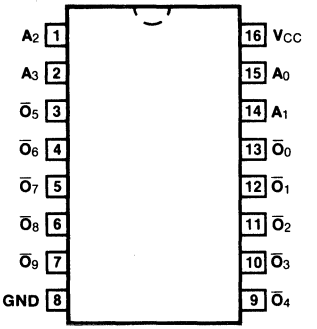
SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C_L = 15 pF		C_L = 15 pF			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$		35 30		36 36	ns	Figs. 3-1, 3-20

9302

1-OF-10 DECODER

(With Open-Collector Outputs)

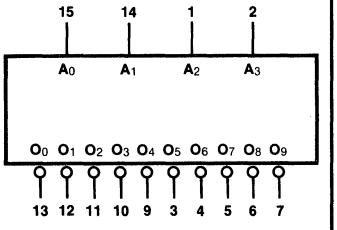
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '02 is a multipurpose decoder designed to accept four inputs and provide ten mutually exclusive outputs. The open-collector outputs provide wired-OR capability which can be used for numerous summing, decoding and demultiplexing operations.

- **OUTPUTS HAVE WIRED-OR CAPABILITY**
- **PROVIDES CAPABILITY TO GENERATE AND SUM MINTERMS OF 3 OR 4 VARIABLES**
- **ACTIVE LOW OUTPUTS ARE USEFUL FOR DRIVING LOW VOLTAGE LAMPS AND RELAYS**
- **MULTIFUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **DEMULTIPLEXING CAPABILITY**
- **TYPICAL POWER DISSIPATION OF 145 mW**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9302PC		9B
Ceramic DIP (D)	A	9302DC	9302DM	6B
Flatpak (F)	A	9302FC	9302FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
$\overline{A_0} - \overline{A_3}$	Address Inputs	1.0/1.0
$\overline{O_0} - \overline{O_9}$	Decoder Outputs (Active LOW)	OC*/10

*OC — Open Collector

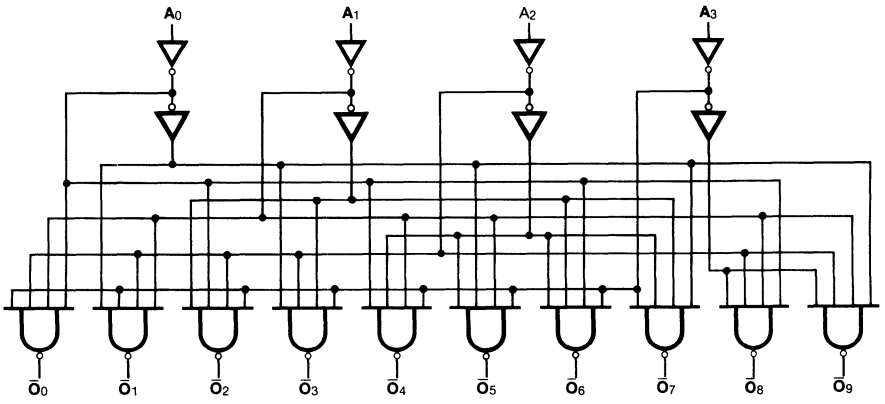
FUNCTIONAL DESCRIPTION — The '02 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by the logic symbol. The open-collector outputs provide easy summing of input terms. The '02 provides the capability in one package to generate and sum any or all of the minterms of three variables, or the first 10-or-16 minterms of four variables. The logic design of the '02 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs. The most significant input (A_3) produces a useful inhibit function when the '02 is used as a 1-of-8 decoder.

TRUTH TABLE

INPUTS				OUTPUTS									
A_0	A_1	A_2	A_3	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$	$\overline{O}_8$	$\overline{O}_9$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		Min	Max		
I_{CEX}	Output HIGH Leakage Current		250	μA	V_{CC} = Min, V_{CEX} = 5.5 V V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{CC}	Power Supply Current		44	mA	V_{CC} = Max

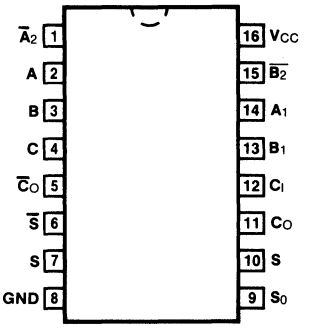
AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF R_L = 400 Ω		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$		35 30	ns	Figs. 3-2, 3-20

9304

DUAL FULL ADDER

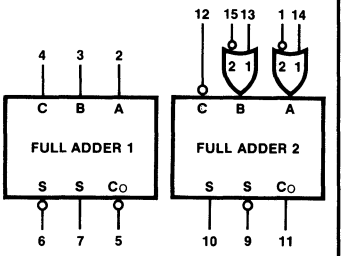
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '04 consists of two independent, binary full adders. The adders are useful in a wide variety of applications including multiple bit parallel add/serial carry addition, parity generation and checking, code conversion and majority gating.

- **MULTIFUNCTION CAPABILITY**
- **8.0 ns CARRY PROPAGATION DELAY**
- **COMPLEMENTARY INPUTS AND OUTPUTS AVAILABLE**
- **TYPICAL POWER DISSIPATION OF 150 mW**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10 %, T_A = -55°C to +125°C	
Plastic DIP (P)	A	9304PC		9B
Ceramic DIP (D)	A	9304DC	9404DM	6B
Flatpak (F)	A	9304FC	9304FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
Full Adder 1		
A, B	Operand Inputs	4.0/4.0
C_I	Carry Input	4.0/4.0
S	Sum Output	20/10
$\overline{S}$	Complementary Sum Output	20/10
$\overline{C}_O$	Carry Output (Active LOW)	14/7.0
Full Adder 2		
A_1, B_1	OR Operand Inputs (Active HIGH)	1.0/1.0
$\overline{A}_2$, $\overline{B}_2$	OR Operand Inputs (Active LOW)	4.0/4.0
$\overline{C}_I$	Carry Input (Active LOW)	4.0/4.0
S	Sum Output	20/10
$\overline{S}$	Complementary Sum Output	20/10
C_O	Carry Output (Active HIGH)	14/7.0

FUNCTIONAL DESCRIPTION — The '04 logic block consists of two separate high speed carry dependent sum full adders. This design allows a minimum carry propagation time when the adders are used in ripple carry applications. The adders are identical except that adder 2 has provision for either active HIGH or active LOW inputs at the A and B terminals. The adders produce a LOW carry and both LOW and HIGH sum with active HIGH inputs, a HIGH carry and both HIGH and LOW sum when active LOW inputs are used. This principle of duality is shown in the diagram below, where the adders are drawn as functional blocks.

TRUTH TABLES

ADDER 1

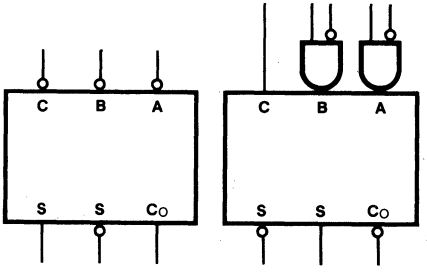
INPUTS			OUTPUTS		
$\overline{C}_I$	B	A	$\overline{C}_O$	$\overline{S}$	S
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

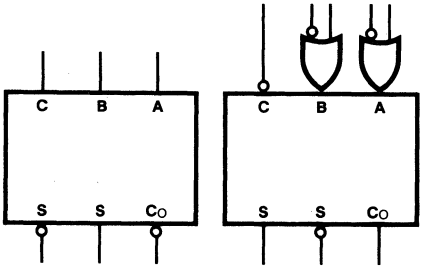
ADDER 2

INPUTS					OUTPUTS		
$\overline{C}_I$	B_1	A_1	$\overline{B}_2$	$\overline{A}_2$	C_O	S	$\overline{S}$
L	L	L	L	L	H	H	L
L	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H
L	L	L	H	H	L	H	L
L	L	H	L	L	H	H	L
L	L	H	L	H	H	H	L
L	L	H	H	L	H	L	H
L	L	H	H	H	H	L	H
L	H	L	L	L	H	H	L
L	H	L	L	H	H	L	H
L	H	L	H	L	H	H	L
L	H	L	H	H	H	L	H
L	H	H	L	L	H	H	L
L	H	H	L	H	H	H	L
L	H	H	H	L	H	H	L
L	H	H	H	H	H	H	L
H	L	L	L	L	H	L	H
H	L	L	L	H	L	H	L
H	L	L	H	L	L	H	L
H	L	L	H	H	L	L	H
H	L	H	L	L	H	L	H
H	L	H	L	H	H	L	H
H	L	H	H	L	L	H	L
H	L	H	H	H	L	H	L
H	H	L	L	L	H	L	H
H	H	L	L	H	L	H	L
H	H	L	H	L	H	L	H
H	H	L	H	H	L	H	L
H	H	H	L	L	H	L	H
H	H	H	L	H	H	L	H
H	H	H	H	L	H	L	H
H	H	H	H	H	H	L	H

ACTIVE LOW

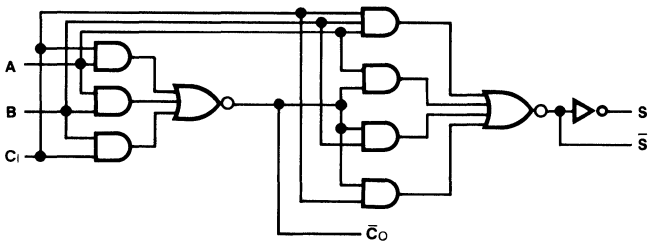


ACTIVE HIGH

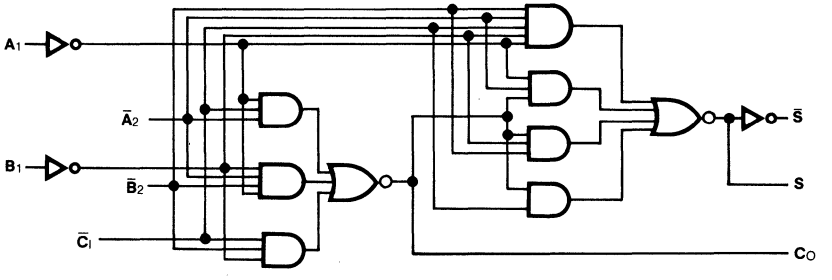


LOGIC DIAGRAM

ADDER 1



ADDER 2



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		Min	Max		
I_{SC}	Output Short Circuit Current	-20	-70	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current		55	mA	V_{CC} = Max, Pins 13 & 14 = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		C_L = 15 pF			
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to $\bar{S}$		36 35	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay C_I to C_O		13 13	ns	Figs. 3-1, 3-4

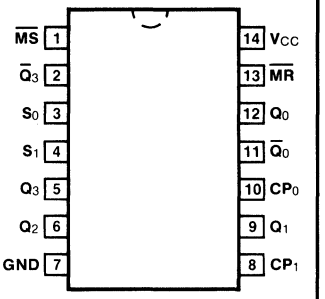
9305

VARIABLE MODULUS COUNTER

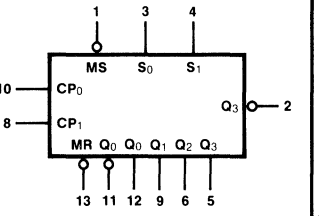
DESCRIPTION — The '05 is a monolithic, high speed, variable modulus counter circuit. It is a semisynchronous counter which can be programmed without extra logic to provide division or counting by either 2 and 4, 5, 6, 7, 8 or 10, 12, 14, 16. A binary count sequence can be obtained for all of the preceding counter modulos as well as 50% duty cycle output for dividers of 8, 10, 12, 14, 16. The device also features asynchronous overriding Master Reset and Set inputs and the negation output of the final flip-flop output which allows the cascading of stages.

- **VARIOUS BINARY COUNTING MODES**
  MODULO 2 AND MODULO 5, 6, 7, 8
  MODULO 10 (8421 BCD) 12, 14, 16
- **VARIOUS DIVISION MODES WITH 50% DUTY CYCLE OUTPUT**
  MODULO 8, 10, 12, 14, 16
- **LOGIC SELECTION OF COUNTING MODE**
- **ASYNCHRONOUS MASTER RESET ANS SET INPUTS**
- **MULTISTAGE COUNTING OPERATION**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9305PC		9A
Ceramic DIP (D)	A	9305DC	9305DM	6A
Flatpak (F)	A	9305FC	9305FM	3B

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
S_0 , S_1	Select Inputs	1.0/1.0
CP_0	First Stage Clock Pulse Input (Active Rising Edge)	1.0/1.0
CP_1	Three Stage Clock Pulse Input (Active Rising Edge)	1.0/1.0
$\overline{MS}$	Master Set Input (Active LOW)	1.0/1.0
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0
Q_0	First Stage Output	16/8.0
$\overline{Q}_0$	Complementary First Stage Output	16/8.0
$Q_1 - Q_3$	Three Stage Counter Outputs	16/8.0
$\overline{Q}_3$	Complementary Last Stage Output	20/10

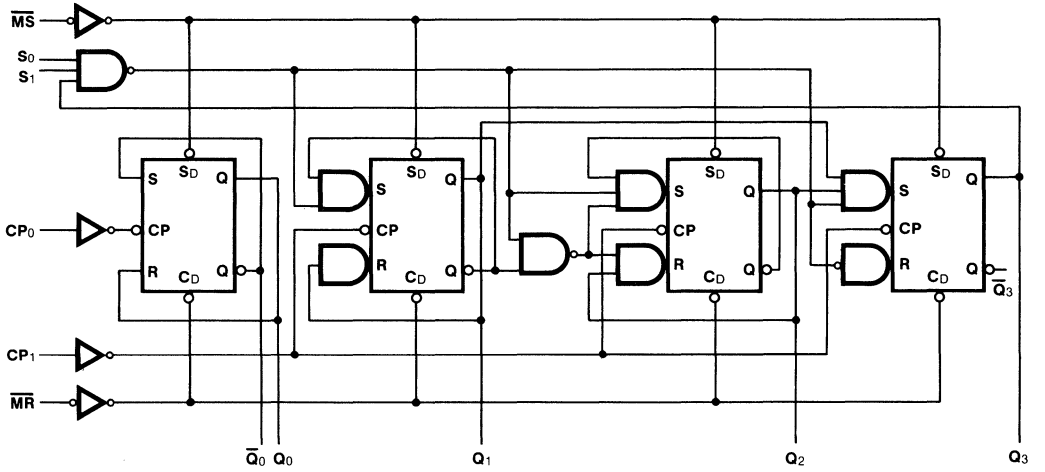
FUNCTIONAL DESCRIPTION — The '05 consists of four master/slave flip-flops which are separated into two functional units — a single toggle stage and a three stage synchronous counter. All four flip-flips change state on the LOW-to-HIGH transition of the clock. The three stage counter can be programmed with external connections to provide moduli of either 5, 6, 7 or 8. This basic configuration allows synchronous binary counting by the last three stages and independent modulo 2 operation with the first single stage.

A four stage binary counter with a modulo of 10, 12, 14 or 16 is obtained by applying the incoming clock to the single toggle stage and feeding its negation output to the clock input of the three stage counter. A 4-stage divider with 50% duty cycle output is produced by feeding the incoming clock to the three stage counter and clocking the single stage with the $\overline{Q}_3$ output. In either the binary or 50% division mode the modulo (10, 12, 14, 16) is determined by the external programming connections for the three stage counter. These 4-stage counters or dividers are not fully synchronous (semisynchronous) but have only one flip-flop ripple delay in either configuration. Counter moduli other than 10, 12, 14, 16 can be formed with a few extra gates.

Several '05 variable modulus counters programmed in any modulo can be connected together without extra logic to form asynchronous (ripple) type multistage counters. This is done by connecting the $\overline{Q}_3$ output of the less significant counter to the clock input of the following counter.

The Master Set and Reset will asynchronously set or reset all four stages when activated. The active LOW Reset input when LOW will clear the counter, overriding the clock and forcing the outputs Q_0 — Q_3 LOW and outputs $\overline{Q}_0$, $\overline{Q}_3$ HIGH. The active LOW Set input when LOW will preset the counter, overriding the clock and forcing the outputs Q_0 — Q_3 HIGH and outputs $\overline{Q}_0$, $\overline{Q}_3$ LOW. The master set provides a synchronous clear, since the first clock pulse following the asynchronous master set will reset all stages. This action is independent of the molulo programmed.

LOGIC DIAGRAM



COUNTING MODE

The following are rules specifying the external connections required for various counter and divider modulos.

ASYNCHRONOUS MODE

INPUTS		OUTPUTS					
$\overline{MS}$	$\overline{MR}$	Q_0	$\overline{Q_0}$	Q_1	$\overline{Q_2}$	Q_3	$\overline{Q_3}$
L	H	H	L	H	H	H	L
H	L	L	H	L	L	L	H
H	H	COUNT*					

*As determined by programming connections.
H = HIGH Voltage Level
L = LOW Voltage Level

PROGRAMMING CONNECTIONS FOR LAST THREE STAGES

S_0	S_1	MODULO
NC	NC	5
Q_1	NC	6
NC	Q_1	6
Q_2	NC	7
NC	Q_2	7
Q_1	Q_2	8
Q_2	Q_1	8

NC = Not Connected

CONNECTIONS FOR MODULO 10, 12, 14, 16 BINARY COUNTERS AND 50% DUTY CYCLE DIVIDERS

For Binary Counting $\overline{Q_0}$ connected to CP_1 Incoming clock to CP_0
For 50% Duty Cycle Output $\overline{Q_3}$ connected to CP_0 Incoming Clock to CP_1

ALTERNATE PROGRAMMING CONNECTIONS FOR LAST THREE STAGES**

MODULO	INPUTS		OUTPUT	AVAILABLE OUTPUT FAN-OUT
	S_0	S_1		
5	Q_3	Q_3	Q_3	14/8.0
6	Q_1	Q_1	Q_1	14/7.0
7	Q_2	Q_2	Q_2	14/7.0
8	Q_1	Q_2	Q_2	15/7.0
8	Q_2	Q_1	Q_1	15/7.0

**The alternate programming connections program the counter and conveniently terminate unused select inputs (NC). Since these inputs form the inputs to a single NAND gate (See logic diagram), their connection to the counter outputs for the various count modulos provides the indicated output drive.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		Min	Max		
I_{SC}	Output Short Circuit Current	-20	-70	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current		66	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

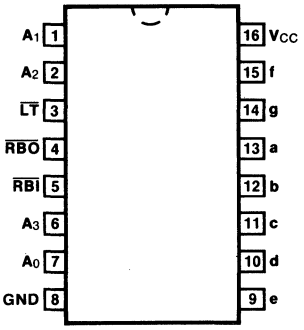
SYMBOL	PARAMETER	93XX C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Count Frequency	23		MHz	Modulo 16 (S_0 to Q_1, S_1 to Q_2, Q_0 to CP_1, Input to CP_0) Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP_0 to $\overline{Q}_3$ (Modulo 16 Connection)		38 48	ns	
t_{PLH} t_{PHL}	Propagation Delay CP_0 to $\overline{Q}_0$		21 30	ns	Modulo-16 Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP_1 to $\overline{Q}_3$ or $\overline{Q}_3$		23 30	ns	Modulo-8 Figs. 3-1, 3-8
t_{PLH}	Propagation Delay $\overline{MS}$ to Q_1		26	ns	Modulo-8 Figs. 3-1, 3-16
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_1		35	ns	Modulo-8 Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		Min	Max		
t_w	CP_0 Pulse Width	22		ns	Fig. 3-8
t_w	$\overline{MR}$ or $\overline{MS}$ Pulse Width	24		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MS}$ to CP_1	25		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP_1	30		ns	Fig. 3-16

9307
7-SEGMENT DECODER

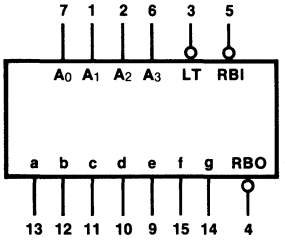
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '07 7-segment decoder is designed to accept four inputs in 8421 BCD code and provide the appropriate outputs to drive a 7-segment numerical display. The decoder can be used with 7-segment incandescent lamp, neon, electro-luminescent, or CRT numeric displays.

- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING-EDGE ZEROES**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **LAMP TEST FACILITY**
- **BLANKING INPUT**
- **ACTIVE HIGH OUTPUTS**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9307PC		9B
Ceramic DIP (D)	A	9307DC	9307DM	6B
Flatpak (F)	A	9307FC	9307FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
$A_0 - A_3$	BCD Inputs	0.25/1.0
$\overline{RBI}$	Ripple Blanking Input (Active LOW)	0.25/0.5
$\overline{LT}$	Lamp Test Input (Active LOW)	1.25/4.0
$\overline{RBO}$	Ripple Blanking Output (Active LOW)	1.75/1.5
a — g	Segment Outputs (Active HIGH)	0/6.25

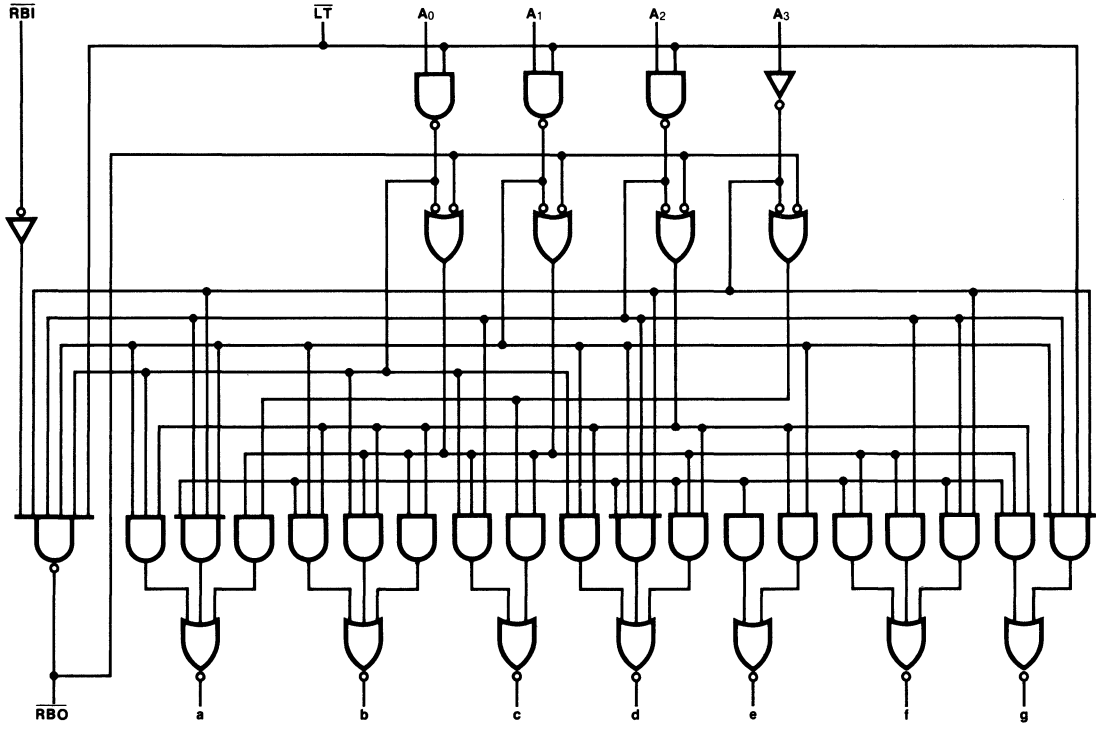
FUNCTIONAL DESCRIPTION — The '07 7-segment decoder accepts a 4-bit BCD 8421 code input and produces the appropriate outputs for selection of segments in a 7-segment matrix display used for representing the decimal numbers 0-9. The seven outputs (a, b, c, d, e, f, g) of the decoder select the corresponding segments in the matrix shown in *Figure a*. The numeric designations chosen to represent the decimal numbers are shown in *Figure b*, together with the resulting displays for input code configurations in excess of binary nine.

The decoder has active HIGH outputs so that a buffer transistor may be used directly to provide the high currents required for incandescent displays. If additional base drive current is required external resistors may be added from the supply voltage to the seven segment outputs of the decoders. If additional base drive current is required external resistors may be added from the supply voltage to the seven segment outputs of the decoders. The value of this resistor is constrained by the 10 mA current sinking capability of the output transistors of the circuit.

The device has provision for automatic blanking of the leading and/or trailing-edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading-edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and, since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing-edge zeroes.

The decoder has an active LOW input Lamp Test which overrides all other input combinations and enables a check to be made on possible display malfunctions. The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL gates.

LOGIC DIAGRAM



TRUTH TABLE

INPUTS						OUTPUTS								
$\overline{LT}$	$\overline{RBI}$	A_0	A_1	A_2	A_3	a	b	c	d	e	f	g	$\overline{RBO}$	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	
H	L	L	L	L	L	L	L	L	L	L	L	L	L	0
H	H	L	L	L	L	H	H	H	H	H	H	L	H	0
H	X	H	L	L	L	L	H	H	L	L	L	L	H	1
H	X	L	H	L	L	H	H	L	H	H	L	H	H	2
H	X	H	H	L	L	H	H	H	H	L	L	H	H	3
H	X	L	L	H	L	L	H	H	L	L	L	H	H	4
H	X	H	L	H	L	H	L	H	H	L	H	H	H	5
H	X	L	H	H	L	H	L	H	H	H	H	H	H	6
H	X	H	H	H	L	H	H	H	L	L	L	L	H	7
H	X	L	L	L	H	H	H	H	H	H	H	H	H	8
H	X	H	L	L	H	H	H	H	H	L	H	H	H	9
H	X	L	H	L	H	L	L	L	H	H	L	H	H	10
H	X	H	H	L	H	L	L	L	H	L	L	H	H	11
H	X	L	L	H	H	L	H	H	L	L	H	H	H	12
H	X	H	L	H	H	H	L	H	H	L	H	H	H	13
H	X	L	H	H	H	L	L	L	H	H	H	H	H	14
H	X	H	H	H	H	L	L	L	L	L	L	L	H	15

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

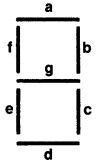


Fig. a Segment Designation

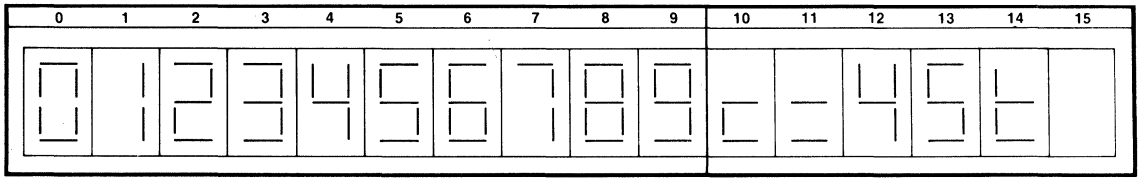


Fig. b Numerical Designations

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			93XX Min	93XX Max	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	at a—g		4.3		V	V_{CC} = Min I_{OH} = 0 mA	
		at $\overline{RBO}$	XM XC	3.0 2.7		V	V_{CC} = Min I_{OH} = -70 μA	
V_{OL}	Output LOW Voltage	at a—g	XM		0.4	V	I_{OL} = 12.5 mA	V_{CC} = Max
			XC		0.45		I_{OL} = 11.5 mA	
		at $\overline{RBO}$	XM		0.4	V	I_{OL} = 3.1 mA	
			XC		0.45		I_{OL} = 2.75 mA	
		at a—g	XM		0.4	V	I_{OL} = 10 mA	V_{CC} = Min
			XC		0.45			
		at $\overline{RBO}$	XM		0.4	V	I_{OL} = 2.4 mA	
			XC		0.45			
I_A	Available Output Current at a—g		XM	-1.0		mA	V_{OUT} = 0.85 V	V_{CC} = Min
			XC	-1.1			V_{OUT} = 0.75 V	T_A = Max
I_{OS}	Output Short Circuit Current at a—g		XM		-3.7	mA	V_{CC} = Max, T_A = +25°C V_{OUT} = 0 V	
			XC		-4.0			
I_{CC}	Power Supply Current		XM		73	mA	V_{CC} = Max	
			XC		82			

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

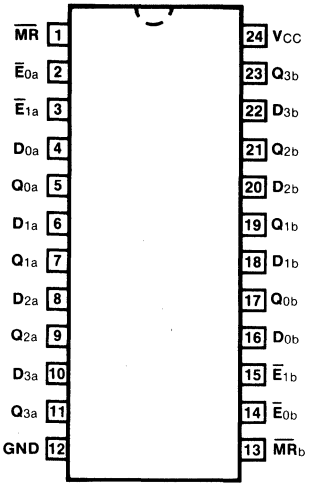
SYMBOL	PARAMETER	93XX C_L = 30 pF Min	93XX C_L = 30 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_0—A_3 or $\overline{RBI}$ to a—g or $\overline{RBO}$		750 750	ns	Fig. 3-20

6

9308
93L08
DUAL 4-BIT LATCH

DESCRIPTION — The '08 is a dual 4-bit D-type latch designed for general purpose storage applications in digital systems. Each latch contains both an active LOW Master Reset input an active LOW Enable inputs. The 54/74116 is a pin for pin equivalent of the 9308.

CONNECTION DIAGRAM
PINOUT A



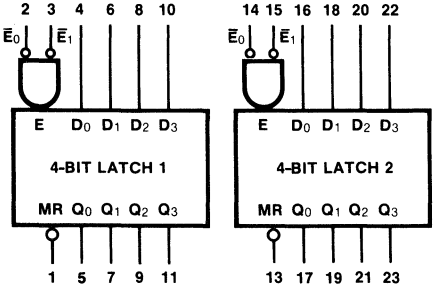
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	9308PC, 93L08PC		9N
Ceramic DIP (D)	A	9308DC, 93L08DC	9308DM, 93L08DM	6N
Flatpak (F)	A	9308FC, 93L08FC	9308FM, 93L08FM	4M

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
D_{0a} — D_{3a}, D_{0b} — D_{3b}	Parallel Latch Inputs	1.5/1.5	0.75/0.375
$\bar{E}_{0a}$, $\bar{E}_{1a}$, $\bar{E}_{0b}$, $\bar{E}_{1b}$	AND Enable Inputs (Active LOW)	1.0/1.0	0.5/0.25
$\overline{MR}_a$, $\overline{MR}_b$	Master Reset Inputs (Active LOW)	1.0/1.0	0.5/0.25
Q_{0a} — Q_{3a}, Q_{0b} — Q_{3b}	Parallel Latch Outputs	20/10	10/5.0 (3.0)

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

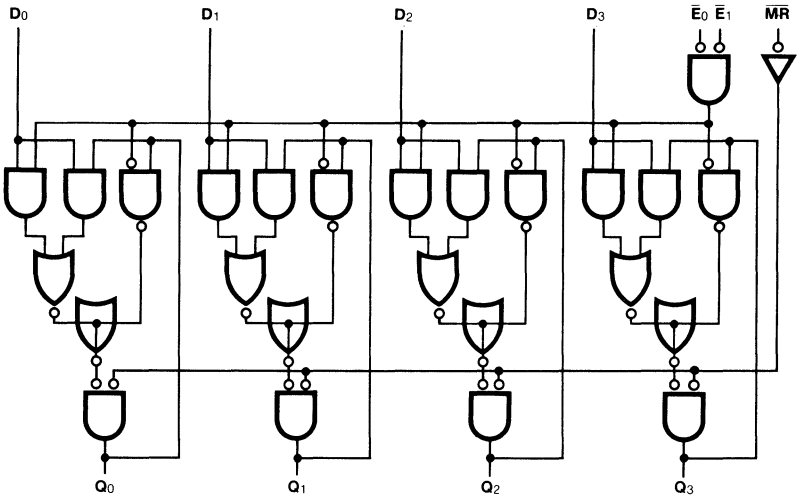
FUNCTIONAL DESCRIPTION — Data can be entered into the latch when both of the enable inputs are LOW. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes HIGH, the data present in the latch at that time is held in the latch and is no longer affected by data input. The master reset overrides all other input conditions and forces the outputs of all the latches LOW when a LOW signal is applied to the Master Reset input.

TRUTH TABLE

$\overline{MR}$	$\overline{E}_0$	$\overline{E}_1$	D	Q_n	OPERATION
H	L	L	L	L	Data Entry
H	L	L	H	H	Data Entry
H	L	H	X	Q_{n-1}	Hold
H	H	L	X	Q_{n-1}	Hold
H	H	H	X	Q_{n-1}	Hold
L	X	X	X	L	Reset

Q_{n-1} = Previous Output State
Q_n = Present Output State
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		100		29	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C_L = 15 pF, R_L = 400 Ω		C_L = 15 pF			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_n$ to Q_n		30 22		45 38	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		15 18		27 29	ns	Figs. 3-1, 3-5
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		22		30	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

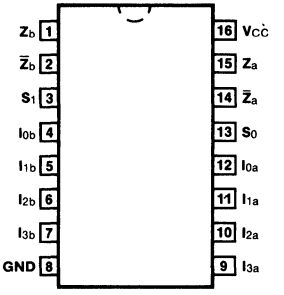
SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H)	Setup Time HIGH, D_n to $\overline{E}_n$	10		8.0		ns	Fig. 3-13
t_h (H)	Hold Time HIGH, D_n to $\overline{E}_n$	-2.0		0		ns	
t_s (L)	Setup Time LOW, D_n to $\overline{E}_n$	12		18		ns	Fig. 3-13
t_h (L)	Hold Time LOW, D_n to $\overline{E}_n$	8.0		4.0		ns	
t_w (L)	$\overline{E}_n$ Pulse Width LOW	18		30		ns	Fig. 3-21
t_w (L)	$\overline{MR}$ Pulse Width LOW	18		32		ns	Fig. 3-16
t_{rec}	Recovery Time, $\overline{MR}$ to $\overline{E}_n$	8.0		10		ns	Fig. 3-16

9309
93L09
DUAL 4-INPUT MULTIPLEXER

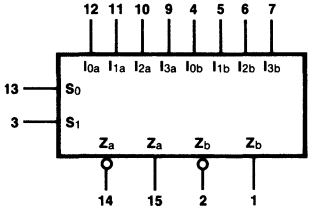
DESCRIPTION — The '09 monolithic dual 4-input digital multiplexers consist of two multiplexing circuits with common input select logic. Each circuit contains four inputs and fully buffered complementary outputs. In addition to multiplexer operation, the '09 can generate any two function of three variables. Active pullups in the outputs ensure high drive and high speed performance. Because or its high speed performance and on-chip select decoding, the '09 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output bus.

- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9309PC, 93L09PC		9B
Ceramic DIP (D)	A	9309DC, 93L09DC	9309DM, 93L09DM	6B
Flatpak (F)	A	9309FC, 93L09FC	9309FM, 93L09FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
S_0, S_1	Common Select Inputs	1.0/1.0	0.5/0.25
I_{0a} — I_{3a}	Multiplexer A Inputs	1.0/1.0	0.5/0.25
Z_a	Multiplexer A Output	20/10	10/5.0 (3.0)
$\overline{Z}_a$	Complementary Multiplexer A Output	18/9.0	10/5.0 (3.0)
I_{0b} — I_{3b}	Multiplexer B Inputs	1.0/1.0	0.5/0.25
Z_b	Multiplexer B Output	20/10	10/5.0 (3.0)
$\overline{Z}_b$	Complementary Multiplexer B Output	18/9.0	10/5.0 (3.0)

FUNCTIONAL DESCRIPTION — The '09 dual 4-input multiplexers are able to select two bits of either HIGH or LOW data or control from up to four sources, in one package. The '09 is the logical implementation of two-pole, four-position switch, with the position of the switch being set by the logic levels supplied to the two select inputs. Both assertion and negation outputs are provided for both multiplexers. The logic equations for the outputs are shown below:

$$Z_a = I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0$$
$$Z_b = I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0$$

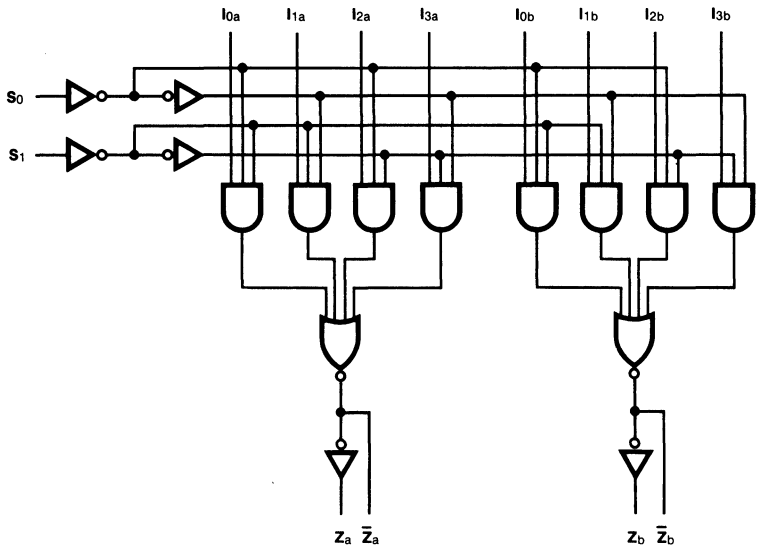
The '09 is frequently used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the select inputs. A less obvious application is as a function generator. The '09 can generate two functions of three variables. This is useful for implementing random gating functions.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)				OUTPUTS (a or b)	
S_0	S_1	I_0	I_1	I_2	I_3	Z	$\overline{Z}$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current			-10	-40	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current		44		11.5	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load definitions)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C_L = 15pF		C_L = 15pF			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_0 to Z_a		29 27		70 60	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay S_0 to $\overline{Z}_a$		21 21		55 50	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay I_{0a} to $\overline{Z}_a$		12 13		40 60	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay I_{0a} to Z_a		20 21		70 65	ns	Figs. 3-1, 3-5

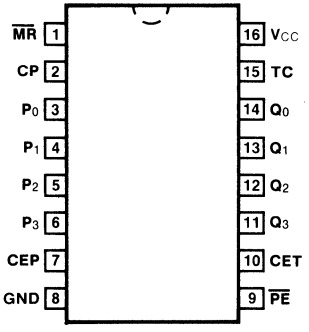
9310 • 9316
93L10 • 93L16
93S10 • 93S16

BCD DECADE COUNTER/ 4-BIT BINARY COUNTER

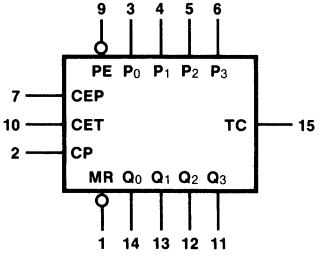
DESCRIPTION — The '10 is a high speed synchronous BCD decade counter and the '16 is a high speed synchronous 4-bit binary counter. They are synchronously presetable, multifunctional MSI building blocks useful in a large number of counting, digital integration and conversion applications. Several states of synchronous operation are obtainable with no external gating packages required through an internal carry lookahead counting technique.

- **SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **DECODED TERMINAL COUNT**
- **BUILT-IN CARRY CIRCUITRY**
- **EASY INTERFACING WITH DTL, LPDTL, AND TTL FAMILIES**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

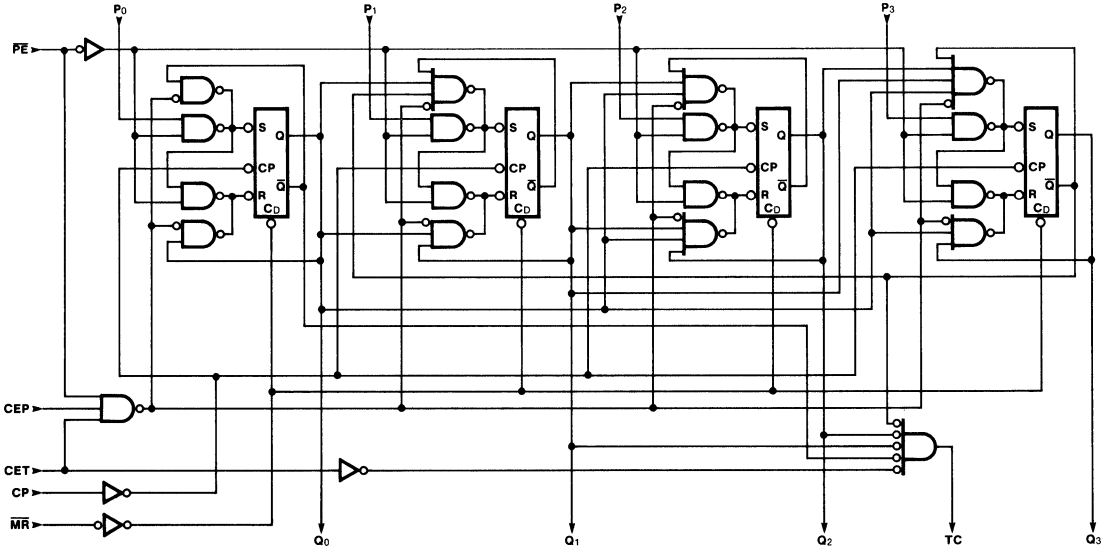
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9310PC, 9316PC 93L10PC, 93L16PC 93S10PC, 93S16PC		9B
Ceramic DIP (D)	A	9310DC, 9316DC 93L10DC, 93L16DC 93S10DC, 93S16DC	9310DM, 9316DM 93L10DM, 93L16DM 93S10DM, 93S16DM	6B
Flatpak (F)	A	9310FC, 9316FC 93L10FC, 93L16FC 93S10FC, 93S16FC	9310FM, 9316FM 93L10FM, 93L16FM 93S10FM, 93S16FM	4L

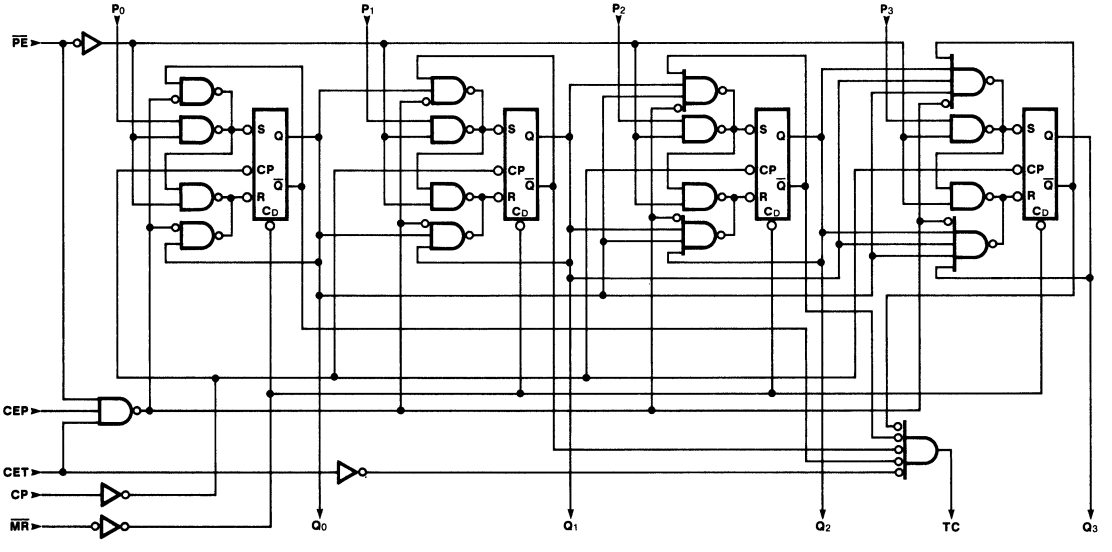
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW	93S (U.L.) HIGH/LOW
CEP	Count Enable Parallel Input	1.0/1.0	0.5/0.25	2.5/2.5
CET	Count Enable Trickle Input	2.0/2.0	1.0/0.5	3.1/3.1
CP	Clock Pulse Input (Active Rising Edge)	2.0/2.0	1.0/0.5	3.1/3.1
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	0.5/0.25	1.25/1.25
$P_0 - P_3$	Parallel Data Inputs	0.67/0.67	0.33/0.17	1.25/1.25
$\overline{PE}$	Parallel Enable Input (Active LOW)	2.0/2.0	1.0/0.5	2.5/2.5
$Q_0 - Q_3$	Flip-flop Outputs	16/8.0	10/5.0 (3.0)	20/10
TC	Terminal Count Output	20/10	10/5.0 (3.0)	25/12.5

LOGIC DIAGRAMS
'10, 'L10

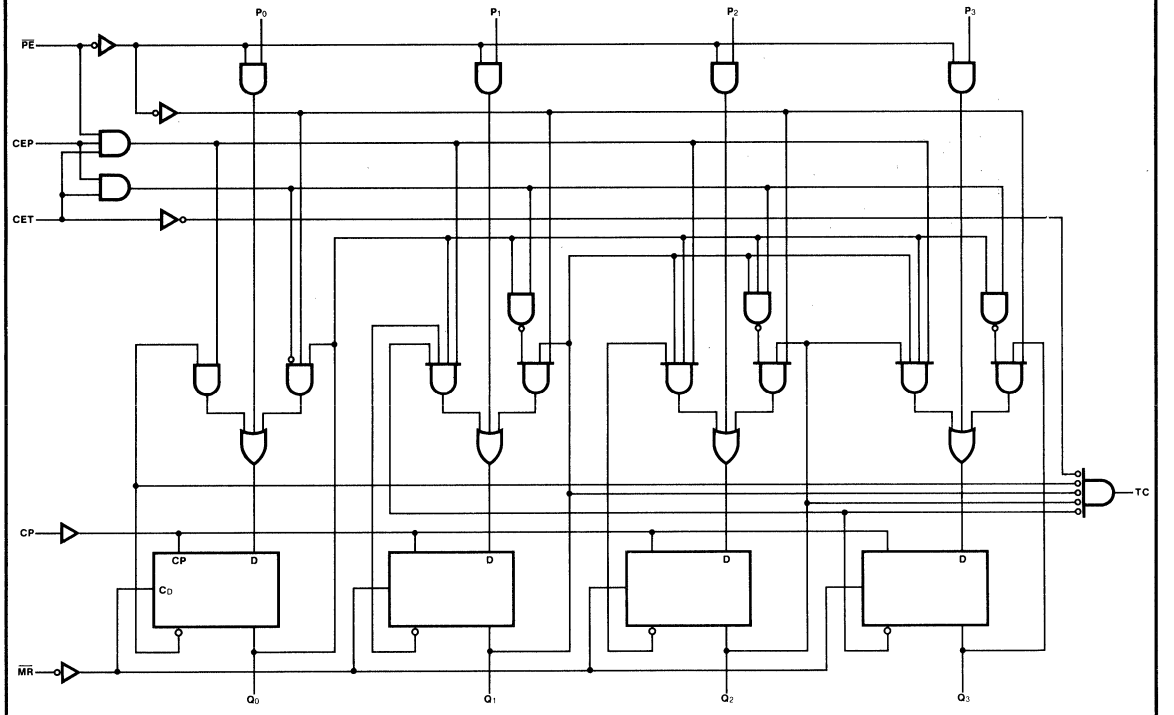


'16, 'L16

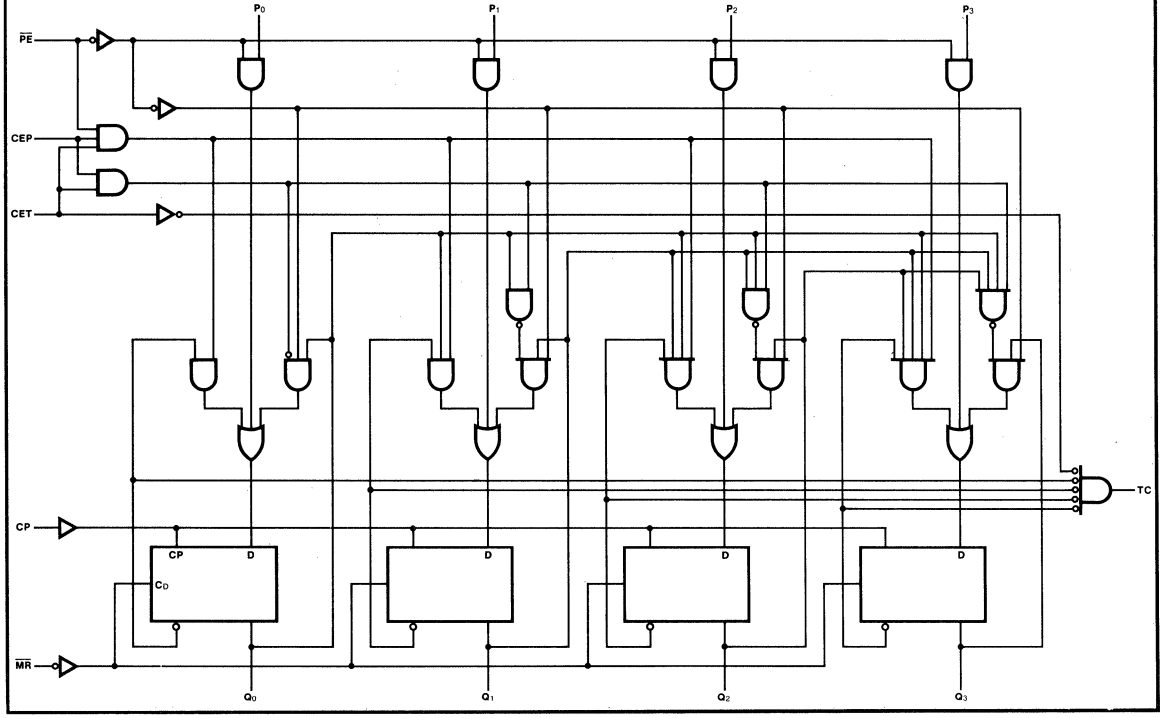


LOGIC DIAGRAMS

'S16



'S10



FUNCTIONAL DESCRIPTION — The '10 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it increments to state 0 (LLLL). The '16 counts modulo-16 in binary sequence. From state 15 (HHHH) it increments to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset, parallel load, count-up and hold. Four control inputs — Master Reset ($\overline{MR}$) Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The TTL and LP-TTL versions ('10, '16, 'L10 and 'L16 as opposed to the 'S10 and 'S16) contain masterslave flip-flops which are "next-state catching" because of the JK feedback. This means that when CP is LOW, information that would change the state of a flip-flop, whether from the counting logic or the parallel entry logic if either mode is momentarily enabled, enters the master and is locked in. Thus to avoid inadvertently changing the state of a master latch, and the subsequent transfer of the erroneous information to the slave when the clock rises, it is necessary to insure that neither the counting mode, nor the parallel entry mode is momentarily enabled while CP is LOW. The S-TTL versions ('S10 and 'S16) use D-type edge-triggered flip-flops and changing the $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in its maximum count state (9 for the decade counters, 15 for the binary counters — fully decoded in both types). To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. These two schemes are shown in *Figures a and b*. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the state diagrams.

Multistage Counting — The '10/'16 counters may be cascaded to provide multistage synchronous counting. Two methods commonly used to cascade these counters are shown in *Figures a and b*.

In multistage counting, all less significant stages must be at their terminal count before the next more significant counter is enabled. The '10/'16 internally decodes the terminal count condition and "ANDs" it with the CET input to generate the terminal count (TC) output. This arrangement allows one to perform series enabling by connecting the TC output (enable signal) to the CET input of the following stage, *Figure a*. The setup requires very few interconnections, but has the following drawback: since it takes time for the enable to ripple through the counter stages, there is a reduction in maximum counting speed. To increase the counting rate, it is necessary to decrease the propagation delay of the TC signal, which is done in the second method.

The scheme illustrated in *Figure b* permits multistage counting, limited by the fan-out of the terminal count. The CEP input of the '10/'16 is internally "ANDed" with the CET input and as a result, both must be HIGH for the counter to be enabled. The CET inputs are connected as before except for the second stage. There the CET input is left floating and is therefore HIGH. Also, all CEP inputs are connected to the terminal output of the first stage. The advantage of this method is best seen by assuming all stages except the second and last are in their terminal condition. As the second stage advances to its terminal count, an enable is allowed to trickle down to the last counter stage, but has the full cycle time of the first counter to reach it. Then as the TC of the first stage goes active (HIGH), all CEP inputs are activated, allowing all stages to count on the next clock.

MODE SELECT TABLE

INPUTS					RESPONSE
$\overline{MR}$	$\overline{PE}$	CEP	CET	CP	
L	X	X	X	X	Clear; All Outputs LOW
H	L	X	X	↑	Parallel Load; $P_n \rightarrow Q_n$
H	H	L	X	X	Hold
H	H	X	L	X	Hold; TC = LOW
H	H	H	H	↑	Count Up

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC EQUATIONS

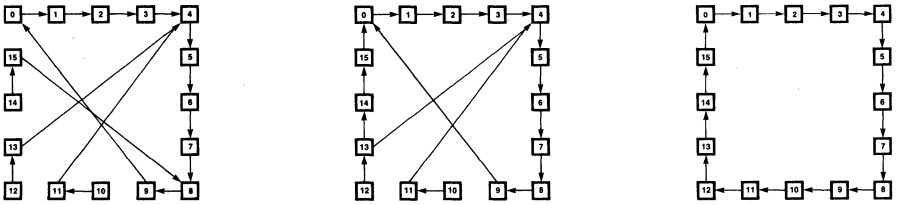
Count Enable = MR • PE • CEP • CET

Terminal Count = CET • Q_0 • Q_1 • Q_2 • Q_3 ('16)

Terminal Count = CET • Q_0 • $\overline{Q_1}$ • $\overline{Q_2}$ • Q_3 ('10)

STATE DIAGRAMS

'S10 '10, 'L10 '16, 'S16, 'L16



NOTE: The '20 can be preset to any state, but will not count beyond 9. If preset to state 10,11,12,13,14 or 15, it will return to its normal sequence within two clock pulses.

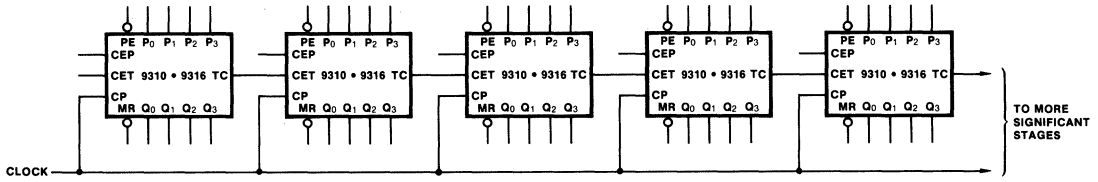


Fig. a Synchronous Multistage Counting Scheme (Slow)

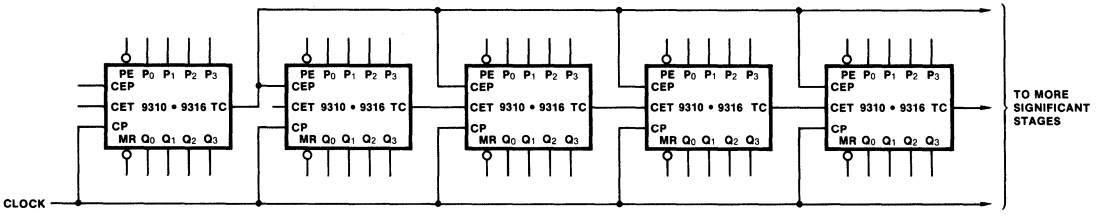


Fig. b Synchronous Multistage Counting Scheme (Fast)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		93S		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current	-20	-80	-2.5	-25	-40	-100	mA	V_{CC} = Max
I_{CC}	Power Supply Current		92		27.5		127	mA	V_{CC} = Max, $\overline{MR}$ = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		93L		93S		UNITS	CONDITIONS
		C_L = 15 pF		C_L = 15 pF		C_L = 15 pF			
		Min	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	30		13		70		MHz	
t_{PLH} t_{PHL}	Propagation Delay CP to Q		20 23		32 39		9.0 13	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to TC		35 22		66 30		18 12	ns	
t_{PLH} t_{PHL}	Propagation Delay CET to TC		19 19		35 30		10 10	ns	Figs. 3-1, 3-5
t_{PHL}	Propagation Delay $\overline{MR}$ to Q		45		62		20	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	93XX		93L		93S		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n to CP	30 30		75 75		8.0 5.0		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n to CP	0 0		10 10		0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{PE}$ to CP	Note 2 30		Note 2 53		10 5.0		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{PE}$ to CP	-7.0 Note 2		7.0 Note 2		0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW CEP or CET to CP	22 Note 1		26 Note 1		9.0 7.5		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW CEP or CET to CP	Note 1 0		Note 1 10		0 0		ns	
t_w (H) t_w (L)	CP Pulse Width	17 17		25 25		6.5 7.0		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	30		65		14		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	15		55		5.5		ns	Fig. 3-16

NOTES:
(1) The Setup Time "t_s (L)" and Hold Time "t_h (H)" between the Count Enable (CEP and CET) and the Clock (CP) indicate that the HIGH-to-LOW transition of the CEP and CET must occur only while the Clock is HIGH for conventional operation.
(2) The Setup Time "t_s (H)" and Hold Time "t_h (L)" between the Parallel Enable ($\overline{PE}$) and Clock (CP) indicate that the LOW-to-HIGH transition of the $\overline{PE}$ must occur only while the Clock is HIGH for conventional operation.

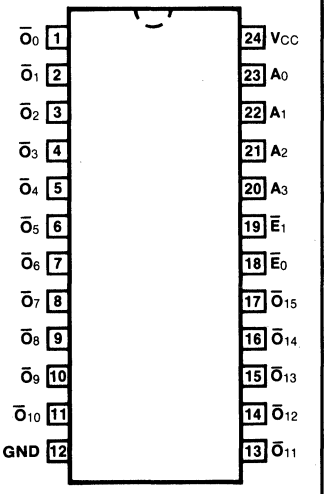
6

9311
93L11
1-OF-16 DECODER/DEMULTIPLEXER

DESCRIPTION — The '11 is a multipurpose decoder designed to accept four inputs and provide 16 mutually exclusive outputs. The 9311 is a faster replacement for the 74154.

- **MUTUALLY EXCLUSIVE OUTPUTS**
- **HIGH CAPACITIVE DRIVE CAPABILITY**
- **DEMULTIPLEXING CAPABILITY**
- **TYPICAL POWER DISSIPATION OF 175 mW FOR '11, 58 mW FOR 'L11**
- **2-INPUT ENABLE GATE**

CONNECTION DIAGRAM
PINOUT A



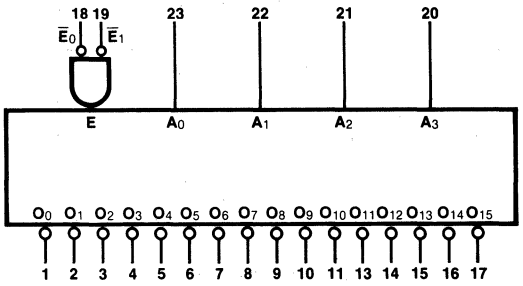
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9311PC, 93L11PC		9N
Ceramic DIP (D)	A	9311DC, 93L11DC	9311DM, 93L11DM	6N
Flatpak (F)	A	9311FC, 93L11FC	9311FM, 93L11FM	4M

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	1.0/1.0	0.5/0.25
$\overline{E}_0$, $\overline{E}_1$	AND Enable Inputs (Active LOW)	1.0/1.0	0.5/0.25
$\overline{O}_0 - \overline{O}_{15}$	Decoder Outputs (Active LOW)	20/10	10/5.0 (3.0)

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

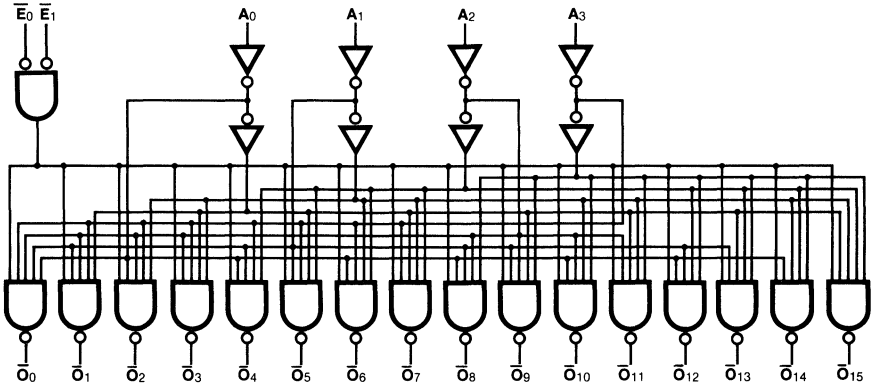
FUNCTIONAL DESCRIPTION — The '11 decoder accepts four inputs and provides 16 mutually exclusive active LOW outputs, as shown by the logic symbol. The active LOW outputs facilitate addressing other MSI units with active LOW enable. The '11 can demultiplex data by routing it from one input to one of 16 possible decoder outputs. The desired output is addressed and the data is applied to one of the enable inputs. Providing that the other enable is LOW, the addressed output will follow the state of the applied data.

TRUTH TABLE

INPUTS						OUTPUTS													
$\overline{E}_0$	$\overline{E}_1$	A_0	A_1	A_2	A_3	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$	$\overline{O}_8$	$\overline{O}_9$	$\overline{O}_{10}$	$\overline{O}_{11}$	$\overline{O}_{12}$	$\overline{O}_{13}$	$\overline{O}_{14}$	$\overline{O}_{15}$
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

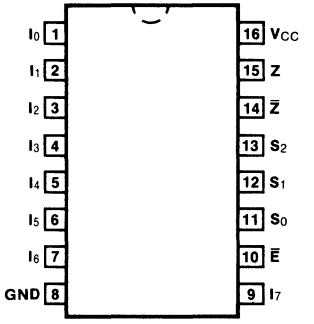
SYMBOL	PARAMETER		93XX Min	93XX Max	93L Min	93L Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	XM	-20	-55	-2.5	-25	mA	V_{CC} = Max, V_{OUT} = 0 V
		XC	-20	-57	-2.5	-25		
I_{CC}	Power Supply Current	XM		49		16.5	mA	V_{CC} = Max
		XC		56		16.5		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF, R_L = 400 Ω Min	93XX Max	93L C_L = 15 pF Min	93L Max	UNITS	CONDITIONS
t_{PLH}	Propagation Delay		31		75	ns	Figs. 3-1, 3-20
t_{PHL}	A_n to O_n		28		85		
t_{PLH}	Propagation Delay		23		60	ns	Figs. 3-1, 3-5
t_{PHL}	E_n to O_n		24		65		

9312
93L12
93S12
8-INPUT MULTIPLEXER

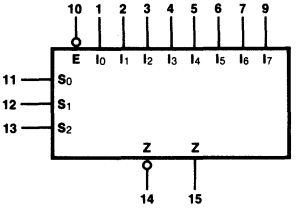
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '12 is a monolithic, high speed, 8-input digital multiplexer circuit. It provides, in one package, the ability to select one bit of data from up to eight sources. The '12 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9312PC, 93L12PC 93S12PC		9B
Ceramic DIP (D)	A	9312DC, 93L12DC 93S12DC	9312DM, 93L12DM 93S12DM	6B
Flatpak (F)	A	9312FC, 93L12FC 93S12FC	9312FM, 93L12FM 93S12FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93S (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
$S_0 - S_2$	Select Inputs	1.0/1.0	1.25/1.25	0.5/0.25
$\bar{E}$	Enable Input (Active LOW)	1.0/1.0	1.25/1.25	0.5/0.25
$I_0 - I_7$	Multiplexer Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Z	Multiplexer Output	20/10	25/12.5	10/5.0 (3.0)
$\bar{Z}$	Complementary Multiplexer Output	20/10	25/12.5	10/5.0 (3.0)

FUNCTIONAL DESCRIPTION — The '12 is a logical implementation of a single pole, eight position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Enable input ($\overline{E}$) is active LOW. When it is not activated the negation output is HIGH and the assertion output is LOW, regardless of all other inputs. The logic function provided at the output is:

$$Z = E \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2).$$

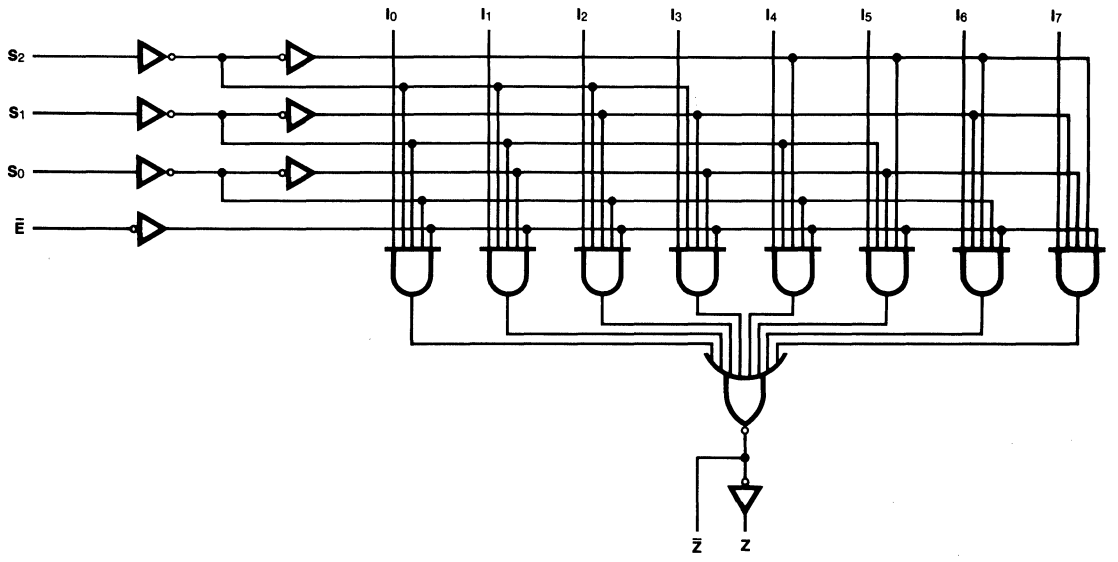
The '12 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the '12 can provide any logic function of four variables and its negation. Thus any number of random logic elements used to generate unusual truth tables can be replaced by one '12.

TRUTH TABLE

INPUTS												OUTPUTS	
$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93S		93L		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
I_{CC}	Power Supply Current		44		62		13.3	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF		93S C_L = 15 pF		93L C_L = 15 pF		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay		34		17		60	ns	Figs. 3-1, 3-5
t_{PHL}	S_0 to Z		34		18		75		
t_{PLH}	Propagation Delay		24		16		45	ns	Figs. 3-1, 3-4
t_{PHL}	S_0 to $\overline{Z}$		26		15		65		
t_{PLH}	Propagation Delay		30		13		50	ns	Figs. 3-1, 3-4
t_{PHL}	$\overline{E}$ to Z		30		16		70		
t_{PLH}	Propagation Delay		20		14		35	ns	Figs. 3-1, 3-5
t_{PHL}	$\overline{E}$ to $\overline{Z}$		23		11		60		
t_{PLH}	Propagation Delay		24		12		60	ns	Figs. 3-1, 3-5
t_{PHL}	I_n to Z		24		12		55		
t_{PLH}	Propagation Delay		14		8.0		45	ns	Figs. 3-1, 3-4
t_{PHL}	I_n to $\overline{Z}$		16		9.0		45		

9313

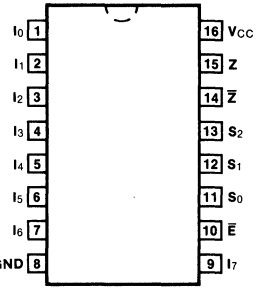
8-INPUT MULTIPLEXER

(With Open-Collector Output)

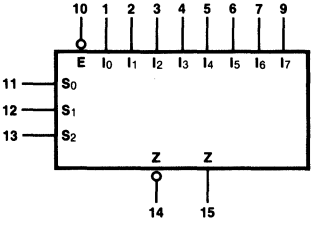
DESCRIPTION — The '13 is an 8-input multiplexer with open-collector output. It has the same pinning and logic configuration as the '12, but with an open-collector $\overline{Z}$ output which allows for easy expansion of input terms. The device can select one bit of data from up to eight sources. The '13 has an active LOW enable and internal select decoding.

- **PIN FOR PIN REPLACEMENT FOR THE SIGNETICS 8231**
- **SAME PINNING AND LOGIC CONFIGURATION AS THE 9312 BUT WITH OPEN-COLLECTOR OUTPUT**
- **OPEN-COLLECTOR OUTPUT $\overline{Z}$ FOR EASY EXPANSION OF INPUT TERMS (WIRED-OR APPLICATIONS)**
- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED Z OUTPUT**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9313PC		9B
Ceramic DIP (D)	A	9313DC	9313DM	6B
Flatpak (F)	A	9313FC	9313FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
$S_0 - S_2$	Select Inputs	1.0/1.0
$\overline{E}$	Enable Input (Active LOW)	1.0/1.0
$I_0 - I_7$	Multiplexer Inputs	1.0/1.0
Z	Multiplexer Output	20/10
$\overline{Z}$*	Complementary Multiplexer Output	OC**/10

*An external pull-up resistor is needed to provide HIGH level drive capability. This output will sink a maximum of 16 mA at V_{OUT} = 0.4 V.
**OC — Open Collector

FUNCTIONAL DESCRIPTION — The '13 is a logical implementation of a single pole, eight-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. An open-collector output $\overline{Z}$ is provided for easy expansion of input terms. Also a fully buffered Z output is available. The Enable Input ($\overline{E}$) is active LOW. When it is not activated the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

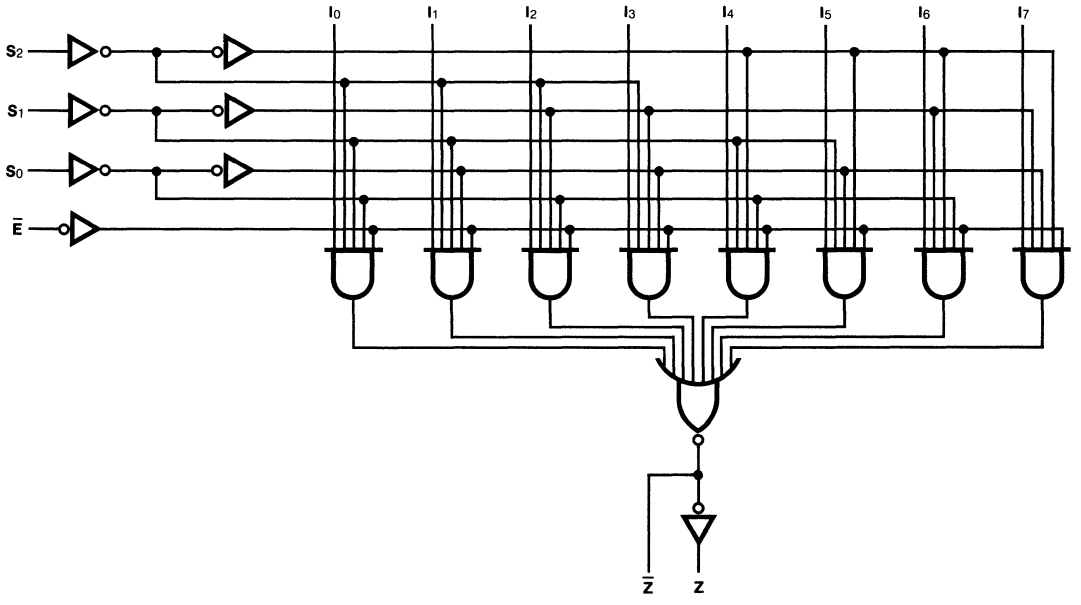
The '13 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the '13 can provide any logic functions of four variables and its negation.

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{E}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

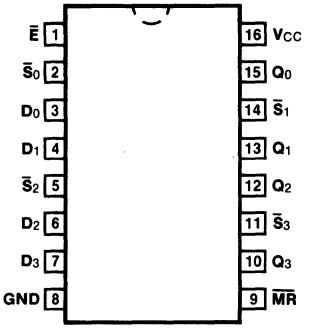
SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		Min	Max		
I_{OH}	Output HIGH Current, $\overline{Z}$		150	μA	V_{CC} = 4.5 V, V_{OUT} = 4.5 V, V_{IN} = 0.6 V on Data Input, V_{IN} ($\overline{E}$ & S_n Inputs) = V_{IL} or V_{IH} per Truth Table
I_{OS}	Output Short Circuit Current, Z	-20	-70	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current		47	mA	V_{CC} = Max, I_0 — I_7 = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		C_L = 15 pF			
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_0 to Z		34 34	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay S_0 to $\overline{Z}$		29 28	ns	Figs. 3-2, 3-20 R_L = 400 Ω
t_{PLH} t_{PHL}	Propagation Delay I_0 to Z		30 30	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay I_0 to $\overline{Z}$		26 24	ns	Figs. 3-2, 3-4 R_L = 400 Ω
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z		34 36	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$		27 29	ns	Figs. 3-2, 3-5 R_L = 400 Ω

9314
93L14
QUAD LATCH

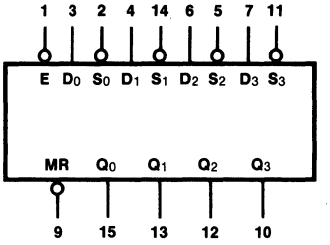
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '14 is a multifunctional 4-bit latch designed for general purpose storage applications in high speed digital systems. All outputs have active pull-up circuitry to provide high capacitance drive and to provide low impedance in both logic states for good noise immunity.

- **CAN BE USED AS SINGLE INPUT D LATCHES OR SET/RESET LATCHES**
- **ACTIVE LOW ENABLE GATE INPUT**
- **OVERRIDING MASTER RESET**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	9314PC, 93L14PC		9B
Ceramic DIP (D)	A	9314DC, 93L14DC	9314DM, 93L14DM	6B
Flatpak (F)	A	9314FC, 93L14FC	9314FM, 93L14FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
$\overline{E}$	Enable Input (Active LOW)	1.0/1.0	0.5/0.25
$D_0 - D_3$	Data Inputs	1.5/1.5	0.75/0.375
$\overline{S}_0 - \overline{S}_3$	Set Inputs (Active LOW)	1.0/1.0	0.5/0.25
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0	0.5/0.25
$Q_0 - Q_3$	Latch Outputs	20/10	10/5.0 (3.0)

FUNCTIONAL DESCRIPTION — The '14 consists of four latches with a common active LOW Enable input and active LOW Master Reset input. When the Enable goes HIGH, data present in the latches is stored and the state of the latch is no longer affected by the $\overline{S}_n$ and D_n inputs. The Master Reset when activated overrides all other input conditions forcing all latch outputs LOW. Each of the four latches can be operated in one of two modes:

D-TYPE LATCH — For D-type operation the $\overline{S}$ input of a latch is held LOW. While the common Enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the Enable goes HIGH.

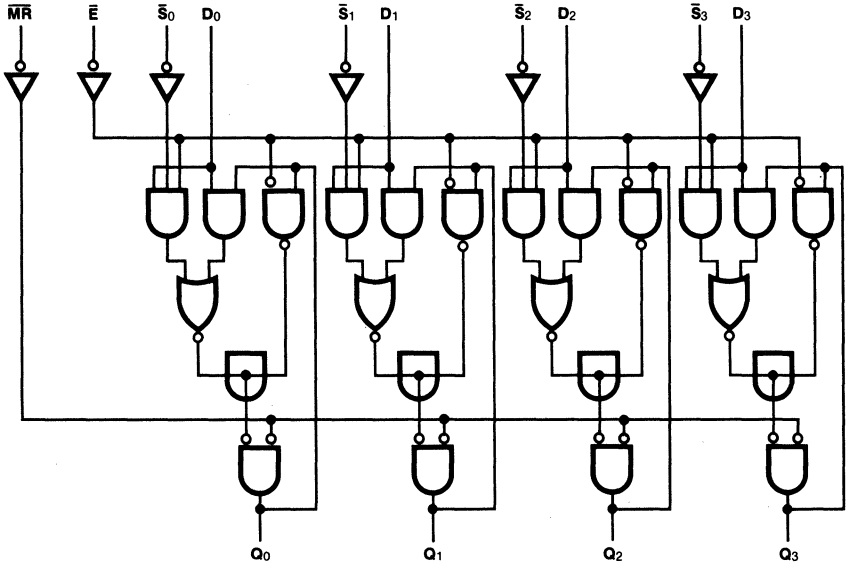
SET/RESET LATCH — During set/reset operation when the common Enable is LOW a latch is reset by a LOW on the D, input, and can be set by a LOW on the $\overline{S}$ input if the D input is HIGH. It both $\overline{S}$ and D inputs are LOW, the D input will dominate and the latch will be reset. When the Enable goes HIGH, the latch remains in the last state prior to disablement. The two modes of latch operation are shown in the Truth Table.

TRUTH TABLE

$\overline{MR}$	$\overline{E}$	D	$\overline{S}$	Q_n	OPERATION
H	L	L	L	L	D MODE
H	L	H	L	H	
H	H	X	X	Q_{n-1}	
H	L	L	L	L	R/S MODE
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{n-1}	
H	H	X	X	Q_{n-1}	
L	X	X	X	L	RESET

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Q_{n-1} = Previous Output State
Q_n = Present Output State

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		55		16.5	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C_L = 15 pF		C_L = 15 pF			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n		24 24		45 36	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		12 24		30 30	ns	Figs. 3-1, 3-5
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n		18		30	ns	Figs. 3-1, 3-16
t_{PHL}	Propagation Delay $\overline{S}_n$ to Q_n		24		33	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to $\overline{E}$	5.0 18		10 20		ns	Fig. 3-13
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to $\overline{E}$	0 5.0		0 10		ns	
t_s (H)	Setup Time HIGH, D_n to $\overline{S}_n$	8.0		15		ns	Fig. 3-13
t_h (L)	Hold Time LOW, D_n to $\overline{S}_n$	8.0		5.0		ns	
t_w (L)	$\overline{E}$ Pulse Width LOW	18		30		ns	Fig. 3-9
t_w (L)	$\overline{MR}$ Pulse Width LOW	18		25		ns	Fig. 3-16
t_{rec}	Recovery Time, $\overline{MR}$ to $\overline{E}$	0		5.0		ns	Fig. 3-16

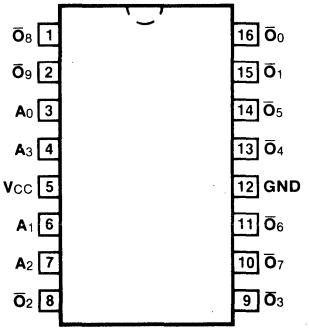
9315

1-OF-10 DECODER

DESCRIPTION — The '15 accepts 1248 binary coded decimal inputs and provides ten mutually exclusive outputs to directly control the ionizing potentials of many gas filled cold cathode indicator tubes. The '15 is a pin-for-pin equivalent to the 7441 and is similar in operation to the CμL9960 but can be driven from any TTL or DTL product.

- **STABLE HIGH VOLTAGE OUTPUT CHARACTERISTICS**
- **DIRECT DISPLAY DRIVE CAPABILITY**
- **BCD ACTIVE HIGH INPUTS**
- **BLANKING TEST MODE**
- **-55°C to +125°C TEMPERATURE CAPABILITY**

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

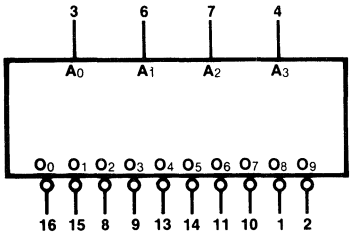
PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	9315PC		9B
Ceramic DIP (D)	A	9315DC	9315DM	6B
Flatpak (F)	A	9315FC	9315FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
A_0 — A_3	Address (Data) Inputs	0.13/0.94
$\overline{O}_0$ — $\overline{O}_9$	Decoder Outputs (Active LOW)	OC*/7.0 mA

*OC — Open Collector

LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 12

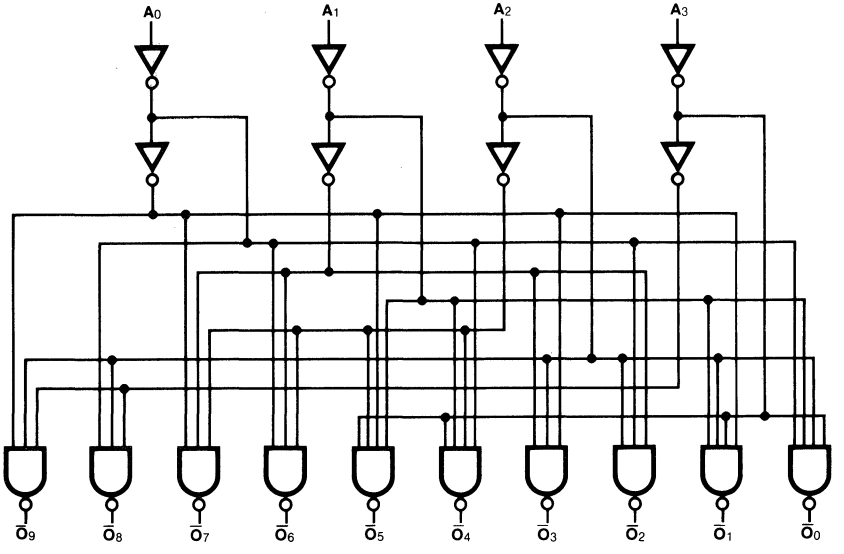
FUNCTIONAL DESCRIPTION — The 1-of-10 decoder/driver accepts BCD inputs from all TTL circuits and produces the correct output selection to directly drive gas filled cold cathode indicator tubes. The outputs are selected as shown in the Truth Table. It is capable of driving all known available cold cathode indicator tubes having 7.0 mA or less cathode current. Unused input codes 12 and 13 cause all the outputs to remain HIGH; no cathode will be selected. This results in the indicator tube being blanked. Using this feature for blanking may cause a slight glow to appear in the tube.

TRUTH TABLE

	INPUTS				OUTPUTS									
	A_0	A_1	A_2	A_3	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$	$\overline{O}_8$	$\overline{O}_9$
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	H	L	L	L	H	L	H	H	H	H	H	H	H	H
2	L	H	L	L	H	H	L	H	H	H	H	H	H	H
3	H	H	L	L	H	H	H	L	H	H	H	H	H	H
4	L	L	H	L	H	H	H	H	L	H	H	H	H	H
5	H	L	H	L	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	H	H	H	L	H	H	H	H	H	H	H	L	H	H
8	L	L	L	H	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
10	L	H	L	H	H	H	L	H	H	H	H	H	L	H
11	H	H	L	H	H	H	H	L	H	H	H	H	H	L
12	L	L	H	H	H	H	H	H	H	H	H	H	H	H
13	H	L	H	H	H	H	H	H	H	H	H	H	H	H
14	L	H	H	H	H	H	H	H	H	H	L	H	H	H
15	H	H	H	H	H	H	H	H	H	H	H	L	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

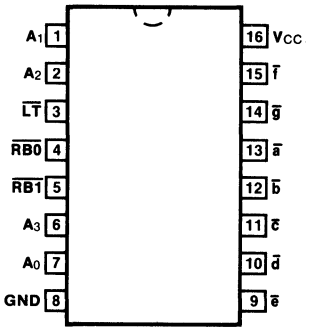
SYMBOL	PARAMETER		93XX Min	93XX Max	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage		70		V	V_{CC} = Max, Force 2.0 mA into HIGH Output
V_{OL}	Output LOW Voltage	XM		2.5	V	V_{CC} = Min, I_{OL} = 7.0 mA Inputs at Threshold Voltages, (V_{IL} or V_{IH}) as per Truth Table
		XC		3.0		
V_{IH}	Input HIGH Voltage	XM	1.9		V	Guaranteed Input HIGH Threshold Voltage
		XC	2.0			
V_{IL}	Input LOW Voltage	XM		1.1	V	Guaranteed Input LOW Threshold Voltage
		XC		0.85		
I_{OH}	Output HIGH Current	XM		20	μA	V_{CC} = Max, V_{OUT} = 55 V Inputs at Threshold Voltages, (V_{IL} = Gnd, V_{IH} = 4.5 V), as per Truth Table
		XC		40		
I_{IH}	Input HIGH Current	XM		2.0	μA	V_{CC} = Max, V_{IN} = 4.5 V Other Inputs Open
		XC		5.0		
I_{IL}	Input LOW Current			-1.5	mA	V_{CC} = Max, V_{IN} = 0.4 V Other Inputs Open
I_{CC}	Power Supply Current	XM		29	mA	V_{CC} = 5.0 V, No Connection to Input or Output Pins
		XC		31		

9317B
9317C
7-SEGMENT DECODER/DRIVER

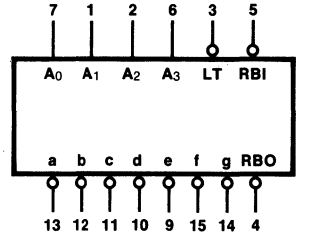
DESCRIPTION — The '17 is a seven segment decoder/driver designed to accept four inputs in 8421 BCD code and provide the appropriate outputs to drive a 7-segment numerical display. The decoder can be used to directly drive 7-segment incandescent lamp displays and light emitting diode indicators (or indirectly drive neon, electro-luminescent, numeric displays). The '17 is available in two output current and latch voltage versions, the '17B and C.

- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING AND/OR TRAILING-EDGE ZEROES**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **LAMP TEST FACILITY/BLANKING INPUT**
- **CODES IN EXCESS OF BINARY 9 DISABLE OUTPUTS**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9317PC		9B
Ceramic DIP (D)	A	9317DC	9317DM	7B
Flatpak (F)	A	9317FC	9317FM	4L

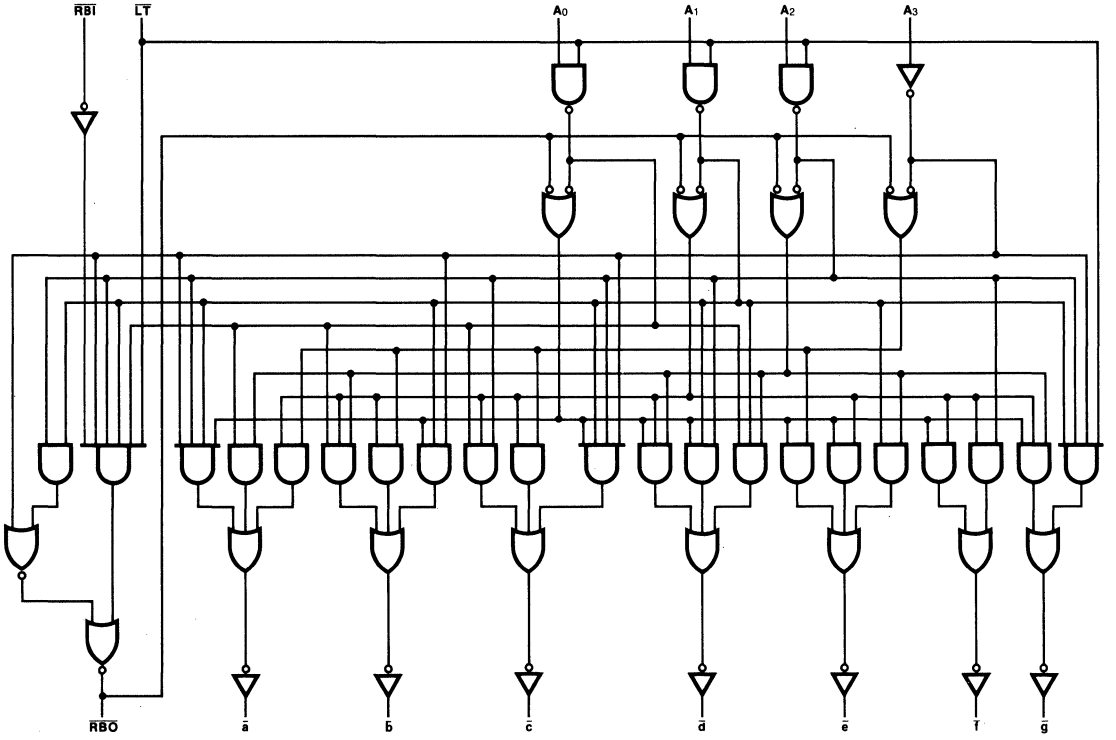
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	1.0/1.0
$\overline{LT}$	Lamp Test Input (Active LOW)	5.0/4.0
$\overline{RBI}$	Ripple Blanking Input (Active LOW)	1.0/0.5
$\overline{RBO}$	Ripple Blanking Output (Active LOW)	1.5/1.5
$\overline{a} - \overline{g}$	Outputs	See Options

OPTIONS

PARAMETER	9317B	9317C
Latch Voltage	20 V	30 V
Output Current (Pins 9 through 15)	40 mA	20 mA

LOGIC DIAGRAM



TRUTH TABLE

INPUTS						OUTPUTS								DECIMAL OR FUNCTION
$\overline{LT}$	$\overline{RBI}$	A_0	A_1	A_2	A_3	$\bar{a}$	$\bar{b}$	$\bar{c}$	$\bar{d}$	$\bar{e}$	$\bar{f}$	$\bar{g}$	$\overline{RBO}$	
L	X	X	X	X	X	L	L	L	L	L	L	L	H	
H	L	L	L	L	L	H	H	H	H	H	H	H	L	0
H	H	L	L	L	L	L	L	L	L	L	L	H	H	0
H	X	H	L	L	L	H	H	H	H	L	L	H	H	1
H	X	L	H	L	L	L	L	H	L	L	H	L	H	2
H	X	H	H	L	L	L	L	L	L	H	H	L	H	3
H	X	L	L	H	L	H	L	L	H	H	L	L	H	4
H	X	H	L	H	L	L	H	L	L	H	L	L	H	5
H	X	L	H	H	L	H	H	L	L	L	L	L	H	6
H	X	H	H	H	L	L	L	L	H	H	H	H	H	7
H	X	L	L	L	H	L	L	L	L	L	L	L	H	8
H	X	H	L	L	H	L	L	L	H	H	L	L	H	9
H	X	L	H	L	H	H	H	H	H	H	H	H	L	10
H	X	H	H	L	H	H	H	H	H	H	H	H	L	11
H	X	L	L	H	H	H	H	H	H	H	H	H	L	12
H	X	H	L	H	H	H	H	H	H	H	H	H	L	13
H	X	L	H	H	H	H	H	H	H	H	H	H	L	14
H	X	H	H	H	H	H	H	H	H	H	H	H	L	15

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

FUNCTIONAL DESCRIPTION — The '17 7-segment decoder/driver accepts a 4-bit BCD 8421 code input and produces the appropriate outputs for selection of segments in a seven segment matrix display used for representing the decimal numbers 0 — 9. The seven outputs ($\overline{a}$ — $\overline{g}$) of the decoder select the corresponding segments in the matrix shown in *Figure a*. The numeric designations chosen to represent the decimal numbers are shown in *Figure c*. Code configurations in excess of binary nine disable the outputs.

The decoder has active LOW outputs so that it may be used directly to drive incandescent displays or light emitting diode indicators. The device has provision for automatic blanking of the leading and/or trailing-edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading-edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and, since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar precedure for the fractional part of a display will provide automatic suppression of trailing-edge zeroes.

The decoder has an active LOW input Lamp Test which overrides all other input combinations and allows checking on possible display malfunctions. The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL gates. Forcing the $\overline{RBO}$ LOW will blank the display, regardless of the $\overline{LT}$ or A_n inputs.

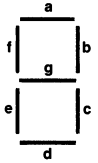


Fig. a Segment Designation

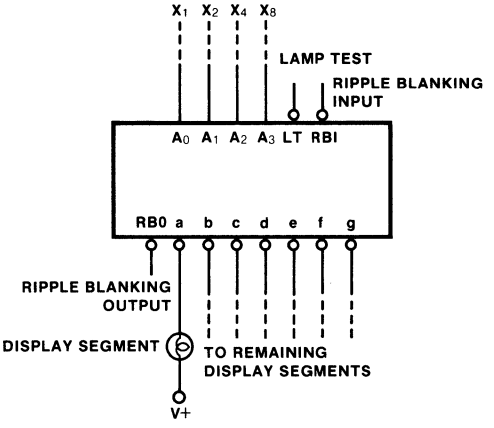


Fig. b Seven segment Decoder Driving Incandescent Lamp Display

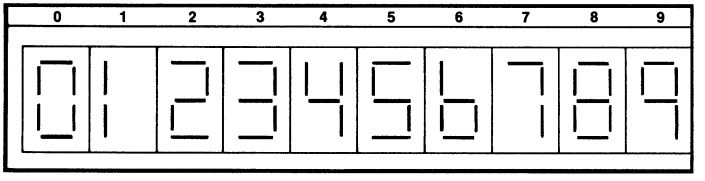


Fig. c Numerical Designations

DC AND AC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE: V_{CC} = +5.0 V ±5%

SYMBOL	PARAMETER		0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage on $\overline{RBO}$ Only		3.0		3.0		3.0		V	V_{CC} = 4.75 V I_{OH} = -70 μA Pin 5 = V_{IH} Pins 1,2,6,7=0V
V_{OL}	Output LOW Voltage on $\overline{RBO}$ Only			0.45		0.45		0.45	V	V_{CC} = 5.25 V I_{OL} = 2.75 mA Inputs at V_{IH} or V_{OL} per Truth Table
				0.45		0.45		0.45		V_{CC} = 4.75 V I_{OL} = 2.4 mA Inputs at V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	9317B		0.9		0.9		0.9	V	V_{CC} = 4.75 I_{OL} = 40 mA Pin 3 = 0 V
		9317C		0.45		0.45		0.45		V_{CC} = 4.75 V I_{OL} = 20 mA Pin 3 = 0 V
V_{LATCH}	Output Latch Voltage	9317B	20		20		20		V	I_{OL} = 10 mA Inputs = Open
		9317C	30		30		30			
V_{IH}	Input HIGH Voltage		2.0		2.0		2.0		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage			0.85		0.85		0.85	V	Guaranteed Input LOW Threshold
I_{OH}	Output HIGH Current					200		250	μA	V_{CC} = 5.25 V V_{CEX} = 30 V ('17C) 20 V ('17B) Inputs at V_{IH} or V_{IL} per Truth Table
t_{PLH} t_{PHL}	Propagation Delay					500 500			ns	Fig. 3-20

DC AND AC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE: V_{CC} = +5.0 V ±10%

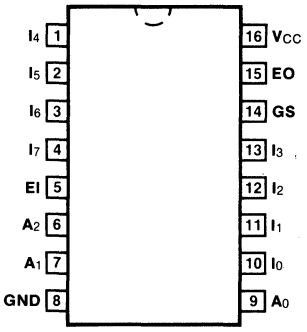
SYMBOL	PARAMETER		-55°C Min	-55°C Max	25°C Min	25°C Max	125°C Min	125°C Max	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage on $\overline{RBO}$ Only		3.0		3.0		3.0		V	V_{CC} = 4.5 V I_{OH} = -70 μA Pin 5 = V_{IH} Pins 1,2,6,7 = 0 V
V_{OL}	Output LOW Voltage on $\overline{RBO}$ Only			0.4		0.4		0.4	V	V_{CC} = 5.5 V I_{OL} = 3.1 mA Inputs at V_{IH} or V_{IL} per Truth Table
				0.4		0.4		0.4		V_{CC} = 4.5 V I_{OL} = 2.4 mA Inputs at V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	9317B		0.8		0.8		0.8	V	V_{CC} = 4.5 V I_{OL} = 40 mA Pin 3 = 0 V
		9317C		0.4		0.4		0.4		V_{CC} = 4.5 V I_{OL} = 20 mA Pin 3 = 0 V
V_{LATCH}	Output Latch Voltage	9317B 9317C	20 30		20 30		20 30		V	I_{OUT} = 10 mA Inputs = Open
V_{IH}	Input HIGH Voltage		2.1		1.9		1.7		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage			1.4		1.1		0.8	V	Guaranteed Input LOW Threshold
I_{OH}	Output HIGH Current					200		250	μA	V_{CC} = 5.5 V V_{CEX} = 30 V ('17C) 20 V ('17B) Inputs at V_{IH} or V_{IL} per Truth Table
t_{PLH} t_{PHL}	Propagation Delay					500 500			ns	Fig. 3-20

9318
93L18
8-INPUT PRIORITY ENCODER

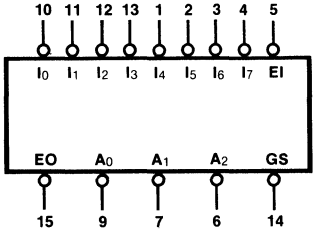
DESCRIPTION — The '18 multipurpose encoders are designed to accept eight inputs and produce a binary weighted code of the highest order input.

- **MULTIFUNCTION CAPABILITY**
  - **CODE CONVERSIONS**
  - **MULTI-CHANNEL D/A CONVERTER**
  - **DECIMAL TO BCD CONVERTER**
- **CASCADING FOR PRIORITY ENCODING OF N BITS**
- **INPUT ENABLE CAPABILITY**
- **PRIORITY ENCODING — AUTOMATIC SELECTION OF HIGHEST PRIORITY INPUT LINE**
- **OUTPUT ENABLE — ACTIVE LOW WHEN ALL INPUTS HIGH**
- **GROUP SIGNAL OUTPUT — ACTIVE WHEN ANY INPUT IS LOW**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

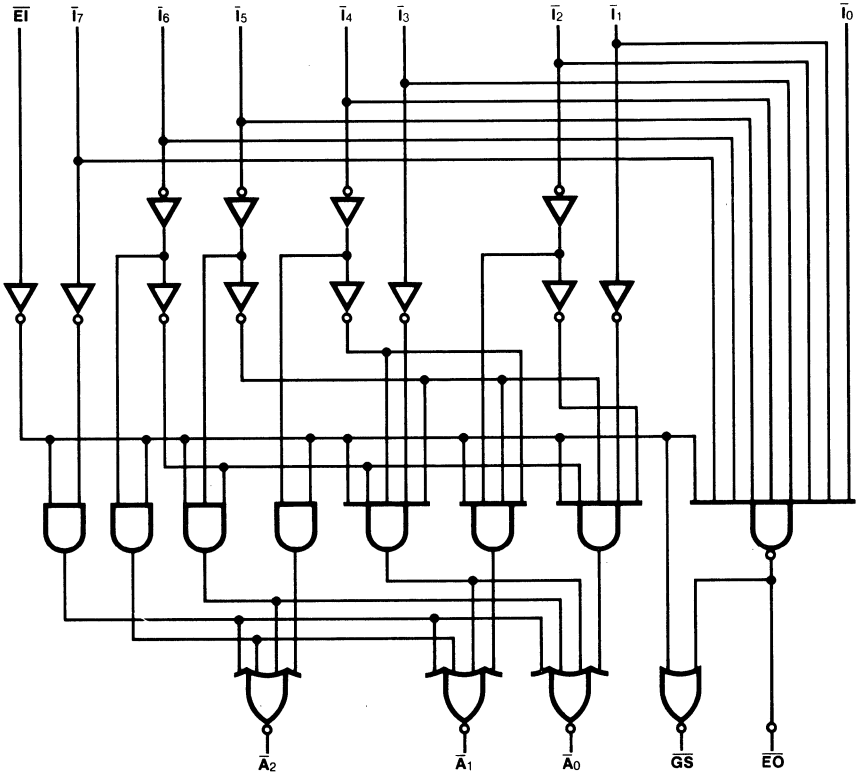
PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9318PC, 93L18PC		9B
Ceramic DIP (D)	A	9318DC, 93L18DC	9318DM, 93L18DM	6B
Flatpak (F)	A	9318FC, 93L18FC	9318FM, 93L18FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
$\overline{I_0}$	Priority Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{I_1} - \overline{I_7}$	Priority Inputs (Active LOW)	2.0/2.0	1.0/0.5
$\overline{EI}$	Enable Input (Active LOW)	2.0/2.0	1.0/0.5
$\overline{EO}$	Enable Output (Active LOW)	20/10	10/5.0 (3.0)
$\overline{GS}$	Group Select Output (Active LOW)	20/10	10/5.0 (3.0)
$\overline{A_0} - \overline{A_2}$	Address Outputs (Active LOW)	20/10	10/5.0 (3.0)

FUNCTIONAL DESCRIPTION — The '18 8-input priority encoder accepts data from eight active LOW inputs and provides a binary representation on the three active LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority. A HIGH on the Enable Input ($\overline{EI}$) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs. A Group Signal output ($\overline{GS}$) and Enable Output ($\overline{EO}$) are provided with the three data outputs. The $\overline{GS}$ is active LOW when any input is LOW; this indicates when any input is active. The $\overline{EO}$ is active LOW when all inputs are HIGH. Using the output enable along with the input enable allows priority encoding of N input signals. Both $\overline{EO}$ and $\overline{GS}$ are in the inactive HIGH state when the input enable is HIGH.

LOGIC DIAGRAM



TRUTH TABLE

INPUTS									OUTPUTS				
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	$\overline{GS}$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{IH}	Input HIGH Current $\overline{I}_0$ - $\overline{I}_7$, $\overline{EI}$		1.0			mA	V_{CC} = Max, V_{IN} = 5.5 V
I_{OS}	Output Short Circuit Current	-20	-70			mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current		77		22	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

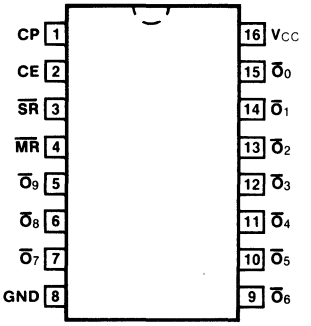
SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C_L = 15 pF		C_L = 15 pF			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_n$ to $\overline{EO}$		10 18		18 50	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{EI}$ to $\overline{GS}$		14 16		20 28	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{EI}$ to $\overline{EO}$		14 22		20 36	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{EI}$ to $\overline{A}_n$		17 17		33 26	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_n$ to $\overline{GS}$		14 16		60 26	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_n$ to $\overline{A}_n$		21 21		36 36	ns	Figs. 3-1, 3-20

9319 • 9320
DECADE SEQUENCERS

DESCRIPTION — The '19 and '20 are high speed counters with ten decoded active LOW outputs. The '19 has standard TTL totem pole outputs, and the '20 has resistor pull-up outputs for wired-AND applications. The devices provide a 1-of-10 sequential output pattern by the application of ten pulses to the Clock input. Shorter sequences can be obtained by using external feedback, either hard-wired or programmable via multiplexing.

- **COMBINATION DECADE COUNTER AND 1-OF-10 DECODER**
- **GLITCHLESS, SEQUENTIAL 1-OF-10 OUTPUT PATTERN**
- **IDEAL FOR MULTIPHASE CLOCK GENERATION**
- **ANY SEQUENCE BETWEEN TWO AND TEN OBTAINABLE**
- **HIGH SPEED CLOCK INPUTS — TYPICALLY 50 MHz**
- **WIRED-AND CAPABILITY (9320 ONLY)**

CONNECTION DIAGRAM
PINOUT A



6

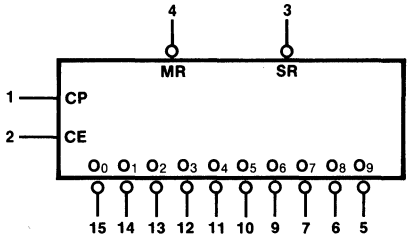
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	9319PC, 9320PC		9B
Ceramic DIP (D)	A	9319DC, 9320DC	9319DM, 9320DM	6B
Flatpak (F)	A	9319FC, 9320FC	9319FM, 9320FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

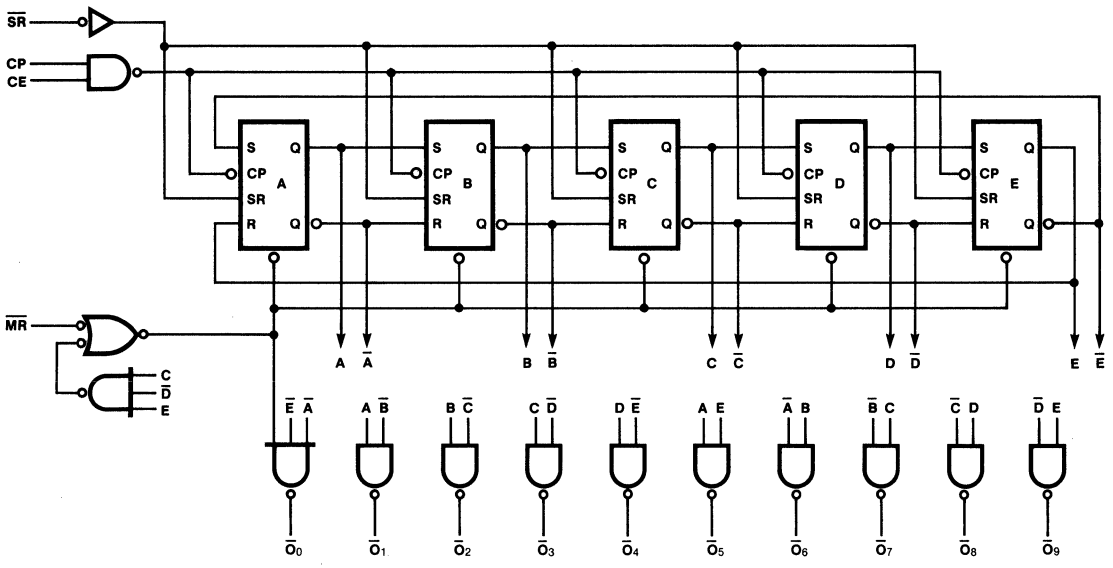
PIN NAMES	DESCRIPTION	9319 (U.L.) HIGH/LOW	9320 (U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	1.0/1.0
$\overline{CE}$	Clock Enable Input	1.0/1.0	1.0/1.0
$\overline{SR}$	Synchronous Reset Input (Active LOW)	1.0/1.0	1.0/1.0
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	1.0/1.0
$\overline{O}_0 - \overline{O}_9$	Decoded Outputs (Active LOW)	20/10	3.0/10

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS									
	$\overline{MR}$	$\overline{SR}$	CE	CP	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	•	•	•	•	$\overline{O}_7$	$\overline{O}_8$	$\overline{O}_9$
Initialize, Asynchronous Reset	L	X	X	X	H	H	H					H	H	H
	L→H	X	(quiescent)		L	H	H					H	H	H
Synchronous Reset	H	L	H	⌐	L	H	H					H	H	H
Hold	H	X	L	X	(No Change)									
Sequence/Count	H	H	H	⌐	L	H	H	•	•	•	•	H	H	H
	H	H	H	⌐	H	L	H	•	•	•	•	H	H	H
	H	H	H	⌐	H	H	L	•	•	•	•	H	H	H
	•	•	•	•	•	•	•					•	•	•
	•	•	•	•	•	•	•					•	•	•
	•	•	•	•	•	•	•					•	•	•
	•	•	•	•	•	•	•					•	•	•
	H	H	H	⌐	H	H	H	•	•	•	•	L	H	H
	H	H	H	⌐	H	H	H	•	•	•	•	H	L	H
	H	H	H	⌐	H	H	H	•	•	•	•	H	H	L
	H	H	H	⌐	L	H	H	•	•	•	•	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

FUNCTIONAL DESCRIPTION — The '19 and '20 are decade shift counters with active LOW 1-of-10 decoded outputs. The decoded shift counter technique provides ten mutually exclusive, glitchless outputs. The edge-triggered counter is advanced on each LOW-to-HIGH transition of the Clock input (CP). When the Clock Enable ($\overline{CE}$), Synchronous Reset ($\overline{SR}$), Master Reset ($\overline{MR}$) are HIGH, the device is sequenced via the Clock thru output states $\overline{O}_0 - \overline{O}_9$, successively.

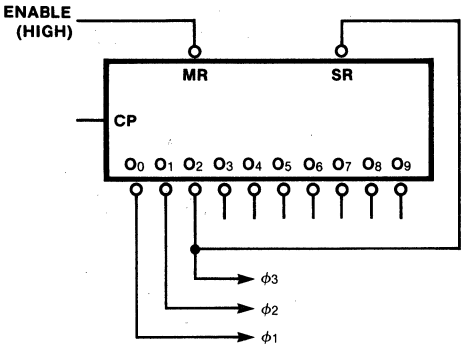
The active HIGH Count Enable (CE) input is gated with the Clock and can be interchanged with Clock for layout convenience. A LOW on the CE input inhibits the Clock and stops the counter. By returning one of the outputs to the CE input, the device will sequence up to that output state and stop until reset with the Master Reset. Because the CE input is gated with the CP input, it cannot be changed from LOW to HIGH while the CP is HIGH.

The active LOW Synchronous Reset ($\overline{SR}$) is used to reset the counter to zero (returning the output to the $\overline{O}_0$ state) in response to the LOW-to-HIGH transition of the Clock. Any sequence between "two" and "ten" can be obtained by connecting the last desired output to the $\overline{SR}$ input. This method of truncating the sequence produces a series of pulses of equal duration as long as the clock frequency remains constant.

A LOW on the Master Reset ($\overline{MR}$) overrides all other input conditions and resets the counter to zero. As long as the $\overline{MR}$ is LOW, all of the outputs are HIGH. When the $\overline{MR}$ goes from LOW to HIGH, the zero output ($\overline{O}_0$) goes LOW. This $\overline{MR}$ gating with the $\overline{O}_0$ output insures complete system resetting or initialization before the first output in the sequencer is activated. For low frequency applications (below 1.0 MHz) the $\overline{MR}$ can be used in lieu of the $\overline{SR}$ for truncating the count sequence. If the input CP rise time is very slow (over 100 ns), the $\overline{MR}$ input should be used to reset the counter to avoid mis-triggering. This is accomplished by returning the next higher output to the $\overline{MR}$ pin. After the desired sequence is completed, the next clock pulse will reset the counter and enable the first output within 50 ns.

The outputs of the '19 are standard TTL totem pole type which can drive up to ten standard TTL unit loads. The outputs of the '20 are DTL resistor pull-up type for applications requiring wired-AND connections. The on-chip pull-up resistors, (about 3 kΩ) of the '20 eliminate the need for external resistors normally required by open-collector outputs. Up to eight '20 outputs can be tied together with enough sink current capability left to drive one standard TTL input or five 93L or 54LS/74LS inputs.

The '19 and '20 will normally require initialization after power is first applied. A LOW pulse on the Master Reset (or a LOW on the Synchronous Reset in conjunction with a clock pulse) will reset the 5-bit register and activate output $\overline{O}_0$. If initialization is not possible or not required, an error correction circuit is provided to detect some of the 22 unused states and return the counter to the proper sequence within ten clock cycles.



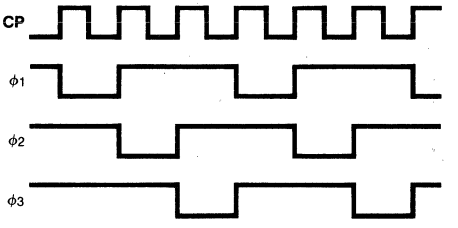
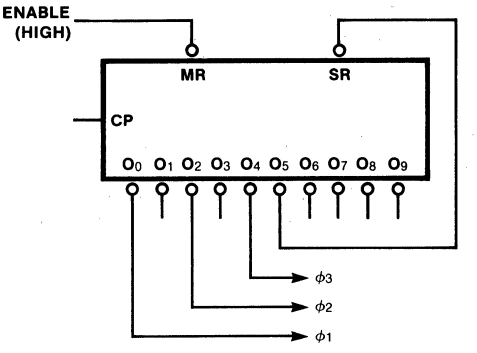


Fig. a Three-Phase Generator Operating at One-Third the Clock Frequency



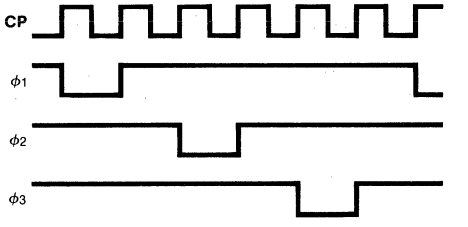


Fig. b Three-Phase Generator Operating at One-Sixth the Clock Frequency

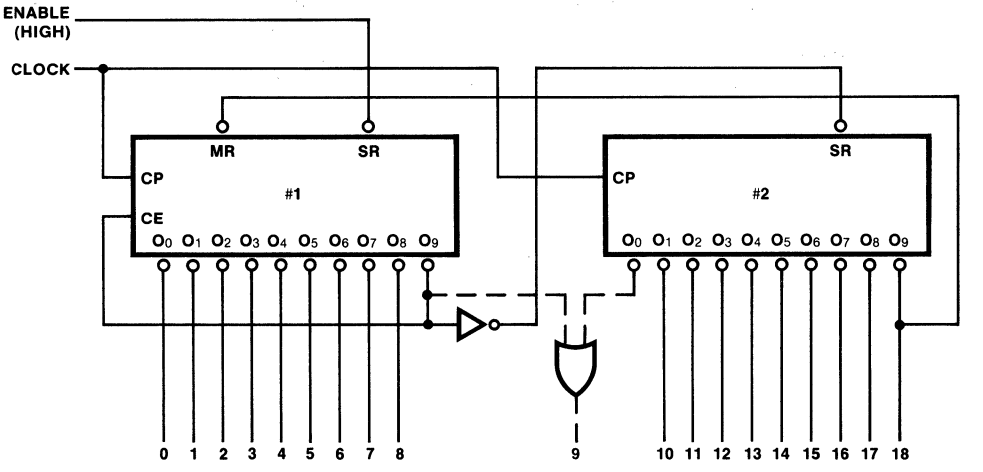


Fig. c Expansion for longer sequences. The first sequencer locks up after $\overline{O}_9$ goes LOW because of the feedback to CE. Simultaneously, $\overline{SR}$ of the second sequencer is released and it starts counting on the next clock. When $\overline{O}_9$ of the second sequencer goes LOW, the feedback to $\overline{MR}$ causes $\overline{O}_9$ of the first sequencer to go HIGH, which then makes $\overline{SR}$ of the second sequencer go HIGH. On the next clock the second sequencer goes to the $\overline{O}_0$ state, releasing $\overline{MR}$ of the first sequencer, making its $\overline{O}_0$ go LOW. On the next clock the first sequencer starts its counting sequence again.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	9319		9320		UNITS	CONDITIONS
		Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage			2.4		V	I_{OH} = -120 μA
I_{OS}	Output Short Circuit Current			-1.3	-3.7	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current		60		60	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	9319		9320		UNITS	CONDITIONS
		C_L = 15 pF		C_L = 15 pF, R_L = 400 Ω			
		Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	35		35		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_n$		40 30		40 30	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to $\overline{O}_n$		50 33		50 33	ns	Figs. 3-1, 3-16

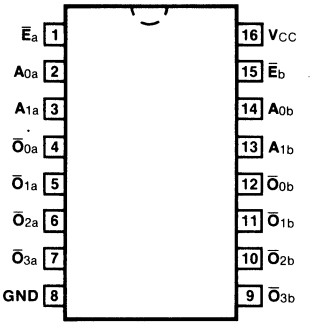
AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	9319		9320		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{SR}$ to CP	10 10		10 10		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{SR}$ to CP	5.0 5.0		5.0 5.0		ns	
t_w	CP Pulse Width	15		15		ns	Fig. 3-16
t_w (L)	$\overline{MR}$ or $\overline{SR}$ Pulse Width LOW	9.0		9.0		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	35		35		ns	Fig. 3-16

6

9321
93L21
DUAL 1-OF-4 DECODER

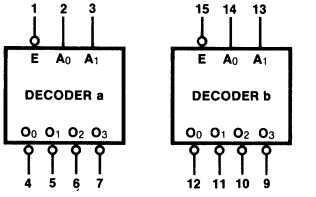
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '21 consists of two independent multipurpose decoders, each designed to accept two inputs and provide four mutually exclusive outputs. In addition an active LOW enable input, which gives demultiplexing capability, is provided for each decoder.

- **MULTIFUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **DEMULTIPLEXING CAPABILITY**
- **ACTIVE LOW ENABLE FOR EACH DECODER**

LOGIC SYMBOL



V_{CC} = Pin 16
Gnd = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	9321PC, 93L21PC		9B
Ceramic DIP (D)	A	9321DC, 93L21DC	9321DM, 93L21DM	6B
Flatpak (F)	A	9321FC, 93L21FC	9321FM, 93L21FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
$\overline{E}_a$, $\overline{E}_b$	Enable Inputs (Active LOW)	1.0/1.0	0.5/0.25
A_{0a}, A_{1a}, A_{0b}, A_{1b}	Address Inputs	1.0/1.0	0.5/0.25
$\overline{O}_{0a}$ — $\overline{O}_{3a}$ $\overline{O}_{0b}$ — $\overline{O}_{3b}$	Decoder Outputs (Active LOW)	20/10	10/5.0 (3.0)

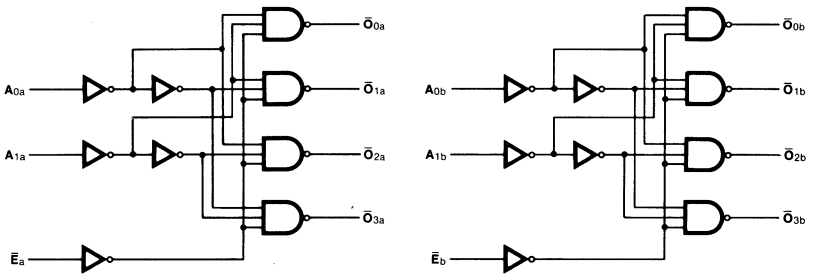
FUNCTIONAL DESCRIPTION — The '21 consists of two separate decoders each designed to accept two binary weighted inputs and provide four mutually exclusive active LOW outputs as shown in the logic symbol. Each decoder can be used as a 4-output demultiplexer by using the enable as a data input.

TRUTH TABLE
(EACH DECODER)

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		50		13.2	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C_L = 15 pF		C_L = 15 pF			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$		20 21		50 65	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{O}_n$		14 18		40 52	ns	Figs. 3-1, 3-5

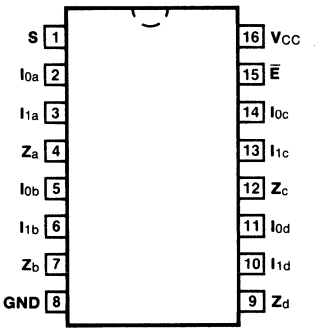
9322
93L22

QUAD 2-INPUT MULTIPLEXER

DESCRIPTION — The '22 quad 2-input digital multiplexers consist of four multiplexing circuits with common select and enable logic; each circuit contains two inputs and one output.

- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED OUTPUTS**

CONNECTION DIAGRAM
PINOUT A



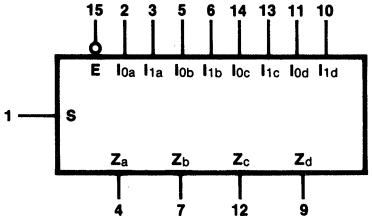
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V, ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9322PC, 93L22PC		9B
Ceramic DIP (D)	A	9322DC, 93L22DC	9322DM, 93L22DM	6B
Flatpak (F)	A	9322FC, 93L22FC	9322FM, 93L22FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
S	Common Select Input	1.0/1.0	0.5/0.25
$\overline{E}$	Enable Input (Active LOW)	1.0/1.0	0.5/0.25
$I_{0a} - I_{0d}$ $I_{1a} - I_{1d}$	Multiplexer Inputs	1.0/1.0	0.5/0.25
$Z_a - Z_d$	Multiplexer Outputs	20/10	10/5.0 (3.0)

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '22 quad 2-input multiplexer provides the ability to select four bits of either data or control from two sources, in one package. The Enable input ($\overline{E}$) is active LOW. When not activated all outputs (Z_n) are LOW regardless of all other inputs.

The '22 quad 2-input multiplexer is the logical implementation of a four-pole, two position switch, with the position of the switch being set by the logic levels supplied to the one select input. The logic equations for the outputs are shown below:

$$Z_a = E \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S}) \qquad Z_b = E \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = E \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S}) \qquad Z_d = E \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

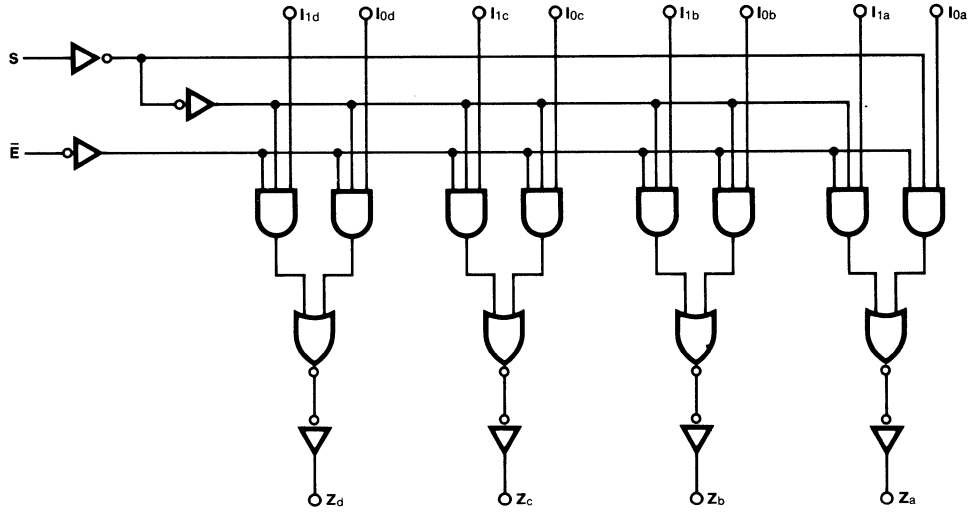
A common use of the '22 is the moving of data from a group of registers to four common output busses. The particular register from which the data comes is determined by the state of the select input. A less obvious use is as a function generator. The '22 can generate four functions of two variables with one variable common. This is useful for implementing random gating functions.

TRUTH TABLE

INPUTS				OUTPUT
$\overline{E}$	S	I_{0n}	I_{1n}	Z_n
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current	-20	-70			mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current		47		13.2	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

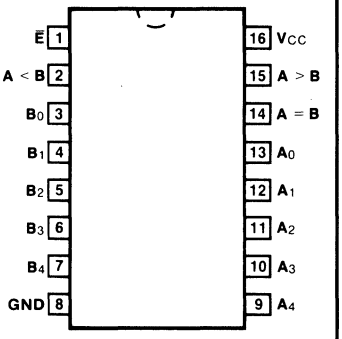
SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C_L = 15 pF R_L = 400 Ω		C_L = 15 pF			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S to Z_n		23 27		36 49	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay I_0 or I_1 to Z_n		14 14		22 30	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z_n		20 21		27 27	ns	Figs. 3-1, 3-4

9324
93L24
5-BIT COMPARATOR

DESCRIPTION — The '24 expandable comparators provide comparison between two 5-bit words and give three outputs — "less than", "greater than" and "equal to". A HIGH on the active LOW Enable Input forces all three outputs LOW.

- **THREE SEPARATE OUTPUTS — A< B, A > B, A = B**
- **EASILY EXPANDABLE**
- **ACTIVE LOW ENABLE INPUT**

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9324PC, 93L24PC		9B
Ceramic DIP (D)	A	9324DC, 93L24DC	9324DM, 93L24DM	6B
Flatpak (F)	A	9324FC, 93L24FC	9324FM, 93L24FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

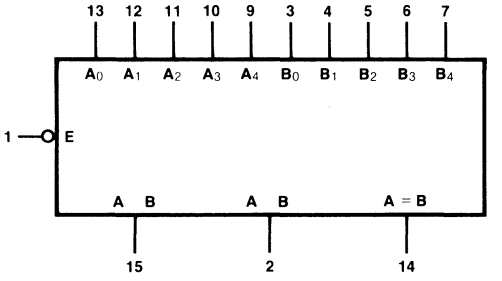
PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
$\overline{E}$	Enable Input (Active LOW)	2.0/2.0	1.0/0.5
A_0 — A_4	Word A Parallel Inputs	2.0/2.0	1.0/0.5
B_0 — B_4	Word B Parallel Inputs	2.0/2.0	1.0/0.5
A < B	A Less than B Output (Active HIGH)	20/10	10/5.0 (3.0)
A > B	A Greater than B Output (Active HIGH)	20/10	10/5.0 (3.0)
A = B	A Equal to B Output (Active HIGH)	20/10	10/5.0 (3.0)

FUNCTIONAL DESCRIPTION — The '24 5-bit comparators use combinational circuitry to directly generate "A greater than B" and "A less than B" outputs. As evident from the logic diagram, these outputs are generated in only three gate delays. The "A equals B" output is generated in one additional gate delay by decoding the "A neither less than nor greater than B" condition with a NOR gate. All three outputs are activated by the active LOW Enable Input ($\overline{E}$).

Tying the A > B output from one device into an A input on another device and the A < B output into the corresponding B input permits easy expansion.

The A_4 and B_4 inputs are the most significant inputs and A_0, B_0 the least significant. Thus if A_4 is HIGH and B_4 is LOW, the A > B output will be HIGH regardless of all other inputs except $\overline{E}$.

LOGIC SYMBOL



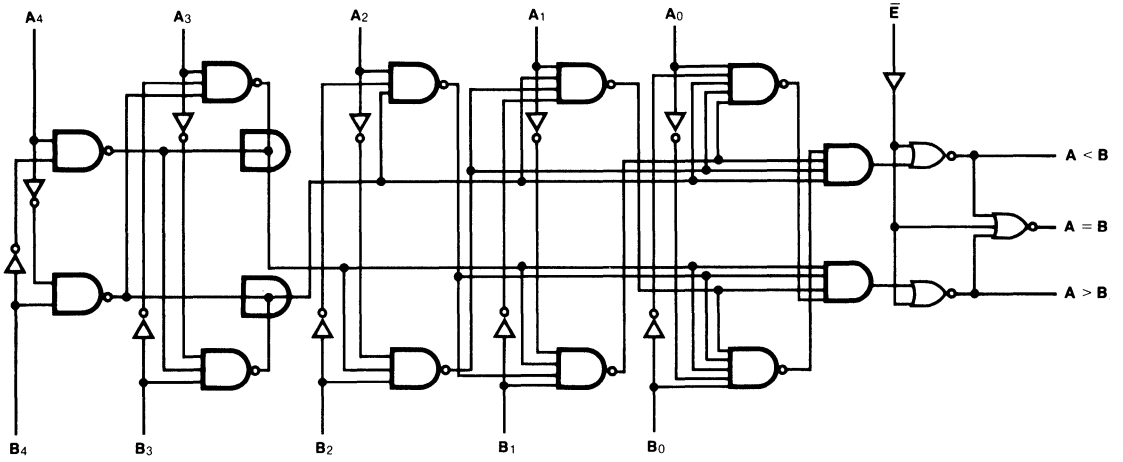
V_{CC} = Pin 16
GND = Pin 8

TRUTH TABLE

INPUTS			OUTPUTS		
$\overline{E}$	A_n	B_n	A < B	A > B	A = B
H	X	X	L	L	L
L	Word A =	Word B	L	L	H
L	Word A >	Word B	L	H	L
L	Word B >	Word A	H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		81		21	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

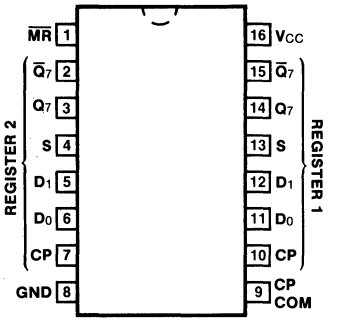
SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C_L = 15 pF		C_L = 15 pF			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\bar{E}$ to A = B		14 14		32 35	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay A_2 to A > B		25 22		54 75	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay A_2 to A < B		26 21		70 77	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay A_2 to A = B		30 32		100 102	ns	Figs. 3-1, 3-20

9328
93L28
DUAL 8-BIT SHIFT REGISTER

DESCRIPTION — The '28 is a high speed serial storage element providing 16 bits of storage in the form of two 8-bit registers. The multifunctional capability of this device is provided by several features: 1) additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources; 2) the clock of each register may be provided separately or together; 3) both the true and complementary outputs are provided from each 8-bit register, and both registers may be master cleared from a common input.

- **2-INPUT MULTIPLEXER PROVIDED AT DATA INPUT OF EACH REGISTER**
- **GATED CLOCK INPUT CIRCUITRY**
- **BOTH TRUE AND COMPLEMENTARY OUTPUTS PROVIDED FROM LAST BIT OF EACH REGISTER**
- **ASYNCHRONOUS MASTER RESET COMMON TO BOTH REGISTERS**

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9328PC, 93L28PC		9B
Ceramic DIP (D)	A	9328DC, 93L28DC	9328DM, 93L28DM	6B
Flatpak (F)	A	9328FC, 93L28FC	9328FM, 93L28FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

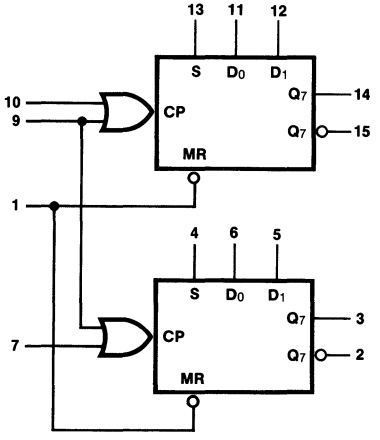
PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
S	Data Select Input	2.0/2.0	1.0/0.5
D_0, D_1	Data Inputs	1.0/1.0	0.5/0.25
CP	Clock Pulse Input (Active HIGH)		
	Common (Pin 9)	3.0/3.0	1.5/0.75
	Separate (Pins 7 and 10)	1.5/1.5	0.75/0.375
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0	0.5/0.25
Q_7	Last Stage Output	20/10	10/5.0 (3.0)
$\overline{Q}_7$	Complementary Output	20/10	10/5.0 (3.0)

FUNCTIONAL DESCRIPTION — The two 8-bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 and 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master/slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR gate are LOW, the slave latches are steady, but data can enter the master latches via the R and S input. During the first LOW-to-HIGH transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain HIGH. During the HIGH-to-LOW transition of the last remaining HIGH clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state. The data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic HIGH signal. Each 8-bit shift register has a 2-input multiplexer in front of the serial data input. The two data inputs D_0 and D_1 are controlled by the data select input (S) following the Boolean expression:

Serial data in: $S_D = SD_0 + SD_1$

An asynchronous master reset is provided which, when activated by a LOW logic level, will clear all 16 stages independently of any other input signal.

LOGIC SYMBOL



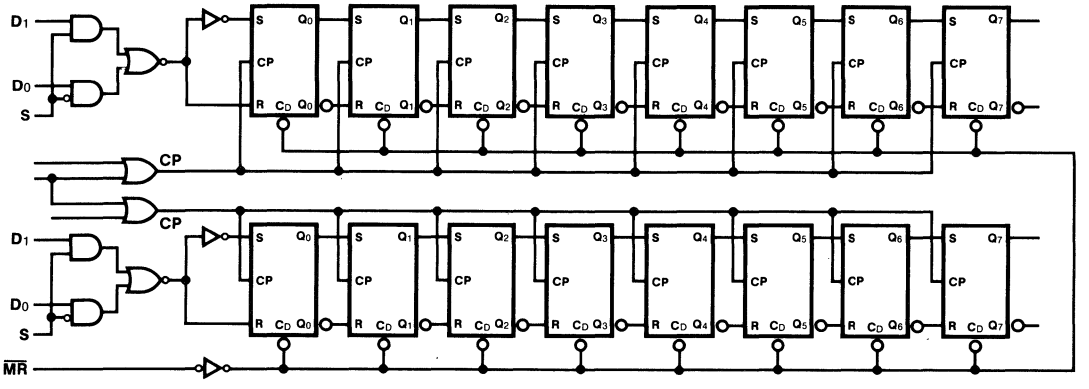
V_{CC} = Pin 16
GND = Pin 8

SHIFT SELECT TABLE

INPUTS			OUTPUT
S	D_0	D_1	Q_7 (t_{n+8})
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
n + 8 = Indicates state after eight clock pulse

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{CC}	Power Supply Current		77		25.3	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C_L = 15 pF, R_L = 400 Ω		C_L = 15 pF			
		Min	Max	Min	Max		
f_{max}	Maximum Shift Right Frequency	20		5.0		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_7 or $\overline{Q}_7$		20 35		45 80	ns	Figs. 3-1, 3-8
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_7		50		110	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

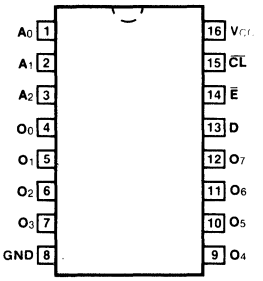
SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Mln	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to CP	20 20		30 30		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to CP	0 0		0 0		ns	
t_w (H) t_w (L)	Clock Pulse Width HIGH or LOW	25 25		55 55		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width with CP HIGH	30		60		ns	Fig. 3-16
t_w (L)	$\overline{MR}$ Pulse Width with CP LOW	40		70		ns	
t_{rec}	Recovery Time $\overline{MR}$ to CP	33				ns	Fig. 3-16

9334
93L34
8-BIT ADDRESSABLE LATCH

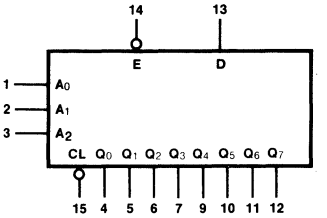
DESCRIPTION — The '34 is an 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level HIGH outputs. The device also incorporates an active LOW common clear for resetting all latches, as well as, an active LOW enable.

- **SERIAL TO PARALLEL CAPABILITY**
- **EIGHT BITS OF STORAGE WITH OUTPUT OF EACH BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY**
- **EASILY EXPANDABLE**
- **COMMON CONDITIONAL CLEAR**

CONNECTION DIAGRAMS
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9334PC, 93L34PC		9B
Ceramic DIP (D)	A	9334DC, 93L34DC	9334DM, 93L34DM	6B
Flatpak (F)	A	9334FC, 93L34FC	9334FM, 93L34FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	1.0/1.0	0.5/0.25
D	Data Input	1.0/1.0	0.5/0.25
$\overline{E}$	Enable Input (Active LOW)	1.5/1.5	0.75/0.38
$\overline{CL}$	Clear Input (Active LOW)	1.0/1.0	0.5/0.25
$Q_0 - Q_7$	Parallel Latch Outputs	18/6.0	10/5.0 (3.0)

FUNCTIONAL DESCRIPTION — The '34 has four modes of operation which are shown in the Mode Select Table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the Data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the Enable should be held HIGH while the Address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the '34 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

MODE SELECT TABLE

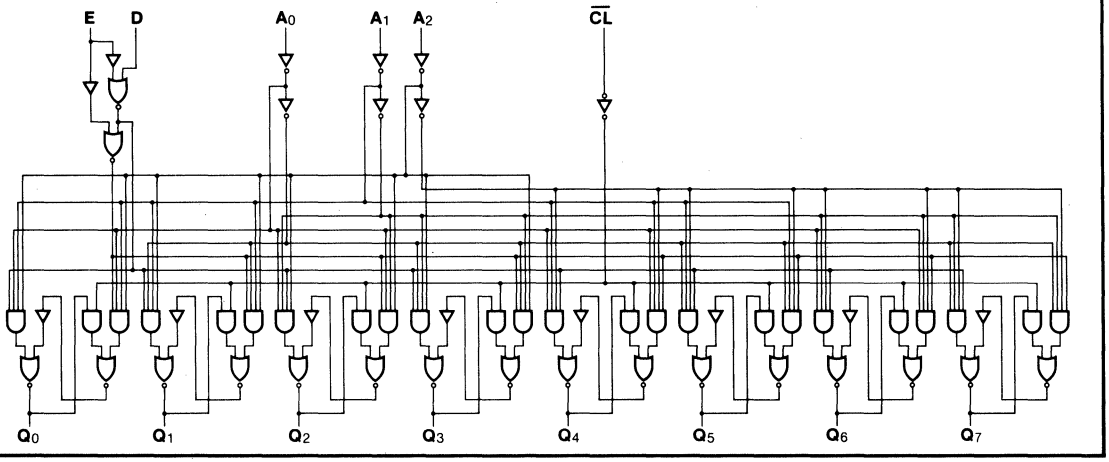
$\overline{E}$	$\overline{CL}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 8-Channel Demultiplexer
H	L	Clear

TRUTH TABLE

INPUTS					OUTPUTS								MODE
$\overline{CL}$	$\overline{E}$	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	D	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	D	L	L	L	L	L	L	
L	L	L	H	L	L	L	D	L	L	L	L	L	
•	•	•	•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	•	•	•	
L	L	H	H	H	L	L	L	L	L	L	L	D	
H	H	X	X	X	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Memory
H	L	L	L	L	D	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Addressable
H	L	H	L	L	Q_{t-1}	D	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Latch
H	L	L	H	L	Q_{t-1}	Q_{t-1}	D	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	
•	•	•	•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	•	•	•	
H	L	H	H	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	D	

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Q_{t-1} = Previous Output State

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		93XX Min	93XX Max	93L Min	93L Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		86		21	mA	V_{CC} = Max
		XC		86		26		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF Min	93XX C_L = 15 pF Max	93L C_L = 15 pF Min	93L C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n		23 24		45 42	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay D to Q_n		28 24		65 45	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n		35 35		66 66	ns	Figs. 3-1, 3-20
t_{PHL}	Propagation Delay $\overline{CL}$ to Q_n		40		55	ns	Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	93XX Min	93XX Max	93L Min	93L Max	UNITS	CONDITIONS
t_s (H)	Setup Time HIGH, D to $\overline{E}$	20		45		ns	Fig. 3-13
t_h (H)	Hold Time HIGH, D to $\overline{E}$	0		-5.0		ns	
t_s (L)	Setup Time LOW, D to $\overline{E}$	17		45		ns	
t_h (L)	Hold Time LOW, D to $\overline{E}$	0		-7.0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to $\overline{E}$	5.0 5.0		10 10		ns	Fig. 3-21
t_w (L)	$\overline{E}$ Pulse Width LOW	17		26		ns	
t_w (L)	$\overline{CL}$ Pulse Width LOW			35		ns	Fig. 3-17

6

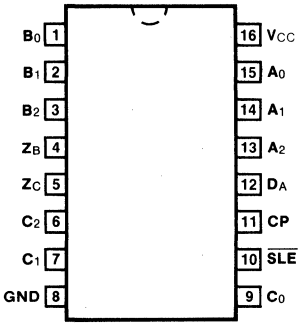
9338
93L38

8-BIT MULTIPLE PORT REGISTER

DESCRIPTION — The '38 is an 8-bit multiple port register designed for high speed random access memory applications where the ability to simultaneously read and write is desirable. A common use would be as a register bank in a three address computer. Data can be written into any one of the eight bits and read from any two of the eight bits simultaneously. The circuit uses TTL technology and is compatible with all TTL families.

- **MASTER/SLAVE OPERATION PERMITTING SIMULTANEOUS WRITE/READ WITHOUT RACE PROBLEMS**
- **SIMULTANEOUSLY READ TWO BITS AND WRITE ONE BIT IN ANY ONE OF EIGHT BIT POSITIONS**
- **READILY EXPANDABLE TO ALLOW FOR LARGER WORD SIZES**

CONNECTION DIAGRAM
PINOUT A



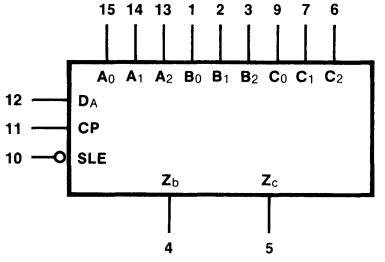
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9338PC, 93L38PC		9B
Ceramic DIP (D)	A	9338DC, 93L38DC	9338DM, 93L38DM	7B
Flatpak (F)	A	9338FC, 93L38FC	9338FM, 93L38FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

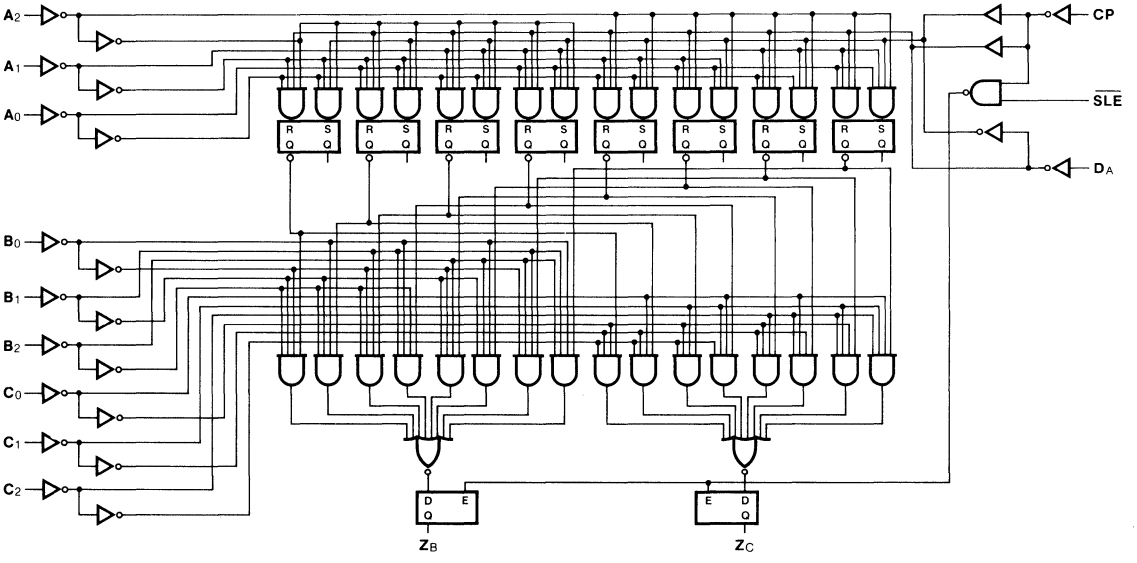
PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
A_0 — A_2	Write Address Inputs	0.67/0.68	0.33/0.17
D_A	Data Input	0.67/0.68	0.33/0.17
B_0 — B_2	B Read Address Inputs	0.67/0.68	0.33/0.17
C_0 — C_2	C Read Address Inputs	0.67/0.68	0.33/0.17
$\overline{CP}$	Clock Pulse Input (Active Rising Edge)	0.67/0.68	0.33/0.17
$\overline{SLE}$	Slave Enable Input (Active LOW)	0.67/0.68	0.33/0.17
Z_B	B Output	20/10	10/5.0 (3.0)
Z_C	C Output	20/10	10/5.0 (3.0)

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The '38 8-bit multiple port register can be considered a 1-bit slice of eight high speed working registers. Data can be written into any one and read from any two of the eight locations simultaneously. Master/slave operation eliminates all race problems associated with simultaneous read/write activity from the same location. When the clock input (CP) is LOW data applied to the data input line (D_A) enters the selected master. This selection is accomplished by coding the three write input select lines (A_0 — A_2) appropriately. Data is stored synchronously with the rising edge of the clock pulse.

The information for each of the two slaved (output) latches is selected by two sets of read address inputs (B_0 — B_2 and C_0 — C_2). The information enters the slave while the clock is HIGH and is stored while the clock is LOW. If Slave Enable is LOW ($\overline{SLE}$), the slave latches are continuously enabled. The signals are available on the output pins (Z_B and Z_C). The input bit selection and the two output bit selections can be accomplished independently or simultaneously. The data flows into the device, is demultiplexed according to the state of the write address lines and is clocked into the selected latch. The eight latches function as masters and store the input data. The two output latches are slaves and hold the data during the read operation. The state of each slave is determined by the state of the master selected by its associated set of read address inputs.

The method of parallel expansion is shown in *Figure a*. One '38 is needed for each bit of the required word length. The read and write input lines should be connected in common on all of the devices. This register configuration provides two words of n-bits each at one time, where n devices are connected in parallel.

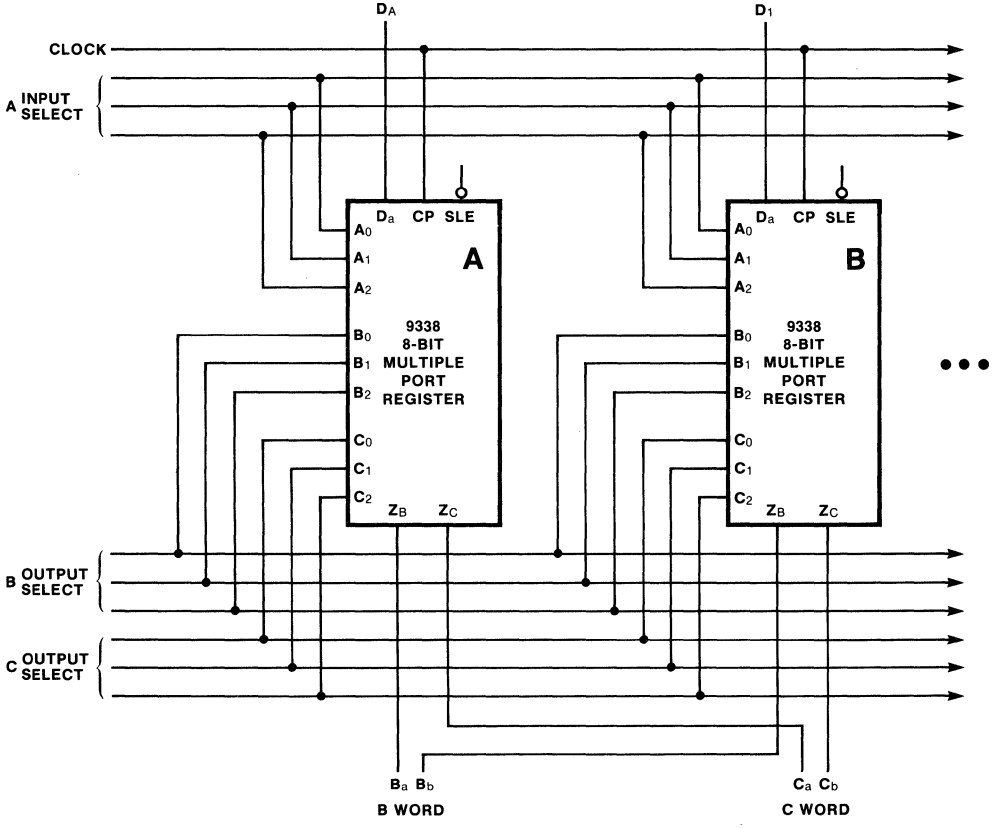


Fig. a Parallel Expansion

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current	-10	-70	-2.5	-25	mA	V_{CC} = Max
I_{CC}	Power Supply Current		135		33	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C_L = 15 pF		C_L = 15 pF			
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay B_n or C_n to Z_n	13 18	40 35		68 95	ns	Figs.3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay D_A to Z_n	25 25	45 50		70 92	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay CP to Z_n	18 13	35 30		65 57	ns	Figs. 3-1, 3-8

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_A to CP	20 12		30 22		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D_A to CP	0 -8.0		0 -4.0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to CP	10 10		0 0		ns	Fig. 3-21
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n to CP	0 0		0 0		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	23 13		40 30		ns	Fig. 3-8

9340

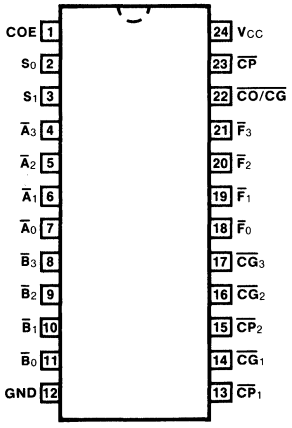
4-BIT ARITHMETIC LOGIC UNIT

(With Carry Lookahead)

DESCRIPTION — The '40 is a high speed arithmetic logic unit with full on-chip carry lookahead circuitry. It can perform the arithmetic operations add or subtract in parallel, or any of six logic functions on two 4-bit binary words. The internal carry lookahead provides either a ripple carry output or carry lookahead outputs. An internal carry input network accepts carry lookahead outputs from up to three other packages producing a 16-bit full carry lookahead ALU without additional gates. Ripple carries can be used between additional blocks of 12 bits to further expand the word length.

- **MULTIFUNCTION CAPABILITY**
  TWO ARITHMETIC OPERATIONS — ADD, SUBTRACT
  SIX LOGIC FUNCTIONS — A EX OR B, A AND B, PLUS FOUR OTHERS
- **ADD TWO 4-BIT WORDS IN 23 ns TYPICAL**
- **SUBTRACT TWO 4-BIT WORDS IN 28 ns**
- **LOOKAHEAD CARRY INPUT AND OUTPUT NETWORKS ON-CHIP**
- **EASILY EXPANDABLE TO LONGER WORD LENGTHS**
- **TYPICAL POWER DISSIPATION OF 425 mW**

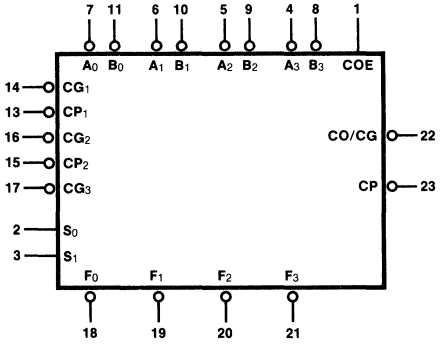
CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9340PC		9N
Ceramic DIP (D)	A	9340DC	9340DM	6N
Flatpak (F)	A	9340FC	9340FM	4M

LOGIC SYMBOL

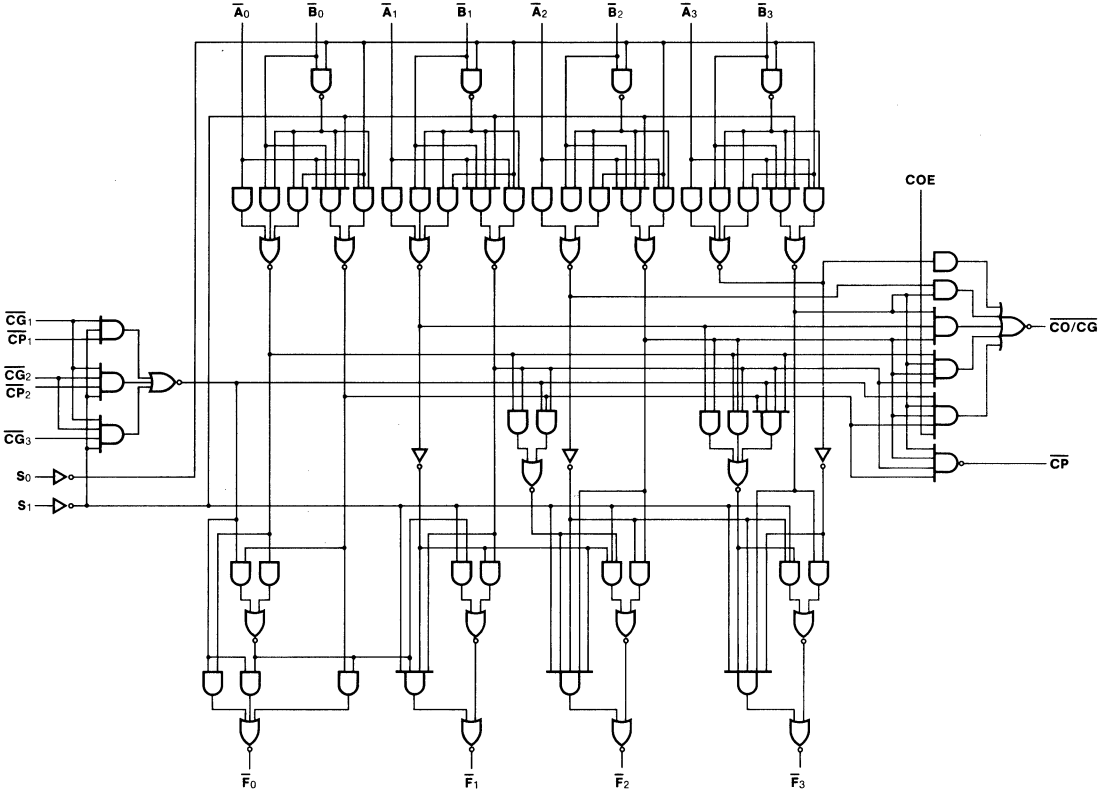


V_{CC} = Pin 24
GND = Pin 12

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
$\overline{A}_0 - \overline{A}_3$, $\overline{B}_0 - \overline{B}_3$	Operand Inputs (Active LOW)	3.0/3.0
S_0, S_1	Mode Select Inputs	1.0/1.0
$\overline{CG}_1$	Carry Generate Input from immediately preceeding stage (Active LOW)	3.0/3.0
$\overline{CP}_1$	Carry Propagate Input from immediately preceeding stage (Active LOW)	1.0/1.0
$\overline{CG}_2$	Carry Generate Input from second preceeding stage (Active LOW)	2.0/2.0
$\overline{CP}_2$	Carry Propagate Input from second preceeding stage (Active LOW)	1.0/1.0
$\overline{CG}_3$	Carry Generate Input from third preceeding stage (Active LOW)	1.0/1.0
COE	Carry Out Enable Input	1.5/1.5
$\overline{F}_0 - \overline{F}_3$	Function Outputs (Active LOW)	20/10
$\overline{CO}/\overline{CG}$	Carry Out/Carry Generate Output (Active LOW)	20/10
$\overline{CP}$	Carry Propagate Output (Active LOW)	20/10

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The '40 accepts two 4-bit words, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$ and $\overline{B}_0$, $\overline{B}_1$, $\overline{B}_2$, $\overline{B}_3$, and produces a 4-bit output, $\overline{F}_0$, $\overline{F}_1$, $\overline{F}_2$, $\overline{F}_3$. The output function is determined by the states on the control lines S_0 and S_1. The inputs and outputs of the '40 may be considered to be active LOW or active HIGH. Logic equivalents for four representations of the '40 are shown in Figure a, b, c, and d.

The add and subtract operations are performed on the entire word, with carries or borrows propagated between bits of different weight. The arithmetic may be performed in 1's complement, 2's complement, or sign-magnitude notation. In the logic modes, carries are inhibited and the device acts like four gates as shown.

To achieve high speed operation, the '40 is designed to be used in a carry lookahead system. Full carry lookahead is used inside the device to propagate carries between bits. Carry lookahead functions over the 4-bit block are available as outputs. These outputs are labeled $\overline{CO/CG}$ (Carry Out/Carry Generate) and $\overline{CP}$ (Carry Propagate) on the logic symbol. The carry in to the device is formed from a set of Carry Generate and Carry Propagate inputs (equation 1) so that three '40's can be interconnected without any additional gates to form a 12-bit full carry lookahead ALU with a carry in. The pin labeled COE (Carry Out Enable) controls the $\overline{CO/CG}$ output according to equation 2. When COE is HIGH, $\overline{CO/CG}$ becomes a Carry Out which can be used to ripple carries between blocks of 12 bits. The $\overline{CG}_1$ input can be used for a ripple carry input, since this signal is sufficient to produce a carry in.

EQUATION:

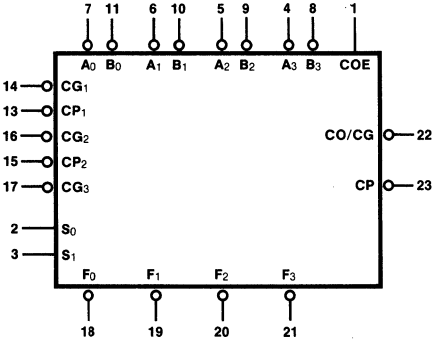
(1) $(\overline{CG}_1) + (\overline{CP}_1)(\overline{CG}_2) + (\overline{CP}_1)(\overline{CP}_2)(\overline{CG}_3) = C_{in}$ (internal)

(2) $\overline{CO/CG} = (\overline{CG}) + (\overline{CP})(C_{in})(COE)$

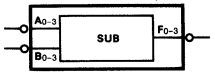
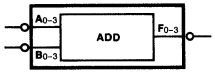
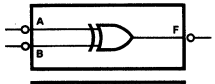
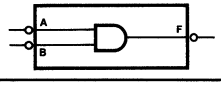
FUNCTION TABLES FOR LOGIC EQUIVALENTS OF THE '40

Note that when the input operands are defined as active HIGH, the carry lookahead inputs and outputs are not formally carry generate and carry propagate. Consequently, these pins have been relabled CX and CY in the active HIGH cases. However, the signals are connected in the same manner as $\overline{CG}$ and $\overline{CP}$.

ACTIVE LOW OPERANDS



V_{CC} = Pin 24
GND = Pin 12

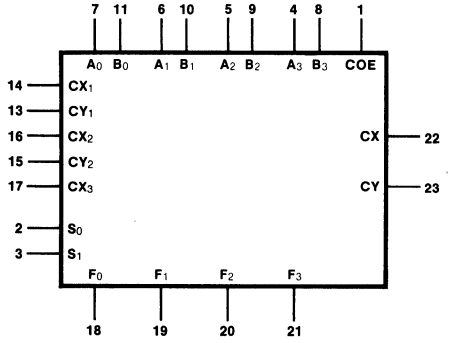
CONTROL INPUTS		OPERATION	EQUIVALENT LOGIC
S_0	S_1		
L	L	A SUBTRACT B	
H	L	A ADD B	
L	H	A EX OR B	
H	H	A AND B	

H = HIGH Voltage Level
L = LOW Voltage Level

Fig. a

FUNCTION TABLES FOR LOGIC EQUIVALENTS OF THE '40 (Cont'd)

ACTIVE HIGH OPERANDS

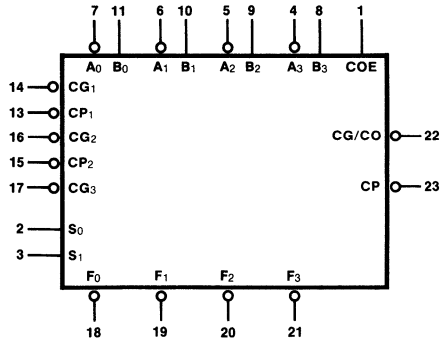


VCC = Pin 24
GND = Pin 12

CONTROL INPUTS S0	S1	OPERATION	EQUIVALENT LOGIC
L	L	A SUBTRACT B	
H	L	A ADD B	
L	H	A EQUIV B	
H	H	A OR B	

Fig. b

ACTIVE LOW OPERANDS WITH INVERTED B

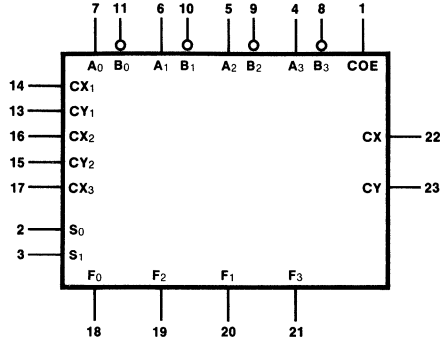


VCC = Pin 24
GND = Pin 12

CONTROL INPUTS S0	S1	OPERATION	EQUIVALENT LOGIC
L	L	A ADD B	
H	L	A SUBTRACT B	
L	H	A EQUIV B	
H	H	A AND $\overline{B}$	

Fig. c

ACTIVE HIGH OPERANDS WITH INVERTED B



VCC = Pin 24
GND = Pin 12

CONTROL INPUTS S0	S1	OPERATION	EQUIVALENT LOGIC
L	L	A ADD B	
H	L	A SUBTRACT B	
L	H	A EX OR B	
H	H	A OR $\overline{B}$	

Fig. d

DC CHARCTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		93XX Min	93XX Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		135	mA	V_{CC} = Max
		XC		146		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF Min	93XX C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay Add Mode, $\overline{B}_0$ to $\overline{F}_3$		30 30	ns	S_0, $\overline{CG}_1$, $\overline{CP}$, $\overline{B}_1$, $\overline{B}_2$ = 4.5 V S_1, $\overline{A}_0$ - $\overline{A}_3$, $\overline{B}_3$ = Gnd Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay for Subtract Mode, $\overline{B}_0$ to $\overline{F}_3$		37 32	ns	$\overline{CG}_1$, $\overline{CP}_1$, $\overline{B}_3$ = 4.5 V; S_0, S_1, $\overline{A}_0$ - $\overline{A}_3$, $\overline{B}_1$, $\overline{B}_2$ = Gnd Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay for Add Mode, $\overline{B}_0$ to $\overline{CO/CG}$		20 20	ns	S_0, $\overline{CG}_1$, $\overline{CP}_1$, $\overline{B}_1$ - $\overline{B}_3$ = 4.5 V; S_1, COE, $\overline{A}_0$ - $\overline{A}_1$ = Gnd Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay for Subtract Mode, $\overline{B}_0$ to $\overline{CO/CG}$		25 22	ns	$\overline{CG}_1$, $\overline{CP}$ = 4.5 V; S_0, S_1, COE, $\overline{A}_0$ - $\overline{A}_3$, $\overline{B}_1$ - $\overline{B}_3$ = Gnd Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay for Either Mode, $\overline{CG}_3$ to $\overline{CO/CG}$		19 19	ns	S_0, $\overline{CG}_1$, $\overline{CG}_2$, COE, $\overline{A}_0$ - $\overline{A}_3$ = 4.5 V; S_1, $\overline{B}_0$ - $\overline{B}_3$ $\overline{CP}_1$, $\overline{CP}_2$ = Gnd Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay for Either Mode, $\overline{CG}_3$ to $\overline{F}_3$		31 29	ns	S_0, $\overline{CG}_1$, $\overline{CG}_2$, $\overline{B}_3$, $\overline{A}_0$ - $\overline{A}_3$ = 4.5 V; S_1, $\overline{B}_0$ - $\overline{B}_2$, $\overline{CP}_1$, $\overline{CP}_2$ = Gnd Figs. 3-1, 3-5

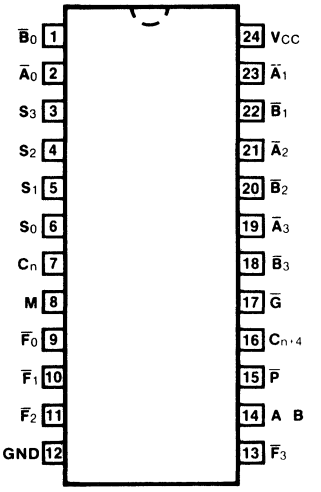
9341
93L41
93S41

4-BIT ARITHMETIC LOGIC UNIT

DESCRIPTION—The '41 4-bit arithmetic logic units can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations; the Add and Subtract modes are the most important. The '41 is a pin replacement for the 54/74181.

- **PROVIDE 16 OPERATIONS**
  ADD, SUBTRACT, COMPARE, DOUBLE
  TWELVE OTHER ARITHMETIC OPERATIONS
- **PROVIDE ALL 16 LOGIC OPERATIONS OF TWO VARIABLES**
  EXCLUSIVE-OR, COMPARE, AND NAND, OR, NOR, PLUS
  TEN OTHER LOGIC OPERATIONS

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9341PC, 93L41PC 93S41PC		9N
Ceramic DIP (D)	A	9341DC, 93L41DC 93S41DC	9341DM, 93L41DM 93S41DM	6N
Flatpak (F)	A	9341FC, 93L41FC 93S41FC	9341FM, 93L41FM 93S41FM	4M

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW	93S (U.L.) HIGH/LOW
$\overline{A}_0 - \overline{A}_3$, $\overline{B}_0 - \overline{B}_3$	Operand Inputs (Active LOW)	3.0/3.0	1.5/0.75	3.75/3.75
$S_0 - S_3$	Function Select Inputs	4.0/4.0	2.0/1.0	5.0/5.0
M	Mode Control Input	1.0/1.0	0.5/0.25	1.25/1.25
C_n	Carry Input	5.0/5.0	2.5/1.25	7.5/7.5
$\overline{F}_0 - \overline{F}_3$	Function Outputs (Active LOW)	20/10	10/5.0 (3.0)	25/12.5
A = B	Comparator Output	OC*/10	OC*/5.0 (3.0)	OC*/12.5
$\overline{G}$	Carry Generator Output (Active LOW)	20/10	10/5.0 (3.0)	25/12.5
$\overline{P}$	Carry Propagate Output (Active LOW)	20/10	10/5.0 (3.0)	25/12.5
C_{n+4}	Carry Output	20/10	10/5.0 (3.0)	25/12.5

*OC—Open Collector

FUNCTIONAL DESCRIPTION — The '41 is a 4-bit high speed parallel arithmetic logic unit (ALU). Controlled by the four Function Select inputs (S_0 — S_3) and the Mode Control input (M), it can perform all the 16 possible operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table below lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead betweeen packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, the '41 can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For super high speed operation the Schottky '41 should be used in conjunction with the '42 carry lookahead circuit.

The A = B output from the '41 goes HIGH when all four $\overline{F}_n$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open-collector and can be wired-AND with the other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated the '41 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labled inside the logic symbol.

FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS		ACTIVE HIGH INPUTS & OUTPUTS	
				LOGIC	ARITHMETIC**	LOGIC	ARITHMETIC**
S_3	S_2	S_1	S_0	(M = H)	(M = L) (C_n = L)	(M = H)	(M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{A}\overline{B}$	AB minus 1	$\overline{A} + \overline{B}$	A + B
L	L	H	L	$\overline{A} + \overline{B}$	$A\overline{B}$ minus 1	$\overline{A}B$	$A + \overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A} + \overline{B}$	A plus $(A + \overline{B})$	$\overline{A\overline{B}}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus $(A + \overline{B})$	$\overline{B}$	$(A + B)$ plus $A\overline{B}$
L	H	H	L	$\overline{A} \oplus \overline{B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$A + \overline{B}$	$A + \overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
H	L	L	L	$\overline{A}B$	A plus (A + B)	$\overline{A} + B$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$A \oplus B$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)	B	$(A + \overline{B})$ plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A*	Logic 1	A plus A*
H	H	L	H	$A\overline{B}$	AB plus A	$A + \overline{B}$	$(A + B)$ plus A
H	H	H	L	AB	$A\overline{B}$ minus A	A + B	$(A + \overline{B})$ plus A
H	H	H	H	A	A	A	A minus 1

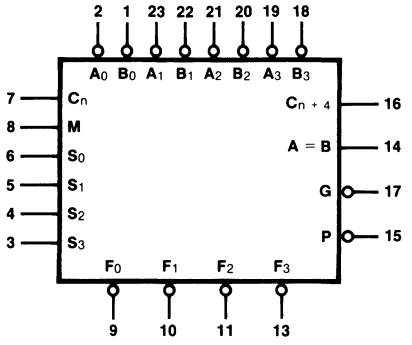
*Each bit is shifted to the next more significant position

**Arithmetic operations expressed in 2s complement notation

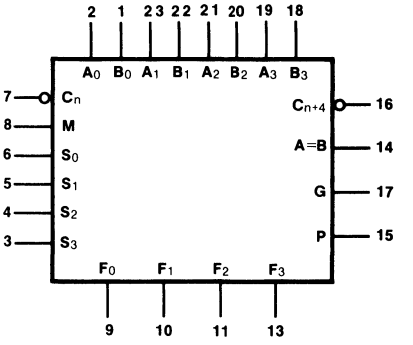
H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC SYMBOLS

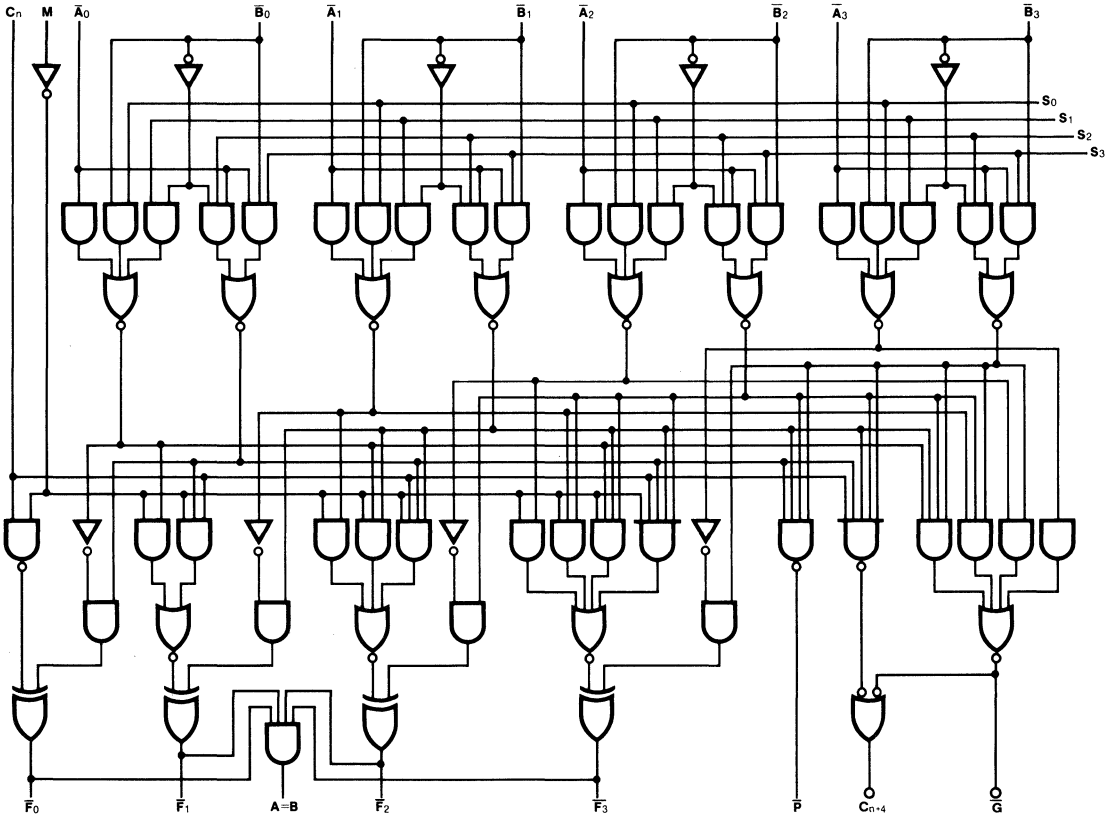
ACTIVE LOW OPERANDS



ACTIVE HIGH OPERANDS



LOGIC DIAGRAM



6

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		93XX Min	93XX Max	93L Min	93L Max	93S Min	93S Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		127				125	mA	V_{CC} = Max C_n, $\overline{B}_0$ - $\overline{B}_3$ = Gnd All Other Inputs = 4.5 V
		XC		140				140		
I_{CC}	Power Supply Current	XM		135				135	mA	V_{CC} = Max M, S_0 - S_3 = 4.5 V All Other Inputs = Gnd
		XC		150				150		
I_{CC}	Power Supply Current					36			mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF, R_L = 400 Ω Min	93XX Max	93L C_L = 15 pF Min	93L Max	93S C_L = 15 pF, R_L = 280 Ω Min	93S Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+4}		16 17		51 22		12 12	ns	M = Gnd Figs. 3-1, 3-4 Tables I & II
t_{PLH} t_{PHL}	Propagation Delay C_n to $\overline{F}$		17 17		37 42		12 12	ns	M = Gnd Figs. 3-1, 3-4 Table I
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$		19 12		51 26		14 14	ns	M, S_1, S_2 = Gnd S_0, S_3 = 4.5 V Figs. 3-1, 3-5 Table I
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$		22 17		50 43		15 15	ns	M, S_0, S_3 = Gnd S_1, S_2 = 4.5 V Figs. 3-1, 3-4, 3-5 Table II
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$		19 15		50 46		14 14	ns	M, S_1, S_2, = Gnd S_0, S_3, = 4.5 V Figs. 3-1, 3-5 Table I
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$		21 21		38 63		15 15	ns	M, S_0, S_3 = Gnd S_1, S_2 = 4.5 V Figs. 3-1, 3-4, 3-5 Table II
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$		26 26		36 65		20 20	ns	M, S_1, S_3 = Gnd S_0, S_3 = 4.5 V Figs. 3-1, 3-5 Table I

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (Cont'd)

SYMBOL	PARAMETER	93XX C_L = 15 pF, R_L = 400 Ω		93L C_L = 15 pF		93S C_L = 15 pF, R_L = 280 Ω		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$		26 32		39 49		21 21	ns	M, S_0, S_3 = Gnd S_1, S_2 = 4.5 V Figs. 3-1, 3-4, 3-5 Table II
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_{i+1}$		29 25		56 62		24 24	ns	M, S_1, S_2 = Gnd S_0, S_3 = 4.5 V Figs. 3-1, 3-5 Table I
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_{i+1}$		29 30		68 71		25 25	ns	M, S_0, S_3 = Gnd S_1, S_2 = 4.5 V Figs. 3-1, 3-4, 3-5 Table II
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}$		24 24		51 49		20 20	ns	M = 4.5 V Figs. 3-1, 3-5 Table III
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+1}		21 30		46 60		18.5 18.5	ns	M, S_1, S_2 = Gnd S_0, S_3 = 4.5 V Figs. 3-1, 3-4 Table I
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+1}		25 30		60 58		23 23	ns	M, S_0, S_3 = Gnd S_1, S_2 = 4.5 V Figs. 3-1, 3-4, 3-5 Table II
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to A = B		40 42		68 72		23 23	ns	M, S_0, S_3 = Gnd S_1, S_2 = 4.5 V R_L = 400 Ω to 5.0 V; Figs. 3-1, 3-4, 3-5; Table II

SUM MODE TEST TABLE I **FUNCTION INPUTS:** $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = M = 0$ V

SYMBOL	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE II **FUNCTION INPUTS:** $S_1 = S_2 = 4.5$ V, $S_0 = S_3 = M = 0$ V

SYMBOL	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}

LOGIC MODE TEST TABLE III **FUNCTION INPUTS:** $S_1 = S_2 = M = 4.5$ V, $S_0 = S_3 = 0$ V

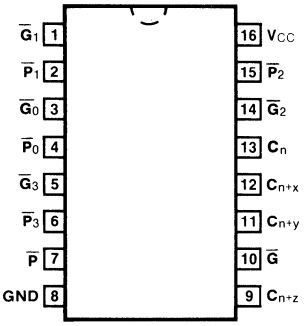
SYMBOL	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$

9342
93S42
CARRY LOOKAHEAD GENERATOR

DESCRIPTION — The '42 is a high speed lookahead carry generator. It is generally used with the 9341 (54/74181) 4-bit arithmetic logic unit to provide high speed lookahead over word lengths of more than four bits. The lookahead carry generator is fully compatible with all members of the TTL family.

- **PROVIDES LOOKAHEAD CARRIES ACROSS A GROUP OF FOUR ALU'S**
- **MULTI-LEVEL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION OVER LONG WORD LENGTHS**

CONNECTION DIAGRAM
PINOUT A



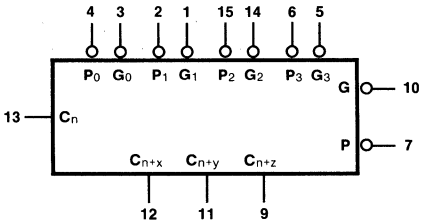
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	9342PC, 93S42PC		9B
Ceramic DIP (D)	A	9342DC, 93S42DC	9342DM, 93S42DM	7B
Flatpak (F)	A	9342FC, 93S42FC	9342FM, 93S42FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93S (U.L.) HIGH/LOW
C_n	Carry Input	1.0/1.0	1.25/1.25
$\overline{G}_0$, $\overline{G}_2$	Carry Generate Inputs (Active LOW)	7.0/7.0	8.75/8.75
$\overline{G}_1$	Carry Generate Input (Active LOW)	8.0/8.0	10/10
$\overline{G}_3$	Carry Generate Input (Active LOW)	4.0/4.0	5.0/5.0
$\overline{P}_0$, $\overline{P}_1$	Carry Propagate Inputs (Active LOW)	4.0/4.0	5.0/5.0
$\overline{P}_2$	Carry Propagate Input (Active LOW)	3.0/3.0	3.75/3.75
$\overline{P}_3$	Carry Propagate Input (Active LOW)	2.0/2.0	2.5/2.5
C_{n+x} — C_{n+z}	Carry Outputs	20/10	25/12.5
$\overline{G}$	Carry Generate Output (Active LOW)	20/10	25/12.5
$\overline{P}$	Carry Propagate Output (Active LOW)	20/10	25/12.5

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '42 lookahead carry generator accepts up to four pairs of active LOW Carry Propagate ($\overline{P}_0$ — $\overline{P}_3$) and Carry Generate ($\overline{G}_0$ — $\overline{G}_3$) signals and an active HIGH Carry input (C_n) and provides anticipated active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The '42 also has active LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead. The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0 C_n$$
$$C_{n+y} = G_1 + P_1 G_0 + P_1 P_0 C_n$$
$$C_{n+z} = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n$$
$$\overline{G} = \overline{G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0}$$
$$\overline{P} = \overline{P_3 P_2 P_1 P_0}$$

Also, the '42 can be used with binary ALU's in an active LOW or active HIGH input operand mode. The connections *(Figure a)* to and from the ALU to the lookahead carry generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last 93S41.

TRUTH TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

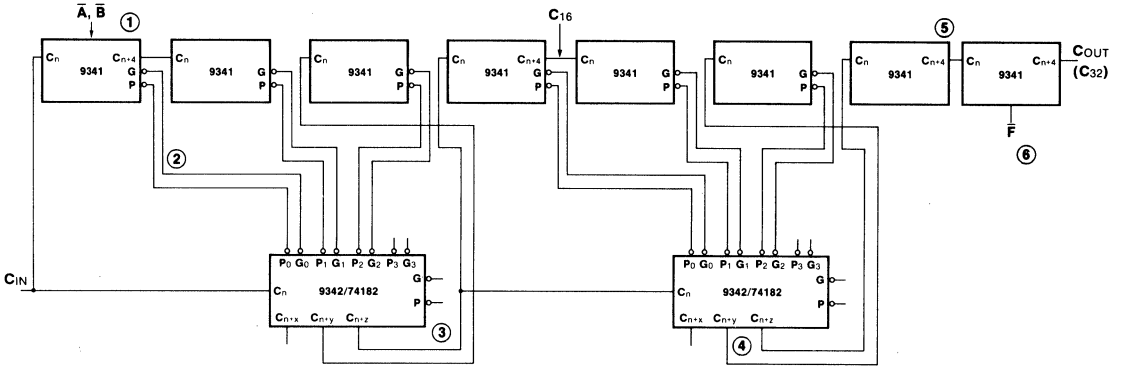
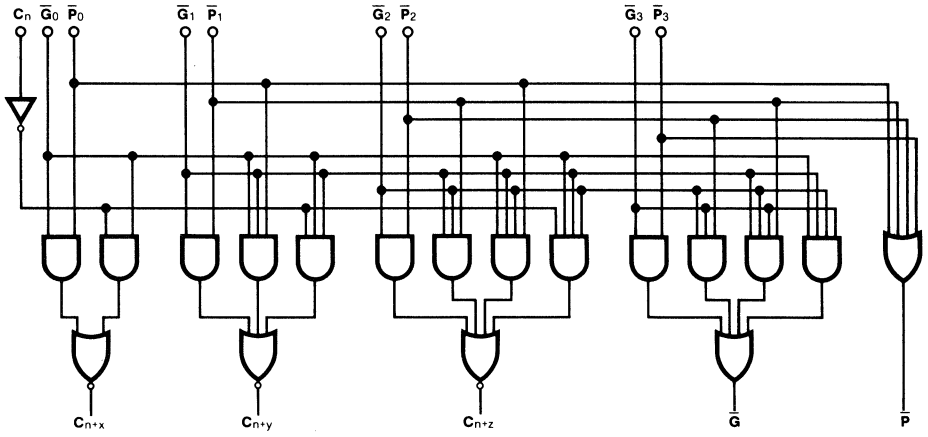


Fig. a 32-Bit ALU with Ripple Carry Between 16-Bit Lookahead ALUs

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		93XX Min	93XX Max	93S Min	93S Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current		-40	-100	-40	-100	mA	V_{CC} = Max
I_{CCH}	Power Supply Current (All Outputs HIGH)	XM		35		45	mA	V_{CC} = Max; $\overline{P}_3$, $\overline{G}_3$ = 4.5 V All Other Inputs = Gnd
		XC		39				
I_{CCL}	Power Supply Current (All Outputs LOW)	XM		65		80	mA	V_{CC} = Max $\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$ = 4.5 V All Other Inputs = Gnd
		XC		72				

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF, R_L = 400 Ω Min	93XX Max	93S C_L = 15 pF Min	93S Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+x}, C_{n+y}, C_{n+z}		16 19		10 11.5	ns	Figs. 3-1, 3-5 $\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$ = Gnd $\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$ = 4.5 V
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_0$, $\overline{P}_1$, or $\overline{P}_2$ to C_{n+x}, C_{n+y}, C_{n+z}		13 14		7.0 7.0	ns	Figs. 3-1, 3-4 $\overline{P}_x$ = Gnd (if not under test) C_n, $\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$ = 4.5 V
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_0$, $\overline{G}_1$, or $\overline{G}_2$ to C_{n+x}, C_{n+y}, C_{n+z}		13 14		7.0 7.0	ns	Figs. 3-1, 3-4 $\overline{G}_x$ = 4.5 V (if not under test) C_n, $\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$ = Gnd
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{G}$		16 19		7.5 10.5	ns	Figs. 3-1, 3-5 $\overline{P}_x$ = Gnd (if not under test) $\overline{G}_n$, C_n = 4.5 V
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_n$ to $\overline{G}$		16 19		7.5 10.5	ns	Figs. 3-1, 3-5 $\overline{G}_x$ = 4.5 V (if not under test) $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$ = Gnd
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_n$ to $\overline{P}$		16 19		6.5 10	ns	Figs. 3-1, 3-5 $\overline{P}_x$ = Gnd (if not under test)

6

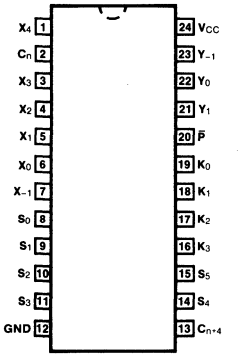
93S43

4-BIT BY 2-BIT TWOS COMPLEMENT MULTIPLIER

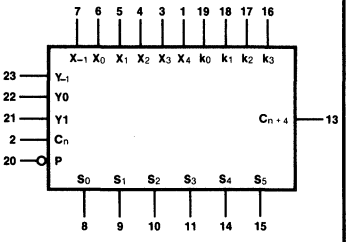
DESCRIPTION — The '43 is a high speed twos complement multiplier. The device is a 4-bit by 2-bit building block that can be connected in an iterative array to perform multiplication of two binary numbers of variable lengths. The device can generate the twos complement product, without correction, of two binary numbers presented in twos complement notation.

- **VERY HIGH SPEED MULTIPLICATION — TWO 12-BIT NUMBERS IN 125 ns (TYP)**
- **PROVIDES TWOS COMPLEMENT PRODUCT WITHOUT CORRECTION**
- **EXPANDS TO ANY SIZE ARRAY WITHOUT ADDITIONAL COMPONENTS**
- **ACCEPTS ACTIVE HIGH OR ACTIVE LOW OPERANDS**
- **EASILY CORRECTABLE FOR UNSIGNED, SIGN-MAGNITUDE OR ONES COMPLEMENT MULTIPLICATION**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 24
GND = Pin 12

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	93S43PC		9N
Ceramic DIP (D)	A	93S43DC	93S43DM	6N
Flatpak (F)	A	93S43FC	93S43FM	4M

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

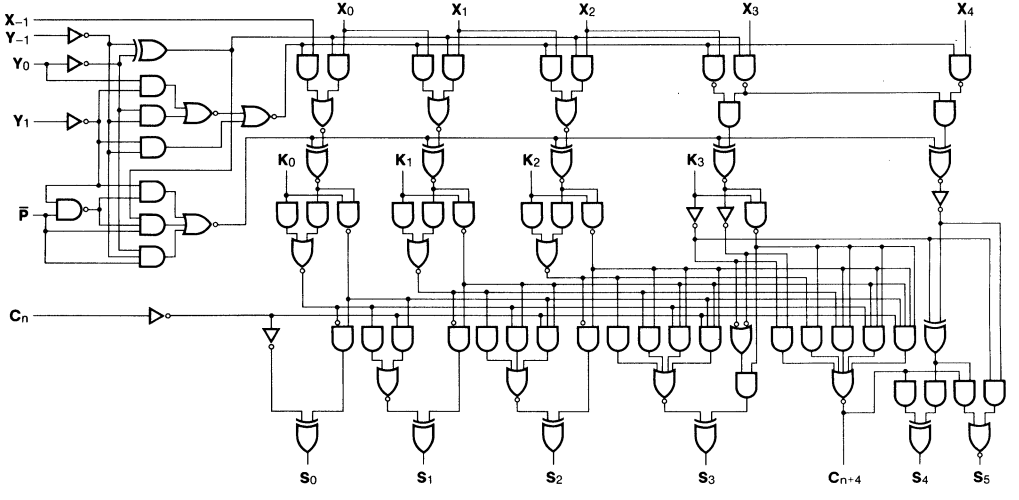
PIN NAMES	DESCRIPTION	93S (U.L.) HIGH/LOW
x_{-1}, x_3, x_4	Multiplicand Inputs	1.0/1.0
x_0, x_1, x_2	Multiplicand Inputs	2.0/2.0
Y_0	Multiplier Input	2.0/2.0
y_{-1}, y_1	Multiplier Inputs	1.0/1.0
k_0 — k_3	Constant Inputs	2.0/2.0
C_n	Carry Input	1.0/1.0
$\overline{P}$	Polarity Control Input (Active LOW for HIGH Operands)	3.0/3.0
S_0 — S_5	Product Outputs	25/12.5
C_{n+4}	Carry Output	25/12.5

FUNCTIONAL DESCRIPTION — The '43 is a super fast hardware multiplier employing Schottky technology and twos complement arithmetic. It multiplies a multiplicand of four bits by a multiplier of two bits and forms a basic iterative logic cell. It can also multiply in active HIGH (positive logic) or active LOW (negative logic) representations by reinterpreting the active levels of the inputs, outputs and the Polarity Control ($\overline{P}$). The binary number with 1 as the most significant bit is treated as a negative number represented in twos complement form. These '43 iterative logic cells can be connected to implement multiplication of an X-bit number by a Y-bit number. This application requires X • Y ÷ 4 • 2 packages and the resulting product has X + Y bits. At the beginning of the array, a constant can be presented at the K inputs that will be added to the least significant part of the product. The packages can be connected in parallel, triangular or split-array scheme depending on the speed requirement. The '41 ALU can be used with these multipliers in the split-array scheme to obtain high speed multiplication.

TABLE I SWITCHING TEST CONDITIONS

INPUT	OUTPUTS	INPUTS AT 0 V (Remaining Inputs at 4.5 V)
C_n	C_{n+4}, S_0 — S_3, S_4, S_5	$\overline{P}$, y_{-1}, y_1, All x
k_0	C_{n+4}, S_0 — S_3, S_4, S_5	$\overline{P}$, y_{-1}, y_1, All x
k_1	C_{n+4}, S_1 — S_3, S_4, S_5	$\overline{P}$, y_{-1}, y_1, All x
k_2	C_{n+4}, S_2, S_3, S_4, S_5	$\overline{P}$, y_{-1}, y_1, All x
k_3	S_3	$\overline{P}$, y_{-1}, y_1, All x
k_3	S_4, S_5	$\overline{P}$, y_{-1}, y_1, All x, C_n
x_{-1}	C_{n+4}, S_0 — S_3, S_4, S_5	$\overline{P}$, y_1, All k
x_0	C_{n+4}, S_0 — S_3, S_4, S_5	$\overline{P}$, y_{-1}, y_1, All k
x_1	C_{n+4}, S_1 — S_3, S_4, S_5	$\overline{P}$, y_{-1}, y_1, All k
x_2	C_{n+4}, S_2, S_3, S_4, S_5	$\overline{P}$, y_{-1}, y_1, All k
x_3, x_4	S_3	$\overline{P}$, y_{-1}, y_1, All k
x_3, x_4	S_4, S_5	$\overline{P}$, y_{-1}, y_1, All k, C_n
x_3, x_4	S_4, S_5	$\overline{P}$, y_{-1}, All k, C_n
y_{-1}	C_{n+4}, S_0 — S_3, S_4, S_5	$\overline{P}$, x_1, x_2, x_3, x_4, All k
y_0	C_{n+4}, S_0 — S_3, S_4, S_5	$\overline{P}$, x_1, x_2, x_3, x_4, All k
y_1	C_{n+4}, S_0 — S_3, S_4, S_5	x_0, x_1, x_2, x_3, x_4, All k

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93S		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		149	mA	V_{CC} = Max

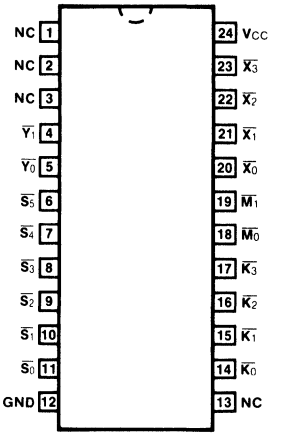
AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93S C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+4}		9.0 9.0	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay C_n to $S_0 - S_3$		13 11	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay C_n to S_4, S_5		16 15	ns	Figs. 3-1, 3'4
t_{PLH} t_{PHL}	Propagation Delay k_n to C_{n+4}		12 13	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay k_n to $S_0 - S_3$		14 12	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay k_n to S_4, S_5		19 17	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay x_n to C_{n+4}		15 24	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay x_n to $S_0 - S_3$		25 25	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay x_n to S_4, S_5		30 21	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay y_n to C_{n+4}		25 27	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay y_n to $S_0 - S_3$		28 27	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay y_n to S_4, S_5		32 30	ns	Figs. 3-1, 3-4

9344

BINARY (4-BIT BY 2-BIT) FULL MULTIPLIER

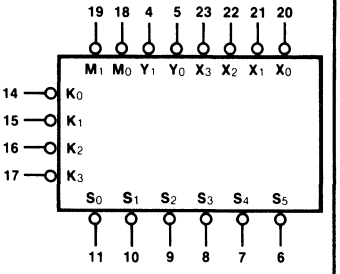
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '44 is a 4-bit by 2-bit full multiplier building block. It multiplies two binary numbers and simultaneously adds two other binary numbers to the product. '44 devices can be interconnected to form a high speed multiplier array of any size. The device is constructed with TTL compatible inputs and outputs. Inputs are buffered to reduce loading.

- **PERFORMS DIRECT MULTIPLICATION**
- **EXPANDS TO ANY SIZE ARRAY WITHOUT ADDITIONAL COMPONENTS**
- **MULTIPLIES AND ADDS SIMULTANEOUSLY**

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE: V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9344PC		9N
Ceramic DIP (D)	A	9344DC	9344DM	6N
Flatpak (F)	A	9344FC	9344FM	4M

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
$\overline{X}_0 - \overline{X}_3$	Multiplicand Inputs (Active LOW)	0.66/0.66
$\overline{Y}_0$, $\overline{Y}_1$	Multiplier Inputs (Active LOW)	0.66/0.66
$\overline{M}_1$	Additive Carry Inputs (Active LOW)	1.0/1.0
$\overline{K}_0$, $\overline{M}_0$		4.0/4.0
$\overline{K}_1 - \overline{K}_3$		2.0/2.0
$\overline{S}_0 - \overline{S}_5$	Outputs	20/10

FUNCTIONAL DESCRIPTION — The '44 is a binary full multiplier for 4-bit by 2-bit words. It is easily expandable in an array to form a high speed parallel multiplier of any length. The functional equation is illustrated below:

$$S\ (6\text{-bits}) = \overline{X}(4\text{-bits})\ \text{times}\ \overline{Y}(2\text{-bits})\ \text{plus}\ \overline{M}(2\text{-bits})\ \text{plus}\ \overline{K}(4\text{-bits})$$

Functionally the '44 multiplies a 4-bit word ($\overline{X}_0 - \overline{X}_3$) by a two bit word ($\overline{Y}_0 - \overline{Y}_1$), generating eight partial products. Two other words, $\overline{K}_0 - \overline{K}_3$ and $\overline{M}_0 - \overline{M}_1$, are added to these partial products through a lookahead carry adder, generating a 6-bit product/sum. The function can be described by the following equation (note that "+" means arithmetic addition):

$$S = 2^0(\overline{X}_0\overline{Y}_0 + \overline{M}_0 + \overline{K}_0) + 2^1(\overline{X}_1\overline{Y}_0 + \overline{X}_0\overline{Y}_1 + \overline{M}_1 + \overline{K}_1) + 2^2(\overline{X}_2\overline{Y}_0 + \overline{X}_1\overline{Y}_1 + \overline{K}_2) + 2^3(\overline{X}_3\overline{Y}_0 + \overline{X}_2\overline{Y}_1 + \overline{K}_3) + 2^4(\overline{X}_3\,\overline{Y}_1)$$

All inputs and outputs are active LOW; $\overline{X}$ and $\overline{Y}$ inputs are buffered to present only one TTL unit load. The device operates only on positive numbers. If two's complement multiplication is required, then the numbers must be changed to sign magnitude before multiplication, or else the product must be corrected following multiplication of the two's complement numbers. The correction algorithm depends on whether $\overline{X}$ or $\overline{Y}$ or both are negative.

If $\overline{X}$ is negative:
Subtract $\overline{Y}$ from most significant half of product.

If $\overline{Y}$ is negative:
Subtract $\overline{X}$ from most significant half of product.

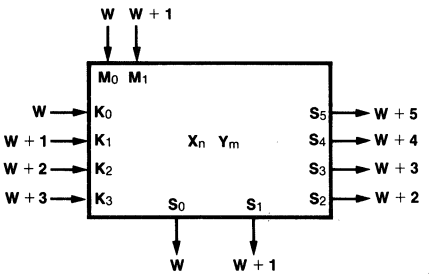
If both $\overline{X}$ and $\overline{Y}$ are negative:
Add $\overline{X}$ plus $\overline{Y}$ to most significant half of product.

The result will be the correct two's complement product.

MULTIPLICATION TIME

NUMBER OF BITS	PACKAGES	TIME (ns)
8 x 8	8	150
12 x 12	18	260
16 x 16	32	350
24 x 24	72	550

WEIGHTING FACTORS OF THE BASIC MULTIPLIER



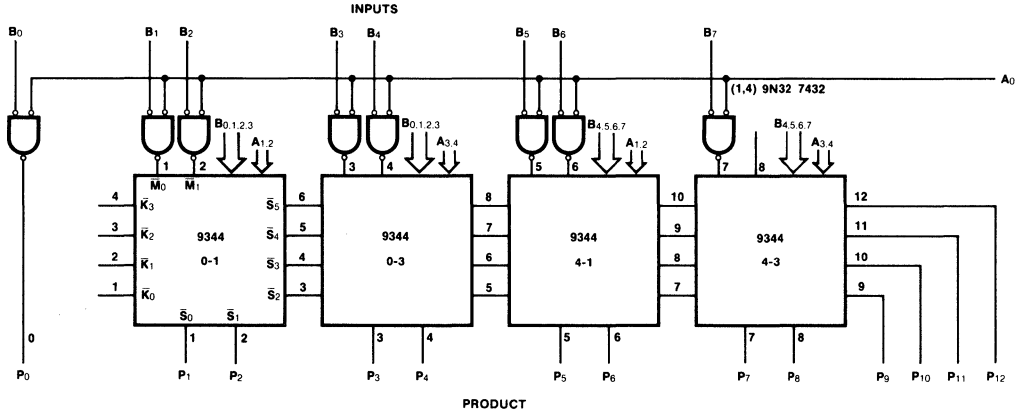
This block represents the basic 4-bit by 2-bit multiplier, and indicates the weighting factors (power of two) attached to each of the inputs and outputs.

TYPICAL MULTIPLICATION ARRAYS

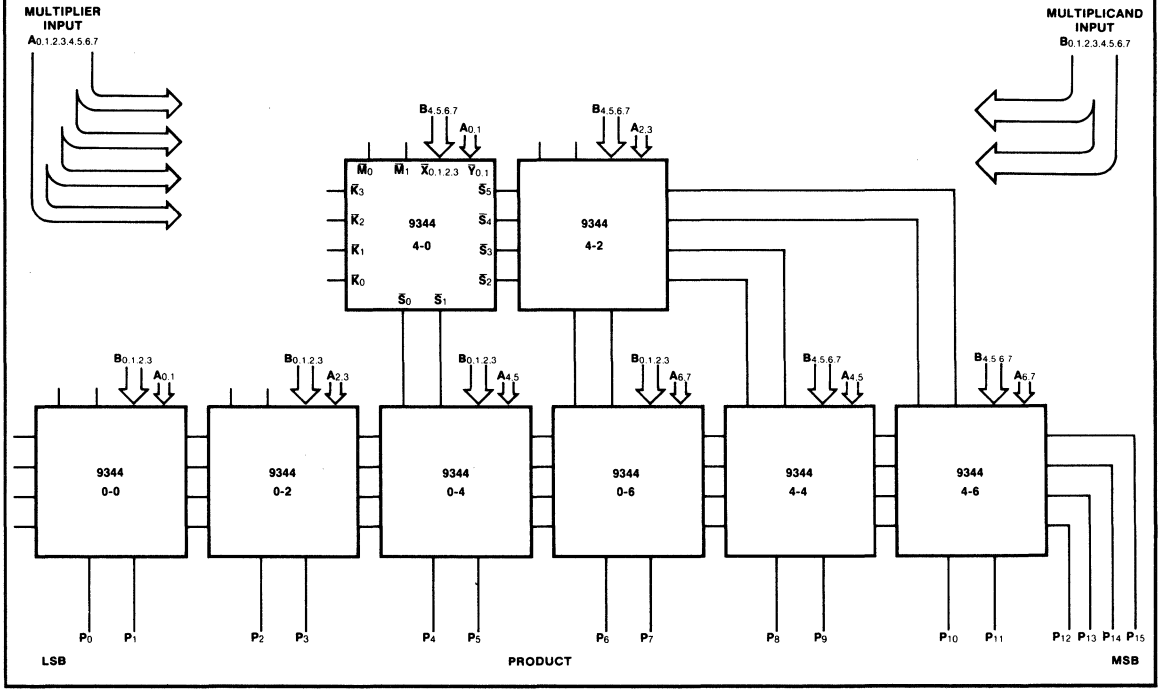
The '44 can be assembled in an iterative structure to perform multi-bit multiplication. The blocks are interconnected so that partial product sums generated in a particular '44 are applied, if necessary, to equal weight carry inputs ($\overline{K}_0 - \overline{K}_3$ or $\overline{M}_0$, $\overline{M}_1$) of succeeding stages.

In the active iteritive multiplication arrays shown, weighting factors of the carry and sums between '44's are indicated (i.e., $0 = 2^0$, $1 = 2^1$, $2 = 2^2$, etc.). Labels inside the blocks identify bits multipled in that block. For instance 0 — 0 refers to multiplicand bits $B_{0,1,2,3}$ and multiplier bits $A_{0,1}$, while 4 — 2 would represent multiplicant bits $B_{4,5,6,7}$ and multiplier bits $A_{2,3}$.

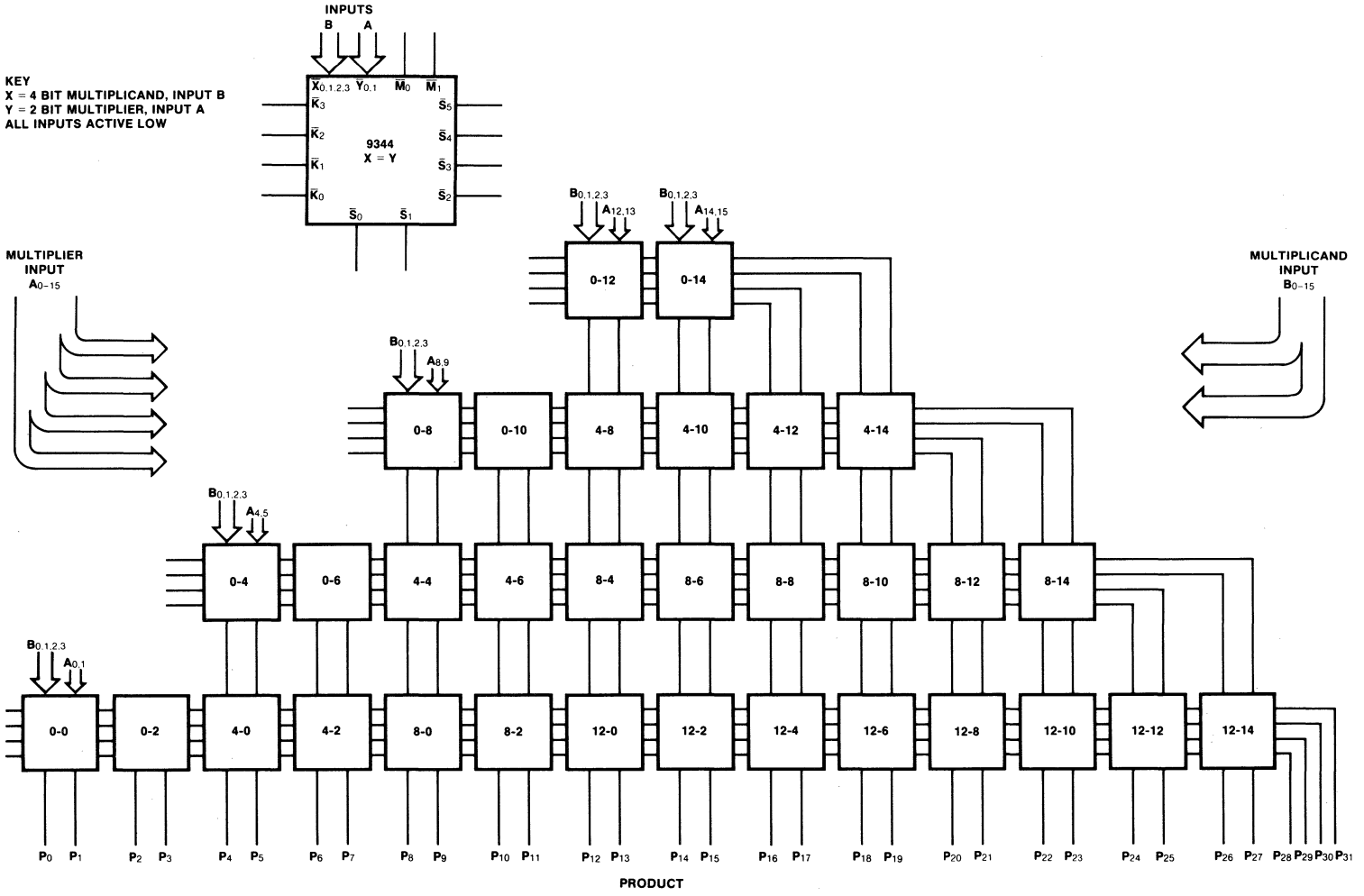
8-BIT BY 5-BIT MULTIPLICATION ARRAY



8-BIT BY 8-BIT MULTIPLICATION ARRAY

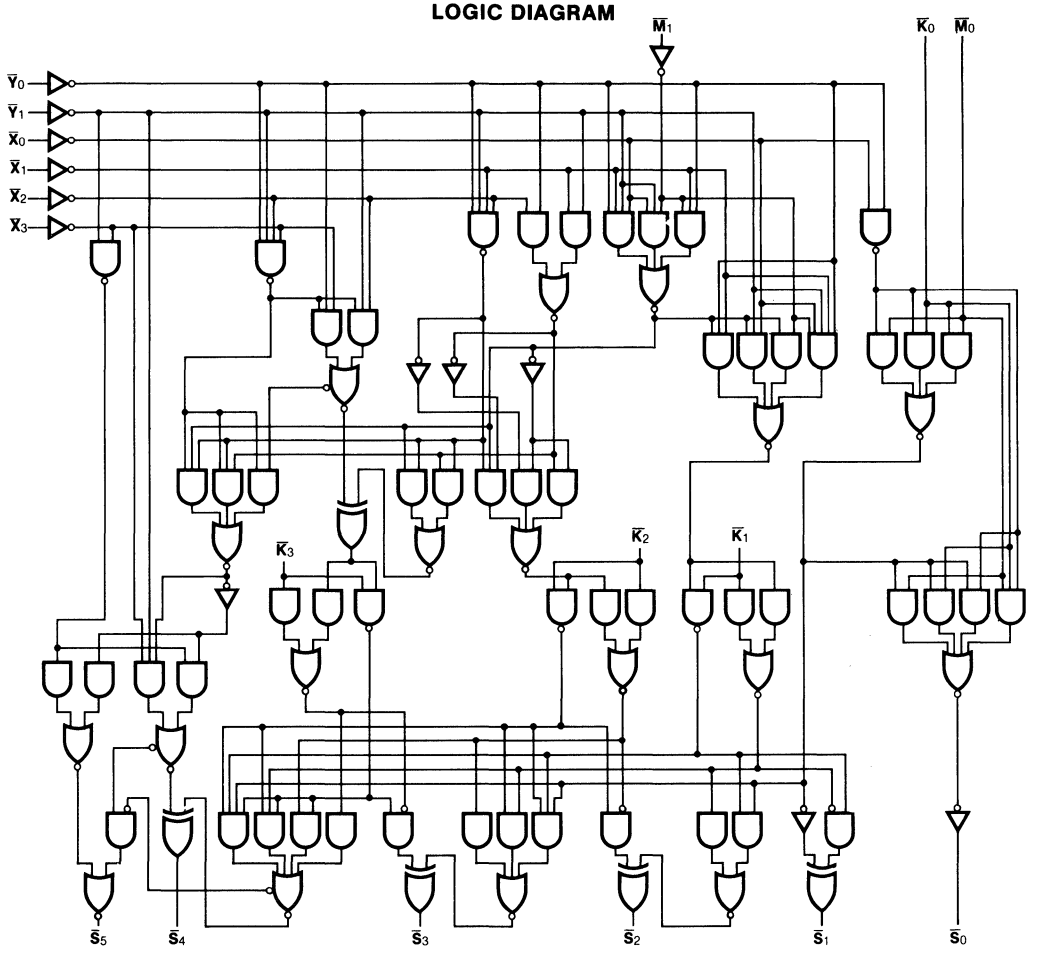


16-BIT BY 16-BIT MULTIPLICATION ARRAY



NOTE:
Each block represents one 9344. Labels inside the blocks identify bits multiplied in that block. The first number is the 4-bit B input, and the second number is the 2-bit A input. For instance, 12-0 refers to multiplicand bits $B_{12,13,14,15}$ and multiplier bits $A_{0,1}$.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		150	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF R_L = 400 Ω		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{M}_1$ to $\overline{S}_3$		51 52	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{K}_0$ to $\overline{S}_5$		22 39	ns	Figs. 3-1, 3-5

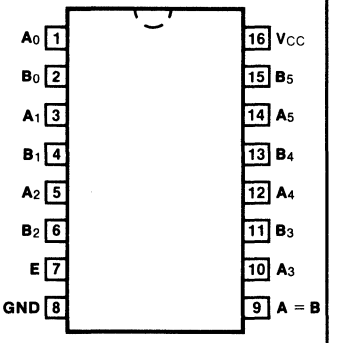
93S46

HIGH SPEED 6-BIT IDENTITY COMPARATOR

DESCRIPTION — The '46 is a very high speed 6-bit identity comparator. The device compares two words of up to six bits and indicates identity in less than 12 ns. It is easily expandable to any word length by using either serial or parallel expansion techniques. When the Enable input (E) is LOW, it forces the output LOW.

- **COMPARES TWO 6-BIT WORDS IN 12 ns**
- **EASILY EXPANDABLE TO ANY WORD SIZE**
- **ACTIVE HIGH ENABLE FOR FAST RIPPLE EXPANSION**

CONNECTION DIAGRAM
PINOUT A



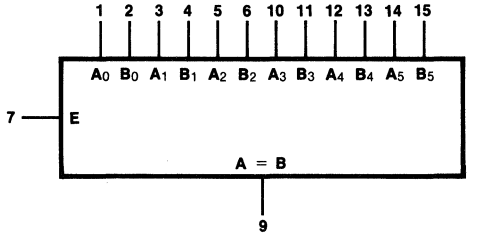
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	93S46PC		9B
Ceramic DIP (D)	A	93S46DC	93S46DM	6B
Flatpak (F)	A	93S46FC	93S46FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93S (U.L.) HIGH/LOW
A_0 — A_5	Word A Inputs	1.25/1.25
B_0 — B_5	Word B Inputs	1.25/1.25
E	Enable Input (Active HIGH)	1.25/1.25
A = B	A Equal to B Output	25/12.5

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '46 is a very high speed 6-bit identity comparator. The A = B output is HIGH when the Enable (E) is HIGH and the two 6-bit words are equal. Equality is determined by Exclusive-NOR circuits which individually compare the equivalent bits from each word. When any two of the equivalent bits from each word have different logic levels, the A = B output is LOW.

$$(A = B) = (\overline{A_0 \oplus B_0}) \bullet (\overline{A_1 \oplus B_1}) \bullet (\overline{A_2 \oplus B_2}) \bullet (\overline{A_3 \oplus B_3}) \bullet (\overline{A_4 \oplus B_4}) \bullet (\overline{A_5 \oplus B_5}) \bullet E$$

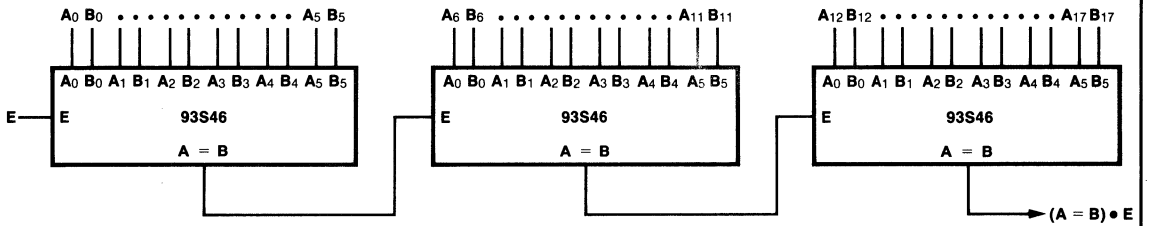
An active HIGH Enable (E) provides a means of fast ripple expansion. By connecting the A = B output of the first stage of the comparator to the enable of the next stage, the comparator can be expanded in 6-bit increments at an additional 4.5 ns per stage. An even faster expansion technique is achieved by connecting the A = B outputs to a Schottky NAND gate. This method compares two words of up to 78 bits each in 15 ns (typical) using the '133 13-input Schottky NAND gate.

TRUTH TABLE

INPUTS		OUTPUT
E	A_n, B_n	A = B
L	$A_n = B_n$	L
L	$A_n \neq B_n$	L
H	$A_n \neq B_n$	L
H	$A_n = B_n$	H

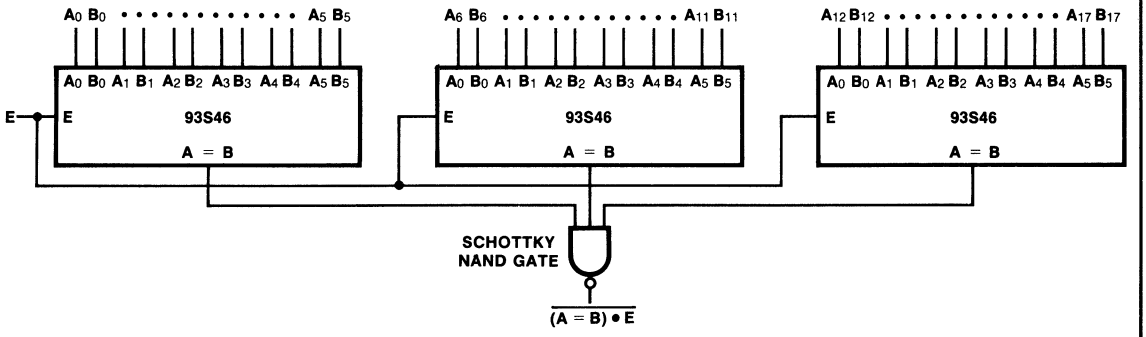
H = HIGH Voltage Level
L = LOW Voltage Level

RIPPLE EXPANSION



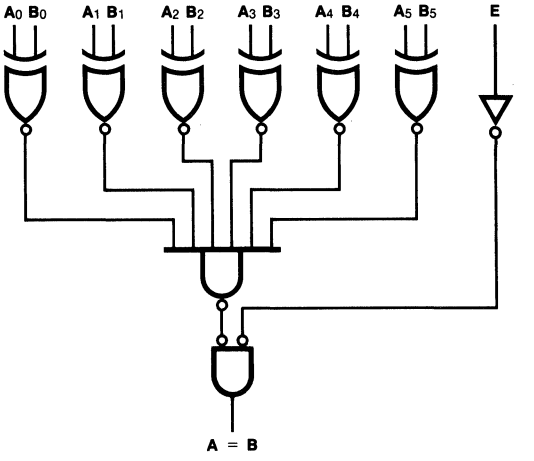
NOTE: This simple method of expansion adds 4.5 ns for each additional '46 used.

PARALLEL EXPANSION



NOTE: This method of expansion adds one gate delay (≈3 ns) to the '46, independent of the word length that is compared.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93S		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		70	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93S C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to A = B	3.0 3.0	17 17	ns	E = 4.5 V, Other Inputs = 4.5 V, Test each input individually, Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to A = B	3.0 3.0	14 15	ns	E = 4.5 V, Other Inputs = Gnd, Test each input individually, Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay E to A = B	2.0 2.0	10 10	ns	A_n = B_n Figs. 3-1, 3-5

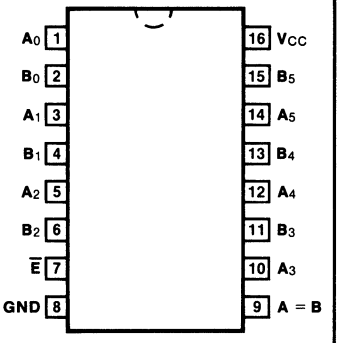
93S47

HIGH SPEED 6-BIT IDENTITY COMPARATOR

DESCRIPTION — The '47 is a very high speed 6-bit identity comparator. The device features an open-collector output for wired-OR expansion and active LOW Enable. The '47 is fabricated with the Schottky barrier diode process for high speed, and is completely compatible with all TTL families. This device is recommended for applications where wired-OR expansion is desired and the speed of an active pull-up is not required. The '47 is a pin-for-pin replacement for the DM7160/8160.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **COMPARE TWO 6-BIT WORDS IN 15 ns**
- **OPEN-COLLECTOR OUTPUT FOR WIRED-OR EXPANSION**

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

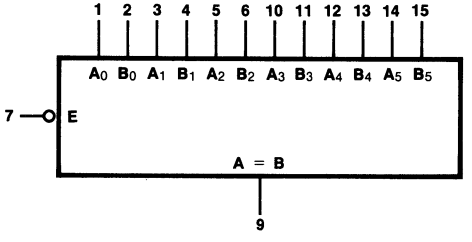
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	93S47PC		9B
Ceramic DIP (D)	A	93S47DC	93S47DM	6B
Flatpak (F)	A	93S47FC	93S47FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93S (U.L.) HIGH/LOW
$A_0 - A_5$	Word A Inputs	1.25/1.25
$B_0 - B_5$	Word B Inputs	1.25/1.25
$\overline{E}$	Enable Input (Active LOW)	1.25/1.25
A = B	A Equal to B Output	OC*/12.5

*OC — Open Collector

LOGIC SYMBOL

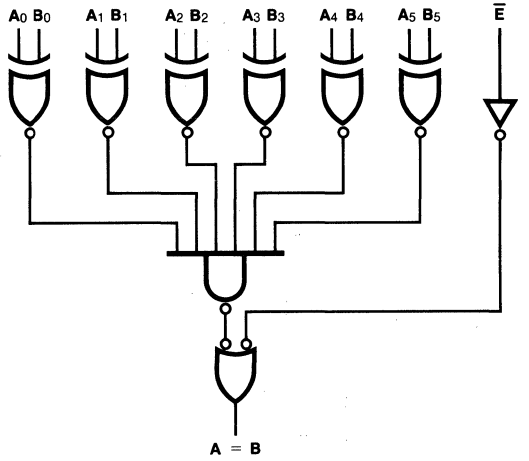


V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '47 is a very high speed 6-bit identity comparator. When enabled ($\overline{E}$ input LOW), the A = B output is HIGH if the two 6-bit words are equal. When disabled ($\overline{E}$ input HIGH), the A = B output is forced HIGH. Equality is determined by Exclusive-NOR circuits which individually compare the equivalent bits from each word. Since the A = B output state is determined by the equality of each pair of inputs, the equivalent A_n and B_n pins can be interchanged to facilitate board layout or wiring. The active LOW Enable ($\overline{E}$) can be used as a high speed strobe. When the Enable is HIGH, the A = B output is forced HIGH. This allows devices tied to a common wired-OR (actually wired-AND) node to be strobed individually or in groups. Only the enabled devices will determine the state of the output node.

$$(A = B) = \overline{E} + \overline{(A_0 \oplus B_0)} \bullet \overline{(A_1 \oplus B_1)} \bullet \overline{(A_2 \oplus B_2)} \bullet \overline{(A_3 \oplus B_3)} \bullet \overline{(A_4 \oplus B_4)} \bullet \overline{(A_5 \oplus B_5)}$$

LOGIC DIAGRAM



TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	A_n, B_n	A = B
L	$A_n = B_n$	H
L	$A_n \neq B_n$	L
H	$A_n \neq B_n$	H
H	$A_n = B_n$	H

H = HIGH Voltage Level
L = LOW Voltage Level

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93S		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		65	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93S C_L = 15 pF R_L = 280 Ω		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to A = B	5.0 5.0	17 17	ns	$\overline{E}$ = Gnd, Other Inputs = 4.5 V, Test each input individually, Figs. 3-2, 3-5
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to A = B	4.0 4.0	14 15	ns	$\overline{E}$ = Gnd, Other Inputs = Gnd, Test each input individually, Figs. 3-2, 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to A = B	3.0 3.0	10 10	ns	$A_n \neq B_n$ Figs. 3-2, 3-5

9348

12-INPUT PARITY CHECKER/GENERATOR

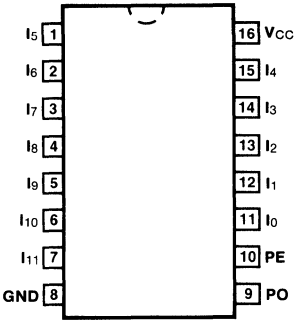
DESCRIPTION — The '48 is a 12-input parity checker/generator generating odd and even parity outputs. It can be used in high speed error detection applications.

- **BOTH ODD AND EVEN PARITY OUTPUTS PROVIDED**
- **GENERATES A PARITY BIT FOR UP TO 12 BITS**
- **CHECKS FOR PARITY ON UP TO 12 BITS**
- **EASILY EXPANDABLE**

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	9348PC		9B
Ceramic DIP (D)	A	9348DC	9348DM	6B
Flatpak (F)	A	9348FC	9348FM	4L

CONNECTION DIAGRAM
PINOUT A

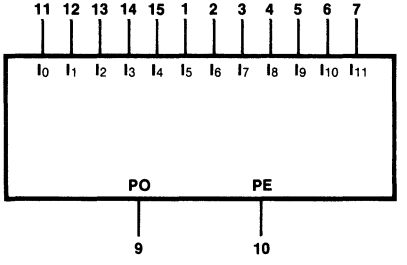


6

INPUT LOADING/FAN-OUT

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
I_0 — I_{11}	Parity Inputs	2.0/2.0
PO	Odd Parity Output	20/10
PE	Even Parity Output	20/10

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '48 is a 12-input parity generator. It provides odd and even parity for up to 12 data bits. The Even Parity output (PE) will be HIGH if an even number of logic ones are present on the inputs. The Odd Parity output (PO) will be HIGH if an odd number of logic ones are present on the inputs. The logic equations for the outputs are shown below.

$$PO = \overline{I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}}$$

$$PE = I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}$$

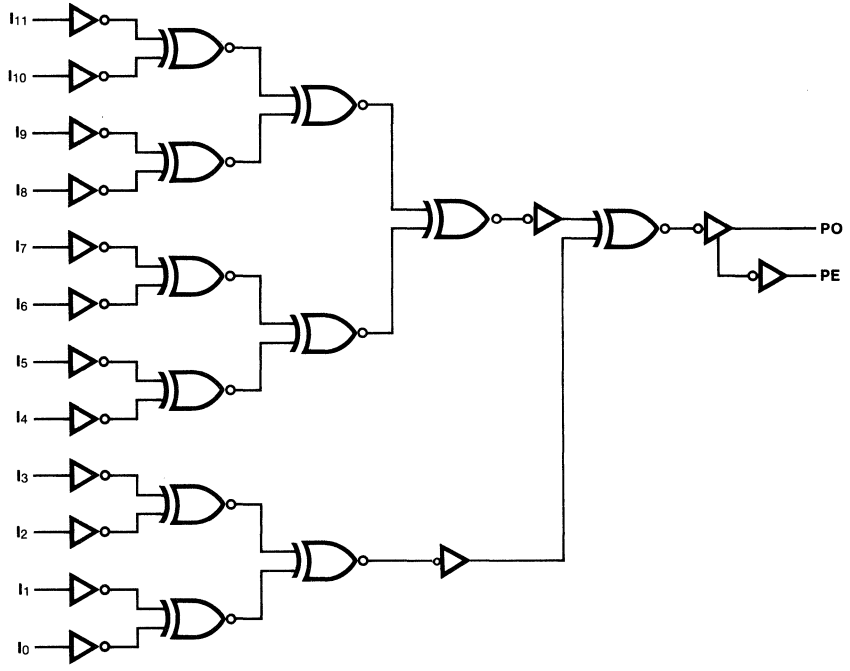
NOTE: Less through delay is encounted from the I_0, I_1, I_2, and I_3 inputs than I_4 thru I_{11} inputs. Therefore, if some signals are slower than others, the slower signals should be applied to these four inputs for maximum speed.

TRUTH TABLE

INPUTS		OUTPUTS	
$I_0 - I_{11}$		PO	PE
All Twelve	Inputs LOW	L	H
Any One	Input HIGH	H	L
Any Two	Inputs HIGH	L	H
Any Three	Inputs HIGH	H	L
Any Four	Inputs HIGH	L	H
Any Five	Inputs HIGH	H	L
Any Six	Inputs HIGH	L	H
Any Seven	Inputs HIGH	H	L
Any Eight	Inputs HIGH	L	H
Any Nine	Inputs HIGH	H	L
Any Ten	Inputs HIGH	L	H
Any Eleven	Inputs HIGH	H	L
Any Twelve	Inputs HIGH	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		82	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configuration)

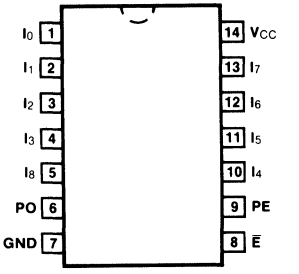
SYMBOL	PARAMETER	93XX C_L = 15 pF R_L = 400 Ω		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_4 to PO		46 42	ns	I_2, I_3, I_7, I_8 = Gnd; Other Inputs (exc. I_4) HIGH Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay I_4 to PE		51 48	ns	I_2, I_3, I_7, I_8 = Gnd; Other Inputs (exc. I_4) HIGH Figs. 3-1, 3-5
t_{PLH}	Propagation Delay I_3 to PO		27	ns	I_7 = HIGH; Other Inputs (exc. I_3) = Gnd Figs. 3-1, 3-4
t_{PHL}	Propagation Delay I_4 to PO		25	ns	All Inputs (exc. I_4) = Gnd Figs. 3-1, 3-5

6

93S62

9-INPUT PARITY CHECKER/GENERATOR

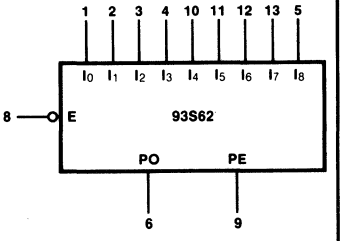
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '62 is a very high speed 9-input parity checker/generator for use in error detection and error correction applications. The '62 provides odd and even parity for up to nine data bits. The even parity output (PE) is HIGH if an even number of inputs are HIGH and $\overline{E}$ is LOW. The odd parity output (PO) will be HIGH if an odd number of inputs are HIGH and $\overline{E}$ is LOW. A HIGH level on the Enable ($\overline{E}$) input forces both outputs LOW.

- **INPUT-TO-OUTPUT DELAY 16 ns**
- **OUTPUT ENABLE TERMINAL**
- **BOTH ODD AND EVEN PARITY OUTPUTS PROVIDED**
- **GENERATES A PARITY BIT FOR UP TO NINE BITS**
- **CHECKS FOR PARITY ON UP TO NINE BITS**
- **EASILY EXPANDABLE**

LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	93S62PC		9A
Ceramic DIP (D)	A	93S62DC	93S62DM	6A
Flatpak (F)	A	93S62FC	93S62FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93S (U.L.) HIGH/LOW
$I_0 - I_8$	Data Inputs	1.25/1.0
$\overline{E}$	Output Enable (Active LOW)	2.5/2.0
PO	Odd Parity Output	25/12.5
PE	Even Parity Output	25/12.5

FUNCTIONAL DESCRIPTION — The '62 is a very high speed 9-input parity checker or generator. It is intended primarily for error detection in systems which transmit data in 8-bit bytes, but it can be expanded to any number of data inputs. Both even and odd parity outputs are available to allow maximum flexibility for both parity generation and parity checking. When the device is enabled ($\overline{E}$ = LOW), the Even Parity output (PE) is HIGH when an even number of inputs is HIGH, and the Odd Parity output (PO) is HIGH when an odd number of inputs is HIGH. The active LOW Enable ($\overline{E}$) controls the state of both outputs; when the Enable ($\overline{E}$) is HIGH, both outputs will be LOW. The Enable may be used to strobe the outputs at very high speeds to synchronize or inhibit the parity data.

The '62 has been designed with two sections using Exclusive-NOR comparison techniques. Eight data inputs I_0 thru I_7 represent one section which will generate a parity bit in 16 to 20 ns. The ninth input (I_8) bypasses three levels of logic and switches the outputs in 6.0 ns to 9.0 ns. This feature may be used to compensate for delayed arrival of the parity bit, allowing faster system cycle times *(Figure a)*. The fast I_8 input is also useful when more than nine bits are to be checked. The output of one '62 drives the I_8 input of a second '62 providing a 17-bit parity check in 29 ns (typ).

When some inputs of the '62 are not used, such as for words of less than nine bits or when using parallel expansion techniques, there is an optimum delay scheme for termination of the unused inputs (see Table II). In essence, if one of the inputs of any Exclusive-NOR stays HIGH, the delay from the other input to the output is minimized.

TRUTH TABLE
($\overline{E}$ = LOW)

Number of Inputs I_0 — I_8 that are HIGH	OUTPUTS	
	PO	PE
1, 3, 5, 7, 9	H	L
0, 2, 4, 6, 8	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

TABLE II — Termination Recommendations for Less Than Nine Bits

Number of Data Inputs	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8
3	D_0	L	D_1	L	D_2	L	L	L	L
4	D_0	L	D_1	L	D_2	L	D_3	L	L
5	D_0	L	D_1	L	D_2	L	D_3	L	D_4
6	D_0	D_1	D_2	D_3	D_4	L	D_5	L	L
7	D_0	D_1	D_2	D_3	D_4	L	D_5	L	D_6
8	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	L

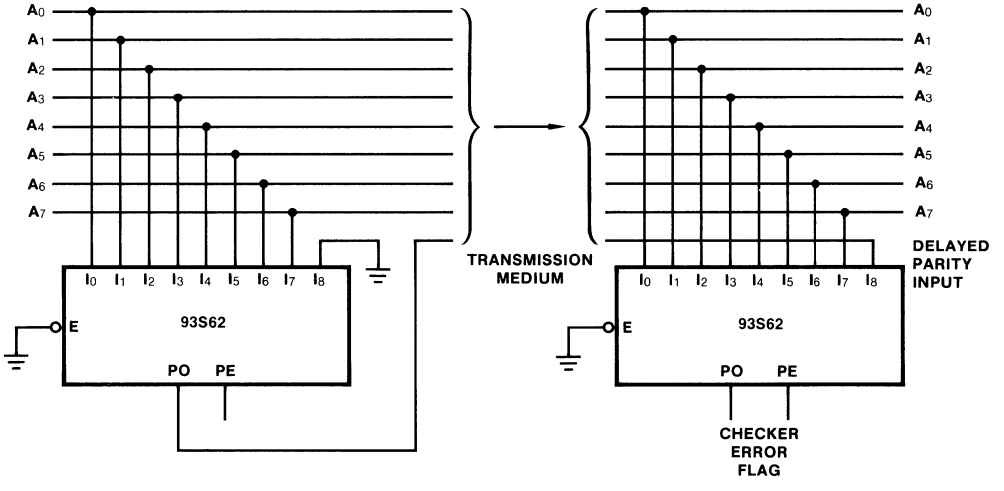
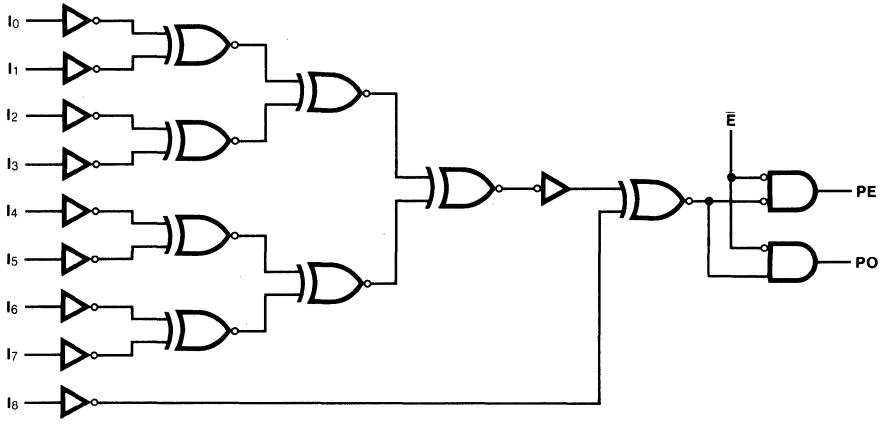


Fig. a Fast Input I_8 Allows Higher System Speed

LOGIC DIAGRAM



$PO = (I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8) \cdot \overline{E}$

$PE = \overline{(I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8)} \cdot \overline{E}$

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		93S Min	93S Max	UNITS	CONDITIONS
I_{IL}	Input LOW Current	$I_0 - I_8$		-1.6	mA	V_{CC} = Max, V_{IN} = 0.5 V
		$\overline{E}$		-3.2		
I_{CC}	Power Supply Current			65	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

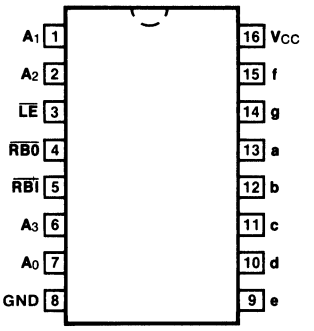
SYMBOL	PARAMETER	93S C_L = 15 pF Min	93S C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay $I_0 - I_7$ to PE		26 22	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay I_8 to PE		12 9.0	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $I_0 - I_7$ to PO		26 26	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay I_8 to PO		13 13	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to PE		7.0 7.0	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to PO		7.0 7.0	ns	Figs. 3-1, 3-4

9368

7-SEGMENT DECODER/DRIVER/LATCH

(Constant Current Source Outputs)

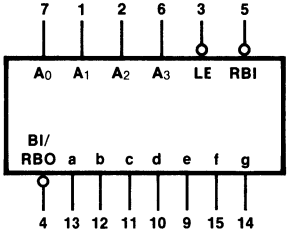
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '68 is a 7-segment decoder driver incorporating input latches and constant current output circuits to drive common cathode type LED displays directly.

- **HIGH SPEED INPUT LATCHES FOR DATA STORAGE**
- **DRIVES COMMON CATHODE LED DISPLAYS SUCH AS FND357 OR FND500 DIRECTLY**
- **ACTIVE LOW LATCH ENABLE FOR EASY INTERFACE WITH MSI CIRCUITS**
- **HEXADECIMAL DECODE FORMAT**
- **LATCH SPEED COMPARABLE TO STANDARD MSI LATCHES**
- **DATA INPUT FAN-IN ZERO WHEN LATCH NOT ENABLED**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROS AND/OR TRAILING EDGE ZEROS**
- **PINOUTS COMPARABLE WITH OTHER STANDARD MSI DECODERS SUCH AS 9307, 9317, 7446, 7447, 7448**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	PKG TYPE
Plastic DIP (P)	A	9368PC	9B
Ceramic DIP (D)	A	9368DC	6B

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
$A_0 - A_3$	Address (Data) Inputs	2.0/1.0*
$\overline{LE}$	Latch Enable Input (Active LOW)	1.0/1.0
$\overline{RBI}$	Ripple Blanking Input (Active LOW)	1.0/1.0
$\overline{RBO}$	Ripple Blanking as Output (Active LOW)	-/2.0
	as Input (Active LOW)	-/2.0
a — g	Segment Outputs (Active HIGH)	20 mA/"OFF"

*Except Loadings is 100 μA at 0.4 V when $\overline{LE}$ is HIGH.

FUNCTIONAL DESCRIPTION — The '68 is a 7-segment decoder driver designed to drive 7-segment common cathode LED displays such as the Fairchild FND357 or FND500 directly. The '68 drives any common cathode LED display rated at a nominal 20 mA at 1.7 V per segment without need for current limiting resistors.

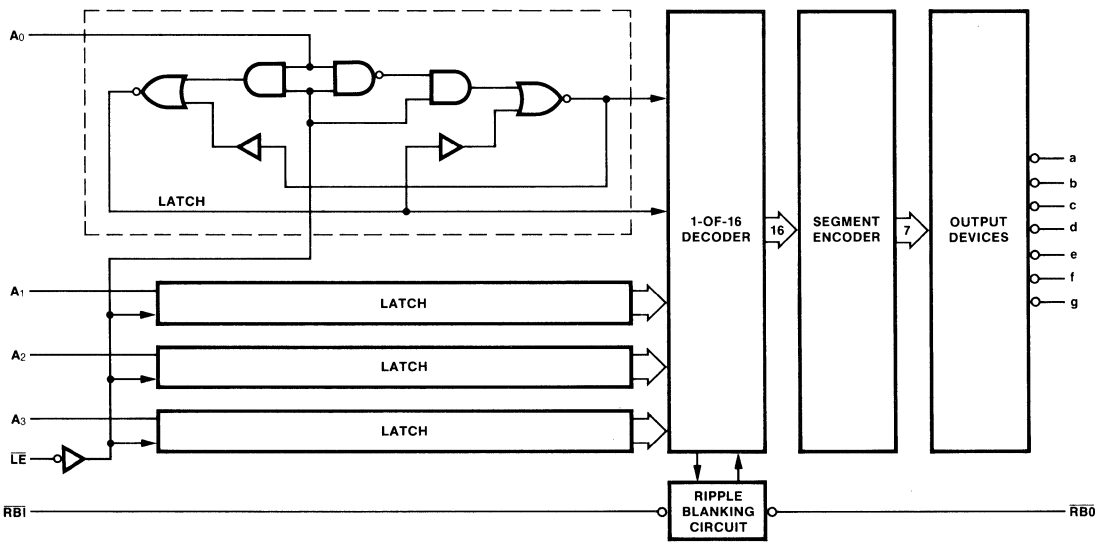
This device accepts a 4-bit binary code and produces output drive to the appropriate segments of the 7-segment display. It has a hexadecimal decode format which produces numeric codes "0" thru "9" and alpha codes "A" thru "F" using upper and lower case fonts.

Latches on the four data inputs are controlled by an active LOW latch enable $\overline{LE}$. When the $\overline{LE}$ is LOW, the state of the outputs is determined by the input data. When the $\overline{LE}$ goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable. The $\overline{LE}$ pulse width necessary to accept and store data is typically 30 ns which allows data to be strobed into the '68 at normal TTL speeds. This feature means that data can be routed directly from high speed counters and frequency dividers into the display without slowing down the system clock or providing intermediate data storage.

Another feature of the '68 is that the unit loading on the data inputs is very low (-100 μA Max) when the latch enable is HIGH. This allows '68s to be driven from an MOS device in multiplex mode without the need for drivers on the data lines.

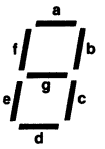
The '68 also has provision for automatic blanking of the leading and/or trailing edge zeros in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeros. The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

LOGIC DIAGRAM



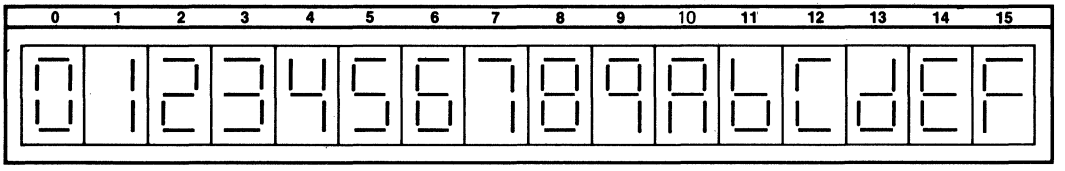
TRUTH TABLE

BINARY STATE	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	A_3	A_2	A_1	A_0	a	b	c	d	e	f	g	$\overline{RBO}$	
—	H	*	X	X	X	X	← STABLE →							H	STABLE
0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	BLANK
0	L	H	L	L	L	L	H	H	H	H	H	H	L	H	0
1	L	X	L	L	L	H	L	H	H	L	L	L	L	H	1
2	L	X	L	L	H	L	H	H	L	H	H	L	H	H	2
3	L	X	L	L	H	H	H	H	H	H	L	L	H	H	3
4	L	X	L	H	L	L	L	H	H	L	L	H	H	H	4
5	L	X	L	H	L	H	H	L	H	H	L	H	H	H	5
6	L	X	L	H	H	L	H	L	H	H	H	H	H	H	6
7	L	X	L	H	H	H	H	H	H	L	L	L	L	H	7
8	L	X	H	L	L	L	H	H	H	H	H	H	H	H	8
9	L	X	H	L	L	H	H	H	H	L	L	H	H	H	9
10	L	X	H	L	H	L	H	H	H	L	H	H	H	H	A
11	L	X	H	L	H	H	L	L	H	H	H	H	H	H	b
12	L	X	H	H	L	L	H	L	L	H	H	H	L	H	C
13	L	X	H	H	L	H	L	H	H	H	H	L	H	H	d
14	L	X	H	H	H	L	H	L	L	H	H	H	H	H	E
15	L	X	H	H	H	H	H	L	L	L	H	H	H	H	F
X	X	X	X	X	X	X	L	L	L	L	L	L	L	L**	BLANK

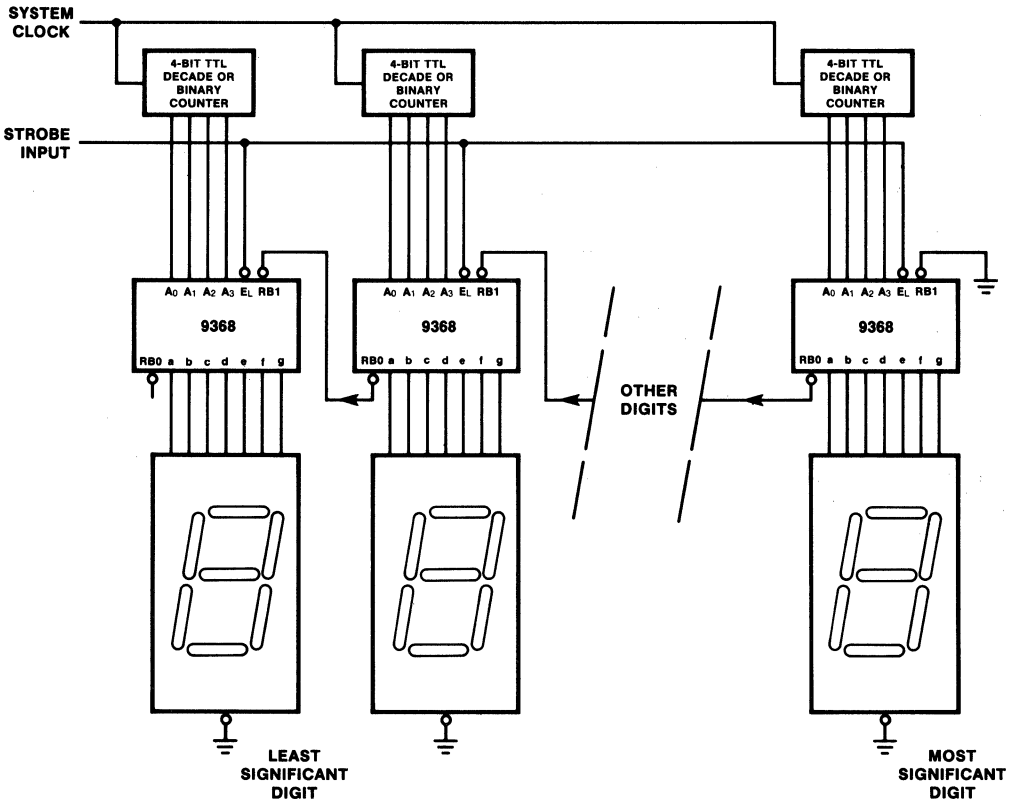


*The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.
**The $\overline{RBO}$ used as an input overrides all other input conditions.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

NUMERICAL DESIGNATIONS

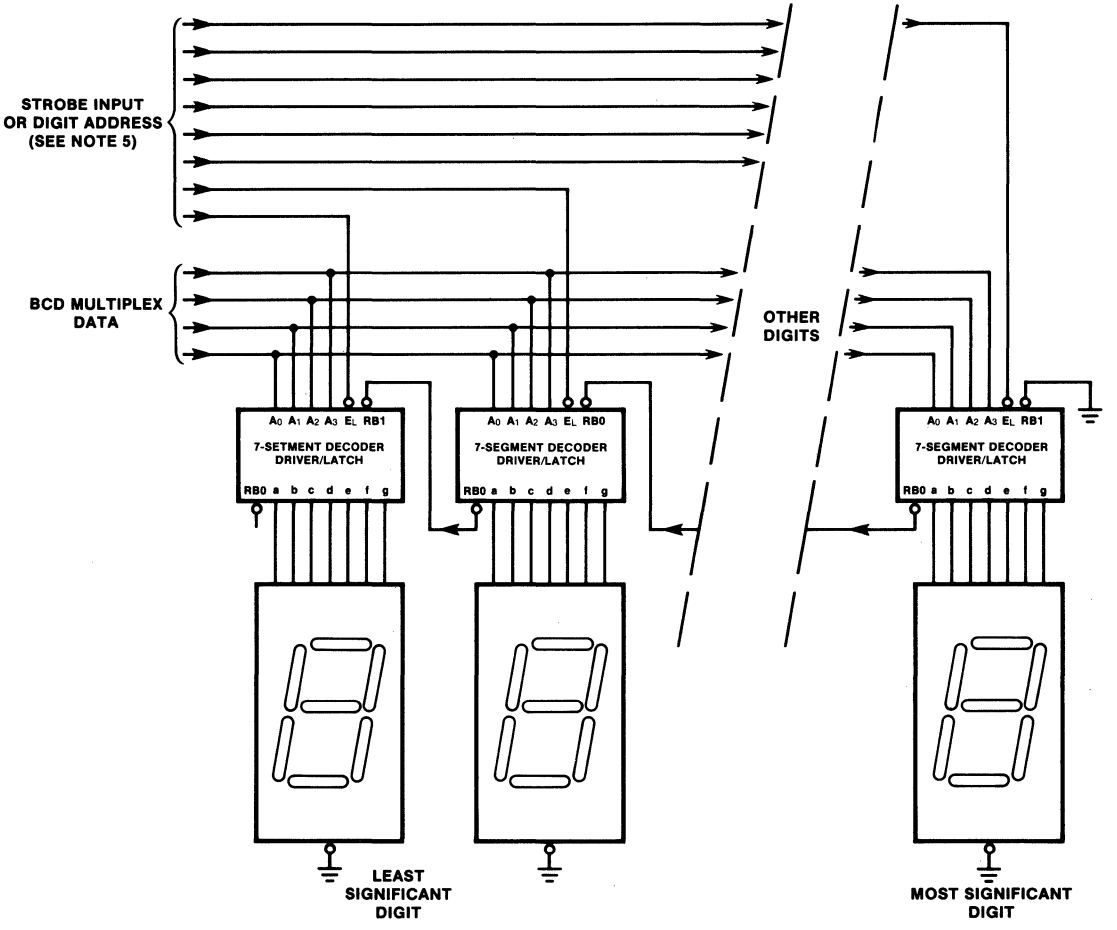


PARALLEL DATA DISPLAY SYSTEM WITH RIPPLE BLANKING



COMMON CATHODE LED DISPLAY,
SUCH AS FAIRCHILD FND357
OR FND500

DISPLAY DEMULTIPLEXING SYSTEM WITH RIPPLE BLANKING



COMMON CATHODE LED DISPLAY,
SUCH AS FAIRCHILD FND357
OR FND500

NOTE:
Digit address data must be non-overlapping. Standard TTL decoders like the 9301, 9311, 7442 or 74155 must be strobed, since the address decoding glitches could cause erroneous data to be strobed into the latches.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		Min	Max		
I_{OH}	Segment Output HIGH Current	-16	-22	mA	V_{CC} = 5.0 V, V_{OUT} = 1.7 V, T_A = +25°C
I_{OL}	Segment Output LOW Current	-250	250	μA	V_{CC} = 5.0 V, V_{OUT} = 1.7 V
I_{CC}	Power Supply Current		67	mA	V_{CC} = Max, Outputs Open, Data & Latch Inputs = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF R_L = 100 Ω		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to a—g		50 75	ns	Fig. 3-21
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$ to a—g		70 90	ns	Fig. 3-9

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

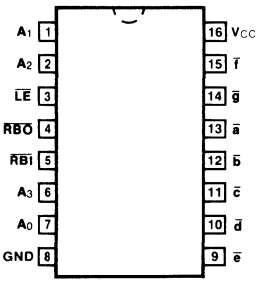
SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		Min	Max		
t_s (H)	Setup Time HIGH A_n to $\overline{LE}$	30		ns	Fig. 3-13
t_h (H)	Hold Time HIGH A_n to $\overline{LE}$	0		ns	Fig. 3-13
t_s (L)	Setup Time LOW A_n to $\overline{LE}$	20		ns	Fig. 3-13
t_h (L)	Hold Time LOW A_n to $\overline{LE}$	0		ns	Fig. 3-13
t_w (L)	$\overline{LE}$ Pulse Width LOW	45		ns	Fig. 3-8

9370

7-SEGMENT DECODER/DRIVER/LATCH

(With Open-Collector Outputs)

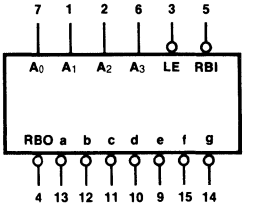
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '70 is a 7-segment decoder driver incorporating input latches and output circuits to directly drive incandescent displays. It can also be used to drive common anode LED displays in either a multiplexed mode or directly with the aid of external current limiting resistors.

- **HIGH SPEED INPUT LATCHES FOR DATA STORAGE**
- **25 mA SINK CAPABILITY TO DRIVE EITHER INCANDESCENT OR COMMON ANODE LED DISPLAYS**
- **HEXADECIMAL DECODE FORMAT**
- **ACTIVE LOW LATCH ENABLE FOR EASY INTERFACE WITH MSI CIRCUITS**
- **DATA INPUT LOADING ESSENTIALLY ZERO WHEN LATCH IS DISABLED**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING AND/OR TRAILING-EDGE ZEROES**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	PKG TYPE
Plastic DIP (P)	A	9370PC	9B
Ceramic DIP (D)	A	9370DC	6B

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	2.0/1.0**
$\overline{LE}$	Latch Enable Input (Active LOW)	1.0/1.0
$\overline{RBI}$	Ripple Blanking Input (Active LOW)	1.0/1.0
$\overline{RBO}$	Ripple Blanking as Output (Active LOW)	2.0/2.0
	as Input (Active LOW)	–/2.0
$\overline{a} - \overline{g}$	Segment Outputs (Active LOW)	OC*/25 mA

*OC — Open Collector
**Except Loading is 100 μA @ 0.4 V when $\overline{LE}$ is HIGH.

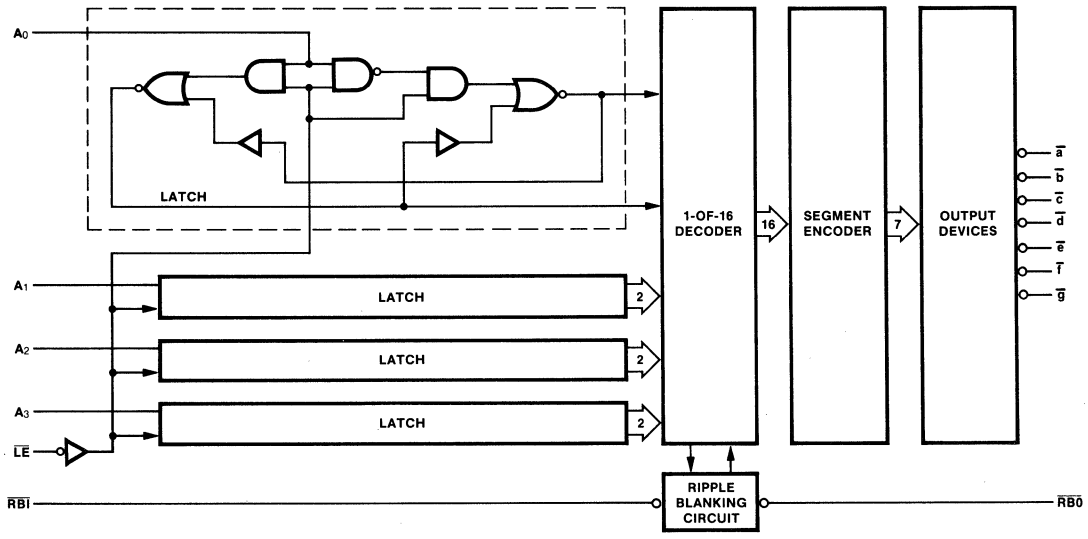
FUNCTIONAL DESCRIPTION — The '70 has active LOW outputs capable of sinking in excess of 25 mA which allows it to drive a wide variety of 7-segment incandescent displays directly. It may also be used to drive common anode LED displays, multiplexed or directly with the aid of suitable current limiting resistors. This device accepts a 4-bit binary code and produces output drive to the appropriate segments of the 7-segment display. It has a hexadecimal decode format which produces numeric codes "0" through "9" and alpha codes "A" through "F" using upper and lower case fonts.

Latches on the four data inputs are controlled by an active LOW latch enable $\overline{LE}$. When the $\overline{LE}$ is LOW, the state of the outputs is determined by the input data. When the $\overline{LE}$ goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable. The $\overline{LE}$ pulse width necessary to accept and store data is typically 30 ns which allows data to be strobed into the '70 at normal TTL speeds. This feature means that data can be routed directly from high speed counters and frequency dividers into the display without slowing down the system clock or providing intermediate data storage.

The latch/decoder combination is a simple system which drives incandescent displays with multiplexed data inputs from MOS time clocks, DVMs, calculator chips, etc. Data inputs are multiplexed while the displays are in static mode. This lowers component and insertion costs since several circuits — seven diodes per display, strobe drivers, a separate display voltage source, and clock failure detect circuits — traditionally found in incandescent multiplexed display systems are eliminated. It also allows low strobing rates to be used without display flicker.

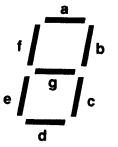
Another '70 feature is the reduced loading on the data inputs when the Latch Enable is HIGH (only 10 μA typ). This allows many '70s to be driven from a MOS device in multiplex mode without the need for drivers on the data lines. The '70 also provides automatic blanking of the leading and/or trailing-edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an 8-digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading-edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing-edge zeroes. The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

LOGIC DIAGRAM



TRUTH TABLE

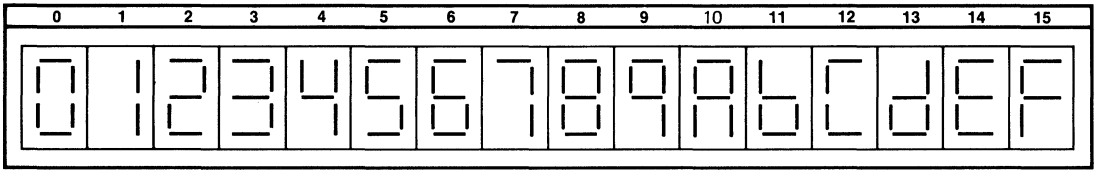
BINARY STATE	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	A_3	A_2	A_1	A_0	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	$\overline{RBO}$	
—	H	*	X	X	X	X	◄			STABLE			►	H	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	H	1
2	L	X	L	L	H	L	L	L	H	L	L	H	L	H	2
3	L	X	L	L	H	H	L	L	L	L	H	H	L	H	3
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	4
5	L	X	L	H	L	H	L	H	L	L	H	L	L	H	5
6	L	X	L	H	H	L	L	H	L	L	L	L	L	H	6
7	L	X	L	H	H	H	L	L	L	H	H	H	H	H	7
8	L	X	H	L	L	L	L	L	L	L	L	L	L	H	8
9	L	X	H	L	L	H	L	L	L	H	H	L	L	H	9
10	L	X	H	L	H	L	L	L	L	H	L	L	L	H	8
11	L	X	H	L	H	H	H	H	L	L	L	L	L	H	8
12	L	X	H	H	L	L	L	H	H	L	L	L	H	H	C
13	L	X	H	H	L	H	H	L	L	L	L	H	L	H	d
14	L	X	H	H	H	L	L	H	H	L	L	L	L	H	E
15	L	X	H	H	H	H	L	H	H	H	L	L	L	H	F
X	X	X	X	X	X	X	H	H	H	H	H	H	H	L**	BLANK



*The $\overline{RBI}$ will blank the display only if binary zero is stored in the latches.
**$\overline{RBO}$ used as an input overrides all other input conditions.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

NUMERICAL DESIGNATION



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYBMOL	PARAMETER		93XX Min	93XX Max	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	$\overline{RBO}$	2.4		V	V_{CC} = Min, I_{OH} -80 μA
V_{OL}	Output LOW Voltage	$\overline{RBO}$		0.4	V	I_{OL} = 3.2 mA; V_{CC} = Min
		$\overline{a}-\overline{g}$		0.4		I_{OL} = 25 mA; V_{CC} = Min
I_{OH}	Output HIGH Current, $\overline{a}-\overline{g}$			250	μA	V_{CC} = Max, V_{OUT} = 5.5 V
I_{CC}	Power Supply Current			105	mA	A_1, A_2, A_3, $\overline{LE}$ = Gnd; V_{CC} = Max, Outputs Open
				94		A_0, A_1, A_2, $\overline{LE}$ = Gnd; V_{CC} = Max, Outputs Open

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF, R_L = 500 Ω Min	93XX C_L = 15 pF, R_L = 500 Ω Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{a}-\overline{g}$		75 50	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$ to $\overline{a}-\overline{g}$		90 70	ns	Figs. 3-1, 3-9

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

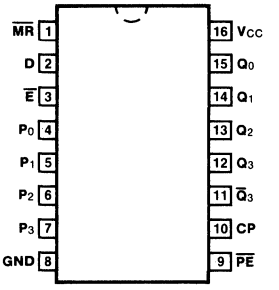
SYMBOL	PARAMETER	93XX Min	93XX Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to $\overline{LE}$		30 20	ns	Fig. 3-13
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n to $\overline{LE}$		0 0	ns	Fig. 3-13
t_w (L)	$\overline{LE}$ Pulse Width LOW		45	ns	Fig. 3-9

93H72

HIGH SPEED 4-BIT SHIFT REGISTER

(With Enable)

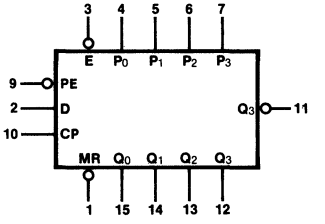
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '72 high speed 4-bit shift register is a multifunctional sequential logic block which is useful in a wide variety of register applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial and parallel-parallel data transfers. The '72 has three synchronous modes of operation: shift, parallel load and hold (do nothing). The hold capability permits information storage in the register independent of the clock.

- **60 MHz TYPICAL SHIFT FREQUENCY**
- **SYNCHRONOUS PARALLEL DATA ENTRY**
- **DATA HOLD (DO NOTHING) INDEPENDENT OF CLOCK**
- **FULLY SYNCHRONOUS, EDGE-TRIGGERED**
- **ASYNCHRONOUS MASTER RESET**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	93H72PC		9B
Ceramic DIP (D)	A	93H72DC	93H72DM	6B
Flatpak (F)	A	93H72FC	93H72FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93H (U.L.) HIGH/LOW
$\overline{E}$	Enable Input (Active LOW)	2.0/2.0
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0
CP	Clock Pulse Input	2.0/2.0
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0
D	Serial Data Input	1.0/1.0
$Q_0 - Q_3$	Parallel Outputs	20/10
$\overline{Q}_3$	Last Stage Complementary Output	20/10

FUNCTIONAL DESCRIPTION — The '72 is a 4-bit shift register with three modes of operation: shift, parallel load and hold (do nothing). The register is fully synchronous with any output change occuring after the rising clock edge. The '72 features edge-triggered type characteristics on all inputs (except $\overline{MR}$) which means there are no restrictions on the activity of these inputs ($\overline{PE}$, $\overline{E}$, $P_0 - P_3$, D) for logic operation except for the setup requirements prior to the LOW-to-HIGH clock transition.

The mode of operation of the '72 is determined by the two inputs, Parallel Enable ($\overline{PE}$) and Enable ($\overline{E}$) as shown in Table 1. The active LOW Enable when HIGH, places the register in the hold mode with the register flip-flops retaining their information. When the Enable is activated (LOW) the Parallel Enable ($\overline{PE}$) determines whether the register operates in a shift or parallel data entry mode.

When the Enable is LOW and the Parallel Enable input is LOW the parallel inputs are selected and will determine the next condition of the register synchronously with the clock as shown in Table II. In this mode the element appears as four common clocked D flip-flops. With $\overline{E}$ LOW and the $\overline{PE}$ input HIGH the device acts as a 4-bit shift register with serial data entry through the D input shown in Table III. In both cases the next state of the flip-flops occurs after the LOW-to-HIGH transition of the clock input.

The asynchronous active LOW Master Reset overrides all inputs and clears the register forcing outputs $Q_0 - Q_3$ LOW and $\overline{Q}_3$ HIGH. To provide for left shift operation, P_3 is used as the serial data input and Q_0 is the serial data output. The other outputs are tied back to the previous parallel inputs, with Q_3 tied to P_2, Q_2 tied to P_1 and Q_1 tied to P_0.

LOGIC DIAGRAM

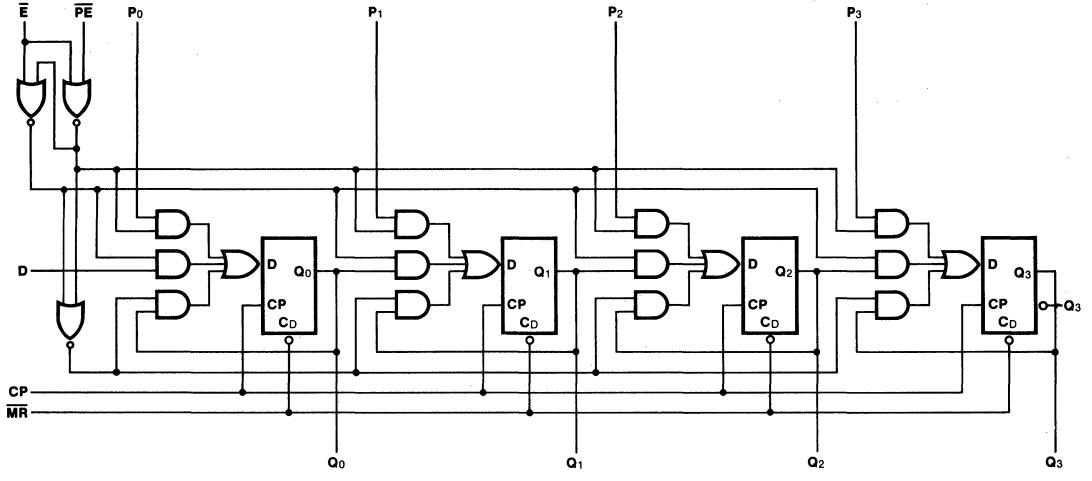


TABLE I. MODE SELECT TABLE

MODE		$\overline{MR}$	$\overline{E}$	$\overline{PE}$	P_0	P_1	P_2	P_3	D
Synchronous	Parallel Load	H	L	L	Parallel Data Entry				X
	Serial Shift	H	L	H	X	X	X	X	Serial Data Entry
	Hold	H	H	L	X	X	X	X	X
	Hold	H	H	H	X	X	X	X	X
Asynchronous	Reset	L	X	X	All Outputs Set LOW ($\overline{Q}_3$ = HIGH)				

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

TABLE II.
PARALLEL DATA ENTRY

$P_0 - P_3$ INPUT @ t_n	Q @ t_{n+1}
L	L
H	H

TABLE III.
SERIAL DATA ENTRY

D INPUT @ t_n	Q_0 @ t_{n+1}
L	L
H	H

t_n = Present State
t_{n+1} = State after next clock
H = HIGH Voltage Level
L = LOW Voltage Level

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		93H Min	93H Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current		-30	-100	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current	XM		120	mA	V_{CC} = Max
		XC		135		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93H C_L = 15 pF Min	93H C_L = 15 pF Max	UNITS	CONDITIONS
f_{max}	Maximum Shift Frequency	45		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		16 21	ns	Figs. 3-1, 3-8
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		26	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

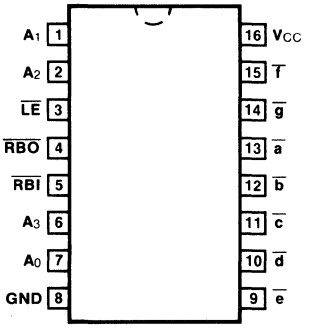
SYMBOL	PARAMETER	93H Min	93H Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW D or P_n to CP	7.0		ns	Fig. 3-6
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{E}$ to CP	17			
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{PE}$ to CP	19		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D, P_n, $\overline{E}$ or $\overline{PE}$ to CP	0			
t_w (L)	$\overline{MR}$ Pulse Width LOW	19		ns	Fig. 3-16
t_{rec}	$\overline{MR}$ Recovery Time	7.0			

9374

7-SEGMENT DECODER/DRIVER/LATCH

(With Constant Current Sink Outputs)

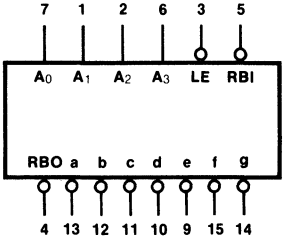
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '74 is a 7-segment decoder driver incorporating input latches and output circuits to directly drive common anode LED displays.

- **HIGH SPEED INPUT LATCHES FOR DATA STORAGE**
- **15 mA CONSTANT CURRENT SINK CAPABILITY TO DIRECTLY DRIVE COMMON ANODE LED DISPLAYS**
- **INCREASES INCANDESCENT DISPLAY LIFE**
- **ACTIVE LOW LATCH ENABLE FOR EASY INTERFACE WITH MSI CIRCUITS**
- **DATA INPUT LOADING ESSENTIALLY ZERO WHEN LATCH DISABLED**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING AND/OR TRAILING-EDGE ZEROES**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	PKG TYPE
Plastic DIP (P)	A	9374PC	9B
Ceramic DIP (D)	A	9374DC	6B

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
$A_0 - A_3$	Address (Data) Inputs	1.0/0.25**
$\overline{LE}$	Latch Enable Input (Active LOW)	0.5/0.25
$\overline{RBI}$	Ripple Blanking Input (Active LOW)	0.5/0.25
$\overline{RBO}$	Ripple Blanking as Output (Active LOW)	1.0/0.5
	as Input (Active LOW)	-/0.75
$\overline{a} - \overline{g}$	Constant Current Outputs (Active LOW)	OC*/15 mA

*OC — Open Collector
**Except Loading is 10 μA @ 0.4 V when $\overline{LE}$ is HIGH.

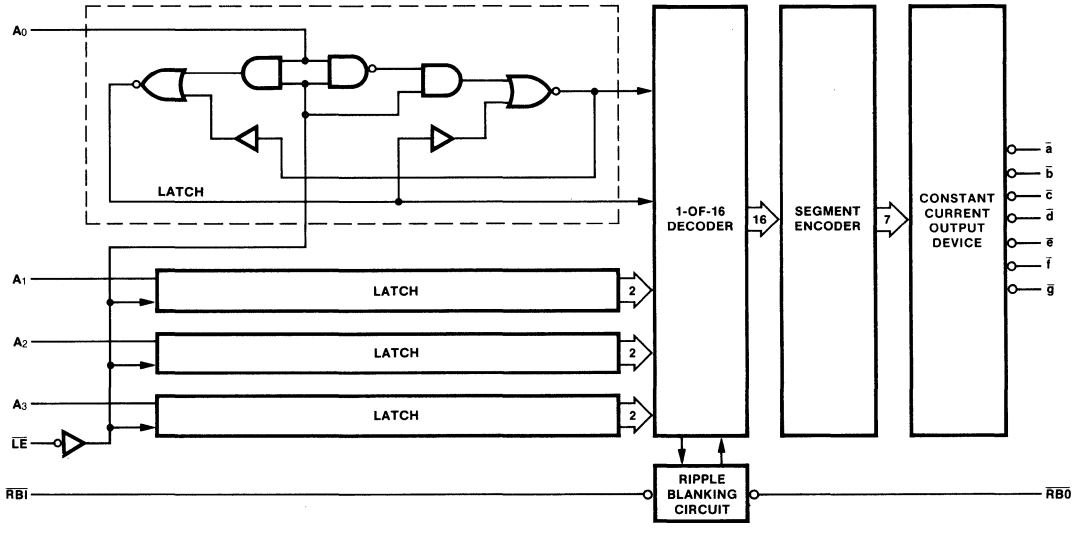
FUNCTIONAL DESCRIPTION—The '74 is a 7-segment deconder/driver with latches on the address inputs and active LOW constant current outputs to drive LEDs directly. This device accepts a 4-bit binary code and produces output drive to the appropriate segments of the 7-segment display. It has a decode format which produces numeric codes "0" through "9" and other codes.

Latches on the four data inputs are controlled by an active LOW Latch Enable, $\overline{LE}$. When $\overline{LE}$ is LOW, the state of the outputs is determined by the input data. When $\overline{LE}$ goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable. The $\overline{LE}$ pulse width necessary to accept and store data is typically 50 ns, which allows data to be strobed into the '74 at normal TTL speeds. This feature means that data can be routed directly from high speed counters and frequency dividers into the display without slowing down the system clock or providing intermediate data storage.

The latch/decoder combination is a simple system which drives LED displays with multiplexed data inputs from MOS time clocks, DVMs, calculator chips, etc. Data inputs are multiplexed while the displays are in static mode. This lowers component and insertion costs, since several circuits — seven resistors per display, strobe drivers, a separate display voltage source, and clock failure detect circuits — traditionally found in multiplexed display systems are eliminated. It also allows low strobing rates to be used without display flicker.

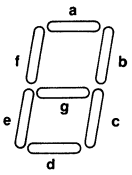
Another '74 feature is the reduced loading on the data inputs when the Latch Enable is HIGH (only 10 μA typ). This allows many '74s to be driven from a MOS device in multiplex mode without the need for drivers on the data lines. The '74 also provides automatic blanking of the leading and/or trailing-edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an 8-digit mixed integer fraction decimal representation, using the automatic blanking capability 0060.0300 would be displayed as 60.03. Leading-edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar precedure for the fractional part of a display will provide automatic suppression of trailing-edge zeros. The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

LOGIC DIAGRAM



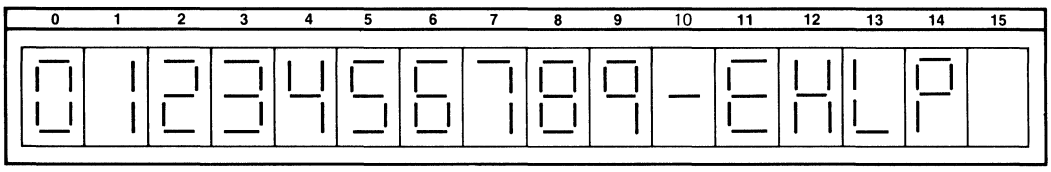
TRUTH TABLE

BINARY STATE	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	A_3	A_2	A_1	A_0	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	$\overline{RBO}$	
—	H	*	X	X	X	X	←			STABLE			→	H	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	H	1
2	L	X	L	L	H	L	L	L	H	L	L	H	L	H	2
3	L	X	L	L	H	H	L	L	L	L	H	H	L	H	3
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	4
5	L	X	L	H	L	H	L	H	L	L	H	L	L	H	5
6	L	X	L	H	H	L	L	H	L	L	L	L	L	H	6
7	L	X	L	H	H	H	L	L	L	H	H	H	H	H	7
8	L	X	H	L	L	L	L	L	L	L	L	L	L	H	8
9	L	X	H	L	L	H	L	L	L	L	H	L	L	H	9
10	L	X	H	L	H	L	H	H	H	H	H	H	L	H	-
11	L	X	H	L	H	H	L	H	H	L	L	L	L	H	E
12	L	X	H	H	L	L	H	L	L	H	L	L	L	H	H
13	L	X	H	H	L	H	H	H	H	L	L	L	H	H	L
14	L	X	H	H	H	L	L	L	H	H	L	L	L	H	P
15	L	X	H	H	H	H	H	H	H	H	H	H	H	H	BLANK
X	X	X	X	X	X	X	H	H	H	H	H	H	H	L**	BLANK



*The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.
**$\overline{RBO}$ used as an input overrrides all other input conditions.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

NUMERICAL DESIGNATIONS



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		93XX Min	93XX Max	UNITS	CONDITIONS
V_{OUT}	Output Voltage, Applied	OFF		10 (Fig. a)	V	Separate LED Supply
		ON				
I_{OL}	Output LOW Current, $\overline{a}$—$\overline{g}$		12	18	mA	V_{CC} = 5.0 V, V_{OL} = 3.0 V T_A = 25°C
I_{OH}	Output HIGH Current $\overline{a}$—$\overline{g}$			250	μA	V_{CC} = Max, V_{OUT} = 5.5 V
I_{CC}	Power Supply Current			50	mA	V_{CC} = Max, V_{IN} = Gnd V_{OUT} = 3.0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF R_L = 1 kΩ Min	93XX C_L = 15 pF R_L = 1 kΩ Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{a}$—$\overline{g}$		140 140	ns	Figs. 3-2, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$ to $\overline{a}$—$\overline{g}$		140 140	ns	Figs. 3-2, 3-9

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	93XX Min	93XX Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to $\overline{LE}$	75 30		ns	Fig. 3-13
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n to $\overline{LE}$	0 0		ns	
t_w (L)	$\overline{LE}$ Pulse Width LOW	85		ns	Fig. 3-9

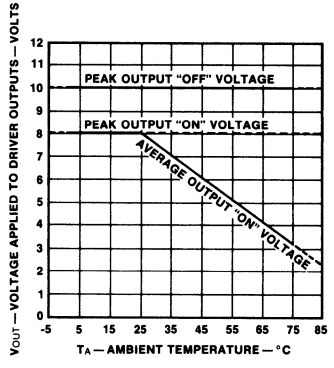


Fig. a Output Voltage Safe Operating Area

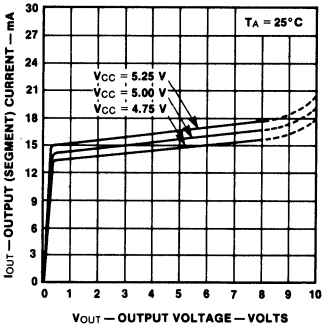


Fig. b Typical Constant Segment Current Versus Output Voltage

APPLICATIONS — It is possible with common anode 7-segment LED displays and constant current sink decoder drivers to save substantial amounts of power by carefully choosing operating points on display supply voltage. First, examine the power used in the normal display driving method where the display and decoder driver are both operated from a +5.0 V regulated supply ($V_{CC} = V_S$).

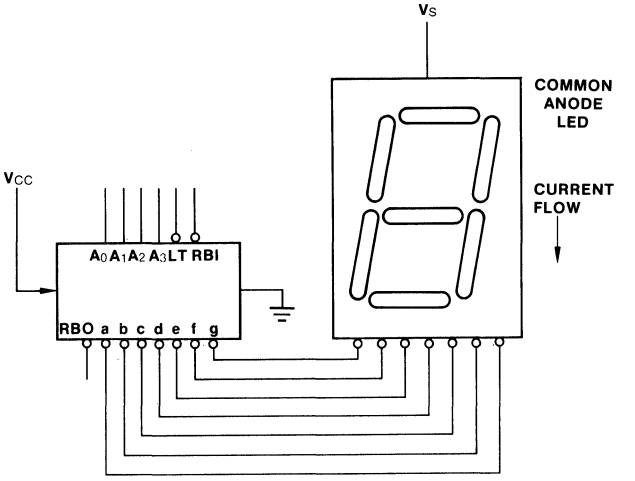


Fig. c Separate Supply for LED Displays

The power dissipated by the LED and the driver outputs is (V_{CC} x I_{seg} x n Segments). The total power dissipated with a 15 mA LED displaying an eight (8) would be:

$$P_{TOT} = 5.0\ V \times 15\ mA \times 7$$
$$= 525\ mW$$

Of this 525 mW, the power actually required to drive the LED is dependent on the V_F drop of each segment. Most GaAsP LEDs exhibit either a 1.7 V or a 3.4 V forward voltage drop. Therefore, the required total power for seven segments would be:

$$P_{(1.7)} = 1.7\ V \times 15\ mA \times 7$$
$$= 178.5\ mW$$
$$P_{(3.4)} = 3.4\ V \times 15\ mA \times 7$$
$$= 357\ mW$$

The remaining power is dissipated by the driver outputs which are maintaining the 15 mA constant current required by the LEDs. Most of this power is wasted, since the driver can maintain approximately 15 mA with as little as 0.5 V across the output device. By using a separate power source (V_S, *Figure c*) for the LEDs, which is set to the LED V_F plus the offset voltage of the driver, as much as 280 mW can be saved per digit. i.e.,

$$V_S = V_F\ (Max) + V_{offset}$$
$$= 2.0\ V + 0.5\ V$$
$$= 2.5\ V$$
$$P_T = 2.5\ V \times 14\ mA\ (from\ \textit{Figure b}) \times 7$$
$$= 245\ mW$$

These figures show that using a separate supply to drive the LEDs can offer significant display power savings. In battery powered equipment, two rechargeable nickle-cadmium cells in series would be sufficient to drive the display, while four such cells would be needed to operate the logic units.

APPLICATIONS (Cont'd) — Another method to save power is to apply intensity modulation to the displays *(Figure d)*. It is well known that LED displays are more efficient when operated in pulse mode. There are two reasons: one, the quantum efficiency of the LED material is better; secondly the eye tends to peak detect. Typically a 20% off duty cycle to displays (GaAsP) will produce the same brightness as operating under dc conditions.

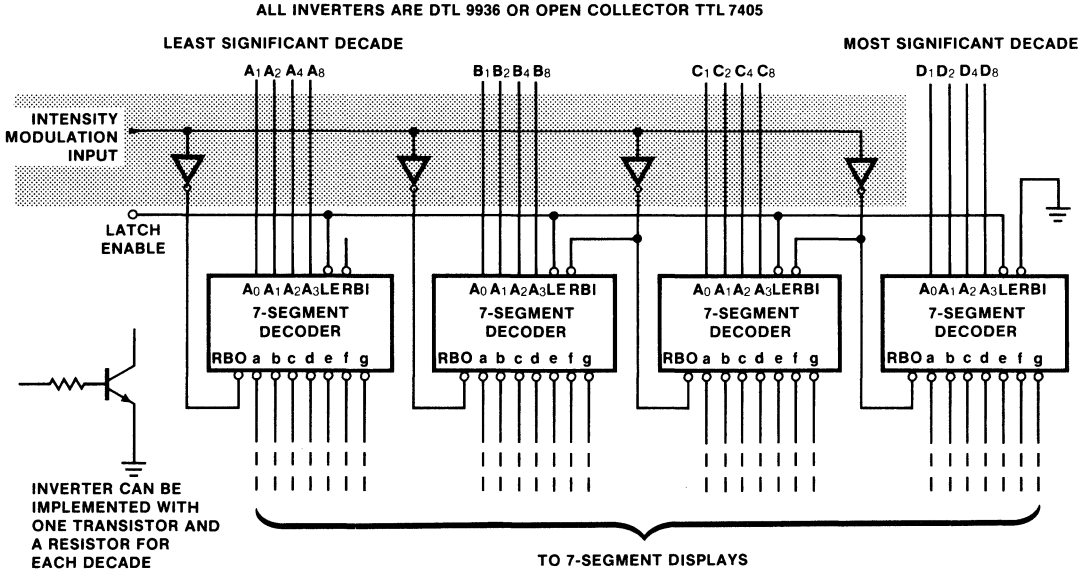


Fig. d Intensity Control by $\overline{\text{RBO}}$ Pulse Duty Cycle

Low Power, Low cost Display Power Sources — In small line operated systems using TTL/MSI and LED or incandescent displays, a significant portion of the total dc power is consumed to drive the displays. Since it is irrelevant whether displays are driven from unfiltered dc or pulsed dc (at fast rates), a dual power system can be used that makes better utilization of transformer rms ratings. The system utilizes a full wave rectified but unsmoothed dc voltage to provide the displays with 120 Hz pulsed power while the rest of the system is driven by a conventional dc power circuit. The frequency of 120 Hz is high enough to avoid display flicker problems. The main advantages of this system are:

- Reduced transformer rating
- Much smaller smoothing capacitor
- Increased LED light output due to pulsed operation

With the standard capacitor filter circuit, the rms current (full wave) loading of the tranformer is approximately twice the dc output. Most commercial transformer manufacturers rate tranformers with capacitive input filters as follows:

Full Wave Bridge Rectifier Circuit
Transformer rms current = 1.8 x dc current required

Full Wave Center Tapped Rectifier Circuit
Transformer rms current = 1.2 x dc current required

Therefore, the removal of a large portion of the filtered dc current requirement (display power) substantially reduces the transformer loading.

APPLICATIONS (Cont'd) — There are two basic approaches. First *(Figure e)* is the direct full wave rectified unregulated supply to power the displays. The '74 decoder driver constant current feature maintains the specified segment current after the LED diode drop and 0.5 V saturation voltage has been reached (≅2.2 V). Care must be exercised not to exceed the '74 power ratings and the maximum voltage that the decoder driver sees in both the "on" and "off" modes.

The second approach *(Figure f)* uses a 3-terminal voltage regulator such as the 7805 to provide dc pulsed power to the display with the peak dc voltage limited to +5.0 V. This approach allows easier system thermal management by heat sinking the regulator rather than the display or display drivers. When this power source is used with an intensity modulation scheme or with a multiplexed display system, the frequencies must be chosen such that they do not beat with the 120 Hz full wave rectified power frequency.

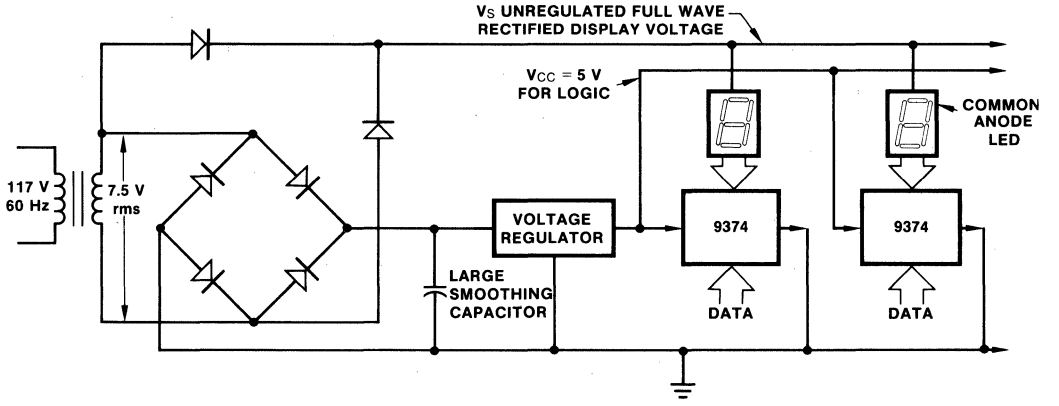


Fig. e Direct Unregulated Display Supply

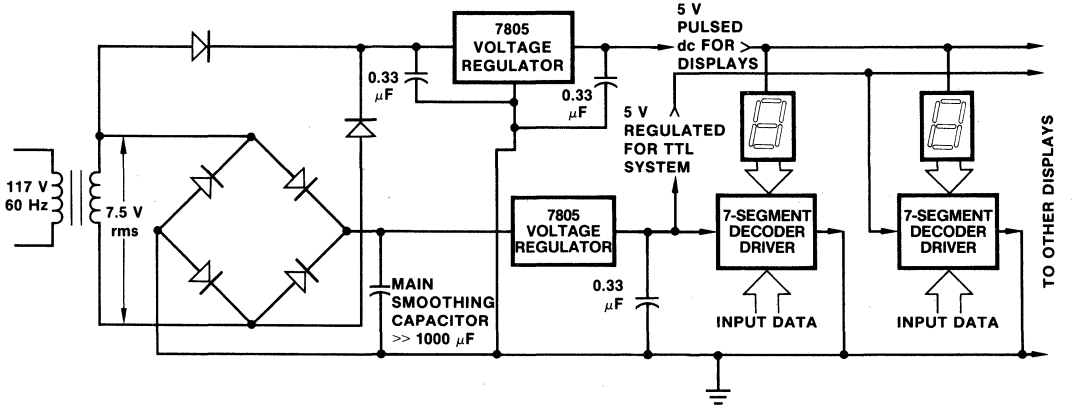
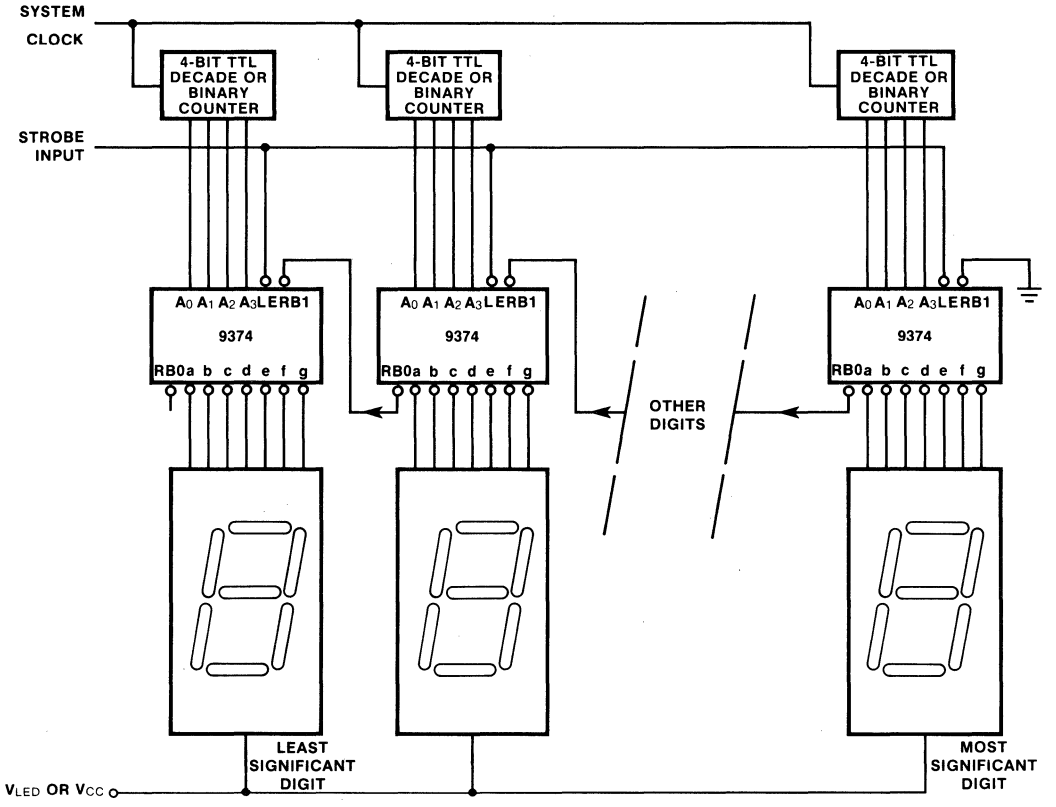


Fig. f Pulsed Regulated Display Supply

PARALLEL DATA SUPPLY SYSTEM WITH RIPPLE BLANKING



9386

4-BIT QUAD EXCLUSIVE-NOR

(With Open-Collector Outputs)

DESCRIPTION — The '86 consists of four independent Exclusive-NOR gates with open-collector outputs. Single 1-bit comparisons may be made with each gate, or multiple bit comparisons may be made by connecting the outputs of the four gates together. Typical power dissipation is 170 mW. The 9386 is equivalent to the 8242.

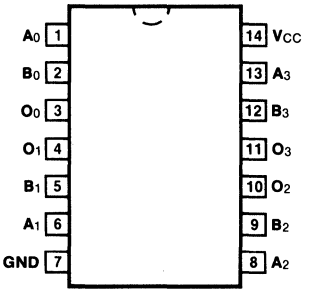
TRUTH TABLE

INPUTS		OUTPUT
A_n	B_n	O_n
L	L	H
H	L	L
L	H	L
H	H	H

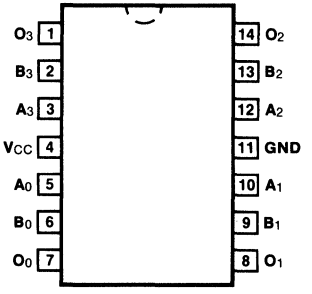
H = HIGH Voltage Level
L = LOW Voltage Level

CONNECTION DIAGRAMS

PINOUT A

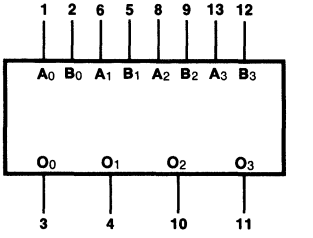


PINOUT B



LOGIC SYMBOL

(DIP only)



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

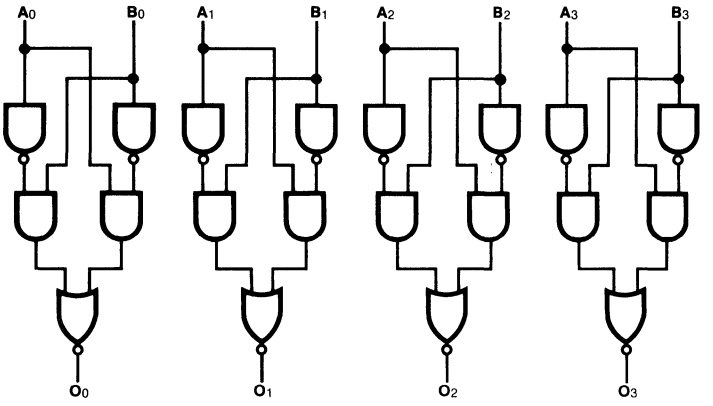
PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9386PC		9A
Ceramic DIP (D)	A	9386DC	9386DM	6A
Flatpak (F)	B	9386FC	9386FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
A_0, B_0	Gate 0 Inputs	2.0/2.0
A_1, B_1	Gate 1 Inputs	2.0/2.0
A_2, B_2	Gate 2 Inputs	2.0/2.0
A_3, B_3	Gate 3 Inputs	2.0/2.0
O_0 — O_3	Gate Outputs	OC*/15

*OC — Open Collector

LOGIC DIAGRAM

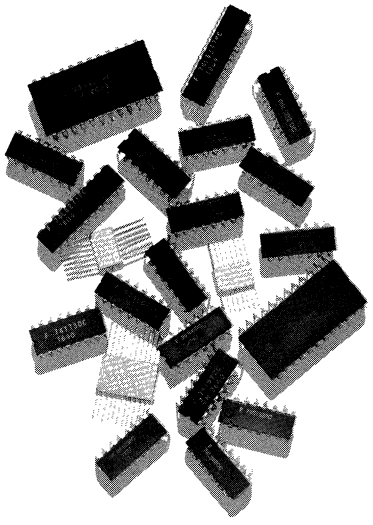


DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		93XX Min	93XX Max	UNITS	CONDITIONS
BV_i	Input Latch Voltage	A Input	5.5		V	I_{IN} (A) = 10 mA, V_{IN} (B) = 0 V
		B Input	5.5			I_{IN} (B) = 10 mA, V_{IN} (A) = 0 V
I_{OH}	Output HIGH Current			150	μA	V_{CC} = Min, V_{IN} = V_{IH} V_{OUT} = 4.5 V
I_{CC}	Power Supply Current			47.5	mA	V_{CC} = 5.25 V V_{IN} (A), V_{IN} (B) = 0.4 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 30 pF R_L = 530 Ω Min	93XX Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to O_0—O_3		25 25	ns	Figs. 3-2, 3-20



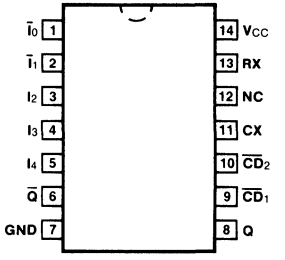
9600

RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

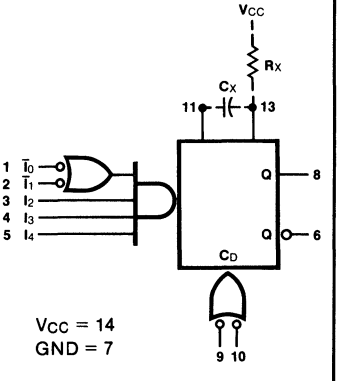
DESCRIPTION — The 9600 monostable, retriggerable, resettable multivibrator provides an output pulse whose duration and accuracy is a function of external timing components. The 9600 has excellent immunity to noise on the V_{CC} and ground lines. It uses TTL technology for high speed and high fan-out capability and is compatible with all members of the Fairchild TTL family.

- **74 ns TO ∞ OUTPUT PULSE WIDTH RANGE**
- **RETRIGGERABLE 0% to 100% DUTY CYCLE**
- **RESETTABLE**
- **LEADING OR TRAILING-EDGE TRIGGERING**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



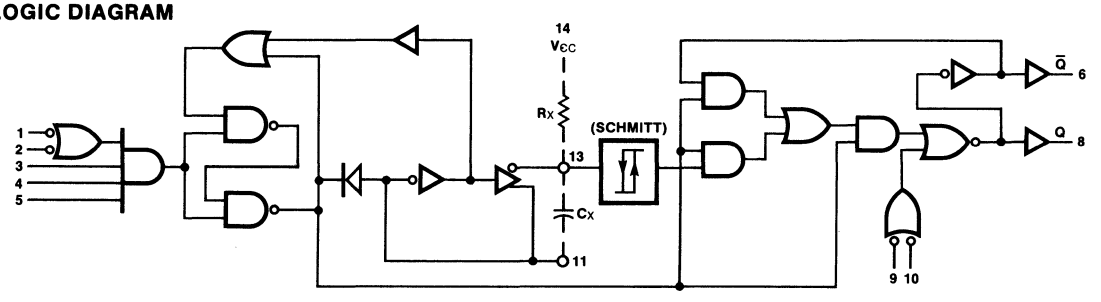
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +75°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	9600PC		9A
Ceramic DIP (D)	A	9600DC	9600DM	6A
Flatpak (F)	A	9600FC	9600FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	96XX (U.L.) HIGH/LOW
$\overline{I}_0$, $\overline{I}_1$	Trigger Inputs (Active Falling Edge)	1.5/1.0
I_2 — I_4	Trigger Inputs (Active Rising Edge)	1.5/1.0
$\overline{C}_{D1}$ — $\overline{C}_{D2}$	Clear Inputs (Active LOW)	1.5/1.0
Q	Pulse Output	24/7.06 (6.2)
$\overline{Q}$	Complementary Pulse Output	24/7.06 (6.2)

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The 9600 monostable multivibrator has five inputs, three active HIGH and two active LOW. This allows leading-edge or trailing-edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 9600 and result in a continuous true output (see Rule 8). Retriggering may be inhibited by tying the negation ($\overline{Q}$) output to an active LOW input. The output pulse may be terminated at any time by connecting either or both reset pins to a LOW logic level pin. Active pullups are provided on the outputs for good drive capability into capacitive loads.

Operating Notes

1. An external resistor (R_X) and an external capacitor (C_X) are required as shown in the logic diagram. The value of R_X may vary from 5.0 kΩ to 50 kΩ for 0° C to +75° C operation and from 5.0 kΩ to 25 kΩ for -55° C to +125° C operation. C_X may vary from 0 to any necessary value available.
2. The following are recommended fixed values of R_X: R_X = 30 kΩ for 0° C to +75° C operation, R_X = 10 kΩ for -55° C to +125° C operation.
3. The output pulse width (t) is defined as follows:
   $t = 0.32\ R_X C_X\ |1 + 0.7/R_X|$ Where R_X is in kΩ, C_X is in pF, t is in ns; for $C_X < 10^3$ pF. (see *Figure a*)
   The value of C_X may vary from 0 to any value necessary and obtainable. If however, C_X has leakage currents approaching 3.0 μA or if stray capacitance from either pin 11 or pin 13 to ground exceeds 50 pF, the timing equation may not represent the pulse width obtained.
4. If electrolytic type capacitors are to be used, the following three configurations are recommended.
   A. Use with low leakage electrolytic capacitors (see *Figure b*).
      The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 V is less than 3.0 μA, and the inverse capacitor leakage at 1.0 V is less than 5.0 μA over the operational temperature range and Rule 3 above is satisfied.
   B. Use with high inverse leakage current electrolytic capacitors. (*Figure c*; this configuration is not recommended with retriggerable operation.)
      The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor.
      $t \approx 0.3\ RC_X$
   C. Use to obtain extended pulse widths. (*Figure d*; this configuration is not recommended with retriggerable operation.)
      This configuration obtains extended pulse widths because of the larger timing resistor allowed by Beta multiplication. Electrolytics with high inverse leakage currents can be used. Q_1 is an npn silicon transistor such as 2N5961 or 2N5962, with h_{FE}, R and R_X related as in the inequality below.
      $R < R_X\ (0.7)\ (h_{FE}\ Q_1)$ or < 2.5 MΩ, whichever is less
      R_X (Min) < R_Y < R_X (Max) R_Y of 5.0 kΩ to 10 kΩ is recommended
      $t \approx 0.3\ RC_X$
5. This circuit is recommended to obtain variable pulse width by remote trimming *(Figure e)*.
6. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. Input Trigger Pulse Rules (see Triggering Truth Table *Figures f* and *g*).
   t_1, t_3 = Min. positive input pulse width > 40 ns.
   t_2, t_4 = Min. negative input pulse width > 40 ns.
8. The retrigger pulse width is equal to the pulse width t plus a delay time (see *Figure h*). For pulse widths greater than 500 ns, t_w can be approximated as t.
   $$t_w = t + t_{PLH} = 0.32\ R_X C_X\ (1 + 0.7/R_X) + t_{PLH}$$
9. Two overriding active LOW resets are provided (see *Figure i*). A LOW to either or both resets can terminate any timing cycle and/or inhibit any new cycle until both reset inputs are restored to a HIGH. Trigger inputs will not produce spikes in the output when either or both resets are held LOW.
10. Use of a 0.01 μF to 0.1 μF bypass capacitor located close to the 9600 is recommended.

TRIGGERING TRUTH TABLE*

INPUT PINS							RESPONSE
1	2	3	4	5	9	10	
X	X	X	X	X	L	X	No Trigger
↘	L	X	X	X	X	X	No Trigger
↘	X	L	X	X	X	X	No Trigger
↘	H	H	H	H	H	H	Trigger
H	H	↗	X	X	X	X	No Trigger
X	X	↗	L	X	X	X	No Trigger
L	X	↗	H	H	H	H	Trigger

*Pins 1 &2 are logically interchangeable, as are pins 3, 4, 5, and also 9 & 10.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE FOR $C_X < 10^3$ pF

For $C_X \geq 10^3$ pF, $t = 0.32\ R_X C_X (1 + 0.7/R_X)$

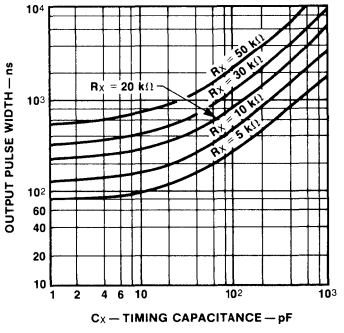


Fig. a

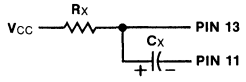


Fig. b

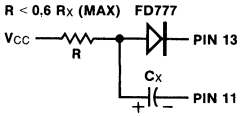


Fig. c

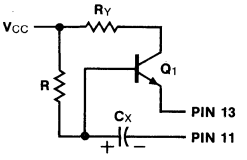


Fig. d

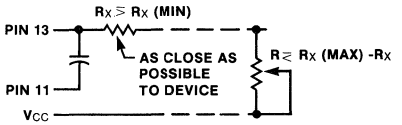


Fig. e Remote Trimming

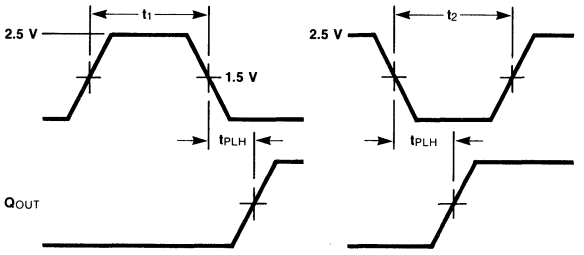


Fig. f Input on Pin 1 or 2

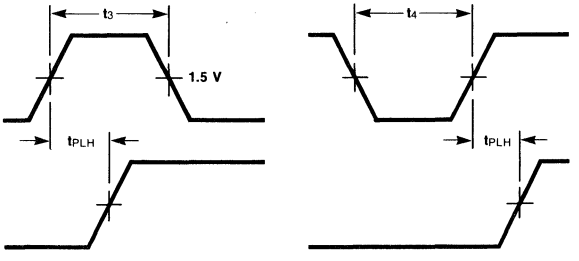
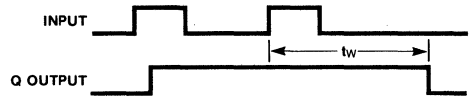


Fig. g Input on Pin 3, 4 or 5

7



NOTE:
Retriggering will not occur if the retrigger pulse comes within ≈ 0.3 C_X ns after the initial trigger pulse (i.e., during the discharge cycle time).

Fig. h

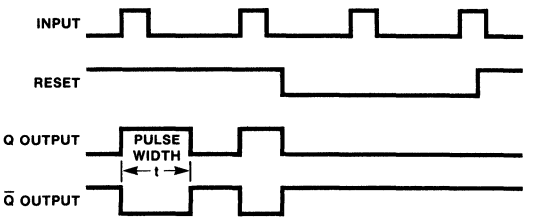
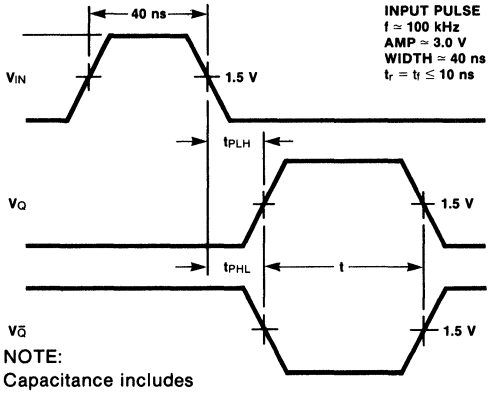


Fig. i



NOTE:
Capacitance includes Jig and Probe

Fig. j

NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

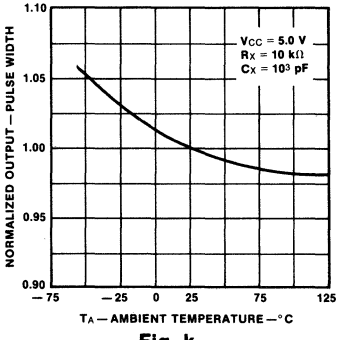


Fig. k

NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE

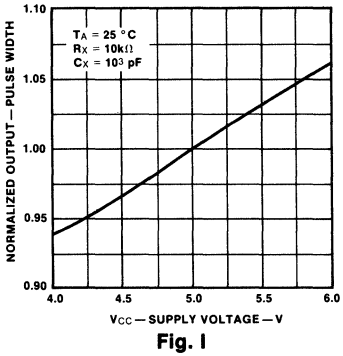


Fig. l

MINIMUM OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

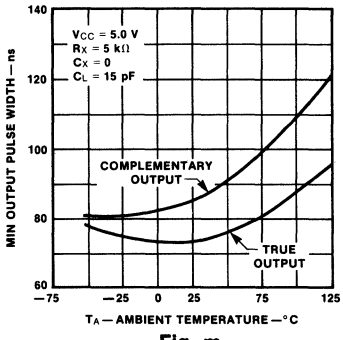


Fig. m

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		96XX Min	96XX Max	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage	XM		0.4	V	I_{OL} = 9.92 mA* V_{CC} = Min
		XC		0.45		I_{OL} = 11.3 mA V_{CC} = Min
V_{OL}	Output LOW Voltage	XM		0.4	V	I_{OL} = 12.8 mA, V_{CC} = Max
		XC		0.45		
V_{IH}	Input HIGH Voltage	XM	1.5		V	T_A = Max
		XC	1.65			
V_{IL}	Input LOW Voltage	XM		0.9	V	T_A = 25°C
		XC		0.85		
I_{IL}	Input LOW Current	XM		-1.6	mA	V_{IN} = 0.4 V V_{CC} = Max
		XC		-1.6		V_{IN} = 0.45 V V_{CC} = Max
I_{OS}	Output Short Circuit Current	XM		-25	mA	V_{CC} = Max, V_{OUT} = 1.0 V* T_A = 25°C
		XC		-35		
I_{PD}	Quiescent Power Supply Drain	XM		24	mA	V_{CC} = 5.0 V, Pins 1, 2 = Gnd
		XC		26		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER		96XX C_L = 15 pF Min	96XX C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH}	Propagation Delay $\overline{I_n}$ to Q	XM		45	ns	R_X = 5.0 Ω, C_X = 0 pF Figs. 3-1, Fig. j
		XC		56		
t_{PHL}	Propagation Delay $\overline{I_n}$ to $\overline{Q}$	XM		40	ns	
		XC		47		
t_w (Min)	Minimum Q Pulse Width	XM		100	ns	R_X = 5.0 Ω, C_X = 0 pF
		XC		120		
t_w (Min)	Minimum $\overline{Q}$ Pulse Width	XM		112	ns	Fig. 3-1, Fig. j
		XC		130		
t_w	Pulse Width	XM	3.2	3.76	μs	R_X = 10 kΩ, C_X = 1000 pF Fig. 3-1, Fig. j
		XC	3.08	3.76		

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER		96XX Min	96XX Max	UNITS	CONDITIONS
C_{STRAY}	Maximum Allowable Wiring Capacitance (Pin 13)			50	pF	Pin 13 to Gnd
R_X (Max)	Maximum Timing Resistor	XM	5.0	25	kΩ	Over Operating Temperature Range
		XC	5.0	50		

*Ground Pin 11 for V_{OL} Pin 6 or V_{OH} Pin 8 or I_{OS} Pin 8, open Pin 11 for V_{OL} Pin 8 or V_{OH} Pin 6 or I_{OS} Pin 6.

9601

RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

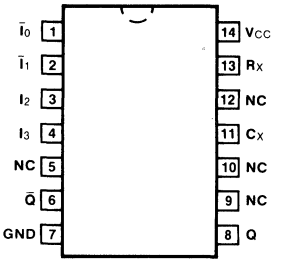
DESCRIPTION — The 9601 is a retriggerable one-shot with versatile trigger gating, rapid recovery, internally compensated reference levels, and high speed capability. It is well suited for a broad variety of applications, including pulse delay generators, square wave generators, long delay timers, pulse absence detectors, and clock pulse generators.

- **RETRIGGERABLE, 0% TO 100% DUTY CYCLE**
- **DC LEVEL TRIGGERING, INSENSITIVE TO TRANSITION TIMES**
- **COMPLEMENTARY INPUTS, FOR LEADING OR TRAILING-EDGE TRIGGERING**
- **COMPLEMENTARY OUTPUTS, WITH ACTIVE PULL-UPS FOR DRIVING LOAD CAPACITANCE.**
- **PULSE WIDTH COMPENSATION FOR V_{CC} AND TEMPERATURE VARIATIONS**
- **50 ns TO ∞ OUTPUT PULSE WIDTH RANGE**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**

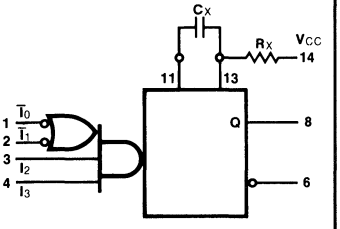
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +75°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	9601PC		9A
Ceramic DIP (D)	A	9601DC	9601DM	6A
Flatpak (F)	A	9601FC	9601FM	3I

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL

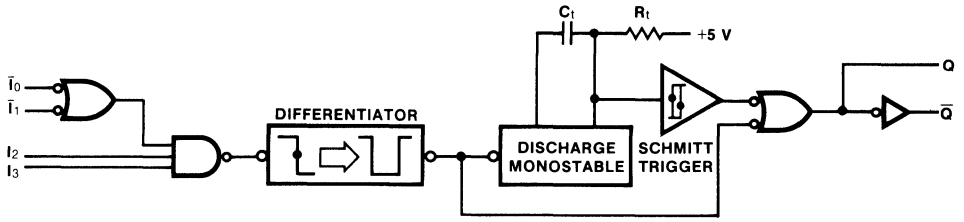


V_{CC} = Pin 14
GND = Pin 7

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	96XX (U.L.) HIGH/LOW
$\overline{I}_0$, $\overline{I}_1$	Trigger Input (Active Falling Edge)	1.5/1.0
I_2, I_3	Trigger Input (Active Rising Edge)	1.5/1.0
Q	Positive Pulse Output	24/8.0 (18)/(6.25)
$\overline{Q}$	Complementary Pulse Output	24/8.0 (18)/(6.25)

FUNCTIONAL BLOCK DIAGRAM



TRIGGERING TRUTH TABLE

Pin 1	Pin 2	Pin 3	Pin 4	RESPONSE
H	H	⎍	X	No Trigger
L	X	⎍	H	Triggers
L	X	⎍	L	No Trigger
⎎	H	H	H	Triggers
⎎	H	L	X	No Trigger
⎎	L	X	X	No Trigger

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

7

OUTPUT t_w vs R_X AND C_X

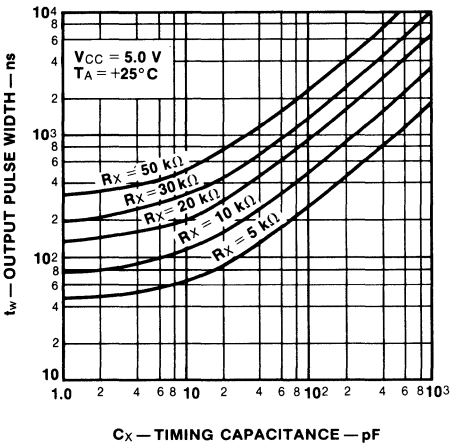
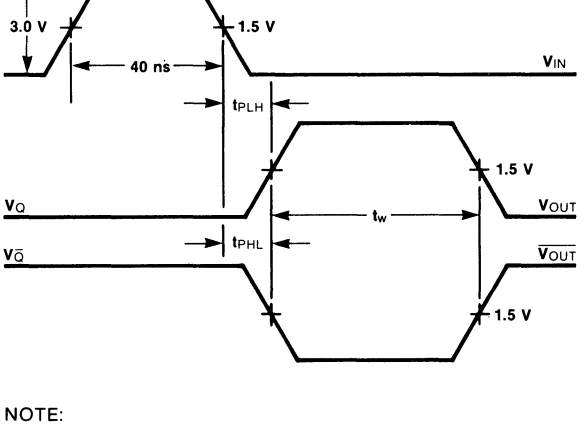


Fig. a



NOTE:
Capacitance includes Jig and Probe

Fig. b

FUNCTIONAL DESCRIPTION — The 9601 monostable multivibrator has four inputs, two active HIGH and two active LOW. This allows a choice of leading-edge or trailing-edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 9601 and result in a continuous true output. Retriggering may be inhibited by tying the negation ($\overline{Q}$) output to an active LOW input. Active pullups are provided on the outputs for good drive capability into capacitive loads.

Operation Notes

1. TRIGGERING — The 9601 has four dc coupled triggering inputs; pins 1 and 2 respond to falling edge signals, while pins 3 and 4 respond to rising edge signals. Triggering occurs as the input signal passes through the threshold region. Triggering logic is outlined in the Table. Input signals can be interchanged between pins 1 and 2, since they are logically identical; the same relationship holds for pins 3 and 4.

2. RETRIGGERING — In a normal cycle, triggering initiates a rapid discharge of the external timing capacitor, followed by a ramp voltage run-up at pin 13. The delay will time out when the ramp voltage reaches the upper trigger point of the Schmitt circuit, causing the outputs to revert to the quiescent state. If another trigger occurs before the ramp voltage reaches the Schmitt threshold, the capacitor will be discharged and the ramp will start again without having disturbed the outputs. The delay period can therefore be extended for an arbitrary length of time by insuring that the interval between triggers is less than the delay time, as determined by the external capacitor and resistor.

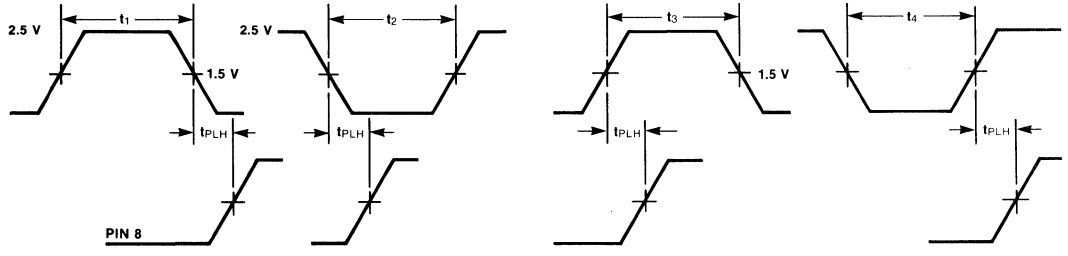
3. NON-RETRIGGERABLE OPERATION — Retriggering can be inhibited logically, by connecting pin 6 back to pin 3 or 4, or by connecting pin 8 back to **both** pins 1 and 2.

4. OUTPUT PULSE WIDTH — An external resistor R_X and an external capacitor C_X are required, as shown in the functional block diagram; to minimize stray capacitance and noise pickup, R_X and C_X should be located as close as possible to the circuit. In applications which require remote trimming of the pulse width, as with a variable resistor, R_X should consist of a fixed resistor in series with the variable resistor; the fixed resistor should be located as close as possible to the circuit. The output pulse width t_w is defined as follows, where R_X is in kΩ, C_X is in pF and t_w is in ns.

$$t_w = 0.32\ R_X C_X\ (1 + 0.7/R_X) \qquad \text{(for } C_X > 10^3 \text{ pF; see also } \textit{Figure a.}\text{)}$$

The values of R_X may vary from 5.0 kΩ to 50 kΩ for 0° to +75°C operation, and 5.0 kΩ to 25 kΩ for -55° to +125°C operation. C_X may vary from 0 to any value.

5. SETUP AND RELEASE TIMES



t_1, t_4 = Setup time > 40 ns t_2, t_3 = Release time > 40 ns

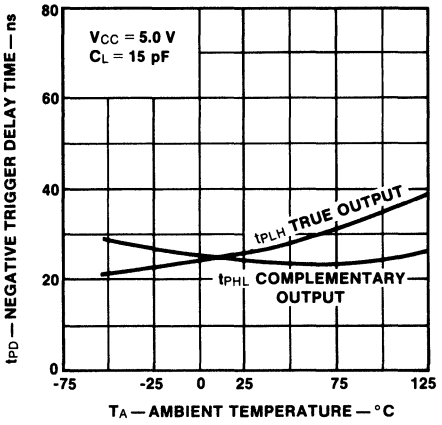
Input to Pin 1 (2)
Pins 2 (1), 3 and 4 = 1

Input to Pin 3 (4)
Pin 4 (3) = 1
Pins 1 or 2 = 0

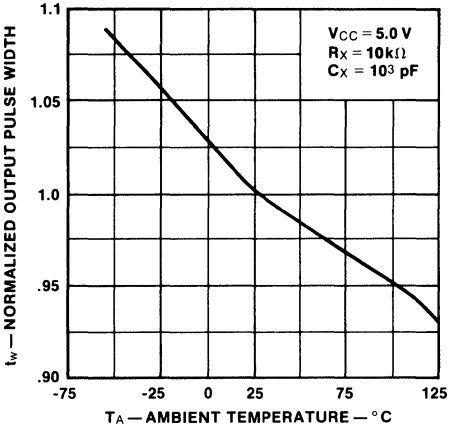
6. CAPACITOR LEAKAGE — Recommendations on electrolytic capacitors and larger values of R_X are discussed in the 9600 data sheet.

TYPICAL CHARACTERISTICS

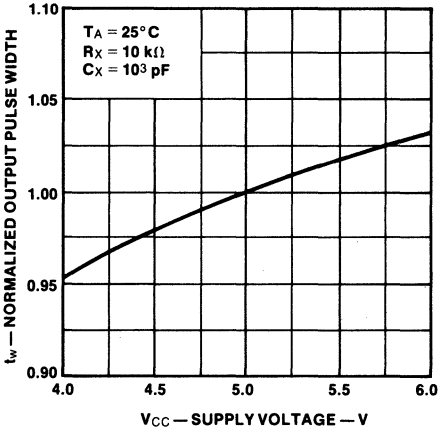
$\overline{I}_n$ DELAY TIME vs T_A



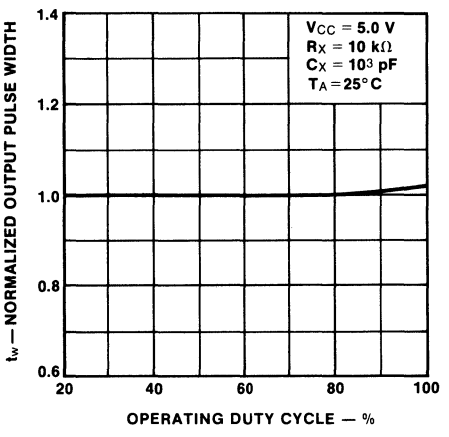
OUTPUT t_w vs T_A



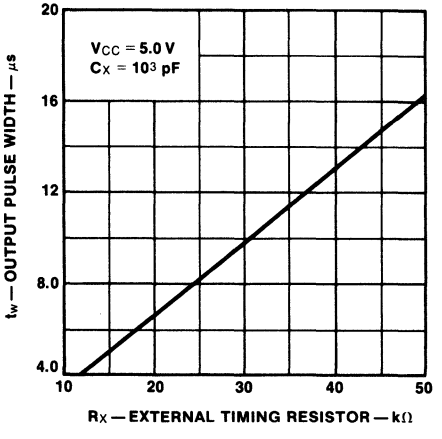
OUTPUT t_w vs V_{CC}



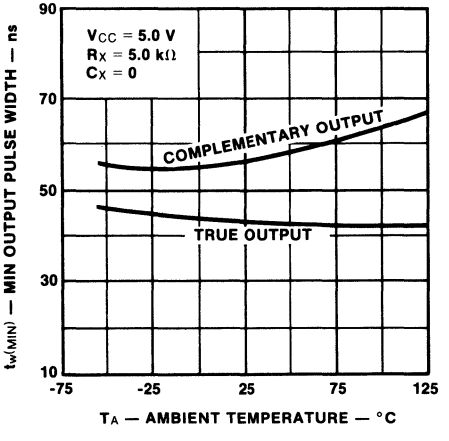
OUTPUT t_w vs DUTY CYCLE



OUTPUT t_w vs R_X



OUTPUT t_w vs T_A



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DC AND AC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE: V_{CC} = +5.0 V except as noted.

SYMBOL	PARAMETER	0°C		+25°C		+75°C		UNITS	CONDITIONS[1]
		Min	Max	Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage[2]	2.4		2.4		2.4		V	V_{CC} = 4.75 V I_{OH} = -0.96 mA
V_{OL}	Output LOW Voltage[2]		0.45		0.45		0.45	V	V_{CC} = 4.75 V I_{OL} = 12.8 mA
V_{IH}	Input HIGH Voltage[3]	1.9		1.8		1.6		V	
V_{IL}	Input LOW Voltage[3]		0.85		0.85		0.85	V	
I_{IL}	Input LOW Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.25 V V_{IN} = 0.45 V
I_{IH}	Input HIGH Current				60		60	μA	V_{CC} = 5.25 V V_{IN} = 4.5 V
I_{OS}	Output Short Circuit Current[2]			-10	-40			mA	V_{OUT} = 0 V
I_{CC}	Power Supply Current		25		25		25	mA	V_{CC} = 5.25 V Gnd Pins 1, 2
t_{PLH}	Propagation Delay $\overline{I_n}$ to Q				40			ns	R_X = 5.0 kΩ C_L = 15 pF C_X = 0, Fig. b
t_{PHL}	Propagation Delay $\overline{I_n}$ to $\overline{Q}$				40			ns	R_X = 5.0 kΩ C_L = 15 pF C_X = 0, Fig. b
t_w (min)	Minimum True Output Pulse Width				65			ns	R_X = 5.0 kΩ C_L = 15 pF C_X = 0, Fig. b
t_w	Pulse Width			3.08	3.76			μs	R_X = 10 kΩ C_X = 1000 pF Fig. b
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50		50		50	pF	Pin 13 to Gnd
R_X	Timing Resistor	5.0	50	5.0	50	5.0	50	kΩ	

(1) Unless otherwise noted, 10 kΩ resistor placed between Pin 13 and V_{CC}, for all tests. (R_X)
(2) Ground Pin 11 for V_{OL} Pin 6 or V_{OH} Pin 8 or I_{OS} Pin 8. Open Pin 11 for V_{OL} Pin 8 or V_{OH} Pin 6 or I_{OS} Pin 6.
(3) Pulse Test to determine V_{IH} and V_{IL} (Min t_w 40 ns).

DC AND AC CHARACTERISITCS OVER MILITARY TEMPERATURE RANGE: V_{CC} = +5.0 V except as noted

SYMBOL	PARAMETER	-55°C		+25°C		+125°C		UNITS	CONDITIONS[1]
		Min	Max	Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage[2]	2.4		2.4		2.4		V	V_{CC} = 4.5 V I_{OH} = -0.72 mA
V_{OL}	Output LOW Voltage[2]		0.4		0.4		0.4	V	V_{CC} = 4.5 V I_{OL} = 10 mA
V_{IH}	Input HIGH Voltage[3]	2.0		1.7		1.5		V	
V_{IL}	Input LOW Voltage[3]		0.85		0.9		0.85	V	
I_{IL}	Input LOW Current		-1.6		-1.6		-1.6	mA	V_{CC} = 5.5 V V_{IN} = 0.4 V
I_{IH}	Input HIGH Current				60		60	μA	V_{CC} = 5.5 V V_{IN} = 4.5 V
I_{OS}	Output Short Circuit Current			-10	-40			mA	V_{OUT} = 0 V
I_{CC}	Power Supply Current		25		25		25	mA	V_{CC} = 5.5 V Gnd Pins 1, 2
t_{PLH}	Propagation Delay $\overline{I}_n$ to Q				40			ns	R_X = 5.0 kΩ C_L = 15 pF C_X = 0, Fig. b
t_{PHL}	Propagation Delay $\overline{I}_n$ to $\overline{Q}$				40			ns	R_X = 5.0 kΩ C_L = 15 pF C_X = 0, Fig. b.
t_w (min)	Minimum True Output Pulse Width				65			ns	R_X = 5.0 kΩ C_L = 15 pF C_X = 0, Fig. b
t_w	Pulse Width			3.08	3.76			μs	R_X = 10 kΩ C_X = 1000 pF Fig. b
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50		50		50	pF	Pin 13 to Gnd
R_X	Timing Resistor	5.0	25	5.0	25	5.0	25	kΩ	

(1) Unless otherwise noted, 10 kΩ resistor placed between Pin 13 and V_{CC}, for all tests. (R_X)
(2) Ground Pin 11 for V_{OL} Pin 6 or V_{OH} Pin 8 or I_{OS} Pin 8. Open Pin 11 for V_{OL} Pin 8 or V_{OH} Pin 6 or I_{OS} Pin 6 .
(3) Pulse Test to determine V_{IH} and V_{IL} (Min t_w 40 ns).

7

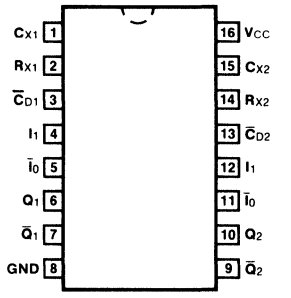
9602
96L02

DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

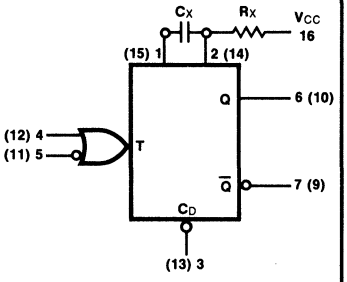
DESCRIPTION — The 9602 is a dual TTL monostable multivibrator with trigger mode selection, reset capability, rapid recovery, internally compensated reference levels and high speed capability. Output pulse duration and accuracy depend on external timing components, and are therefore under user control for each application. It is well suited for a broad variety of applications, including pulse delay generators, square wave generators, long delay timers, pulse absence detectors, frequency detectors, clock pulse generators and fixed-frequency dividers. Each input is provided with a clamp diode to limit undershoot and minimize ringing induced by fast fall times acting on system wiring impedances.

- **RETRIGGERABLE, 0% TO 100% DUTY CYCLE**
- **DC LEVEL TRIGGERING, INSENSITIVE TO TRANSITION TIMES**
- **LEADING OR TRAILING-EDGE TRIGGERING**
- **COMPLEMENTARY OUTPUTS WITH ACTIVE PULL-UPS**
- **PULSE WIDTH COMPENSATION FOR ΔV_{CC} AND ΔT_A**
- **50 ns TO ∞ OUTPUT PULSE WIDTH RANGE**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**
- **RESETTABLE, FOR INTERRUPT OPERATIONS**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

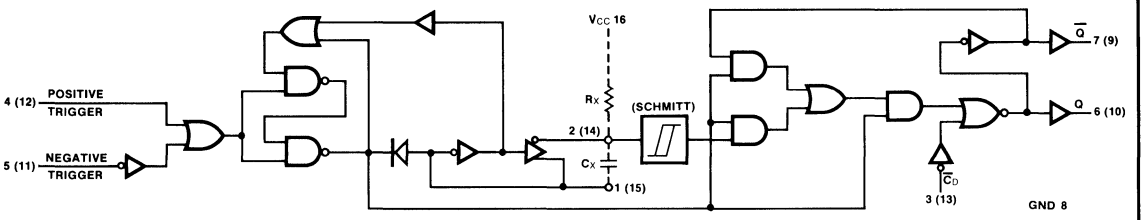
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0° C to +70° C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	9602PC, 96L02PC		9B
Ceramic DIP (D)	A	9602DC, 96L02DC	9602DM, 96L02DM	6B
Flatpak (F)	A	9602FC, 96L02FC	9602FM, 96L02FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	96XX (U.L.) HIGH/LOW	96L (U.L.) HIGH/LOW
$\overline{I}_0$	Trigger Input (Active Falling Edge)	1.5/1.0	0.5/0.25
I_1	Trigger Input (Active Rising Edge)	1.5/1.0	0.5/0.25
$\overline{C}_D$	Direct Clear Input (Active LOW)	1.5/1.0	0.5/0.25
Q	Positive Pulse Output	24/7.0 (6.2)	9.0/3.0
$\overline{Q}$	Complementary Pulse Output	24/7.0 (6.2)	9.0/3.0

FUNCTIONAL BLOCK DIAGRAM



OPERATION NOTES

1. TRIGGERING — can be accomplished by a positive-going transition on pin 4 (12) or a negative-going transition on pin 5 (11). Triggering begins as a signal crosses the input V_{IL}:V_{IH} threshold region; this activates an internal latch whose unbalanced cross-coupling causes it to assume a preferred state. As the latch output goes LOW it disables the gates leading to the Q output and, through an inverter, turns on the capacitor discharge transistor. The inverted signal is also fed back to the latch input to change its state and effectively end the triggering action; thus the latch and its associated feed-back perform the function of a differentiator.

   The emitters of the latch transistors return to ground through an enabling transistor which must be turned off between successive triggers in order for the latch to proceed through the proper sequence when triggering is desired. Pin 5 (11) must be HIGH in order to trigger at pin 4 (12); conversely, pin 4 (12) must be LOW in order to trigger at pin 5 (11).

2. RETRIGGERING — In a normal cycle, triggering initiates a rapid discharge of the external timing capacitor, followed by a ramp voltage run-up at pin 2 (14). The delay will time out when the ramp voltage reaches the upper trigger point of a Schmitt circuit, causing the outputs to revert to the quiescent state. If another trigger occurs before the ramp voltage reaches the Schmitt threshold, the capacitor will be discharged and the ramp will start again without having disturbed the output. The delay period can therefore be extended for an arbitrary length of time by insuring that the interval between triggers is less than the delay time, as determined by the external capacitor and resistor.

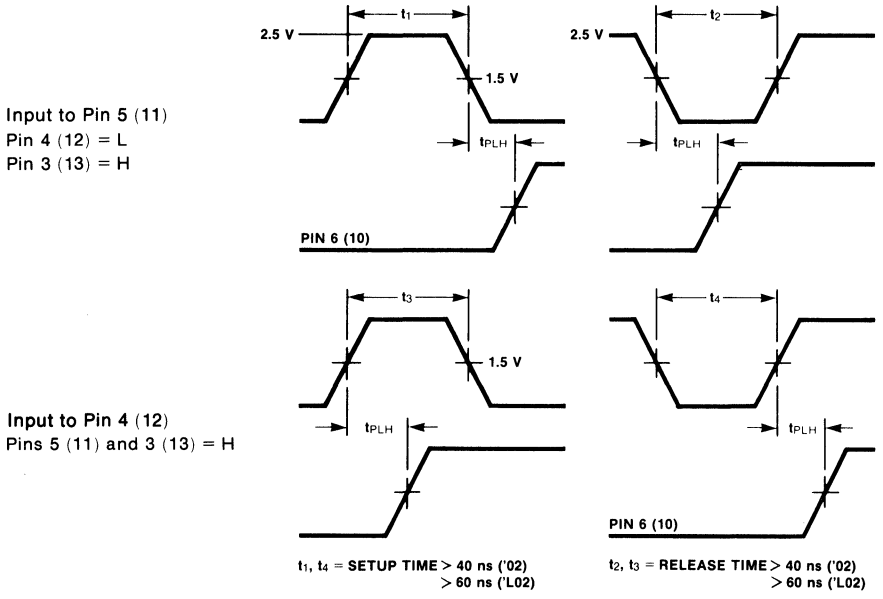
3. NON-RETRIGGERABLE OPERATION — Retriggering can be inhibited logically, by connecting pin 6 (10) back to pin 4 (12) or by connecting pin 7 (9) back to pin 5 (11). Either hook-up has the effect of keeping the latch-enabling transistor turned on during the delay period, which prevents the input latch from cycling as discussed above in the section on triggering.

4. OUTPUT PULSE WIDTH — An external resistor R_X and an external capacitor C_X are required, as shown in the functional block diagram. To minimize stray capacitance and noise pickup, R_X and C_X should be located as close as possible to the circuit. In applications which require remote trimming of the pulse width, as with a variable resistor, R_X should consist of a fixed resistor in series with the variable resistor; the fixed resistor should be located as close as possible to the circuit. The output pulse width t_w is defined as follows, where R_X is in kΩ, C_X is in pF and t_w is in ns.

   (9602) $t_w = 0.31\ R_X C_X\ (1 + 1/R_X)$ for $C_X \geq 10^3$ pF
   $5\ k\Omega \leq R_X \leq 50\ k\Omega$ for 0° C to +75° C
   $5\ k\Omega \leq R_X \leq 25\ k\Omega$ for -55° C to +125° C
   (96L02) $t_w = 0.33\ R_X C_X\ (1 + 3/R_X)$ for $C_X \geq 10^3$ pF
   $16\ k\Omega \leq R_X \leq 220\ k\Omega$ for 0° C to +75° C
   $20\ k\Omega \leq R_X \leq 100\ k\Omega$ for -55° C to +125° C
   C_X may vary from 0 to any value. For pulse widths with C_X less than 10^3 pF see *Figures a and b*.

OPERATION NOTES (Cont'd)

5. SETUP AND RELEASE TIMES — The setup times listed below are necessary to allow the latch-enabling transistor to turn off and the node voltages within the input latch to stabilize, thus insuring proper cycling of the latch when the next trigger occurs. The indicated release times (equivalent to trigger duration) allow time for the input latch to cycle and its signal to propagate.



6. RESET OPERATION — A LOW signal on $\overline{C}_D$, pin 3 (13), will terminate an output pulse, causing Q to go LOW and $\overline{Q}$ to go HIGH. As long as $\overline{C}_D$ is held LOW, a delay period cannot be initiated nor will attempted triggering cause spikes at the outputs. A reset pulse duration, in the LOW state, of 25 ns is sufficient to insure resetting. If the reset input goes LOW at the same time that a trigger transition occurs, the reset will dominate and the outputs will not respond to the trigger. If the reset input goes HIGH coincident with a trigger transition, the circuit will respond to the trigger.

7. CAPACITOR LEAKAGE — For recommendations on electrolytic capacitors and larger values of R_X, please see the 9600 data sheet.

96L02 PULSE WIDTH vs R_X AND C_X

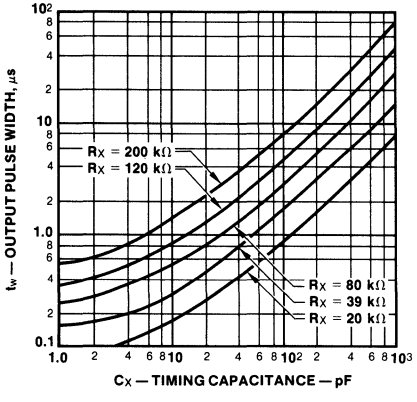


Fig. a

9602 PULSE WIDTH vs R_X AND C_X

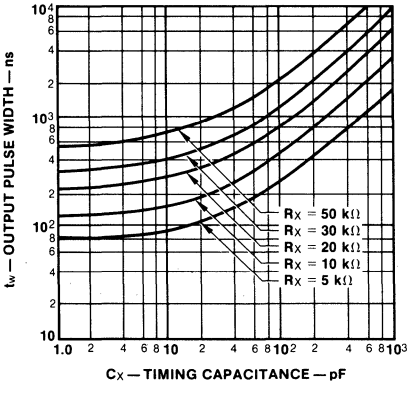
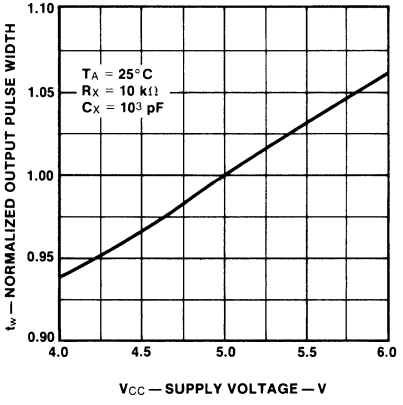


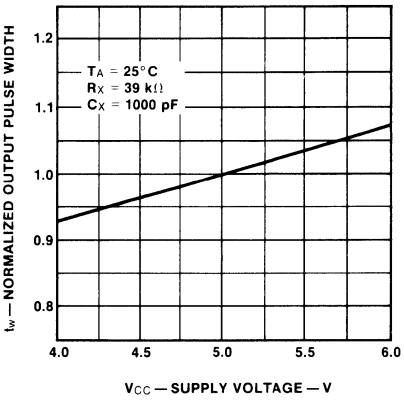
Fig. b

TYPICAL CHARACTERISTICS

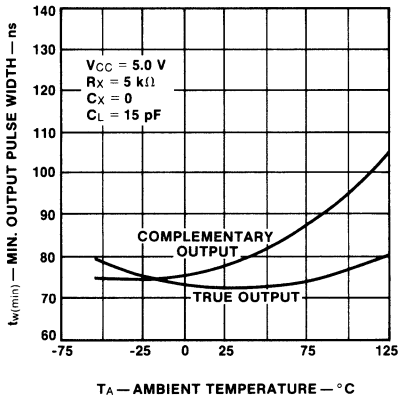
9602 t_w vs V_{CC}



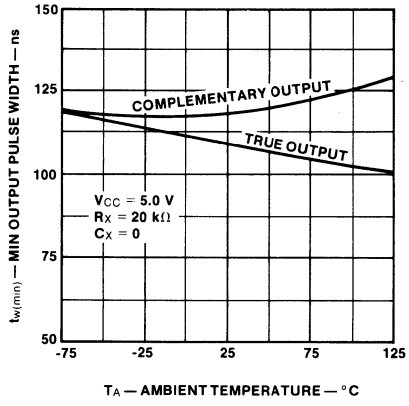
96L02 t_w vs V_{CC}



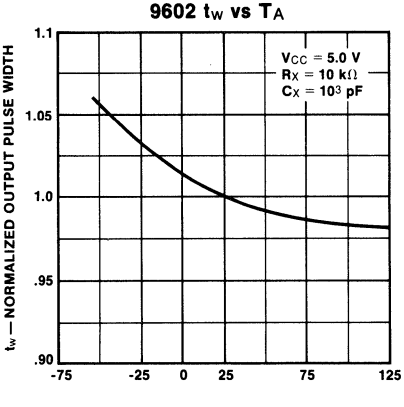
9602 $t_{w(min)}$ vs T_A



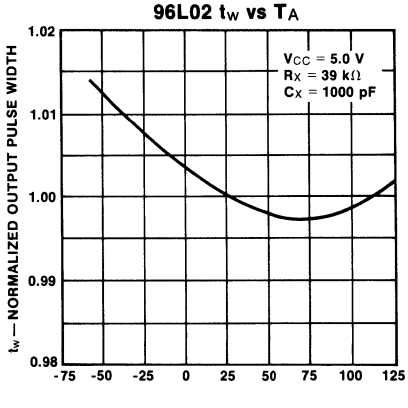
96L02 $t_{w(min)}$ vs T_A



9602 t_w vs T_A



96L02 t_w vs T_A



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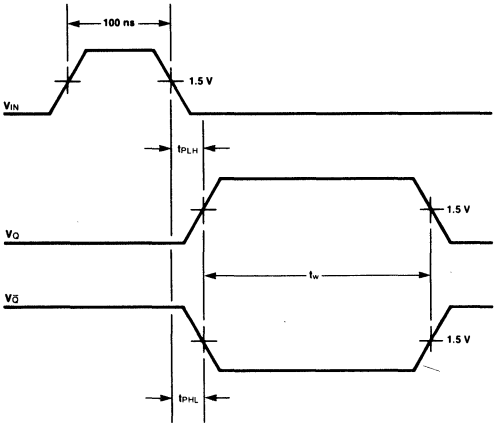
DC AND AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		96XX Min	96XX Max	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage		12.4		V	V_{CC} = Min, I_{OH} = -9.6 mA
V_{OL}	Output LOW Voltage	XM		0.4	V	V_{CC} = 4.5 V, I_{OL} = 9.92 mA V_{CC} = 5.5 V, I_{OL} = 12.8 mA
		XC		0.45	V	V_{CC} = 4.75 V, I_{OL} = 11.3 mA V_{CC} = 5.25 V, I_{OL} = 12.8 mA
V_{IH}	Input HIGH Voltage	XM	2.0		V	Guaranteed Input HIGH Threshold
		XC	1.9			
V_{IL}	Input LOW Voltage			0.85	V	Guaranteed Input LOW Threshold
I_{IL}	Input LOW Current			-1.6	mA	V_{CC} = Max, V_{IN} = V_{OL}
I_{IL}	Input LOW Current	XM		-1.24	mA	V_{CC} = Min, V_{IN} = V_{OL}
		XC		-1.14		
I_{IH}	Input HIGH Current			60	μA	V_{CC} = Max, V_{IN} = 4.5 V
I_{OS}	Output Short Circuit Current	XM		-25	mA	V_{CC} = Max, V_{OUT} = 1.0 V
		XC		-35		
I_{CC}	Power Supply Current	XM		45	mA	V_{CC} = 5.0 V
		XC		52		
t_{PLH}	Propagation Delay $\overline{I_0}$ to Q	XM		35	ns	R_X = 5 kΩ, C_X = 0 C_L = 15 pF, Fig. c
		XC		40		
t_{PHL}	Propagation Delay $\overline{I_0}$ to $\overline{Q}$	XM		43	ns	R_X = 5 kΩ, C_X = 0 C_L = 15 pF, Fig. c
		XC		48		
t_w (min)	Minimum Output Pulse Width at Q	XM		90	ns	R_X = 5 kΩ, C_X = 0 C_L = 15 pF, Fig. c
		XC		100		
	Minimum Output Pulse Width at $\overline{Q}$	XM		100		
		XC		110		
t_w	Output Pulse Width		3.08	3.76	μs	R_X = 10 kΩ C_X = 1000 pF, Fig. c
C_{STRAY}	Maximum Stray Capacitance from Pin 2 (14) to Gnd			50	pF	
R_X	Timing Resistor Range	XM	5.0	25	kΩ	
		XC	5.0	50		

DC AND AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		96L Min	96L Max	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage		2.4		V	V_{CC} = Min, I_{OH} = -0.36 mA
V_{OL}	Output LOW Voltage			0.3	V	V_{CC} = Min, I_{OL} = 4.8 mA
V_{IH}	Input HIGH Voltage		2.0		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage			0.7	V	Guaranteed Input LOW Threshold
I_{IH}	Input HIGH Current			20 1.0	μA mA	V_{IN} = 2.4 V V_{IN} = 5.5 V V_{CC} = Max
I_{IL}	Input LOW Current			-0.4	mA	V_{CC} = Max, V_{IN} = 0.3 V
I_{OS}	Output Short Circuit Current		-2.0	-13	mA	V_{CC} = Max, V_{OUT} = 1.0 V
I_{CC}	Power Supply Current			16	mA	V_{CC} = Max
t_{PLH}	Propagation Delay $\overline{I_0}$ to Q	XM XC		75 80	ns	V_{CC} = 5.0 V, R_X = 20 kΩ C_X = 0, C_L = 15 pF T_A = 25° C
t_{PHL}	Propagation Delay $\overline{I_0}$ to $\overline{Q}$	XM XC		62 65	ns	V_{CC} = 5.0 V, R_X = 20 kΩ C_X = 0, C_L = 15 pF T_A = 25° C
t_w (min)	Minimum Output Pulse Width at Q			110*	ns	V_{CC} = 5.0 V, R_X = 20 kΩ C_X = 0, C_L = 15 pF T_A = 25° C
t_w	Output Pulse Width		12.4	15.2	μs	V_{CC} = 5.0 V, R_X = 39 kΩ C_X = 1000 pF, T_A = 25° C
Δt	Change in Q Pulse Width Over Temperature	XC		1.6	%	R_X = 39 kΩ, C_X = 1000 pF
R_X	Timing Resistor Range	XM XC		100 220	kΩ	

*Typical Value



INPUT PULSE
f ≃ 25 kHz
Amp ≃ 3.0 V
Width ≃ 100 ns
$t_r = t_f \leq 10$ ns

Fig. c

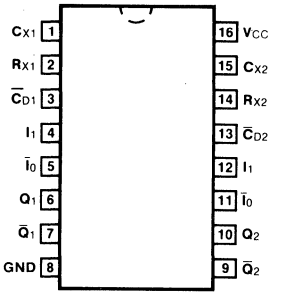
96S02
96LS02

DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

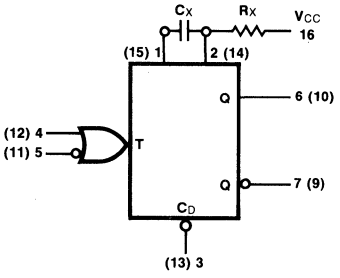
DESCRIPTION — The 96S02 and 96LS02 are dual retriggerable and resettable monostable multivibrators. These one-shots provide exceptionally wide delay range, pulse width stability, predictable accuracy and immunity to noise. The pulse width is set by an external resistor and capacitor. Resistor values up to 1.0 MΩ for the 96LS02 and 2.0 MΩ for the 96S02 reduce required capacitor values. Hysteresis is provided on both trigger inputs of the 96LS02 and on the positive trigger input of the 96S02 for increased noise immunity.

- **REQUIRED TIMING CAPACITANCE REDUCED BY FACTORS OF 10 TO 100 OVER CONVENTIONAL DESIGNS**
- **BROAD TIMING RESISTOR RANGE — 1.0 kΩ to 2.0 MΩ**
- **OUTPUT PULSE WIDTH IS VARIABLE OVER A 2000:1 RANGE BY RESISTOR CONTROL**
- **PROPAGATION DELAY OF 35 ns 96LS02, 12 ns 96S02**
- **0.3 V HYSTERESIS ON TRIGGER INPUTS**
- **OUTPUT PULSE WIDTH INDEPENDENT OF DUTY CYCLE**
- **35 ns TO ∞ OUTPUT PULSE WIDTH RANGE**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

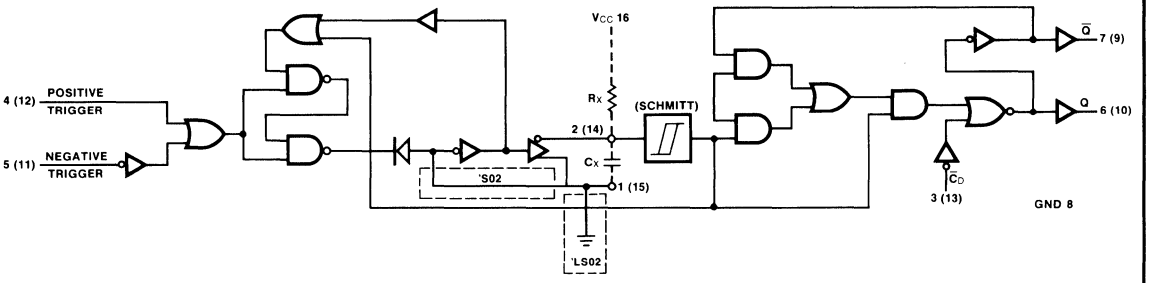
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	96S02PC, 96LS02PC		9B
Ceramic DIP (D)	A	96S02DC, 96LS02DC	96S02DM, 96LS02DM	6B
Flatpak (F)	A	96S02FC, 96LS02FC	96S02FM, 96LS02FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	96S (U.L.) HIGH/LOW	96LS (U.L.) HIGH/LOW
$\overline{I}_0$	Trigger Input (Active Falling Edge)	0.5/0.625	
$\overline{I}_0$	Schmitt Trigger Input (Active Falling Edge)		0.5/0.25
I_1	Schmitt Trigger Input (Active Rising Edge)	0.5/0.625	0.5/0.25
$\overline{C}_D$	Direct Clear Input (Active LOW)	0.5/0.625	0.5/0.25
Q	True Pulse Output	25/12.5	10/5.0 (2.5)
$\overline{Q}$	Complementary Pulse Output	25/12.5	10/5.0 (2.5)

LOGIC DIAGRAM



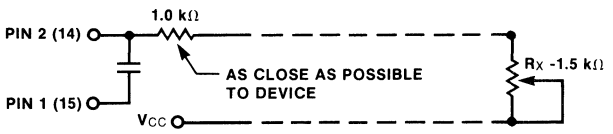
FUNCTIONAL DESCRIPTION — The 96S02 and 96LS02 dual retriggerable resettable monostable multivibrators have two dc coupled trigger inputs per function, one active LOW ($\overline{I}_0$) and one active HIGH (I_1). The I_1 input of both circuit types and the $\overline{I}_0$ input of the 96LS02 utilize an internal Schmitt trigger with hysteresis of 0.3 V to provide increased noise immunity. The use of active HIGH and LOW inputs allows either rising or falling edge triggering and optional non-retriggerable operation. The inputs are dc coupled making triggering independent of input transition times. When input conditions for triggering are met the Q output goes HIGH and the external capacitor is rapidly discharged and then allowed to recharge. An input trigger which occurs during the timing cycle will retrigger the circuit and result in Q remaining HIGH. The output pulse may be terminated (Q to the LOW state) at any time by setting the Direct Clear input LOW. Retriggering may be inhibited by tying the $\overline{Q}$ output to $\overline{I}_0$ or the Q output to I_1. Differential sensing techniques are used to obtain excellent stability over temperature and power supply variations and a feedback Darlington capacitor discharge circuit minimizes pulse width variation from unit to unit. Schottky TTL output stages provide high switching speeds and output compatibility with all TTL logic families.

7

Operation Notes

TIMING

1. An external resistor (R_X) and an external capacitor (C_X) are required as shown in the Logic Diagram. The value of R_X may vary from 1.0 kΩ to 1.0 MΩ (96LS02) or 2.0 MΩ (96S02).
2. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has significant leakage relative to V_{CC}/R_X the timing equations may not represent the pulse width obtained.
3. Polarized capacitors may be used directly. The (+) terminal of a polarized capacitor is connected to pin 1 (15), the (-) terminal to pin 2 (14) and R_X. Pin 1 (15) will remain positive with respect to pin 2 (14) during the timing cycle. In the 96S02, however, during quiescent (non-triggered) conditions, pin 1 (15) may go negative with respect to pin 2 (14) depending on values of R_X and V_{CC}. For values of $R_X \geq 10$ kΩ the maximum amount of capacitor reverse polarity, pin 1 (15) negative with respect to pin 2 (14) is 500 mV. Most tantalum electrolytic capacitors are rated for safe reverse bias operation up to 5% of their working forward voltage rating; therefore, capacitors having a rating of 10 WVdc or higher should be used with the 96S02 when $R_X \geq 10$ kΩ.
4. The output pulse width t_w for $R_X \geq 10$ kΩ and $C_X \geq 1000$ pF is determined as follows:
   (96S02) $t_w = 0.55\ R_X C_X$
   (96LS02) $t_w = 0.43\ R_X C_X$
   Where R_X is in kΩ, C_X is in pF, t is in ns *or* R_X is in kΩ, C_X is in μF, t is in ms.
5. The output pulse width for $R_X < 10$ kΩ or $C_X < 1000$ pF should be determined from pulse width versus C_X or R_X graphs.
6. To obtain variable pulse width by remote trimming, the following circuit is recommended:

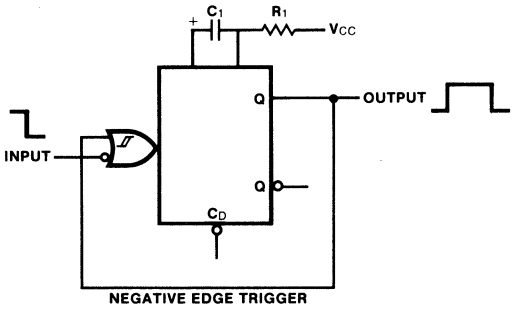


Operation Notes (Cont'd)

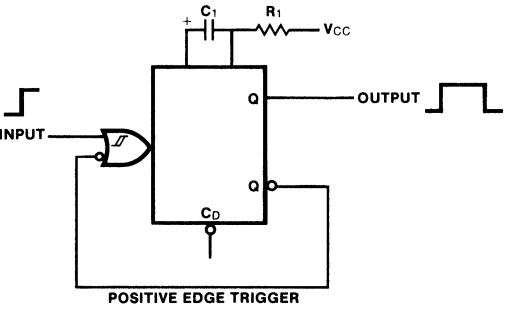
7. Under any operating condition, C_X and R_X (Min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
8. V_{CC} and ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and ground leads do not cause interaction between one shots. Use of a 0.01 μF to 0.1 μF bypass capacitor between V_{CC} and ground located near the circuit is recommended.

TRIGGERING

1. The minimum negative pulse width into $\overline{I}_0$ is 8.0 ns; the minimum positive pulse width into I_1 is 12 ns.
2. Input signals to the 96S02 exhibiting slow or noisy transitions should use the positive trigger input I_1 which contains a Schmitt trigger. Input signals to the 96LS02 exhibiting slow or noisy transitions can use either trigger as both are Schmitt triggers.
3. When non-retriggerable operation is required, i.e., when input triggers are to be ignored during quasi-stable state, input latching is used to inhibit retriggering.



NEGATIVE EDGE TRIGGER



POSITIVE EDGE TRIGGER

4. An overriding active LOW level direct clear is provided on each multivibrator. By applying a LOW to the clear, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW. A LOW-to-HIGH transition on $\overline{C}_D$ will not trigger the 96S02 or 96LS02. If the $\overline{C}_D$ input goes HIGH coincident with a trigger transition, the circuit will respond to the trigger.

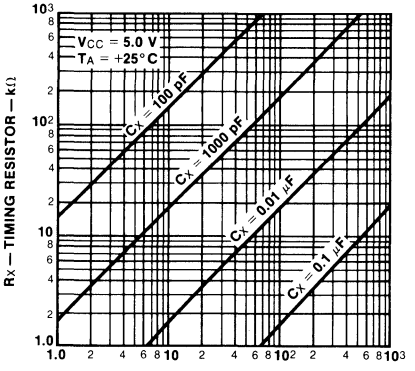
TRIGGERING TRUTH TABLE

PIN NO'S. 5 (11)	4 (12)	3 (13)	OPERATION
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

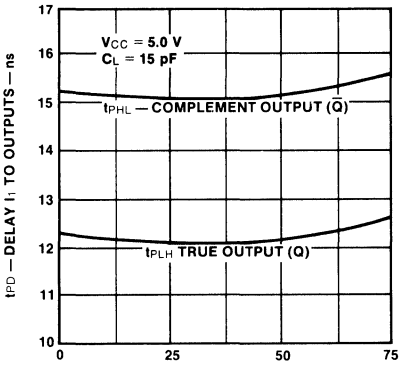
H = HIGH Voltage Level ≥ V_{IH}
L = LOW Voltage Level ≤ V_{IL}
X = Immaterial (either H or L)
H►L = HIGH to LOW Voltage Level transition
L►H = LOW to HIGH Voltage Level transition

TYPICAL CHARACTERISTICS
96S02

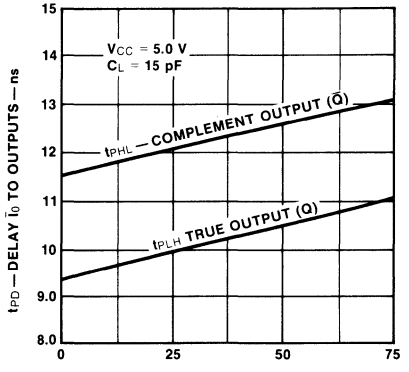
OUTPUT t_w vs R_X and C_X



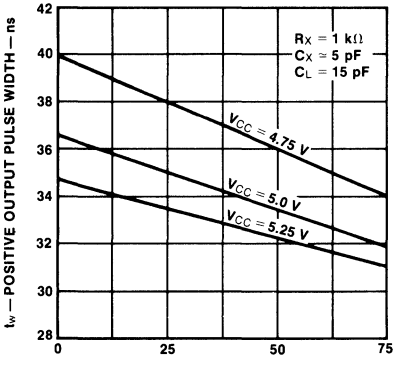
I_1 DELAY TIME vs T_A



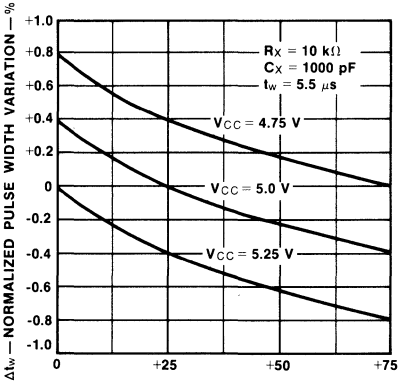
$\bar{I}_0$ DELAY TIME vs T_A



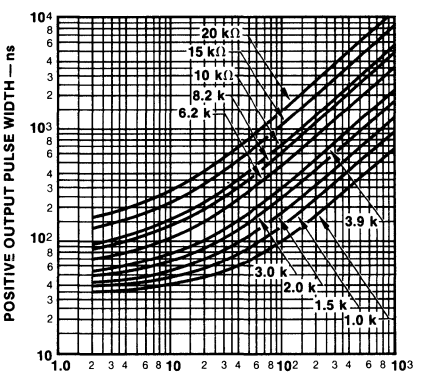
OUTPUT t_w vs T_A



NORMALIZED Δt_w vs T_A

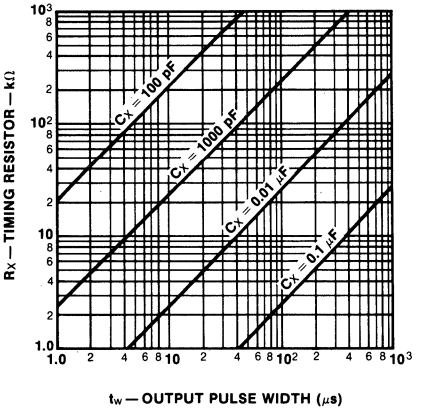


PULSE WIDTH vs R_XC_X

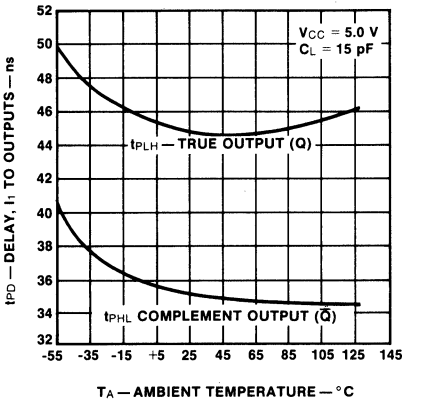


TYPICAL CHARACTERISTICS
96LS02

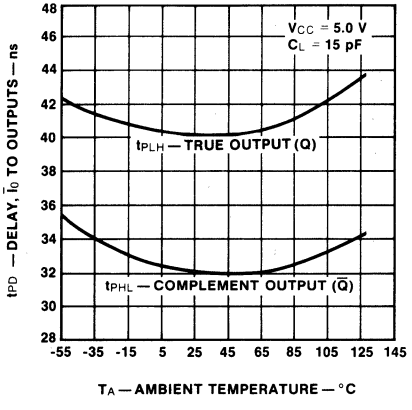
OUTPUT t_W vs R_X and C_X



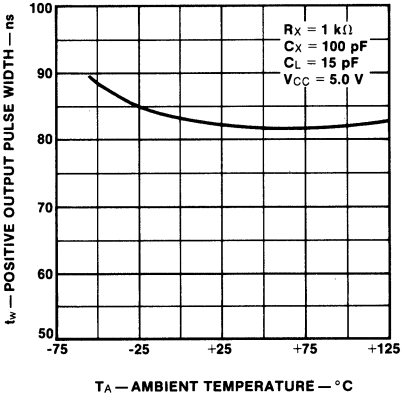
I_1 DELAY TIME vs T_A



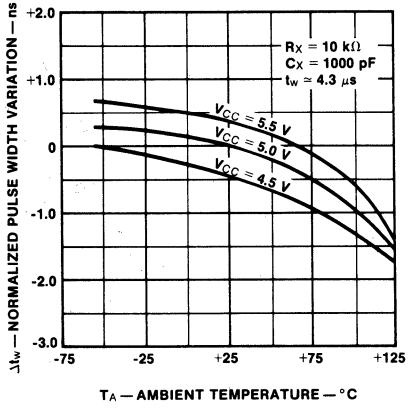
$\bar{I}_0$ DELAY TIME vs T_A



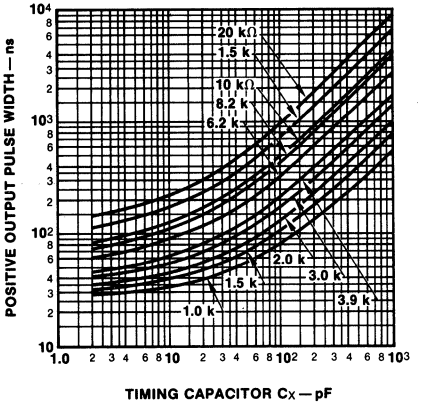
OUTPUT t_W vs T_A



NORMALIZED Δt_W vs T_A



PULSE WIDTH vs R_XC_X



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		96S Min	96S Max	96LS Min	96LS Max	UNITS	CONDITIONS
V_{T+}	Positive-going Threshold Voltage, $\overline{I_0}$, I_1 (96LS02) I_1 (96S02)			2.0		2.0	V	V_{CC} = 5.0 V
V_{T-}	Negative-going Threshold Voltage $\overline{I_0}$, I_1 (96LS02) I_1 (96S02)	XM XC	0.8 0.8		0.7 0.8		V	V_{CC} = 5.0 V
V_{OH}	Output HIGH Voltage	XM XC	2.7 2.7		2.5 2.7		V	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} I_{OH} = -400 μA ('LS02) I_{OH} = -1.0 mA ('S02)
V_{OL}	Output LOW Voltage	XM XC		0.5 0.5		0.5 0.4	V	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}
V_{CX}	Capacitor Voltage Pin 1 (15) Referenced to Pin 2 (14)		-0.85 -0.5 -0.4	3.0 3.0 3.0	0 0 0	3.0 3.0 3.0	V	R_X = 1.0 kΩ R_X = > 10 kΩ R_X > 1.0 MΩ V_{CC} = 4.75 V to 5.25 V
I_{IH}	Input HIGH Current			20 0.1		20 0.1	μA mA	V_{IN} = 2.7 V V_{IN} = 5.5 V ('S02) V_{IN} = 10 V ('LS02) V_{CC} = Max
I_{IL}	Input LOW Current			-1.0		-0.4	mA	V_{IN} = 0.4 V, V_{CC} = Max
I_{OS}	Output Short Circuit Current		-40	-100	-20	-100	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current			75		36	mA	V_{IN} = Open, V_{CC} = Max

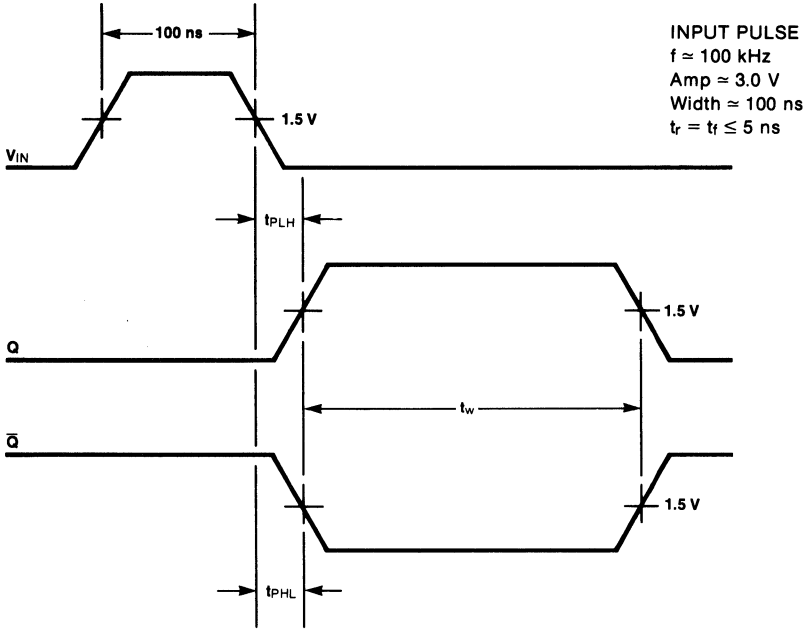


Fig. a

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER		96S C_L = 15 pF Min	96S C_L = 15 pF Max	96LS C_L = 15 pF Min	96LS C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH}	Propagation Delay $\overline{I_0}$ to Q			15		55	ns	Fig. a
t_{PHL}	Propagation Delay $\overline{I_0}$ to $\overline{Q}$			19		50	ns	
t_{PLH}	Propagation Delay I_1 to Q			19		60	ns	
t_{PHL}	Propagation Delay I_1 to $\overline{Q}$			20		55	ns	
t_{PHL}	Propagation Delay $\overline{C_D}$ to Q			20		30	ns	
t_{PLH}	Propagation Delay $\overline{C_D}$ to $\overline{Q}$			14		35	ns	
t_w (L)	$\overline{I_0}$ Pulse Width LOW		8.0		15		ns	
t_w (H)	I_1 Pulse Width HIGH		12		30		ns	
t_w (L)	$\overline{C_D}$ Pulse Width LOW		7.0		22		ns	
t_w (H)	Minimum Q Pulse Width HIGH		30	45	25	55	ns	R_X = 1.0 kΩ, C_X = 10 pF including jig and stray
t_w	Q Pulse Width		5.2	5.8	4.1	4.5	μs	R_X = 10 kΩ, C_X = 1000 pF
R_X	Timing Resistor Range*		1.0	2000	1.0	1000	kΩ	T_A = -55°C to +125°C, V_{CC} = 4.5 V to 5.5 V
t	Change in Q Pulse Width over Temperature	XM				3.0	%	R_X = 10 kΩ, C_X = 1000 pF
		XC		1.0		1.0		
t	Change in Q Pulse Width over V_{CC} Range			1.0		0.8	%	T_A = 25°C, V_{CC} = 4.75 V to 5.25 V, R_X = 10 kΩ, C_X = 1000 pF
						1.5		T_A = 25°C, V_{CC} = 4.5 V to 5.5 V, R_X = 10 kΩ, C_X = 1000 pF

*Applies only over commercial V_{CC} and T_A range for 96S02.

96LS32

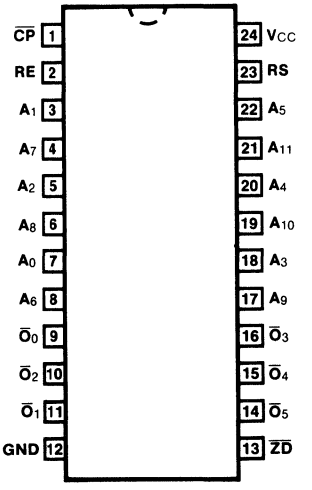
ADDRESS MULTIPLEXER/REFRESH COUNTER

(For 4K Dynamic RAMs)

DESCRIPTION — The 96LS32 is an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of up to six input addresses (or 4K bits for 64 x 64 organization). It multiplexes 12 bits of system applied address to six output address pins. The device also contains a 6-bit refresh counter which is externally clocked so that either distributed or burst refresh may be used. The high performance of the 96LS32 makes it especially suitable for use with high speed n-channel RAMs like the M4027. The 96LS32 operates from a single +5.0 V power supply and is specified for operation over a 0°C to +75°C ambient temperature range.

- **SIMPLIFIES SYSTEM DESIGN**
- **REDUCES PACKAGE COUNT**
- **DRIVES HIGH CAPACITANCE LOADS**
- **USE FOR DISTRIBUTED OR BURST REFRESH**
- **STANDARD 24-PIN DUAL IN-LINE PACKAGE**
- **LOW POWER SCHOTTKY DESIGN MINIMIZES POWER CONSUMPTION**

CONNECTION DIAGRAM
PINOUT A



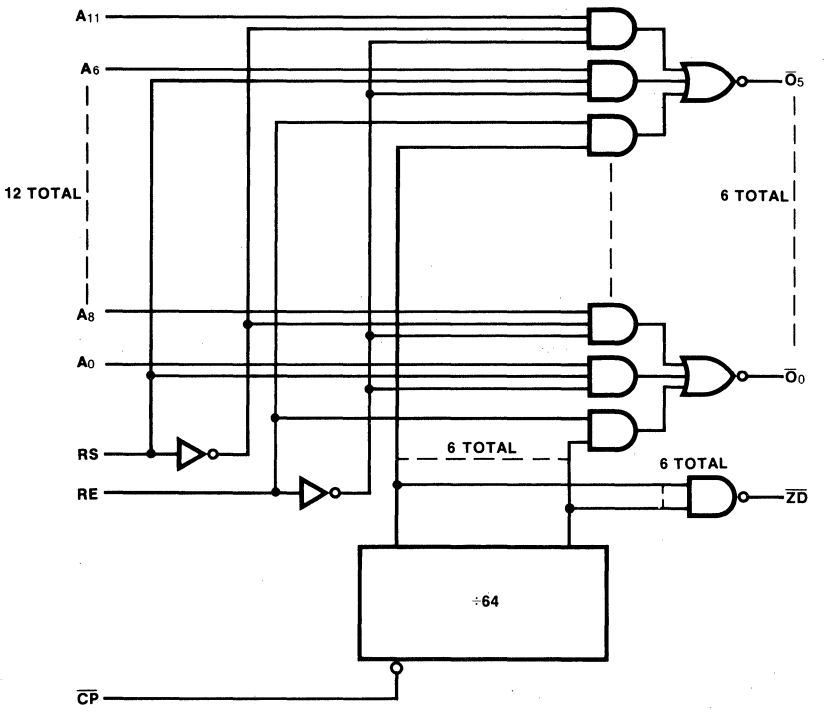
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	96LS32PC		9N
Ceramic DIP (D)	A	96LS32DC	96LS32DM	6N
Flatpak (F)	A	96LS32FC	96LS32FM	4M

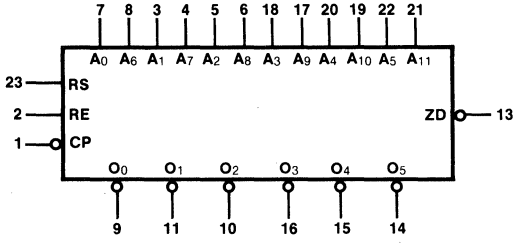
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	96XX (U.L.) HIGH/LOW
A_0 — A_5	Row Address Inputs	0.5/0.13
A_6 — A_{11}	Column Address Inputs	0.5/0.13
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	0.5/0.13
RE	Refresh Enable Input (Active HIGH)	0.5/0.13
RS	Row Select Input (Active HIGH)	0.5/0.13
$\overline{ZD}$	Refresh Counter Zero Detect Output (Active LOW)	25/3.1
$\overline{O}_0$ — $\overline{O}_5$	Address Outputs	25/3.1

LOGIC DIAGRAM



LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

FUNCTIONAL DESCRIPTION — The 96LS32 address multiplexer/refresh counter performs the following functions:

1. Row, Column and Refresh Address multiplexing
2. Address counting for burst or distributed refresh

These functions are controlled by two signals, Refresh Enable and Row Select, both of which are active HIGH TTL inputs. the Function Table shows the levels required to multiplex to the output:

1. Refresh address (from internal counter)
2. Row addresses (A_0 through A_5)
3. Column addresses (A_6 through A_{11})

BURST REFRESH MODE — When refresh is requested the Refresh Enable input is HIGH. This input is ANDed with the six outputs of the internal 6-bit counter. At each $\overline{CP}$ pulse the counter increments by one, sequencing the outputs ($\overline{O}_0 - \overline{O}_5$) through all 64 row addresses. When the counter sequences to all zeroes, the Zero Detect output goes LOW signaling the end of the refresh sequence. Due to counter decoding spikes, the Zero Detect output is valid only after t_{cz} following the LOW going edge of $\overline{CP}$.

DISTRIBUTED REFRESH MODE — In the distributed refresh mode, one row is selected for refresh each ($t_{refresh/n}$) time where n = number of rows in the device and refresh is the specified refresh rate for the device. For the M4027, $t_{refresh}$ = 2.0 ms and n = 64, therefore one row is refreshed each 31 μs. Following the refresh cycle at row n, the $\overline{CP}$ input is pulsed, advancing the refresh address by one row so that the next refresh cycle will be performed on row n + 1. The $\overline{CP}$ input may be pulsed following each refresh cycle or within the refresh cycle after the specified memory device address hold time.

ROW AND COLUMN ADDRESS — All twelve system address lines are applied to the inputs of the 96LS32. When Refresh Enable is LOW and Row Select is HIGH, the input addresses $A_0 - A_5$ are gated to the outputs and applied to the driven memories. Conversely, when Row Select is LOW (with Refresh Enable still LOW), input addresses $A_6 - A_{11}$ are gated to the outputs and applied to the driven memories. When memory devices are driven directly by the 96LS32, the address applied to the memory devices is the inverse of the address at the inputs due to the inverted outputs of the 96LS32. This should be remembered when checking out the memory system.

FUNCTION TABLE

Refresh Enable	Row Select	Outputs
H	X	Refresh Address (from internal counter)
L	H	Row Address (complement of $A_0 - A_5$)
L	L	Column Address (complement of $A_6 - A_{11}$)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

96LS42

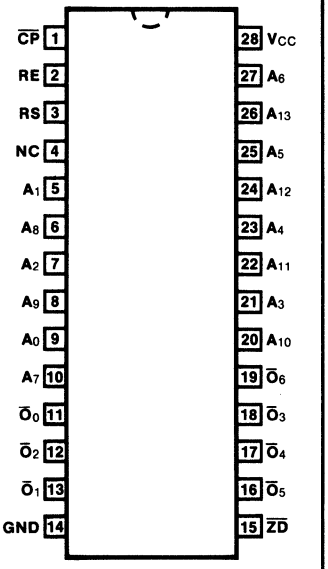
ADDRESS MULTIPLEXER/REFRESH COUNTER

(For 16K Dynamic RAMs)

DESCRIPTION — The 96LS42 is an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of 64 or 128 cycles. It multiplexes 14 bits of system supplied address to seven output address pins. The device also contains a 7-bit refresh counter which is externally controlled so that either distributed or burst refresh may be used. The high performance of the 96LS42 makes it especially suitable for use with high speed n-channel RAMs like the F16K. The 96LS42 is manufactured using Fairchild's advanced low power Schottky process.

- **SIMPLIFIES SYSTEM DESIGN**
- **REDUCES PACKAGE COUNT**
- **DRIVES HIGH CAPACITIVE LOADS**
- **EITHER BURST OR DISTRIBUTED REFRESH**
- **LOW POWER SCHOTTKY DESIGN**
- **STANDARD 28-PIN PACKAGE**

CONNECTION DIAGRAM
PINOUT A



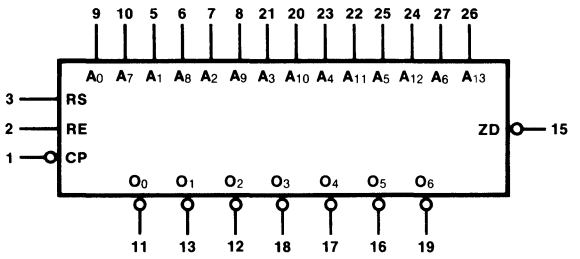
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	96LS42PC		9Y
Ceramic DIP (D)	A	96LS42DC	96LS42DM	8E

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

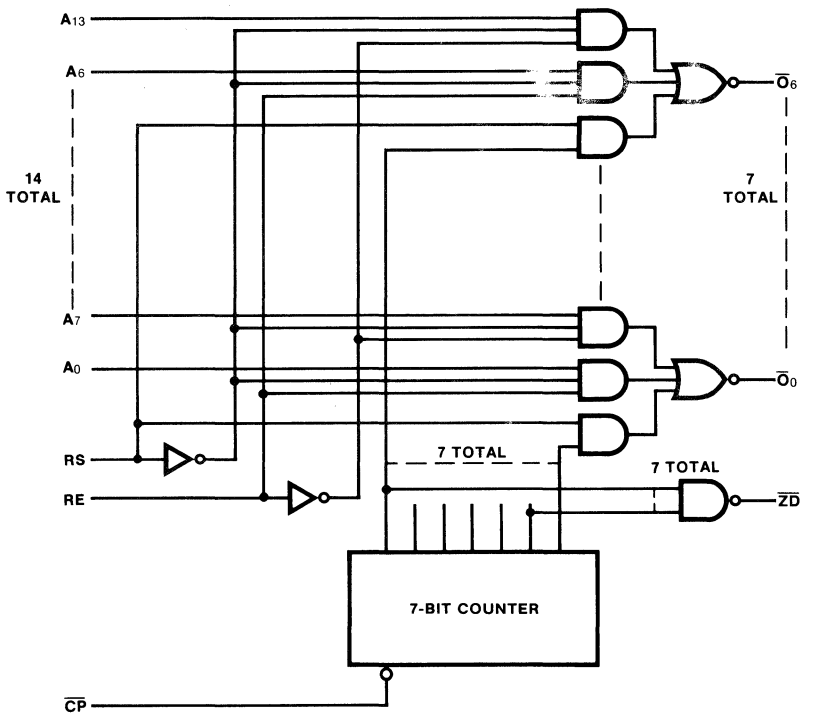
PIN NAMES	DESCRIPTION	96XX (U.L.) HIGH/LOW
A_0 — A_6	Row Address Inputs	0.5/0.13
A_7 — A_{13}	Column Address Inputs	0.5/0.13
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	0.5/0.13
RE	Refresh Enable Input	0.5/0.13
RS	Row Select Input	0.5/0.13
$\overline{ZD}$	Refresh Counter Zero Detect Output (Active LOW)	25/3.1
$\overline{O}_0$ — $\overline{O}_6$	Multiplexer Outputs (Active LOW)	25/3.1

LOGIC SYMBOL



V_{CC} = Pin 28
GND = Pin 14

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The 96LS42 address multiplexer/refresh counter performs the following functions:

1. Row, Column and Refresh Address multiplexing
2. Address counting for burst or distributed refresh

These functions are controlled by two signals, Refresh Enable and Row Select, both of which are active HIGH TTL inputs. The Function Table shows the levels required to multiplex to the output:

1. Refresh addresses (from internal counter)
2. Row addresses (A_0 through A_6)
3. Column addresses (A_7 through A_{13})

Burst Refresh Mode — When refresh is requested the Refresh Enable input is HIGH. This input is AND-ed with the seven outputs of the internal 7-bit counter. At each $\overline{CP}$ pulse the counter increments by one, sequencing the outputs ($\overline{O}_0 - \overline{O}_6$) through all 128 row addresses. When the counter sequences to all zeroes, the Zero Detect output goes LOW signaling the end of the refresh sequence. Due to counter decoding spikes, the Zero Detect output is valid only after t_{CZ} following the LOW going edge of $\overline{CP}$.

Distributed Refresh Mode — In the distributed refresh mode, one row is selected for refresh each ($t_{refresh/n}$) time where n = number of rows in the device and refresh is the specified refresh rate for the device. For the F16 k, Refresh = 2.0 ms and n = 128, therefore one row is refreshed each 62 μS. Following the refresh cycle at row n, the $\overline{CP}$ input is pulsed, advancing the refresh address by one row so that the next refresh cycle will be performed on row n + 1. The $\overline{CP}$ input may be pulsed following each refresh cycle or within the refresh cycle after the specified memory device address hold time.

Row and Column Address — All 14 system address lines are applied to the inputs of the 96LS42. When Refresh Enable is LOW and Row Select is HIGH, the input Addresses $A_0 - A_6$ are gated to the outputs and applied to the driven memories. Conversely, when Row Select is LOW (with Refresh Enable still LOW). Input addresses $A_7 - A_{13}$ are gated to the outputs and applied to the driven memories. When memory devices are driven directly by the 96LS42, the address applied to the memory devices is the inverse of the address at the inputs due to the inverted outputs of the 96LS42. This should be remembered when checking out the memory system.

FUNCTION TABLE

Refresh Enable	Row Select	Outputs
H	X	Refresh Address (from internal counter)
L	H	Row Address (complement of $A_0 - A_6$)
L	L	Column Address (complement of $A_7 - A_{13}$)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

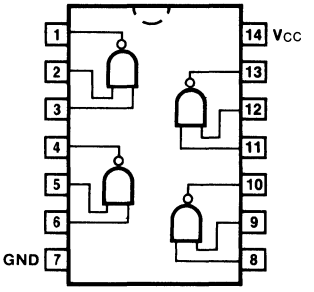
96101

QUAD 2-INPUT POSITIVE NAND BUFFER

(With Open-Collector Output)

DESCRIPTION — The 96101 is similar to the 54/7439, except that the outputs are specified at three levels of I_{OL}; in the HIGH state the I_{OH} current is specified at two levels of V_{OH}. During switching transitions, output current change rate is typically 4.0 mA/ns.

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +75°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	96101PC		9A
Ceramic DIP (D)	A	96101DC	96101DM	6A

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	96XX (U.L.) HIGH/LOW	
Inputs	1.0/1.0	
Outputs	OC**/30	

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	96XX Min	96XX Max	UNITS	CONDITIONS	
V_{IH}	Input HIGH Voltage	2.0		V		
V_{IL}	Input LOW Voltage		0.8	V		
V_{OL}	Output LOW Voltage		0.4 0.5 0.6	V	I_{OL} = 48 mA I_{OL} = 60 mA I_{OL} = 80 mA	V_{CC} = Min V_{IN} = V_{IH}
I_{OH}	Output HIGH Current		25 50	µA	V_{OH} = 3.5 V V_{OH} = 5.5 V	V_{CC} = Min V_{IN} = V_{IL}
I_{IH}	Input HIGH Current		40 1.0	µA mA	V_{IN} = 2.4 V V_{IN} = 5.5 V	V_{CC} = Max
I_{IL}	Input LOW Current		-1.6	mA	V_{IN} = 0.4 V, V_{CC} = Max	
I_{CCH} I_{CCL}	Power Supply Current		8.5 54	mA	V_{IN} = Gnd V_{IN} = Open	V_{CC} = Max
t_{PLH} t_{PHL}	Propagation Delay Input to Output		22 25	ns	C_L = 45 pF, R_L = 120 Ω Figs. 3-2, 3-4	

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V. **OC — Open Collector

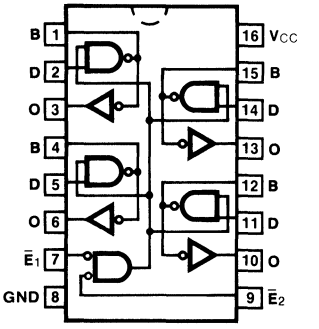
96103

QUAD BUS TRANSCEIVER

(With Common Enable)

DESCRIPTION — Each transceiver contains an open-collector buffer whose output is common to an inverting gate input. When both Enable inputs ($\overline{E}_1$ and $\overline{E}_2$) are LOW, the buffer is enabled, with its output state determined by its Data (D) input. When either Enable input is HIGH, the buffer is disabled (output OFF) and the bus signal is determined by other circuits connected to the bus. The receiver gate has greater input noise immunity than standard TTL, while its output signal levels are standard TTL. In the power-down condition, the B terminal leakage is limited to 100 μA.

CONNECTION DIAGRAM
PINOUT A



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +75°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	96103PC		9B
Ceramic DIP (D)	A	96103DC	96103DM	6B
Flatpak (F)	A	96103FC	96103FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	96XX (U.L.) HIGH/LOW
D	Data Input	1.0/1.0
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)	1.0/1.0
B	Bus Terminal, as Input	2.5/0.05
	as Output	OC*/70 mA
O	Receiver Output	50/12.5

*OC — Open Collector

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		96XX Min	96XX Max	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage at B			0.7	V	I_{OL} = 70 mA, V_{IH} = 2.0 V V_{CC} = Min
V_{IL}	Input LOW Voltage at D or $\overline{E}$	XC		0.8	V	
		XM		0.7		
V_{IHR}	Receiver HIGH Threshold Voltage	XC	1.53		V	V_{CC} = Min
		XM	1.49			
		XC	1.7		V	V_{CC} = Max
		XM	1.84			
V_{ILR}	Receiver LOW Threshold Voltage	XC		1.3	V	V_{CC} = Min
		XM		1.21		
		XC		1.47	V	V_{CC} = Max
		XM		1.56		
I_{OH}	Bus Output HIGH Current			100	μA	V_{CC} = 0 V to Max V_{OH} = 4.0 V, V_D = V_{IL}
I_{IL}	Input LOW Current at B			-85	μA	V_{OUT} = 0 V, V_{CC} = Max V_D = V_{IL}
I_{OS}	Output Short Circuit Current at O		-18	-55	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current			90	mA	D input = 4.5 V V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	96XX C_L = 15 pF Min	96XX C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to B		30 23	ns	R_L = 91 Ω to V_{CC}, 200 Ω to Gnd Figs. 3-4, 3-5
t_{PLH} t_{PHL}	Propagation Delay D to B		25 15	ns	
t_{PLH} t_{PHL}	Propagation Delay B to O	10 10	30 30	ns	R_L = 390 Ω to V_{CC} 1.6 kΩ to Gnd, Fig. 3-4
t_{PLH} t_{PHL}	Propagation Delay B to O	10 10	35 35	ns	R_L= 390 Ω to V_{CC} 1.6 kΩ to Gnd C_L = 50 pF, Fig. 3-4

7

96106

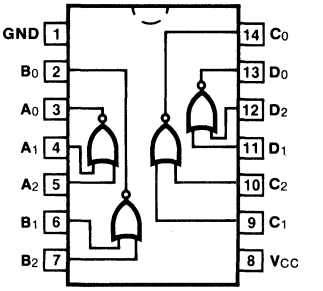
QUAD 2-INPUT NOR RECEIVER

DESCRIPTION — The 96106 inputs are designed to provide higher noise immunity than standard TTL inputs and also present less loading to the signal source. Also, in the power down condition, input leakage is 80 μA or less, making the 96106 well suited for data bus applications. Output signal levels are standard TTL.

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +75°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	96106PC		9A
Ceramic DIP (D)	A	96106DC	96106DM	6A
Flatpak (F)	A	96106FC	96106FM	3I

CONNECTION DIAGRAM
PINOUT A



V_{CC} = Pin 8
GND = Pin 1

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

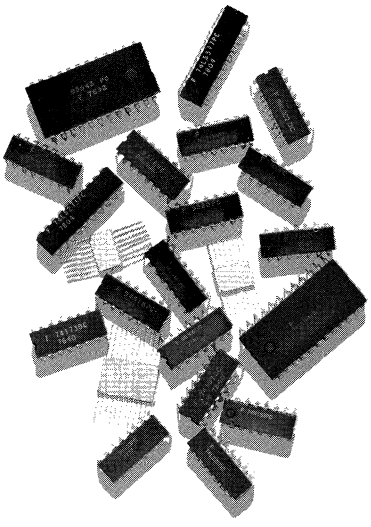
PINS	96XX (U.L.) HIGH/LOW
Inputs	2.0/0.006
Outputs	50/12.5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		96XX Min	96XX Max	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	XC	1.53		V	V_{CC} = Min
		XM	1.49			
		XC	1.70		V	V_{CC} = Max
		XM	1.84			
V_{IL}	Input LOW Voltage	XC		1.30	V	V_{CC} = Min
		XM		1.21		
		XC		1.47	V	V_{CC} = Max
		XM		1.56		
I_{IH}	Input HIGH Current			80	μA	V_{CC} = 0 V to Max, V_{IN} = 4.0 V
I_{IL}	Input LOW Current			-10	μA	V_{CC} = Max, V_{IN} = 0 V
I_{OS}	Output Short Circuit Current		-18	-55	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CCH}	Power Supply Current			40	mA	V_{IN} = 4.5 V; V_{CC} = Max
I_{CCL}				20		V_{IN} = 0 V; V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	96XX		UNITS	CONDITIONS
		C_L = 15 pF			
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay	10 10	30 30	ns	R_L = 390 Ω to V_{CC}, 1.6 kΩ to Gnd, Fig. 3-4
t_{PLH} t_{PHL}	Propagation Delay	10 10	35 35	ns	R_L = 390 Ω to V_{CC} 1.6 kΩ to Gnd C_L = 50 pF, Fig. 3-4



Section 8
OTHER DIGITAL PRODUCTS

RTL MICROLOGIC AND CTL COUNTING MICROLOGIC ELEMENTS

DEVICE NO.	DESCRIPTION	LOGIC/ CONN. DIAGRAM	PKG TYPE	DEVICE NO.	DESCRIPTION	LOGIC/ CONN. DIAGRAM	PKG TYPE
900	Buffer	F8	3F, 5B	**913**	D Flip-Flip	F6	3F, 5B
901	Counter Adapter	F18	3F, 5B	**914**	Dual 2-NOR	F13	3F, 5B
902	Flip-Flop	F19	3F, 5B	**915**	Dual 3-NOR	F14	3F, 5F
903	3-Input NOR	F9	3F, 5B	**921**	Dual 2-Expander	F7	3F, 5B
904	Half Adder	F10	3F, 5B	**923**	JK Flip-Flop	F15	5B
905	Half Shift	F11	3F, 5B	**926**	JK Flip-Flop	F16	3F, 5F
906	Half Shift	F20	3F, 5B	**927**	Quad Inverter	F17	3F, 5F
907	4-Input NOR	F12	3F, 5B	**958**	Decade Counter	F21	5B, 6A
908	Adder	F1	3F, 5B	**959**	4-Bit Latch	F22	6B
909	Buffer	F2	3F, 5B	**960**	BCD Decoder/Dvr	F23	6B
910	Dual 2-NOR	F3	3F, 5B	**974**	JK Flip-Flop	F15	5B
911	4-Input NOR	F4	3F, 5B	**989**	Binary Counter	F21	5B, 6A
912	Half Adder	F5	3F, 5B				

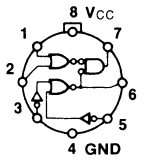
DTL MICROLOGIC

DEVICE NO.	DESCRIPTION	LOGIC/CONN. DIAGRAM	PKG TYPE
930	Dual 4-Input Extendable NAND Gate	G1	3I, 5F, 6A, 9A
932	Dual 4-Input Extendable NAND Buffer Gate	G1	3I, 5F, 6A, 9A
933	Extender	G9	5F, 9A
935	Extendable Hex Inverter	G12	3I, 6A, 9A
936	Hex Inverter	G12	3I, 6A, 9A
937	Hex Inverter	G12	3I, 6A, 9A
941	Monostable Multivibrator	G17	3I, 6A
944	Dual 4-Input Extendable NAND Buffer Gate (Open-Collector)	G1	3I, 5F, 6A, 9A
945	RS Flip-Flop	G18	3I, 5F, 6A, 9A
946	Quad 2-Input NAND Gate	G10	3I, 5F, 6A, 9A
948	RS Flip-Flop	G18	3I, 5F, 6A, 9A

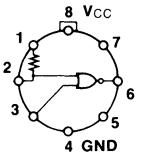
DTL MICROLOGIC (Cont'd)

DEVICE NO.	DESCRIPTION	LOGIC/CONN. DIAGRAM	PKG TYPE
949	Quad 2-Input NAND Gate	G10	3I, 5F, 6A, 9A
950	A-C Coupled RS Flip-Flop	G19	3I, 5F, 6A, 9A
951	Monostable Multivibrator	G17	3I, 5F, 6A, 9A
961	Dual 4-Input Extendable NAND Gate	G1	3I, 5F, 6A, 9A
962	Triple 3-Input NAND Gate	G11	3I, 5F, 6A, 9A
963	Triple 3-Input NAND Gate	G11	3I, 5F, 6A, 9A
1800	Dual 5-Input NAND Gate	G1	9A
1801	Dual 5-Input NAND Gate	G1	9A
1802	Single 8-Input NAND Gate	G2	9A
1803	Single 8-Input NAND Gate	G2	9A
1804	Single 10-Input NAND Gate	G3	9A
1805	Single 10-Input NAND Gate	G3	9A
1806	Quad 2-Input AND Gate	G4	9A
1807	Quad 2-Input AND Gate	G4	9A
1808	Quad 2-Input OR Gate	G5	9A
1809	Quad 2-Input OR Gate	G5	9A
1810	Quad 2-Input NOR Gate	G6	9A
1811	Quad 2-Input NOR Gate	G6	9A
1812	Quad 2-Input Exclusive-OR Gate	G7	9A
1813	Quad Latch	G13	9B
1814	Quad Latch	G14	9A
9093	Dual JK Flip-Flop	G15	3I, 6A, 9A
9094	Dual JK Flip-Flop	G15	3I, 6A, 9A
9097	Dual JK Flip-Flop	G16	3I, 6A, 9A
9099	Dual JK Flip-Flop	G16	3I, 6A, 9A
9109	High Voltage Hex Inverter	G12	6A
9110	High Voltage Hex Inverter	G12	6A
9111	RS Flip-Flop	G20	3I, 6A
9112	High Voltage Hex Inverter	G12	6A
9135	Hex Inverter (Open-Collector)	G12	3I, 6A, 9A
9157	Quad 2-Input Buffered NAND Gate	G8	3I, 6A, 9A
9158	Quad 2-Input Power NAND Gate	G8	6A, 9A

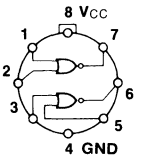
F1
908



F2
909



F3
910



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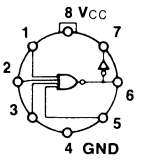

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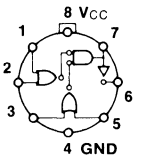

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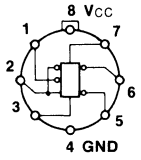

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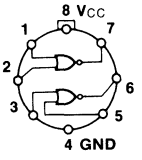

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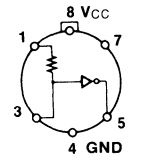

F9
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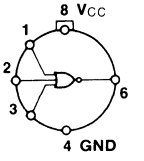

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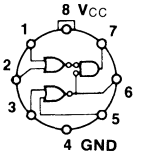

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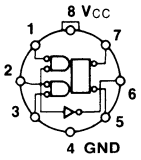

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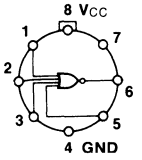

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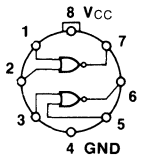

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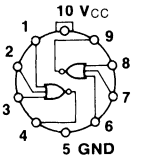
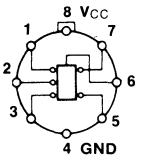


F15
923, 974



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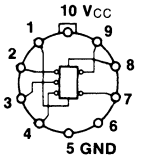
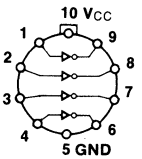


F17
927



F18
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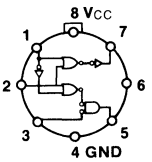

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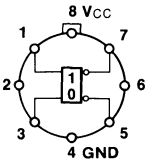

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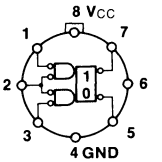
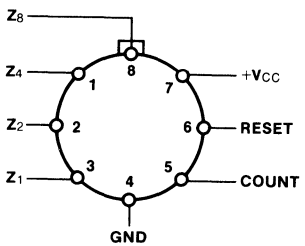


F21
958, 989



F22
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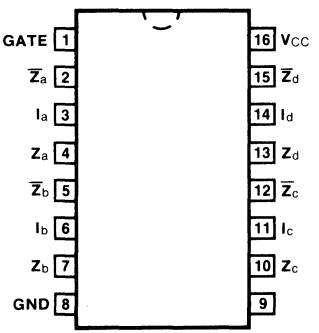
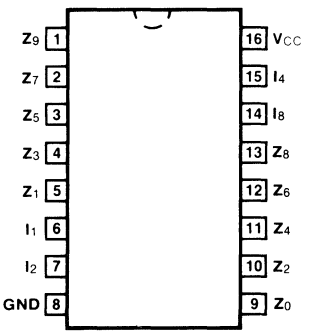
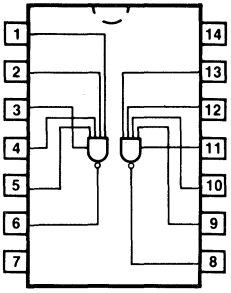


F23
960



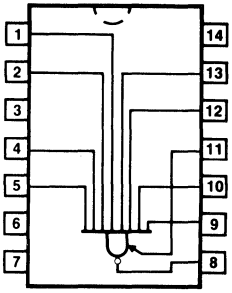
8

G1
930, 932
944, 961
1800, 1801



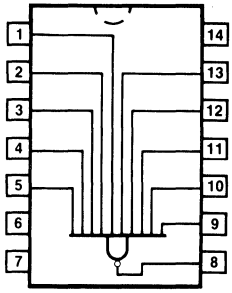
V_{CC} = Pin 14
GND = Pin 7

G2
1802, 1803



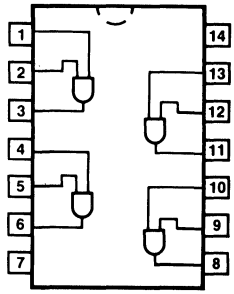
V_{CC} = Pin 14
GND = Pin 7

G3
1804, 1805



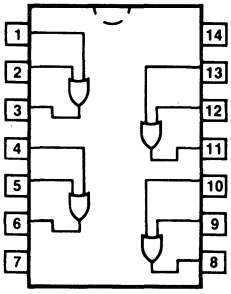
V_{CC} = Pin 14
GND = Pin 7

G4
1806, 1807



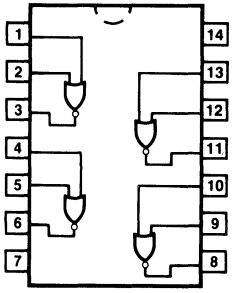
V_{CC} = Pin 14
GND = Pin 7

G5
1808, 1809



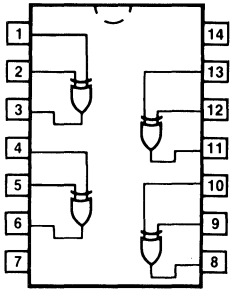
V_{CC} = Pin 14
GND = Pin 7

G6
1810, 1811



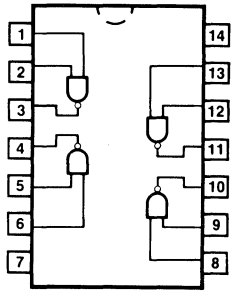
V_{CC} = Pin 14
GND = Pin 7

G7
1812



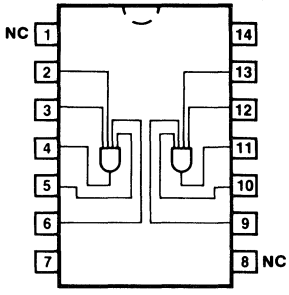
V_{CC} = Pin 14
GND = Pin 7

G8
9157, 9158



V_{CC} = Pin 14
GND = Pin 7

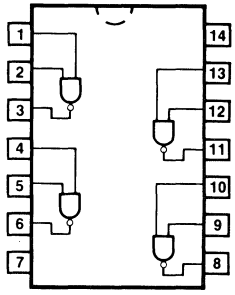
G9
933



No connection required to V_{CC} (Pin 14).

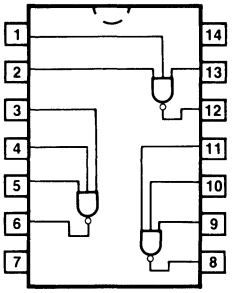
V_{CC} = Pin 14
GND = Pin 7

G10
946, 949



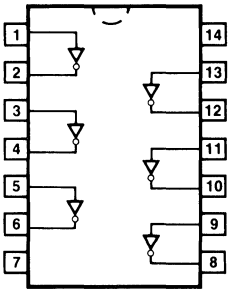
V_{CC} = Pin 14
GND = Pin 7

G11
962, 963



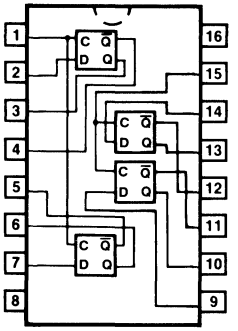
V_{CC} = Pin 14
GND = Pin 7

G12
9109, 9110, 9112
9135, 935, 936
937



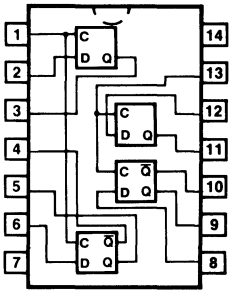
V_{CC} = Pin 14
GND = Pin 7

G13
1813



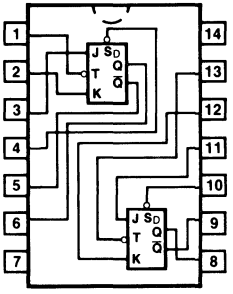
V_{CC} = Pin 16
GND = Pin 8

G14
1814



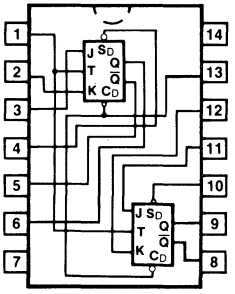
V_{CC} = Pin 14
GND = Pin 7

G15
9093, 9094



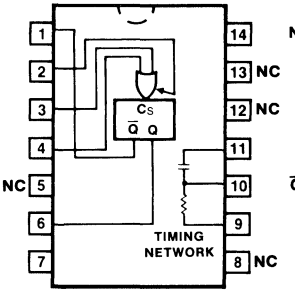
V_{CC} = Pin 14
GND = Pin 7

G16
9097, 9099



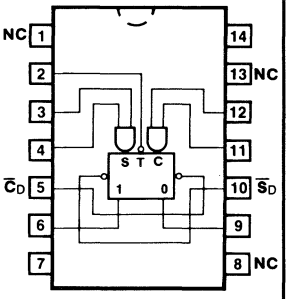
V_{CC} = Pin 14
GND = Pin 7

G17
941, 951



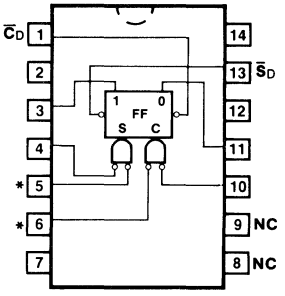
V_{CC} = Pin 14
GND = Pin 7

G18
945, 948



V_{CC} = Pin 14
GND = Pin 7

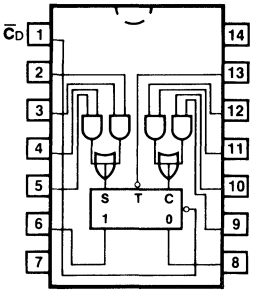
G19
950



*These inputs are capacitively coupled.

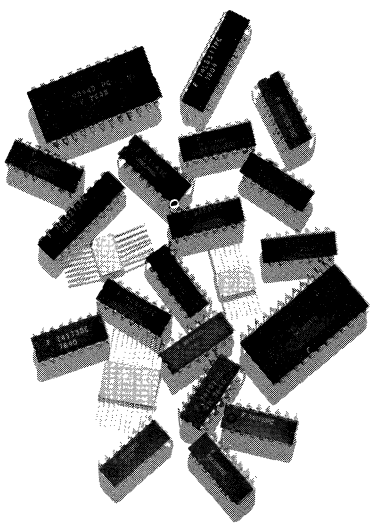
V_{CC} = Pin 14
GND = Pin 7

G20
9111



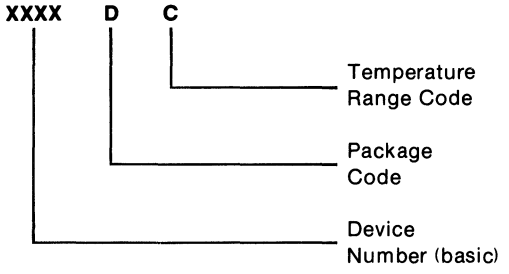
V_{CC} = Pin 14
GND = Pin 7

8



Section 9
ORDERING INFORMATION AND PACKAGE OUTLINES

Specific ordering codes, as well as the temperature ranges and package types available, are listed on the first page of each data sheet in Section 4 through Section 7. The product indices and selection guides given in Section 1 list only the "basic" device numbers. This basic number is used to form part of a simplified purchasing code where the package style and temperature range are defined as follows:



TEMPERATURE RANGE — Two basic temperature grades are in common use:

C = Commercial
0° C to +70° C/75° C

M = Military
-55° C to +125° C

PACKAGE CODE — One letter represents the basic package style. Different package outlines exist within each package style to accommodate varying die sizes and number of pins, as indicated below:

D — Ceramic/Hermetic Dual In-line
4E, 6A, 6B, 6N, 7B, 8E

F — Flatpak
3F, 3I, 4F, 4L, 4M

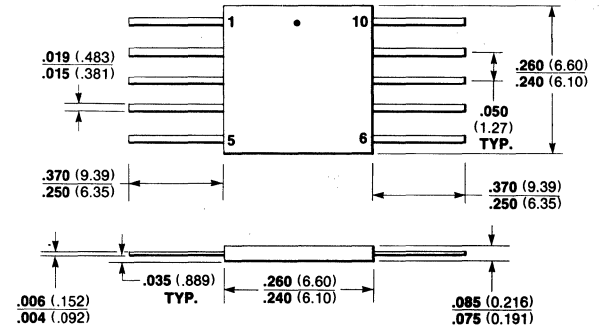
H — Metal Can
5B, 5F

P — Plastic Dual In-line
9A, 9B, 9N, 9Y, 9Z

PACKAGE OUTLINES — The package outlines indicated by the codes above are shown in the detailed outline drawings in this section.

FAIRCHILD PACKAGE OUTLINES

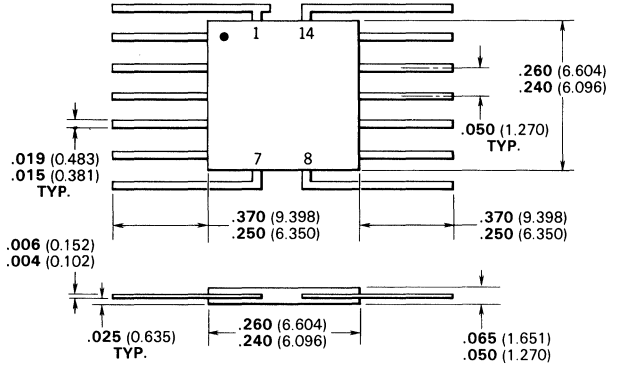
JEDEC TO-91 OUTLINE



3F

NOTES:
Leads are tin plated 42 alloy
Hermetically sealed alumina package
Cavity size is .130 (3.30) diameter
Package weight is 0.26 grams

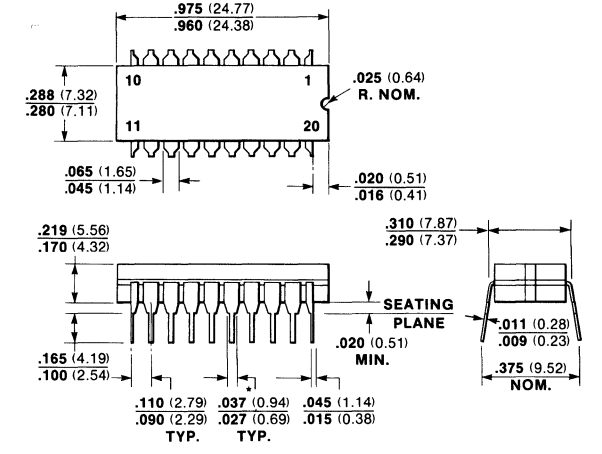
JEDEC TO-86 OUTLINE



3I

NOTES:
Leads are tin-plated 42 alloy
Hermetically sealed alumina package
Lead 1 orientation may be either tab or dot
Cavity size is .130 (3.30)
Package weight is 0.26 gram

20-PIN CERDIP

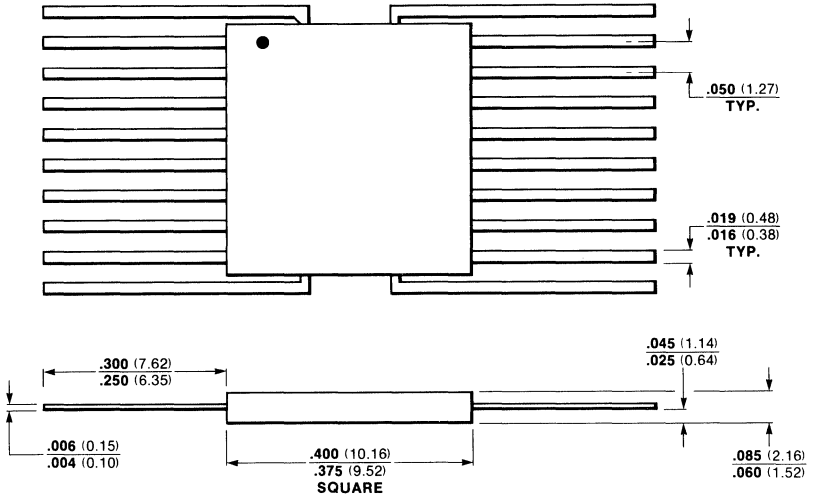


4E

NOTES:
Pins are tin-plated kovar or nickel alloy 42
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .030 (0.76) inch diameter pins
Hermetically sealed alumina package (black)
Cavity size is .140 x .250 (3.56 x 6.35)
*The .037-.027 dimension does not apply to the corner pins
Package weight is 2.4 grams

All dimensions in inches (bold) and millimeters (parentheses)

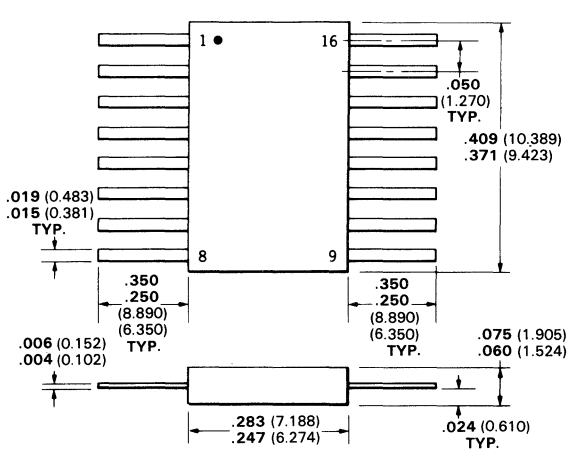
20-PIN CERPAK



4F

NOTES:
Leads are tin plated nickel alloy
Base is AL_2O_3
Cavity size 200 x 200
Package weight ≈ 0.8 grams

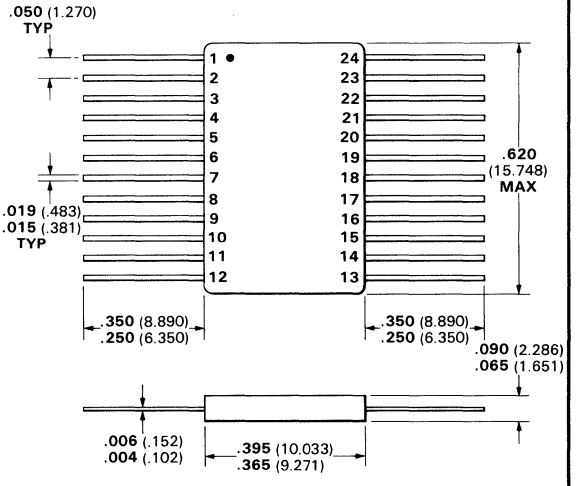
16-PIN BeO CERPAK



4L

NOTES:
Pins are alloy 42
Package weight is 0.4 gram
Hermetically sealed beryllia package

24-PIN CERPAK



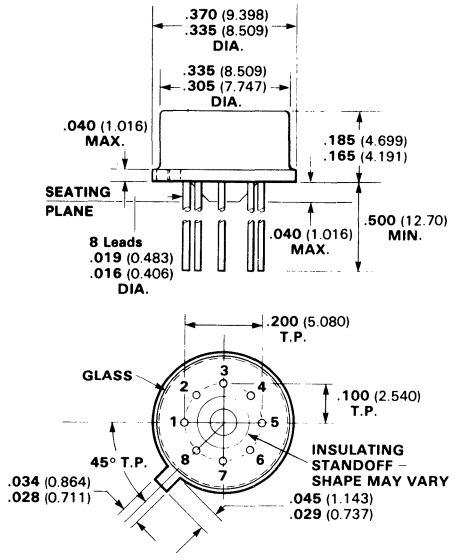
4M

NOTES:
Pins are tin plated nickel alloy
Base is Al_2O_3 or BeO
Cavity size is 200 x 200
Package weight is 0.8 grams

All dimensions in inches (bold) and millimeters (parentheses)

FAIRCHILD PACKAGE OUTLINES

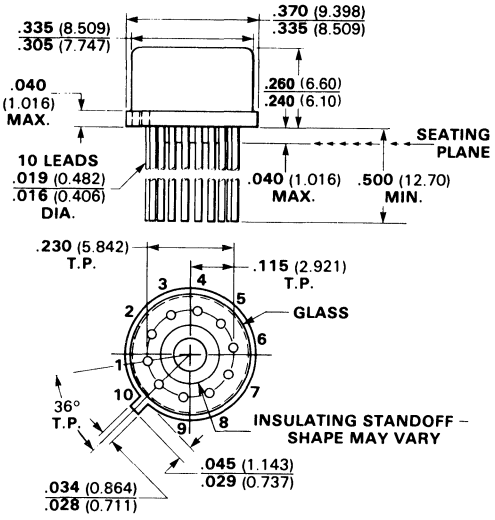
JEDEC TO-99 OUTLINE



5B

NOTES:
Leads are gold-plated kovar
Seven leads thru leads No. 4 connected to case
15 mil kovar header
Package weight is 1.22 grams

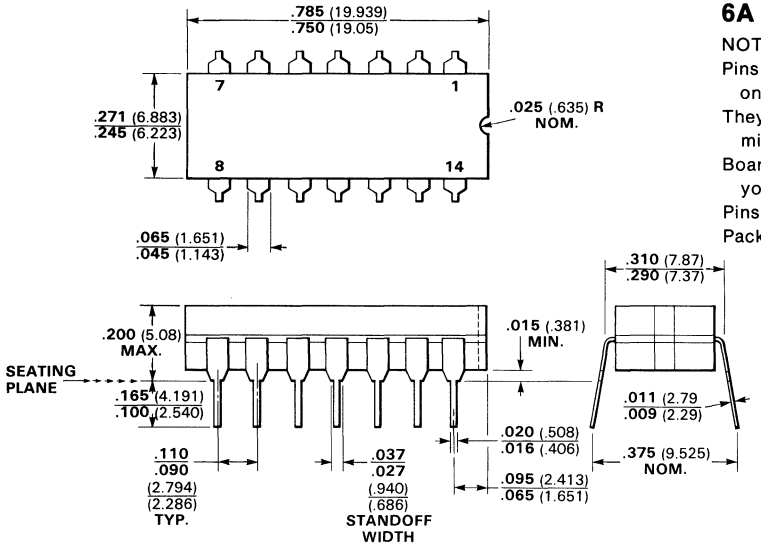
JEDEC TO-100 OUTLINE



5F

NOTES:
Leads are gold-plated kovar
Nine leads through, lead 5 connected to case
15 mil kovar header
Package weight is 1.32

14-PIN HERMETIC DUAL IN-LINE (JEDEC TO-116 OUTLINE)

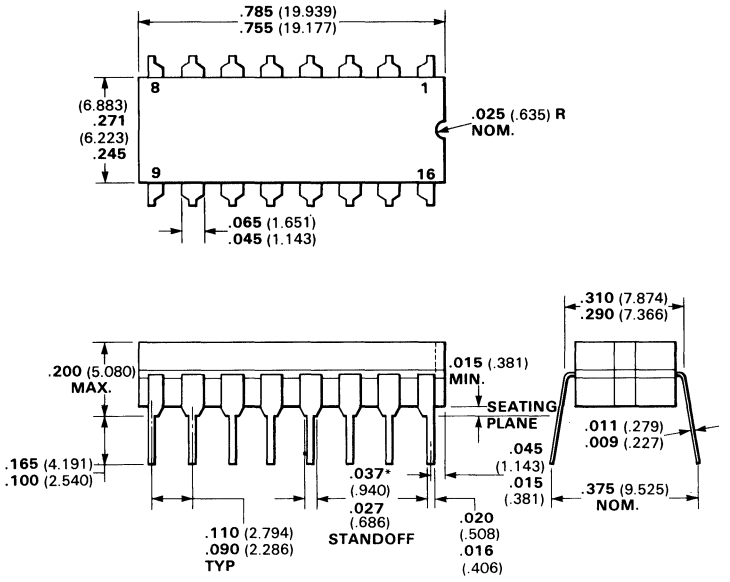


6A

NOTES:
Pins are intended for insertion in hole rows on .300" (7.620) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" (0.508) diameter pin
Pins are alloy 42
Package weight is 2.0 grams

All dimensions in inches (bold) and millimeters (parentheses)

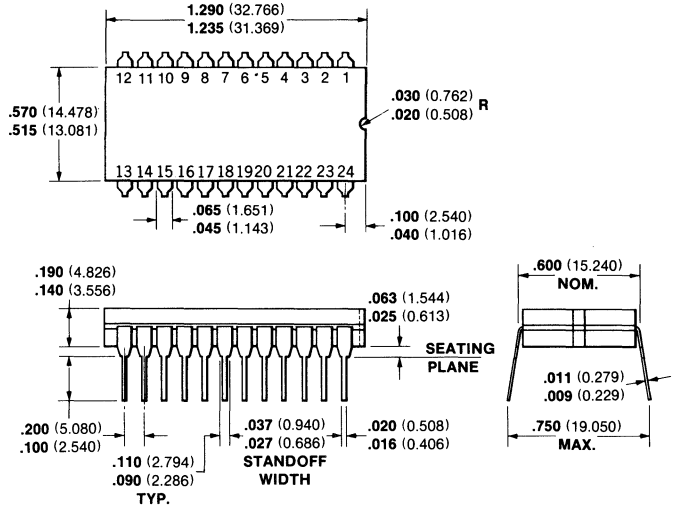
16-PIN DUAL IN-LINE



6B

NOTES:
Pins are tin-plated 42 alloy
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 (0.51) inch diameter pin
Hermetically sealed alumina package
Cavity size is .110 x .140 (2.79 x 3.56)
Package weight is 2.0 grams
*The .037-.027 dimension does not apply to the corner pins

24-PIN DUAL IN-LINE



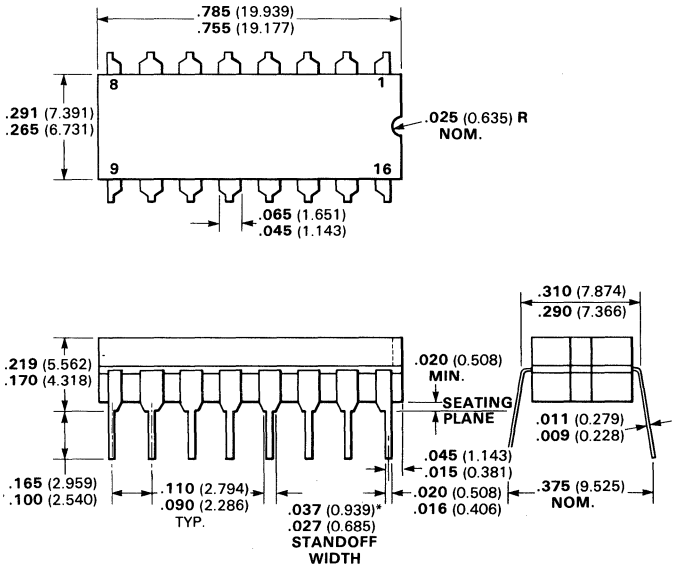
6N

NOTES:
Pins are tin-plated 42 alloy
Package material is alumina
Pins are intended for insertion in hole rows on .600 (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Cavity size is .230 x .230 (5.84 x 5.84)
Package weight is 6.5 grams

All dimensions in inches (bold) and millimeters (parentheses)

FAIRCHILD PACKAGE OUTLINES

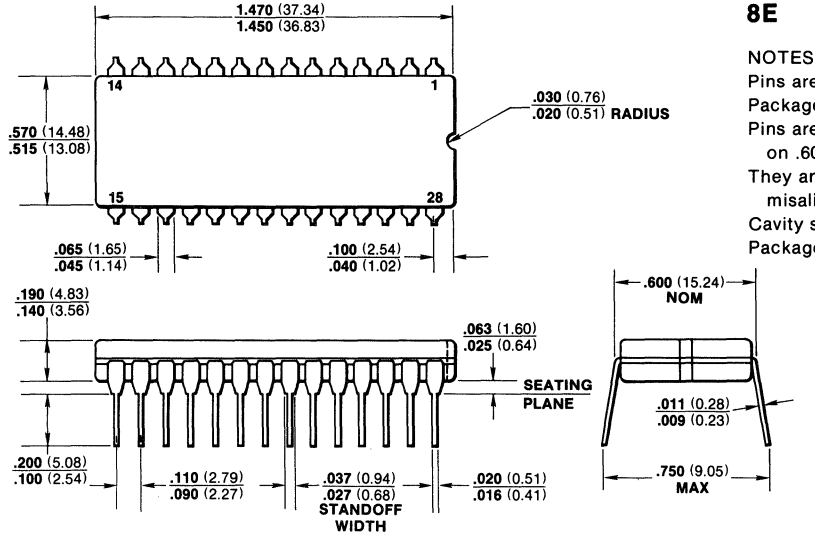
16-PIN DUAL IN-LINE



7B

NOTES:
Pins are tin-plated 42 alloy
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 (0.51) inch diameter pin
Hermetically sealed alumina package
Cavity size is .130 x .230
*The .037-.027 (0.94-0.69) dimension does not apply to the corner pins
Package weight is 2.2 grams

28-PIN DUAL IN-LINE SIDE-BRAZED

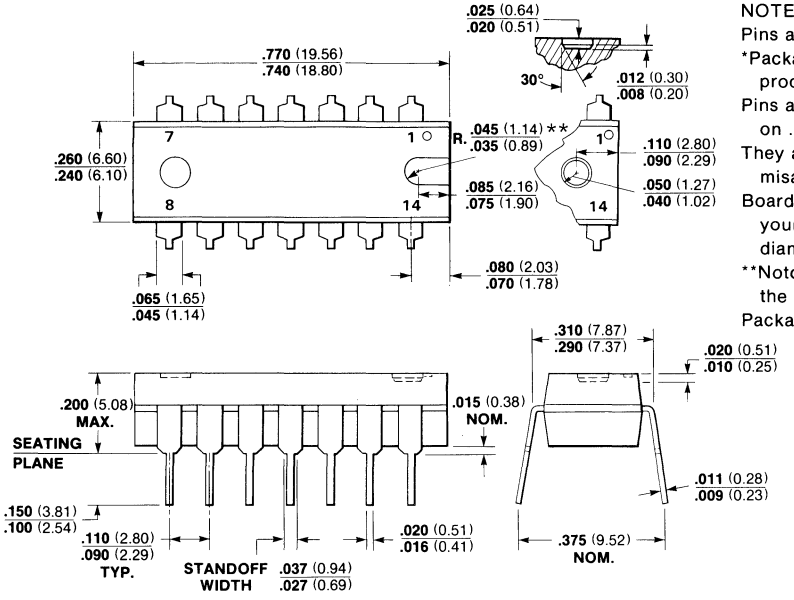


8E

NOTES:
Pins are tin-plated alloy 42
Package material is alumina
Pins are intended for insertion in hole rows on .600 (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Cavity size is .240 (6.095) x .240 (6.096)
Package weight is 7.5 grams

All dimensions in inches (bold) and millimeters (parentheses)

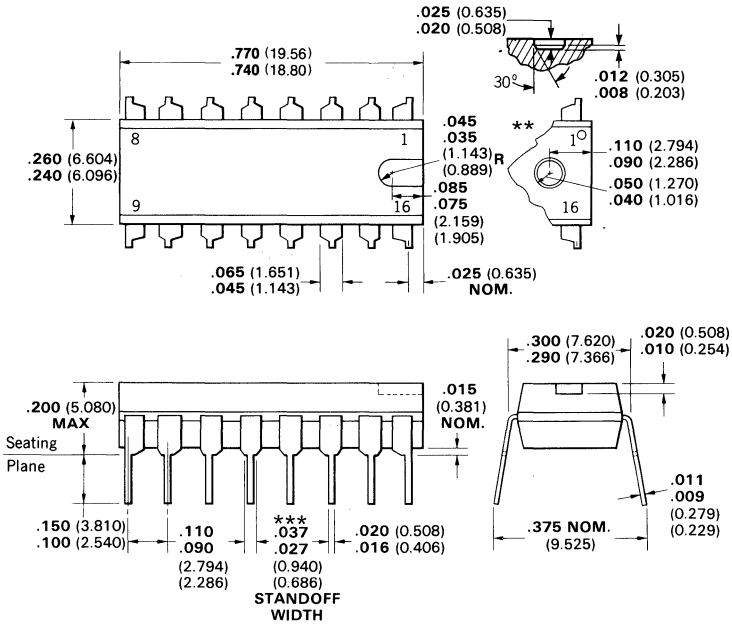
14-PIN *PLASTIC DUAL IN-LINE (JEDEC TO-116 OUTLINE)



9A

NOTES:
Pins are tin plated kovar
*Package material varies depending on the product line
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 (0.508) inch diameter pin
**Notch or ejector hole varies depending on the product line
Package weight is 0.9 grams

16-PIN PLASTIC* DUAL IN-LINE

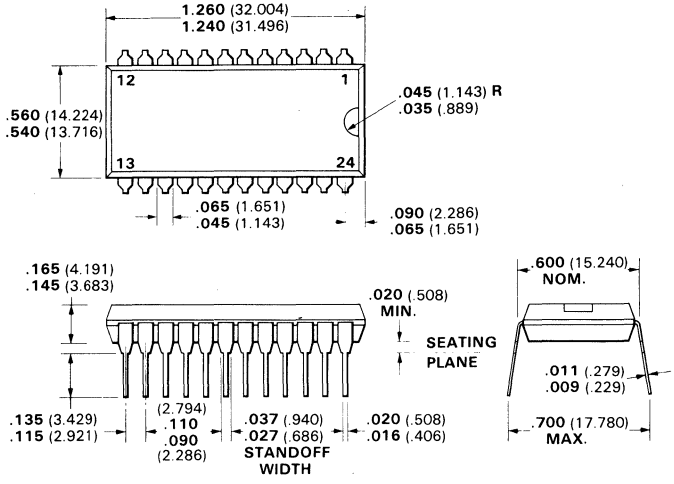


9B

NOTES:
Pins are tin-plated kovar or alloy 42 nickel
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .0210 (0.51) centers diameter pin
Package weight is 0.9 gram
*Package material varies depending on the product line
***The .037-.027 (0.94-9.69) dimension does not apply to the corner pins
***Notch or ejector hole varies depending on the product line

All dimensions in inches (bold) and millimeters (parentheses)

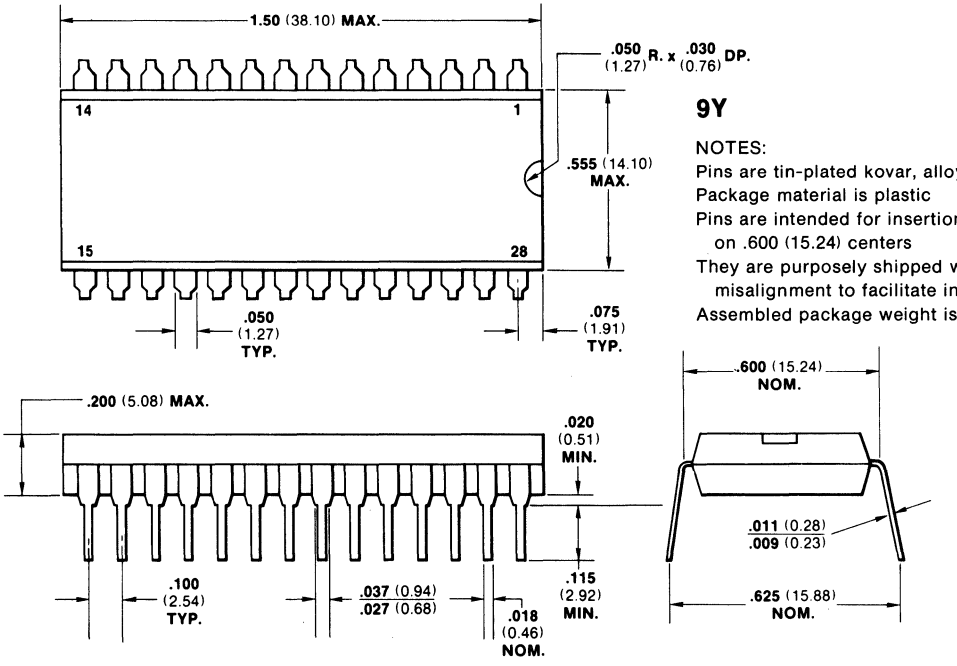
24-PIN PLASTIC DUAL IN-LINE



9N

NOTES:
Pins are tin-plated kovar
Package material is plastic
Pins are intended for insertion in hole rows on .600 (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion

28-PIN PLASTIC DUAL IN-LINE

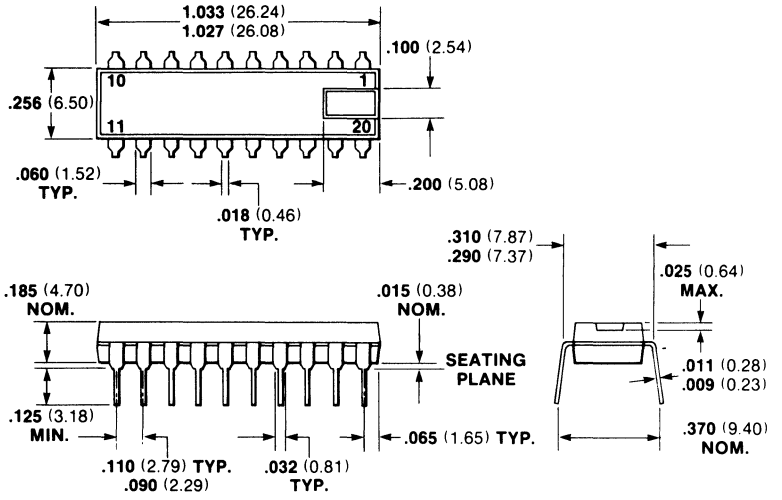


9Y

NOTES:
Pins are tin-plated kovar, alloy 42 or copper
Package material is plastic
Pins are intended for insertion in hole rows on .600 (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Assembled package weight is 4.8 grams

All dimensions in inches (bold) and millimeters (parentheses)

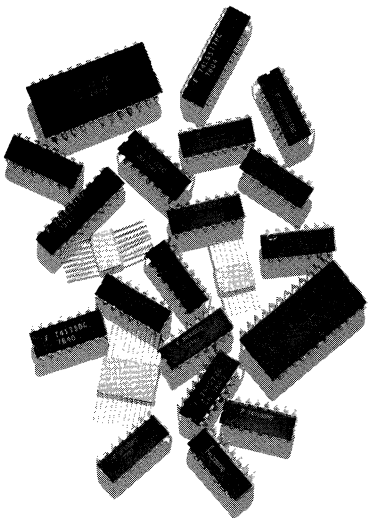
20-PIN PLASTIC DUAL IN-LINE



9Z

NOTES:
Pins are tin plated alloy 42 or copper (olin 195)
Package material varies depending on the product line
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board drilling dimensions should equal your practice for .020" (0.51) diameter pin
Package weight is a little over 1.0 gram

All dimensions in inches (bold) and millimeters (parentheses)



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